Electromagnetic Transient Simulation Tools for Aiding the Short Circuit Analysis of Power Systems with Inverter-Interfaced Resources

by

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Abstract

Some utilities with high penetration of inverter-interfaced resources (IIRs) tend to maintain their power system models in the form of electromagnetic transient (EMT) simulation models. Evaluation of busbar fault levels under various system configurations is often required and obtaining fault current through repeated EMT simulations is time consuming when high accuracy is not a concern. Since all network data is already available in the EMT model, it would be very convenient for study engineers if conventional short circuit analysis can be performed in the EMT environment. Recognizing this need, a tool for performing busbar short circuit analysis was developed for PSCAD EMT simulation software environment employing PSCAD Initializer and Python programming language. The developed automated calculation methodology provides short circuit solutions in compliance with ANSI/IEEE and IEC standards.

The increase of IIRs integrated directly to transmission grids alters the short circuit behavior of networks and the characteristics of fault currents. This is because the power electronic converters limit the short circuit currents to protect the semiconductor devices in the converters. In order to incorporate this nonlinear behavior of IIRs during the faults, an iterative short circuit analysis algorithm is presented to obtain the correct phasor solution. The methodology employs a voltage dependent network equivalent (VDNE) to represent a subsystem with high penetration of IIRs in the phasor domain short circuit calculation process. The proposed VDNE utilizes a voltage dependent current source to capture the nonlinear behavior of the IIRs and the VDNE parameters are derived by repeatedly simulating a detailed EMT model of the portion of network with IIRs. An automated process for obtaining VDNE parameters is implemented in PSCAD using a Python script. The results of the proposed VDNE based iterative short circuit analysis are validated by comparing with the short circuit results obtained through EMT simulations of the complete power system with IIRs. The results obtained for two different test systems, a radial 7-bus system and the IEEE 39-bus system, showed that the iterative short circuit is reasonabaly accurate for three-phase faults.

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Dedication

To my beloved parents and family

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AL	Automation Library
BESS	Battery Energy Storage System
DFIG	Doubly Fed Induction Generator
EMT	Electro-Magnetic Transients
EPRI	Electric Power Research Institute
FFT	Fast Fourier Transform
FRT	Fault Ride-Through
GSC	Grid Side Converter
GUI	Graphical User Interface
HV	High Voltage
IBR	Inverter-Based Resources
IIR	Inverter Interfaced Resources
LV	Low Voltage
LVRT	Low Voltage Ride-Through
MSC	Machine Side Converter
MV	Medium Voltage
PGC	Point of Generator Connection
PMSG	Permanent Magnet Synchronous Generator
PoI	Point of Interconnection
PSCAD/EMTDC	Power System Computer Aided Design/ Electromagnetic Transient with DC
PSS/E	Power System Simulation for Engineering

SG	Synchronous Generator
SPP	Solar Power Plant
TD	Time-domain
VDNE	Voltage Dependent Network Equivalent
WECC	Western Electricity Coordination Council
WPP	Wind Power Plant
WTG	Wind Turbine Generator

Chapter 1

Introduction

1.1 Background

Power system analysis is essential for planning and designing of electric power systems, and then to ensure their economic and stable operation. Several fundamental analysis techniques such as power flow analysis, short circuit analysis, stability analysis, electromagnetic transient analysis, etc. form the basis of numerous types of design and operational studies. Among these, short circuit analysis is performed to examine the system behavior under faulty conditions. The results of short circuit analysis are essential for many tasks such as sizing electrical equipment, verifying acceptable ratings of the equipment, and setting protection relay functions.

The method of short circuit analysis is well established for power systems with conventional synchronous generators (SGs). Due to the rapid advancement of power electronic based converter technology, an increasing number of large-scale wind and solar farms are integrated directly into the transmission grids, with wind energy having a higher share of the two renewable energy technologies [1]. As the level of penetration increases, interconnecting wind power plants (WPPs) and solar power plants (SPPs) into the power grid has become a major issue and the topic has been a matter of interest among the power system engineers.

The evolution of wind power technology has paved the way for better steady-state and dynamic performance and the need of standardized simulation models for interconnection studies became crucial. Initially, the dynamic simulation models of wide variety of wind turbine generators (WTGs) utilized were mostly developed by the manufacturers. These models were incompatible with regional planning and reliability assessment, and to address this issue, the Western Electricity

Coordination Council (WECC) Modeling and Validation Work Group was set up. This working group came up with a classification that grouped the commercially available WTGs into four main types based on the rotor mechanism and power structures as follows [2]-[3].

Type I: Fixed speed induction generator

Type II: Variable slip induction generator

Type III: Doubly fed induction generator (DFIG)

Type IV: Variable speed full converter

In Type I and II WTGs, induction generators are directly connected to the power system and therefore, they can be accurately modeled in the conventional short circuit analysis methods. However, in modern large-scale wind farms, Type III and IV WTG topologies are preferred over Type I and II due to high flexibility, efficiency, and more independent control structure [4]. In Type III, the rotor circuit of the variable speed DFIG is interfaced to the network through two converters (AC/DC and DC/AC) whereas in Type IV, the variable speed generator, which could be induction or permanent magnet synchronous type, is interfaced through converters. Type IV WTGs are becoming more common now due to additional flexibility in control and reduction in the cost of semiconductor devices. From the grid interface point of view, solar power plants and battery energy storage systems (BESS) are similar to Type IV WTGs.

In terms of fault current behavior, renewable energy and energy storage systems interfaced through converters, often referred to as inverter-based resources (IBR) or inverter-interfaced resources (IIRs), are inherently different from the SGs. During a disturbance, the power electronic converters inject controlled currents to the grid. The injected current magnitudes are limited to the rating of the converter to protect the semiconductor equipment [5]-[6]. Moreover, many converter controllers have negative sequence current control capability that would reduce or eliminate the negative sequence short circuit current component. The complete elimination of negative sequence current is feasible with Type IV WTGs, although the capability of suppressing negative sequence currents in Type III is limited due to the presence of the rotor voltage [7]. These controller actions cause deviation of short circuit current characteristics from conventional SGs, and modifications to the protection systems, which are developed based on the typical fault current characteristics, are required to selectively clear faults in the power systems with IIRs.

In the earlier period, IIRs were allowed to disconnect from the network during fault events due to their minor contribution to the recovery from disturbances compared to conventional power generation. However, with increasing penetration, IIRs have a major impact on power system reliability and stability [8], and the system operators introduced a set of requirements through the grid codes to ensure a supporting action from IIRs. For example, according to the recent Manitoba Hydro transmission system interconnection requirements, the WTGs are expected to remain in service and support the grid voltage during balanced and unbalanced short circuit faults as per the low voltage ride-through characteristics. The low voltage ride-through characteristics at the interconnection point of an existing WTG are illustrated in Figure 1.1.

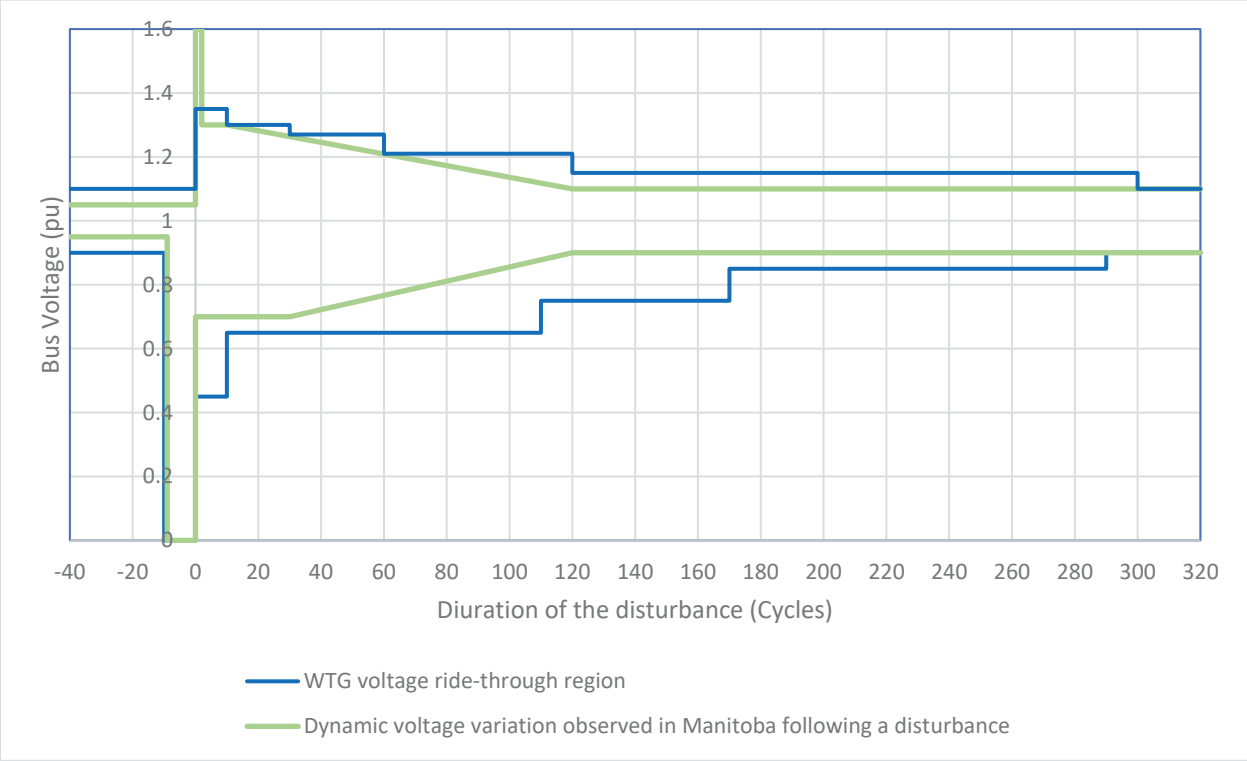

Figure 1.1 Manitoba Hydro transient voltage performance characteristics following a disturbance with WTG voltage ride-through characteristics [9]

There are two regions, the green region for Manitoba Hydro transient voltage performance criteria and the blue region for WTG voltage ride-through. According to the grid code recommendations, the individual WTGs are expected to remain connected to the power system inside the blue and green regions. The WTGs are not permitted to trip inside the blue region, but reduced power

generation is permitted. Tripping is permitted outside of the blue region. When the voltage recovers from the blue to green region, the WTG power output will restore to its nominal value. To comply with the grid code requirements, converter control systems need to inject various amounts of active and reactive currents that depend on the terminal voltage and time from the initial voltage dip due to a fault. In order to account for these controlled current injections from IIRs, several modeling and calculation approaches have been proposed by the developers of short circuit analysis programs [10].

Grid short circuit analysis can be accomplished in two different ways: dynamic simulations, and short circuit analysis. Time-domain (TD) simulations provide more detailed and accurate results of the power system for both steady-state and dynamic system conditions. The comprehensive dynamic simulation model also offers the ability to observe the system response under the effect of specific control modes. But TD analysis method has two major drawbacks: long execution time and requirement of detailed models with fine tuned control parameters. The WTG models often tend to be proprietary and only disclosed to grid operators under confidential terms. In contrast, the short circuit analysis is a simple and fast calculation strategy where the contributing sources can be adequately represented by their approximate models. In this context, where short circuit analysis is preferred over TD simulations [11].

According to IEC and ANSI standards [12] that provide guidelines for short circuit studies, the SGs are represented as constant voltage sources behind an impedance [11]. The same assumptions are not valid for IIRs since they inject controlled active and reactive currents to the power grid during a short circuit event [4]-[6]. An accepted modeling approach is to represent the WTG as a voltage controlled current source and to observe the response through an iterative solution. The conventional short circuit analysis is a one-step solution for the linearized network. But the nonlinear behavior of WTG controls requires an iterative solution taking into account the WTG control actions [13]-[14].

Recognizing the importance of fast and accurate short circuit programs, a number of studies have been conducted to establish calculation methodology for IIR connected to the power grid. In an effort to consolidate these methodologies, IEEE PES working group named “Modification of Commercial Fault Calculation Programs for Wind Turbine Generators” compiled a report describing the issues, the methods used by short circuit program developers to accommodate the

short circuit models for Type III and IV WTGs, and a possible approach for WTG manufacturers to provide data required for the models without revealing the details of controllers [14].

1.2 Problem Statement

In the recent years, alternative methods have been developed to accommodate the response of IIRs in short circuit current calculations. In a grid containing a high penetration of IIRs, TD simulations are mostly recommended for studies due to accuracy and detailed response. The well-known Electromagnetic transient (EMT) modeling is the benchmark technique often used in the power industry to validate protection and control designs. Details of the IIR models are generally not public as various control algorithms remain trade secrets, and the models are often provided as simplified versions or black box models on the software platform used. These black boxed models mask the model details but produce input output relations.

A set of differential equations are utilized in EMT modeling, and therefore simulation of a complex power system is a computationally demanding process. In order to calculate fault currents using TD simulation, the model needs to simulate until it settles at the pre-fault steady-state condition, and then apply the fault and continue the simulation. This is a time-consuming process, especially when electrical machines and prime movers such as wind turbines are modeled in the system.

However, when performing a short circuit analysis during an early stage of planning or design process, a simple yet reasonably accurate methodology is required. Iterative short circuit analysis is an emerging technique where the portion of the system with IIR is modeled as a voltage dependent equivalent source in a conventional short circuit program. The convergence and accuracy of these approaches are yet to be tested thoroughly. Most of the previous studies have been carried out utilizing a simplified Thévenin equivalent for the grid models [6],[15]-[16]. Therefore, there is a need to examine the convergence properties and accuracy when the grid is represented in detail in the short circuit analysis. On the other hand, the fault currents are dependent on the converter operating mode, low voltage ride-through (LVRT) characteristics, and the activation of internal controls. Therefore, obtaining a proper voltage dependent equivalent source is also a challenging task that requires numerous simulation runs. If the process of obtaining

voltage dependent equivalent source can be automated, considerable engineering time can be saved.

Some utilities maintain EMT models of the large networks. It is often required to evaluate approximate busbar fault levels under various system configurations, and this demands repeated EMT simulations with one fault at a time. When high accuracy is not a concern, conventional short circuit analysis is much faster, but requires the use of a separate computer program. Switching between programs can also result in discrepancies in the input data files. Since all the network data is already available in the EMT model, it would be very convenient for study engineers if conventional short circuit analysis can be performed in the EMT environment. But currently, such a facility is not available in common EMT simulation programs.

1.3 Research Motivation

Although short circuit analysis methodology is well established for Type I and II WTG models that of Type III and IV WTG models is still an emerging topic. On the other hand, the WTG manufacturers use PSCAD software, which is a widely used EMT simulation program, to develop and test their WTG models and control algorithms. These models and control algorithms are usually manufacturer specific, and often customized to a given site to meet the applicable grid code. The control models are not disclosed but black-boxed models in PSCAD/EMTDC format are provided to the clients. These black-box models incorporate realistic controls, different operating modes, and various internal protection mechanisms to represent the accurate behavior of WTGs in grid planning and protection studies. Using these EMT models to develop voltage dependent network equivalents that can be used with short circuit programs has the potential to improve the accuracy of the short circuit calculation. There is also a potential for saving engineering time by automating the process of building voltage dependent network equivalents. Similarly, a tool for performing conventional short circuit analysis in PSCAD/EMTDC simulation environment, which is heavily used for IIR integration and other studies would be very useful for study engineers.

1.4 Research Objectives

The overall goal of the proposed research is to develop methods and tools to improve the accuracy of fault current calculations in power systems with high penetration of IIRs. The research particularly explores the use of iterative short circuit calculation procedures and the feasibility of automating EMT type simulations that accurately model the nonlinear behavior of inverter-interfaced generation to obtain nonlinear network equivalents that represent the inverter-interfaced generation in such algorithms. The particular EMT simulation environment considered is PSCAD/EMTDC and the Python programming language is considered for automation and implementing short circuit calculation procedures. To achieve the main goal of the research study, following sub objectives are proposed.

1. Review of methods prescribed in various standards for fault current calculations in power systems and the algorithms proposed for incorporating IIR in fault analysis.
2. Automation of PSCAD/EMTDC to extract information required for fault analysis from an EMT model of a conventional power system.
3. Development of a sequence domain short circuit analysis program in Python and verification of its accuracy.
4. Derivation of a mathematical framework to obtain a voltage dependent network equivalent (VDNE) to represent a portion of a power system with IIR and automation of PSCAD/EMTDC to derive VDNE parameters from a detailed model of the concerned part of the power system.
5. Development and implementation of an iterative fault analysis algorithm that incorporates nonlinear VDNE representing the portion of the power system with IIR, and its validation.

1.5 Thesis Organization

The thesis is structured as follows:

Chapter 2 includes a literature review on Type IV WTG model and the existing short circuit analysis methodologies.

Chapter 3 describes the automated calculation of busbar fault current analysis in PSCAD/EMTDC environment. The method is discussed for bus bar symmetrical and asymmetrical short circuit analysis.

Chapter 4 proposes an iterative short circuit analysis method on Type IV WTG models and presents results of case studies to validate the proposed methods.

Chapter 5 summarizes the research and presents the research conclutions, contributions and future work.

Chapter 2

Literature Review

The penetration of IIRs to the complex transmission network has been increasing recently, resulting in technical challenges on power system protection. The short circuit behavior of an IIRs is predominantly different from the conventional synchronous generators due to the converter interface and associated current limits. EMT simulation tools provide short circuit behavior of the IIRs with high precision. Even though EMT simulations provide detailed short circuit behavior of the system, the process requires comprehensive modeling of the equipment. However, phasor domain short circuit analysis is preferred in the early stage of analysis for protection and planning studies. In this context, developing an accurate phasor model is crucial. Recognizing this industry gap, several phasor domain short circuit analysis models are developed and successfully used in the power system protection sector.

The rest of this chapter is organized as follows: First, an introduction to the conventional short circuit analysis methodology for balanced and unbalanced faults is provided. Then the short circuit behavior of a power network in the presence of IIRs is discussed. The next few sections of this chapter discuss about the approaches used for short circuit analysis of systems with IIRs by several commercial short circuit programs and the Electric Power Research Institute (EPRI). Finally, a comprehensive review of the voltage dependent current source equivalent models utilized for iterative short circuit analysis is presented.

2.1 General Short Circuit Current Calculation

Short circuit analysis which determines the steady-state solution of a liner network is essential for power system design. It is utilized to determine, fault currents, bus voltages, and line currents

during different types of faults. The types of faults are divided into two categories: balanced three-phase faults and unbalanced faults. The information gained by the short circuit analysis is then used to design the network, determine new equipment ratings, determine the settings of protection relays, and analyse the existing systems to verify the acceptable equipment ratings. Different organizations in the world adopt several standards such as IEEE standards, ANSI standards, IEC standards, Chinese standards, and Russian standards for short circuit analysis. These standards adopt a similar short circuit calculation methodology, but with different equipment modeling techniques and pre-fault operating conditions [11].

There are several factors that determine the magnitude and the duration of the short circuit such as the type of the fault, fault current sources, and the impedance between the source and the point of the short circuit. In order to calculate short circuit current with a reasonable degree of accuracy, an equivalent circuit should be created where each element is modeled with sufficient details to represent its performance under short circuit conditions.

Simplifications for the short circuit analysis techniques have been developed due to the fact that solving complex differential equations representing dynamic characteristics of the system is rather complex. One such simplification is that the driving voltage and the phase angle remain unchanged during a short circuit condition. In reality, the internal voltage of the machine varies with time and the loading of the machine. Then the machine's internal voltage reduces faster, and the energy supplied by the machine becomes insufficient to restore the voltage to its steady-state value. The angles between machines will also be affected under a disturbance, where some of the machines begin to accelerate and some begin to slow down [11].

Dealing with many varying voltage sources is a computationally complex process. In addition, the machine impedances remain constant based on their physical design. It is explicitly stated in [11] that the same fault current can be computed by varying the machine impedance and holding the voltage constant at the pre-fault value. The impedance value depends on the fault current duty. The ANSI standards define three types of fault currents according to three distinct time periods; first-cycle currents occur up to one cycle immediately after the inception of the fault, interrupting currents falling within the time window of 1.5 to 4 cycles, and steady-state currents relevant to 30 cycles and beyond. According to the explanation of fault current duty, the first cycle criteria is

associated with a lower machine impedance, and hence a higher short circuit current magnitude, than the equipment evaluated on interrupting or steady-state duty.

For the purpose of fault studies, the machine behavior under short circuit conditions is divided into three categories: the subtransient, transient and steady-state period. The subtransient period lasts only for the first few cycles and the subtransient impedances are primarily used for first-cycle duty calculation.

2.1.1 Balanced Faults

A balanced three-phase fault is a fault where all the three phases are affected simultaneously. There are two types of balanced faults: three-phase faults and three-phase to ground faults. However, both types of faults produce similar currents if the network is ideally balanced. Since the network remains balanced during a three-phase balanced fault, they are analysed on a per-phase basis. The three-phase faults occur rarely, but these are the most severe type of faults which results in the largest fault current.

The following simplifying assumptions are made upon the general short circuit analysis [11]:

1. The ac system frequency remains unchanged at the rated fundamental system frequency.
2. The machine driving voltages are fixed for the duration of the faults.
3. The pre-fault load currents are ignored assuming that they are negligibly smaller compared to the short circuit current magnitudes.
4. The pre-fault voltages of the system are assumed to be rated system voltages.
5. The fault current contribution from induction and synchronous motors are considered as their magnitudes vary upon the inception of the fault.

In order to describe the three-phase fault calculation procedure, consider an n bus power system operating under balanced conditions. The generators of this power system will be represented by constant voltage sources behind their reactances which may be either direct axis subtransient reactance, X''_d, direct axis transient reactance, X'_d, or direct axis reactance, X_d. The fault is to be at bus r through a fault impedance Z_r and the pre-fault bus voltages are obtained through a power flow analysis. The pre-fault bus voltage vector is represented by,

$$V_{BUS}(0) = \begin{bmatrix} V_1(0) \\ \vdots \\ V_r(0) \\ \vdots \\ V_n(0) \end{bmatrix} \tag{2.1}$$

Assume that the bus current injection matrix is expressed as I_{BUS}. The bus current injection vector and the bus voltage vector are related through the bus admittance matrix Y_{BUS} or the bus impedance matrix Z_{BUS} as:

$$\begin{aligned} I_{BUS} &= Y_{BUS} \cdot V_{BUS} \\ V_{BUS} &= Z_{BUS} \cdot I_{BUS} \end{aligned} \tag{2.2}$$

During a fault, the fault current injection to the faulted bus r is $I_r(F)$. Since the fault current is leaving the bus, it is expressed as a negative current injection. Fault current injection to every other bus becomes zero. Thus, the fault current injection vector is,

$$I_{BUS}(F) = \begin{bmatrix} 0 \\ \vdots \\ -I_r(F) \\ \vdots \\ 0 \end{bmatrix} \tag{2.3}$$

After the inception of the fault, the change in bus voltages due to the fault is,

$$\Delta V_{BUS} = \begin{bmatrix} \Delta V_1 \\ \vdots \\ \Delta V_r \\ \vdots \\ \Delta V_n \end{bmatrix} \tag{2.4}$$

The change in the bus voltages due to fault currents can be computed as:

$$\Delta V_{BUS} = Z_{BUS} \cdot I_{BUS}(F) \tag{2.5}$$

Applying superposition theorem to obtain the bus voltages during the fault,

$$\mathrm{V_{BUS}(F)} = \mathrm{V_{BUS}(0)} + \Delta\mathrm{V_{BUS}} \tag{2.6}$$

By substituting for ΔV_{BUS} it is possible to obtain post fault bus voltage vector as:

$$\mathrm{V_{BUS}(F)} = \mathrm{V_{BUS}(0)} + \mathrm{Z_{BUS}} \cdot \mathrm{I_{BUS}(F)} \tag{2.7}$$

Thus, the fault current results in change in voltage at the faulted bus *r* to $V_r(F)$ is given by,

$$\mathrm{V_r(F)} = \mathrm{V_r(0)} - \mathrm{Z_{rr}I_r(F)} \tag{2.8}$$

If the fault impedance is Z_f, the fault voltage at the bus *r* can be alternatively expressed as,

$$\mathrm{V_r(F)} = \mathrm{Z_f I_r(F)} \tag{2.9}$$

Substituting for $V_r(F)$ in (*2.8*) from (2.9) and solving for the fault current $I_r(F)$,

$$\mathrm{I_r(F)} = \frac{\mathrm{V_r(0)}}{\mathrm{Z_{rr}} + \mathrm{Z_f}} \tag{2.10}$$

The balanced three-phase current calculation only requires the Thévenin impedance Z_{rr} as viewed from the faulted bus, fault impedance, and the pre-fault voltage at the faulted bus. Once the fault current is computed in (*2.10*), bus voltages during the fault can be computed from (*2.7*). Also, three-phase fault does not have negative or zero sequence current components, and therefore, only the positive sequence data is required for the analysis.

2.1.2 Unbalanced Faults

Unbalanced or asymmetrical faults can be categorized as: single-phase-to-ground faults, line-to-ground faults, and double line-to-ground faults. These faults are, in fact, the more common types of faults than balanced three-phase faults. The reference [17] states the typical frequency of occurrences of faults in a power system. The frequencies of occurrences are:

Single-phase to ground faults 70%

Double line faults 15%

Double line-to-ground faults 10%

Three-phase balanced faults 5%

The analysis under unbalanced system conditions has to be carried out on three-phase basis and hence the concept of symmetrical components is applied to resolve the unbalanced system. The unbalanced fault calculation methodology requires to obtain separate bus impedance matrices for positive, negative, and zero sequence networks.

The unbalanced fault current calculation procedure also begins with a power flow analysis to determine the pre-fault bus voltages. Assume that the fault happens at bus *r,* and $V_r(0)$ is the pre-fault voltage at the faulted bus *r.* Then the r^{th} diagonal element in each of the bus impedance matrix is the Thévenin impedance seen at the fault point *r* for the respective sequence. The sequence Thévenin impedances, $Z_{rr0}, Z_{rr1}, Z_{rr2}$, are then connected according to the types of faults to obtain the sequence fault currents and fault voltages in the power network. The unbalanced fault current formulas are summarized below.

Single-Phase-to-Ground Fault

This is the most common type of fault that will occur in a power system. Figure 2.1 illustrates the model single-phase to ground fault considered. The fault occurs between phase *A* and ground through an impedance Z_f. Thus, the symmetrical components of the fault current and the fault current are:

$$I_{r0} = I_{r1} = I_{r2} = \frac{V_r(0)}{Z_{rr0} + Z_{rr1} + Z_{rr2} + 3Z_f} \qquad (2.11)$$

$$I_r(F) = 3I_{r0}$$

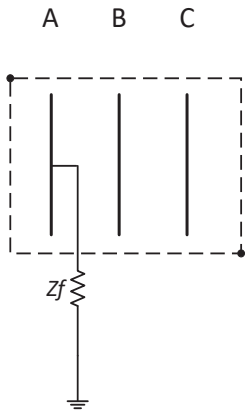

Figure 2.1 Single-phase-to-ground fault at bus r

Line-to-Line Fault

Figure 2.2 illustrates the model of a line-to-line fault at bus *r*. The fault occurs between phase *B* and *C* through an impedance Z_f. The symmetrical components of the fault current and the fault current are:

$$I_{r0} = 0$$

$$I_{r1} = -I_{r2} = \frac{V_r(0)}{Z_{rr1} + Z_{rr2} + Z_f} \tag{2.12}$$

$$I_r(F) = -j\sqrt{3}I_{r1}$$

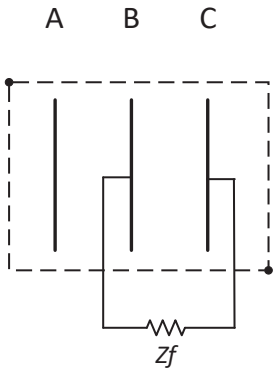

Figure 2.2 Line-to-line fault at bus bar r

Double Line-to-Ground Fault

Figure 2.3 illustrates the model of a double line-to-ground fault at bus *r*. The fault occurs between phase *B* and *C* and then connected to the ground through an impedance Z_f. The symmetrical components of the fault current and the fault current are:

$$
\begin{aligned}
I_{r1} &= \frac{V_r(0)}{Z_{rr1} + \dfrac{Z_{rr2}\,(Z_{rr0} + 3Z_f)}{Z_{rr2} + Z_{rr0} + 3\,Z_f}} \\
I_{r2} &= \frac{V_r(0) - Z_{rr1} I_{r1}}{Z_{rr2}} \\
I_{r0} &= \frac{V_r(0) - Z_{rr1} I_{r1}}{Z_{rr0} + 3Z_f} \\
I_r\,(F) &= 3I_{r0}
\end{aligned}
\tag{2.13}
$$

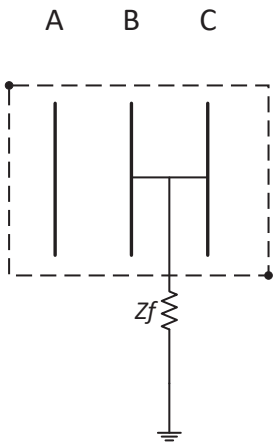

Figure 2.3 Double line-to-ground fault at bus r

2.2 Nature of Fault Currents from Induction Generators and IIR

The early stages of wind and solar power development were mostly off-grid applications. With the rapid development of grid integration technology, grid connected WTGs have become a significant source of power generation. The existing utility scale WTs are often sized above 1 MW. A key

aspect of planning a WPP is the evaluation of its short circuit current contribution in an event of a power system disturbance. The availability of different types of WTGs from different manufacturers imposes a major challenge upon computing short circuit currents. Unlike the magnetizing flux of conventional SGs which is controlled by the field current and sustain for the duration of the fault, the magnetizing flux of induction generators depletes during the fault and hence the fault currents are not sustainable for a long-time duration.

2.2.1 Type I WTG – Fixed-Speed Induction Generator

Type I WTG, shown schematically in Figure 2.4, is the earliest and the most basic utility scale WTG and it employs a squirrel cage type induction generator with a fixed speed wind turbine. The generator is directly coupled to the power grid via a generator transformer which is equipped with switched capacitor banks for power factor compensation. Several steps of these capacitors are switched according to the operating speed of the turbine shaft. The type I WTG produces power when the rotor is made to rotate at a speed greater than the synchronous speed and this difference between the operating speed and the synchronous speed is called slip. The fixed speed induction generator WTs operate with less than 1% rotor speed variation.

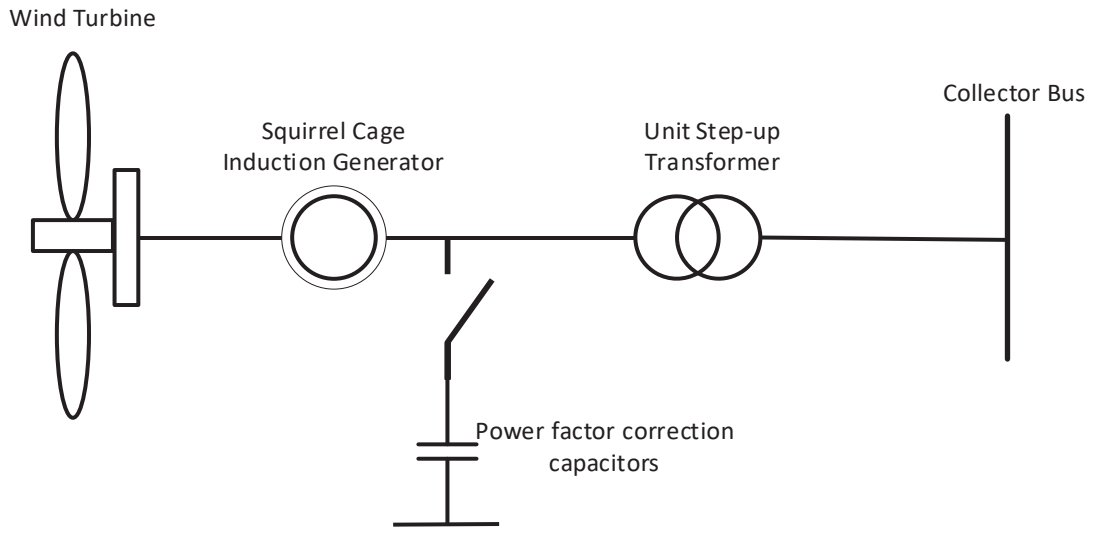

Figure 2.4 Basic structure of a Type I WTG

The transient simulation response of Type I WTG depicted in Figure 2.5 clearly indicates a significant fault current contribution from the fixed speed induction generators which is mainly governed by the electromagnetic configuration of the generator. The waveforms are shown for a Type I WTG connected to an infinite bus. The fault is applied at the terminal of the WTG. The voltage drops to zero at the fault inception time. The fault current contribution from the Type I WTG during the first cycle has reached as high as 14 pu calculated on WTG MVA base (1.816 MVA). As the fault continues, the fault current magnitude starts decreasing. In addition, the rate of decay of the induction generator short circuit current depends on the type of the fault where three-phase to ground fault accounts for the fastest decay rate.

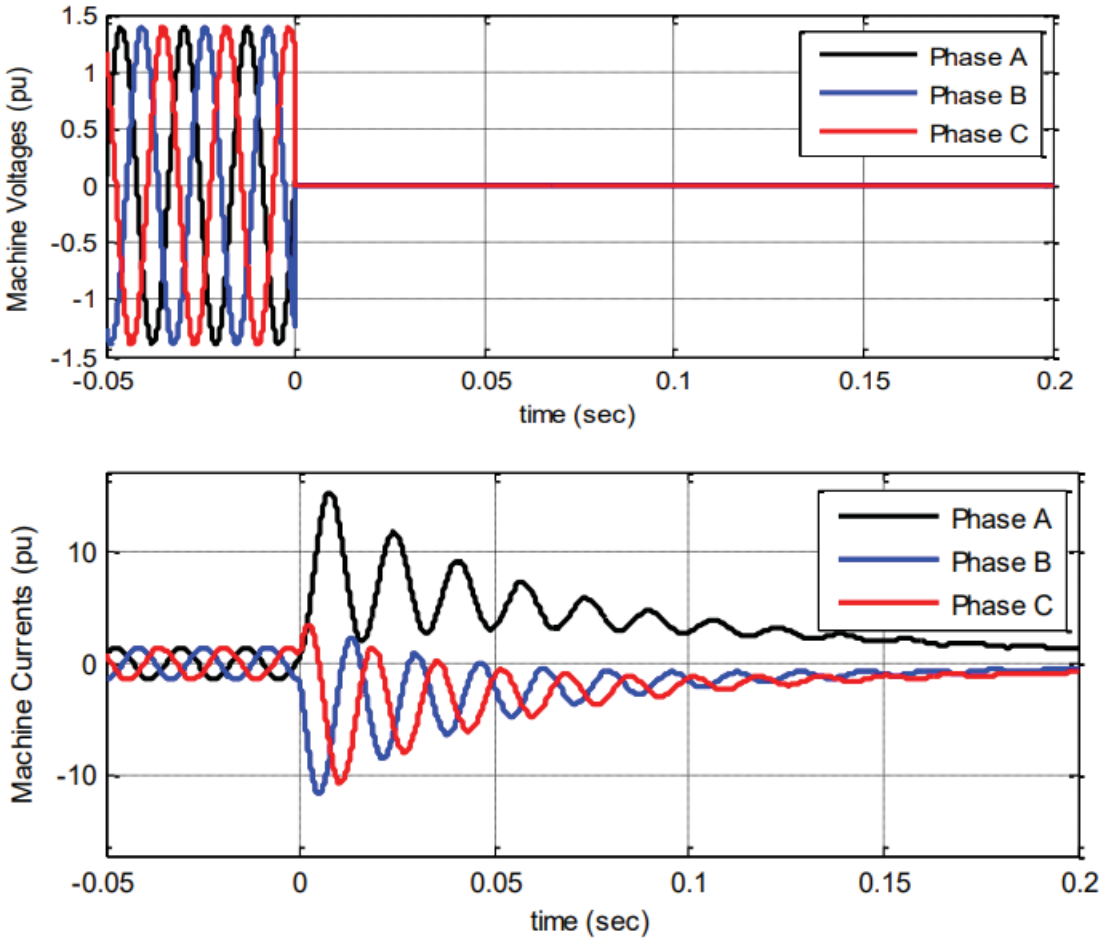

Figure 2.5 Type I WTG terminal bus voltage and current waveform for three-phase-to-ground fault [18]

Figure 2.6 depicts a line-to-ground fault applied at the terminal of the WTG and the faulted phase is phase A. The magnitude of the fault current reaches approximately 10 pu calculated on WTG MVA base (1.816 MVA) which is lower than the fault current magnitude of three-phase-to-ground fault.

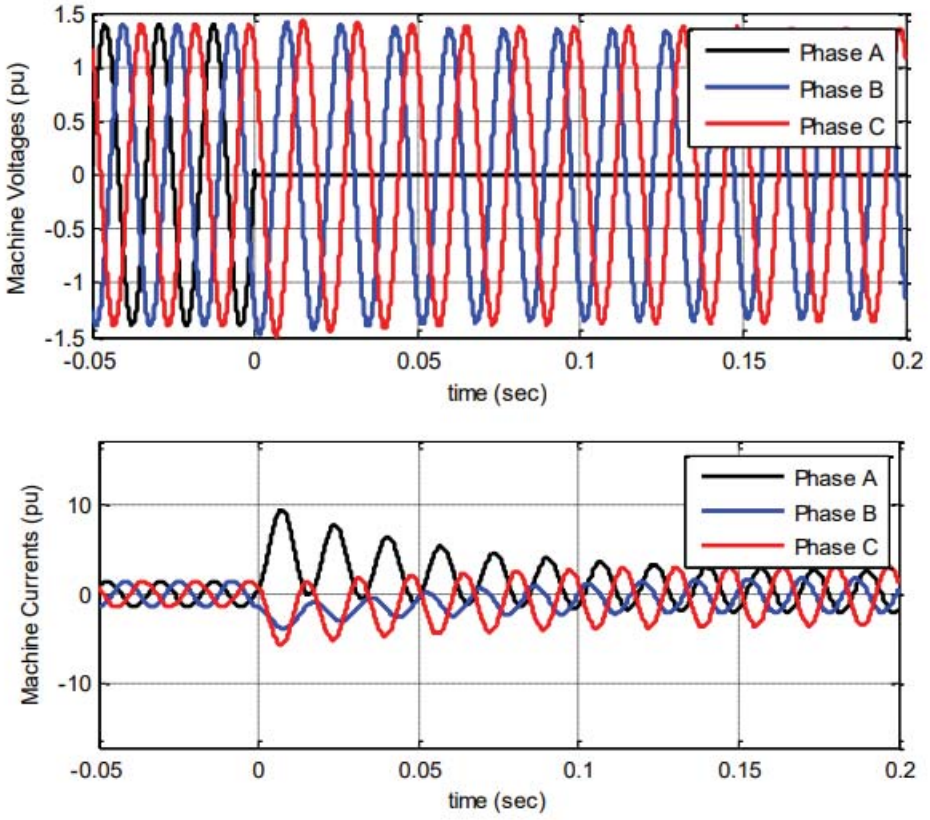

Figure 2.6 Type I WTG terminal bus voltage and current for single-phase-to-ground fault [18]

2.2.2 Type II WTG – Variable Slip Induction Generator

The Type II WTG, shown schematically in Figure 2.7, employs a wound rotor induction generator with a variable external rotor resistance. Unlike in Type I WTG, the three-phase rotor winding of the Type II induction generator is connected to a three-phase external resistance via a power electronic controller component. The torque-speed characteristics of the Type II WTG is well shaped through this fast electronic controller and hence the WTG has the ability to generate power over a wider range of wind speeds compared to the Type I WTG.

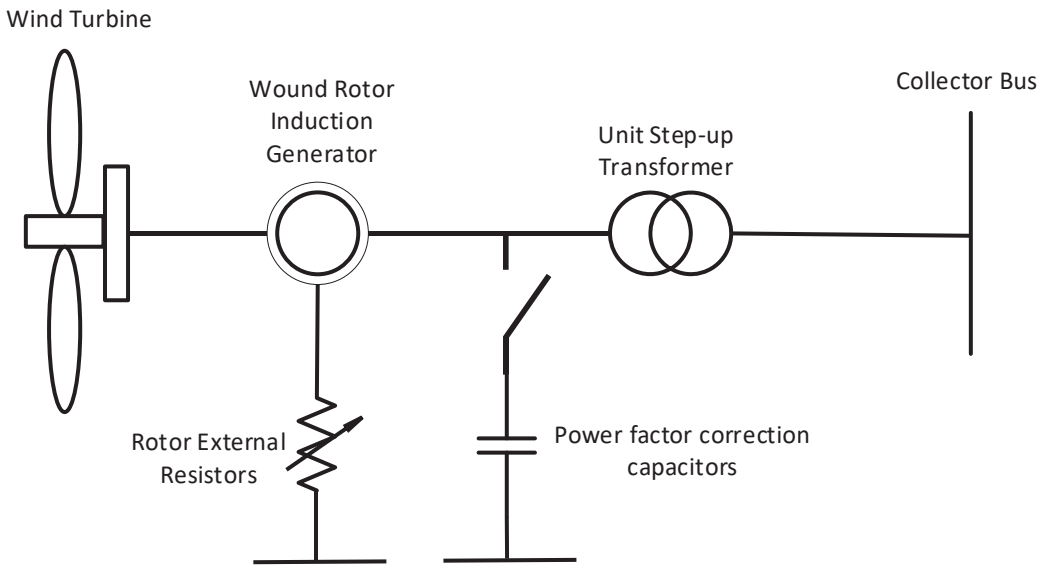

Figure 2.7 Basic structure of a Type II WTG

The maximum short circuit contribution of the Type II WTG occurs when the external resistance is shorted i.e., operating below its rated slip. This is also similar to the short circuit contribution from Type I WTG. The typical operating slip range of an induction generator is in between 0% and -1%. However, for a Type II WTG, the slip is allowed to vary no less than -10% [19]. With higher external rotor resistance values, the operating slip also becomes higher than the rated slip. The higher external rotor resistance results in the reduction of maximum initial fault current and an increase in damping of the fault current. The increased damping reduces the duration of the fault current.

Figure 2.8 shows the variation of the fault current contribution in Amperes for a three-phase to ground fault according to the various rotor resistance values and the blue colored line depicts the predicted fault current for zero rotor resistance.

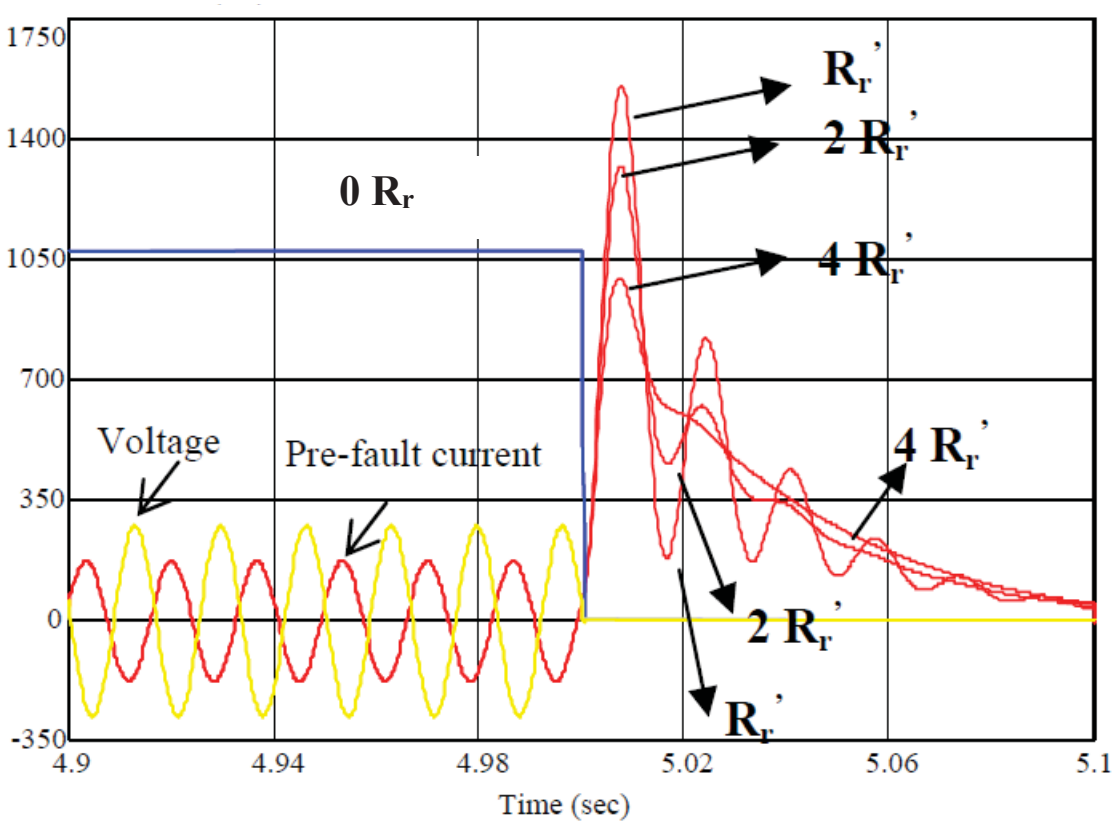

Figure 2.8 Type II WTG fault current contribution for three-phase-to-ground fault [20]

2.2.3 Type III WTG - DFIG

The schematic diagram of Type III WTG consisting of a DFIG which is a variable speed WTG is depicted in Figure 2.9. The stator winding of the Type III WTG is directly connected to the grid. However, the rotor is connected to the power grid through a back-to-back converter configuration allowing independent and instantaneous control of active and reactive power over a ±30% operating slip range.

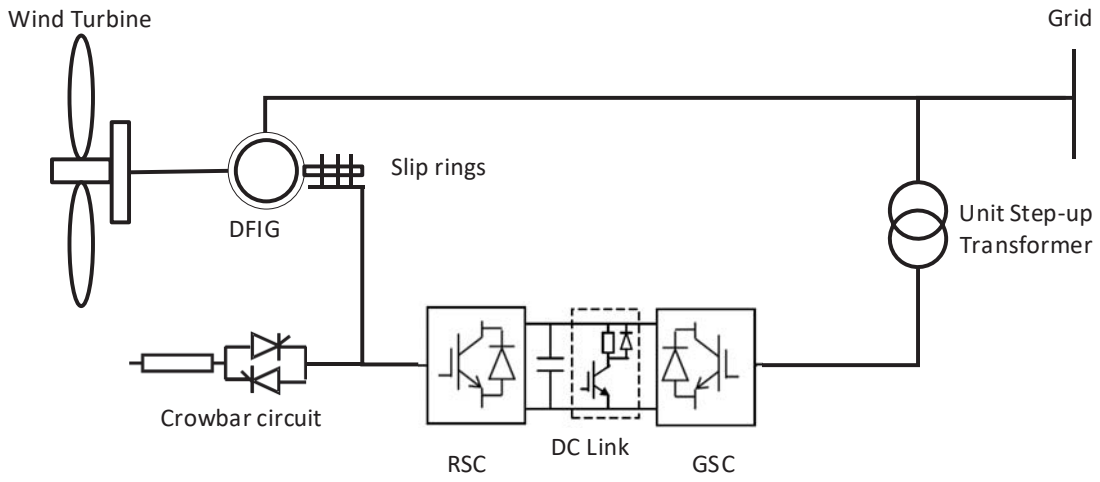

Figure 2.9 Basic structure of Type III WTG

A Type III WTG consists of a Grid Side Converter (GSC) and a Rotor Side Converter (RSC). The GSC of the DFIG is controlled to achieve a constant DC-link voltage across the DC-link capacitor. The GSC is thus responsible to keep a balanced power injection into the DC-link capacitor versus active power exchanged with the grid [21]. The RSC of the DFIG is connected to the GSC via a DC-link capacitor unit, and its role is to control decoupled active and reactive power injection into the grid through the stator.

In contrast to the characteristics of Type I and II WTG, the characteristics of the Type III WTG is preliminarily governed by the power electronic based control system. The power converter configuration of the Type III WTG allows the rotor to rotate at an alternative speed with respect to the synchronous speed. Therefore, the DFIG has the ability to protect against severe power system oscillations which may result in post transient conditions [22]. Besides, the Type III WTG has a special protection scheme called crowbar protection which provides overcurrent protection for RSC and overvoltage protection for DC capacitors. The crowbar circuit consists of a set of three-phase resistors which are controlled by a set of thyristor switches connected back-to-back. The crowbar is activated if the rotor current exceeds its limits beyond a certain threshold. By energizing the crowbar circuit, the RSC is disconnected from the rotor to prevent high rotor currents entering RSC and thus, the three-phase crowbar resistors are connected in series with the rotor winding. The resistors help to dissipate excess power generated in the rotor due to high rotor currents. Once the converters are isolated from the rotors, the WTG performs as a Type I or II

WTG. Modern Type III WTG designs provide intermittent activation of crowbar protection scheme resulting in effective control of fault current through the duration of the fault.

An example of a fault current contribution of a typical Type III WTG is illustrated in Figure 2.10 for a three-phase-to-ground fault. In this study, the crowbar was activated for the first two cycles and then the generator controls have removed the crowbar while the fault still exists. Due to the generator controls, the fault current has been limited to 1.2 pu of the rated value. The WTG provides reactive power support to the grid during three-phase-to-ground faults.

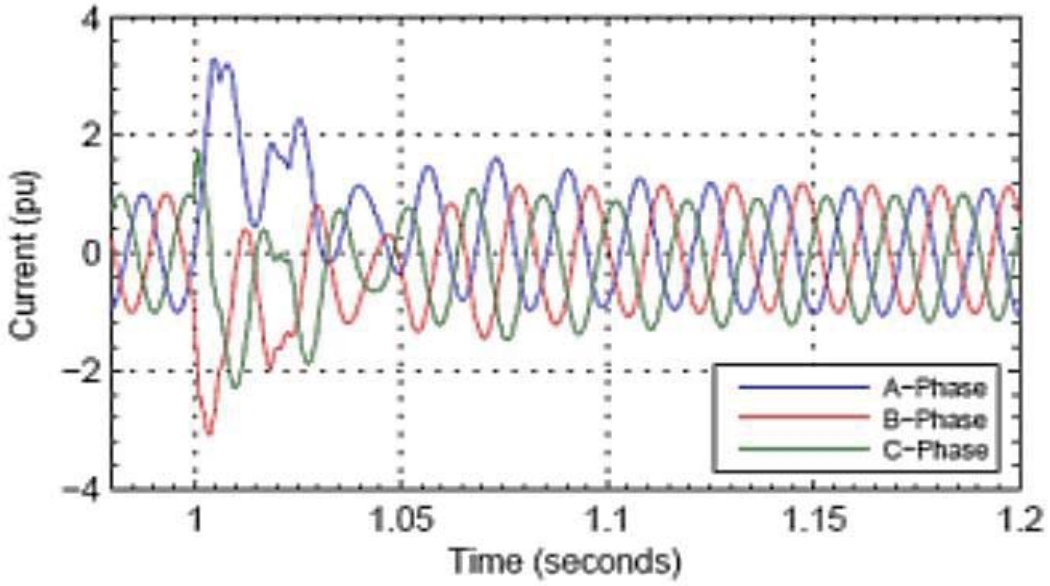

Figure 2.10 Type III WTG fault current contribution for a three-phase-to-ground fault [18]

2.2.4 Type IV WTG-Variable Speed Induction Generator

The Type IV WTG is a more recent development of variable speed WTG (i.e., induction machine or a Permanent Magnet Synchronous Generator (PMSG)) equipped with a full-scale back-to-back power electronic converter as represented in Figure 2.11. The recent technological advancements provide cost-effective provisions of power electronic converters with the same ratings as the turbines, and they adequately control active and reactive power independently and instantaneously within their designed limits. In contrast to the WTG technologies described in previous sections, the machine of the Type IV WTG is completely decoupled from the grid, and the fault response is

fundamentally determined by the characteristics and control strategy of the full-scale converter [23]. In addition, the complete decoupled design between the power grid and the WTG allows the machine to generate variable frequency currents based on the varying wind speed while the grid frequency remains at 60Hz [24]. Therefore, this design of Type IV WTG offers excellent grid integration, flexible operation characteristics including wide frequency and voltage range, and good power quality. The ability of handling a wide range of voltages and frequencies is especially beneficial for weak grid connections.

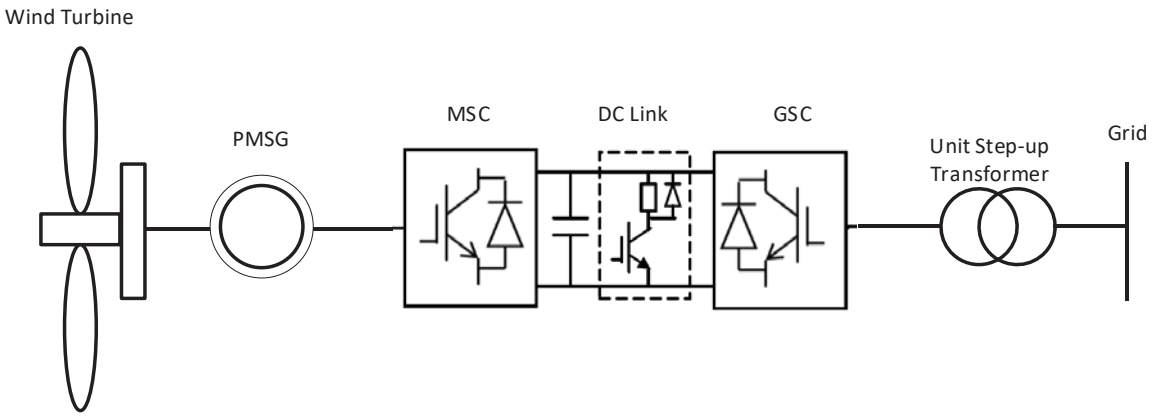

Figure 2.11 Basic structure of Type IV WTG

The full-scale power electronic converter adopted in Type IV WTG consists of GSC, Machine Side Converter and Controller (MSC), and a DC-link. A unit transformer is connected to the GSC terminal to step up the voltage typically from the range of 0.4 kV – 0.69 kV to the range of 33 kV – 34.5 kV [14], [18]. With the presence of the DC-link controller, the GSC is capable of delivering power to the collector system independent of the input power. The DC-link capacitor smooths the voltage whereas to keep it within the manufacturer's specified range. The output of the GSC is also controlled to synchronize with the grid frequency.

The fault response of the Type IV WTG equipped with a full-scale converter is dictated by the converter controls, and not the inherent functioning of the generator. In general, the Type IV WTGs are designed to inject symmetrical current under both balanced and unbalanced fault conditions. Therefore, negative and zero sequence current components are not present in the event of a fault. But recent grid codes impose the requirement for the injection of negative sequence currents from the WTGs and the technological solutions are proposed for Type IV WTGs to comply with the

demanding grid codes [14], [24]. Often, the WTG converters adopt current limiting functionality to protect GSC against overcurrent and are controlled to deliver constant power output. The current limiting functionality often set the output current magnitude close to the nominal current, i.e. 1.1 – 1.3 pu being typical and this is considered as the maximum current limit imposed on the output current magnitude [18].

2.2.4.1 Balanced Fault Characteristics

The Type IV WTG is capable of detecting a fault within a few milliseconds after the occurrence of the fault. During a fault, the output current of the WTG tends to increase in order to maintain a constant active and reactive power level at a lower than rated voltage. However, the maximum RMS line current depends on the converter current limit functionality and the value typically stays in between 1.1 pu – 1.5 pu of the rated value where the pre-fault injected current depends on several factors such as active and reactive current set points, wind condition and the residual voltage.

The Type IV WTG is often equipped with Fault Ride-Through (FRT) control. The FRT mode will be activated after a fault is detected by the WTG control system to adjust the current based on a pre-set value. As stated above, the current value is required to increase in response to the fault which results in under voltage conditions. However, the Type IV WTGs have to fulfill the requirements set by the grid codes of certain countries, and in absence of such grid code requirements, the manufacturer will specify the current injection behavior of the WTG. For instance, the German grid code has imposed requirement for reactive current injection from the WTGs proportional to the deviation of the positive sequence voltage [25].

An example waveform from an EMT simulation of a WPP is provided in Figure 2.12 representing a current response for a balanced three-phase fault on the collector system. The waveform clearly depicts an initial transient overcurrent condition followed by a steady current which has been settled around 1.1 pu close to the nominal current. The steady current represents the controlled current injection of the WTG converter topology. The initial transient period or the uncontrolled response occurs up to 0.5 – 1.5 cycles after the initiation of the fault. Figure 2.12 Fault current waveform from Type IV WTG.

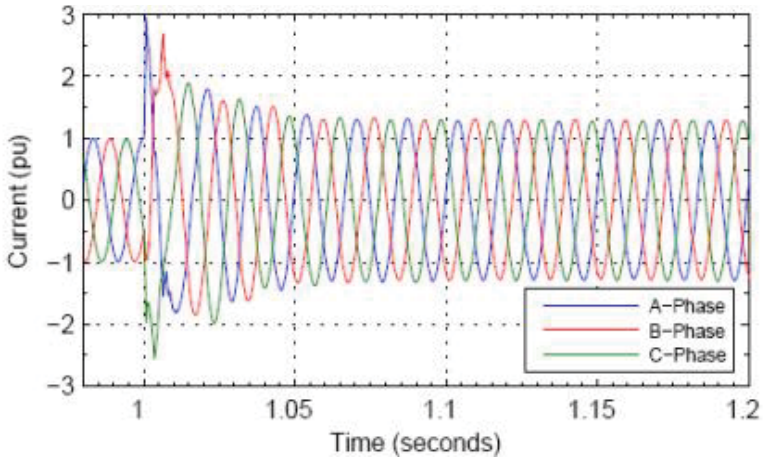

Figure 2.12 Fault current waveform from Type IV WTG [18]

2.2.4.2 Unbalanced Fault Characteristics

The Type IV WTG is usually represented as a controlled current source model for the short circuit studies due to the fact that the power electronic devices are intolerant of over currents. When the currents and voltages reach the thresholds, the control characteristics of the WTGs yield to discrete actions and hence it is difficult to characterize these machines by generic models.

The unbalanced behavior of the Type IV WTG deviates from the behaviors of typical induction and synchronous generators. In WTG, the zero-sequence current is usually neglected since the WTGs are typically ungrounded systems. During an unbalanced fault, both positive and negative currents are injected to the power network with a magnitude limited to the ratings of the power electronic converters. The negative sequence current suppression helps to mitigate power oscillations from the WTGs, and to reduce the negative sequence grid voltage to achieve a balanced grid voltage. However, the negative sequence current is expected to inject to the network if mandated by the grid codes.

An example waveform from an EMT simulation of a WPP is provided in Figure 2.13 representing a current response for a single-phase to ground fault at the WTG terminal.

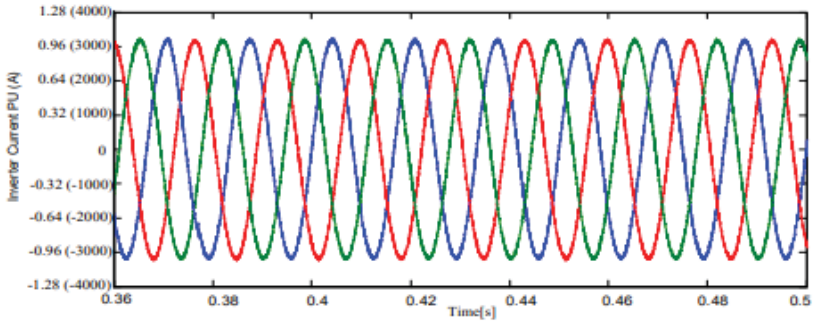

Figure 2.13 The Type IV WTG contribution to a single-phase to ground fault at the WTG terminal [26]

Another approach is described in [26], where the negative sequence contribution is suppressed during an unbalanced fault occurrence. Usually, unbalanced faults result in a large ripple in the DC bus. In order to accommodate this kind of ripple, a large capacitor would require. But the WTG manufacturers adopt control actions to output a balanced current at the WTG terminals rather than accommodating large capacitors. Therefore, although the grid voltage becomes unbalanced due to a fault, the line current can be balanced due to the power converter control. Figure 2.14 clearly depicts a fault current and voltage response to a single-phase to ground fault applied at a Type IV WTG terminal.

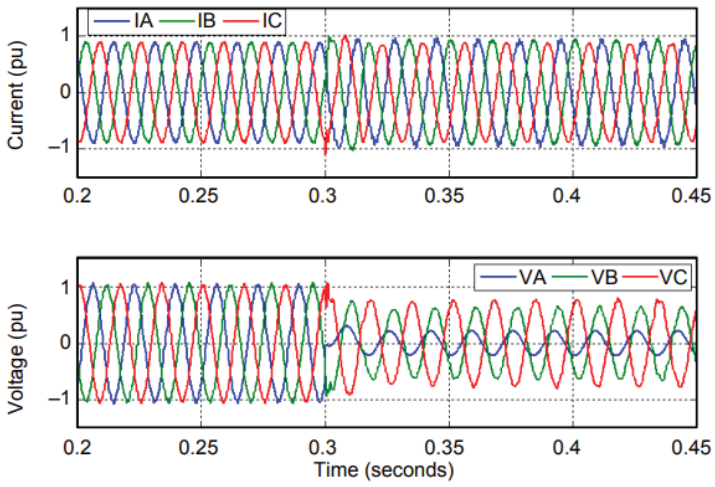

Figure 2.14 Current and voltage for a single-phase to-ground fault at Type IV WTG terminal bus [26]

2.3 Overview of IIR Network Equivalent Model

Electricity generation of a typical WPP is accomplished by utilizing a number of WTGs. These individual generators are connected to a medium voltage bus called a collector bus and the power produced by the WTGs is transmitted through the collector bus to the Point of Interconnection (PoI). A typical WPP substation is equipped with a central controller to control voltage, power factor, and reactive power injection at the PoI.

The short circuit modeling of WPPs favors the models which are capable of acquiring sufficiently accurate and faster responses. This is accomplished by aggregated WPP modeling and often used in EMT type software packages [27]. Thus, the WTGs along with the low voltage to medium voltage step-up transformers are represented with an aggregated model, and an equivalent collector grid model is also adopted to represent the grid integration.

In [13] and [14], a short circuit modeling approach for WTGs is discussed with a voltage controlled current source equivalent model as shown in Figure 2.15. *I_{f}_wtg,* the voltage controlled current source, represents the fault contribution from the WTG and *V_{f}_wtg* represents the voltage at the Point of Generator Connection (PGC). Due to the limiters and controls employed in WTG model, the current source becomes nonlinear. *WTG_filter* represents the Thévenin impedance of the low pass filter component connected to the GSC of the WTG.

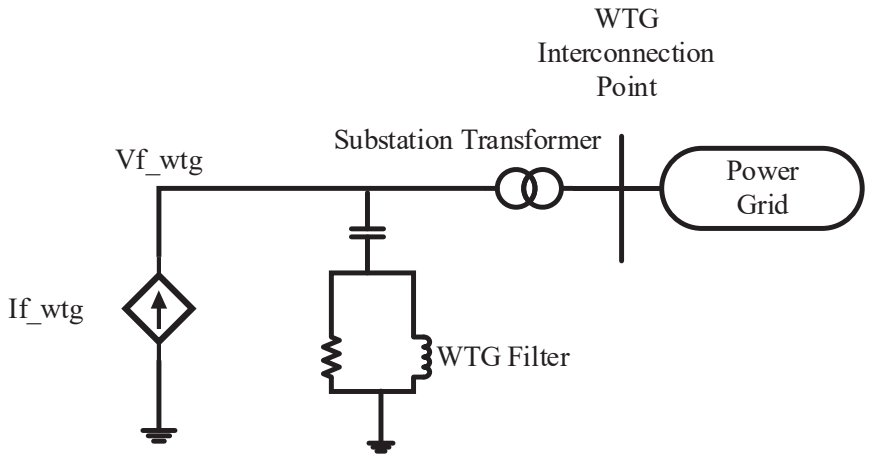

Figure 2.15. Voltage controlled current source model of Type IV WTG [14]

In addition, the impact of WTG mode of operation, inverter controls and the current constraints on the short circuit response are accounted through an iterative solution.

There are numerous research studies that discuss about the voltage controlled current source modeling approach. In [28], a phasor domain modeling approach for Type III WTG is discussed where the Type III WTG is represented by a controlled current source. An iterative solution approach is employed to account for the impact of the converter control actions. The model is limited to analyse three-phase balanced faults that occur in the power system.

The [13] presents a steady-state modeling approach for Type IV WTG which is represented as a controlled current source. The GSC control action is accounted through an iterative short circuit solution. The modeling approach presented in this study has the ability to represent a detailed EMT model in steady-state. In advance, the proposed model is able to account for different control schemes of Type IV WTG including FRT control function and decoupled sequence control action.

2.4 EPRI Model and Algorithm

Electric Power Research Institute (EPRI) is an independent research and development organization based in United States. It provides industry expertise for the electricity sector to identify critical issues in electricity industry and to address the challenges through innovative solutions. EPRI has developed steady-state phasor domain short circuit models and a solution algorithm for Type III and IV WTGs. The research project was carried out in collaboration with Polytechnique Montreal and in partnership with simulation software companies [29]. The developed model can simulate both balanced and unbalanced faults.

2.4.1 Iterative Solution Method

In contrast to the traditional short circuit analysis, the nonlinear behavior of the WTG requires an iterative solution to study the short circuit behavior of IIR. One of the main considerations of iterative short circuit analysis is the GSC control. The ac/dc grid-side voltage source converter (VSC) is used to connect the Type IV WTG with the ac grid and it regulates the DC bus voltage [30]. Figure 2.16 shows the schematic diagram of the GSC.

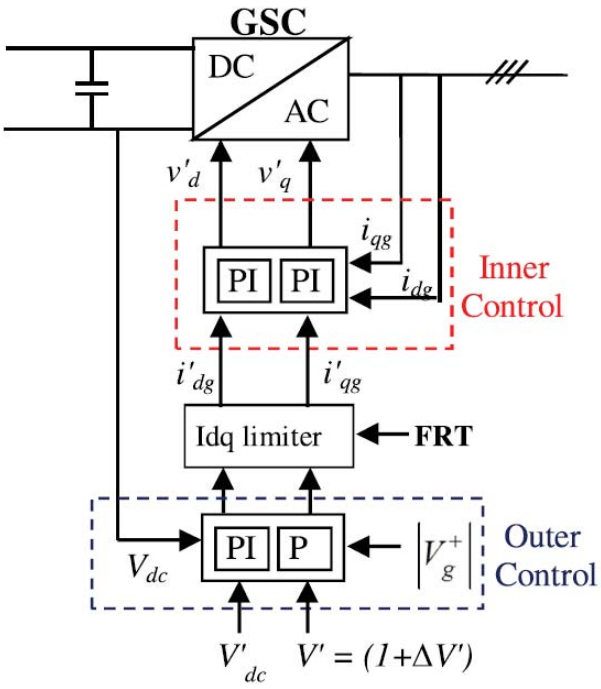

Figure 2.16 GSC coupled sequence control [13]

The GSC control consists of a two stage controller i.e. outer controller and inner controller with a current limiter block. The outer controller computes the reference dq-frame currents, and the inner controller derives the ac voltage reference of the converter. The d-axis current (i_{dg}) of the GSC controls dc bus voltage (V_{dc}) while q-axis current (i_{qg}) controls the terminal voltage magnitude of the GSC ($|V_g^+|$).

The output of GSC depends on the control mode of the converter. The following generic converter control modes are considered in the EPRI short circuit algorithm.

- Constant power factor control mode: Injects or absorbs reactive power based on a given power factor
- Constant reactive power mode: Injects or absorbs a constant amount of reactive power independent of active power.
- Voltage control mode: Controls voltage to the desired value
- Dynamic reactive current control based on the reference curve

2.4.2 Tabular Data Format for EPRI Algorithm

A tabular data format is proposed by the developers which does not require disclosing the manufacturer specific proprietary controls. The information that should be included in the tabular data format is provided in Table 2.1.

Table 2.1. EPRI tabular data format for iterative short circuit model

Time frame (cycles or seconds)					
Fault type					
Converter control mode					
WTG pre-fault active power generation					
Positive sequence			Negative sequence		
Voltage (pu)	Current (pu)	Current angle w.r.t. voltage (deg)	Voltage (pu)	Current (pu)	Current angle w.r.t. voltage (deg)
0.1			0.1		
. . .			. . .		
1.0			1.0		

Then the WTG current injection is computed iteratively until convergence with the use of voltage at the WTG interconnection point. The process continues until two consecutive WTG current injection values reach the required convergence criteria.

2.4.3 EPRI Iterative Short Circuit Algorithm

The EPRI iterative short circuit algorithm is depicted in Figure 2.17.

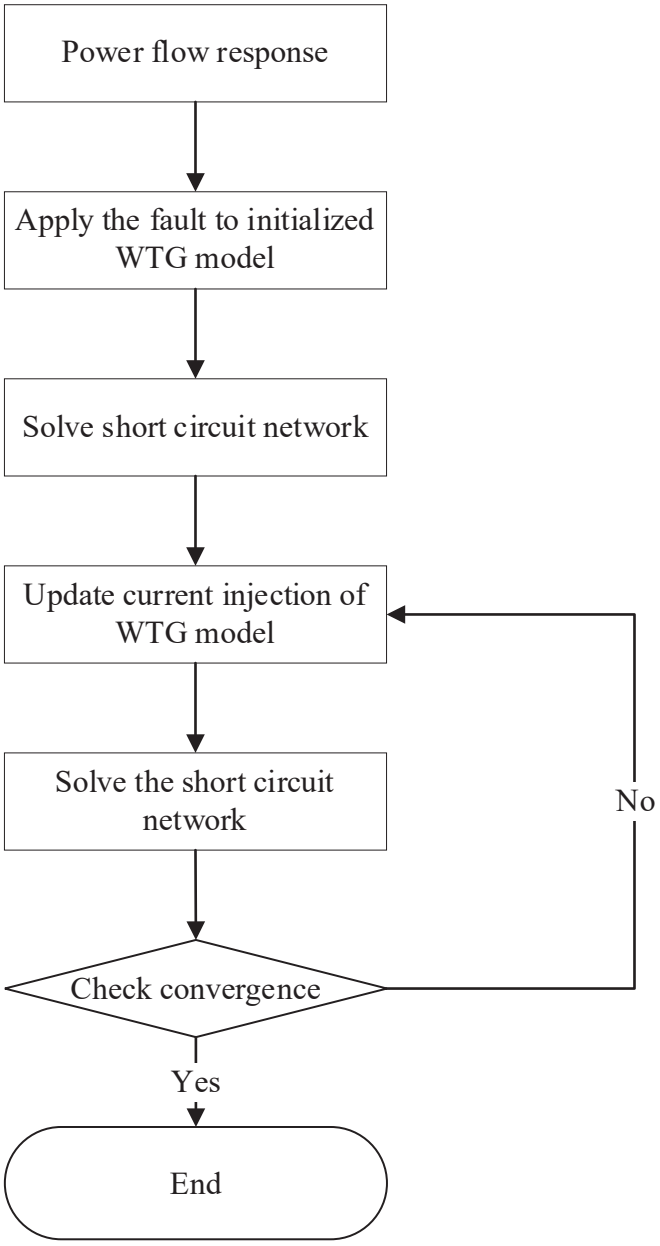

Figure 2.17. EPRI iterative short circuit algorithm

The EPRI iterative short circuit analysis is initialized with a power flow analysis of the complete power system network to linearize the network. The WTG short circuit model is represented as a voltage controlled current source and the model parameters are initialized using the power flow solution. Then a fault is applied on the power system and initiates the short circuit analysis.

Special consideration is given to "Update current injection of WTG model". The data for the model can be obtained from the manufacturers or the user can generate required data using EPRI generic WTG model.

2.5 CAPE Model and Algorithm

The PSS/E CAPE is a software tool specially designed for protection studies by SIEMENS. This section outlines the CAPE model implementation of Type IV WTG in short circuit analysis. CAPE also utilizes an aggregated WPP configuration to reduce the model complexity and computational burden. Similarly, the generic WTG control modes i.e. constant voltage, constant real power, constant power factor and dynamic reactive current injection modes are also considered in computation algorithms [14].

The aggregated model of a typical type IV WTG configuration is depicted in Figure 2.18. This means that all the wind generators, turbines, turbine transformers and shunt filters are aggregated together with the collector grid. Note that PGC is the connection downstream of the filter and is in the low voltage side of the turbine transformer. The turbine transformer connects PGC to the medium voltage collector grid whereas the substation transformer connects the MV (Medium Voltage) collector grid to the high voltage transmission grid. The PoI is the HV side of the substation transformer.

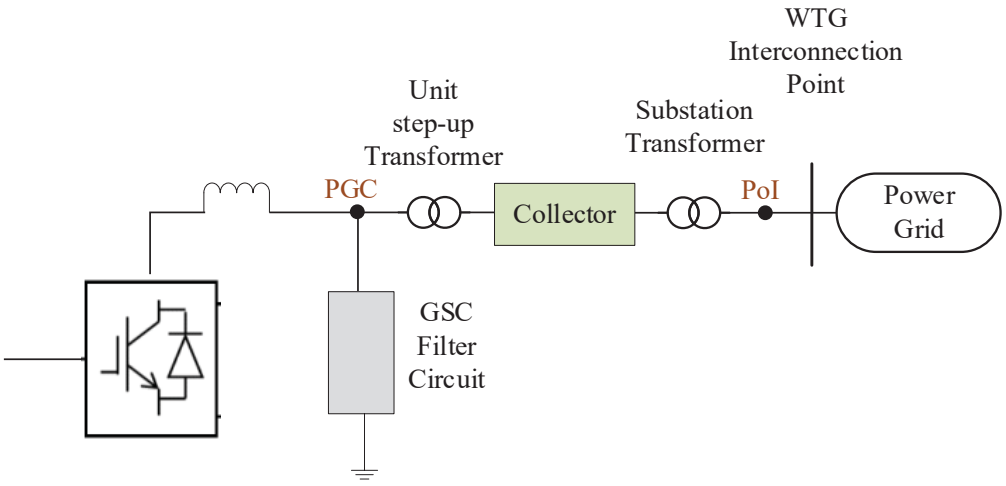

Figure 2.18 Schematic diagram of a Type IV WTG

The aggregated WTG configuration is separated into two sections where the connection downstream of the MV bus is analysed in CAPE model and the collector grid and substation transformer are analysed in network database. In this analysis, the electronically coupled WTG is replaced with a voltage controlled current source of which a positive sequence current is injected to the MV bus. The CAPE model also utilizes the tabular data format discussed in Section 2.4.2 to determine the current injection and power factor angle at the MV bus according to the generator voltage at the MV bus. Due to the nonlinear behavior of the inverter controls of the WTG, an iterative short circuit solution method needs to be hosted. The data required for the CAPE model implementation is given in [14].

Figure 2.19 illustrates with a flow diagram the different steps of the CAPE iterative short circuit algorithm. The solution algorithm starts with a power flow analysis to determine the pre-fault bus voltage profile of the network. Alternatively, a flat voltage profile at 1.0 pu can be utilized. Then the d-axis and q-axis pre-fault current values are determined with the specified pre-fault reference power values, P and Q, of the WTG equivalent model. Afterward, the network is subjected to a fault and solved for the fault current injected by the aggregated WTG model at the MV bus. The current is injected into the network to obtain the bus voltage profile where the modified fault voltage accounts for the summation of pre-fault voltage and the incremental voltage due to the injected current during the fault. During the process, if there are any isolated WPPs, the breakers will remove them from the network.

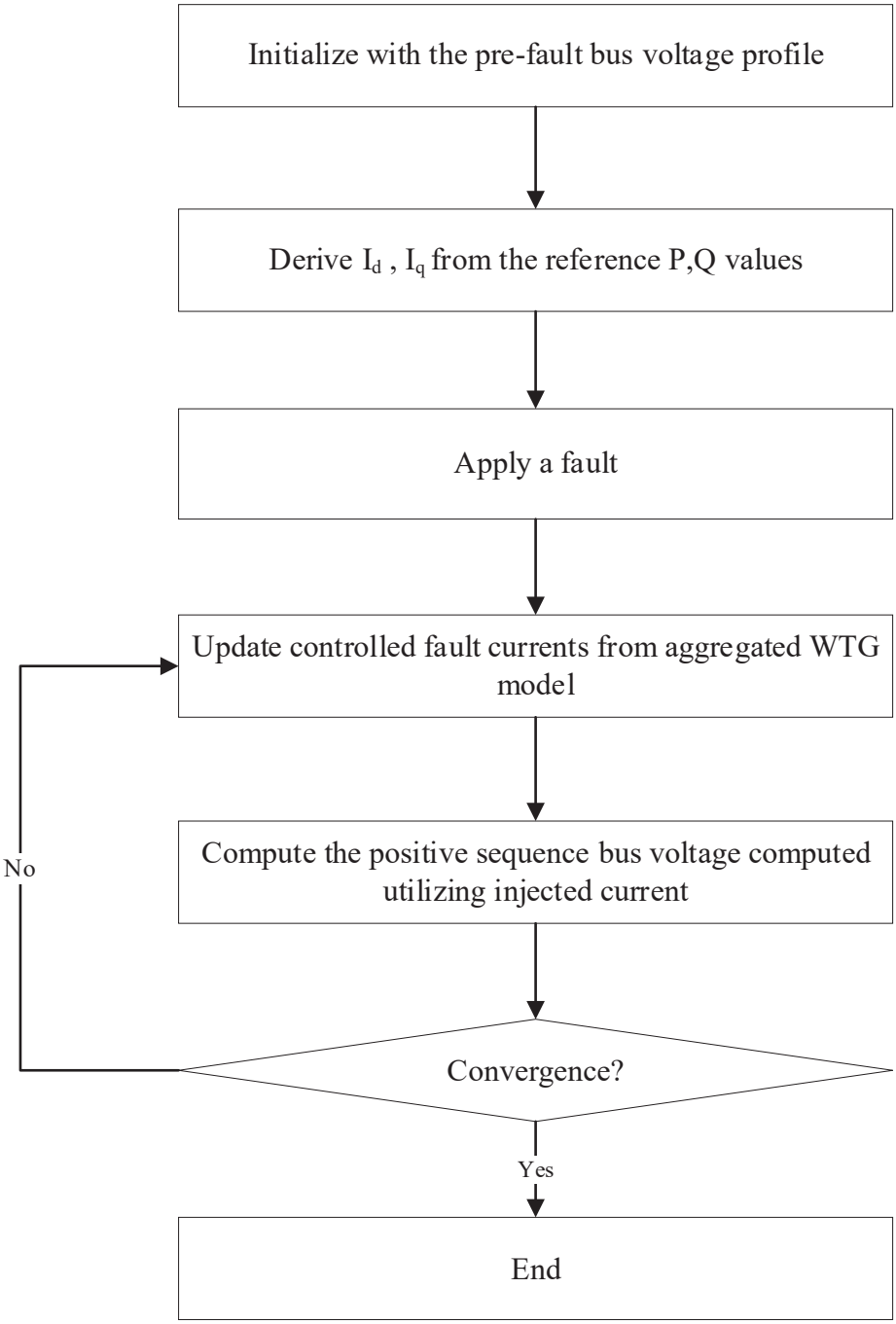

Figure 2.19 CAPE iterative short circuit algorithm

The new network voltages are used to update the current injection of the aggregated WTG model. At this step, the respective current injection is determined according to the calculated voltage using the tabular data format described in Section 2.4.2. Then the network is resolved for the voltages using the updated injected currents. At this step, the positive sequence voltage magnitude at the

MV bus is compared with the previous iteration. The iterative procedure is repeated until convergence. The default CAPE tolerance is 0.01 pu on the system base MVA.

The CAPE short circuit model described in this section does not consider negative sequence current injection. However, in [31] it is mentioned that the negative sequence controls will be implemented in the next versions of CAPE models.

2.6 ASPEN OneLiner Model and Algorithm

This section details the ASPEN OneLiner commercial short circuit algorithm for Type IV WTG. Aspen OneLiner is a software program for short circuit studies and relay coordination. In 2016, ASPEN developed a model for VSC in OneLiner short circuit program in collaboration with ABB which is a prominent converter manufacturer. As per the guidance of ABB, the VSC was modeled as an ideal current source. For this work, ABB provided tabulated current magnitudes and power factor angles at different terminal voltages which yield the converter output. The OneLiner model for Type IV WTG short circuit analysis is later developed as an extension to the ASPEN voltage controlled current source model [32]-[33].

Modern Type IV WPP and solar plants are well equipped with a VSC interface that synthesizes the ac current output using pulse width modulation. One major consideration is the converter current response under a fault condition. The converter fault current response is followed by an initial transient during the first half cycle after the onset of the fault. In [34], the short circuit current response of a Type IV WTG is illustrated with a momentary peak which is 2.4 times the pre-fault current in the first half cycle. Then the converter current output settles into a sinusoidal waveform with a magnitude slightly above the pre-fault level. Although this indicates that short circuit programs are unsuitable for simulating the initial transient response, they provide greater accuracy in simulating the controlled response followed by the transient condition. Similarly, ASPEN OneLiner model is capable to simulate the converter model after the first half cycle of the fault inception.

The WTG phasor models are developed considering the various converter controller behaviors and the controller strategies. Three control configurations act under normal operation on specific electrical parameters namely voltage, reactive power, and power factor and use positive sequence

voltages and currents to determine the control actions. Another control mode, FRT control, is activated following a disturbance to facilitate voltage support. All these control modes are represented in phasor domain equations prior to being used in the WTG model [29]. Similarly, ASPEN Type IV WTG model is developed considering these control strategies and the assumptions listed below:

- Under normal operating conditions, the WTG operates in voltage regulation mode where the terminal voltage is within 0.9 pu – 1.1 pu. In this region, maintaining a constant real power supply is given priority.
- Under abnormal conditions (terminal voltage less than 0.9 pu or greater than 1.1 pu) the FRT strategy will be used.

2.6.1 Fault Ride-Through (FRT) Mode

Modern large-scale WTGs, which provide a large amount of active power to the HV transmission system, are required to remain connected to the grid during faults and provide voltage support to fulfill the grid code requirements. As a result, the FRT function is implemented and activated in the event of a short circuit. The FRT mode is turned on once the positive sequence terminal voltage is outside the deadband. This section briefly explains the FRT control mode present in ASPEN short circuit model. Figure 2.20 illustrates the typical relationship between the q-axis current and the positive sequence terminal voltage magnitude during FRT controls.

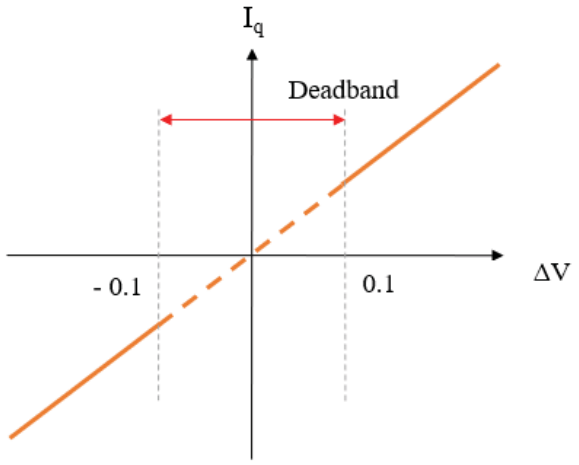

Figure 2.20 An example FRT control curve [29]

The FRT function is activated when the terminal voltage deviates at least 0.1 pu. Equation (2.14) describes the d-axis and q-axis current injections by the converter controls:

$$I_q = -2(1 - V_d) \tag{2.14}$$

where I_q is the q-axis current injection into the network and V_d is the d-axis positive sequence voltage at the converter terminal.

In (2.14), I_q is limited to reactive current limit (1.1 pu) and ASPEN short circuit model requires this as a user input. However, during low voltage conditions, this equation outputs negative I_q meaning a negative reactive current injection to the power network. This response is similar to that of the synchronous generators where a lagging power factor is appeared in the event of a fault. Equation (*2.15*) is used in order to maintain a constant active power output:

$$I_d = \frac{I_{dpre}}{\left(\frac{V_d}{V_{dpre}}\right)} \tag{2.15}$$

where I_d is the d-axis current injection into the network, I_{dpre} is the d-axis pre-fault current injected into the network, and V_{dpre} is the d-axis positive sequence voltage at the converter terminal. All these quantities are given in per unit. Finally, I_d is evaluated to ensure $I_d + I_q$ does not exceed the defined maximum current limit as:

$$I_d \leq \sqrt{I_{max}^2 - I_q^2} \tag{2.16}$$

If the I_d exceeds the limit, then it is held to the I_{max} limit.

Note that the above process has to be iterative since the terminal voltage is subjected to change due to the change in the current injection. The ASPEN OneLiner short circuit program performs this iterative process before and after the fault.

2.6.2 ASPEN OneLiner Iterative Algorithm

The ASPEN OneLiner model also requires a set of data similar to the EPRI model and the data structure can be found in Table 2.1. An aggregated WPP model is used in the computational process to represent all generating units. The model lumps all the generating units into a voltage

controlled current source [32]. The pre-fault conditions of the network for the OneLiner algorithm can be either determined by a power flow analysis or simply by the flat-start option. ASPEN OneLiner utilizes the following algorithm to compute the steady-state short circuit current from the WPP network:

1. Compute pre-fault voltages for all the terminal buses in the WPP network using power flow analysis or assume a flat voltage profile.
2. Compute the nodal impedance matrix for positive, negative, and zero sequences and reduce the network to a minimum size set only containing faulted buses and buses connected to nonlinear devices i.e., WTGs.
3. Transform reduced sequence matrices to phasor domain matrices and invert the matrices to obtain admittance matrices.
4. Apply a fault in the network and modify the phase admittance matrices according to the applied fault.
5. Solve the nodal equations to obtain the post fault voltages in the reduced network. With the presence of nonlinear elements i.e., voltage controlled current source model which represents the WTG units, an iterative network solution is proposed. In this method, the voltage response of the terminal buses which connect to these nonlinear elements is compared to the previous iteration. If the solution is above a specified threshold, the phasor domain nodal equations are modified to replicate the voltage or current variation. This procedure is repeated until the voltage magnitudes converge.
6. Finally, the network compensation theorem is incorporated in the complete network solution. The changes in the reduced network are reflected in the corresponding full sequence networks with the aid of compensating sequence currents.

The ASPEN OneLiner iterative short circuit solution algorithm is developed based on the method described in [35] where sparse vector techniques are used to produce efficient solutions.

As discussed in this section, the ASPEN OneLiner program for Type IV WTG short circuit analysis is based only on the injection of positive sequence currents, not considering negative sequence current injection from WTs. However, modern converter-based WTs inject both positive and negative sequence currents during unbalanced faults. In advance, German and Spanish grid codes address the impact of negative sequence current injection of IIRs as well [36].

2.7 Concluding Remarks

This chapter described general short circuit current calculation methodology, the behavior of induction generators and IIRs during faults, and the approaches used for incorporating IIRs in a few commercially available short circuit calculation programs.

Chapter 3

Automated Calculation of Busbar Fault Currents in PSCAD/EMTDC Environment

As power systems evolve to include high penetration of IIR, some electric power utilities have started to develop system models in EMT simulation programs such as PSCAD/EMTDC. Although EMT models can be used for calculating network quantities during steady-state and faults accurately, it is time consuming. The ability to perform basic phasor domain studies such as power flow and short circuit analysis to obtain approximate results on the same modeling platform is useful if not essential. This chapter develops an efficient method for busbar short circuit analysis in PSCAD/EMTDC environment with a custom Python script and presents a case study carried out for IEEE 14 bus test system.

3.1 Background

Modern power systems are inherently complex due to the number of equipment interact together to maintain adequate system performance. Therefore, it emerges the necessity for faster and more accurate computer-based analysis tools to model and simulate power systems to perform system studies.

Among them, most widely used are the phasor-based analysis and simulation tools. For example, Power System Simulation for Engineering (PSS/E) [37] is one of the widely used software tools established for steady-state analysis and dynamic simulations. PSS/E is a phasor-based power system solver including a comprehensive set of analysis tools such as power flow analysis, optimal power flow, short circuit analysis, and stability analysis. In order to perform such analyses, the

power system topology, generator, transformer, transmission line sequence impedance data, load active and reactive power data, and dynamic data such as various time constants of equipment and controllers are provided. The presence of sound data in PSS/E enables seamless switching between various analysis tools by adhering to the specified standards. For example, PSS/E possesses essentially required features for standard short circuit calculation including power flow analysis methodology and sequence impedance data of the system equipment. The analysis of the short circuit module is performed in compliance with ANSI C37.5-1979 and IEC 60909-2001 [38]. There are several other similar software suits such as DAS Tools [39], PSLF [40], etc. but they do not have the ability to perform EMT simulations.

There are also software programs specialized for short circuit analysis and protection relay coordination. Examples are ASPEN OneLiner, PSS/E CAPE, ETAP, etc. which use phasor domain techniques and symmetrical components for dealing with unbalanced conditions. These programs come with various additional tools helpful for protection relay setting and coordination. However, they have limitations in modeling power electronics and do not have the ability to perform EMT simulations.

Alternatively, there are software tools specialized for EMT simulations such as PSCAD/EMTDC [41] , EMTP-RV [42], ATP-Draw [43], EMTP, etc. These programs enable multi-phase modeling and analysing power systems using EMT simulations, usually in a graphical environment. PSCAD/EMTDC is one of the most widely used EMT programs and capable of performing time-domain simulations of power systems with embedded power electronics to capture a wide range of transient and dynamic behaviors. Thus, EMT simulation programs such as PSCAD/EMTDC can be used to compute short circuit currents very accurately, provided that the system is modeled properly. This type of short circuit analysis, for example in PSCAD/EMTDC, requires users to model and test their simulation under different scenarios to establish proper pre-fault steady-state conditions, apply faults, and process the time-domain waveforms to obtain phasor values. Therefore, it requires extensive human interaction and consumes a substantial amount of time and engineering effort. But for certain types of studies, short circuit analysis need not to be very accurate, but obtaining adequately accurate solutions under a variety of conditions with less effort and time is more important. For the users who intend to maintain the system models in EMT format, it is inconvenient to transfer the system models to a phasor domain analysis program to

perform such studies. According to Manitoba Hydro International (MHI) which develops PSCAD/EMTDC software, such a simple short circuit analysis feature in PSCAD/EMTDC environment has been requested by the existing PSCAD/EMTDC users.

Recognizing this gap, the automated busbar fault current calculation method is developed in PSCAD/EMTDC environment to obtain fast short circuit solutions on a given power system and estimate fault current contributions and voltage profile of the faulted power system. The development of the Automation Library feature (AL) in Python which is compatible with PSCAD/EMTDC 4.6.1 and the latest versions, allows automating PSCAD/EMTDC with custom scripts and hence reduces human interaction and time consumption as well. The PSCAD Initializer software is also utilized to obtain a proper power flow solution prior to the fault event.

3.2 Proposed Short Circuit Analysis Technique

The automated busbar short circuit procedure is developed in PSCAD/EMTDC V4.6 environment employing PSCAD Initializer software and Python programming language. The PSCAD Initializer is used to set up the power flow conditions and obtain the pre-fault bus voltages prior to applying and analysing PSCAD/EMTDC system for bus bar short circuit conditions.

3.2.1 The Python GUI for Providing Study Parameters

The proposed short circuit analysis process requires a range of data including faulted bus/s, fault type, power flow data, system base MVA, system frequency and fault impedance. In order to obtain the specified user inputs, a Python GUI is developed as illustrated in Figure 3.1.

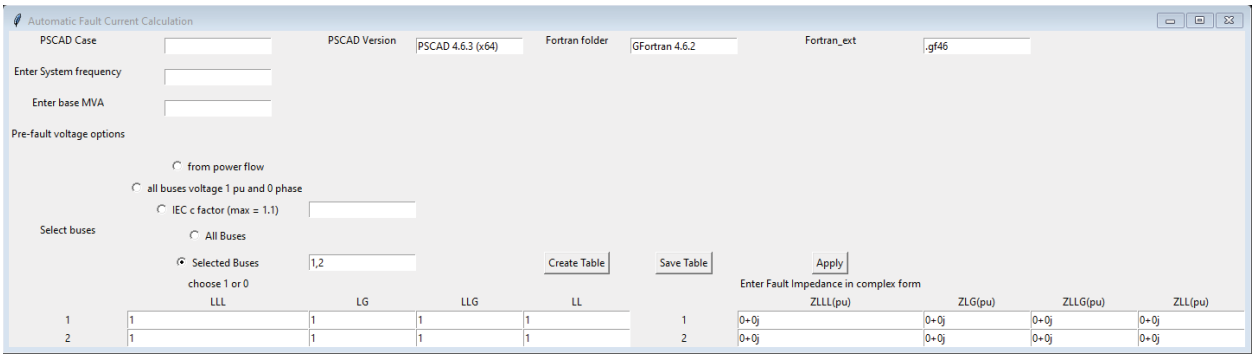

Figure 3.1. Python GUI for automated bus bar short circuit analysis

Through the GUI, the user can specify the pre-fault condition to be adopted; based on the inputs, the procedure is either directed to perform power flow analysis or use a flat voltage profile or IEC recommended user defined factor to create the voltage profile. The sequence impedance data required for the short circuit analysis is extracted from the PSCAD/EMTDC simulation case.

3.2.2 Power Flow Data

Having accurate power flow data such as voltage and phase angles at bus bar terminals, active and reactive power flow through transmission lines etc. are essential prior to simulating a disturbance in a power system. The default power flow engine, the Power Flow Light solver of the PSCAD Initializer software is called through the Python script to solve the power flow for the network according to the power flow equations described in section 2.1. PSS/E software is also available as an alternative solver in the PSCAD Initializer to obtain the power flow response of a given power system. The power flow data generation process is described in Figure 3.2.

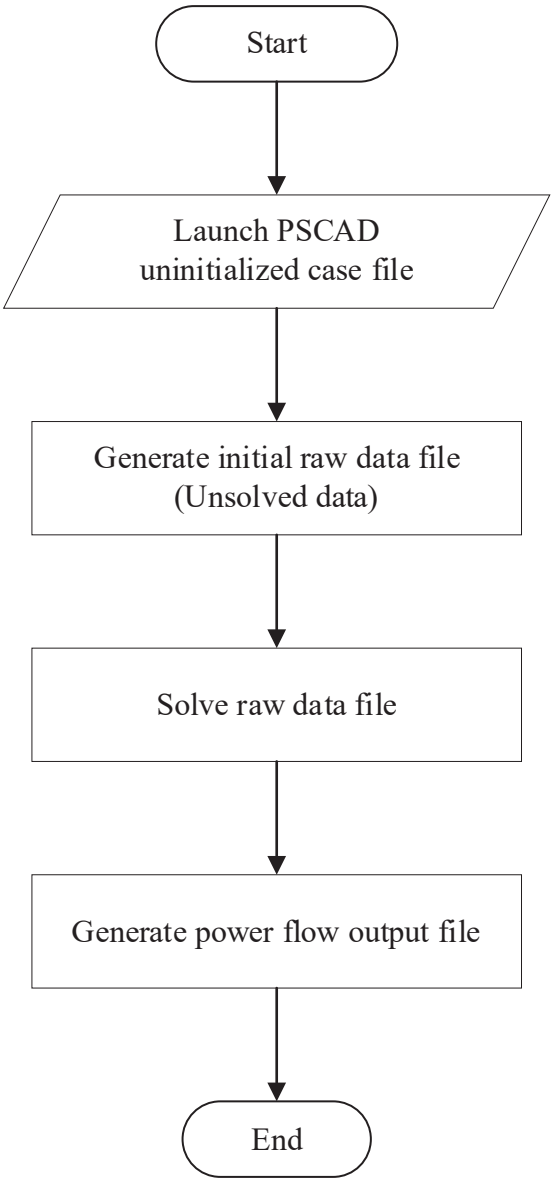

Figure 3.2. PSCAD Initializer power flow data generation

In addition to the above power flow calculation method, the algorithm provides another two alternative options based on ANSI and IEC calculation methods [11]. Both ANSI and IEC methods recommend applying a flat voltage profile (1 pu and 0 degree) or applying a user definable voltage factor known as *c* factor. The range of the *c* factor was defined for different voltage levels, and 1.1 is the maximum value of c factor for all the voltage levels [12].

3.2.3 Thévenin Impedances of Sequence Networks

Accurate modeling of the system equipment is one of the most important parts of the short circuit analysis. While performing balanced and unbalanced short circuit analysis, consideration must be given to the sequence impedance diagram and the specified connection types for each type of fault. For the bus bar short circuit calculation, Thévenin equivalent impedances of sequence networks at the faulted bus are required as discussed in Section 2.1. In phasor-based power system analysis programs and short circuit programs, these are obtained through the bus impedance matrix. However, in EMT programs such as PSCAD/EMTDC, the data is not available in a form that can be directly used to construct the conventional bus impedance matrix.

However, a model called "Interface to harmonic impedance solution (Frequency scanner)" is available in PSCAD/EMTDC master library. This frequency scanner component provides multi-port impedance of a given electrical network over a range of frequencies. This existing component can be used to obtain the Thévenin equivalent impedances of sequence networks at the faulted bus, at the required system frequency, 50 Hz or 60 Hz. There are several different purposes to carry out short circuit studies. One purpose is protective device duty calculation. In general, first cycle currents, 1.5 - 4 cycle currents, and 30 cycle currents are considered for duty calculation. Depending on the type of protective device duty, sub-transient, transient, or steady-state impedance values should be applied to the equipment models. Therefore, the test system should be modeled with appropriate impedance data in PSCAD/EMTDC to obtain the correct Thévenin impedances via the Frequency scanner.

The knowledge of harmonic impedance is an important parameter for harmonic suppression, accurately represent power system frequency response and harmonic impedance-based stability criteria. The harmonic impedance of a system characterizes the impedance of a specific port in a power system at different frequencies. The Thévenin equivalent circuit for measurement of harmonic impedance is depicted in Figure 3.3. For the harmonic impedance calculation, the frequency scanner injects a synthesized wide band current signal to the point of interest and the voltage and current waveforms are extracted from the point of measurement. Then, the Fast Fourier Transform (FFT) technique is employed to calculate the fundamental and harmonic magnitudes

along with phase angles of each signal [44]. With the output of the FFT, harmonic voltage *(Uh(jω)*, harmonic current *(Ih(jω))* and the harmonic impedance *Zh(jω)* can be calculated as:

$$Zh(j\omega) = \frac{Uh(j\omega)}{Ih(j\omega)} \tag{3.1}$$

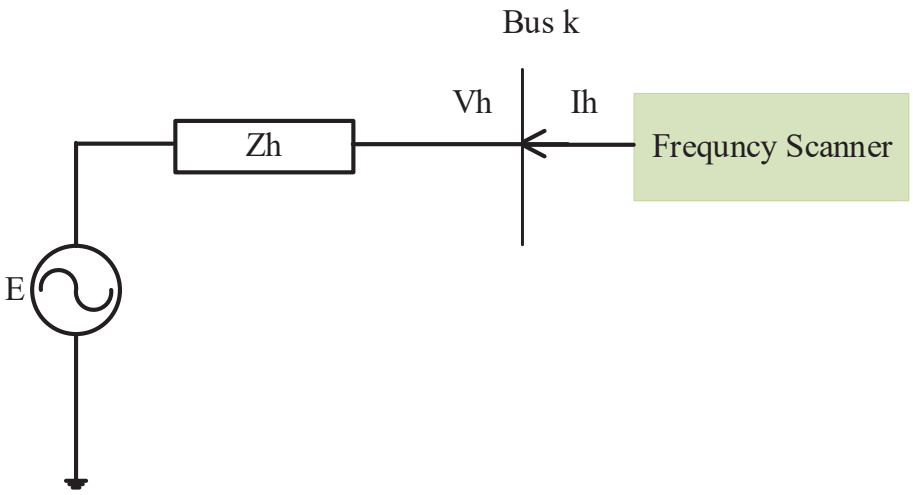

Figure 3.3 Measurement of harmonic impedance

However, defining a range of frequency is unnecessary for the short circuit study and hence the system frequency, 50 Hz, or 60 Hz, is used for the calculation procedure in busbar automated short circuit analysis.

A frequency scanning method adopted by the Frequency Scanner component is as follows. The basic principle is to inject a small harmonic current I_h at the point where the harmonic impedance Z_h is to be measured. The current is injected while the system is in steady-state. Then the harmonic voltage at the specified bus, $U_{h\_60Hz,}$ will be measured in response to the $I_{h\_60\,Hz}$ [45]. The Thévenin impedance Z_h will be calculated by the Ohm's Law by,

$$Z_h = \frac{U_{h\ 60\ Hz}}{I_{h\ 60\ Hz}} \tag{3.2}$$

The algorithm used here does not actually perform a complete time-domain simulation to calculate the harmonic impedances but uses network data in PSCAD/EMTDC model to extract the

information. This component extracts the status of breakers/faults and variable resistance, inductance, and capacitance values in the first time-step and the solution is found in the second time-step. Therefore, the user needs to run the simulation only for 2 time-steps. Thus, it is a quick procedure and provides results as a matrix in the sequence domain or in phasor domain including mutual impedances. More complete details of the algorithm used in the PSCAD/EMTDC frequency scanner component can be found in [45]. The following assumptions are made in the frequency scanner [46]:

- Transformer saturation and arresters are assumed to be in their unsaturated region.
- All the power electronic devices are assumed to be in their OFF state.
- Synchronous and induction machines are represented as grounded inductors.
- The zero-sequence impedance of an SVC is represented as the primary-delta leakage reactance of the transformer, and the positive and negative sequence impedances are represented by the defined shunt loss conductance.
- The minimum frequency to calculate system impedance is 1 mHz. Therefore, DC resistance is not computed.

3.3 Automation of Short Circuit Analysis Procedure

The short circuit calculation for a power system network was performed in compliance with the IEEE Std 3002.3-2008 [11]. The steps involved in the calculation are described below.

1. Determine pre-fault voltage profile of the power system network based on a valid power flow calculation method or assume base voltage of the buses where initial power flow calculation is not made.
2. Obtain the Thévenin impedance of the sequence impedance networks of the system components (i.e., generators, motors, transformers, loads and power transmission equipment etc.) as seen from the faulted bus.
3. Construct the sequence networks according to the type of fault applied.
4. Calculate sequence currents and fault currents.

The steps involved in automated busbar short circuit simulation are illustrated in Figure 3.4.

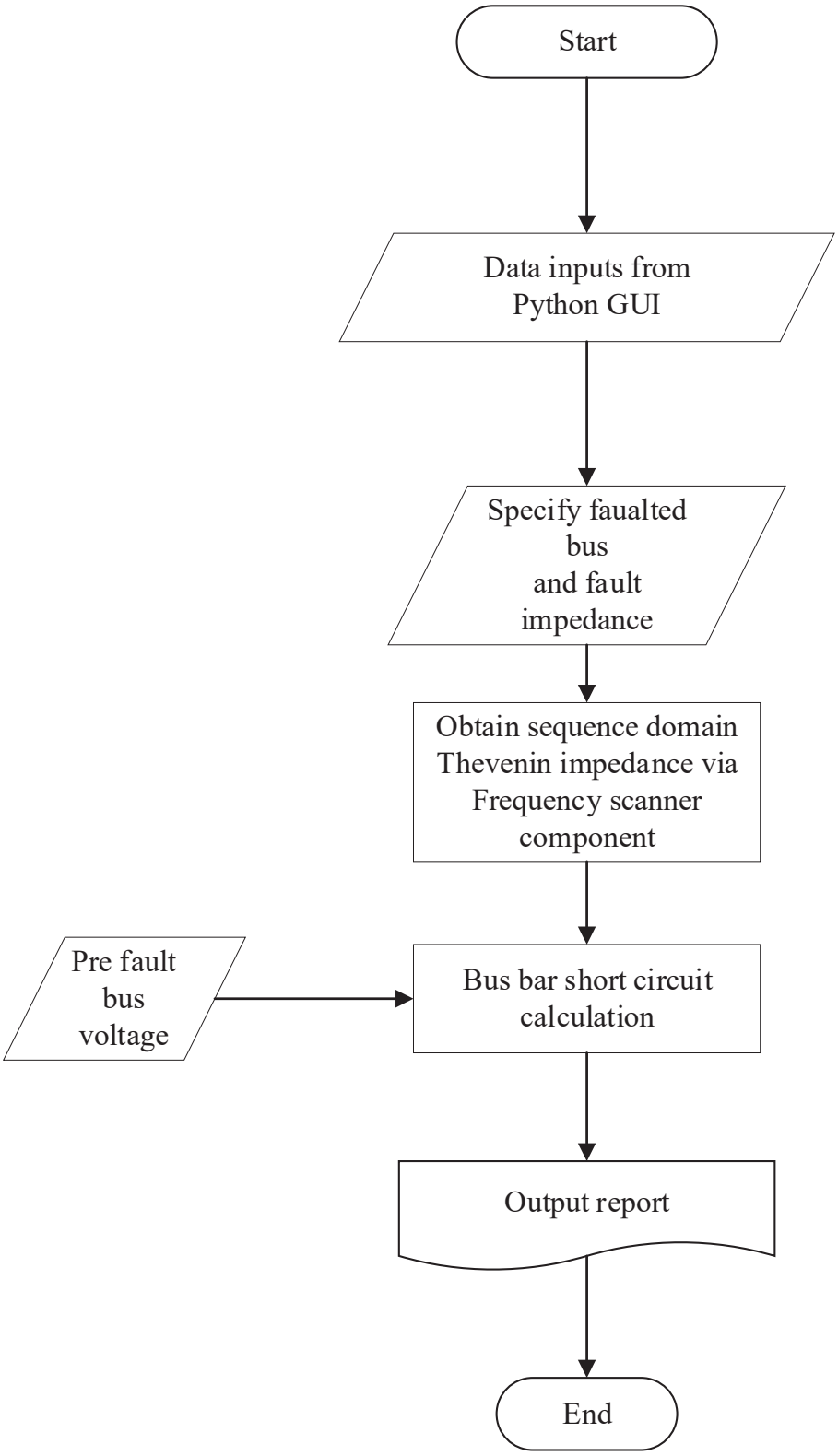

Figure 3.4. Short circuit calculation procedure

3.4 Case Study: IEEE 14 Bus Test System

A complete time-domain simulation for symmetrical and asymmetrical faults is performed on IEEE 14 bus system as illustrated in Figure 3.5 and the system data is given in Appendix B. It consists of 5 generator buses and 7 load buses. The system is implemented in PSCAD/EMTDC, and balanced and unbalanced faults are applied separately at each bus to measure the fault currents. The fault duration is 0.5s.

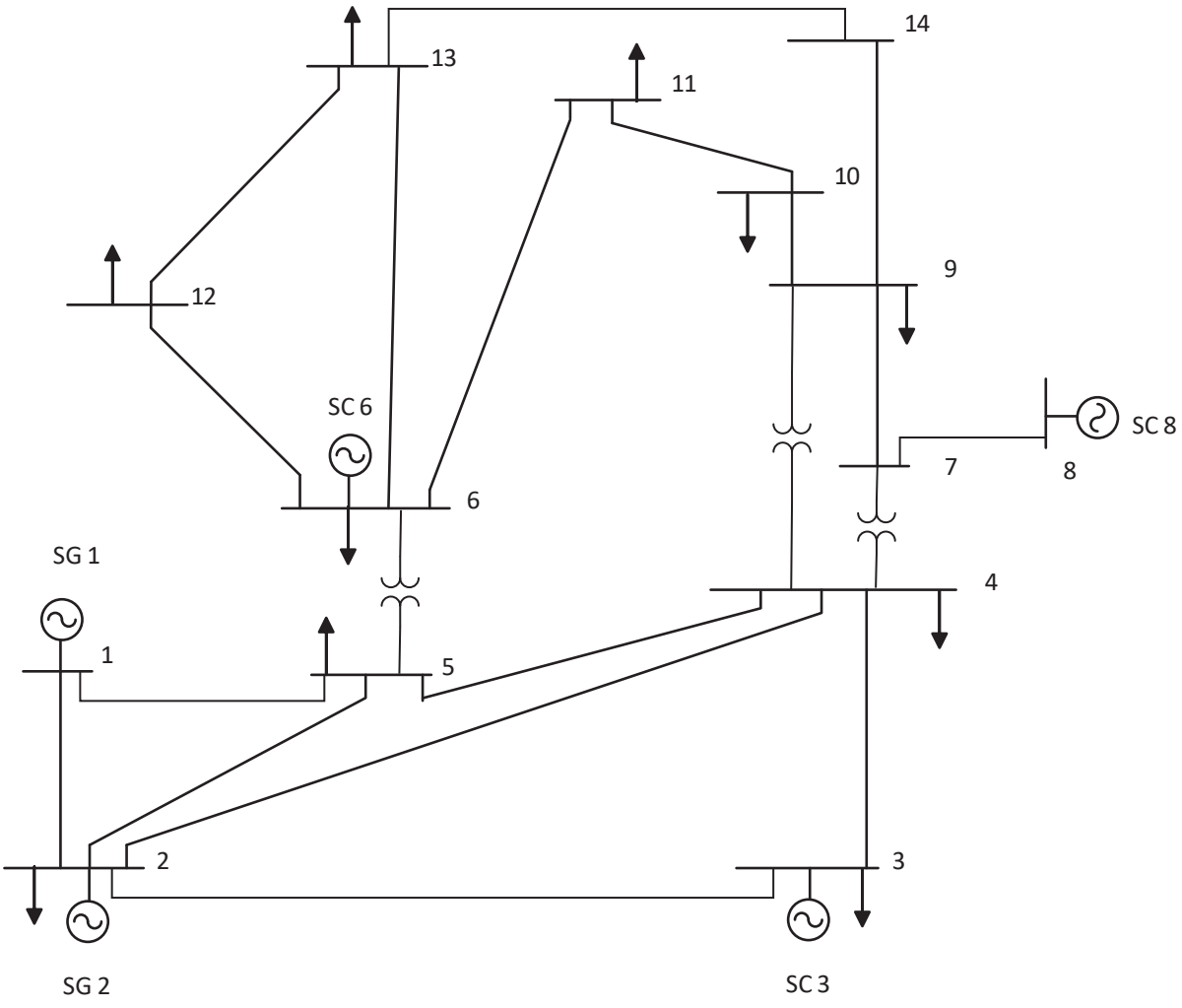

Figure 3.5 IEEE 14 bus test system

The comparison of busbar fault current response from the automated script is compared with the TD simulation performed in PSCAD/EMTDC. The results are presented in the form of magnitudes in pu and angles in degree. Table 3.1 presents a comparison of pre-fault voltage magnitudes and angles obtained from PSCAD initializer and PSCAD/EMTDC TD simulation. The highest magnitude difference is 0.02 pu, and the highest phase angle difference is 0.64°. The values are acceptable to perform protection studies. Table 3.2 Sequence Thévenin impedances of the IEEE 14 bus test systemTable 3.2 presents the sequence Thévenin impedances of the IEEE 14 bus network. Table 3.3 to Table 3.6 illustrate a comparison between TD analysis and automated busbar fault analysis solutions for balanced and unbalanced faults.

Table 3.1 Pre-fault bus voltage magnitudes and phase angles

Bus no.	Bus voltage magnitude (pu)		Bus voltage phase angle (degrees)	
	PSCAD Initializer	PSCAD/EMTDC TD simulation	PSCAD Initializer	PSCAD/EMTDC TD simulation
1	1.0600	1.0597	0.00	-0.00
2	1.0450	1.0437	-4.96	-4.98
3	1.0100	1.0085	-12.63	-12.74
4	1.0271	1.0153	-10.38	-10.30
5	1.03348	1.0166	-8.96	-8.75
6	1.0700	1.0644	-14.89	-14.25
7	1.0453	1.0558	-13.46	-13.37
8	1.0900	1.0851	-13.46	-13.37
9	1.02801	1.0496	-15.08	-14.96
10	1.0279	1.0448	-15.33	-15.12
11	1.0451	1.0510	-15.22	-14.82
12	1.0531	1.0505	-15.72	-15.11
13	1.0463	1.0446	-15.74	-15.19
14	1.0177	1.0294	-16.40	-16.07

Table 3.2 Sequence Thévenin impedances of the IEEE 14 bus test system

Bus no.	Z+ (pu)	Z- (pu)	Z0 (pu)
1	0.0012+0.0281i	0.0012+0.0281i	0.0004+0.0214i
2	0.0113+0.0538i	0.0113+0.0538i	0.0111+0.07i
3	0.029+0.1013i	0.029+0.1013i	0.0272+0.1254i
4	0.0248+0.081i	0.0248+0.081i	0.0339+0.1214i
5	0.0218+0.0795i	0.0218+0.0795i	0.0276+0.1204i
6	0.0383+0.1808i	0.0383+0.1808i	0.0358+0.2024i
7	0.0304+0.1701i	0.0304+0.1701i	0.0352+0.2132i
8	0.0207+0.2596i	0.0207+0.2596i	0.0126+0.3107i
9	0.0459+0.1844i	0.0459+0.1844i	0.0655+0.2567i
10	0.0671+0.2248i	0.0671+0.2248i	0.1005+0.3539i
11	0.0826+0.253i	0.0826+0.253i	0.1191+0.4108i
12	0.1321+0.305i	0.1321+0.305i	0.1889+0.4864i
13	0.0841+0.2395i	0.0841+0.2395i	0.1185+0.3526i
14	0.1207+0.2974i	0.1207+0.2974i	0.1938+0.5105i

Table 3.3 LLLG fault current magnitude and phase angle comparison

Bus no.	Fault current magnitude (kA)		Phase angle (deg)	
	TD Analysis	Automated Busbar Fault Analysis	TD Analysis	Automated Busbar Fault Analysis
1	13.855	13.908	-78.28	-78.13
2	15.920	15.997	-82.95	-82.71
3	11.393	11.407	-89.44	-89.23
4	7.869	7.955	-85.73	-85.11
5	7.734	7.802	-86.22	-85.53
6	10.649	10.691	-93.74	-93.39
7	4.613	4.652	-97.17	-96.22
8	9.991	10.018	-94.17	-94.01
9	3.564	3.599	-93.38	-92.47
10	2.663	2.703	-88.49	-87.83
11	2.568	2.607	-84.43	-83.46
12	2.135	2.159	-76.62	-75.94
13	3.251	3.291	-81.32	-80.54
14	1.752	1.786	-83.23	-81.98

Table 3.4 LG fault current magnitude and phase angle comparison

Bus no.	Fault current magnitude (kA)		Phase angle (deg)	
	TD Analysis	Automated Busbar Fault Analysis	TD Analysis	Automated Busbar Fault Analysis
1	12.984	13.009	-78.71	-78.70
2	14.755	14.787	-83.34	-83.26
3	10.825	10.824	-89.60	-89.60
4	6.441	6.460	-86.01	-86.10
5	6.510	6.524	-87.39	-87.15
6	10.442	10.467	-93.68	-93.47
7	3.851	3.863	-96.94	-96.48
8	9.793	9.801	-93.98	-93.96
9	2.916	2.914	-92.85	-92.68
10	2.085	2.094	-89.35	-89.00
11	1.979	1.987	-85.95	-85.67
12	1.673	1.677	-78.68	-78.59
13	2.582	2.587	-82.50	-82.38
14	1.355	1.356	-83.77	-83.77

Table 3.5 LLG fault current magnitude and phase angle comparison

Bus no.	Fault current magnitude (kA)		Phase angle (deg)	
	TD Analysis	Automated Busbar Fault Analysis	TD Analysis	Automated Busbar Fault Analysis
1	13.352	13.404	164.64	164.76
2	15.289	15.355	160.49	160.70
3	11.083	11.084	152.92	153.09
4	7.297	7.333	162.62	163.13
5	7.145	7.188	161.02	161.56
6	10.532	10.571	147.27	147.60
7	4.319	4.343	150.56	152.43
8	9.897	9.921	146.97	147.08
9	3.332	3.341	155.18	156.04
10	2.441	2.465	160.83	161.90
11	2.321	2.348	165.75	166.62
12	1.929	1.942	172.91	173.47
13	2.971	2.990	167.97	168.62
14	1.598	1.615	167.16	168.27

Table 3.6 LL fault current magnitude and phase angle comparison

	Fault current magnitude (kA)		Phase angle (deg)	
	TD Analysis	Automated Busbar Fault Analysis	TD Analysis	Automated Busbar Fault Analysis
1	12.014	12.045	-168.23	-168.13
2	13.810	13.854	-172.91	-172.71
3	9.874	9.879	-179.38	-179.23
4	6.837	6.889	-175.54	-175.11
5	6.719	6.757	-175.99	-175.53
6	9.228	9.259	176.31	176.61
7	4.000	4.029	173.04	173.78
8	8.665	8.676	175.90	175.99
9	3.096	3.116	176.89	177.53
10	2.310	2.341	178.73	-177.83
11	2.234	2.258	-174.11	-173.46
12	1.857	1.870	-166.37	-165.94
13	2.828	2.850	-171.06	-170.54
14	1.528	1.547	-172.75	-171.98

Table 3.3 to illustrates the accuracy of the proposed automated short circuit model for balanced and unbalanced fault conditions. The highest magnitude error between TD analysis and automated busbar fault analysis is less than 1.5%, and the highest phase angle difference is less than 1.2%. This accuracy is acceptable for fault analysis.

3.5 Concluding Remarks

The chapter proposed an automated calculation methodology for busbar fault currents in PSCAD/EMTDC environment. PSCAD/EMTDC software is extensively used for power system studies, and it is capable of producing accurate results for short circuit studies. The objective of this study was to obtain a fast and adequately accurate short circuit response on a given power system which is modeled in an EMT environment. The chapter illustrates the accuracy of the methodology by comparing the results with PSCAD/EMTDC TD analysis for different types of faults applied on different locations. The proposed method provides accurate results and for the

considered case study, the fault current magnitude difference was less than 0.5% and the phase angle difference was less than 0.3% in most cases. However, user written components interfaced to EMT may not be considered in the frequency scanner component and will result in an inaccurate busbar Thévenin impedance solution.

Chapter 4

Iterative Short Circuit Analysis of Power Systems with Type IV Wind Generators

This Chapter presents a phasor domain iterative short circuit analysis methodology for power systems with Type IV WTGs.

The first section of this chapter describes the Type IV WTG model utilized in this study. The Section 4.4 and 4.5 describe the VDNE framework and data generation process and proposed iterative short circuit analysis methodology for IIRs. Finally, this chapter analyses the proposed methodology on two test cases: 7-bus radial test system and IEEE 39-bus system.

4.1 Introduction

Modern power systems utilities employ various EMT simulation software such as PSCAD/EMTDC and, EMTP-RV to model and simulate the networks with IIRs for control and protection studies. In general, manufacturers provide EMT models of IIR to the power system utilities as black boxed models. This approach allows manufacturers to realistically model their control architecture but maintain them as confidential details. These models generate input and output relations utilizing the nondisclosed controls. Although EMT software platforms are widely employed for modeling and simulation of short circuit responses of individual plants, it is cumbersome to completely model a large power system with IIR in EMT programs and perform short circuit studies. As a solution, phasor domain iterative short circuit analysis techniques have been proposed. This chapter develops and implements an iterative short circuit analysis technique similar to the approach proposed by EPRI [14], which was discussed in Chapter 2, for a Type IV

WTG. The scope of the analysis is limited to balanced three-phase faults. In addition, an automated process to obtain the data required for voltage depended network equivalent of the inverter-interfaced power plant using PSCAD/EMTDC simulations is developed. Python programming language is used for short circuit calculation and PSCAD/EMTDC automation process.

4.2 Proposed Approach for Iterative Short Circuit Analysis

As the case of power flow calculation procedure, the short circuit analysis of the network containing WTGs is also accomplished through an iterative approach. In iterative short circuit analysis, the complete system is divided into two segments; the external system i.e. large transmission network which is represented as a linear phasor-domain model and the subsystem with IIR, i.e. small part of the system consisting of the WTG model represented as a nonlinear model referred to as voltage dependent network equivalent (VDNE). This small part of the network is developed as an EMT model in PSCAD/EMTDC to obtain the parameters of the VDNE through TD simulations.

This concept is shown in Figure 4.1 which illustrates a power system with a wind farm represented using an aggregated WTG model. The subsystem with IIR will be modeled in detail in an EMT simulation for TD simulations. For the TD simulations, the external system is represented as a Thévenin equivalent model.

The proposed iterative short circuit analysis utilizes conventional short circuit calculation, where it runs many times as iterations to obtain the accurate voltage and current phasor solutions of the concerned network. In order to perform short circuit calculation, the subsystem with IIRs is represented as a combination of a linear voltage source behind an impedance and a voltage controlled current source.This modeling approach is called voltage dependent network equivalent. A detailed description of the formation of the VDNE will be given in Section 4.4.

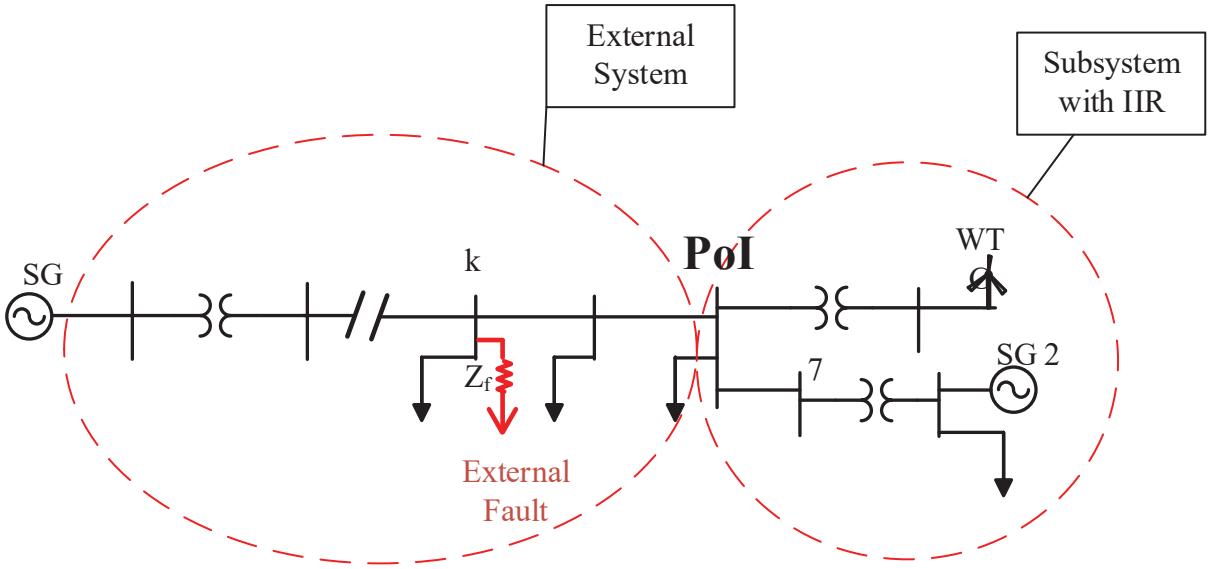

Figure 4.1 Division of a power system with IIR into external system and subsystem with IIR for iterative fault analysis

The challenge is to account for the nonlinear behavior of the IIR and hence to compute the injected current and the voltage at the PoI. As described in Section 2.2, IIRs inject controlled currents limited to the converter current limits. Therefore, the detailed PSCAD/EMTDC simulation model of the small part of the system is utilized to generate voltage and current injections at the PoI which will then be used for the iterative calculation procedure.

The iterative short circuit analysis starts either with a power flow analysis to determine the pre-fault bus voltages of the concerned power system or assuming pre-fault bus voltages as 1 pu with zero phase angles. In these pre-fault conditions, loads are modeled as constant impedances. Also, the sub-transient impedance of the SGs is considered in the computation. In each iteration, the classical short circuit calculation is executed considering the fault type and fault impedance applied to the external system. It determines bus voltages and fault currents flowing in the branches with the aid of Thévenin and superposition methods.

In the first iteration, the pre-fault current injected by the subsystem with IIRs and the initial fault voltage at the PoI are calculated with the aid of the network modeled in sequence domain. However, the current injected by the subsystem with IIRs is expected to have a nonlinear behavior. So, an iterative approach is necessary to obtain an accurate solution. Based on the voltage references generated at the PoI, the fault current injection from the subsystem with IIRs is

determined. Then the faulted bus voltage is recalculated using the difference caused by the fault current injection. Each time, faulted bus voltages at the buses including PoI are updated. With the new PoI voltage, the fault current injection from the subsyetm with IIRs is updated and the process is repeated. At each iteration, the voltage at the PoI is compared with the previous iteration, and iterations are continued until it meets the convergence criteria.

4.3 Type IV WTG Generator Model in PSCAD/EMTDC

According to the classification of WECC and IEC, a WTG interfaced through a full-scale power converter is referred to as a Type IV WTG. Due to the advanced control flexibility, Type IV WTGs are widely used in modern wind farms, despite the need for more expensive full-scale power converters. The Type IV WTG considered in this work consists of a PMSG and is connected to the grid through a back-to-back converter connected through a dc link.

The TD model of the Type IV WTG used in this study is based on the detailed model presented in [41] and [47]. This section presents the structure and essential electrical elements of the EMT model for Type IV WTG. The model consists of two sections: mechanical system and electrical system. The mechanical system and the electrical system are interfaced through a PMSG which converts mechanical energy produced by the WT to electrical energy. The mechanical system is out of the scope of the thesis and only the features of the electrical system are described. The main components of the electrical system model are as follows:

- Grid side converter
- Machine side converter (MSC)
- DC link capacitor
- Converter shunt filters
- Unit transformer
- Scaling unit

The AC-DC-AC converter configuration of the Type IV WPP model is shown in Figure 4.2.

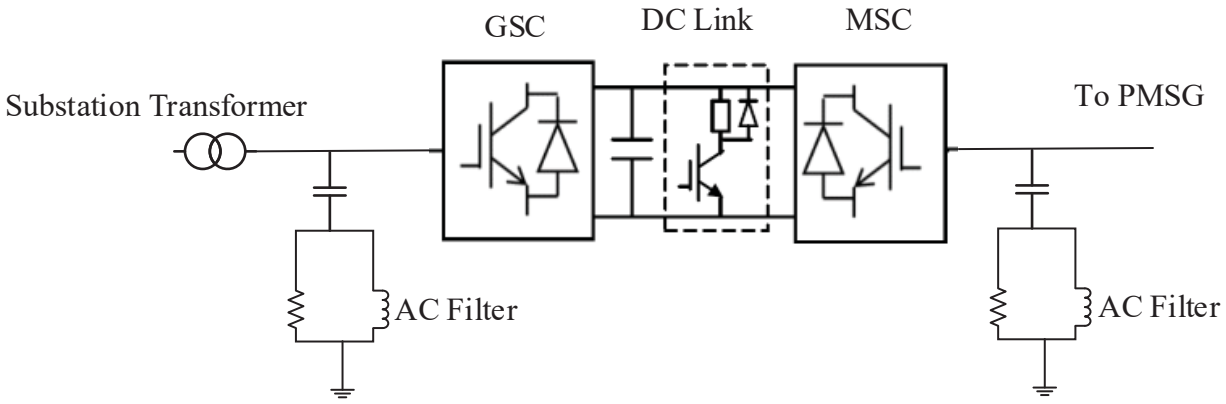

Figure 4.2 AC-DC-AC converter configuration of Type 4 WTG model

The converter model consists of GSC and MSC, a DC link capacitor and the converter shunt filters/low pass filter (LPF).

In this study, both the MSC and GSC are VSCs. But, MSC can be designed as a VSC or a diode rectifier depending on the WTG rating [30]. The role of the MSC is to control the active power injection and AC voltage at the PMSG terminal and hence to maintain specified ratings at the generator terminals. The role of the GSC is to regulate DC bus voltage and AC voltage on grid side.

In addition, a DC link capacitor circuit is included in the model to protect the DC bus from the undesired overvoltage conditions. The low pass filters are connected on the AC side of the GSC and MSC to reduce the voltage harmonic distortion.

The remaining scaling unit represents an aggregated WPP which is having a number of individual WTG units. The scaling unit multiplies the output current of the WTG model by the number of WTG units and the resultant current is injected to the power network.

4.4 Voltage Dependent Network Equivalent (VDNE)

The subsystem consisting of the WTG model is represented using a voltage dependent network equivalent in the phasor domain iterative short circuit analysis. In this study, Type IV WTG consisting of full-scale converters is considered. Figure 4.1 illustrates the external system and the subsystem with IIR. This subsystem with IIR needs to be represented in detail for performing TD

simulations to determine the VDNE parameters, and in TD simulations, the external system is represented by its Thevenin equivalent circuit. Figure 4.3 represents the configuration of VDNE used for the matrix-based iterative short circuit analysis.

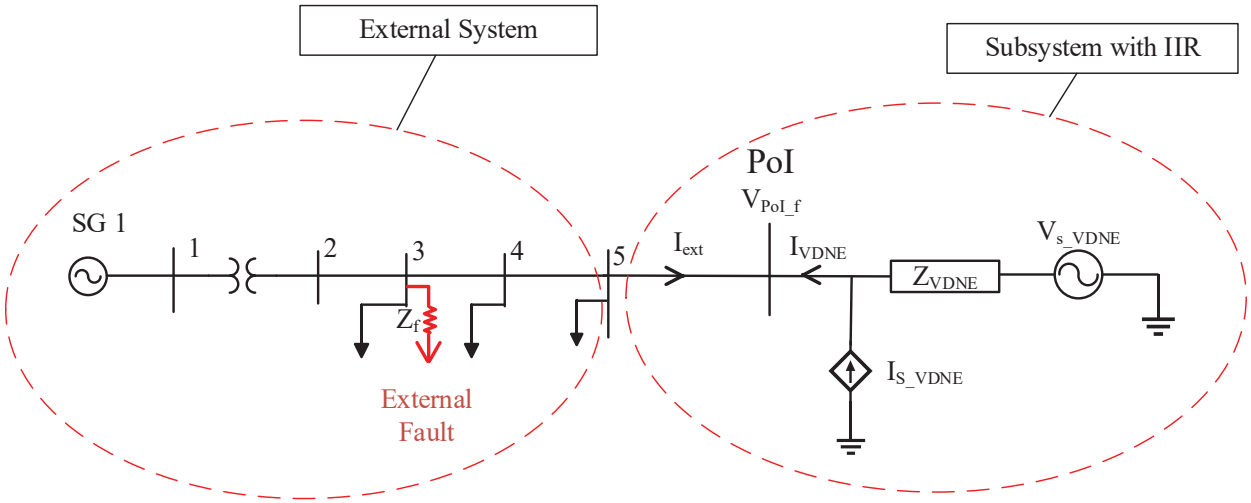

Figure 4.3 VDNE for iterative short circuit analysis

In Figure 4.3, V_{POI_f} is the post-fault voltage of the PoI. The combination of WTG and substation transformer block in Figure 4.1 represents the aggregated WTGs and the rest of the power system components including conventional synchronous generators, transformers, transmission lines, and loads are modeled in detail in the TD model. The TD model of the subsystem with IIR, including WTG and substation transformer, depicted in Figure 4.1 will then be converted into a VDNE as illustrated in Figure 4.3. The VDNE network represents the aggregated WTG model as a combination of the voltage source (V_{s_VDNE}) behind the Thévenin equivalent impedance (Z_{VDNE}) and a voltage dependent current source (I_{S_VDNE}). I_{VDNE} is the addition of converter injected current I_{S_VDNE} and the current contributed by V_{s_VDNE}. The computation of Z_{VDNE} as seen from the PoI is comprised of the complex Thévenin impedance of the subsystem with IIR up to the GSC output terminal including shunt filter impedance of the GSC output terminal and WTG unit transformer impedance; VSCs are open circuited in this calculation. In this model, the current contribution of the WTG is represented through I_{S_VDNE}. However, the calculation of I_{S_VDNE} is not straightforward

and hence required a calculation methodology. Section 4.4.1 describes the calculation procedure of the Is_{VDNE}.

4.4.1 Data Table Generation

The iterative short circuit calculation approach, which will be discussed in detail in Section 4.5 onwards, utilizes a voltage dependent network equivalent to represent a portion of the power system with high penetration of IIRs. The proposed VDNE framework utilizes a voltage dependent current source to capture the nonlinear behavior of the IIRs. The VDNE parameters are derived by repeatedly simulating a detailed model of the portion of the network with IIRs in PSCAD/EMTDC, which is heavily used for IIR integration through an automated process. The PSCAD/EMTDC model automation is accomplished through Python programming language.

This section describes the Is_{VDNE} calculation process which is determined through a measurement-based approach involving PSCAD/EMTDC simulations. In Figure 4.4, the external system is simplified into a voltage source behind its' sequence Thévenin impedance as seen at the PoI. Z_{ext} is the complex Thévenin equivalent impedance of the external grid as seen at the PoI. V_{ext} is the voltage source behind the Z_{ext} in the external system. Z_f is the fault impedance at the PoI and $\bar{V}_{POI_f}$ is the fault voltage at the PoI which will be utilized in the calculation procedure described in this section. Other symbols represent the same notation as in Figure 4.3. The data table generation process requires the following data:

- Pre-fault bus voltage matrix
- Sequence impedance data of the system components
- Faulted bus number
- Fault impedance
- Fault MVA at the PoI
- X/R ratio

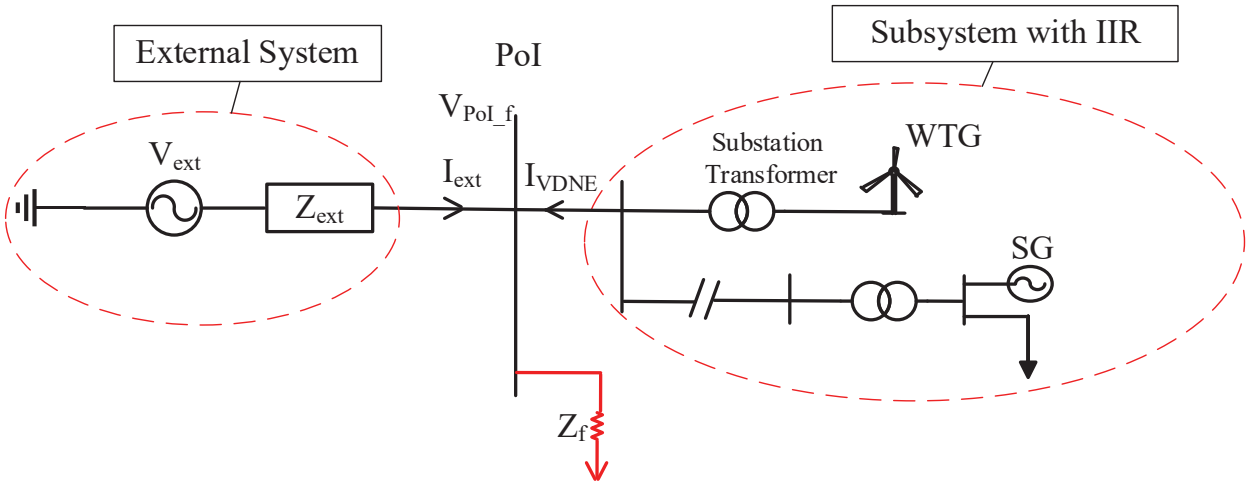

Figure 4.4 EMT simulation model used for obtaining the VDNE parameters

With the availability of short circuit capacity/fault level (*FMVA)* and X/R ratio (*XR ratio)* at the PoI, the positive sequence Thévenin impedance, Z_{ext}, at the PoI is calculated as,

$$\begin{aligned} \mathrm{R_{ext}} &= \frac{\mathrm{V_{PoI}} \times \mathrm{S_{base}}}{\mathrm{FMVA} \times \sqrt{1 + \mathrm{XR\ ratio}^2}} \\ \mathrm{X_{ext}} &= \mathrm{XR\ ratio} \times \mathrm{R_{ext}} \\ \mathrm{Z_{ext}} &= \mathrm{R_{ext}} + \mathrm{jX_{ext}} \end{aligned} \tag{4.1}$$

S_{base} is the base apparent power which is considered 100 MVA.

The objective is to formulate a set of $\bar{I}_f$ versus $\bar{V}_{POI_f}$ data by applying a series of steady-state fault conditions at the PoI by varying fault impedance Z_f at the PoI. According to the equivalent circuit depicted in Figure 4.4, I_{VDNE} is the only unknown parameter once the fault current and voltage, $\bar{I}_f$ and $\bar{V}_{PoI_f}$, are known.

The data table comprises of a series of $\bar{V}_{PoI_f}$ values varying from 0.1 pu to 1.0 pu with the steps of 0.05 pu. A series of fault impedance values is utilized to obtain the desired voltages at the PoI, and the value of Z_f required to achieve a required PoI voltage is computed as given in (*4.2*) to (*4.3*).

$$\bar{\mathrm{I}}_{\mathrm{f}} = \frac{\mathrm{n} \times \bar{\mathrm{V}}_{\mathrm{step}}}{\mathrm{Z}_{\mathrm{f}}}$$

$$\bar{I}_f = \frac{\bar{V}_{ext} - n \times \bar{V}_{step}}{Z_{ext}} \tag{4.2}$$

From (*4.2*), Z_f is computed as:

$$\mathrm{Z}_{\mathrm{f}} = \frac{\mathrm{n} \times \bar{\mathrm{V}}_{\mathrm{step}}}{\bar{\mathrm{V}}_{\mathrm{ext}} - \mathrm{n} \times \bar{\mathrm{V}}_{\mathrm{step}}} \times \mathrm{Z}_{\mathrm{ext}} \tag{4.3}$$

where *n* is the number of fault voltage steps and $\bar{\mathrm{V}}_{\mathrm{step}}$ is the minimum voltage step value.

Once the fault voltage and current are obtained, $Is\__{VDNE}$ is determined as,

$$I_{s_{VDNE}} = \mathrm{I}_{\mathrm{f}} - \mathrm{I}_{\mathrm{ext}} - \frac{(\mathrm{V}_{\mathrm{sVDNE}} - \mathrm{V}_{\mathrm{PoI}})}{Z_{VDNE}} \tag{4.4}$$

Finally, the data table will be generated by tabulating d and q components of the I_{VDNE} against $\bar{V}_{PoI_f}$. The d and q components of I_{VDNE} are calculated as follows:

$$\mathrm{I}_{\mathrm{VDNE_d}} = \mathrm{I}_{\mathrm{VDNE}} \cos(\theta)$$

$$\mathrm{I}_{\mathrm{VDNE_q}} = \mathrm{I}_{\mathrm{VDNE}} \sin(\theta) \tag{4.5}$$

I_{VDNE_d} is the d component of the converter injected current, I_{VDNE}, which is in phase with $\bar{V}_{PoI_f}$, and I_{VDNE_q} is the q component of the converter injected current, which is in quadrature to $\bar{V}_{PoI_f}$. The angle θ is the phase angle difference between $\bar{V}_{PoI_f}$ and I_{VDNE}.

4.5 Iterative Short Circuit Analysis Methodology

Once the VDNE parameters are obtained through a tabular format with the use of EMT simulation, the data can be utilized to analyze the faults in part of the network modeled in the phasor domain. Since the current injected by the WTG, I_{VDNE}, exhibits a nonlinear behavior, an iterative short circuit solution approach similar to those described in Section 2.4 is proposed to analyze short circuit conditions.

Assume a three-phase fault occurs in *bus k* in the external grid. The iterative short circuit calculation starts by calculating the initial fault current, I_{VDNE-0}, injected to the PoI. The initial fault current and fault voltage calculations for a fault at bus *k* are given by the equations (*4.8*) - (*4.10*). This is further discussed under three-phase balanced fault current calculation in Section 2.1.1.

$$\mathrm{V_k(F)} = \mathrm{V_k(0)} - \mathrm{Z_{kk} I_k(F)} \tag{4.6}$$

$$\mathrm{V_k(F)} = \mathrm{Z_f I_k(F)} \tag{4.7}$$

$$\mathrm{I_k(F)} = \frac{\mathrm{V_k(0)}}{\mathrm{Z_{kk} + Z_f}}) \tag{4.8}$$

This fault current calculation is performed in sequence domain where the subsystem containing the IIR is represented as a VDNE. This computation allows the computation of the sequence components of the fault currents If_{k1}.

The deviations of bus voltage due to the fault current leaving the faulted bus, *k,* is given by,

$$\mathrm{\Delta V_{i1}} = \mathrm{Z_1[i,k]} \times (-\mathrm{If_{k1}}) \tag{4.9}$$

where *i* is the bus number i.e. *i = 1, 2, 3, …, n.*

The post fault bus voltages are given by:

$$\mathrm{V_{F,i}^{iter}} = \mathrm{V_{i0}} + \mathrm{\Delta V_{i1}} \tag{4.10}$$

where *iter* is the iteration number and $\mathrm{V_{i0}}$ is the pre-fault bus voltage at the bus *i*.

Then the iterative short circuit analysis procedure starts. Using (4.10) it is possible to compute the voltage at the interface bus between the external system represented in phasor domain model and a portion of the power system with a wind power plant represented using VDNE. The parameters of VDNE are found from detailed TD simulations in the form of a table of currents injected to the interface bus at different voltages during a fault, as explained in Section 4.5. From this table, the

total injected current from the VDNE corresponding to the calculated fault voltage at the PoI ($V_{\mathrm{PoI_F}}^{\mathrm{iter}}$) can be obtained. Consider that the wind farm injected current is $\mathrm{I_{VDNE}}_{tbl}$.

From the data table generation process described in Section 4.4.1, the $\mathrm{I_{VDNE}}_{tbl}$ value can be calculated as follows:

$$\mathrm{I_{VDNE_{tbl}}} = \mathrm{I_{VDNE_d}} \times \frac{\mathrm{V_{PoI_F}^{iter}}}{|\mathrm{V_{PoI_F}^{iter}}|} + \mathrm{I_{VDNE_q}} \times \frac{\mathrm{V_{PoI_F}^{iter}}}{|\mathrm{V_{PoI_F}^{iter}}|}\, j \tag{4.11}$$

However, the injected current at the PoI consists of the converter current and the current contribution from $V_{s_{VDNE}}$. The total injected current at the PoI, I_{VDNE} is:

$$\mathrm{I_{VDNE}} = \mathrm{I_{VDNE_{tbl}}} + \frac{\mathrm{V_{s_{VDNE}}} - \mathrm{V_{PoI_F}^{iter}}}{\mathrm{Z_{VDNE}}} \tag{4.12}$$

Therefore, the change in fault current becomes:

$$\Delta\mathrm{I_{VDNE}} = \mathrm{I_{VDNE}} - \mathrm{I_{VDNE-0}} \tag{4.13}$$

The change in faulted bus voltages due to ΔI_{VDNE} is:

$$\Delta\mathrm{V_{fVDNE}} = \mathrm{Z1[i, PoI]} \times \Delta\mathrm{I_{VDNE}} \tag{4.14}$$

Then, the change in fault current in the faulted bus due to the deviation of the injected current from the WTG becomes:

$$\Delta\mathrm{If_k} = \frac{\Delta\mathrm{V_{fVDNE}[k]}}{\mathrm{Z[k,k]} + \mathrm{Z_f}} \tag{4.15}$$

According to the above calculations, the fault bus voltages can be updated as:

$$\Delta\mathrm{V_{f_{VDNE}}^{\Delta}} = \mathrm{Z[i,k]} \times (-\Delta\mathrm{If_k}) \tag{4.16}$$

$$\mathrm{V_{POI_i}^{iter+1}} = \mathrm{V_{0i}} + \Delta\mathrm{V_{fVDNE}} + \Delta\mathrm{V_{f_{fVDNE}}^{\Delta}}$$

Then, the difference in $V_{POI_i}^{iter}$ between consecutive iterations is obtained to evaluate the convergence criteria:

$$|V_{PoI_i}^{iter+1} - V_{PoI_i}^{iter}| < \varepsilon \quad (4.17)$$

The iterative short circuit calculation process is depicted in Figure 4.5.

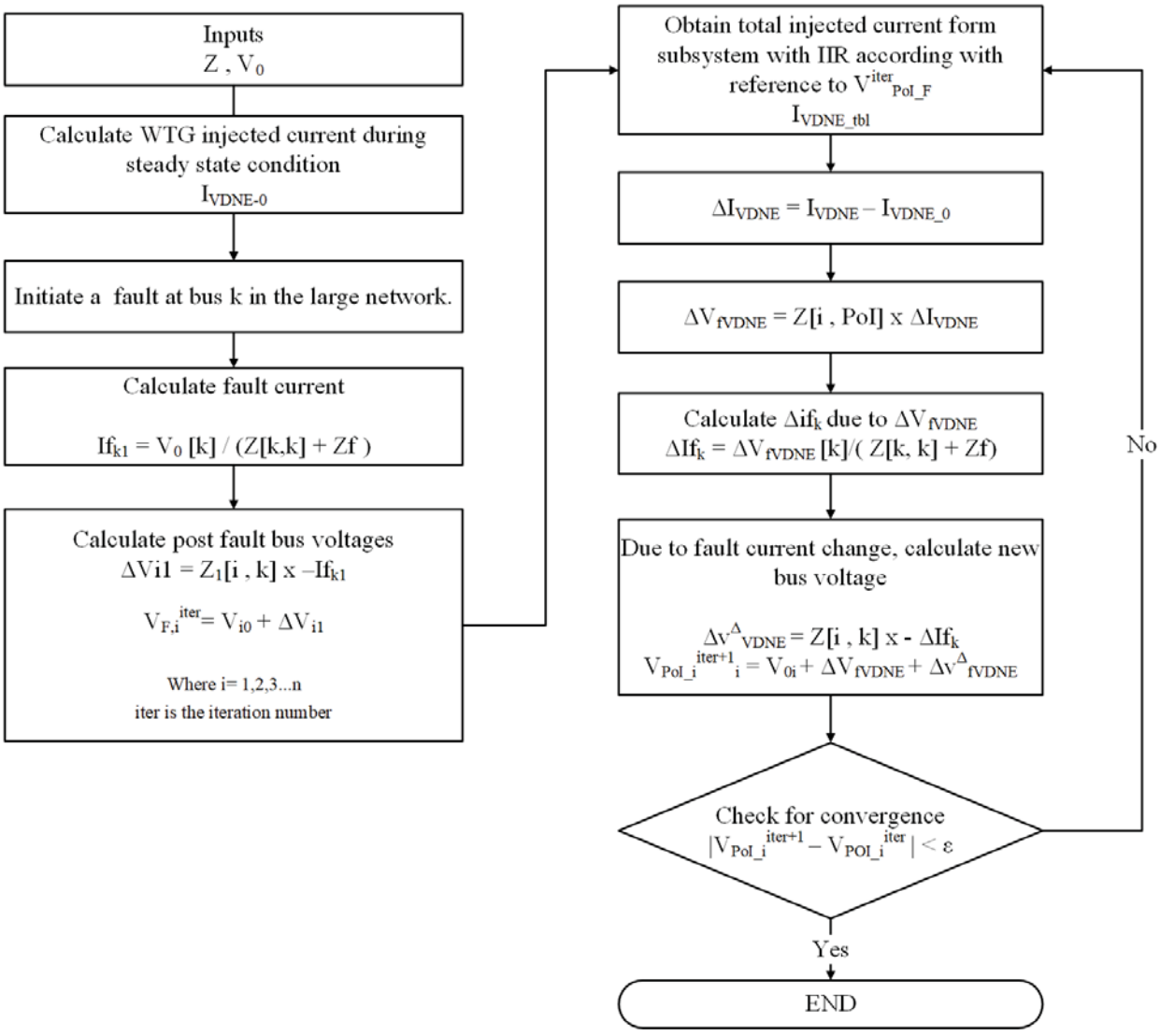

Figure 4.5 Iterative short circuit calculation process

4.6 Test Case 1: 7-bus Test System

The test system consists of seven buses and four transmission lines, Bus 1 is the slack bus, and a wind power plant is connected at Bus 6. The WPP is represented as an aggregated model of 35 WTGs of Type IV WTGs, each rated at 2 MW. The schematic diagram of the 7-bus test system is illustrated in Figure 4.6.

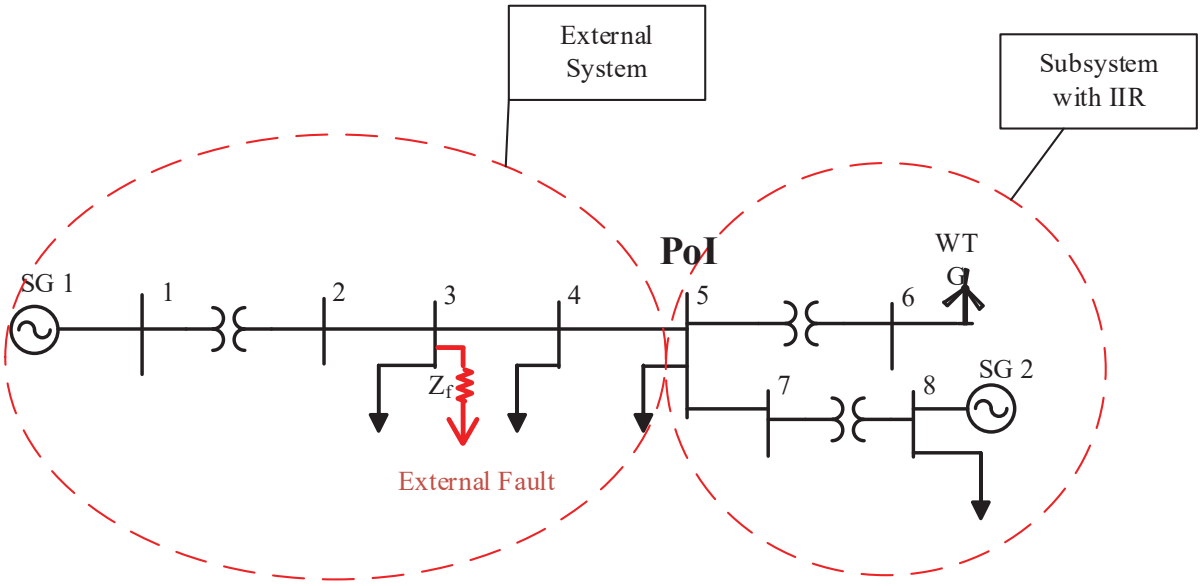

Figure 4.6 7-bus radial test system

The first step is to create an EMT simulation case of subsystem consisting of the wind power plant in PSCAD/EMTDC for the purpose of obtaining parameters of VDNE. The simulation case is initialized from a power flow solution. The input parameters to perform VDNE calculation in PSCAD/EMTDC environment is given in Table 4.1.

Table 4.1 Input parameters for VDNE calculation procedure on PSCAD/EMTDC, 7-bus test system

PoI	Bus 5
Pre-fault bus voltage at PoI (pu)	$1.0190 \angle 26.13^{o}$
Sequence impedance data of the large system (pu)	$Z^{+} = 0.0394 + 0.1165j$
Fault MVA at the PoI (MVA)	813.2496
X/R ratio at the PoI	2.9597

VDNE parameters of the 7-bus test system are obtained with the proposed mathematical model depicted in Figure 4.3. A sample set of d and q components of the converter injected current, I_{VDNE}, is tabulated in Table 4.2 and Table 4.3. I_{VDNE_d} and I_{VDNE_q} are measured at the PoI after 3-cycles and 6-cycles respectively of the fault inception. The current mearements are obtained at nominal wind speed which is 10 kmph.

Table 4.2 I_{VDNE_d} and I_{VDNE_q} measured 3-cycles after fault inception for the WPP connected to 7-bus test system in pu

$\lvert V_{PoI_f} \rvert$	$\lvert I_{VDNE_d} \rvert$ Wind speed = 10 kmph	$\lvert I_{VDNE_q} \rvert$ Wind speed = 10 kmph
0.010	0.696	-0.139
0.061	0.699	-0.132
0.113	0.687	-0.176
0.165	0.683	-0.168
0.216	0.684	-0.142
0.267	0.689	-0.103
0.318	0.686	-0.078
0.368	0.691	-0.029
0.418	0.687	-0.002
0.468	0.688	0.033
0.518	0.675	0.043
0.568	0.674	0.075
0.617	0.672	0.105
0.666	0.669	0.131
0.714	0.666	0.152
0.762	0.666	0.181
0.811	0.658	0.194
0.858	0.656	0.227
0.904	0.642	0.245

Table 4.3 I_{VDNE_d} and I_{VDNE_q} measured 6-cycles after fault inception for the WPP connected to 7-bus test system in pu

$\lvert V_{PoI_f} \rvert$	$\lvert I_{VDNE_d} \rvert$ Wind speed = 10 kmph	$\lvert I_{VDNE_q} \rvert$ Wind speed = 10 kmph
0.174	0.531	0.154
0.217	0.539	0.128
0.261	0.545	0.109
0.305	0.551	0.108
0.350	0.557	0.106
0.394	0.560	0.113
0.439	0.564	0.117
0.483	0.570	0.123
0.528	0.576	0.131
0.573	0.580	0.141
0.617	0.585	0.154
0.661	0.588	0.168
0.705	0.591	0.182
0.748	0.592	0.197
0.791	0.593	0.213
0.833	0.593	0.232
0.874	0.597	0.255
0.915	0.602	0.278

I_{VDNE_d} and I_{VDNE_q} of the WPP with respect to the fault voltage at the PoI for 3-cycles and 6-cycles are depicted in Figure 4.7 and Figure 4.8 respectively. Third degree polynomials are fitted to the values of d and q-axis currents in tables with a 95% confidence bound. These polynomials facilitate computation of the values of I_{VDNE_d} and I_{VDNE_q} at intermediate $\lvert V_{PoI_f} \rvert$ values, that are not in the tables.

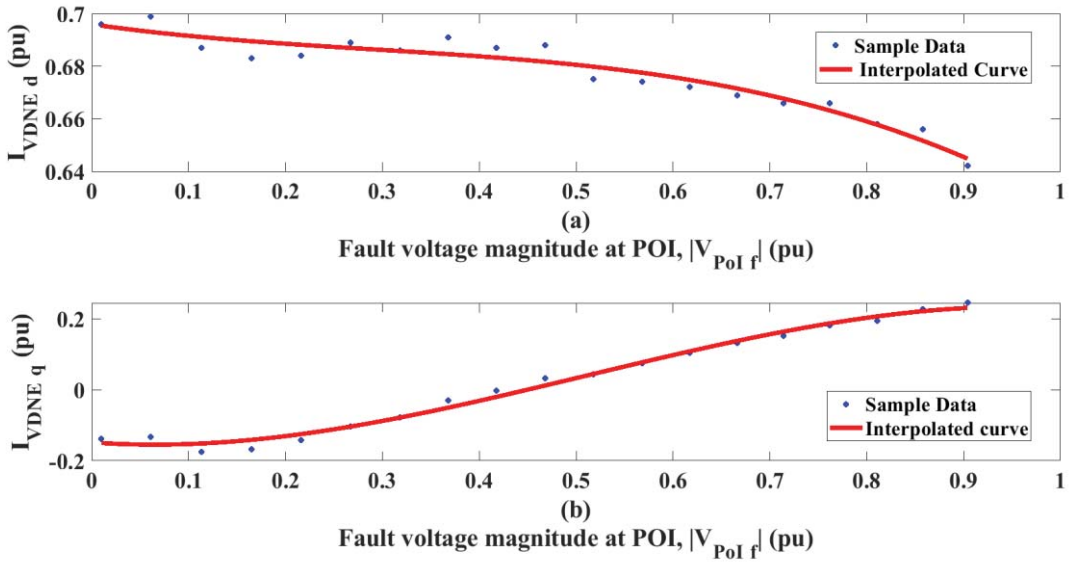

Figure 4.7 Variations of (a) I_{VDNE_d} and (b) I_{VDNE_q} (in pu) with the voltage magnitude at the PoI during three-phase faults. Measurements are taken 3-cycles after the fault inception.

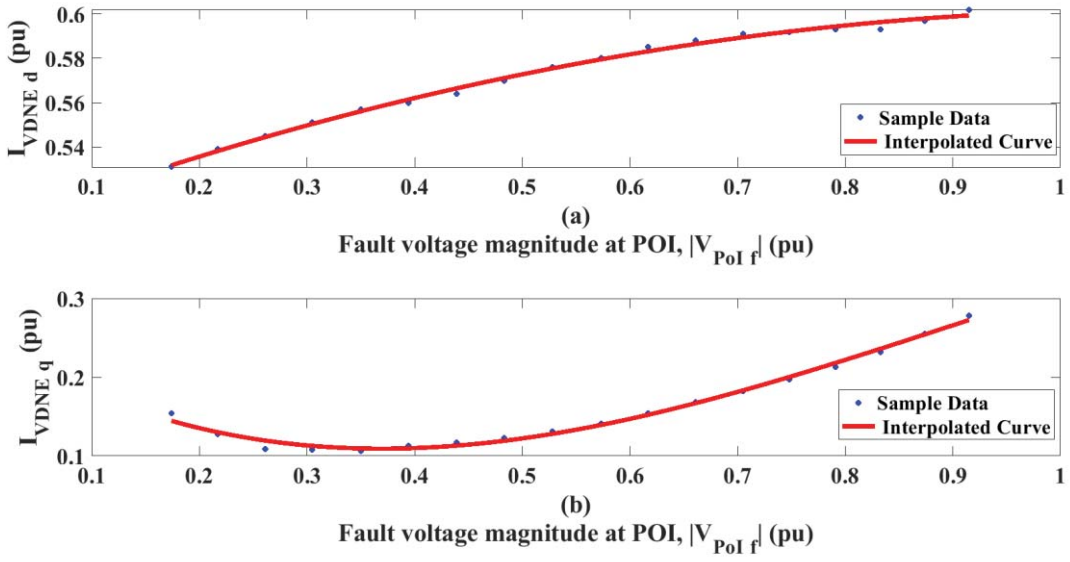

Figure 4.8 Variations of (a) I_{VDNE_d} and (b) I_{VDNE_q} (in pu) with the voltage magnitude at the PoI during three-phase faults. Measurements are taken 6-cycles after the fault inception.

Once all the parameters of the VDNE of the 7-bus test system are identified, the iterative short circuit analysis is performed following a three-phase-to-ground fault applied at Bus 3, a location

outside the subsystem that contains the wind power plant. The fault resistance and the number of cycles after the inception of the fault are varied to obtain the results. In order to test the accuracy of the results, the complete system including the wind power plant is simulated in PSCAD/EMTD using EMT models. The fault is applied at Bus 3, and the phasor values of the fault current are computed considering once cycle data window captured, 3-cycles and 6-cycles after the inception of the fault.

The fault current, the voltage and current at the interface between the VDNE and the external network during the 3-phase to ground fault at Bus 3 are shown in Table 4.4 to Table 4.6 for measurements taken 3-cycles after the inception of fault. Voltage and current values are given in pu. The fault current and voltage values of the proposed model are compared with the EMT solutions. The errors in the fault voltage and the fault current are higher for the bolted three-phase-to-ground fault and the percentage error is decreasing with the increasing fault impedance.

Table 4.4 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 3-cycles after fault inception: Z_f = 0 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.218 ∠ 42.03º	0.211 ∠ 42.39 º	3.3
V_{f_3}	0	0	0
I_f	9.55 ∠ -44.59 º	9.252 ∠ -45.37 º	3.2
I_{PoI}	0.753 ∠ 29.35 º	0.752 ∠ 35.09 º	0.1

Table 4.5 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 3-cycles after fault inception: Z_f = 10 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.293 ∠ 11.37 º	0.286 ∠ 10.55 º	2.4
V_{f_3}	0.174 ∠ -36.36 º	0.172 ∠ -37.16 º	1.7
I_f	9.16 ∠ -36.78 º	9.103 ∠ -37.22 º	0.6
I_{PoI}	0.713 ∠ 6.62 º	0.701 ∠ 9.05 º	1.7

Table 4.6 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 3-cycles after fault inception: Z_f = 20 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.403 ∠ 0.862 º	0.395 ∠ 0.331 º	2.0
V_{f_3}	0.321 ∠ -29.5 º	0.317 ∠ -29.71 º	1.3
I_f	8.478 ∠ -29.57 º	8.384 ∠ -29.71 º	1.1
I_{PoI}	0.693 ∠ 3.30 º	0.681 ∠ 4.94 º	1.7

The fault current, the voltage and current at the interface between the VDNE and the external network during a 3-phase to ground fault at Bus 3 are shown in Table 4.7 to Table 4.9 for measurements taken 6-cycles after the inception of the fault. The highest errors in the fault voltage and fault current error are observed for the bolted three-phase-to-ground fault and with the increase of fault impedance, the errors decreased similar to the results taken 3-cycles after the fault inception.

Table 4.7 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 6-cycles after fault inception: Z_f = 0 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.313 ∠ 37.6 º	0.300 ∠ 40.38 º	4.2
V_{f_3}	0	0	0
I_f	8.483 ∠ -48.86 º	8.266 ∠ -48.19 º	2.6
I_{PoI}	0.639 ∠ 21.11 º	0.624 ∠ 55.45 º	2.4

Table 4.8 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 6-cycles after fault inception: Z_f = 10 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.421 ∠ 35.04 º	0.406 ∠ 38.80 º	3.7
V_{f_3}	0.257 ∠ 37.15 º	0.252 ∠ 39.32 º	2.0
I_f	7.178 ∠ 52.1 º	7.067 ∠ -50.68 º	1.6
I_{PoI}	0.635 ∠ 27.33 º	0.62 ∠ 53.44 º	2.4

Table 4.9 Test case 1, comparison between phasor domain and EMT solution for LLLG fault at Bus 3, currents and voltages 6-cycles after fault inception Z_f = 20 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.546 ∠ 34.41 º	0.532 ∠ 36.57 º	2.6
V_{f_3}	0.410 ∠ 35.07 º	0.404 ∠ 36.48 º	1.6
I_f	5.737 ∠ -54.16 º	5.671 ∠ -53.51 º	1.2
I_{PoI}	0.622 ∠ 39.13 º	0.635 ∠ 51.74 º	2.1

4.7 Test Case 2: 39-Bus Test System

The test system is composed of 39 buses with a subsyetm that includes a WPP connected at Bus 39. Bus 37 is the slack bus. The WPP is represented using an aggregated model of 150 Type IV WTGs, each with 2 MW active power rating. The schematic diagram of IEEE 39-bus test system with the added WPP is illustrated in Figure 4.9.

Power flow simulations are initialized from a flat voltage profile where pre-fault bus voltage at each bus is assumed to be 1 pu magnitude and 0-degree phase angle. The input parameters to perform VDNE calculation in PSCAD/EMTDC environment are given in Table 4.10. The parameters of the VDNE that represent the subsystem with WPP connected to 39-bus test system are obtained with the proposed mathematical model depicted in Figure 4.3

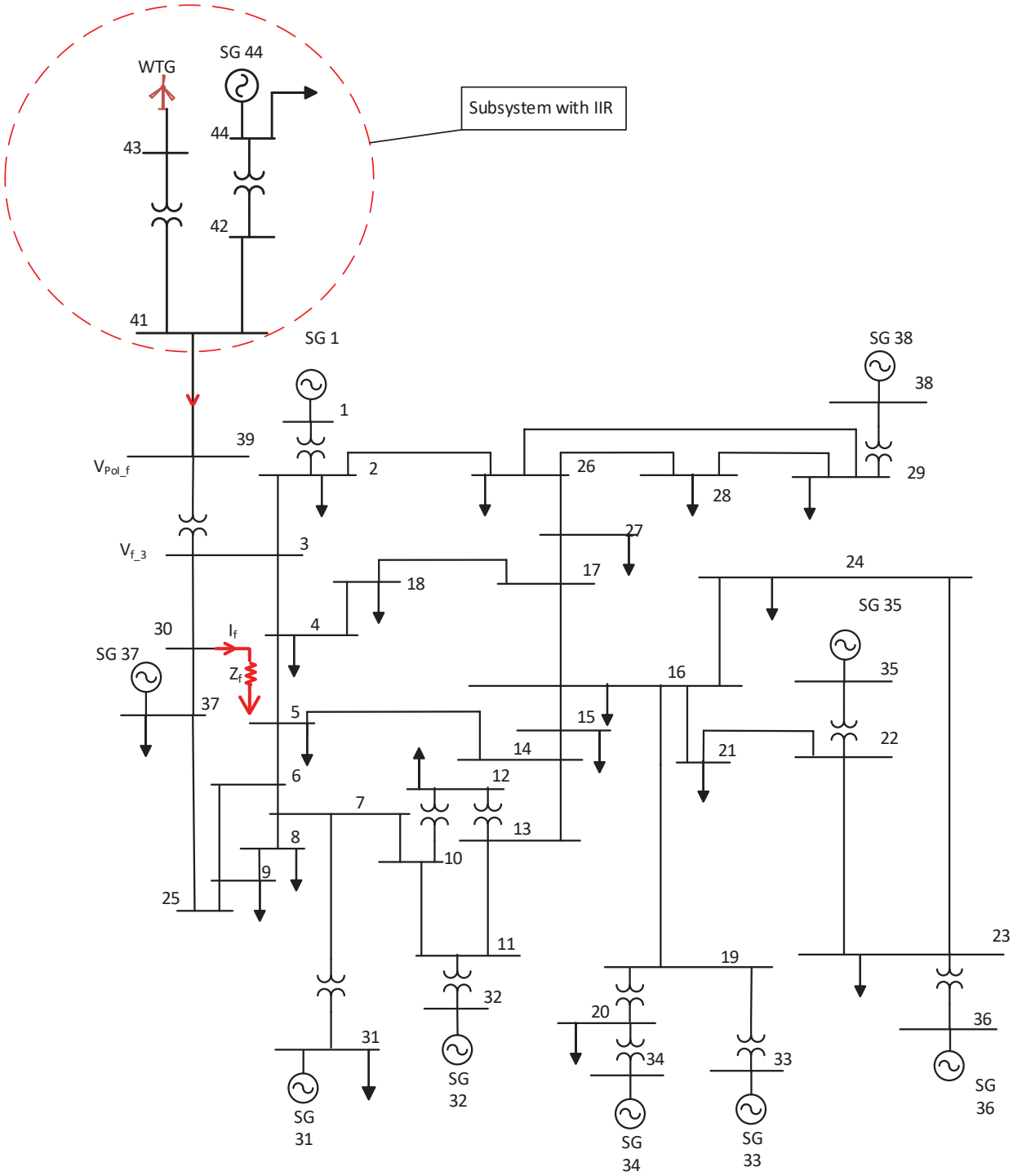

Figure 4.9 IEEE 39-bus test system augmented with a wind power plant

Table 4.10 Input parameters for VDNE calculation procedure on PSCAD/EMTDC, IEEE 39-bus system

PoI	39
Pre-fault bus voltage at PoI (pu)	$1.0 \angle 0.0^{o}$
Sequence impedance data of the large system (pu)	0.008 + 0.0368j
Fault MVA at the PoI (MVA)	2661.090
X/R ratio at the PoI	4.749

Sample sets of converter injected currents I_{VDNE_d} and I_{VDNE_q} measured 3-cycles and 6-cycles after fault inception are tabulated in Table 4.11 and Table 4.12 respectively. The current mearements are obtained at nominal wind speed which is 10 kmph.

Table 4.11 I_{VDNE_d} and I_{VDNE_q} measured 3-cycles after fault inception for the WPP connected to 39-bus test system in pu

$\lvert V_{PoI_f} \rvert$	$\lvert I_{VDNE_d} \rvert$ Wind speed = 10 kmph	$\lvert I_{VDNE_q} \rvert$ Wind speed = 10 kmph
0.113	0.469	-2.076
0.167	0.864	-1.794
0.220	1.460	-1.458
0.272	1.749	-1.220
0.324	1.937	-1.020
0.375	2.054	-0.837
0.426	2.100	-0.704
0.479	2.103	-0.626
0.528	2.187	-0.452
0.579	2.188	-0.373
0.630	2.176	-0.306
0.678	2.228	-0.163
0.729	2.252	-0.105
0.779	2.263	-0.049
0.828	2.265	0.034
0.874	2.250	0.160
0.918	2.233	0.304

Table 4.12 I_{VDNE_d} and I_{VDNE_q}measured 6-cycles after fault inception for the WPP connected to 39-bus test system in pu

$\lvert V_{PoI_f} \rvert$	$\lvert I_{VDNE_d} \rvert$	$\lvert I_{VDNE_q} \rvert$
0.254	1.753	-0.247
0.299	1.775	-0.231
0.345	1.791	-0.225
0.391	1.811	-0.200
0.437	1.840	-0.174
0.483	1.871	-0.139
0.528	1.901	-0.094
0.574	1.927	-0.050
0.619	1.974	0.013
0.665	2.002	0.065
0.709	2.019	0.114
0.754	2.055	0.182
0.796	2.086	0.260
0.840	2.092	0.309
0.882	2.066	0.363
0.924	2.043	0.394

The variations of I_{VDNE_d} and I_{VDNE_q} of the WPP with the fault voltage at the PoI are depicted in Figure 4.10 and Figure 4.11 for the measurements taken 3-cycles and 6-cycles after the fault inception respectively. The third-degree polynomial fitted the data given in tables with a 95% confidence bound are also shown on the same plots.

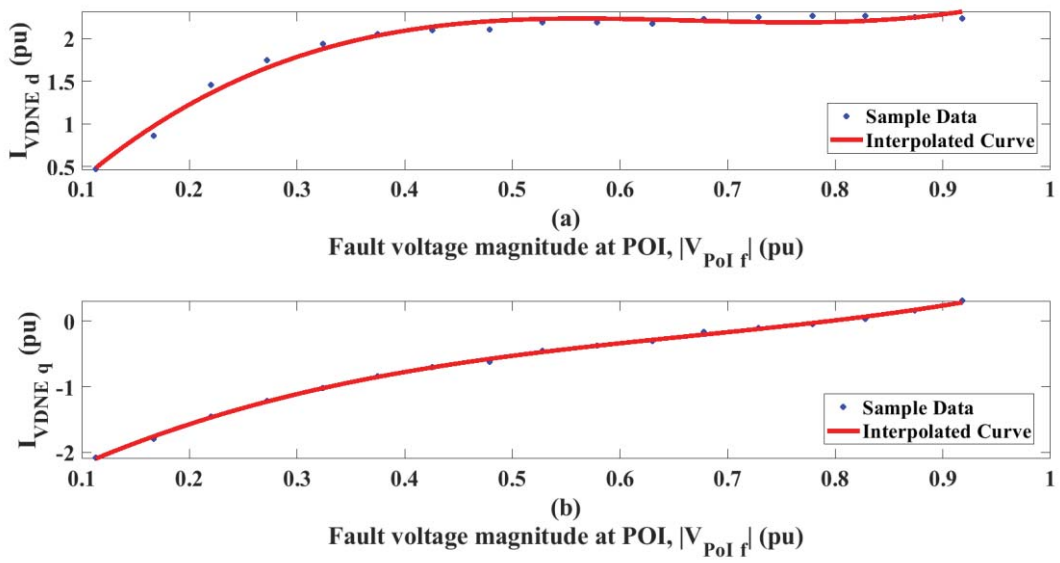

Figure 4.10 Variations of (a) I_{VDNE_d} and (b) I_{VDNE_q} (in pu) with the voltage magnitude at the PoI during three-phase faults. Measurements are taken 3-cycles after the fault inception.

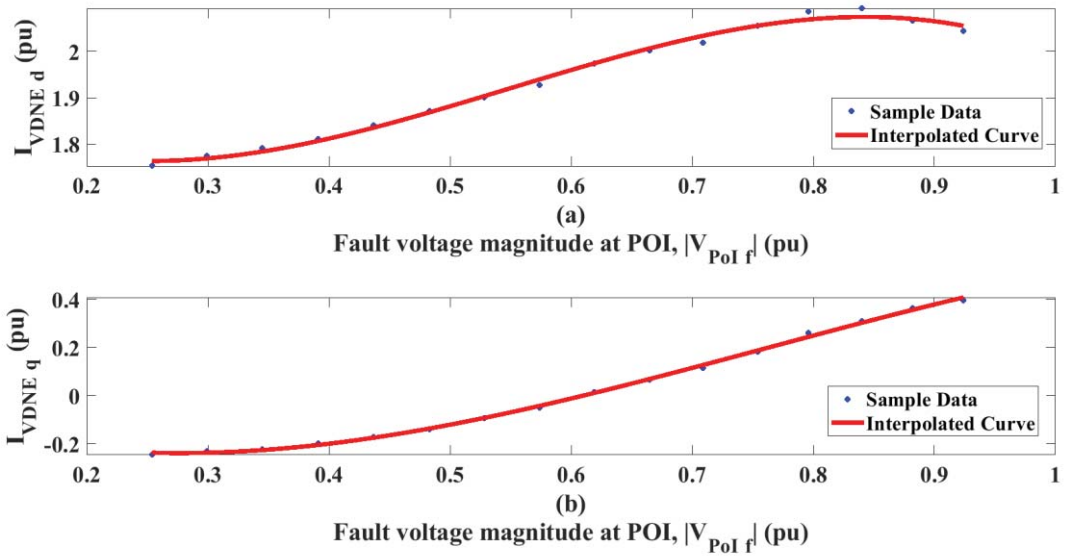

Figure 4.11 Variations of (a) I_{VDNE_d} and (b) I_{VDNE_q} (in pu) with the voltage magnitude at the PoI during three-phase faults. Measurements are taken 6-cycles after the fault inception.

Once all the parameters of the VDNE of the 39-bus test system are identified, the iterative short circuit analysis is performed for a three-phase-to-ground fault applied at a Bus 30, a location

outside the part of the network modeled in VDNE. The fault resistance is varied, and the calculations are made 3 and 6-cycles after the inception of the fault. The results are compared with fault analysis results obtained by simulating the complete power system including the WPP in PSCAD/EMTD for verifying the accuracy.

The computed fault currents, the current and voltage at the PoI during the three-phase to ground fault at Bus 30 are shown in Table 4.13 to Table 4.15 for 3-cycles after fault inception and in Table 4.16 to Table 4.18 for 6-cycles after fault inception. The voltage and current values are given in pu. When compared with the EMT solutions, the fault current and voltage values obtained from phasor domain computations using the iterative method, the highest percentage error remained below 2.5%. Compared to the 7-bus system, the WPP model in 39-bus system is connected to a strong grid having an X/R ratio of 4.75.

Table 4.13 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 3-cycles after fault inception: $Z_f = 0$ ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.918 ∠ -33.97 º	0.917 ∠ -33.60 º	0.1
V_{f_3}	0	0	0.0
I_f	6.150 ∠ -97.37 º	6.074 ∠ -97.21 º	1.3
I_{PoI}	2.26 ∠ -46.68 º	2.29 ∠ -32.95 º	1.4

Table 4.14 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 3-cycles after fault inception: $Z_f = 10$ ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{PoI_f}	0.920 ∠ -34.62 º	0.921 ∠ -34.22 º	0.1
V_{f_3}	0.112 ∠ -91.81 º	0.11 ∠ -91.53 º	1.8
I_f	5.950 ∠ -92.18 º	5.838 ∠ -91.53 º	1.9
I_{PoI}	2.260 ∠ -47.47 º	2.273 ∠ -34.1 º	0.6

Table 4.15 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 3-cycles after fault inception: Z_f = 20 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{f_PoI}	0.929 ∠ -35.15 º	0.927 ∠ -34.72 º	0.2
V_{f_3}	0.215 ∠ -86.93 º	0.211 ∠ -86.33 º	1.9
I_f	5.69 ∠ -87.05 º	5.569 ∠ -86.33 º	2.2
I_{PoI}	2.260 ∠ -47.75 º	2.261 ∠ -34.91 º	0.01

Table 4.16 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 6-cycles after fault inception: Z_f = 0 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{f_PoI}	0.920 ∠ -34.29 º	0.909 ∠ -33.75 º	1.2
V_{f_3}	0	0	0.0
I_f	6.03 ∠ -98.54 º	6.011 ∠ -97.21 º	0.3
I_{PoI}	2.117 ∠ -52.22 º	2.116 ∠ -25.68 º	0.05

Table 4.17 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 6-cycles after fault inception: Z_f = 10 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{f_PoI}	0.927 ∠ -34.92 º	0.914 ∠ -34.35 º	1.4
V_{f_3}	0.110 ∠ -92.78 º	0.109 ∠ -91.51 º	0.9
I_f	5.890 ∠ -92.78 º	5.778 ∠ -91.51 º	1.9
I_{PoI}	2.105 ∠ -51.42 º	2.108 ∠ -26.75 º	0.2

Table 4.18 Test case 2, comparison between phasor domain and EMT solution for LLLG fault at Bus 30, currents and voltages 6-cycles after fault inception: Z_f = 20 ohm

	Phasor Domain Solution	EMT solution	Magnitude error %
V_{f_PoI}	0.930 ∠ -35.39 º	0.920 ∠ -34.84 º	1.1
V_{f_3}	0.251 ∠ -87.39 º	0.208 ∠ -86.28 º	0.9
I_f	5.61 ∠ -87.39 º	5.513 ∠ -86.28 º	1.7
I_{PoI}	2.110 ∠ -51.09 º	2.106 ∠ -27.49 º	0.2

4.8 Concluding Remarks

This chapter proposed a mathematical framework and automated process to obtain a voltage dependent network equivalent to represent a subsystem with Type IV of WTGs for short circuit analysis. The proposed VDNE framework utilizes a voltage dependent current source to capture the nonlinear behavior of the WTGs. The VDNE parameters were derived by repeatedly simulating a detailed model of the WPP and an equivalent of the external network in PSCAD/EMTDC through an automated process.

An iterative short circuit analysis algorithm was presented to incorporate the nonlinear behavior of the WTGs to get the correct phasor solution. The proposed VDNE based iterative short circuit analysis methodology was tested by simulating a three-phase to ground fault on 7-bus test system and IEEE 39-bus test system. The fault calculation was carried out by varying the fault impedance for two different time points after the fault inception. The phasor solution obtained by the proposed model was compared with EMT time-domain simulation results and the results were proven accurate.

Chapter 5

Conclusions

5.1 Introduction

This thesis proposed a methodology for automated calculation of bus bar short circuit currents of a power system modeled in PSCAD/EMTDC. Then a method to obtain a VDNE of a power network consisting of a wind power plant with Type-IV WTGs was developed, and the developed VDNE was used for phasor domain short circuit analysis through an iterative procedure.

5.2 Summary and Conclusions

After the review of literature on fault analysis in conventional power systems and power systems with inverter-interface resources, a methodology for automated calculation of busbar fault currents in a conventional power system modeled in PSCAD/EMTDC environment was proposed in Chapter 3. The purpose of this development was to obtain adequately accurate values of fault currents of a given power system modeled in PSCAD/EMTDC simulation environment in a quick manner, without resorting to time-domain simulations. The main feature of this method was the extraction of Thévenin impedances of sequence networks at a busbar using harmonic impedance solution (frequency scanner) tool available in PSCAD/EMTDC. Pre-fault bus voltages were to be obtained from a power flow solution or from one of the approaches prescribed in the IEEE Std 3002.3-2018 or IEC standards: assuming a flat voltage profile (1 pu magnitude and 0-degree phase angle) or applying user definable voltage factor known as *c* factor. The whole calculation procedure was automated using Python scripting. The test results presented in Chapter 3 illustrated the accuracy of the methodology in comparison to the fault currents obtained through time-domain

simulations performed in PSCAD/EMTDC for different types of faults. The proposed method provided accurate results and in most cases, the fault current magnitude difference was less than 0.5% and the phase angle difference was less than 0.3%. The developed Python based tool with a simple user interface allows users to specify busbars where the fault currents are to be computed, fault types and fault impedances, and perform multiple fault current calculations in a single run. However, user written component models interfaced to EMT model may not be taken into account in the process of Thévenin impedance evaluation resulting in inaccurate busbar fault currents.

In Chapter 4, a method for accurate calculation of short circuit currents in a power system with inverter-interfaced resources using phasor domain techniques was proposed. In this approach, a voltage dependent network equivalent was used to represent a portion of the power system with high penetration of IIR. The proposed VDNE framework utilized a voltage dependent current source to capture the nonlinear behavior of the IIRs. An automated process was developed to obtain the VDNE parameters by repeatedly simulating a detailed model of the portion of the network with IIRs in PSCAD/EMTDC. The automated process allows conviniet calculation of VDNE parameters for different cases if necessary, for example considering different pre-fault operating conditions of the WPP. An iterative short circuit analysis algorithm was used to incorporate the nonlinear behavior of the WTGs to get the correct phasor solution. The results of the proposed VDNE based iterative short circuit analysis methodology was compared with the fault currents obtained from time-domain simulations in PSCAD/EMTDC for three-phase to ground faults for two different test systems: 7-bus test system and IEEE 39-bus test system. The fault calculation was carried out by varying fault impedance for two different time points after the fault inception. The phasor solutions obtained by the proposed model were compared with EMT time-domain simulation results and the results were proven accurate.

5.3 Contributions

During the course of research, the following contributions were made:

Development of a methodology to perform bus bar fault analysis in PSCAD/EMTDC environment without resorting to full time-domain simulations and evaluation of its accuracy through case studies.

Development of a Python based tool equipped with a graphical user interface to implement the proposed busbar fault analysis method exploiting PSCAD/EMTDC automation capabilities.

Development of a methodology and automation tool to obtain a voltage dependent network equivalent of a power system with inverter-interfaced resources through EMT simulations performed in PSCAD/EMTDC. The inverter-interfaced resource can be modeled with detailed controls and the model can incorporate black boxed models of IIRs.

Development of an iterative phasor domain short circuit analysis approach for power systems with IIRs, where the subnetwork around IIR is represented as a VDNE. The methodology was validated for three-phase faults.

5.4 Future Work

In order to further develop the phasor domain iterative fault analysis, the following future work is proposed.

- Extension of the iterative fault analysis methodology to perform unbalanced fault analysis. This requires obtaining VDNEs of negative and zero sequence networks through automated PSCAD/EMTDC simulations.
- Extension of the iterative short circuit procedure to incorporate multiple IIR locations in a single network.

Appendix. A 7-bus Test System

Table A.1 7-bus test system bus data

Bus Number	Type	|V| (pu)	Gen (MW)	Shunt (MVAr)	Load	
					P (MW)	Q (MVAr)
1	Slack	1.036	300	-	-	-
2	P-Q	-	-	-	-	-
3	P-Q	-	-	-	150	75
4	P-Q	-	-	20	90	30
5	P-Q	-	-	60	75	30
6	P-V		70	-	-	-
7	P-Q	-	-	-	-	-
8	P-V		2	-	5	5

Table A.2 7 bus test system transformer data

From Bus	To Bus	X (pu)	Tap Ratio
1	2	0.002	1
5	6	0.0125	1
7	8	1	1

Table A.3 7-bus test system transmission line data

From Bus	To Bus	R (pu)	X (pu)	B (pu)
2	3	0.00572	0.045555	0.091305
3	4	0.006864	0.054666	0.109566
4	5	0.00572	0.045555	0.091305
5	7	0.003432	0.027333	0.054783

Table A.4 7-bus test system pre-fault voltage and phase angle data

Bus	|V| (pu)	V phase angle (degree)
1	1.036	-0.4522
2	1.0342	29.27
3	1	25.11
4	1.0068	24.39
5	1.019	26.13
6	1.005	20.51
7	1.006	19.95
8	0.968	-12.2

Appendix. B IEEE 14-Bus Test System with Modified WTG

Table B.1 IEEE 14-bus system bus data

Bus Number	Type	|V| (pu)	Gen (MW)	Shunt (MVAr)	Load	
					P (MW)	Q (MVAr)
1	Slack	1.060	-	-	-	-
2	PV	1.045	40	-	21.7	12.7
3	PV	1.010	0	-	94.2	19.0
4	PQ	-	-	-	47.8	-3.9
5	PQ	-	-	-	7.6	1.6
6	PV	1.070	0	-	11.2	7.5
7	PQ	-	-	-	-	-
8	PV	1.090	0	-	-	-
9	PQ	-	-	190	29.5	16.6
10	PQ	-	-	-	9.0	5.8
11	PQ	-	-	-	3.5	1.8
12	PQ	-	-	-	6.1	1.6
13	PQ	-	-	-	13.5	5.8
14	PQ	-	-	-	14.9	5.0

Table B.2 IEEE 14-bus system transformer data

From Bus	To Bus	R (pu)	X (pu)	Tap Ratio
4	7	0.0	0.20912	0.978
4	9	0.0	0.55618	0.969
5	6	0.0	0.25202	0.932

Table B.3 IEEE 14-bus system transmission line data

From Bus	To Bus	R (pu)	X (pu)	B (pu)
1	2	0.01938	0.05917	0.0264
1	5	0.05403	0.22304	0.0246
2	3	0.04699	0.19797	0.0219
2	4	0.05811	0.17632	0.0187
2	5	0.05695	0.17388	0.0170
3	4	0.06701	0.17103	0.0173
4	5	0.01335	0.04211	0.0064
6	11	0.09498	0.19890	-
6	12	0.12291	0.25581	-
6	13	0.06615	0.13027	-
7	8	0.0001	0.17615	-
7	9	0.0001	0.1101	-
9	10	0.03181	0.08450	-
9	14	0.12711	0.27038	-
10	11	0.08205	0.19207	-
12	13	0.22092	0.19988	-
13	14	0.17093	0.34802	-

Appendix. C Bus Impedance Matrix Formation Algorithm

The Bus impedance matrix, Z_{Bus}, formation algorithm is a computationally attractive step-by-step programmable technique. The algorithm proceeds by adding a branch by branch to the existing system. The main advantage of this algorithm is that it does not require complete rebuilding of Z_{Bus}. The proof of the Z_{Bus} formation equations mentioned below are given in [48].

In the below context, i and j denote old buses, r denotes the reference bus and k denotes the new bus. Assume that Z_{Bus} is built up to a certain stage and the addition of another branch,

Type I modification: Addition of a branch with impedance z_b from a new bus *k* to the reference bus *r*.

$$Z_{Bus(new)} = \begin{bmatrix} Z_{Bus(old)} & 0 \\ 0 & z_b \end{bmatrix} \tag{C.1}$$

Type II modification: Addition of a branch with impedance z_b from a new bus *k* to the existing bus *i.* Suppose that the ith column of Z_{Bus} is Z_i and iith element of Z_{Bus} is Z_{ii}.

$$V_k = Z_b I_k + V_i \tag{C.2}$$

$$V_k = Z_{i1} I_1 + Z_{i2} I_2 + \cdots + Z_{ii} I_i + \cdots + Z_{in} I_n + (Z_{ii} + Z_b) I_k \tag{C.3}$$

$$Z_{Bus(new)} = \begin{bmatrix} Z_{Bus(old)} & Z_i \\ Z_i^T & Z_{ii} + z_b \end{bmatrix} \tag{C.4}$$

Where,

$$Z_i = \begin{bmatrix} Z_{1i} \\ Z_{2i} \\ Z_{3i} \\ \vdots \\ Z_{ni} \end{bmatrix} \tag{C.5}$$

Type III Modification: Addition of a branch with impedance z_b from an existing bus *i* to the reference bus r.

Considering Type II modification in (C.4),

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ 0 \end{bmatrix} = \begin{bmatrix} Z_{Bus(old)} & Z_i \\ Z_i^T & Z_{ii} + z_b \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ I_k \end{bmatrix} \tag{C.6}$$

Where Z_i is given in (C.5). The voltage at $(n+1)^{th}$ bus is equal to the voltage at the reference bus which is equal to zero. The $Z_{Bus(new)}$ is then obtained as follows by performing Kron Reduction [49] on (C.6).

$$\begin{aligned} 0 &= Z_{i1}I_1 + Z_{i2}I_2 + \ldots + Z_{in}I_n + (Z_{ii} + z_b)I_k \\ I_k &= -\frac{1}{Z_{ii} + z_b}\left(Z_{i1}I_1 + Z_{i2}I_2 + \cdots + Z_{in}I_n\right) \end{aligned} \tag{C.7}$$

Substituting (C.*7*) in (C.*6*) and rearranging the matrix,

$$Z_{Bus(new)} = Z_{Bus(old)} - \frac{1}{Z_{ii} + z_b} \begin{bmatrix} Z_{1i} \\ Z_{2i} \\ \vdots \\ Z_{ni} \end{bmatrix} \begin{bmatrix} Z_{i1} & Z_{i2} & \cdots & Z_{in} \end{bmatrix} \tag{C.8}$$

Type IV Modification: Addition of a branch with impedance z_b between two existing buses *i* and *j*.

Suppose that the *i*th and *j*th columns of the Z_{Bus} are Z_i and Z_j respectively. Then,

$$Z_{Bus(new)} = Z_{Bus(old)} - \beta y y^T \tag{C.9}$$

Where,

$$y = Z_i - Z_j$$

$$\beta = \frac{1}{\left(z_b + Z_{ii} + Z_{jj} - 2Z_{ij}\right)} \tag{C.10}$$

Appendix. E Sequence Connection Diagram

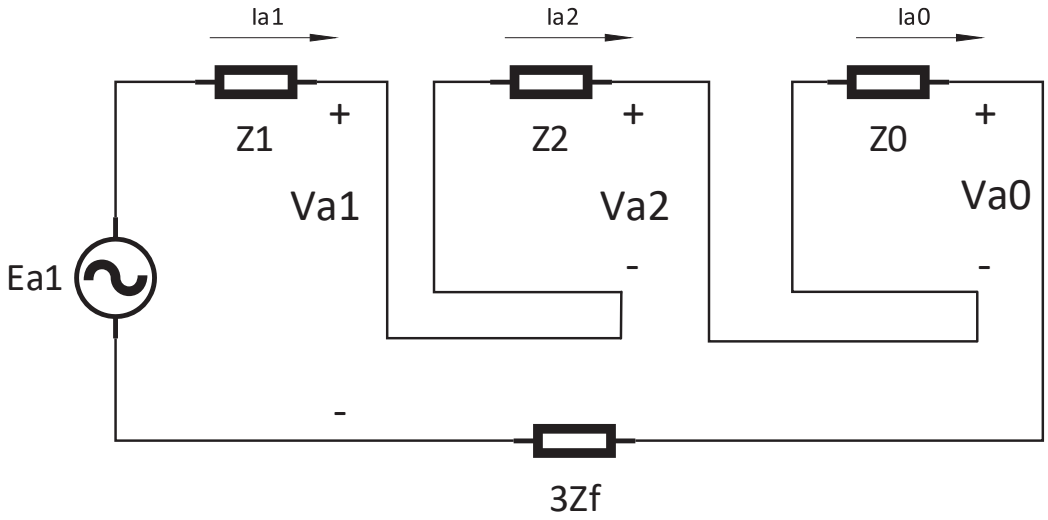

Figure E.1 Sequence network connection diagram for single-phase-to-ground fault

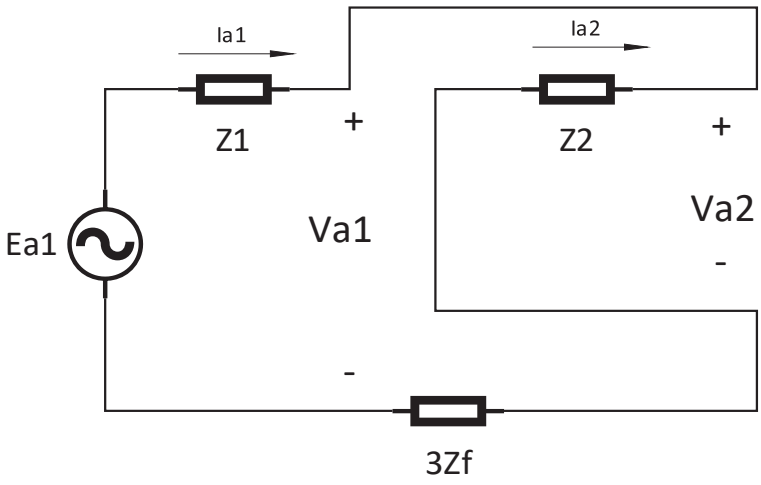

Figure E.2 Sequence network diagram for line-to-line fault

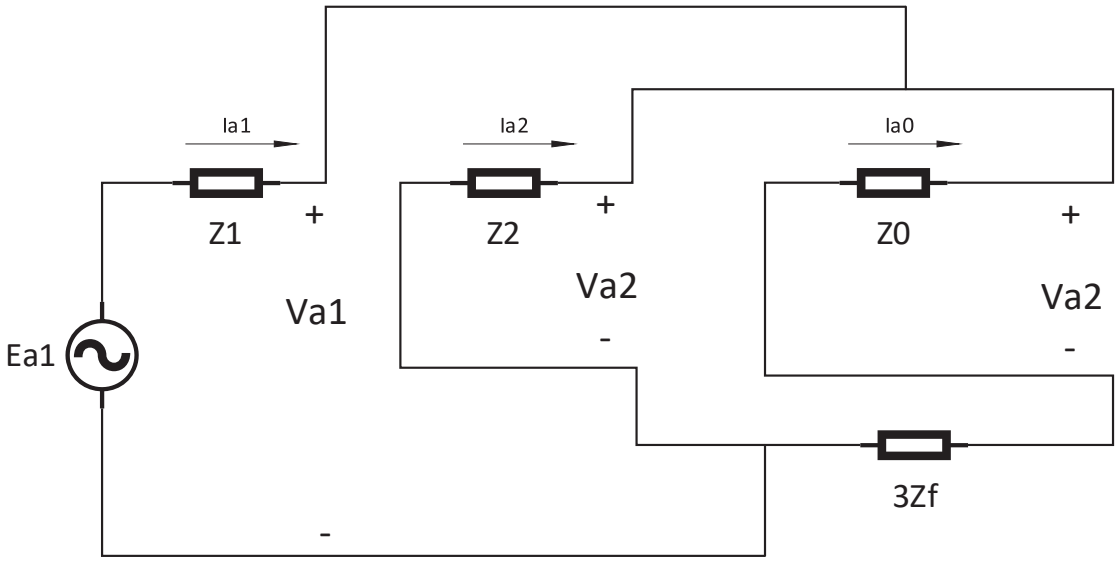

Figure E.3 Sequence network diagram for line-to-line-to-ground fault

References

[1] British Petroleum PLC, “Statistical Review of World Energy 2021,” British Petrolium PLC, London, United Kingdom, 2021. Accessed on: July, 2021. [Online]. Available: https://www.bp.com/content/dam/bp/business-sites/en/global/corporate/pdfs/energy-economics/statistical-review/bp-stats-review-2021-full-report.pdf.

[2] M. Behnke et al., “Development and validation of WECC variable speed wind turbine dynamic models for grid integration studies,” AWEA’s 2007 Wind. Conf., pp. 1–5, 2007.

[3] Western Electricity Coordinating Council Modeling and Validation Work Group, “WECC Wind Plant Dynamic Modeling Guidelines,” vol. 2010, no. November 2010, pp. 1–42, 2014.

[4] Ö. Göksu, R. Teodorescu, P. Rodriguez, and L. Helle, “A Review of the State of the Art in Control of Variable-Speed Wind Turbines,” *9 th Int. Work. Large-Scale Integr. Wind Power into Power Syst. as well as Transm. Networks Offshore Wind Power Plants.*, 2010.

[5] T. Kauffmann, U. Karaagac, I. Kocar, S. Jensen, J. Mahseredjian and E. Farantatos, "An Accurate Type III Wind Turbine Generator Short Circuit Model for Protection Applications," in IEEE Transactions on Power Delivery, vol. 32, no. 6, pp. 2370-2379, Dec. 2017, doi: 10.1109/TPWRD.2016.2614620.

[6] Ö. Göksu, R. Teodorescu, B. Bak-Jensen, F. Iov and P. C. Kjær, "An iterative approach for symmetrical and asymmetrical Short-circuit calculations with converter-based connected renewable energy sources. Application to wind power," *2012 IEEE Power and Energy Society General Meeting*, 2012, pp. 1-8, doi: 10.1109/PESGM.2012.6344906..

[7] I. Erlich, T. Neumann, F. Shewarega, P. Schegner and J. Meyer, "Wind turbine negative sequence current control and its effect on power system protection," *2013 IEEE Power & Energy Society General Meeting*, 2013, pp. 1-5, doi: 10.1109/PESMG.2013.6672880.

[8] R. A. Walling, E. Gursoy and B. English, "Current contributions from Type 3 and Type 4 wind turbine generators during faults," *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-6, doi: 10.1109/PES.2011.6039740.

[9] Manitoba Hydro, “Transmission System Interconnection Requirements,” Manitoba Hydro, MB, Canada,2016. Accessed on: July, 2016.

[10] M. Brucoli, T. C. Green and J. D. F. McDonald, "Modelling and Analysis of Fault Behaviour of Inverter Microgrids to Aid Future Fault Detection," *2007 IEEE International Conference on System of Systems Engineering*, 2007, pp. 1-6, doi: 10.1109/SYSOSE.2007.4304253.

[11] "IEEE Recommended Practice for Conducting Short-Circuit Studies and Analysis of Industrial and Commercial Power Systems," in IEEE Std 3002.3-2018 , vol., no., pp.1-184, 29 March 2019, doi: 10.1109/IEEESTD.2019.8672198.

[12] *BS EN 60909-0:2016 short circuit currents in three-phase a.c. systems, part 0: Calculation of currents (IEC 60909-0:2016)*, vol. BS EN 6090. 2016.

[13] T. Kauffmann et al., "Short-Circuit Model for Type-IV Wind Turbine Generators With Decoupled Sequence Control," in IEEE Transactions on Power Delivery, vol. 34, no. 5, pp. 1998-2007, Oct. 2019, doi: 10.1109/TPWRD.2019.2908686.

[14] Power System Relaying and Control Committee Report of Working Group C-24 of the System Protection Subcommittee, "Modification of Commercial Fault Calculation Programs for Wind Turbine Generators," 2020.

[15] R. M. Furlaneto, I. Kocar, A. Grilo-Pavani, U. Karaagac, A. Haddadi, and E. Farantatos, "Short circuit network equivalents of systems with inverter-based resources," *Electr. Power Syst. Res.*, vol. 199, 2021.

[16] F. Iov, M. Valentini, V.Akhmatov, J.Thisted, "Fault Current Contribution from VSC-based Wind Turbines to the Grid," in Proceedings of the Second International Symposium on Electrical and Electronics Engineering, ISEEE08, Galati, Romania, June, 2008.

[17] D. P. Kothari and I. J. Nagrath, *Modern Power System Analysis*, 3rd ed. New Delhi: McGrow-Hill Companies, 2003.

[18] IEEE PES Joint Working Group, "Fault Current Contributions from Wind Plants," 2013.

[19] D. C. Aliprantis and W. Lafayette, "Fundamentals of Wind Energy Conversion for Electrical Engineers," West Lafayette, 2014.

[20] E. Muljadi, N. Samaan, V. Gevorgian, J. Li and S. Pasupulati, "Different Factors Affecting Short Circuit Behavior of a Wind Power Plant," 2010 IEEE Industry Applications Society Annual Meeting, 2010, pp. 1-9, doi: 10.1109/IAS.2010.5616819.

[21] M. Singh and S. Santoso, "Dynamic models for wind turbines and wind power plants," National Renewable Energy Laboratory, Colorado, USA, Oct., 2012.

[22] E. Muljadi and V. Gevorgian, "Short-circuit modeling of a wind power plant," *IEEE Power Energy Soc. Gen. Meet.*, no. March, 2011.

[23] R. A. Walling, E. Gursoy and B. English, "Current contributions from Type 3 and Type 4 wind turbine generators during faults," 2011 IEEE Power and Energy Society General Meeting, 2011, pp. 1-6, doi: 10.1109/PES.2011.6039740.

[24] S. Chandrasekar, "Short Circuit Modeling of Wind Turbine Generators," M.Sc. Thesis, Department of Electrical and Computer Engineering University of Sasketchewan, Canada, 2013.

[25] Eon Netz GmbH, “Grid Code High and Extra High Voltage,” 2006. [Online]. Available: http://www.pvupscale.org/IMG/pdf/D4_2_DE_annex_A3_EON_HV_grid__connection_requirements_ENENARHS2006de.pdf.

[26] B. Chen, A. Shrestha, F. A. Ituzaro and N. Fischer, "Addressing protection challenges associated with Type 3 and Type 4 wind turbine generators," 2015 68th Annual Conference for Protective Relay Engineers, 2015, pp. 335-344, doi: 10.1109/CPRE.2015.7102177.

[27] R. M. Furlaneto, I. Kocar, A. Grilo-Pavani, U. Karaagac, A. Haddadi, and E. Farantatos, “Short circuit network equivalents of systems with inverter-based resources,” *Electr. Power Syst. Res.*, vol. 199, no. April, p. 107314, 2021.

[28] T. Kauffmann et al., "Phasor domain modeling of Type III wind turbine generator for protection studies," 2015 IEEE Power & Energy Society General Meeting, 2015, pp. 1-5, doi: 10.1109/PESGM.2015.7286606.

[29] T. Kauffmann, “Modeling of wind parks for steady state short circuit studies,” Doctor of Philosophy thesis, Department of Electrical Engineering, Polytechnique MontrealUniversity of Montreal, Canada, 2018.

[30] U. Karaagac et al., "Phasor domain modeling of type-IV wind turbine generator for protection studies," 2015 IEEE Power & Energy Society General Meeting, 2015, pp. 1-5, doi: 10.1109/PESGM.2015.7286537.

[31] Siemens Industry Inc., “Inverter-Based Generator Models with Controlled Power and Current,” 2020.

[32] ASPEN, “Technical Bulletin on Modeling Type-4 Wind Plant and Solar Plants,” 2018.

[33] S. Chan, “Simulation of wind and solar plant models in ASPEN OneLiner,”, 2021.

[34] R. A. Walling and M. L. Reichard, “Short circuit behavior of wind turbine generators,” *2009 62nd Annu. Conf. Prot. Relay Eng.*, pp. 492–502, 2009.

[35] V. Brandwajin and W. F. Tinney, “Generalized method of fault analysis,” *IEEE Trans. Power Appar. Syst.*, vol. PAS-104, no. 6, pp. 1301–1306, 1985.

[36] A. Haddadi, I. Kocar, J. Mahseredjian, U. Karaagac, and E. Farantatos, “Negative Sequence Quantities-Based Protection Under Inverter-Based Resources - Challenges and Impact of the German Grid Code,” *IEEE Power Energy Soc. Gen. Meet.*, vol. 2020-Augus, no. June, 2020.

[37] SIEMENS, “PSS®E – transmission planning and analysis | PSS® power system simulation and modeling software | Siemens Global.” [Online]. Available: https://new.siemens.com/global/en/products/energy/energy-automation-and-smart-grid/pss-software/pss-e.html. [Accessed: 30-Dec-2021].

[38] Siemens Industry Inc., “Program Operation Manual - PSS®E 35.0.0,” no. September, 2019.

[39] Powertech, “DSATools.” [Online]. Available: https://www.dsatools.com/. [Accessed: 30-Dec-2021].

[40] GE Energy Colsulting, “PSLF | Transmission Planning Software | GE Energy Consulting.” [Online]. Available: https://www.geenergyconsulting.com/practice-area/software-products/pslf. [Accessed: 30-Dec-2021].

[41] Manitoba Hydro International Ltd., “PSCAD.” [Online]. Available: https://www.pscad.com/. [Accessed: 10-Jan-2022].

[42] “EMTP® User Manual | EMTP®.” [Online]. Available: https://www.emtp.com/documentation/emtp-user-manual. [Accessed: 10-Jan-2022].

[43] “ATPDraw Home.” [Online]. Available: https://www.atpdraw.net/. [Accessed: 10-Jan-2022].

[44] H. Shi, Y. Guo, W. Zhang, and J. Pan, “The study of the harmonic impedance measurement,” *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 490, no. 7, 2019.

[45] Xiao Jiang and A. M. Gole, "A frequency scanning method for the identification of harmonic instabilities in HVDC systems," in IEEE Transactions on Power Delivery, vol. 10, no. 4, pp. 1875-1881, Oct. 1995, doi: 10.1109/61.473368.

[46] Manitoba HVDC Research Centre, “PSCAD User’s Guide,” *Winnipeg*, 2018.

[47] Manitoba Hydro International, “Type-4 Wind Turbine Model (v4.5),” 2018.

[48] H. Saadat, *Power System Analysis*, 3rd ed. PSA publishing, 2011.

[49] A. R. Bergen and V. Vittal, *Power Systems Analysis*, Second. New Jersey: Prentice Hall, 2007.