Dynamic Modelling and Simulation of a Multiport DC Hub with Closed-Loop Control

by

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Abstract

This thesis firstly studies a dc hub and proposes a control method for its multiport operation. The proposed control method is tested on a three-port dc hub in PSCAD/EMTDC and its stability and response to a transient are demonstrated. In addition, this thesis introduces a dynamic average-value model for a multiport dc interconnection hub based upon the concept of generalized averaging (i.e., dynamic phasors). The developed model is able to predict the transient and steady state response of a dc hub and its closed loop control system with comparable accuracy to and markedly higher computational efficiency than a conventional EMT model. Simulation results are presented for a three-port dc hub and are compared with detailed EMT simulation results from PSCAD/EMTDC. Simulation efficiency is significantly improved by applying the proposed average-value model.

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Dedications

To my journey in Winnipeg

To my families

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List of Symbols

ω	Angular frequency
R	Resistor
L	Inductor
C	Capacitor
T	Period (of a periodic signal)
f	Frequency
θ	Power factor angle
j	$\sqrt{-1}$
M_i	Modulation index for port i
I_i	Current of port i
V_i	Voltage of port i
X_d	d component of the vector X
X_q	q component of the vector X

List of Abbreviations

ac	Alternating current
dc	Direct current
HVDC	High voltage direct current transmission
VSC	Voltage sourced converter
LCC	Line-commutated converter
EMT	Electromagnetic transient
RMS	Root-mean square
STATCOM	Static synchronous compensator
MMC	Modular multilevel converter
SM	Submodule
HBSM	Half bridge submodule
FBSM	Full bridge submodule
PWM	Pulse-width modulation
PSS	Periodic steady state
PLL	Phase lock loop
IGBT	Insulated gate bipolar translator
GTO	Gate turn-off thyristor
MOSFET	Metal-oxide-semiconductor field effect transistor

Chapter 1 Introduction

1.1 Background

The demand for electricity is growing rapidly as industrialization and globalization continue to grow. Due to this escalating trend providing secure and reliable energy and reducing the production of greenhouse gases have come to be major issues [1]. Electric power transmission is either in the form of ac or dc. With the increasing demand for generation of clean energy from renewable energy resources (e.g., offshore wind farms and solar farms) research and development on dc power grids, especially with high- or medium-power dc-dc converters, has attracted much attention. Compared to ac transmission over long distances, dc transmission has a number of advantages including no need for reactive compensation, low losses, feasibility to interconnect ac systems with different frequencies and so on. Nowadays, many electric power grids are experiencing hybridization with both dc and ac systems present.

Over the past few decades, dc systems have seen great expansion as dc power can be readily stored and efficiently converted to both ac and dc. AC power transfer is popular since ac voltages can be easily increased or decreased by means of transformers. Before the invention of dc-dc converters, it was challenging to do the same type of transformation with dc voltages directly. Conventional ac power systems have been operating for several decades with little or no significant dc subsystems. DC systems, however, have been gaining increasing appeal due to the proliferation of such technologies as solar power generation and bulk energy storage, both of which are dc in nature. One important requirement for dc grids is the ability to interconnect different levels of dc voltages. It is also necessary to investigate how these primarily dc systems are to be interconnected to existing ac power systems. Meanwhile, there is a need to develop and investigate means for interconnection of large dc subsystems together as they become more prevalent and the concept of dc grids becomes a closer reality.

An important issue to address is how to integrate multiple dc grids (or subsystems) with different voltage levels. In conventional line-commutated HVDC transmissions, power transfers are usually point-to-point and the cost will be extremely high if there are a large amount of dc systems that need to be interconnected. Therefore, it will be economically efficient if multiport dc systems can be interconnected directly through one point or a single device. Several state-of-the-art multiport dc-dc converters for use in high-medium power systems have been proposed and studied in the past [2]-[7]. In [8], a multiport high power LCL dc hub is proposed based upon the idea of an LCL resonant converter [9]. For example, based on the concept from [8], Figure 1-1 shows a multiple dc hub that interconnects multiple dc links including a generation station, a battery storage system, a remote community, and other public environments (such as a national park). The dc hub has a multiport configuration and can be used as the interconnection point of different dc voltages. Each port has the ability of bidirectional power flow and operates independently from the other ports. Power flow may occur among different networks. The power exchange point is an ac bus, which only connects different LCL resonant tanks with a relatively high fundamental frequency so that the size of reactive components can be reduced. In case of a dc fault, the faulted port can be isolated by opening the ac breaker installed after the LCL filter. Another key advantage of this topology is the ability to add new ports to the dc hub without making any component changes to the other ports. Theoretically, the dc hub can have as many ports as needed. These features provide an ideal scenario to for the interconnection of various dc subsystems.

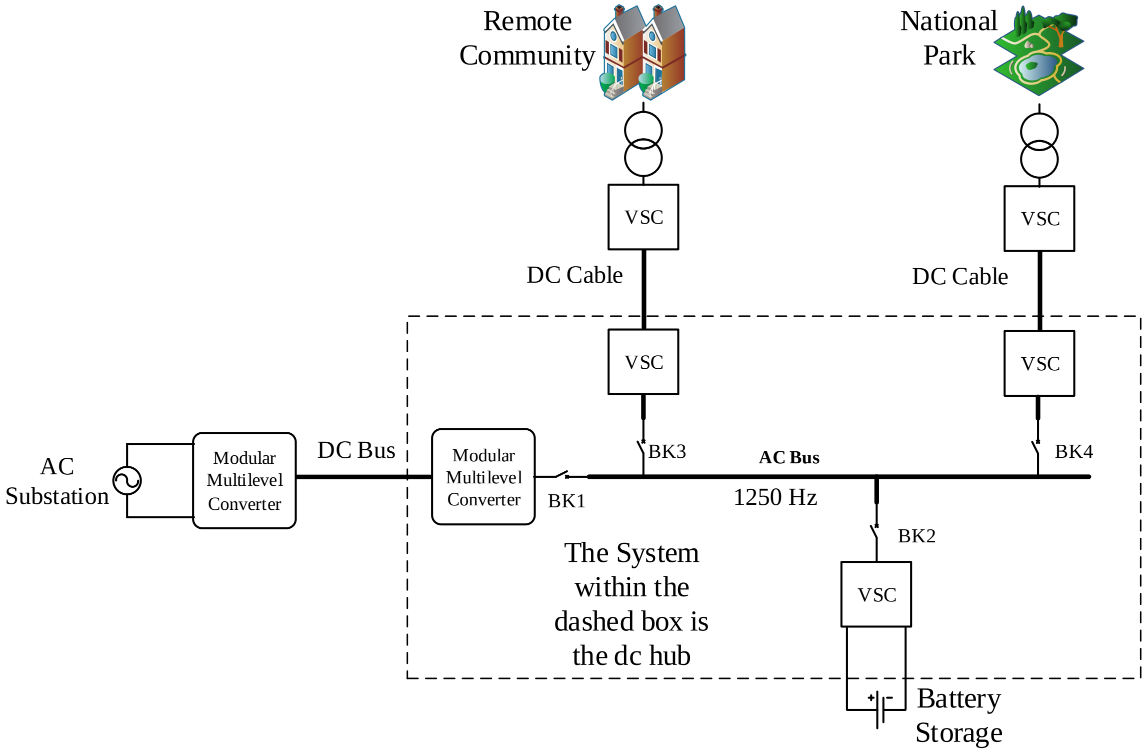

Figure 1-1: DC hub structure overview

In [10], a two-port dc hub has been prototyped with closed loop control to validate the topology from [8]. However, several questions regarding the control of a multiport dc hub remain unanswered. Moreover, [11] states that simulating such a dc hub with a medium-range fundamental frequency (200-2000 Hz) in an electromagnetic transient (EMT) simulation software, such as PSCAD/EMTDC, requires extremely small time-steps to achieve sufficient accuracy due to the numerical instability that may result from the one time-step delay when the EMT solver performs numerical integration of the control systems and the vector angle delay associated with the dq0 transformations. The proposed solutions in [11] for these two problems are to avoid the time-step delay in the numerical integration and to compensate the vector angle delay of the dq0 transformations. By applying the proposed solutions, [11] reports significant improvements in the speed and accuracy of simulating a medium-frequency two-port dc hub.

1.2 Problem Definition

Several questions regarding the control of a multiport dc hub remain unanswered and one is how a multiport dc hub can be controlled effectively. Power transfer among ports must be properly analyzed and suitable control schemes be developed.

A state-space model of a two-port dc hub is proposed in [11] and solved numerically using different numerical integration methods to verify its accuracy and efficiency. However, there is no developed state-space model for a multiport dc hub and no control method has been tested on a multiport dc hub with closed loop control.

According to the above description, there are two main problems that this thesis addresses: control of a multiport dc hub and effective numerical simulation of a dc hub. This research work is, first of all, to develop a universal control scheme to control a dc hub with an arbitrary number of ports. Secondly, a dynamic generalized average-value model is developed to accelerate the speed of simulation.

1.3 Motivation

Based upon the existing literatures related to dc hubs, no control systems of a multiport dc hub is presently available. Therefore, to investigate the performance of a multiport dc hub under closed loop control, it is necessary to extend the control method of a two-port dc hub to a universal method for multiport dc hubs. To build a control system for a dc hub with an arbitrary number of ports is essential to perform further research on control interactions, stability, and dynamic performance of multiport dc hubs.

Besides, a small simulation time-step implies high computation load for simulation software and potentially it means low simulation speed. To develop a new model, which does not require a small time-step to simulate, becomes significant and relevant to studies of dc hubs as such a model can reduce the time for simulating a dc hub when evaluating its dynamic performance. Based upon the developed control system and the dynamic model, the motivation of this thesis is to propose a dynamic model with high simulation efficiency and to validate the model with closed loop control.

1.4 Thesis Organization

This thesis has six chapters; the following provides an overview of the contents of the remaining chapters.

Chapter 2 reviews the commonly used power electronic converters in dc grid applications. This chapter explains the operation and application of both thyristor-based LCC and VSCs including two-level VSCs and MMCs. Chapter 3 introduces the architecture and operating principles of a multiport dc hub. Steady state analysis and harmonic effects of a multiport dc-dc converter are covered. Chapter 4 proposes a control topology for multiport dc hubs based on the existing literature for the control of a two-port dc hub. Chapter 5 provides a dynamic model for a multiport dc hub. This model is simulated with closed loop control and compared to the simulation results obtained from PSCAD/EMTDC. Chapter 6 concludes and summarizes the contributions and conclusions of this thesis. Potential directions for future work are also presented in this chapter.

Chapter 2 Power Electronic Converters in DC Grids

2.1 Line-Commutated Converters

Contemporary LCCs are almost exclusively thyristor-based converters, although other technologies such as mercury-arc valves were prevalent in the past. LCC is a mature and proven technology and has been widely used in HVDC transmission, particularly for bulk power transfer, since the late 1960s [12]. LCCs are popular in HVDC transmission due to their low cost and appealing loss performance compared to other HVDC systems. As shown in Figure 2-1, an LCC-HVDC transmission requires two LCCs, one of which acts as a rectifier that converts power from ac to dc and the other as an inverter that inverts power from dc to ac. The two LCCs are connected through a transmission line with unidirectional flow of dc current due to the presence of unidirectional thyristors. Compared to other HVDC topologies such as VSCs, LCCs have lower costs and better dc fault handling capability, which provide the allowance of using overhead lines for power transmission.

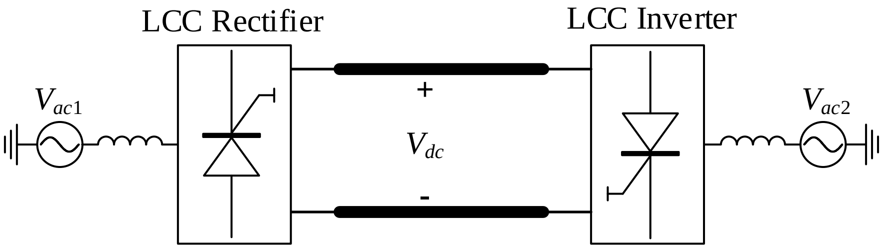

Figure 2-1: Block diagram of an LCC-HVDC transmission system

A thyristor is a semiconductor switch and it is the key element that makes LCCs controllable. The performance of a thyristor is neither similar to uncontrollable switches (e.g., diodes) nor fully controllable switches (e.g., MOSFETs, IGBTs, and GTOs). A thyristor is commonly defined as a type of semi-controllable semiconductor switch. The symbol of a thyristor is shown in Figure 2-2. Unless given a firing pulse when the voltage V across the device is positive the thyristor will be in the "off" state and will block the flow of current. Once a thyristor turns "on" by applying a gate pulse when it is forward biased, it behaves similar to a diode and remain on until either the voltage or current is negative. Therefore, a thyristor can only be controlled to turn it on. The direction of current flowing through a thyristor cannot be reversed.

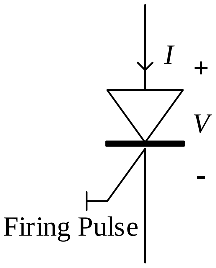

Figure 2-2: Symbol of a thyristor

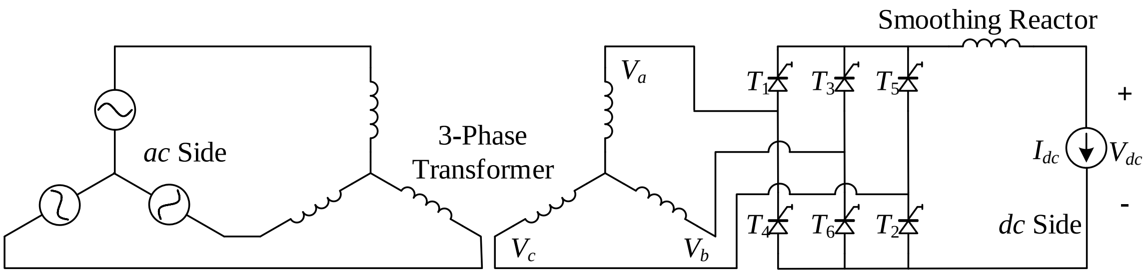

Figure 2-3: Three phase 6-pulse bridge thyristor-based LCC

Figure 2-3 shows the circuit diagram of a grid connected three-phase, 6-pulse thyristor-based LCC acting as a rectifier, which consists of six thyristor valves. The three-phase transformer between the ac side and thyristor valves provides electrical isolation between the ac network and the LCC and it can be considered as an equivalent inductors on each phase. The smoothing reactor at the dc side provides a means to maintain the dc current, which is shown in the form of a current source.

The firing pulse is the only means to control LCCs. By comparing a reference signal V_{ab}, which is the line-to-line voltage between phases a and b, the phase angle at which the firing pulse sent to T_1 is defined as the firing angle α. The firing pules sent to other thyristors can be computed based on the firing angle α by adding certain phase shifts. Due to the source side transformer inductances, the phase currents cannot change instantaneously. This introduces a delay on turning off the corresponding thyristor and causes an overlap angle μ. The extinction angle γ is the phase duration that the thyristor is off. It is worth mentioning that the extinction angle represents the remaining time of the corresponding off switches before turning on again. Thus, commutation failure may occur if γ is not adequately large. The summation of α, μ, and γ is equal to 180 degrees. During the overlap angle, there are four thyristors turned on simultaneously and the voltage (V_p or V_n) at the dc terminal with respect to the ground is equal to half of the sum of the phase voltages being commutated [13].

Figure 2-4 shows the voltage waveforms on the positive terminal and the negative terminal of the dc side, the voltage waveform across the dc side, and the phase current I_a while the LCC is under rectifier operation. The average voltage on the dc side can be expressed as,

$$V_{dc} = V_p - V_n = \frac{3\sqrt{2}}{\pi} V_{LL} \cos\left(\alpha\right) - \frac{3}{\pi} X_s I_{dc} \tag{2.1}$$

where V_{LL} is the line to line voltage and X_s is the source-side impedance. The voltage at the output consists of harmonic orders of multiples of six since the frequency of the voltage ripple is six times the fundamental ac frequency. The phase currents contain harmonics with the orders of 5th, 7th, and 11th, 13th and so on. The impact from harmonics can be eliminated by placing filters on both ac and dc sides. Besides, the dominant harmonics on both ac and dc side can be significantly reduced by stacking two LCCs in series with placing a Y-Y and Y-Δ transformer when connecting to the ac side.

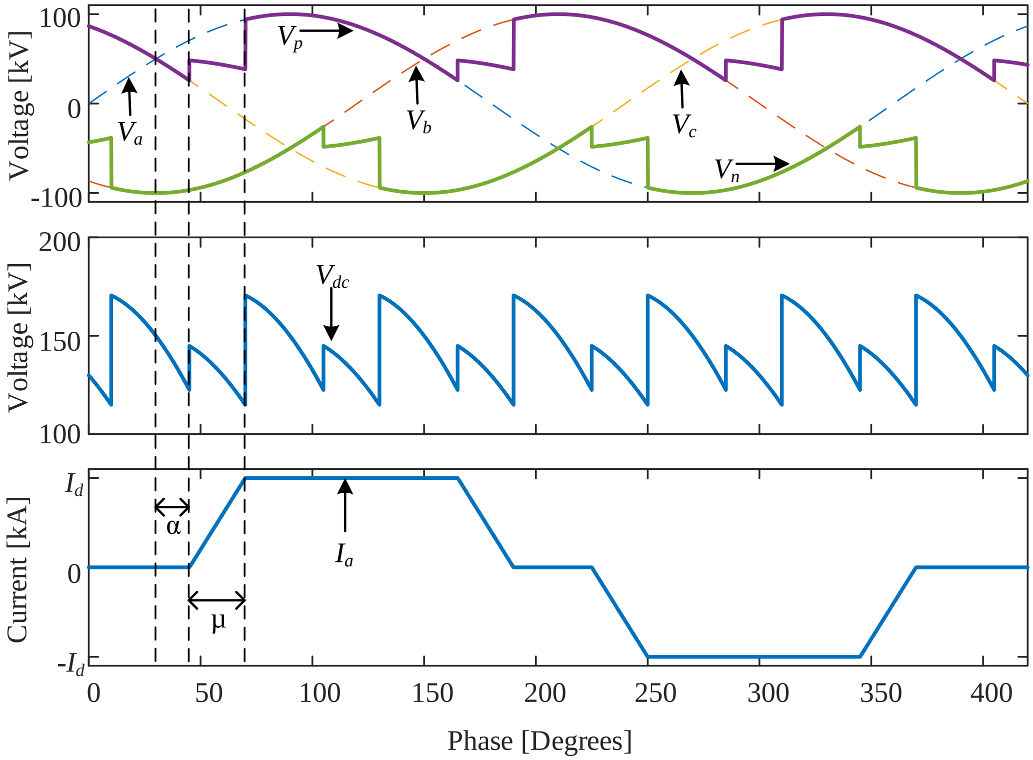

Figure 2-4: Voltages and currents waveforms of a 6-pulse LCC

Normally the LCC-HVDC system are either connected as a monopolar dc transmission system with ground or metallic return or a bipolar system as shown in Figure 2-5. The costs of a monopolar configuration is less than that of a bipolar configuration, whereas bipolar a LCC-HVDC configuration may keep delivering power in case of outage of one of the poles.

Any external dc system connecting to the ac system can be considered as connecting an equivalent impedance along with the ac side. If the equivalent impedance is too large, the LCCs would be under risk to connect to the ac system and the indication of the relative strength of the ac system is called short circuit ratio. Therefore, evaluating the short circuit ratio before connecting an LCC converter to the ac system is important. In common cases, it is safe to connect an LCC if the short circuit ratio is high than 2.5. LCCs may not be able to recover from commutation failure or dc faults if the ac system is weak [15]. Therefore, there is a limitation for interconnection of an LCC to an ac system that the ac system has to be strong enough. Another drawback of an LCC system is that there is no independent real power and reactive power control as thyristors are semi-controllable device.

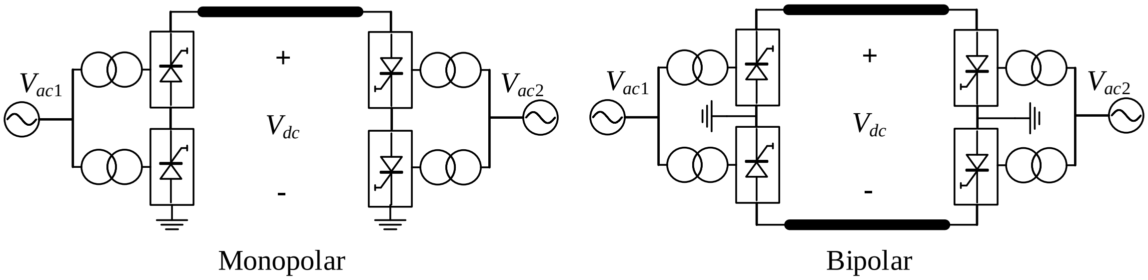

Figure 2-5: Monopolar and bipolar LCC-HVDC configurations [15]

2.2 Voltage Sourced Converters

Lowering the energy losses during transmission and conversion is a major concern in bulk power transmission. New developments in power electronics support sustainability goals by enabling cost-efficient and reliable integration of renewable energy resources into the power system [16]. This is because power electronic devices are highly efficient due to the low losses of semiconductor devices, flexibility in operation, as well as fast dynamic response. Due to these reasons, the use of VSC-HVDC is becoming increasingly popular and significant in HVDC transmission systems.

The semiconductor switches commonly used in VSCs include GTOs, IGBTs, and MOSFETs, which are self-commutating devices [17]. Since these semiconductor switches are fully controllable devices in which both the “on” and “off” states may be controlled, they can provide additional means for control and operation of systems built based upon them. This gives the freedom of controlling active power and reactive power independently. Meanwhile, VSCs can act as STATCOMs to regulate local ac networks and provide reactive power compensations. The direction of power flow between two VSCs can be changed without reversal of the polarity of the dc link voltage. Compared to LCCs, VSCs can be connected to weak ac systems. Due to their fast switching feature, harmonic filtering is often much easier than LCCs.

There are many existing VSC topologies such as diode-clamped converters, floating capacitor converters, and multilevel converters including monolithic and modular. The most common VSCs, including two-level VSC and MMCs, will be reviewed in this chapter.

2.2.1 Two-Level Voltage Sourced Converters

The structure of a two-level VSC is similar to the three phase 6-pulse bridge thyristor-based LCC. However, the switches used in two-level VSCs are fully controllable semiconductor switches, which can be controlled to turn on and turn off, such as IGBTs, MOSFETs, and GTOs. Thus, VSCs have one more degree freedom to be controlled compared to LCCs, so that both real power and reactive power of VSCs can be independent controlled. Each switch of the two-level VSC has a diode that is connected anti-parallel to the switch. This is to provide a path for current during the negative cycle. A circuit of a three-phase two-level VSC is shown in Figure 2-6.

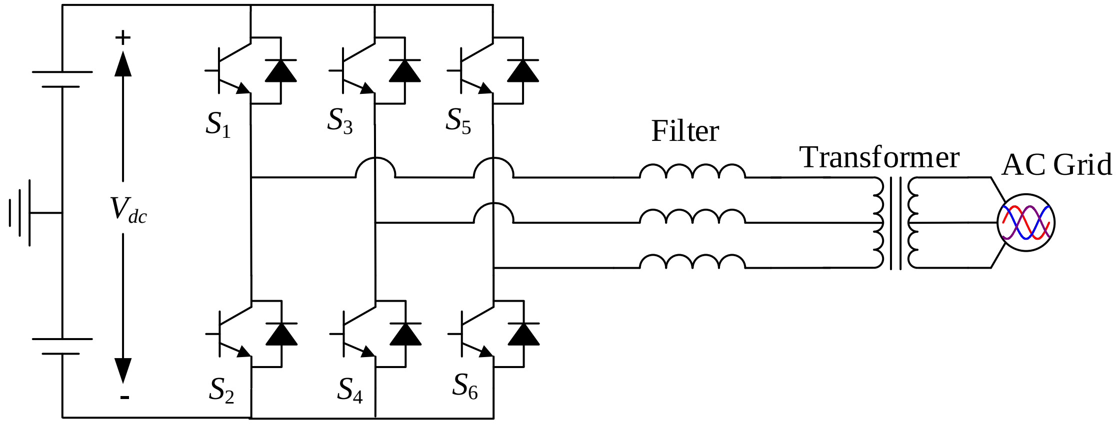

Figure 2-6: Grid connected three-phase two-level VSC

There are a few switching schemes, including space-vector modulation (SVM), optimal PWM (OPWM), and bipolar and unipolar PWM that have been widely used to give switching pulses to two-level VSCs. Bipolar sinusoidal PWM (SPWM) scheme is reviewed in the following. Figure 2-7 shows how the switching pulses to a two-level VSC are generated. The reference signal is given as

$$v_{ref} = m \sin\left(\omega t + \theta\right) \tag{2.2}$$

where m is the modulation index, ω is the angular frequency, and θ is the phase shift of the reference signal. The modulation index is to control the magnitude of the output voltage and must be less than unity in the linear operation range. In the linear operating range the fundamental component of the phase voltage can be expressed as

$$v_p = m \frac{V_{dc}}{2} \sin(\omega t + \theta) \tag{2.3}$$

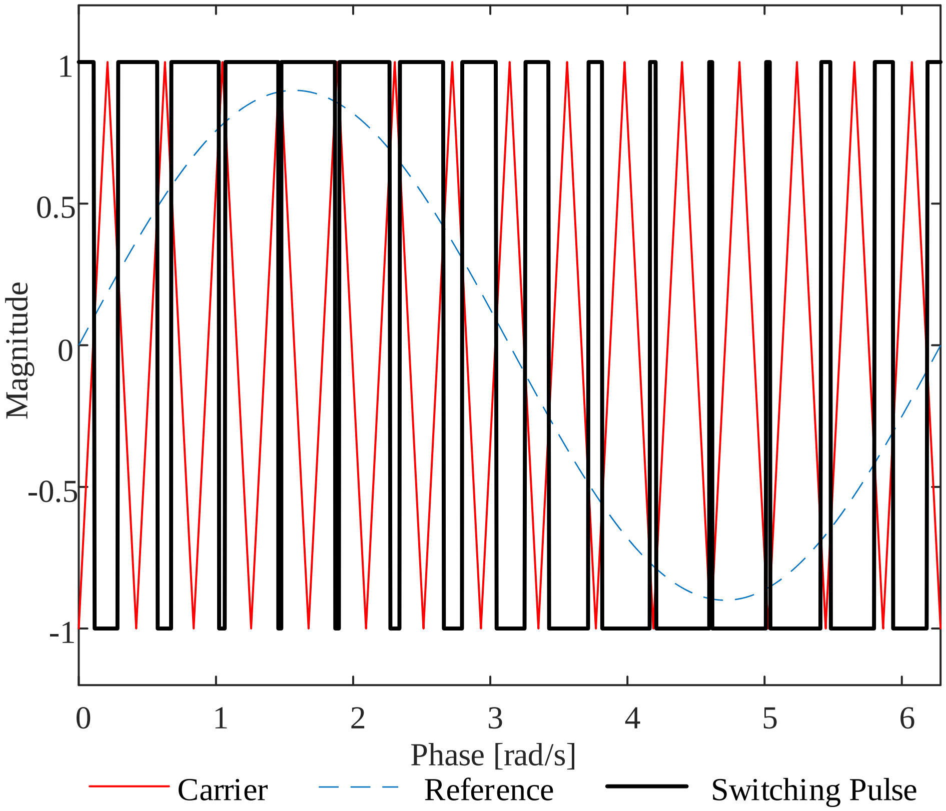

Figure 2-7: Bipolar SPWM for a single phase two-level VSC

The triangular waveform with a duty cycle of 0.5 shown in Figure 2-7 is the carrier. To generate the switching pulses to drive the switch gates, the reference signal is compared to the carrier. If the reference is higher than the carrier, the corresponding switch will be turned on. Selection of the switching frequency of a VSC depends on the application, harmonic requirements, consideration of losses, sizing, limitations of the switching devices, and so on. A high switching frequency normally yields better harmonic performance and better power quality; meanwhile it can also reduce the size of the converter's energy storage elements. However, a high switching frequency implies high switching losses and requires use of fast switching device. The switching frequency can be defined as,

$$f_s = m_f f_1 \tag{2.4}$$

where m_f is the frequency modulation index and f_1 is fundamental frequency of the switching pulse or the frequency of the reference signal. Normally the switching frequency should be higher than 15 times the fundamental frequency. To eliminate the 3rd order harmonic and its multiples in a three-phase VSC, the frequency modulation index m_f is selected to be a multiple of three.

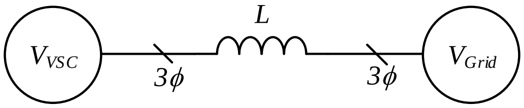

Figure 2-8: Grid connected VSC equivalent circuit

Before connecting to the grid, there are filters and a transformer that are connected in between. The inductive filter reduces the impact from voltage harmonics on the grid and the transformer provides electrical isolation and steps up/down the voltage between the VSC and the grid. The transformer can also be considered as a series phase inductor. Therefore, the circuit is equivalent to Figure 2-8.

2.2.2 Modular Multilevel Converters

In the past two decades, the booming of development of modular multilevel converters has made them attractive in both industrial applications and academic research. MMCs were firstly proposed by R. Marquardt and A. Lesnicar in Germany [18] and the first MMC-HVDC plant was built by Siemens in the United States. Compared with conventional power electronic converters in high- or medium-power applications, the advantages of MMCs include the capability of delivering very high power with exceptional harmonic performance with relatively low switching frequency, modularity, low losses, and reliability due to the use of redundant SMs.

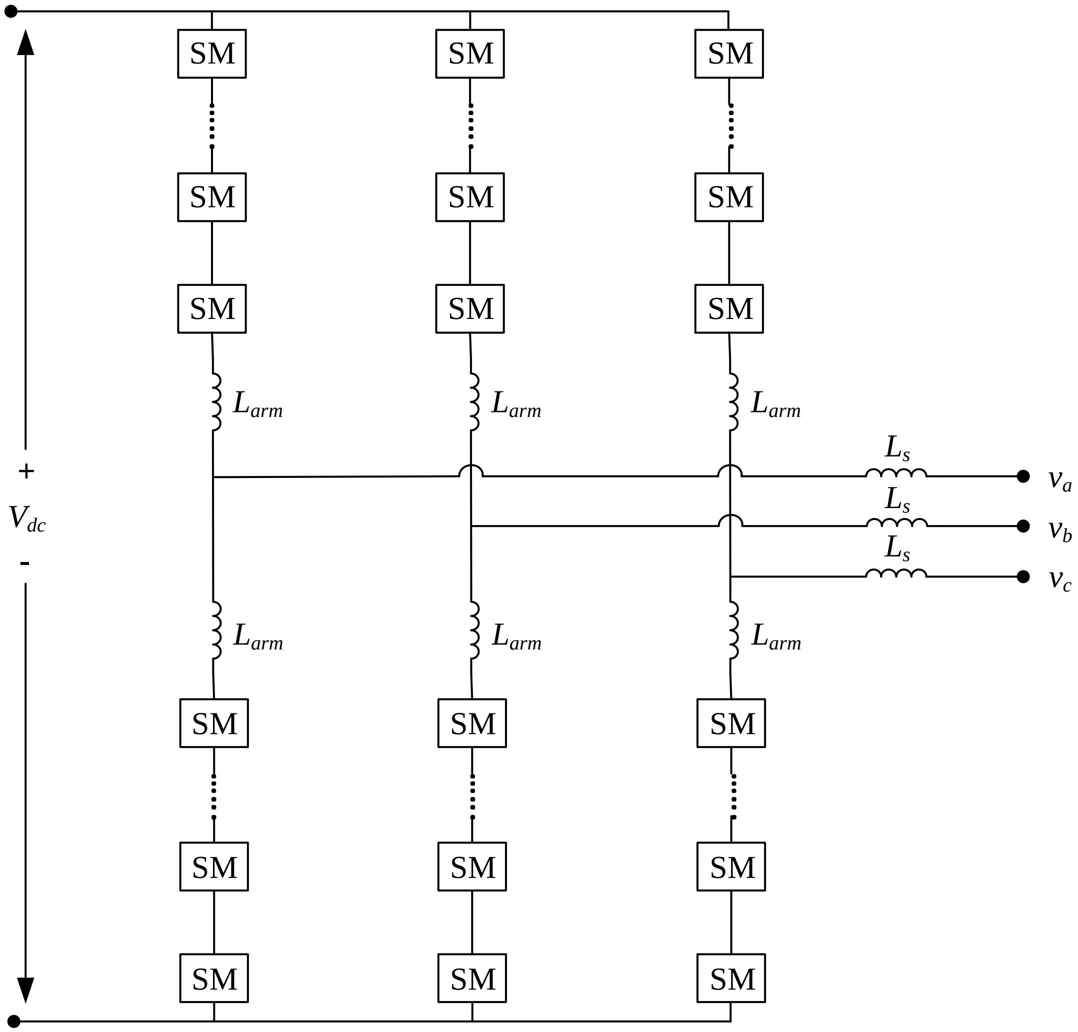

Figure 2-9: Three-phase MMC structure overview

As a type of voltage sourced converters, MMCs are widely used in HVDC or FACTS applications. Figure 2-9 shows an overview of the structure of a typical three-phase MMC. It contains two arms in each phase and each arm includes multiple SMs. Arm SMs may have the same or different configurations depending on the application. In addition, the large number of series connected SMs provides more voltage levels in generating a high-quality sinusoidal output waveform. Consequently, the larger the number of SMs the smoother the output waveform. However, the increasing number of SMs brings problems and more complexity to the control of the MMC.

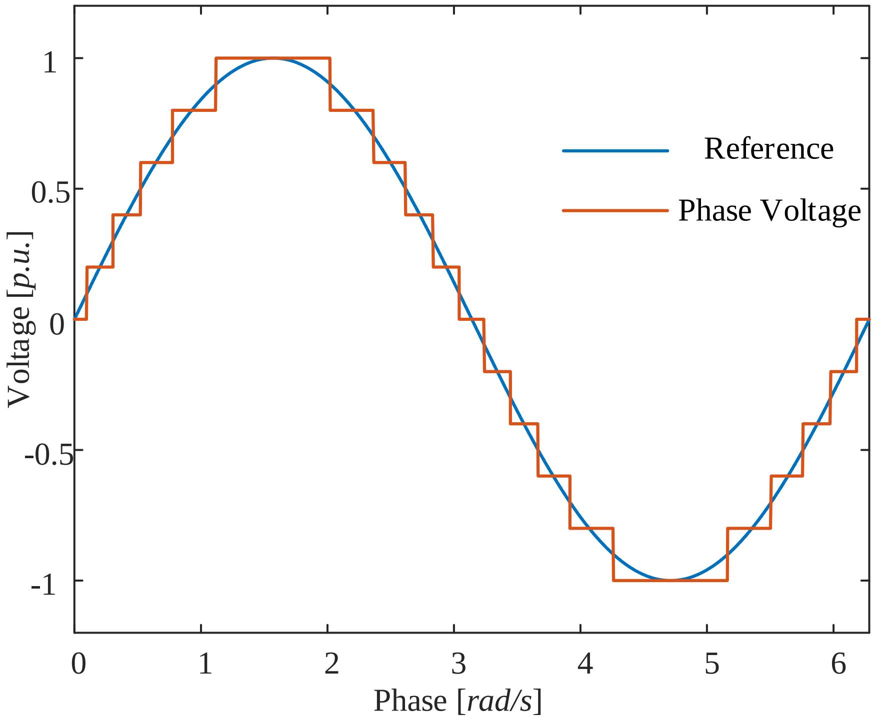

Figure 2-10: Phase voltage of a MMC *vs*. the reference

The power converted by an MMC has good quality due to its excellent harmonic performance. As shown in Figure 2-10, the output waveform of an MMC closely follows a sinusoidal waveform and, therefore, there is no need to place large and expensive filters at the output to filter out high order harmonics. The phase voltage can be calculated as,

$$v_{phase} = \frac{V_{lower} - V_{upper}}{2} \tag{2.5}$$

where V_{lower} and V_{upper} are the voltage across the lower arm and upper arm, respectively. The property of modularity allows decreasing the installation cost and the low switching frequency feature lowers the switching losses of the MMCs during its operation. Meanwhile, the modular structure allows the high dc voltage to be distributed among the large number of SMs.

One of the critical challenges for MMCs is the capability to handle dc faults, such as lightning strikes, short circuits on the cables, and so on. Some MMCs topologies have such an ability to deal with a dc fault without a circuit breaker and some do not.

The design of SMs is usually dependent on the expectation from the MMCs. Different SMs have different advantages or drawbacks. In most cases, consideration for designing a SM include losses (both conduction and switching losses), level of modularity at the cell level, voltage scalability, PQ controlling, capacitor sizing, energy storage, capacitor voltage balancing, circulating current control, unipolar or bipolar voltage operation of the arm, and dc fault handling capability. Generally, there are two common SM topologies that are popular in many MMCs; these are the half-bridge (HB) SM and the full-bridge (FB) SM as shown in Figure 2-11. The following paragraphs introduce the general behavior and characteristics of these two SM topologies.

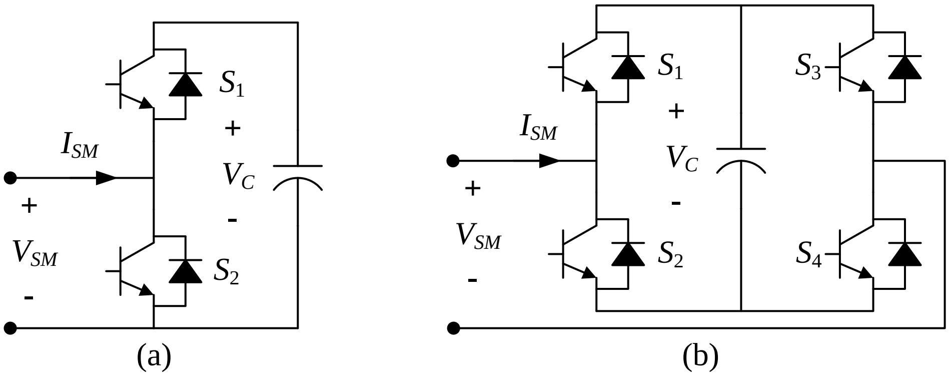

Figure 2-11: Typical MMC SMs (a) HBSM; (b) FBSM

Figure 2-11 (a) shows the circuit of a half bridge SM. There are two semiconductor switches with anti-parallel diodes connected on the terminals of the semiconductor switches to provide a path for the negative current and a capacitor to hold the voltage of the SM. The operation mode of the half bridge SM can be summarized as in Table 2-1.

Table 2-1: Operation Modes of HBSM

S_1	S_2	V_{SM}
ON	OFF	V_C
OFF	ON	0

Under normal operation, the two semiconductor switches are always on or off with complementary states. The output voltage of this SM is equal to either the capacitor voltage, V_C, or 0; therefore, the switching of this SM is unipolar since it cannot have a negative output voltage. The advantages of using half bridge SMs to build an MMC include low material costs and low energy losses since there are only two switches in this SM. However, the drawback of HBSM topology is that there is no dc fault handling capability. When a dc fault occurs, the half-bridge MMC cannot block the fault current although all HBSMs are blocked, since the capacitor may be bypassed and the de-energization process on the arm inductor is very slow. Consequently, usually a circuit breaker is placed in the MMC circuit if half bridge SMs are the only used topologies for all the SMs [19].

Table 2-2: Operation Modes of FBSM

S_1	S_2	S_3	S_4	V_{SM}
ON	OFF	OFF	ON	V_C
OFF	ON	ON	OFF	$-V_C$
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0

To handle a dc fault and to have bipolar switching FBSM topologies are proposed and implemented in MMCs. Similar to a HBSM, it also consists of semiconductor switches, anti-parallel diodes, and a capacitor. However, there are two more switches added in this SM circuit as shown in Figure 2-11 (b). The operation of the FBSM can be concluded as shown in Table 2-2.

Compared to HBSMs, FBSM design can have three different voltage levels of $\pm V_C$ and 0 at the output, which means that the switching of FBSMs is bipolar. One of the advantages of FBSMs is the capability to handle dc faults. When a dc fault occurs, all SMs are blocked. The capacitor in the FBSM is inserted into the fault path regardless of the current polarity. The equivalent voltage and current in the fault loop always have negative reference direction. Therefore, the fault current will decay until it reaches zero. However, the disadvantage of this SM is in its efficiency. As mentioned previously, more semiconductor devices added cause an increase in both conduction losses and switching losses, as well as the material costs.

In recent research, there are new topologies developed based on the modifications on the HBSM and FBSM. For example, clamp-single SM, clamp-double SM, improved hybrid SM, series-connected double SM, three-level cross-connected and so on [20]. These topologies of SMs are proposed to improve the fault handling capability of MMCs. When a dc fault is temporary, the MMCs should be able to protect the circuit components and afterward restart the operation of the system once the fault been cleared. Whereas, if the fault is permanent, the MMCs should at least have self-protecting ability to ensure the components can survive.

The control algorithm for finding the output voltage level that the MMC should deliver has two types: nearest level control and multicarrier PWM. Based upon the reference signal, the controller computes the number of SMs needs to be inserted in each arms. The selection of which SMs should be inserted is based on the current direction and voltages of each SM. Unlike two-level converters, due to multiple semiconductor switches involved in each arm, sorting the operation order of the switches of every arm is introduced. The principle of SMs selection is to ensure that all SMs have a nearly balanced dc voltage. It is to ensure all the switches can be used in such uniform rate and further to protect the devices. Above these procedures, the gate signal will be sent to the MMC. Besides, since there is a large number of energy storage elements in MMC circuits, pre-charging these elements may become necessary. Similar to most power electronic devices, capacitors or inductors operate in periodic steady state (PSS) under normal operation. Therefore, the energy stored in these elements should be controlled and this includes the total energy control to control the energy stored in the SM capacitors of each phase and the difference energy control to balance the energy of the upper and lower arms in the same phase. Similar to two-level converters, the dc voltage needs to be controlled and maintained at the reference value, although the dc-link capacitor is not necessary to be in place for MMCs.

2.3 Application in DC Grids

In present power networks, ac and dc systems are intertwined. The development of technologies related to renewable energies are tied with the research on dc grids. The main consideration in dc grids include cost, efficiency, bi-directional power transfer, stability, controls, fault handling capability, and so on.

2.3.1 LCCs in DC Grids

Research on the application of LCCs in dc grids over the past few decades provides many ideas to interconnect multiple dc networks. There are two major ways - parallel connection and serial connection - that have been proposed; these two connection schemes are shown in Figure 2-12. It is necessary to mention that all ac sources shown in the graphs require another stage of conversion to dc voltage, so they can be ready to integrate into a dc grid.

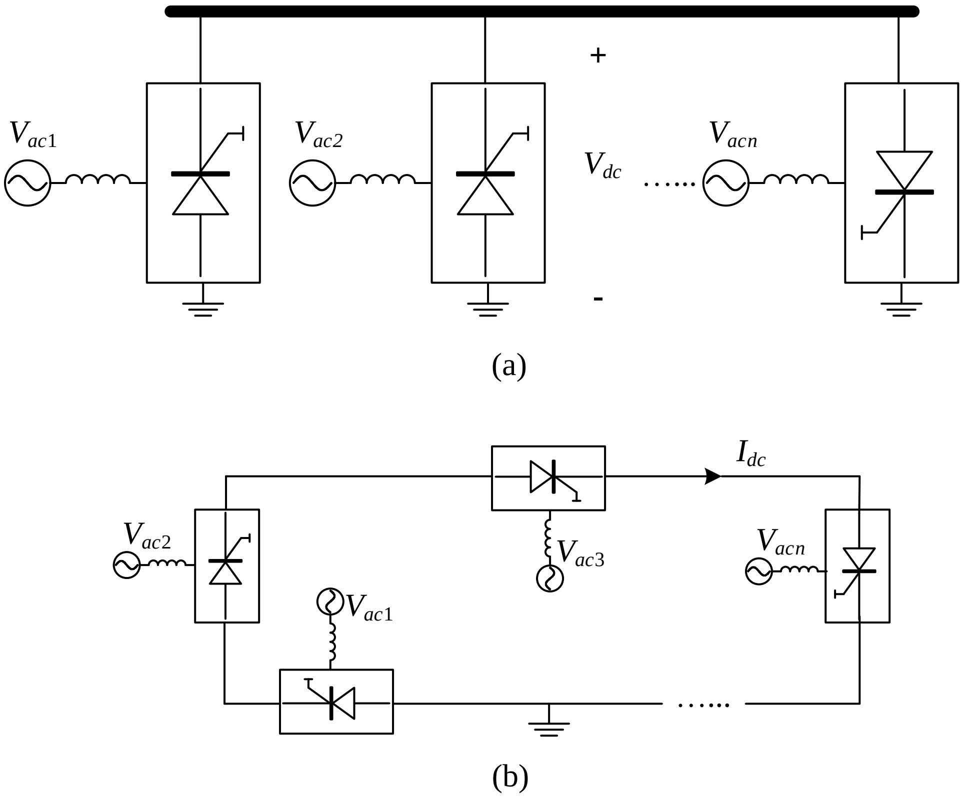

Figure 2-12: (a) Parallel connection; (b) Serial connection [15]

For parallel connection of LCC-HVDC systems, the dc voltages at the dc terminals of all LCCs are uniform and the polarity of the dc link voltage and the direction of current flow cannot be changed unless employing mechanical changes. There is a master LCC to be in charge of regulating the dc voltage and all other LCCs take control of their own dc currents flowing to the network. Therefore, any dc fault, which is possible to happen when commutation failure occurs on any of the LCCs, can result in a global power interruption.

Unlike the parallel connection, serial connection requires uniform current circulating in the LCCs' loop. The dc current in the LCC's loop brings large losses since the current is always at the rated value. Similarly, one master LCC must take control of the regulation of dc current and other LCCs need to control their own dc voltage so that the power transfer to each LCC can be controlled. Commutation failures in local LCCs would not interrupt the global power service. Meanwhile, the direction of power transfer can be reversed since the polarity of dc voltages of LCCs in this case can be changed [15].

2.3.2 VSCs in DC Grids

As illustrated in Section 2.2, VSCs have many advantages compared to LCCs. One of which is the flexibility of power flow and control. The following section reviews two state-of-the-art VSC based dc-dc converter topologies in dc grid applications proposed in the past few years. VSC-HVDC technology is also often used for offshore wind farm and bulk power transfer.

A dual active bridge dc-dc converter normally consists of two VSC stages as shown in Figure 2-13. A dc-ac converter is connected back-to-back to another dc-ac converter typically through either a transformer (for both isolation and maintaining a stepping ratio purposes) or a resonant circuit. For this interconnection method, there is no restriction on the topology of VSCs, so the selection of the topologies of VSCs depends on many conditions including financial and technical considerations. The first generation of dual active bridge dc-dc converter topologies operating in high power range was proposed and analyzed in [2]-[3]. The dual active bridge topology is attractive because of its bidirectional power flow, low component stresses, and high-power density features [3]. In [21], the paper analyzes the difference between the dual active bridge dc-dc converter in [2] and the dc-dc converter based on MMCs in [22] from the viewpoints of efficiency, cost, and limitation of use in various dc grid connections.

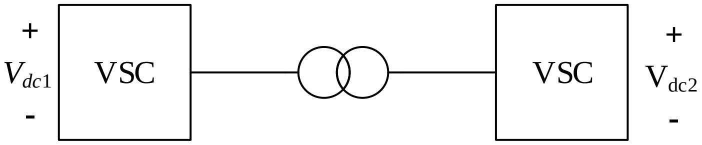

Figure 2-13: Dual active bridge converter

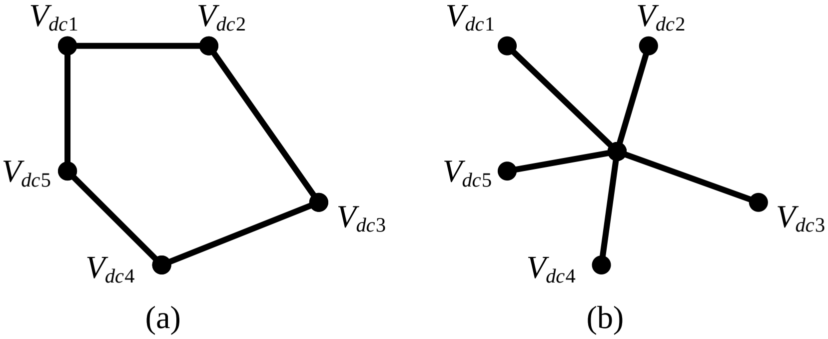

Figure 2-14: Current and future dc grids

The current and future integration of multiple dc networks can be summarized in Figure 2-14. The existing dc networks are connected on a point-to-point basis. Whereas, the future dc grid is formed by interconnecting multiple dc links to a single point or a single device. This method can save cost on both installation of converters and transmission lines. Consequently, developing an efficient and reliable multiport dc-dc converter plays a significant role for the improvement of dc grids. A state-of-the-art VSC based multiport dc-dc converter is investigated and analyzed in the following chapter.

Chapter 3 Architectures and Operations of a Multiport DC Hub

3.1 Topology Review

In the previous chapter, it was mentioned that future dc grids require the interconnection of multiple dc links. In [8], a solution for the interconnections of multiple dc networks is proposed. The idea is to use a dc hub, which is a multiport dc-dc converter, to link different dc networks with different voltage levels and make bidirectional power flow becomes possible. The structure of the multiport dc-dc converter is shown in Figure 3-1.

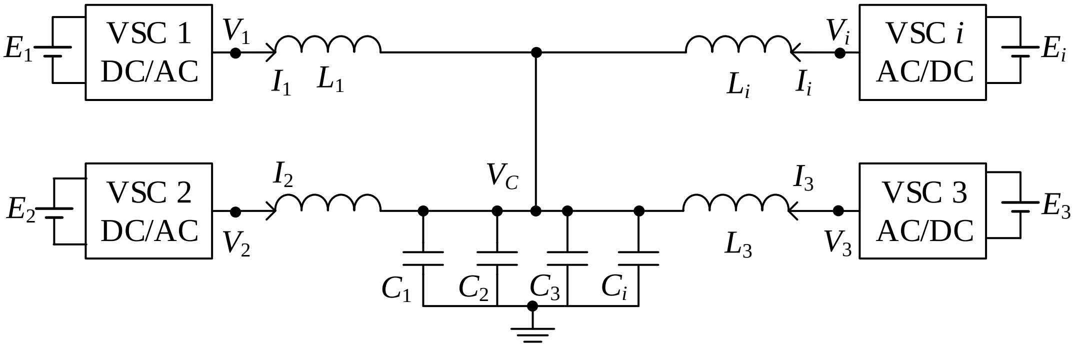

Figure 3-1: DC hub structure [8]

The topologies of VSCs in the dc hub can be arbitrary, such as half-bridge or full-bridge two-level VSCs, MMCs, and so on. Without considering losses and cost of a dc hub, under the existing HVDC converter technologies, MMCs would be the best choice for the VSCs of a dc hub since the harmonic performance of MMCs is much better than other VSC topologies. In the investigations shown in the following chapters, for consideration of creating a more challenging environment of simulation, the VSCs adopted in the dc hub are considered as half-bridge two-level VSCs as the harmonics from two-level VSCs are much more considerable than the harmonics from MMCs, as shown in Figure 3-2. The voltages across the dc terminals are denoted as V_{dci}, where i indicates the port number. In an ideal case, the number of ports of a dc hub can be extended without having influences on other ports. Power control in each dc terminal is arbitrary as long as the summation of network powers in a dc hub is zero.

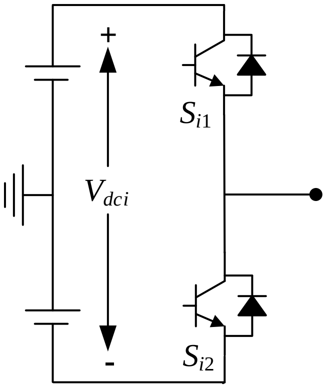

Figure 3-2: Half-bridge two-level VSC

The ac outputs of all VSCs in a dc hub are linked by a specially designed multiport LCL filter and then the energy exchange happens at the node of capacitors, as shown in Figure 3-1. The equivalent capacitor is not an actual ac bus in its conventional form. Instead, it can be considered as a single node that only links the VSCs within the dc hub. In addition, the frequency of the voltage across the capacitors is in the kHz range and is much higher than the conventional 50/60 Hz ac system due to the filtering purposes and considerations on sizing of the reactive components. Better filtering ability may lower the switching frequency of the VSCs so that the switching losses can potentially be reduced. Besides, reducing the size of reactive components of a dc hub can potentially decrease the cost of materials. The design method of LCL filter plays a key role for the power conversion process. The design method has been fully explained in [8] and the inductor and capacitor values can be calculated using the following two equations.

$$L_i = \frac{M_i^r V_i^r \sqrt{\left(V_C^r\right)^2 - \left(M_i^r V_C^r\right)^2}}{P_i^r \omega_0} \tag{3.1}$$

$$C_i = \frac{1}{\omega_0 \left(V_C^r\right)^2} \frac{P_i^r \sqrt{\left(V_C^r\right)^2 - \left(M_i^r V_C^r\right)^2}}{M_i^r V_i^r} \tag{3.2}$$

where *i* denotes the number of the corresponding port, and *r* denotes the rated value. M_i^r is the rated modulation index of port *i*, V_i^r and V_C^r are the rated fundamental components of the ac voltage of port *i* and the ac voltage on the capacitors at the center of the dc hub, respectively. P_i^r is the rated maximum power of each port and ω_0 is the fundamental frequency of the ac voltage across the capacitors at the center of the dc hub, or it may be considered as the operating frequency of the dc hub. To design the LCL filter, first of all, it is necessary to select the rated P_i^r, V_{dci} and ω_0. According to the design principles in [8], V_C^r can be selected around 20% higher than the highest V_i^r due to the considerations on limiting fault currents and avoiding problems with the resonant frequency. Once these factors have been defined, L_i and C_i can be computed accordingly.

3.2 Principles of Operation

The voltage source converters in the dc hub can be of any type including two-level, multi-level, or modular multilevel converters. Using the design principles in [8], the values of LCL filter components are selected based on factors such as the rated power, dc link voltages, number of ports, operating frequency, considerations of resonant frequency, and so on. Since the application of a dc hub is mainly for connecting multiple dc links, the internal harmonics of a dc hub are not a significant concern. Basic operating principles of a dc hub under normal conditions are illustrated in [8] and summarized as follow.

a. The ac voltage and current of each port are in phase; therefore, all ports operate at unity power factor to reduce the currents drawn and losses;
b. The phase of voltage across the parallel capacitors, V_C, is considered as reference angle, so that the imaginary part of V_C is forced to be zero and no PLL is required;
c. With the above, the zero summation of the real part of the port currents is an indication of power balance in a dc hub.

In any circuit, the complex power can be presented as follows.

$$S = VI^* = P + jQ \tag{3.3}$$

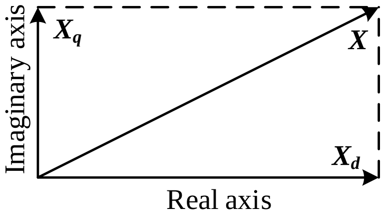

Figure 3-3: Vector in phasor domain

In phasor domain, any vector (denoted as X) as shown in Figure 3-3, can be represented as in (2).

$$X = X_d + jX_q \tag{3.4}$$

The complex power can, therefore, be re-written as follows.

$$S = (V_d + jV_q)(I_d - jI_q)$$
$$S = V_d I_d + V_q I_q + j(V_q I_d - V_d I_q) \tag{3.5}$$

Thus, the port current shown in Figure 3-1 is given in (4).

$$I_i = \frac{V_i - V_C}{j\omega L_i} = \frac{V_{id} + jV_{iq} - V_{Cd} - jV_{Cq}}{j\omega L_i} \tag{3.6}$$

where V_i is the port voltage. As mentioned earlier, V_{Cq} is forced to be zero, which implies that (3.6) can be simplified as follows.

$$I_i = I_{id} + jI_{iq} = \frac{V_{iq}}{\omega L_i} + j\frac{V_{Cd} - V_{id}}{\omega L_i} \tag{3.7}$$

According to (3.5) and with V_{Cd} equal to V_C, the port's real power is

$$P_i = V_{id} I_{id} + V_{iq} I_{iq} = \frac{V_{iq} V_{Cd}}{\omega L_i} = I_{id} V_C \tag{3.8}$$

Based on (3.8), the I_{id} component of the port current controls the real power as V_C is left to be an uncontrolled variable, although the magnitude of V_C may be impacted by the variation of port currenta. In (3.7), it is clear that I_{id} can be controlled by V_{iq} or effectively the q component of the modulation index since port voltages can be expressed as follows.

$$V_i = V_{id} + jV_{iq} = M_{id} E_i + jM_{iq} E_i \tag{3.9}$$

where M_{id} and M_{iq} are the modulation indices for dq components of the port voltages, respectively.

3.3 Steady State Analysis

As indicated in the previous section of topology review, a dc hub consists of multiple VSCs interconnected by a multiport LCL filter. Ideally, the averaged model of a VSC is equivalent to an ac voltage source with a single frequency component (i.e., the fundamental). As an example, the average model of a three-port dc hub can be shown in Figure 3-4.

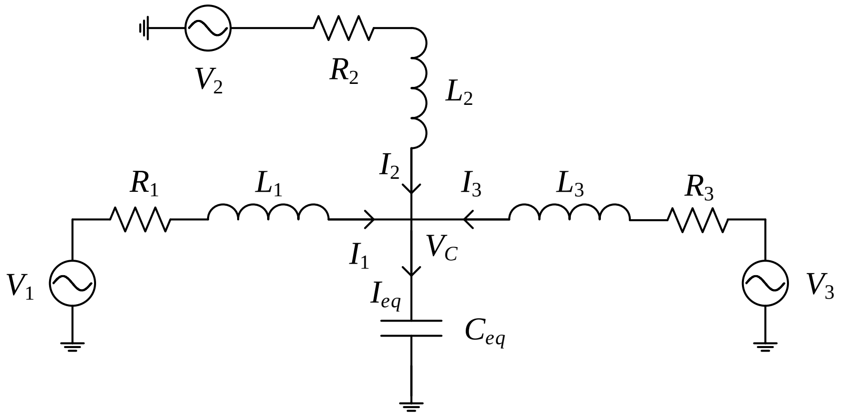

Figure 3-4: Three-port dc hub in the averaged model

Prior to designing the control system for a multiport dc hub, a steady state analysis is performed. This is to validate that there exists a desired operating point, so that it is possible to design a control system for the dc hub and let the dc hub operate at the desired operating point. For a multiport dc hub, the given conditions and parameters are as follows:

a. Power from each port is known;
b. The operating frequency and all the inductor and capacitor values are given;
c. The voltage and current of each port are assumed to be sinusoidal and in phase (unity power factor);
d. V_{Cq} is equal to zero.

By using the three-port case as an example, to solve all voltages and currents in this circuit without over-determining the system of equations, there are five primary unknowns of V_C, I_1, I_2, θ_1 and θ_2, where V_C is the voltage across the capacitor, and I_1 and I_2 are the magnitudes of the currents from port 1 and port 2. All other parameters, such as I_3 with its phase and the capacitor current I_{eq} are the natural outcomes after these primary unknowns are solved. An example of the vector diagram of the currents at each port is shown in Figure 3-5.

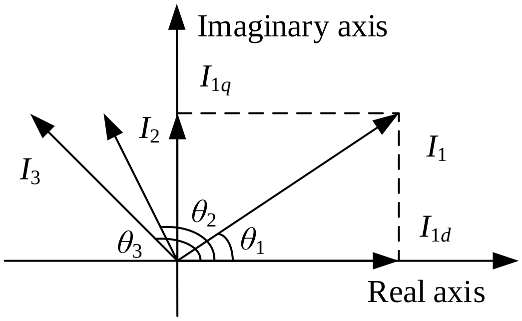

Figure 3-5: Vector diagram of port currents

Based on the power theory, under steady state, the first two equations can be expressed as,

$$P_1 = V_C I_1 \cos(\theta_1) \tag{3.10}$$

$$P_2 = V_C I_2 \cos(\theta_2) \tag{3.11}$$

Since all ports provide unity power factor, the other two equations can be formed as,

$$\tan(\theta_1) = \frac{I_1 \cos(\theta_1)\omega L_1}{V_C - I_1 \sin(\theta_1)\omega L_1} = \frac{\sin(\theta_1)}{\cos(\theta_1)} \tag{3.12}$$

$$\tan(\theta_2) = \frac{I_2 \cos(\theta_2)\omega L_2}{V_C - I_2 \sin(\theta_2)\omega L_2} = \frac{\sin(\theta_2)}{\cos(\theta_2)} \tag{3.13}$$

These two can be simplified as,

$$I_1 \omega L_1 - V_C \sin(\theta_1) = 0 \tag{3.14}$$

$$I_2 \omega L_2 - V_C \sin(\theta_2) = 0 \tag{3.15}$$

Moreover, the tangent value of the current's phase angle at port 3 can be defined as,

$$\tan\left(\theta_3\right)=\frac{I_3\cos\left(\theta_3\right)\omega L_3}{V_C-I_3\sin\left(\theta_3\right)\omega L_3}=\frac{I_{3d}\omega L_3}{V_C-I_{3q}\omega L_3} \tag{3.16}$$

However, by replacing I_3, I_{3d}, I_{3q}, and θ_3 by the primary unknowns, the following equation can be obtained,

$$\begin{aligned}&\left[\left(V_C\omega C_{eq}\right)^2+I_1{}^2+I_2{}^2+2I_1I_2\cos(\theta_1-\theta_2)-2V_C\omega C_{eq}\left(I_1\sin\left(\theta_1\right)+I_2\sin\left(\theta_2\right)\right)\right]\omega L_3\\&=V_C\left(V_C\omega C_{eq}-I_1\sin\left(\theta_1\right)-I_2\sin\left(\theta_2\right)\right)\end{aligned} \tag{3.17}$$

There is a critical point on the sign of the tangent functions that needs to be clarified. For such a port that is providing negative power, that means the voltage and current are 180° out of phase. The tangent function for θ_i is the same in which value is solved by either I_q/I_d or V_q/V_d .

A three-port dc hub is designed and simulated in open loop to validate the steady state analysis performed above. The parameters of power circuit components of the dc hub are designed based on (3.1) and (3.2), and the default modulation indices are set to be 0.9 for all VSCs. The source side resistors are assumed to be zero under ideal conditions. The power components and operating data are listed in Table 3-1 and Table 3-2, respectively.

Table 3-1: Power circuit components of the three-port dc hub

L_1 (H)	L_2 (H)	L_3 (H)	C_{eq} (μF)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
0.0103	0.0154	0.0178	2.0465	0	0	0

By solving the system of equations of (3.10), (3.11), (3.14), (3.15), and (3.17), there are three operating points are met the requirements and under additional investigation. The solutions are listed in the Table 3-3.

Table 3-2: Operation parameters of the three-port dc hub

Port 1	Rated maximum power	150 MW
	DC link voltage	±150 kV
Port 2	Rated maximum power	-100 MW
	DC link voltage	±100 kV
Port 3	Rated maximum power	-50 MW
	DC link voltage	±50 kV
Fundamental frequency		1.25 kHz

Table 3-3: Operating points

Port Number	1	2	3
Solution 1			
Current (kA)	$1.1108\angle 33.53^\circ$	$1.1107\angle 123.76^\circ$	$1.1107\angle 106.13^\circ$
Voltage (kV)	$135.04\angle 33.53^\circ$	$90.03\angle -56.24^\circ$	$90.03\angle -73.87^\circ$
Modulation Index	0.9003	0.9003	0.9003
V_C	162.00 kV		
Solution 2			
Current (kA)	$1.3029\angle 42.36^\circ$	$0.8899\angle 136.16^\circ$	$1.0597\angle 107.63^\circ$
Voltage (kV)	$115.13\angle 42.36^\circ$	$112.38\angle -43.84^\circ$	$47.18\angle -72.37^\circ$
Modulation Index	0.7675	1.1238	0.9437
V_C	155.79 kV		
Solution 3			
Current (kA)	$1.8105\angle 60.40^\circ$	$1.2008\angle 119.77^\circ$	$0.3085\angle 165.07^\circ$
Voltage (kV)	$82.85\angle 60.40^\circ$	$83.28\angle -60.23^\circ$	$162.07\angle -14.93^\circ$
Modulation Index	0.5523	0.8328	3.2415
V_C	167.74 kV		

However, not all solutions are feasible in reality. For two-level VSCs, the modulation index should be less than unity to ensure that the operation is in the linear range. Therefore, in the control system, the modulation index is limited to unity. Meanwhile, as mentioned earlier, the modulation indices are designed to be 0.9 for all VSCs in the dc hub. Thus, only solution 1 can be feasible in reality as only in solution 1 all modulation indices are less than unity.

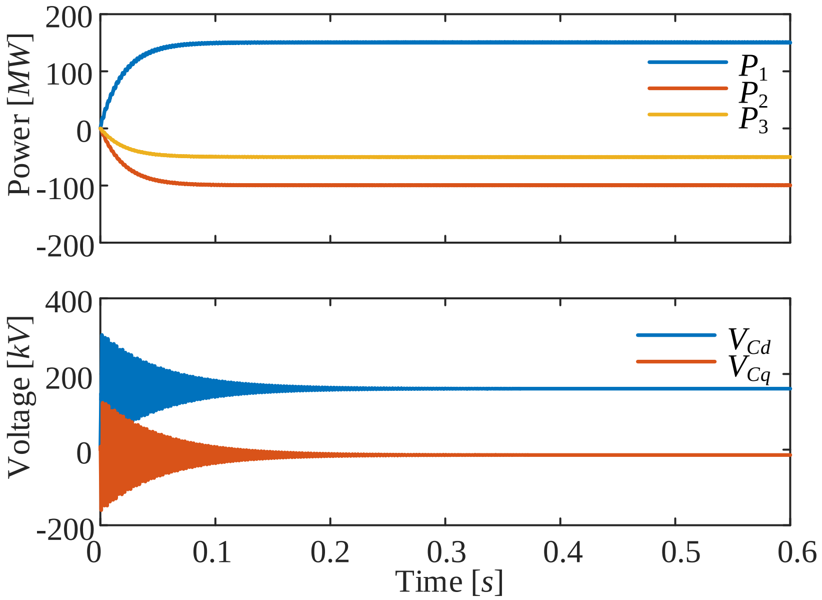

Figure 3-6: PSCAD/EMTDC simulation for the averaged model of a three-port dc hub

To verify this solution, this model is simulated in PSCAD/EMTDC. It is important to mention that the source side resistance cannot be zero in reality. This is because the dc hub will lack damping if there is no resistance.

The simulation results of maximum port powers and dq component of the dc hub are shown in Figure 3-6. The maximum powers of these three ports are 150 MW, -100 MW and -50 MW, respectively. The value of V_{Cd} is around 161.2 kV and V_{Cq} is close to 0 kV, under steady state. The simulation result closely match the results in the steady state analysis. The minor differences are resulted from adding the source side resistance in the simulation and the errors can be taken care of when a closed-loop control system is added.

Overall, the simulation in PSCAD/EMTDC has verified the operating point from the steady state analysis.

3.4 Harmonic Analysis

In [8], it is claimed that the dc hub with two-level VSCs only requires the switching frequency of three times the operating frequency. Although the LCL filter may be strong and may take care of the current harmonics from each port, a low switching frequency may result in an inaccurate RMS value of the fundamental component of the voltage, V_i^m , at each VSC. Equation (3.18) given in [8] approximates the magnitude of the fundamental component of the switching pulse under ideal case.

$$V_i^m \simeq \frac{4M_iE_i}{\pi\sqrt{2}} \tag{3.18}$$

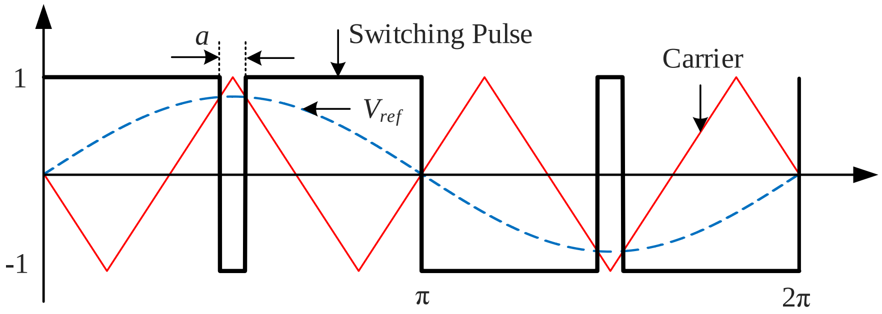

Figure 3-7: Bipolar switching of a two-level VSC

$$S = \begin{cases} 1 & 0 \le \omega t < a \\ -1 & a \le \omega t < \pi - a \\ 1 & \pi - a \le \omega t < \pi \\ -1 & \pi \le \omega t < \pi + a \\ 1 & \pi + a \le \omega t < 2\pi - a \\ -1 & 2\pi - a \le \omega t < 2\pi \end{cases} \tag{3.19}$$

The switching pulse of a two-level VSC with a switching frequency of three times the fundamental frequency is shown in Figure 3-7 and the its expression if shown in (3.19). To perform harmonic analysis, the Fourier series of the switching functions can be defined as in (3.20).

$$C_k = \frac{1}{T}\int_0^T S_{(t)} e^{-jk\frac{2\pi}{T}\omega t} d\omega t \tag{3.20}$$

The sinusoidal function has a period of $T = 2\pi$, therefore,

$$C_k = \frac{1}{T}\left[\int_0^a e^{-jk\omega t} - \int_a^{\pi-a} e^{-jk\omega t} + \int_{\pi-a}^{\pi} e^{-jk\omega t} - \int_{\pi}^{\pi+a} e^{-jk\omega t} + \int_{\pi+a}^{2\pi-a} e^{-jk\omega t} - \int_{2\pi-a}^{2\pi} e^{-jk\omega t}\right] d\omega t \tag{3.21}$$

Based on the property of quarter cycle symmetry there is no dc component and,

$$C_k = \begin{cases} \frac{2}{T}\left(S_{(k)} - S_{(-k)}\right), & odd\, k \\ 0, & even\, k \end{cases} \tag{3.22}$$

Therefore, there is no even order harmonics and,

$$C_{k,odd} = \frac{2j}{\pi k}\left(e^{-jka} + e^{jka} - 1\right) = \frac{2j}{\pi k}\left(2\cos(ka) - 1\right) \tag{3.23}$$

The Fourier series can be written as,

$$S_{(t)} = C_0 + \sum_{k=1,odd}^{+\infty} 2\left|C_k\right| \cos\left(k\frac{2\pi}{T_0}\omega t + \angle C_k\right) \tag{3.24}$$

where $C_0 = 0$ due to the property of quarter cycle symmetry. The value of a depends on the modulation index m of the VSC. It can be solved by the following function,

$$m\sin(a) = -2 + \frac{6}{\pi}a \tag{3.25}$$

Based upon equation (3.25), the relationship between the modulation index and a can be plotted as shown in Figure 3-8.

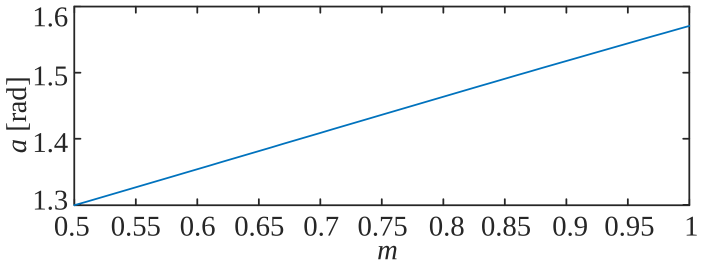

Figure 3-8: Modulation index vs. α

As an example, a two-level VSC with a modulation index of 0.9 is investigated and $\alpha = 1.52$ in this case. The Fourier spectrum of the switching pulse is plotted in Figure 3-9.

The VSC theoretically is a replacement of a voltage source. Thus, the fundamental component should be close enough to the equivalent voltage source. Under this case, the modulation index is set to be 0.9; however, the 1st order harmonic has a magnitude of 1.14, which is higher than the desired modulation index of 0.9. Therefore, to ensure the accuracy of the modulation index, it is possible to introduce a correction factor, *CF*, which is to be multiplied by the reference signal of the VSC. It is important to mention that adding the correction factor is to reduce the error between the desired magnitude of the fundamental component and the actual one. The correction factor *CF* in this case can be found as,

$$CF = \frac{0.9}{1.14} = 0.79 \tag{3.26}$$

To verify the correction factor, a comparison of the capacitor voltage is conducted as an inaccurate ac fundamental component from the VSC sides will affect the value of the capacitor voltage. The anticipated magnitude of the capacitor voltage is 162 kV. Based on the design in this case, with three voltage sources connected, the harmonic spectrum of the capacitor voltage is shown in Figure 3-10.

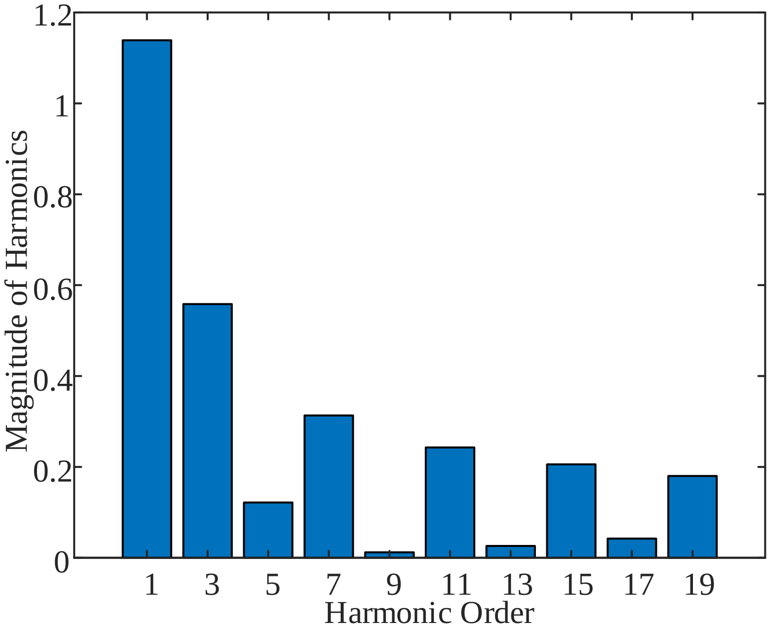

Figure 3-9: Harmonic spectrum of the switching pulse

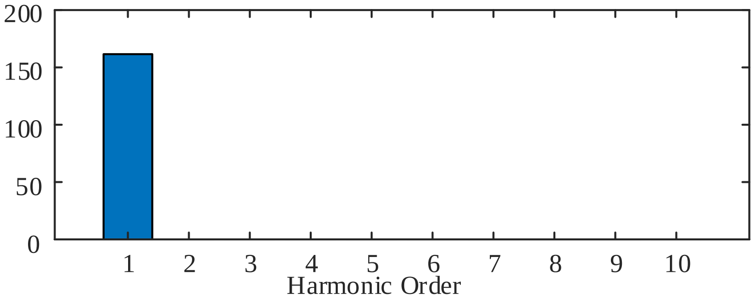

Figure 3-10: Capacitor voltage of the dc hub with ac sources connected

With the VSCs connected and when the correction factor is not applied, the harmonic spectrum of the capacitor voltage is shown in Figure 3-11.

After the correction factor applied, the harmonic spectrum of the capacitor voltage is shown in Figure 3-12.

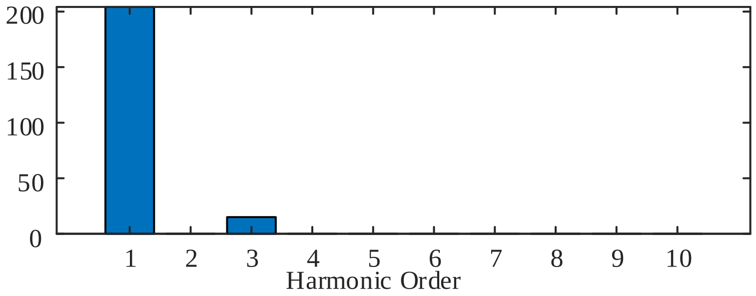

Figure 3-11: Capacitor voltage of the dc hub without correction factor applied

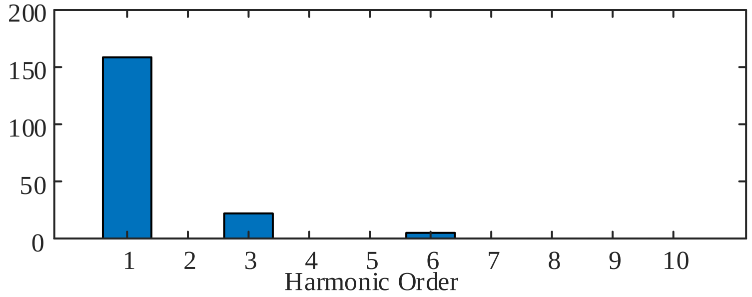

Figure 3-12: Capacitor voltage of the dc hub with correction factor applied

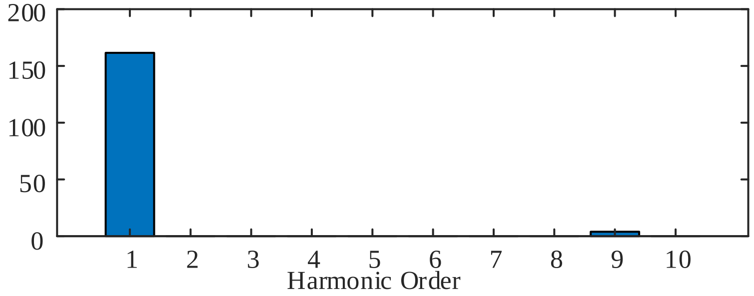

Figure 3-13: Capacitor voltage of the dc hub with increased switching frequency

According to the above harmonic spectra of the capacitor voltage under different conditions, the dc hub with voltage sources connected shows a reasonable value of the capacitor voltage; the dc hub with VSCs connected has a fairly large fundamental component; therefore, it results in a large value of capacitor voltage; by adding the correction factor, the fundamental component of the capacitor voltage drops to such value that is close to the one obtained from the dc hub with voltage sources connected. Moreover, with VSCs connected to the dc hub, there is a considerably large amount of 3rd harmonic. A large high order harmonic may result in challenges to control, as it will bring oscillations to the dq components if dq0 transformation is applied in the control method.

Alternatively, it is possible to increase the switching frequency to reduce the impact due to the low switching frequency. The harmonic spectrum of the capacitor voltage is shown as Figure 3-13. The fundamental component of the capacitor voltage is very close to the simulation result from the dc hub with ac source connected. In addition, the most significant harmonic is 9th and its magnitude is almost negligible.

Chapter 4 Dynamic Control for DC Hubs

4.1 Single Phase dq Transformation

Figure 3-3 shows that any vector in phasor domain can be decomposed into a real part and an imaginary part. In control systems with conventional controllers such as proportional-integral (PI) blocks, static (dc type) quantities are much easier to work with than dynamic quantities such as sinusoidal waveforms. Therefore, single phase dq transformation may be introduced to present the time-based ac waveforms in terms of two dc signals, i.e., *d* and *q* components, whose magnitudes are equal to the real part and imaginary part of such a vector in phasor domain.

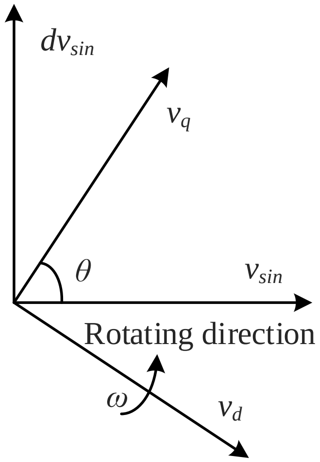

Figure 4-1: Single phase dq transformation

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{bmatrix} v_{\sin} \\ dv_{\sin} \end{bmatrix} \tag{4.1}$$

In general, d and q are two rotating vectors that are orthogonal to one another, as shown in Figure 4-1. To implement dq transformation, first of all, it is required to obtain two sinusoidal signals, defined as v_{sin} and dv_{sin} such that dv_{sin} that has a 90^o phase shift relative to v_{sin}. The phase θ changes with a speed of ω. The magnitude of v_d and v_q can be computed based on the projections of v_{sin} and dv_{sin} on v_d and v_q vectors. Thus, the transformation can be represented in matrix form as in (4.1) and the magnitude of the real part and imaginary part of v_{sin} can be defined through this transformation.

4.2 Control System of a Multiport DC Hub

According to the operating principles summarized earlier, a three-port dc hub control system is shown in Figure 4-2. The concept of this control is based on the two-port dc hub control method proposed in [10]. Similar to the two-port dc hub control, there are six inner loops to control the dq components of port currents. Each I_{iq} reference is computed based on its corresponding I_{id} reference and the phase angle to ensure that the port operates at unity power factor. The current flow from the VSCs to V_C can be simplified in Figure 4-2.

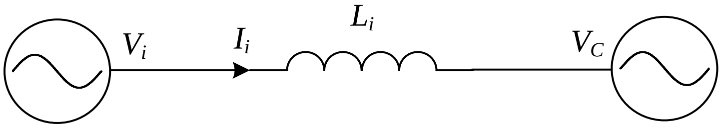

Figure 4-2: Current flow from a port to centre of the dc hub

Since the phase angle of V_C is considered as reference, V_{Cq} is always defined as zero. Under steady state, (4.2) can be written.

$$j\omega L_i (I_{id} + jI_{iq}) = V_{id} + jV_{iq} - V_{Cd} \tag{4.2}$$

From (4.2), the dq components of I_i can be determined as,

$$I_{id} = \frac{V_{iq}}{\omega L_i} \tag{4.3}$$

$$I_{iq} = \frac{V_C}{\omega L_i} - \frac{V_{id}}{\omega L_i} \tag{4.4}$$

In (4.3) and (4.4), ωL_i is a constant and V_C is assumed to be constant in steady state. Therefore, I_{id} can be controlled by controlling V_{iq} and I_{iq} can be controlled by controlling V_{id}. In the control system, M_{id} and M_{iq} are the two direct factors that can control V_{id} and V_{iq}, respectively.

However, the power references to the outer loops are given individually except for one port power that must balance the total power. For instance, in Figure 4-3, P_{2ref} and P_{3ref} are given individually to generate the I_{id} references for these two ports. However, I_{1ref} is computed directly based on the I_{id} reference for other ports since the sum of I_{id} must be zero to force V_{cq} to be zero. The reason for not adding another PI controller to generate I_{1d} references based on P_{1ref} is that in reality the dc hub will not be lossless; the sum of port powers is not zero if losses are considered. This control design can be extended to a larger number of ports. In such a case, all inner loop controllers will remain unchanged. All I_{id} references are the output of the power control loops except only one for which the I_{id} reference is automatically known from other I_{id} references.

In addition, although the harmonics in the dc hub do not play any role in power conversion or power quality, they will bring challenges to the controllers. The harmonics will generate considerably large ripples and oscillations on the dq components after performing dq transformation. As a consequence, filters are added in the control loops to filter out ripples on the dq components of the port currents.

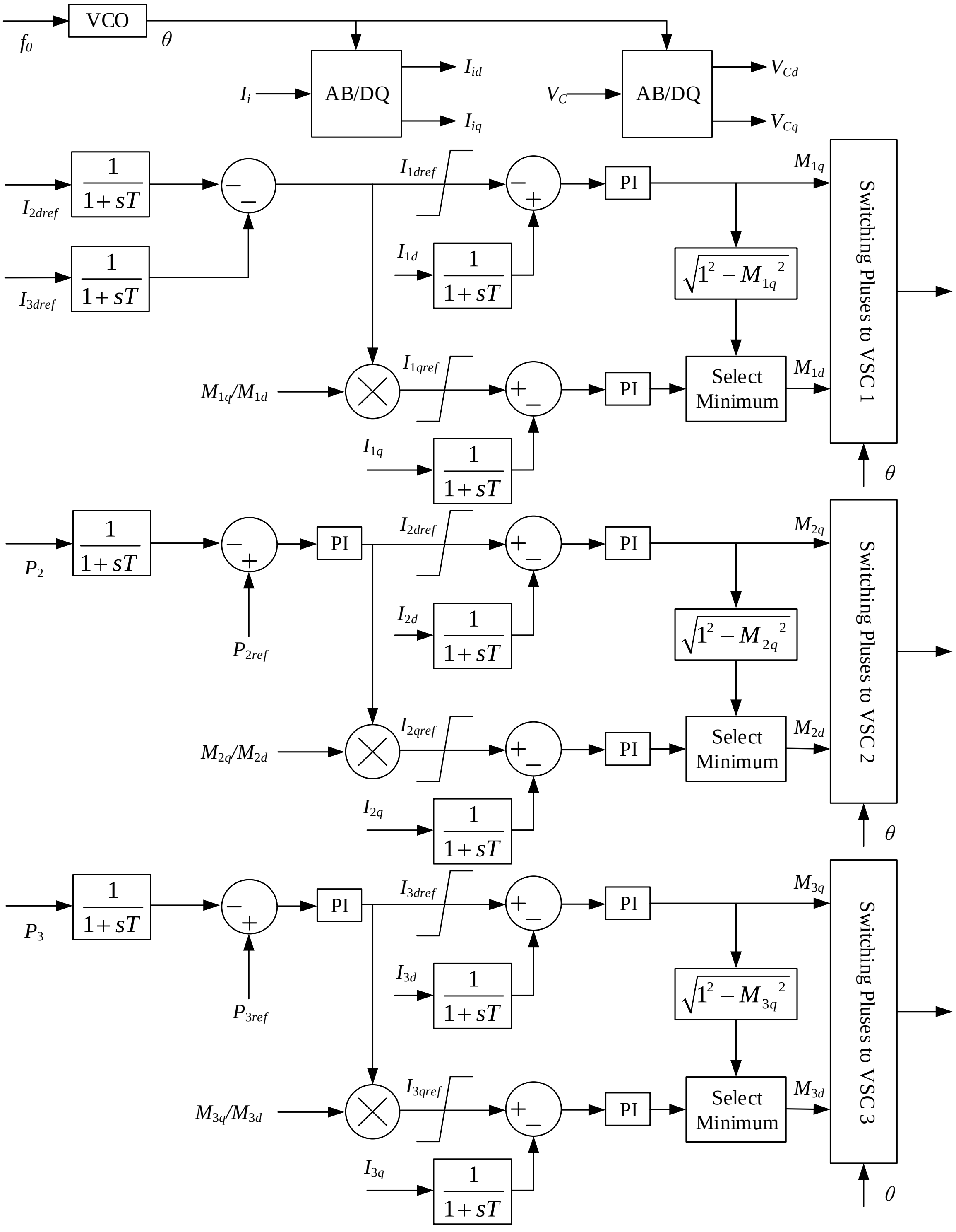

Figure 4-3: Control diagram of a three-port dc hub

The minimum selecting block on M_{id} is to ensure that the modulation indices M_i for all ports are always within the linear operation range.

4.3 Nonlinearity of the Control System

PI controllers are used in this control system and, in general, PI controllers are considered as a linear controller. From (4.3) and (4.4), it is obvious that I_{id} and I_{iq} have linear relationships to M_{iq} and M_{id}, respectively. However, the reference I_{idref} is a function of the dq components of the modulation index. The function of M_{id} can be written as,

$$M_{id} = \left(\frac{M_{iq}}{M_{id}} - I_{iq}\right)\left(K_p + \frac{K_i}{s}\right) \tag{4.5}$$

Thus, after adding outer loops from port powers control the control system for the dc hub loses its linearity.

4.4 Validation of the Control System

This control system is tested on the designed three-port dc hub in PSCAD/EMTDC simulation with a time-step of 0.1 µs to obtain detailed simulation results. The LCL filter parameters are shown in Table 3-1, and the source side resistances R_i are set to be 0.5 Ω. In Section 3.4, it was shown that under a low switching frequency the high order harmonics have noticeable magnitudes and they may bring significant oscillations into the dq components if dq transformation is applied. This makes it challenging to properly respond to the changes in the dc hub as the filters in the control system need a very large time constant to smooth out the dq component of the current. A large time constant on the filter will potentially decrease the speed of response of the controllers. To avoid this issue, the switching frequency is set to be 11.25 kHz, which is nine times the fundamental frequency of V_C. The frequency modulation index of nine is still much smaller than the conventional modulation index of 15 for two-level VSCs.

The PI controller tuning follows the guidance in [10] and the parameters for PI controllers are shown in Table 4-1.

Table 4-1: Parameters of PI controllers of the three-port dc hub

PI	I_{1d}	I_{1q}	I_{2d}	I_{2q}	I_{3d}	I_{3q}	P_2	P_3
K_p	0.05	0.05	0.05	0.05	0.05	0.05	10^{-4}	10^{-4}
$T_i\,(1/K_i)$	0.06	0.4	0.4	2	0.4	0.5	200	200
Upper Limit	1	1	1	1	1	1	0	0
Lower Limit	-1	0.01	-1	0.01	-1	0.01	-3	-3

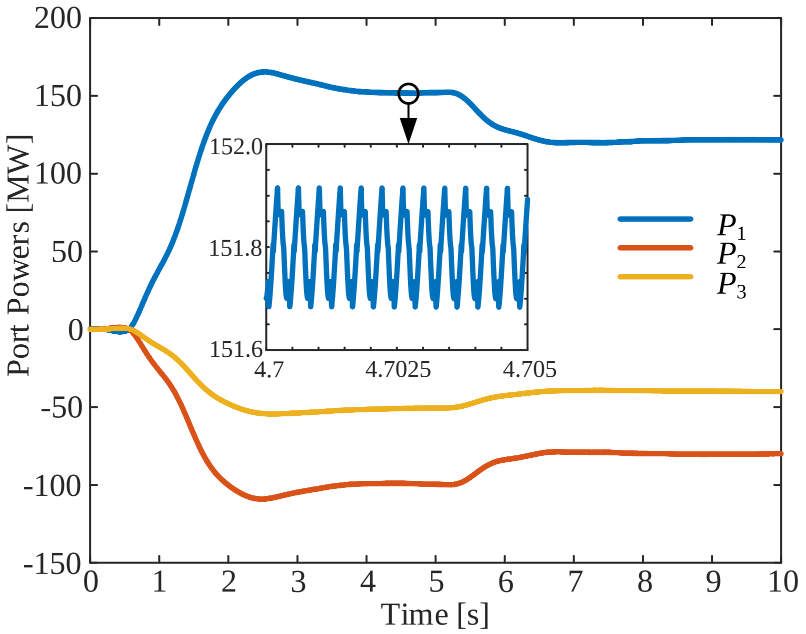

Figure 4-4: Power plots of a three-port dc hub with closed loop control

The simulation runs from a time period of zero to ten seconds and changes to power references are given to the controller at $t = 5$ s. At this point, the powers for port 2 and 3 are dropped from -100 MW and -50 MW to -80 MW and -40 MW. In any circuit, the port in the network must have a zero summation. Hence, the power for port 1 is equal to the absolute value of not only the sum of power for port 1 and port 2, but also the losses from switching and source side resistances. The dc hub takes about 1.5 s to achieve steady state after the transient is applied. The response speed is strongly depending on the time constant of the PI controllers in the outer loop of its control system.

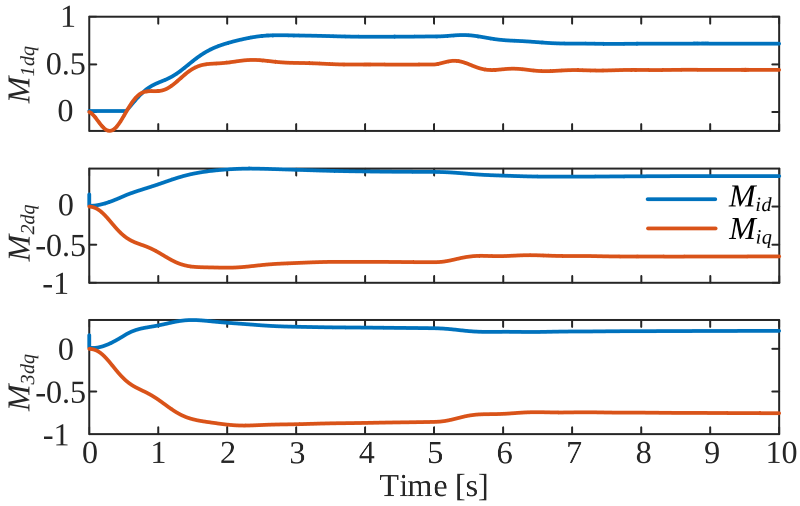

Figure 4-5: dq components of the modulation indices

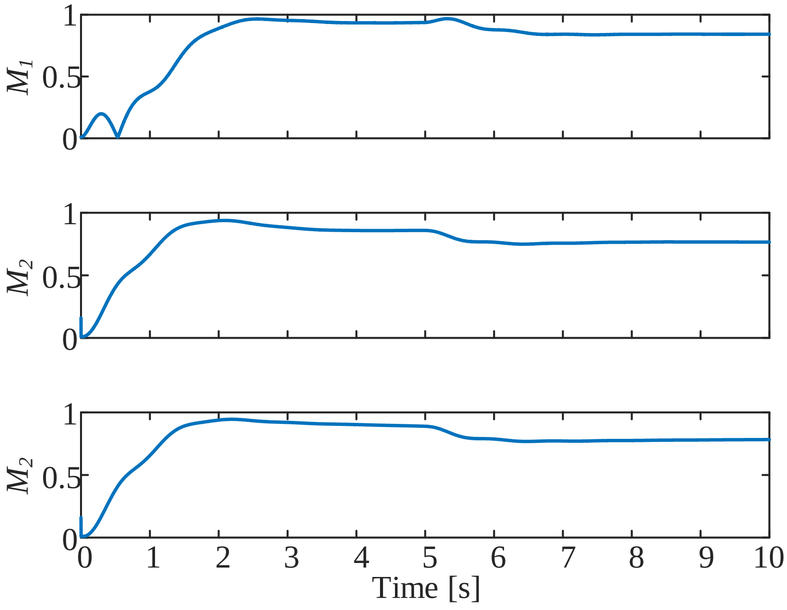

Figure 4-6: Modulation indices of the dc hub

Figure 4-5 shows the dynamic changes on the dq component of the modulation indices, which are the outputs from the inner loop PI controllers. All M_{id} and M_{iq} are always within the limited range of the outputs of the PI controllers.

Figure 4-6 indicates the magnitude of modulation indices of the dc hub are less than unity and all three VSCs are operating under linear operation range. It implies the minimum selection blocks in the control system are not active in this process.

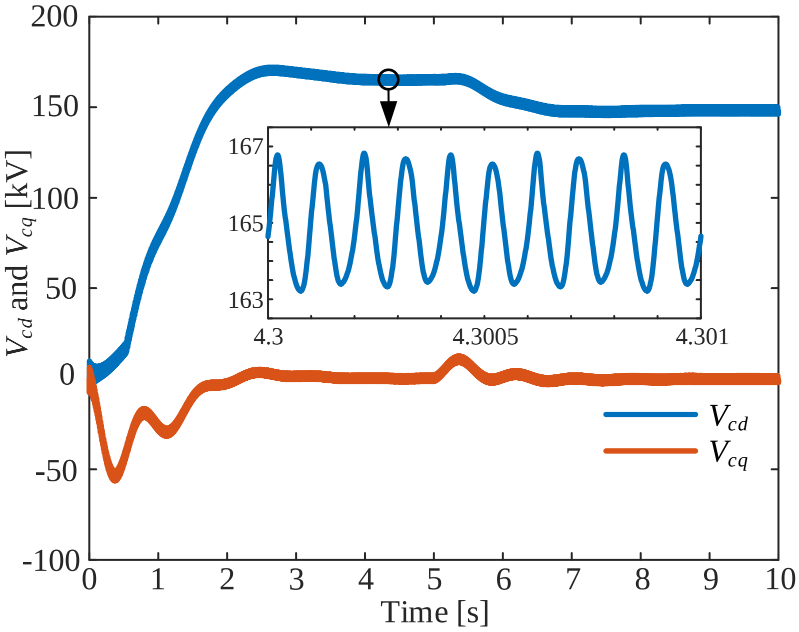

Figure 4-7: dq components of V_C

Figure 4-7 shows that phase of V_C is locked to be the reference angle since V_{Cq} oscillates around zero under steady state. The capacitor voltage is close to the designed value 162 *kV*, and the error is resulted from R_i.

Figure 4-8 shows the dq components of I_i. The summation of all I_{iq} are about zero. This implies there is no reactive power from the VSCs to the center of the dc hub. In addition, this is also a sign that all VSCs are operating with a unity power factor, i.e., the voltage and current for every port are in phase.

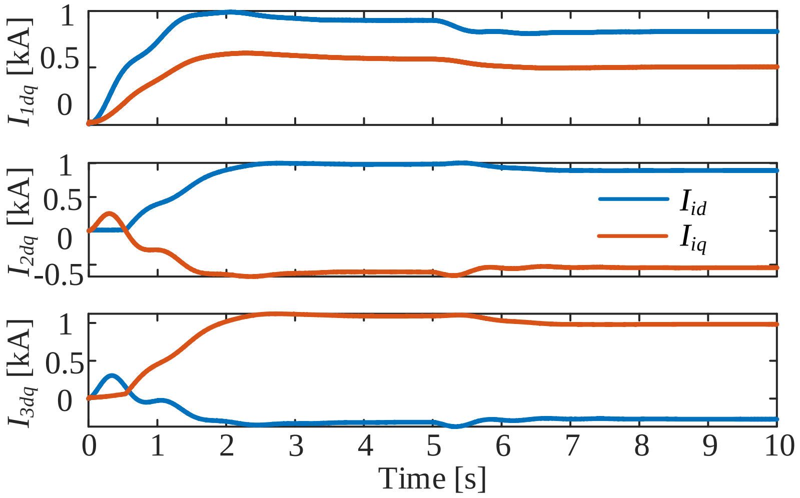

Figure 4-8: dq component of I_i

Overall, the closed loop control for a multiport dc hub has been verified by implementing in a three-port dc hub with dynamic changes. The simulation results match the theoretical values and principles of operation.

Chapter 5 Dynamic Modeling of DC Hubs

5.1 Dynamic Phasor Model

Since the control system only processes and controls the dq components, it is not beneficial to simulate the dc hub in the original *abc* domain. For example, the default simulation mode in PSCAD/EMTDC uses nodal analysis for the power circuit components and the currents and voltages are in the original *abc* domain. To process the control system, all signals in the *abc* domain must be converted into a dq frame. However, performing dq transformation will cause a small angle delay for signals in the dq components [11]. This angle delay may not be significant for a low-frequency system (e.g., 60 Hz); however, it will have a considerable impact on the phase angle information if the base frequency is large (e.g., 1 kHz). Table 5-1 indicates the significance of the phase angle delay due to the one time-step delay. The EMT simulation speed of the dc hub with closed loop control built in PSCAD/EMTDC requires a very small time-step. Therefore, the simulation speed is slow.

Table 5-1: Phase delay impacts

Operating Frequency	Simulation Time-step	Phase Delay
60 Hz	50 μs	1.08 degrees
1250 Hz	50 μs	22.5 degrees
1250 Hz	2.5 μs	1.125 degrees

The harmonic contents of the dc hub may be reduced using higher switching frequencies, MMC topologies, or optimal pulse width modulation (OPWM) methods. The focus of this paper will be on the fundamental component dynamics of the dc hub, and the average-value model in this paper is developed for this purpose. A three-port dc hub is investigated and the VSCs are considered as ac sources in the averaged model depicted in Figure 3-4.

To model this circuit, the concept of generalized averaging method [23] is employed. Each *abc*-domain variable is approximated with its fundamental component, which itself is represented by its time-varying Fourier coefficients (or dq components) as follows.

$$x(t) = x_d + jx_q \tag{5.1}$$

The dq components are, in general, functions of time because of the transients in the original variables. The following expression is useful in modeling using the generalized averaging concept.

$$\frac{d}{dt}\langle x\rangle_k(t) = \langle \frac{d}{dt}x\rangle_k(t) - jk2\pi f\langle x\rangle_k \tag{5.2}$$

where f is the frequency of the fundamental component.

The dc hub may be controlled using the magnitude and phase of each converter output, or in other words the dq components of the port voltages. Thus, the state space equations for the ac part of the hub are as follows.

$$\frac{d}{dt}I_{id} = \frac{1}{L_i}(V_{di} + \omega L_i I_{iq} - V_{Cd} - R_i I_{id}) \tag{5.3}$$

$$\frac{d}{dt}I_{iq} = \frac{1}{L_i}(V_{qi} - \omega L_i I_{id} - V_{Cq} - R_i I_{iq}) \tag{5.4}$$

$$\frac{d}{dt}V_{Cd} = \frac{1}{C_{eq}}(I_{Cd} + \omega C_{eq} V_{Cq}) \tag{5.5}$$

$$\frac{d}{dt}V_{Cq}=\frac{1}{C_{eq}}(I_{Cq}-\omega C_{eq}V_{Cd}) \tag{5.6}$$

Therefore, the state space equations can be written in the matrix form as follows.

$$\frac{d}{dt}\begin{bmatrix} I_{1d} \\ I_{1q} \\ I_{2d} \\ I_{2q} \\ I_{3d} \\ I_{3q} \\ V_{Cd} \\ V_{Cd} \end{bmatrix} = \boldsymbol{A}\begin{bmatrix} I_{1d} \\ I_{1q} \\ I_{2d} \\ I_{2q} \\ I_{3d} \\ I_{3q} \\ V_{Cd} \\ V_{Cd} \end{bmatrix} + \boldsymbol{B}\begin{bmatrix} V_{1d} \\ V_{1q} \\ V_{2d} \\ V_{2q} \\ V_{3d} \\ V_{3q} \end{bmatrix} \tag{5.7}$$

where $\boldsymbol{A}$ is expressed as,

$$\boldsymbol{A}=\begin{bmatrix} -\frac{R_1}{L_1} & \omega & 0 & 0 & 0 & 0 & -\frac{1}{L_1} & 0 \\ -\omega & -\frac{R_1}{L_1} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{R_2}{L_2} & \omega & 0 & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & -\omega & -\frac{R_2}{L_2} & 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & 0 & 0 & -\frac{R_3}{L_3} & \omega & -\frac{1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & -\omega & -\frac{R_3}{L_3} & 0 & -\frac{1}{L_3} \\ \frac{1}{C_{eq}} & 0 & \frac{1}{C_{eq}} & 0 & \frac{1}{C_{eq}} & 0 & 0 & \omega \\ 0 & \frac{1}{C_{eq}} & 0 & \frac{1}{C_{eq}} & 0 & \frac{1}{C_{eq}} & -\omega & 0 \end{bmatrix}$$

where $\boldsymbol{B}$ is expressed as,

$$\boldsymbol{B} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_3} \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

In the state space equations, all the state variables are dc quantities in steady state; during transients the variations of dq components represent the changes in the magnitude and phase angle of the fundamental component of the respective variable. The above differential equations can be solved numerically using a suitable integration method. Since the system of equations in (5.7) is linear, the trapezoidal integration method may be applied readily.

5.2 Control Processing

In a linear system, controllers may be written directly into the state space equations and become a part of ***A*** and ***B*** matrices. However, the control system of a dc hub is nonlinear; linearization around an operating point may be used at the expense of losing large-signal representability. In this work, the nonlinear control system is formulated and solved separately from the linear systems equations. This allows the use of different integration methods, e.g., trapezoidal method for linear system equations and Euler's method for the nonlinear controls.

A proportional-integral (PI) controller is shown in Figure 5-1.

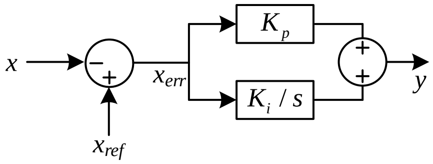

Figure 5-1: Block diagram of a PI controller

The input to the PI controller is

$$x_{err}(t) = x_{ref} - x(t) \tag{5.8}$$

where x is the controlled variable and x_{ref} is the desired reference. The output of the PI controller is

$$y(t) = K_p x_{err}(t) + \int K_i x_{err}(t) dt \tag{5.9}$$

where K_p and K_i are the gains of the PI controller. With

$$a(t) = \int K_i x_{err}(t) dt \tag{5.10}$$

Euler's method may be used to implement the integration with proper saturation limits in place for those in both $a(t)$ and the PI controller output $y(t)$. Moreover, the transfer functions of all filters in the control system are in the same form as shown below,

$$G_f(s) = \frac{1}{1+sT} \tag{5.11}$$

where T is the time constant of the filter. This first-order differential equation may also be solved using either of the two integration methods.

5.3 Model Validation

The same three-port dc hub with closed loop control is investigated by using the proposed averaged model. The three-port dc hub with closed loop control is simulated in PSCAD/EMTDC (detailed EMT simulation) and its results are used to benchmark the accuracy and computational advantage of the developed average-value model (implemented in MATLAB).

Both models are run for a simulation time period of 10 s. The time-step used in the EMT model is 0.1 μs, which is necessary to have proper representation of the switching converters. For the simulation of developed average-value model, a time-step of 1000 μs is selected to ensure the numerical stability and simulation accuracy. In the EMT model, the integration method is trapezoidal rule. For the integration of the averaged model, the state equations are solved by the trapezoidal rule and the control system is solved using Euler's method. The procedure of these two integration methods can be summarized as follow. Assume there is a linear time invariant state space equations,

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t) \tag{5.12}$$

For Euler's method,

$$\boldsymbol{x}(t+\Delta t) = \boldsymbol{x}(t) + \left(\boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t)\right)\Delta t \tag{5.13}$$

For Trapezoidal method,

$$\boldsymbol{x}(t+\Delta t) = \left(\boldsymbol{I} - \frac{1}{2}\boldsymbol{A}\Delta t\right)^{-1}\left[\left(\boldsymbol{I} + \frac{1}{2}\boldsymbol{A}\Delta t\right)\boldsymbol{x}(t) + \boldsymbol{B}\frac{\boldsymbol{u}(t)+\boldsymbol{u}(t+\Delta t)}{2}\Delta t\right] \tag{5.14}$$

where $\boldsymbol{I}$ is the identity matrix and Δt is the time-step for the numerical integration.

The simulation results based on computation from the proposed averaged model are compared to the simulation results from PSCAD/EMTDC. Comparison of the simulation results, including port powers, dq components of modulation indices, port currents, as well as the capacitor voltage, is shown in Figure 5-2 to Figure 5-5.

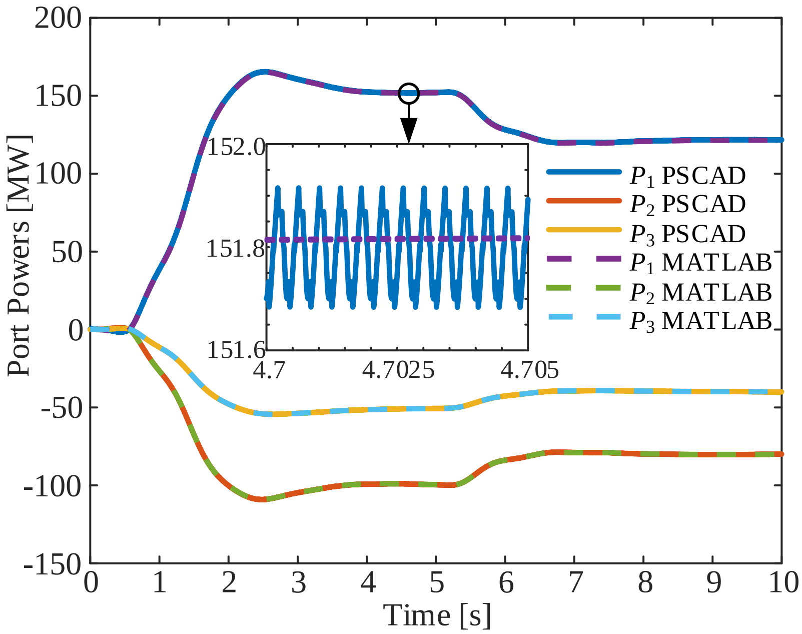

Figure 5-2: Simulation results comparison of port powers

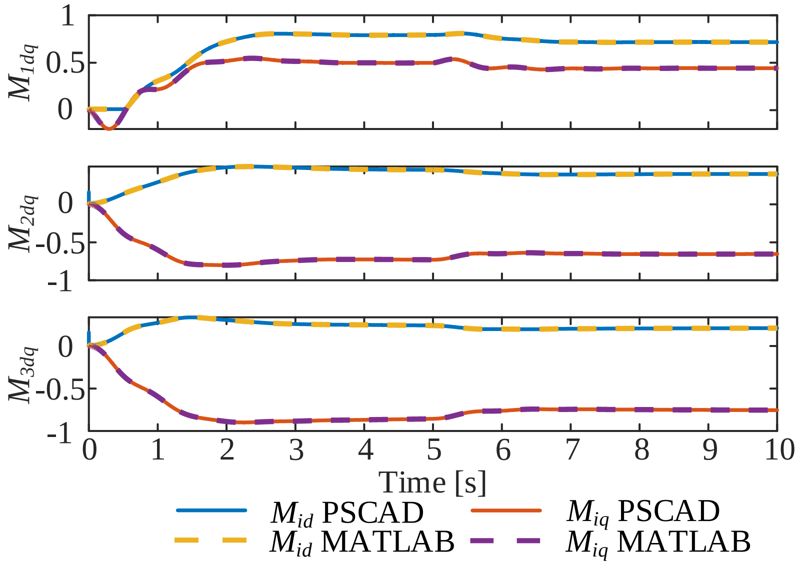

Figure 5-3: Simulation results comparison of dq components of modulation indices

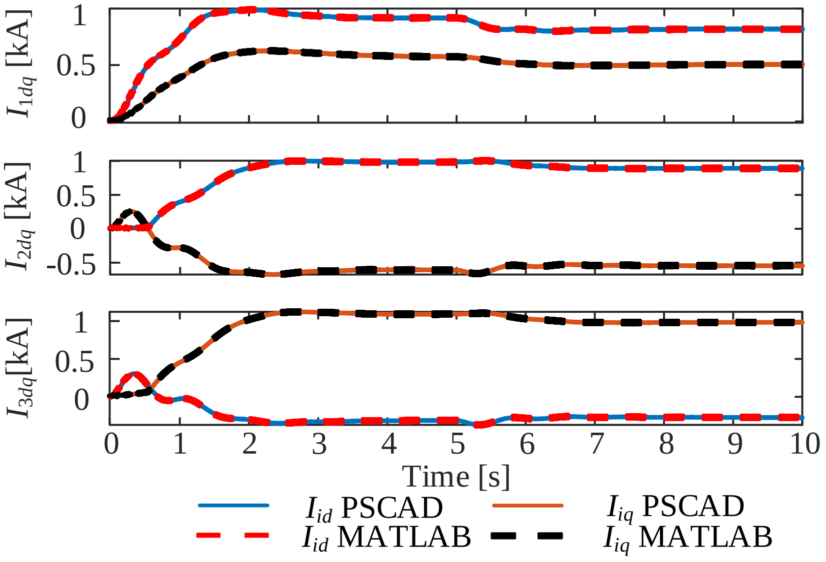

Figure 5-4: Simulation results comparison of filtered I_{idq}

The simulation results from both the PSCAD/EMTDC model and the average-value model match closely, which validates the accuracy of the proposed average model.

As indicated in Chapter 4, there are only two references for the 3-port system. In the simulations, power references are initially set to -100 MW and -50 MW for ports 2 and 3, respectively. To verify the dynamics of the averaged model under the proposed control method shown in Figure 3-4, step changes in power references are applied at $t = 5$ s to ports 2 and 3, which drop to -80 MW and -40 MW, respectively. As shown in Figure 5-2 to Figure 5-5, the system quickly responds to these step changes and the dc signals of corresponding dq components settle to the desired values under both simulations using PSCAD/EMTDC and the averaged model. Therefore, the proposed control method for multiport dc hub is effective and the averaged model can accurately represent the system operation with a much larger time-step.

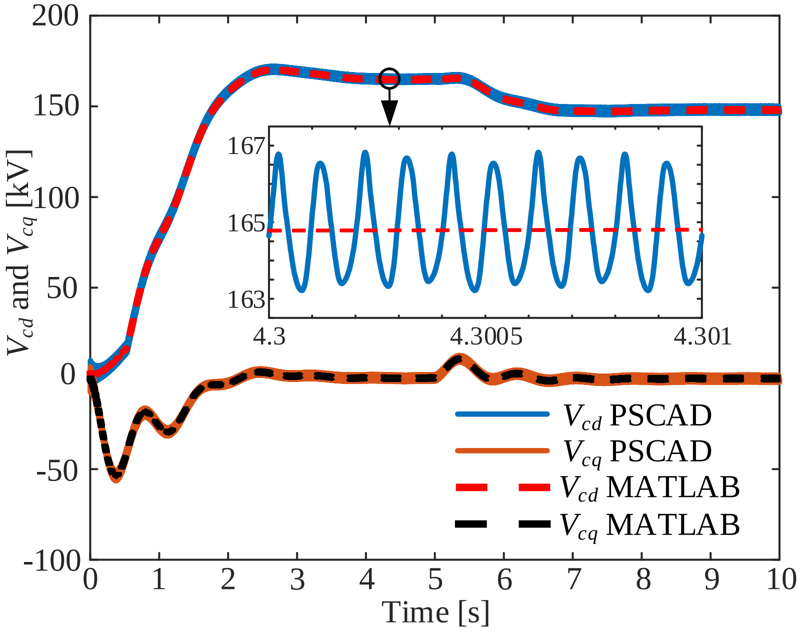

Figure 5-5: Simulation results of dq components of V_C

5.4 Comparison of Simulation Efficiency

The simulations using these two models are performed on the same computer. Computational efficiency is summarized in Table 5-2. Without noticeable loss of accuracy, the simulation speed of the proposed average model is clearly faster than the EMT model due to the significantly larger time-steps that may be used in this model. The simulation time-steps shown in Table 5-2 are the largest values for each simulator to produce accurate results. As seen the developed average-value model is in more than 600 times faster than the EMT model, yet produces results of virtually identical quality. It must be noted that the two models are implemented in markedly different computing environments. The average-value model is implemented in MATLAB, whereas the EMT model is in PSCAD/EMTDC. MATLAB is a far slower platform than the FORTRAN-based EMTDC solver; despite this disadvantage, the average-value model outperforms that EMT model significantly. If the two models are implemented in the same environment, the computational advantage of the average value model will be even more pronounced.

Table 5-2: Simulation efficiency comparison

Model	Simulation time-step	CPU time of computations
PSCAD/EMTDC	0.1 μs	about 450 s
Averaged Model	1000 μs	0.67 s

5.5 AC Waveforms Recovery

Due to the large time-step used in the simulation of the proposed model, recovery of the ac waveforms for display purposes needs special attention. Since the fundamental frequency is high, there will not be sufficient data points to show the ac waveforms using the granular data points in the respective *dq* quantities. To obtain the ac waveforms, an ac waveform recovery method is used. As a rule of thumb, the largest time-step that can be used in simulation is

$$t_{largest} \leq \frac{1}{10} \times \frac{1}{f_{highest}} \tag{5.15}$$

where $f_{highest}$ is the largest harmonic component of interest. For instance, a 1.25 kHz ac system may be simulated with a time-step no larger than 80 μs. With more points within one cycle, ac waveforms can be recovered more accurately. To recover an ac waveform, it is possible to insert more data points in its *dq* components before conversion to the *abc* frame. The computation of the inserted data points can be approximately decided based on the slope and the values between two original points. For example, in a dc waveform, suppose that there are two points (d_1 and d_2), and the time-step is Δt_1. If the required time-step for displaying the ac waveforms is Δt_2, then the number of data points to be inserted between d_1 and d_2 is,

$$n = \frac{\Delta t_1}{\Delta t_2} - 1 \tag{5.16}$$

The inserted data points can be computed as

$$d'_i = i \frac{d_2 - d_1}{\Delta t_1} \Delta t_2, i = 1, 2, ..., n \tag{5.17}$$

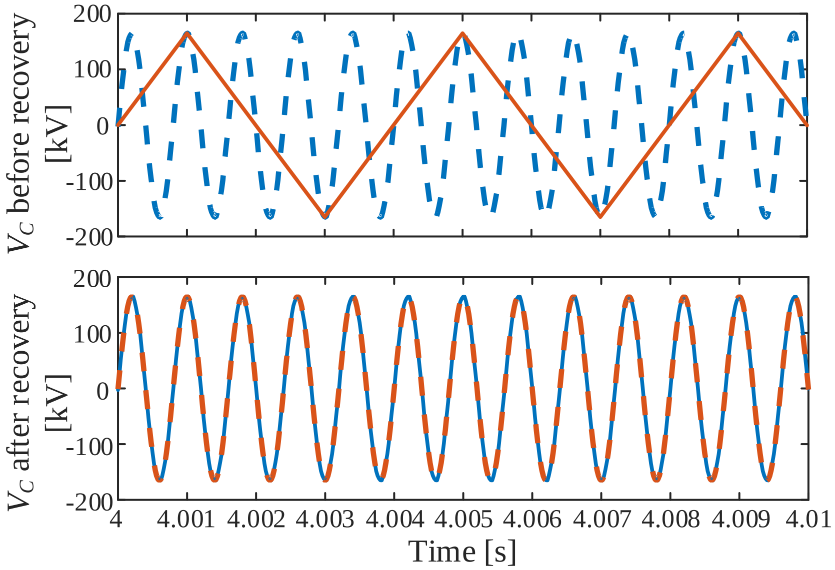

Figure 5-6: Comparison of AC waveform on V_C

Using this method, the capacitor voltage and port currents are recovered from *dq* components and compared to the simulation results obtained from the EMT model, as shown in Figure 5-6 and Figure 5-7. It is observed from Figure 5-6 that the original V_C envelope waveform computed by the proposed average model does not display a sinusoidal waveform, while the recovered capacitor voltage waveform in MATLAB matches well to the result from the detailed EMT model.

In Figure 5-7, with the same recovery method, the recovered current waveforms show excellent fit into the detailed simulation results. The port currents do not completely match with the PSCAD/EMTDC solution is because this method only provides allowance to display the fundamental ac waveform since the proposed average model only simulates the fundamental component. Nevertheless, by adding more harmonics this method will provide adequately accurate representations of ac waveforms.

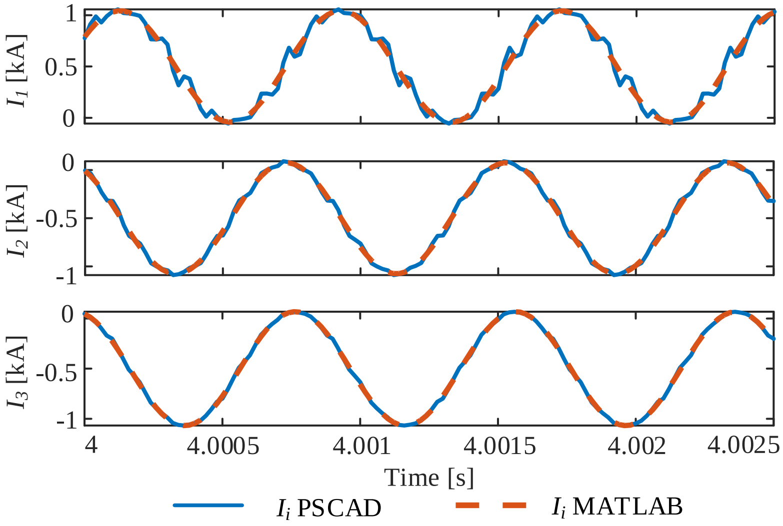

Figure 5-7: Comparison of AC waveform on I_i

Chapter 6 Conclusion and Future Work

6.1 Contributions and Conclusions

This thesis discussed a few problems related to a multiport dc hub including its control system, modeling, and simulation. The key contributions for this thesis are listed as follows:

1. Summarized the architecture and operation of a multiport dc hub;
2. Provided a detailed study on the steady state analysis of a three-port dc hub; in addition, this thesis performed a comprehensive harmonic analysis to a three-port dc hub under low switching frequency; it showed that low switching frequency can result in an error on the magnitudes of the fundamental components of the voltage at the output of the VSCs;
3. Based upon the existing closed loop control system for a two-port dc hub proposed, this thesis extended this control method to a multiport circuit. Meanwhile, the proposed control system was validated on a three-port dc hub in PSCAD/EMTDC simulation;
4. In accordance with the principle of dynamic phasors, this thesis proposed an average-value model of a multiport dc hub to reduce the computational cost of its simulation. Compared with the EMT simulation results, the averaged model with a large time-step showed high accuracy to emulate the *dq* components of operating signals in dc hub under both steady-state and dynamic operations. This validated

the benefits of the averaged model (high accuracy and computational efficiency) to study the operation and dynamic behaviors of dc hub. Additionally, an ac waveform recovery method was introduced for displaying high-resolution ac waveform, since averaged model is generally simulated with large time-steps.

In conclusion, firstly, this thesis reviewed the fundamental knowledge of HVDC transmission and concepts of dc grids. Besides, the topology of a multiport dc hub was studied in depth. Based on a survey of existing literature, no methods exists to demonstrate the control systems for a multiport dc hub. Thus, this thesis has provides a feasible solution to control a multiport dc hub, and the provided control diagram has been verified on a three-port dc hub in PSCAD/EMTDC simulation. Moreover, the proposed average-value model can significantly improve the simulation efficiency by giving allowance to use a large time-step. By testing the model in MATLAB, the simulation efficiency was shown to be improved to nearly 600 times faster than the simulation in PSCAD/EMTDC.

6.2 Future Work

This thesis focused on two problems: control and simulation of a multiport dc hub. The following suggestions are made mainly on the development of control and simulation of a dc hub in order to extend the work presented here:

1. The stability of this control system can be investigated. The control system alone with the power circuit can be written into a matrix form (linearized around an operating point) and the stability of the control system can be observed from the eigenvalues of this matrix.

2. The dc sides of this dc hub are considered as constant dc sources in this thesis. In the future work, dc sources need be replaced by real dc networks or transmission lines. It is important to perform system studies after connecting the dc hub into a power network.
3. Although the proposed model can provide adequate accuracy comparted with EMT simulation results, the harmonics cannot be presented by the proposed first-order dynamic phasor model. It is possible to increase the number of harmonics in the dynamic phasor model; therefore the simulation results from the dynamic model can become more realistic.

6.3 Publication

Part of the research work in this thesis has been accepted for publication in the International Conference on Power Systems Transients, 2019.

L. Liu, S. Filizadeh, X. Shi, and D. Jacobson, "Dynamic Modeling and Simulation of a Multiport DC Hub with Closed Loop Control," in *Proc. International Conference on Power Systems Transients (IPST), 2019.*

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