Fabrication of planar interdigitated electrodes for dielectric spectroscopy of thin films

by

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Abstract

The dielectric properties of polymeric thin films (100-200 nm thick) are hard to measure with the standard approaches as the samples aren't free standing necessitating a supporting substrate. Consequently, a planar interdigitated sample holder has been designed to hold the thin film where the polymeric capacitance was derived from the passing fringing fields.

The electrodes were fabricated by creating 120 nm trenches in a SiO_2/Si wafer; 20 nm Cr was deposited as an adhesion layer prior to the deposition of Cu by thermal evaporation. The electrical measurements were implemented using HP 4294A and a probe station.

Devices of 20 to 70 fingers were measured and the results were compared to the analytical and finite element simulation. At 10 KHz, the total measured capacitance of a typical 20-finger device was about 8 pF such that 3 % represented the polymeric contribution. The measurements differed from the calculations or finite modeling results by about 12%.

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List of Abbreviations

MUT	Material Under Test
PL	Parallel Line
IDC	Interdigitated capacitor
RF	Radio Frequency
MW	Microwave
OLED	Organic Light emitting diodes
PV	Photovoltaic cells
Q	Quality factor
PM	Perturbation method
SPR	Split post resonator
SMM	Scanning mircowave microscopy
TL	Transmission Lines
OCP	Open coaxial probes
CPL	Coplanar line
MSL	Microstrip lines
NSFL	Nano systems fabrication laboratory
Low-K	Relative permittivity ϵ_r (2.0 - 3.9)
VNA	Vector Network Analyzer
MOCVD	Metalorganic chemical vapor deposition

List of Symbols

$\epsilon_\circ$	Vacuum permittivity
ϵ_{SiO_2}	Relative permittivity of SiO_2
$\epsilon_{polymer}$	Relative permittivity of polymer
σ_{Si}	Conductivity of Silicon
μ	Mobility of the holes
$C_{substrate}$	Capacitance of the SiO_2/Si substrate
$C_{polymer}$	Capacitance of the polymer layer
C_{SiO_2}	Capacitance of the SiO_2 layer
$C_{elec-pad}$	Capacitance between the pad and the neighboring finger
C_p	Parallel capacitance
D	Dissipation factor
Z	Impedance of the fabricated IDC
θ°	Phase angle of the fabricated IDC
k_B	Boltzman Constant
$W_{depletion}$	Width of the depletion region
n_i	Intrinsic carrier concentration of Si at room temperature
N_a	hole concentration in the p-type wafer
ρ	Resistivity
T	Absolute temperature
q	charge of the electron
K	Elliptical integral of the 1st kind

List of Constants

$\epsilon_\circ$	$8.85\text{x}10^{-12} Fm^{-1}$
ϵ_{SiO_2}	4.2
$\epsilon_{polymer}$	2.2-2.7
σ_{Si}	$22.53\text{x}10^{3} Sm^{-1}$
q	$1.6\text{x}10^{-19} C$
n_i	$1.0\text{x}10^{10} cm^{-3}$
ρ_{Si}	$0.002{-}0.005 \Omega.cm$
ϵ_{Si}	11.7
μ_{Si}	0.05 m^2/Vs
T	300 Kelvin
k_B	$1.38\text{x}10^{-23} m^2 kg s^{-2} K^{-1}$
ρ_{SiO_2}	$10^{15} \Omega.cm$
$\rho_{polystyrene}$	$10^{14} \Omega.cm$
σ_{Cu}	$5.96\text{x}10^{7} Sm^{-1}$
μ_{Cu}	$1.26\text{x}10^{-6} Hm^{-1}$

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Publications / Conference talks

- **Peer-reviewed journal submission**

  - *Fabrication of an interdigitated sample holder for dielectric spectroscopy of thin films*, M. Shenouda and D.R. Oliver, submitted to Journal of Physics: Conference Series.

- **Conference presentations**

  1. *Dielectric spectroscopy of thin films using interdigitated planar electrodes*, M. Shenouda and D.R. Oliver presented at the International Conference on Optical, Optoelectronic and Photonic Materials and Applications (ICOOPMA14), Leeds, UK, July 27 - August 1, 2014 Paper 287.

  2. *Dielectric spectroscopy of thin films*, M. Shenouda and D.R. Oliver presented at 16th Canadian Semiconductor Science & Technology Conference, Thunder Bay, ON, Canada, August 12-16, 2013, Paper ThO11.

  3. *Dynamic polarization responses with spatial resolution less than a micrometer: dielectric spectroscopy with a scanning probe microscope*, D.R. Oliver, S. Asgari, M. Shenouda and M. Nadimi, presented at IoP Dielectrics 2013, University of Reading, Reading UK, April 10-12, 2013.

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to the innocent souls who paid their lives for starting a new phase of democracy and equality in Egypt

Chapter 1

Introduction

Dielectric spectroscopy is a nondestructive technique to estimate the dielectric properties of a material under test as a function of frequency. Applying an electric field polarizes the sample and results in the alignment of dipoles with the electric field direction. The relative permittivity is a complex quantity where, its real part is directly proportional to how easily the material polarizes in response to an applied electric field. The imaginary part of the permittivity represents the energy lost in the dielectric medium when the composed dipoles are aligned by the applied field in spite of the disruptions associated with thermal energy. Dielectric spectroscopy provides a data set from which these two components of permittivity which are material dependent can be estimated [1]. Such a measurement technique is useful in characterization of materials [2], serving applications like food processing and testing of high voltage power equipment [3].

The goal of this work is to design an appropriate sample holder for thin films (100-200 nm) to enable the measurement of their dielectric properties. The samples

of interest are polymeric films with low-k dielectric constants. The challenge is that thin films aren't free-standing samples, necessitating thick substrates as supports. However, the standard measurement approaches (*i.e.* transmission lines, resonant cavities) are more suitable for bulk samples [4]. This sample holder was achieved by fabricating electrodes on a substrate to form an interdigitated like capacitor (IDC), where the film could be spun coated on the whole ensemble afterwards. The fringing fields passing through the polymeric film constitute a capacitor from which its permittivity could be extracted. In polymers, the anticipated polarization mechanism is the orientational dipolar, whose loss tangent resonate in the radio range around 0.5-1 MHz [1]. Thus the electrical measurements lied in this frequency range.

The motivation of characterizing polymeric thin films stems from the great potential behind using them in applications like organic light emitting diodes (OLEDs) and photovoltaic cells (PV)[5]. Typically, membranes of a PV cell are nanometer thick to provide a short path for the generated electrons and holes to pass through. The transparency of such membranes reduces the recombination losses and improve the quantum efficiency. The low weight, cheap cost and mechanical flexibility are added reasons for adopting photovoltaic cells in the near future [6].

The designed sample holder in this project comprised of copper electrodes embedded in a thick substrate to make the substrate surface as leveled as possible ready for the thin film deposition. The electrodes were terminated with sufficiently wide pads allowing the placement of probes for capacitive measurements. The design also entailed a control structure, composed of two parallel electrodes embedded in the substrate, to predict the order of magnitude pertaining to the anticipated total ca-

pacitance. The choice of this parallel line structure in particular returned to the simplicity associated with derivation of a suitable analytical model which was next validated by a finite element simulation. However, the calculated total capacitance of the parallel line device was comparable to the surrounding noise in the probe station, compromising the measurement accuracy. Lengthening the electrodes would have been a solution to obtain a high total capacitance. In the meantime, it was important to preserve the uniformity of the film which would deteriorate with long lines. Consequently, the interdigitated structure was next introduced as a solution for achieving high total capacitance about 5 times that of the parallel line with equivalent lengths in addition to retaining the uniformity of thin film.

The process of constructing the interdigitated device demanded a theoretical model based on solving for the total capacitance of multilayered coplanar waveguide structure. The accuracy of the theoretical model was next validated by a finite element simulation. The choice of suitable dimensional ranges for fabrication satisfied that the finger width and spacing of the interdigitated device should be greater than 1 μm as this was the least limit for lithography resolution inside the clean room (NSFL). The final dimensions of the fabricated devices were selected upon maximizing the ratio $\frac{C_{polymer}}{C_{total}}$, where the C_{total} term included the contribution of the substrate, electrodes, pads and the polymeric film. The maximization of this ratio implicitly implied that the unwanted crosstalk between fingers should be minimized, while $C_{polymer}$ got amplified enough to be detectable by the impedance analyzer. Then, a fabrication process was developed, which was validated by a successive testing phase. Some preliminary electrical measurements were done with the fabricated test devices

to assess the closeness between the theoretical and the experimental values. Upon approving the results, a shadow mask was created to pattern the parallel line and interdigitated devices on a 4" wafer. In order to use the entire wafer area, the mask encompassed about 40 devices of varying size and finger count. The parameterized design was meant to examine the scalability of the polymer capacitance in response to the fingers' counts.

The electrical measurements were achieved by a HP impedance analyzer and a probe station. The estimation of $C_{polymer}$ was performed in a differential manner where the first measurement was taken with the device exposed to the air whereas the second one upon the deposition of the thin film. The recorded data were post-processed by MATLAB to estimate the dielectric constant of the polymeric film. The preparation of thin film took place at the Chemistry Department of the University of Manitoba.

1.1 Contributions

This thesis provides the design of an appropriate sample holder to carry thin films in the order of 100-200 nm. The sample holder functions for dielectric spectroscopy purposes. Although parallel plate holder is commonly used, it falls short for very slim samples due to the possible squeeze and damage of the film upon sandwiching between the plates. Therefore, the planar interdigitated design is introduced to hold the non-freestanding films in a non-destructive way. The specimen of interest were low-k polymers *i.e.* polystyrene or polycarbonate. The long range objective of this sample

holder is to study the dielectric properties of composite thin films like PEDOT:PSS with silicon microwires. Composite films are of potential use in the solar project that acts as a novel research based upon artificial photosynthesis [7].

In order to accomplish this design, a finite element modeling was implemented to predict the total capacitance of the interdigitated device. The accuracy of this model was verified by a precedent theoretical calculations. Eventually, the dimensions chosen based upon the mentioned techniques were utilized for fabrication inside the (NSFL).

This project succeeded in 3 different aspects:

- to develop a FEM with novel meshing method for solving structures whose features vary with 4-5 order of magnitude, which speed up the processing, rendering the solution convergent. This could be harvested for meshing sensor structures that might have cm dimensions with some fine features in the μm scale.
- to create a generic function in the mask plotting software by C++ code, that could draw the parallel line or interdigitated device with arbitrary dimensions, which proved to be an efficient solution for editions or enhancements. Writing generic codes for mask design could be invested in the future for designing sensors or actuators with multi repetitive patterns.
- to achieve a simple manual technique for pads' exposure upon the deposition of the thin film. This alleviated the necessity for an extra mechanical mask, offering a cost-effective solution without compromising the performance.

1.2 Thesis Arrangement

The second chapter of the thesis is a literature review. Previous techniques that involve permittivity measurement of bulk films are illustrated. In addition, the reasons behind the inapplicability of these techniques to the thin film measurement are mentioned. The discussion concludes with coplanar waveguide as an appropriate solution for the thin film sample holder. This is followed by a short overview of the analytical models of both the fabricated parallel line and interdigiated structures.

The third chapter talks about the experimental methods. This starts with a description of how the dimensions of the parallel line and interdigitated devices were chosen to maximize the ratio $\frac{C_{polymer}}{C_{total}}$ of their respective theoretical models. COMSOL simulations used to model the devices are discussed and the fabrication process is presented. Then, the measurement setup is shown and concluded by demonstrating the equipment used to verify the fabrication process.

The results and discussion is the topic of the fourth chapter. The chapter starts with illustrating the setup for doing the capacitive and resistive measurements of the fabricated structures. The measurements taken encompass plots of the impedance (Z) versus the phase angle θ^o and parallel capacitance C_p versus dissipation factor (D). Then a comparison between the results of theoretical, finite element modeling and measurements for the fabricated parallel line devices take place in order to show how far the measurements approach the pre-designed calculations. This comparison is repeated for interdigitated devices with different finger counts. The chapter also mentions the reasons behind the uncertainty of the measurements and the drift of the experimental results from the calculations.

The last chapter mentions the conclusions from this project. This is followed by listing some recommendations that can be added for future work.

Chapter 2

Literature Review

2.1 Dielectric Characterization Techniques

Accurate dielectric measurements necessitate designing an appropriate sample holder for the applicable frequency range (radio frequency and/or microwave). Suitable modeling of the sample holder carrying the specimen is also another condition for reliable estimation of permittivity parameters [8]. Choosing a permittivity characterization method is based on [9]

- the applicable frequency band
- the properties of the sample, i.e isotropic , anistropic, etc
- the physical composition of sample, solid, liquid, thin film, etc

A common method of dielectric spectroscopy for bulk samples is carried out in a parallel plate fashion. The holder comprises 2 stationary metallic electrodes sandwiching the specimen. For the case of polymers, the electrodes could be evaporated on the

specimen [10]. Despite the simplicity of the parallel sample holder, it wasn't convenient for the nature of thin film. Such films are defined in terms of their thicknesses that vary from few nanometers to several micrometers [11]. The mechanical strength of thin films is a serious issue as the film might be collapsed with the parallel sample holder leading to undesired shorts between the electrodes [10]. Furthermore, the ability of the film to retain its character through a sample preparation process was also questionable. There were also other measurement methods convenient for bulk samples shown in figure 2.1. The measurement setup of the following methods can be classified as being broadband or resonant.

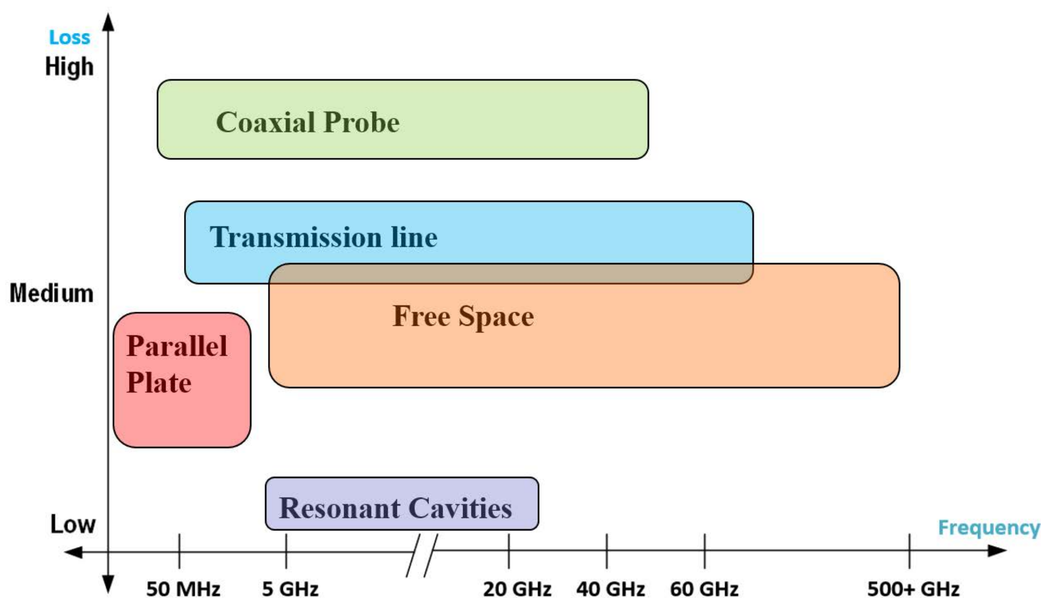


Figure 2.1: Measurement techniques for permittivity extraction. Each technique is specified in terms of dielectric losses and frequency range. Copyright permission granted [12].

2.1.1 Resonant Cavities

Resonant cavities provide very narrow bandwidth where the measurement can occur. These methods are more accurate than broadband methods for estimating the permittivity of materials in addition to simplicity of use and data collection. [13]

Figure 2.2 demonstrates a resonant cavity built upon the perturbation method. Such a method is a microwave measurement technique based upon that the electric field of the perturbed cavity due to the insertion of dielectric material or change of the geometric dimensions isn't significantly different from the unperturbed case. The cavity contains a a clearance hole at its center which specifies the location of maximum electric field.

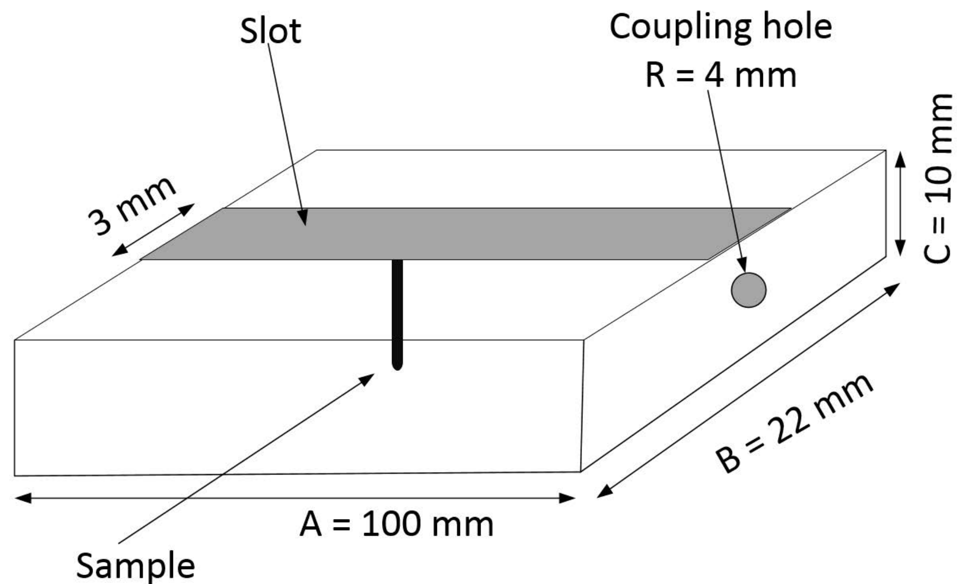


Figure 2.2: The setup for the perturbation method. The dimensions shown aren't into scale for the limitation of the drawing space. The sample is placed in the middle of the slot for permittivity measurement. The SMT connectors, supposedly on the outer edges of the cavity were excluded, to simplify the drawing. Copyright permission granted from [14].

A specimen of precise shaped rod should be situated at the center of the hole. A sharp rise of the $|S21|$ parameter at the resonant frequency is used to determine the dielectric properties of the cavity. Between an empty and loaded cavity, there will be a change in both the magnitude, width of the center frequency and quality factor. Such a change is a function of the permittivity of the material under test. The perturbation method is rejected within this work due to the involving preparation of the sample which would destroy the thin film. Furthermore, the tiny thickness of the thin film also won't produce a change sufficient enough to calculate the permittivity [14].

A Fabry Perot resonator consists of two spherical mirrors with equal curvature. The dielectric sample lies symmetrically at the center of the resonator [15].

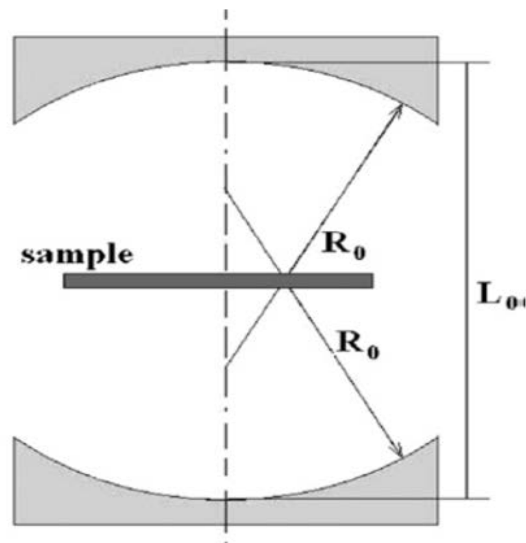


Figure 2.3: The setup for the fabry perot method. The sample is placed between two spherical mirros with equal curvature. Copyright permission granted from [13].

This resonator usually functions in the milli-meter frequency band with a very

high Q factor between 100,000 to 200,000. The insertion of the sample changes the optical length, which could be taken to determine the permittivity. Likewise, the loss factor could be extracted from the Q factor measurements of both the empty and loaded resonator. TEM_{00} is the operating mode in the resonator. Analytically, this mode can be approximated by the gaussian beam. TEM_{00} enables accurate permittivity measurements when the sample is almost equal to half of the incident wavelength. Larger samples size are favored for containing nearly all the beam energy to reduce the losses resulted from the edge diffraction. Clearly, the large sample size and complex preparation aren't suitable for thin films [16].

The test fixture of split post resonator demonstrated in figure 2.4 is formed of 2 parallel faces where the sample is placed on the bottom one. The operating frequency range is between 1 to 10 GHz, where the measurement frequency is a function of sample thickness and relative permittivity. The larger the sample size or the higher the permittivity, the lower is the tuning frequency of the resonator. By taking two consecutive measurements of empty and loaded resonator, there will be a change in the frequency of the resonator and its quality factor. The permittivity of the sample is a function of this change.

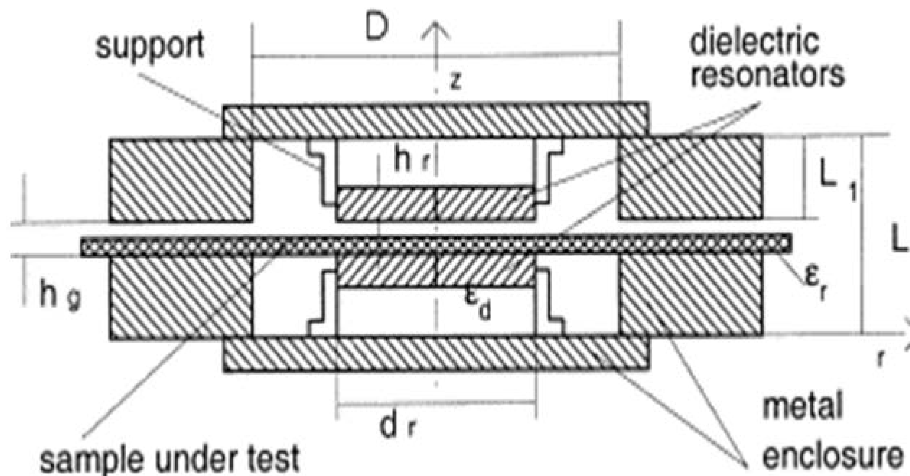


Figure 2.4: Schematic diagram of the split post resonator. h_g was the height of the air gap, while ϵ_r was the permittivity of the sample under test. The image was granted as a courtesy of [17]

This technique surpasses the perturbation method, as the sample needn't be precisely shaped. Additionally, the permittivity measurements aren't sensitive to the existing air gap between the resonator faces, which simplifies the setup. For a noticeable frequency shift within the operating range, the film thickness should be 1 μm or above. As a result, this method wasn't recommended due to the thickness limit that exceeds that of thin films within this work. [18]

Scanning microwave microscopy is a resonator comprised of a sharp tip that can raster-scan the surface. The technique lies in the microwave range for permittivity characterization of materials with high spatial resolution. When the tip is positioned close to the sample, a shift in the center frequency and the quality factor of the resonator occurs. Then, the permittivity of the sample can be described in terms of such a shift. However, this method isn't convenient for low-k samples, because the

small dielectric constants (2.0 - 2.7) won't induce a noticeable frequency shift that can be practically measured [19]. Additionally, the polymeric thin films exhibit naturally pores that could trap the tip, distorting the quality of the resulted image [20].

2.1.2 Transmission line

These are broadband methods widely used for determining the permittivity of materials. Among this family are the coaxial cable, mircostrip, strip lines and coplanar waveguides [4].

A coaxial line technique works by preparing the sample in an annular shape to fit inside a coaxial cable. The dielectric constant can be calculated from the measured S-parameters and characteristic impedance.

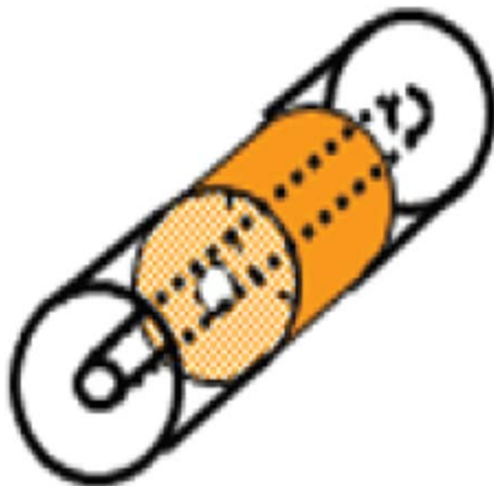


Figure 2.5: The sample was prepared in an annular shape to fit inside a coaxial probe. The image was granted as a courtesy of [21]

The sample must fill entirely the coaxial cable to mitigate the air gap effect which

deteriorates the accuracy of measurements. The necessary precise preparation of the sample could destroy the films of (100 - 200) nm thick [21].

An open coaxial probe is a broadband technique, suitable for the dielectric characterization of liquids and soft samples. The test fixture has a planar side that faces the sample whereas the other side is the measuring probe. The measured reflection coefficient is used to solve for the permittivity of the specimen. This method is widely adopted, due to the flexibility of using one probe only for measurements. As opposed to the coaxial line technique, the material under test doesn't necessitate precise preparation. However, this method requires bulky specimen to produce a good quality reflected wave, making it unsuitable for thin film specimen. [22]

Short-circuit reflection is a method where the sample terminates the center conductor of a shorted transmission line. The specimen should be prepared in the form of a circular disc, whose diameter fits exactly that of the center conductor. This setup treats the specimen as a circular parallel plate capacitor. The permittivity can be extracted from the measured scattering parameters. The complex requirement for sample preparation and measurement setup might damage the targeted thin films of this work. [23]

The Free space method shown in Figure 2.6 is suitable for non-homogeneous dielectric materials or testing samples in special conditions like high temperature. The sample is placed between a transmitting and receiving antennas where, both connected to a de-embedded vector network analyzer (VNA). De-embedding is a mathematical model of the test fixture, whose effect is automatically subtracted by the analyzer from the overall measurement to give an accurate estimation of the

specimen only [24]. Consequently, the measured S-parameters of the sample under test could be extracted to solve for the permittivity constant.

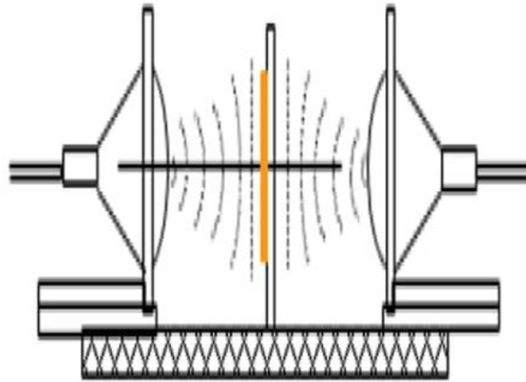


Figure 2.6: The sample was prepared in an annular shape to fit inside a coaxial probe. The image was granted as a courtesy of [21]

Accurate measurements condition that the sample size should be larger than the incident wavelength to give a good reflected wave, otherwise, the reflected responses are weak insufficient to extract the S-parameters. Had this method been utilized, the tiny size of devices within this work on the order of 5 mm x 0.75 mm, would fail the permittivity measurements [25].

In microstrip line-based approaches, the material under test is incorporated into the structure surrounding the microstrip line. The presence of the material changes the propagation and attenuation constants of the transmission line which, in turn, enables the extraction of the dielectric characteristics of the material under test. The isolation of the capacitance and conductance of the sample from those of the microstrip line necessitates 2 measurements. The first measurement is for the propa-

gation constant and the characteristic impedance of the microstrip line, followed by the those of whole ensemble (mircostrip line + thin film). Then, the extracted capacitance of the sample as well as the physical dimensions of the line are the parameters used to solve for the permittivity. The sample preparation necessitates depositing a metallic conductor on the sample which would damage the thin films within this work. Besides, the resistive losses due to the metallic conductor are greater than the dielectric losses of the thin film, compromising the measurement sensitivity. [26]

Coplanar waveguide transmission lines are simple to integrate with external circuits exhibiting less dispersion at high frequencies compared to other transmission lines. By depositing thin film on the coplanar structure, the permittivity measurements can be taken in a non-destructive manner meaning that the quality of the film could be maintained without damage. Additionally, there's no limitation of how tiny the thickness of the sample is. Due to such benefits, the design of the parallel line and interdigiated devices in this work was based on coplanar multi-layered structures. The following discussion will introduce the theoretical models for the above mentioned devices. [27]

2.2 Modeling of the Fabricated Structures

2.2.1 Parallel line capacitor

As previously introduced, the parallel line device acted as a control element to benchmark the measured capacitance against the theoretical calculations and finite element simulation. The relative simplicity of its analytical model comes from the

ability to segment this device into components whose capacitance can be calculated by quick models *i.e* parallel plate rule or equivalent. Furthermore, the simple geometry of the device was adequate as a first step for finite element modeling. The following discussion will demonstrate the theoretical modeling of such a structure shown in figure 2.7.

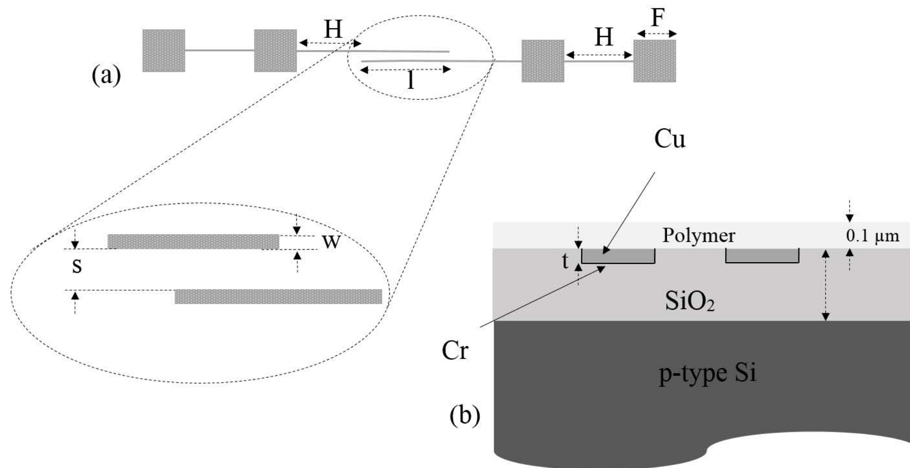


Figure 2.7: a) The plane view comprising 2 parallel lines with length l, width w and spacing s. b) Cross section view of the embedded electrodes, where the thickness of the p-type Si was about $500\mu m$

Since the impedance analyzer measured the total capacitance of the fabricated parallel device, it was important to analytically quantify the order of magnitude of this device's capacitance for comparing the measurements against the calculations.

The total capacitance of the parallel line device could be divided into 5 sub types C_{elec}, $C_{elec-pad}$, C_{Si} , $C_{polymer}$ and $C_{substrate}$.

The first type is the capacitance between the two parallel lines depicted in the

plan view of figure 2.7 defined by

$$C_{elec} = \frac{lt}{s}. \tag{2.1}$$

Likewise, the capacitance between the parallel lines and the neighboring pads was approximated by

$$C_{elec-pad} = 2\frac{wt}{H}. \tag{2.2}$$

The fringing fields inside the p-type Si could be modeled by a circular arc given by eq. (2.3), assuming that the thickness of the Si substrate extended to infinity in order to simplify the model [28]

$$C_{Si} = \frac{\epsilon_\circ \epsilon_{Si}}{\pi} \ln\left(1 + \frac{2w}{s}\right) l. \tag{2.3}$$

The same relation was utilized to estimate the fringing fields inside the polymer layer by substituting the permittivity of Si with that of the polymer

$$C_{polymer} = \frac{\epsilon_\circ \epsilon_{polymer}}{\pi} \ln\left(1 + \frac{2w}{s}\right) l. \tag{2.4}$$

The capacitance of the substrate was the series equivalent of C_{SiO_2} and $C_{depletion}$ [29]. The former referred to the contribution of the SiO_2 layer, while the latter expressed the effect of the depletion layer in the p-type Si resulting from applying a positive voltage (50 mV) to the electrodes. Both capacitances can be approximated

by the parallel plate rule as demonstrated in eq. (2.5) - (2.7)

$$C_{SiO_2} = \epsilon_\circ \epsilon_{SiO_2} \frac{lw}{h_{SiO_2}} \tag{2.5}$$

$$C_{depletion} = \epsilon_\circ \epsilon_{Si} \frac{lw}{W_{depletion}} \tag{2.6}$$

$$C_{substrate} = C_{h_{SiO_2}} \parallel C_{depletion}. \tag{2.7}$$

The width of the depletion layer $W_{depletion}$ was determined by the following discussion, where q is the electron charge = $1.6 * 10^{-19}C$, n_i [30] is the intrinsic hole concentration of Si at room temperature = $1.0 * 10^{10}cm^{-3}$ and N_a is the hole concentration of p-type wafer as estimated from its resistivity $\rho = 0.002 - 0.005\Omega.cm$.

Assuming the resistivity equal to $\rho = 0.0035\Omega.cm$, the hole concentration was calculated to be $3.96 * 10^{18}cm^{-3}$ by eq. (2.8)

$$N_a = \frac{1}{qn\mu_{hole}}. \tag{2.8}$$

Eq. (2.9) determines the depletion layer width where the hole mobility is 0.05 m^2/Vs [30], T is the absolute temperature = 300 K and ϵ_{Si} is equal to 11.7

$$W_{depletion} = \sqrt{\frac{4\epsilon_{Si}KT}{q^2 N_a} \ln\left(\frac{N_a}{n_i}\right)}. \tag{2.9}$$

Since all the mentioned capacitance terms were in parallel, C_{total} could be calcu-

lated eq. (2.10)

$$C_{total} = C_{elec} + C_{elec-pad} + C_{Si} + C_{substrate} + C_{polymer}. \tag{2.10}$$

2.2.2 Interdigitated capacitor

The interdigitated structure is a variant of coplanar lines chosen to increase the electromagnetic interaction between the fingers, which improves the sensitivity of the capacitance measurements [31]. The composition of such a structure is shown in figure 2.8. The electric field between the fingers isn't uniform, but elliptical shape. Giovanni et al [32], attained a closed form formula for this structure using conformal mapping to convert the elliptical shaped fringing fields inside the polymer and the substrate into the parallel plate equivalent [33].

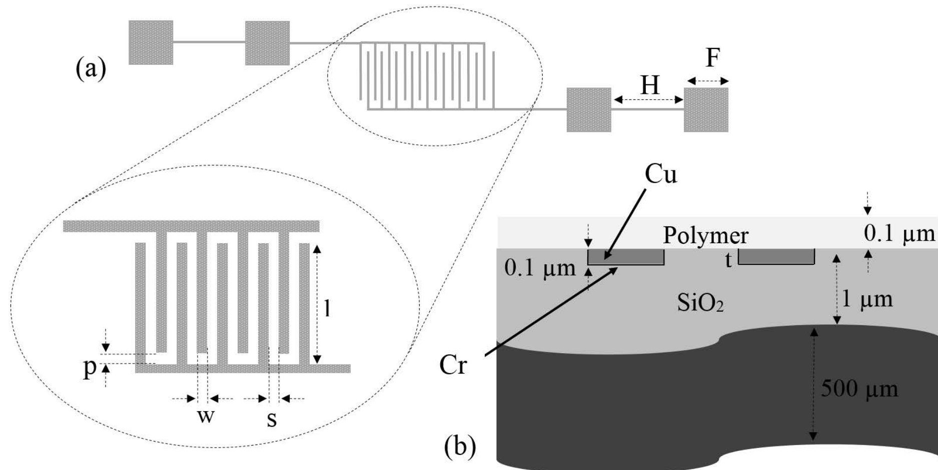


Figure 2.8: a)Planar view of the device showing the arrangement of the electrodes and the contact pads. b) Cross-section view of the embedded electrodes. The thickness of the p-type silicon wafer was on the order of 500 μm. The chromium diffusion barrier surrounding the metal electrode was indicated as the interfaces with the SiO_2 layer.

The complex capacitance $C^*_{substrate}$ associated with the fringing capacitance contribution due to the SiO_2/Si substrate is given by eq. (2.11)

$$C^*_{substrate} = \frac{N-1}{2}\frac{1}{\left[\frac{1}{\epsilon_{SiO_2}C(h_{SiO_2})} + \frac{1}{\epsilon^*_{Si}}\left(\frac{1}{C(\infty)} - \frac{1}{C(h_{SiO_2})}\right)\right]} \tag{2.11}$$

The complex term was necessary to account the dependency of the fringing fields inside the substrate on the conductivity of the Si which appeared in the imaginary part of eq. (2.12). The term ϵ^*_{Si} calculated the Si permittivity at an arbitrary frequency where, σ_{Si} was the conductivity of the substrate wafer equal to 28.57x$10^3 S/m$ and N was the number of fingers [34]

$$\epsilon^*_{Si} = \epsilon_{Si} - i\frac{\sigma_{Si}}{\omega\epsilon_\circ}. \tag{2.12}$$

ω was the radial frequency given by eq. (2.13)

$$\omega = 2\pi f. \tag{2.13}$$

$C(h_{SiO_2})$ defined in eq. (2.14) was the capacitance contribution of the SiO_2 layer, where K is the elliptical integral of the 1st kind [34]

$$C(h_{SiO_2}) = 2\epsilon_o\frac{K(k)}{K(k')}l. \tag{2.14}$$

k and k′ in eq. (2.15) and (2.16) referred to the elliptic and complementary

moduli repectively

$$k = \frac{\tanh \frac{\pi w}{4h_{SiO_2}}}{\tanh \frac{\pi(w+2s)}{4h_{SiO_2}}} \tag{2.15}$$

$$k' = \sqrt{1 - k^2}. \tag{2.16}$$

$C(\infty)$ in eq. (2.17) referred to the capacitance of the infinite air layer defined by the following equation [35]

$$C(\infty) = 2\epsilon_0 \frac{K(k_\infty)}{K(k'_\infty)} l \tag{2.17}$$

$$k_\infty = \sin\left(\frac{w}{w+2s}\right) \tag{2.18}$$

$$k'_\infty = \sqrt{1 - k_\infty^2}. \tag{2.19}$$

Likewise, the contribution of the polymeric layer could be calculated eq. (2.20) [36]. $\epsilon_{polymer}$ was taken as 2.4 equivalent to the permittivity of the polystyrene, used as the coating material of the thin films within this work

$$C_{polymer} = (N-1)\epsilon_o \epsilon_{polymer} \frac{K(k_{polymer})}{K'(k_{polymer})} l \tag{2.20}$$

$$k_{polymer} = \frac{\sinh \frac{\pi w}{4h_{polymer}}}{\sinh \frac{\pi(w+2s)}{4h_{polymer}}} \tag{2.21}$$

$$k'_{polymer} = \sqrt{1 - k_{polymer}^2}. \tag{2.22}$$

C_{elec} expressed the capacitance of the electrodes while $C_{elec-pad}$ represented the

capacitance between the finger and the neighboring pad. Both capacitances were estimated by the parallel plate rule as concluded in eq. (2.23) - (2.24)

$$C_{elec} = (2N-1)\epsilon_0 \epsilon_{SiO_2} \frac{lt}{s} \tag{2.23}$$

$$C_{elec-pad} \approx 2\epsilon_0 \epsilon_{SiO_2} \frac{lt}{H}. \tag{2.24}$$

Because the capacitance terms in (2.11), (2.17), (2.23), (2.24) and (2.20) were in parallel, the overall capacitance was the summation of them. $\Re$ is meant the real part of $C^*_{substrate}$ referring to the measurable quantity of $C^*_{substrate}$ regardless of the substrate losses

$$C_{total} = \Re\left(C^*_{substrate}\right) + C_{elec} + C_{polymer} + C_{elec-pad}. \tag{2.25}$$

Chapter 3

Experimental

3.1 Introduction

The theoretical models of the parallel line and interdigitated devices were the initial step towards their implementation. Continuing this path, this chapter provides in-depth discussion of the fabrication process. The ratio $\frac{C_{polymer}}{C_{total}}$ was the figure of merit for the design upon which, the geometric parameters were chosen and ultimately utilized for fabrication.

3.2 Dimensions of the parallel line device

The design's figure of merit is maximized by raising the $C_{polymer}$ as well as reducing the effect of C_{elec} and $C_{elec-pad}$ terms. This was performed by writing MATLAB scripts for the closed form theoretical models, where the range of each parameter in the design was defined. One simulation goal was to determine the collection of

dimensions leading to the highest $\frac{C_{polymer}}{C_{total}}$ as demonstrated in table 3.1.

Table 3.1: The chosen dimensions of the parallel line device and the reasons behind each parameter.

Parameter	Range	Chosen dimension	Reason
F	N/A	200 μm	To provide sufficient room for placing the probes during the measurement.
H	N/A	500 μm	This spacing was enough to decrease the unwanted coupling between the electrodes and the pads.
L	3000-5000 μm	5000 μm	Increasing the length of the electrodes increased the fringing fields inside the polymer rising $C_{polymer}$.
t	100-300 nm	100 nm	Decreasing the thickness of the electrodes decreased the undesired crosstalk between the electrodes C_{elec}.
w	20-50 μm	50 μm	Increasing the width of the electrodes increased the fringing fields inside the polymer rising $C_{polymer}$.
s	100-200 μm	200 μm	Increasing the spacing between the electrodes reduced their unwanted coupling reducing C_{elec}.

3.3 Dimensions of the interdigitated device

Based upon the $\frac{C_{polymer}}{C_{total}}$ ratio, other MATLAB scripts were written to select the dimensions of the interdigitated counterpart. The results of the numeric calculations were displayed in the following table.

Table 3.2: The chosen dimensions of the interdigitated device and the reasons behind each parameter.

Parameter	Range	Chosen dimension	Reason
F	N/A	200 μm	To provide sufficient room for placing the probes during the measurement.
H	N/A	500 μm	This spacing was enough to decrease the un-wanted coupling between the electrodes and the pads $C_{elec-pad}$.
w, p	20:50 μm	50 μm	Increasing the width of the electrodes increased the fringing fields inside the polymer rising $C_{polymer}$.
s	20:50μm	50 μm	Increasing the spacing between the electrodes decreased the undesired coupling between the electrodes C_{elec}.
l	300:500μm	500 μm	Increasing the length of the electrodes increased the fringing fields inside the polymer rising $C_{polymer}$.
t	100:300 nm	100 nm	Decreasing the thickness of the electrodes decreased their undesired crosstalk.

3.4 COMSOL Modeling

The theoretical calculations were verified by finite element modeling. COMSOL was the software chosen for such a modeling. The package included an *Electric Current EC* module that enabled the use of scalar voltage to solve a current conservation problem [37]. The capacitance extraction was implemented for the parallel line and interdigitated devices by solving the Laplacian $\nabla^2\phi = 0$ [38]. A frequency domain

study was done to determine the capacitance of the respective devices at any arbitrary frequency in the desired range (40 Hz − 110 MHz).

The simulation was accomplished in the following consecutive steps. First, a 3D shape was constructed to match the geometrical architecture of some device *i.e* interdigitated device. This was followed by choosing different materials required for building the structure. For instance, copper was selected as the candidate material of the electrodes. Solving the model necessitated assigning proper governing equations as well as appropriate boundary equations.

For instance, the total electric charge (Q) C on the modeled structure can be evaluated from the divergence of the current density (J) A/m^2 as given in eq. (3.1)

$$\nabla.\mathbf{J} = \mathbf{Q}. \tag{3.1}$$

The first source of the generated charges were those produced by the applied electric field (E) as demonstrated in eq. (3.2), where σ referred to the conductivity of the material while, (J_e) was the external current density. Furthermore, the polarization of the dielectric medium as a function of frequency contributed to the total charges in eq. (3.2) where, ω defined the radial frequency

$$\mathbf{J} = \sigma\mathbf{E} + \mathbf{J_e} + \omega\epsilon_{\mathbf{o}}\epsilon_{\mathbf{r}}\mathbf{E}. \tag{3.2}$$

The electric field resulted from the gradient of the applied voltage as in eq. (3.3). The applied voltage quantified to be 50 mV on the live conductors and 0 mV on the ground portion as shown in figure 3.1

$$\mathbf{E} = -\nabla \mathbf{V} \tag{3.3}$$

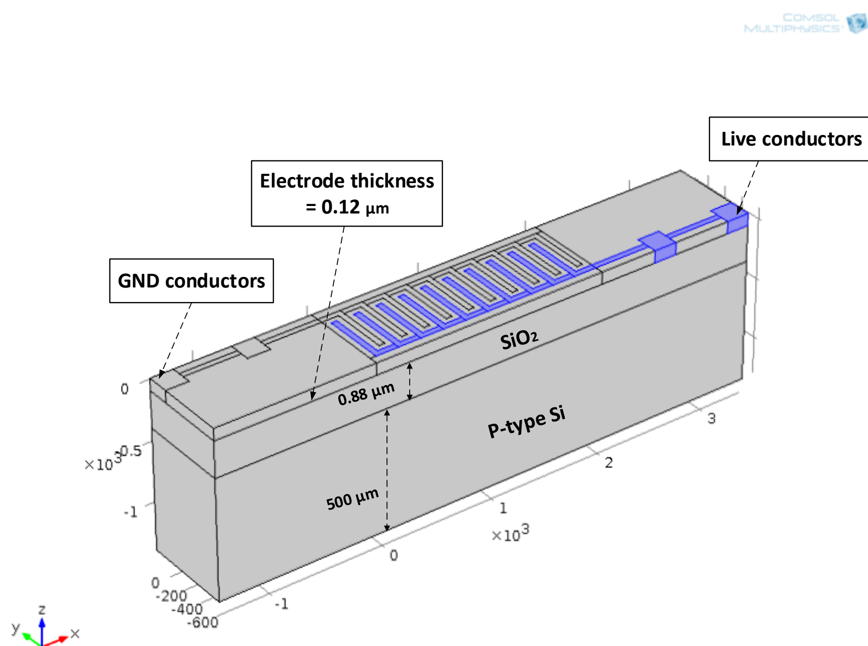


Figure 3.1: 3d view of the finite element model of the interdigitated device. The dimensions aren't scaled but magnified for illustration purposes. The live conductors had a 50 mV, while the GND electrodes had 0 volts. The electrode thickness were about 120 nm embedded in a 1 μm SiO_2.

Since no current flowed from the electrodes to the substrate comprised the SiO_2 and p-type Si layers, the proper boundary condition was that defined in eq. (3.4), which meant that the normal component of the current density across the structure was equal to zero

$$\mathbf{n.J} = \mathbf{0}. \tag{3.4}$$

For the meshing to converge, the meshing step should typically be about quarter of the smallest dimension in the simulated model. Given, the tiny thickness of electrodes in the order of 100 nm, this implied that the appropriate meshing step should be about 25 nm. However, meshing a thick substrate of (500 μm) would take forever if this meshing step was utilized. Therefore, the solution was to segment the whole model into different layers and selecting an appropriate meshing step for each layer. Following this logic, a 25 nm step was a suitable candidate for the electrodes and the polymeric layer, while 50 μm was favored for the substrate. This segmentation technique attained its results, rendering the meshing convergent with a net simulation time of 7-10 minutes on a Mac pro desktop computer with 120GB RAM and 2.4 GHz 8 core processor.

3.5 Fabrication Process

The fabrication flow shown in figure 3.2 was required to be within the capabilities of the clean room at the University of Manitoba, for instance the minimum features that can be resolved by lithography should be greater than 1 μm. Fortunately, all the dimensions for the above-mentioned devices are larger than this limit. A test phase preceded the creation of the mask to check the validity of proposed fabrication process. This was initiated by choosing an older mask with devices of comparable features to the targeted ones in this work. Upon ascertaining the success of the fabrication flow, a specific mask containing multiple devices was created using *L-Edit* [39]. The mask design considered some guidelines like the existence of parallel

line lines with different lengths. These devices acted as benchmarks to assess the closeness between the results derived from calculations or fintite element modeling and the measurements. Additionally, the mask must include some test devices to probe the resistivity of the deposited copper upon thermal evaporation using the 4 point probe method.

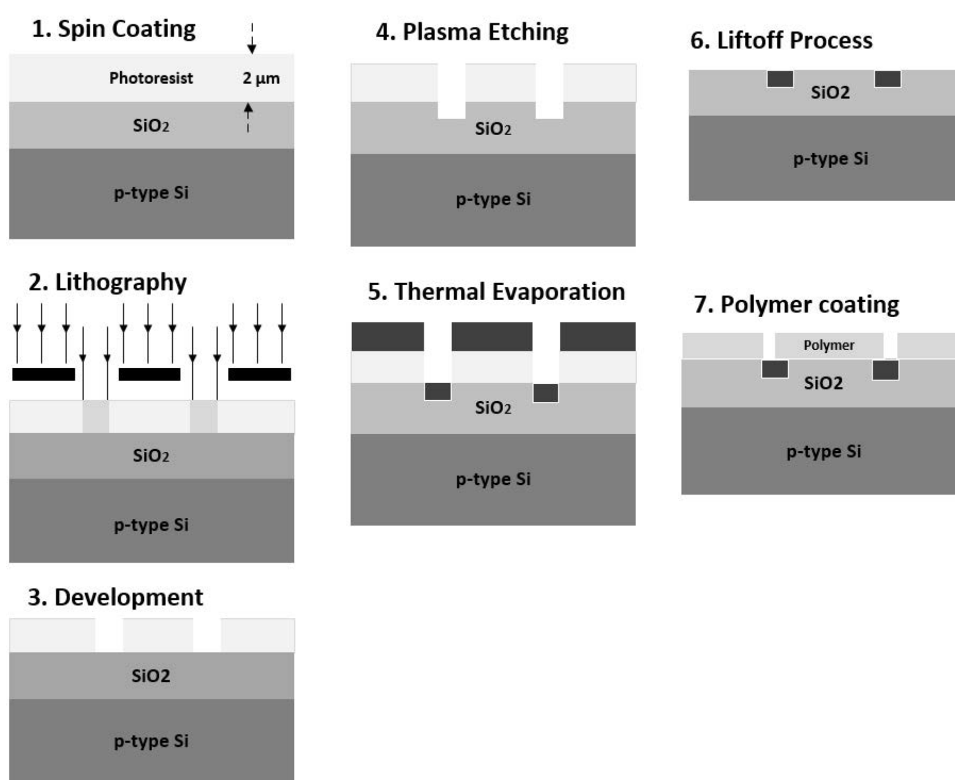


Figure 3.2: The steps of the fabrication process in order. The chosen photoresist was HPR504. The gases used in plasma etching were 45 sccm CF_4 + 5 sccm O_2. The metallization was achieved by thermal evaporation, where 20 nm Cr adhesion layer was deposited before the Cu layer. In the 7th step, the polymer was half filling the electrodes underneath to indicate the partial removal of the polymeric layer by a cotton swap to expose the electrodes for capacitance measurements.

First a [100] 4$''$ SiO_2/p-Si wafer was chosen for the fabrication. The high resistivity

of the SiO_2 $(10^{16}\Omega.cm)$ [40] was mandatory to guard against the leakage of the Cu electrodes that could have happened if the substrate had been only p-type Si. In the lithography step, the exposed regions were ultimately the locations of the electrodes. Such a patterning could be achieved either by creating a negative mask with a positive photoresist or a positive mask with a negative photoresist. The first option was favored for creating the mask. The layer of the photoresist (HPR 504) was chosen to be the thickest possible to stand the few damage that might happen during the etching process. The complete recipe of every step is mentioned fully in Appendix A.

In the literature, wet or plasma etching could be used for creating the trenches in SiO_2 [41]. In this work, plasma etching was preferred as it was a controllable process resulting in 20 nm/min etching rate. This was chosen instead of the wet etching process resulted typically in an etch rate of 200 nm/min [42]. The pressure set and the reactive ion power were chosen to be 200 mTorr and 300 W respectively. The latter parameters guaranteed the etching to be slow with low radiation damage, which was a necessity for smoother trenches.

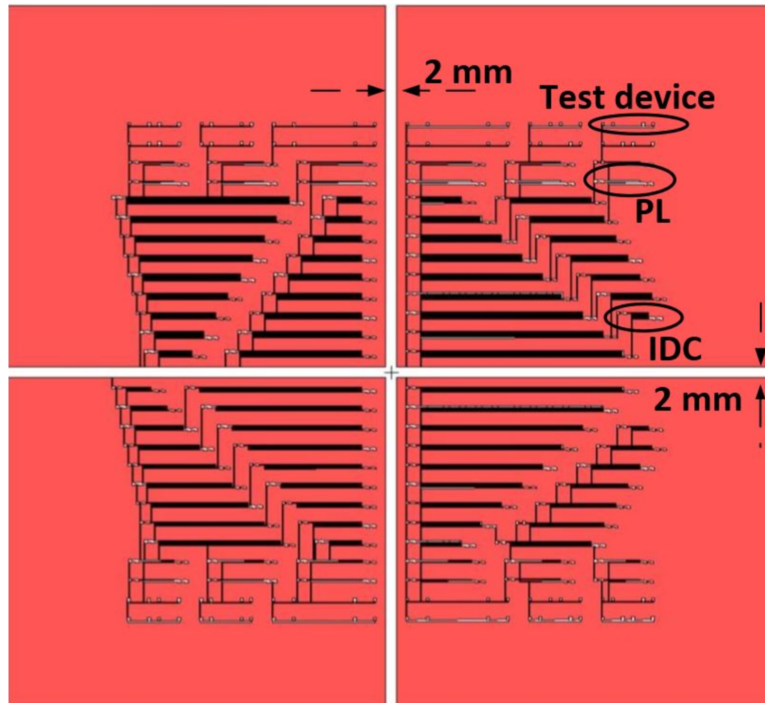
Since the desired electrode thickness was on the order of 100 nm, the deposition process must be controllable. This mandated the deposition rate had to be around 10-20 nm/min so that full deposition took 4-5 minutes to finish. Thermal evaporation was the best candidate for the electrode metallization as it had evaporation rates of 10 nm/min. In contrast, the rates expected from a similar process like electroplating was about 10 μm/min [43]. Before evaporating the copper layer, about 20 nm chromium was deposited as a adhesion layer for sticking the copper to the SiO_2 [43]. In addition. the chromium layer guarded against the diffusion of deposited copper in the p-type

substrate [43].

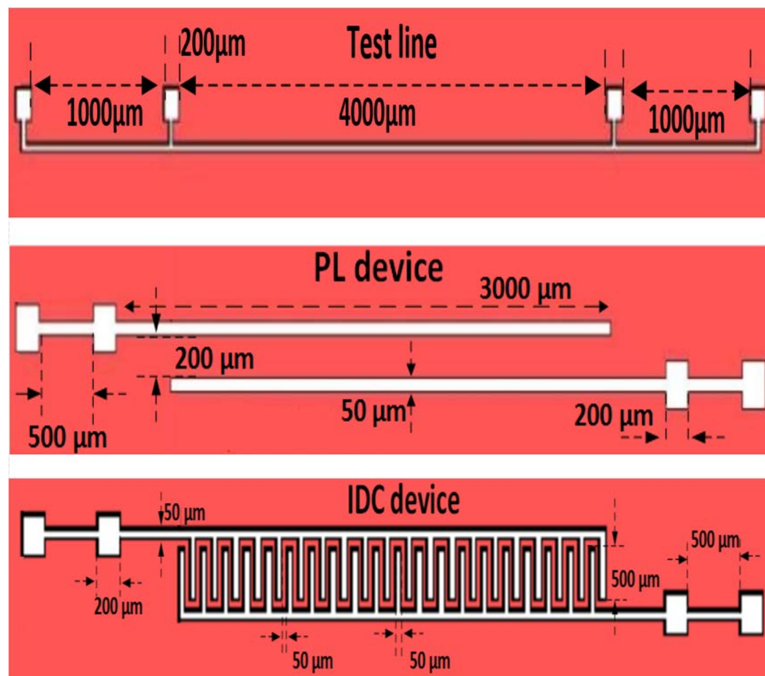
One other merit about thermal evaporation was its poor sidewall coverage [43], which ultimately allowed the removal of the photoresist by liftoff process. The photoresist was dissolved in an ultrasonic bath containing acetone (30 minutes agitation). Remnants of the photoresist were removed by wiping the fabricated structure with a cotton swap.

3.5.1 Mask description

There were some design considerations about the mask. First, the mask was a negative tone or chromium dominated. Chromium is a dark material that impedes the visibility of the wafer underneath. Consequently, there must be windows on the mask to see the wafer and fix the alignment of the mask with that of the wafer. In the meantime, there had to be an alignment mark that can be viewed by the eyepieces of the microscope. A crosshair mark lying in the middle of the wafer was taken as both a window and an alignment mark. As shown in figure 3.3, the crosshair divided the wafer into 4 identical compartments. The width of the crosshair was 2 mm, wide enough as a window size without compromising too much the remaining space of the wafer. This width was also chosen to provide sufficient room for cutting the wafer using the saw, in case a single compartment needed to be tested only. Testing one compartment at a time saved the resources during the testing phase.



(a)



(b)

Figure 3.3: a) Complete mask picture with a crosshair in its middle, the width of the crosshair was 2mm b) The 3 magnified devices: test, parallel line and interdigitated devices with the shown dimensions.

Due to the nature of parallel line devices as control elements, nearly 90% of the mask space was dominated by interdigitated capacitors. The mask design was also parameterized. The intent of the parameterized design was to examine the scalability of $C_{polymer}$ with the devices area. The selected width and spacing (w,s) of the electrodes were 20, 30, 40 and 50 μm. This range was sufficient to provide measurable $C_{polymer}$ by the impedance analyzer and guaranteed the void of unwanted shorts between the electrodes. The possibility of such shorts returned to fabrication mistakes that might occur during lithography or deposition. The length of the electrodes were 300 and 500 μm. The electrodes were long enough to provide high C_{total} term and include as many devices on the available wafer area. The finger count for the devices was 10 to 100 with a step of 10 fingers to detect a noticeable capacitance change ΔC between two successive devices.

The coupling between the multiple devices on the mask introduced parasitics, that could have distorted the capacitance contributions of each device. As a result, the devices was positioned far apart from one another on the layout to reduce their unwanted coupling.

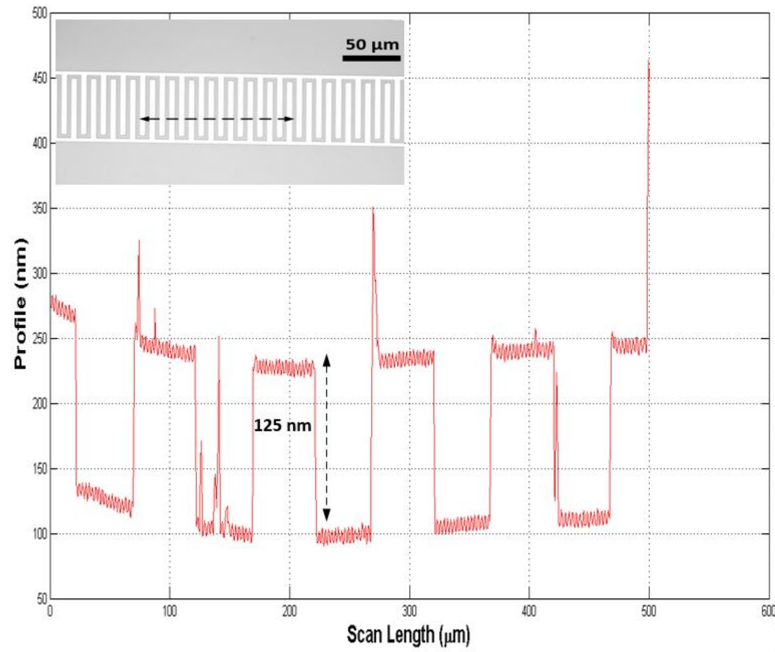
The chosen separation in the horizontal and vertical directions was 2 mm. The parallel plate rule was utilized to roughly estimate the order of magnitude of such parasitics. The coupling between two devices with an average length = 12 mm, average width = 1 mm and thickness = 100 nm was about 15fF. The order of capacitance for the parallel line and interdigitated devices was in the pF range which exceeded the parasitic range by 3 orders of magnitude. Consequently, the coupling parasitics could be ignored relative to C_{total} for all practical purposes.

As shown in figure 3.3, the larger devices of 100 fingers count positioned close to the crosshair, while devices with fewer fingers situated near the rim of the wafer.

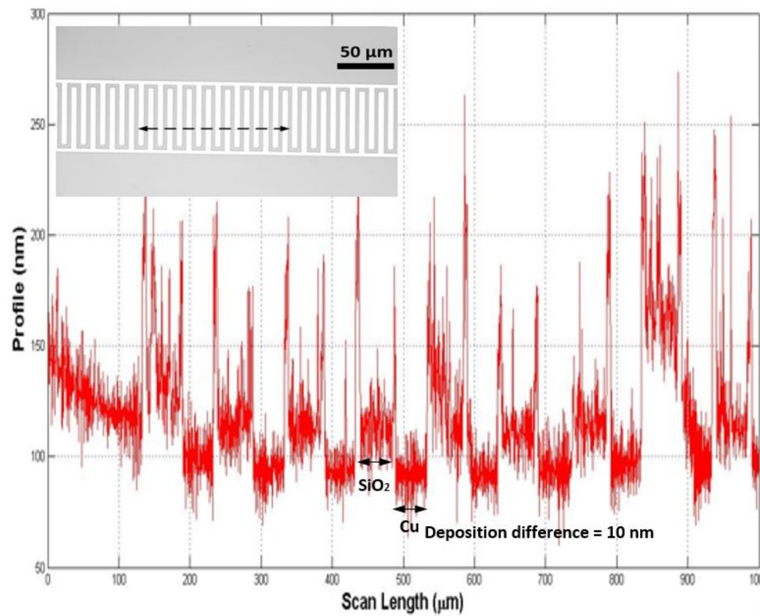
3.6 Fabrication validation

There were measurements occurred for fabrication intermediate steps to check the validity of the process in meeting the expected results. *A KLA Tencor AS-500 Alpha-Step Profilometer* was used for surface relief measurements to ascertain the electrode trench etch depth and spin coated polymer thickness. The thickness of the copper and the SiO_2 was confirmed using a *Veeco DI3100* and a *Nanoscope IV* controller operating in contact atomic force microscopy mode (AFM). Figure 3.4(a) shows the plasma etching results of some interdigitated sample. The etching results were in agreement with the required trench depth (120 nm). Figure 3.4(b), shows the deposition results of the thermal evaporation. The slight difference (10 nm) between SiO_2 layer and the deposited copper implied the controllability of the thermal evaporation process.

The apparent measurement "noise" in Figure 3.4(b) may be attributed to the size of the profilometer needle (large compared to the trench size being measured). This observation was confirmed via AFM measurements.



(a)



(b)

Figure 3.4: The etching results of some sample, where the scanned sample was shown in the inset. The grey and white color indicated the SiO_2 layer and the etched trenches respectively. b) The deposition results for the same sample, where the difference between the Cu and the SiO_2 layer was about 10 nm.

It was also important to quantify the fabrication errors resulted namely from the etching and deposition processes. Given that, the trench depth of the electrodes was assumed during calculations and finite modeling as 120 nm. However, the measured trench depth across the wafer wasn't constant but varied within 10-15 nm. This returned to non-uniformity of plasma inside the etching chamber. Likewise, the deposited copper electrodes by thermal evaporation were fluctuating within 10 nm. Consequently, the uncertainty of the finger depth reached about 20-25 nm, corresponding to a difference of about 10 % between the measurements in comparison to both the analytical and FEM models. The discrepancy between the actual and targeted dimensions due to fabrication were summarized in table 3.3

Table 3.3: The actual and target dimensions of fabrication with the induced measurement errors.

Parameter	Target dimension	Actual measurement
F	200 μm	200 $\pm$ 2 μm
H	500 μm	500 $\pm$ 5 μm
w,p	50 μm	50 $\pm$ 1 μm
s	50 μm	50 $\pm$ 1 μm
l	500 μm	500 $\pm$ 5 μm
t	120 nm	120 $\pm$ 10 nm

3.7 Polymer preparation

The thin film was prepared from a 2% wt/wt polystyrene solution dissolved in toluene. The solution was prepared in Freund's lab (506) of the Department of Chemistry at the University of Manitoba. Spin coating was exploited to cover the wafer with the polymer film. By controlling the spin speed to about 1000 rpm, the film thickness reached about 100 $\pm$ 30 nm. The device pads were exposed with a

cotton swap dipped in a toluene solution followed by surface cleaning using IPA. Then, the deposited film was placed in an oven for 30 min. at 110° to remove the solvent. Full details about the film preparation are provided in Appendix B.

In order to quantify the measurement error due to uncertainty of the film thickness, a COMSOL simulation was implemented. Given that the film thickness fluctuated within 100 ± 30 nm, this meant that 30 % uncertainty in the film thickness accounted for 2 % excess of the measurements over the FEM results.

3.8 Electrical measurements

As demonstrated in Figure 3.5, the sample was held on a glass slide where the whole ensemble was placed on a grounded chuck. The impedance analyzer cables weren't connected directly to the sample to close the doors of the probe station while taking the measurements. As a result, the accompanying parasitics reached the least about 20 fF on average. Since one of the sample electrodes was already grounded, the bottom of the sample was meant to be floating as not to introduce another unnecessary ground that would turn out $C_{polymer}$ almost half of its current value. For instance, the measurement of the 20 finger device was about 8 pF in the case of the floating chuck, compared to 4.5 pF for the grounded one.

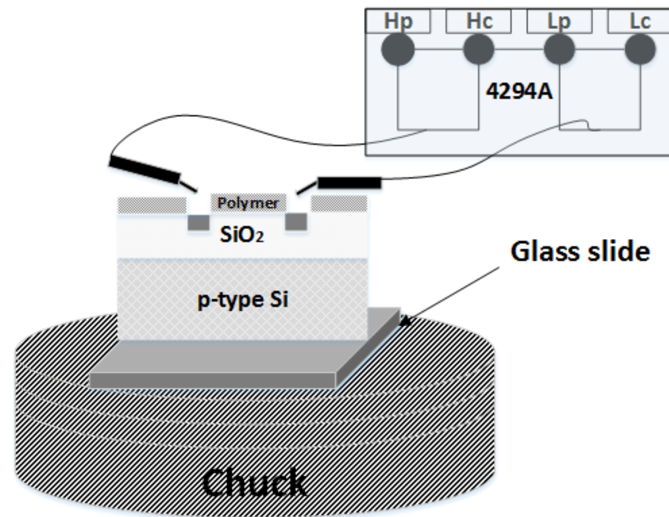


Figure 3.5: Capacitance measurement setup of the fabricated sample. The sample was placed on a glass slide on the chuck of the probe station, where the probes of the impedance analyzer was attached to the sample as shown.

Chapter 4

Results & Discussion

4.1 Measurement setup

The capacitance measurements taken by the impedance analyzer were C_p versus D. C_p referred to the parallel capacitance of the device. In this work, C_p and C_{total} were used interchangeably, and both referred to the same quantity. D stands for the dissipation factor or the loss tangent given by eq. (4.1) [38]

$$D = tan\frac{\epsilon''}{\epsilon'}. \tag{4.1}$$

For capacitors, D should be < 1 [44], which meant that the dielectric losses must be less than the real part of the permittivity. The operating range of the measurement lied between 40 Hz and 7.5 MHz. The higher frequency bound was estimated by trial and error as it was shown that above such a frequency, the dissipation factor would be higher than 1. The loss tangent of 1 was taken arbitrarily as a metric to stop the

frequency sweeping. At such a point, the losses were almost equal to the real part, which didn't imply a valid capacitor measurement.

Another measurement was carried out to check the plausibility of the fabricated structure (parallel line or interdigitated) as a valid capacitor. This test was done by measuring Z vs θ^o. For capacitors, the expected phase angle θ^o must be almost -90° at DC [9], then the phase varied with frequency afterwards as demonstrated in Figure 4.1

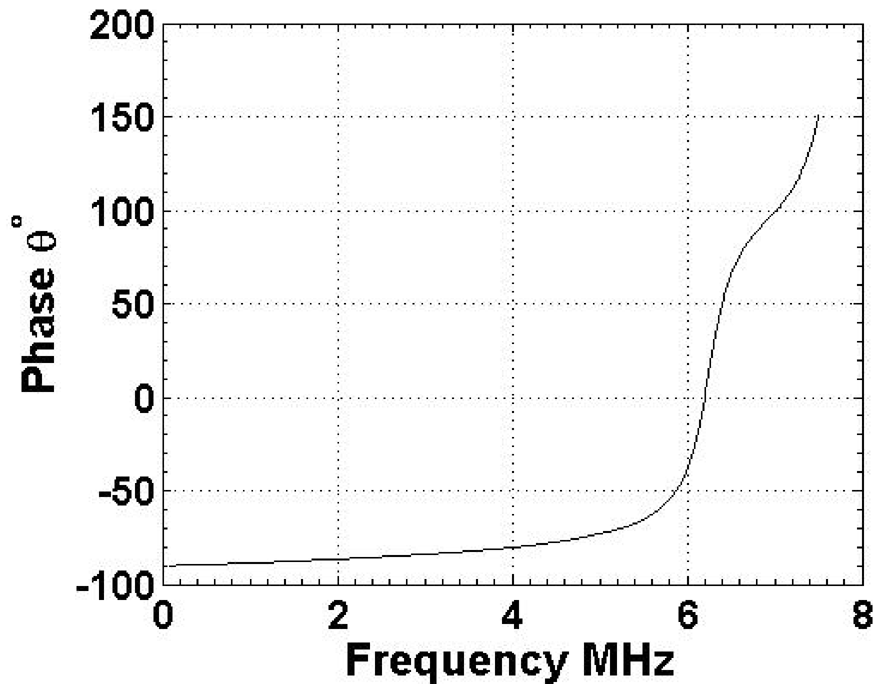


Figure 4.1: The phase angle of an arbitrary IDC to confirm its validity as a capacitor. As shown, $\theta^o = -90°$ from 0 to about 1 MHz, then the phase rose with increasing the applicable frequency.

Test samples comprising some surface mount capacitors were placed to examine whether the suggested setup was appropriate for taking correct capacitance measure-

ments and to determine the parasitic contributions. The final measurement setup was established when a consistency was observed between the measurements and the fixed values of the tested capacitors.

The system showed multiple resonances at frequencies (10MHz-20MHz), (20MHz-30MHz),...till 110MHz. Likewise, the corresponding dissipation factors in these respective frequencies were mostly above 1. Such resonances displayed on the impedance analyzer originated from the reactive components of the cables, probes, the impedance analyzer, as well as the sample under test. That's why such ranges weren't considered during the measurements.

The contribution of the polymer capacitance was estimated from differential measurements. The 1st measurement was done with the electrodes exposed to the air, while the 2nd measurement was implemented upon spin coating the thin film. All the measured quantities in this work were sampled by 801 points [38] which was the highest sampling representation achieved by the HP impedance analyzer, in order to attain the best resolution of displaying data.

To examine the reproducibility of the measurements, the displayed points were taken as an average of 5 independent trials. In each trial, the thin film was spin coated, the pads were exposed then, the film was stripped off and the measurement was retaken. The variability of the measurement was estimated by $\frac{max(C_{total})-min(C_{total})}{2}$.

The parasitic profile in Figure 4.2 was quantified by placing the probes in an open circuit fashion [38] where, the 2 probes spaced from one another and faced the chuck.

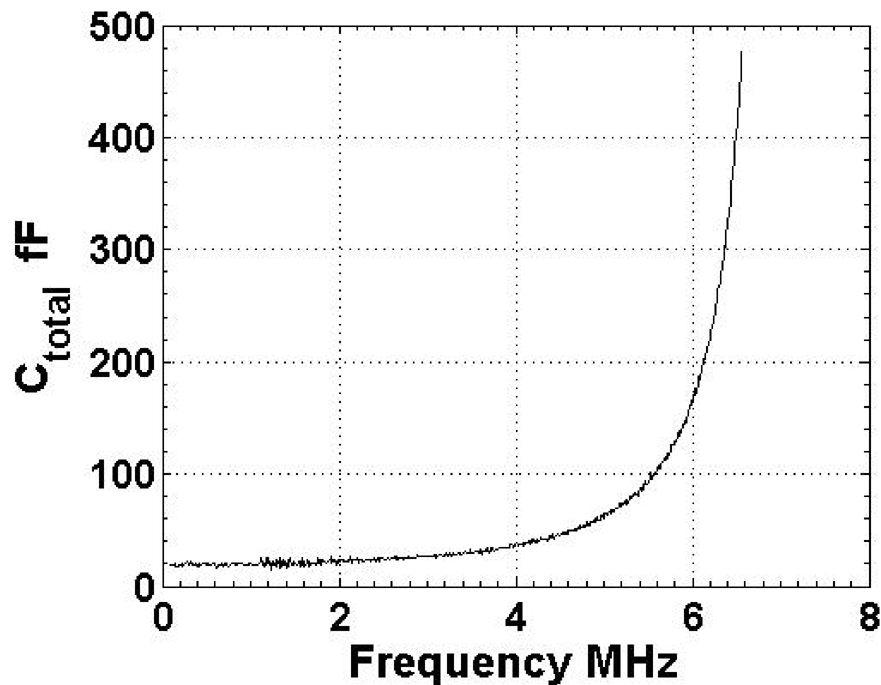
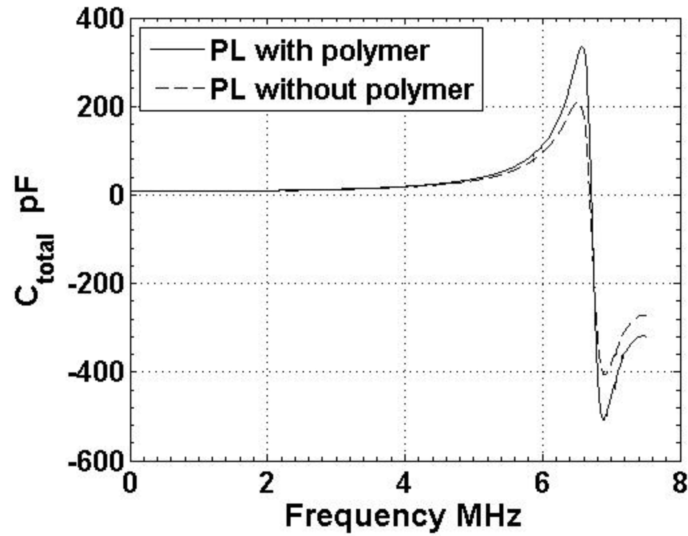


Figure 4.2: The measurement of the noise inside a probe station. The profile was about 20 fF till 2 MHz then it increased with frequency.

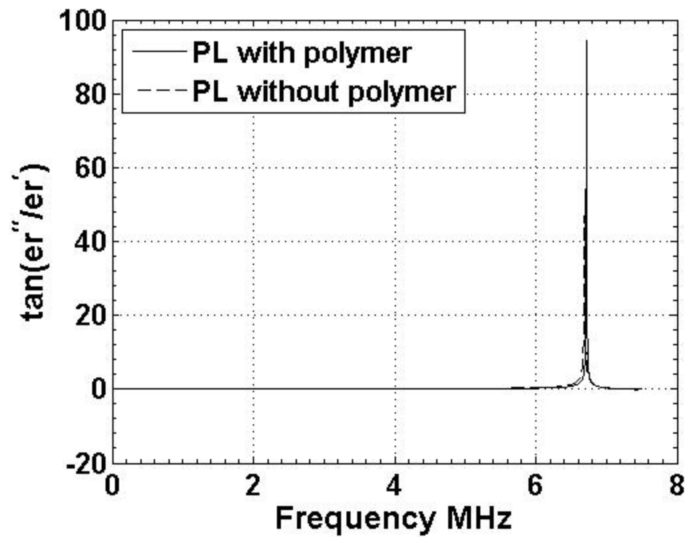
4.2 Capacitance of the parallel line device

The results shown below belonged to the 3000 μm device, which was selected as a representative of similar ones on the fabricated wafer. The feature appeared in Figures 4.3(a) and 4.3(b) occurred around 6.8 MHz. This was the location of the first resonance of the system resulted from the parasitic capacitances and inductances associated with the combination of cables and probes used in conjunction with the probe station and the impedance analyzer. The negative capacitances beyond the resonance point implied that the parallel line device behaved more like an inductor as

the dielectric losses were significant than the real part of the permittivity to render the loss tangent factor greater than 1.



(a)



(b)

Figure 4.3: The measurements taken for a parallel line device with the following dimensions l = 3000 μm , w = 50 μm , s = 200 μm and t = 120 nm. a) the total capacitance of this device with and without polymer b) the loss tangent of the above mentioned device with and without polymer.

The values of the dissipation factors shown in figure 4.3(b) were about 0.01 almost negligible to those at resonance, which explained the obvious overlapping between the respective curves. By taking the difference between the 2 curves of figure 4.3(a), the polymeric contribution $C_{polymer}$ of the 3000 μm device could be extracted as demonstrated in Figure 4.4.

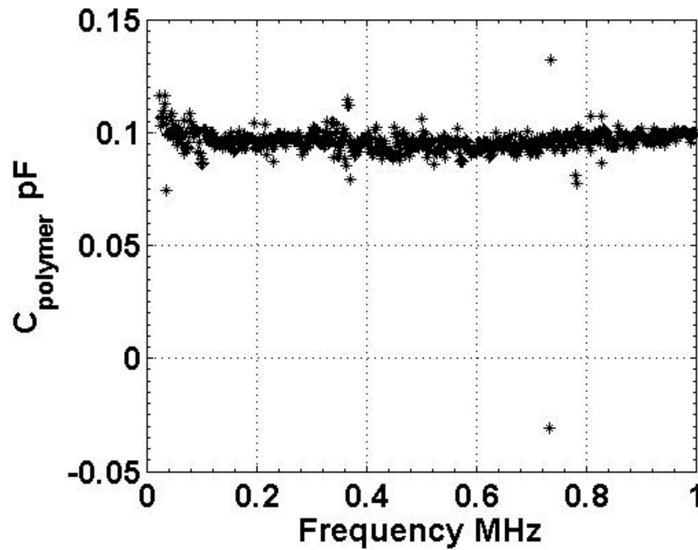


Figure 4.4: The polymeric contribution $C_{polymer}$ of a parallel line device with the following dimensions l = 3000 μm , w = 50 μm , s = 200 μm and t = 120 nm.

4.3 Comparison between the theoretical, FEM and measurements of the PL device

The purpose of that comparison was meant to show how far the measurements agreed with the calculations and finite element simulated models. The measurements

were taken at 9.414 KHz as this frequency represented the low frequency range. As demonstrated in figure 4.5, the points of the theoretical calculations were about 3 times as much as the recorded measurements. This discrepancy returned to the simplicity of the theoretical model when assuming that the thickness of the substrate or the polymer extended to infinity. Although, these assumptions might seem unrealistic, yet they were adopted due to the nature of such devices as control variables with the intent to give a fast prediction of the anticipated total capacitance order of magnitude. The accuracy of the prediction enhanced upon re-solving the problem using the finite element modeling. As shown, there was an observed tiny gap between the measurements and the results of finite modeling. The errors bars of the points manifested the uncertainty of the measurements and quantified to be 0.1 pF on average. The high value of the correlation coefficient in figure 4.5, indicated by the R^2 which reflected the linearity of the 3 methods relative to the lengths of the parallel lines.

The reference point of figure 4.5 referred to parallel lines of zero length on the horizontal axis, which corresponded to the parasitic noise on the vertical axis. If the slopes of the lines were extrapolated till the reference point, the intercepts of both the analytical and FEM would meet at the (0,0) point. This seemed logical because both methods were ideal, void of any accompanying noise. However, the measurements intercept at the 0 μm, registered tiny capacitance about 20 fF, which agreed with the estimated parasitic capacitance inside the probe station.

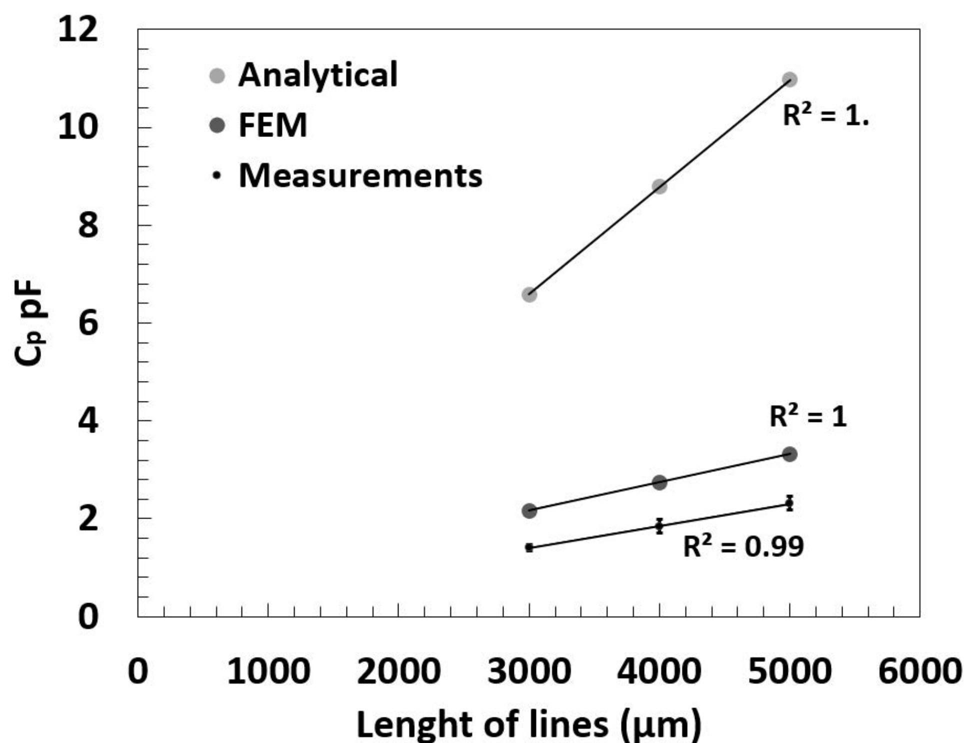


Figure 4.5: The lines depicted the comparison between the measurements against the theoretical and finite element models for the fabricated parallel line devices. The devices investigated had following dimensions l = 3000 μm , 4000 μm, 5000 μm , w = 50 μm , s = 200 μm and t = 120 nm. The legend of the measurements was reduced to view the errors bars clearly. The uncertainty of the measurement points was 0.1 pF on average.

4.4 Capacitance of the interdigitated device

The same capacitance measurements were repeated for the interdigitated case, where the following results specifically illustrated the behaviour of the 20 finger device. The curves of C_{total} and tangent loss factor were almost close to those of the parallel line device therefore, the curve of the polymeric capacitance was sufficient to be mentioned. As shown in figure 4.6, the polymeric contribution of this device remained

steady around 0.27 pF from 0 till 1 MHz.

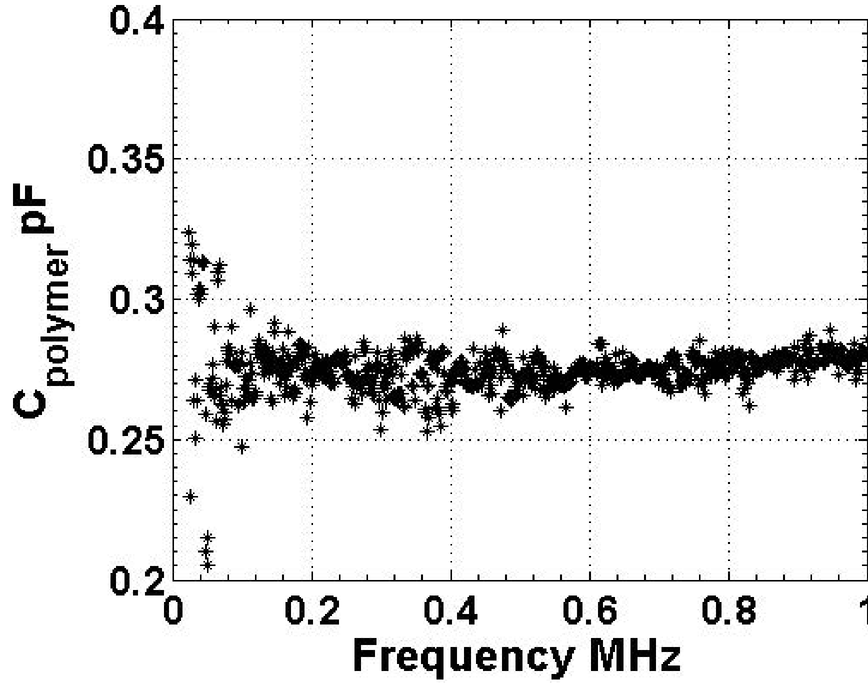


Figure 4.6: The curve depicted the $C_{polymer}$ of a 20 finger device with the following dimensions l = 500 μm, w = 50 μm, s = 50 μm, p = 50 μm and t = 120 nm.

4.5 Comparison between the theoretical, FEM and measurements of the IDC

Two frequencies (9.414 KHz and 1 MHz), sampled by the impedance analyzer in the range of 40 Hz till 7.5 MHz were chosen for drawing the comparison between the 3 different methods. The frequency 9.414 KHz represented the low frequency range instead of 40 Hz as the D factor at the latter frequency kept oscillating, which seemed

unreliable to be taken as a reference for the low frequency range. Furthermore, the 1 MHz was selected to signify the high frequency range.

As evident from figure 4.7(a) and 4.7(b), the data points of the theoretical analysis closely matched those of the finite element and experimental measurements. A high degree of correlation was observed between the data points indicated by R^2 = 0.98 and 1. On average, the polymeric contribution represented about 3% with respect to the total capacitance of the tested devices.

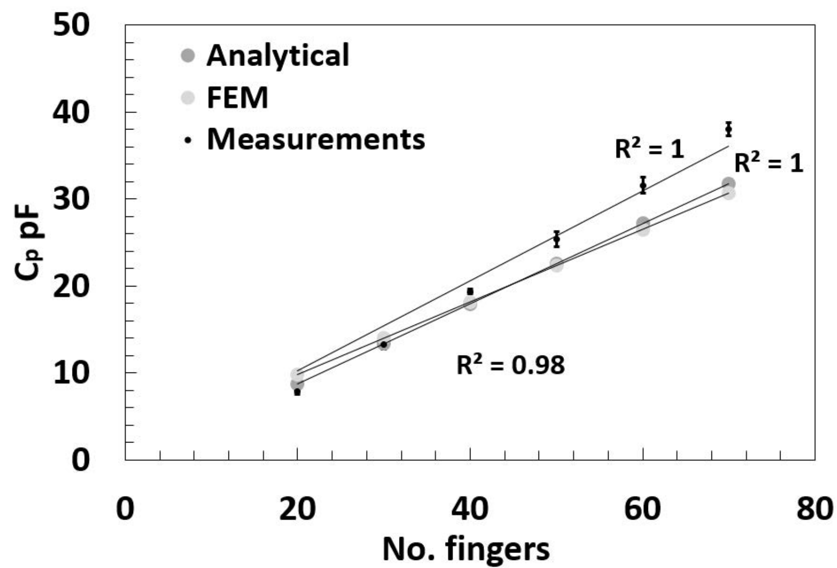
The results of the 3 methods at 9.414 KHz were almost equal to those at 1 MHz, which implied the preciseness of the suggested theoretical model in predicting the measured total capacitance irrespective of the applied frequency. The drift between the measured and theoretical C_{total} at 9.414 KHz and 1 MHz was estimated to be 10% and 13% respectively.

On average, the uncertainty of the measurement points were estimated to be 1.5 % of the total capacitance of the fabricated devices. The first source of this uncertainty originated from the noise due to the contact between the probes and the pads in addition to the random noise resulted from the surroundings. Another reason for the measurements variability was the scratching of the pads due to the removal and placement of the measurement probes. As noted, the parasitic capacitance was in order of 20 fF with, smaller than the nominal capacitance of the fabricated devices by about 3 orders of magnitude. Therefore, the drift between the measurements and calculations due to such a noise could be ignored altogether.

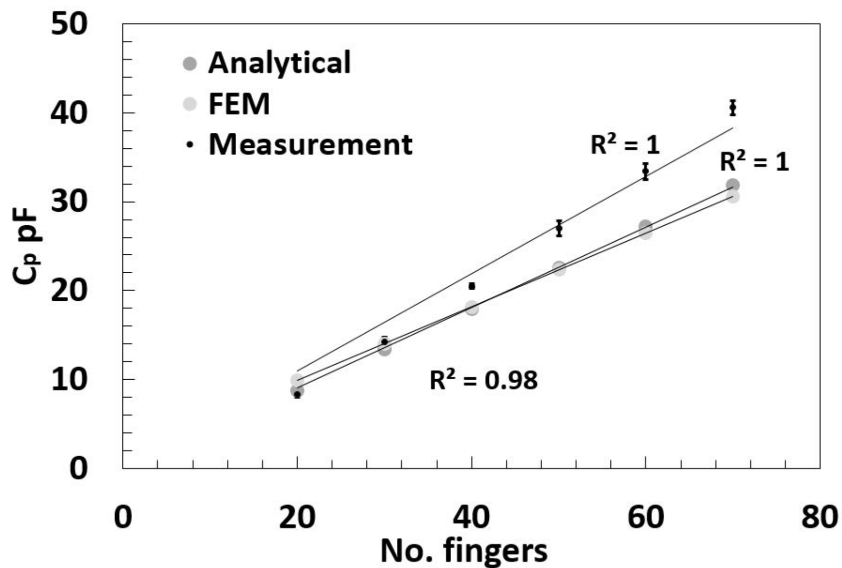
The measurements exceeded the results of both the analytical and FEM models by about 12 % on average. As previously mentioned, such a discrepancy resulted

from the normal uncertainties during the fabrication process and film deposition.

At 9.414 KHz and 1 MHz, extrapolating the analytical line intersected the axes at the (0,0) points. This indicated zero noise for no fingers as predicted due to ideality of the model. The same scenario occurred for the FEM case. However, the measurements slope line recorded about 20 fF at the reference point, equivalent to the existing parasitic capacitance inside the probe station.



(a)



(b)

Figure 4.7: The comparison between the theoretical, FEM and experimental measurements for multiple IDC devices. The dimensions of each device l = 500 μm, w = 50 μm , s = 50 μm, p = 50 μm and t = 120 nm. The fingers count ranged from 20,30, till 70 fingers. The data points in 4.7(a) and 4.7(b) were taken at 9.414 KHz and 1 MHz respectively. On average, the uncertainty of the measurement points was 1.5% relative to the total capacitance of the tested devices.

4.6 Scalability of $C_{polymer}$

Confirming the scalability of $C_{polymer}$ was one of the research goals in this project. As shown in figure 4.8, $C_{polymer}$ was directly proportional to the device's surface area or the fingers' count. The linearity of $C_{polymer}$ relative to the number of fingers was also predicted from eq. (2.11). Furthermore, the data points of the profiles in figures 4.8, exhibited a constancy throughout the operating frequency range. This concluded that the relative permittivity constant $\epsilon'_{polymer}$ of the polystyrene thin film isn't dispersive. This was expected because polystyrene in a solid state is an example of non-polar polymers [1], free from orientation polarization mechanism. The solid state was guaranteed upon the removal of the tolune solvent by heating the deposited films inside an oven.

By taking the average of the third column in table 4.1, the capacitance contribution of each finger was estimated to be 10 fF.

Table 4.1: The $C_{polymer}$ per finger of some fabricated interdigiated devices. Each of the examined devices had the following dimensions: l = 500 μm , w = 50 μm , s = 50 μm, p = 50 μm and t = 120 nm with 20, 40 and 60 finger counts.

Finger	$C_{polymer} pF$	$\frac{C_{polymer}}{finger} pF$
20	0.275	0.014
40	0.497	0.012
60	0.639	0.011

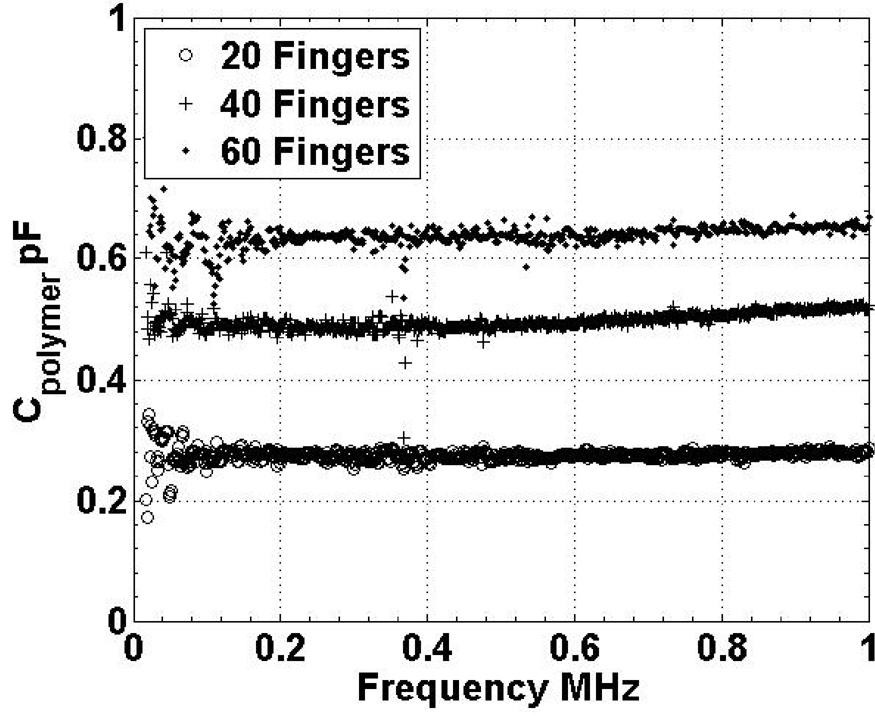


Figure 4.8: The profiles demonstrated the scalability of the $C_{polymer}$. The measurements were based upon multiple IDC devices with finger count 20, 40 and 60, each with the following dimension: l = 500 μm, w = 50 μm , s = 50 μm , p = 50 μm and t = 120 nm. The tiny fluctuations appeared in the measured profiles, especially at low frequencies around (40 Hz- 50 KHz) occurred due to the normal non-idealities of the impedance analyzer resulting from the quantized sampling. One can notice that such fluctuations were quantified to be $\pm$ 0.1 pF, at low frequency range but died out afterwards.

4.7 Extraction of permittivity constants

The relative permittivity constant $\epsilon'_{polymer}$ of the polystyrene thin film could be extracted from the measured $C_{polymer}$. Regarding the frequency range shown in figure 4.9, the measurement of $C_{polymer}$ was based upon 5 independent trials to ensure the reproducibility of the results. By solving eq. (4.2) with the following dimensions: l

= 500 μm, w = 50 μm , s = 50 μm and p = 50 μm and N=20, one could estimate the $\epsilon'_{polymer}$ in the frequency range (0-1MHz)

$$\epsilon'_{polymer} = \frac{C_{polymer}}{(N-1)\epsilon_{\circ} l} \frac{K(k'_{polymer})}{K(k_{polymer})}. \tag{4.2}$$

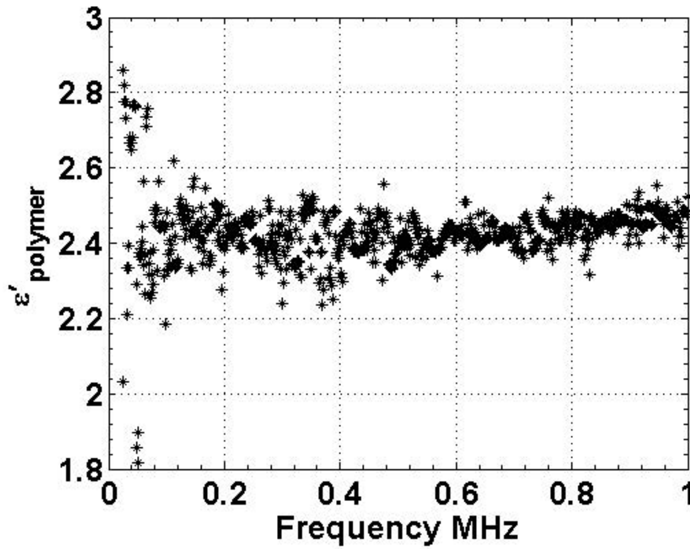


Figure 4.9: The curve of $\epsilon'_{polymer}$ vs frequency. This was achieved by measuring $C_{polymer}$ for a 20 finger device, then solve for $\epsilon'_{polymer}$ using (4.2)

Figure 4.9 predicted that the relative permittivity of the polystyrene thin film was fluctuating around 2.4. This number fell within the range of the dielectric constant of bulk polystyrene $(2.4 - 2.7)$ [45].

The imaginary part of the polymer permittivity $\epsilon''_{polymer}$ was determined by solving first for the dissipation factor of the polymer as in eq. (4.3). This was followed by multiplying $\epsilon'_{polymer}$ derived from eq. (4.2) by eq. (4.3). The few disruptions of the imaginary part in Figure 4.3, resulted from the quantized sampling of the impedance

analyzer. Another reason for the disruption was the smoothing algorithm used in post-processing the data by MATLAB to remove unwanted spurious noise and enhance the continuity of the viewed points.

$$\delta_{polymer} = \delta_{with-polymer} - \delta_{without-polymer}$$
$$tan^{-1}\left(\frac{\epsilon''_{polymer}}{\epsilon'_{polymer}}\right) = \tan^{-1} D_{with-polymer} - \tan^{-1} D_{without-polymer} \tag{4.3}$$

$$\epsilon''_{polymer} = \epsilon'_{polymer} * \tan\left(tan^{-1}\left(\frac{\epsilon''_{polymer}}{\epsilon'_{polymer}}\right)\right) \tag{4.4}$$

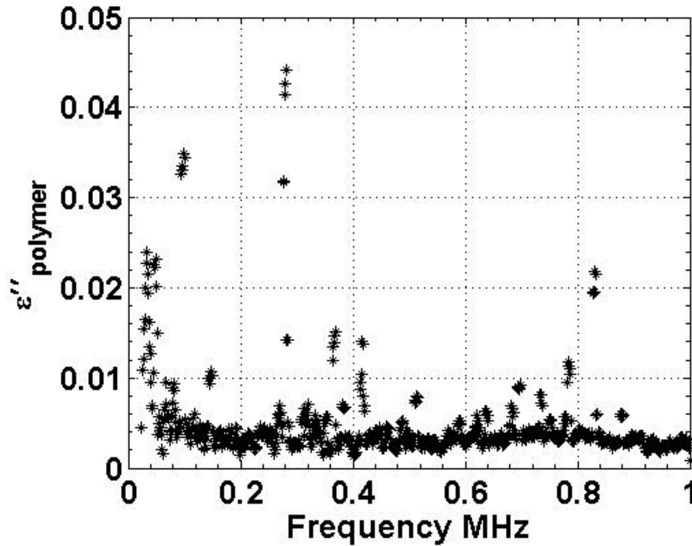


Figure 4.10: The curve demonstrated the behavior of $\epsilon''_{polymer}$ vs frequency. This was achieved by solving multiplying eq. (4.2) by eq. (4.3)

4.8 Resistance measurement of the IDC

In order to fully model the impedance of the fabricated interdigitated device, it was also important to measure its resistance and inductance. The measured inductances for the tested devices were in the order of μH, which could be ignored for all practical purposes. The measured resistance was next compared with the anticipated calculations. Based upon the resistance modeling of the interdigitated device shown in figure 4.11, the overall resistance could be computed by:

$$R_{total} = R_{polymer} \parallel [R_{elec} + (R_{SiO_2} \parallel R_{Si})] \tag{4.5}$$

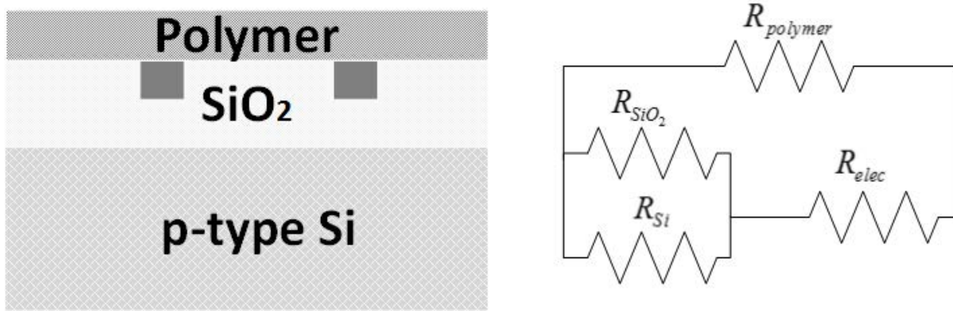


Figure 4.11: The resistance modeling of the IDC, where $R_{polymer}$, R_{elec}, R_{SiO_2} and R_{Si} represented the equivalent resistance of the polymer layer, electrodes, the oxide layer and the p-type Si substrate respectively.

The expected skin depth in the metallization layer was calculated to be 65 μm at 1 MHz using the following formula [46]

$$\delta_{Cu} = \frac{1}{\sqrt{\frac{1}{2}\omega\sigma_{Cu}\mu_{Cu}}}. \tag{4.6}$$

where σ_{Cu} and μ_{Cu} were equal to 5.96x$10^7 Sm^{-1}$ and 1.26x$10^{-6} Hm^{-1}$ respectively [9]. Because the electrodes thickness was less than the skin depth [47], the resistance per unit length as well as the total resistance of the electrodes could be approximated by eq. (4.7)-(4.8) where, t and s referred to the thickness and the spacing between the electrodes respectively

$$R_{per-unit} = \frac{1}{s\sigma_{Cu}t} \quad (4.7)$$

$$R_{elec} = (2N-1)R_{per-unit}l. \quad (4.8)$$

The electrode contribution R_{elec} of a 20 finger device with electrodes of 500 μm long, 50 μm width and spacing, thickness of 100 nm was calculated to be about 67 Ω.

The resistance of the p-type Si substrate, SiO_2 and the polymeric layer were determined by eq. (4.10), where R_s was defined as the sheet resistance [9]

$$R_s = \frac{\rho}{t} \quad (4.9)$$

$$R = R_s\frac{l}{w}. \quad (4.10)$$

Based upon the previous equations, the resistance of the p-type Si substrate, SiO_2 and the polymeric layer of an interdigitated device were listed in the following table.

Table 4.2: The listed values were pertinent to a 20 finger device with w = 50 μm , s = 50 μm, l = 500 μm and t = 120 nm. The electrodes were fabricated on a SiO_2/Si wafer with a resistivity ρ = 0.002–0.005$\Omega.cm$

Layer	ρ ($\Omega.cm$)	t (μm)	l (μm)	w μm	R (Ω)
SiO_2	10^{15}	1	4900	950	$5.21 * 10^{19}$
Si	$35 * 10^{-4}$	500	4900	950	0.2
polystyrene	10^{14} [45]	0.1	4900	950	$5.21 * 10^{21}$

The resistance measurement was a key because it implied the overall system losses. According to eq. (4.5), it was obvious the total resistance R_{total} of such a device was almost equal to the contribution of the electrodes R_{elec}, that's why the calculated R_{total} was about 67 Ω. The measured resistance of the above mentioned device using the impedance analyzer at 1 MHz was about 81 Ω. The difference between the calculated and measured resistance quantified to be 17%. This difference resulted from the additional resistance of the tungsten probes, coaxial cables as well as the contribution of the impedance analyzer. To estimate that difference, the 2 probes were shorted out by a shorting brass which was placed on a glass slide. The measured resistance of the shorted loop by the impedance analyzer recorded 14 Ω on average, equivalent to the difference between the measured and calculated resistance.

Chapter 5

Conclusion & Future work

The work done in this thesis was devoted to design a sample holder appropriate for thin films (100-200 nm) for measuring the dielectric properties of polymeric materials. To achieve this, multiple interdigitated devices fabricated on SiO_2/Si wafer were created, with a deposited thin film of polystyrene. The dimensions for the ultimate device were chosen upon amplifying the $\frac{C_{polymer}}{C_{total}}$ ratio. Based upon this criteria, the polymeric capacitance was maximized while, the electrodes capacitance which referred to their crosstalk was minimized.

The polymeric contribution was determined by differential capacitance measurements which were post-processed in MATLAB. This rendered the mask design simpler, without the necessity of a capacitive bridge that would have led to more involving and complex fabrication process.

The measured total capacitance for a 20 finger device with electrodes of 50 μm finger width and spacing, 500 μm finger length from the contact pads had a capacitance of about 8 pF. The polymeric contribution represented about 3% of the total

capacitance. Additionally, $C_{polymer}$ was found to be scalable or directly proportional to the device's area or finger count. There was an observed close matching between the measurements and the anticipated results derived from the theoretical of finite modeling. It was found that the measurements exceeded the theoretical values by about 12%.

Regarding the resistance, the measured resistance for a 20 finger device with the above dimensions amounted to be 81 Ω. This value was higher than the calculated resistance by 17%.

5.1 Future Work

The future progress can be spanned two pathways. The first option encompasses an improvement to the sample holder itself. Despite the simplicity of the mask design and fabrication process, yet the estimation of the polymeric capacitance was a lengthy process. For instance, the differential capacitance measurements of the sample holder demanded data acquisition from the HP impedance analyzer, followed by post-processing using MATLAB.

The future design of the sample holder might be a capacitive bridge. The suggested model for implementation is a Wheatstone bridge [48]. The capacitance of the unknown branch that mimics the deposited thin film could be detected from the other 3 known branches lying in the order of pF. Upon the thin film deposition, this structure should detect the polymeric contribution immediately by the impedance analyzer. This design will lead easier and faster obtainment of results than the current

differential method. On the contrary, the fabrication mask would be more involving; requiring one or more layers for the electrodes metallization, while another layer for the polymer coating. After stabilizing the fabrication process in this work as well as learning some fine details about mask creation, the construction of this bridge would be a calculated adventure worth experimenting.

The second pathway relates to the sample itself. Polymers exhibit a “glass transition T_g phenomenon”, which expresses the temperature at which the polymer molecules attain large mobility to change from a crystalline into a glassy state [49]. At the T_g point, both the thermal expansion and heat capacity of the polymeric sample reveal sudden changes [49]. Gauging the T_g for different polymers could be doable using this sample holder. For the case of thin films, this transition is probed by ellipsometry [50], where the measurements are a function of the refractive index and the thickness of the film [50].

Ferromagnetic thin films like BST are of great importance nowadays in applications like high-K capacitors [51]. From a research perspective, it would be interesting to characterize the dielectric constants of such films using the current sample holder. One potential method to prepare BST sample on the SiO_2/Si substrate, is through metal organic chemical vapor deposition (MOCVD) and chemical solution deposition (CSD) [52]. As a prerequisite, the pads should be coated using tiny pieces of parafilm before the deposition.

Concerning dielectric spectroscopy, the capacitance measurements done in this project were taken at ambient temperature. For a complete dielectric study, the samples should be exposed to a wide range of temperature to monitor the different

relaxation mechanisms i.e α,β and γ [1]. Furthermore, the interfacial polarization mechanism resulted from the trapped charges at the electrode substrate or polymer substrate interfaces worth quantifying. However, the HP impedance analyzer falls short to that purpose because the lowest applicable frequency is 40 Hz higher than the typical range of the interfacial resonance (around 1 Hz) [9]. One possible technique is to utilize a contact-less electric force microscopy (EFM) to map the dielectric spectroscopic variations with submicron spatial resolution. Instrumentally, this could be implemented on the fabricated sample holder , where a pair of the pads provides the location for the EFM measurements while, the other pair of pads as well the electrodes would be grounded.

Appendix A

Fabrication Recipe

In this project, the PL and IDC devices were fabricated on SiO_2/Si 4″[100] wafer. The thickness of the Si layer was 500 μm. At the top of the Si layer, 1μm layer of SiO_2 was grown. The following listing clarifies the recipe of each process in detail.

- **Photolithograpy**
  - Spin coat the wafer will HPR504 photoresist at 2000 rpm for 30 Sec.
  - Soft bake the wafer for 90 sec.
  - Cool down the baked wafer for 5 sec on a metallic table.
  - Expose the wafer under i-line UV for 6 sec.
  - Develop the exposed wafer using HPR345 developer.
  - Dry the developed wafer using N_2 gun.
  - Hard bake the developed wafer in an oven at 110° for 30 min.
- **Plasma Etching**

- Cut the wafer using the crosshair mark into 4 compartments.
- Place each compartment into the plamsa chamber.
- Pump down the chamber.
- Pressure set: 200 mTorr.
- ICP: 300 Watts.
- RIE: 50 Watts.
- Flow CF_4/O_2 with concentration 45/5 sccm.
- Ignite the plasma for 7 min.
- Depth of trenches in the SiO_2 layer was $\approxeq$ 120 nm.

• **Thermal Evaporation**

- Surface clean a Cr rod using IPA.
  * Apply steps of 2A until the pressure increases to 20 mTorr.
  * When the Cr outgases, decrease the current rightway to 0A.
  * Repeat this process 2-3 times, until the Cr stops outgasing.
- Evaporate the Cr, when the current reaches 9-10 A, this gives an evaporation rate of 5nm/sec.
- The evaporation lasts for 4 sec to deposit 20 nm.
- Place the Cu pallets in a boat, increase the current till it reaches 25-28A.
- Upon reaching this current level, evaporate the Cu pallets. This gives an evaporation rate of 10 nm/sec.

  - Continue the evaporation for 12 sec.

- **Liftoff process**
  - Place the metalized wafer into a glass beaker full of acetone.
  - Ultra sonicate the beaker for 30 min.
  - If any PR remanants are still there on the wafer, wipe out the wafer in one direction only using a cotton swap filled with acetone.
  - Watch the devices under the microscope, repeat the wiping out until no remnants are remaining.
  - Surface clean the wafer using IPA.
  - Dry the wafer using N_2 gun.

Appendix B

Polymer Coating

The fabricated wafer was spin coated with a polystyrene 2% wt/wt. The polystyrene film was removed to expose the pads for permittivity measurements. The solvent for such a solution was toluene. The following section gives a detailed recipe about the solution preparation.

- **Solution Preparation**
  - Bring a fresh clean glass beaker of a volume > 100 mL.
  - Place the beaker on the scale, then zero the weight.
  - Drop 100 mL of toluene solution into the beaker, this is equivalent to 78 g.
  - The weight of polystyrene is 2% of the toluene , this is equivalent to 1.56 g.
  - Take the beaker off the scale.

  - Bring a fresh new solute holder, and place the polystyrene granules on the scale until the weight reaches 1.56 g.
  - Drop the polystyrene solute in the toluene solvent.

- **Sonication**
  - Shake the beaker for 1-2 min, for the polystyrene to start dissolve in toluene.
  - Cover the beaker top with a parafilm, to protect the toluene from evaporation.
  - Place the beaker in the Sonicator, apply the sonication time to be 50 min.

- **Spin coating**
  - Adjust the spin coater to have 3 consecutive processes.
  - The dumping of the solution takes 5 sec and spins at 100 rpm.
  - The spreading of the solution takes 10 sec and spins at 500 rpm.
  - Run the spin coater at 1000 rpm for 50 sec.
  - The thickness of the polystyrene film is about 100 ± 30 nm.
  - Hard bake the deposited polystyrene film in an oven at $110°$ for 30 minutes.

- **Pads exposure**
  - Bring 2 petri dishes, put about 20 mL of toluene solution in the first one, and 20 mL of IPA in the second dish.

- Dip a cotton swap in the toluene dish, dry the swap against the dish wall to remove the excess of the toluene droplets.
- Use another fresh new cotton swap and repeat the previous step with the IPA. solution.
- Apply the toluene swap against the coated wafer, to expose the pads.
- Apply the IPA swap against the exposed pads to remove any excess droplets of toluene.
- Watch the exposed devices under the microscope. If there any leftovers on the pads, repeat the 2 previous steps to remove any film remnants from the pads.

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