Power Quality Conditioning Technology for Power Grids with Modern Lighting Loads

by

Radwa Mohamed Sayed Abdalaal

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University of Manitoba

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Examining Committee

Prof. Carl Ngai Man Ho, Dept. of Electrical and Computer Engineering, University of Manitoba

Prof. Udaya Annakkage, Dept. of Electrical and Computer Engineering, University of Manitoba

Prof. Qiuyan Yuan, Dept. of Civil Engineering, University of Manitoba

Prof. Ka-Hong Loo, Dept. of Electronic and Information Engineering, Hong Kong Polytechnic University

Abstract

Poor power quality network, including long and short voltage variations, is directly reflected into visual light flickering in light emitting diode (LED) lighting networks. On the other hand, a large scale of LED lighting network injects high harmonic contents that are generated by the internal driver of LEDs. Accordingly, this will distort the quality of the grid leading to high voltage and current total harmonics distortion.

This thesis proposes a power electronics apparatus to mitigate major power quality problems in LED lighting networks and improve the overall quality of distribution networks. An active power filter has been proposed as a comprehensive solution to improve grid current and light intensity flickers in a large-scale LED lighting network. The first part of the research study is conducted to gain a better understanding of the characterization of commercial dimmable LED lamps as nonlinear loads. The second part of the research study proposes a single-phase transformerless unified power quality conditioner (TL-UPQC) topology with its controls. The topology provides a stable output voltage for a flicker free lighting network. An active power filter injects harmonic and reactive currents to provide unity power factor. A dynamic voltage restorer quickly supports the load voltage for any voltage dip, swell or flickering in the network. Stability of the designed controllers is analyzed by a small-signal modeling technique. In addition, the proposed topology has been utilized as a central dimmer system for LED lamps while maintaining high voltage and current quality.

The TL-UPQC features have been extended to improve the grid voltage profile by designing an ac voltage control loop to achieve reactive power compensation into the input grid. Moreover, the thesis presents a novel approach for a supervisory remote management system to regulate a secondary control system that is based on the available capacity of distributed units connected to

the same point of common coupling. The TL-UPQC system topology and its controller methodology have been verified experimentally with a 500VA / 120V prototype. Modularized distributed TL-UPQC systems have been evaluated by implementing a controller hardware-in-the-loop test. All described strategies' experimental results show good agreements with the theoretical concept.

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Dedication

"To my loving parents, Mr. Mohamed Sayed Abdalaal and Ms. Maha Mustafa"

Table of Contents

Examinee Committees ii
Abstract iii
Acknowledgments v
Dedication vii
Table of Contents viii
List of Tables xii
List of Figures xiii
Chapter 1 Introduction xx
1.1 Background 1
1.2 Overview of Power Quality Definition and Standards 2
1.2.1 Power Quality Steady-State Issues 4
1.2.2 PQ Disturbances Issues 8
1.3 Motivation and Research Objectives 9
1.4 Research Contributions 175
1.5 Thesis Layout 12
Chapter 2 Literature Review of Power Quality Mitigation in a Distribution Network 15
2.1 Introduction 15
2.2 UPQC - State of Art 15
2.2.1 Classification of UPQC Topologies 16
2.2.2 Transformerless UPQC topology 23
2.2.3 Series APF Compensation Control Strategy 23
2.2.4 Shunt APF Compensation Control Strategy 25
2.3 Grid Voltage Regulation Techniques 27
2.4 Parallel Operation of Modularized Converters 30
2.5 Chapter conclusion 34
Chapter 3 Characterization of Commercial LED Lamps for Power Quality Studies 35
3.1 Introduction 35
3.2 LED Lamps Technology 36
3.2.1 LED Semiconductor material 37

3.2.2 LED Drivers 37
3.2.3 LED International Regulations 41
3.3 LED Lamps Power Quality Problems 42
3.4 Experimental Setup of LED Characterization 44
3.5 Experimental Results and Analysis 47
3.5.1 Harmonic Analysis 48
3.5.2 Static Relationship between Light Intensity, LED Array Voltage and Input Voltage 50
3.5.3 Dimming with amplitude variation technique 51
3.5.4 Flickering and Sensitivity to Voltage Fluctuations 53
3.5.5 Voltage Sag and Swell 59
3.6 Chapter Conclusion 61
Chapter 4 Transformerless Unified Power Quality Conditioner 63
4.1 Introduction 63
4.2 Proposed TL-UPQC Topology 64
4.2.1 Principle of operation 64
4.2.2 Series DVR Compensation Approach 68
4.3 Controller Design and Implementation 69
4.3.1 Control topology of APF 69
4.3.2 Control Methodology of DVR 71
4.4 System modeling and Characterization 76
4.4.1 State space model of APF 76
4.4.2 State space model of DVR 80
4.5 TL-UPQC Sizing 82
4.6 Experimental Verifications 85
4.6.1 Verifications of Mathematical Model 86
4.6.2 Results of Reactive Power Compensation and Current Harmonics Elimination 88
4.6.3 Results of Voltage Variations and Flickers Elimination 89
4.7 Chapter Conclusion 92
Chapter 5 A Remotely Central Dimming System 93
5.1 Introduction 93
5.2 State of Art of Dimming Technology 95
5.2.1 LED Driver Dimming Techniques 95

5.2.2 TRIAC-Based Dimmers 97
5.2.3 Protocols of Dimming Systems 99
5.3 Proposed Remote Control Dimming System 101
5.3.1 Principle of Operation 103
5.3.2 Remote System and Devices 105
5.4 System Modelling and Characterization 107
5.4.1 Stability of Control system 107
5.4.2 System Loss Estimations 108
5.5 Experimental Verifications 110
5.5.1 Implementation of Testbed 110
5.5.2 Evaluation of Dimming Performance 110
5.5.3 Static Power Quality Evaluations 111
5.5.4 Voltage Sag and voltage swell 113
5.5.5 Interactive GUI and Network Latency 114
5.6 Chapter Conclusion 117
Chapter 6 Enhanced Control Methodology for Input Grid Voltage Regulation 118
6.1 Introduction 118
6.2 System Description and Operation 119
6.2.1 Power Flow Analysis 122
6.2.2 Enhanced Controller Strategy 124
6.3 System Modeling 126
6.3.1 Dc voltage loop 128
6.3.2 Ac voltage loop 129
6.3.3 System stability and controller design 130
6.4 Experimental Verifications 134
6.4.1 Controller implementation 136
6.4.2 Nonlinear load at the load bus 138
6.4.3 Linear load at bus B 139
6.4.4 Transient 139
6.5 Chapter Conclusion 142
Chapter 7 A Supervisory Remote Management System for Modularized distributed TL-UPQC Systems 143
7.1 Introduction 143

7.2 Parallel-Operated TL-UPQCs 145
7.2.1 Distributed System Operation 147
7.2.2 Control Scheme Structure 151
7.2.3 Control Scheme Coordination 155
7.3 System implementation 164
7.4 Experimental Verification 166
7.4.1 Validation of one TL-UPQC module 166
7.4.2 Validation of parallel operation of TL-UPQCs 168
7.5 Chapter Conclusion 172
Chapter 8 Conclusion and Future Work 173
8.1 Conclusion and major contributions 173
8.2 Future Work 178
References 188

List of Tables

Table 1-I Power Quality Standards 3

Table 3-I Comparison Between The Efficacy of Various Types of Lighting Sources [16] 36

Table 3-II Power Supply Requirements in Energy Star Program [98] 42

Table 3-III Basic Parameters Measured for LED Lamps Under Test 48

Table 3-IV Power Quality Parameters with Varying Voltage Amplitude 53

Table 3-V Percent Flicker for 2% Step Change in Modulation Index 57

Table 3-VI Percent Flicker Under Different Dimming Levels 59

Table 4-I System Parameters 85

Table 4-II Measured Power Analysis Parameters with Connection to a Nonlinear Load 89

Table 5-I Communication Parameters 117

Table 6-I Enhanced TL-UPQC System Parameters 136

Table 6-II TL-UPQC Controller Design 136

Table 6-III Power Analysis Measurements without and with UPQC System 138

Table 7-I Communication Delay Effect 162

Table 7-II Measured Power Analysis Parameters for Various Types of Loads 168

Table 7-III System Specifications 169

Table 8-I TL-UPQC System Features 175

List of Figures

Figure 1-1. Voltage fluctuations of 161 kV substation supplying an electric arc furnace load [3]. 2

Figure 1-2. Power quality problems classification [4]. 4

Figure 2-1. General block diagram of UPQC topology (a) VSC (b) CSC. 16

Figure 2-2. Classification of UPQC [20]. 17

Figure 2-3. (a) 1P2W FB UPQC topology (b) 1PP2W HB UPQC topology (c) 1P2W three-leg UPQC topology. 19

Figure 2-4. (a) 3P3W UPQC topology (b) 3P4W UPQC topology. 20

Figure 2-5. Left UPQC configuration. 21

Figure 2-6. (a) DG unit integration with UPQC (b) Battery integration with UPQC. 22

Figure 2-7. UPQC configuration with (a) interline (b) multi-converter. 22

Figure 2-8. Phasor diagrams of DVR compensation methodologies (a) UPQC-P (b) UPQC-Q (c) UPQC-S 24

Figure 2-9. (a) Instantaneous reactive power control technique (b) Synchronous reference frame control technique. 27

Figure 2-10. Voltage control mode of a D-STATCOM in the d-q frame [57], [58]. 29

Figure 2-11. (a) Decentralized control scheme (b) centralized control scheme. 32

Figure 2-12. (a) Master/slave control scheme (b) distributed control scheme. 33

Figure 3-1. Sectional view diagram of an LED lamp..... 37

Figure 3-2. Passive LED driver based on valley-fill circuit [92]. 40

Figure 3-3. Single-stage LED driver based on buck converter 40

Figure 3-4. Single-stage LED driver based on flyback converter. 40

Figure 3-5. Two-stage LED driver. 40

Figure 3-6. Conventional two-stage LED driver for high power applications. 40

Figure 3-7. Experimental setup (a) block diagram (b) laboratory setup. 45

Figure 3-8. Black box dimension. 45

Figure 3-9. Input voltage and input current drawn by LEDs (a) sinusoidal input voltage (b) distorted input voltage..... 49

Figure 3-10. Harmonic spectrum of the current drawn by the LEDs. 50

Figure 3-11. Input voltage vs (a) LED voltage and (b) light intensity. 51

Figure 3-12. Applied voltage flickering to LED lamps..... 55

Figure 3-13. LED voltage and light intensity with (a) no flickering input voltage (b) 15 Hz voltage flickering (c) 4 Hz voltage flickering. 56

Figure 3-14. Measured and perceived light intensity under different voltage levels. 58

Figure 3-15. Measured and perceived illuminance with voltage flickering (a) 100% light intensity (b) 16% light intensity. 58

Figure 3-16. Voltage across the LED for different applied voltage sag levels. 60

Figure 3-17. LED voltage at (a) 23% voltage sag (b) 110% voltage swell. 60

Figure 4-1. The conceptual idea of a TL-UPQC to solve PQ issues of a LED lighting network. 64

Figure 4-2. The proposed single-phase TL-UPQC. 65

Figure 4-3. (a) Steady-state circuit model of the proposed TL-UPQC (b) a block diagram of power flow in the TL-UPQC system. 66

Figure 4-4. Phasor diagrams of (a) normal operation (b) voltage swell (v) voltage sag. ... 68

Figure 4-5. Half-bridge inverter configuration of APF. 69

Figure 4-6. Control block diagram of the APF. 69

Figure 4-7. Half-bridge inverter configuration of DVR. 72

Figure 4-8. Switching trajectories of DVR. 72

Figure 4-9. Typical waveforms of the DVR [115]. 74

Figure 4-10. Flow chart of boundary control law. 76

Figure 4-11. Small-signal control block diagram of the shunt APF converter. 77

Figure 4-12. Frequency response of power stage (Tp), controller (Tc) and Overall open loop system (TOL). 80

Figure 4-13. Small-signal control block diagram of the DVR converter. 82

Figure 4-14. Frequency plot of boundary control. 82

Figure 4-15. Experimental setup. 86

Figure 4-16. Connection diagram for frequency response analyzer Bode100. 87

Figure 4-17. Frequency response of mathematical model, simulation and experiment. 88

Figure 4-18. APF experimental results with (a) linear (b) nonlinear load. 89

Figure 4-19. DVR results for voltage flickering of 6Hz (a) 100 ms/div (b) 20 ms/div. 90

Figure 4-20. DVR results for (a) over voltage 135V (b) under voltage 90V. 91

Figure 4-21. Voltage sag waveforms in time scale of (a) line cycle, and (b) switching cycle. 91

Figure 4-22. Voltage waveforms for input voltage swell. 91

Figure 5-1. An LED dimming system. 93

Figure 5-2. Proposed remote control VSC dimmer system. 95

Figure 5-3. Dimming techniques (a) AM (b) PWM. 96

Figure 5-4. Standard TRIAC-dimmer lighting system. 98

Figure 5-5. 0-10V dimmer system. 100

Figure 5-6. DALI dimmer system. 100

Figure 5-7. Wireless dimmer system. 100

Figure 5-8. Example of dimming profile for street lighting system. 102

Figure 5-9. Modified TL-UPQC control strategy for the addition of dimming function. 103

Figure 5-10. Equivalent circuit of VSC dimmer system. 103

Figure 5-11. Phasor diagrams of VSC dimmer system under a dimming level (a) steady-state (b) voltage swell (c) voltage sag. 105

Figure 5-12. Power flow under a dimming level (a) steady-state (b) voltage swell (c) voltage sag. 105

Figure 5-13. System architecture of communication and interface..... 106

Figure 5-14. Small-signal model the VSC dimmer system control scheme. 108

Figure 5-15. Estimated loss in 500VA, 120V VSC dimmer system. 109

Figure 5-16. Estimated Efficiency of the VSC dimmer system under various dimming levels, 20%, 50% and 80% of rated illuminance..... 109

Figure 5-17. Testbed setup. 110

Figure 5-18. Waveforms at 50% illuminance with (a) TRIAC-based dimmer (b) VSC dimmer system. 111

Figure 5-19. Power quality measurements comparison (a) THD of input current (b) THD of lamp voltage (c) PF (d) efficiency (e) output/input power (f) input VA. 112

Figure 5-20. 70% dimming level under voltage sag and voltage swell. 114

Figure 5-21. Webpage GUI for dimming lighting systems. 115

Figure 5-22. Webpage Light intensity feedback signal. 115

Figure 5-23. Desktop application for dimming lighting systems. 116

Figure 6-1. TL-UPQC topology for voltage regulation in LV Distribution Network. 119

Figure 6-2. Phasor diagrams of (a) PFC mode (b) capacitive mode (c) inductive mode. 121

Figure 6-3. A block diagram of power flow in a TL-UPQC system. 122

Figure 6-4. Control block diagram of the enhanced control methodology. 125

Figure 6-5. Small-signal block diagram of the dc voltage loop. 129

Figure 6-6. Small-signal block diagram of the ac voltage loop. 130

Figure 6-7. Frequency response of the dc voltage loop without a compensator. 133

Figure 6-8. Frequency response of the dc voltage loop including a compensator. 133

Figure 6-9. Frequency response of the ac voltage loop including a compensator. 133

Figure 6-10. Experimental test block diagram. 135

Figure 6-11. Laboratory setup. 135

Figure 6-12. Block diagram of PLL implantation in DSP. 137

Figure 6-13. System waveforms for nonlinear loads at the load bus (a) without TL-UPQC (b) with TL-UPQC. 140

Figure 6-14. System waveforms during an under voltage for linear loads at the load bus (a) without TL-UPQC (b) with TL-UPQC. 141

Figure 6-15. System waveforms during an over voltage for linear loads at bus B (a) without TL-UPQC (b) with TL-UPQC. 141

Figure 6-16. Waveforms with TL-UPQC system ($Ssag = ON$) (a) a sudden load change at PCC bus (b) with rapid voltage fluctuation. 141

Figure 7-1. Conventional central D-STATCOM architecture. 144

Figure 7-2. Proposed modularized distributed TL-UPQC systems architecture. 144

Figure 7-3. Topology and structure of an individual TL-UPQC system. 146

Figure 7-4. Control scheme of parallel operation of distributed TL-UPQC systems. 152

Figure 7-5. Small-signal control block diagram of CC and one LC. 156

Figure 7-6. Frequency response of the dc voltage loop gain ($TOLd$) and the ac voltage loop gain ($TOLq$) 159

Figure 7-7. Nyquist diagram of the ac voltage loop gain without communication effect $TOLq(s)$. 159

Figure 7-8. Nyquist plot of the ac voltage loop gain under various communication delays $TOLq'(s)$. 159

Figure 7-9. Impulse sampling representation of ZOH. 161

Figure 7-10. Frequency response of ZOH. 161

Figure 7-11. Marginally stable Nyquist plot of the ac voltage loop. 163

Figure 7-12. Controller hardware-in-the-loop (CHIL) testbed. 165

Figure 7-13. System implementation using CHIL with RTDS. 165

Figure 7-14. PFC mode (experimental results with (a) linear (b) nonlinear load – LED lamps (c) nonlinear load – rectifier bridge circuit. 167

Figure 7-15. GUI - control center panel. 170

Figure 7-16. Steady-state waveforms for (a) capacitive mode (b) inductive mode. 170

Figure 7-17. Steady-state waveforms captured in RTDS for (a) capacitive mode (b) inductive mode. 171

Figure 7-18. Dc link measurements as captured in RTDS. 171

List of Abbreviations

1P2W	Single-phase two-wire
3P3W	Three-phase three wire
3P4W	Three-phase four wire
ADC	Analogue to digital converter
AlGa	Aluminum Gallium arsenide
AM	Amplitude modulation
APF	Active power filter
BCSSS	Boundary control with second order switching surface
CC	Central controller
CFL	Compact fluorescent lamps
CHIL	Controller hardware-in-the-loop
CLA	Control low accelerator
CM	Common-mode
CSC	Current source converter
CSI	Current source inverters
DALI	Digital addressable lighting interface
DER	Distributed energy resources
DG	Distributed generation
DSP	Digital signal processer
D-STATCOM	Distribution static synchronous compensator
DVR	Dynamic voltage restorer
E-Caps	Electrolytic capacitors
EMI	Electromagnetic interference
ePWM	Enhanced pulse width modulation
FACTS	Flexible ac transmission systems
FB	Full-bridge
FPGA	Field-programmable gate array
GaN	Gallium Nitride
GaP	Gallium phosphide
GPIO	General-purpose input/output
GTAO	Giga-transceiver analogue output
GTDI	Giga-transceiver digital input
GUI	Graphical user interface
HB	Half-bridge
HBVSI	Half-bridge voltage source inverter
HID	high-intensity discharge
HPF	High pass filter

HPS	High pressure sodium
HPS	Hypertext transfer protocol
IGBT	Insulated-gate bipolar transistors
InGaN	Indium Gallium Nitride
IP	Internet protocol
ISR	Interrupt service routine
LC	Local controller
LED	Light emitting diode
LPF	low pass filter
LV	Low voltage
MMC	Multi-modular converter
MV	Medium voltage
OLED	Organic light emitting diode
PCC	Point of common coupling
PF	Power factor
PFC	Power factor correction
PLL	Phase locked loop
PQ	Power quality
PV	Photovoltaic
PWM	Pulse width modulation
rms	Root-mean-square
RTDS	Real time digital simulator
SCR	Short circuit ratio
Si	Silicon
SiC	Silicon Carbide
SPI	Serial peripheral interface
SRF	Synchronous reference frame
SSH	Secure shell
SSL	Solid-state lighting
STATCOM	Static synchronous compensator
THD	Total harmonic distortion
TL-UPQC	Transformerless unified power quality conditioner
UART	Asynchronous receiver/transmitter
UPFC	Unified power flow conditioner
UPQC	Unified power quality conditioner
UPQC-DG	Distributed generation unified power quality conditioner
UPQC-L	Left unified power quality conditioner
UPQC-R	Right unified power quality conditioner
UPS	Uninterruptible power supply
VSC	Voltage source converter
VSI	Voltage source inverters
WBG	Wide bandgap

Chapter 1 Introduction

1.1 Background

Increasing advances in smart grid technologies aim for a more efficient and reliable network. Following the widespread use of solid-state controls for power conditioning, power quality (PQ) has become a significant issue. Currently, the practice of achieving high PQ standards is very challenging due to the extensive employment of power electronics-based appliances. Poor PQ will ultimately influence various sectors including industrial processes, essential services, residential applications, commercial investments, etc. Equipment may malfunction or be damaged during a voltage sag or a voltage swell. Besides, loads based on advanced electronic devices are very sensitive to PQ variations, which directly affect many customers. Therefore, both the utility and consumers require high demand for improved PQ parameters.

Manitoba Hydro has set certain standards to deliver a reliable and a high quality power service to every customer whose lines are connected to their network [1]. However, the company has been striving to achieve a flicker free network after receiving 57 reports of blinking LED street lights across the province [2]. In addition to the concerns that light flicker could trigger seizure for people with certain medical condition. Light flickering is frequently recounted in cities with large steel industry, since electric arc furnaces represent a major source of voltage fluctuations happening in

the network as indicated in Figure 1-1 [3].

In this chapter, PQ definitions and terms that are used in the conducted research are presented. Causes and effects of PQ issues are discussed. A quick overview of PQ standards and measurements are given. The motivation of the conducted research is highlighted followed by research objectives, author contributions and the organization of this thesis.

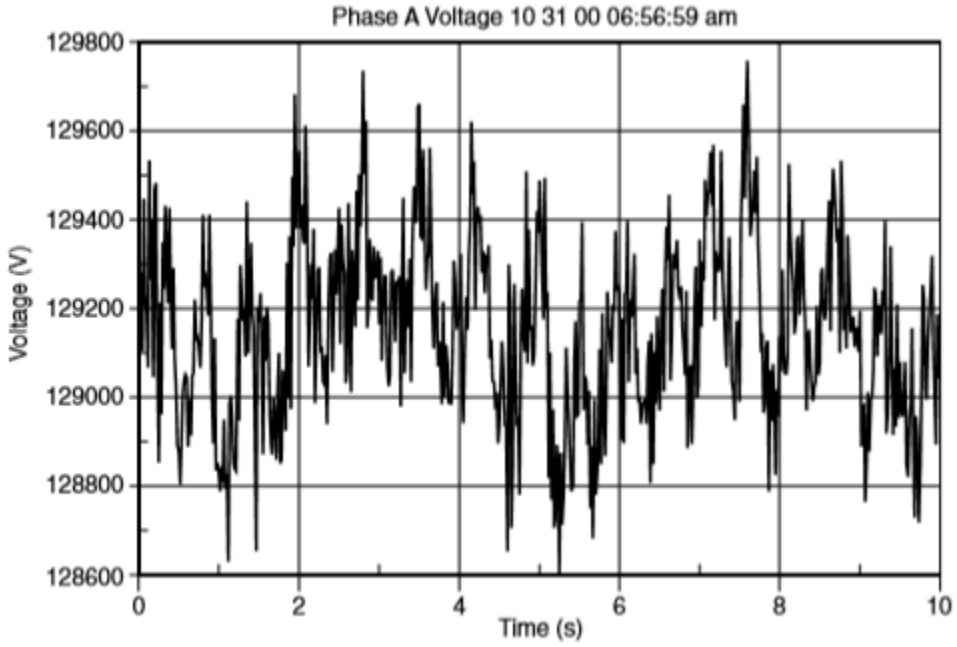


Figure 1-1. Voltage fluctuations of 230 kV substation supplying an electric arc furnace load [3].

1.2 Overview of Power Quality Definition and Standards

According to [3], PQ is mainly a consumer driven issue and can be defined from the user point of view as “any power problem revealed in voltage, current, or frequency deviations, that results in failure or malfunction of customer equipment”. It can also be defined as “the characteristics of power supply that enable the equipment to work properly”.

PQ issues are related to both voltage quality and current quality. There are international standards that have been formalized to define the guidelines of the power quality characteristics that customers should expect from their local electric utility. IEC and IEEE are the main organizations for PQ standards and requirements in the international community. Table 1-I gives most commonly standards of recommended practices for voltage and current characteristics. In general, PQ issues are classified into two main groups [4]; steady-state and disturbances as illustrated in Figure 1-2. The steady-state category is specified for continuous and periodic characteristics (voltage regulations, i.e. long duration voltage variations, unbalance, harmonics and flickering). On the contrary, disturbance appears randomly and occurs for a short time (transients, short duration voltage variations and interruptions). PQ causes and their consequences are summarized in the following subsection [3].

TABLE 1-I POWER QUALITY STANDARDS

Standard	**Specification**
IEEE 1159	Provides power quality definitions, terms description and general guidelines
EN 50160	Specifies voltage characteristics provided by the supplier in public distribution systems
IEEE Std 1547	Provides technical requirements and specifications regarding distributed resources.
IEC 61000-3-2	Specifies harmonic currents injection limitation into the public grid
IEEE 519	Gives recommended practices of voltage and current harmonics in electric power systems
IEC 61000-3-3	Sets limitation of voltage fluctuations and flickering reverted on the public grid
IEC 61000-4-15	Identifies design specifications for flickering measuring techniques and devices
IEEE PAR1789	Addresses human biological effects due to visible and invisible light flicker

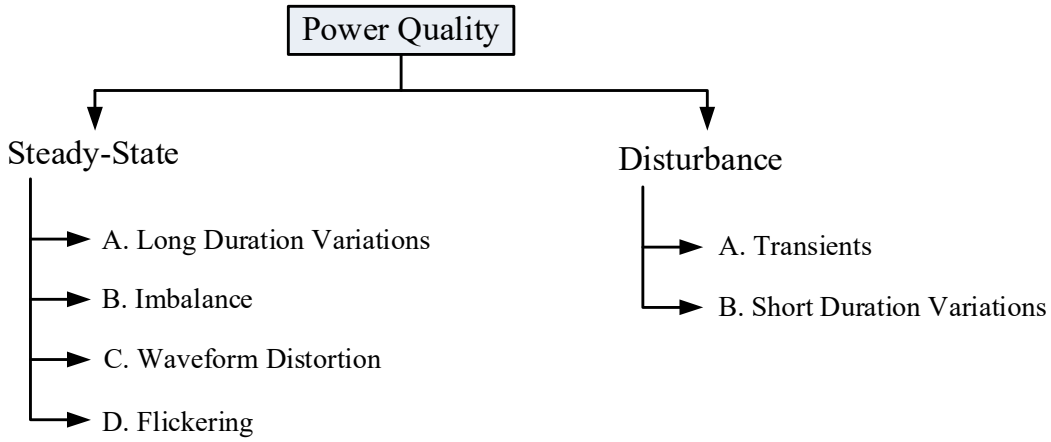


Figure 1-2. Power quality problems classification [4].

1.2.1 Power Quality Steady-State Issues

A. Long Duration Voltage Variations

As stated by IEEE Standard 1159 [6], long duration root-mean-square (rms) voltage variations are deviations in voltage that last for longer than 1 min. These variations are either over voltages or under voltages. Typical values for an over voltage are between 1.1 to 1.2 pu, while an under voltage is a decrease in the rms voltage, typically ranges between 0.8 to 0.9 pu. The supply voltage characteristic according to EN 50160 [7] should be within ±10% of its nominal value for 95% of the week. Protection circuit breakers should be designed to trip when the system voltage exceeds these limits. IEEE Std 1547 [8] sets the maximum acceptable voltage deviation caused by a distributed generation (DG) unit to be $\pm 5\%$ at PCC.

Causes: load changes and utility faults. Over voltages are caused by switching off heavy loads or connection of a large capacitor bank. On the other hand, switching on large loads, and overloaded networks are the cause of under voltages.

Consequences: reduced lifetime of equipment, system shutdown and loss of data.

B. Imbalance

Imbalance, also called unbalance, is a PQ problem related to both voltage and current in a three-phase system. It is defined in ANSI C84.1 [9] as "the maximum deviation from the average of the three-phase voltages or currents, divided by the average of the three-phase voltages or currents, expressed in percent". The imbalance is calculated in IEEE Standard 1159 as follows,

$$\%Imbalance = \frac{V_{neg}}{V_{pos}}\ x\ 100\ \% \tag{1. 1}$$

where, V_{neg} is the magnitude of the negative sequence components and V_{pos} is the positive sequence component.

In general, a voltage/current unbalance in a three-phase system is a phenomenon in which the three voltage/current magnitudes or the phase-angle differences between them are not equal. The maximum voltage unbalance recommended by ANSI C84.1 under no load conditions is 3%. The limit specified by EN 50160 should not exceed 2% for normal system and 3% for systems with single-phase loads.

Causes: unequal single-phase loading in a three-phase system. Faults results in broken fuses of one phase of a three-phase capacitor bank.

Consequences: negative sequence induced into the system, which is harmful to three-phase loads. Heating and failure of loads.

C. Waveform Distortion

A waveform distortion is a deviation from the ideal sinusoidal waveform. This deviation is characterized by the spectral content of the waveform, which contains dc offset, harmonics, interharmonics, notching and noise [1]. Voltage and current harmonics are the primary concern of the PQ of the network. Harmonic components are sinusoidal components with frequencies that are equal to integer multiples of the fundamental frequency (usually 50 or 60 Hz). Fourier series can represent a distorted periodic waveform by an infinite number of sinusoidal waves, which contain the fundamental frequency and the harmonics components. Nonlinear loads create harmonic currents. The interaction of harmonic currents with the system impedance will cause harmonic voltage distortion. The term total harmonic distortion (THD) is used to measure the distortion factor of a waveform with respect to its fundamental component. The THD of current THD_i and voltage THD_v are calculated using the following expressions respectively,

$$THD_i = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \tag{1. 2}$$

$$THD_v = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \tag{1. 3}$$

where, h is harmonic order, $I_h \; and \; V_h$ are rms value of the harmonic component order n of current and voltage respectively, while $I_1 \; and \; V_1$ are rms value of the fundamental component of current and voltage respectively.

IEC 61000-3-2 [10] and IEEE 519 [11] standards are widely adopted recommendations practice for harmonic control in electric power systems. IEEE 61000-3-2 provides limitation of harmonic current emissions that are being injected into the public grid. This standard is applicable

for equipment connected to the low voltage (LV) distribution network with a 16 A per phase. For each individual harmonic current component, a certain percentage of the fundamental current limit is set. IEEE 519 provides guidelines for voltage as well as current harmonic emissions. For bus voltage below 1 kV, the maximum THD in voltage distortion is 8%, while it is 5% for bus voltage between 1 kV and 69 kV. The current THD considering harmonic components up to the 50th order excluding interharmonics is limited to 5%.

It is noteworthy that lower THD in power systems will result in higher power factor (PF) and higher efficiency. The term power factor is the ratio of the total power input in watts to the total apparent power in VA. PF is calculated using the following expression [12],

$$PF = \frac{1}{\sqrt{1+THD_i^2}} \cos(\theta_v - \theta_i) \tag{1.4}$$

Where, $\theta_v - \theta_i$: is the phase difference between voltage and current.

For linear loads, the PF will be equal to $\cos(\theta_v - \theta_i)$. This is not the full definition of power factor and is called displacement power factor. The displacement power factor is only true if both voltage and current waveforms are sinusoidal. Therefore, PF is calculated in terms of distortion factor and displacement power factor.

Causes: nonlinear loads such as arc furnace, arc welder, all power electronics equipment, switched mode power supply, adjustable speed drives, and LED lamps.

Consequences: overheating in cables and equipment, high core and copper losses in motors and transformers, lower efficiency, and electromagnetic interference (EMI) with communication systems.

D. Flickering

Flickering is a voltage fluctuation with regular variation. It is defined as "a series of random or continuous voltage changes" [3]. Voltage magnitude changes and the frequency by which the change take place are used to characterize the flickering phenomenon [4]. The term flicker is derived from the impact of voltage changes on the variation of the light intensity of lamps in a way that will be perceived by the human eye. Flickering at certain frequencies have direct human health risks that have been addressed by IEEE PAR1789 [13]. IEC 61000-3-3 [14] specifies limitation of voltage fluctuations in LV distribution network, while IEC 61000-4-15 [15] sets the international standard to design apparatus (flickermeter) for flickering measurements. The flickermeter gives two measurements, short-term flicker severity (P_{st}) for a period of 10 min and long-term flicker severity (P_{lt}) that takes an evaluation time of 12 consecutive short-term flicker severity index. According to IEC 6100-3-3 the flicker perception level of the P_{st} index and the P_{lt} should not exceed 1 and 0.65 respectively, in order to comply with the user's preferences for a comfortable environment.

Causes: arc furnace, arc welder and frequent start/stop of heavy loads.

Consequences: Visual perception of flickering for various lighting sources.

1.2.2 PQ Disturbances Issues

A. Transients

Transient is a fast change in voltage or current. Transients can be measured by the peak magnitude, the rate of rise or the change of a waveform from one operating point to the next operating point. Transients are classified into impulsive and oscillatory transient. Impulsive

transient is a unidirectional sudden change in the steady-state condition of voltage/current. In contrast, oscillatory transient is a bidirectional sudden change in the steady-state condition of voltage/current [1], [4].

Causes: Switching of capacitive or inductive loads, lighting surge and utility fault clearing.

Consequences: Loss of data and possible damage.

B. Short Duration Voltage Variations

Short duration voltage variations are changes in voltage magnitude that last less than 1 min as defined in IEEE 1159 standard. These variations are temporary, and it can be either an increase (voltage swell), or a decrease (voltage sag) in voltage magnitude or a total loss of voltage supply (interruption). According to EN50160 standard, a voltage dip (sag) is a sudden decrease in rms voltage between 0.1 to 0.9 pu for durations from 0.5 cycle to 1 min. Whereas, a voltage swell is a sudden increase in rms voltage between 1.1 to 1.8 pu for duration from 0.5 cycle to 1 min. An interruption occurs when the supply voltage decreases to lower than 0.1 pu of the nominal voltage.

Causes: A fault in the power system, utility failure, component failure, starting of heavy loads and large motors.

Consequences: Circuit breaker tripping, loss of data, equipment damage, short lifetime and malfunction.

1.3 Motivation and Research Objectives

Consequent to recent developments in the technology of solid-state lighting (SSL) and hence light emitting diode (LED) lamps, high luminous intensity LEDs are now taking a significant share

of the lighting sources market. It is well known that the main advantages of utilizing LED lamps are long lifetime and low energy consumption compared to conventional lighting technologies, such as incandescent lamps and florescent lamps [16], [17]. However, some low-cost LED lamps inject harmonic currents into the grid, which affect the power system network especially in a large-scale lighting system such as a street lighting network and a parking building lighting network [18]. In addition, LED lamps are sensitive to power system disturbances like voltage sags and voltage flickering. Even though a voltage sag lasts for few milliseconds it may cause the lamp to flicker or even get damaged in some cases. This is particularly important for lighting networks, which are located near electric arc furnaces [19], since light intensity changes rapidly in response to voltage flickers.

The work done in this thesis is intended to develop a comprehensive solution for most power quality problems related to modern lighting loads. The ultimate goal is to remove flickering on LED lighting networks, which is a major concern to many users, and to enhance the overall electric power quality at distribution levels. Specific objectives followed in this research can be listed as follows,

- Review PQ standards and existing active power filter (APF) topologies to fulfill these standards in LV distribution networks.
- Review LED lamp technology including LED drivers, LED PQ standards and LED dimming techniques.
- Characterize and analyze different aspects of the behavior of commercial LED lamps to comprehend the main causes of PQ issues linked to LEDs utilization. This characterization is essential before developing a solution that limits LEDs influences on

system PQ parameters.

- Employ APF as a promising solution for PQ problems related to LED lighting networks. The system is intended to,
  a) Mitigate voltage flickering, by maintaining the voltage across the LEDs at a constant amplitude.
  b) Achieve a high dynamic response to be able to compensate for voltage sags and swells which are interpreted by the LEDs as a dimming request causing light flickering.
  c) Improve the PF and reduce the THD of the input current by eliminating harmonic components injected by LEDs.
  d) Allow amplitude voltage control to achieve light dimming and endorse energy saving.
  e) Provide input grid voltage support and improve the overall stability of the grid.
- Design and implement a transformerless unified power quality conditioner (TL-UPQC) to mitigate current and voltage quality problems as discussed in the previous point.
- Validate the proposed topology through conducting various experimental tests while emulating PQ problems happening in the network.
- Develop a remote management central dimming technique for LED lamps applying the same power electronic apparatus.
- Maximize functions of the TL-UPQC system and extend its feature to deliver reactive power compensation for input grid voltage regulation.

- Provide stability analysis and design guidelines for the TL-UPQC system control methodology to achieve a desired performance including control system bandwidth and phase margin design.
- Formulate a suitable secondary control strategy that manages parallel operation of modularized TL-UPQC converters to improve grid voltage stability. The control methodology should cope with the new developments and structure of smart grid applications.

This thesis proposes a single-phase transformerless active power filter topology to achieve the goal of PQ improving for LED lighting networks. The apparatus serves as a power quality conditioner that is connected between the ac supply and LEDs. The proposed TL-UPQC mitigates most of voltage and current problems. It solves flickering phenomenon happening in the network. The system's control methodology attains stability and fast dynamic response for short disturbance. It should be emphasized that there is currently no developed solution for this problem in the literature or the market. A hardware prototype has been built to verify the theoretical findings with the experimental results. Steady-state and dynamic analysis have been performed.

1.4 Thesis Layout

This thesis is comprised of 8 chapters. The contents of the remainder of this thesis are briefly described as follows,

In chapter 2, since a unified power quality conditioner (UPQC) system has been adopted as the solution to solve PQ issues in LED lighting networks, this chapter focuses on reviewing UPQC topologies and control strategies. Grid voltage regulation techniques that have been proposed in

the literature are also presented. In addition, parallel operation of modular converters is reviewed and discussed.

In chapter 3, a broad analysis of the main PQ issues related to the use of LEDs is presented. An overview of LED lamps technology is given including the structure, LED drivers and international regulations of LED lighting industry. PQ problems related to LEDs are discussed with proposed solutions in the literature. Then, the methodology followed in this research to evaluate the performance and the behavior of LEDs, laboratory setup description and experimental results are presented in detail.

In chapter 4, a comprehensive power quality conditioner, which is the TL-UPQC system is introduced. The topology's principle of operation and implementation are described. Stability of the designed controllers is analyzed by small-signal modeling technique and verified experimentally with a gain-phase analyzer. The chapter also presents a derived set of generalized equations to size the UPQC system. A description of the laboratory prototype along with experimental results to validate the operation of the TL-UPQC as a power quality conditioner is presented.

In chapter 5, the functions of the topology presented in Chapter 4 are extended to include a dimming function to LED lamps. The chapter reviews existing dimming techniques in the literature and the market to highlight the advantages of the proposed dimming technique. The implementation of the remote management system and data acquisition are explained. Small-signal characteristics and the influence of communication delay on system stability are analyzed. Experimental results and power analysis comparison between utilizing the TRIAC-based dimmer and the proposed TL-UPQC dimmer system for dimming function are conducted and discussed.

In chapter 6, the TL-UPQC will perform as a distribution static synchronous compensator (D-STATCOM) to provide reactive power support to the input grid, in addition to the features that have been presented in Chapter 4 and Chapter 5. The enhanced control strategy is developed in accordance to the controller design criteria. Three different modes of operation are analyzed according to the power flow analysis between the TL-UPQC system and the grid. System modeling for each control loop is studied. The laboratory prototype is applied to validate the proposed enhanced feature.

In chapter 7, parallel operation of distributed TL-UPQCs connected to low voltage distribution networks is proposed. The operation is intended to improve the grid voltage profile while considering the connected modules rated capacity. An advanced control technique that allows monitoring, wireless communication and coordination between the connected modules is presented. The proposed control methodology is evaluated by controller hardware-in-the-loop approach, where the power stage is simulated in a real time digital simulation, while the control algorithm is developed in a digital signal processor. Experimental results including random behavior of a photovoltaic system are presented.

In Chapter 8, the main points of this thesis are concluded. Future work recommended to further continue this research study is discussed.

Chapter 2 Literature Review of Power Quality Mitigation in Distribution Networks

2.1 Introduction

Nowadays, power electronic based devices signify a potential solution to maintain high PQ in modern power systems. While, flexible ac transmission systems (FACTS) are used to enhance the PQ in the ac transmission line networks, APFs mitigate harmonics and voltage disturbances in distribution networks. The principle of operation of an APF is to inject an equal and an opposite voltage/current to compensate the actual disturbance. There are three types of APFs: shunt, series and a combination of both. Shunt APF injects current into the grid to compensate for load current harmonics and reactive power consumption. On the other hand, series APF injects voltage to mitigate voltage disturbances propagating in the network, such as flickering, voltage swells and voltage sags. A UPQC is a combination of series and shunt active filters. Therefore, it is a cost effective and a comprehensive solution to suppress PQ issues that are related to both voltage and current disturbances. Therefore, the UPQC topology has been selected as the solution to compensate for voltage/current related problems existing in an LED lighting network.

2.2 UPQC - State of Art

A literature review on UPQC topologies to improve the PQ of the network has been reported in [20]. A general block diagram of a UPQC topology is shown in Figure 2-1. It consists of two

inverters, a shunt inductor L_P and an LC filter. The shunt inductor connects the shunt inverter to the system and injects current to the network. The LC filter is a low pass filter (LPF) that cancels high frequency switching ripples in the inverter output voltage. The two inverters share a common dc link. A series transformer is required to step down the voltage or the current of the series inverter.

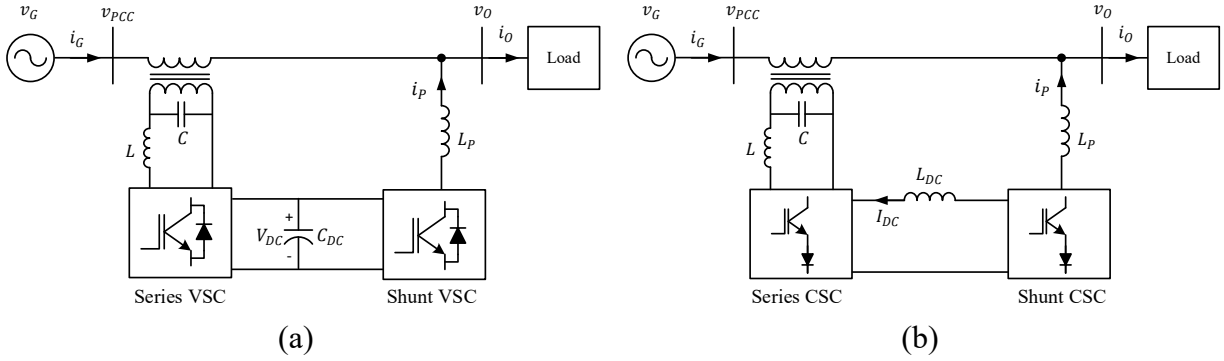


Figure 2-1. General block diagram of UPQC topology (a) VSC (b) CSC.

2.2.1 Classification of UPQC Topologies

Figure 2-2 shows classification of UPQC topologies according to a) converter topology; voltage source converter (VSC) or current source converter (CSC) b) supply system; single-phase or three-phase system c) UPQC configuration that takes various converters configuration including shunt location, energy storage integration, interline, multi-converter and multi-modular converter (MMC) topologies [20].

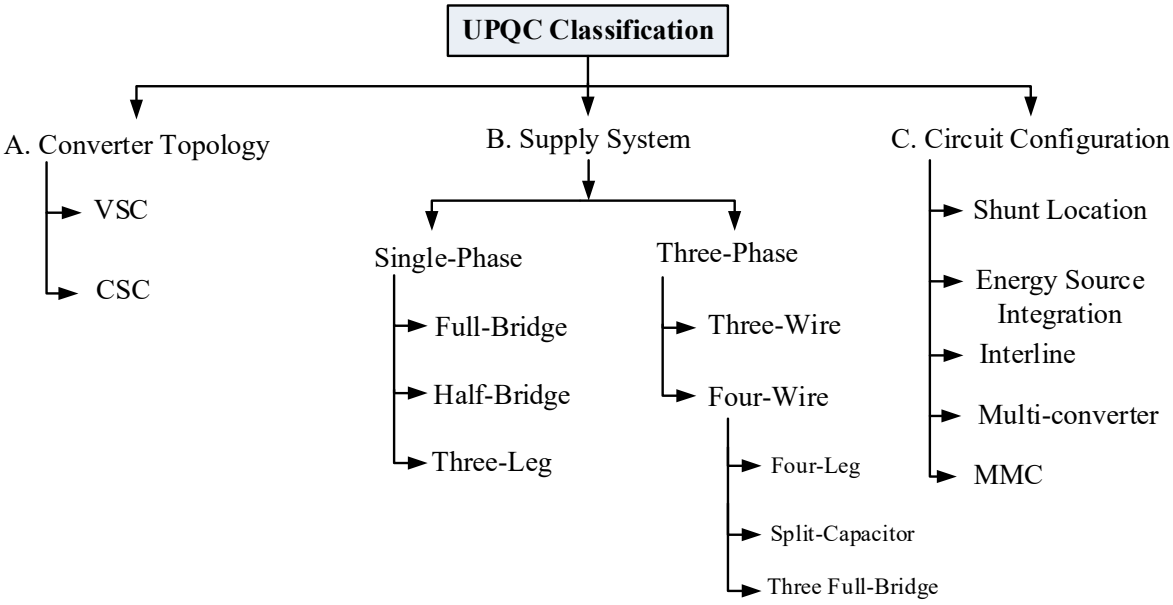


Figure 2-2. Classification of UPQC [20].

A. Converter Topology

The most adopted converter topology is the VSC topology, which is shown in Figure 2-1 (a) [21], [22]. It consists of two voltage source inverters (VSIs) with a common energy storage capacitor C_{dc} as its dc link. The VSC is a cost-effective topology and offers the ability of multilevel operation for high voltage application. Nevertheless, the electrolytic capacitor limits the lifetime of the converter. Figure 2-1 (b) depicts the second topology, which is based on a CSC topology [23], [24]. In this topology, two current source inverters (CSI) share a common reactor L_{dc}. The CSC topology has an inherent protection capability against short circuits. However, it requires series connection of blocking diodes, which leads to high on-state losses. Moreover, high dc link losses are associated with the use of a bulky inductor.

A comparison study between VSC and CSC shunt active power filters has been investigated in [25]. It was concluded that both voltage and current source shunt active filters are effective for

filtering harmonics. The THD_I of the input current was less than 5% for both topologies. The major contribution of losses in the CSC topology was the dc link reactor. Whereas, the main source of losses in the VSC topology, was found to be the ac filter. The efficiency of the VSC topology was found to be higher than the efficiency of the CSC topology at nominal operating point. In addition, the CSC topology requires a separate clamp circuit for overvoltage protection, which adds complexity to the main circuit.

B. Supply System

UPQC systems are classified according to the input supply. The input source can be a single-phase or three-phase supply. Voltage and current unbalance compensation are additional PQ problems to be mitigated in a three-phase system. Other voltage and current related PQ problems are similar for both single and three-phase systems.

A conventional single-phase two-wire (1P2W) UPQC system topology comprises of two full-bridge (FB) converters as shown in Figure 2-3 (a) [26], [27]. It consists of eight switching devices, which increases the number of gate drivers as well as the conduction losses compared to other topologies. Though, as an advantage, a smaller filter size can be used if a unipolar switching technique is employed. A UPQC topology that is based on two half-bridge (HB) converters is shown in Figure 2-3 (b). The configuration requires less number of switching devices. It consists of two legs, one leg each for shunt and series inverters. This configuration has fewer semiconductor device counts. Nevertheless, it requires higher dc link voltage and higher breakdown voltage for semiconductors. Three-leg single-phase UPQC topology has been proposed in the literature [29]. It consists of six switches as shown in Figure 2-3 (c). Two HB converters are used; one leg (switches $S_1 \& S_2$) is for the series inverter and one leg (switches $S_3 \& S_4$) is for the shunt inverter,

while the third leg (switches S_5& S_6) is common between the two inverters. This configuration offers a compromise between the number of switching components, dc voltage and filters size.

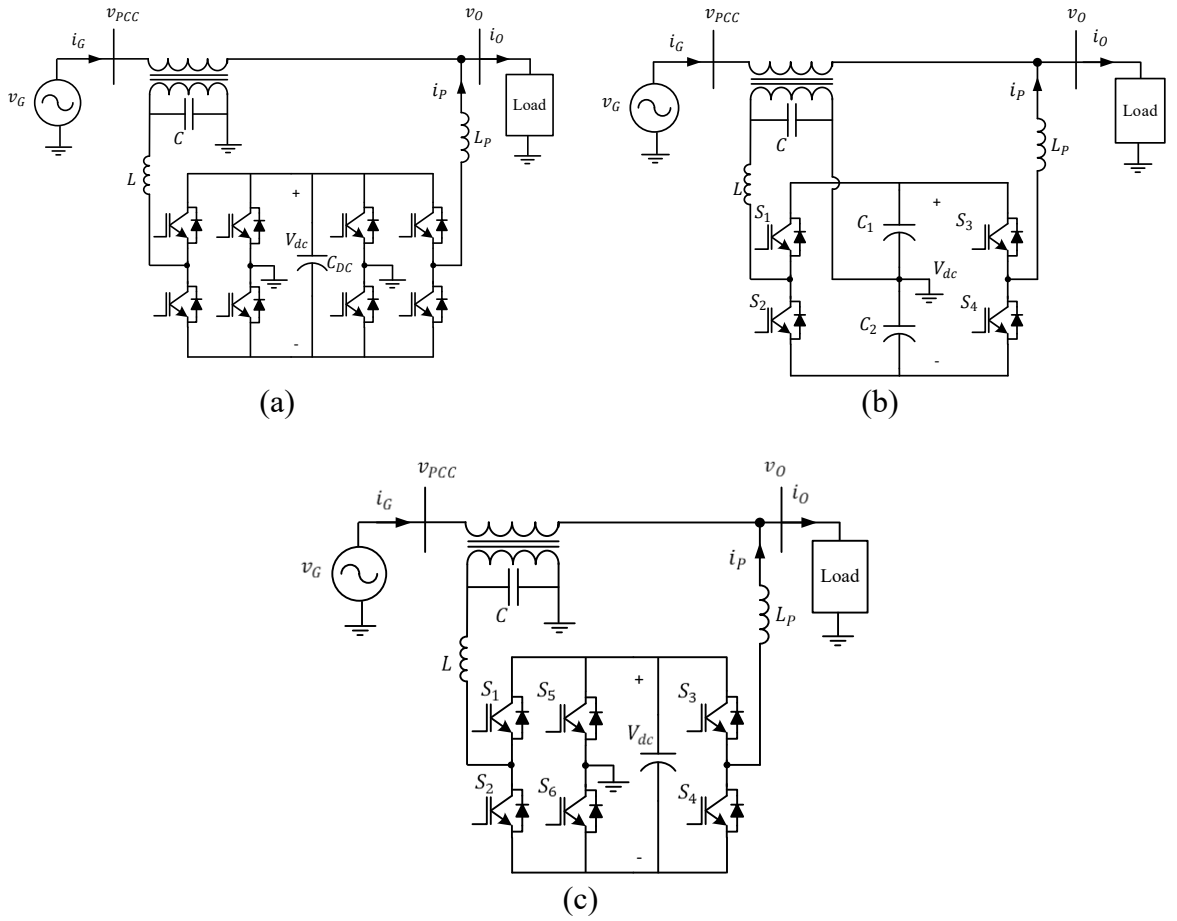
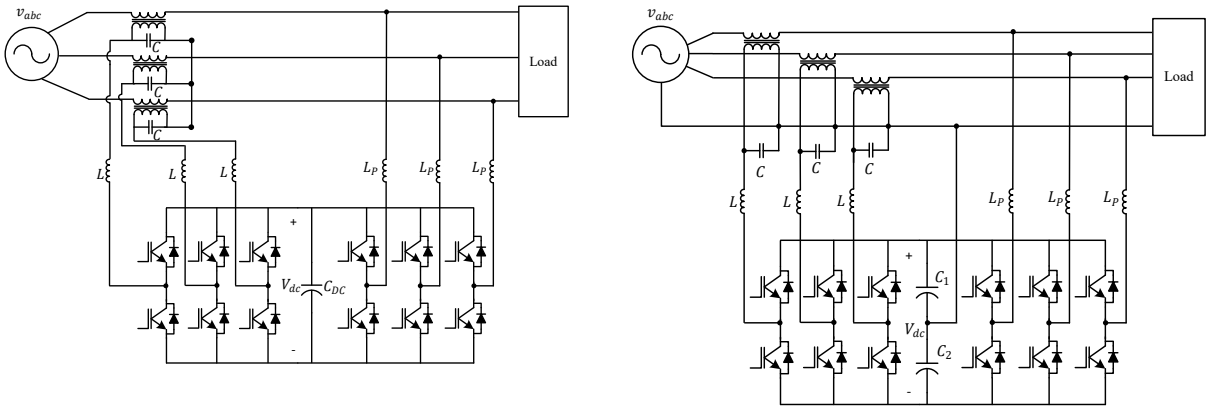


Figure 2-3. (a) 1P2W FB UPQC topology (b) 1PP2W HB UPQC topology (c) 1P2W three-leg UPQC topology.

For a three-phase system, UPQC topology can be either three-phase three wire (3P3W) topology [30] as shown in Figure 2-4 (a), or three-phase four wire (3P4W) topology [31], [32] as shown in Figure 2-4 (b). 3P3W UPQC system is employed with industrial loads e.g. frequency converters, arc furnace, and arc welding machines, whereas 3P4W UPQC system is utilized with unbalanced three-phase loads or assortment of single-phase loads. Various three-phase topologies have been proposed [20], e.g. four-leg [31] and two-split capacitor [32] as in Figure 2-4 (b). A

single-phase to three-phase UPQC system has been proposed in [33]. This topology can be applied in rural or remote areas when only single-phase distribution system is accessible for economic reasons.



(a) (b)

Figure 2-4. (a) 3P3W UPQC topology (b) 3P4W UPQC topology.

C. Circuit Configuration

A UPQC system can be classified according to the location of the shunt converter with respect to the series converter. Right UPQC (UPQC-R) configuration is when the shunt converter is placed to the right of the series converter as shown in Figure 2-1. Left UPQC (UPQC-L) configuration is when the shunt converter is placed to the left of the series converter as shown in Figure 2-5. The UPQC-R configuration is more popular, as the shunt converter will guarantee a sinusoidal input current going through the transformer under different loading conditions. When harmonic currents go through a transformer, its ohmic losses and eddy current losses will increase [34] leading to temperature rise in the transformer.

Due to the reduction of fossil fuels energy sources, replacing conventional power generators with clean energy resources is now encouraged. Consequently, DG units based on renewable

energy sources are becoming widely utilized. Many researches propose the integration of DG with UPQC system (UPQC-DG) [35]-[37]. Energy source integration will allow the UPQC system to compensate for a power outage as well. The DG unit is connected to the dc link as an energy source through a suitable converter as illustrated in Figure 2-6 (a). The advantage of a UPQC-DG system over a conventional UPQC system is the capability to inject active power at the event of a voltage interruption. Loads connected to the point of common coupling (PCC) will continue to receive power from the DG unit. Moreover, the UPQC-DG system will be able to inject active power to the grid. A photovoltaic (PV) system integrated with a UPQC system has been proposed in [36], [37]. The PV UPQC-DG system is able to transfer power in both interconnected mode and islanded mode.

A battery can replace the DG unit in a UPQC system as shown in Figure 2-6 (b). In [38], [39], a combined super capacitor energy storage system and battery storage system has been proposed to compose an additional energy source to the UPQC system. The combined system is connected to the dc link through s bidirectional dc/dc converter. In this case, the topology will maintain the dc voltage constant and supply sensitive loads under power supply interruptions forming an uninterruptible power supply (UPS).

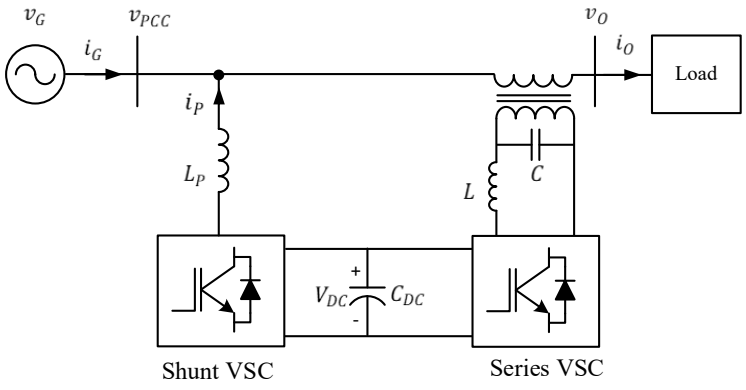
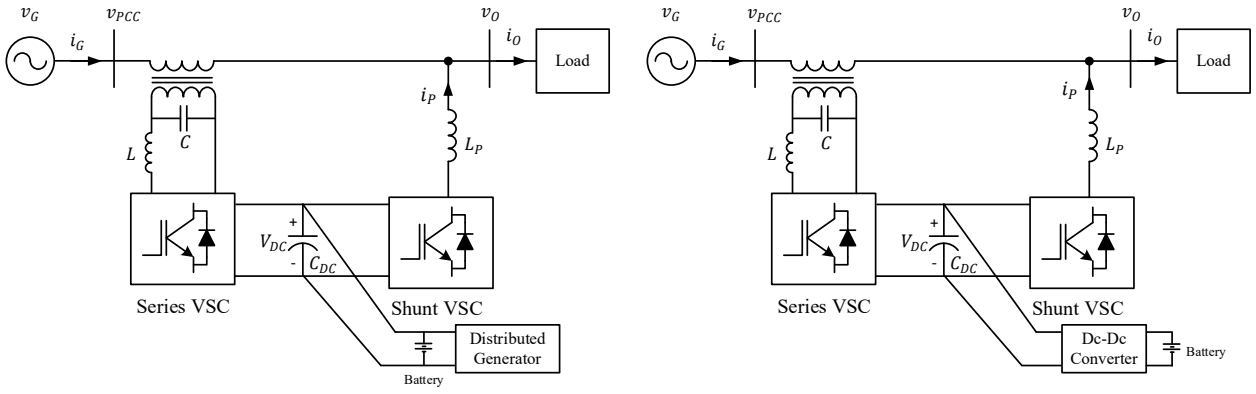
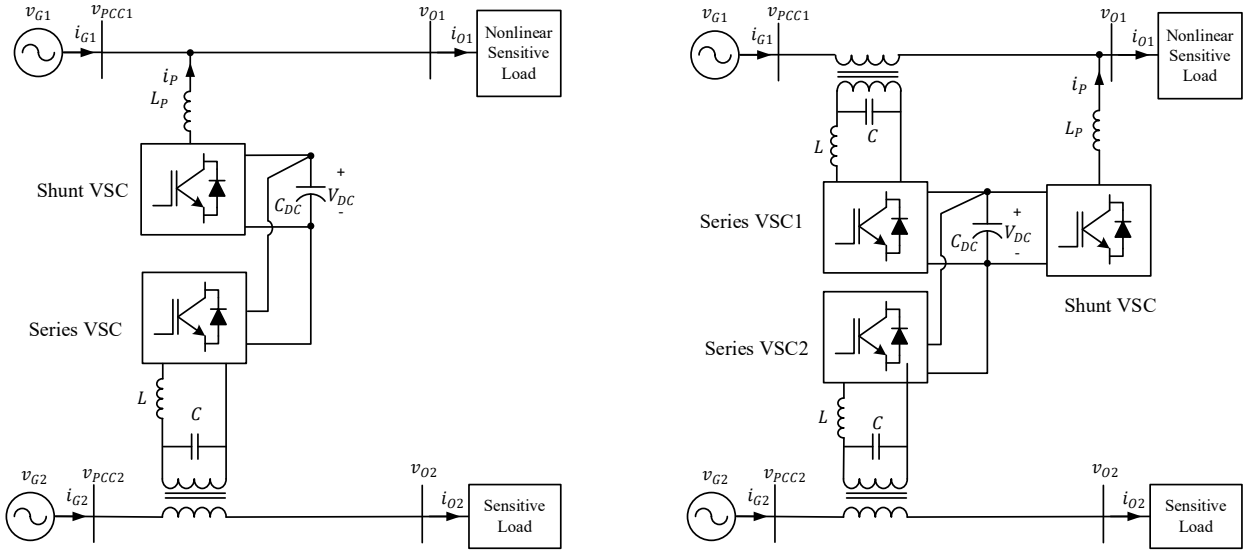


Figure 2-5. Left UPQC configuration.



(a) (b)

Figure 2-6. (a) DG unit integration with UPQC (b) Battery integration with UPQC.



(a) (b)

Figure 2-7. UPQC configuration with (a) interline (b) multi-converter.

The term interline has been introduced in the literature for both unified power flow conditioner (UPFC) and UPQC systems to control the power flow in two different transmission lines or distribution feeders as shown in Figure 2-7 (a) [40], [41]. The authors in [42], [43] has proposed a multi-converter UPQC topology as depicted in Figure 2-7 (b). The multi-converter topology extends the interline topology by connecting a third converter to improve the overall performance

of the UPQC system. For medium to high voltage levels, MCC UPQC system has been proposed [44], [45]. Adopting the MMC technology will reduce the voltage stress across the switching devices and enhance the quality of the output voltage waveform.

2.2.2 Transformerless UPQC topology

A conventional UPQC topology requires a series isolated transformer. Nevertheless, transformers are bulky, and add more cost and losses to the system. A transformerless FB UPQC topology for single-phase applications is presented in [46]. The authors highlighted the importance of considering the circulating current problem in the converter design. A transformerless three-leg UPQC has been proposed in [47]. Despite the fact that the topology has less switching and conduction losses compared to a FB UPQC topology, the shared leg introduce mutual coupling between the two converters. The authors in [29] has proposed a specific modulation control technique to deal with the coupling issue introduced by the shared leg. The topology introduces constrains in practical applications due to the presence of leakage current.

2.2.3 Series APF Compensation Control Strategy

As mentioned earlier in this chapter, the series APF compensates for voltage related problems and acts as a dynamic voltage restorer (DVR). One of the major power quality voltage related problem is voltage sag/swell. Three main voltage sag/swell compensation techniques have been reported in the existing literature. Figure 2-8 shows the phasor diagrams of these techniques.

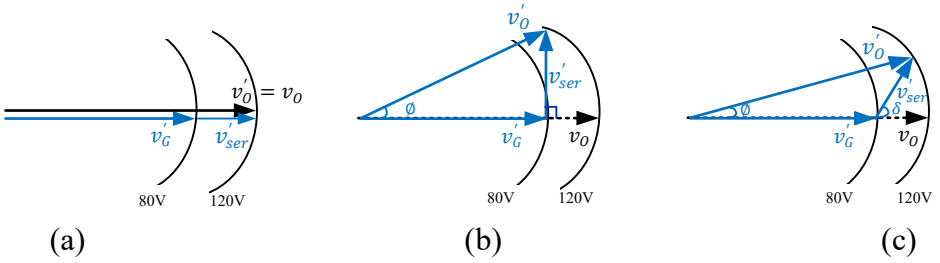


Figure 2-8. Phasor diagrams of DVR compensation methodologies (a) UPQC-P (b) UPQC-Q (c) UPQC-S

Active power control (UPQC-P) technique is the most common approach to compensate voltage disturbances [26]. This technique's concept is to inject/absorb a voltage v_{ser} in phase/out of phase with the main supply voltage through the series converter to mitigate a voltage sag/swell. The shunt converter under steady-state operation supplies the active power demand of the series converter. During a voltage sag (transient condition), the dc link supplies the series converter with the active power demand. The shunt inverter draws an equivalent active power to charge up the dc link voltage.

Reactive power control (UPQC-Q) technique has been employed in [30] to compensate for a voltage sag. The technique is based on injecting the series voltage v_{ser} that is in phase quadrature with the source current in UPQC-R or with the load current in UPQC-L. As the shunt APF maintain unity power factor, the energy injected by the DVR is minimum. A phase angle is created between the supply voltage and the delivered voltage in order to inject a quadrature voltage. Therefore, a larger injection voltage magnitude is needed than in a UPQC-P technique for an equal compensation of voltage sag.

Active reactive power control technique, donated by (UPQC-S), is a technique where the series converter delivers complex power. The authors in [48] has proposed minimum volt-ampere loading (UPQC-VA_{min}) technique during a voltage sag. The principle of operation for this

technique is to inject the series voltage v_{ser} in an optimal angle with respect to the source current.

In order to enhance the operation of the series APF under all condition, the authors in [49] has presented maximum VA loading approach. Similar to UPQC-VA_{min}, the injected voltage is controlled at an appropriate angle based on operational requirements. The series APF shares reactive power delivery with the shunt APF under steady-state and transient conditions. Consequently, the series converter loading will be maximized on the contrary to UPQC-VA_{min} technique. This technique will reduce the loading on the shunt APF as well as its VA rating. However, it employs several control loops, which adds complexity to the system controller.

2.2.4 Shunt APF Compensation Control Strategy

The shunt APF is mainly used for current harmonics mitigation caused by nonlinear lads connected to the PCC. The APF controller detects the harmonic contents in the load current and generates a reference current to oppose them. Once, the generated current is injected into the grid, the load harmonics current is suppressed, and the source current will contain only the fundamental component of the load current. The shunt APF is also used to deliver reactive power required by the load in order to achieve a voltage in phase source current with a unity power factor. There are various techniques that have been reported in the literature to generate the reference currents [50].

The instantaneous reactive power theory has been widely adopted in the literature. It is based on a mathematical calculation for the instantaneous active power (P) and reactive power (Q). The calculations are done in the time domain, where the load voltages and load currents are transformed to the d-q frame, from which the instantaneous load P and Q are calculated as follows,

$$P = v_d i_d + v_q i_q \tag{2. 1}$$

$$Q = v_q i_d - v_d i_q \tag{2. 2}$$

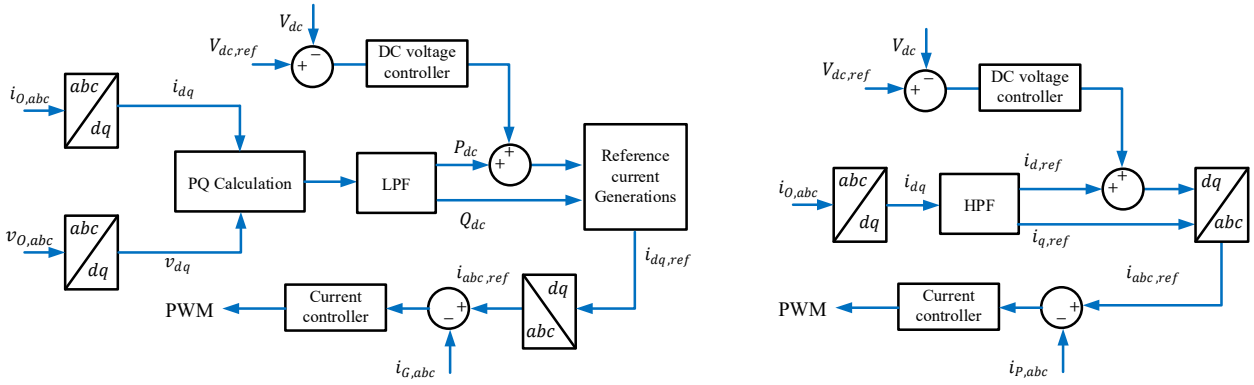
where, v_{dq} and i_{dq} are the d-q components of the load voltages and currents respectively.

p and q components are fed into a LPF to decompose the power into dc component an ac component. The dc components represent the power required by the connected load. In order to have a unity power factor, the dc component of the reactive power is set to zero while the dc power is added to the losses required by the converter to maintain the dc link voltage. Accordingly, the source reference currents are generated as shown in Figure 2-9 (a).

The second control methodology is the synchronous reference frame (SRF) technique, which relies on extraction the harmonic components of the load current in the time domain. Park transformation is used to transform the load current into the synchronous reference frame. The d-q components are fed into an LPF that filters out the high harmonic components. From there, the filtered d-q components are transformed back to the abc frame forming the current references to be compared with the source current from which the final switching signal are defined. In other techniques, a high pass filter (HPF) is employed to predict the harmonics components as shown in Figure 2-9 (b). In this case, the generated reference signals will be compared with the converter current i_P. In SRF the reference currents are derived directly sensing the load current without relying on the source voltages. Therefore, this control methodology is robust against input voltage distortion or voltage unbalance.

Frequency splitting has been adopted in [51], [52]. In this technique, the harmonic current and reactive power will be compensated separately with two converters. The converter with the high bandwidth will mitigate harmonics while the converter with the low bandwidth will provide the load reactive power demand. This control methodology lacks redundancy also a converter failure

will lead to a failure in meeting the controller objectives. This technique can be used for high power application to reduce the current stress and the overall losses of the converters.



(a) (b)

Figure 2-9. (a) Instantaneous reactive power control technique (b) Synchronous reference frame control technique.

2.3 Grid Voltage Regulation Techniques

Considerable work has been done adopting the advancement of semiconductor technology to provide grid voltage support [53]-[68]. Static synchronous compensator (STATCOM) is widely employed to provide line voltage regulation due to its large dynamic range and fast response under various operating conditions [53], [54]. A STATCOM is a semiconductor-based VSC that belongs to the FACTS family that is installed to enhance the grid voltage stability in ac transmission lines. Whereas, a D-STATCOM is connected to the power network at the distribution level. The D-STATCOM supports the grid voltage by means of controlling the reactive power injection into the power system. The generated output voltage will control the flow of active and reactive power between the converter and the grid as follows,

$$P = \frac{V_{PCC}V_c}{X_P}\sin\delta \tag{2. 3}$$

$$Q = \frac{V_{PCC}V_c}{X_P}\cos\delta - \frac{V_{PCC}^2}{X_P} \quad (2.4)$$

where, V_{PCC}, V_c are the rms values of the PCC voltage and converter output voltage respectively, δ is the phase angle of the converter voltage with respect to the PCC voltage and X_P is the coupling reactance.

From the above equation, it can be noted that the active power flow can be controlled by adjusting the phase angle of the converter's generated output voltage. The exchange of active power will mitigate for the converter losses and maintain the dc link voltage. On the other hand, controlling the output voltage V_c will control the operation of the converter in the inductive or the capacitive mode to maintain the PCC voltage. In the voltage control mode, the output voltage of a D-STATCOM is controlled to convey sinusoidal and balanced PCC voltages to the loads [45], [55]-[58]. The D-STATCOM can also operate in current control mode to achieve a harmonic free line current similar to the operation of an APF [59], [60]. Generally, voltage and current sensed information are transformed into the SRF to achieve decouple P-Q control as shown in Figure 2-10 [45], [56] - [58].

A centralized D-STATCOM [61], [62], that is installed at medium voltage (MV) distribution networks, is adequate to provide good voltage support at this network level. However, it will not be able to compensate for local problems happening at the LV side. Since massive number of distributed energy resources (DER) are being installed at the residential or commercial side, PQ improvement techniques should be installed adjacent to these points. This will allow more units to join grid operation without affecting the upstream voltage. The authors in [63] have proposed a D-STATCOM to inject minimum power to maintain the PCC voltage in LV distribution networks. While, the D-STATCOM is usually set to regulate the voltage at 1 pu, the authors have proposed

maintaining the PCC within permissible voltage ranges. Nevertheless, this proposed control strategy is suitable only for non-sensitive loads. In fact, some sensitive loads like digital electronic devices with memories, will suffer from information loss in the event of a very short duration voltage disturbance [8]. PV-STATCOM [64] has also been proposed in the literature, however rating limitation should be considered in the designing process.

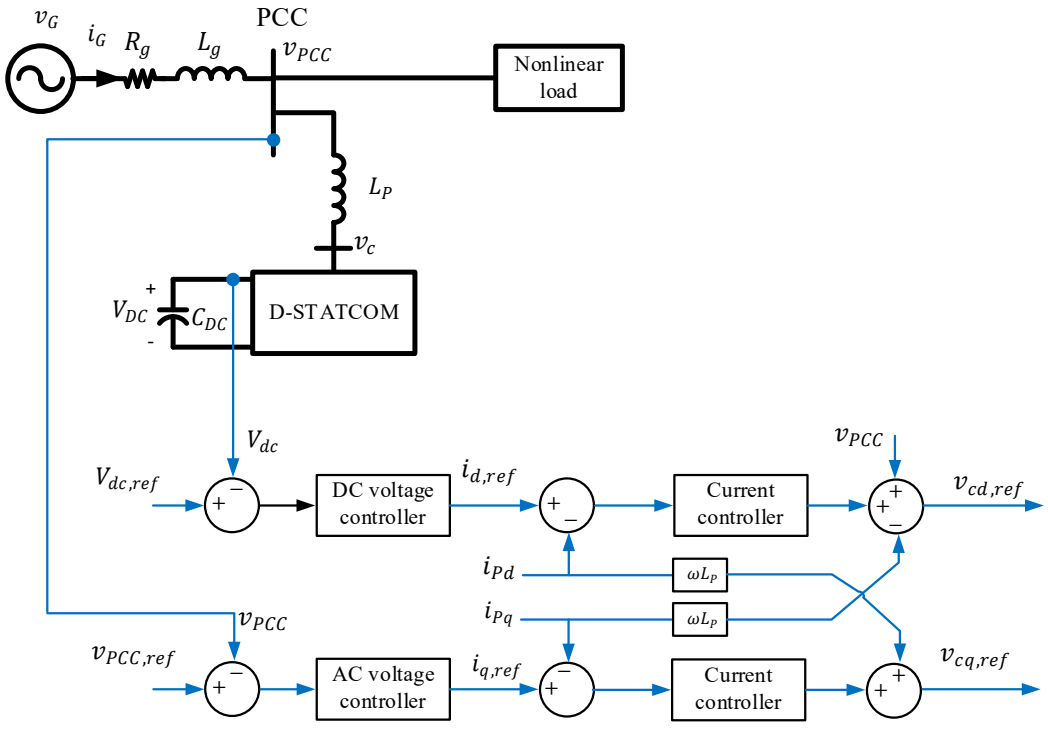


Figure 2-10. Voltage control mode of a D-STATCOM in the d-q frame [57], [58].

A three-phase improved dual UPQC topology (iUPQC) has been proposed in [65] that includes the functionality to achieve voltage regulation at the ac grid side as well. Regardless that the topology limits the power density of the system, it is based on controlling the shunt converter as a voltage source while the series converter is controlled as a current source. The incentive of this control strategy is to avoid generating non-sinusoidal voltage and current references. However, this is not the case if the source current and the output voltage are controlled directly. It also

requires an extra current sensor at the load side to calculate the amount of active power required to supply the load and feed it forward to the dc voltage loop since P-Q control methodology has been adopted.

Electric spring has been proposed in the literature to mitigate for voltage and frequency in microgrids [66]-[68]. Electric spring topology counts on the presence of non-critical loads in the network to form together a smart load. A DER, or in the future a microgrid, are often integrated with the grid at the PCC. Unless the loads connected to the PCC are treated as non-critical loads, it is essential to regulate the PCC voltage.

2.4 Parallel Operation of Modularized Converters

Parallel operation of several power converters is used to realize higher rated power and lower current ripples with lower rated power devices. In a parallel configuration, converters share in the improvement of power quality parameters either equally or proportional to their capacity [69], [70]. Several reactive power sharing techniques among APFs have been proposed in the literature including decentralized control, centralized and droop controls. These control methods can be classified into communication-based [71], [72] and non-communication based control schemes [73]-[76].

In a decentralized control scheme, controllers operate independently based on local information as shown in Figure 2-11 (a). Cascaded operation that is based on capacity limitation control technique has been proposed [73], [74]. The module that is closest to the load will compensate the large portion of harmonics and reactive power until its rated power is met. Each module treats the rest of the connected modules as part of its load. Cascaded operation relies on

load and converter current information from which the remaining reactive power and harmonic contents to be compensated are acquired. This concept does not require communication and offers the ability of extending the system capacity with slow dynamic response. Alternatively, a centralized control scheme [71], [72], referred to as load current distribution or power splitting, is shown in Figure 2-11 (b). The methodology is simple to implement and provides system redundancy. Equal distribution current references are achieved through a central controller tracking the load current, which will require identical units compensating for one load. A proportional reactive power and harmonic current sharing technique according to the ratio of the modules' power ratings have been proposed in [72]. The proposed techniques are designed for modules that are connected to the same feeder and compensating for loads connected at the end of this feeder.

Frequency splitting technique has also been reported for parallel operation of APF [48]. Frequency splitting control methodology lacks redundancy. Besides a converter failure will lead to failure in meeting the controller objectives. A distributed active filter systems that are installed at different locations along a distribution feeder has been proposed in [75], [76]. Each unit has been modeled as a damping resistor to damp the harmonic distortion in the network, from which the droop characteristics between a proportional gain and the unit VA is developed. Droop control is a conventional control method to achieve active and reactive power sharing among DG units in islanded operation of microgrid. Even though droop characteristics offers cooperative sharing between multiple modules without relying on communication systems, unequal line impedances and units' power ratings lead to a mismatch and poor reactive power sharing [77]-[84]. In order to solve this problem, virtual output impedance, adaptive control and hierarchical methods can be performed [79]. Hierarchical control strategies have been proposed to guarantee accurate

performance for mircogrid operation [81]-[84]. Hierarchical control strategy is divided into three levels; primary, secondary and tertiary levels. The primary control relies on local measurement to stabilize voltage and frequency within milliseconds in a decentralized manner. The secondary control operates in a slower response within 1 to 10 seconds to eliminate error deviation caused by the primary control. The tertiary control is the highest level with the slowest response of 15 minutes [83]. It deals with energy management, operation scheduling and economic optimization considering multiple microgrids and the upper grid.

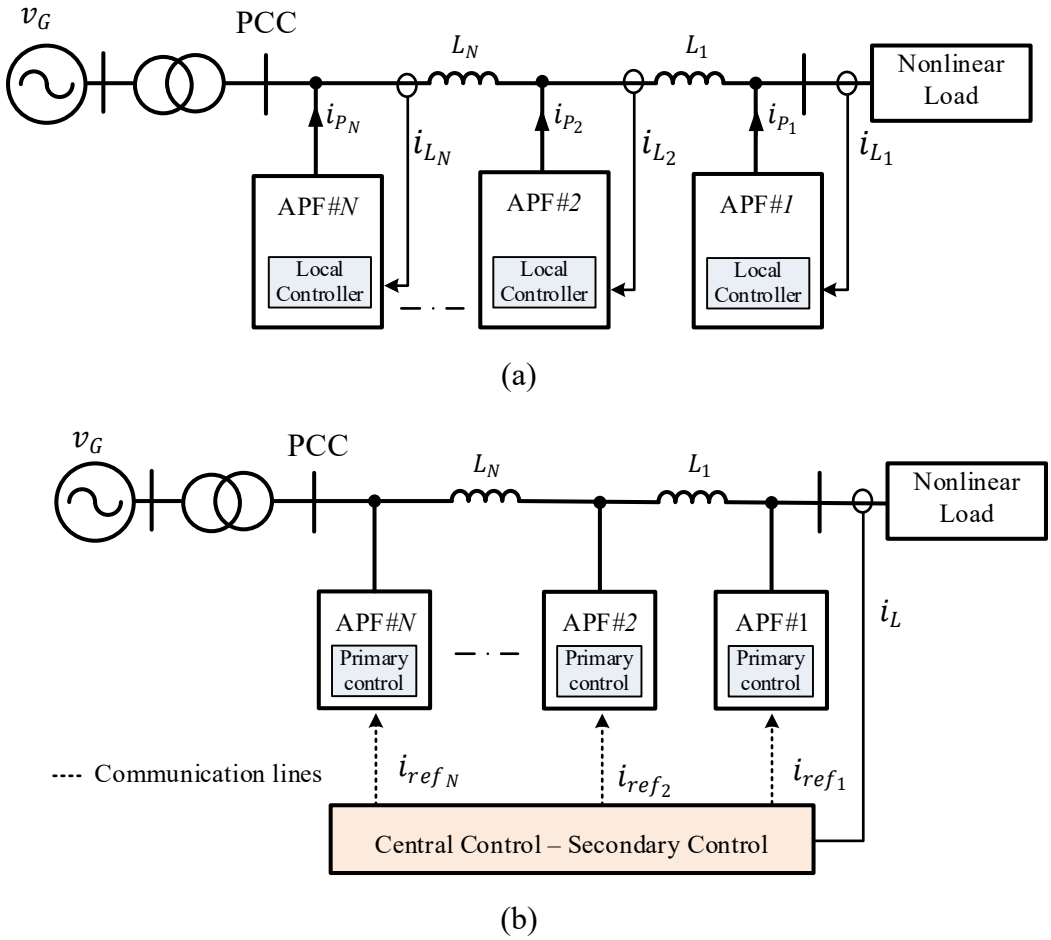
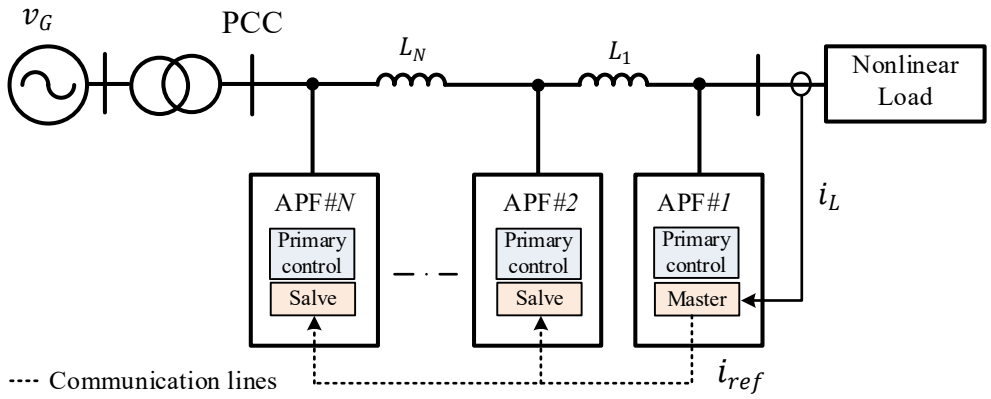
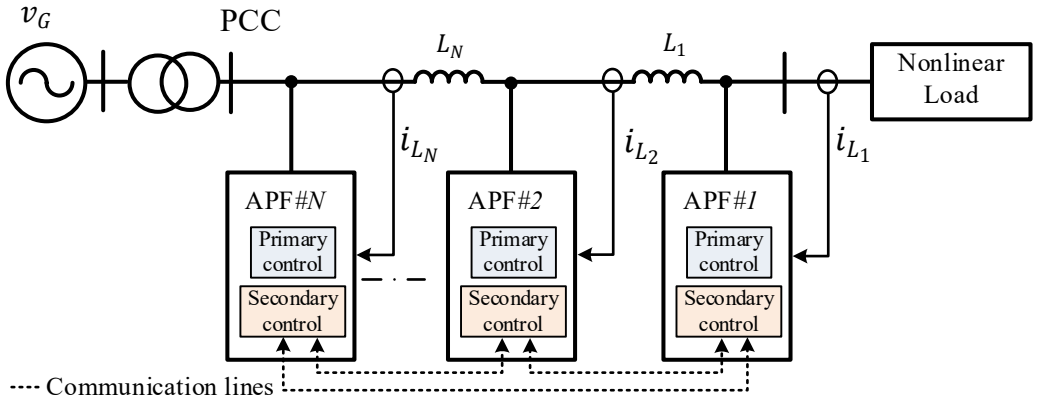


Figure 2-11. (a) Decentralized control scheme (b) centralized control scheme.



(c) Master/slave control scheme

(a)



(d) Distributed control scheme

(b)

Figure 2-12. (a) Master/slave control scheme (b) distributed control scheme.

Communication-based techniques for islanding operation of microgrid includes three categories, central, master/slave and distributed control [85]. In contrary to the central control, the master/slave control does not require synchronization methods in each module. The reason is that the slave modules will receive the specified reference current from the master module. However, high current overshoot during transients and unbalanced current might occur [85], [86]. Under a distributed control, units use collected neighbor information in addition to their local information

to achieve appropriate cooperative performance. Distributed control or multi-agent system technique competes over the centralized mode in terms of reliability and scalability [84], [85]. Figure 2-12 (a) and (b) illustrate multiple APFs communicate under the adoption of a master/slave or a distributed control scheme correspondingly.

2.5 Chapter conclusion

This chapter presented a review of the state of art of UPQC topologies and control methodologies. UPQC topologies are classified according to the adopted converter topology, input supply and circuit configuration. A comparative study between several control methodologies of the series and shunt converter were presented. Various grid voltage regulation techniques were presented and discussed. The shunt converter of the UPQC system can deliver the same function of a D-STATCOM when it is controlled probably to provide grid voltage stability. Even though the injection of reactive power for grid voltage regulation by a three-phase UPQC system has been presented, its application to single-phase UPQC system has not been introduced yet. It can also be concluded from the discussion of the parallel operation of modularized converters that parallel operation of DG units in a microgrid has been extensively studied. Nevertheless, the parallel operation of modularized converters for power quality improvement is not well developed.

Chapter 3 Characterization of Commercial LED Lamps for Power Quality Studies

3.1 Introduction

Technological advancements in LED lighting industry currently offer high luminous efficacy with low cost and high color rendering index (CRI) LED lamps. Table 3-I gives a comparison between the efficacies of different types of lighting sources given their general efficacy range measured in Lumen/Watt [16]. It also indicates the range of each lamp CRI and lifetime. Manufactures are currently competing to break through the predicted theoretical luminous efficacy limit 260-300 lm/W of white LEDs [16], [17]. Moreover, LED lamps are high reliable products with long-lasting lifetime that ranges from 50000 up to 100000 hours. LEDs are also ecologically friendly with no toxic substances or ultra-violet emitted energy [16].

Energy saving programs are taking place in Canada to encourage the market and the consumer choices towards more efficient products that include replacing conventional lighting sources with LED lamps [16]. This replacement has raised a concern over PQ problems associated with utilizing LEDs and their undesirable effects on the power grid. Even though LEDs show the most efficient lighting source, they do not offer the best choice when high PQ parameters are essential. Studies have been carried out to evaluate the performance of LEDs compared to compact fluorescent lamps (CFL), high pressure sodium (HPS) and incandescent bulbs [87]-[89]. LEDs show a better performance in terms of THD and PF in contrast to CFL driven by an electronic ballast. However,

The work presented in this chapter has been published in the following paper: R. Abdalaal and C. Ho, "Characterization of commercial LED lamps for power quality studies," *IEEE Can. J. Elect. Computer Eng*., 2020, early access.

a CFL driven by an electromagnetic ballast would achieve higher PQ parameters [89].

The wide utilization of LEDs dictates the need to perform more studies to examine the characteristics and behavior of commercial LED lamps. For the purpose of this research study, the effects of voltage flickering, voltage harmonics, current harmonics and the interaction between them are studied as steady-state PQ problems. Voltage sags and voltage swells which happen for a short period of time are studied as disturbance PQ problems.

TABLE 3-I COMPARISON BETWEEN THE EFFICACY OF VARIOUS TYPES OF LIGHTING SOURCES [16]

Type of lamp	Lumen/Watt	CRI	Lifetime
Incandescent	10 to 35	95+	1000-4000
Mercury Vapor	30 to 80	20-45	24000+
LED	40 to150	50-95+	50000-100000
Fluorescent	40 to100	60-90	6000-30000
Metal Halide	50 to 115	65-90	6000-20000
High Pressure Sodium	85 to 150	20-30	24000-80000
Low Pressure Sodium	100 to 200	N/A – Low	18000
Induction	50 to 100	80-85	60000-100000
Plasma	70 to 150	70-85	3000-50000

3.2 LED Lamps Technology

Figure 3-1 gives a sectional view diagram of the structure of a commercial LED lamp. The main components that are of interest and have been investigated in this study are the LED string and the LED driver.

3.2.1 LED Semiconductor material

An LED lamp consists of a solid-state device that emits light when electric current passes through it. LEDs are fabricated by either inorganic semiconductor materials such as; indium gallium nitride (InGaN), aluminum gallium arsenide (AlGa) and gallium phosphide (GaP), or by organic (OLED) carbon-based semiconductors [90]. Inorganic LEDs produce concentrated output light. They are mainly applied in residential, commercial and outdoor lighting applications. OLEDs allow for thinner, lightweight and larger surface area displays that can be used in TV, cellphones and tablets [91]. Due to their diffuse output light, they are suitable for indoor and decorative lighting applications. Both technologies continue to advance and develop in different applications.

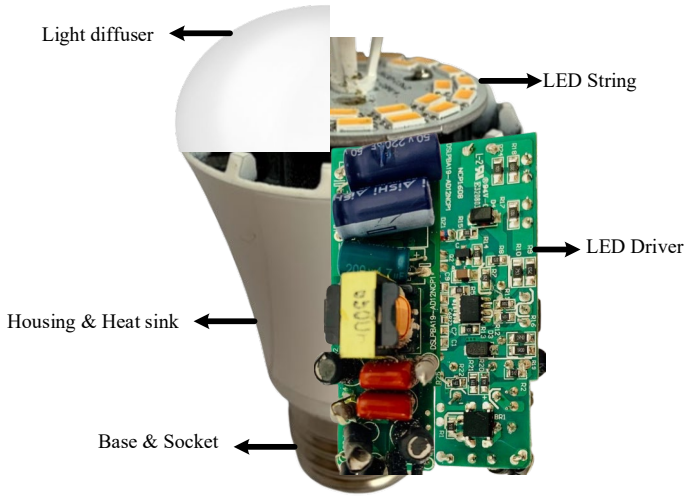


Figure 3-1. Sectional view diagram of an LED lamp.

3.2.2 LED Drivers

In order to characterize the behavior of an LED light bulb, it is important to study the operation

of its internal driver circuit first. An LED lamp is a dc voltage load. Therefore, LED requires conditioning the input power and a current regulating driving circuit that delivers constant current to the LED. The LED driver is the main source of PQ problems. Various techniques have been developed to improve the reliability as well as the driving circuit of LEDs. LED drivers can be categorized into passive, active and dc driver.

A. Passive Driver

Passive LED drivers comprise only of passive components (e.g. resistors, inductors, capacitors and diodes). They are preferred in outdoor applications due to their high reliability and high efficiency. However, it becomes challenging to achieve low THD and high PF on top of low output voltage ripple. The valley-fill circuit has been proposed and modified, as shown in Figure 3-2, to eliminate the large electrolytic capacitors (E-caps) that limit the life span of LEDs [92], [93]. Passive drivers require large inductors that make the driver bulky and heavy.

B. Active Driver

Active drivers contain active semiconductor devices operating at high frequency that can achieve precise output control. The Literature classifies active LED drivers according to the number of power stages included [90], [94].

A single-stage topology has one controller where the ac input voltage is rectified and applied directly to the LED string. A typical single-stage topology is a rectifier bridge then a dc/dc converter that can be either buck, boost or buck-boost. A buck topology is shown in Figure 3-3. The rectifying circuit draws current when the instantaneous input voltage exceeds the capacitor

voltage as illustrated in the waveforms in Figure 3-3. This will result in a high-distorted input current with low PF. The authors in [95] proposed a buck topology with current path control switches for LED segments for improved PF. Another popular single-stage topology is the flyback converter shown in Figure 3-4 [96]. Flyback converter topology offers isolation and can function as a power factor correction (PFC) circuit. Generally, single-stage topology offers high power density with less number of switching devices. Nevertheless, it suffers from meeting the requirements of both high efficiency and long lifespan for LEDs due to the need of large E-caps at the output to reduce the output ripples.

It is challenging to achieve high PF, low output ripple and current control with one converter. For that reason, researchers introduced adding another converter. A two-stage topology, as depicted in Figure 3-5, is typically used to offer a better performance and a reduction of output ripple. The first stage includes a PFC to shape the input current. The boost topology is mostly used for this stage due to its easy implementation. The second stage includes a dc/dc converter to maintain the voltage and the driving power of the LED string. The two stages will work independently. Having independent control loops and gate drivers will add to the cost of the system. Besides the energy is processed twice which will decrease the overall efficiency. For higher LED lighting applications (>100W), LLC converter has been introduced [97]. Figure 3-6 shows a traditional topology for high wattage LED applications. As the PFC dc output voltage is high, an isolation is required. The dc/dc stage consists of a half bridge LLC resonant converter that drives the LED strings. Due to the increased number of switching devices, attention should be given to the switching loss.

Integrated single-stage solutions have been introduced in the literature [98], [99] in which the PFC stage and the dc/dc stage are combined in one converter. This is attained by sharing the power

transistor to achieve low input current harmonics and low output ripple. Integrated single-stage topology requires less number of switches, control and gate driving circuits. However, high voltage stress will be imposed across the switch. Therefore, it is mostly used in low power application.

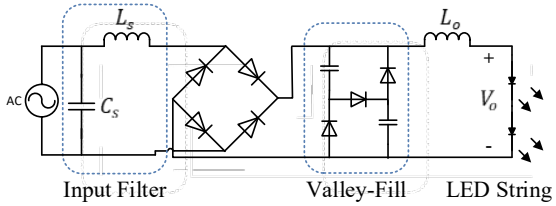


Figure 3-2. Passive LED driver based on valley-fill circuit [92].

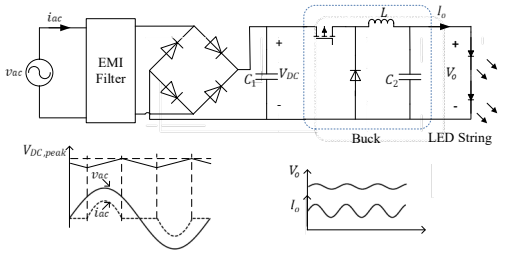


Figure 3-3. Single-stage LED driver based on buck converter

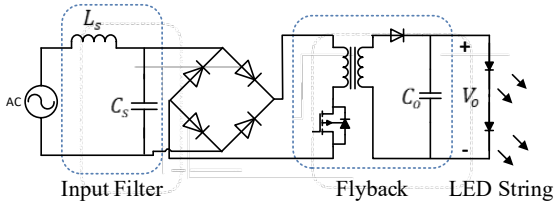


Figure 3-4. Single-stage LED driver based on flyback converter.

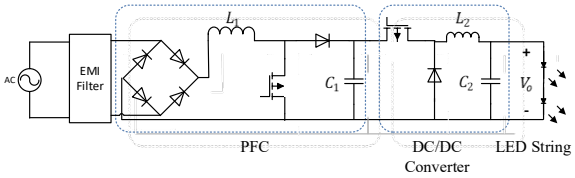


Figure 3-5. Two-stage LED driver.

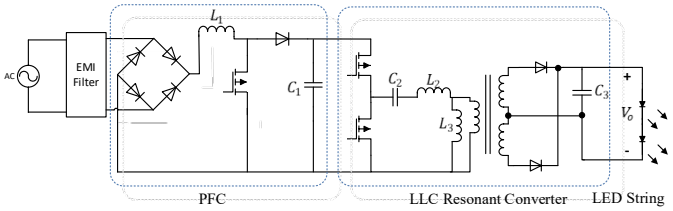


Figure 3-6. Conventional two-stage LED driver for high power applications.

C. Dc Driver

Dc microgrid is now being introduced with the adoption of recent technology of renewable

energy sources. In a dc grid, there will be no need for the ac-dc conversion stage increasing the overall efficiency. Recent studies are proposing topologies for LED drivers that are compatible with dc grid. A buck-boost LED dc driver that allows battery operation has been presented in [100], while the authors in [101] have proposed a half bridge inverter with a variable inductor for current regulation. A dc grid does not guarantee a flicker-free environment. Power quality issues related to ac voltage networks are applied to dc voltage networks. In dc voltage networks, voltage variations can result from the fast changes in solar irradiance in PV generation. AC/DC conversion will introduce voltage ripples in the network. In addition, faults and sudden heavy load changes will cause voltage dips and swells. The immunity of LED lamps to flickering in low voltage dc networks is still being investigated [102].

It is important to note that flickering levels and amount of harmonics injected by LEDs are not constant and vary with the type of the utilized driving methodology.

3.2.3 LED International Regulations

Efficiency, power density, cost and lifetime are the four main criteria to design an LED lamp. However, manufactures must take into consideration international standards and regulations in their selection of an LED driver. The most adopted SSL standards are the IEC standard for limits of harmonic current emissions [10] and the Energy Star program [103]. In IEC 61000 3-2 standard, lighting equipment is under class C for power ratings > 25W or class D for ≤ 25W, in which harmonic contents of the input current, up to order 40, shall not exceed maximum permissible limits.

TABLE 3-II POWER SUPPLY REQUIREMENTS IN ENERGY STAR PROGRAM [98]

Power Factor	Commercial ≥ 0.9, Residential ≥ 0.7
Minimum Operating Temperature	-20°C or below for outdoor applications
Operating Frequency	≥ 120 Hz
Electromagnetic and Radio Frequency Interference	Commercial: Class A in FCC part 18 Residential: Class B in FCC part 18
Transient Protection	IEEE C.62.41-1991, Class A operation.

ANSI, IESNA, UL and NEMA are the lighting standards referenced in the Energy Star program that defines performance characteristics and procedures to test SSL products. These criteria are applied for residential and commercial lighting products that are connected to the electric grid. Table 3-II gives general requirements for power supply adopted in LED.

3.3 LED Lamps Power Quality Problems

A. Harmonics

As discussed in the previous section, a driving circuit is necessary to condition the voltage applied to LEDs. Therefore, their actual characteristics as loads will change according to the power electronic devices employed in the driver. Power electronics introduce high harmonic contents in the power network. Some low cost LED bulbs contain high harmonic contents that exceed the requirements specified by the standards IEC 61000-3-2 and IEEE 519 [10], [11]. Different manufactures employ dissimilar filtering techniques; therefore, LEDs harmonic current emissions are not identical. A frequency-domain LED model to simulate a large-scale of LED lighting network has been presented in [18]. The study shows that despite the low power consumption of LEDs, many LEDs connected to the same bus would pollute the network voltage, increasing the

harmonic voltage distortion level. In addition, dimmable LEDs will add additional reduction to the PF with more harmonic contents reaching 360% using TRIAC-based dimmer [104], [105].

To mitigate the injected harmonics, researchers are proposing including a passive filter or a PFC circuit to the LED internal driver. A PFC circuit adds complexity and increases the cost of an individual LED bulb. The authors in [106] recommended connecting a combination of CFL, LED and incandescent bulbs as an optimized solution to avoid their disadvantages if they were employed individually. This solution is not practical to the user and does not follow the advancements of SSL and power semiconductor devices.

B. Flickering

LEDs are also subjected to flickering. Flickering has been defined in Chapter 1 subsection 1.2.1.D. Rapid heavy load changes are typically the cause of system flickering. For example, large spot-welding machines often operate in or near 5-10 Hz. A human eye/brain is most sensitive to low frequencies. There will be random voltage variations over a wide frequency band when ac electric arc furnaces are in operation that yield to a major source of flickering [19]. Flickering has brought concerns to both utility and end-users, due to human biological effects of light flicker. Potential health risks caused by flickering in LEDs has been addressed in IEEE standards PAR1789 [13]. The risk of epileptic seizure is high when flicker occurs at frequencies within the range of 3–70 Hz. Other less severe neurological symptoms including malaise and migraine might happen due to a visible or invisible flickering. Frequencies of 100 Hz for 50 Hz electric network in Europe or 120 Hz for 60Hz electric network in North America cause distraction and headaches, usually when there is a large variation in the light intensity [13].

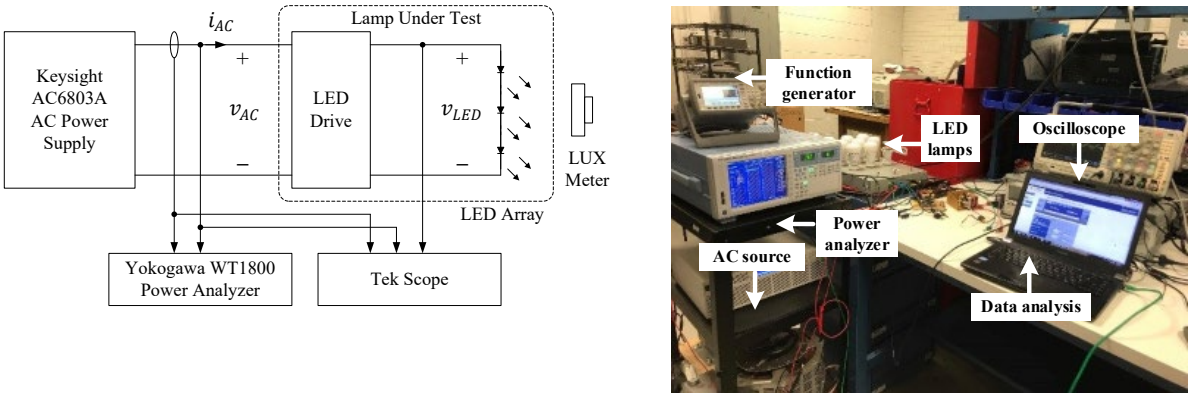
Providing constant current to LEDs will reduce the flickering phenomenon due to the correlate

relation between the LED forward current and its output light intensity. This approach is not applicable with dimmable LEDs, as they are sensitive to voltage variations in the network. A smart bulb has been introduced as a flicker-free LED in [107]. The dimming signal will be received by an external transceiver to vary the pulse width modulation (PWM) signal duty cycle. However, this technique requires additional wireless communication modules in each individual bulb to support this technology, which adds complexity to the LED driver, and increases the cost of a large lighting network.

3.4 Experimental Setup of LED Characterization

In order to characterize the LED light bulbs working under different PQ conditions, an experimental setup has been implemented, which is used to execute light intensity, harmonic current contents and LED array driving voltage measurements.

A block diagram of the test setup, laboratory setup and the LEDs under test are shown in Figure 3-7 and Figure 3-8 respectively. An ac power supply (Keysight AC6801A) is used to provide different ac voltage levels to the LED light bulbs. Besides, the ac power supply output can be controlled by an external reference signal from a function generator, thus it can simulate different voltage quality issues, such as voltage dip, swell and flickering. A 50MHz current probe, a 50MHz differential probe and an oscilloscope (Tek MDS3204) have been used to measure the current and voltage waveforms. A Power Analyzer (Yokogawa WT1800) is used to measure the current harmonics and PF.



(a) (b)

Figure 3-7. Experimental setup (a) block diagram (b) laboratory setup.

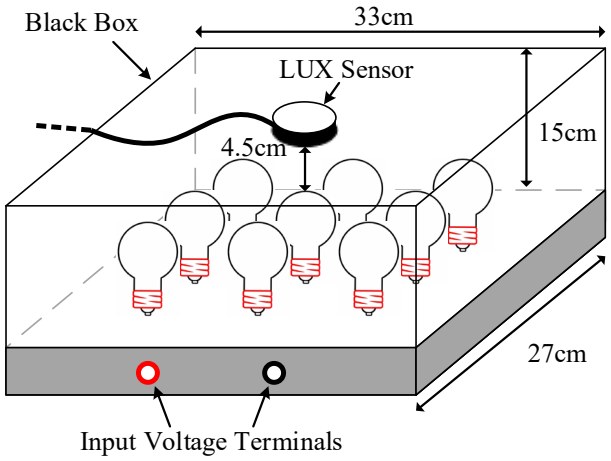


Figure 3-8. Black box dimension.

A LUX meter (Anaheim Scientific H100) is used to measure the light intensity of the LED light bulbs when the ac power supply changes across the LEDs. A black box covers the lamp fixture. The detailed of the black box dimension is given in Figure 3-8. The LUX meter is placed on top of the box with 4.5 cm distance from the top of the light bulbs. It is important to mention that the purpose of using the black box is to have a fixed environment for the LEDs setup to analyze

the change of the relative light intensity of the LEDs under various PQ conditions. The maximum output light intensity is measured under nominal voltage. Then, relative luminance values are measured under different PQ problems.

The internal driver of three dimmable LED lamps were studied: Cree, TCP and Sunbeam LED lamps. The printed circuit board (PCB) and a summary of the lamps' specification are given in Appendix A.1. The internal drivers of the lamps under studied were found to be single-phase topologies and their operation almost encountered similar behavior. Therefore, Sunbeam LED lamp has been selected to be extensively studied in this research.

The experimental measurements employed have been conducted on 9 Sunbeam LED bulbs with 12 W power consumption each that is equivalent to a 60 W incandescent lamp. The LED lamp is Energy Star certified. The internal driver of the LED bulb is a single-stage topology that consists of a bridge rectifier and a buck converter as shown in Figure 3-9. The complete schematic is given in Appendix A.1. A controller NCP1609 has been adopted to regulate the output voltage across the LED string. The controller is based on voltage mode control that operates in critical conduction mode and suitable for applications up to 350W [108]. The controller regulates the output voltage using an internal error amplifier (EA). The inverting input of the EA is the feedback pin (FB) which is sensed using a resistor divider that scales down the buck output voltage. The non-inverting input of the EA is connected to a reference voltage. The output of the EA is the control pin (Control) that controls the on time (t_{on}) of the switch. The on time is constant for a given rms input voltage and output load as follows,

$$t_{on} = \frac{2P_{out}L}{\eta V_{ac}^2} \tag{3. 1}$$

where P_{out} is the load output power, η is the efficiency and $V_{ac}$is the rms input voltage [108].

The off time varies with the instantaneous input voltage by observing the voltage of an

auxiliary winding that is sensed by zero current detection (ZCD) pin to detect the inductor demagnetization for critical conduction mode operation. The controller is also working in a closed loop system, with a varying LED string reference voltage. In NCP1609 controller, an internal voltage ($V_{control}$) varies with the variation of the rms input voltage, which is compared to the (Ct) pin voltage. The circuit controls the power switch on time hence controlling the power delivered to the LED string. The Ct pin sources a current to charge the external capacitor and discharges the capacitor at the end of the on time period [108].

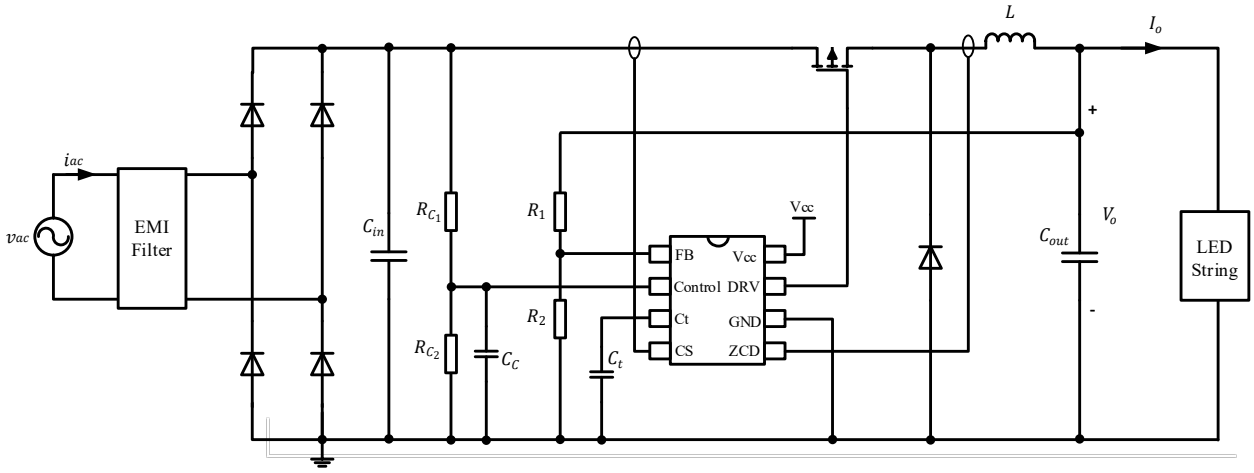


Figure 3-9. Sunbeam internal driver schematic.

3.5 Experimental Results and Analysis

Since LED lamps mainly employ power electronic devices to convert ac voltage to dc voltage and maintain the LED array driving voltage. These devices bring nonlinear characteristics to the LED lamps. Various tests have been conducted to analyze and characterize the behavior of the LEDs under dynamic and static changes.

3.5.1 Harmonic Analysis

The first test is to evaluate the current quality of the LED light bulbs. A pure sinusoidal input voltage has been applied directly across LEDs under test. Table 3-III lists the testing conditions under nominal operating point. The internal driver of the LED bulb under this test consists of a PFC topology using buck converter. The maintained output voltage is set to a value lower than the peak ac voltage. Input current will flow when the instantaneous ac voltage is higher than the output voltage. Otherwise, the bridge rectifier is reverse biased. Therefore, there is a zero-current zone at the grid voltage zero crossings. Figure 3-10 (a) shows the input current drawn by the LEDs with a nominal input voltage of 120V rms. Lower bus voltage level is required in a PFC buck topology compared to a PFC boost topology. Nevertheless, achieving high PF and low THD is limited [109].

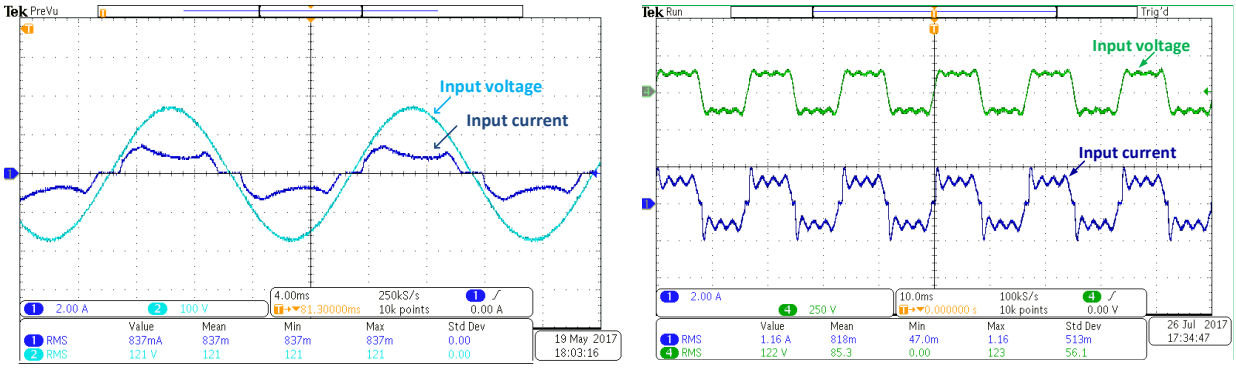
TABLE 3-III BASIC PARAMETERS MEASURED FOR LED LAMPS UNDER TEST

Parameter	Value	Parameter	Value
$V_{AC,rms}$	119.93 V	$I_{AC,rms}$	0.876 A
f_{Line}	60 Hz	PF	0.94414
P	98.9 W	S	105.1 VA
THD_V	0.051%	THD_i	31.104%

The input PF, the total harmonic distortion of the voltage (THD_v) and the current (THD_i) have been measured using the power analyzer and given in Table 3-III under nominal operating condition. The results show that the PF of the LEDs under test is acceptable, however THD_i is high since it cannot provide a sinusoidal current at the input. High harmonics injected to the network will lead to overheating in cables and equipment, high core and copper losses in motors and transformers, and EMI with communication systems. Moreover, the interference of two or more nonlinear loads will result in a distorted bus voltage, which in return influences all the loads

connected to the same bus. Hence, more harmonic contents will be injected back to the network.

The second test is to observe the interaction between voltage and current harmonics. In this test, a distorted input voltage has been applied across the LEDs. The applied voltage contains up to 7th order harmonic components. Figure 3-10 (b) shows the waveforms of the applied distorted voltage and the corresponding drawn current by the LEDs. Power analysis measurements have been recorded. The results give an increase of the THD_i from 31.104% to 36.736%, and an increase of input current from 0.876A to 1.130A. Thus, an increase of input power delivered to the load by 3%. This indicates that not only the harmonics level will be higher for a distorted bus voltage, yet a sudden increase in the total power demand will occur especially, if a large number of LEDs are connected.



(a) (b)

Figure 3-10. Input voltage and input current drawn by LEDs (a) sinusoidal input voltage (b) distorted input voltage.

The chart given in Figure 3-11 shows the harmonic current spectrum expressed in mA. The graph highlights two scenarios: harmonic current spectrum with pure sinusoidal input voltage and with distorted input voltage. Higher harmonic components are experienced with the distorted input voltage. The test results are compared with maximum allowable current in IEC 61000-3-2 standard. Harmonic contents exceed for 7th, 9th and 11th harmonic order. Even though an individual

LED bulb adds a minor effect to a large network, the harmonic distortion level will be high when several LEDs are connected to the same feeder e.g. street lighting or parking lot lighting.

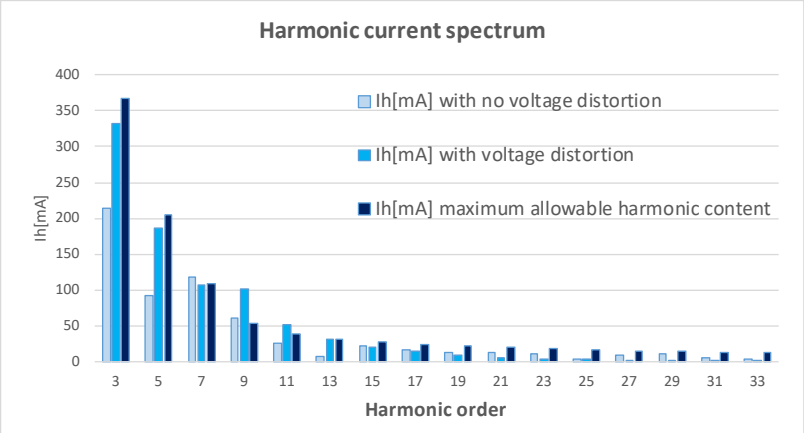


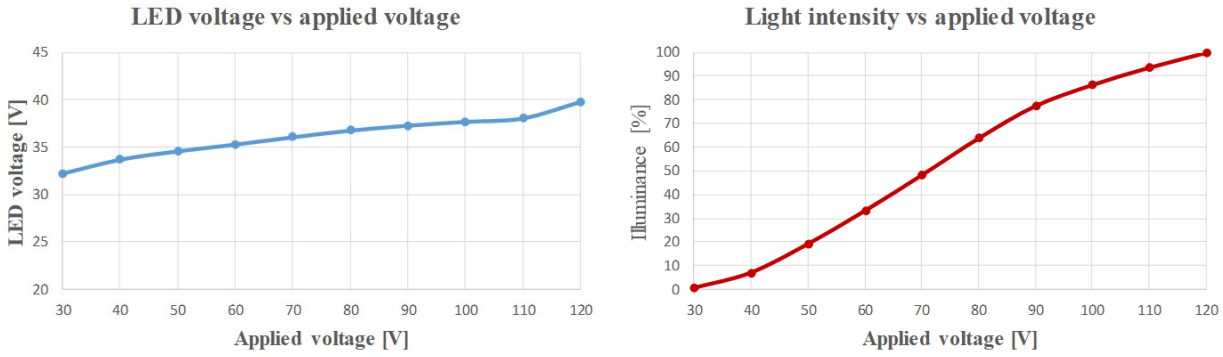
Figure 3-11. Harmonic spectrum of the current drawn by the LEDs.

3.5.2 Static Relationship between Light Intensity, LED Array Voltage and Input Voltage

One of the advantages of utilizing an LED bulb as a light source is its compatibility with TRIAC dimmer. The amount of light intensity provided by an LED is proportional to the average current passing through it [110]. The LED driver provides dimming capability by sensing the change in the input voltage level and accordingly the controller adjusts the average current fed to the LED string [111]. Subsequently, the output light intensity can be controlled.

A test has been conducted to study the change in the output light intensity by varying the ac-applied voltage across the LED lamps. The ac voltage across the LEDs has been gradually decreased from 120V rms to zero. Below 30V rms, the voltage cannot sustain the LED array and the lamps turn off completely. At 120V the total luminous flux incident on a surface per unit area (illuminance) is found to be 12800 LUX. This value has been taken as the maximum output light

intensity of the LEDs under the test condition. As the black box has been used to cover the LEDs in this test, all other measurements are given relative to the maximum output illuminance expressed in percentages. The results in Figure 3-12 show that if the applied voltage is reduced, the voltage across the LEDs will be changed and hence the output light intensity will be decreased accordingly, until it reaches 30V. This means that the LED driver will translate the reduction of the applied voltage into a request of dimming. The reason of the light intensity dropping is that the change in the input voltage is sensed by the controller as depicted in Figure 3-9. Therefore, the controller will interpret this change as a dimming request and will react accordingly to reach a new operating point based on (3.1). Hence a reduced voltage will be applied across the LED string. Since there's a direct relation between the LED forward current and its output light intensity, the lamp's output illuminance will decrease as well. This directly affects the power consumption of the LEDs.



(a) (b)

Figure 3-12. Input voltage vs (a) LED voltage and (b) light intensity.

3.5.3 Dimming with amplitude variation technique

From the discussion in the previous subsection, dimming an LED can be achieved by varying

the amplitude of the voltage applied, therefore controlling the LED forward current, hence its light intensity. Figure 3-13 illustrates the waveforms of the drawn input currents for a reduced applied rms voltage levels across the LEDs under test. As explained earlier, for a buck topology the diode bridge rectifier is reverse biased when the instantaneous input voltage is less than the dc bus voltage level. The input current starts to flow if the instantaneous input voltage is greater than the dc bus voltage. Hence, the diode bridge rectifier becomes forward biased. This period is referred to as conduction angle (σ). The current sensor (CS) pin, in Figure 3-9, limits the current through the power switch to a maximum-programmed sensed current. A high dc bus voltage leads to a short conduction angle increasing the current total harmonic distortion.

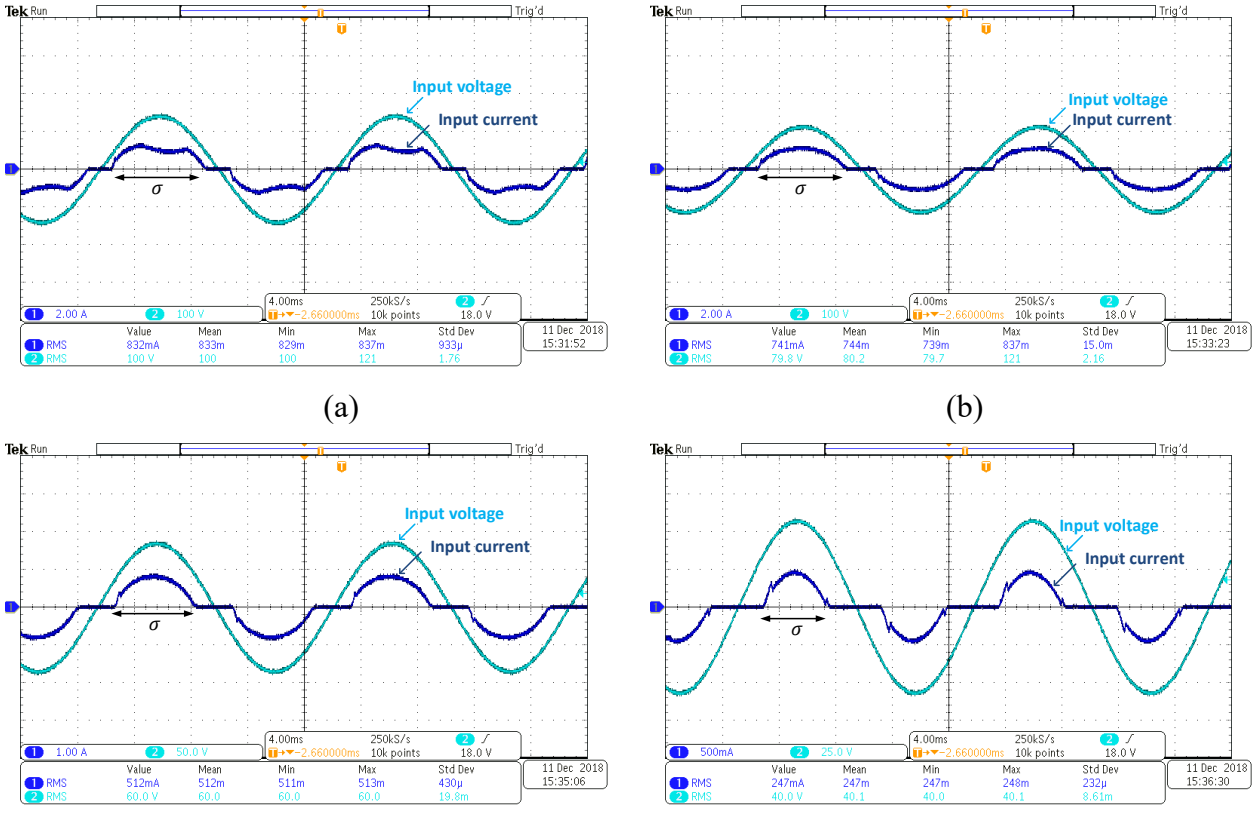


Figure 3-13. LED waveforms under various rms voltage levels (a) 100V (b) 80V (c) 60V (d) 40V.

TABLE 3-IV POWER QUALITY PARAMETERS WITH VARYING VOLTAGE AMPLITUDE

Applied rms voltage	Fundamental current [mA]	3rd harmonic [mA]	5th harmonic [mA]	7th harmonic [mA]	THD_i [%]
110	843.1	145	125.5	98.5	25.64
100	846.7	65	138.9	72.2	20.31
90	829.2	54.9	118.5	52.4	17.35
80	749.8	101.9	93.6	41.6	19.37
70	630.8	117.8	82.4	24	22.98
60	504.7	128.6	63	5	27.86
50	369.7	129.4	33.7	15.2	34.71
40	226.4	108.4	2.4	18.3	44.19
30	106.8	74.1	29.4	3.1	60.59
< 30	LEDs turn off				

Table 3-IV depicts the PQ parameters with the varying ac applied voltage. It can be noted that the total harmonic distortion of the input current varies under different operating conditions. This is due to different conduction angles under each voltage level. In addition, at low input voltage levels the fundamental current is small compared to the harmonic contents. The results depict that the distortion level is still within the permissible limits given that dimming has been achieved by reducing the sinusoidal voltage amplitude. Harmonic contents depend mainly on the PFC circuit implemented in the LED driver. However it can be observed that reducing the sinusoidal voltage amplitude to achieve dimming would limit the input current distortion to the level designed by the manufacture.

3.5.4 Flickering and Sensitivity to Voltage Fluctuations

Since light intensity flickering is directly correlated with voltage fluctuations, the severity of flickering mainly interrelated with the amplitude and the frequency range of these voltage variations. In this chapter, the percent flicker will be calculated as a measure of flickering as follows [112],

$$Percent\ flicker = \frac{\max LUX - \min LUX}{\max LUX + \min LUX} \quad (3.\ 2)$$

Amplitude modulation (AM) technique is used to emulate flickering. A programmable ac-source with a modulated amplitude signal is applied across the LEDs. The amplitude-modulated signal is expressed by,

$$s(t) = [A_c + A_m \sin(2\pi f_m t)] \sin(2\pi f_c t) \quad (3.\ 3)$$

where,

$$\text{Carrier signal: } c(t) = A_c \sin(2\pi f_c t) \quad (3.\ 4)$$

$$\text{Modulation signal: } m(t) = A_m \sin(2\pi f_m t) \quad (3.\ 5)$$

and,

$$\text{Modulation index: } m = \frac{A_m}{A_c} \quad (3.\ 6)$$

The modulation index (m) is a measure of how much a modulated signal is varied with respect to its unmodulated level. The effect of changing the modulation frequency and the modulation index on the output light intensity has been investigated. Figure 3-14 shows an amplitude-modulated signal with 60 Hz carrier frequency, 4 Hz modulation frequency waveforms and 8%

modulation index. It can be seen that the LED voltage is fluctuating with the same frequency as the input voltage.

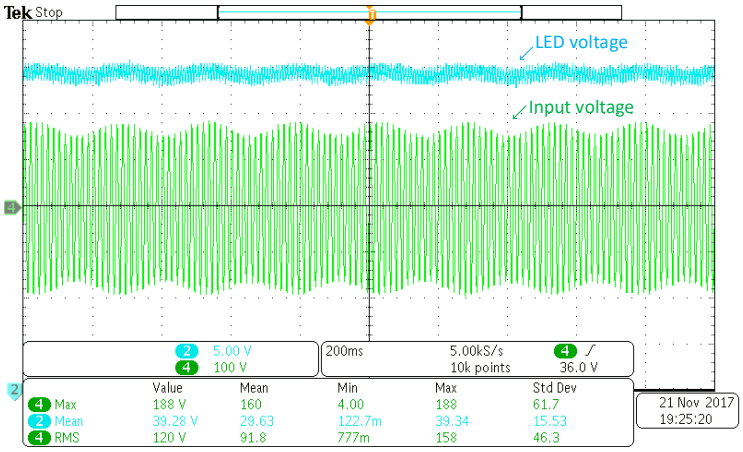
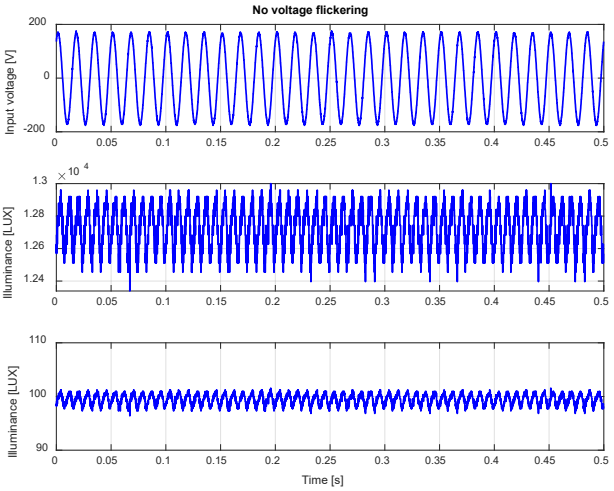
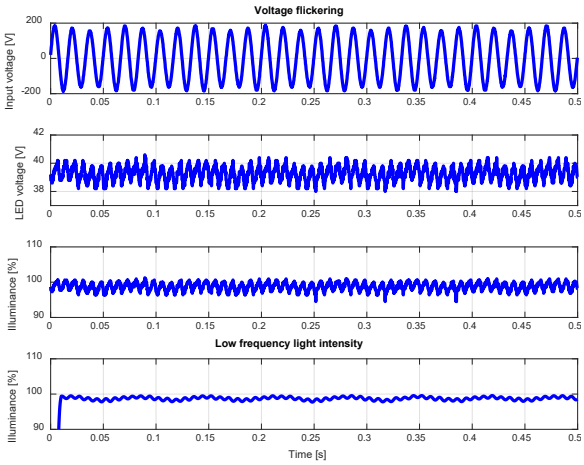


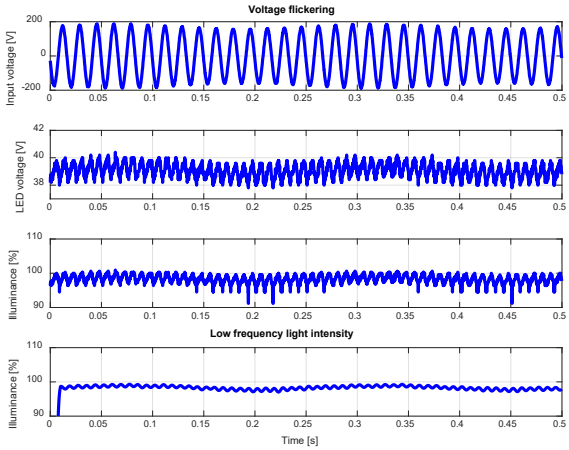
Figure 3-14. Applied voltage flickering to LED lamps.

A string of LED has I-V characteristics similar to a diode. An LED is a p-n junction with a dynamic resistance that shifts as the forward current changes. A slight change of an LED voltage will result in a large change in LED current. The LED string can be modeled as a threshold voltage in series with a dynamic resistance [98]. Therefore, an assumption has been made in the measurements that the dynamic response of the LED array is very quick for changing the array voltage to the light intensity and cannot be recorded using the LUX meter. Hence, curve fitting has been done using Figure 3-12 measured results to map the light intensity to the scope measured LED array voltage. Figure 3-15 (a) shows a steady-state input voltage of 120 V rms without voltage flickering, which results in high frequency changes (including double line frequency and switching frequency) in the light intensity that are not observable by human eyes. Yet, there is no low frequency variation in the light intensity. In contrast, a further experiment by inputting a modulated ac signal to represent voltage flickering that has frequencies of 60±15 Hz, shown in Figure 3-15 (b).



(a)





(b) (c)

Figure 3-15. LED voltage and light intensity with (a) no flickering input voltage (b) 15 Hz voltage flickering (c) 4 Hz voltage flickering.

In order to have a better observation of low frequency components, high frequency signals, which are not observed by human eyes, are removed by means of data processing with MATLAB software tool using the recorded light intensity measurements. A waveform with a low frequency

variation of light intensity can be seen at the bottom row of Figure 3-15 (b). The low frequency variation in the LED voltage caused a visible rapid change in the illuminance of the LEDs. It is the reason to have observable flickers from LED light bulbs. Figure 3-15 (c) shows that for slower flickering frequencies less than 5 Hz, the variation of light intensity is very slow to be observed by a human eye. However, these invisible variations might cause a health risk as addressed by the PAR1789 standards, as the sensitivity of a human eye to flickering differs from one person to another.

The effect of varying the modulation index (m) on the percent flicker is shown in Table 3-V. The percent flicker is calculated for input voltage flickering with a 2% step change in m. The results verify that, lower m, meaning lower voltage peaks variations, will result in lower flickering.

TABLE 3-V PERCENT FLICKER FOR 2% STEP CHANGE IN MODULATION INDEX

m	2%	4%	6%	8%	10%
Percent flicker	38.01%	41.26%	41.26%	43.17%	43.17%

The observed light intensity by a human eye is dissimilar from the light intensity measured by a lux meter. The relation between the measured and the perceived light intensity is nonlinear and governed by the following [112],

$$P_i\ (\%) = \ 100 * \sqrt{M_i\ (\%)/100} \tag{3. 7}$$

where: P_i is the perceived light intensity, and M_i is the measured light intensity.

For instant, a bulb that is dimmed to 5% of its full intensity will be perceived by 22.4%, while 80% dimming level will be perceived as 89.4%. Figure 3-16 shows the measured and the perceived light for LEDs under test with different applied voltage levels. It can be noted that at low dimming

levels the perceived light intensity will be higher than the desired one. The reason is at low light levels, the human eye enlarges the pupil to permit a greater amount of light to enter the eye [112]. In order to examine if this difference would improve the percent flicker for the end-user, various light intensities have been considered.

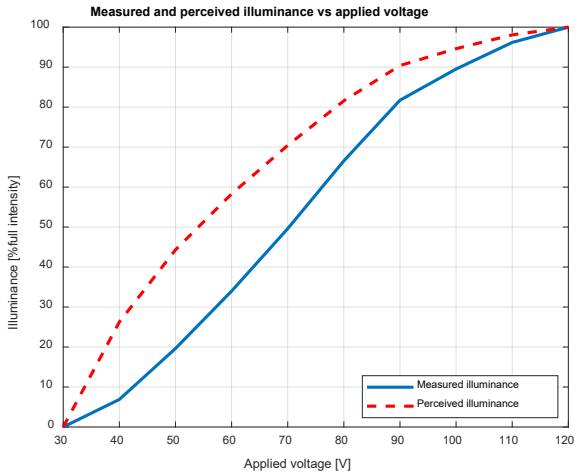
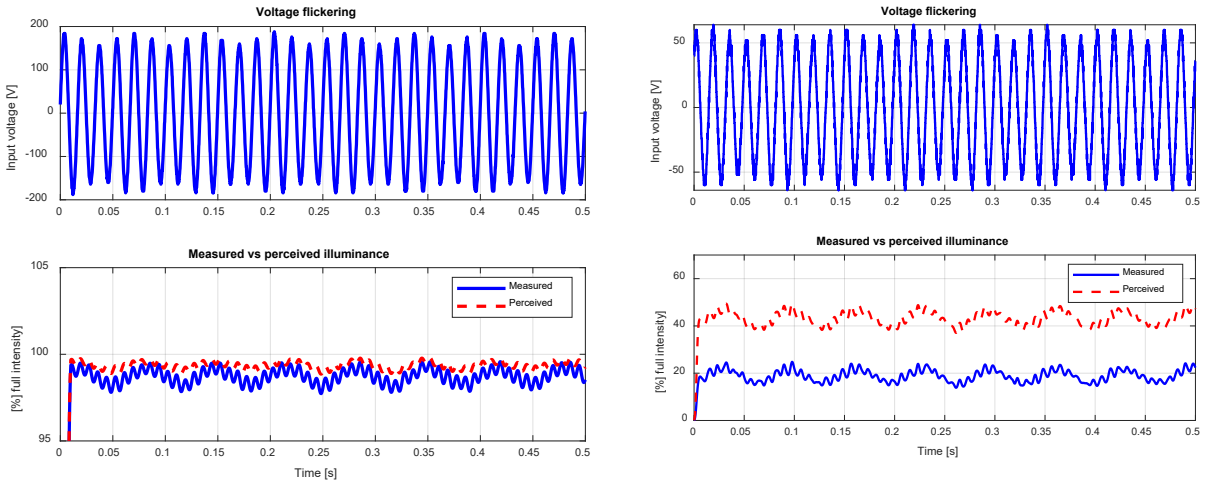


Figure 3-16. Measured and perceived light intensity under different voltage levels.



(a) (b)

Figure 3-17. Measured and perceived illuminance with voltage flickering (a) 100% light intensity (b) 16% light intensity.

Dimming has been achieved by varying the amplitude of the sinusoidal voltage across the LEDs. Figure 3-17 (a) and (b) show measured and perceived light intensity with input voltage flickering at 100% and 16% light intensity respectively. Perceived illuminance for 16% dimming level is found to be 40%. The percent flicker has been calculated when the lamps are dimmed.

Measured and perceived percent flicker under various dimming levels applying same modulation index and same frequency flickering input voltage are given in Table 3-VI. The results indicate that dimming LEDs would increase the amount of flicker produced even though the perceived percent flicker is improved compared to the measured one. In other words, LEDs are more sensitive to flickering in the presence of dimming.

TABLE 3-VI PERCENT FLICKER UNDER DIFFERENT DIMMING LEVELS

Applied voltage	40V	60V	80V	100V	120V
Light intensity	7%	34%	66.5%	89.5%	100%
PF (measured)	66.28%	43.17%	25.02%	8.44%	4.4%
PF (perceived)	37.9%	22.7%	12.71%	4.23%	2.2%

3.5.5 Voltage Sag and Swell

This test aims to examine how LEDs would react in the presence of a voltage sage or a voltage swell. Different levels of voltage sag have been applied across the LEDs as shown in Figure 3-18. The voltage sag levels are 90%, 70% and 50% of nominal voltage respectively. The figure shows that at the event of a voltage sag, the LED voltage, which is the dc voltage applied to the LED string, will be affected and reduced as well. This happened because the LED driver interpreted this voltage reduction as a request to dim the LEDs. Hence, the controller will react to achieve a new

operating point driving the LED string at a lower voltage and a lower forward current. Since the light intensity of the LED changes linearly with its forward current, this reduction in the LED voltage, even if it is for a short time, will result in a corresponding decrease in the bulb output illuminance. This disturbance will cause a visible light flickering that might disrupt the end-user.

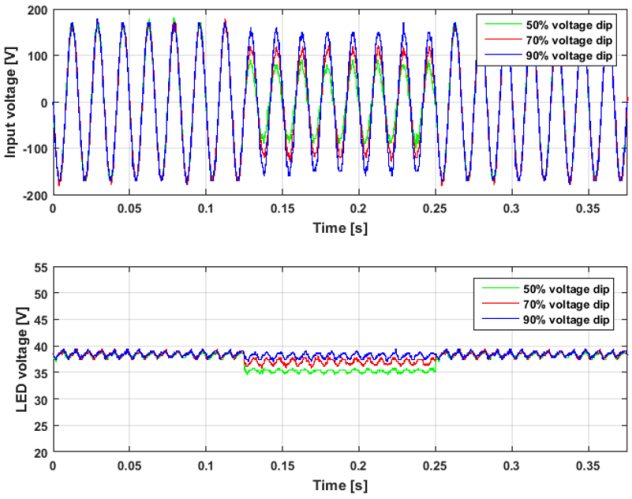
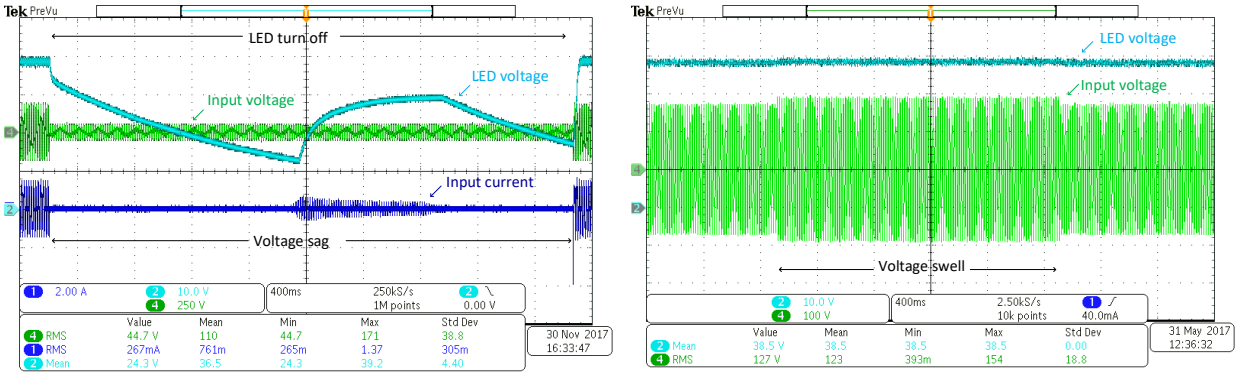


Figure 3-18. Voltage across the LED for different applied voltage sag levels.



(a) (b)

Figure 3-19. LED voltage at (a) 23% voltage sag (b) 110% voltage swell.

Furthermore, it has been observed that the lamps will malfunction and turn off for a voltage sag less than 25% of rated voltage as shown in Figure 3-19 (a). The figure shows that the LED

voltage reaches the new operating point quickly however the controller fails to maintain the new voltage level. As a result, the capacitor starts to discharge through the internal sensing resistors. The controller starts to react again to charge up the capacitor, but the energy provided by the input source was not large enough, therefore the controller fails again. During this period, the LEDs completely turn off until the voltage sag is over. The input current starts to increase charging up the capacitor until the operation reaches steady-state. This can be dangerous especially in street light applications, where it might distract the drivers and cause unexpected response that possibly lead to road accidents.

The sensitivity of LEDs to a voltage swell is similar to their sensitivity to a voltage sag. A voltage swell of 110% of nominal rated voltage has been applied to the LEDs as shown in Figure 3-19 (b). As a result, the voltage across the LEDs has increased respectively. The input power consumed by the 9 LEDs under test has also been increased to 112 W, which means for a large-scale of LEDs, a voltage swell might cause a sudden increase in the total network power demand.

3.6 Chapter Conclusion

The chapter presented characterization and evaluation of commercial dimmable LEDs through an experimental platform. Light intensity measurements, current and voltage waveforms were collected under numerous power quality conditions. The collected data were processed using MATLAB software tool. The results showed that the LEDs under test inject harmonic contents to the network that should not be ignored especially for applications that require a large number of connected LEDs. The results also indicated that the performance of LEDs is significantly affected by the quality of the grid. Flickering in LEDs light intensity was observed in response to various grid events. The amount of flicker produced by an LED lamp was found to be dependent on the

amplitude and the frequency of which the voltage variations occur. This stresses the need to develop a comprehensive power quality improvement technique for such an application.

Chapter 4 Transformerless Unified Power Quality Conditioner

4.1 Introduction

This chapter presents a transformerless power electronic apparatus (including topology and control strategy) to solve power quality issues of applying low cost LED lamps in lighting networks. The conceptual idea is shown in Figure 4-1. A transformerless unified power quality conditioner (TL-UPQC) is proposed as a comprehensive solution for the identified PQ issues related to LEDs presented in Chapter 3. The system is able to mitigate most of critical power quality issues including voltage dips, swells, flickering, current harmonics and low PF. The topology and its control methodology are proposed in this chapter. The TL-UPQC system gives the following advantages,

1. Transformerless – no transformer in between the VSC and the grid. It leads high efficiency and cost effective.
2. Low common-mode (CM) voltage – since transformer is absent, CM voltage and leakage current become significant. The topology can maintain low CM voltage due to the line connecting to the mid-point of the capacitor bank. The potential difference between the ac and dc grounds is clamped [113].

Part of the work described in this chapter has been published in the following paper: R. M. Abdalaal and C. N. M. Ho, "Transformerless single-phase UPQ for large scale LED lighting networks," in *Proc. IECON Ann. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 1629-1634.

3. Simple topology – the topology only has two active devices for each power stage, it is cost effective and reduce the complexity of controller design with less losses.

4. It provides high quality and stable load voltage for LED lighting network with grid voltage transient, e.g. voltage flickering, and steady, e.g. under- or overvoltage, issues.

5. It provides power factor correction and current harmonics elimination features.

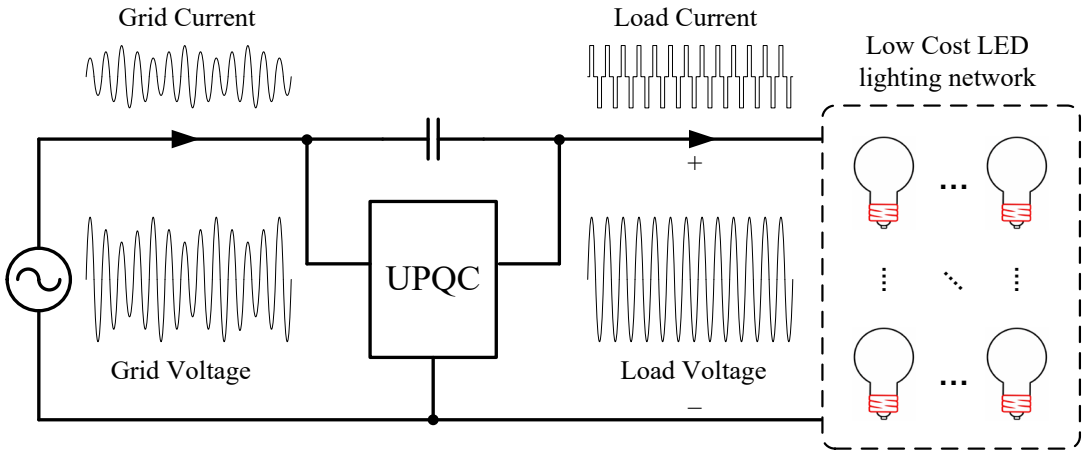


Figure 4-1. The conceptual idea of a TL-UPQC to solve PQ issues of a LED lighting network.

4.2 Proposed TL-UPQC Topology

4.2.1 Principle of operation

Figure 4-2 shows the detailed structure of the proposed single-phase TL-UPQC topology. The topology consists of a full-bridge converter which can be divided into two HB bi-directional VSCs [114], i) shunt APF to inject compensating reactive and harmonic currents, and ii) series APF, which will be referred to as DVR in this thesis, to compensate voltage flickering. The shunt converter is connected to the left side of the series converter.

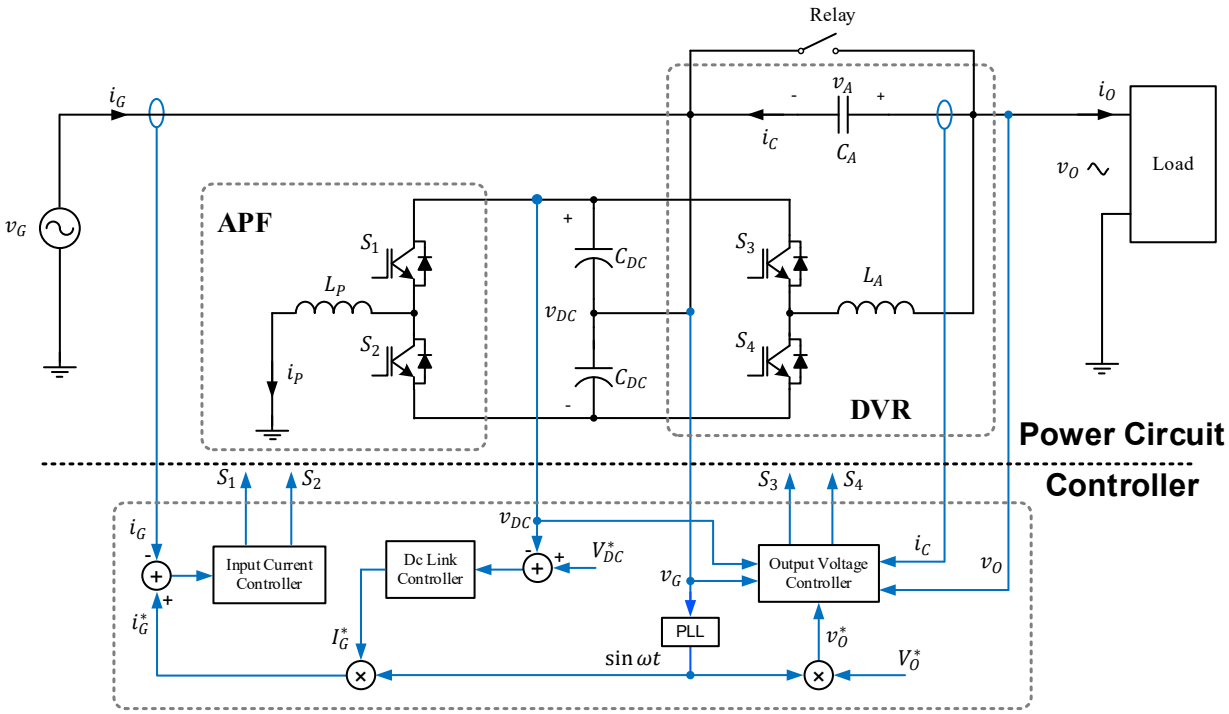


Figure 4-2. The proposed single-phase TL-UPQC.

The proposed strategy mitigates the critical PQ problems and satisfies the following two main objectives,

1. Provide sinusoidal and voltage in-phase current at the input.
2. Provide stable and sinusoidal voltage to supply LED lamps.

Figure 4-3 (a) shows the equivalent circuit of the proposed TL-UPQC system. The controlled current source represents the shunt APF that injects current harmonics and reactive current (i_P) to compensate the distorted current of the load (i_O) in order to shape the input current (i_G) to be sinusoidal and in-phase to the grid voltage (v_G). Thus, the relation of currents is,

$$i_G(t) = i_P(t) + i_O(t) \tag{4. 1}$$

The grid voltage and current relations are,

$$v_G(t) = \sqrt{2}\, V_G \sin \omega t \tag{4. 2}$$

$$i_G(t) = \sqrt{2}\, I_G \sin \omega t \tag{4. 3}$$

where V_G and I_G are the steady-state rms values of the grid voltage and current, respectively and ω is angular grid frequency.

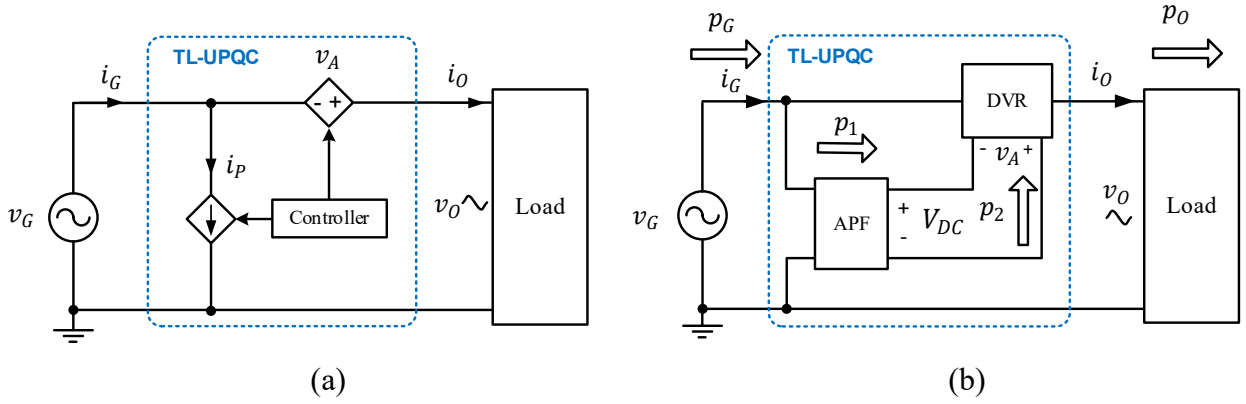


Figure 4-3. (a) Steady-state circuit model of the proposed TL-UPQC (b) a block diagram of power flow in the TL-UPQC system.

The DVR can be seen as a controllable voltage source (v_A) that is placed between the grid voltage (v_G) and the load (v_O). The relation of voltages is,

$$v_O(t) = v_G(t) + v_A(t) \tag{4. 4}$$

In order to regulate the load voltage, reference signal is applied to the DVR converter to define the controlled output voltage. This reference signal can take any value to control the voltage applied to the load. Therefore, this topology can be potentially used to perform as a dimmer for LEDs lighting network when the reference signal is provided externally, which will be implemented in the next chapter.

If there is a dynamic voltage change, e.g. voltage sag, or variation, e.g. flickering, the series DVR is responsible to quickly inject a voltage in series with the grid voltage to compensate the

difference between the nominal voltage and the required voltage to be applied [115], [116]. It can maintain the load voltage to be constant amplitude and high voltage quality. Practically, the DVR can be implemented by a dc-ac voltage source inverter, such as shown in Figure 4-2. It requires energy to maintain the compensating voltage during grid under voltage. Thus, a dc link controller is applied to bridge these two ac sources to exchange power between them and to balance the powers of input and output of the system. Figure 4-3 (b) shows the block diagram of the power flow in the system. The APF VSC works as a current filter to inject current to compensate the current harmonics of the load, meanwhile, it works as a rectifier to supply power to the DVR through the dc link. Thus, the dc link voltage (v_{DC}) is regulated by the dc link voltage controller by adjusting the amplitude of the grid current. The whole system achieves stable which means the input power (p_G) equals the output power (p_O), and the indicator is when the dc link voltage reaches steady-state, in other words, a constant value. The relation of the powers in steady-state is,

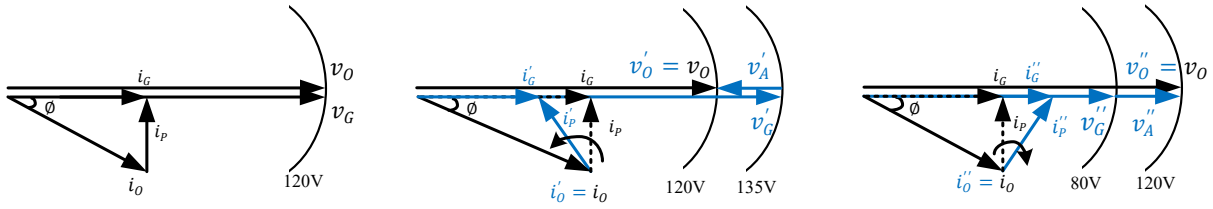
$$p_G(t) = p_1(t) - p_2(t) + p_O(t) \tag{4. 5}$$

In Summary, there are three controllers in the system, and they are shown in Figure 4-2. The functions of the controllers are as follows,

1. Output voltage controller – it is used to maintain the output voltage to be sinusoidal and constant amplitude. In addition, it quickly responds to transients including grid voltage changes.
2. Input current controller – it is used to shape the grid current to be sinusoidal and in-phase to the grid voltage.
3. Dc link voltage controller – it is used to maintain the dc link voltage between two VSCs in order to determine the power balancing point of input and output powers.

4.2.2 Series DVR Compensation Approach

The series DVR compensation approach followed in this topology is based on injecting a voltage that is in phase with the grid voltage for the event of a voltage sag. Accordingly, the injected voltage will be out of phase with the grid voltage to compensate for a voltage swell. Figure 4-4 shows the phasors diagram during normal operation, voltage swell and a voltage sag. v'_G, v'_O, v'_A, i'_G , i'_O and i'_P are the grid voltage, the output voltage, the injected voltage, the grid current, the output current and the shunt current values respectively during a voltage swell. While, v''_G, v''_O, v''_A, i''_G , i''_O and i''_P are the values during a voltage sag. There are three modes of operation; (a) UPQC operates in reactive power mode (b) UPQC absorbs energy through the series converter to compensate the excess power and (c) UPQC delivers energy through the series converter to compensate the missing power. In modes (b) and (c), the shunt converter under steady-state operation supplies the active power demand of the series converter.



(a) (b) (c)

Figure 4-4. Phasor diagrams of (a) normal operation (b) voltage swell (v) voltage sag.

It can be seen from the phasor diagrams that during a voltage sag, which happens more frequent in the network, the series converter will contribute to the reactive power delivery depending on the load phase angle ($\emptyset$). In this case, the DVR is delivering complex power. Hence, enhancing the utilization of the series converter as well as reducing the loading of the shunt converter supporting both the load reactive power demand and the series converter active power

demand during a voltage sag. It is worth mentioning that, since an L-UPQC topology is adopted for the proposed TL-UPQC system, the series DVR can also be controlled to adopt UPQC-Q compensation technique as well (refer to Chapter 2 subsection 2.2.3). However, if an R-UPQC is adopted with UPQC-Q compensation control methodolgy, the topology will be limited to compensate for a voltage sag and will not be able to compensate for a voltage swell.

4.3 Controller Design and Implementation

4.3.1 Control topology of APF

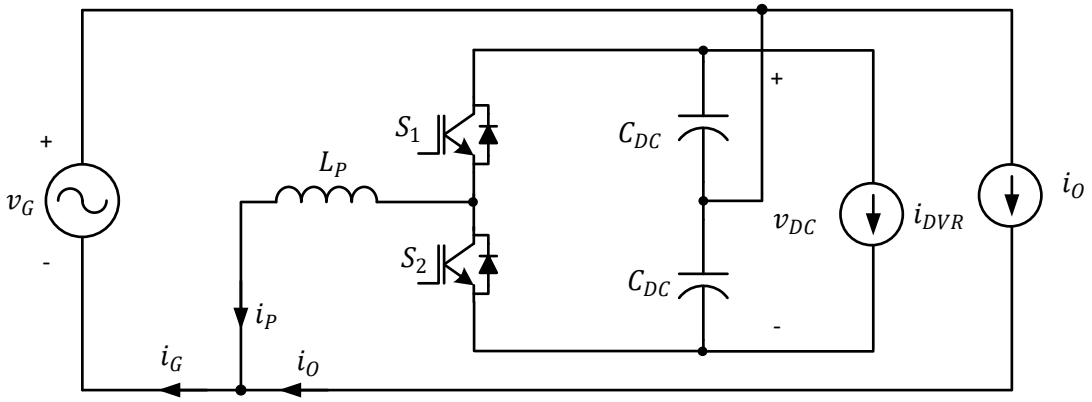


Figure 4-5. Half-bridge inverter configuration of APF.

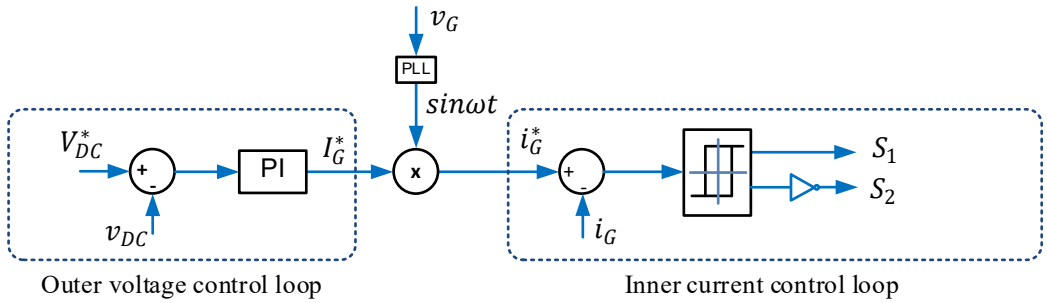


Figure 4-6. Control block diagram of the APF.

Figure 4-5 and Figure 4-6 show the APF circuit of the TL-UPQC and its controller block diagram. There are two controllers in the shunt APF, voltage controller and current controller. Both controllers can be implemented by either analog circuits or digital signal processer (DSP). The latter has been used in this study. The outer voltage control loop is a PI controller which is used to fix the dc link voltage and determine the reference for the inner loop. The inner current control loop is a hysteresis controller that shapes the input current by comparing it to a reference signal that is generated by the outer loop and phase locked loop (PLL). If neglecting the load current i_O in Figure 4-5, the system is a simple PFC, a source is connected to the dc link, while the grid current is the same as the inductor current. A reference current signal with specified upper and lower bands is formed to guide the inductor current following the reference.

Criteria of switching S_1 = on and S_2 = off

When the inductor current hits the lower band, the hysteresis controller will provide an action to change the operating mode of the switches and turn S_1 on, while S_2 is off so that the inductor current starts charging. Thus, the switching criteria will be,

$$i_P(t) \leq i_P^*(t) - \frac{\Delta I_p}{2} \tag{4. 6}$$

where ΔI_P is the inductor current hysteresis ripple band, and $i_P^*(t)$ is reference inductor current.

Criteria of switching S_1 = off and S_2 = on

When the inductor current hits the upper band, the controller will give an action to turn off S_1 and turn on S_2. Therefore, the inductor current starts discharging. The switching criteria will be,

$$i_P(t) \geq i_P^*(t) + \frac{\Delta I_p}{2} \tag{4. 7}$$

For the TL-UPQC system, the APF circuit is connected in parallel to the source as shown in Figure 4-5. Considering the load current to be constant, the grid current ripple is the same as the inductor current ripple. Therefore, a reference signal for the grid current can be formed to compare it with the actual grid current. Equations (4.20) & (4.21) can be rewritten as,

Criteria of switching S_1 = on and S_2 = off

$$i_G(t) \leq i_G^*(t) - \frac{\Delta I_g}{2} \tag{4. 8}$$

Criteria of switching S_1 = off and S_2 = on

$$i_G(t) \geq i_G^*(t) + \frac{\Delta I_g}{2} \tag{4. 9}$$

where ΔI_g is the inductor current hysteresis ripple band, and $i_G^*(t)$ is reference grid current.

4.3.2 Control Methodology of DVR

Figure 4-7 shows the DVR inverter circuit of the TL-UPQC given in Figure 4-2. It is a typical half-bridge voltage source inverter (HBVSI). For the series DVR, the control methodology is based on boundary control with second order switching surface (BCSSS) in which the switching trajectory is used to predict the moves of voltages and currents of passive components, and then gives switching decisions (gate signals) to the inverter at the right moment [114]-[116]. These predictions ensure a very fast dynamic response to any external disturbance. Figure 4-8 indicates the switching trajectories of the DVR system for a resistive load on the state plane $(v_A - i_L)$, which

have been obtained solving the state-space equations of the system. The solid lines represent the on state trajectory, while the dotted lines represent the off state trajectory. The figure shows that the system operating points are realized following the switching trajectories with a defined reference voltage band.

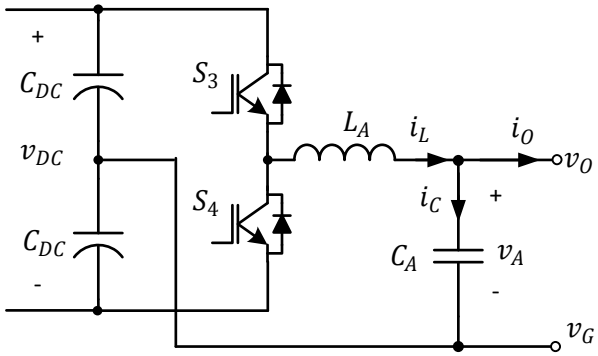


Figure 4-7. Half-bridge inverter configuration of DVR.

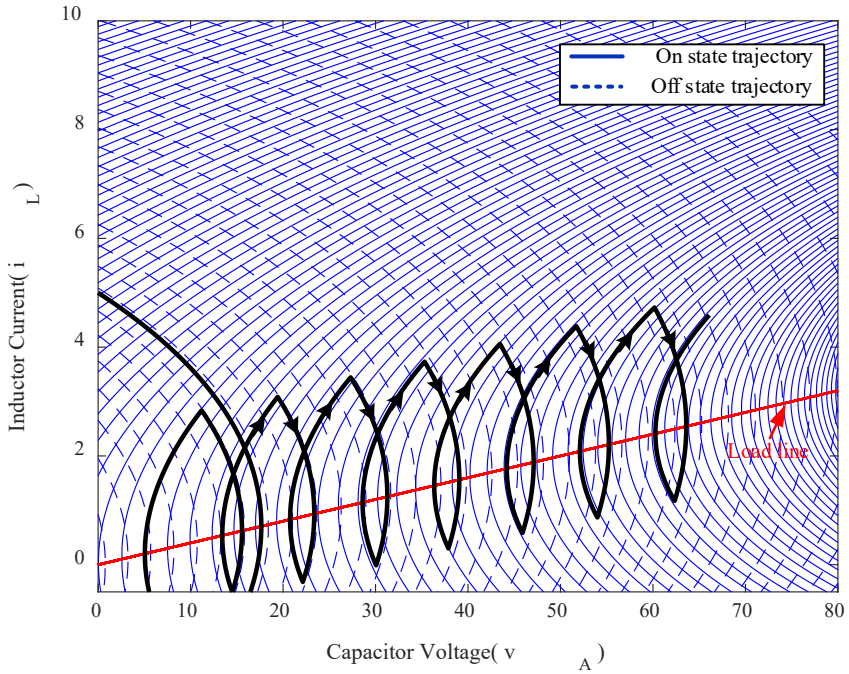


Figure 4-8. Switching trajectories of DVR.

The output of the inverter is used to add the missing voltage between the source voltage and the load voltage to satisfy (4.4). For a simple HBVSI, the switching criteria of the topology with BCSSS have been derived as follows,

Criteria of switching S_3 = on and S_4 = off

$$v_A(t) - v_{A,min} - \left[\frac{k_A}{\frac{v_{DC}}{2} - v_A(t)}\right] i_C^2(t) \leq 0 \tag{4. 10}$$

$$\& \; i_C(t) \leq 0 \tag{4. 11}$$

Criteria of switching S_3 = off and S_4 = on

$$v_A(t) - v_{A,max} + \left[\frac{k_A}{\frac{v_{DC}}{2} + v_A(t)}\right] i_C^2(t) \geq 0 \tag{4. 12}$$

$$\& \; i_C(t) \geq 0 \tag{4. 13}$$

where k_A represents a constant value and it is,

$$k_A = \frac{L_A}{2C_A} \tag{4. 14}$$

$v_{A,min}$ and $v_{A,max}$ are minimum boundary and maximum boundary of reference signal, respectively,

$$v_{A,min} = v_A^*(t) - \Delta V \tag{4. 15}$$

$$v_{A,max} = v_A^*(t) + \Delta V \tag{4. 16}$$

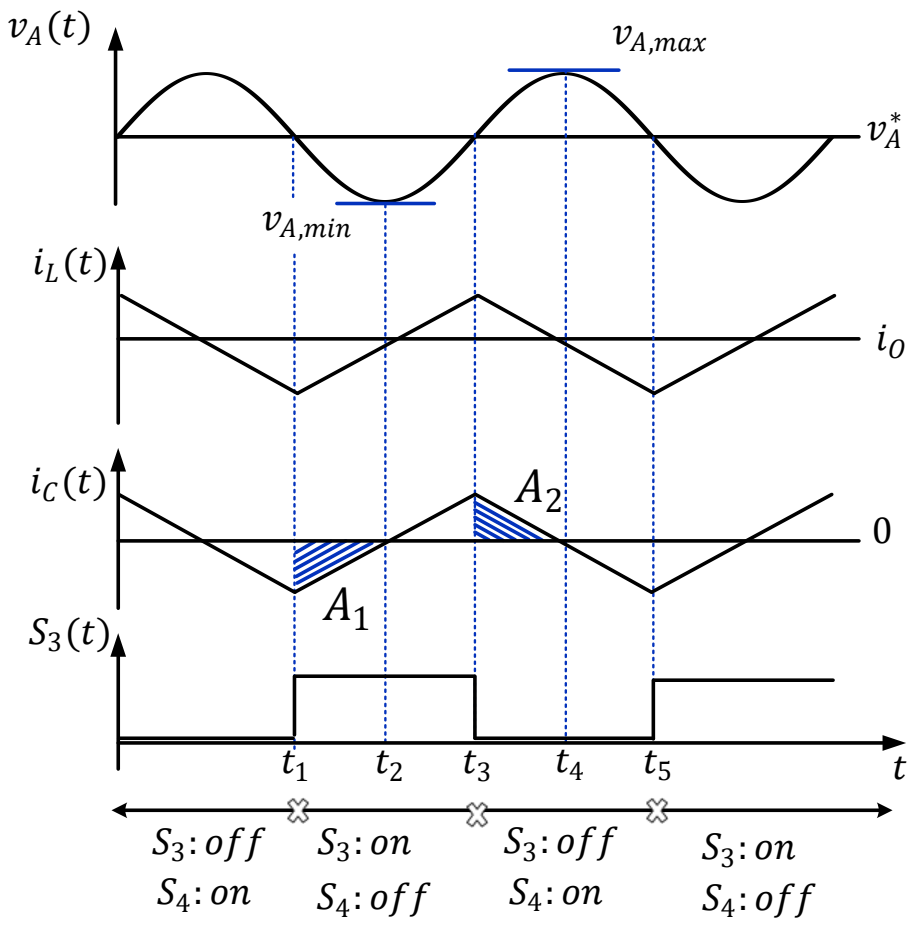


Figure 4-9. Typical waveforms of the DVR [116].

ΔV is hysteresis voltage ripple band. The definition can be found on the waveforms in Figure 4-9. Detailed derivation of equations (4.10) – (4.13) are given in Appendix A.2 [116].

The control objective of the DVR in the UPQC is to maintain the output voltage to be constant amplitude. Thus, the reference signal can be transferred to the output voltage based on (4.4),

$$v_A^*(t) = v_o^*(t) - v_G(t) \tag{4. 17}$$

where $v_o^*(t)$ is the reference load voltage.

By substituting (4.4) and (4.17) into (4.10) – (4.13) to cancel all terms related to $v_A(t)$, the new switching criteria will be,

Criteria of switching S_3 = on and S_4 = off

$$v_O(t) - v_{O,min} - \left[\frac{k_A}{\frac{v_{DC}}{2} - v_O + v_G}\right] i_C^2(t) \leq 0 \tag{4. 18}$$

$$\& \; i_C(t) \leq 0 \tag{4. 19}$$

Criteria of switching S_3 = off and S_4 = on

$$v_O(t) - v_{O,max} + \left[\frac{k_A}{\frac{v_{DC}}{2} + v_O - v_G}\right] i_C^2(t) \geq 0 \tag{4. 20}$$

$$\& \; i_C(t) \geq 0 \tag{4. 21}$$

$$v_{O,min} = v_O^*(t) - \Delta V \tag{4. 22}$$

$$v_{O,max} = v_O^*(t) + \Delta V \tag{4. 23}$$

The amplitude of $v_o^*(t)$ is regulated at a desired rms value with the same frequency of the grid voltage. The load reference voltage v_o^* is generated by the PLL following the sinusoidal input voltage v_G. The gate signals to the switches are determined by the switching criteria of (4.18) - (4.21). Figure 4-10 shows the implementation of the boundary control conditions in a DSP by following the two switching criteria that have been developed from the steady-state characteristics [117]. The output reference voltage amplitude is assigned externally, and with the feedback signals from the UPQC power circuit, the inequalities of the switching criteria are checked and provide

switching actions. From which, a high voltage quality at the load can be obtained.

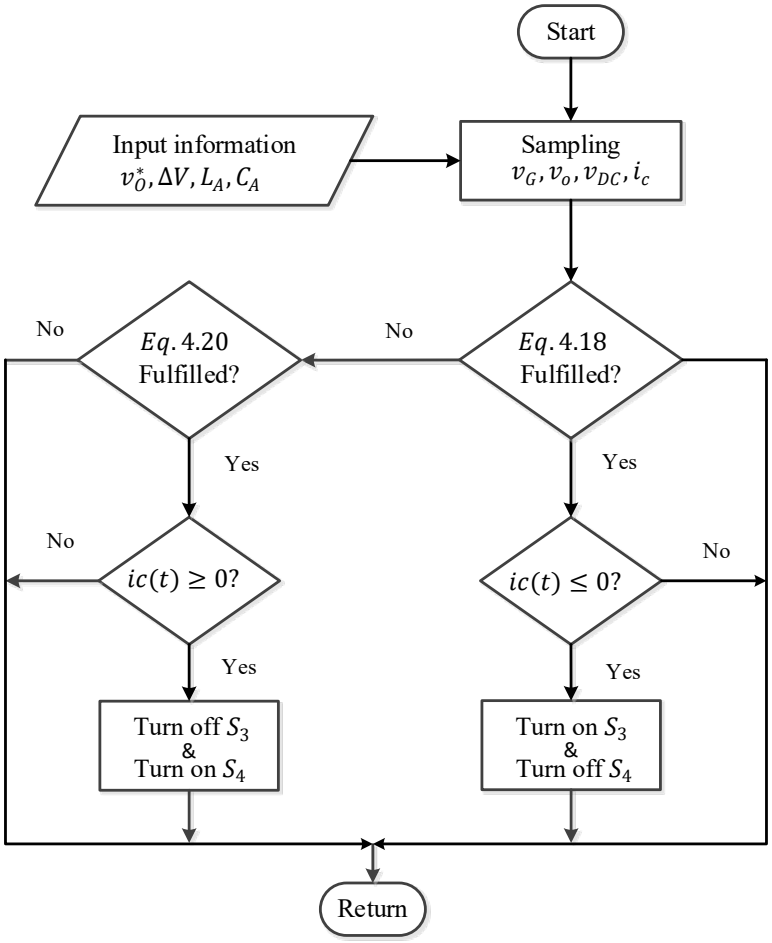


Figure 4-10. Flow chart of boundary control law.

4.4 System modeling and Characterization

In order to analyze the dynamic behaviors of the system, small-signal models are determined.

4.4.1 State space model of APF

As presented before, there are two controllers in the shunt APF; voltage controller and current

controller. The output of the control loop is the dc link voltage. The outer voltage control loop is used to fix the dc link voltage. Therefore, the output of the control loop is the dc link voltage. The controller $T_c(s)$ generates a control signal that is together with the output of the PLL used to generate the grid reference current. The inner current control loop shapes the input current by comparing it to the generated reference signal. The power plant $T_p(s)$ includes the inner control loop $T_{in}(s)$ and the shunt inverter transfer functions $T_{dc}(s)$. The small-signal control diagram is illustrated in Figure 4-11.

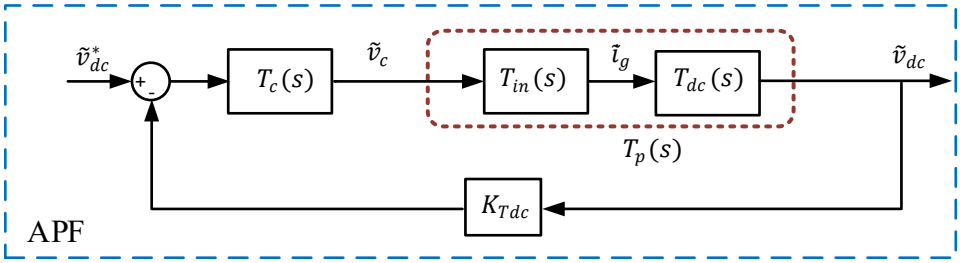


Figure 4-11. Small-signal control block diagram of the shunt APF converter.

The state space model of the converter can be found by determining circuit equations of the APF. The state variables are basically energy storage elements of the system. State matrix A, input matrix B, output matrix C and direct transition matrix D are formed by finding the switching equivalent circuits of the proposed topology. The "on time" is denoted by dT_{s_1}, while the "off time" is donated by $(1-d)T_{s_1}$, where T_{s_1} is switching periodic time of the APF converter. For each interval, the system can be described by a set of linear time invariant equations as follows,

$$\dot{x}(t) = A_1 x(t) + B_1 u(t), \text{ during } dT_{s_1} \tag{4. 24}$$

$$\dot{x}(t) = A_2 x(t) + B_2 u(t), \text{ during } (1-d).T_{s_1} \tag{4. 25}$$

$$y(t) = C_1 x(t) + D_1 u(t), \text{ during } d.T_{s_1} \tag{4. 26}$$

$$y(t) = C_2 x(t) + D_2 u(t), \text{ during } (1-d).T_{s_1} \tag{4. 27}$$

Let $$x(t) = \begin{bmatrix} i_G \\ v_{DC} \end{bmatrix}, u(t) = v_G(t), \; y(t) = \begin{bmatrix} v_{DC} \\ i_G \end{bmatrix} \tag{4. 28}$$

Defining the switching function $q_1(t)$,

$$q_1(t) = \begin{cases} 1 & S_1\ off, S_2\ on \\ 0 & S_1\ on, S_2\ off \end{cases} \tag{4. 29}$$

State space matrices are determined using circuit analysis and circuit equations from which,

$$A_1 = \begin{bmatrix} 0 & \frac{-1}{2L_p} \\ \frac{1}{C_{DC}} & 0 \end{bmatrix}, \; A_2 = \begin{bmatrix} 0 & \frac{1}{2L_p} \\ \frac{-1}{C_{DC}} & 0 \end{bmatrix}, \; B_1 = B_2 = \begin{bmatrix} \frac{1}{L_P} \\ 0 \end{bmatrix} \tag{4. 30}$$

$$C_1 = C_2 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \; D = 0 \tag{4. 31}$$

By introducing small perturbation and linearizing the system around one operating point,

$$x(t) = X + \tilde{x}(t), d(t) = D + \tilde{d}(t), \; v_{DC}(t) = V_{DC} + \tilde{v}_{dc}(t), i_G(t) = I_G + \tilde{\imath}_g(t) \tag{4. 32}$$

where D, V_{DC} and I_G are the steady-state values, while $\tilde{d}, \tilde{v}_{dc}$ and $\tilde{\imath}_g$ are the ac small-signals of d, v_{DC} and i_G respectively.

Based on averaging the state-space equations and transforming into Laplace domain, the transfer functions of the power stage can be obtained,

$$\frac{\tilde{v}_{dc}(s)}{\tilde{d}(s)} = \frac{4I_G L_P s - 2V_{DC}(2D-1))}{2L_P C_{DC} S^2 + (2D-1)^2} \tag{4. 33}$$

$$\frac{\tilde{\imath}_g(s)}{\tilde{d}(s)} = \frac{-[2V_{DC} C_{dc} s + 2I_G(2D-1)]}{2L_P C_{DC} s^2 + (2D-1)^2} \tag{4. 34}$$

In the small-signal model, harmonic components in the load current are neglected as the dynamic of the system is slower than that of harmonics. The fundamental components are considered in the analysis. An assumption of the current control loop is fast enough will not be dynamically affecting the voltage control loop. Therefore, the perturbation in duty cycle can be neglected ($\tilde{d}(s) = 0$). The transfer function of the inverter will be,

$$T_{dc}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{\imath}_g(s)} = \frac{2V_{G,rms}}{C_{DC}\,V_{DC}\,s} \tag{4. 35}$$

The grid current $i_G(t)$ is the same shape as its reference signal with current sensor gain, thus the transfer function of the inner loop $T_{in}(s)$ and the process $T_p(s)$ are,

$$T_{in}(s) = \frac{\tilde{\imath}_g(s)}{\tilde{v}_c(s)} = \frac{K_{PLL}}{\sqrt{2}K_{Ti}} \tag{4. 36}$$

$$T_p(s) = T_{in}(s) \cdot T_{dc}(s) = \frac{2\,K_{PLL}V_{G,rms}}{\sqrt{2}K_{Ti}C_{DC}\,V_{DC}\,s} \tag{4. 37}$$

where K_{Ti} is the sensor gain of the grid current and $K_{PLL}$is the PLL gain.

A PI controller is applied to control the overall process, which has the following transfer function,

$$T_c(s) = \frac{\tilde{v}_c(s)}{\tilde{v}_{dc}(s)} = K_{Tdc}\,\frac{(K_P s + K_I)}{s} \tag{4. 38}$$

where K_{Tdc} is the sensor gain of the dc link voltage.

The controller proportional and integral gains are designed such that the crossover frequency is at least ten times lower than the 2nd harmonic of the grid frequency. The frequency response of the overall open loop system can be found by combining the process and controller transfer functions,

$$T_{OL}(s) = T_c(s).T_p(s) = \frac{2\,K_{Tdc}K_{PLL}V_{G,rms}(K_P s+K_I)}{\sqrt{2}K_{Ti}C_{DC}\,V_{DC}\,s^2} \quad (4.\ 39)$$

Figure 4-12 shows the mathematical model frequency responses of the power stage, controller and overall open loop system. The system is stable with a crossover frequency of $\omega_c = 5.76\ rad/sec$ and phase margin of 49^o.

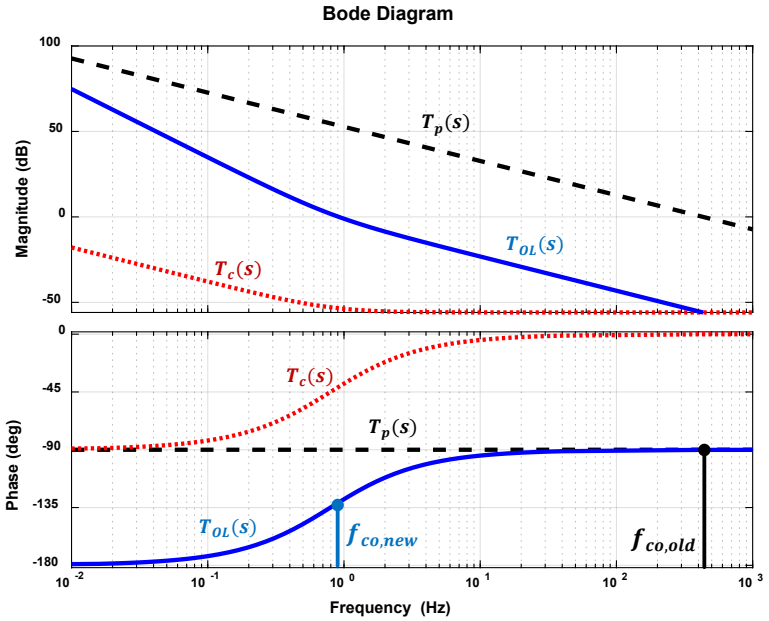


Figure 4-12. Frequency response of power stage (T_p), controller (T_c) and Overall open loop system (T_{OL}).

4.4.2 State space model of DVR

There are two modes of S_3 and S_4, in which they are operating opposite to each other and independent from S_1 and S_2. The converter's state space equations can be derived as follows,

$$\dot{x}(t) = \begin{bmatrix} 0 & -\frac{1}{L_A} \\ \frac{1}{C_A} & -\frac{1}{C_A R} \end{bmatrix} x(t) + \begin{bmatrix} \frac{2q_2(t)-1}{2L_A} & 0 \\ 0 & -\frac{1}{C_A R} \end{bmatrix} u(t) \quad (4.\ 40)$$

$$\text{and,} \qquad y(t) = [0 \quad 1]\, x(t) \tag{4. 41}$$

$$\text{where,} \qquad x(t) = \begin{bmatrix} i_L \\ v_A \end{bmatrix} \ , u(t) = \begin{bmatrix} v_{DC} \\ v_G \end{bmatrix},\ y(t) = v_A \tag{4. 42}$$

The converter's state variable equations are represented by,

$$\frac{di_L}{dt} = \frac{1}{L_A}\left[\frac{v_{DC}}{2}(2d_2(t) - 1) - v_A\right] \tag{4. 43}$$

$$\frac{dv_A}{dt} = \frac{1}{C_A}\left(i_L - \frac{v_A + v_G}{R}\right) \tag{4. 44}$$

where $d(t)$ is average of converter a switching function $q(t)$ that is defined as follows,

$$q_2(t) = \begin{cases} 1 & S_3\ on, S_4\ off \\ 0 & S_3\ off, S_4\ on \end{cases} \tag{4. 45}$$

At steady-state equilibrium point, the duty ratio D_2 of the series converter can be found. It will be a time varying quantity. Its value depends on the amount of the input voltage and the desired output voltage as a sinusoidal waveform,

$$D_2(t) = \frac{v_o(t) - v_G(t)}{v_{DC}} + \frac{1}{2} \tag{4. 46}$$

The boundary control with a second-order switching surface has a fast-dynamic response. $T_{ps}(\mathrm{s})$ and $T_{bc}(s)$ represent the transfer function of the power stage and the controller respectively as shown in Figure 4-13. The closed loop transfer function of the system $G_{BC}(s)$ is expressed as follows [118],

$$G_{BC}(S) = \frac{\tilde{v}_O(s)}{\tilde{v}^*{}_O(s)} = \frac{1}{\frac{T_{S_2}}{4}s + 1} \tag{4. 47}$$

where T_{s_2} is switching period of the DVR converter.

The frequency response of the boundary control is shown in Figure 4-14, in which the boundary control simplifies the system into a first order system that acts as a LPF with a bandwidth of 6.35 kHz.

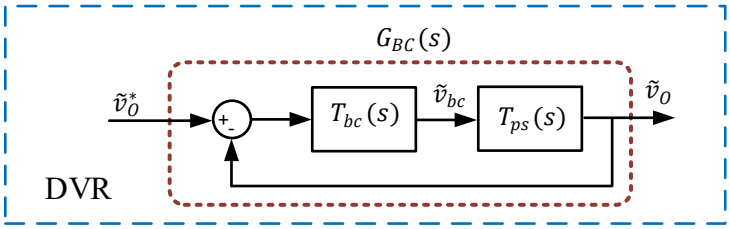


Figure 4-13. Small-signal control block diagram of the DVR converter.

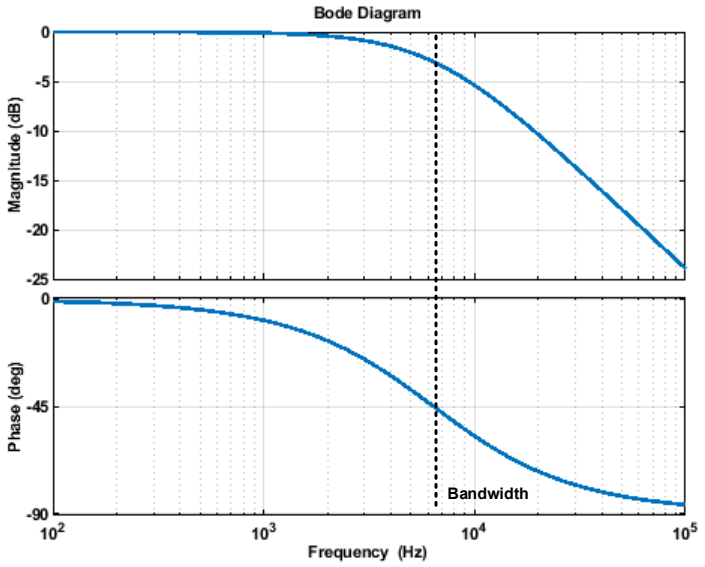


Figure 4-14. Frequency plot of boundary control.

4.5 TL-UPQC Sizing

The TL-UPQC system is sized according to the amount of voltage sag/swell that is required to be compensated. Assume k to be the percent amount of the main supply voltage after a voltage sag/swell in the network, then v_G' and i_G' which are the voltage and current after a sag/swell can be expressed as [49],

$$v'_G(t) = kv_G(t) \quad \& \quad i'_G(t) = \frac{i_G(t)}{k} \tag{4. 48}$$

The load active and reactive power P_O, Q_O will remain constant under voltage disturbances. S_1 and S_2 represent the VA loading of the shunt and the series converters respectively. As the shunt converter is placed to the left of the series one, the apparent power that is handled by the series converter will be the product of the series injected voltage and the load current as follows,

$$|S_2| = |V_O - V'_G||I_O| = |1 - k|V_G I_O \tag{4. 49}$$

The output voltage is in phase with the grid voltage. Therefore, the active and reactive power handled by the series converter will depend on the phase angle of the load. Thus, if there's a voltage sag in the network, not only the series converter injects active power to support the load, as per the power balance indicates in (4.5), but also shares the load reactive power demand beside the shunt converter as follows,

$$P_2 = (1 - k)V_G I_O \cos\emptyset\,,\ Q_2 = (1 - k)V_G I_O \sin\emptyset \tag{4. 50}$$

The shunt converter VA loading will depend on how much voltage sag/swell exists in the network. The reactive power supported will also depend on the sag/swell index *k* as follows,

$$|S_1| = |kV_G||I_P| \tag{4. 51}$$

and, $$I_P = \sqrt{I_O^2 + I_G'^2 - 2I'_G I_O \cos\emptyset} \tag{4. 52}$$

The active power absorbed by the shunt converter is to compensate for the corresponding power supplied by the converter as follows,

$$P_1 = P_2 \tag{4. 53}$$

At steady-state, there will be no reactive power supplied by the grid to achieve unity PF. Therefore, the reactive power of the shunt converter will depend on that required by the load taking into consideration the reactive power sharing of the series converter as follows,

$$Q_1 = Q_2 - Q_O = -kV_G I_O \sin \emptyset \tag{4. 54}$$

The total VA of the L-UPQC topology can be found,

$$S_{UPQC} = S_1 + S_2 \tag{4. 55}$$

The design value of L_P will depend on the shunt inductor ripple current. Assuming that the grid current ripple ΔI_G is the same as the inductor current ripple then,

$$L_P = \frac{v_{DC}}{4 f_{s_1} \Delta I_G} \tag{4. 56}$$

where f_{s_1} is the switching frequency of the APF converter.

The DVR filter components L_A and C_A are designed based on [116]. The selection of L_A will depend on the output current,

$$L_A < \frac{v_{L_A}}{2\pi f \, I_{O,max}} \tag{4. 57}$$

where $v_{L_A} and \, f$ are the voltage drop across L_A and the fundamental line frequency respectively.

The resonant frequency of the converter is required to be at least 10 times (e.g. $x = 0.1$) lower than the switching frequency of the DVR converter f_{s_2},

$$\frac{1}{\sqrt{L_A C_A}} = x. 2\pi f_{s_2} \tag{4. 58}$$

The maximum current that will go through the DVR will depend on the maximum output current plus the inductor ripple current ΔI_{L_A},

$$I_{L_{A,max}} = I_{O,max} + \Delta I_{L_A} \tag{4. 59}$$

4.6 Experimental Verifications

A 500VA/120V UPQC converter prototype with DSP controller has been implemented to experimentally verify the proposed converter. The system parameters are given in Table 4-I. Various PQ problems have been tested to evaluate the performance of the TL-UPQC.

TABLE 4-I SYSTEM PARAMETERS

Parameters	Value
Nominal ac voltage	120 V
Grid frequency	60 Hz
Dc link voltage	400 V
L_P	10 mH
L_A	3.4 mH
C_A	14.1 μF
C_{DC}	1500 μF
f_{s_1}	10 kHz
f_{s_2}	10 kHz

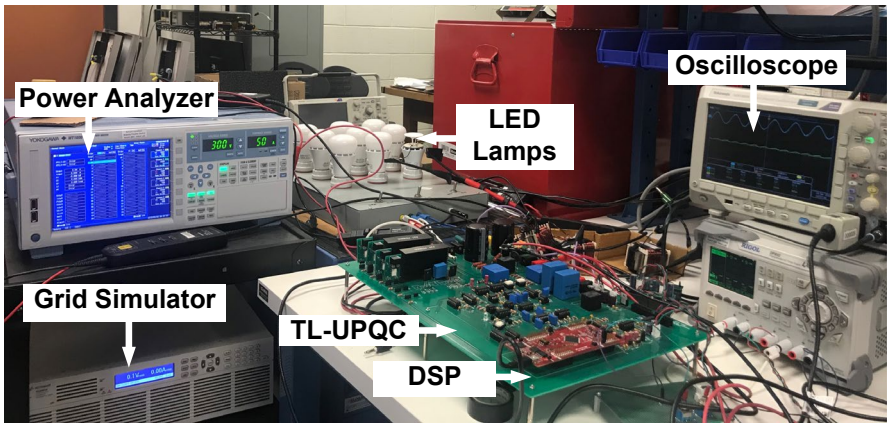


Figure 4-15. Experimental setup.

The laboratory setup, shown in Figure 4-15, consists of a programmable ac power source to simulate the grid for different power quality problems like voltage flickering, voltage sag and swell. The TL-UPQC prototype is connected to the ac source through a relay to bypass the system in case of faults. The output of the system is connected to linear and nonlinear loads. A power analyzer is used to investigate the harmonic contents in the waveforms. The control law has been implemented using Texas Instruments TMS320F28377S. The sampling frequency of the high frequency signal is 500 kHz while the low frequency signals are sampled with 50 kHz. The switching frequency of both converters has been chosen to be 10 kHz. Higher sampling frequency is required for higher switching frequency. Two enhanced pulse width modulation (ePWM) have been deployed with a dead band of 6 µs.

4.6.1 Verifications of Mathematical Model

In order to validate the mathematical model, ac sweep analysis were performed on PLECS simulation model. A perturbation signal has been defined by specifying the frequency sweep range and the number of points on a logarithmic scale. In addition, an experiment test has been employed to analyze the stability of the system using Bode100 gain-phase analyzer. For the test purpose, a

small resistance is added to inject a disturbance signal. The Bode100 will provide the disturbance signal and measures the loop gain of the system through a wide-band injection transformer (WIT-100) that is used for a wide range of frequencies from 1 Hz to 10 MHz. As a result, there will be some limitations injecting the full signal at very low frequencies. Figure 4-16 indicates the suitable injection point in which the perturbation is added to the feedback loop. Figure 4-17 shows good agreement between the mathematical, circuit simulation model results and the measured magnitude and phase.

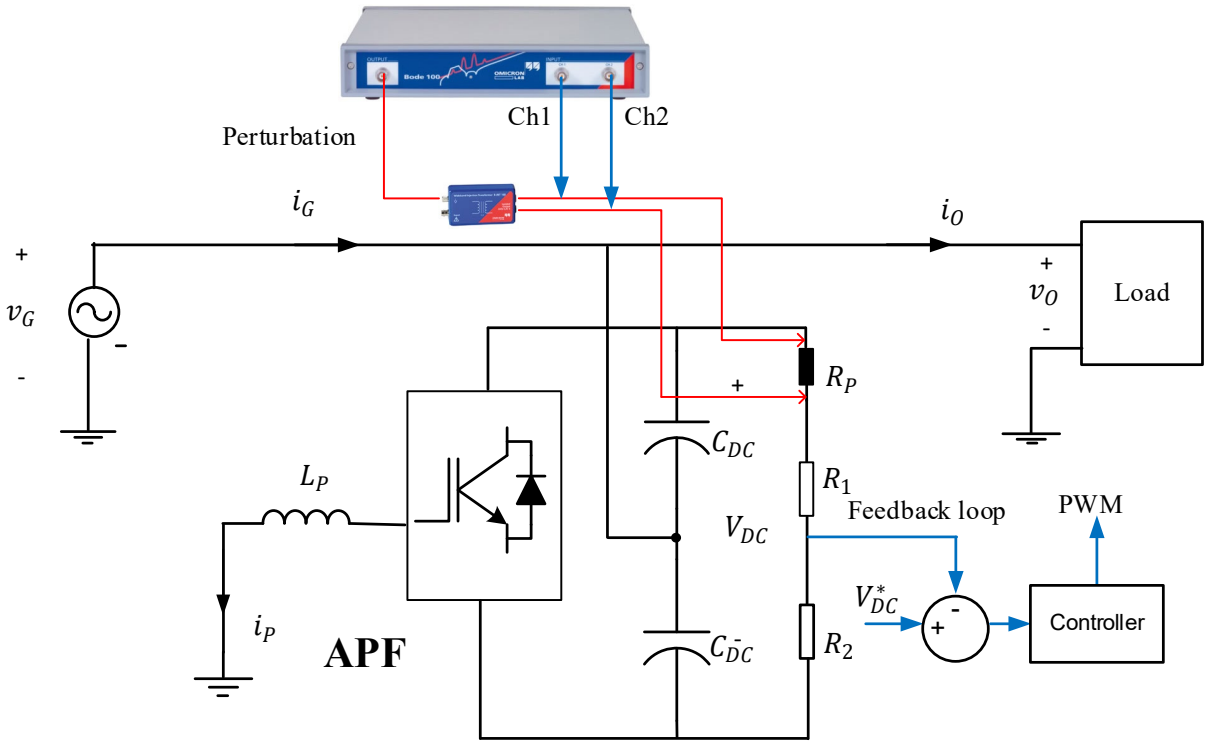


Figure 4-16. Connection diagram for frequency response analyzer Bode100.

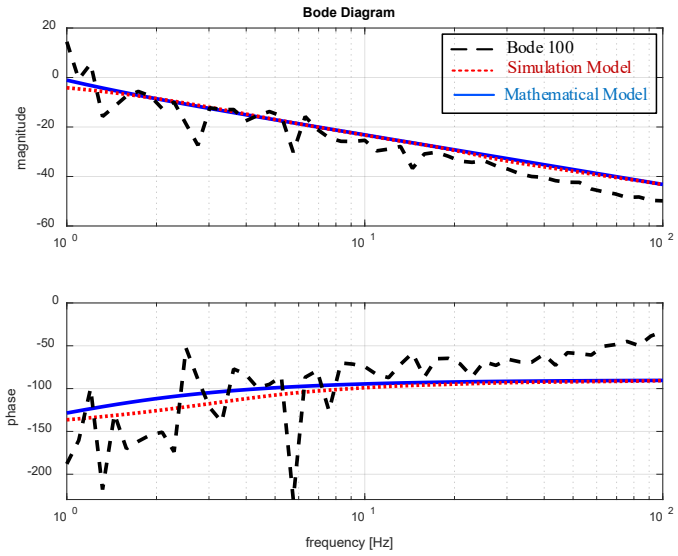
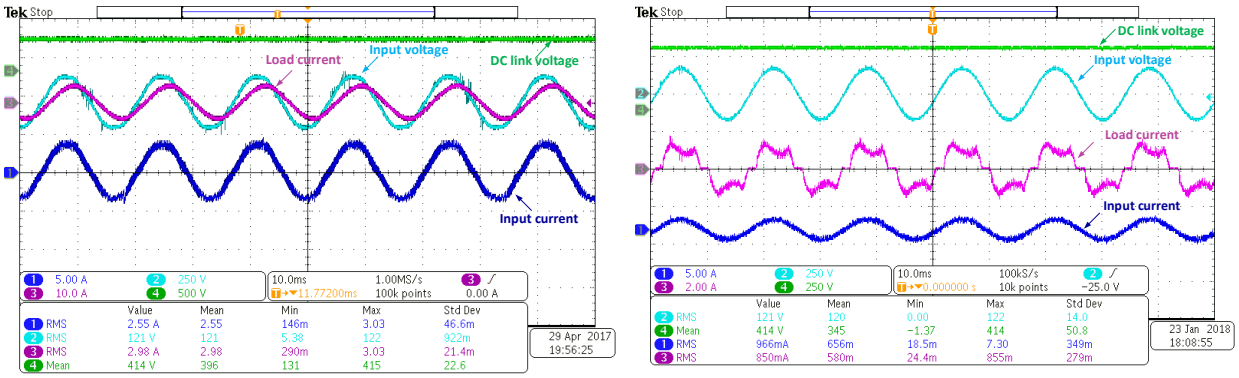


Figure 4-17. Frequency response of mathematical model, simulation and experiment.

4.6.2 Results of Reactive Power Compensation and Current Harmonics Elimination

Two types of loads have been used: linear and nonlinear loads. The linear load consists of a resistor and an inductor to represent reactive power delivery of the APF. The nonlinear load consists of the same 9 LED bulbs that have been used and tested in Chapter 3 section 3.4. The LEDs are tested to show the ability of the system to mitigate harmonics. The results for both loads are shown in Figure 4-18. The dc link has been maintained at a constant value of 400 V. By observing the dc link voltage, grid voltage, grid current and load current, it can be seen in both cases that the input current can be controlled as a sinusoidal waveform with the same phase as the input voltage, i.e. power factor is approximately to 1. In other words, the APF has compensated reactive power for the linear load and all harmonic contents for the nonlinear load. Table 4-II gives the power analysis measurements including PF and THD_i of the current drawn by the LED lamps and the input current after enabling the TL-UPQC system. The results show enhanced current

quality parameters compared to the system acting alone. The TL-UPQC meets the standard IEEE 519 requirements of maintaining the THD_i to be below 5%.



(a) (b)

Figure 4-18. APF experimental results with (a) linear (b) nonlinear load.

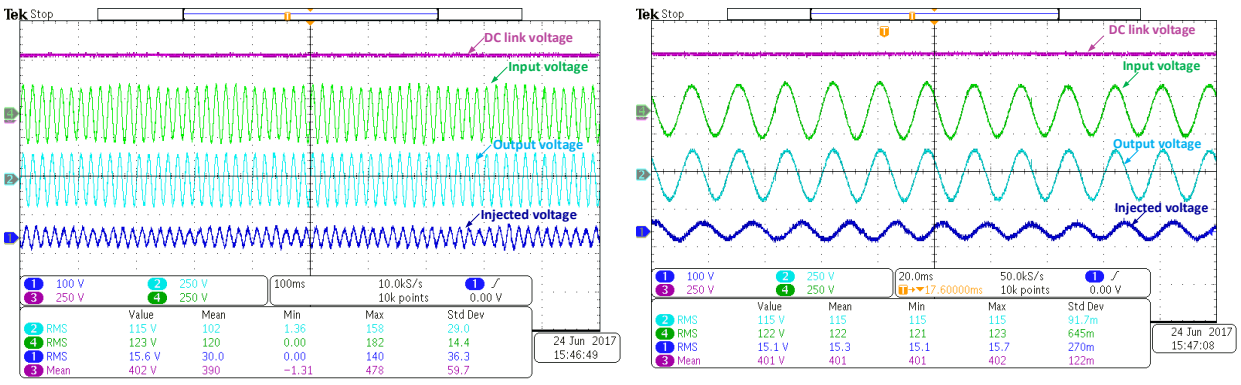
TABLE 4-II MEASURED POWER ANALYSIS PARAMETERS WITH CONNECTION TO A NONLINEAR LOAD

Parameters	Load current	Input current
I_{rms}	850 mA	966 mA
PF	0.94414	0.992
THD_i	31.104%	2.656%

4.6.3 Results of Voltage Variations and Flickers Elimination

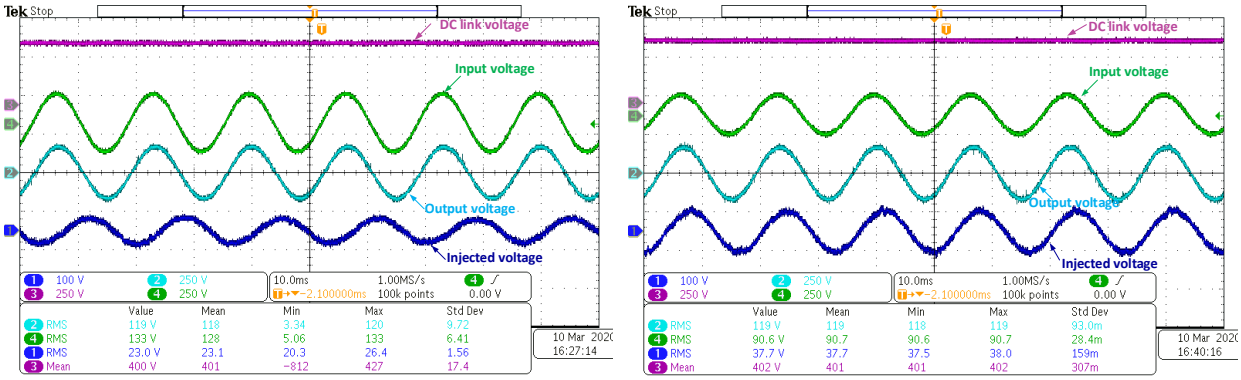
In order to simulate the visual flickering phenomena in LED lamps, a modulated waveform signal of 6Hz in the input voltage has been generated and shown in Figure 4-19 (a). A smaller time division is shown in Figure 4-19 (b) to confirm the quality of the generated output voltage waveform. The results show the ability of the system to eliminate flickering since the output voltage has been maintained as a sinusoidal waveform with a constant peak value. The DVR sources the power from the dc link capacitor and injects voltage to support the load voltage.

Moreover, the DVR supports the network under different circumstances. A constant output voltage of 120V rms is delivered for an over input voltage of 135V shown in Figure 4-20 (a). A stable voltage of 120V rms is also delivered for an under voltage of 90V rms as shown in Figure 4-20 (b). For a better insight of the dynamic response of the controller, a voltage sag of 25% in rms input voltage has been applied in Figure 4-21 (a), while the output voltage has been restored to 120V rms. The dc link has been able to restore the injected power through the parallel converter. The enlarged waveforms in Figure 4-21 (b) show the fast-dynamic response of the controller to support the network in 200 µs. Figure 4-22 shows that the output voltage has been maintained at a constant value for a voltage swell of 10% in input voltage. The high power quality performance of the UPQC system has been achieved with a maintained output voltage and sinusoidal, in phase input current with high PQ parameters as illustrated in Table 4-II.



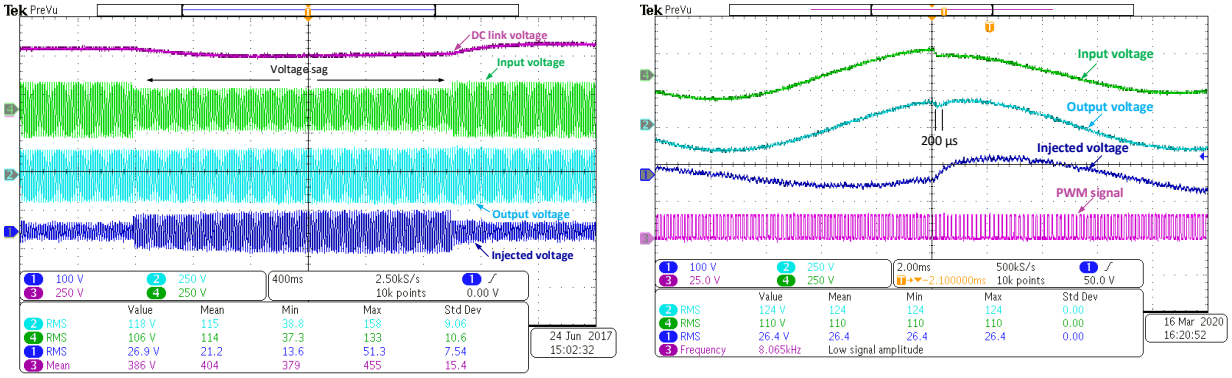
(a) (b)

Figure 4-19. DVR results for voltage flickering of 6Hz (a) 100 ms/div (b) 20 ms/div.



(a) (b)

Figure 4-20. DVR results for (a) over voltage 135V (b) under voltage 90V.



(a) (b)

Figure 4-21. Voltage sag waveforms in time scale of (a) line cycle, and (b) switching cycle.

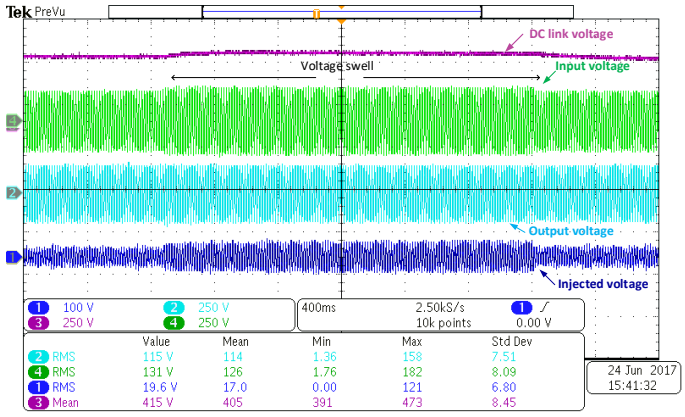


Figure 4-22. Voltage waveforms for input voltage swell.

4.7 Chapter Conclusion

The performance of a TL-UPQC for LED lighting networks was demonstrated in this chapter. Power control was used to balance the input and output powers of the APF using a capacitor bank voltage. The results verified that APF turned unity PF and filtered out the harmonics generated by LED light blubs as well as compensated all voltage fluctuations in the supply voltage to prevent LED flickering. The system can solve the critical dynamic and static PQ problems for LED lighting networks. The chapter also presented small-signal models of the proposed system. These models were used to understand the dynamic behavior and evaluate the stability of the TL-UPQC system. ATL-UPQC prototype was built to validate the ability of the proposed topology to achieve high power quality. Bode100 was used to verify the small-signal models and the overall system stability. The results showed good agreements between simulation, experimental results and theory.

Chapter 5 A Remotely Central Dimming System

5.1 Introduction

With the extensive use of LEDs for different indoor and outdoor lighting applications, a dimming function is required to regulate the output light intensity of the bulbs. Dimming comes with several advantages including energy saving, aesthetic pleasure, and increased productivity. Dimming can also expand the lifetime of an LED [119]. The reason is that the lifetime prediction of an LED lamp varies with temperature. Therefore, driving the LED at a lower current will extend its predicted lifetime. An LED dimming system, as shown in Figure 5-1, consists of an LED string, as the light source, an LED driver and a dimmer. The LED driver can be mounted externally or internally contained within in the household bulb.

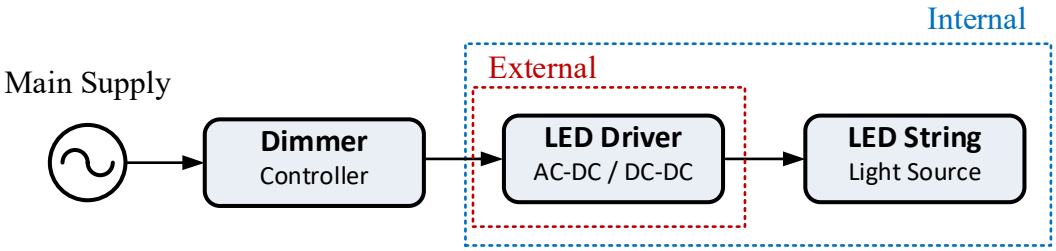


Figure 5-1. An LED dimming system.

A dimmer, sometimes referred to as a controller, is usually placed between the main supply and the LED driver. The LED driver can either sense the changes in the input voltage or receive

The work presented in this chapter has been published in the following paper: R. M. Abdalaal, C. N. M. Ho, C. K. Leung and H. S. Chung, "A remotely central dimming system for a large-scale LED lighting network providing high quality voltage and current," *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 5455-5465, Sept.-Oct. 2019.

an external dimming signal according to the dimming protocol implemented. Based on this information, the driver adjusts its forward current in response to its dimming operation. Utilizing different dimming protocols has brought concerns to their impact on the PQ of the network. Even though an LED bulb shows a good PQ parameters under rated operating point, its current harmonic distortion level under different dimming intensities might violate the standard values depicted by IEC61000-3-2 [104]. Several research work have been developed to improve LED drivers that provide precise dimming control [120], [121]. Dimming of a ballast driven lighting system to achieve high PQ has been proposed in [122], by connecting a reactive power device in series between the grid and the ballast. This method is appropriate for inductive high-intensity discharge (HID) lamps, and not compatible with LEDs.

In this chapter, The TL-UPQC has been proposed as a new remote-controlled dimming system for LED lighting networks. The system can provide the following dimming features,

1. One central dimmer can serve a large number of LED lamps.
2. No rewiring for existing lighting network and low-cost commercial dimmable LED lamps can be used.
3. Achieving high current and voltage quality with a wide range of LED dimming.
4. Remote control dimming and monitoring with capability to schedule a dimming profile.

The proposed dimming system is compatible with dimmable commercial LEDs. Non-dimmable LEDs in the market cannot be dimmed using this technique. The system employs connecting the TL-UPQC system, proposed in Chapter 4, between the grid and the lighting network as shown in Figure 5-2. In this chapter, the TL-UPQC system will be referred to as VSC dimmer system. In order to differentiate the proposed system and existing solutions, a review of

existing dimmer technologies, along with the pros and cons including phase cut, analog, digital, and wireless dimming protocol is presented first. Afterwards, the operation of the TL-UPQC system as a VSC dimmer system is discussed in detail.

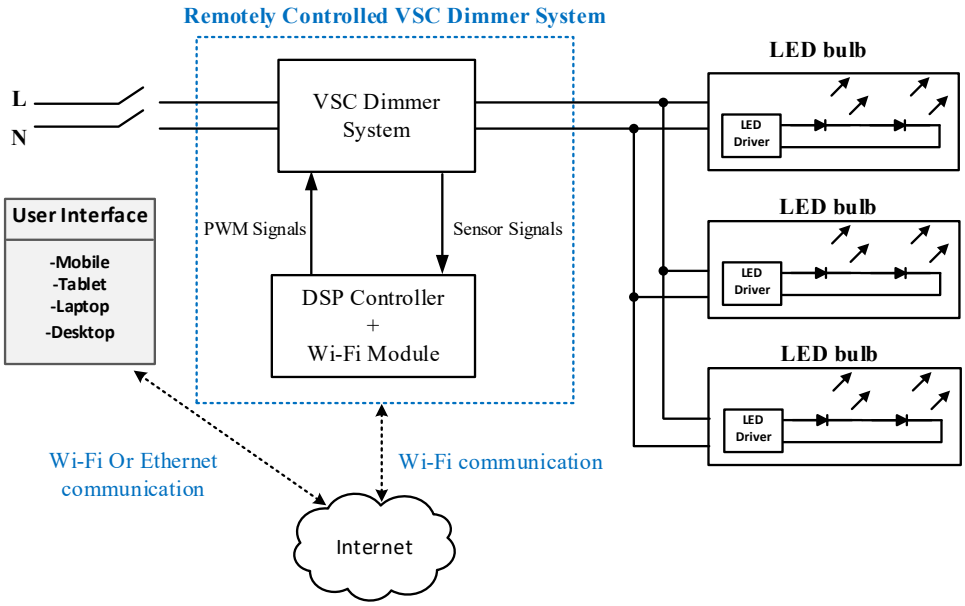


Figure 5-2. Proposed remote control VSC dimmer system.

5.2 State of Art of Dimming Technology

Existing work in the literature review and the market includes wired and wireless dimming systems. It should be noted that the dimmable LED driver must be compatible with the dimming method used.

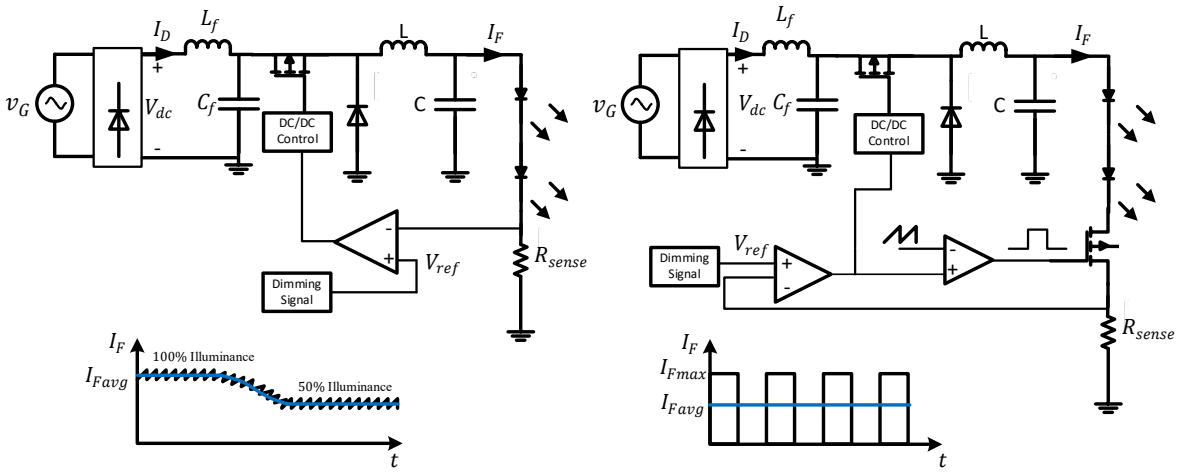
5.2.1 LED Driver Dimming Techniques

There are mainly two dimming techniques that are employed in an LED driver to achieve LEDs illuminance control: AM and PWM techniques. As the light intensity is proportional to the LED current flow [123], both techniques are controlling the average current going through the

LED string. In AM technique, also called continuous current reduction, dimming is achieved by controlling the magnitude of the forward dc current fed to the LED string as shown in Figure 5-3 (a). Lower LED current will result in a lower brightness while higher LED current will result in a higher light intensity. Under PWM technique, the diode string is turned on and off completely with a fixed frequency. During the on state, the LED current will reach its rated value as illustrated in Figure 5-3 (b). By varying the duty cycle d the average forward current will be changed. The output light intensity will be proportional to the duty cycle as,

$$I_{Favg} = I_F * d \tag{5. 1}$$

where, I_{Favg} is average forward diode current and I_F is maximum forward current of the LED string.



(a) (b)

Figure 5-3. Dimming techniques (a) AM (b) PWM.

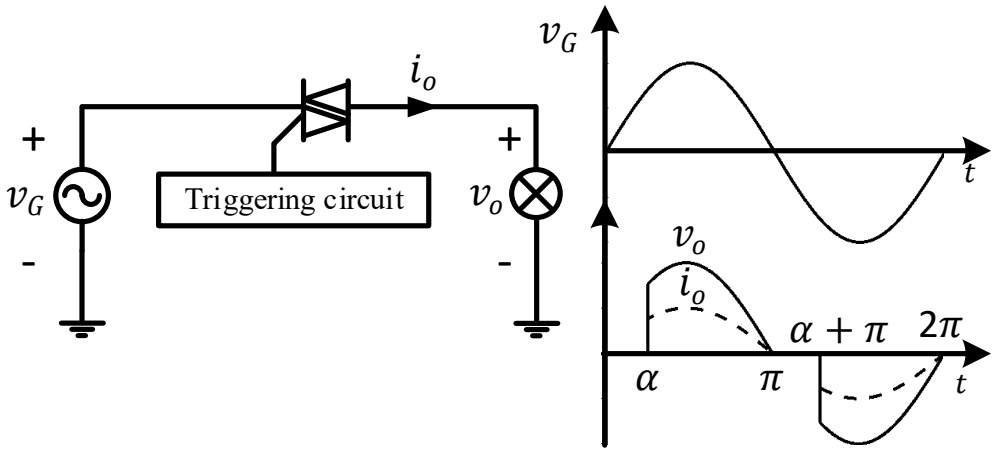
AM is simple to implement as it does not require additional electronic circuit connection. However, variation of LED current may cause color temperature change of the emitted light [124].

On the other hand, PWM technique drives the LED string at the rated forward current provided by the manufacturer, preventing color temperature change. PWM technique also provides good regulation at very low current levels. The frequency of the PWM should be high enough to avoid flickering. Fast transients of simultaneous switching of LEDs might cause EMI and potential noise could be generated [125], [126]. Hybrid AM/PWM dimming technique to combine the advantages of both techniques has also been proposed in the literature [127], [128].

5.2.2 TRIAC-Based Dimmers

Phase cut dimmers are widely used to dim LEDs. They are mostly adopted in LEDs with integrated LED drivers. They also can be used with compatible external LED drivers. Existing phase cut dimmer system includes a standard TRIAC-based dimmer with a triggering circuit, as shown in Figure 5-4 (a) that is used to control the firing angle of a TRIAC switch. By controlling the phase angle delay α, the ac voltage waveform is chopped; hence, the rms output voltage will be controlled. This technique has been firstly introduced to dim incandescent bulbs. The power sent to the bulb is controlled, which results in an adjustable light illuminance of the lamp. Nevertheless, for a desired dimming level the delay angle is not zero. Consequently, there will be a deviation of the input current from its sinusoidal shape. Typical waveforms of a TRIAC dimmer circuit for a resistive load is shown in Figure 5-4 (b). The compatibility of LED lamps with standard TRIAC-based light dimmers has brought many challenges due to their low power consumption. The low input current absorbed by an LED, which could be lower than the TRIAC holding current, results in a restricted dimming profile range. The LED lamp current has to be sufficient enough otherwise the user might experience light flickering. In order to overcome these challenges, a phase angle detection circuit and a passive, active or adaptive bleeder is utilized to

adjust the LED current and maintain the latching and holding current of the TRIAC dimmer [129]. An addition bleeder circuit will add cost and increase losses of the overall system.



(a) (b)

Figure 5-4. Standard TRIAC-dimmer lighting system.

Generally, employing a TRIAC dimmer is cost effective that requires no change to the existing wiring networks. However, it has poor PQ parameters. By chopping the input voltage to dim the LED lamp, the nonlinear behavior of the LED as a load will inject undesirable harmonics into the network. In contrast to an incandescent bulb, an LED bulb has an internal driver, which greatly differs across various manufactures and designs. By chopping the input voltage to dim the LED lamp, the input current drawn will be more distorted with higher harmonic contents. This nonlinear behavior of the LED as a load will inject more undesirable harmonic into the power system network. Moreover, under rated conditions with zero firing angle the TRIAC switch will always be conducting which will add to the conduction loss of the overall system even if no dimming is required. Another significance is that during startup, for a sudden change in the chopped input voltage, an inrush current will flow to charge up charge up the input E-Caps. The drawn current by an LED driver will have a second-order system characteristics as follows,

$$I_D = \frac{V_{dc}}{L_f C_f} \frac{sC_f + \frac{1}{R}}{s^2 + s\frac{1}{RC_f} + \frac{1}{L_f C_f}} \quad (5.2)$$

$$V_{dc} = \frac{\sqrt{2}V_G}{\pi} (\cos\alpha + 1) \quad (5.3)$$

where R represents equivalent resistance of an LED string, V_{dc} the average dc voltage after rectifying the ac signal, and V_G is rms value of the grid voltage.

A high inrush current will lead to temperature rise of the E-Caps and hence complete failure [130]. This inrush current might damage the LED or shorten its lifetime.

5.2.3 Protocols of Dimming Systems

Low voltage dimming signal defined in IEC 60929 (Annex E) [131], in which the dimming signal is separated from the main supply voltage. It is applied mainly with external LED drivers. The low voltage signal can be analog (0-10V dimming protocol) as shown in Figure 5-5 or digital addressable lighting interface (DALI) protocol as shown in Figure 5-6. The dimming system consists of a switch that controls the turning on and off the LEDs and a low voltage dimming circuit. Multiple drivers can be connected in parallel to the dimmer system. The communication is unidirectional in the analog system with no monitoring capability, while it is based on a bidirectional communication in the digital system. One DALI interface can connect up to 64 devices including luminaires, sensors and switches. It has a relatively yet acceptable low baud rate of 1.2 kbits per second (bps) [132]. The digital communication is done on a master-slave arrangement. Applying low voltage dimming protocol requires additional control wiring and proper LED driver controller that is compatible with the dimming protocol used. Low voltage dimming system provides central control in commercial and industrial buildings. It can be used

with new installations rather than replacing existing lighting system networks.

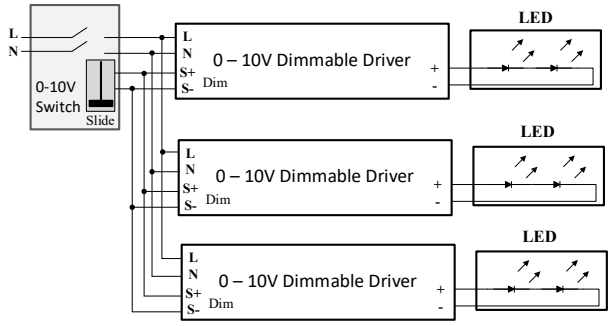


Figure 5-5. 0-10V dimmer system.

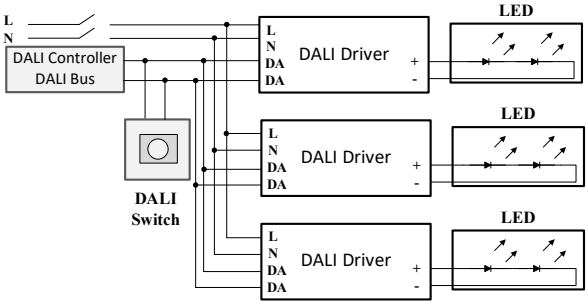


Figure 5-6. DALI dimmer system.

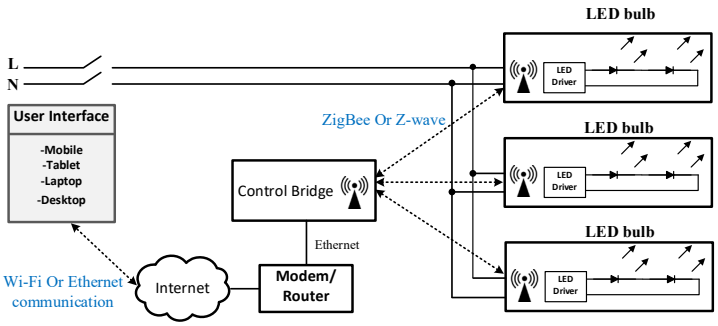


Figure 5-7. Wireless dimmer system.

Smart bulbs and internet of things are gaining a lot of interest in the lighting industry. ZigBee and Z-wave are the most leading protocols that allow the user to wirelessly control the on/off, dimming, color change of the lighting sources. ZigBee operates at 2.4 GHz ISM band with 250 kbps data rate [133]. Z-wave does not interfere with Wi-Fi as it operates in 906 MHz in North America and 868 MHz in Europe [134]. Z-wave typically transmits information at data rate of 40 kbps. Both ZigBee and Z-wave are low power wireless communication protocol. They both employ mesh network topology where each device can connect to other devices (nodes) and find the nearest available path in the network within its range. A gateway node is needed to serve as a bridge between the mesh network and TCP/IP network as shown in Figure 5-7. In contrast, Wi-Fi

communication protocol [135], does not need a gateway for internet connectivity. The downsides of Wi-Fi technology is the high power consumption and high cost compared to other low power wireless protocols. Wi-Fi is based on a star network topology in which each node of the network is connected to the central node. A wireless control system based on ZigBee protocol has been proposed in [136]. The study has been conducted on a street lighting application with traffic based dimming strategy. The main drawback utilizing wireless smart dimming is that each LED driver has to support the wireless dimming protocol employed, e.g. Bluetooth, ZigBee, Zwave and Wi-Fi. This adds complexity to LED drivers and increases the cost of the network, especially for large penetrations of LEDs in streetlight or parking lot applications.

5.3 Proposed Remote Control Dimming System

The proposed system shown in Figure 5-2 represents a remote central dimming system for a large-scale LED lighting network. The system can attain continuous dimming for LED lamps while improving the PF and reducing the current harmonics that are generated by the internal driver, as discussed in Chapter 3 subsection 3.2.2, in commercial dimmable LEDs. The remote management system allows scheduling a continuous dimming profile for existing lighting systems, which will endorse energy saving. This can be accomplished by setting a profile to dim the LEDs according to the ambient daylight or productivity requirement. Figure 5-8 shows an example of a dimming profile for road lighting systems. For instance, the dimming level can be set to a high level in evening and early morning rush hours at which full energy is acquired. Conversely, the dimming level can be set to decrease gradually during sunrise and to be zero during daylight. Furthermore, energy saving can be achieved during mid-night by setting the dimming level to 80% brightness.

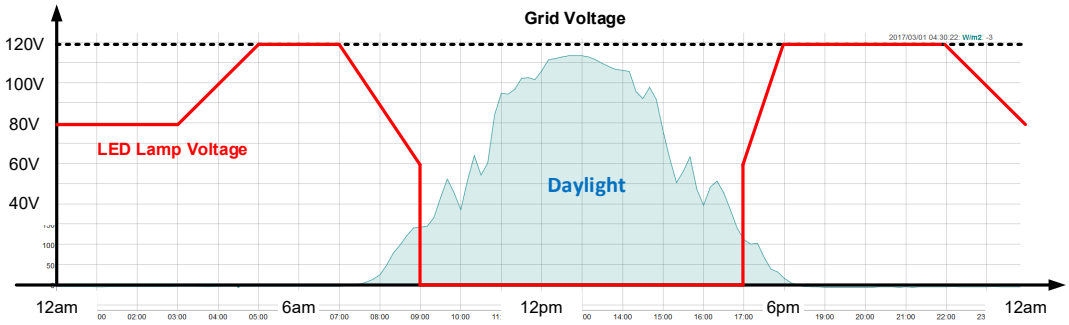


Figure 5-8. Example of dimming profile for street lighting system.

The proposed system consists of three main parts: a VSC dimmer (which corresponds to the TL-UPQC), a controller with a Wi-Fi module and a control center. The VSC dimmer controls the magnitude of the output voltage delivered to the LED lamps with a sinusoidal voltage. This will eliminate the inrush current drawn by the filter capacitor. By varying the output voltage magnitude, the LED driver will receive a new desired dimming level and change the output light intensity accordingly. The VSC dimmer controls the input current as well to achieve high PQ parameters at the input side. The controller receives the sensor signals and sends the PWM signals based on the desired reference signal. To build a remote management system, a Wi-Fi module is used to allow communication between the VSC dimmer, the controller, and the control center unit through internet. A desktop/webpage application running on a control center will be the interface between the operator and the VSC dimmer. The operator will send a command with a desired power to dim the LED lighting system. This information will be received by the Wi-Fi module, which will set the new operating point to the controller. The controller then will take the right action and send corresponding PWM signals to the VSC dimmer. The operator will be able to receive feedback information from the system for monitoring purpose. Two feedback signals are sent: measured power in watts and LUX values.

5.3.1 Principle of Operation

The VSC dimmer topology is based on the TL-UPQC topology depicted in Figure 4-2 in Chapter 4. The system control block diagram will be the same. To achieve dimming, the reference output voltage will be provided externally as indicated in Figure 5-9.

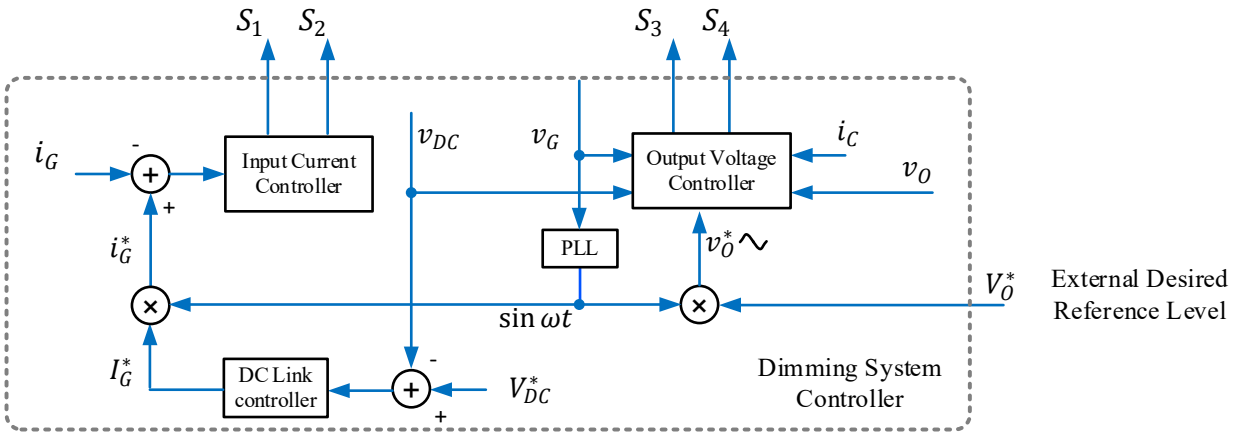


Figure 5-9. Modified TL-UPQC control strategy for the addition of dimming function.

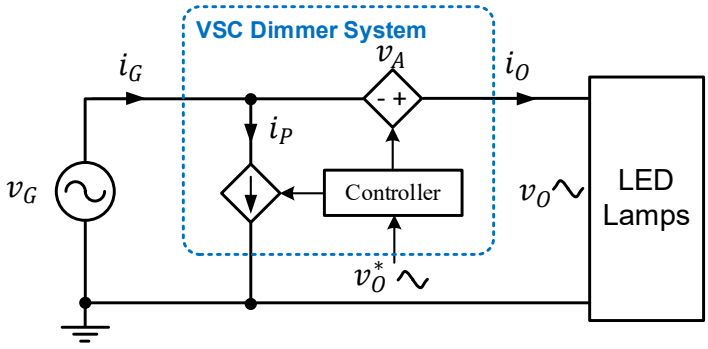


Figure 5-10. Equivalent circuit of VSC dimmer system.

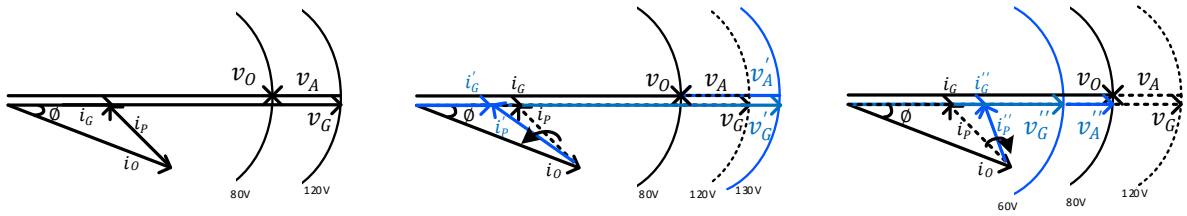
To illustrate how the system provides dimming, Figure 5-10 indicates the equivalent circuit of the system. As discussed in Chapter 4, the series converter can be modeled as a voltage-controlled voltage source. The apparatus achieves dimming by controlling the voltage applied to the lamps through the series voltage source. The dimmer operates as a controllable voltage source

v_A that is connected between the grid and the load voltage v_O. Since the voltage applied across the LEDs has a direct relationship with its output light intensity, as illustrated in Chapter 3, the reference voltage that corresponds to a specific dimming level can be obtained. By varying the series voltage, a smaller voltage than the grid will be applied across the LEDs. This can be achieved using the following formula,

$$v_A^*(t) = v_o^*(t) - v_G(t) \tag{5. 4}$$

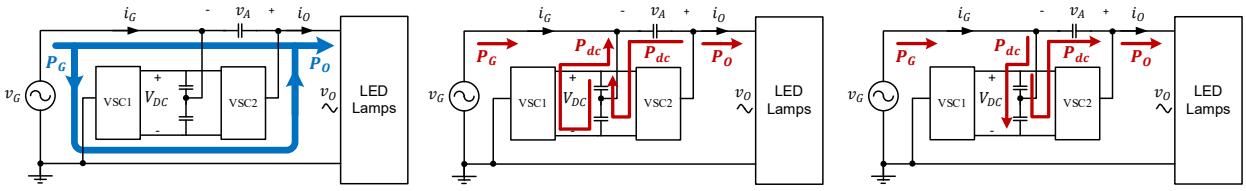
where $v_A^*(t)$ is reference voltage-controlled voltage source, and $v_o^*(t)$ is the desired voltage applied to LED lamps.

Figure 5-11 (a) shows the phasor diagrams under one dimming level. At steady-state, the series voltage v_A is in out of phase of v_G delivering a smaller magnitude across the LEDs. The dc link voltage is regulated at a pre-set voltage level V_{DC}^*. By creating a power branch, the dimmer compensates and regulates the power delivery from the source to the load. The parallel converter will restore the power absorbed/delivered by the series converter as shown in Figure 5-12 (a). Furthermore, the system is able to compensate a voltage sag/swell while maintaining the desired dimming level constant. In a voltage swell v_G', the series voltage will increase v_A' maintaining v_O constant as illustrated in the phasor diagram in Figure 5-11 (b). The parallel current i_P' will change accordingly to meet the new operating point after a change in i_G'. As the power delivered to the LEDs is maintained constant, the end user will experience no change in the output light intensity. During transient, the excess power will be absorbed by the dc link capacitor as shown in Figure 5-12 (b). On the contrary, in a voltage sag v_A'' will be in phase with v_G'' as shown in Figure 5-11 (c). The active power demand is supplied by the dc link capacitor during transient as depicted in Figure 5-12 (c). The dc link capacitor will charge back up to steady-state through the parallel VSC.



(a) (b) (c)

Figure 5-11. Phasor diagrams of VSC dimmer system under a dimming level (a) steady-state (b) voltage swell (c) voltage sag.



(a) (b) (c)

Figure 5-12. Power flow under a dimming level (a) steady-state (b) voltage swell (c) voltage sag.

5.3.2 Remote System and Devices

A. Data Acquisition and Communication

The system is a bidirectional communication between the VSC dimmer and the control center unit. Data acquisition is done through the sensors and sampled with an analogue to digital (ADC) converter in a DSP. Figure 5-13 shows the detailed system architecture between the VSC dimmer system, DSP, Wi-Fi module, and the control center. Voltage sensors are for input voltage, output voltage that is applied across the lighting network, dc capacitor voltage, and current sensors are for input current and filter capacitor current i_C. The developed boundary control algorithm, presented in Chapter 4, will define the switching actions according to the instantaneous sensed signals. At

the same time, data transfer is taking place between the DSP and the Wi-Fi module through serial or parallel communication. Universal asynchronous receiver/transmitter (UART), serial peripheral interface (SPI), or general-purpose input/output (GPIO) can be used for interface. The Wi-Fi module is responsible to sending/receiving the data to/from the server. The control center that represents the remote management system will receive/send the data from/to the server.

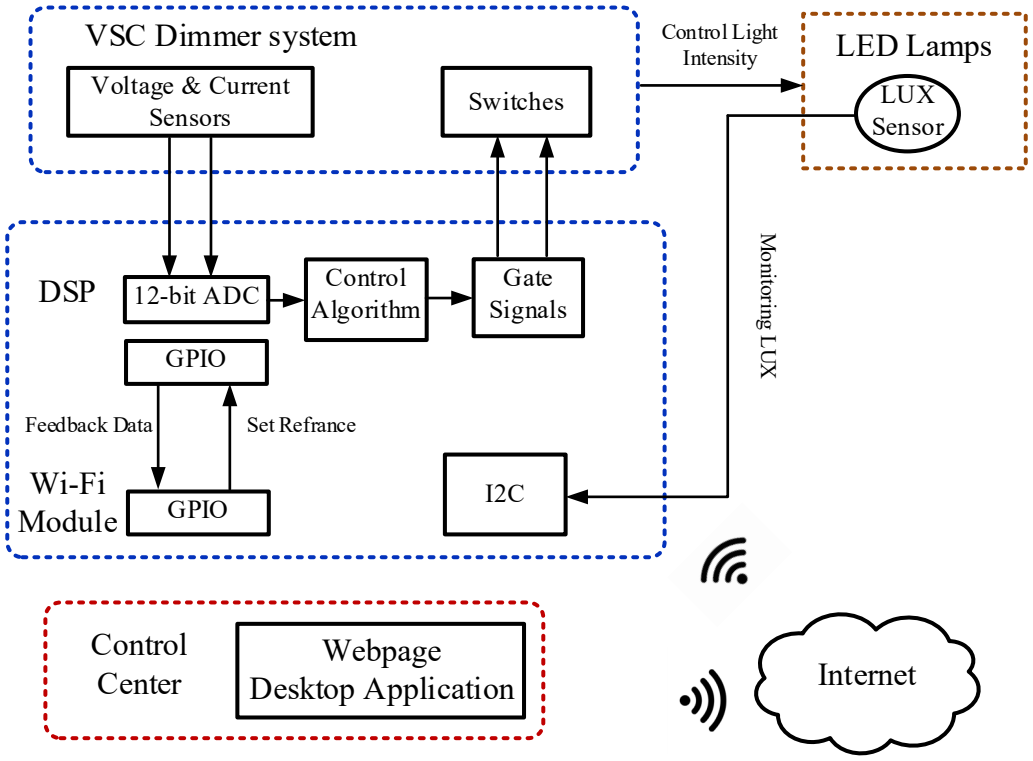


Figure 5-13. System architecture of communication and interface.

B. User Interface Implementation

Graphical User Interface (GUI) is designed to allow the user to send commands and receive feedback information through a webpage or a desktop application. The user can send a request through the webpage browser. HyperText Transfer Protocol (HTTP) is used a communication

protocol between the client and the host server. The Wi-Fi module runs a program (written in Python programming language), which reads and writes data to the server. The user will set a desired reference value through the web browser. This external dimming signal will be sent to the VSC dimmer system. The Wi-Fi module will request this information and get a response from the web server. A command will be sent from the Wi-Fi module to the DSP to change the reference signal. For monitoring the system performance, the sensed signals at the load side are used to calculate the average power delivered. The server will request to display this information on the GUI. MATLAB software is used for the purpose of implementing a desktop application. The application running on the control center will communicate with the Wi-Fi module through Secure Shell (SSH) connection. The user will set a desired power level using the desktop application. As a response, the controller will take a proper control action according to the received new desired reference signal. The desktop application will always allow remote controlling to the dimmer system even if the internet connection is down through the LAN network, which will increase the overall system reliability. In addition, the operator will be able to monitor real-time light intensity values. This is achieved by placing a LUX meter at the lighting network side. The Wi-Fi module will receive the lux value through I2C pins or wirelessly using Zigbee.

5.4 System Modelling and Characterization

5.4.1 Stability of Control system

As discussed in the previous section, the series converter is responsible for delivering a smaller voltage across the LED lamps than the applied main supply voltage. The system receives the reference from an external signal that is originated by the end user. This signal represents a

desired dimming level. As the data will be transmitted over the internet, a network latency is introduced. Consequently, a system delay is introduced in the control loop. The network latency is the time it takes for a data to travel from one point to another over the network. The small-signal model of the series converter considering network delay is shown in Figure 5-14. The transfer function of the communication delay, represented by $T_{comm}(s)$, will not affect the stability of the system as it will be much slower than the voltage control loop. The bandwidth of the DVR voltage loop has been designed to 6.35 kHz as presented in Chapter 4 subsection 4.4.2. This indicates that the reference update will be much slower than the controller dynamics. Therefore, it will not influence the performance of the overall system. The communication delay transfer function is expressed by,

$$T_{comm}(S) = \frac{\tilde{v}_O^*(s)}{\tilde{v}_{OR}^*(s)} = T_D(s).T_{ZOH} = e^{-sT_d}.\frac{(1-e^{-sT_z})}{T_z s} \quad (5.5)$$

where T_d is the signal transmission delay and T_z is the zero order hold (ZOH) step time delay [138].

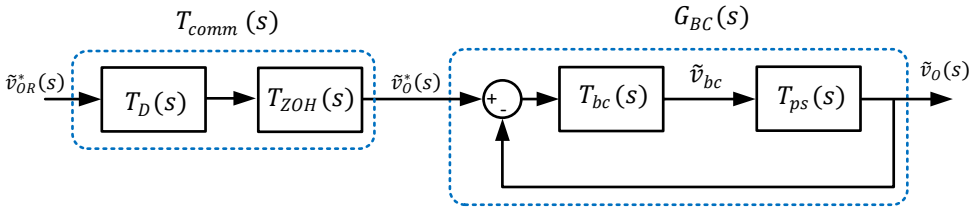


Figure 5-14. Small-signal model the VSC dimmer system control scheme.

5.4.2 System Loss Estimations

Loss breakdown of the system has been estimated for system design optimization. The semiconductor devices and the filter inductors cause the main losses in the converter. In this study,

the trench field stop insulated-gate bipolar transistors (IGBT) have been selected due to their high performance and low conduction and switching losses. Semiconductor losses are estimated according to [137], in which the losses are determined using the electrical characteristics specified in the datasheet for the corresponding operating point. The magnetic material used to form the inductor is the Metglas C-Core AMCC. The inductor core loss is calculated based on "Steinmetz" equation as follows,

$$P_{croe} = 6.5.f^{1.51}.B_{ac}^{1.74}.wt \quad (5.\ 6)$$

where f is the switching frequency in kHz, B_{ac} is the ac flux and wt is the weight of the core [139]. Figure 5-15 shows the estimated loss in the 500VA/120V dimmer system prototype. For a light load (e.g. small number of connected LEDs) the efficiency of the system is low, this is because the switching losses are dominant at low power levels. The conduction losses are increasing as the number of connected LEDs to the system increases. Figure 5-16 shows that the efficiency will increase when a larger scale of lighting network is supplied.

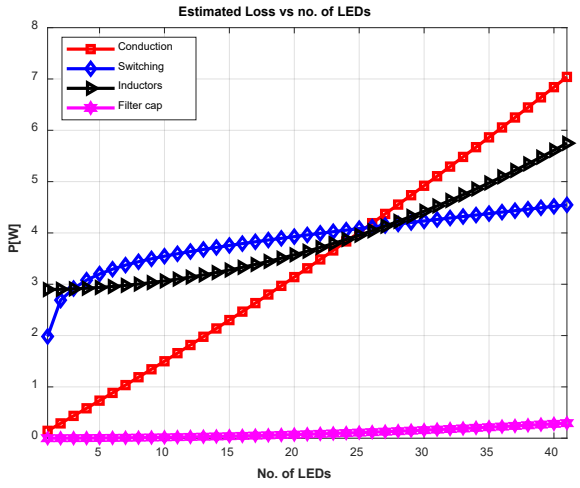


Figure 5-15. Estimated loss in 500VA, 120V VSC dimmer system.

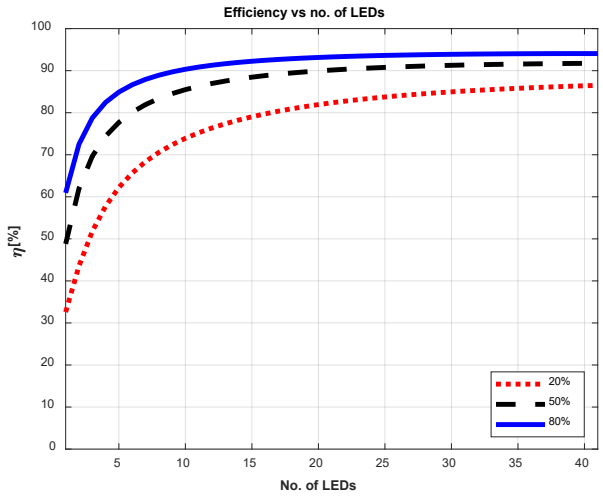


Figure 5-16. Estimated Efficiency of the VSC dimmer system under various dimming levels, 20%, 50% and 80% of rated illuminance.

5.5 Experimental Verifications

5.5.1 Implementation of Testbed

The TL-UPQC 500VA/120V prototype has been evaluated as a VSC dimmer system to verify the proposed dimming system. A Wi-Fi module has been attached to the system to enable internet access to the system as shown in Figure 5-17. The LEDs, described in Chapter 3 section 3.4, have been tested under the proposed dimming system. The power analyzer is used to measure PQ parameters including PF, total harmonic distortion of output voltage (THD_{V_O}), total harmonic distortion of input current (THD_i), and efficiency (η).

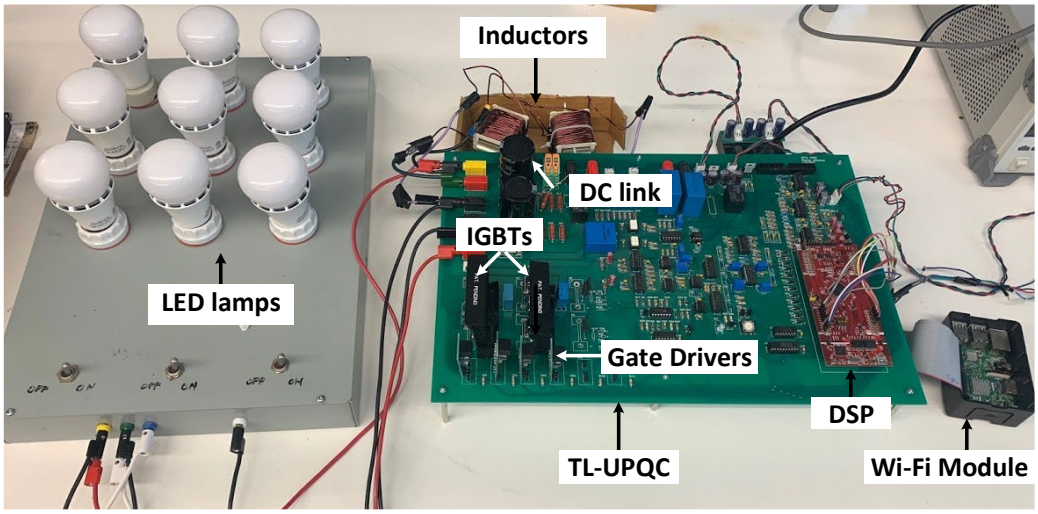
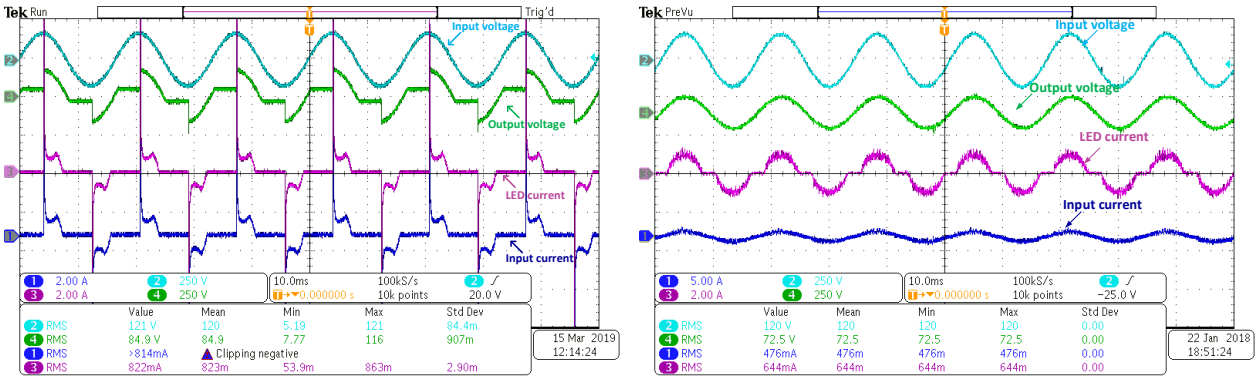


Figure 5-17. Testbed setup.

5.5.2 Evaluation of Dimming Performance

In order to benchmark the performance, a standard TRIAC-based dimmer is used to provide dimming function for LED lamps. The results in Figure 5-18 (a) show the waveforms of the input

voltage, output voltage across LEDs, LED current and input current drawn at 50% light intensity. There's an inrush current when the TRIAC turns on to charge up the filter capacitor as discussed in eq. (5.2). The inrush current is found to be 10 times the magnitude of the LED rated current. This inrush current might shorten the lifetime of the LEDs and decreasing its luminous efficacy. Conversely, the VSC dimmer system has been utilized to provide dimming to the LEDs under test. Figure 5-18 (b) shows the waveforms at 72 V RMS reference output voltage, which corresponds to 50% light intensity. The results show high quality waveforms for input current and output voltage as well as LED current.



(a) (b)

Figure 5-18. Waveforms at 50% illuminance with (a) TRIAC-based dimmer (b) VSC dimmer system.

5.5.3 Static Power Quality Evaluations

Power analysis measurements are shown in Figure 5-19 to study the effect of different dimming levels on PQ parameters, including THD_i, THD_{v_o} (lamp voltage), PF, η, output/input power and input VA, utilizing TRIAC and VSC dimmers. The TRIAC dimmer failed to achieve 100% illuminance due to the very small firing angle for conducting all the time even though no dimming requirement ($\alpha \cong 0$). The graphs show that, with using TRIAC dimmer higher harmonic

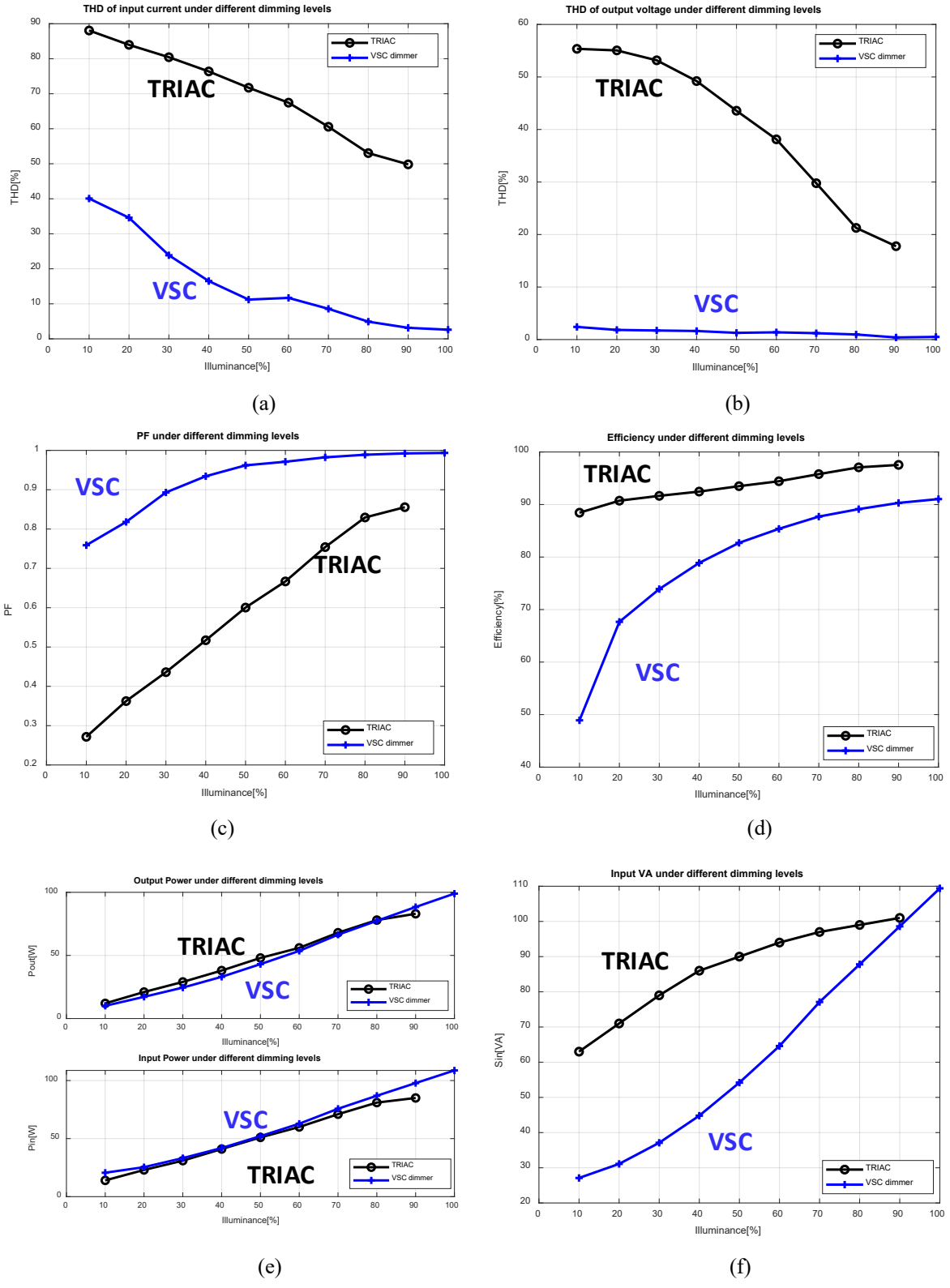


Figure 5-19. Power quality measurements comparison (a) THD of input current (b) THD of lamp voltage (c) PF (d) efficiency (e) output/input power (f) input VA.

contents as well as lower PF are experienced when the lamps are dimmed. This is due to the higher delay angle at lower dimming levels. On the contrary, the VSC dimmer shows a better performance in terms of PQ parameters. Regardless of, the TRIAC dimmer has a high efficiency as in Figure 5-19 (d); the output power drawn to achieve the same level of illuminance in LUX using a TRIAC dimmer is higher compared to that using the VSC dimmer system as shown in Figure 5-19 (e). The reason is that the inrush current that will go into an LED, while using the TRIAC dimmer, will lead to an increase in the LED junction temperature. Higher LED junction temperature will lead to a lower luminous efficacy meaning lower lm/W [140]. Therefore, the input power drawn for both dimmer systems are quite similar. In addition, the input VA is much lower using the VSC dimmer due to its high PF in Figure 5-19 (f). Thus, the VSC dimmer has an overall better performance compared to the traditional dimmer. It is also important to mention that there are 9 LEDs under this test according to the laboratory scale setup. This justifies the low measured efficiency at light load. Especially at 10% illuminance that corresponds to only 4% of the system full rating. This has been estimated and justified in 5.4. The efficiency of the system can increase significantly when it is fully utilized or with the use of recent development of power semiconductor - wideband gap semiconductor devices.

5.5.4 Voltage Sag and Voltage Swell

If a voltage sag/swell occurs in the network, the driver of a dimmable LED identifies it as a request of changing its light intensity. Therefore, the end user will observe visible flickering for the period of the sag/swell. The VSC dimmer system is able to compensate a voltage sag or swell in the network. A test has been conducted at 70% dimming level, in which the voltage across the LEDs has been controlled at 87 V rms. A voltage swell and then a voltage sag, 110% and 75% of

the nominal grid voltage, respectively, have been applied to the main supply. The VSC dimmer system was able to maintain the output voltage constant in both transient conditions as shown in Figure 5-20. Therefore, the power delivered to the LEDs has been maintained constant as well.

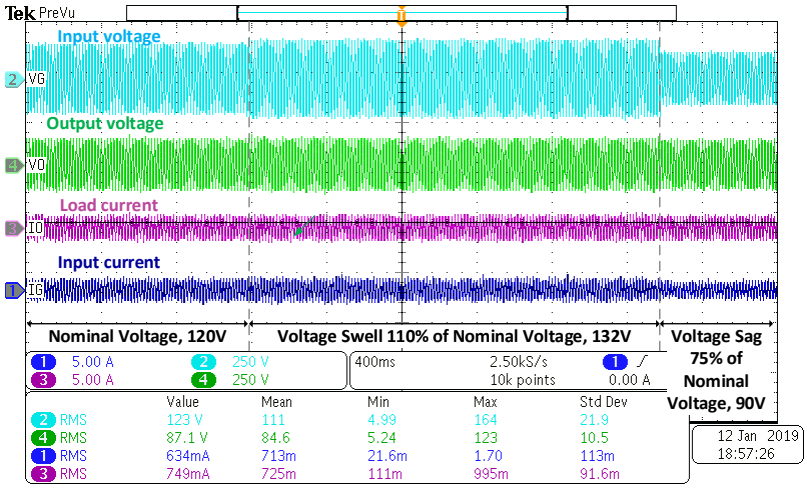


Figure 5-20. 70% dimming level under voltage sag and voltage swell.

5.5.5 Interactive GUI and Network Latency

Figure 5-21, Figure 5-22 and Figure 5-23 Show the webpage and desktop control panel of the remote dimmer system. The GUI allows the user to set a dimming level either manually through a slider or automatically by setting a schedule to create a dimming profile for the day. It can be accessible anywhere using a laptop or a cell phone. A snapshot of the webpage is shown in Figure 5-21. The schedule event is set to change the power level from 100% rated power to 50%, then 30%, 80% back to 100%. For the test purpose, each power level lasts for 30 seconds. The results show that the feedback power signal matches with the reference signal. The GUI allows the user to choose displaying the power level feedback signal or the measured light intensity feedback signal. TSL25661 luminosity sensor is used to measure the light intensity of LED lamps. The LUX sensor is placed on top of the light bulbs as illustrated in Chapter 3 section 3.4.

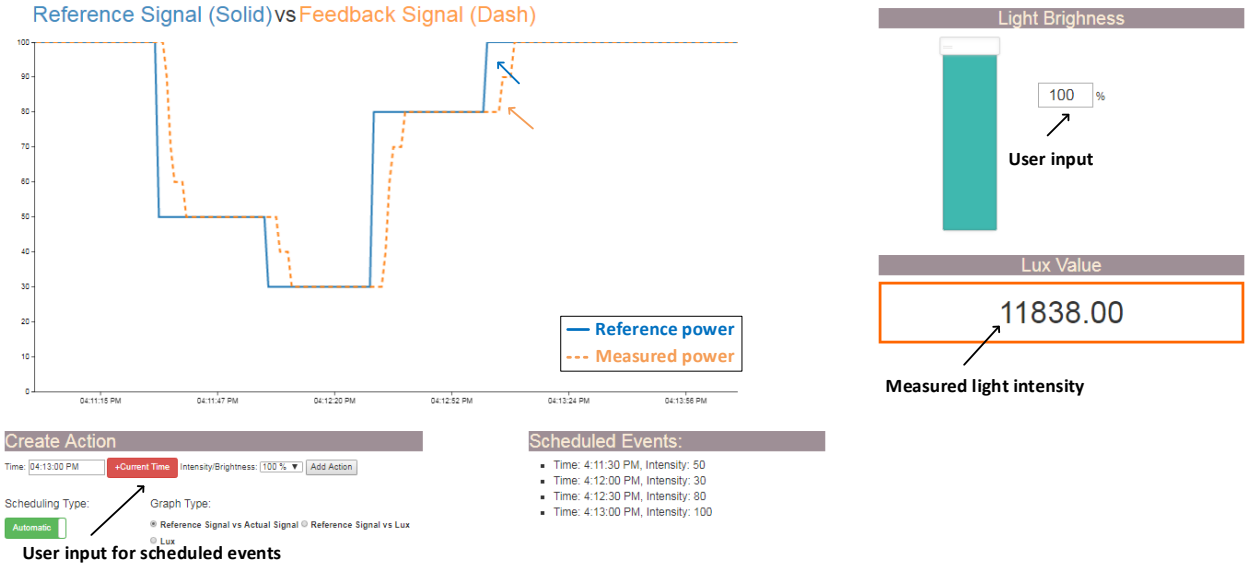


Figure 5-21. Webpage GUI for dimming lighting systems.

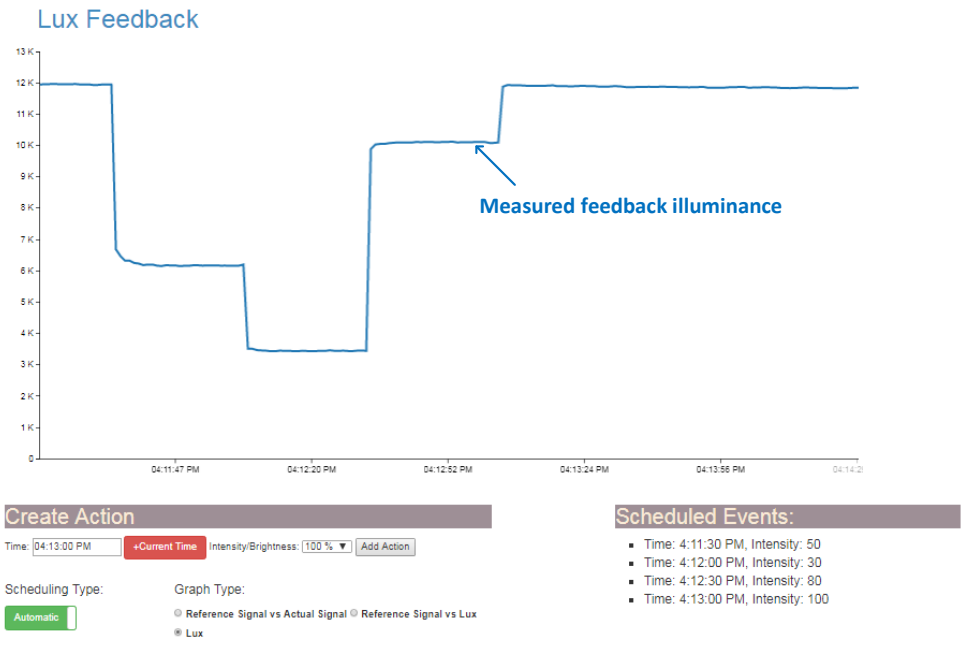


Figure 5-22. Webpage Light intensity feedback signal.

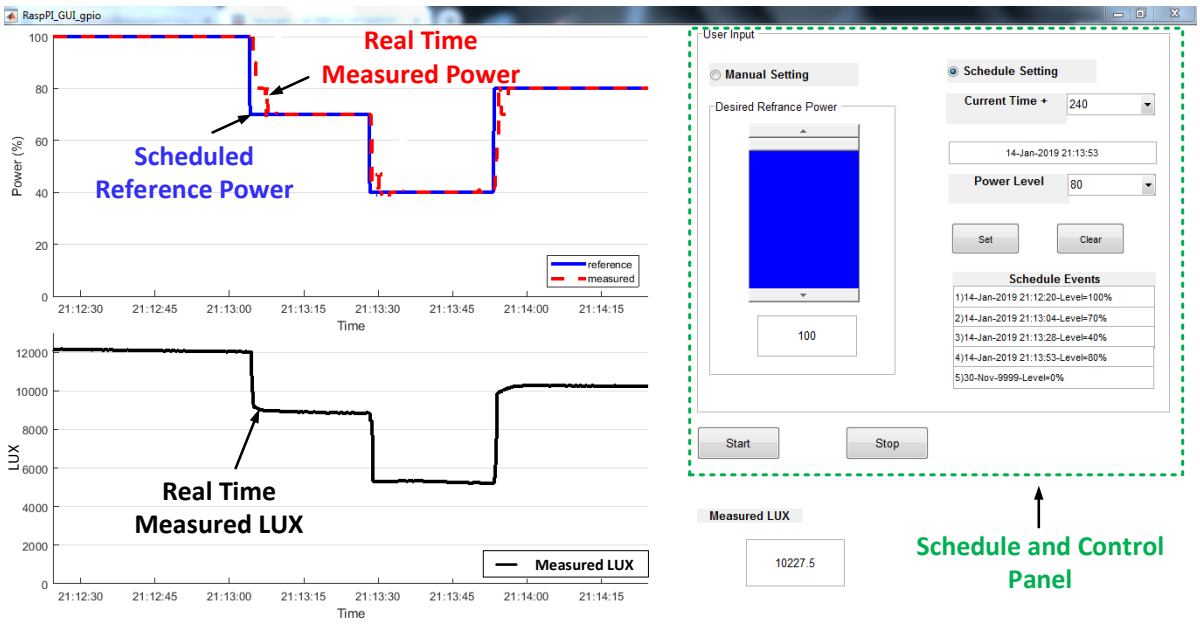


Figure 5-23. Desktop application for dimming lighting systems.

Figure 5-22 shows the lux feedback values for the conducted test at different dimming levels. The desktop application snapshot is shown in Figure 5-23. The schedule event for the conducted test is to change the power level from 100% rated power to 70%, 40% then 80%. The results show that the real-time measured power and light intensity are following the change in the power level. The GUI displays the measured light intensity feedback signal using TSL25661 luminosity sensor. The data transferring through the network can definitely introduce delay and inconsistency in time. The total network latency has been characterized running a MATLAB program. First, The MATLAB program initiates communication with the Wi-Fi module to send data and commands through the network before actual execution takes place. Likewise, when transferring back data from the Wi-Fi module to MATLAB program. Table 5-I gives the average travel time of the message in the network under the performed test conditions.

TABLE 5-I COMMUNICATION PARAMETERS

Parameter	Value
T_{d}	5 ms
T_{z}	10 ms
I2C	9600 bps

5.6 Chapter Conclusion

A central remote-control dimming technique for commercial dimmable LED lamps has been proposed. The proposed system does not require rewiring the existing lighting network while providing remote dimming control function with high PQ features. The technique is based on adding a VSC dimmer system between the main supply and the LEDs. The experimental results proved that the VSC dimmer system achieved high PQ parameters compared to conventional diming techniques. Moreover, the system was able to compensate for voltage variations in the network resulting in a flickering free lighting network. The operator at the control center can control dimming through a webpage or a desktop application. The system employs a bidirectional communication between the VSC dimmer system and the control center. No specific additional controller for the LED driver is required. The results showed good agreements with the theoretical concept. This technique is promising for street lighting or commercial lighting systems that require large penetration of LEDs with central dimming and monitoring.

Chapter 6 Enhanced Control Methodology for Input Grid Voltage Regulation

6.1 Introduction

High penetration of small-scale DER is now connected to LV distribution ac networks. For example, a PV system offers a reliable and a clean source of energy that becomes a popular choice to meet the increasing load demand. Large-scale wind power plants are widely adopted in electric power transmission and small-scale wind farms are integrated with ac microgrids. Even though renewable energy sources are the proper replacement to conventional power plants to increase the power generation level while reducing greenhouse gas emissions, their intermittent nature conveys many challenges to the utility grid. A sudden voltage rise might occur due to reverse power flow at peak PV generation with low load connected to the network [141]. Partial shading also results into a fluctuating power that is reflected on the grid as a fluctuating voltage [142]. Therefore, setting limits for PV penetration at LV distribution network has been a vital argument. The stochastic nature of wind active and reactive power results into PQ problems by exceeding voltage flickering levels [143], [144]. Moreover, a voltage drop might result due to a sudden load increase in a hybrid/ac microgrid (e.g. Electric vehicles charging at the same time). On the contrary, light loads might lead to a voltage rise. Voltage variation in the network is a critical PQ issue that causes systems shutdown, loss of data, high losses, overheating of equipment and reduced lifetime. The larger the voltage variation, the more likelihood of components failure.

Research done to improve the stability of the grid voltage has been reviewed in Chapter 2 section 2.3. The work in this chapter proposes an enhanced control strategy to extend the advantages of the TL-UPQC system presented in Chapter 4 and Chapter 5. The system will include

enhancing the PCC voltage quality and eventually support the upstream voltage. The enhanced control methodology offers the functions of a STATCOM and a UPQC system with a single converter. The TL-UPQC system would continue to mitigate major PQ issues at the load side in addition to provide input grid voltage support. This methodology copes with the new distributed nature of a microgrid grid rather than the centralized power network that mitigates PQ issues elevated at LV distribution networks.

6.2 System Description and Operation

Figure 6-1 shows the construction of the single-phase TL-UPQC coupled to the PCC at a LV distribution network. The TL-UPQC topology is the same as the one described in Chapter 4. A shunt filter capacitor C_P is added to the system to act as a low impedance for the high frequency components introduced by the converter. This will minimize the switching harmonics injected by the shunt converter into the grid.

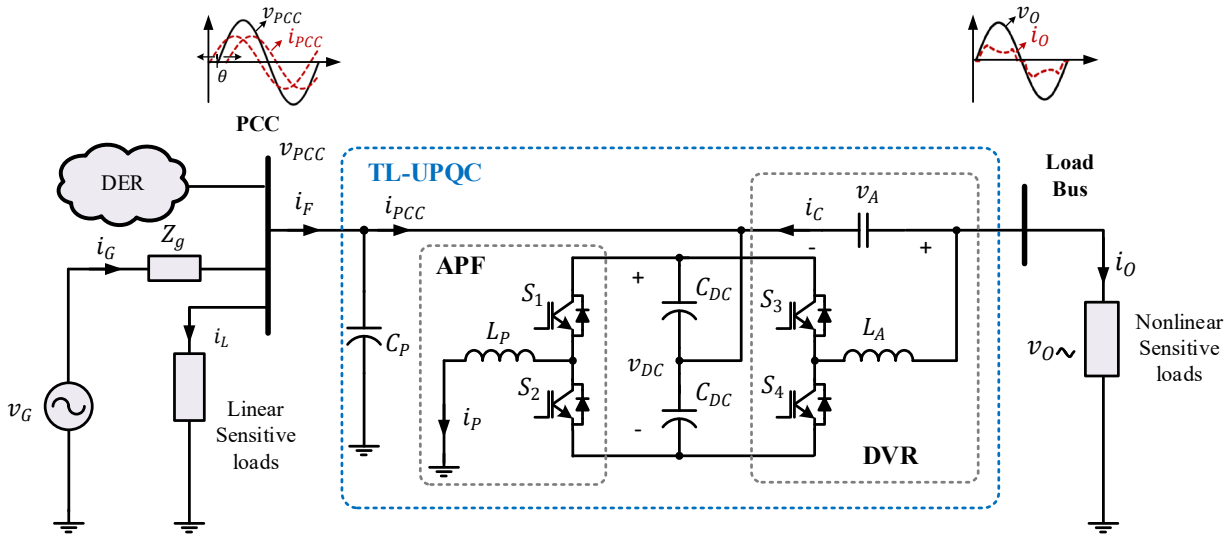


Figure 6-1. TL-UPQC topology for voltage regulation in LV Distribution Network.

While TL-UPQC is intended to be installed at LV distribution network, it can be fully utilized without the need of installing more STATCOMs, the control strategy of the TL-UPQC system is extended to include the following advantages,

1. Provides reactive power compensation to achieve voltage regulation to the loads connected to the PCC.
2. Improves voltage quality at the PCC that is affected by the interaction between voltage and current harmonics.
3. Relies on means of collected local information and does not require additional sensors.

In order to understand the operation of the enhanced TL-UPQC system, the waveforms of the input voltage, input current, output voltage and output current are illustrated in Figure 6-1. In a typical TL-UPQC system, the APF injects current harmonics and reactive current i_P to compensate the distorted current of the nonlinear load i_O. This will shape the input current i_{PCC} to be sinusoidal and in-phase with the PCC voltage. The grid current $i_G(t)$ will carry the apparent power demand of the PCC load that is quantified by the PCC load current $i_L(t)$. It will also carry the active power demand consumed by the load connected to the load bus in addition to the necessary active power required to maintain the dc link voltage and compensate for converter losses.

The grid voltage and the PCC voltages can be expressed as,

$$v_G(t) = \sqrt{2}\, V_G \sin \omega t \tag{6. 1}$$

$$v_{PCC}(t) = \sqrt{2}\, V_{PCC} \sin(\omega t - \delta) \tag{6. 2}$$

where ω is the angular grid frequency and δ is the displacement angle of the PCC voltage. V_G and V_{PCC} are the steady-state rms values of grid and PCC voltages respectively.

At the event of heavy load changes, or the event of a sudden power change in a DER, there will be an over/under voltage at the PCC voltage. In the enhanced control methodology, a phase angle θ is created between v_{PCC} & i_{PCC} as depicted in Figure 6-1. If reactive power compensation is needed at the grid side, the phase θ is controlled according to the measured PCC voltage v_{PCC}. The active and reactive power at the PCC can be expressed as follows,

$$P_{PCC} = V_{PCC} I_{PCC} \cos\theta \;\; \& \; Q_{PCC} = V_{PCC} I_{PCC} \sin\theta \tag{6. 3}$$

where I_{PCC} is the steady-state rms value of the feeder current, while θ is the PCC current displacement angle with respect to the PCC voltage.

By controlling the phase angle θ, the TL-UPQC will be able to perform in three reactive power compensation modes. The phasor diagram shown in Figure 6-2 illustrates the operation of the three modes: a) power factor correction (PFC) mode in which no reactive power compensation is needed at the grid side, b) capacitive mode in which reactive power is being injected to the grid and c) inductive mode in which reactive power is being absorbed from the grid. I'_{PCC}, I'_G and V'_{PCC} represent the steady-state values without grid reactive power compensation. It can be noted that the PCC voltage is lagging the grid since the active power is transferred from the grid to the system.

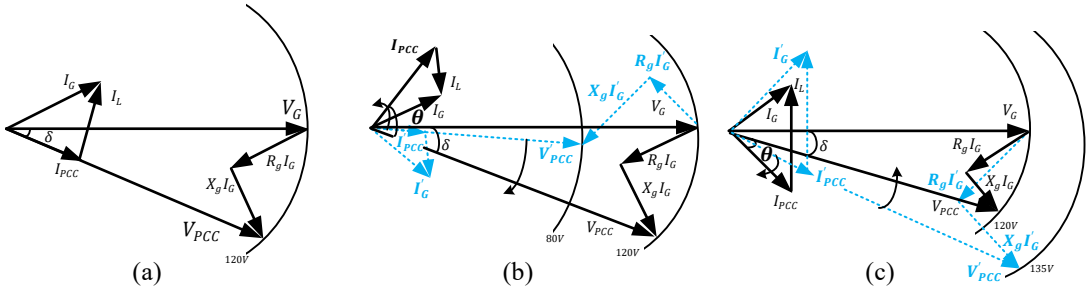


Figure 6-2. Phasor diagrams of (a) PFC mode (b) capacitive mode (c) inductive mode.

6.2.1 Power Flow Analysis

Figure 6-3 shows a block diagram of the power flow in a TL-UPQC system. The amount of grid active and reactive power transferred from the grid to the PCC bus can be expressed by,

$$P_G = \frac{V_G V_{PCC}}{Z_g}\cos(-\delta + \emptyset_g) - \frac{V_{PCC}^2}{Z_g}\cos(\emptyset_g) \quad (6.4)$$

$$Q_G = \frac{V_G V_{PCC}}{Z_g}\sin(-\delta + \emptyset_g) - \frac{V_{PCC}^2}{Z_g}\sin(\emptyset_g) \quad (6.5)$$

where Z_g represents the grid impedance with a displacement angle of $\emptyset_g$.

A linear load represents the load connected to the PCC. The load active and reactive power are given as follows,

$$P_L = \frac{V_{PCC}^2}{Z_L}\cos(\emptyset_L) \;\; \& \;\; Q_L = \frac{V_{PCC}^2}{Z_L}\sin(\emptyset_L) \quad (6.6)$$

where Z_L is the load impedance connected to the PCC with a displacement angle of $\emptyset_L$.

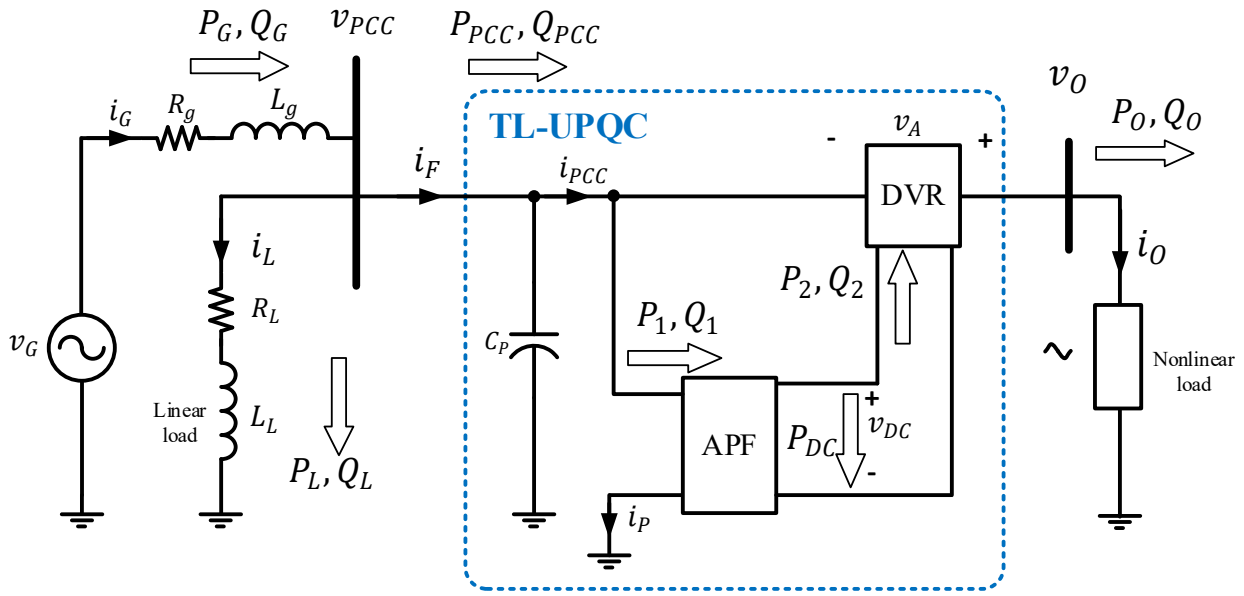


Figure 6-3. A block diagram of power flow in a TL-UPQC system.

A nonlinear load is connected to the TL-UPQC system. In this study, the nonlinear load is chosen to be dimmable LED lamps, due to their extreme sensitivity to voltage flickering and their nonlinear characteristics. Since the TL-UPQC system will compensate for the load harmonics, the LED lamps is assumed to be seen as a resistive load from the grid point of view. The amount of active power consumed by this critical load is given by,

$$P_O = \frac{V_O^2}{R_O} \tag{6. 7}$$

where, R_O is the equivalent fictitious resistance of the LEDs and V_O is the output rms voltage maintained by the TL-UPQC system across the load bus.

At the PCC, the relation between the active powers is governed by,

$$P_G(t) = P_{PCC}(t) + P_L(t) \tag{6. 8}$$

The power going through the shunt converter P_1 , assuming no losses in the converter, is used to charge up the dc link capacitor and maintain the dc link voltage by compensating for the power needed by the series converter P_2. The indicator is the dc link voltage reached steady-state, in other words, a constant value. The whole system achieves stable when,

$$P_1 = P_2 \tag{6. 9}$$

At system equilibrium, the input power $P_{PCC}(t)$ equals the output power $P_O(t)$, from which the following equation can be found,

$$\frac{V_G V_{PCC}}{Z_g}\cos(-\delta + \emptyset_g) - \frac{V_{PCC}^2}{Z_g}\cos(\emptyset_g) = \frac{V_O^2}{R_O} + \frac{V_{PCC}^2}{Z_L}\cos(\emptyset_L) \tag{6. 10}$$

Consequently, the power angle δ can be obtained.

The TL-UPQC system regulates the PCC voltage by injecting/absorbing reactive power $Q_{PCC}(t)$ to/from the grid. Thus, the amount of reactive power needed by the TL-UPQC system to accomplish voltage regulation can be found using the following equation,

$$Q_{PCC}(t) = \frac{V_G V_{PCC}}{Z_g}\sin(-\delta + \emptyset_g) - \frac{V_{PCC}^2}{Z_g}\sin(\emptyset_g) - \frac{V_{PCC}^2}{Z_L}\sin(\emptyset_L) \quad (6.\ 11)$$

The capacitor C_P together with inductor L_P form an *LC* filter at the grid side. The value of L_P depends on the shunt inductor ripple current. Assuming that the PCC current ripple ΔI_{PCC} is the same as the inductor current ripple then,

$$L_P = \frac{v_{DC}}{4 f_{s_1} \Delta I_{PCC}} \quad (6.\ 12)$$

where, f_{s_1} is the switching frequency of the APF converter.

The resonant frequency of the LC filter is designed to be one tenth of the switching frequency of the converter to avoid any interaction, hence C_P is chosen as follows,

$$C_P \geq \frac{1}{L_P}\left(\frac{1}{0.2\pi f_{s_1}}\right)^2 \quad (6.\ 13)$$

6.2.2 Enhanced Controller Strategy

With the aim of extending the functionality of the proposed control strategy of TL-UPQC, a fourth controller is formalized as follows,

- AC voltage controller – it is used to provide input voltage regulation to the PCC bus through means of reactive power injection.

Figure 6-4 shows the enhanced controller block diagram of the shunt converter. There are three controllers in the shunt APF. Two voltage control loops and one current control loop. In order

to provide voltage support to the grid, the injected APF current is controlled. The default-operating mode of the TL-UPQC system is the PFC mode. In order to provide input grid voltage support, the system will operate in either the inductive or the capacitive mode, hence controlling the phase angle θ of the PCC current. The phase angle θ is governed by the amount of reactive power needed to regulate the PCC voltage. It will also take role to define the absorption of active power. So that the system is decoupled, $i_{PCC}(t)$ is converted into the d-q axis,

$$I_D = I_{PCC}\cos\theta \quad \& \; I_Q = I_{PCC}\sin\theta \tag{6. 14}$$

where,

$$I_{PCC} = \sqrt{I_D^2 + I_Q^2} \tag{6. 15}$$

I_{PCC} represents the steady-state rms values of the PCC current, while I_D and I_Q represent its direct and quadrature components respectively.

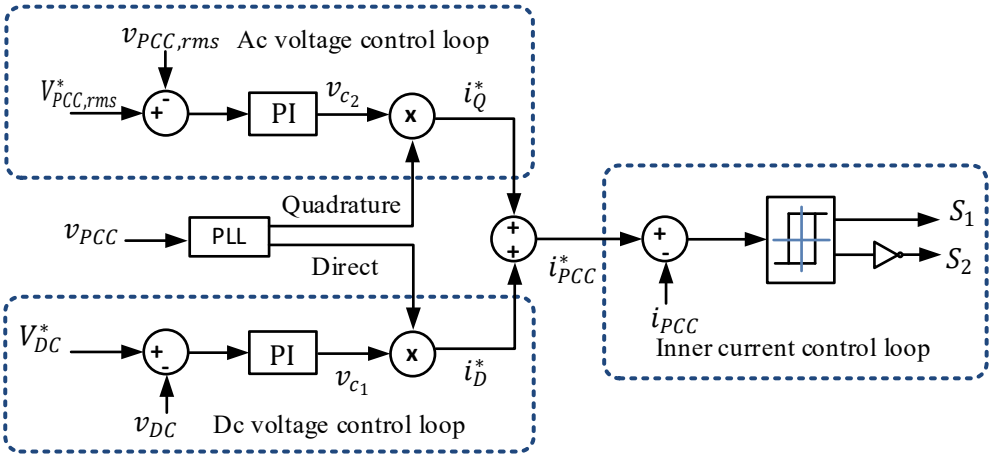


Figure 6-4. Control block diagram of the enhanced control methodology.

The dc voltage control loop is a PI controller, which is used to fix the dc link voltage and determine the direct component of the injected current. The ac voltage control loop is also a PI controller that is used to regulate the PCC voltage and generate the quadrature component of the

PCC current. The reference current signal is then generated by the two outer voltage loops combined with the PLL as follows.

$$i_{PCC}^{*}(t) = i_{D}^{*}(t) + i_{Q}^{*}(t) \tag{6. 16}$$

The inner current control loop is a hysteresis control with specified upper and lower bands as described before in Chapter 4 section 4.3, from which the switching decisions are formed. The series DVR compensation will remain unchanged since the adopted second order boundary control strategy proved to be sufficient enough to provide a fast dynamic response to regulate the output voltage, Chapter 4 subsection 4.6.3.

6.3 System Modeling

For a better insight of the system' dynamic behaviors, the small-signal models determined in Chapter 4 section 4.4 are modified to include the PCC voltage and current. The system new set of linear time invariant equations are defined as follows,

$$\text{Let } \; x(t) = \begin{bmatrix} v_{PCC}(t) \\ i_{PCC}(t) \\ v_{DC}(t) \\ i_{L}(t) \\ i_{G}(t) \end{bmatrix}, u(t) = v_{G}(t), y(t) = \begin{bmatrix} v_{PCC}(t) \\ v_{DC}(t) \end{bmatrix} \tag{6. 17}$$

$$\dot{x}(\mathrm{t}) = \begin{bmatrix} 0 & -\frac{1}{C_P} & 0 & -\frac{1}{C_P} & \frac{1}{C_P} \\ \frac{1}{L_P} & 0 & \frac{1-2q_1(t)}{2L_P} & 0 & 0 \\ 0 & \frac{2q_1(t)-1}{C_{DC}} & 0 & 0 & 0 \\ \frac{1}{L_L} & 0 & 0 & -\frac{R_L}{L_L} & 0 \\ -\frac{1}{L_g} & 0 & 0 & 0 & -\frac{R_g}{L_g} \end{bmatrix} x(t) + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{1}{L_g} \end{bmatrix} u(t) \tag{6. 18}$$

$$y(t) = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} x(t) \tag{6. 19}$$

The state-space matrices are derived using circuit analysis and circuit equations, where $q_1(t)$ is a switching function that is defined as follows,

$$q_1(t) = \begin{cases} 1 & S_1\ off, S_2\ on \\ 0 & S_1\ on, S_2\ off \end{cases} \tag{6. 20}$$

Introducing small perturbations to the state-space variables and linearizing the system around one operating point as follows,

$$v_{PCC}(t) = V_{PCC} + \tilde{v}_{pcc}(t),\ i_{PCC}(t) = I_{PCC} + \tilde{\imath}_{pcc}(t),\ v_{DC}(t) = V_{DC} + \tilde{v}_{dc}(t)$$

$$,\ i_L(t) = I_L + \tilde{\imath}_l(t),\ i_G(t) = I_G + \tilde{\imath}_g(t) \tag{6. 21}$$

where, $V_{PCC}, I_{PCC}, V_{DC}, I_L$ and I_G are the steady-state values, while $\tilde{v}_{pcc}, \tilde{\imath}_{pcc}, \tilde{v}_{dc}, \tilde{\imath}_l$ and $\tilde{\imath}_g$ are the small-signal perturbations of $v_{PCC}, i_{PCC}, v_{DC}, i_L$ and i_g respectively,

In the small-signal model, harmonic components in the load current are neglected as the dynamic of the system is slower than that of harmonics. The fundamental components are considered in the analysis. An assumption has been made that the current control loop is fast enough and will not dynamically affect the voltage control loops. Therefore, the perturbation in duty cycle can be neglected. Hence, the transfer functions of the power stages can be obtained as follows,

$$T_{ac}(s) = \frac{\tilde{v}_{pcc}(s)}{\tilde{\imath}_{pcc}(s)} = \frac{-\left(s+\frac{R_g}{L_g}\right)\left(s+\frac{R_L}{L_L}\right)}{sC_P\left(s+\frac{R_g}{L_g}\right)\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_g}\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_L}\left(s+\frac{R_g}{L_g}\right)} \tag{6. 22}$$

$$T_{dc}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{\imath}_{pcc}(s)} = \frac{2V_{PCC}}{s\,C_{DC}\,V_{DC}} \tag{6. 23}$$

The PCC current $i_{PCC}(t)$ is the same shape as its reference signal with a current sensor gain K_{Ti} as follows,

$$\tilde{\imath}_{pcc} = \frac{\tilde{\imath}^*_{pcc}}{K_{Ti}} \tag{6. 24}$$

The PCC current reference signal is generated by adding the two output of the compensators multiplied by the PLL output with a gain of K_{PLL}, if only rms values are considered,

$$i^*_{pcc}(t) = K_{PLL}(v_{C_1}(t)\sin\omega t + v_{C_2}(t)\cos\omega t) \tag{6. 25}$$

$$i^*_{pcc,rms} = \frac{K_{PLL}}{\sqrt{2}}\sqrt{(v^2_{C_1} + + v^2_{C_2})} \tag{6. 26}$$

Introducing perturbation to i^*_{pcc}, v_{C_1} and v_{C_2} and taking Laplace transformation, the following relation can be found,

$$\tilde{\imath}_{pcc}(s) = \frac{K_{PLL}\cos\theta}{\sqrt{2}K_{T_i}}\tilde{v}_{c_1} + \frac{K_{PLL}\sin\theta}{\sqrt{2}K_{T_i}}\tilde{v}_2 \tag{6. 27}$$

6.3.1 Dc Voltage Loop

Figure 6-5 shows the small-signal model block diagram of the dc voltage loop in a TL-UPQC system. To study the dc voltage loop separately, $\tilde{v}_{c_2}$ is assumed to be zero, thus the transfer functions of the inner loop $T_{in}(s)$ and the process $T_d(s)$ are,

$$T_{in}(s) = \frac{\tilde{\imath}_{pcc}(s)}{\tilde{v}_{c_1}}|_{\tilde{v}_{c_2}=0} = \frac{K_{PLL}\cos\theta}{\sqrt{2}K_{T_i}} \tag{6. 28}$$

$$T_d(s) = T_{in}(s).T_{dc}(s) = \frac{K_{PLL}\cos\theta}{\sqrt{2}K_{T_i}}\frac{2V_{PCC}}{C_{DC}V_{DC}}.\frac{1}{s} \tag{6. 29}$$

A PI controller is applied to control the overall process, which has the following transfer function,

$$T_{C_1}(s) = \frac{\tilde{v}_{c_1}(s)}{\tilde{v}_{dc}(s)} = K_{Tdc}\frac{(K_{P_1}s+K_{I_1})}{s} \tag{6. 30}$$

where K_{Tdc}: is the sensor gain of the dc link voltage.

The frequency response of the overall open loop system can be found by combining the process and controller transfer functions,

$$T_{OL_d}(s) = T_{C_1}(s)\cdot T_d(s) = \frac{2K_{Tdc}K_{PLL}V_{PCC}\cos\theta(K_{P_1}s+K_{I_1})}{\sqrt{2}\,K_{T_i}C_{DC}\,V_{DC}\,s^2} \tag{6. 31}$$

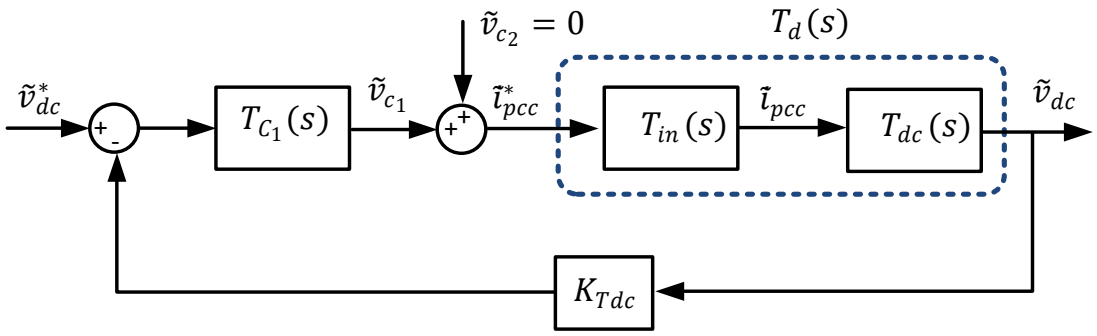


Figure 6-5. Small-signal block diagram of the dc voltage loop.

6.3.2 Ac Voltage Loop

Now, to study the ac voltage loop separately, $\tilde{v}_{c_1}$ is assumed to be zero as shown in Figure 6-6,

$$T_{in}(s) = \frac{\tilde{\imath}_{pcc}(s)}{\tilde{v}_{c_2}}\Big|_{\tilde{v}_{c_1}=0} = \frac{K_{PLL}\sin\theta}{\sqrt{2}\,K_{T_i}} \tag{6. 32}$$

$$T_q(s) = \frac{K_{PLL}\sin\theta}{\sqrt{2}\,K_{T_i}}\cdot\frac{-(s+\frac{R_g}{L_g})(s+\frac{R_L}{L_L})}{sC_P\left(s+\frac{R_g}{L_g}\right)\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_g}\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_L}\left(s+\frac{R_g}{L_g}\right)} \tag{6. 33}$$

Since the open loop gain of the system is negative, the PI controller is designed to include a negative component so the overall gain of the system is positive.

$$T_{C_2}(s) = \frac{\tilde{v}_{c_2}(s)}{\tilde{v}_{dc}(s)} = -K_{Tpcc}\frac{(K_{P_2}s+K_{I_2})}{s} \tag{6. 34}$$

where K_{Tpcc}: is the sensor gain of the PCC voltage.

Now, the transfer function of the overall loop gain of the system is expressed by,

$$T_{OL_q}(s) = \frac{K_{Tpcc}K_{PLL}\sin\theta(K_{P_2}s+K_{I_2})}{\sqrt{2}\,K_{T_i}s} \times \left[\frac{(s+\frac{R_g}{L_g})(s+\frac{R_L}{L_L})}{sC_P\left(s+\frac{R_g}{L_g}\right)\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_g}\left(s+\frac{R_L}{L_L}\right)+\frac{1}{L_L}\left(s+\frac{R_g}{L_g}\right)}\right] \tag{6. 35}$$

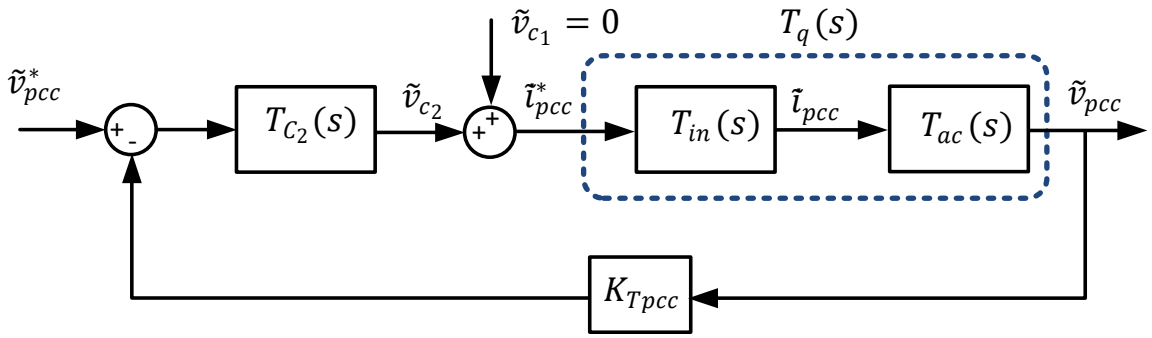


Figure 6-6. Small-signal block diagram of the ac voltage loop.

6.3.3 System Stability and Controller Design

The parameters used for this study are tabulated in Table 6-I. Two criteria have been considered while designing the PI parameters. The first criterion is the limitation of the controller's bandwidth while the second criterion is that the phase margin of the overall system should be sufficient enough to provide control system stability.

The dc voltage loop establishes the reference component in which the dc link capacitor charges. The output voltage ripple across the dc link can be expressed as,

$$\Delta v_{dc}(t) = \frac{V_{PCC}}{2\pi f C_{DC} V_{DC}} [\, -I_{PCC} \sin(2\omega t - 2\delta \pm \theta) + I_O \sin(2\omega t - 2\delta - \emptyset_O)] \quad (6.36)$$

where f is the line frequency and I_O is the steady-state rms value of the load current connected to the output voltage with a displacement angle of $\emptyset_O$. Derivation of (6.36) is given in the Appendix A.3.

It can be observed from (6.36) that the dc link voltage ripple contains 2nd order harmonic components. Therefore, the parameters selection of the PI controller T_{C_1} should be selected to have an overall dc voltage loop bandwidth of approximately one-tenth the double line frequency. Based on (6.29), the frequency response of the dc voltage loop $T_d(s)$ before adding the controller under different operating conditions is highlighted in Figure 6-7. The figure indicates a cross over frequency range of ω_{co_1}: $672.3 - 2714.3\ rad/sec$, which is clearly much higher than the double line frequency.

By defining ω'_{co_1} as the frequency at which the magnitude of the overall open loop system including the controller $T_{OL_d}(s)$ is zero dB,

$$\left|T_{OL_d}(j\omega'_{CO_1})\right| = 1 \quad (6.37)$$

Then, the selection of K_{P_1} and K_{P_2} should satisfy the following criteria,

$$\frac{2K_{Tdc}K_{PLL}V_{PCC}\cos\theta\sqrt{[K_{P_1}^2\omega_{co_1}'^2 + K_{I_1}^2]}}{\sqrt{2}\,K_{T_i}C_{DC}\,V_{DC}\,\omega_{co_1}'^2} = 1 \quad (6.38)$$

and,

$$\omega'_{co_1} \leq 0.1 * 4\pi f \quad (6.39)$$

Since the controller encloses adding a pole at the origin to the overall system, the system is subjected to a phase lag causing a drop in the available phase margin. Consequently, the PI parameters should be selected to provide a sufficient phase margin to the overall system as follows,

$$PM_1' = 180 + \angle T_d(j\omega_{CO_1}') - \tan^{-1}\frac{K_{I_1}}{\omega_{co_1}' K_{P_1}} \geq 45^{\circ} \quad (6.40)$$

where, PM_1' is the phase margin of the overall dc voltage loop open-loop transfer function at the frequency ω_{co_1}'.

Satisfying (6.38) to (6.40), the PI parameter have been chosen to shift the cross over frequency to 13.6 rad/sec maximum at light loads with a minimum phase margin of 74° at heavy loads as shown in Figure 6-8. Light loads indicates that the injected reactive power from the TL-UPQC system to the grid is minimum. It can be concluded that the mathematical model of the dc voltage loop appears to provide a stable operation under different operating points.

The PI parameters of the ac voltage loop T_{C_2} are selected to provide a slower dynamic response than the dc voltage control loop. To avoid any possible interference between the two loops, the bandwidth of the ac voltage loop is designed to be at least ten times slower than the dc voltage loop. It is clear from equation (6.35) that the load connected to the PCC point constitutes the ac voltage control loop. This is true, since PCC voltage fluctuation in a weak grid is dramatically affected by whether the load is light or heavy. In addition, the Thévenin impedance of the connected ac system governs the variation of the PCC system. Based on (6.33) and (6.34), the controller parameters K_{P_2} and K_{I_2} are selected to satisfy the following criteria,

$$K_{Tpcc} \times \frac{\sqrt{K_{P_2}^2 \omega_{co_2}'^2 + K_{I_2}^2}}{\omega_{co_2}'} \times \left|T_q(j\omega_{co_2}')\right| = 1 \quad (6.41)$$

and,

$$\omega'_{co_2} \leq 0.1 * \omega'_{co_1} \tag{6. 42}$$

Similarly, the second criteria to design the PI parameters is,

$$PM'_2 = 180 + \angle T_q(j\omega'_{CO_2}) - \tan^{-1}\frac{K_{I_2}}{\omega'_{co_2} K_{P_2}} \geq 45^{\circ} \tag{6. 43}$$

where, PM'_2 is the phase margin of the overall ac voltage loop open-loop transfer function at the frequency ω'_{co_2}.

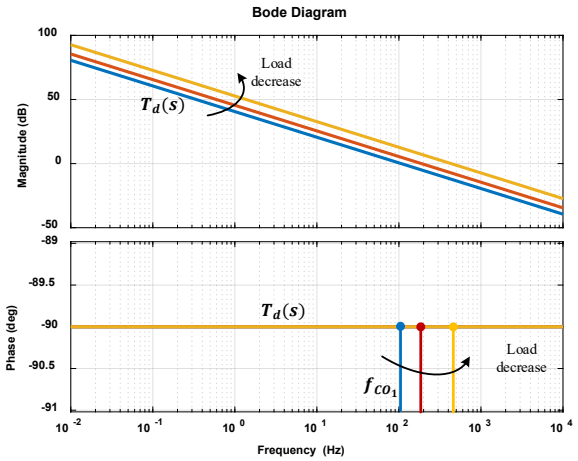


Figure 6-7. Frequency response of the dc voltage loop without a compensator.

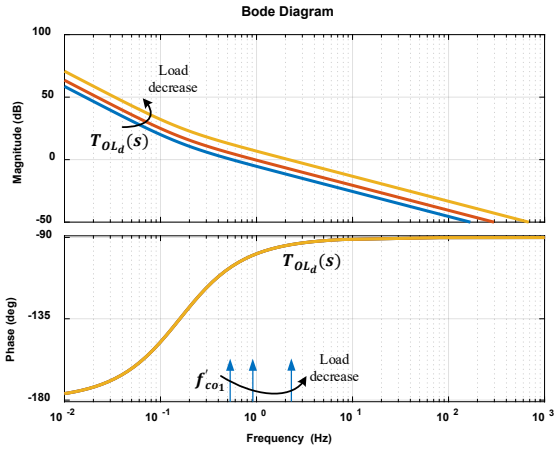


Figure 6-8. Frequency response of the dc voltage loop including a compensator.

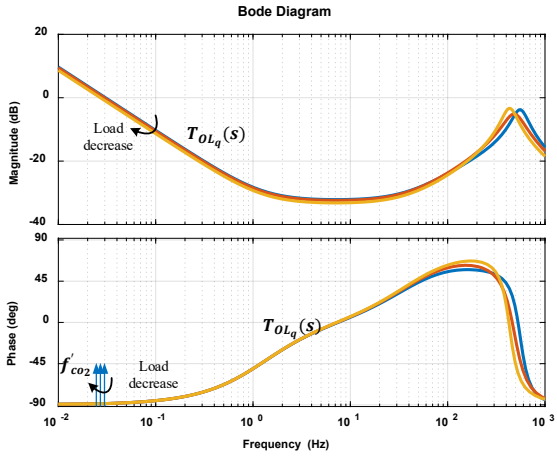


Figure 6-9. Frequency response of the ac voltage loop including a compensator under different loads.

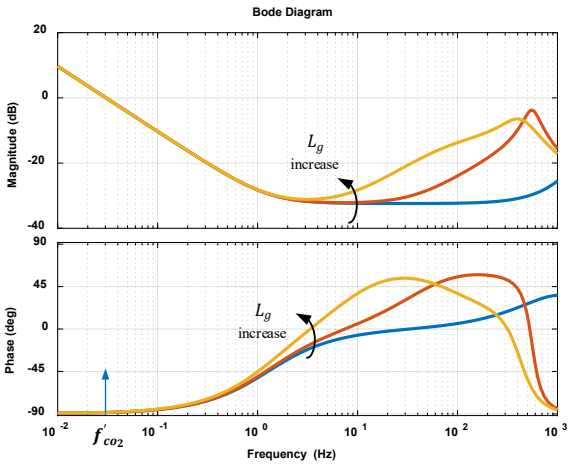


Figure 6-10. Frequency response of the ac voltage loop including a compensator under different grid inductances.

The controller design of the ac voltage loop should take into consideration the maximum loading of the feeder where the TL-UPQC is to be connected. Figure 6-9 depicts the frequency response of the overall system considering the ac voltage loop under different operating points. Satisfying (40) to (42), the phase margin is maintained at 91.4°, while the cross over frequency is 0.2 rad/sec for maximum load (e.g. maximum reactive power injection). To investigate the controller's performance under variations in grid impedance parameters, Figure 6-10 shows the frequency responses of the overall system for $L_g = 0.1\ mH, 20\ mH\ and\ 100\ mH$. The results show that since the location of the system's poles and zeros are at higher frequency, the bandwidth of the system will not be significantly affected. Higher R_g will indicate a higher damping on the grid side. Many techniques have been reported in the literature for grid estimation including passive and active methods [118]. The impact of the grid impedance on grid connected converters should not be neglected, especially for weak grids.

6.4 Experimental Verifications

The TL-UPQC converter prototype has been used to experimentally verify the proposed control strategy for grid voltage support. The laboratory block diagram and setup are shown in Figure 6-11 and Figure 6-12 respectively. An actual resistor and an inductor have been linked between the grid emulator and the PCC to emulate a weak grid. PQ measurements have been performed to investigate the harmonic contents in the waveforms. The PI parameters given in Table 6-I have been chosen based on the small-signal model to satisfy the controllers bandwidth specified in TABLE 6-II.

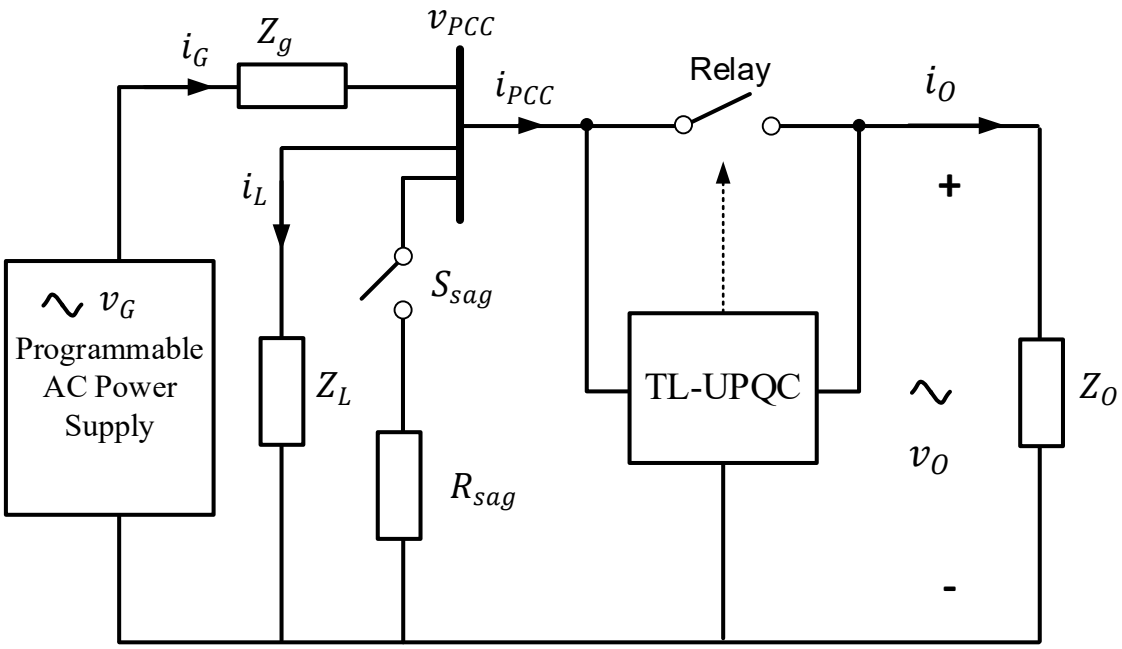


Figure 6-11. Experimental test block diagram.

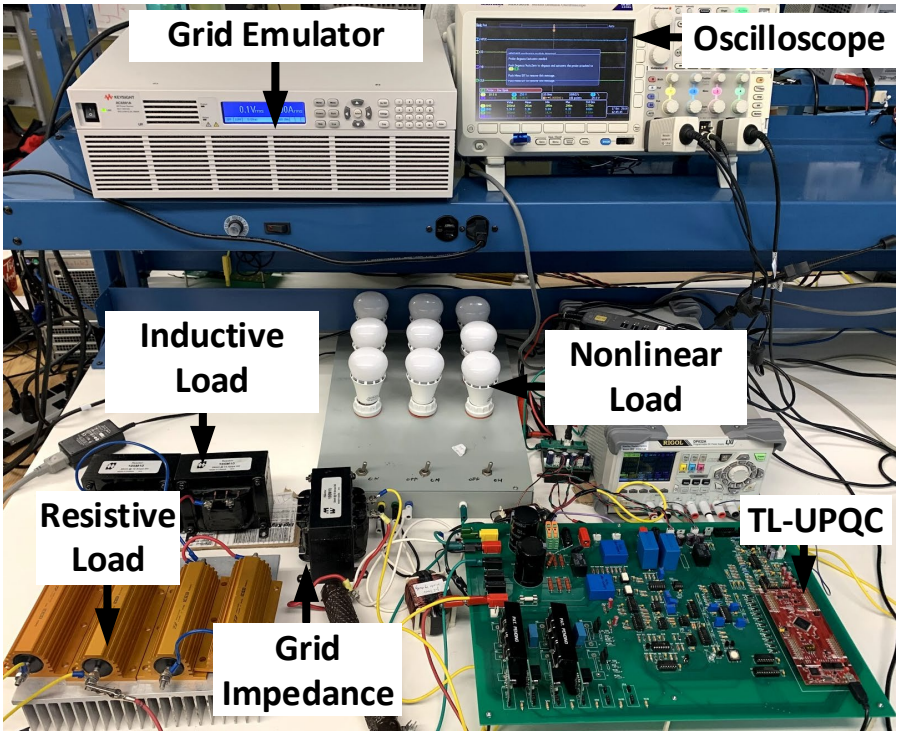


Figure 6-12. Laboratory setup.

TABLE 6-I ENHANCED TL-UPQC SYSTEM PARAMETERS

Parameters	Value	Parameters	Value
PCC voltage	120 V	L_A, C_A	3.4 mH, 14.1 μF
Grid frequency	60 Hz	K_{T_i}, K_{PLL}	1, 9.6
Dc link Voltage	400 V	$K_{T_{dc}}, K_{T_{pcc}}$	0.01, 0.08
R_g, L_g	5 Ω, 20 mH	K_{P_1}, K_{I_1}	0.5, 0.5
C_{DC}	1500 μF	K_{P_2}, K_{I_2}	0.01, 0.08
L_P, C_P	10 mH, 6.8 μF	R_L, R_{sag}	100 Ω, 100 Ω
Nonlinear load at bus B		LED lamps (R_O)	141.18 Ω
Linear load at bus B		R_O, L_O	100 Ω, 40 mH

TABLE 6-II TL-UPQC CONTROLLER DESIGN

Control loop	Bandwidth
Output voltage	6.35 kHz
Input current	1 kHz
Dc voltage	2.17 Hz
Ac voltage	0.03 Hz

6.4.1 Controller Implementation

The whole control law is built in DSP. The measured signals are sampled by the ADC and read by control low accelerator (CLA). The CLA has a low response delay time due to its operation independently from the main central processing unit [145]. Two interrupt service routine (ISR) for high rate and low rate are used. Sensed signals for the APF controller v_{PCC} and v_{DC} are sampled at the low rate ISR, while , i_{PCC} is sampled at high rate to avoid the loss of high switching frequency information and precisely control the inner loop. The PLL block diagram shown in Figure 6-13

has been implemented digitally using the sampled data of v_{PCC}. A notch filter is used to filter out twice the PCC frequency in addition to the exiting loop filter in a conventional PLL.

PI controllers have been executed in the z transform of the continuous time function. The phase information of the PLL output has been used to create two signals. Direct signal PLL_d that has the same phase as of v_{PCC}, the quadrature signal PLL_q leads v_{PCC} by 90°. Alternately, the reference PCC voltage, and the dc link voltage are programed internally from which the sinusoidal converter current reference signal is generated. This reference signal, will carry the phase information θ that will decide which mode is activated, hence the corresponding phase angle δ is decided. DVR controller requires fast dynamic response, therefore the measured signals v_O, i_C, and v_{DC} are sampled with the high ISR rate. The amplitude of the load bus reference voltage is multiplied by PLL_d following the PCC voltage phase.

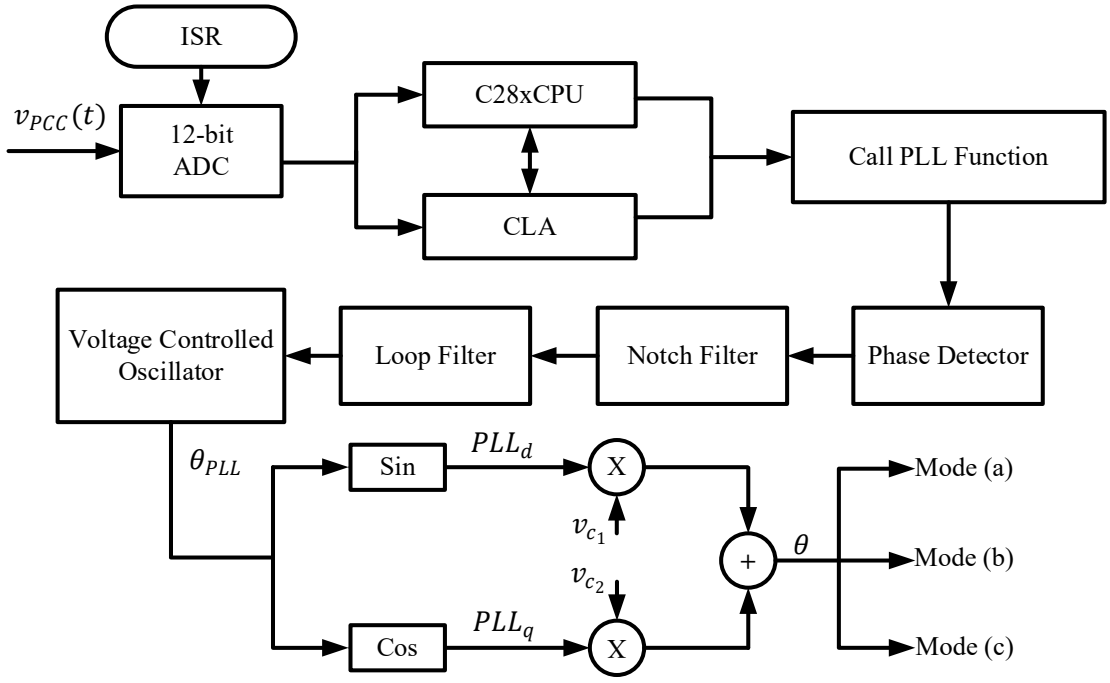


Figure 6-13. Block diagram of PLL implantation in DSP.

6.4.2 Nonlinear Load at the Load Bus

The nonlinear load used in this test is the 9 dimmable LEDs described in Chapter 3 section 3.4. Meanwhile the ac voltage under this test signifies the characteristics of a weak grid. Consequently, nonlinear loads connected to the distribution feeders will not only increase the harmonic contents of the drawn grid current, their nonlinear characteristics behavior will also influence the PCC bus voltage quality. Figure 6-14 (a) displays waveforms of the PCC voltage, grid current, the voltage across the LEDs and the LEDs current without the connection of the TL-UPQC system. The waveforms show highly distorted voltage and current quality. Figure 6-14 (b) and (c) depict the same waveforms after enabling the TL-UPQC. The system is capable of retaining both PCC voltage and the load bus at 120V at the same time. Both voltages have been raised back to 120V. The system is able to perform harmonics mitigation as well. The shunt converter current contains the harmonics contents of the LEDs current, resulting in a low THD in the grid current. Table 6-III gives a comparison between the power quality measurements without and with the operation of the TL-UPQC system for input voltage, output voltage and input current.

TABLE 6-III POWER ANALYSIS MEASUREMENTS WITHOUT AND WITH UPQC SYSTEM

Parameters	W/O TL-UPQC	With TL-UPQC
V_{PCCC}	111.668 V rms	120.008 V rms
$THD - v_{PCCC}$	9.60 %	1.78 %
$THD - v_O$	9.76 %	1.75 %
$THD - i_G$	13.73 %	1.43 %
$THD - i_O$	28.21 %	28.09 %

6.4.3 Linear Load at the Load Bus

To show the ability of the system to provide reactive power support for all types of loads. In this test, the LEDs will be replaced by a linear load. If no voltage regulation is required, the system will be operating in the PFC mode. It follows that, the shunt converter injects reactive power rather than harmonics to achieve unity power factor. The linear load parameters, connected to the output voltage controlled by the TL-UPQC system in this test given in Table 6-I. Figure 6-15 (a) shows the voltage waveforms of the grid voltage, the PCC voltage and the grid current before assisting the TL-UPQC system. In this case, there's an under voltage at the PCC with 108V rms. Figure 6-15 (b) shows the waveforms after activating the TL-UPQC. It can be seen that the shunt converter current $i_P(t)$ leads the PCC voltage in order to inject reactive power and increase the PCC voltage level, which indicates the operation of the system in the capacitive mode. Alternatively, to emulate an over voltage at the PCC bus, the programmable ac power supply voltage was raised to deliver an over voltage of 132V rms at the PCC bus as shown in Figure 6-16 (a). Despite the reflected over voltage at the PCC, the voltage has been maintained at 120V rms by enabling the TL-UPQC as depicted in Figure 6-16 (b). In this case, the TL-UPQC system emulates the behavior of an inductive load absorbing reactive power. In other words the shunt converter current lags the PCC voltage.

6.4.4 Transient

The next experimental case has been carried out to verify the behavior of the UPQC system under dynamic voltage change while it is already in operation. The closure of circuit breaker S_{sag} results in a voltage sag in the network due to a sudden load increase. Figure 6-17 (a) validates the

ability of the UPQC to regulate the PCC voltage under a sudden load increase at the PCC from $R_L = 100\ \Omega\ to\ 50\ \Omega$. Moreover, to emulate the rapid voltage fluctuations of the PCC voltage due to the connection of DER, the programmable ac power supply voltage was varied from 108V to 155V rms while S_{sag} is on. Considering the voltage drop across the grid impedance and before enabling the TL-UPQC system, the PCC voltage was correspondingly fluctuating between 92V and 132V rms. The transitory response of the PCC voltage waveform depicted in Figure 6-17 (b), shows that by enabling the TL-UPQC, the PCC voltage has been successfully maintained sinusoidal with a constant amplitude.

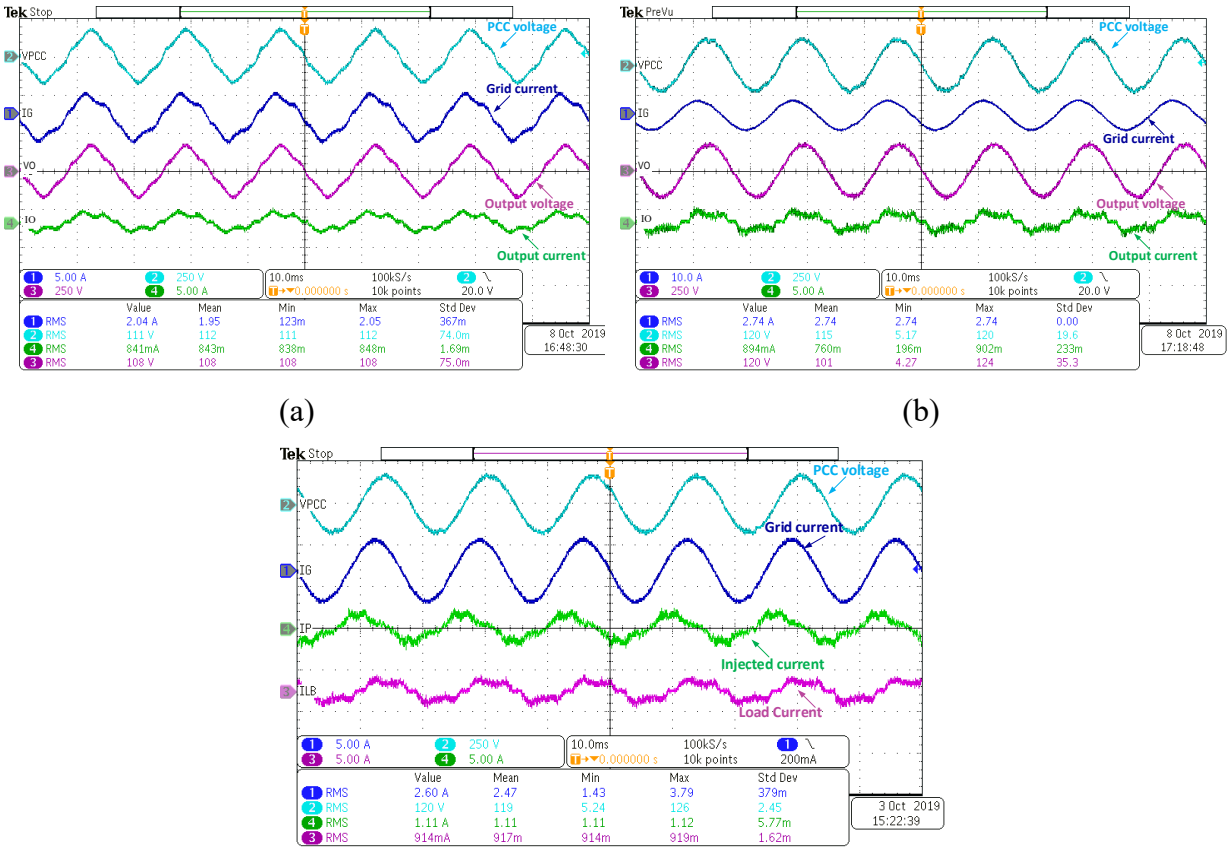
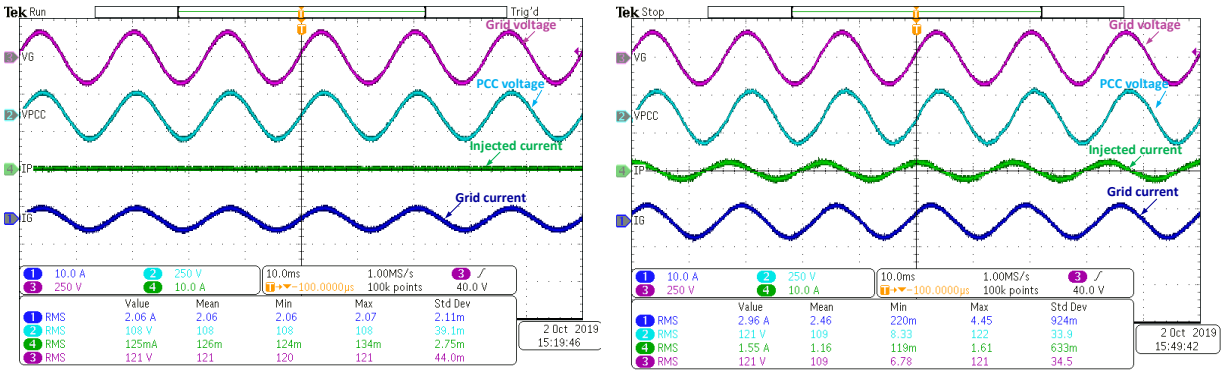
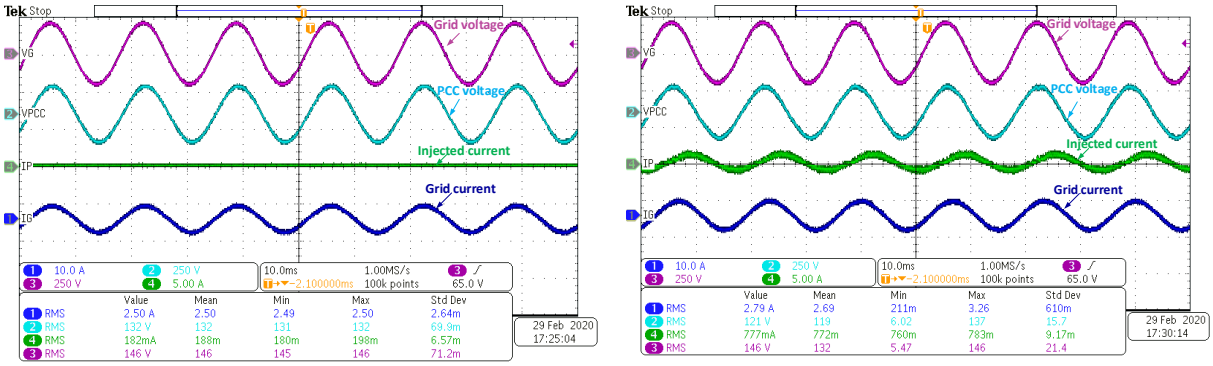


Figure 6-14. System waveforms for nonlinear loads at the load bus (a) without TL-UPQC (b) and (c) with TL-UPQC.



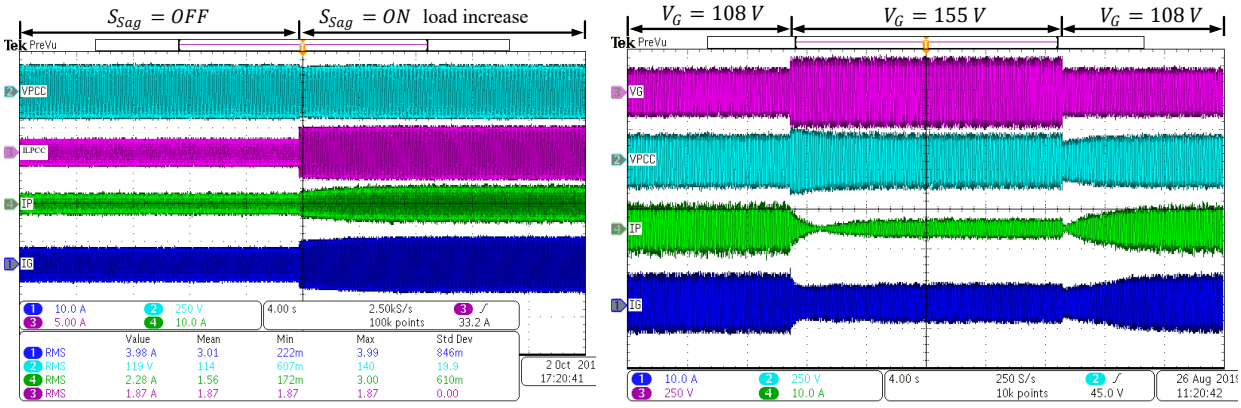
(a) (b)

Figure 6-15. System waveforms during an under voltage for linear loads at the load bus (a) without TL-UPQC (b) with TL-UPQC.



(a) (b)

Figure 6-16. System waveforms during an over voltage for linear loads at bus B (a) without TL-UPQC (b) with TL-UPQC.



(a) (b)

Figure 6-17. Waveforms with TL-UPQC system ($S_{sag} = ON$) (a) a sudden load change at PCC bus (b) with rapid voltage fluctuation.

6.5 Chapter Conclusion

The chapter expanded the control strategy of a TL-UPQC system to be capable of providing reactive power compensation to t system to be capable of injecting and absorbing reactive power into and from the input grid in low voltage distribution networks. Employing the proposed enhanced control strategy, the TL-UPQC was able to filter out harmonic components generated by nonlinear loads, compensate all voltage fluctuations across sensitive loads with fast dynamic response and improve the voltage profile of the input grid. A detailed stability analysis and control design criteria employing small-signal models were presented. The experimental results validated the capability of the system to provide voltage regulation at the PCC while supplying linear and nonlinear sensitive loads at the same time. The system was able to reduce the THD of the PCC voltage, the load bus voltage and the grid current. The operation of the TL-UPQC in the inductive and capacitive modes were demonstrated. The system was competent to deliver a stable voltage with a constant amplitude to the loads connected to the PCC in the event of voltage sags and swells. Experimental results favorably showed good agreements with the theoretical findings.

Chapter 7 Modularized Distributed TL-UPQC Systems with Supervisory Remote Management System

7.1 Introduction

The adoption of DERs connected to the LV distribution network has reformed the configuration of the power system dramatically. Therefore, it is essential to reform existing compensation methods to improve the power quality of the grid as well. Usually, central compensators installed at MV distribution network, as shown in Figure 7-1, require transformers and switchgears for isolation and protection [69]. This configuration fails to guarantee a stable voltage profile for long distance loads. In addition, a failure to the central compensator system leads to complete loss of the existing voltage regulation compensation methodology. Moreover, central harmonic compensators are no longer effective due to the distributed nature of nonlinear loads connected to the network. Compensation units with low power ratings, distributed along LV feeders, would be the right alternative. Distributed compensation units will permit direct interaction between the compensator unit and the load as well as assure identification and mitigation for power quality problems elevated at the LV side where loads are connected. Parallel operation of multiple active filters to share harmonic compensation has been reviewed in

Part of the work presented in this chapter has been published in the following paper: R. Abdalaal and C. Ho, "A Supervisory remote management system for parallel operation of modularized D-STATCOM," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC),* 2020.

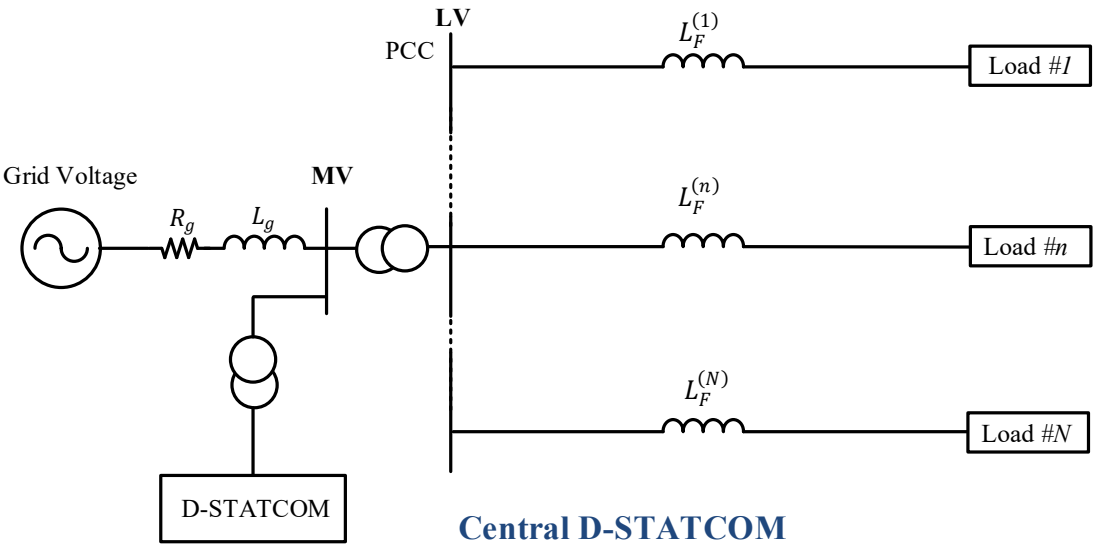


Figure 7-1. Conventional central D-STATCOM architecture.

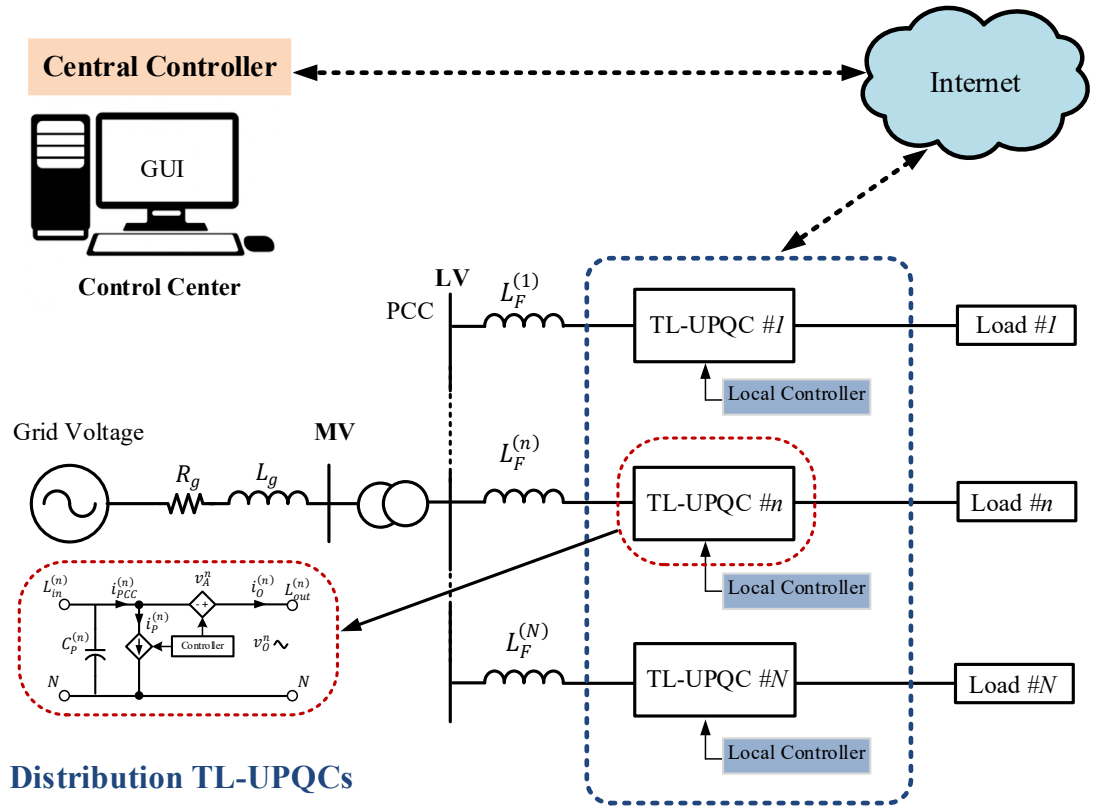


Figure 7-2. Proposed modularized distributed TL-UPQC systems architecture.

Chapter 2 section 2.4. Nevertheless, the coordination between several compensators connected to the same PCC to provide grid voltage support has not been developed yet, neither the unequal reactance of multiple feeders has been considered. In a smart grid, the operation is expected to provide communication and coordination between installed units while providing monitoring capability.

The contribution of this chapter is to propose parallel operation of distributed TL-UPQC systems as depicted in Figure 7-2. The modularized architecture copes with the new distributed nature of a smart grid rather than the centralized power network. The concept of parallel operation of distributed TL-UPQCs is to install modularized small rated TL-UPQCs at LV distribution feeders instead of installing a large capacity D-STATCOM device at the main primary distribution network.

7.2 Parallel-Operated TL-UPQCs

The TL-UPQC system are to be located adjacent to sensitive non-linear loads in the network. Each TL-UPQC module will assure a stable voltage with a constant amplitude across the load bus delivered to the end user and the load connected to the PCC bus. At the same time, the system will eliminate harmonic currents that are being injected to the network due to the nonlinearity nature of the load. In this chapter several TL-UPQC units will work together in parallel to inject/absorb reactive power, hence maintain the PCC voltage at a predefined reference voltage level. The additional advantages of the proposed distributed TL-UPQCs are,

- Parallel operation of TL-UPQCs modules allowing reactive power sharing strategy.

- Improved redundancy allowing multi-module parallel operation while offering high reliability.
- Plug and play feature that does not require identical TL-UPQC modules.
- Smart grid feature by communicating and exchanging information between the distributed modules and the control center.

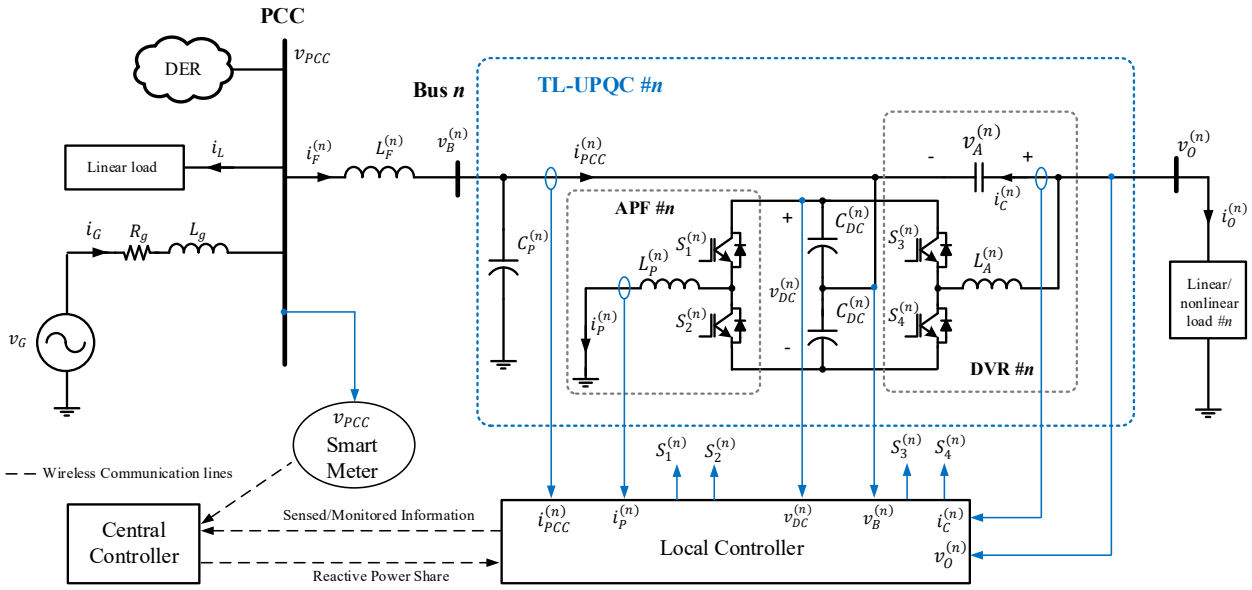


Figure 7-3. Topology and structure of an individual TL-UPQC system.

The coordination between the parallel modules is achieved via a central controller (CC) that is managed by the operator at the distribution substation. Each module will have its own local controller (LC) that will collect local measurements and exchange information with the CC through internet as illustrated in Figure 7-2. The CC monitors the PCC voltage regularly and commands the distributed modules to operate in the input grid voltage regulation mode if necessary. The operation of an individual TL-UPQC converter is based on the topology and the theory of operation that has been developed in Chapter 4 and Chapter 6 as shown in Figure 7-3, which illustrates the topology and the structure of the proposed parallel operation of distributed

TL-UPQs for an individual module *n* in the network, where the parameter's superscript indicates the module's number.

7.2.1 Distributed System Operation

Assuming *N* distributed TL-UPQC units are connected to the network. Each TL-UPQC module is connected to one LV distribution feeder forming a distributed compensator between the network and the load. The module consists of two VSCs that are controlled separately and independently through means of voltage and current controllers as shown in Figure 7-3. Similar to the operation described in Chapter 6, there are three modes of operation; PFC, capacitive and inductive modes.

The system is operating in the PFC mode when no reactive power injection is required to regulate the PCC voltage. In this mode, the module's APF current $i_P^{(n)}$ contains the opposite components of the harmonic currents that are generated by the load connected to the same feeder. It will also contain the reactive power requirement for the load to have a resistive load characteristic. As a result, a sinusoidal and voltage in-phase input current $i_{PCC}^{(n)}(t)$ is drawn from the network bus. The operation of this mode is similar to the converter operation described in Chapter 4. Since this control feature is dependent on information that are collected locally by means of the signals $i_{PCC}^{(n)}$ and $v_{DC}^{(n)}$ which are sampled by the LC, it offers an independent operation of the CC. The generated reference signal is synchronized with module's point of connection bus voltage $v_B^{(n)}$, where each module has its own synchronization angle developed using PLL. Consequently, no wireless communication between the distributed TL-UPQC modules is needed. In this mode of operation, the bus voltage $v_B^{(n)}$ is equal to the PCC voltage v_{PCC}, which

indicates no reactive power exchange is taking place between the converters the network. On the other hand, in order for the TL-UPQC to perform voltage regulation to the PCC voltage, the system will operate either in the capacitive mode or the in the inductive mode. Under the operation of these two modes, the system is no longer providing unity power factor. However, it is still able to compensate for harmonic currents. The module's APF emulates a capacitive or an inductive reactance and injects a current with a full leading (capacitive mode) or full lagging (inductive mode) capability when no active power is required to maintain the dc link voltage.

Different lengths for distribution feeders would lead to line impedance mismatches between the converters and the common bus, causing an unequal voltage drops across the feeder impedances. The PCC voltage and the fundamental component of the bus voltage across each module can be written as,

$$v_{PCC}(t) = \sqrt{2}\, V_{PCC} \sin(\omega t) \tag{7. 1}$$

$$v_B^{(n)}(t) = \sqrt{2} V_B^{(n)} \sin(\omega t - \delta_B^{(n)}) \tag{7. 2}$$

where ω is angular grid frequency, V_{PCC} and $V_B^{(n)}$ are the steady-state rms value of the PCC voltage and the n^{th} module's point of connection bus voltage respectively, while $\delta_B^{(n)}$ is the bus voltage angle corresponding to the PCC voltage.

The active and reactive power transfer between the load bus including the distributed TL-UPQC and the PCC bus are expressed by,

$$P_B^{(n)} = \frac{V_B^{(n)} V_{PCC} \sin \delta_B^{(n)}}{X_F^{(n)}} \tag{7. 3}$$

$$Q_B^{(n)} = \frac{V_B^{(n)} V_{PCC} \cos \delta_B^{(n)} - V_B^{2(n)}}{X_F^{(n)}} \tag{7. 4}$$

The active power flow will be from the bus with the higher phase angle. Usually the active power flow is being transferred from the PCC bus to the load bus unless a DG unit is installed at the load side. In order for the TL-UPQC system to be able to inject reactive power to the grid the magnitude of the module's point of connection bus voltage $v_B^{(n)}$ should be greater than the PCC voltage. On the other hand, the system will tend to operate at a reduced bus voltage magnitude to be able to absorb reactive power. The direction of the reactive power flow is guided by the PCC voltage status. In other words, the direction of the reactive power flow from the distributed TL-UPQC unit to the network will depend on if the disturbance happening in the network is an over voltage or an under voltage. The amount of the injected power by a DER unit or a microgrid into the network, in a grid connected mode operation, directly contributes to the voltage disturbances happening at the point of connection. The relative strength of the ac system is described by the short circuit ratio (SCR) at the connection point. Low SCR is an indication of a weak grid suffering from high voltage variation. The definition of the SCR is expressed as follows,

$$SCR = \frac{V_{nom}^2}{Z_g S_{nom}} \tag{7. 5}$$

where V_{nom} is the nominal rms voltage of the ac network, Z_g is the grid impedance seen from the PCC point, and S_{nom} is the rated capacity of the DER unit.

The module's DVR converter is able to boost or reduce its series voltage $v_A^{(n)}$ by applying BCSSS to the module's DVR. Adopting boundary control technique enables the system to react to voltage disturbances and return to steady-state operation in two switching cycles, which is adequate for sensitive loads. Accordingly, the voltage across the load $v_O^{(n)}$ is regulated as follows,

$$v_A^{*(n)} = v_O^{*(n)} - v_B^{(n)} \tag{7. 6}$$

Now, considering that load bus voltages $v_O^{(n)}$ are being regulated by the series converter, the distributed TL-UPQC systems can take role of providing voltage support to the network. In order for the system to function in the inductive mode or the capacitive mode, a phase angle $\theta^{(n)}$ is created between the drawn input current $i_{PCC}^{(n)}(t)$ and the module's point of connection bus voltage $v_B^{(n)}$. All modules will take part in managing reactive power compensation to support the PCC voltage. The PCC current handled by each module $i_{PCC}^{(n)}(t)$ is expressed by,

$$i_{PCC}^{(n)}(t) = \sqrt{2} I_{PCC}^{(n)} \sin(\omega t - \delta_B^{(n)} \pm \theta^{(n)}) \tag{7. 7}$$

where $I_{PCC}^{(n)}$ is the steady-state drawn PCC current passing through the n^{th} feeder, while $\theta^{(n)}$ is the phase angle of the n^{th} feeder PCC current with respect to the module's point of connection voltage.

The phase angle $\theta^{(n)}$is governed by the amount of the reactive power that is being injected by the n^{th} module into the grid. A leading phase angle indicates that the module is operating in the capacitive mode. Alternatively, a lagging phase angle indicates that the module is operating in the inductive mode. It is worth mentioning that the drawn input current $i_{PCC}^{(n)}(t)$ carries the active power delivered to the load in addition to the reactive power injected to the grid. Therefore, to include a separate controller that manages the reactive power flow from the converter to the network, $i_{PCC}^{(n)}(t)$ is converted to the d-q frame. Hence, controlling the active and the reactive power flow can be accomplished as follows,

$$I_D^{(n)} = I_{PCC}^{(n)} \cos\theta^{(n)} \qquad \& \qquad P_B^{(n)} = V_B^{(n)} I_{PCC_D}^{(n)} \tag{7. 8}$$

$$I_Q^{(n)} = I_{PCC}^{(n)} \sin\theta^{(n)} \qquad \& \qquad Q_B^{(n)} = V_B^{(n)} I_{PCC_Q}^{(n)} \tag{7. 9}$$

where, $I_D^{(n)}$ and $I_Q^{(n)}$ are the direct and the quadrature component of the PCC feeder current respectively.

Ideally the TL-UPQC processed active power of the shunt and series converters are balanced in the equilibrium state. While the reactive power that is handled by the shunt converter of the TL-UPQC module $Q_P^{(n)}$ can be written as,

$$Q_P^{(n)} = \frac{V_B^{(n)} V_{PCC} \cos \delta_B^{(n)} - V^2{}_B^{(n)}}{X_F^{(n)}} + (V_A^{(n)} - V_O^{(n)})\, I_O^{(n)} \sin \emptyset_O^{(n)} \qquad (7.10)$$

It can be observed from (7.10) that the reactive power share of the module's shunt converter is constrained by the load connected at its output terminal. Subsequently, the module's injected shunt current $i_P^{(n)}$contains both reactive power that is needed to support the load and the network. The shunt filter capacitor $C_P^{(n)}$ is designed to provide a high conductance path for the high frequency components that will be injected by the converter. Therefore, the effect of the switching harmonics introduced by the converter can be minimized. Based on the discussed considerations the control law of the parallel operation of distributed TL-UPQCs is obtained in the next subsection.

7.2.2 Control Scheme Structure

The detailed control scheme of the proposed parallel operation of distrusted TL-UPQCs is illustrated in Figure 7-4. The hierarchical structure involves primary and secondary controllers. The primary control represents the LC of each module that collects local measurements. The shunt converter's control law is the main interest of this chapter. The series converter controller will remain unchanged to the control law presented in Chapter 4.

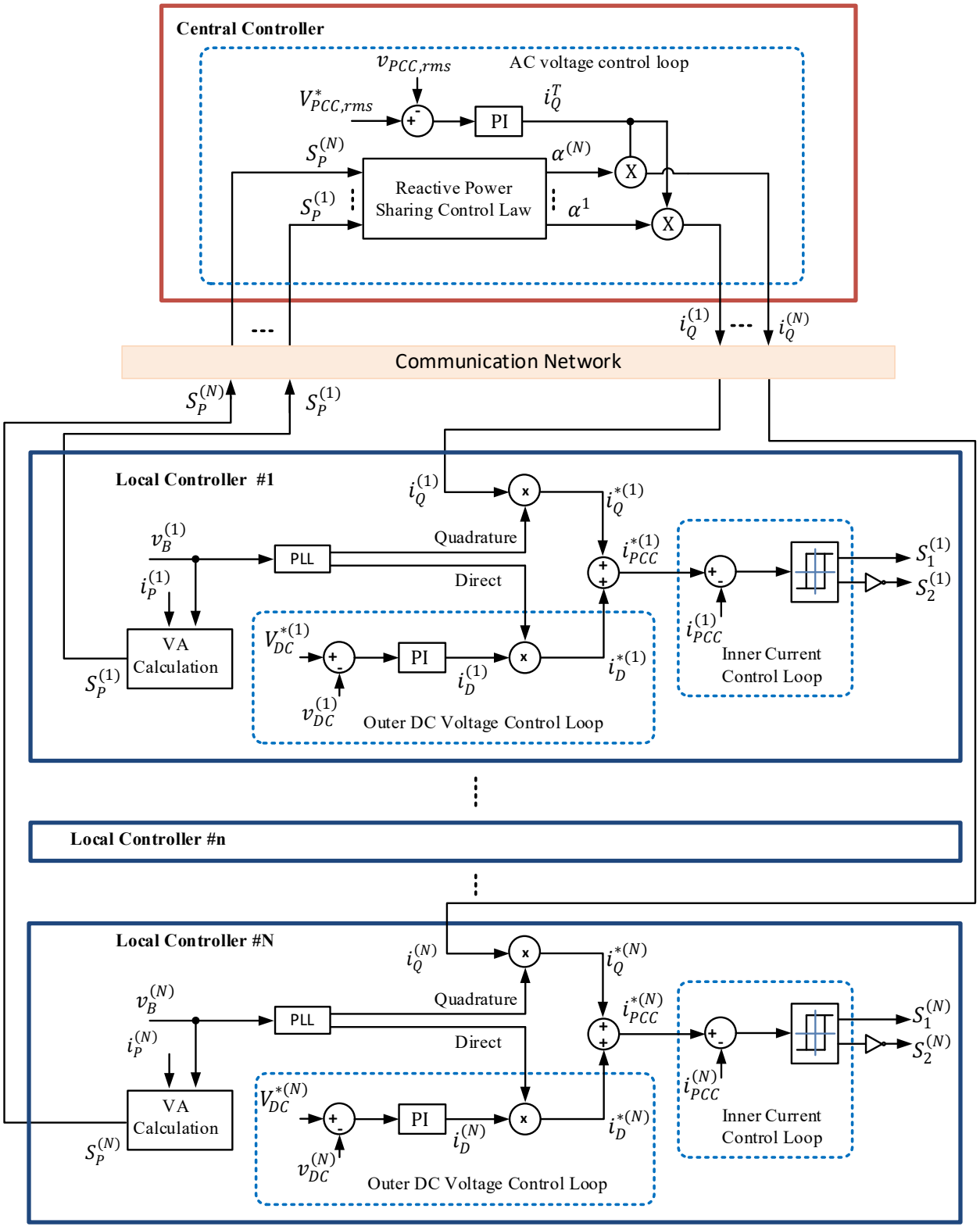


Figure 7-4. Control scheme of parallel operation of distributed TL-UPQC systems.

The sensed signals comprising, the module's dc link voltage, the module's inductor current, the module's point of connection voltage and the drawn input current. These signals are sampled and processed by the module's LC. The secondary control, referred to as supervisory controller, includes the CC. A smart meter is placed at the PCC to monitor the PCC voltage v_{PCC} and the injected power by the DER. This information will be sent wirelessly through internet-based communication network to the CC.

There are two control loops in the LC of the module's shunt converter; 1) an outer dc voltage control loop that is responsible of maintaining the module's own dc link voltage and 2) an inner control loop that shapes the module's input current to follow a specified reference current. A second voltage control loop that controls the PCC voltage at a predetermined value is implemented in the CC. This control loop will be referred to as ac voltage control loop. The output of the module's dc voltage control loop specifies the amount of the active power flow to charge up the dc link capacitor and compensates for the converter losses. It also includes the delivered active power to the load connected to the same feeder. Based on the dc reference decided in the module's LC, the output of the dc voltage controller for each module is given by,

$$i_D^{(n)}(t) = K_{Pm}^{(n)}\left(V_{DC}^{*(n)} - v_{DC}^{(n)}(t)\right) + K_{Im}^{(n)}\int\left(V_{DC}^{*(n)} - v_{DC}^{(n)}(t)\right)dt \qquad (7.11)$$

The CC is responsible to command the distributed TL-UPQCs to exchange reactive power between the modules and the grid, based on the feedback information transmitted by the smart meter. This command will be initiated at the event of voltage disturbances happening at the network side. Otherwise the modules are operating independently on the PFC mode. In the proposed control scheme, a centralized coordination scheme has been adopted, in which reactive power compensation is allocated proportionally among all the modules by the supervisory control.

Thus, the CC will also request each TL-UPQC module to send its measured VA power that is handled by the module's shunt converter $S_P^{(n)}$. The CC will then calculate the proper reactive power share for each module with regard to the module's power rating and its available capacity accordingly. The proportional coefficient $\alpha^{(n)}$ can be found as follows,

$$\alpha^{(n)} = \frac{S_R^{(n)} - S_P^{(n)}}{\sum_{j=1}^{N}(S_R^{(j)} - S_P^{(j)})} \tag{7. 12}$$

where $S_R^{(n)}$ is the rated capacity of the n^{th} module.

The total reference reactive power required is generated based on the reference voltage that is assigned by the operator at the CC and the measured PCC voltage. The response of the output of the ac voltage controller can be found as follows,

$$i_Q^T(t) = K_{Pc}\left(V_{PCC,rms}^* - v_{PCC,rms}(t)\right) + K_{Ic}\int\left(V_{PCC,rms}^* - v_{PCC,rms}(t)\right)dt \tag{7. 13}$$

Afterwards, the CC will assign each module to its proportional reactive power share. Internet protocol (IP) address is used to locate individual TL-UPQCs in the network. The amount of the reactive power share of each module that will be transmitted through the network can be expressed as follows,

$$i_Q^{(n)}(t) = \alpha^{(n)}.i_Q^T(t) \tag{7. 14}$$

It can be noted that current reference of the module's input current comprises two components: 1) direct reference current $i_D^{*(n)}(t)$ and 2) quadrature reference current $i_Q^{*(n)}(t)$. The expressions of currents can be expressed as follows,

$$i_D^{*(n)}(t) = i_D^{(n)}(t)\sin(\omega t - \delta_B^{(n)}) \tag{7. 15}$$

$$i_Q^{*(n)}(t) = i_Q^{(n)}(t)\cos\left(\omega t - \delta_B^{(n)}\right) \quad (7.16)$$

$$i_{PCC}^{*(n)}(t) = i_D^{*(n)}(t) + i_Q^{*(n)}(t) \quad (7.17)$$

Since the injected current follows the module's input voltage PLL, harmonics mitigation is attained. The inner current control loop is implemented using a hysteresis controller that shapes the module's sensed input current. The reference signal is formed with specified upper and lower bands to guide the current following the reference. The module's input current is compared with the actual reference current signal. Hence, the switching criteria of the TL-UPQC's shunt converter semiconductor switches is defined.

Adopting proportional reactive power sharing control law has the advantage of considering the reactive power consumption and/or the harmonic components of the loads that are required by the TL-UPQC system to compensate as well. Non-identical modules can also contribute to the process, which will enhance the plug-n-play feature. In addition, the control law is simple to implement and does not require specific algorithms to estimate the distribution feeders' parameters.

7.2.3 Control Scheme Coordination

The coordination between modules and the supervisory controller is achieved via communication-based control technique. To gain insight into the communication delay effect with respect to the system stability, small-signal analysis has been developed.

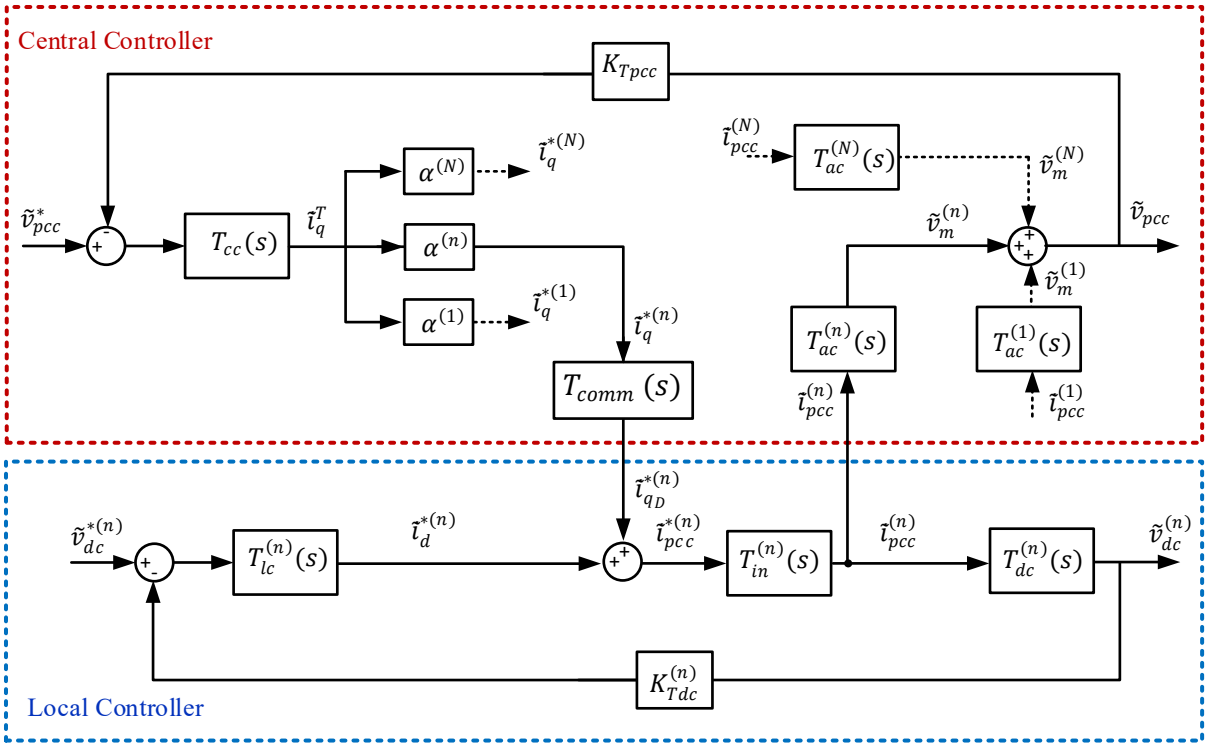


Figure 7-5. Small-signal control block diagram of CC and one LC.

The small-signal control block diagram of one module's LC with its relation to the CC is shown in Figure 7-5. There will be no internal communication between the individual modules. The supervisory controller initiates communication, acquires information and sends control commands to each TL-UPQC module. The perturbation in the PCC voltage $\tilde{v}_{pcc}$ is a result of all modules contributing to provide input grid reactive power support. By means of superposition theorem, the perturbation in the PCC voltage can be represented by,

$$\tilde{v}_{pcc}(s) = \sum_{n=1}^{N} T_{ac}^{(n)}(s)\, \tilde{\imath}_{pcc}^{(n)}(s) \tag{7. 18}$$

Considering one module with its relation to the CC, the transfer functions $T_{dc}^{(n)}(s)$ and $T_{ac}^{(n)}(s)$, which correspond to the dc and ac power stages, can be found deploying state-space analysis as follow,

$$T_{dc}(s) = \frac{\tilde{v}_{dc}^{(n)}(s)}{\tilde{i}_{pcc}^{(n)}(s)} = \frac{2V_B^{(n)}}{s\, C_{DC}^{(n)}\, V_{DC}^{(n)}} \tag{7. 19}$$

$$T_{ac}^{(n)}(s) = \frac{\tilde{v}_m^{(n)}(s)}{\tilde{i}_{pcc}^{(n)}(s)} = \frac{L_F^{(n)}[T_G(s) - T_L(s)]s + 1}{T_G(s) - T_L(s) - C_P s} \tag{7. 20}$$

where,

$$T_L(s) = \frac{L_g}{L_{eq}} \frac{s + \frac{R_g}{L_g}}{\left(s + \frac{R_L}{L_L + L_F^{(n)}}\right)\left(s + \frac{R_g}{L_g + L_F^{(n)}}\right) - \frac{L_F^{2(n)}}{L_{eq}} s^2} \tag{7. 21}$$

$$T_G(s) = \frac{-L_L}{L_{eq}} \frac{s + \frac{R_L}{L_L}}{\left(s + \frac{R_L}{L_L + L_F^{(n)}}\right)\left(s + \frac{R_g}{L_g + L_F^{(n)}}\right) - \frac{L_F^{2(n)}}{L_{eq}} s^2} \tag{7. 22}$$

$$L_{eq} = \left(L_L + L_F^{(n)}\right)\left(L_g + L_F^{(n)}\right) \tag{7. 23}$$

R_L and L_L are load parameters connected to the PCC bus, while R_g and , L_g are the grid impedance parameters and $L_F^{(n)}$is the n^{th} feeder impedance parameter. The derivation of equation (7.20) is given in the Appendix A.4.

The dynamic response of the inner loop is assumed to be very fast with respect to the dc voltage loop. Hence, the transfer function of the inner loop $T_{in}^{(n)}(s)$ can be considered as a constant value throughout the study. The rms value of the output current can be expressed as follows,

$$T_{in}^{(n)}(s) = \frac{K_{PLL}}{\sqrt{2}\, K_{Ti}} \tag{7. 24}$$

where, K_{Ti} is the current sensor gain and K_{PLL} is the PLL gain.

The controller transfer functions T_{cc} and $T_{lc}^{(n)}$ correspond to the two PI controllers used to implement the ac and dc voltage control loops respectively Since the open loop gain of the ac power stage is negative, the CC controller is designed to have a negative gain with the intent to

introduce an overall positive gain into the system. In a hierarchal structure, with moving from primary control to secondary control the controller bandwidth should decrease. Therefore, the bandwidth of the CC has been designed to be at least 10 times slower than the bandwidth of the LC. In other words, the proportional K_{Pc} and the integral controller gain K_{Ic} of the CC are chosen such that the controller dynamics are much slower than the controller response of the dc voltage loop. In this case, the perturbation of the quadrature reference current is neglected with respect to the LC voltage loop and vice versa.

Disregarding the communication delay accompanying the ac voltage control loop, the overall loop gain transfer function of this loop considering one module only can be expressed as follows,

$$T_{OL_q}(s) = -\frac{K_{Tpcc}K_{PLL}}{\sqrt{2}\,K_{Ti}}\left[\frac{K_{Pc}s+K_{Ic}}{s} \times \frac{L_F^{(n)}[T_G(s)-T_L(s)]s+1}{T_G(s)-T_L(s)-C_Ps}\right] \quad (7.25)$$

Figure 7-6 shows the frequency response of the dc voltage loop $T_{OL_d}(s)$ and the ac voltage loops $T_{OL_q}(s)$ in which the bandwidth of the ac voltage loop has been designed to be 0.03 Hz. Figure 7-7 shows the Nyquist diagram of the ac voltage loop ignoring the communication delay effect. Given that the system open loop transfer function does not include any pole in the right-half plane and there's zero encirclements around the critical point (-1, j0), the system is stable. It can also be observed that the ac voltage loop has an infinite gain margin as there is no intersection between the Nyquist plot and the negative real axis.

Nonetheless, wireless communication usually introduces relatively a large delay in the control loop. This means that the communication delay will lead into an even slower bandwidth for the CC. The communication delay corresponds to the network latency $T_D(s)$ that depends on the speed of wireless network and the zero order hold (ZOH) $T_{ZOH}(s)$ that represents the delay caused by sampling a continuous time signal. The reference grid reactive power support will be transferred

to each LC with a delay. The transfer function of the communication delay can be defined as follows,

$$T_{comm}(s) = T_D(s).T_{ZOH}(s) = e^{-sT_d}.\frac{(1-e^{-sT_z})}{sT_z} \quad (7.\ 26)$$

where T_d is the signal transmission delay and T_z is the ZOH step time delay [138].

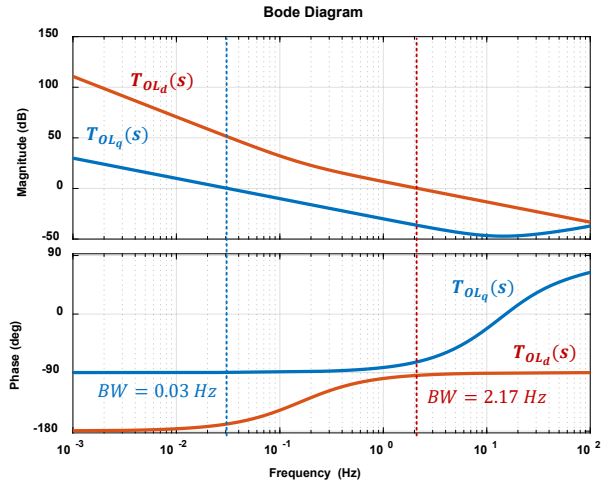


Figure 7-6. Frequency response of the dc voltage loop gain (T_{OL_d}) and the ac voltage loop gain (T_{OL_q}) .

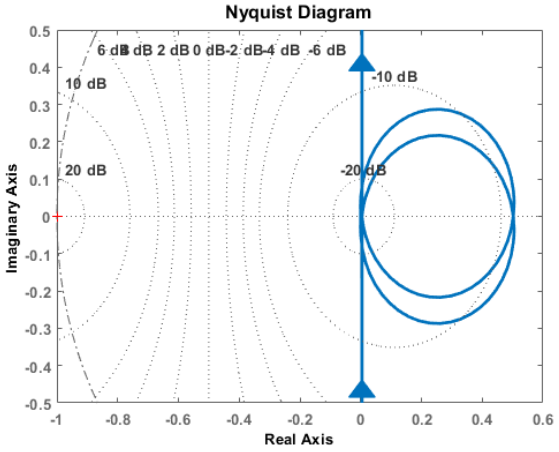


Figure 7-7. Nyquist diagram of the ac voltage loop gain without communication effect $T_{OL_q}(s)$.

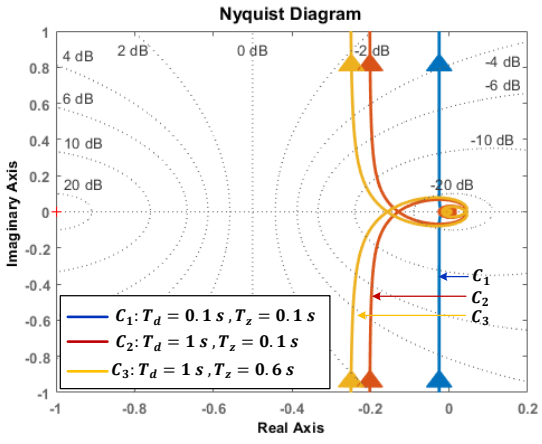


Figure 7-8. Nyquist plot of the ac voltage loop gain under various communication delays $T'_{OL_q}(s)$.

Therefore, the overall loop gain transfer function considering the effect of communication delay is expressed as,

$$T'_{OL_q}(s) = T_{comm}(s).T_{OL_q}(s) \tag{7. 27}$$

The Nyquist diagrams of the overall loop gain of the ac voltage controller at different time delays are shown in Figure 7-8. Even though the diagram indicates that the system is robust under large delays (1 sec), the figure indicates that communication delay would directly affect the system characteristics. It is worth noticing that the Nyquist plot of the system transfer function T_{OL_q} did not intersect with the negative real axis, while the transfer function considering the delay T'_{OL_q} happens to cross the negative real axis an infinite number of time. Therefore, it is important to evaluate the achievable delay margin for the system to time out. The delay margin corresponds to the maximum delay the system can handle before it becomes unstable.

First analyzing the effect of the ZOH, in which a continuous signal is sampled at T_z as highlighted in Figure 7-9. Typically the impulse sampling approach is emulating the behavior of the ZOH implemented in discrete time control systems. For a continuous signal $f(t)$, the output sampled signal, represented by $f^*(t)$, is reconstructed from the sampled data as follows,

$$f^*(t) = f(t)\sum_{k=-\infty}^{k=\infty}\delta(t - kT_z) \tag{7. 28}$$

This can be seen as a two unit step functions that are delayed by one sampling interval with a sampler in front. The ZOH can be further approximated using first order Padé approximation as follows,

$$T_{ZOH}(s) = \frac{\left(1-e^{-sT_z}\right)}{sT_z} \approx \frac{s}{s^2\frac{T_z}{2}+s} \tag{7. 29}$$

Figure 7-10 gives the frequency response of the ZOH and its approximated expression. It can be observed that the ZOH acts as a low pass filter. For signals with frequency components that are greater than the Nyquist frequency $\omega_N = \pi/T_z$, aliasing will take place.

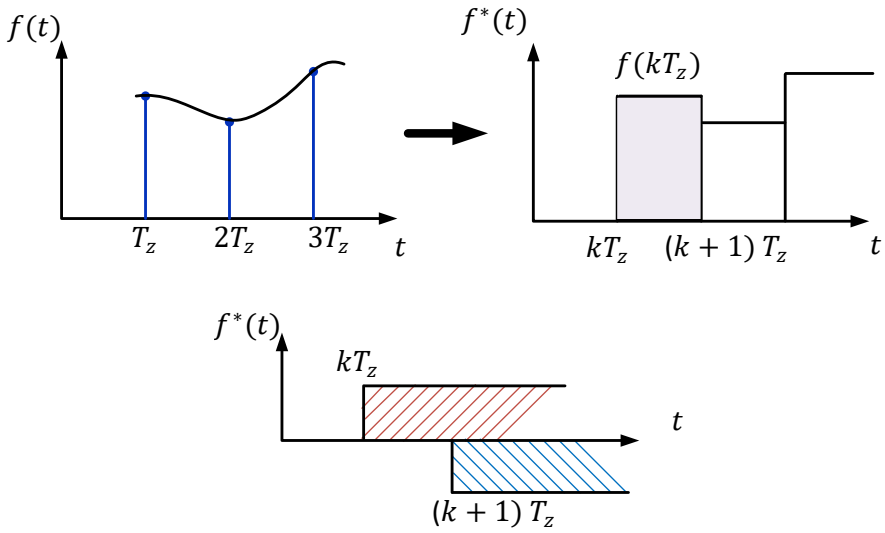


Figure 7-9. Impulse sampling representation of ZOH.

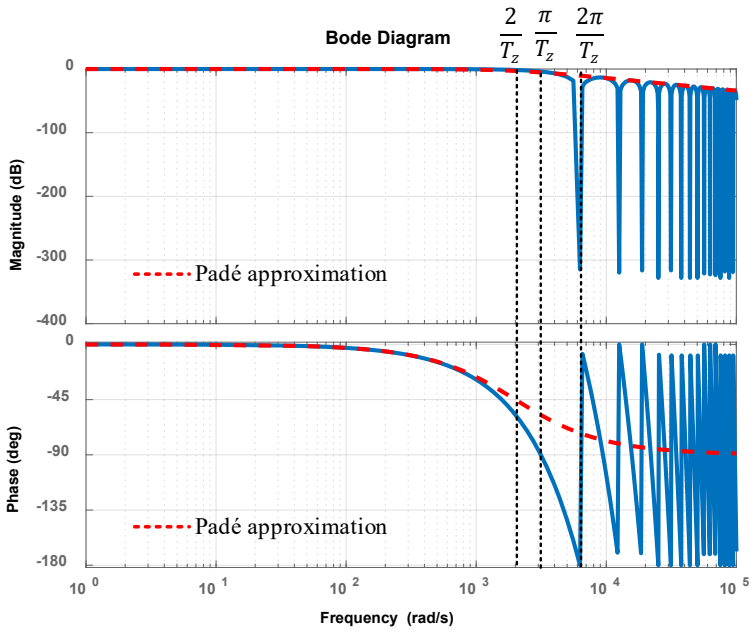


Figure 7-10. Frequency response of ZOH.

Typically an antialiasing filter is added before the sampler to limit the bandwidth of the sampled signals. Moreover, the sampling frequency should be high enough to avoid introducing unwanted phase lags to the designed control system at frequencies lower than the Nyquist frequency. From Padé approximation phase lags starts one decade before the cutoff frequency. It can be concluded that the sampling rate should be designed as follows,

$$\frac{2}{T_Z} \geq 10\omega_c \tag{7. 30}$$

where ω_c is the bandwidth of the ac voltage loop in rad/sec.

TABLE 7-I COMMUNICATION DELAY EFFECT

Parameters	Value
$T_{OL_q}(s)$	$\omega_c = 0.2\ rad/\text{s}, PM_c = 90.2^\circ$
T_z	$1\ ms$
$T_{ZOH}(s).T_{OL_q}(s)$	$\omega_i = 0.2\ rad/\text{s}, PM_i = 90.2^\circ$
$T'_{OL_q}(s) = T_D(s).T_{ZOH}(s).T_{OL_q}(s)$	$T_{d,max} = 7.98\ s$

T_Z can be defined in the digital controller. Table 7-I gives the parameter of the designed control loops including their phase margins. It can be seen that since T_Z is small enough to nearly have any effect on the designed bandwidth and phase margin (without delay). Unfortunately, it is not the case with the communication signal delay T_d. The reason is that this time delay is not fixed and changes according to the speed of the network. Nevertheless, a maximum achievable delay margin can be set to enable system timeout. The magnitude and phase of the delay transfer function can be found as follows,

$$|T_D(s)| = 1, \emptyset_D = -\omega T_d \tag{7. 31}$$

Let PM_i is the phase margin at the frequency ω_i at which,

$$\left|T_{ZOH}(j\omega_i).T_{OL_q}(j\omega_i)\right| = 1 \tag{7. 32}$$

Therefore, the effect of the transmission delay signal on the phase margin will be as follows,

$$PM_i' = PM_i - \omega_i T_d \tag{7. 33}$$

where PM_i' is the phase margin considering communication delay.

It can be observed that the main effect of the signal transmission time delay is a reduction of the phase margin. Hence, the maximum delay margin $T_{d,max}$ can be related to the cross over frequency of the system as well as its phase margin as follows,

$$T_{d,max} = \frac{PM_i}{\omega_i} \tag{7. 34}$$

In order for the system to be robust against large delays, it should have a low bandwidth. According to Table 7-I, the delay margin is found to be 7.98 s. Figure 7-11 shows that the system is marginally stable at the maximum achievable delay margin where,

$$e^{-j\omega_i T_{d,max}}.T_{ZOH}(j\omega_i).T_{OL_q}(j\omega_i) = -1 \tag{7. 35}$$

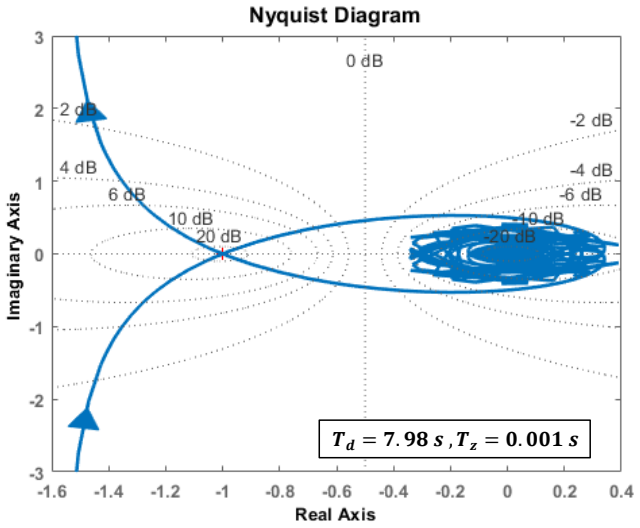


Figure 7-11. Marginally stable Nyquist plot of the ac voltage loop.

7.3 System implementation

To validate the proposed methodology, a controller hardware-in-the-loop (CHIL) testing methodology has been implemented. The experimental set up is shown in Figure 7-12. Figure 7-13 describes the detailed system implementation structure. The test has been performed on two identical TL-UPQCs with shunt rated capacity of 2 kVA. The grid network and the TL-UPQC modules are developed and simulated in real time digital simulator (RTDS). RSCAD simulator program has been used for interface with the RTDS. The series converter has been modeled as a voltage controlled voltage source that regulates the voltage across the output load as depicted in the figure. While the parallel operation of the shunt converters is the interest of this chapter, it is important to include the influence of the series converter on the overall system performance. Therefore, a controlled current source connected to the dc link is modeled inside RTDS, which represents the power needed by the shunt converter to support the series converter.

A current source has been connected to the PCC to emulate the behavior of a PV system. The PV injected power to the network is intended to create voltage variations in the network. Both the grid and the TL-UPQC modules have been simulated using the small-time step library at $2.2\ \mu s$, whereas the PV system, which is modeled as a current source, has been simulated in the large time step at $50\ \mu s$. Different loads are connected at the output of TL-UPQCs. A linear load is also connected to the PCC point to demonstrate that the proposed parallel operation of distributed TL-UPQCs is able to regulate the PCC voltage regardless the loads connected to the PCC. The LC has been implemented using a DSP F28377S with 12 bit ADC resolution. The sensed signals to the controller are sent using Giga-transceiver analogue output (GTAO) card. The digital interface, Giga-transceiver digital input (GTDI) card, provides the gate pulses decided by the DSP to the

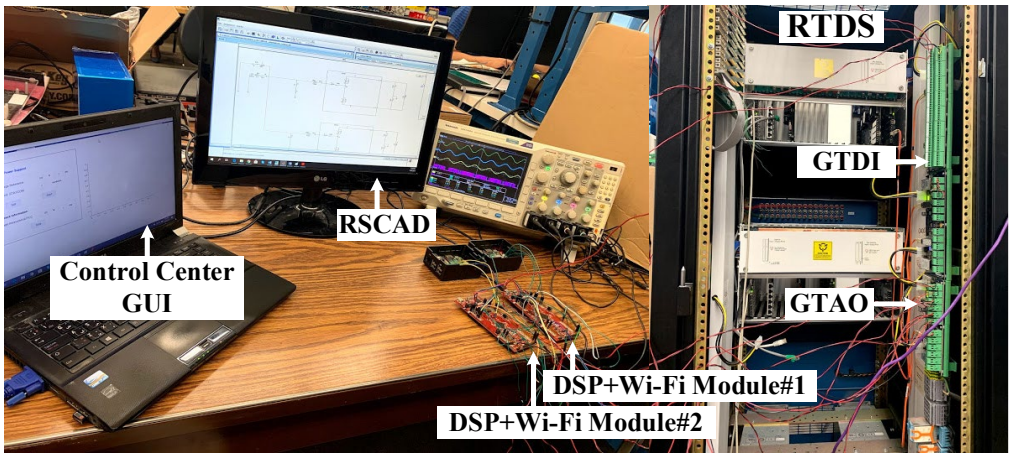


Figure 7-12. Controller hardware-in-the-loop (CHIL) testbed.

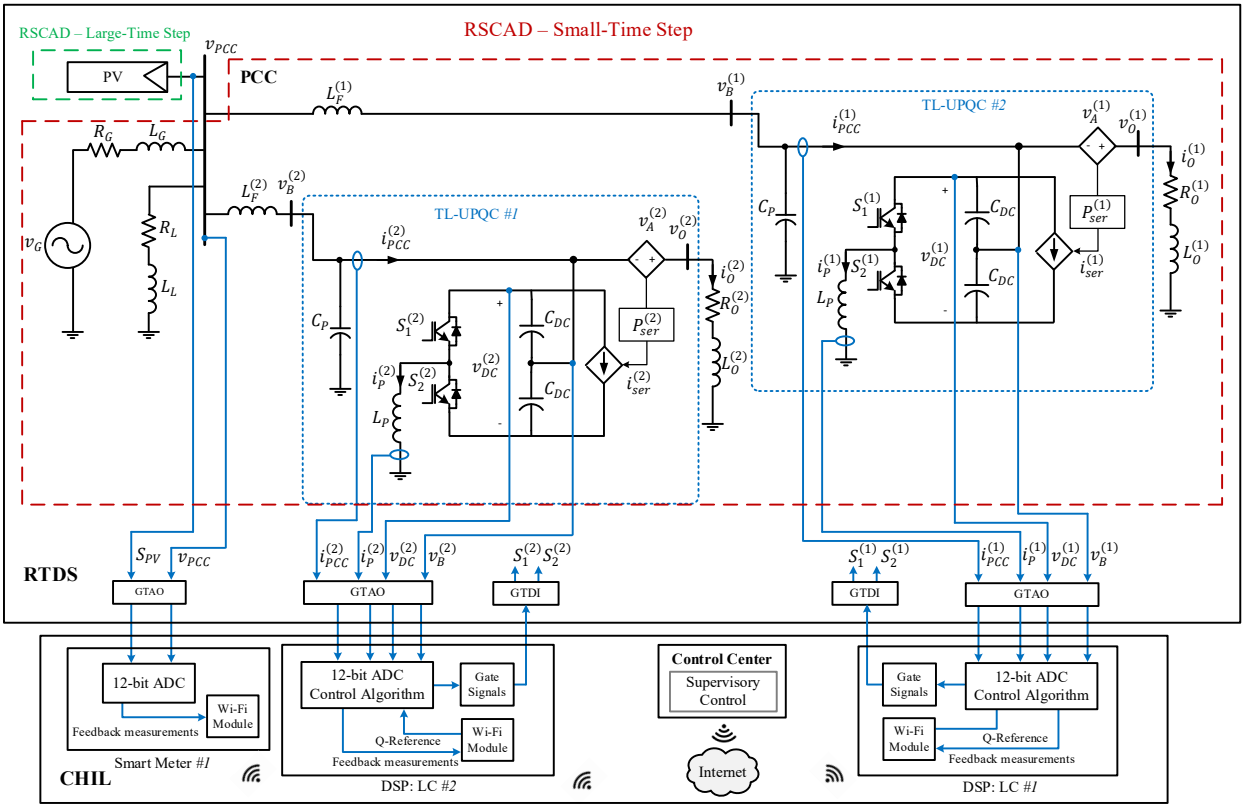


Figure 7-13. System implementation using CHIL with RTDS.

converters modeled inside RTDS. The CC has been implemented in MATLAB software from which a GUI has been developed. A Wi-Fi module has been attached to each DSP to allow wireless

communication between the LC and the CC. SPI has been deployed to exchange data between each DSP and its Wi-Fi module. The smart meter has been also implemented using a DSP with its Wi-Fi module to sample the signals sensed at the PCC point and send the information through the internet to the supervisory control.

7.4 Experimental Verification

7.4.1 Validation of one TL-UPQC module

First the operation of an individual TL-UPQC system will be validated under the CHIL test. The module will operate independently from the supervisory control in the PFC mode and the results will be compared with the achieved steady-state results presented in Chapter 4 section 4.6 subsection 4.6.2. Since the operation is in the PFC, the reactive power share of the TL-UPQC system to support the grid is zero (i.e $i_Q^{(1)} = 0$). Figure 7-14 (a) shows the PFC mode experimental results for a linear load connected at the TL-UPQC output voltage, while Figure 7-14 (b) shows the experimental results for a load comprising of LEDs connected to the system output terminals. The LEDs have been modeled inside RSCAD as a controlled current source that decomposes applying Fourier's series into a fundamental component and a summation of harmonic components. The amplitudes and phases of the injected components of the LEDs current have been calculated using the information of the Sunbeam LEDs under test used in the study presented in Chapter 3. The LED current can be expressed as follows,

$$i_{O,LED} = \sum_{m=1}^{\infty} \sqrt{2}\, I_m \sin(m\omega t + \varphi_m) \tag{7. 36}$$

Another nonlinear load comprises a controlled rectifier bridge circuit with a resistive and an inductive load has been modeled to corroborate the ability of the system to mitigate harmonics for

various nonlinear loads as shown in Figure 7-14 (c). Power quality measurements of the load current and of the input drawn current activating the PFC mode are given in Table 7-II. The results endorses the performance of an individual TL-UPQC to achieve almost unity power factor and THD below 5%. The steady-state results given in Figure 7-14 (a) and (b) shows good agreement with the results presented in Figure 4-18. Note that, the GTAO card includes a 16-bit digital to analogue converter (DAC) and provides an output analogue signal with $\pm$ 10 V output range. Nevertheless, the input signals to the DSP are scaled down within a range of 0-3 V.

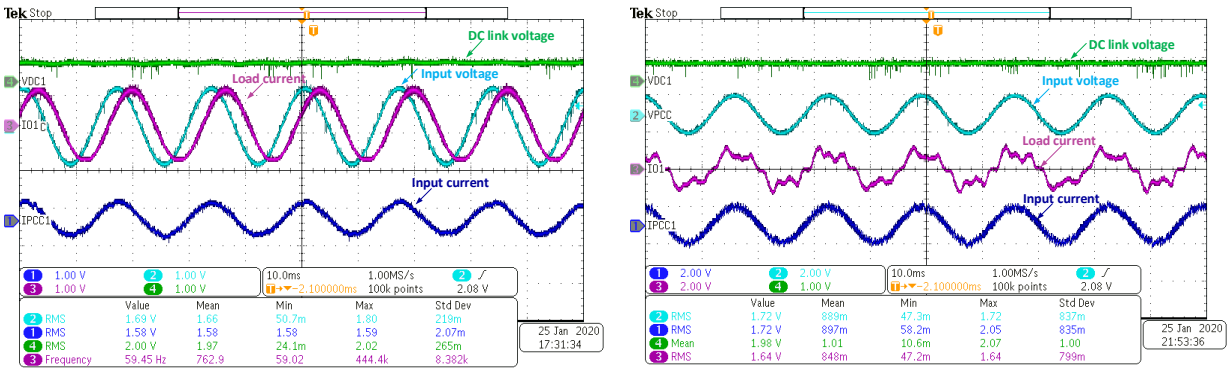


Figure 7-14. PFC mode (experimental results with (a) linear (b) nonlinear load – LED lamps (c) nonlinear load – rectifier bridge circuit.

TABLE 7-II MEASURED POWER ANALYSIS PARAMETERS FOR VARIOUS TYPES OF LOADS

Load under test	Load current	Input current
Case (a)	$PF = 0.55$	$PF = 0.973$
Case (b)	$THD_i = 32.27\%$	$THD_i = 4.65\%$
Case (c)	$THD_i = 15.69\%$	$THD_i = 4.34\%$

7.4.2 Validation of parallel operation of TL-UPQCs

Now the parallel operation of two TL-UPQC modules to provide input grid voltage regulation is evaluated. A case study has been conducted with a PV system rated at 8 kW and an SCR of 0.92. The PCC voltage is to be maintained at 120V rms. The parameters of the system under study have been specified in Table 7-III. As mentioned before, the default operation mode of each module is to operate independently at the PFC mode without relying on any communication signals as presented in the previous section. Therefore, in order for the system to switch its operation to the inductive or the capacitive mode, a command will be initiated by the supervisory control.

Figure 7-15 shows the GUI that allows the operator to define an ac voltage reference and start the reactive power support operation based on the number of the available TL-UPQC modules in the network. The GUI also includes real time data logging and monitoring for the available generated PV power and the PCC voltage measurements. The results shown in Figure 7-15 imply that the PCC voltage is fluctuating between 0.8 and 1.2 pu voltage before enabling the parallel operation of the distributed TL-UPQCs. These voltage fluctuations are happening due to the random behavior of the PV injected power as the figure indicates. Nevertheless the PCC voltage has been maintained at 1 pu after activating the reactive power support of the connected modules.

The steady-state waveforms in Figure 7-16 (a) show that the operation of both modules is coordinated in the capacitive mode to regulate the PCC voltage. It can be seen that both currents are leading the PCC voltage under this mode of operation to boost the PCC voltage. Though, the contribution of the first module to support the grid is larger with 60% share of grid reactive power support (e.g. $\alpha_1 = 0.6$ and $\alpha_2 = 0.4$). This is expected due to the fact that the load connected to the second module is larger than the load connected to the first module, hence the second module is already contributing with a larger reactive power compensation to its load, which is the module's highest priority. The operation is contradictory in the inductive operation mode as shown in Figure 7-16 (b). The injected currents by the TL-UPQCs are lagging in this case since there is an over voltage. For a better insight regarding the module's currents waveforms with respected to the module's point of connection voltage, the waveforms in both modes as captured in RSCAD run time are shown in Figure 7-17. Both modules' dc link voltages have been maintained at 400V as captured in RSCAD run time environment in Figure 7-18.

TABLE 7-III SYSTEM SPECIFICATIONS

Parameters	**Value**
PCC voltage	120 V
Grid frequency	60 Hz
No. of connected modules *N*	2
Module's dc link Voltage, C_{DC}	400 V, 1500 µF
R_g, L_g	0.5 Ω, 5 mH
R_L, L_L	5 Ω, 10 mH
L_p, C_P	10 mH, 47 µF
$L_F^{(1)}, L_F^{(2)}$	1 mH, 2 mH
$R_O^{(1)}, L_O^{(1)}$	100 Ω, 80 mH
$R_O^{(2)}, L_O^{(2)}$	10 Ω, 20 mH

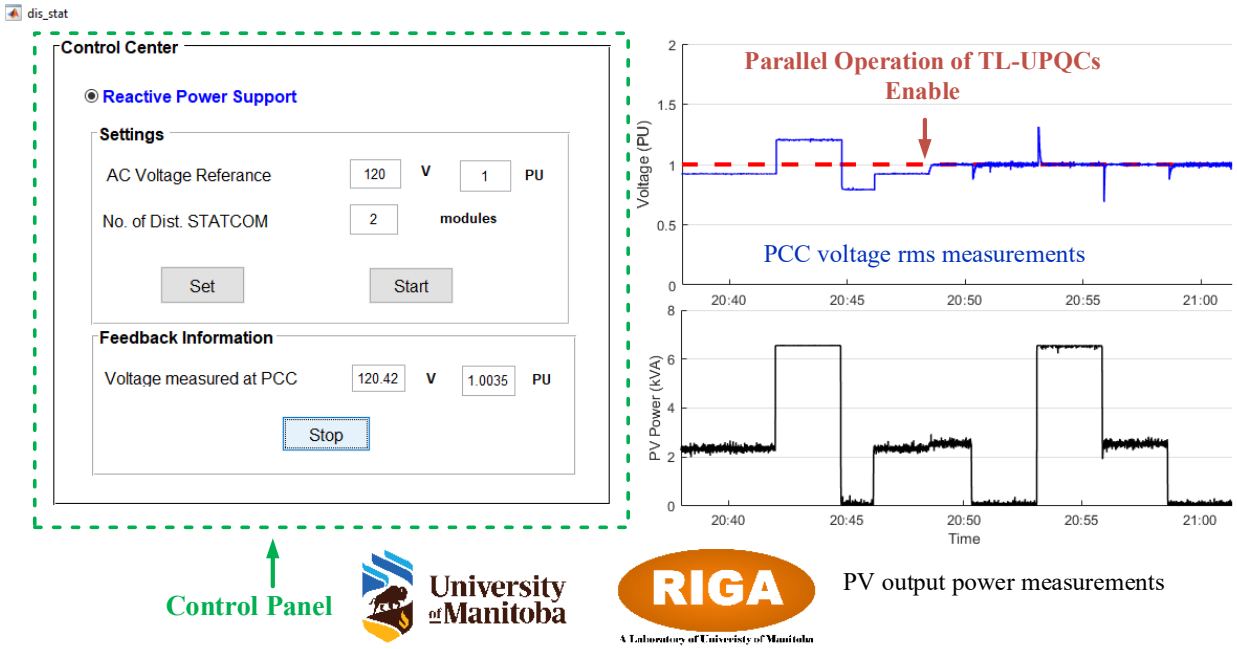
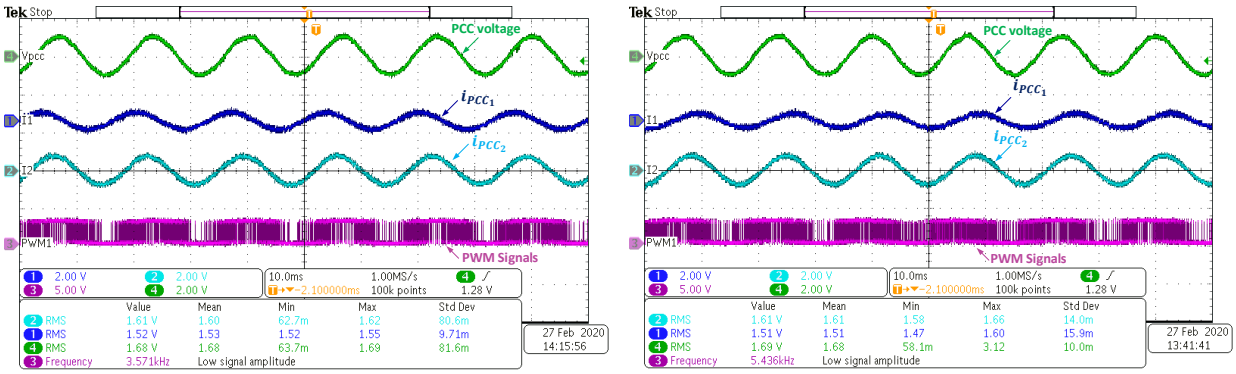
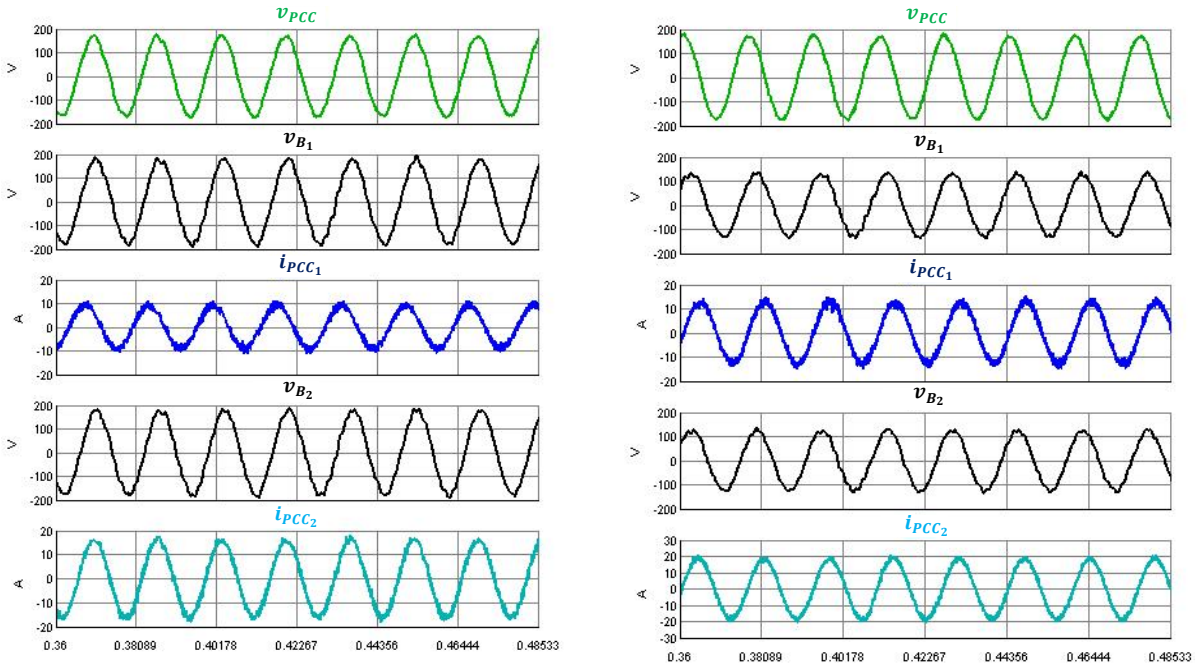


Figure 7-15. GUI - control center panel.



(a) (b)

Figure 7-16. Steady-state waveforms for (a) capacitive mode (b) inductive mode.



(a) (b)

Figure 7-17. Steady-state waveforms captured in RTDS for (a) capacitive mode (b) inductive mode.

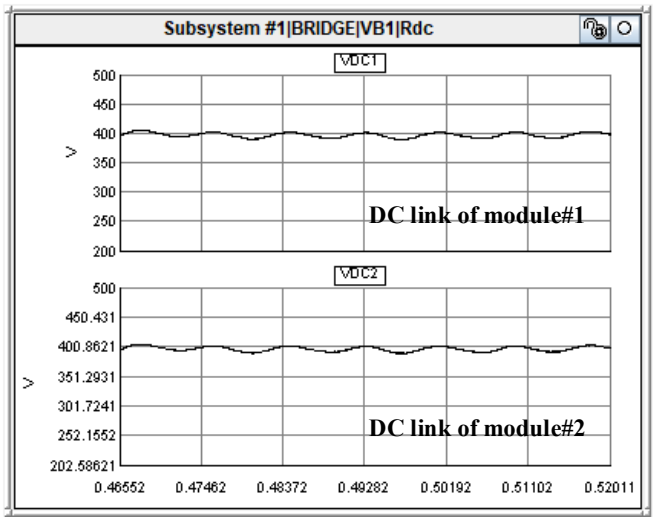


Figure 7-18. Dc link measurements as captured in RTDS.

7.5 Chapter Conclusion

The paper proposed a coordinated operation of distributed TL-UPQCs connected to LV feeders. Proportional reactive power sharing technique to support the input grid voltage based on the unit capacity was presented. A remote management system that represents a centralized supervisory control was proposed. The control commands are sent from the central controller to the local controllers, with no interaction between individual modules. This allow independent operation of the modules if no voltage regulation is necessary. A GUI was developed to perform as a supervisory management system in the control center. The communication delay between the central controller and the local controller was considered in the control design criteria. Maximum achievable delay margin was defined and calculated to be considered during the controller design process. The experiment test was conducted in real time simulation, with the power stage in RTDS while controllers are implemented in DSP. The results verified the ability of the TL-UPQC modules to provide grid voltage stability. The stability of the PCC voltage was improved and maintained at 1 pu. The experimental results of the controller hardware-in-the-loop test showed good agreements with the theoretical concept.

Chapter 8 Conclusion and Future Work

8.1 Conclusion

This thesis investigated the operation of light emitting diode (LED) lamps and their behavior as nonlinear loads. The key findings of the LEDs characterization tests are two main power quality issues associated with the utilization of LED lighting technology: harmonics injection affecting the utility side and flickering phenomena affecting the end-users. Recommendation determined from the study that applying amplitude variation technique to achieve dimming should be followed rather than using conventional dimming techniques such as TRIAC-dimmer system. This will limit the injected harmonics to the level designed by the manufacture.

A transformerless unified power quality conditioner (TL-UPQC) system was proposed to perform as a power quality conditioner that is connected between the ac source and the LED lighting network. Boundary control with second order switching surface was employed in the series converter in order to retain the output voltage across the LEDs in two switching cycles. The shunt converter showed an inherently stable operation under hysteresis control. The system can be applied to sensitive and nonlinear loads. Based on the results of the implemented laboratory prototype, the system proved to mitigate harmonics and compensate reactive power by injecting opposing current components through the shunt converter. The results showed a stable and a constant amplitude voltage across the LED lamps through the series converter. The system was able to mitigate flickering, under and over voltages. The performance of the system showed a fast dynamic response against voltage sags and swells. A novel approach was adopted to achieve

dimming and endorse energy saving. Dimming was achieved with high voltage and current quality waveforms that lead to a high power factor and a low input current harmonic distortion. A remotely central dimming system for a large penetration of LEDs was proposed. The remote management system allowed the operator in the control center to schedule a dimming profile for the system to follow automatically. The system is applicable to commercial dimmable LED lamps and does not require additional wiring nor specific adjustments to the LED driver. The system is not valid for dimming non-dimmable LED lamps.

The TL-UPQC features were enhanced by including input grid voltage regulation. The experimental results showed that the system was able to support loads connected to the PCC as well by means of reactive power support. The controller took action based on local information collected by the TL-UPQC with no requirements of additional sensor circuits or grid information dependency. A small-signal model that characterized the dynamics of the power stage and the controller was developed along with controller design criteria.

Hierarchical control structure for modularized distributed TL-UPQC was proposed. The secondary controller design included a lower bandwidth than the primary control. The experimental results of the CHIL test showed good agreements with the theoretical concept. The most critical challenge in wireless communication technology is the delay time of communication between the control center and the TL-UPQC system. The delay time may lead to unstable operations since it is in the system control loop. Therefore, a methodology to determine the system's delay margin before it becomes unstable was developed. Overall system stability analysis to identify the influences of load changes, grid impedance variations and delay time were conducted.

Overall, the system is considered to be a promising and a comprehensive solution covering most aspects of issues related to power quality in low voltage distribution networks. Table 8-I provides the key features of the proposed TL-UPQC with a reference guide to the thesis content where each power quality problem mitigation technique has been presented, analyzed and validated.

TABLE 8-I TL-UPQC SYSTEM FEATURES

TL-UPQC system features	**Chapter**
High input current power factor with low total harmonic distortion: • Harmonic mitigation and reactive power compensation.	4
A sinusoidal with constant amplitude output voltage: • Critical loads support against voltage flickering, short and long voltage variations. • Fast dynamic response.	4
Allow amplitude voltage variation technique: • Achieve dimming • High quality voltage and current waveforms.	5
Input grid voltage regulation: • Input grid reactive power support. • Improve the grid voltage profile.	6
Coordination between modularized distributed modules: • Reactive power sharing technique between the modules.	7

8.2 Research Contributions

The key contributions of the research work presented in this thesis are listed below:

- The thesis comprehends a solid reference for researchers working on power quality improvement of LED lamps.

- An intensive study covering the basic structure of LEDs, driver topologies, LED standards, harmonics emission and output light sensitivity to voltage fluctuations was presented.
- APFs were introduced as a promising solution for LED applications. The TL-UPQC topology was proposed to solve most of dynamic and static power quality problems in LED lighting networks. A prototype was implemented and validated the proposed system and its controller strategy.
- The system can be adopted to any sensitive load by maintaining the voltage across the load at a constant and a stable value.
- Developments of small-signal models and their validations were presented.
- Detailed design criteria to extend the TL-UPQC system features and include input grid reactive power support was presented.
- Parallel operation between modularized distributed TL-UPQCs was proposed and validated in real time simulation.
- Smart grid feature by allowing controlling and monitoring capability through a supervisory remote management system was introduced.
- Methodology to determine the maximum communication network delay was developed.

Journal/Transaction Papers

1) R. M. Abdalaal, C. N. M. Ho, C. K. Leung and H. S. Chung, "A remotely central dimming system for a large-scale LED lighting network providing high quality voltage and current," *IEEE Trans. Ind. Appl. vol.* 55, no. 5, pp. 5455-5465, Sept.-Oct. 2019.

2) R. Abdalaal and C. Ho, "Characterization of Commercial LED Lamps for Power Quality Studies," *IEEE Can. J. Elect. Computer Eng*. 2020, early access.

3) R. Abdalaal and C. Ho, "Enhanced single-phase transformerless UPQC integrated input grid voltage regulation in low-voltage distribution networks," *IEEE J. Emerg. Sel. Topics Power Electron.* **(Under Review)**

4) R. Abdalaal and C. Ho, "Analysis and validations of modularized distributed TL-UPQC systems with supervisory remote management system," *IEEE Trans. Smart Grid* **(Under Review)**

Filed Patent

5) N. Ho, R. Abdalaal, and H. Chung, "Transformerless Single-Phase Unified Power Quality Conditioner (UPQC) for Large Scale LED Lighting Networks, US Patent Application, US20190182917A1, 13/06/2019.

Conference Papers

6) R. M. Abdalaal and C.Ho, "Characterization of commercial LED lamps for power quality studies," in *Proc. IEEE Elect. Power Energy Conf. (EPEC),* 2017, pp. 1–6.

7) R. M. Abdalaal and C. N. M. Ho, "Transformerless single-phase UPQ for large scale LED lighting networks," in *Proc. IECON Ann. Conf. IEEE Ind. Electron. Soc*., 2017, pp. 1629–1634.

8) R. Abdalaal and C. Ho, "A remotely control dimming system for LED lamps with power factor correction", in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE),* 2018, pp. 4721–4727.

9) R. Abdalaal and C. Ho, "A supervisory remote management system for parallel operation of modularized D-STATCOM," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC),* 2020.

8.3 Future Work

This section describes suggestions for further research as an extension for the research work conducted in this thesis.

- Improving the performance of the TL-UPQC controller by pushing the switching frequency to higher values. One way is to investigate different control methodologies like PI control for the series converter or increase the sampling frequency employing field-programmable gate array (FPGA).
- Increase the system's bandwidth for the ac voltage loop of the shunt converter by investigating different control methodologies.
- While Silicon (Si) power semiconductor devices limit the efficiency of the system, wide bandgap (WBG) devices are gaining a lot of interest recently to improve the efficiency of the system and achieve high power density. It is recommended to evaluate the performance of the TL-UPQC while utilizing Silicon Carbide (SiC) and Gallium Nitride (GaN) power semiconductor devices to achieve higher efficiency especially for applications that require dimming function. Higher power density with lower filter sizes can also be achieved.
- The proposed TL-UPQC has been proposed for single-phase application, however it can be utilized for three-phase systems. Three-phase TL-UPQC system can be proposed as a continuation for this research work. A three-phase system will include output voltage balancing control, input current balancing with unity power factor. The three-phase output

voltage regulation can be controlled independently. Fast recovery response for the output voltage when boundary control is utilized. In addition, a balanced three-phase input grid voltage support can be achieved.

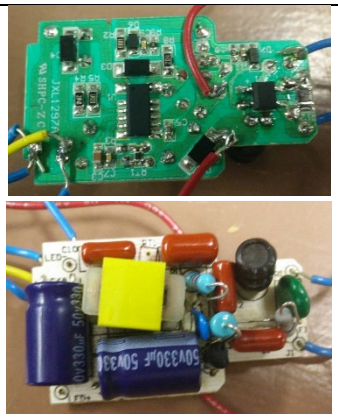
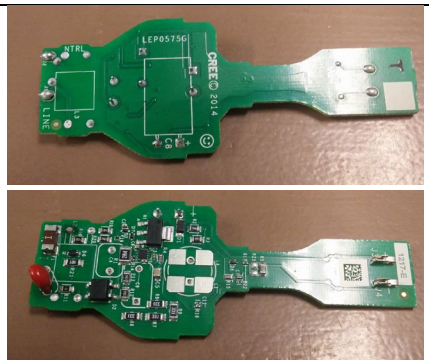
- The TL-UPQC can provide voltage recovery for a long duration in the event of a voltage sag, in this case it is an under voltage, since the shunt converter transfers the energy to the dc link. Nevertheless, the TL-UPQC system cannot support the load for a power outage or interruption. As discussed in the state of art of Chapter 4, the dc link of the TL-UPQC can be further integrated with a battery or a DG unit through a third converter. The operation of a TL-UPQC system as a UPS in this case can be further analyzed and evaluated. In addition, if there's no power interruption, the DG unit can inject active and reactive power to the grid through the TL-UPQC. A novel battery/load management system in that case should be developed.
- A comparative study between various control schemes of reactive power sharing among modularized distributed TL-UPQC systems can be conducted. Droop control for a decentralized operation can be developed. The future integrated control methodologies trends are mainly concerned with energy management systems for smart grid application. It is recommended to further investigate this system for a distributed multi-agent system, in which cyber-security and converters self-fault monitoring should be further investigated and studied.

Appendix

A.1 Sunbeam LED driver

Reverse engineering technique has been done on the internal drivers of Cree, TCP and Sunbeam LED lamps. TABLE A- I shows the specifications, the adopted topology and the PCB of each lamp. Detailed schematic diagram of Sunbeam LED driver is shown in Figure A- 1.

TABLE A- I SPECIFICATIONS OF LED LAMPS UNDER STUDY

Sunbeam 30411617 • Buck topology • Dimmable • Controller IC: NCP1608 • 12W usage • 38V DC output	
TCP LED10A19OD27K • Buck topology • Dimmable • Controller IC: SSL 2108 • 10W usage • 42V DC output	
Cree BA19 08050OMF • Buck-Boost topology • Dimmable • Unknown controller IC • 9W usage • 220V DC output	

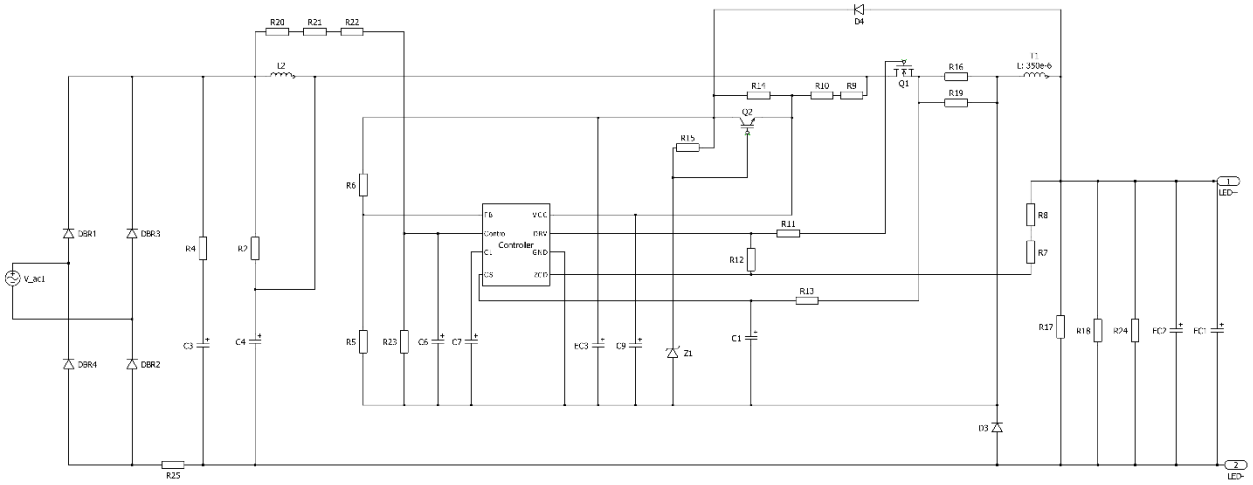


Figure A- 1. Schematic of Sunbeam LED driver.

A.2 Derivation of (4.10) – (4.13)

Criteria of switching S_3 = on and S_4 = off

Assuming at the hypothesized time instant t_1, the switches S_3 & S_4 turns on and off respectively as illustrated in Figure 4-9. During the time interval $t_1 \rightarrow t_3$, the inductor current $i_L(t)$, the capacitor current $i_C(t)$ and the capacitor voltage $v_A(t)$ can be expressed as follows,

$$\frac{di_L}{dt} = \frac{1}{L_A}\left(\frac{v_{DC}(t)}{2} - v_A(t)\right) \tag{A. 1}$$

$$i_C(t) = i_L(t) - i_O(t) \tag{A. 2}$$

$$v_A(t) = \frac{1}{C_A}\int i_C(t)dt \tag{A. 3}$$

While most of the inductor ripple will go through the capacitor, the output current $i_O(t)$ can be assumed to be constant during a small period of time. Therefore the following equation can be obtained,

$$\frac{di_C}{dt} = \frac{di_L}{dt} = \frac{1}{L_A}\left(\frac{v_{DC}(t)}{2} - v_A(t)\right) \quad \text{(A. 4)}$$

The capacitor current at the time instant t_2 can also be found as follows,

$$i_C(t_2) = \frac{di_C}{dt}.\Delta t + i_C(t_1) \quad \text{(A. 5)}$$

Substituting (A.4) in (A.5),

$$\Delta t = \frac{-L_A}{\left(\frac{v_{DC}(t)}{2} - v_A(t)\right)} i_C(t_1) \quad \text{(A. 6)}$$

According to (A.3) the minimum voltage across the capacitor can be expressed as follows,

$$v_{A,min} = \frac{1}{C_A}\int_{t_1}^{t_2} i_C(t)dt + v_A(t_1) \quad \text{(A. 7)}$$

It is clear from (A.7) that the integral of $\int_{t_1}^{t_2} i_C(t)dt$ is the area under the curve A_1as indicated in Figure 4-9. Based on (A.6), the capacitor voltage does not exceed its defined minimum value if criteria (4.10) and (4.11) are met.

Criteria of switching S_3 = off and S_4 = on

Similarly, at the hypothesized time instant t_3, the switches S_3 & S_4 turns off and on respectively as illustrated in Figure 4-9. In this case, during the time interval $t_3 \rightarrow t_5$, the following relation can be obtained,

$$\frac{di_C}{dt} = \frac{di_L}{dt} = \frac{1}{L_A}\left(\frac{-v_{DC}(t)}{2} - v_A(t)\right) \quad \text{(A. 8)}$$

The capacitor current at the time instant t_4 can also be found as follows,

$$i_C(t_4) = \frac{di_C}{dt}.\Delta t + i_C(t_3) \quad \text{(A. 9)}$$

$$\rightarrow \Delta t = \frac{L_A}{\left(\frac{v_{DC}(t)}{2} + v_A(t)\right)} i_C(t_3) \quad \text{(A. 10)}$$

The maximum voltage across the capacitor can be expressed as follows,

$$v_{A,max} = \frac{1}{C_A} \int_{t_3}^{t_4} i_C(t)dt + v_A(t_3) \quad \text{(A. 11)}$$

The integral of $\int_{t_3}^{t_4} i_C(t)dt$ is the area under the curve A_2 as indicated in Figure 4-9. Based on (A.10) and (A.11), the capacitor voltage does not exceed its defined maximum value if criteria (4.12) and (4.13) are met.

A.3 Derivation of (6.36)

The energy e_{DC} stored in the dc capacitors and the power flow of the capacitor p_{DC} in the steady-state are,

$$e_{DC}(t) = \frac{1}{2} \cdot \frac{C_{DC}}{2} v_{DC}^2(t) \quad \text{(A. 12)}$$

$$p_{DC}(t) = \frac{C_{DC}}{4} \frac{dv_{DC}^2(t)}{dt} \quad \text{(A. 13)}$$

By introducing small-signal perturbations into p_{DC} and v_{DC},

$$p_{DC}(t) = P_{DC} + \Delta p_{dc}(t) = \frac{C_{DC}}{4} \frac{d[V_{DC} + \Delta v_{dc}(t)]^2}{dt} \quad \text{(A. 14)}$$

$$\Delta p_{dc}(t) = \frac{C_{DC} V_{DC}}{2} \frac{d\Delta v_{dc}(t)}{dt} \quad \text{(A. 15)}$$

On the other hand the instantaneous ac power handled by the converter is,

$$p_{AC}(t) = v_G(t)(i_{PCC}(t) - i_O(t)) \quad \text{(A. 16)}$$

where,

$$i_{PCC}(t) = \sqrt{2}\, I_{PCC} \sin(\omega t - \delta \pm \theta) \quad \text{(A. 17)}$$

$$i_O(t) = \sqrt{2}\, I_O \sin(\omega t - \delta - \emptyset_O) \quad \text{(A. 18)}$$

Then,

$$p_{AC}(t) = P_{AC} + \Delta p_{dc}(t) = V_{PCC} I_{PCC}[\cos(\mp\theta) - \cos(2\omega t - 2\delta \pm \theta)]$$

$$-V_{PCC} I_O[\cos(\emptyset_O) - \cos(2\omega t - 2\delta - \emptyset_O)] \quad \text{(A. 19)}$$

Based on the energy conversion law,

$$p_{DC}(t) = p_{AC}(t) \quad \text{(A. 20)}$$

By combining (A.14), (A.19) and (A.20),

$$\Delta v_{dc}(t) = \frac{2\, V_{PCC}}{C_{DC} V_{DC}}[-I_{PCC} \int \cos(2\omega t - 2\delta \pm \theta)\, dt + I_O \int \cos(2\omega t - 2\delta - \emptyset_O)\, dt] \quad \text{(A. 21)}$$

$$\Delta v_{dc}(t) = \frac{V_{PCC}}{C_{DC} V_{DC} \omega}[-I_{PCC} \sin(2\omega t - 2\delta \pm \theta) + I_O \sin(2\omega t - 2\delta - \emptyset_O)] \quad \text{(A. 22)}$$

From (A.22), (6.36) can be obtained.

A.4 Derivation of (7.20)

The state-space matrices of the distributed TL-UPQC system including the feeder reactance can be found applying superposition for module *n.* The new set of state-space equations are described as follows,

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & \left(L_L + L_F^{(n)}\right) & -L_F^{(n)} \\ 0 & 0 & 0 & -L_F^{(n)} & \left(L_g + L_F^{(n)}\right) \end{bmatrix} \dot{x}(t) = \begin{bmatrix} 0 & -\frac{1}{C_P} & 0 & -\frac{1}{C_P} & \frac{1}{C_P} \\ \frac{1}{L_P} & 0 & \frac{1-2q_1(t)}{2L_P} & 0 & 0 \\ 0 & \frac{2q_1(t)-1}{C_{DC}} & 0 & 0 & 0 \\ 1 & 0 & 0 & -R_L & 0 \\ -1 & 0 & 0 & 0 & R_g \end{bmatrix} x(t) + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} u(t) \quad \text{(A. 23)}$$

and,

$$y(t) = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} x(t) \quad \text{(A. 24)}$$

where,

$$x(t) = \begin{bmatrix} v_B^{(n)}(t) \\ i_{PCC}^{(n)}(t) \\ v_{DC}^{(n)}(t) \\ i_L(t) \\ i_G(t) \end{bmatrix}, u(t) = v_G(t), y(t) = \begin{bmatrix} v_B^{(n)}(t) \\ v_{DC}^{(n)}(t) \end{bmatrix} \quad \text{(A. 25)}$$

$$q_1(t) = \begin{cases} 1 & S_1\ off, S_2\ on \\ 0 & S_1\ on, S_2\ off \end{cases} \quad \text{(A. 26)}$$

Small ac perturbations are introduced to the stat-space variables as follows, $v_B^{(n)} = V_B^{(n)} + \tilde{v}_b^{(n)}$, $i_{PCC}^{(n)} = I_{PCC}^{(n)} + \tilde{\imath}_{pcc}^{(n)}$, $v_{DC}^{(n)} = V_{DC}^{(n)} + \tilde{v}_{dc}^{(n)}$, $i_L = I_L + \tilde{\imath}_l$ and $i_G = I_G + \tilde{\imath}_g$. The small-signal equations can be obtained by neglecting the steady-state terms and transferred into the Laplace domain, from which the following can be derived,

$$\frac{\tilde{\imath}_g(s)}{\tilde{v}_b^{(n)}(s)} = T_G(s) = \frac{-L_L}{L_{eq}} \frac{s+\frac{R_L}{L_L}}{\left(s+\frac{R_L}{L_L+L_F^{(n)}}\right)\left(s+\frac{R_g}{L_g+L_F^{(n)}}\right)-\frac{L_F^{2(n)}}{L_{eq}}s^2} \quad \text{(A. 27)}$$

$$\frac{\tilde{\imath}_l(s)}{\tilde{v}_b^{(n)}(s)} = T_L(s) = \frac{L_g}{L_{eq}} \frac{s+\frac{R_g}{L_g}}{\left(s+\frac{R_L}{L_L+L_F^{(n)}}\right)\left(s+\frac{R_g}{L_g+L_F^{(n)}}\right)-\frac{L_F^{2(n)}}{L_{eq}}s^2} \quad \text{(A. 28)}$$

where,

$$L_{eq} = \left(L_L + L_F^{(n)}\right)\left(L_g + L_F^{(n)}\right) \quad \text{(A. 29)}$$

The perturbation in the PCC voltage $\tilde{v}_{pcc}$ due to reactive power injection of one module will be referred to as $\tilde{v}_m^{(n)}$ where,

$$\tilde{v}_{pcc} = \sum_{n=1}^{N} \tilde{v}_m^{(n)} \quad \text{(A. 30)}$$

And $\tilde{v}_m^{(n)}$ can be expressed as follows,

$$\tilde{v}_m^{(n)} = L_F^{(n)} s \left(\tilde{\imath}_g(s) - \tilde{\imath}_l(s)\right) + \tilde{v}_b^{(n)}(s) \quad \text{(A. 31)}$$

Substituting (A.27) and (A.28) into (A.31), the following can be obtained,

$$\frac{\tilde{v}_m^{(n)}(s)}{\tilde{v}_b^{(n)}(s)} = L_F^{(n)}[T_G(s) - T_L(s)]s + 1 \quad \text{(A. 32)}$$

In addition, the relation between the perturbation of the module's point of connection voltage $\tilde{v}_b^{(n)}$ due to the module's injected current $\tilde{\imath}_{pcc}^{(n)}$ can be expressed as follows,

$$\tilde{v}_b^{(n)} = \frac{1}{C_P s}(\tilde{\imath}_g(s) - \tilde{\imath}_l(s) - \tilde{\imath}_{pcc}^{(n)}) \quad \text{(A. 33)}$$

$$\frac{\tilde{\imath}_{pcc}^{(n)}(s)}{\tilde{v}_b^{(n)}(s)} = T_G(s) - T_L(s) - C_P s \quad \text{(A. 34)}$$

From (A.32) and (A.34), expression (7.20) can be found.

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