SWITCH-MODE POWER AMPLIFIERS WITH FAST-DYNAMIC CHARACTERISTICS FOR DC SOURCE EMULATION IN MICROGRID TESTBEDS

by

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A thesis submitted to the Faculty of Graduate Studies of

the University of Manitoba

in partial fulfillment of the requirements of the degree of

DOCTOR OF PHILOSOPHY

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Abstract

Recent development in microgrids (MGs) has led to rigorous testing of power electronic interface converters, ensuring their seamless integration into the power grid or used as an off-grid alternative. In photovoltaic (PV)-based MG testbeds, DC source emulators are established as a replacement for their real counterparts as they avoid the hassle of setting up bulky, expensive and uncontrollable testing environment. Meanwhile, DC source emulators based on switch-mode power amplifiers (PAs) have attracted a great deal of attention for their low cost, high efficiency and high power density over linear PA-based emulators on complete hardware testbeds or power hardware-in-the-loop (PHIL) simulations. However, switch-mode PA has much slower dynamic response time compared to linear PAs. It is essential to have a high-bandwidth PA in a DC source emulator, like a PV emulator, to replicate the actual dynamic source characteristics and test fast load converters and also in PHIL simulations for better accuracy and stability.

This thesis develops fast-dynamic switch-mode PAs for DC source emulation through the application of non-linear boundary control (BC). Firstly, this research studies the shortcomings in second-order BC schemes for buck derived converters cascaded to capacitive loads and non-linear switching converters and proposes a BC with a corrected second-order switching surface for buck-derived PAs to overcome the loading capacitor effect. The proposed voltage-mode PA is applied to develop a fast-dynamic standalone PV emulator for testing boost-derived PV converters with fast MPPT algorithms. A novel instantaneous output impedance matching controller is introduced to generate a stable and fast convergent reference signal in PV emulators regardless of the operating region in the I-V curve. Secondly, this thesis

proposes voltage-mode and current-mode switch-mode PA designs based on a synchronous buck converter with a two-stage LC filter to maintain the boundary-controlled PA performance under all types of non-linear switching loads. Results show that proposed PAs guarantee fast-dynamic characteristics without increasing switching frequency and maintain system performance under non-linear switching loads. The thesis also presents the comprehensive design and implementation of a PHIL-based PV emulator with the proposed current-mode PA.

Moreover, PHIL testbeds that incorporate two source emulators are introduced to evaluate DC-coupled PV-battery energy storage system (BESS) converters and grid-connected electric vehicle (EV) battery chargers. Mathematical frameworks to describe small-signal dynamics and analyze the stability and accuracy of PHIL setups are presented in this thesis. All DC source emulator designs are validated via experimental prototypes, and results agree well with the theoretical studies.

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- **I. Jayawardana**, C. N. M. Ho, and M. Pokharel, "Design, Implementation and Stability Analysis of a Switch-mode PV Emulator using Power-HIL Simulation," in *IEEE Transactions on Industry Applications*, (to be submitted).
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Acknowledgements

First and foremost, I would like to express my sincere gratitude to my supervisor Dr. Carl Ho for his insightful guidance, motivation and endless support throughout my doctoral program. I am forever grateful to Dr. Ho for giving me an opportunity to join the Renewable Energy Interface and Grid Automation (RIGA) lab and creating a professional research environment. I feel proud to be part of his team. And I learned immensely from his research attitude, work ethics and knowledge of power electronics, and I'll always be indebted to him for that. I am also very much thankful for my advisory and examining committee, Dr. Athula Rajapakse and Dr. Yang Wang, and my external examiner, for their valuable suggestions and comments to improve the quality of this work.

I want to thank my friends in the RIGA lab and power system research group for fruitful discussions and simply for making my life balanced at the university. I especially like to thank Dr. Mandip Pokharel, Dr. Radwa Abdalaal and Avishek Ghosh for spending time with me to discuss technical matters and providing me with their valuable advice on different practical issues. I also would like to acknowledge Dr. Dong Li, Dr. Ken Siu, Yanming Xu, Yang Zhou, Zhuang Zhang, Hafis Umar-Lawal, Garry Bistyak, Kasun Samarawickrama, Dr. Akbo Rupasinghe and Sachintha Kariayawasam for making my PhD journey fun and memorable. I also appreciate Dr. Yuanbin He for providing me technical feedback and sharing his knowledge.

I like to thank Dr. Aniruddha Gole, Dr. Udaya Annkage and Dr. Shaahin Filizadeh for the invaluable knowledge they shared during the course works. I would also like to thank all supporting staff, especially Erwin Dirks, Shrimal Koruwage, Oleg Shevchenko, Amy Dario, Traci Gledhill, and Heather Katrick, for their timely assistance. I also greatly appreciate the financial support received from University of Manitoba and Natural Science and Engineering Research Council.

In a personal note, I am always grateful for my lovely better half, Ruu, for her patience, love and support to keep me upright and motivated during hard times. She worked hard and sacrificed a ton for me, and I am truly thankful for that. Lastly, I would like to thank my loving parents and my dearest brothers for brought me up this far and encouraging me to pursue my goals.

Dedication

To my loving Amma, Thaththa and Ruu!

Table of Contents

List of Tables

List of Figures

Nomenclature

List of Symbols

σ^2	Boundary control with second-order switching surface
σ_{cor}^2	Boundary control with corrected second-order switching surface
I_{PH}	Photocurrent generated by the incidence of irradiation on the solar cell
I_{on}	Reverse saturation current of the diode in the PV cell
a	Diode ideality constant in the PV cell model
R_S	Structural resistance in the PV cell model
R_P	Leakage effect of the solar cell semiconductor material in the PV cell
V_t	Thermal voltage of the PV cell
k	Boltzmann constant
q	Magnitude of an electron charge
T	Temperature
G	Irradiance
N_{cs}, N_{cp}	Series-and-parallel connected PV modules in a PV array
V_{oc}, I_{sc}	Open-circuit voltage and short-circuit current of the PV module
V_{mp}, I_{mp}	Voltage and current at maximum power point of the PV module
G	Irradiance
Δ	Reference voltage band
C	Capacitance of the single-stage LC filter
L	Inductance of the single-stage LC filter

v_S	Input voltage of the power conversion stage or buck-derived converter
i_O	Output current of the PV emulator
i_C	Capacitor current of the single-stage LC filter
i_L	Inductor current of the single-stage LC filter
R_L, R	Load resistance
Δi_L	Change in or peak-to-peak ripple of the inductor current
Δi_C	Change in or peak-to-peak ripple of the inductor current
k_1	BC switching criteria gain during Switch ON
k_2	BC switching criteria gain during Switch OFF
v_{ref}, v_{Oref}	Reference voltage for the power amplifier
${\sigma^2}_{\Delta+}$	Second-order BC switching surface at the upper boundary
${\sigma^2}_{\Delta-}$	Second-order BC switching surface at the lower boundary
C_L	Capacitance of the input filter of the load converter
L_B	Boost-stage inductance
i_{LB}	Boost-stage inductor current
$\Delta_{C,m}, \Delta_m$	Measured peak-to-peak voltage ripple of v_C
k_D	Switching criteria gains of σ_{cor}^2 due to loading capacitance
S_1, S_2	Switching signals
f_{S2}	Switching frequency of load boost converter
$v_{C,max}$	Upper boundary of v_C
$v_{C,min}$	Lower boundary of v_C
i_{LH}	AC signal of i_L
f_S	Switching frequency

d	Duty ratio
T_S	Switching time period of the system
K_P, K_I	Proportional and integral gain of the voltage ripple feedback loop
L',C'	Inductance and capacitance after deviations
α, β	Tolerances of L and C
$v_{C,Avg}$	Average output voltage
v_{ripple}	Output voltage ripple
k_D'	Switching criteria gains of σ_{cor}^2 due to all filter parameter variations
$Msps$	Mega Samples per second
$R//C$	Resistive-capacitive parallel load
i_R	Current corresponds to the load line in IOIM controller
i_{Oref}	Current corresponds to PV model in IOIM controller
k_i	Integral gain of the IOIM controller
Δi_{Lmax}	Maximum peak-to-peak inductor current ripple
r_L	Variable load resistance in Section 4.3
g_{pv}	Partial derivative gain of the I-V curve at a given operating point
$f_{S_{PI}}$	Switching frequency of the conventional PV emulator with PI control
k_{P1}, k_{I1}	Proportional and integral gain of PI controller in conventional PVE
v_{DC}	Output voltage of the load boost converter
k_{P2}, k_{I2}	Proportional and integral gain of PI controller in load boost converter
C_F	Capacitance of the second-stage LC filter
L_2	Second-stage inductor
K_C	Deadeat controller gain

$i_{O,ref}$	Current reference signal for current-mode PA
T_{S1}	Sample period of the deadbeat control loop
V_{pv}, I_{pv}	DC voltage and current of PV array at the linearization point
R_{eq}	Small-signal Thevenin equivalent resistance of the PV array
Z_L	Small-signal impedance of the DUT or load
T_{MCU}	Sampling period for reference signal in the microcontroller
T_{PA}	Input-to-output signal latency of the PA
G_{aaf}	Gain of the antialiasing filter
f_{aaf}	Cut-off frequency of antialiasing filter
$T_{RT}, \Delta t$	Simulation time step of real time simulation
T_{AI}	ADC conversion time delay of the analog input card
T_{AO}	DAC conversion time delay of the analog output card
T_{total}	Total latency of the PHIL interface
f_C	Cut-off of frequency of the voltage measurement feedback filter
E_{TFP}	Error function due to transfer function perturbation
W_0	weighting function for different accuracy levels for frequency range
r_{L2}	Equivalent series resistance of L_2
f_{res}	Resonance frequency of the second-stage LC filter
T_{disc}	simulation time-step in RTS
T_{sw}	Period of switching signal
E_{duty}	Upper limit for the absolute error of duty ratio
v_{Bat}	The BESS voltage from the real time battery model in RTS
v_B	Output voltage of battery emulator

i_B	Output current of the battery emulator
v_{Bref}	Voltage reference of the PA in PHIL-based BE
R_d	Parallel resistor at the DC power source output
P_{cmax}	Maximum power dissipation in R_d during the charging operation
v_{OC}	Open-circuit voltage of the battery model
R_S	Resistance responsible for the instantaneous voltage drop of step response in the battery model
R_{t_S}, C_{t_S}	Battery model RC values that account for short-term transients
R_{t_L}, C_{t_L}	Battery model RC values that account for long-term transients
r_C, r_L	ESR of the single-stage capacitor and inductor (BE PA)
Q	Battery capacity
SOC_{init}	Initial SOC level
Q	Battery capacity
v_{bat}, i_{bat}	Voltage and current of a single Li-ion battery model
N_s, N_p	Series-and-parallel connected batteries in a BESS
v_{Bat}, i_{Bat}	Voltage and current of a BESS
$Z_{b,eq}$	Small signal equivalent impedance of the BESS
Z_{DUT}	Closed-loop output/input impedance
Z_{outCL}	Closed-loop output impedance of the load converter during charging
Z_{inCL}	Closed-loop input impedance of the load converter during discharging
R_e	Small-signal load resistance when EV battery charger in CV mode
k_P, k_I	Proportional and integral gain of PI controller in BE PA

G_M	PWM scheme gain of PI controller in BE PA
$H(s)$	Voltage sensor feedback gain in BE PA
Z_S	Equivalent grid impedance
R_g, L_g	Grid resistance and inducatnce
Z_{DUTac}	AC side input impedance of the EV battery charger
T_b	Latency of linear PA
T_a	Cut-off of linear PA
T_{cp}	Time constant of the lead compensator
T_{fil}	Filter cut-off of the current feedback signal
$\Delta x, \tilde{x}$	Small-signal term of any given variable x

List of Abbreviations

AAF	Antialiasing Filter
AC	Alternative Current
ADC	Analogue to Digital Converter
AO	Analogue Output
AI	Analogue Input
BC	Boundary Control
BE	Battery Emulator
BES	Battery Energy Storage
BESS	Battery Energy Storage System
CC	Constant Current
CM	Current Mode

CCM	Continuous Conduction Mode
CCR	Constant Current Region
CLA	Control Law Accelerator
CPL	Constant Power Load
CPU	Central Processing Unit
CV	Constant Voltage
CVR	Constant Voltage Region
DAC	Digital to Analogue Converter
DC	Direct Current
DCM	Discontinuous Conduction Mode
DIM	Damping Impedance Method
DRM	Direct Reference Method
DSP	Digital Signal Processors
DUT	Device Under Test
EA	Error Amplifier
ECM	Equivalent Circuit Model
EMT	Electro Magnetic Transient
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FPGA	Field Programmable Gate Arrays
GaN	Gallium Nitride
GE	Grid Emulator
GTAO	Giga-Transceiver Analogue Output

GTAI	Giga-Transceiver Analogue Input
G2V	Grid-to-Vehicle
HPF	High Pass Filter
IA	Interface Algorithm
I-V	Current vs Voltage
ISR	Interrupt Service Routine
ITM	Ideal Transformer Method
LC	Inductor and Capacitor
LPF	Low Pass Filter
LV	Low Voltage
LUT	Look Up Table
MG	Microgrid
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NSS	Natural Switching Surface
PA	Power Amplifier
PCS	Power Conversion Stage
PE	Power Electronic
PHIL	Power Hardware in the Loop
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PQ	Power Quality
PU	Power Unit

PV	Photovoltaic
PVE	PV Emulator
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RGA	Reference Generation Algorithm
RT	Real time
RTS	Real Time Simulator
R-H	Routh-Hurwitz
SiC	Silicon Carbide
SMC	Sliding Mode Control
SMI	Solar Micro-Inverter
SOC	State of Charge
SOSM	Second-order Sliding Mode
STC	Standard Test Conditions
TF	Transfer Function
TFP	Transfer Function Perturbation
VM	Voltage Mode
V-I	Voltage vs Current
V2G	Vehicle-to-Grid
ZOH	Zero Order Hold

Chapter 1

Introduction

1.1. Background

Renewables have provided a greater share of electricity generation in the global electricity mix over the past decade as a result of technological advancements, lower manufacturing cost and their impact against climate change. Among renewables, solar photovoltaic (PV) is now an established option for both utility-scale and small-scale renewable generation [1]. Due to their intermittent nature, PV generation systems often require battery energy storage (BES) systems. Along with advancements in PV-BES systems, microgrid (MG) concepts have evolved as an efficient way of utilizing renewable energy sources, which integrate distributed generation, energy storage and loads with local control schemes [2]-[4]. Figure 1.1 shows a simplified diagram of a flexible microgrid structure suitable for remote power supply and future smart grids [4]. Power electronic (PE) converters are required to interface various microgrid components and achieve power conversion, power flow control and voltage regulation. Developing such complex MGs involves conducting studies and rigorous testing before their installation to achieve high energy efficiency and reliable power supply. Moreover, studies need to be performed to develop advanced PE interface converters,

evaluate their impact on the power system's stability and investigate issues related to power quality (PQ), harmonic current generation and propagation, islanding of distributed sources and many more [5].

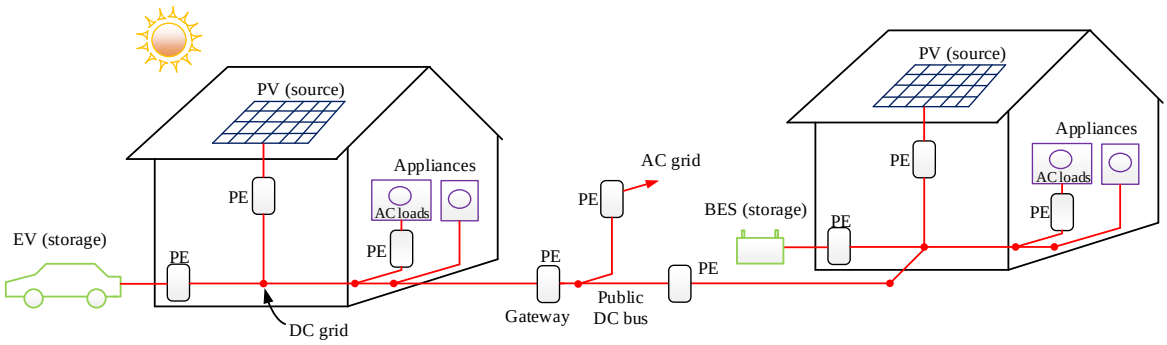


Figure 1.1 Conceptual structure of a microgrid system with PE converters.

Research and development studies related to PV-BES systems are more often achieved using appropriate simulation tools [1], [6]. However, the validity of the simulation-based studies significantly relies on the accuracy of PE converter models [6]. Thus, in some cases, simulation-based conclusions are validated via experiments by installing a prototype system and carrying out lab or field tests. Implementing a test setup with actual PV arrays and BES systems (BESS) for system studies is costly, time consuming and requires a larger space. Moreover, the output current-voltage (I-V) characteristics of a PV cell depend on environmental conditions like solar irradiation level and atmospheric temperature [7]. Hence, it is not feasible to maintain a controllable testing environment with these real DC sources (PV arrays, BESS). To overcome these challenges, PV and battery emulators that mimic the response of solar PV arrays and BESS have been developed [8]-[11]. These standalone DC source emulators offer flexible and reproducible test conditions with lesser cost and shorter setup time than real sources. Consequently, they have become an essential device among power and energy researchers as a tool to conduct experiments.

Basic structure of DC source emulator consists of three elements: power conversion stage (PCS), inner control system and outer reference generation algorithm (RGA) [12]. Figure 1.2 summarizes the different classifications of DC source emulators based on those three elements considering both PV and battery emulators. In the PV emulator (PVE), the PCS is controlled based on the reference signal generated through a PV model to imitate the I-V characteristics of a real PV array at a given irradiance and temperature. External load characteristics determine the operating point on the I-V curve. Same structure is used with a battery model to implement battery emulators (BEs). Battery is a non-linear voltage source, and its output voltage and output impedance rely on present operating conditions as well as how it was treated in the past. Thus, battery models are typically developed to provide the battery voltage as a function of the state of charge (SOC) or battery current at a specified temperature [13]. Also, the PCS of BE is operated in voltage-mode (VM) control and designed with a bidirectional PCS to ensure charging and discharging operation.

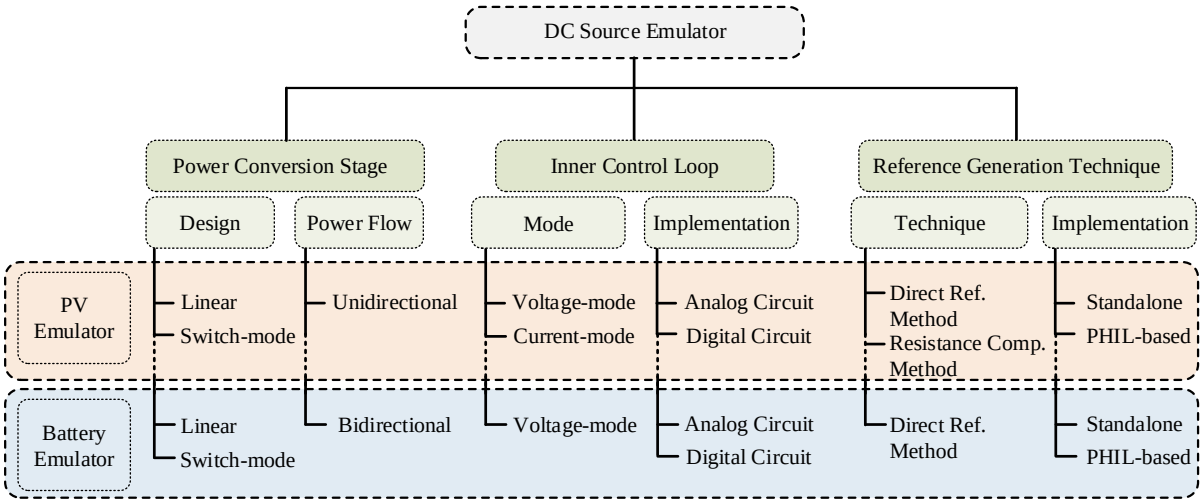


Figure 1.2 DC source emulator classification.

The PCS of the DC source emulator is designed either with a linear power amplifier (PA) [9], [14] or a switch-mode power amplifier [8], [15]-[18]. In the linear PA, semiconductor

switches operate in the linear region (e.g., class A, class B, class AB), whereas semiconductor devices in the switch-mode PA operated in either fully on or fully off states [19]. These differences in the operating principles lead to contrasting characteristics between the linear and switch-mode PAs, as listed in Table 1-1.

Table 1-1 Comparison of linear PA and switch-mode PA [20], [22]-[24].

Features	**Linear PA**	**Switch-mode PA**
Power rating	Low (<25 kW)	High (kW to MW)
Bandwidth	High (>10 kHz)	Low (<3 kHz)
Response time	Short (in μs)	Long (in ms)
Power Efficiency	Low (40% - 60%)	High (~95%)
Cost Efficiency	Low	High
Size	Large	Small

The power rating of the linear PAs is limited due to high power loss and manufacturing complexity [20] whereas, with switch-mode PAs, power rating can go up from kW to a few MW with present semiconductor technology [21], [22]. Linear PA has higher bandwidth (> 10 kHz) and shorter response times (<~20 μs) than switch-mode PAs [23]-[26]. Thus, linear PA is well suited for source emulators that require fast-dynamic characteristics. However, linear PA's use is often limited due to low efficiency, low power density and high cost [22]-[24]. In MG testbeds, switch-mode PA-based DC source emulators have been extensively used for their advantages of low cost, high efficiency, high-power density and less complexity in manufacturing [20], [22]-[24]. Typical topologies of switch-mode PA-based DC source emulators are the non-isolated buck derived topologies such as DC-DC buck converter [15], [16], synchronous DC-DC buck converter [17], [18], full bridge inverter [27] for their

advantages in implementation and cost. The limitation of the switch-mode PA mainly lies in dynamic response characteristics that primarily depend on the control algorithm, switching frequency and filter parameters. These aspects should be correctly engineered to overcome the challenge of slow response in switch-mode PAs. Figure 1.3 shows the basic system configuration of a conventional voltage-mode source emulator with a switch-mode PA.

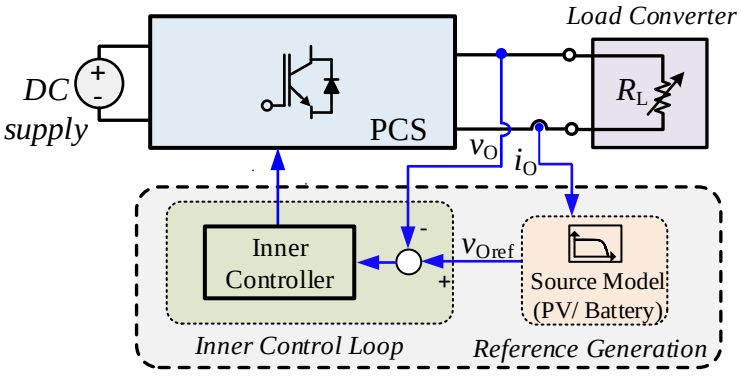


Figure 1.3 Conventional VM source emulator configuration with a switch-mode PA.

The control scheme of the source emulator is comprised of two stages, namely: the inner control loop and outer reference generation algorithm loop. The inner control loop regulates the output voltage/ current of the PA at a given reference. Classical linear controllers (i.e. proportional-integral (PI), proportional-integral-derivative (PID) are commonly used in standalone PV and battery emulators to regulate it in either current-mode (CM) or voltage-mode [28]-[30]. The issue of applying a linear controller for switch-mode PA is that it has a low bandwidth-to-switching frequency ratio [31]. As a result, the switch-mode PA needs to operate with a much higher switching frequency to achieve high control bandwidth and fast dynamic response, leading to high switching losses and more heat-sink requirements. To accomplish fast-dynamic characteristics, a fast control method is required for switch-mode DC source emulators.

In the RGA loop, the reference signal is generated according to a source model based on measured load information (i.e., output voltage or current of the PA or load resistance). Accuracy of the source emulator relies on the accuracy of the PV or battery model, while the speed of the RGA will depend on the implementation technique. Significant research effort has been put into developing PV and battery models to characterize the steady-state and dynamic electrical behavior of solar PV cells [32] and batteries [13]. The most common RGA implementation strategy can be defined as the direct reference method (DRM), in which load side current is measured and fed into a source model to calculate the voltage reference directly. The same logic has been implemented by measuring load side voltage and generating current reference for the inner loop. Particularly with PV emulators, DRM creates an oscillatory reference signal in one region of operation (i.e., in constant voltage region (CVR) with current-mode control and constant current region (CCR) with voltage-mode control) due to the nature of I-V characteristics and ac ripple of the feedback signal [29]. Thus, stable operation of PV emulators in both CCR and CVR with DRM is challenging. Alternatively, dual-mode control methods with two separate direct referencing blocks [28], [29], and resistance comparison methods that use the load resistance as the feedback signal [8], [33], are used as the RGA to resolve oscillatory reference signal problem in PV emulators. In battery emulators, only DRM with current feedback is employed to generate voltage reference for the inner loop as it provides stable operation.

Apart from standalone source emulators, DC source emulation through power hardware-in-the-loop (PHIL) simulations is steadily getting popular with the advancement of real time simulators (RTSs) and its extensive usage in grid integration studies [34], [35]. The PHIL technique is a semi-simulation setup that decouples the original circuit using a power interface

as such a part of the circuit is being simulated inside the RTS, and the rest of the circuit is completed with an actual device under test (DUT). Thus, PHIL setup can emulate a physical environment via the power interface to evaluate real power apparatus. Signal exchange between RTS and DUT is determined by an interface algorithm (IA) [36]. The power interface consists of PA, analog-digital converter (ADC), digital-to-analog converter (DAC) and sensor. The power amplifier is employed to amplify the signal sent from the RTS and emulate the behavior of the simulated circuit. The real power is exchanged between the PA and DUT.

Typically, PHIL simulations are applied in experimental testbeds where complete hardware implementations are very expensive and perhaps not even feasible to reproduce under full experimental setups, like DC MG developments. Figure 1.4 shows a typical PHIL test configuration with a maximum power point tracking (MPPT) PV inverter, in which the PV inverter is interfaced to the simulated power system network in RTS through a power interface [37], [38]. Here, the PHIL simulation is applied to operate the AC side PA as a grid emulator (GE). This setup allows testing and validating both the physical PE converters and the system they operate ((i.e., power grid or MG) with several attractive features such as reduced cost, less time, scalability, repeatability, flexibility and perhaps most notably with low-risk testing. Like AC grid emulator, PHIL simulation can be applied to emulate DC source behavior creating fully power electronics-based PHIL platform with both DC source and power grid emulation and enabling power cycling to enhance burn-in test efficiency [39].

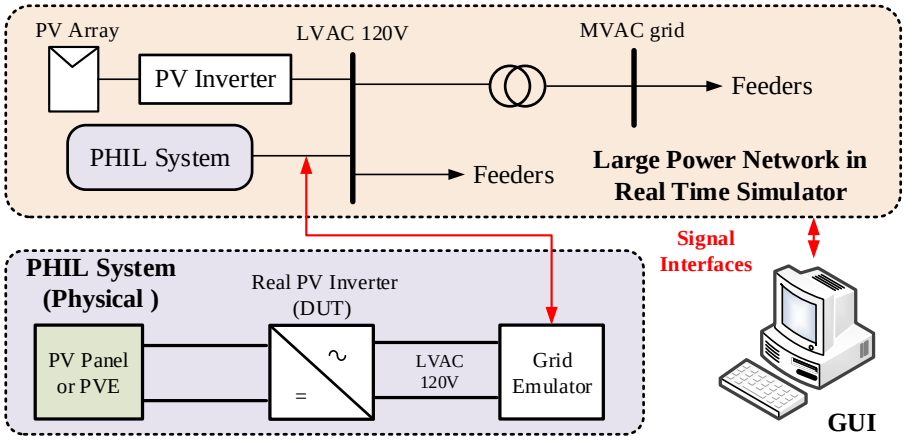


Figure 1.4 Typical PHIL test configuration for PV grid integration studies [37], [38].

A DC source emulator based on PHIL simulation is achieved by integrating the source model in RTS (i.e., PV model, battery model) with the power interface. In this way, the PA in the power interface can be configured to emulate nonlinear sources such as AC or DC grid, PV array and BESS [35], [40]-[43]. Unlike a standalone DC source emulator with all the associated controls attached to the PA, the PHIL-based DC source emulator utilizes a PV model developed in RTS to generate the reference signal for the PA. This PHIL-based approach provides enhanced controllability and flexibility than standalone DC source emulators. Also, it takes advantage of the PHIL grid integration setup since high-performing RTS is already in place. The critical problem with PHIL simulations is that the components involved in the power interface introduce time delays and limited bandwidth that do not exist in the original circuit, significantly impacting the accuracy and stability of PHIL simulations [36]. Hence, having a high-bandwidth PA is vital to reduce time delays within the loop and achieve a stable and accurate PHIL simulation for DC source emulation [44]. Also, it is crucial to develop the PHIL system model, including all the interface components, to determine the stability and accuracy of the PHIL setup before real PHIL tests.

1.2. Research Motivation

Switch-mode PA-based DC source emulators have gained attention for their low cost, high efficiency and high-power density than linear PA-based emulators in testing PE interface converters via complete hardware testbeds or PHIL simulations. However, as described in the previous section, switch-mode PA has a much slower dynamic response time compared to linear PAs. Meanwhile, in PHIL simulations, it is essential to have a high-bandwidth PA to increase the accuracy and stability, as described in the previous section.

Moreover, in source emulation, the dynamic performance is a critical parameter, particularly for PVEs to replicate dynamic characteristics close to real PV arrays and test fast MPPT converters. Firstly, real PV modules exhibit fast dynamic response and have proven to reach the steady-state within few microseconds to tens of microseconds for sudden transients [18]. Dynamic characteristics of an actual PV module are mainly governed by the RC filter formed by the load resistance and inherent source capacitance which represents the diffusion effect of PV cells [45]. Thus, PV emulators should be designed with fast dynamic characteristics as a DC source emulator to replicate dynamic characteristics close to real PV arrays. In comparison to PVEs, BE has less demand for transient responses as real BESS takes few seconds to reach steady for sudden transient unless battery emulator is opting to emulate transient characteristics as well [47]. Secondly, the tracking speed of MPPT converters has been improved significantly, targeting to improve the extraction efficiency and minimize errors of applications that go through rapidly changing irradiance conditions and large-scale applications [48],[49]. To maintain the dynamic stability of the cascaded system composed of source and load converter, the control bandwidth of the source converter should be higher than that of the load converter when the output impedance of the source converter is intersected

with the output impedance of the load converter [50], [51]. Therefore, it is also necessary to have a high bandwidth source emulator to avoid such problems and test tightly regulated load converters.

These aforementioned factors motivated this research to investigate possible switch-mode PA solutions with fast-dynamic characteristics for DC source emulators like PVEs and develop PHIL-based DC source emulators using fast-dynamic switch-mode PAs to ensure stable and accurate PHIL simulation.

1.3. Problem Statements

Although standalone or PHIL-based DC source emulators based on switch-mode PAs are extensively employed in testbeds, the limitation of switch-mode PA in achieving fast-dynamic response should be first addressed. The dynamic performance of a switch-mode PA is primarily dependent on the control algorithm. Mostly linear PI controllers are used in switch-mode PAs and however, as highlighted in Section 1.1, linear controllers have a shortcoming in achieving faster response. Also, applying a linear controller to regulate the source converter in cascaded DC-DC configuration would require additional passive [52] or active damping [53] method to mitigate constant power load (CPL) instability issue [50], [51] which arises due to negative impedance characteristics of the tightly regulated load converter.

Alternatively, large signal-based boundary control (BC) methods are used to achieve high control bandwidth and robust and stable operation compared to linear pulse-width modulated control schemes [54]-[61]. Among BC methods, BC with curved switching surfaces, such as second-order switching surface [56]-[58], and natural switching surface (NSS) [59]-[61], can provide a near-optimal response for large signal disturbances. Yet, the

system performance of boundary-controlled converters is significantly affected when connected to a second-stage converter with a large input capacitor. Existence of a parallel capacitor of the second-stage/load converter and the current ripple components generated due to the switching actions of the second-stage converter would create a discrepancy between BC control law and real converter, resulting in incorrect switching actions. This is a common problem in cascaded DC-DC converter systems where source converter control relies on capacitor current measurement and filter parameters and often abundant in the existing literature. Examples of such control methods are sliding mode control (SMC) [54], natural switching surface [59] and BC with second-order switching surface (σ^2) [56]. Hence, a detailed investigation is required before adopting such fast-dynamic non-linear BC methods for source emulators such as PVEs and BEs.

Another critical design aspect of the source emulator is the RGA, which significantly affects the accuracy and response time of the system. Accuracy of the source emulator relies on the accuracy of the PV or battery model, while the speed of the RGA will depend on the implementation technique. Significant research effort has been put into developing PV and battery models to characterize the steady-state and dynamic electrical behavior of solar PV panels and batteries. However, particularly in standalone PVEs, the oscillatory reference signal with DRM limits its ability to emulate the entire I-V curve. Further, with DRM, the reference generation loop is coupled with the inner control loop, limiting the response time of the reference signal by the inner loop bandwidth. Therefore, a universal RGA is required for standalone PVEs to generate a stable reference signal in both CCR and CVR of the I-V characteristics curve while preserving fast convergent speed.

As described in Section 1.1, PHIL simulation has been adopted for emulation of PV arrays and BESS to examine respective interconnected systems [35], [40]-[43]. Although the PHIL concepts are well known and analyzed in general, particularly the implementation, modelling, and stability analysis of PHIL-based PVE or BE via an IA have not been sufficiently addressed in the literature. Further, the existing stability and accuracy studies of a switch-mode PA interface for PHIL simulations are mostly developed with small-signal models derived considering a standard resistive divider network [36], [37], [44], [62]. Therefore, it is necessary to derive a comprehensive small-signal model of the PHIL-based source emulator, including the virtual source model and power interface, and develop a mathematical framework to analyze stability and accuracy under different operating conditions.

The problems mentioned above are the key limitations identified related to the PV and battery emulators. Thus, the work done in this thesis is intended to address those problems to improve the accuracy and dynamic performance of DC source emulators and enhance their implementation through PHIL simulations. Moreover, in this thesis, the switch-mode DC source emulator primarily focuses on emulating PV arrays since PV demands a fast dynamic response as a DC source emulator than other DC sources such as BESS and fuel cells [18].

1.4. Research Objectives

This thesis is focused on topology and advanced controls of switch-mode DC emulators suitable for PV arrays and BESS to ensure their applicability in testing fast PE converters and enhance their implementation via PHIL simulations. The ultimate goal of this thesis is to develop switch-mode DC source emulators with fast-dynamic characteristics for microgrid testbeds. The specific research objectives pursued are listed below;

- Detailed review on state-of-the-art standalone PV emulators to identify their limitations on fast dynamic response.
- Employ BC with second-order switching surface method in buck-derived switch-mode PA to achieve ultra-fast response time and robust operation.
    - Review and study shortcomings of conventional σ^2 method for buck derived converters cascaded to capacitive loads and non-linear switching converters.
    - Derive a non-linear BC scheme for buck-derived converters to overcome limitations with capacitive and non-linear switching loads and operate within specified control parameters. Also, develop a voltage-mode switch-mode PA using the derived BC scheme to achieve fast dynamic characteristics.
- Develop a universal RGA for PVEs based on output impedance measurement to suppress the oscillatory reference signal, ensuring good performance over the entire I-V curve.
- Develop a fast-dynamic switch-mode PV emulator by incorporating the proposed BC scheme and RGA and validate its performance with MPPT PV converters.
- Employ a non-linear cascade controller and develop a current-mode switch-mode PA with fast-dynamic characteristics to minimize PHIL power interface latency.
- Develop a PHIL-based PVE with proposed current-mode PA for conducting burn-in tests with enhanced flexibility. And study stability and accuracy of the PHIL-based PVE by deriving the comprehensive small-signal model.
- Develop a PHIL testbed with proposed fast-dynamic switch-mode PAs to emulate PV array and DC grid response, including the real-time converter models of PV-BESS for testing a DC-coupled PV-BES converter.

- Design and validate a PHIL testbed consisting of a PHIL-based battery emulator and a grid emulator to mimic the DC side battery and the AC side low-voltage (LV) grid behavior to evaluate grid-connected electric vehicle (EV) chargers. Also, develop a mathematical framework to analyze the stability and predict the accuracy of both PHIL-based emulators.

1.5. Research Strategy

The ultimate goal of this research is to develop a DC microgrid testbed composed of PV, battery, and DC grid emulators to test PE converters and conduct system-level studies. Thus, this thesis introduces designs of voltage-mode and current-mode switch-mode PA for DC source emulation in standalone or via PHIL simulations. Figure 1.5 summarizes the conceptual DC microgrid testbed structure considered in this thesis with proposed DC source emulators.

This thesis first studies shortcomings of applying second-order BC methods for switch-mode PAs and proposes a BC with corrected second-order switching surface (σ_{cor}^2) for buck-derived switch-mode PAs to achieve fast-dynamic response and maintain system performance even under loading capacitor effect of switching load converters. The proposed σ_{cor}^2 is applied to develop a voltage-mode standalone PV emulator together with a novel instantaneous output impedance matching (IOIM) controller as the outer RGA. The proposed IOIM controller provides a stable reference signal in both CCR and CVR of the I-V characteristics curve and decouples the inner control loop response from the reference generation loop, allowing to design it independently. Design of σ_{cor}^2 and IOIM controllers are introduced in detail in Chapter 3 and Chapter 4 of this thesis, respectively.

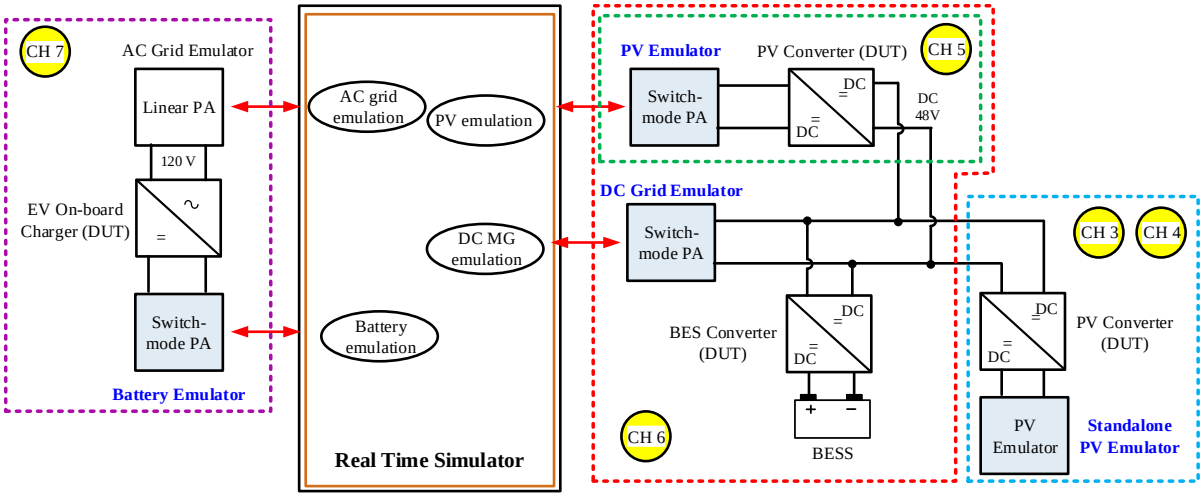


Figure 1.5 Conceptual DC microgrid testbed.

Second phase of the thesis focused on developing PHIL-based DC source emulators using fast-dynamic current-mode and voltage-mode PAs, including the stability analysis and accuracy prediction of PHIL simulation of PV arrays and BESS. A current-mode PA is proposed based on a synchronous buck converter with a two-stage LC filter to develop a PV emulator based on PHIL simulation. The control scheme of the current-mode PA employs a cascaded control scheme consists of an outer deadbeat controller and inner σ_{cor}^2. This topology and control architecture eliminates the effect of switching load converter on the source converter control while providing the fast current tracking capability. Chapter 5 will introduce detailed designs of the current-mode PA as well as the PHIL simulation setup for PV emulation. The voltage-mode PA for PHIL setup is realized by modifying the proposed σ_{cor}^2-controlled PA with a second-stage passive LC filter, which can also maintain the controller performance under all types of non-linear switching loads. The developed switch-mode PAs guarantee fast-dynamic characteristics through the application BC without increasing switching frequency, which is suitable for PHIL testbeds as it would minimize the interface latency.

To demonstrate the applicability of designed switch-mode PAs, an experimental PHIL testbed is developed with RTDS^{TM} real time simulator for evaluating DC-coupled PV-BESS converters, as shown in Figure 1.5. The PHIL testbed comprises a PHIL-based PVE and a PHIL-based DC grid emulator to mimic the PV array and DC grid response. Scalable DC MG is modelled in RSCAD, and the performance of a PV-BES converter prototype is tested by interfacing with the emulated DC MG in Chapter 6. This thesis also develops a PHIL testbed for evaluating grid-connected EV chargers, consisting of a PHIL-based battery emulator and a grid emulator to mimic the DC side battery and the AC side LV grid behavior, respectively. Design considerations for the PHIL-based battery emulator and mathematical framework to analyze the stability and predict the accuracy of both PHIL-based emulators are presented in Chapter 7. After all, the outcome of this research can be directly adapted by researchers, utilities, and vendors to develop a PHIL testbed capable of testing advanced PV-BES converters and EV chargers and conducting power system studies to investigate possible stability and power quality issues.

1.6. Outline of the Thesis

In total, this thesis consists of 8 chapters that are organized as follows;

Chapter 1 presented an introduction to the thesis topic. Limitations of switch-mode DC source emulators and the need for fast-dynamic characteristics for DC source emulators were explained. The problems related to both standalone and PHIL-based DC source emulators were highlighted. Main research goal and research objectives to address those limitations were described, and finally, contributions of this research work were summarized.

Chapter 2 provides a thorough literature review on key identified components that are important to conduct this research. It includes a literature review on PV emulators and their dynamic performance, battery emulators, PHIL simulation and nonlinear BC method.

Chapter 3 presents a BC scheme for buck-derived switch-mode PAs to maintain the output voltage even when cascaded to capacitive loads and achieve fast-dynamic characteristics. An outer control loop based on voltage ripple feedback is introduced to generate the corresponding switching criteria gain factor of σ_{cor}^2 that accounts for any mismatches due to unknown load capacitance or filter parameter deviations. The detailed derivation and implementation of the σ_{cor}^2, and design procedure of the outer feedback loop are provided in this chapter, including simulation and experimental validations. Also, proposed σ_{cor}^2 method's applicability in DC source emulator applications and limitations are discussed.

In Chapter 4, a fast-dynamic standalone PVE is developed by employing the σ_{cor}^2-controlled voltage-mode PA proposed in Chapter 3 with a novel IOIM controller as the RGA to evaluate high-bandwidth MPPT converters. The IOIM controller suppresses the oscillatory reference signal problem, providing a stable and fast convergent reference signal in all regions of the I-V curve. The small-signal model of the PVE is derived to design the IOIM controller and prove that the RGA is decoupled from the inner control loop response.

Chapter 5 focuses on the design and implementation of a PHIL-based PVE using a fast-dynamic current-mode PA. The voltage-mode PA proposed in Chapter 3 is extended to a current-mode PA by modifying the topology and control architecture to maintain PA performance under all types of nonlinear switching converter loads while guaranteeing high-control bandwidth. The switch-mode PA design has been discussed in detail. Also, the stability

of the PHIL-based PVE is analysed by deriving the comprehensive small-signal model. Experiment results are provided to verify the theoretical analysis.

In Chapter 6, a PHIL testbed for evaluating DC-coupled PV-BESS converters is developed by combining the PHIL-based PVE proposed in Chapter 5 and a PHIL-based DC grid emulator based on fast-dynamic voltage-mode PA. For the PHIL-based DC grid emulator, the VM PA proposed in Chapter 3 is modified by adding a second-stage passive LC filter to decouple the load converter dynamics on the PA performance. Design considerations of the VM PA to maintain an accurate output voltage and retain fast dynamics are described. Scalable DC MG with PV-BESS converters is modelled in RSCAD, and modelling of DC-DC converters for real time application is discussed. Experimental performance of the PHIL testbed with a PV-BES converter prototype is presented to demonstrate the application of the platform.

Chapter 7 presents a comprehensive study and validation of a PHIL testbed for testing grid-connected EV chargers. The testbed consists of a PHIL-based BE and PHIL-based grid emulator to mimic the DC side battery and AC side LV grid behavior. The main focus of this work is to derive the comprehensive small-signal model of the PHIL testbed for stability and accuracy analysis and validate developed models and theoretical predictions through experiments.

Chapter 8 concludes this thesis by summarizing the work presented and their contributions and suggesting recommendations for future work.

Chapter 2

Literature Review on Fast-dynamic DC Source Emulation

2.1. Introduction

With the rapid advancement in research and development of renewable and clean energy-based systems, DC source emulators have become an essential tool for testing downstream PE converters than using their real counterparts. Main DC sources involved with renewable and clean energy-based systems are solar PV, battery power and fuel cell energy. Principle operation of the DC source emulator is to mimic the static and dynamic characteristics of a given DC source model. Hence, the dynamic performance of the DC source emulator is a critical design parameter to replicate real DC source performance. And dynamic characteristics of those DC sources vary to one another. Typically, PV arrays respond ultra-fast for sudden transients than other DC sources [18],[45] and have the most critical demand for transient responses as a DC source emulator, as highlighted in Chapter 1. If the DC source emulator is designed for PV emulation, it will be capable of emulating any other DC source after proper adjustments. Therefore, this thesis primarily focused on PV emulator technology.

In this chapter, a detailed literature review on switch-mode PVE emulators is presented. Moreover, this thesis aims to develop fast-dynamic DC source emulators with the application of nonlinear boundary controllers. Therefore, in this chapter, a review of nonlinear BC methods is also presented to understand the large-signal control concept and identify its shortcomings. Further, to meet the other objectives of this research, knowledge of PHIL simulation and battery emulators is necessary. Hence, a literature review on those two areas is also presented in this chapter.

2.2. Photovoltaic Emulator

The PVE is a device capable of emulating the output characteristics of a real PV array with a capability of change in solar irradiation, temperature and any other PV cell parameters. Typically, PVE is composed of three main elements: PCS, inner control loop, and RGA.

2.2.1 Power Conversion Stage

The PCS of PVEs is realized using either a linear power stage [9], [14], [63], or a switch-mode power stage [8], [12], [15]-[17]. The PVEs with linear PCS offer exceptional dynamic performance but are often limited to low power applications due to their low efficiency, low power density and high cost, as highlighted in Chapter 1. These drawbacks exert a significant influence on high-power applications where switch-mode PCS are preferred. Also, switch-mode-based PVEs are extensively used in MG testbeds in any power rating, mainly for their advantages in cost, efficiency, and size [20].

The switch-mode PCS of the PVE requires operating in buck mode to emulate the I-V characteristics curve effectively. Various non-isolated buck-derived topologies are presented for PVE application, includes conventional DC-DC buck converters [15], [16], synchronous

DC-DC buck converter [17], [18], DC-DC buck converter with two-stage LC filter [64], LLC resonant DC-DC converter [65], zero voltage zero current switching converter [66], full bridge DC-DC converter [67], two-quadrant DC-DC converter [30], and three-phase interleaved DC-DC buck converter with an active front end converter [68]. The two-stage LC filter provides a higher resonance frequency, allowing the control loop to have a higher control bandwidth with the same ripple attenuation.

The DC source for the switch-mode PCS is typically realized with a frond-end AC-DC converter with power factor correction (PFC), as done in [68]. Several PVEs based on switch-mode PCSs have presented a similar design compromised with two stages, in which the first stage is a full bridge diode rectifier [69] or a controlled ac-dc rectifier [68], [70], and the second stage with a buck-derived converter. The front-end converter enhances the portability of PVE and reduces cost in the overall test setups. However, the design and control of an active front-end converter for the DC source emulator have not been considered in the scope of this thesis. In summary, non-isolated conventional DC-DC buck converters are most commonly used to realize the main PCS of PVEs due to their simplicity in implementation and low cost.

2.2.2 Inner Control Loop

The inner control loop is implemented in either voltage-mode or current-mode control to regulate output voltage or output current based on the output of the reference signal generator. Current-mode controls are generally implemented with linear PI controllers [12], [66], [70]. In [71], an adaptive PI control method is used to achieve critically damped operation in a wide range of operating points. Also, a hysteresis current control method is employed in [17] to achieve fast dynamics. It requires operating with increased switching frequency or a large inductor to maintain a lower output current ripple. Thus, hysteresis control is not preferable for

PVEs. Similar to the CM control methods, different VM control methods, including open-loop control methods [8], [69], linear PI control controllers [18], are exploited to regulate the PCS. In [18], the PI control scheme is implemented via analog circuits with high switching frequency (i.e., 1 MHz) to achieve excellent dynamic characteristics. A common issue with either high bandwidth VM or CM control approach would be that operation of the PVE is limited to one region of the I-V curve (i.e., unstable in CCR since VM control in place and unstable in CVR since VM control in place) due to the oscillatory reference signal.

To resolve the oscillatory reference signal issue, dual-mode control methods are employed as the inner control scheme, which applies two separate control loops based on the operating region of the I-V curve [16], [28], [29]. In [16], a passivity-based control method is used as the CM controller, and a non-linear control method based on capacitor current is used as the VM control to achieve faster response characteristics. The main limitations of the dual-mode control method are that it increases the complexity of the control scheme and requires an additional control algorithm to improve performance in the vicinity of maximum power point (MPP) [28].

Moreover, in [30], a non-linear SMC is used to regulate the power stage with fast dynamics. However, its performance with PV MPPT converters has not been investigated. Further, applying non-linear VM control methods that rely on filter values and capacitor current for PVE with buck topologies is challenging due to the existence of a high-frequency filtering input capacitor of the load converter and current harmonics generated due to the switching of load converter, as described in section 1.3. As a result, large-signal-based control methods such as SMC, natural switching surface, and boundary control with second-order switching surface haven’t been employed in PVE applications.

2.2.3 Reference Generation Algorithm

The function of RGA is to determine the operating point current/voltage reference on the I-V characteristics curve based on load information. Most of the RGAs are fall under two categories: DRM [18], [30], [64], [67], [68] and resistance comparison method [8], [33] based on the feedback signal. In DRM, load side voltage/current is measured and fed into a PV model to directly calculate a current/voltage reference. The problem with DRM is that it creates an oscillatory reference signal in one region of operation (i.e., in CVR with current-mode control and CCR with voltage-mode control) as feedback signal always has an ac ripple [28]. As shown in Figure 2.1, the I-V curve can be divided into two regions: CCR and CVR. In CCR, a small change in current would escalate a significant change in voltage. Similarly, in CVR, a small change in voltage would escalate a large change in current. Thus, the operation of PVE in both CCR and CVR is challenging with DRM.

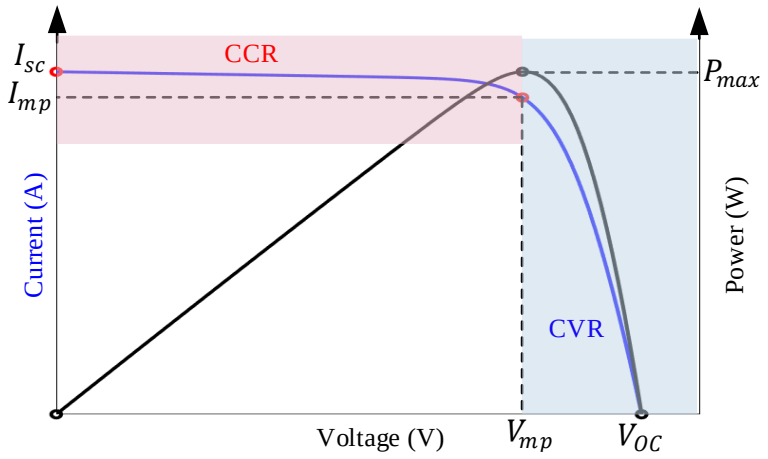


Figure 2.1 I-V and power vs voltage (P-V) characteristics of PV array.

As mentioned in the previous section, dual-mode control methods are employed to resolve oscillatory reference signal by using two separate direct referencing blocks and accordingly choosing the control mode considering the operating regions in I-V curve; CCR

or CVR [28], [29]. Alternatively, the oscillatory reference signal's impact can be minimized by designing the inner control loop with a lower control bandwidth. Low bandwidth inner controller eliminates the effect of high-frequency oscillations but at the expense of the dynamic performance of the PVE. However, linear controllers with lower bandwidth are generally used over fast-dynamic non-linear control methods in PVEs to maintain stability in both CCR and CVR. Further, with DRM, the reference generation loop is coupled with the inner control loop response. Hence response time of the RGA is limited by the inner loop bandwidth. Since low bandwidth inner controllers are typically used to overcome the oscillatory response in the reference, this will further impact the overall system response of PVE.

Resistance comparison methods based on load resistance feedback are considered to decouple the outer reference generation loop from the inner control loop response and suppress reference oscillatory problem [8], [33]. In PVEs, the load line determines the operating point reference on the I-V characteristics curve. Hence, by using load resistance as the feedback signal, any change in load information would be immediately reflected in the reference generation block and would not loop through PCS and inner loop during transients like in DRM. In the resistance comparison method, the load information can be determined instantaneously by measuring output current and voltage. In this way, the RGA will be decoupled from the rest of the system. However, in [8], [33], the reference signal is converged to an operating point through an iterative method by comparing the measured load resistance and reference load resistance. The problem with this approach is the number of iterations that it takes to reach steady-state, which leads to the slow transient response of PVE. References [72], [73] have taken steps to develop a current-resistance PV model to generate the current reference directly based on measured resistance.

2.2.4 PV Model Implementation Techniques

Regardless of the RGA (i.e., DRM or resistance-based methods), the integral element of the RGA is the PV model implementation technique. Implementation of the PV model characteristics is exploited in both analog hardware circuits [9], [18], [64], and in digital platforms with microcontrollers [15]-[17]. Different analog circuits are implemented to produce the reference signal, including a photodiode with an LED [9], a small PV cell with a light source [74], PV equivalent analog circuit with both voltage-controlled voltage source and voltage-controlled current source [64] and PV single-diode five-parameter model equivalent analog circuit [18]. Although analog implementations are preferred for high accuracy, minimizing costs, and achieving higher bandwidth in the reference generation process, PV models implemented in digital platforms are much popular due to ease of implementation and flexibility. Methods of implementing PV model in digital platforms can be classified into three types;

1) PV model via numerical solution of the implicit I-V characteristics.
2) PV model via analytical solution
3) Look up table (LUT).

2.2.4.1 PV model via numerical solution of the implicit I-V characteristics

In literature, several mathematical models are used to describe the PV array I-V characteristics. These models differ based on the number of parameters involved, the procedure used to calculate parameters and required accuracy. Most widely used model is known as the single-diode model in which PV cell is modelled using an equivalent circuit, as shown in Figure 2.2 [32].

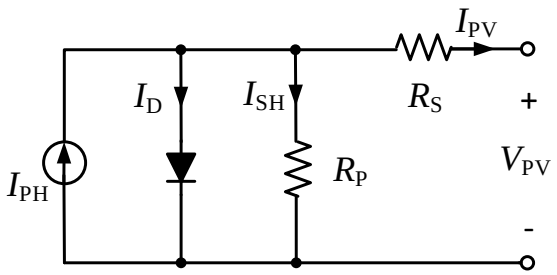


Figure 2.2 Circuit of the single–diode PV model [32].

The non-linear I-V characteristics equation of a single-diode PV model is given by,

$$I = I_{PH} - I_{on}\left[exp\left(\frac{V+R_sI}{aV_t}\right) - 1\right] - (\frac{V+R_sI}{R_p}) \quad (2\text{-}1)$$

where I_{PH} is the photocurrent generated by the incidence of irradiation on the solar cell, I_{on} is reverse saturation current of the diode, a is the diode ideality constant, R_S represents the structural resistance in the PV cell, R_P represents the leakage effect of the solar cell semiconductor material, $V_t = kT/q$ is the thermal voltage of the PV cell in which k is the Boltzmann constant (1.3806503×10-23 J/K), and q is the magnitude of an electron charge (1.602176×10–19 C) [32]. The I-V characteristics of PV cell is shown by Figure 2.1, which ranges from short circuit current $(I_{sc}, 0)$ to open circuit voltage $(0, V_{oc})$ through the knee point (I_{mp}, V_{mp}) for a given solar irradiance (G) and temperature (T). A single PV cell circuit can be scaled up to determine the I-V expression for a PV array that composed of series-and-parallel connected modules (N_{cs}, N_{cp}) by modifying (2.1) with $I_{ph,array} = N_{cp}I_{ph}$, $I_{o,array} = N_{cp}I_{ph}$, $V_{t,array} = N_{cs}V_t$, $R_{s,array} = R_s.N_{cs}/N_{cp}$ and $R_{p,array} = R_s.N_{cs}/N_{cp}$.

The I-V relationship of this model is an implicit non-linear equation that requires an iterative method to find the solution accurately. Finding a solution for I-V characteristic equation using an iterative approach is challenging in fixed time step discrete environments. Hence, in [6], [15], [75], the PV model is solved numerically using the current calculated from

the previous time step considering a smaller time step. Here, this method is referred to as the PV model via numerical solution of the implicit I-V characteristics. It requires knowledge of all PV cell parameters. When PV cell parameters are unknown for given conditions, parameters can be extracted using analytical methods [76], [77], and numerical method [32], [78] based on data points obtained by experiments or manufacture's datasheets.

2.2.4.2 PV model via analytical solution

Approximate explicit I-V characteristics are presented in [66], [69], [79], [80] to calculate current reference. Also, the single-diode four parameter model (i.e., by neglecting shunt resistance) has an explicit voltage vs current (V-I) equation that is used as an explicit model to generate the voltage reference [69], [81]. These models can easily be adopted in PVEs and are accurate enough to consolidate actual I-V curves.

2.2.4.3 Look Up Table

The third technique is the LUT approach, in which current-voltage pairs are used to represent I-V curves without any formulas [8], [16]. In the PVE context, this technique is highly exploited in implementing I-V curves for its easy implementation in static memory and allows to generate either current reference or voltage reference as required. However, its accuracy will be dependent on the amount of stored data.

2.2.5 Dynamic Performance of Switch-mode PVEs

As highlighted in Chapter 1, PVE demands fast transient performance as a nonlinear source emulator to replicate the actual dynamic bahavior of a PV array. Even though switch-mode PAs have been extensively used in the literature for PVEs, most of them have poor performance in dynamic response time compared to linear power stage schemes. Following

Table 2-1 summarises the dynamic performance of some of the key PVEs based on switch-mode PA together with their characteristics. In both [18] and [68], the control scheme is implemented via analog circuits with high switching frequency (i.e. 1 MHz and 30 kHz) to achieve excellent dynamic characteristics. However, it will lead to higher switching losses and more heat sink requirements. Dynamic performance of buck-derived converters is determined by control algorithm, switching frequency, LC filter parameters and the voltage conversion ratio [82]-[84]. As stated in Chapter 1, these parameters need to be properly designed in switch-mode PA design to mimic similar dynamic characteristics of an actual PV module.

Table 2-1 Dynamic performance and characteristics of existing switch-mode PVEs.

Reference	Settling time for a load step change	PCS	Inner Control Loop + RGA
Nguyen-Duy 2016 [18]	10 μs ([17, Fig.17])	Synchronous DC-DC buck converter two-stage LC filter	PID + PV array small-signal circuit (Analog circuit)
Koran 2010 [68]	3.8 ms ([67, Fig.17])	DC-DC buck converter two stage LC filter	PID + PV equivalent circuit (Analog circuit)
Chung 2013 [66],	6 ms ([66, Fig.12])	LLC resonant DC-DC converter	Frequency modulation control + RGA is not found
Zeng 2002 [8]	~100 ms ([7, Fig.12])	DC-DC buck converter	Open-loop control+ Resistance comparison with a LUT

Also, the dynamic performance of the PVE is a critical parameter for testing fast-dynamic MPPT converters. High-performance MPPT algorithms are proposed to improve the extraction efficiency and minimize errors of applications that go through rapid changing irradiance conditions as well as large-scale applications. To understand the convergence speed

of modern-day MPPT algorithms, of high performing MPPT algorithms. provides the transient time of some of the high performance MPPT algorithms for an irradiance step change.

Table 2-2 Dynamic performance of high performing MPPT algorithms.

Reference	Method	Startup transient	Settling time for an irradiance step change from 50% to 100%
Zhou 2019 [85]	Dual-stage *(dp/dv* tracking method Plus BC)	Not found	0.3 ms
Zurbriggen 2018 [48],	State-plane direct	1.2 ms	0.7 ms
Paz 2016 [49]	Single-stage (Lock in amplifier based)	17.3 ms	34.6 ms
Haroun 2015 [86]	Dual-stage (Sliding mode)	25 ms	Not found

2.3. Boundary Control

BC is known as a geometric-based control method that guides the state variables along a switching surface until it reaches the intended operating point [87]-[90]. The switching surface is defined as a boundary condition in the state plane that decides the state of the switches of the converter. Hysteresis control [91],[92], and SMC [54], [93], are the widely used BC methods with a first-order switching surface in which state variables are guided along a straight line. This results in multiple switching actions to reach the steady-state during transients and leads to slower response time. The second-order sliding mode (SOSM) control methods are exploited using the twist and optimal algorithms to achieve better transient responses compared to 1st order SMC method [94]-[96]. Similarly, by using BC with curved switching surfaces such as σ^2 [56]-[58], NSS [59]-[61], the converter can achieve near-optimal response for large signal disturbances.

In σ^2, a second-order switching surface is derived by predicting the trajectory of state variables of the converter after a switching action. Hence, σ^2 will enhance the tangential velocity of the trajectory along the switching surface, which helps in providing a superior transient response over other BC methods with first-order switching surface [57]. Furthermore, it allows maintaining complete control over the operation of the converter, including startup, transients, and steady-state conditions [56]. Typically, σ^2 has been proposed for buck-derived converters [97]-[100] to regulate its output voltage by controlling the capacitor voltage at a specified voltage band (Δ) that governs the switching frequency of the system. In [101],[102], boost-derived PFC converters are proposed with σ^2 for dc-link voltage control, and it is shown that a steady-state can be achieved within two switching actions. According to literature, the σ^2 provides a near-optimal switching surface to achieve fast-dynamic response while improving the system stability and robustness with constant power loads.

2.3.1 Control law derivation

The basic principle of σ^2 builds on state trajectories of the converter and guiding the converter in a near-optimal manner to achieve control objectives. Switching criteria are determined by identifying the right moment to turn ON or OFF as the movement of voltage and current can be predicted based on the steady-state operation of the converter. The switching criteria consider the area under capacitor current (i_C) with a hypothesized switching action until $i_C = 0$, and comparing this area with a fixed ratio of the output voltage error instantaneously [56]. It assumes that output current (i_O) is relatively constant by considering the load as pure resistive (R_L) and change of inductor current (i_L), Δi_L equals to the change of

i_C, Δi_C. Figure 2.3 shows the buck converter schematics with a resistive load. The switching criteria for buck converter can be derived as below,

Switch ON Criteria

$$v_C(\mathrm{t}) \leq v_{C,min} + k_1 i_C(\mathrm{t})^2 \quad , i_C(\mathrm{t}) < 0 \tag{2-2}$$

Switch OFF Criteria

$$v_C(\mathrm{t}) \geq v_{C,max} - k_2 i_C(\mathrm{t})^2 \quad , i_C(\mathrm{t}) > 0 \tag{2-3}$$

where $v_{C,min} = v_{ref} - \Delta$, $v_{C,max} = v_{ref} + \Delta$ and k_1, k_2 are constants. The ideal values of k_1 and k_2 are,

$$\{k_1, k_2\} = \left\{\frac{L}{2\,C(v_S(\mathrm{t}) - v_{ref})}, \frac{L}{2\,C\,v_{ref}}\right\} \tag{2-4}$$

where v_S is the input DC voltage. A detailed derivation of (2.2)-(2.4) can be found in [56].

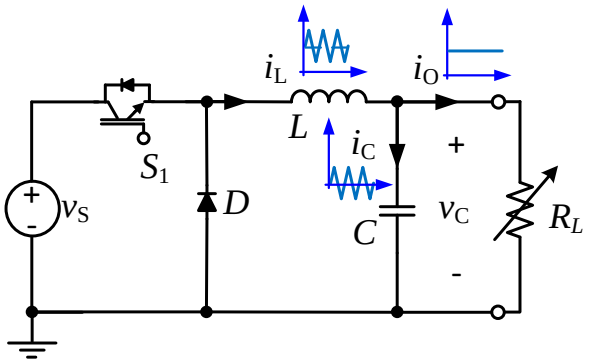


Figure 2.3 Circuit schematics of a buck converter with a resistive load.

Figure 2.4 shows the switching trajectory of σ^2 from starting up to target operating point on the $v_C - i_L$ state plane for a resistive load. It illustrates that the system reaches steady-state within two switching actions while maintaining the defined voltage band. Ideal state on and off trajectories are obtained by solving state-space equations of the converter for different

initial conditions. The on-state trajectories are represented in solid lines, and off-state trajectories are represented in dotted lines. The reason for such a faster dynamic response is that the switching surface of the σ^2 at maximum and minimum boundaries closely follows the natural state trajectories of the system. Once the system meets the switching surface, it moves along the switching surface. Switching surface at upper (${\sigma^2}_{\Delta+}$) and lower (${\sigma^2}_{\Delta-}$) boundaries are shown in Figure 2.5. The specifications of the considered buck converter are tabulated in Table 2-3.

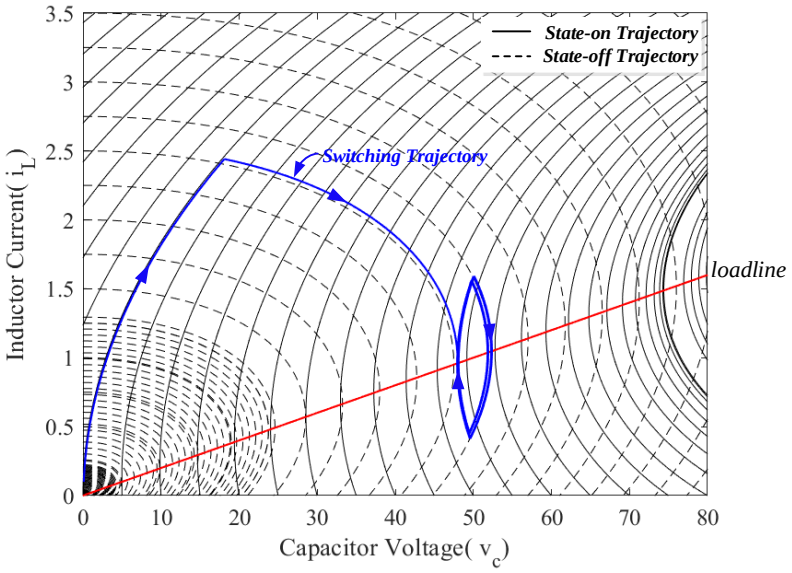


Figure 2.4 System trajectories on the inherent state plane with σ^2 for a resistive load from start up to steady-state operation.

Table 2-3 Parameter values used in the buck converter design.

Parameter	Value	Parameter	Value
v_S	120 V	L	3.5 mH
v_{ref}/Δ	50 V/2V	C	4.7 µF

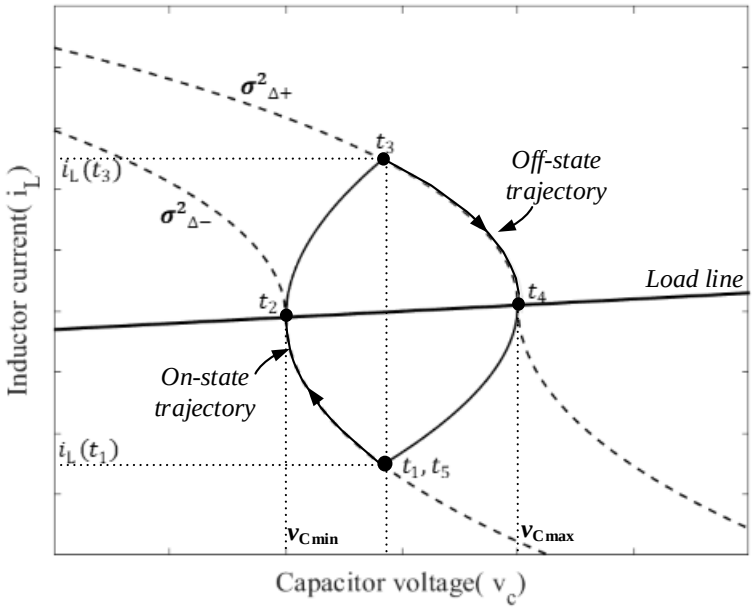


Figure 2.5 Switching surface of σ^2 at its boundary conditions on the inherent state plane.

2.3.2 Limitations of conventional σ^2

Despite its advantages in settling time, dynamic response and system stability, σ^2 is sensitive to parameter variations [57]. Also, its performance is significantly affected when a second-stage load converter is connected to it. The switching criteria of σ^2 is a function of parameters such as L and C. Hence, if practical L and C values in the converter are different from the nominal values considered in the switching criteria, σ^2 leads the converter to operate with inaccurate voltage ripple, switching frequency and average output voltage [57], [58]. In the worst case, the deviation in voltage ripple may even cause the converter to operate in discontinuous conduction mode (DCM). These deviations will be aggravated when σ^2 controlled buck converter is cascaded to a non-linear switching converter. The second-stage converter mostly consists of a high frequency filtering input capacitor (C_L) that appears in parallel with the first-stage output filter capacitor (C). This would change the equivalent

capacitance seen by the first-stage/source converter; hence it changes the original state-plane trajectories of the first-stage/source converter and creates a significant discrepancy between actual system and derived switching criteria, σ^2. Moreover, current ripple components led by the switching of both first and second-stage converters would pass through C and C_L. Thus, the shape of i_C waveform cannot be approximated as a triangular in steady-state and the steps taken to derive conventional σ^2 in [56] would no longer be valid.

Such discrepancies between the real system and designed switching criteria would lead to incorrect switching actions. It is the main limitation of applying a large-signal-based control method (i.e., SMC, NSS and σ^2) for source converter control. As a result, the standard linear control methods such as PID, PI with pulse width modulation (PWM) schemes are more often applied for source converter control to avoid this issue [103]. However, linear control methods require a much higher switching frequency to achieve faster responses and require an additional damping method to avoid the negative impedance instability with CPLs, as stated in Chapter 1 [104], [105]. Further, different signal-based control approaches like proximate time-optimal control [106],[107], and SOSM [94] that utilize a capacitor current estimator are utilized to improve transient response and robustness of buck converters.

Nevertheless, the σ^2 method is a promising option to achieve faster dynamic performance for buck converter with linear loads, given the fact that it can reach steady-state within two switching actions. The performance of σ^2 in a cascaded configuration with a load converter has not been investigated in detail in the literature. Applying conventional σ^2 for a cascaded configuration would yield incorrect switching actions, and specified control parameters cannot be maintained. It is, therefore, desirable to correct the BC law by considering the impact from a second-stage converter while preserving fast response characteristics.

2.4. Power Hardware in the Loop (PHIL) Simulations

PHIL simulation is an extension to the real time (RT) simulation, which interacts with real power devices through a power interface. A basic PHIL simulation can be illustrated by Figure 2.6, in which an original circuit is formed into a hybrid configuration of software (i.e., simulation in RTS) and hardware (i.e., DUT) through a power interface. The PA is required to amplify the signals from RTS, and real power is exchanged between the PA and the DUT. The signal links between the RTS and PA/sensor can be either analog or digital depending on the input/output devices of both the RTS and the PA [36]. Typically, the power interface consists of PA, ADC, DAC and sensor, as shown in Figure 2.6.

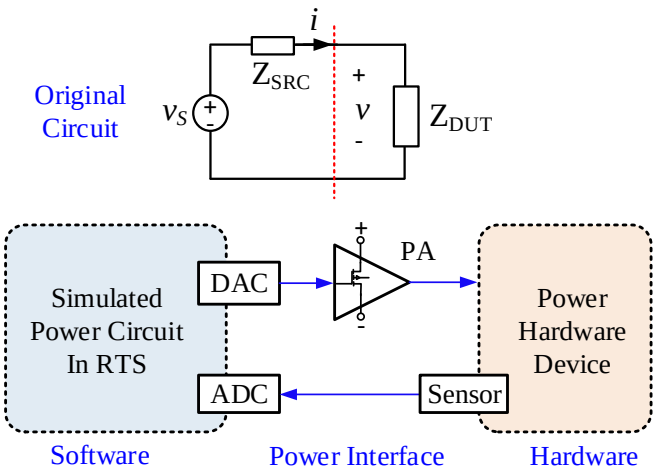


Figure 2.6 Original circuit vs Basic configuration of the PHIL simulation.

In PHIL, the interface algorithm determines how the signals are exchanged between RTS and DUT. The IA can be either voltage and/or current type, depending on the selected PA. Choosing a proper IA is vital as it creates unique challenges in terms of stability, accuracy, power loss and lack of generality [108]. Several IAs are presented in the literature, including the ideal transformer method (ITM), the transmission line model, the partial circuit duplication

and the damping impedance method (DIM) and, their performance is analyzed extensively in [36],[62], [108] -[109]. The ITM is the most commonly used IA due to its high accuracy, low computational requirement and easy implementation. Therefore, ITM IA is considered though out this thesis to implement PHIL simulations. Figure 2.7 shows the system configuration of voltage-type and current-type ITM IAs. In voltage-type ITM, voltage is applied to the terminals of the DUT via the PA and current measured from the DUT is sent back to the RTS as a feedback signal. Similarly, current-type ITM is configured by sending out current reference to the CM PA and feeding back the voltage.

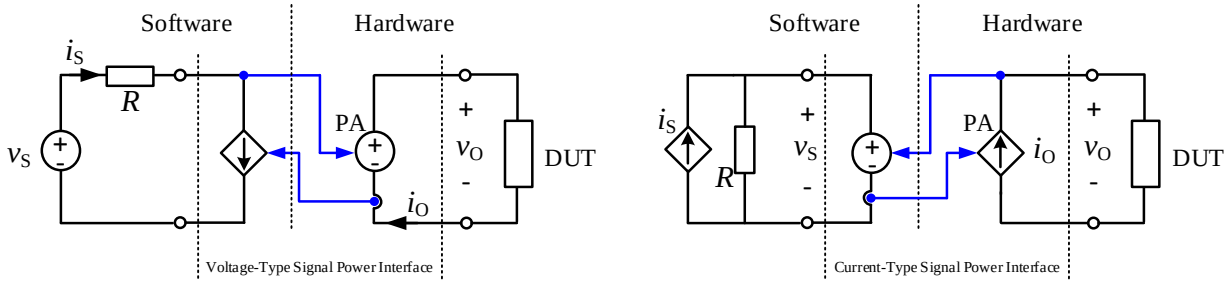


Figure 2.7 ITM interface (a) voltage-type (b) current-type [36].

The PA is a crucial component in the PHIL simulation with a requirement of low cost, efficiency and fast dynamics. To achieve a stable PHIL and reduce time delays within the loop, PA selected should have higher bandwidth and minimum time delay [20]. Both linear PAs and switch-mode PAs are commonly used in different PHIL applications depending on their requirements [20], [35]. As already highlighted, switch-mode PA is more favourable for high power PHIL setups for its advantages, but it suffers from slow dynamic characteristics [20]. Therefore, PHIL simulations require switch-mode PAs that have higher control bandwidth. Table 2-4 summarizes the features and dynamic specifications of some commercial PAs in the PHIL industry.

Table 2-4 Dynamic Performance and Characteristics of Commercial PAs for PHIL.

PA	Type	Operating Mode	Power Range	Large-signal Bandwidth	Dynamic Characteristics			
					Slew ate	Settling time	Input-output delay	Small-signal Bandwidth
Spitzenberger & Spieß PAS 100 [20]	Linear PA	AC/DC	10kVA-150 kVA	0 - 15 kHz	> 52 V/µs	N/A	4 µs	-
AE Techron 7224 [25]	Linear PA	AC/DC	1 kVA	0-300 kHz	75 V/µs	<10 µs	< 1 µs	-
Ponova PA series [110]	Linear PA	AC/DC	10kVA-150 kVA	0 - 5 kHz	-	<20 µs	< 20 µs	-
Egston CDA [111]	Switch-mode PA	AC/DC	100-120 kVA	0 - 5 kHz	-	-	4 µs	0-15kHz
Opal-RT OP1400-10 [112]	Switch-mode PA	AC/DC	5kW-15kW	0 - 10 kHz	5 V/µs	-	5 µs-8 µs	-
Puissance plus (PA-24K) [113]	Linear PA	AC/DC	1kW-750kW	0 - 30 kHz	-	<20 µs	-	0-150 kHz

2.4.1 Applications and advantages of PHIL simulations

The hybrid nature of PHIL simulations makes it well-suited for evaluating renewable energy integration and microgrid applications. It allows to test and validate both the physical PE interface converters and the distribution network it operates with several attractive features such as reduced cost, less time, scalability, repeatability, flexibility and perhaps most importantly, with low-risk testing [114]. The PHIL concept is already proven and adapted in applications such as grid-connected PV [37], [38] and BESS integrations [42], [43] as a grid emulator. Also, it has been adopted for emulation of PV arrays [40], [41], wind turbines [115], fuel cells [116], battery [117], [118], and electric machines [119], [120], to examine respective interconnected systems. PHIL for emulating sources would improve the flexibility and controllability of the grid integration testbed and provide the advantage from the grid integration test setup since RTS is already in place.

2.4.2 Stability and accuracy analysis for PHIL simulations

As highlighted in Chapter 1, the key limitation of the PHIL is the components involved in the power interface introduce time delays and limited bandwidth that do not exist in the

original circuit. Those would affect the stability and accuracy of the PHIL simulation [44], [62], [108], [109], [121], [122]. Therefore, the stability and accuracy of the PHIL simulations with different IAs such as ITM and DIM have been extensively studied in the literature [108], [109]. Most straightforward method to evaluate the stability of a PHIL simulation system is applying the Nyquist stability criterion on the open-loop transfer function (TF) of the PHIL system [121]. The open-loop TF of the PHIL system enables the investigation of system stability comprehensively using any other traditional frequency-domain techniques such as Bode plots, Bode stability criterion, and Routh-Hurwitz (R-H) stability criterion [44], [109], [121], [122]. Both Bode stability criterion and R-H stability criterion measure relative stability for determining exact instability points over the range of variables. However, both methods inherit their own drawbacks for non-minimum phase systems such as PHIL systems that consist of time delays and right half plane zeros. The R-H stability criterion requires approximating the time delay using methods such as the Pade approximation. Hence, it is not preferable for systems with time delays. Unlike the R-H stability criterion, the bode stability criterion does not require the time delay to be approximated to determine stability. It becomes complex in PHIL systems for analytically determining phase cross points and evaluating the magnitudes. Both Nyquist and bode plots are graphical methods that provide a necessary and sufficient condition for stability and do not require approximating time delays.

Two crucial factors for the stability of ITM IA are the loop delay and the impedance ratio between simulation and hardware. The time delay of the power interface is primarily determined based on the RTS simulation time step and PA characteristics. The required minimum simulation time step depends on the computational capability of RTS, which again depends on the size of the simulated network, levels of details of the model and simulation

hardware [23]. Digital links between RTS and PA with Aurora protocol are considered to eliminate ADC and DAC converters, reducing the latency in the power interface [23]. Nonetheless, the ITM interface may pose some stability and accuracy issues in the PHIL experiment depending on case-specific factors like the impedance ratio between simulation and hardware and non-idealities in the power interface. Hence, it is vital to investigate the stability of a given PHIL-based system to understand the impact of power interface and DUT before PHIL experiments. In addition to stability, PHIL simulation must be accurate to ensure the validity of the results. A method to evaluate accuracy is described by W. Ren et al. [62], that derived the transfer function of the system response with respect to interface disturbances for assessing the error. The detailed derivation of this method can be found in [62].

2.5. Battery Emulator

In this section, a brief review of BEs is conducted to identify differences compared to PVEs as a DC source emulator. The BE is composed of a controllable power source with a controller that can emulate the electrical behavior of batteries with battery models. Typically, the battery model is updated with the load current measurement to account for the charging/discharging of the battery and simulated to generate the reference voltage for the power source controller [118]. The main difference of BE compared to PVE is that the PCS must handle bidirectional power flow for emulating charging and discharging operations.

The PCS of the BE is operated in VM control with a possibility of bidirectional power flow to ensure both charging/discharging operations. The switch-mode PCSs have been extensively used in literature for standalone BEs targeting accurate emulation of real batteries. The switch-mode topologies that consider in BE include; DC-DC buck-boost converter [123],

three-phase interleaved boost [124], three-phase synchronous DC-DC buck converter [118], multi-phase synchronous DC-DC buck converter [125], cascaded dual active bridge [126]. Multi-phase configuration is considered to maintain a lower output current ripple without raising the switching frequency. All these topologies must be equipped with a reversible power supply at the front end to handle the reverse current during charging mode. Typically, the reversible supply is realized with an active rectifier circuit [118] or a resistive dissipation circuit with a blocking diode [123].

Lithium-ion batteries have emerged as a universal technology due to their high energy density and low maintenance requirements [123], [124]. Therefore, this thesis only considers the BE technology related Lithium-Ion batteries with switch-mode PAs. Furthermore, battery emulation depends significantly on the battery model, which has been developed with a wide variety of approaches to capture the battery characteristics for specific purposes, from battery design, performance evaluation to circuit simulation. Equivalent circuit models (ECM) are often adopted in BE due to their simulation ability, less complexity than electrochemical models and reasonable accuracy [13]. ECM can be classified into three categories; (a) Thevenin-Based (b) Impedance Based (c) Run-Time Based as shown in Figure 2.8. In [13], Thevenin based ECM model is presented to replicate the short-term and long-term transient behaviors of a Lithium-ion battery. Thermal dependency has not been considered in this model. In this model, a curve fitting technique is used to extract all non-linear circuit parameters given as a function of SOC. In [127], [128], the effect of temperature is considered by changing the Thevenin-Based ECM parameters using the LUT approach.

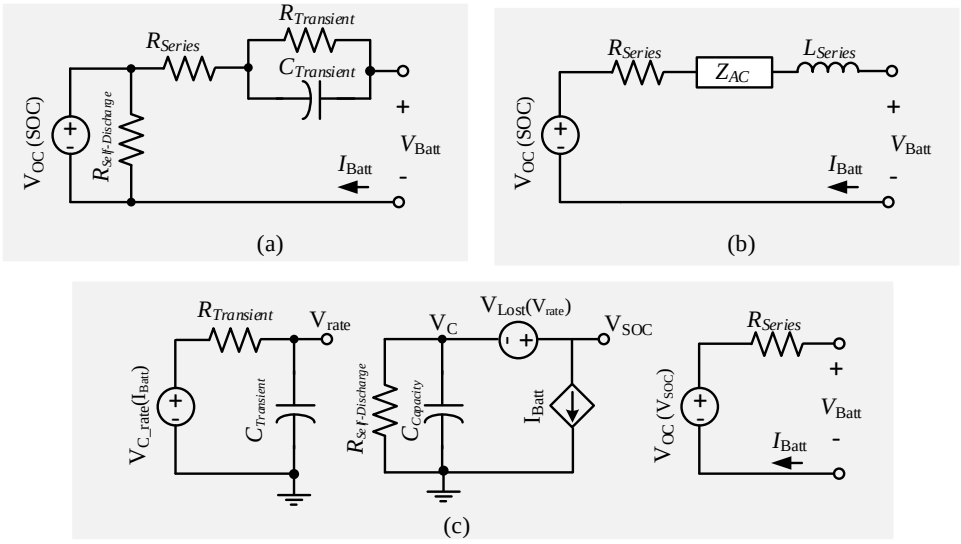


Figure 2.8 State of the art in ECM (a) Thevenin-based (b) Impedance-based (c)Runtime-based [13].

2.6. Summary

This chapter presented a general overview of PV emulators, boundary control methods, PHIL simulation and battery emulators highlighting state-of-the-art, operating principles and their limitations. Those four areas are identified as crucial components to conduct this research. This chapter builds a foundation to achieve the research objectives mentioned in Chapter 1.

Chapter 3

Boundary Control with Corrected Second-order Switching Surface for Buck Converters Cascaded to Capacitive Loads

The work described in this chapter was published in the following paper: I. Jayawardana, C. N. M. Ho and Y. He, "Boundary Control with Corrected Second-Order Switching Surface for Buck Converters Connected to Capacitive Loads," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 183-196, Feb. 2021.

This chapter studies the shortcomings in second-order boundary control schemes of buck converters with capacitive loads and non-linear switching loads. Secondly, the chapter introduces a boundary control scheme with corrected second-order switching surface to drive buck converters cascaded to boost converters. The proposed method is verified using both simulations and experiments, and the applicability of this method in DC source emulators and its limitations are explained.

3.1. Introduction

Boundary control with second-order switching surface is exploited for achieving faster response time and robust operation of switching power converters. However, the system performance of the boundary-controlled converters is significantly affected when it is connected to a second-stage converter with a large input capacitor, as highlighted in Section 2.3.2. Therefore, this chapter aims to extend the conventional σ^2 suitable for buck converters cascaded to capacitive loads and boost converters. Figure 3.1 shows a cascaded DC-DC system configuration composed of a conventional σ^2- controlled buck converter connected to a second-stage boost converter (hereafter referred it also as cascaded buck-boost). The second-stage boost converter is considered to represent capacitive loads.

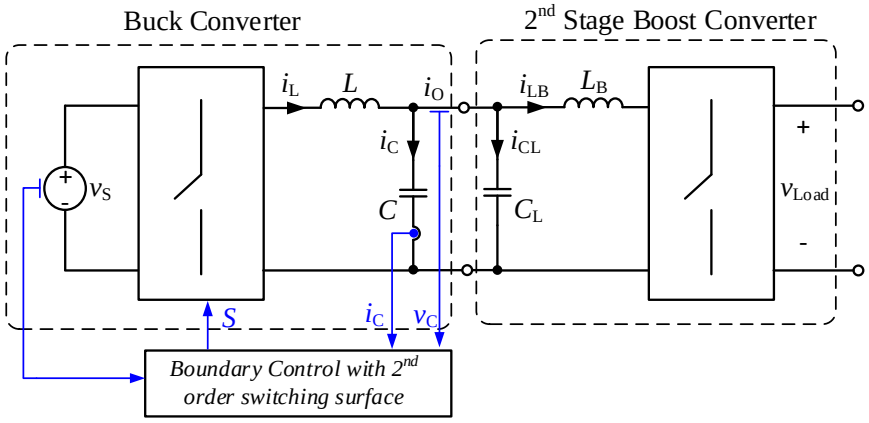


Figure 3.1 General configuration of a system composed of buck converter cascaded to boost converter.

The parallel capacitor from the second-stage/load converter would change the equivalent capacitance seen by the first-stage/source converter. Hence it changes the original state-plane trajectories of the first-stage/source converter and creates a discrepancy between the actual system and derived σ^2, as the switching surface of σ^2 relies on filter parameters. Moreover,

σ^2 depends on the instantaneous measurement of capacitor current and capacitor voltage, and its ripple may be affected by the ripple components generated by the switching actions of the second-stage converter. Thus, applying conventional σ^2 for a cascaded buck-boost configuration would yield incorrect switching actions, and specified control parameters can not be maintained. Therefore, it is desirable to correct the boundary control law by considering the impact from the second-stage converter while preserving fast response characteristics.

The cascaded DC-DC configuration shown in Figure 3.1 is a typical configuration for a system that uses a buck stage as a source converter and can be seen in applications such as non-isolated switch-mode power supply [129], PV emulator [64] and fuel cell emulator [130]. Particularly in PV emulators, the buck-based converter is mostly used as the controlled power source to emulate required PV models with a second-stage boost converter as the DUT. Targeting such applications, a boundary control scheme with a corrected switching surface for buck converters connected to second-stage boost converters is presented in this chapter. The proposed switching surface is derived by considering the presence of load capacitance as well as addressing any switching criteria gain mismatches due to filter parameter variations. An innovative outer voltage ripple feedback loop is introduced to determine a corresponding switching criterion gain factor that accounts for mismatch due to additional load capacitance as well as any variations in filter parameters in the real system.

In this chapter, the limitations of conventional σ^2 in cascaded buck-boost configurations and theoretical approximations considered to derive σ_{cor}^2 are described first. Derivation of the σ_{cor}^2 and detailed design of the BC scheme are then presented, including the design procedures of the outer feedback control loop. In Section 3.4 and 3.5, simulation and experiment results of the proposed controller are presented to validate the theoretical analysis.

3.2. Issues of σ^2 with second-stage boost converter as a load

The second-stage boost converter commonly consists of an input capacitor (C_L) to filter high-frequency ripple components in the input current [131]. Existence of C_L would change and the equivalent capacitance seen by the first stage converter, to $C + C_L$ as C_L will be directly connected in parallel with C. Inductor current ripple is shared between C, C_L and input branch of the second-stage converter based on their impedance. Hence, the assumption that is taken in [56] to derive the switching criteria of Δi_L equals to Δi_C is violated. Also, capacitance considered in the switching criteria is different from the real circuit. These scenarios create a discrepancy between the system used to derive the switching criteria and the real system. Figure 3.2 shows the movement of the converter on the $v_C - i_L$ state plane when the buck converter is connected to a resistive-capacitive load. This shows that the converter operates with a larger voltage and current ripple due to incorrect switching actions.

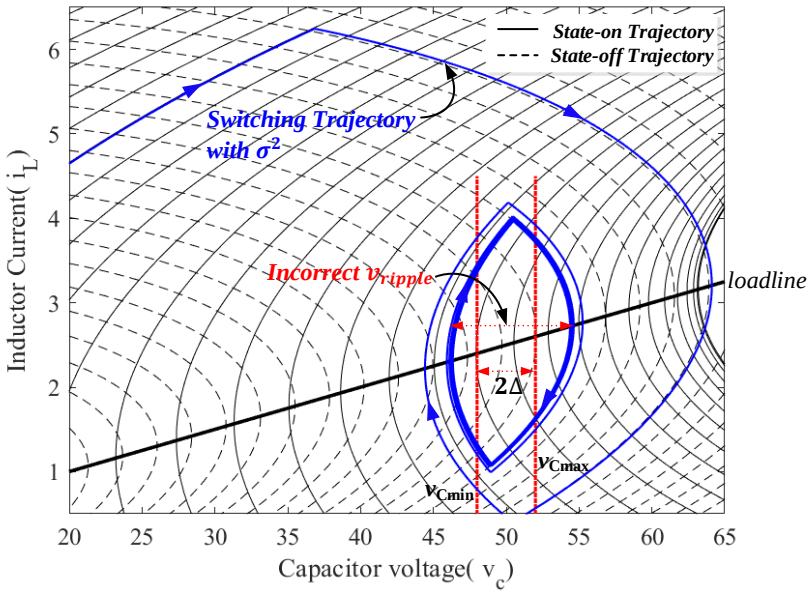


Figure 3.2 System trajectories on the inherent state plane with σ^2 for Resistive-capacitive load (R_L=20 Ω, C_L=10 µF, v_{ref}=50 V and Δ =2 V).

In cascaded buck-boost configuration, the boost-stage inductor acts as a high impedance path for high-frequency current ripple components of the buck-stage inductor current and vice versa. The parallel capacitors are typically designed to have a significantly low impedance path for current ripple components of i_L. Hence the current ripple components of i_L passing through L_B is negligible. Similarly, it can be understood that the current ripple components of boost stage inductor current (i_{LB}) are not visible in i_L. i.e., if the impedance of each inductor at high frequencies (in the range of switching frequency) is 30 times higher than the impedance of the combined capacitor branches, only 3.3% of current ripple components are passing through the opposite stage inductor. Thus, it can be concluded that the current ripple of i_L will be shared mainly with capacitor branches (C and C_L) and it will be free from the current ripple component led by the boost stage. Figure 3.3 shows how current ripple components would interact among passive elements in the cascaded buck-boost configuration.

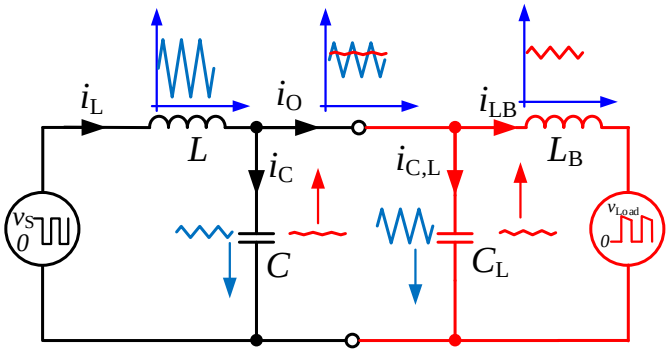


Figure 3.3 Simplified equivalent circuit of the cascaded buck-boost system.

Further, under conditions of the current ripple of i_{LB} is maintained smaller than the current ripple of i_L and C_L is much larger than C, it can be approximated that the current ripple component passing through C due to the switching of the boost converter is negligible. These are valid conditions for a boost converter since the current ripple of the boost inductor is designed to maintain around ~20% of the nominal value and large C_L is placed to filter high

frequency signal of the input current [131]-[133]. Based on the above considerations, derivation of a corrected boundary control with second-order switching surface (σ_{cor}^2) is presented in the next section.

3.3. Control Law Formulation

The proposed switching surface is derived by considering the presence of load capacitance as well as addressing any switching criteria gain mismatches due to filter parameter variations. Therefore, an outer voltage ripple feedback loop is introduced to determine the corresponding switching criteria gain factor that adjusts the overall gain while maintaining the output voltage ripple at a specified voltage band. Figure 3.4 shows the architecture of the complete system, which consists of four main elements, including the buck converter as the PCS, σ_{cor}^2, voltage ripple measurement block and the error amplifier (EA).

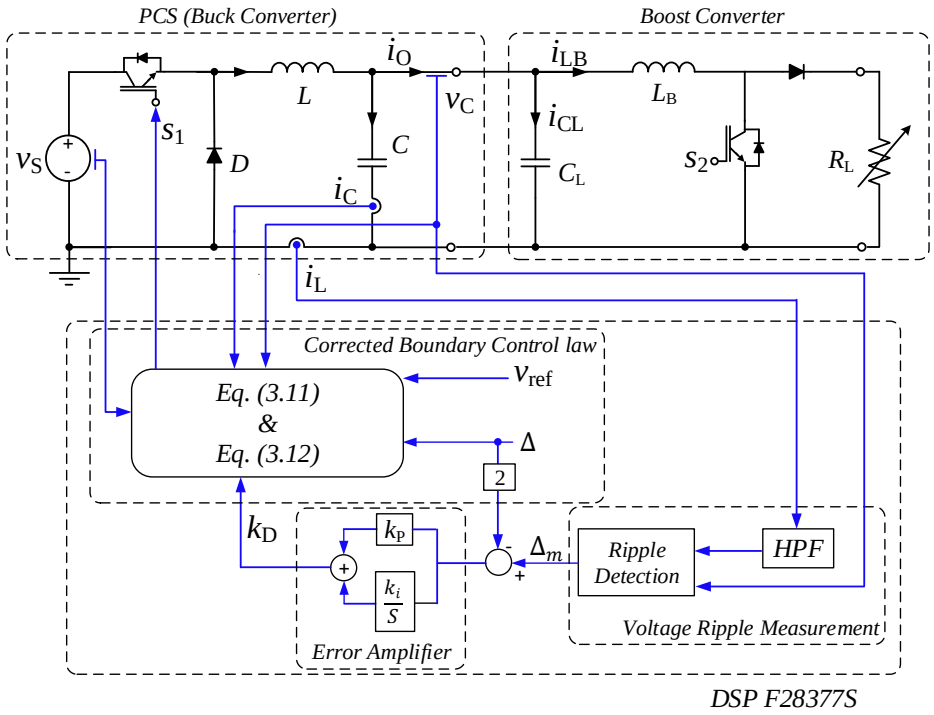


Figure 3.4 Architecture of the corrected boundary control scheme.

Firstly, voltage ripple measurement block identifies the peak-to-peak ripple of v_C (Δ_m) using i_L and v_C. Then, Δ_m is compared with a reference peak-to-peak voltage band (2Δ) using EA. The output of the error amplifier, k_D is used to adjust the deviation of switching criteria gains of σ_{cor}^2 due to filter parameter variations. The σ_{cor}^2 determines switching instants for S_1 in PCS based on v_C, i_C, v_S, v_{ref}, Δ and k_D.Thus, above mentioned elements form a controller scheme to regulate v_C together with a feedback loop for regulating $\Delta_{C,m}$ with considering the effect of C_L.

3.3.1 Derivation of σ_{cor}^2

The PCS operates with two states, namely Turn-ON state and Turn-OFF state, in one switching cycle. The fundamental time-domain waveforms of the system are shown in Figure 3.5. Following derivations are done by assuming all components are ideal. Based on the capacitor voltage equations at common output node for both C and C_L, the relationship between slope of i_C and slope of i_{CL} is derived as,

$$\frac{di_{CL}(t)}{dt} = \frac{C_L}{C}\frac{di_C(t)}{dt} \tag{3-1}$$

Applying Kirchhoff's current law at the output node,

$$i_C(t) = i_L(t) - i_O(t) \tag{3-2}$$

where $i_O = i_{CL} + i_{LB}$, and as explained before, by approximating that i_{LB} is a constant DC current from the buck converter perspective, and it is free from ripple. With this assumption, (3.2) can be differentiated to estimate the slope of i_C as;

$$\frac{di_C(t)}{dt} \cong \frac{di_L(t)}{dt} - \frac{di_{CL}(t)}{dt} \tag{3-3}$$

Thus, combining (3.1) and (3.3), slope of the i_L can be expressed as,

$$\frac{di_L(t)}{dt} \cong (1 + k_D)\frac{di_C(t)}{dt} \tag{3-4}$$

where $k_D = \frac{C_L}{C}$. Further, following the similar method described in [56], BC law can be formulated by incorporating k_D that represents the adjustments in switching criteria gains $\{k_1, k_2\}$ due to the appearance of C_L. The corrected boundary law is derived considering the steady-state characteristics during Turn-ON state and Turn-OFF state of the buck converter.

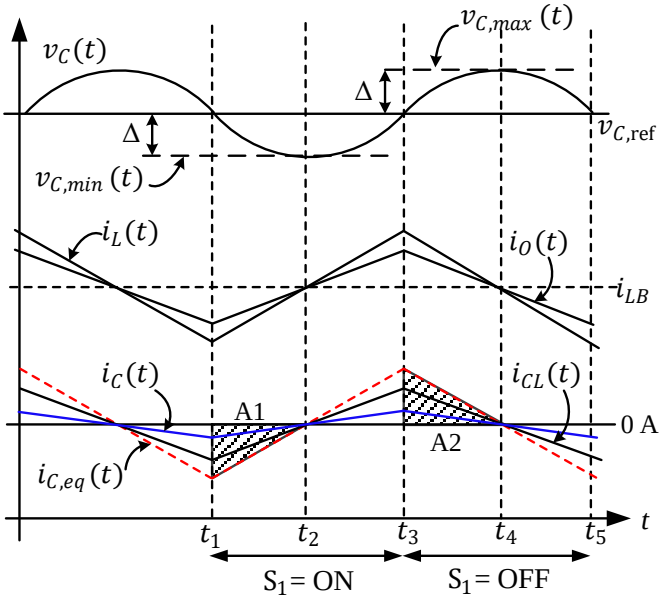


Figure 3.5 Typical waveforms of v_C, i_L, i_O and i_C.

Switch ON Criteria

Switching ON criteria is derived by determining t_1 such that v_C will reach the lower boundary $v_{C,min}$ at t_2 at which $i_C = 0$. Assumed that i_C varies linearly in Turn-ON state. Thus, the right moment to switch ON the converter should fulfill the following expression:

$$v_C(t_1) = v_{C,min} + \left[\frac{L}{2C}\frac{1}{v_S - v_{ref}}\right][1 + k_D]{i_C}^2(t_1) \tag{3-5}$$

Detailed derivation of (3.5) is given in Appendix A.1. In order to ensure that v_C(t) would not reach below v_{Cmin}, the right moment to switch ON the converter should fulfill the following expression:

$$v_C(\mathrm{t}) \leq v_{C,min} + \left[\frac{L}{2C}\frac{1}{v_S(\mathrm{t})-v_{ref}}\right][1+k_D]i_C(t)^2 \tag{3-6}$$

$$\text{and} \quad i_C(\mathrm{t}) < 0 \tag{3-7}$$

Switch OFF Criteria

The objective is to determine a time instant t_3 such that v_C will reach the upper boundary $v_{C,max}$ at t_4 at which $i_C = 0$. Thus, the right moment to switch OFF the converter should fulfill the following expression;

$$v_C(t_3) = v_{C,max} - \left[\frac{L}{2C}\frac{1}{v_{ref}}\right][1+k_D]{i_C}^2(t_3) \tag{3-8}$$

Detailed derivation of (3.8) is given in Appendix A.1. In order to ensure that v_C(t) would not reach beyond v_{Cmax}, switching OFF criteria for S_1 is derived as,

$$v_C(\mathrm{t}) \geq v_{C,max} - \left[\frac{L}{2C}\frac{1}{v_{ref}}\right][1+k_D]i_C(\mathrm{t})^2 \tag{3-9}$$

$$\text{and} \quad i_C(\mathrm{t}) > 0 \tag{3-10}$$

Based on (3.6), (3.7), (3.9) and (3.10), switching surface of σ_{cor}^2 can be concluded as,

$$\sigma_{cor,\Delta-}^2 = \left\{(v_C(\mathrm{t}) - v_{C,min} - k_1'(i_C(\mathrm{t}))^2, i_C(\mathrm{t}) < 0\right\} \tag{3-11}$$

$$\sigma_{cor,\Delta+}^2 = \left\{(v_C(\mathrm{t}) - v_{C,max}) + k_2'(i_C)^2, i_C(\mathrm{t}) > 0\right\} \tag{3-12}$$

where k'_1 and k'_2 are constants.

$$\{k_1', k_2'\} = \{k_1(1+k_D), k_2(1+k_D)\} \tag{3-13}$$

The σ_{cor}^2 requires instantaneous values of v_S, v_C, i_C and $k_D$to determine the switching actions. The values of k_1 and k_2 are constants and defined with nominal parameters, as given in Table 2-3.

3.3.2 Output Ripple Amplitude Detection

The output voltage ripple amplitude is used as the feedback variable in the outer control loop. Determining the peak-peak ripple of v_C over a switching cycle may not be straightforward since v_C is mixed with voltage ripple components introduced by the second-stage converter. In contrast, the i_L is unaffected by the current ripple components led by the switching of the second-stage converter as they are filtered out by C and C_L. The i_L waveform is, therefore, much smoother than v_C as it only consists of current ripple components generated due to the switching of the first-stage converter. Hence, Δ_m is determined considering the instantaneous values of both i_L and v_C. Algorithm of the voltage ripple measurement block implemented in a software platform is shown in Figure 3.6. Measured i_L is passed through a high pass filter (HPF) to eliminate the dc offset and obtain the ac signal of i_L (i_{LH}). Cut-off frequency of the HPF is designed to be lower than the minimum switching frequency of the system.

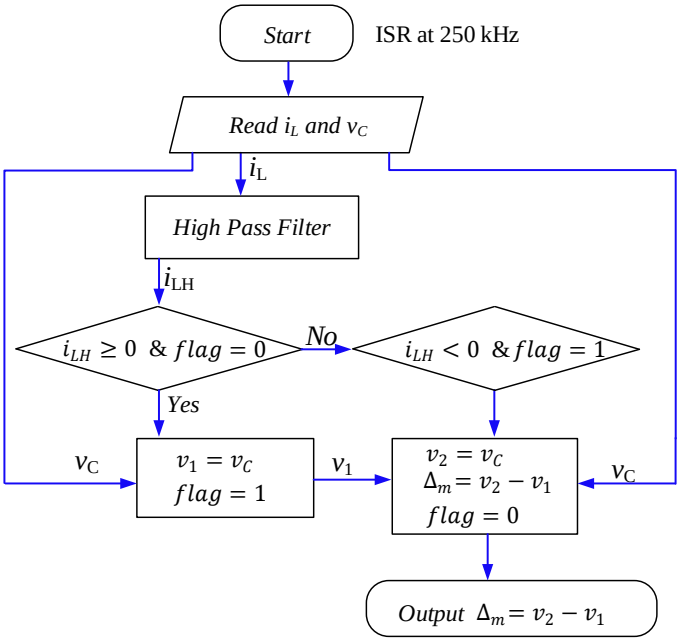


Figure 3.6 Flow chart for Δ_m measurement.

Figure 3.7 shows that v_C would be at a minimum, $v_{C,min}$ when i_{LH} is crossing zero from the negative side and v_C would be at a maximum, $v_{C,max}$ when i_{LH} is crossing zero from the positive side. Hence, at the zero crossings of i_{LH}, a flag is triggered to store the instantaneous values of v_C. Then voltage ripple magnitude is calculated at each switching cycle based on stored values.

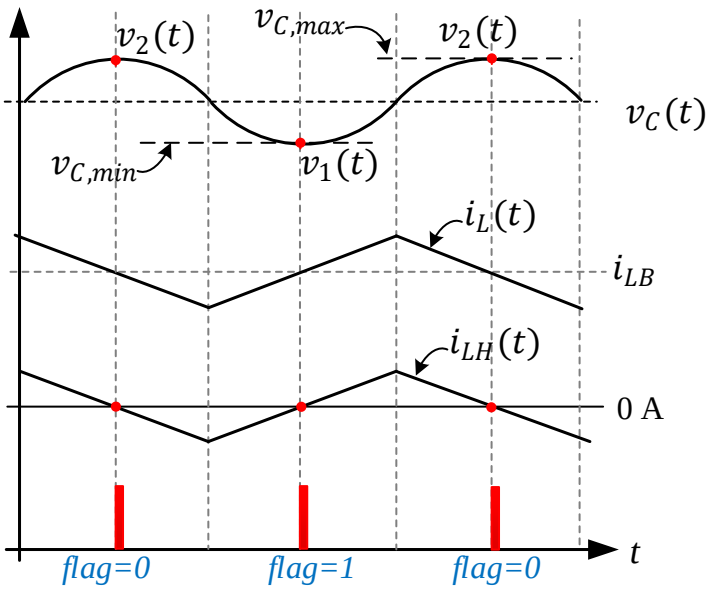


Figure 3.7 Key waveforms of voltage ripple amplitude detection.

3.3.3 Design of Outer Feedback Control Loop

The value of k_D is dependent on C_L which is typically unknown as the second-stage boost converter is often a black-box. Hence, an outer control loop is employed to determines the k_D using an outer voltage ripple feedback loop. To study system dynamics and design EA parameters, the small-signal model of the outer control loop is derived. Figure 3.8 shows the small-signal control block diagram of the outer voltage ripple feedback loop. The measured v_C ripple magnitude is compared with specified voltage ripple to check whether the boundary

controller maintains it to the specified value. The voltage ripple error is amplified by EA to generate the required k_D based on the feedback loop mechanism shown in Figure 3.8.

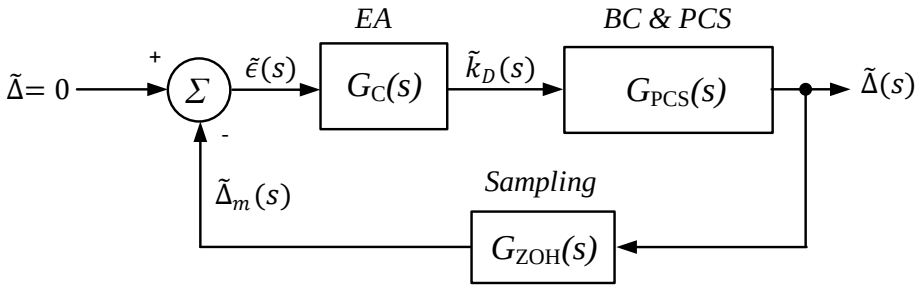


Figure 3.8 Small-signal control block diagram for the outer feedback loop.

The small-signal k_D-to-voltage ripple transfer function is derived based on the large-signal relationship between Δ and k_D. In [98], a large-signal relationship between switching frequency (f_S) and Δ of a σ^2-controlled buck converter is derived in detail. Following a similar procedure, the large-signal relationship between Δ and k_D is derived using state equations during Turn-ON state and Turn-ON state as well as considering the σ^2_{cor} switching criteria equations. The f_S of the systems is given as,

$$f_S = HK\Delta^{-0.5}(1 + k_D)^{-0.5} \tag{3-14}$$

where $H = \frac{v_{ref}(v_S - v_{ref})}{Lv_S}$ and $K = \frac{\sqrt{k_1 k_2}}{\sqrt{2dk_1}+\sqrt{2(1-d)k_2}}$. A detailed derivation of (3.14) is given in Appendix A.2. Further, (3.14) is simplified to determine the relationship between k_D and Δ.

$$k_D^{0.5} = \left(\frac{HK}{f_S}\right)\Delta^{-0.5} - 1 \tag{3-15}$$

By linearizing (3.15) at a steady operating point would yield the small-signal TF between Δ and k_D, is given by,

$$G_{PCS}(s) = \frac{\tilde{\Delta}(s)}{\tilde{k}_D(s)} = -\left(\frac{HK}{f_S}\right)\bar{k}_D^{-0.5}\bar{\Delta}^{-1.5} \tag{3-16}$$

Further, TF of the inner boundary control loop is assumed to be a unity gain since the crossover frequency of the outer voltage ripple feedback loop will be designed much lower than the f_S. Hence, the TF of $G_{PCS}(s)$ including inner σ_{cor}^2-controlled loop is represented by (3.16). The ripple measurement block is modelled as a continuous zero-order hold (ZOH) to represent the discretization process and the time delays. As mentioned, Δ_m is calculated in every half switching cycle, the transfer function of ZOH can be written as,

$$G_{ZOH}(s) = \frac{1-e^{-\frac{sT_S}{2}}}{\frac{sT_S}{2}} \tag{3-17}$$

where $T_S = \frac{1}{f_S}$ is the switching time period of the system. The EA is implemented using a PI controller and TF of $G_C(s)$ is given below in (3.18).

$$G_C(s) = -(K_P + \frac{K_i}{s}) \tag{3-18}$$

Since the gain of $G_{PCS}(s)$ is negative, the PI controller is designed with negative parameters to introduce a positive loop gain to the system. Thus, compensated open-loop gain $T_{OL}(s)$ of the outer voltage ripple feedback loop is expressed as,

$$T_{OL}(s) = G_{PCS}(s)G_{ZOH}(s)G_C(s) \tag{3-19}$$

By calculating the uncompensated open-loop TF (i.e., $T_{OLuc}(s) = G_{PCS}(s)G_{ZOH}(s)$), the $G_C(s)$ can be designed with frequency response methods. Figure 3.9 shows the bode plot of $T_{OLuc}(s)$ for different switching frequencies that are calculated based on parameters given in Table 3-1. The EA is designed in such a way that the crossover frequency of open-loop TF of the outer loop is at least 10 times lower than the minimum switching frequency present in the system. The uncompensated plant of the outer feedback loop is a non-minimum phase system with the characteristics of $G_{ZOH}(s)$. The transfer function of $G_{ZOH}(s)$ depends on the switching frequency of the converter. Hence, crossover frequency of the outer loop should be designed

much lower than the minimum expected f_S. Further, this will decouple inner boundary control dynamics from the outer feedback control loop. The minimum f_S of the buck converter prototype in Section 3.5 is considered as 1.12 kHz that is calculated based on the parameters given Table 3-1. Considering these guidelines and minimum f_S, EA is designed with K_P =0.2 and K_i=400 to obtain a crossover frequency of 33 Hz as shown in Figure 3.9.

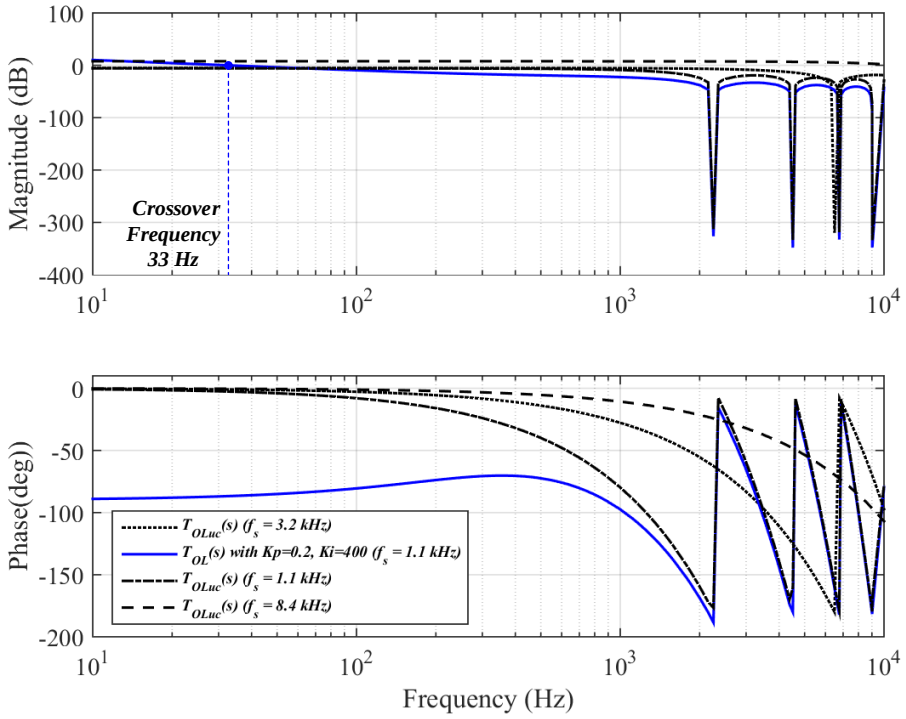


Figure 3.9 Frequency response of the outer loop gain with different switching frequencies.

If the cross-over frequency is designed closer to the switching frequency, the phase margin of the system will be lower, and the outer loop becomes less stable due to the low phase margin, as shown in Figure 3.10. Therefore, it is important to design the crossover frequency of open-loop TF of the outer loop at least 10 times slower than the minimum switching frequency present in the system to sustain the stability of the outer loop. The bandwidth of the outer feedback loop decides the response time of the k_D that compensates the output voltage ripple. Here, k_D is an additional gain factor that determines the correct switching surface.

Hence, the outer loop does not decrease the transient response time of the inner boundary controller. The outer loop bandwidth only has an effect during start-up transients since C_L is changed only when a new capacitive load is connected. However, the system still reaches the target operating point within two switching actions, and a specified output voltage ripple is achieved based on the outer loop bandwidth. The validity of above statements is confirmed by the experimental measurements in Section 3.5.

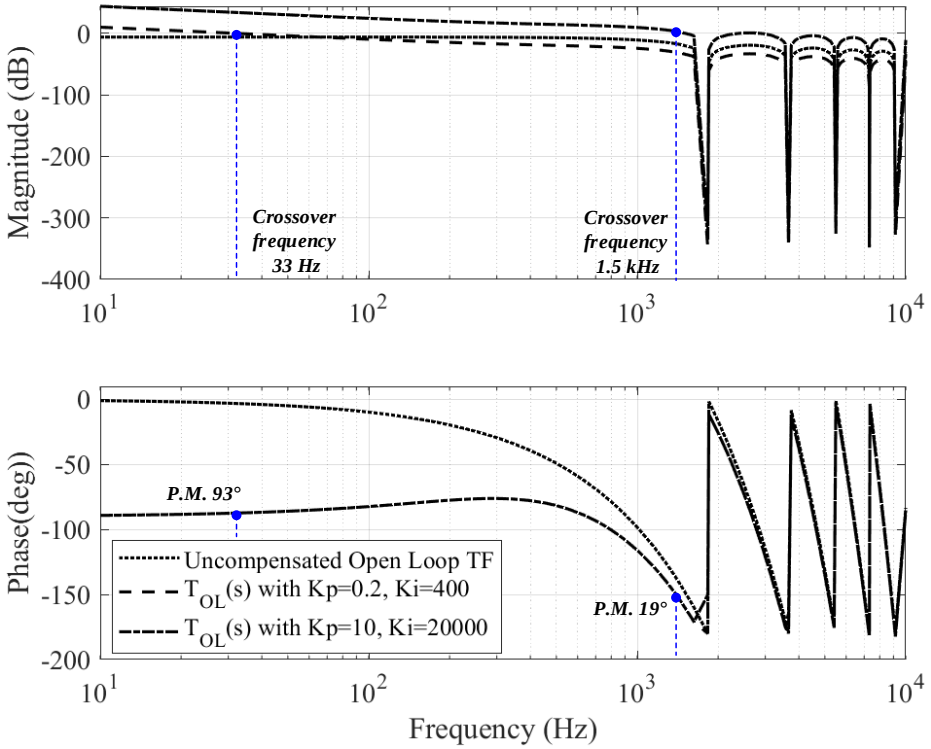


Figure 3.10 Frequency response of the uncompensated and compensated outer loop gain with different PI parameters.

3.3.4 Effect of Variation in Filter Parameters

The corrected switching laws represented in (3.10) and (3.11) are derived considering the addition of C_L and it has not addressed the deviation in filter parameters. If deviations are considered in L and C, they can be expressed as, $L' = L(1+\alpha)$ and $C' = C(1+\beta)$ where α

and β are the tolerances of L and C respectively. Substituting L and C values in (3.10) and (3.11) by $L^{'}$ and $C^{'}$, the switching ON and OFF criteria of σ_{cor}^2 can be expressed as,

$$v_{C,min} \leq -\left[\left(\frac{L}{2C}\frac{1}{v_S(\mathrm{t})-v_{ref}}\right)k_D'\right]i_C(\mathrm{t})^2 + v_C(\mathrm{t}) \text{ and } i_C(\mathrm{t}) < 0 \quad (3\text{-}20)$$

$$v_{C,max} \geq \left[\left(\frac{L}{2C}\frac{1}{v_{ref}}\right)k_D'\right]{i_C}^2 + v_C(\mathrm{t}) \text{ and } i_C(\mathrm{t}) > 0 \quad (3\text{-}21)$$

where $k_D' = \frac{(1+k_D)(1+\alpha)}{(1+\beta)}$.The outer voltage ripple feedback loop is still capable of determining the additional switching gain, k_D' which is directly corresponding to C_L, α and β of the real system.

Table 3-1 Parameter values used for the analysis of outer loop design.

f_S = 8.42 kHz		f_S = 3.25 kHz		f_S = 1.12 kHz	
Parameter	Value	Parameter	Value	Parameter	Value
v_S/v_{ref}	120 V/ 50V	v_S/v_{ref}	120 V/ 50V	v_S/v_{ref}	120 V/ 50V
L	3.5 mH	L	3.5 mH	L	3.5 mH
C	4.7 µF	C	4.7 µF	C	4.7 µF
Δ	0.5 V	Δ	2 V	Δ	2 V
C_L	10 µF	C_L	20 µF	C_L	200 µF

3.3.5 Average Output Voltage and Output Voltage Ripple

The expressions for average output voltage ($v_{C,Avg}$) and output voltage ripple are derived based on the steady-state trajectories with σ_{cor}^2.

$$v_{C,Avg} = v_{ref} + \frac{\left(\frac{L}{2\,C\,v_{ref}} - \frac{L}{2\,C\,(v_S - v_{ref})}\right)\frac{1}{1+k_D} - (k_2' - k_1')}{k_1' + k_2'}.\Delta \quad (3\text{-}22)$$

$$v_{ripple} = v_{Cmax} - v_{Cmin} = \frac{L\Delta}{C(1+k_D)(k_1'+k_2')}\frac{v_S}{v_{ref}(v_S - v_{ref})} \quad (3\text{-}23)$$

A detailed derivation of average output voltage and output voltage ripple expressions with conventional σ^2 can be found in [57]. A similar approach is used to derive (3.22) and (3.23). If k_1' and k_2' are ideal values, (3.22) and (3.23) can be simplified to;

$$v_{C,Avg} = v_{ref} \tag{3-24}$$

$$v_{ripple} = 2\Delta \tag{3-25}$$

3.4. Simulation Results

Simulations are carried out using PLECS™ to validate the proposed σ_{cor}^2 for a cascaded buck-boost system with (a) boost converter with open-loop control and (b) boost converter regulated as a CPL. The system parameters used in the simulation are listed in Table 3-2. Following assumptions are taken for PLECS simulations through out this thesis.

- Parasitic parameters on synchronous buck converter and their influence on the circuit has been neglected.
- Switches are modelled as ideal switches using resistive switch models and switching losses are neglected.

3.4.1 Boost converter with open-loop control

Figure 3.11 illustrates the steady-state converter trajectory on i_L-v_C state plane with the proposed σ_{cor}^2 and conventional σ^2, when a boost converter is acting as a load, and it is operated with open-loop control. It shows that the proposed σ_{cor}^2 regulates the output voltage at specified voltage band, whereas with σ^2, there is a significant error in output voltage ripple and runs into DCM. Transient performance results with both σ_{cor}^2 and conventional BC is shown in Figure 3.12 by changing the resistive load of the boost converter from 15 Ω to 7.5 Ω. Under the σ_{cor}^2, voltage band is accurately maintained at specified value as expected and

operating f_S is at 30.3 kHz. While with σ^2, there is a significant error in the voltage ripple due to inaccurate switching actions. The transient behavior of output voltage and current under both control schemes is similar. It can be observed that the output current response is slower and takes ~1.8 ms to reach steady-state condition. Since the boost converter is operated with open-loop control, the transient response depends on the cut-off frequency of the low pass filter (LPF) formed by C, C_L and L_B.

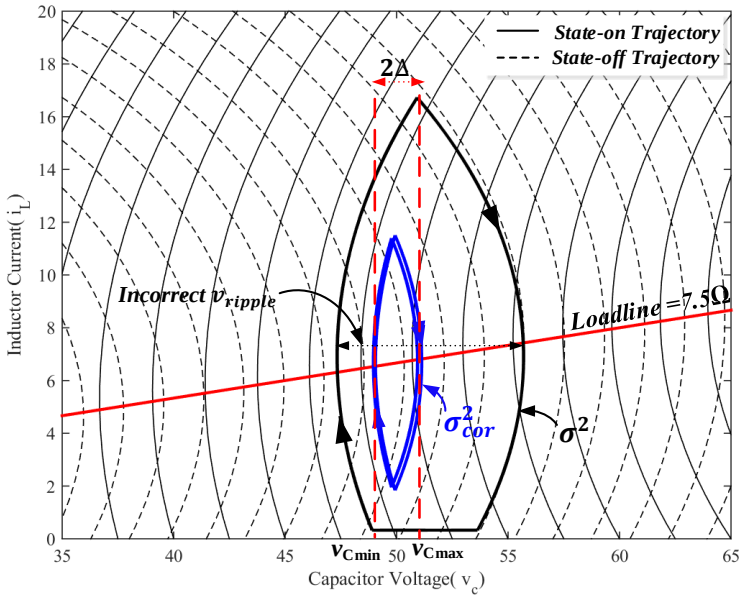
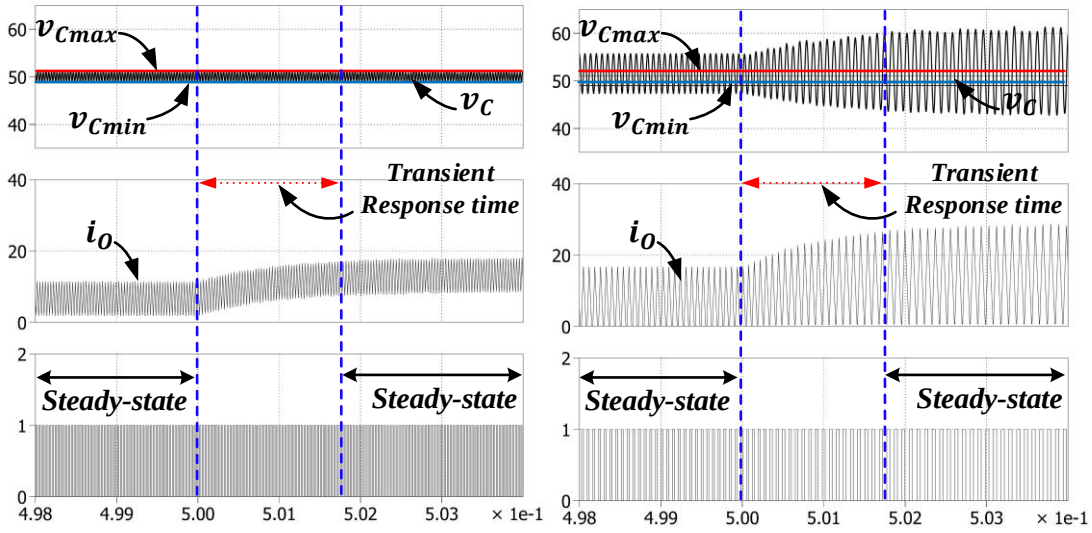


Figure 3.11 Steady-state system trajectories for σ^2 and σ^2_{cor} when boost converter with open loop control (R_L=50 Ω).

Table 3-2 Parameter values used in PLECS™ simulations.

BUCK STAGE		BOOST STAGE	
Parameter	Value	Parameter	Value
v_S/ Δ	120 V/ 1V	L_B	3.5 mH
v_{ref}	50 V	C_L	20 µF
L	0.1 mH	f_{S2}	50 kHz
C	1 µF	$d_{openloop}$	0.5
K_P, K_I	0.2, 400		

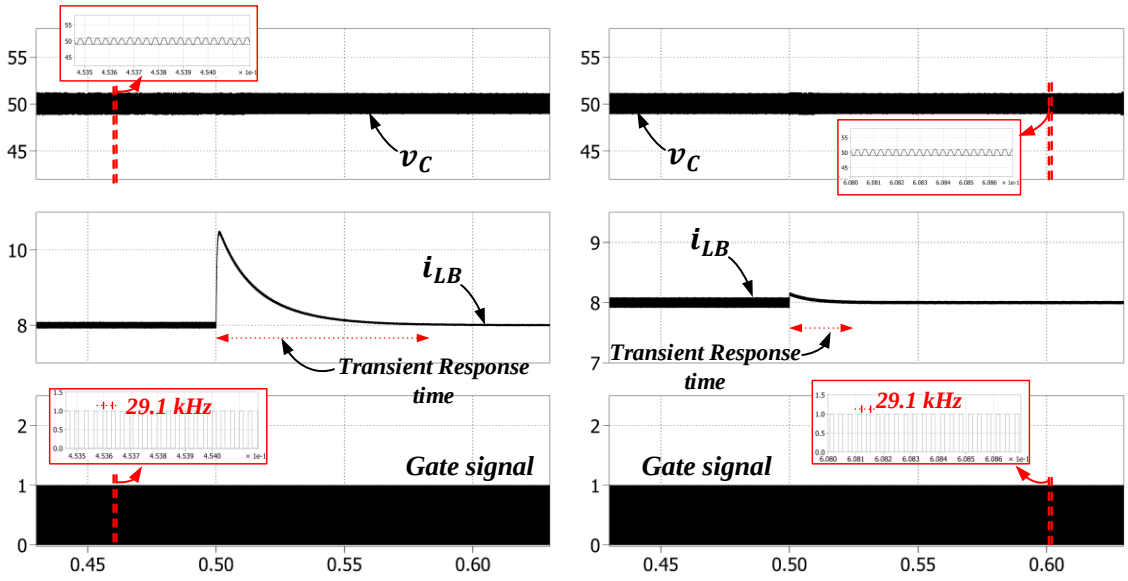


(a) (b)

Figure 3.12 Time-domain output waveforms for a boost-stage load transient (15 Ω to 7.5 Ω) with (a) σ_{cor}^2 (b) σ^2.

3.4.2 Boost converter as a constant power load

In case of constant power load, the input current of the boost converter must be tightly regulated, and its dynamic response will be relying on the control bandwidth of the boost-stage current controller. Figure 3.12 (a) and (b) show the output waveforms of the buck converter with σ_{cor}^2 when boost converter is regulated with a control bandwidth of ~700 Hz and 7 kHz, respectively. The response of the output voltage (v_C) after a load transient, is much faster due to boundary control, and it reaches steady-state within one or two switching actions while maintaining the voltage ripple at the specified value. As expected, the output current transient is much faster with higher control bandwidth system. Results show a good agreement with the theory.



(a) (b)

Figure 3.13 Time-domain output waveforms for a load transient when boost converter is regulated as CPL (15 Ω to 7.5 Ω) for a control bandwidth of (a) 700 Hz (b) 7 kHz.

3.5. Experimental Validation

In this section, the proposed control scheme is verified with a 250 W DC-DC buck converter prototype, and the experimental test setup is shown in Figure 3.14. The parameters of the cascaded buck-boost prototype are listed in Table 3-3. Control scheme is implemented using a Texas Instruments (TI) TMS320F28377S digital signal processor (DSP). The ADC is based on a 12-bit converter. The measured signals are sampled by the ADC and read by the control law accelerator (CLA). The CLA operates parallel to the main central processing unit (CPU) and has a low ADC sample to output delay. Thus, CLA extends the capabilities of the CPU by parallel processing, enabling faster system response and high-frequency control loops. The corrected boundary control and the voltage ripple measurement codes are implemented in interrupt service routine (ISR) running at 250 kHz, while error amplifier codes are

implemented in an ISR running at 12 kHz. The measured variables are i_L, i_C, v_C and v_S and all of them are sampled at 250 kHz. The proposed controller is evaluated with different loads, including resistive-capacitive parallel (R//C) loads and a boost converter and a dc electronic load to validate its performance.

Table 3-3 Key parameter values used in the experiments.

BUCK STAGE		BOOST STAGE	
Parameter	Value	Parameter	Value
v_S	120 V	L_B	3.5 mH
v_{ref}/Δ	50 V/ 2V	C_L	100 µF
L	3.5 mH	f_{S2}	10 kHz
C	4.7 µF	$d_{openloop}$	0.5
K_P, K_I	0.2, 400	R_L	25 Ω

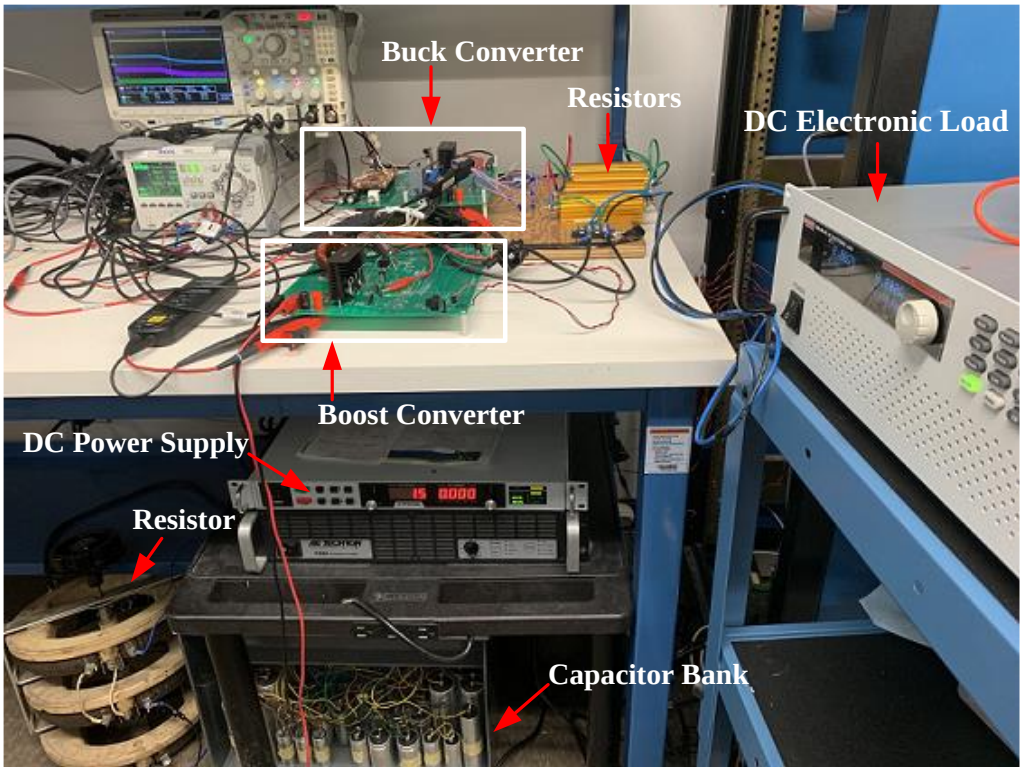
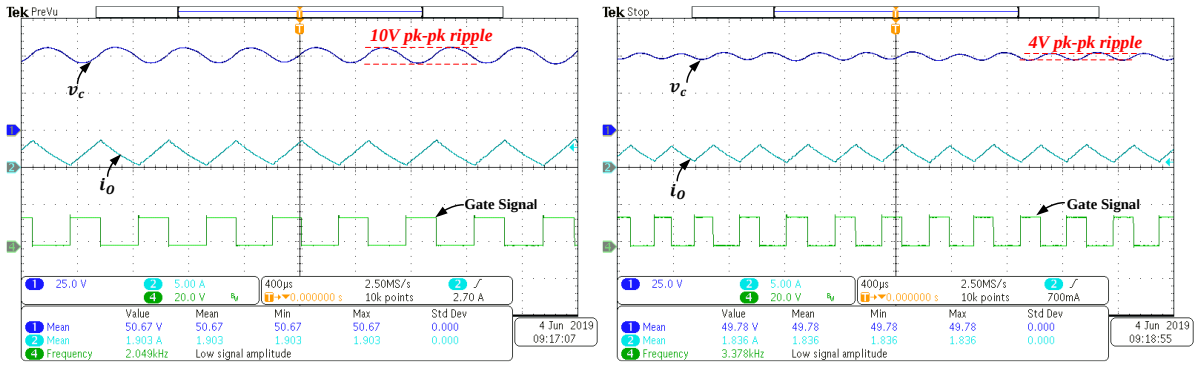


Figure 3.14 Experimental test setup.

3.5.1 Evaluation with R//C Loads

To evaluate the dynamic response of the proposed method under linear loads, the buck converter is operated with R//C loads. Figure 3.15 compares the steady-state waveforms of the buck converter with the proposed σ_{cor}^2 and σ^2. The converter is operated with a R//C load of 20Ω and 20µF. It is observed that under σ_{cor}^2, the output voltage can be regulated within the specified voltage band around a given reference.



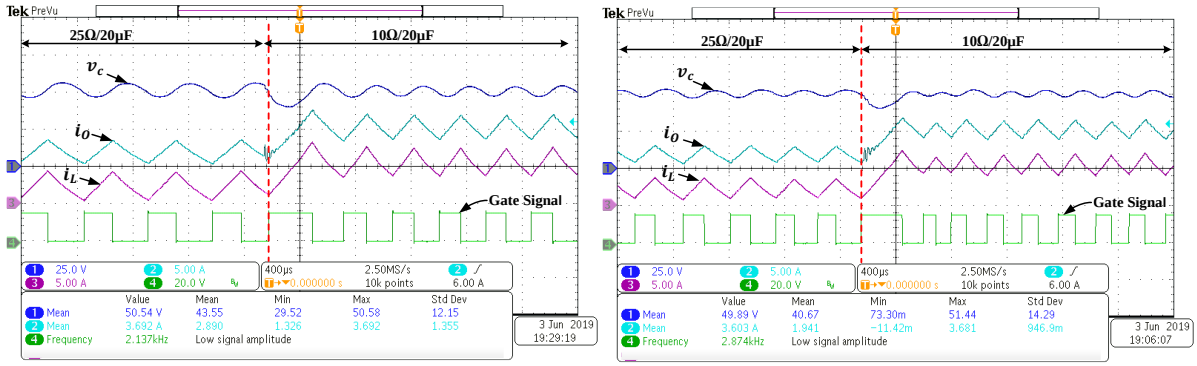
(a) (b)

Figure 3.15 Experimental results when system operating with R_L=25Ω, C_L=20µF, Δ =2 V and v_{ref}= 50V (a) with σ^2 (b) with σ_{cor}^2.

Figure 3.16 shows the system performance for a R//C load step-up change from 25Ω//20µF to 10Ω//20µF with both σ_{cor}^2 and σ^2. Noticed that the settling time is approximately ~400 µs with both controllers and only σ_{cor}^2 provides a constant voltage ripple size before and after the transient. This validates that the dynamic performance of σ_{cor}^2 is unaffected by the bandwidth of the outer feedback loop. Further, it verifies that the v_C is maintained within the specified band with σ_{cor}^2 with a greater accuracy.

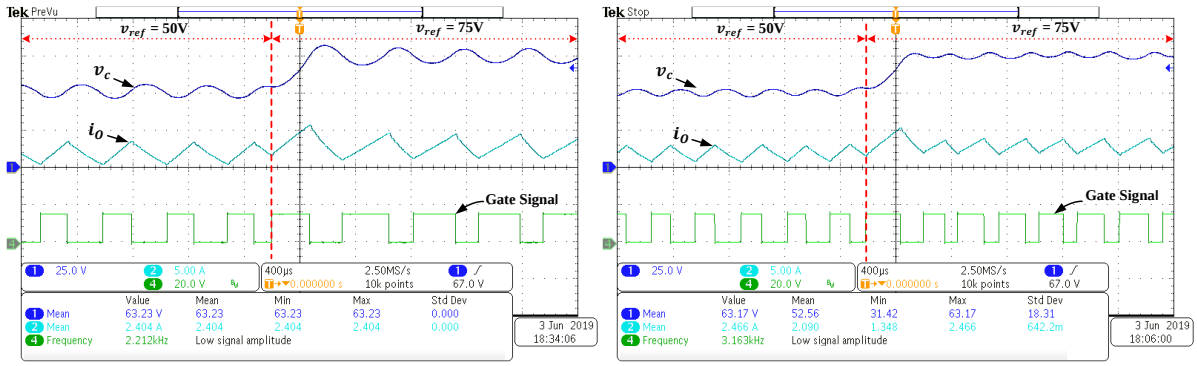
Figure 3.17 shows the transient performance of the system for a v_{ref} step change from 50 V to 75V with both σ_{cor}^2 and σ^2. The system performance with conventional σ^2 is

degraded significantly in terms of output voltage and current ripple as well as the switching frequency of the system. But, the system with σ_{cor}^2 operates as expected. Figure 3.18 (a) and Figure 3.18 (b) illustrate the converter trajectories on i_L-v_C state plane during the load transient and v_{ref} change respectively. The start-up transient response with σ_{cor}^2 in time-domain and state-plane are shown by Figure 3.19. Overall, the results presented reveal that σ_{cor}^2 provides a significant improvement in comparison with σ^2 for regulating the output voltage when a R//C connected as a load.



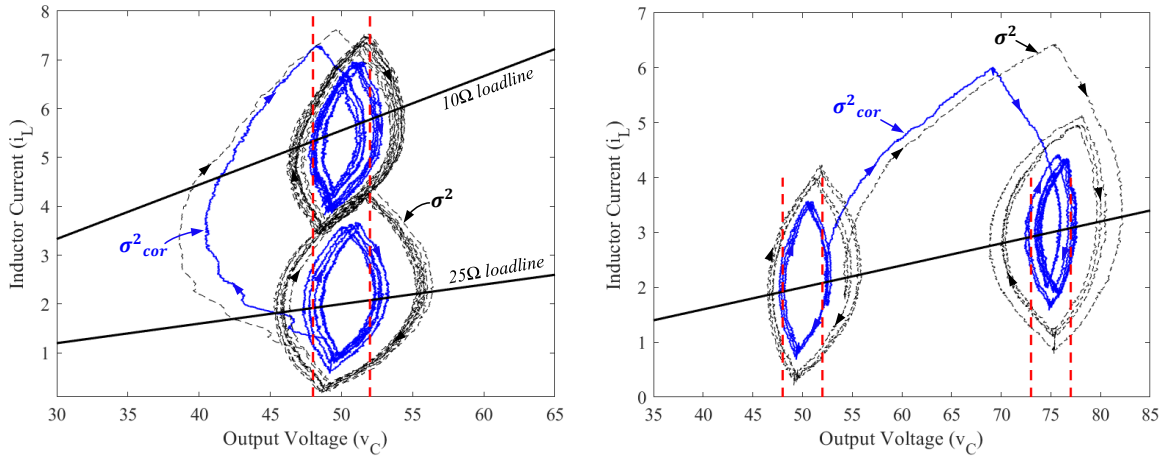
(a) (b)

Figure 3.16 Converter transient response when RC load is increased from 25Ω//20μF to 10 Ω//20μF with Δ =2 V and v_{ref}= 50V (a) with σ^2 (b) with σ_{cor}^2.



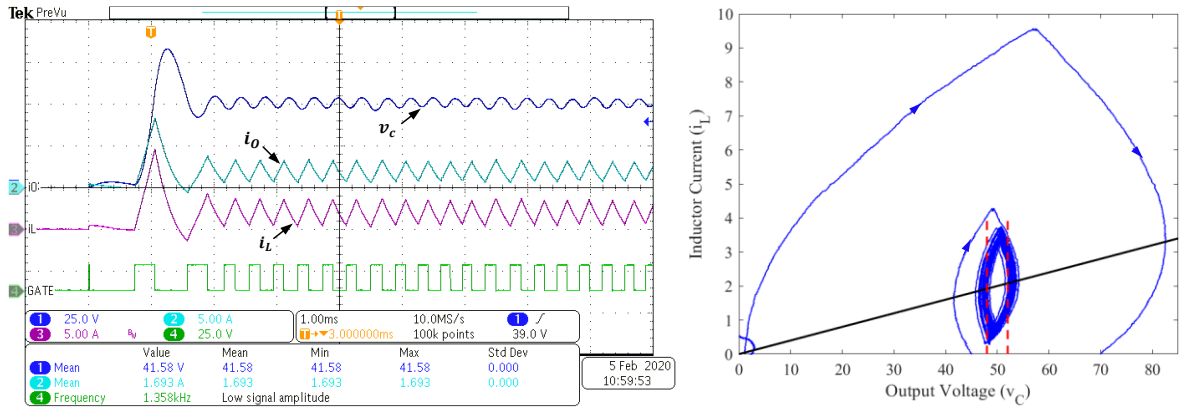
(a) (b)

Figure 3.17 Converter transient response for reference voltage from 50V to 75V with R_L=25 Ω , C_L=20μF, Δ =2 V and v_{ref}= 50V (a) with σ^2 (b) with σ_{cor}^2.



(a) (b)

Figure 3.18 Converter operating point trajectory during transients (a) load is increased from 25Ω//20μF to 10 Ω//20μF (b) reference voltage from 50V to 75V.



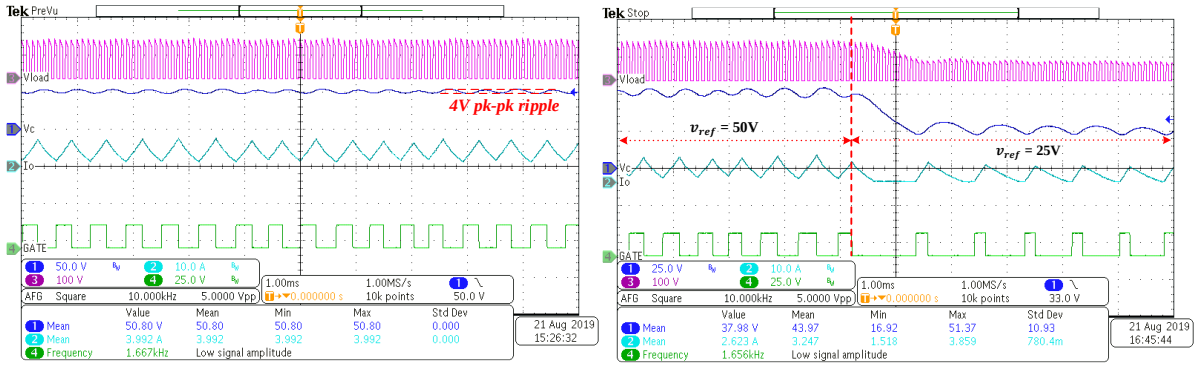
(a) (b)

Figure 3.19 Startup transient response results for R//C load of 25Ω//20μF (a) time domain. (b) state-plane.

3.5.2 Performance under Boost Converter as a Load

The steady-state operation of the cascaded buck-boost system is evaluated with the proposed control scheme, and results are shown in Figure 3.20 (a). It verifies that the output voltage ripple is closely tracked within the specified band. The measured switching frequency is about 1.66 kHz, which is close to the theoretical switching frequency of 1.57 kHz under this

testing condition. The boost converter is operated with open-loop control, and the parameters of the boost converter prototype are listed in Table 3-3. Figure 3.20 (b) shows the dynamic response results of the cascaded buck-boost system for a v_{ref} change from 50 V to 25 V. The v_C reaches the target operating point with two switching actions, and the recorded settling time is approximately 1.2 ms. It should be noted that transient response of i_O is limited by input filter dynamics of the boost converter as it is operated with open-loop control. Results showed that under proposed σ_{cor}^2, v_C can be regulated at specified voltage band. Moreover, the experimental results obtained closely match with the results from simulations.



(a) (b)

Figure 3.20 Experimental results with the boost converter (a) steady-state operation. (b) voltage reference change from 50 V to 25 V. (Δ =2 V, R= 25 Ω).

The operating switching frequency of the boost converter is changed from 20 kHz to 5 kHz to validate the proposed control scheme when the current ripple of the boost-stage inductor is ~20% of the rated DC current. Figure 3.21 shows that v_C is maintained at designed voltage band even when the current ripple of the boost stage inductor is ~ 30 % of the nominal dc value. This validates the theoretical approximations that are considered to derive the control law for cascaded buck-boost systems.

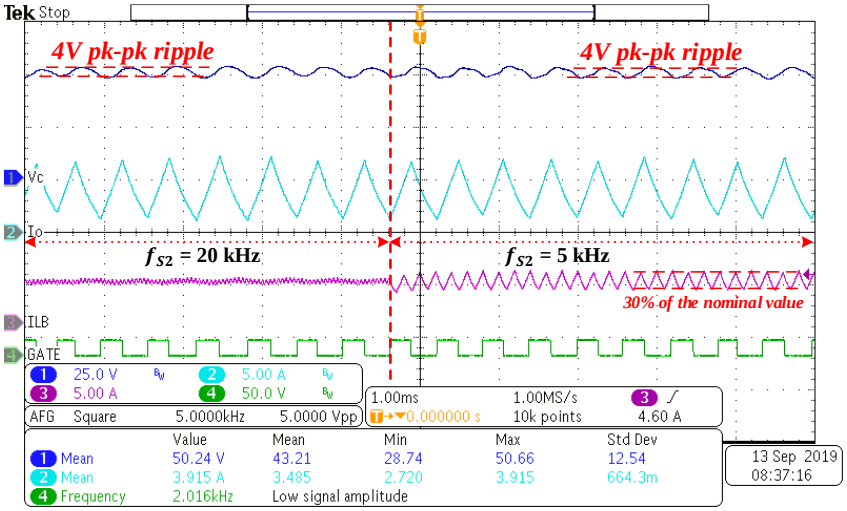
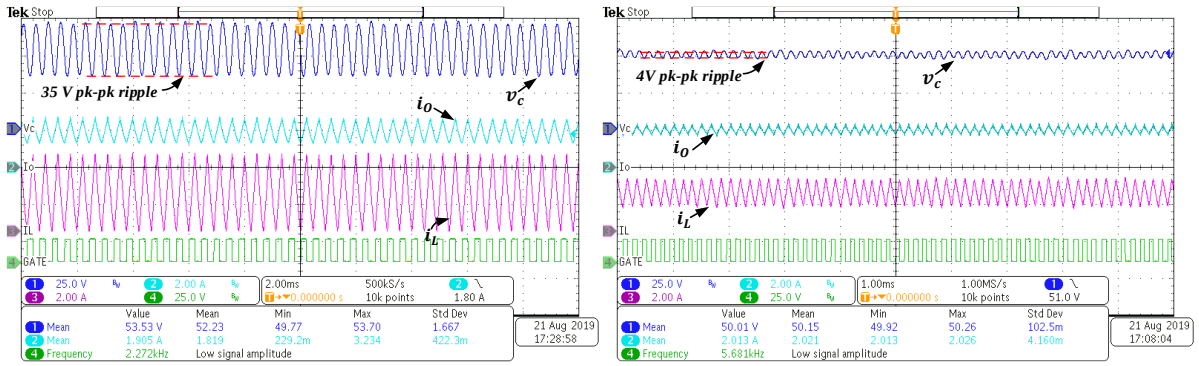


Figure 3.21 Experimental results with the boost converter when f_{S2} varied from 20 kHz to 5 kHz (Δ =2 V, R= 25 Ω).

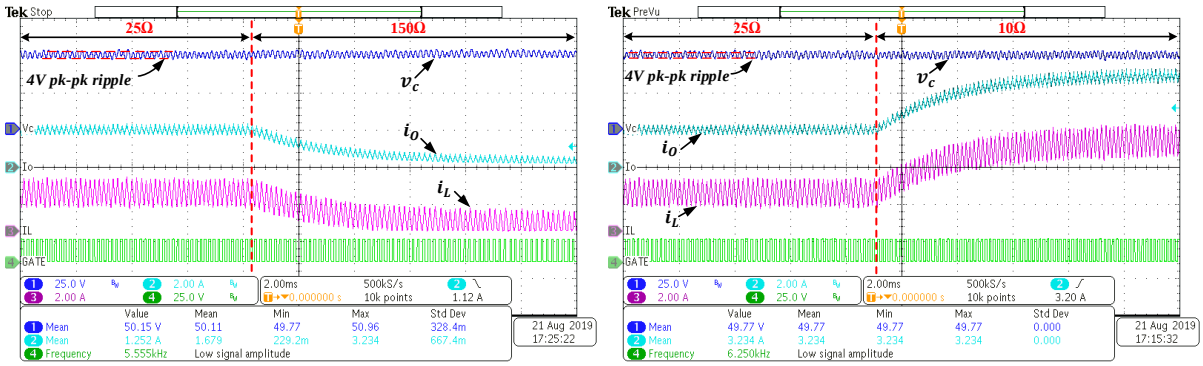
3.5.3 Performance with a DC Electronic Load

In order to validate the proposed method with an unknown non-linear switching load, the buck converter is connected to a commercial DC electronic load (KEIETHLY 2380-500-30). It is operated in constant resistance mode in this test setup. Figure 3.22 compares the steady-state operation for conventional σ^2 and proposed σ_{cor}^2. It is evident that the output voltage is not regulated significantly with σ^2 due to incorrect switching actions. The voltage ripple is 35 V that is much higher than the specified voltage ripple of 4 V, and the switching frequency is ~2.27. kHz. Contrarily, the output voltage is maintained within the specified band with σ_{cor}^2 with a greater accuracy. Load step-down and load step-up transients for the proposed method are shown in Figure 3.23. As expected, the transient response of the buck converter is limited by the dynamic response of the DC electronic load. The steady-state voltage ripple is maintained at 4 V at the given reference of 50 V. The recorded transient response time is approximately ~7 ms for both step-up and step-down transients.



(a) (b)

Figure 3.22 Experimental results for steady-state operation with DC electronic load (a) with σ^2 (b) with σ_{cor}^2.



(a) (b)

Figure 3.23 Experimental results using σ_{cor}^2 for load transients through DC electronic load (a) load step-down (25Ω -150Ω). (b) load step-up (25Ω -10Ω).

3.6. Discussion

Challenges in Implementation

The proposed BC scheme is demonstrated thoroughly in previous sections as an exciting prospect for controlling buck-based converters loaded with linear capacitive loads and boost-based switching converter loads with fast-dynamic characteristics. However, in practical

implementation, the BC-based buck converters face certain challenges in terms of achieving high switching frequency and thereby having better dynamic responses.

The σ_{cor}^2 requires instantaneous values of current and voltages to predict the next switching action. Thus, the main considerations for implementing BC scheme with high f_S are the sampling rate of measured signals required for control law and computation time. The TI™ TMS320F28377S digital signal processor (DSP) used in this work has 2 ADC channels with a maximum sampling rate of 3.5 Mega samples per second (Msps) for each channel. Four signals need to be measured for the proposed control architecture. Hence actual maximum sampling rate is reduced to 1.75 Msps. Considering the program length and execution time, experienced that the maximum operating frequency of the ISR is limited to 500 kHz. Thus, the target switching frequency will be limited to 10 kHz based on 50 points per cycle and does not meet the requirements mentioned in simulations. Hence high-performance ADC and computational power are required to operate the system with a higher switching frequency.

In simulations, there is no upper limit to the system operating f_S and as given in (3.14), it can be increased by minimizing LC filter parameters and Δ. Simulation results are provided in Section 3.4 with 30 kHz operating f_S to verify the proposed control theory under high switching frequency operation. This proven concept can be easily extended to achieve an ultra-fast response compatible with commercial PAs with the use of advanced hardware like ADC with high precision and high sampling rate, a Field Programmable Gate Arrays (FPGA) for implementing control law and use of Silicon Carbide (SiC) / Gallium Nitride (GaN) semiconductor switches. Dynamic performance comparison between boundary-controlled PA and commercial PA will be discussed in Section 5.4.3. Further, this controller can be easily

scaled up for applications requiring high power by applying this control scheme on a multiphase interleaved DC-DC converter.

3.6.1 Limitations of the Proposed Method

The proposed BC scheme is derived considering the fact that interaction of current ripple components with i_C due to the switching of load converter is negligible. This is true for non-linear switching loads such as boost-based converters as it has a negligible impact on i_C , as explained in Section. 3.2. However, if current ripple components led by load converter are significantly visible in i_C, the derived BC switching criteria contradicts the existing system, which leads to incorrect switching actions. Thus, the proposed corrected BC scheme does not guarantee to maintain the system performance as expected under all types of non-linear switching loads. Further, the source emulator's switching frequency and output current ripple will still depend on the load capacitance, C_L. As an alternative solution for this limitation, we recommend adding a second-stage LC filter between the voltage-mode source emulator and load converter to decouple high-frequency current ripple components led by load converter passing into the source emulator and vice versa. It will extend the proposed method for buck-derived DC source emulators with any non-linear switching load. The second-stage LC filter needs to be designed considering attenuation and fast dynamic response. This approach will be further discussed and presented in Chapter 6.

3.7. Summary

Boundary control techniques that depend on filter parameters and capacitor current needs a corrected switching surface to deal with capacitive and non-linear switching loads. Conventional boundary control with curved switching surface techniques is derived

considering the nominal filter parameters and constant load current. Hence, any discrepancies between the switching surface and real system parameters would lead to undesirable output voltage ripple and switching frequency. Thus, this chapter derived a BC with corrected second-order switching surface for buck-derived converters cascaded to second-stage boost converters with a capacitive input filter. The proposed corrected switching surface is proven to be applicable for buck converters cascaded to any linear load and non-linear switching loads that have a negligible impact on the filter capacitor current from the current ripple components generated due to switching of the second-stage converter.

An innovative outer feedback loop is implemented to determine the corresponding switching criteria gain factor, which accounts for unknown load capacitance or filter parameter deviations while maintaining the output voltage ripple at a specified voltage band. A simple methodology is introduced to detect the output voltage ripple amplitude using the instantaneous measurement of the output voltage and the inductor current. The proposed control scheme has been validated by both simulations and experimental results under different loads, including boost converter, R//C load and dc electronic load. Results showed that the proposed VM PA maintains the output voltage ripple at the specified voltage band and reaches a steady-state within 400 µs after sudden transients. The proposed σ_{cor}^2 will be applied for controlling the v_C of PCS of the DC source emulator in the rest of the thesis.

Chapter 4

A Fast-dynamic Voltage-Mode PV Emulator with Instantaneous Output Impedance Matching Controller

The work presented in this chapter is the result of original work published under I. D. G. Jayawardana, C. N. M. Ho, M. Pokharel and G. E. Valderrama, "A Fast-Dynamic Control Scheme for a Power-Electronics-Based PV Emulator," *IEEE Journal of Photovoltaics*, vol. 11, no. 2, pp. 485-495, March 2021. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2017.

In this chapter, a standalone voltage-mode PV emulator based on a synchronous buck converter with a novel reference generation method is introduced for testing PV converters with fast MPPT algorithms. A universal reference generation method based on output impedance measurement is developed to suppress the oscillatory reference problem in PV emulators and provide accurate emulation in all regions of the I-V characteristics curve. The BC scheme proposed in Chapter 3 is used as the inner control loop to regulate the converter at

a given reference within a short time. This work also investigates the interdependency between RGA and the inner control loop to identify its limitations related to dynamic performance.

4.1. Introduction

Among nonlinear DC source emulators, PV emulator critically demands fast transient responses to replicate dynamic characteristics close to real PV arrays and test applications with fast MPPT algorithms. However, existing switch-mode PVE designs have shown much slower response time and limited bandwidth compared to linear PA-based PVEs, as highlighted in Chapter 2. The dynamic performance of switch-mode PVE based on buck-derived converters is mainly governed by the inner control loop bandwidth and relies on LC filter values, switching frequency and voltage conversion ratio as well. Thus, a high-bandwidth control algorithm is necessary to achieve fast-dynamic characteristics.

Moreover, in PVEs, the outer loop RGA plays a significant impact on the accuracy and response time as well as PVE's ability to emulate the entire I-V curve. As described in Section 2.2.3, the DRM is the most used outer loop RGA, which creates an oscillatory reference signal in one region of operation (i.e., in CVR with current-mode control and CCR with voltage-mode control) as feedback signal always has an ac ripple. Further, in DRM, the reference generation loop is coupled with the inner control loop response. Hence, the response time of the reference signal is limited by the inner loop bandwidth. To minimize the oscillatory reference signal with DRM, typically linear controllers (i.e., PI, PID) with a lower control bandwidth are used. It eliminates the effect of high-frequency oscillations but at the expense of the dynamic performance of the PVE. Therefore, one aim of this chapter is to develop a universal RGA for standalone PVEs using load resistance feedback to make it independent

from the inner control loop response and achieve a stable and fast convergent reference signal in both CCR and CVR regions of the I-V curve.

In this chapter, a buck-based PV emulator with a comprehensive voltage-mode control scheme is developed to achieve fast-dynamic responses and emulate accurately in all regions of the I-V characteristic curve. The proposed PV emulator includes a synchronous DC-DC buck converter as the power conversion stage and utilizes the σ_{cor}^2 proposed in Chapter 3 as its inner controller to regulate the converter at a given voltage reference within a short time. A novel instantaneous output impedance matching controller is introduced as the RGA to generate the voltage reference signal based on load resistance feedback. In contrast to DRM, the IOIM controller suppress the oscillatory reference problem and generates a stable voltage reference throughout the I-V curve. Further, it has the advantage over the resistance comparisons method [8], [33] in terms of convergent speed, and its bandwidth is mainly dependent on the integral gain and the operating point in the I-V curve. The idea of employing non-linear controller like σ_{cor}^2 is to provide robustness against switching converters and achieve high control bandwidth, enabling PVE's usefulness in testing real MPPT converters with a convergence speed of tens of milliseconds [48], [49].

The chapter is organized as follows. Section 4.2 describes the comprehensive system architecture of the standalone PVE with IOIM controller, including the power stage design considerations. A detailed small-signal model of the PVE is presented in Section 4.3 to design the IOIM control loop and prove that the reference generation loop is independent of PCS and the inner control loop. In Section 4.4 and 4.5, simulation and experiment results of the proposed PVE under steady-state operation and different transient conditions, including load step change and irradiance level changes with linear loads as well as an MPPT micro-inverter are presented.

A 130 W, 60 V input DC-DC synchronous buck converter prototype is built to verify the proposed control scheme.

4.2. System Description and Control Strategy

The structure of the proposed PVE is shown in Figure 4.1. The power conversion stage is formed by a synchronous DC-DC buck converter that operates in VM control.

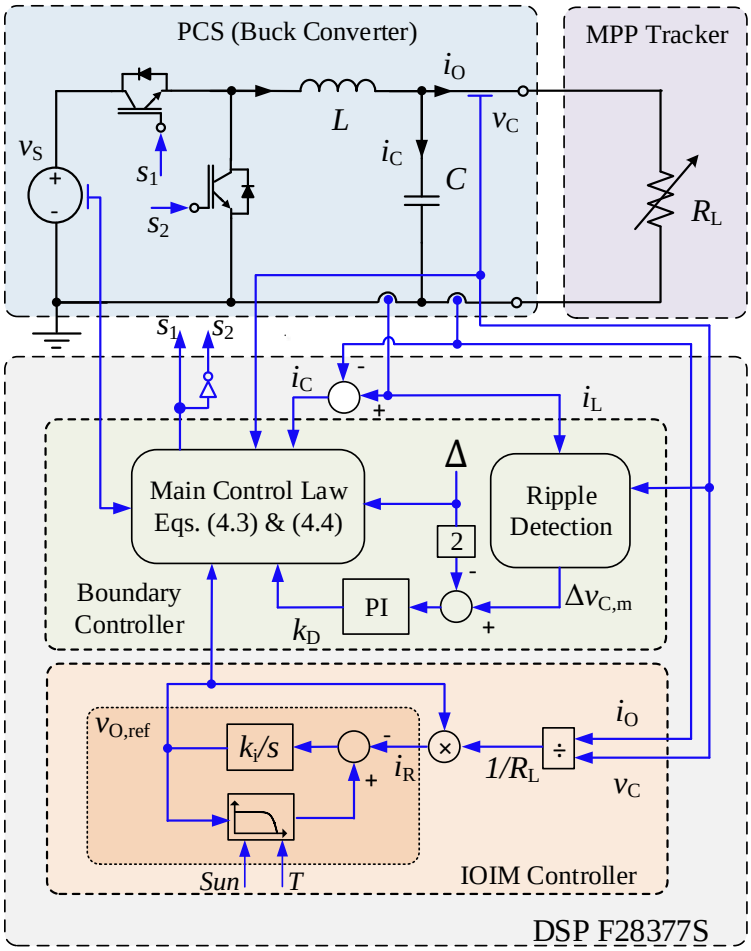


Figure 4.1 Architecture of the PVE with the proposed control scheme.

The proposed controller consists of IOIM controller as the reference generation block and inner control loop to regulate capacitor voltage at a given voltage reference (v_{Oref}). Firstly,

output current (i_O) and voltage (v_C) are sensed and fed into the IOIM controller to obtain the load information (R_L) instantaneously. In IOIM, current correspond to both PV model, and load resistance are matched through integral controller action while generating the v_{Oref}. The conventional V-to-I look up table is used to implement the PV model. Boundary control with corrected second-order switching surface is employed as the inner controller, which determines switching instants for S_1 and S_2 in PCS.

4.2.1 Instantaneous Output Impedance Matching Controller

The task of the RGA method is to determine the operating point current/voltage reference on the I-V characteristics curve based on load characteristics feedback signal (i.e., current/voltage/resistance). The output characteristics of a PV module depend on load condition, and its operating point must satisfy both load and I-V characteristics. From a mathematical point of view, the operating point can be identified by solving the non-linear I-V characteristics equation of a single-diode PV model given by (4.1), and the load characteristics equation given by (4.2).

$$I = I_{PH} - I_{on}\left[exp\left(\frac{V+R_sI}{aV_t}\right) - 1\right] - \left(\frac{V+R_sI}{R_p}\right) \tag{4-1}$$

$$I = \frac{V}{R_L} \tag{4-2}$$

The above parameters are already defined in Section 2.2.4. Due to the implicit non-linear characteristics of (4.1), solving both equations numerically would slow down the reference generation process. Therefore, an instantaneous output impedance matching controller based on load resistance feedback is proposed in this work, as shown in Figure 4.2 below. In IOIM, a control approach is taken to solve these two equations and extract v_{Oref} for a measured load

resistance. As shown in Figure 4.2, current corresponds to the load line (i_R) and current corresponds to PV model (i_{Oref}) is compared to determine impedance matching voltage through an integral controller. The i_R is obtained by multiplying v_{Oref} and R_L. PV model is implemented using an I-V LUT that used to generate i_{Oref} for a given v_{Oref} feedback signal. The LUT approach is chosen over an approximate explicit I-V equation [79] for its easy implementation and to minimize the computational burden on the microcontroller.

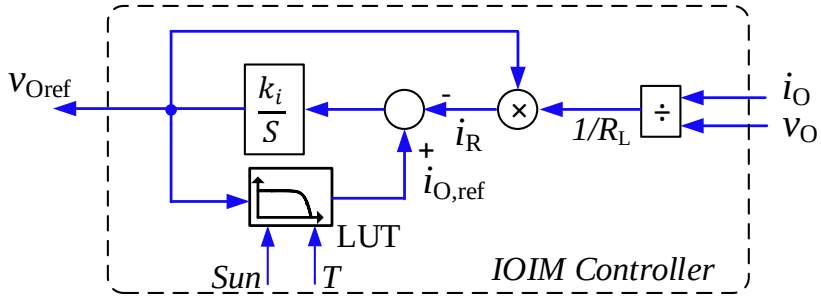


Figure 4.2 IOIM controller for voltage reference generation.

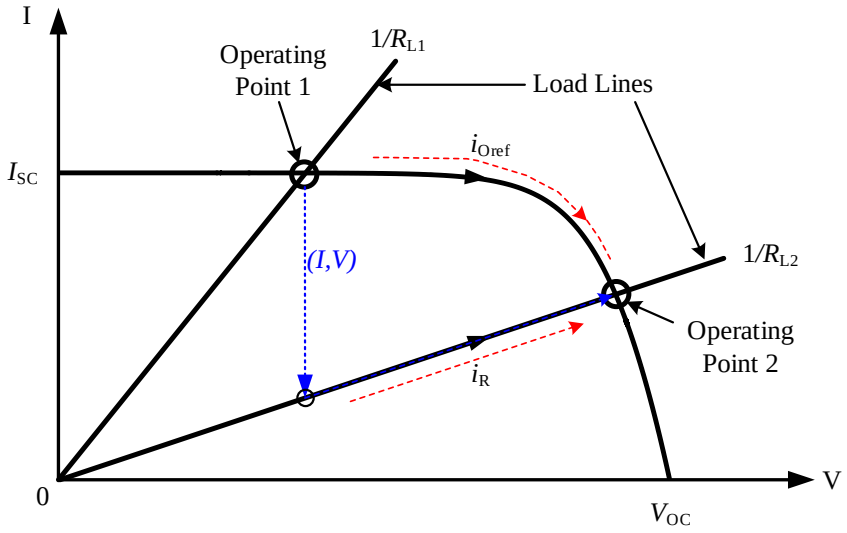


Figure 4.3 Trajectory of control parameter under a load step up on I-V plane.

Figure 4.3 shows the trajectory of i_R and i_{Oref} when load is changed from R_{L1} to R_{L2}. Controller moves both i_R and i_{Oref} towards the new operating point until the steady-state error

is zero. The IOIM controller guarantees a stable reference signal irrespective of the operating region in I-V curve, and the bandwidth of the IOIM controller can be adjusted mainly through the integral gain (k_i). Design procedure for the IOIM controller is presented in Section 4.3. Further, the IOIM control technique also can be used to generate a current reference for a PVE operated in current-mode as shown in Figure 4.4. Hence, this technique can be easily adopted for both CM and VM PV emulators depending on the requirement.

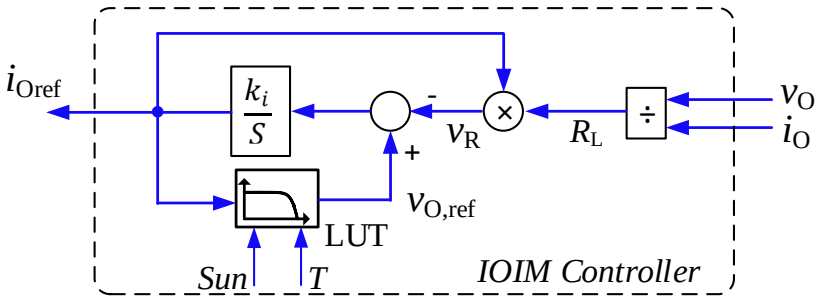


Figure 4.4 IOIM control for current reference generation.

4.2.2 Inner Control Loop Design

A stable voltage reference is determined by IOIM within a short time; a fast-dynamic controller is required to regulate v_C at the reference value. The load of the PVE is typically a non-linear boost-based switching converter and has a large input capacitor, C_L to filter the high-frequency switching components. Hence, σ_{cor}^2 presented in Chapter 3 is chosen as the inner loop controller for achieving faster response time and robust operation with non-linear switching loads. The switching criteria of σ_{cor}^2 for the buck converter and its detailed design procedure, including the outer voltage ripple feedback loop and ripple measurement block, are given in Chapter 3. The Turn ON and OFF criteria are formulated as below,

Switch ON Criteria (S_1=1 and S_2=0)

$$v_C \leq v_{C,min} + k_1[1 + k_D]{i_C}^2 \qquad \& \qquad i_C < 0 \tag{4-3}$$

Switch OFF Criteria (S1=0 and S2=1)

$$v_C \geq v_{C,max} - k_2[1 + k_D]{i_C}^2 \qquad \& \qquad i_C > 0 \tag{4-4}$$

where $v_{C,min} = v_{Oref} - \Delta$, $v_{C,max} = v_{Oref} + \Delta$, $k_D = C_L/C$, $k_1 = \frac{L}{2C}\frac{1}{v_S - v_{Oref}}$ and $k_2 = \frac{L}{2C}\frac{1}{v_{Oref}}$.

The σ_{cor}^2 requires instantaneous values of v_S,v_C, i_C, Δ and k_D to determine the switching actions. The value of k_D is determined by an outer feedback loop, as shown in Figure 4.1. The error amplifier generates the required k_D value based on the voltage ripple error, which is calculated by taking the difference between specified peak-to-peak voltage band (2Δ) and peak-to-peak ripple of v_C ($\Delta v_{C,m}$). The detailed design procedure for the outer feedback loop is provided in Chapter 2. The ripple magnitude of v_C is measured by using i_L and v_C. The control law derived is valid for converter operating in both continuous conduction mode (CCM) and DCM [56]-[58]. Hence, PVE can operate in open circuit voltage output. Further, synchronous buck converter topology allows regulating system at open circuit condition. However, PVE would not be able to operate in short circuit current output as this is a voltage output converter. The minimum output voltage will be decided by considering the minimum duty ratio (d) that can be implemented and the peak-to-peak voltage ripple.

4.2.3 LC Filter Design Considerations

The filter inductor value, *L* is designed by considering the design specifications of the PVE to allow a maximum peak-to-peak inductor current ripple (Δi_{Lmax}) and to maintain a

desired switching frequency range. The switching frequency of the PVE is varying under σ_{cor}^2, and as per (3.14), it will be dependent on LC filter values, voltage conversion ratio, Δ and load capacitance. The Δi_{Lmax} can be determined based on the steady-state characteristics of the buck converter as given below,

$$\Delta i_L = v_S d(1-d)/(Lf_S) \tag{4-5}$$

The variation in f_s and Δi_L with L can be determined from (3.14) and (4.3). The range of C_L and v_C are key specifications in selecting the inductor value that would maintain desired current ripple and f_S range. Figure 4.5 shows the variation of both f_S and Δi_L with L at upper and lower bound conditions for given Δ and C. It provides a guideline to determine the inductor value for a specified current ripple and desired f_S range. The upper bound condition for f_S is determined when C_L is minimum and d=0.5 while lower bound of f_S is determined when C_L is maximum and $d(1-d)$ is minimum. The current ripple will be at a maximum at the lower boundary condition of f_S and vice versa.

The output capacitance is typically selected by considering the effect of output voltage ripple, inductor current ripple and transient load response capability of the capacitor under an extreme transient from maximum load to no load. This yields,

$$C_{min} = \Delta i_{Lmax}/[8f_s.(2\Delta)] \tag{4-6}$$

$$C_{min} = L * I_{L,peak}/(V_{OS}^2 - v_O^2) \tag{4-7}$$

where $I_{L,peak}$ is the maximum peak current of the inductor, V_{OS} is the output voltage overshoot at maximum load. Both (4.6) and (4.7) are taken into consideration for selecting the capacitance.

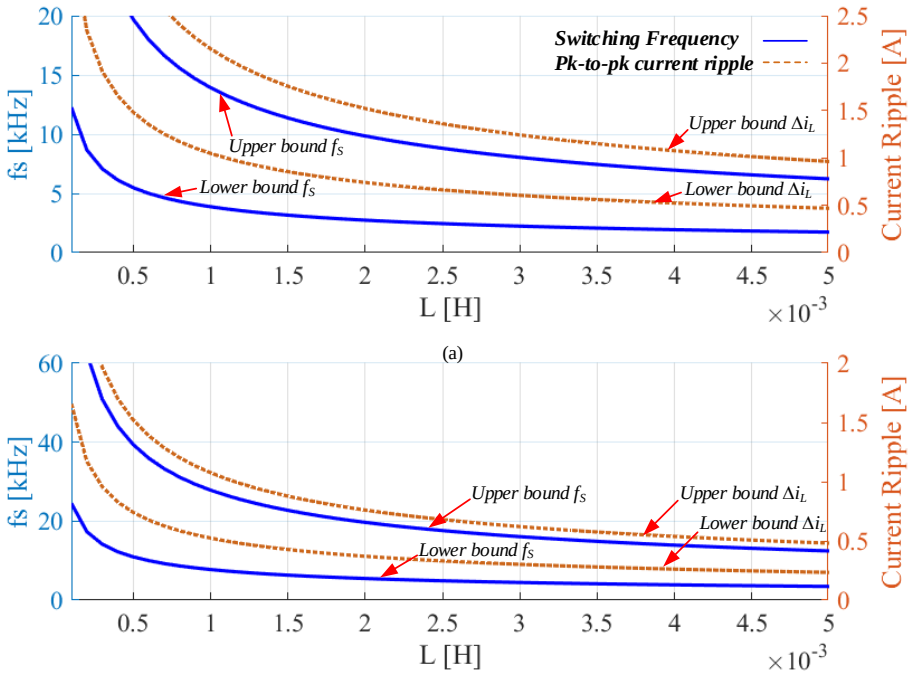


Figure 4.5 Variation of f_S and Δi_L with L for upper bound condition for f_S (C_L=0, d= 0.5) and lower bound condition for f_S (C_L=30µF, d= 0.16) (a) Δ =1 V (b) Δ= 0.25 V.

4.3. System Modelling and Analysis

This section aims to derive the small-signal model of the proposed PVE to prove that the reference generation block is decoupled from PCS and the inner control loop. The analysis is done considering a resistive load at the output. First, the small-signal relationships based on load resistance and voltage reference will be developed by considering the load resistance (r_L) as an input variable to the system. In the Laplace domain, the following formulas can be derived by applying Ohms law for the proposed PVE shown in Figure 4.1.

$$v_C(s) = r_L(s) i_O(s) \tag{4-8}$$

$$v_{Oref}(s) = r_L(s) i_R(s) \tag{4-9}$$

By introducing small-signal perturbations in (4.8)-(4.9), the relationship among small-signal terms of v_C (Δv_C), i_O (Δi_O), r_L (Δr_L) and v_{Oref} (Δv_{Oref}) are derived as,

$$\Delta r_L(s) = \frac{1}{I_O}\Delta v_C(s) - \frac{R_L}{I_O}\Delta i_O(s) \tag{4-10}$$

$$\Delta i_R(s) = \frac{1}{R_L}\Delta v_{Oref}(s) - \frac{I_R}{R_L}\Delta i_O(s) \tag{4-11}$$

where R_L, I_O, I_R are the DC terms of r_L, i_O, i_R respectively. To determine the transfer function between Δi_{Oref} and Δv_{Oref}, the linearized model of PV is required. The linear model of PV is described by the line tangent to the I-V characteristic curve at the linearization point (V_{pv}, I_{pv}) [134], i.e.,

$$\Delta i_{Oref} = \left(I_{pv} - g_{pv}V_{pv}\right) + g_{pv}\Delta v_{Oref} \tag{4-12}$$

where g_{pv} is the linear gain of the I-V curve at a given operating point. It is obtained by partially differentiating (4.1) with respect to voltage and given by (4.13).

$$g_{pv}\left(V_{pv}, I_{pv}\right) = \frac{\Delta i_{Oref}(s)}{\Delta v_{Oref}(s)} = -\frac{\frac{I_O}{aV_t}exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right)-\frac{1}{R_{sh}}}{1+\frac{I_O R_S}{aV_t}exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right)+\frac{R_S}{R_{sh}}} \tag{4-13}$$

The PV module parameters required for (4.13) are determined using an iterative method presented in [32]. This allows extracting parameters based on the manufacturer's datasheet. The key parameters of the PV module (BP365, 65 W) under standard test conditions (STC) are tabulated in Table 4.1. The TF between Δi_R and Δv_{Oref} can be derived by utilizing the PV model in (4.13) to the IOIM control architecture shown in Figure 4.2, which yields,

$$\Delta v_{Oref}(s) = G_{IOIM}(s)\Delta i_R(s) \tag{4-14}$$

where $G_{IOIM}(s) = \frac{-k_i/s}{1-(k_i/s)g_{pv}}$.

Table 4.1 Parameters of the BP365 PV Module at 25 ^{0}C, 1000 W/m^2

Parameter		Value
Maximum power	P_{max}	65 W
Short circuit current	I_{SC}	3.99 A
Open circuit voltage	V_{OC}	22.1 V
Voltage at P_{max},	V_{MPP}	17.6 V
Current at P_{max}	I_{MPP}	3.69 A
Temperature Coefficient of V_{OC}	K_V	-(80±10) mV/ºC
Temperature Coefficient of I_{SC}	K_I	(0.065±0.015)% / ºC
Number of cells in series,	N_S	36
Reverse saturation current of the diode	I_{on}	7.41984e^{-10} A
Equivalent series resistance	R_S	0.444
Equivalent parallel resistance	R_P	*204.02*
Diode ideality constant	a	*1.067635*

The TF of the inner BC loop scheme is often considered to be a unity gain due to its faster response. However, in this model, the TF of the inner BC loop is estimated based on the experimental results from the gain/phase analyzer. It is noticed that the closed-loop TF of the inner BC loop can be approximated as a low pass filter with a cross-over frequency of switching frequency. Thus, it is given by,

$$G_{inner}(s) = \frac{\Delta v_C(s)}{\Delta v_{Oref}(s)} = \frac{1}{1+\tau_{fs}s} \tag{4-15}$$

where $\tau_{fs} = 1/2\pi f_S$. The validity of this approximation is confirmed in Section 4.5.2.2 using the experimental frequency response results of the inner loop. The control block diagram of PVE, including the reference generation loop and boundary-controlled PCS, can be derived with small signal relationships that are given by (4.10), (4.11), (4.14), (4.15), and the derived control block diagram is shown in Figure 4.6.

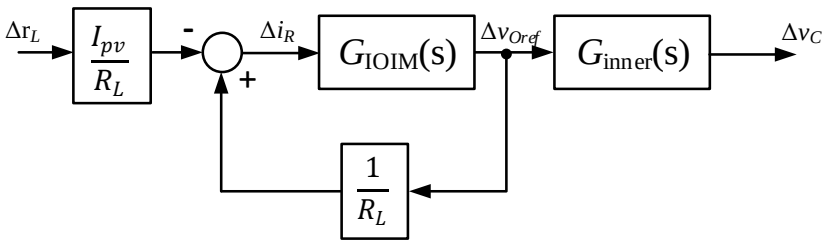


Figure 4.6 Control block diagram of the proposed PVE.

From Figure 4.6, the loop gain of the IOIM control loop is derived as follows:

$$G_{OL_{IOIM}}(s) = \frac{\Delta v_{Oref}(s)}{\Delta r_L(s)} = \frac{-G_{IOIM}(s)}{R_L} \tag{4-16}$$

The closed-loop TF of the reference generation loop ($G_{CL\_IOIM}(s)$) can be derived as below,

$$G_{CL_{IOIM}}(s) = -\frac{I_{pv}}{R_L}\frac{G_{IOIM}(s)}{1-\frac{G_{IOIM}(s)}{R_L}} \tag{4-17}$$

From (4.16) and (4.17), it is evident that the IOIM control loop is independent of $G_{inner}(s)$.

Table 4.2 Key system parameter values used in simulations.

Parameter	Value	Parameter	Value
v_S / Δ	60 V/ 0.25 V	f_S	7.7 kHz - 27 kHz
L	1 mH	C_L	0-30 µF
C	4.7 µF	Δi_L	0.5- 1 A
v_O	10 - 44.2 V	K_P, K_I	0.2, 400

To validate the derived small-signal model of the reference generation loop, the frequency response of $G_{CL\_IOIM}(s)$ is compared with AC sweep results from PLECS™ simulations. In Figure 4.7, the closed-loop frequency response of the developed mathematical model is compared with AC sweep results from PLECS™ for three different operating points

to validate the model in entire regions of the I-V curve, including CCR, CVR and MPP. The system parameters used in the simulation is listed in Table 4.2.

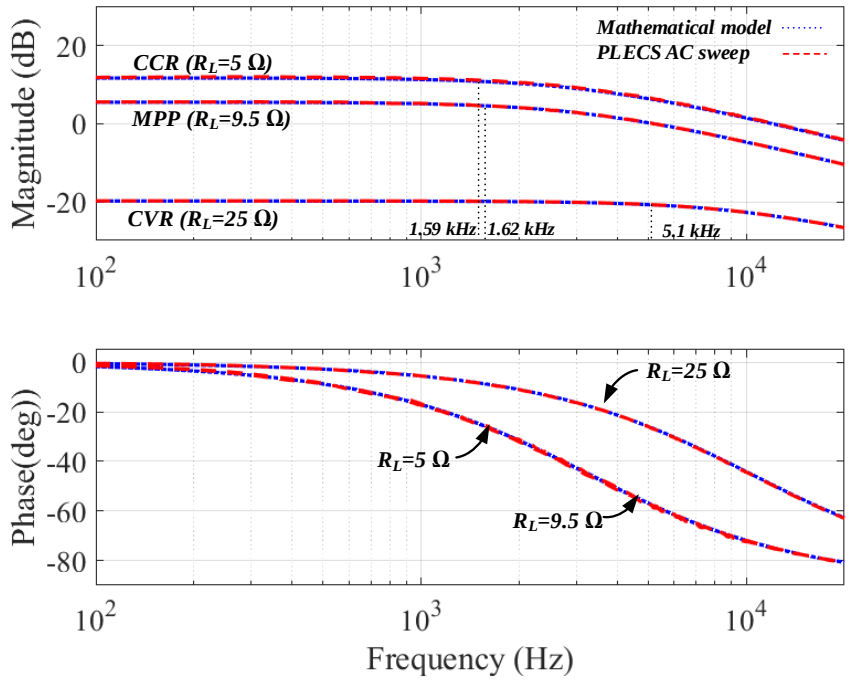


Figure 4.7 Closed-loop bode plot of IOIM control loop with k_i =50000.

Results in Figure 4.7 exhibit a close match, thus, validates the small-signal model derived for the reference generation loop. The IOIM control loop's bandwidth should be designed lower than the bandwidth of the BC loop to filter out switching frequency ripple components from the instantaneous impedance measurement. Hence, the maximum bandwidth of the IOIM should be chosen lower than the lowest f_S of the PVE to avoid ripple components passing into the IOIM control loop. Further, for a given k_i, the bandwidth of IOIM control loop will vary according to the value of g_{pv} that is dependent on the operating point in the I-V curve. As shown in Figure 4.7, the closed-loop bandwidth of the IOIM controller will be highest in CVR. Therefore, the integral gain should also be designed by taking that PVE operates at a point in CVR to generate a stable reference signal throughout the I-V curve.

Figure 4.8 shows step responses of the IOIM control loop for different k_i under above mentioned operating points. Moreover, Table 4.3 provides the closed-loop bandwidth of the IOIM controller for different k_i values.

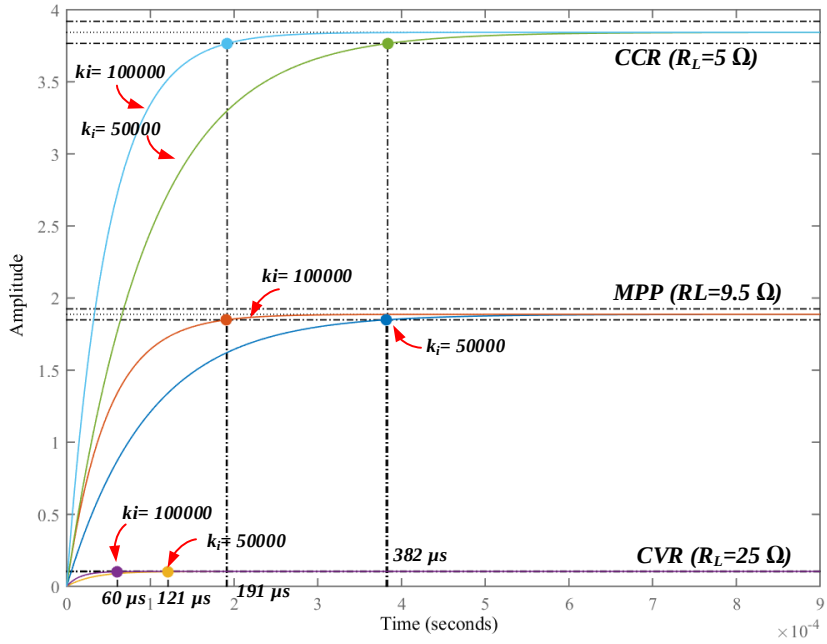


Figure 4.8 Step response of IOIM control loop with k_i=50000 and k_i=100000.

Table 4.3 Dynamic Characteristic of IOIM Control Loop

k_i	Closed-loop Bandwidth		
	@CVR	@MPP	@CCR
10,000	1.03 kHz	0.331kHz	0.326 kHz
20,000	2.07 kHz	0.651 kHz	0.645 kHz
50,000	5.11 kHz	1.62 kHz	1.59 kHz
100,000	10.20 kHz	3.28 kHz	3.23 kHz
	Settling time		
	@CVR	@MPP	@CCR
10,000	606 µs	1.91 ms	1.92 ms
20,000	303 µs	954 µs	959 µs
50,000	121 µs	382 µs	384 µs
100,000	60 µs	191 µs	192 µs

To highlight the advantage of proposed IOIM control compared to DRM, the control system block diagram of the DRM-based VM PVE presented in Figure 1.3, is derived similarly by considering the r_L as an input variable to the system and shown in Figure 4.9. The open-loop TF of the reference generation loop is given by:

$$G_{OL_{DRT}}(s) = \frac{\Delta v_{Oref}(s)}{\Delta r_L(s)} = \frac{-G_{inner}(s)}{g_{pv}R_L} \tag{4-18}$$

From (4.18), it is clearly seen that reference generation loop is coupled with the closed-loop TF of the inner control loop.

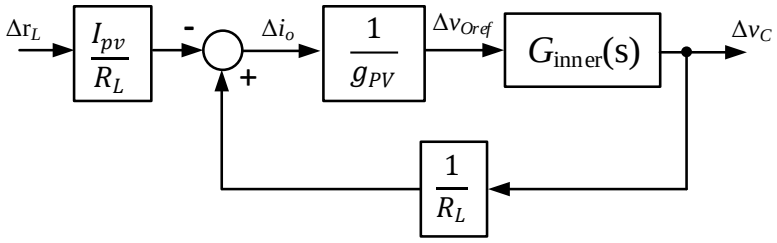


Figure 4.9 Control block diagram of the PVE with DRM.

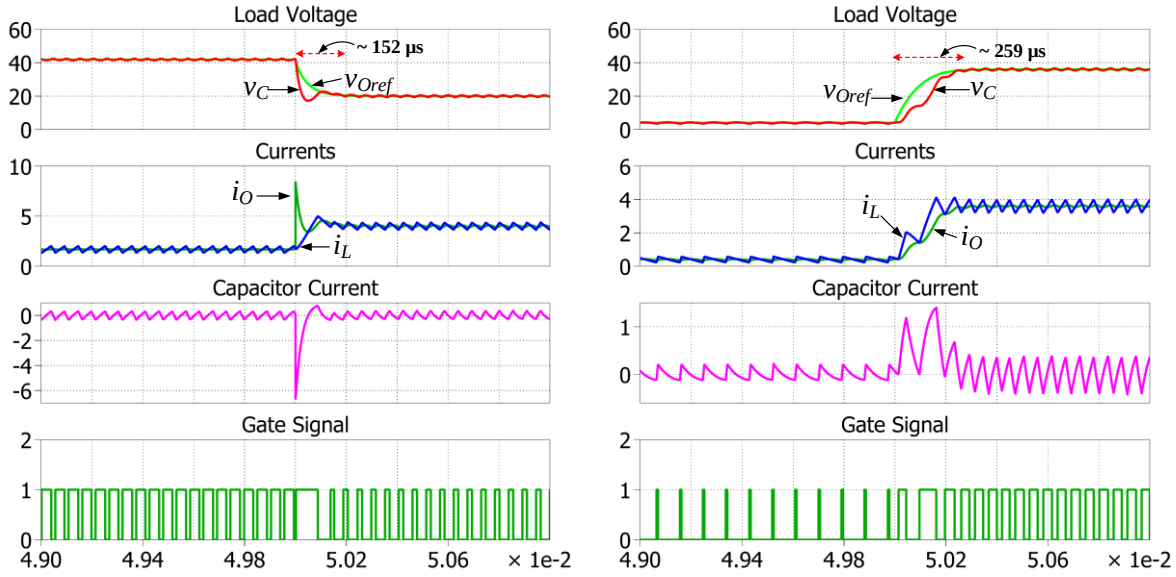
4.4. Simulation Results

The proposed PVE is examined using PLECS^{TM} circuit simulations to verify its performance under various test conditions. Further, its dynamic response is compared with a conventional PVE under linear resistive loads and MPPT converters to exalt the performance of the proposed method. A buck converter with an inner PI controller plus an I-to-V LUT as the reference generation method is considered as a conventional PVE in the comparison analysis. Key parameters used in both conventional and proposed PVEs in the simulations are listed in Table 4.4. Both PVEs are designed to emulate two BP365 PV modules connected in

series. Subsequent sections provide the simulation results obtained with resistive loads and MPPT converters.

4.4.1 Evaluation with Resistive Loads

Circuit simulations are carried out to evaluate the dynamic performance of the proposed PVE under load transients and irradiance changes with resistive loads. Figure 4.10 (a) shows the PLECS^{TM} simulation results for a load step change which moves the operating point from CVR to CCR.



(a) (b)

Figure 4.10 Simulation results of proposed PVE for (a) load step change from 25 Ω to 5 Ω at 1kW/m^2. (b) solar irradiance step-up change from 0.1 to 1.0 kW/m^2 at 10 Ω.

As seen, the proposed PVE reaches the steady-state within 152 µs. Transient response results for a step-change in irradiance (i.e., from 0.1 kW/m^2 to 1 kW/m^2) are shown in Figure 4.10 (b). The PVE takes multiple switching actions before reaching steady-state since the reference signal is limited by the settling time of the IOIM control loop. These simulation results prove that IOIM is able to generate a stable reference signal in both CCR and CVR

regions with fast convergent speed and the inner BC loop regulates the v_C at given v_{Oref} within two switching actions. Further, simulations are carried out to investigate how the trajectories of state variables ($i_L - v_C$), current and voltage reference signals ($i_{Oref} - v_{Oref}$), output current and voltage ($i_O - v_C$) behave in the I-V plane during transients with the proposed method. Figure 4.11 demonstrates the simulation results for series of load transients in the I-V plane. As shown, the load is changed from a light load to a heavy load in the steps of 25 Ω-8 Ω-4 Ω for tracing the I-V curve in both CCV and CCR. The $i_L - v_C$ trajectory provides operating behavior of the buck converter, and it is seen that the converter reaches the steady-state within two switching actions during every transient. Trajectory of $i_{Oref} - v_{Oref}$ proves that IOIM controller provides a stable v_{Oref} regardless of the region of operation in the I-V curve. During a transient, $i_O - v_C$ trajectory meets the new load line instantaneously and follows until it settles down at the intersection point of the load line and I-V curve.

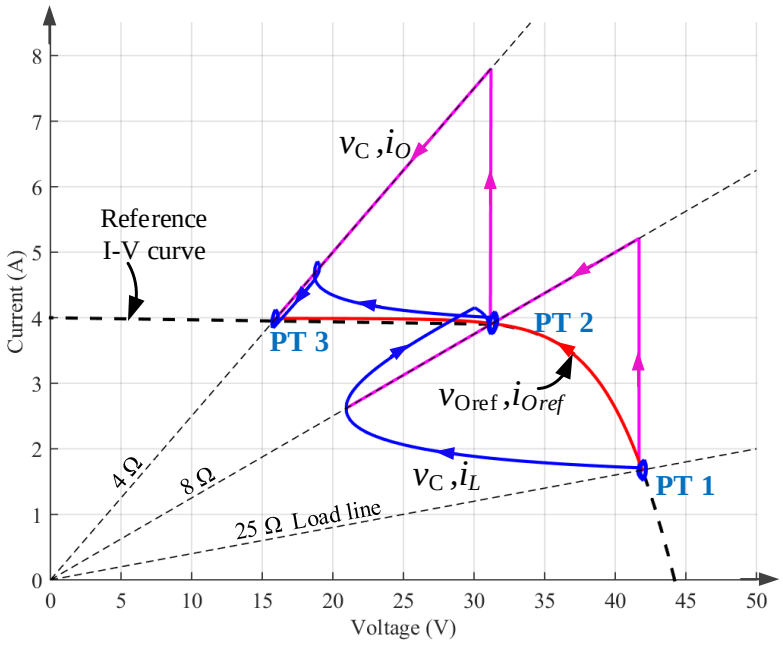
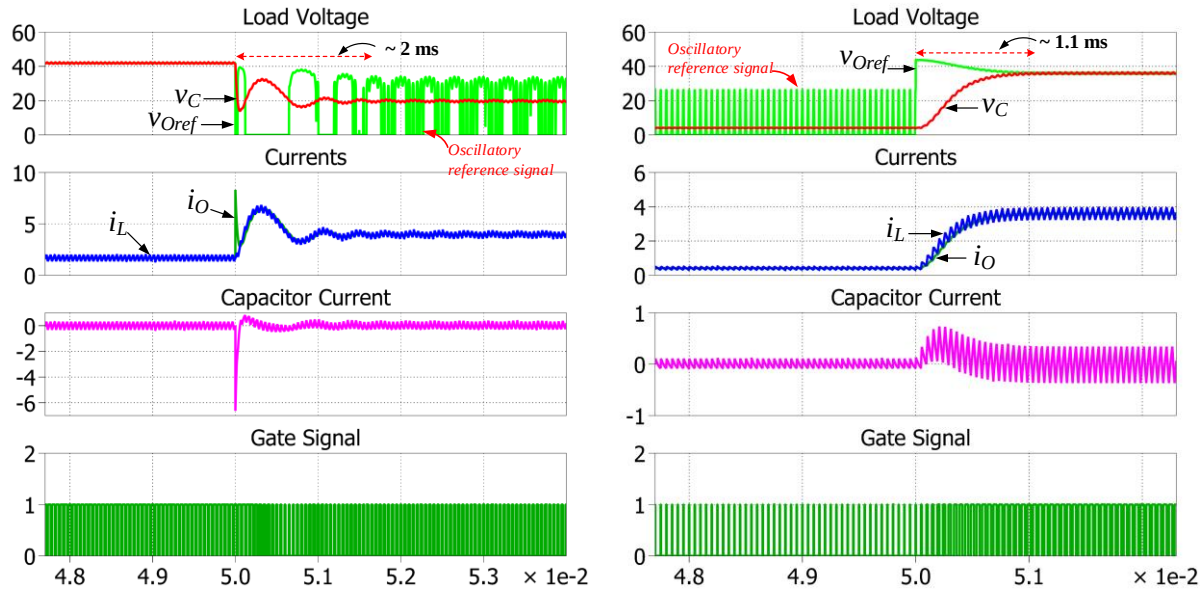


Figure 4.11 Trajectories of reference, state variables and output current and voltage during load transients in I-V curve.

Table 4.4 System specification of proposed PVE and conventional PVE in simulation.

PROPOSED PVE (BC +IOIM)		CONVENTIONAL PVE (PI+DRM)	
Parameter	Value	Parameter	Value
v_S/Δ	60 V / 0.25 V	v_S	60 V
L	1 mH	L	1 mH
C	4.7 µF	C	4.7 µF
k_i	100,000	$f_{S_{PI}}$	20 kHz
$f_{S_{BC}}$	7.7 kHz – 27 kHz	k_{P1}, k_{I1}	5.7x10-4 ,38
K_P, K_I	0.2, 400	PWM gain	1

In order to compare the fast-dynamic performance of the proposed PVE, a conventional PVE is simulated by applying the same disturbances as discussed in Figure 4.10. The PI control parameters of the conventional DRM-based PVE are designed considering the open-loop TF of the inner voltage loop. The power conversion stage is modelled using the state-space averaging technique, and the system is linearized at an operating point where the system is highly underdamped (i.e. near CVR, R_L = 87.7 Ω). The PI controller is designed to have a crossover frequency of 370 Hz for a switching frequency of 20 kHz. Figure 4.12 shows simulation results for load and irradiance transients with the conventional PVE. As expected, settling times are much longer during transients (1 ms – 2 ms), and the voltage reference signal is highly oscillatory in the CCR. Hence, the PI controller is designed to have low control bandwidth to suppress the oscillatory reference signal and mitigate undesired output voltage and current waveforms.



(a) (b)

Figure 4.12 Simulation results of conventional PVE for (a) load step change from 25 Ω to 5 Ω at 1kW/m^2. (b) solar irradiance step-up change from 0.1 to 1.0 kW/m^2 at 10 Ω.

4.4.2 Evaluation with MPPT Converters

Simulation results of the proposed PVE with a high-performance MPPT converter are provided in this section and compared with a conventional PVE (i.e., a buck converter with an inner PI controller plus an I-to-V LUT as the RGA). The inverted buck topology is chosen to realize the MPPT converter, which represents a common choice for the front-end dc-dc stage in PV applications. The control scheme consists of a *dp/dv* tracking scheme as the MPPT algorithm and a PI controller to regulate the input voltage of the MPPT converter. The cascaded system configuration is shown in Figure 4.13, and MPPT converter parameters used in the simulation are listed in Table 4.5. The control bandwidth of the conventional PVE is designed with 370 Hz to achieve a shorter settling time while avoiding the oscillatory reference issue, as mentioned in the previous section.

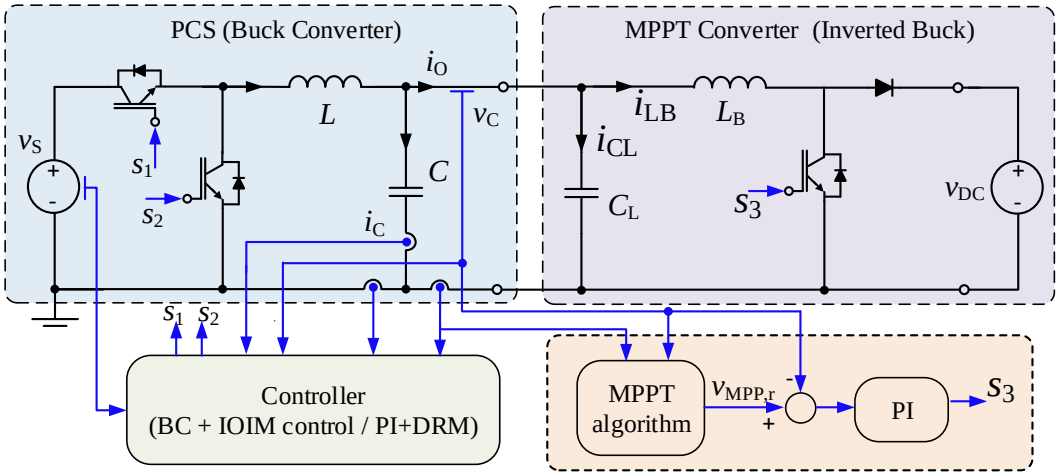


Figure 4.13 The system configuration of a PVE cascaded to a VM MPPT converter.

Simulation results of a PV array, the proposed PVE and the conventional PVE measured under a step-change in irradiance are shown in Figure 4.14.

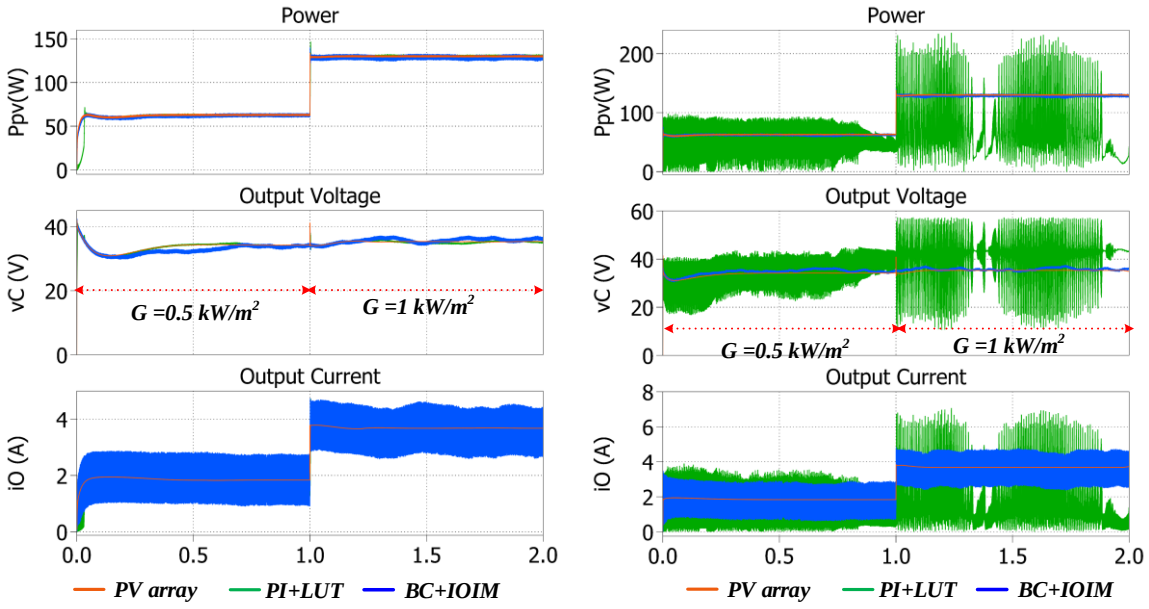


Figure 4.14 Simulation comparison of PV array, proposed PVE and traditional PVE with PI+DRM for a step change in solar irradiance from 0.5 kW/m^2 to 1 kW/m^2 with a VM MPPT converter for (a) a low bandwidth PI loop (4.25 Hz) and (b) a high bandwidth PI loop (1.96 kHz).

Figure 4.14 (a) shows the input power, input voltage and input current of the MPPT converter when its inner PI controller bandwidth is set to 4.25 Hz (k_{P2}=0.0065, k_{I2}= 0.5). It is shown that MPPT converter is able to track the MPP accurately with all three PV emulation methods. However, the system with conventional PVE becomes unstable when the bandwidth of the inner PI loop of the MPPT converter is increased to 1.96 kHz (k_{P2}=0.039, k_{I2}= 3) as shown in Figure 4.14 (b), while, under the proposed method, the MPPT converter is still able to track the MPP. In this way, the comparison highlights how the proposed PVE emulator enables faster MPPT algorithms than traditional PVEs.

Table 4.5 Parameter values of MPPT converter in simulation.

Parameter	Value	Parameter	Value
v_{DC}	48 V	k_{P2}	0.006
L_B	3.5 mH	k_{I2}	0.5
C_L	15 µF	f_{S2}	20kHz

4.5. Experimental Validation

A 130 W, 60 V input dc voltage, synchronous DC-DC buck converter prototype has been implemented which is based on the design block diagram in Figure 4.1. The design specification of the PVE prototype is given in Table 4.6, which is intended to emulate a PV array with two BP365 modules connected in series. Control scheme is implemented using a Texas Instruments TMS320F28377S DSP. BC scheme is implemented in an interrupt service routine running at 300 kHz while outer voltage ripple feedback loop and IOIM controller are implemented in an ISR running at 50 kHz. The measured variables are i_O, i_L, i_C, v_C and v_S and all of them are sampled at 300 kHz. The k_i gain in IOIM controller is chosen as 50,000 to limit the maximum bandwidth of the IOIM loop to be lower than 5.11 kHz. The IOIM uses a

LUT to implement the BP365 PV module where the I-V pairs are stored in a 3-D array with evenly spaced voltage array for solar irradiation levels between 0 to 1 kW/m^2 in steps of 0.1 kW/m^2 and three temperature values of 0 ºC, 25 ºC and 50 ºC. The resolution of the LUT is maintained at 49 mV.

Tests are conducted with resistive loads to evaluate the accuracy and dynamic performance of the proposed PVE. In addition, PVE is tested with PV MPPT converters to evaluate the steady-state and dynamic performance of the cascaded system.

Table 4.6 Key parameters of PVE prototype.

Parameter	Value	Parameter	Value
v_S	60 V	Δ	1 V
L	1 mH	C	4.7 µF
v_C	10 V – 44.2 V	i_O	0 A - 3.99 A
C_L	0 - 50 µF	f_S	3.2 kHz - 14.1 kHz

4.5.1 Dynamic Performance of Commercial Panel and PVE

The response time of a real PV array and a commercial PV emulator are examined first to identify their dynamic performance and compare them with the proposed PVE in modern solar power conditioning test setups. The transient response of a real PV array is determined with a test setup that has four Siemens PowerMax SP75 PV modules connected in series with a resistor bank. Figure 4.15 shows the transient response of the SP75 array for a load step down from 50 Ω to 25 Ω. The recorded settling time is 10 µs which is expected as it is known to have fast-dynamic characteristics.

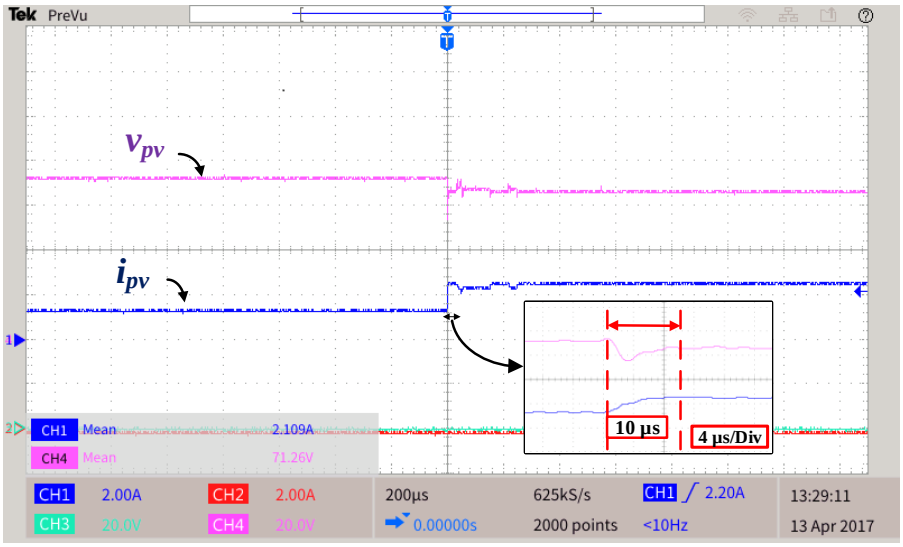
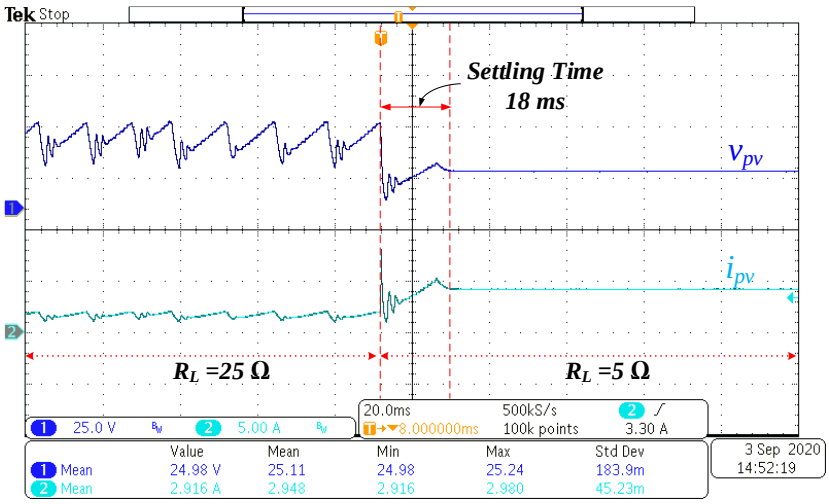
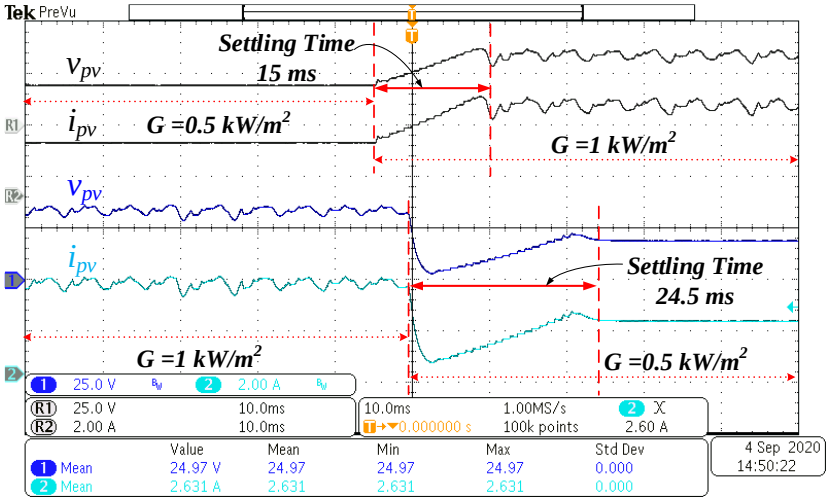


Figure 4.15 Transient response of a real SP75 PV array (4x1) for a load change from 50 Ω to 25 Ω.

Figure 4.16 (a) and Figure 4.16 (b) present transient response results of a Chroma 62050H-600S solar PVE for a load step change from 25 Ω to 5 Ω, and irradiance step-change between 0.5 kW/m2 and 1 kW/m2, respectively. In these tests, Chroma PVE is programmed to emulate two BP365 PV modules connected in series with V_{oc} = 44.2 V and I_{sc} = 3.99 A. The output voltage and current of Chroma 62050H-600S take between 15 ms – 24.5 ms to reach ± 5 % of the steady-state output value after transients. These test results verify that the dynamic response of tested commercial PVE is far from the real PV modules. Further, it is observed that Chroma PVE has an oscillatory output during its operation in CVR, which solidifies the oscillatory reference is a problem in existing commercial PVEs.



(a)



(b)

Figure 4.16 Transient response of Chroma 62050H-600S PVE for (a) a load change from 25 Ω to 5 Ω at 1 kW/m^2 and for (b) a step change in irradiance between 0.5 kW/m^2 to 1 kW/m^2 at 10 Ω.

4.5.2 Proposed PVE - Resistive Loads Evaluations

Tests are conducted with resistive loads to evaluate the accuracy and dynamic performance of the proposed PVE. With resistive loads, fast load transients can be applied, which allows testing the dynamic performance of PVE under the toughest transients.

4.5.2.1 Steady-state performance with resistive loads

The steady-state performance of the PVE prototype is tested by operating at different resistive load levels. Figure 4.17 and Figure 4.18 show the output waveforms (i.e. v_C, i_O) of PVE in steady-state for a load condition that lies in CVR and CCR, respectively. Results show that the peak-to-peak ripple of v_C is maintained at specified voltage ripple of 2 V, and stable operation of PVE is achieved in both regions of the I-V curve. Figure 4.19 illustrates the steady-state operating point trajectories for different load levels on the I-V plane when PVE is intended to emulate a PV array with two BP365 modules connected in series. It is tested with a maximum load of 4.75 Ω and until open circuit voltage output and results are compared with the reference I-V curve of 1 kW/m^2 and 0.5 kW/m^2.

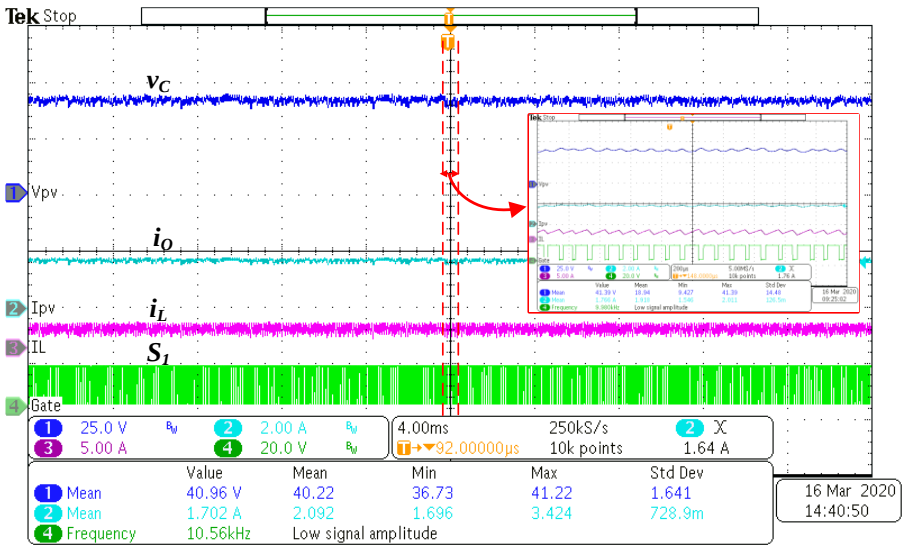


Figure 4.17 Experimental results of steady-state operation with 23.8 Ω (in CVR).

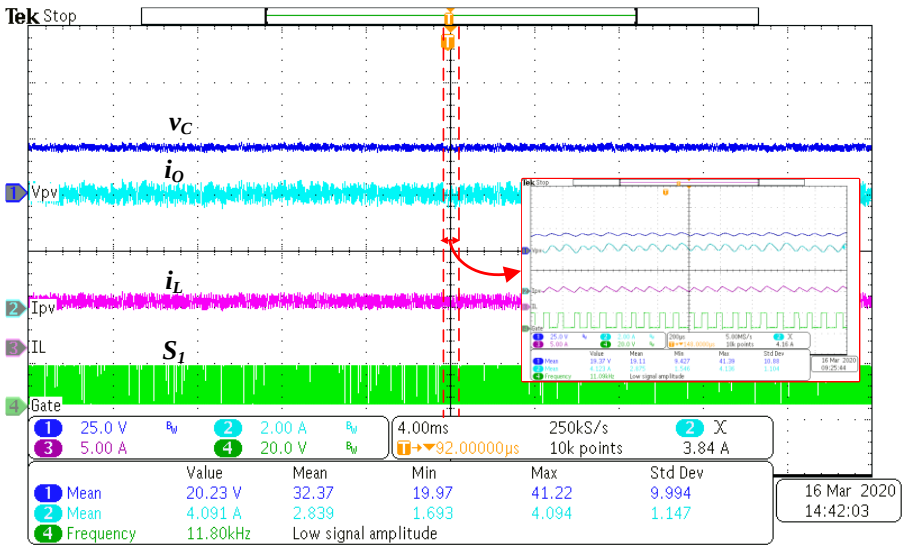


Figure 4.18 Experimental results of steady-state operation with 4.75 Ω (in CCR).

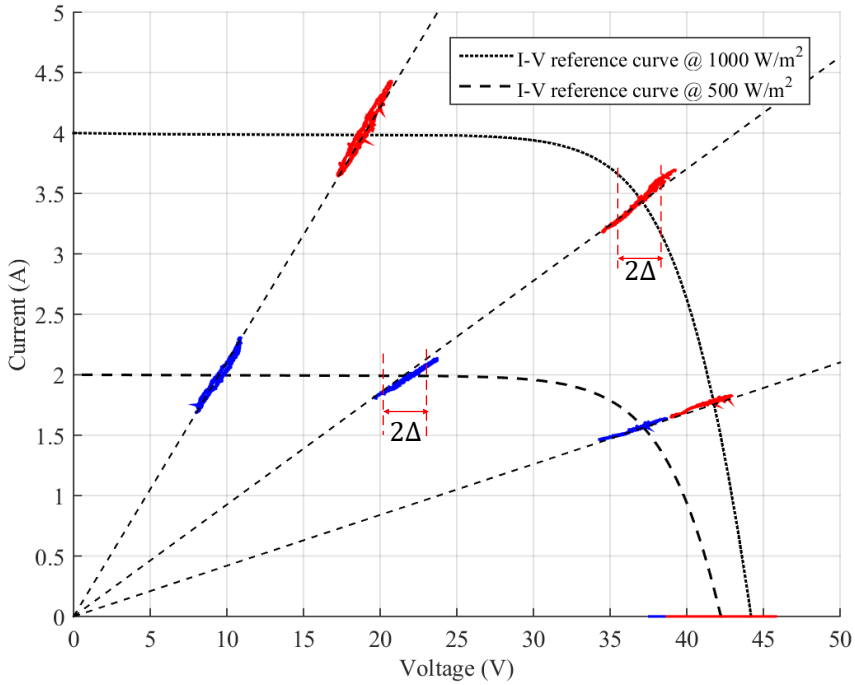


Figure 4.19 Steady-state I-V trajectory with resistive loads.

Accuracy of PVE is evaluated by taking the average value of measured v_C, i_O and compare it with PLECS PV model simulation results. Table 4.7 presents the comparison results, and it shows that error percentages are within 3.5 %. Furthermore, the system's

efficiency under different loading conditions is recorded, as shown in Table 4.7. It shows that the efficiency varies between 95% - 83%, which agrees with the theoretical efficiency of the converter. The theoretical efficiency of PVE is calculated based on losses in the inductor (i.e. core loss and copper loss) and semiconductor losses (i.e. conduction loss, switching loss, and diode reverse recovery loss).

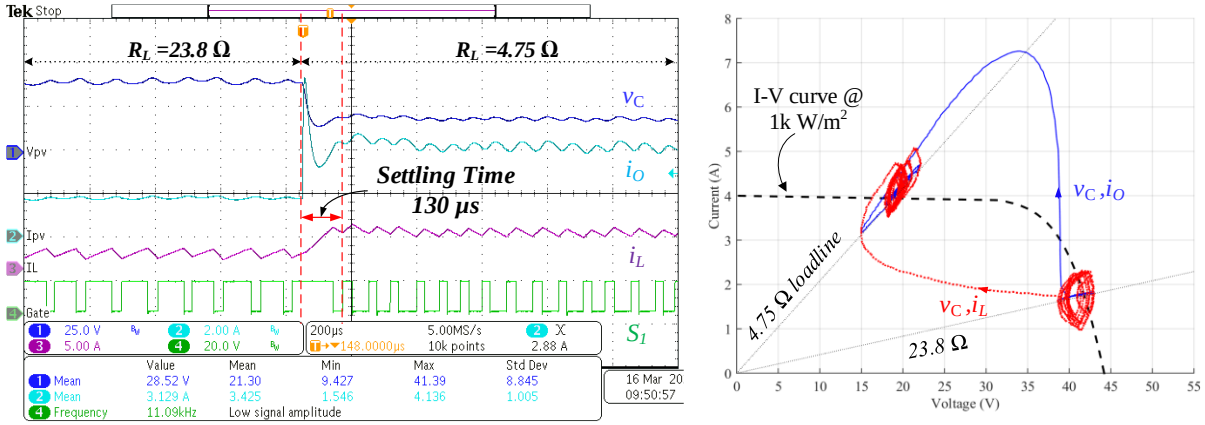
Table 4.7 Performance evaluation of the proposed PVE.

$R_L(\Omega)$		v_C (V)		Error %	i_O (A)		Error %	Efficiency (%)	
		PLECS	PVE		PLECS	PVE		Theoretical	Measured
1 kW/m^2	23.8	41.78	41.39	0.93%	1.756	1.766	-0.6%	95.87%	94.84%
	10.8	37.09	36.89	0.54%	3.434	3.435	-0.1%	95.57%	93.40%
	4.75	18.95	19.37	-2.21%	3.988	3.988	0.0%	91.08%	87.43%
	OC	44.2	43.11	2.47%	0	-	0.00%	-	-
0.5 kW/m^2	23.8	37.19	36.58	1.63%	1.562	1.547	1.0%	94.94%	94.61%
	10.8	21.53	21.78	-1.17%	1.993	1.973	1.0%	92.63%	91.72%
	4.75	9.48	9.54	-0.65%	1.995	1.994	0.0%	84.94%	83.41%
	OC	42.3	40.93	3.25%	0	-	0.0%	-	-

4.5.2.2 Transient performance with resistive loads

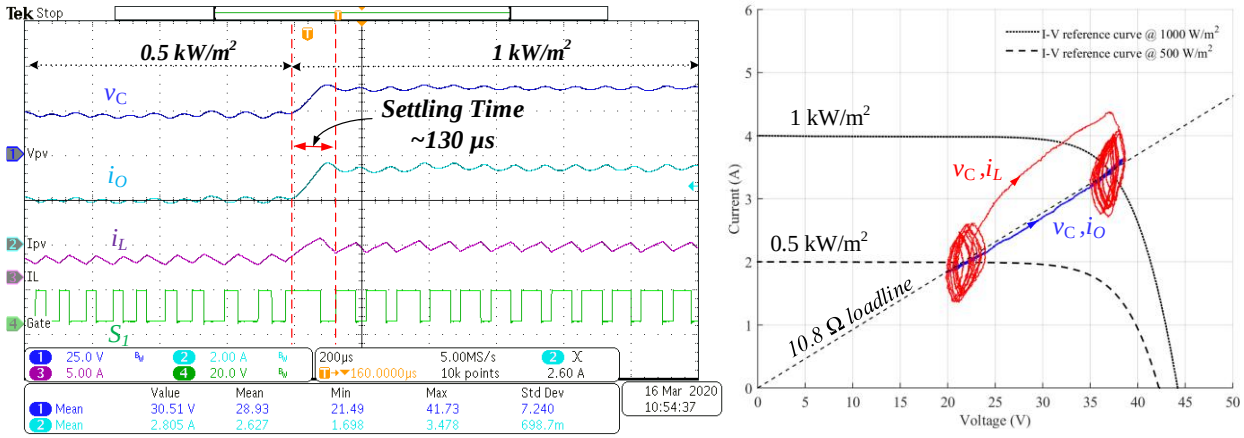
Experiments results for a load step down transient (23.8 Ω to 4.75 Ω) in time and I-V domains are shown in Figure 4.20. This is tested under the condition of irradiance equals to l kW/m2, T=25 ºC and recorded settling time is found as approx. 130 µs, as shown in Figure 4.20 (a). The PVE reaches steady-state within a few switching actions, and the operating switching frequency is in the range of 8.3 kHz to 12.5 kHz. The I-V trajectory during this transient is presented by Figure 4.20 (b). Similarly, transient response for an irradiance step up

from 0.5 kW/m^2 to 1 kW/m^2 is shown in Figure 4.21. The output voltage is maintained within the specified voltage band and recovers within ~130 µs to ±3.5 % of steady-state output value.



(a) (b)

Figure 4.20 Experimental results for a load step down (23.8 Ω to 4.75 Ω at 1 kW/m^2) in (a) time-domain (b) I-V plane.



(a) (b)

Figure 4.21 Experimental results for a step change in solar irradiance from 0.5 kW/m^2 to 1 kW/m^2 at 10.8 Ω in time and I-V domain.

In the second test, the load is switched between two values: 23.8 Ω and 10.8 Ω with a frequency of 1 Hz to evaluate the versatility of the proposed PVE. Recorded results are presented in Figure 4.22, and it can be seen that load step-up and step-down transient response

time is ~130 µs, highlighting the fast transient response achieved with the proposed PVE. Even though the proposed PVE is 13 times (i.e., 130 µs compared to 10 µs) slower than a real PV array, it is still capable of testing MPPT converters that have a short response time between a few milliseconds to several seconds. However, a detailed investigation is required to identify the influence of the control bandwidth of PVE on the stability of load converters.

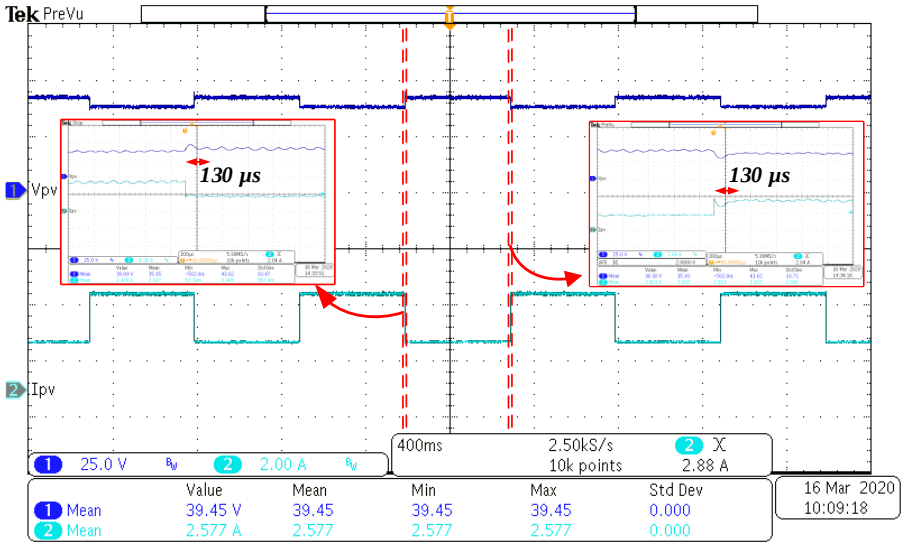


Figure 4.22 Experimental transient response for a series load step test (23.8 Ω-10.8 Ω).

Figure 4.23 shows the measured closed-loop frequency response of the inner BC loop at an operating point near MPP (v_S=60 V, v_C=35 V, i_O=3.5 A, f_S=11.6 kHz). As seen, gain of the closed-loop TF decreases around 11.5 kHz resembling low-pass filter characteristics with crossover frequency equal to f_s. This verifies the closed-loop bandwidth of the inner control loop is equals to the operating switching frequency.

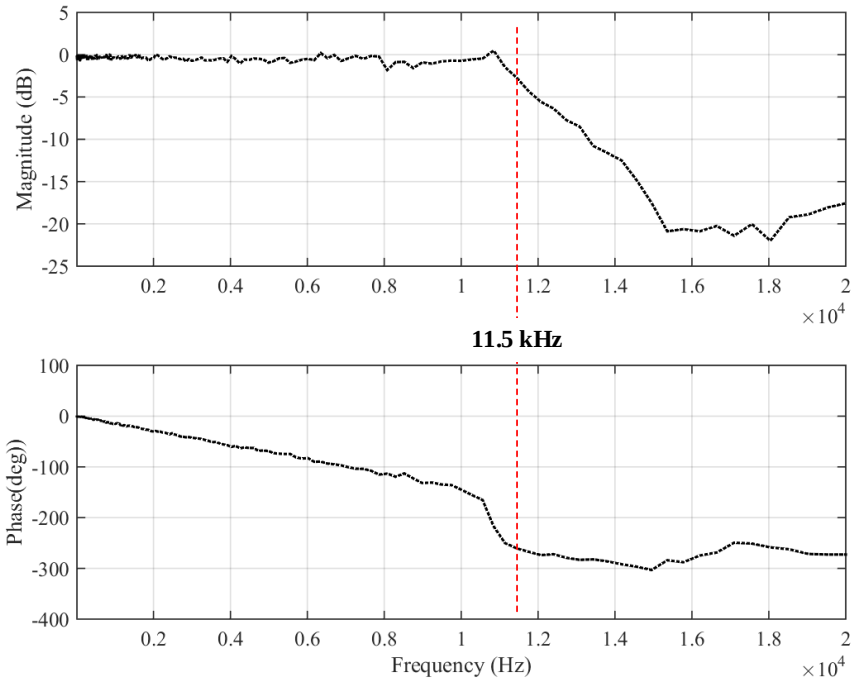
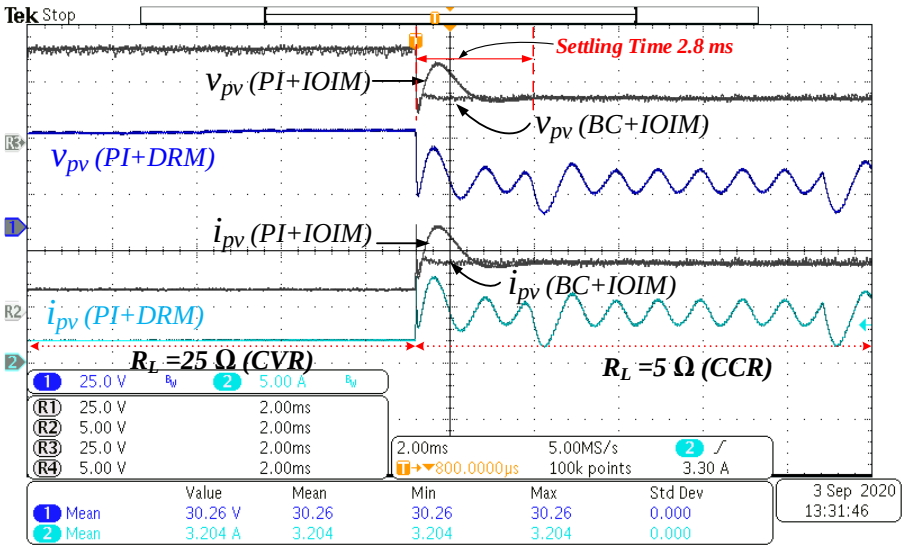


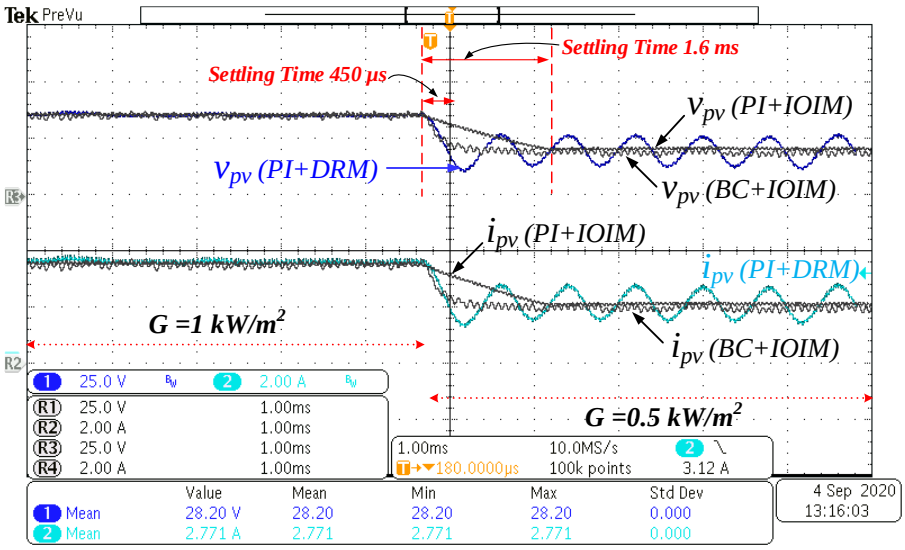
Figure 4.23 Measured closed-loop frequency response of inner boundary control loop ($G_{inner}(s)$) at an operating point near MPP.

4.5.3 Comparative Analysis with a Conventional PI-based PVE

Experimental results of the proposed BC+IOIM control scheme are compared against a traditional VM PVE with PI+DRM as well as a PVE with PI+IOIM control to validate its fast dynamic performance and stable operation in both CVR and CCR of the I-V characteristic curve. The same parameters are used in the power stage for a fair comparison, while the switching frequency of the PI-based PVE is chosen as 20 kHz. The PI controller is designed with k_{P1}= 0.00057, k_{I1}= 38.45 to have a crossover frequency of 370 Hz at an operating point where the system is highly underdamped (i.e., near CVR, R_L = 87.7 Ω). Experimental results for the above mentioned three methods under load and irradiance transients are shown in Figure 4.24 (a) and (b), respectively.



(a)



(b)

Figure 4.24 Comparison of proposed PVE, traditional PVE with PI+DRM and PVE with PI+IOIM control under (a) a load step change from 25 Ω to 5 Ω at 1 kW/m^2 (b) a step change in solar irradiance from 1 kW/m^2 to 0.5 kW/m^2 at 10 Ω.

As shown in Figure 4.24 (a), output waveforms of the proposed PVE reach steady-state within 0.2 ms, providing a stable output in both regions of the I-V characteristic curve. In contrast, both PI-based PVEs show a slower response of about 2.8 ms, while the PVE with

conventional DRM delivers an oscillatory output whenever it is operated in CCR. The PVE with PI+IOIM operates stably in both CVR and CCR since IOIM generates a stable reference signal allowing a design of a high bandwidth PI control loop. A similar outcome is noticed with a solar irradiance step change as shown in Figure 4.24 (b) as the converter operated in CCR when conditions changed to 0.5 kW/m2 at 10 Ω. The oscillatory output can be solved by designing a slower PI control loop, as shown in Figure 4.25, at the expenses of a slower dynamic response.

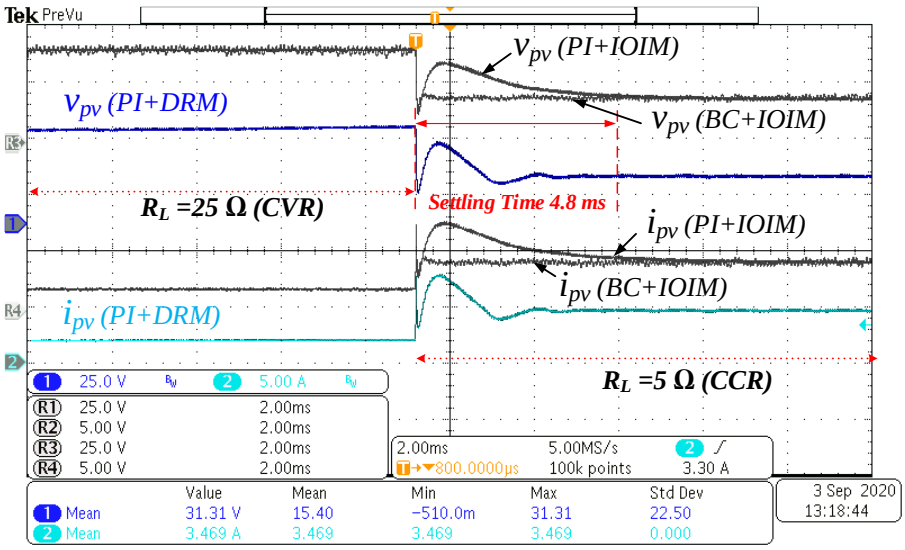


Figure 4.25 Comparison of the proposed PVE, traditional PVE with PI+DRM and PVE with PI+IOIM control with a control bandwidth of 61 Hz (k_P= 0.00057, k_i= 6.4).

Table 4.8 summarises the dynamic performance of some of the key switch-mode PA-based PVEs in recent works together with their characteristics. In [18], a control scheme is implemented via analog circuits with a much higher switching frequency (i.e., 1 MHz) to achieve excellent dynamic characteristics. It is clearly seen from Table 4.8, and also from the experimental results of traditional PVE that the application of the BC+IOIM control for a synchronous buck converter can result in a better transient tracking performance and

simultaneously having a stable operation in both CCR and CVR regions of the I-V characteristic curve.

Table 4.8 Dynamic performance and characteristics comparison with existing PVEs.

Reference	Settling time for a load step change	Power Stage	Control Method		Controller Implementation
			Inner loop	RGA	
Proposed PVE	**130 µs**	**Synchronous DC-DC buck converter**	**σ^2_{cor}**	**IOIM**	**Digital**
Nguyen-Duy 2016 [18]	10 µs (Fig.17 in [18])	Synchronous DC-DC buck converter with LCLC filter	PID (VM)	PV array small-signal circuit	Analog circuit
Koran 2010 [64]	3.8 ms (Fig.17 in [64])	DC-DC buck converter with LCLC filter	PID (Current mode)	PV equivalent circuit	Analog circuit
Chang 2013 [65]	6 ms (Fig.12 in [65])	LLC resonant DC-DC converter	Frequency modulation control	Not found	Digital
Ayop 2019 [73]	21.25 ms (Fig.10 in [73])	DC-DC buck converter	PI control	Current-to-resistance PV model	Digital

4.5.4 Proposed PVE – MPPT Micro-Inverter Evaluations

The proposed PVE is cascaded to a solar micro-inverter (TI TMDSSOLARUINVKIT) to test the performance of PVE as well as the MPPT controller. The schematic of the experimental test setup is shown in Figure 4.26. A filter inductor is placed between the PV emulator and the solar micro inverter to represent the EMI filter inductor. The flyback stage of the micro-inverter controls the current from the PV source such that the PV module operates at its MPP [135]. Technical specifications of the solar micro-inverter (SMI) are provided in Table 4.9.

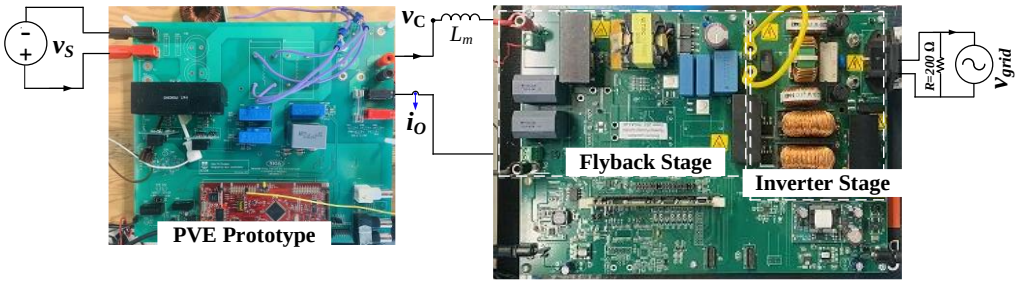


Figure 4.26 Test setup schematic with the MPPT micro-inverter.

The steady-state output waveforms of the PVE and SMI for irradiance levels of 1 kW/m^2 and 0.5 kW/m^2 are shown in Figure 4.27. It shows a stable DC voltage at PVE and stable AC voltage on the grid side.

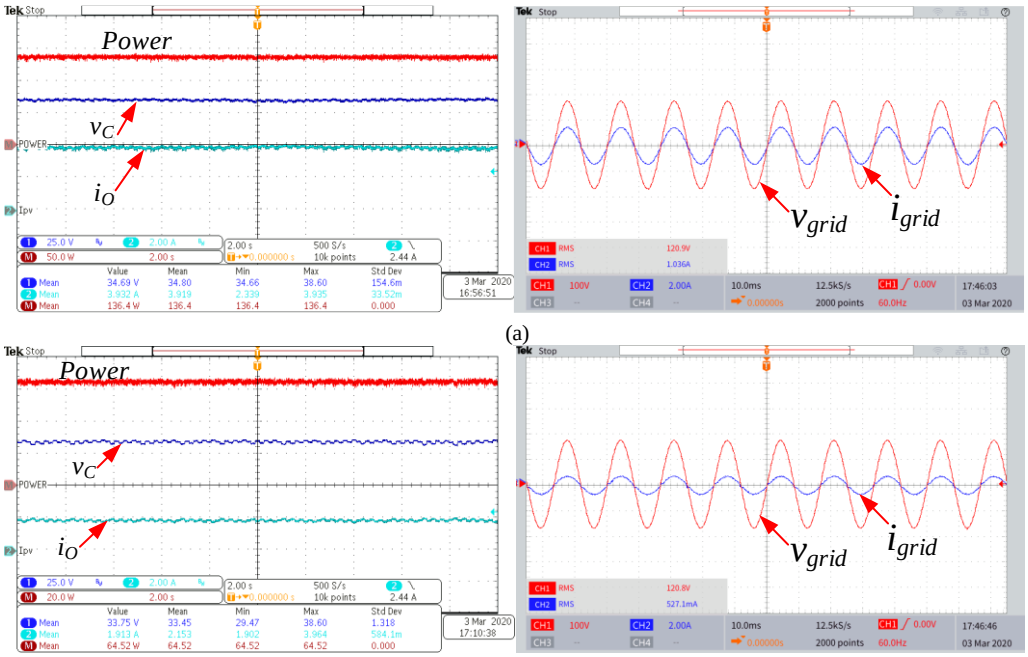
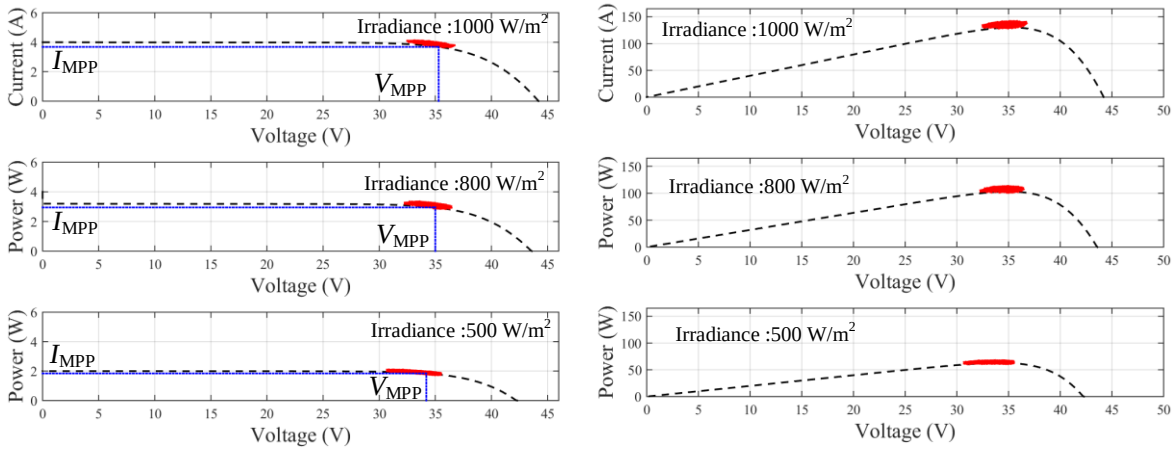


Figure 4.27 Steady-state results of proposed PVE with SMI at (a) 1 kW/m^2 (b) 0.5 kW/m^2.

Table 4.9 Specifications of the MPPT Micro Inverter.

Parameter	Value	Parameter	Value
Solar Panel Output	25 V- 44 V	EMI Filter Inductor	200 µH
Rated Power for 110Vrms	140 Wmax	Power Resistor	200 Ω

In order to demonstrate that it is operated at v_{mpp} and P_{max}, experimental results under steady-state conditions are shown in Figure 4.28, where I-V and P-V plots are presented for irradiance levels of 1 kW/m^2 0.8 kW/m^2 and 0.5 kW/m^2. The plots verify its equilibrium operation around the MPP with a static MPPT efficiency above 94% and v_C is tightly regulated by the PVE at V_{mpp} with an accuracy of 1.7 %.



(a) (b)

Figure 4.28 Steady-state experimental results of the proposed PVE with a MPPT micro inverter under 1000 W/m^2, 800 W/m^2 and 500 W/m^2 (a) I-V plot, (b) P-V plot.

Figure 4.29 (a) shows the response of the proposed PVE for a solar irradiance step change from 0.5 kW/m^2 to 1 kW/m^2. It shows that the micro-inverter searched a new MPP after the change and reached steady-state within 6.4 s. Here, the transient response time of the system depends on the control loop bandwidth of the flyback stage of the micro-inverter. To demonstrate that it is operated at v_{mpp} and P_{max}, Figure 4.29 (b) and Figure 4.29 (c) present the waveform trajectory for different irradiance levels, including 1 kW/m2 and 0.5 kW/m2 in the I-V and P-V plots. One possible reason for these minor discrepancies is the voltage drop across the equivalent series resistance (ESR) of the additional filter inductor. The micro

inverter operated correctly with the proposed PVE since maximum power has been extracted under steady-state and transient conditions.

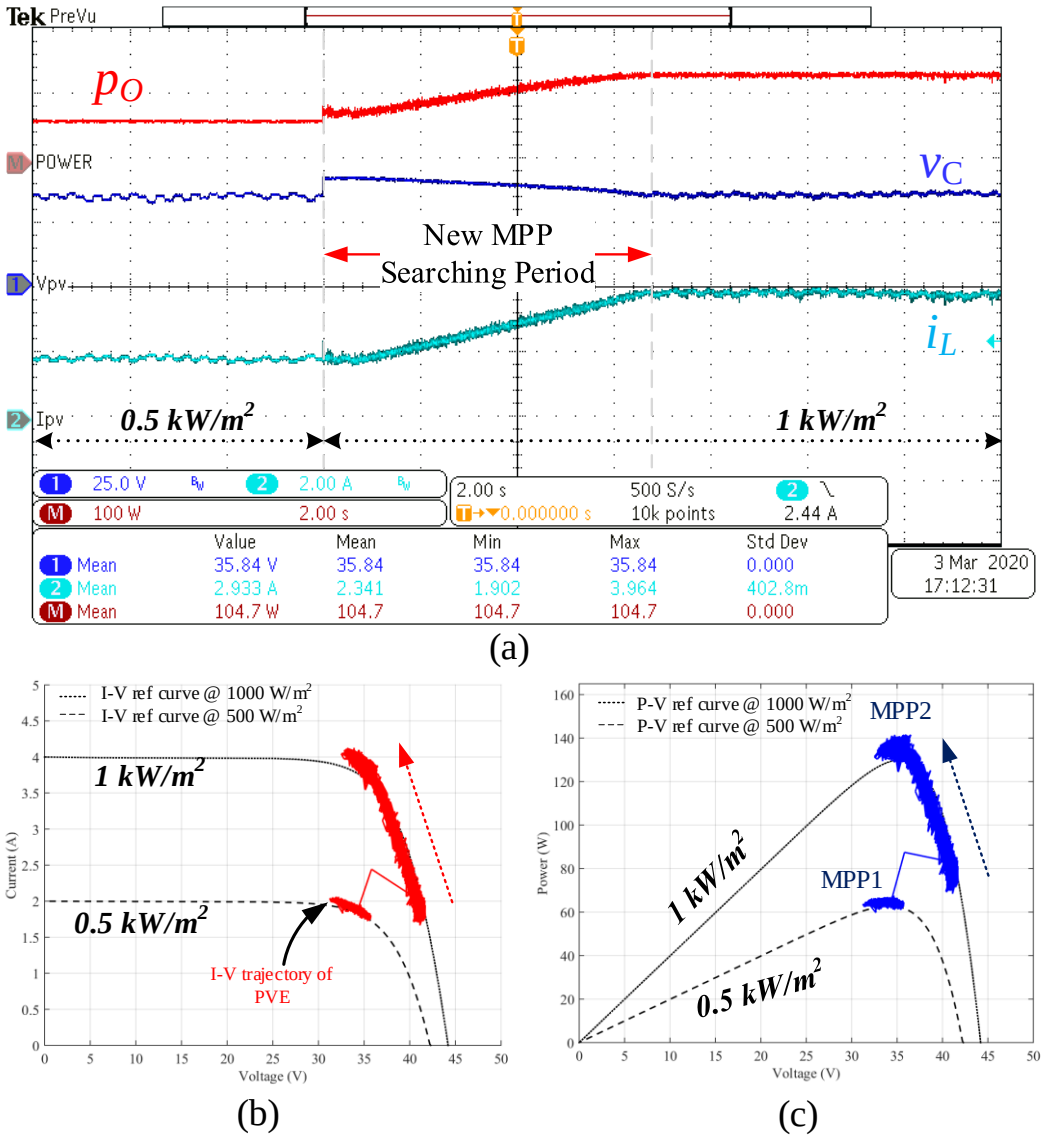


Figure 4.29 Transient response of PVE with a MPPT micro-inverter for irradiance step- up from 0.5 kW/m^2 to 1 kW/m^2 (a) time (b) I-V (c) P-V domain.

Further, a dynamic MPPT efficiency test is performed according to EN 50530 by applying a test sequence for fluctuations between medium and high irradiation intensities

[136]. The dynamic MPPT test result for a test sequence ramps of 40 % -100 % nominal power ($P_{DC,n}$) with a slope of 8.6 W/m^2/s is shown in Figure 4.30. It is seen that the PVE is fast enough to emulate such test patterns, and micro-inverter is capable of tracking the MPP under such irradiance fluctuations.

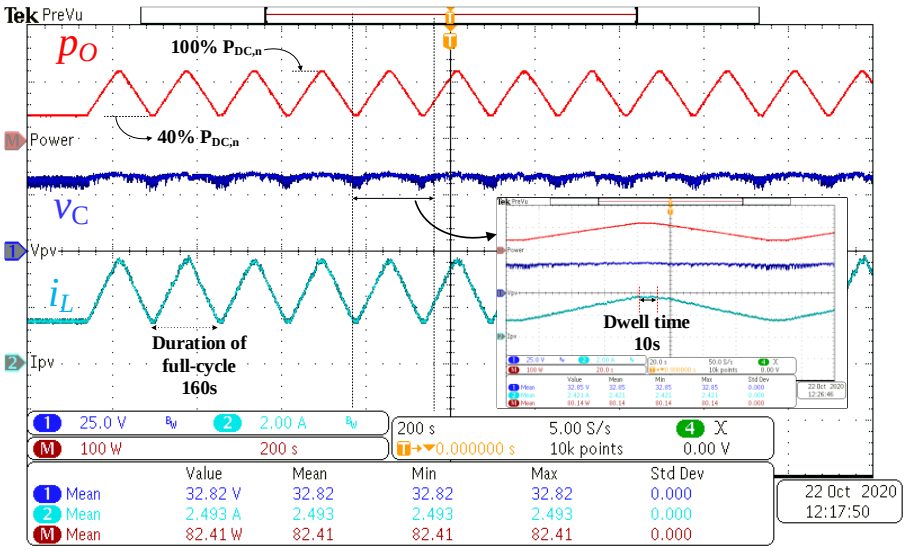


Figure 4.30 Dynamic MPPT test under EN 50530 with proposed PVE.

4.6. Summary

This chapter presented a comprehensive voltage-mode control scheme for buck-based PVEs to improve the dynamic response while maintaining the accurate emulation of the I-V characteristic curve. An innovative IOIM controller is introduced to decouple the inner control loop response from the reference generation loop and generate a stable voltage reference regardless of the operating point region in the I-V characteristic curve. The boundary control scheme derived in Chapter 3 is employed to control the output voltage at a given reference within two switching actions. Detailed mathematical procedures are provided to design the IOIM controller, BC loop and buck-stage inductor. The PVE parameters should be designed

by taking the effect from load capacitance as well as considering the compromise between the switching frequency and the current ripple. The performance of the PVE was confirmed through simulation and experimental results in a 130 W laboratory prototype. Results show that the dynamic response time of the system has reduced to hundreds of microseconds which enables the possibility to evaluate faster MPPT algorithms without increasing the switching frequency.

It must be acknowledged that the operation of the proposed PVE is still influenced by the value of C_L. The system parameters such as f_s, Δi_{Lmax} are significantly affected by C_L even though PVE has the freedom of varying L and Δ to achieve design specifications. Moreover, C_L has a considerable impact on the dynamic performance of the proposed PVE since the dynamic response of the PVE is mainly governed by the operating f_S. It is shown that the bandwidth of the inner BC control loop is approximately equal to the f_s and the maximum bandwidth of the IOIM loop should be designed lower than the minimum f_s of the system to filter out switching frequency ripple components from the instantaneous impedance measurement. Thus, maximum C_L must be specified as a constraint to achieve design specifications with the proposed approach. To eliminate this limitation, topology and non-linear control architecture that has a minimum effect from C_L is required. A switch-mode PA based on a synchronous buck converter with a two-stage LC filter will be presented targeting PV emulation in current-mode in Chapter 5 to eliminate this limitation while preserving the fast-dynamic characteristics.

Chapter 5

Design, Implementation and Stability Analysis of a Switch-mode PV Emulator using Power-HIL Simulation

The work described in this chapter was submitted for publication as the following paper: I. D. G. Jayawardana, C. N. M. Ho, and M. Pokharel, "Design, Implementation and Stability Analysis of a Switch-mode PV Emulator using Power-HIL Simulation," in *IEEE Transactions on Industry Applications,* to be submitted. The part of the work was also presented as a conference paper at the IEEE ECCE 2019.

In this chapter, the use of PHIL simulations for PV emulation is studied, including a switch-mode PA design to identify its applicability in testing modern-day MPPT converters. The voltage-mode PA developed in Chapter 3 is extended to a current-mode PA by introducing a topology and control modification, and then it is used to develop the PHIL-based PVE. The stability of the PHIL-based PV emulator is studied by deriving the comprehensive small-signal model.

5.1. Introduction

Use of PHIL simulation for DC source emulation is getting popular as it offers a realistic, controlled and easily reconfigurable testing environment compared to standalone source emulators. In [35], [40], [41], PHIL-based PVEs are implemented by integrating a PV model in RTS through the power interface that consists of PA, analog-to-digital converter, digital-to-analog converter and sensor. The PA of the PHIL interface operates to imitate the PV characteristics, and real power is exchanged between PA and DUT. Advantage of PHIL-based PVE is that it provides a platform for conducting burn-in tests with enhanced flexibility for different commercial PV arrays compared to standalone PVEs, and it takes advantage of the grid integration testbed since RTS is already in place for grid emulation. In all these works, the focus is on developing a comprehensive PV model for real time simulations. However, modelling and stability analysis of the PHIL-based PVE via IA has not been investigated in detail.

Moreover, although the PHIL simulation via ITM IA is well known, and its stability and accuracy are analysed in general, particularly the implementation, modelling, and stability analysis of PHIL-based PVE via an IA have not been sufficiently addressed in the existing literature. Further, the existing stability and accuracy studies of a switch-mode PA interface for PHIL simulations are mostly developed with small-signal models derived considering a standard resistive divider network and detail small-signal system model with a nonlinear DC source haven't been described [36], [37], [62], [108]. Therefore, this chapter presents a comprehensive study and analysis on a PHIL-based PV emulator implemented via ITM IA with a switch-mode PA. The current-type ITM IA is used to interface the PV model in RTS with the switch-mode PA. A comprehensive small-signal model of the system, including the

virtual PV model and power interface, is derived for analyzing the emulator's stability and accuracy under different operating regions of the I-V characteristic curve.

Further, selecting a proper power interface is crucial in minimizing latency and facilitating a correct PHIL simulation. The critical problem of the PHIL technique is that the power interface introduces unavoidable dynamics such as time delays and limited bandwidth that do not exist in the original circuit, as described in Section 2.4. This will play a significant role in the accuracy and stability of PHIL simulations [36], [37], [44], [108], [109]. Therefore, the PA of the PHIL interface should have as minimum delay as possible if it is to be used in PHIL experiments. Besides, the transient response of PA is also crucial as it decides the response time of the overall PHIL simulation. Therefore, this chapter also seeks to develop a current-mode switch-mode PA with fast-dynamic characteristics to minimize the PHIL power interface latency, which is also one of the main focuses of this thesis.

Large-signal-based control methods such as second-order BC [56]-[58] and sliding mode control [54] can be used in buck-based PAs to achieve improved transient responses and robustness against CPLs that have destabilizing negative impedance characteristics. However, PA performance under large-signal-based control methods will be significantly affected when it is cascaded to switching load converters, as described in Chapter 3.2. In Chapter 3, a BC with a corrected second-order switching surface is presented to regulate the output voltage of a buck-based PA within a specified band under capacitive loads and filter parameter variations. Nevertheless, the PA's switching frequency and output current ripple still depend on the load capacitance. Also, controller performance is still be degraded when high-frequency current ripple components that are led by the load converter are significant than the source converter high-frequency current ripple components.

To overcome these limitations, in this chapter, a switch-mode PA based on a synchronous buck converter with a two-stage LC filter is proposed with a cascade control scheme to use it as a current-mode PA for PHIL simulations. The cascaded control scheme employs an outer deadbeat controller and inner BC scheme to regulate outer inductor current and inner capacitor voltage through the LCL filter. The second-stage LC filter decouples high-frequency current ripple components led by the load converter passing into the inner LC filter and vice versa. It enables applying a BC scheme through the inner LC filter and regulating inner capacitor voltage without affecting PA's performance in switching frequency, output current and voltage ripple due to the switching-load converter. The fast-dynamic BC scheme maintains the inner voltage loop bandwidth to be the same as switching frequency, as confirmed in Section 4.5.2.2. Thus, the outer current loop can be designed with higher control bandwidth, maintaining a higher overall bandwidth-to-switching frequency ratio and guarantees fast current tracking ability. The original idea comes from the application of grid-connected PV inverter with LCL filter [99], in which the combination of BC and deadbeat control is applied to guarantee wide control bandwidth and eliminate the challenge of filter resonance with LCL filter.

The subsequent section of this chapter describes the detailed PHIL-based PVE design along with the design strategy of the proposed current-mode PA as well as the implementation of the PHIL power interface. The stability and accuracy of the PHIL-based PVE are analysed in different operating regions of the I-V curve using small-signal analysis in Section 5.3. In Section 5.4, experiment results with linear resistive loads as well as with PV micro inverters are presented to validate the accuracy, stable operation, and fast current tracking ability of the proposed system.

5.2. System Architecture

Figure 5.1 shows the proposed system configuration of the PHIL-based PVE via current-type ITM IA, which consists of a PV model simulated in RTS, signal interfaces and a switch-mode PA. This setup forms a PHIL-based PVE for testing physical PE converters. The following subsections discuss the key elements that form the architecture of PHIL-based PVE.

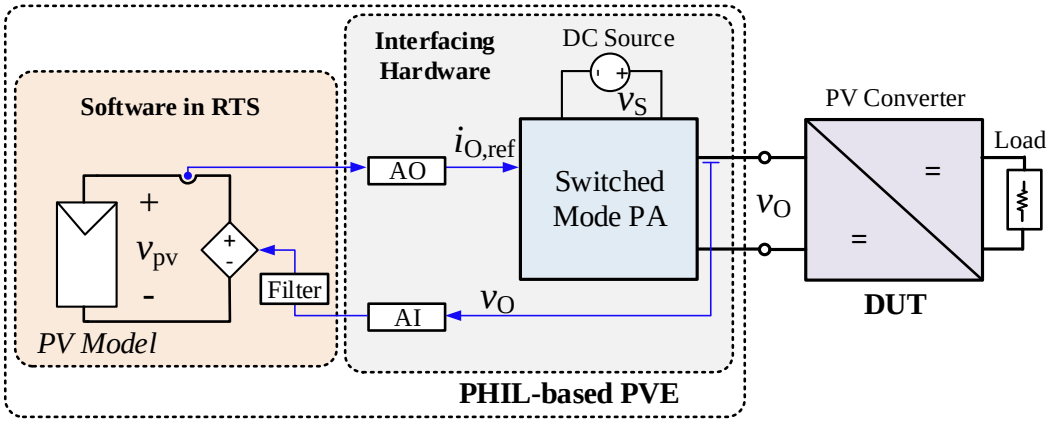


Figure 5.1 Block diagram of the proposed PHIL-based PVE.

5.2.1 Switch-mode Power Amplifier

Figure 5.2 shows the detailed architecture of the proposed CM PA, which consists of two main components, the PCS and the cascade control scheme. The PCS consists of a synchronous buck converter with a two-stage LC filter formed by an inductor L, a capacitor C, an outer inductor L_2 and an outer capacitor C_F. L_2 is designed to provide a high impedance path for high frequency current ripple components from the inner inductor current. The objective of C_F is to provide a circulating path for the current in L_2 when PVE is operated in open circuit condition rather than increasing the attenuation as generally done in the two-stage LC filter. Hence, C_F can be designed much smaller than C to push the second resonance frequency further away from the switching frequency f_S, avoiding any interactions with the control loop.

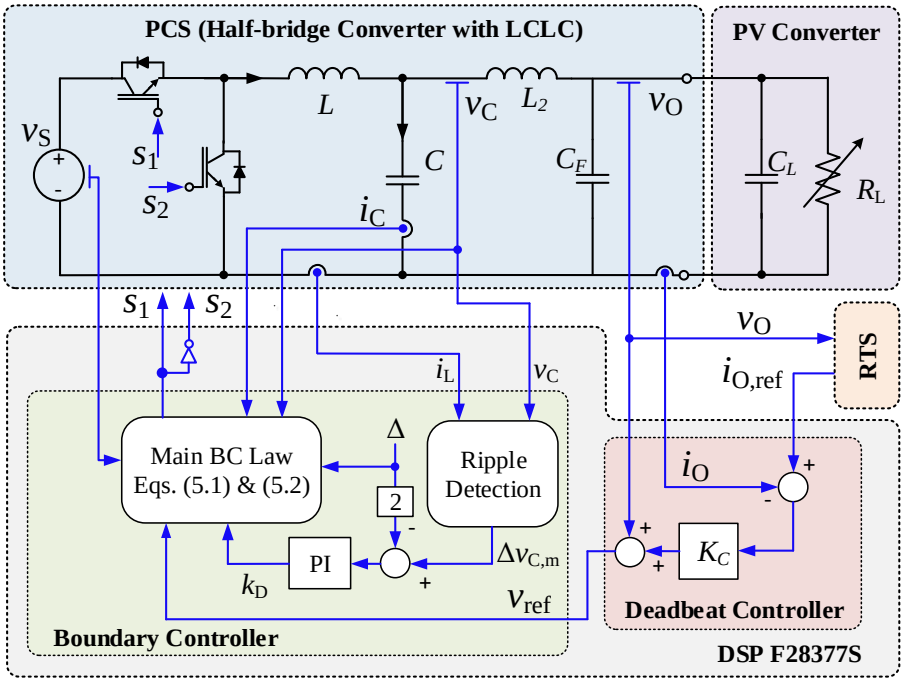


Figure 5.2 Architecture of the switch-mode PA on PHIL.

Control scheme utilizes a cascade control structure. The outer loop regulates the outer inductor current (i_O) by using a deadbeat controller that generates the voltage reference, v_{ref} for the inner loop. The inner control loop regulates the inner capacitor voltage (v_C) by using the σ_{cor}^2 proposed in Chapter 3. The σ_{cor}^2 determines the switching instants for S_1 and S_2 in PCS, and it precisely aids in determining correct switching criteria gains for any filter parameter variations compared to conventional BC schemes. From Section 3.3.4, the σ_{cor}^2 switching criteria for the synchronous buck converter can be re-written as,

Switch ON Criteria (S_1=1 and S_2=0)

$$v_C \leq v_{C,min} + k_1 k_D' {i_C}^2 \qquad \& \qquad i_C < 0 \tag{5-1}$$

Switch OFF Criteria (S_1=0 and S_2=1)

$$v_C \geq v_{C,max} - k_2 k_D' {i_C}^2 \qquad \& \qquad i_C > 0 \tag{5-2}$$

where $v_{C,min} = v_{ref} - \Delta$, $v_{C,max} = v_{ref} + \Delta$, $k_1 = \frac{L}{2C}\frac{1}{v_S - v_{ref}}$, $k_2 = \frac{L}{2C}\frac{1}{v_{ref}}$ and $k_D^{'} = (1 + \alpha)/(1 + \beta)$.

Here, Δ is the reference voltage band, and α and β are the tolerances of L and C respectively. The detailed derivation for the σ_{cor}^2 and design procedure for outer feedback loop and ripple detection block is given in Chapter 3. The σ_{cor}^2 provides ultra-fast response in voltage regulation, and it has been proven that control bandwidth of the inner BC control (i.e., v_C) is equal to the switching frequency in Section 4.5.2.2. Hence, the system-order controlled by the deadbeat controller can be viewed as an L-filter system even though the actual output filter is *LCL* type [99]. Thus, deadbeat current control law for the system is derived as,

$$v_{ref}[k] \cong K_c\big(i_{O,ref}[k] - i_O[k]\big) + v_O[k] \tag{5-3}$$

where $i_{O,ref}[k]$, $i_O[k]$, $v_O[k]$ and $v_{ref}[k]$ are values at the *k*-th sample and as per deadbeat control, it is considered that i_O reaches $i_{O,ref}$ within the specified sample period of T_{S1}. The gain of deadbeat controller, K_C is given as L_2/T_{S1} by neglecting the equivalent series resistance of L_2. Design considerations for the deadbeat controller will be discussed in Section 5.3.2.

Overall, this topology allows decoupling the effect of C_L to the inner voltage control loop enabling for applying any large-signal-based controller. The combination of deadbeat plus BC structure provides a fast current tracking capability and robust operation. It also benefits from the LCL filter's original advantage, requiring smaller reactive components than the LC filter.

5.2.2 Power Interface with ITM IA

Figure 5.3 shows how an original PV array simulation is extended to its corresponding PHIL-based simulation via a current-type ITM IA. The circuit is decoupled at the load connecting point as marked in Figure 5.3 (a), and a power interface is added to complete the circuit with actual loads. In current-type ITM IA, the current reference signal is sent out through the analog output (AO) card in signal level to the controller of the PA and load voltage is measured through a sensor at the load connecting point and fed back into the simulation through the analog input (AI) card. In this way, PA operates to mimic the I-V characteristics of a given PV model and real power is exchanged between PA and PV converter. A digital low-pass filter is used to eliminate the noise associated with voltage measurement, and its parameters should be selected to offer an acceptable trade-off between noise reduction, improve stability and system response.

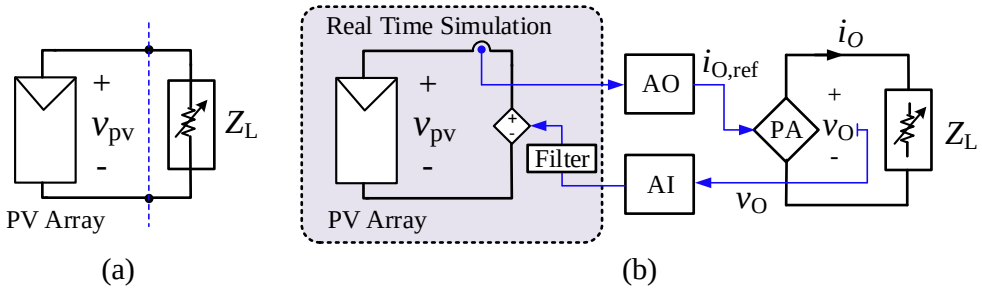


Figure 5.3 PV array (a) with RT simulation, and (b) with PHILS.

5.2.3 PV Array Modelling and Simulation in RTS

The PV model is an integral part of the PVE accuracy. A solar PV cell can be electrically represented using an equivalent circuit that includes a current source anti-parallel with a diode, a shunt resistance, and a series resistance, known as the single diode model, as shown in Figure 2.2. From the equivalent circuit, the basic I-V equation that characterizes the solar cell is given

by (2.1). Solving the non-linear I-V characteristics given by (2.1) accurately requires an iterative approach due to its implicit I-V relationship. However, finding a solution for (2.1) using an iterative approach in RT simulations is challenging. Hence, considering the small-time step used in RT simulations (i.e., <50 μs), the PV model in (2.1) can be solved by using the previous time step current and voltage values [6], [75] as given below,

$$I[k] = I_{PH} - I_{on}\left[exp\left(\frac{V[k-1]+R_S I[k-1]}{aV_t}\right) - 1\right] - \left(\frac{V[k-1]+R_S I[k-1]}{R_P}\right) \quad (5\text{-}4)$$

This method can be implemented in any RT circuit simulator that accepts embedded programming. However, RTS should be able to complete the calculation within the specified time step in real time. Further, (5.4) requires knowledge of all PV module parameters. When PV module parameters are unknown for given conditions, parameters can be extracted using analytical methods [38], [77], and iterative approaches using Newton-Raphson algorithm [38], [32] based data points obtained through experiments or manufacture's datasheets. This work used an iterative method presented in [32] to extract parameters based on the manufacture's datasheet values, and estimated parameters at standard test conditions of the BP365 PV module are given in Table 4.1. Further, parameter variation with temperature and irradiation needs to be considered, and detailed expressions are described in [32]. Once parameters are known for given G and T, time domain simulation of the PV array model can be achieved by numerically solving the I-V equation given by (5.4).

5.3. System Modelling and Analysis

The PHIL-based PVE consists of non-ideal components and factors such as sampling processes, digital computational delays, transmission latencies and analog/digital filters, leading to magnitude variations and phase shifts resulting in unstable poles [44]. Thus, the

small-signal model of the PHIL-based PVE is derived in this section to conduct small-signal stability and accuracy analysis at a given operating point. Key components of the system model include PV array, switch-mode PA, Giga-Transceiver Analog Output (GTAO) card, Giga-Transceiver Analog Input (GTAI) card and feedback filter. The block diagram that represents the PHIL-based PVE in Figure 5.1 is shown in Figure 5.4. The open-loop TF of this block diagram is given by,

$$T_{OL}(s) = \frac{Z_L}{R_{eq}} G_{AO}(s) G_{ii}(s) G_{AI}(s) G_{fil}(s) \tag{5-5}$$

where R_{eq} is the Thevenin equivalent resistance of the PV array, Z_L is the impedance of the DUT, $G_{\mathrm{AO}}(s)$ is the model of GTAO card in RTS, $G_{ii}(s)$ is the TF of proposed CM PA, $G_{AI}(s)$ is the model of GTAI card in RTS, $G_{fil}(s)$ is the TF of the voltage measurement/feedback filter. The following subsections describe the details about modelling the key elements that represent the PHIL-based PVE system.

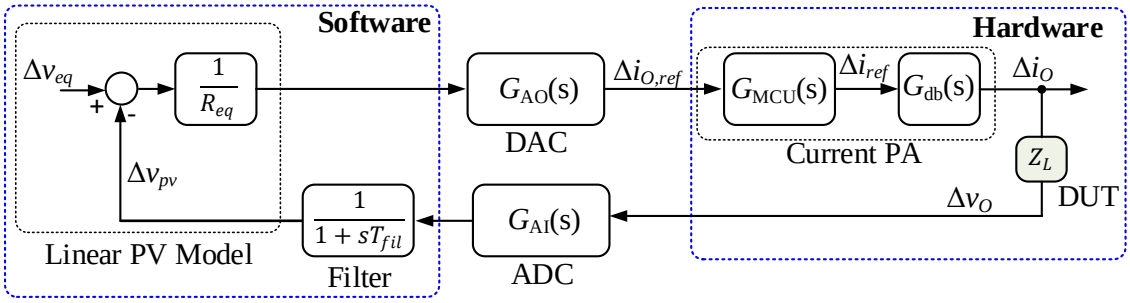


Figure 5.4 Block diagram of the PHIL-based PVE with current-type ITM.

5.3.1 Linearized Model of PV

The linear model of PV is described by the line tangent to the I-V curve at the linearization point (V_{pv}, I_{pv}) [137].

$$\Delta i_{pv} = \left(I_{pv} - g_{pv}V_{pv}\right) + g_{pv}\Delta v_{pv} \tag{5-6}$$

Further, this can be represented by an equivalent circuit shown in Figure 5.5 where $R_{eq} = -1/g_{pv}$, and $V_{eq} = V_{pv} - I_{pv}/g_{pv}$. The g_{pv} can be obtained by partially differentiating (2.1) at any operating point on the I-V curve and given by (5.7).

$$g_{pv}(V_{pv}, I_{pv}) = \frac{\Delta i_{pv}}{\Delta v_{pv}} = -\frac{\frac{I_O}{aV_t}exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right) - \frac{1}{R_{sh}}}{1+\frac{I_O R_S}{aV_t}exp\left(\frac{V_{pv}+R_S I_{pv}}{aV_t}\right) + \frac{R_S}{R_{sh}}} \tag{5-7}$$

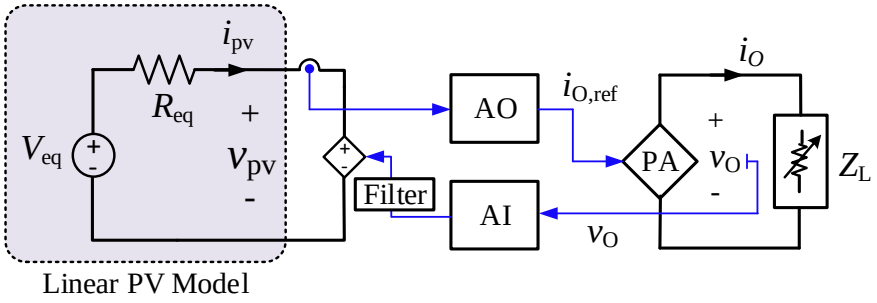


Figure 5.5 System configuration with linearized PV model.

5.3.2 Switch-mode PA Model and Design Criteria for Deadbeat Control

Figure 5.6 shows the control system block diagram of the proposed CM PA, including the inner BC scheme, outer deadbeat control and sampling effect on i_{Oref}.

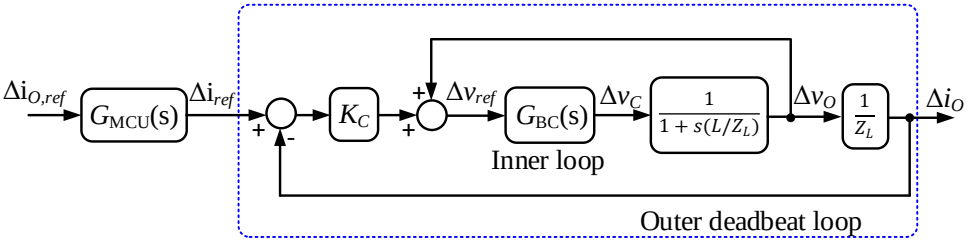


Figure 5.6 Control block diagram of the proposed CM PA.

As described in Chapter 3, closed-loop TF of the inner BC loop ($G_{BC}(s)$) can be estimated as a first-order low pass filter with a cross-over frequency of f_S.

$$G_{BC}(s) = \frac{\Delta v_C(s)}{\Delta v_{Oref}(s)} = \frac{1}{1+\tau_{fs}S} \tag{5-8}$$

where $\tau_{fs} = 1/2\pi f_S$. The switching frequency calculation for the boundary-controlled system is given in Chapter 3.3.3. The loop gain of the deadbeat controller can be derived from Figure 5.6 and it is given by,

$$G_{db}(s) = \frac{\Delta i_O(s)}{\Delta i_{ref}(s)} = \frac{K_C/Z_L}{s^2\tau_{fs}\tau+s(\tau_{fs}+\tau)} \tag{5-9}$$

where $\tau = L/Z_L$. Based on the parameters given in Table 5-1, Figure 5.7 shows the open-loop frequency response of the deadbeat controller for operating points in the CCR and CVR of the I-V curve.

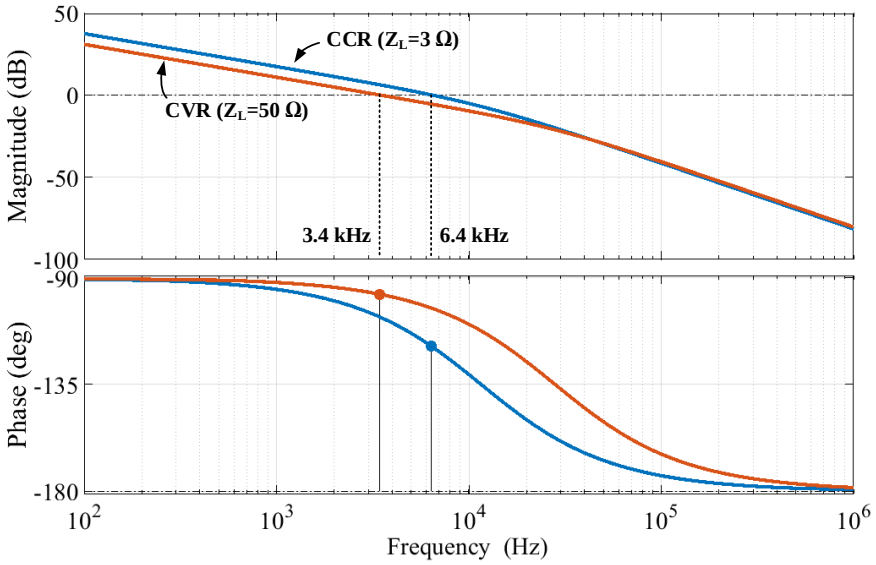


Figure 5.7 Bode plot for the open-loop TF of the PA.

It is seen that the bandwidth of the outer loop will be higher when PA operates in CCR compared to CVR. This is due to high loop gain resulting from the low load impedance (Z_L) in CCR. As shown in Figure 5.7, the bandwidth is 3.4 kHz and 6.4 kHz for a load of 50 Ω and 3 Ω, respectively. To avoid any interactions between the inner and outer loop, the outer loop's

bandwidth needs to be designed lower than the bandwidth of the inner loop. Additionally, the outer loop bandwidth should be designed considering an operating point in CCR since it has higher bandwidth than an operating point in CVR.

The sampling of the current reference signal by the microcontroller has been modelled as a continuous ZOH with an additional delay function, and it is given by,

$$G_{MCU}(s) = \frac{\Delta i_{ref}(s)}{\Delta i_{O,ref}(s)} = \frac{(1-e^{-sT_{MCU}})}{sT_{MCU}} e^{-sT_{PA}} \tag{5-10}$$

where T_{MCU} is the sampling period for i_{Oref} in the microcontroller and T_{PA} represents the input-to-output signal latency of the PA. The closed-loop TF of the switch-mode PA can be derived using (5.9) and (5.10), and it is given as,

$$G_{ii}(s) = \frac{\Delta i_O(s)}{\Delta i_{O,ref}(s)} = \frac{(1-e^{-sT_{MCU}})}{sT_{MCU}} e^{-sT_{MCU}} \frac{G_{db}(s)}{1+G_{db}(s)} \tag{5-11}$$

This model is validated experimentally using a gain phase analyzer (Bode100). Results are overlaid in Figure 5.8, which shows that the experimental result is in close agreement. The discrepancy between the theoretical model and experimental results at higher frequencies is mainly due to the approximations taken to derive the TF of the BC loop. By considering the bandwidth of the inner BC (i.e., 10.6 kHz at 3 Ω or 13.2 kHz at 10 Ω), the separation of the dynamic response between the internal and external loop is not evident. Thus, the outer control loop can be designed with higher control bandwidth, maintaining a higher overall bandwidth-to-switching frequency ratio compared to classical cascade control with linear PI controllers (i.e.,10%-20%). Further, the theoretical step responses of PA with resistive loads are shown in Figure 5.9 and response time is in the range of 133 µs to 195 µs with a time delay of 23 µs. It clearly shows that system has non-minimum phase characteristics due to the time delay.

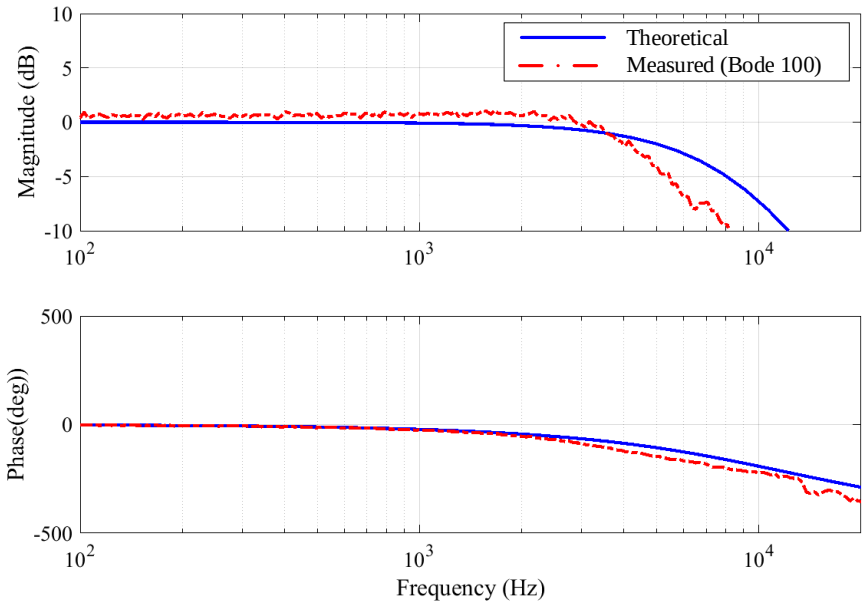


Figure 5.8 Model validation using the closed-loop frequency response of PA (operating point: 10Ω resistive load and i_{oref} 3.5 A).

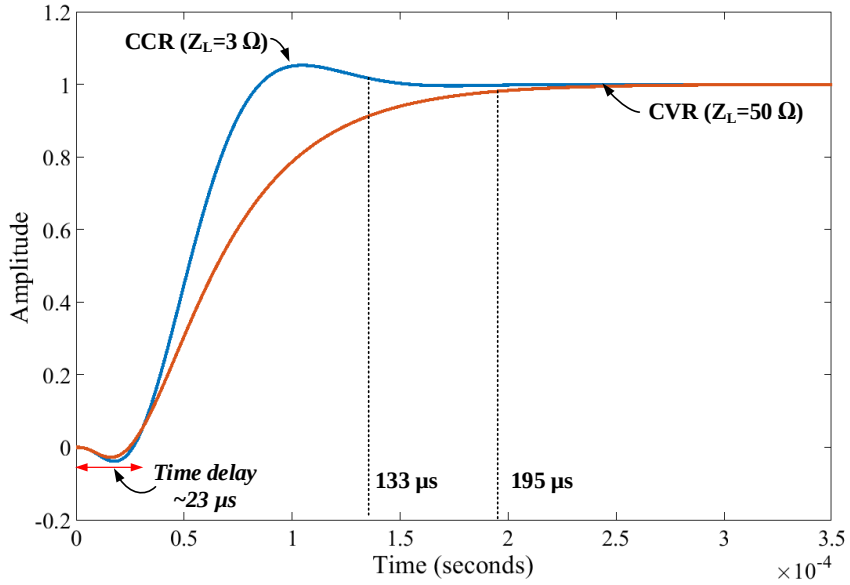


Figure 5.9 Step response of the PA.

Table 5-1 Key Parameters of the CM PA.

Parameter	Value	Parameter	Value	Parameter	Value
v_S	60 V	Δ	1 V	T_{S1}	20 μs
L	1 mH	L_2	0.5 mH	f_s	9.5- 14.1 kHz
C	4.7 μF	C_F	0.1 μF	PI (for k_D)	K_P=0.2 K_I=400

5.3.3 Modelling of Other Interface Devices

The GTAI card in RTS typically consists of anti-aliasing filter (AAF) and a sampler [23]. Sampling function is modelled using a continuous ZOH. This ZOH model is widely used in PHIL applications for its ability to capture a wide range of frequencies [44]. Thus, the model of GTAI is given by,

$$G_{AI}(s) = \frac{G_{aaf}(1-e^{-sT_{RT}})}{sT_{RT}(1+sT_{aaf})} e^{-sT_{AI}} \tag{5-12}$$

where G_{aaf} is the gain of AAF, $T_{aaf} = 1/2\pi f_{aaf}$ is the filter cut-off of the AAF, T_{RT} is the sampling time of the AO, which equals the time step of the RT simulation and T_{AI} is the ADC conversion time delay of the analog input card. The AO card and RT simulation process can be represented by a time delay.

$$G_{AO}(s) = e^{-s(T_{RT}+T_{AO})} \tag{5-13}$$

where T_{AO} is the DAC conversion time delay of the analog output card. Total latency of the loop (T_{total}) is given by,

$$T_{total} = T_{PA} + T_{RT} + T_{AO} + T_{AI} \tag{5-14}$$

The effect of T_{AI} and T_{AO} is minimal compared to T_{RT} hence one may neglect those from the analysis. The TF of the voltage measurement/ feedback filter is given by,

$$G_{fil}(s) = \frac{1}{(1+sT_{fil})} \tag{5-15}$$

where $T_{fil} = 1/2\pi f_c$, f_c is the cut-off of frequency of the filter. The latency of the sensor is negligible compared to the other time delays. Thus, it is ignored from this analysis.

5.3.4 Stability of PHIL System

Nyquist plots are used to determine the system stability based on the open-loop TF of the PHIL system derived from Figure 5.6. $T_{OL}(s)$ contains irrational terms due to the presence of exponential terms representing the latencies and DAC operation. To completely represent the effect of delays on stability analysis, the Nyquist plot is preferred over other existing tools [44]. A system consists of PHIL-based PVE connected to resistive loads is considered to conduct the stability test, and it is intended to emulate two BP365 modules connected in series. The PHIL interface parameters are summarized in Table 5-2, considering PHIL simulation is implemented in an RTDS™ simulator. The Nyquist stability test results for three different operating points on the I-V curve are shown in Figure 5.10. It indicates that the system is stable in all three operating points with the designed parameters listed in Table 5-2 and Table 5-3. However, the stability margin is much lower when the system operates in CVR compared to CCR and near MPP.

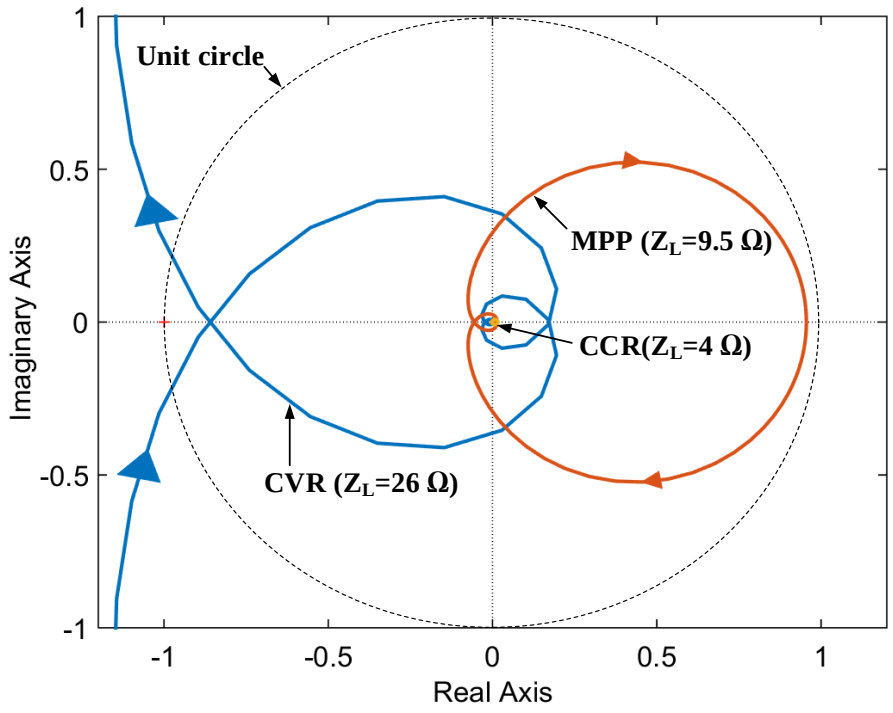


Figure 5.10 Nyquist plot of the PHIL-based PVE with resistive loads.

Table 5-2 PHIL Interface Parameters.

Parameter	Value	Parameter	Value	Parameter	Value
T_{RT}	50 µs	T_{AO}	9.2 µs	G_{AAF}	1
T_{AI}	7.2 µs	f_C	80 Hz	f_{aaf}	10.1 kHz
T_{MCU}	20 µs	T_{PA}	40 µs	T_{total}	126.4 µs

Table 5-3 Details of Operating Points for Stability Test.

	V_{Pv}	I_{pv}	f_s (Δ= 1V)	R_{eq}	Z_L/R_{eq}
CVR (26 Ω)	*41.6V*	*1.58 A*	*13.1 kHz*	*1.8 Ω*	*>1*
MPP (9.5 Ω)	*35.2 V*	*3.69 A*	*13.9 kHz*	*9.9 Ω*	*≅1*
CCR (4 Ω)	*15.9 V*	*3.92 A*	*7.98 kHz*	*4 Ω*	*<1*

Figure 5.11 shows the Nyquist stability test results of the system with or without the voltage measurement/feedback filter. The system becomes unstable when it operates without a feedback filter in CVR. Thus, it is necessary to implement the system with a feedback filter inside RTS to operate the PVE stably in all regions of the I-V curve. In summary, the developed mathematical framework can ensure a stable operation of the PHIL-based PVE. Moreover, it can be adopted to investigate the stability of the PHIL-based PVE connected to a PV converter by replacing all the Z_L terms in (5.5) by the closed-loop input impedance of the PV converter.

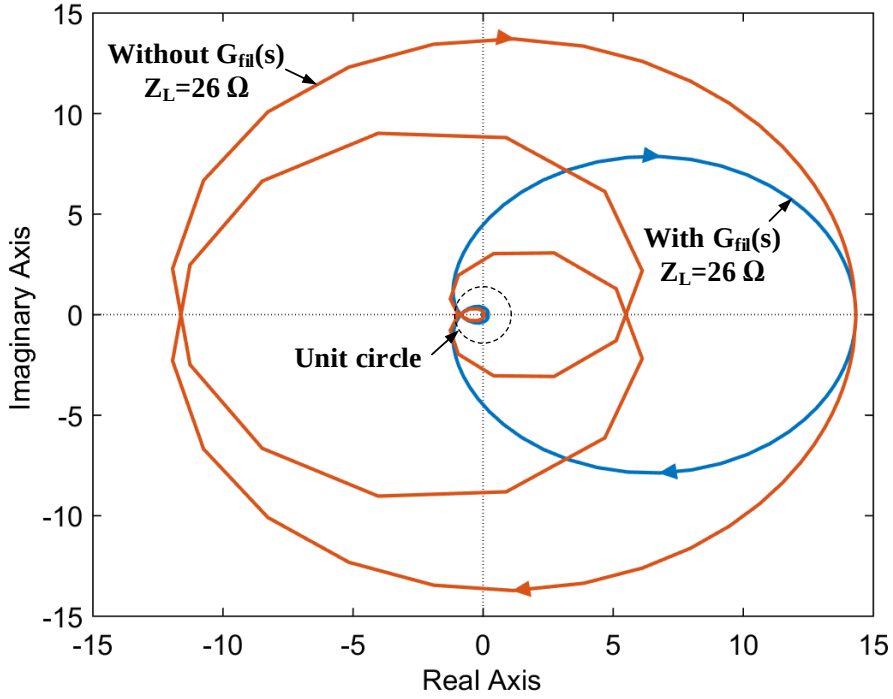


Figure 5.11 Nyquist stability test with/ without $G_{fil}(s)$ in CVR operation.

5.3.5 Accuracy Evaluation of the PHIL System

The accuracy of designed PHIL simulation for PV arrays is evaluated based on the method proposed by W. Ren et al. [62] in which the PHIL simulation error function is derived considering the perturbations caused by non-idealities of the interface as well as external

noises. It defines the perturbation comes from non-idealities of the power interface as the transfer function perturbation (TFP). The error function due to TFP (E_{TFP}) is derived as,

$$E_{TFP} = \left| W_0 \frac{G_{LP}(s)\Delta G_{int}(s)}{(1+(1+\Delta G_{int}(s)))} \right| \tag{5-16}$$

$$\Delta G_{int}(s) = G_{int}(s) - 1 \tag{5-17}$$

where G_{LP} (s) is the open-loop TF of the original circuit (i.e., without interface perturbation), $G_{int}(s)$ is the TF of the non-ideal interface and, W_0 is a weighting function for adding different accuracy levels at different frequencies [62]. From Figure 5.6, G_{LP} and $G_{int}(s)$ for PHIL-based PVE can be derived and, those are given by (5.18) and (5.19).

$$G_{LP}(s) = Z_L/R_{eq} \tag{5-18}$$

$$G_{int}(s) = G_{ii}(s)G_{AO}(s)G_{AI}(s)G_{fil}(s) \tag{5-19}$$

In this work, simulation error comes due to the TFP has only been investigated while noise perturbations are considered to be negligible. The E_{TFP} for i_O can be determined by solving (5.16). The theoretical error results of i_O over the frequency domain under different operating points on the I-V curves are plotted in Figure 5.12. The error is equally treated by taking W_0=1. It is seen that the normalized error below 1 Hz is < 0.02, which means that the PHIL interface would not have a significant impact on accuracy by applying PHIL simulation for PV emulation.

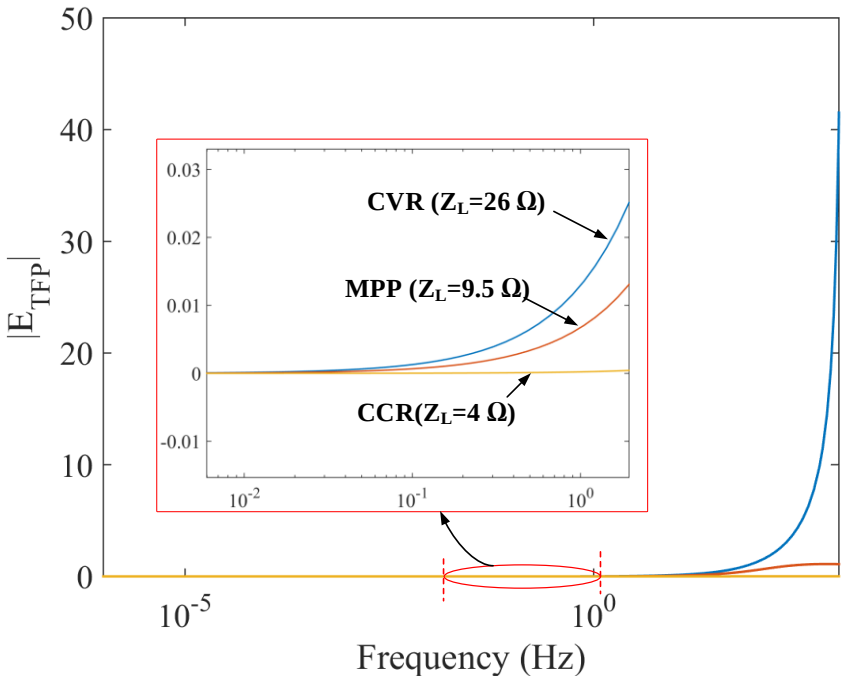


Figure 5.12 Predicted variation of TFP error function of i_O over frequency under different operating points on the I-V curve.

5.4. Experimental Validation

The proposed PHIL-based PVE has been implemented by connecting the RTDS™ simulator with a CM PA prototype and laboratory testbed is shown in Figure 5.13. A 130W synchronous buck converter prototype is implemented to operate it as the CM PA, and its design parameters are listed in Table 5-1. Control scheme of the PA is implemented using a Texas TI™ TMS320F28377S microcontroller. The BC scheme is implemented in an ISR running at 300 kHz, while the outer voltage ripple feedback loop and deadbeat controller are implemented in an ISR running at 50 kHz. All measured variables (i.e., i_O, i_L, i_C, v_C, v_O and v_S) are sampled at 300 kHz. The PV array circuit simulation is developed in RSCAD™, as shown in Figure 5.14. The real time simulation in RSCAD is solved with a time step of 10 µs.

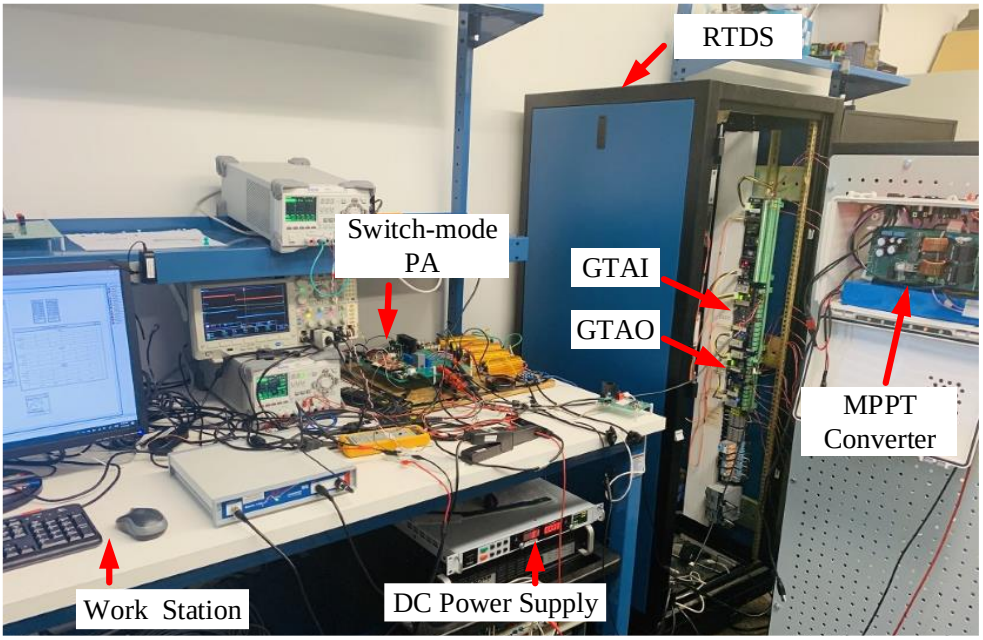


Figure 5.13 Testbed of PHIL-based PV Emulator.

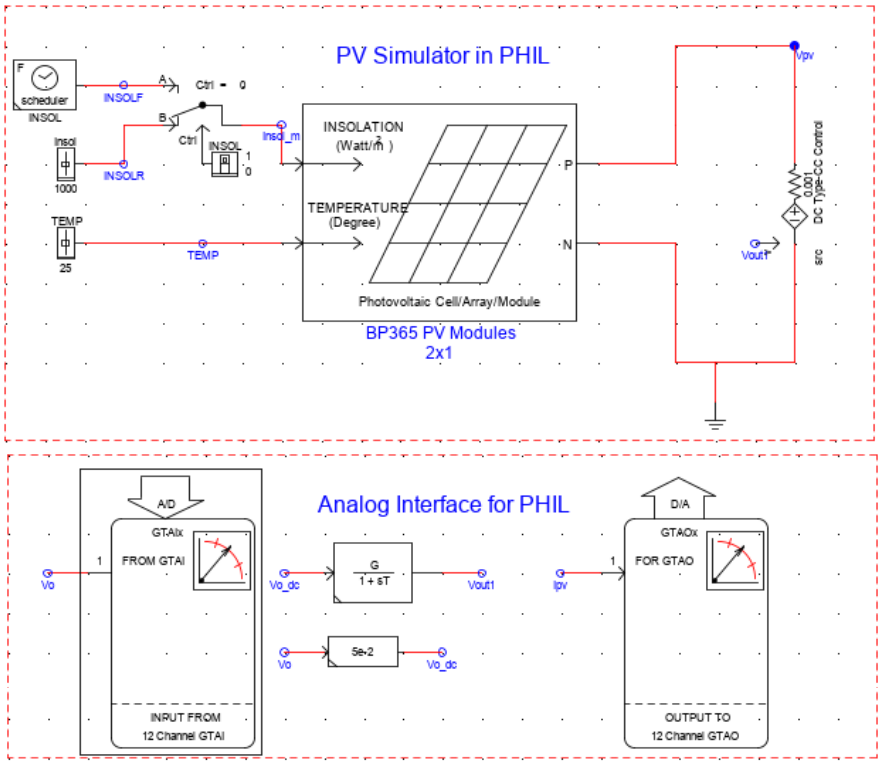


Figure 5.14 Implementation of PV array simulation in RSCAD

The designed PHIL-based PVE is tested with different loads, including resistive loads, TI™ solar micro-inverter and DC-DC PV converter prototype to validate its performance under steady-state and transient conditions. Following subsections provide experiment results under above mentioned load conditions.

5.4.1 Steady-state Performance with Resistive Loads

The steady-state performance of the proposed system is tested by operating it at different resistive load conditions. Figure 5.15 and Figure 5.16 show the output waveforms (i.e. v_O, i_O) of PVE in steady-state for load condition that lies in CCR and CVR, respectively. Results show that stable operation of PVE is achieved in both regions of the I-V curve. Similarly, Figure 5.17 (a) illustrates the steady-state operating point trajectories for different load levels on I-V plane when PVE is intended to emulate a PV array with two BP365 modules connected in series. It is tested with a maximum load of 4.75 Ω and until open circuit voltage output and operating points are compared with the reference I-V curve of 1 kW/m^2 and 0.5 kW/m^2.

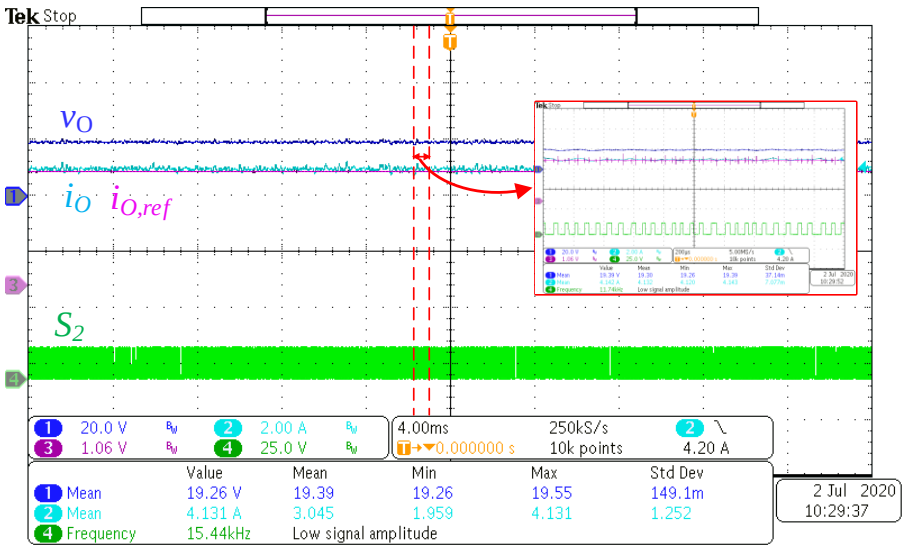


Figure 5.15 Experimental results of steady-state operation with 4.75 Ω (in CCR).

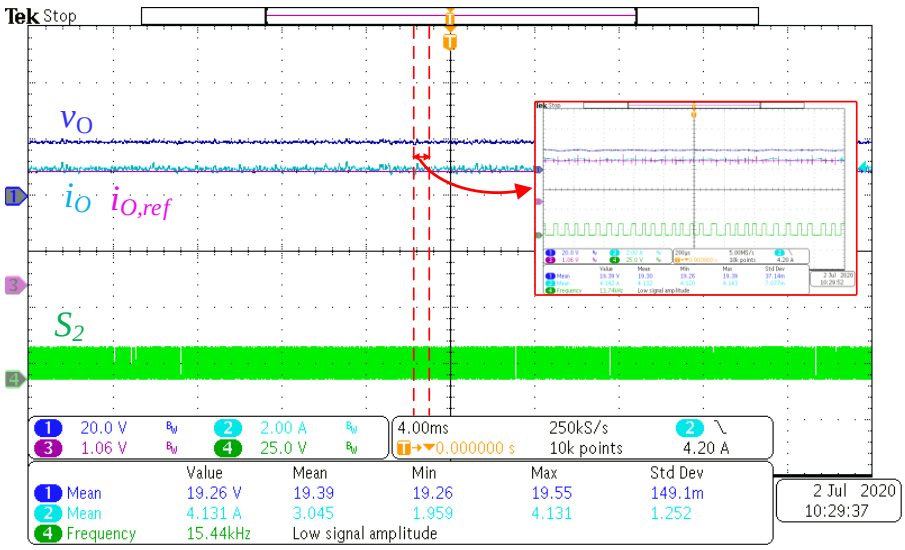
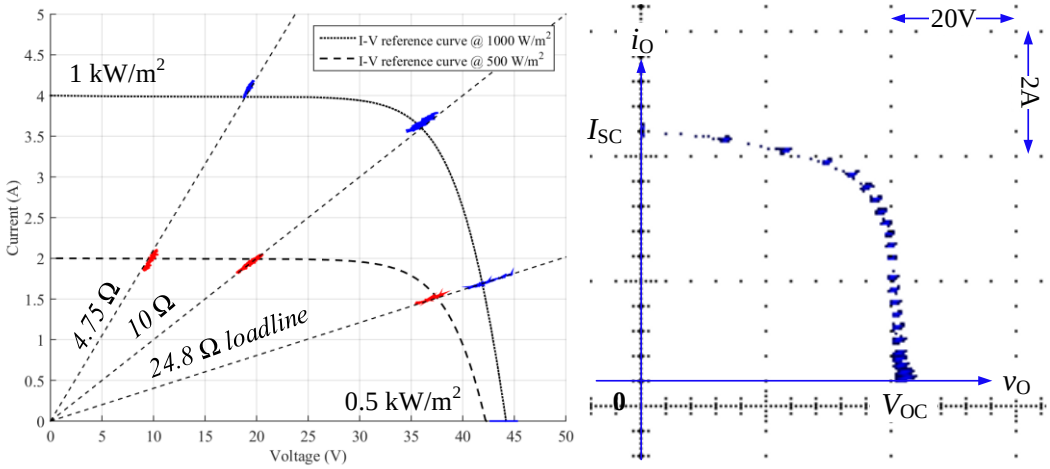


Figure 5.16 Experimental results of steady-state operation with 25 Ω (in CVR).



(a) (b)

Figure 5.17 Steady-state I-V trajectory with (a) resistive loads, and (b) dc electronic load at 1 kW/m^2

Figure 5.17 (b) shows the experimental I-V curve generated by connecting to a commercial DC electronic load (KEIETHLY 2380-500-30). To characterize the proposed PVE, the DC electronic load is operated in constant voltage mode, and the set voltage is manually changed from V_{OC} to 5V. To evaluate the accuracy of the proposed PVE, average

values of v_C, i_O are measured and compared with RSCAD PV model RT simulation results. Table 5-3 presents the comparison results, and it shows that error percentages are within 4.1 %.

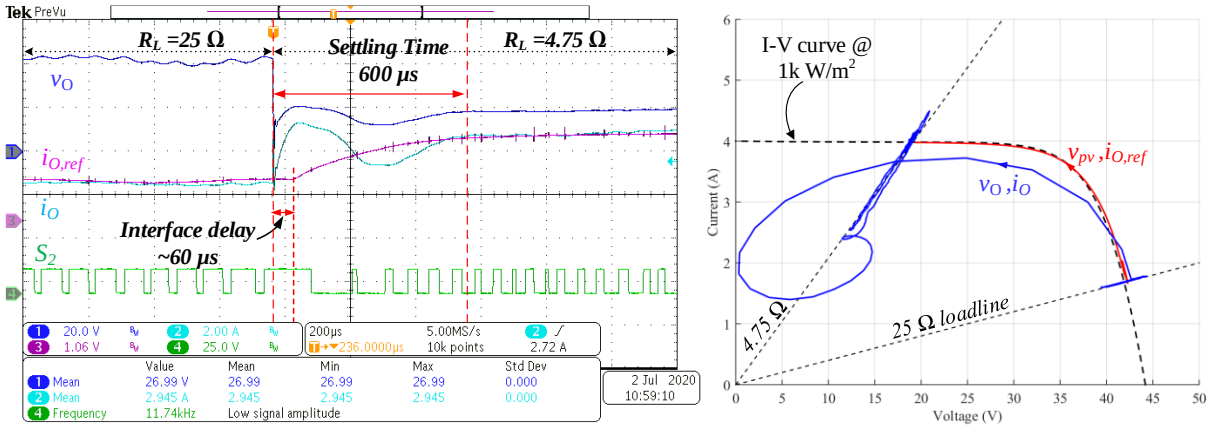
Table 5-4 Accuracy Evaluation of the Proposed PHIL-based PVE.

Z_L		v_O (V)		Error	i_O (A)		Error
		RSCAD	PVE	%	RSCAD	PVE	%
1 kW/m^2	24.8 Ω	41.23	41.85	0.90%	1.703	1.685	1.04%
	10Ω	36.06	36.07	-0.02%	3.606	3.666	-1.67%
	4.75 Ω	18.9	19.38	-2.54%	3.978	4.140	-4.07%
	OC	44.2	43.90	0.68%	0	-	0.00%
0.5 kW/m^2	24.8 Ω	37.08	36.42	1.77%	1.495	1.483	0.82%
	10.8 Ω	19.87	19.55	1.61%	1.987	1.961	1.28%
	4.75 Ω	9.46	9.81	-3.69%	1.993	1.997	0.00%
	OC	42.3	40.93	3.24%	0	-	0.00%

5.4.2 Transient Performance with Resistive Loads

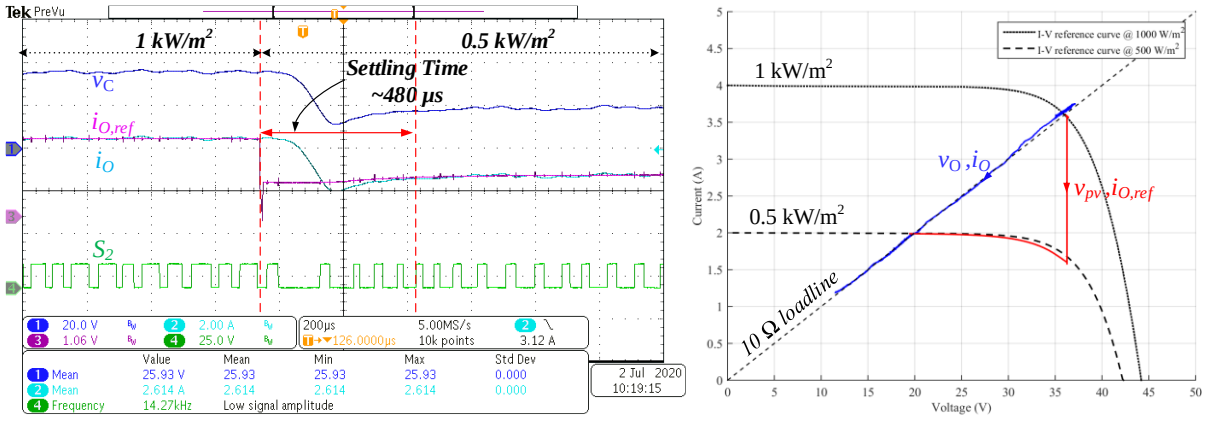
The dynamic performance of PHIL-based PVE is tested with resistive loads that allow the application of fast load transients and verify its dynamic performance. Experiments results for a load step-up transient (25 Ω to 4.75 Ω) in time and I-V domains are shown in Figure 5.18. This test is performed under the condition of G=l kW/m^2, T=25 ºC and recorded settling time is approximately 600 µs as shown in Figure 5.18 (a). Further, the total time delay of the signal interface from v_O to $i_{O,ref}$ is recorded ~60 µs. The PHIL-based PVE reaches steady-state within a few switching actions, and the switching frequency is in the range of 12.1 kHz to 12.5 kHz. The I-V trajectory during this transient is presented by Figure 5.18 (b). Similarly,

transient response for an irradiance step-down from 1 kW/m^2 to 0.5 kW/m^2 is shown in Figure 5.19. The dynamic response time of the system is found to be ~480 µs, including the latency of the interface.



(a) (b)

Figure 5.18 Experimental results for a load step-down (50.3 Ω to 9 Ω at 1 kW/m^2) in (a) time domain (b) I-V plane.



(a) (b)

Figure 5.19 Experimental results for a step change in solar irradiance from 0.5 kW/m^2 to 1 kW/m^2 at 10.8 Ω in time and I-V domain.

5.4.3 Performance of the switch-mode PA stage and Discussion

The dynamic response of the current-mode PA stage is evaluated separately by applying a step response, and results are shown in Figure 5.20. Multiple test runs were made to determine dynamic characteristics of the current-mode PA and found out that settling time is < 300 µs and input-to-output delay time is ~ 40 µs. Table 5-5 summarises the dynamic performance and characteristics of the proposed PA, dynamic switch-mode PVEs and commercial PAs. As shown in Table 5-5, the proposed PHIL-based PVE has a fast current tracking ability for an operating f_S range of 9.5 kHz-14.1 kHz compared to existing switch-mode PVEs in recent literature. Even though proposed PA demonstrated as an exciting prospect to achieve fast response, it is evident that the PA response time with its current hardware platform is not comparable enough with linear PAs.

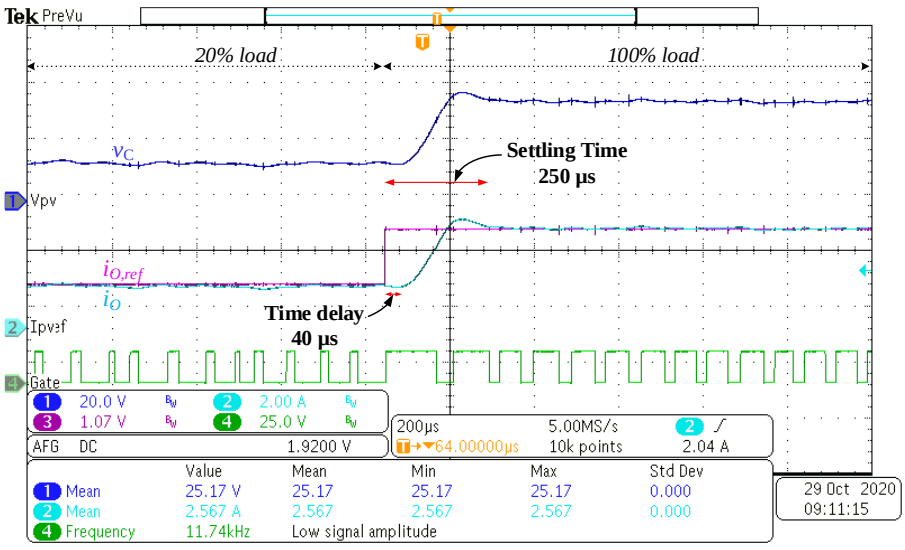


Figure 5.20 Step response of the current-mode PA.

Table 5-5 Dynamic Performance and Characteristics Comparison with Existing PVEs and Commercial PAs

PVE	***Settling time for a load step change***	***Power Stage***	***Control Method***		***Switching Frequency***
			Inner Control	***Reference Generation***	
Proposed PHIL-based PVE	<600 µs	Synchronous buck converter with LCLC filter	BC + deadbeat	PHIL simulation of PV	9.5-14.1 kHz
Nguyen-Duy 2016 [18]	10 µs (Fig.17 in [18])	Synchronous buck converter with LCLC filter	PID (VM)	PV array small-signal circuit	1 MHz
Koran 2010 [64]	3.8 ms (Fig.17 in [64])	DC-DC buck converter with LCLC filter	PID (CM)	PV equivalent circuit	30 kHz
Chang 2013 [65]	6 ms (Fig.12 in [65])	LLC resonant DC-DC converter	Freq. modulation	Not found	60-250 kHz
Commercial PA	***Large-signal Bandwidth***	***Power Stage & Control***	***Dynamic Characteristics***		***Switching Frequency***
			Slew ate	***Settling Time***	
Opal-RT OP1400-10 [112]	0 - 10 kHz	Switch-mode PA (Proprietary)	5 V/µs	-	Proprietary
Egston CDA [111]	0 - 5 kHz	Switch-mode PA (Proprietary)	-	-	Proprietary
AE Techron 7224 [25]	0-300 kHz	Linear PA (Proprietary)	75 V/µs	<10 µs	Not Applicable
Spitzenberger & Spieß PVS1000 [20]	-	Linear PA (Proprietary)	-	100 µs	Not Applicable

To achieve better dynamic responses, the inner BC scheme should be operated with higher f_S, which allows to design outer deadbeat controller with a higher bandwidth. The f_S of the BC scheme can be increased with proper choice of parameters like L, C, Δ and sampling frequency according to (3.14). A simulation is performed using PLECS^{TM} to demonstrate this case which requires an advanced hardware platform that compliment BC scheme as well as topology with high f_S. Figure 5.21 shows the simulation results for the step response of a BC + deadbeat control employed synchronous buck converter with a two-stage LC filter for the parameters tabulated in Table VII. The transient response time of 26.5 µs for switch-mode PA

is a significant improvement that shows the possibility of having improved dynamic response close to linear PAs with the selection of proper hardware.

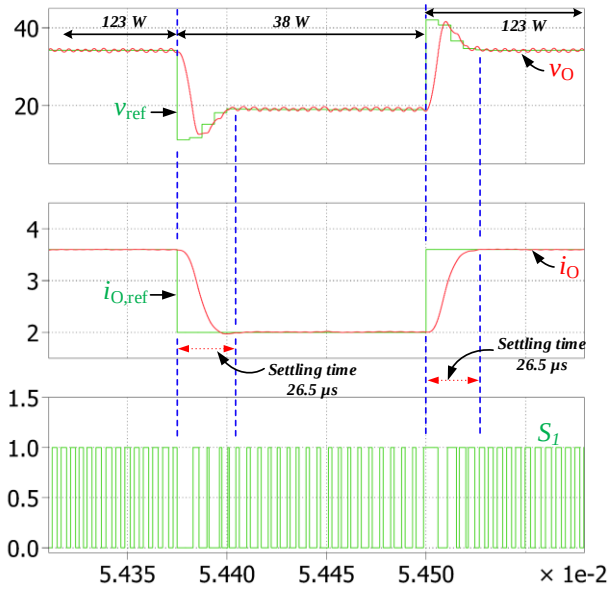


Figure 5.21 Simulation results for a step response of the switch-mode PA.

Table 5-6 Simulation Parameters of the CM PA

Parameter	Value	Parameter	Value	Parameter	Value
v_S	60 V	Δ	0.25 V	T_{S1}	6.25 µs
L	100 µH	L_2	100 µH	f_s	16 - 43 kHz
C	0.5 µF	C_F	0.1 µF	PI (for k_D)	K_P=0.2 K_I=400

Main considerations for implementing BC scheme with high f_S are the sampling rate of measured signals required for control law and computation time. The TI™ TMS320F28377S DSP used in this chapter does not meet the requirements mentioned in simulations. However, this proven concept can be easily extended to achieve an ultra-fast response compatible with commercial PAs, as given in Table 5-5, with the use of advanced hardware like ADC with high precision and high sampling rate, FPGA for implementing control law and use of SiC/GaN

semiconductor switches. Further, the proposed PA can be scaled up for applications requiring high power by applying this control scheme on a multiphase interleaved DC/DC converter.

5.4.4 Evaluations with PV conditioning systems

In this section, the static and dynamic performance of a solar micro-inverter and non-commercial DC-DC PV converter for micro-grid applications are tested using the proposed PHIL-based PVE to evaluate the performance of PVE as well as the MPPT controller.

5.4.4.1 With grid-connected micro inverter

The TI™ solar micro-inverter consists of two power stages: the flyback stage and the inverter stage [135]. The flyback stage controls the current from the PV source such that the PV module operates at its MPP. The technical specifications of the micro-inverter are tabulated in Table 5-7. Figure 5.22 (a) shows the waveforms of the proposed PVE when the irradiance level is changed from 0.5 kW/m^2 to 1 kW/m^2. It shows that the micro-inverter is searching for a new MPP after the change. Before and after the MPP search, it shows stable DC voltages at PVE: the overall system is in steady-state and operating at the MPPs. To demonstrate that it is operated at V_{MPP}, I_{MPP} and P_{max}, Figure 5.22 (b) and (c) presents the waveform trajectory for different irradiance levels, including 1 kW/m^2 and 0.5 kW/m^2 in the I-V and P-V domains. It shows that i_O is tightly regulated by the PVE at I_{mpp} with an accuracy of 1.9 % and static MPPT efficiency is kept higher than 94 %. This also includes the error due to the PHIL interface. The micro-inverter operated correctly with the proposed PVE as maximum power has been extracted under steady-state.

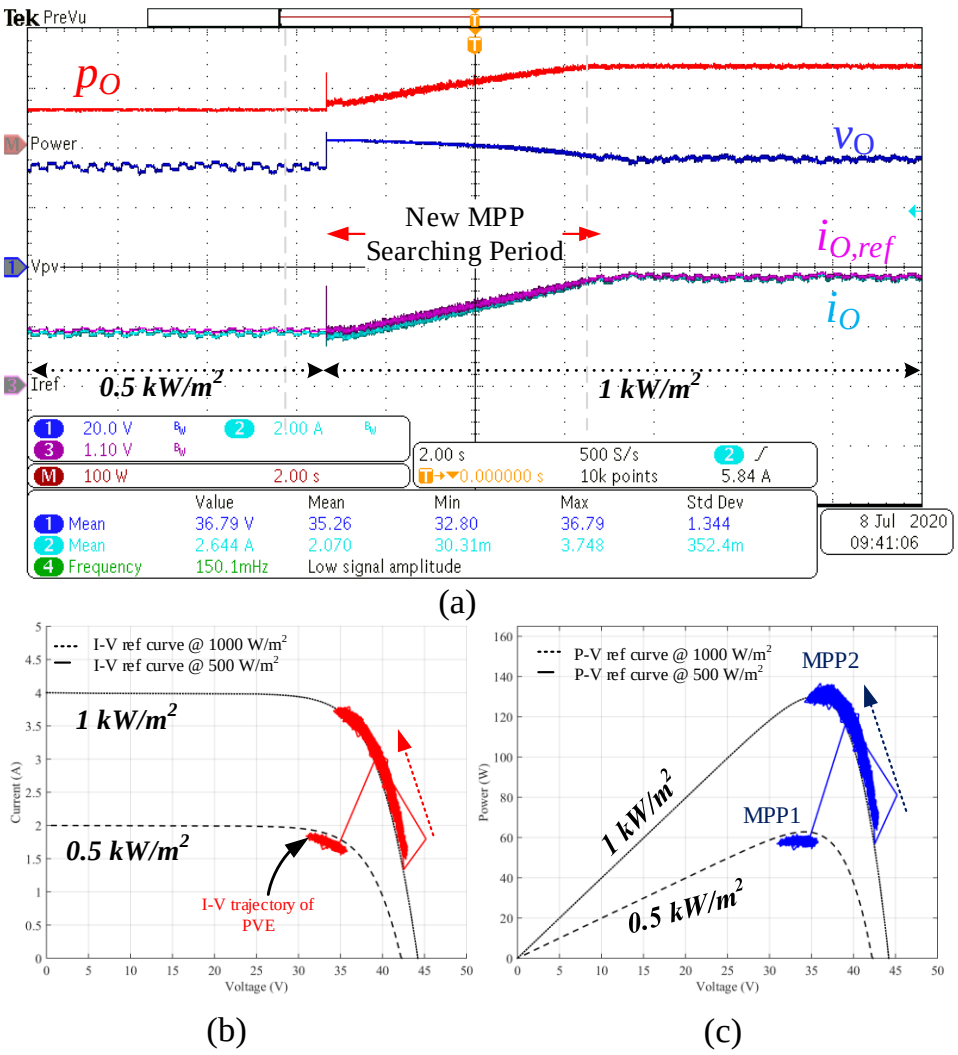


Figure 5.22 Transient response of the PVE with a MPPT micro inverter for irradiance step-up from 0.5 kW/m^2 to 1 kW/m^2 (a) time (b) I-V (c) P-V domain.

The dynamic MPPT efficiency test is performed according to EN50530 by applying a test sequence for fluctuations between medium and high irradiation intensities [136]. The dynamic MPPT test results are shown in Figure 5.23, and the recorded dynamic MPPT efficiency from the PHIL-based PVE is 95 %.

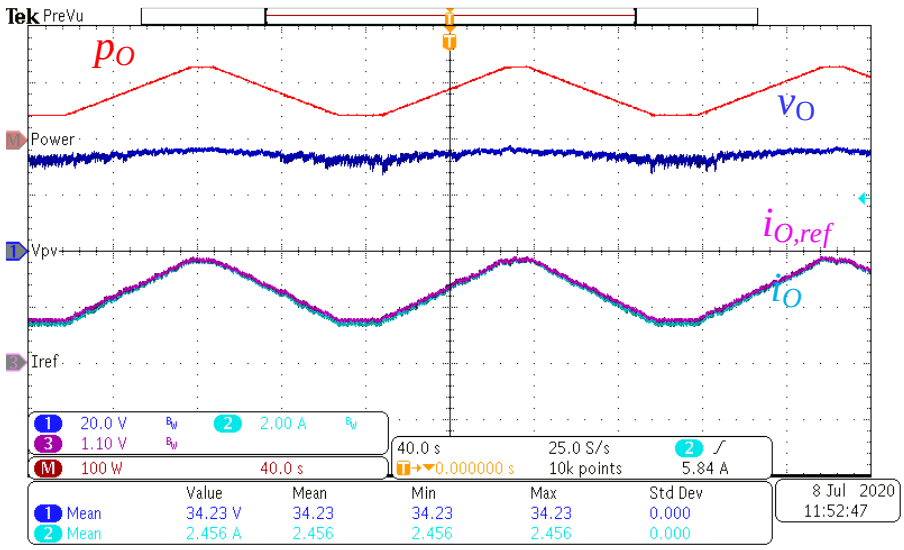


Figure 5.23 Dynamic MPPT test under EN 50530 with proposed PVE.

Table 5-7 Specification of the evaluated PV conditioning systems

Solar micro inverter (TI TMDSSOLARUINVKIT)			
Parameter	Value	Parameter	Value
Solar Panel Output	25 V- 44V	Output Voltage	110 Vrms
Rated Power for 110Vrms	140 Wmax	Power Resistor	200 Ω
DC-DC PV Converter (Non-commercial)			
Parameter	Value	Parameter	Value
Solar Panel Output	5 V- 30V	Output Voltage	48 Vdc
Rated Power	100 Wmax	Battery capacity	10 Wh

5.4.4.2 With DC-DC PV converter

A DC-DC PV + battery energy storage (BES) converter proposed in [138] for scalable plug-n-play DC microgrids is used to conduct this test. This power conditioning unit can be integrated into a module-based hierarchical microgrid architecture with fully decentralized control, and its technical specifications are tabulated in Table 5-7. Figure 5.24 shows the output waveforms of the proposed PVE for an irradiance step change from 1 kW/m^2 to 0.3 kW/m^2

with the PV converter as the load. It shows that system is in steady-state and operating at the MPPs before and after the MPP search. The oscillation during the transient is possibly due to the MPPT control loop of the PV converter. The MPPT controller has considerable oscillation during the steady-state operation, suggesting that the MPPT controller's performance needs to be improved for better performance. These experimental results suggest that the proposed PHIL-based PVE has a fast transient response relative to tested MPPT algorithms.

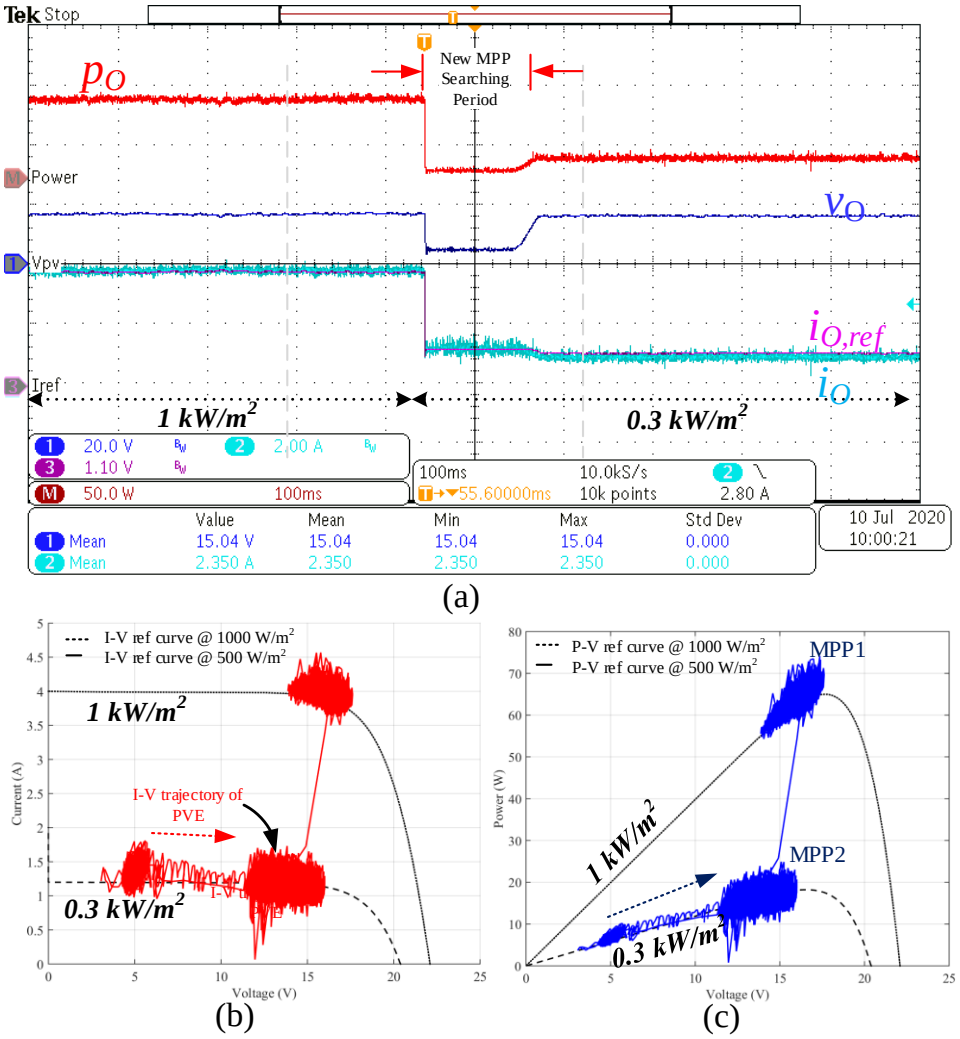


Figure 5.24 Transient response of PVE with a DC-DC PV converter [138] for irradiance step-up from 0.5 kW/m^2 to 1 kW/m^2 (a) time (b) I-V (c) P-V domain.

5.5. Summary

This chapter described and demonstrated a PHIL-based switch-mode PVE that enhances PV emulation flexibility for testing PV converters in grid integration testbeds with RTSs. The proposed PVE is formed by integrating a PV array model in RTDS™ with a switch-mode PA via current-type ITM IA. Use of IA allows for seamless integration with RT PV array simulation platforms that can be easily configured to apply different contingency test scenarios by varying irradiance, temperature, and even partial shading conditions. In this work, the switch-mode PA is realized by using a synchronous buck converter with a two-stage LC filter and a combination BC plus deadbeat controller is applied to achieve a fast transient response minimizing the interface latency. Results showed that the proposed power stage and controller of the PA guarantee wide control bandwidth without increasing the switching frequency and eliminate the effect of load capacitance on the non-linear voltage control loop's performance in PVEs. The system design considerations have been discussed in detail. Further, a comprehensive small-signal model of the PHIL-based PVE has been derived to analyse stability and accuracy under different operating points on the I-V characteristics curve. Designed emulator is validated experimentally with both resistive loads and PV converters. The results of the PHIL-based PVE showed a stable and accurate operation under steady-state and during load and irradiance transient conditions.

Chapter 6

Power Electronics based-Power-HIL Testbed for Evaluating PV-BES Converters on DC Microgrids

In this chapter, a real time PHIL testbed, suitable for evaluating DC-coupled PV-BES converters on scalable DC microgrids, is introduced by employing the fast-dynamic voltage-mode PA presented in Chapter 3 to mimic the DC grid behavior and the current-mode PA presented in Chapter 5 to mimic the PV array response. The boundary-controlled VM PA presented in Chapter 3 is modified by adding a second-stage passive LC filter to maintain the system performance under all types of non-linear switching loads. BC-based advanced control schemes improve the dynamic response of switch-mode PAs and provide robustness with CPLs. To highlight the proposed testbed's applicability, PHIL simulation results of a fully decentralized DC MG are presented with two DC-coupled PV-BES converters, in which one power unit is modelled inside RTS, and it is interfaced to a physical converter using the PHIL technique.

6.1. Introduction

Scalable DC microgrids have gained more attention among academia and industry as a promising solution to the energy poverty problem in rural areas [139]. However, developing complex DC MGs requires conducting studies and rigorous testing. Hardware implementation and experimental verifications of a complex MG are expensive and perhaps not even feasible to reproduce under full experimental setups. As highlighted in Chapter 1, the application of real time PHIL testing for DC MG development is an appropriate approach as it offers a platform for integrating the PEs-based physical hardware with real time software simulations [36]. It allows to test and validate real PE converters within the complex system they operate with various advantages in terms of flexibility, space requirement, time and perhaps most importantly, low-risk testing.

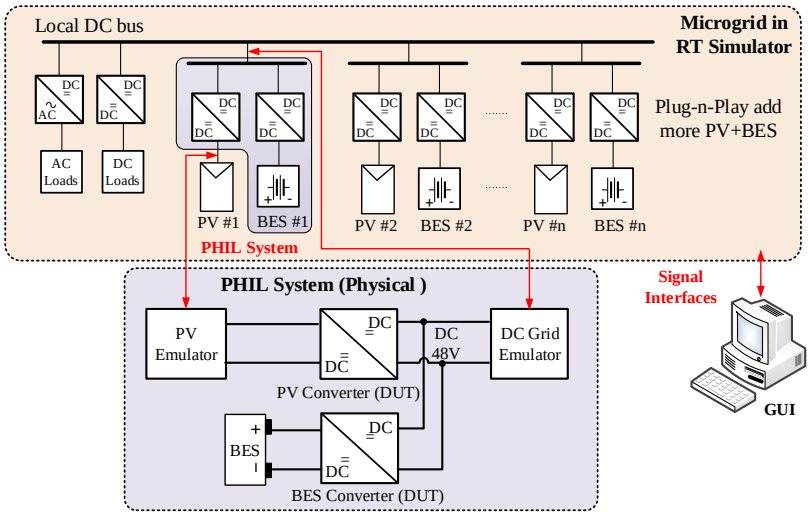


Figure 6.1 Conceptual PHIL test configuration of a scalable microgrid with PV-BES systems.

In this regard, this chapter aims to develop a PHIL testbed with fast-dynamic switch-mode PAs for evaluating DC-coupled PV-BES systems. Figure 6.1 shows the conceptual PHIL

test configuration of a PV-BES converter connected to a scalable MG with multiple PV-BES systems. Unlike conventional PHIL grid integration testbeds based on standalone source emulators, it consists of two PHIL simulations to emulate both PV array and DC MG response. Use of multiple PHIL simulations will enhance the flexibility of the testbed, which will lead to rapid and cost-effective prototyping. Having a high-bandwidth PA is crucial to minimize delays in the power interface of PHIL. Therefore, in the proposed PHIL testbed, CM PA developed in Chapter 5 is directly applied to mimic the PV array response, while PHIL-based DC grid emulator is developed based on the VM PA proposed in Chapter 3. In Chapter 3, a BC with a corrected second-order switching surface is presented to regulate the output voltage within a specified band under capacitive loads and filter parameter variations. Nevertheless, the PA's switching frequency and output current ripple still depend on the load capacitance. Therefore, in this chapter, the PCS of the VM PA is modified by adding a second-stage passive LC filter to decouple high-frequency current ripple components led by load converter passing into the PA and vice versa. Therefore, this enables applying the BC scheme through the inner LC filter and regulating inner capacitor voltage without affecting PA's performance in switching frequency, output current and voltage ripple due to the switching-load converter.

The rest of the chapter is organized as follows: Section 6.22 describes the testbed configuration, including the PHIL interface design, power stage and controller design consideration of the VM PA for DC grid emulation. The outer passive LC filter design considerations to maintain an accurate output voltage and retain fast dynamics are also discussed. The modelling of PV-BES converters for real time simulation is described briefly in Section 6.3. Section 6.4 shows the experimental performance of the PHIL testbed with a PV-BES power module proposed in [138] to demonstrate the application of the platform.

6.2. Configuration of the PHIL Testbed

Figure 6.2 shows the detailed system configuration of the proposed PHIL testbed for evaluating PV-BES systems that consist of two PHIL simulations to emulate PV array response and DC grid behavior.

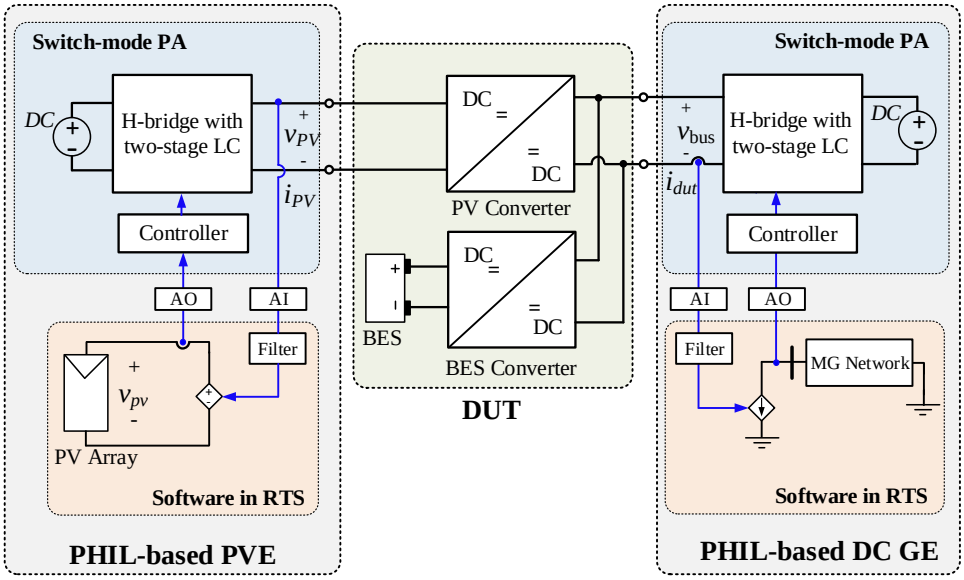


Figure 6.2 Block diagram of the PHIL testbed for PV-BES converters on DC MG.

6.2.1 PHIL-based PVE

The PHIL-based PVE developed in Chapter 5 is directly applied to emulate the PV array source of this test setup. The PHIL-based PVE is implemented using the current-type ITM IA since current-mode control is used in the PA. As shown in Figure 6.2, the PV array current from the PV model in RTS is interfaced to the PV converter input terminals through a DAC and switch-mode PA, and the voltage measurement of the PV converter is sent back to the RTS through an ADC to complete the virtual PV model simulation. In this way, current-mode PA operates to imitate the current-voltage (I-V) characteristics of a given PV model and real power is exchanged between PA and PV converter. The detailed design of the CM PA is

described in Chapter 5, including the stability evaluation and experimental validation of the PHIL-based PVE.

6.2.2 PHIL-based DC Grid Emulator

Like the PHIL-based PVE, the PHIL-based DC grid emulator (GE) schematic with all measurement points at the hardware and software runtime environment is shown in Figure 6.2. The PHIL-based PVE is developed by decoupling the DC MG network simulation using the voltage-type ITM IA. The DC bus voltage from the simulated MG network in RTS is interfaced to the PV-BES power module output side through a DAC and voltage-mode PA. The current measurement is sent back to the RTS to compute the state of the modelled MG network. In both PHIL-based emulators, a digital low-pass filter is used to eliminate the noise associated with current measurement, and its parameters should be selected to offer an acceptable trade-off between noise reduction, improve stability and system response.

6.2.2.1 Voltage-mode PA Design

The delay and limited bandwidth of the PA in PHIL significantly affect the stability and accuracy of a PHIL. Thus, voltage-mode PA with fast-dynamic characteristics is proposed in this section. Figure 6.3 shows the detailed architecture of the proposed VM PA, which is developed by extending the VM PA presented in Chapter 3 by adding a second-stage LC filter to the PCS. The PCS consists of a synchronous buck converter with a two-stage LC filter formed by an inductor L, a capacitor C, an outer inductor L_2 and an outer capacitor C_F. The second-stage LC filter is placed to decouple the loading capacitor effect and minimize the load converter switching effect on the source converter's nonlinear control loop. L_2 is designed to provide a high impedance path for high-frequency current ripple components from the inner inductor

current and vice versa. Basically, this arrangement would separate C from load capacitor (C_L) and allow to apply a large-signal-based controller through the inner LC filter for achieving fast response. Thus, the control scheme utilizes a BC with corrected second-order switching surface to regulate the inner capacitor voltage (v_C) and thereby maintaining the output voltage (v_O). Design criteria for the second-stage LC filter is given in the next section. The switching ON and OFF criteria of σ_{cor}^2 for the synchronous buck converter is given in Chapter 3.

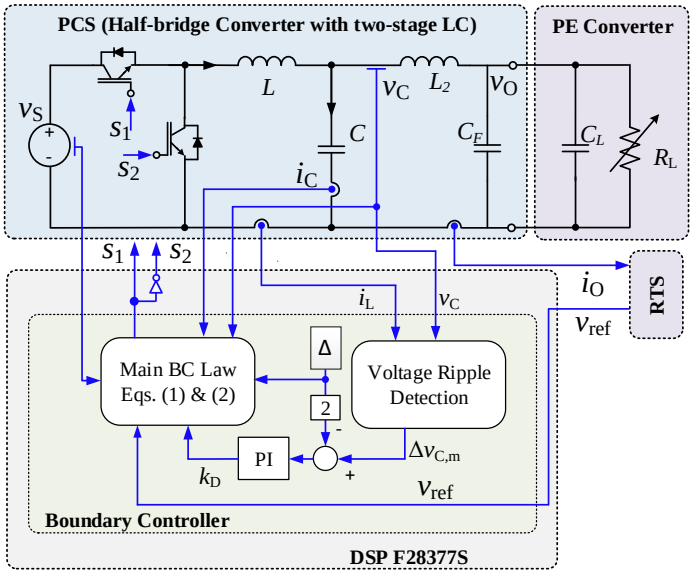


Figure 6.3 Detailed system configuration of the proposed voltage-mode PA.

6.2.2.2 Second-stage LC filter design

Designing the first-stage LC filter for a converter with BC is straightforward, as already described in section 4.2.3. The inductor is selected to maintain a specified current ripple range (about 15%- 30%) for the desired switching frequency range. The capacitor is chosen with sufficiently low ESR to maintain output voltage ripple requirement and sustain transient load response capability under extreme transients. However, selection of second-stage LC filter is crucial to approximate that the $v_O \approx v_C$ and retain high control bandwidth in the proposed PA.

The L_2 is designed to have at least 10 times higher impedance than first-stage filter capacitor impedance for current ripple components at switching frequency.

$$Z_{L2} \geq 10\, Z_C \tag{6-1}$$

where $Z_{L2} = j\omega_{fs}L_2$, $Z_C = 1/j\omega_{fs}C$. Thus, from (6.1), design criteria for L_2 is given in (6.2).

$$L_2 \geq \frac{10}{\omega_{fs}^2 C} \tag{6-2}$$

where $\omega_{fs} = 2\pi f_S$. Further, L_2 should have a low DC resistance to minimize the voltage drop across L_2. To maintain a voltage error less than 5%, ESR of L_2 (r_{L2}) should be chosen as per (6.3).

$$r_{L2} \leq 5\% \left(\frac{v_{omin}}{i_{Omax}}\right) \tag{6-3}$$

The dynamic performance of the PA is defined by the response of output voltage (i.e., v_O) and control bandwidth of the v_O is dependant on the second-stage LC filter and control bandwidth of the BC loop. In the proposed PA, v_C is controlled by the σ_{cor}^2 within two switching actions, and it has proven that the closed-loop bandwidth of the σ_{cor}^2-control loop for the synchronous buck converter with a single-stage LC filter is approximately equal to the switching frequency in Section 4.5.2.2. Therefore, the second filter resonance frequency of the two-stage filter should be placed higher than the switching frequency of the converter to minimize its impact on the dynamic performance. The equivalent circuit of the PA for high frequency is shown in Figure 6.4. The second filter resonance frequency is given by (6.4)

$$f_{res} = \frac{1}{2\pi\sqrt{L_2 C_S}} \tag{6-4}$$

where $C_S = \frac{1}{\frac{1}{C}+\frac{1}{C_F}}$.

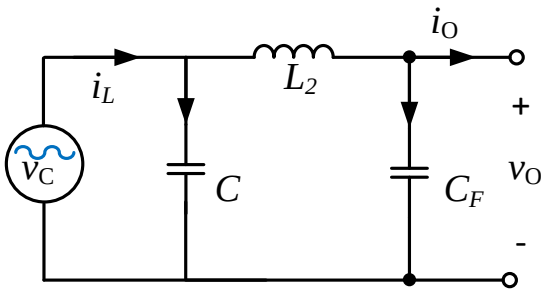


Figure 6.4 High-frequency circuit for calculating second filter resonance.

Considering the above, the C_F is designed in such a way that the second filter resonance frequency to be at least two times higher than f_S, avoiding any interactions with the control loop and minimizing the impact on dynamic performance. From (6.4), design criteria for C_F is given by (6.5) and (6.6).

$$C_S \leq \frac{1}{L_2 \omega_{fs}^2} \tag{6-5}$$

$$C_F = \frac{1}{\frac{1}{C_S} - \frac{1}{C}} \tag{6-6}$$

6.3. DC-DC Converters Modelling in Real Time Simulation

In this section, a switch model for DC-DC converters in real time simulations is introduced, which can be applied to model PV-BES converters in RTSs. Real time simulators employ a fixed time-step solver and compute the state of the modelled power system network at discrete time instances called the simulation time step. Smaller time-steps (< 5 μs) are required to simulate higher frequency components and capture transients in PE converters generated from switching events. Thus, switch modelling has always been a challenge for electro-magnetic Transient (EMT) type real time simulation. Resistor switch-model is the commonly used traditional switch model, in which the ON-state and OFF-state of the switch

are modelled as a small and large resistor, respectively. However, the resistor switch model requires an inversion of the system admittance matrix when switching instant changes resulting in a large computational burden. Alternatively, sub-cycle average models [140]-[142] are used to keep the admittance matrix invariant, thereby avoiding computationally expensive matrix inversion. In sub-cycle averaging, the converter is averaged over simulation time-step (Δt) based on the instantaneous signals to obtain the linear converter model, whereas conventional average techniques average over exactly one switching cycle.

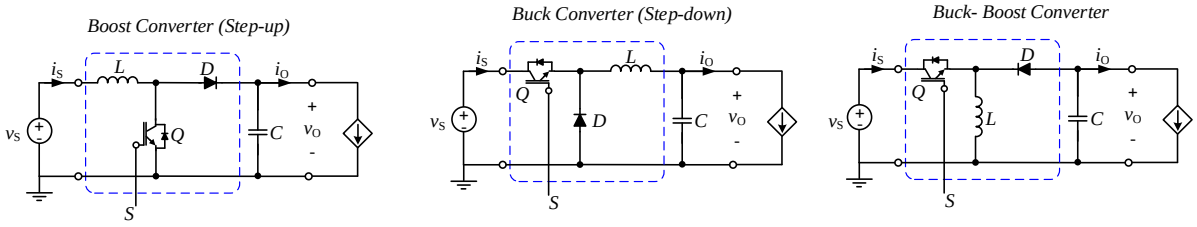


Figure 6.5 Basic types of DC-DC converters.

In this work, a sub-cycle average switch model (SM) based on equivalent state-space equations is employed to implement DC-DC converters in RTS. All basic DC-DC converter types consist of a switching cell with switch, diode and inductor, as highlighted in Figure 6.5. In the proposed model, the main switching cell is replaced using two dependent current sources. Figure 6.6 shows a boost converter with the sub-cycle average model that contains two current sources controlled by i_S and i_O. Reference values for i_S and i_O are determined by discretizing the inductor equation based on the equivalent circuit during switch ON and OFF and considering switching signal (S), as follows.

$$i_S(t) = \frac{\Delta t}{2L}[v_S(t) - \bar{S}(t)v_O(t)] + \left[\frac{\Delta t}{2L}\left(v_S(t-\Delta t) - \bar{S}(t)v_O(t-\Delta t)\right) + i_s(t-\Delta t)\right] \quad (6\text{-}7)$$

$$i_O(t) = S(t)i_S(t) \quad (6\text{-}8)$$

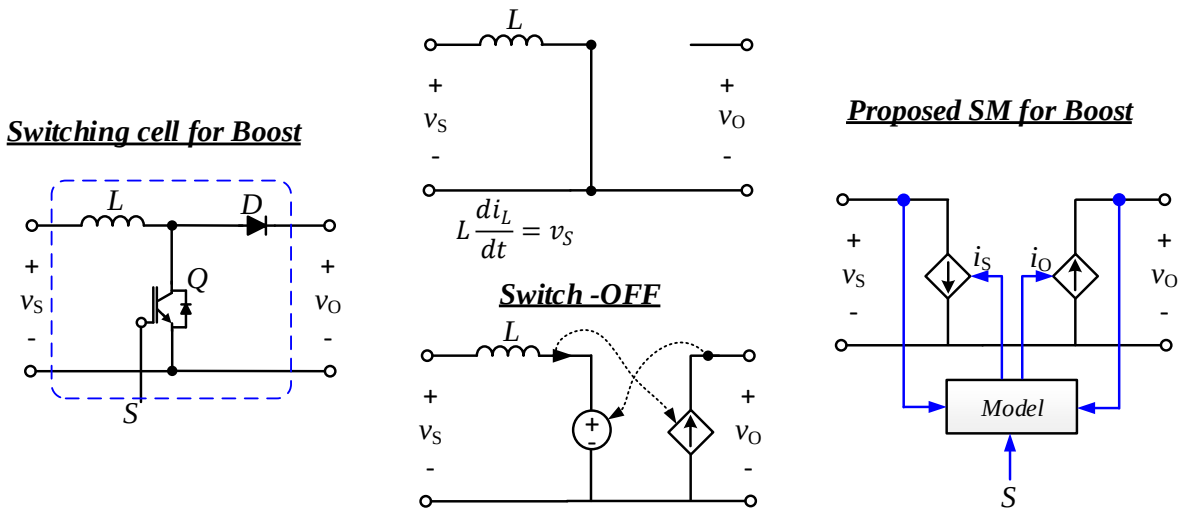


Figure 6.6 Boost converter with sub-cycle average switch model.

Since the inductor and diode current is calculated within the time step, the switch-model can ensure the current flow direction. Thus, this model is valid for both CCM and DCM. Similarly, this model can be extended to buck and buck-boost topologies, as shown in Figure 6.7 and Figure 6.8, respectively.

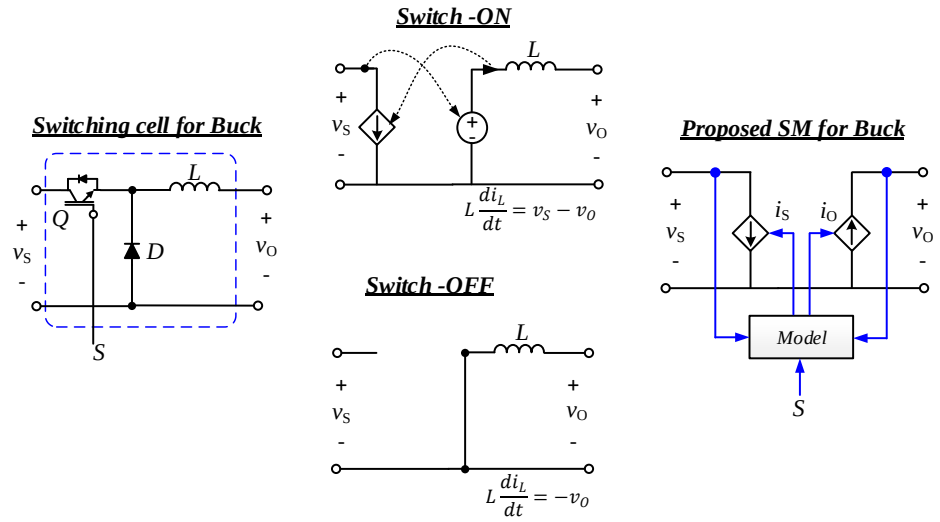


Figure 6.7 Buck converter with sub-cycle average switch model.

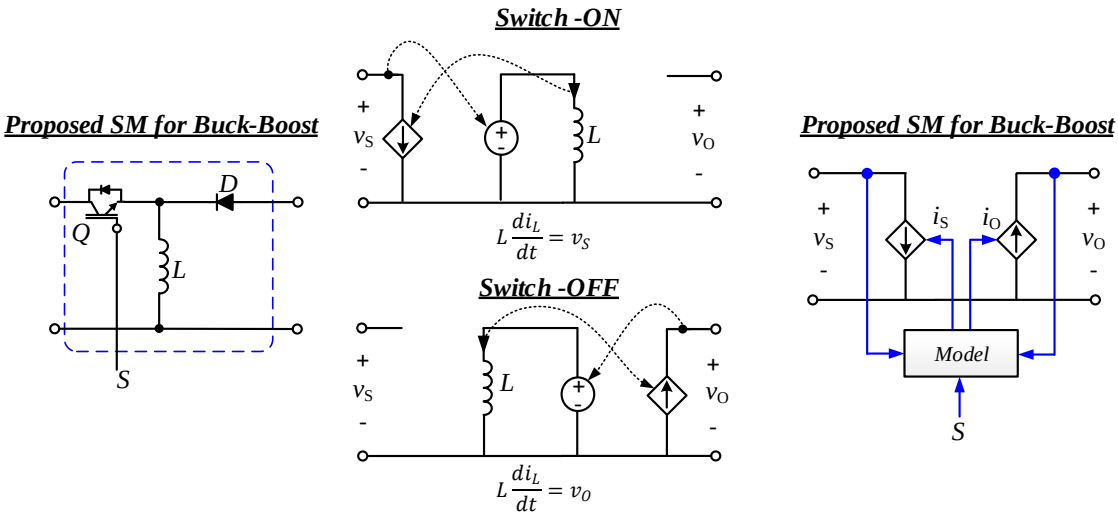


Figure 6.8 Buck-boost converter with sub-cycle average switch model.

Main limitation of the sub-cycle SM is that there will be one time-step delay in v_O when calculating the reference current i_S during real time EMT simulation. However, if the simulation time step is maintained much shorter than the switching cycle of the converter, this error can be kept to a minimum. Moreover, limited resolution in the switching signal may lead to an error in the duty ratio when the switching event is detected in the simulation time-step (T_{RT}) after the event is occurred [142]. Considering one on-transition and one off-transition over the period of switching signal (T_{sw}), the upper limit for the absolute error of duty ratio (E_{duty}) is given by (6.8)

$$E_{duty} < \frac{T_{RT}}{T_{sw}} \tag{6-9}$$

Based on (6.9), the error increases for larger T_{disc} and shorter T_{sw}. And the error of duty ratio can be directly translated to calculate error in state variables. As mentioned in RT simulations, the time step is much shorter than the switching cycle of the converter. Hence this switch model can be applied for modelling DC-DC converters to represent dynamics with reasonable accuracy.

6.3.1 Sub-cycle Average Switch-model Validation

This section discusses simulation results of a boost converter in steady-state and transients using sub-cycle average SM and resistor SM implemented in RSCAD™ sub-step simulation environment. Both are compared with a reference solution obtained with PLECS using a resistor SM. Developed PLECS case is shown in Figure 6.9, and it used the fixed time-step solver. The simulation time step is taken as 1µs for all three scenarios, which is the resolution time for S. The boost converter is operated in open-loop control with a switching frequency of 20 kHz and a duty ratio, d=0.5.

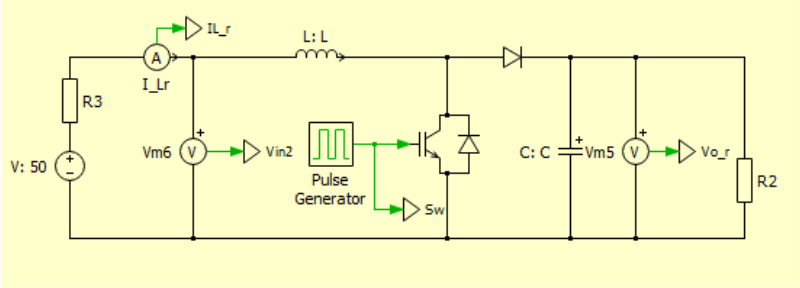


Figure 6.9 Boost converter with resistor SM in PLECS with L= 3.5mH, C=100µF, R_L= 10 Ω for CCM.

Figure 6.10 shows the simulation results of the boost converter in CCM under all three scenarios. It shows that the sub-cycle average SM solution closely matches the RSCAD resistor SM solution and PLCES reference solution for the inductor current and capacitor voltage, and the mean error % is less than 0.33%. Since the switching signal is sampled at the same resolution in all three scenarios, the error is primarily due to one time-step delay in v_C for calculating reference current i_S. In Figure 6.11, transient results of the boost converter for a sudden change in input voltage are shown with both proposed sub-cycle average SM and

RSCAD resistor SM. These results prove that sub-cycle average SM can be applied to model DC-DC in EMT-type real time simulations.

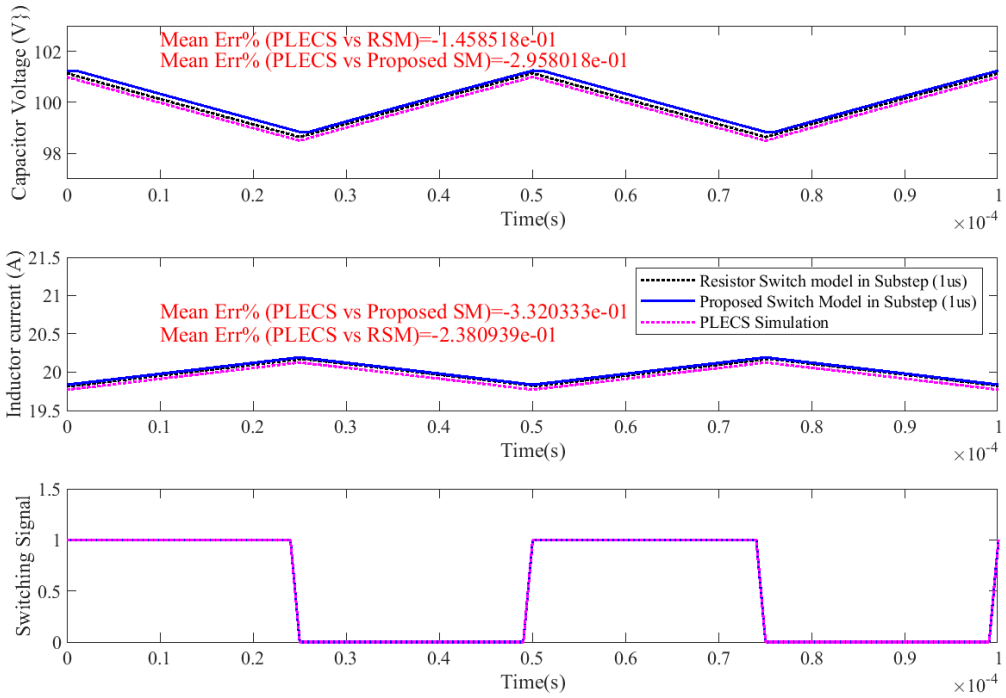


Figure 6.10 Simulation results of the boost converter in CCM.

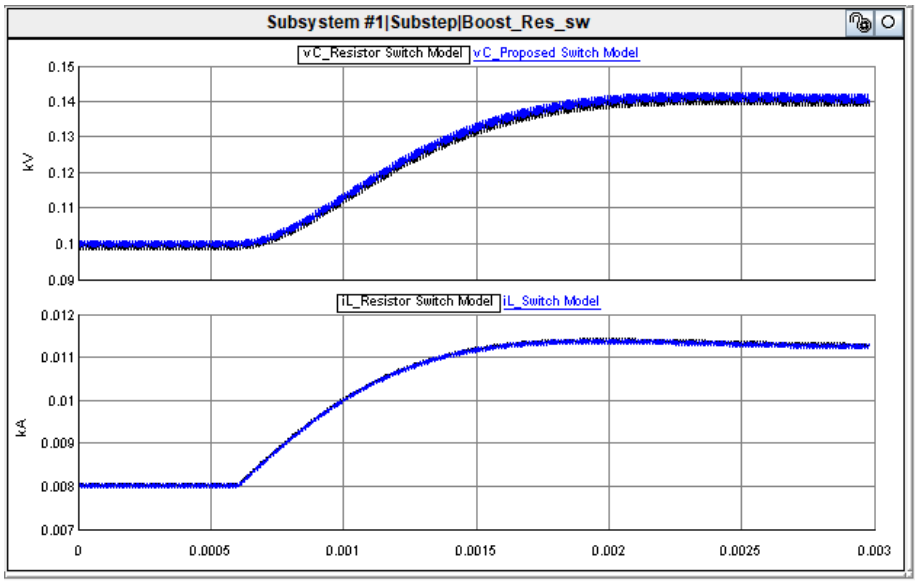


Figure 6.11 Simulation results of the boost converter for a transient in input voltage.

6.4. Experimental Evaluation

The PHIL testbed described in Section 6.2 has been implemented for experimentally evaluating an in-house developed and implemented PV-BES power unit interfacing to a DC MG. Figure 6.12 shows the experimental test setup of the PHIL testbed. The RTDS™ simulator is used as the RTS for developing RT models of PV array and scalable DC MG with PV-BES systems. Two synchronous buck converter prototypes are implemented to realize switch-mode PAs for PVE and DC GE, and the control scheme of the PA is implemented using a Texas TI™ TMS320F28377S microcontroller. The design parameters of the PHIL-based DC grid emulator are listed in Table 5-1, and the design parameters of the PHIL-based PVE are the same as given in Chapter 5.

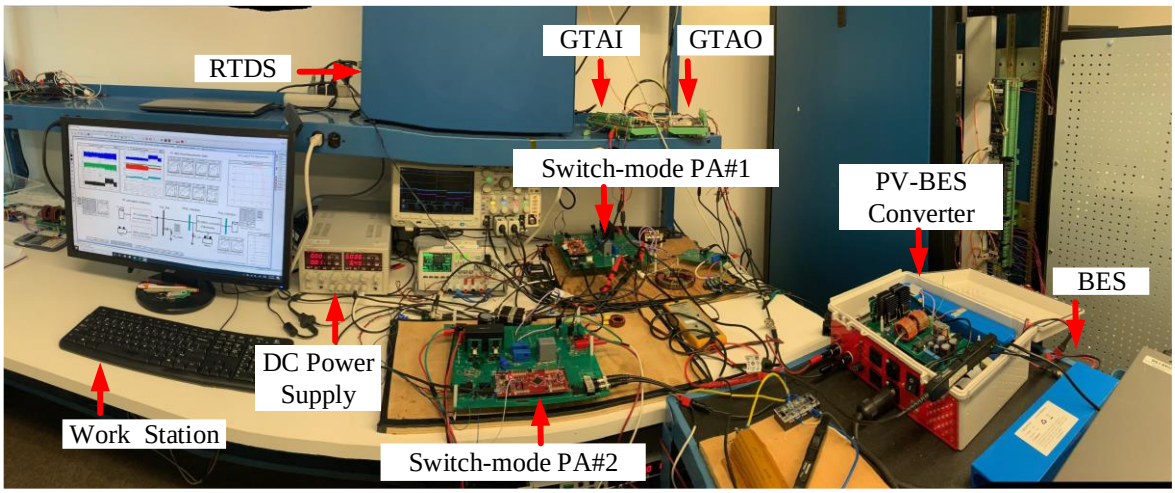


Figure 6.12 PHIL testbed in the laboratory.

The DC MG with one PV-BESS power unit simulation is developed in RSCAD™, as shown in Figure 6.13. Fully decentralized PV-BES coordination control method presented in [138] is implemented to regulate the PV-BESS power unit. In BES converter control, an outer droop controller is employed to regulate the DC bus voltage for compensating power mismatch and achieve BES SOC self-convergence without communication, while the inner control loop

regulates the battery current. The PV converter controller employs a cascade control scheme to operate under MPPT control when load dominant mode and droop control when generation dominant mode (i.e., when BESS is fully charged). The outer V-I droop control loop maintains the local DC link voltage with a higher voltage reference value than BES droop control. Thus mode transition from MPPT to droop is seamless. The implemented PV converter and BES converter control schemes are shown in Figure 6.14. The real time simulation in RSCAD is solved with a time step of 15 µs.

Table 6-1 Key Design Parameters of the PHIL-based DC GE.

Parameter	Value	Parameter	Value	Parameter	Value
v_S	80 V	Δ	1 V	T_{S1}	20 µs
L	1 mH	L_2	0.5 mH	f_s	9.5- 14.1 kHz
C	4.7 µF	C_F	0.1 µF	PI (for k_D)	k_p=0.2 k_i=400
f_C	100 Hz	G_{AAF}	1	f_{aaf}	10.1 kHz

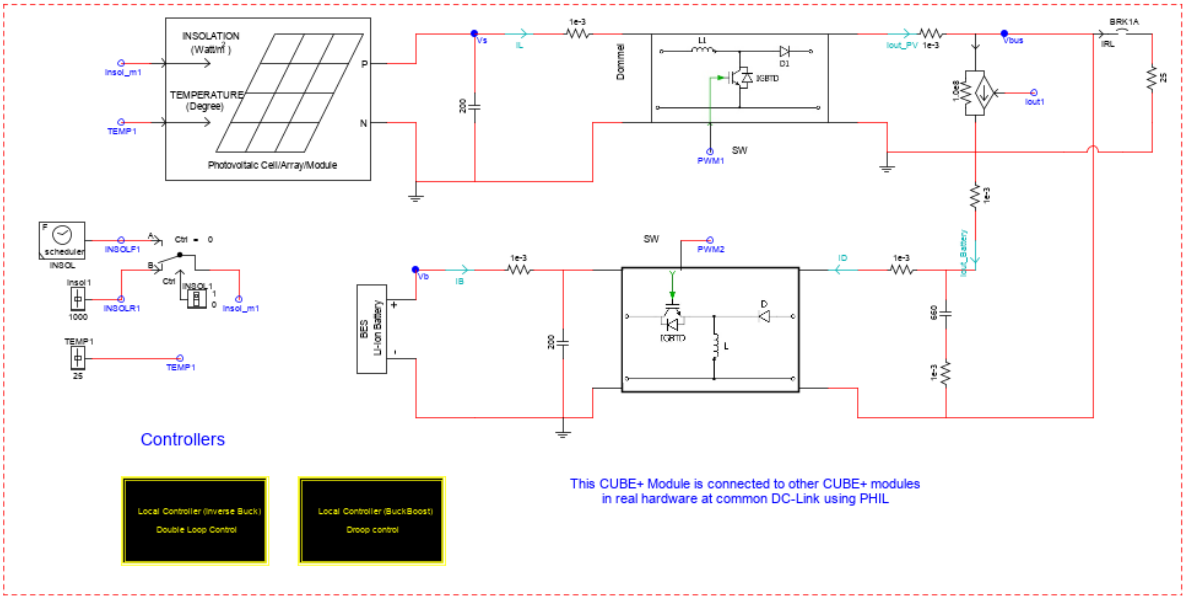


Figure 6.13 Implementation of fully decentralized DC MG with PV-BESS in RSCAD

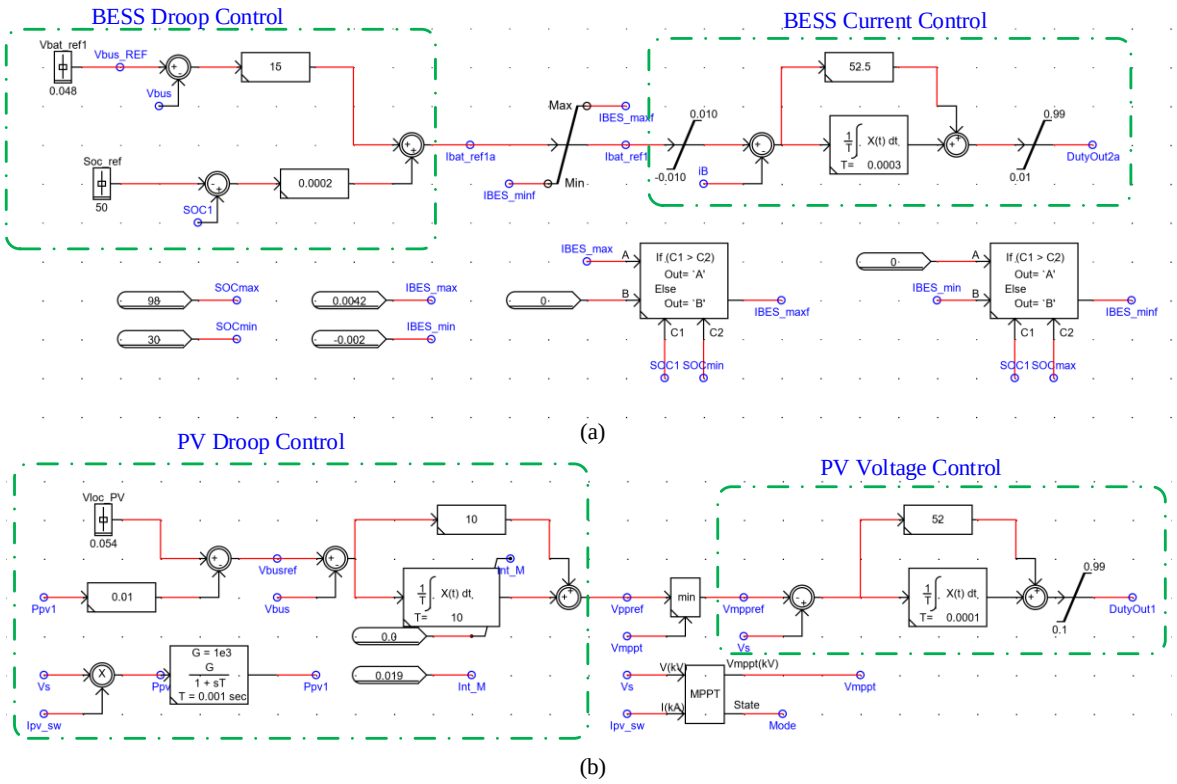


Figure 6.14 Implementation of control scheme (a) PV converter (b) BES converter in RSCAD.

The dynamic response of the VM PA stage is evaluated separately by applying a load step change, and results are shown in Figure 6.15. The PA dynamic response time was found to be 148 µs, proving its fast voltage regulation.

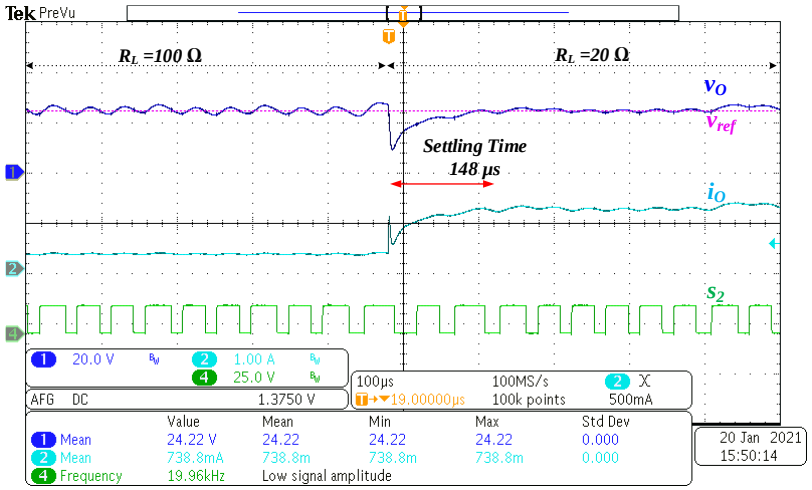


Figure 6.15 VM PA transient response for a load step change from 100Ω to 20Ω.

Figure 6.16 shows the operation of a standalone PV-BES PU with PHIL-based PVE, showing PV MPPT control and BES droop control. In t_0-t_1, BES maintains dc bus voltage(v_{bus}) with droop control and PVE is off. At, t_1, PVE is connected and the PV converter regulates its input power at MPP with MPPT control; the BES converter is changed to charging mode, absorbing the excess power, and the dc bus is still under BES droop control. At t_2, solar irradiance is reduced, and the PV converter is still under MPPT control with reduced power. At t_3, PVE is disconnected, and BES changed back to discharging mode. In this way, the proposed PHIL-based PVE is successfully used to evaluate the performance of the standalone PV-BES control schemes.

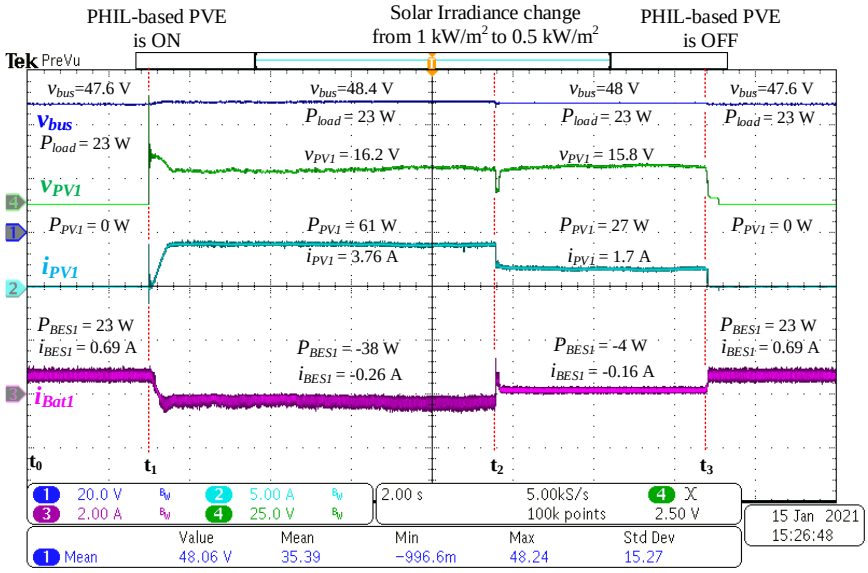
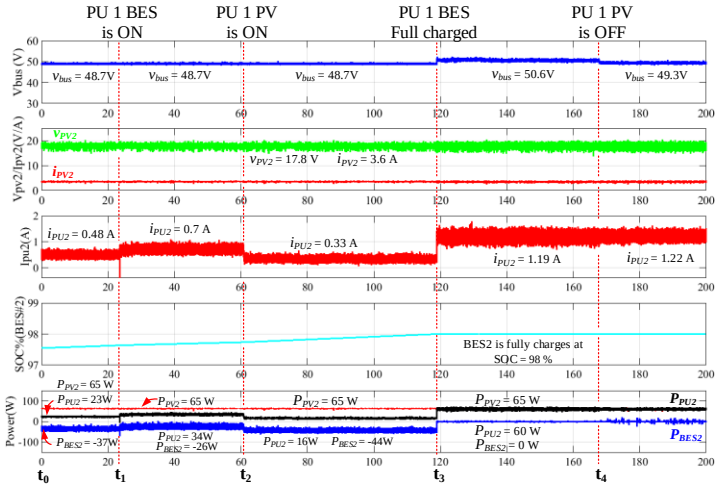


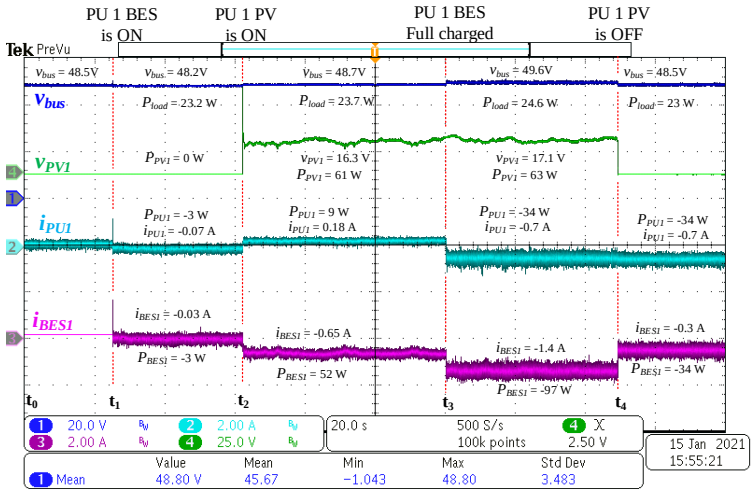
Figure 6.16 Experimental waveforms of a standalone PV-BES PU with PHIL-based PVE.

A DC MG system with two PV-BES PUs is tested by using the proposed PHIL platform. One PU (PU#2) is modelled in RSCAD™, and it is interfaced to a real PU (PU#1) via a proposed switch-mode PA. The designed PHIL-based PVE is used to source the PV converter of PU#1. Figure 6.17 shows the operation of MG with two PV-BES PUs under generation-dominating mode. During t_0-t_1, only PU#2 is operated to supply the load of 100Ω. As shown

in Figure 6.17 (a), the PV converter of PU#2 operates at MPP, and BES of PU#2 maintains v_{bus} with droop control. At t_1, BES of PU#1 is switched ON; now both BESs maintains the v_{bus}. At t_2, PV of PU#1 is connected to evalaue the system with both PUs. Power is shared by both units, and respective BESs absorb the excessive PV power. At t_3, PU#2 BES is fully charged; PU#2 BES absorbs all the surplus power with droop control; PV converters are kept at MPPT control. These results suggest that the developed PHIL platform can be successfully applied to evaluate DC MG systems.



(a)



(b)

Figure 6.17 PHIL test results of the DC MG showing power-sharing (a) RT software measurement of PV-BES PU#2 (b) Experimental waveforms of PV-BES PU#2.

6.5. Summary

In this chapter, a PHIL testbed composed of PHIL-based PV emulator and PHIL-based DC grid emulator is developed targeting DC Microgrids with PV-BES system analysis. The PHIL-based PVE design presented in Chapter 5 is directly adapted to emulate the PV array. A VM PA based on a synchronous buck converter with a two-stage LC filter is introduced for DC grid emulation. Like the VM PA in Chapter 3, σ_{cor}^2 is applied through the first-stage LC filter to control capacitor voltage, and additionally, a second-stage LC filter is placed to decouple high-frequency current ripple components led by the load converter. It is proven that the impact of the second-stage LC filter on accuracy and dynamic response can be kept minimum through analysis and experiments. Thus, the second-stage LC filter allows for applying a non-linear large-signal-based controller to regulate the PA fast dynamically without affecting its performance due to the switching-load converter.

Further, in this chapter, a sub-cycle average switch model is utilized to model DC-DC converters in real time EMT type simulation. It reduces the computational burden on RTS by keeping the admittance matrix invariant, and model accuracy is verified via PLECS simulations. This technique is used to model a DC MG with one PV-BES converter PU in RTDS™ and performed PHIL simulations to evaluate a physical PV-BES converter prototype. Results showed that the developed PHIL testbed could be successfully applied to assess a physical PV-BES converter and their control schemes with enhanced flexibility.

Chapter 7

Power-HIL Testbed for Evaluating Grid-Connected EV Chargers

The work described in this chapter was submitted for publication as the following paper: I. D. G. Jayawardana, C. N. M. Ho and Y. Zhang, " A Comprehensive Study and Validation of a Power-HIL Testbed for Evaluating Grid-Connected EV Chargers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, (Early Access).

This chapter presents a PHIL testbed composed of PHIL-based battery emulator and grid emulator for testing grid-connected EV chargers. Idea of this work is mainly to study the application of PHIL simulations for battery emulation with a switch-mode PA. Also, mathematical frameworks are developed to analyze the stability and predict the accuracy of both PHIL-based emulators. The BE in this work considers a switch-mode PA with a linear PI controller. Thus, design strategies of this linear controller are also discussed in the context of cascaded DC-DC configuration. The performance of a commercial Level 1 EV charger is presented with the validated PHIL tested.

7.1. Introduction

Electric vehicles have become increasingly popular and mature in terms of their technology, and accordingly, their rapid growth is expected to persist in the coming decades [143]. Subsequently, EV charging is on the verge of becoming a commodity. Among residential communities, the use of on-board EV chargers has become a preferable choice simply for its ability to connect to a single-phase residential plug with functions of grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operations [144], [145]. Extensive addition of EV chargers into the LV grid may create PQ issues such as voltage sag and harmonics, and alternatively, EV chargers could also be affected by PQ issues originated elsewhere [146]. These scenarios have urged to conduct studies for evaluating PQ issues in the LV grid as well as to develop advanced EV chargers.

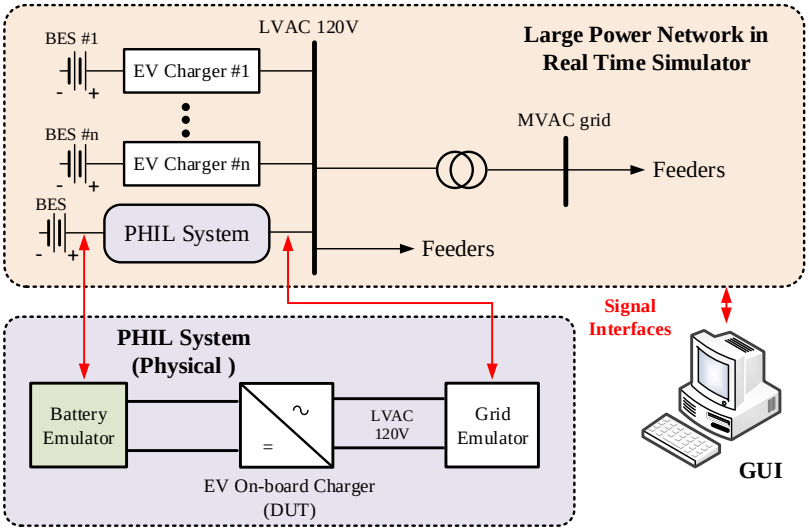


Figure 7.1 The PHIL test configuration for grid-connected EV chargers.

To achieve such studies, a PHIL testbed configuration composed of two PHIL simulations is presented in this chapter, for evaluating grid-connected EV chargers, as shown in Figure 7.1. Unlike conventional PHIL grid integration testbeds based on standalone source

emulators both battery source and grid network are emulated through PHIL simulations. The PHIL-based battery emulator provides a platform for conducting burn-in tests with enhanced flexibility for different commercial battery arrays compared to standalone BEs, and it takes advantage from the grid integration testbed since RTS is already in place [118], [147], [148]. Although the implementation of PHIL simulation of battery is well known [117], [118], the detailed modelling and analysis of the PHIL-based BE have not been sufficiently addressed in the literature. The presence of an EV charger at the output of the PHIL-based BE composed of a switch-mode power interface creates a cascaded dc-dc configuration. Thus, a detailed model of the cascaded DC-DC system is necessary to design the classical linear controller of the source-side converter to avoid the negative impedance instability [104], [105]. Further, as highlighted in Chapter 6, the stability and accuracy studies of a switch-mode power amplifier interface for PHIL simulations are mostly developed with small signal models derived considering resistive loads [36], [37], [62], [108]. Thus, possible stability degradation issues at the common dc link between the PHIL-based emulator and the EV charger have not been assessed in PHIL testbed applications. This chapter aims to address these deficiencies by deriving a comprehensive small signal model of the PHIL-based BE, including the virtual battery model, power interface and impedance characteristics of the DUT for analysing stability and accuracy of the PHIL simulation. Cascaded system model composed of a switch-mode PA and DUT is derived to design linear control parameters of the PA.

Additionally, this chapter provides a systematic approach for designing and implementation of a PHIL testbed with two PHIL simulations for testing grid-connected EV chargers and conduct related system studies. The chapter is organized as follows. Section 7.2 describes the comprehensive system architecture of the PHIL testbed, including the

implementation of power interfaces for both DC and AC sides of the EV charger. Detailed small signal model of the PHIL-based battery emulator with interconnecting EV charger is presented in Section 7.3 for stability and accuracy analysis. Also, mathematical framework of the PHIL-based GE is summarized to determine stability and accuracy analysis. Section 7.4 shows the experimental performance of the PHIL testbed with a commercial EV charger to demonstrate the application of the platform. In Section 7.4, a case study is conducted by integrating the PHIL simulation of EV charger with a weak grid scenario simulated in RTS.

7.2. Configuration of the PHIL Testbed

Two PHIL simulations form the PHIL testbed for evaluating EV chargers to emulate both the DC side battery behavior and the AC side LV grid behavior, as shown in Figure 7.2. The RT simulations are implemented using the RTS from RTDS Technologies Inc. and the RSCAD™ user interface. The following subsections discuss the critical elements of the PHIL platform in detail.

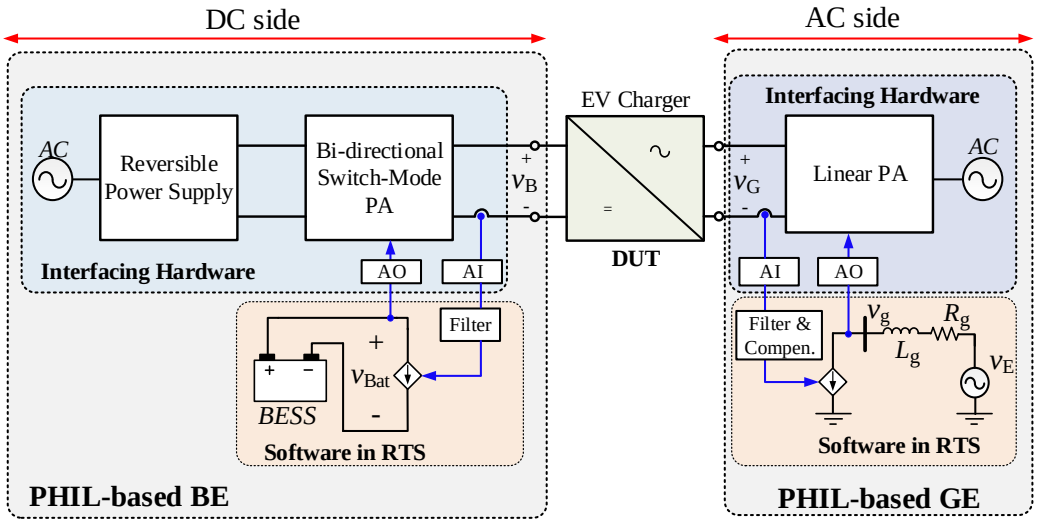


Figure 7.2 Detailed block diagram of the PHIL test platform for EV chargers.

7.2.1 PHIL-based Battery Emulator

As shown in Figure 7.2, the PHIL-based BE is composed of a battery model in RTS, signal interface and bi-directional switch-mode PA, which is implemented using the voltage-type ITM IA. A voltage-type ITM IA is employed since voltage-mode (VM) control is used in the PA. Figure 7.3 illustrates how an original BESS simulation is extended to its corresponding PHIL-based simulation via voltage-type ITM IA. The circuit is decoupled at the load converter (i.e., EV charger) connecting point as marked in Figure 7.3 (a), and a power interface is added to complete the circuit with a DUT, as shown in Figure 7.3. The BESS voltage from the real time battery model in RTS (v_{Bat}) is interfaced to the EV charger output terminals through DAC and switch-mode PA and current measurement of the EV charger (i_B) is sent back to the RTS to complete the virtual battery model simulation. In this way, PA operates to imitate the charge/discharge characteristics of a given battery model and real power is exchanged between PA and EV charger. A digital low-pass filter is used to eliminate the noise associated with the current measurement, and its parameters should be selected to offer an acceptable trade-off between noise reduction, improve stability and system response.

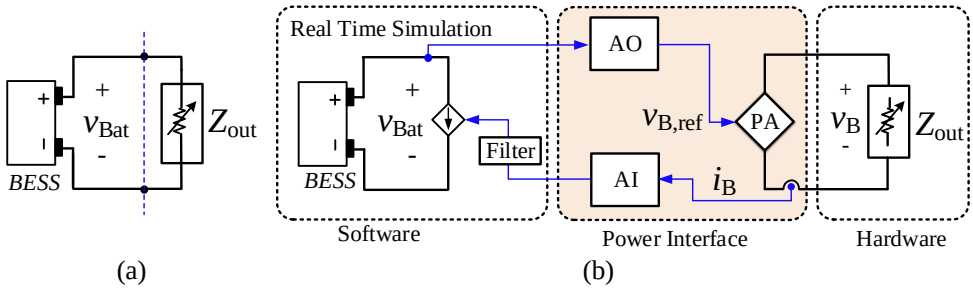


Figure 7.3 BESS (a) with real time simulation, and (b) with PHILS.

7.2.1.1 Switch-mode PA

The BE should be able to emulate the non-linear characteristics of batteries together with its power flow. Therefore, switch-mode PA of the BE is generally operated in VM control with a possibility of bidirectional power flow to ensure both charging/discharging operations. In this work, the PA is realized using a bidirectional DC-DC synchronous buck converter with a reversible dc power supply and a digital controller. The detailed architecture of the VM PA is shown in Figure 7.4. A DC power source with a parallel resistor (R_d) is used for implementing reversible power supply (i.e., front end converter of the BE). The R_d is designed considering the maximum power during the charging operation (P_{cmax}) (i.e.,$R_d < v_S^2/P_{cmax}$). Note that, design and control of active front end converter for the BE is not the scope of this thesis. As shown in Figure 7.4, a linear PI control with PWM scheme is used to regulate the output voltage of PA (v_B) at given voltage reference (v_{Bref}). The PI control parameters can be designed using cascaded system model as presented in Section 7.3.1.1.

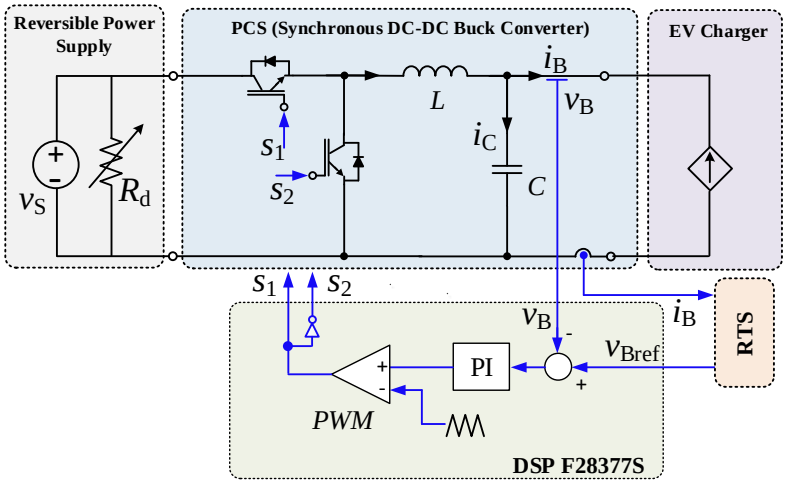


Figure 7.4 Architecture of the bi-directional switch-mode PA for BE.

7.2.1.2 Battery Model and Simulation in RTS

The battery model is an integral part of the BE accuracy. In this work, Min/Rincon Mora et al. model [13] is adapted to represent the Li-ion battery dynamics in RT simulation. Li-ion batteries are chosen for emulation in this work as they are commonly used in EVs for their high energy density, long lifetimes, and lightweights. Figure 7.5 shows the equivalent electrical circuit of the Min/Rincon Mora et al. model consisting of a series resistor and two RC parallel networks for representing the battery's electrical behavior, including short-term and long-term transient response [13].v_{OC} is the open-circuit voltage; R_S is responsible for the instantaneous voltage drop of step response; R_{t_S} and C_{t_S} account for short-term transients, while R_{t_L} and C_{t_L} are responsible for long-term transients. However, this model has not considered the thermal dependency of the circuit parameters and the battery lifetime modelling aspects.

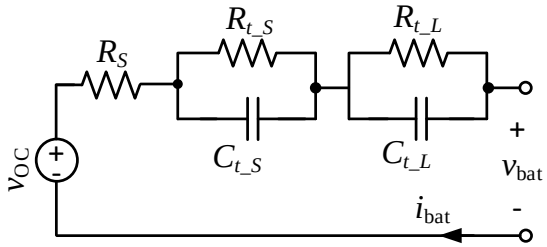


Figure 7.5 The electrical equivalent circuit of the Min/Rincon Mora model [41.5].

In [41.5], all the model parameters have been derived as a function of the SOC based on experimental results of a commercial Li-ion polymer battery (TCL-PL-383562). Table 7-1 presents the technical specification for TCL-PL-383562 battery. As a function of SOC, expressions for model parameters are given by (7.1)-(7.6).

$$v_{OC}(soc) = -1.031e^{-35\,SOC} + 3.685 + 0.2156\,SOC - 0.1178\,SOC^2 + 0.3201\,SOC^3 \quad (7\text{-}1)$$

$$R_S(soc) = 0.1562e^{-24.37\,SOC} + 0.07446 \quad (7\text{-}2)$$

$$R_{t\_S}(soc) = 0.3208e^{-29.14\,SOC} + 0.04669 \tag{7-3}$$

$$C_{t\_S}(soc) = -752.9e^{-13.51\,SOC} + 703.6 \tag{7-4}$$

$$R_{t\_L}(soc) = 6.603e^{-155.2\,SOC} + 0.04984 \tag{7-5}$$

$$C_{t\_L}(soc) = -6056e^{-27.12\,SOC} + 4475 \tag{7-6}$$

In RT simulation, SOC can be calculated at each simulation time step (T_{RT}) as given below,

$$SOC[k] = SOC_{init} + \left(\frac{T_{RT}}{Q}\frac{i_{bat}[k] + i_{bat}[k-1]}{2}\right) \tag{7-7}$$

where Q is the battery capacity, SOC_{init} is the initial SOC level. The V-I characteristics equation of the Li-ion battery is derived by applying Kirchhoff's voltage law for the equivalent circuit model shown in Figure 7.5, and it is given in the Laplace domain by,

$$v_{bat}(s) = v_{OC}(s) - Z_b(s)i_{bat}(s) \tag{7-8}$$

where,
$$Z_b(s) = R_S + \frac{R_{t\_S}}{1 + R_{t\_S}\,C_{t\_S}\,s} + \frac{R_{t\_L}}{1 + R_{t\_L}\,C_{t\_L}\,s} \tag{7-9}$$

A single Li-ion battery model can be scaled up to determine the BESS model composed of series-and-parallel connected batteries (N_s, N_p) by modifying v_{OC} and RC network by considering N_s and current injection through the circuit with N_p. This model can be implemented in any RT circuit simulator that accepts embedded programming RTS can complete the calculation within the specified time step in real-time.

Table 7-1 Technical Specifications for TCL-PL-383562 Li-ion Battery

Parameter	Value	Parameter	Value
Nominal Capacity	0.85 Ah	Max. Charge current	1275mA (1.5C)
Nominal Voltage	3.7 V	Charged Voltage	4.2 V

7.2.2 PHIL-based Grid Emulator

The schematic of PHIL-based GE with all measurement points at hardware and software runtime environment is shown in Figure 7.2. Like the PHIL-based BE, it is developed by decoupling the grid network simulation using the voltage-type ITM IA. The AC bus voltage from the simulated power system network in RTS is interfaced to the EV charger input side through a DAC and PA. The current measurement is sent back to the RTS to compute the state of the modelled power system network. In the PHIL-based GE, voltage amplification is realized by using a commercial linear PA that should be able to source real and reactive power. Further, a digital low-pass filter is used to eliminate the noise associated with the current measurement. This would improve the stability margin of the PHIL system due to the presence of a left half-plane pole [37], [44]. However, the filter would introduce an additional magnitude attenuation and phase lag in the current feedback signal. Therefore, as suggested in [37], a compensator is added to minimize the magnitude attenuation at the desired frequency range (15 Hz to 300 Hz) and compensate for phase lag associated with the filter. Another important factor for PHIL-based GE is the level of details of the AC network simulated in RTS. A simple grid equivalent network that consists of an AC voltage source in series with grid impedance, as shown in Figure 7.2, can be considered when evaluating EV charger performance. For system-level studies, a single-phase equivalent representation of a benchmark LV network can be implemented in RTS, and it should be interfaced to the EV charger through the PA.

7.3. Modelling and Analysis of the PHIL Testbed

7.3.1 PHIL-based Battery Emulator

This section aims to conduct small-signal stability and accuracy analysis of the PHIL-based BE loaded by an EV charger:

1. The cascaded DC-DC system model composed of switch-mode PA and EV charger is presented to design the linear controller of the PA and to evaluate the cascaded system's stability.
2. The detailed model of the PHIL-based BE is presented to investigate overall system stability and predict PHIL simulation accuracy.

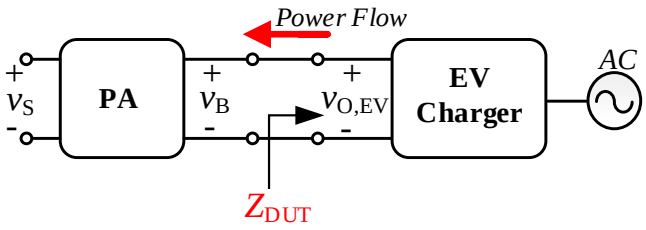


Figure 7.6 Cascaded DC-DC configuration between the PA and EV charger.

7.3.1.1 Cascaded system model for control design

Figure 7.6 shows the cascaded DC-DC configuration in which the PA is considered as the source converter and the EV charger as the load converter. In the cascaded system model, the load converter can be represented by its closed-loop output/input impedance (Z_{DUT}) (i.e., seen by the PA) depending on whether the load converter is operated in charging/discharging mode, respectively. Thus, the small signal relation between v_B and i_B is governed by (7.10).

$$\tilde{v}_B(s) = Z_{DUT}(s)\tilde{i}_B(s) \tag{7-10}$$

The switch-mode PA consists of a synchronous buck converter shown in Figure 7.4, which is modelled with filter inductor (L), filter capacitor (C), ESR of the capacitor (r_C) and ESR of the inductor (r_L). The parasitic resistances are considered to improve the accuracy of modelling. The converter is controlled via PWM duty cycle command, d. The canonical circuit model in Figure 7.7 can be developed to represent small-signal dynamics and transfer functions of the synchronous buck converter in CCM [133].

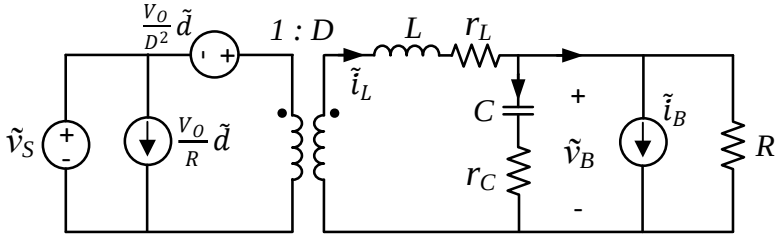


Figure 7.7 Canonical circuit model of the synchronous buck converter with parasitic resistances.

By using the single converter canonical model and conventional linear circuit analysis techniques, the cascaded DC-DC system model can be mathematically represented through TFs, as shown in Figure 7.8. In the cascaded system, the dynamics of $\tilde{i}_B$ and $\tilde{v}_B$ depend on the load converter thus, open-loop TFs should be derived by neglecting the resistive load (R) since it has been replaced by the Z_{DUT}. Derived open-loop TF of the buck converter with parasitic resistances required for this study are as follows:

$$G_{VD}(s) = \frac{\tilde{v}_B(s)}{\tilde{d}(s)}\Big|_{\tilde{v}_S,\hat{i}_B=0} = \frac{V_S}{\left(1+\frac{r_C}{R}\right)LCs^2+\left(\frac{L}{R}+r_LC\left(1+\frac{r_C}{R}\right)+r_CC\right)s+\left(1+\frac{r_L}{R}\right)} \tag{7-11}$$

$$Z_{OUT}(s) = \frac{\tilde{v}_B(s)}{-\hat{i}_B(s)}\Big|_{\tilde{v}_S,\tilde{d}=0} = \frac{(Ls+r_L)(1+r_CCs)}{\left(1+\frac{r_C}{R}\right)LCs^2+\left(\frac{L}{R}+r_LC\left(1+\frac{r_C}{R}\right)+r_CC\right)s+\left(1+\frac{r_L}{R}\right)} \tag{7-12}$$

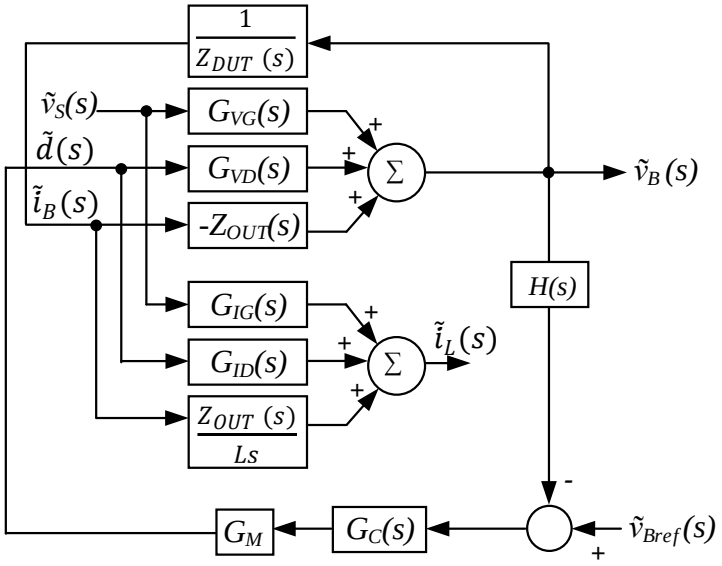


Figure 7.8 Mathematical representation of the cascaded DC-DC system.

Impedance of DUT during charge/discharge

When the PA emulates charging operation (G2V), Z_{DUT} will be the closed-loop output impedance of the load converter (Z_{outCL}). While in discharging (V2G), Z_{DUT} will be the closed-loop input impedance of the load converter (Z_{inCL}) since power flow is reversed. Therefore, developing a generic mathematical model for Z_{DUT} in designing the PA controller is challenging and may not be accurate. Further, unlike the PA, the topology and control strategy of EV charger is unknown, and it is proprietary for manufactures. Thus, TF of the Z_{DUT} is unknown. However, the closed-loop input impedance of a converter is proven to exhibit negative impedance characteristics when its output is tightly regulated [50]. Thus, in literature, Z_{inCL} of complex PE-based converter is often approximated as a constant power load (CPL) [150]. By linearizing the CPL at an operating point (V_B, P), the Z_{DUT} in discharging mode can be modeled as below,

$$Z_{DUT_{CPL}}(s) = Z_{inCL} = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = -\frac{V_B^2}{P} \tag{7-13}$$

where $P = V_B I_B$.

In charging mode, Z_{outCL} is measured experimentally using an impedance analyzer (Bode 100) and used to estimate the TF of Z_{DUT}. This way provides an experimental approach for deriving a case-specific model of the Z_{DUT}. Figure 7.9 shows the measured Z_{outCL} characteristics of a commercial EV charger (delta-Q IC1200) when it is operated in both constant current (CC) and constant voltage (CV) charging modes considering a BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array (10Ah/25.9 V).

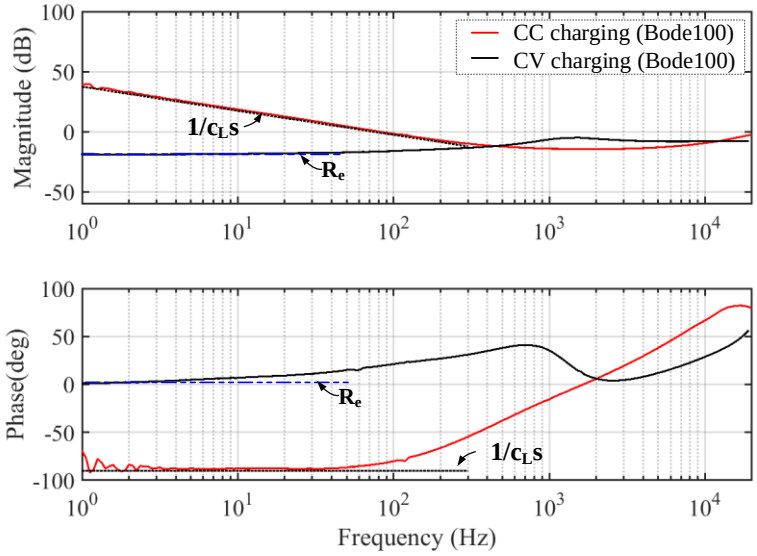


Figure 7.9 Output impedance measurement of an EV charger in CC (v_B=26 V, i_B=5 A) and CV v_B=28 V, i_B=2.2 A) mode.

It is seen that the EV charger resembles a capacitive load ($1/c_L s$) when it is operating in CC mode and a resistive load (R_e) in CV mode over the frequency of interest, in this case, the low-frequency range (DC- 300 Hz). Hence, Z_{DUT} can be represented analytically as a positive impedance depending on the EV charger's operating mode. To improve the accuracy of Z_{DUT},

a software tool like MATLAB^{TM} can also be used to estimate the TF of Z_{DUT} and estimated TFs for two scenarios in Figure 7.9 are given below,

$$Z_{DUT_{cc}}(s) = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = \frac{-1.9s^2 - 2.1*10^4 s - 1.9*10^8}{s^2 - 3.5*10^5 s - 3.6*10^5} \tag{7-14}$$

$$Z_{DUT_{cv}}(s) = \frac{\tilde{v}_B(s)}{\tilde{i}_B(s)} = \frac{-1.9s^2 - 2.1*10^4 s - 1.9*10^8}{s^2 - 3.5*10^5 s - 3.6*10^5} \tag{7-15}$$

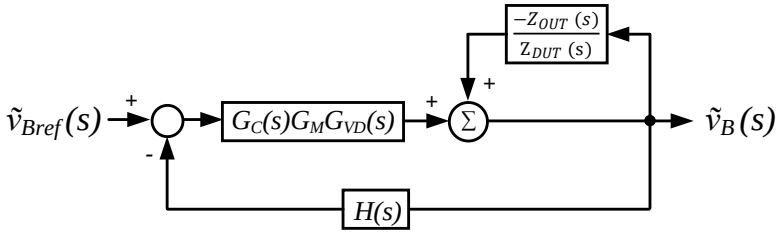


Figure 7.10 Control block diagram for PI control design.

Controller design of the switch-mode PA

To study the voltage control loop dynamics, Figure 7.8 can be simplified to Figure 7.10 by neglecting the perturbations in input voltage (v_S). Thus, the compensated open-loop TF of the PA can be derived using Figure 7.10 and is given by (7.16).

$$G_{PA\_OL}(s) = G_C(s)G_M H(s)G_{VD}(s)\frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}} \tag{7-16}$$

where G_M is the PWM scheme gain, and $H(s)$ is the voltage sensor feedback gain. Since Z_{DUT} is known, (7.16) can be used to design the PI controller (i.e., $G_C(s)$) using any frequency response methods. Typically, the control to output TF ($\hat{v}_B(s)/\hat{d}(s)$) of an ideal buck converter with CPLs has two poles in the right half-plane due to the negative incremental impedance [151]. However, with practical parasitic resistances, the uncompensated plant becomes a stable system, as shown in Figure 7.11. Thus, classical linear PI controllers can be used to control the BE with CPL too. The system parameters considered for analysis are listed in Table 7-2.

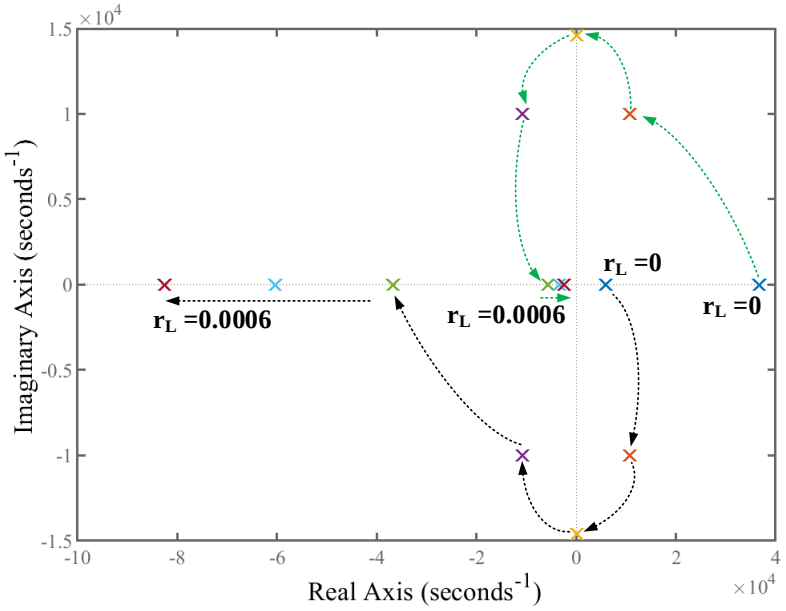
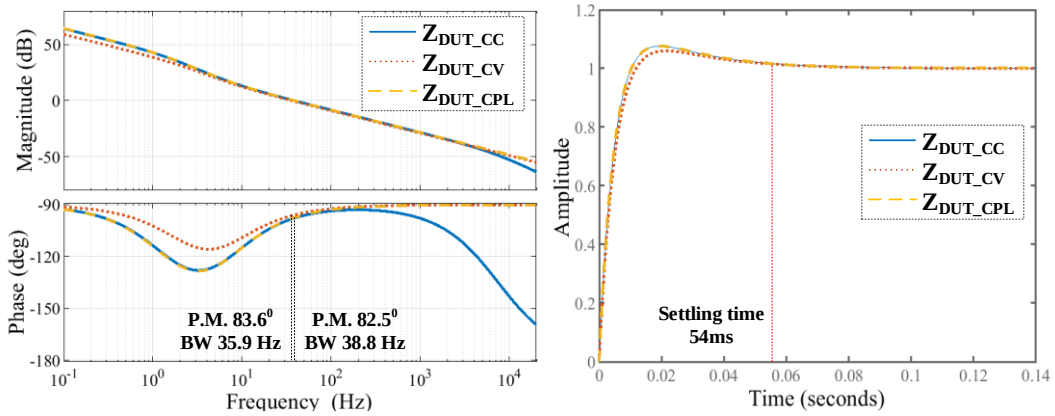


Figure 7.11 Pole movement of a buck converter loaded by a CPL with increasing parasitic resistance (from r_L= 0, , r_C= 0 to r_L= 0.0006, , r_C= 0).

Figure 7.12 (a) shows the bode plot of the $G_{PA\_OL}(s)$ with the designed PI controller indicating that the system is stable with enough phase margin (P.M.) under different load impedance scenarios. The step response of the PA is shown in Figure 7.12 (b) under the same conditions.



(a) (b)

Figure 7.12 The PA response under different load impedances (a) frequency response of the $T_{OL}(s)$. (b) step repsonse.

Table 7-2 Key Parameters of the Switch-mode PA Analysis

Parameter	Value	Parameter	Value	Parameter	Value
v_S	60 V	f_S	20 kHz	r_L, r_C	0.1 Ω, 0.001 Ω
L	3.7 V	k_P, k_I	0.4, 16.8	c_p, R_e	21.3 mF, 0.12 Ω
C	4.7 µF	$H(s)$	1	V_B	25 V
R_d	10 Ω	G_M	1	P	125 W

7.3.1.2 PHIL System Model for Battery Emulation

The PHIL system model is derived by considering the linearized BESS model, model of each device in the power interface, impedance characteristics of the EV charger, and the sampling effect of digital computation in both RTS and microcontroller of the PA. Unlike other PHIL configurations, the linear model of the BESS is a key element in developing the equivalent control block of the system. The linear model of Li-ion battery is developed by differentiating (7.8) at a linearization point (V_{OC}, SOC, V_{bat}, I_{bat}) as given below,

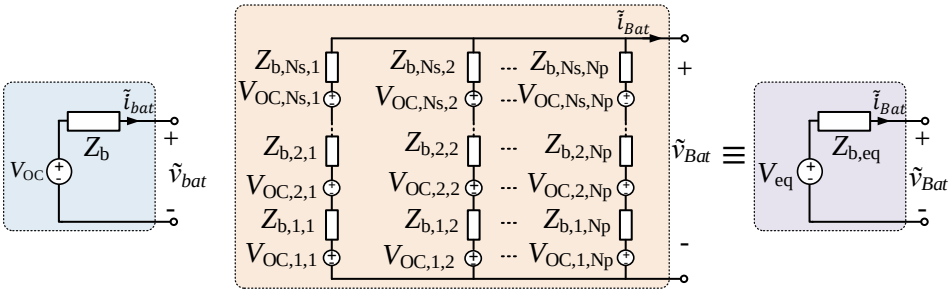
$$\tilde{v}_{bat}(s) = V_{OC} - Z_b(s)\tilde{i}_{bat}(s) \tag{7-17}$$

It is assumed that the variation of SOC of the battery for a small change in $i_{bat}(\tilde{i}_{bat})$ is negligible. Thus, (7.17) is derived by neglecting SOC perturbations (i.e., $\widetilde{SOC}$=0) in the small signal analysis. The linearized battery model given in (7.17) can be represented by an equivalent circuit, as shown in Figure 7.13 (a). Based on (7.17), the BESS model that consists of a $N_s \times N_p$ battery array can be lumped to into an equivalent circuit, as shown in Figure 7.13 where, $V_{eq} = N_s V_{OC}$, $Z_{b,eq} = N_S Z_{b,1} // N_S Z_{b,2} // \cdots // N_S Z_{b,N_p}$ and, $i_{bat} = N_p i_b$. Therefore, linearized model of the BESS is described by,

$$\tilde{v}_{Bat}(s) = V_{eq} - Z_{b,eq}(s)\tilde{i}_{Bat}(s) \tag{7-18}$$

Thus, the small signal relation between v_{Bat} and i_{Bat} is given by (7.19).

$$\tilde{v}_{Bat}(s) = -Z_{b,eq}(s)\tilde{i}_{Bat}(s) \tag{7-19}$$



(a) (b) (c)

Figure 7.13 The equivalent circuit of the linearised (a) battery model (b) BESS model (c) lumped BESS model.

To validate the small signal model of BESS, the frequency response of $Z_{b,eq}(s)$ is compared with AC sweep results obtained experimentally through a Gain/Phase analyzer (Bode100). Figure 7.14 shows the detailed test configuration for impedance measurement along with the indication of measured variables. A small signal perturbation is introduced in the i_{bat} via a gain-phase analyzer and, the voltage and current of the BESS inside RTS are monitored (i.e., v_{bat} and i_{bat}).

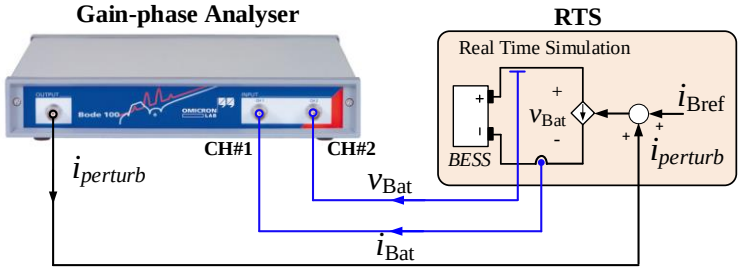


Figure 7.14 Connection scheme for Bode100 for frequency response evaluation of battery model.

The frequency response obtained from Bode100 is super-imposed with the frequency response of the mathematical BESS model in Figure 7.15 for two BESS arrays (7x12 and 21x12). It is observed that the experimental results are closely matching with the response of the mathematical model. Thus, this validates the developed BESS model.

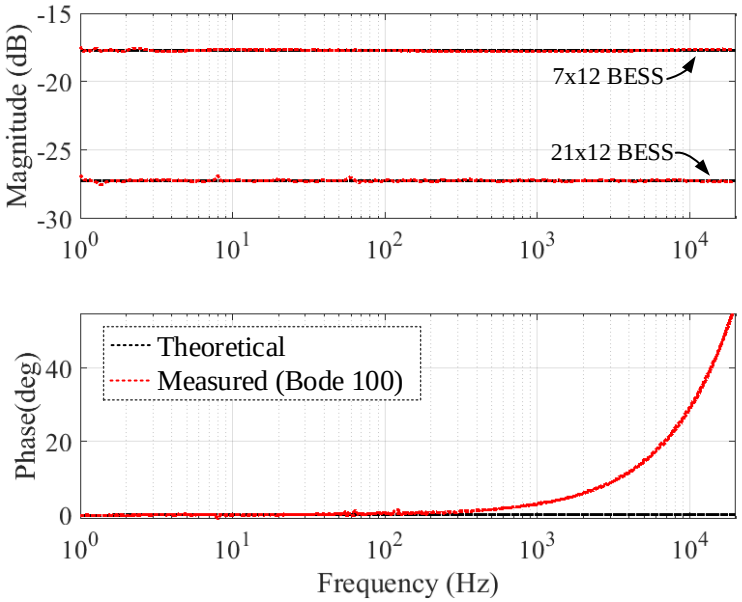


Figure 7.15 Comparison of the input impedance of the BESS array when i_{Bat}= -5A and SOC=50% for model validation.

By considering the linear model of BESS and other mentioned elements, the PHIL-based BE in Figure 7.2 can be represented in a control block diagram, as shown in Figure 7.16. The open-loop TF of the system can be derived using the block diagram in Figure 7.16. and, it is given by,

$$T_{OL\_BE}(s) = \frac{Z_{b,eq}}{Z_{DUT}} G_{AO}(s) G_{vv}(s) G_{AI}(s) G_{fil}(s) \tag{7-20}$$

where $G_{vv}(s)$ is the TF of switch-mode PA, $G_{AI}(s)$ is the model of ADC card in RTS, $G_{\mathrm{AO}}(s)$ is the model of DAC card in RTS, $G_{fil}(s)$ is the TF of the current measurement

feedback filter. The delay time of the sensor is much shorter compared to other latencies. Hence, it is neglected from the analysis. Each power interface device can be modelled with its respective TFs and time delays. The $G_{vv}(s)$ is derived by considering both the voltage control loop of the buck converter and the sampling and latency effect of the v_{Bref} by the microcontroller.

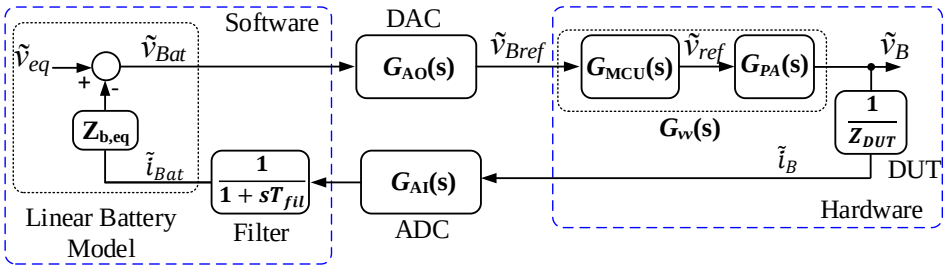


Figure 7.16 Block diagram of the PHIL-based BE via voltage-type ITM.

From (7.16), the closed-loop TF of voltage-mode buck converter ($G_{PA}(s)$) can be derived, and the sampling effect of v_{Bref} in the microcontroller is modelled as a continuous zero-order-hold (ZOH) with an additional delay function and, it is given by,

$$G_{MCU}(s) = \frac{\tilde{v}_{ref}(s)}{\tilde{v}_{Bref}(s)} = \frac{\left(1-e^{-sT_{MCU}}\right)}{sT_{MCU}} e^{-sT_{PA}} \tag{7-21}$$

where T_{MCU} is the sampling period for i_{Oref} in the microcontroller and T_{PA} represents the input-to-output signal latency of PA. The complete model of switch-mode PA is given by,

$$G_{vv}(s) = \frac{\tilde{v}_B(s)}{\tilde{v}_{Bref}(s)} = G_{PA}(s)G_{MCU}(s) \tag{7-22}$$

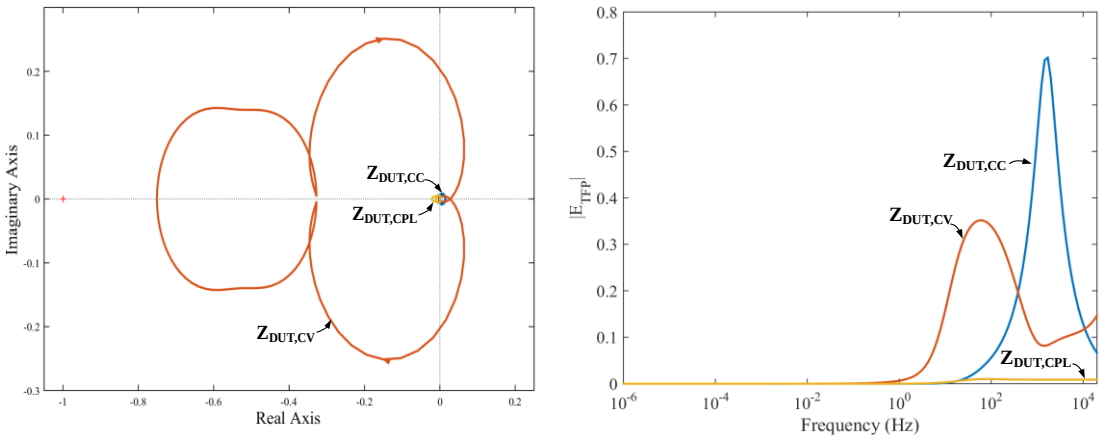
$$G_{PA}(s) = \frac{\tilde{v}_B(s)}{\tilde{v}_{ref}(s)} = \frac{G_C(s)G_M G_{VD}(s)\frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}}}{1+G_C(s)G_M G_{VD}(s)\frac{1}{1+\frac{Z_{OUT}(s)}{Z_{DUT}(s)}}H(s)} \tag{7-23}$$

The TFs for other interface devices (i.e., $G_{AI}(s)$, $G_{AO}(s)$ and $G_{fil}(s)$) are same as in section 5.3.3. Total latency of the loop (T_{total}) is given by,

$$T_{total} = T_{PA} + T_{RT} + T_{AO} + T_{AI} \tag{7-24}$$

7.3.1.3 Investigating Stability of the PHIL-based BE

This work applies Nyquist plots to determine the stability of a defined PHIL-based BE configuration. The stability analysis is done considering a commercial EV charger (delta-Q IC1200) system at the output. The PHIL-based BE intended to emulate BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array (10Ah / 25.9 V). All the parameters of PHIL-based BE are summarized in Table 7-3. The Nyquist stability test results for the designed PHIL system under different Z_{DUT} are shown in Figure 7.17 (a), which indicates that the system has less stability margin with $Z_{DUT_{CV}}$. The stability of voltage-type ITM is proven to be unstable when the ratio $Z_{b,eq}/Z_{DUT}$ is ≥ 1 [37], [38]. From (7.13), Figure 7.9 and, Figure 7.15 show that the $Z_{b,eq}/Z_{DUT_{CV}}$ ratio is close to 1 (0.9328 being the actual value) and, $Z_{b,eq}/Z_{DUT}$ ratios for $Z_{DUT_{CC}}$ and $Z_{DUT_{CPL}}$ are much lower than 1 over the frequency of interest. Thus, designed PHIL-based BE has a higher stability margin for $Z_{DUT_{CC}}$ and $Z_{DUT_{CPL}}$ and has less influence either from the SOC level or the interface parameters to the stability. In summary, the developed mathematical framework can be adopted to ensure a stable operation of the PHIL-based BE with EV charger given that all the interface parameters and, Z_{DUT} are known.



(a) (b)

Figure 7.17 PHIL-based BE (a) stability test results under different Z_{DUT}. (b) TFP error function of v_B over frequency domain.

Table 7-3 Parameters of the PHIL-based BE Interface

Parameter	Value	Parameter	Value	Parameter	Value
T_{RT}	20 µs	T_{AO}	9.2 µs	G_{AAF}	1
T_{AI}	7.2 µs	f_C	100 Hz	f_{aaf}	10.1 kHz
T_{MCU}	50 µs	T_{PA}	40 µs	T_{total}	76.4 µs
Specification of the Emulated Li-ion Battery Array					
Capacity	10 Ah	N_Sx N_P	7x12	*Target Voltage*	4.2V x 7 = 29.4 V

7.3.1.4 Accuracy Evaluation of the PHIL-based BE

The accuracy of the designed PHIL simulation for BESS is evaluated based on the method proposed by W. Ren et al. [62], in which the PHIL simulation error function is derived considering the perturbations caused by non-idealities of the interface as well as external noises. It defines the perturbation comes from non-idealities of the power interface as the transfer function perturbation (TFP). In this work, simulation error comes due to the TFP has

only been investigated while noise perturbations are considered to be negligible. The error function due to TFP (E_{TFP}) is given as,

$$E_{TFP} = \left| W_0 \frac{G_{LP}(s)\Delta G_{int}(s)}{(1+G_{LP}(s)(1+\Delta G_{int}(s)))} \right| \tag{7-25}$$

$$\Delta G_{int}(s) = G_{int}(s) - 1 \tag{7-26}$$

where G_{LP} (s) is the open-loop TF of the original circuit (i.e., without interface perturbation), $G_{int}(s)$ is the TF of the non-ideal interface and, W_0 is a weighting function for adding different accuracy levels at different frequencies [62]. From Figure 7.16, G_{LP} and $G_{int}(s)$ for PHIL-based BE can be derived and, those are given by (7.27) and (7.28).

$$G_{LP}(s) = Z_{b,eq}/Z_{DUT} \tag{7-27}$$

$$G_{int}(s) = G_{vv}(s)G_{AO}(s)G_{AI}(s)G_{fil}(s) \tag{7-28}$$

The E_{TFP} for v_B can be determined by solving (7.25). The theoretical error results of v_B over the frequency domain under different load conditions are plotted in Figure 7.17 (b). The error is equally treated by taking W_0=1. It is seen that the normalized error below 10 Hz is < 0.05, which means that the PHIL interface would not have a significant impact on accuracy by applying PHIL simulation for battery emulation.

7.3.2 PHIL-based Grid Emulator

Similar analysis as in PHIL-based BE can be applied for the PHIL-based GE to evaluate stability and accuracy. The open-loop TF of the PHIL-based GE can be derived from the control block diagram shown in Figure 7.18.

$$T_{OL\_BE}(s) = \frac{Z_S}{Z_{DUT_{AC}}} G_{AO}(s)G_{LPA}(s)G_{AI}(s)G_{CP}(s) \tag{7-29}$$

where Z_S is equivalent grid inductance, Z_{DUTac} is AC side input impedance of the EV charger, $G_{LPA}(s)$ is the linear PA TF, $G_{CP}(s)$ is the TF of the filter and compensator.

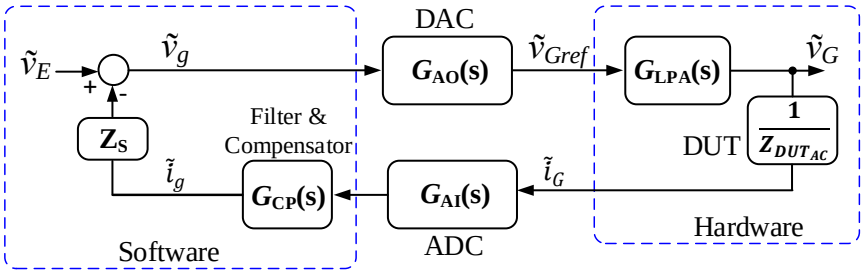


Figure 7.18 Block diagram of the PHIL-based GE via voltage-type ITM.

Expressions for Z_S, $G_{LPA}(s)$ and $G_{CP}(s)$ are given below.

$$Z_S = R_g + sL_g \tag{7-30}$$

$$Z_S = R_g + sL_g \tag{7-31}$$

$$G_{CP}(s) = \frac{sT_{cp}}{1\_sT_{cp}} \frac{1}{1+sT_{fil1}} \tag{7-32}$$

where T_b is the latency of linear PA, T_a is the cut-off of linear PA, T_{cp} is the time constant of the lead compensator and, T_{fil} is filter cut-off of the current feedback signal. The Z_{DUTac} is obtained experimentally via frequency response measurements and used that for estimating the TF of Z_{DUTac}. For e.g., the experimental results obtained from the impedance analyzer (Bode100) and estimated Z_{DUTac} are plotted in Figure 7.19, in which the estimated TF of Z_{DUTac} closely agrees with experimental results. Thus, this procedure can be followed to obtain Z_{DUTac} for a certain operating point to conduct stability and accuracy evaluations.

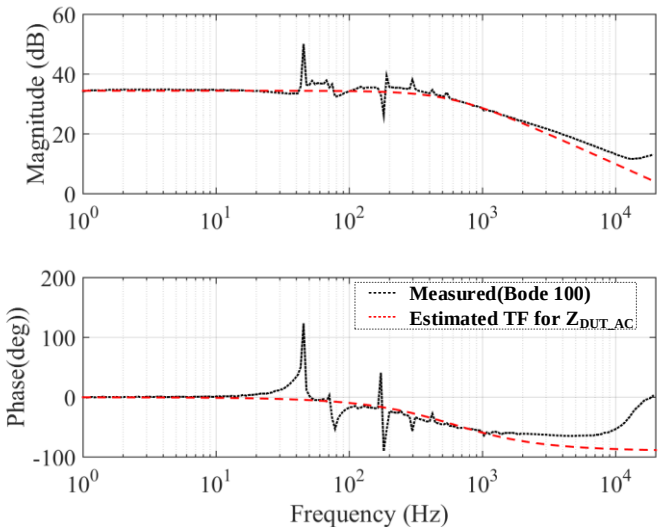


Figure 7.19 Input impedance (Z_{DUT_AC}) results from impedance analyser when EV charger in CC (v_B=26 V, i_B=5 A).

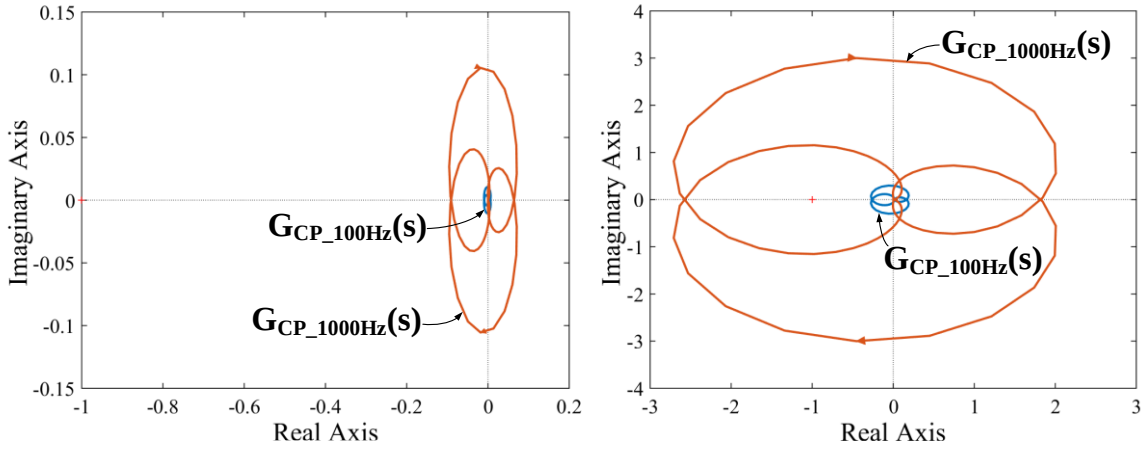
Nyquist stability test results are presented in Figure 7.20 for the designed PHIL-based GE under different Z_S/Z_{DUTac} ratios and different $G_{CP}(s)$. The PHIL simulation is stable for both Z_S with $G_{CP\_100Hz}(s)$ and becomes unstable for R_g =0.193 Ω, L_g =2.5 mH with $G_{CP\_100Hz}(s)$. It confirms that both $G_{CP}(s)$ and Z_s have a significant influence on the stability of the system. The design parameters of the PHIL simulation are tabulated in Table IV. Further, the accuracy of the PHIL interface is evaluated based on the procedure explained in Section IV-A-d. The E_{TFP} of v_G is determined by deriving the G_{LP} and $G_{int}(s)$ of PHIL-based GE from Figure 7.18. Expression for G_{LP} and $G_{int}(s)$ are given by,

$$G_{LP}(s) = Z_S/Z_{DUT_{AC}} \tag{7-33}$$

$$G_{int}(s) = G_{LPA}(s)G_{AO}(s)G_{AI}(s)G_{CP}(s) \tag{7-34}$$

The predicted error results of v_B over the frequency domain under different conditions are plotted in Figure 7.21. Noticed that normalized error is insignificant (<0.02) for frequencies

below 1 kHz when Z_S is low (R_g= 0.001 Ω, L_g=88 µH) under both compensators. However, E_{TFP} becomes significant for higher Z_S, as presented in Figure 7.21.



(a) (b)

Figure 7.20 Nyquist stability test results of the PHIL-based GE under different $G_{CP}(s)$ (a) with R_g=0.001 Ω, Lg=88 µH. (b) R_g=0.193 Ω, Lg=2.5 mH.

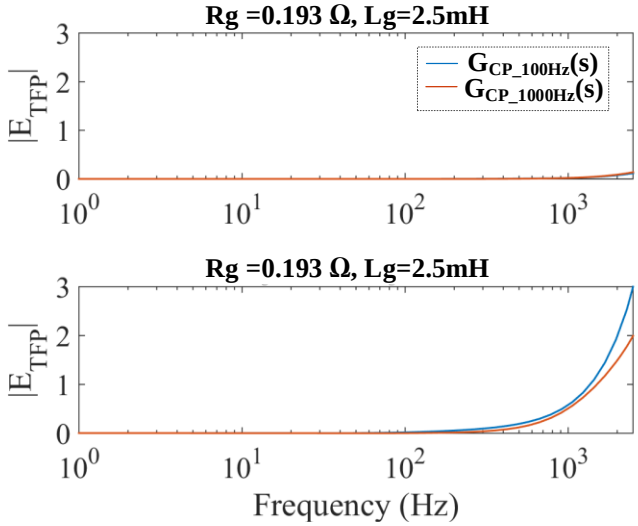


Figure 7.21 Predicted variation of TFP error function of v_G over frequency under different compensators and grid equivalent resistances.

Table 7-4 Parameters of the PHIL-based GE Interface

Parameter	Value	Parameter	Value
$G_{CP\_100Hz}(s)$: T_{fil1}, T_{cp}	1.59 ms, 10.6 ms	T_a, T_b	0.4 µs, 6 µs
$G_{CP\_1000Hz}(s)$: T_{fil1}, T_{cp}	0.159 ms, 26.5 ms	Z_{DUT_AC}	$1.9 * 10^5/(s + 3737)$

7.4. Experimental Validation

The PHIL testbed described in Sections 7.2 and 7.3 has been implemented for evaluating a commercial EV charger (delta-Q IC1200) experimentally. Figure 7.22 shows the experimental test setup of the PHIL testbed.

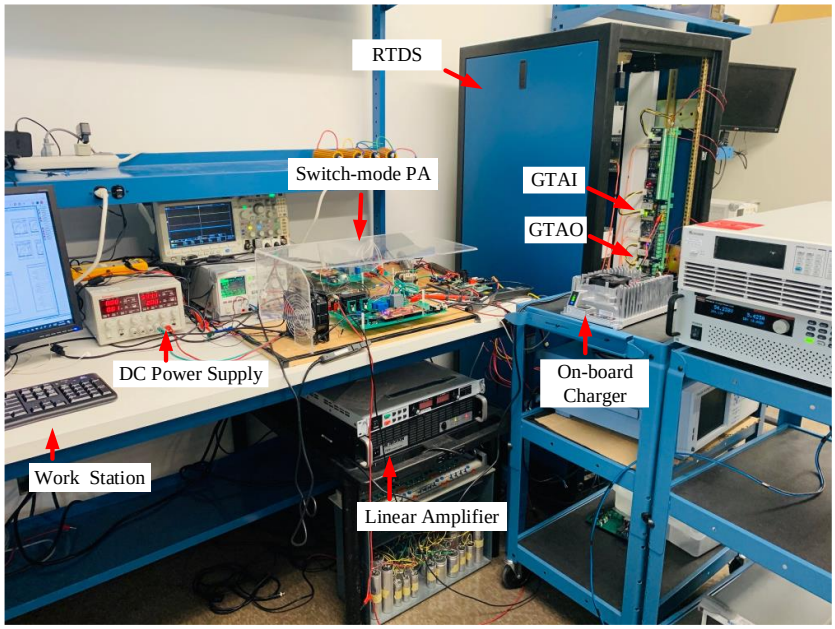


Figure 7.22 The PHIL Testbed.

The RTDS© simulator is used as the RTS for developing the RT models of BESS and LV network, and its RSCAD user interface is installed in the workstation for interfacing with the RTDS simulator. A 300W bi-directional DC-DC buck converter prototype with the voltage controller is implemented to emulate the battery array, and Table 7-2 shows its design

parameters. Throughout the chapter, PHIL-based BE is designed to emulate a BESS consists of a 7x12 TCL-PL-383562 Li-ion battery array and PHIL interface parameters, including the battery array details, are listed in Table 7-3. A 900W AE TECHRON linear PA is used to emulate the grid, and interface parameters of the PHIL-based GE is given in Table 7-4.

7.4.1 PHIL-based BE Validation

The performance of the designed PHIL-based BE is evaluated separately before connecting them with the EV charger. Figure 7.23 shows the experimental results of the PHIL-based BE during the charge operation from 25 % SOC to 100% SOC with i_B= - 8A. This experiment is performed by connecting a controlled current source (Chroma 62050H-600S) at the output of the BE.

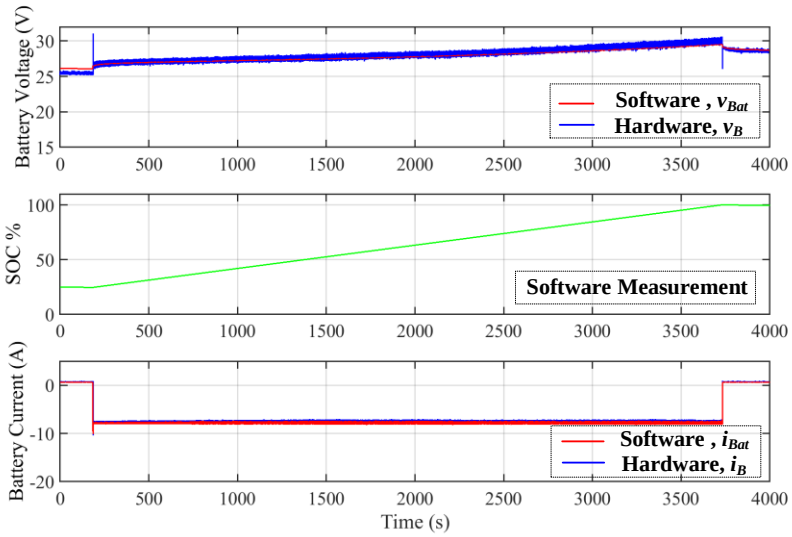


Figure 7.23 Experiment results of the PHIL-based BE during charging operation.

The RT battery model has already been validated with real batteries in [13]. Thus, accuracy of the PHIL-based BE can be evaluated by comparing it with RT simulation results. As illustrated in Figure 7.23, the output waveforms of switch-mode PA (i.e., v_B, i_B) are closely

following the simulated waveforms (i.e., v_{Bat}, i_{Bat}). The error between them is quantified by calculating the mean percentage error (MPE) and found out that it is 1 % for v_B and 0.8 % for i_B. This validates that the PHIL-based BE is accurately emulate the RT battery model. Further, discharge operation of the PHIL-based BE is tested by connecting a DC electronic load (KEITHLEY 2380-500-30) and results obtained are plotted in Figure 7.24. Noticed a minor steady-state error in v_B under no-load conditions as voltage controller is designed by only considering the CCM operation. Except for that, the results are in good agreement with the RT battery model. Figure 7.25 presents the stable operation of PHIL-based BE for a pulse discharge test with a 1C-discharging rate (10.2A), and it verifies that the switch-mode PA can track the battery model transients accurately.

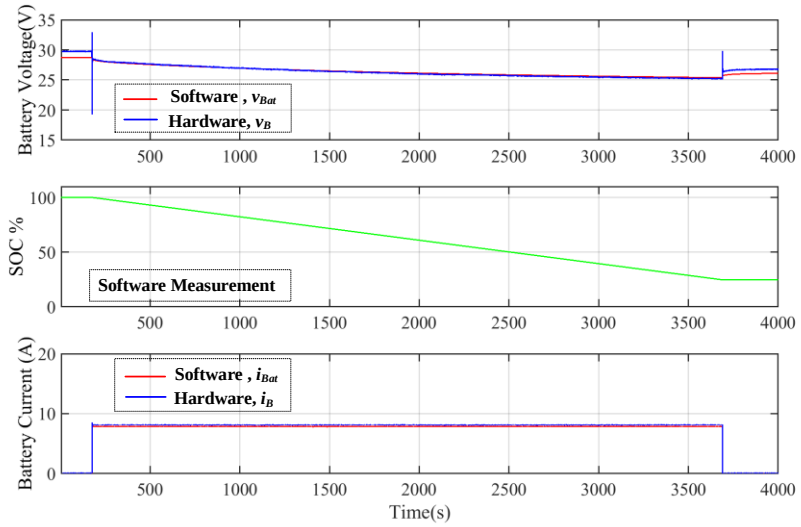
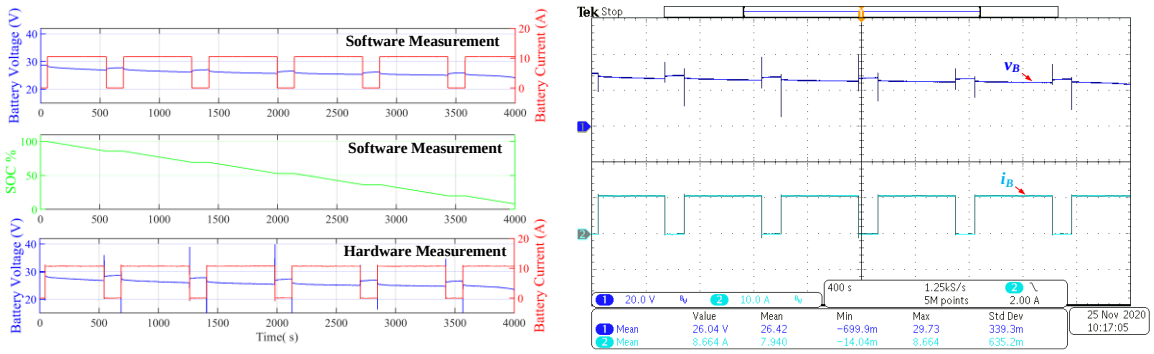


Figure 7.24 Experiment results of the PHIL-based BE during discharging operation with i_B=8 A from 100 SOC% to 25 SOC%.

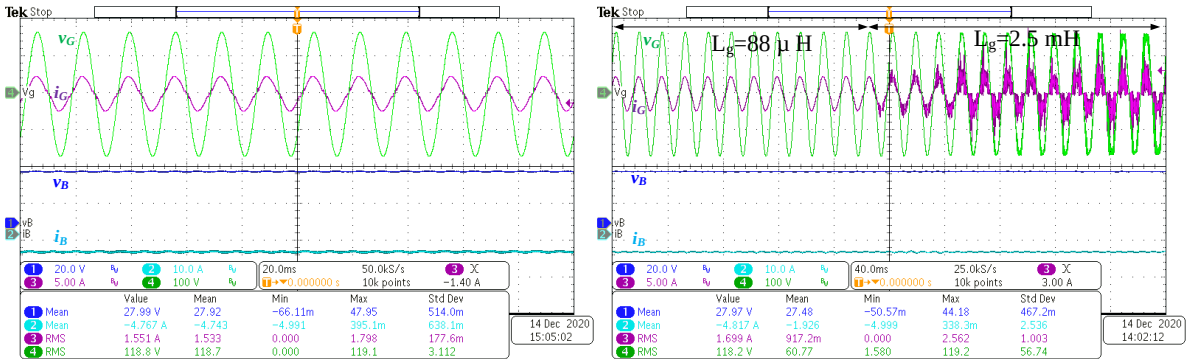


(a) (b)

Figure 7.25 Pulse discharging test results of PHIL-based BE with 1C (10.2A) (a) software (b) hardware measurements.

7.4.2 PHIL-based GE Validation

By employing $G_{CP\_100Hz}(s)$ and other parameters in Table 7-4 to the AC side PHIL implementation, a stable PHIL simulation of delta-Q IC1200 EV charger is obtained with different Z_S as predicted by the stability study. This experiment is conducted according to the configuration shown in Figure 7.2, and the EV charger is programmed with a customized charging algorithm to match the 7x12 TCL-PL-383562 Li-ion battery array parameters. The experiment results for a stable PHIL simulation of EV charger with a grid impedance of R_g=0.001, L_g=88μH is shown in Figure 7.26 (a). To examine the stability predictions made in Section III.B, results are obtained by increasing the grid impedance. Figure 7.26 (b) shows output waveforms of the PHIL-based GE when the L_g increased from 88 μH to 2.5 mH with $G_{CP\_1000Hz}(s)$.These oscillations indicates PHIL simulation of grid is unstable which agrees with theoretical calculations. To demonstrate the accuracy of the PHIL simulation of the grid, PHIL simulation results are compared with the experiment results gathered by directly connecting the EV charger to the local grid. It is approximated that the local grid inherits a similar Z_S (R_g= 0.001, L_g= 88 μH).



(a) (b)

Figure 7.26 PHIL simulation results of the delta-Q IC1200 with $G_{CP\_100Hz}(s)$, $R_g = 0.001$, L_g= 88 µH. (b) with $G_{CP\_1000Hz}(s)$, $R_g = 0.001$ when L_g is increased from 88 µH to 2.5 mH.

The comparison results are plotted in Figure 7.27 which shows that PHIL simulation results are in close agreement with real system results. The error due to the PHIL simulation is quantified by measuring the apparent power (S) difference between two systems, and error results are summarized in Table 7-5.

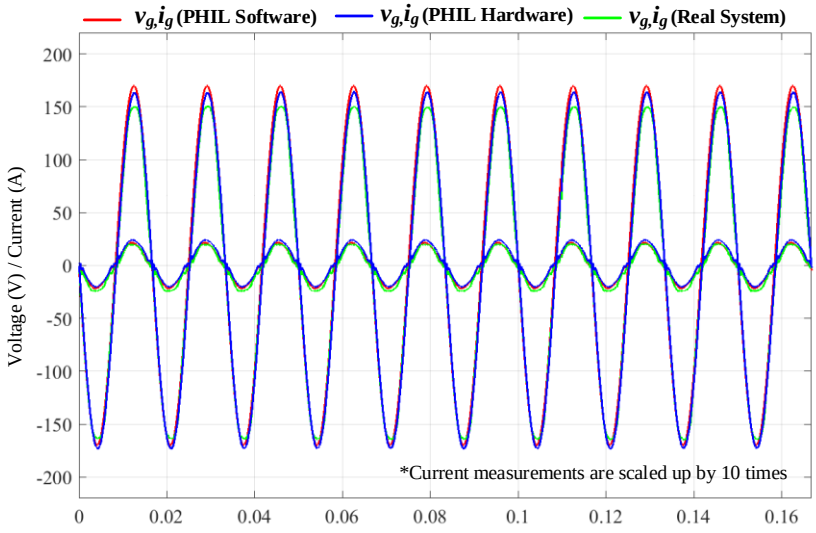


Figure 7.27 Comparison of PHIL simulation results of grid with a real experiment.

Table 7-5 Error Evaluation of the PHIL-based GE

Z_S	System in Grid-side	P (W)	Q (var)	THD %		Error % in S
				v_G	i_G	
R_g=0.001Ω, L_g=88μH	Real Experiment	173.7	*25.6*	*2.3%*	*11.7%*	-
	PHIL Simulation	183.5	*27.1*	*0.1%*	*11.1%*	*-5.7%*
R_g=0.193Ω, L_g=2.5mH	Real Experiment	178.2	*26.1*	*3.1%*	*12.3%*	-
	PHIL Simulation	177.61	*79.7*	*0.2%*	*10.9%*	*-8.1%*

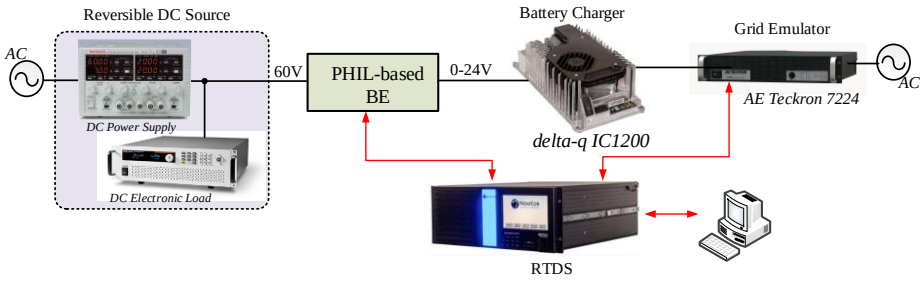


Figure 7.28 PHIL test setup with the EV charger.

7.4.3 EV Charger Performance Evaluation

Experiments are performed using the validated PHIL testbed for investigating the charging algorithm of the EV charger as well as for determining the EV charger response with grid side PQ impacts. The schematic of the experimental test configuration is shown in Figure 7.28. The charging algorithm is customized based on the Li-ion battery array parameters listed in Table 7-3. Figure 7.29 shows the experimental charge cycle results for a customized algorithm when the delta-Q IC1200 charger is connected to the emulated Li-ion battery array. This experiment is performed by setting the SOC% of the PHIL-based BE to 25% at the beginning, and results show that the EV charger is immediately started operating in CC charging mode and changed to CV mode once the BE voltage is increased to 28.5 V. Identified three different charging phases namely, bulk charging, absorption and finishing phase as

shown in Figure 7.29. The algorithm is terminated when the current tapers to a minimum charging current of 0.3 A.

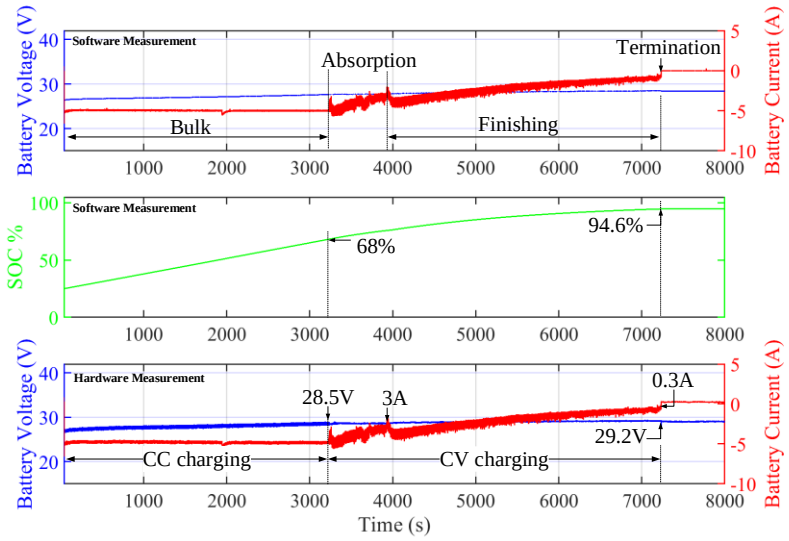


Figure 7.29 The charge cycle for an EV charger algorithm with PHIL-based BE emulating 7x12 Li-ion battery array.

Figure 7.30 shows both AC and DC side results of the same experiment captured at the oscilloscope. The transient performance of the EV charger is investigated under voltage fluctuations by applying voltage sag, 23 % of the nominal v_G and corresponding experimental waveforms are shown in Figure 7.31. Results reveal that grid current controller adjusts the input current to maintain constant power with a response time less than 1ms. Further, the protection scheme of the EV charger is tested by applying an extreme voltage sag, as shown in Figure 7.32. Results indicate that the EV charger disconnects from the grid after 19 cycles. Likewise, the designed PHIL testbed can be employed to test and validate the control system design of a grid-connected EV charger with different battery array configurations and evaluate their overall performance under transient conditions.

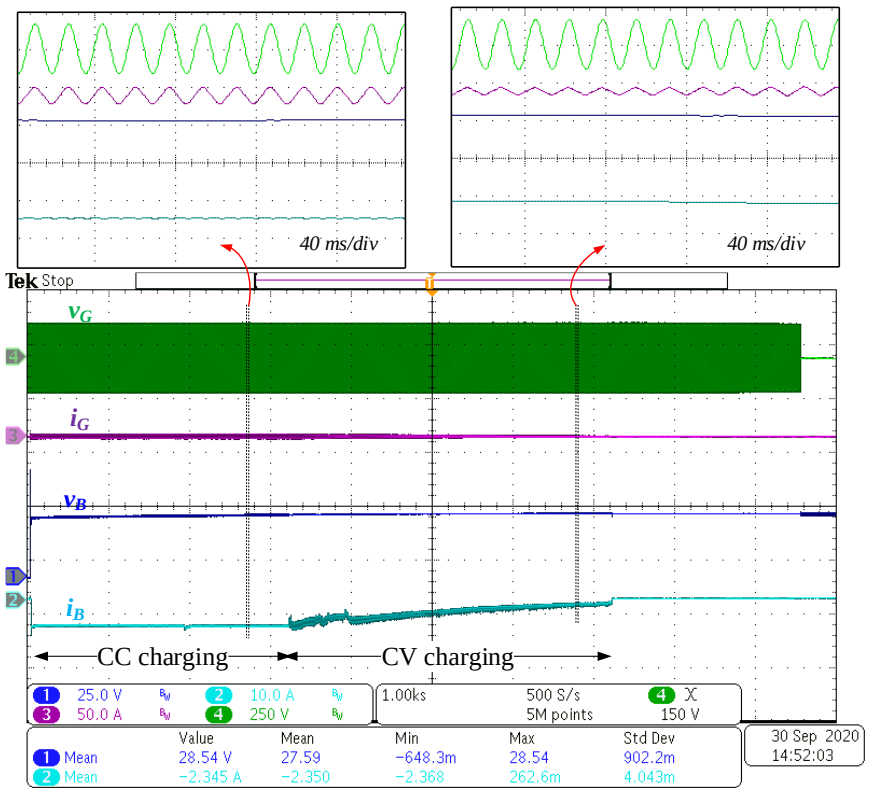


Figure 7.30 The Hardware measurement on both AC and DC side of the EV charger during the charge cycle.

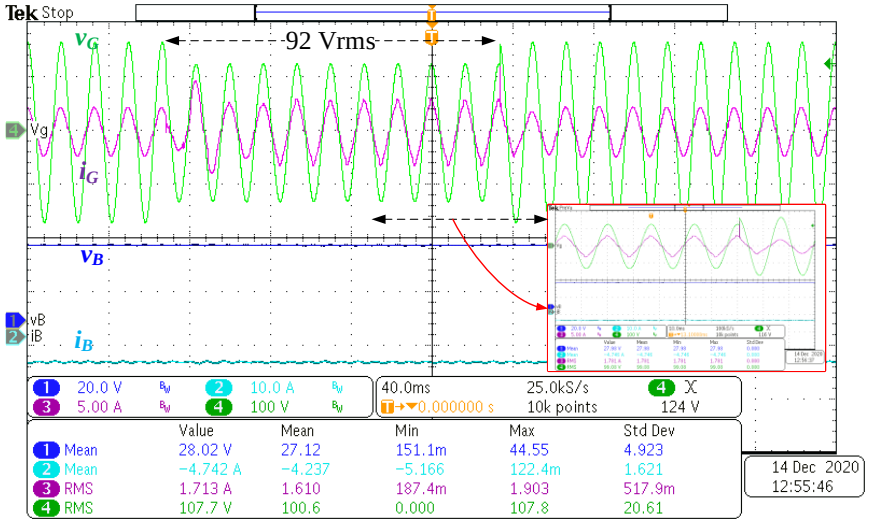


Figure 7.31 Transient response of the EV charger under grid voltage fluctuations (120 Vrms-92 Vrms-120Vrms).

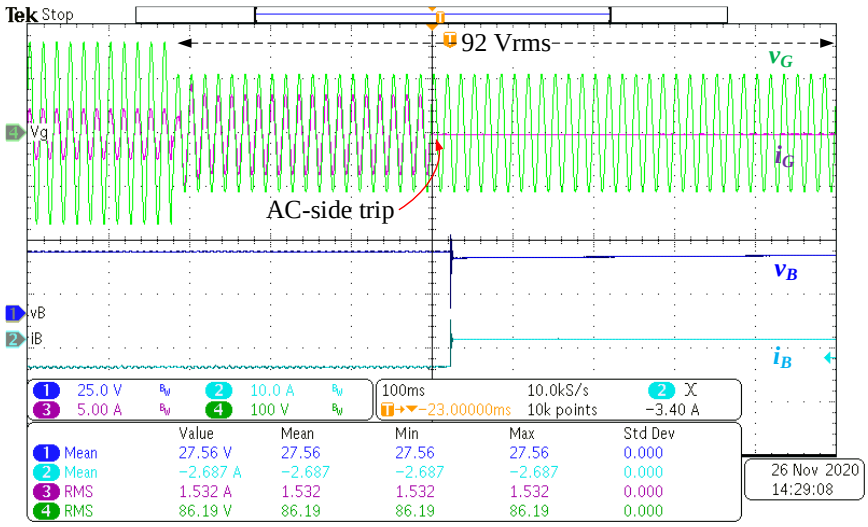


Figure 7.32 Transient response of the EV charger for an extreme voltage sag (120 Vrms-78 Vrms).

7.4.4 Evaluating LV Network: A Case Study

An LV network shown in Figure 7.33 is implemented in the RTDS^{TM} simulator to study the EV charger interactions with a weak grid scenario. The LV network is designed with a short circuit ratio (SCR) of 4 and a PV system rated at 10 kW for representing a weak grid behavior. A PV system modelled as a P-Q source is placed at the point of common coupling (PCC) bus. Voltage and frequency support functions of the PV system are disabled and operated with only P-Q control (i.e., P and power factor (pf) to evaluate the system under voltage variations. The delta-Q IC1200 charger is connected to the PCC bus as the DUT and multiple EV charger units are modelled inside RTS as P-Q load rated with 8 kW/1.25kvar. From the nominal operating conditions, EV load is increased from 8 kW to 14 kW to study the grid behavior, and PHIL simulation results are plotted in Figure 7.34. Grid voltage has reduced by 15% (from 118 Vrms to 90 Vrms) as no reactive support in the network. Although the

system is stable, this indicates that the network requires reactive power support to regulate the grid voltage within +/- 5%.

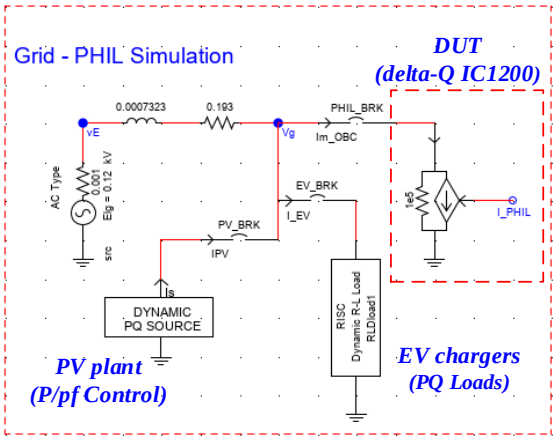


Figure 7.33 The LV network simulated in RTS software.

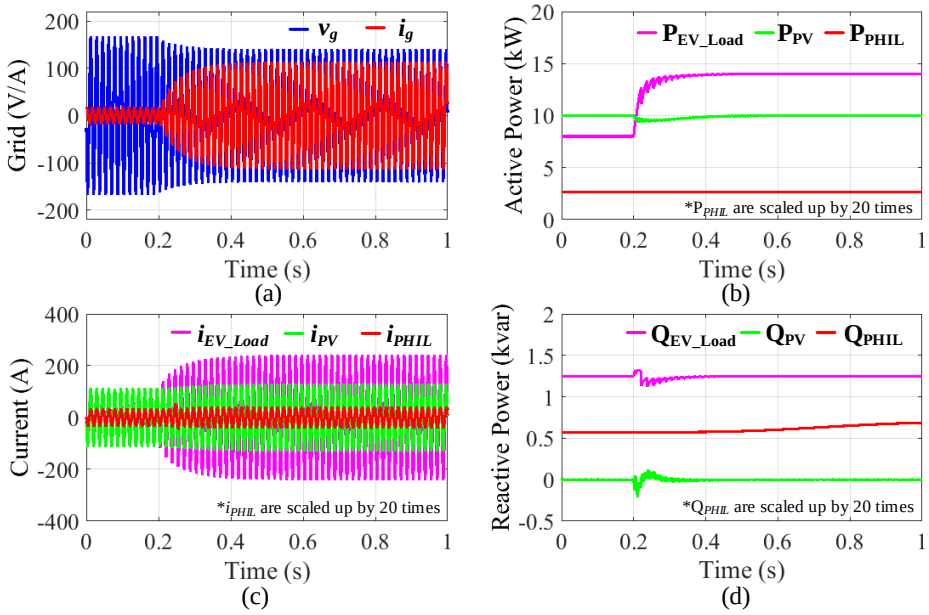


Figure 7.34 PHIL simulation results under a sudden load step change in EV loads (virtual) from 8 kW to 14 kW (a) grid voltage and current, (b) active power, (c) currents (d) reactive power, of EV loads, the PV system and, DUT.

Figure 7.35 shows the PHIL test results of the EV charger under a sudden power drop of the PV system. It indicates that the EV charger has disconnected from the grid after few cycles due to under voltage. Likewise, this approach can be used to design PV system controllers and analyze the power system behavior under different contingency test scenarios.

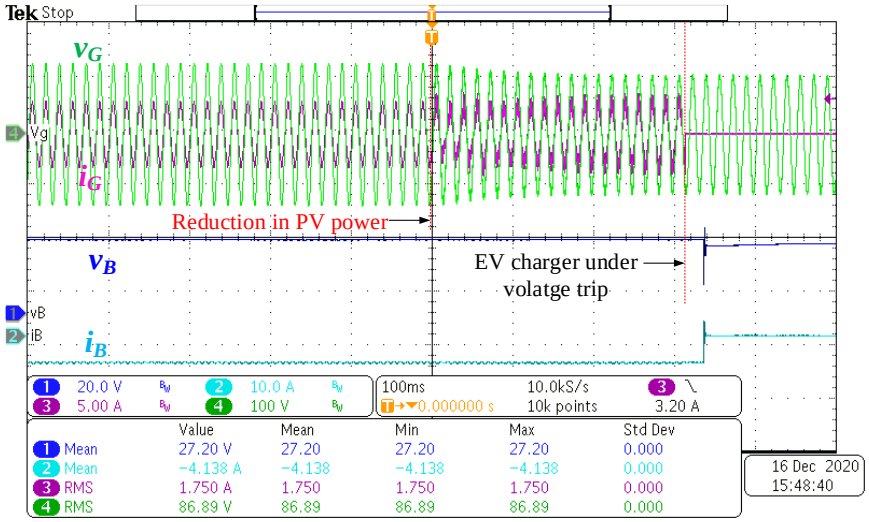


Figure 7.35 Experimental results of delta-Q IC1200 under sudden decrease in PV power from 10 kW to 100W on a weak LV grid (SCR= 4).

7.5. Summary

In this chapter, a comprehensive small-signal model capable of describing the dynamics of a PHIL testbed composed of PHIL-based BE and PHIL-based GE is presented, targeting stability and accuracy analysis. The PHIL-based BE model is developed considering dynamic relationships between the virtual battery model, switch-mode PA, and the impedance characteristics of the EV charger. Procedures to conduct stability and accuracy analysis of the PHIL simulation are presented. Further, design considerations for the linear controller of the switch-mode PA to ensure cascaded DC-DC system stability have been discussed. The impedance characteristics of DUT are obtained experimentally, which appears to be the more

practical method for accurate analysis. A similar analysis is conducted for PHIL-based GE with a linear PA in the power interface. The stability predictions made through models are validated experimentally using a PHIL test platform with an RTDS^{TM} simulator. Performance of both PHIL-based emulators is investigated experimentally, and the accuracy of PHIL simulations is determined. The designed PHIL testbed has been used to evaluate the performance of an EV charger experimentally under both strong grid and weak grid through various PHIL tests. After all, the presented modelling and analysis approach can be directly adapted by researchers, utilities, and vendors to develop a PHIL testbed capable of testing advanced EV chargers and conducting power system studies to investigate possible PQ issues that can be raised by multiple on-board chargers in an LV network.

Chapter 8

Conclusion and Recommendations for Future Research

8.1. Conclusions

This thesis introduced fast-dynamic switch-mode PAs for DC source emulation through the application of non-linear boundary control. Conventional BC with second-order switching surface provides superior transient response over other BC with first-order switching surface methods. Main challenge for σ^2 is that system performance will be significantly degraded when cascaded to non-linear switching loads with a large input capacitor. This thesis proposes a BC with a corrected second-order switching surface for buck-derived PAs to overcome the loading capacitor effect. Furthermore, in order to maintain the boundary-controlled PA performance under all types of non-linear switching loads, switch-mode PA designs based on a synchronous buck converter with a two-stage LC filter were proposed to operate in both voltage-mode and current-mode. The CM PA utilizes a cascade control scheme consists of outer deadbeat control and inner σ_{cor}^2 to guarantee fast current tracking ability. In the VM PA, the second-stage LC filter decouples high-frequency current ripple components led by load

converter passing into the PA and vice versa. Design criteria for LC filter values have been identified, and results showed that the dynamic response of all proposed switch-mode PAs is in the range of 130 µs- 250 µs.

The proposed switch-mode PAs are applied to develop a standalone PV emulator and a PHIL-based PV emulator and showed that those could be effectively used to test MPPT PV converters. In standalone PV emulators, the reference generation algorithm significantly affects the accuracy and response time of the system. A novel IOIM controller is proposed to suppress the oscillatory reference problem and provide a stable and fast convergent reference signal in the entire I-V characteristic curve. The stability of the standalone PVE emulator is analysed using the small-signal modelling technique and proved that, unlike with DRM, the reference generation loop is decoupled from the inner control loop response with IOIM as the RGA. A PHIL-based PVE is developed by integrating a PV array model in RTDS™ with the proposed CM PA via current-type ITM IA. PHIL for PV array emulation enhances the flexibility and controllability for testing PV converters in grid integration testbeds with RTSs. The stability and accuracy of the PHIL-based PVE have been studied by deriving the comprehensive small-signal model, including the virtual PV model and power interface components.

In this thesis, proposed fast-dynamic PAs are used to develop a PHIL testbed to evaluate DC-coupled PV-BES converters, which comprises a PHIL-based PVE and DC grid emulator to mimic the PV array and DC grid responses. PHIL simulations are performed to assess a DC MG with two PV-BES converter PUs in which one is modelled in RTDS™ RTS, and it is interfaced to a real PV-BES converter PU via PHIL simulation. Sub-cycle average switch models are used to simulate PV-BES converter in RSCAD/EMTDC, minimizing computation

burden. Also, this thesis presents a PHIL testbed composed of PHIL-based BE and grid emulator for testing grid-connected EV chargers. Mathematical frameworks were developed to analyze the stability and predict the accuracy of PHIL-based emulators, and stability predictions made through models were validated experimentally. The designed PHIL testbed has been used to evaluate the performance of an EV battery charger experimentally under both strong grid and weak grid through various PHIL tests. Results prove that researchers, utilities, and vendors can directly adapt the presented modelling and analysis approach to develop a PHIL testbed capable of testing advanced EV chargers and conducting power system studies to investigate possible PQ issues that multiple onboard chargers can raise in an LV network.

Major contributions made in this thesis are summarized below.

- To overcome the loading capacitor effect on conventional σ^2, a σ_{cor}^2 is proposed in Chapter 3 targeting buck-derived PAs. Results showed that σ_{cor}^2-controlled PA maintained the output voltage within specified voltage band under capacitive loads. However, this approach is limited for buck converters cascaded to non-linear switching loads that have a negligible impact on the filter capacitor current from the current ripple components generated due to switching of the second-stage converter.
- A standalone voltage-mode PV emulator based on a synchronous buck converter with the IOIM controller as the reference generation method is introduced for testing boost-derived PV converters with fast MPPT algorithms in Chapter 4. Novel IOIM control based on output impedance measurement is proposed to generate the reference signal in standalone PV emulators. Advantage of this method is that it provides a stable and fast convergent reference signal in both CCR and CVR regions of the I-V curve.

- Design and implementation of PHIL-based PVE emulator using current-mode PA are presented in Chapter 5, including the stability analysis and accuracy prediction of PHIL simulation of PV arrays via current-type ITM IA. A current-mode PA is proposed based on a synchronous buck converter with a two-stage LC filter, and its controller employs a cascaded control scheme consists of an outer deadbeat controller and inner σ_{cor}^2. This topology and control architecture eliminates the effect of switching load converter on the source converter control while providing the fast current tracking capability.
- A voltage-mode PA is proposed based on a synchronous buck converter with a two-stage LC filter to implement a PHIL-based DC grid emulator. PA controller utilizes the σ_{cor}^2 through the first-stage LC filter to control capacitor voltage, and a second-stage LC filter is placed to decouple high-frequency current ripple components led by the load converter. The proposed VM PA maintains the system performance under all types of non-linear switching loads.
- PHIL testbed design by incorporating the developed PHIL-based DC grid emulator and PHIL-based PVE is proposed for evaluating DC-coupled PV-BES converters on scalable DC microgrids. A sub-cycle average switch model is presented to simulate PV-BES converters in EMT-type real time simulations.
- A mathematical framework to design and analyze the stability of a PHIL testbed composed of PHIL-based BE and PHIL-based GE is developed in Chapter 7. PHIL-based battery emulator is designed using a switch-mode PA with a linear PI controller. Design strategies of this linear controller are provided in the context of cascaded DC-DC configuration.

8.2. Future work

This thesis proposes and demonstrates the control concepts for switch-mode DC source emulators. Following section list out several extensions that can be taken to improve the performance of DC source emulators as well as further studies that can be explored based on this thesis.

- Proposed switch-mode PA designs can be improved with the use of advanced hardware like ADC with high precision and high sampling rate, a FPGA for implementing control law and use of wide bandgap devices such as SiC / GaN for semiconductor switches to implement with a higher operating switching frequency, thereby achieve an ultra-fast response compatible with commercial linear PAs.
- Power scalability of the proposed design will be limited by the voltage ratings of semiconductors. Thus, a research study can be conducted to determine the maximum power rating achieved with the proposed PA with existing semiconductor ratings. Further, the feasibility of designing the PCS of the PA with a multiphase interleaved buck converter can be conducted to increase the power rating with high efficiency and reduce output ripple. However, a comprehensive research study will be required to apply a boundary control scheme with such PCS.
- Extend the switch-mode PA design with active front end AC-DC converter with bi-directional capability to enhances the portability. The active front-end converter enables to design PHIL testbed with power cycling for burn-in tests.
- In PHIL simulations, employ digital interface protocol like Aurora protocol with fiber optics cables to interface between switch-mode PA and Digital RTS to minimize the interface delay.

- Design a fast-dynamic AC source emulator through application of non-linear BC while performing well with all types of non-linear switching loads.
    - Proposed switch-mode PA designs in this thesis are limited for DC source emulation only because of the synchronous buck converter topology as well as for complexity in implemented outer voltage ripple control loop for σ_{cor}^2. Thus, two-level voltage source converter topology shall be adapted as the PCS topology and detail investigation is required to derive a corrected BC scheme.
- Develop a multiport converter with one AC port and three DC ports to emulate three DC sources targeting PHIL testbeds.
- Detailed stability study for the cascaded system composed of DC source emulator and downstream PE converter under different control modes.

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Appendix A

In this appendix, the derivations of expressions shown in Chapter 3 are presented.

A.1. Derivation of (3.5) and (3.8)

During Turn-ON state, by using Kirchhoff's Voltage law (KVL) for the circuit in Figure 3.4,

$$v_{Cmin} - v_C(t_1) = \frac{1}{C}\int_{t_1}^{t_2} i_C \, dt \tag{A.1}$$

Relationship between i_C and t in the time interval t_1-t_2 is derived by assuming it is a straight line,

$$i_C(t) = \frac{di_C(t)}{dt}.\Delta t + i_C(0) \tag{A.2}$$

Voltage across inductor when S_1 is ON,

$$v_L = L.\frac{di_L(t)}{dt} = v_S - v_C(t) \tag{A.3}$$

Using (3.4) and (A.3),

$$(1 + k_D)\frac{di_C(t)}{dt} = \frac{di_L(t)}{dt} = \frac{v_S - v_C(t)}{L} \tag{A.4}$$

Solving (A.2) from t_1-t_2 , considering at t_2, $i_C(\mathrm{t}_2) = 0$ and then (A.4) yields to,

$$\Delta t = t_1 - t_2 = -\frac{L}{v_S - v_C(t)}[1 + k_D]i_C(t_1) \tag{A.5}$$

The shaded area under i_C, A_1 in Figure 3.5 can be approximated by a triangle. Thus, it can be formulated as,

$$\int_{t_1}^{t_2} i_C\, dt \cong \frac{1}{2} i_C(t_1).\Delta t = -\left[\frac{L}{2(v_S - v_C(t_1))}\right][1 + k_D] {i_C}^2(t_1) \tag{A.6}$$

Thus, (3.5) can be obtained by combining (A.1) and (A.6).

During Turn-OFF state, applying the KVL for the circuit in Figure 3.4,

$$v_{Cmax} - v_C(t_3) = \frac{1}{C}\int_{t_3}^{t_4} i_C\, dt \tag{A.7}$$

The shaded area under i_C, A_2 in Figure 3.5 can be approximated by a triangle.

$$\int_{t_3}^{t_4} i_C\, dt = \left[\frac{L}{2v_C(t_3)}\right][1 + k_D] {i_C}^2(t_3) \tag{A.8}$$

Thus, (3.8) can be obtained by combining (A.7) and (A.8).

A.2. Derivation of (3.14)

By substituting (3.1) into inductor voltage equation during Turn-ON and Turn-OFF, it can be shown that,

$$t_3 - t_1 = L(1 + k_D)\left[\frac{i_C(t_3) - i_C(t_1)}{v_S - v_{ref}}\right] \tag{B.1}$$

$$t_5 - t_3 = -L(1 + k_D)\left[\frac{i_C(t_5) - i_C(t_3)}{v_{ref}}\right] \tag{B.2}$$

Voltage ripple in steady-state for this configuration can be derived as,

$$\Delta = \frac{v_{ref}(1-d)}{16LCf_S^2(1+k_D)} \tag{B.3}$$

where $d = \frac{v_{ref}}{v_S}$. Use of (3.1) and (A.3) into (A.1) for $t_1 \le t < t_3$

$$v_C(t) = v_{ref} - \Delta + \frac{v_S(1-d)}{2LC(1+k_D)}(t - t_2)^2 \tag{B.4}$$

$$(t_1 - t_2) = (t_2 - t_3) = -\frac{d}{2f_S} \tag{B.5}$$

By substituting (B5) into (B.4)

$$v_C(t_1) = v_C(t_3) = v_{ref} - 2\Delta(d - \tfrac{1}{2}) \tag{B.6}$$

Substituting (B.6) in to (9) and (11),

$$i_C(t_1) = i_C(t_5) = \sqrt{\frac{2\Delta d}{k_1'}} \tag{B.7}$$

$$i_C(t_3) = \sqrt{\frac{2\Delta(1-d)}{k_2'}} \tag{B.8}$$

Thus, substituting (B.7) and (B.8) into (B.1) and (B.2) will provide (3.14).