

Hybrid Cascaded Modular Multilevel Converters for HVDC Transmission

by

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Dedications

I dedicate this Ph.D. thesis to my loving father, Mr. Rongyi Shi.

Abstract

This thesis presents a comprehensive study of a class of modular multilevel converters (MMCs) namely hybrid cascaded MMCs. These converters have topological dc-fault blocking capability and are suitable for large-scale, long-distance high-voltage direct current (HVDC) transmission. This thesis investigates an existing hybrid cascaded MMC (HC-MMC) and novel variations thereof (mixed-SM HC-MMC) with a multi-pronged research approach based upon mathematical analyses, detailed computer simulations, and where possible experimental verifications. Several methods are proposed for control and operation of the converter under normal and faulted conditions with a view to (i) enable regulation of submodule capacitor voltages in the phase limb with reduced harmonics and the ability of extending linear modulation range, (ii) ride through balanced and unbalanced ac faults with balanced phase currents and efficient ac-fault recovery, and (iii) successfully ride through dc faults with prompt isolation of the ac and dc sides and rapid decay of the dc fault current. These methods are extensively analyzed using detailed electromagnetic transient simulation and experimental work where possible. Converter losses and efficiency maps are also quantified using detailed computer modeling methods to evaluate the benefits of the existing and proposed HC-MMCs. Compared with the original HC-MMC, the proposed mixed-SM HC-MMC has superior performance in terms of extended linear modulation range, system efficiency, and dc-fault clearing performance. The thesis also formulates the design guidelines of SM capacitor sizing considering submodule redundancy and different control modes. Extensive analytical, simulation-based, and experimental measurements are provided to confirm the validity and efficacy of the developed guidelines.

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Nomenclature

List of symbols

C_{fb}	Full-bridge submodule capacitor in the phase limb	T_o	Fundamental period
C_{fm}	Full-bridge submodule capacitor in the main power stage	v_{2L}	Instantaneous voltage across two arm inductors
C_{hb}	Half-bridge submodule capacitor	v_{2L-2nd}	2 nd harmonic component of v_{2L}
C_p	Stray capacitance	v_{conA}	Converter's phase-A voltage
C_{sm}	Submodule capacitor	$v_{csm-2nd}$	2 nd harmonic component in a submodule capacitor voltage
EoP_{Allsm}	Stored energy in submodule capacitors per power rating unit	v_{csmLow}	Lower-arm submodule capacitor voltage
EoP_{FBmain}	Stored energy in full-bridge submodule capacitors in the main power stage per power rating unit	v_{csmUp}	Upper-arm submodule capacitor voltage
EoP_{FBph}	Stored energy in full-bridge submodule capacitors in the phase limb per power rating unit	$v_{conA-ref}$	Reference voltage for the converter's output in phase A
EoP_{HBmain}	Stored energy in half-bridge submodule capacitors in the main power stage per power rating unit	v_{fbA}	Voltage across the phase-limb submodules in phase A
EoP_{main}	Stored energy in all submodule capacitors in the main power stage per power rating unit	$v_{fbA-ref}$	Reference voltage for the phase limb in phase A
f_{car}	Carrier frequency	v_{lowA}	Voltage across the lower-arm stacked submodules in phase A
f_o	Fundamental frequency	v_{mA}	Voltage crafted by the main power stage in phase A
i_{2nd}	2 nd harmonic current in the arm	v_{mA-ref}	Reference voltage for the main power stage in phase A
i_{conA}	Converter's phase-A current	v_{out}	Synthesized voltage
i_{low}	Lower-arm current	v_{pccABC}	Three phase voltage at the point of common coupling

i_{sABC}	Three-phase source current	v_{ref}	Reference voltage for modulation
i_{up}	Upper-arm current	v_{sABC}	Ideal three-phase source voltage
I_{2nd}	Magnitude of the 2 nd harmonic current	v_{upA}	Voltage across the upper-arm stacked submodules
I_{dc}	DC-side current	v_z	Control variable to eliminate the circulating current in the arm
I_m	Magnitude of phase current	V_{1rms}	Root-mean-square voltage of fundamental component
k_{3rd}	Amount of the injected 3 rd harmonic in the modulation waveform	V_{1st}	Voltage magnitude of fundamental voltage
k_{flt}	Number of faulted submodules over the nominal number of submodules per arm	V_{acref}	Reference of ac voltage magnitude
k_{fm}	Number of full-bridge submodules in the main power stage over the nominal number of submodules per arm	V_{cfb}	Average voltage of FB-SM capacitor in the phase limb
k_{red}	Number of redundant submodules over the nominal number of submodules per arm	$V_{cfbA-avg}$	Average voltage of full-bridge submodule capacitors in the phase limb in phase A
k_{SOGI}	Open-loop gain of the SOGI	V_{cfm}	Average voltage of FB-SM capacitor in the main power stage
k_{trap}	Positive slope of a trapezoidal waveform	$V_{cfb-ref}$	Reference voltage for full-bridge submodule capacitor voltage in the phase limb
K_{ripple}	Requirement of capacitor voltage ripple in percentage	V_{chb}	Average voltage of HB-SM capacitor
L_{arm}	Arm inductance	V_{csm}	Submodule capacitor voltage
L_p	Stray inductance	$V_{csm-2nd}$	Magnitude of $v_{csm-2nd}$
L_s	Source inductance	V_{dc}	DC-link voltage
L_{s_con}	Source inductance reflected to the converter side	V_{rms}	Root-mean-square voltage
m	Modulation index	V_{sin_rms}	Root-mean-square voltage of a sinusoidal waveform
m_{low}	Instantaneous lower-arm modulation waveform	V_{tr-con}	Rated voltage of converter-side windings in a transformer
m_{mpk}	Normalized peak value of the voltage crafted by the main power stage	V_{trap_rms}	Root-mean-square voltage of a trapezoidal waveform
m_{new}	Updated modulation index with increment	V_{tr-sys}	Rated voltage of grid-side windings in a transformer

m_{rated}	Rated modulation index	$V_{s_con_nom}$	Nominal source voltage reflected to the converter side
m_{up}	Instantaneous upper-arm modulation waveform	V_z	Magnitude of v_z
n_{tr}	Transformer's turns ratio	X_{Larm}	Arm inductor's impedance
N_{Allsm}	Number of all submodules in a three-phase converter	X_{TR}	Transformer's leakage inductor's impedance
N_{car}	Number of carriers	Z_s	Source impedance
N_f	Number of full-bridge submodules per phase limb	Z_{s_con}	Source impedance reflected to the converter side
N_{fm}	Number of full-bridge submodules per arm	Δm	Incremental of modulation index
N_h	Number of half-bridge submodules per arm	Δv_{csmLow}	Lower-arm submodule capacitor voltage ripple
P_{conA}	Average power absorbed by the converter's output in phase A	Δv_{csmUp}	Upper-arm submodule capacitor voltage ripple
P_{fbA}	Average power delivered by the phase limb in phase A	$\Delta v_{\text{chbUp_pp}}$	Upper-arm half-bridge submodule capacitor voltage ripple value
P_{mA}	Average power delivered by the main power stage in phase A	ω_b	Fundamental angular frequency
P_{nom}	Nominal real power	φ	Power factor angle
P_{ref}	Reference of real power	θ	Phase angle
q_{up}	Instantaneous charge of upper-arm submodule capacitors	$\theta_{2\text{nd}}$	Phase angle of the 2 nd harmonic current
Q_{ref}	Reactive power reference	θ_{icon}	Phase angle of the converter's phase current
r_{on}	ON resistance of semiconductor	$\theta_{\text{iup1}},$ θ_{iup2}	Critical angles of zero-crossing points of upper-arm current
R_{arm}	Equivalent resistance per arm	$\theta_{\text{mup1}},$ θ_{mup2}	Critical angles of zero-crossing points of upper-arm modulation waveform
R_s	Source resistance	$\theta_{v\text{con}}$	Phase angle of the converter's phase voltage
R_{s_con}	Source resistance reflected to the converter side	θ_{vz}	Phase angle of v_z
S_{TR}	Transformer's capacity		

List of abbreviations

AC	Alternating current
APOD-PWM	Alternative phase-opposition-disposition pulse-width modulation
CCSC	Circulating current suppressing control
CPS-PWM	Carrier phase-shifted pulse-width modulation
DC	Direct current
EMT	Electromagnetic transient
FACTS	flexible alternating current transmission systems
FB	Full-bridge
FFT	Fast Fourier transform
GTAI	Gigabit transceiver analogue input
GTDI	Gigabit transceiver digital input
GTDO	Gigabit transceiver digital output
HB	Half-bridge
HC-MMC	Hybrid-cascaded modular multilevel converter
HVDC	High-voltage and direct-current
IGBT	Insulated gate bipolar transistor
KVL	Kirchhoff's voltage law
KCL	Kirchhoff's current law
LCC	Line commutated converter
MMC	Modular multilevel converter
NLC	Nearest level control
PCC	Point of common coupling
PD-PWM	Phase-disposition pulse-width modulation
POD-PWM	Phase-opposition-disposition pulse-width modulation
PLL	Phase locked loop
PR	proportional-resonant
PWM	Pulse-width modulation
RMS	Root mean square
RTDS	Real-time digital simulator
SCR	Short circuit ratio
SOGI	Second-order generalized integrator
SM	Submodule
THD	Total harmonic distortion
VSC	Voltage-source converter

Chapter 1

Introduction

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1.1 Background and motivation

In recent years, rapid developments in semiconductor technology have driven the upsurge of fully controllable voltage-source converters (VSCs) in high-voltage and high-power applications [1]-[3]. Among the various VSCs, modular multilevel converters (MMCs) have attracted significant research interest in a variety of applications including, but not limited to, high-voltage direct current (HVDC) transmission system [1]-[7], flexible alternating current transmission systems (FACTS) [1], [8], wind energy applications [9]-[10] and renewable energy conversions [11]-[12]. At present, MMCs are considered as the most promising HVDC converter topologies due to various appealing operating attributes. In comparison with conventional multilevel converters such as diode- and capacitor-clamped converters [13]-[14], MMCs possess significant benefits such as a high level of controllability, improved voltage harmonics, and low losses in

scalable topologies that can be adapted to different ratings. In the context of HVDC transmission systems, MMCs offer reduced filtering requirements, immunity to commutation failure, lower voltage insulation requirement on converter transformers, and often a more compact substation footprint than line-commutated converters (LCCs) [15], which are the classical converter type employed in HVDC transmission systems.

The first MMC topology was based upon half-bridge (HB) submodules (SMs) and has been extensively studied for HVDC transmission [16]-[17] and other high-power applications [9]-[10], [18]. Despite its benefits, the conventional HB-MMC topology is unable to topologically block dc short-circuit faults, which is a severe drawback particularly in point-to-point HVDC transmission. To compensate the shortcoming of topological dc-fault blocking incapability of the conventional HB-MMC, a new class of MMC topologies, which primarily take advantage of full-bridge (FB) SMs, are being explored to enable direct, converter-based blocking of dc faults. In general, MMCs, particularly those with dc-fault blocking abilities, are complex systems that require specialized controls to ensure proper operations in steady state, transient, and faulted conditions. A number of key considerations are of importance in this regard and need to be understood and carefully studied.

1.2 Literature review

In this section, a review of relevant previous studies of MMCs is presented. This discussion also explains the rationale for the choice of the MMC topology investigated in this thesis.

1.2.1 SM types

As the attribute of modularity suggests, MMCs are commonly built with a large number of building blocks of either similar or different topologies [4]-[8], [19]-[34]. These building blocks

are commonly named SMs or cells. Generally, SMs are categorized into three types based upon their possible terminal voltage levels: unipolar, symmetrical, and asymmetrical SMs [35]-[36]. A number of typical SMs are shown in Fig. 1.1, where the corresponding terminal voltage levels and operating zones are also displayed. The comparison of hardware configuration for SMs shown in Fig. 1.1 is summarized in Table 1.1. Some observations from Fig. 1.1 and Table 1.1 are summarized as follows:

(i) SMs shown in Fig. 1.1 (a), (c), (d) and (e) are unipolar types, as the SM terminal voltage levels are either zero or a positive value;

(ii) SMs shown in Fig. 1.1 (f), (g) and (h) are asymmetrical bipolar types, because the SM terminal voltage permits both positive and negative levels but not symmetrical levels;

(iii) SMs shown in Fig. 1.1 (b) and (i) are symmetrical bipolar types;

(iv) Compared with SMs shown in Fig. 1.1 (c)-(i), SMs shown in Fig. 1.1 (a)-(b) have relatively simple circuits and operating principles. Therefore, these two SMs, named HB and FB SMs, are the most commonly-used SMs in MMC topologies.

(v) SMs shown in Fig. 1.1 (e) and (g) consist of a configuration of two identical switches (i.e., switches T_1 and T_2 , and T_3 and T_4) in series to achieve equal voltage stresses for all switches;

(vi) As seen from the diagrams that show the relationship between the SM terminal voltage (v_{sm}) and the capacitor currents (i_c , i_{c1} , or i_{c2}), the bipolar SMs allow their capacitors to charge (i.e., $i_c > 0$) and discharge (i.e., $i_c < 0$) regardless of the terminal voltage polarity, which permits high opportunities to balance capacitor voltages. Furthermore, the bipolar SMs may provide dc-fault blocking capability, because the SM capacitors are inserted and charged after all gate signals are blocked. However, the unipolar SMs lack such functionality;

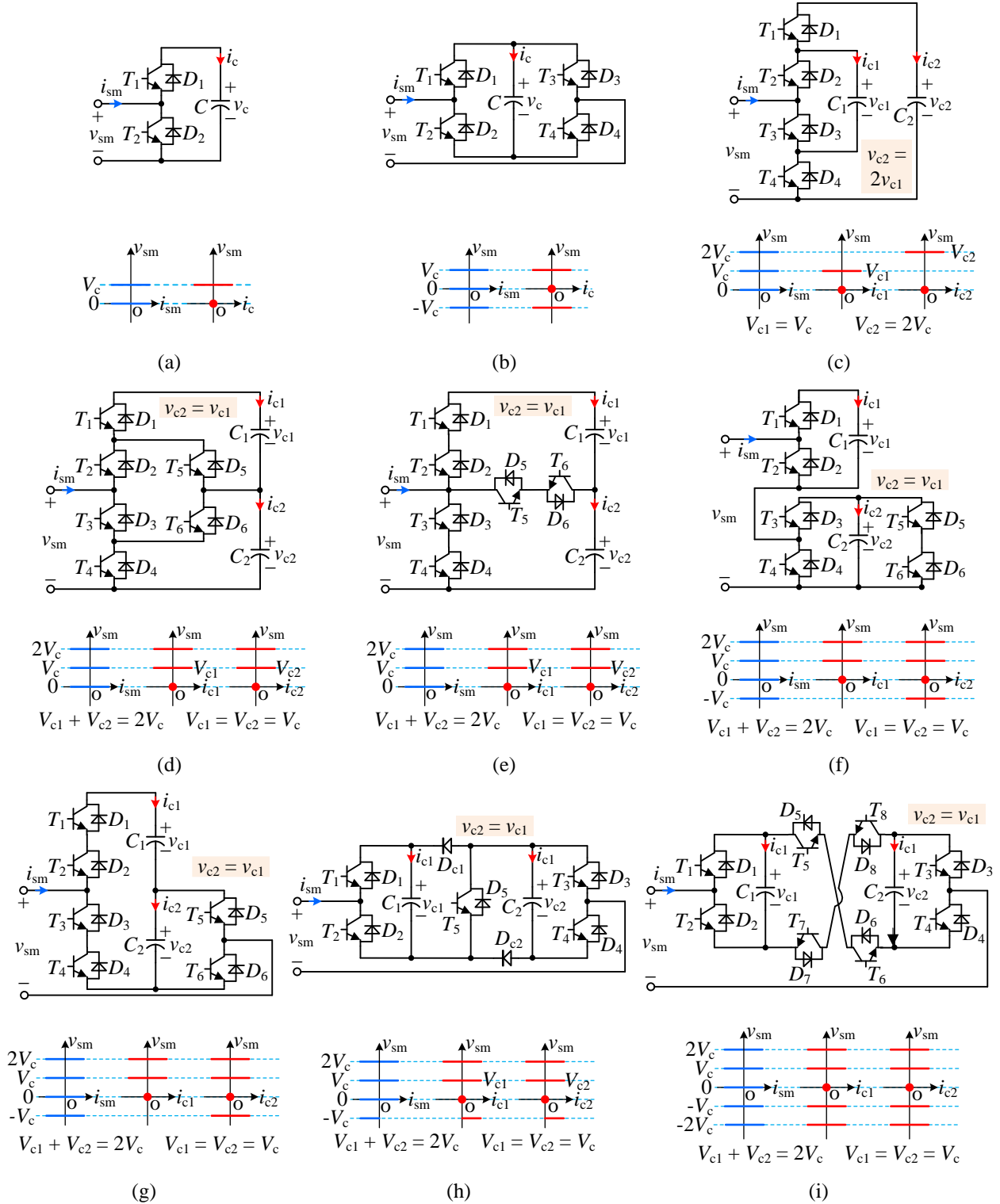


Fig. 1.1: A number of typical SMs for MMCs

(a) HB SM; (b) FB SM; (c) 3L-FC SM; (d) three-level neutral-point clamped (3L-NPC) SM; (e) three-level T-type neutral-point clamped (3L-TNPC) SM; (f) mixed SM; (g) four-level asymmetric SM; (h) four-level double clamped SM; (i) five-level cross-connected SM.

(vii) The SMs shown in Fig. 1.1 (c)-(i) consist of more than one capacitor and possess identical average capacitor voltages, except the three-level flying-capacitor (3L-FC) SM displayed in Fig. 1.1 (c). In this particular SM, the outer capacitor (C_2) has double the average voltage of the inner capacitor (C_1), which makes capacitor voltage balancing more complicated;

(viii) Among the SMs that consist of six switches shown in Fig. 1.1 (d)-(g), the SM shown in Fig. 1.1 (d) has the same functionalities as those of the SM shown in Fig. 1.1 (e) in terms of voltage levels, relationships between v_{sm} and i_{sm} , i_{c1} and i_{c2} , and the number of isolated gate drivers. Comparing SMs shown in Fig. 1.1 (f) and (g), the former SM can achieve the same functionalities with fewer isolated gate drivers than the latter one (see Table 1.1).

Table 1.1: Comparison of hardware configurations for SMs shown in Fig. 1.1

SM	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)
No. of voltage levels	2	3	3	3	3	4	4	4	5
No. of switches	2	4	4	6	6	6	6	7	8
No. of isolated gate drivers	2	3	4	5	5	4	5	4	6
Max. no. of conducting switches	1	2	2	2	2	3	3	3	4
No. of capacitors	1	1	2	2	2	2	2	2	2

In summary, among the SMs shown in Fig. 1.1, HB and FB SMs are essentially basic SMs used to construct a number of different MMC topologies [4]-[8], [19]-[34], because the circuits, operating principles, and capacitor voltage balancing algorithms of HB and FB SMs are relatively simple. They are also proven to be the preferred options in industrial applications [4]. Apart from these two SMs, all the remaining SMs shown in Fig. 1.1 possess not only a global capacitor voltage balancing issue but also local capacitor voltage balancing issues, which makes the task of capacitor voltage balancing control more complicated.

1.2.2 Development of MMC topologies

The conventional three-phase HB-MMC topology is shown in Fig. 1.2 (a), which consists of a stack of HB SMs in series with an arm inductor in each arm. The nominal SM capacitor voltage is set to V_{dc}/N , where V_{dc} is the dc-link voltage and N is the number of SMs per arm. The arm inductor is used to suppress harmonics in the arm currents in normal operation and limit the rate of rise of the fault current under dc-fault conditions. From a practical point of view, stable and reliable operation of MMCs is an important factor to determine their viability in high-voltage and high-power applications. One of the most common applications for MMCs is in HVDC transmission systems, which mostly consist of long-distance overhead lines or undersea cables. Due to adverse disturbances, faults, or equipment failure, the transmission paths may be shorted to one another or to the earth – a condition known as a dc fault, which may cause catastrophic damage to power electronic converters if effective protection mechanisms are not in place.

The widely-used conventional HB-MMC is unable to block dc faults due to its incapability to oppose the ac system voltage. In the event of a dc fault, even though HB SMs are blocked, the ac system continues to feed the faulted dc side through the reverse-conducting diodes used in SMs. To prevent this, a simple solution is to open the ac circuit breakers immediately after a dc fault is detected. However, the reality is that operating ac circuit breakers takes relatively long time, resulting in large fault current flow through SMs and longer recovery time after clearing the fault. The fundamental objectives under dc faults are to protect SM semiconductors from overcurrent and SM capacitors from overvoltage, therefore protecting the converter from damage. Apart from the usage of ac circuit breakers, protective thyristors paralleled with the SM output terminals are also adopted in conventional HB-MMC to deviate a part of the fault current away from the antiparallel diodes. However, these additional components increase the control complexity and

converter cost. Nowadays, another option to block dc faults using hybrid dc breakers is proposed [37]-[39]. Hybrid dc breakers based upon power electronic devices have superior performance than conventional mechanical breakers in terms of break time. However, the demand of large breaking current capacity increases the difficulties in developing hybrid dc breakers.

To enable converter's SMs to provide the voltage with opposite polarity to counter the ac voltage during dc faults, the three-phase FB-MMC was developed as shown in Fig. 1.2 (b), which has a similar hardware configuration to an HB-MMC except for the SM types. In the event of a dc fault, all FB SMs are blocked and all SM capacitors remain in the circuit's conducting path to provide a voltage up to V_{dc} (In fact, $V_{dc}/2$ is the minimum voltage to block dc faults) to oppose the ac voltage. This leads to the fault current to charge the FB-SM capacitors regardless of the current polarity and hence the fault current decays quickly. The stack of FB-SM capacitors is able to oppose the ac system's voltage and counter its contribution to a dc fault, thereby providing dc-fault blocking capability. In normal operation of a FB-MMC, each FB SM is operated as an HB SM, only providing zero and positive voltage levels. Compared with HB-MMC, FB-MMC has double the number of total switches, which leads to higher cost, increased semiconductor losses, and a larger footprint.

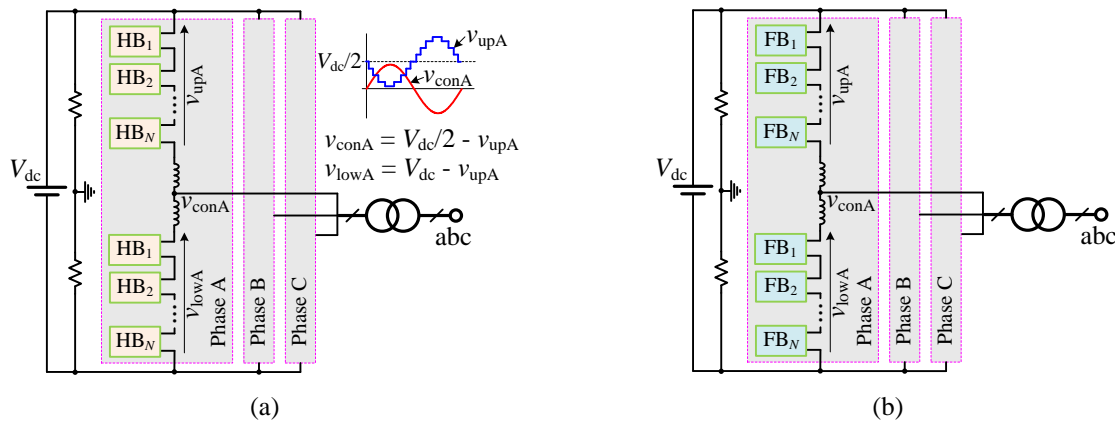


Fig. 1.2: Conventional MMC topologies

(a) half-bridge MMC (HB-MMC); (b) full-bridge MMC (FB-MMC).

As such, the MMC topologies possessing topological dc-fault blocking capability and economical merits have attracted significant research attention [4]-[8], [19]-[34]. These novel MMCs mainly deploy FB SMs in their topologies, either as the only building block or in combination with HB SMs [21], [25] or other controlled switching configurations [31]-[32]. A number of novel MMC topologies with dc-fault blocking capability are shown in Fig. 1.3, where v_{upA} and v_{lowA} are the voltages across the SM stacks in the upper and lower arms of phase A, respectively, and v_{conA} is the converter's output voltage of phase A. Brief descriptions about the operations and comparisons of these topologies are made as follows:

(i) The MMC topology shown in Fig. 1.3 (a) comprises an identical number of HB and FB SMs per arm [30], which essentially lowers the dc-fault blocking voltage to $V_{\text{dc}}/2$. Compared with the conventional FB-MMC, this topology has $2N$ fewer switches in total and N fewer conducting switches at each instant, where N is the total number of SMs per arm.

(ii) Compared to the conventional FB-MMC, Fig. 1.3 (b) shows the alternate arm MMC (AA-MMC), which additionally introduces the director switches DS_p and DS_n with N switches in series to select the proper arm to craft the corresponding phase voltage [21], where N is the number of FB SMs per arm; another difference is that the nominal SM capacitor voltages are set as $V_{\text{dc}}/(2N)$ instead of V_{dc}/N due to the alternating arm operation. As such, AA-MMC only has half the number of FB SMs used in the conventional FB-MMC if switches with the same ratings are employed. However, capacitor voltage balancing between arms in AA-MMC is a major challenge because the capacitor voltages are uncontrollable for the arm not participating in crafting the phase voltage.

(iii) To prevent the phenomenon of arm usage for only a half period in AA-MMC, the hybrid MMC with H-bridges is shown in Fig. 1.3 (c), in which the voltage across the arm SMs is rectified to form the ac phase voltage [26]-[28]. However, in practice, the synchronization of the firing

pulses for semiconductors in series is challenging due to different parasitic parameters in semiconductors.

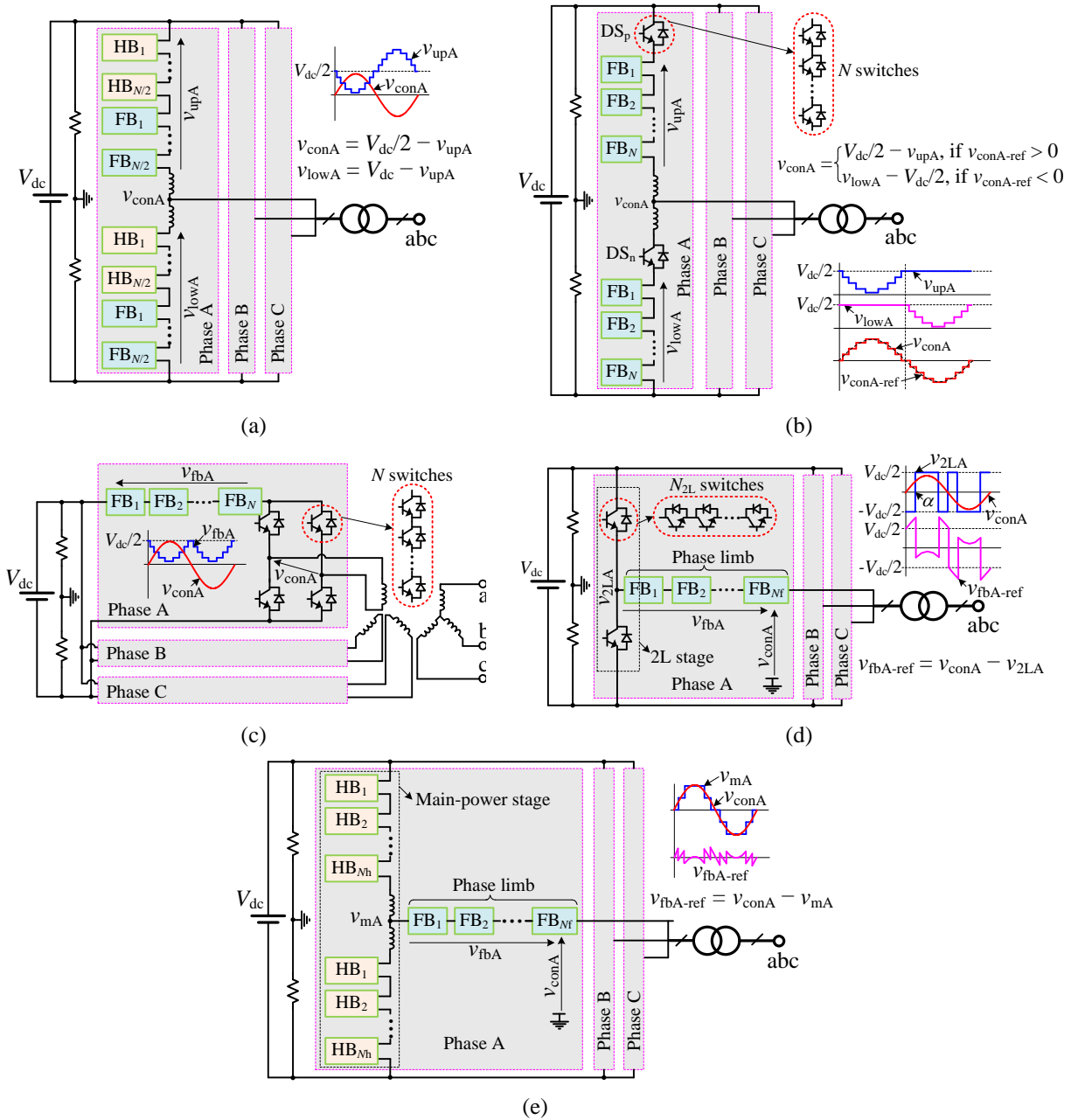


Fig. 1.3: Novel MMC topologies with dc fault blocking capability

(a) mixed-SM MMC; (b) H-bridge alternative arm MMC (AA-MMC); (c) hybrid MMC with dc-side cascaded FB chain links; (d) hybrid cascaded MMC with two-level converter at dc side; (e) hybrid cascaded MMC (HC-MMC).

(iv) The hybrid MMC shown in Fig. 1.3 (d) consists of two stages: the two-level (2L) stage composed of a two-level converter with N_{2L} switches in series and the phase limb made up of cascaded FB SMs [20]-[24]. The 2L stage is responsible to control the fundamental component of the phase voltage, whereas the FB stack in the phase limb is utilized as an active filter to remove the heavy harmonics from the voltage crafted by the two-level converter and establish a staircase-like phase voltage. In order to block dc faults, the total capacitor voltages of the FB stack must be at least equal to $V_{dc}/2$. To achieve the minimum requirement on the voltage stresses of the switches, the nominal voltage across the FB stack is set as $V_{dc}/2$. As such, the nominal capacitor voltage of each FB SM is set as $V_{dc}/(2N_f)$, where N_f is the number of FB SMs per phase limb. In order to make use of the filtering functionality of the cascaded FB SMs, the two-level stage commonly uses the one-notch selective harmonic elimination (SHE) method [20]-[23], which is of low frequency and permits only one controllable angle (α), where the controllable angle is determined by the fundamental component. The reference for the FB stack ($v_{fbA-ref}$) is readily obtained from the subtraction of the reference phase voltage (v_{conA}) and the two-level converter voltage (v_{2LA}). As seen from the typical operating waveforms shown in Fig. 1.3 (d), the waveform of $v_{fbA-ref}$ exceeds $\pm V_{dc}/2$ at some points, which is beyond the maximum capability of the FB stack. To prevent over-modulation in the FB stack, 3rd harmonic subtraction from the reference across the FB stack is used to limit the reference within $\pm V_{dc}/2$ [22]-[23]. Since the two-level converter stage permits low-frequency (commonly three times the fundamental frequency) modulation, it is helpful in lowering the semiconductor losses. However, the large level change (up to V_{dc}) of the voltage crafted by the two-level converter may cause large voltage spikes if the firing pulses are not perfectly synchronized between the two-level converter stage and the FB stack [21]-[24]. In practice, the synchronization of the firing pulses in this topology is challenging due to different

parasitic parameters in semiconductors. Furthermore, the FB-SM capacitor voltages need special supervision to be maintained at their nominal values [24].

(v) To compensate the shortcoming of the hybrid MMC shown in Fig. 1.3 (d), the hybrid cascaded MMC (HC-MMC), which is proposed in [25] and shown in Fig. 1.3 (e), replaces the two-level converter stage with a conventional HB-MMC. Similar to the operation of a conventional HB-MMC, the main power stage holds HB SMs with V_{dc}/N_h capacitor voltages, where N_h is the number of HB SMs per arm. In order to lower the semiconductor losses, the main power stage commonly operates with a low switching frequency. Nevertheless, compared with the topology shown in Fig. 1.3 (d), the voltage crafted by the main power stage is much closer to the phase voltage and thus the reference voltage for the FB stack is much smaller. Since the voltage level change of the main power stage can be as small as V_{dc}/N_h (one HB-SM capacitor voltage), the ensuing voltage spikes can be significantly reduced even with imperfect synchronization of firing pulses. Furthermore, HC-MMC has $2N_h$ more switches in total, and N_h more conducting switches per phase than the MMC shown in Fig. 1.3 (d) if similarly rated switches are used and thus $N_h = N_{2L}$; however, the FB stack in HC-MMC has a significantly smaller filtering burden, which is beneficial in lowering the switching losses of the FB stack. Since the main power stage of HC-MMC can craft a low-harmonic voltage, it is necessary to investigate the influence of different numbers of HB and FB SMs on the harmonics of the phase voltage, and the impact of the switching frequencies for the two stages in HC-MMC on the overall converter losses. In addition, control schemes for FB-SM capacitor-voltage regulation must be investigated and utilized, since there is no inherent mechanism to adjust the FB-SM capacitor voltages to their nominal values.

1.2.3 Key considerations for MMC operation

To properly operate MMCs and thus achieve all their inherent merits, several fundamental requirements must be satisfied including proper component design and control algorithms. As stated in Section 1.2.2, a novel class of MMCs with topological dc-fault blocking capability have attracted much attention [4]-[8], [19]-[34]; however, these topologies have not been fully investigated in terms of design guidelines, SM capacitor sizing, control techniques under normal and faulted conditions, and system efficiency. A brief introduction to the key techniques for MMC operation is given in the following subsections.

1.2.3.1 SM-capacitor voltage balancing methods

To achieve stable and reliable operation for MMCs, it is mandatory that the SM capacitor voltages must be well balanced and maintained at their nominal values to craft the staircase waveform with reduced harmonic distortion and to ensure safe and identical voltage stresses on semiconductor devices. A widely-used balancing method is the sorting and rotating approach [33]. As the method's name suggests, all the capacitor voltages of the SMs in a stack are arranged in either ascending or descending order; the number of inserted SMs at any instant is determined by the modulation method; and the polarity of the current flowing through SMs determines if the SMs with lower or higher capacitor voltages should be inserted. This approach to balance a stack of SMs is proven to be effective. Nevertheless, this method has a main drawback of computational cost when applied to MMCs with a larger number of SMs. As such, novel methods have been proposed to reduce the computational cost and lower the number of switching events [40]-[44]. Additionally, balancing approaches in [44] and [45] are developed to achieve a reduction in the voltage harmonic distortion and to evenly-distribute power losses within converter SMs.

1.2.3.2 SM capacitance selection

Proper MMC operation requires SM capacitor voltages to be balanced and maintained at their nominal value. If SM capacitance is not properly selected, it results in large capacitor voltage ripple and lost control of arm currents with undersized capacitors, and large footprint and high cost with oversized capacitors. It is a common practice that SM capacitor size for the conventional HB-MMC is mainly selected based upon the stored energy in all SM capacitors per power rating unit of 30.0~40.0 kJ/MVA, giving SM capacitor voltage ripple in the range of 10% [46]. This empirical guideline lacks solid analytical foundations. In the existing literature [47]-[48], SM capacitor size is determined by the variation of the energy stored in the SM capacitor, and the operating point used to calculate the stored energy is obtained based upon a number of assumptions, such as ignoring the influence of converter transformers and strength of ac network. In addition, limited literature exists regarding SM capacitor sizing for novel MMCs with dc-fault blocking capability [47]-[48]. Therefore, a systematic and thorough study of SM capacitor sizing is necessary to achieve both proper operation and small physical footprint for such MMCs.

1.2.3.3 DC-fault ride-through capability

In an HVDC transmission system, the primary dc-fault types are pole-to-pole and pole-to-ground faults [49]. The fault behavior may be different for different configurations of pole stations. Generally, two types of pole configurations are used. One is the monopole system and the other is the bipolar system. For the monopole system, the return path may use the ground or sea or metal, and hence the pole-to-ground fault is the most dominant fault type. During a pole-to-ground fault, the dc-link voltage is approximately zero in the monopole system. For the bipolar system, pole-to-pole faults lead to approximately zero voltage across the dc terminals, whereas the pole-to-ground

fault impresses the total dc-link voltage across the ungrounded pole and the return path. Therefore, the fault behavior may be different under different configurations for HVDC transmission systems.

In the context of MMC-based HVDC transmission systems, pole-to-pole faults may lead to rapidly increasing fault currents [50]-[53]. The large fault current may be decayed quickly in some MMC topologies that use FB SMs to acquire the dc-fault blocking capability. Consequently, the FB-SM capacitor voltages may experience large variations. This impacts the restart operation if the dc fault is temporary. Specifically, FB SMs are mainly used in the MMC topologies with dc-fault blocking capability, because FB SMs can be inserted to charge regardless of the current polarity after the converter is blocked. This may give rise to overvoltage damage to SM capacitors, if the SM capacitance is selected only based upon normal operating conditions because variables such as the arm currents during a fault will be drastically different from those during normal operation. Therefore, considerations for SM capacitor sizing under faulted conditions are of importance for the topologies with dc-fault blocking capability. However, existing literature about SM capacitor sizing for novel MMCs with dc-fault blocking capability is inadequate [47]-[48], since no faulted conditions are taken into account. To enable this, the dc-fault behavior of a converter must be fully understood.

1.2.3.4 AC-fault ride-through capability

Apart from dc faults in HVDC transmission systems, ac faults such as line-to-ground, line-to-line, and three-phase short-circuit faults also occur. During ac faults, the synchronizing mechanism of the phase-locked loop (PLL) cannot work properly due to the appearance of double line frequency harmonic in the components transformed to a rotating reference frame [54]-[55]. Due to the incapability of the control system to eliminate the double line frequency harmonic, unbalanced three-phase currents appear that contain positive-, negative- and zero-sequence

components. As the negative- and zero-sequence currents flow through an ac network and converter transformers, the system may experience increased heating as well as core saturation in transformers. To achieve balanced phase currents under unbalanced ac faults, existing methods suggest individual control of the positive-, negative- and zero-sequence components [56]-[57]. These methods require extraction of positive-, negative-, and zero-sequence components of three-phase voltages and currents and complicated control loops. Parkhideh and Bhattacharya [54] proposed a method to control the converter under unbalanced ac grid conditions without sequence component extraction. However, this method is tightly dependent on the converter operation, and it is difficult to extend it to different topologies. Another approach without sequence component extraction is the individual phase control for the three-phase unbalanced system [58]-[59], in which each phase has its own PLL and control loops. To achieve balanced phase currents, these converter systems in [58] and [59] require additional active-filter converter to compensate the current in the faulted phases. Therefore, this thesis aims at improvements to independent phase control methods under unbalanced ac faults, such as removing active-filter converters while still achieving balanced phase currents.

1.2.3.5 Loss evaluation for MMCs

Due to the large number of SMs used in the construction of MMCs, it is essential that semiconductor losses incurred during conduction intervals and switching events be carefully assessed. These losses, which directly affect the efficiency of the converter system, depend not only on the type and configuration of converter SMs, but also on the firing pulse generation, SM capacitor voltage balancing and regulation, and system controls [40]-[41], [44]. Quantification of losses is necessary in order to devise control methods to lower the converter losses particularly in high-power applications. As stated in Section 1.2.2, MMCs with dc-fault blocking capability may

use additional semiconductors and require special provisions to maintain and regulate their SM capacitor voltages. It is, therefore, vital to quantify the operating losses of these converters to fully assess their merits. Use of mathematical or computer simulation models to assess converter losses is a common practice in high-power applications [60]-[70].

1.3 Objectives and methodologies

Based upon the above literature review, the described novel MMC topologies with dc-fault blocking capability are not well understood to date. Although some of these topologies are partially similar to the conventional HB- or FB-MMC, their system controls and performances may be remarkably different from the conventional MMCs [21]-[22], [25]. Therefore, these novel MMC topologies need to be systematically and thoroughly investigated in terms of design guidelines of the main components in topologies, system controls for normal and faulted conditions, dc-fault blocking mechanism, and system efficiency. This thesis aims at systematic and comprehensive investigations of one of these novel topologies, namely the HC-MMC topology (see Fig. 1.3 (e)), using theoretical, simulation, and experimental approaches. This topology not only offers dc-fault blocking ability but also is a topological extension of the conventional HB-MMC and may be considered as an option for expansion of already existing stations. The specific objectives and research methodologies of this thesis are listed as follows:

(1) Develop guidelines for the selection of the number of HB and FB SMs in the HC-MMC to improve the converter's output voltage quality. Although the main purpose of the FB SMs in the phase limb are to block dc faults, the voltages of the FB-SM capacitors need to be controlled and regulated during normal operation to enable proper dc-fault blocking. The FB stack is recommended to be used as only an active filter in normal operation to minimize its real power

delivery and hence reduce the requirement of FB-SM capacitor size. The total harmonic distortion (THD) of the voltage crafted by the HC-MMC with different numbers of HB and FB SMs will be analyzed, and guidelines for the selection of the number of HB and FB SMs will be developed to obtain better voltage quality (lower THD) than that crafted by conventional HB-MMC (i.e., only the main power stage of HC-MMC).

(2) Propose new control strategies and converter topology modifications to regulate the FB-SM capacitor voltages in the phase limb to achieve extended linear modulation range and reduced filtering burden for the FB stack. The thesis will analyze mechanisms to maintain the FB-SM capacitor voltages, and a new control strategy will be proposed and compared with existing methods to regulate the FB-SM capacitor voltages. To enhance the advantages of the proposed control strategy, a topology modification will be proposed. The proposed control strategy and the modified HC-MMC will be validated by both electromagnetic transient (EMT) simulations and experiments.

(3) Develop design guidelines to select proper SM capacitances for the original and proposed modified HC-MMCs based upon the stored energy of SM capacitors per power rating unit. Calculation of the theoretical operating point will be developed considering the converter's transformer and the strength of ac network. Based upon the operating point, the SM capacitor voltage ripple will be derived using electric charge variations, and the stored energy of SM capacitors per power rating unit will be derived for different operation modes (e.g., operation with or without circulating current suppression control (CCSC), and operation with or without 3rd harmonic injection). Simulation and experimental studies will be conducted to validate the analysis of the SM capacitor sizing for both the original and modified HC-MMCs.

(4) Investigate and quantitatively record the losses of the original and modified HC-MMCs to evaluate the relative merits in terms of system efficiency of the proposed FB-SM capacitor-voltage regulation methods. Additionally, loss comparisons will be made between the HC-MMCs and a conventional FB-MMC to evaluate the advantages of this novel topology over the conventional FB-MMC that has topological dc-fault blocking capability. A simulation-based loss calculation method will be used to obtain the losses of HC-MMCs and FB-MMC under different operating points. Comprehensive comparisons of the losses among HC-MMCs and FB-MMC will be made and analyzed in detail.

(5) Develop equivalent models to analyze the performance of both the original and modified HC-MMCs under a pole-to-pole fault and propose design considerations for SM capacitances to avoid adverse SM capacitor voltages. EMT simulations will be conducted to validate the equivalent models and SM capacitance design recommendations.

(6) Propose a control strategy to achieve fast recovery from ac faults with balanced phase currents under unbalanced ac faults. To validate the effectiveness of the proposed control strategy, EMT simulations of HC-MMC system under a phase-to-ground and a line-to-line fault will be conducted.

1.4 Outline of the thesis

The remainder of this thesis is organized as follows:

- In Chapter 2, detailed comparisons for voltage synthesis methods used for MMC operation are presented. Based upon one of the multicarrier-based PWM methods, the operating principles of HC-MMC are analyzed. Compared with the quality of voltage crafted by the

conventional HB-MMC (i.e., only the main power stage of HC-MMC), the selection of the number of HB and FB SMs in the HC-MMC is discussed with the aim of improving the quality of the voltage crafted by the HC-MMC. (Chapter 2's contributions have been published in Shi *et al.* [71])

- In Chapter 3, a new control strategy and a simple topology modification are proposed to regulate the FB-SM capacitor voltage in the FB stack. The proposed control strategy used for both the original and modified HC-MMCs is compared with existing methods and validated by EMT simulations and experiments. (Chapter 3's contributions have been published in Shi *et al.* [72])
- In Chapter 4, SM capacitor sizing of the original and modified HC-MMCs is analyzed under different operation modes. The stored energy of SM capacitors per power rating unit is comprehensively evaluated using extensive parametric studies.
- In Chapter 5, loss evaluation of the original and modified HC-MMCs with different FB-SM capacitor-voltage regulation methods is studied using a simulation-based approach. Comprehensive loss comparisons are made for HC-MMCs and conventional FB-MMC under various operating points and different switching frequencies. (Chapter 5's contributions have been published in Shi *et al.* [73])
- In Chapter 6, the dc-fault behavior of both the original and modified HC-MMCs is investigated. Equivalent models of the dc and ac circulating currents are derived individually under a pole-to-pole fault. In accordance with the equivalent models, additional considerations for SM capacitor sizing to avoid overvoltages for SM capacitors are studied

under a pole-to-pole fault. (Chapter 6's contributions have been partially published in Shi *et al.* [74])

- In Chapter 7, an independent phase-current control strategy is proposed for VSCs to ride through unbalanced ac faults with balanced three-phase currents. This control strategy is implemented for the original HC-MMC to validate its effectiveness. (Chapter 7's contributions have been published in Shi *et al.* [75])
- In Chapter 8, major conclusions and key contributions of this thesis and recommended avenues for future research are presented.
- In Appendix A, the 2nd harmonic currents in HC-MMCs operating with the 3rd harmonic injection are derived. The influence of 3rd harmonic injection on the 2nd harmonic current is evaluated. In addition, an algorithm to obtain SM capacitor voltage ripple of HB and FB SMs in the main power stage of the modified HC-MMC is developed and validated by EMT simulations.

Chapter 2

Operating Principles and Voltage Quality Analysis of HC-MMC

Contents

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Before analyzing the operating principles of an HC-MMC (see Fig. 1.3 (e)), typical modulation techniques for MMCs are summarized and compared. After the comparisons among different modulation methods, one proper modulation approach is selected to operate an HC-MMC for other investigations.

2.1 Voltage synthesis methods for MMCs

Voltage synthesis methods for MMCs fall into two general categories of low-frequency and high-frequency (also known as PWM) methods. To achieve relatively low harmonics, nearest-level control (NLC) is a widely-used low-frequency method [76]-[77] suitable for MMCs with an adequately large number of SMs, whereas PWM methods based upon high-frequency multiple carriers [78] (i.e., multicarrier-based PWM methods) are commonly employed in MMCs with a

small number of SMs. The following subsections (Sections 2.1.1 and 2.1.2) will analyze and compare the characteristics of the multicarrier-based PWM and NLC methods.

2.1.1 Multicarrier-based PWM techniques

Multicarrier-based PWM methods are generally composed of multiple triangular carrier waveforms at a high frequency, which are compared with a low-frequency reference waveform to synthesize the desired voltage levels. Based upon the arrangement of multiple carriers, the multicarrier-based PWM methods are mainly categorized into four types: phase-disposition PWM (PD-PWM), phase-opposition-disposition PWM (POD-PWM), alternative phase-opposition-disposition PWM (APOD-PWM) and the carrier phase-shifted PWM (CPS-PWM). Fig. 2.1 displays these four PWM methods. They are illustrated with four triangular carriers and a sinusoidal reference (v_{ref}) with its peak of $m = 0.9$ and fundamental period T_o , and v_{out} is the synthesized output voltage tracking the reference signal. The features of these four multicarrier-based PWM methods using an arbitrary number of carriers (N_{car}) are summarized as follows:

- (i) The PD-PWM method utilizes in-phase carriers with different offsets;
- (ii) The POD-PWM method employs in-phase carriers above or below zero, and these carriers are mirror-symmetrical through the zero axis;
- (iii) The APOD-PWM method uses neighboring carriers with a phase shift of 90° ;
- (iv) All the carriers used in the PD-, POD-, and APOD-PWM methods are evenly distributed within -1 to $+1$. Both the dc offset between two neighboring carriers and the peak-to-peak of one carrier are equal to $2/N_{\text{car}}$;
- (v) The CPS-PWM method uses neighboring carriers with a phase shift of $2\pi/N_{\text{car}}$, and each carrier varies from -1 to $+1$;

(vi) All these four PWM methods can generate up to $(N_{\text{car}}+1)$ voltage levels for the synthesized output voltage.

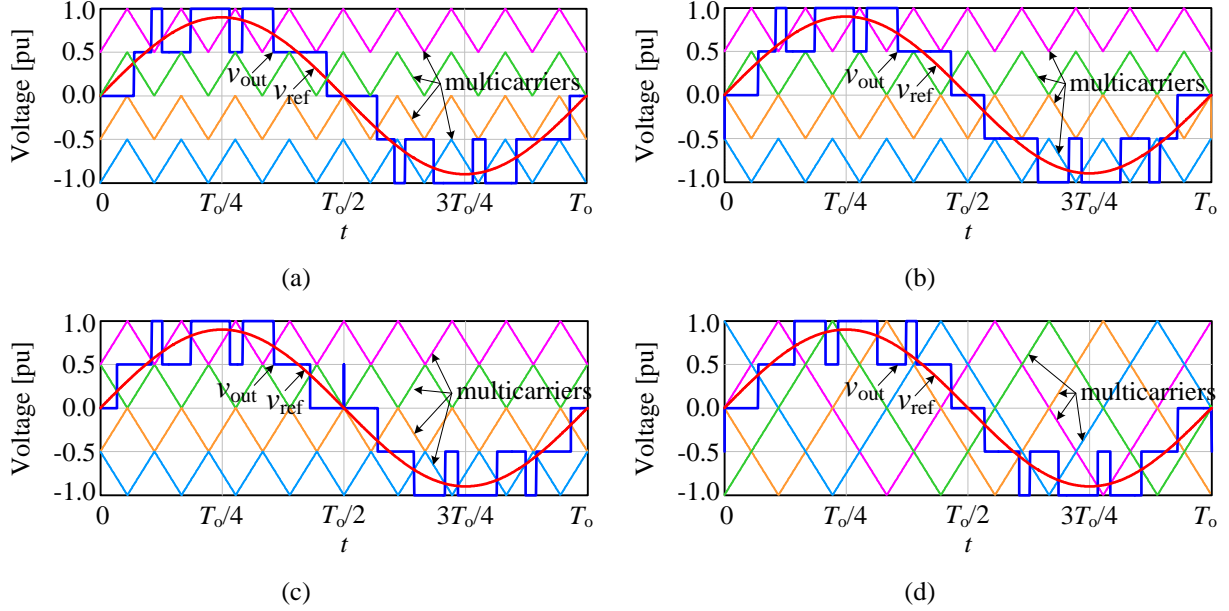


Fig. 2.1: Multicarrier-based PWM methods using 4 carriers and $m = 0.9$
(a) PD-PWM; (b) POD-PWM; (c) APOD-PWM; (d) CPS-PWM.

To evaluate the quality of the voltages synthesized by these four multicarrier-based PWM methods, the harmonic spectra of the synthesized voltages obtained by mathematical fast Fourier transform (FFT) are plotted in Fig. 2.2. It is observed that the THD values of the synthesized voltages are very close, i.e., 31.29%, 32.23%, 31.23%, and 31.83% for the PD-, POD-, APOD- and CPS-PWM methods, respectively. Compared with the carrier frequencies used in these four PWM methods ($9f_o$ in the PD-, POD- and APOD-PWM methods, and $9f_o/4$ in the CPS-PWM method), the dominant harmonic frequencies in the synthesized voltages obtained by the PD-, POD- and APOD-PWM methods are distributed around their carrier frequency ($9f_o$), whereas CPS-PWM method synthesizes the voltage with dominant harmonic frequencies distributed around N_{car} ($N_{\text{car}} = 4$ in the example shown in Fig. 2.1) times of its carrier frequency. Therefore, if the carrier frequency used in the CPS-PWM method is chosen to be $1/N_{\text{car}}$ times of those used in the PD-,

POD- and APOD-PWM methods, these four multicarrier-based PWM methods can synthesize a voltage with nearly identical THD.

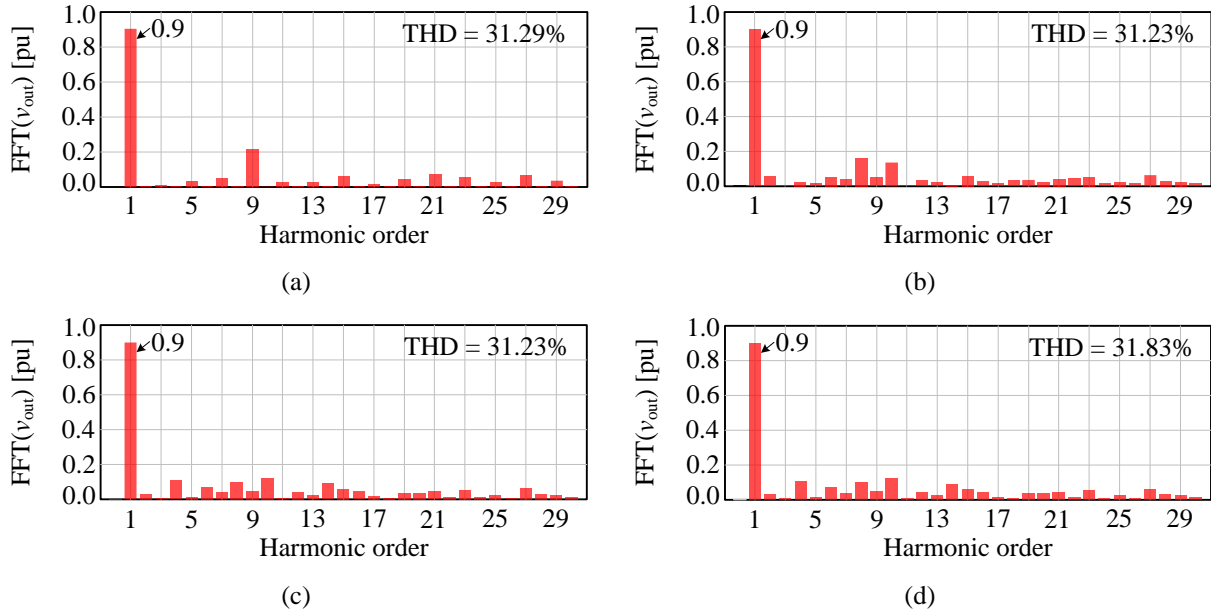


Fig. 2.2: Harmonic spectra of the synthesized voltages under different multicarrier-based PWM methods using 4 carriers and $m = 0.9$

(a) PD-PWM; (b) POD-PWM; (c) APOD-PWM; (d) CPS-PWM.

To parametrically evaluate the characteristics of these four multicarrier-based PWM methods, the relative errors of the fundamental components ($(V_{1st} - m)/m$) and the THD of the synthesized voltages are analyzed as a function of the carrier frequency. The results are shown in Fig. 2.3, where V_{1st} is the amplitude of the fundamental component of the synthesized voltage, the modulation index (m) indicates the peak of the reference, and f_o and f_{car} are the fundamental and carrier frequencies, respectively. It is observed that with higher carrier frequencies ($\geq 9f_o$), the fundamental components of the synthesized voltages are much closer to the desired values for all these PWM methods, whereas THD variations of the synthesized voltages are within $\pm 3\%$. Therefore, all these PWM methods have similar characteristics in terms of their ability to regulate the fundamental component and THD of the synthesized voltages.

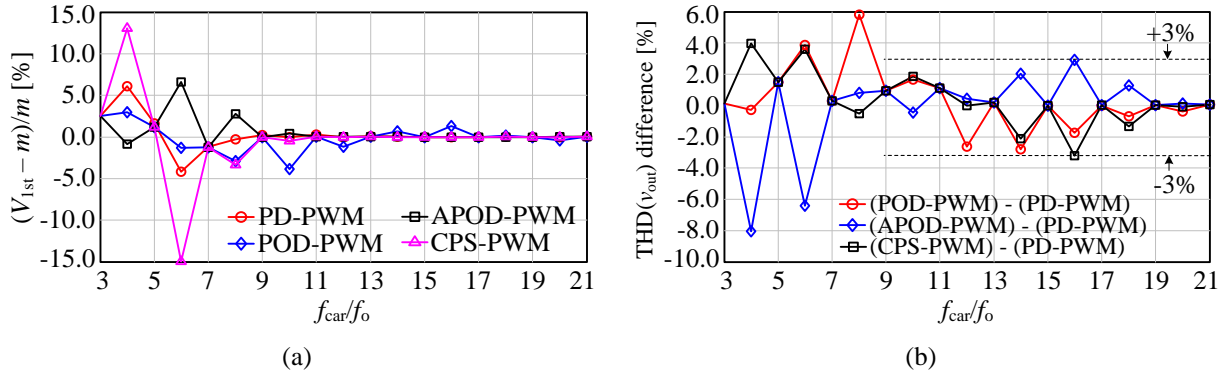


Fig. 2.3: Property comparisons among different multicarrier-based PWM methods using 4 carriers and $m = 0.9$
 (a) relative error of the fundamental component; (b) THD.

2.1.2 NLC method

The NLC method is widely-used for MMCs and the synthesized voltage levels are tightly related to the number of SMs. Fig. 2.4 illustrates the synthesized voltage (v_{out}) and its harmonic spectrum from the NLC method with 10 SMs, whereas Fig. 2.5 shows the relative errors of the fundamental component, $(V_{1st} - m)/m$, and THD with respect to the number of SMs. As observed from Fig. 2.5, the number of SMs must be at least 13 for the relative error of the fundamental component to be less than 1%, and the number of SMs must be at least 16 to obtain the synthesized voltage with THD less than 5%. This indicates that the NLC method is suitable for MMCs with a large number of SMs.

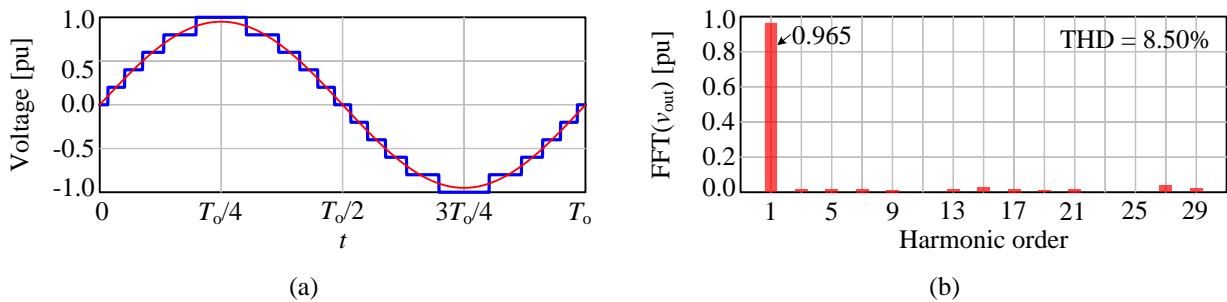


Fig. 2.4: NLC method with $m = 0.95$ and 10 SMs
 (a) normalized synthesized voltage waveform; (b) harmonic spectrum.

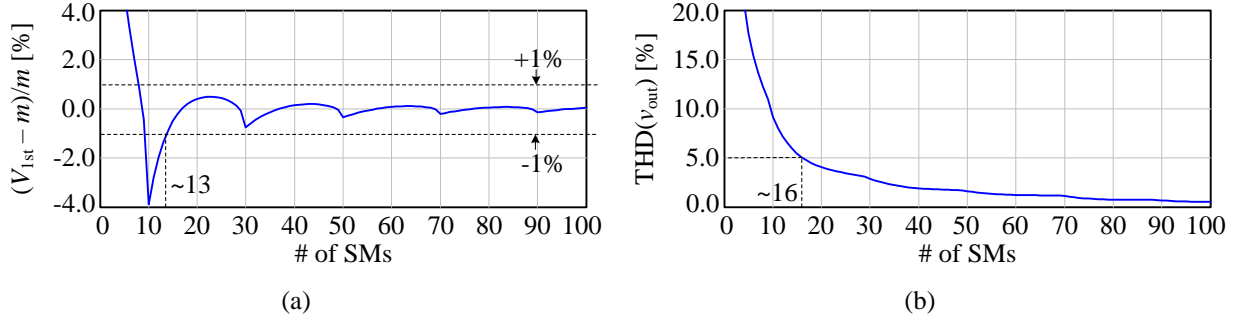


Fig. 2.5: Properties of the NLC method with $m = 0.9$

(a) relative error of the fundamental component; (b) THD of the synthesized waveform.

Since these four investigated multicarrier-based PWM techniques have essentially similar characteristics, only the PD-PWM method is chosen for the remaining analyses of system control, loss evaluation and component design of the HC-MMC in this thesis. Additionally, the NLC method for a large enough number of SMs has similar properties (e.g., THD and ability to regulate the fundamental component) to those of the multicarrier-based PWM methods and as such will not be pursued.

2.2 Operating principles of HC-MMC

A single-phase schematic diagram of the HC-MMC is shown in Fig. 2.6 (a). The converter consists of two building blocks: the main power stage, which is similar to a conventional HB-MMC, and the phase limb comprised of FB SMs. The HB SMs in the main power stage have a nominal voltage of $V_{chb} = V_{dc}/N_h$, where V_{dc} is the dc-link voltage and N_h is the number of SMs (excluding redundancy) per arm. To prevent the ac system's contribution to a dc fault, FB-SM capacitors must maintain a (minimum) nominal voltage of $V_{ctb} = (V_{dc}/2)/N_f$ [25], where N_f is the number of FB SMs (excluding redundancy) per phase. As seen from Fig. 1.1 (a) and (b), the HB SMs can produce two voltage levels: 0 and V_{chb} , whereas the FB SMs can produce three voltage levels: 0 and $\pm V_{ctb}$.

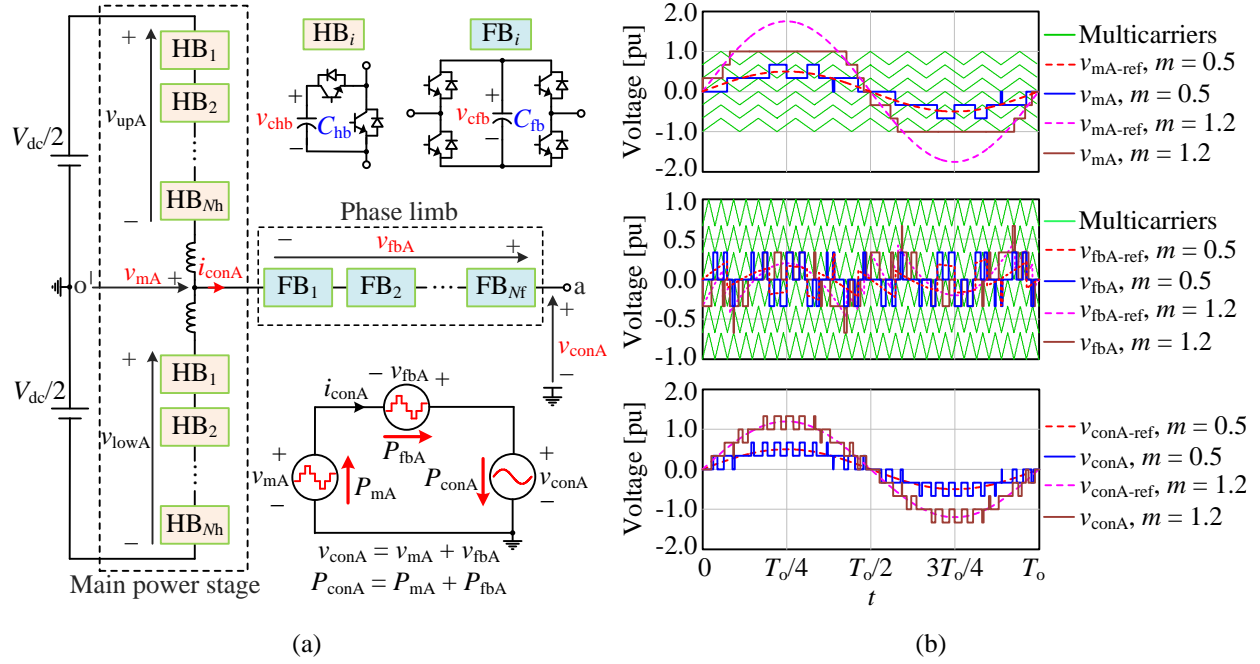


Fig. 2.6: Single-phase HC-MMC topology and basic waveforms

(a) schematic diagram of the single-phase HC-MMC circuit; (b) basic waveforms of the HC-MMC operating with PD-PWM.

The basic operating waveforms for the HC-MMC with $N_h = 6$ and $N_f = 3$ using PD-PWM are shown in Fig. 2.6 (b), where $v_{conA-ref}$, v_{mA-ref} , and $v_{fbA-ref}$ are the references for the converter's output phase voltage, the voltage crafted by the main power stage, and the voltage across the FB stack of phase A, respectively. The main power stage is primarily responsible for crafting a controlled voltage at its terminals (denoted with subscript 'm' in Fig. 2.6 (a)) and for transmitting power between the dc and ac sides. The FB stack is mainly used to block the phase current and isolate the ac and faulted dc sides during a dc fault. To achieve dc-fault blocking capability, the FB stack must be in use in normal operation to control and regulate the FB-SM capacitor voltages. Since the main power stage is able to deliver all the required power to the converter's output, the FB stack is operated as an active filter during normal operation to minimize its real power delivery and hence reduce the requirement of FB-SM capacitor size. Therefore, the main power stage is suggested to operate with low-frequency PD-PWM to reduce losses, and the FB stack operates

with a relatively high-frequency PD-PWM to improve the output voltage quality. Fig. 2.6 (b) illustrates the operating waveforms with $9f_o$ and $27f_o$ carrier frequencies for the main power stage and the FB stack in the phase limb, respectively. It is noticed from Fig. 2.6 (b) that the actual voltage waveform of v_{mA} is unable to track its reference (v_{mA-ref}) when the instantaneous value of v_{mA-ref} becomes larger than 1.0. However, the terminal output phase voltage (v_{conA}) is sinusoidal, taking advantage of the FB stack with a voltage reference of $v_{fbA-ref} = v_{conA-ref} - v_{mA}$. Under this case (i.e., $m > 1.0$), there may be a mismatch between the fundamental component in the voltage crafted by the main power stage and that in the converter's output voltage. As seen from the power flow diagram shown in Fig. 2.6 (a), the FB stack may be required to provide a portion of the real power transmitted to the converter output. This gives rise to FB-SM capacitor voltage drifts if no control supervision is provided for the FB stack. The mechanism and control schemes to regulate the FB-SM capacitor voltages will be analyzed in detail in Sections 3.1 and 3.2, respectively.

2.3 Design considerations for the number of SMs in HC-MMC

To investigate the quality of the output phase voltage crafted by the HC-MMC, its THD with different number of SMs are analyzed under the PD-PWM method with $9f_o$ and $27f_o$ carrier frequencies for the main power stage and the FB stack, respectively. If $N_f = 0$, i.e., there is no cascaded FB SMs connected to the ac side and HC-MMC is degraded to a regular HB-MMC, the main power stage operates under the PD-PWM with $27f_o$ carrier frequency, so that the output phase voltage contains the same dominant harmonics as that crafted by normal HC-MMC. If $N_h = 1$, the voltage crafted by the main power stage is a square waveform to avoid over-modulation in the operation of the FB stack. Fig. 2.7 shows the THD results of the output phase voltage crafted by

HC-MMC with a modulation index of 1.0, where the curve indicating $N_f = 0$ in Fig. 2.7 (a) is corresponding to the THD of the voltage crafted by an HB-MMC with $27f_0$ PD-PWM.

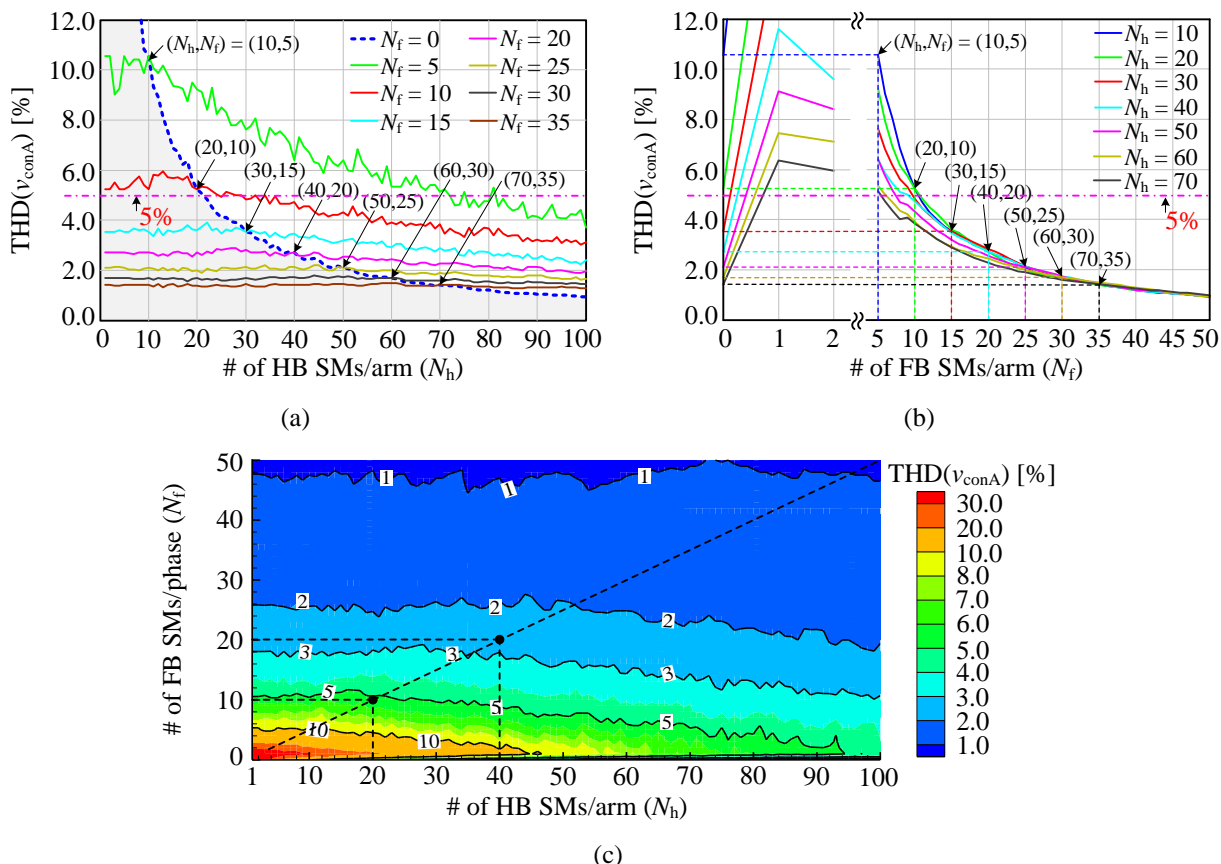


Fig. 2.7: THD of the phase voltage with $m = 1.0$ under PD-PWM method with $9f_0$ and $27f_0$ carrier frequencies respectively for the main power stage and the FB stack

(a) THD of the phase voltage as a function of the number of HB SMs per arm; (b) THD of the phase voltage as a function of the number of FB SMs per phase; (c) contour plot of the THD with different number of HB and FB SMs.

As seen from Fig. 2.7 (a) and taking an example of $N_f = 10$ for the HC-MMC, the THD of the voltage crafted by either only the main power stage (i.e., $N_f = 0$ in Fig. 2.7 (a)) or the HC-MMC decreases as N_h increases; the THD of the voltage crafted by the HC-MMC is lower than that crafted by only the main power stage with $N_h < 20$, and both THDs are approximately equal until $N_h = 20$. As discussed in Section 2.2, each HB- and FB-SM capacitor operates with the average voltage of V_{dc}/N_h and $V_{dc}/(2N_f)$ in normal conditions, respectively. Therefore, compared with the

THD curve for $N_f = 0$, the number of FB SMs must satisfy $N_f \geq N_h/2$ (or $V_{c_{fb}} \leq V_{c_{hb}}$) to ensure that the THD of the phase voltage is lower than that crafted by an HB-MMC (i.e., only the main power stage of HC-MMC). As seen from Fig. 2.7 (b) and taking an example of $N_h = 30$ for the HC-MMC, the THD of the voltage crafted by the HC-MMC reduces as N_f increases, and it is approximately equal to that crafted by only the main power stage (i.e., $N_f = 0$ in Fig. 2.7 (b)) until N_f is increased to 15. Because the voltage across all FB-SM capacitors in the phase limb is at least equal to $V_{dc}/2$ (hence achieving the dc-fault blocking capability), the FB-SM capacitor has a larger voltage with a smaller N_f . Comparing the cases of $N_f = 1$ and $N_f = 15$ under $N_h = 30$, the average voltage across the FB-SM capacitor must be at least equal to $V_{dc}/2$ with $N_f = 1$ and $V_{dc}/30$ with $N_f = 15$. The smaller the FB-SM capacitor voltage, the better the output phase voltage quality can be due to the smaller stair heights to craft the sinusoidal waveform. In addition, Fig. 2.7 (b) shows that the number of FB SMs is the dominant factor influencing the THD of the phase voltage when $N_h \geq 20$.

As seen from the above analysis based upon Fig. 2.7 (a) and (b), to improve the quality of the voltage crafted by only the main power stage (i.e., an HB-MMC), the relationship between the number of HB SMs per arm and the number of FB SMs per phase limb must satisfy $N_f \geq N_h/2$ (or $V_{c_{fb}} \leq V_{c_{hb}}$). According to the IEEE 519 guidelines, the THD of the ac-side voltage in general systems needs to be less than 5%; special applications including hospitals and airports require less than 3% THD in the ac-side voltage; and the THD of the ac-side voltage in dedicated systems for converter loads can be up to 10%. Fig. 2.7 (c) shows the contour graph of the THD of the converter's phase voltage with respect to N_h and N_f . Considering the THD of the ac-side voltage less than 5% and in conjunction with the selection guideline of the number of HB and FB SMs, the number of HB SMs per arm must be larger than 20, and the number of FB SMs per phase limb must be at least 10 (see Fig. 2.7 (c)). Apart from the THD requirement, the selection of the number

of SMs for a certain system also depends on other factors, such as the performance of the selected semiconductors and the dc-link voltage. With these considerations, practical MMCs in high-voltage applications tend to have much larger number of SMs, at times reaching hundreds per arm.

2.4 Summary and key contributions

The commonly-used multicarrier-based PWM and NLC methods for MMCs were analyzed and comprehensively compared. It was shown that the four multicarrier-based PWM methods considered have similar properties in terms of the accuracy of fundamental component and quality of the synthesized voltage. The basic operating principles of HC-MMC were presented based upon PD-PWM. Furthermore, the influence of using different numbers of HB and FB SMs on the THD of the converter's output voltage was studied, and the guideline for selecting the number of HB and FB SMs was developed. It was shown that the number of FB SMs in the phase limb needs to be selected greater than or equal to half of the number of HB SMs per arm in the main power stage to improve the THD of the voltage crafted by only the main power stage (i.e., an HB-MMC).

Chapter 3

Capacitor-Voltage Regulation and Linear-Range

Extension in HC-MMC

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During normal operation, the HB- and FB-SM capacitor voltages in HC-MMC must be well balanced and maintained tightly around their nominal values. To balance the SM capacitor voltages, the conventional sorting and rotating method [33] is implemented for the SMs in each arm and phase limb. For the HB SMs within the main power stage, the total number of inserted SMs from the upper and lower arms in the same phase is guaranteed to be approximately N_h SMs at every instant of time. Based upon Kirchhoff's voltage law (KVL) to obtain $V_{dc} = V_{upA} + V_{lowA} = N_h \cdot V_{chb}$, it is noticed that the HB-SM capacitor voltages can be maintained at their nominal value of V_{dc}/N_h with only the sorting and rotating method. There is, however, no such inherent

mechanism to ensure that the average FB-SM capacitor voltages remain at their desired nominal value of $V_{dc}/(2N_f)$. The sorting and rotating method can only ensure the FB-SM capacitor voltages are balanced but it is unable to maintain the FB-SM capacitor voltage values. Therefore, a control system is required to regulate the average FB-SM capacitor voltages.

The following subsection provides an analysis of the average power delivered by the FB SMs under idealized conditions. This analysis reveals the underlying conditions of power balance between the main power stage and the converter's output for the FB-SM capacitor-voltage regulation. Voltage regulation methods are then developed based upon the conclusions of the power balance analysis.

3.1 Average power analysis

To simplify the following analysis of average power, the system's losses are ignored, and it is assumed that the number of SMs in each stage is sufficiently large so that the converter output voltage is essentially sinusoidal. Based upon all the voltage and current directions labelled in Fig. 2.6 (a), the output phase voltage, v_{conA} , and phase current, i_{conA} , are expressed as follows:

$$\begin{aligned} v_{conA}(t) &= m \frac{V_{dc}}{2} \sin(\omega_o t) \\ i_{conA}(t) &= I_m \sin(\omega_o t + \varphi) \quad \varphi \in [-\pi/2, \pi/2] \end{aligned} \quad (3.1)$$

where m is the converter's modulation index, I_m is the peak of phase current, φ is the phase difference between the phase current and phase voltage, and ω_o is the fundamental angular frequency. Note that $\cos(\varphi) \geq 0$ for inverter-mode operation, and $\cos(\varphi) < 0$ for rectifier-mode operation. The average power absorbed by the converter's output is readily obtained as follows:

$$\begin{aligned}
P_{\text{conA}}(m) &= \frac{1}{T_o} \int_0^{T_o} v_{\text{conA}}(t) \cdot i_{\text{conA}}(t) dt = \frac{1}{T_o} \int_0^{T_o} m \frac{V_{\text{dc}}}{2} \sin(\omega_o t) \cdot I_m \sin(\omega_o t + \varphi) dt \\
&= \frac{m V_{\text{dc}} I_m \cos(\varphi)}{4}
\end{aligned} \tag{3.2}$$

The average power delivered by the main power stage depends on the voltage, v_{mA} , and the phase current, i_{conA} , at its terminals. Since the largest voltage crafted by the main power stage is $V_{\text{dc}}/2$, voltage v_{mA} is purely sinusoidal only when $m \leq 1.0$ and will be clipped at $V_{\text{dc}}/2$ when $m > 1.0$. Therefore, two distinct cases are identified to calculate the average power delivered by the main power stage.

Case 1: $m \leq 1.0$

For this case $v_{\text{mA}}(t) = v_{\text{conA}}(t)$ and as such $v_{\text{fbA}}(t) = v_{\text{conA}}(t) - v_{\text{mA}}(t) = 0$; therefore, the average power delivered by the main power stage is equal to the power absorbed by the converter's output:

$$P_{\text{mA}}(m) = P_{\text{conA}}(m) = \frac{m V_{\text{dc}} I_m \cos(\varphi)}{4} \tag{3.3}$$

According to the power flow diagram shown in Fig. 2.6 (a), the average power delivered by the FB stack is $P_{\text{fbA}}(m) = P_{\text{conA}}(m) - P_{\text{mA}}(m) = 0$, which means that for $m \leq 1.0$ the FB stack will not exchange any net real power with the converter's output and hence will not experience any SM capacitor voltage drift in idealized conditions. However, real converter systems are lossy and physical capacitors have leakage currents, resulting in SM capacitor voltage drop if the small losses in the FB stack are not compensated.

Case 2: $m > 1.0$

For this case, the voltage crafted by the main power stage will be clipped as shown in Fig. 3.1 (a) with $m = 1.2$. Therefore,

$$v_{mA}(t) = \frac{V_{dc}}{2} \cdot \begin{cases} +1 & \text{if } \omega_o t \in [\alpha, \pi - \alpha] \\ -1 & \text{if } \omega_o t \in [\pi + \alpha, 2\pi - \alpha] \\ m \sin(\omega_o t) & \text{otherwise} \end{cases} \quad (3.4)$$

where $\alpha = \sin^{-1}(1/m)$. The resulting voltage across the FB stack in the phase limb is shown below.

$$v_{fbA}(t) = v_{conA}(t) - v_{mA}(t) = \frac{V_{dc}}{2} \cdot \begin{cases} m \sin(\omega_o t) - 1 & \text{if } \omega_o t \in [\alpha, \pi - \alpha] \\ m \sin(\omega_o t) + 1 & \text{if } \omega_o t \in [\pi + \alpha, 2\pi - \alpha] \\ 0 & \text{otherwise} \end{cases} \quad (3.5)$$

In this case, the average power delivered by the main power stage and the FB stack are respectively expressed as follows:

$$\begin{aligned} P_{mA}(m) &= \frac{1}{T_o} \int_0^{T_o} v_{mA}(t) \cdot i_{conA}(t) dt \\ &= \frac{1}{2\pi} \left[\int_0^\alpha m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta + \int_\alpha^{\pi-\alpha} \frac{V_{dc}}{2} \cdot I_m \sin(\theta + \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi-\alpha}^{\pi+\alpha} m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi+\alpha}^{2\pi-\alpha} -\frac{V_{dc}}{2} \cdot I_m \sin(\theta + \varphi) d\theta + \int_{2\pi-\alpha}^{2\pi} m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta \right] \\ &= \frac{V_{dc} I_m \cos(\varphi)}{2\pi} \left(\frac{\sqrt{m^2 - 1}}{m} + m \sin^{-1}\left(\frac{1}{m}\right) \right) \end{aligned} \quad (3.6)$$

$$P_{fbA}(m) = P_{conA}(m) - P_{mA}(m) = \frac{V_{dc} I_m \cos(\varphi)}{2\pi} \left(\frac{\pi m}{2} - \frac{\sqrt{m^2 - 1}}{m} - m \sin^{-1}\left(\frac{1}{m}\right) \right) \quad (3.7)$$

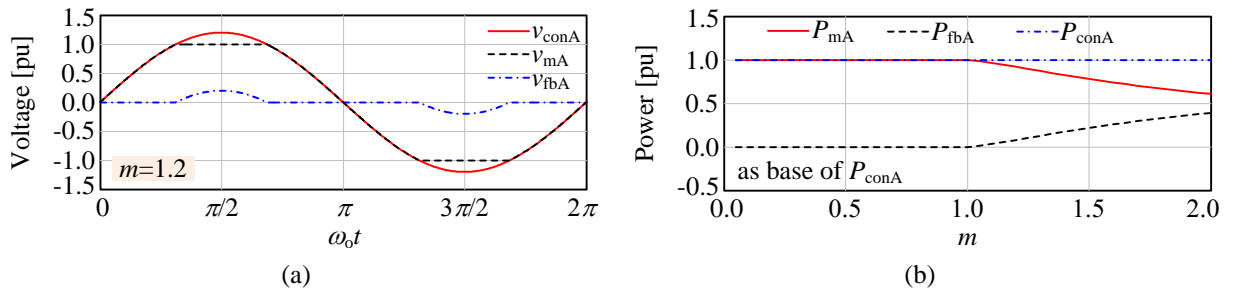


Fig. 3.1: HC-MMC operation under ideal conditions

(a) voltage waveforms (v_{mA} , v_{fbA} and v_{conA}) with $m = 1.2$; (b) average power (P_{mA} , P_{fbA} and P_{conA}) as a function of m .

According to the above analysis, Fig. 3.1 (b) shows the variations of real power for the main power stage and the FB stack (both normalized by the power absorbed by the converter's output, $P_{\text{conA}}(m)$) as a function of modulation index. For $m > 1.0$ the FB stack delivers real power to the converter's output in inverter-mode operation ($\cos(\varphi) > 0$), and absorbs real power in rectifier-mode operation ($\cos(\varphi) < 0$), resulting in the FB-SM capacitor voltage drift.

To conclude, in idealized conditions without considering system losses, if any power imbalance exists between the main power stage and the converter's output, such as in transients or start-up operation, the FB-SM capacitor voltages in the phase limb cannot be maintained at their required value. Therefore, control supervision on the FB-SM capacitor voltages must be exercised to achieve proper operation of HC-MMC.

3.2 FB-SM capacitor-voltage regulation in the phase limb

As seen from the above analysis, the main reason for FB-SM voltage drift is that the power delivered by the main power stage does not match the power absorbed by the converter's output. Since the operating principle of HC-MMC in rectifier mode is similar to that in inverter mode, the inverter-mode operation is considered to elaborate the control strategies to regulate the FB-SM capacitor voltages in the following subsections. If the HC-MMC is in rectifier-mode operation, a simple action, i.e., using $(V_{\text{cfbA-avg}} - V_{\text{cfb-ref}})$ as the control error in the control methods shown in Fig. 3.2 (b) and (d), is taken to obtain effective control to regulate the FB-SM capacitor voltages in the phase limb, where $V_{\text{cfb-ref}}$ and $V_{\text{cfbA-avg}}$ are the voltage reference and the average FB-SM capacitor voltage in the phase-A limb, respectively.

A method for FB-SM capacitor-voltage regulation using a trapezoidal PWM method is given in [34] to obtain zero-net energy exchange by the FB stack, which is briefly described in Section

3.2.1. However, this method is commonly known to suffer from the low-frequency harmonics embedded in its trapezoidal reference [79], which yield a large THD (see Section 3.3) and hence increase the filtering burden for the FB stack. In view of this shortcoming, a new voltage regulation method is proposed in Section 3.2.2 to extend the linear modulation range and reduce the filtering burden for the FB stack. To further extend the advantages of the proposed control strategy, a topology modification is proposed in Section 3.2.3, resulting in a new HC-MMC topology named mixed-SM HC-MMC in this thesis. The proposed mixed-SM HC-MMC brings additional benefits of relaxing the requirements for SM capacitor sizing, lowering converter losses, and promptly decaying arm currents during dc faults, which will be proven and analyzed in Sections 4.3.2, 5.3.2, and 6.1.2, respectively.

3.2.1 Trapezoidal PWM with variable slope

Ghat *et al.* [34] proposed a method to regulate the FB-SM capacitor voltages in the phase limb using a slope-adjustable trapezoidal PWM for the main power stage [34]. Fig. 3.2 (a) and (b) respectively show the operating waveforms and implementation of the control strategy for inverter-mode operation, where $V_{\text{cfb-ref}}$ and $V_{\text{cfbA-avg}}$ are the voltage reference and the average capacitor voltages of all FB SMs in phase-A limb, respectively. The detailed derivations based on the zero-net energy exchange by the FB stack are shown in [34]. However, [34] only analyzes the relationship between the slope of the trapezoidal reference, k_{trap} , and its equivalent fundamental component when $k_{\text{trap}} > 2\omega_0/\pi$ (i.e., $m > 8/\pi^2$), for which the reference is trapezoidal. Note that for $k_{\text{trap}} < 2\omega_0/\pi$ (i.e., $m < 8/\pi^2$), the reference degrades to a triangular waveform with its peak below unity (see waveforms for $m = 0.7$ in Fig. 3.2 (a)). The expressions for the trapezoidal reference for the two cases are shown as follows:

$$v_{mA}(t) = \begin{cases} k_{\text{trap}} t, & t \in [0, T_o/4] \cup [3T_o/4, T_o] \\ -k_{\text{trap}} (t - T_o/4), & t \in [T_o/4, 3T_o/4] \end{cases} \quad \text{if } k_{\text{trap}} \leq \frac{2\omega_o}{\pi}$$

$$v_{mA}(t) = \begin{cases} k_{\text{trap}} t, & t \in [0, 1/k_{\text{trap}}] \cup [T_o - 1/k_{\text{trap}}, T_o] \\ -k_{\text{trap}} (t - T_o/2 + 1/k_{\text{trap}}), & t \in [T_o/2 - 1/k_{\text{trap}}, T_o/2 + 1/k_{\text{trap}}] \\ 1, & t \in [1/k_{\text{trap}}, T_o/2 - 1/k_{\text{trap}}] \\ -1, & t \in [T_o/2 + 1/k_{\text{trap}}, T_o - 1/k_{\text{trap}}] \end{cases} \quad \text{if } k_{\text{trap}} > \frac{2\omega_o}{\pi} \quad (3.8)$$

According to the detailed analysis of this method in [34], the relationship between the converter modulation index, m , and the slope of the trapezoidal waveform, k_{trap} , is expressed as:

$$m = \begin{cases} \frac{8k_t}{\pi^2} & \text{if } 0 < k_t \leq 1 \\ \frac{8k_t}{\pi^2} \sin\left(\frac{\pi}{2k_t}\right) & \text{if } k_t > 1 \end{cases} \quad (3.9)$$

where $k_t = k_{\text{trap}}/(2\omega_o/\pi)$. It is noticed that the linear-regulation range of the trapezoidal PWM method is up to $8/\pi^2$, and the relationship between the control variable (k_t) and the modulation index is highly nonlinear for $m > 8/\pi^2$ (see Fig. 3.3 (a)).

3.2.2 Modified sinusoidal PWM with linear-range extension

As seen from Fig. 3.1 (b), for $m > 1.0$ the main power stage does not deliver all the average power required by converter's output. To resolve this issue and also to achieve low harmonics in the voltage crafted by the main power stage, the voltage reference for the main power stage is selected to be in phase with that of the converter's output voltage, but with a different modulation index from that of the converter's output. Based upon this idea, Fig. 3.2 (c) and (d) respectively show the operating waveforms and control implementation for inverter-mode operation, where Δm is the difference between the modulation indices of the main power stage and the converter's output, and m_{mpk} ($= 1.0$ for the original HC-MMC) corresponds to the peak value of the voltage

crafted by the main power stage normalized by $V_{dc}/2$. As seen from Fig. 3.2 (c), the voltage reference and the actual voltage of the main power stage (v_{mA-ref} and v_{mA}) are sinusoidal when $m < 1.0$. However, v_{mA} is partially clipped at $V_{dc}/2$ when $m > 1.0$, although v_{mA-ref} is still sinusoidal. As such, the proposed method is named modified sinusoidal PWM method.

For $m \leq 1.0$, the average power delivered by the FB stack is zero and thereby $m_{new} = m$ and $\Delta m = 0$ in theory. Considering system losses in practice, Δm will not be exactly zero but a small value close to zero. For $m > 1.0$, the average power delivered by the main power stage (in (3.6)) must be recalculated using m_{new} to replace m . The power delivered by the FB stack, which must be equal to zero to maintain the FB-SM capacitor voltages in steady-state operation, is as follows:

$$\begin{aligned}
P_{fbA} &= P_{conA}(m) - P_{mA}(m_{new}) = 0 \\
\Rightarrow \frac{mV_{dc}I_m \cos(\varphi)}{4} - \frac{V_{dc}I_m \cos(\varphi)}{2\pi} \left(\frac{\sqrt{m_{new}^2 - 1}}{m_{new}} + m_{new} \sin^{-1}\left(\frac{1}{m_{new}}\right) \right) &= 0 \quad (3.10) \\
\Rightarrow m &= \frac{2}{\pi} \left[\frac{\sqrt{m_{new}^2 - 1}}{m_{new}} + m_{new} \sin^{-1}\left(\frac{1}{m_{new}}\right) \right] \quad \text{if } m > 1
\end{aligned}$$

Therefore, this proposed method extends the linear-regulation range to 1.0. Within the nonlinear-regulation range, i.e., $m > 1.0$, the expression in (3.10) readily demonstrates how to adjust the modulation index for the main power stage, m_{new} , such that the power exchange with the FB stack is zero, and thus the FB-SM capacitor voltages remain regulated at the desired value. Since the modulation index of the converter's output is feedforwarded to create m_{new} for the main power stage (see Fig. 3.2 (d)), the control system can judiciously adjust Δm to ensure that the real power required for the converter's output is entirely provided by the main power stage. In general, 3rd harmonic injection can be used for the sinusoidal PWM method to extend the linear modulation index range [80]. Fig. 3.2 (d) also shows the proposed control system including the 3rd harmonic

injection, where k_{3rd} denotes the proportion of the 3rd harmonic added to the fundamental component. The value of k_{3rd} is typically set to 1/6 in order to extend the linear range up to 1.15 [80]. It is noticed that the 3rd harmonic injection does not impact the operation of the FB stack, because the same amount of the 3rd harmonic is injected to the voltage references for both the main power stage and the converter's output. Thereby, compared with the trapezoidal PWM method, the proposed modified sinusoidal PWM method is capable of injecting the 3rd harmonic into the reference voltages to further extend the linear-regulation range.

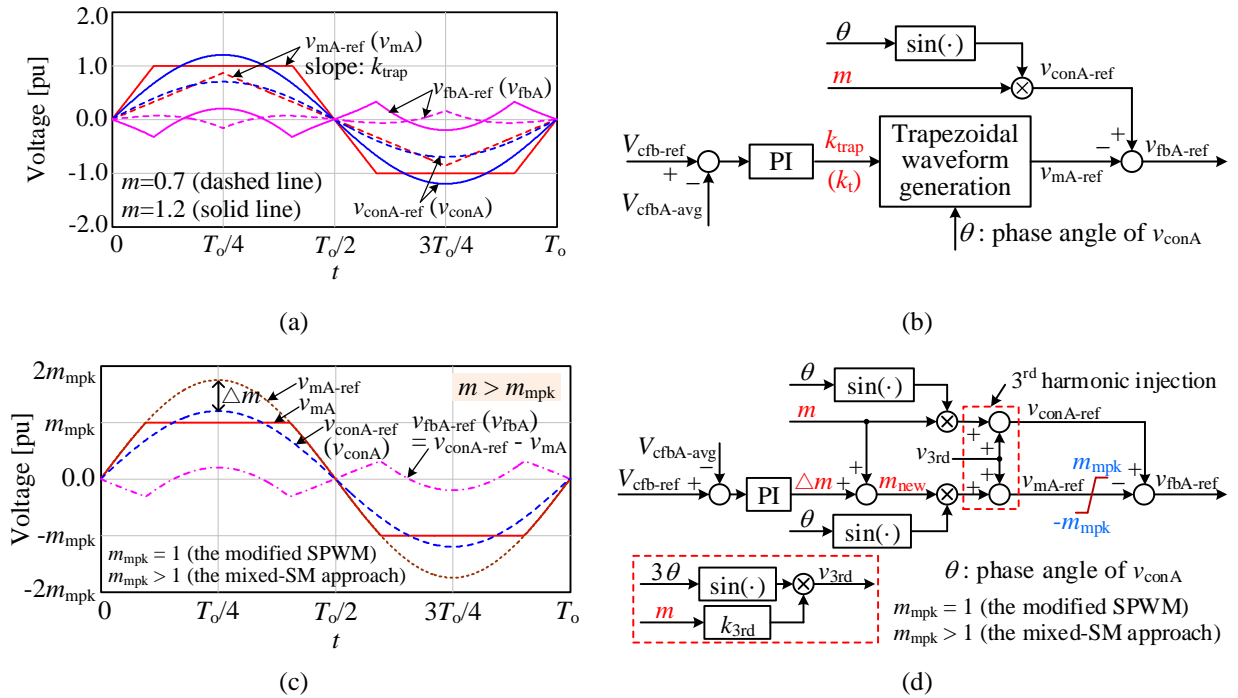


Fig. 3.2: Trapezoidal and modified sinusoidal PWM methods to regulate the FB-SM capacitor voltages in the phase limb of HC-MMC in inverter-mode operation

(a) reference waveforms under trapezoidal PWM; (b) voltage regulator with the trapezoidal PWM; (c) reference waveforms under the modified sinusoidal PWM; (d) voltage regulator with the modified sinusoidal PWM.

3.2.3 Mixed-SM approach with linear-range extension

To further extend the linear modulation range of the HC-MMC beyond the modulation index of 1.0, a topology modification is proposed for the original HC-MMC, i.e., adding FB SMs to the

main power stage and in series with the existing HB SMs in each arm, resulting in a mixed-SM HC-MMC. The linear range is extended because FB SMs can insert negative capacitor voltages whereas HB SMs cannot. The capacitance (denoted as C_{fm}) and capacitor voltage (denoted as V_{cfm}) of these FB SMs used in the main power stage are the same as those for the existing HB SMs, i.e., $C_{fm} = C_{hb}$ and $V_{cfm} = V_{chb} = V_{dc}/N_h$. Assuming that the number of FB SMs added to the main power stage per arm is N_{fm} , the minimum voltage crafted by the upper arm in the main power stage will be $v_{upA} = -N_{fm} \cdot V_{cfm} = -N_{fm} \cdot V_{dc}/N_h$ if all FB SMs in the upper arm are inserted with negative capacitor voltages and all HB SMs are bypassed. Thus, the peak voltage of the main power stage voltage is $V_{dc}/2 - v_{upA} = (1+2N_{fm}/N_h) \cdot V_{dc}/2$, resulting in an improved main power stage clipping level of $m_{mpk} = 1+2N_{fm}/N_h$. Therefore, based upon the proposed modified sinusoidal PWM method, the operating waveform and control implementation for the mixed-SM HC-MMC in inverter-mode operation are shown in Fig. 3.2 (c) and (d), respectively, with $m_{mpk} = (1+2N_{fm}/N_h)$.

Table 3.1 shows the voltage levels of the mixed-SM HC-MMC with $N_h = 6$ and $N_{fm} = 1$, where each level is equal to the nominal SM capacitor voltage ($V_{dc}/6$ in this example). In Table 3.1, the voltage levels for v_{upA} and v_{lowA} reflect the number of inserted SMs from the upper and lower arms, respectively, and the negative number indicates the required number of FB SMs inserted with negative capacitor voltages. As observed from Table 3.1, the peak value of v_{mA} is at $4V_{dc}/6$, which is consistent with $(1+2N_{fm}/N_h) \cdot V_{dc}/2$. Furthermore, the equivalent number of inserted SMs with positive capacitor voltage is always N_h for all possible voltage levels of v_{mA} . This indicates that the operating mechanism that ensures N_h SMs are inserted for each pair of upper and lower arms is still maintained for the mixed-SM HC-MMC. Therefore, the sorting and rotating method can still be used to ensure that the HB and FB SMs in the main power stage of the mixed-SM HC-MMC can be balanced and maintained at their nominal value (V_{dc}/N_h).

Table 3.1: Voltage levels for the mixed-SM HC-MMC with $N_h = 6$ and $N_{fm} = 1$

Voltage level of v_{upA}	-1	0	1	2	3	4	5	6	7
Voltage level of $v_{mA} (= V_{dc}/2 - v_{upA})$	4	3	2	1	0	-1	-2	-3	-4
Voltage level of $v_{lowA} (= V_{dc}/2 + v_{mA})$	7	6	5	4	3	2	1	0	-1
Equivalent inserted # of SMs	6	6	6	6	6	6	6	6	6

Note: Each voltage level is equal to the nominal SM capacitor voltage of $V_{dc}/6$ in this example.

Based upon the above analysis for the mixed-SM HC-MMC, the voltage v_{mA} is purely sinusoidal when $m \leq m_{mpk}$ and partially clipped to m_{mpk} when $m > m_{mpk}$. Similar to the analysis in Section 3.1, v_{mA} and v_{fbA} are as follows:

$$v_{mA}(t) = \frac{V_{dc}}{2} \cdot \begin{cases} +m_{mpk} & \text{if } \omega_0 t \in [\alpha, \pi - \alpha] \\ -m_{mpk} & \text{if } \omega_0 t \in [\pi + \alpha, 2\pi - \alpha] \\ m \sin(\omega_0 t) & \text{otherwise} \end{cases} \quad (3.11)$$

$$v_{fbA}(t) = v_{conA}(t) - v_{mA}(t) = \frac{V_{dc}}{2} \cdot \begin{cases} m \sin(\omega_0 t) - m_{mpk} & \text{if } \omega_0 t \in [\alpha, \pi - \alpha] \\ m \sin(\omega_0 t) + m_{mpk} & \text{if } \omega_0 t \in [\pi + \alpha, 2\pi - \alpha] \\ 0 & \text{otherwise} \end{cases} \quad (3.12)$$

where $\alpha = \sin^{-1}(m_{mpk}/m)$ and $m > m_{mpk}$. The average power delivered by the main stage is:

$$\begin{aligned} P_{mA}(m) &= \frac{1}{T_o} \int_0^{T_o} v_{mA}(t) \cdot i_{conA}(t) dt \\ &= \frac{1}{2\pi} \left[\int_0^\alpha m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta + \int_\alpha^{\pi-\alpha} m_{mpk} \cdot \frac{V_{dc}}{2} \cdot I_m \sin(\theta + \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi-\alpha}^{\pi+\alpha} m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta \right. \\ &\quad \left. + \int_{\pi+\alpha}^{2\pi-\alpha} -m_{mpk} \cdot \frac{V_{dc}}{2} \cdot I_m \sin(\theta + \varphi) d\theta + \int_{2\pi-\alpha}^{2\pi} m \frac{V_{dc}}{2} \sin(\theta) \cdot I_m \sin(\theta + \varphi) d\theta \right] \\ &= \frac{V_{dc} I_m \cos(\varphi) m_{mpk}}{2\pi} \left(\frac{\sqrt{m^2 - m_{mpk}^2}}{m} + \frac{m}{m_{mpk}} \sin^{-1} \left(\frac{m_{mpk}}{m} \right) \right) \end{aligned} \quad (3.13)$$

Similar to (3.7), let the average power delivered by the FB stack be zero and be controlled by the modified SPWM method when $m > m_{mpk}$, and it yields:

$$\begin{aligned}
P_{\text{fbA}} &= P_{\text{conA}}(m) - P_{\text{mA}}(m_{\text{new}}) = 0 \\
\Rightarrow \frac{mV_{\text{dc}}I_m \cos(\varphi)}{4} - \frac{V_{\text{dc}}I_m \cos(\varphi)m_{\text{mpk}}}{2\pi} \left(\frac{\sqrt{m_{\text{new}}^2 - m_{\text{mpk}}^2}}{m_{\text{new}}} + \frac{m_{\text{new}}}{m_{\text{mpk}}} \sin^{-1}\left(\frac{m_{\text{mpk}}}{m_{\text{new}}}\right) \right) &= 0 \quad (3.14) \\
\Rightarrow m = \frac{2m_{\text{mpk}}}{\pi} \left[\frac{\sqrt{m_{\text{new}}^2 - m_{\text{mpk}}^2}}{m_{\text{new}}} + \frac{m_{\text{new}}}{m_{\text{mpk}}} \sin^{-1}\left(\frac{m_{\text{mpk}}}{m_{\text{new}}}\right) \right] &\text{ if } m > m_{\text{mpk}}
\end{aligned}$$

To compare the properties of the three FB-SM capacitor voltage regulation methods, Fig. 3.3 (a)-(c) illustrate the relationship between the modulation index (m) and the control variable k_t for the trapezoidal PWM method and m_{new} for both the modified sinusoidal PWM method and the mixed-SM approach based upon the expressions shown in (3.9), (3.10) and (3.14), respectively.

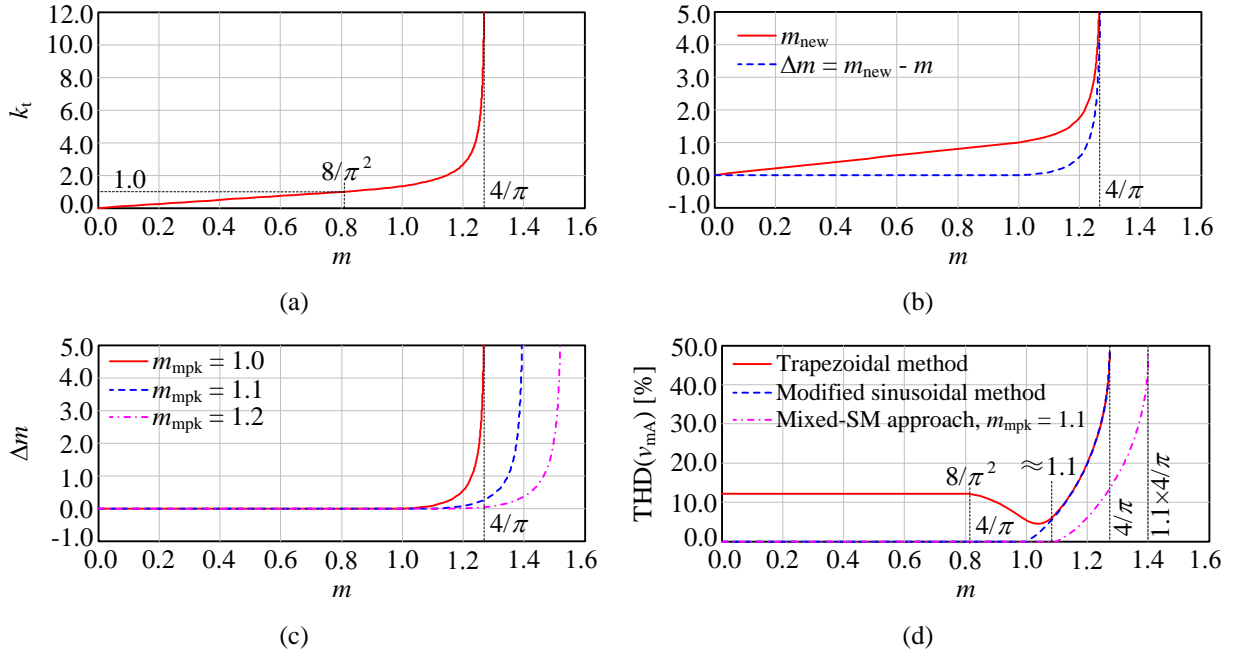


Fig. 3.3: Comparison of the methods to regulate the FB-SM capacitor voltages in the phase limb

(a) trapezoidal PWM method: $k_t(m)$; (b) modified sinusoidal PWM method: $m_{\text{new}}(m)$ and $\Delta m(m)$; (c) modified sinusoidal PWM method with mixed SMs: $\Delta m(m)$ for different m_{mpk} ; (d) THD of voltage v_{mA} .

As seen from Fig. 3.3 (a), the trapezoidal PWM method has a linear-regulation range up to $8/\pi^2$ and achieves the maximum modulation index of $4/\pi$. Compared with the trapezoidal PWM method, the proposed modified sinusoidal PWM method extends the linear-regulation range to 1.0 and

permits a maximum modulation index of $4/\pi$ as illustrated in Fig. 3.3 (b). It is seen from Fig. 3.3 (c) that the proposed mixed-SM approach further extends the linear-regulation range up to m_{mpk} and the maximum modulation index to $4m_{\text{mpk}}/\pi$, where $m_{\text{mpk}} = (1+2N_{\text{fm}}/N_{\text{h}})$. For example, if 5% additional FB SMs are added to the main power stage, i.e., $N_{\text{fm}}/N_{\text{h}} = 0.05$, the linear range of the converter will be extended by 10%. Furthermore, if 3rd harmonic injection is used (see Fig. 3.2 (d)), the linear modulation index can extend to $1.15m_{\text{mpk}}$. The selection of the ratio of the numbers of FB and HB SMs in the main power stage of the mixed-SM HC-MMC (i.e., $N_{\text{fm}}/N_{\text{h}}$) depends not only on the expected linear modulation range but also other factors, such as the SM capacitor size, system efficiency, dc-fault performance and so forth. After the analysis of SM capacitor sizing in Chapter 4, the recommended ratio of the numbers of FB and HB SMs in the main power stage of mixed-SM HC-MMC will be summarized in Section 4.3.2.3 and hence the range of m_{mpk} can be readily obtained. The influence of the added FB SMs on converter losses and dc-fault performance will be analyzed in Sections 5.3.2 and 6.1.2, respectively.

Based upon the above analysis, Table 3.2 summarizes the properties of the three voltage regulation methods. Both the trapezoidal and modified sinusoidal PWM methods have a maximum modulation index of $4/\pi$, whereas the mixed-SM approach has a higher range up to $4m_{\text{mpk}}/\pi$. The linear modulation range becomes progressively larger from $8/\pi^2$ (trapezoidal) to 1.0 (modified sinusoidal) and to m_{mpk} (mixed-SM). If 3rd harmonic injection is used, the linear ranges of the modified sinusoidal PWM and the mixed-SM approaches may be increased by an additional 15%.

Table 3.2: Properties of three voltage regulation methods

Property \ Method	Trapezoidal PWM	Modified sinusoidal PWM	Mixed-SM approach
Linear range	$[0, 8/\pi^2]$	$[0, 1.0]$	$[0, m_{\text{mpk}}]$
Maximum modulation index	$4/\pi$	$4/\pi$	$4m_{\text{mpk}}/\pi$

3.3 THD analysis of the main power stage voltage

As described in Section 3.2, the discussed voltage regulation methods are to adjust the voltage reference for the main power stage (v_{mA-ref}), which directly influences the filtering burden for the FB stack in the phase limb. In order to evaluate the filtering burden on the FB stack, the THD of the voltage crafted by the main power stage (v_{mA}) is analyzed for the different voltage regulation methods. In general, the THD of a periodic waveform is defined as follows:

$$\text{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} V_{hrms}^2}}{V_{1rms}} = \frac{\sqrt{V_{rms}^2 - V_{1rms}^2}}{V_{1rms}} = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1} \quad (3.15)$$

where V_{rms} and V_{hrms} are the root mean square (RMS) of the waveform and the h -th harmonic component, respectively.

For the trapezoidal PWM method, the RMS values of the trapezoidal waveform (expressed in (3.8)) and its fundamental component are as follows:

$$\begin{aligned} V_{\text{trap_rms}}^2 &= \frac{2}{T_o} \int_0^{T_o/2} v_{mA}(t)^2 dt \\ &= \begin{cases} \frac{1}{\pi} \left[\int_0^{\pi/2} \left(\frac{2}{\pi} k_t \theta\right)^2 d\theta + \int_{\pi/2}^{\pi} \left(-\frac{2}{\pi} k_t (\theta - \pi/2)\right)^2 d\theta \right] = \frac{1}{3} k_t^2 & \text{if } 0 < k_t \leq 1 \\ \frac{1}{\pi} \left[\int_0^{\pi/2k_t} \left(\frac{2}{\pi} k_t \theta\right)^2 d\theta + \int_{\pi/2k_t}^{\pi - \pi/2k_t} 1^2 d\theta + \int_{\pi - \pi/2k_t}^{\pi} \left(\frac{2}{\pi} k_t (\theta - \pi + \pi/2k_t)\right)^2 d\theta \right] = 1 - \frac{2}{3k_t} & \text{if } k_t > 1 \end{cases} \quad (3.16) \end{aligned}$$

$$\begin{aligned}
V_{\text{trap_1rms}} &= \frac{1}{\sqrt{2}} \cdot \frac{2}{T_o} \int_0^{T_o/2} v_{\text{mA}}(t) e^{-j\omega_o t} dt = \frac{1}{\sqrt{2}\pi} \int_0^{\pi/2} v_{\text{mA}}(\theta) e^{-j\theta} d\theta \\
&= \begin{cases} \frac{8k_t}{\sqrt{2}\pi^2} & \text{if } 0 < k_t \leq 1 \\ \frac{8k_t}{\sqrt{2}\pi^2} \sin\left(\frac{\pi}{2k_t}\right) & \text{if } k_t > 1 \end{cases} \quad (3.17)
\end{aligned}$$

Thus, the THD of v_{mA} under the trapezoidal PWM method is readily obtained as follows:

$$\text{THD}_{\text{trap}} = \sqrt{\frac{V_{\text{trap_rms}}^2}{V_{\text{trap_1rms}}^2} - 1} = \begin{cases} \sqrt{\frac{\pi^4}{96} - 1} \approx 12.115\% & \text{if } 0 < k_t \leq 1 \\ \sqrt{\frac{\pi^4 (3k_t - 2)}{96k_t^3 \sin^2(\pi/2k_t)} - 1} & \text{if } k_t > 1 \end{cases} \quad (3.18)$$

For the modified sinusoidal PWM methods, the RMS values of the waveform (expressed in (3.11)) and its fundamental component of the mixed-SM HC-MMC are as follows:

$$\begin{aligned}
V_{\text{sin_rms}}^2 &= \frac{2}{T_o} \int_0^{T_o/2} v_{\text{mA}}(t)^2 dt \\
&= \begin{cases} \left(\frac{m_{\text{new}}}{\sqrt{2}}\right)^2 = \frac{m_{\text{new}}^2}{2} & \text{if } m_{\text{new}} \leq m_{\text{mpk}} \\ \frac{m_{\text{mpk}}^2}{\pi} \left[\pi + \left(\left(\frac{m_{\text{new}}}{m_{\text{mpk}}}\right)^2 - 2 \right) \sin^{-1}\left(\frac{m_{\text{mpk}}}{m_{\text{new}}}\right) - \sqrt{\left(\frac{m_{\text{new}}}{m_{\text{mpk}}}\right)^2 - 1} \right] & \text{if } m_{\text{new}} > m_{\text{mpk}} \end{cases} \quad (3.19)
\end{aligned}$$

$$\begin{aligned}
V_{\text{sin_1rms}} &= \frac{1}{\sqrt{2}} \cdot \frac{2}{T_o} \int_0^{T_o/2} v_{\text{mA}}(t) e^{-j\omega_o t} dt = \frac{1}{\sqrt{2}\pi} \int_0^{\pi/2} v_{\text{mA}}(\theta) e^{-j\theta} d\theta \\
&= \begin{cases} \frac{m_{\text{new}}}{\sqrt{2}} & \text{if } m_{\text{new}} \leq m_{\text{mpk}} \\ \frac{\sqrt{2}m_{\text{mpk}}}{\pi} \left[\sqrt{1 - \left(\frac{m_{\text{mpk}}}{m_{\text{new}}}\right)^2} + \left(\frac{m_{\text{new}}}{m_{\text{mpk}}}\right) \cdot \sin^{-1}\left(\frac{m_{\text{mpk}}}{m_{\text{new}}}\right) \right] & \text{if } m_{\text{new}} > m_{\text{mpk}} \end{cases} \quad (3.20)
\end{aligned}$$

Therefore, the THD of v_{mA} with the modified sinusoidal PWM method is as follows:

$$\text{THD}_{\sin} = \sqrt{\frac{V_{\sin_rms}^2}{V_{\sin_1rms}^2} - 1} = \begin{cases} 0 & \text{if } m_{\text{new}} \leq m_{\text{mpk}} \\ \sqrt{\frac{\pi}{2} \cdot \frac{K_1}{K_2} - 1} & \text{if } m_{\text{new}} > m_{\text{mpk}} \end{cases} \quad (3.21)$$

where K_1 and K_2 are

$$\begin{aligned} K_1 &= \pi + \left(\left(\frac{m_{\text{new}}}{m_{\text{mpk}}} \right)^2 - 2 \right) \sin^{-1} \left(\frac{m_{\text{mpk}}}{m_{\text{new}}} \right) - \sqrt{\left(\frac{m_{\text{new}}}{m_{\text{mpk}}} \right)^2 - 1} \\ K_2 &= \left[\sqrt{1 - \left(\frac{m_{\text{mpk}}}{m_{\text{new}}} \right)^2} + \left(\frac{m_{\text{new}}}{m_{\text{mpk}}} \right) \cdot \sin^{-1} \left(\frac{m_{\text{mpk}}}{m_{\text{new}}} \right) \right]^2 \end{aligned} \quad (3.22)$$

where $m_{\text{mpk}} = 1$ for the original HC-MMC, and $m_{\text{mpk}} > 1$ for the mixed-SM HC-MMC. Further, combining the THD expressions (shown in (3.18) and (3.21)) with (3.9) and (3.14), the relationships between THD with the converter's modulation index, m , can be established.

Fig. 3.3 (d) shows the THD of v_{mA} with these three different voltage regulation methods. It is observed that the trapezoidal PWM method has much higher THD due to the low-frequency harmonics embedded in its reference waveform, whereas the modified sinusoidal PWM method used for the original HC-MMC is devoid of harmonics in idealized conditions when $m < 1.0$, and has markedly lower THD when $m < 1.1$. For modulation indices larger than approximately 1.1, these two PWM methods have nearly identical THD. Thereby, the modified sinusoidal PWM method has better ability in both extending the linear range of the converter operation and generating less harmonic content. Additionally, for the mixed-SM approach in conjunction with the modified sinusoidal PWM method, the THD of the voltage crafted by the main power stage is lower than both the trapezoidal and the modified sinusoidal PWM methods used for the original HC-MMC.

3.4 Experimental validation for the voltage regulation methods

A downscaled laboratory setup, shown in Fig. 3.4, is used to verify the ability of the discussed methods for regulating the FB-SM voltages. Table 3.3 shows the specifications of the setup, which is controlled via a real-time digital simulator (RTDS) and feeds a passive RL load as an inverter. Compared with theoretical analysis, the physical setup includes small losses, stray parameters in the power circuit path and semiconductors, high-order harmonics and small tolerances in component values. A digital oscilloscope and voltage probes with 200 MHz bandwidth are used to measure the experimental waveforms with industrial-grade accuracy.

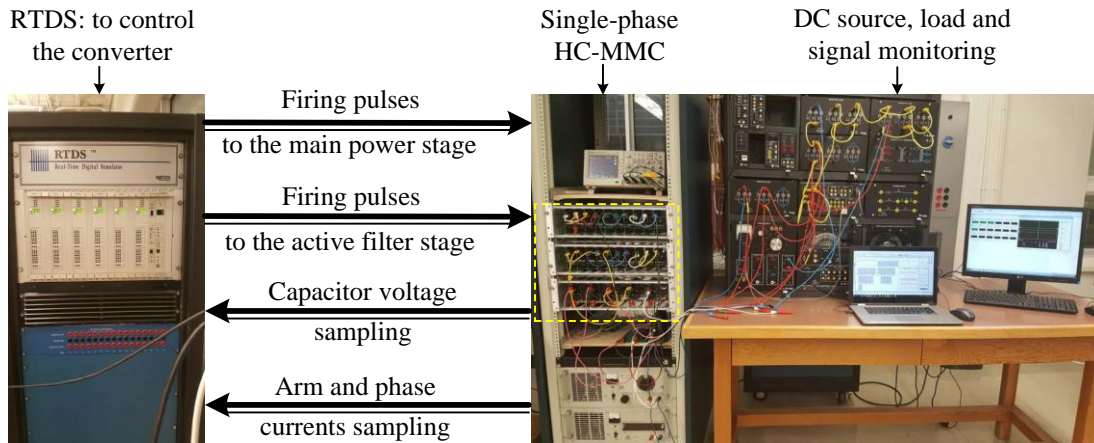


Fig. 3.4: Downscaled laboratory prototype of HC-MMC

Table 3.3: Specifications of the experimental HC-MMC hardware

DC-link voltage: 120 V	Base frequency: 60 Hz	Arm inductance: 2.2 mH	Load: 57 Ω and 0.23 H
# of SMs and SM capacitance	6 HB SMs/arm and 4.7 mF; 3 FB SMs/phase and 1.0 mF		
For mixed-SM approach	1 FB SM/arm and 4.7 mF		
SM capacitor voltage	20 V per SM		
Modulation method	PD-PWM ($9f_0$ for the main power stage, and $27f_0$ for the phase limb)		

The experimental waveforms using the trapezoidal and modified sinusoidal PWM methods for the original HC-MMC are shown in Fig. 3.5 (a) and (b), respectively, whereas the experimental results for the mixed-SM HC-MMC operating with the modified sinusoidal PWM method are

shown in Fig. 3.5 (c). It is seen from Fig. 3.5 that the average FB-SM capacitor voltage in the phase limb tracks the reference well for all methods. For the modified sinusoidal PWM method (Fig. 3.5 (b)), the control variable Δm is nearly zero for $m = 0.9$ (within linear range). It becomes a positive value to force the main power stage to compensate the power delivered by the FB stack in the phase limb when $m = 1.2$ (within the nonlinear range) in order to maintain the FB-SM capacitor voltages.

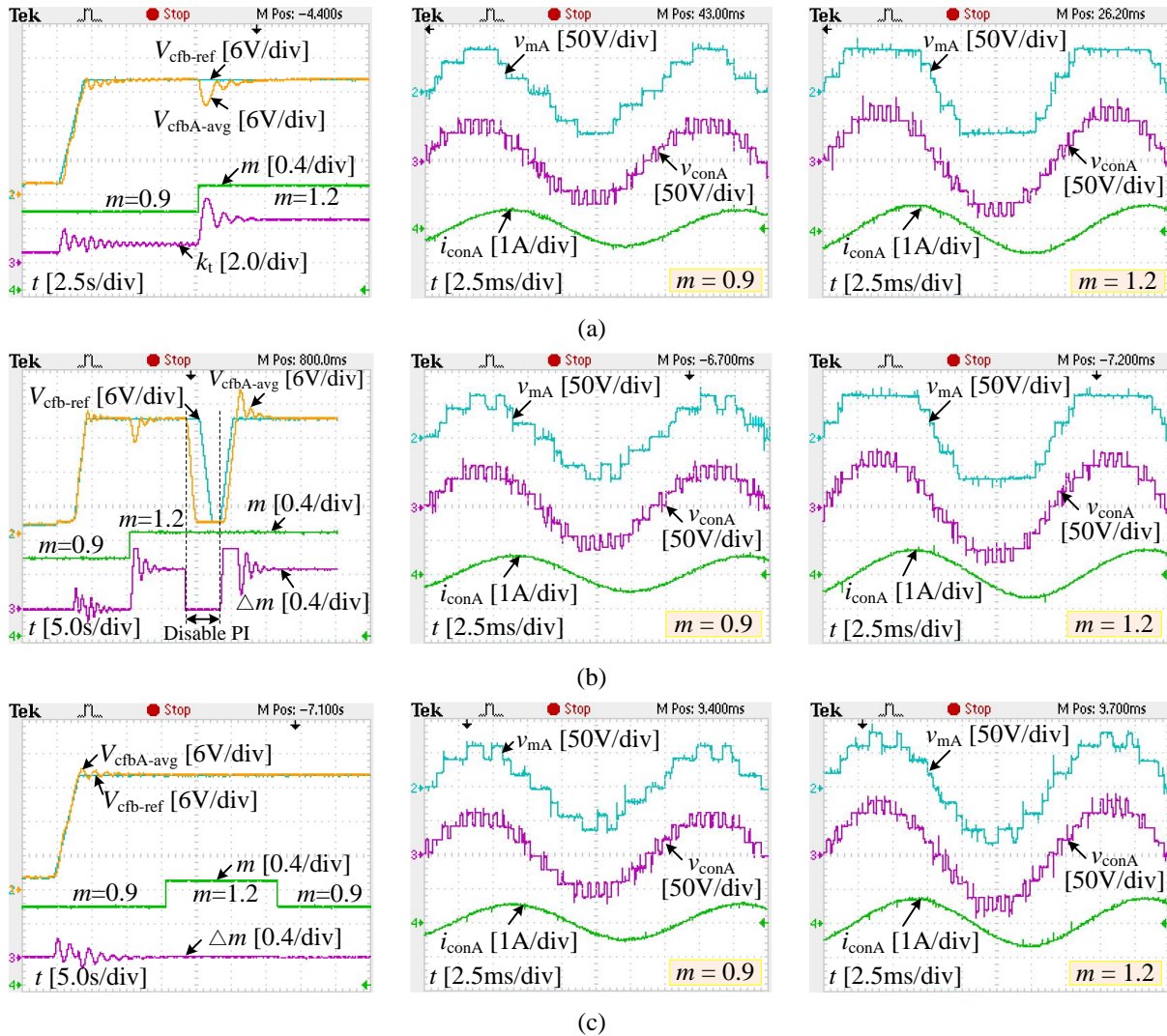


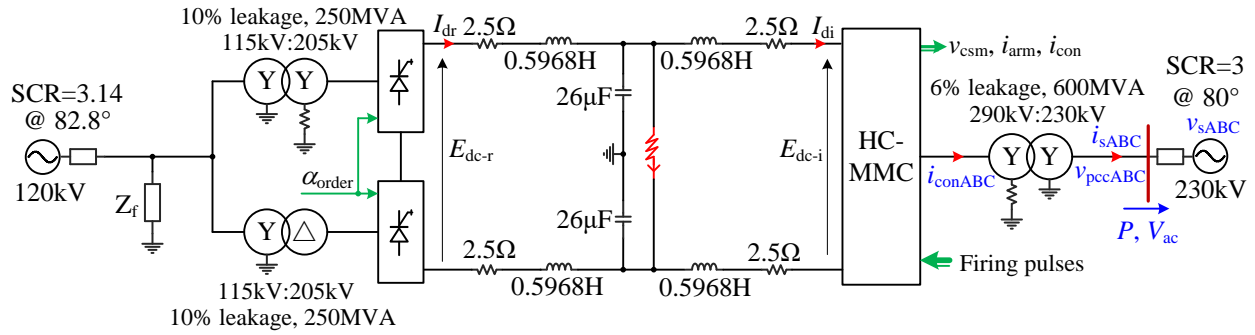
Fig. 3.5: Experimental results with different FB-SM capacitor-voltage regulation methods and steady-state waveforms for $m = 0.9$ and $m = 1.2$

(a) trapezoidal PWM method; (b) modified sinusoidal PWM method; (c) mixed-SM HC-MMC with modified sinusoidal PWM method.

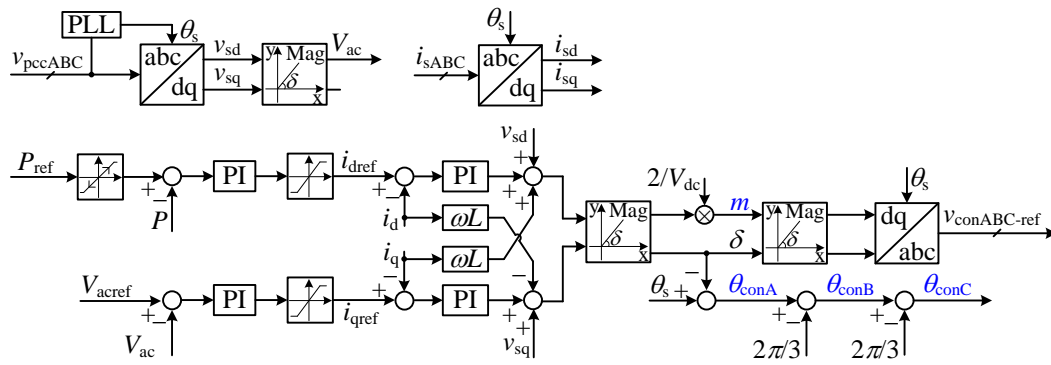
To further demonstrate the regulating effect of Δm , the PI controller is deactivated momentarily as shown in Fig. 3.5 (b) for $m = 1.2$. This causes the average FB-SM capacitor voltage to drop, which is consistent with the analysis in Section 3.1; upon reactivation of the PI controller, the FB-SM capacitor voltages are restored to their nominal value (20 V). As seen from Fig. 3.3 (d) for the mixed-SM approach, the variable Δm remains negligible even for the modulation index of 1.2 (compared with Fig. 3.5 (b)), and the average capacitor voltage of all FB SMs in phase limb remains tightly around their nominal value (20.0 V) while experiencing dynamic variations. That is because the insertion of one FB SM in series with the existing 6 HB SMs extends the linear range to $(1+2 \times 1/6) \approx 1.333$. In addition, as seen from the steady-state waveforms of v_{mA} and v_{conA} shown in Fig. 3.5 (a)-(c), the individual voltage steps of both v_{mA} and v_{conA} are approximately the nominal value (20.0 V). Therefore, it can be concluded that the all the SM capacitor voltages are well balanced.

3.5 Simulation-based case study

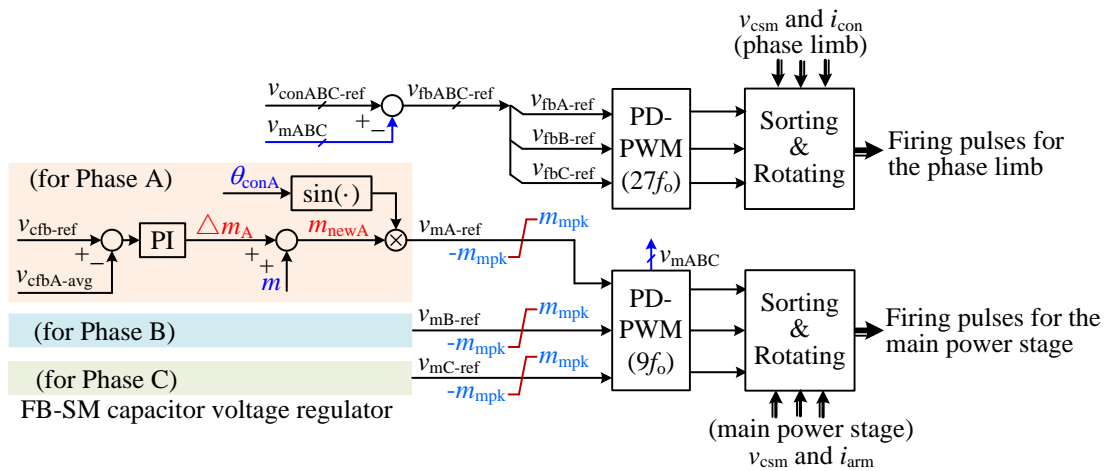
A large point-to-point HVDC transmission system with a LCC rectifier and an HC-MMC inverter, shown in Fig. 3.6 (a), is simulated in PSCADTM/EMTDCTM to validate the FB-SM capacitor-voltage regulation schemes proposed in Section 3.2. System parameters are given in Table 3.4 and Fig. 3.6 (a). The dc-side parameters are adopted from CIGRE HVDC Benchmark [81] and modified for a metallic return. The system control diagrams for HC-MMC and LCC are displayed in Fig. 3.6 (b)-(d), where Fig. 3.6 (b) shows the decoupled control for the PV bus at the inverter side, and Fig. 3.6 (c) illustrates the FB-SM capacitor voltage control for individual phase limb, and Fig. 3.6 (d) presents the dc-link voltage control and force-retard function for LCC.



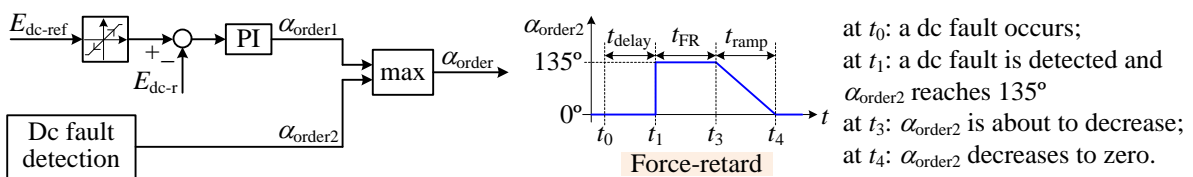
(a)



(b)



(c)



(d)

Fig. 3.6: LCC-HC-MMC transmission system

(a) schematic diagram; (b) decoupled control for the HC-MMC; (c) FB-SM capacitor voltage regulator based upon the modified sinusoidal PWM methods; (d) controls for LCC rectifier.

Table 3.4: System specifications of HC-MMC inverter

DC side: 500 MW, 500 kV	Base frequency: 60 Hz	Arm inductance: 0.05 H
AC grid voltage: 120 kV (rectifier); 230 kV (inverter)	SM capacitor voltage: 5.0 kV per SM	
# of SMs and SM capacitance	100 HB SMs/arm and 5.0 mF; 50 FB SMs/phase and 1.0 mF	
For the mixed-SM approach	5 FB SMs/arm and 5.0 mF	
Modulation method	PD-PWM ($9f_o$ for the main power stage, and $27f_o$ for the phase limb)	

3.5.1 Steady-state operation

Under normal conditions, the LCC's controller maintains the dc-link voltage, whereas the HC-MMC controls the active power and the ac voltage magnitude using decoupled control [82]. Simulation results of the inverter are shown for different capacitor voltage regulation methods.

Fig. 3.7 (a) illustrates the system response to reference variations at the inverter side with the proposed modified sinusoidal PWM method. The power order (P_{ref}) changes from 1.0 pu to 0.7 pu at 5.0 s and back to 1.0 pu at 7.0 s; the ac voltage magnitude reference (V_{acref}) changes from 1.0 pu to 1.2 pu at 9.0 s and back to 1.0 pu at 12.0 s. It is observed that the system accurately tracks the references with reasonable transient behavior. Additionally, the inverter-side modulation index is ~ 0.95 for 1.0 pu ac voltage magnitude reference and ~ 1.18 for 1.2 pu.

Based on the same reference changes, simulation results for the trapezoidal PWM, modified sinusoidal PWM, and mixed-SM approaches are shown in Fig. 3.7 (b), (c) and (d), respectively. As seen from Fig. 3.7 (c), with the modified sinusoidal PWM method, the required adjustment of the phase-A main power stage's modulation index (Δm_A) is approximately zero when the HC-MMC operates with $m \approx 0.95$ (voltage reference = 1.0 pu), and increases to ~ 0.32 when $m \approx 1.18$ (voltage reference = 1.2 pu). In addition, the average FB-SM capacitor voltage in the phase limb is tightly controlled to 5.0 kV as desired. Since harmonics are introduced for operation with $m > 1.0$ and must be filtered by the FB stack in the phase limb, the average FB-SM capacitor voltage

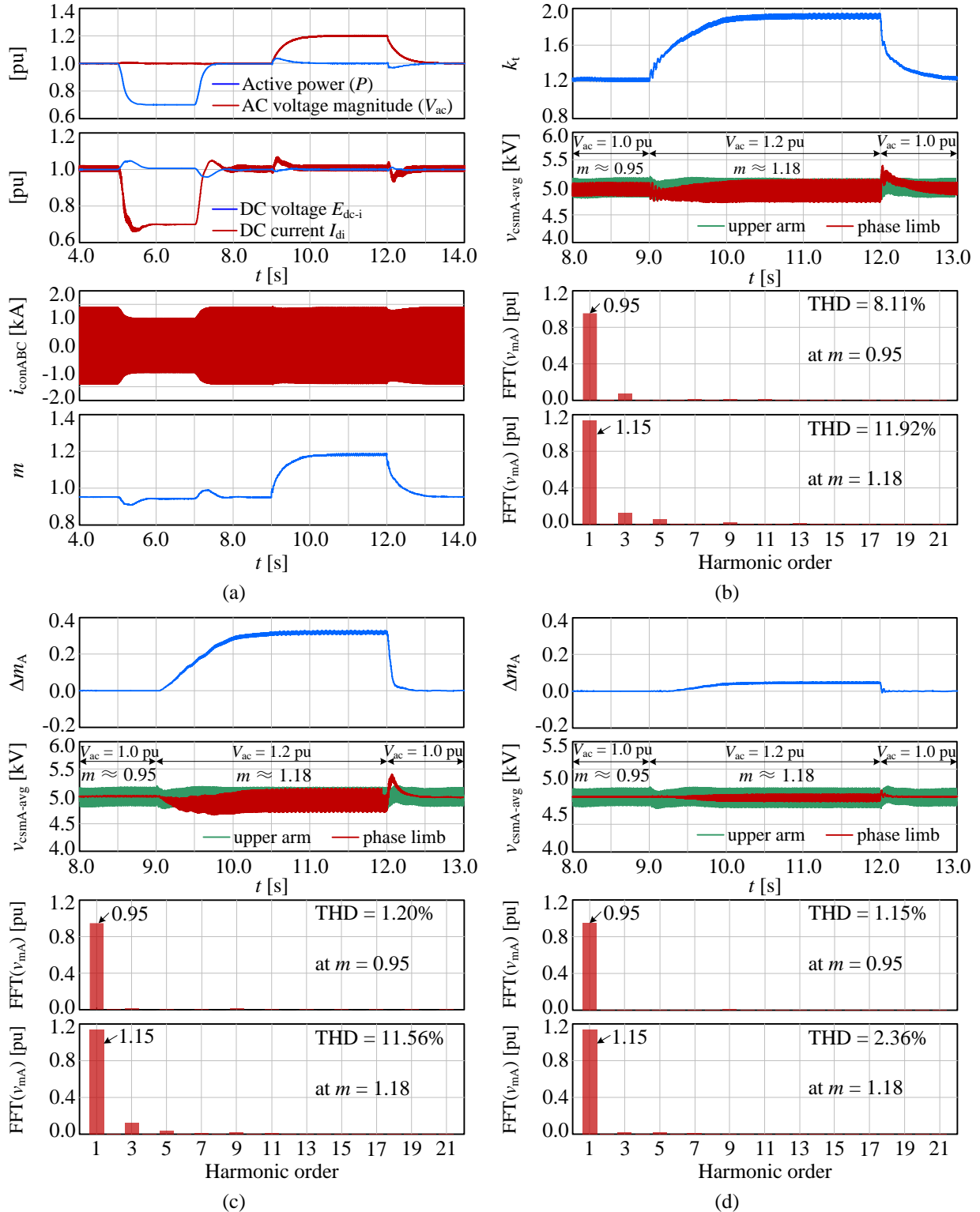


Fig. 3.7: Inverter-side waveforms with different voltage regulation methods for HC-MMC

(a) inverter-side waveforms with the modified sinusoidal PWM method; (b) system response with the trapezoidal PWM method; (c) system response with the modified sinusoidal PWM method; (d) system response with the mixed-SM approach and modified sinusoidal PWM methods.

has larger ripple compared with the operation with $m < 1.0$. In comparison, the trapezoidal PWM method always introduces harmonics in the voltage crafted by the main power stage. Compared to the operation with the modified sinusoidal PWM method shown in Fig. 3.7 (c), the ripple of the average FB-SM capacitor voltage in the phase limb is larger for the operation with the modulation index of 0.95 as shown in Fig. 3.7 (b).

The HC-MMC is also simulated with addition of FB SMs in the main power stage. Five FB SMs are added to each arm in the main power stage, corresponding to a 5% increase in the number of SMs and a 10% increase in the linear modulation range. Fig. 3.7 (d) shows that the required Δm_A to produce an output voltage of 1.0 pu (for $t < 9.0$ s) is negligible with the modulation index of 0.95, and is far less than the adjustment in Fig. 3.7 (c) for modulation index of 1.18 due to the extended linear range. The ripple of the average FB-SM capacitor voltage (Fig. 3.7 (d)) is smaller than the original HC-MMC due to the reduced harmonic contents of the voltage crafted by the main power stage.

3.5.2 DC-fault performance

After the development of effective controls for the original and mixed-SM HC-MMCs, their dc-fault blocking capability is investigated by simulating a pole-to-pole fault in the middle of the dc transmission line. This dc fault is applied at $t = 4.0$ s for 0.1 s, and the dc-fault detection delay is set as 8.0 ms. As seen from Table 3.4, the system parameters of the mixed-SM HC-MMC are the same as those of the original HB-MMC, except that the mixed-SM HC-MMC has five additional FB SMs per arm in its main power stage. The simulation results of the original and mixed-SM HC-MMCs under the dc fault are shown in Fig. 3.8 (a) and (b), respectively. During the fault, the LCC employs force-retard [83] while the HC-MMCs are blocked and their power-orders are reduced to zero as illustrated in the first subplots of Fig. 3.8 (a) and (b). As seen from

the third subplots in Fig. 3.8 (a) and (b), the three-phase currents promptly decay to zero after the dc fault is detected and the inverter is blocked. This benefits from the existence of FB SMs in the phase limb.

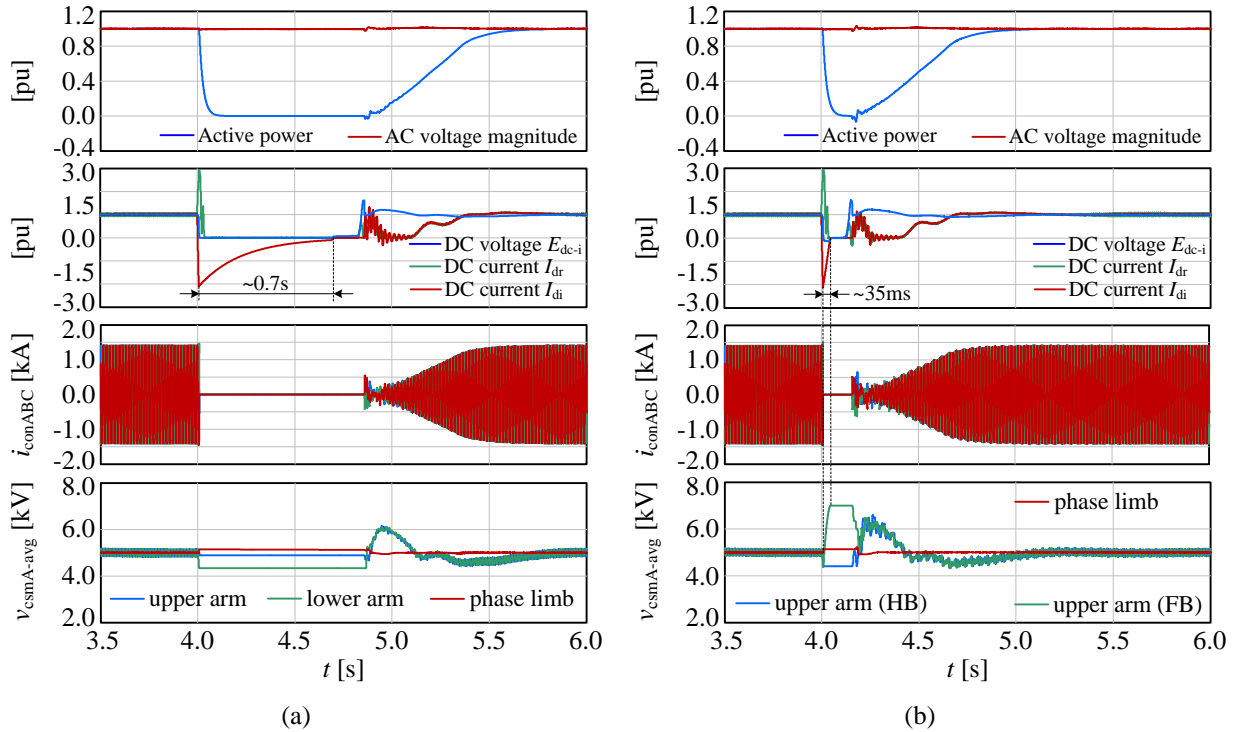


Fig. 3.8: Inverter response of the original and mixed-SM HC-MMCs to a pole-to-pole dc fault
(a) waveforms for the original HC-MMC; (b) waveforms for the mixed-SM HC-MMC.

After the inverter is blocked, all the FB SMs in the phase limb are inserted to charge to quickly decay the phase currents. As shown in the second subplots of Fig. 3.8 (a) and (b), the rectifier-side dc current rapidly decays to zero due to LCC's forced-retard operation, and the original and mixed-SM HC-MMCs take approximately 0.7 s and 35.0 ms to clear their dc-side fault currents, respectively. It is noticed that the original HC-MMC takes 20 times longer time than the mixed-SM HC-MMC. The dc-side fault current in the original HC-MMC circulates between the converter arms and the dc network and decays due to the line resistance, which takes a relatively long time to diminish. Due to the existence of FB SMs in the main power stage of the mixed-SM HC-MMC,

the dc-side fault current promptly decays to zero since the FB SMs are inserted to charge after blocking the converter. This validates the additional benefit of the proposed mixed-SM HC-MMC on clearing dc fault. As seen from the fourth subplots in Fig. 3.8 (a) and (b), the system restarts and all the SM capacitor voltages are quickly restored to the required value (5.0 kV) after the dc fault clearance. Nevertheless, the FB-SM capacitors in the main power stage are charged to large voltage values during the dc fault. To avoid overvoltage damage, proper SM capacitance selection is of importance, which is one of the aims in this thesis. Considering normal and dc-fault conditions, the details about SM capacitor sizing for the original and mixed-SM HC-MMCs can be found in Chapter 4 and Chapter 6.

3.6 Summary and key contributions

Based upon the analysis of average power for the HC-MMC, it was shown that regulation of the FB-SM capacitor voltages in the phase limb requires modifications to the control scheme of the main power stage. The existing trapezoidal PWM method [34] was shown to have a relatively small linear range ($m < 8/\pi^2 \approx 0.81$) and excessive harmonic distortion. To improve the performance of regulating the FB-SM capacitor voltages, a modified sinusoidal PWM method was proposed and proven to have an extended linear range ($m < 1.0$ or 1.15 with 3rd harmonic injection) and reduced harmonics in its linear range. To enhance the advantages of the proposed control method, a topology modification was proposed by adding FB SMs to the main power stage. Experimental results on a scaled-down laboratory setup verified the efficacy of the proposed control strategy to regulate the FB-SM capacitor voltages for both the original and mixed-SM HC-MMCs. Furthermore, extensive EMT simulations displayed the operation and functionality of the proposed control method for the original and mixed-SM HC-MMCs in a large transmission system.

Chapter 4

SM Capacitor Sizing for HC-MMCs Considering Normal Operation

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Important considerations to obtain proper operations of the investigated HC-MMCs, including the selection of the number of SMs and the FB-SM capacitor-voltage regulation methods, were studied in Chapter 2 and Chapter 3, respectively. However, proper selection of MMC circuit parameters is also of significant importance to achieve a small footprint (e.g., small SM capacitors, arm inductors, and transformers) and high efficiency. SM capacitor sizing has attracted a great deal of attention [47]-[48], [84], since these capacitors have large footprints in high-voltage and high-current applications and there is a large number of SM capacitors in an MMC.

In most contemporary literature, SM capacitance is selected based upon the operation with CCSC and the stored energy variations in SM capacitors [47]-[48]. The operating point used to

calculate the stored energy is obtained based upon a number of assumptions, such as ignoring the influence of converter transformers and the strength of the ac network. In [84] the SM capacitor selection under the operation without CCSC is discussed considering high-order harmonics, resulting in complicated models. However, the high-order harmonic contents are often much smaller than the 2nd harmonic and can be neglected to simplify the analysis. To evaluate the influence of the 2nd harmonic current on the SM capacitor voltage ripple, the 2nd harmonic current must be derived firstly. In [85], the 2nd harmonic current was derived based upon the assumption that the 2nd harmonic voltage across the two arm inductors is distributed equally among the total number of SMs per phase. This assumption is, however, not valid (see the derivation in Section 4.2.1 and validation in Section 4.2.3), and produces large errors in the estimated magnitude of 2nd harmonic current. Therefore, it is necessary to improve the calculation of the 2nd harmonic current to evaluate its influence on component sizing.

Compared to the original HC-MMC shown in Fig. 2.6, another HC-MMC (i.e., mixed-SM HCMMC) using additional FB SMs in the main power stage was proposed in Section 3.2.3 to further extend the linear modulation range. The topologies of the original and mixed-SM HC-MMCs and their operating waveforms are displayed in Fig. 4.1, where $N_{fm} = 0$ for the original HC-MMC and $N_{fm} > 0$ for the mixed-SM HC-MMC. Since the operation of the main power stage of the original HC-MMC is similar to that of the conventional HB-MMC, it may be possible to use the existing empirical guideline [46], i.e., a stored energy in all SM capacitors per power rating unit of 30~40 kJ/MVA, to select the SM capacitance used in the main power stage. However, this empirical guideline lacks solid analytical foundations. Nevertheless, there is no design guideline for the FB SM capacitance used in the phase limb and the main power stage of the mixed-SM HC-MMC in the existing literature. Therefore, this chapter aims at a mathematical and systematic

analysis of the SM capacitance selection for the original and mixed-SM HC-MMCs under normal operation with different operating modes, such as operation with or without CCSC, and operation with or without 3rd harmonic injection. In order to obtain safe operation and prompt recovery under dc faults, additional considerations for SM capacitance are required, which are analyzed in Chapter 6 based upon the equivalent models derived under dc faults. Note that, in this thesis, the parameter indicating the SM capacitor size is defined by the stored energy in SM capacitors per power rating unit in kJ/MVA or equivalently in millisecond, which is specifically expressed as follows:

$$EoP_{\text{Allsm}} = \frac{N_{\text{Allsm}} C_{\text{sm}} V_{\text{csm}}^2 / 2}{P_{\text{nom}}} \times 10^3 \text{ [kJ/MVA]} \quad (4.1)$$

where N_{Allsm} is the number of all SMs in a three-phase MMC, C_{sm} is the SM capacitance, V_{csm} is the nominal SM capacitor voltage, and P_{nom} is the converter's nominal power.

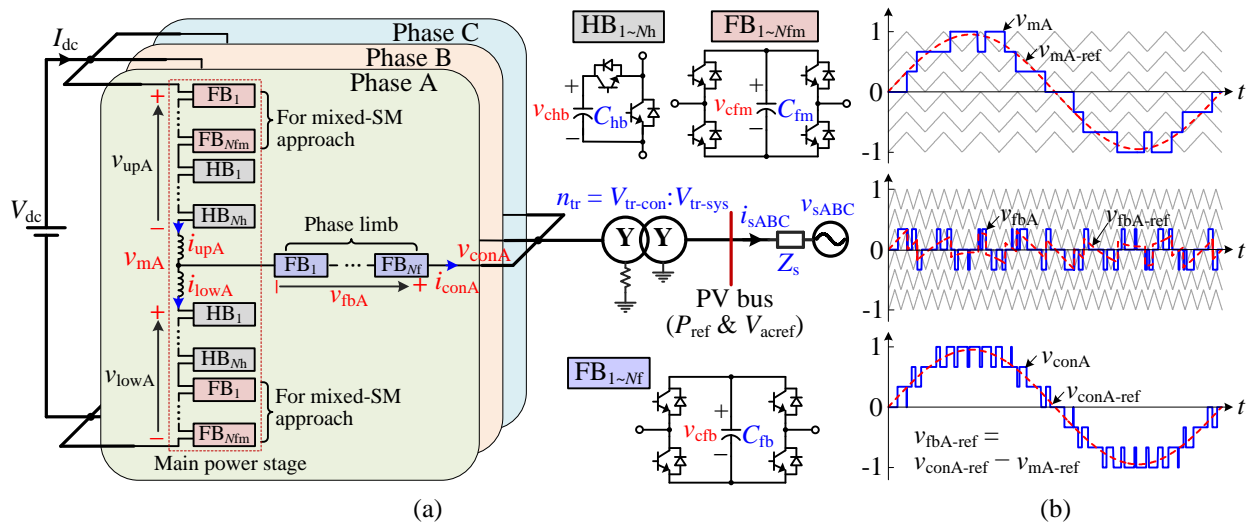


Fig. 4.1: Three-phase topologies of the original and mixed-SM HC-MMCs and typical operation waveforms (a) schematic; (b) operation waveforms with PD-PWM.

The analyses of SM capacitor sizing are investigated considering different control modes for HC-MMCs and they are presented in several subsections. For convenience of the reader, the content organization of this chapter is displayed in Fig. 4.2. Before the analysis of SM capacitance

design, operating point for a VSC connected to an ac grid is theoretically analyzed considering transformers and strength of ac network in Section 4.1. Then a general approach to calculate SM capacitor voltage ripple based upon electric charge variations is proposed in Section 4.2, wherein the 2nd harmonic in the arm current is accurately and explicitly derived in Section 4.2.1, and the derivation of the CCSC control output is shown in Section 4.2.2. Then the selections of SM capacitance for the main power stage in the original and mixed-SM HC-MMCs are shown in Sections 4.3.1 and 4.3.2, respectively; the SM capacitance design for the FB stack in both the original and mixed-SM HC-MMCs is shown in Section 4.3.3.

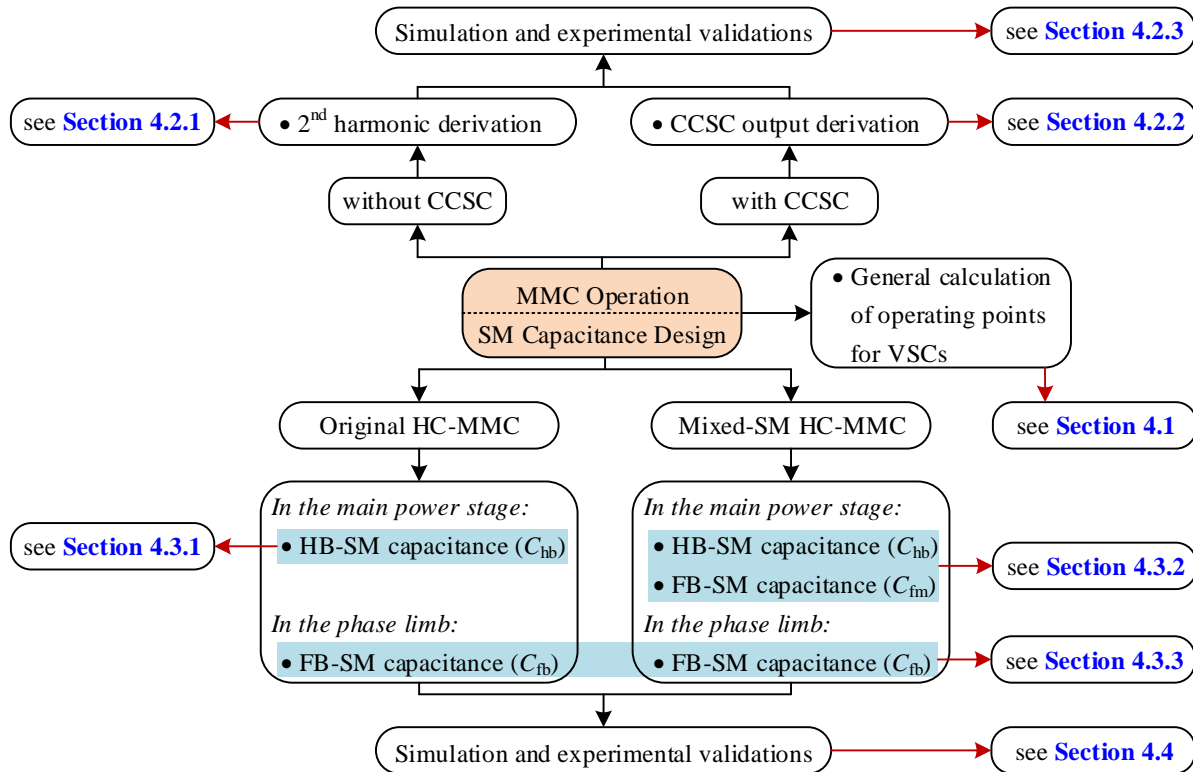


Fig. 4.2: Content organization of Chapter 4

4.1 Calculation of operating points for grid-connected VSCs

In order to estimate SM capacitor voltage ripple, the steady-state operating points are required to calculate the electric charge variations in SM capacitors. Fig. 4.3 shows the typical connection

of a VSC in an HVDC transmission system. Neglecting the converter's losses, the dc-side current is calculated as follows:

$$I_{dc} = P_{dc} / V_{dc} = P_{ref} P_{nom} / V_{dc} \quad (4.2)$$

where I_{dc} is the dc-side current, V_{dc} is the dc-link voltage, P_{nom} is the nominal real power, and P_{ref} is the real power reference in per-unit with a base value of P_{nom} .

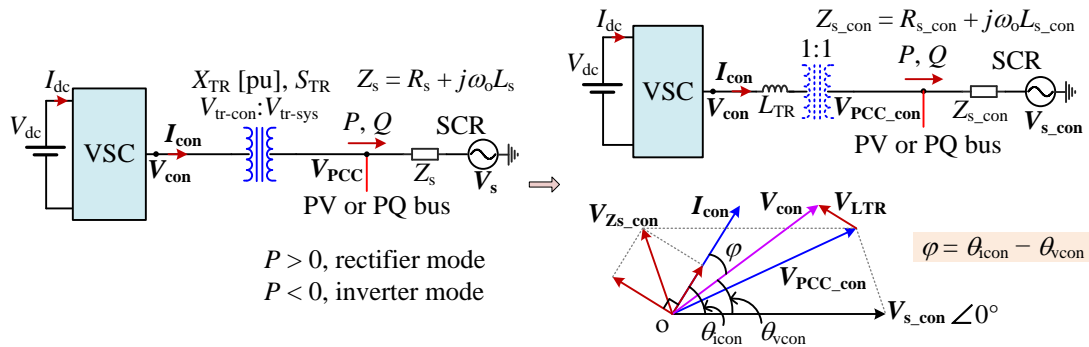


Fig. 4.3: Connection of a VSC to an ac system

As seen from Fig. 4.3, the VSC is connected to an ac network through a transformer, whose rating and leakage inductance are denoted as S_{TR} and X_{TR} in per-unit. The nominal dc power is selected as the base value for power and the leakage inductance of the transformer is per-unitized based upon the transformer's own voltage and power ratings. In practice, the ac network is not an infinite bus and its short circuit ratio (SCR) is commonly used to describe its strength. The definition of SCR is as follows:

$$SCR = \frac{V_{sLL_nom}^2}{|Z_s| P_{nom}} \angle Z_s \quad (4.3)$$

where V_{sLL_nom} is the nominal RMS line-to-line voltage of the ac network, Z_s is the ac-network impedance generally composed of resistance (R_s) and inductance (L_s) in series. By reflecting the ac network to the converter side, the transformer is eliminated or regarded as an ideal transformer

with unity turns ratio as shown in Fig. 4.3, wherein V_{s_con} and $Z_{s_con} (= R_{s_con} + j\omega_0 L_{s_con})$ are the ac network RMS voltage and impedance reflected to the converter side, respectively.

Other parameters are defined under nominal conditions to obtain a general expression for the operating point at the ac side of a VSC, and they are listed as follows:

(1) m_{rated} (rated modulation index): it defines the relationship between the nominal dc-side voltage and the nominal voltage magnitude of the ideal ac network. To achieve reasonable voltage utilization, its practical range is selected within [0.9, 1.0] or [0.9, 1.15] with 3rd harmonic injection;

(2) SCR (short circuit ratio): it describes the strength of the ac network as shown in (4.3), and its typical range in HVDC transmission system is considered within [2.0, 8.0] for the magnitude and [75°, 90°] for the impedance angle;

(3) X_{TR}/S_{TR} (equivalent per-unit value of leakage inductance): the transformer capacity (S_{TR}) is typically larger than that of the nominal real power delivered by the system, since it must be capable of handling some amount of reactive power as well. In general, the leakage inductance is commonly described based upon the transformer's MVA rating. As such, the equivalent leakage inductance is introduced as X_{TR}/S_{TR} in per-unit value based upon the system's nominal real power, where S_{TR} presents the per-unit value based upon the system's nominal real power. In practice, the typical range of X_{TR}/S_{TR} is considered within [0.05 pu, 0.2 pu];

(4) X_{Larm} (the per-unit value of arm inductance): arm inductors are commonly used in MMCs to achieve high-quality current and limit the dc-fault current. In practice, arm inductors are primarily determined by the requirement of limiting the rising rate of dc-fault current. The typical range of X_{Larm} is considered within [0.1 pu, 0.2 pu] of the ac-side equivalent impedance for nominal operation.

With the above parameters, for a VSC with a nominal dc-link voltage of V_{dc} and nominal real power of P_{nom} , the circuit parameters can be calculated as follows:

$$\begin{aligned}
V_{s_con_nom} &= \frac{m_{rated} V_{dc}}{2\sqrt{2}} \\
Z_{s_con} &= \frac{\left(\sqrt{3}V_{s_con_nom}\right)^2}{P_{nom} |\text{SCR}|^2} \cdot \text{SCR} = \frac{3m_{rated}^2 V_{dc}^2}{8P_{nom} |\text{SCR}|^2} \left(\text{Re}(\text{SCR}) + j \text{Im}(\text{SCR})\right) = R_{s_con} + j\omega_o L_{s_con} \\
L_{TR} &= \frac{X_{TR}}{S_{TR}} \cdot \frac{\left(\sqrt{3}V_{s_con_nom}\right)^2}{P_{nom} \omega_o} = \frac{3m_{rated}^2 V_{dc}^2}{8P_{nom} \omega_o} \cdot \frac{X_{TR}}{S_{TR}} \\
L_{arm} &= X_{Larm} \cdot \frac{\left(\sqrt{3}V_{s_con_nom}\right)^2}{P_{nom} \omega_o} = \frac{3m_{rated}^2 V_{dc}^2}{8P_{nom} \omega_o} \cdot X_{Larm}
\end{aligned} \tag{4.4}$$

where ω_o is the system's fundamental angular frequency, $V_{s_con_nom}$ is the nominal ac network RMS voltage reflected to the converter side, and L_{TR} and L_{arm} are the leakage and arm inductance, respectively. In (4.4), operators $\text{Re}(\cdot)$ and $\text{Im}(\cdot)$ denote the real and imaginary parts, respectively.

In HVDC transmission systems, the PCC is typically controlled to be either a PV or a PQ bus as shown in Fig. 4.3. Based upon the respective set-points (P_{ref} , and V_{acref} or Q_{ref}), the following expressions hold:

$$\begin{aligned}
P_{ref} P_{nom} &= 3V_{s_con_nom} I_{con} \cos(\theta_{icon}) + 3I_{con}^2 R_{s_con} && \text{(for } P_{ref} \text{ constraint)} \\
V_{acref} V_{s_con_nom} &= \left| I_{con} e^{j\theta_{icon}} \cdot Z_{s_con} + V_{s_con_nom} \right| && \text{(for } V_{acref} \text{ constraint)} \\
Q_{ref} P_{nom} &= -3V_{s_con_nom} I_{con} \sin(\theta_{icon}) + 3I_{con}^2 \omega_o L_{s_con} && \text{(for } Q_{ref} \text{ constraint)}
\end{aligned} \tag{4.5}$$

where P_{ref} , V_{acref} and Q_{ref} are per-unit references of real power, ac-voltage magnitude and reactive power, respectively; I_{con} is the RMS phase current at converter side and θ_{icon} is the phase angle of the phase current relative to the ideal ac source voltage (see Fig. 4.3). Note that $P_{ref} > 0$ for inverter-mode operation and $P_{ref} < 0$ for rectifier-mode operation. The phase current can be solved by (4.5) and expressed as follows:

$$I_{\text{con}} = \frac{4P_{\text{nom}}}{3m_{\text{rated}}V_{\text{dc}}}\sqrt{X_0}$$

$$\cos(\theta_{\text{icon}}) = \frac{P_{\text{ref}}}{\sqrt{2X_0}} - \frac{\text{Re}(\text{SCR})}{|\text{SCR}|^2}\sqrt{2X_0}$$
(4.6)

where for PV control,

$$X_0 = P_{\text{ref}} \text{Re}(\text{SCR}) + V_{\text{acref}}^2 \text{Im}(\text{SCR})^2 + (1 - V_{\text{acref}}^2) |\text{SCR}|^2 / 2$$

$$- \text{Im}(\text{SCR}) \left[V_{\text{acref}}^2 |\text{SCR}|^2 - (P_{\text{ref}} - V_{\text{acref}}^2 \text{Re}(\text{SCR}))^2 \right]^{1/2}$$
(4.7)

$$\sin(\theta_{\text{icon}}) = \cos(\theta_{\text{icon}}) \frac{\text{Re}(\text{SCR})}{\text{Im}(\text{SCR})} + \frac{(1 - V_{\text{acref}}^2) |\text{SCR}|^2 + 2X_0}{2\sqrt{2X_0} \text{Im}(\text{SCR})}$$

and for PQ control,

$$X_0 = \frac{1}{4} \left(2P_{\text{ref}} \text{Re}(\text{SCR}) + 2Q_{\text{ref}} \text{Im}(\text{SCR}) + |\text{SCR}|^2 \right)$$

$$- \frac{1}{4} \left[\left(2P_{\text{ref}} \text{Re}(\text{SCR}) + 2Q_{\text{ref}} \text{Im}(\text{SCR}) + |\text{SCR}|^2 \right)^2 - 4(P_{\text{ref}}^2 + Q_{\text{ref}}^2) |\text{SCR}|^2 \right]^{1/2}$$
(4.8)

$$\sin(\theta_{\text{icon}}) = \frac{-Q_{\text{ref}}}{\sqrt{2X_0}} + \frac{\text{Im}(\text{SCR})}{|\text{SCR}|^2} \sqrt{2X_0}$$

As seen from (4.6), (4.7), and (4.8), X_0 and θ_{icon} are independent of the nominal power P_{nom} and dc-link voltage V_{dc} , whereas the RMS phase current I_{con} is proportional to $P_{\text{nom}}/V_{\text{dc}}$. Using the values of $\cos(\theta_{\text{icon}})$ and $\sin(\theta_{\text{icon}})$, θ_{icon} is determined as follows:

$$\theta_{\text{icon}} = \begin{cases} \cos(\cos(\theta_{\text{icon}}))^{-1} & \text{if } \sin(\theta_{\text{icon}}) \geq 0 \\ 2\pi - \cos(\cos(\theta_{\text{icon}}))^{-1} & \text{if } \sin(\theta_{\text{icon}}) < 0 \end{cases}$$
(4.9)

After obtaining the converter-side phase current, the converter's phase voltage is obtained as

$$V_{\text{con}} = V_{\text{s_con_nom}} + \left[j\omega_o (L_{\text{arm}}/2 + L_{\text{TR}}) + Z_{\text{s_con}} \right] \cdot I_{\text{con}} e^{j\theta_{\text{icon}}} = \frac{m_{\text{rated}} V_{\text{dc}}}{2\sqrt{2}} Y_0$$
(4.10)

where

$$Y_0 = 1 + \sqrt{2X_0} \left[\frac{\text{SCR}}{|\text{SCR}|^2} + j \left(\frac{X_{\text{Larm}}}{2} + \frac{X_{\text{TR}}}{S_{\text{TR}}} \right) \right] e^{j\theta_{\text{icon}}} \quad (4.11)$$

and Y_0 is independent of P_{nom} and V_{dc} . Note that X_{Larm} appears due to the presence of arm inductors used in MMCs. If there are no inductors (such as in a two-level VSC), X_{Larm} is set to zero in (4.11). As seen from (4.10), the phase angle of the converter-side voltage relative to the ideal ac source voltage (see Fig. 4.3), θ_{vcon} , is determined by

$$\theta_{\text{vcon}} = \arg(Y_0) \quad (4.12)$$

Therefore, the angle difference between the phase current and voltage, φ , is equal to

$$\varphi = \theta_{\text{icon}} - \theta_{\text{vcon}} = \cos^{-1} \left(\frac{P_{\text{ref}}}{\sqrt{2X_0} |Y_0|} \right) \quad (4.13)$$

Then the operating modulation index, m , is expressed as follows:

$$m = \frac{\sqrt{2}|V_{\text{con}}|}{V_{\text{dc}}/2} = m_{\text{rated}} |Y_0| \quad (4.14)$$

With the above solutions, Table 4.1 summarizes the relationship between operating parameters and the nominal real power and dc-link voltage. It is seen that the power factor angle (φ) and operating modulation index (m) are independent of P_{nom} and V_{dc} , whereas I_{dc} and I_{con} are proportional to $P_{\text{nom}}/V_{\text{dc}}$.

Table 4.1: Relationship between operating parameters and nominal real power and dc-link voltage

I_{dc}	I_{con}	θ_{con}	θ_{vcon}	$\varphi (= \theta_{\text{con}} - \theta_{\text{vcon}})$	m
Proportional to $P_{\text{nom}}/V_{\text{dc}}$	Proportional to $P_{\text{nom}}/V_{\text{dc}}$	Independent of P_{nom} and V_{dc}	Independent of P_{nom} and V_{dc}	Independent of P_{nom} and V_{dc}	Independent of P_{nom} and V_{dc}

The calculation to obtain the operating points shown above is suitable for VSCs, including regular MMCs and HC-MMCs. Based upon the steady-state operating point, the SM capacitor voltage ripple in MMCs is derived in the following section.

4.2 Derivations of SM capacitor voltage ripple

The conventional HB-MMC is taken as an example to show the underlying concepts to derive SM capacitor voltage ripple. Fig. 4.4 shows the one-phase schematic of a three-phase HB-MMC under normal operation, where R_{arm} is the equivalent resistance per arm. Each arm has $N \cdot (1+k_{\text{red}})$ SMs in series with a nominal capacitor voltage of V_{dc}/N , where N is the nominal number of SMs per arm and k_{red} is the SM redundancy ratio. Neglecting the converter's losses, the real power balance between dc and ac sides yields:

$$V_{\text{dc}} I_{\text{dc}} = 3 \frac{m V_{\text{dc}}}{2\sqrt{2}} I_{\text{con}} \cos(\varphi) \Rightarrow \cos(\varphi) = \frac{2\sqrt{2} I_{\text{dc}}}{3 I_{\text{con}} m} \quad (4.15)$$

where m is the operating modulation index, and φ is power factor angle.

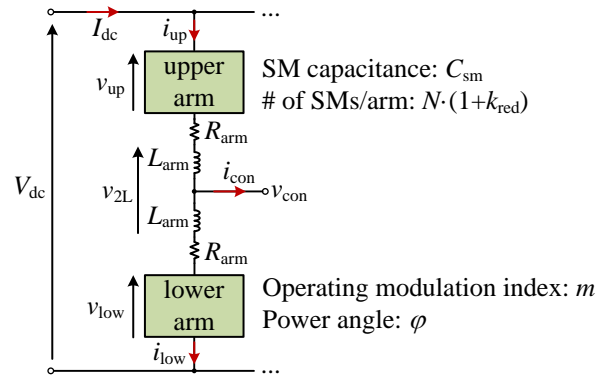


Fig. 4.4: Single-phase schematic diagram of HB-MMC under normal operation

SM capacitor voltage balancing strategies are required to provide all SMs with equal charge/discharge opportunities, resulting in approximately similar voltage ripples for all SM

capacitors within one arm. The voltage variation, ΔV , of a capacitor, C , is determined by its electric charge variation, ΔQ , i.e., $C \cdot \Delta V = \Delta Q$. Therefore,

$$\begin{aligned} (1+k_{\text{red}})NC_{\text{sm}}\Delta v_{\text{csmUp}}(t) &= \int Nm_{\text{up}}(t)i_{\text{up}}(t)dt \\ \Rightarrow \Delta v_{\text{csmUp}}(t) &= \frac{1}{(1+k_{\text{red}})C_{\text{sm}}} \cdot \int m_{\text{up}}(t)i_{\text{up}}(t)dt \end{aligned} \quad (4.16)$$

where $m_{\text{up}}(t)$ and $i_{\text{up}}(t)$ are the upper-arm modulation waveform and current, respectively, Δv_{csmUp} represents the instantaneous upper-arm SM capacitor voltage ripple, and C_{sm} is the capacitance used in each SM. Similarly, the SM capacitor voltage ripple of the lower arm is:

$$\Delta v_{\text{csmLow}}(t) = \frac{1}{(1+k_{\text{red}})C_{\text{sm}}} \cdot \int m_{\text{low}}(t)i_{\text{low}}(t)dt \quad (4.17)$$

where $m_{\text{low}}(t)$ and $i_{\text{low}}(t)$ are the lower-arm modulation waveform and current, respectively, and Δv_{csmLow} is the instantaneous lower-arm SM capacitor voltage ripple. Therefore, the actual SM capacitor voltages are as follows:

$$\begin{aligned} v_{\text{csmUp}}(t) &= V_{\text{dc}}/N + \Delta v_{\text{csmUp}}(t) \\ v_{\text{csmLow}}(t) &= V_{\text{dc}}/N + \Delta v_{\text{csmLow}}(t) \end{aligned} \quad (4.18)$$

Applying KVL to the dc-side loop (see Fig. 4.4) yields:

$$\begin{aligned} V_{\text{dc}} &= v_{\text{up}}(t) + v_{\text{low}}(t) + (i_{\text{up}}(t) + i_{\text{low}}(t))R_{\text{arm}} + v_{2L}(t) \\ &= m_{\text{up}}(t)Nv_{\text{csmUp}}(t) + m_{\text{low}}(t)Nv_{\text{csmLow}}(t) + (i_{\text{up}}(t) + i_{\text{low}}(t))R_{\text{arm}} + v_{2L}(t) \end{aligned} \quad (4.19)$$

As seen from Fig. 4.4, $v_{\text{up}}(t)$ and $v_{\text{low}}(t)$ are the voltage across the stack of SMs in the upper and lower arms, respectively, and $v_{2L}(t)$ is the voltage across two arm inductors. As seen from (4.16) and (4.17), the SM capacitor voltage ripple is influenced by the corresponding modulation waveform and arm current. The arm current shows different harmonic components between the

operations with and without CCSC. Without CCSC, the 2nd order ac power per phase leads to 2nd order harmonic in the arm currents. Therefore, for the operation without CCSC, the knowledge of 2nd harmonic current is necessary to investigate the SM capacitance selection given a certain ripple requirement.

4.2.1 Derivation of 2nd harmonic arm current without CCSC

In steady-state operation without CCSC, the arm currents primarily have dc, 1st, and 2nd harmonic components, and high order harmonics have negligible amounts [86] and are ignored in the following analysis. Assume that the 2nd harmonic arm current is denoted as

$$i_{2nd}(t) = I_{2nd} \cos(2\omega_o t + \theta_{2nd}) \quad (4.20)$$

As such the 2nd harmonic voltage across the two arm inductors, $v_{2L-2nd}(t)$, is as follows:

$$v_{2L-2nd}(t) = -4\omega_o L_{arm} I_{2nd} \sin(2\omega_o t + \theta_{2nd}) \quad (4.21)$$

and the upper- and lower-arm currents are as given below.

$$\begin{aligned} i_{up}(t) &= \frac{I_{dc}}{3} + \frac{\sqrt{2}I_{con}}{2} \sin(\omega_o t + \varphi) + I_{2nd} \cos(2\omega_o t + \theta_{2nd}) \\ i_{low}(t) &= \frac{I_{dc}}{3} - \frac{\sqrt{2}I_{con}}{2} \sin(\omega_o t + \varphi) + I_{2nd} \cos(2\omega_o t + \theta_{2nd}) \end{aligned} \quad (4.22)$$

The upper- and lower-arm modulation waveforms are denoted as follows:

$$m_{up}(t) = \frac{1}{2} \cdot (1 - m \sin(\omega_o t)), \quad m_{low}(t) = \frac{1}{2} \cdot (1 + m \sin(\omega_o t)) \quad (4.23)$$

Substituting (4.22)-(4.23) into (4.16)-(4.17), respectively, and using the relationship shown in (4.15), the upper- and lower-arm SM capacitor voltage ripples are as follows:

$$\Delta v_{\text{csmUp}}(t) = \frac{1}{(1+k_{\text{red}})\omega_o C_{\text{sm}}} \cdot \left[\begin{aligned} &I_{\text{dc}} m \cos(\omega_o t)/6 - \sqrt{2}I_{\text{con}} \cos(\omega_o t + \varphi)/4 + \sqrt{2}I_{\text{con}} m \sin(2\omega_o t + \varphi)/16 \\ &+ I_{2\text{nd}} \sin(2\omega_o t + \theta_{2\text{nd}})/4 + I_{2\text{nd}} m (\cos(3\omega_o t + \theta_{2\text{nd}})/3 - \cos(\omega_o t + \theta_{2\text{nd}}))/4 \end{aligned} \right] \quad (4.24)$$

$$\Delta v_{\text{csmLow}}(t) = \frac{1}{(1+k_{\text{red}})\omega_o C_{\text{sm}}} \cdot \left[\begin{aligned} &-I_{\text{dc}} m \cos(\omega_o t)/6 + \sqrt{2}I_{\text{con}} \cos(\omega_o t + \varphi)/4 + \sqrt{2}I_{\text{con}} m \sin(2\omega_o t + \varphi)/16 \\ &+ I_{2\text{nd}} \sin(2\omega_o t + \theta_{2\text{nd}})/4 - I_{2\text{nd}} m (\cos(3\omega_o t + \theta_{2\text{nd}})/3 - \cos(\omega_o t + \theta_{2\text{nd}}))/4 \end{aligned} \right] \quad (4.25)$$

These show that the SM capacitor voltage ripples have 1st, 2nd, and 3rd harmonics. Substituting (4.24) and (4.25) into (4.18), then (4.18) and (4.23) into (4.19), $v_{2L}(t)$ is expressed as follows:

$$v_{2L}(t) = -2R_{\text{arm}} \left(\frac{I_{\text{dc}}}{3} + I_{2\text{nd}} \cos(2\omega_o t + \theta_{2\text{nd}}) \right) + \frac{1}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \cdot \left[\begin{aligned} &I_{\text{dc}} m^2 \sin(2\omega_o t)/12 - 3\sqrt{2}I_{\text{con}} m \sin(2\omega_o t + \varphi)/16 \\ &-I_{2\text{nd}} \left(\frac{1}{4} + \frac{m^2}{6} \right) \sin(2\omega_o t + \theta_{2\text{nd}}) + \frac{m^2 I_{2\text{nd}}}{24} \sin(4\omega_o t + \theta_{2\text{nd}}) \\ &+ \sqrt{2}I_{\text{con}} m \sin(\varphi)/8 + I_{2\text{nd}} m^2 \sin(\theta_{2\text{nd}})/8 \end{aligned} \right] \quad (4.26)$$

where $C_{\text{eq}} = C_{\text{sm}}/N$. By equating the 2nd harmonic term in (4.26) and (4.21), the phase angle and magnitude of the 2nd harmonic current are obtained as shown in (4.27) and (4.28), respectively.

$$\tan(\theta_{2\text{nd}}) = \frac{4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} (1-m^2/3) + [8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - 1/2 - m^2/3] \tan(\varphi)}{[8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - 1/2 - m^2/3] (1-m^2/3) - 4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} \tan(\varphi)} \quad (4.27)$$

$$I_{2\text{nd}} = \frac{I_{\text{dc}}}{2} \cdot \frac{1-m^2/3}{[8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - 1/2 - m^2/3] \cos(\theta_{2\text{nd}}) + 4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} \sin(\theta_{2\text{nd}})} \quad (4.28)$$

Typically, R_{arm} can be neglected in high-voltage applications. With $R_{\text{arm}} = 0$, the phase angle and magnitude of the 2nd harmonic current can be simplified as expressed in (4.29) and (4.30).

$$\tan(\theta_{2\text{nd}}) = \frac{\tan(\varphi)}{1 - m^2/3} \quad (4.29)$$

$$I_{2\text{nd}} = \frac{I_{\text{dc}}}{2 \cos(\theta_{2\text{nd}})} \cdot \frac{1 - m^2/3}{8(1 + k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - 1/2 - m^2/3} \quad (4.30)$$

Note that for $\varphi = \pm 90^\circ$ (purely reactive power operation), $\theta_{2\text{nd}} = \pm 90^\circ$ and $I_{2\text{nd}} = 0$ due to $I_{\text{dc}} = 0$.

With the solved $I_{2\text{nd}}$ and $\theta_{2\text{nd}}$, the SM capacitor voltage ripple waveform can be obtained using (4.24) and (4.25). In [85], another solution for the 2nd harmonic arm current is shown, which assumes that the 2nd harmonic voltage across the two arm inductors is equally distributed among $2N$ SM capacitors. However, such assumption is not entirely valid, and the proof is shown below.

The magnitude of the 2nd harmonic of the SM capacitor voltage ripple may be approximated as in (4.31) by neglecting the small difference between φ and $\theta_{2\text{nd}}$ (see Fig. 4.8 (a) for validation).

$$V_{\text{csm-2nd}} \approx \frac{I_{\text{dc}} + 3I_{2\text{nd}} \cos(\varphi)}{12(1 + k_{\text{red}})\omega_o C_{\text{sm}} \cos(\varphi)} \quad (4.31)$$

Therefore, according to (4.21), the relationship between $V_{2L-2\text{nd}}$ and the total 2nd harmonic voltage of $2N$ SMs is as follows:

$$\frac{V_{2L-2\text{nd}}}{2N \cdot V_{\text{csm-2nd}}} \approx \frac{12 \sin(\varphi) / \sin(\theta_{2\text{nd}})}{8 + \frac{3 \sin(\varphi) / (2 \sin(\theta_{2\text{nd}})) - 1/2 - m^2/3}{(1 + k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}}}} \quad (4.32)$$

It can be observed that the relationship between $V_{2L-2\text{nd}}$ and $2N \cdot V_{\text{csm-2nd}}$ depends on the operating point (φ and m) and system parameters (L_{arm} , C_{eq} , ω_o , and k_{red}). At a given operating point, $V_{2L-2\text{nd}} / (2N \cdot V_{\text{csm-2nd}})$ increases when k_{red} , L_{arm} , or C_{eq} increases; as such there is no inherent mechanism to ensure that the 2nd harmonic voltage across the two arm inductors is equally distributed among $2N$ SM capacitors, as assumed in [85]. Comparisons of simulation and

experimental results of the 2nd harmonic calculation method presented in this thesis and that in [85] are made in Section 4.2.3.

4.2.2 Derivation of the control output from CCSC

With CCSC, the arm currents primarily have dc and fundamental components, i.e., $I_{2nd} = 0$ in (4.22). CCSC strategies essentially adjust the modulation waveforms of the upper and lower arms with the aim of eliminating the 2nd harmonic in the arm current. Denoting the compensation variable as v_z , the arm modulation waveforms in (4.23) are modified as follows:

$$m_{up}(t) = \frac{1}{2}(1 - m \sin(\omega_o t) - v_z(t)), \quad m_{low}(t) = \frac{1}{2}(1 + m \sin(\omega_o t) - v_z(t)) \quad (4.33)$$

Compared to the fundamental component of the modulation waveform, v_z is generally much smaller and can be neglected in calculating the SM capacitor voltage ripple. As such, the upper-arm and lower-arm SM capacitor voltage ripples are retained similar to those in (4.24) and (4.25) but with $I_{2nd} = 0$. Thus, the SM capacitor voltage ripples only contain 1st and 2nd harmonics.

To calculate v_z , substitute (4.24) and (4.25) with $I_{2nd} = 0$ into (4.18), and then (4.18) and (4.33) into (4.19); thus:

$$v_{2L}(t) = V_{dc}v_z(t) - 2R_{arm}I_{dc}/3 + \frac{1}{(1+k_{red})\omega_o C_{eq}} \cdot \left[\frac{I_{dc}m^2 \sin(2\omega_o t)/12 - 3\sqrt{2}I_{con}m \sin(2\omega_o t + \varphi)/16}{+\sqrt{2}I_{con}m \sin(2\omega_o t + \varphi)v_z(t)/16 + \sqrt{2}I_{con}m \sin(\varphi)/8} \right] \quad (4.34)$$

If the 2nd harmonic in the arm currents is eliminated, the 2nd harmonic voltage across the two arm inductors will disappear too. In general, $v_z(t)$ primarily includes only 2nd harmonic to cancel the 2nd harmonic term in (4.34). As such, the second last term in (4.34) results in dc and 4th harmonic. Let the 2nd harmonic of $v_{2L}(t)$ expressed in (4.34) be zero, and $v_z(t)$ is obtained as follows:

$$v_z(t) = \frac{-I_{dc} m^2 \sin(2\omega_o t)/12 + 3\sqrt{2} I_{con} m \sin(2\omega_o t + \varphi)/16}{(1+k_{red}) \omega_o C_{eq} V_{dc}} \quad (4.35)$$

After simplification, the magnitude and phase angle of $v_z(t) = V_z \cdot \sin(2\omega_o t + \theta_{vz})$ are obtained as:

$$\tan(\theta_{vz}) = \frac{\tan(\varphi)}{1 - m^2/3} \quad (4.36)$$

$$V_z = \frac{I_{dc}}{4(1+k_{red}) \omega_o C_{eq} V_{dc}} \sqrt{(1 - m^2/3)^2 + \tan(\varphi)^2} \quad (4.37)$$

It is observed that θ_{vz} is independent of SM capacitance, whereas V_z is inversely proportional to $(1+k_{red}) \cdot \omega_o \cdot C_{eq}$ and proportional to I_{dc}/V_{dc} , which is equal to $P_{ref} P_{nom}/V_{dc}^2$. In practice, $v_z(t)$ is obtained by a closed-loop control system by regulating the 2nd harmonic component of the circulating current to zero.

4.2.3 Validation of the voltage ripple and 2nd harmonic current

To validate the theoretical analysis of SM capacitor voltage ripple and the 2nd harmonic in the arm current, comparisons between the theoretical results and both EMT simulations and experimental results are made and shown in the following subsections, where the theoretical calculations ignore the high-order harmonics due to their negligible contribution to the 2nd harmonic and capacitor voltage ripple [86].

4.2.3.1 Validation against EMT simulations

The simulated system of HB-MMC is shown in Fig. 4.5, where the PCC is controlled as a PV bus. System parameters are listed in Table 4.2. Two SM redundancy ratios (0% and 10%) are simulated both with and without CCSC. The equivalent arm resistance is primarily determined by semiconductor ON resistance values. The simulated system has a resistance of $100 \times 5 \text{ m}\Omega = 0.5 \text{ }\Omega$

per arm. The voltage across the equivalent arm resistance is small in a 500-kV application. As such, the theoretical results shown in this subsection are obtained by neglecting the arm resistance.

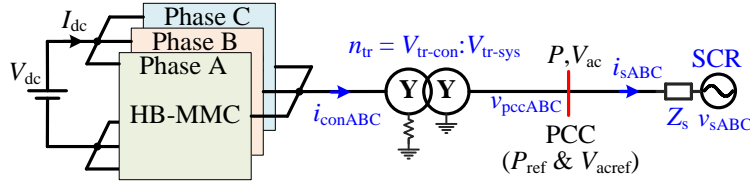


Fig. 4.5: Schematic diagram of the simulated HB-MMC

Table 4.2: System parameters for EMT simulations

DC side: 500 MW, 500 kV	AC side: 230 kV, 60 Hz, and SCR = $3.0 \angle 80^\circ$	
Transformer: 290 kV: 230 kV (conv./sys.), 600 MVA with 6% leakage	Arm inductance: 0.05 H	
Nominal # of SMs/arm: 100	SM redundancy ratio: 0% and 10%	SM capacitance: 2.5 mF
Semiconductor (switch and diode) ON resistance: 5 m Ω		

Fig. 4.6 shows theoretical and simulation waveforms of the HB-MMC under rated conditions ($P_{\text{ref}} = 1.0$ pu, and $V_{\text{acref}} = 1.0$ pu). According to the analysis shown in Section 4.1, the nominal operating point is theoretically calculated as $I_{\text{dc}} = 1.0$ kA (see (4.2)), $I_{\text{con}} = 1.0$ kA (see (4.6)), $\varphi = -2.46^\circ$ (see (4.13)), and $m = 0.948$ (see (4.14)). According to the calculated operating point, theoretical upper-arm modulation and current waveforms are shown in Fig. 4.6 (a), which are used to calculate the upper-arm SM capacitor voltage ripples (see (4.16)). The comparison between the theoretical and simulation results of the SM capacitor voltage ripple waveforms is displayed in Fig. 4.6 (b). It is observed that with or without CCSC, the theoretical and simulation results of the instantaneous SM capacitor voltage ripple waveforms closely match for both 0% and 10% SM redundancies. The comparison of SM capacitor voltage ripple values between the theoretical and simulation results under various operating conditions is displayed in Fig. 4.7. It is observed that with $V_{\text{acref}} = 0.9$ pu, the power factor angle varies within $[6^\circ, 28.0^\circ]$, and the theoretical and simulation results of the SM capacitor voltage ripple values are well matched. These validate the accuracy of the method to derive the SM capacitor voltage ripple presented in Section 4.2.

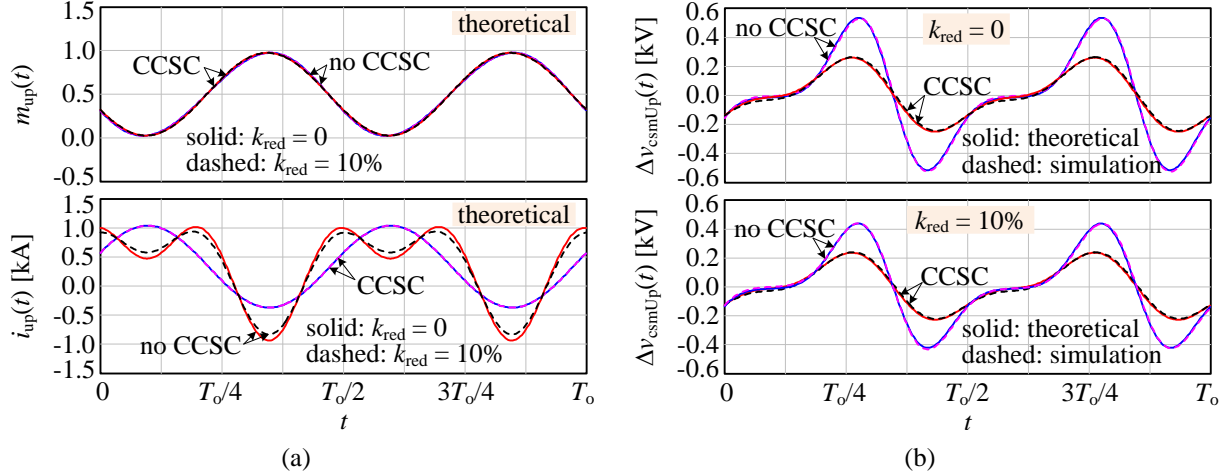


Fig. 4.6: Theoretical and simulation results of HB-MMC under $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$ pu

(a) theoretical upper-arm modulation waveforms and currents; (b) theoretical and simulation results of Δv_{csmUp} with 0% and 10% redundancies.

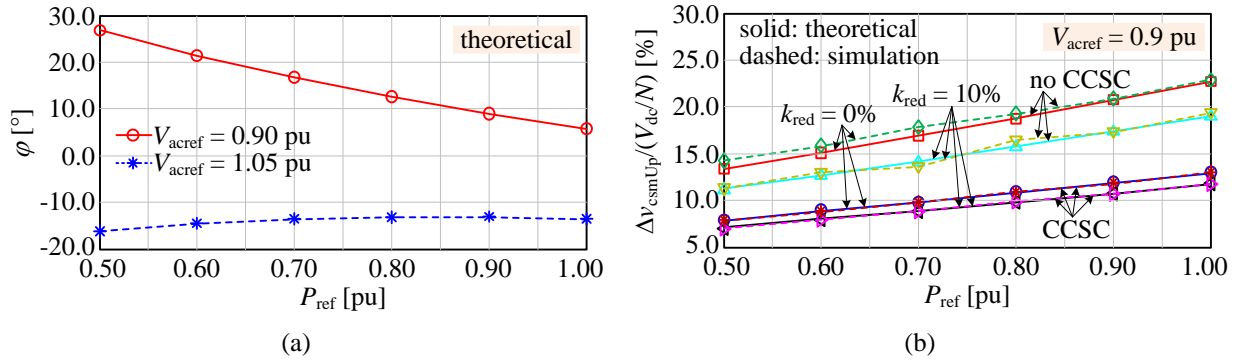


Fig. 4.7: Theoretical power factor angles and SM capacitor voltage ripple values under various operating conditions (a) theoretical power factor angles; (b) theoretical and simulation results of SM capacitor voltage ripple values.

Fig. 4.8 shows the theoretical results of $(\varphi - \theta_{2\text{nd}})$ and $V_{2\text{L-}2\text{nd}}/(2N \cdot V_{\text{csm-}2\text{nd}})$ as shown in (4.32). It is observed in Fig. 4.8 (a) that $|\varphi - \theta_{2\text{nd}}|$ is less than 6.0° , resulting in $\cos(\varphi - \theta_{2\text{nd}}) \approx 1.0$ under various operating points ($V_{\text{acref}} = 0.8$ pu to 1.05 pu and $P_{\text{ref}} = 0.5$ pu to 1.0 pu). Therefore, it is reasonable to obtain (4.31) by neglecting the difference between φ and $\theta_{2\text{nd}}$. As seen from Fig. 4.8 (b), the ratio between the 2nd harmonic voltage across the two arm inductors and that of $2N$ SM capacitor voltage ripples varies with operating points and is in the range of $[0.89, 0.91]$ under the considered operating conditions. This demonstrates the inaccuracy of the assumption of $V_{2\text{L-}2\text{nd}}/(2N \cdot V_{\text{csm-}2\text{nd}}) = 1.0$ used in [85].

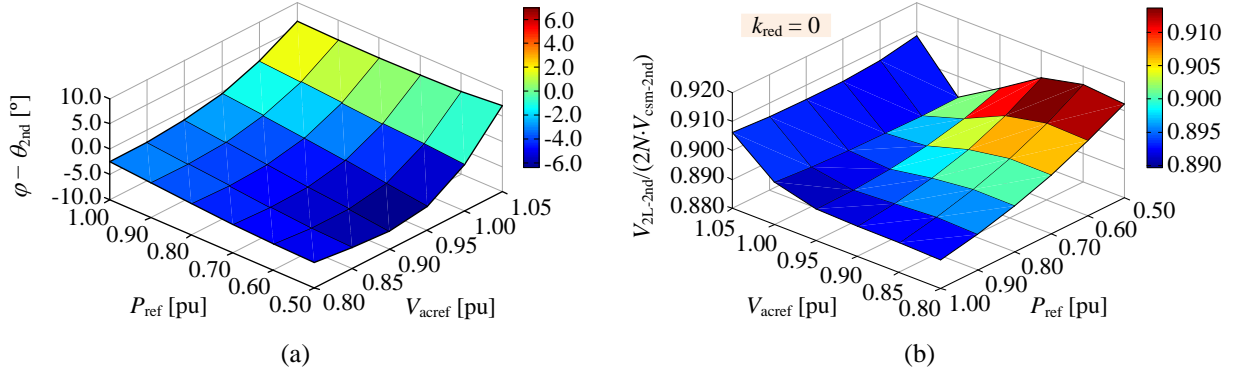


Fig. 4.8: Theoretical results of φ and $V_{2L-2nd}/(2N \cdot V_{csm-2nd})$
(a) $\varphi - \theta_{2nd}$; (b) $V_{2L-2nd}/(2N \cdot V_{csm-2nd})$.

The comparisons between the theoretical and simulation results of I_{2nd} , θ_{2nd} , V_z , and θ_{vz} are displayed in Fig. 4.9. The power factor angle φ (determined by P_{ref} and V_{acref}) from simulation is shown in Fig. 4.7 (a) for $V_{acref} = 0.9$ pu and 1.05 pu, and its is approximately $[-20^\circ, 30^\circ]$.

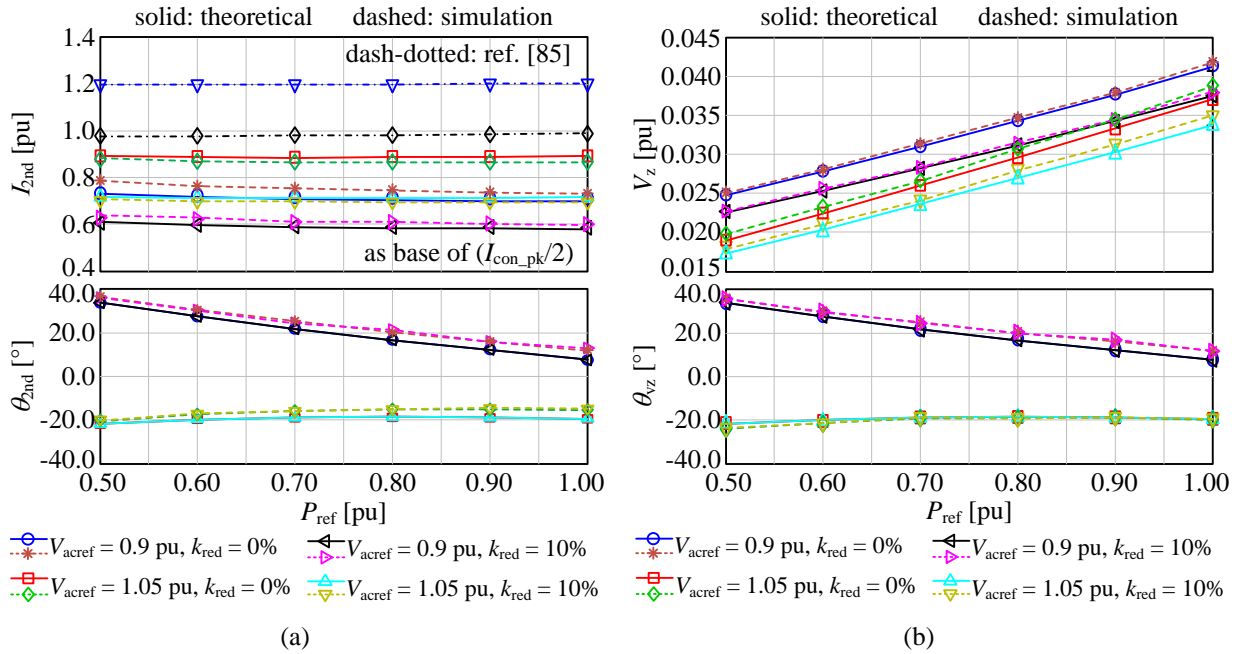


Fig. 4.9: Comparison of the theoretical and simulation results of I_{2nd} , θ_{2nd} , V_z and θ_{vz}
(a) results of I_{2nd} and θ_{2nd} ; (b) results of V_z and θ_{vz} .

As seen from Fig. 4.9 (b), the per-unit values of I_{2nd} (using $I_{con_pk}/2.0$ as the base) obtained by the theoretical calculation shown in Section 4.2.1 closely match those from EMT simulations for

both SM redundancy ratios and with or without CCSC. However, I_{2nd} values calculated from the method in [85] are much higher than those from EMT simulations. In addition, [85] does not provide any provisions for calculating the 2nd harmonic component including SM redundancies. Therefore, the calculation method of 2nd harmonic current described in Section 4.2.1 is more accurate than the existing method [85] and includes provisions for SM redundancy. As seen from Fig. 4.9 (b), the theoretical results of θ_{2nd} , V_z , and θ_{vz} are also close to those obtained from simulation results.

4.2.3.2 Validation against experimental tests

The specifications of the experimental setup are listed in Table 4.3, and Fig. 4.10 shows the equivalent ac circuit used to theoretically calculate the operating points. Comparisons of the results of the 2nd harmonic specifications under three loads are summarized in Table 4.4.

Table 4.3: System parameters of the experimental setup

V_{dc} : 300 V	f_o : 60 Hz	L_{arm} : 2.5 mH	C_{sm} : 5.0 mF	N : 10/arm
R_{arm} : 0.7 Ω	k_{red} : 0%	m : 0.8	Modulation method: PD-PWM	
Load 1: $R_{load} = 12 \Omega$	Load 2: $R_{load} = 12 \Omega$, $L_{load} = 8.4$ mH, $r_{Lload} = 0.4 \Omega$		Load 3: $R_{load} = 12 \Omega$, $L_{load} = 12.6$ mH, $r_{Lload} = 0.6 \Omega$	

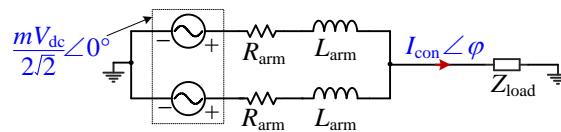


Fig. 4.10: Equivalent ac circuit to calculate the operating point

Table 4.4: Comparison of theoretical and experimental results

Load (power angle)	I_{2nd} [A] (relative error to the experimental value)			
	Experiment	Proposed method		Method in [85]
		R_{arm} included	R_{arm} excluded	
Load 1 ($\varphi = -2.2^\circ$)	2.34	2.52 (7.7%)	3.14 (34.2%)	4.48 (91.5%)
Load 2 ($\varphi = -16.0^\circ$)	2.33	2.39 (2.6%)	3.00 (28.8%)	4.15 (78.1%)
Load 3 ($\varphi = -22.0^\circ$)	2.35	2.31 (-1.7%)	2.88 (22.6%)	3.94 (67.7%)

As seen in Table 4.4, I_{2nd} calculated by the method in [85] has much higher relative errors (up to 91.5%). With the proposed method in Section 4.2.1 and neglecting R_{arm} , the results of I_{2nd} also show large differences to the experimental results (up to 34.2%). However, these differences are significantly reduced by considering R_{arm} . This shows that in low-voltage (< 10 kV) applications, R_{arm} needs to be considered for improved accuracy in calculating the 2nd harmonic current. The experimental and theoretical results of currents and average SM capacitor voltage ripple for loads 1 and 2 are shown in Fig. 4.11. It shows that the theoretical waveforms match well with the experimental results, which further confirms the accuracy of the method developed in Section 4.2.1.

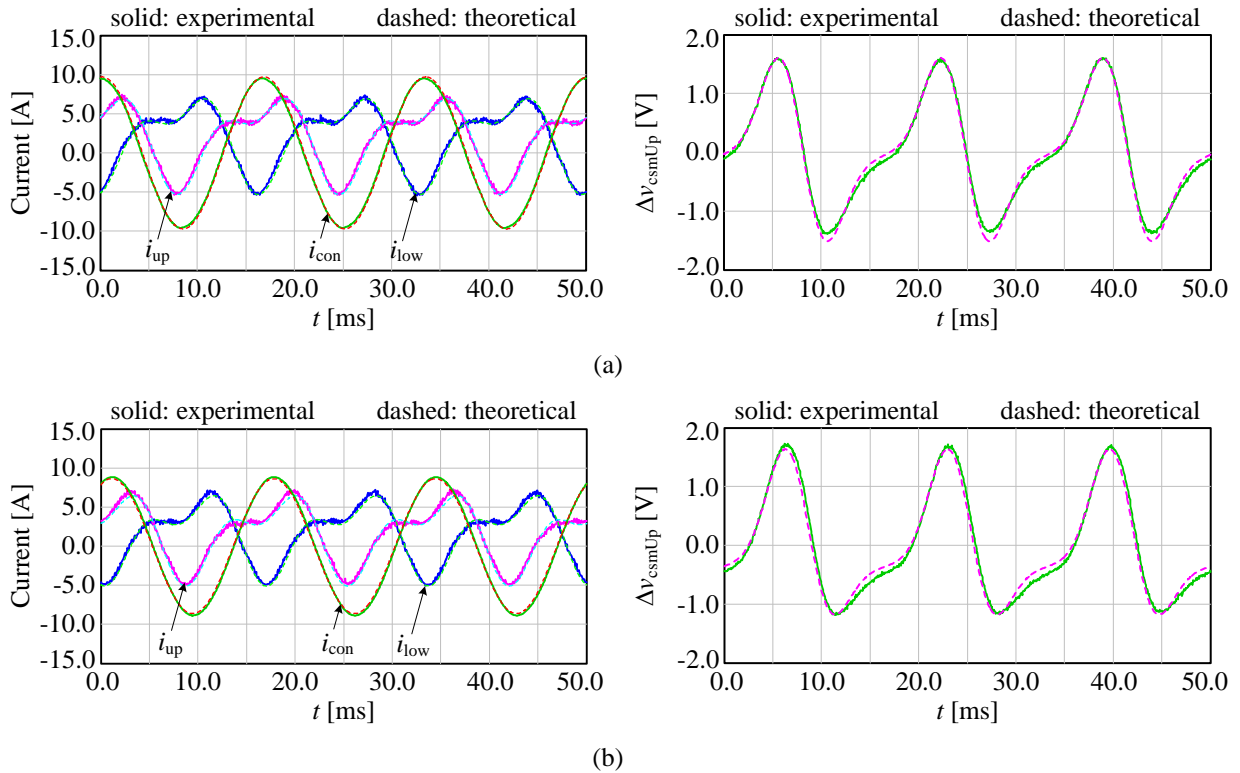


Fig. 4.11: Experimental and theoretical results of phase and arm currents, and average SM capacitor voltage ripple (a) load 1; (b) load 2.

4.3 Capacitor sizing of HC-MMCs under normal operation

Based upon the calculation of operating point shown in Section 4.1 and the analysis of SM capacitor voltage ripple for conventional HB-MMC shown in Section 4.2, the SM capacitor sizing of the original and mixed-SM HC-MMCs will be analyzed in the following subsections. Since the upper and lower arms operate symmetrically, only the operation of the upper arm is analyzed.

4.3.1 Capacitor design of the main power stage in the original HC-MMC

Since the main power stage in the original HC-MMC is identical to a conventional HB-MMC, the analyses of SM capacitor voltage ripple and the 2nd harmonic in arm currents shown in Section 4.2 remain suitable for the original HC-MMC.

4.3.1.1 Capacitor sizing of the main power stage with CCSC

The upper-arm modulation waveform and current with CCSC are expressed as follows:

$$\begin{aligned} m_{\text{up}}(t) &= \frac{1}{2} \left(1 - m \sin(\omega_o t) - k_{3\text{rd}} m \sin(3\omega_o t) \right) \\ i_{\text{up}}(t) &= \frac{I_{\text{dc}}}{3} + \frac{\sqrt{2} I_{\text{con}}}{2} \sin(\omega_o t + \varphi) \end{aligned} \quad (4.38)$$

where the small amount of 2nd harmonic controlled by CCSC in the modulation waveform is neglected, and $k_{3\text{rd}}$ is the amount of injected 3rd harmonic if applicable. Generally, $k_{3\text{rd}}$ is selected as 1/6 to obtain the maximum extended linear range. If no 3rd harmonic is injected, $k_{3\text{rd}} = 0$ in the following discussions.

Similar to the derivation of SM capacitor voltage ripple shown in (4.16), the instantaneous voltage ripple of the upper-arm HB-SM capacitor in the main power stage of the original HC-MMC, $\Delta v_{\text{chbUp}}(t)$, is analyzed as follows:

$$\begin{aligned}
(1+k_{\text{red}})N_h C_{\text{hb}} \Delta v_{\text{chbUp}}(t) &= \int m_{\text{up}}(t) \cdot N_h \cdot i_{\text{up}}(t) dt \\
\Rightarrow \Delta v_{\text{chbUp}}(t) &= \frac{1}{(1+k_{\text{red}})C_{\text{hb}}} \cdot q_{\text{up}}(t)
\end{aligned} \tag{4.39}$$

where C_{hb} is the HB SM capacitance, N_h is the nominal number of HB SMs per arm in the main power stage, and k_{red} is the SM redundancy ratio. With the relationship shown in (4.15), the instantaneous electric charge, $q_{\text{up}}(t)$, is calculated as follows:

$$\begin{aligned}
q_{\text{up}}(t) &= \frac{I_{\text{dc}} m}{6\omega_o} \cos(\omega_o t) - \frac{I_{\text{dc}}}{3\omega_o m \cos(\varphi)} \cos(\omega_o t + \varphi) + \frac{I_{\text{dc}}}{12\omega_o \cos(\varphi)} \sin(2\omega_o t + \varphi) \\
&+ k_{3\text{rd}} \left[\frac{I_{\text{dc}} m}{18\omega_o} \cos(3\omega_o t) - \frac{I_{\text{dc}}}{6\omega_o \cos(\varphi)} \left(\frac{1}{2} \sin(2\omega_o t - \varphi) - \frac{1}{4} \sin(4\omega_o t + \varphi) \right) \right]
\end{aligned} \tag{4.40}$$

where it is seen that $q_{\text{up}}(t)$ is independent of SM capacitance.

Fig. 4.12 shows typical waveforms in the upper arm for the operation with CCSC. As seen from (4.39) and Fig. 4.12, the SM capacitor voltage ripple is increased when $m_{\text{up}}(t) \cdot i_{\text{up}}(t) > 0$, and vice versa. Generally, the operating modulation index (m) is less than 1.0 (or 1.15 if 3rd harmonic is injected) to avoid overmodulation. In other words, the range of the modulation waveform is within $[-1, 1]$, resulting in $m_{\text{up}}(t) > 0$ over the entire fundamental period. Therefore, the charging and discharging intervals for SM capacitors can be determined by the polarity of $i_{\text{up}}(t)$ only.

Let $i_{\text{up}}(t)$ shown in (4.38) be equal to zero, and the critical angles to divide the charging and discharging intervals are obtained as follows:

$$\theta_{\text{iup1}} = \pi + \theta_0 - \varphi, \quad \theta_{\text{iup2}} = 2\pi - \theta_0 - \varphi \tag{4.41}$$

where

$$\theta_0 = \sin^{-1} \left(\frac{2I_{\text{dc}}}{3\sqrt{2}I_{\text{con}}} \right) = \sin^{-1} \left(\frac{m \cos(\varphi)}{2} \right) = \sin^{-1} \left(\frac{m_{\text{rated}} P_{\text{ref}}}{2\sqrt{2}X_0} \right) \tag{4.42}$$

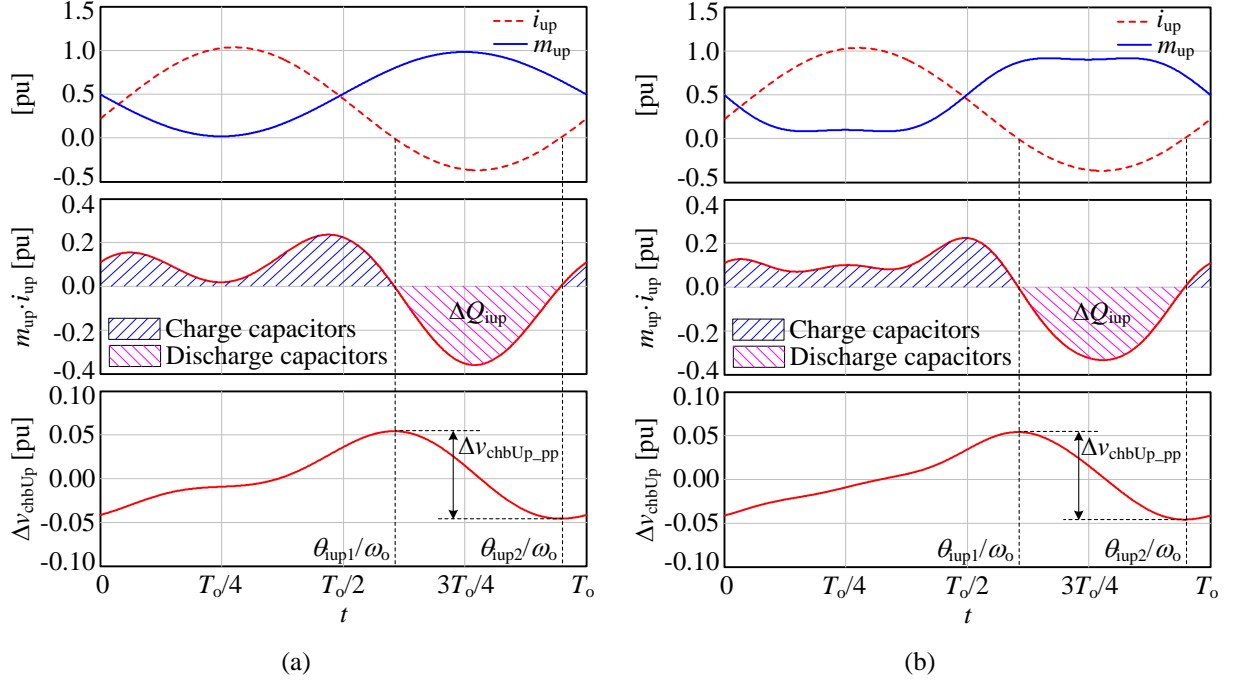


Fig. 4.12: Upper-arm modulation, current and HB-SM capacitor voltage ripple waveforms in the original HC-MMC operating with CCSC

(a) without 3rd harmonic injection ($k_{3rd} = 0$); (b) with 3rd harmonic injection ($k_{3rd} = 1/6$).

Then the SM capacitor voltage ripple value, ΔV_{chbUp_pp} , is obtained by calculating the accumulated charge value, ΔQ_{iup} , within $[\theta_{iup1}, \theta_{iup2}]$, and expressed as follows:

$$\Delta V_{chbUp_pp} = \frac{1}{(1+k_{red})C_{hb}} \cdot \Delta Q_{iup} = \frac{I_{dc}}{(1+k_{red})\omega_o C_{hb}} \Delta Q_{iup0} \quad (4.43)$$

where

$$\Delta Q_{iup0} = \left| \begin{aligned} & \left(\frac{m \cos(\varphi)}{3} - \frac{2}{3m \cos(\varphi)} \right) \cos(\theta_0) - \frac{1}{6} \sin(2\theta_0) \\ & + k_{3rd} \cos(3\varphi) \cdot \left(\frac{m}{9} \cos(3\theta_0) + \frac{1}{6 \cos(\varphi)} \left(\sin(2\theta_0) - \frac{1}{2} \sin(4\theta_0) \right) \right) \end{aligned} \right| \quad (4.44)$$

If the maximum allowed capacitor voltage ripple is denoted by K_{ripple} in per-unit based upon the SM capacitor's nominal voltage (i.e., V_{dc}/N_h for the HB SMs in the main power stage).

Therefore, the minimum equivalent SM capacitance ($C_{\text{eq}} = C_{\text{hb}}/N_{\text{h}}$) is obtained using $\Delta v_{\text{chbUp_pp}} \leq K_{\text{ripple}} \cdot V_{\text{dc}}/N_{\text{h}}$ as follows:

$$C_{\text{eq}} = \frac{C_{\text{hb}}}{N_{\text{h}}} \geq \frac{I_{\text{dc}}}{(1+k_{\text{red}})\omega_o K_{\text{ripple}} V_{\text{dc}}} \Delta Q_{\text{iup0}} \quad (4.45)$$

With (4.45) and the expression of $I_{\text{dc}} = P_{\text{ref}} \cdot P_{\text{nom}}/V_{\text{dc}}$, the stored energy of all the HB-SM capacitors in the main power stage of a three-phase HC-MMC per power rating unit, EoP_{HBmain} , is calculated as follows:

$$\begin{aligned} EoP_{\text{HBmain}} &= \frac{6(1+k_{\text{red}})N_{\text{h}} \cdot C_{\text{hb}} \cdot (V_{\text{dc}}/N_{\text{h}})^2/2}{P_{\text{nom}}} \times 10^3 \\ &= \frac{3(1+k_{\text{red}})C_{\text{eq}}V_{\text{dc}}^2}{P_{\text{nom}}} \times 10^3 \geq \frac{3P_{\text{ref}}\Delta Q_{\text{iup0}}}{\omega_o K_{\text{ripple}}} \times 10^3 \text{ [kJ/MVA]} \end{aligned} \quad (4.46)$$

As seen from (4.44), ΔQ_{iup0} is independent of P_{nom} , V_{dc} , K_{ripple} , k_{red} , C_{eq} and ω_o , and is related to m_{rated} , $X_{\text{TR}}/S_{\text{TR}}$, X_{Larm} , P_{ref} , and V_{acref} . Therefore, EoP_{HBmain} is not influenced by P_{nom} , V_{dc} , and k_{red} , and is inversely proportional to K_{ripple} and the fundamental frequency.

In practice, the SM capacitance is generally selected under nominal operating conditions (i.e., $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$) and without considering redundant SMs (i.e., $k_{\text{red}} = 0$). This ensures that under nominal operation with $k_{\text{red}} \cdot N_{\text{h}}$ redundant SMs, the SM capacitor voltage ripple is still within the required bounds even with a certain number ($\leq k_{\text{red}} \cdot N_{\text{h}}$) of SMs faulted and bypassed. After the SM capacitance is selected based upon nominal conditions without redundancy, the actual stored energy of all HB-SM capacitors is increased by k_{red} times when $k_{\text{red}} \cdot N_{\text{h}}$ redundant SMs are added. If $k_{\text{flt}} \cdot N_{\text{h}}$ SMs are bypassed due to SM faults, where k_{flt} is the ratio of the number of faulted SMs over N_{h} and $0 \leq k_{\text{flt}} \leq k_{\text{red}}$, ΔQ_{iup0} is not influenced (see (4.44)) and C_{eq} ($= C_{\text{hb}}/N_{\text{h}}$) is unchanged because the SM capacitance has been already selected. Therefore, the actual

capacitor voltage ripple in operation with the equivalent redundancy ratio of $(k_{\text{red}} - k_{\text{flt}})$ is given as follows:

$$K_{\text{ripple-SMflt}} = \frac{I_{\text{dc}}}{(1 + k_{\text{red}} - k_{\text{flt}})\omega_o C_{\text{eq}}} \Delta Q_{\text{iup}0} = \frac{1}{1 + k_{\text{red}} - k_{\text{SMflt}}} K_{\text{ripple}} \quad (4.47)$$

where K_{ripple} is the normalized SM capacitor voltage ripple value under nominal operating conditions and with no redundant SMs. It is seen that if there are no faulted SMs, the SM capacitor voltage ripple is reduced with the redundancy ratio increased. However, a large redundancy ratio results in high losses in the converter.

4.3.1.2 Capacitor sizing of the main power stage without CCSC

The upper-arm modulation waveform and current without CCSC are expressed as follows:

$$\begin{aligned} m_{\text{up}}(t) &= \frac{1}{2} (1 - m \sin(\omega_o t) - k_{3\text{rd}} m \sin(3\omega_o t)) \\ i_{\text{up}}(t) &= \frac{I_{\text{dc}}}{3} + \frac{\sqrt{2} I_{\text{con}}}{2} \sin(\omega_o t + \varphi) + I_{2\text{nd}} \cos(2\omega_o t + \theta_{2\text{nd}}) \end{aligned} \quad (4.48)$$

The detailed derivation and analysis of the 2nd harmonic with 3rd harmonic injection is shown in Appendix A.1. It is proven that the influence of the 3rd harmonic injection on the 2nd harmonic current amount is overly complicated and is negligible for the most part. Therefore, in the following theoretical analysis the influence of the 3rd harmonic injection on the 2nd harmonic current is neglected, and the 2nd harmonic current specifications ($\theta_{2\text{nd}}$ and $I_{2\text{nd}}$) in (4.48) are used the same as those without 3rd harmonic injection as shown in (4.29) and (4.30), respectively.

Similar to the analysis in Section 4.3.1.1, the upper-arm instantaneous electric charge is calculated as follows:

$$\begin{aligned}
q_{\text{up}}(t) &= \int m_{\text{up}}(t) \cdot i_{\text{up}}(t) dt \\
&= \frac{I_{\text{dc}} m}{6\omega_o} \cos(\omega_o t) - \frac{I_{\text{dc}}}{3\omega_o m \cos(\varphi)} \cos(\omega_o t + \varphi) + \frac{I_{\text{dc}}}{12\omega_o \cos(\varphi)} \sin(2\omega_o t + \varphi) \\
&\quad + \frac{I_{2\text{nd}}}{4\omega_o} \left[\sin(2\omega_o t + \varphi) + m \left(-\cos(\omega_o t + \varphi) + \frac{1}{3} \cos(3\omega_o t + \varphi) \right) \right] \\
&\quad + k_{3\text{rd}} \left[\frac{I_{\text{dc}} m}{18\omega_o} \cos(3\omega_o t) - \frac{I_{\text{dc}}}{6\omega_o \cos(\varphi)} \left(\frac{1}{2} \sin(2\omega_o t - \varphi) - \frac{1}{4} \sin(4\omega_o t + \varphi) \right) \right] \\
&\quad + \frac{I_{2\text{nd}} m}{4\omega_o} \left(\frac{1}{5} \cos(5\omega_o t + \varphi) + \cos(\omega_o t - \varphi) \right)
\end{aligned} \tag{4.49}$$

where $I_{2\text{nd}}$ shown in (4.30) is related to the equivalent SM capacitance, i.e., $C_{\text{eq}} = C_{\text{hb}}/N_{\text{h}}$.

Typical upper-arm waveforms for the operation without CCSC are shown in Fig. 4.13. It is seen that the charging and discharging intervals for SM capacitors are determined by $i_{\text{up}}(t)$ due to $m_{\text{up}}(t) > 0$ over the entire fundamental period.

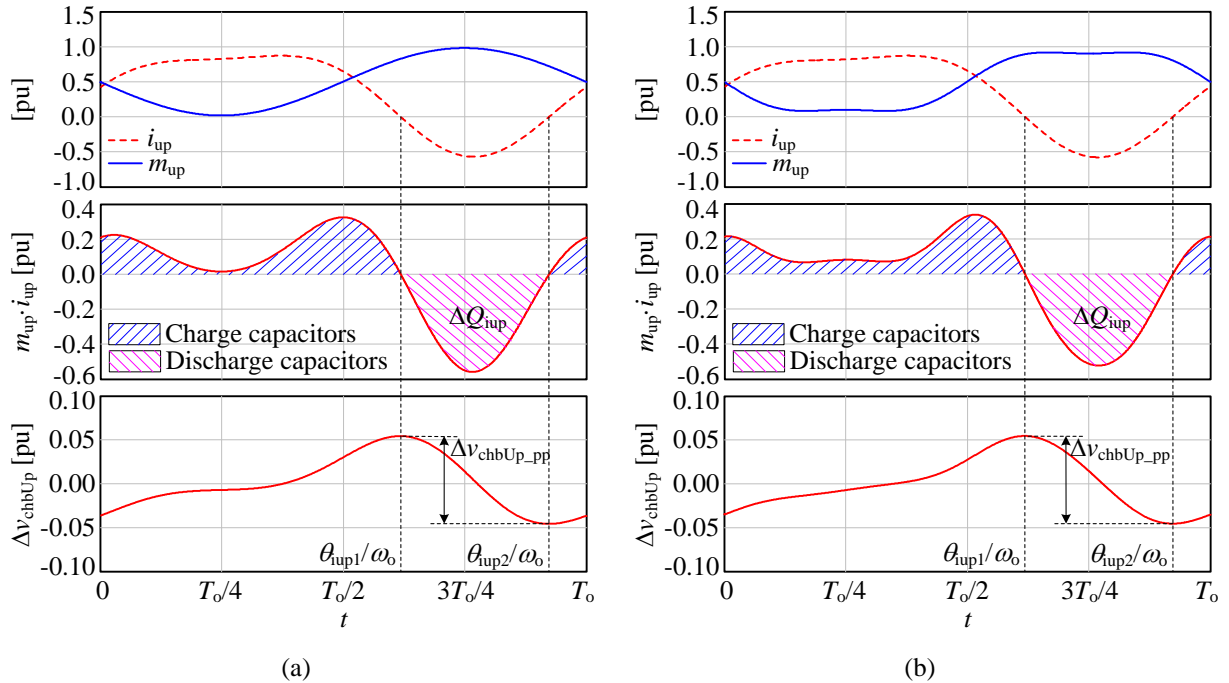


Fig. 4.13: Upper-arm modulation wave, current, and HB-SM voltage ripple waveforms in the original HC-MMC operating without CCSC

(a) without 3rd harmonic injection ($k_{3\text{rd}} = 0$); (b) with 3rd harmonic injection ($k_{3\text{rd}} = 1/6$).

However, $i_{up}(t)$ shown in (4.48) is overly complicated to find the explicit solutions of critical angles θ_{up1} and θ_{up2} to meet $i_{up}(\theta_{upj}/\omega_b) = 0$, where $j = 1$ and 2 . Therefore, a computer-aided method is recommended to solve $i_{up}(t) = 0$. As seen from (4.39), the SM capacitor voltage ripple is related to SM capacitance and electric charge $q_{up}(t)$, and $q_{up}(t)$ is related to I_{2nd} and hence SM capacitance (see (4.30)). Therefore, an iterative method is recommended to find the SM capacitance to meet a certain ripple requirement.

Assuming $C_{eq} = K_0 \cdot P_{nom} / [(1+k_{red}) \cdot \omega_b \cdot V_{dc}^2]$ and substituting C_{eq} and the expression of L_{arm} shown in (4.4) into (4.30), the magnitude of the 2nd harmonic current is modified as

$$I_{2nd} = \frac{I_{dc}}{2 \cos(\theta_{2nd})} \cdot \frac{1 - m^2/3}{3m_{rated}^2 X_{Larm} K_0 - 1/2 - m^2/3} \quad (4.50)$$

The operating modulation index (m) is less than 1.0 or 1.15, depending on whether or not 3rd harmonic injection is used. This results in $1 - m^2/3 > 0$. As such, to obtain the magnitude of the 2nd harmonic current $I_{2nd} \geq 0$, it needs to ensure that

$$3m_{rated}^2 X_{Larm} K_0 - 1/2 - m^2/3 \geq 0 \Rightarrow K_0 \geq \frac{1/2 + m^2/3}{3m_{rated}^2 X_{Larm}} \quad (4.51)$$

The iterative method to find K_0 to meet the ripple requirement is described as follows:

- (i) Set the initial range of K_0 within $[K_{0min}, K_{0max}]$, where K_{0min} satisfies (4.51);
- (ii) With K_0 respectively equal to K_{0min} and K_{0max} ,
 - (a) Calculate $C_{eq} = K_0 \cdot P_{nom} / [(1+k_{red}) \cdot \omega_b \cdot V_{dc}^2]$, then I_{2nd} and θ_{2nd} ;
 - (b) Calculate the critical angles of θ_{up1} and θ_{up2} by solving $i_{up}(t) = 0$;

(c) Calculate the accumulated charge within $[\theta_{\text{up}1}, \theta_{\text{up}2}]$ as $\Delta Q_{\text{iup}} = |q_{\text{up}}(\theta_{\text{up}2}/\omega_o) - \Delta q_{\text{up}}(\theta_{\text{up}1}/\omega_o)|$ with $q_{\text{up}}(t)$ shown in (4.49);

(d) According to the ripple requirement of $\Delta v_{\text{chbUp_pp}} \leq K_{\text{ripple}} \cdot V_{\text{dc}}/N_h$, calculate the capacitor voltage ripple using $K_{\text{ripple}0} = \Delta Q_{\text{iup}}/[(1+k_{\text{red}}) \cdot C_{\text{eq}} \cdot V_{\text{dc}}]$;

(iii) Compare the calculated voltage ripple $K_{\text{ripple}0}$ with the target ripple requirement of K_{ripple} , and modify $K_{0\text{min}}$ and $K_{0\text{max}}$ based upon the principle of bisection method. The iteration is stopped when $K_{\text{ripple}0}$ is close to K_{ripple} within a pre-set tolerance. Here, the tolerance $|K_{\text{ripple}0} - K_{\text{ripple}}| \leq 10^{-6}$ is used. Then the final K_0 is found and hence C_{eq} is obtained by $K_0 \cdot P_{\text{nom}}/[(1+k_{\text{red}}) \cdot \omega_o \cdot V_{\text{dc}}^2]$.

Therefore, the stored energy of all HB-SM capacitors, EoP_{HBmain} , can be calculated by

$$EoP_{\text{HBmain}} = \frac{6N_h \cdot C_{\text{hb}} \cdot (V_{\text{dc}}/N_h)^2 / 2}{P_{\text{nom}}} \times 10^3 = \frac{3C_{\text{eq}} V_{\text{dc}}^2}{P_{\text{nom}}} \times 10^3 \geq \frac{3K_0}{\omega_o} \times 10^3 \text{ [kJ/MVA]} \quad (4.52)$$

In practice, the SM capacitance is selected under nominal operating conditions (i.e., $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$) and without considering redundant SMs (i.e., $k_{\text{red}} = 0$). After the SM capacitance is selected based upon the nominal conditions without redundancy, $k_{\text{red}} \cdot N_h$ SMs are used as redundancy. Considering $k_{\text{flt}} \cdot N_h$ SMs bypassed due to SM faults, the actual 2nd harmonic current in (4.50) should be calculated with the equivalent redundancy ratio of $(k_{\text{red}} - k_{\text{flt}})$. Then the critical angles $\theta_{\text{up}1}$ and $\theta_{\text{up}2}$ can be found by solving $i_{\text{up}}(t) = 0$, and the actual SM capacitor voltage ripple is shown as follows:

$$K_{\text{ripple-SMflt}} = \frac{1}{(1 + k_{\text{red}} - k_{\text{SMflt}}) C_{\text{eq}} V_{\text{dc}}} \cdot \left| q_{\text{up}}(\theta_{\text{up}2}/\omega_o) - q_{\text{up}}(\theta_{\text{up}1}/\omega_o) \right| \quad (4.53)$$

4.3.1.3 Impact of m_{rated} , SCR, X_{TR}/S_{TR} and X_{Larm} on the SM capacitor size

As seen from the analysis in Section 4.3.1.1, EoP_{HBmain} is independent of P_{nom} , V_{dc} , and k_{red} . However, due to the absence of CCSC strategy, the existing 2nd harmonic in the arm current increases the complexity of the calculation of EoP_{HBmain} . There is no explicit relationship between EoP_{HBmain} and P_{nom} , V_{dc} , and k_{red} . Therefore, for capacitor sizing without CCSC, the value K_0 is evaluated with different P_{nom} , V_{dc} , and k_{red} while using fixed m_{rated} , SCR, X_{TR}/S_{TR} , and X_{Larm} , which is equivalent to evaluating the relationship between EoP_{HBmain} ($= 3K_0/\omega_b$) and P_{nom} , V_{dc} , and k_{red} .

With $f_o = 60$ Hz, $k_{red} = 0$, $m_{rated} = 0.95$, SCR = $3\angle 80^\circ$, $X_{TR}/S_{TR} = 0.1$ pu, $X_{Larm} = 0.15$ pu, and $K_{ripple} = 0.1$ pu, Fig. 4.14 (a) shows the variable K_0 used in the capacitor sizing without CCSC with respect to different P_{nom} and V_{dc} . As seen, K_0 is largely independent of P_{nom} and V_{dc} , and so is EoP_{HBmain} . Therefore, it is reasonable to use one set of P_{nom} and V_{dc} values to evaluate the relationship between K_0 and k_{red} , which is shown in Fig. 4.14 (b). It is observed that K_0 is also independent of k_{red} . To conclude, with or without CCSC and with or without 3rd harmonic injection, the energy densities are all essentially independent of P_{nom} , V_{dc} , and k_{red} .

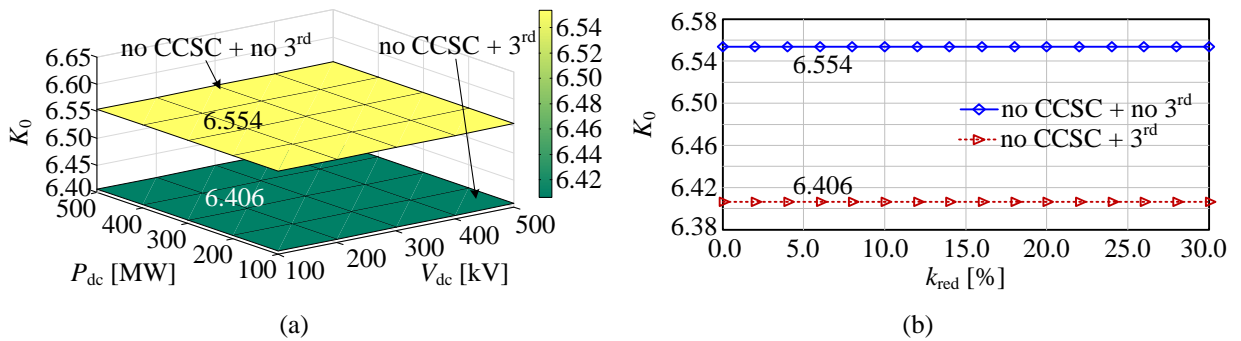


Fig. 4.14: Variable K_0 used in capacitor sizing without CCSC for $f_o = 60$ Hz, $m_{rated} = 0.95$, SCR = $3\angle 80^\circ$, $X_{TR}/S_{TR} = 0.1$ pu, $X_{Larm} = 0.15$ pu, and $K_{ripple} = 0.1$ pu

(a) with respect to P_{nom} and V_{dc} under $k_{red} = 0$; (b) with respect to k_{red} under $P_{nom} = 500$ MW and $V_{dc} = 500$ kV.

Under the ripple requirement of $K_{ripple} = 0.1$ pu and PV control with $P_{ref} = 1.0$ and $V_{acref} = 1.0$ pu, EoP_{HBmain} for the operation with or without CCSC and with or without 3rd harmonic injection

is shown in Fig. 4.15 with respect to m_{rated} , $X_{\text{TR}}/S_{\text{TR}}$, X_{Larm} , and SCR, respectively. As seen from Fig. 4.15 (a), EoP_{HBmain} increases as the rated modulation index decreases, with or without CCSC and with or without 3rd harmonic injection. Fig. 4.15 (b) shows that with $X_{\text{TR}}/S_{\text{TR}}$ varying within [0.05, 0.20] pu, EoP_{HBmain} has negligible change for the considered four control methods. As seen from Fig. 4.15 (c), with X_{Larm} varying within [0.1, 0.25] pu, EoP_{HBmain} for the operation with CCSC has negligible change, whereas EoP_{HBmain} for the operation without CCSC reduces as X_{Larm} increases. This is because the 2nd harmonic of the arm current is reduced as X_{Larm} increases (see (4.50)), resulting in smaller capacitor voltage ripple.

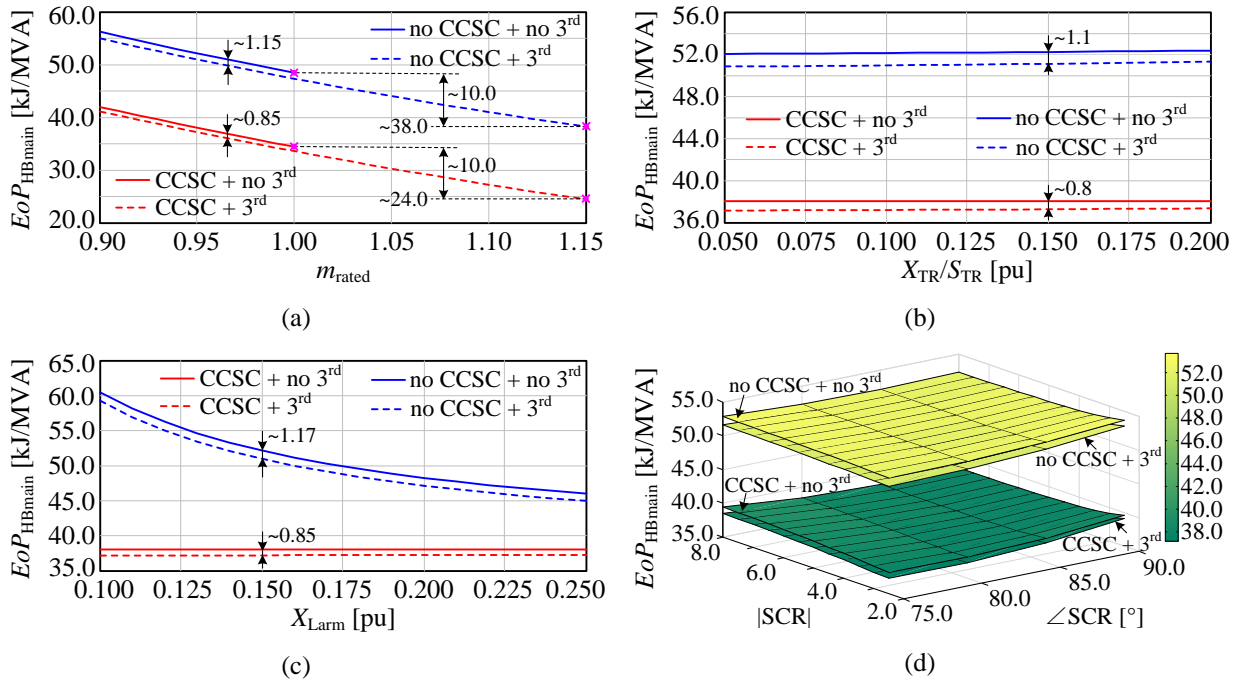


Fig. 4.15: Stored energy of all HB-SM capacitors per power rating unit (EoP_{HBmain}) with respect to m_{rated} , $X_{\text{TR}}/S_{\text{TR}}$, X_{Larm} and SCR under $K_{\text{ripple}} = 0.1$ pu and $k_{\text{red}} = 0$

- (a) EoP_{HBmain} with respect to m_{rated} under $f_o = 60$ Hz, $X_{\text{TR}}/S_{\text{TR}} = 0.1$ pu, $X_{\text{Larm}} = 0.15$ pu, and $\text{SCR} = 3\angle 80^\circ$;
- (b) EoP_{HBmain} with respect to $X_{\text{TR}}/S_{\text{TR}}$ under $f_o = 60$ Hz, $m_{\text{rated}} = 0.95$ pu, $X_{\text{Larm}} = 0.15$ pu, and $\text{SCR} = 3\angle 80^\circ$;
- (c) EoP_{HBmain} with respect to X_{Larm} under $f_o = 60$ Hz, $m_{\text{rated}} = 0.95$ pu, $X_{\text{TR}}/S_{\text{TR}} = 0.1$ pu, and $\text{SCR} = 3\angle 80^\circ$;
- (d) EoP_{HBmain} with respect to SCR under $f_o = 60$ Hz, $m_{\text{rated}} = 0.95$ pu, $X_{\text{TR}}/S_{\text{TR}} = 0.1$ pu, and $X_{\text{Larm}} = 0.15$ pu.

In Fig. 4.15 (d), with the magnitude of SCR varying within [2.0, 8.0] and its angle varying within [75°, 90°], EoP_{HBmain} is seen to have negligible change for the considered four control

methods. It is also observed from Fig. 4.15 (a)-(d) that under the same system parameters and operating point, the operation with 3rd harmonic injection requires slightly lower EoP_{HBmain} (~1.0 kJ/MVA smaller) compared with that without 3rd harmonic injection, whereas EoP_{HBmain} for the operation without CCSC is much higher than that with CCSC. Taking $m_{rated} = 0.95$ as an example in Fig. 4.15 (a), $EoP_{HBmain} \approx 37.0$ kJ/MVA with CCSC and $EoP_{HBmain} \approx 52.0$ kJ/MVA without CCSC, resulting in $(52.0 - 37.0)/37.0 \approx 40.5\%$ higher EoP_{HBmain} for operation without CCSC.

The influence of system parameters on the stored energy of all HB-SM capacitors per power rating unit in the main power stage (EoP_{HBmain}) is summarized in Table 4.5. For the operation with or without CCSC and with or without the 3rd harmonic injection, EoP_{HBmain} is independent of system's power rating and dc-link voltage; X_{TR}/S_{TR} and SCR have slight influence on EoP_{HBmain} ; and EoP_{HBmain} is increased with the rated modulation index, system fundamental frequency, and K_{ripple} decreasing. The arm inductance has slight influence on EoP_{HBmain} under the operation with CCSC, whereas EoP_{HBmain} increases as the arm inductance decreases under the operation without CCSC. Therefore, two cases of m_{rated} and X_{Larm} values are analyzed to obtain the general range of EoP_{HBmain} with respect to K_{ripple} . With $f_o = 60$ Hz, $X_{TR}/S_{TR} = 0.1$ pu, $k_{red} = 0$, and $SCR = 3 \angle 80^\circ$, the relationship between EoP_{HBmain} with respect to K_{ripple} is displayed in Fig. 4.16 under two cases of m_{rated} and X_{Larm} values (case 1: $m_{rated} = 1.0$ and $X_{Larm} = 0.2$ pu, and case 2: $m_{rated} = 0.9$ and $X_{Larm} = 0.1$ pu). It is seen that EoP_{HBmain} is increased with the required ripple value decreasing. As seen from Fig. 4.16 (b), EoP_{HBmain} for the operation with CCSC is inversely proportional to K_{ripple} since $EoP_{HBmain} \cdot K_{ripple}$ is approximately constant. However, EoP_{HBmain} is not inversely proportional to K_{ripple} for the operation without CCSC. As seen from Fig. 4.16 (a), with the ripple requirement of $K_{ripple} = 0.1$ pu, EoP_{HBmain} is in the range of [33.0 kJ/MVA, 41.0 kJ/MVA] under the operation with CCSC and [44.0 kJ/MVA, 65.0 kJ/MVA] under the operation without CCSC. Therefore, the

operation with CCSC is preferred to reduce the system's footprint by allowing usage of smaller capacitors.

Table 4.5: Influence of system parameters on EoP_{HBmain} for the HB-SM capacitor sizing in the main power stage

Operation mode	P_{dc}	V_{dc}	m_{rated}	X_{Larm}	X_{TR}/S_{TR}	SCR	$f_o (\omega_b)$	K_{ripple}	EoP_{HBmain}
CCSC and 3 rd or not	No	No	↓	Slight	Slight	Slight	↓	↓	↑
No CCSC and 3 rd or not	No	No	↓	↓	Slight	Slight	↓	↓	↑

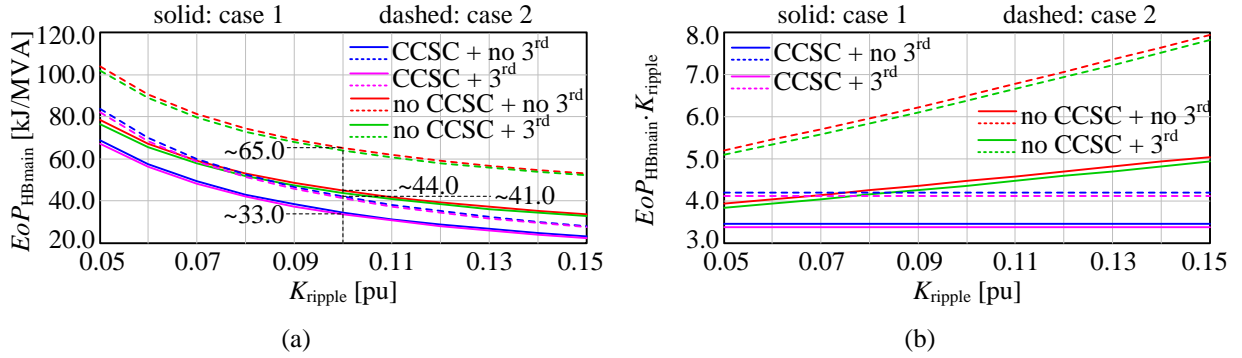


Fig. 4.16: Stored energy of all HB-SM capacitors (EoP_{HBmain}) with respect to K_{ripple} under $f_o = 60$ Hz, $X_{TR}/S_{TR} = 0.1$ pu, $k_{red} = 0$, and $SCR = 3\angle 80^\circ$ and two cases of m_{rated} and X_{Larm} (case 1: $m_{rated} = 1.0$ and $X_{Larm} = 0.2$ pu, case 2: $m_{rated} = 0.9$ and $X_{Larm} = 0.1$ pu)

(a) EoP_{HBmain} with respect to K_{ripple} ; (b) $EoP_{HBmain} \cdot K_{ripple}$ with respect to K_{ripple} .

With system specifications of $f_o = 60$ Hz, $m_{rated} = 0.95$, $k_{red} = 0$, $X_{TR}/S_{TR} = 0.1$ pu, $X_{Larm} = 0.15$ pu, and $SCR = 3\angle 80^\circ$ and a ripple requirement of $K_{ripple} = 0.1$ pu, EoP_{HBmain} is calculated as 38.0 kJ/MVA (with CCSC) and 52.0 kJ/MVA (without CCSC) for operation without 3rd harmonic injection under $P_{ref} = 1.0$ and $V_{acref} = 1.0$ pu. The SM capacitor ripple is evaluated under different redundancies and SM fault ratios as shown in Fig. 4.17. As seen from Fig. 4.17 (a), with increased redundancy, EoP_{HBmain} increases, and the SM capacitor voltage ripple without CCSC reduces more than that with CCSC. However, the operation with CCSC is still preferred, since EoP_{HBmain} calculated under nominal conditions is much smaller than that without CCSC. Considering SM faults in the operation, the actual capacitor voltage ripple is increased but less than the nominal ripple requirement as seen from Fig. 4.17 (b).

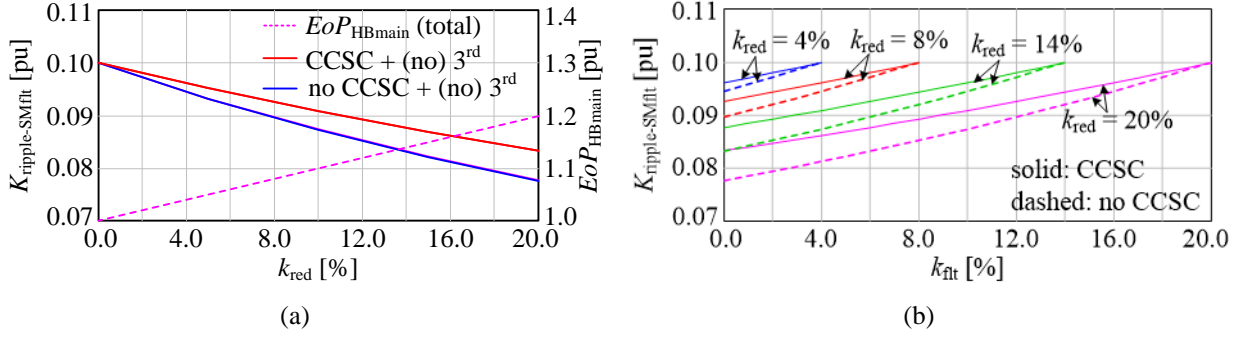


Fig. 4.17: Evaluation of capacitor voltage ripple under different redundancies and SM fault ratios

(a) with respect to k_{red} ; (b) with respect to k_{fit} under different k_{red} .

4.3.2 Capacitance design of the main power stage in mixed-SM HC-MMC

The mixed-SM HC-MMC has two SM types (HB and FB SMs) in its main power stage. FB SMs can output not only the same voltage levels as HB SMs but also negative voltage levels. When $m_{\text{up}}(t) > 0$ over the entire fundamental period, i.e., the operating modulation index is less than 1.0 (or 1.15 with 3rd harmonic injection), all HB and FB SMs only output zero and positive voltage levels. As such, the mixed-SM HC-MMC can be regarded as the original HC-MMC with the redundancy ratio of $(k_{\text{red}} + k_{\text{fm}})$, where $k_{\text{fm}} = N_{\text{fm}}/N_{\text{h}}$, and the SM capacitance selection is the same as that for the original HC-MMC shown in Section 4.3.1. Therefore, the ripple waveform of each SM capacitor in the main power stage of mixed-SM HC-MMC can be obtained by replacing k_{red} with $(k_{\text{red}} + k_{\text{fm}})$ in (4.39), and expressed as follows:

$$\begin{aligned}
 (1 + k_{\text{red}} + k_{\text{fm}}) N_{\text{h}} C_{\text{sm}} \Delta v_{\text{csmUp}}(t) &= \int m_{\text{up}}(t) \cdot N_{\text{h}} \cdot i_{\text{up}}(t) dt \\
 \Rightarrow \Delta v_{\text{csmUp}}(t) &= \frac{1}{(1 + k_{\text{red}} + k_{\text{fm}}) C_{\text{sm}}} \cdot \int m_{\text{up}}(t) \cdot i_{\text{up}}(t) dt
 \end{aligned} \tag{4.54}$$

where $C_{\text{hb}} = C_{\text{fm}} = C_{\text{sm}}$. As seen from the SM capacitance selection of the original HC-MMC in Section 4.3.1, the stored energy of all SM capacitors in the main power stage is independent of k_{red} , i.e., $(k_{\text{red}} + k_{\text{fm}})$ in the mixed-SM HC-MMC. In other words, if the upper-arm modulation waveform is above zero over the entire fundamental period, the stored energy of all SM capacitors (including

both HB and FB SMs) in the main power stage of the mixed-SM HC-MMC is independent of the number of additional FB SMs per arm.

However, in the region that $m_{up}(t) < 0$, only FB SMs are required to be inserted, resulting in different capacitor voltage ripple waveforms for HB and FB SMs in the main power stage. Table 4.6 shows the contents organization of the SM capacitance selection of main power stage in the mixed-SM HC-MMC under different control conditions. For the cases when $m_{up}(t)$ has a negative zone during the fundamental period, the SM capacitance selection for the main power stage of the mixed-SM HC-MMC with CCSC and no 3rd harmonic injection is firstly investigated in Section 4.3.2.1; then the other control modes of operations without CCSC and with or without 3rd harmonic injection are discussed in Section 4.3.2.2.

Table 4.6: Contents organization of the SM capacitance selection of main power stage in mixed-SM HC-MMC

CCSC	3 rd harmonic injection	Condition		Contents organization
Yes/No	No	$m \leq 1.0$	$m_{up}(t)$ is positive over the whole fundamental period	section 4.3.1 (use $k_{red} + k_{fm}$ as redundancy and $C_{hb} = C_{fm}$)
Yes/No	Yes	$m \leq 1.15$		
Yes	No	$m > 1.0$	$m_{up}(t)$ has negative zone over the fundamental period	see Section 4.3.2.1
No	No	$m > 1.0$		See Section 4.3.2.2
No	Yes	$m > 1.15$		

4.3.2.1 Capacitor sizing with CCSC and without 3rd harmonic injection

In order to clearly show the SM capacitance design concept for the mixed-SM HC-MMC, the operation with CCSC and without 3rd harmonic injection is analyzed next due to its simplicity of the upper-arm current and modulation waveforms. To make use of the extended linear modulation range, the turns ratio of the transformer is increased to $(1+2k_{fm}) \cdot n_{tr0}$, where n_{tr0} is the turns ratio of the transformer used for the HC-MMC with $k_{fm} = 0$. Under this circumstance, the range of the modulation waveform partially exceeds ± 1.0 , and the upper-arm modulation waveform will not always be positive over the entire fundamental period. Denote the required numbers of inserted

HB and FB SMs as $k_{\text{HBin}}(t) \cdot N_h$ and $k_{\text{FBin}}(t) \cdot N_h$, respectively, where $k_{\text{HBin}}(t) + k_{\text{FBin}}(t) = m_{\text{up}}(t)$, and the detailed algorithm to determine $k_{\text{HBin}}(t)$ and $k_{\text{FBin}}(t)$ can be found in Section A.2. Therefore, the HB- and FB-SM capacitor voltage ripple are derived as follows:

$$\begin{aligned} (1+k_{\text{red}})N_h C_{\text{hb}} \Delta v_{\text{chbUp}}(t) &= \int k_{\text{HBin}}(t) N_h \cdot i_{\text{up}}(t) dt \\ \Rightarrow \Delta v_{\text{chbUp}}(t) &= \frac{1}{(1+k_{\text{red}})C_{\text{hb}}} \cdot \int k_{\text{HBin}}(t) \cdot i_{\text{up}}(t) dt \end{aligned} \quad (4.55)$$

$$\begin{aligned} k_{\text{fm}}N_h C_{\text{fm}} \Delta v_{\text{cfmUp}}(t) &= \int k_{\text{FBin}}(t) N_h \cdot i_{\text{up}}(t) dt \\ \Rightarrow \Delta v_{\text{cfmUp}}(t) &= \frac{1}{k_{\text{fm}}C_{\text{fm}}} \cdot \int k_{\text{FBin}}(t) \cdot i_{\text{up}}(t) dt \end{aligned} \quad (4.56)$$

The overall SM capacitor voltage ripple waveform is calculated as follows:

$$\begin{aligned} \Delta v_{\text{csmUp-avg}}(t) &= \frac{(1+k_{\text{red}})\Delta v_{\text{chb}}(t) + k_{\text{fm}}\Delta v_{\text{cfm}}(t)}{1+k_{\text{red}}+k_{\text{fm}}} \\ &= \frac{1}{1+k_{\text{red}}+k_{\text{fm}}} \cdot \left(\frac{1}{C_{\text{hb}}} \int k_{\text{HBin}}(t) \cdot i_{\text{up}}(t) dt + \frac{1}{C_{\text{fm}}} \int k_{\text{FBin}}(t) \cdot i_{\text{up}}(t) dt \right) \end{aligned} \quad (4.57)$$

If $C_{\text{hb}} = C_{\text{fm}} = C_{\text{sm}}$, the overall average capacitor voltage can be simplified as follows:

$$\Delta v_{\text{csmUp-avg}}(t) = \frac{\int (k_{\text{HBin}}(t) + k_{\text{FBin}}(t)) i_{\text{up}}(t) dt}{(1+k_{\text{red}}+k_{\text{fm}})C_{\text{sm}}} = \frac{1}{(1+k_{\text{red}}+k_{\text{fm}})C_{\text{sm}}} \cdot \int m_{\text{up}}(t) i_{\text{up}}(t) dt \quad (4.58)$$

It is seen that the overall SM capacitor voltage ripple waveform is the same as that derived using the concept that the total charges are evenly distributed among all SMs in one arm (this is similar to the derivation for the original HC-MMC). If $C_{\text{hb}} \neq C_{\text{fm}}$, the overall SM capacitor voltage ripple is close to that shown in (4.58) with $C_{\text{sm}} \approx C_{\text{hb}}$, because the number of HB SMs is generally much larger than that of FB SMs in the main power stage. Therefore, the overall SM capacitor voltage ripple is primarily determined by the voltage ripple across the HB-SM capacitors.

Fig. 4.18 shows typical waveforms for the mixed-SM HC-MMC operating with a modulation index larger than 1.0, with CCSC and without the 3rd harmonic injection. In Zone 1, i.e., when $i_{up}(t) < 0$ and $m_{up}(t) > 0$, both HB and FB SMs in the main power stage have chances to be discharged, whereas in Zone 2, i.e., when $m_{up}(t) < 0$ and $i_{up}(t) > 0$, only FB SMs in the main power stage have chances to be discharged. Therefore, the overall SM capacitor voltage ripple is determined by the charge (Q_{iup0}) in Zone 1, and the actual FB-SM capacitor voltage ripple is determined by the charge (Q_{mup0}) in Zone 2.

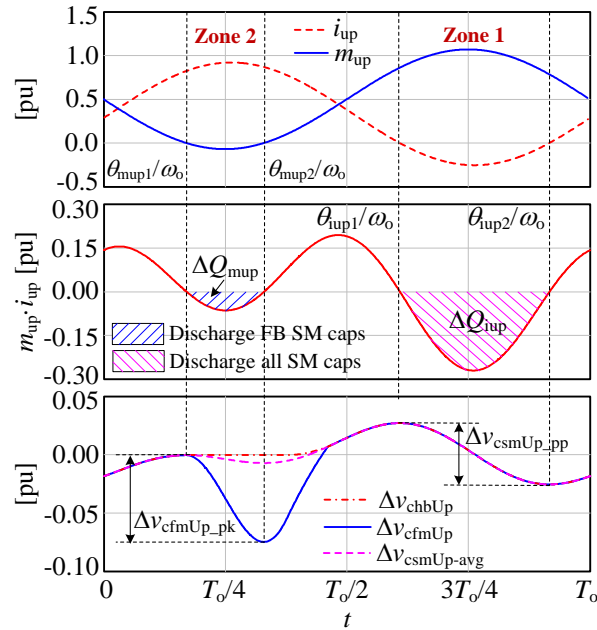


Fig. 4.18: Upper-arm modulation wave, current, and SM capacitor voltage ripple waveforms in mixed-SM HC-MMC with CCSC and without 3rd harmonic injection

If the influence of the small number of FB SMs with relatively large capacitor voltage ripple is not a concern, the SM capacitance selection can be based upon the overall average SM capacitor voltage ripple with $C_{hb} = C_{fm}$, and only the calculation in subsection (i) shown below is required to find the proper SM capacitance. If both the HB- and FB-SM capacitor voltage ripple values are considered to meet the ripple requirement, the SM capacitances for HB and FB SMs must be selected separately, and both calculations in subsection (i) and (ii) shown below are required.

(i) Calculation of the overall SM capacitor voltage ripple in Zone 1

Let $i_{up}(t) = 0$, and the critical angles θ_{up1} and θ_{up2} that divide the charging and discharging intervals are the same as those for the original HC-MMC as shown in (4.41). Considering the same SM capacitance for both HB and FB SMs in the main power stage (i.e., $C_{fm} = C_{hb} = C_{sm}$), the capacitor voltage ripple value within $[\theta_{up1}, \theta_{up2}]$ is obtained by calculating the charge value ΔQ_{iup} shown in Fig. 4.18, and expressed as follows:

$$\begin{aligned}\Delta v_{csmUp_pp} &= \frac{1}{(1+k_{red}+k_{fm})N_h C_{sm}} \cdot \left| \int_{\theta_{up1}/\omega_o}^{\theta_{up2}/\omega_o} N_h m_{up}(t) i_{up}(t) dt \right| \\ &= \frac{\Delta Q_{iup}}{(1+k_{red}+k_{fm})C_{sm}} = \frac{I_{dc}}{(1+k_{red}+k_{fm})\omega_o C_{sm}} \Delta Q_{iup0}\end{aligned}\quad (4.59)$$

where ΔQ_{iup0} is the same as that shown in (4.44) with $k_{3rd} = 0$, and it is expressed as follows:

$$\Delta Q_{iup0} = \left| \left(\frac{m \cos(\varphi)}{3} - \frac{2}{3m \cos(\varphi)} \right) \cos(\theta_0) - \frac{1}{6} \sin(2\theta_0) \right| \quad (4.60)$$

If the maximum allowed capacitor voltage ripple in each SM capacitor is $K_{ripple} \cdot (V_{dc}/N_h)$, the minimum SM capacitance of either HB or FB SMs can be obtained using $\Delta v_{csmUp_pp} \leq K_{ripple} \cdot V_{dc}/N_h$:

$$C_{eq1} = \frac{C_{sm}}{N_h} \geq \frac{I_{dc}}{(1+k_{red}+k_{fm})\omega_o K_{ripple} V_{dc}} \Delta Q_{iup0} \quad (4.61)$$

The above expression is similar to that shown in (4.45), however, the equivalent redundancy ratio is $(k_{red} + k_{fm})$ in the mixed-SM HC-MMC. Note that if equal SM capacitances for HB and FB SMs are preferred and the overall average SM capacitor voltage ripple value is the main concern, the following calculation for FB-SM capacitor voltage ripple is not required.

(ii) Calculation of the FB-SM capacitor voltage ripple in Zone 2

Let $m_{\text{up}}(t) = 0$, and the critical angles θ_{mup1} and θ_{mup2} that divide the charging and discharging intervals are calculated as follows:

$$\theta_{\text{mup1}} = \alpha_0 = \sin^{-1}(1/m), \quad \theta_{\text{mup2}} = \pi - \alpha_0 \quad (4.62)$$

Then the charge value ΔQ_{mup} shown in Fig. 4.18 within $[\theta_{\text{mup1}}, \theta_{\text{mup2}}]$ is calculated as follows:

$$\Delta Q_{\text{mup}} = \left| \int_{\theta_{\text{mup1}}/\omega_o}^{\theta_{\text{mup2}}/\omega_o} m_{\text{up}}(t) i_{\text{up}}(t) dt \right| = \frac{I_{\text{dc}}}{\omega_o} \Delta Q_{\text{mup0}} \quad (4.63)$$

where

$$\Delta Q_{\text{mup0}} = \left| \left(\frac{m}{3} - \frac{2}{3m} \right) \cos(\alpha_0) + \frac{1}{6} \sin(2\alpha_0) \right| \quad (4.64)$$

Within $[\theta_{\text{mup1}}, \theta_{\text{mup2}}]$, $m_{\text{up}}(t) < 0$ and only FB SMs are inserted to provide negative voltage levels.

With the sorting and balancing control, the charge is evenly distributed among N_{fm} FB SMs within the interval $[\theta_{\text{mup1}}, \theta_{\text{mup2}}]$. Therefore,

$$\begin{aligned} N_{\text{fm}} C_{\text{fm}} \Delta v_{\text{cfmUp_pk}} &= k_{\text{fm}} N_{\text{h}} C_{\text{fm}} \Delta v_{\text{cfmUp_pk}} = \left| \int_{\theta_{\text{mup1}}/\omega_o}^{\theta_{\text{mup2}}/\omega_o} N_{\text{h}} m_{\text{up}}(t) i_{\text{up}}(t) dt \right| = N_{\text{h}} \Delta Q_{\text{mup}} \\ \Rightarrow \Delta v_{\text{cfmUp_pk}} &= \frac{\Delta Q_{\text{mup}}}{k_{\text{fm}} C_{\text{fm}}} = \frac{I_{\text{dc}}}{k_{\text{fm}} \omega_o C_{\text{fm}}} \Delta Q_{\text{mup0}} \end{aligned} \quad (4.65)$$

In order to have $\Delta v_{\text{cfmUp_pk}} \leq (K_{\text{ripple}}/2) \cdot (V_{\text{dc}}/N_{\text{h}})$, the minimum FB-SM capacitance must satisfy:

$$C_{\text{eq2}} = \frac{C_{\text{fm}}}{N_{\text{h}}} \geq \frac{2I_{\text{dc}} \Delta Q_{\text{mup0}}}{k_{\text{fm}} \omega_o K_{\text{ripple}} V_{\text{dc}}} \quad (4.66)$$

Therefore, to satisfy the ripple requirement for FB-SM capacitor voltage in both zones, the FB-SM capacitance is selected to be the larger value between C_{eq1} and C_{eq2} . According to the expressions in (4.61) and (4.66), it holds that if

$$C_{eq1} \geq C_{eq2} \quad \Rightarrow \quad \frac{\Delta Q_{iup0}}{\Delta Q_{mup0}} \geq \frac{1+k_{red}+k_{fm}}{2k_{fm}} \quad (4.67)$$

Overall, the SM capacitance selections for HB and FB SMs in the main power stage of mixed-SM HC-MMC are $C_{hb} = N_h \cdot C_{eq1}$ and $C_{fm} = N_h \cdot \max(C_{eq1}, C_{eq2})$, respectively. Such capacitance selection satisfies $C_{fm} \geq C_{hb}$, and the overall SM capacitor voltage ripple shown in (4.57) is still within the ripple requirement.

According to $I_{dc} = P_{ref} \cdot P_{nom} / V_{dc}$ (see (4.2)), the stored energy of all HB-SM capacitors (including redundancy) in the main power stage of a three-phase mixed-SM HC-MMC per power rating unit, EoP_{HBmain} , is calculated as follows:

$$\begin{aligned} EoP_{HBmain} &= \frac{6(1+k_{red})N_h \cdot C_{hb} \cdot (V_{dc}/N_h)^2 / 2}{P_{nom}} \times 10^3 \\ &= \frac{3(1+k_{red})C_{eq1}V_{dc}^2}{P_{nom}} \times 10^3 \geq \frac{3P_{ref}\Delta Q_{iup0}(1+k_{red})}{\omega_o K_{ripple}(1+k_{red}+k_{fm})} \times 10^3 \text{ [kJ/MVA]} \end{aligned} \quad (4.68)$$

If $C_{eq1} \geq C_{eq2}$, then $C_{fm} = N_h \cdot C_{eq1}$ and the stored energy of all FB-SM capacitors in the main power stage of a three-phase mixed-SM HC-MMC per power rating unit, EoP_{FBmain} , is calculated as follows:

$$\begin{aligned} EoP_{FBmain} &= \frac{6k_{fm}N_h \cdot C_{fm} \cdot (V_{dc}/N_h)^2 / 2}{P_{nom}} \times 10^3 = \frac{k_{fm}}{1+k_{red}} EoP_{HBmain} \\ \Rightarrow EoP_{main} &= EoP_{HBmain} + EoP_{FBmain} \geq \frac{3P_{ref}\Delta Q_{iup0}}{\omega_o K_{ripple}} \times 10^3 \text{ [kJ/MVA]} \end{aligned} \quad (4.69)$$

If $C_{eq1} < C_{eq2}$, then $C_{fm} = N_h \cdot C_{eq2}$ and the stored energy of all FB-SM capacitors in the main power stage of a three-phase mixed-SM HC-MMC per power rating unit, EoP_{FBmain} , is calculated as follows:

$$\begin{aligned}
 EoP_{FBmain} &= \frac{6k_{fm}N_h \cdot C_{fm} \cdot (V_{dc}/N_h)^2/2}{P_{nom}} \times 10^3 \geq \frac{6P_{ref}\Delta Q_{mup0}}{\omega_o K_{ripple}} \times 10^3 \text{ [kJ/MVA]} \\
 \Rightarrow EoP_{main} &= EoP_{HBmain} + EoP_{FBmain} \\
 &\geq \frac{3P_{ref}}{\omega_o K_{ripple}} \left(\frac{1+k_{red}}{1+k_{red}+k_{fm}} \Delta Q_{iup0} + 2\Delta Q_{mup0} \right) \times 10^3 \text{ [kJ/MVA]}
 \end{aligned} \tag{4.70}$$

4.3.2.2 Capacitor sizing without CCSC and with or without 3rd harmonic injection

Since the number of FB SMs per arm is generally much smaller than that of HB SMs, the overall average SM capacitor voltage ripple of the main power stage can be approximately determined by HB SMs as shown in (4.58), which is similar to the expression used to analyze the 2nd harmonic current shown in (4.16). Therefore, for the operation of mixed-SM HC-MMC without CCSC, the magnitude and phase angle of 2nd harmonic current are approximately the same as those derived for the original HC-MMC, which are shown in (4.27) and (4.28). However, the operation of the mixed-SM HC-MMC without CCSC makes the current expression complicated due to the existence of 2nd harmonic component, and similar operation with 3rd harmonic injection makes the upper-arm modulation waveform complicated. This leads to difficulties in finding the critical angles of θ_{up1} and θ_{up2} that make $i_{up}(\theta_{upj}/\omega_o) = 0$, and θ_{mup1} and θ_{mup2} that make $m_{up}(\theta_{mupj}/\omega_o) = 0$, where $j = 1$ and 2 . As such, a computer-aided method is recommended to calculate the proper SM capacitance used in the main power stage of the mixed-SM HC-MMC. This method directly calculates the capacitor voltage ripple value by finding the maximum and minimum values of the ripple waveforms, as shown in Section A.2 in Appendix A.

4.3.2.3 Discussions on HB- and FB-SM capacitor size in the main power stage

Based upon both the HB- and FB-SM capacitor-voltage ripple within the ripple requirement, parametric study of the stored energy of HB- and FB-SM capacitors per power rating unit in the main power stage of the mixed-SM HC-MMC is conducted in this subsection.

Compared with the original HC-MMC, the mixed-SM HC-MMC is able to extend the linear modulation range to $(1+2k_{fm})$. With the same system parameters (i.e., dc-link voltage and ac network) as in the original HC-MMC, the transformer's turns ratio must be changed to make use of the extended linear range in the mixed-SM HC-MMC. However, applications may arise wherein the transformer is already designed for the original HC-MMC and it is impractical to change its turns ratio. The added FB SMs are only used to promptly decay the dc-fault current flow through converter's arms. Therefore, two cases for the mixed-SM HC-MMC after adding FB SMs in the main power stage are discussed below.

Case 1: Transformer's turns ratio kept unchanged from that in the original HC-MMC

All the system parameters are kept the same as those for the mixed-SM HC-MMC with $k_{fm} = 0$, i.e., the original HC-MMC. Under this circumstance, the operating points are unchanged even after adding extra FB SMs in the main power stage. Therefore, the mixed-SM HC-MMC can be regarded as the original HC-MMC with FB SMs as redundant SMs. As discussed in Section 4.3.1.3, the stored energy of all SM capacitors in the main power stage is independent of SM redundancy for the original HC-MMC. In brief, the total stored energy of both HB and FB SMs in the main power stage of the mixed-SM HC-MMC will be the same as that of the original HC-MMC, and the actual SM capacitance has such relationship as $C_{sm_mix} = C_{sm_orig}/(1+k_{fm})$, where C_{sm_mix} and C_{sm_orig} are the capacitances per SM in the main power stages of both the mixed-SM and original HC-MMCs, respectively.

Case 2: Transformer's turns ratio proportionally changed for the mixed-SM HC-MMC

To proportionally make use of the linear modulation range after adding FB SMs in the main power stage, the transformer's turns ratio (seen from the converter side to system-side) is increased to $(1+2k_{\text{fm}}) \cdot n_{\text{tr}0}$, where $n_{\text{tr}0}$ is the turns ratio for the original HC-MMC, i.e., mixed-SM HC-MMC with $k_{\text{fm}} = 0$. Denote the rated modulation index and per-unit arm inductance as $m_{\text{rated}0}$ and $X_{\text{Larm}0}$ for the original HC-MMC. Therefore, for the mixed-SM HC-MMC with $k_{\text{fm}} \cdot N_{\text{h}}$ FB SMs per arm, the actual rated modulation index is equal to $m_{\text{rated}} = (1+2k_{\text{fm}}) \cdot m_{\text{rated}0}$, and the per-unit arm inductance is modified to $X_{\text{Larm}} = X_{\text{Larm}0} / (1+2k_{\text{fm}})^2$ to keep the arm inductance value unchanged.

With the system specifications of $f_o = 60$ Hz, $m_{\text{rated}0} = \{0.9, 0.95, 1.0\}$, $X_{\text{Larm}0} = 0.15$ pu, $X_{\text{TR}}/S_{\text{TR}} = 0.1$ pu, $\text{SCR} = 3.0 \angle 80^\circ$, $k_{\text{red}} = 0$ and the ripple requirement of $K_{\text{ripple}} = 0.1$ pu, Fig. 4.19 shows the stored energy of all HB- and FB-SM capacitors in the main power stage per power rating unit (EoP_{HBmain} and EoP_{FBmain}), the relationship between the HB- and FB-SM capacitance in the main power stage, and the operating modulation index and phase current magnitude in the mixed-SM HC-MMC operating with CCSC and no 3rd harmonic injection. As seen from Fig. 4.19 (a), EoP_{HBmain} is decreased with k_{fm} increasing, since the converter current is reduced (see Fig. 4.19 (d)). As discussed in Section 4.3.2.1, when the operating modulation index is larger than 1.0, $m_{\text{up}}(t)$ has a negative zone in which only FB SMs are inserted to charge or discharge. This may require FB SMs to use larger capacitance to obtain a ripple within the requirement. As seen from Fig. 4.19 (a) and (c), EoP_{FBmain} is increased largely when $C_{\text{fm}}/C_{\text{hb}} > 1.0$, as the corresponding modulation index is higher than 1.0 (see Fig. 4.19 (d)). As seen from Fig. 4.19 (b), EoP_{main} firstly decreases and then increases with k_{fm} increasing, and EoP_{main} at $k_{\text{fm}} = 0$ is the value for the original HC-MMC. Therefore, EoP_{main} of the mixed-SM HC-MMC can be smaller than that of the original HC-MMC with proper selection of k_{fm} . With $m_{\text{rated}0} = \{0.9, 0.95, 1.0\}$, the optimal EoP_{main} for the

mixed-SM HC-MMC is reached when k_{fm} is selected approximately as {12%, 9%, 6%}, respectively. All the above three cases of m_{rated0} and optimal k_{fm} result in approximately $m_{rated} = (1+2k_{fm}) \cdot m_{rated0} \approx 1.12$, and the optimal EoP_{main} is approximately in the range of [30.0 kJ/MVA, 32.0 kJ/MVA]. Compared with EoP_{main} required for the original HC-MMC, the optimal EoP_{main} for the mixed-SM HC-MMC is reduced by 7.0%~28.0%.

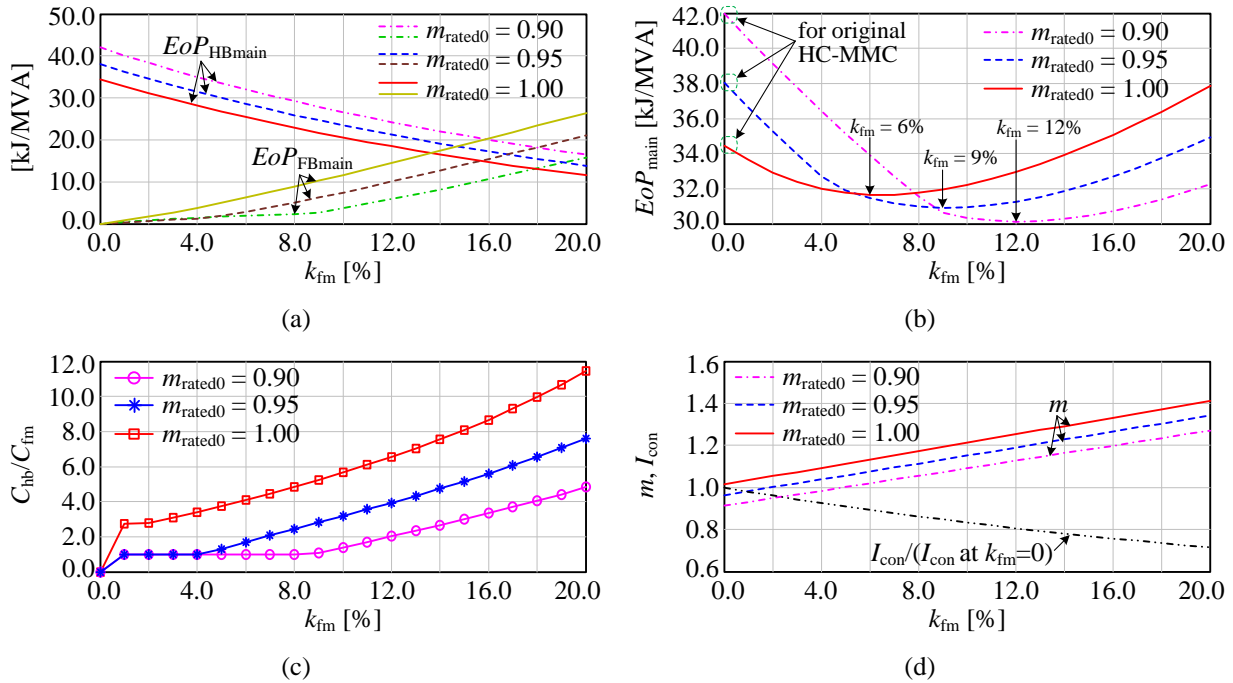


Fig. 4.19: Stored energy of all HB- and FB-SM capacitors per power rating unit and the relationship between HB- and FB-SM capacitances in the main power stage of the mixed-SM HC-MMC operating with CCSC and no 3rd harmonic injection

(a) EoP_{HBmain} and EoP_{FBmain} ; (b) EoP_{main} ; (c) SM capacitance ratio of C_{hb}/C_{fm} ; (d) operating modulation index and the converter current as base of I_{con} at $k_{fm} = 0$.

Based upon the above system parameters and $P_{dc} = 500$ MW, $V_{dc} = 500$ kV, and $N_h = 100$, the SM capacitance values in the main power stage of the mixed-SM HC-MMC are selected for both HB and FB SMs to meet the ripple requirement of $K_{ripple} = 0.1$ pu under 6 cases of k_{fm} , and the results are listed in Table 4.7. The HB- and FB-SM capacitor voltage ripple waveforms are shown in Fig. 4.20, where C_{fm} uses the same value as C_{hb} in Fig. 4.20 (a), and C_{hb} and C_{fm} use their own

designed values in Fig. 4.20 (b). As seen from Fig. 4.20 (a), the HB-SM capacitor voltage ripple waveform is different from that of FB-SM capacitor when modulation index is larger than 1.0, and the FB-SM capacitor voltage ripple is increased as k_{fm} increases. If FB-SM capacitance is properly selected based upon the charge Q_{mup0} , the capacitor voltage ripple values of both HB and FB SMs will be within the ripple requirement, as shown in Fig. 4.20 (b).

Table 4.7: HB- and FB-SM capacitance values in the main power stage of mixed-SM HC-MMC under different k_{fm}

k_{fm}	2%	4%	6%	8%	10%	12%
C_{hb}	2.3 mF	2.1 mF	1.9 mF	1.7 mF	1.6 mF	1.4 mF
C_{fm}	2.3 mF	2.1 mF	3.2 mF	4.2 mF	5.0 mF	5.6 mF

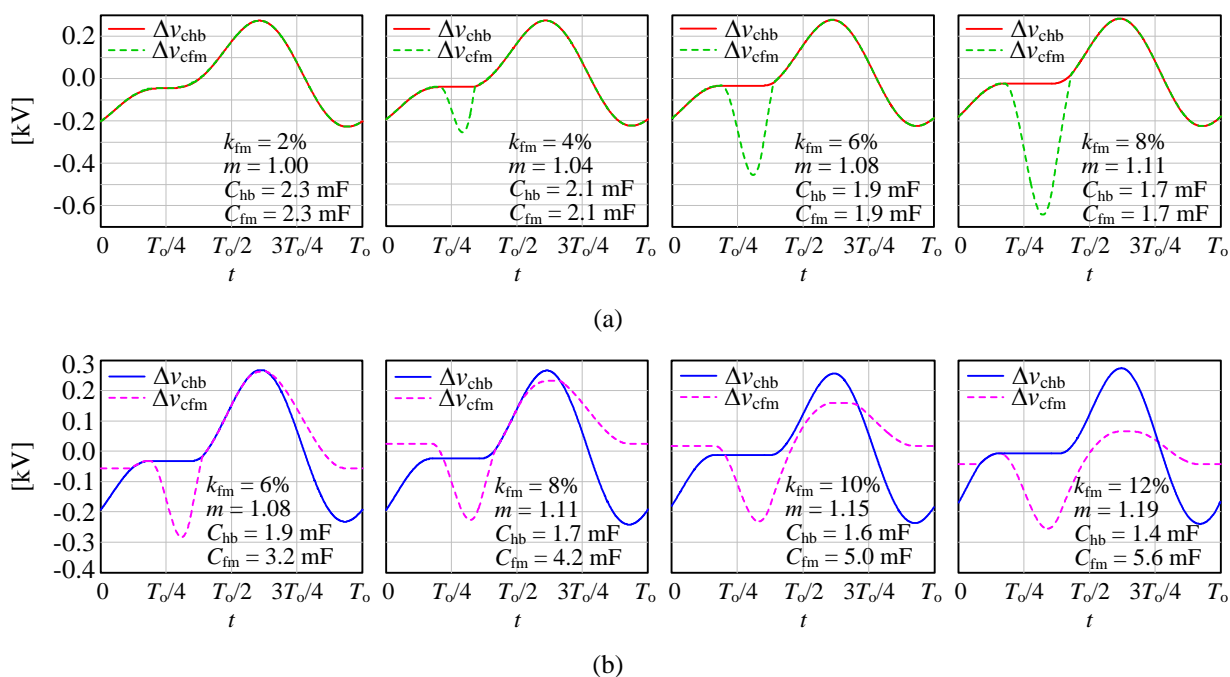


Fig. 4.20: Capacitor voltage ripple waveforms for individual HB and FB SMs in the main power stage of mixed-SM HC-MMC under different k_{fm}

(a) with $C_{fm} = C_{hb}$; (b) with $C_{fm} > C_{hb}$.

4.3.3 Capacitance design of the FB Stack in the phase limb

As seen from the operating principle introduced in Section 2.2, the voltage reference for the FB stack is equal to $v_{fbA-ref} = v_{conA-ref} - v_{mA-pu}$, where v_{mA-pu} is the per-unitized voltage crafted by

the main power stage of phase A and is influenced by the regulation method for the FB-stack capacitor voltages. In the following analysis, the proposed modified sinusoidal PWM method shown in Section 3.2.2 is used to control the capacitor voltages in the FB stack. With this method, the FB-SM capacitor-voltage regulation control loop generates the incremental Δm to adjust the modulation index of the main power stage. In steady state, the main power stage provides all the required real power to the load and the real power to compensate the small losses in the FB stack, whereas the FB stack plays the role of an active filter and operates with approximately reactive power only. Under this condition, the capacitor voltage drift of the FB stack is small in normal operation, resulting in a small Δm for the voltage reference of the main power stage. Therefore, the voltage reference of the main power stage is approximately close to that of the output phase voltage. In practice, the operating modulation index for the output phase voltage is selected within the linear modulation range. Since the modulation index increment (Δm) is small, the modulation waveform for the main power stage is approximately within the linear modulation range. Therefore, the actual voltage output from the main power stage is approximately the same as its reference, and as a result the voltage reference for the FB stack is also small (approximately zero).

Fig. 4.21 shows the PWM operation of the FB stack in both the original and mixed-SM HC-MMCs, where v_{mA-pu} is the actual voltage output from the main power stage normalized by $V_{dc}/2$; $v_{conA-ref}$ and $v_{fbA-ref}$ are the reference waveforms for the output phase voltage and the FB stack, respectively; and N_{f-in} is the required number of FB SMs to be inserted in the FB stack. As mentioned earlier, the reference for the main power stage is close to that of the output phase voltage due to the small Δm required in steady state. Therefore, it is observed from Fig. 4.21 that the voltage crafted by the main power stage is a staircase waveform and close to the output phase voltage reference. The difference between v_{mA-pu} and $v_{conA-ref}$ is within ± 0.5 , resulting in the

required number of FB SMs to be inserted to be within ± 1.0 . Based upon the sorting and balancing algorithm, the sorting function is typically enabled when the required number of inserted SMs changes. Therefore, the capacitance selection for the FB stack is based upon the individual SM capacitor voltage fluctuation.

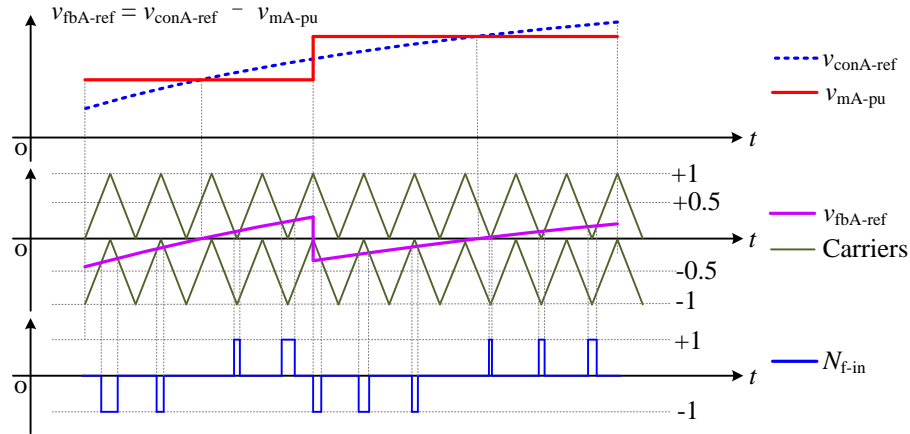


Fig. 4.21: PWM operation of the FB stack in both the original and mixed-SM HC-MMCs

As seen from the waveform of N_{f-in} shown in Fig. 4.21, its duty ratio (based upon the switching period of the FB stack) varies from period to period and within $[0.0, 0.5]$. The maximum fluctuation of the individual FB-SM capacitor is determined by the maximum electric charge. The maximum possible charge occurs at the positive and negative peaks of the phase current together with the maximum duty ratio of N_{f-in} . The maximum voltage ripple of the FB-SM capacitors in the FB stack at the positive peak point of the phase current is derived as follows:

$$\begin{aligned}
 C_{fb} \Delta v_{cfb_max} &= Q_{fb_max} = \sqrt{2} I_{con} D_{fb_max} / f_{sw_fb} \\
 \Rightarrow \Delta v_{cfb_max} &= \frac{\sqrt{2} I_{con} D_{fb_max}}{f_{sw_fb} C_{fb}}
 \end{aligned} \tag{4.71}$$

where f_{sw_fb} is the carrier frequency for the FB stack, D_{fb_max} is the maximum duty ratio of N_{f-in} . Considering the worst-case scenario that the same FB-SM capacitor is inserted at both the positive

and negative peaks of the phase current, the actual FB-SM capacitor voltage is $2\Delta v_{\text{cfb_max}}$. Denote the allowed individual SM capacitor voltage ripple percentage as K_{ripple} based upon $V_{\text{dc}}/(2N_f)$ and let $2\Delta v_{\text{cfb_max}} \leq K_{\text{ripple}} \cdot V_{\text{dc}}/(2N_f)$. The required SM capacitance in the FB stack is calculated as follows:

$$\begin{aligned}
2\Delta v_{\text{cfb_max}} &= \frac{2\sqrt{2}I_{\text{con}} D_{\text{fb_max}}}{C_{\text{fb}} f_{\text{sw_fb}}} \leq \frac{K_{\text{ripple}} V_{\text{dc}}}{2N_f} \\
\Rightarrow C_{\text{eq}} &= \frac{C_{\text{fb}}}{N_f} \geq \frac{4\sqrt{2}I_{\text{con}} D_{\text{fb_max}}}{f_{\text{sw_fb}} K_{\text{ripple}} V_{\text{dc}}} = \frac{16P_{\text{nom}} D_{\text{fb_max}}}{3m_{\text{rated}} f_{\text{sw_fb}} K_{\text{ripple}} V_{\text{dc}}^2} \sqrt{2X_0}
\end{aligned} \tag{4.72}$$

where the expressions of I_{con} and X_0 are shown in (4.6) and (4.7), respectively. Therefore, the stored energy of all FB-SM capacitors in the FB stack of a three-phase original or mixed-SM HC-MMC per power rating unit, EoP_{FBph} , is expressed as follows:

$$\begin{aligned}
EoP_{\text{FBph}} &= \frac{3N_f \cdot C_{\text{fb}} \cdot (V_{\text{dc}}/(2N_f))^2 / 2}{P_{\text{nom}}} \times 10^3 \\
&= \frac{3C_{\text{eq}} V_{\text{dc}}^2}{8P_{\text{nom}}} \times 10^3 \geq \frac{2\sqrt{2X_0} D_{\text{fb_max}}}{m_{\text{rated}} f_{\text{sw_fb}} K_{\text{ripple}}} \times 10^3 \text{ [kJ/MVA]}
\end{aligned} \tag{4.73}$$

where the maximum possible duty ratio is $D_{\text{fb_max}} = 0.5$ as seen from the waveform of $N_{\text{f-in}}$ shown in Fig. 4.21. As seen from (4.7), the value of X_0 is determined by P_{ref} , V_{acref} , and SCR. Typically, SM capacitance is selected based upon nominal operations, i.e., $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$. Therefore, EoP_{FBph} is related to SCR, independent of the number of FB SMs in the phase limb and inversely proportional to the rated modulation index (m_{rated}), the switching frequency for the FB stack ($f_{\text{sw_fb}}$), and K_{ripple} . If the transformer's turns ratio in mixed-SM HC-MMC is proportionally changed to $(1+2k_{\text{fm}})$ times that of the original HC-MMC, EoP_{FBph} for the mixed-SM HC-MMC will be $1/(1+2k_{\text{fm}})$ times that of the original HC-MMC.

Fig. 4.22 shows the value of X_0 with various SCR values under $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$ pu. It is seen that SCR changes have slight influence on X_0 value hence EoP_{FBph} . Therefore, only one

case of SCR ($= 3.0\angle 80^\circ$, resulting in $X_0 = 0.5$ under $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$ pu) is used to evaluate the range of EoP_{FBph} . With the system specifications of $\text{SCR} = 3.0\angle 80^\circ$, $f_o = 60$ Hz, $f_{\text{sw_fb}} = 27f_o$ and the ripple requirement of $K_{\text{ripple}} = 0.1$ pu, EoP_{FBph} under normal operations is in range of [6.17 kJ/MVA, 6.86 kJ/MVA] if m_{rated} is in the range of [0.9, 1.0].

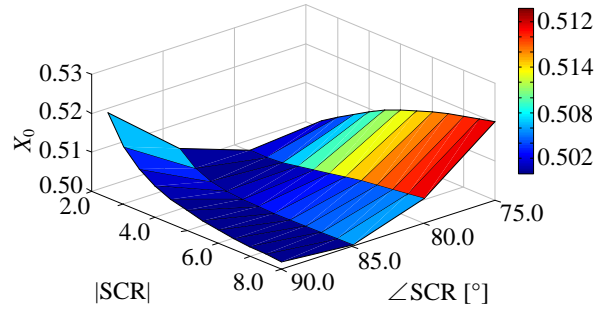


Fig. 4.22: Value of X_0 with various SCR values under $P_{\text{ref}} = 1.0$ pu and $V_{\text{acref}} = 1.0$ pu

Note that the stored energy of all FB-SM capacitors in phase limb per power rating unit is typically small under normal operation and a certain ripple requirement, since the FB stack operates with primarily zero real power and small reactive power under normal operations. The main purpose of the FB stack is to block dc faults. Therefore, the FB-SM capacitance selection for the phase limb must also consider dc-fault conditions to avoid overvoltage damage to SM capacitors, since FB-SM capacitors are charged regardless of the current direction when FB SMs are blocked. More details about such considerations under dc faults can be found in Section 6.2.3.

4.4 Experimental validation of capacitance design

In order to validate the analysis of SM capacitor sizing for both the original and mixed-SM HC-MMCs, a laboratory setup of three-phase HC-MMCs is built and controlled by a RTDS as inverters. A general diagram of the developed laboratory setup is displayed in Fig. 4.23. As shown all sampled data and signals for protection detection from the MMC setup are sent to RTDS using

gigabit transceiver analogue input (GTAI) and gigabit transceiver digital input (GTDI) boards via fiber optic connections, and RTDS sends out gate signals using gigabit transceiver digital output (GTDO) boards to all SMs in the setup. The specifications of this setup are listed in Table 4.8.

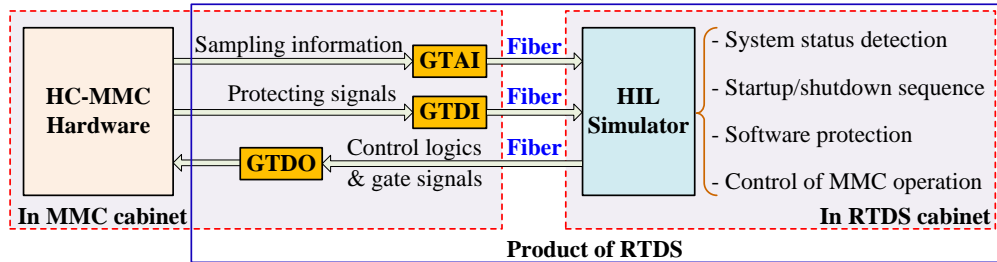


Fig. 4.23: General diagram of the laboratory setup of HC-MMCs controlled by RTDS

Table 4.8: System specifications of laboratory setup of three-phase HC-MMCs

Rated dc-link voltage: 240 V	Rated power: 5.0 kW	Fundamental frequency: 60 Hz	
# of SMs	12 HB/arm, 6 FB/limb, 2 FB/arm for mixed-SM HC-MMC		
SM capacitance	4.7 mF for all SM capacitors	Arm inductance	5.0 mH
Nominal capacitor voltage	20.0 V for all SM capacitors	Arm resistor	1.0 Ω
Modulation method	PD-PWM ($9f_o$ for main power stage and $27f_o$ for the FB stack)		
Semiconductors	MOSFET: IPP045N10N3 (100 V, 137 A and ON-resistance $r_{ds} = 4.5$ m Ω) Diode: STPS30100ST (100 V, 30 A and forward voltage drop $V_F = 0.385$ V)		
Inductive loads	$R_{load} = 12.6 \Omega, 20.0 \Omega, 30.0 \Omega, 40.0 \Omega$ and 60.0Ω ; $L_{load} = 10.0$ mH and 35.0 mH		

Both the original and mixed-SM HC-MMC have 12 HB SMs per arm and 6 FB SMs per phase limb, and there are 2 additional FB SMs per arm in the main power stage of the mixed-SM HC-MMC, resulting in 90 and 102 SMs for the three-phase original and mixed-SM HC-MMCs, respectively. Therefore, the original and mixed-SM HC-MMCs require 90 and 102 analog sampling channels to sample all SM capacitor voltages, and 108 and 132 digital output channels to send out gate signals, respectively. In addition, there are other sampling requirements, such as six samples for arm currents, three samples for ac-side voltages, and two samples for dc-side voltage and current. In the present setup, each GTAI board has 12 analog input channels, and there are 64 digital channels in each GTDO board. As such, the original and mixed-SM HC-MMC need 9 and 10 GTAI boards, and 2 and 3 GTDO boards, respectively, which will be costly. To reduce

the required number of GTAI boards to save space and cost, a multiplexer (IDTQS4A215) is used to sample the large number of SM capacitor voltages in a sequence.

Under the conditions of $V_{dc} = 240V$, $R_{load} = 20.0 \Omega$, and $L_{load} = 10 \text{ mH}$, the experimental waveforms of the original and mixed-SM HC-MMCs are shown in Fig. 4.24 with and without CCSC. It is observed that the voltage level changes in the three-phase voltages are approximately 20.0 V. This indicates that all SM capacitor voltages are approximately maintained at 20.0 V and the laboratory setup works properly and as expected.

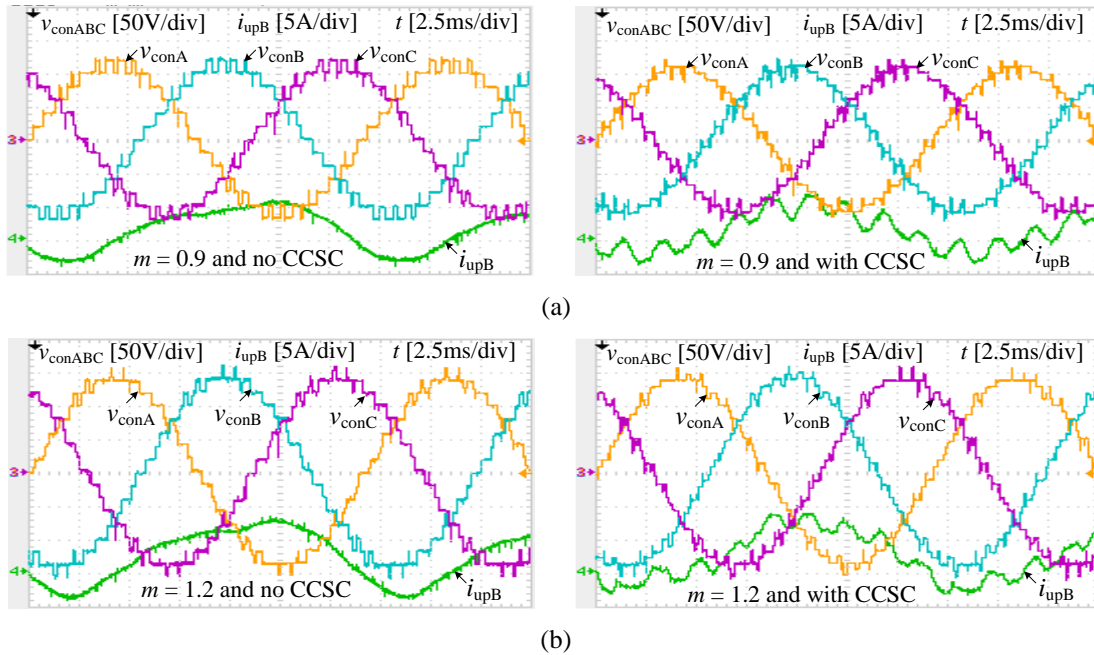


Fig. 4.24: Experimental waveforms of three-phase voltages and phase-B upper-arm current under $R_{load} = 20.0 \Omega$, $L_{load} = 10.0 \text{ mH}$ and with (without) CCSC

(a) for original HC-MMC with $m = 0.9$ and $V_{dc} = 240V$; (b) for mixed-SM HC-MMC with $m = 1.2$ and $V_{dc} = 240V$.

Operation with different loads was used to validate the theoretical analysis of SM capacitor ripple waveforms and values. Theoretical and experimental values of SM capacitor voltage ripples are compared in the following subsections for the original and mixed-SM HC-MMCs, where the theoretical calculations ignore the high-order harmonics due to their negligible contribution to the 2nd harmonic and capacitor voltage ripple [86].

4.4.1 Validations for original HC-MMC

With an inductive load of $R_{load} = 12.6 \Omega$ and $L_{load} = 10.0 \text{ mH}$, the comparison between experimental and theoretical results of instantaneous SM capacitor voltage ripple and arm current waveforms for the original HC-MMC operating with and without CCSC is shown in Fig. 4.25. In the theoretical calculations of arm currents, the dc and 1st components are considered for the operation with CCSC and the additional 2nd component is considered for the operation without CCSC. It is seen that the experimental waveforms are well matched with the theoretical results. This validates the theoretical analysis of SM capacitor voltage ripple waveform shown in Section 4.2. Therefore, the SM capacitor sizing based upon the ripple waveform derived in Section 4.2 has valid foundations.

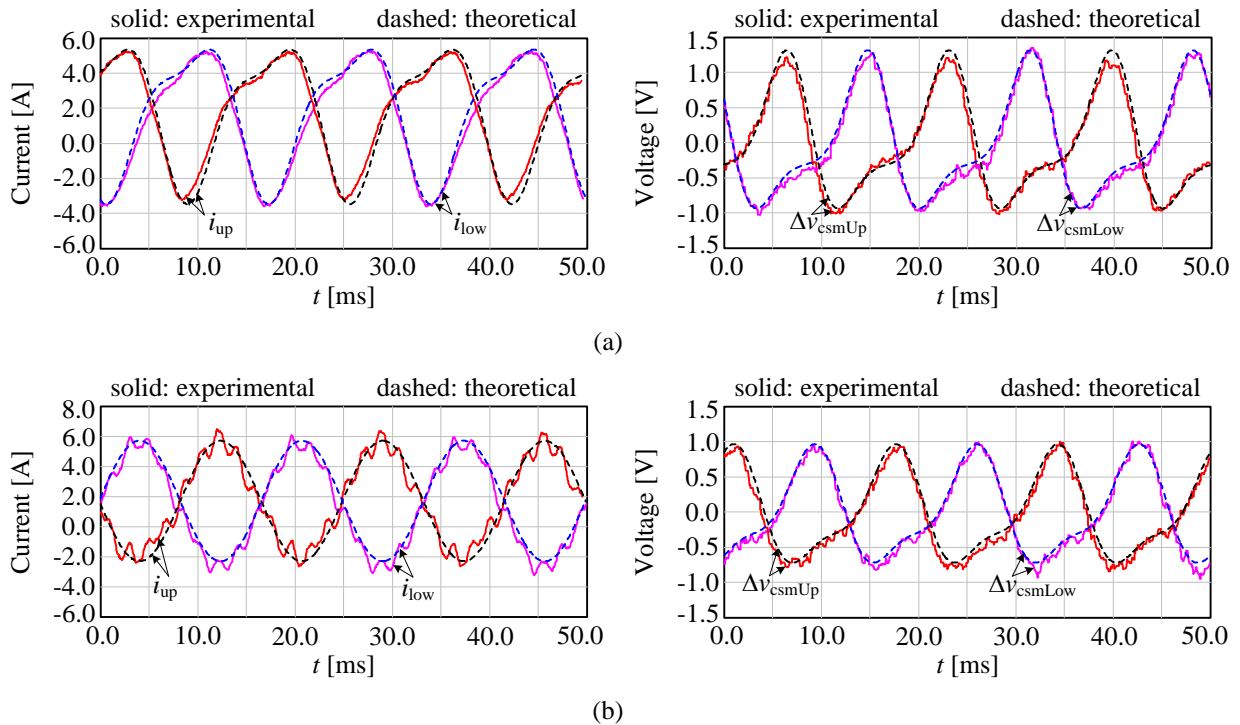


Fig. 4.25: Comparison between the experimental and theoretical results of arm currents and capacitor voltage ripple for original HC-MMC operating with $m = 0.9$, $R_{load} = 12.6 \Omega$, and $L_{load} = 10.0 \text{ mH}$

(a) without CCSC; (b) with CCSC.

As seen from (4.45) for SM capacitance selection, the theoretical ripple value can be calculated by substituting the known SM capacitance. With loads composed of various resistors and 10.0 mH or 35.0 mH inductors, the theoretical and experimental ripple values of SM capacitor voltage are analyzed and compared in Fig. 4.26, where the SM capacitor voltage ripple value is calculated and averaged based upon 100 fundamental periods. It is observed that the experimental results match the theoretical results very well. Therefore, it validates the calculations used for SM capacitor sizing shown in Sections 4.3.1.1 and 4.3.1.2.

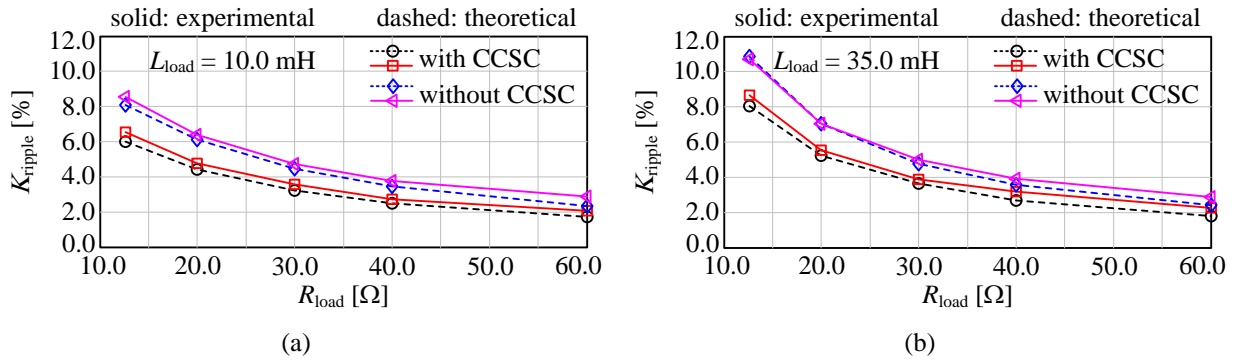


Fig. 4.26: Comparison between the experimental and theoretical results of SM capacitor voltage ripple values for original HC-MMC under different loads

(a) with $L_{\text{load}} = 10.0$ mH; (b) with $L_{\text{load}} = 35.0$ mH

4.4.2 Validations for mixed-SM HC-MMC

For the mixed-SM HC-MMC operating with and without CCSC, Fig. 4.27 shows the comparison between experimental and theoretical results of instantaneous HB- and FB-SM capacitor voltage ripple waveforms and arm currents in the main power stage under an inductive load ($R_{\text{load}} = 20.0 \Omega$ and $L_{\text{load}} = 10.0$ mH). In the theoretical calculation of arm currents without CCSC, the 2nd harmonic current is calculated by regarding the mixed-SM HC-MMC as the original HC-MMC with the FB SMs as redundant SMs in the main power stage, because the number of FB SMs is small. As seen from Fig. 4.27, the experimental HB-SM capacitor voltage ripple waveforms

(Δv_{chbUp}) are close to the theoretical results, and the experimental FB-SM capacitor voltage ripple waveforms (Δv_{cfmUp}) appear to contain discontinuities. This is because only two FB SMs per arm are used in the main power stage and there is less chance to rotate SMs to insert for charging or discharging, since the sorting and rotating function is enabled when the number of inserted SMs changes. However, the traces of Δv_{cfmUp} are close to the theoretical waveforms in the operation with and without CCSC. The experimental results of arm currents are well matched with the theoretical results in the operation without CCSC (see Fig. 4.27 (a)), and their traces (without harmonics) are close to the theoretical results in the operating with CCSC. This validates the ripple waveform analysis for the main power stage in the mixed-SM HC-MMC shown in Section 4.3.2, which is the main concept used for SM capacitor sizing in mixed-SM HC-MMC.

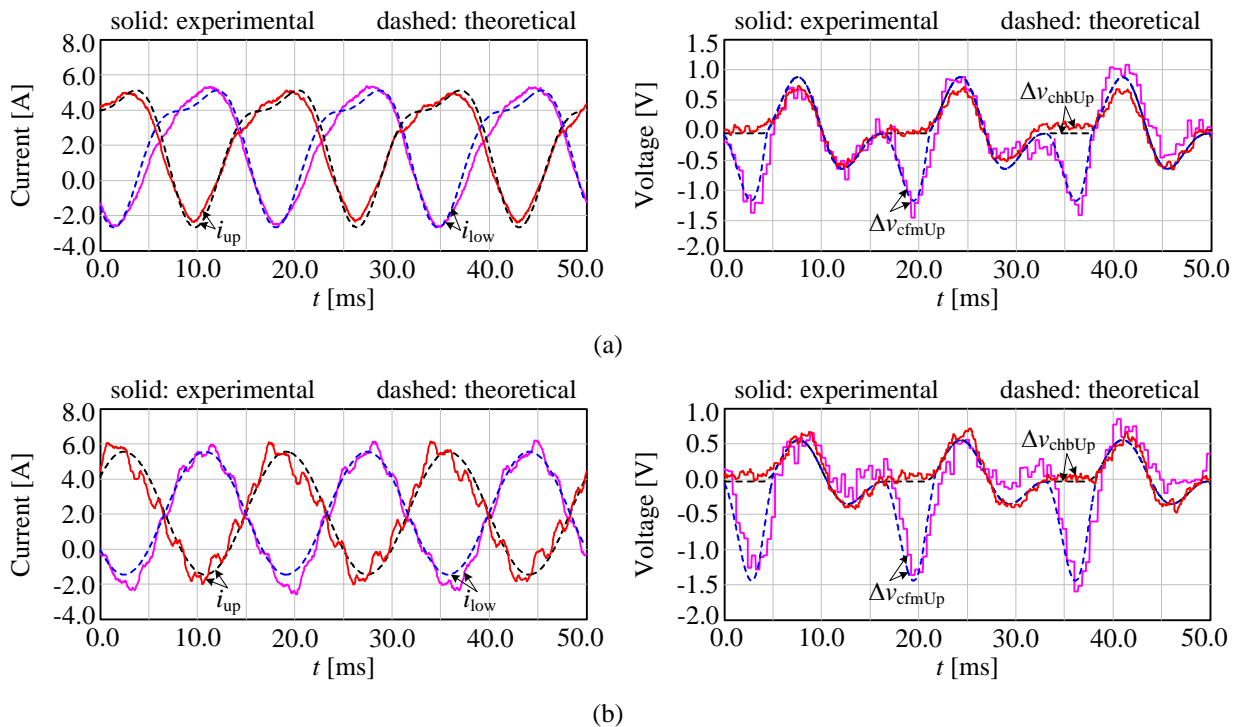


Fig. 4.27: Comparison between the experimental and theoretical results of arm currents and capacitor voltage ripple for mixed-SM HC-MMC operating with $m = 1.2$, $R_{\text{load}} = 20.0 \Omega$ and $L_{\text{load}} = 10 \text{ mH}$.

(a) without CCSC; (b) with CCSC.

Based upon the algorithm shown in Section A.2 and with the known operating conditions and SM capacitance values, the theoretical HB- and FB-SM capacitor voltage ripple waveforms in the main power stage of the mixed-SM HC-MMC can be readily obtained. With the loads composed of various resistors and 10.0 mH or 35.0 mH inductors, the theoretical and experimental ripple values of SM capacitor voltages are analyzed and compared in Fig. 4.28, where the SM capacitor voltage ripple value is calculated and averaged based upon 100 fundamental periods. It is observed that the experimental results match the theoretical results very well. Therefore, it validates the calculations used for SM capacitor sizing shown in Section 4.3.2.

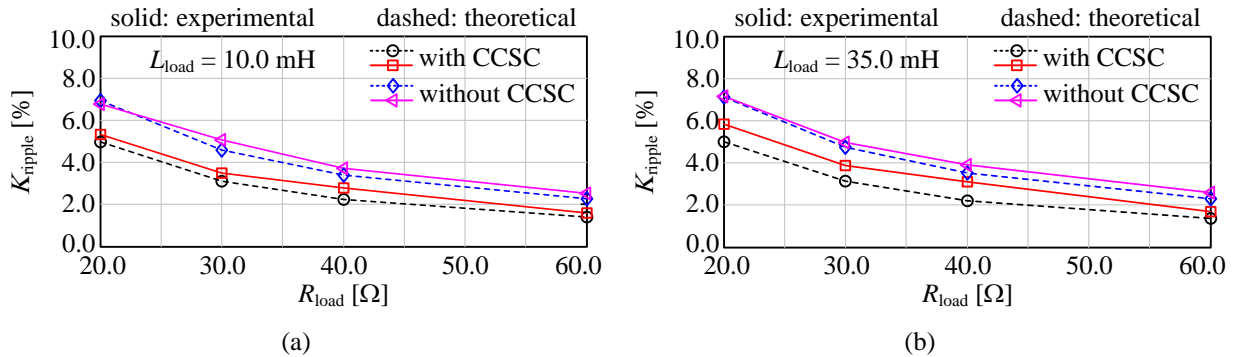


Fig. 4.28: Comparison between the experimental and theoretical results of SM capacitor voltage ripple values for mixed-SM HC-MMC under different loads

(a) with $L_{load} = 10.0$ mH; (b) with $L_{load} = 35.0$ mH

4.5 Summary and key contributions

To facilitate the analysis of SM capacitor sizing in both the original and mixed-SM HC-MMCs, the theoretical operating point of a VSC connected to an ac grid was derived considering the interface transformer and the ac system strength. The underlying concepts using the variation of electric charge to obtain the SM capacitor voltage ripple waveform were introduced for HB-MMC. Based upon the SM capacitor voltage ripple waveform, the 2nd harmonic current was derived to a better accuracy compared to methods in existing literature [85] for HB-MMC operating without

CCSC, which is also suitable for the original and mixed-SM HC-MMCs. The theoretical analysis of 2nd harmonic current and SM capacitor voltage ripple waveform was validated by both EMT simulations and experiments. The SM capacitance sizing using stored energy of SM capacitors per power rating unit was studied for both the original and mixed-SM HC-MMCs. The influence of system parameters on the stored energy of SM capacitors per power rating unit was comprehensively investigated under normal operation. Lastly, a laboratory-scale experimental setup was used to validate the effectiveness and correctness of the calculated stored energy of SM capacitors per power rating unit with respect to the SM capacitor voltage ripple. The experimental results of SM capacitor voltage ripple were close to those obtained by theoretical calculation.

Key observations from this chapter are listed as follows:

- Given a 10% SM capacitor voltage ripple, the stored energy of all HB-SM capacitors in the main power stage of the original HC-MMC (EoP_{HBmain}) is required to be in the range of [33.0 kJ/MVA, 41.0 kJ/MVA] with CCSC and [44.0 kJ/MVA, 65.0 kJ/MVA] without CCSC;
- The original HC-MMC operating with 3rd harmonic injection requires slightly smaller EoP_{HBmain} to select the SM capacitance;
- With transformer's turns ratio proportionally changed, the stored energy of all HB- and FB-SM capacitors in the main power stage of mixed-SM HC-MMC can have an optimal value in the range of [30.0 kJ/MVA, 32.0 kJ/MVA] by adding 6%~12% FB SMs into the main power stage with rated modulation index of approximately 1.12;
- The stored energy of all FB-SM capacitors in the phase limb per power rating unit (EoP_{FBph}) is inversely proportional to the rated modulation index, the switching frequency for the FB stack, and K_{ripple} . Given a 10% SM capacitor voltage ripple, EoP_{FBph} is required to be approximately 6.5 kJ/MVA with $27f_o$ switching frequency.

Chapter 5

Loss Evaluation under Different Voltage-Regulation

Methods

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Apart from proper design of system parameters, loss evaluation of HC-MMCs is also of importance as it influences the cooling system and footprint of converters. In order to optimize SM packaging and thermal management solutions, it is critical to evaluate the semiconductor losses incurred during conduction intervals and switching events. Equally importantly, making proper decisions on the selection of topologies and control schemes, including firing pulse generation, SM capacitor voltage balancing and regulation and system controls, requires reliable estimations of semiconductor losses [33]-[34], [40], [72]. Quantification of losses is necessary to devise control methods to lower converter losses particularly in high-power applications, where even small reductions in losses imply significant gains in cooling and operating costs over the converter station's lifetime.

This chapter investigates the losses of HC-MMCs under different SM capacitor-voltage regulation methods for the FB stack, which are discussed in detail in Section 3.2. The method proposed in [34] adopts a trapezoidal PWM method, which introduces a heavy filtering burden for the FB stack to achieve a high-quality phase voltage at the converter terminals. The heavy filtering burden on the FB stack implies more switching actions and increased losses. To improve the SM capacitor-voltage regulation, two novel methods based upon a modified sinusoidal PWM scheme were introduced in Section 3.2, wherein the performance comparisons between different voltage regulation methods were made. The analysis in Section 3.2 demonstrated that the newly proposed control method and topology modification not only extend the converter's linear-regulation range but also reduce the filtering burden of the FB stack. The aim of this chapter is to systematically analyze and quantify semiconductor losses of HC-MMCs under different operating conditions and with different methods to regulate the FB-SM capacitor voltages in the phase limb.

Utilizing mathematical or computer simulation models to assess converter losses is a common practice in high-power applications, where experimental investigations are prohibitively difficult [61]-[68]. Furthermore, loss calculation of MMCs is challenging due to the irregularity of switching events in SMs, caused by SM capacitor voltage balancing schemes. To consider the influences of control schemes, this chapter utilizes the simulation-based method proposed in [70] to estimate the semiconductor losses. This method calculates the semiconductor losses based upon the corresponding voltage and current waveforms obtained from EMT simulation of the converter together with its control schemes. The findings of loss comparisons are useful in assessing the relative merits of different FB-SM capacitor-voltage regulation methods for HC-MMCs. In addition, the quantitative loss comparisons between HC-MMC and FB-MMC are provided, since FB-MMC is a conventional MMC topology that possesses topological dc-fault blocking capability.

The remainder of the chapter is organized as follows: the preliminaries of loss evaluation from literature is presented in Section 5.1. The switching characteristics of semiconductors and the extensively-used loss calculation method based upon simulations are discussed in Section 5.2. Semiconductor loss comparisons between five considered MMCs are made in Section 5.3. Lastly, the major conclusions of this chapter are presented in Section 5.4.

5.1 Preliminaries of loss evaluation

A significant volume of research work has been dedicated to investigating switching and conduction losses of power electronic circuits [61]-[68]. Generally, conduction losses are readily obtained as the product of the forward saturation voltage and the conducting current. However, the calculation of switching losses in MMCs becomes complicated due to the irregularity of switching events and the presence of a large number of switches operating under pulsating dc capacitor voltages (due to SM capacitor voltage balancing algorithms) [61], [63]. Therefore, existing calculation methods for switching losses in MMCs are often based upon simplifying assumptions and approximations. These may include:

(i) Assuming that MMCs operate with sinusoidal ac currents, constant dc-link voltage, ideal SM capacitors, and sinusoidal modulating signals. This simplifies the expressions for voltage, current, and duty cycle [61]-[66];

(ii) Assuming that losses are equally distributed among the converter's arms; i.e., all SMs incur the same average amount of losses, and only one SM is taken into consideration [61];

(iii) Assuming switching events are uniformly distributed over the fundamental cycle regardless of the impact of SM capacitor voltage balancing algorithms [63]-[64];

(iv) Considering the influence of the balancing methods on switching losses, the averaged or maximum switching actions are used to count the switching events per cycle [62]-[63];

(v) Assuming that switching losses are linearly or piecewise-linearly proportional to current or the product of current and voltage at the switching events using switching-energy curves if provided in device datasheets [63]-[66];

To estimate semiconductor losses considering the impact of converter's control schemes, EMT simulation-based loss calculation methods have attracted much attention [67]-[70]. In these methods, the electrical network solution is obtained using simple ON-OFF switching models, which have no representations of the physics of switching transients. The semiconductor losses are externally estimated using specialized algorithms [67], [70] to create switching transient waveforms based upon the pre- and post-switching voltages and currents. To include the influence of temperature variations, a temperature correction factor is introduced in [70] to correct the semiconductors' forward saturation voltage. It is exceedingly helpful for EMT simulators to have provisions to concurrently calculate semiconductor losses while simulating the system-level electrical behavior. Since no detailed physics of switching transients are simulated, the EMT simulation-based methods for loss calculation permit relatively large simulation time-steps, which significantly reduces the computation cost. The method proposed in [70] has been extensively used in several studies of MMC losses and is shown to produce reliable loss estimations [68]-[70]. In this chapter, the method proposed in [70] is used for the loss calculations of the considered MMCs.

5.2 Overview of the EMT-based loss calculation method

Semiconductor losses are divided into four categories of insulated gate bipolar transistor (IGBT) conduction and switching losses and diode conduction and reverse-recovery losses.

Conduction losses are readily calculated using the product of the device's current and forward saturation voltage. However, calculations of the switching losses of an IGBT and the reverse-recovery losses of a diode are much more complicated, especially the turn-on switching losses. Turn-on switching characteristics of an IGBT are tightly related to the stray inductance of the conduction path and the reverse-recovery characteristic of a diode. Consider the simple circuit in Fig. 5.1 that is used to describe the switching characteristics of IGBTs and diodes, where the dotted inductor denotes the stray inductance of the conduction path, which has a distributed nature, and the dotted capacitors denote the stray capacitance mainly determined by the output capacitance of semiconductors.

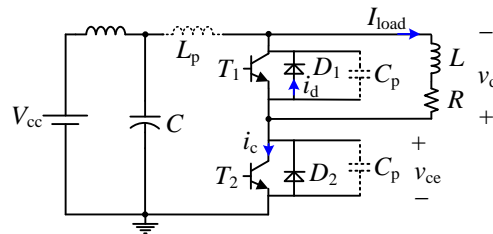


Fig. 5.1: Simple circuit to test the switching characteristics of IGBTs and diodes

Fig. 5.2 (a) and (b) show the characteristic waveforms of the switching events of IGBT and diode (reverse recovery), where Δt is the simulation time-step, t_0 represents the starting point of one time-step in an EMT simulator, and the gate signal changes its status at t_0 . In order to clearly show the switching transient waveforms, the duration of the switching transients is significantly magnified compared to the simulation time-step. As seen from Fig. 5.1 and Fig. 5.2 (a), during $[t_0, t_1]$, T_2 in Fig. 5.1 is switched on at t_0 ; however, the IGBT actually starts to conduct at t_1 when the gate signal (v_g) reaches the IGBT's threshold voltage (V_{th}), and the turn-on delay, $t_{d(on)}$, depends on the IGBT itself. In $[t_1, t_3]$, the IGBT's conducting current (i_c) increases with an approximately constant slope, which depends on the reverse-recovery speed of the commutating diode D_1 . These two devices, T_2 and D_1 , are commonly known as a switching pair [87]. When the diode current (i_d)

becomes negative after t_2 , current i_c exceeds its steady-state value (I_{c0}) to meet the load current (I_{load}). Since diode D_1 conducts positive current throughout $[t_0, t_2]$, voltage v_d across D_1 stays around its conduction voltage-drop value (v_{ds}). Additionally, voltage v_{ce} across T_2 decreases from its steady-state value (V_{ce0}) to an intermediate value for a short time, a phenomenon known as the Miller effect [88]. In $[t_3, t_4]$, current i_d increases to zero whereas the IGBT's conducting current decreases to the value of load current. The reverse-recovery operation of diode approximately ends at t_4 and voltage v_d increases to its steady-state reverse voltage value (V_{d0}), whereas voltage v_{ce} falls to its saturated voltage value (v_{ces}). The turn-off transient of an IGBT mainly depends on its own turn-off characteristic. As seen from Fig. 5.2 (b), there is a turn-off delay, $t_{d(off)}$, after the turn-off command, in which v_{ce} increases, whereas i_c stays at its steady-state value. Thereafter, v_{ce} increases while i_c rapidly falls to its tail current value and takes a while to reach zero.

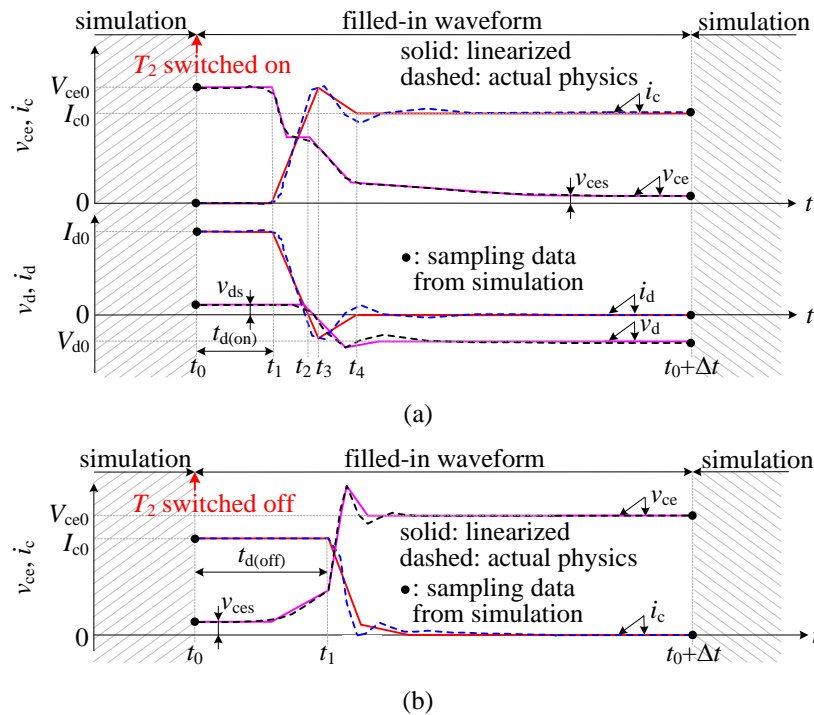


Fig. 5.2: Piecewise linear approximations for hard switching transient waveforms (a) turn-on transients for IGBT and reverse-recovery transients for diode; (b) turn-off transients for IGBT.

An EMT simulator using conventional ON-OFF switching models cannot represent the detailed switching physics. To calculate the switching losses, piecewise linear approximations of transient switching waveforms, as shown in Fig. 5.2, are theoretically constructed based upon the pre- and post-switching voltage and current waveforms that are obtained from the previous and next time-steps [70]. The closed-form expressions for switching losses are shown in [70] in detail, which are used in an EMT simulator to calculate the switching losses for each switching event that are then added to the conduction losses to obtain the overall losses. Since these closed-form expressions replace the actual waveforms during a switching event, simulation time-steps do not need to be reduced thus saving computational load.

Several parameters, as listed in Table 5.1, are needed to form the piecewise linear approximations of device switching characteristics as described in [70]. The parameters related to the semiconductors, such as the on-state saturation voltage and diode peak reverse-recovery current, can be found in the device datasheets, whereas the stray inductance and capacitance in the conducting path are generally tested from the circuit, obtained from detailed physics-based simulations, or estimated by experience. In this thesis, these stray parameters use the recommended values in the semiconductor's datasheet.

5.3 Loss comparisons of the considered MMCs

Based upon the described loss estimation method, a conventional FB-MMC and HC-MMCs operating with the three capacitor-voltage regulation methods presented in Section 3.2 are simulated in PSCADTM/EMTDCTM simulator to compare their semiconductor losses. For referencing, the simulated MMCs are labelled 1-5 as follows: MMC₁: FB-MMC, MMC₂: HC-

MMC with the modified sinusoidal PWM, MMC₃: HC-MMC with the trapezoidal PWM, MMC₄: HC-MMC with 5% mixed SMs, and MMC₅: HC-MMC with 10% mixed SMs.

A schematic diagram of the simulated system and its controls are shown in Fig. 5.3. These five MMCs are operated with PD-PWM and are connected to an ac grid. The real power and ac voltage magnitude at the PCC are controlled. The conventional FB-MMC is controlled to operate as HB-MMC and is analyzed as it has dc-fault blocking capability similar to an HC-MMC. The following loss comparisons are based upon various operating points determined by the control orders.

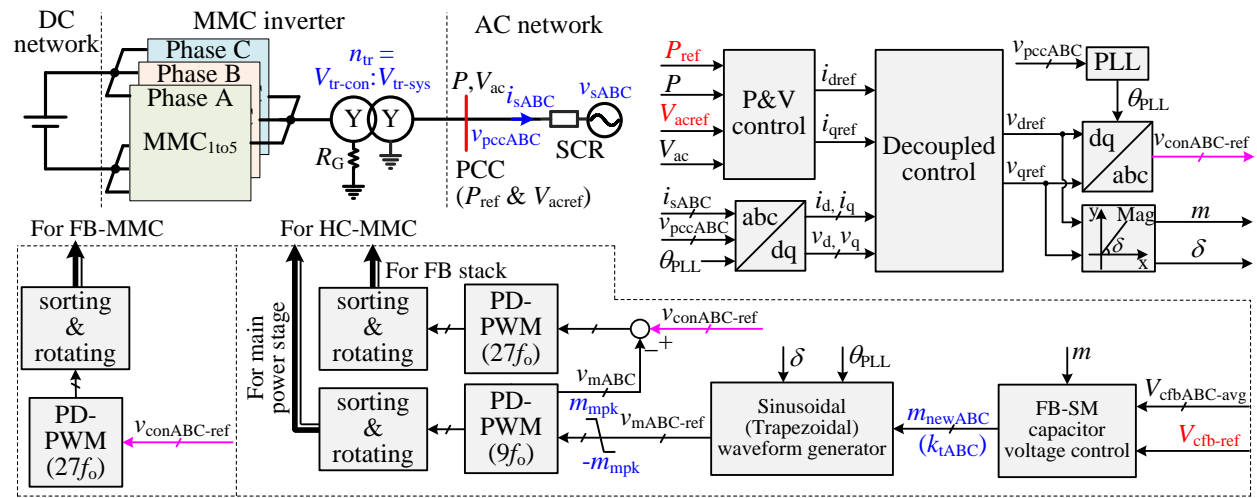


Fig. 5.3: Simulation system of three-phase MMCs for loss evaluation

5.3.1 Conditions for a fair loss comparison

To compare the losses of the investigated MMC topologies in a fair manner, the considered MMCs are designed for the same HVDC transmission system using the same semiconductor devices. The following additional conditions have also been included:

- (i) Rated dc- and ac-side system voltages and currents are identical for all MMCs;
- (ii) All SMs have same nominal capacitor voltages to enable usage of the same semiconductors;

(iii) The MMCs have similar potentials to deal with ac voltage fluctuations; i.e., all the considered MMCs are designed to craft the same maximum voltage at the PCC when operating with their corresponding maximum modulation indices. In this case, the transformer's turns ratio (seen from the converter-side to the grid-side) in the mixed-SM HC-MMC will increase to $(1+2N_{fm}/N_h)$ times of that in the original HC-MMC;

(iv) The MMCs produce approximately identical harmonic quantity at the phase or line voltage.

In this chapter, the IGBT ST1500GXH24 with 4.5-kV and 1.5-kA ratings (identical to the switch used in [68]) is used. Using the datasheet of this device, the parameters needed for the loss simulations are listed in Table 5.1. In estimating the losses, it is assumed that cooling system maintains a temperature of 40 °C.

Table 5.1: Loss-estimation parameters

Part number of IGBT module: ST1500GXH24		
Stray inductance (L_p): 330 nH	Stray capacitance (C_p): 5.0 nF	IGBT saturation voltage (V_{ces}): 3.0 V
Turn-on delay time ($t_{d(on)}$): 600.0 ns	Turn-on rising time (t_r): 400.0 ns	Diode saturation voltage (V_{ds}): 3.2 V
Turn-off delay time ($t_{d(off)}$): 7500.0 ns	Turn-off falling time (t_f): 2500.0 ns	Reverse recovery time (t_{rr}): 1300.0 ns

To sufficiently protect this IGBT from overvoltage and overcurrent, the nominal voltage and continuous current stresses are set as 2.25 kV (100% margin) and 1.0 kA (50% margin), respectively. Subsequently, the nominal SM capacitor voltage is set as 2.25 kV, whereas the RMS phase current is set as 1.0 kA as this IGBT is also used in the FB stack of HC-MMC. To limit the computational burden of EMT simulations for MMCs with hundreds of loss-enabled switch models [70], 20 SMs per arm are used for both FB-MMC and HC-MMC. As such a 45-kV dc-link voltage and up to 480 semiconductors for the three-phase FB-MMC (see Table 5.2) are used. The nominal modulation index is set as 0.95 for both the FB-MMC and the HC-MMC to obtain considerable voltage utilization and linear-range operation. As such, the inverter-side RMS line

voltage is 26.18 kV and the real power is 45.0 MW. In most MMC applications, the arm inductors serve to suppress current harmonics and curb the di/dt of the fault current, and their value is generally selected as approximately 0.15 pu on the ac system base impedance [89]. Here, a 0.0045-H arm inductance is used for all considered MMCs, which is approximately 0.175 pu of the ac system base impedance. The detailed specifications of the HVDC system used to estimate the losses of the five considered MMCs are shown in Table 5.2.

Table 5.2: Specifications for FB-MMC and HC-MMCs

Parameter	MMC ₁	MMC ₂	MMC ₃	MMC ₄	MMC ₅	
Rated power	45.0 MW					
AC grid	Line voltage (RMS): 20.9 kV, frequency: 60 Hz, SCR = $3.0\angle 80^\circ$					
DC side ratings	45.0 kV, 1.0 kA					
Arm inductance	0.0045 H					
SM capacitor voltage	2.25 kV for both arm and phase SMs					
SM capacitance	8.0 mF and 2.0 mF for the arm and phase SMs, respectively					
Transformer	Rating	54.0 MVA				
	Ratio (conv./sys.)	26.18 kV/20.9 kV		28.80 kV/20.9 kV	31.42 kV/20.9 kV	
Switching frequencies	1620 Hz	Main power stage: 540 Hz, Phase limb: 1620 Hz				
Modulation method	PD-PWM (see Fig. 2.1 (a))					
SMs	Arm	20 (FB)	20 (HB)	20 (HB)	20 (HB), 1 (FB)	20 (HB), 2 (FB)
	Limb	N/A	10 (FB)	10 (FB)	10 (FB)	10 (FB)
Total # of switches	480	360	360	384	408	

Based upon the specifications shown in Table 5.2, conditions (i) and (ii) listed above in this section, are well satisfied. Neglecting the voltage across the leakage inductance of transformers, the peak value of the phase voltage at PCC is approximately $(m_{\max} \cdot V_{dc}/2)/n_{tr}$, where n_{tr} is the turns ratio of transformer seen from the converter side to the grid side (see Fig. 5.3). Since MMCs 4 and 5 extend the maximum modulation indices by 1.1 and 1.2 times, respectively, higher than that of MMC₂ (see Table 3.2), the turns ratios of the transformers used in MMCs 4 and 5 should be 1.1 and 1.2 times, respectively, higher to satisfy condition (iii). Therefore, the converter-side line

voltages of the transformer are set to 28.80 kV ($= 1.1 \times 26.18$ kV) and 31.42 kV ($= 1.2 \times 26.18$ kV) for MMCs 4 and 5, respectively.

Although THD is commonly used to evaluate the voltage quality, it is important to ensure that the considered MMCs have similar overall harmonic spectra to achieve condition (iv). This requires comparable single harmonic distortion (SHD) among MMCs. With the specifications shown in Table 5.2, the nominal modulation indices for MMC₁₋₃, MMC₄ and MMC₅ are 0.95, 1.045 ($= 1.1 \times 0.95$) and 1.14 ($= 1.2 \times 0.95$), respectively. Fig. 5.4 and Fig. 5.5 show the waveforms and harmonic spectrum of the phase voltage under nominal conditions for FB-MMC (MMC₁) and four hybrid MMCs (MMC₂₋₅) under ($9f_0$, $27f_0$) switching frequencies, respectively, where f_0 represents the fundamental frequency; $9f_0$ is used for the main power stages in MMC₂₋₅ and $27f_0$ is used for MMC₁ and for the FB stacks in MMC₂₋₅. Fig. 5.5 shows that the four HC-MMCs all have dominant harmonics at $27f_0$. As such, the switching frequency for FB-MMC is set at the same value. As seen from Fig. 5.4 and Fig. 5.5, MMCs 1-3 all have virtually identical harmonic spectra and a THD of 6.1%, whereas MMCs 4 and 5 have slightly lower THDs of 5.1% and 5.0%, respectively. Lower THDs for MMCs 4 and 5 are achieved due to the additional voltage levels (23 for MMC₄ and 25 for MMC₅).

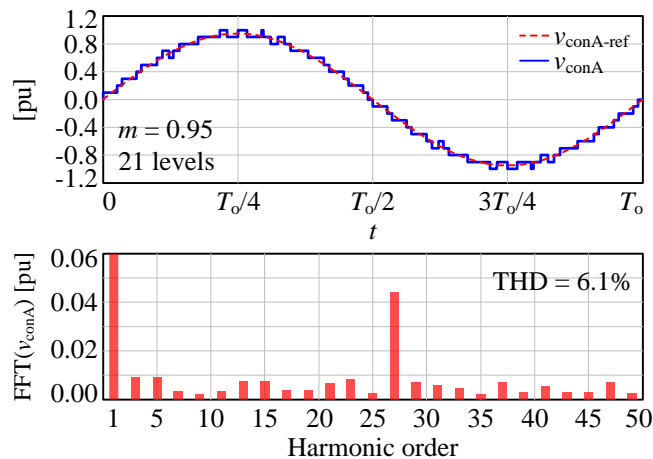


Fig. 5.4: Waveforms and FFT of phase voltage under nominal operation and $27f_0$ switching frequency for FB-MMC

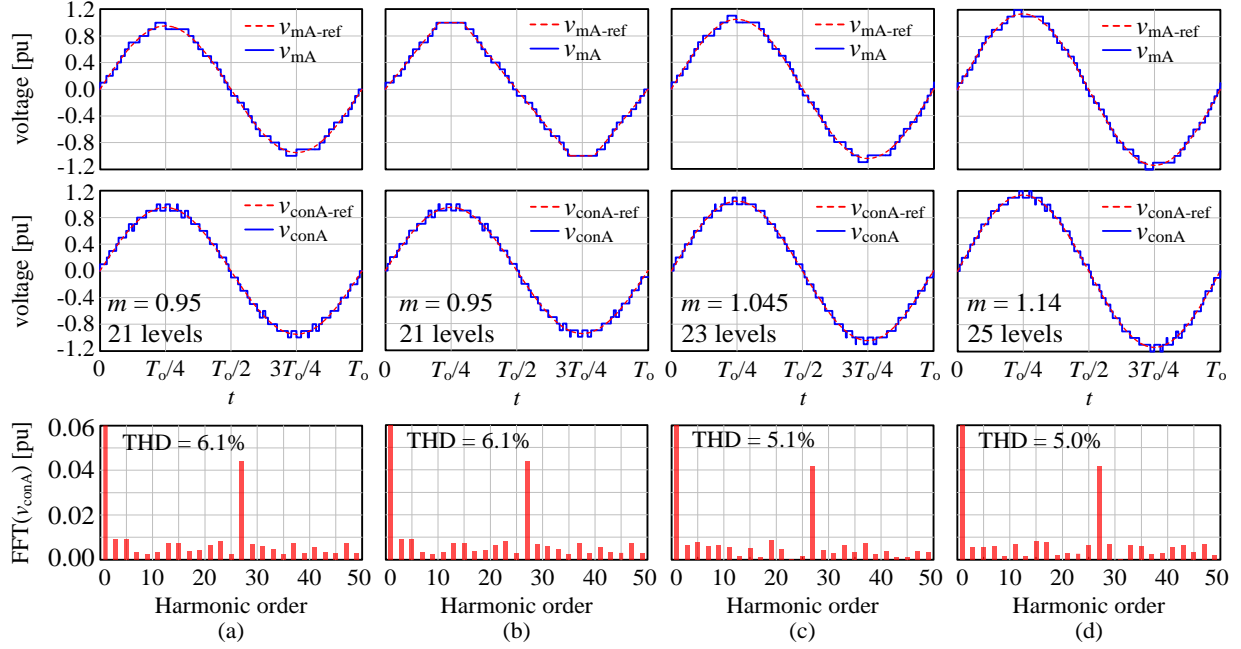


Fig. 5.5: Waveforms and FFT of phase voltages under nominal operations and $(9f_o, 27f_o)$ switching frequencies (a) HC-MMC with sinusoidal PWM (MMC₂); (b) HC-MMC with trapezoidal PWM (MMC₃); (c) HC-MMC with 5% mixed SMs (MMC₄); (d) HC-MMC with 10% mixed SMs (MMC₅).

5.3.2 Loss comparisons between the considered MMCs

With the specifications in Table 5.2, the hardware comparisons for MMC₁₋₅ are summarized in Table 5.3. Compared with MMC₁, MMCs 2 and 3 have N fewer conducting switches per phase, whereas MMCs 4 and 5 have $(1-4k) \cdot N$ fewer conducting switches per phase, where k ($\leq 25\%$) represents the percentage over N of the number of FB SMs per arm. The phase current of MMCs 4 and 5 is reduced by $(2k)/(1+2k)$, which can decrease the conduction losses for the FB stack.

Table 5.3: Comparison of hardware configuration between FB-MMC and HC-MMCs (per phase)

Converter	MMC ₁	MMC _{2 and 3}	MMC _{4 and 5}
SMs/arm	N (FB)	N (HB)	N (HB), $k \cdot N$ (FB)
SMs/limb	----	$N/2$ (FB)	$N/2$ (FB)
SM capacitors	$2N$	$2.5N$	$(2.5+2k) \cdot N$
Switches	$8N$	$6N$	$(6+8k) \cdot N$
Cond. switches	$4N$	$3N$	$(3+4k) \cdot N$
Conv. voltage	1.0 pu	1.0 pu	$(1.0+2k)$ pu
Phase current	1.0 pu	1.0 pu	$1.0/(1.0+2k)$ pu

The real power reference (P_{ref}) and the ac-voltage magnitude reference (V_{acref}) at the PCC shown in Fig. 5.3 are varied from 0.8 pu to 1.15 pu (to avoid transformer overloading), and 0.9 pu to 1.1 pu (except for MMC₁), respectively. To avoid over-modulation, the maximum V_{acref} for MMC₁ is set to 1.025 pu, for which its modulation index approaches unity considering the voltage across the leakage inductance of transformer.

Based upon the loss calculation method outlined in Section 5.2, the loss simulations of the considered MMCs with the system specifications in Table 5.2 are conducted in the PSCADTM/EMTDCTM simulator. The results of comparative analysis of losses are discussed in the following subsections. Under different operating points, Sections 5.3.2.1-5.3.2.4 show the detailed loss differences between MMC₂ and the remaining four MMCs, when they operate with the ($9f_0$, $27f_0$) switching frequencies. Section 5.3.3 studies the impact of switching frequency variations on the loss differences. In the following subsections, the loss values are shown in percentage based upon the actual real power output (P_{out}) at the considered operating point, which is determined by the control orders P_{ref} and V_{acref} . The loss difference between two MMCs is calculated as follows:

$$Loss_{\text{MMC}_i-\text{MMC}_j} = \frac{P_{\text{LossMMC}_i} - P_{\text{LossMMC}_j}}{P_{\text{out}}} \times 100\% \quad (5.1)$$

5.3.2.1 Loss comparison between MMC₁ and MMC₂

This subsection is to determine the relative merits of HC-MMC in reducing losses in comparison with the conventional FB-MMC. This analysis is vital because FB-MMC is the conventional dc-fault blocking MMC topology, but is commonly considered to have excessive losses due to its SM circuitry. As an alternative topology with dc-fault blocking capability, the losses of HC-MMC are quantified and compared with FB-MMC.

Semiconductor losses of MMC₁ and MMC₂ and their loss difference are shown in Fig. 5.6. It is observed that the losses of MMC₁ vary from 1.45% to 1.85% depending on the operating point, and MMC₂ has losses of 1.40% to 1.70%. Table 5.4 shows a breakdown of the switching and conduction losses for the considered MMCs, where the switching losses include the switching-on and -off losses of IGBT and the reverse-recovery loss of diode; the conduction losses include the conduction losses of both IGBT and diode. As seen from the loss comparison between MMC₁ and MMC₂ in Table 5.4, MMC₁ has up to 0.14% lower switching losses and 0.215% higher conduction losses than MMC₂. The lower switching losses in MMC₁ are because the FB SMs in MMC₁ are controlled to operate as HB SMs, which results in half of the total switches being always on or off, i.e., no switching actions. As such, MMC₁ has $2N$ fewer switches with switching actions per phase than MMC₂ (see Table 5.3). However, MMC₁ has N more switches per phase contributing to the conduction losses. Finally, MMC₁ has higher overall losses than MMC₂ as seen from Fig. 5.6 (c), which shows that the overall losses of MMC₂ are 0.06% to 0.14% lower than that of MMC₁. As seen from Fig. 5.6 (a) and (b), at the rated operating point of $V_{\text{acref}} = 1.0$ pu and $P_{\text{ref}} = 1.0$ pu, the losses of MMC₁ and MMC₂ are approximately 1.52% and 1.46%, respectively, which results in a relative loss difference of $(1.52\% - 1.46\%) / 1.46\% \approx 4.1\%$. The maximum relative loss difference is reached at $V_{\text{acref}} = 0.975$ pu and $P_{\text{ref}} = 0.8$ pu. At this operating point, the losses of MMC₁ and MMC₂ are approximately 1.72% and 1.58%, respectively. As such, the maximum relative loss difference is $(1.72\% - 1.58\%) / 1.58\% \approx 9.0\%$.

It must be pointed out that the seemingly small percentage loss differences (see Fig. 5.6 (c)) can have significant positive consequences particularly in the context of large HVDC transmission systems. For example, a 0.1% reduction in losses of a 2000-MW HVDC converter is equal to 2.0

MW of power. It would be lost as dissipated heat in the converter valve hall, require substantial cooling system upgrades, and result in massive revenue loss over the converter's lifetime.

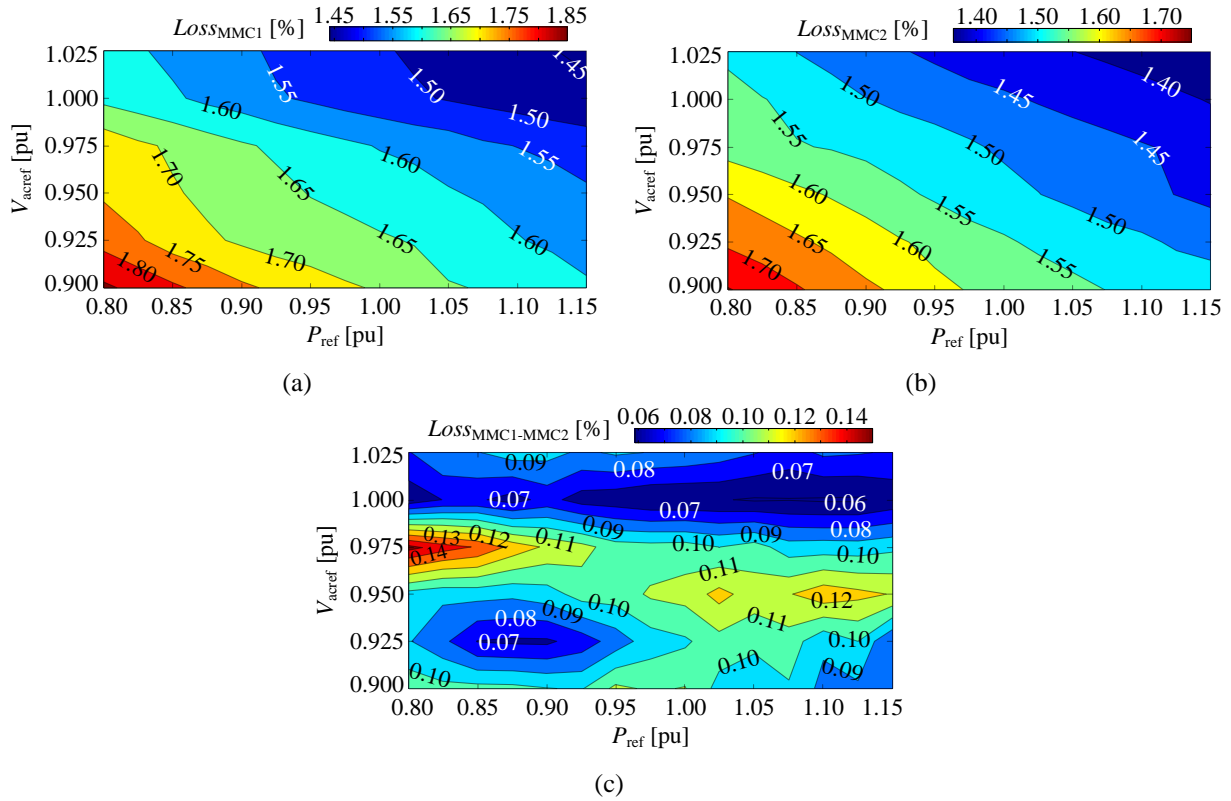


Fig. 5.6: Loss comparison between MMC_1 and MMC_2

(a) losses of MMC_1 ; (b) losses of MMC_2 ; (c) loss difference between MMC_1 and MMC_2 .

5.3.2.2 Loss comparison between MMC_3 and MMC_2

This subsection determines the relative merits of the proposed modified sinusoidal PWM-based capacitor-voltage regulation method with the existing trapezoidal PWM-based method. Chapter 3 showed the merits of the modified sinusoidal PWM method over trapezoidal PWM in extending the converter's linear-regulation range and reducing THD of v_{mA} . It is equally important to compare the HC-MMC losses under these two methods to assess the true benefits of the modified sinusoidal method in reducing the filtering burden of the FB stack in the phase limb.

Fig. 5.7 shows loss comparisons between MMCs 2 and 3 (HC-MMC with modified sinusoidal PWM and trapezoidal PWM methods). Fig. 5.7 (a) shows that the THD of v_{mA} in MMC₃ is 1.0% to 6.0% higher than that in MMC₂, whereas Fig. 5.7 (b) shows that the MMC₃ losses are 0.04% to 0.14% higher than that of MMC₂.

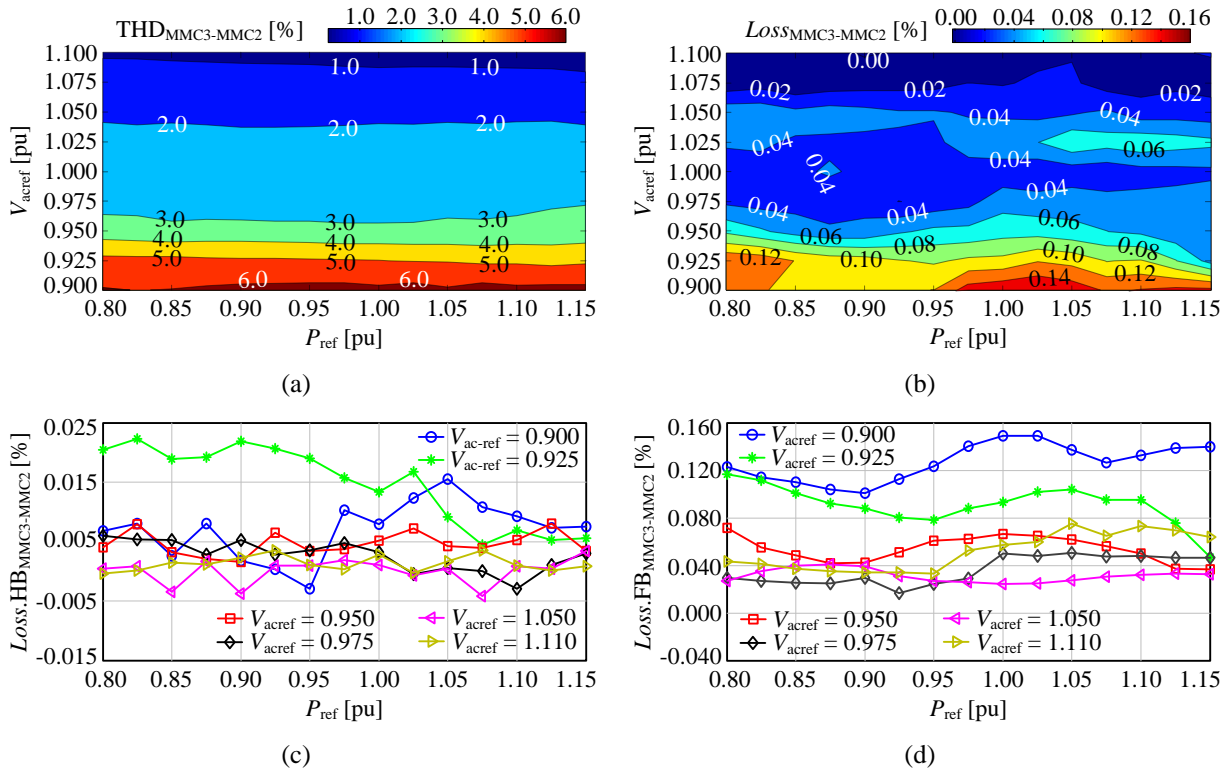


Fig. 5.7: Loss comparison between MMC₃ and MMC₂

(a) THD difference of v_{mA} ; (b) loss difference; (c) loss difference between the main power stages; (d) loss difference between the FB stacks.

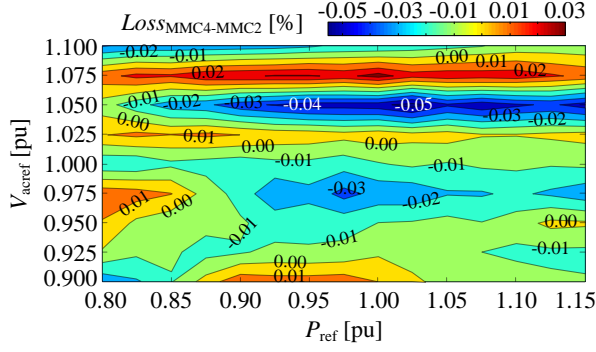
As seen from the loss comparison of the main power stages between MMC₃ and MMC₂ in Table 5.4, MMC₂ and MMC₃ have close switching and conduction losses, which results in close total losses of the main power stage in both converters as observed in Fig. 5.7 (c). However, as seen from the loss comparison of the FB stack in the phase limb between MMC₃ and MMC₂ in Table 5.4, MMC₃ has close conduction losses but exhibits much higher (up to 0.14%) switching losses than MMC₂. As such, the FB stack under the trapezoidal PWM has up to 0.14% more total

losses than that under the modified sinusoidal PWM as shown in Fig. 5.7 (d). Therefore, the higher THD of the main power stage voltage increases the switching losses of the FB stack due to a heavier filtering burden. As such, there are clear advantages for MMC₂ in not only an extended linear-regulation range but also improved efficiency.

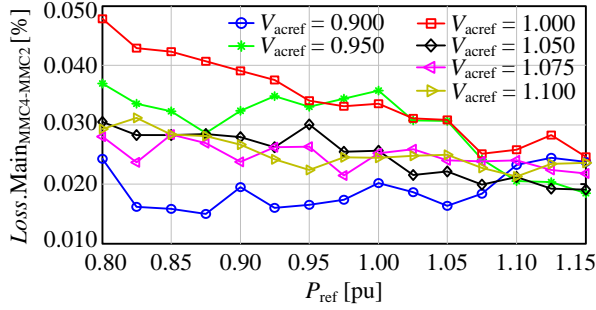
5.3.2.3 Loss comparison between MMC_{4,5} and MMC₂

This subsection determines the impact of additional FB SMs in the main power stage on the converter losses. This analysis will clarify how the addition of FB SMs in the main power, which are used to further extend its linear and low-THD range, may impact the converter losses.

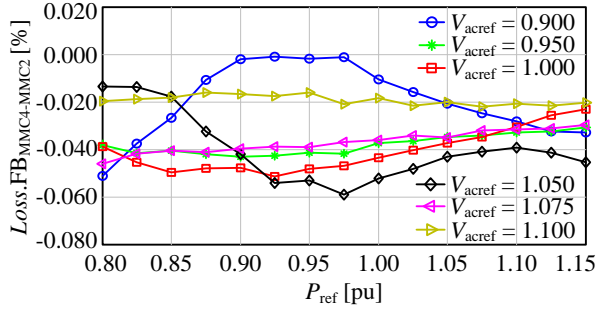
Fig. 5.8 and Fig. 5.9 show loss comparisons between MMC₂ and HC-MMCs with 5% (MMC₄) and 10% (MMC₅) FB SMs in the main power stage. Although the overall loss differences are negligible (within -0.03% to 0.03% for most cases), the losses of MMCs 4 and 5 are up to 0.05% lower relative to the losses of MMC₂ at certain operating points. However, from Fig. 5.8 (b) and Fig. 5.9 (b), it is noted that MMCs 4 and 5 show about 0.03% and 0.05% higher losses in their main power stage than MMC₂, respectively, since they have more semiconductors and slightly higher conduction losses are exhibited as seen from the loss comparisons of the main power stages between MMCs 4 and 5 and MMC₂ listed in Table 5.4. The slight reduction in the total losses for MMCs 4 and 5 is achieved by up to 0.06% and 0.1% lower losses of their FB stacks, respectively, as shown in Fig. 5.8 (c) and Fig. 5.9 (c). The mixed-SM HC-MMCs benefit from reduced phase currents due to their extended linear modulation range and larger converter-side transformer's nominal voltages, which lowers the conduction losses of the FB stack as seen from the loss comparisons of the FB stack in the phase limb between MMCs 4 and 5 and MMC₂ listed in Table 5.4.



(a)

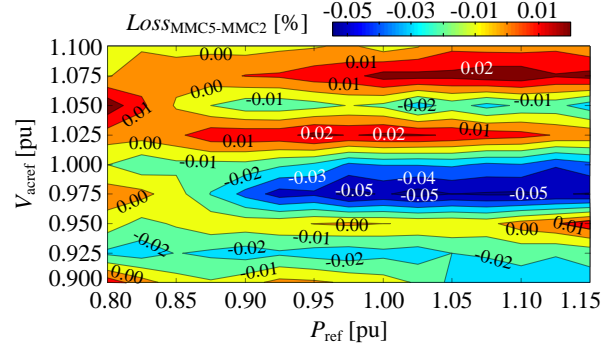


(b)

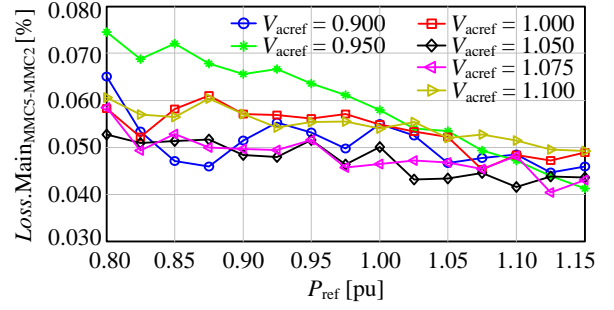


(c)

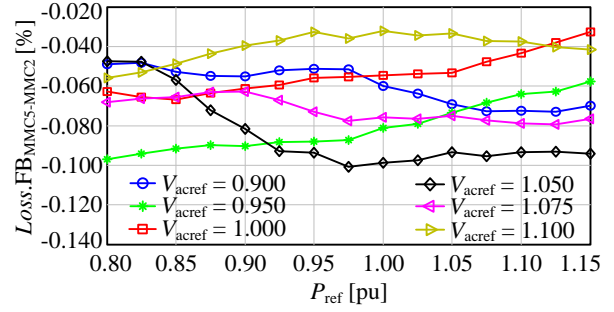
Fig. 5.8: Loss comparison between MMC₄ and MMC₂ (a) loss difference; (b) loss difference in the main power stages; (c) loss difference of the FB stacks.



(a)



(b)



(c)

Fig. 5.9: Loss comparison between MMC₅ and MMC₂ (a) loss difference; (b) loss difference in the main power stages; (c) loss difference of the FB stacks.

Table 5.4: Switching and conduction loss differences between considered MMCs

Loss difference		$Loss_{MMC1-MMC2}$ (%)	$Loss_{MMC3-MMC2}$ (%)	$Loss_{MMC4-MMC2}$ (%)	$Loss_{MMC5-MMC2}$ (%)
Main power stage ^①	For switching loss	[-0.140, -0.060]	[-0.010, 0.020]	[-0.020, 0.010]	[-0.010, 0.015]
	For conduction loss	[0.175, 0.215]	[-0.005, 0.006]	[0.022, 0.036]	[0.045, 0.075]
FB stack in the phase limb	For switching loss	-----	[0.020, 0.140]	[-0.030, 0.030]	[0.040, 0.070]
	For conduction loss	-----	[-0.0005, 0.0015]	[-0.036, -0.031]	[-0.068, -0.056]

Note ①: The entire converter is used for the loss comparison between MMC₁ and MMC₂, since MMC₁ (FB-MMC) only has one power stage.

5.3.2.4 Comprehensive loss comparisons among MMCs 1 to 5

The loss differences between all considered MMCs are shown in Table 5.5. Since the loss comparisons in the symmetrical cells shown in Table 5.5 are conducted between the same groups of MMCs, only the comparisons in the upper triangular cells are given. As seen from Table 5.5, compared with MMC₁ (conventional FB-MMC) or MMC₃ (HC-MMC operating with the trapezoidal PWM), MMCs 2, 4 and 5 (HC-MMC operating with the modified sinusoidal PWM methods) have lower losses. However, compared with MMC₁, MMC₃ has higher losses at certain operating points, even though there are fewer switches in MMC₃ (see Table 5.3). Therefore, apart from the fewer number of switches, proper control methods for HC-MMC are also of importance to reduce losses.

Table 5.5: Loss differences between MMCs 1 to 5

Loss difference (%)	MMC ₁	MMC ₂	MMC ₃	MMC ₄	MMC ₅
MMC ₁	-----	[0.06, 0.15]	[-0.06, 0.12]	[0.07, 0.13]	[0.07, 0.14]
MMC ₂	-----	-----	[-0.16, 0.00]	[-0.03, 0.05]	[-0.02, 0.05]
MMC ₃	-----	-----	-----	[0.00, 0.16]	[-0.02, 0.16]
MMC ₄	-----	-----	-----	-----	[-0.04, 0.02]
MMC ₅	-----	-----	-----	-----	-----

Note: Each value in this table represents the loss difference between MMCs shown in the corresponding row and column. For example, the value shown in the shadowed cell equals to $(Loss_{MMC1} - Loss_{MMC2})$.

5.3.3 Impact of switching frequency variations on loss differences

Table 5.6 shows the loss differences between MMC₂ and the remaining four MMCs for different switching frequencies. The switching frequencies considered are $(9f_0, 21f_0)$, $(9f_0, 27f_0)$, $(11f_0, 27f_0)$ and $(11f_0, 33f_0)$, wherein the former frequencies are for the main power stages in MMC₂₋₅ and the latter ones are for MMC₁ and the FB stacks in MMC₂₋₅. As seen the overall loss differences vary marginally with switching frequencies. Compared with MMC₂, MMCs 1 and 3 have higher overall losses, whereas MMCs 4 and 5 have lower losses at certain operating points.

In other words, compared with FB-MMC and HC-MMC using the trapezoidal PWM method [34], HC-MMCs operating with the proposed modified sinusoidal PWM method and mixed-SM approach shown in Sections 3.2.2 and 3.2.3 possess significant benefits of lower semiconductor losses.

Table 5.6: Loss differences between MMCs under different carrier frequencies

Carrier frequencies	LOSS _{MMC1-MMC2} (%)	LOSS _{MMC3-MMC2} (%)	LOSS _{MMC4-MMC2} (%)	LOSS _{MMC5-MMC2} (%)
$(9f_o, 21f_o)$	[0.06, 0.16]	[0.00, 0.14]	[-0.02, 0.01]	[-0.03, 0.03]
$(9f_o, 27f_o)$	[0.06, 0.15]	[0.00, 0.14]	[-0.05, 0.03]	[-0.05, 0.02]
$(11f_o, 27f_o)$	[0.06, 0.12]	[0.00, 0.18]	[-0.04, 0.01]	[-0.04, 0.01]
$(11f_o, 33f_o)$	[0.02, 0.22]	[0.00, 0.12]	[-0.06, 0.03]	[-0.06, 0.02]

5.4 Summary and key contributions

Loss comparisons for HC-MMCs with different FB-SM capacitor-voltage regulation methods and under different switching frequencies were presented. The analysis of loss comparisons showed several significant observations: Firstly, the HC-MMC with the modified sinusoidal PWM-based voltage regulator has markedly lower losses than FB-MMC. This confirms that HC-MMC is a superior alternative to FB-MMC when converters with dc-fault blocking capabilities are concerned. Secondly, the HC-MMC with the modified sinusoidal PWM was shown to have lower losses than that with the trapezoidal PWM method due to the reduced harmonic filtering burden of the FB stack in the phase limb. This indicates that the modified sinusoidal PWM method not only extends the linear-regulation range of an HC-MMC but also does so while lowering the semiconductor losses. Thirdly, it showed that the mixed-SM HC-MMCs with 5% and 10% addition of FB SMs in the main power stage have slightly lower losses than the original HC-MMC at certain operating points. This further supports the recommendation of adding 6%~12% FB SMs to the main power stage from the perspective of SM capacitor size. This implies that the mixed-

SM HC-MMC topology offers an extended linear-regulation range without increasing losses and potentially even reducing them due to reduced phase currents. Variations of losses as a function of switching frequencies were also investigated. It was shown that switching frequency variations do not change the overall trend of loss differences and as such the conclusions drawn about the relative merits of considered MMCs remain valid.

Chapter 6

DC-Fault Analysis and SM Capacitance Considerations under DC Faults

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HVDC transmission systems are particularly designed for long-distance power delivery, and dc faults are likely to occur due to several factors, such as complicated environmental events or equipment failure. To avoid fatal damages to HVDC transmission systems, the dc-fault behavior of the converters used in HVDC transmission is necessary to be studied [49]-[53]. Presently, most studies focus on the conventional HB-MMC [50]-[53]. However, MMCs with topological dc-fault blocking capability are becoming increasingly appealing. Most of these topologies employ FB SMs to block dc faults, by inserting the FB-SM capacitors into the fault path to decay the fault current after blocking the converter. Regardless of the fault current polarity the inserted FB-SM capacitors are charged, which may result in adverse SM capacitor overvoltage.

This chapter investigates the dc-fault behavior of both the original and mixed-SM HC-MMCs based upon their equivalent models under a pole-to-pole fault. The equivalent models under a pole-to-pole fault are validated by EMT simulations. In addition, considerations for SM capacitance selection are investigated under a pole-to-pole fault to avoid overvoltage damages to SM capacitors.

6.1 Modelling of HC-MMCs under a pole-to-pole fault

The schematic diagram of the original or mixed-SM HC-MMCs with a pole-to-pole dc fault is shown in Fig. 6.1, where the detailed topologies of the original and mixed-SM HC-MMCs are shown in Fig. 4.1 (a); n_{tr} ($= V_{tr-con}/V_{tr-sys}$) is the transformer's turns ratio seen from the converter side to the system side; $Z_s = R_s + j\omega_b L_s$ and $Z_{s-con} = R_{s-con} + j\omega_b L_{s-con}$ are the impedances at the system side and that reflected to the converter side, respectively; v_{sABC} and $v_{sABC-con}$ are the three-phase voltage source at the grid side and that reflected to the converter side, respectively; and resistor R_G is a large resistance connected to the neutral point of the converter-side windings of the interfacing transformer.

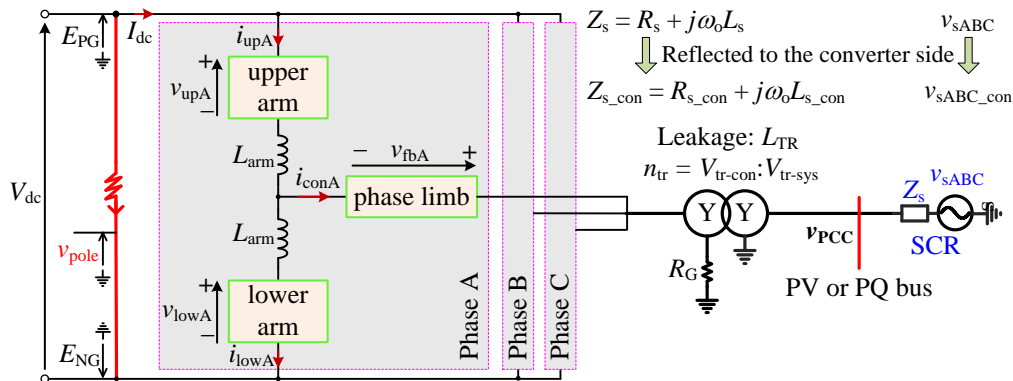


Fig. 6.1: Brief schematic of the original or mixed-SM HC-MMC with a pole-to-pole fault

In normal operation, the potential of the neutral point of transformer's converter-side windings is approximately zero, because three-phase currents are well balanced. If a pole-to-pole fault

occurs, three-phase currents quickly decay to zeros due to the existence of FB SMs in the phase limb in both the original and mixed-SM HC-MMCs, and the potential of the neutral point of transformer's converter-side winding will remain approximately zero. However, the faulted dc terminals are floating. As such, the potential of faulted dc terminals, v_{pole} (see Fig. 6.1), is of interest.

The three-phase equivalent circuit of the original or mixed-SM HC-MMC with a pole-to-pole fault at the converter's terminal is shown in Fig. 6.2, where the grid side is reflected to the converter side, and N_h and N_f are the numbers of HB SMs per arm and FB SMs per phase limb, respectively. In idealized operation, the voltages $v_{\text{up}j}$, $v_{\text{low}j}$ and $v_{\text{fb}j}$ ($j = A, B$ and C) can be expressed by their corresponding reference signals. If the converter's firing pulses are blocked in response to a pole-to-pole fault, all FB SMs are inserted and will be charged regardless of current flow direction. Since dc-side terminals are shorted with a small impedance, the arm currents ($i_{\text{up}j}$ and $i_{\text{low}j}$, where $j = A, B$ and C) typically become negative quickly. As such, all HB SMs in the main power stage are bypassed after the system is blocked. Therefore, the expressions in (6.1) are obtained.

$$\begin{aligned}
 v_{\text{up}j} &= \frac{V_{\text{dc}}}{2} \cdot \begin{cases} (1 - v_{\text{mj-ref}}), & \text{before blocking} \\ \text{sign}(i_{\text{up}j}) \cdot 2k_{\text{fm}}, & \text{after blocking} \end{cases} \\
 v_{\text{low}j} &= \frac{V_{\text{dc}}}{2} \cdot \begin{cases} (1 + v_{\text{mj-ref}}), & \text{before blocking} \\ \text{sign}(i_{\text{low}j}) \cdot 2k_{\text{fm}}, & \text{after blocking} \end{cases} \\
 v_{\text{fb}j} &= \frac{V_{\text{dc}}}{2} \cdot \begin{cases} v_{\text{fb}j\text{-ref}}, & \text{before blocking} \\ -\text{sign}(i_{\text{con}j}), & \text{after blocking} \end{cases}
 \end{aligned} \tag{6.1}$$

where $v_{\text{mj-ref}}$ and $v_{\text{fb}j\text{-ref}}$ are the per-unit references for the main power stage and FB stack in the phase limb, respectively, and $k_{\text{fm}} = N_{\text{fm}}/N_h$ and N_{fm} is the number of FB SMs per arm in the main power stage. For the original HC-MMC, use $k_{\text{fm}} = 0$ in (6.1).

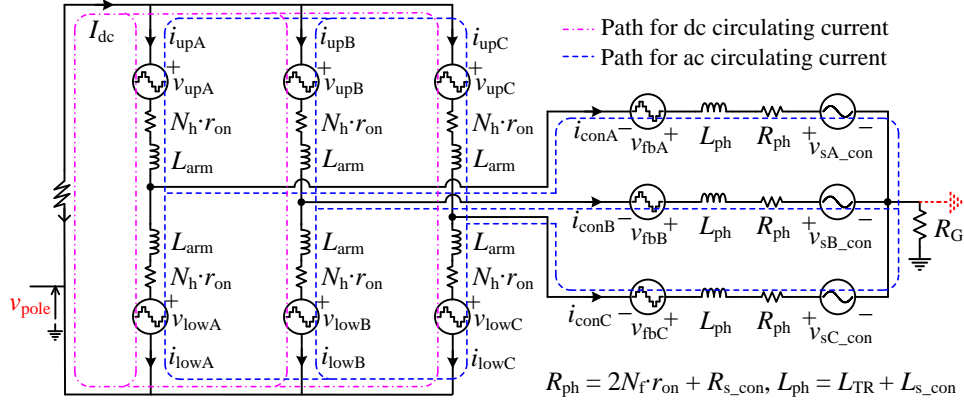


Fig. 6.2: Three-phase equivalent circuit of the original or mixed-SM HC-MMC with a pole-to-pole fault

By applying KVL and Kirchhoff's current law (KCL) to the circuit in Fig. 6.2, the equations shown in (6.2) are obtained. After simplifications, the expression of v_{pole} is shown in (6.3).

$$\begin{cases}
 v_{\text{up}j} + v_{\text{low}j} + L_{\text{arm}} \left(\frac{di_{\text{up}j}}{dt} + \frac{di_{\text{low}j}}{dt} \right) + N_h r_{\text{on}} \cdot (i_{\text{up}j} + i_{\text{low}j}) = 0 \\
 v_{\text{pole}} = v_{\text{up}j} + L_{\text{arm}} \frac{di_{\text{up}j}}{dt} + N_h r_{\text{on}} i_{\text{up}j} + L_{\text{ph}} \left(\frac{di_{\text{up}j}}{dt} - \frac{di_{\text{low}j}}{dt} \right) + R_{\text{ph}} (i_{\text{up}j} - i_{\text{low}j}) - v_{\text{fb}j} + v_{s_{j\text{con}}} \\
 i_{\text{up}A} - i_{\text{low}A} + i_{\text{up}B} - i_{\text{low}B} + i_{\text{up}C} + i_{\text{low}C} = 0 \\
 \text{where } j = A, B \text{ and } C
 \end{cases} \quad (6.2)$$

$$v_{\text{pole}} = \frac{1}{6} (v_{\text{up}A} - v_{\text{low}A} + v_{\text{up}B} - v_{\text{low}B} + v_{\text{up}C} - v_{\text{low}C}) - \frac{1}{3} (v_{\text{fb}A} + v_{\text{fb}B} + v_{\text{fb}C}) \quad (6.3)$$

In practice, if a dc fault occurs in a converter system, the system is blocked due to either the dc-fault detection or overcurrent protection. Typically, a pole-to-pole fault at the converter terminals is considered as the worst-case scenario, since the line inductance does not contribute to limit the fault current. Under this worst-case condition, all the arm currents become negative referred to the defined current direction shown in Fig. 6.2 regardless of inverter- or rectifier-mode operation, and their magnitudes rise sharply to large values. Typically, the converter system is blocked primarily due to its overcurrent protection. The delay to trigger the overcurrent protection of the arm current is generally small (≤ 1.0 ms) [52] under a pole-to-pole fault at the converter's

terminal. Within such a short delay, i.e., after the dc fault occurs and before it is detected, the control system operates as normal, resulting in approximately balanced three-phase references for the main power stage ($v_{mj\text{-ref}}$) and the FB stacks in the phase limbs ($v_{fbj\text{-ref}}$), where $j = A, B$ and C . In other words, $v_{mA\text{-ref}} + v_{mB\text{-ref}} + v_{mC\text{-ref}} = 0$ and $v_{fbA\text{-ref}} + v_{fbB\text{-ref}} + v_{fbC\text{-ref}} = 0$. Substituting (6.1) into (6.3), the expression of v_{pole} before blocking is obtained as follows:

$$v_{\text{pole}} = \frac{V_{\text{dc}}}{12} \left(\begin{aligned} & (1 - v_{mA\text{-ref}}) - (1 + v_{mA\text{-ref}}) + (1 - v_{mB\text{-ref}}) \\ & - (1 + v_{mB\text{-ref}}) + (1 - v_{mC\text{-ref}}) - (1 + v_{mC\text{-ref}}) \end{aligned} \right) \quad (\text{before blocking}) \quad (6.4)$$

$$- \frac{V_{\text{dc}}}{6} (v_{fbA\text{-ref}} + v_{fbB\text{-ref}} + v_{fbC\text{-ref}}) = 0$$

After all firing pulses are blocked, all HB SMs in the main power stage are bypassed due to negative arm currents, and all FB SMs in the phase limbs and those in the main power stage of mixed-SM HC-MMC are inserted and will be charged regardless of the current flow direction. Since both the upper- and lower-arm currents are negative, $(v_{\text{up}j} - v_{\text{low}j}) = 0$ for both the original and mixed-SM HC-MMCs, where $j = A, B$ and C . Therefore, the expression of v_{pole} after blocking is obtained as follows:

$$v_{\text{pole}} = \frac{V_{\text{dc}}}{6} (\text{sign}(i_{\text{conA}}) + \text{sign}(i_{\text{conB}}) + \text{sign}(i_{\text{conC}})) = \pm \frac{V_{\text{dc}}}{6} \quad (\text{after blocking}) \quad (6.5)$$

where the voltage rises in FB-SM capacitors in the phase limb after the converter is blocked are ignored. Since the three-phase currents are balanced in normal operations before a dc fault occurs, the three-phase currents upon blocking must include two of the same polarities and one of opposite polarity. As such, the value of v_{pole} after blocking can be $V_{\text{dc}}/6$ or $-V_{\text{dc}}/6$.

As seen from Fig. 6.2, after a pole-to-pole fault occurs, the dc-side fault current circulates between the shorted path and all the arms, and the ac-side currents circulate among all arms, phase limbs and ac-side circuit. Due to the similarity of three phases, a single-phase circuit is used to

analyze the dc-fault behavior for both the original and mixed-SM HC-MMCs during dc faults. Note that a constant voltage source ($V_{dc}/6$ or $-V_{dc}/6$) is used to present the potential of v_{pole} in the following analysis of equivalent models for the ac circulating current in both the original and mixed-SM HC-MMCs.

6.1.1 Equivalent circuit models for the original HC-MMC

After a pole-to-pole fault occurs at converter's dc-side terminals, firing pulses are typically blocked within a short delay (≤ 1.0 ms), which is caused by either a dc fault detection or overcurrent protection mechanism. Denote the dc fault instant as t_{flt} and the blocking delay as t_{blk} . Within a short interval of $[t_{flt}, t_{flt} + t_{blk}]$, the control system operates as normal and ac circulating currents have negligible change, because the ac circulating circuit and its control are essentially unchanged. However, the dc circulating circuit is changed at the dc terminals compared with that in normal operation (see Fig. 6.2). Therefore, after a dc fault occurs and before its detection, only the equivalent circuit for dc circulating current is considered. Since the reactions of control system are neglected within a short interval after a dc fault occurs, the total number of inserted SMs in each phase is approximately N_h at any instant of time before blocking the converter. Therefore, the equivalent model for dc circulating current is an RLC circuit as shown in Fig. 6.3 (a) with an equivalent capacitance (C_{eq}) of C_{hb}/N_h , an equivalent resistance (R_{eq}) of $2N_h \cdot r_{on}$ and an equivalent inductance (L_{eq}) of $2L_{arm}$, where C_{hb} is the HB-SM capacitance in the main power stage, L_{arm} is the arm inductance per arm, and r_{on} denotes the ON resistance of each semiconductor (considered equal for switches and diodes).

Typically, the dc circulating current ($i_{dc-cir1}$) becomes negative and its magnitude increases promptly due to HB-SM capacitors discharging through the faulted path. Therefore, after all firing pulses are blocked, i.e., $t > t_{flt} + t_{blk}$, all HB SMs in the main power stage are bypassed due to the

negative dc circulating current, and all FB SMs in the phase limb are inserted and charged regardless of phase current polarity. As such, the equivalent model for the dc circulating current changes to an RL circuit with $R_{eq} = 2N_h \cdot r_{on}$ and $L_{eq} = 2L_{arm}$ as shown in Fig. 6.3 (b). The equivalent model for the ac circulating current is an RLC circuit as shown in Fig. 6.3 (c), where C_{fb} is the SM capacitance for FB SMs; R_{s_con} and L_{s_con} are components of the ac-source impedance reflected to the converter side (see Fig. 6.1); V_{s_conFlt} is approximately constant within a short interval and its value is determined by the ac-source voltage reflected to the converter side upon blocking the converter, i.e., the value of v_{s_con} at $t = t_{flt} + t_{blk}$; and the expression of v_{pole} after blocking is shown in (6.5). Note that the polarity of the inserted FB-SM capacitor voltage (i.e., v_{ceq3} shown in Fig. 6.3 (c)) after blocking is related to the polarity of $i_{ac-cir1}$.

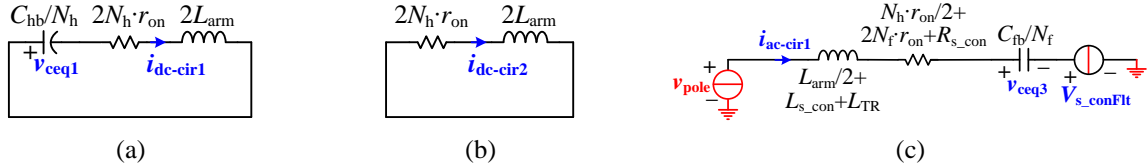


Fig. 6.3: Equivalent circuits of the original HC-MMC under a pole-to-pole fault

(a) model for the dc circulating current before blocking; (b) model for the dc circulating current after blocking; (c) model for the ac circulating current after blocking.

As seen from Fig. 6.3, the equivalent circuits are either RL or RLC circuits. Since the equivalent ON resistance is small, the RLC circuits shown in Fig. 6.3 are underdamped. General RL and RLC circuits, which are used to find general solutions of capacitor voltage and inductor current with underdamped case for RLC circuit, are shown in Fig. 6.4, where V_s is a constant voltage source. The solutions of capacitor voltage and branch current in RLC circuit shown in Fig. 6.4 (a) are as follows:

$$\begin{aligned} v_{ceq}(t) &= \left[K_1 \cos(\omega_d(t-t_0)) + K_2 \sin(\omega_d(t-t_0)) \right] e^{-\alpha(t-t_0)} - V_s, \quad \text{for } t \geq t_0 \\ i_{Leq}(t) &= \left[A_1 \cos(\omega_d(t-t_0)) + A_2 \sin(\omega_d(t-t_0)) \right] e^{-\alpha(t-t_0)}, \quad \text{for } t \geq t_0 \end{aligned} \quad (6.6)$$

where

$$\begin{aligned} \alpha &= R_{\text{eq}} / (2L_{\text{eq}}), \quad \omega_r = 1 / \sqrt{L_{\text{eq}} C_{\text{eq}}}, \quad \omega_d = \sqrt{\omega_r^2 - \alpha^2} \\ K_1 &= V_{\text{ceq0}} + V_s, \quad K_2 = (V'_{\text{ceq0}} + K_1 \alpha) / \omega_d = (I_{\text{Leq0}} / C_{\text{eq}} + K_1 \alpha) / \omega_d \\ A_1 &= I_{\text{Leq0}}, \quad A_2 = (I'_{\text{Leq0}} + A_1 \alpha) / \omega_d = [-(V_{\text{ceq0}} + R_{\text{eq}} I_{\text{Leq0}} + V_s) / L_{\text{eq}} + A_1 \alpha] / \omega_d \end{aligned} \quad (6.7)$$

and V_{ceq0} and I_{Leq0} are the initial values at $t = t_0$, respectively. In an underdamped circuit, $\alpha < \omega_r$, i.e., $R_{\text{eq}} < 2\sqrt{L_{\text{eq}}/C_{\text{eq}}}$. During dc faults, the fault-current clearing time and SM capacitor voltage variations are of interest. The dc-fault clearing time, t_{clr} , is calculated by solving $i_{\text{Leq}}(t_0 + t_{\text{clr}}) = 0$:

$$t_{\text{clr}} = \tan^{-1}(-A_1/A_2) / \omega_d \quad (6.8)$$

Substituting $t = t_0 + t_{\text{clr}}$ into (6.6), the equivalent capacitor voltage v_{ceq} can be evaluated.

The inductor current of the generic RL circuit shown in Fig. 6.4 (b) is as follows:

$$i_{\text{Leq}}(t) = (I_{\text{Leq0}} + V_s / R_{\text{eq}}) e^{-(t-t_0)/\tau} - V_s / R_{\text{eq}}, \quad \text{for } t \geq t_0 \quad (6.9)$$

where $\tau = L_{\text{eq}} / R_{\text{eq}}$. The current i_{Leq} typically takes approximately 5τ to decay to zero.



Fig. 6.4: General circuit configurations for RLC and RL circuits

(a) RLC circuit; (b) RL circuit.

Based upon the above analysis of the response for generic RL and RLC circuits, the solutions of the equivalent circuits shown in Fig. 6.3 can be readily obtained. The parameters are summarized in Table 6.1, where $v_{\text{csm-final}}$ is the final SM capacitor voltage under a dc fault, and the expression of v_{pole} is shown in (6.5).

Table 6.1: Parameters for the equivalent circuit models (in Fig. 6.3) of the original HC-MMC

Parameters	DC equivalent circuit models		AC equivalent circuit models
	Before blocking ($t_{\text{flt}} < t < t_{\text{flt}} + t_{\text{blk}}$)	After blocking ($t_{\text{flt}} + t_{\text{blk}} < t < t_{\text{flt}} + t_{\text{blk}} + t_{\text{clr}}$)	After blocking ($t_{\text{flt}} + t_{\text{blk}} < t < t_{\text{flt}} + t_{\text{blk}} + t_{\text{clr}}$)
Circuit type	RLC	RL	RLC
Solution variables	v_{ceq1} and $i_{\text{dc-cir1}}$	v_{ceq2} and $i_{\text{dc-cir2}}$	v_{ceq3} and $i_{\text{ac-cir1}}$
R_{eq}	$2N_{\text{h}} \cdot r_{\text{on}}$	$2N_{\text{h}} \cdot r_{\text{on}}$	$N_{\text{h}} \cdot r_{\text{on}} / 2 + 2N_{\text{f}} \cdot r_{\text{on}} + R_{\text{s_con}}$
L_{eq}	$2L_{\text{arm}}$	$2L_{\text{arm}}$	$L_{\text{arm}} / 2 + L_{\text{s_con}} + L_{\text{TR}}$
C_{eq}	$C_{\text{hb}} / N_{\text{h}}$	N/A	$C_{\text{fb}} / N_{\text{f}}$
t_0	t_{flt}	$t_{\text{flt}} + t_{\text{blk}}$	$t_{\text{flt}} + t_{\text{blk}}$
I_{Leq0}	$(i_{\text{up}} + i_{\text{low}}) / 2 \mid t = t_{\text{flt}}$	$i_{\text{dc-cir1}} \mid t = t_{\text{flt}} + t_{\text{blk}}$	$i_{\text{con}} \mid t = t_{\text{flt}} + t_{\text{blk}}$
V_{ceq0}	V_{dc}	N/A	$\text{sign}(I_{\text{Leq0}}) \cdot V_{\text{dc}} / 2$
V_{s}	0	0	$(v_{\text{s_con}} \mid t = t_{\text{flt}} + t_{\text{blk}}) - v_{\text{pole}}$
t_{clr}	N/A	$5L_{\text{eq}} / R_{\text{eq}}$	$\tan^{-1}(-A_1 / A_2) / \omega_{\text{t}}$
$v_{\text{csm-final}}$	$v_{\text{ceq}} / N_{\text{h}} \mid t = t_{\text{flt}} + t_{\text{blk}}$	N/A	$\text{sign}(I_{\text{Leq0}}) \cdot v_{\text{ceq}} / N_{\text{f}} \mid t = t_{\text{flt}} + t_{\text{blk}} + t_{\text{clr}}$

With the system parameters of $V_{\text{dc}} = 500.0$ kV, $P_{\text{dc}} = 500.0$ MW, $N_{\text{h}} = 100$, $N_{\text{f}} = 50$, $L_{\text{arm}} = 0.05$ H, $r_{\text{on}} = 5$ m Ω , $\text{SCR} = 3.0 \angle 80^\circ$, $V_{\text{tr-con}} / V_{\text{tr-sys}} = 290$ kV / 230.0 kV, and $L_{\text{TR}} = 0.045$ H, a pole-to-pole fault is applied to investigate the performance of the equivalent models of the original HC-MMC. Fig. 6.5 shows the response of the dc circulating current and HB-SM capacitor voltage with respect to different blocking delays in the original HC-MMC after a pole-to-pole fault occurs and before the converter is blocked. It is seen that the initial dc circulating current upon the dc fault is equal to $I_{\text{dc}}/3$ and the current decreases quickly to a negative value with a large magnitude within a short time. The magnitude of the dc circulating current becomes larger if the blocking delay (t_{blk}) is longer. After the HB-SM capacitor voltage decreases to zero, the equivalent model for the dc circulating current changes to the same RL circuit shown in Fig. 6.3 (b), even though firing pulses are not blocked. As seen from Fig. 6.5 (a) and assuming that the blocking delay is 1.0 ms, the HB-SM capacitance has slight influence on the value of the dc circulating current upon blocking, and the HB-SM capacitor voltage is significantly decreased with C_{hb} decreasing. In order to quickly

recover to normal operation after the dc fault is cleared, the final HB-SM capacitor voltage is preferred be closer to its nominal value. The considerations for HB-SM capacitor sizing under a pole-to-pole fault are discussed in Section 6.2.1 with $R_{eq} = 0 \Omega$ to simplify the analysis, since the equivalent resistance has negligible influence on the dc circulating current and HB-SM capacitor voltage as seen from Fig. 6.5 (b).

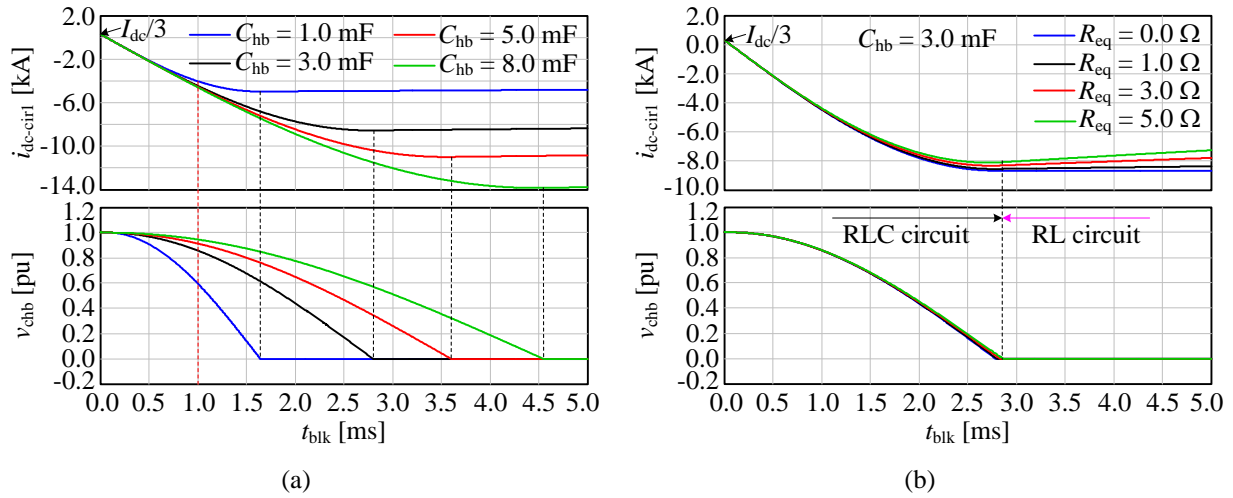


Fig. 6.5: Responses of the dc circulating current and HB-SM capacitor voltage with respect to different blocking delays in the original HC-MMC after a pole-to-pole fault occurs and before the converter is blocked

(a) responses with various C_{hb} and $R_{eq} = 2N_h \cdot r_{on}$; (b) responses with $C_{hb} = 3.0$ mF and various R_{eq} .

With the same system parameters used above, a pole-to-pole fault is applied at the peak of phase-A current to investigate the performance of the equivalent models after blocking. Since the equivalent model for dc circulating current is an RL circuit, it takes approximately 0.5 s, which is equal to $5\tau = 5L_{eq}/R_{eq} = 10L_{arm}/(2N_h \cdot r_{on})$, to decay the dc current to zero, no matter how large the dc current is upon blocking. Through theoretical calculation, the initial branch current is equal to $(i_{conA} | t = t_{flt} + t_{blk}) = 1.4$ kA, and $V_{s_conFlt} = (v_{sA_con} | t = t_{flt} + t_{blk}) = 224.0$ kV and $v_{pole} = -V_{dc}/6$ for the equivalent model in Fig. 6.3 (c). With various FB-SM capacitance (C_{fb}) and equivalent resistance (R_{eq}) values, the responses of ac phase current and FB-SM capacitor voltage in phase-A limb in the original HC-MMC after blocking are shown in Fig. 6.6. It is observed from Fig. 6.6

(a) that the ac phase current is cleared within a short time (~ 0.5 ms) due to the existence of FB SMs in the circulating path, and the FB-SM capacitance has slight influence on the clearing time. It implies that the usage of FB SMs in the phase limb can quickly isolate the faulted dc side from ac side, resulting in topological dc-fault blocking capability. However, the FB-SM capacitor voltage rise is significantly reduced with large SM capacitance. Therefore, to achieve safe operation during dc faults, considerations for FB-SM capacitance selection in the phase limb under a pole-to-pole fault are discussed in Section 6.2.3. As seen from Fig. 6.6 (b), the equivalent resistance varying within a reasonable range ($0.0 \Omega \sim 10.0 \Omega$) has negligible influence on the ac-current clearing time and the FB-SM capacitor voltage rise. As such, the equivalent resistance R_{eq} shown in Fig. 6.3 (c) is neglected to simplify the analysis in Section 6.2.3.

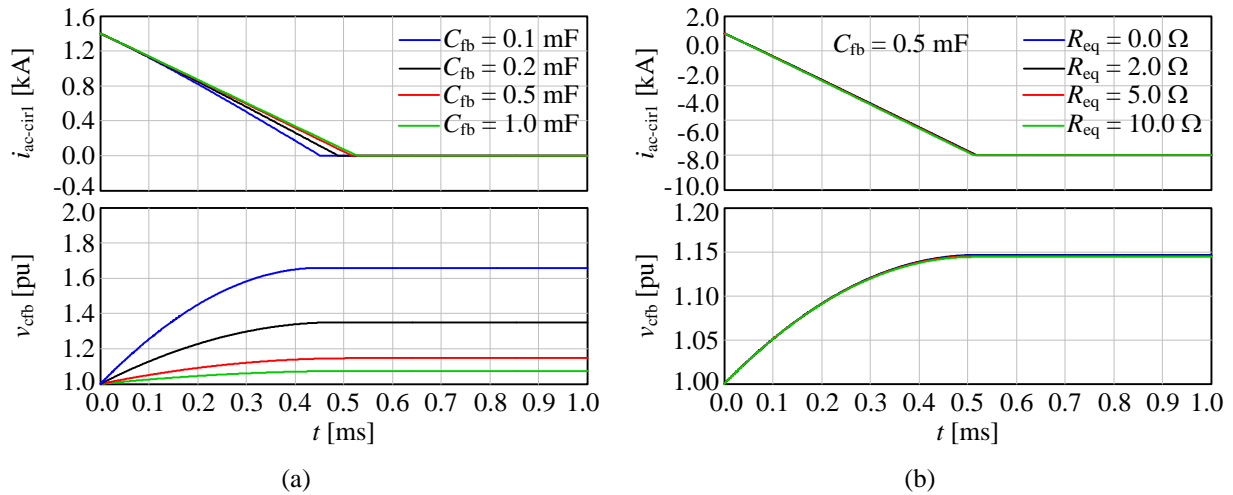


Fig. 6.6: Responses of ac phase current and FB-SM capacitor voltage in original HC-MMC after blocking (a) responses with various C_{fb} and $R_{eq} = N_h \cdot r_{on}/2 + 2N_f r_{on} + R_{s-con}$; (b) response with $C_{fb} = 0.5$ mF and various R_{eq} .

6.1.2 Equivalent circuit models for the mixed-SM HC-MMC

Compared with the original HC-MMC, the main power stage of the mixed-SM HC-MMC has not only HB but also FB SMs. Since the number of FB SMs in the main power stage is generally much smaller than that of HB SMs, only HB SMs are assumed to be discharged after a dc faults

occurs and before the converter is blocked for simplicity. As such, the equivalent model of the dc circulating current for the mixed-SM HC-MMC before blocking (see Fig. 6.7 (a)) is similar to that of the original HC-MMC. After the converter is blocked, the equivalent models of the dc and ac circulating current for the mixed-SM HC-MMC are shown in Fig. 6.7 (b) and (c), where C_{fm} is the FB-SM capacitance in the main power stage. It is seen that the equivalent model for the dc circulating current is an RLC circuit due to the existence of FB SMs in the main power stage, and the equivalent model for ac circulating current is similar to that of the original HC-MMC. As seen from Fig. 6.7 (b) and (c), the FB-SM capacitor voltage variation in the main power stage is contributed to by both the dc and ac circulating currents, and those in the phase limb are contributed to by the ac circulating currents only. Note that the polarities of the inserted FB-SM capacitor voltages (i.e., v_{ceq2} and v_{ceq3}) after blocking shown in Fig. 6.7 (b) and (c) are related to the polarities of $i_{dc-cir2}$ and $i_{ac-cir1}$, respectively.

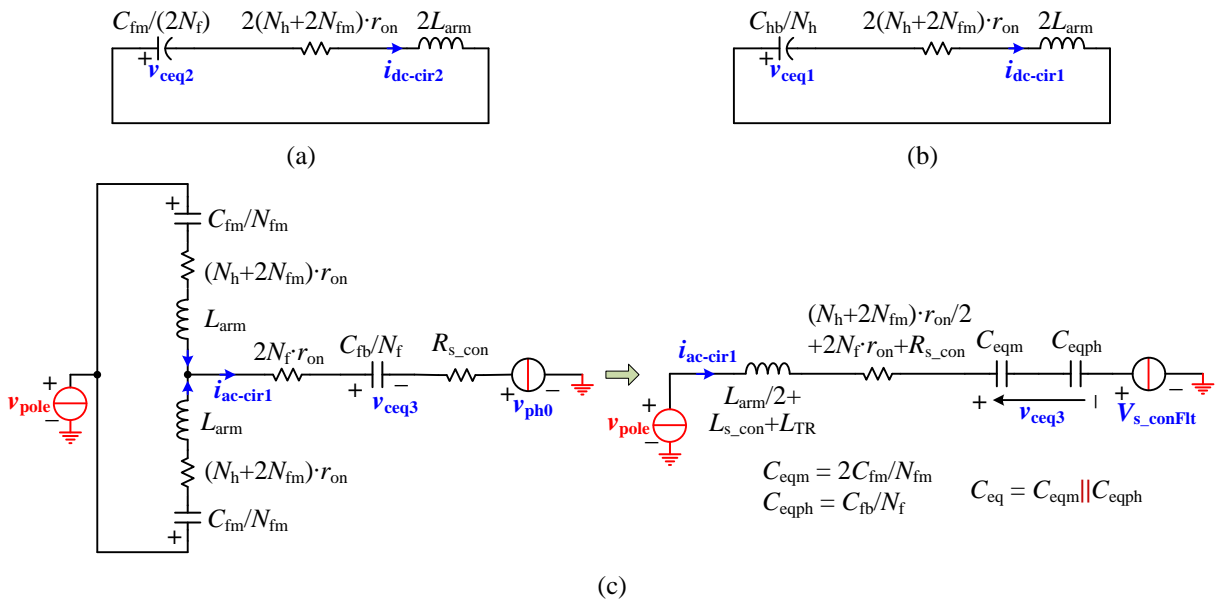


Fig. 6.7: Equivalent circuits of the mixed-SM HC-MMC under pole-to-pole fault

(a) model for the dc circulating current before blocking; (b) model for the dc circulating current after blocking; (c) model for the ac circulating current after blocking.

Based upon the analysis of the responses of generic RL and RLC circuits in Section 6.1.1, the parameters used for the responses of branch current and capacitor voltage in the circuits in Fig. 6.7 are summarized in Table 6.2, where v_{pole} is shown in (6.5). The final FB-SM capacitor voltages in the main power stage ($v_{\text{cfm-final}}$) and the phase limb ($v_{\text{cfb-final}}$) are calculated as follows:

$$v_{\text{cfm-final}} = \frac{\text{sign}(i_{\text{dc-cir2}}|_{t=t_{\text{flt}}+t_{\text{blk}}})v_{\text{ceq2}}|_{t=t_{\text{flt}}+t_{\text{blk}}+t_{\text{clr}}} + \frac{C_{\text{eqph}}}{C_{\text{eqm}} + C_{\text{eqph}}} \frac{\text{sign}(i_{\text{ac-cir1}}|_{t=t_{\text{flt}}+t_{\text{blk}}})\Delta v_{\text{ceq3}}}{N_{\text{fm}}}}{2N_{\text{fm}}} \quad (6.10)$$

$$v_{\text{cfb-final}} = \frac{V_{\text{dc}}}{2N_{\text{f}}} + \frac{C_{\text{eqm}}}{C_{\text{eqm}} + C_{\text{eqph}}} \frac{\text{sign}(i_{\text{ac-cir1}}|_{t=t_{\text{flt}}+t_{\text{blk}}})\Delta v_{\text{ceq3}}}{N_{\text{f}}} \quad (6.11)$$

where

$$\Delta v_{\text{ceq3}} = v_{\text{ceq3}}|_{t=t_{\text{flt}}+t_{\text{blk}}+t_{\text{clr}}} - \text{sign}(i_{\text{ac-cir1}}|_{t=t_{\text{flt}}+t_{\text{blk}}})(1 + 2N_{\text{fm}}/N_{\text{h}})V_{\text{dc}}/2 \quad (6.12)$$

Table 6.2: Parameters for the equivalent circuit models (in Fig. 6.7) of the mixed-SM HC-MMC

Parameters	DC equivalent circuit models		AC equivalent circuit models
	Before blocking ($t_{\text{flt}} < t < t_{\text{flt}}+t_{\text{blk}}$)	After blocking ($t_{\text{flt}}+t_{\text{blk}} < t < t_{\text{flt}}+t_{\text{blk}}+t_{\text{clr}}$)	After blocking ($t_{\text{flt}}+t_{\text{blk}} < t < t_{\text{flt}}+t_{\text{blk}}+t_{\text{clr}}$)
Circuit type	RLC	RLC	RLC
Solution variables	v_{ceq1} and $i_{\text{dc-cir1}}$	v_{ceq2} and $i_{\text{dc-cir2}}$	v_{ceq3} and $i_{\text{ac-cir1}}$
R_{eq}	$2(N_{\text{h}}+2N_{\text{fm}}) \cdot r_{\text{on}}$	$2(N_{\text{h}}+2N_{\text{fm}}) \cdot r_{\text{on}}$	$(N_{\text{h}}+2N_{\text{fm}}) \cdot r_{\text{on}}/2 + 2N_{\text{f}} \cdot r_{\text{on}} + R_{\text{s_con}}$
L_{eq}	$2L_{\text{arm}}$	$2L_{\text{arm}}$	$L_{\text{arm}}/2 + L_{\text{s_con}} + L_{\text{TR}}$
C_{eq}	$C_{\text{hb}}/N_{\text{h}}$	$C_{\text{fm}}/(2N_{\text{fm}})$	$C_{\text{eqm}} \parallel C_{\text{eqph}}$
t_0	t_{flt}	$t_{\text{flt}} + t_{\text{blk}}$	$t_{\text{flt}} + t_{\text{blk}}$
I_{Leq0}	$(i_{\text{up}}+i_{\text{low}})/2 _{t=t_{\text{flt}}}$	$i_{\text{dc-cir1}} _{t=t_{\text{flt}} + t_{\text{blk}}}$	$i_{\text{con}} _{t=t_{\text{flt}} + t_{\text{blk}}}$
V_{ceq0}	V_{dc}	$\text{sign}(I_{\text{Leq0}}) \cdot (2N_{\text{fm}}/N_{\text{h}})V_{\text{dc}}$	$\text{sign}(I_{\text{Leq0}}) \cdot (1+2N_{\text{fm}}/N_{\text{h}}) \cdot V_{\text{dc}}/2$
V_{s}	0	0	$(v_{\text{s_con}} _{t=t_{\text{flt}} + t_{\text{blk}}}) - v_{\text{pole}}$
t_{clr}	N/A	$\tan^{-1}(-A_1/A_2)/\omega_{\text{d}}$	$\tan^{-1}(-A_1/A_2)/\omega_{\text{d}}$
$v_{\text{csm-final}}$	$v_{\text{ceq}}/N_{\text{h}} _{t=t_{\text{flt}} + t_{\text{blk}}}$	see (6.10)	see (6.11)

Comparing the circuits shown in Fig. 6.3 (c) and Fig. 6.7 (c), the ac equivalent model of the mixed-SM HC-MMC after blocking is similar to that of the original HC-MMC. The analysis of

the original HC-MMC shown in Fig. 6.6 is also valid for the mixed-SM HC-MMC. However, the dc equivalent circuit of the mixed-SM HC-MMC after blocking is different from that of the original HC-MMC, where the mixed-SM HC-MMC has FB-SM capacitors inserted in the path for dc circulating current. With the system parameters of $V_{dc} = 500.0$ kV, $P_{dc} = 500.0$ MW, $N_h = 100$, $N_{fm} = 10$, $L_{arm} = 0.05$ H, and $r_{on} = 5$ m Ω for mixed-SM HC-MMC, a pole-to-pole fault is applied at the dc circulating current with -5.0 kA upon blocking. With various FB-SM capacitance (C_{fm}) and equivalent resistance (R_{eq}), Fig. 6.8 displays the responses of the dc circulating current and FB-SM capacitor voltage in the main power stage of the mixed-SM HC-MMC after blocking.

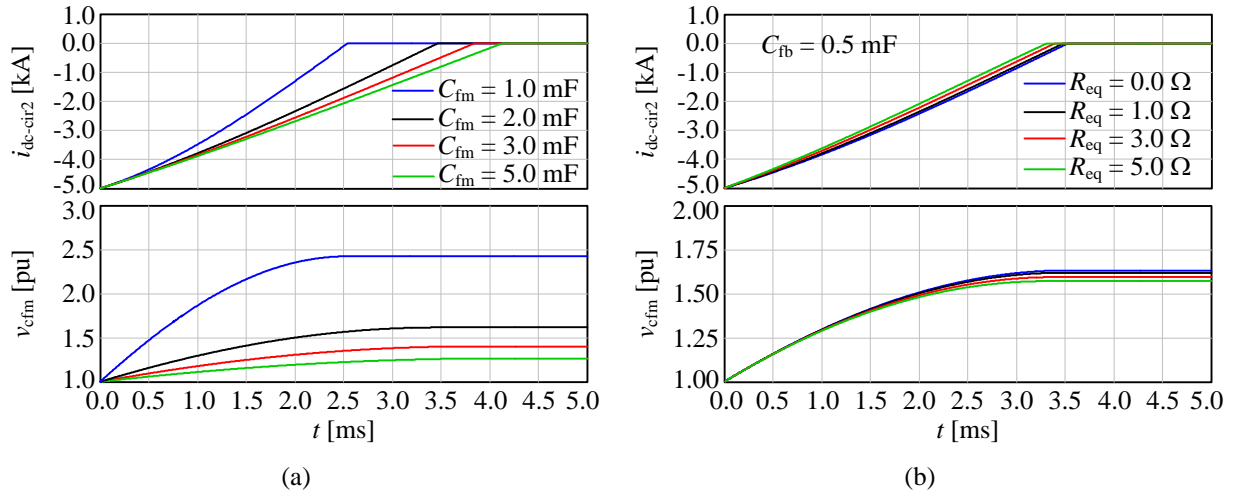


Fig. 6.8: Responses of the dc-side current and FB-SM capacitor voltage in the main power stage of mixed-SM HC-MMC after blocking

(a) responses with various C_{fm} and $R_{eq} = 2(N_h + 2N_{fm}) \cdot r_{on}$; (b) responses with $C_{fm} = 2.5$ mF and various R_{eq} .

As observed from Fig. 6.8, the dc fault current is quickly cleared (≤ 4.0 ms) with C_{fm} varying within 1.0 mF ~ 5.0 mF. If there are no FB SMs in the main power stage, the dc fault current takes approximately 0.5 s, which is equal to $5\tau = 5L_{eq}/R_{eq} = 10L_{arm}/(2N_h \cdot r_{on})$, to decay to zero. This results in approximately 125 times of the dc-current clearing time in the mixed-SM HC-MMC. However, the FB-SM capacitor voltage in the main power stage is increased due to charging with the large dc circulating current. As such, considerations for capacitor sizing in the main power

stage under a pole-to-pole fault is of importance to avoid overvoltage damage for FB-SM capacitors, which is shown in Section 6.2.2. As seen from Fig. 6.8 (b), the equivalent resistance varying within a reasonable range ($0.0 \Omega \sim 5.0 \Omega$) has slight influence on both the dc-current clearing time and FB-SM capacitor voltage rise. Therefore, the equivalent resistance in the equivalent model in Fig. 6.7 (b) is neglected in the analysis in Section 6.2.2.

6.2 Considerations for SM capacitance under a pole-to-pole fault

In practice, when a pole-to-pole fault occurs, the system blocks the gate signals of the converter within a short time due to either the overcurrent protection or the dc-fault detection [90]. After the dc fault occurs and before blocking, the converter is still in operation as normal but with a faulted dc side, resulting in voltage drops in the SM capacitors. If the SM capacitor voltages drop excessively, the converter may require a pre-charge function for SM capacitors to avoid large inrush currents in the arms, resulting in long recovery time from the dc fault. To promptly recover the system to normal operation after the dc fault is cleared, proper SM capacitance must be selected to maintain the capacitor voltages close to their nominal values. After blocking the converter, the FB SMs in the main power stage of the mixed-SM HC-MMC are charged to decay the dc-side fault current, whereas the FB stacks in both the original and mixed-SM HC-MMCs are charged to decay the ac-side current. The FB-SM capacitance used in the main power stage and the phase limb must be properly selected to avoid overvoltage damage during a dc fault.

The equivalent circuit models under a pole-to-pole fault for the original and mixed-SM HC-MMCs are shown in Fig. 6.3 and Fig. 6.7, respectively. To simplify the analysis, the equivalent resistors in all RLC equivalent models are neglected, as they are generally very small and have negligible influence within a very short blocking or dc- and ac-current clearing time. As such, the

parameters α and ω_d shown in (6.7) are simplified as $\alpha = 0$ and $\omega_d = \omega_r$. The general solution expressed in (6.6) can be modified as follows:

$$\begin{aligned} v_{\text{ceq}}(t) &= (V_{\text{ceq}0} + V_s) \cdot \cos(\omega_r(t - t_{\text{start}})) + I_{\text{Leq}0} \sqrt{\frac{L_{\text{eq}}}{C_{\text{eq}}}} \sin(\omega_r(t - t_0)) - V_s, \text{ for } t \geq t_{\text{start}} \\ i_{\text{Leq}}(t) &= I_{\text{Leq}0} \cos(\omega_r(t - t_{\text{start}})) - (V_{\text{ceq}0} + V_s) \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}} \sin(\omega_r(t - t_0)), \text{ for } t \geq t_{\text{start}} \end{aligned} \quad (6.13)$$

Assume that the voltage and current shown in (6.13) reach $k_v \cdot V_{\text{ceq}0}$ and $k_i \cdot I_{\text{Leq}0}$ at the time $t = t_0 + t_{\text{oc}}$. With the expressions shown in (6.13), the general relationship between C_{eq} and k_v or k_i is obtained as in (6.15).

$$\begin{aligned} (V_{\text{ceq}0} + V_s) \cdot \cos(\omega_r t_{\text{oc}}) + I_{\text{Leq}0} \sqrt{\frac{L_{\text{eq}}}{C_{\text{eq}}}} \sin(\omega_r t_{\text{oc}}) - V_s &= k_v V_{\text{ceq}0} \\ I_{\text{Leq}0} \cos(\omega_r t_{\text{oc}}) - (V_{\text{ceq}0} + V_s) \sqrt{\frac{C_{\text{eq}}}{L_{\text{eq}}}} \sin(\omega_r t_{\text{oc}}) &= k_i I_{\text{Leq}0} \end{aligned} \quad (6.14)$$

$$\begin{aligned} C_{\text{eq}} &= L_{\text{eq}} \left(\frac{I_{\text{Leq}0}}{V_{\text{ceq}0} + V_s} \right)^2 \frac{k_i^2 - 1}{1 - k_{\text{veq}}^2} \quad \text{or} \quad k_{\text{veq}} = \sqrt{1 - \frac{L_{\text{eq}}}{C_{\text{eq}}} \left(\frac{I_{\text{Leq}0}}{V_{\text{ceq}0} + V_s} \right)^2 (k_i^2 - 1)} \\ \sin(\omega_r t_{\text{oc}}) &= \text{sign} \left(\frac{I_{\text{Leq}0}}{V_{\text{ceq}0} + V_s} \right) \cdot \frac{(1 - k_i^2)}{k_{\text{veq}} + k_i} \sqrt{\frac{1 - k_{\text{veq}}^2}{k_i^2 - 1}} \end{aligned} \quad (6.15)$$

where

$$k_{\text{veq}} = \frac{k_v + V_s/V_{\text{ceq}0}}{1 + V_s/V_{\text{ceq}0}}, \quad \omega_r = \frac{1}{\sqrt{L_{\text{eq}} C_{\text{eq}}}} \quad (6.16)$$

Based upon the equivalent models under a pole-to-pole fault (see Section 6.1) and the general solutions shown in (6.15) for RLC circuits, considerations of SM capacitor sizing for the original and mixed-SM HC-MMCs under a pole-to-pole fault are discussed in the following subsections. They include the HB-SM capacitance requirement in the main power stage in both the original and

mixed-SM HC-MMCs (see Section 6.2.1), the FB-SM capacitance requirement in the main power stage of the mixed-HC-MMC (see Section 6.2.2), and the FB-SM capacitance requirement in both the original and mixed-SM HC-MMCs (see Section 6.2.3).

6.2.1 Considerations of HB-SM capacitance in the main power stage

Within the interval after the dc fault occurs and before blocking the converter, the equivalent model of the main power stage for the original HC-MMC shown in Fig. 6.3 (a) is a special case of the mixed-SM HC-MMC with $k_{fm} = 0$ shown in Fig. 6.7 (a). As seen from the parameters summarized in Table 6.1 and Table 6.2, the equivalent circuit parameters and initial values at the instant of dc fault are expressed as follows:

$$\begin{aligned} V_{ceq0} &= V_{dc}, \quad I_{Leq0} = I_{dc}/3, \quad V_s = 0, \quad t_{start} = t_0 \\ L_{eq} &= 2L_{arm}, \quad C_{eq} = C_{hb}/N_h \end{aligned} \quad (6.17)$$

where the dc fault occurs at $t = t_0$. Regardless of the rectifier- or inverter-mode operation, the dc circulating current is typically negative upon blocking the converter after a pole-to-pole fault occurs. Assume that the individual HB-SM capacitor voltage drops to $k_{vcsmFlt} \cdot V_{dc}/N_h$, when the overcurrent protection triggers due to dc faults at the current of $-k_{iarmPro} \cdot \text{sign}(I_{dc}) \cdot I_{dc}/3$, which is negative for either rectifier- or inverter-mode operation. Compared with the equations shown in (6.14), the equivalent k_i and k_v are expressed as follows:

$$\begin{cases} i_{Leq}(t_0 + t_{blk}) = -k_{iarmPro} \text{sign}(I_{dc}) I_{dc} / 3 = -k_{iarmPro} \text{sign}(I_{dc}) I_{Leq0}, \\ v_{ceq}(t_0 + t_{blk}) = k_{vcsmFlt} V_{dc} = k_{vcsmFlt} V_{ceq0} \end{cases} \quad (6.18)$$

$$\Rightarrow k_i = -k_{iarmPro} \text{sign}(I_{dc}), \quad k_v = k_{vcsmFlt}$$

where $k_{iarmPro} > 1.0$, and $k_{vcsmFlt} < 1.0$, because the HB-SM capacitor voltages are decreased and the dc-fault current is increased after the dc fault occurs. Substituting (6.17) and (6.18) into (6.15),

the expressions of the equivalent capacitance ($C_{eq} = C_{hb}/N_h$) in the equivalent models shown in Fig. 6.3 (a) and Fig. 6.7 (a) and the blocking delay time (t_{blk}) are obtained as follows:

$$\begin{aligned}
C_{eq} &= 2L_{arm} \left(\frac{I_{dc}}{3V_{dc}} \right)^2 \frac{k_{iarmPro}^2 - 1}{1 - k_{vcsmFlt}^2} = \frac{(P_{ref} m_{rated})^2 P_{nom} X_{Larm}}{12V_{dc}^2 \omega_o} \cdot \frac{k_{iarmPro}^2 - 1}{1 - k_{vcsmFlt}^2} \\
\sin(\omega_r t_{blk}) &= \text{sign} \left(\frac{I_{dc}}{3V_{dc}} \right) \frac{\sqrt{(1 - k_{vcsmFlt}^2)(k_{iarmPro}^2 - 1)}}{\text{sign}(P_{ref}) k_{iarmPro} - k_{vcsmFlt}} \\
\Rightarrow t_{blk} &= \frac{4\omega_o}{P_{ref} m_{rated}^2 X_{Larm}} \sqrt{\frac{1 - k_{vcsmFlt}^2}{k_{iarmPro}^2 - 1}} \sin^{-1} \left(\text{sign}(P_{ref}) \frac{\sqrt{(1 - k_{vcsmFlt}^2)(k_{iarmPro}^2 - 1)}}{\text{sign}(P_{ref}) k_{iarmPro} - k_{vcsmFlt}} \right)
\end{aligned} \tag{6.19}$$

where C_{eq} is simplified with the expressions of L_{arm} and I_{dc} shown in (4.2) and (4.4), and $P_{ref} > 0$ for inverter-mode operation and $P_{ref} < 0$ for rectifier-mode operation. As such, the stored energy of all HB-SM capacitors in both the original and mixed-SM HC-MMC per power rating unit under a pole-to-pole fault, $EoP_{HBmainFlt}$, is calculated as follows:

$$\begin{aligned}
EoP_{HBmainFlt} &= \frac{6N_h \cdot C_{sm} \cdot (V_{dc}/N_h)^2 / 2}{P_{nom}} \times 10^3 = \frac{3C_{eq} V_{dc}^2}{P_{nom}} \times 10^3 \\
&= \frac{(P_{ref} m_{rated})^2 X_{Larm}}{4\omega_o} \cdot \frac{k_{iarmPro}^2 - 1}{1 - k_{vcsmFlt}^2} \times 10^3 \text{ [kJ/MVA]}
\end{aligned} \tag{6.20}$$

It is seen that both C_{eq} in (6.19) and $EoP_{HBmainFlt}$ in (6.20) are proportional to $m_{rated}^2 \cdot X_{Larm}$, and t_{blk} in (6.19) is inversely proportional to $m_{rated}^2 \cdot X_{Larm}$. Consider two cases for the mixed-SM HC-MMC after adding FB SMs in the main power stage: (i) all the system parameters are kept the same as those for the original HC-MMC, i.e., $k_{fm} = 0$; (ii) only the parameter of transformer's turns ratio is changed to $(1+2k_{fm}) \cdot n_{tr0}$, where n_{tr0} is the transformer's turns ratio for the original HC-MMC. The latter case results in $m_{rated}' = (1+2k_{fm}) \cdot m_{rated}$ and $X_{Larm}' = X_{Larm}/(1+2k_{fm})^2$ to keep the arm inductance value unchanged, where m_{rated} and X_{Larm} are the parameters for the original HC-MMC. As such, $m_{rated}'^2 \cdot X_{Larm}' = m_{rated}^2 \cdot X_{Larm}$. In other words, $m_{rated}^2 \cdot X_{Larm}$ is independent of k_{fm} under the

considered two cases. Therefore, $EoP_{HBmainFlt}$, $C_{eq} (= C_{hb}/N_h)$, and t_{blk} for the mixed-SM HC-MMC are independent of k_{fm} and have the the same values as those of the original HC-MMC.

With the system parameters of $f_o = 60$ Hz, $P_{ref} = 1.0$ pu (inverter mode), $m_{rated} = 1.0$, $X_{Larm} = 0.2$ pu, $k_{iarmPro}$ in the rage of [2.0 pu, 6.0 pu] as base of $I_{dc}/3$, and $k_{vcsmFlt}$ in the range of [0.50 pu, 0.95 pu], $EoP_{HBmainFlt}$ for the original HC-MMC under a pole-to-pole fault and the blocking delay are plotted in Fig. 6.9. It is seen that $EoP_{HBmainFlt}$ is increased when $k_{iarmPro}$ and $k_{vcsmFlt}$ increase, and the blocking delay is increased when $k_{iarmPro}$ increases and is slightly influenced by $k_{vcsmFlt}$. Under the investigated system parameters, the value of $EoP_{HBmainFlt}$ is in the range of [5.0 kJ/MVA, 45.0 kJ/MVA] and t_{blk} is less than 1.0 ms.

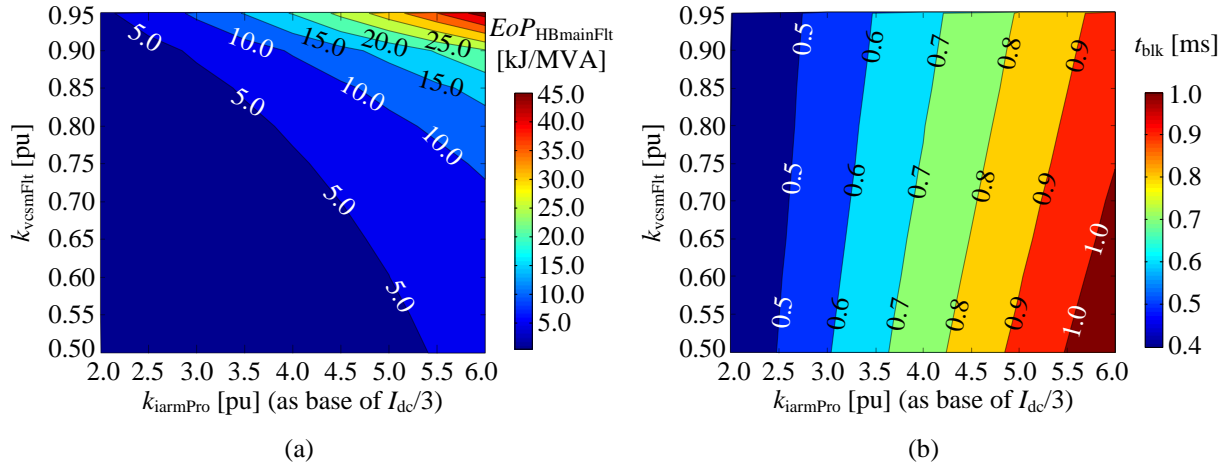


Fig. 6.9: Stored energy of all HB-SM capacitors in the original HC-MMC per power rating unit under a pole-to-pole fault and blocking delay

(a) $EoP_{HBmainFlt}$; (b) blocking delay.

Comparing $EoP_{HBmainFlt}$ under a pole-to-pole fault with EoP_{HBmain} in normal operation, the maximum value is selected to meet both the ripple requirement in normal operation and the performance requirement under a pole-to-pole fault. If the stored energy of HB-SM capacitors per power rating unit is selected as a certain value (denoted as $EoP_{HBmain0}$), the HB-SM capacitor voltage upon blocking under a pole-to-pole fault is calculated as follows:

$$k_{\text{vcsmFlt}} = \sqrt{1 - \frac{2L_{\text{arm}}}{C_{\text{eq}}} \left(\frac{I_{\text{dc}}}{3V_{\text{dc}}} \right)^2 (k_{\text{iarmPro}}^2 - 1)} = \sqrt{1 - \frac{(P_{\text{ref}} m_{\text{rated}})^2 X_{\text{Larm}}}{4\omega_o EoP_{\text{HBmain0}}} (k_{\text{iarmPro}}^2 - 1) \times 10^3} \quad (6.21)$$

As seen from EoP_{HBmain} under normal operation shown in Fig. 4.16 and Fig. 4.19 (a), EoP_{HBmain} is selected in the range of 30.0~50.0 kJ/MVA for the original HC-MMC and 18.0~32.0 kJ/MVA for the mixed-SM HC-MMC with 6%~12% FB SMs added to the main power stage and transformer's turns ratio proportionally changed. Considering the system with $f_o = 60\text{Hz}$, $P_{\text{ref}} = 1.0$ pu, $m_{\text{rated}} = 0.95$ and $X_{\text{Larm}} = 0.15$ pu, the HB-SM capacitor voltage decreases to 0.988~0.993 pu with $k_{\text{iarmPro}} = 3.0$, and 0.946~0.968 pu with $k_{\text{iarmPro}} = 6.0$ for the original HC-MMC. With the same system parameters shown above, the HB-SM capacitor voltage decreases to 0.98~0.989 pu with $k_{\text{iarmPro}} = 3.0$, and 0.909~0.95 pu with $k_{\text{iarmPro}} = 6.0$ for the mixed-SM HC-MMC. It shows that with SM capacitor size selected based upon normal operation, the SM capacitor voltages have relatively small drops after a dc fault occurs and before the converter is blocked within a short time. Therefore, the HB-SM capacitance selections for both the original and mixed-SM HC-MMCs based upon normal operation are adequate to achieve proper performance during dc faults.

6.2.2 Considerations of the FB-SM capacitance in the main power stage of mixed-SM HC-MMC

Since the dc circulating current is typically negative upon blocking the converter after a pole-to-pole fault, the equivalent capacitor voltage (i.e., v_{ceq2} in Fig. 6.7 (b)) in the equivalent model of the dc circulating current after blocking is negative. As seen from the parameters summarized in Table 6.2, the equivalent circuit parameters and the initial points upon blocking are as follows:

$$\begin{aligned} V_{\text{ceq0}} &= -2k_{\text{fm}} V_{\text{dc}}, \quad I_{\text{Leq0}} = -k_{\text{iarmPro}} \text{sign}(I_{\text{dc}}) I_{\text{dc}}/3, \quad V_{\text{s}} = 0, \quad t_{\text{start}} = t_0 + t_{\text{blk}} \\ L_{\text{eq}} &= 2L_{\text{arm}}, \quad C_{\text{eq}} = C_{\text{fbm}}/(2N_{\text{fm}}) = C_{\text{fbm}}/(2k_{\text{fm}} N_{\text{h}}) \end{aligned} \quad (6.22)$$

where $k_{iarmPro} > 1.0$ and $I_{Leq0} < 0$ for either rectifier- or inverter-mode operation; t_{blk} is the blocking delay after the dc fault occurs. As discussed in Section 6.2.1, upon blocking the converter, the HB-SM capacitor voltage drops are fairly small with the HB-SM capacitance selection under normal operation. Therefore, the initial value of the equivalent capacitor voltage (v_{ceq2} in Fig. 6.7 (b)) upon blocking is approximately $-2k_{fm}V_{dc}$ as used in (6.22). Assume that the individual FB-SM capacitor voltage in the main power stage of mixed-SM HC-MMC is charged to $k_{vcfmBlk} \cdot V_{dc}/N_h$, when the fault current decays to zero. Compared with the equations shown in (6.14), the equivalent k_i and k_v are expressed as follows:

$$\begin{aligned} i_{Leq}(t_0 + t_{blk} + t_{dc-clr}) &= 0, \quad v_{ceq}(t_0 + t_{blk} + t_{dc-clr}) = k_{vcfmBlk}(-2k_{fm}V_{dc}) = k_{vcfmBlk}V_{ceq0} \\ \Rightarrow k_i &= 0, \quad k_v = k_{vcfmBlk} \end{aligned} \quad (6.23)$$

where $k_{vcfmBlk} > 1.0$, since the FB-SM capacitor voltages are charged after the converter is blocked. Substituting (6.22) and (6.23) into (6.15), the expressions of equivalent capacitance (C_{eq}) shown in Fig. 6.7 (b) and the dc-current clearing time (t_{dc-clr}) are obtained as follows:

$$\begin{aligned} C_{eq} &= 2L_{arm} \left(\frac{k_{iarmPro} \text{sign}(I_{dc}) I_{dc}}{6k_{fm} V_{dc}} \right)^2 \frac{1}{k_{vcfmBlk}^2 - 1} = \frac{(P_{ref} m_{rated})^2 P_{nom} X_{Larm}}{12V_{dc}^2 \omega_o} \cdot \frac{k_{iarmPro}^2}{4k_{fm}^2 (k_{vcfmBlk}^2 - 1)} \\ \sin(\omega_r t_{dc-clr}) &= \text{sign} \left(\frac{k_{iarmPro} \text{sign}(I_{dc}) I_{dc}}{6k_{fm} V_{dc}} \right) \frac{\sqrt{k_{vcfmBlk}^2 - 1}}{k_{vcfmBlk}} = \frac{\sqrt{k_{vcfmBlk}^2 - 1}}{k_{vcfmBlk}} \\ \Rightarrow t_{dc-clr} &= \frac{8\omega_o k_{fm} \sqrt{k_{vcfmBlk}^2 - 1}}{P_{ref} m_{rated}^2 X_{Larm} k_{iarmPro}} \sin^{-1} \left(\frac{\sqrt{k_{vcfmBlk}^2 - 1}}{k_{vcfmBlk}} \right) \end{aligned} \quad (6.24)$$

where C_{eq} and t_{dc-clr} are simplified with the expressions of L_{arm} and I_{dc} shown in (4.2) and (4.4), respectively; $k_{vcfmBlk} > 1$, because the FB-SM capacitor voltages are charged after the converter is blocked. The stored energy of all FB-SM capacitors in the main power stage of the mixed-SM HC-MMC per power rating unit under a pole-to-pole fault, $EoP_{FBmainFlt}$, is calculated as follows:

$$\begin{aligned}
EoP_{\text{FBmainFlt}} &= \frac{6N_{\text{fm}} \cdot C_{\text{fbm}} \cdot (V_{\text{dc}}/N_{\text{h}})^2/2}{P_{\text{nom}}} \times 10^3 = \frac{6C_{\text{eq}} (k_{\text{fm}} V_{\text{dc}})^2}{P_{\text{nom}}} \times 10^3 \\
&= \frac{(P_{\text{ref}} m_{\text{rated}})^2 X_{\text{Larm}}}{8\omega_o} \cdot \frac{k_{\text{iarmPro}}^2}{k_{\text{vcfmBlk}}^2 - 1} \times 10^3 \text{ [kJ/MVA]}
\end{aligned} \tag{6.25}$$

It is seen that both C_{eq} in (6.24) and $EoP_{\text{FBmainFlt}}$ in (6.25) are proportional to $m_{\text{rated}}^2 \cdot X_{\text{Larm}}$, and $t_{\text{dc-clr}}$ in (6.24) is inversely proportional to $m_{\text{rated}}^2 \cdot X_{\text{Larm}}$. Similar to the analysis of $m_{\text{rated}}^2 \cdot X_{\text{Larm}}$ for the mixed-SM HC-MMC shown in Section 6.2.1, $m_{\text{rated}}^2 \cdot X_{\text{Larm}}$ is independent of k_{fm} , whether the mixed-SM HC-MMC keeps the transformer's turns ratio same as that in the mixed-SM HC-MMC with $k_{\text{fm}} = 0$ or changes the transformer's turns ratio to $(1+2k_{\text{fm}}) \cdot n_{\text{tr0}}$, where n_{tr0} is the turns ratio for the transformer in the mixed-SM HC-MMC with $k_{\text{fm}} = 0$. Therefore, $EoP_{\text{FBmainFlt}}$ is independent of k_{fm} , and C_{eq} shown in (6.24) is inversely proportional to k_{fm}^2 and $t_{\text{dc-clr}}$ is proportional to k_{fm} .

With the system parameters of $f_o = 60$ Hz, $P_{\text{ref}} = 1.0$ pu, $m_{\text{rated}} = 1.0$, $X_{\text{Larm}} = 0.2$ pu, $k_{\text{fm}} = 0.1$, k_{iarmPro} in the range of [2.0 pu, 6.0 pu] as base of $I_{\text{dc}}/3$, and k_{vcfmBlk} in the range of [1.05 pu, 1.5 pu], $EoP_{\text{FBmainFlt}}$ for the mixed-SM HC-MMC under a pole-to-pole fault and the dc-current clearing time are displayed in Fig. 6.10.

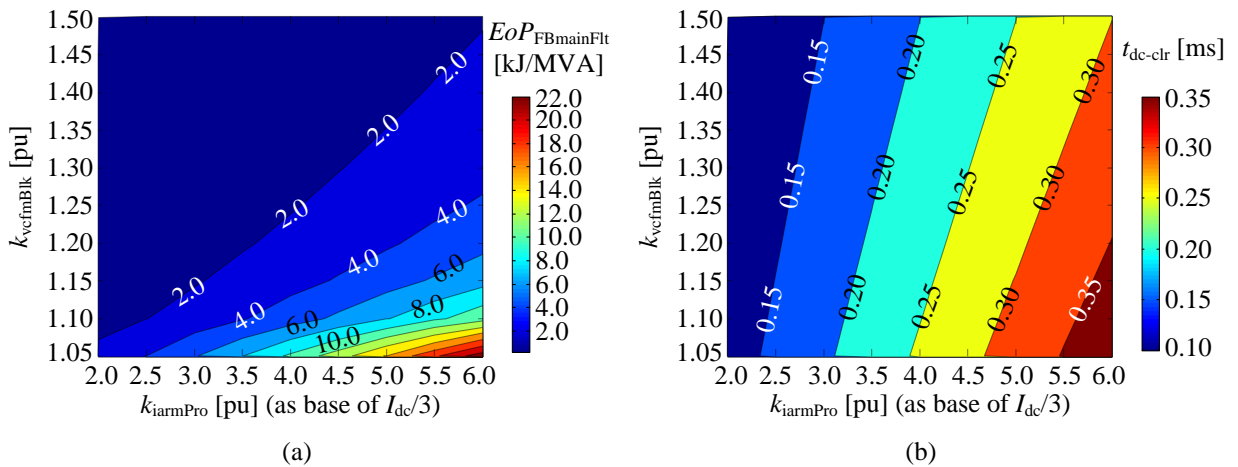


Fig. 6.10: Stored energy of all FB-SM capacitors in the main power stage of mixed-SM HC-MMC under a pole-to-pole fault per power rating unit and the dc-current clearing time with $k_{\text{fm}} = 0.1$

(a) $EoP_{\text{FBmainFlt}}$; (b) dc-current clearing time.

As seen from Fig. 6.10 (a), $EoP_{FBmainFlt}$ is increased with $k_{iarmPro}$ increasing and $k_{vcfmBlk}$ decreasing, and it is in the range of [2.0 kJ/MVA, 22.0 kJ/MVA] under the investigated conditions. As seen from Fig. 6.10 (b), the influence of $k_{vcfmBlk}$ on the dc-current clearing time can be neglected, and t_{dc-clr} is slightly increased with $k_{iarmPro}$ increasing and is small in the range of [0.05 ms, 0.35 ms] under the investigated system parameters.

Comparing $EoP_{FBmainFlt}$ under a pole-to-pole fault with EoP_{FBmain} in normal operation, the maximum value is selected to ensure proper and safe operation for the FB SMs in the main power stage. If the stored energy of all FB-SM capacitors per power rating unit is selected as a certain value (denoted as $ED_{FBmain0}$), the FB-SM capacitor voltage after blocking the dc fault is calculated as follows:

$$k_{vcfmBlk} = \sqrt{1 + \frac{2L_{arm}}{C_{eq}} \left(\frac{k_{iarmPro} I_{dc}}{6k_{fm} V_{dc}} \right)^2} = \sqrt{1 + \frac{(P_{ref} m_{rated})^2 X_{Larm} k_{iarmPro}^2}{8\omega_o EoP_{FBmain0}} \times 10^3} \quad (6.26)$$

As seen from EoP_{FBmain} under normal operation shown in Fig. 4.19 (a), EoP_{FBmain} is selected in the range of 2.0~15.0 kJ/MVA for the mixed-SM HC-MMC with 6%~12% FB SMs added to the main power stage and transformer's turns ratio proportionally changed. Considering the system with $f_o = 60\text{Hz}$, $P_{ref} = 1.0$ pu, $m_{rated} = 0.95$ and $X_{Larm} = 0.15$ pu, the FB-SM capacitor voltage in the main power stage of the mixed-SM HC-MMC increases to 1.013~1.096 pu with $k_{iarmPro} = 3.0$, and 1.096~1.345 pu with $k_{iarmPro} = 6.0$. However, if $k_{iarmPro}$ is large and selected as 10.0 for example, the FB-SM capacitor voltage will increase to 1.14~1.8 pu. Therefore, after selecting the FB-SM capacitance for the main power stage of the mixed-SM HC-MMC under normal operation, it is recommended to calculate the FB-SM capacitor voltage rise using the system's permissible dc-fault current. If the capacitor voltage reaches a value much higher than the capacitor's rated voltage, the capacitance calculated under dc-fault conditions must be used to avoid overvoltage damages.

6.2.3 Considerations of the FB-SM capacitance in the phase limb

The equivalent models of the ac circulating current for the original and mixed-SM HC-MMCs after blocking the converter are shown in Fig. 6.3 (c) and Fig. 6.7 (c), respectively. It is seen that the equivalent model for the mixed-SM HC-MMC has two capacitors with capacitance of C_{eqm} ($= 2C_{fm}/N_{fm}$) and C_{eqph} ($= C_{fb}/N_f$). Assuming that the FB-SM capacitances in the main power stage and phase limb are designed based upon normal operation, the relationship between C_{eqm} and C_{eqph} is derived as follows:

$$\frac{C_{eqm}}{C_{eqph}} = \frac{2C_{fm}/N_{fm}}{C_{fb}/N_f} = \frac{2EoP_{FBmain}P_{nom}/(3V_{dc}^2k_{fm}^2)}{8EoP_{FBph}P_{nom}/(3V_{dc}^2)} = \frac{EoP_{FBmain}}{4k_{fm}^2EoP_{FBph}} \quad (6.27)$$

As seen from Fig. 4.19 (a) and the analysis in Section 4.3.3, EoP_{FBmain} and EoP_{FBph} are roughly selected as 12.0 kJ/MVA with $k_{fm} = 0.1$ and 6.0 kJ/MVA, respectively. Under this condition, C_{eqm} is equal to $50C_{eqph}$. Therefore, C_{eqm} is much larger than C_{eqph} . To simplify the equivalent model of the ac circulating current for the mixed-SM HC-MMC, C_{eqm} is replaced with a constant voltage source with a voltage of $\pm k_{fm}V_{dc}$, where the voltage polarity is determined by the polarity of current $i_{ac-cir1}$ shown in Fig. 6.7 (c). The equivalent model of the original HC-MMC can be regarded as the special case of the mixed-SM HC-MMC with $k_{fm} = 0$. Therefore, the consideration of FB-SM capacitance in the phase limb of mixed-SM HC-MMC is analyzed.

Based upon the theoretical calculation of operating points for a VSC shown in Fig. 4.1, denote the ideal grid source reflected to the converter-side and the converter-side current of phase A as follows:

$$\begin{aligned} v_{sA_con}(t) &= \sqrt{2}V_{s_con_nom} \sin(\omega_o t) \\ i_{conA}(t) &= \sqrt{2}I_{con} \sin(\omega_o t + \theta_{icon}) \end{aligned} \quad (6.28)$$

where I_{con} and $\cos(\theta_{\text{con}})$ are shown in (4.6). Assume that the phase angle of $v_{\text{sA_con}}(t)$ is θ_{blk} when the converter is blocked after a pole-to-pole fault occurs. With the parameters summarized in Table 6.2 and the expression of v_{pole} after blocking shown in (6.5), the equivalent circuit parameters and the initial points upon blocking are expressed as follows:

$$\begin{aligned} I_{\text{Leq0}} &= \sqrt{2}I_{\text{con}} \sin(\theta_{\text{blk}} + \theta_{\text{icon}}), \quad V_{\text{ceq0}} = \text{sign}(I_{\text{Leq0}}) \cdot V_{\text{dc}}/2 \\ V_{\text{s}} &= \sqrt{2}V_{\text{s_con_nom}} \sin(\theta_{\text{blk}}) + \text{sign}(I_{\text{Leq0}}) \cdot k_{\text{fm}} V_{\text{dc}} - v_{\text{pole}} = \text{sign}(I_{\text{Leq0}}) m_{\text{eq}} V_{\text{dc}}/2 \\ L_{\text{eq}} &= L_{\text{arm}}/2 + L_{\text{s_con}} + L_{\text{TR}}, \quad C_{\text{eq}} = C_{\text{fb}}/N_{\text{f}}, \quad t_{\text{start}} = t_0 + t_{\text{blk}} \end{aligned} \quad (6.29)$$

where $L_{\text{s_con}}$ and L_{TR} are shown in (4.4), and

$$m_{\text{eq}} = \text{sign}(\sin(\theta_{\text{blk}} + \theta_{\text{icon}})) \left[\frac{m_{\text{rated}} \sin(\theta_{\text{blk}}) + 2k_{\text{fm}} \cdot \text{sign}(\sin(\theta_{\text{blk}} + \theta_{\text{icon}}))}{- \frac{1}{3} \left(\text{sign}(\sin(\theta_{\text{blk}} + \theta_{\text{icon}})) + \text{sign}(\sin(\theta_{\text{blk}} + \theta_{\text{icon}} - 2\pi/3)) \right)} \right] \quad (6.30)$$

Since the blocking delay is short, the influence on the FB-SM capacitor voltages in the phase limb before blocking is neglected. As such, the total voltage across the FB stack in the phase limb after blocking is approximately $V_{\text{dc}}/2$ as used in (6.29). Assume the individual FB-SM capacitor voltage in the phase limb is charged to $k_{\text{vcfbBlk}} \cdot V_{\text{dc}}/(2N_{\text{f}})$, when the phase current decays to zero. Compared with the equations shown in (6.14), the equivalent k_{i} and k_{v} are expressed as follows:

$$\begin{aligned} i_{\text{Leq}}(t_0 + t_{\text{blk}} + t_{\text{ac-clr}}) &= 0, \quad v_{\text{ceq}}(t_0 + t_{\text{blk}} + t_{\text{ac-clr}}) = k_{\text{vcfbBlk}} V_{\text{ceq0}} \\ \Rightarrow k_{\text{i}} &= 0, \quad k_{\text{v}} = k_{\text{vcfbBlk}}, \quad k_{\text{veq}} = \frac{k_{\text{vcfbBlk}} + V_{\text{s}}/V_{\text{ceq0}}}{1 + V_{\text{s}}/V_{\text{ceq0}}} = \frac{k_{\text{vcfbBlk}} + m_{\text{eq}}}{1 + m_{\text{eq}}} \end{aligned} \quad (6.31)$$

where $k_{\text{vcfbBlk}} > 1$, since the FB-SM capacitor voltages are charged after the converter is blocked. Substituting (6.29) and (6.31) into (6.15), the expressions of equivalent capacitance (C_{eqph}) shown in Fig. 6.7 (c) and the ac-current clearing time ($t_{\text{ac-clr}}$) are obtained as follows:

$$\begin{aligned}
C_{\text{eqph}} &= (L_{\text{arm}}/2 + L_{\text{s_con}} + L_{\text{TR}}) \left(\frac{\sqrt{2}I_{\text{con}} \sin(\theta_{\text{blk}} + \theta_{\text{icon}})}{(1+m_{\text{eq}})V_{\text{dc}}/2} \right)^2 \frac{1}{k_{\text{veq}}^2 - 1} \\
&= \frac{16P_{\text{nom}} X_0 \sin^2(\theta_{\text{blk}} + \theta_{\text{icon}})}{3V_{\text{dc}}^2 \omega_o (k_{\text{vcfbBlk}} - 1)(k_{\text{vcfbBlk}} + 1 + 2m_{\text{eq}})} \left[\frac{X_{\text{Larm}}}{2} + \frac{X_{\text{TR}}}{S_{\text{TR}}} + \frac{\text{Im}(\text{SCR})}{|\text{SCR}|^2} \right] \\
\sin(\omega_r t_{\text{ac-clr}}) &= \text{sign} \left(\frac{\sqrt{2}I_{\text{con}} \sin(\theta_{\text{blk}} + \theta_{\text{icon}})}{(1+m_{\text{eq}})V_{\text{dc}}/2} \right) \frac{\sqrt{k_{\text{veq}}^2 - 1}}{k_{\text{veq}}} \\
&= \text{sign} \left(\frac{\sin(\theta_{\text{blk}} + \theta_{\text{icon}})}{1+m_{\text{eq}}} \right) \frac{\sqrt{(k_{\text{vcfbBlk}} - 1)(k_{\text{vcfbBlk}} + 1 + 2m_{\text{eq}})}}{k_{\text{vcfbBlk}} + m_{\text{eq}}}
\end{aligned} \tag{6.32}$$

where C_{eqph} is simplified with the expressions of L_{arm} , L_{TR} and $L_{\text{s_con}}$ shown in (4.2), I_{dc} shown in (4.4) and $\cos(\theta_{\text{con}})$ shown in (4.6); the expression of X_0 is shown in (4.7). The stored energy of all FB-SM capacitors in the phase limb of the mixed-SM HC-MMC under a pole-to-pole fault per power rating unit is calculated as follows:

$$\begin{aligned}
EoP_{\text{FBphFlt}} &= \frac{3N_f \cdot C_{\text{fb}} \cdot (V_{\text{dc}}/(2N_f))^2/2}{P_{\text{nom}}} \times 10^3 = \frac{3C_{\text{eqph}} V_{\text{dc}}^2}{8P_{\text{nom}}} \times 10^3 \\
&= \frac{2X_0 \sin^2(\theta_{\text{blk}} + \theta_{\text{icon}})}{\omega_o (k_{\text{vcfbBlk}} - 1)(k_{\text{vcfbBlk}} + 1 + 2m_{\text{eq}})} \left[\frac{X_{\text{Larm}}}{2} + \frac{X_{\text{TR}}}{S_{\text{TR}}} + \frac{\text{Im}(\text{SCR})}{|\text{SCR}|^2} \right] \times 10^3 \text{ [kJ/MVA]}
\end{aligned} \tag{6.33}$$

It is seen that EoP_{FBphFlt} is related to the system parameters, including SCR, transformer's leakage inductance and arm inductance, and m_{eq} shown in (6.30) which is related m_{rated} and k_{fm} . Consider two cases of transformer's turns ratio for the mixed-SM HC-MMC after adding $k_{\text{fm}}N_h$ FB SMs per arm in the main power stage: (i) transformer's turns ratio is kept unchanged as $n_{\text{tr}0}$, and (ii) transformer's turns ratio is changed to $(1+2k_{\text{fm}}) \cdot n_{\text{tr}0}$, where $n_{\text{tr}0}$ is the transformer's turns ratio for original HC-MMC, i.e., the mixed-SM HC-MMC with $k_{\text{fm}} = 0$.

Considering the case that the converter is blocked at the positive peak of phase current, $\theta_{\text{flt}} = \pi/2 - \theta_{\text{con}}$, resulting in $\sin(\theta_{\text{flt}} + \theta_{\text{con}}) = 1.0$ and $\sin(\theta_{\text{flt}}) = \cos(\theta_{\text{con}})$, and v_{pole} shown in (6.5) is equal

to $-V_{dc}/6$. With system parameters of $f_o = 60$ Hz, $P_{ref} = 1.0$ pu, $m_{rated} = 1.0$, $X_{Larm} = 0.2$ pu, $X_{TR}/S_{TR} = 0.1$ pu, $SCR = 3.0 \angle 80^\circ$, and $k_{vcfbBlk}$ in the range of [1.05 pu, 1.5 pu], $EoP_{FBphFlt}$ in the phase limb of mixed-SM HC-MMC under a pole-to-pole fault and the ac-current clearing time when blocking the converter at the positive peak of phase current are displayed in Fig. 6.11 and Fig. 6.12 with the transformer's turns ratio unchanged and proportionally changed with $(1+2k_{fm})$, respectively.

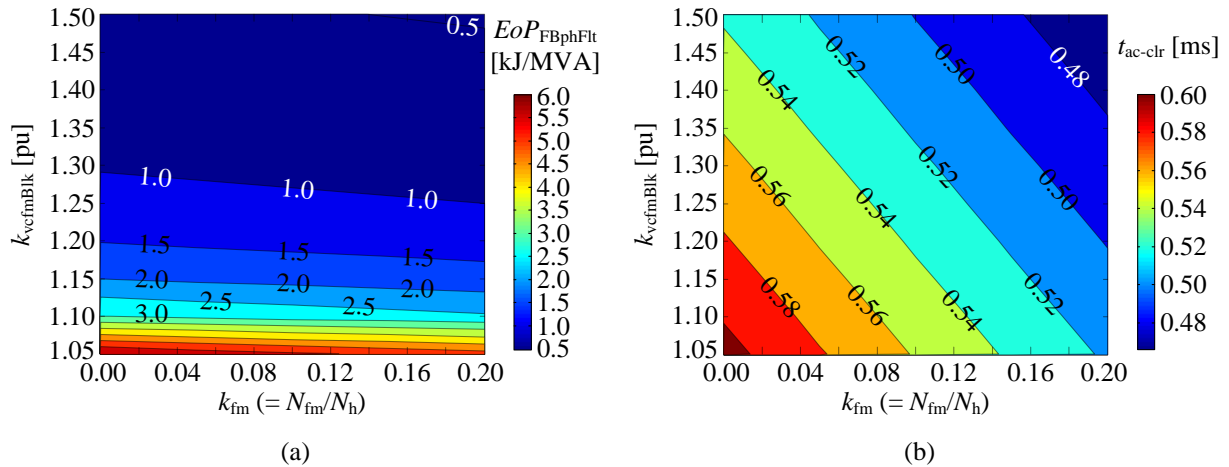


Fig. 6.11: Stored energy of all FB-SM capacitors in the phase limb of mixed-SM HC-MMC under a pole-to-pole fault per power rating unit and the ac-current clearing time with transformer's turns ratio unchanged and the converter blocked at the positive peak of phase current

(a) $EoP_{FBphFlt}$; (b) ac-current clearing time.

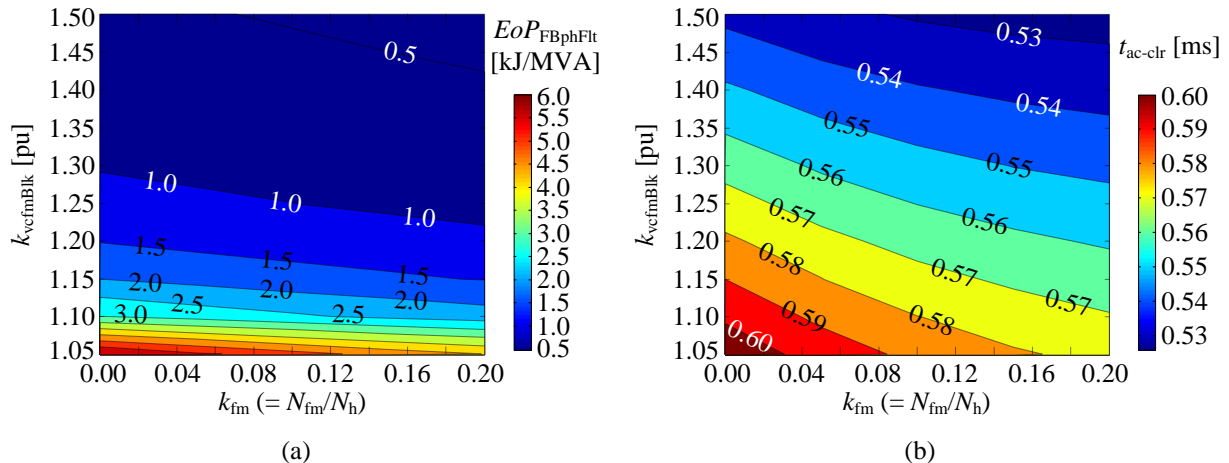


Fig. 6.12: Stored energy of all FB-SM capacitors in the phase limb of mixed-SM HC-MMC under a pole-to-pole fault per power rating unit and the ac-current clearing time with transformer's turns ratio proportionally changed with $(1+2k_{fm})$ and the converter blocked at the positive peak of phase current

(a) $EoP_{FBphFlt}$; (b) ac-current clearing time.

As seen from Fig. 6.11 (a) and Fig. 6.12 (a), EoP_{FBphFlt} is in the range of [0.5 kJ/MVA, 6.0 kJ/MVA] under the two considered cases of transformer's turns ratio, and it is increased when k_{vcfbBlk} decreases and experiences negligible changes under different k_{fm} . The ac-current clearing time is small (≤ 0.6 ms) for both cases of considered transformer's turns ratio. With k_{fm} or k_{vcfbBlk} increased, $t_{\text{ac-clr}}$ is slightly reduced for both cases of transformer's turns ratio. Overall, the change of k_{fm} has slight influence on EoP_{FBphFlt} of the mixed-SM HC-MMC. Therefore, EoP_{FBphFlt} and $t_{\text{ac-clr}}$ are evaluated with $k_{\text{fm}} = 0$ (i.e., original HC-MMC) to see its change with various SCR. With the system parameters of $f_o = 60$ Hz, $P_{\text{ref}} = 1.0$ pu, $m_{\text{rated}} = 1.0$, $X_{\text{Larm}} = 0.2$ pu, $X_{\text{TR}}/S_{\text{TR}} = 0.1$ pu, $k_{\text{vcfbFlt}} = 1.1$ pu, and $k_{\text{fm}} = 0$, Fig. 6.13 shows EoP_{FBphFlt} and the ac-current clearing time under various SCR. It is observed that with a various range of SCR, $t_{\text{ac-clr}}$ is small (≤ 0.8 ms), and EoP_{FBphFlt} is in a small range of [2.0 kJ/MVA, 4.0 kJ/MVA]. The angle of SCR has negligible influence on EoP_{FBphFlt} and $t_{\text{ac-clr}}$, and both EoP_{FBphFlt} and $t_{\text{ac-clr}}$ are slightly reduced with the magnitude of SCR increasing.

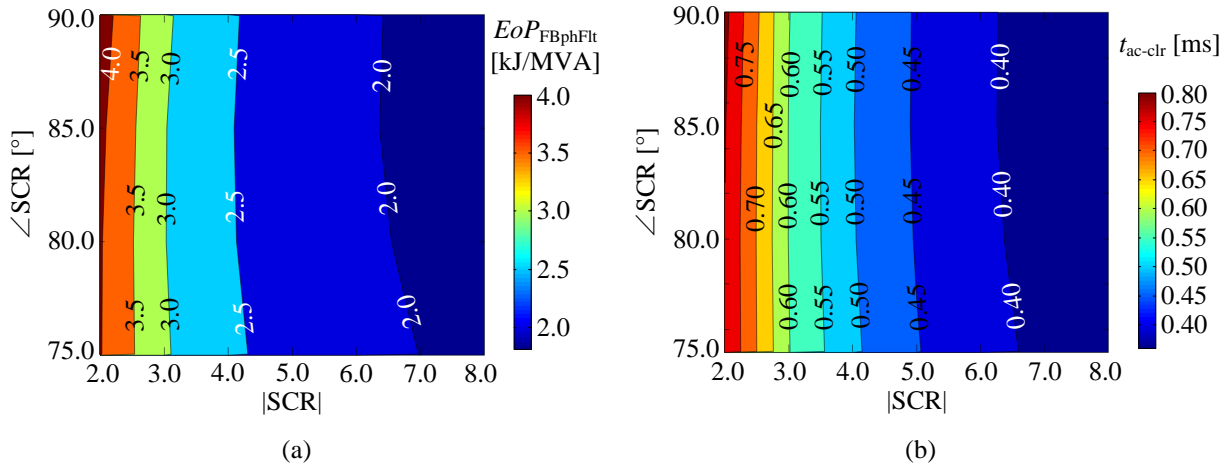


Fig. 6.13: Stored energy of all FB-SM capacitors in the phase limb of original HC-MMC under a pole-to-pole fault per power rating unit and the ac-current clearing time

(a) EoP_{FBphFlt} ; (b) ac-current clearing time.

Comparing EoP_{FBphFlt} in (6.33) under a pole-to-pole fault with EoP_{FBph} in (4.48) for normal operation, the maximum value is selected to ensure proper and safe operation for the FB SMs in

the phase limb. If the stored energy of all FB-SM capacitors per power rating unit is selected as a certain value (denoted as EoP_{FBph0}), the FB-SM capacitor voltage after blocking the dc fault is calculated as follows:

$$\begin{aligned}
k_{\text{veq}} &= \sqrt{1 + \frac{(L_{\text{arm}}/2 + L_{\text{s_con}} + L_{\text{TR}})}{C_{\text{eq}}} \left(\frac{\sqrt{2}I_{\text{con}} \sin(\theta_{\text{blk}} + \theta_{\text{icon}})}{(1 + m_{\text{eq}})V_{\text{dc}}/2} \right)^2} \\
&= \sqrt{1 + \frac{2X_0 \sin(\theta_{\text{blk}} + \theta_{\text{icon}})^2}{\omega_o (1 + m_{\text{eq}})^2 EoP_{\text{FBph0}}} \left[\frac{X_{\text{Larm}}}{2} + \frac{X_{\text{TR}}}{S_{\text{TR}}} + \frac{\text{Im}(\text{SCR})}{|\text{SCR}|^2} \right] \times 10^3} \quad (6.34) \\
k_{\text{vcfbBlk}} &= k_{\text{veq}} (1 + m_{\text{eq}}) - m_{\text{eq}}
\end{aligned}$$

As discussed in Section 4.3.3, EoP_{FBph} for normal operation is related to the switching frequency of the FB stack ($f_{\text{sw_fb}}$). Considering $27f_o$ switching frequency for the FB stack in the phase limb, EoP_{FBph} under normal operation is in range of [6.17 kJ/MVA, 6.86 kJ/MVA]. As seen from EoP_{FBphFlt} shown in Fig. 6.11, Fig. 6.12 and Fig. 6.13, the FB-SM capacitor voltage is increased to approximately 1.075 pu with $EoP_{\text{FBph}} = 6.0$ kJ/MVA. If the switching frequency for the FB stack changes, i.e., the stored energy requirement for the FB SMs in the phase limb under normal operation changes, the FB-SM capacitor voltage rise should be examined under dc faults.

6.3 Simulation validation and comparison

To validate the equivalent models, the system in Fig. 6.1 is simulated in PSCADTM/EMTDCTM. The system parameters of the original and mixed-SM HC-MMCs are given in Table 6.3. Both converters adopt PD-PWM and conventional sorting and rotating algorithms and they are controlled as inverters with CCSC. Compared with the original HC-MMC, the mixed-SM HC-MMC has additional 10 FB SMs per arm, and the transformer's turns ratio is increased to 1.2 times of that in the original HC-MMC. The PCC is controlled to be a PV bus using decoupled control.

Table 6.3: System parameters for simulated HC-MMCs

Power: 500 MW		AC system: 230 kV (L-L, RMS), 60 Hz		SCR = 3.0 \angle 80°	DC system: 500 kV, 1 kA
Parameter		Original HC-MMC		Mixed-SM HC-MMC	
Arm inductance		0.05 H		0.05 H	
SM cap. and number	Arm	2.5 mF and 100 (HB) ($EoP_{HBmain} = 37.5$ kJ/MVA)		1.5 mF and 100 (HB); 4.5 mF and 10 (FB) ($EoP_{HBmain} = 22.5$ kJ/MVA; $EoP_{FBmain} = 6.75$ kJ/MVA)	
	Limb	1.0 mF and 50 (FB) ($EoP_{FBph} = 3.75$ kJ/MVA)		1.0 mF and 50 (FB) ($EoP_{FBph} = 3.75$ kJ/MVA)	
Transformer	Rating	600 MVA; 6% leakage		600 MVA; 6% leakage	
	Ratio (con./sys.)	290 kV: 230 kV		348 kV: 230 kV	
Modulation method		PD-PWM; carrier frequency: 540 Hz (main stage) and 1620 Hz (phase limb)			
ON resistance		5.0 m Ω per semiconductor			
Nominal SM-capacitor voltage		5.0 kV per HB or FB SM			

(A) Case study of the original HC-MMC under a pole-to-pole dc fault

Under nominal conditions, the HC-MMC with parameters shown in Table 6.3 is simulated under pole-to-pole faults at different instants, where the blocking delay is set to 1 ms. The results for phase A variables using EMT simulations and equivalent models are shown in Fig. 6.14, where the upper- and lower-arm currents from modelling are calculated by the dc and ac circulating current models. As seen from Fig. 6.14 (a), after the dc fault and before blocking, the dc circulating current increases rapidly owing to the inserted HB SMs discharging, whereas the phase current flows as normal. After blocking, the phase current decays quickly (within ~ 0.4 ms), because all FB SMs in the phase limb are inserted to charge. Before the phase current starts decaying to zero, the potential of the shorted dc-terminals is approximately 83.0 kV ($\approx V_{dc}/6.0$) as analysed in (6.5). However, the dc fault takes much longer (~ 0.5 s calculated according to Table 6.1) to be cleared at the dc side. In the theoretical analysis, the SM capacitor voltage ripples are ignored to simplify the calculation of equivalent models. This has slight influence on the comparisons between theoretical and simulation results of FB-SM capacitor voltage in the phase limb, since the voltage ripple of

FB-SM capacitors in the phase limb is small during normal operation. However, this results in relatively large, but still acceptable, differences in the inserted HB-SM capacitor voltages between EMT simulations and equivalent models. To estimate the voltage drops, ignoring the voltage ripples is acceptable to simplify the calculations. Apart from the inserted HB-SM capacitor voltage, all the remaining waveforms from modelling show high accuracy.

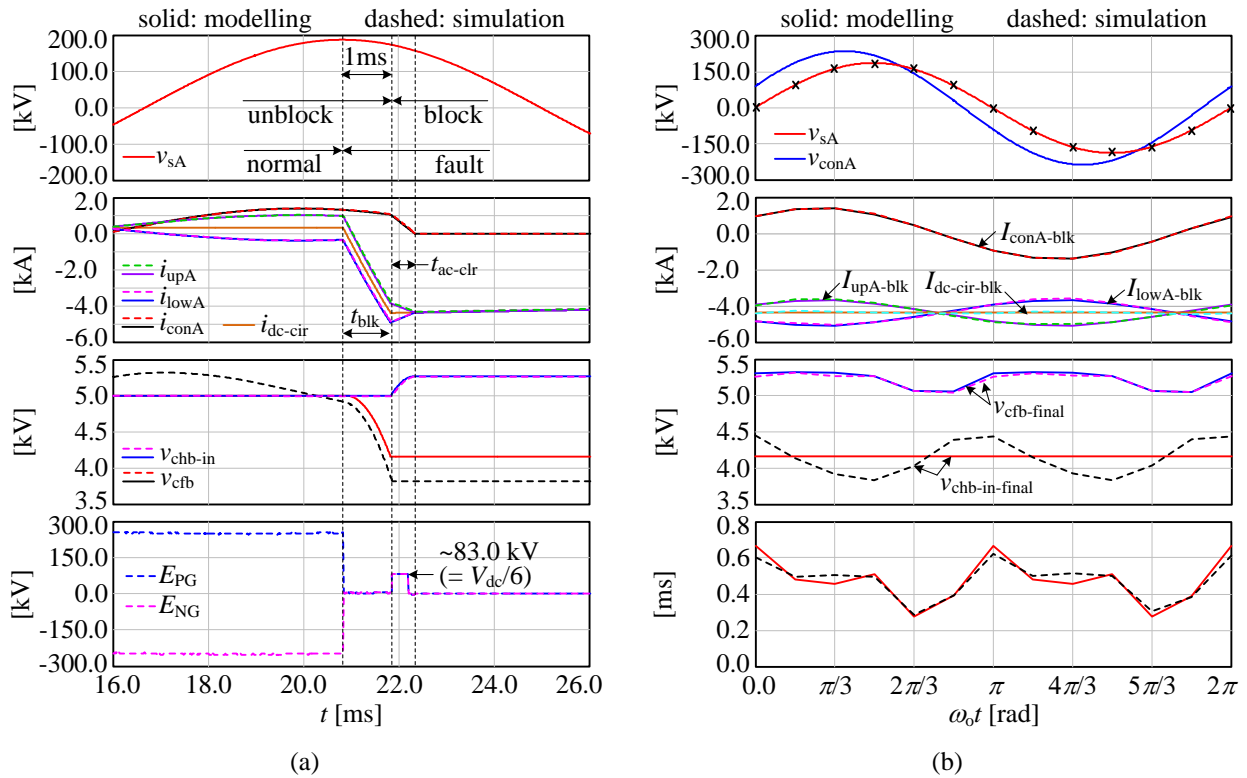


Fig. 6.14: Simulation results of the original HC-MMC under a pole-to-pole fault and nominal conditions (a) fault occurs at the instant of the positive peak of grid voltage; (b) fault occurs at different instants.

Fig. 6.14 (b) shows the currents upon blocking and the final SM capacitor voltages at different fault instants. It is observed that the final voltage of the inserted HB SMs obtained from modelling is slightly different from EMT simulations although the difference is small. Compared with the results obtained from EMT simulations, the currents upon blocking and the time to isolate the faulted dc and ac sides show high accuracy.

(B) Case study of mixed-SM HC-MMC under pole-to-pole fault

Similarly, the mixed-SM HC-MMC with parameters shown in Table 6.3 is simulated under nominal conditions with pole-to-pole faults applied at different instants. The blocking delay is set to 1 ms. Fig. 6.15 shows the results (for phase A) using EMT simulations and equivalent models.

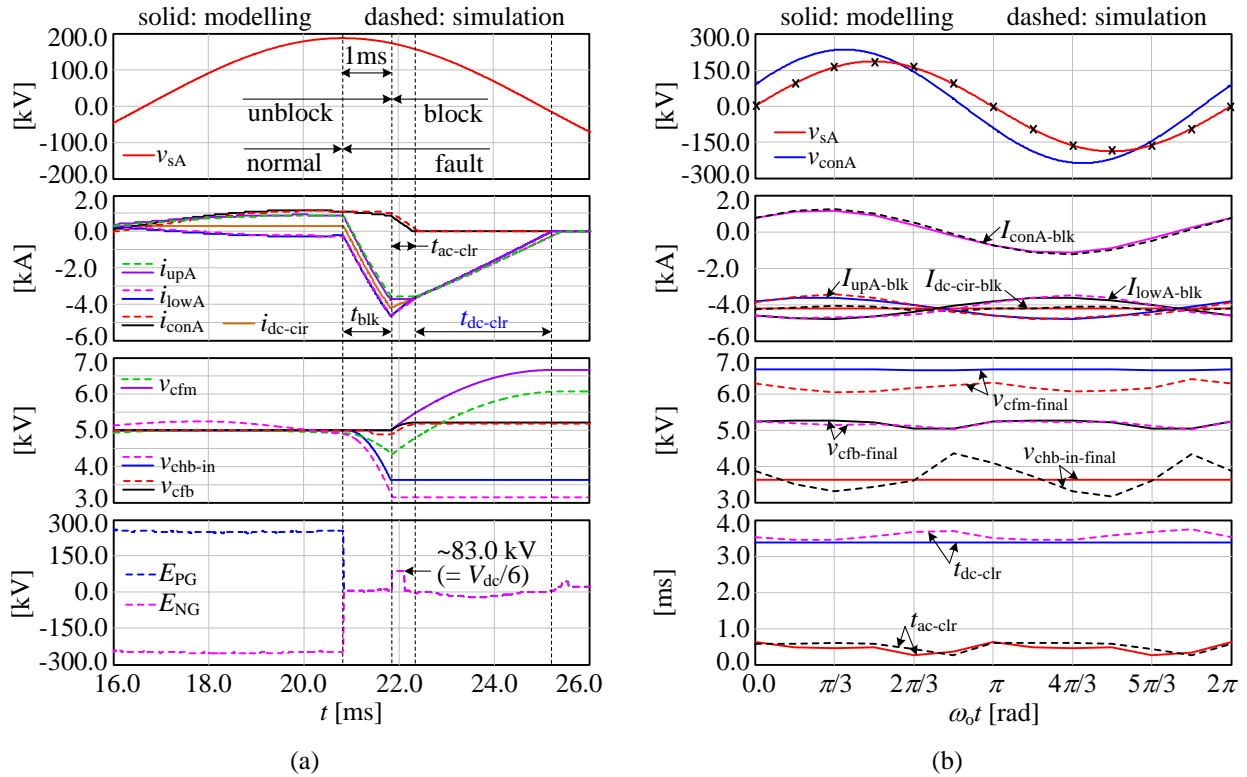


Fig. 6.15: Simulation results of mixed-SM HC-MMC under a pole-to-pole fault and nominal conditions (a) fault occurs at the instant of the positive peak of grid voltage; (b) fault occurs at different instants.

Fig. 6.15 (a) shows that the dc circulating current after the dc fault and before blocking and the ac circulating currents have similar performances with those of the original HC-MMC. After blocking and before the phase current decreasing to zero, the potential of the shorted dc terminals is approximately 83.0 kV ($\approx V_{dc}/6.0$) as analysed in (6.5). The difference between the original and mixed-SM HC-MMCs lies in the dc circulating current after blocking. Due to the existence of FB SMs in the main power stage, the dc-side fault current is rapidly decayed to zero (within ~ 3.5 ms), resulting in fast clearing of the dc fault at the expense of increased FB-SM capacitor voltages. The

loss analysis in Section 5.3 showed that the added FB SMs in the main power stage do not deteriorate system efficiency. Therefore, the mixed-SM HC-MMC is beneficial from the dc-fault performance perspective without adverse effects on efficiency. Ignoring SM capacitor voltage ripple and the assumption that only HB SMs discharge before blocking, which simplifies the modelling, have some effect on the SM capacitor voltage waveforms as seen in Fig. 6.15 (b); however, the effect is quite small. The current behaviour obtained from modelling shows high accuracy. The dc-fault clearing time and time to isolate the faulted dc and ac sides calculated by modelling are close to those in EMT simulations.

6.4 Summary and key contributions

The behavior of the original and mixed-SM HC-MMCs under a pole-to-pole fault was analyzed based upon equivalent models individually derived for the dc and ac circulating currents. The developed equivalent models were validated by EMT simulations of HC-MMCs under a pole-to-pole fault. Due to the existence of FB SMs in the phase limb, the ac circulating current is decayed quickly to zero after blocking the converter. Compared with the original HC-MMC, the mixed-SM HC-MMC with FB SMs in the main power stage showed superior performance in clearing dc-side fault current. Based upon the equivalent models of the original and mixed-SM HC-MMC, considerations for SM capacitance selection were analyzed to avoid adverse SM capacitor voltages under a pole-to-pole fault. Key observations for SM capacitor sizing are summarized as follows:

- The HB-SM capacitance in the main power stage of both the original and mixed-SM HC-MMCs can be selected based upon normal operation to ensure proper operation in normal and dc fault conditions;

- It is recommended to calculate the stored energy of SM capacitors per power rating unit based upon both the normal and dc fault conditions to select the larger value for FB-SM capacitance in the main power stage of the mixed-SM;
- Since the stored energy of FB-SM capacitors in the phase limb per power rating unit is related to the switching frequency for the FB stack, it is recommended to check the FB-SM capacitor voltage rise after selecting the FB-SM capacitance based upon normal operation;
- After selecting the SM capacitance based upon normal operation, it is recommended to double check the SM capacitor voltage variation under a dc fault.

Chapter 7

Specialized Control Algorithms for Unbalanced AC Faults

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Nowadays, VSCs are commonly used in high-voltage and high-power applications in ac grids, especially HVDC transmission systems. The ac system may encounter various faults as a result of which the protection system blocks the converters; it may take a long time to re-start the system. Therefore, a great deal of attention has been paid to ac-fault ride-through capability of advanced converters [91]-[93].

The general approach to control three-phase VSCs is the decoupled control based upon three-phase coordinate transformations [94]. However, the conventional decoupled control cannot work properly under imbalances, since the rotating reference-frame (dq) components exhibit double-line-frequency oscillations (see Fig. 7.1) and are unable to perform proper control without consideration of the 0 component, which is normally excluded in the decoupled control scheme. Due to the failure of the control system, unbalanced three-phase currents appear that contain

positive-, negative- and zero-sequence components. As the negative- and zero-sequence currents flow through an ac network and converter transformers, the system may experience increased heating as well as core saturation in the transformers. To achieve balanced phase currents under unbalanced ac faults, various methods have been proposed in the literature [95]-[98]. One popular method is to individually control the positive-, negative-, and zero-sequence components [95]-[96]. However, accurate extraction of sequence components and the design of various control loops are complicated. As such, individual phase control schemes have been proposed [97]-[98] attempting to simplify the controls under unbalanced conditions. Individual phase control structures were presented in [95] and [96]; however, these methods are unable to provide balanced grid currents and fast recovery under imbalances. A vector control method without sequence-component extraction was proposed in [54]. However, this control scheme is highly tied to the converter topology, which makes it difficult to be readily extended to other converter types.

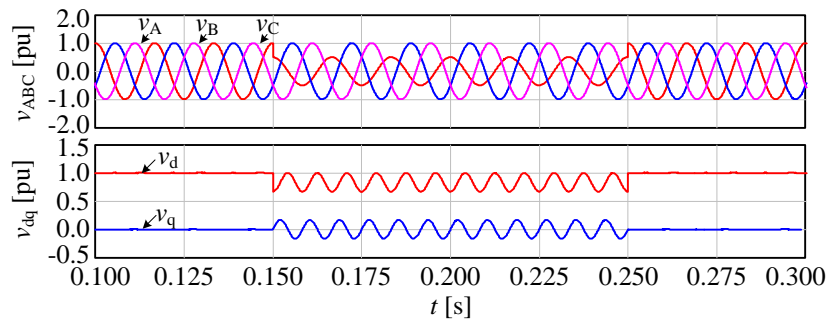


Fig. 7.1: Three-phase voltages with unbalanced variations and the dq components based upon three-phase coordinate transformations

This chapter presents a novel, generalized independent-phase control scheme suitable for various VSCs and capable of prompt recovery and operating the converter with balanced grid currents. The proposed independent-phase control comprises an outer loop and three independent current control loops. The outer loop is responsible for active power and ac voltage control and is shared among three phases, whereas the inner current control loops are used to control the system

to operate with balanced currents. Additionally, special algorithms are introduced and implemented to enable fast recovery.

The remainder of the chapter is organized as follows: Section 7.1 describes the preliminaries for three-phase VSCs based on individual phase control. Section 7.2 proposes a new improvement on the second-order generalized integrator (SOGI)-based PLL and the control architecture of the proposed generalized independent phase-current control. Validation of the proposed controller is conducted using detailed EMT simulations in Section 7.3.

7.1 Control preliminaries for independent-phase control

To implement independent-phase control for three-phase VSCs, basic techniques such as two-phase coordinate transformations and single-phase PLLs are utilized. These are briefly introduced in the following subsections.

7.1.1 Two-phase coordinate transformation

Two-phase coordinate transformations are those between two-phase static (2s) and two-phase rotating (2r) coordinate systems. Three types of common two-phase coordinate transformations are displayed in Fig. 7.2, where v_1 and qv_1 axes form the static coordinates; the synchronously rotating frame is composed of v_d and v_q axes; vector V is the rotating vector with an angular frequency of ω , and θ_{PLL} is the conversion angle. As the direction of rotation is from v_1 axis to qv_1 axis, signals on the qv_1 axis must be orthogonal and have a 90° phase delay relative to those on the v_1 axis.

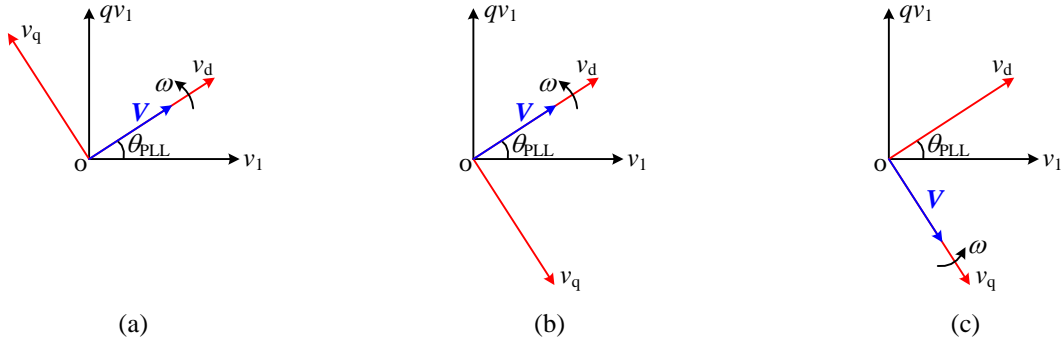


Fig. 7.2: Two-phase static and rotating coordinates

(a) type 1; (b) type 2; (c) type 3.

The transformation matrices for the coordinates shown in Fig. 7.2 are as follows:

$$\text{Type 1: } \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \\ -\sin \theta_{\text{PLL}} & \cos \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} \Leftrightarrow \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} = \begin{bmatrix} \cos \theta_{\text{PLL}} & -\sin \theta_{\text{PLL}} \\ \sin \theta_{\text{PLL}} & \cos \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (7.1)$$

$$\text{Type 2: } \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \\ \sin \theta_{\text{PLL}} & -\cos \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} \Leftrightarrow \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} = \begin{bmatrix} \cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \\ -\sin \theta_{\text{PLL}} & \cos \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (7.2)$$

$$\text{Type 3: } \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin \theta_{\text{PLL}} & -\cos \theta_{\text{PLL}} \\ \cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} \Leftrightarrow \begin{bmatrix} v_1 \\ qv_1 \end{bmatrix} = \begin{bmatrix} \sin \theta_{\text{PLL}} & \cos \theta_{\text{PLL}} \\ -\cos \theta_{\text{PLL}} & \sin \theta_{\text{PLL}} \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} \quad (7.3)$$

7.1.2 Single-phase PLL methods

Many robust and reliable single-phase PLL methods have been reported in the literature [99]-[101]. Based upon a two-phase transformation, most PLL methods achieve locking by adjusting the speed of the synchronously rotating frame, until the projections of the rotating vector to rotating frame become constants. When it is locked, one of the projections is zero and the other one presents the magnitude of the ac input. In order to use a two-phase transformation on a single-phase signal, an orthogonal system generation method is required, which is also the main difference among various single-phase PLL methods. Three commonly-used PLL methods, namely SOGI-based PLL [99], the delay-based PLL [100], and enhanced PLL (EPLL) [101], are introduced next. The

first two methods differ in the orthogonal system generation, whereas the last method is derived from the gradient descent method [101].

7.1.2.1 SOGI-based PLL

The diagram of an ideal SOGI is shown in Fig. 7.3, which generates two orthogonal signals (v_1 and qv_1) using a single input signal (v_{in}). The transfer functions from v_1 and qv_1 to v_{in} are expressed as follows:

$$H_d(s) = \frac{v_1(s)}{v_{in}(s)} = \frac{k_{\text{SOGI}}\omega_o s}{s^2 + k_{\text{SOGI}}\omega_o s + \omega_o^2} \quad (7.4)$$

$$H_q(s) = \frac{qv_1(s)}{v_{in}(s)} = \frac{k_{\text{SOGI}}\omega_o^2}{s^2 + k_{\text{SOGI}}\omega_o s + \omega_o^2} \quad (7.5)$$

where ω_o is the fundamental angular frequency of the input signal, and k_{SOGI} is the open-loop gain of the SOGI.

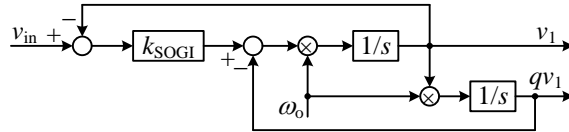


Fig. 7.3: Diagram of ideal SOGI

With $H_d(j\omega_o) = 1$ and $H_q(j\omega_o) = -1j$, it is easy to prove that signals v_1 and qv_1 have the same magnitude as the input signal, and v_1 is in phase with the input signal and qv_1 is 90° delayed. Since the ac grid may be polluted with low-frequency harmonics, the parameter k_{SOGI} can be adjusted to suppress low-frequency harmonics (e.g., 3rd) [99]. Fig. 7.4 shows the bode plots of $H_d(s)$ and $H_q(s)$ under different k_{SOGI} . It is seen that when k_{SOGI} decreases, $H_d(s)$ and $H_q(s)$ have smaller gains at the harmonic frequencies above the fundamental frequency. It indicates that SOGI method can provide a heavy filtering with a smaller k_{SOGI} . However, a small k_{SOGI} will lead to a slow dynamic

response. Therefore, trade-offs between the filtering ability and the dynamic response speed must be made to select a proper k_{SOGI} .

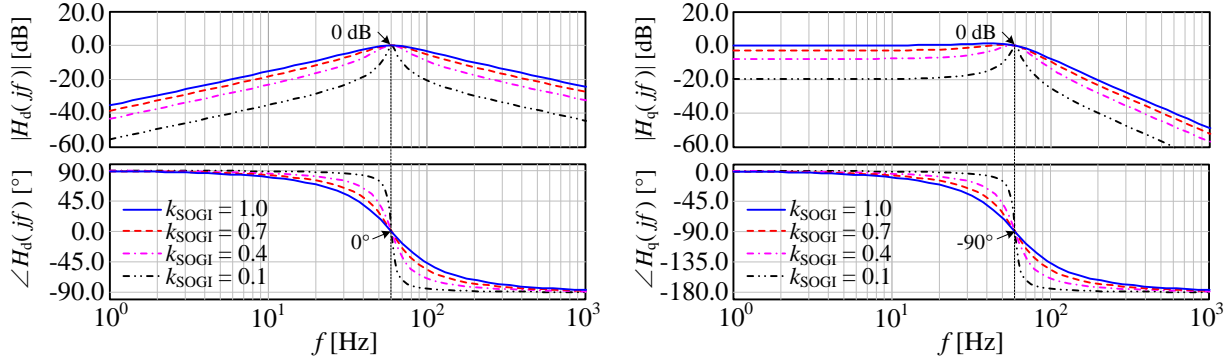


Fig. 7.4: Bode plots of $H_d(s)$ and $H_q(s)$ under different k_{SOGI}

The SOGI-based PLL is shown in Fig. 7.5, wherein the $2s/2r$ block denotes the transformation from static to rotating coordinates. Note that SOGI is independent of the phase tracking loop, which is beneficial to separately design the parameters for SOGI and the PI controller for PLL. To simplify the control system, v_q is controlled to be zero so that the vector \mathbf{V} overlaps entirely with the v_d axis, and the v_d component directly represents the magnitude of \mathbf{V} . Table 7.1 shows the specified signs in Fig. 7.5 for different coordinate types in Fig. 7.2.

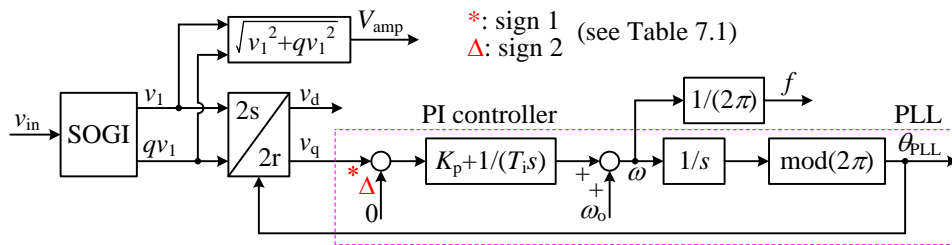


Fig. 7.5: Control diagram of single-phase SOGI-based PLL

Table 7.1: Specified signs for SOGI-based PLL in Fig. 7.5 under different coordinate types

2s/2r coordinate	sign 1 (*)	sign 2 (Δ)	v_{in} as function of
Type 1	+	-	$\cos(\theta_{\text{PLL}})$
Type 2	-	+	$\cos(\theta_{\text{PLL}})$
Type 3	+	-	$\sin(\theta_{\text{PLL}})$

Taking the second coordinate type in Fig. 7.2 (b) for PLL as an example, the input signal must be as cosine function of θ_{PLL} telling from the projection relationship of vector \mathbf{V} onto the v_1 -axis. Assuming the input signal is $v_{\text{in}} = V_{\text{amp}} \cdot \cos \theta_{\text{real}}$, where θ_{real} is the real phase angle of v_{in} , the signals v_1 (in phase with v_{in}) and qv_1 (90° delayed to v_{in}) obtained from SOGI are expressed as follows:

$$v_1 = v_{\text{in}} = V_{\text{amp}} \cos \theta_{\text{real}}, \quad qv_1 = V_{\text{amp}} \cos(\theta_{\text{real}} - \pi/2) = V_{\text{amp}} \sin \theta_{\text{real}} \quad (7.6)$$

Therefore, v_q can be simplified as

$$\begin{aligned} v_q &= v_1 \sin \theta_{\text{PLL}} - qv_1 \cos \theta_{\text{PLL}} = V_{\text{amp}} \cos \theta_{\text{real}} \sin \theta_{\text{PLL}} - V_{\text{amp}} \sin \theta_{\text{real}} \cos \theta_{\text{PLL}} \\ &= V_{\text{amp}} \sin(\theta_{\text{PLL}} - \theta_{\text{real}}) \end{aligned} \quad (7.7)$$

When $v_q > 0$ (i.e., $\theta_{\text{PLL}} > \theta_{\text{real}}$), the rotating coordinate must slow down its rotating speed, i.e., decreasing ω , and vice versa. Therefore, $(0 - v_q)$ should be used as the input of the PI controller. Similarly, the signs for phase tracking loop using the other two coordinate types can be derived.

7.1.2.2 Delay-based PLL

The control diagram of the delay-based PLL method is shown in Fig. 7.6, where T_o is the fundamental period of the input signal. The orthogonal components are obtained by introducing a delay of $T_o/4$ to the input signal. Compared with the SOGI-based PLL in Fig. 7.5, the delay-based PLL has the same control structure except for the generation of the two orthogonal signals.

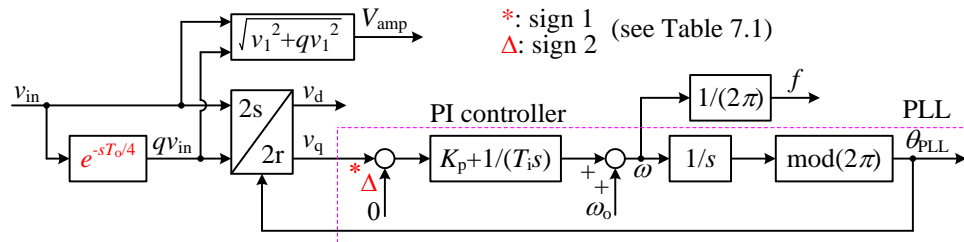


Fig. 7.6: Control diagram of single-phase delay-based PLL

7.1.2.3 Enhanced PLL (EPLL)

The control diagram of the EPLL is depicted in Fig. 7.7, where A_o and ω_o are the nominal amplitude and angular frequency, respectively. As seen the synchronizing and orthogonal signals are involved with the phase-tracking loop, which makes the control parameters k_1 , k_2 , and k_3 more complicated to tune.

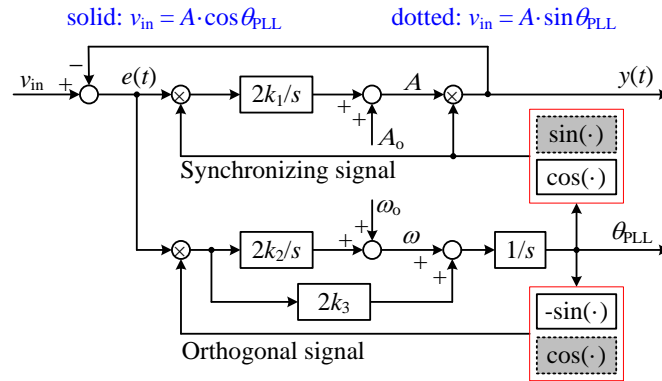


Fig. 7.7: Control diagram of single-phase EPLL

Compared with the single-phase EPLL, SOGI- and delay-based PLLs have less complexity in the design of control parameters. Since SOGI is capable of suppressing low-frequency harmonics, the SOGI-based PLL is more appealing than the delay-based PLL. However, one sampling time-step delay for v_1 and qv_1 may be introduced into the feedback loops in SOGI when discretised for digital implementation. This can lead to the signals generated by SOGI carrying inaccurate information of the input signal and thereafter influence the accuracy of magnitude estimation and the phase-tracking loop. Therefore, a novel improvement to the SOGI-based PLL will be proposed in the next section and its performance will be compared with that of the other two PLL methods.

7.2 Independent-phase current control for three-phase VSCs

To ride through ac faults, the proposed independent-phase current control is presented next. The SOGI-based PLL method will be improved first to obtain accurate magnitude estimation, which permits accurate and fast detection of the grid conditions.

7.2.1 Improved SOGI-based PLL method and performance evaluation

Fig. 7.8 depicts the two possible ways that one sampling time-step delay may be introduced. If qv_1 is calculated first, a one sampling time-step delay is introduced to calculate v_1 (see Fig. 7.8 (a)); if v_1 is calculated first, both v_1 and qv_1 will have one sampling time-step delay (see Fig. 7.8 (b)). The influence of this delay on the magnitude estimation and phase-tracking accuracy is analyzed next, and correction factors are proposed in the SOGI-based PLL to alleviate the influence caused by the involved delay.

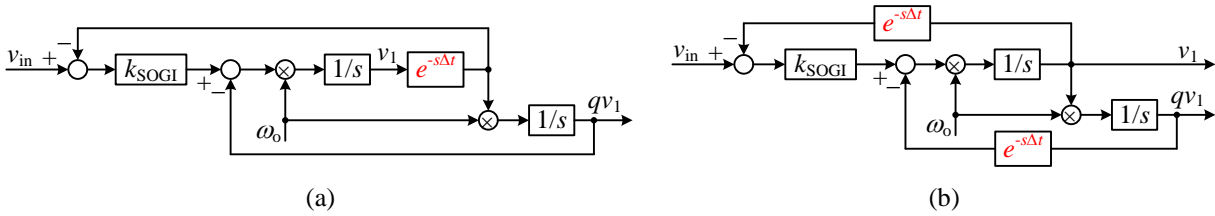


Fig. 7.8: Diagram of practical SOGI function

(a) SOGI diagram that updates qv_1 first and then v_1 ; (b) SOGI diagram that updates v_1 first and then qv_1 .

7.2.1.1 Improved SOGI-based PLL

It can be shown that both methods to implement SOGI shown in Fig. 7.8 result in the same transfer function of $v_1(s)/v_{in}(s)$, given as follows:

$$H'_d(s) = \frac{v_1(s)}{v_{in}(s)} = \frac{k_{SOGI}\omega_0 s}{s^2 + k_{SOGI}\omega_0 e^{-s\Delta t} s + \omega_0^2 e^{-s\Delta t}} \quad (7.8)$$

Let $s = j\omega$, v_1/v_{in} shown above is expressed as

$$\begin{aligned} \left. \frac{v_1}{v_{in}} \right|_{s=j\omega_o} &= \frac{jk_{\text{SOGI}}\omega_o^2}{(j\omega_o)^2 + jk_{\text{SOGI}}\omega_o^2 e^{-j\omega_o\Delta t} + \omega_o^2 e^{-j\omega_o\Delta t}} \\ &= \frac{jk_{\text{SOGI}}}{(\cos(\omega_o\Delta t) - 1 + k_{\text{SOGI}} \sin(\omega_o\Delta t)) + j(k_{\text{SOGI}} \cos(\omega_o\Delta t) - \sin(\omega_o\Delta t))} \end{aligned} \quad (7.9)$$

Since Δt is the sampling time-step and generally in the order of μs , $(\omega_o\Delta t)$ results in a small angle so that $\sin(\omega_o\Delta t) \approx \omega_o\Delta t$, and $\cos(\omega_o\Delta t) \approx 1.0 - (\omega_o\Delta t)^2/2$ (for magnitude calculation) and $\cos(\omega_o\Delta t) \approx 1.0$ (for phase calculation). Therefore, the relationships of magnitude and phase angle between v_{in} and v_1 at the fundamental frequency are shown in (7.10) and (7.11), respectively.

$$\begin{aligned} \left| \frac{v_{in}}{v_1} \right|_{s=j\omega_o} &= \frac{1}{k_{\text{SOGI}}} \sqrt{k_{\text{SOGI}}^2 + 2(1 - \cos(\omega_o\Delta t)) - 2k_{\text{SOGI}} \sin(\omega_o\Delta t)} \\ &\approx \frac{1}{k_{\text{SOGI}}} \sqrt{k_{\text{SOGI}}^2 + 2\left(1 - \left(1 - (\omega_o\Delta t)^2/2\right)\right) - 2k_{\text{SOGI}}\omega_o\Delta t} \\ &= \frac{|k_{\text{SOGI}} - \omega_o\Delta t|}{k_{\text{SOGI}}} < 1.0 \end{aligned} \quad (7.10)$$

$$\begin{aligned} \angle \frac{v_{in}}{v_1} \Big|_{s=j\omega_o} &= \angle v_{in} - \angle v_1 = -\tan^{-1} \left(\frac{\cos(\omega_o\Delta t) - 1 + k_{\text{SOGI}} \sin(\omega_o\Delta t)}{k_{\text{SOGI}} \cos(\omega_o\Delta t) - \sin(\omega_o\Delta t)} \right) \\ &\approx -\tan^{-1} \left(\frac{1 - 1 + k_{\text{SOGI}}\omega_o\Delta t}{k_{\text{SOGI}} - \omega_o\Delta t} \right) \approx -\frac{k_{\text{SOGI}}\omega_o\Delta t}{k_{\text{SOGI}} - \omega_o\Delta t} \end{aligned} \quad (7.11)$$

As seen from (7.10), the output signal v_1 has a larger magnitude than the input signal. To obtain an accurate magnitude from SOGI, the magnitude of the input signal is scaled down accordingly so that the output signal v_1 has the same magnitude as v_{in} . As seen from Fig. 7.5, the phase angle θ_{PLL} is directly locked to that of v_1 . However, signal v_1 has a phase shift with the input signal (see (7.11)). Therefore, the magnitude correction factor, k_{cf} , and phase correction factor, θ_{cf} , are introduced to improve the performance of the SOGI-based PLL, as shown in Fig. 7.9. The introduced factors are expressed as follows:

$$k_{cf} = \frac{|k_{SOGI} - \omega_o \Delta t|}{k_{SOGI}}, \quad \theta_{cf} = -\frac{k_{SOGI} \omega_o \Delta t}{k_{SOGI} - \omega_o \Delta t} \quad (7.12)$$

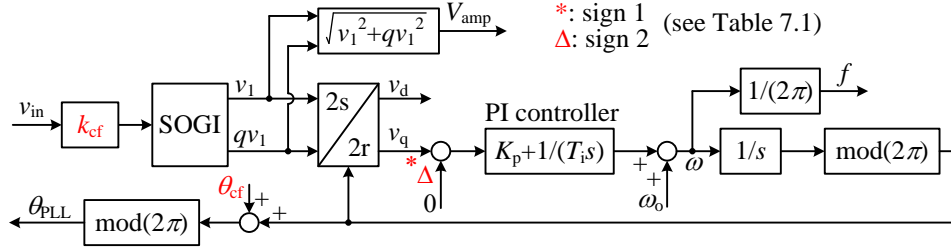


Fig. 7.9: Improved single-phase SOGI-based PLL

Magnitude estimation from SOGI for an input with unity peak and the phase corrector factor (θ_{cf}) under different k_{SOGI} and sampling time-steps are shown in Fig. 7.10. Without the magnitude correction, the voltage magnitude has significant difference with the actual value when a small k_{SOGI} and a large sampling time-step are used. However, the phase angle difference between the input signal v_{in} and the output signal v_1 is small with various k_{SOGI} . Therefore, with the correction factors used in the single-phase SOGI-based PLL, k_{SOGI} can be selected to be relatively small to suppress the influence of low-frequency harmonics on the phase-angle tracking and voltage magnitude estimation.

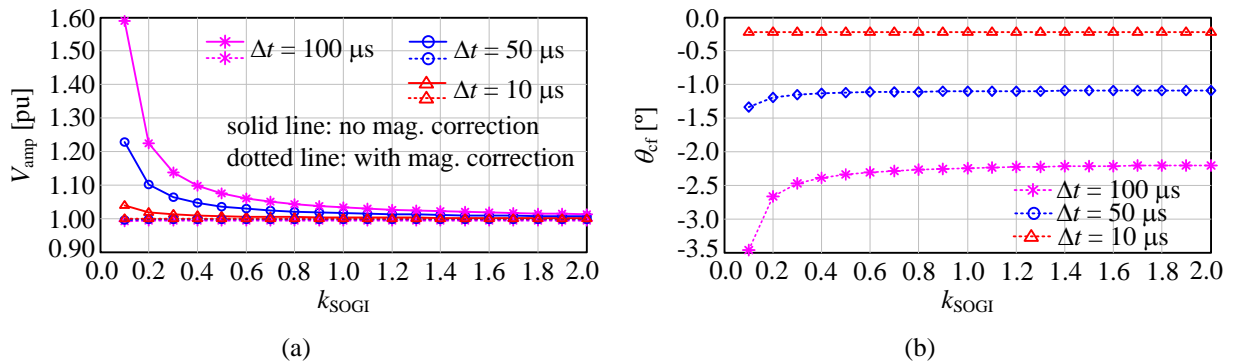


Fig. 7.10: Evaluation of correction factors used in the improved single-phase SOGI-based PLL under different k_{SOGI} and sampling time-steps

(a) estimation of voltage magnitude; (b) phase correction factor.

7.2.1.2 Performance evaluation

Comparisons among the three PLL methods with voltage magnitude change and with the 3rd harmonic present are shown in Fig. 7.11 (a) and (b), respectively, where $\Delta\theta = \theta_{\text{PLL}} - \theta_{\text{real}}$. The control parameters for each method are listed in Table 7.2, and the magnitude calculated by definition is expressed as follows:

$$V_{\text{amp-def}}(t) = \sqrt{2} \cdot \sqrt{\frac{1}{T_o} \int_{t-T_o}^t v_{\text{in}}(t)^2 dt} \quad (7.13)$$

Table 7.2: Control parameters for different PLL methods

PLL method	SOGI-based PLL	Delay-based PLL	EPLL
Control parameters	$k_{\text{SOGI}} = 0.6, K_p = 20.0, T_i = 0.001$	$K_p = 20.0, T_i = 0.001$	$k_1 = 120.0, k_2 = 100.0, k_3 = 100.0$

As seen from the subplots of V_{amp} in Fig. 7.11 (a) and (b), the improved SOGI and EPLL exhibit similar dynamic performance to obtain the fundamental magnitude close to the real value even with 3rd harmonic present. However, the magnitude obtained by the delay method experiences large variations when the input has 3rd harmonic. Nevertheless, it also has large variations during transients even with a purely sinusoidal input. This is caused by its incapability of suppressing low-frequency harmonics. The magnitude calculated from (7.13) does not match the fundamental magnitude when low-frequency harmonics are present. From the subplots of $\Delta\theta$ in Fig. 7.11 (a) and (b), it is observed that the improved SOGI-based PLL has similar dynamic performance with EPLL under a purely sinusoidal input, whereas improved SOGI-based PLL has smaller phase-tracking variations than EPLL with 3rd harmonic present. Overall, the improved SOG-based PLL shows better performance in phase-tracking control and magnitude estimation. Therefore, the improved SOGI-based PLL is used in the proposed independent-phase control method, which is introduced in the following subsections.

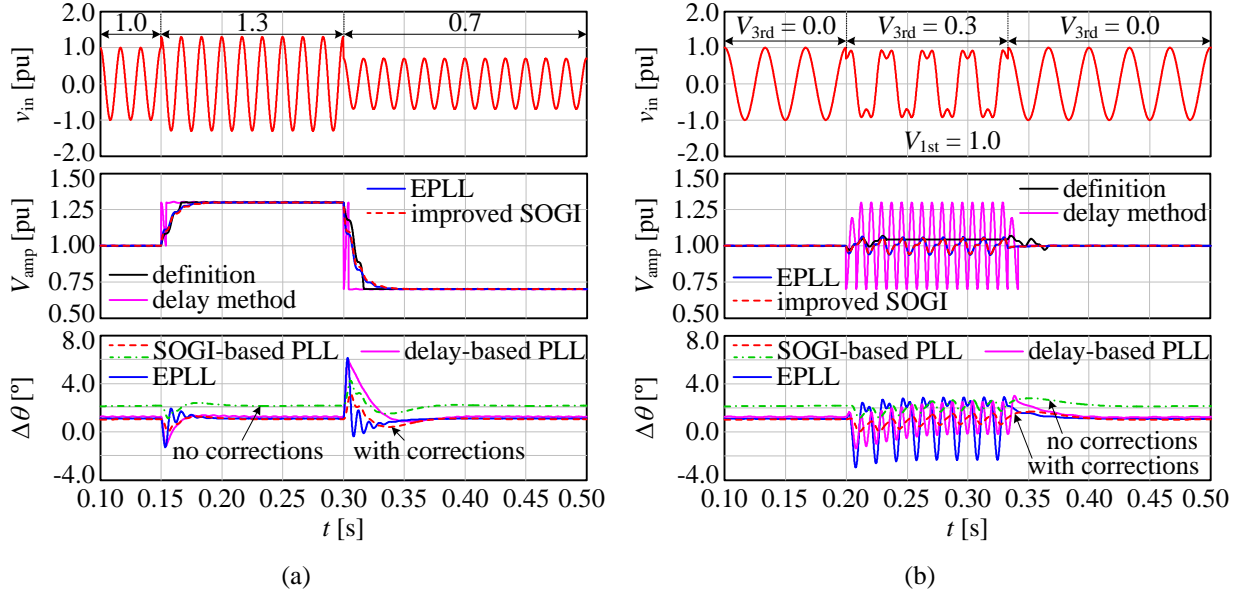


Fig. 7.11: Performance comparisons of three PLL methods with $\Delta t = 50 \mu s$
(a) with the change in the input voltage magnitude; (b) with 3rd harmonic present.

7.2.2 Proposed independent-phase current control

A new independent-phase current control strategy that enables three-phase VSCs to operate and produce balanced ac currents under unbalanced grid conditions, and without sequence component extraction, is introduced in the following subsections.

7.2.2.1 Control architecture

The schematic diagram of the proposed independent-phase current control is shown in Fig. 7.12. It is composed of a master control and independent-phase current controls. The master control receives the references of active power (P_{ref0}) and phase-voltage magnitude (V_{acref0}) and is responsible to provide reference currents (i_{sAref} , i_{sBref} , and i_{sCref}) to the three phase-current control loops. Each phase-current control sends back its real power (P_{sA} , P_{sB} , and P_{sC}), phase voltage magnitude (v_{sApk} , v_{sBpk} , and v_{sCpk}) and phase-tracking angle (θ_{A0} , θ_{B0} , and θ_{C0}) to the master control.

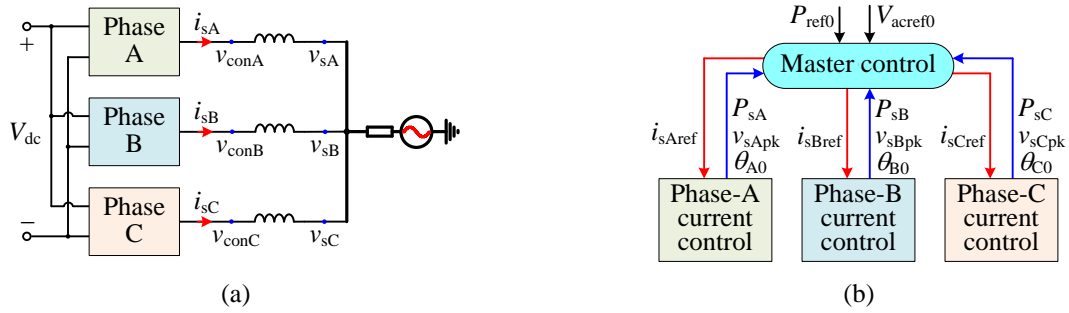


Fig. 7.12: Independent-phase control for a three-phase VSC

(a) typical topology of a three-phase VSC; (b) high-level view of the proposed independent-phase control.

The detailed diagrams of the master control and phase-A current control are shown in Fig. 7.13 (a) and (b), respectively. Since the three phase-current controls in Fig. 7.12 (b) are similar, only phase-A current control is depicted for brevity. As seen from Fig. 7.13 (a), the system status detection block detects the grid's status based upon the three phase-voltage magnitudes (v_{sApk} , v_{sBpk} , and v_{sCpk}), and sends out two flags (StatusFlag and PhFlag). According to PhFlag, the magnitude feedback to the voltage-magnitude control loop (v_{ac-pk}) is selected and the phase angle for phase A is calculated. The actual reference for the active-power control loop (P_{ref}) is modified according to the system status (StatusFlag and three-phase voltage magnitudes) and its original references P_{ref0} and V_{acref0} . The three-phase current references (i_{sAref} , i_{sBref} , and i_{sCref}) are determined by the outputs of control loops for active power and voltage magnitude (i_{dref} and i_{qref}), and the phase-A angle (θ_A). Since the three-phase currents are intended to be balanced even under imbalances, the symmetrical three-phase currents can be obtained by a three-phase coordinate transformation with phase-A angle (θ_A). As seen from the phase-current control loop shown in Fig. 7.13 (b), the improved SOGI-based PLL is utilized to obtain the phase-A angle (θ_{A0}) and voltage magnitude (v_{sApk}). The active power (P_{sA}) is calculated as $v_{sA} \cdot i_{sA}$ followed by a notch filter to remove the 2nd harmonic. A proportional-resonant (PR) controller is adopted to track the sinusoidal reference, and its expression is shown as follows:

$$G_{PR}(s) = K_p + \frac{2K_r \omega_{PRC} s}{s^2 + 2\omega_{PRC} s + \omega_o^2} \quad (7.14)$$

where K_p and K_r are the coefficients of PR controller, and ω_{PRC} is the cut-off frequency at -3 dB bandwidth.

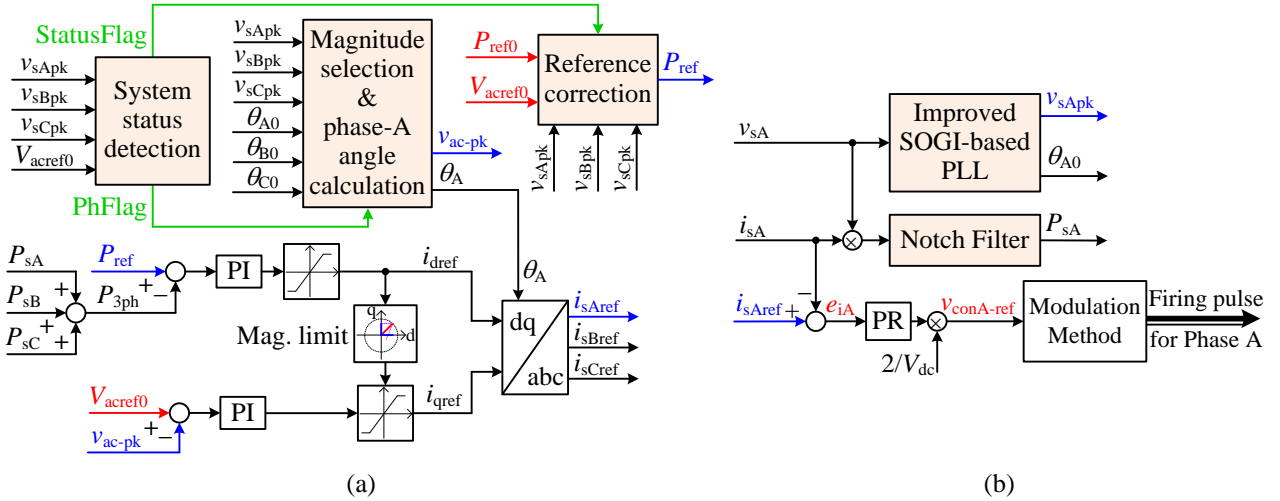


Fig. 7.13: Independent-phase current control for a three-phase VSC
(a) master control; (b) current control of phase A.

The types of system faults considered in this thesis include phase voltage sags, phase-to-ground (phase-to-G) faults, and line-to-line (L-to-L) faults. Fig. 7.14 illustrates the flowcharts of system status detection, magnitude selection and phase-A angle calculation, and reference correction used in the master control loop (see Fig. 7.13 (a)). Fig. 7.14 (a) shows that the system status is identified as balanced with three phase voltages at nominal values ($StatusFlag = 0$), the status of only one L-to-L fault ($StatusFlag = 1$) and the status of all the other types of faults including phase-to-G faults and phase voltage sags ($StatusFlag = 2$). Additionally, the status of $PhFlag$ is utilized to identify the phase that has the minimum error among the three phase-voltage magnitudes and the pre-set reference of ac voltage magnitude (V_{acref0}). Fig. 7.14 (b) illustrates that the phase-A angle and the feedback voltage magnitude to the ac voltage control loop are selected based upon $PhFlag$, which

indicates the phase that has the closest voltage magnitude to the voltage-magnitude reference is selected. Therefore, the system delivers minimum reactive power, i.e., the minimum i_{qref} in Fig. 7.13 (a), so that it has better capability to deliver active power under unbalanced ac faults.

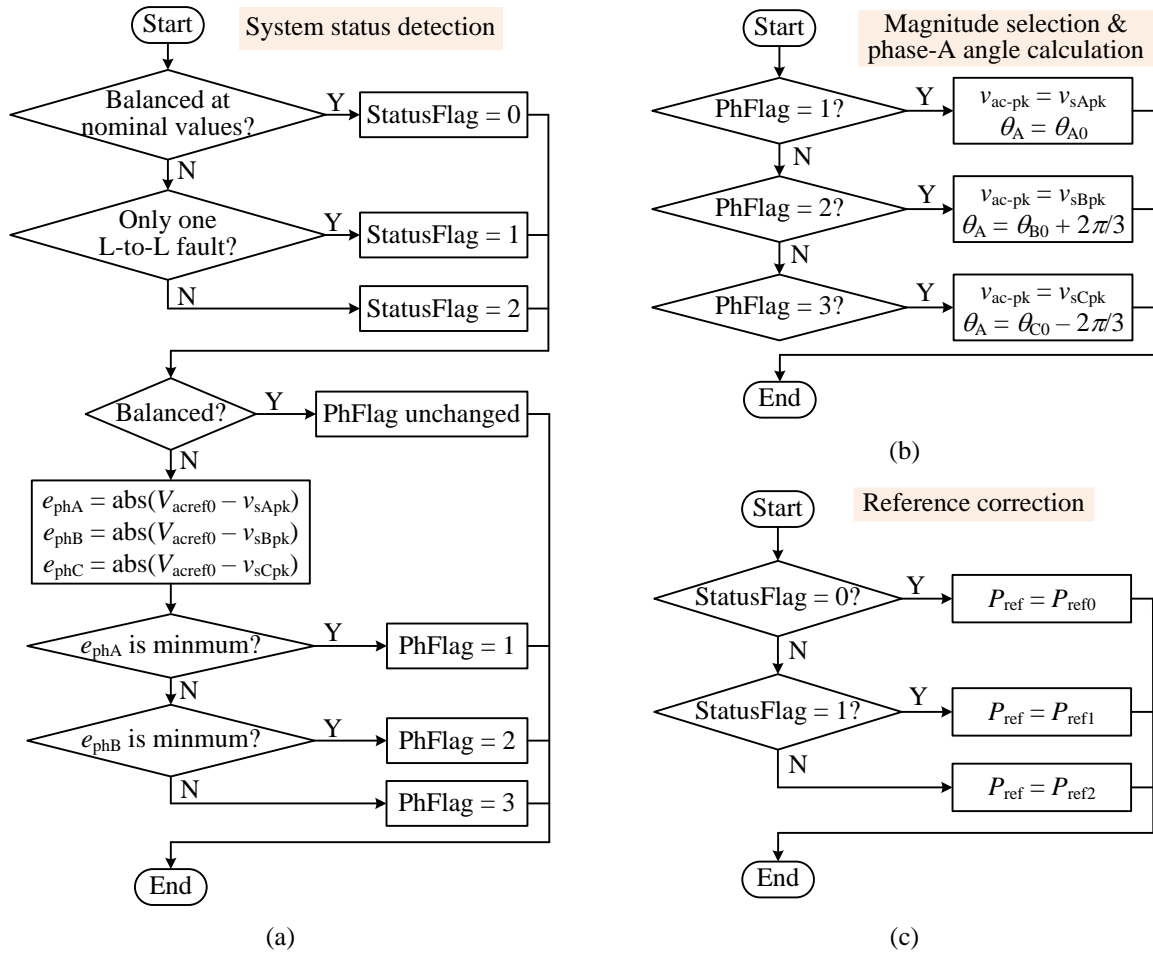


Fig. 7.14: Flowcharts of three functions in the master control

(a) system status detection; (b) magnitude selection and phase-A angle calculation; (c) reference correction.

Fig. 7.14 (c) shows the reference correction of the actual active-power reference (P_{ref}). In order to quickly operate the system in steady state after recovery from ac faults or voltage sags, the current reference i_{dref} from the active-power control loop (see Fig. 7.13 (a)) is preferred to not change drastically. To meet this requirement, the active-power order is strategically selected as the phase-voltage magnitudes change. Under balanced conditions, the rotating voltage and current

vectors related to three phase voltages and currents are shown in Fig. 7.15 (a), where $v_A/v_B/v_C$ and $qv_A/qv_B/qv_C$ form the static coordinate for three phase voltages, and the rotating coordinates for phase A, B, and C are composed of d_A and q_A , d_B and q_B , and d_C and q_C , respectively. Since the three phase voltages and currents are symmetrical, the rotating voltage vectors \mathbf{V}_A , \mathbf{V}_B , and \mathbf{V}_C have equal magnitudes and phase angles of 120° apart, and so do the three phase currents \mathbf{I}_A , \mathbf{I}_B , and \mathbf{I}_C . The three phase active powers calculated by the dq components of phase current and voltage are expressed as follows:

$$P_j = (v_{jd} \cdot i_{jd} + v_{jq} \cdot i_{jq})/2, \text{ where } j = A, B \text{ or } C \quad (7.15)$$

Under balanced operations, the following conditions hold: $v_{Ad} = v_{Bd} = v_{Cd} = V_{\text{amp}}$, $v_{Aq} = v_{Bq} = v_{Cq} = 0$, $i_{Ad} = i_{Bd} = i_{Cd} = I_d$, and $i_{Aq} = i_{Bq} = i_{Cq} = I_q$. As such, $P_A = P_B = P_C = (V_{\text{amp}} \cdot I_d)/2$ and $P_{3\text{ph}} = P_A + P_B + P_C = (3V_{\text{amp}} \cdot I_d)/2$. However, when the ac system encounters a single L-to-L fault, the delivered power must be decreased to prevent i_{dref} from changing excessively. Fig. 7.15 (b) illustrates the relationship between rotating vectors under a phase-B-to-C fault. To satisfy KVL, the three phase voltages must meet $v_B(t) = v_C(t) = -v_A(t)/2$ so that $\mathbf{V}_B = \mathbf{V}_C = -\mathbf{V}_A/2$ as shown in Fig. 7.15 (b). Based upon the function of magnitude selection and phase-A angle calculation shown in Fig. 7.14 (b), phase A is selected as the base phase angle and the other two phase-angles are derived from it with corresponding 120° phase shifts. Therefore, the three dq rotating reference frames still have phase angles of 120° apart, which is similar to the balanced conditions shown in Fig. 7.15 (a). The projections of \mathbf{V}_B and \mathbf{V}_C onto their own rotating reference frames are

$$\begin{aligned} v_{Bd} &= (v_{Ad}/2) \cdot \cos 60^\circ = v_{Ad}/4 = V_{\text{amp}}/4, & v_{Bq} &= -(v_{Ad}/2) \cdot \sin 60^\circ = -\sqrt{3}V_{\text{amp}}/4 \\ v_{Cd} &= (v_{Ad}/2) \cdot \cos 60^\circ = V_{\text{amp}}/4, & v_{Cq} &= (v_{Ad}/2) \cdot \sin 60^\circ = \sqrt{3}V_{\text{amp}}/4 \end{aligned} \quad (7.16)$$

Therefore, considering approximately unchanged current vectors from balanced operation, the three phase active powers calculated by relevant dq components are expressed as follows:

$$\begin{aligned}
P_A &= (v_{Ad} \cdot i_{Ad} + v_{Aq} \cdot i_{Aq})/2 = V_{\text{amp}} I_d / 2 \\
P_B &= (v_{Bd} \cdot i_{Bd} + v_{Bq} \cdot i_{Bq})/2 = \left[(V_{\text{amp}}/4) \cdot I_d - (\sqrt{3}V_{\text{amp}}/4) \cdot I_q \right] / 2 \\
P_C &= (v_{Cd} \cdot i_{Cd} + v_{Cq} \cdot i_{Cq})/2 = \left[(V_{\text{amp}}/4) \cdot I_d + (\sqrt{3}V_{\text{amp}}/4) \cdot I_q \right] / 2
\end{aligned} \tag{7.17}$$

The total active power of the faulted phases B and C is

$$P_{L\text{-to-L}} = P_B + P_C = V_{\text{amp}} I_d / 4 \tag{7.18}$$

Compared with the total active power calculated under balanced operation, i.e., $P_{3\text{ph}} = (3V_{\text{amp}} \cdot I_d)/2$, only 1/6 of the active power can be delivered for the two phases with a L-to-L fault if the three-phase symmetrical currents are the same to those under balanced operation. Considering that each phase voltage may encounter voltage sags, the active power references under a single L-to-L fault (StatusFlag = 1) and other faults or voltage sags (Status Flag = 2) are respectively denoted as P_{ref1} and P_{ref2} and expressed as follows:

$$P_{\text{ref1}} = \frac{P_{\text{ref0}}}{6} + \frac{P_{\text{ref0}}}{3} \frac{v_{sApk} + v_{sBpk} + v_{sCpk} - 1.0}{V_{\text{acref0}}} \tag{7.19}$$

$$P_{\text{ref2}} = P_{\text{ref0}} \cdot \frac{v_{sApk} + v_{sBpk} + v_{sCpk}}{3V_{\text{acref0}}} \tag{7.20}$$

If there is only a single L-to-L fault and the remaining phase does not experience any sags or faults,

$$P_{\text{ref1}} = P_{\text{ref0}}/2.$$

As seen from above introduction of the proposed control scheme, it is concluded that this scheme does not need extraction of sequence components, and controls the converter's operation

with balanced ac currents under both balanced and unbalanced conditions. In addition, the proposed approach can help the system to quickly recover to steady state with special control algorithms (e.g., the functions of the magnitude selection and the reference correction) under various ac faults and voltage sags. To validate the proposed control scheme, simulation-based case studies will be conducted in the next section. However, practical systems may have different requirements on ac-fault ride-through capability, such as support of PCC voltage in the faulted ac grid. Under this circumstance, the feedback signal of v_{ac-pk} and reference signals of P_{ref} and V_{acref} (see Fig. 7.13 (a)) should be modified differently from the presented algorithm. This investigation is proposed as future work in Section 8.2.

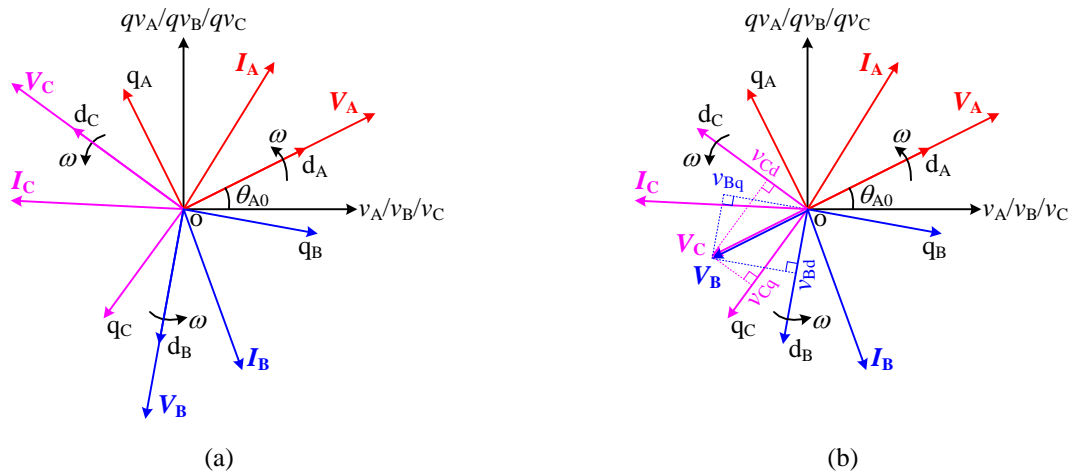


Fig. 7.15: Two-phase transformations for three phases
(a) balanced ac systems; (b) single L-to-L fault (B-to-C fault).

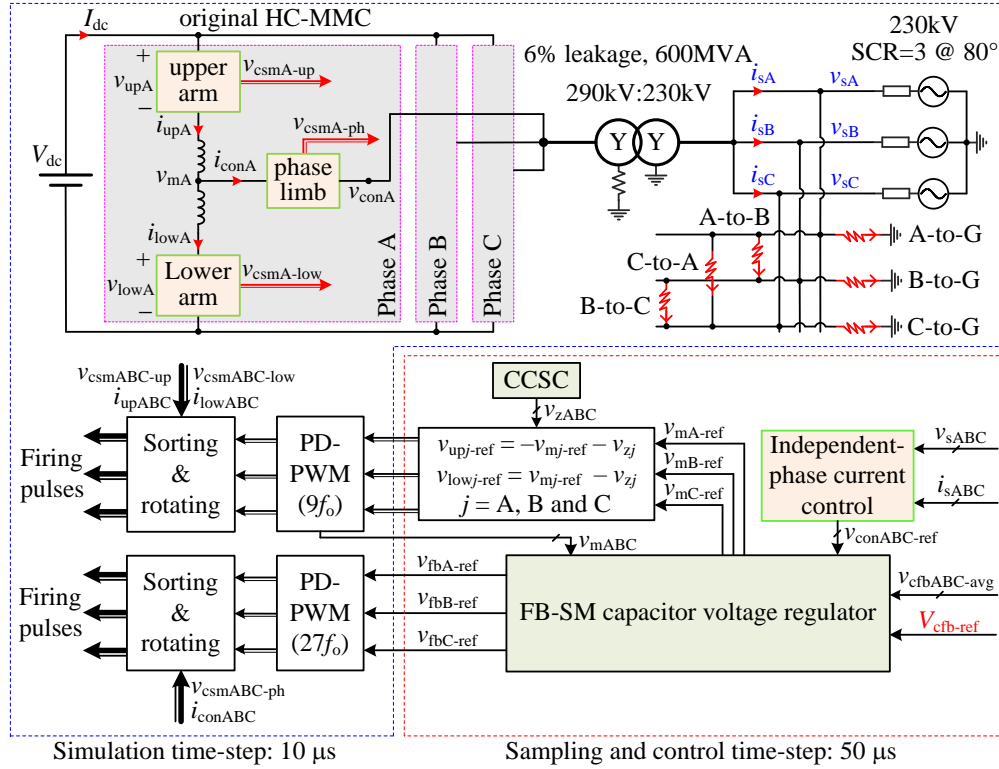
7.3 Simulation validation of the proposed control

Extensive EMT simulation studies in PSCADTM/EMTDCTM are conducted for a 500-MW, 500-kV (dc) original HC-MMC connected to a 230-kV/60-Hz ac system and operating as an inverter. This converter has 100 HB SMs per arm in the main power stage and 50 FB SMs in the phase limb. The HB- and FB-SM capacitances are selected as 5.0 mF and 1.0 mF, respectively;

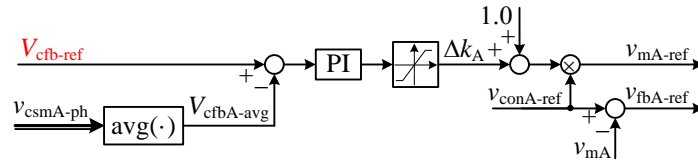
the arm inductance is selected as 0.05H, which is 17.5% (recommended range is 10%~20% [102]) of the system base impedance. Other system specifications are shown in Fig. 7.16 (a), wherein the diagram of the independent-phase current control is shown in Fig. 7.13. The HB- and FB-SM capacitor voltage balancing is achieved using the conventional sorting and rotating method, whereas the FB-SM capacitor voltage value is regulated with additional supervision as shown in Fig. 7.16 (b). Note that the implementation of the FB-SM capacitor voltage regulator is different from that shown in Fig. 3.2 (d), since there is no explicit information of modulation index in the control loop shown in Fig. 7.13 (b). As such, the control signal from the FB-SM capacitor voltage regulator is used as the magnification coefficient for the modulating signal obtained from independent phase-current control, e.g., $(1+\Delta k_A) \cdot v_{\text{conA-ref}}$ for phase A. To alleviate the influence of circulating currents under unbalanced grid conditions, CCSC is adopted to provide the references of v_{zA} , v_{zB} , and v_{zC} . The control diagram of CCSC for phase A is shown in Fig. 7.16 (c), where the dc-current reference is determined by the converter's real power of the corresponding phase. The actual references for upper and lower arms are as follows:

$$\begin{aligned} v_{\text{up}j\text{-ref}} &= -v_{\text{mj-ref}} - v_{zj} \\ v_{\text{low}j\text{-ref}} &= v_{\text{mj-ref}} - v_{zj} \end{aligned} \quad \text{where } j = \text{A, B and C} \quad (7.21)$$

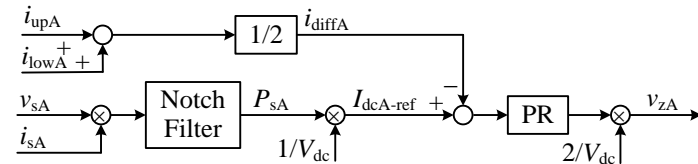
To closely emulate the actual implementation of the studied system, the time-step for voltage and current sampling and control system is set as 50 μs , whereas the time-step for the system modulation and network solution is set as 10 μs . This is based upon the notion that control signals and digital controllers use a finite sampling time (in this case using 50 μs), whereas the physical system is a continuous time one (represented here with a fine sampling time of 10 μs). Since a phase-to-ground fault is the worst-case scenario of the phase voltage sag, only the phase-to-ground faults and line-to-line faults with low impedance are investigated.



(a)



(b)



(c)

Fig. 7.16: Simulation system and controls for original HC-MMC

(a) HC-MMC system and controls; (b) control diagram of FB-SM capacitor voltage regulator for phase A; (c) control diagram of CCSC for phase A.

7.3.1 Simulation of phase-A-to-G fault

7.3.1.1 SM capacitor voltage balancing issue

The operating waveforms of the original HC-MMC under a phase-A-to-G fault are shown in Fig. 7.17. The fault occurs at $t = 1.55$ s and is cleared at $t = 1.70$ s, with a fault detection delay of

approximately 5.0 ms. As proposed, StatusFlag is determined by three-phase ac voltage magnitudes, and PhFlag is determined by the phase that has the closest voltage magnitude to the reference of ac voltage magnitude ($V_{ac-ref0}$), which is clearly shown in Fig. 7.14 (a). As seen from Fig. 7.17 (a), StatusFlag changes from 0 (i.e., system is balanced at nominal condition) to 2 (i.e., system encounters ac fault except single L-to-L fault), and PhFlag changes from 1 (i.e., phase A) to 2 (i.e., phase B). The feedback ac-voltage magnitude (v_{ac-pk}) shown in Fig. 7.13 (a) is selected based upon PhFlag and its value is determined by phase-A and phase-B voltage magnitudes before and after the ac fault is detected, respectively. The three-phase real power is decreased to about $330.0 \text{ MW} \approx 500\text{MW} \times (1.0 \text{ pu} + 1.0 \text{ pu}) / 3.0$ during the fault, which is well matched with the reference correction shown in (7.20).

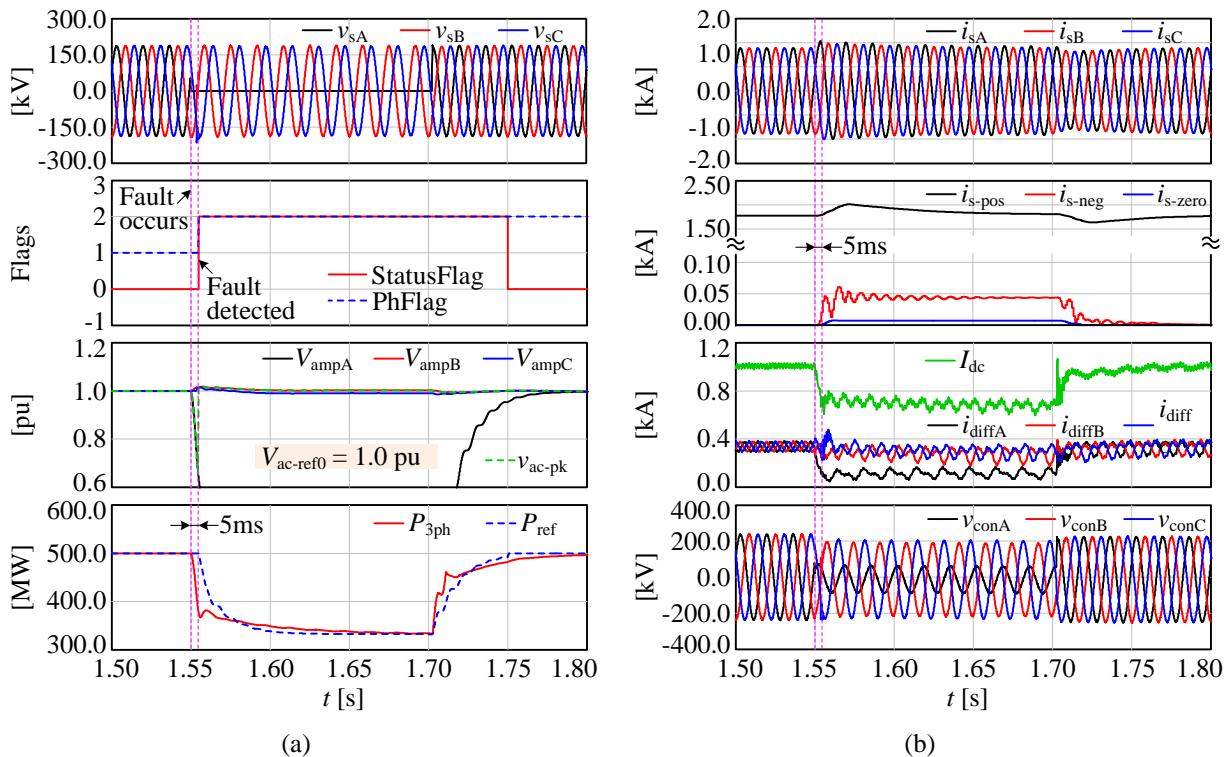


Fig. 7.17: Operation of HC-MMC under a phase-A-to-G fault with the proposed independent phase-current control (a) three-phase grid voltages, status and phase flags, three-phase grid voltage amplitudes and feedback signal, and real power and its reference; (b) three-phase grid currents and their sequence components, dc-circulating currents and dc-side current, and three-phase converter-side voltage.

As seen from Fig. 7.17 (b), during the ac fault, the three-phase grid currents, i_{sABC} , are well balanced and ride through the fault smoothly. The circulating current in arms of phase A is decreased, as the real power delivered by phase A is reduced due to the ground fault. To explicitly show the balanced nature of the line currents, their sequence components are analyzed and shown in the 2nd subplot of Fig. 7.17 (b). The negative- and zero-sequence magnitudes are ~ 40.0 A and ~ 7.0 A, respectively, resulting in 2.0% and 0.35% of the positive-sequence component (~ 2.0 kA).

Fig. 7.20 (a) shows the average HB- and FB-SM capacitor voltages and the dc components of three-phase converter voltages under the above ac fault. It is seen that the FB-SM capacitor voltages are regulated well at the nominal value (5.0 kV) before, during, and after the ac fault. The HB-SM capacitor voltages are well balanced before the fault but exhibit a small dc offset between the average HB-SM capacitor voltages of upper and lower arms during and after the fault. This dc offset is gradually decreased as time lapses, and so do the dc offsets of converter phase voltages.

Assuming that the dc component of the circulating current through phase A arms is I_{dcA} , phase A deals with the real power of $P_{conA} = V_{dc} \cdot I_{dcA}$. If all SM-capacitor voltages are balanced, each arm should deal with half of the real power. Fig. 7.18 shows the analysis of HC-MMC with the phase-A voltage reference containing negative dc offset, where e_{iA} and $v_{conA-ref}$ are the signals from the phase-A current control loop (see Fig. 7.13 (b)), and v_{upA} and v_{lowA} are the voltages across the upper and lower arms in phase A. It is seen that once the error signal e_{iA} has a negative offset and so does the converter voltage reference $v_{conA-ref}$ under PR controller. As a result, the voltages v_{upA} and v_{lowA} have dc offsets larger and lower than $V_{dc}/2$, respectively. This implies that the upper arm receives more than half of the real power in phase A, resulting in its average HB-SM capacitor voltage higher than the nominal value. Similarly, the lower arm has the average HB-SM capacitor voltage smaller than the nominal value. The results in Fig. 7.20 (a) validate this observation.

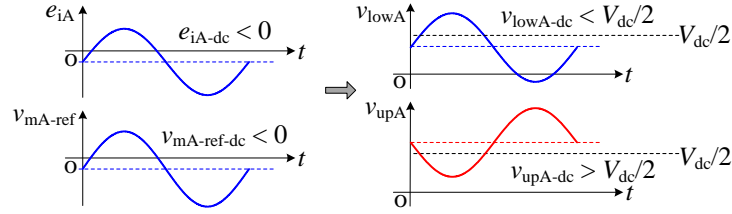


Fig. 7.18: Analysis of the main power stage of HC-MMC with phase-A voltage reference exhibiting dc offset

7.3.1.2 Improvement of the proposed control and validation

To accelerate the decay of dc offset embedded in the voltage reference, the dc offset of the error signal in the current control loop is feedforwarded to the current feedback unit through an integrator, as shown in Fig. 7.19.

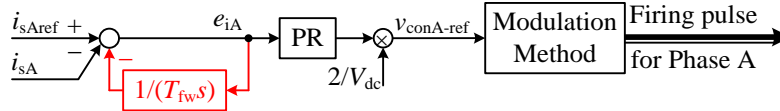


Fig. 7.19: Control diagram of the improved current control loop

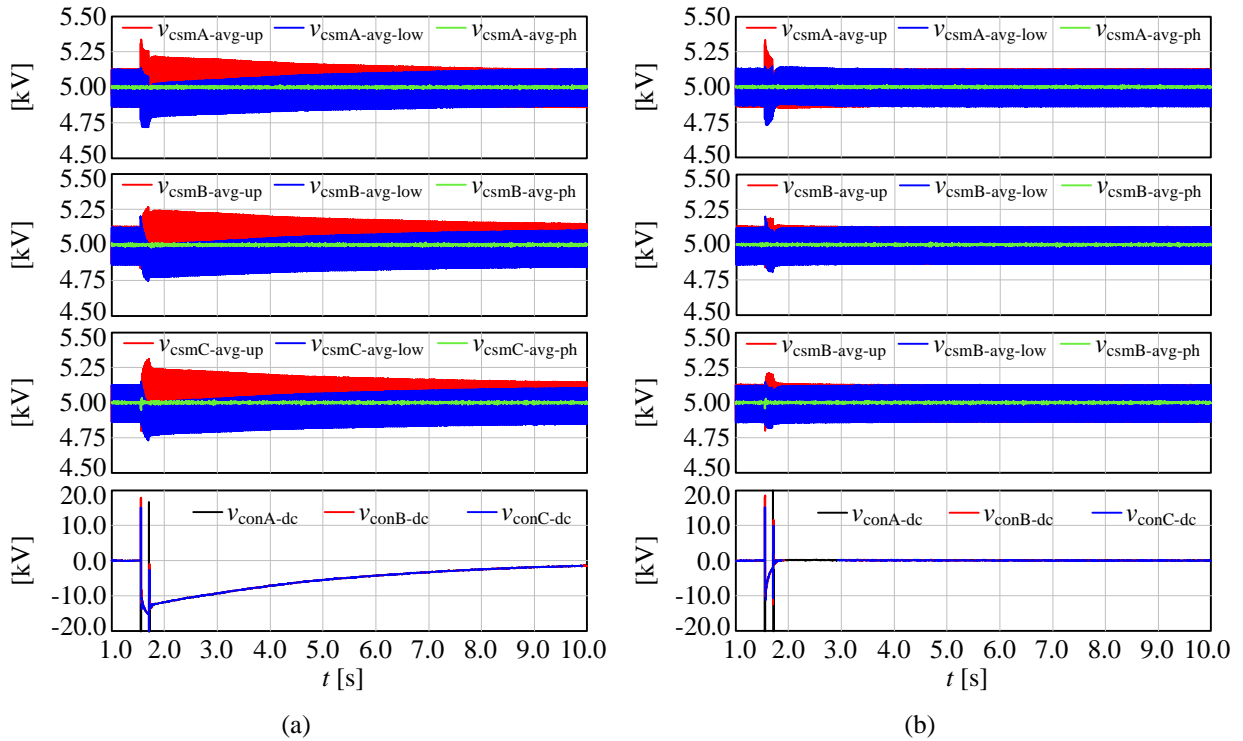


Fig. 7.20: Average HB- and FB-SM capacitor voltages and dc components of three-phase converter voltages under a phase-A-to-G fault

(a) without improvement on the proposed control; (b) with improvement on the proposed control.

Similar phase-A-to-G fault depicted in Section 7.3.1.1 is applied for the original HC-MMC with the improved control scheme displayed in Fig. 7.19. The operating waveforms are similar to those shown in Fig. 7.17. The average HB- and FB-SM capacitor voltages and the dc components of three-phase converter voltages under phase-A-to-G fault is shown in Fig. 7.20 (b). It shows that the controller in Fig. 7.19 rapidly decays the dc offsets in converter voltages, and the average HB-SM capacitor voltages between upper and lower arms are quickly balanced after the fault is cleared.

7.3.2 Simulation of phase-A-to-B fault

The operating waveforms of the original HC-MMC under a phase-A-to-B fault are shown in Fig. 7.21. This fault occurs at $t = 1.55$ s and is cleared at $t = 1.70$ s, with a fault detection delay of approximately 5.0 ms. As seen from Fig. 7.21 (a), StatusFlag changes from 0 (i.e., system is balanced at nominal condition) to 1 (i.e., system encounters a single L-to-L fault) at 1.55 s. Since the calculation of the voltage magnitude based upon SOGI method takes time to obtain the steady-state value, StatusFlag temporarily changes to 2 after the single L-to-L fault is cleared and before the estimated three-phase voltage magnitudes reach approximately nominal values. PhFlag changes from 1 (i.e., phase A) to 3 (i.e., phase C), since phases A and B are involved with ac fault. The feedback ac-voltage magnitude (v_{ac-pk}) shown in Fig. 7.13 (a) is selected as phase-A and phase-C voltage magnitudes before and after the ac fault is detected, respectively. The three-phase real power is decreased to ~ 250.0 MW ($= 500$ MW/2) during the fault, which is well matched with the reference correction shown in (7.19). The dc circulating currents in the arms of phases A and B are decreased, because the delivered real power is reduced due to phase-A-to-B fault. As seen from Fig. 7.21 (b), the zero-sequence component is nearly zero, whereas the negative-sequence component of the grid currents is approximately 65.0 A, which results in 3.25% of the positive-sequence component (~ 2.0 kA). This implies that the three-phase currents are well balanced during

the unbalanced ac fault. Additionally, the HB- and FB-SM capacitor voltages are balanced before, during, and after the fault.

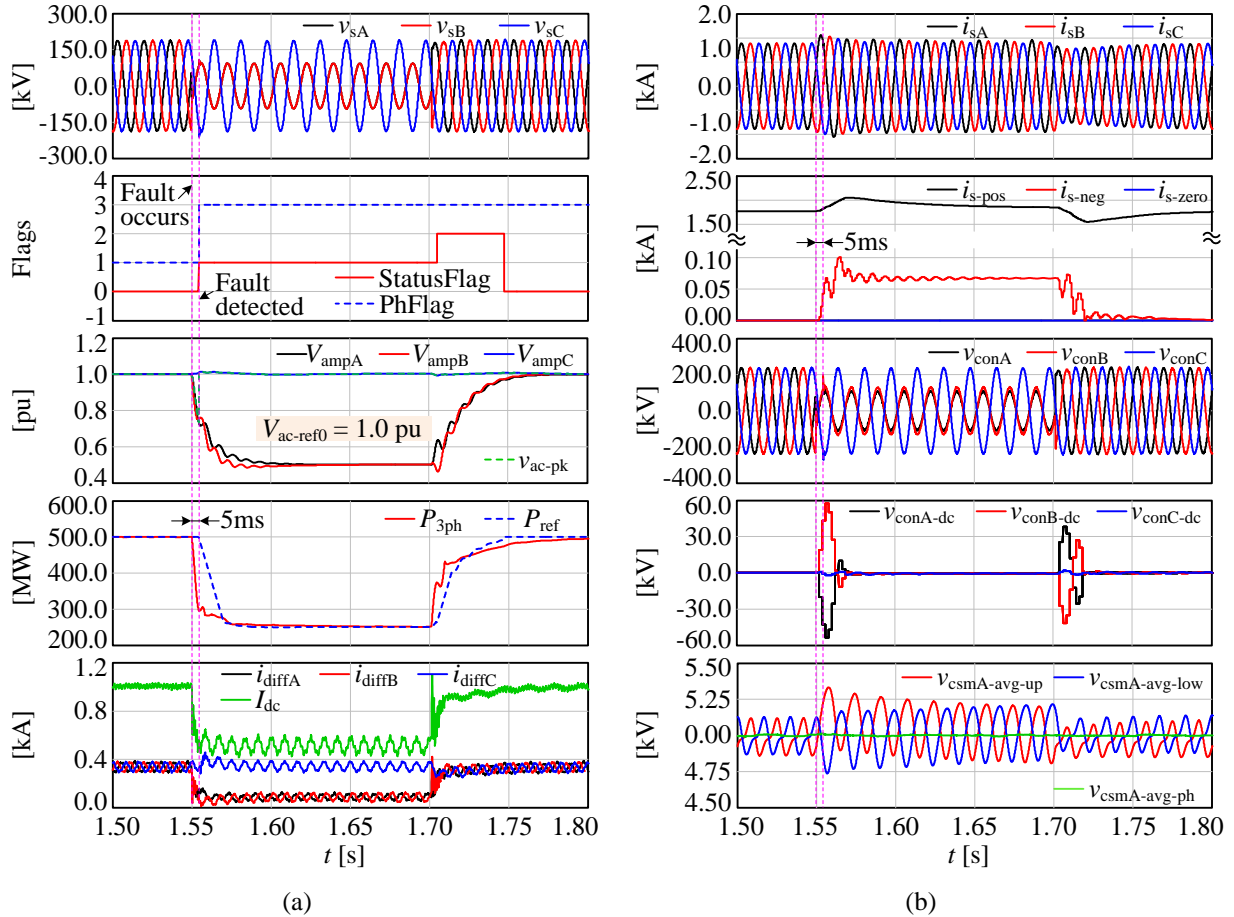


Fig. 7.21: Operations of HC-MMC under a phase-A-to-B fault with improved independent phase-current control

(a) three-phase grid voltages, status and phase flags, three-phase voltage magnitudes and its feedback magnitude, real power and its reference, and the dc circulating currents and dc-side current; (b) three-phase grid currents and their sequence components, three-phase converter voltages and their dc components, and average HB- and FB-SM capacitor voltages of phase A.

Overall, the system is able to successfully ride through ac faults with balanced and magnitude-limited currents under the proposed control scheme. With the dc-offset feedforward in the current control loop, the converter voltage gains prompt dc-offset elimination, which has the additional benefit of quickly balanced HB-SM capacitor voltages between arms. Therefore, the proposed independent-phase current control is proved to be effective and reliable.

7.4 Summary and key contributions

The chapter proposed a novel independent-phase current control method for three-phase VSCs to achieve balance enable operation through system imbalances. Extensive EMT simulation results of the original HC-MMC showed that the system under the proposed control scheme continues to operate with balanced and magnitude-limited currents under unbalanced grid conditions. Underlying conditions for HB-SM capacitor voltage imbalances were identified and corrected via simple and effective modifications to the controller.

Chapter 8

Contributions, Conclusions, and Recommendations for Future Work

Contents

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This chapter summarizes the overall contributions of this thesis and its major conclusions. Recommendations are also made for future work to extend the scope of the work in this thesis.

8.1 Major contributions and conclusions

The original and newly proposed HC-MMC topologies in this thesis were comprehensively studied, including their operating principles, the selection of the number of SMs and SM capacitance, losses and efficiency, dc-fault behavior and dc-fault blocking mechanism, and ac-fault ride-through capability. The major contributions and conclusions are listed as follows:

1. Based upon the THD analysis of the voltages crafted by the main power stage and the ac output voltage, design guidelines for the selection of the number of HB and FB SMs in the original HC-MMC were developed. It was shown that the number of FB SMs per phase limb must be

selected greater than or equal to half of the number of HB SMs per arm in the main power stage to improve the quality of voltage crafted by the main power stage only.

2. A novel control method was proposed to regulate the FB-SM capacitor voltages in the phase limb based upon a modified sinusoidal PWM scheme. Compared with an existing voltage regulation method based upon trapezoidal PWM [34], the proposed control method not only extends the linear modulation range but also reduces the filtering burden for the FB stack. The mixed-SM HC-MMC topology was proposed by adding FB SMs to the main power stage to further extend the advantages of the proposed control method.

3. The operating point of a VSC connected to an ac network was derived theoretically considering the interfacing transformer and the strength of ac network. The SM capacitor voltage ripple waveform was derived in a formula based upon electric charge variations, and the 2nd harmonic in the arm current was derived to a better accuracy compared to the existing literature [85] for the operation without CCSC. Design guidelines of SM capacitance for both the original and mixed-SM HC-MMCs were developed based upon the stored energy of SM capacitors per power rating unit under different operating modes (e.g., operation with or without CCSC, and operation with or without 3rd harmonic injection). The stored energy of SM capacitors per power rating unit was studied under different system parameters and their general ranges were provided. It was shown that (i) the HB-SM capacitor size in the main power stage of the original HC-MMC must be selected based upon the stored energy requirement in the range of 33.0~41.0 kJ/MVA with CCSC and 44.0~65.0 kJ/MVA without CCSC; (ii) by adding 6%~12% FB SMs into the main power stage and increasing the transformer's turns ratio accordingly, the optimal stored energy requirement of all HB- and FB-SM capacitor in the main power stage can be reached and it is in the range of 30.0~32.0 kJ/MVA; and (iii) the stored energy requirement of all FB-SM capacitors

in the phase limb is inversely proportional to the switching frequency of the FB stack and is approximately 6.5 kJ/MVA with $27f_o$ switching frequency.

4. Loss comparisons for HC-MMCs with different FB-SM capacitor-voltage regulation methods and with different switching frequencies were conducted. The results, that are the first of their kind to be reported, indicate that HC-MMC is a superior alternative to FB-MMC when converters with dc-fault blocking capabilities are concerned. It was shown that the original HC-MMC with the proposed modified sinusoidal PWM has lower losses than with the existing methods, and that the proposed mixed-SM HC-MMC offers an extended linear-regulation range without increasing losses and even reducing them due to reduced phase currents.

5. Equivalent models individually derived for the dc and ac circulating currents were developed to study the behavior of the original and mixed-SM HC-MMCs under a pole-to-pole dc fault. It was shown that both the original and mixed-SM HC-MMCs have the ability to isolate the faulted dc side from the ac side. Compared with the original HC-MMC, the mixed-SM HC-MMC has much faster performance in clearing the dc-fault current. Additional considerations for SM capacitance selection were analyzed to avoid adverse SM capacitor voltages under a pole-to-pole fault. It was shown that (i) the HB-SM capacitance in the main power stage of both the original and mixed-SM HC-MMCs can be selected based upon normal operation to ensure proper operation in both normal and dc fault conditions; (ii) it is recommended to check all FB-SM capacitor voltages due to a dc fault after selecting their capacitance based upon normal operation to ensure that these SM capacitors have acceptable voltage rise during a fault. If the faulted voltage rise is not acceptable, then larger capacitors need to be selected.

6. A new independent-phase current control method for three-phase VSCs was proposed to achieve fast recovery from unbalanced ac faults with balanced phase currents and minimized

reactive power. Extensive EMT simulation results of the original HC-MMC validated the effectiveness of the proposed control. The underlying conditions for SM capacitor voltage imbalances were identified and corrected via simple and effective modifications to the controller.

7. The mixed-SM HC-MMC was proven to have superior performance than the original HC-MMC in terms of FB-SM capacitor voltage regulation, system efficiency, and dc-fault clearing time. Moreover, with 6%~12% FB SMs added to the main power stage and the rated modulation index of approximately 1.12, the requirement of the stored energy of all SM capacitors in the main power stage of the mixed-SM HC-MMC is 7.0%~28.0% lower than that of the original HC-MMC.

The author's publications arising from the research in this thesis are listed as follows:

(1) X. Shi, S. Howell, C. Shumski, S. Filizadeh and D. Jacobson, "Capacitor-voltage regulation and linear-range extension of a hybrid cascaded modular multilevel converter," *IEEE Gener. Transm. & Dis.*, vol. 11, no. 18, pp. 4588-4598, 2017.

(2) X. Shi, S. Filizadeh and D. A. Jacobson, "Loss evaluation for the hybrid cascaded MMC under different voltage-regulation methods," *IEEE Trans. Energy Convers.*, vol. 33, no. 3, pp. 1487-1298, 2018.

(3) X. Shi and S. Filizadeh, "Design considerations of a hybrid cascaded modular multilevel converter," in *Cigre Session*, Vancouver, Canada, 2017.

(4) X. Shi and S. Filizadeh, "Pole-to-pole dc-fault behavior analysis of a hybrid cascaded modular multilevel converter in HVDC applications," in *Cigre Session*, Calgary, Canada, 2018.

(5) X. Shi and S. Filizadeh, "Independent-phase current control of a three-phase voltage-source converter under unbalanced operating conditions," *The Journal of Engineering*, vol. 2019, no. 16, pp. 1338-1345, 2019.

(6) X. Shi and S. Filizadeh, "Laboratory setup of modular multilevel converters with RTDS as controller," in *RTDS Technologies North American Appl. + Tech. Conf.*, Denver, USA, 2019.

(7) X. Shi, S. Filizadeh and L. Wang, "Analysis of submodule capacitor voltage ripple and second-harmonic current in MMCs," in *IEEE COMPEL 2019*, Toronto, Canada, 2019.

8.2 Future work

As a continuation of the research work conducted in this thesis, the following topics are suggested:

1. The investigation methods for SM capacitor sizing, dc-fault behavior analysis and ac-fault ride-through control shown in this thesis are not limited to the original and mixed-SM HC-MMCs, and they can be extended to either conventional or novel MMC topologies. Therefore, SM capacitance selection and dc-fault performance among different MMCs can be investigated and comprehensively compared to evaluate their relative merits.

2. Loss comparisons between the investigated HC-MMCs and other MMC topologies that have topological dc-fault blocking capabilities can be made. This is useful to evaluate if the HC-MMC has relative merits based on system efficiency.

3. At present, conventional HB-MMC has been in use in practical HVDC transmission systems. Due to its inability of blocking dc faults, hybrid dc breakers may be required in the converter system. The loss comparisons between the investigated HC-MMCs and the conventional HB-MMC with hybrid dc breakers can be made to evaluate if the investigated HC-MMCs in this thesis have relative advantages based on system efficiency.

4. In the existing literature, 2nd harmonic is controlled to optimize the losses in conventional HB-MMC [103]-[105]. Since the HC-MMC has similar structure and operation with the conventional HB-MMC, similar methods can be used for the HC-MMC to optimize its losses. Under this circumstance, the influence of the controlled 2nd harmonic current on the SM capacitor sizing can be investigated using analyses similar to what were shown in Section 4.3.

5. In practice, a dc short-circuit fault may occur in different locations along the transmission line. Based upon a similar analysis shown in Section 6.1, equivalent models can be developed to evaluate the relevant dc-fault performance.

6. As seen from the dc-fault analysis shown in Chapter 6, the HC-MMC takes a relatively long time to clear the dc-side circulating current during dc faults, and the mixed-SM HC-MMC can promptly decay the dc fault current to zero due to the existence of FB SMs in the main power stage. As such, a new HC-MMC topology can be proposed by replacing a certain number of HB SMs in the main power stage of the original HC-MMC with FB SMs instead of adding extra FB SMs. In normal operation, the new HC-MMC operates the FB SMs in the main power stage as HB SMs, i.e., the FB SMs only output 0 and positive voltage levels. Under dc faults, the FB SMs in the main power stage of the new HC-MMC are inserted to decay the dc-side fault current. The selection of the number of FB SMs that are used to replace HB SMs in the main power stage of the original HC-MMC should be investigated to obtain proper dc-fault blocking performance. The SM capacitor sizing of the FB SMs in the main power stage can also be discussed.

7. In practical systems, the requirement of ac-fault ride-through capability may be different. In some cases, the systems are required to support the PCC bus at the faulted ac grid. To achieve such requirement, only the reference signals (P_{ref} and V_{acref}) and the feedback signal (V_{ac-pk}) should be modified accordingly, and the main control hierarchy can be kept the same as that proposed in

Section 7.2.2. The relevant algorithms to modify reference and feedback signals can be developed and validated by EMT simulations.

8. During dc faults, MMC topologies may be controlled as a static compensator (STATCOM) to support the ac grid and maintain SM capacitor voltages under control [106]-[107]. Similarly, controls for HC-MMC to operate as a STATCOM during dc faults can be studied.

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Appendix A

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A.1 Derivation of the 2nd harmonic current considering the 3rd harmonic injection

In Section 4.2.1, the derivation of the 2nd harmonic current does not consider the 3rd harmonic injection in the modulation waveforms. If the 3rd harmonic injection is used to extend the linear modulation range, the derivation of the 2nd harmonic current in the arms of HB-MMC will be highly complicated. The single-phase schematic of HB-MMC is shown in Fig. 4.4. Denote the upper- and lower-arm modulation waveforms and currents without CCSC and with 3rd harmonic injection as

$$\begin{aligned}
 m_{\text{up}}(t) &= \frac{1}{2} \left(1 - m \sin(\omega_o t) - k_{3\text{rd}} m \sin(3\omega_o t) \right), & i_{\text{up}}(t) &= \frac{I_{\text{dc}}}{3} + \frac{\sqrt{2} I_{\text{con}}}{2} \sin(\omega_o t + \varphi) + i_{2\text{nd}}(t) \\
 m_{\text{low}}(t) &= \frac{1}{2} \left(1 + m \sin(\omega_o t) + k_{3\text{rd}} m \sin(3\omega_o t) \right), & i_{\text{low}}(t) &= \frac{I_{\text{dc}}}{3} - \frac{\sqrt{2} I_{\text{con}}}{2} \sin(\omega_o t + \varphi) + i_{2\text{nd}}(t)
 \end{aligned} \tag{A.1}$$

where $i_{2\text{nd}}(t)$ is assumed to be

$$i_{2\text{nd}}(t) = I_{2\text{nd}} \cos(2\omega_o t + \theta_{2\text{nd}}) \tag{A.2}$$

According to the expressions shown in (4.18) and (4.19), the voltage across two arm inductors can be obtained as follows:

$$\begin{aligned}
v_{2L}(t) &= V_{dc} - m_{up}(t)Nv_{csmUp}(t) - m_{low}(t)Nv_{csmLow}(t) - (i_{up}(t) + i_{low}(t))R_{arm} \\
&= \frac{N}{2} \left[m \sin(\omega_o t) + k_{3rd} m \sin(3\omega_o t) \right] \cdot \left[\Delta v_{csmUp}(t) - \Delta v_{csmLow}(t) \right] \\
&\quad - \frac{N}{2} \left[\Delta v_{csmUp}(t) + \Delta v_{csmLow}(t) \right] - 2R_{arm} \left(\frac{I_{dc}}{3} + I_{2nd} \cos(2\omega_o t + \theta_{2nd}) \right)
\end{aligned} \tag{A.3}$$

where $\Delta v_{csmUp}(t)$ and $\Delta v_{csmLow}(t)$ are shown in (4.16) and (4.17), respectively. Substituting (A.1) into (A.3), the terms of the expression of $v_{2L}(t)$ shown in (A.3) are expressed as follows:

$$\begin{aligned}
&\frac{N}{2} m \sin(\omega_o t) \cdot \left[\Delta v_{csmUp}(t) - \Delta v_{csmLow}(t) \right] \\
&= \frac{1}{(1+k_{red})\omega_o C_{eq}} \cdot \left[\begin{aligned} &\frac{I_{dc} m^2}{12} \sin(2\omega_o t) - \frac{\sqrt{2} I_{con} m}{8} (\sin(2\omega_o t + \varphi) - \sin(\varphi)) \\ &+ \frac{I_{2nd} m^2}{8} \left(\frac{1}{3} \sin(4\omega_o t + \theta_{2nd}) - \frac{4}{3} \sin(2\omega_o t + \theta_{2nd}) + \sin(\theta_{2nd}) \right) \\ &+ \frac{k_{3rd} I_{dc} m^2}{36} (\sin(4\omega_o t) - \sin(2\omega_o t)) \\ &+ \frac{k_{3rd} I_{2nd} m^2}{8} \left(\frac{1}{5} (\sin(6\omega_o t + \varphi) - \sin(4\omega_o t + \varphi)) \right. \\ &\quad \left. + \sin(2\omega_o t - \varphi) + \sin(\varphi) \right) \end{aligned} \right]
\end{aligned} \tag{A.4}$$

$$\begin{aligned}
&\frac{N}{2} k_{3rd} m \sin(3\omega_o t) \cdot \left[\Delta v_{csmUp}(t) - \Delta v_{csmLow}(t) \right] \\
&= \frac{k_{3rd}}{(1+k_{red})\omega_o C_{eq}} \cdot \left[\begin{aligned} &\frac{I_{dc} m^2}{12} (\sin(4\omega_o t) + \sin(2\omega_o t)) + \frac{k_{3rd} I_{dc} m^2}{36} \sin(6\omega_o t) \\ &- \frac{\sqrt{2} I_{con} m}{8} (\sin(4\omega_o t + \varphi) + \sin(2\omega_o t - \varphi)) \\ &+ \frac{I_{2nd} m^2}{8} \left(\frac{1}{3} (\sin(6\omega_o t + \theta_{2nd}) - \sin(\theta_{2nd})) \right. \\ &\quad \left. - \sin(4\omega_o t + \theta_{2nd}) - \sin(2\omega_o t - \theta_{2nd}) \right) \\ &+ \frac{k_{3rd} I_{2nd} m^2}{8} \left(\frac{1}{5} (\sin(8\omega_o t + \varphi) - \sin(2\omega_o t + \varphi)) \right. \\ &\quad \left. + \sin(4\omega_o t - \varphi) + \sin(2\omega_o t + \varphi) \right) \end{aligned} \right]
\end{aligned} \tag{A.5}$$

$$\begin{aligned}
& -\frac{N}{2} \left[\Delta v_{\text{csmUp}}(t) + \Delta v_{\text{csmLow}}(t) \right] \\
& = \frac{-1}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \cdot \left[\begin{aligned} & \frac{\sqrt{2}I_{\text{con}}m}{16} \sin(2\omega_o t + \varphi) + \frac{I_{2\text{nd}}}{4} \sin(2\omega_o t + \theta_{2\text{nd}}) \\ & + \frac{k_{3\text{rd}}\sqrt{2}I_{\text{con}}m}{16} \left(\frac{1}{2} \sin(4\omega_o t + \varphi) - \sin(2\omega_o t - \varphi) \right) \end{aligned} \right] \quad (\text{A.6})
\end{aligned}$$

where $C_{\text{eq}} = C_{\text{sm}}/N$ and the relationship between I_{con} and I_{dc} is shown in (4.15). Therefore, the 2nd harmonic term of the voltage across two arm inductors can be obtained as follows:

$$v_{2L-2\text{nd}}(t) = a_1 \sin(2\omega_o t) + a_2 \cos(2\omega_o t) \quad (\text{A.7})$$

where a_1 and a_2 are expressed as

$$\begin{aligned}
a_1 & = 2R_{\text{arm}} I_{2\text{nd}} \sin(\theta_{2\text{nd}}) - \frac{I_{\text{dc}}}{4(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(1 - \frac{m^2}{3} - \frac{2k_{3\text{rd}}m^2}{9} + \frac{k_{3\text{rd}}}{3} \right) \\
& \quad - \frac{I_{2\text{nd}} \cos(\theta_{2\text{nd}})}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(\frac{1}{4} + \frac{m^2}{6} + \frac{k_{3\text{rd}}m^2}{8} \right) + \frac{I_{2\text{nd}} \cos(\varphi)m^2k_{3\text{rd}}}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(\frac{1}{8} + \frac{k_{3\text{rd}}}{10} \right) \\
a_2 & = -2R_{\text{arm}} I_{2\text{nd}} \cos(\theta_{2\text{nd}}) - \frac{I_{\text{dc}} \tan(\varphi)}{4(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(1 - \frac{k_{3\text{rd}}}{3} \right) \\
& \quad - \frac{I_{2\text{nd}} \sin(\theta_{2\text{nd}})}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(\frac{1}{4} + \frac{m^2}{6} - \frac{k_{3\text{rd}}m^2}{8} \right) - \frac{I_{2\text{nd}} \sin(\varphi)m^2k_{3\text{rd}}}{(1+k_{\text{red}})\omega_o C_{\text{eq}}} \left(\frac{1}{8} - \frac{k_{3\text{rd}}}{10} \right) \quad (\text{A.8})
\end{aligned}$$

With the 2nd harmonic current shown in (A.2), the 2nd harmonic voltage of $v_{2L}(t)$ can be expressed in another form as

$$\begin{aligned}
v_{2L-2\text{nd}}(t) & = -4\omega_o L_{\text{arm}} I_{2\text{nd}} \sin(2\omega_o t + \theta_{2\text{nd}}) \\
& = -4\omega_o L_{\text{arm}} I_{2\text{nd}} \cos(\theta_{2\text{nd}}) \sin(2\omega_o t) - 4\omega_o L_{\text{arm}} I_{2\text{nd}} \sin(\theta_{2\text{nd}}) \cos(2\omega_o t) \quad (\text{A.9})
\end{aligned}$$

Comparing the expressions shown in (A.7) and (A.9), it must satisfy the following conditions:

$$a_1 = -4\omega_o L_{\text{arm}} I_{2\text{nd}} \cos(\theta_{2\text{nd}}), \quad a_2 = -4\omega_o L_{\text{arm}} I_{2\text{nd}} \sin(\theta_{2\text{nd}}) \quad (\text{A.10})$$

After simplifications, the following equation can be obtained.

$$b_1 \sin(\theta_{2\text{nd}}) + b_2 \cos(\theta_{2\text{nd}}) + b_3 = 0 \quad (\text{A.11})$$

where the coefficients b_1 , b_2 and b_3 are shown as follows:

$$\begin{aligned} b_1 &= 4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} \left(1 - \frac{k_{3\text{rd}}}{3}\right) \tan(\varphi) \\ &\quad - \left[8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - \left(\frac{1}{2} + \frac{m^2}{3} + \frac{k_{3\text{rd}} m^2}{4}\right) \right] \cdot \left(1 - \frac{m^2}{3} - \frac{2k_{3\text{rd}} m^2}{9} + \frac{k_{3\text{rd}}}{3}\right) \\ b_2 &= 4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} \left(1 - \frac{m^2}{3} - \frac{2k_{3\text{rd}} m^2}{9} + \frac{k_{3\text{rd}}}{3}\right) \\ &\quad + \left[8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - \left(\frac{1}{2} + \frac{m^2}{3} + \frac{k_{3\text{rd}} m^2}{4}\right) \right] \cdot \left(1 - \frac{k_{3\text{rd}}}{3}\right) \tan(\varphi) \\ b_3 &= k_{3\text{rd}} m^2 \sin(\varphi) \cdot \left[\left(\left(1 - \frac{k_{3\text{rd}}}{3}\right) \cdot \left(\frac{1}{4} + \frac{k_{3\text{rd}}}{5}\right) + \left(1 - \frac{m^2}{3} - \frac{2k_{3\text{rd}} m^2}{9} + \frac{k_{3\text{rd}}}{3}\right) \cdot \left(\frac{1}{4} - \frac{k_{3\text{rd}}}{5}\right) \right) \right] \end{aligned} \quad (\text{A.12})$$

After obtaining $\theta_{2\text{nd}}$ by solving (A.11), the 2nd harmonic current magnitude $I_{2\text{nd}}$ can be calculated by the expression shown below.

$$I_{2\text{nd}} = \frac{I_{\text{dc}}}{2} \cdot \frac{1 - \frac{m^2}{3} - \frac{2k_{3\text{rd}} m^2}{9} + \frac{k_{3\text{rd}}}{3}}{\left[\begin{aligned} &\left(8(1+k_{\text{red}})\omega_o^2 L_{\text{arm}} C_{\text{eq}} - \left(\frac{1}{2} + \frac{m^2}{3} + \frac{k_{3\text{rd}} m^2}{4}\right) \right) \cos(\theta_{2\text{nd}}) \\ &+ 4(1+k_{\text{red}})\omega_o C_{\text{eq}} R_{\text{arm}} \sin(\theta_{2\text{nd}}) + k_{3\text{rd}} m^2 \sin(\varphi) \left(\frac{1}{4} + \frac{k_{3\text{rd}}}{5}\right) \end{aligned} \right]} \quad (\text{A.13})$$

Substituting $k_{3\text{rd}} = 0$ into the expressions shown in (A.11) and (A.13), the same expressions as shown in (4.27) and (4.28) can be obtained for $\theta_{2\text{nd}}$ and $I_{2\text{nd}}$, respectively. If substituting $k_{3\text{rd}} = 0$ and $R_{\text{arm}} = 0$ into (A.11) and (A.13), the same expressions as shown in (4.29) and (4.30) can be obtained.

With the system specifications shown in Table 4.2 and $k_{red} = 0$, the comparisons of the theoretical results of 2nd harmonic current between the operations with ($I_{2nd(k3rd)}$ and $\theta_{2nd(k3rd)}$) and without (I_{2nd} and θ_{2nd}) 3rd harmonic injection are displayed in Fig. A.1, where the injected the 3rd harmonic amount is $k_{3rd} = 1/6$. It is observed that under various operating conditions ($P_{ref} = [0.5 \text{ pu}, 1.0 \text{ pu}]$ and $V_{acref} = [0.8 \text{ pu}, 1.05 \text{ pu}]$), the magnitude difference is within $[-0.5\%, -2.0\%]$ as base of $I_{con_pk}/2$ (i.e., the fundamental component of the arm current), and the phase angle difference is in the range of $[-1.5^\circ, 2.5^\circ]$. Therefore, the influence of the 3rd harmonic injection on the 2nd harmonic current is small and is reasonable to be neglected to simplify the analysis.

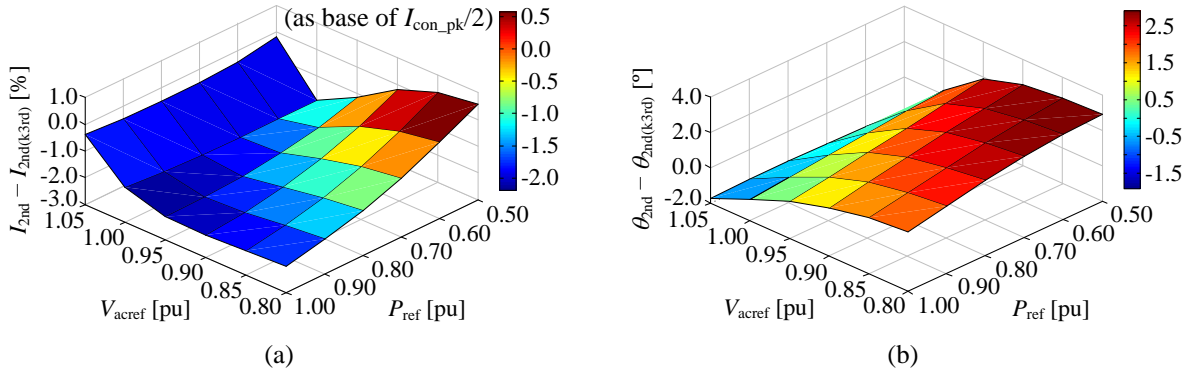


Fig. A.1: Comparison of theoretical results between the operations with and without the 3rd harmonic injection (a) error of the 2nd harmonic current magnitude ($I_{2nd} - I_{2nd(k3rd)}$) normalized by $I_{con_pk}/2$; (b) error of the 2nd harmonic current angle ($\theta_{2nd} - \theta_{2nd(k3rd)}$).

The same system as that shown in Table 4.2 is simulated with and without the 3rd harmonic injection. The simulation results of the 2nd harmonic current under the operation with and without the 3rd harmonic injection are compared in Fig. A.2. It is also shown that under various operation points ($P_{ref} = [0.5 \text{ pu}, 1.0 \text{ pu}]$ and $V_{acref} = [0.8 \text{ pu}, 1.05 \text{ pu}]$) and two redundancy cases ($k_{red} = 0$ and 10%), the 2nd harmonic current with the 3rd harmonic injection is close to that without the 3rd harmonic injection. Therefore, the influence of the 3rd harmonic injection on the 2nd harmonic current is neglected to simplify the analysis in Section 4.3.1.2.

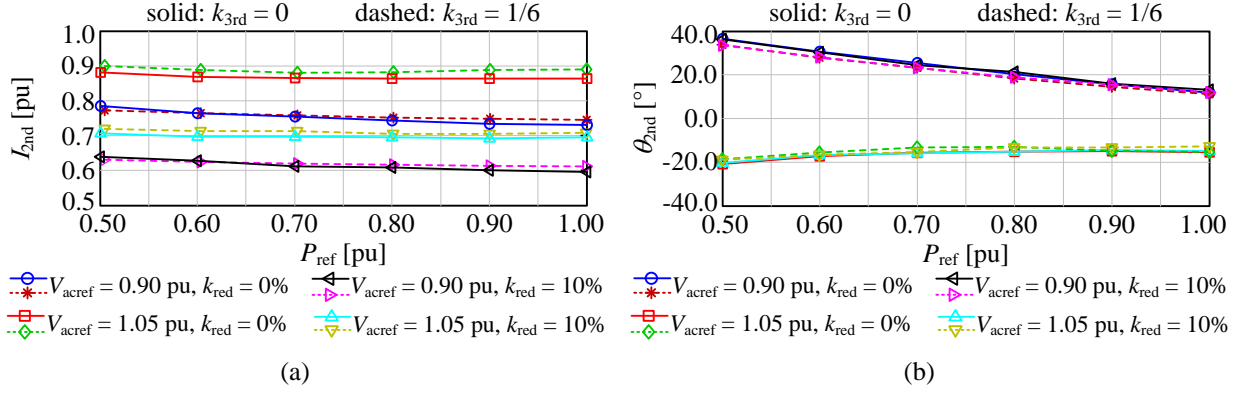


Fig. A.2: Comparison of simulation results between the operations with and without the 3rd harmonic injection (a) the 2nd harmonic current magnitude; (b) phase angle of the 2nd harmonic current.

A.2 Algorithm to obtain the SM capacitor voltage ripple waveform in the main power stage of the mixed-SM HC-MMC

As discussed in Section 4.3.2, when $m_{up}(t) < 0$, only FB SMs are required to be inserted. When $m_{up}(t) > 0$, the required SMs to be inserted can be either HB or FB SMs or both HB and FB SMs, which is determined by the current polarity and sorting sequence of all the SM capacitor voltages in one arm, since both HB and FB SMs can output positive voltage levels. Therefore, if $m_{up}(t)$ has negative zone over the fundamental period, the charging and discharging chances for HB and FB SMs in the main power stage are different, resulting in different capacitor voltage ripple waveforms for HB- and FB-SM capacitors in the main power stage.

The charging status for HB and FB SMs in the main power stage is summarized in Table A.1, where N_h is the nominal number of HB SMs per arm, and k_{red} and k_{fm} are the number of redundant HB SMs per arm and the number of FB SMs per arm over N_h , respectively. When $m_{up}(t_0) < 0$, only FB SMs have the chance to be charged or discharged. Based upon the balancing algorithm and $m_{up}(t_0) > 0$, when $[\Delta v_{cfm}(t_0 - \Delta t) - \Delta v_{chb}(t_0 - \Delta t)] \cdot i_{up}(t_0) < 0$, FB SMs are in the higher priority to insert to charge ($i_{up}(t_0) > 0$) and discharge ($i_{up}(t_0) < 0$), and additional HB SMs are inserted until

$m_{\text{up}}(t_0) > k_{\text{fm}}$; when $[\Delta v_{\text{cfm}}(t_0 - \Delta t) - \Delta v_{\text{chb}}(t_0 - \Delta t)] \cdot i_{\text{up}}(t_0) > 0$, HB SMs are firstly selected to insert to charge ($i_{\text{up}}(t_0) > 0$) and discharge ($i_{\text{up}}(t_0) < 0$), and additional FB SMs are required to insert until $m_{\text{up}}(t_0) > (1+k_{\text{red}})$. Denote the number of inserted HB and FB SMs as $k_{\text{HBin}} \cdot N_{\text{h}}$ and $k_{\text{FBin}} \cdot N_{\text{h}}$, respectively, where $(k_{\text{HBin}} + k_{\text{FBin}})$ must be equal to $m_{\text{up}}(t_0)$. The total charges for HB and FB SMs are approximately $(k_{\text{HBin}} \cdot N_{\text{h}} \cdot i_{\text{up}}(t_0) \cdot \Delta t)$ and $(k_{\text{FBin}} \cdot N_{\text{h}} \cdot i_{\text{up}}(t_0) \cdot \Delta t)$ within the time interval of $[t_0 - \Delta t, t_0]$, where Δt is a short time length. In order to balance the SM capacitor voltages, the total charges are required to be evenly distributed to the total number of HB and FB SMs in one arm. Therefore, the capacitor voltage changes for one HB and FB SM can be calculated as follows:

$$\begin{aligned} (1+k_{\text{red}})N_{\text{h}}C_{\text{hb}}(\Delta v_{\text{chb}}(t_0) - \Delta v_{\text{chb}}(t_0 - \Delta t)) &= k_{\text{HBin}}N_{\text{h}}i_{\text{up}}(t_0)\Delta t \\ \Rightarrow \Delta v_{\text{chb}}(t_0) - \Delta v_{\text{chb}}(t_0 - \Delta t) &= \frac{k_{\text{HBin}}i_{\text{up}}(t_0)\Delta t}{(1+k_{\text{red}})C_{\text{hb}}} \end{aligned} \quad (\text{A.14})$$

$$\begin{aligned} k_{\text{fm}}N_{\text{h}}C_{\text{fm}}(\Delta v_{\text{cfm}}(t_0) - \Delta v_{\text{cfm}}(t_0 - \Delta t)) &= k_{\text{FBin}}N_{\text{h}}i_{\text{up}}(t_0)\Delta t \\ \Rightarrow \Delta v_{\text{cfm}}(t_0) - \Delta v_{\text{cfm}}(t_0 - \Delta t) &= \frac{k_{\text{FBin}}i_{\text{up}}(t_0)\Delta t}{k_{\text{fm}}C_{\text{fm}}} \end{aligned} \quad (\text{A.15})$$

where $(k_{\text{HBin}} + k_{\text{FBin}}) = m_{\text{up}}(t_0)$.

Table A.1 Charging status of the HB and FB SMs in the main power stage of mixed-SM HCMC

Conditions		Status	Required # of inserted SMs	
			# of HB SMs	# of FB SMs
$m_{\text{up}}(t_0) < 0$		charging ($i_{\text{up}}(t_0) > 0$) discharging ($i_{\text{up}}(t_0) < 0$)	0	$m_{\text{up}}(t_0) \cdot N_{\text{h}}$
$\Delta v_{\text{cfm}}(t_0 - \Delta t) > \Delta v_{\text{chb}}(t_0 - \Delta t)$ and $i_{\text{up}}(t_0) < 0$	$0 < m_{\text{up}}(t_0) \leq k_{\text{fm}}$	discharging	0	$m_{\text{up}}(t_0) \cdot N_{\text{h}}$
	$m_{\text{up}}(t_0) > k_{\text{fm}}$	discharging	$(m_{\text{up}}(t_0) - k_{\text{fm}}) \cdot N_{\text{h}}$	$k_{\text{fm}} \cdot N_{\text{h}}$
$\Delta v_{\text{cfm}}(t_0 - \Delta t) < \Delta v_{\text{chb}}(t_0 - \Delta t)$ and $i_{\text{up}}(t_0) > 0$	$0 < m_{\text{up}}(t_0) \leq k_{\text{fm}}$	charging	0	$m_{\text{up}}(t_0) \cdot N_{\text{h}}$
	$m_{\text{up}}(t_0) > k_{\text{fm}}$	charging	$(m_{\text{up}}(t_0) - k_{\text{fm}}) \cdot N_{\text{h}}$	$k_{\text{fm}} \cdot N_{\text{h}}$
$\Delta v_{\text{cfm}}(t_0 - \Delta t) > \Delta v_{\text{chb}}(t_0 - \Delta t)$ and $i_{\text{up}}(t_0) > 0$	$0 < m_{\text{up}}(t_0) \leq (1+k_{\text{red}})$	charging	$m_{\text{up}}(t_0) \cdot N_{\text{h}}$	0
	$m_{\text{up}}(t_0) > (1+k_{\text{red}})$	charging	$(1+k_{\text{red}}) \cdot N_{\text{h}}$	$[m_{\text{up}}(t_0) - (1+k_{\text{red}})] \cdot N_{\text{h}}$
$\Delta v_{\text{cfm}}(t_0 - \Delta t) < \Delta v_{\text{chb}}(t_0 - \Delta t)$ and $i_{\text{up}}(t_0) < 0$	$0 < m_{\text{up}}(t_0) \leq (1+k_{\text{red}})$	discharging	$m_{\text{up}}(t_0) \cdot N_{\text{h}}$	0
	$m_{\text{up}}(t_0) > (1+k_{\text{red}})$	discharging	$(1+k_{\text{red}}) \cdot N_{\text{h}}$	$[m_{\text{up}}(t_0) - (1+k_{\text{red}})] \cdot N_{\text{h}}$

Based upon the charging status shown in Table A.1, the algorithm to obtain the HB and FB-SM capacitor voltage ripple waveforms in the main power stage of mixed-SM HC-MMC is shown in Fig. A.3, where it only calculates the voltage ripple at $t = t_0$ based upon the information from previous time-step. The capacitor voltage ripple waveforms for the HB and FB SMs can be obtained by using loops of this algorithm.

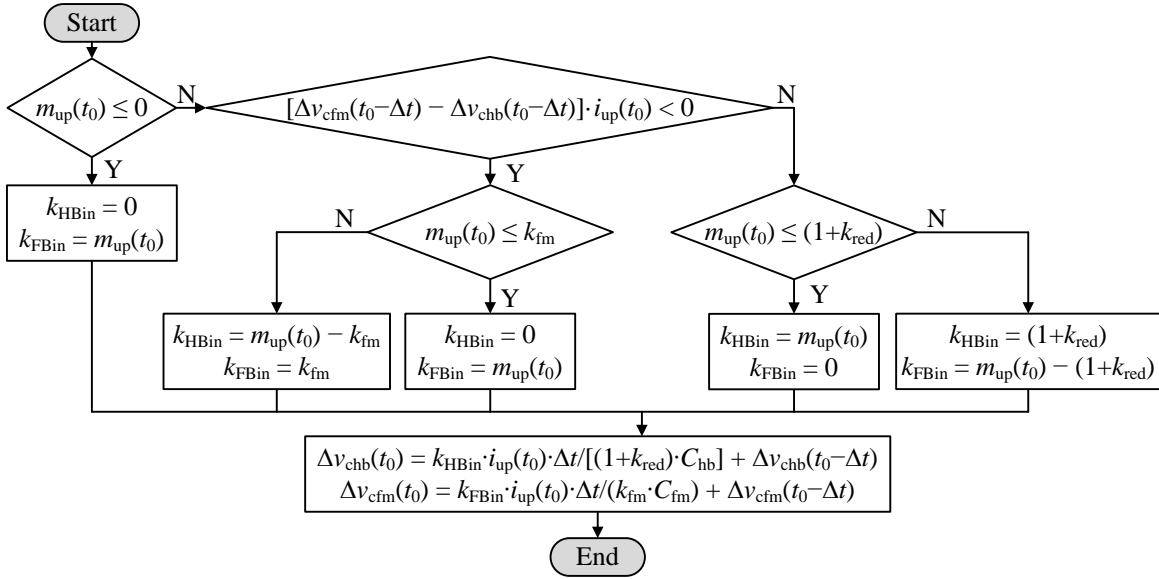


Fig. A.3: Algorithm to obtain the HB- and FB-SM capacitor voltage ripple waveforms in the main power stage of mixed-SM HC-MMC

In order to validate the proposed algorithm to obtain the SM capacitor voltage ripple waveforms, the three-phase system of mixed-SM HC-MMC shown in Fig. A.4 is simulated, and the system specifications are listed in

Table A. 2. The comparison between the theoretical and simulation results of the HB- and FB-SM capacitor voltage ripple waveforms is displayed in Fig. A.5 for two simulation cases. It is seen that the theoretical results are well matched with the simulation results. This validates the effectiveness of the proposed algorithm shown in Fig. A.3. In addition, it is observed that FB-SM capacitor voltage ripple waveform is different from that of the HB SM in the main power stage of mixed-SM HC-MMC. Therefore, the SM capacitance selection for mixed-SM HC-MMC is different from that of original HC-MMC, which is discussed in Section 4.3.2.

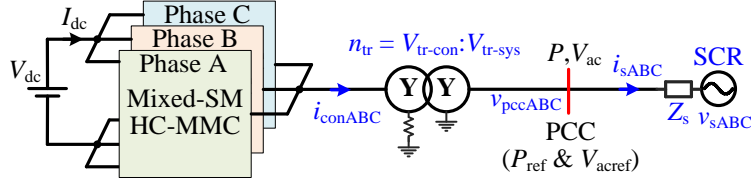


Fig. A.4: Schematic diagram of the simulated mixed-SM HC-MMC

Table A. 2: System parameters of EMT simulations of mixed-SM HC-MMC

DC side: 500 MW, 500 kV		AC side: 230 kV, 60 Hz, and SCR = $3.0 \angle 80^\circ$		Arm inductance: 0.05 H
Case #	Nominal # of HB SMs/arm and capacitance/SM	# of FB SMs/arm and capacitance/SM	HB-SM redundancy	Transformer (conv./sys.)
Case 1	100 and 2.5 mF	10 and 2.5 mF	0%	1.2×290 kV: 230 kV, 600 MVA with 6% leakage
Case 2	100 and 2.5 mF	10 and 10.0 mF	10%	

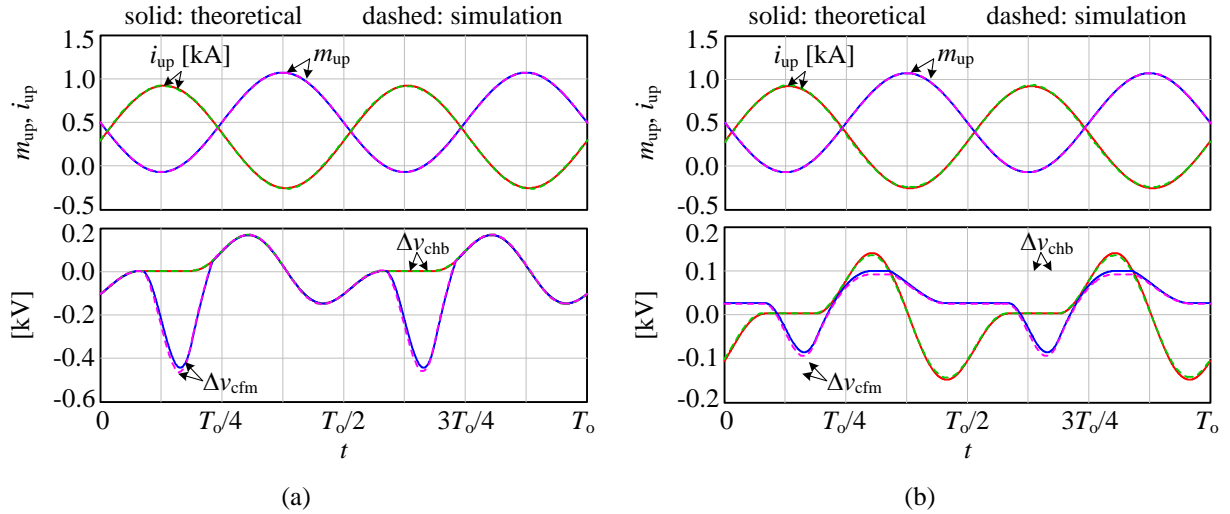


Fig. A.5: Comparison between the theoretical and simulation results of the HB- and FB-SM capacitor voltage ripple waveforms

(a) case 1 ($N_h = 100$, $N_{fm} = 10$, $k_{red} = 0\%$, $C_{hb} = 2.5$ mF and $C_{fm} = 2.5$ mF); (b) case 2 ($N_h = 100$, $N_{fm} = 10$, $k_{red} = 10\%$, $C_{hb} = 2.5$ mF and $C_{fm} = 10.0$ mF).