Load Balancing, Power Factor Correction, and Voltage Regulation Using a Static Var Compensator

by

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Abstract

This thesis presents the modelling of the FACTS device SVC for dynamical load balancing, power factor correction, and voltage regulation. The algorithm presented here is based on the Steinmetz method to balance a single phase load at the end of a 3-phase transmission line. First, a general open loop control is derived for an SVC coupled through a Y-Y or Y-D transformer, then this algorithm is tested using EMTP/PSCAD simulations. In addition, this thesis presents the design and implementation of a laboratory scale static var compensator to demonstrate the load balancing and power factor correction. The developed board connects to LabVolt bench equipment to complete the SVC system. The digital implementation of this compensator is done using a Texas Instruments microcontroller. The SVC is intended for demonstrating SVC operation and dynamic load balancing fundamentals to students.

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Dedication

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Abbreviations

3D	Three Dimensional
ac	Alternating Current
ADC	Analog to Digital Converter
AGC	Automatic Generation Control
ANN	Artificial Neural Network
ChDMA	Channel Direct memmory access
dc	Direct Current
DPF	Dynamic Power Filters
dq	Direct-Quadrature
DSP	Digital Signal Processing
EMT/PSCAD	Electromagnetic Transient / Power System Computer Aided Design
F	Farads
FACTS	Flexible ac Transmission Systems
FC	Fixed Capacitor
FFT	Fast Fourier Transform
GSA	Gravitational Search Algorithm
GWO	Grey Wolf Optimizer
H	Henries
Hz	Hertz
IGBTs	Insulated-Gate bipolar Transistors
IGCT	Integrated Gate-Commuted Thyristors
IPFC	Interline Power Flow Controller
kV	kilo Volts
l-l	line to line
max	Maximum
MHz	Megahertz

ms	Millisecond
MSC	Mechanically Switched Capacitor
MVA	Mega Voltampere
NPS	Negative-Phase-Sequence
PCB	Printed Circuit Board
PCC	Point of Common Coupling
PF	Power Factor
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
PPS	Positive-Phase-Sequence
pu	Per Unit
pwm	Pulse Width Modulation
rms	Root Mean Square
s	Second
S	Siemens (unit of susceptance)
SSSC	Static Synchronous Series Compensator
StatCom	Static Synchronous Compensator
SUVC	Static Unbalanced Var Compensator
SVC	Static Var Compensator
TCPS	Thyristor-Controlled Phase Shifter
TCR	Thyristor Controlled Reactor
TCSC	Thyristor-Controlled Series Capacitor
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TI	Texas Instrument
TSC	Thyristor Switched Capacitor
UPFC	Unified Power Flow Controller

V	Volts
VSCs	Voltage Source Converters
VSI	Voltage Source Inverter
ZPS	Zero-Phase-Sequence

CHAPTER 1 Introduction

1.1 Background

The increasing complexity of power systems has a large impact on its stability by producing different types of disturbances. The most common types of disturbances are voltage and current unbalances, voltage swings, transients and harmonics [1]. Voltage swings and current unbalances are serious problems in power systems. The effects of these types of instability result in damages to generators and protection devices. These problems have been mitigated with the use of methods and devices that are continuously evolving as is the case of the Static VAR Compensator (SVC).

There are different causes for voltage and current swings and unbalances. One of the sources for such unbalances in a 3-phase system is asymmetries in the lengths of the conductors and it is solved by transposing the conductors. However, the bigger contribution to unbalances come from unbalanced loads. Unbalanced currents from unbalanced loads are more difficult to deal with and the leading problems are significantly more harmful to a power system. Those problems include additional power losses and negative sequence currents that damage rotating machines, prevention of full line's capacity usage, voltage asymmetry, negative impact in power electronics, and generation of current harmonics [2]. In the case of voltage swings, the causes can be swings in rotor, variations of a distribution system, transformer tap-changers, and switching of reactive components [3].

Methods to mitigate voltage swings and current unbalances in use now are different from those of the past. Originally, separate devices were used to achieve control of voltage and to provide reactive power for current balancing or power factor correction. One of the well-known

technologies to deal with compensation of reactive power is the synchronous compensator, which is a synchronous motor running on no load and only supplying reactive current in order to regulate voltage. Although the machine itself is robust and capable of handling overcurrent, its dynamic response is slow and its cost is high, and due to its rotating parts, maintenance requirements are expensive. Another way to compensate reactive power is a mechanically switched bank of capacitors but these are also too slow. An old method for controlling power generation include the Automatic Generation Control (AGC) that consists of monitoring the difference between the demand and the generated power using a speed governor and other signals to generate feedback and decide if the turbine needs more or less steam/water to drive the torque of the power generator. Another device for voltage control is the Tap-Changer Control, which works as a transformer with different settings that can be adjusted online or offline depending on the type to control voltage and consequently power flow. In addition, a Phase-Shifting Transformer can be used for power flow control. These relatively "old" devices can be adjusted to control the flow of power in terms of phase, magnitude or both [4]. Some of the disadvantages of these old systems include their limited range, limited controllability, their speed of operation, which is generally slow, and they present wear and maintenance problems.

Newer technologies to deal with voltage control and reactive power compensation have appeared as a consequence of new developments in the semiconductor sector in the last two or three decades. These arrangements that blend power electronics and power systems are known as Flexible Alternating Current Transmission Systems (FACTS). What makes FACTS an interesting option is that these devices can deal with more than one issue at a time. For instance, they can both control voltage and balance load using one controller. In addition, the response time is much faster compared to old methods and since they use less moving parts their wear decreases [3]. FACTS

devices can be divided in two types; first and second generation. First generation include the Static Var Compensator and its subsystems, thyristor-controlled Series Capacitor (TCSC) and Thyristor-Controlled Phase Shifter (TCPS). The second generation includes Static Synchronous Compensator (StatCom), Static Synchronous Series Compensator (SSSC), Unified Power Flow Controller (UPFC) and Interline Power Flow Controller (IPFC)[5].

1.2 Reactive Power Supply Using Power Electronic Converters (SVCs, StatComs)

One of the ways to provide the necessary reactive power is by using fixed capacitors and inductors, however; these are fixed at a value and cannot provide dynamic compensation, unless they can be switched on and off rapidly, which is generally not possible with mechanical switching. In this section an introduction to SVC is given as well as a brief overview of StatComs. These devices are "true static equivalents of the rotating synchronous condenser" [6] in addition they are fast and do not contain moving parts.

1.2.1 Static Var Compensator

The Static Var Compensator (SVC) is a system that comprises both reactors and capacitors and with the help of power electronics it provides or absorbs reactive power in a continuous form. SVCs consist of one or a group of devices with different functions and characteristics. However, adding SVCs in a system leads to harmonic currents in the system. These harmonics are a result of controlling the thyristor controlled reactor at different angles. Normally, for symmetrical firing angles for both positive and negative cycles only odd harmonics are generated.

In order to use SVCs to provide reactive power in a three phase system, special arrangements should be made. There can be more than one topology for SVCs in a three phase system depending on the requirements. SVCs can provide leading and lagging VARs (+Q and -Q) as summarized in Table 1-1.

The classification of SVCs is as follows:

Thyristor Controlled Reactor (TCR) –It is the most important element in an SVC system, this is because it provides the flexibility of adjusting the susceptance of SVC in a continuous manner. It provides reactance only that can be controlled as a susceptance that goes from –B to zero.

Fixed Capacitor (FC) - It provides a fixed value of susceptance that is always +B thus providing positive reactive power (+Q). This capacitor(s) can be chosen to also act as a filter, which is usually the case.

Thyristor Switched Capacitor (TSC) - The thyristor switched capacitor connects banks of capacitors into the system in a discrete way (in steps). These steps can be chosen to be of equal size or in a binary way whichever works best for the needed purpose. It provides capacitance only with a susceptance that is zero or B or N times B with N as number of capacitors connected in parallel.

Static Var Compensator (SVC) System. We can have an SVC system with a combination of at least a TCR in parallel with a TSC, FC or other combinations.

Table 1-1 Reactive power compensation range of the SVC Family

	Continuous +Q	Continuous -Q	Discrete +Q
Thyristor Controlled Reactor (TCR)		X	
Fixed Capacitor (FC)			X
Thyristor Switched Capacitor (TSC)			X
Combination of (TCR) + (TSC or FC)	X	X	

1.2.2 Static Synchronous Compensator (StatCom)

The development of semiconductors has given rise to new devices in power electronics, these in turn have made possible new arrangements of FACTS devices. In this section the StatCom

will be overviewed as an example of a new FACTS device; however, other important FACTS devices are available that can provide similar compensation as the SVC.

StatComs are controllable sources of reactive power and new members ("newly developed" or second generation) of the flexible ac transmission system (FACTS). These devices are shunt connected based on VSCs (Voltage Source Converters) and improve the stability and performance of a power system. Like the SVC it controls the voltage in transmission and distribution systems, reduces voltage flicker and power oscillations, and provides reactive power compensation [4] . StatComs work by controlling reactive power into the system at their points of common coupling (PCC) with the main system. The reactive power injected into the system is managed by controlling the amount of current injected "in quadrature with the line voltage" [7] at the point of common coupling. To ride through transient unbalances, it requires an energy storage capacitor to support the dc-side voltage but unlike the SVC it does not require bulky reactors or capacitor banks [4]. Using this dc voltage generates a set of 3-phase ac-output voltages, with the necessary frequencies and phases coupled to the ac system through a device such as a transformer or reactor [4].

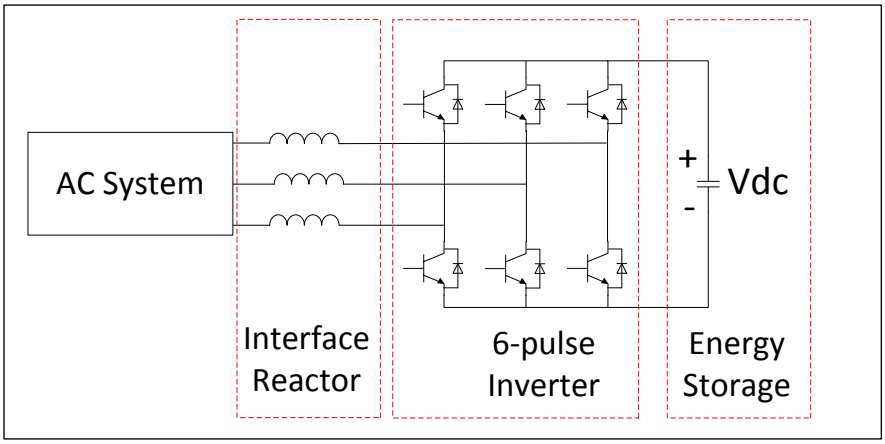


Figure 1.1 StatCom System.

A diagram of a StatCom is shown in Figure 1.1. Its main components consist of an inverting circuit, an energy storage, e.g. capacitor bank, and an interface 3-Phase reactor. The inverting circuit, better known as voltage source inverter (VSI), makes use of semiconductor switches such as insulated-gate bipolar transistors (IGBTs), integrated gate-commuted Thyristors (IGCT), or gate turn-off thyristors (GTOs). These switches are high power and can use a technique such as pulse width modulation (PWM) to limit the harmonics. In addition to providing coupling for the system, the transformer and reactor provide some filtering for harmonics generated thus making the output voltages more sinusoidal. The StatCom can be classified according to its circuit topology and examples of such classifications are the cascaded multi-level topology and the asymmetric multi-level 3H [8].

1.3 **Applications of SVC in Power Systems**

Because of its reactive power supply capability, the SVC has multiple uses; it can be used as a means for power factor correction (PFC), voltage control and load balancing. A high power factor correction is necessary to have an efficient transmission of power. Higher power factor means more power will be transmitted, making the transmission line efficient and thus saving

money. Voltage control is used to maintain a constant reference voltage at various points of the power system. Usually the control used is a closed loop proportional-integral-derivative (PID) controller. If each phase in the 3-phase ac system has a different load the ac side currents will no longer be balanced, and the unbalanced voltage drops in the network impedances will lead to unbalanced voltages as well. Load balancing is achieved by the SVC using Steinmetz's method [9] . Load balancing implies that there is a reduction or elimination of negative sequence currents in the symmetrical components[10]. Avoiding negative sequence currents helps protect power system devices such as rotating machines.

The main applications of the SVC are briefly described below.

Voltage Flickering. Voltage flickering is characterized by continuous small rapid fluctuations in the voltage supply. This is typically observed at the connection point of an arc furnace and the main ac system. SVCs are largely used in this industry because they can fix flickering as well as load balancing which is another common problem of an arc furnace.

Power Factor Correction. An ideal electrical system transmits purely active power, which happens when the angle of respective phases between voltage and current is zero. Thus by providing the correct reactive power factor to the system, an SVC can bring the power factor closer to one.

Load Balancing. It was shown by Steinmetz that an unbalanced three phase system can be made balanced by adding purely reactive elements. In this way, by having an SVC in each phase, we can calculate the amount of reactive power needed in each phase and thus balance the system.

Voltage Regulation. Traditionally, SVC is used for voltage control. The SVC can be used to keep the voltage seen by the source at a determined voltage reference. Details of voltage control are given in sections 4.2.2.

One of the most important FACTS devices is the SVC because of its reliability, cost effectiveness and overall industry proven capacities. SVC systems can be used in combination with newer technologies in order to avoid overdesign. Some industries prefer to use well developed and tested "new technologies" because it reduces the risk of catastrophic malfunctions[11]. However, even though SVCs have been around for some time, there is a lack of proper testbeds for academic use.

1.4 **Objective of this Thesis**

SVC manufacturers typically do not reveal the internal details of their control systems. Hence, one objective of this thesis is to develop a simulation model to explore the interactions within the SVC used for load balancing and voltage control. For this, it is necessary to review the different published algorithms and theories around PFC and load balancing, and select a combination of the most appropriate ones for this purpose. Using this simulation model, a lab scale prototype of an SVC capable of demonstrating power factor correction and load balancing is to be developed. Lastly, because manufacturers typically do not reveal internal details, one of the purposes is to develop an open source guideline for the design and implementation of this SVC with off-the-shelf components that can be easily replaceable because they are in general readily available.

CHAPTER 2 Literature Review

2.1 Introduction

The Static Var Compensator (SVC) has served and continues to serve numerous applications. While some authors have described the theory behind the different applications, others have focused on solving the problems that come with the installation of SVCs mainly reducing the harmonics injected into the systems by the TCR. These solutions come in the form of algorithms or topologies.

2.2 Load Balancing and Power Factor Correction

Unity power factor can be defined in various ways, simply stated it is when the supply "sees" a purely resistive load and therefore maximum transfer of power occurs. Analyzed from a phasor or symmetrical components point of view, unity power factor occurs when the current phasors are 120^{o} apart from each other and are zero degrees apart from their corresponding voltage phasor. Additionally, in symmetrical components a unity power factor means having no imaginary part for the positive sequence. With regards to load balance, an unbalanced load in a three-phase system can be defined as three loads connected in wye (Y) or delta (D) that are different in magnitude. This imbalance can be expressed in the form of phasors or symmetrical components. For phasors, a balanced system is when the three magnitudes of the three current phasors are the same and in term of symmetrical components, a balanced system is when the negative sequence is zero. These two applications of SVC, power factor correction and load balance, are often done simultaneously and many papers discuss the different ways of achieving these tasks.

2.3 **Steinmetz Circuit**

One of the most important theories addressing load balancing and power factor correction is the Steinmetz Circuit. Since its development, the Steinmetz method has been studied by various authors and its application to load balancing is crucial. Authors have offered proof of the Steinmetz method's ability to balance loads and other authors have used it as a basis to develop other techniques to balance loads and improve power factor.

Figure 2.1 Charles Steinmetz (right) with Albert Einstein [1].

The circuit consists of adding two reactive elements, an inductor and a capacitor. Figure 2.2 shows the Steinmetz circuit with the necessary values of susceptance to balance a purely resistive load. The balancing circuit was proposed by Charles Proteus Steinmetz (see Figure 2.1) and is based in the assumption that the load has no zero sequence currents and there is a balanced power supply[12].

[1] Picture taken from:http://cr4.globalspec.com/blogentry/6825/Charles-Proteus-Steinmetz-The-Wizard-of-GE-Part-1

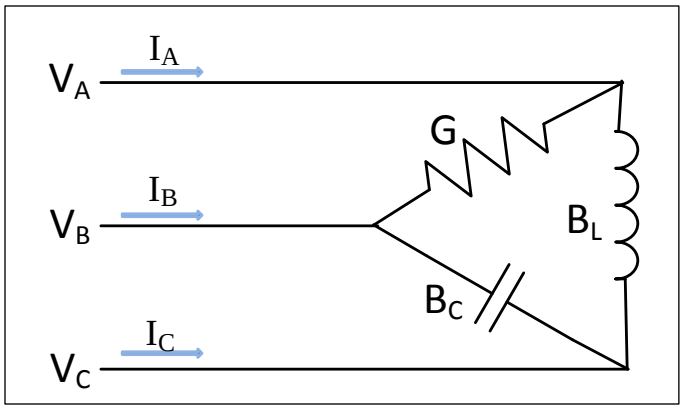


Figure 2.2 Steinmetz circuit for balancing a load using reactive components.

Where in order to have a balanced load the following is true:

$$B_C = \frac{G}{\sqrt{3}} \quad and \quad B_L = -\frac{G}{\sqrt{3}} \tag{2. 1}$$

SVCs are a more practical way to apply the Steinmetz method because of their ability to provide, given the right topology, the needed reactive power within certain limits. For example, for a single load connected across phases ab (Yab), an SVC can be connected across phases ab, bc and ca and supply the needed dynamic susceptances (B^xab,B^xbc,B^xca) in Equations 2.2-2.5 [9] .

$$Y_{ab} = G_{ab} + j\, B_{ab} \tag{2. 2}$$

$$B^x_{ab} = -j\, B_{ab} \tag{2. 3}$$

$$B^x_{bc} = \frac{G_{ab}}{\sqrt{3}} \tag{2. 4}$$

$$B^x_{ca} = -\frac{G_{ab}}{\sqrt{3}} \tag{2. 5}$$

If there were an unbalanced delta connected load, a delta connected SVC would be necessary and the compensating susceptance would be the addition of the compensating susceptances for each phase (Equations 2.6-2.8).

$$B^c_{ab} = -B_{ab} + \frac{G_{ca} - G_{bc}}{\sqrt{3}} \tag{2. 6}$$

$$B_{bc}^{c} = -B_{bc} + \frac{G_{ab} - G_{ca}}{\sqrt{3}} \quad (2.7)$$

$$B_{ca}^{c} = -B_{ca} + \frac{G_{bc} - G_{ab}}{\sqrt{3}} \quad (2.8)$$

These equations can also be expressed in terms of powers[9], [13] , line currents and line voltages , symmetrical components of currents and voltages[14] [9]. Equations (2.6-2.8) provide a simple way to balance loads and adjust power factor to unity.

2.3.1 Symmetrical Components

A second method for load balancing and power factor correction is controlling the amount of sequence currents injected into the system by an SVC either in an open loop that has dependent values for three branches of a delta SVC or by independently controlling each branch for a closed loop control.

For example, [14] uses equations that relate the compensating symmetrical currents to average values at fundamental frequency of measured reactive and active powers at the load. These compensating symmetrical currents are converted into triggering angles for the thyristors using another set of equations. Therefore, the control consists of providing the needed zero-phase-sequence (ZPS), negative-phase-sequence (NPS), and the imaginary part of the positive-phase-sequence (PPS) currents such that the system becomes balanced and has unity power factor. In addition, closed loop control can also be used to adjust symmetrical components. A proportional-integral (PI) closed loop controller can be used for the purpose of balancing a system by using as reference symmetrical values of voltage [15].

The use of symmetrical components is very useful when analyzing multiple systems with different connections for both open loop[13], [16] and closed loop type control [15], [17]. It is important to know how to derive the compensating susceptance needed from the SVC for each

type of connection since some loads are connected at the same point as the SVC and for others there may be a transformer between the SVC and the load. For the particular connection, several authors show how to derive the components needed for load balancing [10], [18]. A mathematical procedure to calculate the required compensator susceptances ($B_{ab}^{C}, B_{bc}^{C}, B_{ca}^{C}$) which are provided by the SVC and result in a fully compensated (load balance and PF of 1) system as seen from the point of connection can be found in [18]. An open loop control strategy for balancing both voltage and current that takes as inputs P, Q and V readings is also provided in this paper.

2.4 Control Systems for Implementing Load Balance and Power Factor Correction

Some of the issues that are caused by the installation of SVCs are the injection of harmonics into the system and the investment costs associated with its size. Consequently, papers have been dedicated to dealing with harmonics and minimizing the size of the SVC.

When implementing the SVC for reactive power compensation there are different types of control methods described in literature. These control methods are for different aspects of the compensation and while some authors describe different ways of obtaining the signals needed, others describe algorithms for minimizing harmonics or size, and still others describe algorithms for optimization of gains of PI control systems used with SVCs. These control methods and algorithms have been evolving over the years based on other technologies for example on speed of microcontrollers and how much memory they have.

2.5 Control Strategies

2.5.1 Open Loop Control

When implementing one of the methods for load balancing and power factor correction different aspects of it such as measurement signals and gains for controls have to be taken into

consideration. Therefore, some papers show how to implement the same theory using different control approaches. For the feedforward open loop control, the formulas above can be represented with respect to different quantities available.

For example, in [13], the authors present a compact equation where the compensating admittances are given in terms of powers (both, reactive and real) and voltages (Eqns 2.9-2.11) which are similar to the Steinmetz equations. To obtain these values, five transducers are needed; two for powers and three for voltages.

$$B_{ab}^{C} = \frac{1}{3(V^{L})^{2}}\left(3Q_{ab}^{L} - \sqrt{3}\,P_{cb}^{L}\right) \tag{2. 9}$$

$$B_{bc}^{C} = \frac{1}{3(V^{L})^{2}}\left(\sqrt{3}P_{ab}^{L} + 3Q_{cb}^{L}\right) \tag{2. 10}$$

$$\mathrm{B_{ca}^{C}} = \frac{1}{3(V^{L})^{2}}\left(-\sqrt{3}P_{ab}^{L} + \sqrt{3}P_{cb}^{L}\right) \tag{2. 11}$$

One way to obtain the necessary values from measurements is by using the rolling synchronous symmetrical component method [16]. This method results in a more precise compensation because it works even when there are distortions of voltage and current. The method uses a relation of symmetrical components to give the compensation admittance of each branch of delta connected SVC. This method uses filters and special transformations to convert distorted time dependent measured signals of line voltages and currents into symmetrical components separated by real and imaginary components; these values then go directly into Equations (2.12-2.14) to obtain the admittances required for balancing.

$$B_{ab}^{C} = -\frac{1}{3U}(Im\,I_{a_+} - \sqrt{3}\,Re\,I_{a_-} + Im\,I_{a_-}) \tag{2. 12}$$

$$B_{bc}^{C} = -\frac{1}{3U}\left(Im\,I_{a_+} - 2\,Im\,I_{a_-}\right) \tag{2. 13}$$

$$B_{ca}^{C} = -\frac{1}{3U}\left(Im\,I_{a_+} + \sqrt{3}\,Re\,I_{a_-} + Im\,I_{a_-}\right) \tag{2. 14}$$

Sometimes, these balancing admittances are divided in half in order to use two SVCs, for example when Y-Y and Y-D connected SVCs are connected together to give 12-pulse operation. Alternatively, new equations have to be obtained by dividing the amount of compensation as [14] divides the capacities of active and passive filters first then leaves part of the compensation to a D connected SVC to compensate PPS, and NPS currents and part of the compensation, that is ZPS, is left for a Y connected SVC. Here, new compensating admittances are obtained which in [14] are given in terms of powers (Q, P) and voltages (V)

Sometimes there are unbalances in a three phase four wire system and the Steinmetz method cannot directly be applied. A solution to this problem can be nullifying the current on the neutral wire and then applying the Steinmetz Method[19]. Nullifying the current on the neutral wire requires a special type of delta connected SVC explained later (section 2.6 part iii) 10-Pulse SVC).

2.5.2 Closed Loop Control

Based on the fact that load balancing and power factor correction can be achieved by setting certain parts of symmetrical components to zero or by setting a displacement current to zero, closed loop control can be used for this task. For example, [17] describes a PI controller designed to maintain the sequence currents at the reference setting depending on the amount of balancing and power factor correction desired. This method uses αβ transformations to transform rotating sets ia,ib,ic axis into stationary two set axis. It applies another transformation to convert the stationary αβ into synchronously rotating axes i_d and i_q. The DC negative sequence components (i_{dn} and i_{qn}) are extracted using low pass filters. The output of the proportional integral control system provides the signal to make i_{dn} and i_{qn} zero. Simulations show that this method can balance the following types of unbalances.

Type I: Single phase connection in a three phase system.

Type II: Double phase connection in a three phase system (on ‘a’ and ‘b’ phase sections.)

Another paper that uses a PI controller for balancing is [15]. The PI controller is used as a method to independently manipulate sections of the symmetrical components; by using a PI for each part of the symmetrical components, one can individually control the positive sequence (PS) voltage, negative sequence (NS) voltage, or PS and NS voltage together. The PI uses *dq0* (direct-quadrature-zero) components of voltage as reference to control the susceptance of the TCR (Btcr) from a B_{min} to a B_{max}, these compensating admittances are then translated into the firing angles used for the triggering pulses. Even though the paper describes the control of voltage symmetrical components this can be used for the control of current symmetrical components as well.

Another method for load balancing and power factor correction is by controlling a displacement current phasor [20]. For this method, a phasor called displacement current (Id) is defined as a displacement from a desired state of current phasors that represents a balanced load with unity PF. The condition for a balanced system is that “any two line currents are equal in magnitude and phase displaced by $120^{o"}$ [20]. Therefore, the control consists of keeping Id as close to zero as possible by means of an SVC and closed loop control. This control as described by the author is for an unbalanced load across phase ab in the arrangement described by Figure 2.3 where the inductor has been replaced by a TCR and the capacitor by a TCR-FC.

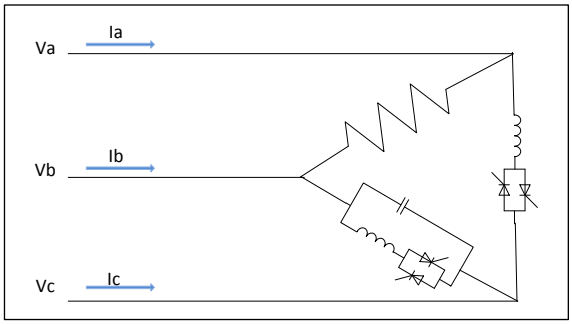


Figure 2.3 Dynamic Steinmetz Circuit.

2.5.3 Other Types of Control

i) Combined Control

There can also be controllers that are a combination of open and closed loop control. For example, [21] describes a method of compensation based on the Steinmetz method because it is fast but includes a PI controller for slow correction to eliminate steady state unbalance errors. The values needed for the balancing admittances are; fundamental negative and positive sequence of current and fundamental positive values of voltage which are obtained from line voltage and current measurements, this is also obtained using a transformation from *abc* to *dq* axes.

The second set of balancing susceptances comes from a PI closed loop control based on voltage. These two sets of balancing susceptances are added to form "the balancing susceptances". According to the author, this combined type of control of open and closed loop form a more complete and stable compensation technique.

ii) Cooperative Control

In cooperative control, SVCs work around preinstalled equipment to provide reactive power. In this context, an SVC is used for load balancing and power factor correction but its control becomes more complicated since it is not the only device assigned for a task and it can conflict

with the control of other devices[22]. A theoretical background for the operation of SVC in an environment of "cooperative control" is given in [22].

2.5.4 Optimization Algorithms

The algorithms presented in this section are summarized in Table 2-1

Table 2-1 Optimization algorithms

	Algorithm	Function	Type of Control
1.	Size Optimization	Minimize SVC size	Open Loop
2.	Grey Wolf Optimization (GWO)	Minimize control gains of a PI	Closed Loop
3.	Gravitational Search Algorithm (GSA)	Minimize THD	Open Loop
4.	Artificial Neural Network (ANN).	Minimize TDD or size	Open Loop
5.	golden search routine (GSA)	Minimize energy	Open Loop

Size Optimization can be applied when full PF correction and/or load balancing is not needed. When using Steinmetz Circuit for power factor correction and load balancing limits can be applied to reduce the capacity of the SVC needed. The limits can be set for a range of power factor correction, level of balancing or both resulting in a minimization of the components. Results show that there is a significant reduction on the capacity needed for the SVC. A reduction in capacity of up to 50% of full balancing based on Steinmetz method can be achieved using this method [23].

The Grey Wolf Optimizer (GWO) algorithm is used to optimize the control gains of a PI SVC controller. GWO “is a meta-heuristic that mimics leadership order and preying behavior of grey wolves in a group (Canis lupus)” [24]. The PI with values obtained from the GWO regulates

the firing angles from an alpha minimum (α_{min}) to alpha maximum (α_{max}) which for these thyristors is from 90^o to 180^o and have as reference a voltage (ΔVref(s)). The components of the control are a transfer function for the PI regulator, limiting function for minimum and maximum values of firing angle, a thyristor firing delay transfer function and a phase sequence delay transfer function. The output of the control block is a value for susceptance ΔBsvc(s). The modeling equations are based on power and energy functions. This is used for power factor correction and load balancing.

The gravitational search algorithm (GSA) technique uses feedforward open loop control to balance loads and improve power factor. The control consists of obtaining balancing reactive powers instead of balancing susceptances from inputs of measured powers in Equations 2.15-2.17. Then the compensating reactive powers Qab, Qbc, Qca, are converted into firing angles using Equation 2.18. This equation has no single solution and therefore GSA is applied to obtain the firing angles with minimum total harmonic distortion (THD). Optimization indices are computed offline for their use in online compensation [25].

The compensating reactive powers for a Y connected SVC are given by [25]:

$$Q_a^T = Q_{La} - Q_f - Q_s + \frac{P_{Lc} - P_{Lb}}{\sqrt{3}} \quad (2.15)$$

$$Q_b^T = Q_{Lb} - Q_f - Q_s + \frac{P_{La} - P_{Lc}}{\sqrt{3}} \quad (2.16)$$

$$Q_c^T = Q_{Lc} - Q_f - Q_s + \frac{P_{Lb} - P_{La}}{\sqrt{3}} \quad (2.17)$$

$$Q_{ab} = \left[\frac{2\pi - 2\alpha - sin2\alpha}{\pi\chi^0}\right] 3V_1^2 \quad (2.18)$$

"Where: χ^0 is the reactance for full conduction of thyristor (α=0) and V_1 is the per phase fundamental component of TCR" [25].

Another algorithm for minimizing harmonics or reactive power supplied when providing reactive power compensation is the artificial neural network (ANN). Before applying ANN, an

open loop control is used to calculate the balancing susceptances [26]. These equations are similar to those in Equations 2.15-2.17 and use the same firing angle relationship as in Equation 2.18 but it is given in terms of susceptances. Therefore, similarly to the previous algorithm, this equation has multiple solutions and a fuzzy logic algorithm is used to determine the possible operating states and create an index based on the total demand distortion (TDD) to later select the best one. Finally, an ANN controller is trained using outputs given by the fuzzy logic and this speeds up the process of calculation and optimization enough to use this algorithm on real time control. Moreover, this algorithm can be set to minimize TDD or to minimize the SVC capacity (Qs).

Lastly, the golden search routine can be used in a control approach related to "energy distribution principle" to optimize the "energy usage in an electrical network". GSA is used on a "cost equation" to find a minimum energy point from all possible firing angles of the thyristors between 90^{o} to180^{o} [27]. This routine successively iterates and calculates the currents that need to be supplied by the SVC.

These optimization algorithms offer better results for load compensation, however, one of the downsides is that the time taken for computation in the algorithms may be higher than the desired time for compensation. For example, the total time to perform the ANN compensation algorithm is 0.65s in average which is higher than a half 60 Hz cycle. It is desired to have a time less than half cycle because that is how fast the firing angles can change. Moreover, such algorithms may be too complicated to be implemented on-line on a digital platform not only in terms of size but also in terms of processor speed needs.

2.6 **Topologies for Reactive Power Compensation and Voltage Regulation**

Starting from the fundamental building blocks of an SVC (FC-TCR and TSC-TCR), special arrangements can be made to improve aspects of the system's design such as harmonic reduction and minimization of SVC components in a three phase system.

i) TSC Banks

Capacitor banks can be switched into the system by a thyristor in order to supply reactive power. In a three-phase system these banks can be connected in a delta or wye form and they can have N number steps. Figure 2.4 shows a TSC delta connected with 3 steps [6]. Every step added to a phase can have the same rating or it can be binary based [4].

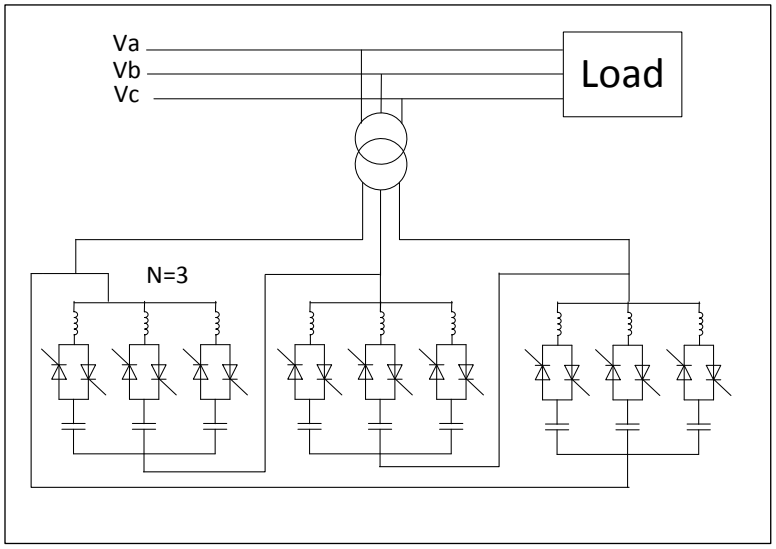


Figure 2.4 Thyristor switched capacitor banks.

ii) 6-Pulse SVC

The number of pulses traditionally refers to the number of TCRs being used. A common topology that gets its name this way is the 6-pulse SVC. A 6-pulse SVC is used in a 3-phase system to control the amount of reactive positive or negative power injected. Depending on the range of reactive power desired, the SVC connections may include FC-TCR[9] (Figure 2.5) or TSC-TCR

per phase. These connections can be made in delta or wye form. Figure 2.5 shows a 6-pulse FC-TCR type of SVC and it can be observed that there are three TCRs being used (1, 2, and 3 in the figure) but for every TCR two firing pulses are needed thus the 6-pulse name. FC-TCR is one of the best solutions for controllable VARs, it is economical and gives the necessary performance and reliability[6] .

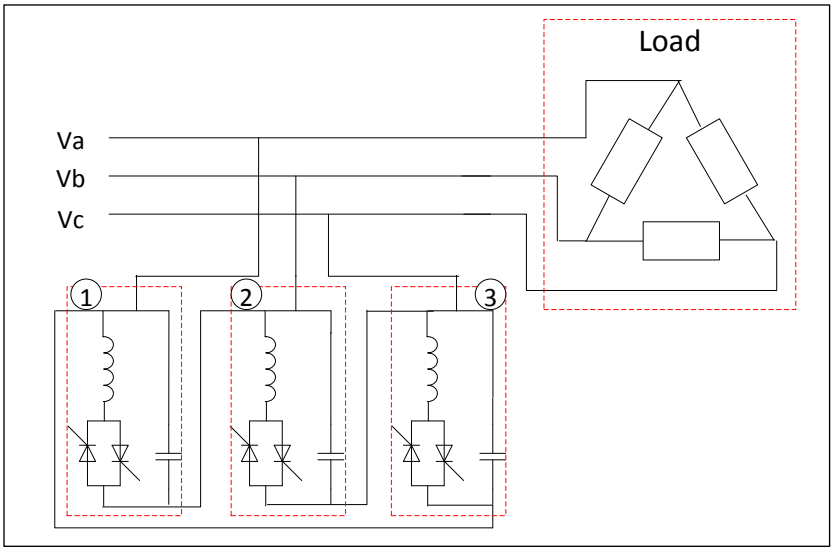


Figure 2.5 6-pulse FC-TCR 1) BCab, 2) BCbc, 3) BCca.

iii) 10-Pulse SVC

Steinmetz method and SVCs can be applied to four-wire loads by nullifying the current of the neutral wire with the help of a 10-pulse SVC (Figure 2.6) or Static Unbalanced VAR Compensator (SUVC) [19]. Two sections of the SUVC have the purpose of making the current in the neutral zero. The other three sections work as a regular 6-pulse SVC. Simulations and lab scale results in [19] show the efficiency of this proposed method/topology.

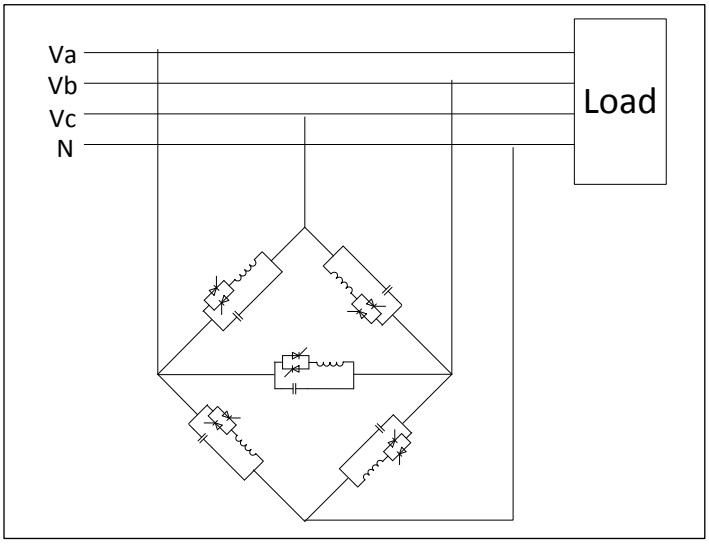


Figure 2.6 Static Unbalanced Var Compensator (SUVC).

iv) 12-Pulse SVC

Another delta connected arrangement is the 12-pulse SVC [28] (Figure 2.7). The 12-pulse SVC is a topology that consists of a Y-Y and Y-D transformer that connect to the main system as shown in Figure 2.7. It consists of two delta connected SVCs comprising six TCRs in total therefore requiring 12 pulses, two for each TCR. One of the main advantages of having a 12-pulse SVC is to get rid of some harmonics. The third harmonic is eliminated by the delta connection and harmonics of order $n\pm1$ (5^{th} , 7^{th} , 19^{th}, etc.) are cancelled by the 30^{o} phase shift between the Y-Y and the Y-D windings, leaving only higher order harmonics of order $12n\pm1$ [12].

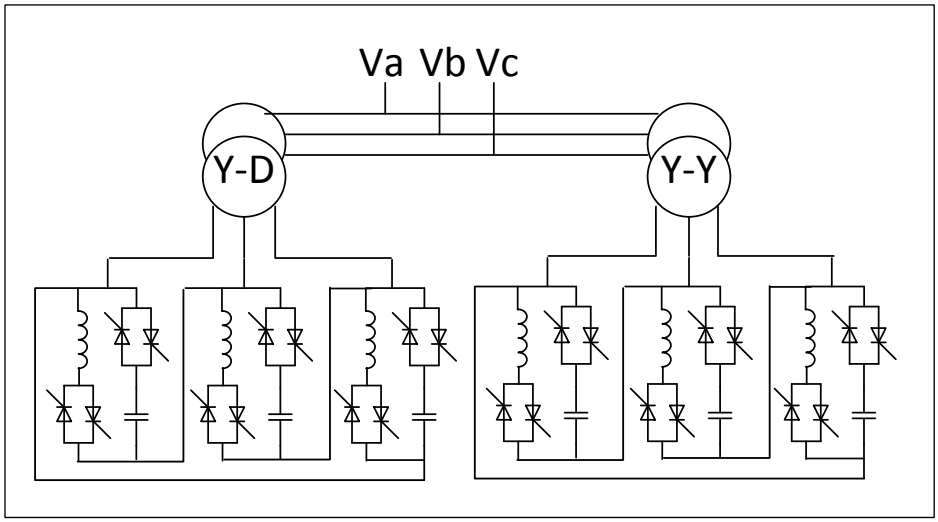


Figure 2.7 Twelve pulse SVC with double transformer.

There are alternative methods for twelve pulse arrangements using a single transformer. Figure 2.8 [29] shows a 12-pulse arrangement for its use in a three-phase system with the objective to reduce/eliminate the 5th and 7th order harmonic currents. This 12-pulse arrangement uses a delta connected TCR and a wye connected TCR.

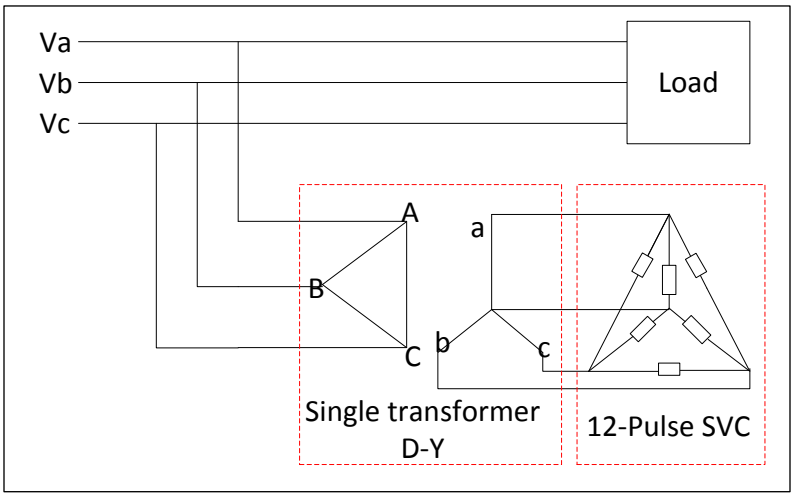


Figure 2.8 Alternative 12-pulse SVC with single transformer.

There are many advantages to this arrangement, primarily the use of one transformer instead of two. This single transformer is able to eliminate the 5^{th} and 7^{th} harmonics at the junction

of the two subsystems. Additionally, transformer losses are lower (about 0.1 pu) and the system works for different unbalance scenarios and degrees of unbalance [29]. The test system is designed to keep the line voltage disturbances up to 10% caused by any changes in the load characteristics.

v) Hybrid Arrangements

Hybrid arrangements can be made by using an SVC together with an older technology, e.g. synchronous generator (SG), or a newer technology, e.g. voltage source converter (VSC). These combinations result in topologies such as the SVC+SG[24] , and SVC+VSC [14], [27]. In these cases, the SVC can play the main role supplying most of the compensation or it can play a secondary role delivering reactive power shortage in addition to the reactive power from other devices.

An example of a hybrid system with an SVC being used as the main supply of reactive power and a newer technology playing a secondary role is shown in Figure 2.9 [30]. This topology can be used as a combined power compensation method for load balancing and voltage flicker. This structure includes a delta connected SVC for reactive power control, passive filters and an active filter. The active filter enhances the performance of the passive filter while reducing the harmonics at the connection point with the source or loads and can be connected in series with the source or with the passive filter.

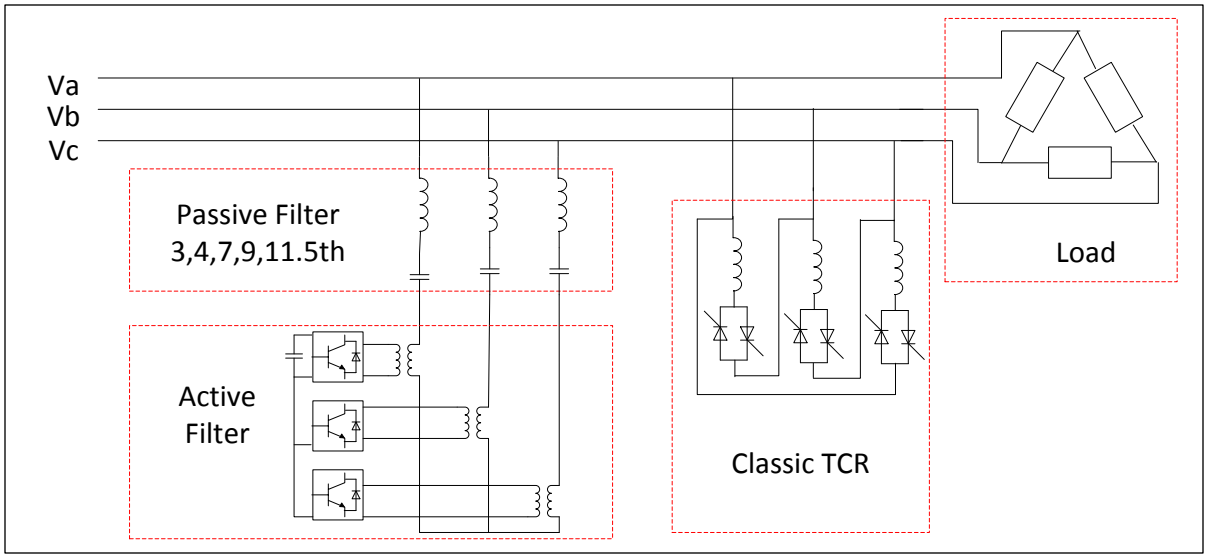


Figure 2.9 Hybrid system combining classic TCR, passive and active filters.

The passive filter consists of 3rd, 5th, 7th, 9th, and 11th single tuned filters. Additions of active filters represent a small percentage of traditional passive filters with percentages as low as 2% of the passive filters. The addition of the active filter reduces the rms values of the harmonics while keeping the same power factor improvement as compared to the classic SVC [30].

Another arrangement of a hybrid structure is shown in Figure 2.10. This arrangement places delta connected fixed capacitors in parallel with the TCR instead of placing them in series with the active filter. Another difference is that in this arrangements the active filter is connected through a transformer. This topology can effectively be used for power factor correction and load balancing. First a compensation stage with an SVC is used and for extra filtering a three phase dynamic power filters (DPF) is used [27].

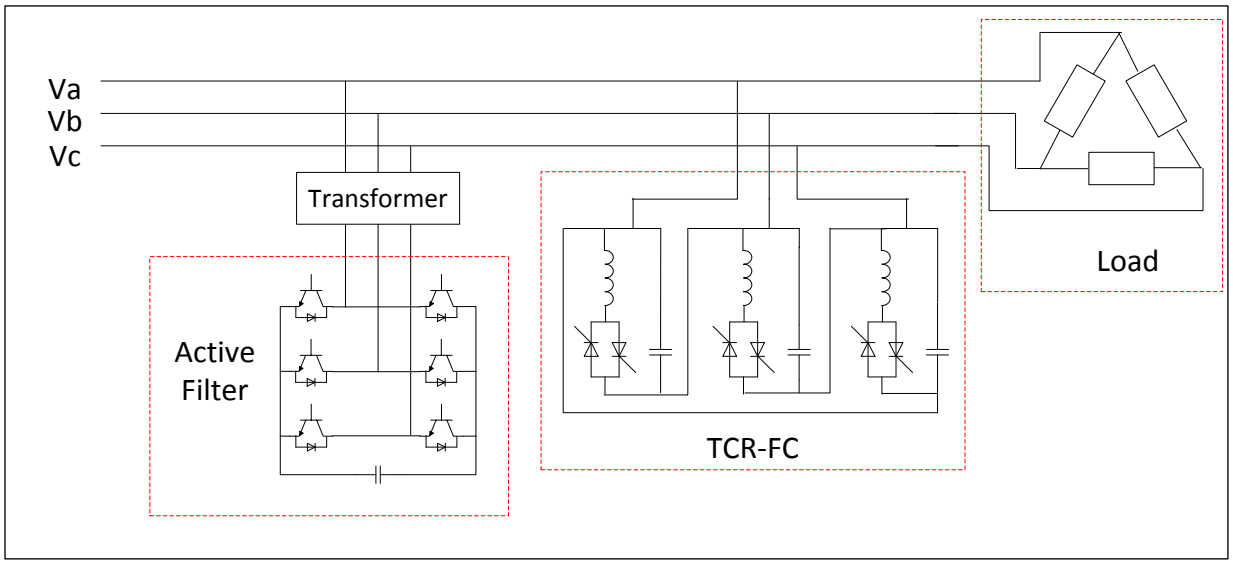


Figure 2.10 Hybrid system combining TCR-FC and an active filter.

vi) System-SVC-Load Connections

Special connections are needed for large loads such as those used in electric trains. The SVC is connected to the ac system through a transformer. The load can be either directly coupled to the ac system or through a transformer.

For example, Figure 2.11 illustrates a method to connect an electric train and an SVC consisting of fixed capacitors and TCRs to the power system [21]. In this topology the SVC (type FC-TCRs) is coupled (through a D-Y transformer) to the transformer of the electric train and another set of FCs are connected at the side of the load. The FCs on the SVC side contain three and five times filter branch to filter the harmonics coming from the SVC. The extra set of filters contain three, five and seven times filter branch to filter the harmonics coming from the load and they are connected in a wye configuration. The set of SVC, FC and traction load are coupled into the main ac system through another Y-D transformer.

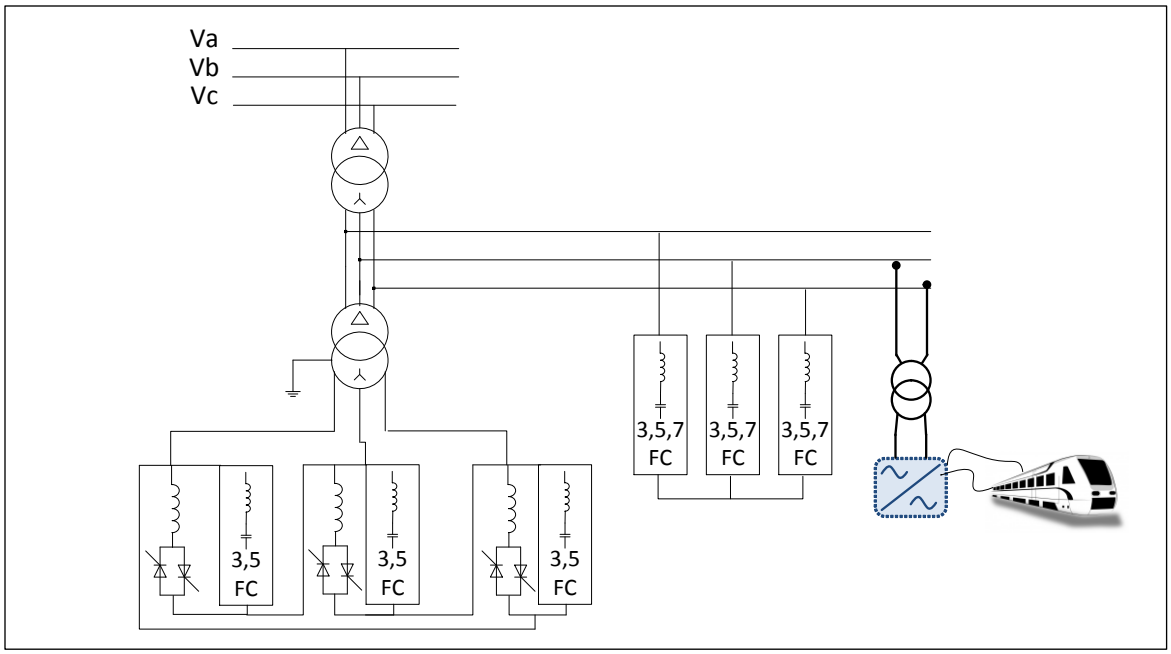


Figure 2.11 Electric train connection to SVC and system through intermediate stage.

Another two examples of system-svc-load connections are illustrated in Figure 2.12 [31]. These two types of connections are 1) Power traction transformer directly to the grid (Figure 2.12 a)) and 2) Power traction with intermediate level (Figure 2.12 b)). Both of these topologies can be used as a means for power factor correction and load balance in electrical traction systems. However, having an intermediate level allows for better handling of the harmonics from both load and SVC in addition to maintaining the track voltage at a reference. In contrast, having a direct connection makes it harder to handle the harmonics coming from the SVC and the load.

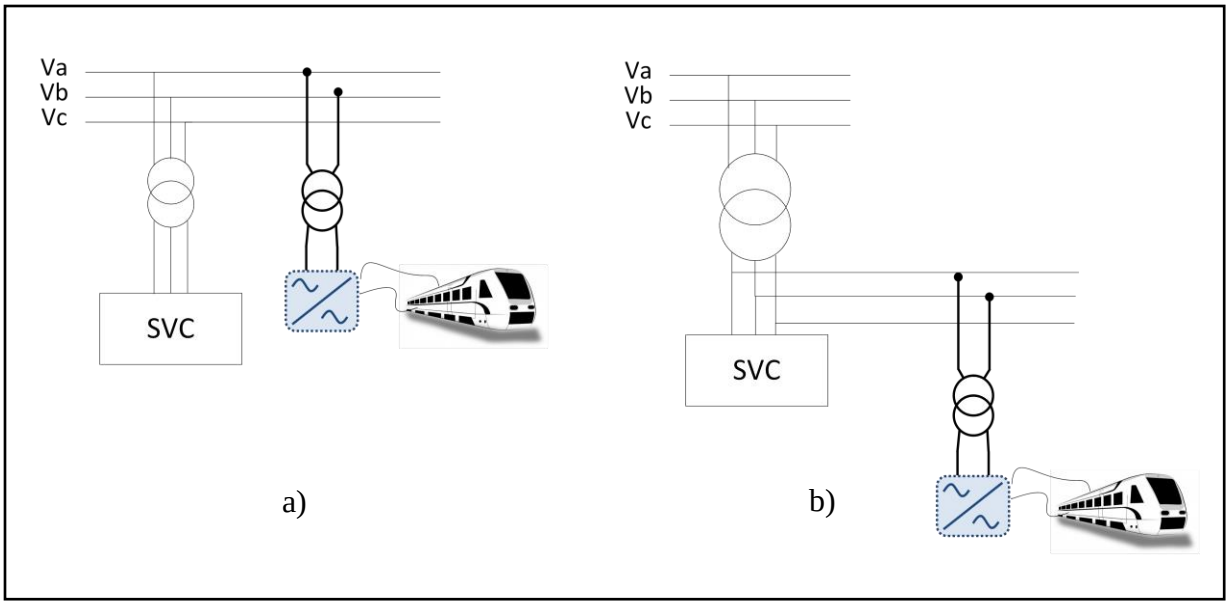


Figure 2.12 Electric train connection; a) direct connection and b) intermediate stage.

CHAPTER 3 Reactive Power from Static VAR Compensators

This chapter gives an overview of the basics of reactive power and its influence on the transmission of active power. Moreover, it describes each subsystem of the SVC and the process to generate any amount of reactive power needed (in a controlled manner) which could be lagging or leading. Furthermore, some of the critical issues caused by the use of the SVCs are specified. One of the load balancing techniques will be discussed and studied in Chapter 4.

3.1 Reactive Power

The flow of power in an electrical system can be represented by a phasor diagram with active and reactive components of power as shown in Figure 3.1[4]. It can be seen by the diagram that the total power phasor can be adjusted in both magnitude and phase by adjusting the lagging and leading reactive powers.

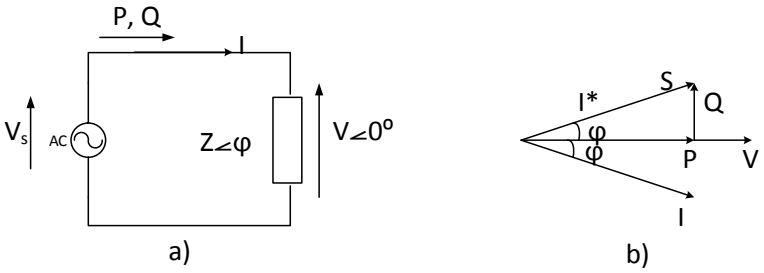


Figure 3.1 Power transfer in ac system. a) Power system b) Phasor representation.

The complex power is written in the form:

$$S = \bar{V} \cdot \bar{I}^* = P + jQ = VIcos\theta + jVI\ sin\theta \quad (3.\ 1)$$

$$PF = \cos(\theta) \quad (3.\ 2)$$

The SVC (with TCR and TSC elements) is capable of providing both leading and lagging reactive powers, thus it is able to control the total complex power in a system up to a certain rating. This feature is very useful when dealing with disturbances to the electric system that need dynamic reactive power. Research has shown throughout the years the different uses of the SVC. The different components of an SVC provide different values in different forms of reactive power. This controllability of reactive power is what makes SVCs very dynamic and useful.

3.2 **Thyristor Controlled Reactor (TCR)**

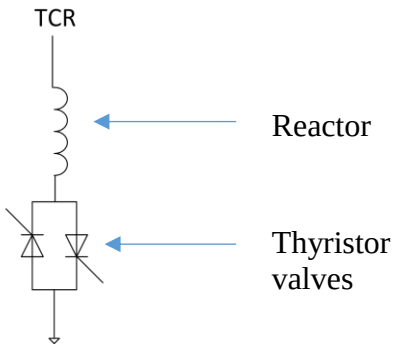


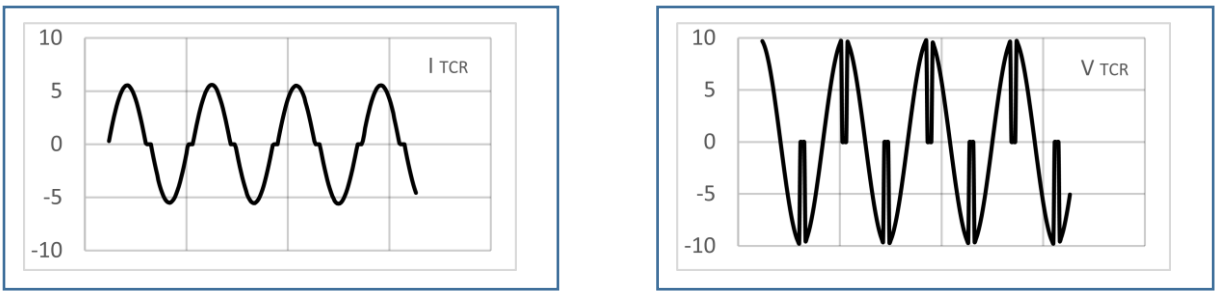
Figure 3.2 Thyristor Controller Reactor (TCR).

One of the most important devices in the Static Var Compensator (SVC) is the Thyristor Controlled Reactor (TCR) illustrated in Figure 3.2 because of the ability to continuously control its reactance. The reactance in the TCR is regulated by controlling the current through the reactor.

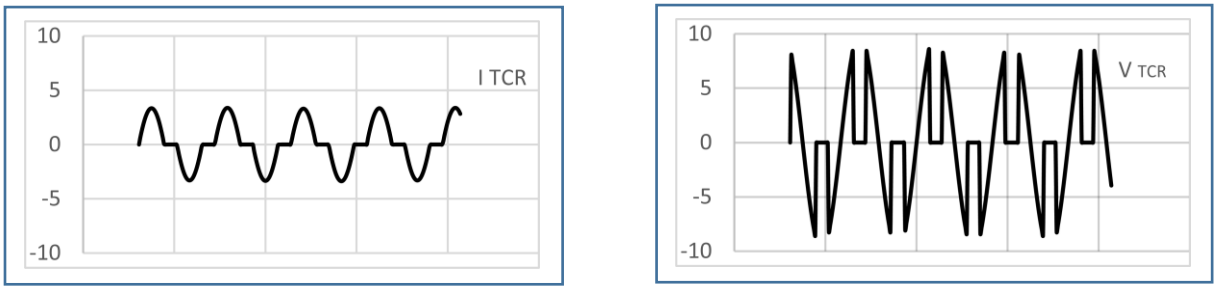
The thyristor conducts current when it is on (when it is fired) and stops conducting when the conducting current reaches zero. The exact moment when the thyristor is set on with respect to the voltage phase is known as the “firing angle”. In the TCR topology, the current through the inductor is always symmetrical with respect to the voltage zero crossing as observed in Figure 3.3. This is because the current is proportional to the integral of the voltage as indicated in equation

3.4. Figure 3.3 shows the current and voltages across a TCR with different firing angles obtained from SVC simulations in PSCAD (EMTP).

a) α=100°



b) α=120°



c) α=160°

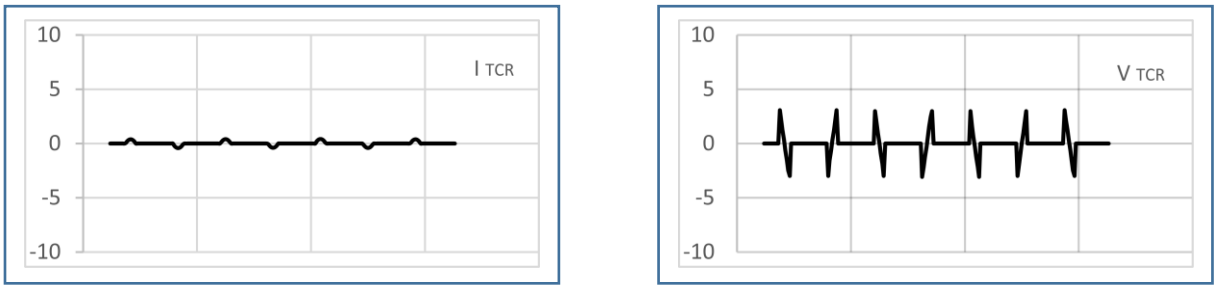


Figure 3.3 Current and voltage through the inductor for firing angles (α).

The equations for the TCR current are as follows [4]:

$$L\frac{di}{dt} - v_s(t) = 0 \tag{3. 3}$$

L is the inductance. By integrating (3.3)

$$i(t) = \frac{1}{L}\int v_s(t)dt + C \tag{3. 4}$$

Where C is the constant of integration

Alternatively,

$$i(t) = \frac{\mathrm{V}}{\omega L}\cos\omega t \ + C \tag{3. 5}$$

For the boundary condition, $i(\omega t = \alpha) = 0$,

$$i(t) = \frac{V}{\omega L}(\cos\alpha - cos\omega t) \tag{3. 6}$$

Where α is the firing angle.

It is evident by observing the waves in Figure 3.3 that the resulting current contains harmonics and their magnitude depends on the firing angle. Thus, it means that the firing angle influences two things; the fundamental component of the current and the level of harmonics injected.

The fundamental component of the current (I*l*) through the inductor with respect to firing angle (α) can be found by Fourier analysis and it has the form of Equation (3.7) [9] .

$$Il(\alpha) = \frac{V}{\omega L}\frac{2\pi - 2\alpha + \sin(2\alpha)}{\pi} \tag{3. 7}$$

From equation 3.7 the relation of the susceptance (B_{TCR}) to the firing angle (α) is [9]:

$$B_{TCR}(\alpha) = B_L\frac{2\pi - 2\alpha + \sin(2\alpha)}{\pi} \tag{3. 8}$$

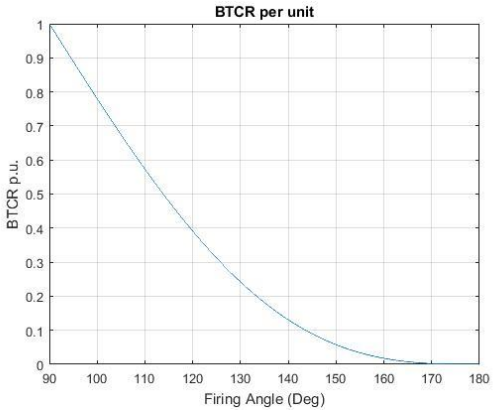


Figure 3.4 B_{TCR} pu as a function of firing angle.

Figure 3.4 is a graphical representation of Equation 3.8 in per unit and shows that the maximum reactance is obtained at the 90º firing angle and the minimum at 180º. Angles outside the range of $90^o < \alpha < 180^o$ must be avoided to prevent unwanted results such as a dc component [12].

The firing angle of the TCR generates harmonics in the system except 90º at full conduction and 180º at no conduction. All other firing angles produce some amount of harmonics illustrated in Figure 3.5 and given by Equation 3.9 [12].

$$Ih(\alpha, n) = \left|\frac{V}{\omega L}\frac{4}{\pi}\left(-\frac{1}{n}Cos[\alpha]Sin[n\alpha] + \frac{1}{2}\left(\frac{Sin[(n-1)\alpha]}{n-1} + \frac{Sin[(n+1)\alpha]}{n+1}\right)\right)\right| \qquad (3.9)$$

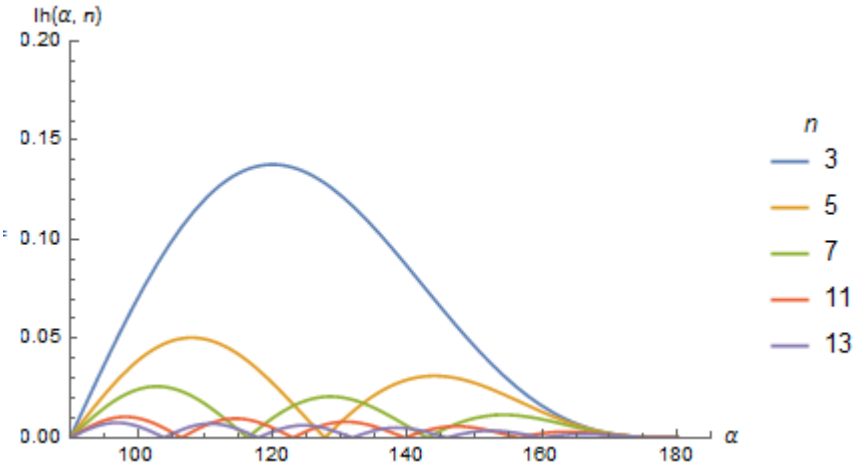


Figure 3.5 Magnitude of TCR harmonic currents (pu) with respect to firing angle.

3.3 **Fixed Capacitor (FC)**

The fixed capacitor is a capacitor permanently connected in parallel with a TCR. Thus, it has a fixed value that can be arranged and tuned to act as a harmonic filter. Since this capacitor is always connected, there are no harmonics from this device and its equivalent susceptance is a fixed amount (B_C).

3.4 Thyristor Switched Capacitor (TSC)

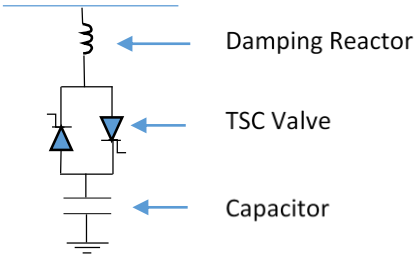


Figure 3.6 Thyristor Switched Capacitor (TSC).

In this arrangement, one or more capacitors are discretely connected using thyristors with a firing pulse that is always on or off. A damping reactor can be used in order to avoid large influx currents, The damping reactor can be carefully chosen in order to be used also as a filter [12].

Switching on and off capacitors using thyristors is a process that requires caution to avoid undesired behavior. In order to avoid transients, capacitor banks are switched on when their voltage and the system's voltage reach a minimum difference. Consequently, the maximum time delay is half a cycle for turning on capacitors. In addition, inrush currents and resonances with the system are avoided by including a damping reactor in series with the capacitor as shown in Figure 3.6. Another aspect to take into account when turning on a capacitor is the amplification factor (Equation 3.10) and the resonant circuit it creates with the inductor [12].

Amplification factor:

$$B_{TSC} = \frac{B_C\, n^2}{n^2 - 1} \tag{3. 10}$$

Sometimes the capacitors can be switched in/out with a mechanical switch, in this case the arrangement is known as Mechanically Switched Capacitor (MSC).

3.5 **The Complete SVC System**

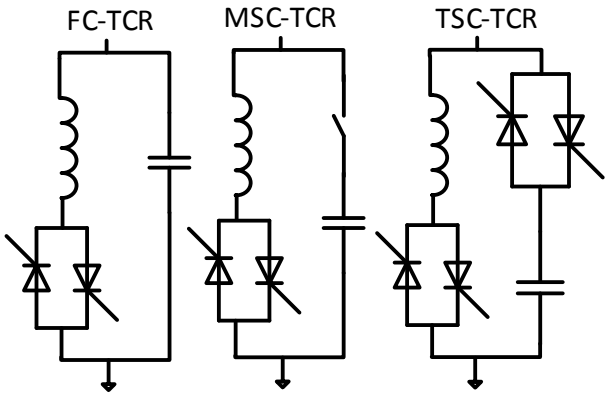


Figure 3.7 SVC systems.

In order to achieve a range of reactive power, which can go from negative to positive, a combination of reactors and capacitors is required with such combinations shown in Figure 3.7 [4]. This includes the FC-TCR, MSC-TCR, and TCR-TSC. The total susceptance of the system is the sum of the parallel connections of each subsystem. Since the capacitors are turned on in discrete values the total susceptance will be controlled by the TCR. If the FC is used in parallel with a TCR the total susceptance is $B_{SVC}=B_C+B_{TCR}$. When there is more than one TSC there must be an overlap area between switching capacitors on and off to avoid excessive switching [12]. Figure 3.8 shows the susceptance Bsvc of the system with respect to the $B_{TCR.}$

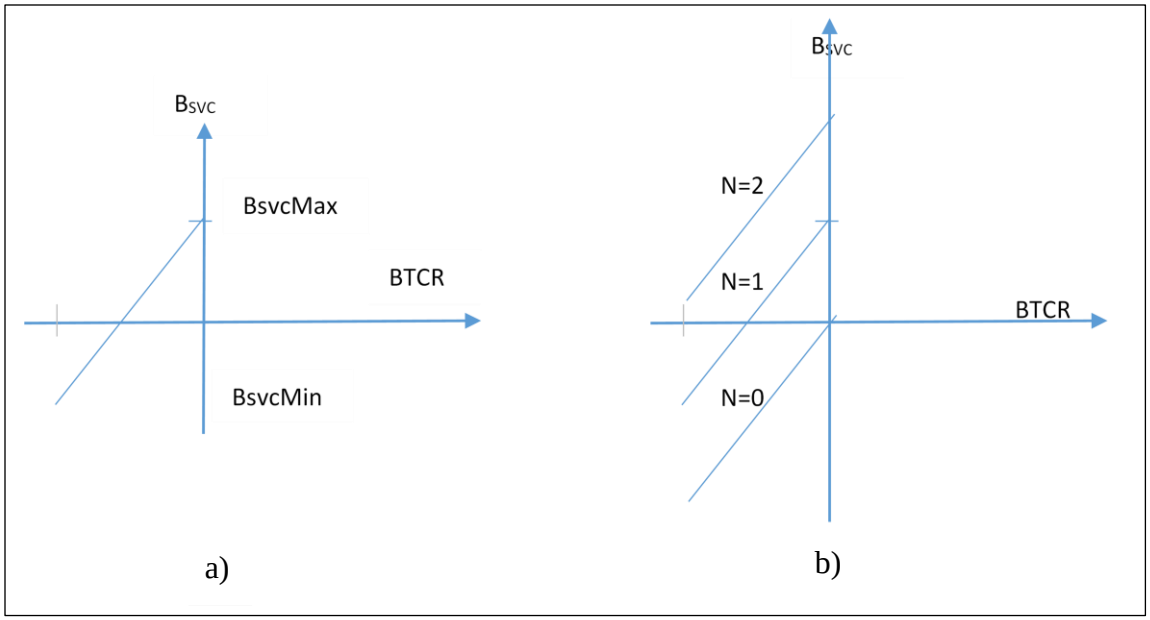


Figure 3.8 Reach of SVC systems. a) TCR-FC, b) TCR-TSC.

The upper and lower limits of susceptance for the two different types of SVC systems in Figure 3.8 are given by the following equations:

For FC-TCR

$$B_{SVC}Max = B_C \rightarrow \alpha = 180^o \quad (3.\ 11)$$

$$B_{SVC}Min = B_C + B_L \rightarrow \alpha = 90^o \quad (3.\ 12)$$

For TSC-TCR is:

$$B_{SVC}Max = B_C \rightarrow \alpha = 180^o \quad (3.\ 13)$$

$$B_{SVC}Min = B_L \rightarrow \alpha = 90^o \quad (3.\ 14)$$

As we can see in Figure 3.8, the reach of the SVC is larger both capacitive and inductive when TSCs are used.

3.6 **Voltage-Current Characteristics of the SVC**

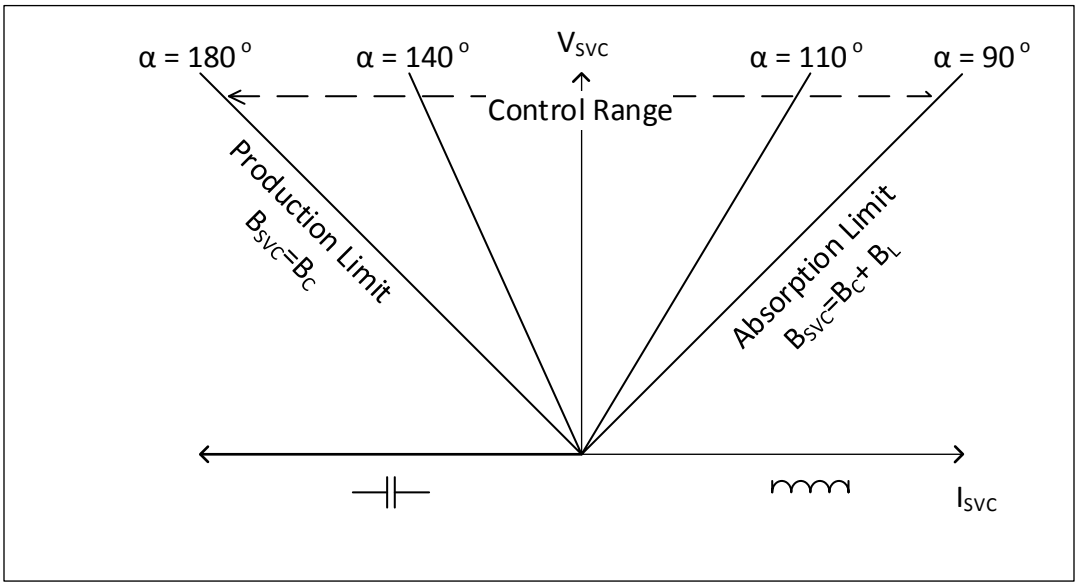


Figure 3.9 Voltage-Current Characteristics of an FC-TCR SVC.

The voltage-current characteristics of a FC-TCR SVC is shown in Figure 3.9. The absorption limit is when the TCR is operating at full capacity so the total susceptance of the SVC is the combination of the capacitive and inductive susceptance. If the inductive susceptance is double as that of the capacitive then we can have equal amount of production as of absorption. In the case of a TSC-TCR, it is not necessary to have double the inductive susceptance because the capacitor can be switched off which allows a greater range of the absorption limit.

3.7 Chapter Conclusions

In this chapter, the basics of the operation of the SVC both as individual parts and as a system were described. In order to have both lagging and leading reactive power it is important to have fixed capacitors or thyristor switched capacitors in parallel with the TCR. However, the controllability of susceptance in a continuous form comes from the control of the TCR, for this reason, the TCR is the most important element of any SVC.

After discussing about the basics of the SVCs and the types of control for load balancing, the next chapter describes a control algorithm based on Steinmetz Method used for different studies and validated by EMTP/PSCAD simulations.

CHAPTER 4 Electromagnetic Transients (EMT) Simulation Model of SVC

This chapter discusses the derivation of an open loop control system designed in this thesis for load balancing and power factor correction of a 3-phase system using a 6-pulse SVC. To validate this algorithm, simulations performed using an EMT program are presented. All the blocks used and developed for the simulation are explained. Different scenarios with different levels of unbalance are given to properly test the algorithm and capabilities of the SVC.

In addition, the load-balancing controller is further enhanced with the addition of a voltage control function via a closed-loop Proportional-Integral (PI) control system.

The purpose of doing simulations

The algorithm developed is tested through simulations in EMTP/PSCAD simulations are provided as a means to verify the algorithm developed, study system characteristics and behavior and benchmark the topologies. First, the PSCAD blocks used are illustrated and briefly described. Second, the derivation of open loop control algorithm is given. Third, a general overview of the study cases is defined. Last, the simulation results are presented for the cases; load balancing with a 6-pulse and 12-pulse SVC, and enhanced voltage control with load balancing by a 6-pulse SVC.

4.1 System Architecture

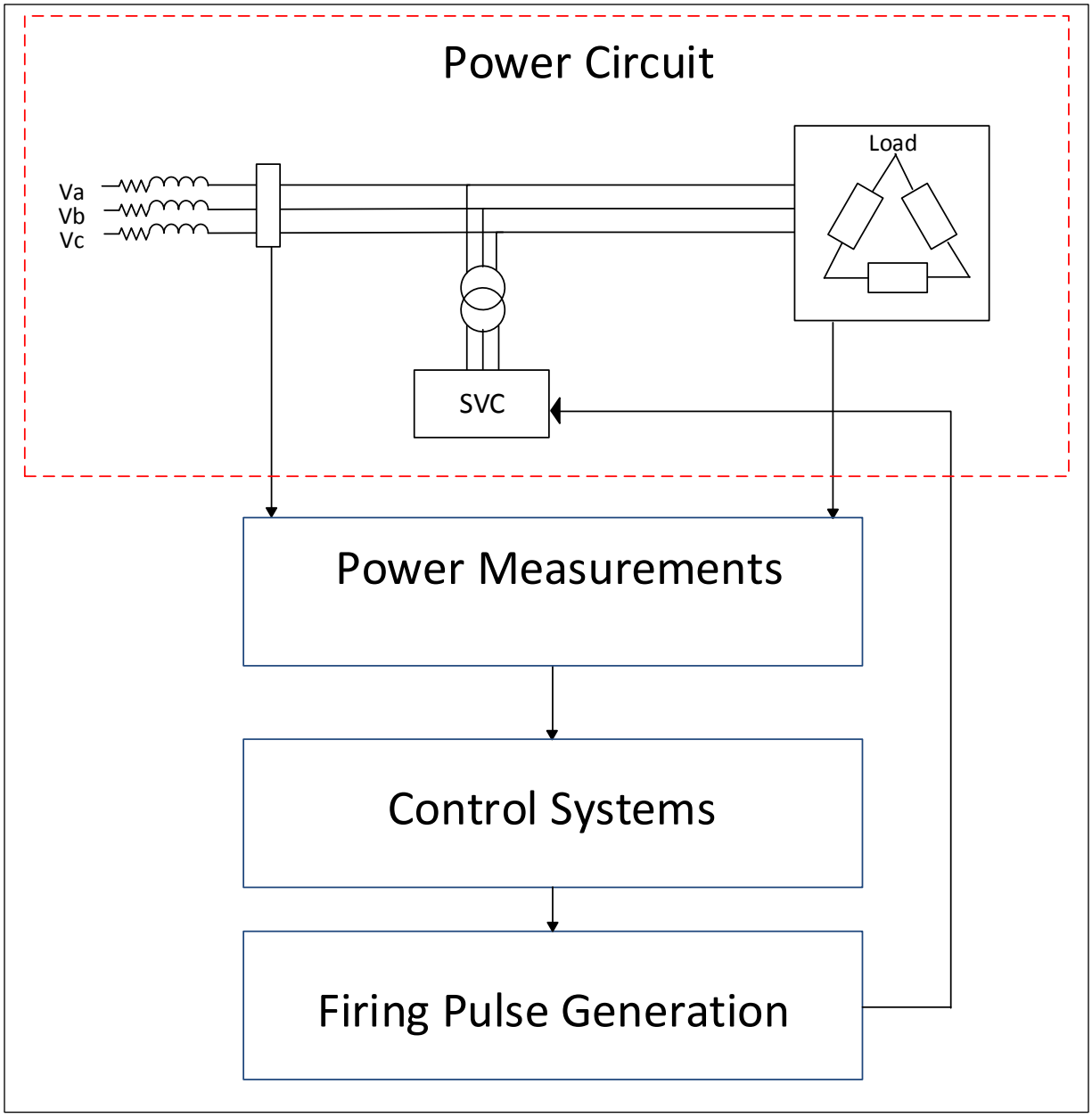


Figure 4.1 System architecture used for EMTP/PSCAD simulations.

4.2 Simulation Blocks

Simulations of an SVC were implemented using PSCAD software. The source is a 210 V rms 3-phase supply, the transmission line is modeled as a source resistor and an inductor, the load is connected in delta form, and for the SVC the TCR has an inductor of $6.01X10^{-2}$ [H] and two TSCs of $6.5X10^{-5}$ [F] capacitors. The single-line diagram of the system is shown in Figure 4.2.

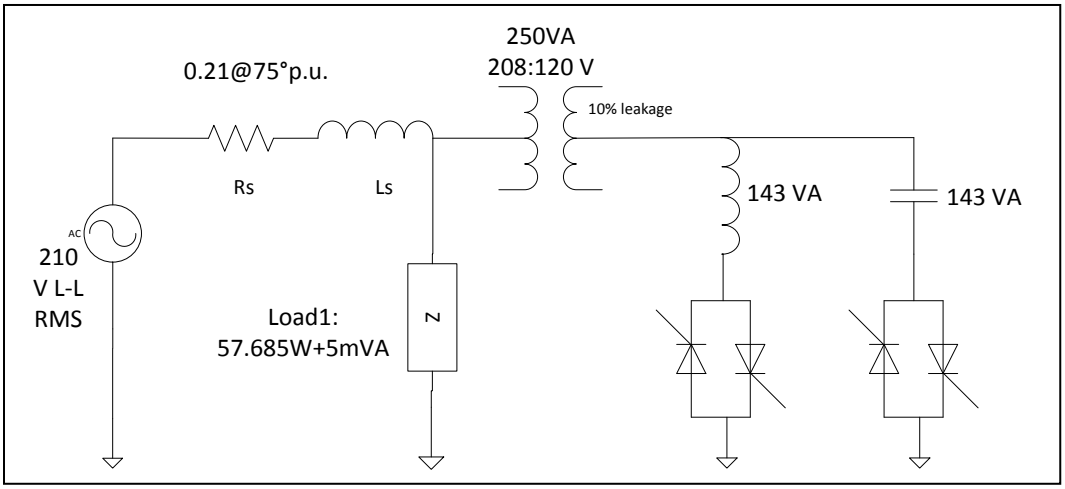


Figure 4.2 Overall layout system.

This section describes the different PSCAD blocks used for the different simulations.

4.2.1 Load and Source Power Measurement

The main purpose of the measurement blocks is to obtain information for feedback in both the voltage control and load balancing cases. These measurements are; the rms voltage at the load point for voltage control, peak values of voltage and current as well as phase differences for the calculation of impedances. For this purpose, two types of blocks are used; the 3-phase rms and the FFT (Fast Fourier Transform) block.

The 3-phase rms block is used together with a series of digital filters; a low pass at 90 Hz and two notch filters one at 60 Hz and another at 120 Hz. The outputs of these filters become one

of the feedback signals for the PI control. A 3% current droop is also part of the feedback signal. In addition, the rms blocks are used to verify that the loads have been effectively balanced.

The FFT block (Figure 4.3) is used to obtain the value of the peak of the fundamental frequency component for both voltage and current and their corresponding phase with respect to a cosine. The magnitude of the impedance is computed using the peak values of voltage and current and the phase is computed from their phase difference (Equations 4.1 through 4.3). By obtaining the value of impedance, we can get the values of $G - jB$(Eqn 4.4) per phase needed for the balancing equations.

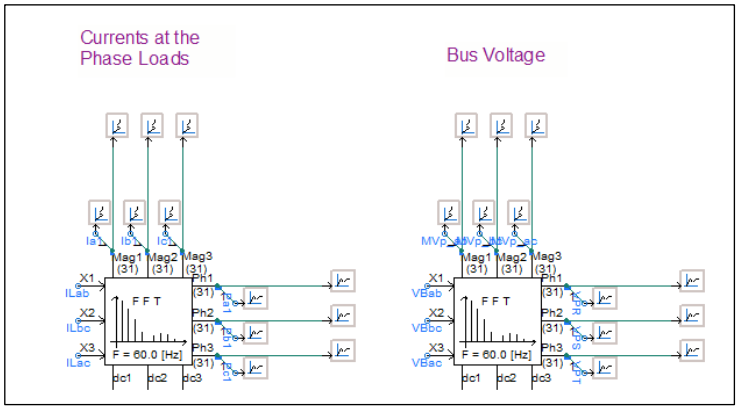


Figure 4.3 FFT measurement blocks used to calculate susceptance values at the load.

$$V = V \measuredangle \theta_{\mathrm{V}} \tag{4. 1}$$

$$I = I \measuredangle \theta_{\mathrm{I}} \tag{4. 2}$$

$$Z = \frac{V}{I} \measuredangle (\theta_{\mathrm{V}} - \theta_I) \tag{4. 3}$$

$$Y = Z^{-1} = G - jB \tag{4. 4}$$

4.2.2 Control Systems

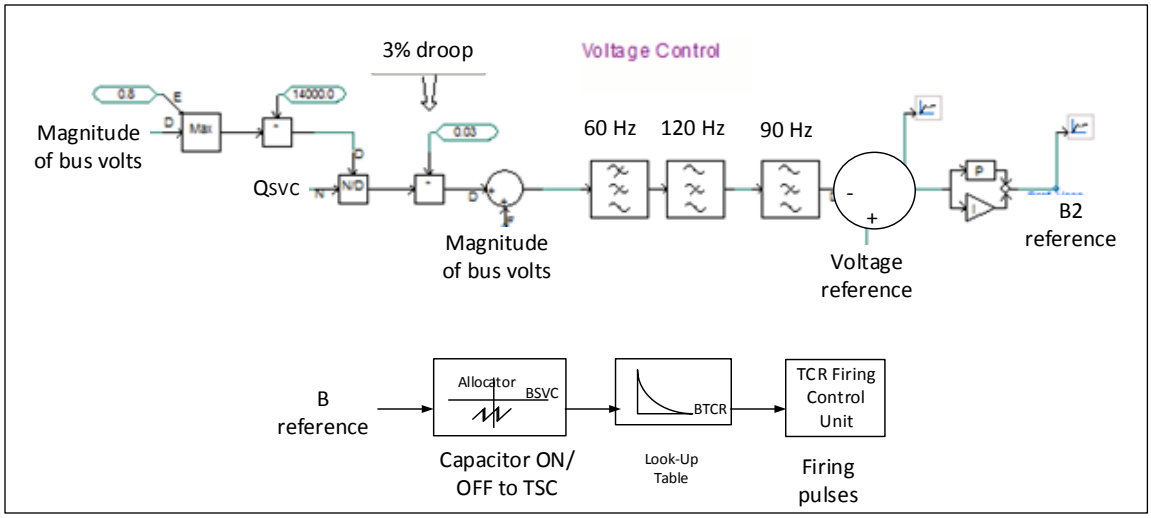


Figure 4.4 Proportional Integral voltage control system.

The simulation includes a PI closed loop controller for voltage regulation and an open loop control for load balancing. The PI control system blocks illustrated in Figure 4.4 are included in the PSCAD library and are based on [12]. The feedback are measurements at the source of the 3-phase l-l rms voltage and it includes a current droop, and the output is a reference of susceptance (B2 reference). Later, this reference is added to B reference from the load-balancing algorithm to become a single one before going to the allocator. The load balancing processing blocks are custom built (shown in Figure 4.5) and they implement the algebraic calculations developed (details shown in section 4.3). Inputs for these blocks are the load susceptances while the outputs are the balancing susceptance per phase and the reference for the susceptance allocation controller. These two processing sections work jointly to provide voltage regulation and load balancing.

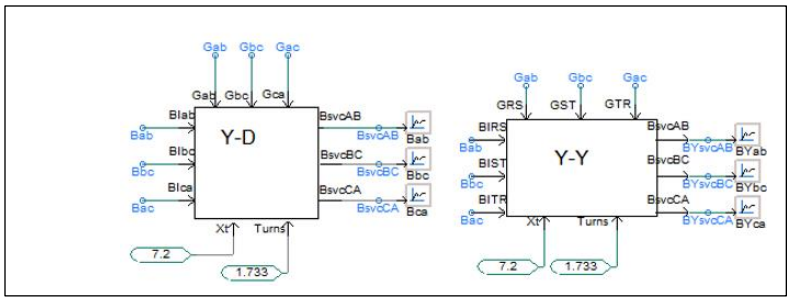


Figure 4.5 Load balancing control system blocks.

4.2.3 Susceptance Allocation Controller

The reference SVC susceptances computed in the blocks of Figure 4.5 become the susceptance orders for the SVC. These orders are then decomposed into an inductive TCR susceptance order (B_{TCR}) and a capacitor selection signal to add/remove capacitor banks and provide capacitive susceptance [12]. Equation 4.5, given in per unit, is used to calculate the needed B_{TCR}. The number of capacitors on (N) is multiplied by the susceptance of that capacitor (B_C) and subtracted from a reference susceptance (Bαβ) [12]. If B_{TCR} is less than maximum susceptance of the inductor (B_L), the number of capacitor banks is decreased, on the other hand if B_{TCR} is greater than zero then the number of capacitor banks is increased, this is graphically shown in Figure 4.6. Once the needed B_{TCR} is obtained the firing angle can be found in the look-up table. This table is constructed from a piecewise linearization of Equation 3.6. In the case of a 12-pulse SVC there are two sets of the components in Figure 4.6 because the values from the reference calculations are different for each side.

$$B_{TCR} = B_{\alpha\beta} - NB_C \tag{4. 5}$$

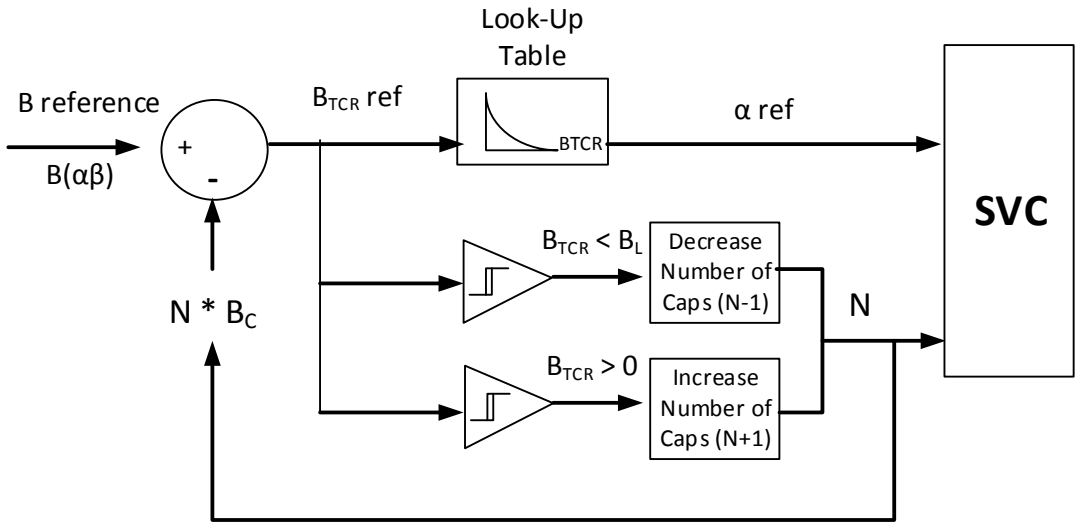


Figure 4.6 Susceptance allocation control.

4.2.4 Synchronizing System and Firing Pulses

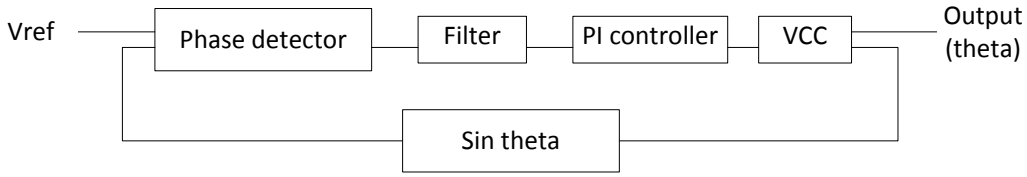


Figure 4.7 Phase locked loop block diagram.

The firing angles from the look up table are converted into firing pulses for the thyristor valves. A firing pulse is issued when the phase of the appropriate signal reference (i.e. line-line voltage ab) equals the firing angle. The line voltage phase is tracked by using a Phase Locked Loop (PLL), shown in Figure 4.7. Figure 4.8 shows the graphical outputs of the PLL and its respective voltage reference. The PLL outputs a saw-tooth signal which is in phase with the line-line voltage that is used as a reference and goes from 0^0 to 360^0. The pulse becomes high when this reference matches the alpha order and lasts 5 ms before returning to a low state and start the process all over. The corresponding antiparallel thyristor is turned on with a pulse that is 180^0 apart from the first positive one.

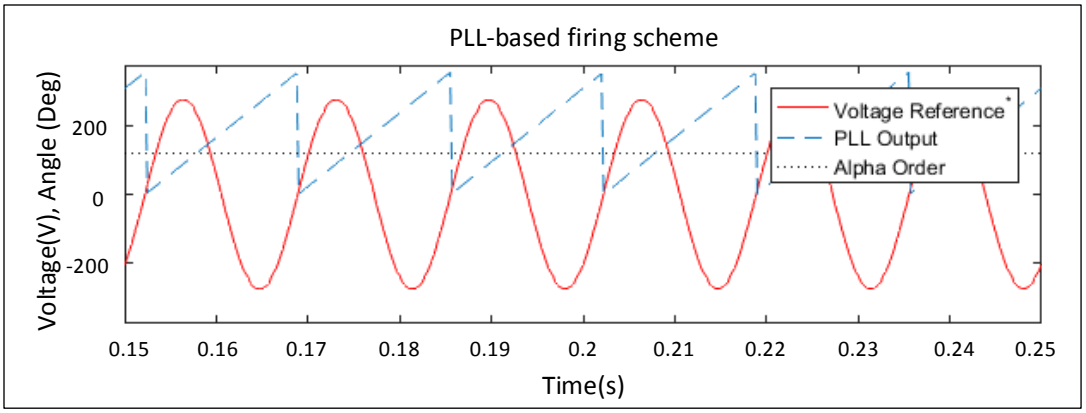


Figure 4.8 PLL firing scheme from zero crossing reference and alpha order (α).

4.3 **Open Loop Control Derivation.**

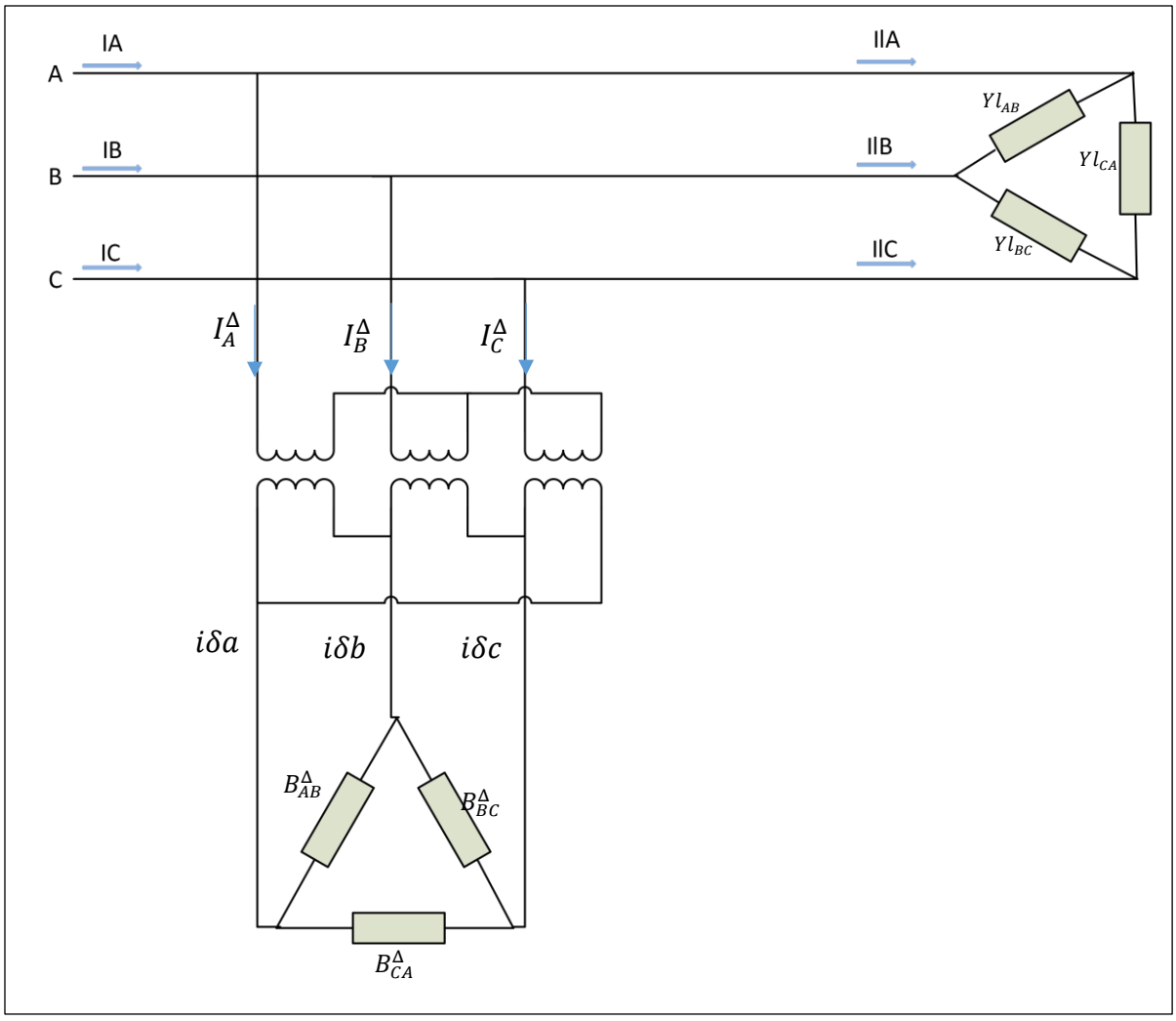


Figure 4.9 6-Pulse SVC connected to system through a Y-D transformer.

The method used to calculate required susceptance is a combination of circuit analysis as described in [10], [18] with some modifications [32]. The topology used in this derivation is a 6-pulse SVC connected to a load though a transformer as illustrated in Figure 4.9. The objective is to calculate the required amount of susceptance per phase for load balancing starting from the known loads that can be deduced by a measurement of voltages and currents. To do this there has to be an assumption that the load has no zero sequence currents (which is always true in a three wire connection) and the ac power supply is balanced.

The steps followed in order to calculate values of balancing susceptance are:

1) Calculate sequence currents at the load by first deriving line currents through circuit analysis
2) Calculate the compensator line currents at the secondary side without inclusion of the transformer leakage reactance
3) Transform line currents from primary side to sequence currents at the secondary side
4) Solve equations for full reactive compensation and load balance
5) Model transformer reactance (Xt) as a Y connected symmetrical load at secondary
6) Convert values of compensator from D to Y connection and add Xt
7) Convert Y connection back to Delta connection

A. Unbalanced load

Given an unbalanced load connected in delta with the following admittances:

$$Yl_{AB} = G_{AB} + jB_{AB}^{l} \quad (4.\ 6)$$

$$Yl_{BC} = G_{BC} + jB_{BC}^{l} \quad (4.\ 7)$$

$$Yl_{CA} = G_{CA} + jB_{CA}^{l} \quad (4.\ 8)$$

B. Assumptions

The following assumptions were made for the calculation of the compensating circuit. The variable *t* represents the turns ratio of the transformer and θ is a phase shift; for wye-delta is 30^0 and for wye-wye is 0^0.

1. Voltages at the source are balanced

$$V_{AB} = U\ ;\ V_{BC} = Ua^2;\ V_{CA} = \ U\ a \quad (4.\ 9)$$

$$a = 1\angle 120^0 \quad (4.\ 10)$$

2. *Voltages at the secondary side of transformer (U') are also balanced and shifted by θ.*

$$U' = \left(\frac{1}{t}\right) U\, e^{j\theta} \quad (4.\ 11)$$

3. *Load does not have zero sequence currents*

4. *The compensating components consist of susceptances B^{C}_{ab},*

C. Equations to solve

a) Sequence currents at the Load

$$I^{+}_{load} = 1/3\ (Il_A + a * Il_B + a^2 * Il_C) \quad (4.\ 12)$$

$$I^{-}_{load} = 1/3\ (Il_A + a^2 * Il_B + a * Il_C) \quad (4.\ 13)$$

b) Sequence currents at the compensator secondary (LV) side

$$I^{-}_{\delta} = 1/3\ (i\lambda a + a^2 * i\lambda b + a * i\lambda c) \quad (4.\ 14)$$

$$I^{+}_{\delta} = 1/3\ (i\lambda a + a * i\lambda b + a^2 * i\lambda c) \quad (4.\ 15)$$

c) Sequence currents at the compensator primary (HV) side

$$I^{+}_{\Delta} = \left(\frac{1}{t}\right) I^{+}_{\delta}\, e^{j+\theta} \quad (4.\ 16)$$

$$I^{-}_{\Delta} = \left(\frac{1}{t}\right) I^{-}_{\delta}\, e^{j-\theta} \quad (4.\ 17)$$

D. Solution to equations

Equations 4.12 and 4.13 are the sequence components for line currents at load and Equations 4.14 and 4.15 are the sequence components for the compensator at secondary side and are transferred to primary side using Equations 4.16 and 4.17. The solutions can be found once all quantities are referred to the primary side. Equations 4.18 through 4.23 show these two sets of solutions derived in this thesis, one for the wye-delta transformer and another for the wye-wye

transformer. Derivations are presented in Appendix I. The reactance of the transformer has not been included for simplification reasons but the next part (E) will demonstrate how to include it.

1) Wye-Delta transformer

$$B_{AB}^{\Delta} = \frac{1}{3}\left(-2B_{AB}^{l} + B_{BC}^{l} - 2B_{CA}^{l} + \sqrt{3}G_{AB} - \sqrt{3}G_{CA}\right)t^2 \quad (4.\ 18)$$

$$B_{BC}^{\Delta} = \frac{1}{3}\left(-2B_{AB}^{l} - 2B_{BC}^{l} + B_{CA}^{l} - \sqrt{3}G_{AB} + \sqrt{3}G_{BC}\right)t^2 \quad (4.\ 19)$$

$$B_{CA}^{\Delta} = \frac{1}{3}\left(B_{AB}^{l} - 2B_{BC}^{l} - 2B_{CA}^{l} - \sqrt{3}G_{BC} + \sqrt{3}G_{CA}\right)t^2 \quad (4.\ 20)$$

2) Wye-Wye transformer

$$B_{AB} = \left(-B_{AB}^{l} + \frac{G_{CA} - G_{ST}}{\sqrt{3}}\right)t^2 \quad (4.\ 21)$$

$$B_{BC} = \left(-B_{BC}^{l} + \frac{G_{CA} - G_{CA}}{\sqrt{3}}\right)t^2 \quad (4.\ 22)$$

$$B_{CA} = \left(-B_{CA}^{l} + \frac{(G_{BC} - G_{RS})}{\sqrt{3}}\right)t^2 \quad (4.\ 23)$$

E. Compensating for the reactance of the transformer (Xt)

The transformer reactance (Xt) is modelled as a series reactance as illustrated in Figure 4.10 a), and then the compensator susceptances ($B^{C}_{\alpha\beta}$) from Equations 4.18 through 4.23 are converted into wye connected susceptances as in Figure 4.10 b) using the Delta-Y transformation. This is followed by the conversion of Xt and $B^{C}_{\alpha\beta}$ into proper values to be added and finally convert back to delta connection shown in Figure 4.10 c). Then the previous equations 4.18 through 4.23 once again become directly applicable. By following the steps mentioned above, we obtain the final results (Shown in Appendix I). These results are used in the overall open loop control diagram (see block labelled calculation of balancing susceptances Bab, Bbc, Bca) shown in Figure 4.11.

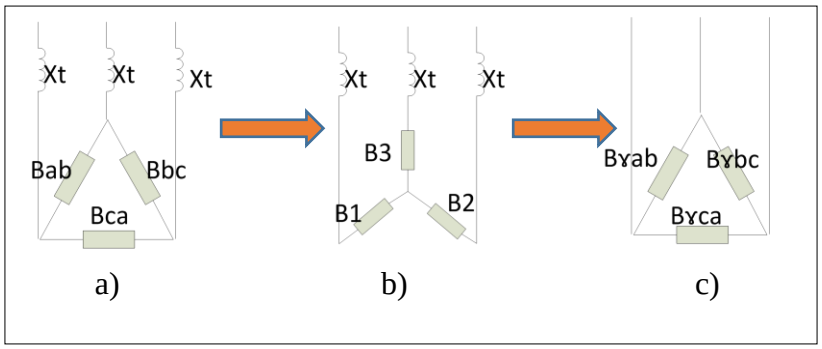


Figure 4.10 Graphical steps for the inclusion of Xt.

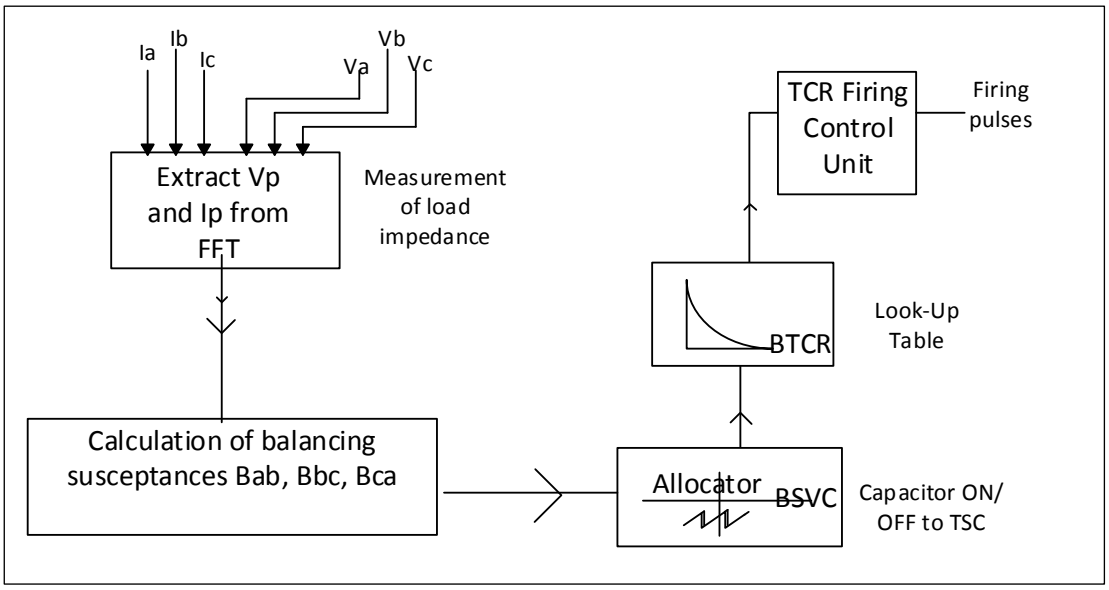


Figure 4.11 Overall SVC open loop control diagram for load balancing.

4.4 **12-Pulse Load Balancing EMTP (PSCAD) Simulation**

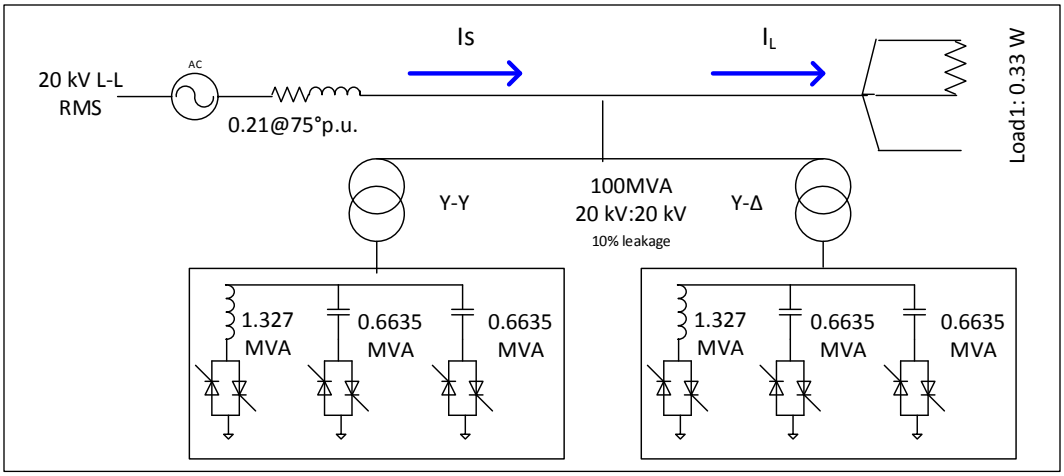


Figure 4.12 System diagram with 12-pulse SVC.

Figure 4.12 shows the system utilized to demonstrate load balancing using a 12-pulse SVC. The voltage source is a 3-phase 20 kV l-l rms, the load is asymmetrical with only one resistance across phases a and b and the SVC is a 12-pulse system with leading capacity per phase of 1.327 MVA and lagging capacity of 1.327 MVA divided into two steps of capacitor banks. The coupling transformers for the SVC are rated at 100 MVA with a turns ratio of 1:1. Because of the different phase shifts of the Y-D transformers, the same susceptance orders cannot be given to the Y-Y and Y-D branches. However, with different susceptance orders, load balancing is achieved. The balancing susceptance orders used for this simulation are the solutions found in the previous section (modified Equations 4.18-4.23). Before calculating the balancing susceptances, the load is divided by half because each side (i.e., Y-Y and Y-D) is providing half the compensation. This results in different firing angles for every one of the twelve pulses; therefore, the advantage of a 12-pulse SVC, which is the cancellation of some harmonics, cannot be used. In addition, an SVC coupled through a Y-D transformer cannot provide the imaginary part of the positive sequence currents and so it is not possible to correct power factor, nevertheless the load is balanced.

4.4.1 Load Balancing Results Using a 12-Pulse SVC

Fig 4.13 a) shows that the load currents are unbalanced, with line A and line B of equal magnitude and 180^{o} apart and line C is zero. The source line currents are balanced with the addition of the SVC currents as observed in Figure 4.13 b). Figure 4.14 shows: a) unbalance percentage, b) total harmonic distortion and c) power factor at source. At steady state, the unbalance percentage is 0.75% and it is found using symmetrical components as given by Equation 4.24, the Total Harmonic Distortion (THD) is 0.8 % and it is measured using the THD PSCAD component, and finally the power factor is above 0.95 for the three lines.

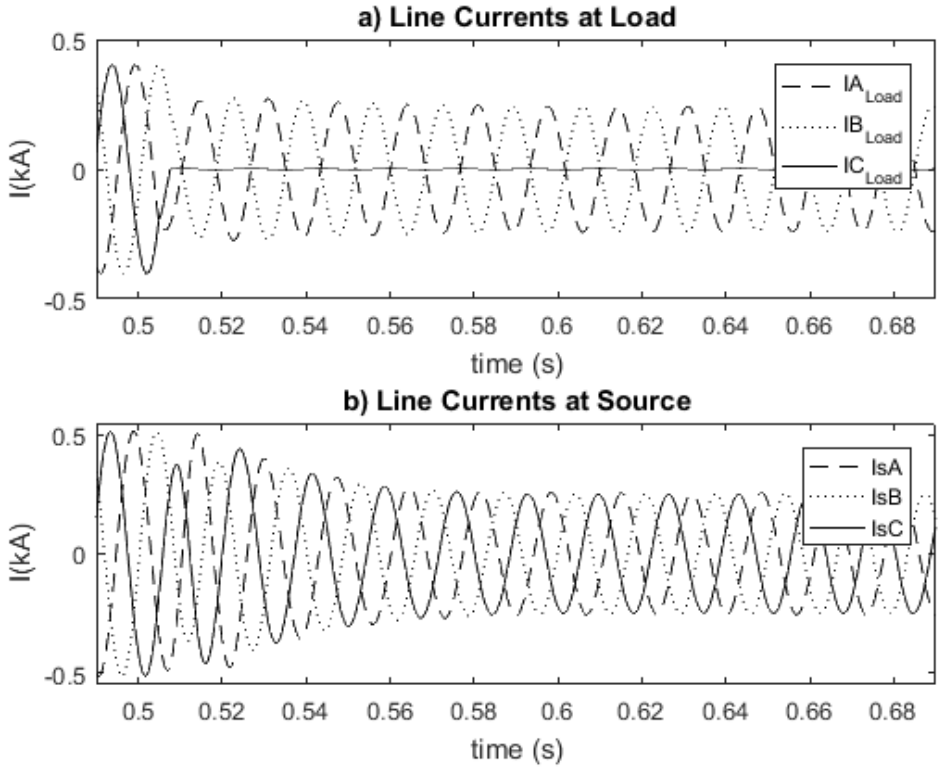


Figure 4.13 12-pulse line currents at a) Load and b) Source.

The unbalance percentage is given by the following equation:

$$\epsilon_I(\%) = \frac{|I_-|}{|I_+|} X100 \tag{4. 24}$$

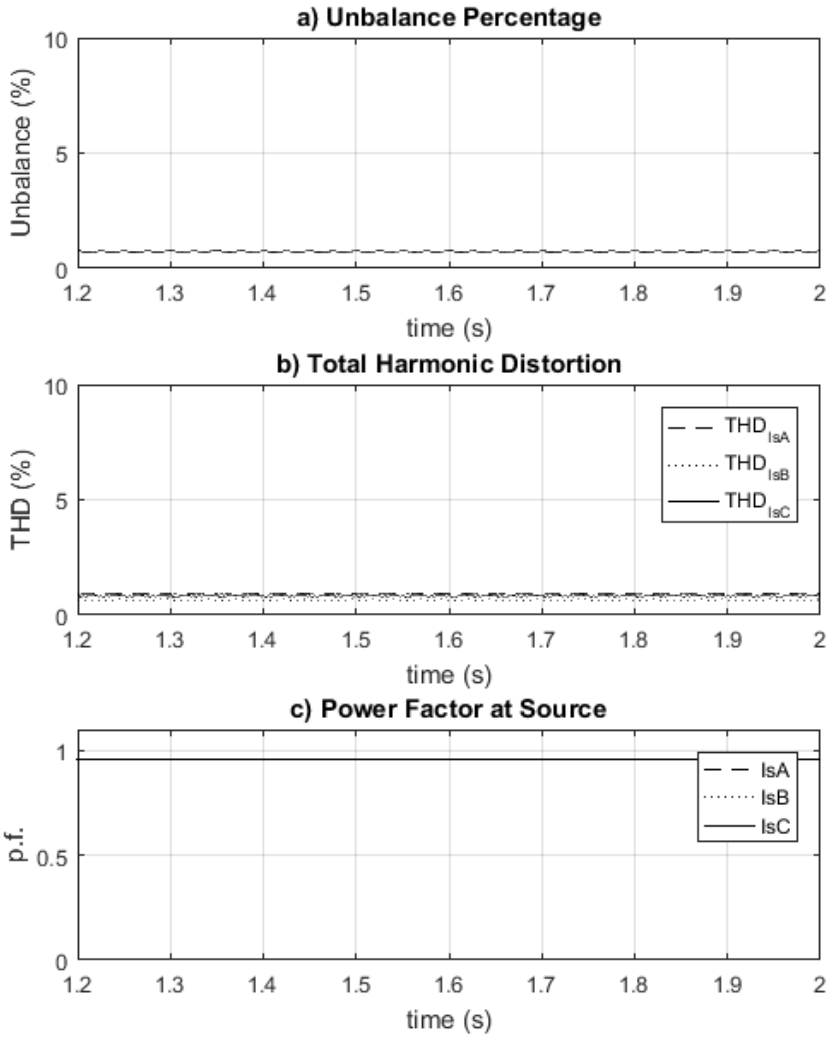


Figure 4.14 12-pulse at steady state a) Unbalance, b) THD, and c) PF at source.

4.5 **Load Balancing Using a 6-Pulse SVC**

A 6-pulse SVC with a Y-Y coupling transformer can provide reactive power for both load balancing and power factor correction as demonstrated in the following section.

4.5.1 System Layout for Load Balance

A. 6-Pulse SVC System 1 Diagram

Figure 4.15 shows the single line diagram simulated in PSCAD. The 3-phase connection is done in delta configuration for both SVC and load. The values selected for this simulation are comparable to the values available in the laboratory.

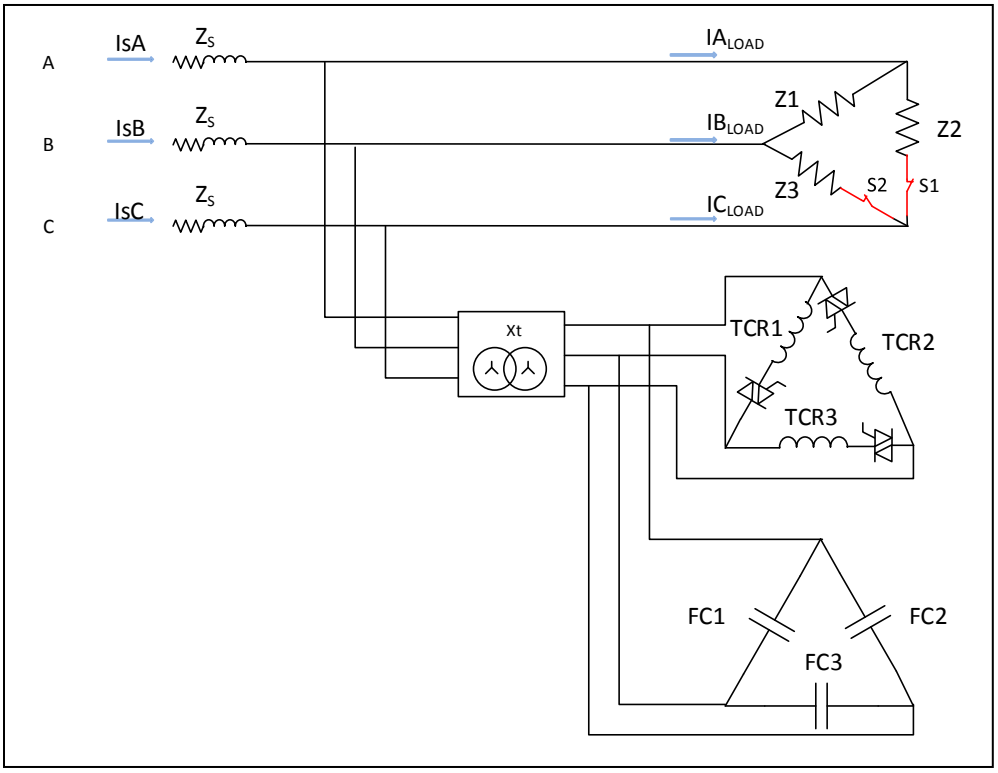


Figure 4.15 Single-phase view of PSCAD System 1: Load Balancing.

B. 6-Pulse SVC System 1 Data

i) Base Values

The base values for the per-unit quantities used are as follows:

$$VA_{base} = 100\,VA$$
$$V_{base} = 208\,V$$
$$Z_{base} = 432.64\,\Omega$$

ii) Load

$$Z = 750$$
$$S = 57.685\ W$$

iii) SVC

$$L = 0.4\ H$$
$$C = 8.8X10^{-6}\ F$$
$$Q_L = 143\ VA$$
$$Q_C = -143\ VA$$

iv) Source

$$Z_s = 0.20\ @75^0\ pu$$

4.5.2 Load Balancing Results Using a 6-Pulse SVC

The simulation of the system in Figure 4.15 starts at time t = 0.0s with a balanced load and at time t = 0.3s, switches S1 and S2 are open and the loads on phases BC and CA are disconnected leaving an unbalanced system. Figure 4.16 a) shows that the line currents at the load are unbalanced (99% unbalance); with currents IA and IB having same magnitude and being 180^o apart and IC being zero magnitude. Figure 4.16 b) shows balanced line currents at the source (3.39% unbalance) due to the balancing compensation by the SVC. However, it is evident from the figure that the currents become balanced at the expense of added harmonics.

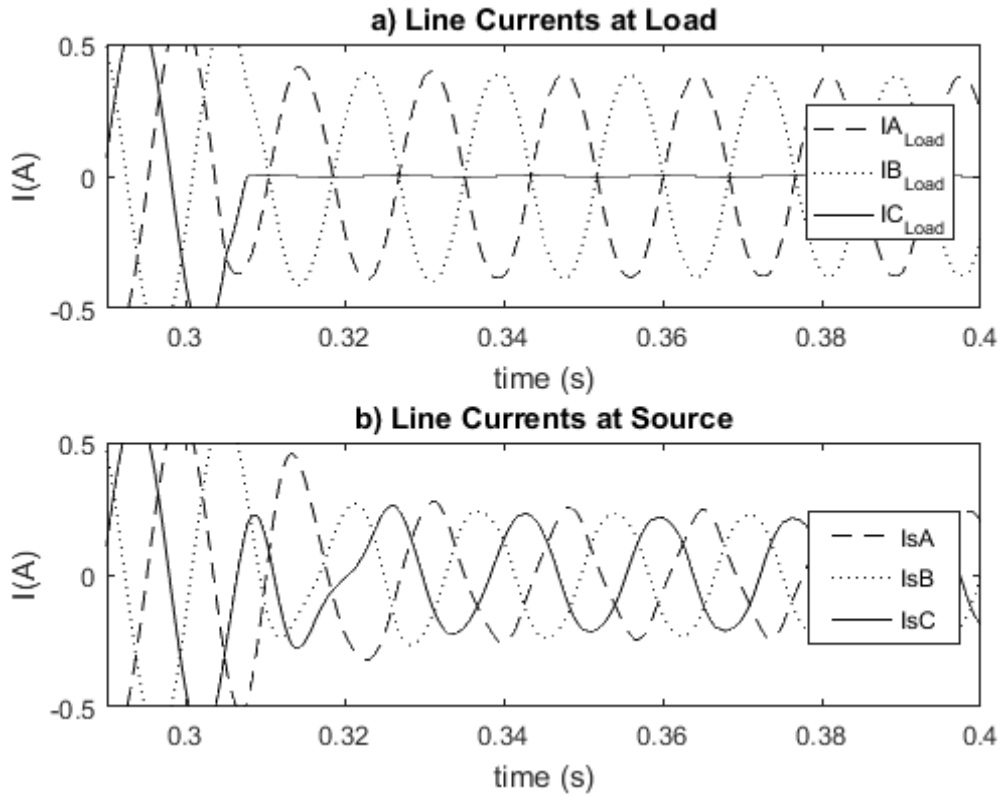


Figure 4.16 6-pulse line currents at: a) load (unbalanced) and b) source (balanced).

Additionally, Figure 4.17 shows the resulting levels of a) current unbalance, b) total harmonic distortion (THD) and c) power factor at source. The steady state value of current unbalance is 3.39 %; the THD percentages for lines A, B, and C are 7.404%, 4.43%, and 3.177% respectively. The power factor at the source for lines A, B, and C are 0.99, 0.99, and 0.98 respectively.

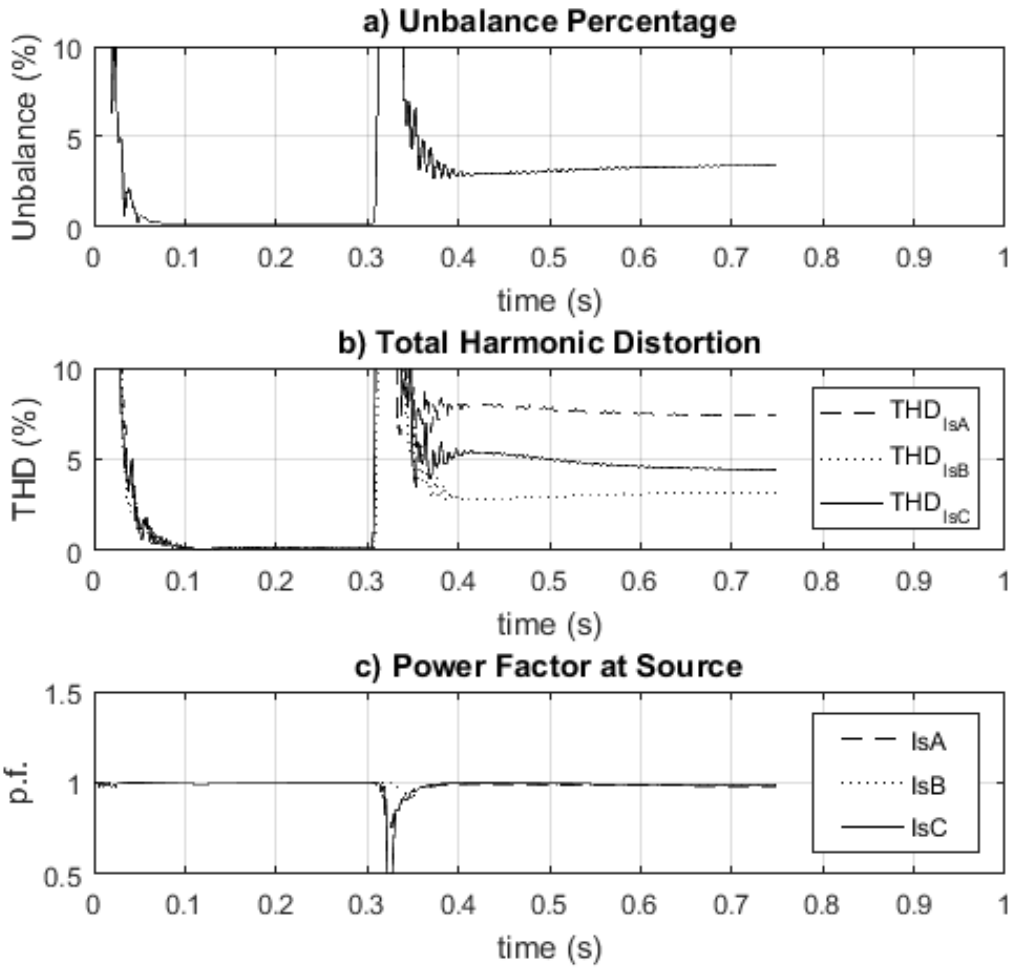


Figure 4.17 Simulation results for dynamically balanced currents.

4.5.3 Load Balancing Results for Different Levels of Current Unbalance

In order to provide a more complete set of results it is necessary to know what the SVC behavior is under different amounts of unbalances and also what kind of results are obtained when there is not enough reactive power for full compensation. For this purpose, a table with different types of unbalances based on their level is defined and shown in Table 4-1.

Table 4-1 Loading for different cases of unbalances

Loading	**Load *ab* (Ω)**	**Load *bc* (Ω)**	**Load *ca* (Ω)**
Case 1 (successful balancing and pf correction)	700	600	500
Case 2 (successful)	1800	900	550
Case 3 (successful)	600	open	open
Case 4 (not successful)	600	300	150

Results, summarized in Table 4-2 and Figure 4.18, show that the SVC can handle unbalances in cases 1-3 even if two phases are open (case 3) such as in cases where railways are connected to a single phase. Case 4 is not balanced in the same proportion as the others even when its unbalance (25.6%) is almost the same as case 2 (28.46%). This is because the reactive power capacity of the SVC in one or more phases is smaller than the necessary reactive power capacity needed to balance this load. In other words, the rating is not sufficient to balance this load. Figure 4.19 shows the amount of susceptance needed by the compensator per phase and it is clear that a load of 150Ω is outside the range of the SVC. The rating of the SVC in terms of susceptance is ± $3.3X10^{-3}$ (S). This is the equivalent to providing balancing susceptance to a minimum resistance of around 550 Ω connected across phase a and phase b. In addition, a PF of 1 is achieved as observed in Table 4-2.

Table 4-2 Power factor correction with and without SVC

	PF Line A		PF Line B		PF Line C	
Loading	Without SVC	With SVC	Without SVC	With SVC	Without SVC	With SVC
Case 1	0.9947	0.999	0.999	0.999	0.999	0.999
Case 2	0.939	0.996	0.987	0.998	0.990	0.998
Case 3	0.8	0.989	0.8	0.992	NA	0.995
Case 4	0.875	0.986	0.993	0.992	0.979	0.984

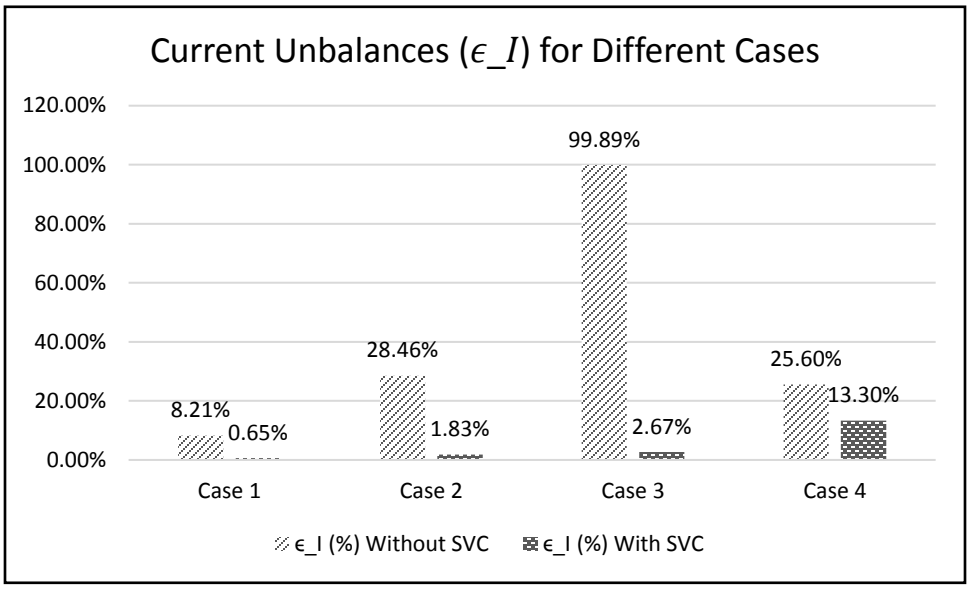


Figure 4.18 Line currents at the source for different cases of percentage unbalance.

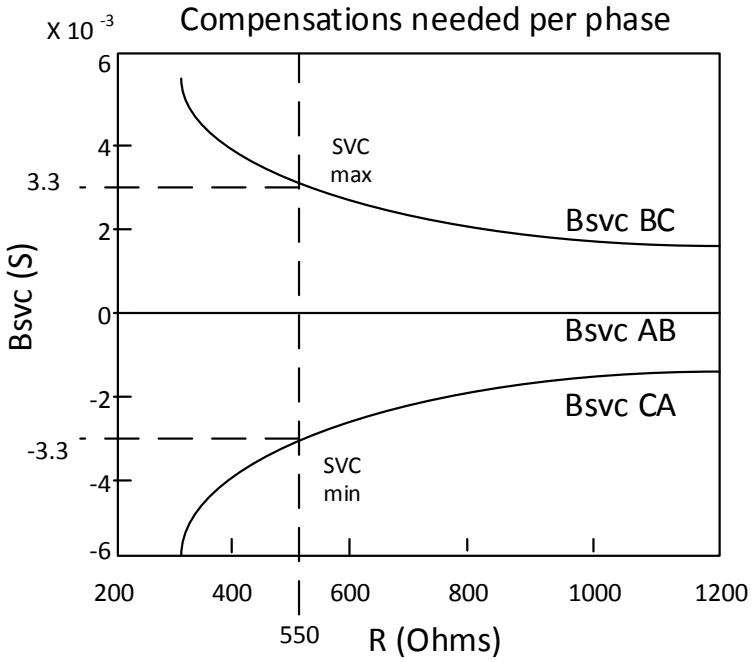


Figure 4.19 Per phase compensations for a resistive load (R) in phase ab.

4.6 Enhanced Load Balancing Control System

In addition to load balancing, the power factor correction feature in the above controller can be replaced with a voltage control feature. In this case, instead of having full reactive compensation (where total Q exchange is zero) as was the case with PFC to unity power factor, a PI control system is added to generate the necessary amount of reactive power to regulate the 3-phase rms voltage. The output of the PI is a reference of susceptance, adding this to each of the susceptance references from the load balancing technique gives the total susceptances needed for achieving both load balancing and voltage control functions. The new orders are sent to the susceptance allocator and can be provided by the SVC.

4.6.1 Study System for Evaluating the Enhanced Control System

The single line diagram simulated in PSCAD is shown in Figure 4.20. It consists of a 3-phase balanced load (at first) connected in delta. At time t = 0.3s, switches S1 and S2 (similarly as in previous Figure 4.15) open and create an unbalanced situation. In addition, there is a change of load at time t = 0.4s added by closing the switch S3 in Figure 4.20. The SVC configuration is a 6-pulse TSC-TCR with two steps of capacitors connected through a Y-Y transformer with the characteristics illustrated in Figure 4.20. The susceptance needed for voltage regulation is added to the susceptance needed for load balancing and then provided by the SVC. Measurements were taken at source (I_S) , load (I_L) and at point of common connection for voltage regulation control.

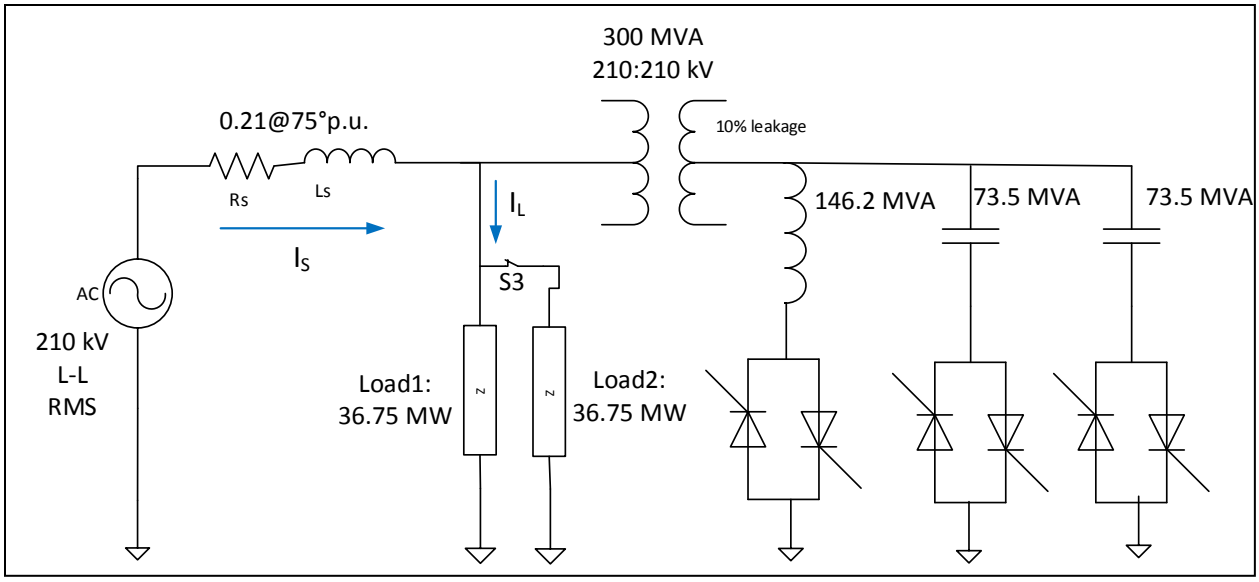


Figure 4.20 Single phase view of System: Load balancing and voltage regulation.

4.6.2 Simulation Results

The results of the simulation are shown in Figure 4.21 and Figure 4.22. Figure 4.21 shows the results of the balancing algorithm. The currents at the load are 100 % unbalanced (Figure 4.21 a)) but this unbalance is reduced to less than 3% at the source side (Figure 4.22 c)) by the action of the SVC.

As explained before, a major drawback of the SVC is the amount of harmonics injected into the system. Figure 4.22 b) shows that for this case there is no significant harmonic distortion in the system, however, this percentage may change with the amount of reactive power injected into the system and the kind of firing angles used to do so.

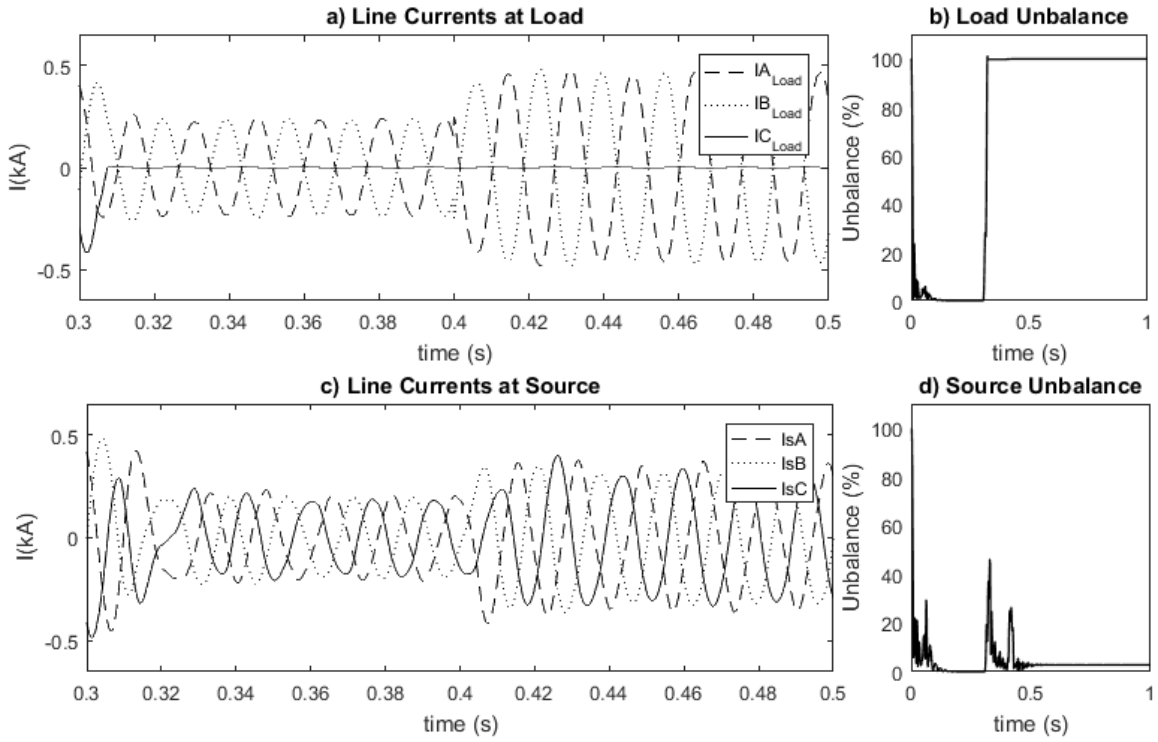


Figure 4.21 PSCAD simulation results: unbalances at load and source.

Figure 4.22 shows the 3-phase rms voltage, power factor, and the total harmonic distortion of the system before and after the switch. Figure 4.22 a) shows the 3-phase rms voltage using a PI controller that was tuned by trial and error. At initialization, the overshoot is less than 15% and it takes about 0.1 seconds to reach steady state. At 0.3 seconds when the system becomes unbalanced, the system responds with an overshoot of about 10% and it takes 0.1 seconds to reach steady state. At time t = 0.4s a second load is added and the system responds in about 0.4 s. As can be seen in the graph, the steady state error is small. The THD oscillates during transient but in about 600 ms, its final state is below 6% with lines A, B, and C of 5.5 %, 3.94%, and 1.84% respectively (Figure 4.22 b)). The power factor also oscillates during transient time but at steady state lines A, B, and C reach a PF close to unity with values of 0.995, 0.997, and 0.993 respectively.

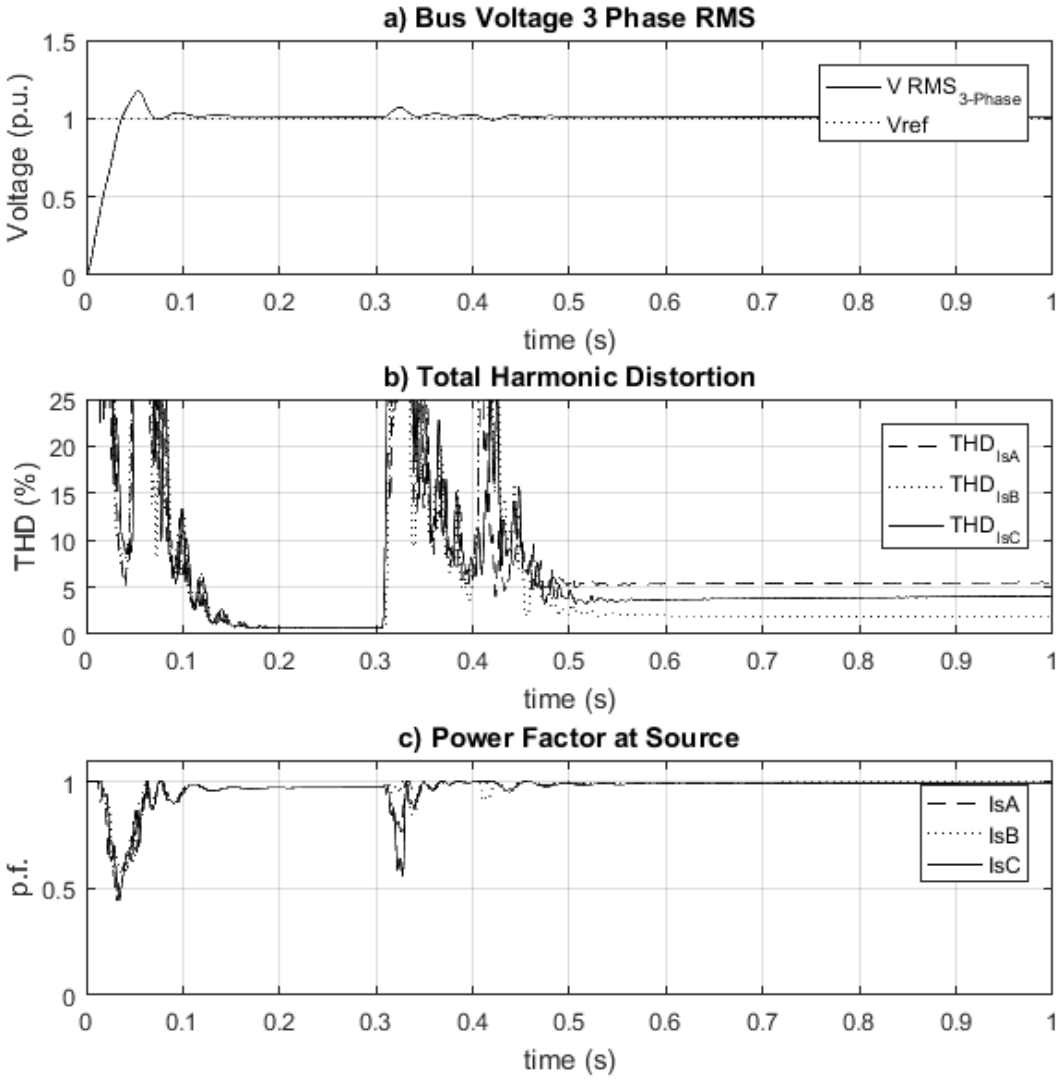


Figure 4.22 PSCAD simulation results: a) voltage rms b) THD c) PF at source

4.7 Current Harmonics in a 6-Pulse SVC

Odd Harmonics 1 through 25 were recorded while changing the single-phase load (Load 1 in Fig. 4.20) and allowing the SVC to perform load balancing. Figure 4.23 shows the rms magnitudes of the odd harmonics for the individual line currents at different loadings.

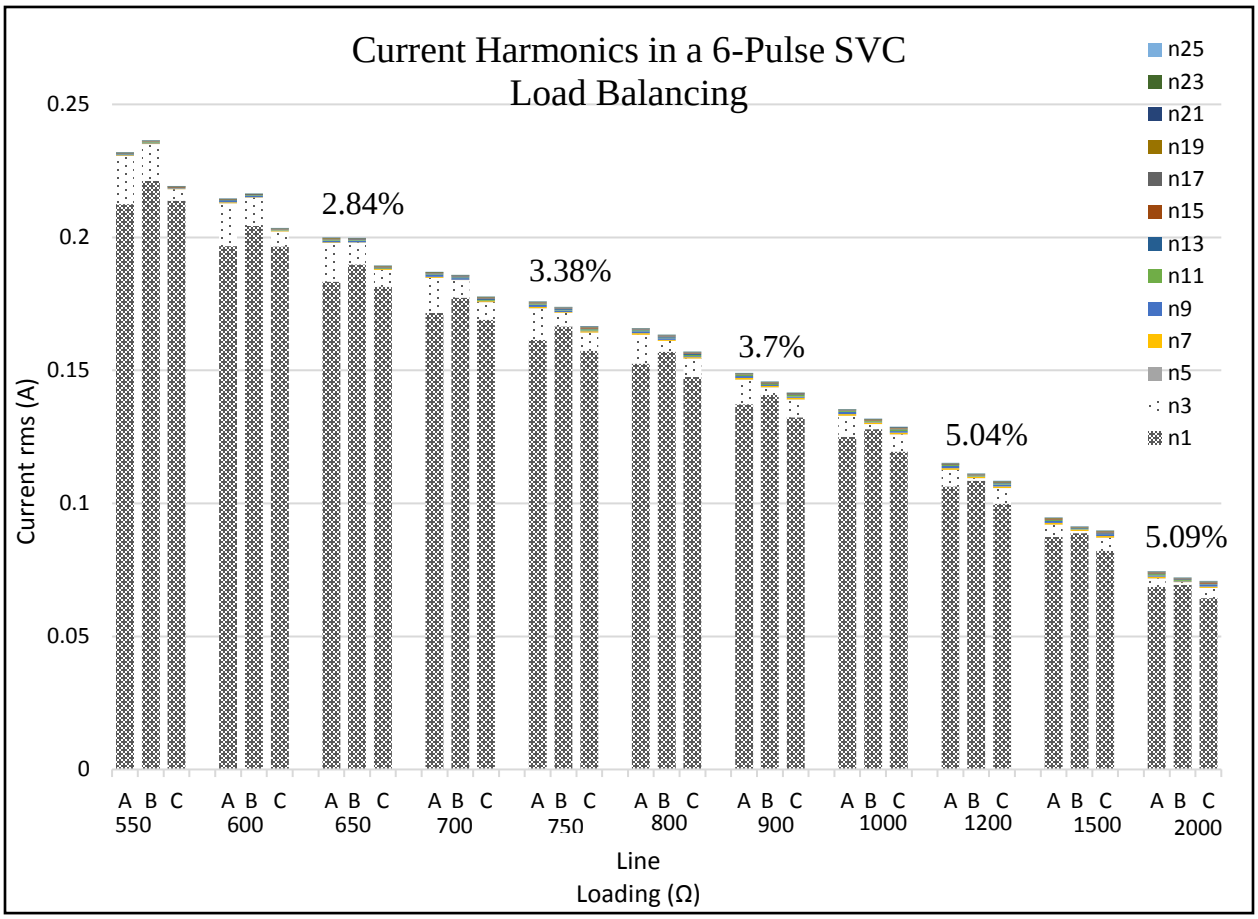


Figure 4.23 Current Harmonics in a 6-Pulse SVC.

It is observed in Figure 4.23 that the third harmonic is significant with respect to the base frequency. In this figure, the variation of other harmonics cannot be noticed because they are relatively small. In addition, the unbalance percentage is shown above the bars. Figure 4.23 shows that the unbalance increases as the load increases.

In order to study the other harmonics and the pattern they follow with respect to load changes, the magnitude of the harmonics was plotted at different load changes. Figure 4.24 shows the resulting plot from this changes. The figure shows that for lines A, B, and C, the 5^{th} harmonic is much smaller compared to the others and the largest harmonic is the 9^{th} . The other harmonics decrease as n (harmonic number) increases. Some of the harmonics increase and others decrease or stay the same with an increase in load.

For example, in line A and B, the 7^{th}, 9^{th}, and 11^{th} harmonics increase with a load increase but in line B only 7^{th} increases, 9^{th} decreases and 11^{th} stays the same. The other harmonics oscilate with a tendency to approach zero.

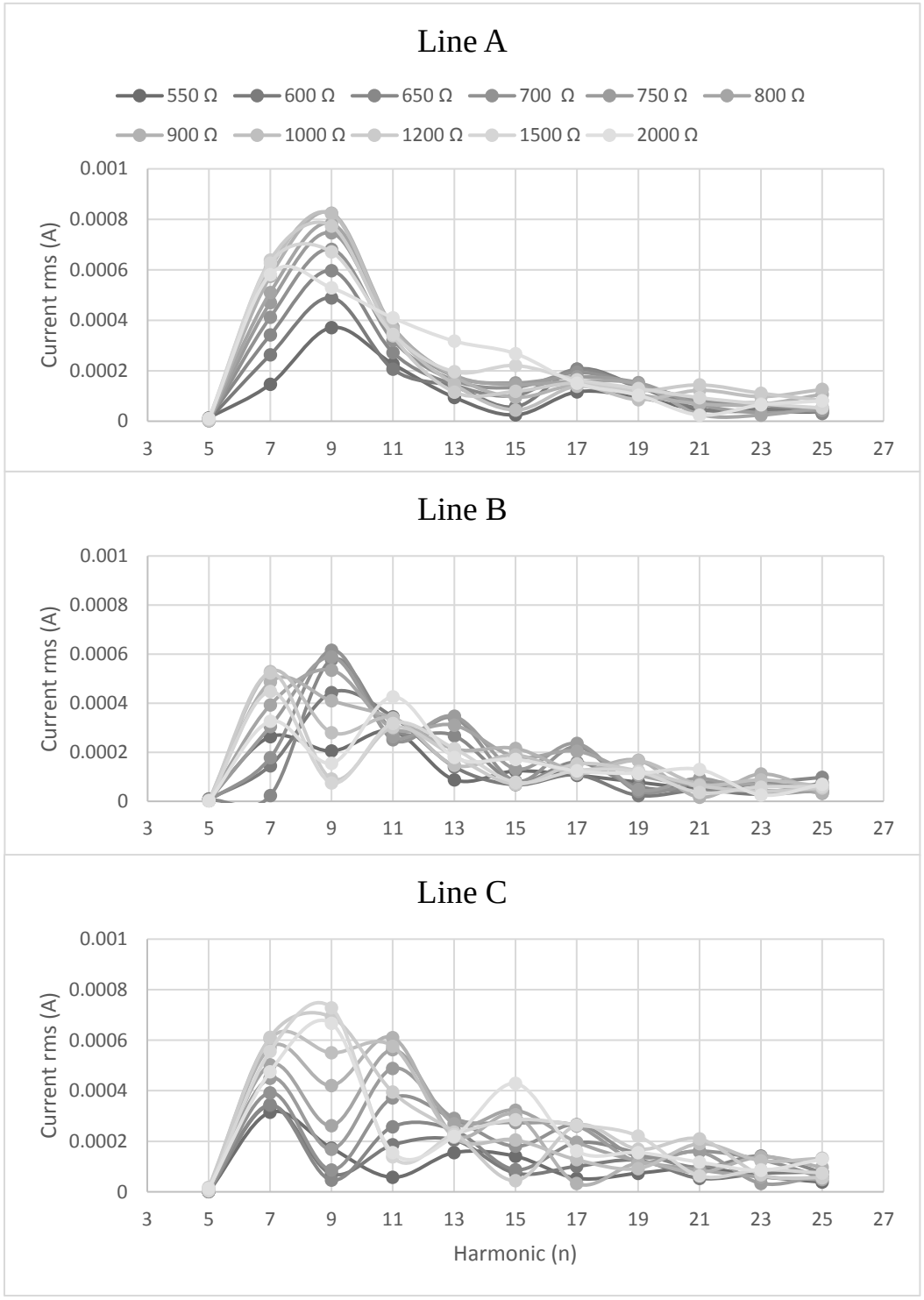


Figure 4.24 Current Harmonics in a 6-Pulse SVC for load balancing.

4.8 **Current Harmonics in a 12-Pulse SVC**

Figure 4.25 shows the rms magnitude of the hamonics in a 12-Pulse SVC. The figure shows three different bars, one for each line of current (A, B, C). For this configuration the 3rd harmonic is less noticeable than the one in the 6-pulse. Conversely, for this configuration, the unbalance and the magnitude of the 3rd harmonic decrease as the load increases.

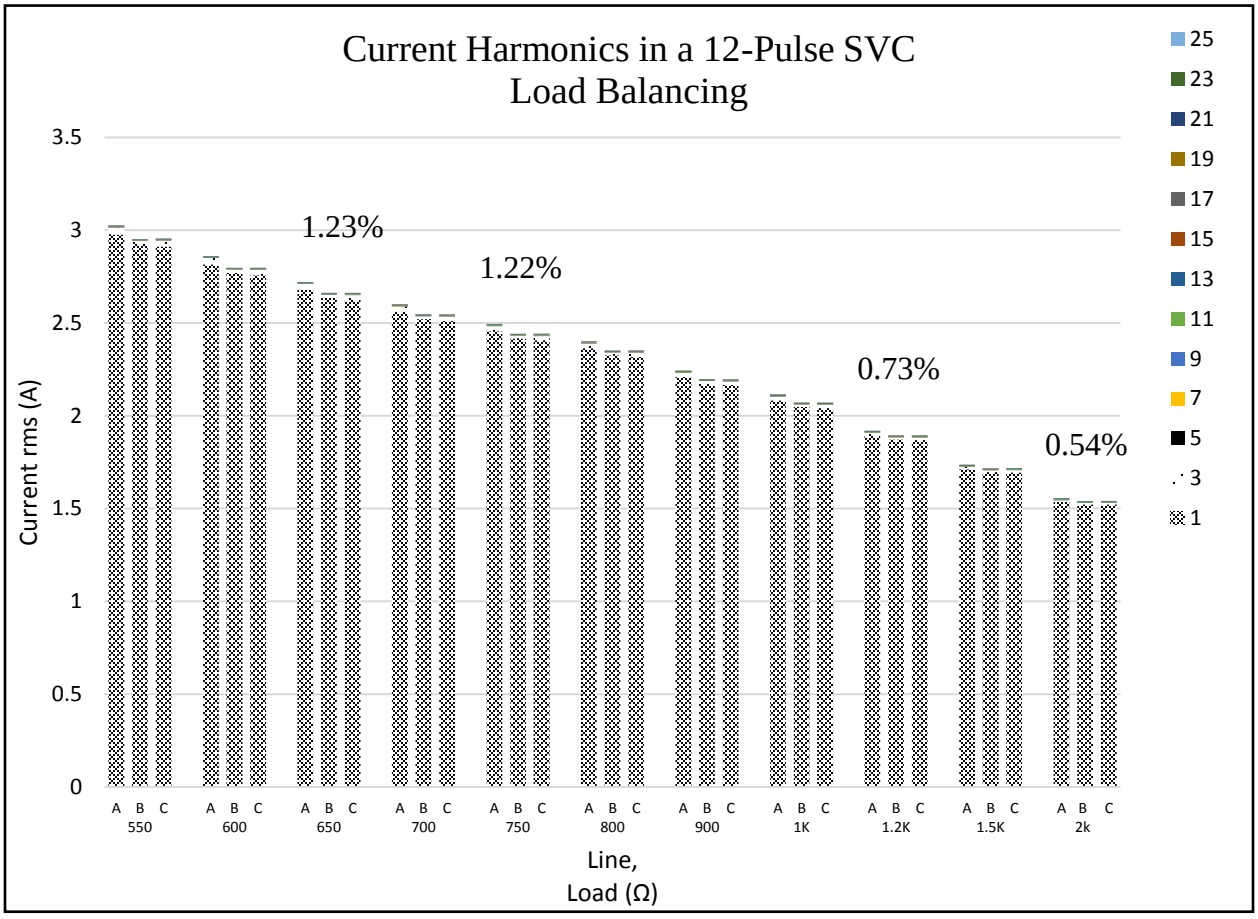


Figure 4.25 Current harmonics at the source for a 12-Pulse SVC.

The current unbalance is also shown in Figure 4.25 as percentages above bars. These percentages show that the unbalance reduces as the load increases.

Figure 4.26 shows that for lines A, B and C, the 5th harmonic decreases when the load decreases (unlike the case of the 6-pulse SVC where this harmonic is almost non-existing for all

cases). The largest harmonic is 11^{th} which increases as the load increases. The other harmonics decrease as n (harmonic number) increases and their magnitude decreases with an increase in load. Therefore, it could be said that a decrease in unbalance results in a decrease of the harmonics, mainly the 3^{rd}, which is the most significant but also 5^{th}, 9^{th}, 15^{th}, 17^{th}, and 19^{th} decrease.

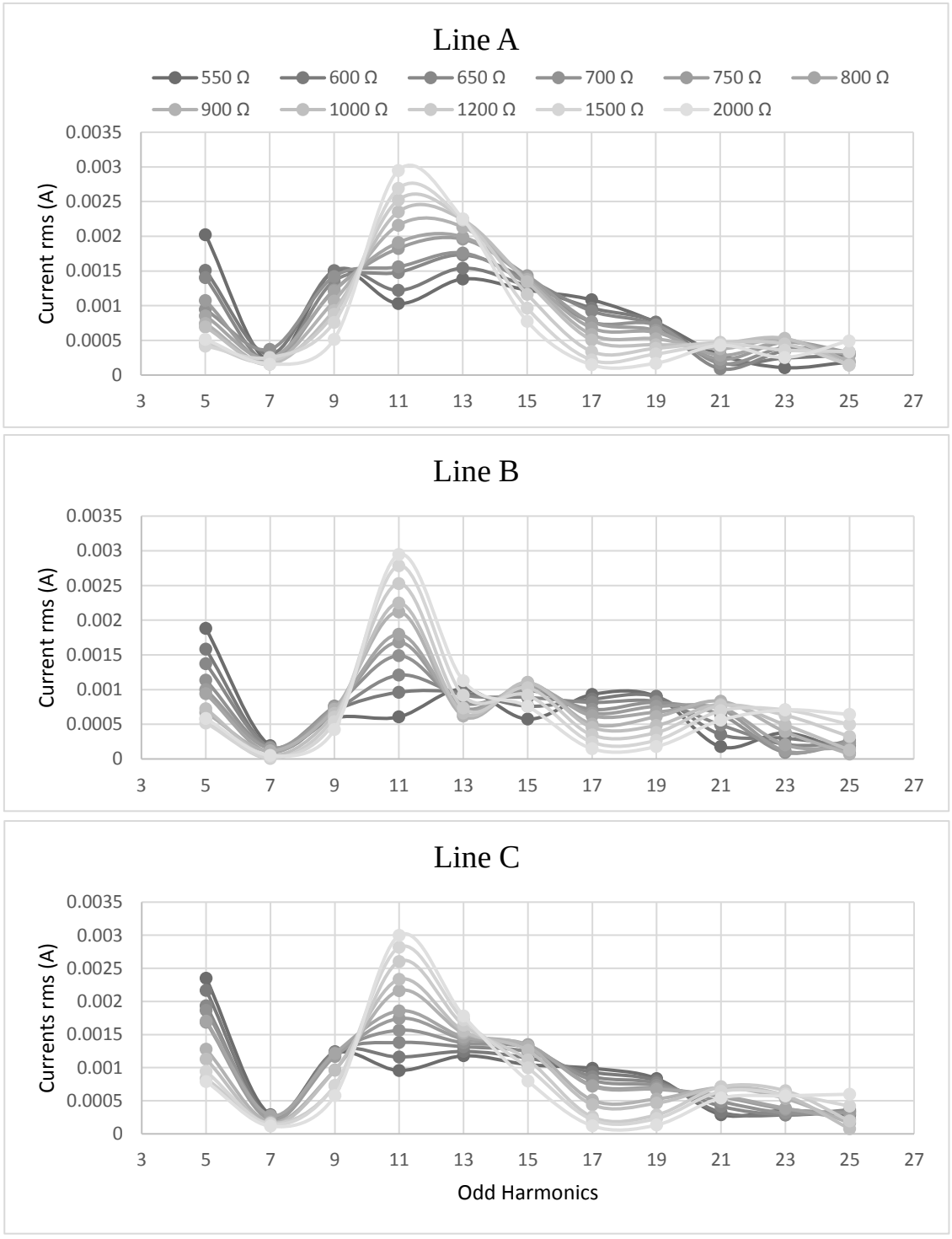


Figure 4.26 Odd harmonics in a 12-Pulse SVC for different loadings.

4.9 Chapter Conclusions

It was demonstrated in this chapter that the SVC algorithm developed for load balancing works, although with some power quality degradation, i.e., additional harmonics result due to the TCR operation. These can be reduced with 12-pulse operation. If necessary, additional filters can be added, but this was not carried out in this thesis. Another important application of the SVC is voltage regulation. It was shown that voltage regulation could work in a closed loop without interfering with the load balancing algorithm therefore achieving load balancing and voltage regulation with the same SVC.

The load balancing case by a 12-pulse SVC takes the unbalanced load and divides it into two; 50% for compensation by the Y-Y side and 50% for compensation by the Y-D side. It was not done here but perhaps an optimization of the distribution of the load would give better results when it comes to handling the harmonics.

In order to test that this algorithm is fast enough for digital computation and perform on-line, a hardware set up was developed. The design and implementation of this lab-scale SVC is presented in the next chapter.

CHAPTER 5 Hardware Development of a 6-Pulse SVC

Developing a lab scale model of the simulation validates the proposed balancing method and provides a testbed for future applications.

It is necessary to integrate hardware experiments into the academic curriculum for a better understanding of power electronics and its role when integrated into a complete power system. Therefore, in order to impart a full and complete study of SVCs at a university level, a laboratory hardware set-up is necessary to support simulations when students are trained in the use of SVCs.

5.1 Overview of the System

In this chapter the design and development of a lab-scale SVC is presented. The developed power electronics board connects to LabVolt bench equipment to form a complete power system that is used for the demonstration of the load balancing algorithm. The laboratory scale SVC consists of power electronics and a processing board interconnected with existing power equipment available in the laboratory. The printed circuit board uses triacs and a pwm firing system and it is equipped to be interconnected to external elements using banana connectors. Furthermore, this chapter will present some similarities and differences between the developed SVC and the simulated one.

5.2 Requirements

The requirements for the construction of the hardware is that it should use available components in the lab, have a circuit with minimum complexity and cost. A basic case was created to test the balancing method using a configuration which includes the following from the LabVolt components: a three phase voltage source, a transmission line, capacitors and inductors for SVC, and resistors for the load. The SVC is rated at 120 V and 48 VA per phase.

5.3 System Layout

The complete system consists of external elements available in the lab, and a PCB interface which was developed for this purpose. The layout, shown in Figure 5.1 consists of two main parts; a) a central power system and b) a 6-pulse SVC. The topology selected for this demonstration is FC-TCR connected into the main ac system through a Y-Y transformer.

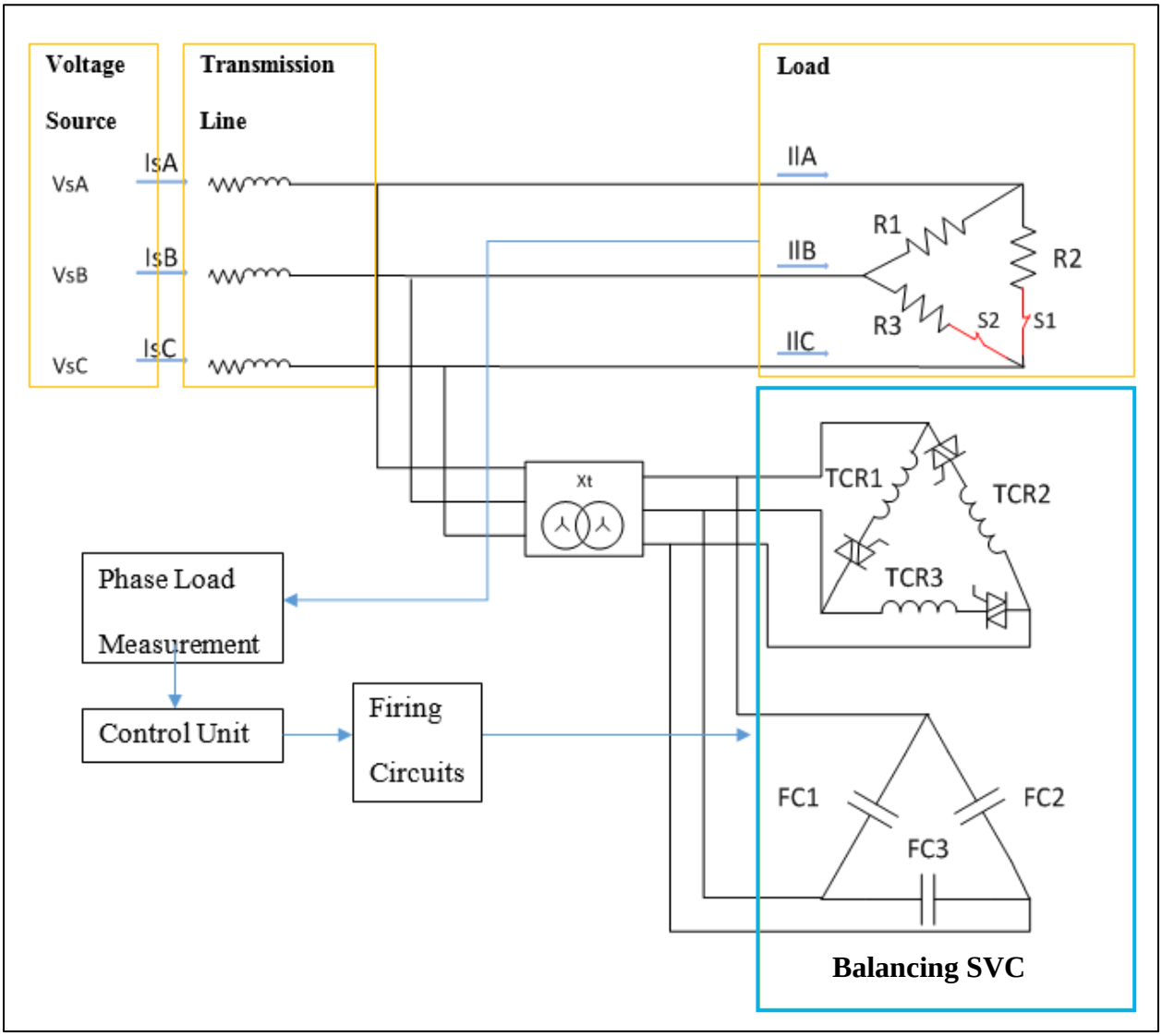


Figure 5.1 Overall system layout for hardware implementation.

A) Central power system

The central power system used for the implementation is a functional 3-phase system that delivers power to an unbalanced resistive load. Its main parts are a 3-phase voltage source, a transmission line and a resistive load. These three elements are shown in Figure 5.1 and they are available in the lab as part of LabVolt bench work blocks which can be interconnected using banana cables.

The voltage source is a 3-phase source that can range from 0 to 208 V line-to-line rms and has a capacity of 15 Amps. The transmission line block has three impedance settings; 60 Ω, 120 Ω and 180 Ω. The resistive load block contains three resistors with values and ratings of 1200 Ω (0.1A), 600 Ω (0.2), and 200 Ω (0.4). The 200-ohm resistor value is not used in the prototype, thus giving a maximum load of 69.36 W with the 600-ohm resistor in one phase. Low currents are more difficult to process because they are more affected by noise, therefore, in order to get better readings for the control system, values with highest ratings were chosen as shown in Table 5-1.

Table 5-1 Power system characteristics

Elements	**Constraints**	
	Size	Current Rating
Voltage Source	208 l-l rms (max)	15 A
Transmission Line	60 Ω	0.33 A
Load	600 Ω	0.2 A

B) SVC components

The ratings of the elements in the laboratory are summarized in Table 5-2 and they have to be considered when designing the SVC. The components for a FC-TCR were chosen such that the inductive capacity is double that as the capacitor consequently achieving an equal amount of injecting and absorbing power. Figure 5.2 shows the reactive power capacity of the FC-TCR.

Table 5-2 SVC characteristics

Elements	**Constraints**	
	Size	***Max. Current Rating***
Capacitors	8.8 μF→ -48 VA	0.4 A
Inductors, 2 in parallel	0.4 H → +96 VA	0.4 A (per inductor)
Coupling transformer rating	208/120 (l-l rms) , 250 VA	1.2 A

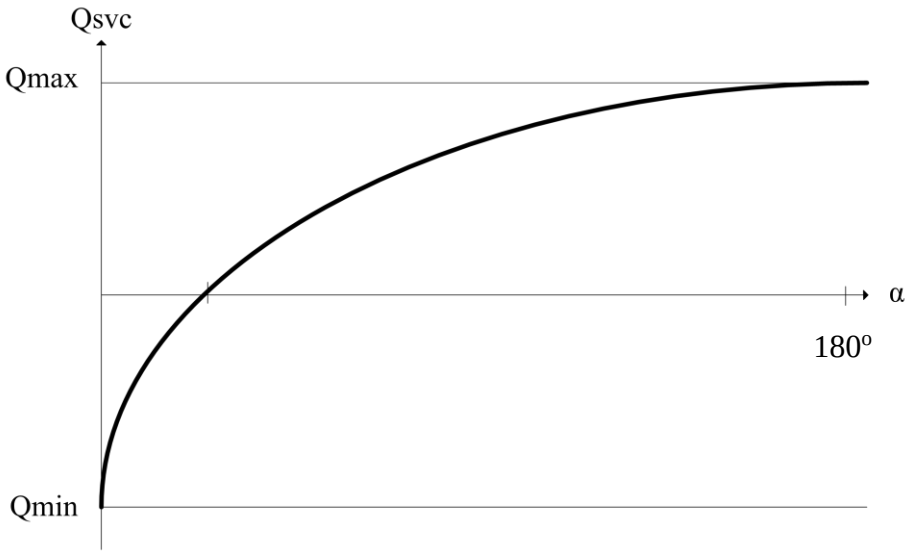


Figure 5.2 Reactive capacity if FC-TCR SVC with respect to firing angle.

From the available elements in Table 5-3 C and L are chosen as:

$$C = 8.8\mu F \tag{5. 1}$$

$$Zc = \frac{1}{j\omega C} = -j301.43\Omega \tag{5. 2}$$

$$Qc = \frac{V^2}{Z_C} = -\frac{120^2}{301.43} \approx -48\,VA \tag{5. 3}$$

$$Q_L \approx 96VA \rightarrow L = \frac{V^2}{Q_L\omega} \approx 0.4H \tag{5. 4}$$

In order to have equal amount of lagging and leading power in the FC-TSR, double amount of inductive power is needed. This is achieved by connecting two 0.8 H inductors in parallel, giving a maximum VA rating for the TCR part of 96 VA. Additionally, two transformers were used for the realization of the hardware implementation. The main one is a coupling transformer to connect the SVC to the main ac system and the other one is to obtain the synchronization pulses for the firing of the thyristors. The main transformer is a LabVolt block that consists of three single phase transformers with taps of 208/120 and 208/208. These three single phase transformers can be

connected to make a Y-Y or a D-Y three phase transformer. The second transformer is a smaller single phase transformer with ratio of 10:1. It is connected to phase AB at the secondary of the main transformer and provides the reference for the zero crossing detector.

C) Capabilities and limitations

The SVC limitations are given by the amount of reactive power it can provide in this case 48 VA of lagging and 48 VA of leading power as calculated in Equations 5.3 and 5.4. In this case, no back to back thyristors were used to disconnect the capacitors. If the thyristors could have been switched off, 96 VA of leading VARs would be possible. Figure 5.3 a) and b) show graphs of the SVC compensation susceptances needed for different values of resistive load when this load is connected across phase ab at the end of a three phase system.

The figures are different when the SVC is coupled to the system through a Y-Y (a) or Y-D (b) transformer. The figures appear to be the same; however, the required compensation from each phase of SVC is shifted when using different transformer connections. For a Y-Y connected SVC, the required compensation is the same as a directly connected SVC, which are the values given by the Steinmetz Circuit and changes only by the ratio of the transformer and its susceptance. Conversely, the compensation values needed in a SVC coupled through a Y-D transformer have the same values but are shifted for phases AB and BC with most capacitive compensation provided from phase AB. The plots come from modified equation 4.13- 4.18 shown in appendix B.

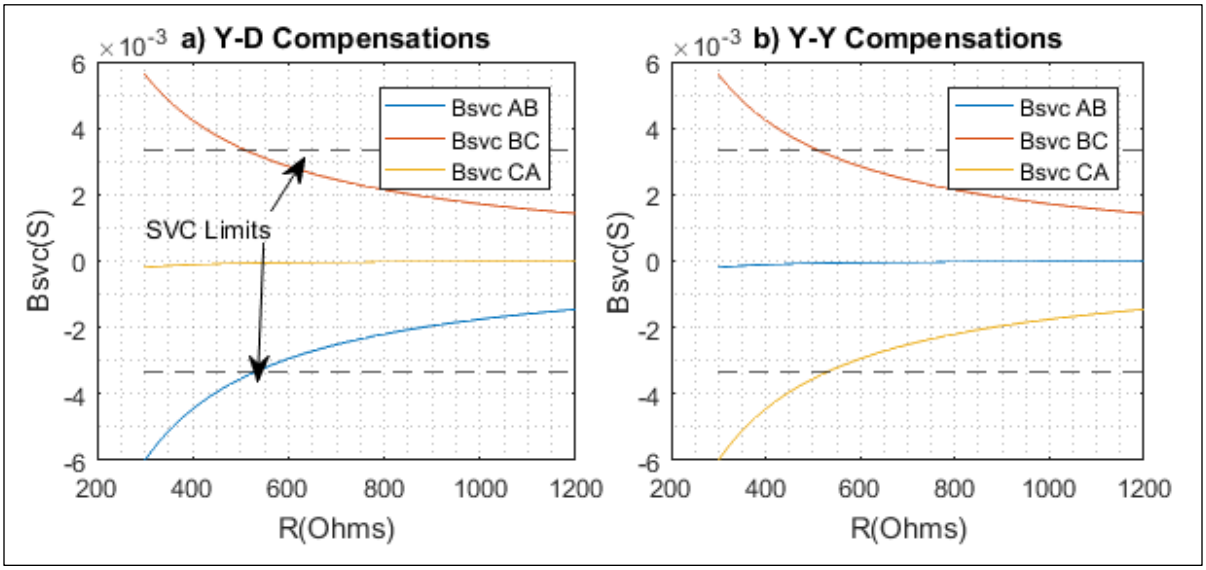


Figure 5.3 Per phase SVC compensations for a resistive load.

The curves in Figure 5.3 were necessary since the values for the reactor and capacitors of the SVC were chosen first, so the graphs helped select the acceptable range of test loads. For a first test, the selected transformer chosen was Y-Y connected. As a result, the SVC is able to balance any resistor above 550 Ω connected between two phases, say A and B, with nothing connected between phases B and C or C and A. This is marked in Figure 5.3 a) as the SVC limits. These figures give a graphical representation of the compensation capacity of the SVC

5.4 **Power Electronics Interface**

As previously discussed, it is called a 6-pulse SVC because each TCR uses two antiparallel thyristors and they require their own firing pulse which are 180^{o} apart from each other. However, in this lower rating experiment triacs were used instead of thyristors as the power electronic switch. Triacs have the function of two antiparallel thyristors but only require a single pulse. The use of triacs makes it more attractive for the lab equipment as it simplifies the firing scheme by getting rid of one firing signal. Finally, it is easier to connect and replace a single component instead of

two which is also a desired feature for this equipment. Some of the necessary components of the SVC are the trigger synchronization, FC-TCR modules and the digital-analog interface.

The power electronics block is shown in Figure 5.4. It consists of the sensor circuits, thyristor firing circuits, and the control unit.

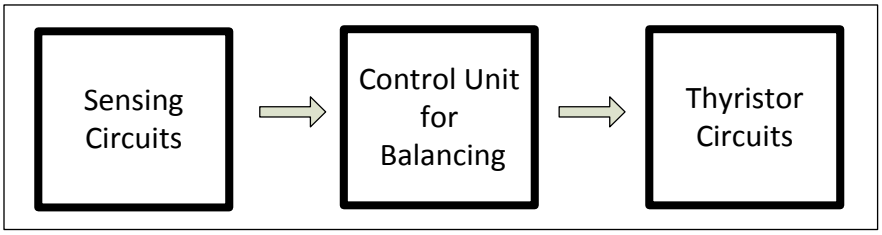


Figure 5.4 Block diagram of PCB.

i) Data Acquisition

The data acquisition block is the necessary set of electronics to obtain the information needed for the processing of the compensation algorithm. It includes two different types of blocks to read voltage (Figure 5.5 a)) and current (Figure 5.5b)) across the phase loads. The first block is a peak detector for fast analog-digital processing of resistive load and the second block is designed to shift signals to positive values for all digital processing. The principal parts of both blocks are the current sensor and the voltage sensor.

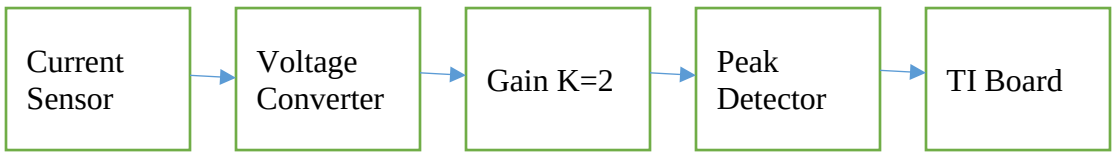


Figure 5.5 Current sensor block diagram.

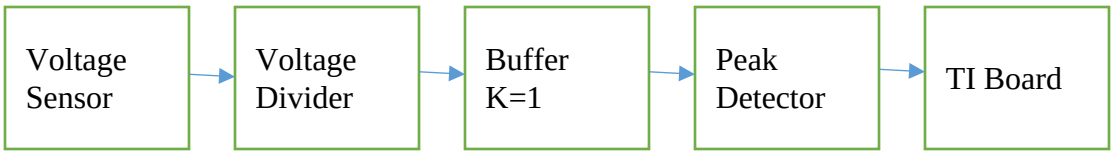


Figure 5.6 Voltage sensor block diagram.

The current sensor is an LEM LA 25-NP current transducer and its output may go to a peak detector or a voltage shifter.

Figure 5.7 and Figure 5.8 show the circuits and simulation results for obtaining peak values of current and voltage respectively. The process begins with the current sensor connected in series with the resistor being measured, then the transducer converts these values into lower values of current set to a ratio of 1000:3. Next, this output is converted into a voltage with the use of a resistor connected to ground. Then this voltage is buffered, amplified and it goes to a peak detector and finally it goes to the input of the digital signal processing (DSP) board. This peak detector is based on a design of buffered peak detector [33].

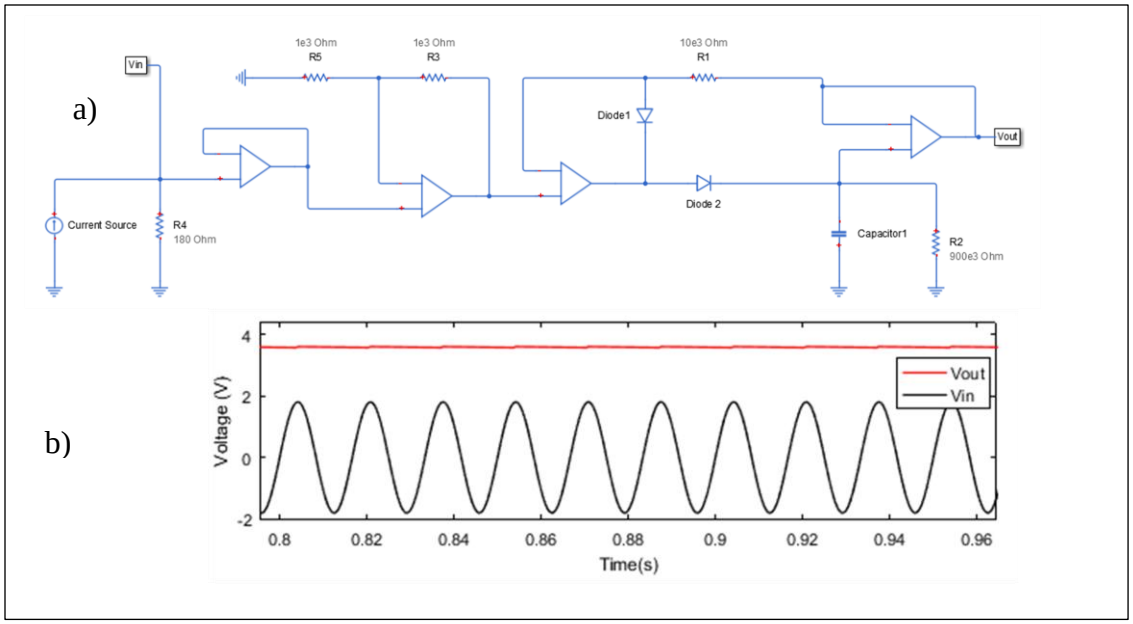


Figure 5.7 Current peak detector.

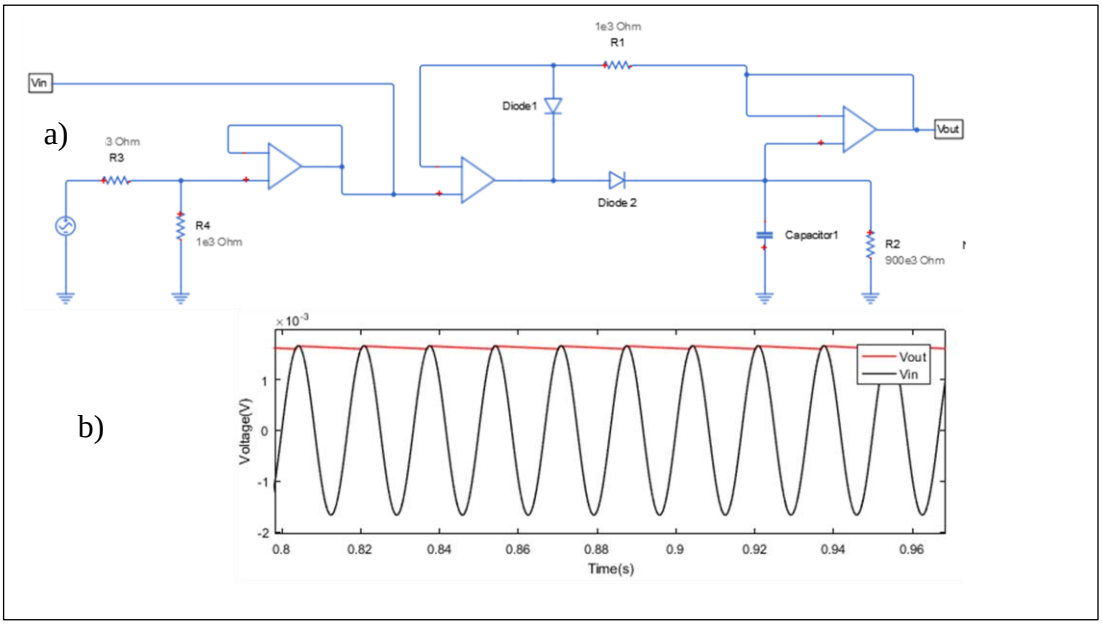


Figure 5.8 Voltage peak detector.

The voltage sensor is composed of two stages based on voltage division as presented in Figure 5.8. The first stage converts high voltage ac phase-to-phase into low voltage ac phase-to-phase and it is connected in parallel across the voltage being measured. The second stage divides the voltage

one more time and it has ground as reference. This voltage also goes through a buffer (gain=1) and then a peak detector before going into the input of the processing board. This simple configuration allows for quick computation of the resistance value per phase using Equation (5.5).

Figure 5.7 b) and Figure 5.8 b) show the simulation outputs of the current and voltage peak detectors. This figure shows that the output of the peak detector is a dc with a ripple. This ripple depends on value of the capacitor but making the ripple too small can prevent the peak detector from following changes in voltage.

$$R = \frac{V_{peak}}{I_{peak}} \tag{5. 5 }$$

Values of resistance can be computed fast using this method but clearly this only works for a purely resistive load, as was the case in the experiment. Complete sets of impedance measurements require a magnitude and a phase. Phase measurements can be obtained with additional analog circuits or from digital processing. For the purpose of full signal processing, a second block has been added to the PCB. This block uses the same output from the voltage and current sensors but it is fed into a voltage shifter such that all values are positive before being fed into the processing DSP board. These signals can be digitally processed to obtain peak, rms values and the phase between voltage and current waves. For example, a Fast Fourier Transform (FFT) can be applied to the signal to obtain the fundamental components of and determine magnitude and phase of an impedance that is not purely resistive. However, these processes add delay to the system. The current laboratory system only works for resistive unbalanced loads, and the extension to other load types is left for future work.

ii) Control Unit for Balancing

The signal processing and control unit used to implement the balancing algorithm is a Texas Instrument microcontroller illustrated in Figure 5.9. It is a Digital Signal Processing Card (DSP)-F28M35 that can run up to 150 MHz. Table 5-4 summarizes all the important aspects of this microcontroller as described in [34]. The F28M35x has two subsystems; a master and a real time control but all the processing for this application was done using the control subsystem.

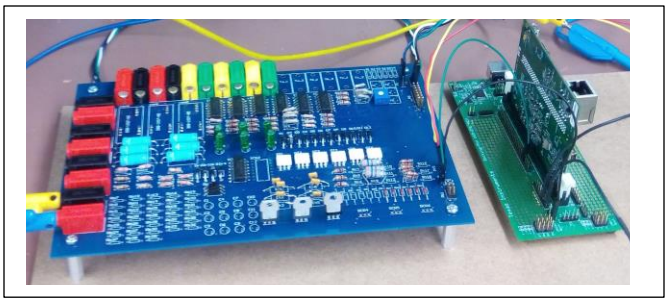


Figure 5.9 PCB board (left) and F28M35x DSP board from Texas Instruments (right).

Table 5-3 Microcontroller characteristics

Subsystem		**CPU type**	**Speed**	**Memory**		
TI 32-bit F28x	Floating point	C28 32-bit CPU	Up to 150 MHz	256-512 KB ECC Flash	20 kB ECC RAM	6Ch DMA
ARM 32-bit Cortex		ARM Cortex M3 32-bit CPU	Up to 100 MHz	256-512 KB ECC Flash	16 kB ECC RAM	32Ch DMA

The balancing algorithm in the control unit begins by obtaining the peak values of voltage and current. These values are read using the on-chip analog to digital converter (ADC) in the DSP and store these conversions in memory. Six input channels are used and they correspond to three current readings and three voltage readings. Then from the peak values, the value of the resistive

load is calculated. Next, the balancing susceptances are obtained and finally the corresponding PWM signals are sent to the firing circuitry.

Load Balancing Control

The flow diagram for load balancing is illustrated in Figure 5.10 [32] with a block diagram illustrated in Figure 5.11. This diagram shows the process when the system has an N number of TSCs (steps). Therefore, the SVC will try to keep the system balanced until it reaches its maximum capacity.

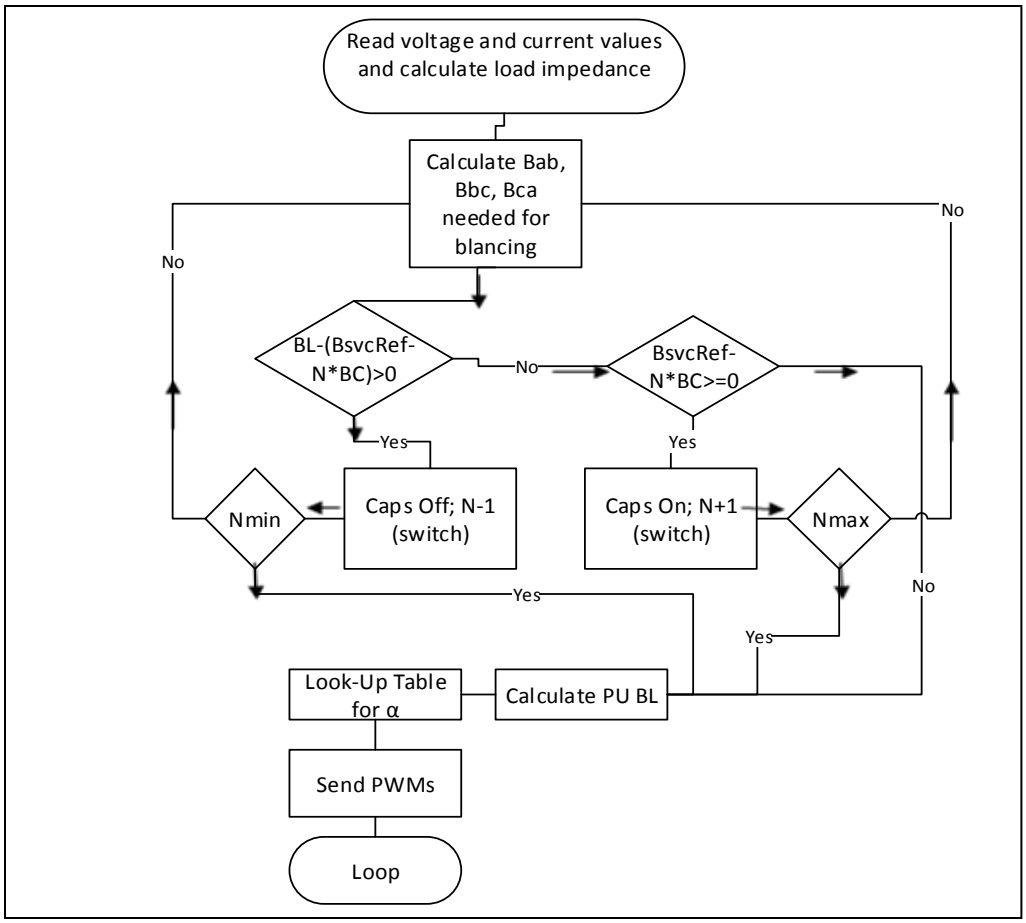


Figure 5.10 Flow diagram for the balancing algorithm.

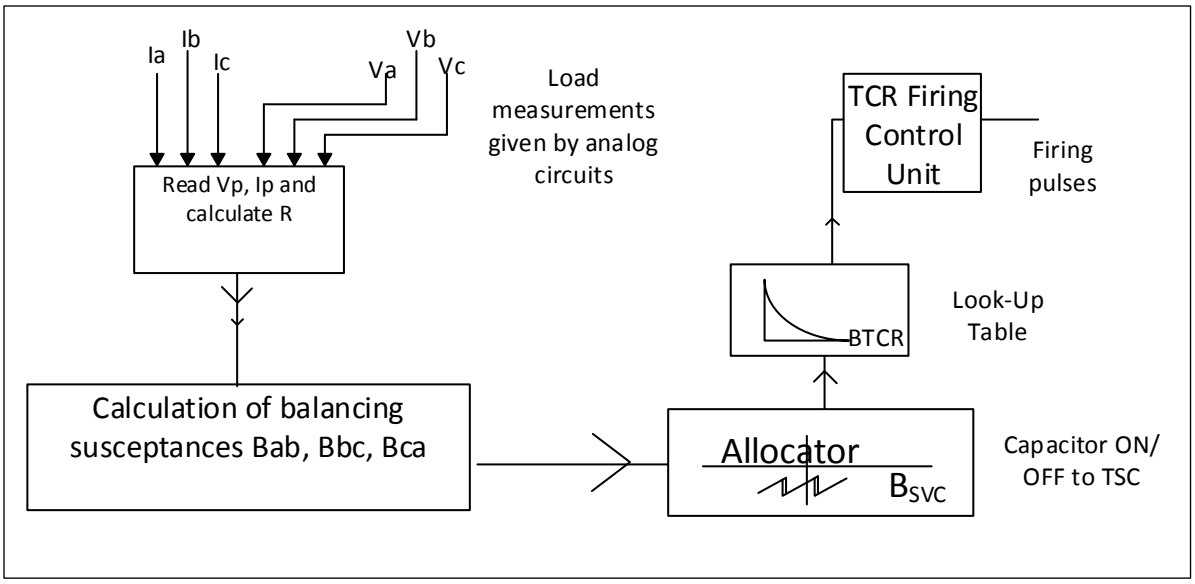


Figure 5.11 Block diagram for on-line load balancing of a purely resistive load.

Given Equations in appendix B, the values needed to compute the balancing values of susceptance are t (turns ratio of the transformer), Xt (Transformer reactance), and $B_{\alpha\beta}$ for each phase of the load and base quantities to calculate the per unit values. Quantities t and Xt are input into the program and values $B_{\alpha\beta}$ are calculated either from peak values of voltage and current for purely resistive loads or from FFT analysis for non-purely resistive loads. Once the balancing susceptances are calculated and converted into per unit values an inner control (susceptance controller) decides the switching of the capacitors. Once the proper amount of capacitors is on the susceptance needed from the TCR is calculated according to Equation 5.6. The values of B_{TCR} per unit are limited from zero to -1.1. Then, the values of B_{TCR} are multiplied by the B_{base} and divided by the susceptance of the TCR (B_L) in order to be able to use the look up table.

$$B_{TCR} = B_{\alpha\beta} - NB_C \tag{5. 6}$$

$$B_{TCR}(\alpha) = B_L \frac{2\pi - 2\alpha + \sin(2\alpha)}{\pi} \tag{5. 7}$$

For the implementation of Equation 5.7, a piecewise function was used instead of a look-up table but it is called look-up table in this section. The nonlinear function given by Equation 5.7 was plotted (Figure 5.12) and approximated by a series of linear functions at the points marked (*). The figure shows that this piecewise function is a very good approximation to the continuous function and thus it can be used for implementation. Table 5-4 gives the list of ten functions implemented on the DSP. Using these approximations speeds up the processing time because it is faster to compute linear functions than the non-linear Equation 5.7. The values of firing angles (α) obtained from the look-up table are converted into timed pulses. The complete process of firing the triacs is detailed in the next section.

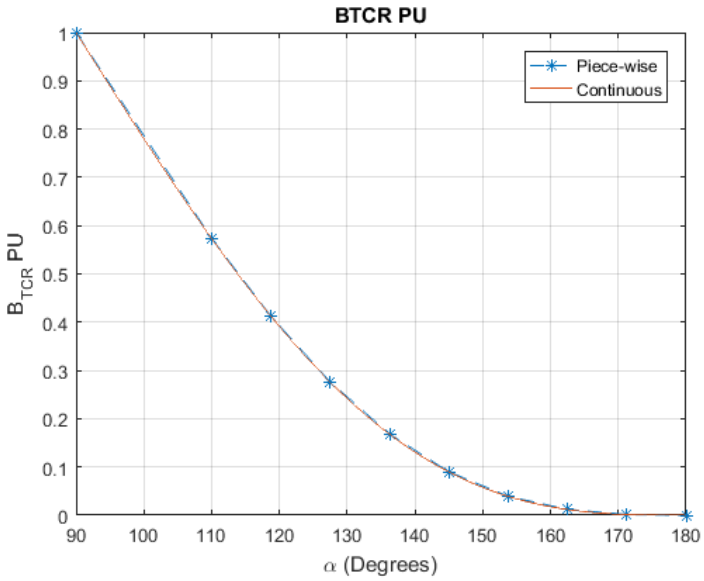


Figure 5.12 BTCR pu vs firing angle.

Table 5-4 Firing angle linearization

$B_{TCR(>)}$	Firing angle (α)	Function for implementation
1.0	90^o	$\alpha = 9000$
0.5732	110^o	$\alpha = -4686.04x + 13686.04$
0.4121	118.75^o	$\alpha = -5431.409x + 14113.28$
0.2759	127.5^o	$\alpha = -6424.38x + 14522.48$
0.1681	136.25^o	$\alpha = -8116.883117x + 14989.45$
0.0898	145^o	$\alpha = -11175x + 15503.51$
0.0391	153.75^o	$\alpha = -17258.38264x + 16049.8$
0.0119	162.5^o	$\alpha = -32169.1x + 16632.81$
0.0015	171.25^o	$\alpha = -84134.61538x + 17251.2$
0.0	180.0^o	$\alpha = -583333x + 18000$
=<0	=<180^o	$\alpha = 18000$

iii) Thyristor firing circuits

The process of firing triacs consists of three main parts; the zero crossing circuit, the digital counter, and the triacs circuit. The zero crossing detector circuits shown in Figure 5.13 a) provides short duration pulses every time the voltage is zero, which means these pulses have a frequency of 120 Hz because the system runs at 60 Hz. When the board receives the zero crossing pulses it starts a 32-bit digital counter on the DSP that is adjusted to represent 0^o to 180^o. The firing pulses are generated when the counter matches a reference given by the alpha value (α) from the look up table and converted into counts. The pulse lasts the necessary amount of time as suggested by the triacs reference sheet. These pulses are isolated through MOC3020 photocouplers and finally fed to the

triacs as shown in Figure 5.13 b). Since all the thyristors needed here come in antiparallel pair triacs can be used in order to simplify the hardware model. The important parameters to be considered when turning on a triac are the turn on current, the open voltage, and the pulse duration.

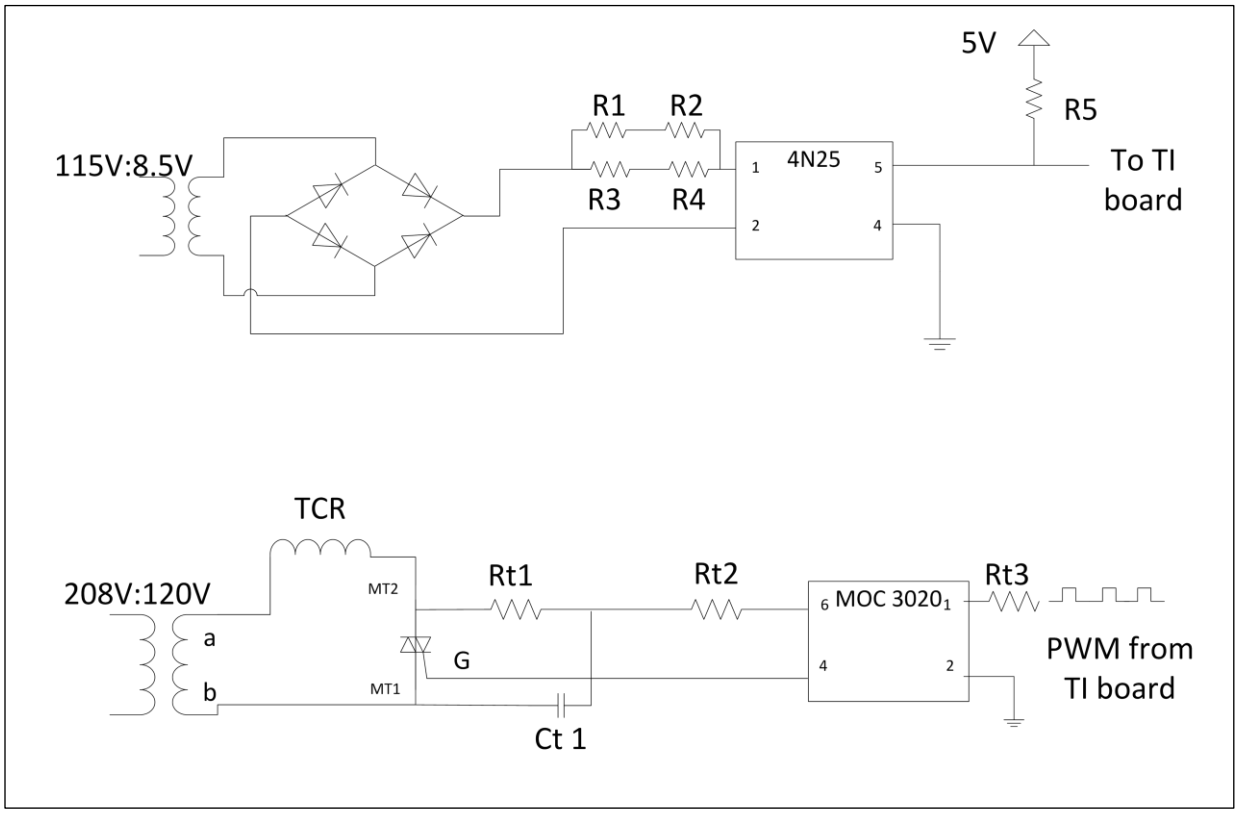


Figure 5.13 a) Zero crossing circuit and b) Firing through isolation circuit.

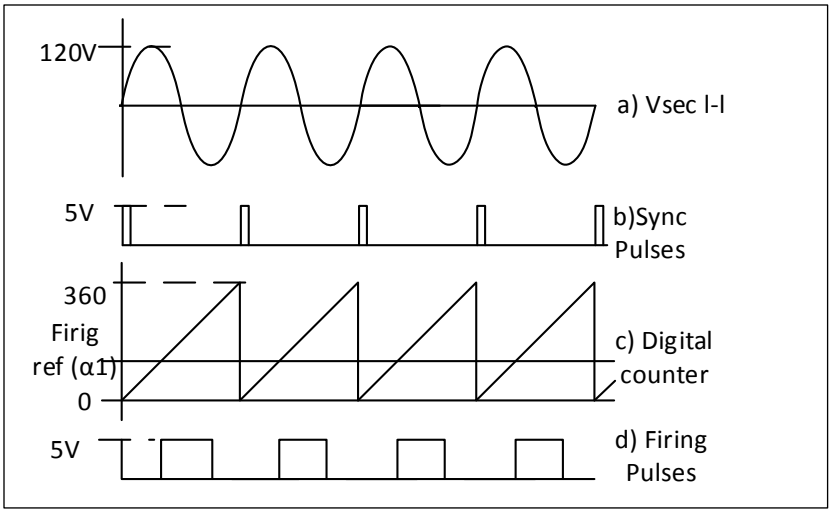


Figure 5.14 Firing pulse generation process.

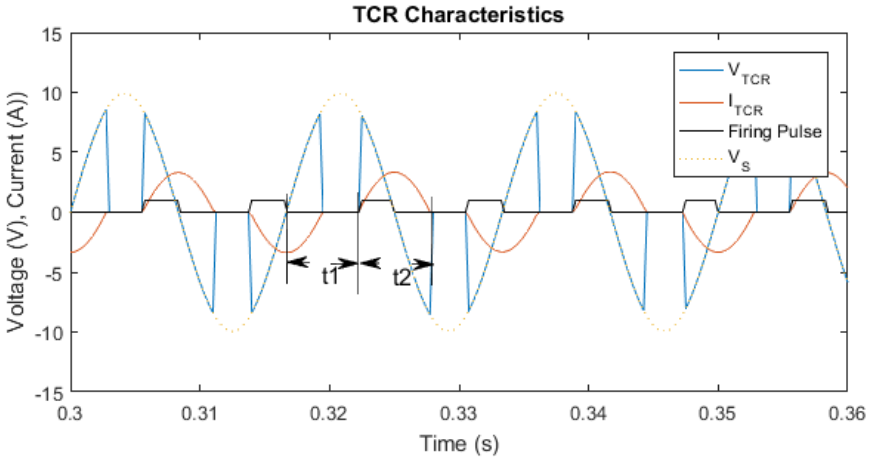


Figure 5.15 TCR Characteristics for a firing angle of 120^{o}.

Details of the PWM process are shown in Figure 5.14 and Figure 5.15 shows important characteristics of the TCR when it is fired at an angle (α=120^{o}). Figure 5.15 shows that the triac is off during time t1 (positive half cycle) and it starts conducting when the pulse comes in. There is

no need to turn off the triacs because they turn off when the current across them equals zero. A 3D view of the PC board designed using Altium software is shown in Figure 5.16.

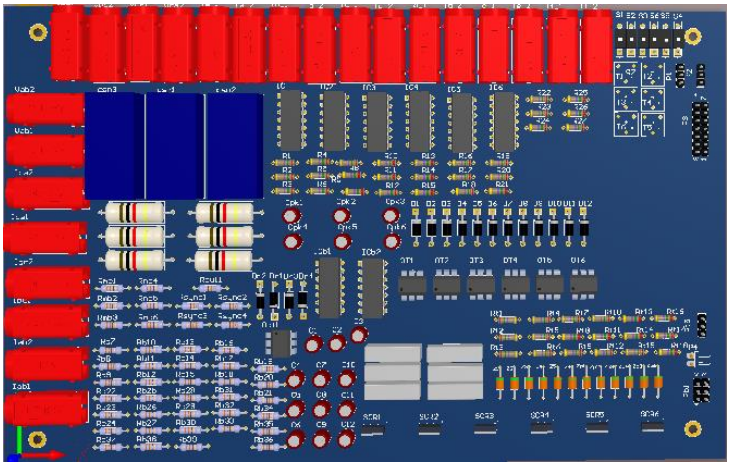


Figure 5.16 3D View of the designed PCB.

5.5 **Experimental Results**

The algorithm presented in this paper was used on the fabricated testbed. A 600 Ohm load was connected between phases A and B, giving unbalanced currents as shown in Figure 5.17. Note that IA = -IB, and IC = 0. The SVC could produce compensating currents as shown in Fig. 5. 19 [32]. The resulting source side current is thus essentially balanced as shown in Figure 5.18 [32], demonstrating the effectiveness of the approach. The load currents were plotted using a separate oscilloscope and the phase relationship cannot be easily identified between them and the other waveforms. They are also of a different color. The waveform is not purely sinusoidal because the SVC is a 6-pulse device and no harmonic filters were used. Table 5-6 shows that the line currents are mostly balanced, i.e., with nearly equal magnitudes and approximately 120^{o} phase shifts. Additionally, it is clear that the power factor is also essentially 1.

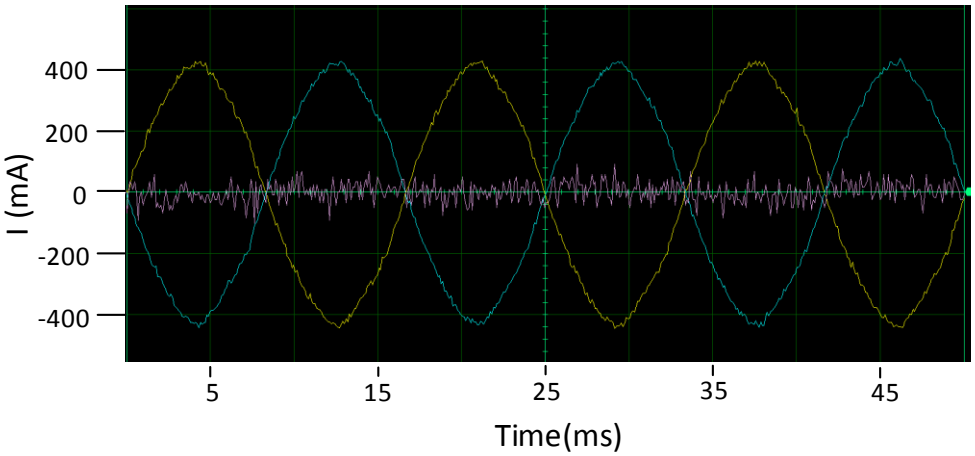


Figure 5.17 Unbalanced line load currents.

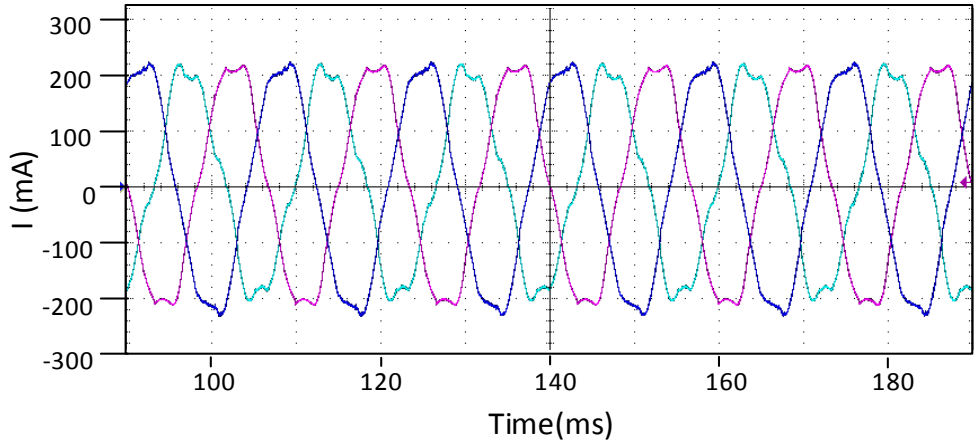


Figure 5.18 Balanced line source currents.

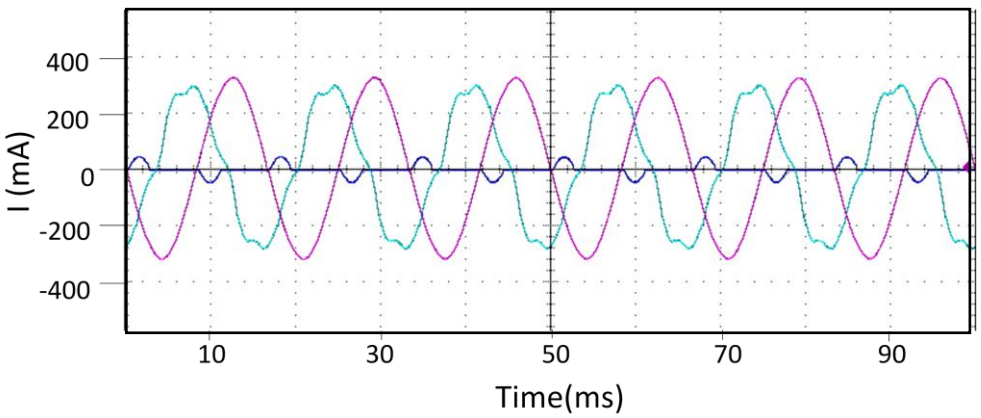


Figure 5.19 Compensating line currents from SVC.

Table 5-5 System line and SVC phase currents

Current	**Value**	
	RMS Current	***Phase***
Load current (unbalanced)		
Line A	300 mA	0^o
Line B	290 mA	180^o
Line C	0	----
Source current (balanced)		
Line A	160.9 mA	0.0^o
Line B	144.5 mA	-124.6^o
Line C	156.3 mA	123.8^o
SVC line current		
Line A	18.4 mA	
Line B	204.2 mA	
Line C	224.0 mA	

The set-up using LabVolt components, TI board and thyristor firing circuits are illustrated in Figure 5.20. This figure shows the custom made interface circuits being connected to the already existing laboratory equipment.

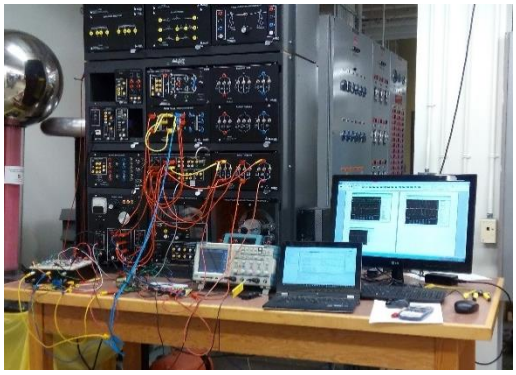


Figure 5.20 Complete set-up using LabVolt components.

5.6 Chapter Conclusions

In this chapter, the complete process for building a lab scale SVC was described. Two of the most important parts of the process are the flow diagram for the programming of the load-balancing algorithm and the PCB for the interconnection of all the parts of the SVC. This process was programmed for online applications using a TI microcontroller board. Results show that the load balancing is effectively achieved and that the power factor correction gets close to unity.

CHAPTER 6 Concluding Remarks and Future Work

This thesis discusses load balancing by means of an SVC. This study includes a thorough investigation on the literature of this topic and the basics of the SVC components and its operation. Following the literature review, an algorithm for load balancing using a 12-Pulse SVC is designed. This algorithm was simulated using EMTP/PSCAD software and further validated by a lab scale-model developed for this purpose.

The first step was to conduct a comprehensive literature review on the techniques used for load balancing with an SVC. While the use of SVCs has been around for several years, it was evident that not enough research has been done on certain topologies of the SVC and combinations of its control system. For example, a 12-pulse load balancing SVC is not commonly used and neither is the application of load balancing in combination with voltage regulation. Therefore, this thesis shows an algorithm to achieve these two things. Furthermore, a lab-scale set up was designed and implemented to complement the results of simulations.

Based on the literature review, simulations results and hardware experiments from the research in this thesis, the general conclusions are as follows:

1) **An open loop control was derived for load balancing**

    - The load-balancing algorithm was based on the Steinmetz method where reactive elements are introduced in a delta connection. However, as these elements were to be implemented on the secondary side of a transformer, another contribution of this work was the derivation of mathematical equations to compensate for the transformer reactance.

- The resulting equations derived for the Y-Y and Y-D connections are different, and have to be appropriately implemented in hardware. This is especially important when performing load balancing using a 12-pulse SVC.

2) **A simulation model of the compensation for a 6-pulse and 12-pulse SVC was developed and its steady state as well as dynamic performance was evaluated using electromagnetic transients simulation.**

By running different types of loads and levels of unbalance, the following conclusions are derived:

- It was observed that the balancing algorithm reduced the current unbalance significantly. For example, the unbalance of a system was reduced from 100 % to 2.67 %, and for smaller levels of unbalance, the resulting unbalance was below this 2.7 %.
- The response of the system to a sudden change (from 0% unbalanced to 100% unbalanced) happens in terms of milliseconds (ms); 400 ms in a 6-pulse SVC and 600 ms in a 12-pulse SVC
- SVCs add harmonics into the system but there are differences in harmonics content for a 6-Pulse and a 12-pulse SVC. In a 6-pulse SVC without any added filters, the Total Harmonic Distortion (THD) is below 5% for the base case and it is shown that the there is a tendency for this percentage to increase as the load increases and vice versa. Note that in this thesis, ac filters were not considered, being one reason for the harmonics, which increase with the loading. The harmonics most notable in a 6-Pulse SVC are 7^{th}, 9^{th}, 11^{th} and 15^{th}

- For the 12-pulse case, the load balancing algorithm requires different susceptances in each phase, and consequently unequal firing angles. Hence, the natural cancellation of the 6n+/- 1 harmonics for odd n no longer happens. For the 12-pulse SVC the THD is 0.81 % for the base case and included harmonics of order 3^{rd}, 5^{th} and 11^{th}. In the examples considered, the higher loads were actually more balanced and so showed lesser harmonic content. At high loads, only the 11^{th} harmonic was dominant.

3) **The Load Balancing Control method was enhanced with the addition of a voltage regulation closed loop control system.**

- The addition of the closed loop does not interfere with the existing load balancing algorithm and it can be implemented using a 6-pulse or 12-pulse SVC. The control system of the voltage regulator was independently tuned by trial and error with satisfactory results. Even though this thesis only constructed a working 6-pulse SVC prototype due to hardware availability issues, the applicability to a 12-pulse SVC was tested and confirmed using EMT simulation.

4) **Validation of Algorithm through hardware experimentation**

- A lab-scale 6-pulse SVC prototype was built to demonstrate the algorithm for load balancing. The algorithm was optimized so that it could be implemented in real-time on a Texas instruments (TI- F28M35x DSP) microcontroller and do automated balancing on-line. The results from this prototype show satisfactory results.
- An open source guideline for design and implementation of the power electronics board for interconnections was developed.

- A PCB board was designed and assembled. This PCB interconnects a DSP, power electronics and existing equipment in power systems lab.

Future Work

Two things to consider for future work:

- Optimize the distribution of load balancing between the two sides (Y-Y and Y-D transformer connected sides) of a 12-pulse SVC to see if the harmonics reduce. For example 60% and 30% as opposed to 50%-50%.
- Test the 12-Pulse SVC in a lab size set-up.

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Appendix I

A. Complete solutions to balancing equations

Solutions for the open loop control susceptances with reactance of transformer (Xt) included

Y-D Transformer

$$BsvcAB = (t^2(2BlTR - \sqrt{3}\,GRS + \sqrt{3}\,GTR + \sqrt{3}\,BlTR * GRS\,t^2\,Xt - GRS^2\,t^2\,X - \sqrt{3}\,BlTR\,GST\,t^2\,Xt + GRS\,GST\,t^2\,Xt - GST^2\,t^2\,Xt + GRS\,GTR\,t^2\,Xt + GST\,GTR\,t^2\,Xt - GTR^2\,t^2\,Xt + BlRS\,(2 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,(-1 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))/(3\,(1 + 2\,BlTR\,t^2\,Xt + \sqrt{3}\,BlTR\,GRS\,t^4\,Xt^2 - GRS^2\,t^4\,Xt^2 - \sqrt{3}\,BlTR\,GST\,t^4\,Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4\,Xt^2 + GRS\,GTR\,t^4\,Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2\,t^4\,Xt^2 + BlRS\,t^2\,Xt(2 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,t^2\,Xt\,(2 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))$$

$$BsvcBC = (t^2(-BlTR + \sqrt{3}\,GRS - \sqrt{3}\,GST + \sqrt{3}\,BlTR\,GRS\,t^2\,Xt - GRS^2\,t^2\,Xt - \sqrt{3}\,BlTR\,GST\,t^2\,Xt + GRS\,GST\,t^2\,Xt - GST^2\,t^2\,Xt + GRS\,GTR\,t^2\,Xt + GST\,GTR\,t^2\,Xt - GTR^2\,t^2\,Xt + BlRS\,(2 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,(2 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))/(3\,(1 + 2\,BlTR\,t^2\,Xt + \sqrt{3}\,BlTR\,GRS\,t^4\,Xt^2 - GRS^2\,t^4\,Xt^2 - \sqrt{3}\,BlTR\,GST\,t^4\,Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4\,Xt^2 + GRS\,GTR\,t^4\,Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2\,t^4\,Xt^2 + BlRS\,t^2\,Xt\,(2 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,t^2\,Xt\,(2 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2Xt)))$$

$$BsvcCA = (t^2(2\,BlTR + \sqrt{3}\,GST - \sqrt{3}\,GTR + \sqrt{3}\,BlTR\,GRS\,t^2\,Xt - GRS^2\,t^2\,Xt - \sqrt{3}\,BlTR\,GST\,t^2\,Xt + GRS\,GST\,t^2\,Xt - GST^2\,t^2\,Xt + GRS\,GTR\,t^2\,Xt + GST\,GTR\,t^2\,Xt - GTR^2\,t^2\,Xt + BlRS\,(-1 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,(2 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))/(3\,(1 + 2\,BlTR\,t^2\,Xt + \sqrt{3}\,BlTR\,GRS\,t^4\,Xt^2 - GRS^2\,t^4\,Xt^2 - \sqrt{3}\,BlTR\,GST\,t^4\,Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4\,Xt^2 + GRS\,GTR\,t^4\,Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2\,t^4\,Xt^2 + BlRS\,t^2\,Xt\,(2 + 3\,BlST\,t^2\,Xt + 3\,BlTR\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlST\,t^2\,Xt\,(2 + 3\,BlTR\,t^2\,Xt - \sqrt{3}\,GRS\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))$$

Y-Y Transformer

$$BYsvcAB = -((t^2\,(-\sqrt{3} * GTR - 3\,BlSTy\,BlTRy\,t^2\,Xt - \sqrt{3}\,BlSTy\,GRS\,t^2\,Xt + \sqrt{3}\,BlTRy\,GRS\,t^2\,Xt + GRS^2\,t^2\,Xt + GST^2\,t^2\,Xt + \sqrt{3}\,BlSTy\,GTR\,t^2\,Xt - GRS\,GTR\,t^2\,Xt + GTR^2\,t^2\,Xt - GST\,(-\sqrt{3} + \sqrt{3}\,BlTRy\,t^2\,Xt + GRS\,t^2\,Xt + GTR\,t^2\,Xt) + BlRSy\,(3 - 3\,BlSTy\,t^2\,Xt - 3\,BlTRy\,t^2\,Xt + \sqrt{3}\,GST\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt)))/(3\,(1 - 2\,BlTRy\,t^2\,Xt - \sqrt{3}\,BlTRy\,GRS\,t^4\,Xt^2 - GRS^2\,t^4\,Xt^2 + \sqrt{3}\,BlTRy\,GST\,t^4\,Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4\,Xt^2 + GRS\,GTR\,t^4\,Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2\,t^4\,Xt^2 + BlSTy\,t^2\,Xt\,(-2 + 3\,BlTRy\,t^2\,Xt + \sqrt{3}\,GRS\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlRSy\,t^2\,Xt\,(-2 + 3\,BlSTy\,t^2\,Xt + 3\,BlTRy\,t^2\,Xt - \sqrt{3}\,GST\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt))))$$

$$BYsvcBC = (t^2(-\sqrt{3}\,GTR + 3\,BlRSy\,BlTRy\,t^2\,Xt - GRS^2\,t^2\,Xt - \sqrt{3}\,BlRSy\,GST\,t^2Xt + \sqrt{3}\,BlTRy\,GST\,t^2Xt - GST^2t^2Xt + \sqrt{3}\,BlRSy\,GTR\,t^2Xt + GST\,GTR\,t^2\,Xt - GTR^2\,t^2Xt + GRS(\sqrt{3} - \sqrt{3}\,BlTRy\,t^2\,Xt + GST\,t^2\,Xt + GTR\,t^2\,Xt) + BlSTy\,(-3 + 3\,BlRSy\,t^2\,Xt + 3\,BlTRy\,t^2\,Xt + \sqrt{3}\,GRS\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt)))/(3\,(1 - 2\,BlTRy\,t^2\,Xt - \sqrt{3}\,BlTRy\,GRS\,t^4\,Xt^2 - GRS^2\,t^4\,Xt^2 + \sqrt{3}\,BlTRy\,GST\,t^4\,Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4\,Xt^2 + GRS\,GTR\,t^4\,Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2\,t^4\,Xt^2 + BlSTy\,t^2\,Xt\,(-2 + 3\,BlTRy\,t^2\,Xt + \sqrt{3}\,GRS\,t^2\,Xt - \sqrt{3}\,GTR\,t^2\,Xt) + BlRSy\,t^2\,Xt\,(-2 + 3\,BlSTy\,t^2\,Xt + 3\,BlTRy\,t^2\,Xt - \sqrt{3}\,GST\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt)))$$

$$BYsvcCA = -((t^2(-\sqrt{3}\,GST - 3BlRSy\,BlSTy\,t^2\,Xt + GRS^2t^2Xt + \sqrt{3}\,BlRSy\,GST\,t^2Xt + GST^2t^2Xt - \sqrt{3}\,BlRSy\,GTR\,t^2Xt + \sqrt{3}\,BlSTy\,GTR\,t^2Xt - GST\,GTR\,t^2Xt + GTR^2t^2Xt + BlTRy(3 - 3BlRSy\,t^2Xt - 3BlSTy\,t^2Xt + \sqrt{3}GRS\,t^2Xt - \sqrt{3}\,GSTt^2Xt) - GRS(-\sqrt{3} + \sqrt{3}\,BlSTy\,t^2Xt + GSTt^2Xt + GTR\,t^2Xt)))/(3(1 - 2BlTRy\,t^2Xt - \sqrt{3}BlTRy\,GRS\,t^4\,Xt^2 - GRS^2t^4\,Xt^2 + \sqrt{3}BlTRy\,GSTt^4Xt^2 + GRS\,GST\,t^4\,Xt^2 - GST^2\,t^4Xt^2 + GRS\,GTR\,t^4Xt^2 + GST\,GTR\,t^4\,Xt^2 - GTR^2t^4Xt^2 + BlSTy\,t^2Xt\,(-2 + 3BlTRy\,t^2\,Xt + \sqrt{3}GRS\,t^2Xt - \sqrt{3}\,GTR\,t^2Xt) + BlRSy\,t^2\,Xt(-2 + 3 * BlSTy\,t^2Xt + 3BlTRy\,t^2\,Xt - \sqrt{3}GST\,t^2\,Xt + \sqrt{3}\,GTR\,t^2\,Xt))))$$