Real-Time and Non-Real-Time EMT Simulation of an Alternate Arm Converter

by

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Abstract

This thesis investigates mechanisms for energy balancing in an alternate arm converter (AAC) using detailed real-time and non-real-time electromagnetic transient (EMT) models. A method for regulating submodule capacitor voltages and maintaining energy balance between the ac and dc systems is developed and fully analyzed using detailed EMT simulations. Detailed simulations verify the effectiveness of the submodule capacitor voltage regulation method under normal operating conditions and in response to faults on the dc and ac systems.

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Dedication

To my family and friends for their support.

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List of Symbols

Δt	simulation time-step
θ	power factor angle
μ	onset angle of an overlap period
ϕ	angular difference (between AAC's output phase voltage and current)
ω	angular frequency
AAC	alternate arm converter
AC	alternating current
C	capacitance
DS	director switch
EPLL	enhanced phase-locked loop
FB	full-bridge [submodule]
HB	half-bridge [submodule]
HVDC	high-voltage direct current
I_{m}	peak phase current
L	Inductance
LCC	line-commutated converter
m	modulation index
MMC	modular multilevel converter
MZCS	modified zero-current switching
N	ideal number of submodules
NLC	nearest level control

OOC	overlap onset control
P	real power
PCC	point of common coupling
PLL	phase locked loop
pu	per unit
PWM	pulse-width modulation
Q	reactive power
R	resistance
SM	submodule
VCO	voltage-controlled oscillator
V_{dc}	dc link voltage
V_{m}	voltage magnitude
VSC	voltage-source converter
ZCS	zero-current switching

Chapter 1: Introduction

1.1 Background

In recent years, the continuously increasing demand for electric power and utilization of renewable energy have made high-voltage dc (HVDC) transmission an important player in modern power systems [1]. Instead of using fossil fuels, renewable and sustainable energy sources become major suppliers of power and offer several economic and environmental advantages. In order to connect renewable sources of energy, such as offshore wind and solar power, to an existing power grid, HVDC transmission systems are more suitable compared to conventional ac systems. Conventional ac systems face difficulty and become expensive in long distance, high power transmission compared to HVDC transmission systems [2]. Therefore, HVDC transmission systems are widely used for bulk power transmission over long distances and for connecting renewable energy sources to the grid.

Thyristor-based line-commutated converter (LCC) HVDC transmission systems were commonly used in high power applications. In these conventional HVDC transmission systems, sending and receiving ends are only able to offer limited control. The rectifier side often controls the dc current while the inverter side takes care of dc voltage. For the rectifier and inverter sides, the control parameters are firing and extinction angles, respectively. At the inverter side, if the extinction angle becomes too small, it will result in commutation failure in the converter, which is a major operating abnormality. LCC-HVDC systems also need extensive and bulky filtering and reactive power support at both ends.

Voltage-source converter (VSC)-based HVDC systems have become popular compared to LCC-HVDC transmission systems [1], [3], and [4]. In [5], early generations of VSC-based transmission systems are introduced with comparatively simple and flexible control methods compared to conventional HVDC transmission systems. The schematic diagram of a VSC-based HVDC transmission system is shown in Fig. 1.1.

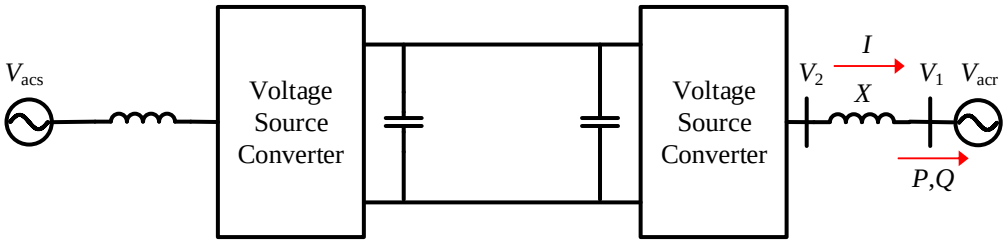

Fig. 1.1: Schematic diagram of a VSC-based HVDC transmission system

In a VSC-based HVDC transmission system, real and reactive power can be controlled independently by adjusting the phase angle and magnitude of the converter's ac terminal voltage. That is, the real and reactive power of ac system can be determined as follows.

$$P = \frac{V_1 V_2}{X} \sin \delta \tag{1.1}$$

$$Q = \frac{V_1 V_2 \cos \delta - V_1^2}{X} \tag{1.2}$$

where V_1 and V_2 are terminal source voltage and converter's output voltage, respectively, and δ is the phase angle between the phasors of V_1 and V_2. From (1.1) and (1.2), it is seen that the VSC-based HVDC transmission system can easily change power flow direction by simply modifying the phase angle δ. In addition, the VSC-based HVDC transmission system has the capability to interconnect to weak ac systems as well as back-to-back connection of two power systems [1].

In a VSC-based HVDC transmission system, power electronic devices need to operate with high voltage and high switching frequencies leading to high conduction and switching losses. Since the conduction and switching losses of semiconductors are high, the overall efficiency of a VSC will decrease. Moreover, the semiconductors used in a VSC need to be able to withstand large magnitudes of voltage and conduct large currents during steady-state operation. From the perspective of converter costs, the switching devices in a VSC would be expensive to meet all requirements of bulk power applications. Due to operation with high switching frequencies, some level of ac filters may be required to remove high-frequency harmonics. The other shortcomings of VSC-based HVDC transmission systems are related to electromagnetic interference and transformer insulation problems [4]. In order to improve the performance of converters from dynamic behavior and cost perspectives, multilevel voltage-source converters were developed for HVDC transmission.

There are different types of multilevel converters for VSC-based HVDC transmission including the neutral-point diode clamped [6-9] and flying capacitor converters [10]. By using multilevel converters, power and switching frequency ratings for semiconductor devices are reduced to lower values. Although multilevel converters can improve the ratings and dynamic response of HVDC transmission systems, there are disadvantages related to such converter configurations. As the number of voltage levels increases, the topologies of multilevel converters become increasingly more complex. That is, the number of semiconductor devices and the footprint of multilevel converters increase dramatically as the voltage levels increase. In addition, the control complexity of gate pulses for switching devices will increase significantly. In practice, HVDC transmission systems with conventional multilevel converters have been limited to three-level converter

topologies. Higher-level converters (five and above) have been used in lower-power applications such as electric motor drives. To overcome the difficulties of using conventional multilevel converters for HVDC transmission, modular multilevel converters (MMCs) have been proposed and implemented [11].

A modular multilevel converter topology is based on identical building blocks, e.g., half-bridge (HB) or full-bridge (FB) submodules [12]. Compared to conventional multilevel converters, MMCs have more scalability and modularity regardless of the voltage levels of an HVDC transmission system. Submodules of MMCs allow the semiconductor devices to have lower ratings and lower switching frequencies, resulting in lower conduction and switching losses. Overall MMCs have higher efficiency compared to conventional multilevel converters in high power applications. In [13], MMC control schemes and operating principles are reviewed and compared. Due to the identical structure of submodules, the controlled gate pulses of switches would be generated according to different techniques including various pulse-width modulation (PWM) [14-20] and nearest level control (NLC) methods [21], [22]. As a result, the output voltage of an MMC is close to a purely sinusoidal waveform if the voltage step generated by each submodule is relatively small. MMCs need less or no filtering for high-frequency harmonics, leading to a lower substation cost. Another feature of MMC-based HVDC transmission systems is reduced maintenance costs for the converter. MMCs are always designed to have redundant submodules, which is beneficial if a failure occurs to one or more submodules of the converter.

In HVDC transmission systems, protection of converters and the system itself is a necessary and important consideration. MMCs with HB submodules cannot react to and

block dc fault conditions (as will be detailed later). During a dc fault, even if the switches of HB submodules are turned off, the fault current can still flow from the ac system to the faulted dc system via the reverse-conducting diodes of the submodules, which would result in significant and sustained fault currents. The large magnitude of current flowing through the converter may damage the submodules [23-25]. Ideally, a dc breaker can be implemented for isolating the dc and ac systems during fault condition. However, dc breakers are expensive pieces of equipment and there is no dc breaker with desired ratings that is ready for use in high power applications [26], [27]. Thus, MMC topologies with dc fault blocking capability have become attractive in HVDC transmission systems.

Full-bridge submodules are able to generate output voltages equal to zero, positive and negative of the submodule capacitor voltage [12], [13]. By replacing HB submodules with FB submodules, conventional MMCs have the ability to block current during dc faults without additional devices. During a dc fault, all the switches of the FB submodules will be blocked. The current flowing from ac to the faulted dc system would charge up the submodule capacitors via the reverse-conducting diodes, thereby opposing current flow from ac to dc. Thus, the ac system will be isolated from the faulted dc system. Although conventional MMCs with FB submodules can block dc faults, there are a number of shortcomings related to this topology including lower efficiency and higher costs [28]. From the structure of the building blocks, the number of semiconductor devices in a FB submodule is twice as many as the ones in a HB submodule. With respect to identical system ratings, the overall losses of FB submodules will be much higher than the HB submodules [29-31]. Therefore, it is necessary to develop alternative topologies of MMCs

with dc-fault blocking capability, high efficiency, and relatively low cost for high power applications.

1.2 Problem Statement

As the importance of dc-fault blocking capability increases, alternative MMCs with FB submodules that can replace HB-MMCs have become a growing focus area of research in high power applications. The alternate arm converter (AAC) [32], [33] is a topology in the recently-introduced family of dc-fault blocking MMCs. The AAC operates differently compared to conventional MMCs. During normal operation, the voltage stack of the upper arm creates the positive part of the output phase voltage and the lower arm takes care of the negative portion. Thus, the upper and lower arms are not inserted into the conduction path simultaneously to generate the output phase voltage. As a result, the submodule capacitors of the upper and lower arms do not have equal chances to charge or discharge, leading to voltage variations in the FB submodule capacitors of the AAC. The existing research studies generally focus on biasing the AAC at an operating point at which the net energy exchange of FB submodules is equal to zero without additional control. The presently available energy-balance control methods can only operate the AAC within a limited range of modulation index values.

This thesis investigates ways to improve the energy balancing behavior of FB submodules in both the upper and lower arms of an AAC and to extend its operating region. The energy-balance control method is firstly applied to an AAC system model developed in an electromagnetic transient simulator. A real-time simulation model is also

implemented to further investigate the submodule voltage regulation method and to pave the way for interfacing with an actual AAC hardware.

1.3 Motivations of Research

The motivation of this thesis is to investigate the viability of a new energy-balance control method that can operate an AAC over a larger range of modulation index values. The research studies in this thesis focus on developing a real-time simulation model, which consists of an AAC and its control system in order to demonstrate the effectiveness of this energy-balance method. Steady-state and transient responses of system controllers are evaluated within a complete HVDC system in response to a wide range of operating conditions including normal voltage and power reference variations, and operation under various faults.

1.4 Thesis Organization

The thesis is divided into six chapters as described in the following.

Chapter 2 reviews the importance of alternative MMCs with full-bridge submodules. The AAC's basic operating principles and related energy imbalance issues are discussed in detail. In this chapter, the existing methods used for energy balancing in an AAC are reviewed.

Chapter 3 introduces and discusses the overlap onset control (OOC) method used for energy balancing in an AAC and for regulating submodule capacitor voltages to the desired value. A zero-current switching (ZCS) control is developed to commutate arm currents

during an overlap period. For real-time implementation with large simulation time-steps, a modified zero-current switching (MZCS) control is developed.

Chapter 4 describes the decoupled controllers (in different reference frames) in PSCAD/EMTDC and RTDS models. In this chapter, the control algorithm of AAC's director switches is introduced incorporating both OOC and ZCS methods. Moreover, a single-phase phase-locked loop (PLL) known as enhanced phase-locked loop (EPLL) is discussed.

Chapter 5 presents simulation results from both the PSCAD/EMTDC and RTDS models of an AAC-based HVDC system. Steady-state and dynamic behaviors of the energy-balance controllers are evaluated in detail.

Chapter 6 summarizes the contributions of the thesis as well as the key conclusions that are drawn from the studies conducted. In addition, Chapter 6 provides direction for future work on this topic to further extend the developed methods.

Chapter 2: Overview of MMC Topologies with DC-Fault Blocking Capability

In this chapter, a number of MMC topologies with dc-fault blocking capability are discussed. Then the alternate arm (modular multilevel) converter (AAC) is analyzed in Section 2.2.

Recently, MMC topologies using FB submodules with dc-fault blocking capability have become a focusing area of research and development. Maintaining the losses and costs as low as possible is another important consideration in these efforts. The parallel-hybrid MMC with dc-side cascaded FB submodules and the hybrid MMC with ac-side cascaded FB submodules will be briefly introduced and discussed in Section 2.1.

Although alternative MMCs with FB submodules can achieve the goals of reduced losses and dc-fault blocking capability, there are still shortcomings related to the hybrid MMCs. Therefore, the AAC becomes one of the better options. The basic operating principles of AAC are described in Section 2.2. In addition, the related energy-balancing issues of an AAC and existing research studies for solving problems will be discussed in detail.

2.1 Review of Alternative MMC Topologies

Conventional FB MMCs have been considered in HVDC system to block dc faults as an alternative to using dc breakers. However, FB submodules directly implemented as a replacement for HB submodules will increase the cost (twice as many switches) and losses of the converter. Consequently, alternative MMCs [34] with FB submodules have been

developed with dc-fault blocking capability; examples include parallel hybrid MMC [35], [36], hybrid cascaded MMC [37-40], and alternate arm MMC [32], [41].

The schematic diagram of a hybrid MMC with dc-side cascaded FB submodules is shown in Fig. 2.1 [37], [38]. Each phase consists of a FB director switch and a series connection of FB submodules. For FB submodules, the output voltage can be either zero, positive, or negative of the submodule's capacitor voltage. With a FB cascade connection, the output of each phase can be controlled according to the reference voltage. Before operation of FB director switches, the output voltage of each phase synthesizes a fully rectified sinusoidal waveform with the desired magnitude. The FB director switches operate based on the reference sinusoidal waveform at fundamental frequency. The switches are controlled by zero-voltage switching method, which means that S_{a1} and S_{a4} conduct during the positive half-cycle of the reference waveform and S_{a2} and S_{a3} operate during the negative half-cycle. When there is a dc fault, the hybrid cascaded MMC with dc side FB submodules can oppose the current flow from the ac side to the faulted dc side by blocking all FB submodules. In addition, the FB director switches operate based on the direction of fault current. The fault current will charge up the capacitors of cascaded FB submodules, resulting in isolation between the ac and dc systems.

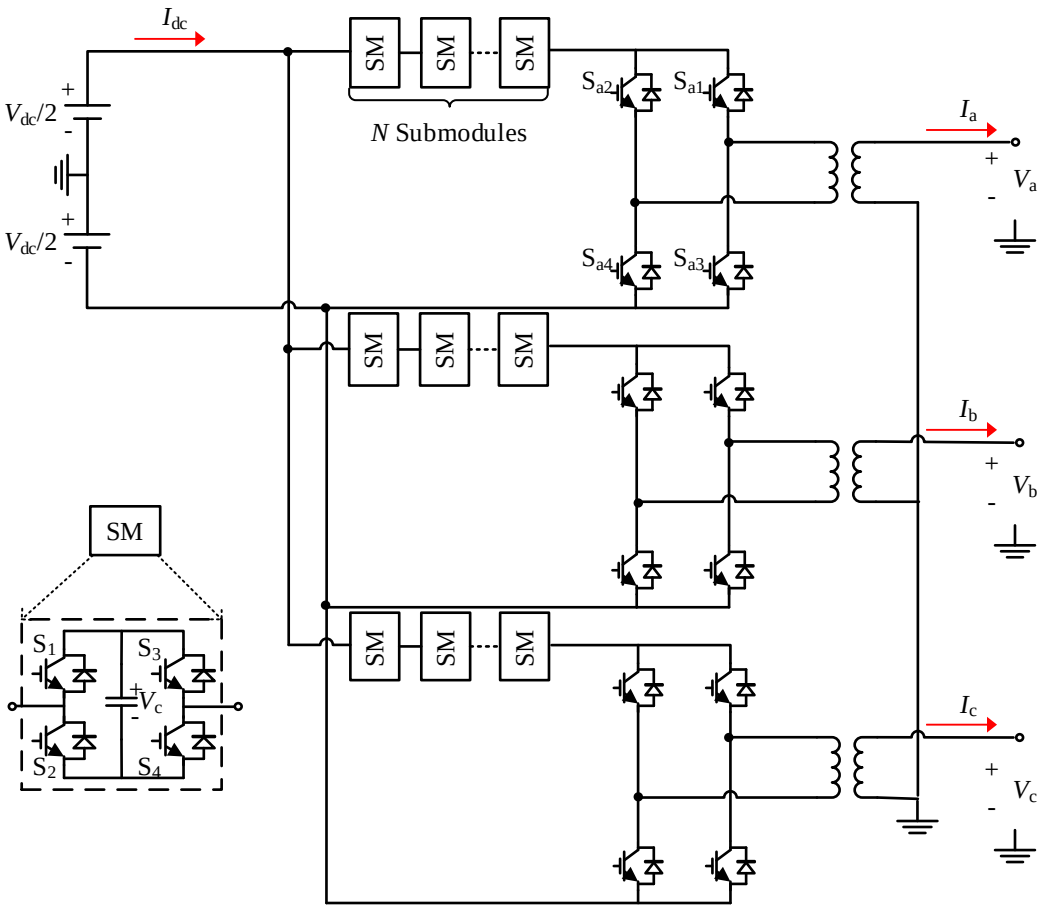

Fig. 2.1: Schematic diagram of hybrid MMC with dc-side cascaded H-bridge submodules.

The schematic diagram of the hybrid cascaded MMC is shown in Fig. 2.2 including its main power stage and active power stage [39], [40]. The main power stage uses HB submodules in series, which is the same as the conventional MMC. The main power stage is connected through a cascaded FB chain link to the ac system, and enables dc fault blocking. For normal operation, the cascaded FB chain link behaves as an active filter. The active filter stage of the cascaded FB chain link needs to produce a controlled reference waveform in order to attenuate harmonics in the output voltage of the main power stage. When a dc fault occurs, the cascaded FB submodules of the active filter stage can eliminate current flow from ac system to the faulted dc system by blocking all submodules of the

main power stage and active filter stage. The phase current flowing from ac to dc system can charge the submodule capacitors through the reverse-conducting diodes of FB submodules. Consequently, the phase current will be opposed and there will be no inrush current during the fault condition.

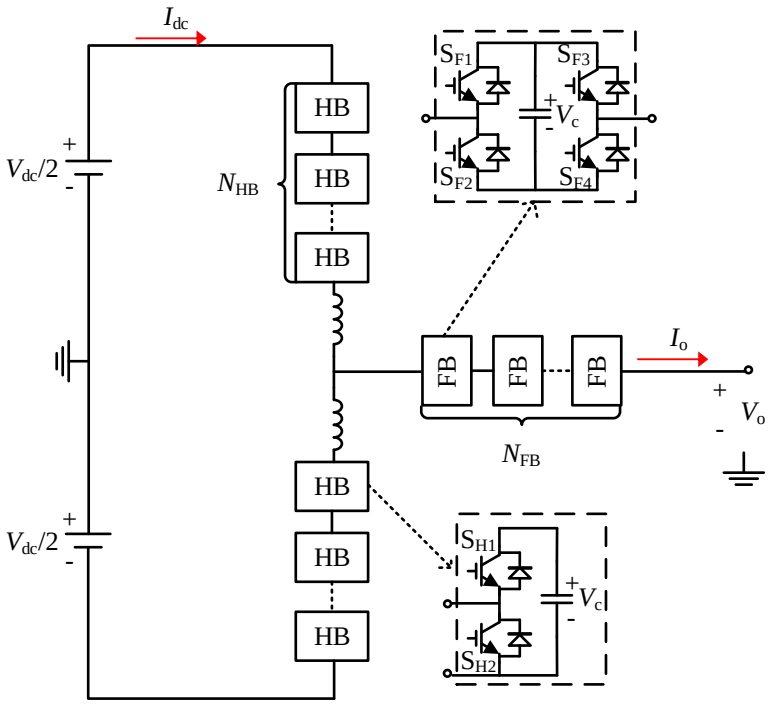

Fig. 2.2: Single-phase schematic diagram of hybrid MMC with ac-side cascaded H-bridge submodules.

Although the above alternative MMCs with FB submodules have dc fault blocking capability, these topologies introduce more operational losses and costs [37]. The hybrid MMC with dc-side cascaded FB submodules has N submodules as shown in Fig. 2.1. For FB director switches of the hybrid MMC, each director switch is implemented with N cascaded semiconductor devices in order to have lower ratings for each device. Therefore, the total number of switches inserted in conduction path would be $4N$ during normal operation, which leads to high costs of semiconductor devices [37]. The hybrid MMC with dc-side cascaded FB submodules uses half of the dc link voltage compared to the

conventional MMC with respect to the same peak magnitude of output voltage [37]. Thus, the rated dc current doubles during normal operation, which leads to higher conduction losses. Also, the hybrid MMC with dc-side cascaded FB submodules is not suitable for long distance applications due to its system ratings with low rated voltage and large rated current [37].

For hybrid cascade MMC with ac-side cascaded FB chain link, the main power stage can produce a staircase output voltage and the cascaded FB submodules take care of harmonic attenuation. Therefore, the reference waveform for the active filter stage must be generated based on the main power stage. However, there is no fixed, prescribed combination of submodules for the HB submodules in the main power stage and FB submodules in the active filter stage. In order to select optimal number of submodules used in the two separate stages, the design process for determining and evaluating different set of numbers can be complex taking into account of performance of harmonic elimination and total conduction losses [42], [43].

Therefore, the alternate arm (modular multilevel) converter (AAC) with dc fault blocking capability has been introduced. The AAC uses FB submodules connected in series for each arm. For each arm of an AAC, a chain link of semiconductor switches operates as the director switch controlling the cascaded FB submodules to synthesize a corresponding portion of the reference waveform. The number of submodules can be easy to determine based on system ratings. The AAC's outputs do not have significant amount of harmonics to be eliminated during normal operation. The detailed operation of AAC will be discussed in the following section.

2.2 AAC's Basics of Operation

2.2.1 Fundamentals

The basic structure of the AAC topology is depicted in Fig. 2.3. The AAC topology is considered to be a hybrid of a two-level voltage source converter and a traditional FB MMC. Each arm of the AAC uses cascaded FB submodules to generate the desired output voltage. A series of IGBTs with reverse-conducting diodes are implemented as director switches to control the operation period of each arm. The AAC arms only conduct during a half-cycle of the desired output voltage waveform. This is done by controlling the director switch corresponding to each arm to produce the desired portion of the output voltage waveform. That is, the upper and lower arms create the positive and negative portions of output voltage, respectively.

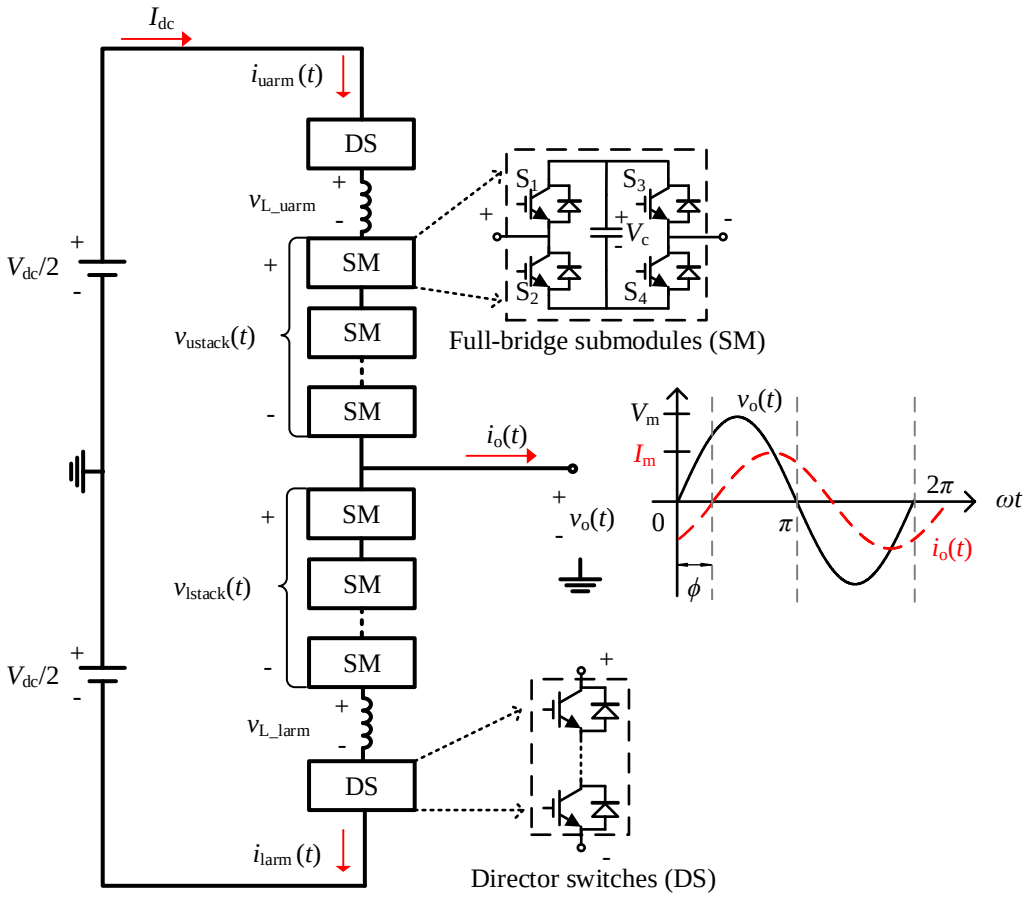

Fig. 2.3: Single-phase schematic diagram of an AAC.

In order to generate the positive half-cycle of the output voltage, the upper arm's director switches insert the upper stack of cascaded FB submodules into the conduction path, which means each arm needs to withstand the maximum stack voltage for half of the dc link voltage of $V_{dc}/2$. The negative portion of the output voltage is applied by the lower arm's director switch and produced based on the lower stack's voltage. The cascaded FB submodules of each stack are responsible for generating the staircase waveform when the corresponding arm is in the conduction path. Assume the output phase current is lagging the phase voltage; the output voltage and current as well as the corresponding references for the upper and lower arms are shown in Fig. 2.4.

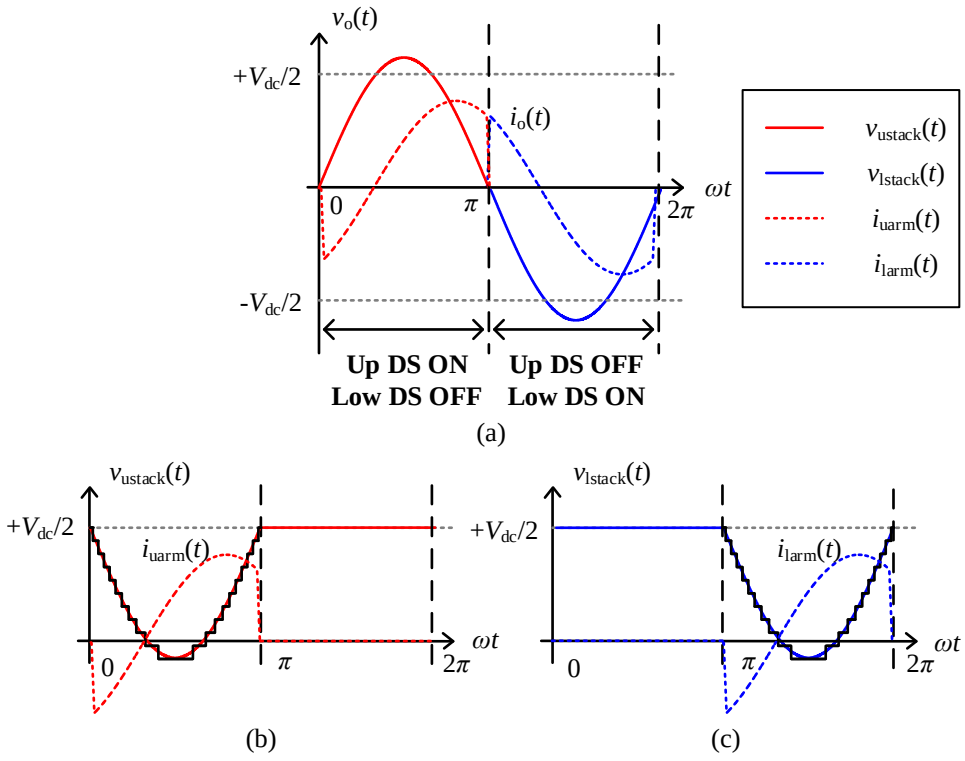

Fig. 2.4: References for upper and lower arms of AAC.
(a) AAC's output voltage and currents, (b) upper stack's voltage and arm current, (c) lower stack's voltage and arm current.

In Fig. 2.4(a), the red and blue curves indicate the conduction periods of the upper and lower arms, respectively. The solid line represents the voltage waveform and the dashed line shows the current waveform. When the output voltage is positive, the upper director switches turn on and the lower director switches turn off. The voltage of the upper arm's stack is inserted in the conduction path and synthesizes the staircase output voltage as shown in Fig. 2.4(b). The corresponding arm current flows through the upper stack as indicated by the red dashed curve. Once the output voltage crosses zero and moves to the negative half-cycle, the upper and lower director switches alter states for creating a continuous output voltage. That is, the lower stack starts to conduct and generates voltage by turning on lower director switches and turning off upper director switches. The

reference voltage waveform for the lower stack is shown in Fig. 2.4(c). The blue dashed line represents the arm current for the lower arm. Since the upper and lower arm currents have the same direction that flow into the positive side of cascaded FB submodules, the arm currents indicated as dashed lines have the same shape as shown in Fig. 2.4 (b) and (c). Based on the single-phase schematic diagram of AAC in Fig. 2.3, the output phase current has an opposite direction compared to the lower arm current. The resulting output phase current is a continuous sinusoidal waveform as indicated in Fig. 2.4(a). Reference voltage waveforms for the upper and lower stacks are given as follows.

$$v_{\text{ustack}}(t) = \frac{V_{\text{dc}}}{2} - \frac{V_{\text{dc}}}{2} m \sin(\omega t) \tag{2.1}$$

$$v_{\text{lstack}}(t) = \frac{V_{\text{dc}}}{2} + \frac{V_{\text{dc}}}{2} m \sin(\omega t) \tag{2.2}$$

where V_{dc} is the dc link voltage and m is the modulation index. The output phase voltage created by the upper and lower arms is as follows.

$$v_{\text{o}}(t) = \begin{cases} \dfrac{V_{\text{dc}}}{2} - v_{\text{ustack}}(t) & \text{if} \quad 0 \le \omega t \le \pi \\ v_{\text{lstack}}(t) - \dfrac{V_{\text{dc}}}{2} & \text{if} \quad \pi \le \omega t \le 2\pi \end{cases} \tag{2.3}$$

Since the output phase current is assumed to be lagging the phase voltage as shown in Fig. 2.3, the corresponding phase voltage and current waveforms are given as follows.

$$v_{\text{o}}(t) = V_{\text{m}} \sin(\omega t) \tag{2.4}$$

$$i_{\text{o}}(t) = I_{\text{m}} \sin(\omega t - \phi) \tag{2.5}$$

where I_{m} is the peak phase current and ϕ is the angular different between phase voltage and current. FB submodules of the upper and lower voltage stacks synthesize the output phase voltage. In (2.4), V_{m} is the peak of phase voltage that is controlled by the modulation index m as follows.

$$V_{\mathrm{m}} = m\frac{V_{\mathrm{dc}}}{2} \tag{2.6}$$

Note that the angular different ϕ between phase voltage and current can be either positive or negative; that is, the actual current can lag or lead the voltage waveform.

2.2.2 Energy Balance in an AAC

In order to produce the desired staircase output phase voltage, the submodule capacitor voltages of both the upper and lower stacks need to be maintained at their nominal value. For energy balancing of submodule capacitors in a conventional MMC, an algorithm is developed based on the capacitor voltages and the instantaneous current [11]. Submodule capacitor voltages are monitored and sorted in either ascending or descending order. When current is flowing from positive to negative polarity of capacitors, i.e., charging the capacitor voltages, capacitors with the lowest voltages are inserted into the circuit. In contrast, capacitors with the highest voltages are discharged once the current flows out the positive polarity of capacitors.

With the conventional sorting and balancing algorithm [11], all submodules of conventional MMC can be charged and discharged in order to balance energy and maintain submodule capacitor voltages at the desired value. Conventional MMC circuits provide equal opportunities for submodule capacitors to charge and discharge during normal operation. However, an AAC has a different situation in that each arm only conducts during

a half-cycle of the desired output voltage waveform. Because submodule capacitors do not have equal chances to charge and discharge over a period, additional control is needed to balance their energy exchange and regulate capacitor voltages to the nominal value.

From an energy-flow viewpoint, if there is no net energy exchange between the converter's dc and ac sides, submodule capacitors can be balanced using conventional sorting and balancing algorithm. Each arm of an AAC conducts only for a half-cycle over a period. The corresponding voltage stack reference voltage and arm current for upper and lower arms are shown in Fig. 2.4 (b) and (c), respectively. For the voltage stack on each arm, the magnitude and shape of voltage and current are identical during the half-cycle conduction period. Thus, the exchanged energy among submodule capacitors within the conduction cycle would be the same for both upper and lower arms. Therefore, the following energy-flow analysis only focuses on the positive half-cycle. During the positive half-cycle, the amount of energy delivered to ac system is given as follows.

$$\begin{aligned} E_{\mathrm{AC}} &= \int_0^{\frac{T}{2}} v_{\mathrm{o}}(t) i_{\mathrm{o}}(t) dt \\ &= \int_0^{\frac{T}{2}} \frac{V_{\mathrm{dc}}}{2} m \sin(\omega t) \cdot I_{\mathrm{m}} \sin(\omega t - \phi) dt \\ &= \left(\frac{m\pi}{4} \right) \frac{V_{\mathrm{dc}} I_{\mathrm{m}} \cos(\phi)}{\omega} \end{aligned} \tag{2.7}$$

Assuming that the dc link voltage is constant, the energy supplied by the dc system in the same period is given as follows.

$$
\begin{aligned}
E_{\mathrm{DC}} &= \int_0^{\frac{T}{2}} \frac{V_{\mathrm{dc}}}{2} i_{\mathrm{o}}(t)dt \\
&= \int_0^{\frac{T}{2}} \frac{V_{\mathrm{dc}}}{2} \cdot I_{\mathrm{m}} \sin(\omega t - \phi)dt \\
&= \frac{V_{\mathrm{dc}} I_{\mathrm{m}} \cos(\phi)}{\omega}
\end{aligned}
\tag{2.8}
$$

The energy difference between dc and ac systems affects the net energy of submodules. Submodule capacitors will be charged or discharged depending on the energy flow within the converter. The energy difference over the positive half-cycle is as follows.

$$
\begin{aligned}
E_{\mathrm{SM}} &= E_{\mathrm{DC}} - E_{\mathrm{AC}} \\
&= \frac{V_{\mathrm{dc}} I_{\mathrm{m}} \cos(\phi)}{\omega} \left(1 - \frac{m\pi}{4}\right)
\end{aligned}
\tag{2.9}
$$

During steady-state operation, the dc link voltage V_{dc} and peak of phase current I_{m} are nearly constant. Since ϕ (the angular difference between phase voltage and current) varies as $-90° \le \phi \le 90°$, the corresponding range for the power factor is $0 \le \cos(\phi) \le 1$. Therefore, the energy difference between dc and ac system varies based on the modulation index of the AAC. The net energy of submodules with respect to modulation index can be described as follows.

$$
E_{\mathrm{SM}} \begin{cases} > 0 & \text{if} \quad m < \dfrac{4}{\pi} \\ = 0 & \text{if} \quad m = \dfrac{4}{\pi} \\ < 0 & \text{if} \quad m > \dfrac{4}{\pi} \end{cases}
\tag{2.10}
$$

From (2.10) the energy supplied by the dc system and the energy delivered to the ac system are equal when the modulation index is $m = 4/\pi$. As there is no energy difference between dc and ac system, the submodules do not need to supply or absorb any energy to balance the system and submodule capacitor voltages are maintained at their desired value. This operating point for a modulation index of $m = 4/\pi$ is called the "sweet spot" [33]. By properly choosing the converter transformer's turns ratio at the "sweet spot", the net energy of submodules can be maintained from the system's point of view. For individual capacitor voltages, a sorting and balancing algorithm is required to charge and discharge capacitors in terms of the measured voltage and current direction.

However, the net energy of submodules is non-zero when the modulation index is not equal to $m = 4/\pi$. When an AAC operates with $m < 4/\pi$, the energy supplied by the dc system is higher than the energy delivered to the ac system, resulting in a capacitor voltage increment. If the modulation index changes to $m > 4/\pi$, the net energy of submodules and individual capacitor voltage decreases, which means the energy absorbed at the ac side is larger than the energy supplied by the dc side. In order to prevent net energy exchange with the submodules, AAC operation needs to be controlled to balance the net energy and regulate individual capacitor voltages to the nominal value. Special methods have been proposed and implemented to eliminate the energy difference by introducing a short period during which both upper and lower arms are inserted into the conduction path. This period is called the overlap period. During the overlap period, upper and lower arms' director switches turn on and upper and lower stacks of submodules start to generate the desired output voltage. Therefore, the resulting circulating current within the AAC helps submodules to supply or absorb power in order to balance the energy mismatch between

dc and ac systems. In addition, adjustment of net energy within the overlap period can maintain submodule capacitor voltages at the desired value [33], [44-51].

For overlap period operation, each arm of AAC needs to insert more submodules in order to regulate individual capacitor voltages. Each arm has N submodules and each submodule capacitor has a voltage rating of $V_{dc}/2N$. In [45] and [46], both arms insert all submodules during the overlap period, which means that the AAC outputs nearly zero voltage instead of tracking the reference output voltage. However, if the overlap period extends too long, the output voltage have noticeable distortion around the zero-voltage region. Therefore, methods as in [33], [47] and [48] that track the reference output voltage during the overlap period have been proposed. In order to track the output voltage during the overlap period, submodules of both arms need to generate voltages higher than $V_{dc}/2$. To create stack voltages higher than $V_{dc}/2$, the number of submodules must be higher than N. The more additional submodules are used during the overlap period, the more negative the output voltage can be tracked and the longer the period both arms can conduct. Although these methods maintain the output voltage when both arms are conducting, the AAC requires additional submodules compared to the non-tracking methods.

When both arms of the AAC conduct simultaneously, the current can quickly commutate with a soft-switching method that opens director switches after the arm current goes to zero. The major purpose of introducing the overlap period is to regulate the energy mismatch between dc and ac systems. Depending on the amount of net energy imbalance, the length of the overlap period varies [45], [46]. If the energy mismatch is small, i.e. when the modulation index is close to the “sweet spot”, the energy can be quickly balanced by implementing a short period of overlap. However, correcting large energy imbalances

becomes impractical because the duration of overlap needs to extend to longer periods. Methods that produce nearly zero voltage by inserting all submodules during the overlap period have significantly distorted output voltage waveforms. As for the reference voltage tracking methods, a longer overlap period results in a larger number of additional submodules to create the negative portion of the output voltage. In addition, the conduction losses increase if both arms of the AAC conduct simultaneously for a long time.

An improved reference voltage tracking method can balance submodule capacitor voltages based on the reference voltage with 3rd harmonic injection [51]. The 3rd harmonic component is subtracted from the stack voltage reference and the AAC is connected to ac system via a Y-Δ transformer. By properly injecting 3rd harmonic component to the reference voltage, the additional number of submodules needed for tracking the output voltage can be decreased, which will reduce the conduction losses as well.

The next chapter will discuss and analyze an improved method to control and balance the energy flow through the AAC arms. This overlap onset control (OOC) approach can track the reference output voltage and extend the range of converter's operation. Since submodules track the reference output voltage, the distortion of phase voltage will be minimal. In addition, the OOC method for energy imbalance does not increase the length of overlap period during which submodules of both arms generate the output voltage, likely resulting in reduced converter losses.

Chapter 3: Overlap Onset Control for Energy Balancing

In this chapter, the overlap onset control (OOC) method for energy balancing and corresponding zero-current switching (ZCS) method for minimizing switching losses are discussed in detail in Sections 3.1 and 3.2, respectively. Moreover, a modified zero-current switching (MZCS) method for real-time simulation is introduced in Section 3.3.

The OOC method can control and balance the energy flowing through the submodules of an AAC. If the modulation index varies and is not close to the “sweet spot”, the OOC helps submodule capacitors of the AAC to maintain zero net energy exchange and retain their nominal voltage. This energy balancing technique for the AAC is based upon modifying the onset of the overlap period instead of its duration. By modifying the onset of the overlap period, the energy transferred from the dc system to the ac system can be balanced and this ensures that the submodule capacitor voltages remain regulated to their desired value. This is accomplished by using a control system that modifies the overlap onset based upon the difference between the average submodule capacitor voltages and the desired capacitor voltage.

In order to maintain low conduction losses and low stress for the switching devices, a ZCS control scheme, also known as soft-switching, is implemented. The ZCS method allows the director switches to turn off when the arm current is reduced to zero. The switching losses of the director switches will then be minimized.

In real-time simulation of an AAC, the sampling frequency may be different (typically lower) compared to the non-real-time PSCAD/EMTDC simulation with arbitrary small time-steps. The time-step of the real-time simulation is 50 μs, which is much larger than

the 1 μs time-step of the PSCAD/EMTDC simulation. Since the regular ZCS method operates by detecting the zero-crossing of the arm current, the detecting signal in real-time simulation becomes inaccurate due to the larger time-step used. If the ZCS cannot behave properly, it may result in a large overshoot in the current that actually increases the switching losses of the director switches. Therefore, a modified ZCS method (MZCS) is necessary for real-time implementation of OOC. The MZCS method predicts the current for the next time-step based on the previous and present values. By modifying the detection signal, the potential overshoot current can be eliminated. Therefore, the switching losses and the rate of change of current can be minimized.

3.1 Overlap Onset Angle

The OOC method can control and balance the energy flowing through the submodules of an AAC. The OOC has an overlap period that is different compared to other methods. In existing methods, the overlap period is often defined as a period of time that is symmetrically located around the zero-crossing of the output voltage waveform. During the overlap period, the director switches of both arms turn on and both stacks conduct simultaneously. However, the OOC method described in this chapter has a different definition for the overlap period. Here the overlap period has a variable onset around the zero-crossing of the output voltage. The end of the overlap period is controlled by the ZCS method, which implies that one arm is switched out of the conduction path once its arm current decreases to zero. Overall, the overlap period have a variable duration and onset depending on the net energy difference of submodules.

Without implementing the OOC method, the instantaneous power flowing through submodules within a half-cycle conduction period is shown in Fig. 3.1. The power of the upper arm is evaluated only for the positive half-cycle of output voltage, which starts from 0 to π. When the AAC operates at the "sweet spot" (i.e., modulation index of $m = 4/\pi$), the total area under the black curve shown in Fig. 3.1 is equal to zero, which means that the net energy exchange of the submodules is equal to zero. As the modulation index decreases to $m < 4/\pi$, the instantaneous power curve is similar to the blue curve in Fig. 3.1. Within a half-cycle conduction period, the positive area is larger than the negative area, resulting in a positive total area. Therefore, the energy supplied by the dc system is higher than the energy delivered to the ac system and the net energy of submodules increases. The instantaneous power curve changes as the modulation index increases to the region of $m > 4/\pi$, denoted by the red curve in Fig. 3.1. The total area under the curve is lower than zero; that is, the energy delivered to ac system is higher than energy supplied by dc system and the net energy of submodules decreases. Therefore, the net energy imbalance of submodules will lead to capacitor voltage variations.

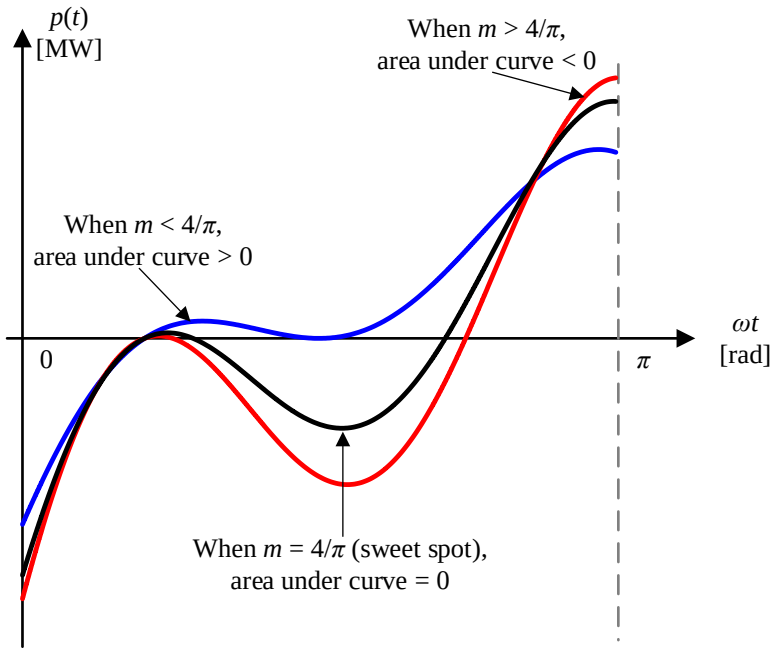

Fig. 3.1: Instantaneous power flowing through submodules for different modulation indices.

Ideally, the upper and lower arms conduct separately for the positive and negative half-cycles of output voltage. For example, the upper arm conducts from 0 to π and lower arm conducts for negative half-cycle from π to 2π. The OOC method introduces a controlled overlap period that modifies the conduction intervals for both arms. The μ represents the overlap onset angle that controls the onset of the overlap period with respect to the zero-crossing of the output phase voltage. If $\mu = 0$, the overlap period starts at the zero-crossing of the output voltage. If $\mu < 0$, the onset of overlap period moves to the left side of zero-crossing. The onset of overlap period starts at the right side of zero-crossing if $\mu > 0$.

Assume the overlap onset μ is smaller than zero, which means the overlap period starts at left side of zero-crossing, the corresponding voltage reference waveforms for OOC operation are shown in Fig. 3.2. In Fig. 3.2 (a), the red and blue curves represent conduction periods for upper and lower arms, respectively. The director switch of the upper arm turns on and the lower arm is taken out, which means the upper arm is conducting from $\mu < \omega t$

$< \mu+\pi$ and the corresponding voltage reference for the upper stack is shown in Fig. 3.2(b). From $\mu+\pi < \omega t < \mu+2\pi$, the lower director switch turns on and the lower stack generates voltage as shown in Fig. 3.2(c). The overlap period finishes as soon as the outgoing arm's current decreases to zero. The duration of the overlap period mainly depends on the rate of change of current for soft-switching method.

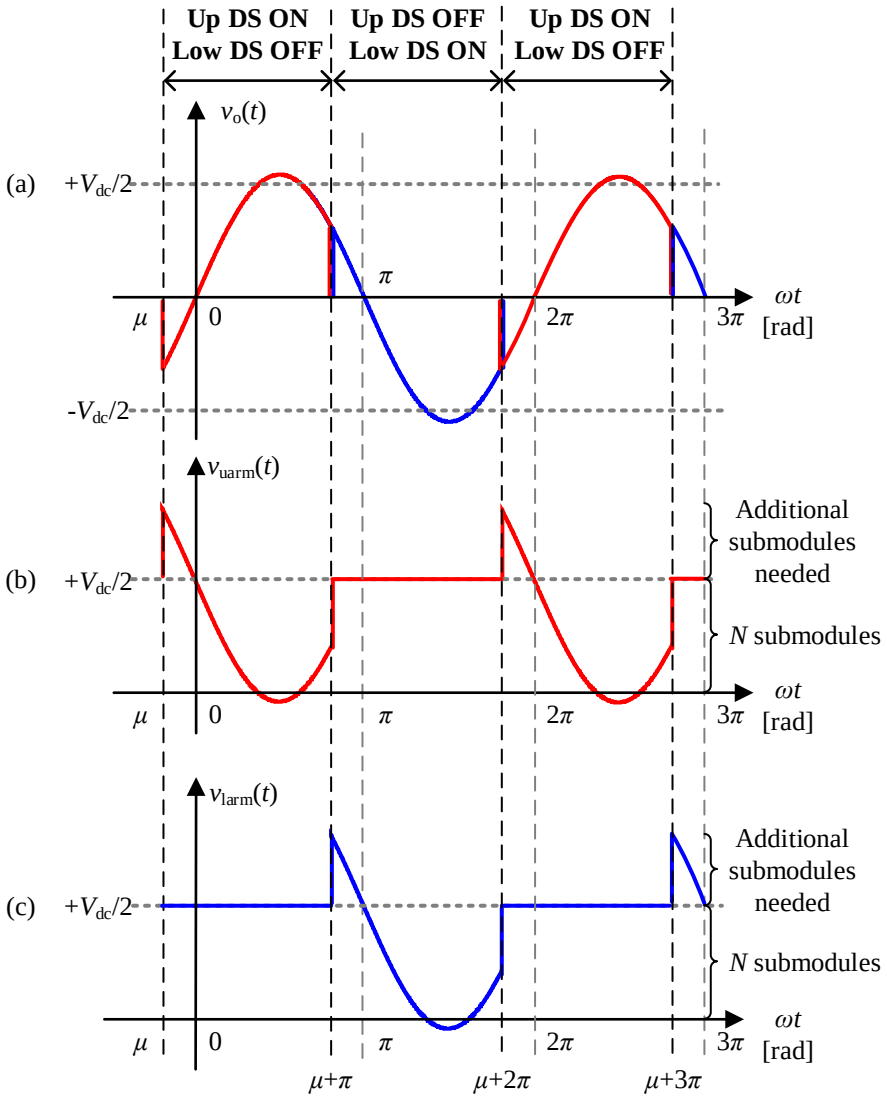

Fig. 3.2: Overlap onset control output and arm voltage waveforms for $\mu < 0$.
(a) AAC's output phase voltage, (b) stack voltage of upper arm, (c) stack voltage of lower arm.

In order to track the output voltage during the overlap period, additional submodules are needed to generate a higher stack voltage. As shown in Fig. 3.2(b), from $\mu < \omega t < 0$, the output voltage is negative and is generated by the corresponding reference for the upper stack voltage. Therefore, the upper stack inserts more submodules than N, creating a voltage higher than $V_{dc}/2$. The operation of the lower arm is similar as shown in Fig. 3.2(c). For the OOC method, if the operating point has a modulation index that is not equal to the "sweet spot", additional submodules are necessary in order to track the output phase voltage. The total number of submodules required for upper and lower arms to construct voltages greater than $V_{dc}/2$ is as follows.

$$N_{\text{total}} = \frac{\frac{V_{\text{dc}}}{2}[1 + m\sin(\mu)]}{V_{\text{cnom}}} \tag{3.1}$$

where V_{cnom} is the nominal voltage of submodule capacitor and μ is the onset angle of overlap period. The additional number of submodules is influenced by the term $m\sin(\mu)$, which is corresponding to the output phase voltage when the overlap period starts. Since the OOC method tracks the output voltage to minimize distortion, the total number of submodules determined by (3.1) could be much larger than the nominal number of submodules N. However, the number of submodules required can be significantly reduced by injecting third harmonic into the reference voltage [51].

By introducing μ as the onset angle of overlap period, the net energy of submodules can be adjusted with variable conduction period of both arms. The instantaneous power curve with OOC method is illustrated in Fig. 3.3.

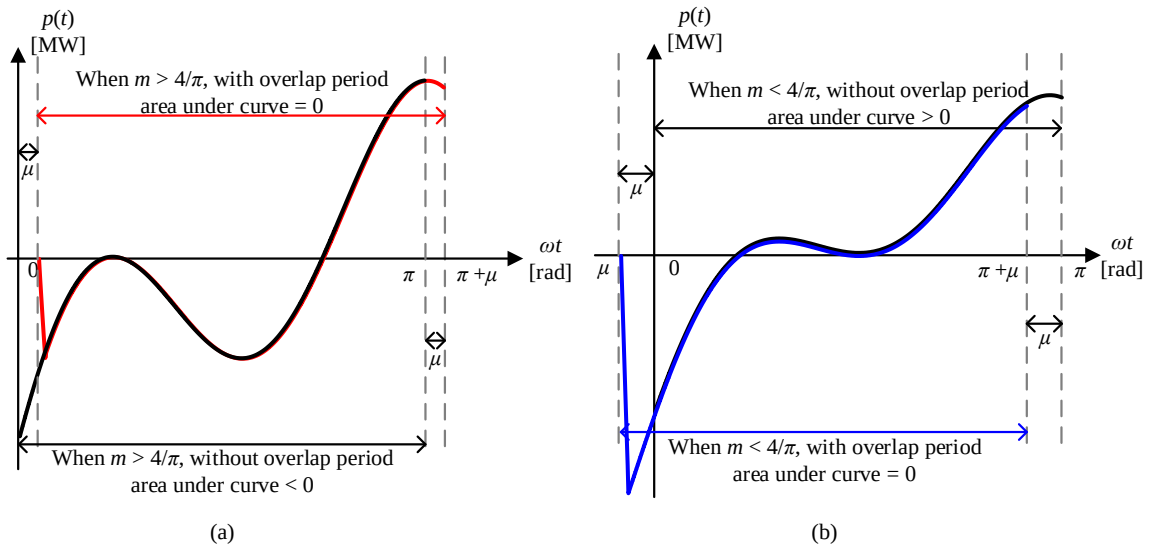

Fig. 3.3: Modifying the conduction interval produces net energy flow of zero for the submodules. (a) modulation index $m > 4/\pi$ with overlap onset $\mu > 0$, (b) modulation index $m = 4/\pi$ with overlap onset $\mu < 0$.

For operation at $m = 4/\pi$, the onset of overlap period is equal to zero with no extra net energy flowing through submodules. In Fig. 3.3(a), the net energy of submodules without OOC method is indicated by the area under black curve. For a modulation index $m > 4/\pi$, the total area under black curve is smaller than zero, leading to the energy supplied by dc system becoming smaller than the energy delivered to ac system and net energy of submodules decreases. As shown in Fig. 3.3(a), the total area under the red curve becomes zero by introducing the overlap period. The resulting onset of the overlap period, μ, is positive and modifies the conduction period by moving it to the right of zero-crossing, which further increases the time duration for charging submodule capacitors. The instantaneous power curve for modulation index $m < 4/\pi$ is shown as the blue curve in Fig. 3.3(b). Without energy imbalance control, the area under black curve is higher than zero, which indicates that the net energy of submodules increases and the energy delivered to ac system is smaller compared to the energy supplied by dc system. By properly adjusting the conduction period with OOC method, the modified power curve has a net energy of zero

that is shown as blue curve in Fig. 3.3(b). The onset angle of the overlap period is negative leading to a prolonged discharge period.

Considering the modified conduction period from $\mu < \omega t < \mu+\pi$ based on the OOC method, the resulting energy difference over the half-cycle when upper arm conducts is as follows.

$$\begin{aligned} E_{\mathrm{SM}} &= E_{\mathrm{DC}} - E_{\mathrm{AC}} \\ &= \int_{\frac{\mu}{\omega}}^{\frac{\pi+\mu}{\omega}} \left[\frac{V_{\mathrm{dc}}}{2} \cdot I_{\mathrm{m}} \sin(\omega t - \phi) - V_{\mathrm{m}} I_{\mathrm{m}} \sin(\omega t) \sin(\omega t - \phi) \right] dt \\ &= \frac{I_{\mathrm{m}}}{\omega} \left[V_{\mathrm{dc}} \cos(\phi - \mu) - \frac{V_{\mathrm{m}} \pi \cos(\phi)}{2} \right] \end{aligned} \tag{3.2}$$

where V_{m} is the peak of phase voltage, I_{m} is the peak phase current and ϕ is the angular different between phase voltage and current. The μ represents the overlap onset angle that determines the starting point of overlap period. From (3.2), the theoretical value of the onset angle that makes net energy of submodules equal to zero is calculated as follows.

$$\mu = \phi - \cos^{-1}\left[\frac{m\pi}{4} \cos(\phi) \right] \tag{3.3}$$

As for normal operation of an AAC, the overlap onset angle is controlled by a feedback system. The schematic diagram of overlap onset controller is shown in Fig. 3.4.

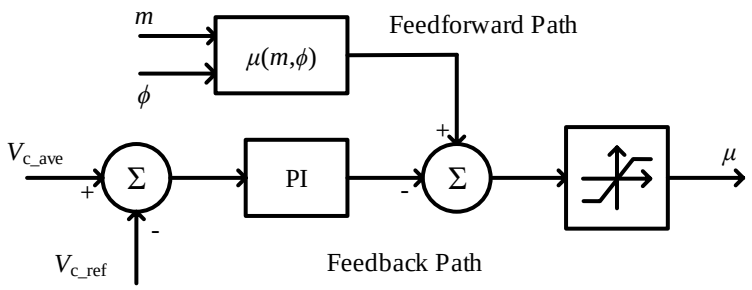

Fig. 3.4: Overlap onset angle controller.

The overlap onset angle μ is determined based on the capacitor voltage difference between the measured average voltage (V_{c_ave}) and the nominal value (V_{c_ref}). Due to the symmetry of the output phase voltage, the defined operating range of overlap onset angle varies from -90° to 90°. In order to improve the response time of the feedback controller, a feedforward path is added to the overlap onset controller to predetermine the value of onset angle. With measured values of modulation index and angular difference between AAC's output voltage and current, the feedforward path can easily calculate the overlap onset angle from (3.3). Then the feedback path can only slightly adjust the angle depending on the measured capacitor voltages.

Once the OOC method is implemented for AAC energy balancing, the overlap onset angle can vary based on the measured submodule capacitor voltages, which means the overlap onset angle controls submodules to supply or absorb power within the system. In order to have minimal switching losses, the director switches need to alter states with the soft-switching method by reducing the corresponding arm current to zero before turning off the director switches. The detailed ZCS control will be discussed in the following section.

3.2 Zero-Current Switching Control

The ZCS method controls the arm current flowing through director switches in order to have minimal switching losses. When the overlap period starts, the corresponding outgoing arm's current is not necessarily equal to zero. During the overlap period, the arm director switches change their states, which can result in excessive current if care is not taken to ensure that the current is commutated in a controlled manner from the outgoing director switch to the incoming director switch. Excessive arm current increases the stress for director switches in terms of the sharp rate of change of current. A ZCS controller is designed to commutate the arm current and ensure the phase current can be conducted continuously.

The operation of ZCS for arm currents is shown in Fig. 3.5. The upper arm current has the same direction as the output phase current. However, the lower arm has an opposite direction compared to the output current. In Fig. 3.5, the arm currents is shown with respect to the overlap period that commutates current from the upper to the lower arm. When the upper arm is in conduction period, the upper director switch turns on and the lower director switch turns off. The output phase current is equal to arm current that flows through the upper arm. Once the OOC method determines the overlap onset angle, the overlap period begins during which both director switches turn on and the output phase current is the sum of both arm currents. In order to achieve ZCS control, the upper arm current decreases gradually within the overlap period. Consequently, the related magnitude of the lower arm current increases to maintain continuous output phase current. As soon as the upper arm current decreases to zero, the overlap period ends and director switches of both arms assume opposite states to what they had prior to the overlap period. By turning off the

upper director switch, the lower voltage stack starts to generate the output phase voltage. Within the conduction period of the lower arm, the output phase current is equal to the (negative of) lower arm current. If the ZCS control operates properly, there will be no large current overshoot while both arms are changing states. In addition, the output phase current would be continuous and with minimal distortion.

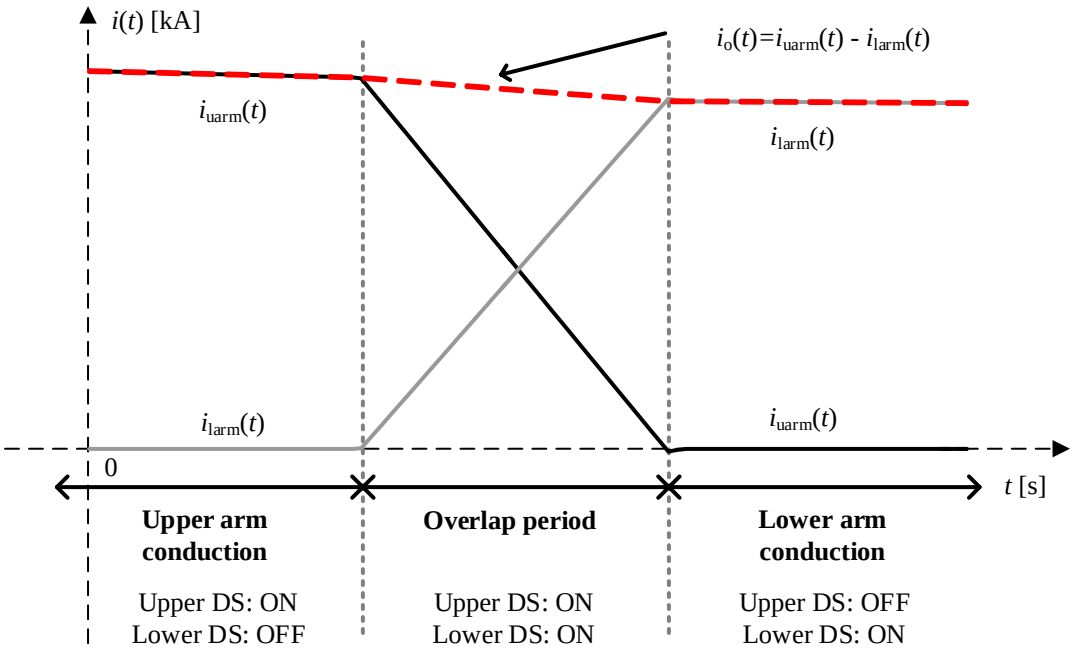

Fig. 3.5: ZCS control of the overlap period.

Since the overlap onset angle can be positive or negative with respect to the zero-crossing of the output voltage, the ZCS control must be able to take care of arm currents for different situations. When the overlap period happens, both arms insert at least N submodules, which results in zero output phase voltage. The total voltage for N submodules is equal to half of dc link voltage, i.e., $V_{dc}/2$. In order to control arm currents, additional operations are needed by varying the voltage across the arm inductor. As shown in Table 3.1, N_{uarm} and N_{larm} are the number of submodules inserted positively during the overlap

period [45]. When the arm currents are zero, there is no extra control needed for ZCS operation. The duration of overlap period will be zero, i.e., both arms can change states immediately. Once the overlap period starts with an arm current higher than zero, the upper and lower arms insert additional submodules leading to N+1 submodules. Due to the zero output voltage, the voltage difference within each arm of the AAC is cancelled out by the voltage across the arm inductor. The resulting negative voltage across the arm inductor tries to induce current flowing in the opposite direction with respect to the corresponding arm current. Thus, arm currents gradually decrease during the overlap period, which is similar to current commutation shown in Fig. 3.5. In contrast, the upper and lower voltage stacks require N-1 submodules if the arm current is negative when the overlap period begins. The arm inductor voltage becomes positive to increase the outgoing arm's current from a negative value to zero. Based on Kirchhoff's Current Law, the incoming arm current increases to have approximately the same current magnitude compared to the output phase current. Note that the lower arm current has an opposite direction in terms of AAC's output phase current.

Table 3.1: ZCS operation control during overlap period [45]

Output Voltage	**Outgoing Arm Current**	N_{uarm}	N_{larm}	**Inductor Voltage**
0	Zero	N	N	Zero
~0	Positive	N+1	N+1	Negative
~0	Negative	N-1	N-1	Positive

Basically, the ZCS method controls the arm currents to perform a soft-switching operation depending upon the number of submodules inserted in the conduction path during the overlap period. Note that the OOC method only controls the onset of the overlap

period. The ZCS method determines the actual duration of overlap period until the outgoing arm has a current magnitude of zero. In terms of ZCS control operation, Table 3.1 does not indicate the only way to commutate current between the arms of AAC. Any number of submodules other than *N* can provide the required positive or negative arm inductor voltage. The current rate of change depends on voltage across the arm inductor and the size of arm inductor.

The ZCS method determines the duration of the overlap period by properly commutating current from the outgoing arm to the incoming arm. After changing the state of director switches, the arm that finishes its conduction period has an arm current of zero. When its director switch turns off, *N* submodules are inserted to keep its voltage stack at $V_{dc}/2$. The reason for maintaining a voltage of $V_{dc}/2$ is that the corresponding arm current will be zero if there is no voltage difference between the stack and dc link voltages. However, the instantaneous voltage of submodule capacitors always varies around the nominal value due to the conduction period for charging and discharging. When the arm is not in the conduction period, the individual submodule capacitor voltage could be a little bit lower or higher than the nominal value. If individual submodule capacitor voltage of outgoing arm is slightly higher than its rated value, the summation of voltage stack will have higher voltage compared to the half of dc link voltage. The voltage difference between the stack and dc link voltages leads to arm current flowing in the outgoing arm. As soon as the overlap period ends, director switches turn off and the corresponding arm that is not conducting should not produce any extra conduction losses. However, the voltage difference makes reverse diodes of director switches change to forward bias region, which enables the current to flow in the outgoing arm, resulting in discharge of submodule

capacitors. Therefore, addition control needs to be implemented in order to fully avoid undesired current flow in the arm that is taken away from the conduction path.

Instead of inserting N submodules, N-1 submodules are used in order to guarantee reverse diodes of director switches do not turn on. Thus, the outgoing arm current is kept at zero and the submodule capacitor voltages would maintain at the same voltage when the arm is switched off.

3.3 Modified Zero-Current Switching Control

The OOC method adjusts the onset of overlap period and ZCS method takes care of the end. The overlap period lasts until the outgoing arm detects a zero-crossing of its current. The gate pulse of its director switch will indicate an OFF state as soon as the zero-crossing of current happens, which implies that the gate pulse always has one time-step delay compared to the zero-current flag. In real-time simulation or in an actual implementation, since all control signals are processed with a large time-step (compared to a non-real-time simulation), the arm current will continue to flow through submodules for an additional 50-μs instead of only 1-μs as in the PSCAD/EMTDC simulation, resulting in a large current going through the reverse diodes of director switches. Since the upper and lower arms are symmetrical, the phase current does not see any significant distortion; however, reverse diodes of director switches would still conduct and the actual overlap period are extended. In order to reduce losses, the current flowing through reverse diodes needs to be minimized properly and the overlap period must end as closely as possible to the true zero-crossing of arm current.

In Fig. 3.6, upper and lower arm currents as well as the output phase current simulated in real-time are illustrated. Ideally, the overlap period must finish as indicated by the vertical black dashed lines with the implemented ZCS method. However, the actual duration of the overlap period wherein both arms conduct together is shown by the vertical red dashed lines. In terms of turn-off operation for the overlap period, the director switches can only alter states when the current zero-crossing detector has a flag of "1". Therefore, in real-time simulation, the director switches will turn off after 50-μs once the arm current detects a zero-crossing. The turn-off command for director switches is shown by the vertical blue dashed line. As shown in Fig. 3.6, both arm currents controlled by the ZCS method continue to decrease before the upper director switches turns off. Since the upper arm has a relatively large current magnitude when the overlap period finishes, the corresponding director switches will turn off with increased switching losses. For the arm that is not going to conduct within the following half-cycle, N-1 submodules are inserted to block and oppose the current flowing in the reverse direction. Thus, the upper arm current needs to commutate slowly through the reverse diodes of director switches, which will extend the conduction period for both arms. Furthermore, the conduction losses of each arm of AAC increase due to the longer conduction cycle.

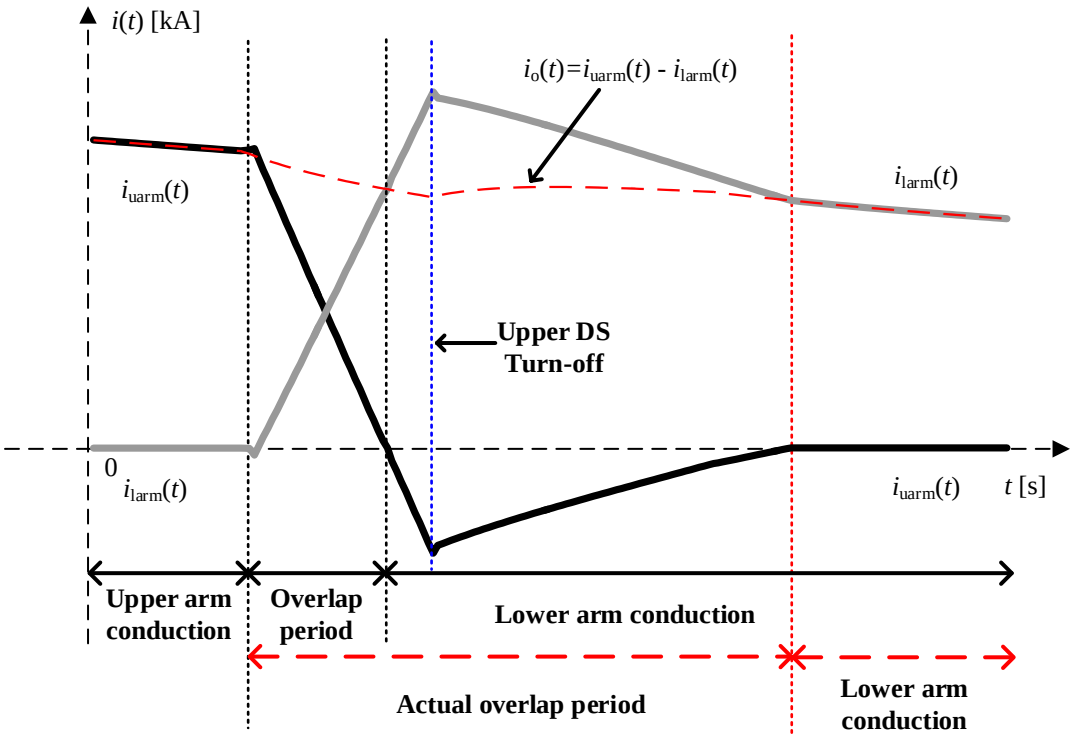

Fig. 3.6: ZCS control of overlap period in real-time simulation.

With regard to minimization of the reverse arm current, a modified ZCS (MZCS) method that predicts the zero-crossing of arm current is introduced and implemented in the real-time simulation. If the arm is not in the conduction path and the number of submodules inserted can properly reverse bias the diodes of the director switches, the major reason of reverse arm current is the additional time-step delay. Instead of detecting the exact zero-crossing for the director switches' turn-off operation, the MZCS method uses values of the arm current from the previous and present time steps and calculates the slope using the two points as follows.

$$k = \frac{I_{\text{now}} - I_{\text{pre}}}{\Delta t} \tag{3.4}$$

where I_{now} and I_{pre} are the present and previous time-step values of the current. Δt is the time-step and k is the corresponding slope. Based on the current value and calculated slope, the arm current for the next time-step can be estimated as follows.

$$I_{next} = I_{now} + k \cdot \Delta t \tag{3.5}$$

where I_{next} is the magnitude of current for the next time-step. Once the overlap period starts, the MZCS method predicts the current value as a flag to decide when the director switches need to turn off. Upon this calculation, if the arm current is predicted to cross zero at the next measurement, the signal for zero-crossing detection goes high in advance compared to the ZCS method. Consequently, the gate pulse for the director switches is one time-step earlier, resulting in much smaller reverse arm current. If MZCS method operates properly, the switching losses of director switches and conduction losses for outgoing arm can be reduced.

However, if AAC only uses MZCS method as a replacement of ZCS method to determine the duration of overlap period in real-time simulation, there are some limitations as discussed below. When the overlap period starts, the MZCS method measures and stores the magnitude of the present and previous time-step currents. If the slope of current is not as calculated, the detection signal for zero-crossing of the arm current will be inaccurate. For example, the slope of current could be calculated before inserting additional submodules to commutate current. Then the predicted rate of change for the arm current is slower than the actual variation, leading to a late detection flag for zero-crossing of current. Thus, the determined overlap period is extended to a longer period and the MZCS method becomes invalid. A possible situation for inaccurate detection is indicated in Fig. 3.7. The overlap period determined by ZCS method in real-time simulation is shown by the black

solid line in Fig. 3.7. Points B and C represent the measured current for the previous and present time-steps. Point A stands for current at the onset of overlap period, which is one time-step ahead of point B. Based on calculation with points A and B, the predicted current for the following time-step will not decrease to zero is shown as point C'. Therefore, the MZCS method performs predetermined calculations for the next time-step as shown in point D in Fig. 3.7. Whereas, the forecasted duration from point A to point D is longer compared to the actual overlap period, which could lead to large reverse current flowing after director switches turn off.

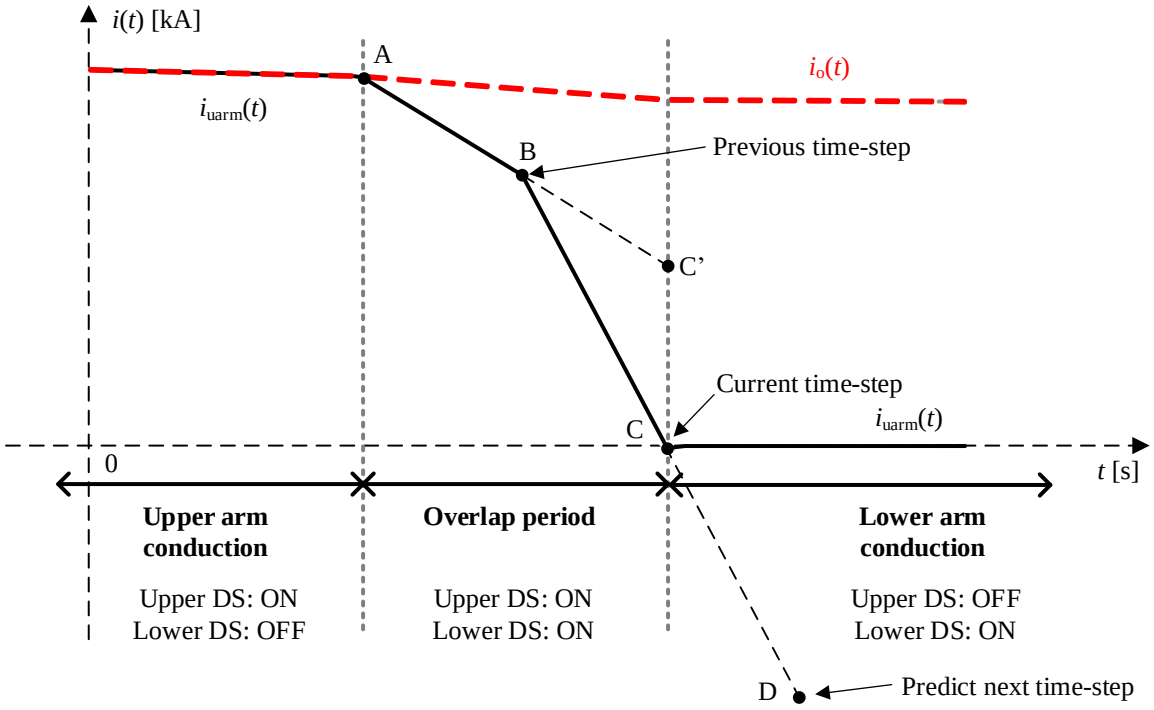

Fig. 3.7: Possible situation for MZCS mal-operation.

Therefore, the MZCS method does not directly replace the original ZCS method. In real-time simulation with a large time-step of 50 μs, the MZCS method only modifies the detection signal for the zero-crossing of the arm current in order to minimize switching losses. If the signal based on predicted calculation detects zero-crossing earlier compared

to the ZCS method, the director switches would turn off depending upon the modified signal. Conversely, if the zero-crossing detector has a flag of “1” before MZCS detection, the gate pulses are controlled by the original ZCS method.

Chapter 4: System Control

The Section 4.1 and Section 4.2 of this chapter will introduce a detailed discussion and derivation of decoupled control for AAC and control logic for director switches during normal operation. Also, a single-phase phase-locked loop (PLL) is implemented for the control system and will be described in Section 4.3.

For the complete system using AAC as a dc-ac converter, a decoupled controller is implemented to control the voltage at the point-of-common-coupling (PCC) and the power order delivered into the ac system. Before designing the decoupled controller, vector decomposition requires transformation from ABC to DQ0 domain. The decoupled controller controls essentially dc values aligned with the d and q axes instead of instantaneous values in the original (three-) phase domain.

With respect to director switches of AAC's two arms, the upper and lower arms become alternating arms by properly turning on and off their director switches. Also, director switches need to finalize control in terms of OOC and ZCS methods for the purpose of balancing energy within the submodule capacitors of AAC. Since the control logic of director switches operates based on the PLL output locked at the PCC, the dynamic and transient responses of the employed PLL become critical to the AAC's operating performance. When the system is unbalanced, the original three-phase PLL may have a distorted output waveform. Therefore, the operation of director switches could be affected by the PLL waveform with distortion. In order to reduce the sensitivity caused by the PLL, a single-phase PLL known as enhanced PLL (EPLL) is discussed and implemented [52].

4.1 Decoupled Control of Power and Voltage

In order to control the AAC system with a decoupled controller, a transformation from ABC to DQ0 domain needs to be implemented for vector decomposition. The ABC to DQ0 transformation transfers three-phase quantities (ABC quantities) to quantities in terms of two axes. By implementing this transformation, the instantaneous three-phase values become two potentially constant values. Therefore, the control scheme for power and voltage of three-phase system would be simpler to analyze and develop.

The ABC to DQ0 transformation uses reference frames as shown in Fig. 4.1. The $v_a(t)$, $v_b(t)$ and $v_c(t)$ represent the three-phase sinusoidal signals. The rotating frame consists of d and q axes where the q axis is perpendicular to d axis. In Fig. 4.1(a), the q axis is leading the d axis and the d axis will be aligned with vector $v_a(t)$ when $t = 0$. One possible reference frame is shown in Fig. 4.1(a) and another reference frame for vector decomposition is indicated as Fig. 4.1(b). In the rotating frame in Fig. 4.1(b) the d axis is rotated 90 degrees back with respect to vector $v_a(t)$. The q axis lags the d axis where the q axis will be aligned with vector $v_a(t)$ when $t = 0$. Assuming the transformation is applied to signal $v(t)$, the corresponding vector components V_d and V_q aligned with d and q axes are shown by the red solid line with an arrow. In terms of different reference frames, the related transformation matrices used for decomposition would be different. In the following subsections, the ABC to DQ0 transformation matrices for rotating frames as in Fig. 4.1 will be introduced in detail.

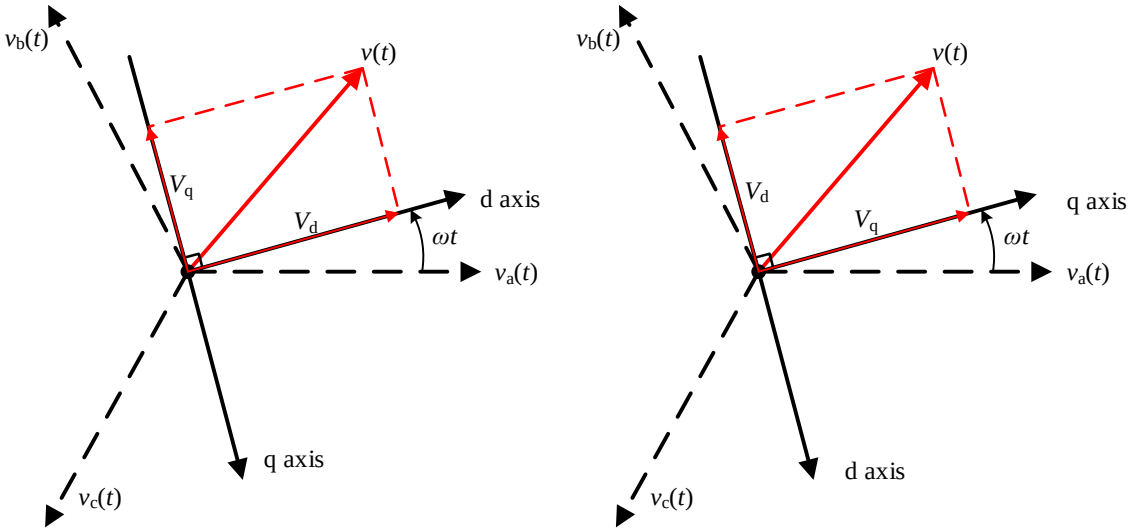

Fig. 4.1: Reference frames for ABC and DQ0 transformation.
(a) rotating frame with q axis leading d axis, (b) rotating frame with q axis lagging d axis.

By properly choosing the rotating frame of d and q axes, a decoupled controller can be designed with respect to the two constant components along the d and q axes. The equivalent system diagram of an AAC is shown in Fig. 4.2 in which the converter is represented as a voltage source connecting to the PCC via a transmission line (and the interface transformer) represented with an inductor and a resistor. The phase current is identified by the red arrow and flows out from the AAC to the ac system. The ac system is indicated as an equivalent voltage source.

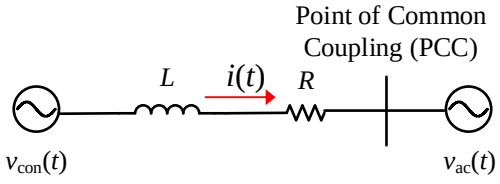

Fig. 4.2: Equivalent schematic of AAC system for decoupling control.

The state space equation for the AAC system is as follows.

$$v_{\text{con}}(t) = R \cdot i(t) + L\frac{di(t)}{dt} + v_{\text{ac}}(t) \tag{4.1}$$

where $v_{\text{con}}(t)$ is the converter output voltage and $v_{\text{ac}}(t)$ is the voltage of equivalent ac system. $i(t)$ is the current flowing out to ac system. L and R are the inductance and resistance of the equivalent transmission line and transformer (combined).

Since the standard reference frames in PSCAD/EMTDC and RTDS real-time simulation are different, the transformation matrices used for derivation would be different. In the following subsections, the decoupled control system will be derived with respect to both rotating frames.

4.1.1 Decoupled Control in PSCAD/EMTDC Simulation

In PSCAD/EMTDC simulation, the reference frame used for transformation from ABC to DQ0 is shown in Fig. 4.1(a). The corresponding transformation is described as follows.

$$\begin{bmatrix} v_{\text{d}} \\ v_{\text{q}} \\ v_{0} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v_{\text{a}}(t) \\ v_{\text{b}}(t) \\ v_{\text{c}}(t) \end{bmatrix} \tag{4.2}$$

Appling ABC to DQ0 transformation to the state space equation as (4.1), the d and q components are determined as follows.

$$\begin{aligned} v_{\text{cond}} &= \omega L i_{\text{q}} + R \cdot i_{\text{d}} + L\frac{di_{\text{d}}}{dt} + v_{\text{acd}} \\ v_{\text{conq}} &= -\omega L i_{\text{d}} + R \cdot i_{\text{q}} + L\frac{di_{\text{q}}}{dt} + v_{\text{acq}} \end{aligned} \tag{4.3}$$

where i_d and i_q are the dq components of converter output current and v_{cond} and v_{conq} are decomposed from AAC's output phase voltage. In addition, v_{acd} and v_{acq} are the dq components of equivalent voltage for ac system. The detailed derivation for (4.3) is shown in Appendix A.

Therefore, in the PSCAD/EMTDC simulation, the power order of the converter and terminal ac voltage are controlled in a decoupled manner by converter's modulation index and phase shift relative to the PCC as shown in Fig. 4.3. i_d controls the power order of AAC and i_q determines the PCC voltage.

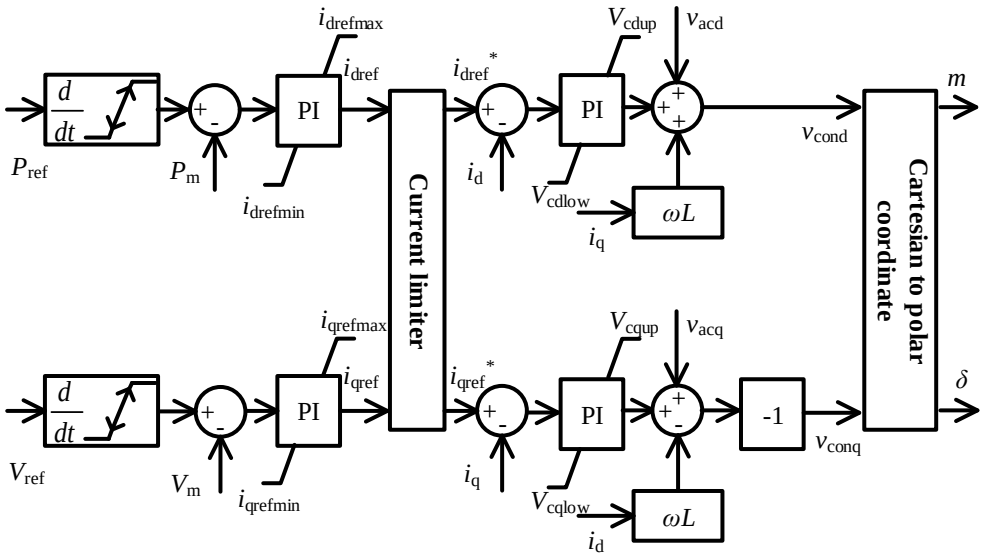

Fig. 4.3: Decoupled controller of AAC system in PSCAD/EMTDC simulation.

As illustrated in Fig. 4.3, the differences between measurements and reference values for power order and the PCC voltage are compared. PI controllers are implemented to eliminate the steady-state errors, which also provide current references as dq components for the inner-loop controllers. The current has a limiter as introduced in [53] where the i_{qref} would be maintained in order to keep the PCC voltage relatively constant. Thus, the i_{dref}

has a limiter determined by the corresponding maximum current magnitude and the i_{qref} component. In PSCAD/EMTDC simulation, the reference voltage is defined in cosine base as described below.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos(\omega t - \frac{2\pi}{3}) \\ V_m \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{4.4}$$

When the dq components of converter voltage are transferred back to modulation index and the phase shift between AAC's output phase voltage and the PCC voltage, the q component needs to be multiplied by -1 in order to generate the correct output response.

4.1.2 Decoupled Control in Real-time Simulation

In real-time simulation, the reference voltage is defined in a sine base. The reference frame used for transformation from ABC to DQ0 is shown in Fig. 4.1(b). The corresponding transformation is indicated below.

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{4.5}$$

From state space equation in (4.1), the d and q components (after using ABC to DQ0 transformation) are given below.

$$v_{\text{cond}} = -\omega L i_{\text{q}} + R \cdot i_{\text{d}} + L\frac{di_{\text{d}}}{dt} + v_{\text{acd}}$$

$$v_{\text{conq}} = \omega L i_{\text{d}} + R \cdot i_{\text{q}} + L\frac{di_{\text{q}}}{dt} + v_{\text{acq}} \tag{4.6}$$

where v_{cond} and v_{conq} are decomposed from AAC's output phase voltage and v_{acd} and v_{acq} are the dq components of equivalent voltage for ac system. The current flowing through the system can be decomposed as i_{d} and i_{q}. The detailed derivation for (4.6) is shown in Appendix A.

In real-time simulation, the decoupled controller is indicated in Fig. 4.4. Basically, the PCC voltage and power order are controlled by i_{d} and i_{q} current components, respectively. However, the resulting control is different compared to the controller in PSCAD/EMTDC simulation.

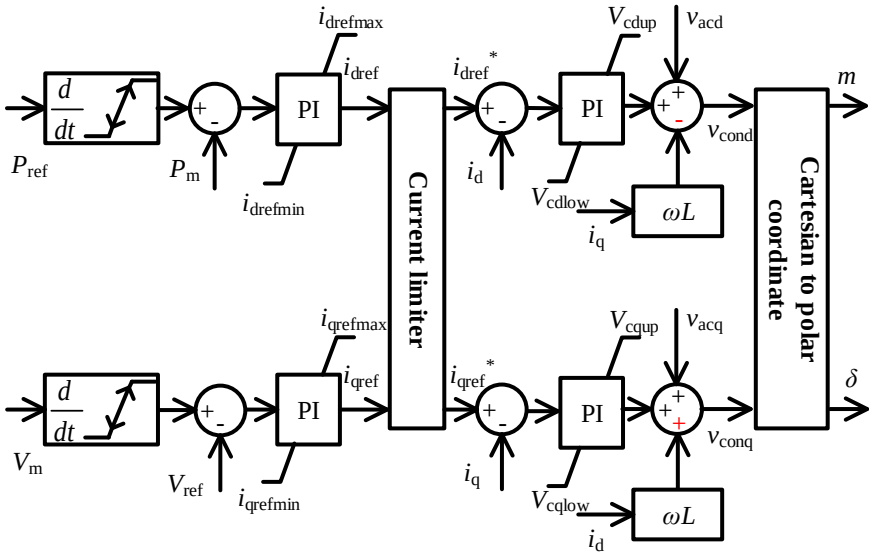

Fig. 4.4: Decoupled controller of AAC system in real-time simulation.

The decoupled controller is implemented based on (4.6) and the overall structure is similar to the PSCAD/EMTDC simulation. In terms of the PCC voltage, the error signal

has an opposite sign with reference to the controller in Fig. 4.3. To determine the expected values for dq components of AAC's output voltage, the decoupled terms have to be introduced to bias the controller properly by adding or subtracting i_d and i_q current components. In Fig. 4.4, the signs are shown in red indicating the differences compared to the PSCAD/EMTDC simulation. The real-time simulator defines voltages in a sine base as follows.

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} V_m \sin(\omega t) \\ V_m \sin(\omega t - \frac{2\pi}{3}) \\ V_m \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{4.7}$$

Therefore, modulation index and phase shift of AAC's output phase voltage with respect to the PCC voltage can be determined directly using dq components from the decoupled controller. By properly altering the decoupled controller, it can work as expected in real-time simulation.

4.2 Director Switches Control for AAC under Normal Operation

In order to have alternating arm operation of AAC, the director switches have to be controlled properly for different arms' conduction periods. In addition, the director switches need to take care of the OOC and ZCS method to balance the submodules energy and regulate capacitor voltages.

Overall, the operation for AAC arms can be divided into four periods in a complete conduction cycle. Firstly, the upper director switches turn on and lower director switches turn off, which result in the upper arm conduction period wherein the upper voltage stack creates a staircase output phase voltage. Secondly, the overlap period with both arms

conducting occurs, which is used for commutating the upper arm current to zero before switching that arm out from the conduction path. Thirdly, the director switch for the upper arm turns off; this starts the lower arm's conduction period, during which the output phase voltage is generated by the submodules of the lower voltage stack. Fourthly, both arm director switches turn on in order to alter states from lower to upper arm. By repeating this complete conduction period, the AAC can generate continuous output phase voltage and current during normal operation. The flowchart of director switches' logic is illustrated in Fig. 4.5.

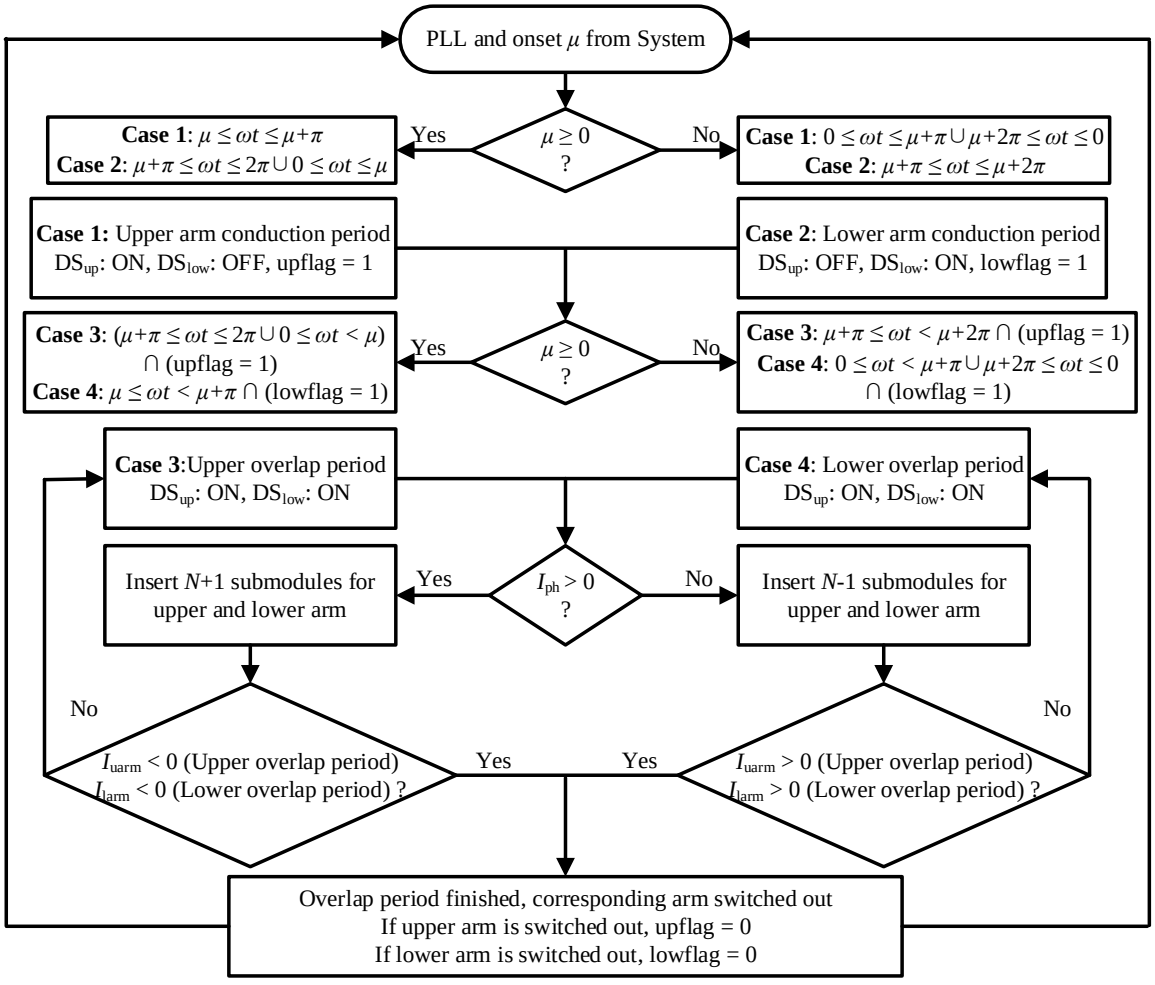

Fig. 4.5: Flowchart of director switches' control logic.

To determine the conduction period of director switches, a PLL signal locked onto the PCC is used instead of the instantaneous phase voltage. Assume an overlap onset angle of $\mu < 0$, for example; the corresponding conduction periods are indicated separately. From $\mu < \omega t < \mu+\pi$ of the PLL signal, the AAC is in the upper conduction period. The lower conduction period ranges from $\mu+\pi < \omega t < \mu+2\pi$ in which the submodules of the lower voltage stack generate the output phase voltage. The overlap period that commutates current from the upper to the lower arm starts at $\omega t \geq \mu+\pi$ and ends until the upper arm current crosses zero. As shown in Fig. 4.5, the director switches determine the end point based on the location of the overlap onset and the related arm current. For overlap period altering conduction from lower to upper arms, the overlap period begins when $\omega t \geq \mu+2\pi$ and finishes when the zero-crossing of arm current happens.

4.3 Single-Phase PLL

The director switches' logic operation relies on the PLL signal locked at the PCC. If the PLL signal has distortion, it may affect the normal operation of AAC. Consequently, the submodule capacitor voltages may not be able to balance properly due to undesired conduction periods. Generally, the PLL signal to the PCC is generated from a three-phase PLL. This control scheme can take care of normal operation with ease. However, when three-phase quantities are unbalanced, the PLL output may have either unequal periods or distortions. Therefore, a single-phase PLL is introduced in order to provide an output signal with less sensitivity to such abnormal operating modes.

A method introduced and analyzed in [52] known as an enhanced PLL (EPLL) is discussed in detail in this section. The EPLL method generates PLL signals with reduced

sensitivities to system distortions such as noise and harmonics. During unbalanced conditions, the EPLL has better adaptive frequency compared to normal PLL signal. In other words, the EPLL has a faster transient response and can track the frequency more accurately. With respect to EPLL method, the phase angle is estimated by using the block diagram shown in Fig. 4.6. Under unbalanced conditions, the positive sequence components of the PCC voltage are balanced without influence from system faults or disturbances. Therefore, the output phase angle is locked on to the positive sequence components of phase A. v_{afund}, $v_{bfund,}$ and v_{cfund} are fundamental-frequency components for three-phase PCC voltages. In addition, $v_{afund90}$, $v_{bfund90,}$ and $v_{cfund90}$ have 90-degree phase shifts compared to the fundamental components.

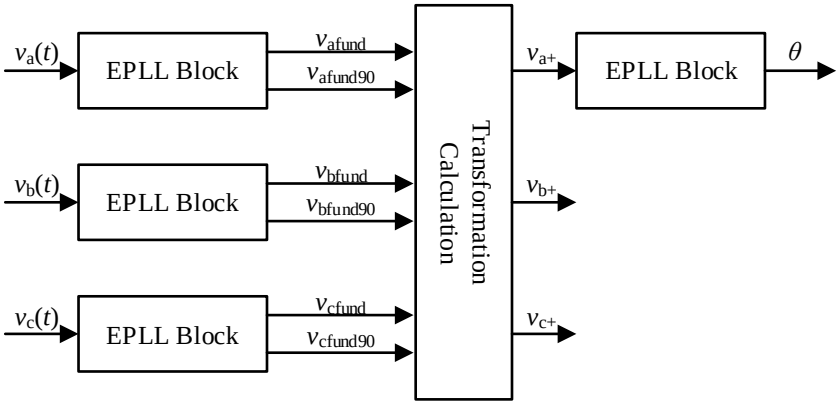

Fig. 4.6: Block diagram of the enhanced single phase-locked loop for AAC.

To calculate the positive sequence components of the three-phase quantities, the EPLL block is used for decomposition in terms of each phase's voltage. The EPLL block can output fundamental-frequency components and corresponding components with 90-degree phase shifts. In addition, the EPLL block can estimate the phase angle with respect to the positive sequence of the three-phase quantities. The relationship for transformations of positive sequence components is as follows.

$$\begin{bmatrix} v_{a+} \\ v_{b+} \\ v_{c+} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \tag{4.8}$$

$$\alpha = e^{j120^\circ} = -(\frac{1}{2}) \pm (\frac{\sqrt{3}}{2})e^{j90^\circ} \tag{4.9}$$

where v_{a+}, $v_{b+,}$ and v_{c+} are positive sequence components of the PCC voltage $v_a(t)$, $v_b(t)$, and $v_c(t)$ quantities, respectively. By substituting (4.9) in (4.8), the positive sequence components can be calculated as follows.

$$v_{a+} = \frac{1}{3}v_a(t) - \frac{1}{6}[v_b(t) + v_c(t)] - \frac{1}{2\sqrt{3}}S_{90}[v_b(t) - v_c(t)]$$

$$v_{b+} = \frac{1}{3}v_b(t) - \frac{1}{6}[v_a(t) + v_c(t)] - \frac{1}{2\sqrt{3}}S_{90}[v_c(t) - v_a(t)] = -v_{a+} - v_{c+} \tag{4.10}$$

$$v_{c+} = \frac{1}{3}v_c(t) - \frac{1}{6}[v_a(t) + v_b(t)] - \frac{1}{2\sqrt{3}}S_{90}[v_a(t) - v_b(t)]$$

where S_{90} is defined as 90-degree phase shift operator as in [54]. With reference to the EPLL block used in Fig. 4.6, a detailed structure is indicated in Fig. 4.7.

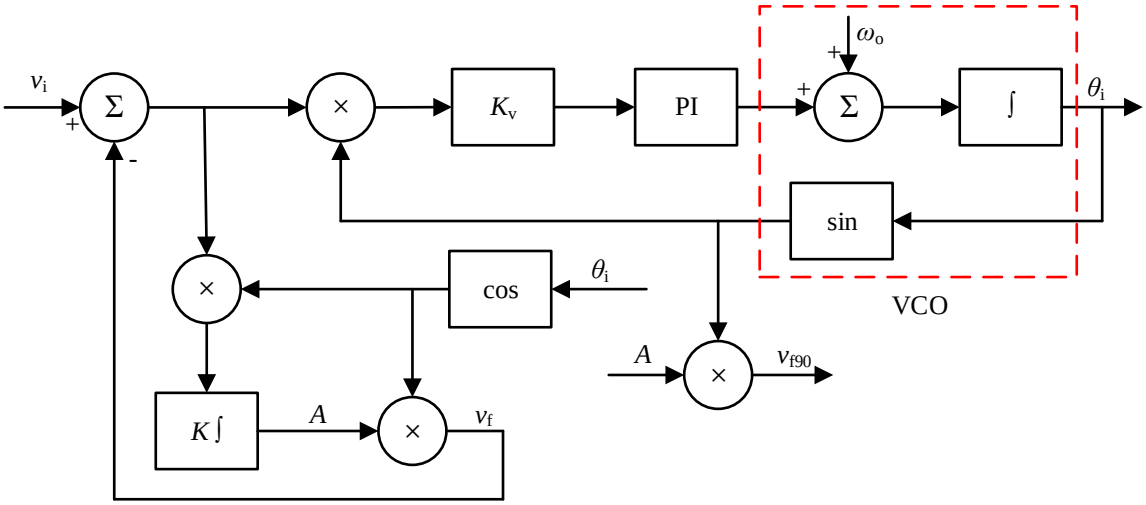

Fig. 4.7: Block diagram of EPLL method.

The EPLL block introduced in [55] has a similar structure to the conventional single-phase PLL. The phase angle estimation uses a voltage-controlled oscillator (VCO) to create a sawtooth waveform with respect to the fundamental frequency and error signal. The error signal is determined between the original and smooth signals for each phase quantities. The PI controller can eliminate the steady-state error in order to obtain better PLL output. Overall, the EPLL block can decompose phase quantities into the fundamental components and 90-degree phase shifted versions thereof. Furthermore, the VCO generates the output as PLL signal based on the error signal. Combining the EPLL block with transformation calculation block, the phase angle can be estimated fast and accurately on the positive sequence of phase-A voltage.

Chapter 5: System Implementation and Simulation Results

In this chapter, implementation of AAC system will be discussed in terms of system ratings and performance during dynamic and steady-state operation. The system parameters and setup will be introduced in Section 5.1. Section 5.2 will show the steady-state and transient responses of the AAC system concerning simulation case in PSCAD/EMTDC simulation. As for the real-time simulation results, Section 5.3 analyzes the performance regarding steady-state and dynamic behaviors.

In order to test the AAC system with OOC energy-balance control, different simulation cases are performed in terms of reference step changes and fault conditions. With respect to reference step change studies, the references for power order and the PCC voltage are changed starting from steady-state operation to evaluate the AAC system behavior. For the fault conditions, dc fault blocking and ac fault ride-through capabilities are tested to determine the dynamic responses of the AAC with OOC control method.

5.1: System Implementation and Ratings

A simulation model of AAC is implemented based on a system shown in Fig. 5.1. The AAC behaves as a dc to ac converter connecting the dc system to the ac system. The three-phase AAC with all director switches and cascaded FB submodules is developed based on the operation principles described in Chapter 3. Since director switches for each arm operate simultaneously, only one set of director switches is implemented for each arm to simplify the complexity of simulation case. The dc system is represented with a constant dc voltage of V_{dc} and connects to AAC through a dc filter. The AAC creates the output voltage by properly inserting FB submodules and turning director switches on and off. The

AAC delivers power to ac system via a transformer to generate the desired voltage at the PCC. For energy balancing of submodule capacitors, AAC is controlled by OOC method to modify the onset of the overlap period. The OOC method adjusts the overlap onset angle based on the predetermined value calculated from the (3.3) by using modulation index and the angular difference between AAC's output voltage and current. The feedback path of OOC controller modifies the overlap onset angle with a PI controller. The ZCS method executes turn off commands for director switches when the arm current detects zero-crossing. In addition, the MZCS method is incorporated with ZCS method to determine when overlap period ends in real-time simulation case. From the system's perspective, the power order of converter and terminal ac voltage are decoupled-controlled by converter's modulation index and phase shift relative to the PCC.

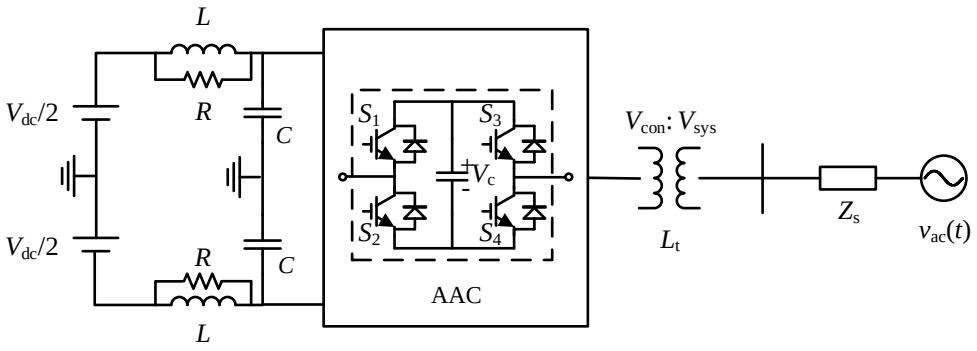

Fig. 5.1: Schematic diagram of the AAC system.

The AAC system model is developed with specifications listed in Table 5.1. The overall AAC system operates with a fundamental frequency of 60 Hz, the corresponding dc link and rated ac system voltages are 500 kV (±250 kV) and 230 kV, respectively. The AAC connects to ac system through a 700 MVA transformer with a turns ratio of 370/230 kV and leakage inductance of 0.1 pu. In addition, there are dc filters between dc link and AAC

with *R*, *L* and *C* values indicated in Table 5.1. For AAC's submodules, the rated voltage of each capacitor is 25 kV with a capacitance of 2 mF. With these ratings, the number of submodules should be $N = 10$ for each arm since the upper stack generates the positive portion and lower stack takes care of the negative cycle of the output voltage. However, additional submodules are needed to track the voltage reference during the overlap period. In this case, the total number of submodules for each arm of AAC is selected to be $N = 15$; that is, the stacks can track reference voltage $V_{dc}/4$ higher than half of dc link voltage ($V_{dc}/2$). In order to commutate arm currents smoothly from one arm to another, the arm inductor is chosen as 5 mH to oppose the current flow during the overlap period.

Table 5.1: System specifications

AC System Specifications		
Frequency = 60 Hz	Rated voltage = 230 kV	SCR = 4.0
Transformers Specifications		
370 (conv.)/230 (sys.) [kV]	Rated MVA = 700 MVA	Leakage reactance = 10%
Converter Specifications		
SM rated voltage = 25 kV	SMs per arm = 15	
SM capacitor = 2.0 mF	Arm inductor = 5 mH	
DC System Specifications		
Rated voltage = 500 kV	Filter: $R = 1.87\ \Omega$ Filter: $L = 3.52$ mH	Capacitor: $C = 2.0$ mF

In order to analyze AAC system responses regarding different studies, the control system including decoupled control and OOC method need to be tuned properly. For the decoupled controller, the inner current loop should react faster compared to the outer loop, which determines the current reference in the dq domain. With respect to studies of reference adjustment, the controller only needs to guarantee the measured signals can track

the references in a controlled manner. However, the decoupled controller needs to take care of the recovery from different fault situations as well. To successfully recover from the fault conditions, the arm and phase currents cannot have large overshoots that exceed the maximum current limit of 3.0 kA. Thus, the response of the decoupled controller should not produce sharp increment or decrement, which may lead to saturation of PI controllers.

The OOC method controls the overlap onset angle depend on the modulation index and angular difference between AAC's output voltage and current as shown in (3.3). Because the OOC controller consists of feedforward and feedback paths, the dynamic response can quickly track the reference based on the predetermined overlap onset angle. Therefore, the submodule capacitor voltages can be regulated to the nominal value in a short period. If the OOC method has a fast transient response, the system testing including reference step changes, dc fault blocking and ac balanced fault ride-through can operate as expected since the submodule capacitor voltages can be quickly restored to the steady-state or pre-fault value. However, the OOC method with fast response cannot recover from the ac unbalanced faults because the feedforward path reaches the maximum limit and the feedback path rapidly gains error that results in saturation of the OOC controller. Once the overlap onset angle saturates, the director switches will not turn on and off as expected, which leads to much slower response of submodule capacitor voltages. Furthermore, the energy imbalance of system may cause oscillation and trigger the blocking signal. Therefore, the OOC method should have a slower dynamic response to overcome all the system tests. With slower transient behavior, the AAC can still regulate submodule capacitor voltages to their desired value.

In Sections 5.2 and 5.3, the simulation results in term of PSCAD/EMTDC and RTDS real-time simulations will be discussed and analyzed in detail. The OOC method used in those two simulation models are tuned to have moderate transient response to react to all system tests. The controller gains for both PSCAD/EMTDC and RTDS simulation models are listed in the Table 5.2.

Table 5.2: Controller gains in PSCAD/EMTDC and RTDS real-time simulations

PSCAD/EMTDC Simulation Model				
PI Controller	OOC Controller	Decoupled Current Controller (Inner-loop)	Decoupled Voltage Controller (Outer-loop)	Decoupled Power Controller (Outer-loop)
Proportional gain (K_p)	5	1	2	3
Integration time (T_i) [s]	0.05	0.005	0.02	0.01
RTDS Real-time Simulation Model				
PI Controller	OOC Controller	Decoupled Current Controller (Inner-loop)	Decoupled Voltage Controller (Outer-loop)	Decoupled Power Controller (Outer-loop)
Proportional gain (K_p)	0.005	1	1	2
Integration time (T_i) [s]	5	0.005	0.05	0.02

5.2 PSCAD/EMTDC Simulation Studies

5.2.1 Voltage Step Change

A step change to the reference terminal ac voltage (PCC voltage) is applied to analyze that the response of the system. Simulation results of AAC system in PSCAD/EMTDC case are shown in Fig. 5.2 and Fig. 5.3.

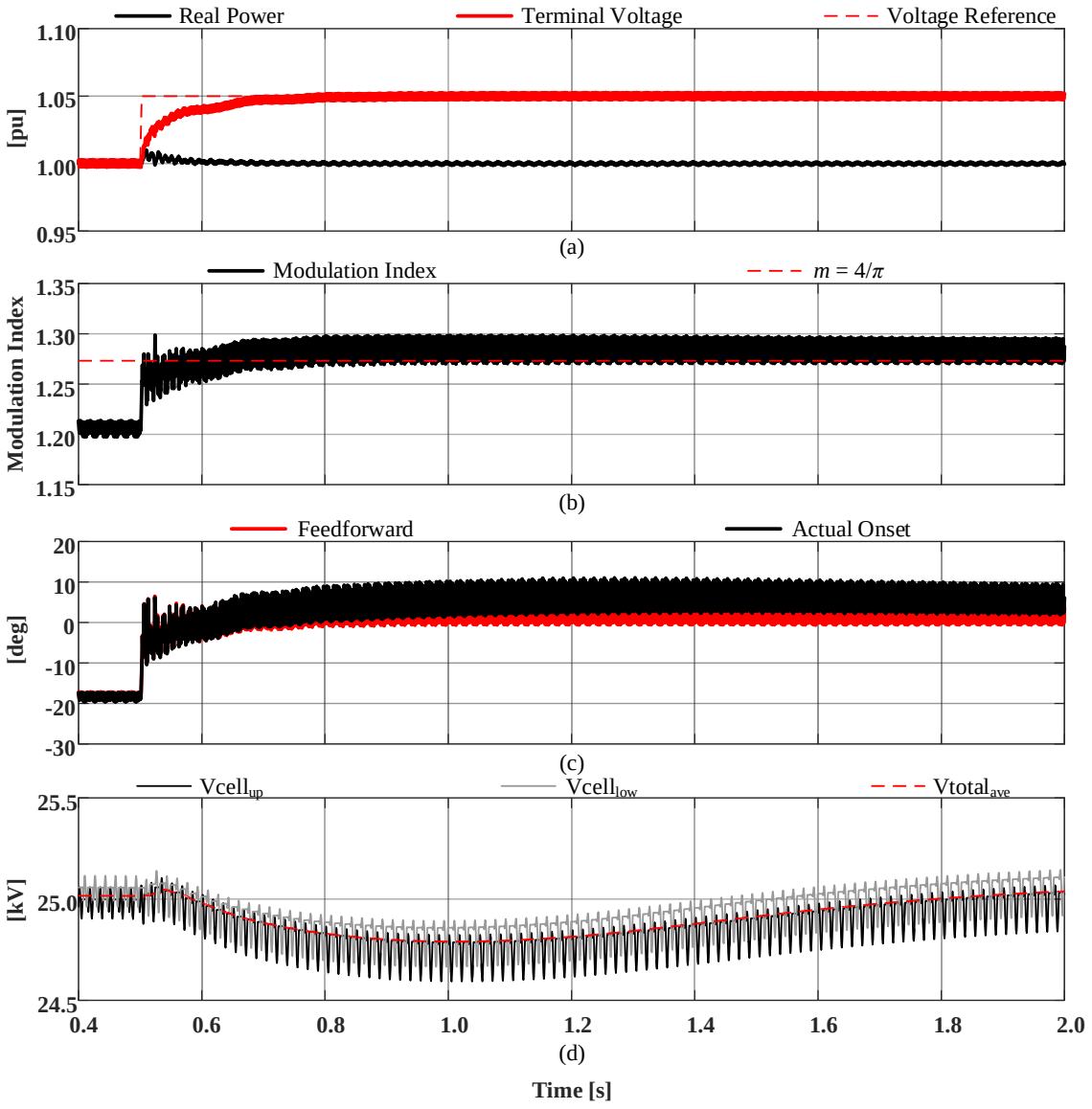

Fig. 5.2: System responses with reference terminal voltage changes from 1.0 to 1.05 pu. PSCAD/EMTDC simulation with step change in reference terminal (PCC) voltage from 1.0 to 1.05 pu at t = 0.5 s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

The step change response for different reference terminal voltages is simulated in the PSCAD/EMTDC simulation with system specifications described in Table 5.1. In Fig. 5.2(a), the reference terminal voltage increases from 1.0 to 1.05 pu at time t = 0.5 s. As shown in Fig. 5.2(b) and (c), the magnitude of overlap onset angle is reduced as modulation

index increases from approximately 1.2 to 1.29. Since the modulation index of AAC increases to a value higher than the "sweet spot" as indicated by red dashed line in Fig. 5.2(b), the energy supplied by dc system is smaller compared to the energy delivered to ac system. The energy imbalance between dc and ac sides leads to a voltage drop of submodule capacitor voltages as shown in Fig. 5.2(d). The overlap onset angle is controlled by the OOC method in order to increase the net energy for FB submodules. In Fig. 5.2(c), OOC controller updates the calculated μ and slightly adjusts the actual μ regarding the difference between rated and measured submodule capacitor voltages. Consequently, the submodule capacitor voltages in Fig. 5.2(d) increase and return to the nominal value.

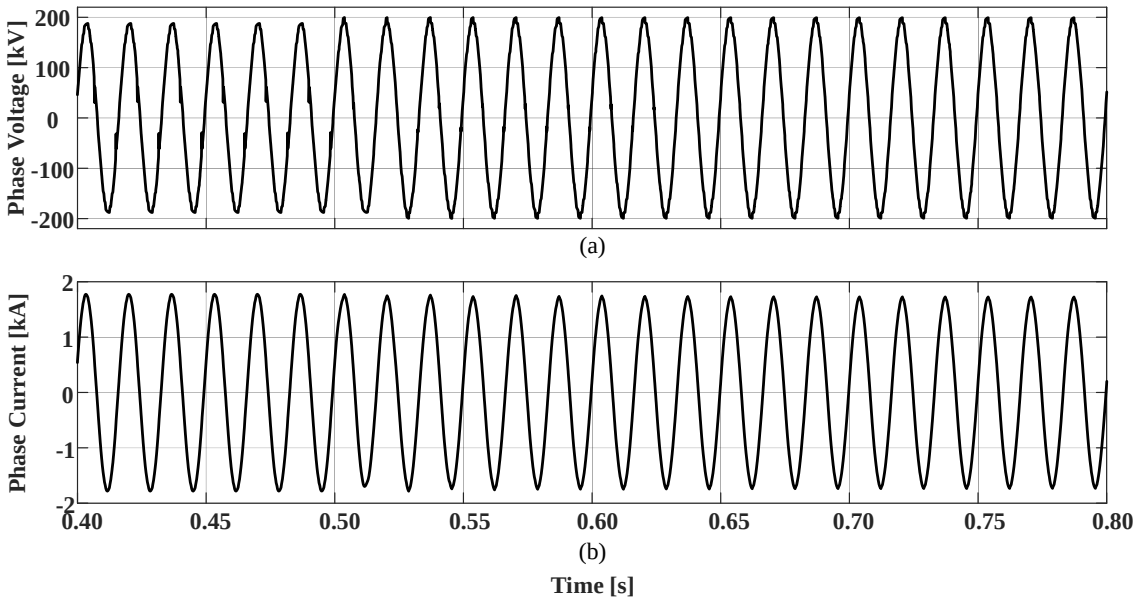

Fig. 5.3: Phase voltage and current with reference terminal voltage changes from 1.0 to 1.05 pu. PSCAD/EMTDC simulation with step change in reference terminal (PCC) voltage from 1.0 to 1.05 pu at t = 0.5 s. (a) PCC voltage of phase A, (b) PCC current of phase A.

In Fig. 5.3, a zoomed version of phase voltage and current are captured from t = 0.4 to 0.8 s. The phase voltage and current for the PCC are illustrated in Fig. 5.3 (a) and (b), respectively. The magnitude of phase voltage increases at time t = 0.5 s due to the reference

terminal voltage changes from 1.0 to 1.05 pu. Since the power order remains unchanged, the corresponding amplitude of phase current decreases slightly.

5.2.2 Power Step Change

This case changes the power order reference of AAC with the purpose of analyzing the response of the system. In the following figures (Fig. 5.4 and Fig. 5.5) steady-state and transient system responses are indicated for the simulation model in PSCAD/EMTDC.

In Fig. 5.4, the PSCAD/EMTDC simulation results are generated based on reference adjustment of power order from 0.8 to 1.0 pu at time t = 0.5 s. As shown in Fig. 5.4(a), the reference terminal voltage remains constant while power order increases at time t = 0.5 s. The measured terminal voltage at the PCC has a small overshoot and then settles into steady-state quickly. Since the reference terminal voltage is maintained at 1.0 pu, the corresponding modulation index stays approximately the same during the step change of power order as shown in Fig. 5.4(b). When the power order reference is increased to 1.0 pu, the energy supplied by dc system increases and becomes higher than the energy delivered to ac system, which results in net energy imbalance of submodules. Consequently, the increased net energy of submodule capacitors leads to a increase of voltages for both upper and lower arms as in Fig. 5.4(d). In Fig. 5.4(c), the OOC slightly reduces the magnitude of overlap onset angle to balance and restore submodule capacitor voltages back to their nominal value. As shown in Fig. 5.5, the waveforms of phase voltage and current are indicated within a time window from t = 0.4 to 0.8 s. The output voltage and current measured at the PCC for phase A are shown in Fig. 5.5 (a) and (b), respectively. Due to the same reference terminal voltage, the magnitude of measured output voltage for phase A is nearly constant while

power order changes from 0.8 to 1.0 pu. Thus, the corresponding magnitude of phase current increases to provide more real power to the ac system.

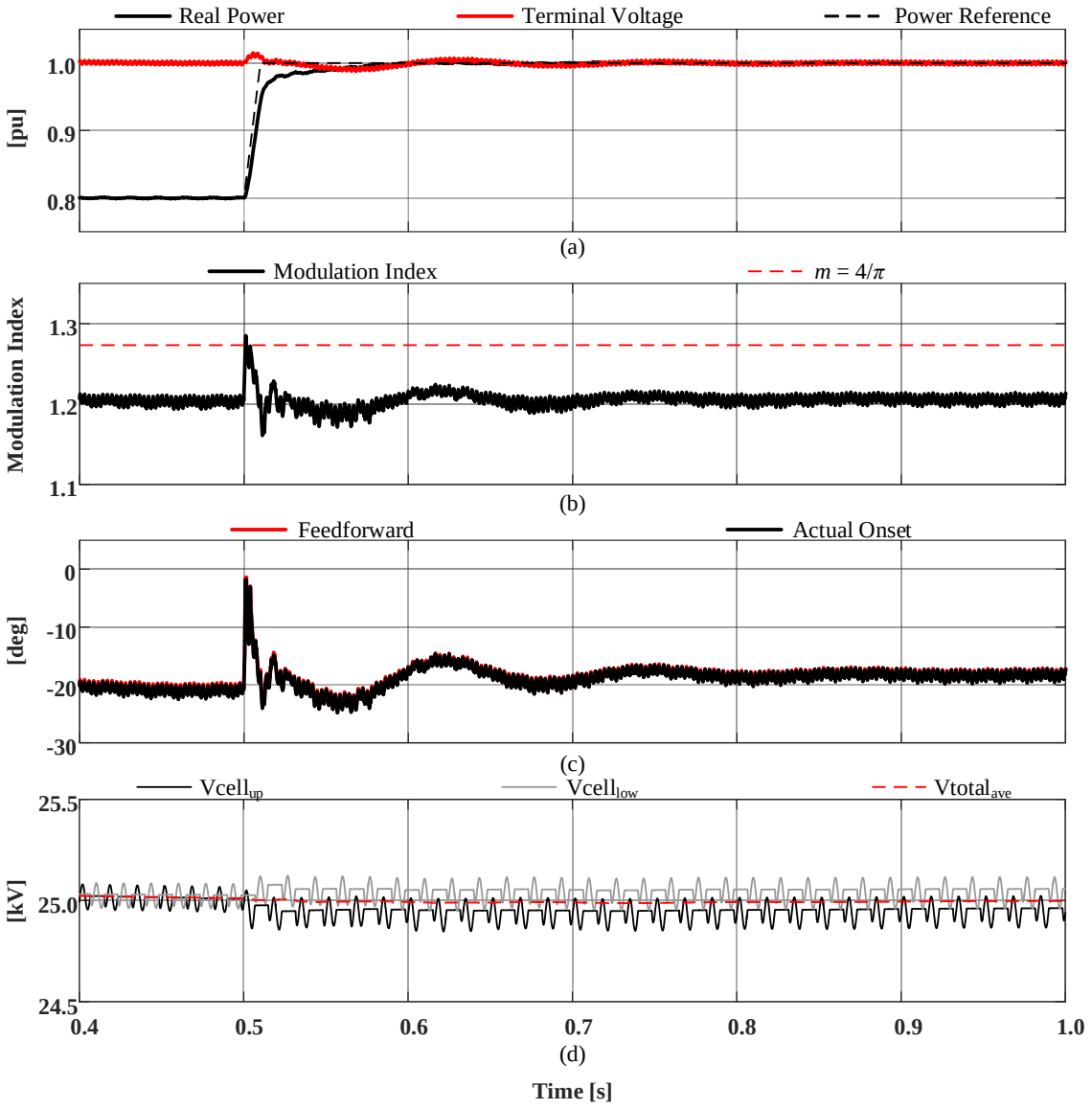

Fig. 5.4: System responses with power order changes from 0.8 to 1.0 pu.
PSCAD/EMTDC simulation with step change in power order reference from 0.8 to 1.0 pu at t = 0.5 s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

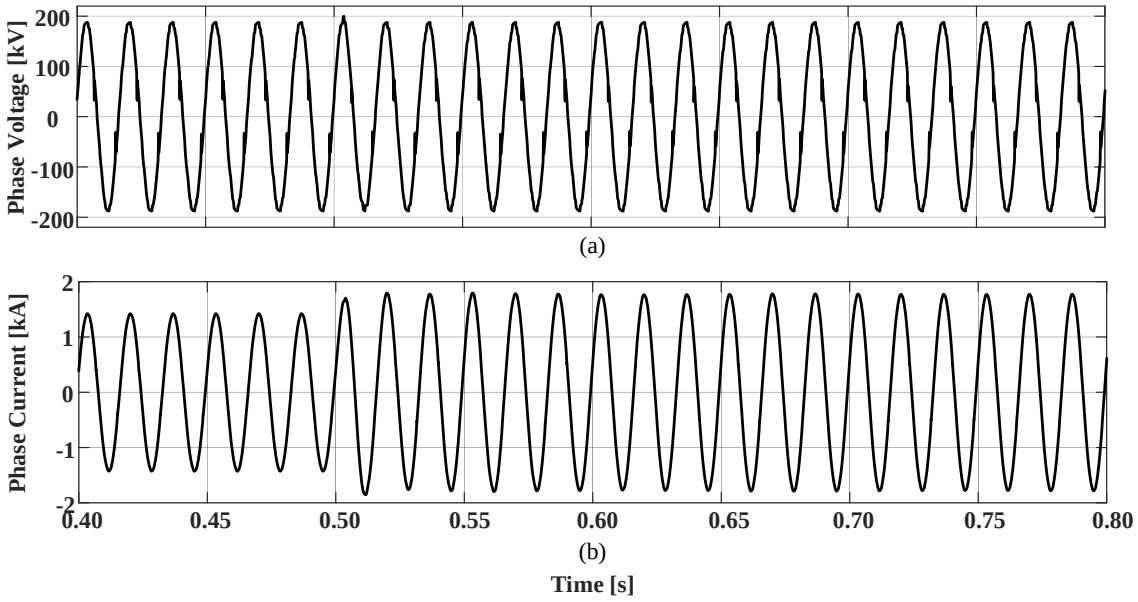

Fig. 5.5: Phase voltage and current with power order changes from 0.8 to 1.0 pu.
PSCAD/EMTDC simulation with step change in power order reference from 0.8 to 1.0 pu at t = 0.5 s. (a) PCC voltage of phase A, (b) PCC current of phase A.

5.2.3 DC Fault Blocking Capability

The AAC has a prominent feature that the FB submodules of each arm can block dc fault and oppose current flowing from ac to dc side during fault conditions. Its pole-to-pole dc fault blocking capability is tested in PSCAD/EMTDC simulation as shown in Fig. 5.6 and Fig. 5.7. In the following two figures, the results indicate system behaviors regarding operation before, during, and after the fault.

In Fig. 5.6, a pole-to-pole dc fault is applied to the AAC system at time t = 0.5 s with a duration of 150 ms. When the fault is applied to the system, the fault detector will detect any arm currents that exceed the maximum threshold of 3.0 kA. As shown in Fig. 5.6, the dc fault is detected at t = 0.502 s with an arm current higher than 3.0 kA. Once the dc fault is detected, all submodules are blocked and director switches are turned off. During the dc fault, the current starts to flow from ac to the faulted dc system. By blocking all FB

submodules, the current charges up the submodule capacitors which can further oppose the current flow and isolate dc and ac systems. After a 5-ms delay at t = 0.507 s, the power order reference is decreased to zero gradually as shown in Fig. 5.6(a). As shown in Fig. 5.6(d), the submodule capacitor voltages are maintained at the pre-fault value since all submodules are blocked. Thus, the overlap onset angle keeps constant during the fault condition. When the dc fault is cleared at t = 0.65 s, the block signal holds for an additional 50 ms to avoid any possible current overshoot that may retrigger the blocking signal. Also, the power order is ramped up to 1.0 pu at t = 0.707 s to recover back to steady-state operation. The system responses of phase voltage and current for the pole-to-pole dc fault are shown in Fig. 5.7. In Fig. 5.7 (a) and (b), the output phase voltage and current at the PCC are plotted within a time window from t = 0.4 to 1.0 s. For the phase voltage, the spike on the waveform indicates the beginning of dc fault. The magnitude of the spike on the output voltage waveform depends on the point-on-wave behaviors, i.e. the time when dc fault is applied to the system. As soon as the dc fault occurs, the phase current decreases to zero immediately as indicated in Fig. 5.7(b).

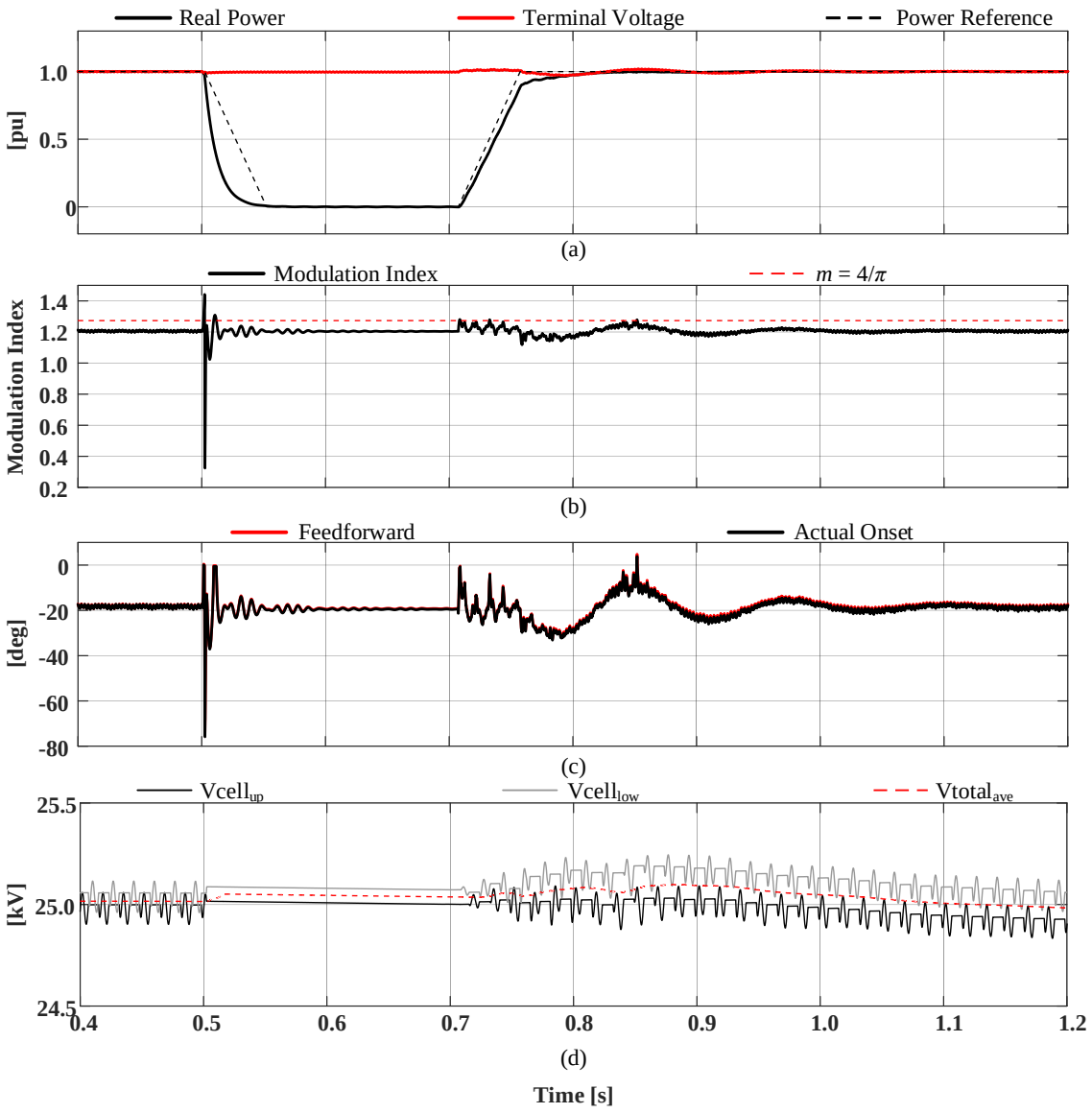

Fig. 5.6: System responses with pole-to-pole dc fault.
PSCAD/EMTDC simulation with pole-to-pole dc fault at t = 0.5 s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

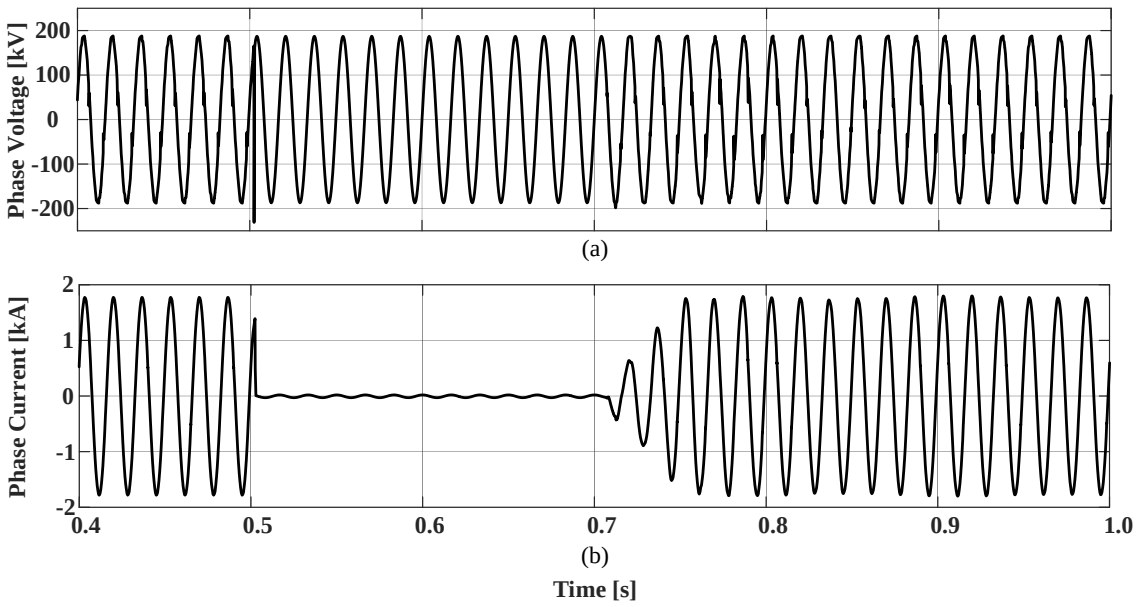

Fig. 5.7: Phase voltage and current with pole-to-pole dc fault.
PSCAD/EMTDC simulation with pole-to-pole dc fault at t = 0.5 s. (a) PCC voltage of phase A, (b) PCC current of phase A.

5.2.4 AC Three-Phase-to-Ground Fault Ride-through

The AAC system is tested regarding the ride-through ability for ac three-phase-to-ground fault in PSCAD/EMTDC simulation as shown in Fig. 5.8 and Fig. 5.9. The AAC system's behaviors before, during, and after the fault are plotted in the following two figures.

The dynamic responses are shown in Fig. 5.8 when AAC system rides through an ac three-phase-to-ground fault at time t = 1.5 s with a duration of 150 ms. When the three-phase ac fault happens, the magnitude of currents start to increase and the AAC's output voltage reduces to zero as shown in Fig. 5.8(a). Also, the corresponding measured power of AAC system decreases to zero in Fig. 5.8(a). In Fig. 5.8(b), the related modulation index decreases from 1.2 to 0 (theoretically) due to the decrement of output phase voltage. The OOC method determines the overlap onset angle regarding modulation index during the

fault condition as indicated in Fig. 5.8(c). Since the power delivered to the faulted ac system is nearly zero, the power supplied by the dc system charges up submodule capacitor voltages as indicated in Fig. 5.8(d). Moreover, the output phase voltage and power order are close to zero, which makes the OOC method difficult to balance the capacitor voltage during the fault condition. The fault is cleared after a duration of 150 ms at t = 1.65 s. The AAC system starts to recover to the normal operation. In Fig. 5.8 (a) and (b), the measured voltage, power order and corresponding modulation index remain at the pre-fault values. The OOC modifies the overlap onset angle so that the submodule capacitor voltages can regulate to the nominal value as illustrated in Fig. 5.8(d). As for Fig. 5.9, it indicates the system response of phase voltage and current during the three-phase ac fault. When the ac fault occurs, the phase voltage at the PCC decreases to zero immediately as shown in Fig. 5.9(a). In order to ride-through the ac three-phase-to-ground fault, the phase current is maintained within the maximum current limit of 3.0 kA in Fig. 5.9(b).

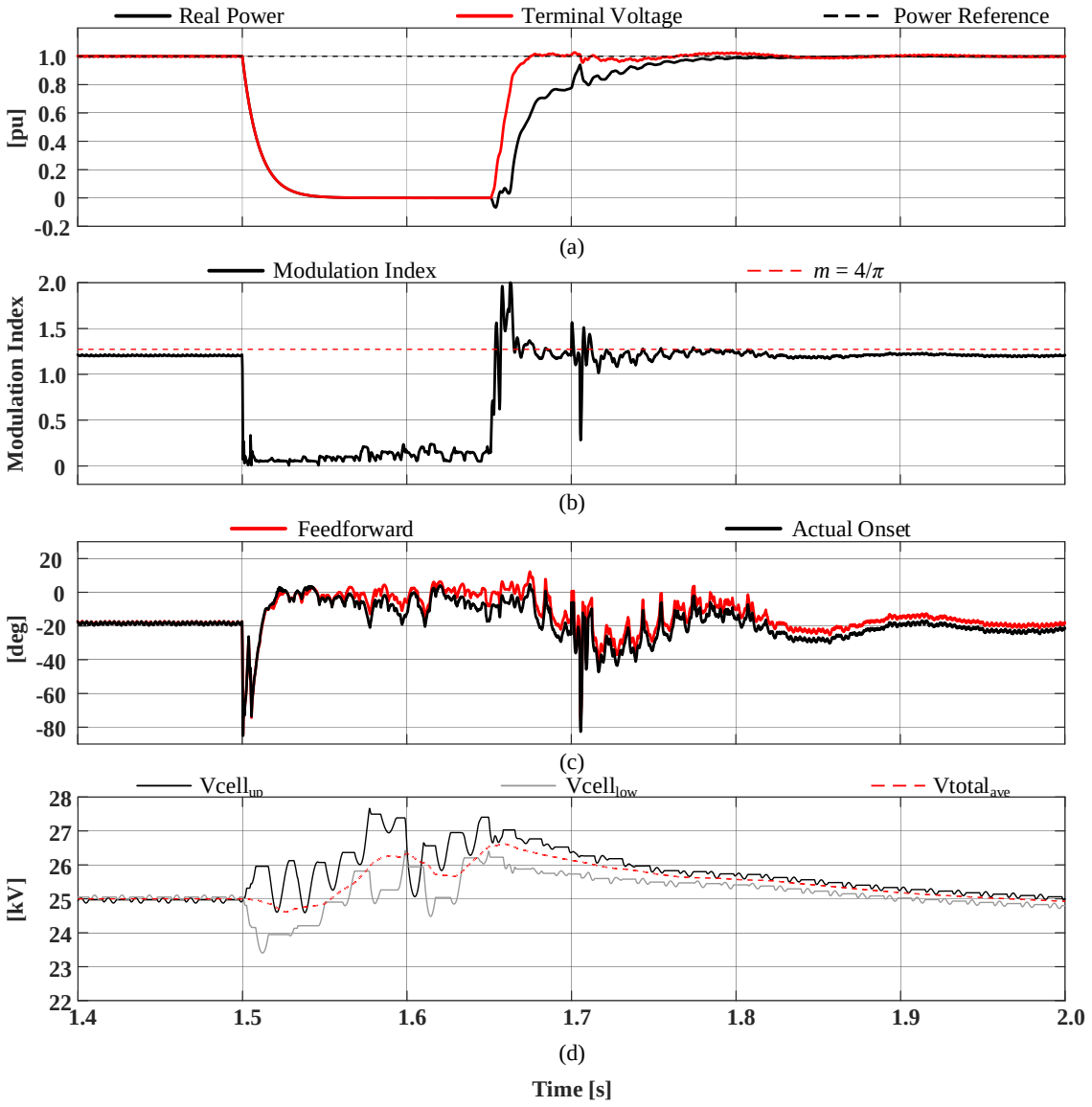

Fig. 5.8: System responses with ac three-phase-to-ground fault.
PSCAD/EMTDC simulation with ac three-phase-to-ground fault at t = 1.5 s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

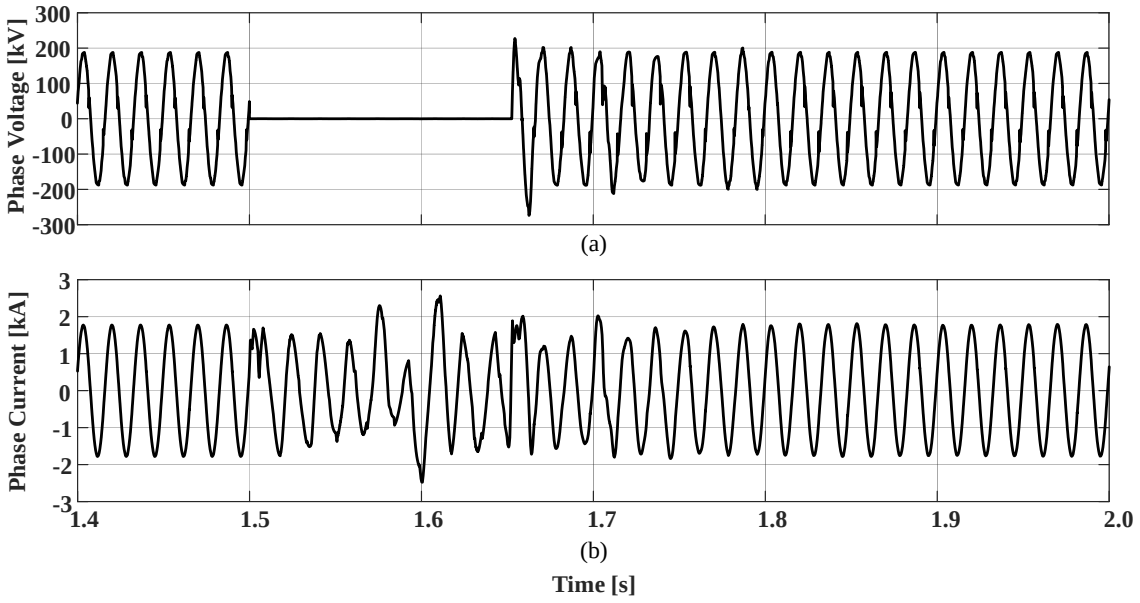

Fig. 5.9: Phase voltage and current with ac three-phase-to-ground fault.
PSCAD/EMTDC simulation with ac three-phase-to-ground fault at t = 1.5 s. (a) PCC voltage of phase A, (b) PCC current of phase A.

5.2.5 AC Remote Fault Ride-through

To demonstrate ac remote fault ride-through capability, the dynamic responses of AAC system in PSCAD/EMTDC simulation are plotted in Fig. 5.10 and Fig. 5.11. In order to analyze the system performances, the operations before, during, and after the fault are captured in the following figures.

In Fig. 5.10, the system behaviors are shown when ac remote fault is applied at time t = 0.5 s with a duration of 150 ms. In order to simulate ac remote faults, it is emulated using a 10% reduction in voltage magnitude and a 5° phase shift. When the ac remote fault occurs, the measured output voltage at the PCC decreases as indicated by Fig. 5.10(a) and the corresponding modulation index reduces to about 1.1 immediately as shown in Fig. 5.10(b). In Fig. 5.10(c), the magnitude of overlap onset angle varies from -20 to -10 degrees by adjustment of OOC method, resulting in balanced capacitor voltages. After the fault is

cleared at t = 0.65s, the measured output voltage restores to 1.0 pu while the power order remains at 1.0 pu. As illustrated in Fig. 5.10(d), the OOC modifies the overlap onset angle back to its pre-fault value of -20 degree and the system successfully rides through the ac remote fault.

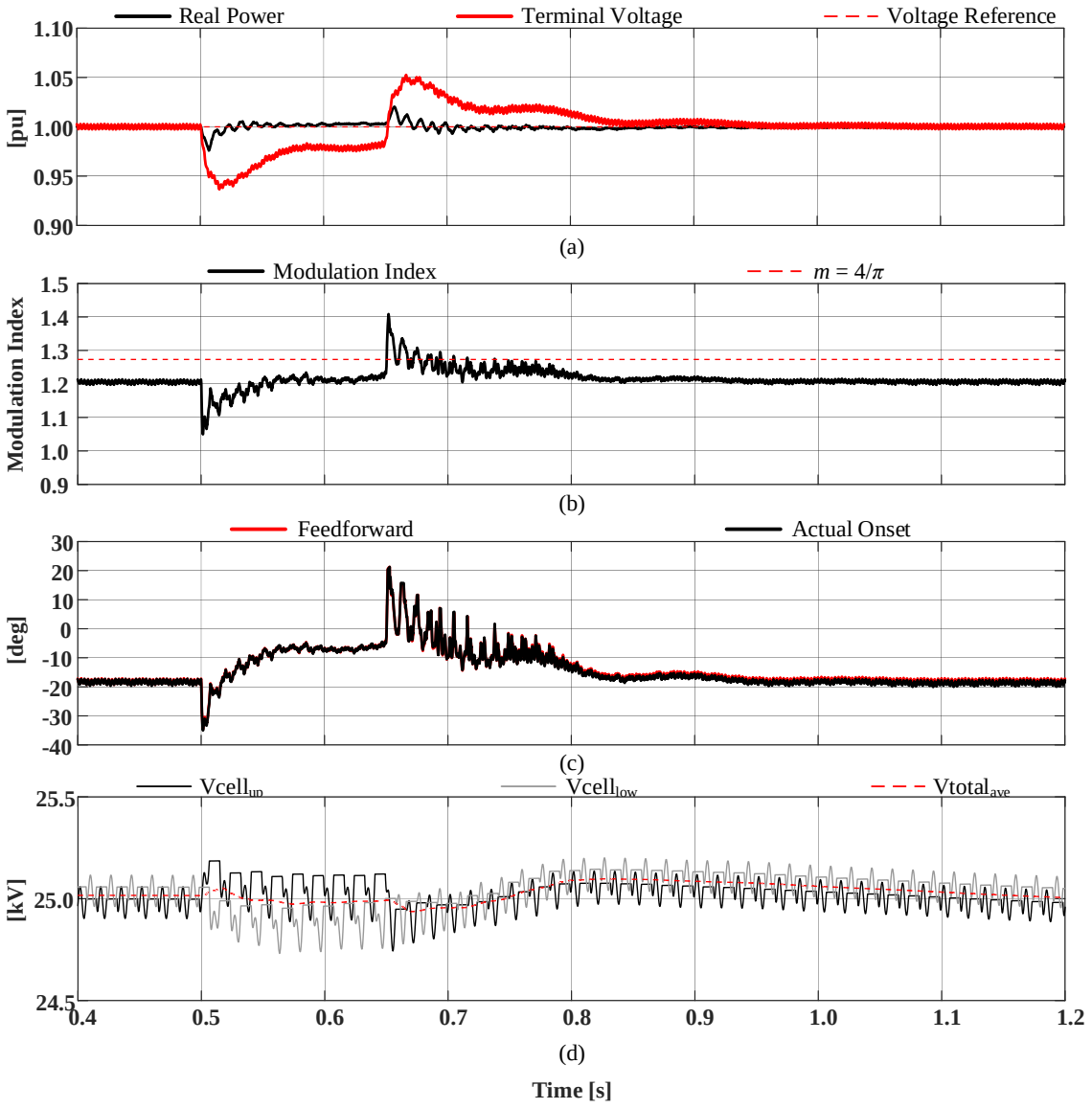

Fig. 5.10: System responses with ac remote fault.
PSCAD/EMTDC simulation with ac remote fault at t = 0.5 s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

The system behaviors for ac remote fault concerning phase voltage and current with a zoomed plot from t = 0.4 to 1.0 s are displayed in Fig. 5.11. The phase voltage of the PCC slightly decreases when the ac remote fault happens as shown in Fig. 5.11(a). Since the power order remains at 1.0 pu during the fault, the magnitude of the phase current increases as plotted in Fig. 5.11(b). The OOC controller can quickly react to ac remote fault by adjusting the overlap onset angle in order to balance the energy difference.

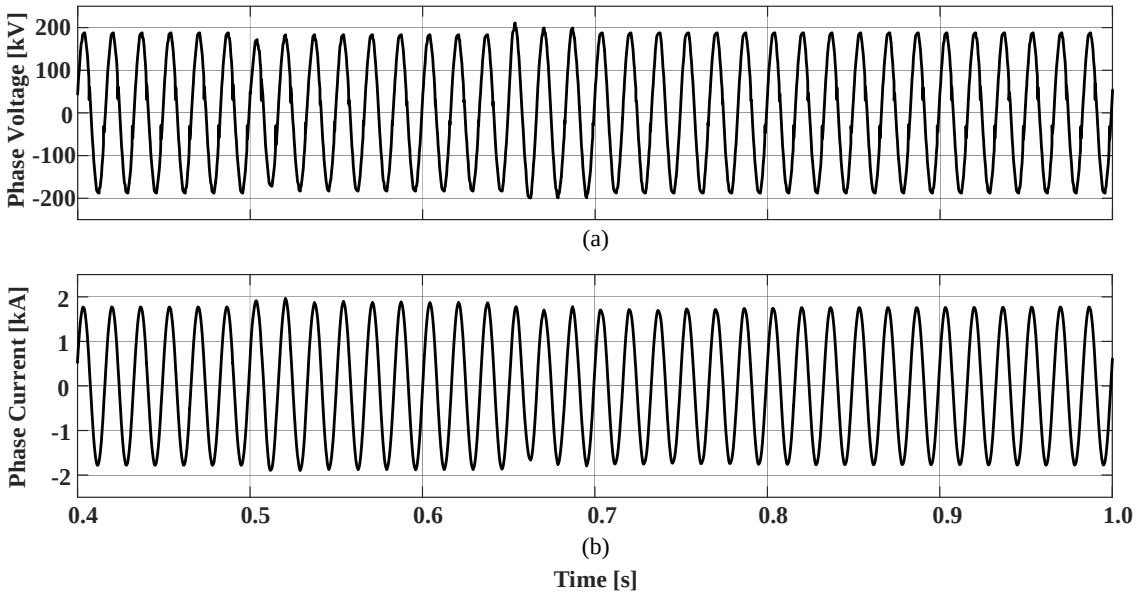

Fig. 5.11: Phase voltage and current with ac remote fault.
PSCAD/EMTDC simulation with ac remote fault at t = 0.5 s. (a) PCC voltage of phase A, (b) PCC current of phase A.

5.2.6 AC Single-Phase-to-Ground Fault Ride-through

An unbalanced single-phase-to-ground fault at the PCC is implemented in PSCAD/EMTDC simulation. The system responses in terms of pre-fault, during-fault and after-fault conditions are illustrated in Fig. 5.12 and Fig. 5.13.

In Fig. 5.12, the ac single-phase-to-ground fault is applied to phase A of AAC system at time t = 0.5 s with a fault duration of 150 ms. Once the unbalanced ac fault occurs, the

phase current of the faulted arm increases immediately. To avoid reaching the maximum current limit, the resulted terminal voltage decreases to approximately 0.75 pu (as a result of controller action) as indicated in Fig. 5.12(a). The power order reduces to about -0.5 pu, which means that the AAC starts to draw power from the unbalanced fault. The corresponding average value of modulation index decreases as the magnitude of phase voltage reduces. As shown in Fig. 5.12(b), the oscillation has a frequency which is twice as the fundamental frequency during the unbalanced fault of phase A. The unbalanced fault is applied to phase A, which is the same phase as illustrated in the simulation results. In Fig. 5.12(d), the submodule capacitor voltages decrease dramatically before the fault is detected. Then the OOC adjusts overlap onset angle based on the modulation index to maintain submodule capacitor voltages at approximately 25 kV during the unbalanced fault condition as shown in Fig. 5.12(c). The unbalanced fault is cleared at t = 0.65 s after a duration of 150 ms. The AAC system starts to recover from the fault and settles to the normal operation. The measured phase voltage, real power and corresponding modulation index return to the pre-fault values with fast transient responses indicated in Fig. 5.12 (a) and (b). The submodule capacitor voltages can be regulated to the desired value by restoring the pre-fault value for the overlap onset angle as illustrated in Fig. 5.12(d). The system responses of phase voltage and current with a zoomed plot from t = 0.4 to 1.0 s are shown in Fig. 5.13. When the ac single-phase-to-ground fault occurs, the terminal phase voltage decreases to zero immediately as shown in Fig. 5.13(a). Since the unbalanced fault is applied to phase A, the corresponding simulation result of phase current at converter side is indicated in Fig. 5.13(b). During the unbalanced fault condition, the maximum current limit of the decoupled controller is reduced to a lower value in order to keep the magnitude

of phase current below 3.0 kA. In Fig. 5.13(b), the magnitude of phase current has a small overshoot due to the transient response of system performance when the fault is detected.

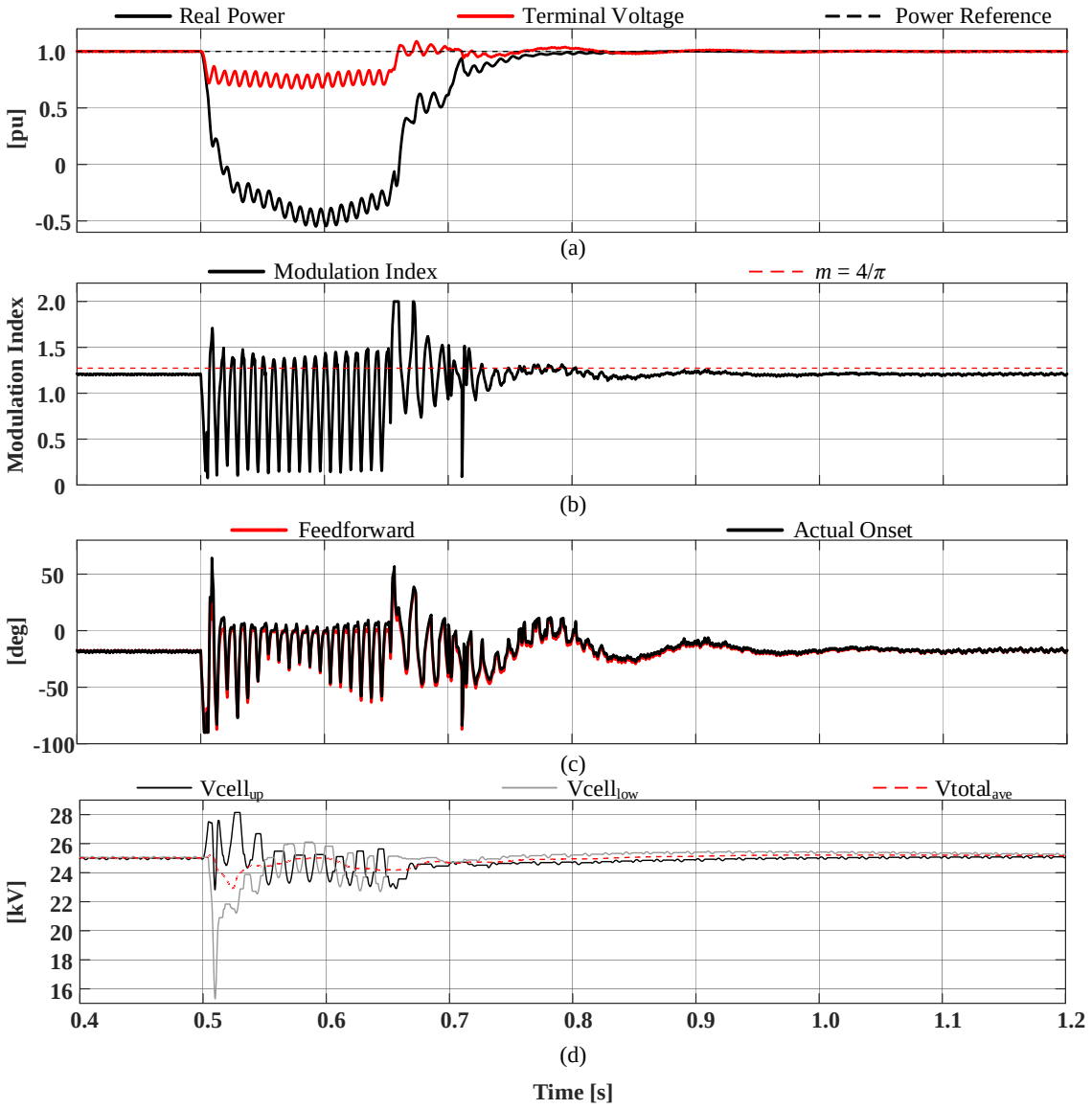

Fig. 5.12: System responses with ac single-phase-to-ground fault.
PSCAD/EMTDC simulation with ac single-phase-to-ground fault at $t = 0.5$ s. (a) real power and RMS terminal voltage, (b) modulation index and the "sweet spot", (c) calculated μ and actual μ, (d) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors.

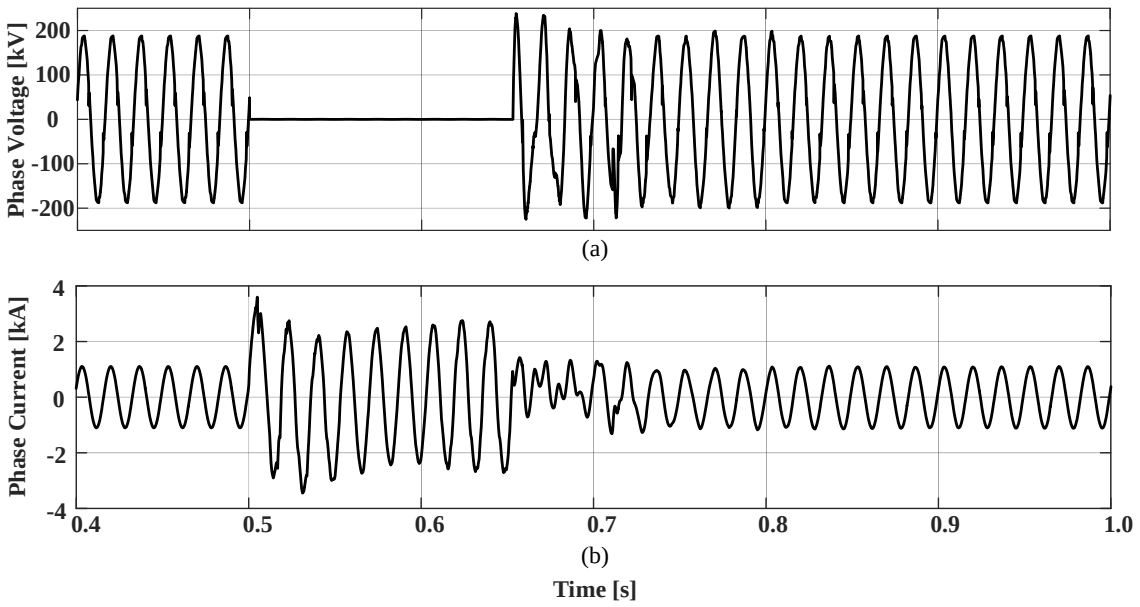

Fig. 5.13: Phase voltage and current with ac single-phase-to-ground fault.
PSCAD/EMTDC simulation with ac single-phase-to-ground fault at t = 0.5 s. (a) PCC voltage of phase A, (b) converter side current of phase A.

5.3 Real-time Simulation Studies

The AAC model in PSCAD/EMTDC simulation can be used to analyze the detailed operation of OOC and ZCS methods. However, there are some limitations for directly transferring the AAC model into the real-time simulation. In real-world applications, control signals and measurements are not always sampled and updated at a sampling rate of 1 MHz (as was done in PSCAD/EMTDC simulations). The processor may not be able to finish processing all the calculations and control algorithms within a 1 μs time-step. Regarding control signals and measurements, the AAC with OOC method has to operate based on the instantaneous signals instead of interpolated signals, especially for voltage and current measurements. By applying the OOC method, the overlap period needs to have flexible onset and duration to be able to regulate submodule capacitor voltages. Thus, the ZCS method becomes more important in a large time-step system to guarantee the desired

turn-off commands for the director switches. Based on the ZCS method, the overlap period will finish as soon as the arm current goes across zero, which means that the actual gate pulse of director switches always has one time-step delay compared to the zero-crossing flag. For a 1-μs time-step delay, the arm current would not change dramatically to produce a large reverse current through the reverse-conducting diodes of director switches. However, if the time delay becomes 50 μs (as is the case with the deployed real-time simulator) instead of 1 μs, the arm current would have an extended period with undesired current magnitude. If the overlap period extends to longer durations, the conduction losses of both arms will increase. In addition, if the arm is switched out with non-zero arm current, the switching losses would also increase. Therefore, it is necessary to produce a real-time model in order to analyze the OOC control in a more realistic way.

Real-time simulation in RTDS allows modeling the system with both small time-step and large time-step operations. If the AAC system can be implemented in the real-time simulation with a small time-step, it would be similar to the PSCAD/EMTDC model. However, there are some limitations for small time-step implementation. The amount of monitored input and output signals are limited, which means it is hard to implement all the measurements and control signals for the three-phase AAC in the small time-step simulation. Also, if all calculations and control algorithms are built based on small time-step operation, the processor with a clock rate of 1.7 GHz is not be able to finish within the maximum allowable time-step of 3.75 μs. Therefore, it is important to implement and analyze AAC system that consists of OOC and ZCS methods in a large time-step manner.

In the real-time simulation case, power electronic components including the director switches and cascaded FB submodules for three-phase AAC are implemented with small

time-step models. However, all the calculations and control algorithms need to be developed in the large time-step system, which means that signals are sampled and updated every 50 μs. In order to complete the real-time simulation model using RTDS, some additional modifications need to be considered and implemented.

Since AAC system is implemented in small time-steps and control algorithms are implemented in large time-steps, additional components are required to connect and communicate between the two parts of simulations. The simulations with small and large time-steps are connected by a component of the interface transmission line model. The interface component is developed based on the Bergeron traveling wave transmission line model with some built-in inductances. To implement the AAC with the same system specifications as in PSCAD/EMTDC model, the arm inductances for both the upper and lower arms and transformer leakage inductance need modifications by subtracting the built-in inductances from the original values.

The overlap period finishes depending on the zero-crossing of the arm current. In fact, the actual gate pulse of director switches would go high after detecting the zero-crossing flag. With an additional 50 μs time-delay, the arm current will commutate into the reverse direction. When the overlap period ends, non-zero current will increase the switching losses of director switches. Also, the corresponding arm switched out from the conduction path would have current flowing through the reverse-conducting diodes of director switches. Despite the director switches of outgoing arm turning off, the current is still flowing, and the FB submodules are still conducting. Therefore, the MZCS method described in Section 3.3 is implemented in real-time simulation in order to minimize the possible increment of switching and conduction losses.

In the following subsections, real-time simulation in RTDS uses the same system parameters as PSCAD/EMTDC model. The steady-state and dynamic responses of AAC with OOC method are evaluated based on system tests including reference adjustment, dc fault blocking capability and ac fault ride-through abilities. The corresponding figures are used to demonstrate simulation results of the real-time simulation.

5.3.1 Voltage Step Change

The system response to a step change of terminal voltage reference is simulated in the real-time simulation model. As shown in Fig. 5.14, the simulation results are generated and plotted for both AAC and system operations. The reference terminal voltage is adjusted from 1.0 to 1.05 pu at time t = 0.2 s, with the power order remaining at 1.0 pu.

When the reference of terminal voltage increases from 1.0 to 1.05 pu at time t = 0.2 s, the measured voltage tracks the reference signal as expected shown in Fig. 5.14(a). The phase voltage at the PCC is indicated in Fig. 5.14(d). Since the measured power order is maintained at 1.0 pu before and after the step change of voltage, the corresponding magnitude of the phase current decreases slightly, which is indicated in Fig. 5.14(e). Once the reference terminal voltage is stepped up to 1.05 pu, modulation index and the submodule capacitor voltages increase immediately. The OOC method adjusts the overlap onset angle in order to eliminate the energy imbalance and regulate submodule capacitor voltages back to their nominal value. As indicated in Fig. 5.14(c), the overlap onset angle changes from -20 degrees to nearly 10 degrees. The submodule capacitors reach steady-state and remain at an approximate voltage of 24 kV in Fig. 5.14(b).

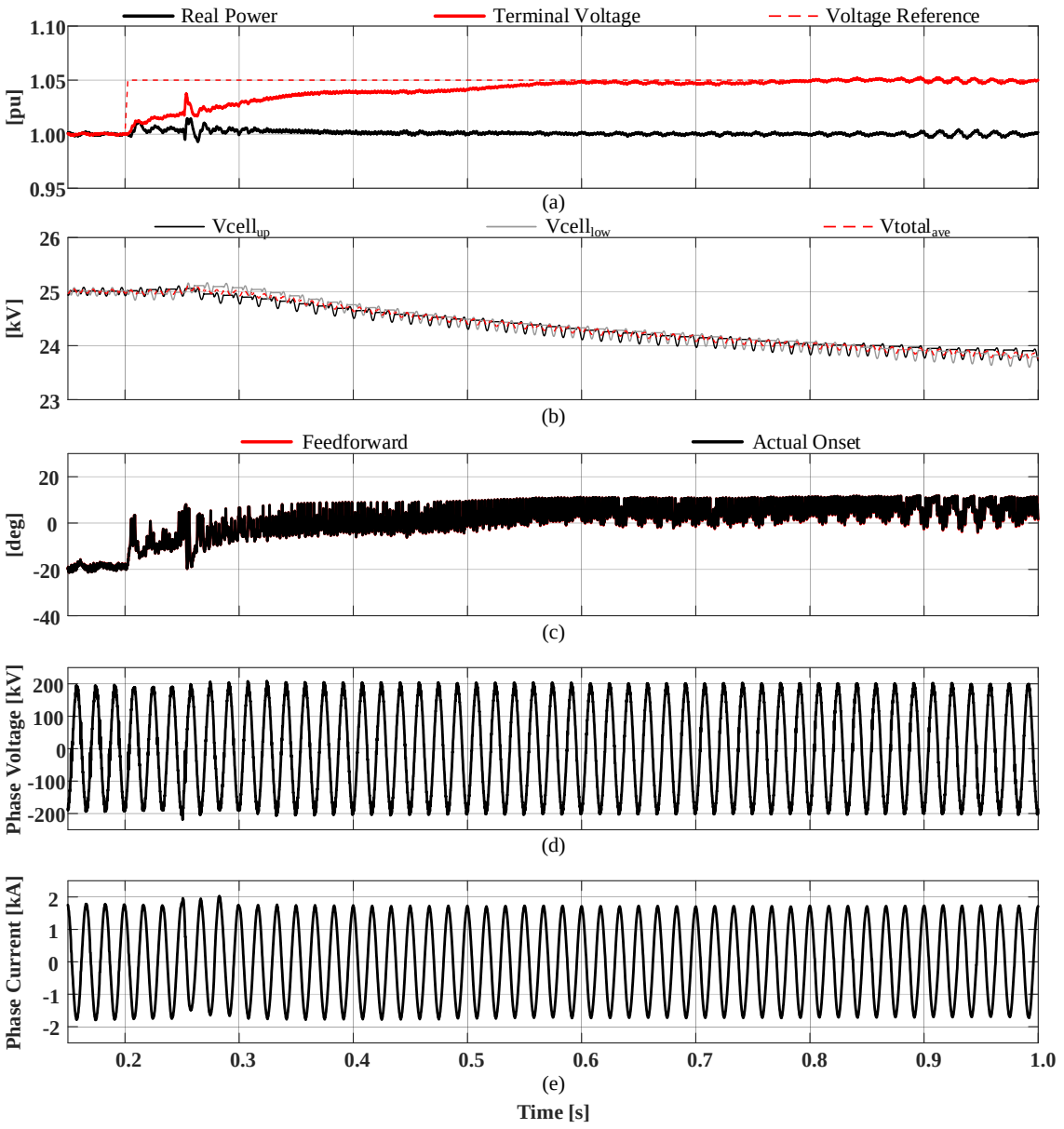

Fig. 5.14: Real-time system responses with reference voltage changes from 1.0 to 1.05 pu. RTDS simulation with step change in reference terminal voltage from 1.0 to 1.05 pu at t = 0.2 s. (a) real power and RMS terminal voltage, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) PCC current of phase A.

Two possible issues may affect the response of the OOC method, which cannot balance the submodule capacitor voltages to the rated value. Firstly, the operating point used to generate real-time simulation result has a modulation index close to the "sweet spot" of $m = 4/\pi$ and a power factor close to unity. That is, from (3.3) the product of $m\pi\cos(\phi)/4$ would

be approximately equal to one, which may reach the maximum limit of inverse cosine calculation. The OOC has a feedforward path using (3.3) to predetermine the value of overlap onset angle. The feedback path is used to slightly adjust the overlap onset angle based on the submodule capacitor voltages. Since the feedback controller is tuned to react to small adjustment, the same feedback path of OOC method cannot control the overlap onset angle independently. Thus, if the feedforward path is saturated, the PI controller of feedback loop can quickly saturate by accumulating excessive errors. When the inverse cosine term becomes very close to the maximum limit, such as 0.99, the OOC method needs to block the feedback path to avoid saturation of overlap onset angle. However, the simulation result in PSCAD/EMTDC model does not experience a situation as shown in Fig. 5.14. This is because all the calculations and control algorithms in PSCAD/EMTDC are implemented in small time-step of 1 μs instead of 50 μs in the real-time simulation of RTDS. Thus, the OOC method would behave less favorably than expected if the system operates too close to the region with $m\pi\cos(\phi)/4$ nearly equal to unity.

Secondly, the overlap onset angle may be located close to the zero-crossing of phase current; i.e., the arm current is very small when the overlap period happens. During the overlap period, both arms insert more than N submodules to commutate current before arm switches out from the conduction path. The PSCAD/EMTDC model uses a small time-step, which can determine the zero-crossing of current much more accurately compared to real-time simulation with time-step of 50 μs. For example, in real-time simulation, both arms insert 11 submodules to drive down the arm current during the overlap period. If the arm current is small when the overlap period starts, the actual arm current can be commutated into the reverse direction, which may result in unbalanced capacitor voltages and energy

imbalance between dc and ac systems. Furthermore, the unbalanced capacitor voltages may lead to system oscillations. The combination of ZCS and MZCS methods can either detect or predict the zero-crossing of arm current in order to turn off director switches with minimal losses. Therefore, the resulting overlap period could be too small for balancing net energy different between dc and ac sides. From (2.10), if the modulation index has a value of $m > 4/\pi$, the net energy of submodules and corresponding capacitor voltages would decrease. By implementing the OOC method, the submodule capacitor voltages slowly balance to approximate 24 kV and remain at this value.

5.3.2 Power Step Change

The dynamic response analysis concerning the step change of power order is tested in the real-time simulation model. The simulation results are indicated in the traces in Fig. 5.15. At time $t = 0.2$ s, the power reference is adjusted from 0.8 to 1.0 pu with the terminal voltage at the PCC maintained at 1.0 pu.

As shown in Fig. 5.15(a), the measured terminal voltage at the PCC overshoots to about 1.02 pu while the power reference increases from 0.8 to 1.0 pu. Then the measured voltage settles into steady-state operation and stays at 1.0 pu, resulting in a relatively constant modulation index of $m = 1.2$. When the power order is stepped up to 1.0 pu, the energy supplied by the dc system increases, which is higher than the energy delivered to the ac system. The energy imbalance between dc and ac systems leads to the growth of net energy within submodule capacitors. Therefore, both upper and lower submodule capacitor voltages increase as illustrated in Fig. 5.15(b). In order to balance the energy difference and regulate the submodule capacitor voltages to the desired value, the OOC method starts to adjust the overlap onset angle as shown in Fig. 5.15(c). The resulting overlap onset angle

has an overshoot to 0 degrees and then slowly changes from -20 degrees to -16 degrees. By properly adjusting the overlap onset angle, the submodule capacitor voltages are restored to their nominal value of 25 kV. In Fig 5.15 (d) and (e), the terminal phase voltage and current at the PCC indicate the transient responses from the system's point of view. When the power order increases to 1.0 pu, the magnitude of the phase voltage does not change because the reference terminal voltage remains at 1.0 pu. In order to supply more real power to the ac system, the corresponding magnitude of phase current increases at time t = 0.2 s as illustrated in Fig. 5.15(e).

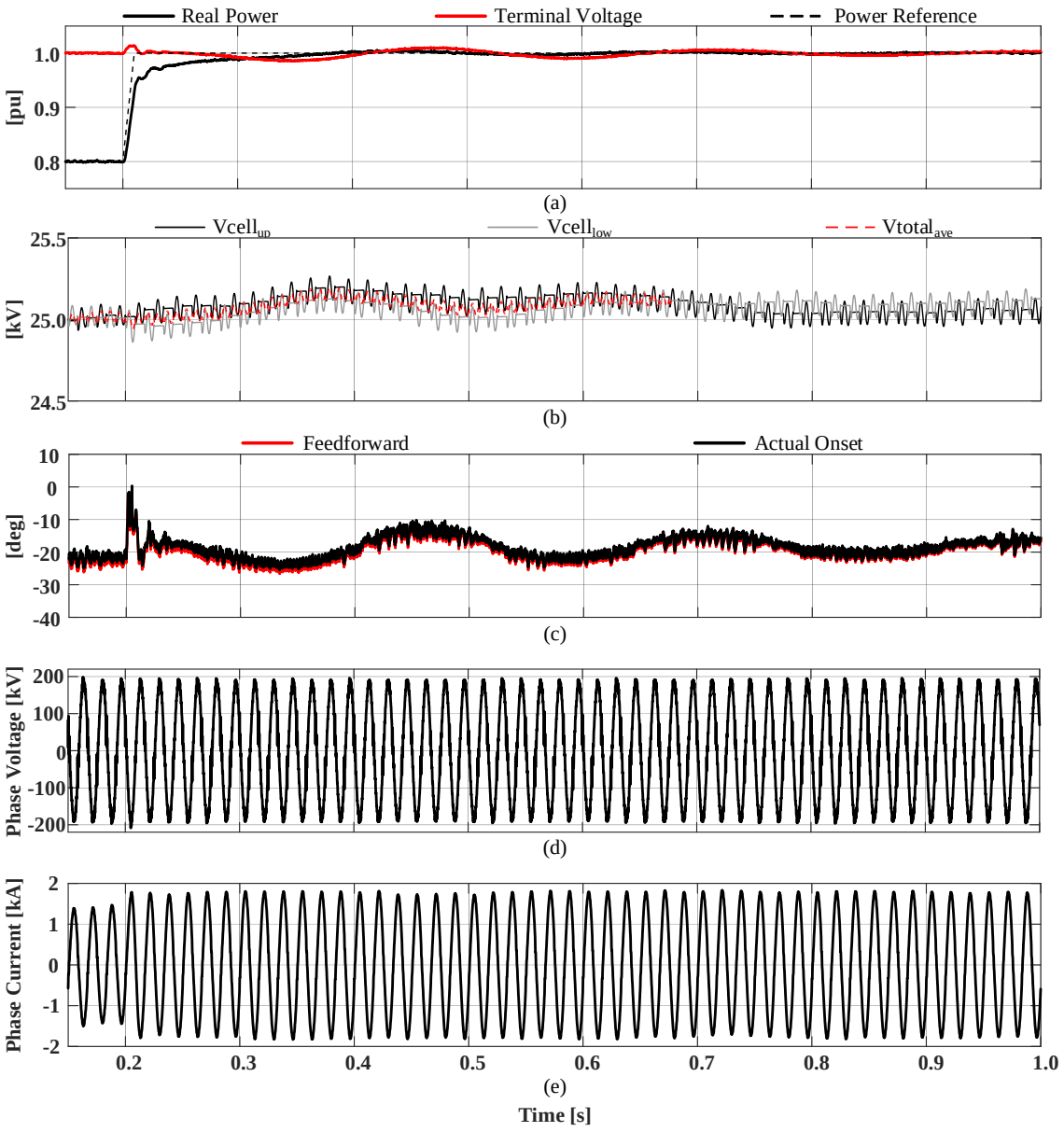

Fig. 5.15: Real-time system responses with power order changes from 0.8 to 1.0 pu.
RTDS simulation with step change in power order from 0.8 to 1.0 pu at t = 0.2 s. (a) real power and RMS terminal voltage, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) PCC current of phase A.

5.3.3 DC Fault Blocking Capability

A dc pole-to-pole fault is applied to the AAC system in order to evaluate the dc fault blocking capability of FB submodules. The system responses of real-time simulation model

regarding pre-fault, during-fault and after-fault conditions are plotted in Fig. 5.16. The pole-to-pole dc fault occurs at time t = 0.2 s with a fault duration of 150 ms.

To detect the dc fault, each arm of the AAC requires a current detector with the maximum limit of 3.0 kA. If any arm experiences that current flowing through it exceeds the threshold value, the dc fault is detected and submodules are blocked. In Fig. 5.16, the dc fault is detected at time t = 0.205 s. When the dc fault occurs, two poles are connected through a small resistance and the phase current flows from the ac side to the faulted dc system. Then all the submodules are blocked, and director switches are turned off. Once the FB submodules are blocked, the phase current flows through each arm and charge up the submodule capacitors. In addition, the FB submodules can oppose the current flowing from ac to the faulted dc side, resulting in isolation between ac and dc systems. As shown in Fig. 5.16(a), the power reference decreases to zero with a 5-ms delay once the dc fault is detected. During the dc fault, the submodule capacitor voltages remain at the pre-fault values, and OOC method freezes the overlap onset angle as illustrated in Fig. 5.16 (b) and (c), respectively. After 150 ms at time t = 0.35 s, the dc fault is cleared. However, the blocking signal is held for 200 ms to avoid large current overshoot, which may lead to re-blocking command of the AAC. When the blocking signal finishes, the power order is ramped up gradually to 1.0 pu as shown in Fig. 5.16(a). The OOC method adjusts the overlap onset angle in order to recover from the fault condition. In Fig. 5.16(d), the spike of terminal phase voltage indicates the beginning of the blocking signal. The appearance of a voltage spike depends on the time when the dc fault is applied to the AAC system. The phase current decreases to zero during the fault and ramps up when the system is in the recovery period as shown in Fig. 5.16(e).

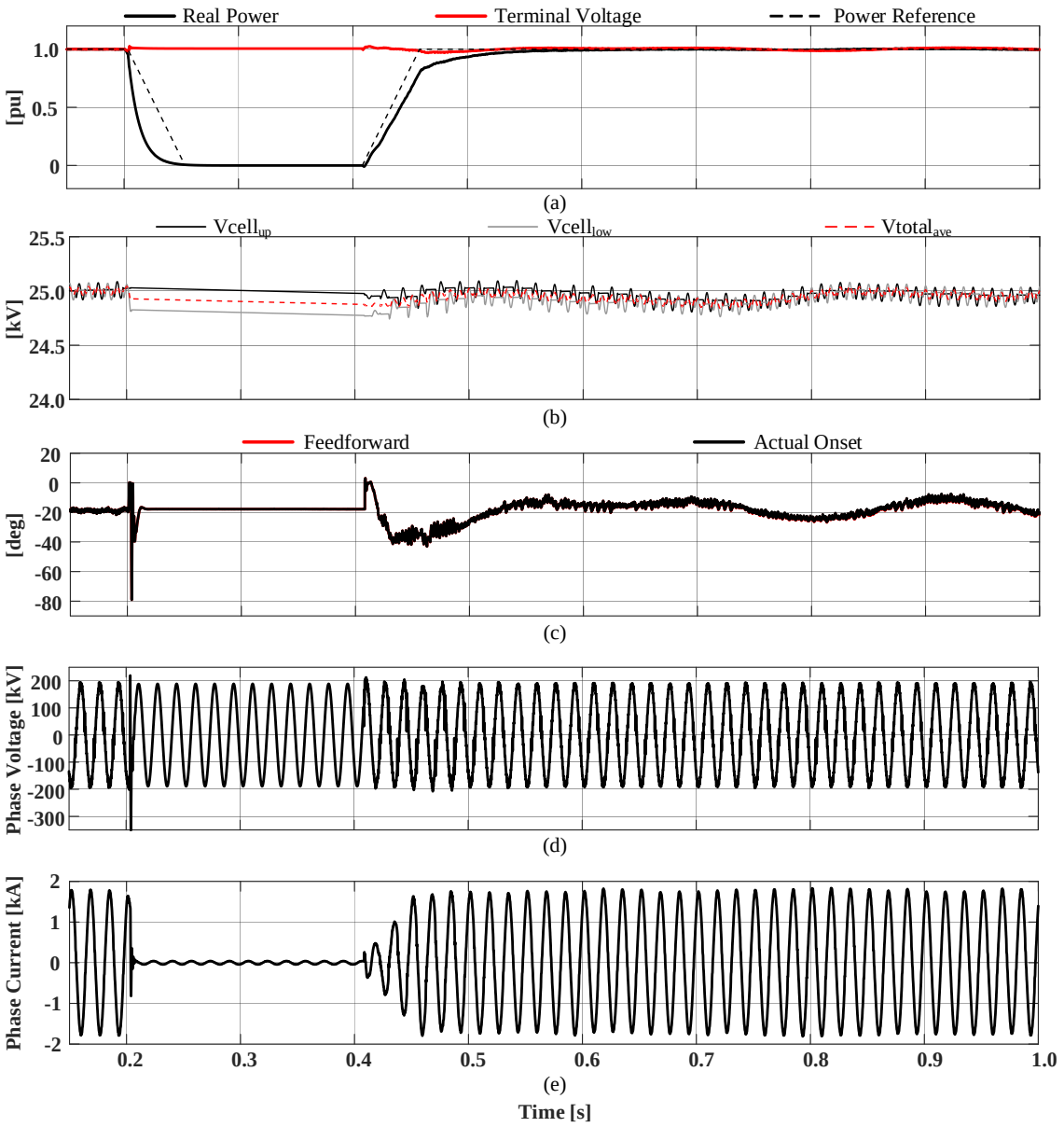

Fig. 5.16: Real-time system responses with dc pole-to-pole fault.
RTDS simulation with dc pole-to-pole fault at t = 0.2 s. (a) real power and RMS terminal voltage, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) PCC current of phase A.

5.3.4 AC Three-phase-to-ground Fault Ride-through

In the real-time simulation, the ac three-phase-to-ground fault ride-through ability is implemented for AAC, and the simulation results are indicated in Fig. 5.17. The ac three-phase-to-ground fault is applied to AAC system at time t = 0.2 s with a fault duration of

150 ms. In order to analyze the system behavior, the operations before, during, and after the fault are compared in Fig. 5.17.

When the three-phase ac fault is applied, the PCC is connected to ground through a small resistance of 0.01 Ω leading to a large current flowing through the arms and phases. For the ride-through capability, the blocking signal of submodules should not be trigged during the fault condition. The measured power and terminal voltage reduce to zero during the fault as shown in Fig. 5.17(a). Due to the three-phase ac fault, the submodule capacitor voltages decrease to about 24 kV immediately as indicated in Fig. 5.17(b). In order to eliminate the energy imbalance within submodules capacitors, the OOC method determines the overlap onset angle based on (3.3). Thus, the overlap onset angle moves from -20 degrees to nearly 0 degrees in Fig. 5.17(c). By adjusting the overlap onset angle, the submodule capacitors charge up and return to the desired voltage. The fault is cleared at time t = 0.35 s with a fault duration of 150 ms, the measured power and terminal voltage are restored to the pre-fault values of 1.0 pu. Since the operating point of the system varies, the OOC method needs to modify the overlap onset angle back to approximately -20 degrees to maintain the submodule capacitor voltages during the normal operation. In Fig. 5.17 (d) and (e), the terminal phase voltage and current for the simulation results of three-phase ac fault are shown. When the ac three-phase-to-ground fault occurs, the terminal voltage at the PCC reduces to zero, leading to an increased magnitude of phase current.

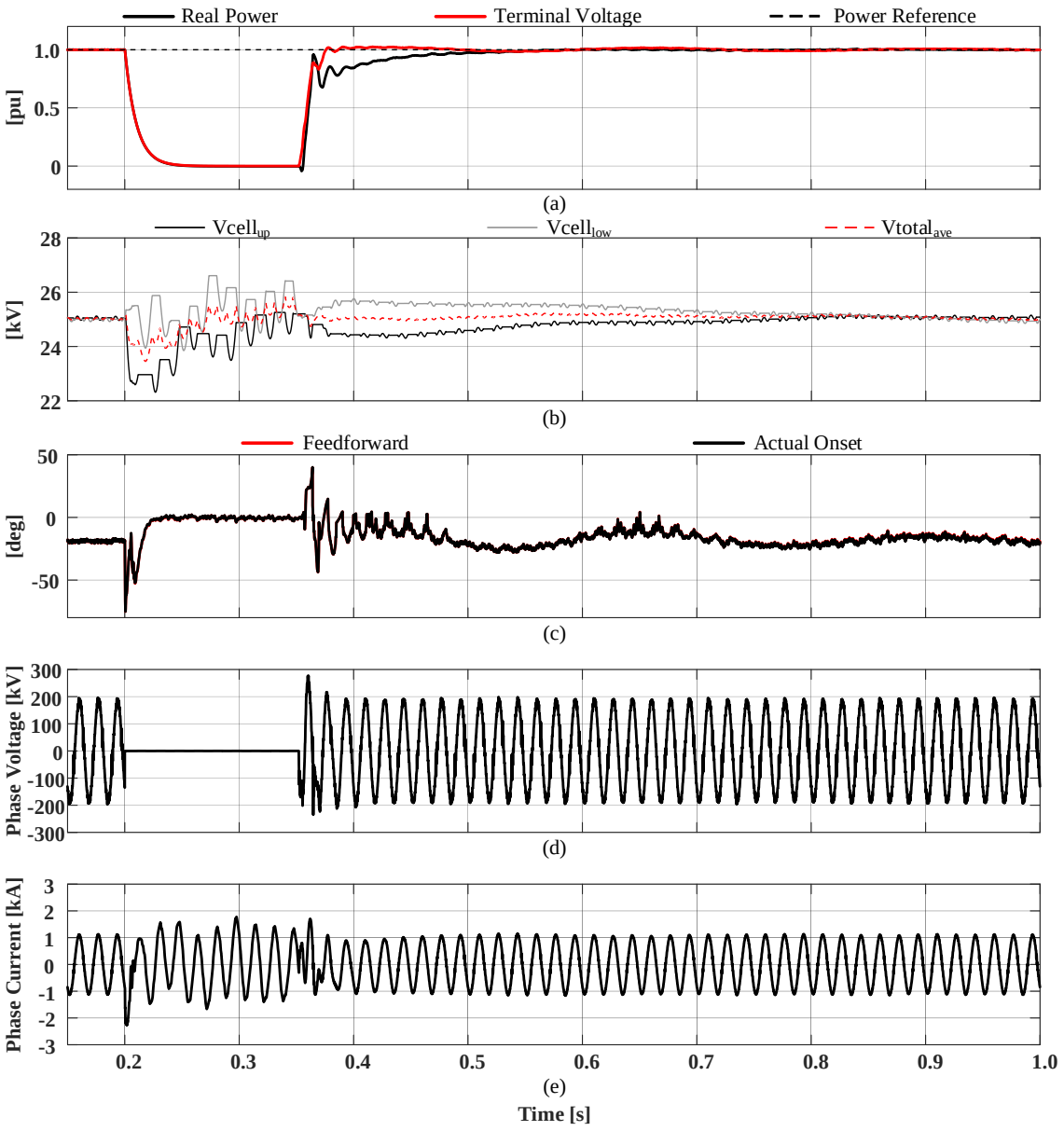

Fig. 5.17: Real-time system responses with ac three-phase-to-ground fault.
RTDS simulation with ac three-phase-to-ground fault at t = 0.2 s. (a) real power and RMS terminal voltage, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) converter side current of phase A.

5.3.5 AC Remote Fault Ride-through

For ac remote fault ride-through capability, the real-time simulation results of AAC system are illustrated in Fig. 5.18. The ac remote fault happens at time t = 0.2 s with a fault duration of 150 ms. To emulate the ac remote fault at the ac system side, 10% magnitude

reduction and 5° of phase shift are implemented to the ac source. The system performance regarding the operations before, during, and after the fault are captured in Fig. 5.18.

In Fig. 5. 18(a), the measured terminal voltage at the PCC reduces to approximately 0.92 pu once the ac remote fault is applied to the AAC system. Meanwhile, the measured power order remains relatively constant at 1.0 pu. The OOC method takes care of the energy imbalance when the fault occurs. Because both the voltage magnitude and phase shift are changed to emulate the ac remote fault, the overlap onset angle varies from -20 degree to about -8 degrees as indicated in Fig. 5.18(c). As illustrated in Fig. 5.18(b), the resulting submodule capacitor voltages remain at the nominal value during the ac remote fault. The remote fault is cleared after 150 ms at time t = 0.35 s by modifying the ac source back to the pre-fault condition. The measured terminal voltage increases to the steady-state value of 1.0 pu. The OOC reacts quickly to bring the overlap onset angle to the pre-fault value. The system responses regarding phase voltage and current are shown in Fig. 5.18 (d) and (e). Due to the voltage reduction at ac side, the magnitude of the phase voltage decreases when the ac remote fault occurs. The magnitude of phase current increases correspondingly to supply the same amount of power to the AAC system.

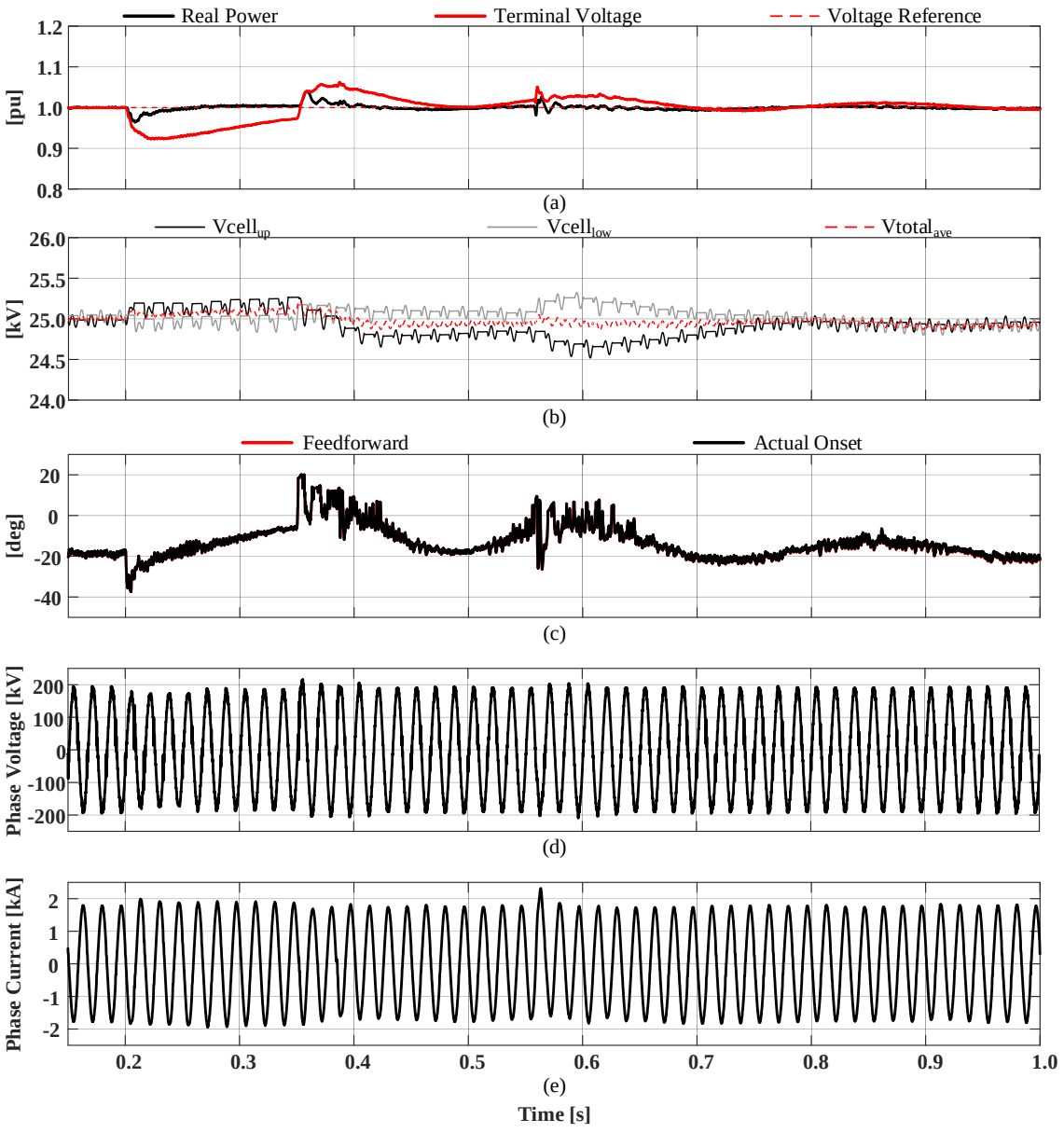

Fig. 5.18: Real-time system responses with ac remote fault.
RTDS simulation with ac remote fault at t = 0.2 s. (a) real power and RMS capacitors, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) PCC current of phase A.

5.3.6 AC Single-phase-to-ground Fault Ride-through

Based on the simulation results in the previous two sections, AAC system can ride through the balanced faults without blocking the converter and tripping ac breakers. In order to evaluate system performance during an unbalanced fault, an ac single-phase-to-

ground fault is applied to phase A of the AAC system at time t = 0.2 s with a fault duration of 150 ms. The real-time simulation results are shown in Fig. 5.19 including the operation before and after the fault as well as during the fault conditions.

When the ac single-phase-to-ground fault is applied to phase A, the faulted phase has an increased phase current and zero phase voltage as shown in Fig. 5.19 (d) and (e), respectively. Due to the unbalanced fault, the RMS terminal voltage has a reduction to approximately 0.75 pu as shown in Fig. 5.19(a). Also, the measured power order reduces to nearly zero during the ac single-phase-to-ground fault. When the unbalanced fault occurs, submodule capacitors discharge based on the net energy difference between dc and ac systems. In order to ride-through the unbalanced fault, an additional three submodules, i.e., 13 submodules are inserted for the MZCS operation. In Fig. 5.19(c), the OOC method controls the overlap onset angle based on the modulation index with some ripples. The ripples have a frequency that is twice of the fundamental frequency component. The submodule capacitor voltages maintain at about 22 kV once the unbalanced fault is detected as shown in Fig. 5.19(b). During the fault, the current for phase A at the converter side is indicated in Fig. 5.19(e). The phase current has a small overshoot with a magnitude slightly higher than 3.0 kA, which is the transient response of the system when the fault is detected. However, most of the current magnitude is maintained within the threshold of 3.0 kA during the steady-state operation. After a fault duration of 150 ms at time t = 0.35 s, the unbalanced ac fault is cleared. The OOC method modifies the overlap onset angle to restore to the normal operation. In Fig. 5.19(c), the overlap onset angle slowly increases and settles to the pre-fault value of -20 degrees. The measured terminal voltage and power at the PCC

side retain their normal condition of 1.0 pu. Consequently, the submodule capacitor voltages increase gradually and regulate back to the nominal value of 25 kV.

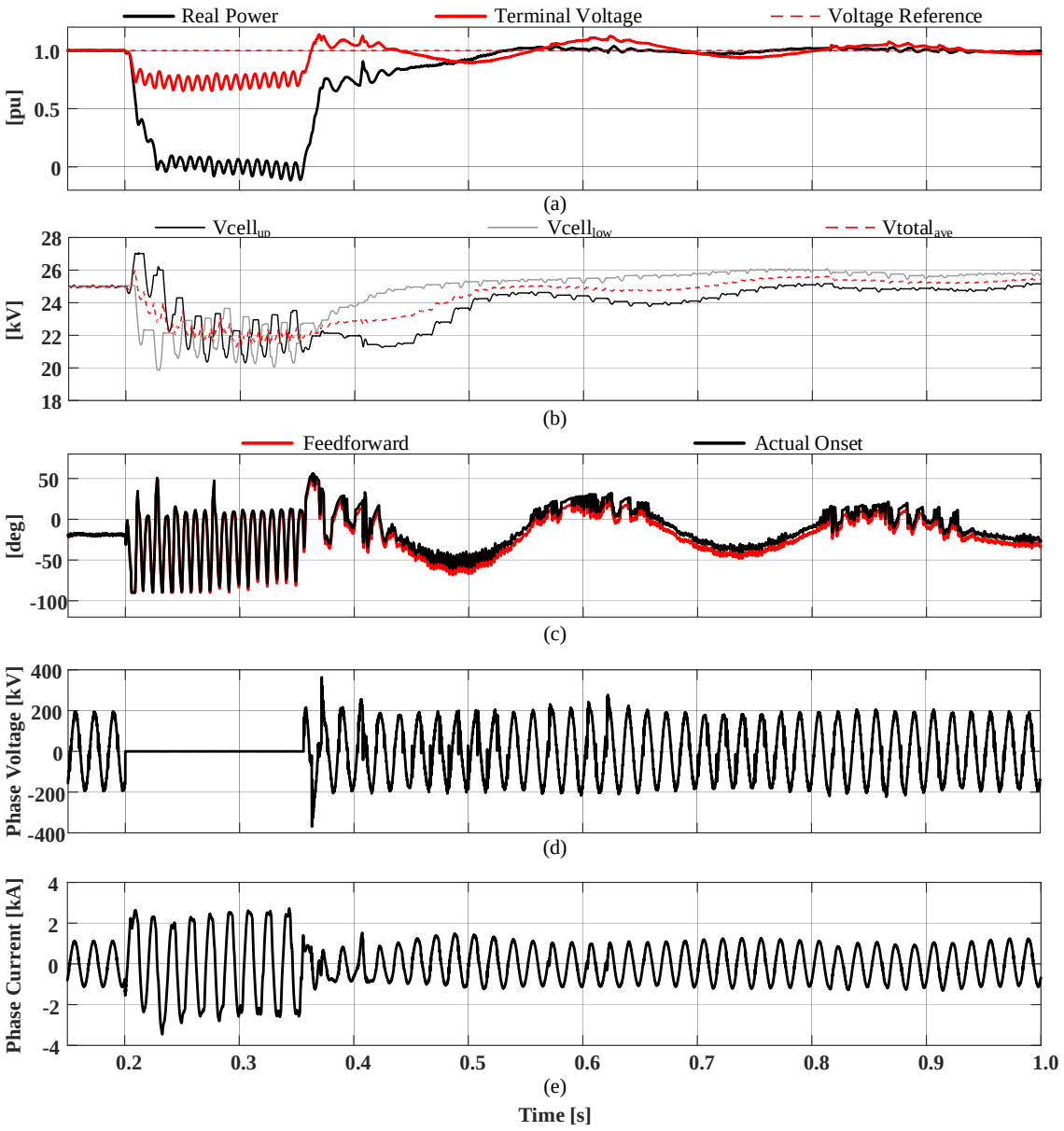

Fig. 5.19: Real-time system responses with ac single-phase-to-ground fault.
RTDS simulation with ac single-phase-to-ground fault at t = 0.2 s. (a) real power and RMS terminal voltage, (b) upper and lower submodule capacitor voltages and the average voltage for all submodule capacitors, (c) calculated μ and actual μ, (d) PCC voltage of phase A, (e) converter side current of phase A.

Chapter 6: Contributions, Conclusions, and Recommendations for Future Work

In this chapter, the overall contributions and conclusions of the research studies conducted in the thesis are discussed. Recommendations are made for future work based on the analysis and simulation results shown in this thesis.

6.1 Contributions

This thesis discussed the alternate arm converter (AAC) and a control method (OOC) to address the energy imbalance issues within the converter. The contributions are listed as following:

1. Basic operation of the alternate arm converter (AAC) was analyzed using simplified converter models;
2. Energy imbalance issues within the converter were analyzed;
3. A new method for capacitor voltage regulation and energy balancing, referred to as overlap onset control (OOC) was co-developed (with another graduate student). This method functions based upon adjustments to the onset of the overlap period and deploys zero-current switching.
4. A real-time model of the AAC and the associated OOC and ZCS schemes were implemented and fully tested.
5. An enhanced phase-locked loop (EPLL), specially designed for unbalanced faults, was analyzed and implemented in both in PSCAD/EMTDC and RTDS real-time simulators.

6. A comprehensive suite of analyses was conducted both in PSCAD/EMTDC and RTDS real-time simulators to fully analyze the developed converter control systems under normal and faulted operating conditions.

6.2 Conclusions

The results of EMT analyses in PSCAD/EMTDC showed that the AAC can operate properly from system aspects; i.e., the AAC tracks its reference signal and recovers from different fault conditions as expected. The OOC method was able to balance the energy difference and regulate submodule capacitor voltages to the desired value. Regardless of the type of system tests, the OOC method was able to adjust the overlap onset angle to maintain the capacitor voltage.

In real-time simulation of RTDS, the AAC system with the same parameters showed dynamic and steady-state performances that were approximately identical to the simulation results in PSCAD/EMTDC. The OOC method controlled the overlap onset angle based on the derived equation as (3.3) and feedback adjustments, resulting in a good performance to restore submodule capacitor voltage to the nominal value. However, for the simulation results of the terminal voltage step change, it showed that OOC method with a large time-step may have difficulty to balance the net energy of FB submodules. The OOC method had two possible constraints including the saturation of the feedforward path in the OOC controller and undesired magnitude of phase current when overlap period occurred. The OOC method was only able to retain submodule capacitor voltages at a value that is not equal to the desired voltage. The OOC method cannot work as well as expected if the operation point is too close to the saturation limits of the feedforward path.

6.3 Recommendations for Future Work

In terms of the dynamic performance for OOC method and operation of AAC system under fault conditions, the following recommendations for future work are made:

1. To avoid saturation of the feedforward path in the OOC controller, two possible modifications may be implemented.
    a) Implement and use the AAC with respect to a system with non-unity power factor instead of unity power factor; this implies that the system will generate/absorb reactive power during steady-state operation and ac system faults.
    b) Use the feedforward loop as a reference or guidance instead of direct offset for adjusting the overlap onset angle.
2. For ac single-phase-to-ground fault ride-through operation, the phase current could be balanced among three-phase with smaller magnitude by introducing complex control methods such as positive and negative sequence decoupled control [56-61].
3. Inject third harmonic components to the reference waveforms of the stack voltage in order to reduce the additional number of submodules required for output voltage tracking during overlap period conduction [51].
4. To evaluate the losses using the OOC method and make a comparative assessment with other energy regulation methods discussed in the existing research studies [62].

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Appendix A

Decoupled Control in PSCAD/EMTDC Simulation

Appling ABC to DQ0 transformation with relationship matrix (4.2) to the state space equation in (4.1), the d and q components are determined as follows. For clear explanation, the relationship matrix is denoted as $K_p(\theta)$.

$$\begin{aligned} v_{con\_dq0}(t) &= K_p(\theta)\cdot v_{con\_abc}(t) \\ &= K_p(\theta)\cdot L\cdot\frac{d}{dt}[K_p{}^{-1}(\theta)\cdot i_{dq0}(t)] + K_p(\theta)\cdot R\cdot K_p{}^{-1}(\theta)\cdot i_{dq0}(t) + v_{ac\_dq0}(t) \\ &= K_p(\theta)\cdot L\cdot\{[\frac{d}{dt}K_p{}^{-1}(\theta)]\cdot i_{dq0}(t) + [\frac{d}{dt}i_{dq0}(t)]\cdot K_p{}^{-1}(\theta)\} + \\ & K_p(\theta)\cdot R\cdot K_p{}^{-1}(\theta)\cdot i_{dq0}(t) + v_{ac\_dq0}(t) \end{aligned}$$

Substituting $K_p(\theta)$ by (4.2), the d and q components are calculated as shown below.

$$\begin{bmatrix} v_{cond} \\ v_{conq} \\ v_{con0} \end{bmatrix} = \begin{bmatrix} 0 & \omega L & 0 \\ -\omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} \frac{d}{dt}i_d \\ \frac{d}{dt}i_q \\ \frac{d}{dt}i_0 \end{bmatrix} + R\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} v_{acd} \\ v_{acq} \\ v_{ac0} \end{bmatrix}$$

The d and q components of converter's voltage is described as follows, which is the same as (4.3).

$$v_{cond} = \omega L i_q + R\cdot i_d + L\frac{di_d}{dt} + v_{acd}$$

$$v_{conq} = -\omega L i_d + R\cdot i_q + L\frac{di_q}{dt} + v_{acq}$$

Decoupled Control in Real-time Simulation

Appling ABC to DQ0 transformation with relationship matrix (4.5) to the state space equation as (4.1), the d and q components are determined as follows. For clear explanation, the relationship matrix is denoted as $K_r(\theta)$.

$$\begin{aligned} v_{con\_dq0}(t) &= K_r(\theta)\cdot v_{con\_abc}(t) \\ &= K_r(\theta)\cdot L\cdot\frac{d}{dt}[K_r{}^{-1}(\theta)\cdot i_{dq0}(t)] + K_r(\theta)\cdot R\cdot K_r{}^{-1}(\theta)\cdot i_{dq0}(t) + v_{ac\_dq0}(t) \\ &= K_r(\theta)\cdot L\cdot\{[\frac{d}{dt}K_r{}^{-1}(\theta)]\cdot i_{dq0}(t) + [\frac{d}{dt}i_{dq0}(t)]\cdot K_r{}^{-1}(\theta)\} + \\ &\quad K_r(\theta)\cdot R\cdot K_r{}^{-1}(\theta)\cdot i_{dq0}(t) + v_{ac\_dq0}(t) \end{aligned}$$

Substituting $K_r(\theta)$ by (4.5), the d and q components are calculated as shown below.

$$\begin{bmatrix} v_{cond} \\ v_{conq} \\ v_{con0} \end{bmatrix} = \begin{bmatrix} 0 & -\omega L & 0 \\ \omega L & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} \frac{d}{dt}i_d \\ \frac{d}{dt}i_q \\ \frac{d}{dt}i_0 \end{bmatrix} + R\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} v_{acd} \\ v_{acq} \\ v_{ac0} \end{bmatrix}$$

The d and q components of converter's voltage is described as follows, which is the same as (4.6).

$$v_{cond} = -\omega L i_q + R\cdot i_d + L\frac{di_d}{dt} + v_{acd}$$

$$v_{conq} = \omega L i_d + R\cdot i_q + L\frac{di_q}{dt} + v_{acq}$$