DESIGN OF CANONIC WAVE DIGITAL FILTERS WHICH SUPPRESS ALL ZERO-INPUT PARASITIC OSCILLATIONS

by

Mark R. Jarmasz

A thesis
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ABSTRACT

This thesis proposes two methods of designing canonic wave digital filters with a diagonal reference conductance matrix. The first method is based on the exact diagonalization of the nondiagonal reference conductance matrix which results when redundant delays are eliminated from the wave digital structure. The second method uses a network equivalence transformation to obtain analog prototype networks with a minimum number of reactive elements. It is shown that, in most cases, it is necessary, and furthermore possible, to redefine the independent design parameter set such that the resulting entries in the scattering matrix S are expressed as sums of products of the new independent parameters. This is sufficient to ensure that the subsequent quantization of the independent parameters to binary fractions also produces binary fractions for the entries in S. Solutions are presented for the Brune, 3rd-, and 5th-order elliptic topologies.

This thesis also demonstrates that it is possible to obtain quantized designs that satisfy the given specifications via a simple search in a bounded feasible region. The search generates a large number of feasible, quantized parameter sets which are then tested to determine their suitability.

The existence of the corresponding analog prototype provides an efficient way of computing the required attenuation characteristic, which greatly reduces the total execution time.

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Chapter I

INTRODUCTION

A digital filter is a structure that implements a computational algorithm which is derived from a difference equation. This structure operates on an input sequence of numbers and produces an output sequence of numbers. A specific filtering algorithm is characterized by the relationship existing between the input and output sequences, which is either specified in the time or the frequency domain. A number of techniques exist for the implementation of the computational algorithm. These range from a software program executed on a general-purpose computer to a dedicated single chip realization [1].

Digital filters are synthesized and analyzed using the discrete-time system theory. A particular class of linear, shift-invariant (LSI) systems is suitable for this purpose, and a number of important references have been published [2]-[6]. In a practical simulation of a discrete-time system, signals and system coefficients are approximated using finite precision arithmetic. Errors arising due to these approximations are termed finite-word- length (FWL) effects, and are placed in three categories [7]-[8]:

1. Coefficient quantization refers to truncation or rounding of multiplier coefficients or some other intermediate design parameters, and causes degradation of the filter's frequency response. The degradation is deterministic and the linearity of the system is preserved.
2. Roundoff error is caused by rounding off or truncating the products formed within the digital structure. In most cases this error can be modelled with an uncorrelated noise source, however periodic roundoff error sequences are possible and are referred to as parasitic oscillations or limit cycles of the granularity type. These oscillations are self-sustaining and exist under zero-input conditions.
3. Overflow occurs when the signal is too large for storage, using the given register length. If no compensation is made, then large errors in the filter output appear either in the form of transients or overflow oscillations.

Clearly, digital filter structures with the ability to control and minimize FWL effects are preferred.

A particular choice of a digital filter structure is made easier by using the well-known fact that structures with low sensitivity to coefficient quantizations also generate low levels of roundoff noise [9]-[11]. The traditional method of direct realization of the transfer function H(z), where

coefficients of H(z) are the actual multipliers, suffers from high sensitivity to coefficient quantizations. Factorization of H(z) into the parallel or cascade forms of first- and second-order sections greatly reduces the sensitivity problems, but performance with respect to other FWL effects is still poor. Ultimately, first- and second-order sections were developed that suppress all parasitic oscillations [12]-[14], and generate low levels of roundoff noise due to low coefficient sensitivities [15]-[17]. The actual choice, however, is made difficult due to the available tradeoffs that exist between the various sections with respect to: 1) suppression of parasitic oscillations, 2) low coefficient sensitivities, 3) number of coefficients that must be quantized, 4) availability of the design tools (how easy is it to program the various design strategies), 5) complexity of the resulting computational algorithm.

An alternative to the conventional structures, which compares favorably with respect to the five points mentioned above, was developed by Fettweis et. al. [18]-[21], and is known as the wave digital (WD) structure. Wave digital filters are based on the premise that digital filter structures that imitate the topology of analog ladder networks, which are known to have low coefficient sensitivity properties, will also have these properties and can be implemented with low-coefficient word lengths. To make the resulting digital filter computable [22], Fettweis used voltage waves for the

signals which together with the bilinear z-transformation map the analog reference network into the corresponding digital structure. Using this scheme, reactive elements map into simple delays, and the parallel and series interconnections of ports are simulated using adaptors [23]. Further developments include symmetrical lattice [24] and Jaumann [25] topologies as prototypes.

In addition to low-coefficient sensitivity, Fettweis and Meerkötter [26] have derived, using the concept of stored pseudopower or equivalently the Lyapunov function, a magnitude truncation scheme which is sufficient to ensure the suppression of all zero-input parasitic oscillations.

The number of delays in the WD structure equals the number of reactive elements in the analog prototype. Ladder networks with finite attenuation poles (transmission zeros) are nonminimal in the number of reactive elements, and WD filters derived from them have more delays than are necessary. Fettweis has developed methods for removing the redundant delays at the expense of no longer being able to guarantee the suppression of all zero-input parasitic oscillations using the magnitude truncation scheme [27]-[28].

Wave digital ladder filters consist of an interconnection of basic adaptors. These adaptors simulate parallel and series interconnection of at most three ports, which is to ensure that the independent design parameters become the actual multipliers in the flowgraphs of the adaptors [23]. A

consequence of this arrangement is that WD filters require more adders than conventional designs [2]. An alternative to the above structure, developed by Martens and Meerkötter [29], employs an overall scattering matrix representation for the entire network, which results in a single n-port adaptor. An advantage of this approach is that networks with arbitrary topology can be used as prototypes for WD structures. Also, Ashley [30] has derived methods for removing all types of reactive redundancies without introducing additional parameters. This was not possible using Fettweis's multiple adaptor approach. Ashley has also derived the necessary and sufficient conditions for the existance of a diagonal Lyapunov function which is sufficient for ensuring the suppression of all zero-input parasitic oscillations. It turns out, however, that these condtions cannot be satisfied by most networks. Moon [31] has shown that nonlinear stability can be guaranteed by using a near-diagonal Lyapunov function, and derived bounds on the off-diagonal terms. These bounds, however, were quite restrictive, and De Luca [32] employed the concept of strict pseudopassivity to derive less stringent bounds. Furthermore, De Luca and Martens [33] have applied the concept of strict pseudopassivity to general state-space structures.

An alternate approach for ensuring nonlinear stability is to diagonalize the available nondiagonal port reference conductance matrix [30]. This method necessarily introduces

additional parameters which can be expressed as rational functions of the independent parameters.

This thesis proposes an exact diagonalization procedure which effectively transforms the nonminimal ladder prototypes into minimal prototypes with ideal transformers. The independent design parameter set is redefined such that all entries in the new scattering matrix are expressed as sums of products of the independent parameters. This is sufficient to ensure that subsequent quantization of the independent parameters to FWL binary numbers results in the FWL binary scattering matrix. Thus, the resulting WD structure is based on a canonic number of design parameters, which is equal to the number of degrees of freedom, and consists of a canonic number of delays which is equal to the order of the filter. Also, a diagonal Lyapunov function exists which together with a sign- magnitude truncation scheme ensures the complete suppression of all zero-input parasitic oscillations.

Chapter II presents a brief summary of the relationship between continuous-time and discrete-time signals, and of the classical approach to the design of digital filters. WD filters realized using n-port adaptors generally require more multiplications than the canonic number. Consequently, these adaptors are better suited for implementation using the newly developed distributed arithmetic techniques [34]-[40]. Chapter II concludes with a discussion of digital

filter implementation using distributed arithmetic structures.

Chapter III introduces the concept of WD filters. The n-port adaptor approach is described along with the reflection-free property which is necessary to effect the interconnection of various adaptors. Design examples of adaptors based on the parallel, series, and 3rd-order elliptic topologies are presented using the n-port adaptor approach. Next, linear stability of WD networks is deduced using the general properties of these networks. Also, sufficient conditions for ensuring nonlinear stability are stated. Canonic WD n-port adaptors are obtained using the reactive redundancy removal procedure developed by Ashley [30], and the removal of redundancies due to capacitive loops is discussed in detail. The chapter concludes with the application of the exact diagonalization procedure, as introduced by Ashley [30] and elaborated upon in [41], to the 3rd-order elliptic adaptor.

In Chapter IV we derive the independent parameter sets for the basic minimal adaptors, including the Brune, 3rd- and 5th-order elliptic topologies. It is shown that these parameter sets can be derived using two distinct approaches: 1) method of redundancy removal followed by diagonalization, 2) application of a network equivalence to generate minimal analog prototypes. Also, it is demonstrated that an imposition of certain element constraints leads to much simplified designs. The entries in the resulting S matrices are ex-

pressed as sums of products of the independent parameters, which is sufficient to ensure that with the subsequent parameter quantizations the resulting coefficient matrix S is FWL binary.

An advantage gained in constraining the number of parameter quantizations to the canonic number, which contrasts with the methods proposed in [30]-[33], is that a corresponding analog network exists which can be used in evaluating the frequency response of the corresponding discrete-time filter. As a result, the computational requirement in evaluating the attenuation characteristic is greatly reduced. In Chapter V we use this reduction and propose a simple quantization algorithm that is based on a finite search in the neighborhood of an initial FWL binary approximation of the parameter set. The search generates a large number of feasible quantized parameter sets which are then tested to determine their suitability. The chapter concludes with the presentation of design examples of WD filters based on 3rd- and 5th-order elliptic prototypes.

Chapter II

INTRODUCTION TO DISCRETE-TIME SYSTEMS AND DIGITAL FILTERS

This chapter presents a brief summary of the relationship between continuous-time and discrete-time signals which is fundamental to the analysis and synthesis of discrete-time systems. The classical approach to the design of digital filters based on the transformation of the analog transfer function to a digital transfer function is briefly described. Also, implementation of digital filters based on the principle of distributed arithmetic for the computation of inner products is discussed.

2.1 RELATIONSHIP BETWEEN CONTINUOUS-TIME AND DISCRETE-TIME SIGNALS

Discrete-time signals are defined only for discrete values of the independent variable, i.e., the independent variable is quantized. Mathematically, such signals are represented as sequences of numbers. Discrete-time signals that take on a continuum of values are referred to as sampled-data signals, whereas those with quantized amplitudes are digital signals [3].

Discrete-time signals are usually derived from sampling a continuous- time signal, $f(t)$. Sampled signals $f^*(t)$ can be expressed in a number of ways [6]:

$$f^*(t) = f(t)\delta_T(t) \tag{2.1a}$$

$$= \sum_{n=-\infty}^{\infty} f(nT)\delta(t-nT) \tag{2.1b}$$

$$= \frac{1}{T}\sum_{n=-\infty}^{\infty} f(nT)e^{-jn\omega_s t} \tag{2.1c}$$

where T is the sampling period, $\omega_s=2\pi/T$, $\delta(t)$ the Dirac impulse, and (2.1c) follows from the Fourier series expansion of the impulse train function, $\delta_T(t)$. The Fourier transform of (2.1b) yields

$$F^*(\omega) = \sum_{n=-\infty}^{\infty} f(nT)e^{-jn\omega T} \tag{2.2}$$

The two-sided z-transform of the sequence { f(nT), n is an integer }, is defined as

$$F(z) \triangleq \sum_{n=-\infty}^{\infty} f(nT)z^{-n} \tag{2.3}$$

If the region of convergence of F(z) includes $z=e^{j\omega T}$, which is the unit circle in the z-plane, then $F(e^{j\omega T})$ is defined as the frequency spectrum of { f(nT), n is an integer}. That this definition is justified follows from (2.2) and (2.3), i.e.

$$F(z)\Big|_{z=e^{j\omega T}} = F^*(\omega) \tag{2.4}$$

from which it is clear that the z-transform of a sequence evaluated on the unit circle equals the Fourier transform of that sequence. A more general result can be obtained by us-

ing the Laplace transform instead of the Fourier transform. Using (2.1b) and (2.1c), the Laplace transform of f*(t) yields

$$F^*(s) = \sum_{n=-\infty}^{\infty} f(nT)e^{-snT} \tag{2.5a}$$

$$= F(z)\Big|_{z=e^{sT}} \tag{2.5b}$$

$$= \frac{1}{T}\sum_{n=-\infty}^{\infty} F(s+jn\omega_s) \tag{2.5c}$$

The nonlinear mapping, $z=e^{sT}$, maps horizontal strips of width $2\pi/T$ in the s-plane onto the entire z-plane [3]-[6]. It is clear from (2.5c) that $F^*(\omega)=F(\omega)/T$ only if $F(\omega)=0$ for $|\omega|>\omega_s/2$. If this condition is violated, then aliasing is said to have occurred and f(t) cannot be recovered from its samples {f(nT), n is an integer }. The above is stated more generally in the form of a sampling theorem [6].

Sampling Theorem: Let f(t) be a band-limited signal with its highest frequency component less than W. Then, f(t) is completely specified by its sampled values with sampling frequency equal to or greater than 2W.

As a result of the sampling theorem, most discrete-time systems that derive their input signal from sampling a continuous-time signal are preceded in practice by an anti-aliasing or guard filter. Also, the spectrum of the input signal is periodic, hence, the frequency response of the discrete-time system must also be periodic.

2.2 CLASSICAL APPROACHES TO THE DESIGN OF DIGITAL FILTERS

Design of a digital filter is a search for a linear, shift-invariant discrete-time system that satisfies given specifications and is implemented using finite precision arithmetic. Various approximation techniques are used to find an appropriate discrete-time system. For infinite-impulse-respose (IIR) filters the desired frequency response is approximated by a rational function of z, and for finite-impulse-response (FIR) filters a polynomial approximation is used. For standard analog specifications, such as Butterworth,Chebyshev, and elliptic, extensive analog design tables are available. Thus, the traditional approach to the design of IIR digital filters involves a transformation of an analog transfer function in ψ to a discrete-time transfer function in z [3]-[6]. In this approach ψ is replaced by a function of z which has the following properties:

1. The $j\Omega$ axis in the ψ-plane,or an appropriate part thereof, maps into the unit circle in the z-plane. This property preserves the desired frequency response in the resulting digital filter.
2. Poles in the left-half ψ-plane map into poles inside the unit circle in the z-plane. This property ensures that the resulting digital filter is linearly stable.

The most widely used transformation

$$\psi = \tanh(sT/2) = \frac{e^{sT} - 1}{e^{sT} + 1} = \frac{z - 1}{z + 1} \qquad (2.6)$$

possesses the above properties and is called the bilinear z-transformation. Using (2.6), a rational function in ψ becomes a rational function in z, i.e.

$$H(z) = T(\psi)\Big|_{\psi = \frac{z-1}{z+1}} \tag{2.7}$$

The relationship between the digital frequency ω and the analog frequency Ω is obtained by setting $\psi = j\Omega$ and $z=e^{j\omega T}$ in (2.6), which yields

$$\Omega = \tan(\omega T/2) \tag{2.8}$$

The nonlinear mapping between Ω and ωT , introduced by the bilinear transformation, can be compensated for by prewarping the coefficient values in the analog prototype transfer function. Prewarping transforms the critical analog frequencies into the desired critical digital frequencies. The nonlinear mapping as expressed in (2.8) is depicted in Fig. 2.1.

Another common transformation used involves sampling of the impulse response of a continous-time filter to obtain the impulse response sequence of the digital filter. This technique is called the impulse invariance and the relationship between ψ and z is mathematically eqivalent to the relationship between s and z as derived for continuous and discrete-time signals. This method is only applicable to band-limited characteristics.

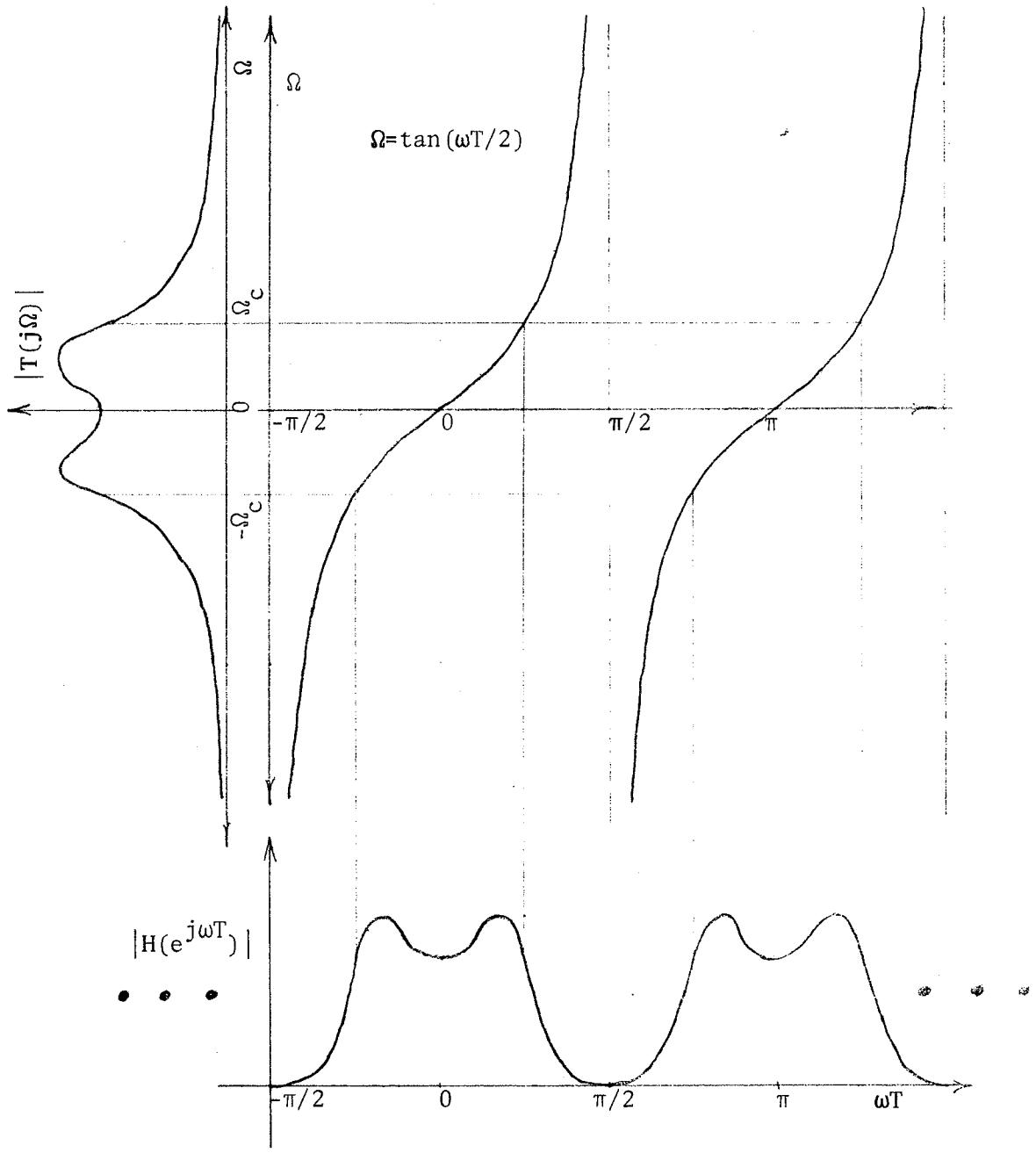


Figure 2.1: Nonlinear mapping $\Omega = \tan(\omega T/2)$ due to bilinear z-transformation

The discrete-time transfer function H(z) can be expressed according to the chosen mode of implementation, i.e. let

$$H(z) = \frac{\sum_{k=0}^{N} b_k z^{-k}}{1 - \sum_{k=1}^{N} a_k z^{-k}} = b_o \prod_{i=1}^{K} H_i(z) = c + \sum_{j=1}^{K} H_j(z) \qquad (2.9a,b,c)$$

where K=[(N+1)/2] ([] denotes integer part of), and c is proportional to b_N. Decomposition of a high-order system (N>2) into a cascade form (2.9b) or parallel form (2.9c) reduces the sensitivity of the overall system to coefficient quantizations [4]. $H_i(z)$ and $H_j(z)$ are either first or second-order sections that correspond to cascade and parallel forms, respectively. The realization of a second-order section using the direct form 2 is depicted in Fig. 2.2.

The delay operator z^{-1} is used to transform (2.9a) into the difference equation form

$$y(n) = \sum_{k=0}^{N} b_k x(n-k) + \sum_{k=1}^{N} a_k y(n-k) \qquad (2.10)$$

This representation is most useful from the realization point of view since it explicitly provides an algorithm for the computation of the present value for the output. Also, (2.10) specifies a computational requirement that is common to all digital filter algorithms, which is the computation of one (vector) or several (matrix) linear combinations or inner products.

Another useful representation of discrete-time systems is the state variable representation where

$$\begin{bmatrix} x(n+1) \\ \hline y(n) \end{bmatrix} = \left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right] \begin{bmatrix} x(n) \\ \hline u(n) \end{bmatrix} \tag{2.11a}$$

(2.11b)

and u, x, and y are the input, state, and output vectors, respectively; A is an N x N matrix, and B, C, and D are matrices of appropriate dimensions [42]. The transfer function can be easily obtained by solving (2.11a) for X(z) in terms of U(z) and substituting the result in (2.11b), i.e.

$$X(z) = (Iz-A)^{-1}BU(z) \tag{2.12}$$

and

$$Y(z) = CX(z) + DU(z) \tag{2.13a}$$

$$= (C(Iz-A)^{-1}B + D)U(z) \tag{2.13b}$$

$$= H(z)U(z) \tag{2.13c}$$

where I is an N x N identity matrix. A non-singular transformation of the state variables as in

$$\tilde{x}(n) = P^{-1}x(n) \tag{2.14a}$$

$$\tilde{A} = P^{-1}AP \tag{2.14b}$$

$$\tilde{B} = P^{-1}B \tag{2.14c}$$

$$\tilde{C} = CP \tag{2.14d}$$

$$\tilde{D} = D \tag{2.14e}$$

where P is non-singular, leads to a digital structure with different nonlinear properties while leaving the linear in-

put-output relationship the same. A transformation of special interest is one that results in $\tilde{A}$ becoming the companion matrix [43] for the transfer function in (2.9a), i.e.

$$\tilde{A} = \begin{bmatrix} a_1 & a_2 & \cdots & a_N \\ 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & & & \vdots \\ 0 & 0 & \cdots & 0 \end{bmatrix} \qquad (2.15a)$$

$$\tilde{B} = (1 \quad 0 \quad \cdots \quad 0)^T \qquad (2.15b)$$

$$\tilde{C} = (b_o a_1 + b_1 \quad \cdots \quad b_o a_N + b_N) \qquad (2.15c)$$

$$\tilde{D} = b_o \qquad (2.15d)$$

The resulting digital network is referred to as the direct form 2 and has the canonic number of delays [4]. Example of a second-order network is shown in Fig. 2.2.

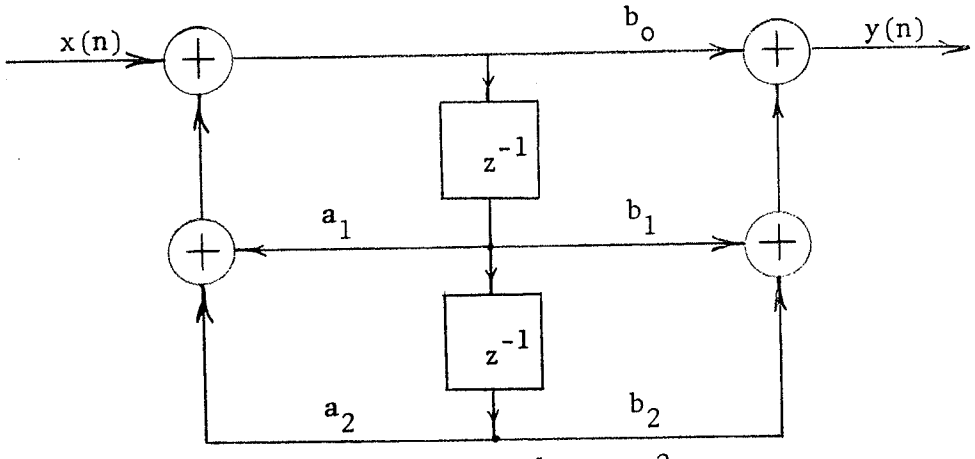


Figure 2.2: Block diagram representation of the direct form 2 second-order section

2.3 IMPLEMENTATION OF DIGITAL FILTERS

As mentioned in the previous section a requirement that is common to all digital filters is the computation of an inner product of the form

$$y = \sum_{j=1}^{M} a_j x_j \tag{2.16}$$

where y can either be the next state or output signal, x_j is a vector of present states and input signals, and a_j are the filter coefficients. The conventional method of realizing (2.16) uses a multiplier-based structure [5]. In this approach, a hardware multiplier or a multiply routine computes the products $a_j x_j$ which are then rounded to the alloted number of bits and added to the accumulator that ultimately contains the result $\tilde{y}$ ($\tilde{y}$ is different from y due to quantization effects). This method may suffer from excessive roundoff noise accumulation since in the computation of (2.16) M quantizations are performed. However, in the case where the digital structure is fixed and the filter coefficients a_j are changed to effect a different response, the multiplier-based implementation is still preferred.

There are two popular methods of formulating the computation in (2.16) such that the result is computed with full precision and thereafter an appropriate truncation is performed. These methods are based on the concept of distributed arithmetic. Such computational units are amenable to large scale integration (LSI) implementation due to the mod-

ularity of the computing algorithm [40]. Also, overflows can be easily detected and corrected for.

2.3.1 Stored-Product or Distributed Arithmetic Algorithm

This algorithm was developed independently by Croisier et. al. [35] and Peled and Liu [36]. Its derivation stems from the representation of x_j using 2's complement arithmetic, i.e.,

$$x_j = -x_{jo} + \sum_{k=1}^{B-1} x_{jk} 2^{-k} \tag{2.17}$$

where x_{jo} is the sign bit and $|x_j|<1$. Substituting (2.17) into (2.16) and interchanging the order of summations yields

$$y = \sum_{k=1}^{B-1} \left[\sum_{j=1}^{M} a_j x_{jk} \right] 2^{-k} - \sum_{j=1}^{M} a_j x_{jo} \tag{2.18a}$$

$$= \sum_{k=1}^{B-1} F_k 2^{-k} - F_o \tag{2.18b}$$

$$= ((..(0+F_{B-1})/2 + F_{B-2})/2+...+F_1)/2-F_o \tag{2.18c}$$

where F_k is a function of M binary valued variables which derive from signal bit values of equal significance. Since x_{jk} are either 0 or 1, F_k has 2^M possible values which for a constant coefficient set can be conveniently stored, hence the name stored-product, in a read-only-memory (ROM), or in a random-access-memory (RAM). Thus, the M-bit argument of F_k is used as the address that decodes the memory to produce the function value F_k which is then added to the shifted

value of the accumulator, as shown in Fig. 2.3. The two operations of memory decoding and accumulation are pipelined to speedup the overall computation. The computation time is mainly dependent on the wordlength (B bits in 2.18a-c) of the variables x_j and is independent of the number of terms in the linear combination in (2.16). However, M must be limited to a reasonable number, typically 8-10, due to the exponential growth of the storage requirements. The required wordlength in the ROM depends on the max $\{F_k\}$. Large wordlength in the ROM is not only costly in terms of storage but also causes a long carry propagation time in the adder/subtracter.

The restrictions of small M and small coefficient wordlength can be circumvented by properly partitioning (2.16). For large M, the summation in (2.16) can be broken up into a series of summantions with a smaller number of terms each of which can be computed separately. For high coefficient wordlength, partitioning of $F_k = F_{k1} + 2^{-p} F_{k2}$ can be employed where the wordlengths of F_{k1} and F_{k2} are acceptable. The problem of optimum partitioning with respect to M and the coefficent wordlength has been addressed in [38].

A drawback of the stored-product method is that for a coefficient set $\{a_j\}$ that varies, all the function values F_k must be reevaluated. Also, for systems described by a matrix equation, each inner product (row equation) must be evaluated separately, hence no saving in the overall storage requirement is possible.

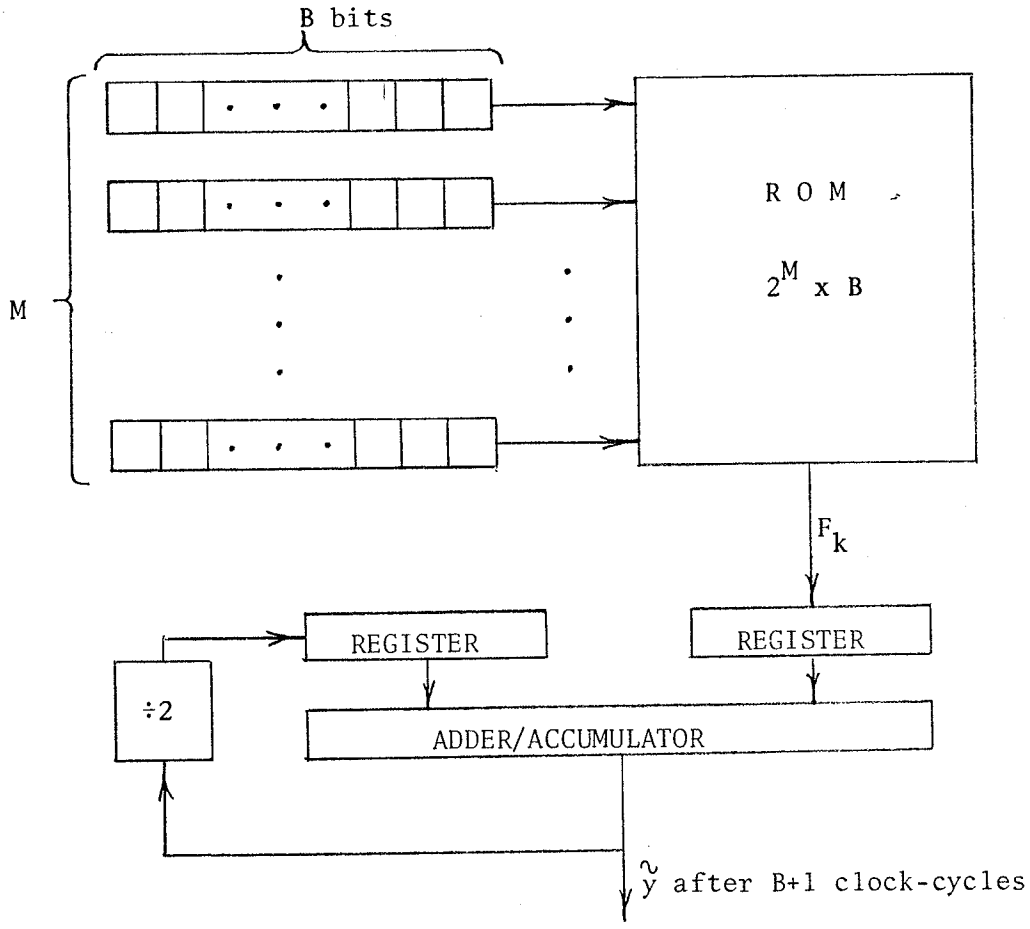


Figure 2.3: Block diagram representation of the stored-product algorithm

2.3.2 The Shift/Add Algorithm

Another method of evaluating the inner product with full precision is the shift/add algorithm. This algorithm was developed by Moon and Martens [33], and can also be classified as a distributed arithmetic algorithm. In the stored-product algorithm the distribution is performed with respect to the variables x_j, and in the shift/add algorithm with respect to the coefficients a_j. The concept of the shift/add

algorithm derives from the decomposition of the coefficients a_j in (2.16) using the binary series expansion, followed by the application of the canonical signed-digit code (CSDC) to minimize the number of non-zero entries in the series, i.e.,

$$a_j = \sum_{k=0}^{B} a_{jk} 2^{-k} \quad , \quad j=1,2,\ldots,M \tag{2.19}$$

where, for convenience, $|a_j|<1$, $a_{jk} \in \{-1,0,1\}$, and the number of non-zero a_{jk} is a minimum [44]. The application of CSDC is very important since, as will be shown, it drastically reduces the number of non-zero additive combinations of the variables x_j actually required, as well as the number of adders needed to perform the shift/add sequence using a hardware implementation. Substituting (2.19) in (2.16) and interchanging the order of summations yields

$$y = \sum_{k=0}^{B} \left[\sum_{j=1}^{M} a_{jk} x_j \right] 2^{-k} \tag{2.20}$$

For ease of presentation, we define

$$D_k = \sum_{j=1}^{M} a_{jk} x_j \quad , \quad k=0,1,\ldots,B \; ; \tag{2.21}$$

Substituting (2.21) into (2.20) gives

$$y = \sum_{k=0}^{B} D_k 2^{-k} \tag{2.22a}$$

$$= ((..(0+D_B)/2+D_{B-1})/2+\ldots+D_1)/2+D_0 \tag{2.22b}$$

The designation "shift/add" becomes apparent by examining (2.22b), however, the stored-product algorithm shares the

same property, as shown by (2.18c). Thus, the shift/add algorithm consists of: (1) computation of D_k, k=0,1,...,B, which are additive (subtractive) combinations of the variables x_k, j=1,2,...,M, given by (2.21); (2) a sequence of shift and add operations applied to the combinations D_k, given by (2.22a,b).

The combinations D_k are realized by a network of interconnected 2-input adders, or in a subroutine format by 2-input additions. As a result of the 2-input restriction, a reduction in the number of adders can be achieved by exploiting the occurrence of common partial sums in the D_k. An algorithm that, in most cases, drastically reduces the overall number of adders has been presented in [45], and is based on the consecutive application of a search for and removal of the most common partial sum remaining in the combinations D_k. Also, for systems that must compute multiple inner products, as in matrix multiplication, there is a possibility of existence of a segment of a particular shift/add sequence that is common to some other shift/add sequence. In such a case, tapping can be utilized in reducing the overall computational requirement (# of adders as well as the # of shifts).

Chapter III

DESIGN OF WAVE DIGITAL FILTERS

In the previous chapter we have briefly described the traditional approach to the design of digital filters. In this chapter we present the concept of wave digital filtering which was introduced by Fettweis [18] in 1971. WD filters imitate the properties of low-sensitivity analog networks. The process of translating the analog prototype into the corresponding discrete-time structure is based on using voltage waves for signals. These ensure that delay-free loops are eliminated and that discrete-time equivalents of the analog elements and their interconnections are simple. In Sec.3.2 the n-port adaptor approach, derived by Martens and Meerkötter [29], is described along with the reflection-free property [21] which is needed to ensure that no delay-free paths exist due to the interconnection of adaptors. Design examples of basic adaptors that simulate parallel, series, and 3rd-order elliptic topologies are derived using the n-port adaptor approach.Next, some general properties of WD networks are presented from which linear stability as well as sufficient conditions for guaranteeing nonlinear stability are deduced. Canonic WD filters are obtained by using the reactive redundancy removal procedure developed by

Ashley [30], and the removal of redundant capacitive loops is discussed in detail. The chapter concludes with the presentation of the exact diagonalization procedure. The 3rd-order elliptic ladder topology is used to show that corresponding to the resulting diagonal reference conductance matrix there is a canonic (number of reactive elements equals the order of the network) analog prototype.

3.1 INTRODUCTION TO WAVE DIGITAL FILTERS

WD filters are derived from analog prototype networks. For reasons of low sensitivity to element variations and the availability of extensive design tables, the analog prototype used is the doubly-terminated lossless reciprocal network displayed in Fig.3.1.

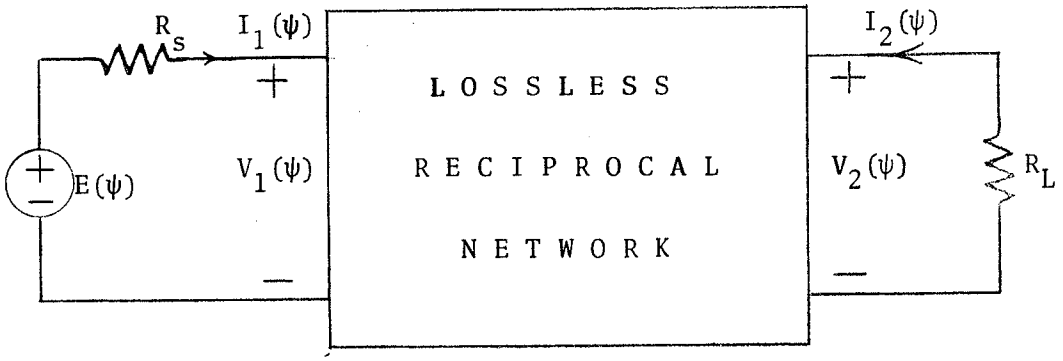


Figure 3.1: Doubly-terminated lossless reciprocal analog prototype.

The lossless and reciprocal part of the network in Fig.3.1 consists of an interconnection of inductances, capacitances, and ideal transformers. The overall network is passive,

hence stable, due to the resistive source and load ports [49]. Translation of the analog prototype into the discrete-time filter involves mapping, via the bilinear z-transformation, the analog elements and their interconnections into the corresponding discrete-time equivalents. Fettweis [18] has shown that using voltages and currents as signal carrying quantities is not sufficient to ensure freedom from delay-free paths in the discrete-time structure. The problem is circumvented by utilizing voltage waves for signals which are defined as follows:

$$a(t) \triangleq v(t) + Ri(t) \tag{3.1a}$$

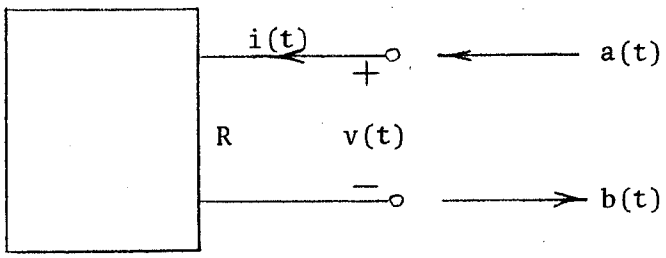
$$b(t) \triangleq v(t) - Ri(t) \tag{3.1b}$$

and in the frequency domain

$$A(\psi) \triangleq V(\psi) + RI(\psi) \tag{3.1c}$$

$$B(\psi) \triangleq V(\psi) - RI(\psi) \tag{3.1d}$$

where a(t) and b(t) are referred to as the incident and reflected voltage waves, respectively, and R is an arbitrary port reference resistance. The references of v(t) and i(t) with respect to an arbitrary port are shown below.



Setting $R=R_s$ for the source port and $R=R_L$ for the load port in Fig.3.1, we obtain using the given references and (3.1)

$$A_1(\psi) = E(\psi) \tag{3.2a}$$

$$B_1(\psi) = 2V_1(\psi) - E(\psi) \tag{3.2b}$$

$$A_2(\psi) = 0 \tag{3.2c}$$

$$B_2(\psi) = 2V_2(\psi) \tag{3.2d}$$

It is now easy to show that the voltage transfer function $T(\psi)$ and the voltage wave transfer function $W(\psi)$ are equal but for a frequency independent constant, i.e.

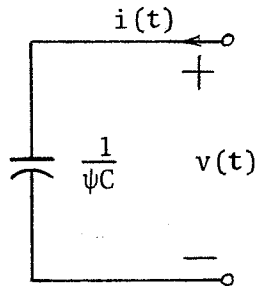
$$\begin{aligned} W(\psi) &= B_2(\psi)/A_1(\psi) \\ &= 2V_2(\psi)/E(\psi) \\ &= 2T(\psi) \end{aligned} \tag{3.3}$$

To derive the discrete-time equivalents of the analog elements we use the bilinear z-transformation

$$z = (1 + \psi)/(1 - \psi) \tag{3.4}$$

In general, the port reference resistance R is chosen so that the discrete-time equivalents have simple block diagram representations. To achieve this, we set R equal to R, L, 1/C for resistive, inductive, and capacitive ports (branches),respectively, and obtain the following discrete-time equivalents:

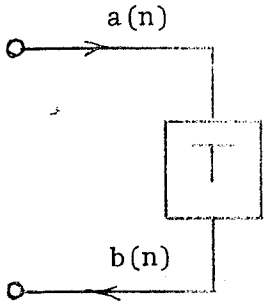
Capacitance



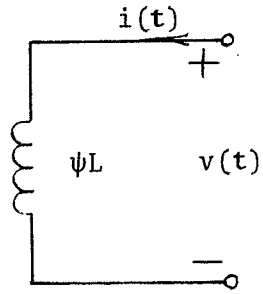
$I=\psi CV \rightarrow A=V(1+\psi)$, $B=V(1-\psi)$

$B/A=(1-\psi)/(1+\psi)= z^{-1}$

$b(n) = a(n-1)$



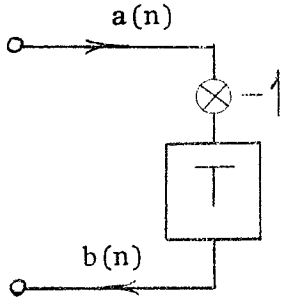
Inductance



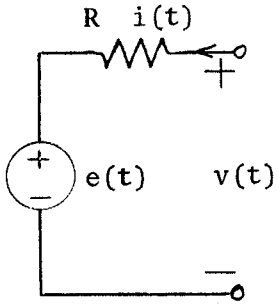
$V=\psi LI \rightarrow A=LI(1+\psi)$, $B=LI(\psi-1)$

$B/A=-(1-\psi)/(1+\psi) = -z^{-1}$

$b(n) = -a(n-1)$



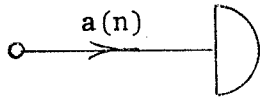
Resistance

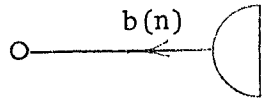


$V=E+RI \rightarrow A=2V-E$, $B = E$

$a(n) = 2v(n) - e(n)$

$b(n) = e(n)$





For purely resistive ports we set $e(n)=0$.

To obtain a complete WD structure we must also have the discrete-time equivalents that simulate the interconnections of the prototype ports. These equivalents are called adap-

tors, since at an interconnection, the voltage waves must be adapted so that Kirchhoff's current (KCL) and voltage (KVL) laws are satisfied. In the next section we derive an overall n-port adaptor that simulates the topological constraints for the entire network. In contrast to this approach, Fettweis et. al. [18]-[19],[23] choose to construct ladder WD filters using low-order adaptors that simulate parallel and series interconnection of at most three ports. This approach has the advantage of generating multiplier coefficients for the adaptors that are the actual design parameters. Consequently, discrete optimization can be performed with respect to these parameters to minimize the overall computational requirement [46]-[47]. A disadvantage, however, is that not all prototype topologies can be simulated using low-order parallel and series adaptors, e.g. bridge-tee networks [29] and Brune networks [48]. No topological restrictions exist for designing WD filters using the n-port adaptor approach.

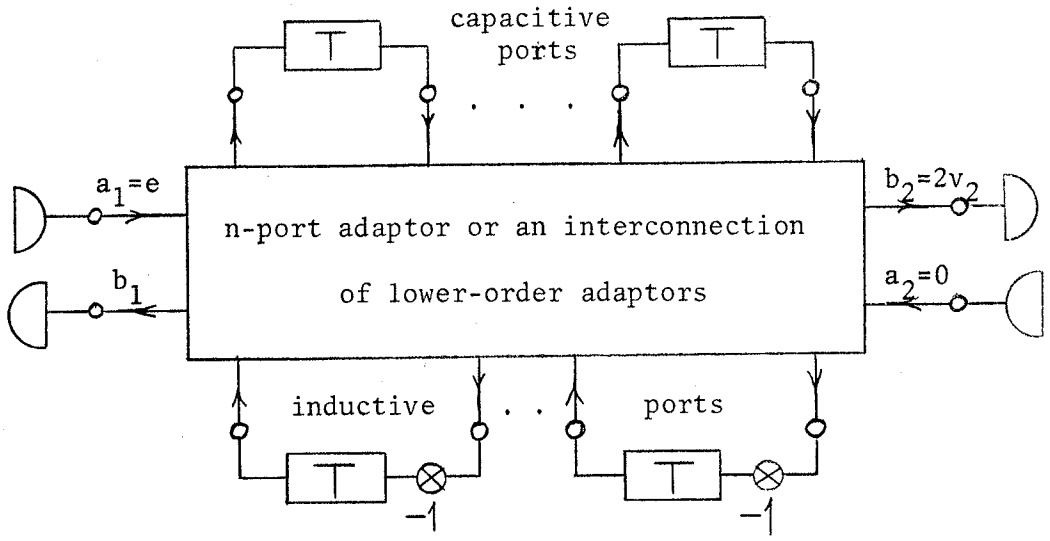


Figure 3.2: Discrete-time equivalent of the doubly-terminated lossless reciprocal analog prototype

The analog prototype network in Fig.3.1 together with the discrete-time equivalents derived above translate into the corresponding discrete-time structure, as shown in Fig.3.2.

3.2 DERIVATION OF THE N-PORT ADAPTOR REPRESENTATION

WD n-port adaptors are designed by deriving the n-port voltage scattering matrix representation for the corresponding analog prototype [29], i.e.

$$b = S\,a \tag{3.5}$$

where b and a are the reflected and incident voltage-wave vectors, respectively, and S is an nxn constant voltage-wave scattering matrix. With reference to the analog prototype, we partition the available ports into ℓ link ports and t tree ports, such that $\ell+t=n$. The current and voltage vectors i and v can now be expressed as the linear combinations of link current and tree voltage vectors i_ℓ and v_t, i.e.

$$i = B^T i_\ell \tag{3.6}$$

$$v = Q^T v_t \tag{3.7}$$

From Tellegen's theorem (due to KVL and KCL)

$$v^T i = 0 \tag{3.8}$$

we have together with (3.6,7)

$$QB^T = 0 \tag{3.9}$$

The incident and reflected voltage wave vectors are

$$a = v + Ri$$
$$b = v - Ri \tag{3.10}$$

where R is a diagonal matrix of positive port resistances. Substituting (3.6,7) into (3.10), we obtain

$$a = Q^T v_t + RB^T i_\ell$$
$$b = Q^T v_t - RB^T i_\ell \tag{3.11}$$

Premultiplying (3.11) by QG, where $G=R^{-1}$ is the diagonal matrix of positive port conductances, we obtain

$$QGa = QGQ^T v_t + QB^T i_\ell$$
$$QGb = QGQ^T v_t - QB^T i_\ell \tag{3.12}$$

Solving for v_t by using (3.9) yields

$$v_t = Y^{-1}QGa$$
$$= Y^{-1}QGb \tag{3.13}$$

where by definition

$$Y \triangleq QGQ^T \tag{3.14}$$

is the positive definite symmetric node admittance matrix [49]. From (3.10) we have

$$a + b = 2v \tag{3.15a}$$

$$= 2Q^T v_t \tag{3.15b}$$

$$= 2Q^T Y^{-1} QGa \tag{3.15c}$$

$$= 2Q^T Y^{-1} QGb \tag{3.15d}$$

where appropriate substitutions using (3.7,13) were made. Solving (3.15c) for b yields

$$b = [\, 2Q^T Y^{-1} QG - U \,]\, a \triangleq S\, a \tag{3.16}$$

where S is the desired voltage scattering matrix, and U is a unit matrix of appropriate dimensions(a designation used throughout). Similarly, we can solve for a using (3.15d) and obtain

$$a = [\, 2Q^T Y^{-1} QG - U \,]\, b = S\, b \tag{3.17}$$

Substituting (3.17) into (3.16) yields

$$b = S^2\, b \tag{3.18}$$

which for an arbitrary non-zero vector b implies that

$$S^2 = U \quad \text{or} \quad S = S^{-1} \tag{3.19,20}$$

Using (3.16), the scattering matrix representation for an arbitrary topology can be obtained if the fundamental cut-set matrix Q and the port reference conductance matrix G are known. This approach, however, involves the operation of matrix inversion which complicates the procedure of obtaining binary fractions as the final entries in the S matrix[50]. More managable expressions for S can be derived by first expressing Q, B, and G in the partitioned forms, i.e.

$$Q = [\, N \quad U \,] \tag{3.21a}$$

$$B = [\, U \quad -N^T \,] \tag{3.21b}$$

$$G = \begin{bmatrix} G_\ell & 0 \\ 0 & G_t \end{bmatrix} \tag{3.21c}$$

where N is a matrix of turns-ratios of an ideal transformer multiport network which reduces to the non-unit part of the fundamental cut-set matrix for a network which is free of ideal transformers (i.e. wire interconnections only). Substituting (3.21) into (3.16) yields

$$\left[\begin{array}{c} b_\ell \\ \hline b_t \end{array}\right] = \left[\begin{array}{c|c} 2N^T Y^{-1} N G_\ell - U & 2N^T Y^{-1} G_t \\ \hline 2Y^{-1} N G_\ell & 2Y^{-1} G_t - U \end{array}\right] \left[\begin{array}{c} a_\ell \\ \hline a_t \end{array}\right] \tag{3.22}$$

and into (3.14), we have

$$Y = G_t + N G_\ell N^T \tag{3.23}$$

To consolidate matters, we define

$$K \triangleq Y^{-1} N G_\ell = [\, G_t + N G_\ell N^T \,]^{-1} N G_\ell \tag{3.24}$$

from which, using (3.23), we obtain

$$\begin{aligned} Y^{-1}G_t &= U - Y^{-1}NG_\ell N^T \\ &= U - KN^T \end{aligned} \tag{3.25}$$

Substituting (3.24,25) into (3.22), we obtain the various expressions for the scattering matrix S [29,48]:

$$S = \begin{bmatrix} 2N^TK-U & 2N^T[U-KN^T] \\ 2K & U-2KN^T \end{bmatrix} \tag{3.26a}$$

$$= \begin{bmatrix} -U & N^T \\ 0 & U \end{bmatrix} \begin{bmatrix} -U & 0 \\ -2K & U \end{bmatrix} \begin{bmatrix} -U & N^T \\ 0 & U \end{bmatrix} \triangleq F\,T\,F \tag{3.26b}$$

$$= \begin{bmatrix} U-N^TK & N^T \\ -K & U \end{bmatrix} \begin{bmatrix} -U & 0 \\ 0 & U \end{bmatrix} \begin{bmatrix} U & -N^T \\ K & U-KN^T \end{bmatrix} \triangleq M\Lambda M^{-1} \tag{3.26c}$$

where (3.26c) displays the eigenvalues and the eigenvectors of S, and F and T are self-inverse. Clearly, using (3.26), the problem of obtaining the scattering matrix representation is reduced to obtaining the matrices N and K.

The matrix N can be obtained directly from the oriented graph which is derived from the network topology. For multiport networks that contain ideal transformers it is usually simpler to solve for N using

$$i_t = -N\, i_\ell \quad \text{or} \quad v_\ell = N^T v_t \qquad (3.27a,b)$$

The network interpretation of K is obtained as follows:

1. Terminate all of the tree ports in their reference resistances, i.e. $a_t=0$ and $b_t=2v_t$.
2. Terminate all of the link ports in their reference resistances in series with a voltage source, i.e. $a_\ell=e_\ell$, where e_ℓ denotes the link voltage source vector.

Substituting the above conditions into (3.26) yields

$$v_t = K\, e_\ell \qquad (3.28)$$

which specifies K as a voltage transfer matrix that contains the constants required in expressing tree port voltages as linear combinations of the link port voltage sources. Using the resistively terminated prototype, the symbolic solutions for the constants can be obtained by utilizing any suitable network analysis techniques (usually Thevenin's Theorem and superposition suffice). The number of entries in K is $t\ell$ which is usually greater, except in some special cases, than the number of degrees of freedom (for n-ports containing ideal transformers the number of degrees of freedom is equal

to n-1 plus the number of non- trivial turns-ratios). Consequently, if a canonic solution is desired where the number of design parameters is equal to the number of degrees of freedom, then the entries in K cannot be defined as the design parameters. The canonic solution yields entries in K that are functions of the independent design parameters which are defined in the course of solving (3.28). Furthermore, if the functions are of the sum of products (SOP) form, then quantization of the design parameters to binary fractions is sufficient to ensure that all the entries in N and K, and consequently S, are also binary fractions (entries in N are 0's, 1's, -1's, and turns-ratios which are part of the independent design parameter set). The SOP requirement imposes a restriction on the possible independent design parameter sets that can be defined.

3.2.1 Reflection-free Property

In many instances it is advantageous with respect to the overall computational requirement to separate the n-port adaptor into an interconnection of lower-order adaptors. In order to effect this separation, it is important to examine the problem of interconnecting two adaptors, as shown in Fig.3.3.

To make the interconnecting ports compatible, i.e. $b_i=a_j$ and $a_i=b_j$, it is easy to show that $R_i=R_j$ is required. Furthermore, we must ensure that the delay-free loop created by the

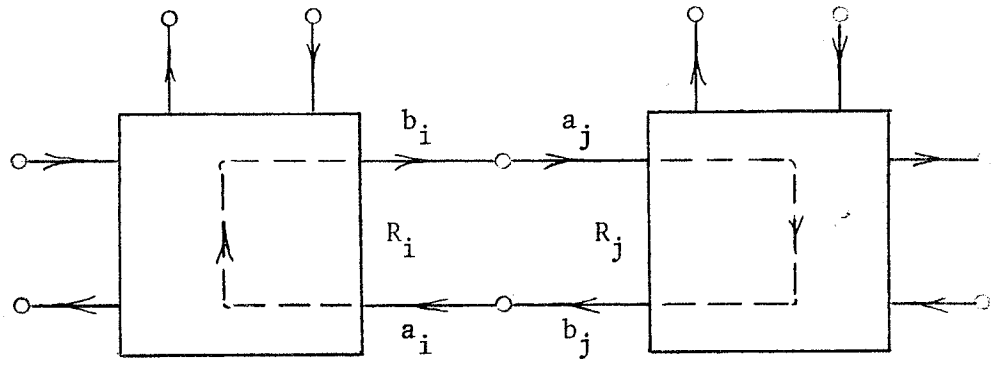


Figure 3.3: Delay-free path created by adjacent adaptors

interconnection is broken up so that the structure is computable [22]. One solution to this problem is to insert extra delays in the path, however, a more practical solution exists which restricts the value of the common reference resistance to only two choices [21]. Depending upon which choice is made, either of the two ports can be made reflection-free, i.e. the reflected wave at that port becomes independent of the incident wave. With reference to Fig.3.3, if we select port i to be reflection-free, then the value of R_i is derived as follows:

1. Terminate all the remaining ports in their reference resistances, i.e. $a_k=0$ $k=1,2,..,i-1,i+1,..,n$.
2. The reflected wave b_i is now only dependent on a_i, i.e. $b_i=(v_i-R_i i_i)/(v_i+R_i i_i)a_i$.
3. To make b_i independent of a_i, the coefficient relating the two waves must be set to zero, i.e. $(v_i-R_i i_i)/(v_i+R_i i_i)=0$.

4. Solving for R_i, we obtain $R_i = v_i/i_i$.

Thus, an arbitrary port can be made reflection-free by setting the reference resistance equal to the driving point resistance looking into that port when all other ports are terminated in their reference resistances. The majority of ports are terminated with the discrete-time equivalents of the analog elements. Consequently, their reference resistances are obtained as shown in Sec.3.1.

Using the n-port adaptor approch, port i can be made reflection-free by setting the corresponding diagonal entry in the S matrix equal to zero, i.e. $s_{ii}=0$. Clearly, this procedure will ensure that b_i is independent of a_i. Using (3.26a), the condition $s_{ii}=0$ corresponds to setting

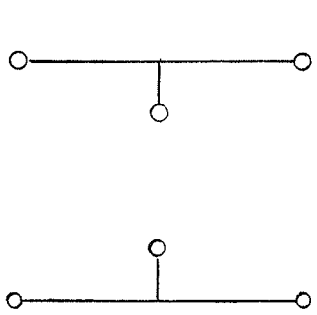
$$\sum_{j=1}^{t} n_{ij}k_{ji} = \frac{1}{2} \quad , \quad \sum_{j=1}^{\ell} k_{ij}n_{ij} = \frac{1}{2} \qquad (3.29a,b)$$

for a reflection-free link and tree port, respectively. In (3.29), n_{ij} and k_{ij} are entries of N and K matrices, respectively. It can be shown that the conditions specified by (3.29) are in fact equivalent to setting the reference resistance of the appropriate port equal to the driving point resistance at that port. Also, the dependence relationship in (3.29) reduces the number of degrees of freedom for that subnetwork by one. This ensures that the total number of degrees of freedom is still canonic.

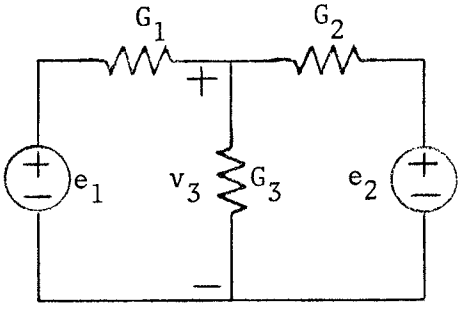
3.2.2 Illustrative Examples

To illustrate the general procedure we consider the design of parallel and series adaptors using the n-port adaptor approach. These adaptors are used in the WD synthesis of ladder prototype networks. In the third example, a 3rd order elliptic lowpass filter is designed according to Fettweis's procedure using the elementary adaptors as well as using the n-port approach.

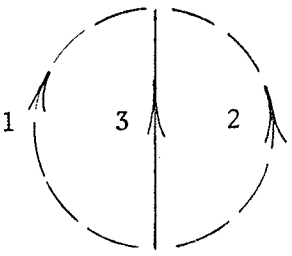
Example#1 3-port parallel adaptor



3-port parallel connection



resistively terminated network for solving $v_t = Ke_\ell$



oriented-graph for obtaining N

$$\alpha_1 = 2G_1/(G_1+G_2+G_3)$$

$$\alpha_2 = 2G_2/(G_1+G_2+G_3)$$

$$v_3 = [\ \alpha_1/2 \quad \alpha_2/2\ ] \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} = K\, e_\ell$$

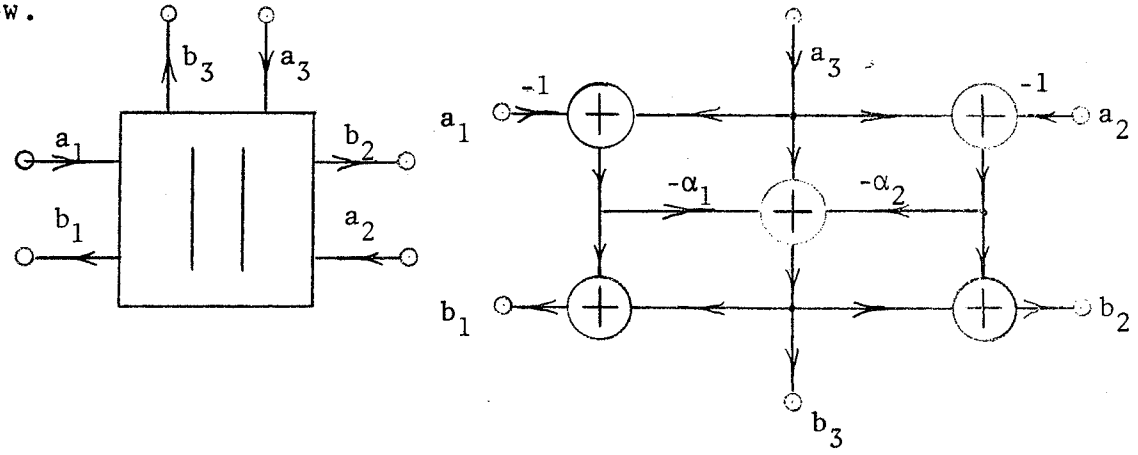
$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} [\ v_3\ ] = N^T v_t$$

Using (3.26b)

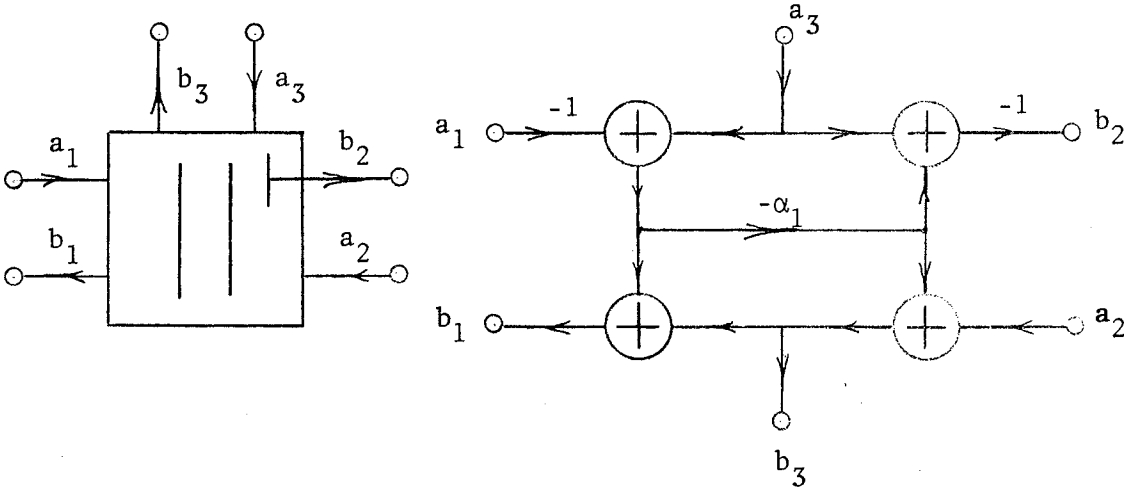
$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} -1 & 0 & 1 \\ 0 & -1 & 1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ -\alpha_1 & -\alpha_2 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 & 1 \\ 0 & -1 & 1 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

$$= \begin{bmatrix} \alpha_1 - 1 & \alpha_2 & 2 - \alpha_1 - \alpha_2 \\ \alpha_1 & \alpha_2 - 1 & 2 - \alpha_1 - \alpha_2 \\ \alpha_1 & \alpha_2 & 1 - \alpha_1 - \alpha_2 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

The symbolic representation and the corresponding signal-flow diagram for the 3-port parallel adaptor are shown below.

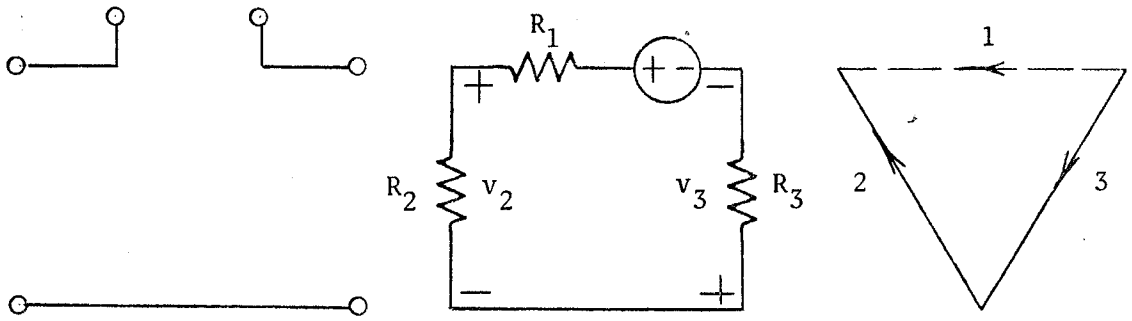


If we choose port#2 as reflection-free, then we have $G_2=G_1+G_3$, $\alpha_2=1$, and as expected $s_{22}=0$. This ensures the independence of b_2 of a_2. The symbolic representation and the corresponding signal-flow diagram are shown below.



The general 3-port parallel adaptor requires 6 additions and 2 multiplications, whereas the reflection-free design requires 4 additions and 1 multiplication [23].

Example#2 3-port series adaptor



$$\alpha_1 = 2R_2/(R_1+R_2+R_3)$$

$$\alpha_2 = 2R_3/(R_1+R_2+R_3)$$

$$\begin{bmatrix} v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} \alpha_1/2 \\ \alpha_2/2 \end{bmatrix} [\, e_1 \,] = K\, e_\ell$$

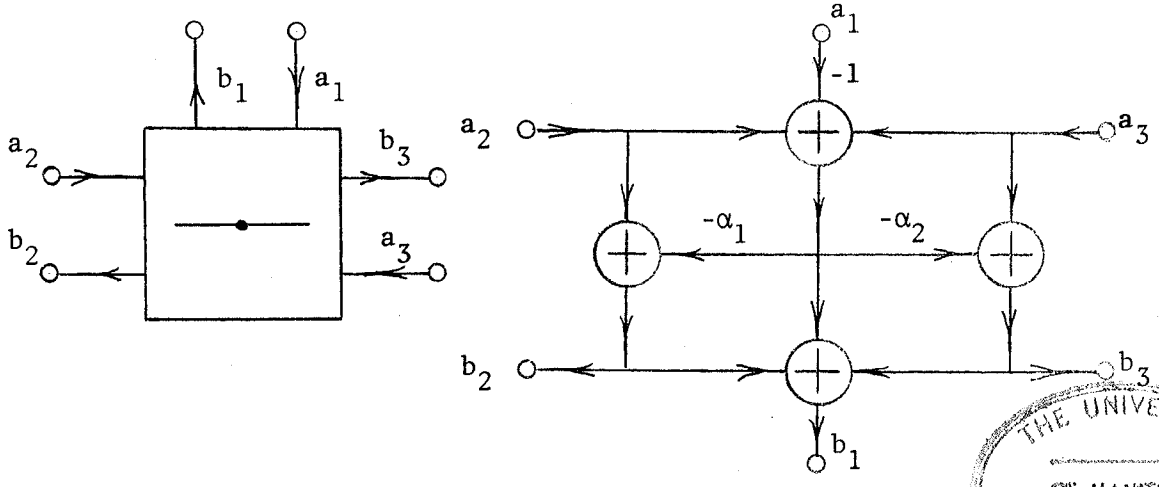
$$v_1 = [\, 1 \;\; 1 \,] \begin{bmatrix} v_2 \\ v_3 \end{bmatrix} = N^T v_t$$

Using (3.26b)

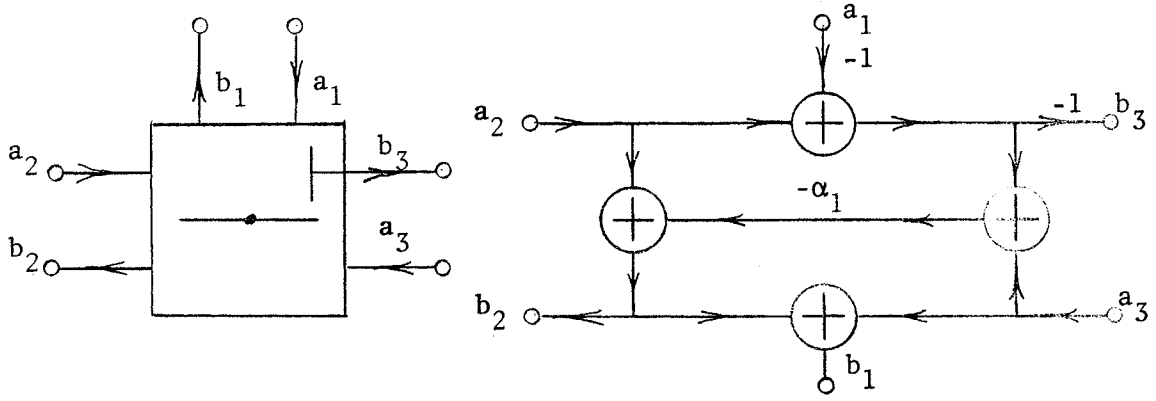
$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} -1 & 1 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 & 0 \\ -\alpha_1 & 1 & 0 \\ -\alpha_2 & 0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 1 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

$$= \begin{bmatrix} \alpha_1 + \alpha_2 - 1 & 2 - \alpha_1 - \alpha_2 & 2 - \alpha_1 - \alpha_2 \\ \alpha_1 & 1 - \alpha_1 & -\alpha_1 \\ \alpha_2 & -\alpha_2 & 1 - \alpha_2 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

The symbolic representation and the corresponding signal-flow diagram for the 3-port series adaptor are shown below.



If we choose port#3 as reflection-free, then we have $R_3=R_1+R_2$, $\alpha_2=1$, and as expected $s_{33}=0$. This ensures the independence of b_3 of a_3. The symbolic representation and the corresponding signal-flow diagram are shown below.



The general 3-port series adaptor requires 6 additions and 2 multiplications, whereas the reflection-free design requires 4 additions and 1 multiplication. Also, the series adaptor can be derived from the parallel adaptor and vice versa by the application of a procedure called flow-graph reversal or transposition, as described in [23].

Example#3 3rd-order elliptic lowpass filter

As our final example, we present the design of a WD filter based on a 3rd-order elliptic lowpass prototype, as depicted in Fig. 3.4. The WD structure shown in Fig.3.4c was derived using the discrete-time equivalents of the analog elements and the parallel and series adaptors from examples #1 and #2. The numbering of ports in Fig. 3.4c corresponds to the individual adaptors.

The overall computational requirement includes 18 additions, 5 multiplications, and 3 negations, where 2 additions

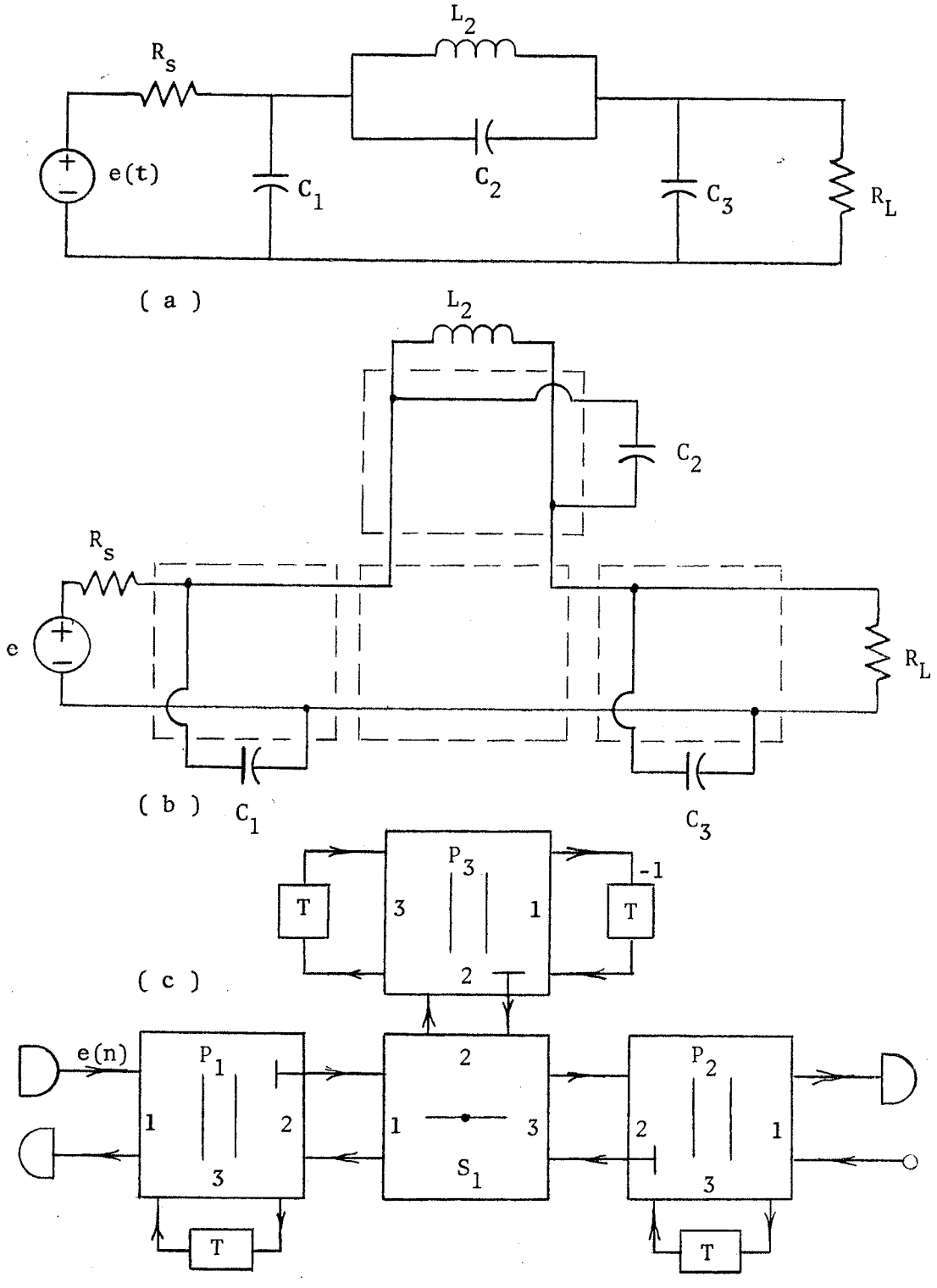


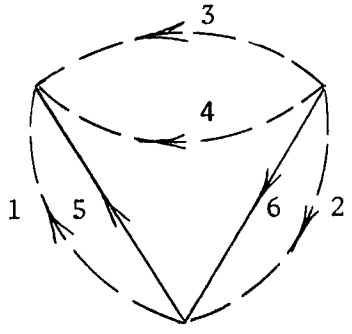
Figure 3.4: The 3rd-order elliptic prototype and the corresponding WD structure.

can be eliminated by using the fact that the incident wave at the output port is equal to zero and the computation of the reflected wave at the input port is optional. The distribution of reflection-free ports in Fig.3.4c imposes a particular sequence of operations to be followed in the computation of the required signals, i.e.:

1. The reflected waves at ports #2 of adaptors P1, P2, and P3 are computed.
2. The reflected waves at all ports of adaptor S1 are computed.
3. The reflected waves at ports #1 and #3 of adaptors P1, P2, and P3 are finally computed.

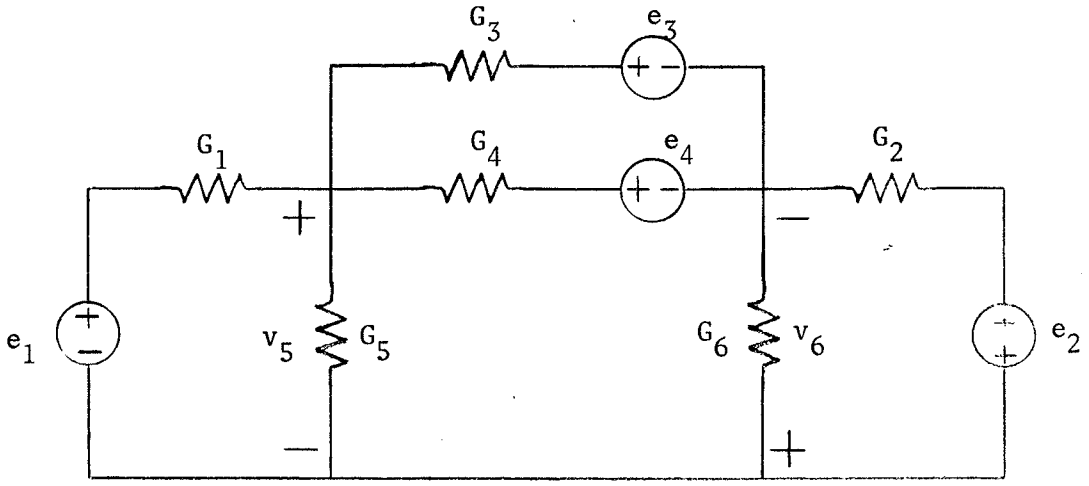
As a rule, the adaptor without the reflection-free port should be located in the centre of the structure in order to reduce the longest computational path.

To derive the n-port adaptor we need to obtain the N and K matrices. To obtain N we use the oriented graph shown below:



$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} v_5 \\ v_6 \end{bmatrix} = N^T v_t$$

To determine the K matrix we use the resistively terminated network shown below.



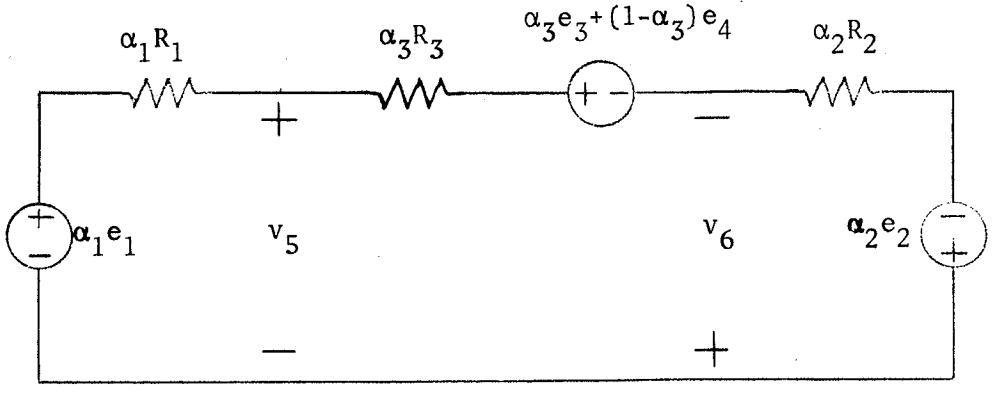
Let

$$\alpha_1 = \frac{G_1}{G_1 + G_5} \quad , \quad \alpha_2 = \frac{G_2}{G_2 + G_6} \quad , \quad \alpha_3 = \frac{G_3}{G_3 + G_4}$$

where, with respect to Fig.3.4a, we have

$G_1 = 1/R_s$, $G_2 = 1/R_L$, $G_3 = C_2$, $G_4 = 1/L_2$, $G_5 = C_1$, $G_6 = C_3$

Applying Thevenin's Theorem to the above network results in a simplified network shown below:



Let

$$\alpha_4 = \frac{\alpha_1 R_1}{\alpha_1 R_1 + \alpha_2 R_2 + \alpha_3 R_3} \quad , \quad \alpha_5 = \frac{\alpha_2 R_2}{\alpha_1 R_1 + \alpha_2 R_2 + \alpha_3 R_3} \quad , \quad R_i = \frac{1}{G_i}$$

and we obtain using the simplified network

$$\begin{bmatrix} v_5 \\ v_6 \end{bmatrix} = \begin{bmatrix} \alpha_1(1-\alpha_4) & -\alpha_2\alpha_4 & \alpha_3\alpha_4 & (1-\alpha_3)\alpha_4 \\ -\alpha_1\alpha_5 & \alpha_2(1-\alpha_5) & \alpha_3\alpha_5 & (1-\alpha_3)\alpha_5 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \end{bmatrix}$$

$$= K\, e_\ell$$

The N and K matrices are combined according to (3.26) to obtain the 6-port S matrix. Note that the entries in K are functions of the independent parameter set $\{ \alpha_i \}_{i=1}^{5}$ and are in the required sum of products form.

3.3 STABILITY OF WAVE DIGITAL FILTERS

In this section we examine some important properties of WD networks. Since WD networks are derived from stable analog networks via the bilinear z-transformation it follows that the resulting WD filters are also stable. In this section we use Lyapunov's direct method [51] in deducing linear and nonlinear stability of WD networks. Sufficient conditions are presented for ensuring suppression of zero-input parasitic oscillations. These results serve as a summary and were originally presented by Fettweis and Meerkötter [26]; the presentation here follows, in part, Ashley [30].

Linear WD n-port networks are said to be pseudolossless since the instantaneous pseudopower, defined by

$$p(n) = v^T(n)i(n) \tag{3.30a}$$

$$= (a^T(n)Ga(n) - b^T(n)Gb(n))/4 \tag{3.30b}$$

which is absorbed by the WD n-port at time t=nT, is equal to zero [20]. This result is derived from Tellegen's theorem. For linear n-port adaptors we also have

$$b(n) = S\, a(n) \tag{3.31}$$

Hence, for pseudolossless n-port adaptors we obtain

$$0 = a^T(n)(G - S^TGS)a(n) \tag{3.32}$$

which must hold for an arbitrary incident voltage wave vector a(n), and therefore

$$G = S^TGS \tag{3.33}$$

Postmultiplying by S and using $S^2 = U$, we obtain

$$GS = S^TG \tag{3.34}$$

which states that linear WD n-ports are reciprocal with respect to the symmetric reference conductance matrix G [48]. The pseuodolossless and reciprocal properties hold for n-port adaptors that have been modified for realizability if the number of design parameters is canonic. The n-port adaptors proposed in this thesis are canonic as well as pseudolossless and reciprocal.

Before investigating the stability of linear WD networks, we first formulate the state-variable representation of WD systems. To achieve this, we partition the voltage-wave vectors according to reactive and resistive ports, i.e.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.35}$$

where b_1, a_1 correspond to delay-terminated ports and b_2, a_2 to input/ output ports. With respect to the n-port adaptor ports, we have at the delay-terminated ports

$$b_1 = zPa_1 \tag{3.36}$$

where P is a diagonal matrix with constant entries of 1's and -1's corresponding to capacitive and inductive ports in the prototype network, respectively. Substituting (3.36) into (3.35) yields

$$\begin{bmatrix} za_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} PS_{11} & PS_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3.37}$$

where we used $P=P^{-1}$. The corresponding state equations in the discrete-time domain are

$$\begin{bmatrix} a_1(n+1) \\ b_2(n) \end{bmatrix} = \begin{bmatrix} PS_{11} & PS_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \end{bmatrix} \tag{3.38}$$

where a_1, b_2, and a_2 are the state, output, and input vectors, respectively.

The zero-input stability of both linear and nonlinear WD filters can be investigated using Lyapunov's direct method [51]. For the system presently under consideration, we define the stored pseudopower as the Lyapunov function, i.e.

$$V(a_1) = a_1^T G_{11} a_1 \tag{3.39}$$

where $G=(G_{11} \dotplus G_{22})$ is partitioned conformably with a_1 and a_2. Using the pseudolossless property in (3.33), it is easy to show that from $t=nT$ onwards, the stored pseudopower defined by (3.39) is a nonincreasing function of time, i.e.

$$\Delta V(a_1) \triangleq V(a_1(n)) - V(a_1(n+1)) \tag{3.40a}$$
$$= a_1^T G_{11} a_1(n) - a_1^T(n+1) G_{11} a_1(n+1) \tag{3.40b}$$
$$= a_1^T(n) G_{11} a_1(n) - a_1^T(n) S_{11}^T P G_{11} P S_{11}^T a_1(n) \tag{3.40c}$$
$$= a_1^T(n)(G_{11} - S_{11}^T G_{11} S_{11}) a_1(n) \tag{3.40d}$$
$$= a_1^T(n) S_{21}^T G_{22} S_{21} a_1(n) \tag{3.40e}$$
$$= b_2^T(n) G_{22} b_2(n) \tag{3.40f}$$

Since G_{22} is positive definite, we have

$$\Delta V(a_1) \geq 0 \tag{3.41}$$

which is sufficient for stability in the sense of Lyapunov [51]. From (3.41) we have $\Delta V(a_1)=0$ for $b_2=0$, which for a non-zero state vector a_1 can only occur if the system is unobservable. Therefore, a pseudolossless linear WD system

is asymptotically stable, i.e. $\Delta V(A_1)>0$, if and only if it is observable. Ashley [30] has shown that reciprocal WD networks that are observable are also controllable, and therefore minimal (canonic in the number of delays). Thus, linear WD systems that are minimal are asymptotically stable in the sense of Lyapunov.

Lyapunov's stability test can be applied to nonlinear systems, where signals before the delays must be altered so as to satisfy the finite register length requirement, i.e. we compute $\tilde{a}_1(n+1)$ from $a_1(n+1)$ by applying a chosen nonlinear function. Also, a given nonlinear finite state WD system can be output stable, i.e. $\tilde{b}_2(n)=0$, but not completely stable, i.e. $\tilde{a}_1(n+1)\neq 0$. Fettweis and Meerkötter [26] used the concept of pseudopassivity, i.e. $\underline{G} \geq \underline{S}^T \underline{G} \underline{S}$, to derive a signal modification scheme that is sufficient for ensuring output stability. They also showed that if the WD system is canonic then complete stability for the nonlinear system is guaranteed. Ashley [30] has extended complete stability to include nonlinear WD systems that contain extra delays.

In general, a nonlinear finite state WD system is completely stable if it is derived from a linear WD system which is asymptotically stable and

$$V(\tilde{a}_1(n+1)) \leq V(a_1(n+1)) \tag{3.42}$$

If the linear system is stable, then

$$V(\tilde{a}_1(n+1)) < V(a_1(n+1)) \tag{3.43}$$

is sufficient [30]. For the case where G_{11} is diagonal and positive definite, we have

$$V(a_1) = a_1^T G_{11} a_1 = \sum_{i=1}^{M} g_{ii} a_{i1}^2 \qquad (3.44)$$

where M stands for the number of delays. Using (3.44), the conditions specified by (3.42,43) can be satisfied by choosing a nonlinear function which ensures that

$$|\tilde{a}_1(n+1)| \leq |a_1(n+1)| \quad , \quad |\tilde{a}_1(n+1)| < |a_1(n+1)| \qquad (3.45,46)$$

respectively. The signal modifications implied by (3.45,46) can be implemented by using the sign–magnitude truncation scheme. Using this scheme, the signals are truncated in magnitude to the nearest discrete value available in the register. In fixed-point 2's complement arithmetic, the above scheme is realized most economically by adding the sign bit to the least significant position in the register.

For the case where G_{11} is nondiagonal, (3.45) or (3.46) may no longer be sufficient for guaranteeing nonlinear stability. This situation occurs naturally when redundant delays are removed using Ashley's [30] procedure. This procedure produces minimal WD systems and is presented in the next section. To circumvent the problem of nondiagonal G_{11}, one possible solution is to diagonalize G_{11} at the expense of introducing new design parameters. In Chapter IV, we show that the method of redundancy removal followed by diagnalization of G_{11} is equivalent to transforming the nonmini-

mal analog prototype into a minimal network with ideal transformers. The solution to the problem of reducing the number of design parameters to the canonic number for some basic adaptors is also presented.

3.4 DESIGN OF CANONIC WAVE DIGITAL FILTERS.

In general, the number of delays in a WD filter is equal to the number of reactive elements in the analog prototype network. Consequently, if the analog prototype contains more reactive elements than the order of the filter (eg. ladder filters with finite attenuation poles), then the number of delays is greater than is necessary in the resulting WD structure. The excess delays are usually due to loops and/or cutsets of reactive elements and can be effectively removed by following a simple procedure developed by Ashley [30]. This procedure does not introduce additional multipliers,unlike the procedure developed by Fettweis [32] which cannot handle reactive cutsets without introducing additional multipliers. The redundancies most often encountered are due to capacitive loops (inductive cutsets for dual networks) and are the focus of this section.

The procedure derived by Ashley that removes all four types of reactive redundancies is based on the topological characterization of the reactive redundancies followed by the formulation of constraint equations from which one can deduce the form of the symbolic change of variables. The

analysis is performed with respect to the normal tree which contains, by definition, the maximum number of capacitive twigs and the minimum number of inductive twigs [52]. Kirchhoff's voltage law, when partitioned with respect to the normal tree, yields

$$\left[\begin{array}{ccc|ccc} U & 0 & 0 & -N_{CS}^T & 0 & 0 \\ 0 & U & 0 & -N_{CR}^T & -N_{GR}^T & 0 \\ 0 & 0 & U & -N_{CL}^T & -N_{GL}^T & -N_{\Gamma L}^T \end{array}\right] \left[\begin{array}{c} v_S \\ v_R \\ v_L \\ \hline v_C \\ v_G \\ v_\Gamma \end{array}\right] = 0 \qquad (3.47)$$

where the subscripts S,R,L,C,G and Γ denote link: capacitances, resistances, inductances; twig: capacitances, resistances and inductances, respectively. The capacitance-only loops, defined by the link capacitances S, appear explicitly in the first KVL equation, i.e.

$$\begin{aligned} 0 &= v_S - N_{CS}^T v_C && (3.48a) \\ &= a_S - N_{CS}^T \mathbf{a}_C + b_S - N_{CS}^T b_C && (3.48b) \\ &= (b_S - N_{CS}^T b_C)(z + 1) && (3.48c) \\ &= (a_S - N_{CS}^T a_C)(z^{-1} + 1) && (3.48d) \end{aligned}$$

where we used 2v=a+b, and for capacitive ports we have a=zb. Theoretically, the capacitive loops in the analog prototype can, under zero-input conditions, support a non-zero current at $\psi = \infty$. This undesirable mode maps, via the bilinear z-transformation, into the corresponding mode at z=-1 in the

WD network. Although this mode is unobservable and cannot be excited from the input ports, in the WD filter this mode, however, can be excited at power-up, i.e. when the states are initialized with random values. Consequently, an oscillation occurs due to the eigenvalue of -1 which drastically reduces the dynamic range of the filter.

From (3.48c,d) we have

$$\begin{aligned} a_S - N_{CS}^T a_C &= 0 \\ b_S - N_{CS}^T b_C &= 0 \end{aligned} \tag{3.49}$$

for $z \neq -1$. We now show that the effect of imposing the constraints in (3.49), via a similarity transformation, is to inhibit the excitation of modes at $z=-1$.

Since the only elements that can support a non-zero current at $\psi = \infty$ are the capacitances in the capacitance-only loops, then open-circuiting all the non-capacitive elements does not alter this current distribution. The fundamental loop equations for this subnetwork are given by (3.48a), and since the subnetwork is purely capacitive, the scattering matrix S given by (3.26) becomes the state-transition matrix with eigenvalues of 1 for capacitive cutsets and -1 for capacitive loops. We constrain the state vector a_{SC} using (3.49), i.e.

$$a_{SC} = \begin{bmatrix} a_S \\ a_C \end{bmatrix} = \begin{bmatrix} N_{CS}^T \\ U \end{bmatrix} a_C \tag{3.50}$$

The next state, $a_{SC}(n+1)$, for the constrained system is given by

$$\begin{aligned} a_{SC}(n+1) &= S\, a_{SC}(n) \\ &= \begin{bmatrix} -U & N_{CS}^T \\ 0 & U \end{bmatrix} \begin{bmatrix} -U & 0 \\ -2K_{CS} & U \end{bmatrix} \begin{bmatrix} -U & N_{CS}^T \\ 0 & U \end{bmatrix} \begin{bmatrix} N_{CS}^T \\ U \end{bmatrix} a_C(n) \\ &= \begin{bmatrix} N_{CS}^T \\ U \end{bmatrix} a_C(n) \\ &= a_{SC}(n) \end{aligned} \tag{3.51}$$

Clearly, the constrained system can only excite the modes that correspond to the eigenvalues equal to unity, and modes at z=-1 are suppressed. Imposing the same constraints in the original network will also suppress the modes at z=-1.

The constraints in (3.49) display the form of the non-singular transformation matrix which, without altering the transfer function from input to output, decouples the undesirable modes due to capacitance-only loops, i.e. let

$$T = \left[\begin{array}{ccc|ccc} U & 0 & 0 & N_{CS}^T & 0 & 0 \\ 0 & U & 0 & 0 & 0 & 0 \\ 0 & 0 & U & 0 & 0 & 0 \\ \hline 0 & 0 & 0 & U & 0 & 0 \\ 0 & 0 & 0 & 0 & U & 0 \\ 0 & 0 & 0 & 0 & 0 & U \end{array}\right] \tag{3.52}$$

which is partitioned according to (3.47). The new system is given by

$$\begin{aligned} T^{-1}b &= T^{-1}S\,T\,(\,T^{-1}a\,) \\ &\triangleq \tilde{S}\,\tilde{a} \\ &\triangleq \tilde{b} \end{aligned} \tag{3.53}$$

where

$$\begin{aligned} \tilde{a}_S &= a_S - N_{CS}^T\,a_C = 0 \\ \tilde{b}_S &= b_S - N_{CS}^T\,b_C = 0 \end{aligned} \tag{3.54}$$

and consequently, the rows and columns in $\tilde{S}$ that correspond to capacitive links can be deleted. This decreases the dimension of the system by the number of capacitive loops.

The pseudolossless property must also hold for the transformed system, i.e.

$$\tilde{G} = \tilde{S}^T\,\tilde{G}\,\tilde{S} \tag{3.55}$$

where it is easy to show that

$$\tilde{G} = T^T\,G\,T \tag{3.56}$$

Writing (3.56) in the partitioned form with the redundant rows and columns deleted yields

$$\tilde{G} = \left[\begin{array}{cc|cc} G_R & 0 & 0 & 0 \\ 0 & G_L & 0 & 0 \\ \hline 0 & 0 & G_C+N_{CS}G_SN_{CS}^T & 0 \\ 0 & 0 & 0 & G_G \end{array}\right] \qquad (3.57)$$

The nondiagonal part of the reduced $\tilde{G}$ matrix,

$$G_\xi \triangleq G_C + N_{CS}\, G_S\, N_{CS}^T \qquad (3.58)$$

is the node conductance matrix for the capacitive subnetwork discussed above.

Ashley [30] has shown that the application of the similarity transformation in (3.53) followed by the deletion of the redundant rows and columns in the $\tilde{S}$ matrix is equivalent to deleteting the capacitive link columns in the original N and K matrices. Therefore, the reduced system is characterized by

$$\tilde{N} = \begin{bmatrix} N_{CR} & N_{CL} \\ N_{GR} & N_{GL} \end{bmatrix}, \quad G_\ell = \begin{bmatrix} G_R & 0 \\ 0 & G_L \end{bmatrix}, \quad G_t = \begin{bmatrix} G_\xi & 0 \\ 0 & G_G \end{bmatrix} \qquad (3.59)$$

$$\tilde{K} = [\, G_t + \tilde{N}\, G_\ell\, \tilde{N}^T \,]^{-1}\, \tilde{N}\, G_\ell$$

If the analog prototype contains redundancies which are only due to capacitive loops then the corresponding WD network described by (3.59) is minimal.

3.5 DIAGONALIZATION OF THE REFERENCE CONDUCTANCE MATRIX G

The sufficient conditions, given by (3.45,46), for guaranteeing nonlinear stability are applicable to systems with a diagonal reference conductance matrix G. The procedure of removing redundant delays due to capacitive loops in the prototype produces a nondiagonal symmetric reference conductance matrix. Ashley [30] has shown that it is possible to diagonalize G, given by (3.57), via a congruence transformation, i.e.

$$\hat{G} = W^T G W \tag{3.60}$$

where $\hat{G}$ is diagonal and positive definite. The G matrix in (3.57) is block diagonal with respect to the link and tree ports. Consequently, W is also block diagonal and (3.60) can be partitioned accordingly;

$$\hat{G}_\ell = W_\ell^T G_\ell W_\ell \quad , \quad \hat{G}_t = W_t^T G_t W_t \tag{3.61a,b}$$

where

$$G = \begin{bmatrix} G_\ell & 0 \\ 0 & G_t \end{bmatrix} , \quad \hat{G} = \begin{bmatrix} \hat{G}_\ell & 0 \\ 0 & \hat{G}_t \end{bmatrix} , \quad W = \begin{bmatrix} W_\ell & 0 \\ 0 & W_t \end{bmatrix} \tag{3.62a,b,c}$$

The scattering matrix that corresponds to $\hat{G}$ is obtained by applying a similarity transformation to the reduced S matrix, i.e. from the pseudolossless property we have

$$
\begin{aligned}
W^T G W &= \left(W^T S^T W^{-1^T} \right)\left(W^T G W \right)\left(W^{-1} S\, W \right) \\
&= \hat{S}^T\, \hat{G}\, \hat{S} \\
&= \hat{G}
\end{aligned}
\tag{3.63}
$$

and

$$
\hat{S} = W^{-1}\, S\, W \tag{3.64}
$$

Using (3.26), it was shown in [41] that

$$
\hat{N}^T = W_\ell^{-1}\, N^T\, W_t \quad , \quad \hat{K} = W_t^{-1}\, K\, W_\ell \tag{3.65,66}
$$

To diagonalize G, we apply a sequence of elementary column and row operations that clear out the off-diagonal terms. Consequently, W can be expressed as a product of these elementary operators, i.e.

$$
W = W_1\, W_2 \, . \, . \, . \, W_k \tag{3.67}
$$

where an elementary column (row) operator is defined by [43]

$$
W_i = \begin{bmatrix}
1 & 0 & . & . & . & 0 & 0 \\
0 & 1 & . & . & . & 0 & 0 \\
. & . & 1 & -\gamma_i & . & . & \\
. & . & 0 & 1 & . & . & \\
0 & 0 & . & . & . & 1 & 0 \\
0 & 0 & . & . & . & 0 & 1
\end{bmatrix} \tag{3.68}
$$

To diagonalize G, we let

$$
\gamma_i = g_{ij}/g_{ii} \tag{3.69}
$$

where $G=\{g_{ij}\}_{nxn}$. The operation GW_i yields a zero for the entry ij, and since G is symmetric, the operation $W_i^T G$ yields a zero for the ji entry. The upper bound on the number of elementary column operations required is one half the number of the off-diagonal terms. The operator W_i^T is also a valid elementary column operator and can be used instead of W_i. The inverse of W_i is obtained by replacing γ_i with $-\gamma_i$.

To illustrate the procedure, consider Example#3 in Sec.3.2.2. The single capacitive loop in Fig.3.4a is characterized by

$$N_{CS} = \begin{bmatrix} 1 \\ \\ 1 \end{bmatrix}$$

Using (3.58), we obtain

$$G_\xi = \begin{bmatrix} G_5 & 0 \\ 0 & G_6 \end{bmatrix} + \begin{bmatrix} 1 \\ \\ 1 \end{bmatrix} [\, G_4 \,][\, 1 \quad 1 \,]$$

$$= \begin{bmatrix} G_4 + G_5 & G_4 \\ G_4 & G_4 + G_6 \end{bmatrix} = G_t$$

The 2 off-diagonal terms can be removed by applying a single elementary column operation followed by the corresponding row operation. The diagonalization can be effected in 2 ways:

(1)
$$\hat{G}_t = \begin{bmatrix} 1 & 0 \\ \\ -\gamma_1 & 1 \end{bmatrix} \begin{bmatrix} G_5 + G_4 & G_4 \\ G_4 & G_4 + G_6 \end{bmatrix} \begin{bmatrix} 1 & -\gamma_1 \\ 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} G_4 + G_5 & 0 \\ 0 & G_6 + G_4(1-\gamma_1) \end{bmatrix}, \quad \gamma_1 = \frac{G_4}{G_4 + G_5}$$

$$(2)\qquad \hat{G}_t = \begin{bmatrix} 1 & -\gamma_2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} G_4 + G_5 & G_4 \\ G_4 & G_4 + G_6 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -\gamma_2 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} G_5 + G_4(1-\gamma_2) & 0 \\ 0 & G_4 + G_6 \end{bmatrix}, \quad \gamma_2 = \frac{G_4}{G_4 + G_6}$$

and, as assumed from the outset, no inductive redundancies are present, thus $W_\ell = U$ and $\hat{G}_\ell = G_\ell$.

The canonic set of design parameters, $\{\alpha_i\}_{i=1}^{5}$, was defined in Sec.3.2.2. It follows that γ_1 and γ_2 are dependent and can be expressed as functions of α_i, i.e

$$\gamma_1 = \frac{G_4}{G_4 + G_5} = \frac{(1-\alpha_3)\alpha_4}{(1-\alpha_3)\alpha_4 + (1-\alpha_1)(1-\alpha_4-\alpha_5)}$$

$$\gamma_2 = \frac{G_4}{G_4 + G_6} = \frac{(1-\alpha_3)\alpha_5}{(1-\alpha_3)\alpha_5 + (1-\alpha_2)(1-\alpha_4-\alpha_5)}$$

In general, the approximation of $\{\alpha_i\}_{i=1}^{5}$ to binary fractions does not yield binary fractions for γ_1 and γ_2. However, it suffices to redefine the independent parameter set such that all dependencies are expressable as sums of products of the independent parameters. The solutions for various basic adaptors using this approach are presented in Chapter IV.

The diagonalization procedure yields a diagonal reference conductance matrix $\hat{G}$, as well as the transformed $\hat{N}$ and $\hat{K}$ ma-

trices. Based on these and the transformed voltage-wave variables, it is possible to construct the corresponding minimal analog prototype [53]. For the present example, we obtain using γ_1 and (3.65)

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 1 \end{bmatrix}}_{W_t} \underbrace{\begin{bmatrix} 1 & -\gamma_1 \\ 0 & 1 \end{bmatrix}}_{} \underbrace{\begin{bmatrix} 1 & \gamma_1 \\ 0 & 1 \end{bmatrix}}_{W_t^{-1}} \begin{bmatrix} v_5 \\ v_6 \end{bmatrix}$$

$$= \begin{bmatrix} 1 & -\gamma_1 \\ 0 & 1 \\ 1 & 1-\gamma_1 \end{bmatrix} \begin{bmatrix} v_5 + \gamma_1 v_6 \\ v_6 \end{bmatrix} = \hat{N}^T \hat{v}_t$$

The corresponding analog network with a minimal number of reactive elements is depicted in Fig.3.5. The minimal property is achieved at the expense of introducing an additional design parameter, namely the ideal transformer turns-ratio γ_1.

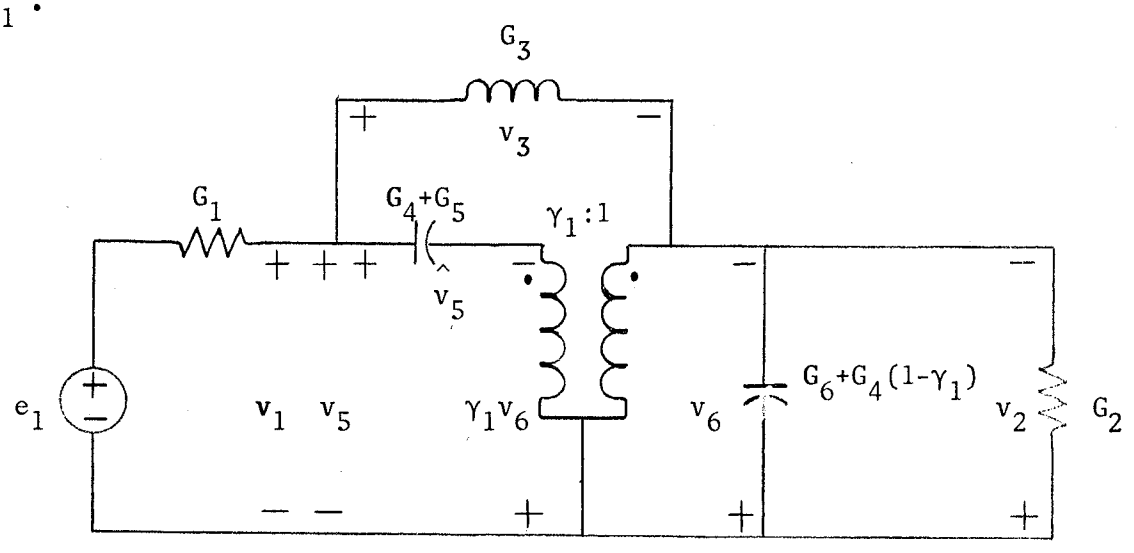


Figure 3.5: 3rd-order elliptic filter with a minimal number of reactive elements.

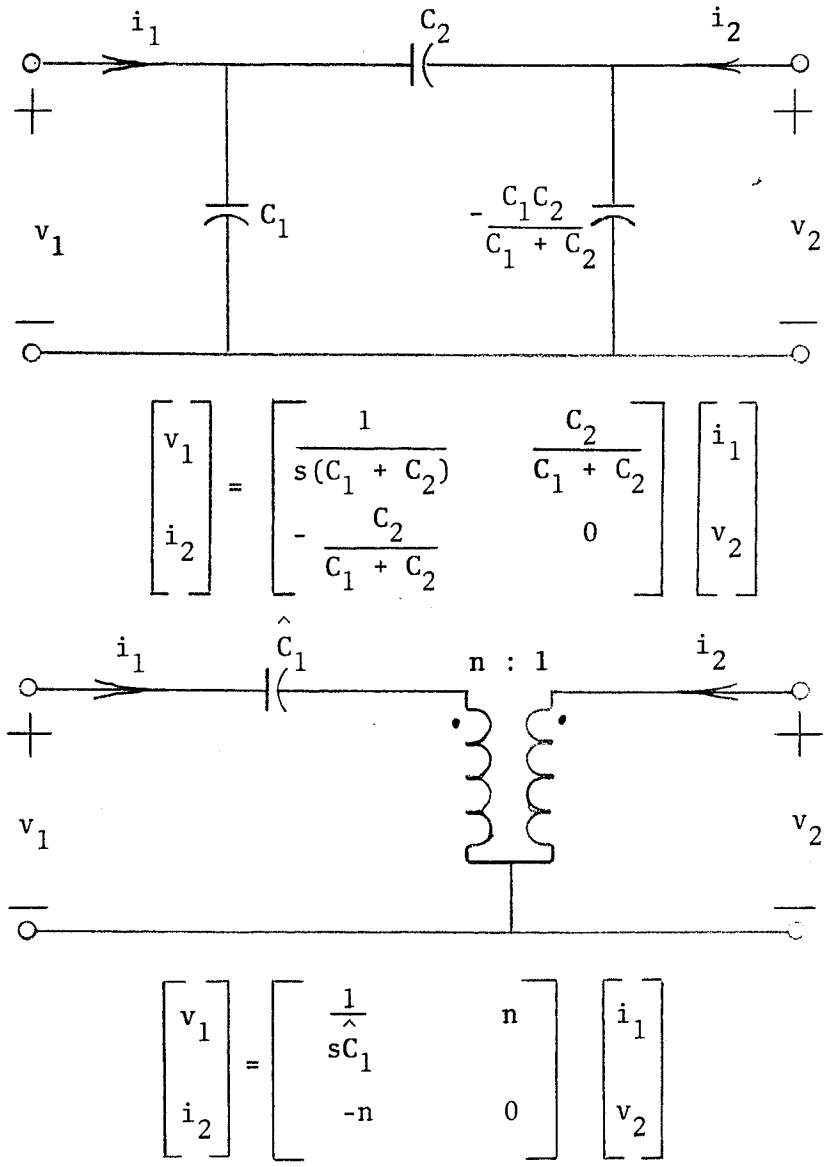
Chapter IV

DESIGN OF BASIC CANONIC ADAPTORS

Dependent parameters arising either from the diagonalization process or from the solution of the K matrix are rational functions of the independent parameters. This chapter presents designs of basic canonic adaptors where the independent set of parameters has been redefined such that the entries in K and N matrices are expressed as sums of products (SOP) of the independent parameters. This is sufficient to ensure that subsequent quantization of the independent parameters to binary fractions produces an S matrix with binary fractions for entries. Solutions presented are for the Brune, 3rd and 5th order elliptic topologies. Also presented are simplified designs with a reduced number of degrees of freedom due to the imposition of certain element constraints.

4.1 GENERAL RESULTS

The network equivalence shown in Fig.4.1 can be used in eliminating capacitive loops from nonminimal analog networks. Application of this network equivalence to the network in Fig. 3.4 produces the minimal network shown in Fig. 3.5. Thus, the process of redundancy removal followed by diagonalization is equivalent to generating the minimal prototype via the network equivalence in Fig.4.1.



The above networks are equivalent if:

$$\hat{C}_1 = C_1 + C_2 \quad , \quad n = \frac{C_2}{C_1 + C_2}$$

$$\frac{C_1 C_2}{C_1 + C_2} = C_1 n = C_2 (1 - n)$$

Figure 4.1: Network equivalence used in generating minimal analog prototypes.

The design of WD n-port adaptors usually begins with the partitioning of the available ports into link and tree ports such that

$$v_\ell = N^T v_t \quad , \quad v_t = K e_\ell \qquad (4.1a,b)$$

At the outset, however, it is not clear how to partition the available ports. Certain choices may lead to a simplified solution. Until a particular tree is chosen, solutions to (4.1) cannot be obtained. One can, however, derive a general voltage transfer matrix by terminating every port with a resistance in series with a voltage source. Consequently,

$$b = 2v - e \quad , \quad a = e \qquad (4.2a,b)$$

and using b=Sa, we obtain

$$v = \frac{1}{2}(S + U)e \qquad (4.2c)$$

$$\triangleq Le \qquad (4.2d)$$

where $L=\{ \ell_{ij} \}_{nxn}$ is the overall voltage transfer matrix. Once a choice for a tree is made, then

$$L = \begin{bmatrix} N^T K & N^T(U - KN^T) \\ K & U - KN^T \end{bmatrix} \qquad (4.3a)$$

$$= \begin{bmatrix} -U & N^T \\ 0 & U \end{bmatrix} \begin{bmatrix} 0 & 0 \\ -K & U \end{bmatrix} \begin{bmatrix} -U & N^T \\ 0 & U \end{bmatrix} \qquad (4.3b)$$

$$= \frac{1}{2} F (T + U) F \qquad (4.3c)$$

where links are numbered first, and F and T were defined in (3.20b). A particular advantage in using the L matrix is the ease with which one can obtain the dependence relation which results from choosing port m reflection-free. Using (3.29), we obtain

$$\ell_{mm} = \frac{1}{2} \tag{4.4}$$

as the required condition. Another advantage in deriving L is the visibility of certain parameter constraints that, if implemented, reduce significantly the complexity of the overall design.

4.2 DESIGN OF THE BRUNE ADAPTOR

Consider the Brune section shown in Fig. 4.2. Many analog ladder networks can be transformed using the network equivalence in Fig.4.1 into minimal networks that contain Brune sections. To solve v=Le we use the appropriately terminated network shown in Fig.4.3. Using the given references, the fundamental loop equations become

$$v_1 + v_2 = v_3 \tag{4.5a}$$

$$v_1 + nv_2 = v_4 \tag{4.5b}$$

The Brune section has 4 ports, any 2 of which can be chosen as the tree-ports. Consequently, there are 6 possible partitionings. These are derived using the loop equations and are given below:

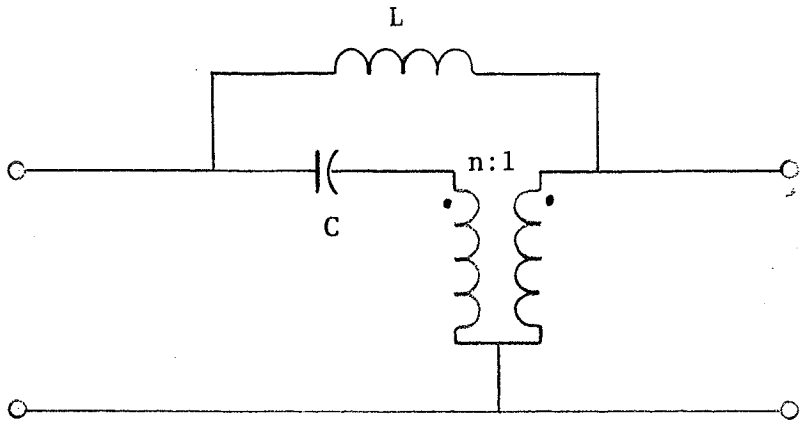


Figure 4.2: The Brune section.

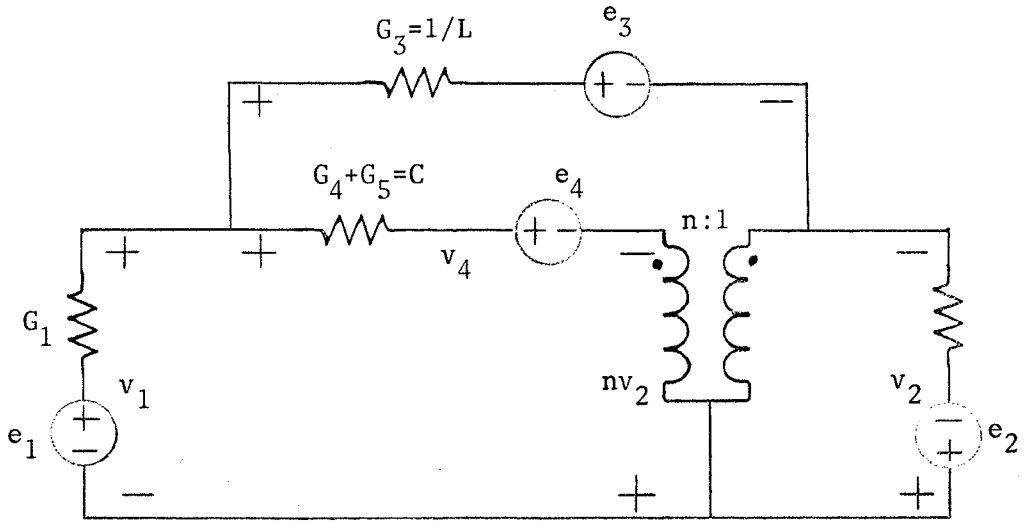


Figure 4.3: Resistively terminated Brune section.

$$
\begin{aligned}
&(1)\ \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \frac{-n}{1-n} & \frac{1}{1-n} \\ \frac{1}{1-n} & \frac{-1}{1-n} \end{bmatrix} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} \qquad (2)\ \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & n \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \\
&(3)\ \begin{bmatrix} v_1 \\ v_3 \end{bmatrix} = \begin{bmatrix} -n & 1 \\ 1-n & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ v_4 \end{bmatrix} \qquad (4)\ \begin{bmatrix} v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ 1-n & n \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \end{bmatrix} \qquad (4.6) \\
&(5)\ \begin{bmatrix} v_1 \\ v_4 \end{bmatrix} = \begin{bmatrix} -1 & 1 \\ n-1 & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ v_3 \end{bmatrix} \qquad (6)\ \begin{bmatrix} v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} \frac{-1}{n} & \frac{1}{n} \\ \frac{n-1}{n} & \frac{1}{n} \end{bmatrix} \begin{bmatrix} v_1 \\ v_4 \end{bmatrix}
\end{aligned}
$$

where

$$n = \frac{G_4}{G_4 + G_5} \tag{4.6a}$$

is the ideal transformer turns ratio. To circumvent the problem of working with ideal transformers, we apply the network equivalence to Fig.4.3, except that capacitances are replaced by conductances. The resulting ladder network is shown in Fig.4.4.

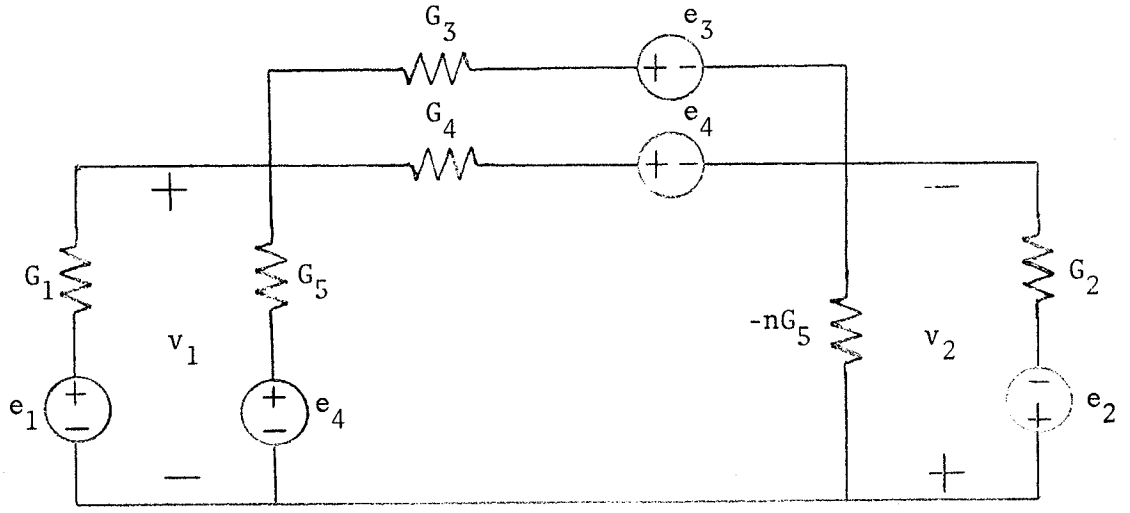


Figure 4.4: The ladder network used to derive the L matrix for the Brune section.

To obtain the L matrix it is sufficient to solve only for v_1 and v_2 in terms of e_i, i=1,2,3,4. The remaining voltages are obtained using (4.5). Let

$$\alpha_1 = \frac{G_1}{G_1 + G_5} \quad , \quad \alpha_2 = \frac{G_2}{G_2 - nG_5} \quad , \quad \alpha_3 = \frac{G_3}{G_3 + G_4} \tag{4.7,8,9}$$

Using Thevenin's theorem and the above, we obtain the simplified network shown in Fig. 4.5.

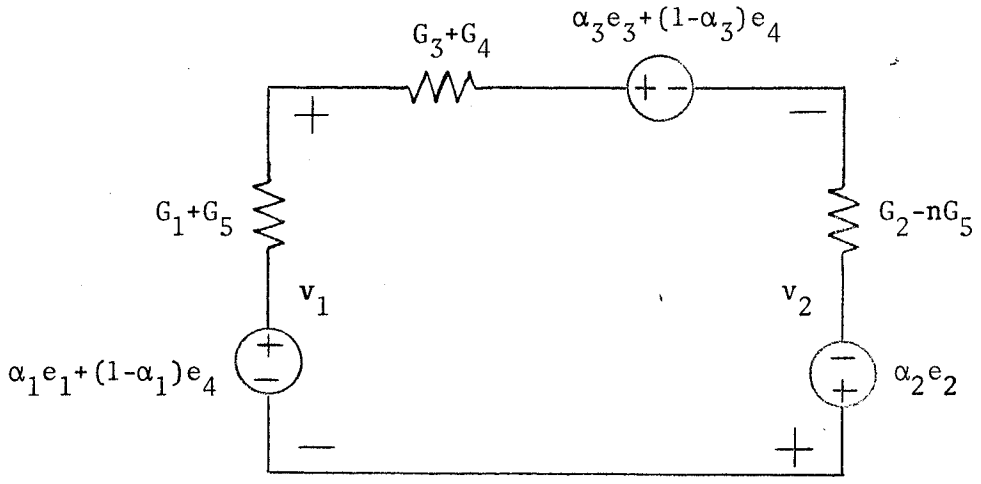


Figure 4.5: Simplified resistive network.

Furthermore, let

$$\alpha_4 = \frac{1}{1 + \frac{G_1 + G_5}{G_3 + G_4} + \frac{G_1 + G_5}{G_2 - nG_5}} \qquad \alpha_5 = \frac{1}{1 + \frac{G_2-nG_5}{G_3+ G_4} + \frac{G_2-nG_5}{G_1+ G_5}} \qquad (4.10,11)$$

Using these and Fig. 4.5, we obtain

$$v_1 = \alpha_4[\alpha_3e_3 + (1-\alpha_3)e_4 - \alpha_2e_2] + (1-\alpha_4)[\alpha_1e_1+(1-\alpha_1)e_4] \qquad (4.12)$$

$$v_2 = \alpha_5[\alpha_3e_3+(1-\alpha_3)e_4-\alpha_1e_1-(1-\alpha_1)e_4] + (1-\alpha_5)\alpha_2e_2 \qquad (4.13)$$

and together with (4.5) we obtain

$$L=\begin{bmatrix} \alpha_1(1-\alpha_4) & -\alpha_2\alpha_4 & \alpha_3\alpha_4 & 1-\alpha_1+\alpha_4(\alpha_1-\alpha_3) \\ -\alpha_1\alpha_5 & \alpha_2(1-\alpha_5) & \alpha_3\alpha_5 & \alpha_5(\alpha_1-\alpha_3) \\ \alpha_1(1-\alpha_4-\alpha_5) & \alpha_2(1-\alpha_4-\alpha_5) & \alpha_3(\alpha_4+\alpha_5) & 1-\alpha_1+(\alpha_4+\alpha_5)(\alpha_1-\alpha_3) \\ \alpha_1(1-\alpha_4-n\alpha_5) & \alpha_2(n(1-\alpha_5)-\alpha_4) & \alpha_3(\alpha_4+n\alpha_5) & 1-\alpha_1+(\alpha_4+n\alpha_5)(\alpha_1-\alpha_3) \end{bmatrix} \quad (4.14)$$

The L matrix is used in conjunction with one of the choices in (4.6) in deriving the corresponding K matrix. Let

$$\{\ 1\ ,\ 2\ ,\ 3\ ,\ 4\} <=> \{i\ ,\ j\ ,\ m\ ,\ n\} \quad (4.15)$$

then, if i and j are link ports, we have

$$\begin{bmatrix} v_i \\ v_j \end{bmatrix} = N^T \begin{bmatrix} v_m \\ v_n \end{bmatrix}\ ,\quad \begin{bmatrix} v_m \\ v_n \end{bmatrix} = \begin{bmatrix} \ell_{mi} & \ell_{mj} \\ \ell_{ni} & \ell_{nj} \end{bmatrix} \begin{bmatrix} e_i \\ e_j \end{bmatrix} \quad (4.16)$$

where $L=\{\ \ell_{ij}\ \}_{2x2}$. As an example, if we choose ports 1 and 3 as link ports (choice #3 in (4.6)), then

$$\begin{bmatrix} v_1 \\ v_3 \end{bmatrix} = \begin{bmatrix} -n & 1 \\ 1-n & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ v_4 \end{bmatrix}\ ,\quad \begin{bmatrix} v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} -\alpha_1\alpha_5 & \alpha_3\alpha_5 \\ \alpha_1(1-\alpha_4-n\alpha_5) & \alpha_3(\alpha_4+n\alpha_5) \end{bmatrix} \begin{bmatrix} e_1 \\ e_3 \end{bmatrix} \quad (4.17a,b)$$

In the process of solving eqn. (4.2) we have defined $\{\ \alpha_i\ \}_{i=1}^{5}$. With n, as an additional parameter, the total number of parameters is 6. The independent set can only contain 4 (# of ports - 1 plus the # of nontrivial turns-ratios), and therefore we have 2 dependencies. Choosing G_2

as a reference, the following conductance ratios are derived using (4.6a,7-11):

$$\frac{G_1}{G_2} = \frac{\alpha_1(\alpha_2-1)}{n(1-\alpha_1)\alpha_2} = \frac{\alpha_1\alpha_5}{\alpha_2\alpha_4} \quad , \quad \frac{G_3}{G_2} = \frac{\alpha_3\alpha_5}{\alpha_2(1-\alpha_4-\alpha_5)}$$

$$\frac{G_4}{G_2} = \frac{(1-\alpha_3)\alpha_5}{\alpha_2(1-\alpha_4-\alpha_5)} = \frac{(\alpha_2-1)}{(1-n)\alpha_2} \quad , \quad \frac{G_5}{G_2} = \frac{(\alpha_2-1)}{n\alpha_2} \qquad (4.18)$$

The 2 dependence relationships are derived using (4.18), i.e.

$$1-\alpha_1 = \frac{(1-n)(1-\alpha_3)\alpha_4}{n(1-\alpha_4-\alpha_5)} \qquad (4.19)$$

$$= \frac{(\alpha_2-1)\alpha_4}{n\alpha_5} \qquad (4.20)$$

In order to transform these dependencies to an SOP form, a new set of independent parameters must be defined.

In the following, we use the K matrix as defined in (4.17). This choice is independent of α_2, which decreases the number of dependencies to 1, which is given by (4.19).

4.2.1 Non-reflection-free Brune Designs

Using (4.19), the following 3 solutions for redefining the parameters exist:

(1)
$$\beta_1 = n \qquad \alpha_1 = 1-(1-\beta_1)\beta_2\beta_4$$
$$\beta_2 = \alpha_4 \qquad \alpha_3 = 1-\beta_1(1-\beta_2-\beta_3)\beta_4$$
$$\beta_3 = \alpha_5$$
$$\beta_4 = \frac{1-\alpha_3}{n(1-\alpha_4-\alpha_5)} \qquad (4.21)$$

$$\beta_1 = n \qquad \alpha_4 = \beta_1(1-\beta_2)\beta_4$$
$$\beta_2 = \alpha_1 \qquad \alpha_5 = 1-\beta_4(\beta_1(1-\beta_2)+(1-\beta_1)(1-\beta_3))$$
$$\beta_3 = \alpha_3$$
$$\beta_4 = \frac{\alpha_4}{n(1-\alpha_1)} \tag{4.22}$$

$$\beta_1 = n \qquad \alpha_3 = 1-\beta_1(1-\beta_2)\beta_4$$
$$\beta_2 = \alpha_1 \qquad \alpha_5 = 1-\beta_3(1+(1-\beta_1)\beta_4)$$
$$\beta_3 = \alpha_4 \tag{4.22a}$$
$$\beta_4 = \frac{1-\alpha_3}{n(1-\alpha_1)}$$

Clearly, the redefinitions allow α_1 , α_3 , α_4 , α_5 , and n to be expressed as the SOPs of $\{ \beta_i \}_{i=1}^{4}$. Generally speaking, design #2 is preferred because β_3 fixes the location of the attenuation pole.

4.2.2 Reflection-free Brune Designs

The imposition of the reflection-free property at an interconnecting port decreases the number of degrees of freedom by one. This decrease is characterized by an additional dependence relationship that exists between the design parameters.

Port #1 reflection-free:

Using (4.4), the additional dependence relationship is obtained by setting $\ell_{11} = \frac{1}{2}$ in (4.14). This yields

$$\alpha_1(1-\alpha_4) = \frac{1}{2} \tag{4.23}$$

Substituting (4.23) into (4.19) and solving for α_5, we obtain

$$\alpha_5 = \frac{(1-\alpha_4)(1-2(1-n)(1-\alpha_3)\alpha_4)}{n(1-2\alpha_4)} \tag{4.24}$$

Using (4.23,24), we can eliminate α_1 and α_5 from the entries in the K matrix given by (4.17), i.e.

$$\alpha_1\alpha_5 = \frac{1}{2}\left(1- \frac{2(1-n)\sqrt{(1-\alpha_3)}\alpha_4}{\sqrt{n(1-2\alpha_4)}}\right) \tag{4.25}$$

$$\alpha_3\alpha_5 = \alpha_3(1-\alpha_4)\left(1- \frac{2(1-n)\sqrt{(1-\alpha_3)}\alpha_4}{\sqrt{n(1-2\alpha_4)}}\right) \tag{4.26}$$

and the remaining terms in the K matrix are either constant or functions of α_3, α_4, and n only. To remove the rational dependence in (4.25,26), it suffices to define the term enclosed by the dashed line as a new parameter, i.e let

$$\begin{aligned} \beta_1 &= n & \alpha_1 &= \frac{1}{2(1-\beta_2)} \\ \beta_2 &= \alpha_4 & \alpha_3 &= 1-\beta_1(1-2\beta_2)\beta_3 \\ \beta_3 &= \frac{1-\alpha_3}{n(1-2\alpha_4)} & \alpha_5 &= (1-\beta_2)(1-2(1-\beta_1)\beta_2\beta_3) \end{aligned} \tag{4.27}$$

and $\{\beta_i\}_{i=1}^{3}$ is the new independent parameter set. This set generates entries in the S matrix that are in the SOP form.

Solving (4.20) for α_2 yields

$$\alpha_2 = 1 + \frac{n(1-\alpha_1)\alpha_5}{\alpha_4} \tag{4.28}$$

which is used, together with (4.27), in solving for a unique set of conductance ratios given by (4.18).

Port #2 reflection-free:

The additional dependence relationship is obtained by setting $\ell_{22}=\frac{1}{2}$ in (4.14), which yields

$$\alpha_2(1-\alpha_5) = \frac{1}{2} \tag{4.29}$$

Substituting (4.29) into (4.20), and solving for α_1, and α_3, we obtain

$$1-\alpha_1 = \frac{\alpha_4(2\alpha_5-1)}{2n\alpha_5(1-\alpha_5)} \tag{4.30}$$

$$1-\alpha_3 = \frac{(1-\alpha_4-\alpha_5)(2\alpha_5-1)}{2(1-n)\alpha_5(1-\alpha_5)} \tag{4.31}$$

Using (4.30,31), we eliminate α_1 and α_3 from the entries in the K matrix:

$$\begin{aligned}
\alpha_1\alpha_5 &= \alpha_5 - \frac{\alpha_4(2\alpha_5-1)}{2n(1-\alpha_5)} \\
\alpha_3\alpha_5 &= \alpha_5 - \frac{(1-\alpha_4-\alpha_5)(2\alpha_5-1)}{2(1-n)(1-\alpha_5)} \\
\alpha_1(1-\alpha_4) &= 1-\alpha_4 - \frac{(1-\alpha_4)\alpha_4(2\alpha_5-1)}{2n(1-\alpha_5)} \\
\alpha_3\alpha_4 &= \alpha_4 - \frac{\alpha_4(1-\alpha_4-\alpha_5)(2\alpha_5-1)}{2(1-n)\alpha_5(1-\alpha_5)}
\end{aligned} \tag{4.32}$$

The redefinition process is more involved than in the previous case because it is not possible to obtain SOP form by

defining only one new multiplier. For this case, it suffices to (1) define a parameter that removes part of the rational dependence in (4.32), (2) make the appropriate substitution in (4.32), (3) define a second parameter that removes the remaining rational dependence. Using this procedure we obtain 2 solutions:

(1) Let

$$\begin{aligned} \beta_1 &= n & \alpha_1 &= 1-2(1-\beta_1)\beta_2\beta_3 \\ \beta_2 &= \frac{\alpha_4}{2n\alpha_5(1-\alpha_5)} & \alpha_3 &= 1-\frac{(1-2\beta_1\beta_2\alpha_5)\beta_3}{\alpha_5} \\ \beta_3 &= \frac{2\alpha_5-1}{2(1-n)} & \alpha_4 &= 2\beta_1\beta_2\alpha_5(1-\alpha_5) \\ & & \alpha_5 &= (1-\beta_1)\beta_3+\frac{1}{2} \end{aligned} \tag{4.33}$$

where β_2 is contained by the dashed line in (4.30).

(2) Let

$$\begin{aligned} \beta_1 &= n & \alpha_1 &= 1-\frac{(1-2(1-\beta_1)\beta_2\alpha_5)\beta_3}{\alpha_5} \\ \beta_2 &= \frac{1-\alpha_4-\alpha_5}{2(1-n)\alpha_5(1-\alpha_5)} & \alpha_3 &= 1-\beta_1\beta_2\beta_3 \\ & & \alpha_4 &= (1-\alpha_5)(1-2(1-\beta_1)\beta_2\alpha_5) \\ \beta_3 &= \frac{2\alpha_5-1}{2n} & \alpha_5 &= \beta_1\beta_3+\frac{1}{2} \end{aligned} \tag{4.34}$$

where β_2 is contained by the dashed line in (4.31).

4.2.3 Simplified Brune Section Designs

The complexity of the Brune adaptor can be reduced significantly by imposing the following constraint: let

$$\alpha_1 = \alpha_3 \tag{4.35}$$

which together with (4.19) also implies that

$$\alpha_4 = n(1-\alpha_5) \tag{4.36}$$

Substituting (4.35,36) into (4.14) yields

$$L = \begin{bmatrix} \alpha_1(1-n(1-\alpha_5)) & -n(1-\alpha_1\alpha_5) & \alpha_1 n(1-\alpha_5) & 1-\alpha_1 \\ -\alpha_1\alpha_5 & 1-\alpha_1\alpha_5 & \alpha_1\alpha_5 & 0 \\ \alpha_1(1-\alpha_5)(1-n) & (1-n)(1-\alpha_1\alpha_5) & \alpha_1(\alpha_5+n(1-\alpha_5)) & 1-\alpha_1 \\ \alpha_1(1-n) & 0 & \alpha_1 n & 1-\alpha_1 \end{bmatrix} \tag{4.37}$$

The constraint reduces the number of degrees of freedom to 3. The entries in (4.37) are functions of α_1, α_5, and n only, and are in the SOP form. It follows, then, that the reflection-free design is essentially complete. However, instead of using α_5, we choose to define $\alpha_1\alpha_5$ as one of the design parameters. This reduces the maximum number of components in the product terms in (4.37) from three to two. Consequently, lower word-lengths can be achieved for the adaptor multipliers.

The port #2 reflection-free design is obtained by setting ℓ_{22}=1/2, which yields

$$\alpha_1\alpha_5 = \frac{1}{2} \tag{4.38}$$

and (4.37) reduces to

$$L = \begin{bmatrix} \alpha_1(1-n)+\frac{n}{2} & -n/2 & n(\alpha_1-\frac{1}{2}) & 1-\alpha_1 \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 \\ (\alpha_1-\frac{1}{2})(1-n) & \frac{1}{2}(1-n) & \frac{1}{2}+n(\alpha_1-\frac{1}{2}) & 1-\alpha_1 \\ \alpha_1(1-n) & 0 & \alpha_1 n & 1-\alpha_1 \end{bmatrix} \tag{4.39}$$

Again, all entries are in the SOP form and the number of independent design parameters, α_1 and n, is equal to the number of degrees of freedom. Consequently, the design is complete.

The constraint on the conductance values that corresponds to (4.36) is given by

$$G_1G_4 = G_3G_5 \tag{4.40}$$

If the elements of the analog prototype satisfy (4.40), then either (4.37) or (4.39) should be used in

$$S = 2L - U \tag{4.41}$$

where (4.41) was obtained using (4.2). In some cases the analog prototype can be redesigned, using any suitable optimization technique, such that (4.40) is satisfied.

4.3 DESIGN OF THE 3RD-ORDER ELLIPTIC ADAPTOR

Elliptic transfer functions can be realized by nonminimal ladder networks with finite transmission zeros. The 3rd order case is presented in Fig.4.6.

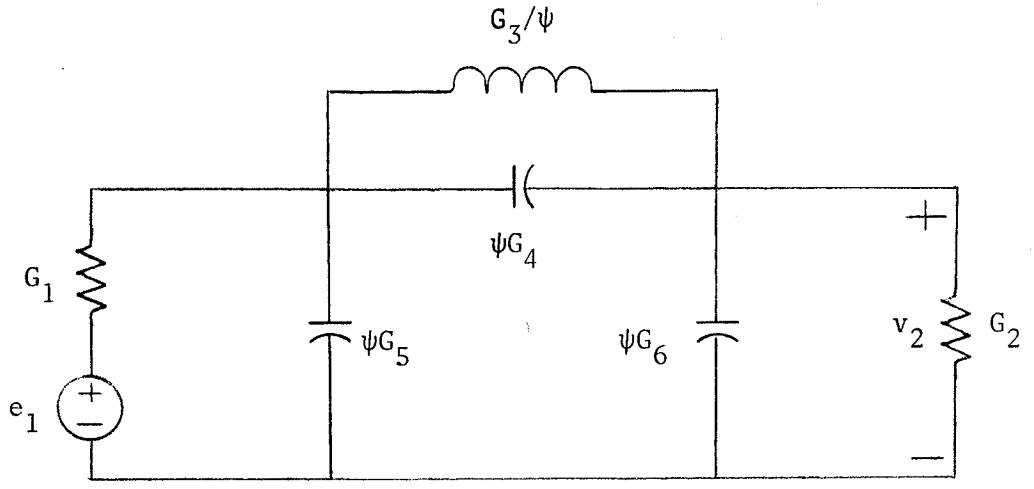


Figure 4.6: 3rd order elliptic filter.

The design of the WD adaptor based on the above prototype was presented in example #3, Sec.3.2.2. In this section we present a simplified design as well as minimal and diagonalized designs.

The minimal adaptor is characterized by

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} v_5 \\ v_6 \end{bmatrix} \tag{4.42}$$

$$\begin{bmatrix} v_5 \\ v_6 \end{bmatrix} = \begin{bmatrix} \alpha_1(1-\alpha_4) & -\alpha_2\alpha_4 & \alpha_3\alpha_4 \\ -\alpha_1\alpha_5 & \alpha_2(1-\alpha_5) & \alpha_3\alpha_4 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix}$$

where the redundant link port #4, due to the capacitive loop in Fig.4.6, has been deleted. Ashley [30] has derived the corresponding diagonal Lyapunov function that is different from the reference conductance matrix G. This function, however, is only applicable when the adaptor is operated by itself and is not a part of a larger system.

A 3rd-order elliptic transfer function can be realized by the network in Fig.4.6 with two element constraints:

$$G_1 = G_2 \quad , \quad G_5 = G_6 \tag{4.43a,b}$$

Using G_4 as a reference and $\{ \alpha_i \}_{i=1}^{5}$ as defined in Sec.3.2.2, we obtain

$$\frac{G_1}{G_4} = \frac{\alpha_1 c}{\alpha_4} \qquad \frac{G_2}{G_4} = \frac{\alpha_2 c}{\alpha_5} \qquad \frac{G_5}{G_4} = \frac{(1-\alpha_1)c}{\alpha_4} \qquad \frac{G_6}{G_4} = \frac{(1-\alpha_2)c}{\alpha_5}$$

$$\frac{G_3}{G_4} = \frac{\alpha_3}{1-\alpha_3} \qquad c = \frac{1-\alpha_4-\alpha_5}{1-\alpha_3} \tag{4.44}$$

The element constraints together with (4.44) imply that

$$\alpha_1 = \alpha_2 \quad , \quad \alpha_4 = \alpha_5 \tag{4.45a,b}$$

With the two element constraints the number of degrees of freedom is 3. Using (4.45), α_2, and α_5 can be removed from the entries in K, thus leaving 3 independent parameters. Define

$$\beta_1 = \alpha_1 \quad , \quad \beta_2 = \alpha_1\alpha_4 \quad , \quad \beta_3 = \alpha_3\alpha_4 \tag{4.46}$$

The resulting K matrix and the conductance ratios with respect to G become

$$K = \begin{bmatrix} \beta_1 - \beta_2 & -\beta_2 & \beta_3 \\ -\beta_2 & \beta_1 - \beta_2 & \beta_3 \end{bmatrix} \qquad (4.47)$$

$$\frac{G_3}{G_1} = \frac{\beta_3}{\beta_1 - 2\beta_2} \quad , \quad \frac{G_4}{G_1} = \frac{\beta_2 - \beta_1\beta_3}{\beta_1(\beta_1 - 2\beta_2)} , \quad \frac{G_5}{G_1} = \frac{1 - \beta_1}{\beta_1} \qquad (4.48)$$

An example using the simplified adaptor is presented in the next chapter.

The minimal adaptor with a diagonal reference conductance matrix was derived in Sec.3.5. To remove the rational dependence, the independent design parameter set must be redefined. From Sec.3.5 we have

$$W_\ell = U \quad , \quad W_t = \begin{bmatrix} 1 & -\gamma_1 \\ 0 & 1 \end{bmatrix} \quad , \quad \gamma_1 = \frac{G_4}{G_4 + G_5} \qquad (4.49)$$

and using (3.65,66), we obtain

$$\hat{N}^T = W_\ell^{-1} N^T W_t = \begin{bmatrix} 1 & -\gamma_1 \\ 0 & 1 \\ 1 & 1-\gamma_1 \end{bmatrix} \qquad (4.50)$$

$$\hat{K} = W_t^{-1} K W_\ell = \begin{bmatrix} \alpha_1(1-\alpha_4-\gamma_1\alpha_5) & \alpha_2(\gamma_1(1-\alpha_5)-\alpha_4) & \alpha_3(\alpha_4+\gamma_1\alpha_5) \\ -\alpha_1\alpha_5 & \alpha_2(1-\alpha_5) & \alpha_3\alpha_5 \end{bmatrix} \qquad (4.51)$$

The single dependence relationship is given by

$$\gamma_1 = \frac{1}{1 + \dfrac{(1-\alpha_1)(1-\alpha_4-\alpha_5)}{(1-\alpha_3)\alpha_4}} \qquad (4.52)$$

4.3.1 Non-reflection-free 3rd-order Elliptic Adaptor Designs

Based on (4.52), the following 3 solutions for redefining the parameter set exist:

(1) Solving (4.52) for α_1, we obtain

$$1 - \alpha_1 = \frac{\boxed{(1-\alpha_3)}\alpha_4(1-\gamma_1)}{\boxed{(1-\alpha_4-\alpha_5)\gamma_1}} \qquad (4.53)$$

Define

$$\beta_1 = \gamma_1 \qquad \alpha_1 = 1-(1-\beta_1)\beta_3\beta_4$$

$$\beta_2 = \alpha_2 \qquad \alpha_3 = 1-\beta_1\beta_3(1-\beta_4-\beta_5)$$

$$\beta_3 = \frac{1-\alpha_3}{(1-\alpha_4-\alpha_5)\gamma_1} \qquad (4.54)$$

$$\beta_4 = \alpha_4$$

$$\beta_5 = \alpha_5$$

where β_3 is enclosed by the dashed line in (4.53).

(2) Solving (4.52) for α_5, we obtain

$$1 - \alpha_5 = \alpha_4\left(1 + \frac{\boxed{(1-\alpha_3)}(1-\gamma_1)}{\boxed{(1-\alpha_1)\gamma_1}}\right) \qquad (4.55)$$

Define

$$\beta_1 = \alpha_1 \qquad \alpha_3 = 1-(1-\beta_1)\beta_3\beta_5$$

$$\beta_2 = \alpha_2 \qquad \alpha_5 = 1-\beta_4(1+(1-\beta_3)\beta_5)$$

$$\beta_3 = \gamma_1$$

$$\beta_4 = \alpha_4 \qquad (4.56)$$

$$\beta_5 = \frac{1-\alpha_3}{(1-\alpha_1)\gamma_1}$$

where β_5 is enclosed by the dashed line in (4.55).

(3) Rewriting (4.55), we obtain

$$1 - \alpha_5 = \left[\frac{\alpha_4}{(1-\alpha_1)\gamma_1}\right](\gamma_1(1-\alpha_1)+(1-\alpha_3)(1-\gamma_1)) \qquad (4.57)$$

Define

$$\beta_1 = \alpha_1 \qquad \alpha_4 = (1-\beta_1)\beta_4\beta_5$$

$$\beta_2 = \alpha_2 \qquad \alpha_5 = 1-\beta_4(1-\beta_3+(\beta_3-\beta_1)\beta_5)$$

$$\beta_3 = \alpha_3$$

$$\beta_4 = \frac{\alpha_4}{(1-\alpha_1)\gamma_1} \qquad (4.58)$$

$$\beta_5 = \gamma_1$$

where β_4 is enclosed by the dashed line in (4.57). Generally speaking, design (4.58) is preferred because β_3 fixes the location of the attenuation pole.

4.3.2 Reflection-free 3rd-order Elliptic Adaptor Designs

Port #1 reflection-free:

The additional dependence relationship

$$\alpha_1(1-\alpha_4) = \frac{1}{2} \tag{4.59}$$

is obtained using (3.29a). Substituting (4.59) into (4.52), and solving for α_3, we obtain

$$1 - \alpha_3 = \frac{\gamma_1 \boxed{(1-\alpha_4-\alpha_5)(1-2\alpha_4)}}{2(1-\gamma_1)(1-\alpha_4)\alpha_4} \tag{4.60}$$

Define

$$\begin{aligned} \beta_1 &= \gamma_1 & \alpha_3 &= 1-\beta_1\beta_3(1-2\beta_4) \\ \beta_2 &= \alpha_2 & \alpha_5 &= (1-\beta_4)(1-2(1-\beta_1)\beta_3\beta_4) \\ \beta_3 &= \frac{1-\alpha_4-\alpha_5}{2(1-\gamma_1)(1-\alpha_4)\alpha_4} & \alpha_1 &= \frac{1}{2(1-\beta_4)} \\ \beta_4 &= \alpha_4 \end{aligned} \tag{4.61}$$

where β_3 is enclosed by the dashed line in (4.60).

Port #2 reflection-free:

The additional dependence relationship

$$\alpha_2(1-\alpha_5) = \frac{1}{2} \tag{4.62}$$

is obtained using (3.29a). Using (4.62) and (4.53), we can eliminate α_1, α_2, and α_3 from the entries in the K matrix. The only rational term remaining

$$\alpha_2\alpha_4 = \frac{\alpha_4}{2(1-\alpha_5)} \tag{4.63}$$

can be removed by defining it as one of the parameters, i.e. define

$$\begin{aligned}
\beta_1 &= \gamma_1 & \alpha_1 &= 1-2(1-\beta_1)(1-\beta_2)\beta_3\beta_4 \\
\beta_2 &= \alpha_5 & \alpha_2 &= \frac{1}{2(1-\beta_2)} \\
\beta_3 &= \frac{1-\alpha_3}{\gamma_1(1-\alpha_4-\alpha_5)} & \alpha_3 &= 1-\beta_1(1-\beta_2)\beta_3(1-2\beta_4) \\
\beta_4 &= \frac{\alpha_4}{2(1-\alpha_5)} & \alpha_4 &= 2(1-\beta_2)\beta_4
\end{aligned} \tag{4.64}$$

which completes the design.

As was mentioned in Sec.3.5, the diagonalization can be effected in 2 different ways. The designs based on the second method can be shown to be equivalent to the designs derived above by interchanging G_1 with G_2 and G_5 with G_6. This is because the prototype is topologically symmetrical. Also, other simplified designs can be derived by imposing different constraints; for example $\alpha_1 = \alpha_3$ or $\alpha_2 = \alpha_3$. These designs can be shown to be equivalent to the simplified Brune adaptors interconnected with the parallel adaptor.

4.4 DESIGN OF THE 5TH-ORDER ELLIPTIC ADAPTORS

The ladder network shown in Fig.4.7 can be used in realizing 5th-order elliptic transfer functions.

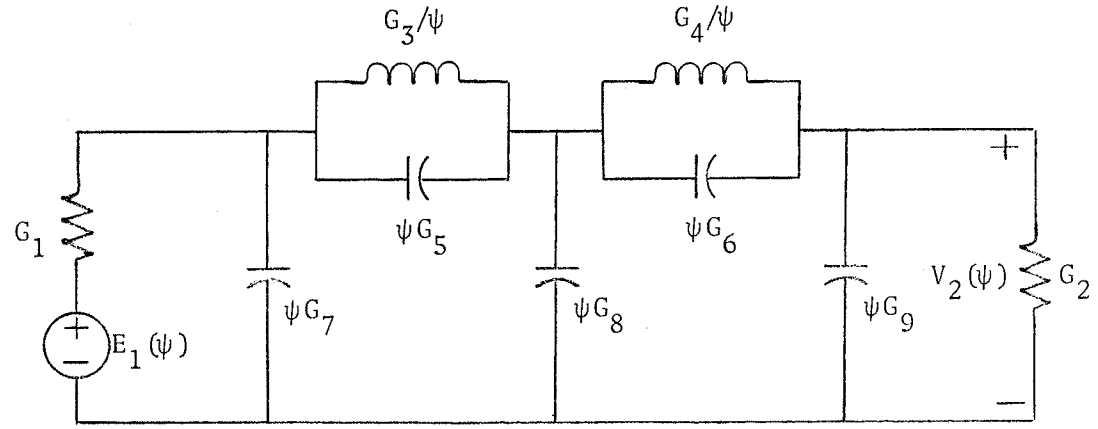


Figure 4.7: The 5th-order elliptic ladder topology.

The above network is nonminimal with 2 redundant capacitive loops. A minimal network can be derived by applying the network equivalence in Fig.4.1 two times. One possible result is shown in Fig.4.8.

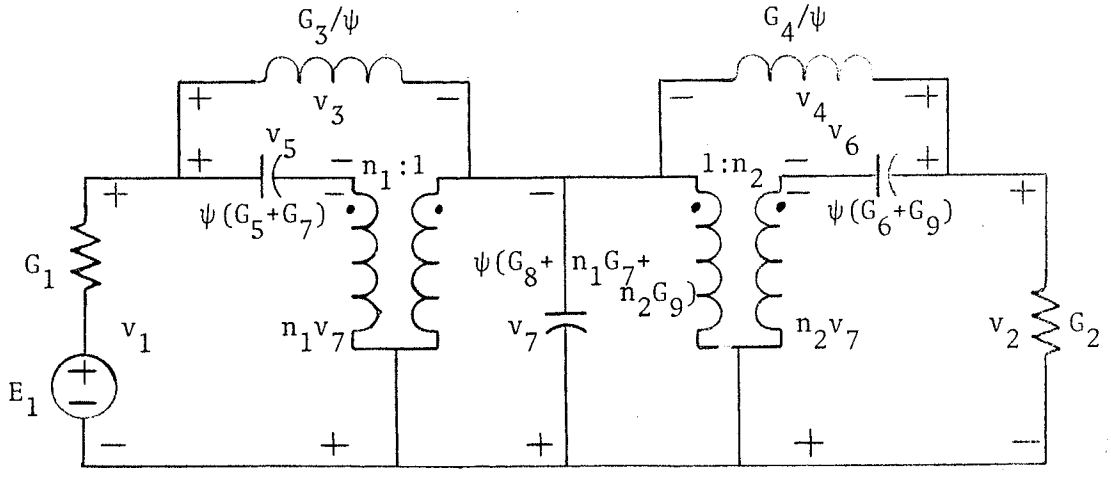


Figure 4.8: A minimal referenced 5th-order elliptic prototype.

With reference to Fig.4.8, the loop equations become

$$\begin{aligned} v_1 + n_1 v_7 &= v_5 \\ v_2 + n_2 v_7 &= v_6 \\ v_1 + v_7 &= v_3 \\ v_2 + v_7 &= v_4 \end{aligned} \tag{4.65}$$

and

$$n_1 = \frac{G_5}{G_5 + G_7} \quad , \quad n_2 = \frac{G_6}{G_6 + G_9} \tag{4.66}$$

are the ideal-transformer turns-ratios. We select

$$\begin{aligned} v_\ell &= [\, v_1 \, , \, v_2 \, , \, v_3 \, , \, v_4 \,]^T \\ v_t &= [\, v_5 \, , \, v_6 \, , \, v_7 \,]^T \end{aligned} \tag{4.67}$$

as the link- and tree-port voltage vectors, respectively. Using (4.65,67), we can obtain the required N matrix:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & -n_1 \\ 0 & 1 & -n_2 \\ 1 & 0 & 1-n_1 \\ 0 & 1 & 1-n_2 \end{bmatrix}}_{N^T} \begin{bmatrix} v_5 \\ v_6 \\ v_7 \end{bmatrix} \tag{4.68}$$

To solve for the K matrix we first obtain the resistively terminated version of the analog prototype which is shown in Fig.4.9.

As was the case with the Brune design, we circumvent the problem of working with the ideal-transformers by using the

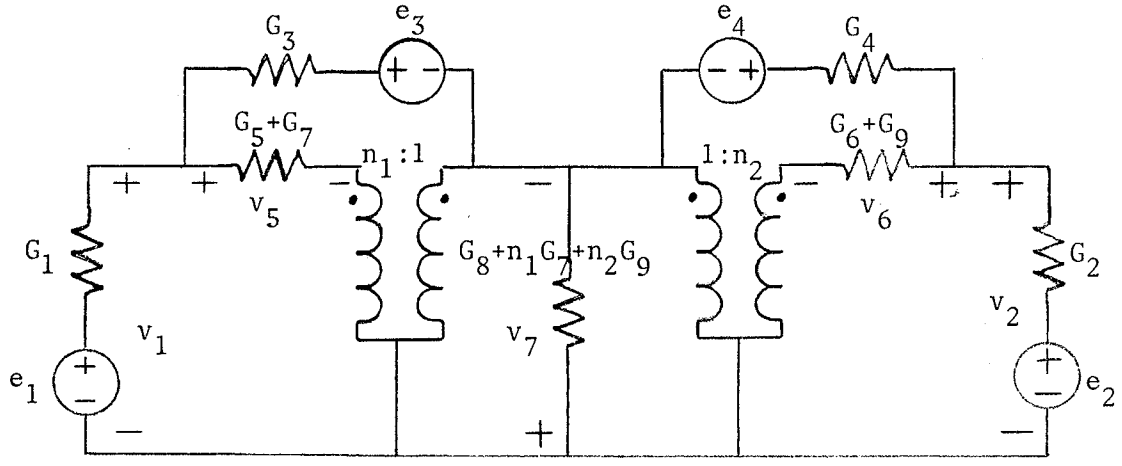


Figure 4.9: Resistively terminated prototype network

resistively terminated ladder prototype to solve for the easily obtainable voltages which, together with the loop equations in (4.65), yield the remaining tree-port voltages. The resistively terminated ladder prototype is displayed in Fig.4.10.

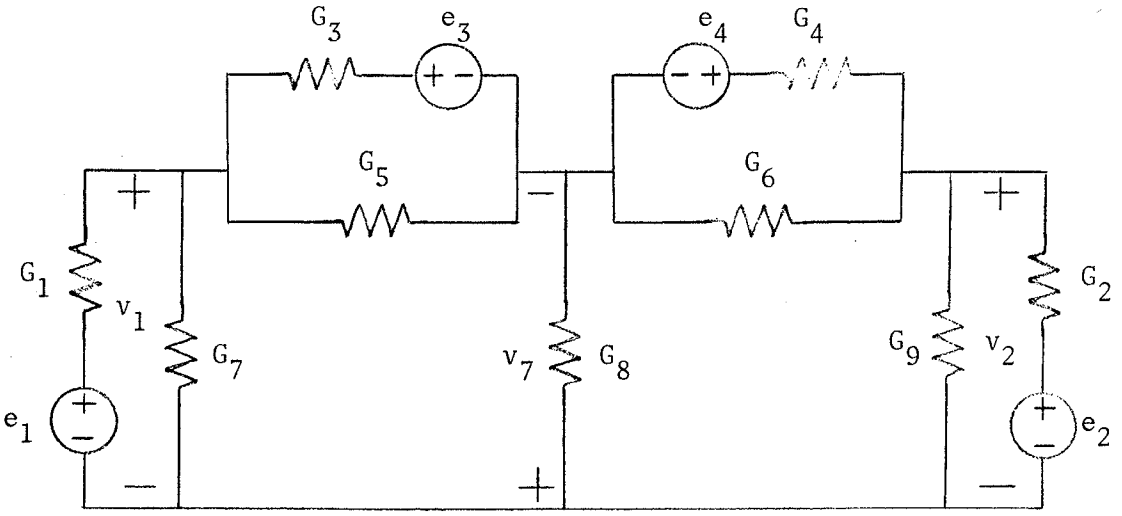


Figure 4.10: Resistively terminated ladder prototype.

We now apply Thevenin's theorem to obtain a succession of simpler networks, i.e. with reference to Fig.4.10 let

$$\alpha_1 = \frac{G_1}{G_1+G_7} \qquad \alpha_2 = \frac{G_2}{G_2+G_9} \qquad \alpha_3 = \frac{G_3}{G_3+G_5} \qquad \alpha_4 = \frac{G_4}{G_4+G_6} \tag{4.69a-d}$$

Using these , we obtain the simplified network shown in Fig.4.11.

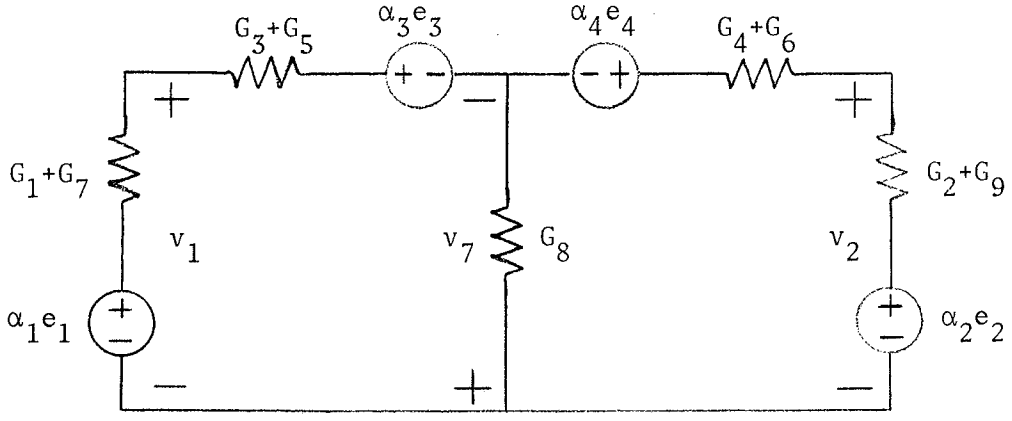


Figure 4.11: A simplified resistive ladder.

Also, let

$$\alpha_5 = \frac{G_3+G_5}{G_3+G_5+G_1+G_7} \qquad \alpha_6 = \frac{G_4+G_6}{G_4+G_6+G_2+G_9} \tag{4.70}$$

from which we have using superposition

$$v_1 = \alpha_5(\alpha_3 e_3 - v_7) + (1-\alpha_5)\alpha_1 e_1 \tag{4.71}$$

$$v_2 = \alpha_6(\alpha_4 e_4 - v_7) + (1-\alpha_6)\alpha_2 e_2 \qquad (4.72)$$

Using (4.70), we also obtain the simplified network shown in Fig.4.12.

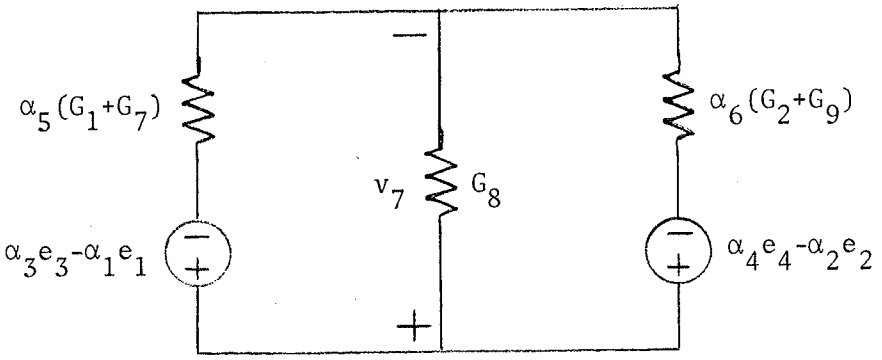


Figure 4.12: A simplified resistive network.

Finally, let

$$\alpha_7 = \frac{1}{1 + \dfrac{G_8+\alpha_6(G_2+G_9)}{\alpha_5(G_1+G_7)}} \quad , \quad \alpha_8 = \frac{1}{1 + \dfrac{G_8+\alpha_5(G_1+G_7)}{\alpha_6(G_2+G_9)}} \qquad (4.73a,b)$$

and from Fig.4.12 we have

$$v_7 = \alpha_7(\alpha_3 e_3 - \alpha_1 e_1) + \alpha_8(\alpha_4 e_4 - \alpha_2 e_2) \qquad (4.74)$$

Using v_1, v_2, v_7, and the first 2 loop equations in (4.65), we solve for the K matrix:

$$K=\begin{bmatrix} \alpha_1(1-\alpha_5)+\alpha_1\alpha_7(\alpha_5-n_1) & \alpha_2\alpha_8(\alpha_5-n_1) & \alpha_3\alpha_5-\alpha_3\alpha_7(\alpha_5-n_1) & -\alpha_4\alpha_8(\alpha_5-n_1) \\ \alpha_1\alpha_7(\alpha_6-n_2) & \alpha_2(1-\alpha_6)+\alpha_2\alpha_8(\alpha_6-n_2) & -\alpha_3\alpha_7(\alpha_5-n_1) & \alpha_4\alpha_6-\alpha_4\alpha_6(\alpha_6-n_2) \\ -\alpha_1\alpha_7 & -\alpha_2\alpha_8 & \alpha_3\alpha_7 & \alpha_4\alpha_8 \end{bmatrix} \quad (4.75)$$

Choosing G_8 as reference, we obtain using $\{\alpha_i\}_{i=1}^{8}$ the following conductance ratios:

$$\frac{G_1}{G_8}=\frac{\alpha_1 c_1}{\alpha_5} \qquad \frac{G_3}{G_8}=\frac{\alpha_3 c_1}{1-\alpha_5} \qquad \frac{G_5}{G_8}=\frac{(1-\alpha_3)c_1}{1-\alpha_5} \qquad \frac{G_7}{G_8}=\frac{(1-\alpha_1)c_1}{\alpha_5}$$

$$\frac{G_2}{G_8}=\frac{\alpha_2 c_2}{\alpha_6} \qquad \frac{G_4}{G_8}=\frac{\alpha_4 c_2}{1-\alpha_6} \qquad \frac{G_6}{G_8}=\frac{(1-\alpha_4)c_2}{1-\alpha_6} \qquad \frac{G_9}{G_8}=\frac{(1-\alpha_2)c_2}{\alpha_6} \quad (4.76)$$

$$c_1=\frac{\alpha_7}{1-\alpha_7-\alpha_8} \qquad c_2=\frac{\alpha_8}{1-\alpha_7-\alpha_8}$$

The number of degrees of freedom in the prototype is 8 whereas 10 parameters were defined in solving for N and K. The 2 dependence relationships are obtained using (4.66) and (4.76):

$$1-\alpha_1=\frac{(1-\alpha_3)(1-n_1)\alpha_5}{n_1(1-\alpha_5)} \quad (4.77)$$

$$1-\alpha_2=\frac{(1-\alpha_4)(1-n_2)\alpha_6}{n_2(1-\alpha_6)} \quad (4.78)$$

The rational dependence is eliminated by defining the terms enclosed by the dashed lines as new parameters, i.e. let

$$\begin{aligned}
&\beta_1 = n_1 && \beta_5 = \alpha_5 && \alpha_1 = 1-(1-\beta_1)\beta_3\beta_5 \\
&\beta_2 = n_2 && \beta_6 = \alpha_6 && \alpha_2 = 1-(1-\beta_2)\beta_4\beta_6 \\
&\beta_3 = \frac{1-\alpha_3}{n_1(1-\alpha_5)} && \beta_7 = \alpha_7 && \alpha_3 = 1-\beta_1\beta_3(1-\beta_5) \\
&\beta_4 = \frac{1-\alpha_4}{n_2(1-\alpha_6)} && \beta_8 = \alpha_8 && \alpha_4 = 1-\beta_2\beta_4(1-\beta_6)
\end{aligned} \tag{4.79}$$

and the design is complete.

In general, the computational requirement of a WD filter can be reduced if the number of coefficients in the product terms in the entries of K is also reduced. For the adaptor presently under consideration, this can be achieved by imposing the following constraints:

$$\beta_5 = \frac{1}{1 + \frac{G_1+G_7}{G_3+G_5}} = n_1 = \frac{1}{1 + \frac{G_7}{G_5}} \tag{4.80}$$

$$\beta_6 = \frac{1}{1 + \frac{G_2+G_9}{G_4+G_6}} = n_2 = \frac{1}{1 + \frac{G_9}{G_6}} \tag{4.81}$$

which, in terms of the conductance values, can also be expressed as

$$G_3G_7 = G_1G_5 \quad , \quad G_4G_9 = G_2G_6 \tag{4.82a,b}$$

The above conductance constraints together with (4.69) also imply that

$$\alpha_1 = \alpha_3 \quad , \quad \alpha_2 = \alpha_4 \qquad (4.83a,b)$$

The number of degrees of freedom is reduced to 6, however, because of (4.83), we also have only 6 parameters. The canonic set of design parameters can be defined as follows:

$$\begin{aligned} \beta_1 &= \alpha_1 = \alpha_3 & \beta_4 &= \alpha_6 = n_2 \\ \beta_2 &= \alpha_2 = \alpha_4 & \beta_5 &= \alpha_1\alpha_7 \\ \beta_3 &= \alpha_5 = n_1 & \beta_6 &= \alpha_2\alpha_8 \end{aligned} \qquad (4.84)$$

and (4.75) reduces to

$$\begin{bmatrix} v_5 \\ v_6 \\ v_7 \end{bmatrix} = \begin{bmatrix} \beta_1(1-\beta_3) & 0 & \beta_1\beta_3 & 0 \\ 0 & \beta_2(1-\beta_4) & 0 & \beta_2\beta_4 \\ -\beta_5 & -\beta_6 & \beta_5 & \beta_6 \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_4 \end{bmatrix} \qquad (4.85)$$

The entries in (4.85) are functionally simpler than the entries in (4.75). Consequently, one can reasonably expect a substantial reduction in the computational requirement.

In general, the 5th-order elliptic topology can be simulated using either a combination of two Brune and a single parallel adaptor or one Brune and one 3rd-order elliptic adaptor. Using this approach, the overall design parameter set becomes the union of the parameter sets for the lower-

order adaptors. This set is usually different from the set given by (4.79). It turns out, however, that for the simplified design the set given by (4.84) is the union of the parameter sets from two Brune adaptors with reflection-free ports (defined by (4.39)) and one parallel adaptor (example #1, Sec.3.2.2), i.e. we can partition (4.84) as follows:

$$\{ \underbrace{\beta_1 , \beta_3}_{\text{Brune}} , \underbrace{\beta_5 , \beta_6}_{\text{parallel}} , \underbrace{\beta_2 , \beta_4}_{\text{Brune}} \} \qquad (4.86)$$

Consequently, an equivalent structure composed of two Brune and one parallel adaptor can be obtained, and is shown in Fig.4.13.

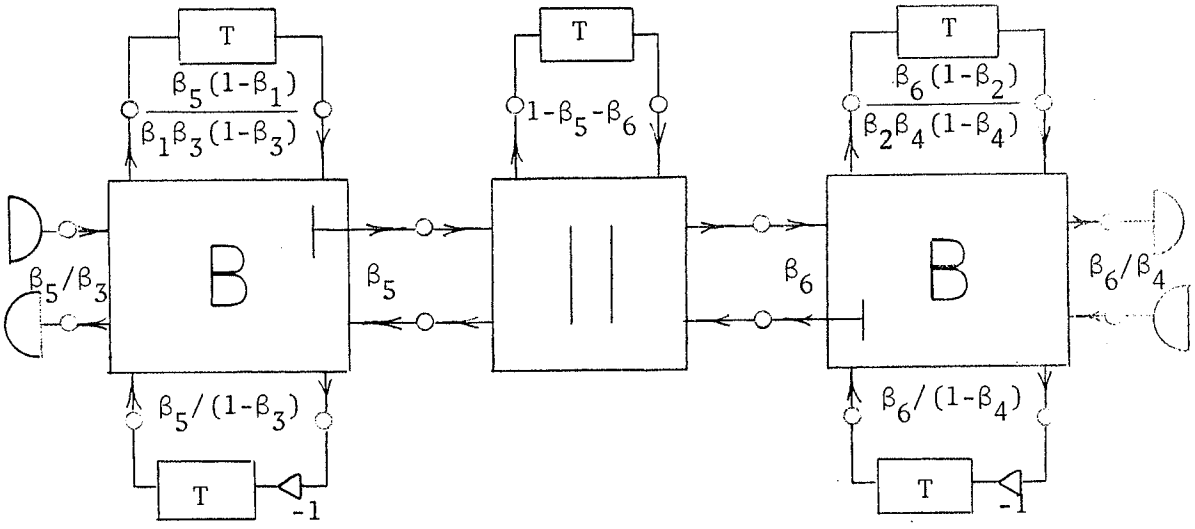


Figure 4.13: Equivalent structure for the simplified 5th-order adaptor

In Fig.4.13, we give the port-reference conductances in terms of the design parameters. The above structure is an alternate and can be used, as will be shown with examples in Chapter V, in reducing the overall computational requirement.

Chapter V

DETERMINATION OF QUANTIZED DESIGNS USING A SEARCH ALGORITHM

In the previous chapter we derived independent parameter sets for the basic minimal adaptors. These adaptors, together with the adaptors described in Sec.3.2.2, can be interconnected to obtain higher-order structures. In a practical situation, the independent parameters must be approximated with binary fractions to ensure realizability with digital components. In this chapter we present a finite search algorithm which, beginning with an initial binary fraction approximation, varies the numerators of the approximations and records all solutions that meet the specifications. Design examples of WD filters based on the 3rd and 5th-order elliptic prototypes are presented.

5.1 A FINITE SEARCH ALGORITHM

Consider a set of M independent parameters $\beta = \{ \beta_i \}_{i=1}^{M}$. Initially, parameter quatization is achieved as follows: let

$$\hat{\beta}_i = \frac{n_i}{2^{m_i}} \simeq \beta_i \quad , \quad i=1(1)M \tag{5.1}$$

where n_i and m_i are integers, and quantization employs rounding. Also, for each rational approximation we compute the corresponding error

$$e_i = \left| 1 - \hat{\beta}_i/\beta_i \right| \quad , \quad i=1(1)M \qquad (5.2)$$

To find approximated designs which satisfy the specifications, we propose a finite search algorithm which consists of the following steps:

1. The numerators of the binary fractions $\{ \hat{\beta}_i \}$ are varied within the specified ranges and all solutions that satisfy given specifications are recorded. If at least one solution is found, the search is stopped.
2. If no solution is found, then the m for the parameter with maximum e_i, i=1(1)M, is increased by one, and n_i and e_i are recomputed.
3. The search is repeated with care being taken to ensure that no duplicate designs (with respect to the previous search) are tested.

Note, that in the limit, a solution exists because the initial sets for each successive search converge to the continuous solution. The reasons for using this approach include:

1. The entries of the approximated S matrix are sums of products of $\{ \beta_i \}_{i=1}^{M}$. Consequently, in order that the overall word length of the adaptor remain reasonably small it suffices to ensure that m_i, i=1(1)M are small.
2. Solutions with small m_i, i=1(1)M exist because WD filters are known to be insensitive to parameter quantizations [9,46,47].

3. For stability reasons it is required that $G_i>0$ i=1(1)n, where n is the number of ports. This requirement results in two types of constraints for the corresponding parameters:

$$0 < \beta_i < 1 \quad , \quad g(\beta_i) > 0 \qquad (5.3,4)$$

where $g(\beta_i)$ is a continuous function derived from the formulae for the conductance ratios. The above are termed explicit and implicit constraints, respectively. These constraints define the feasible region and, for all design sets defined in Chapter IV, this region is bounded. This means that for constant m_i, i=1(1)M, the number of feasible design parameter sets that can be tested, as well as the time required to do so, is finite.

4. Solutions from all local optimum regions are recorded. These can then be compared with respect to the computational requirements.

It is important to note that, although theoretically it is possible to test all feasible parameter sets, the computer time to do so is prohibitive. Consequently, the ranges within which the numerators are allowed to vary must be decreased. Another approach is to confine the search to a subspace, i.e. a subset of the parameters becomes fixed and the rest are allowed to vary. In most cases, partitioning of the parameter set is apparent since the parameters are defined with respect to topologically symmetrical prototypes.

5.1.1 Computation of the Offset Vector

To generate the different parameter sets we allow the numerators, defined as p_i, of the rational approximations to vary within specified ranges, i.e. we let

$$p_i \in [\, n_i - s_i \;,\; n_i + s_i \,] \;,\quad i=1(1)M \tag{5.5}$$

where s_i, i=1(1)M are positive integers. Define

$$P_o = [\, n_1 \;,\; n_2 \;,\; \ldots \;,\; n_M \,] \tag{5.6}$$

and

$$R = [\, r_1 \;,\; r_2 \;,\; \ldots \;,\; r_M \,] \tag{5.7}$$

where r_i are integers. The new numerator vector $P=\{p_i\}_{i=1}^{M}$ can be computed as follows:

$$\begin{aligned} P &= P_o + R \\ &= [\, n_1+r_1 \;,\; n_2+r_2 \;,\; \ldots \;,\; n_M+r_M \,] \\ &= [\, p_1 \;,\; p_2 \;,\; \ldots \;,\; p_M \,] \end{aligned} \tag{5.8}$$

and

$$\hat{\beta}_i = \frac{p_i}{2^{m_i}} \;,\quad i=1(1)M \tag{5.8a}$$

The R vector is referred to as the offset vector and its elements are generated by counting in a mixed base number system. In this system, the 'digits' r_i count from $-s_i$ to s_i. The counting algorithm is presented in Fig.5.1.

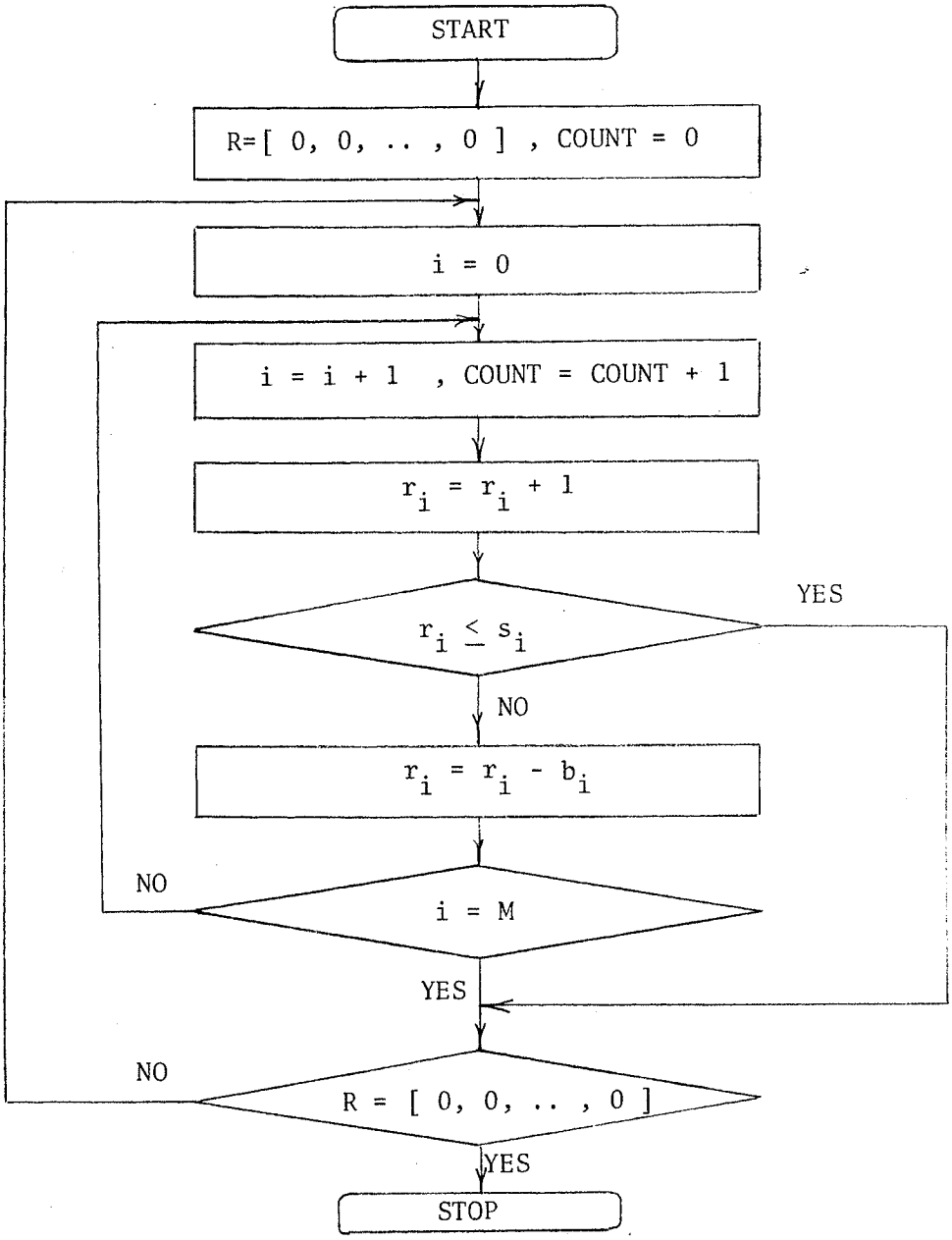


Figure 5.1: Flowchart for generating all possible R vectors

From Fig.5.1, we see that the value for COUNT, when STOP is reached, is

$$\begin{aligned} \text{COUNT} &= \prod_{i=1}^{M} (2s_i + 1) \\ &\triangleq \prod_{i=1}^{M} b_i \\ &\triangleq \text{COUNT}_{max} \end{aligned} \tag{5.9}$$

where b_i, i=1(1)M are defined as the bases. The value of $COUNT_{max}$ corresponds to the maximum number of possible R vectors, and hence possible design sets, that can be generated given the ranges s_i, i=1(1)M. In lexicographic notation the value of COUNT can also be represented by

$$COUNT = r_M r_{M-1} \cdots r_2 r_1 \tag{5.10}$$

The decimal equivalent is computed using

$$COUNT = \sum_{i=2}^{M} r_i \prod_{j=1}^{i-1} b_j + r_1 \tag{5.11}$$

and if COUNT<0 (this is possible because r_i are allowed to be negative), then replace COUNT with COUNT+$COUNT_{max}$. Clearly then, there exists a one-to-one correspondence between the integer set { i=1(1)$COUNT_{max}$ } and the R vectors generated by the algorithm in Fig.5.1. To illustrate, consider the case M=2, $s_1=s_2=1$. Using (5.9), we obtain

$$COUNT_{max} = \prod_{i=1}^{2} 3 = 9$$

and the correspondence between R and COUNT is shown below:

$r_2 r_1$	COUNT
0 1	1
1-1	2
1 0	3
1 1	4
-1-1	5
-1 0	6
-1 1	7
0-1	8
0 0	9

The numbers $r_2 r_1$ were generated sequentially using the algorithm in Fig.5.1.

The numerical correspondence between R and COUNT is used to speed up the process of generating all possible R vectors, which together with P , generate feasible sets of design parameters. To show this, consider the offset number

$$r_M r_{M-1} \cdot \cdot r_j r_{j-1} \cdot \cdot r_2 r_1 \tag{5.13}$$

such that

$$\hat{\beta}_j = \frac{n_j + r_j}{2^{m_j}} \tag{5.14}$$

is outside the feasible region (this can occur for parameters with implicit constraints). To cause the search to return to the feasible region, the value for r_j must change. To accomplish this, one possible method is to count up from R given by (5.13) until r_j changes. A more economical method, takes advantage of the relationship given by (5.11), i.e. we add

$$0\ 0\ \cdot\ \cdot\ 1\ -(s_{j-1}+r_{j-1})\ \cdot\ \cdot\ -(s_2+r_2)\ -(s_1+r_1) \tag{5.15}$$

to the number in (5.13). The result is given by

$$r_M r_{M-1} \cdot \cdot (r_j+1)\ -s_{j-1} \cdot \cdot -s_2\ -s_1 \tag{5.16}$$

which shows that, as required, the value for r_j changes. Addition in the mixed base system with positive and negative 'digits' is analogous to the decimal system, the difference

being that the 'digits' r_i are bounded by $[-s_i, s_i]$ instead of [0,9]. The variable COUNT changes by the positive value corresponding to (5.15), i.e.

$$\Delta COUNT = \prod_{k=1}^{j-1} b_k - \sum_{i=2}^{j-2} (s_i+r_i) \prod_{k=1}^{i-1} b_k - (s_1+r_1) \qquad (5.17)$$

Clearly, for problems where M is high, this method may substantially reduce the total execution time by skipping over most of the nonfeasible R vectors. To illustrate, consider the second entry in the above table:

$$r_2 r_1 = 1\text{-}1 \quad , \quad COUNT = 2$$

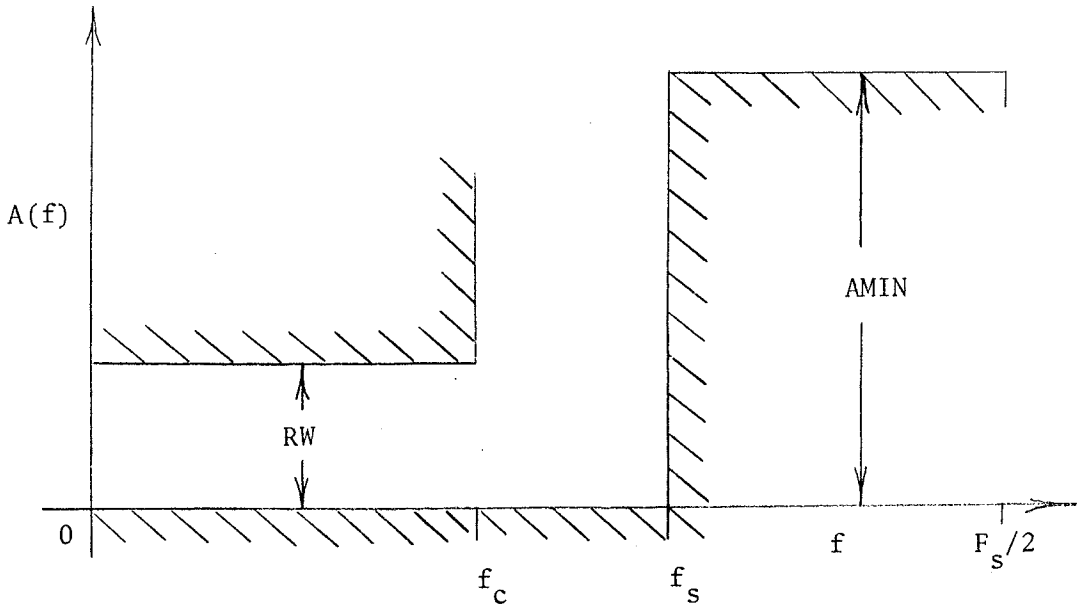
and suppose that $\hat{\beta}_2$ is outside the feasible region. Then, using (5.15-17)we obtain

$r_2 r_1$	COUNT	
1-1	2	
+ 1 0	3	← ΔCOUNT
1 | -1-1	5	

where $r_2 r_1$ =-1-1 is the 5th entry in the table, and the carry digit is ignored. The R vectors 10 and 11 were skipped over. A procedure similar to the above was used in [35] in reducing the number of complex multiplications in the computation of the discrete Fourier Transform (DFT).

5.1.2 Computation of Figure of Merit

To determine acceptability of a specific design each feasible set $\{ \hat{\beta}_i , i=1(1)M \}$ must be assigned a figure of merit (FM). To compute the FM, we first examine the specifications which are usually given in the form of a tolerance scheme in the frequency domain. The general lowpass case is shown in Fig.5.2.



RW —— ripple width

AMIN —— minimum allowable attenuation in the stopband

f_c —— passband corner

f_s —— stopband corner

F_s —— sampling frequency

A(f) —— attenuation characteristic in dB

Figure 5.2: Lowpass attenuation tolerance scheme.

In Fig.5.2, f is the discrete-time domain frequency variable ($F_s/2$ is the Nyquist frequency). To compute the figure of merit, we first evaluate A(f) at a few selected points in the passband and stopband. From these, we determine the following:

$$\begin{aligned} a_{max} &= \text{maximum attenuation in the passband} \\ a_{min} &= \text{minimum attenuation in the passband} \\ s_{min} &= \text{minimum attenuation in the stopband} \end{aligned} \tag{5.18}$$

Using (5.18), we define

$$FM \triangleq \max \left[\frac{a_{max} - a_{min}}{RW} \; , \; \frac{AMIN}{s_{min} - a_{min}} \right] \tag{5.19}$$

Clearly, designs that satisfy the specifications have $FM \leq 1$.

The time required to compute the FMs for all feasible designs can be greatly reduced if only a small number of points is examined (we suggest 4 points in both the pass and stopbands). Once the value of $COUNT_{max}$ is reached then, all the designs that tentatively satisfy the specifications are reexamined at 128 equally spaced points in the range $[0, F_s/2)$. Using this approach, the rate at which feasible designs that do not satisfy the specifications are rejected is increased.

The attenuation characteristic A(f), at the selected points, is evaluated using the analog prototype network, i.e.

$$A(f) = 20\log \left. \frac{E_1(j\Omega)}{V_2(j\Omega)} \right|_{\Omega = \tan(\pi f/F_s)} \qquad (5.20)$$

where E_1 is the voltage source at the input port and V_2 the voltage accross the output port. The conductance values, G_i i=1(1)n, are obtained from $\{ \hat{\beta}_i , \ i=1(1)M \}$ using an algorithm based on the formulae derived in Chapter IV. The frequency response algorithm can be easily obtained from the topology of the analog prototype. It is important that this algorithm compute the A(f) with the fewest number of multiplications and additions possible. This is because this algorithm is used extensively throughout the search. Also, for nonfeasible designs, the algorithm that computes the conductance values from the independent parameters must return the index value of the parameter that renders the set nonfeasible. In the case of multiple nonfeasible parameters, the highest index is chosen in order that the largest Δ COUNT, calculated using (5.17), is obtained. The listing of the search algorithm, written in FORTRAN WATFIV, is given in Appendix A. Also listed are examples of routines that compute the conductance values using (4.48) and A(f) for the 3rd-order elliptic prototype.

5.2 SUMMARY OF THE DESIGN PROCEDURE

The following points serve as a summary for the design of canonic WD filters:

1. Based on the specifications in the dicsrete-time domain, the corresponding requirements are obtained for the analog prototype using

$$\Omega = \tan(\pi f/F_s) \tag{5.21}$$

2. An analog prototype with specified element values is obtained using a suitable catalog or any other appropriate synthesis technique.
3. The analog prototype is denormalized (prewarped) using (5.21) as the frequency scaling factor. This, in effect, maps a critical analog frequency point (usually the passband corner) into the desired discrete-time frequency point.
4. The adaptors, which simulate the topology of the prototype, are selected. For most ladder designs, the adaptors derived in Chapter IV are sufficient. Also, if necessary, reflection-free ports are chosen.
5. For each adaptor, the nominal independent parameter set $\{ \beta_i , i=1(1)M \}$ is computed.
6. An algorithm that determines the feasibility of a design and computes the conductance values for the entire network is obtained from the conductance ratios formulae for each adaptor.

7. An algorithm that computes the attenuation characteristic is obtained using the topology of the analog prototype.
8. The integers m_i, s_i i=1(1)M, and the frequency points from which the FM is to be computed are chosen. These are supplied to the search algorithm which, using the algorithms from points 6 and 7, selects any suitable quantized designs.
9. Finally, a digital filter algorithm is obtained using the methods described in Sec.2.3.

5.3 DESIGN EXAMPLES

5.3.1 Example #1

Consider a lowpass characteristic with the following specifications:

$$f_c/F_s = 0.125 \qquad RW = 0.06 \text{ dB}$$

$$f_s/F_s = 0.3125 \qquad AMIN = 32.0 \text{ dB}$$

Using (5.21), the corresponding analog critical frequencies are:

$$\Omega_c = \tan(\pi f_c/F_s) = 0.41421$$

$$\Omega_s = \tan(\pi f_s/F_s) = 1.49661$$

The normalized value for the stopband corner is Ω_s/Ω_c =3.61313. Using Saal's catalog [54], the given speci-

fications can be satisfied with a 3rd-order elliptic characteristic designated by CC031017. With reference to Fig.4.6, the normalized and denormalized element values are:

normalized	denormalized
$G_1 = G_2 = 1.0$	$G_1 = G_2 = 1.0$
$G_3 = 0.97260$	$G_3 = 0.40286$
$G_4 = 0.063045$	$G_4 = 0.15220$
$G_5 = G_6 = 0.808974$	$G_5 = G_6 = 1.95304$

where, to denormalize, we used Ω_c as the frequency scaling factor. To design the corresponding WD filter, we choose the 3rd-order elliptic adaptor given by (4.46-48), i.e.

$$\beta_1 = \frac{G_1}{G_1 + G_5} = 0.33863 \qquad \beta_2 = \frac{1}{2 + \frac{G_1+G_5}{G_3+G_4}} = 0.046261$$

$$\beta_3 = \frac{G_3}{2(G_3 + G_4) + G_1 + G_5} = 0.09915$$

To ensure that $G_i>0$, i=1(1)6, we use (4.48) to derive

$$0 < \beta_3 < \beta_2/\beta_1 < \frac{1}{2} \quad , \quad 0 < \beta_1 < 1 \qquad (5.22)$$

as the necessary and sufficient conditions. A routine (written in FORTRAN) that checks for the above constraints and computes the conductance values is listed in Appendix A.

The attenuation characteristic is computed using the following algorithm:

let

$$Y_1 = G_1 + j\Omega G_5 \qquad \frac{e_1(j\Omega)}{v_2(j\Omega)} = \frac{Y_1(2 + Y_1 Z_2)}{G_1}$$

$$Z_2 = j\Omega/(G_3 - \Omega^2 G_4)$$

which is derived using Fig.4.6. This algorithm, written in FORTRAN, is also listed in Appendix A.

Approximating $\{ \beta_i \}_{i=1}^{3}$ with 5 bits, i.e. $m_1=m_2=m_3=5$, yields

$$\hat{\beta}_1 = \frac{11}{32} \quad , \quad \hat{\beta}_2 = \frac{1}{32} \quad , \quad \hat{\beta}_3 = \frac{3}{32}$$

and using (5.5,22), the numerators of the binary fractions can be allowed to vary within the following ranges:

$$p_1 \in [\ 11-10\ ,\ 11+20\ ] \quad \text{let} \quad s_1 = 20 \qquad b_1 = 41$$

$$p_2 \in [\ 1-0\ ,\ 1+14\ ] \quad \text{let} \quad s_2 = 14 \qquad b_2 = 29$$

$$p_3 \in [\ 3-2\ ,\ 3+12\ ] \quad \text{let} \quad s_3 = 12 \qquad b_3 = 25$$

where s_i , i=1,2,3 are chosen as the maximum allowable deviations. Using (5.9), we obtain $COUNT_{max}$ =29,725. The number of designs actually tested was 1739, i.e. 27,986 design parameter sets were rejected because these did not satisfy (5.22). The FMs were computed using 7 points: 4 in the passband including f_c and 3 in the stopband including f_s. The search was completed in 2.5 seconds of execution time (using the AMDAHL V/8 CPU). Out of 1739 feasible designs, 1 passed :

$$R = [\ 1\ ,\ 1\ ,\ 1\ ] \iff \hat{\beta} = \frac{1}{32}\ [\ 12\ ,\ 2\ ,\ 4\ ]$$

and using (4.48), we have

$$G_1 = G_2 = 6 \quad , \quad G_3 = 3 \quad , \quad G_4 = 1 \quad , \quad G_5 = G_6 = 10$$

The attenuation characteristic is displayed in Fig.5.3. With port numbering as shown in Fig.4.6, the state equations become

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \\ a_5(n+1) \\ a_6(n+1) \end{bmatrix} = \frac{1}{8} \begin{bmatrix} -3 & -1 & 2 & 9 & -1 \\ -1 & -3 & 2 & -1 & 9 \\ -4 & -4 & 4 & -8 & -8 \\ 5 & -1 & 2 & 1 & -1 \\ -1 & 5 & 2 & -1 & 1 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \\ a_3(n) \\ a_5(n) \\ a_6(n) \end{bmatrix}$$

where the redundant state a_4 has been removed. Applying the shift/add decomposition described in Sec.2.3.2 to the above matrix (with the second column deleted since $a_2(n)=0$) results in the following algorithm:

$$d_6 = a_1 + a_5$$

$$d_7 = a_6 - d_6$$

$$d_8 = a_3 - a_1$$

$$d_9 = a_5 + a_6$$

$$b_1(n) = ((-d_7/2 + a_3)/2 - a_1)/2 + a_5$$

$$b_2(n) = (d_7/2 + a_3)/4 + a_6$$

$$a_3(n+1) = d_8/2 - d_9$$

$$a_5(n+1) = ((-d_7/2 + a_3)/2 + a_1)/2$$

$$a_6(n+1) = (d_7/2 + a_3)/4$$

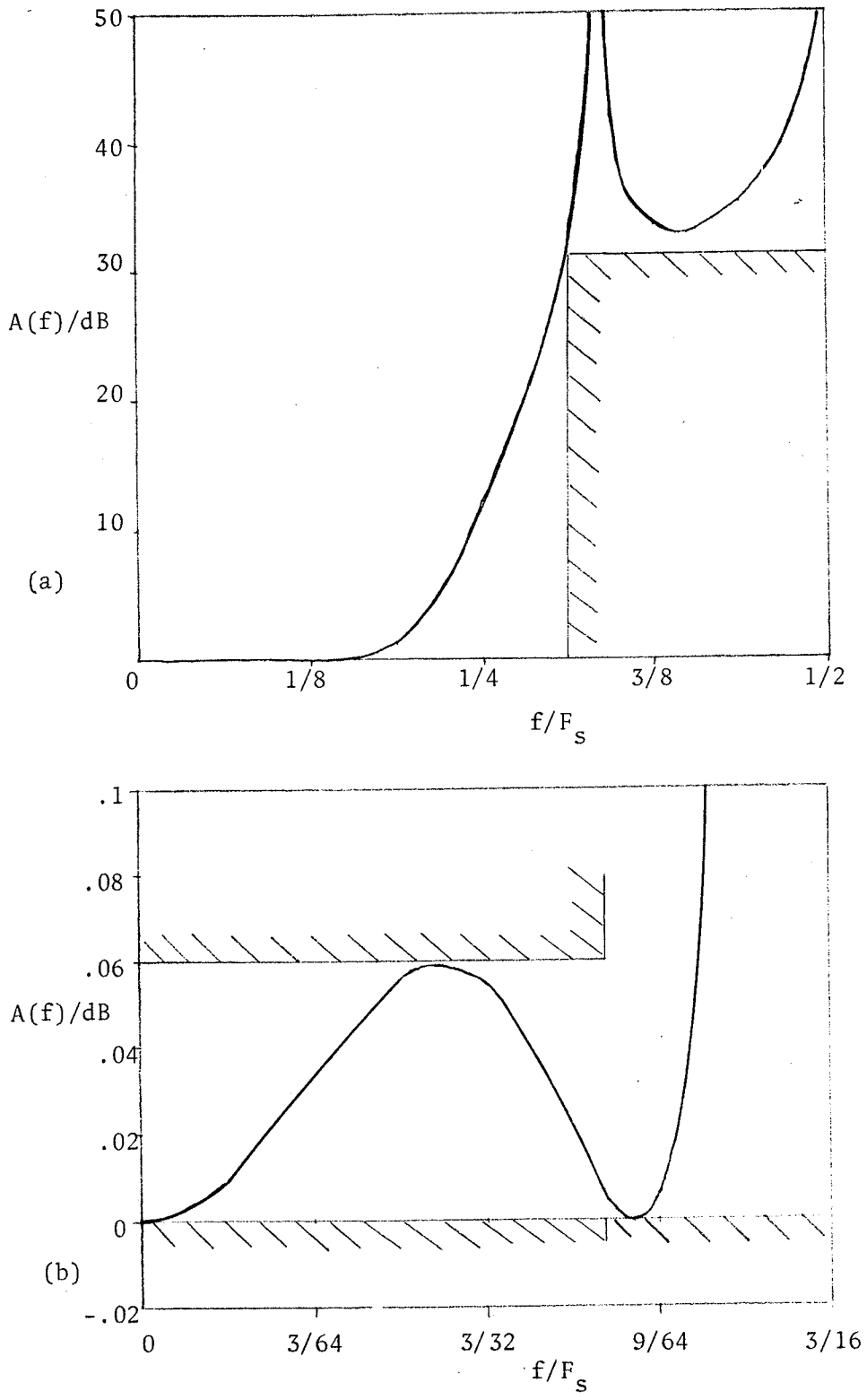


Figure 5.3: Attenuation characteristic for example #1: a) stopband, b) passband.

The above algorithm can be implemented with 11 adders. If we elect not to compute b_1, which is optional, then the count reduces to 9 adders. Employing magnitude truncation at the states guarantees suppression of the zero-input parasitic oscillations.

5.3.2 Example #2

Consider the following specifications:

f_c = 3.4 kHz RW = 0.3 dB

f_s = 4.6 kHz AMIN = 32.0 dB

F_s = 32.0 kHz

An interpolator which increases the sampling rate from 8 kHz to 32 kHz requires a lowpass filter with the above specifications to filter out the baseband [55,56]. From Saal [54], we have that a 5th-order elliptic characteristic designated by CC051548 and frequency scaled by

$$\Omega_c = \tan(\pi f_c/F_s) = 0.34677$$

satisfies the specifications. With reference to Fig.4.7, we have

normalized	denormalized
$G_1 = G_2 = 1.0$	$G_1 = G_2 = 1.0$
$G_3 = 0.86162$	$G_3 = 0.29878$
$G_4 = 1.24601$	$G_4 = 0.432077$
$G_5 = 0.209114$	$G_5 = 0.603034$
$G_6 = 0.643405$	$G_6 = 1.85542$
$G_7 = 0.983399$	$G_7 = 2.835884$
$G_8 = 1.52876$	$G_8 = 4.40858$
$G_9 = 0.704588$	$G_9 = 2.031861$

As an initial attempt, we choose the simplified 5th-order elliptic adaptor given by (4.84). Using (4.82), we can solve for G_1 and G_2, i.e.

$$G_1 = \frac{G_3 G_7}{G_5} = 1.40509 \qquad G_2 = \frac{G_4 G_9}{G_6} = 0.47316$$

We compute the corresponding parameters using (4.84):

$$\beta_1 = \frac{G_1}{G_1 + G_7} = 0.331313 \qquad \beta_2 = \frac{G_2}{G_2 + G_9} = 0.18889$$

$$\beta_3 = \frac{G_5}{G_5 + G_7} = 0.175356 \qquad \beta_4 = \frac{G_6}{G_6 + G_9} = 0.47731$$

$$\beta_5 = \frac{\beta_1}{1 + \frac{G_8 + \beta_4(G_2+G_9)}{\beta_3(G_1+G_7)}} = 0.038815 \qquad \beta_6 = \frac{\beta_2\beta_5}{\beta_1\beta_3(G_1+G_7)} = 0.035578$$

From (4.76) and (4.84), we have

$$\frac{G_1}{G_8} = \frac{c_1\beta_1}{\beta_3} \qquad \frac{G_2}{G_8} = \frac{c_2\beta_2}{\beta_4}$$

$$\frac{G_3}{G_8} = \frac{c_1\beta_1}{1-\beta_3} \qquad \frac{G_4}{G_8} = \frac{c_2\beta_2}{1-\beta_4}$$

$$\frac{G_5}{G_8} = \frac{c_1(1-\beta_1)}{1-\beta_3} \qquad \frac{G_6}{G_8} = \frac{c_2(1-\beta_2)}{1-\beta_4}$$

$$\frac{G_7}{G_8} = \frac{c_1(1-\beta_1)}{\beta_3} \qquad \frac{G_9}{G_8} = \frac{c_2(1-\beta_2)}{\beta_4}$$

$$c_1 = \frac{\beta_5\beta_1}{1-\beta_5/\beta_1-\beta_6/\beta_2} \qquad c_2 = \frac{\beta_6\beta_2}{1-\beta_5/\beta_1-\beta_6/\beta_2} \qquad (5.23)$$

and to ensure that $G_i > 0$, i=1(1)9, it is necessary and sufficient that

$$\begin{aligned} 0 < \beta_i &< 1 \quad , \quad i=1(1)4 \\ 0 < \beta_5 &< \beta_1 \\ 0 < \beta_6 &< \beta_2(1-\beta_5/\beta_1) \end{aligned} \qquad (5.24)$$

The attenuation characteristic is computed using the following algorithm, which was derived from Fig.4.7:

$$
\begin{aligned}
Y_1 &= G_1 + j\Omega G_7 & Y_4 &= 1 + Z_1 Y_1 \\
Z_1 &= j\Omega/(G_3 - \Omega^2 G_5) & Y_5 &= Y_1 + Y_2 Y_4 \\
Y_2 &= j\Omega G_8 & Y_6 &= Y_4 + Z_2 Y_5 \\
Y_3 &= G_2 + j\Omega G_9 & \frac{E_1(j\Omega)}{V_2(j\Omega)} &= \frac{Y_5 + Y_3 Y_6}{G_1} \\
Z_2 &= j\Omega/(G_4 - \Omega^2 G_6)
\end{aligned}
\qquad (5.25)
$$

The imposition of the element constraints changes the response of the nominal filter. If the resulting prototype does not satisfy given specifications, then, it is necessary to determine if a set of element values for the prototype exists that does satisfy the specifications and the two element constraints. If no such set can be found, then, a different adaptor must be used.

The optimization to determine the existence of an alternate set of element values can be performed with respect to either the element values or the corresponding parameters. We used the simplex algorithm [57] because it is easy to program and does not require evaluations of partial derivatives. For the present example, the optimized parameter set is:

$$
\begin{aligned}
\beta_1 &= 0.3560 \simeq \frac{3}{8} & \beta_2 &= 0.2016 \simeq \frac{1}{4} \\
\beta_3 &= 0.22453 \simeq \frac{1}{4} & \beta_4 &= 0.3310 \simeq \frac{3}{8} \\
\beta_5 &= 0.03991 \simeq \frac{10}{256} & \beta_6 &= 0.03956 \simeq \frac{10}{256}
\end{aligned}
$$

where we also give the initial binary fraction approximations. Using (5.24), the following ranges can be used:

$$s_1 = 4 \quad s_2 = 2 \quad s_3 = 2 \quad s_4 = 4 \quad s_5 = 10 \quad s_6 = 10$$
$$b_1 = 9 \quad b_2 = 5 \quad b_3 = 5 \quad b_4 = 9 \quad b_5 = 21 \quad b_6 = 21$$

Using (5.9), we obtain $COUNT_{max}$=893,025. The number of designs actually tested was 176,400, and it took 128 seconds of execution time to complete the search. Out of the designs tested 18 passed the specifications. These designs, however, turned out to be equivalent and differed only with respect to internal scaling levels. We chose

$$R = [\ -1\ 0\ 0\ -1\ 6\ -7\ ] \quad , \quad \hat{\beta} = [\ \tfrac{1}{4}\ \tfrac{1}{4}\ \tfrac{1}{4}\ \tfrac{1}{4}\ \tfrac{1}{16}\ \tfrac{3}{256}\ ]$$

with the corresponding conductance values obtained using (5.23):

$$G_1 = 48 \qquad G_3 = 16 \qquad G_5 = 48 \qquad G_7 = 144$$
$$G_8 = 135$$
$$G_2 = 9 \qquad G_4 = 3 \qquad G_6 = 9 \qquad G_9 = 27$$

The attenuation characteristic is shown in Fig.5.4. The state equations, with port numbering as shown in Fig.4.8, are derived using (3.38):

$$\begin{bmatrix} b_2(n) \\ a_3(n+1) \\ a_4(n+1) \\ a_5(n+1) \\ a_6(n+1) \\ a_7(n+1) \end{bmatrix} = \frac{1}{512} \begin{bmatrix} 16 & -16 & 61 & 0 & 768 & -237 \\ -144 & 400 & -9 & -768 & 0 & -711 \\ 48 & -48 & 439 & 0 & -768 & -711 \\ 192 & 64 & 0 & 256 & 0 & 0 \\ 0 & 0 & 64 & 0 & 256 & 0 \\ -64 & 64 & 12 & 0 & 0 & 436 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_3(n) \\ a_4(n) \\ a_5(n) \\ a_6(n) \\ a_7(n) \end{bmatrix}$$

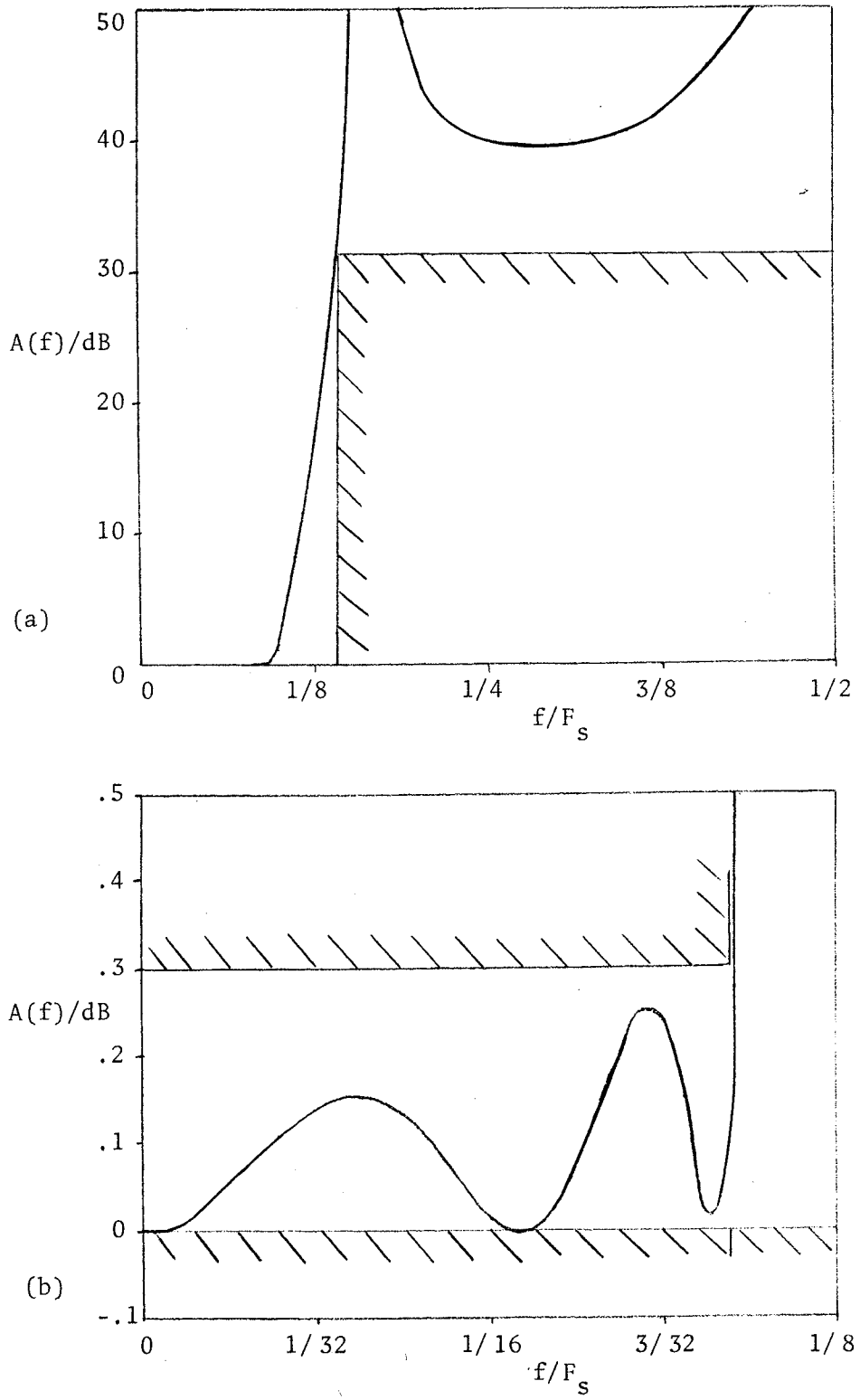


Figure 5.4: Attenuation characteristic for example #2: a) stopband, b) passband.

Applying the shift/add decomposition to the above matrix equation results in the following algorithm:

$$d_8 = a_4 - a_7 \qquad d_{11} = a_4 + a_7 \qquad d_{14} = a_1 + a_3$$
$$d_9 = a_1 - a_3 \qquad d_{12} = a_5 + a_7 \qquad d_{15} = a_1 + a_5$$
$$d_{10} = a_6 + a_7 \qquad d_{13} = a_7 + d_9 \qquad d_{16} = d_8 - d_9$$

$$b_2(n) = (((((\, d_8/4 - d_8)/4 + d_{13})/4 + a_4)/4 - d_{10})/4 + a_6)2$$

$$a_3(n+1) = (((((((-d_8/8 - d_{11})/2 - d_9)/4 + a_7)/2 - d_{14})/2 + d_{12})/2 + a_3)/2 - d_{12})2$$

$$a_4(n+1) = ((((((-d_8/8 - d_{11})/2 - d_9)/4 - d_{16})/4 + d_{10})/2 + a_4)/2 - d_{10})2$$

$$a_5(n+1) = (\, -d_9/4 + d_{15})/2$$

$$a_6(n+1) = (\, a_4/4 + a_6\,)/2$$

$$a_7(n+1) = ((\, -d_8/4 + d_8)/4 - d_{13})/8 + a_7$$

The above algorithm can be implemented using 28 adders. We can reduce the number of adders by employing the equivalent structure shown in Fig.4.13. Since $\beta_1 = \beta_2$ and $\beta_3 = \beta_4$, the scattering matrices for the Brune adaptors are equal. The state equations and their shift/add realizations for the Brune and parallel adaptor are given below:

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \\ a_4(n+1) \end{bmatrix} = \frac{1}{8} \begin{bmatrix} -3 & -2 & -1 & 12 \\ -8 & 0 & 8 & 0 \\ 3 & -6 & 1 & -12 \\ 3 & 0 & 1 & 4 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \\ a_3(n) \\ a_4(n) \end{bmatrix}$$

$$d_5 = a_1 - a_3$$

$$d_6 = a_1 + a_4$$

$$b_1(n) = (((\, d_5/2 - a_2)/2 - d_6)/4 + a_4)2$$

$$b_2(n) = -d_5$$

$$a_3(n+1) = ((((\, -d_5/2 + a_2)/2 + d_6)/2 - a_2)/2 - a_4)2$$

$$a_4(n+1) = (\, -d_5/4 + d_6)/2$$

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \end{bmatrix} = \frac{1}{128} \begin{bmatrix} -112 & 3 & 237 \\ 16 & -125 & 237 \\ 16 & 3 & 109 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \\ a_3(n) \end{bmatrix} \quad \begin{aligned} d_4 &= a_2 - a_3 \\ d_5 &= a_1 - a_3 \end{aligned}$$

$$b_1(n) = ((((-d_4/4+d_4)/4+d_5)/2+a_3)/2+a_3)/2+d_5$$

$$b_2(n) = ((((-d_4/4+d_4)/4+d_5)/2+a_3)/2+a_3)/2-d_4$$

$$a_3(n+1) = ((((-d_4/4+d_4)/4+d_5)/2+a_3)/2+a_3)/2$$

With respect to Fig.4.13, we have that the left-hand-side Brune adaptor requires 7 adders (computation of b_1 is not required), the parallel adaptor 8 adders, and the right-hand-side Brune adaptor 6 adders ($a_1=0$) which brings the total to 21 adders. The structure is operated as follows: compute

1. reflected waves at ports #2 from both Brune adaptors,
2. reflected waves from all ports in the parallel adaptor,
3. all the remaining reflected waves from both Brune adaptors.

Also, the reflected waves from the delay-terminated ports become the incident waves at the next sampling instant.

5.3.3 Example #3

A lowpass filter, with specifications as shown in Fig.5.5, is used in an interpolator that increases the sampling rate from 8 kHz to 64 kHz [58]. From Saal [54], we have that a

5th-order elliptic characteristic designated by CC055048 and frequency scaled by

$$\Omega_c = \tan(3.4\pi/64.0) = 0.16846$$

satisfies these specifications. With reference to Fig.4.7, we have:

	normalized	denormalized
	$G_1 = G_2 = 1.0$	$G_1 = G_2 = 1.0$
	$G_3 = 1.12338$	$G_3 = 0.18925$
	$G_4 = 1.49094$	$G_4 = 0.25117$
	$G_5 = 0.272642$	$G_5 = 1.6184$
	$G_6 = 0.769882$	$G_6 = 4.57$
	$G_7 = 2.09392$	$G_7 = 12.43$
	$G_8 = 2.49416$	$G_8 = 14.805$
	$G_9 = 1.743254$	$G_9 = 10.348$

As an initial attempt, we choose the simplified 5th-order elliptic adaptor given by (4.84). Using (4.82), we obtain

$$G_1 = 1.45345 \qquad G_2 = 0.568727$$

We compute the corresponding parameters using (4.84):

$$\beta_1 = 0.104694 \simeq \frac{3}{32} \qquad \beta_2 = 0.052097 \simeq \frac{2}{32}$$

$$\beta_3 = 0.115206 \simeq \frac{1}{8} \qquad \beta_4 = 0.306343 \simeq \frac{2}{8}$$

$$\beta_5 = 0.008479 \simeq \frac{4}{512} \qquad \beta_6 = 0.008822 \simeq \frac{5}{512}$$

where we also give the initial binary fraction approximations. The nominal design, with the two element constraints, still satisfies the specifications and, therefore, optimization is unnecessary. The conductance values, parameter con-

straints, and the attenuation—characteristic algorithm are given by (5.23,24,25), respectively. Using (5.24), the following ranges can be used:

$$s_1 = 5 \quad s_2 = 4 \quad s_3 = 4 \quad s_4 = 4 \quad s_5 = 4 \quad s_6 = 4$$

$$b_1 = 11 \quad b_2 = 9 \quad b_3 = 9 \quad b_4 = 9 \quad b_5 = 9 \quad b_6 = 9$$

Using (5.9), we obtain $COUNT_{max}$=649,539. The number of designs actually tested was 103,590, and it took 87 seconds of execution time to complete the search. Out of the designs tested, 2 passed the specifications. These designs, however, turned out to be equivalent and differed only with respect to internal scaling levels. We chose

$$R = [\ 0\ 0\ 0\ 0\ 0\ -1\ ] \quad , \quad \hat{\beta} = [\ \tfrac{3}{32}\ \ \tfrac{1}{16}\ \ \tfrac{1}{8}\ \ \tfrac{1}{4}\ \ \tfrac{1}{128}\ \ \tfrac{1}{128}\ ]$$

with the corresponding conductance values obtained using (5.23): $G_1 = 42$ $G_3 = 6$ $G_5 = 58$ $G_7 = 406$ $G_8 = 532$ $G_2 = 21$ $G_4 = 7$ $G_6 = 105$ $G_9 = 315$

The attenuation characteristic is shown in Fig.5.5. The state equations, with port numbering as shown in Fig.4.8, are derived using (3.38):

$$\begin{bmatrix} b_2(n) \\ a_3(n+1) \\ a_4(n+1) \\ a_5(n+1) \\ a_6(n+1) \\ a_7(n+1) \end{bmatrix} = \frac{1}{512} \begin{bmatrix} 2 & -2 & 14 & 0 & 960 & -252 \\ -77 & 493 & -7 & -928 & 0 & -882 \\ 6 & -6 & 490 & 0 & -960 & -756 \\ 84 & 12 & 0 & 416 & 0 & 0 \\ 0 & 0 & 16 & 0 & 448 & 0 \\ -8 & 8 & 8 & 0 & 0 & 496 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_3(n) \\ a_4(n) \\ a_5(n) \\ a_6(n) \\ a_7(n) \end{bmatrix}$$

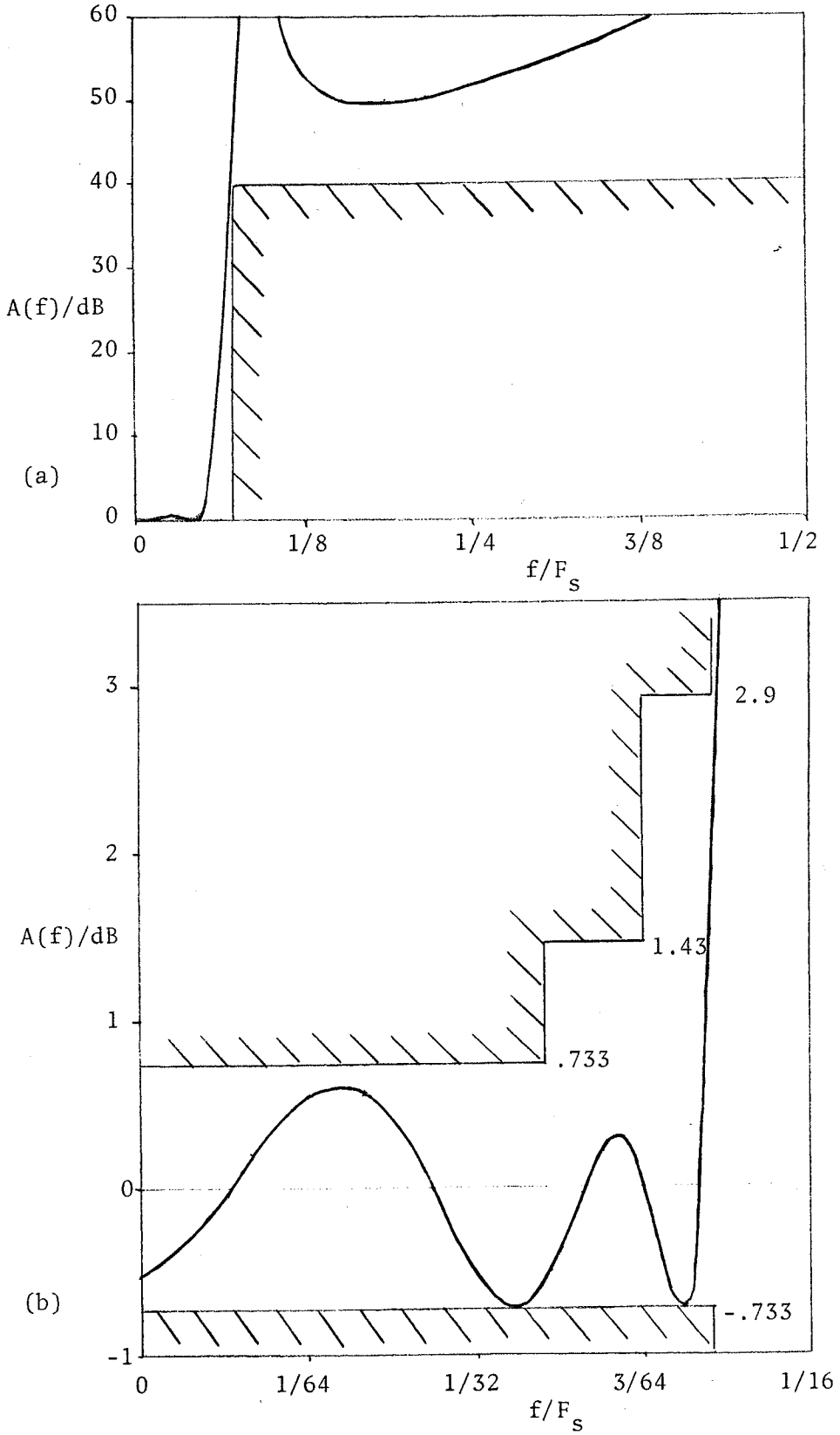


Figure 5.5: Attenuation characteristic for example #3: a) stopband, b) passband.

Applying the shift/add decomposition to the above matrix equation results in the following algorithm:

$$d_8 = a_1 - a_3 \qquad d_{11} = a_5 + a_7 \qquad d_{14} = a_7 - d_{10}$$
$$d_9 = a_4 - d_8 \qquad d_{12} = a_4 + d_8$$
$$d_{10} = a_1 + a_3 \qquad d_{13} = a_6 + a_7$$

$$b_2(n) = (((((-d_9/2+a_7)/4+a_4)/4-a_6)/4-a_7)/4+a_6)2$$

$$a_3(n+1) = (..(d_9/2-a_7)/2+d_8)/2-a_4)/2+d_{14})/2-a_5)/2-a_1)/2+d_{11})/4+a_3)/2-d_{11})2$$

$$a_4(n+1) = (..(d_9/2-a_7)/2+d_{12})/2+a_7)/2-a_4)/2+a_6)/4+a_7)/2+a_4)/2-d_{13})2$$

$$a_5(n+1) = ((((d_8/4+d_{10})/2+a_5)/2+a_1)/2-a_5)/4+a_5$$

$$a_6(n+1) = (a_4/4 - a_6)/8 + a_6$$

$$a_7(n+1) = (d_9/2 - a_7)/32 + a_7$$

The above algorithm can be implemented using 35 adders. We can reduce the number of adders by employing the equivalent structure shown in Fig.4.13. The state equations and their shift/add realizations for the two Brune and parallel adaptors are given below:

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \\ a_4(n+1) \end{bmatrix} = \frac{1}{128} \begin{bmatrix} -91 & -16 & -13 & 232 \\ -128 & 0 & 128 & 0 \\ 91 & -112 & 13 & -232 \\ 21 & 0 & 3 & 104 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \\ a_3(n) \\ a_4(n) \end{bmatrix}$$

$$d_5 = a_1 - a_3$$
$$d_6 = a_1 + a_3$$
$$d_7 = a_2 + a_3$$
$$d_8 = a_1 - a_4$$
$$d_9 = a_1 - a_2$$

$$b_2(n) = -d_5$$

$$a_3(n+1) = (..(-d_5/4-d_6)/2-a_4)/2+d_7)/2-d_8)/4+d_9)/2-a_4)2$$

$$a_4(n+1) = ((((d_5/4+d_6)/2+a_4)/2+a_1)/2-a_4)/4+a_4$$

computation of b_1 is optional, and is omitted.

Parallel adaptor:

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \end{bmatrix} = \frac{1}{64} \begin{bmatrix} -63 & 1 & 126 \\ 1 & -63 & 126 \\ 1 & 1 & 62 \end{bmatrix} \begin{bmatrix} a_1(n) \\ a_2(n) \\ a_3(n) \end{bmatrix} \quad d_4 = a_1 + a_2$$

$$b_1(n) = (((\, d_4/2 - a_3)/32 - a_1)/2 + a_3)2$$

$$b_2(n) = (((\, d_4/2 - a_3)/32 - a_2)/2 + a_3)2$$

$$a_3(n+1) = (\, d_4/2 - a_3)/32 + a_3$$

Right-hand-side Brune adaptor:

$$\begin{bmatrix} b_1(n) \\ b_2(n) \\ a_3(n+1) \\ a_4(n+1) \end{bmatrix} = \frac{1}{32} \begin{bmatrix} -21 & -8 & -7 & 60 \\ -32 & 0 & 32 & 0 \\ 21 & -24 & 7 & -60 \\ 3 & 0 & 1 & 28 \end{bmatrix} \begin{bmatrix} 0 \\ a_2(n) \\ a_3(n) \\ a_4(n) \end{bmatrix} \quad d_5 = a_2 + a_3$$

$$b_1(n) = (((\, a_3/4 - a_4)/2 - d_5)/8 + a_4)2$$

$$b_2(n) = a_3$$

$$a_3(n+1) = ((((\, -a_3/4 + a_4)/2 + d_5)/4 - a_2)/2 - a_4)2$$

$$a_4(n+1) = (\, a_3/4 - a_4)/8 + a_4$$

Note that $a_1(n)=0$.

With respect to Fig.4.13, we have that the left-hand-side Brune adaptor requires 14 adders (computation of b_1 is not required), the parallel adaptor 7 adders, and the right-hand-side Brune adaptor 7 adders ($a_1=0$), which brings the total to 28 adders. The operation of the structure was given in Example #2.

Chapter VI

CONCLUSIONS AND RECOMMENDATIONS

This thesis has proposed two methods of designing canonic WD filters which suppress all types of zero-input parasitic oscillations. The first method is based on the exact diagonalization of the nondiagonal reference conductance matrix that results when redundant delays, due to capacitance -only loops in the analog prototype, are removed from the WD structure. The second method synthesizes a minimal analog prototype via the network equivalence transformation. The nonminimal prototype, which is usually a ladder, is used in defining the design parameters. The resulting WD structure is based on the canonic number of design parameters, which is equal to the number of degrees of freedom, and consists of the canonic number of delays which is equal to the order of the filter. The second method is recommended because it is conceptually simpler and involves a fewer number of steps.

The process of designing canonic WD adaptors produces entries in S which are rational functions of the independent design parameters. It was shown that it is possible to redefine these parameters such that the entries in S are sums of products (SOP) of the new set of parameters. The SOP re-

quirement is sufficient to ensure that the resulting state equations are implementable using digital components. Canonic designs for the Brune, 3rd-, and 5th-order elliptic topologies were presented, and these can be used in obtaining higher-order structures. Also, it seems clear that the method of obtaining the SOP form can be extended to other prototype topologies.

The canonic WD adaptors presented in this thesis are based on diagonal reference conductance matrices. Thus, sign-magnitude truncation at the delays (states) is sufficient to guarantee suppression of zero-input parasitic oscillations. Example #2 in Sec.5.2 was simulated in real-time using a microprocessor-based system (the filtering algorithm was encoded as a program). No limit cycles were observed under zero-input conditions.

A practical implementation of a digital filter requires that the filter coefficients be quantized to finite word length binary numbers. It was proposed that short coefficient word lengths can be obtained for canonic WD filters using a simple search algorithm. The design examples considered showed that it is indeed possible to obtain very short coefficient word lengths which leads to a correspondingly moderate amount of hardware in the realization.

A disadvantage of our proposed search method is that it is exhaustive in nature, and consequently, high-order examples require excessive amounts of execution time. As an al-

ternative, we suggest as further research a method that is based on a "branch and bound" type of an algorithm where the design parameters are quantized sequentially and the remaining parameters are reoptimized using any suitable continuous nonlinear optimization method, e.g., using the simplex algorithm [57].

The reactive redundancies in the analog prototype that were considered in this thesis are due to capacitance-only loops. Other network equivalence transformations should be derived that effectively eliminate redundancies due to both types of reactive cutsets and inductance-only loops.

Appendix A

LISTING OF THE SEARCH PROGRAM

```
C THIS IS A GENERAL OPTIMIZATION ROUTINE BASED ON EXHAUSTIVE SEARCH
C DATA TO BE SUPPLIED :
C   (1) N - NUMBER OF PARAMETERS
C   (2) N1 - NUMBER OF BEST SOLUTIONS PER TRIAL RUN
C   (3) N3 - NUMBER OF (G) CONDUCTANCE RATIOS
C   (4) R1 - R1=1. DONOT DIVIDE ERROR CALCULATIONS BY DENOMINATORS
C            R1=2. DIVIDE ERROR CALCULATIONS BY DENOMINATORS
C   (5) NP(N) - NOMINAL PARAMETER ARRAY
C   (5) P(N) - INITIAL APPROXIMATION PARAMETER SET
C   (6) NV - # OF VARIABLE PARAMETRS
C   (7) V(NV) - ARRAY WITH INDECES OF VARIABLE PARAMETERS
C   (8) IP(NV) - ARRAY WITH RADICES OF VARIABLE PARAMETERS
C   (9) N2 - NUMBER OF FREQUENCY POINTS TO BE EXAMINED IN PASSBAND
C   (10) N4 - TOTAL # OF FREQUENCY POINTS TO BE EXAMINED ( >= N2 )
C   (11) RW - MAXIMUM ATTENUATION IN THE PASSBAND
C   (12) AMIN - MINIMUM ATTENUATION IN THE STOPBAND
C   (13) FS - SAMPLING FREQUENCY
C   (14) W(N2) - FREQUENCY POINTS TO BE EXAMINED
C THE PROGRAM PROVIDES FOR EACH TRIAL RUN THE FOLLOWING INFORMATION :
C   (1) P1(N,2) - THE INITIAL RATIONAL APPROXIMATION PARAMETER ARRAY
C   (2) E(N) - PERCENT ERROR ARRAY
C   (3) IC3 - COUNTS THE TOTAL NUMBER OF TRIED PARAMETER SETS
C   (4) IC4 - COUNTS THE TOTAL NUMBER OF TRIED DESIGNS
C   (5) N1 SETS OF: (I) FO(I) - OPTIMUM OBJECTIVE FUNCTION VALUE
C                   (II) KO(I,J) - OPTIMAL K(N) ARRAY
C                   (III) GO(I,J) - OPTIMUM GR(N) ARRAY
C THE SEARCH IS STOPPED AFTER A DESIGN SATISFYING FREQUENCY SPECS
C IS FOUND
C ---------------------------------------------------------------
      INTEGER V(20),IP(20),IR(20),NB(20)
      REAL NP(20),P1(20,2),P(20),E(20),K(20),KO(300,20),GR(20),W(20)
      REAL X2(20),S(128),AT(128),COR(10),ATT(10),XF(128)
      LOGICAL R2,FINISH
C ---------------------------------------------------------------
      READ,N,N3,FVMAX,R1,(NP(I),P(I),I=1,N)
      READ,NV,(V(I),IP(I),NB(I),I=1,NV)
      READ,N2,N4,FMAX,FMIN,FS,(W(I),I=1,N4)
      READ,NSPEC
      IF(NSPEC.NE.0) READ,(COR(I),ATT(I),I=1,NSPEC)
      CALL EVALG(NV,V,NP,GR,R2,L1)
      PRINT 1,N,R2
      DO 5 I=1,N
5     PRINT,NP(I),P(I)
      PRINT,'NOMINAL G RATIOS'
```

```
      DO 9 I=1,N3
9     PRINT,I,GR(I)
      PRINT,'MAXIMUM OBJECTIVE FUNCTION VALUE=',FVMAX
      PRINT,'THE VARIABLE R1 IS = ',R1
      PRINT,'# OF FREQUENCY POINTS EXAMINED=',N4
      PRINT,'MAXIMUM PASSBAND ATTENUATION=',FMAX
      PRINT,'MINIMUM STOPBAND ATTENUATION=',FMIN
      PRINT,'SAMPLING FREQUENCY=',FS
      PRINT,'NUMBER OF PARAMETERS TO BE VARIED=',NV
      NUM=1
      DO 16 I=1,NV
      IR(I)=NUM
      NUM=NUM*IP(I)
      X2(I)=FLOAT(IP(I)/2)
16    PRINT,V(I),IP(I),IR(I),NB(I)
      PRINT,'MAX NUMBER OF ITERATIONS PER TRIAL RUN =',NUM
      PRINT,'NUMBER OF EXTRA SPECS IN THE PASSBAND = ',NSPEC
      IF(NSPEC.NE.0) PRINT,(COR(I),ATT(I),I=1,NSPEC)
      PRINT 14
      PI=3.14159265  ; N5=N2+1
      IPASS=INT(W(1))+1
      ISTOP=INT(W(N5))+2
      PRINT,'IPASS=',IPASS,'  ISTOP=',ISTOP
      DO 10 I=1,N4
      W1=TAN(PI*W(I)/FS)
      CALL FREQ(GR,W1,FP)
      PRINT 13,W(I),FP
10    W(I)=W1
      CALL FRRS(GR)
      AT(1)=AT(65)=0.0
      DO 17 I=1,128
      S(I)=I-1.
17    XF(I)=TAN(PI*S(I)/256.)
C -------------------------------------------------------------------
      DO 15 I=1,NV
      NP(I)=P(V(I))
      P1(I,2)=2.0**NB(I)
      P1(I,1)=AINT(P1(I,2)*NP(I)+0.5)
      IF(P1(I,1).EQ.0.0) P1(I,1)=1.
      E(I)=100.*ABS(1.-P1(I,1)/P1(I,2)/NP(I))
      IF(R1.EQ.2.) E(I)=E(I)/P1(I,2)
15    CONTINUE
      IC1=IC2=0 ;  PT=8. ; M=1
C -------------------------------------------------------------------
100   IC3=IC4=0 ; IC1=IC1+1 ; L1=1 ; K2=K3=1 ; N1=0
      DO 30 I=1,NV
30    P(V(I))=P1(I,1)/P1(I,2)
      CALL EVALG(NV,V,P,GR,R2,L1)
      DO 32 J=1,NV
32    K(J)=0.0
      PRINT 2,IC1,M,PT
      PRINT 3,(P1(I,1),I=1,NV)
      PRINT 3,(P1(I,2),I=1,NV)
      PRINT 12,(E(I),I=1,NV)
```

```
C ------------------------------------------------------------------
      NUM1=0
35    K2=1
      DO 40 J=L1,NV
      K(J)=K(J)+1.
      IF(K(J).LE.X2(J))GO TO 45
40    K(J)=K(J)-IP(J)
45    K2=MAXO(K2,MINO(NV,J))
      NUM1=NUM1+IR(L1)
      IF(L1.EQ.1)GO TO 46
      L2=L1-1
      DO 47 J=1,L2
      DF=K(J)+X2(J)
      IF(DF.NE.0.0) NUM1=NUM1-DF*IR(J)
47    K(J)=-X2(J)
46    IF(NUM1.GT.NUM)GO TO 70
      K3=MAXO(K3,K2)
      L1=M
      IF(AMOD(ABS(K(M)),2.).EQ.PT)GO TO 35
      DO 50 I=1,K3
50    P(V(I))=(P1(I,1)+K(I))/P1(I,2)
      DO 51 I=1,K3
      L1=K3+1-I
51    IF(P(V(L1)).LE.0.0)GO TO 35
      CALL EVALG(K3,V,P,GR,R2,L1)
      K3=1
      IC3=IC3+1
      IF(.NOT.R2)GO TO 37
      IC2=IC2+1
      IC4=IC4+1
C ------------------------------------------------------------------
      F=F1=F2=0.0
      DO 60 I=1,N2
      W1=W(I)
      CALL FREQ(GR,W1,FP)
      F1=AMAX1(F1,FP)
      F2=AMIN1(F2,FP)
      F3=(F1-F2)/FMAX
      F=AMAX1(F,F3)
60    IF(F.GT.FVMAX)GO TO 37
      DO 61 I=N5,N4
      W1=W(I)
      CALL FREQ(GR,W1,FP)
      F3=FMIN/(ABS(FP-F2)+1.E-20)
      F=AMAX1(F,F3)
61    IF(F.GT.FVMAX)GO TO 37
C ------------------------------------------------------------------
      N1=N1+1
      DO 75 J=1,NV
75    KO(N1,J)=K(J)
      IF(F.LE.1.0) PRINT 6,N1,F,(K(I),I=1,NV)
37    IF(NUM1.LT.NUM)GO TO 35
C ------------------------------------------------------------------
70    PRINT 4,IC3,IC4
```

```
      PRINT,N1,'  DESIGNS ARE CONSIDERED'
      IF(N1.EQ.0) GO TO 250
      J2=0
      FLOW=FVMAX
      DO 105 I=1,N1
      DO 110 J=1,NV
110   P(V(J))=(P1(J,1)+KO(I,J))/P1(J,2)
      CALL EVALG(NV,V,P,GR,R2,L1)
      W1=W(1)
      CALL FREQ(GR,W1,FP)
      F=F1=F2=0.0
      F1=AMAX1(F1,FP)
      F2=AMIN1(F2,FP)
      DO 115 J=2,128
      IF(S(J).EQ.64.) GO TO 115
      W1=XF(J)
      CALL FREQ(GR,W1,FP)
      AT(J)=FP
      F2=AMIN1(F2,FP)
      IF(J.GT.IPASS) GO TO 120
      F1=AMAX1(F1,FP)
120   F3=(F1-F2)/FMAX
      F=AMAX1(F,F3)
      IF(F.GT.FVMAX) GO TO 105
      IF(J.LT.ISTOP) GO TO 115
      F3=FMIN/(FP-F2)
      F=AMAX1(F,F3)
      IF(F.GT.FVMAX) GO TO 105
115   CONTINUE
      W1=W(N5)
      CALL FREQ(GR,W1,FP)
      F3=FMIN/(FP-F2)
      F=AMAX1(F,F3)
      IF(F.GT.FVMAX) GO TO 105
      IF(NSPEC.EQ.0) GO TO 125
      DO 130 L=1,NSPEC
      J1=INT(COR(L))+1
      W1=TAN(PI*COR(L)/FS)
      CALL FREQ(GR,W1,F1)
      F2=AMIN1(F2,F1)
      DO 135 J=2,J1
      F1=AMAX1(F1,AT(J))
      F3=(F1-F2)/ATT(L)
      F=AMAX1(F,F3)
135   IF(F.GT.FVMAX) GO TO 105
130   CONTINUE
125   FLOW=AMIN1(FLOW,F)
      J2=J2+1
      PRINT 201,J2
      PRINT 6,I,F,(KO(I,J),J=1,NV)
      PRINT 3,(KO(I,J)+P1(J,1),J=1,NV)
      PRINT 3,(P1(J,2),J=1,NV)
      DO 210 L=1,N3
210   PRINT 202,L,GR(L)
```

```
      PRINT,'MIN MAX ATTEN(DB) DETECTED',F2,F1
      PRINT 203
      DO 215 L=1,32
215   PRINT 204, (S(L+32*(J-1)),AT(L+32*(J-1)),J=1,4)
      DO 220 L=1,N4
      W1=W(L)
      CALL FREQ(GR,W1,FP)
      WD=ATAN(W1)*256./PI
220   PRINT,'XF=',WD,'  ATT(DB)=',FP
      IF(NSPEC.EQ.0) GO TO 105
      DO 225 L=1,NSPEC
      W1=TAN(PI*COR(L)/FS)
      CALL FREQ(GR,W1,FP)
225   PRINT,'XF=',COR(L),'  ATT(DB)=',FP
105   CONTINUE
      IF(INT(100.*FLOW).LE.100) GO TO 200
250   EM=0.0
      DO 90 I=1,NV
      IF(E(I).LE.EM)GO TO 90
      EM=E(I) ; M=I
90    CONTINUE
      P1(M,2)=P1(M,2)*2.
      P1(M,1)=AINT(P1(M,2)*NP(M)+0.5)
      IF(P1(M,1).EQ.0.0) P1(M,1)=1.
      E(M)=100.*ABS(1.-P1(M,1)/P1(M,2)/NP(M))
      IF(R1.EQ.1.)GO TO 95
      E(M)=E(M)/P1(M,2)
95    PT=AMOD(P1(M,1),2.)
      GO TO 100
C -----------------------------------------------------------------
200   PRINT 8,IC2
      PRINT,'LOWEST OBJECTIVE FUNCTION VALUE = ',FLOW,
     *'  TOTAL NUMBER OF PRINTED SOLUTIONS=',J2
      STOP
1     FORMAT('1','THERE ARE ',I2,' PARAMETERS AND THE NOMINAL SET IS',
     *L2//' ','NOMINAL PARAMETERS',5X,'INITIAL APPROXIMATIONS'//)
2     FORMAT('1','TRIAL #',I3,' WITH STARTING PARAMETER SET',I3,F4.0)
3     FORMAT('0',13X,20F4.0)
4     FORMAT('-','# TRIED PARAMETER SETS',I6,' # OF TRIED DESIGNS',I5)
6     FORMAT('-',I3,F8.5,2X,20F4.0)
8     FORMAT('-',' SEARCH HAS ENDED WITH TOTAL # OF TRIED DESIGNS',I6)
12    FORMAT('-',20F8.3)
13    FORMAT(' ',10X,F5.1,5X,F9.4)
14    FORMAT('0','FREQUENCY POINTS EXAMINED AND THE CORRESPONDING ',
     *'ATTENUATION')
201   FORMAT('1','DESIGN #',I10)
203   FORMAT('-',10X,4('FREQ',5X,'ATTEN(DB)',5X)//)
202   FORMAT(' ',I3,F12.7)
204   FORMAT(' ',10X,4(F4.0,5X,F9.4,5X))
      END
C -----------------------------------------------------------------
      SUBROUTINE FRRS(GR)
      REAL GR(20),S(4),AT(4)
      PI=1.227185E-02
```

```
      PRINT 1
      DO 10 I=1,32
      DO 20 J=1,4
      S(J)=I-1.+32.*(J-1)
      IF(S(J).EQ.64.)GO TO 20
      W=TAN(PI*S(J))
      CALL FREQ(GR,W,FP)
20    AT(J)=FP
10    PRINT 2,(S(J),AT(J),J=1,4)
1     FORMAT('-',10X,4('FREQ',5X,'ATTEN(DB)',5X)//)
2     FORMAT(' ',10X,4(F4.0,5X,F9.4,5X))
      RETURN
      END
C THIS PROGRAM INCLUDES THE ROUTINES REQUIRED FOR THE OPTIMIZATION
C PROGRAM FOR A 3TH ORDER ELLIPTIC FILTER
      SUBROUTINE EVALG(NV,V,P,GR,R2,L)
      INTEGER V(20)
      REAL P(20),GR(20)
      LOGICAL R2
      R2=.FALSE.
      L=1
      IF(P(1).GE.1.0)GO TO 15
      C1=P(2)/P(1)
      IF(C1.GE.0.5)GO TO 15
      IF(P(3).GE.C1)GO TO 15
      C2=P(1)-2*P(2)
      GR(3)=P(3)/C2
      GR(4)=(C1-P(3))/C2
      GR(5)=GR(6)=(1-P(1))/P(1)
      GR(1)=GR(2)=1.0
      R2=.TRUE.
15    RETURN
      END
C ---------------------------------------------------------------------
      SUBROUTINE FREQ(GR,W,FP)
      REAL GR(20)
      COMPLEX Y(6),Z(2)
      W2=W*W
      Y(1)=CMPLX(GR(1),W*GR(5))
      Z(1)=CMPLX(0.0,W/(GR(3)-W2*GR(4)))
      Y(3)=(2.,0.)+Y(1)*Z(1)
      Y(3)=Y(1)*Y(3)
      FP=CABS(Y(3))/GR(1)/2.0
      FP=20.0*ALOG10(FP)
      RETURN
      END
$ENTRY
3 6 1.00 1.
0.3386300  0.338630
0.0462600  0.0462600
0.0991500  0.099150
3  1 41 5  2 29 5  3 25 5
4 7 0.060 32.0 256.  32.0 24. 20. 16.0 80. 090. 100.
0
```

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