# A TRAVELLING-WAVE RELAY FEATURING FAULT CLASSIFICATION AND PHASE SELECTION

by

MOHAMED MOHAMED SAYED MANSOUR

B.Sc., Ain-Shams University, Egypt, 1975
M.Sc., Ain-Shams University, Egypt, 1980

A thesis
presented to the University of Manitoba
in partial fulfillment of the
requirements for the degree of
DOCTOR OF PHILOSOPHY
in
ELECTRICAL ENGINEERING

Winnipeg, Manitoba

# A TRAVELLING-WAVE RELAY FEATURING FAULT CLASSIFICATION AND PHASE SELECTION

BY

MOHAMED M. SAYED MANSOUR

A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

DOCTOR OF PHILOSOPHY

TO MY PARENTS

ABSTRACT

The basis of a new travelling wave protection principle to be used as an ultra high speed (UHS) digital transmission line relaying scheme with phase selection and fault classification capabilities is presented in this study. Verification of the relay operating principle under practical conditions is presented through digital computer numerical simulation using an electromagnetic transients program (EMTP) in conjunction with a simulation of the proposed principle. Parallel digital processing is incorporated through multi-microprocessor implementation. Hardware and software of a multiprocessor prototype are managed in a way to fit the algorithm requirements in as simple a construction as possible. A digitized real time testing system is presented for testing travelling wave-based relays in particular and any other HS/UHS relay type in general. Testing the implemented laboratory prototype through this system shows good practical response under different situations.

It is felt that the proposed protection scheme with its superior capabilities will cope with modern power system protection requirements.

ACKNOWLEDGEMENTS

I gratefully acknowledge the help and supervision I have received from Dr. G.W. Swift, whom I admire, throughout the course of this study.

I am indebted to Mr. K. Biegun for his assistance with the micro-computer hardware, and to Mr. A. McKay who helped in setting up the testing device. Thanks to Mr. J. Sill for his suggestions about realizing and assembling the relay hardware.

Financial assistance from Manitoba Hydro and the Natural Sciences and Engineering Research Council are gratefully acknowledged.

Finally, my sincere thanks to my wife for her great support and unexpected patience during the time of this work.

CONTENTS

LIST OF FIGURES

## LIST OF TABLES

# Chapter I

## INTRODUCTION

Transmission of electric power through long UHV/EHV lines is often required in order to achieve successful operation of modern bulk interconnected electric power systems. The emergence of these UHV overhead lines and EHV cables presents some new and difficult problems to the conventional protective devices. These problems are caused by the "transient" behaviour of the power system after fault inception. The conventional relays, e.g. distance relays, assume that the electromagnetic transients in a power system are negligible and/or disappear very fast. But in long UHV transmission lines and EHV cables, whose charging currents are comparably high, this assumption is not true. Hence the protection system must be designed to take account of such electromagnetic transients.

Moreover, fast fault tripping has a significant effect on the stability and availability of these modern systems. It is known that the rotational transient kinetic energy introduced into a power system by a fault is proportional to the square of the fault clearing time. Therefore high-speed clearing of faults when close to large sources of generation will reduce the system acceleration (increased chance of maintaining stability) more than any other form of dynamic control, which is effective only after the system is already being accelerated [1-3]. This factor besides some other requirements [3,4] led to a

considerable amount of work on reducing breaker operating times to the order of one cycle of the power frequency.

The foregoing considerations are the reason behind a recent interest in travelling wave-based protection schemes [1,2,5-19]. Despite being all based on travelling-wave theory, each scheme has its own unique approach for fault detection and direction discrimination.

In the relay by Dommel and Michels [6,7], a (directional) discriminant function D was proposed. This D is independent of the fault initiation angle as well as (initially) line termination. The discriminant is a function of the fault initiated travelling wave characteristic and its derivative with respect to time. The changes in current and voltage signals composing this wave characteristic are measured as differences from steady-state reference values. For a three phase system three different modal components (D's) are considered. More details about these D's are presented in Chapters 2 and 3.

In the "RALDA" relay [1,2,5], fault detection and direction discrimination are based on the initial changes in the pre-fault signals (voltages and currents). A comparison between the polarities of the initial voltage deviation and the initial current deviation determines the direction of the fault. The polarity comparison is performed at opposite ends of the protected line. These polarities are different (opposite signs) at both ends for an internal fault, while for an external fault they are different only at one end.

Vitins in [16] proposed a relaying principle close to that of "RALDA". The decision in the Vitins relay is based on the fault trajectory of the scaled change in current against the change in voltage. When the trajectory traverses a pre-determined boundary, a fault is detected. An initial intersection in the first or third quadrant means a reverse fault, while an initial intersection in the second or fourth quadrant indicates a forward fault.

The technique presented by Johns in [8] uses the sequence in which the derived fault-initiated forward and backward wave characteristics exceed a given threshold to detect the fault and determine its direction. Again this technique is based on the changes in the voltage and current signals from steady state. Also, three modal components are considered for nullifying the effect of the mutual coupling between the three phases.

The Japanese, through a series of investigating studies [11-15], have developed a current differential carrier relay based on travelling wave theory. The relay is based on using the measured voltage and current signals at each end of the protected zone to combine their respective forward and backward wave characteristics into an error function. For no internal fault this function is less than a threshold, while for an internal fault it exceeds this same threshold which should then lead to initiating a tripping signal.

Crossley and Mclaren [9,10] present a new technique for rapid measurement of the distance to the fault by using the fault initiated travelling waves. The direction to the fault is determined firstly by

the sequence in which the Johns [8] forward and backward directional relaying signals exceed a pre-determined threshold. For a detected forward fault, the fault location is determined by the time difference between the first wave approaching the fault from the relaying point and the corresponding wave reflected from the fault as it passes the relaying point. This is done through a correlation function which gives maximum output when the delay on the section of the incident signal corresponds to twice the distance to the fault.

More details and comparison aspects between these schemes are shown in Table(1.1).

In all these travelling wave relaying schemes, the effects of load current and high frequency transients on the currents and the voltages accompanied with the fault, are reduced to a minimum. In some of them, the UHS feature (i.e. relay decision time of a quarter cycle or less) is achieved. However each of the developed or suggested travelling wave schemes up till now has its own potential limits or problems. For example you cannot find all the following requirements realized together in one of these schemes:

1. Minimum communication requirements between the protected ends.
2. Independency of fault initiation angle.
3. Faulted phase selection and fault classification capability.
4. Insensitivity to parameter variation and different system configurations.

These potential limits of the available or suggested schemes represent the motivation of this present study. The relaying system described here is intended to have all the mentioned capabilities within one scheme. The essence of this relaying system is :

> " a multi-microprocessor directional comparison relaying scheme based on travelling wave theory, by which internal faults are detected and classified within a quarter of a power frequency cycle."

Multi-terminal line problems could also be solved by this new scheme. This new UHS directional detector is intended for use with a transfer trip (or block) carrier communication channel, i.e. with minimum communication requirements. A detection of a fault and its direction is made by a little more elaborate and highly reliable relaying algorithm which makes use of the modal components of the voltages and currents which are caused to be superimposed upon the steady-state prefault power frequency components following the fault inception.

The underlying theory of the proposed scheme is developed with reference to an idealized single-phase transmission line (Chapter 2). Its applicability to 3-terminal lines is discussed. Then the theory is extended to 3-phase idealized lines with the added feature of faulted phase selection and fault classification (Chapter 3). A verification study of the principle with more practical lines is presented through a digital computer numerical simulation by making use of the EMTP program in conjunction with a special program written to simulate the proposed principle. Then the characteristic features of the proposed scheme are discussed (Chapter 4).

Based on the fact that multiprocessor systems extend the range and capabilities of a single microprocessor to more complex areas which were previously in the domain of large computers, as well as the enhancements in the system reliability and the ease of the system design [29-39], it has been decided to use a master-slave multi-microprocessor architecture for realizing the developed algorithm (Chapter 5). A laboratory prototype based on the 8-bit Motorola type 6802 microprocessor was built within the course of this study (Chapter 6).

A real time computerized testing system, which displays the outputs of the EMTP program, was designed for testing the prototype and any other HS/UHS relay. The relay showed good practical behaviour when subjected to different testing cases (Chapter 7).

Finally, the general evaluation of the developed relaying principle and its realization is presented in the form of conclusions and recommendations (Chapter 8).

Some aspects of this relay are shown (in comparison with other schemes) in the last row of Table(1.1).

In summary, the theory of the newly developed protection scheme is based on a well-established understanding of classical electrical networks (i.e. travelling wave theory), and its realization is based on the most recent trends in microprocessor applications (i.e. multiprocessor architectures).

Table (1.1)

Comparisons between different travelling-wave-based relaying schemes

| RELAY PROJECT | STATUS | HARDWARE | COMMUNICATION REQUIREMENT | FAULT INITIATION. ANGLE DEPENDANCE. | PHASE SELECTION | FAULT CLASSIFICATION | SPEED |
|---|---|---|---|---|---|---|---|
| Dommel & Michals [6,7] | theory and computer simulation | ------- | minimum (indication of fault direction) | no | no | no | ? |
| Johns [8] | theory and tested experimental prototype | analogue | minimum (indication of fault direction) | yes | no | no | UHS |
| Crossley & Mclaren [9,10] | theory and tested prototype | analogue | none | yes | no | no | UHS |
| RALDA [1-2] | installed in field | analogue | minimum (indication of fault direction) | yes | yes | no | UHS |
| Vitins [16] | theory and laboratory simulation | -------- | minimum (indication of fault direction) | yes | yes | no | UHS |
| JAPANESE [11-15] | intalled in field | digital | maximum (full information from the two ends to the central processor) | yes | yes | no | HS |
| THIS RELAY | theory and tested laboratory prototype | multi-microprocessor (digital) | minimum (indication of fault direction) | no[1] | yes | yes | UHS |

[1] The theory and the algorithm show independence on fault initiation angle, while the implemented prototype is dependent due to the simple differentiation technique used with this prototype.

## Chapter II

## FAULT DETECTION PRINCIPLE AND RELAYING DISCRIMINANT

### 2.1 INTRODUCTION

In this chapter the basic theory of the fault detection principles used with the proposed scheme is presented with reference to lossless single-phase transmission lines. The discrimination between forward and backward faults is achieved with the developed highly convergent relaying discriminants. The extension of the same principle to the difficult problem of "three-terminal lines" is developed.

### 2.2 BASIC PRINCIPLES AND WAVE CHARACTERISTICS

Considering a single-phase transmission line (R-S) with distributed parameters, a relationship between the voltage and the current can be established at a point "x" on the line at a time "t" by the so-called "telegrapher's equations" of the line [24].

$$-\partial v(x,t)/\partial x = r\, i(x,t) + \ell\, \partial i(x,t)/\partial t \qquad (2.1)$$

$$-\partial i(x,t)/\partial x = g\, v(x,t) + c\, \partial v(x,t)/\partial t \qquad (2.2)$$

where $r, \ell, g$ and $c$ are the series resistance, series inductance, shunt conductance and shunt capacitance per unit length of the line.

Assuming a lossless line the so called "wave equation" can be derived from equations 2.1 and 2.2.

$$\partial^2 v(x,t)/\partial t^2 = (1/\ell\, c)\ \partial^2 v(x,t)/\partial x^2 \qquad (2.3)$$

$$\partial^2 i(x,t)/\partial t^2 = (1/\ell\, c)\ \partial^2 i(x,t)/\partial x^2 \qquad (2.4)$$

A general solution of the wave equations was first given by d'Alembert. This solution for equations (2.3) and (2.4) can be expressed by the following two equations [6,21].

$$i(x,t) = F_1(x-at) + F_2(x+at) \qquad (2.5)$$

$$v(x,t) = Z\ F_1(x-at) - Z\ F_2(x+at) \qquad (2.6)$$

where $Z = \sqrt{\ell/c}$ is the surge impedance, 'a' is the propagation velocity, $F_1$ is a forward current travelling wave and $F_2$ is a backward current travelling wave.

## 2.3 STEADY STATE AND SUPERIMPOSED QUANTITIES

The inception of a fault in a transmission line will cause the postfault voltage $v_R$ and current $i_R$ at the relaying point to deviate from the steady state prefault voltage $v_R'$ and current $i_R'$ respectively. Hence we can write

$$v_R(t) = v_R'(t) + \Delta v_R(t) \qquad (2.7)$$

$$i_R(t) = i_R'(t) + \Delta i_R(t) \qquad (2.8)$$

where $\Delta v_R(t)$ and $\Delta i_R(t)$ denote the fault generated voltage and current deviation from prefault steady state values as functions of time. The approach described here, like others [1,6,8,9,16], utilizes these superimposed quantities of voltage and current at the relaying point for making its decisions.

In Fig.(2.1) with a fault at F the fault currents and voltages are described by the superposition principle. Hence the occurrence of a fault is equivalent to suddenly switching on a fictitious voltage source at the fault point with a voltage which is equal and opposite to the prefault voltage at the fault point. The deviation signals $\Delta v_R$ and $\Delta i_R$ can be considered as those voltages and currents which would arise if this fictitious source were applied to the system with all voltage sources set to zero. This same principle has been used in developing other protection schemes [1,6,8,16].

Now considering the previously mentioned forward and backward travelling waves associated with the superimposed quantities $\Delta v(x,t)$ and $\Delta i(x,t)$ due to the fault we can write

$$\Delta i(x,t) = f_1(x-at) + f_2(x+at) \qquad (2.9)$$

$$\Delta v(x,t) = Z\, f_1(x-at) - Z\, f_2(x+at) \qquad (2.10)$$

where $f_1$ and $f_2$ are the forward and backward travelling wave deviations resulting from fault inception as shown in Fig.(2.1.b).

## 2.4 TERMINATION INDEPENDENT WAVE CHARACTERISTIC [6,8,21]

From equations (2.9) and (2.10) we can write

$$\Delta v(x,t) + Z\Delta i(x,t) = 2\, Z\, f_1(x-at) \qquad (2.11)$$

$$\Delta v(x,t) - Z\Delta i(x,t) = -2\, Z\, f_2(x+at) \qquad (2.12)$$

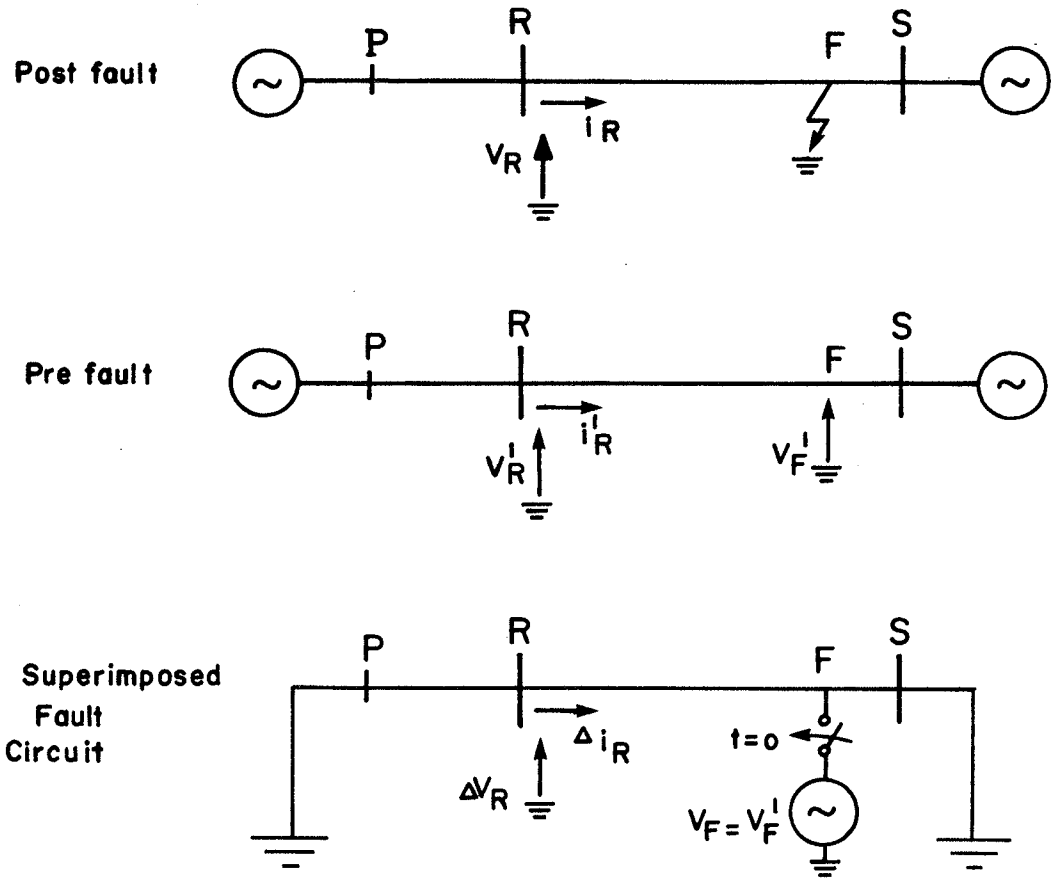



Fig. (2.1) a) Principle of superposition and
b) Travelling wave propagation
for forward fault

It should be noted that the left hand sides of the above two equations (2.11) and (2.12) become constant when (x-at) and (x+at) are constant, respectively.

With the aid of Fig.(2.1.b) and equation (2.11) a wave characteristic at substation "R" can be derived.

Assume that the voltage and the line current changes produced by the fault at the fault point "F" are $v_F$ and $i_{FR}$ (with $i_{FR}$ taken as positive from the fault location towards substation "R" ), and assuming a travel time "$\tau$" between "F" and the point of reflection "P", "$\tau_1$" between "F" and "R" and "$\tau_2$" for "F-R-P-R" as shown in Fig.(2.1.b), we can write

$$v_F(t) + Z\, i_{FR}(t) = \Delta v_R(t+\tau_1) - Z\, \Delta i_R(t+\tau_1) \quad (2.13)$$

where $\Delta i_R$ has a negative sign if it is referenced positive from substation "R" towards "F".

Assume the prefault voltage at "F" $v_F'$ is

$$v_F' = V_{rms}\sqrt{2}\sin(\omega t+\phi) \quad (2.14)$$

where $\omega$ is the power frequency in radians per second and $\phi$ is the fault inception angle.

Then the voltage deviation produced by the fault at the fault point is

$$v_F = -v_F' = -V_{rms}\sqrt{2}\sin(\omega t+\phi) \quad (2.15)$$

Since the backward travelling wave $f_2$ at the fault point is initially zero as shown in Fig.(2.1.b), equation (2.12) yields

$$i_{FR}(t) = v_F(t)/Z \quad (2.16)$$

Combining equations 2.15 and 2.16 we get

$$v_F(t) + Z\, i_{FR}(t) = -\, 2\, V_{rms} \sqrt{2}\, \sin(\omega t + \phi) \qquad (2.17)$$

Combining equations 2.13 and 2.17 the wave characteristic seen at substation "R" is

$$\Delta v_R(t+\tau_1) - Z\, \Delta i_R(t+\tau_1) = -2\, V_{rms} \sqrt{2}\, \sin(\omega t + \phi) \qquad (2.18)$$

$$\text{for } 0 < t < 2\tau$$

This composite-termination-independent expression is observable at "R" from " $\tau_1$" to "$2\tau + \tau_1$", (1st. incidence + 1st. reflection + 2nd. incidence). After that time reflections from the fault location will change it.

It should be noted here that $f_2$ could be detected (as a backward wave) at "R" within the time span " $\tau_2$" to "$2\tau + \tau_2$" from fault inception i.e. soon after or with detecting $f_1$ for a close-in fault. Its value is

$$f_2 = r_c\, f_1 \qquad (2.19)$$

$$\text{for} \quad t > \tau_2$$

where $r_c$ is a reflection coefficient with value depending on the termination characteristic.

## 2.5 HIGHLY RELIABLE DISCRIMINANT FUNCTION [6,7]

The forward wave characteristic in equation 2.18 is initially independent of termination but it does depend on the fault inception angle ($\phi$). For ($\phi$)= 0.0 the characteristic magnitude becomes a ramp function: $2.V_{rms}\sqrt{2}\,\omega t$ which would be difficult to detect within the observable time span $2\tau$ if $\tau \ll T$ ,where T is the period of the power frequency. This problem is avoided by using the wave characteristic in combination with its derivative to define a "forward fault travelling wave discriminant", $D_F$:

$$D_F = (\Delta v_R - Z\,\Delta i_R)^2 + 1/\omega^2\{d/dt(\Delta v_R - Z\,\Delta i_R)\}^2 \qquad (2.20)$$

$$= 0 \quad \text{for } t < \tau_1, \text{ and}$$

$$= 8\,V_{rms}^2 \quad \text{for } \tau_1 < t < 2\tau + \tau_1 \text{ (by substitution from eq. 2.18)}$$

This $D_F$ is independent of the angle of fault inception and is observable at R from $\tau_1$ to $\tau_1+2\tau$ . The magnitude of $D_F$ is zero (except for noise) on a healthy line and is extremely high ($8\,V^2_{rms}$, initially) on a faulted line.

## 2.6 FAULT DIRECTION DISCRIMINATION

It has been shown in the previous section in conjunction with Fig.(2.1.b) that the discriminant $D_F$ derived from the forward travelling wave characteristic (equation 2.11) is highly decisive for detecting internal faults within the protected direction. But a problem will arise with that discriminant when there is a backward fault with respect to the relay location. In this case, as shown in Fig.(2.2), the relay

based only on the forward discriminant $D_F$ [6] could indicate a fault at a time $\tau_2$ and it would be considered as a forward fault.

The solution of the foregoing problem could be achieved through a discriminant based on the backward wave characteristic (equation 2.12). Following the same procedures used in deriving the forward wave discriminant we can establish a backward discriminant $D_B$ in the following form:

$$D_B = (\Delta v_R + Z \Delta i_R)^2 + 1/\omega^2\{d/dt(\Delta v_R + Z \Delta i_R)\}^2 \qquad (2.21)$$

For a reverse fault, $D_B = 8 V^2_{rms}$ for $\tau_1 < t < 2\tau + \tau_1$ as shown in Fig.(2.2)

In the reverse fault case, $D_F$ will converge (after $D_B$ converges) at $t = \tau_2$ which is greater than $\tau_1$ by twice the travelling time from the relaying point to the point of reflection at or after the far end (S). The value of the forward wave in this case would be reduced by the reflection coefficient at the point of reflection.

To summarize, we can base the direction discrimination on calculating both $D_F$ and $D_B$ simultaneously. If $D_B$ converges ( exceeds a certain threshold ) before $D_F$ it means that it is a backward fault, otherwise it is a forward fault. The discrimination is seen to be quite reliable with this procedure.

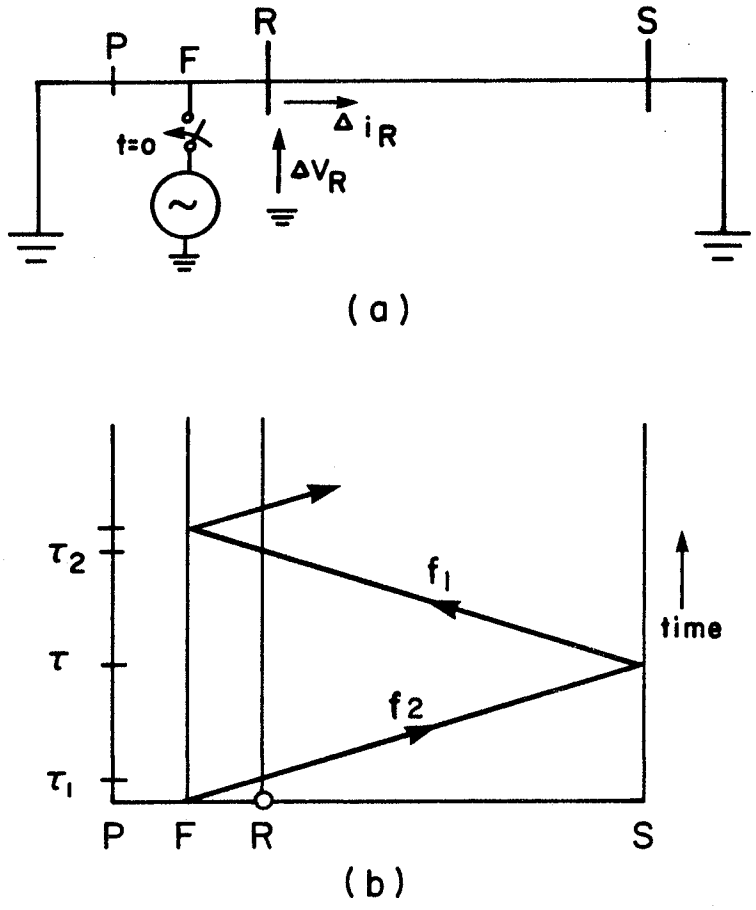



Fig. (2.2) a) Superimposed fault circuit, and
b) Travelling wave propagation
for backward fault

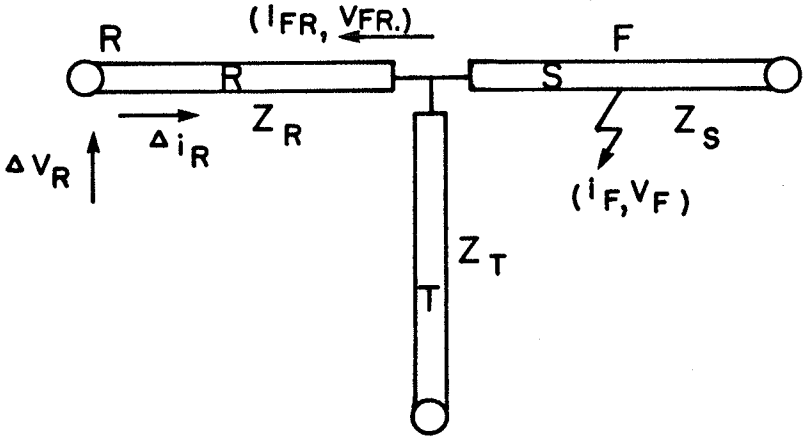



Fig. (2.3) Single phase 3-terminal line

## 2.7 THREE-TERMINAL-LINE DISCRIMINANT FUNCTION

For economical considerations (mainly), the use of three-terminal lines has been and will, in the future, be of even greater interest to the owners of high-voltage transmission networks [20]. However, the protection of multi-terminal lines is never as simple as that of two-terminal lines [20].

Unconventional, essentially travelling wave schemes have been presented for overcoming these difficulties [11,18,19]. The usual multi-terminal line protection problems associated with fault current infeeds and outfeeds, which arise from 60 Hz fault components, are not present for relaying schemes based on the travelling-wave approach.

In this section the highly convergent and highly reliable discriminant approach described above will be extended to multi-terminal lines by considering a 3-terminal single phase line as shown in Fig.(2.3).

Consider $Z_R$, $Z_S$ and $Z_T$ as the surge impedances of the three sections R,S, and T, respectively with the fault point as shown. The effective parallel surge impedance of line R and T is

$$Z_p = Z_R Z_T /(Z_R + Z_T) \tag{2.22}$$

with a refraction (transmission) coefficient [24]:

$$T_r = 2Z_p/(Z_p+Z_S). \tag{2.23}$$

We can write

$$v_{FR} = T_r v_F \tag{2.24}$$

and

$$i_{FR}=T_r(Z_S\ i_F)/Z_R. \qquad (2.25)$$

Then our wave characteristic at substation "R" is

$$\Delta v_R - Z_R\ \Delta i_R = v_{FR} + Z_R\ i_{FR} = T_r(v_F + Z_S\ i_F) \qquad (2.26)$$

Hence the forward discriminant $D_F$ for the 3-terminal line is (initially) related to a corresponding 2-terminal line R-S by the following relationship:

$$D_F(3\text{-ter}) = T_r^{\,2}\ D_F(2\text{-ter}) \qquad (2.27)$$

where the reference two terminal line has the same surge impedance as that of the faulted section of the 3-terminal line.

If all lines have the same surge impedance, then

$$T_r = (2/3).$$

Hence

$$D_F(3\text{-ter}) = (4/9)\ D_F(2\text{-ter}) \qquad (2.28)$$

i.e. the 3-terminal line value is about half the corresponding 2-terminal line value.

It should be noted here that the time span for this initial forward discriminant value is :

$\tau_{S1} + \tau_R < t < \tau_{S1} + \tau_R + 2\tau_T$ for $\tau_T < \tau_R < \tau_{S1}$

$\tau_{S1} + \tau_R < t < 2\tau_{S1} + \tau_R$ for $\tau_{S1} < \tau_T < \tau_R$,

or

$\tau_{S1} + \tau_R < t < 3\tau_R + \tau_{S1}$ for $\tau_R < \tau_T < \tau_{S1}$

depending on which section (R, T or S) has a shorter travelling time (where $\tau_R$, $\tau_T$ and $\tau_{S1}$ are the travelling times over section R, section T, and from the fault point F on section S to the point of connection, respectively).

Similar analysis could be applied with the backward faults and/or the backward discriminants.

It should be noted that regardless of the different reflections, the discriminant will go high right after the travelling time from the fault point to the relaying point. The timing restriction in this case is the fast direction discrimination (before any detected reflection) at the corresponding terminal for the backward fault condition. This should then be used to block the other two terminal relays.

# Chapter III

# PHASE SELECTION AND FAULT CLASSIFICATION FOR 3-PHASE LINES

## 3.1 INTRODUCTION

The basic relaying principle described in the previous chapter is extended in this chapter to include three phase lines. A modal transformation technique, which decomposes the three phase line into three single phase lines, is used for this purpose.

Algorithms based on three different modal transformations are developed for phase selection and fault classification. Each algorithm is derived from a corresponding truth table. The truth tables are constructed for different types of faults with different faulted phases and different transformation bases. These truth tables could be quite helpful in explaining the behaviour of any travelling wave relaying technique using modal transformation analysis.

## 3.2 THREE-PHASE LINE RELAYING DISCRIMINANTS

According to the theory of natural modes [23], a three phase coupled line can be decomposed into three independent single phase lines (modes). On each of these lines (modes) the discussion given in the previous chapter for single phase lines is applicable. The discriminants for fault detection in a three phase line are defined by utilizing the superimposed modal voltages and currents at the relaying point as follows ,

$$D_F^{(k)} = (\Delta v_R^{(k)} - Z^{(k)}\ \Delta i_R^{(k)})^2 + 1/\omega^2 \{\frac{d}{dt}(\Delta v_R^{(k)} - Z^{(k)}\ \Delta i_R^{(k)})\}^2 \quad (3.1)$$

for the mode (k) forward discriminant; and

$$D_B^{(k)} = (\Delta v_R^{(k)} + Z^{(k)}\ \Delta i_R^{(k)})^2 + 1/\omega^2 \{\frac{d}{dt}(\Delta v_R^{(k)} + Z^{(k)} \Delta i_R^{(k)})\}^2 \quad (3.2)$$

for the mode (k) backward discriminant, where $Z^{(k)}$ is the mode (k) surge impedance, and $\Delta v_R^{(k)}$ and $\Delta i_R^{(k)}$ are the mode-k superimposing voltage and current respectively at relay point "R". These modal voltages and currents can be transformed from the corresponding phase quantities by the following equations,

$$[v(t)] = [S]\ [v^{(mode)}(t)] \quad (3.3)$$

$$[i(t)] = [Q]\ [i^{(mode)}(t)] \quad (3.4)$$

where [S] and [Q] are the modal transformation matrices. For an ideally transposed single circuit line , [Q] will be equal to [S] and both will be constant, but except for the zero sequence mode, they will not be uniquely defined.

Discrete transposition of transmission lines is relatively rare. However, conventional practice involves setting the protective relays assuming that the line is ideally transposed [8]. Therefore in the present study, like some others (e.g. [6], [8], [11]), the developed algorithm will be based on the assumption of perfectly transposed transmission lines. The extension to nontransposed lines is

investigated through digital numerical simulation and through the real time testing of an implemented prototype.

Three of these constant modal transformation matrices for perfectly transposed lines are considered within the course of this study, namely

1)Clark transformation [6,11]:

$$[Q] = [S] = \begin{bmatrix} 1 & 1 & 0 \\ 1 & -1/2 & \sqrt{3}/2 \\ 1 & -1/2 & -\sqrt{3}/2 \end{bmatrix} \qquad (3.5)$$

2)Wedepohl(*) transformation [8,23]:

$$[Q] = [S] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix} \qquad (3.6)$$

3) Karrenbauer transformation [6,11]:

$$[Q] = [S] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & -2 & -1 \\ 1 & 1 & -2 \end{bmatrix} \qquad (3.7)$$

---

* It first appeared in [23] by L.M.Wedepohl.

## 3.3 FAULTED PHASE SELECTION AND FAULT CLASSIFICATION

Faulted phase selection, and hence selective pole tripping, is an important relaying capability because it increases the system stability as well as its availability. Fault classification is a relaying feature which also enhances the protection scheme. In this section a phase selection and fault classification relaying principle based on the foregoing discussion is developed through modal transformation theory.

Consider, for example, the Karrenbauer transformation (eq.(3.7)), from which Table (3.1) is constructed. This table shows the forward modal discriminant functions for different fault types and different faulted phase(s) combinations. The transformation to the modal domain in this table is based on phase "a". The table contents are normalized with respect to $V^2_{rms}$, i.e. the square of the operating voltage . Details of the derivation of this table are given in Appendix A . Similar tables could be derived for the other types of transformation ,e.g. Clark and Wedepohl as shown in Appendix A , tables A.1 and A.2 .

By investigating any of these tables it should be noted that some discriminant components vary with respect to the faulted phase(s).

TABLE 3.1

Discriminant components in the Karrenbauer domain

| Discriminant Components | Line - to - Ground | | | Line - to - Line | | | Line - to - Line - to - Ground | | | 3 Phase Short Circuit |
|---|---|---|---|---|---|---|---|---|---|---|
| | a − G | b − G | c − G | a - b | b − c | c - d | a − b − G | b − c − G | c − a − G | |
| $D^{(0)}$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | 0 | 0 | 0 | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | 0 |
| $D^{(1)}$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 0 | 8/9 | 2/9 | 2/9 | 8/9 | $\frac{8}{9}\frac{Z_0^2+Z_1^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | $\frac{8}{9}\frac{Z_1^2+Z_0^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | 8/9 |
| $D^{(2)}$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 0 | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 2/9 | 2/9 | 8/9 | $\frac{8}{9}\frac{Z_0^2+Z_1^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | $\frac{8}{9}\frac{Z_0^2+Z_1^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | 8/9 | 8/9 |

— $D^{(0)}$, $D^{(1)}$ and $D^{(2)}$ are the relaying discriminant components in Karrenbauer domain.

— $Z_0$ and $Z_1$ are the zero and positive sequence surge impedences respectively.

— All the quantities are normalized with respect to $V^2_{RMS}$: line-line prefault voltage.

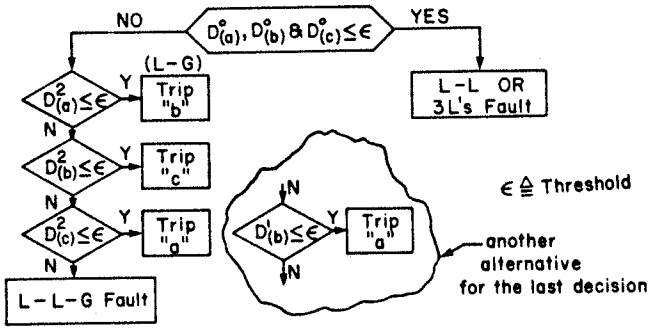
Thus, by calculating the discriminant components for the same faults with the transformation base phase changed from "a" to "b" and then to "c", we can build the truth tables in figures (3.1.a), (3.2.a) and (3.3.a) for Karrenbauer, Clark and Wedepohl respectively. In each of these tables the "0" stands for the zero value of "$D_F$" and the "1" stands for the nonzero very high value of "$D_F$". Out of these tables decision flow charts for phase selection and fault classification are shown in figures (3.1.b), (3.2.b) and (3.3.b) for each of the corresponding transformations.

It is seen that each transformation enables, through the truth tables and consequently through the decision flow charts, the selection of the faulted phase in the line-to-ground (L-G) case, which is the most probable type of fault in a transmission network. For fault classification of other types of faults , the Karrenbauer transformation is less efficient than the other two, (Clark and Wedepohl), which achieve complete fault classification and even faulted phases selection for line-line (L-L) faults.

It is important to emphasize that there is an extremely high change from the "0" situation to the "1" situation in the truth tables. This indicates the highly decisive nature of this relaying scheme as compared to many others [1,8,16].

| Fault → | | L-G | | | L-L | | | L-L-G | | | 3LS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Basis | D's | a | b | c | a-b | b-c | c-a | a-b | b-c | c-a | |
| Ph "a" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "b" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "c" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

a) Truth table

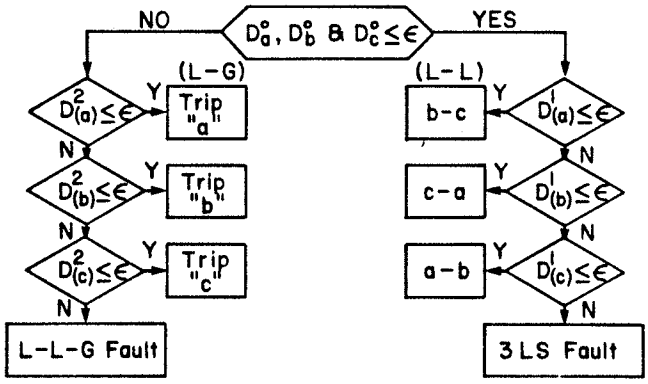



b) Flow chart

Fig. (3.1) Phase selection and fault classification based on the Karrenbauer transform.

| Fault → | | L−G | | | L−L | | | L−L−G | | | 3LS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Basis | D's | a | b | c | a-b | b-c | c-a | a-b | b-c | c-a | |
| Ph "a" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "b" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "c" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

a) Truth table

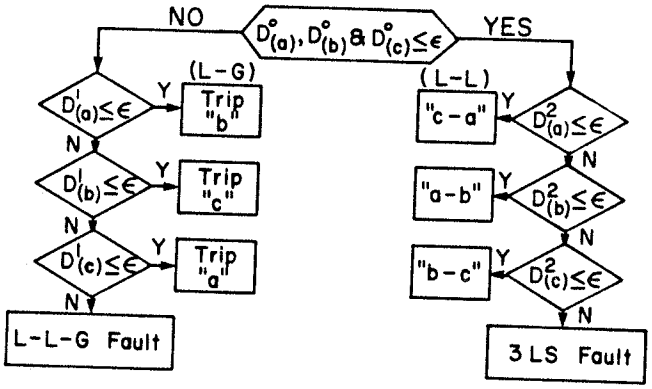



b) Flow chart

Fig. (3.2) Phase selection and fault classification based on the Clark transform.

| Fault → | | L-G | | | L-L | | | L-L-G | | | 3LS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Basis | D's | a | b | c | a-b | b-c | c-a | a-b | b-c | c-a | |
| Ph "a" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| Ph "b" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "c" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |

a) Truth table




b) Flow chart

Fig. (3.3) Phase selection and fault classification based on the Wedepohl transform.

It should be noted also that exactly the same truth tables could be constructed for schemes based only on the wave characteristic $\Delta v_R^{(k)} - Z^{(k)} \Delta i_R^{(k)}$ [8,9], but the non-zero values (the 1's) vary, depending on the fault inception angle. Truth tables with zero and non-zero values for different conditions would help in explaining the behavior of these other schemes.

# Chapter IV

# COMPUTER SIMULATION AND THE RESULTING CHARACTERISTIC FEATURES

## 4.1 INTRODUCTION

The relaying principle developed in the previous chapter is based on the assumption of ideal simple lines, i.e. lossless, ideally transposed, constant (non-frequency dependent) parameters and single circuit lines. A verification of this relaying principle with more practical cases is presented in this chapter. This is done through computer numerical simulation by utilizing the available version of the electromagnetic transient program (EMTP) [27], which is considered as an advanced power system computer simulation program, in conjunction with a special program written to simulate the relaying principle. Two different power systems are considered for the purpose of evaluating the viability of the developed relaying technique with different protected system configurations involving different practical aspects. The chapter concludes by discussing the characteristic features of the proposed relaying scheme.

## 4.2 SIMULATION ENVIRONMENT: THE "EMTP" PROGRAM

The Electromagnetic Transients Program (EMTP) developed at the Bonneville Power Administration (BPA) and based on algorithm by Dommel [21] has been a powerful power systems transients simulation tool for a long time. This general computer program is capable of simulating a large variety of transient conditions for systems of any size and complexity.

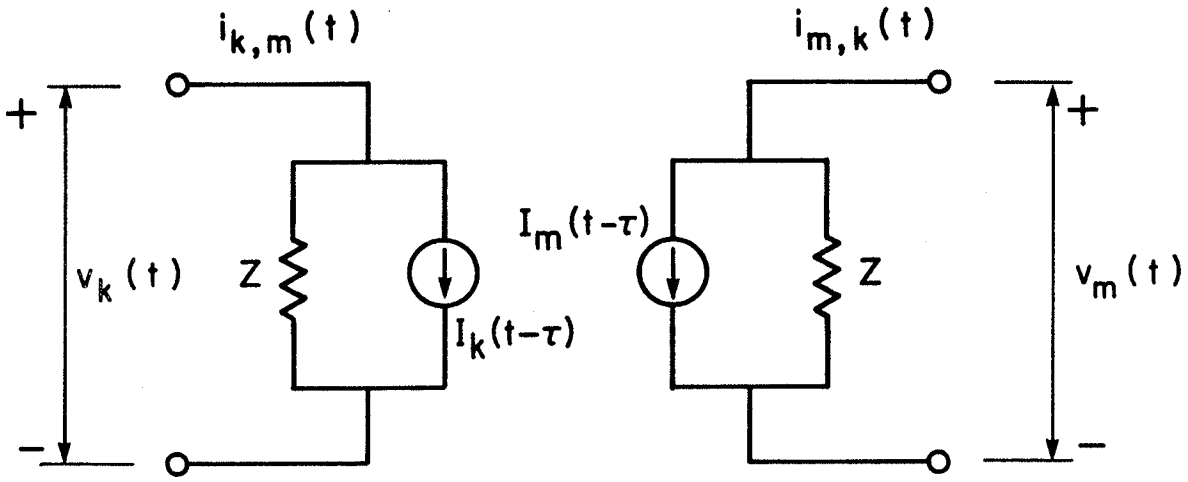
BPA's EMTP uses the trapezoidal rule for integration, which is known to be a fairly stable and accurate integration method. Furthermore, this integration procedure has a direct physical analogy, in the form of simple Norton-equivalent circuits at each time step, i.e. the differential equations for inductors, capacitors and distributed transmission lines yield a set of resistors and current sources [21,22]. For example, models of distributed transmission lines are treated as shown below for a basic representation with no frequency-dependence.

Consider first the lossless line of Fig.(4.1.a). As given in Chapter 2, this line could be represented by the set of equations (2.1) to (2.6). The full signal (not the change) equations equivalent to equations (2.11) to (2.13) can be used to get the equivalent impedance network shown in Fig.(4.1.b), where

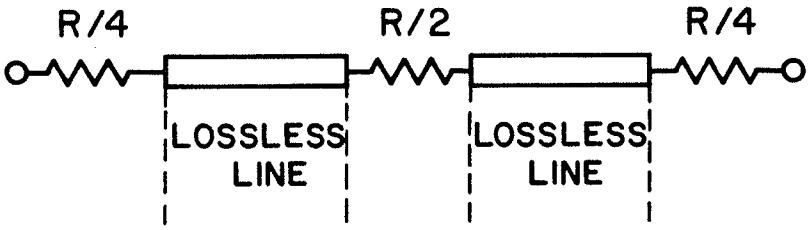
$$v_m(t-\tau) + Z\, i_{m,k}(t-\tau) = v_k(t) + Z(-i_{k,m}(t)) \qquad (4.1)$$

From the above equation the simple two-port relationship for $i_{k,m}$ can be written as


a) Lossless line




b) Equivalent impedance network




c) Modelling of a lossy transmission line
(R = total series resistance of the line)

Fig. (4.1) Dommel's representation of transmission lines
(no frequency dependence)

$$i_{k,m}(t) = (1/Z)v_k(t) + I_k(t-\tau)$$

and by analogy, (4.3)

$$i_{m,k}(t) = (1/Z)v_m(t) + I_m(t-\tau)$$

with equivalent current sources $I_k$ and $I_m$ which are known at state "t" from the past history at time "$t-\tau$",

$$I_k(t-\tau) = -(1/Z)v_m(t-\tau) - i_{m,k}(t-\tau)$$

$$I_m(t-\tau) = -(1/Z)v_k(t-\tau) - i_{k,m}(t-\tau) \qquad (4.4)$$

Fig.(4.1.b) shows the corresponding equivalent impedance network, which describes the lossless line at its terminals. Topologically the terminals are not connected; the conditions at the other end are only seen indirectly and with a time delay $\tau$ through the equivalent current sources I.

The distributed series resistance for this non-frequency dependent line parameter representation could be approximated by treating the line as lossless and adding lumped resistances at both ends or, as considered by the BPA's program [27], by lumping R/4 at both ends and R/2 at the middle of the line where R is the total series resistance (Fig.(4.1.c)). Under this representation considered by BPA, the equivalent impedance network of Fig.(4.1.b) is still valid and the only slight change to be considered is as follows for $I_k$ (as $I_m$ is analogous to $I_k$):

$$Z = \sqrt{\ell/c} + R/4 \qquad (4.5)$$

$$I_k(t-\tau) = ((1+h)/2)\{I_k \text{ from eq.(4.4)}\} + ((1-h)/2)\{I_m \text{ from eq.(4.4)}\} \quad (4.6)$$

where

$$h = (Z - R/4)/(Z + R/4)$$

For transients calculation with frequency dependent parameters, many approaches have been considered in different BPA EMTP versions (e.g. [25], [26]). The one used in this study is the one introduced by Semlyen and Dabuleanu in [26], which is available in the version resident in the mainframe computer of the University of Manitoba.

The Semlyen approach to the frequency dependent problem is based on the concept of recursive evaluation of the convolution integrals in his formulation. This formulation is in terms of the incident and reflected waves and involves "system propagation functions" and "the characteristic admittance function". These functions are approximated by exponential terms. This method also produced a simple Norton-type line equivalent.

Using the trapezoidal rule, as indicated above, the entire network reduces to a resistive network with current source excitation. Numerically this leads to the solution of a system of linear (nodal) equations at each time step.

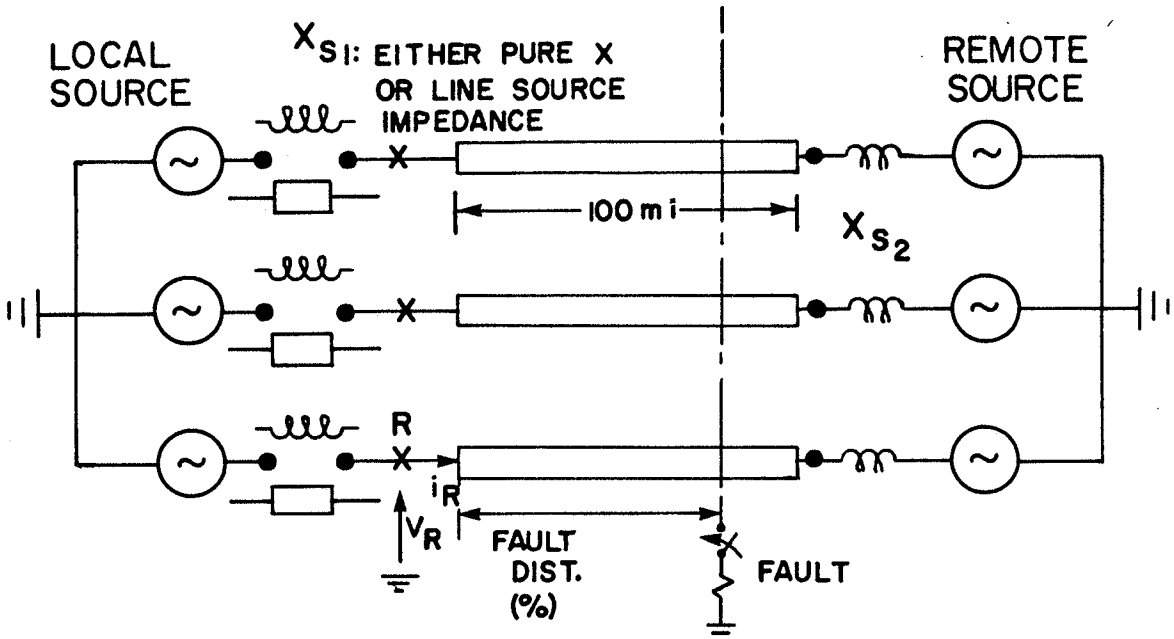
Saturable branches and other network nonlinearities can be modelled by including them in the form of additional dependent current sources in parallel with corresponding resistance elements.

## 4.3 CASE STUDIES

### 4.3.1 SINGLE CIRCUIT 500 KV SYSTEM

The system considered for this case is the one shown in Fig.(4.2) [28]. It is a single circuit ideally transposed 500 KV system. The parameters are non-frequency dependent. Different solid fault types are considered with different fault inception angles and at different locations on the line. For the sake of clarity samples of some simulated conditions based on the Karrenbauer transform are shown in Fig.(4.3) to Fig.(4.8). Each figure corresponds to a certain type of fault as indicated on the figures themselves. The faults are applied at the positive peak (90 degrees) of phase "a" for all the cases shown except for the first one (Fig.(4.3)) which corresponds to a L-G fault at zero-crossing of the faulted phase "a". The first five samples (Fig.(4.3) to Fig.(4.7)) are forward faults, and the last one of Fig.(4.8) is a backward L-G fault, near the relay location at R (-0%). The different types of forward faults are applied at F (80%), as shown in Fig.(4.2). In each figure, besides the phase voltages and currents, three sets of semi-log curves are shown. Each one corresponds to the behaviour of the discriminant components with a different phase as a transformation basis. The time span shown is one-half cycle before fault (steady state) to one-half cycle after fault inception.

Regardless of the fault inception angle, the large distinctive change in the calculated "D's" and their coincidence with the truth tables as shown in these figures is very clear, even though a "real line" is modelled.




Line parameters

phase mode: .....

z = 0.041 + j0.528 ohms/mile
y = 7.86 micro-siemens/mile
a = 185,100 miles/second
Z (surge) = 259 ohms
$\tau$ = 5.40 x (distance between reflection points) microseconds

ground mode:.....

z = 0.449 + j2.020 ohms/mile
y = 4.25 micro-siemens/mile
a = 124,800 miles/second
Z (surge) = 689 ohms
$\tau$ = 8.01 x (distance between reflection points) microseconds

Fig. (4.2) Single circuit 500 KV study system

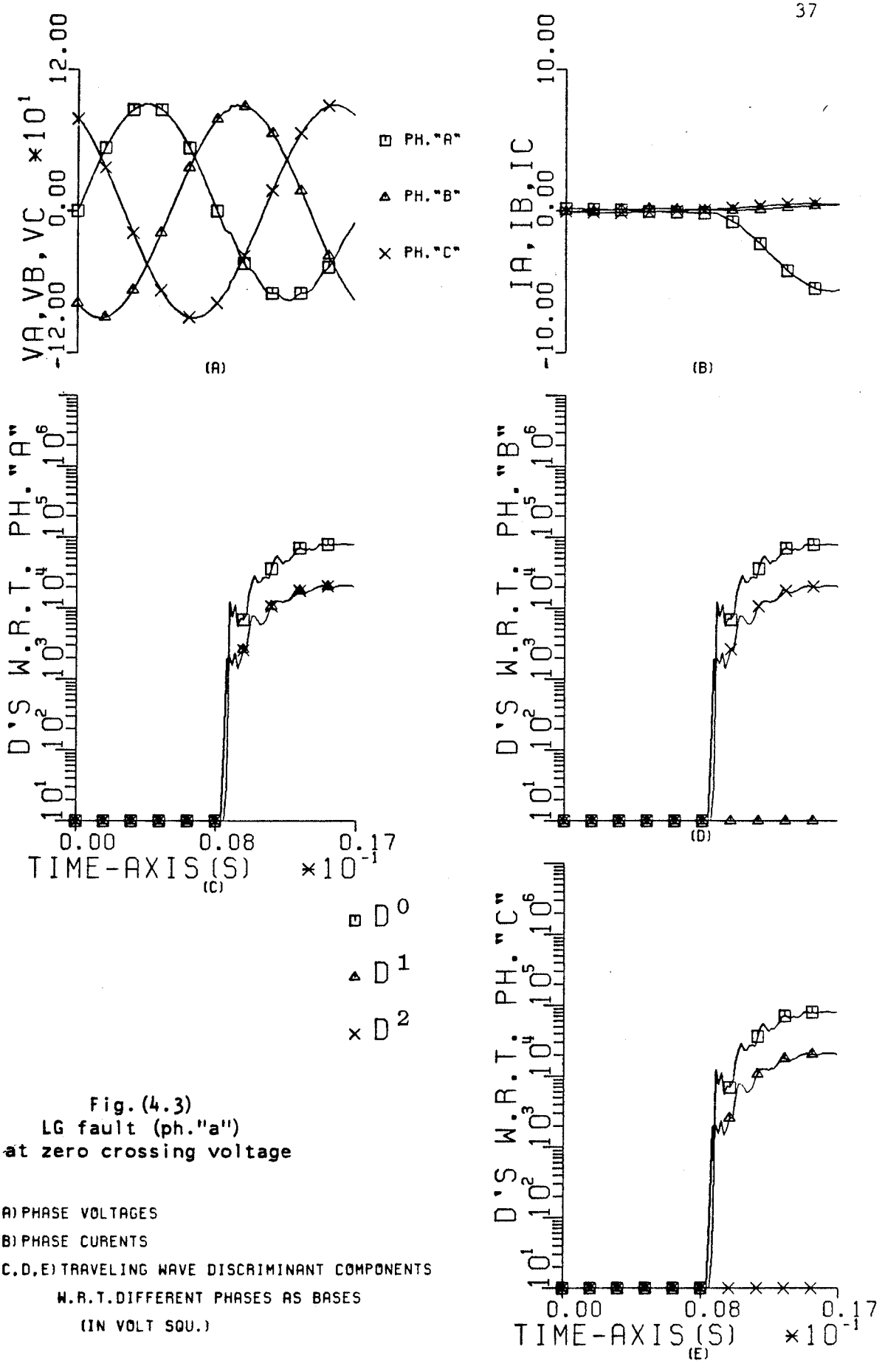



Fig. (4.3)
LG fault (ph."a")
at zero crossing voltage

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

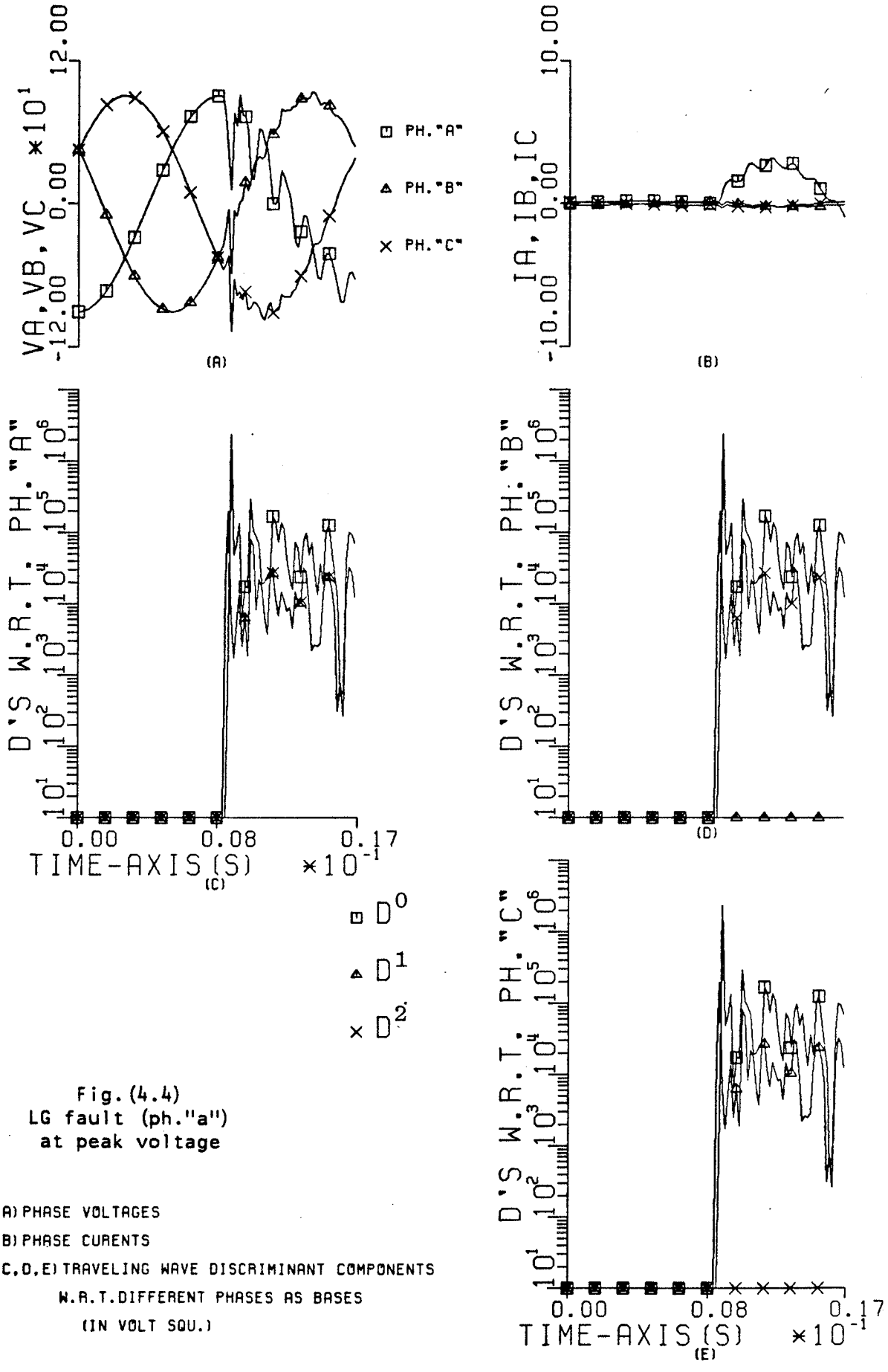



Fig. (4.4)
LG fault (ph."a")
at peak voltage

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

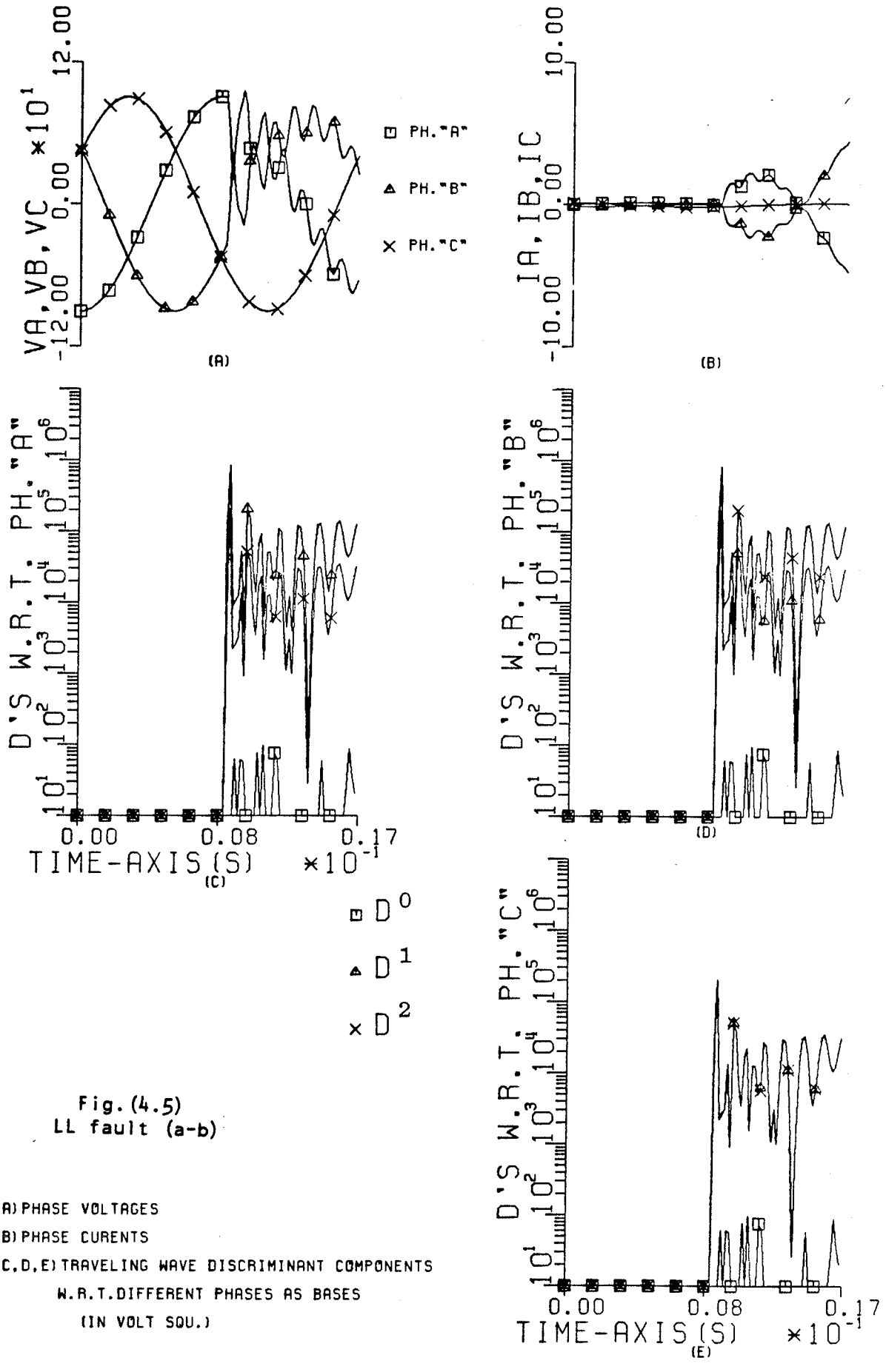



Fig. (4.5)
LL fault (a-b)

A) PHASE VOLTAGES
B) PHASE CURENTS
C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

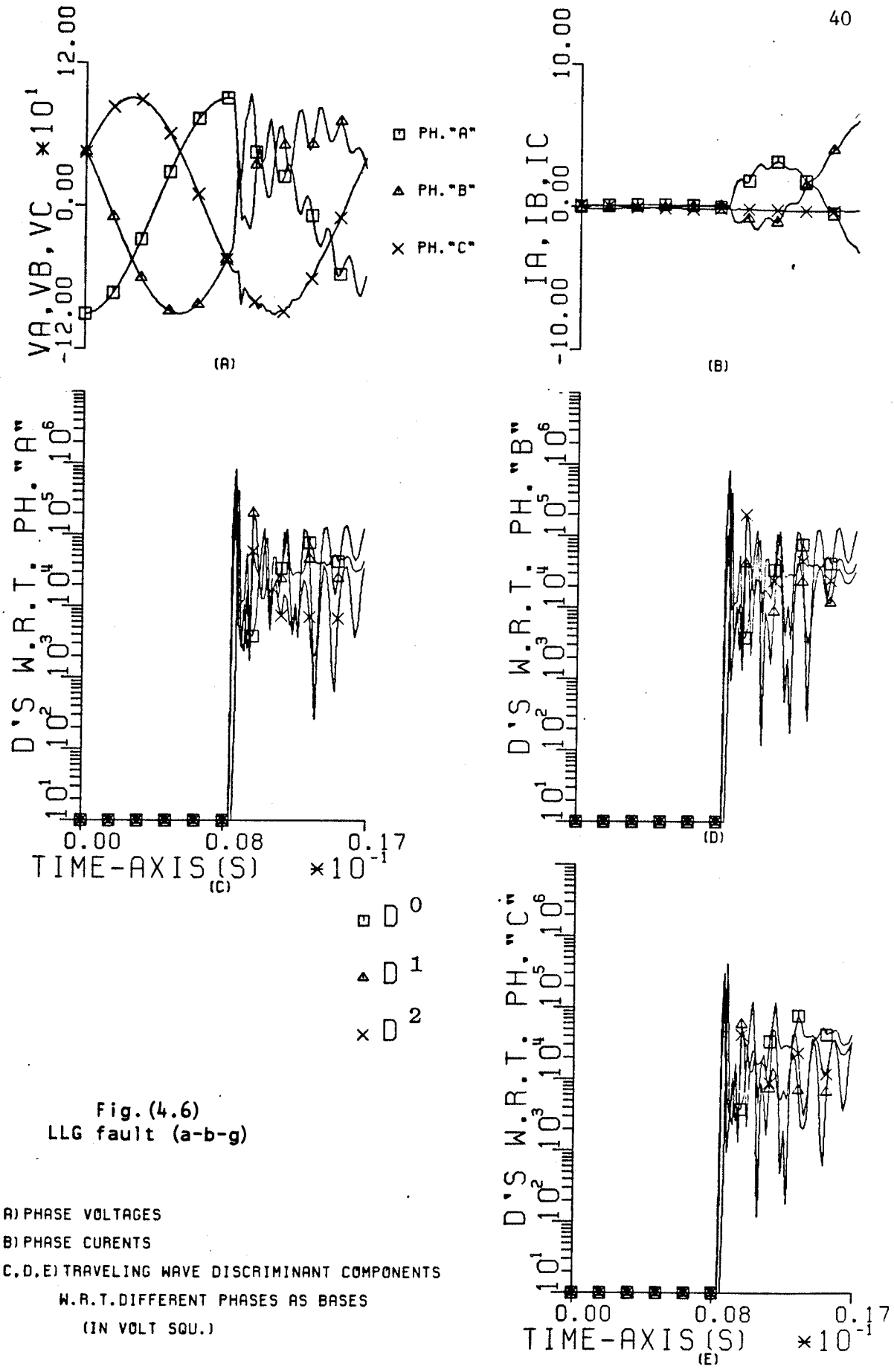



**Fig. (4.6)**
**LLG fault (a-b-g)**

A) PHASE VOLTAGES

B) PHASE CURENTS

C, D, E) TRAVELING WAVE DISCRIMINANT COMPONENTS W.R.T. DIFFERENT PHASES AS BASES (IN VOLT SQU.)

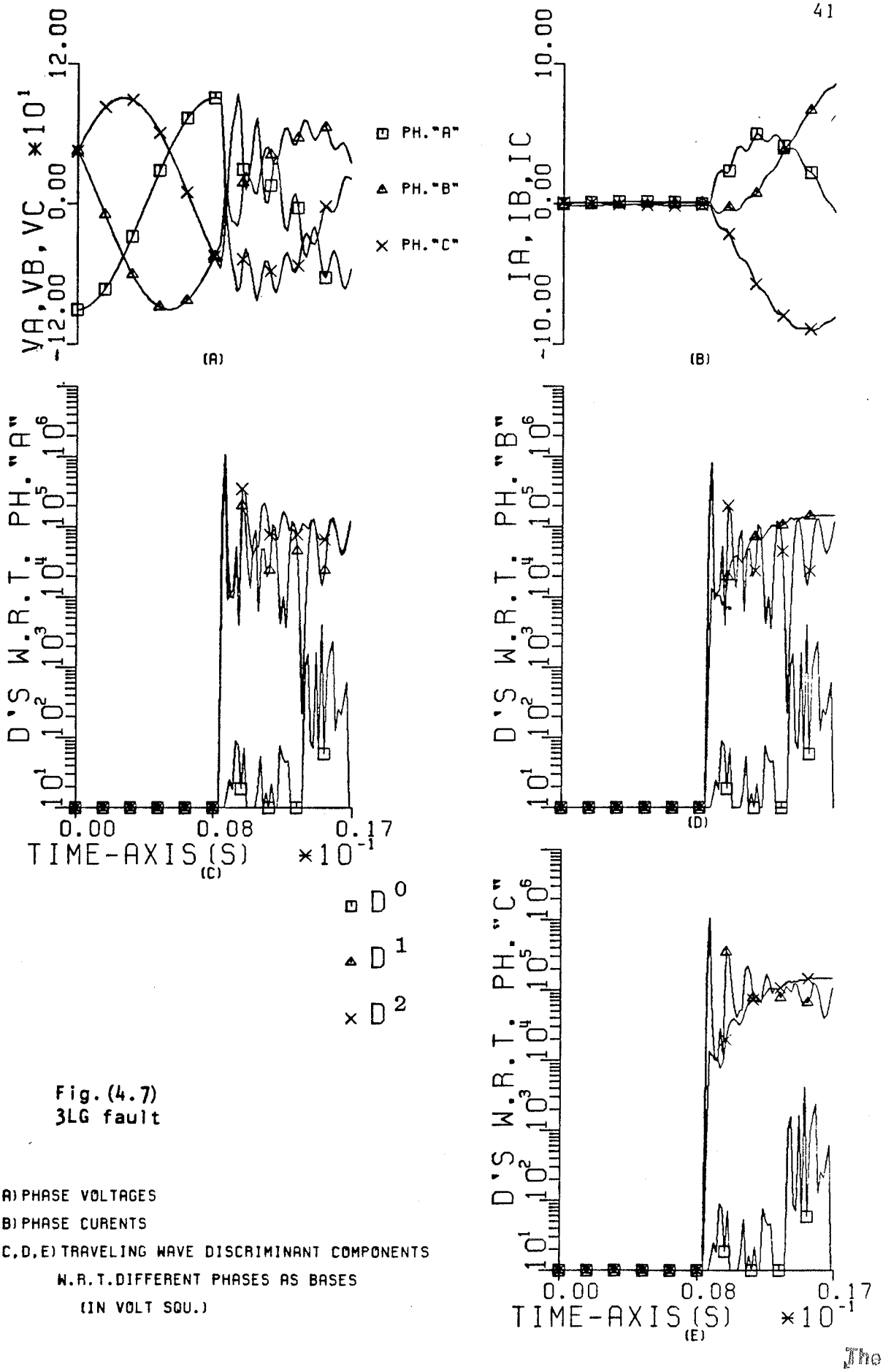



Fig. (4.7)
3LG fault

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

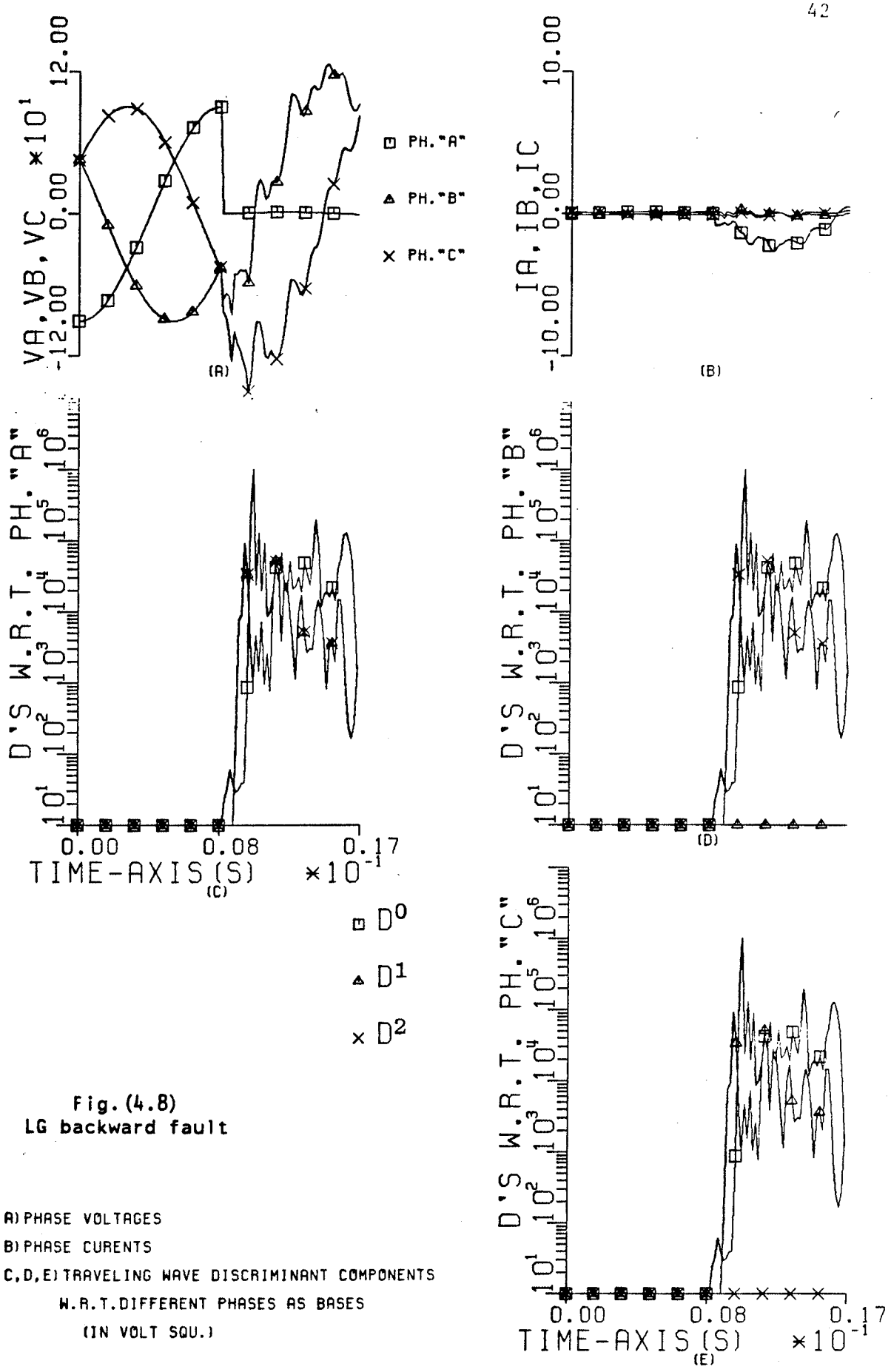



**Fig. (4.8)**
**LG backward fault**

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

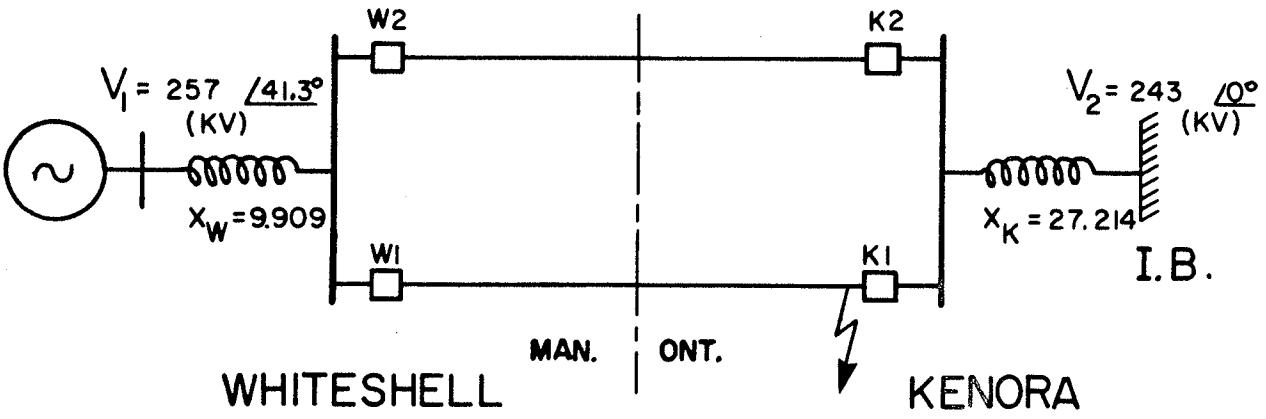
As shown in Fig.(4.8), unless a direction discrimination is considered the relay could detect the backward fault as a forward one. The backward discriminant components in this case of backward fault converge (exceed a threshold) in sufficient time ahead of the convergence of the forward ones (right after fault inception for this close-in backward fault).

### 4.3.2 DOUBLE CIRCUIT 230 KV SYSTEM

The system considered in this case is the one shown in Fig.(4.9). This transmission system is derived from the Manitoba-Ontario (Whiteshell-Kenora) 230 KV double circuit connection line. The Kenora terminal is considered as an infinite-bus (IB), while the Whiteshell terminal as a generating-bus. A certain loading condition, defined by the terminals' voltages (magnitude and angle), is considered. The transmission tower configuration for each circuit is the one shown in Fig.(4.9.b).

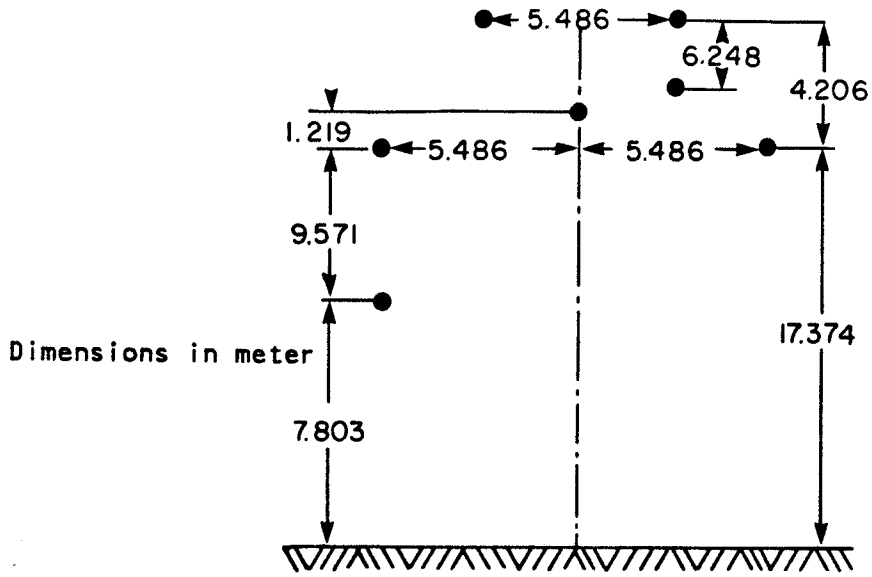
Through simulating this system, the effects of the following practical considerations on the developed principle are investigated.

1. Prefault loading condition.
2. Line parameter frequency dependence.
3. Nontransposition between different conductors.
4. Double circuit transmission system (with the involved mutual coupling).




a) Circuit diagram

Line length = 128.91 Km




b) Tower configuration for each circuit.

Distance between circuits = 33.53 m

Fig. (4.9) Double circuit 230 KV study system.

Samples of the study conducted on this system are considered here, and more are considered for real time testing on the implemented prototype in Chapter 7.

For the Karrenbauer-based transform, again, and for a solid L-G fault only at K1, the simulation results are given by the sets of characteristics shown in Fig.(4.10) to Fig.(4.14). The first three figures correspond to the detailed representation by considering complete nontransposition between the conductors and parameter frequency dependence. The first one, Fig.(4.10), shows the behaviour at the relaying point K1, i.e. the fault point. The second, Fig.(4.11) stands for the relaying behaviour at any of the other transmission circuit ends, i.e. W1 or W2, which are the same for this location of fault. The third, Fig.(4.12), concerns the relaying behaviour at K2, which sees this fault as a backward one. The last two figures (Fig.(4.13) and Fig.(4.14)) are for the same locations as the first and third respectively, i.e. K1 and K2, but with a simple representation through ideal transposition and non-frequency dependent parameters.

From the study conducted on this system, it is concluded that the developed relaying principle which was based originally on an ideal line (Chapter 3), operates correctly for "real lines" with the involved practical aspects considered above. This means that the major capabilities of the relaying principle (namely: faulted phase selection and fault classification, highly decisive nature and fault inception angle independence), are still valid when used with real lines.

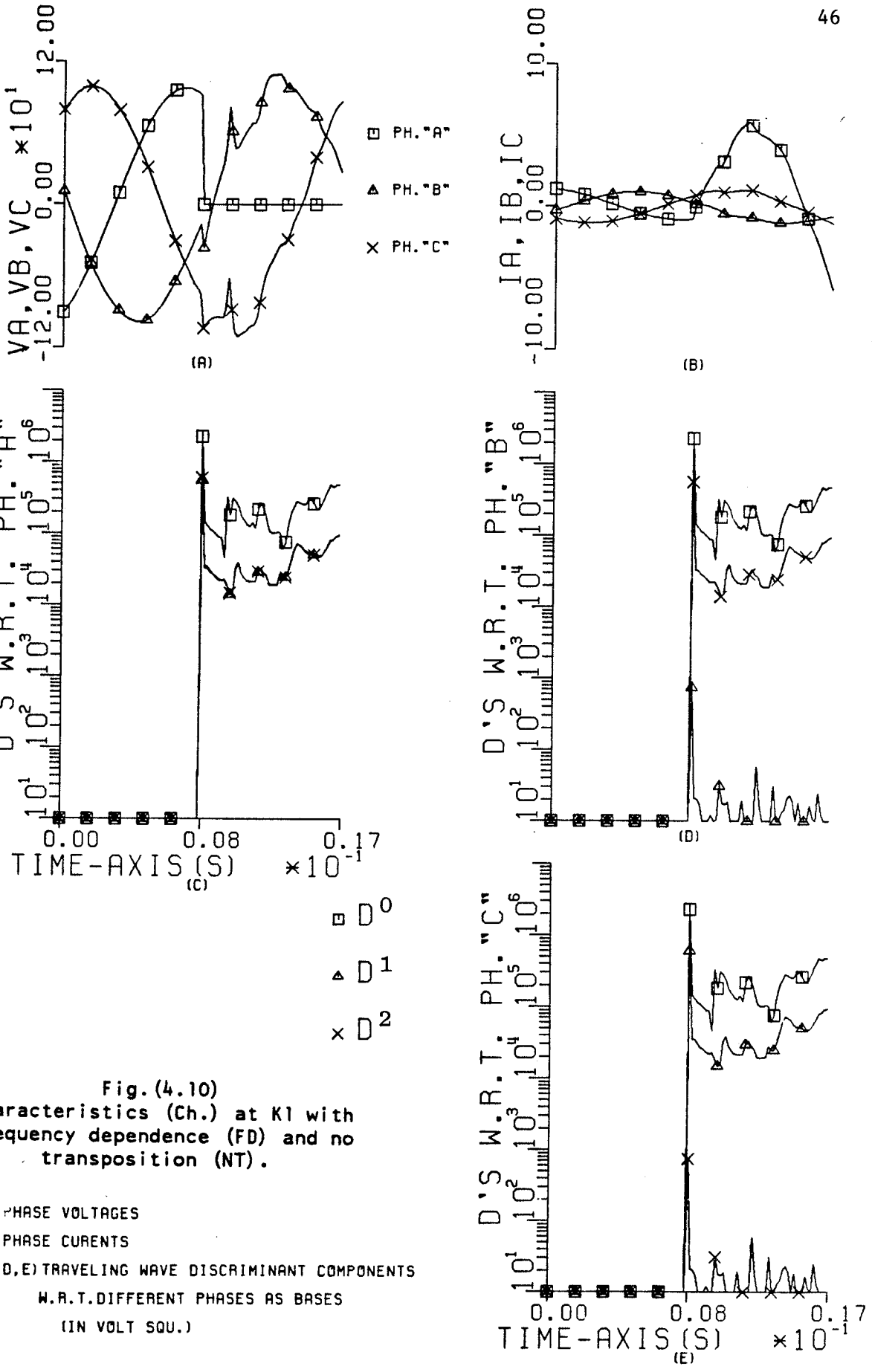



**Fig. (4.10)**
**Characteristics (Ch.) at K1 with frequency dependence (FD) and no transposition (NT).**

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS W.R.T. DIFFERENT PHASES AS BASES (IN VOLT SQU.)

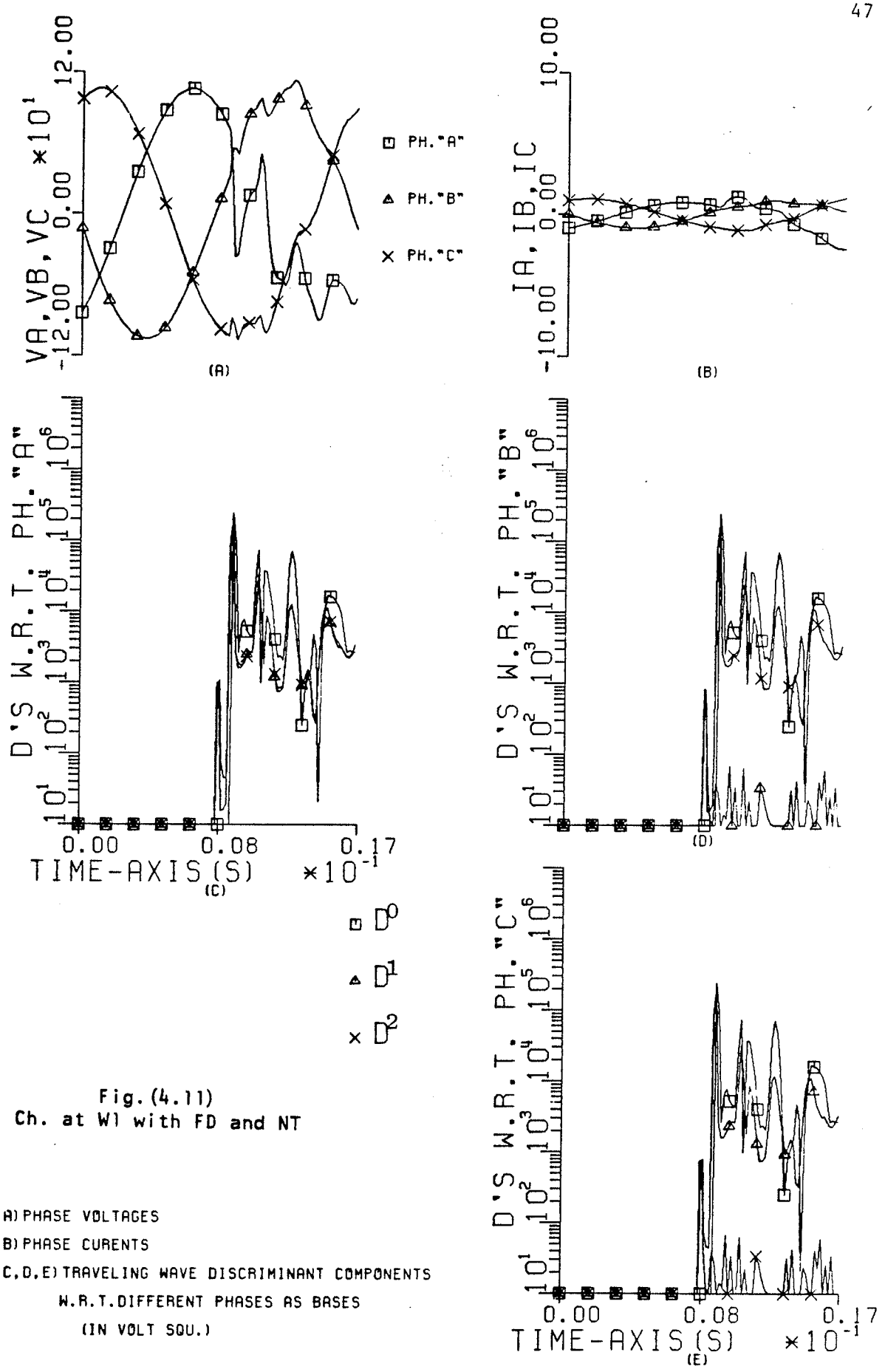



Fig. (4.11)
Ch. at W1 with FD and NT

A) PHASE VOLTAGES

B) PHASE CURENTS

C, D, E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

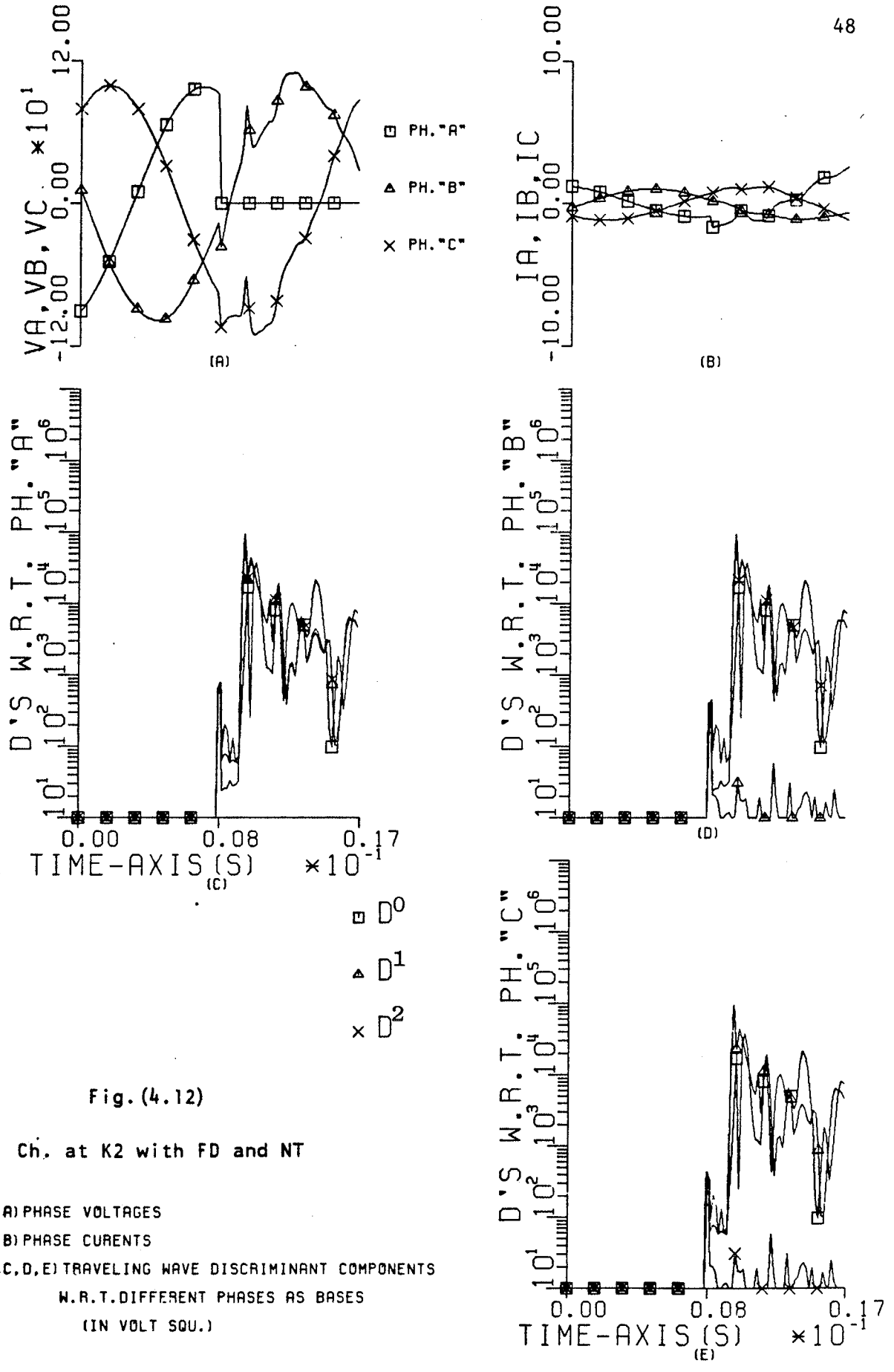



Fig. (4.12)

Ch. at K2 with FD and NT

A) PHASE VOLTAGES

B) PHASE CURENTS

C, D, E) TRAVELING WAVE DISCRIMINANT COMPONENTS W.R.T. DIFFERENT PHASES AS BASES (IN VOLT SQU.)

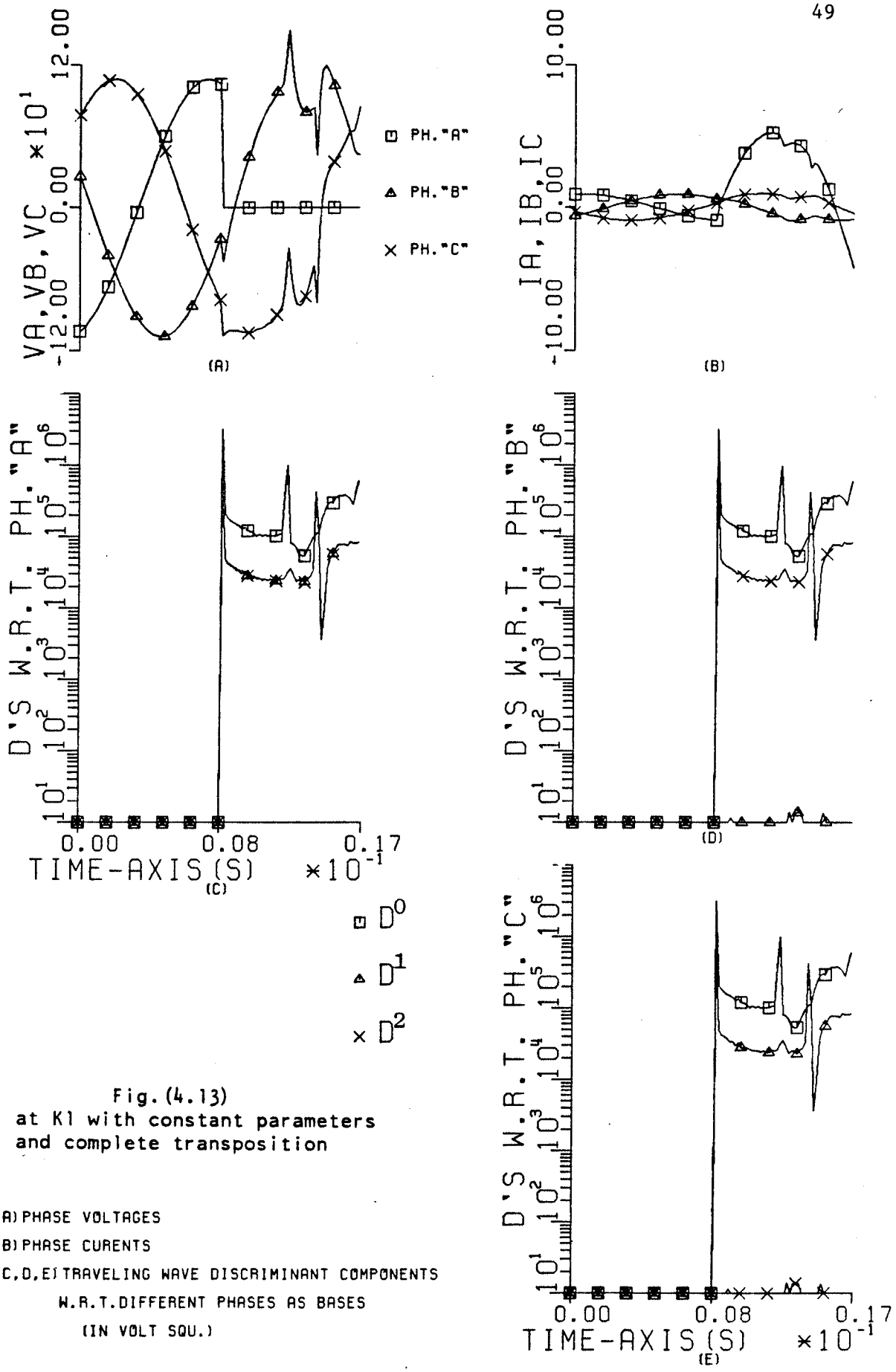



Fig. (4.13)
Ch. at K1 with constant parameters
and complete transposition

A) PHASE VOLTAGES

B) PHASE CURENTS

C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

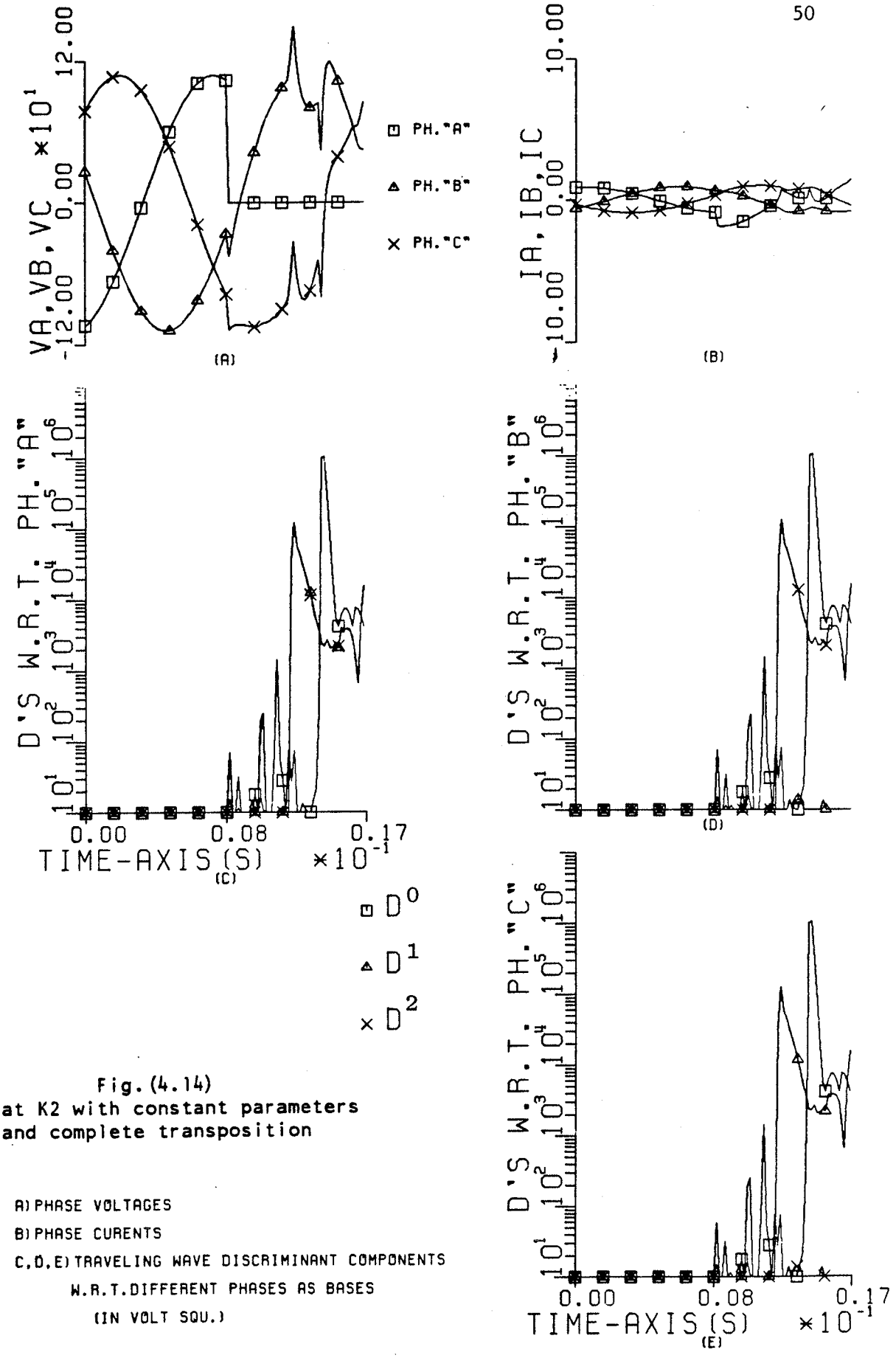



Fig. (4.14)
Ch. at K2 with constant parameters
and complete transposition

A) PHASE VOLTAGES
B) PHASE CURENTS
C,D,E) TRAVELING WAVE DISCRIMINANT COMPONENTS
W.R.T. DIFFERENT PHASES AS BASES
(IN VOLT SQU.)

## 4.4 CHARACTERISTIC FEATURES OF THE PROPOSED RELAYING SCHEME

The following conclusions were based on the analysis of the developed relaying principle as well as the computer numerical study. These and further conclusions will be investigated through real time testing of a realized prototype based on this relaying algorithm (Chapters 6 and 7).

1. The values of the different discriminant components after fault inception are supposed to be, ideally, equal to the corresponding values given on the tables (Chapter 3). However, the different practical aspects (e.g. nontransposition, line lossses, parameter frequency dependence and different wave reflections) cause a deviation from these values listed in the tables. For example, the value of the high components are inversely proportional to the distance to the fault due to the wave attenuation along the line. Nevertheless, there is a dynamic decisive change in the proper components right after fault inception, which stays very high as long as the fault is sustained. The proposed relaying scheme is based on this relative change and not in its precise value.
2. Based on fast calculation of the backward discriminant components (say $D_B^1$ and $D_B^2$) with respect to one phase as a basis, and simultaneous calculation of the forward "D's" ($D_F^0$,$D_F^1$,$D_F^2$) with respect to each phase as a basis, the fault direction, the forward fault type and the forward faulted phases could be defined within less than a quarter of a power frequency cycle, thus achieving the ultra high speed (UHS) requirement.

3. From the above-mentioned conclusions it follows that the proposed relaying scheme could utilize two different modes of operation (as with [1]):
   a) Dependent mode, through which the relay works in conjunction with the communication channel to provide complete pilot protection for the majority of the faults. The direction decision (forward or reverse) and the phase selection and fault classification are made independently at each line terminal and then a trip signal for internal faults (or blocking for external faults) is provided over the channel.
   b) Independent mode, which operates independently of the communication channel to provide faster one-end tripping for the severe close-in faults which result in higher dynamic discriminant components. Faulted phase selection and fault classification still apply for this mode.
4. To achieve security against switching operations the transducers should be on the line side of the circuit breaker as has been considered with other schemes (e.g. [1], [8], [16]).
5. Conventional transducers are convenient for this scheme. Their inherent cut-off frequency, 1 KHz [28], helps in eliminating the travelling wave caused by lightning strikes (MHz harmonic content), which could occur midway on a protected line.
6. Since the relay decisions are supposed to be done in less than a quarter of a cycle after fault inception we can say that this scheme, like some others (e.g. [1], [8]), is not affected by current transformer saturation.

7. Since for close-in faults the change in the voltage is quite large and the proposed relaying scheme effectively utilizes the change itself, the ratio of the signal to the noise generated by the CVT will be high enough to ensure correct operation of the relay which combines, in its decisions, this change in voltage with the significantly high close-in fault change in current.
8. Once the proposed scheme detects a disturbance and makes the corresponding decisions, it must block itself for a convenient time (e.g. five cycles for forward faults) in order to avoid hazard decisions during the fault clearing period (opening and reclosing circuit breakers). Thus it cannot operate for the condition of sustained fault autoreclosure and if another fault occurs internally during the blocking period initiated by a backward disturbance. Moreover, this system is not expected to operate in the condition of switching-into-fault since one period of power frequency in steady state operation (reference cycle) has to elapse before correct decisions are obtained. This drawback (in all travelling wave based fault detectors) could be nullified by providing conventional backup relaying to protect the line for such contingencies [5].
9. The performance of the proposed relaying scheme with high fault resistance is expected to be much better than that of conventional schemes. This was partially confirmed by a study conducted with another scheme [8] which is based on a lower convergency algorithm which depends on fault inception angle (since it detects the faults through the wave characteristic in

equations 2.11 and 2.12). Hence it is expected that this highly decisive scheme will have better performance.

# Chapter V

# MULTI-MICROPROCESSOR REALIZATION

## 5.1 INTRODUCTION

The use of multiple microprocessor systems extends the range and capabilities of a single microprocessor to more complex areas previously in the domain of large computers and leads to other system enhancements such as improved reliability and ease of design [29-39].

A "multiprocessor" is one of the two extreme categories of multiple processor, namely the tightly coupled one. A "computer network" represents the second category, i.e. loosely coupled [35]. There are other structures which combine the better qualities of each, which are more suitable for microprocessor-based systems. These moderately coupled microprocessor-based systems are known as multi-microcomputer (or distributed intelligence microcomputer) systems. The main characteristics of these systems are discussed in detail in [35] , [36] and [37].

This chapter concerns a general approach for multi-microprocessor realization of the developed relaying principle. A general topology which could be used with any transform (Clark, Karrenbauer or Wedepohl) is presented. The corresponding hardware and software general features are described. The value of a multi-microprocessor realization in protective relay design is discussed at the end of the chapter.

## 5.2 MAIN PRINCIPLES OF OPERATION

The device which can detect the faults through the developed relaying principle is expected to be able to calculate concurrently (within each sampling period) all of the forward discriminant components with respect to each phase and the backward discriminant components with respect to only one phase. It should then sense the situation by comparing these components to each other and to a tripping threshold. This main mode of operation is summarized in Fig.(5.1) and could use any of the decision charts presented in Chapter 3, depending on which modal transform is used.

The multi-task feature arises because of the necessity of simultaneous calculation of the discriminant components based on one piece of data with different bases. This leads to a multiprocessor as a convenient digital realization approach [35].

## 5.3 HARDWARE AND SOFTWARE GENERAL FEATURES

Since our system is supposed to be a dedicated special purpose system rather than a general one, it should achieve the objective through as simple a hardware and software construction as possible. This should be realized without sacrificing the main advantage of building a multiprocessor system i.e. the simplicity and modularity of additional hardware [32,35]. Another feature with the proposed system is the possibility of building it up using readily available microcomputers.

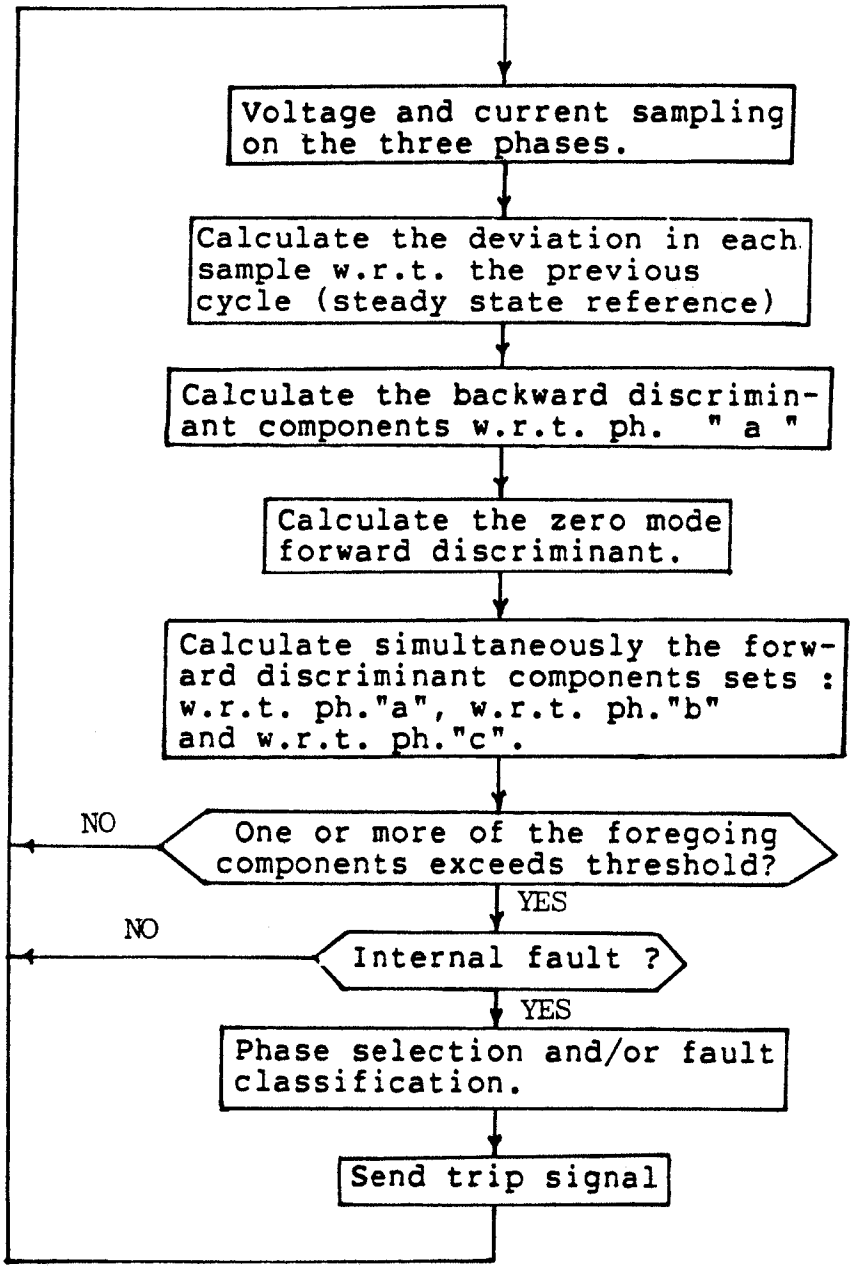



Fig.(5.1) Simplified flow-chart of the relay

A thorough investigation led to considering the two-level hierarchical configuration shown in Fig.(5.2) as a topology consistent with the algorithm. This topology consists, in general, of a master and co-master, as one powerful machine, at one level and three slaves in the second lower level. The functions of each are summarized below.

### 5.3.1 MASTER AND CO-MASTER FUNCTION

The master and the co-master work as one powerful processor which synchronizes the whole relay. The main features of their assignment include:

1. Sampling the six signals and processing them by calculating the differential quantities which are then sent to the slaves.
2. Calculating the common discriminant components, namely the backward ones and the mode zero of the forward ones.
3. Phase selection and fault classification decisions.
4. Sending of the tripping orders and information.
5. Blocking the relay for a convenient short period following a decision, to prevent false operation due to noise.

### 5.3.2 SLAVES FUNCTION

Each of the three slaves, which are identical (same hardware and software), handles the specific problem of calculating the three forward discriminant components with respect to a different phase as a transformation basis.

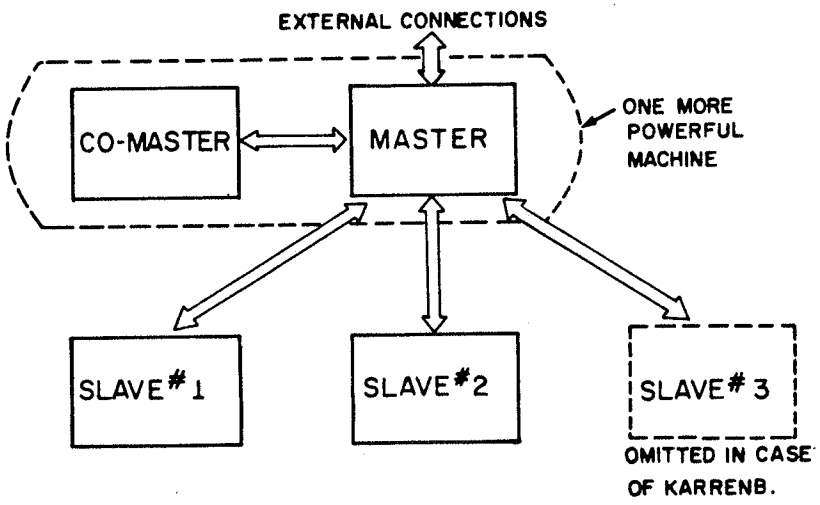



Fig. (5.2) Master-slave multi-microprocessor configuration used with the developed algorithm.

Since the Karrenbauer decision chart (Fig. 3.1.b) shows that its capability of achieving phase selection and fault classification can be realized with only two sets of forward discriminant components rather than three, the implementation based on the Karrenbauer transform reduces the number of slaves by one, i.e. there will be only four microcomputer boards rather than the five necessary for the Clark and Wedepohl transforms.

## 5.4 DATA ACQUISITION SYSTEM

The data acquisition system in the proposed prototype has six fast high resolution analog-to-digital Converters (ADCs) to handle the parallel digitizing of the three secondary phase voltages and the three secondary voltage-converted phase currents ($Z_1 i$, where $Z_1$ is the corresponding positive sequence surge impedance). Depending on the mode of operation of the ADC, some devices like a sample-and-hold and a conditioning circuit could be added to the data acquisition board.

All sampling operations are controlled by the master or the co-master processor.

A laboratory prototype based on the Karrenbauer transform was designed in the course of this study. The details of the hardware and software involved with the prototype and the testing results are reported in the next two chapters.

## 5.5 MULTIPLE MICROPROCESSOR AND PROTECTIVE RELAYS

In the recent literature three different approaches for realizing multi-microprocessor-based distance relays have been presented [29,30,32]. Two of them (Bornard, et al [29] and St-Jacques, et al [32]) are in actual service with different capabilities and good tested performance. The third (Jeyasurya and Smolinski [30]) is a laboratory prototype, which again showed good performance under real time laboratory testing.

In the Bornard scheme a hierarchical topology of one master and three slaves (16-bit microprocessors) is considered. This system incorporates single-phase tripping, directional discrimination and power-swing detection as well as the main function of impedance relaying. A tripping signal is sent within one period of 50 Hz for all faults (half a period for close-in faults).

The second relay (St-Jacques) consists of eight parallel microcomputers. Each processor performs a specific function and the results are obtained from a series of parallel and sequential computations. The relaying functions include impedance, overcurrent, overvoltage and line check algorithms. Moreover, special features such as autocalibration, display, and local/remote monitoring are incorporated. The reported tests show that the detection times recorded for the majority of the faults were on the order of one 60 Hz cycle (less than one-half cycle for the very intensive faults).

The laboratory prototype of Jeyasurya scheme has been built using two single board microcomputers for the purpose of achieving simultaneous

real time filtering of the voltage and current signals and computation of the apparent impedance "in parallel". The test results demonstrate the ability to detect any type of fault in less than one 60 Hz cycle after the fault occurance.

The reasons for considering a multi-microprocessor realization approach in protective relaying schemes could be divided into three major points.

1. Achieving high reliability and security. This is due to the inherent redundancy in most multi-microprocessor systems. In addition, higher reliability can be achieved not only by duplicating the physical elements, but also by duplicating the various tasks in more than one processor. Hence a fault-tolerant system could be obtained. Moreover, the other reliability measures, i.e. flexibility, serviceability and availability are much enhanced in these systems [32,35].
2. Enhancing system performance through enhancing the cost-performance relationship and increasing the system throughput (which is defined as the reciprocal of the time required to execute a given set of algorithms and is measured in terms of number of operations per unit time [36]). This is mainly achieved through partitioning the system functions into slightly dependent tasks that each of the several processors can handle concurrently or "in parallel".

3. Facilitating system design and development measures. This is basically due to the system modularity which can be defined in terms of the compactness and isolation of all the different elements in the system. Modular system designs will generally shorten development and debug time as well as facilitate serviceability due to the fact that independent hardware and software modules with reduced complexity are designed and implemented. Moreover, using the modularity property a multi-processor system can be upgraded to meet a new requirement at minimal cost and this could prolong system life.

Moreover, a multi-processor approach could be considered as a step for integrating the system protection and control into network-automation systems which lead to enhanced operation and supervision [31].

# Chapter VI

# THE LABORATORY PROTOTYPE

## 6.1 INTRODUCTION

This chapter concerns the details of the hardware and software structures of a laboratory prototype for realizing the relaying principle. The prototype algorithm is Karrenbauer-transform based. Although slightly less effective for fault classification, the Karrenbauer-transform-based algorithm shows great simplicity in implementation when being compared with any of the Clark or Wedepohl algorithms. A slight adaptation in the definition of the discriminant function "D" is introduced for the sake of simple programming and to have the system comparable with some other travelling wave relays [8,9].

The nomenclature used with the system in this chapter is consistent with that of other multi-microprocessor literature [29-39]. A microcomputer consists of an interconnected system of microprocessor, memory, and input/output devices. A multi-microcomputer , or alternatively a multi-microprocessor, system is a collection of coupled microcomputers. In the context of multi-microcomputers, a microcomputer is also called a processing element (PE). The terms "processor" and "computer" are used interchangeably.

## 6.2 DESIGN CONSTRAINTS

The environment of this project at its beginning (late in 1982) consisted of a microcomputer laboratory with 8-bit hardware/software development facilities. All these facilities were oriented towards the 6800 family ([40,41]). In particular, 6802 CPU-based single board computers (SBC) were already available.

Given this environment, the Motorola 6802 microprocessor was selected to exploit existing hardware and software resources. However, it should be noted that this microprocessor belongs to an 8-bit type not specially designed to be used in multi-processor systems. Therefore the functions necessary for the implemented multi-processor prototype have been added by means of external hardware and special software.

## 6.3 HARDWARE DETAILS

The design of a system using a multi-processor structure involves several problems. The three major problems are [36]:

1. How to define the most suitable and simple hardware architecture.
2. How to define the activity coordination and the flexible control scheme between the various PEs in such a way as to cope with the timing restrictions for such a system.
3. How to define the best modes of communication between the processors in order to counteract the negative aspects of microprocessors, namely the limited input/output (I/O) flexibility and the memory-processor bottleneck.

A detailed discussion is given in this chapter on multi-microprocessors as they relate to the realization of a prototype, and how the above three problems were solved.

### 6.3.1 PROTOTYPE ARCHITECTURE

Since the relay prototype is a dedicated real time system, the control structure of the multi-processor configuration used must be as simple as possible, so that the time constraints may be met without wasting processing time on complex control schemes.

The system structure chosen for implementing the prototype is slightly different from the general architecture described in the previous chapter. It is a two level master-slave hierarchical system with only one master (M) and three slaves ('S1', 'S2' & 'S3') as shown in Fig.(6.1). The communication protocols and the assignment of each PE will be discussed in the sections which follow.

### 6.3.2 SYSTEM COMPONENTS [40-44]

The implemented prototype consists of seven boards: four PE boards (one master and three slaves), a central clock board, a data acquisition board, and finally the tri-state buffer interfacing board (interfacing the master with S1 and S2). For the wiring diagram of each board see Appendix (B).

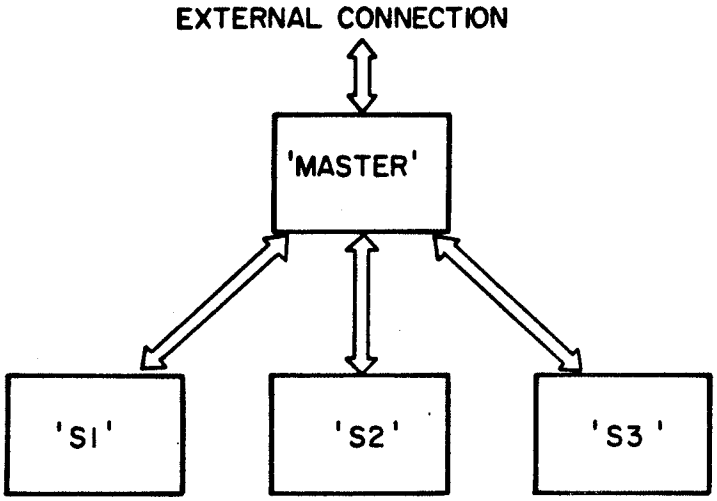



Fig. (6.1) Master-slave multi-microprocessor configuration used with the Karrenbauer-based algorithm

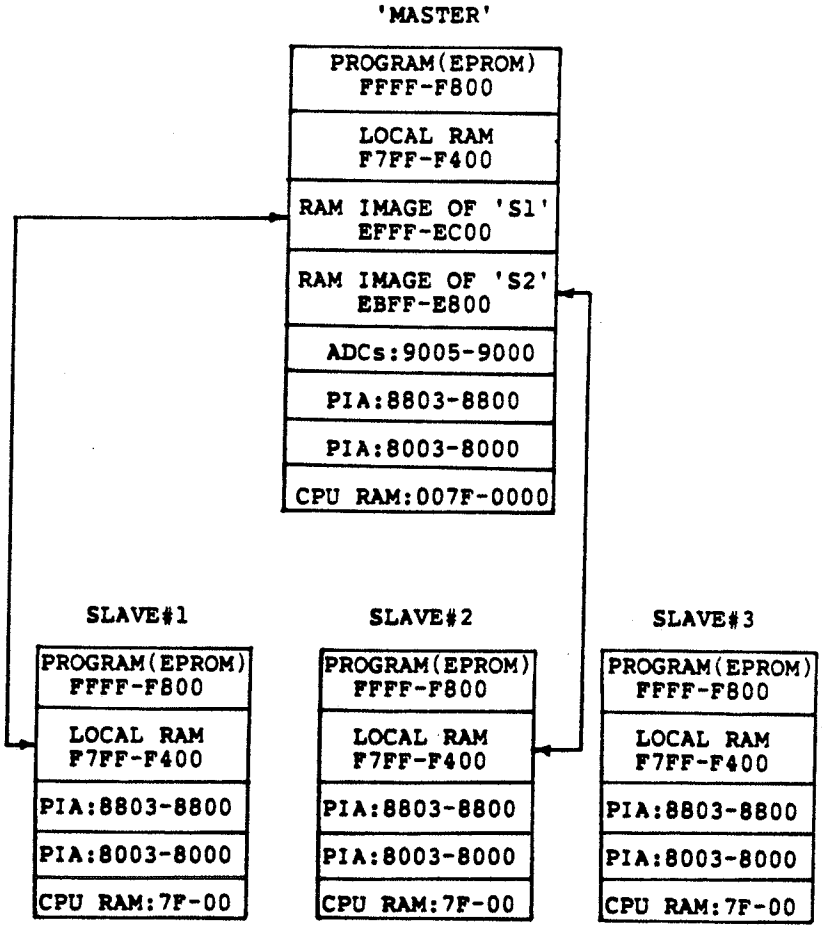



Fig. (6.2) Memory map for the master and slaves

As mentioned before, each of the PEs composing the whole system is a single board computer (U.M. SBC).[1] Each of these boards consists of a 6802 processor, RAM (1K bytes), EPROM (2K bytes), and two PIAs. One central clock for the whole system has been added in order to synchronize the operation of all the PEs.

In the context of our prototype the RAMs of 'S1' and 'S2' are mapped into the master's addressing space. This allows the master to address the RAMs of these two slaves as if they were part of its memory map. The memory maps of the different PEs of this system are shown in Fig.(6.2). It should be noted that the memory map of 'S3' is the same as that of 'S1' and 'S2', except that its RAM is not accessible by the master.

### 6.3.3 INTERPROCESSOR COMMUNICATION

Because this is a special purpose dedicated system, the interprocessor communication modes must be rigid and well defined. The interfacing between the master and 'S3' is shown in Fig.(6.3). The communication between them is achieved through two back-to-back Peripheral Interface Adapters (PIAs), the two ports of each being used for transfering data from the master to 'S3' and from 'S3' to the master. This mode of communication is called the "message mode" [34].

---

[1] U.M. SBC means University of Manitoba designed Single Board Computer.

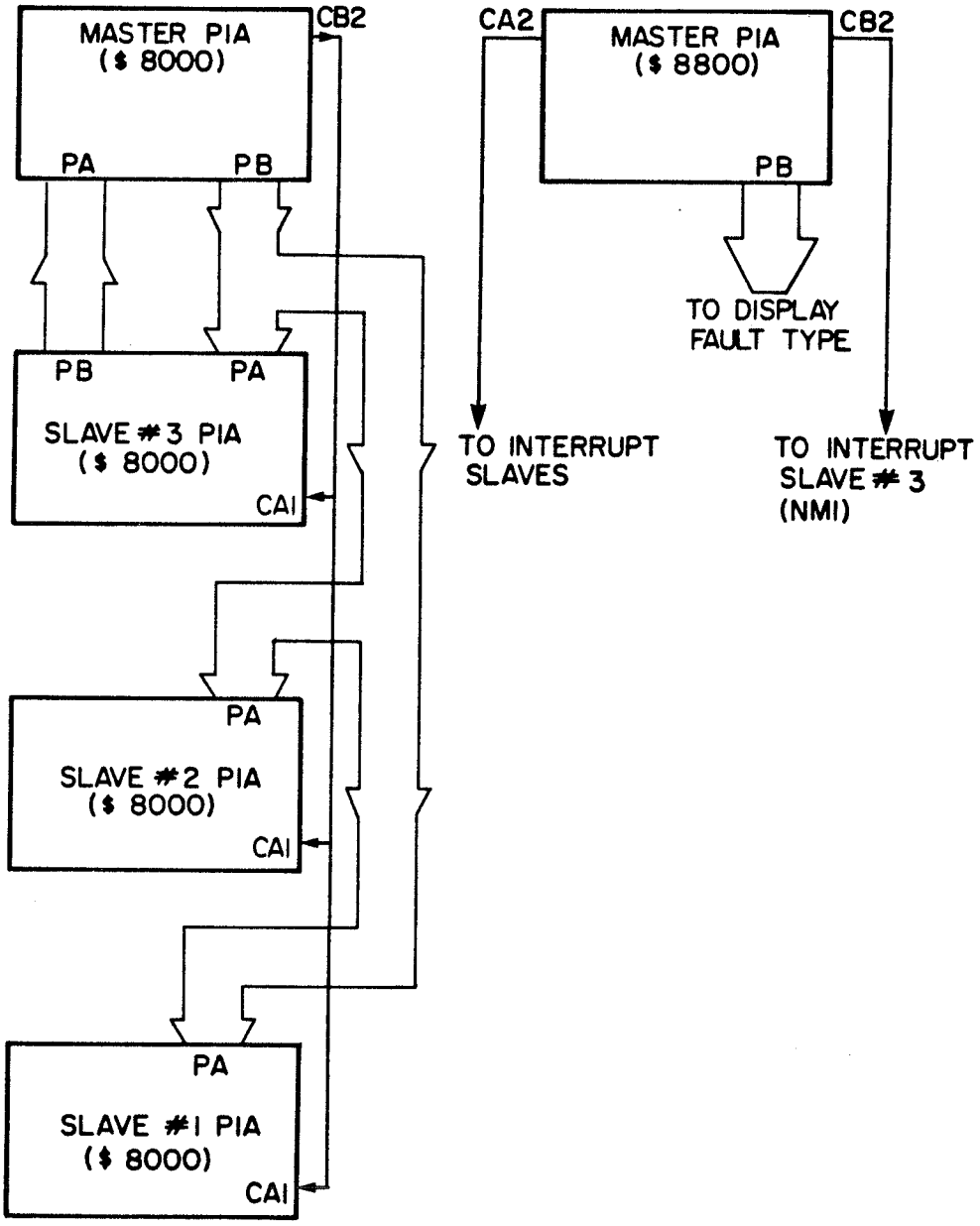



Fig. (6.3) Master-slaves communications through the PIAs

Concerning the slaves, 'S1' and 'S2', there are two different modes of communication between each and the master. The first, which is used to transfer the six sampled signals (voltages), is a broadcasting message mode from the master to all the slaves 'S1', 'S2', and 'S3' simultaneously i.e. through parallel PIAs connected back-to-back to the master's PIA. The interfacing with the slaves 'S1' and 'S2' through this mode is shown in Fig.(6.3).

The second mode of communication, called "direct mode" [34], is illustrated in Fig.(6.4). This architecture allows a distributed and limited memory sharing between the master and each of the slaves 'S1' and 'S2'.

Each of these communication memories is shared by only two processors, one of them being the master. The shared memory is always written and/or read by the corresponding slave and will be accessed by the master after detecting a disturbance. Master access to this memory could be done whenever the slave is in a wait-for-interrupt state. For this dedicated system the slaves are not allowed to access the common (master) bus. This is achieved by the one way switch shown in Fig.(6.4). The wiring details of this switch are shown in Fig.( B.3) in Appendix (B).

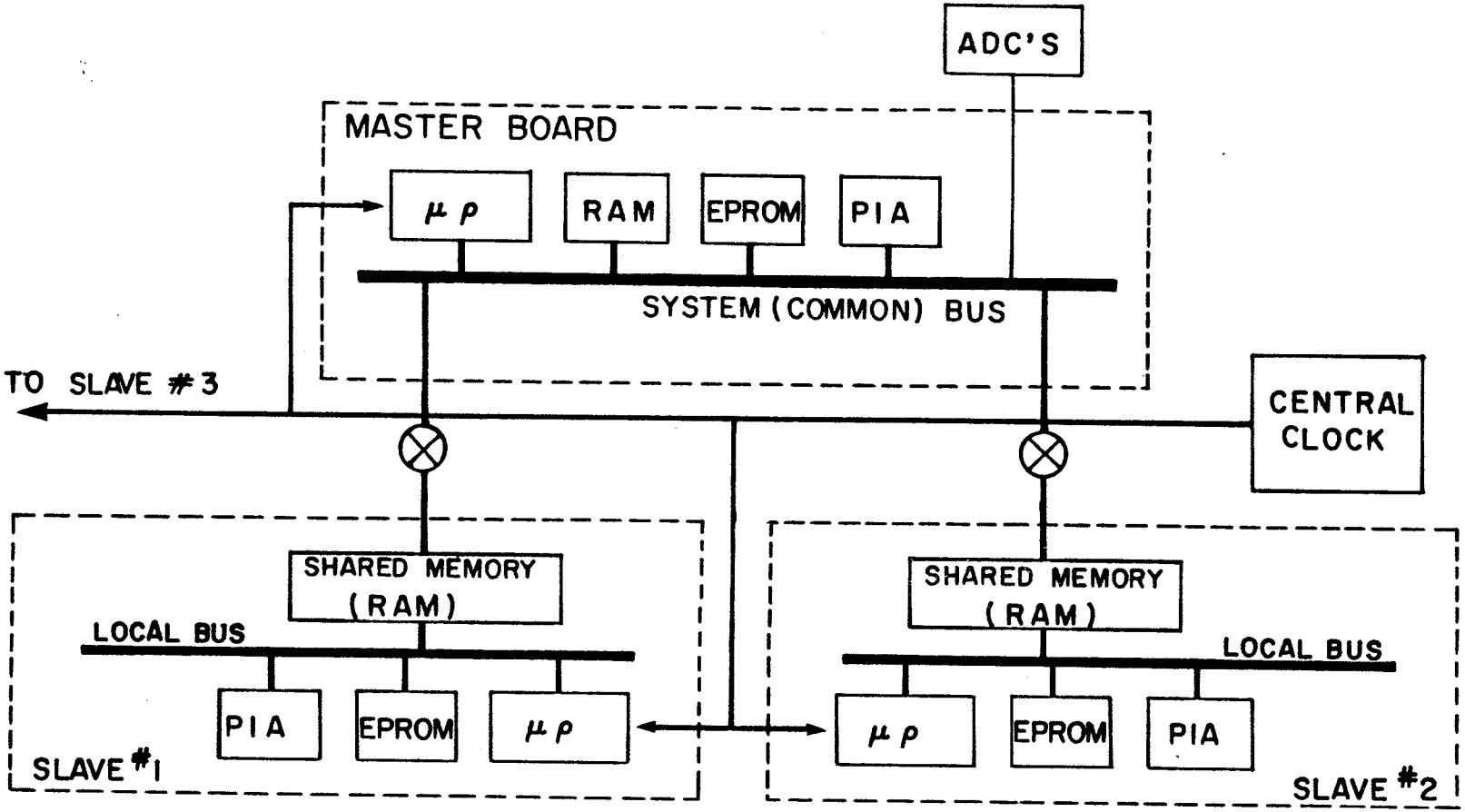



Fig. (6.4) System architecture used for shared memory interfacing between the master and the slaves (S1 and S2)

## 6.4 THE DATA ACQUISITION SYSTEM

The data acquisition system in the prototype has six parallel 8-bit analog-to-digital converters (ADCs) to manipulate the three secondary phase voltages and the three secondary voltage-converted phase currents ($Z_1 i$, where $Z_1$ is the corresponding positive sequence surge impedance).

The sampling operation is initiated by a timer which delivers a "start conversion" command to the six ADCs every 0.5 ms. This leads to about 33 samples/cycle for 60 Hz. This 2 KHz sampling frequency coincides with the sampling theorem when considering a cut-off frequency of 1 KHz for the conventional transducers as claimed in [28]. This same timer output is used to trigger six sample and hold devices in front of the ADCs. After about .1 ms, an "end-of-conversion" signal is sent by each ADC. These six "low" signals are "ORed" and then sent as an interrupt to the master CPU which can then read the sampled values by addressing the corresponding ADC since these ADCs are directly connected to the master CPU extended data bus.

To solve the problem of the dynamic range of currents, it was decided to saturate the corresponding voltage signals for values which exceed 5.0 volts (peak) on the relay side of the transducers. This solution has been found to be more practical than using two parallel ADCs on each channel (one for the low values and one for high values), because the relay decisions will be made far ahead of the peak values of high fault currents.

The wiring diagram of the data acquisition system is shown in Fig.(B.2) in Appendix (B).

## 6.5 SOFTWARE STRUCTURE

In defining the software structure, two major factors have been considered.

Firstly, the software has to be in a form to cope with the limited capabilities of the processor used, as well as the simple hardware configuration suggested.

Secondly, the software structure has to be able to provide rapid and correct detection of all the types of developing and nondeveloping faults.

In order to cope with these factors the following measures have been taken:

1. The calculations are done using integer (fixed point) arithmetic. This does not degrade the algorithm significantly because this algorithm is mainly based on "high-low" or "1-0" comparisons.
2. The system functions were distributed among the PEs such as to have a roughly equal assignment to each from a calculation time point of view.
3. A slight change in the the discriminant function definition has been introduced to help in simplifying the programming. This definition is explained in subsection 6.5.1.
4. Faulted phase selection and fault classification are based on a set of sampled signals which are delayed by one sampling period from the detection of the fault occurrence and its direction. This means that the fault detection and its direction is always

checked. If a forward fault is detected, the decisions will be based on the discriminants of the next set of sampled signals, that is one time step later. This copes with the difference in the travelling time between the aerial modes and the ground mode, besides giving correct decisions in case of fast developing faults.

5. In case of backward faults or after taking decisions for forward faults, the relay will be blocked for about five cycles (with respect to 60 HZ), in order to avoid false decisions due to the transients involved in the signals of these five cycles due the the different switching operations especially with autoreclosing schemes.

The details of the software construction are discussed in the following subsections.

### 6.5.1 THE DEFINITION OF THE DISCRIMINANT FUNCTION

As mentioned before, the definition of the discriminant function is slightly changed from the definition used in the previous chapters. This leads to simpler software and consistence with other schemes [8,9].

For a single phase line the discriminant function becomes

$$D = \sqrt{(d)^2 + (d'/\omega)^2} \qquad (6.1)$$

where d is the wave characteristic at the relay point and d′ is its derivative with respect to time,

$d = \Delta v_R - Z \Delta i_R$ for the forward wave characteristic,

and

$d = \Delta v_R + Z \Delta i_R$ for the backward wave characteristic.

This can be simply handled in a microprocessor implementation by using the "linear magnitude approximation of vector quantities" [45] as explained in Appendix (C). Using this method the approximate square root of the sum of the squares is

$$D = |d| + 1/4\ |(d'/\omega)| \quad \text{for } |d| > |(d'/\omega)| \tag{6.2}$$

or

$$D = 1/4\ |d| + |(d'/\omega)| \quad \text{for } |d| < |(d'/\omega)| \tag{6.3}$$

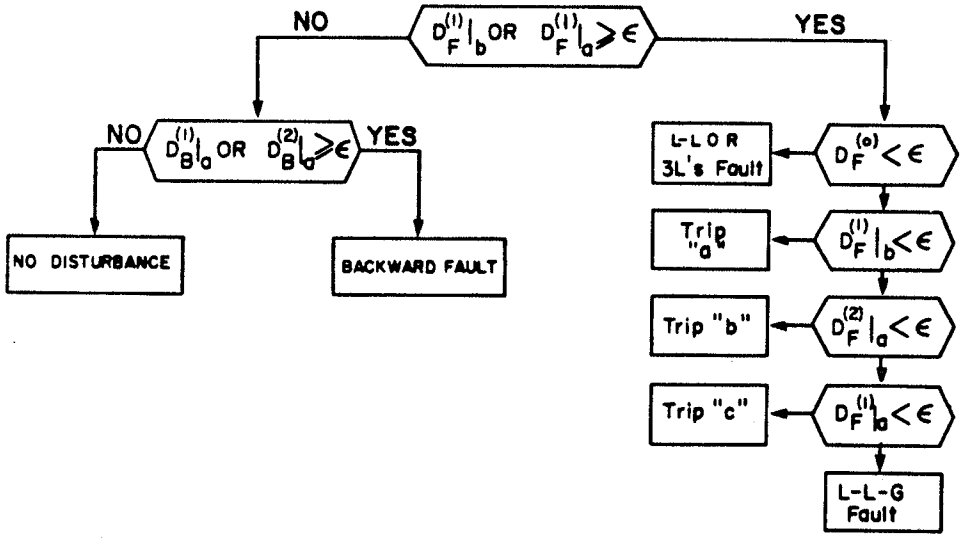
The accuracy of this approximation is acceptable, because of the "high-low" nature of the algorithm and the integer arithmetic used. This change in the definition of "D" could be considered as a matter of scaling. The main characteristics of the discriminant function mentioned in the previous chapters, i.e independence of the fault initiation angle and the possibility of combining the different modal components to achieve faulted phase selection and fault classification are still present in this adapted definition.

### 6.5.2 SPECIAL ALGORITHM FOR KARRENBAUER-BASED TRANSFORM

Recalling the faults truth table of Fig.(3.1.a), which, for convenience is shown again as Fig.(6.5.a), it can be deduced that detecting a fault, its direction, and then, if forward, selecting the faulted phase and/or classifying the type of fault, can be achieved through the following set of components:

| Fault → | | L-G | | | L-L | | | L-L-G | | | 3LS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Basis | D's | a | b | c | a-b | b-c | c-a | a-b | b-c | c-a | |
| Ph "a" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "b" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Ph "c" | $D^0$ | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| | $D^1$ | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | $D^2$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

a) Truth table




b) Flow chart

Fig. (6.5) Fault detection, direction discrimination and phase selection and fault classification based on the Karrenbauer transform

$D_B^{(1)}|_a$ (with respect to phase "a"),
$D_B^{(2)}|_a$,
$D_F^{(0)}$,
$D_F^{(1)}|_b$,
$D_F^{(1)}|_a$ and
$D_F^{(2)}|_a$

This is clearly shown in the flow chart of Fig.(6.5.b). In this flow chart the forward discriminant components $D_F^{(1)}|_a$ and $D_F^{(1)}|_b$, are first compared to a threshold. If either exceeds this threshold a forward fault is indicated. In this case the phase selection and fault classification is determined from the four forward components mentioned above, and in the logic shown in the right side of the flow chart. If none of the checked forward discriminant components exceeds the threshold, the backward components $D_B^{(1)}$ and $D_B^{(2)}$ (with respect to phase "a") are checked. If either exceeds the threshold it indicates a backward fault, otherwise the system is considered sound (no faults). In the latter case a new set of "D's" from the next sampled signals will be checked in the same sequence.

In Appendix (C) a direct formulation of each of the six mentioned "D's" at the sample number "n" is shown as a combination of the signals of this same sample and of the sample delayed by the number of samples/cycle, i.e. the reference sample.

## 6.6 OPERATIONAL DETAILS

The three flow charts of Fig's (6.6), (6.7) and (6.8) demonstrate the operational details of the master, 'S1' (or 'S2'), and 'S3' respectively.

The parallel processing of the different tasks manipulated by each PE is shown in the timing diagram of Fig.(6.9).

The following comments will help in understanding the above mentioned flow charts and the timing diagram.

1. A whole reference cycle should be read and stored sample by sample (within a time of one cycle), just after resetting. These reference samples will be overwritten by the corresponding samples of the new cycle, in the case of no fault detection. Hence, a slow change, as in power swing or a small change as a load variation, will not affect the relay operation security. About five cycles after fault detection, the whole reference cycle is refreshed, i.e. within a time of one cycle again.
2. Except for "S3", the main task of each PE changes between the 'no fault' condition and the 'forward fault' condition. In the normal system operation (no fault condition), each PE is continuously calculating one specific pre-assigned discriminant component which could exceed the threshold for a disturbance in the protected system. In this normal checking, the 'master' and 'S3' are calculating two forward discriminant components ($D_F^{(1)}|_a$ and $D_F^{(1)}|_b$ respectively). At the same time 'S1' and 'S2' are

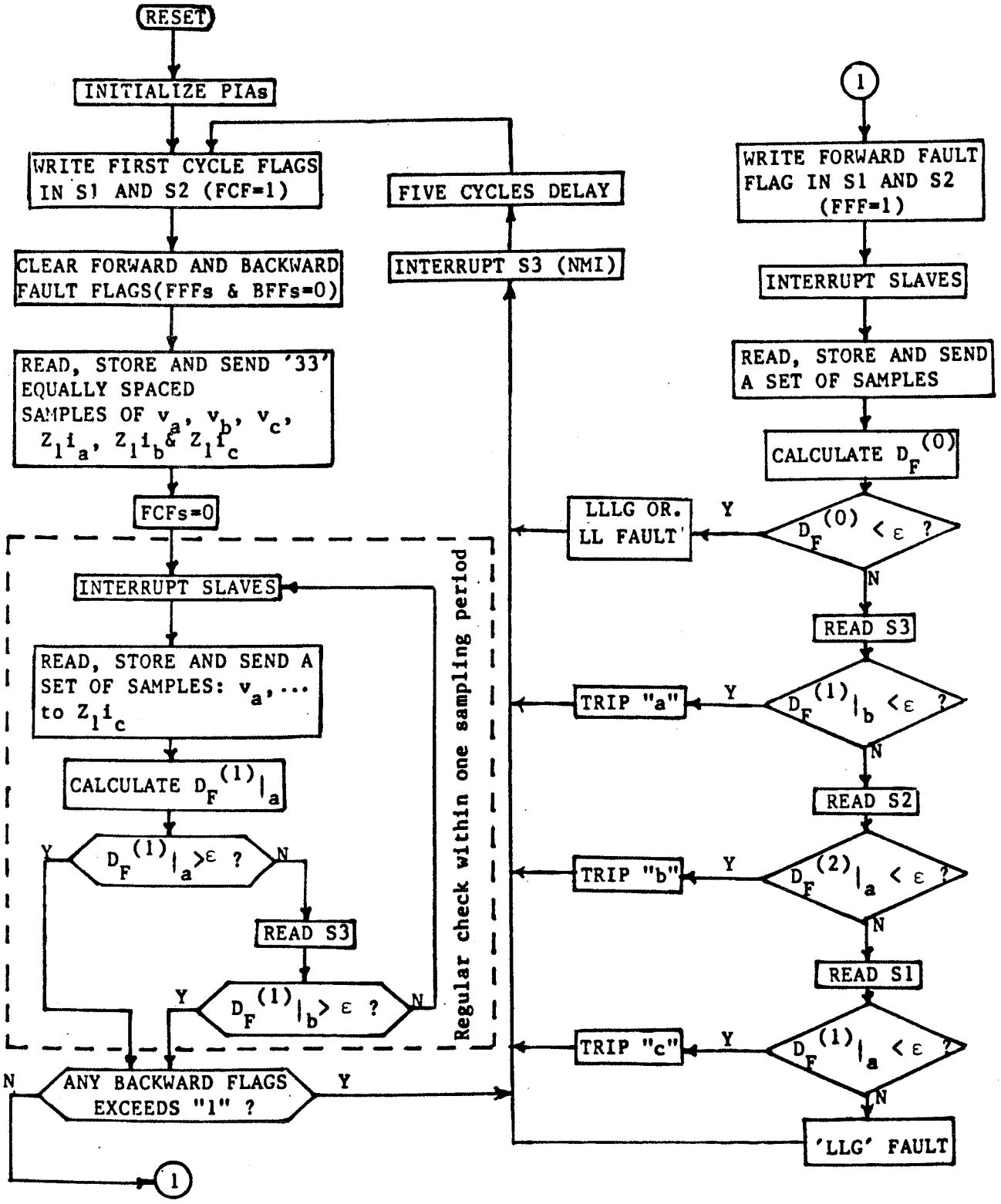
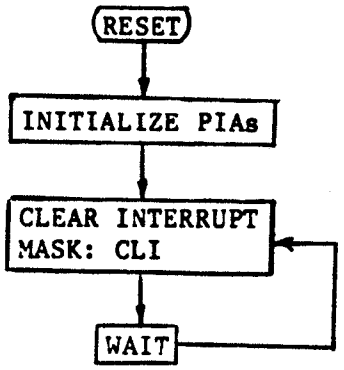
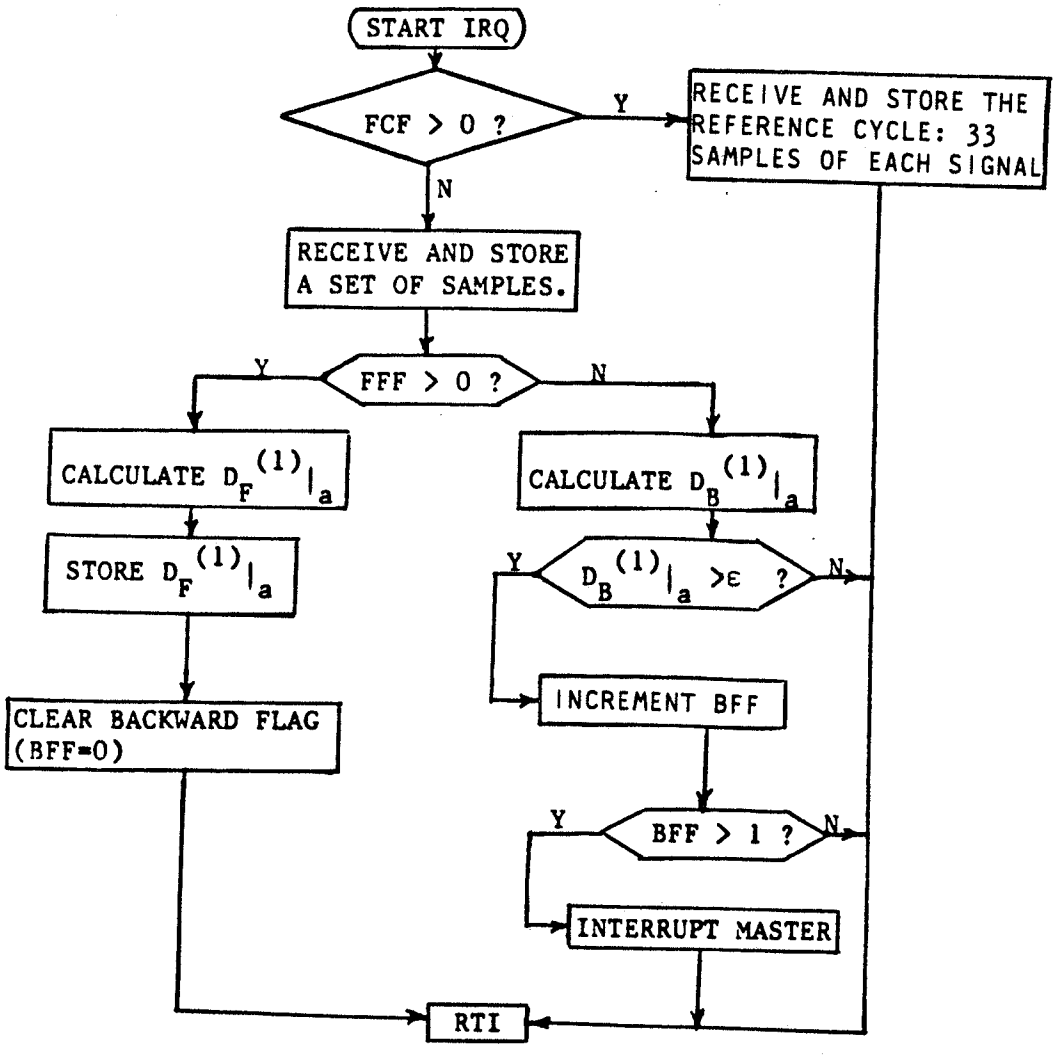



Fig. (6.6) Master detailed flow chart

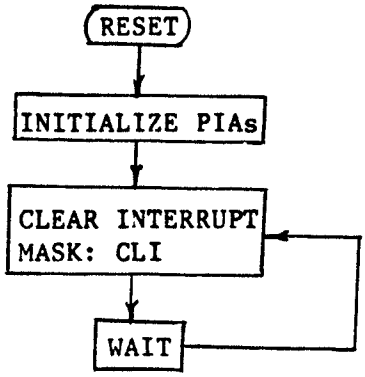



(a) Main program

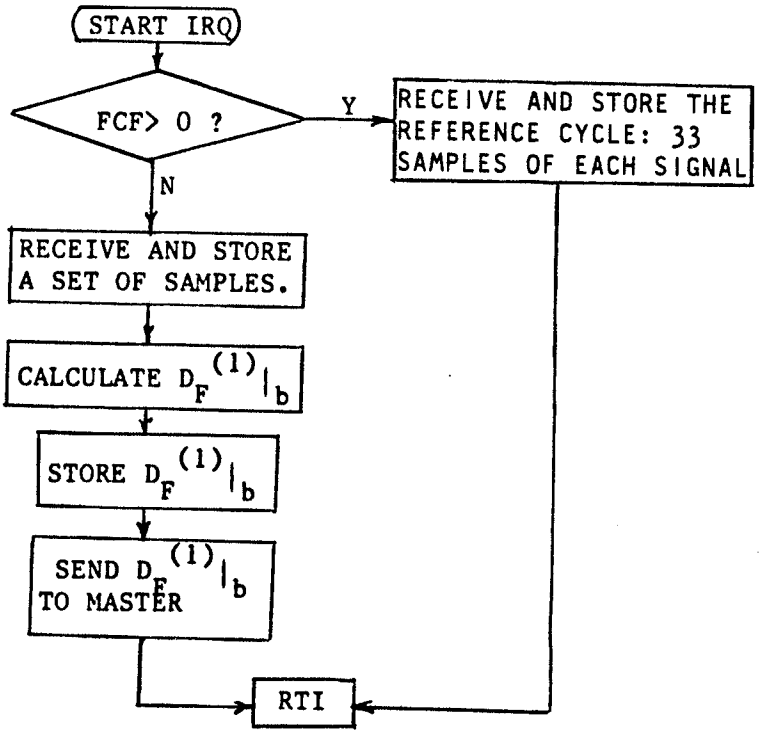



(b) Interrupt routine

Fig.(6.7) Detailed flow chart for S1 (S2 is the same with $D^{(2)}$ instead of $D^{(1)}$)

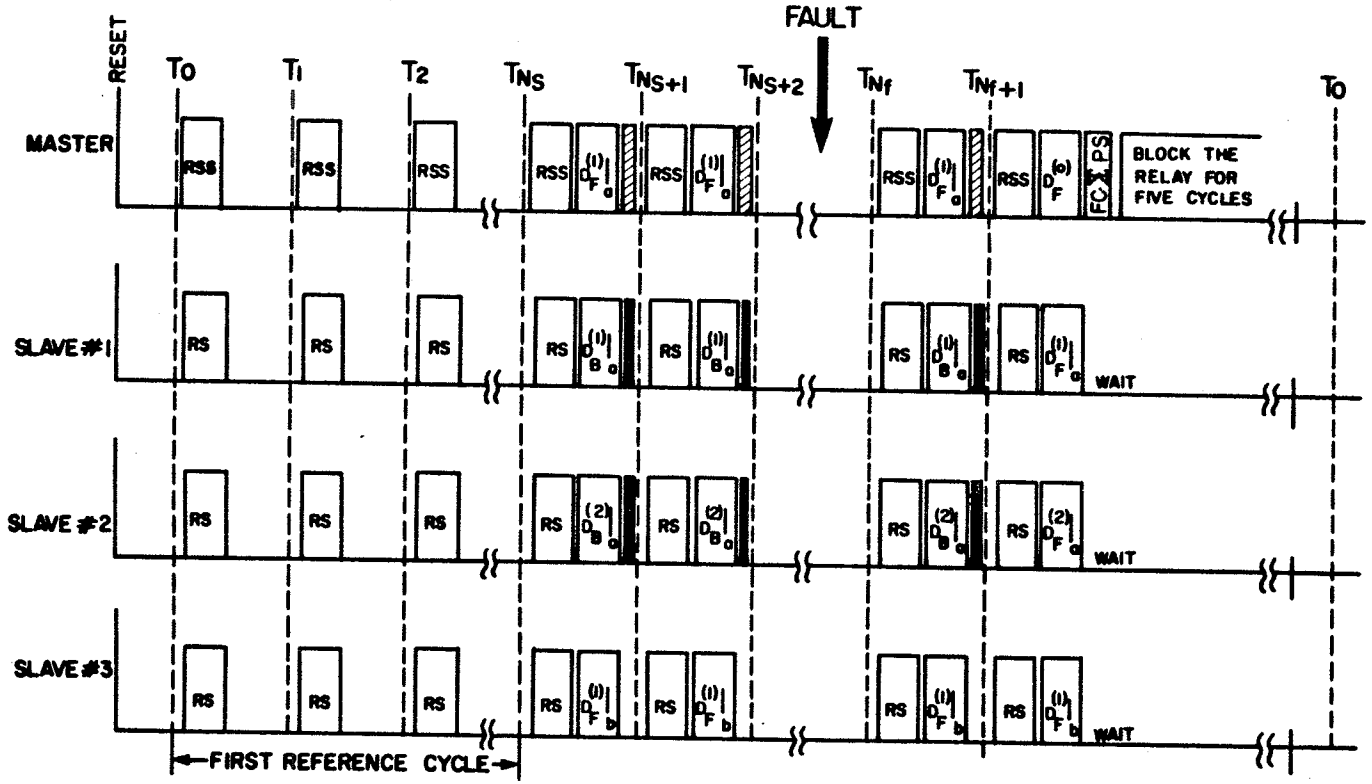



(a) Main program




(b) Interrupt routine

Fig. (6.8) Detailed flow chart for S3




RSS:read(from ADCs), store(in local memory) and send(to slaves) the six signals
RS :receive(from master) and store(in local memory) the six samples
NS =number of samples per cycle.
FC :fault classification
PS :phase selection
▨ :check, to threshold the forward discriminants calculated by the master and S3
■ :check convergence of the calculated backward discriminats.

Fig.(6.9) Timing diagram

calculating two different backward components ($D_B^{(1)}|_a$ and $D_B^{(2)}|_a$ respectively). At least one of these four components will exceed the threshold when a fault occurs. Whether the fault is backward or forward depends on the sequence of exceeding the threshold as discussed in Chapter 2.

3. The master checks the two forward components: the one calculated by itself, and the one written by 'S3' into one of the master's PIA ports. If neither exceeds the threshold, the master will ignore the backward components calculated by 'S1' and 'S2'. If, on the other hand, one of the two forward components exceeds the threshold, there is either a forward fault or a backward fault. The direction discrimination will be achieved through one of two processes depending on the mode of operation:

   a) Transfer tripping mode: In this case the master will access the RAMs of 'S1' and 'S2' to check the backward flags resident there. If either flag exceeds a preset value (say 1) it indicates that a backward component exceeded the threshold before the forward component, i.e. it is a backward fault; otherwise it is a forward fault. In this mode, for a nonsevere backward fault which can not be sensed by the master as a forward fault, the slaves S1 and S2 can reset their backward flags after a reasonable time (say when the backward flag exceeds 10). This helps in increasing the availability of the relay, and hence it can detect faults in the protected line right after the occurrence of these backward faults. Confirming a forward fault, the master will send a tripping

signal to the relay at the other protected line end. This mode is the one used to test the prototype in the next chapter.

b) blocking mode In this mode S1 and/or S2 will interrupt the master (NMI)[2] when the backward flag exceeds the preset value to indicate a backward fault. The master will respond to this interrupt by sending a blocking signal to the other end and blocking the local relay. This mode is the one shown in Fig.(6.7).

4. After detecting a forward fault a new set of six samples will be processed by the relay. In this situation the main tasks of the 'master', 'S1' and 'S2' will be changed to the calculation of $D_F^{(0)}$, $D_F^{(1)}|_a$ and $D_F^{(2)}|_a$, respectively. Since 'S3' does not change its task the hardware and software belonging to this specific PE is somewhat simplified. It should be mentioned here that the ground mode surge impedance is considered equal to three times the sky mode impedance (typically 2 to 3 times within the frequency span 60 Hz to 1 KHz [25]).

5. Each of the slaves finishes with its task within each sample period, and then waits for an interrupt by the master (IRQ).[3] When interrupted by the master each slave handles the new set of sampled signals sent to it by the master in the direction defined by the task flags resident in its RAM. In the case of 'S1' and

---

[2] NMI is the mnemonic for a "Non-Maskable Interrupt" line on the microprocessor.

[3] IRQ is the mnemonic for an "Interrupt Request" line on the microprocessor.

'S2', which each have two different tasks under the 'normal condition' and 'forward fault condition' cases, the task flags are written by the master during the WAIT mode. The refreshed reference cycle, (after resetting the relay from the five cycle blocked condition after fault detection) is recognized by 'S3' by being interrupted (NMI) by the master. The interrupt service routine in this case will jump to the first main program address for this slave ('S3').

6. The faulted phase selection and fault classification decisions are taken by the master which will access the RAM of either 'S1' or 'S2' (or both) if the fault is not a three lines-to-ground, line-to-line, or line "a"-to-ground type.

All the programs were written in Assembly language. This helps in optimizing the execution speed (see Appendix (D)).

## 6.7 SYSTEM DEVELOPMENT

The unique nature of multi-processor system debugging problems is largely a function of the interprocessor communication techniques that are employed. These techniques themselves consist of two identifiable parts: an interprocessor control/signalling mechanism, and a data transfer mechanism.

In order to cope with these problems, a typical methodology for debugging similar types of multi-microprocessor systems is suggested by Schadel in [46]. This method, in conjunction with the Applied Microsystems EM-186 6800/6802 Diagnostic Emulators, has been used to

develop the implemented prototype. The method could be summarized in the following two steps.

1. Independently debug as much of the function of each processor as possible. In this stage it should be possible to algorithmically simulate I/O from the "missing" processor(s), or to manually supply it as required from the development system console.
2. The final system integration task is best facilitated by using at least a pair of emulator modules. Emulator synchronization is important in this stage for two reasons [46]:
   a) Many debugging experiments will be initiated with the goal of observing system behaviour during specific interprocessor race conditions, contention situations and interrupt responses.
   b) When halting the execution of one processor so that the state of the system can be observed, the designer will likely want to simultaneously halt the second processor to ensure that the total system state is not altered, and to allow the system to restart execution from the state at which it was halted.

Because the available emulators did not provide synchronization lines, it was sometimes necessary to manually synchronize the two emulators.

The software required for the relay was first developed on the AMDAHL mainframe computer through the cross-assembler resident there. After being initially debugged, the programs were then downloaded to the emulators for real time debugging. Finally the programs were downloaded to EPROMs to realize the stand-alone feature of the relay.

# Chapter VII

# TESTS ON THE PROTOTYPE

## 7.1 INTRODUCTION

This chapter concerns testing and evaluating the performance of the implemented prototype. Besides the steady state tests carried out for software debugging purposes three main testing procedures were considered.

1. Off line testing of the implemented algorithm at the same level of data flow and accuracy (integer arithmetic within same artificial word length) using a mainframe computer.
2. Real time testing based on digital data downloaded to the master from the mainframe computer. This required a slight adaptation in the master program in order to cope with this artificial situation.
3. Real time testing in the actual mode of operation with analog signals.

Since relay schemes must be tested under conditions as realistic and severe as they must face in service, the third testing procedure is the one to be considered in this chapter.

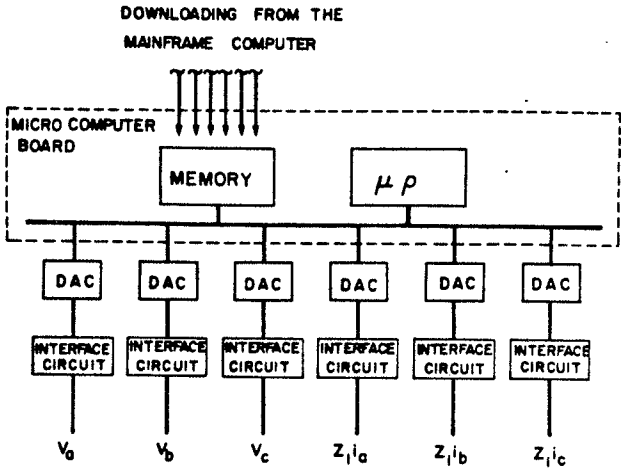
## 7.2 MICROPROCESSOR BASED TESTING SYSTEM

A new microprocessor-based scheme for dynamic testing of transmission line protective relays under conditions very close to reality was realized within the course of this study. Using the EMTP program, protected system components could be simulated accurately and in detail. Once accurate pre-fault and fault waveforms are calculated, they can be downloaded to a semi-permanent memory chip (EPROM) of modest size, and then delivered as real-time data, through amplifiers if necessary. The output stage is a microprocessor-based complex waveform signal generator (CWSG) which delivers six signals in real time: three phase voltages and three phase-current-proportional voltages.

Fig.(7.1.a) shows a block diagram of the equipment, while Fig.(7.1.b) shows the flow chart of the monitoring program responsible for delivering, in real time, the prefault and postfault quantities and the transition between them.

The EMTP voltages and currents at the relaying point are appropriately modified and then downloaded to an EPROM. In the present system, one cycle of pre-fault variables and five cycles of postfault variables are downloaded. Six digital-to-analog converters (DACs) convert the sampled signals to equivalent analog voltages. Interface filters with the proper cut-off frequency for the sampling rate of 40 samples per cycle are used to filter out the discrete levels of the outputs of the DACs. The outputs of these six filters are the inputs to the relay being tested (through appropriate amplifiers if required).

a) Block diagram




b) Operation flowchart

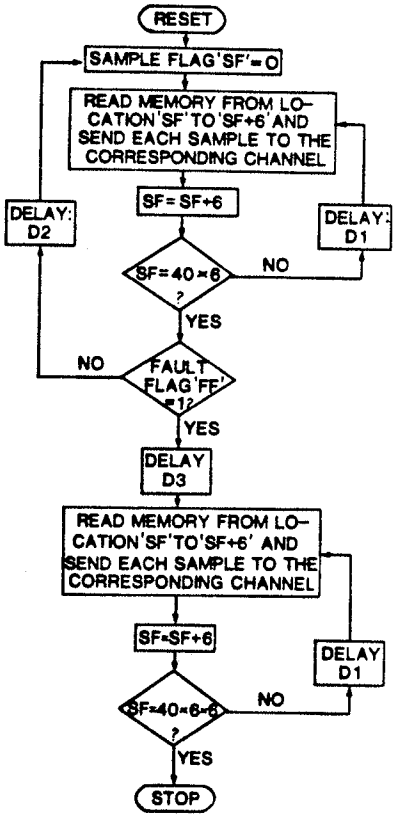



Fig. (7.1) Microprocessor-based complex waveform signal generator

The central processing unit is the 8-bit Motorola 6802 processor [41]. The DACs used are the 8-bit 1408 multiplying converters [44]. The timing is controlled by a timer which delivers an interrupt signal to the processor every 0.4 ms. Analog filtering of the output is achieved through a set of operational amplifiers, resistors and capacitors. The gain of each filter is adjustable to give an output of up to 20 volts peak-to-peak (-10V to +10V). Any signals of higher levels are clipped at these limits.

When output is first initiated, the first cycle of variables is continuously repeated, establishing a steady-state pre-fault condition for as long as desired. Then, when the "fault flag" switch is pressed (manually), the current steady state cycle is completed and the five postfault cycles are delivered to the relay being tested. A complete wiring diagram of this system is shown in Fig.(B.4) in Appendix (B).

The system is useful both for new relay development and for testing of commercial relays.

This CWSG is used for testing and evaluating the performance of the implemented prototype as shown in the rest of this chapter. The testing procedures used with this generator are summarized in the flow diagram of Fig.(7.2).

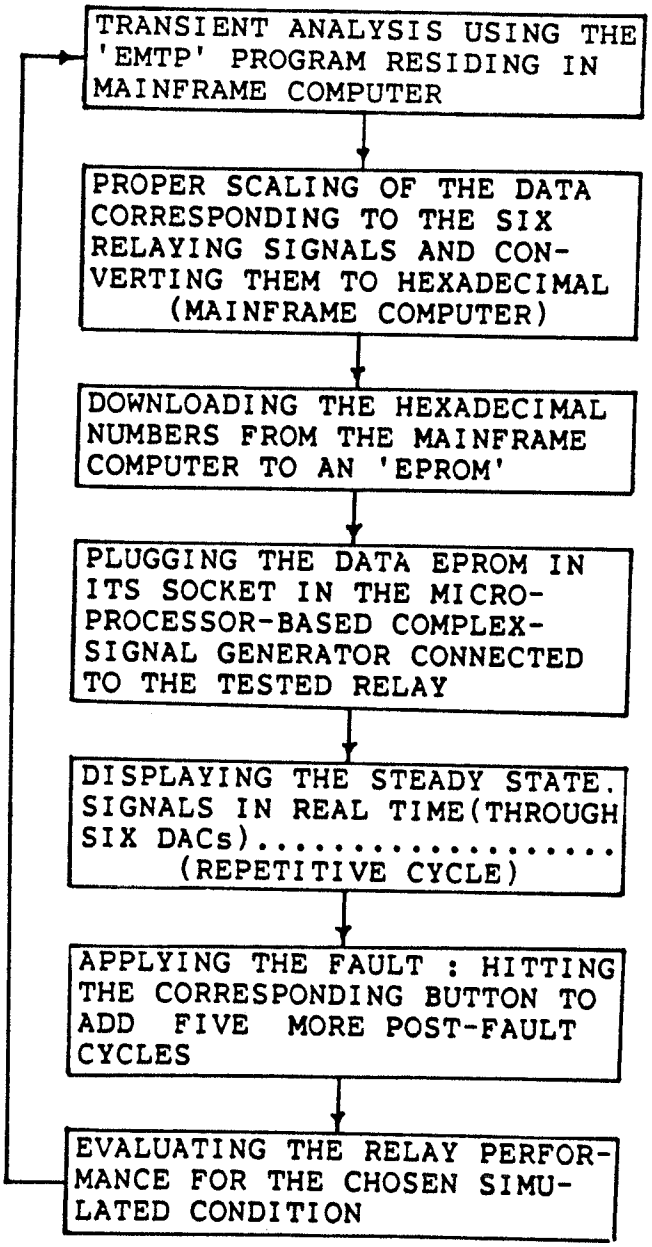


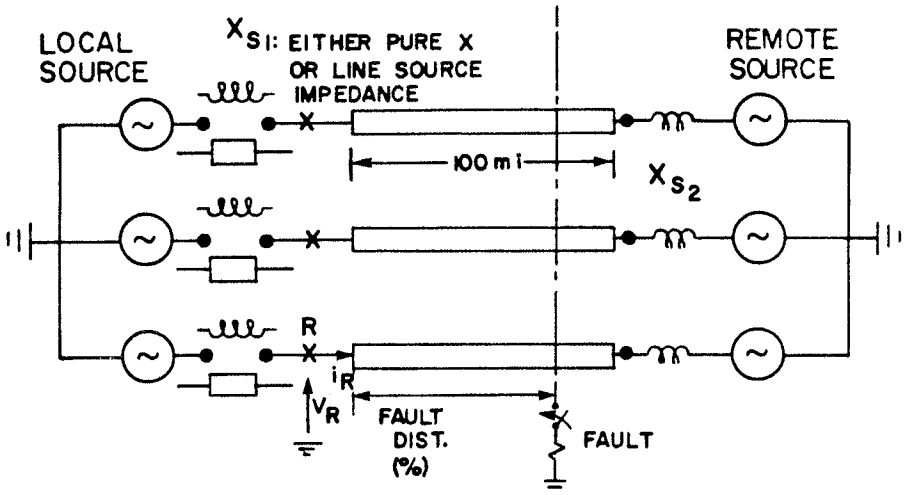

Fig.(7.2) Testing procedure

## 7.3 REAL TIME TESTING

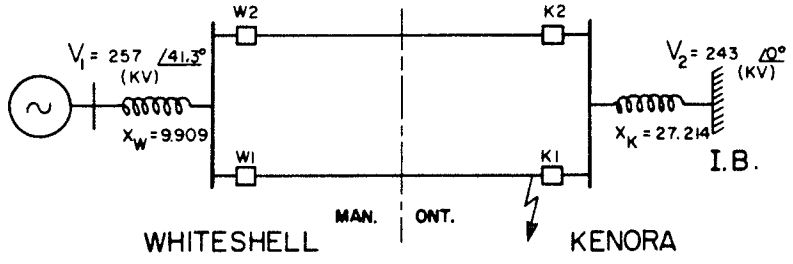
Utilizing the 'CWSG' described above, real time signals proportional to the primary voltages and currents at different relay locations in the two study systems of Chapter 4 (Fig.(7.3.a) and Fig.(7.3.b)) were fed to the prototype relay in order to evaluate its performance when being connected to the corresponding locations.

In order to evaluate the response of the prototype for the different expected disturbances the following measures were taken during the testing operation:

1. The master processor was resident in the circuit emulator used before for system debugging. Hence the different discriminant components after detecting any disturbance could be checked. This measure helped in choosing the proper tripping level, and in getting a clear idea about the consistency of the system.
2. One-shot operation was used for the testing. This meant that the relay was blocked (infinite loop) after detecting any fault. This was done for two reasons:
   a) As mentioned above it was required to check the different discriminant components after each specific fault.
   b) The testing procedure was required to cope with the present state of the testing system which adds only five post fault cycles after the steady-state repetitive cycle. After these five cycles the generated signals are meaningless.




a)




b)

Fig. (7.3) Study systems a) 500 KV single circuit system
b) 230 KV double circuit system

3. The discriminant threshold for each study system was chosen through several (more than 20) trials for each kind of fault. This nonexplicit threshold setting procedure is mainly due to the low resolution of the ADCs used, and the relatively low sampling rate. The adjustment for each system is for the purpose of matching the actual line characteristics. Nevertheless, the following thresholds were found to be consistent with both of the two studied systems:

   a) $15_H$: for the fault detection and direction discrimination threshold.

   b) $0A_H$: for the zero-nonzero threshold for phase selection and fault classification.

### 7.3.1 RESPONSE TO SOLID FAULTS

Considering the 500 KV study system (Fig.(7.3.a)), a series of solid faults were simulated at various points on the protected line and the prototype relay was fed with signals derived from the relay location 'R'. Fig.(7.4) shows the resulting performance obtained. It can be seen that there is a difference in the tripping time according to the fault type, the fault position and the fault inception angle. The slowest condition was encountered following a single phase-to-earth fault at zero voltage point-on-wave. Thus independence of the angle of fault inception, which is a feature of the developed algorithm, as previously shown in Chapters 2, 3, and 4, is not completely realized in the implemented prototype.

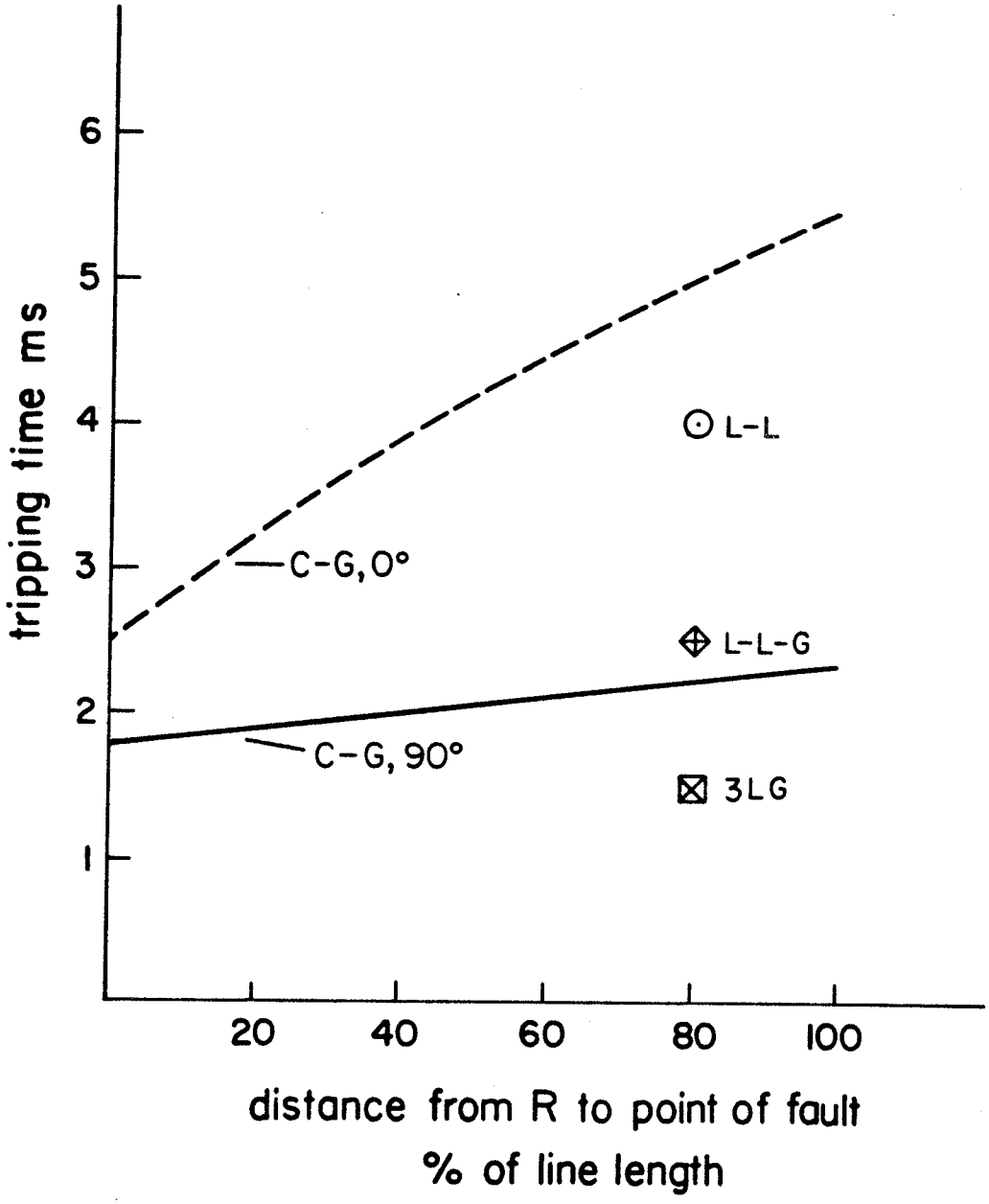



Fig. (7.4) Relationship between tripping time and fault distance for the relay at 'R' in the 500 KV system

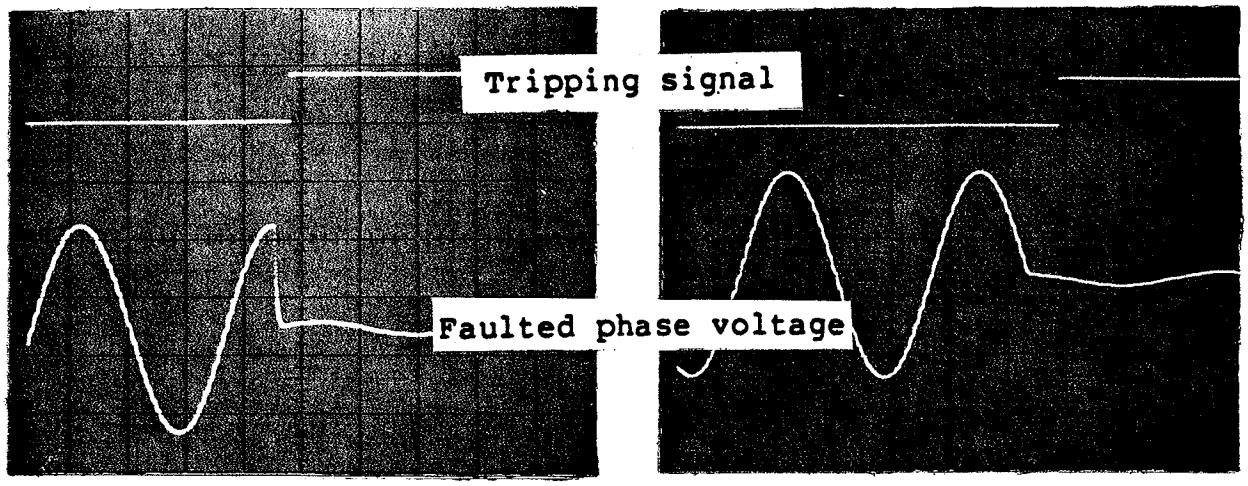
This is simply due to the low accuracy of the backward-difference expression used for the numerical differentiation in the prototype, and the relatively long time step (0.5 ms). This causes the changes in the signals and their differentiations (for this case of a zero inception fault) to take the same slow rising time from zero to the significant values which cause the discriminant to exceed the tripping threshold.

However, because the majority of faults occur near the peak of the prefault voltage, it is the relative clearing times in the vicinity of the 90 degrees point on wave which are of practical importance. The overall maximum tripping time for a fault at the far end in this case is [2.3 - 0.5] (relay) + [2.0] (communication channel)= 3.8 ms.
For the independent mode of operation (Chapter 4) a tripping time of 1.5 ms at the end close to the fault could be achieved.

Figs(7.5-7.7) show oscilloscope recordings taken during testing of the prototype relay when fed with test waveforms at location 'R' of the 500 KV system. The tripping times shown do not include the communication channel time.

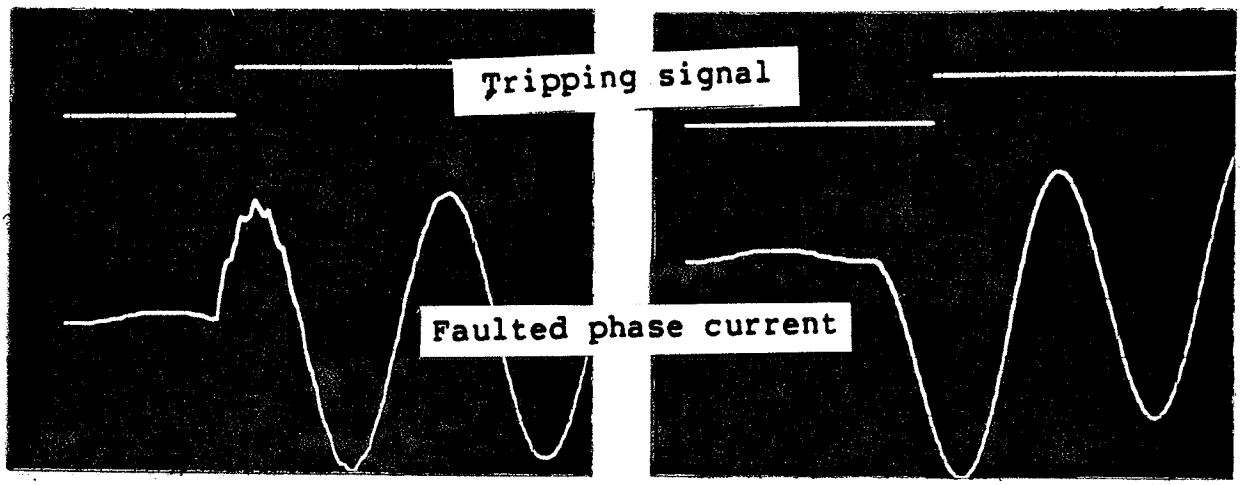
### 7.3.2 RESPONSES TO OTHER PRACTICAL CASES

The double circuit 230 KV system is considered (Fig.(7.3.b)). Some of the conducted case studies (C.S.'s) are summarized in Table(7.1). In all the cases the frequency variation of all the line and earth parameters was simulated.



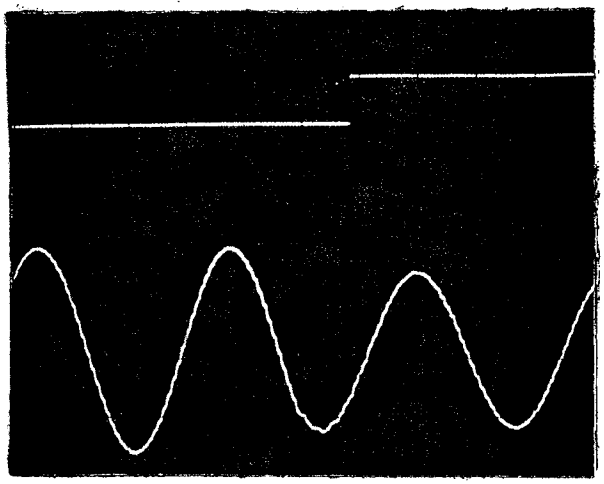

(a) (b)

Fig. (7.5) Relay response at R for a close-in (0%) L-G fault at different fault inception angles
a) 90° b) 0°

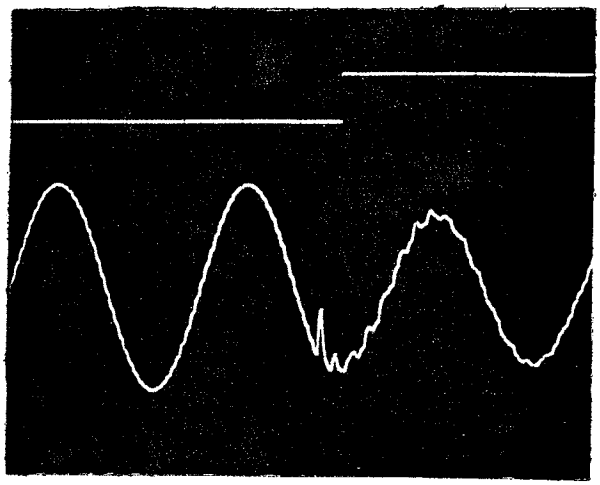



(a) (b)

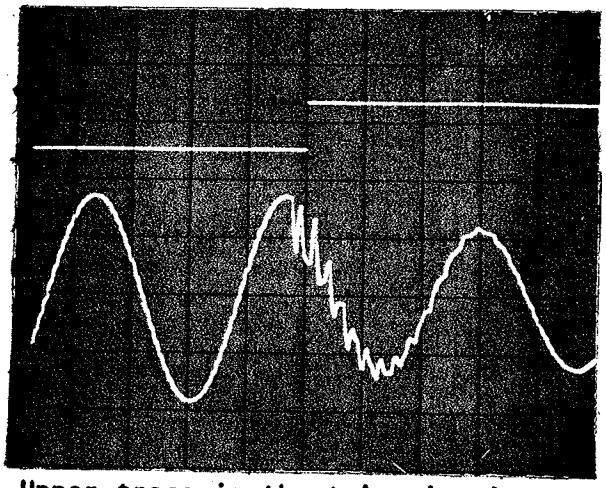
Fig. (7.6) Relay response at R for a far (80%) L-G fault at different fault inception angles
a) 90° b) 0°



(a) Line-to-line fault



(b) Line-to-line-to-ground fault



(c) 3 Lines-to-ground fault

Upper trace is the trip signal
Lower trace is a faulted phase voltage

Fig. (7.7) Relay response at R for different phase faults (80%)

Table (7.1)
Testing Case Studies Applied on the 230 KV System

| CASE # | FAULTED PHASE | RELAY LOCATION | FAULT RESISTANCE | TRIP. TIME | LINE ARRANGEMENT | CORRES. FIGURE |
|---|---|---|---|---|---|---|
| 1 | C-G | K1 | 0 | 1.5 | COM.TR. | (7.8) |
| 2 | C-G | K1 | 30 | 1.5 | COM.TR. | (7.9) |
| 3 | C-G | W1 | 0 | 1.5 | COM.TR. | (7.10) |
| 4 | C-G | W1 | 30 | 1.5 | COM.TR. | (7.11) |
| 5 | C-G | W1 | 80 | 2.0 | COM.TR. | (7.12) |
| 6 | C-G | W1 | 30 | 2.0 | N.TR. | (7.13) |
| 7 | A-G | W1 | 30 | 1.5 | COM.TR. | ----- |
| 8 | B-G | W1 | 30 | 1.5 | COM.TR. | ----- |
| 9 | C-G | K2 | 30 | --- | COM.TR. | (7.14) |

-COM.TR.: Complete transposition
-N.TR. : Nontransposed
-Resistance in ohms
-Time in ms,

Table (7.2)
Discriminant Components for Different Faulted Phases

| FAULTED PHASE | $D^{(1)}\|_b$ | $D^{(0)}$ | $D^{(1)}\|_a$ | $D^{(2)}\|_a$ |
|---|---|---|---|---|
| A | (04) | 55 | 16 | 12 |
| B | 11 | 6A | OD | (04) |
| C | 13 | E5 | (04) | 37 |

VALUES ARE IN HEXADECIMAL

For some cases (e.g. C.S.# 6) a complete nontransposition for the whole system is simulated. The fault considered in all these cases is line to ground at 'K1' with different fault resistances (0 to 80 ohms). For this same fault the prototype performance is investigated when being fed by signals proportional to the relaying signals at different terminals W1 (same as for W2 for this fault location), K1 (fault location) and K2 (which sees the fault as a backward one).

Since it is not an impedance measuring device, the relaying prototype is not subject to the limitations of conventional distance relays in respect of high-resistance line-to-ground faults. However, in the case of very-high-resistance faults the superimposed voltage at the fault point is injected through a relatively high resistance and the superimposed components at the relaying points can lie below the relay setting. Meanwhile, the maximum tolerable fault resistance varies considerably according to fault position and the point-on-wave at which the fault occurs. Nevertheless, the performance with respect to high resistance faults is generally much better than for conventional distance relays. Case study #5 in Table(7.1) and Fig.(7.12) shows the operating time of the relay at W1 with 80 ohm fault resistance.

Table(7.2) contains typical values for the discriminant components calculated by the relay for the different line-to-ground faulted phases. The agreement of these values with the corresponding ones in the Karrenbauer-based truth table is very clear. This led to correct phase selection in all of the conducted line-to-ground fault tests.

The oscilloscope records which correspond to the different case studies applied to the 230 KV system are shown in Figs(7.8-7.14).

### 7.3.3 RESPONSE TO BACKWARD FAULTS

In Fig.(7.15) the relay fault signals and the relay response for a backward (reverse) fault right at the relay location 'R' (-0%) is shown for the 500 KV system. The upper signal is not a tripping signal, but it is a signal corresponding to a 'backward fault detection' which was displayed from a different display PIA bit. Of course, unless directional discrimination is considered, a tripping signal will be issued.

Fig.(7.14) shows the response for the relay at K2 for a fault at K1. The location of the fault is considered by the relay at K2 as a backward one (-0%). Again, the upper signals are backward fault indications from a special bit. This condition is shown as C.S.# 9 in Table(7.1).

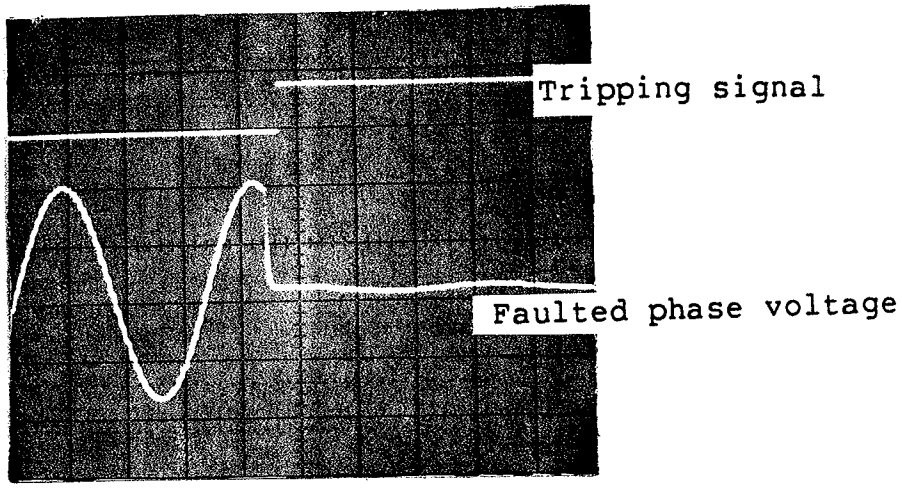



**Fig. (7.8) Relay response at K1 (0%), C.S.#1**
($R_f$ = 0 ohms)

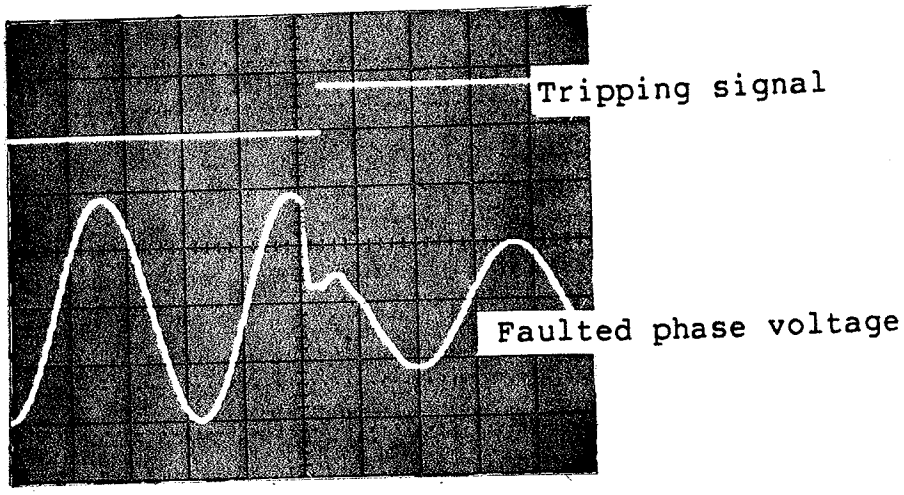



**Fig (7.9) Relay response at K1, C.S.#2**
($R_f$ = 30 ohms)

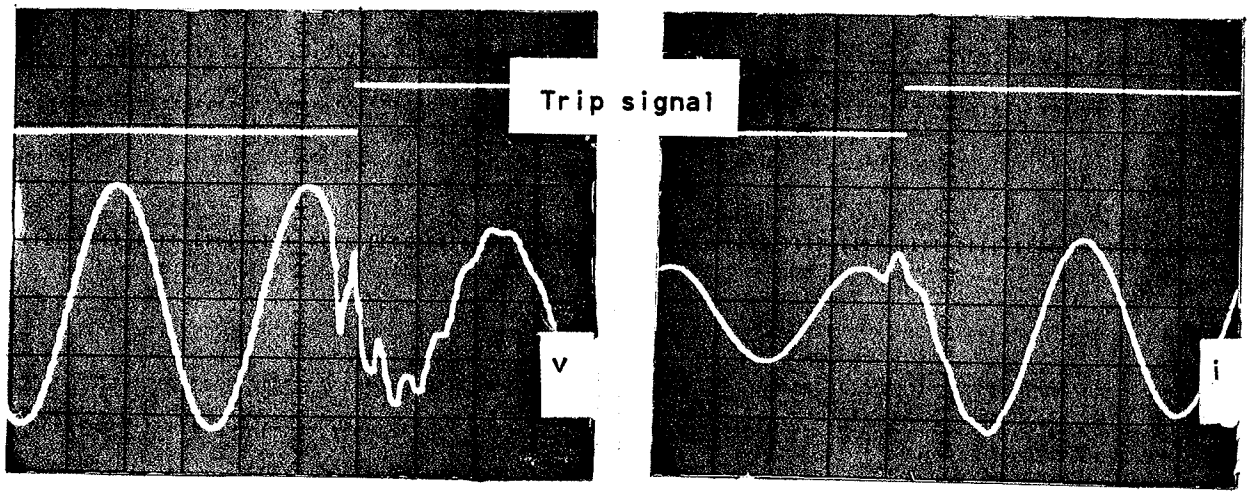



**Fig. (7.10) Relay response at W1, C.S.#3**

($R_f$ = 0 ohms)

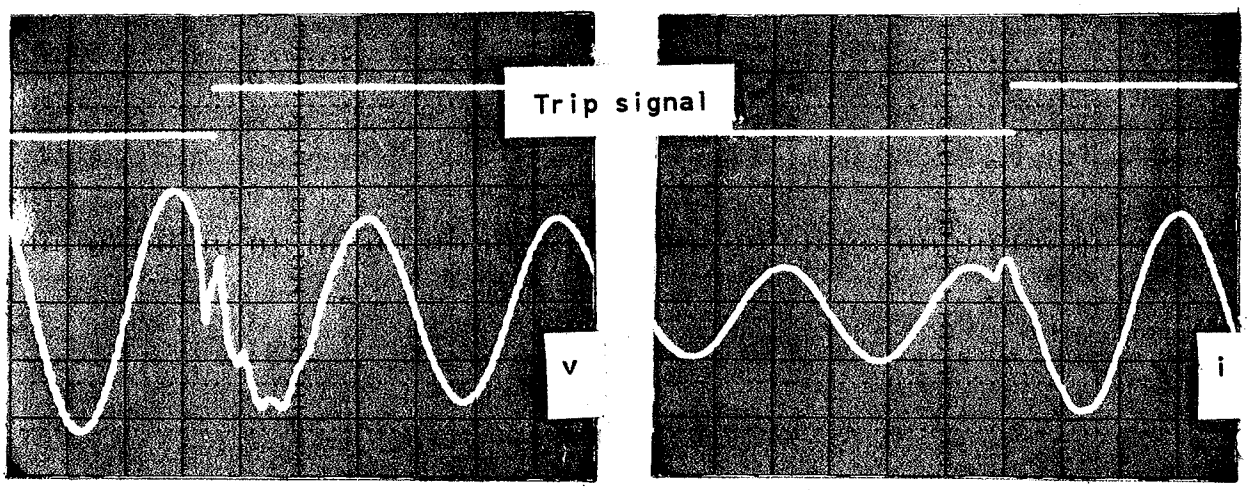



**Fig. (7.11) Relay response at W1, C.S.#4**

($R_f$ = 30 ohms)

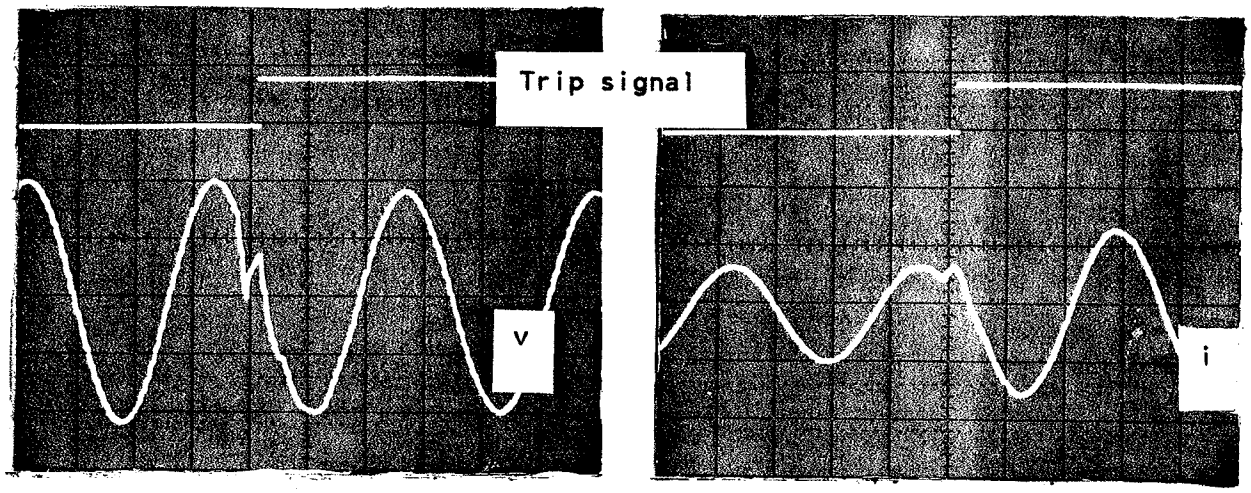



**Fig. (7.12) Relay response at W1, C.S.#5**

($R_f$ = 80 ohms)

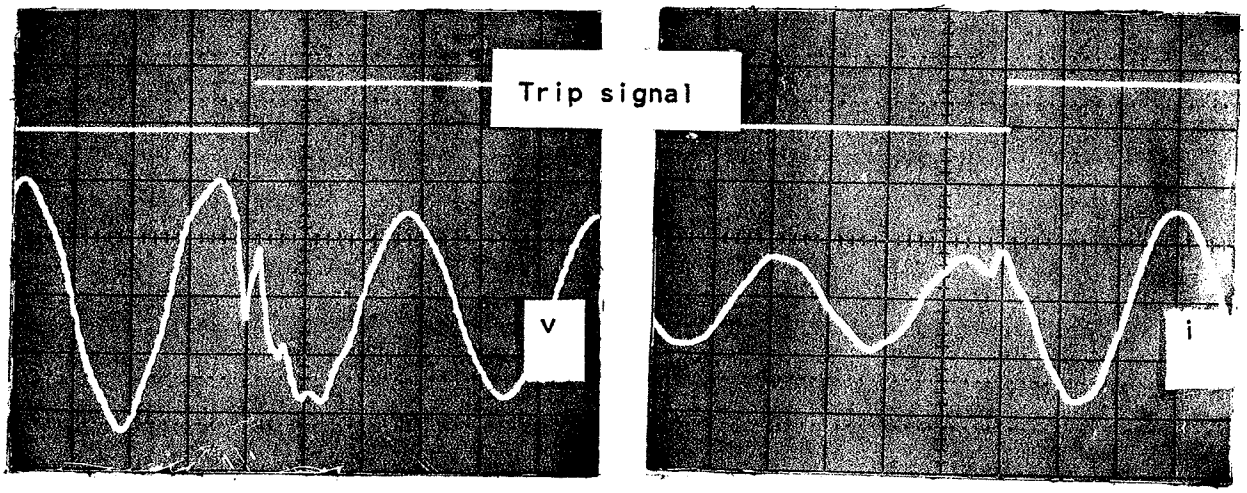
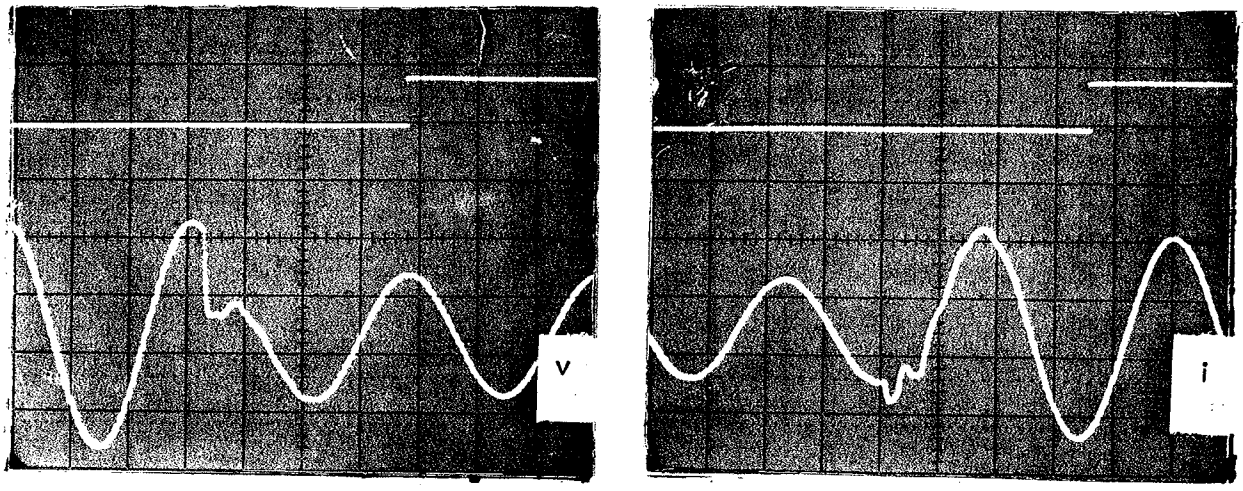


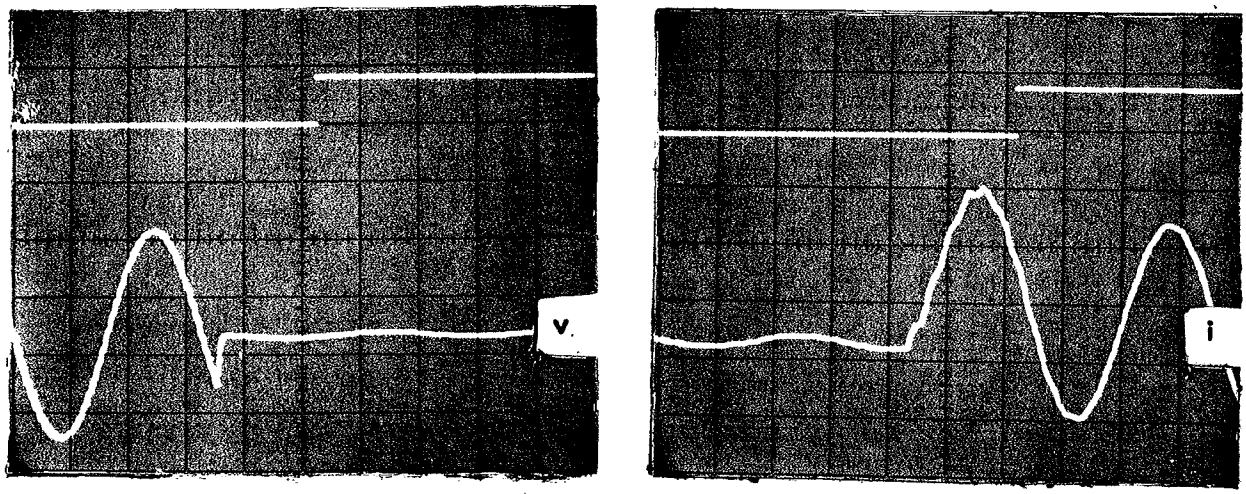

**Fig. (7.13) Relay response at W1, C.S.#6**

($R_f$ = 30 ohms, nontransposed)




Upper trace is the local blocking signal

Fig. (7.14) Relay response at K2 (-0%), C.S.#9
($R_f$ = 30 ohms)




Upper trace is the local blocking signal

Fig. (7.15) Relay response at R (500 KV system)
for a solid backward fault (-0%)

## Chapter VIII

## CONCLUSIONS AND RECOMMENDATIONS

A new travelling-wave protection principle for UHS digital transmission line relaying has been considered in this work. Incorporated in a directional comparison scheme, this relaying principle features not only ultra-high-speed operation, but also phase selection and fault classification capabilities. This relaying principle has been realized in the form of a multi-microprocessor-based experimental prototype. This prototype has been tested in real time under conditions close to reality and has shown great agreement with the theoretically developed and numerically (through computer simulation) tested relaying behaviour. The major advantages of the new principle as compared to previous travelling-wave-based relays can be briefly itemized as follows:

1. A faulted phase selection capability is provided for line-to-ground (and line-to-line) faults, which should then lead to selective pole-tripping and hence enhenced system stability and availability. Fault classification is another inherent special feature of this relay which has not been realized before in any other travelling-wave-based relaying scheme.
2. The relaying discriminant functions used for fault detection and direction discrimination are quite decisive and insensitive to parameter variation, different system configurations, and the fault initiation angle. There is some fault initiation dependence due to hardware limitations.

3. The multi-microprocessor realization approach is another special feature which leads to high reliability and security, enhanced system performance and ease of design and development. With this same realization approach some other relaying functions could be integrated with the available one in one package to provide superior performance by mutual support whereby the inherent strengths of each measurement technique are used to improve the characteristics of others.

However, like any other travelling-wave-based relaying technique, this relay cannot stand alone, but must complement existing techniques (e.g. distance and over current relays) where such techniques are in difficulty.

Further work could be recommended as an extension of this thesis in its two main phases, i.e. the relaying principle and the realization approach.

In the relaying principle phase, extra work could be done in studying the behaviour of the discriminant functions (not only the high-low behaviour presented here) under different conditions. Fault location could be then related to this behaviour and one-terminal relaying based on these same functions could be realized without any communication requirement.

In the realization phase, it is recommended to use more powerful microprocessors (higher speed and longer word length) along with faster ADCs with higher resolutions. This should lead to a higher sampling

rate, more accurate calculation which would provide more reliability and less dependence on fault initiation angle. Self diagnostic programs can be added to ensure more security. Of course, realizing the other algorithms based on the Clark and the Wedepohl transforms, with their complete fault classification and even faulted phase selection for line-to-line faults (besides line-to-ground), is quite feasible with a multi-microprocessor system based on these more powerful microcomputers.

Moreover, further study can be conducted to obtain a fault-tolerant relay, which could operate even in the case of major hardware malfunction (perhaps with downgraded performance). The multiprocessor structure is a good starting point to carry out this concept due to the inherent redundancy feature of this kind of system.

## Appendix A

## DISCRIMINANT COMPONENTS FOR DIFFERENT TYPES OF FAULTS

In this appendix(*) the different discriminant components in the Karrenbauer domain are derived for different fault types and different faulted phase combinations. The basis of the transformation is assumed to be phase "a". The discriminants with respect to other phases could be deduced from the values calculated with respect to "a" by proper rotation of the faulted phase(s). The same procedure could be applied with Clark and Wedepohl transforms. Their corresponding discriminants are shown in tables A.1 and A.2 respectively at the end of this appendix.

Firstly considering equation's 3.3 and 3.7 we can write the following

$$\begin{bmatrix} v^{(0)} \\ v^{(1)} \\ v^{(2)} \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad (A.1)$$

Where $v^{(0)}$, $v^{(1)}$ and $v^{(2)}$ are the components of the superimposed quantities $v_a$, $v_b$, and $v_c$ in the Karrenbauer domain. Similar equations can be written for the deviations in currents to relate $i^{(0)}$, $i^{(1)}$ and $i^{(2)}$ to $i_a$, $i_b$ and $i_c$.

---

* In this appendix the changes in voltages and currents are introduced without the symbol delta " $\Delta$ " to simplify the notation.

## A.1 LINE TO GROUND FAULT

### A.1.1 Phase "a" to ground

The voltage and current changes produced by the fault at the fault point are obtained by connecting a voltage source

$$v_a = - V_{rms} \sqrt{(2/3)} \sin (\omega t + \phi) \qquad (A.2)$$

and two current sources

$$i_b(t) = i_c(t) = 0.0 \qquad (A.3)$$

to the fault location "F", assuming that the prefault voltage in phase "a" was

$$v'_a = V_{rms} \sqrt{(2/3)} \sin (\omega t + \phi)$$

Now from equations A.1 to A.3 we can write

$$v^{(0)} + v^{(1)} + v^{(2)} = v_a \qquad (A.4.a)$$

$$i^{(0)} = i^{(1)} = i^{(2)} \qquad (A.4.b)$$

$$\text{i.e. } v^{(0)}/Z_0 = v^{(1)}/Z_1 = v^{(2)}/Z_1$$

where $Z_0$ and $Z_1$ are the zero and positive sequence surge impedances, respectively.

$$\text{Hence } v^{(1)} = v^{(2)} = v^{(0)} Z_1/Z_0 \qquad (A.5)$$

Combining equations A.5 and A.4 we get

$$v^{(0)} = Z_0/(Z_0 + 2Z_1) \quad v_a(t) \qquad (A.6)$$

$$i^{(0)} = v^{(0)}/Z_0 = 1./(Z_0 + 2Z_1) \quad v_a(t)$$

$$v^{(1)} = v^{(2)} = Z_1/(Z_0 + 2Z_1) \quad v_a(t)$$

$$i^{(1)} = i^{(2)} = 1./(Z_0 + 2Z_1) \quad v_a(t)$$

Now substituting in equation 3.1 we get the discriminants at the relaying point:

$$D^{(0)} = 8/3 \{Z_0/(Z_0 + 2Z_1)\}^2$$

$$D^{(1)} = D^{(2)} = 2/3 \{2Z_1/(Z_0 + 2Z_1)\}^2 \qquad (A.7)$$

All the D's are normalized with respect to $(V_{rms})^2$.

### A.1.2 Phase "b" to ground

Going through steps similar to those for the previous fault

$$v_b = -V_{rms}\sqrt{(2/3)}\sin(\omega t+\phi-120)\ ,$$

$$i_a = i_c = 0.0$$

$$v^{(0)} + v^{(2)} - 2v^{(1)} = v_b(t)\ ,$$

$$i^{(0)} = -i^{(1)} = i_b/3.\ ,$$

$$i^{(2)} = 0.0 \text{ ----} \quad v^{(2)} = 0.0 \text{ -----} \quad D^{(2)} = 0.0 \qquad \text{(A.8)}$$

$$v^{(0)} = Z_0/(Z_0 + 2Z_1)\ v_b$$

$$v^{(1)} = -Z_1/(Z_0 + 2Z_1)\ v_b$$

$$\text{------}D^{(0)} = 8/3\ \{Z_0/(Z_0 + 2Z_1)]^2 \qquad \text{(A.9)}$$

$$\text{------}D^{(1)} = 8/3\ \{Z_1/(Z_0 + 2Z_1)\}^2 \qquad \text{(A.10)}$$

### A.1.3 Phase "c" to ground

Going through similar steps

$$v_c = -V_{rms}\sqrt{(2/3)}\sin(\omega t+\phi+120)\ ,$$

$$i_a = i_b = 0.0$$

$$v^{(0)} + v^{(1)} - 2v^{(2)} = v_c(t)\ ,$$

$$i^{(0)} = -i^{(2)} = ic/3.\ ,$$

$$i^{(1)} = 0.0 \text{ ----} \quad v^{(1)} = 0.0 \text{ -----} \quad D^{(1)} = 0.0 \qquad \text{(A.11)}$$

$$v^{(0)} = Z_0/(Z_0 + 2Z_1)\ v_c$$

$$v^{(2)} = -Z_1/(Z_0 + 2Z_1)\ v_c$$

$$\text{------}D^{(0)} = 8/3\ \{Z_0/(Z_0 + 2Z_1)]^2 \qquad \text{(A.12)}$$

$$\text{------}D^{(2)} = 8/3\ \{Z_1/(Z_0 + 2Z_1)\}^2 \qquad \text{(A.13)}$$

## A.2 LINE-TO-LINE FAULT

### A.2.1 "a-b" short circuit

This type of fault could be simulated through the following set of relationships:

$$v_{ab} = -V_{rms}\sqrt{2}\ \sin(\omega t + \phi + 30)$$

$$v_a = -v_b$$

$$ic = 0.0$$

$$i_a = -i_b$$

This leads to the following ,

$$i^{(0)} = v^{(0)} = 0.0$$

$$v^{(1)} = 2v^{(0)} = 1/3\ v_{ab}$$

Hence

$$D^{(0)} = 0.0$$

$$D^{(1)} = 8/9 \qquad \text{(A.14)}$$

$$D^{(2)} = 2/9 \qquad \text{(A.15)}$$

all normalized with respect to $(V_{rms})^2$.

### A.2.2 "b-c" short circuit

The corresponding signals at the fault point are

$$v_{bc} = -V_{rms}\sqrt{2}\ \sin(\omega t + \phi_2)$$

$$i_a = 0.0$$

$$i_b = -i_c$$

The corresponding modal components are

$$i^{(0)} = 0.0$$

$$i^{(1)} = -i^{(2)} = 1/3\ i_c$$

Hence

$$v^{(0)} = 0.0$$

$v^{(1)} = -1/6\ v_{bc}$

$v^{(2)} = 1/6\ v_{bc}$,

which leads to the following normalized discriminants at the relaying point,

$$D^{(0)} = 0.0 \qquad \text{(A.16)}$$

$$D^{(1)} = 2/9 \qquad \text{(A.17)}$$

$$D^{(2)} = 2/9 \qquad \text{(A.18)}$$

### A.2.3 "c-a" short circuit

In this case the corresponding signal deviations at the point of fault are,

$v_{ca} = - V_{rms}\sqrt{2}\ \sin(\omega t + \phi_3)$

$i_b = 0.0$

$ic = -ia$

These lead to

$v^{(0)} = 0.0$

$v^{(1)} = -1/3\ v_{ca}$

$v^{(2)} = 1/3\ v_{ca}$

Hence the corresponding normalized discriminants at the relaying point are:

$$D^{(0)} = 0.0 \qquad \text{(A.19)}$$

$$D^{(1)} = 2/9 \qquad \text{(A.20)}$$

$$D^{(2)} = 8/9 \qquad \text{(A.21)}$$

## A.3 LINE-TO-LINE-TO-GROUND FAULT

Throughout this section the following relationship is used when needed.

$$A_1\sin(\omega t+\phi_1) + A_2\sin(\omega t+\phi_2) = A\sin(\omega t+\phi) \qquad (A.22)$$

where

$$A^2 = \{A_1^2 + A_2^2 + 2A_1A_2\cos(\phi_2-\phi_1)\}$$

and

$$\tan\phi = (A_1\sin\phi_1 + A_2\sin\phi_2)/(A_1\cos\phi_1 + A_2\cos\phi_2)$$

This relationship can be derived easily from the trigonometry of the corresponding complex domain vectors of the quantities $A_1\sin(\omega t+\phi_1)$, $A_2\sin(\omega t+\phi_2)$ and their vectorial summation.

### A.3.1 "a-b-g" short circuit

In this case the deviation in signals at the fault point are

$$i_c = 0.0\ ,$$

$$v_a = -V_{rms}\sqrt{(2/3)}\sin(\omega t) \quad \text{and}$$

$$v_b = -V_{rms}\sqrt{(2/3)}\sin(\omega t-120)$$

From equation A.1 and the relationship of A.22 we can write

$$v^{(1)} = 1/3(v_a-v_b) = -V_{rms}\sqrt{2/3}\sin(\omega t+30)$$

$$v^{(0)} + v^{(2)} = 1/3(2v_a + v_b) = -V_{rms}\sqrt{2/3}\sin(\omega t-30)$$

By considering the current version of equation A.1 we can write

$$i^{(0)} + i^{(1)} - 2i^{(2)} = 0.0$$

which leads to $v^{(2)} = 1/2(Z_1/Z_0\ v^{(0)} + v^{(1)})$

By a straight forward, somewhat tedious, manipulation of the given equations we can write

$$D^{(0)} = 8/3\{Z_0/(2Z_0 + Z_1)\}^2 \qquad (A.23)$$

$$D^{(1)} = 8/9 \qquad (A.24)$$

$$D^{(2)} = 8/9\ (Z_1^2 + Z_0^2 + Z_1 Z_0)/(2 Z_0 + Z_1)^2 \qquad (A.25)$$

normalized w.r.t. $(V_{rms})^2$.

### A.3.2 "b-c-g" short circuit

Similarly we can write

$v_b = -V_{rms}\ \sqrt{(2/3)}\ \sin(\omega t)$,

$v_c = -V_{rms}\ \sqrt{(2/3)}\ \sin(\omega t-120)$ and

$i_a = 0.0$

Hence through equation A.1 with these equations we can write the following

$$v^{(2)}-v^{(1)} = 1/3\ (v_b-v_c) = -V_{rms}\sqrt{2/3}\ \sin(\omega t+30\ ),$$

$$v^{(0)}-v^{(1)} = 1/3\ (2v_b + v_c) = -V_{rms}\sqrt{2/3}\ \sin(\omega t-30),$$

and with the aid of $i^{(1)} + i^{(2)} + i^{(0)} = 0.0$ we can write

$$v^{(2)} = -Z_1(v^{(1)}/Z_1 + v^{(0)}/Z_0)\ .$$

Combining these equations we get the discriminant components at the relaying point as

$$D^{(0)} = 8/3\ \{Z_0/(2Z_0 + Z_1)\}^2 \qquad (A.26)$$

$$D^{(1)} = 8/9\ (Z_0^2 + Z_1^2 + Z_1 Z_0)/(2 Z_0 + Z_1)^2 \qquad (A.27)$$

$$D^{(2)} = D^{(1)} \qquad (A.28)$$

normalized w.r.t. $(V_{rms})^2$.

### A.3.3 "c-a-g" short circuit

Similarly we can write

$v_a = -V_{rms}\ \sqrt{(2/3)}\ \sin(\omega t)$

$v_c = -V_{rms}\ \sqrt{(2/3)}\ \sin(\omega t+120\ )$

$i_b = 0.0$

Then,

$$v^{(0)} + v^{(1)} = 1/3(2v_a + v_c) = -1/3\ V_{rms}\sqrt{2}\ \sin(\omega t+30.)$$

$$v^{(2)} = 1/3(v_a - v_c) = -1/3\ V_{rms}\sqrt{2}\ \sin(\omega t-30.)$$

$$i^{(0)} + i^{(2)} - 2i^{(1)} = 0.0\ .$$

The last equation leads to

$$v^{(1)} = Z_1/2\ (v^{(0)}/Z_0 + v^{(2)}/Z_1)$$

Finally the discriminants at the relaying point will be

$$D^{(0)} = 8/3\ \{Z_0/(2Z_0 + Z_1)\}^2 \qquad (A.29)$$

$$D^{(1)} = 8/3\ (Z_1^{\,2} + Z_0^{\,2} + Z_0\ Z_1)/(2\ Z_0 + Z_1) \qquad (A.30)$$

$$D^{(2)} = 8/9 \qquad (A.31)$$

normalized w.r.t. $(V_{rms})^2$.

## A.4 3-LINES-TO-GROUND SHORT CIRCUIT

For this most severe type of fault the superimposed quantities due to a fault at the point of fault are

$$v_a = -V_{rms}\sqrt{2/3}\ \sin(\omega t)\ ,$$

$$v_b = -V_{rms}\sqrt{2/3}\ \sin(\omega t-120.) \quad \text{and}$$

$$v_c = -V_{rms}\sqrt{2/3}\ \sin(\omega t+120.)$$

Combining these equations with equation A.1 we get

$$v^{(0)} = 1/3(v_a + v_b + v_c) = 0.0$$

$$v^{(1)} = 1/3(v_a - v_b) = -1/3\ V_{rms}\sqrt{2}\ \sin(\omega t+30.)$$

$$v^{(2)} = -1/3(v_a - v_c) = -1/3\ V_{rms}\sqrt{2}\ \sin(\omega t-30.)$$

These components lead to the corresponding discriminants at the relaying point:

$$D^{(0)} = 0.0 \qquad (A.32)$$

$$D^{(1)} = 8/9 \qquad (A.33)$$

$$D^{(2)} = 8/9 \qquad \text{(A.34)}$$

all normalized w.r.t $(V_{rms})^2$

The same procedures were applied with Clark and Wedepohl transforms and the corresponding normalized discriminants are shown in tables A.1 and A.2 respectively.

TABLE A.1

Discriminant components in the Clark domain

| Discriminant Components | Line-to-Ground | | | Line-to-Line | | | Line-to-Line-to-Ground | | | 3 Phase Short Circuit |
|---|---|---|---|---|---|---|---|---|---|---|
| | a − G | b − G | c − G | a−b | b−c | c−d | a − b − G | b − c − G | c − a − G | |
| $D_0$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | 0 | 0 | 0 | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | 0 |
| $D_\alpha$ | $\frac{8}{3}\left(\frac{2Z_1}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 2 | 0 | 2 | $\frac{8}{3}\frac{Z_1^2+3Z_1Z_0+3Z_0^2}{(Z_1+2Z_0)^2}$ | $\frac{8}{3}\left(\frac{Z_1}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\frac{Z_1^2+3Z_1Z_0+3Z_0^2}{(Z_1+2Z_0)^2}$ | 8/3 |
| $D_\beta$ | 0 | $8\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | $8\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 2/3 | 8/3 | 6 | $\frac{8}{3}\frac{Z_1^2+Z_1Z_0+Z_0^2}{(Z_1+2Z_0)^2}$ | 8/3 | $\frac{8}{3}\frac{Z_1^2+Z_1Z_0+Z_0^2}{(Z_1+2Z_0)^2}$ | 8/3 |

TABLE A.2

Discriminant components in the Wedepohl domain

| Discriminant Components | Line-to-Ground | | | Line-to-Line | | | Line-to-Line-to-Ground | | | 3 Phase Short Circuit |
|---|---|---|---|---|---|---|---|---|---|---|
| | a-G | b-G | c-G | a-b | b-c | c-d | a-b-G | b-c-G | c-a-G | |
| $D^{(0)}$ | $\frac{8}{3}\left(\frac{Z_0}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_1+Z_0}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_1+Z_0}\right)^2$ | 0 | 0 | 0 | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_0}{2Z_0+Z_1}\right)^2$ | 0 |
| $D^{(1)}$ | $6\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 0 | $6\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | 2 | 1/2 | 2 | $2\,\frac{Z_1^2+Z_0^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | $2\,\frac{Z_1^2+Z_0^2+Z_0Z_1}{(2Z_0+Z_1)^2}$ | $\frac{16Z_0^2+12Z_0Z_1+3Z_1^2}{(2Z_0+Z_1)^2}$ x(3/2) | 2 |
| $D^{(2)}$ | $\frac{2}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | $\frac{8}{3}\left(\frac{Z_1}{Z_0+2Z_1}\right)^2$ | $\frac{2}{3}\left(\frac{Z_1}{2Z_1+Z_0}\right)^2$ | 2 | 1/2 | 0 | $\frac{2}{3}\,\frac{Z_1^2+3Z_0^2+3Z_0Z_1}{(2Z_0+Z_1)^2}$ | $\frac{2}{3}\,\frac{3Z_0^2+Z_1^2+3Z_0Z_1}{(2Z_0+Z_1)^2}$ | $\frac{2}{3}\left(\frac{Z_1}{2Z_0+Z_1}\right)^2$ | 2/3 |

# Appendix B

## WIRING DIAGRAMS OF THE DIFFERENT BOARDS

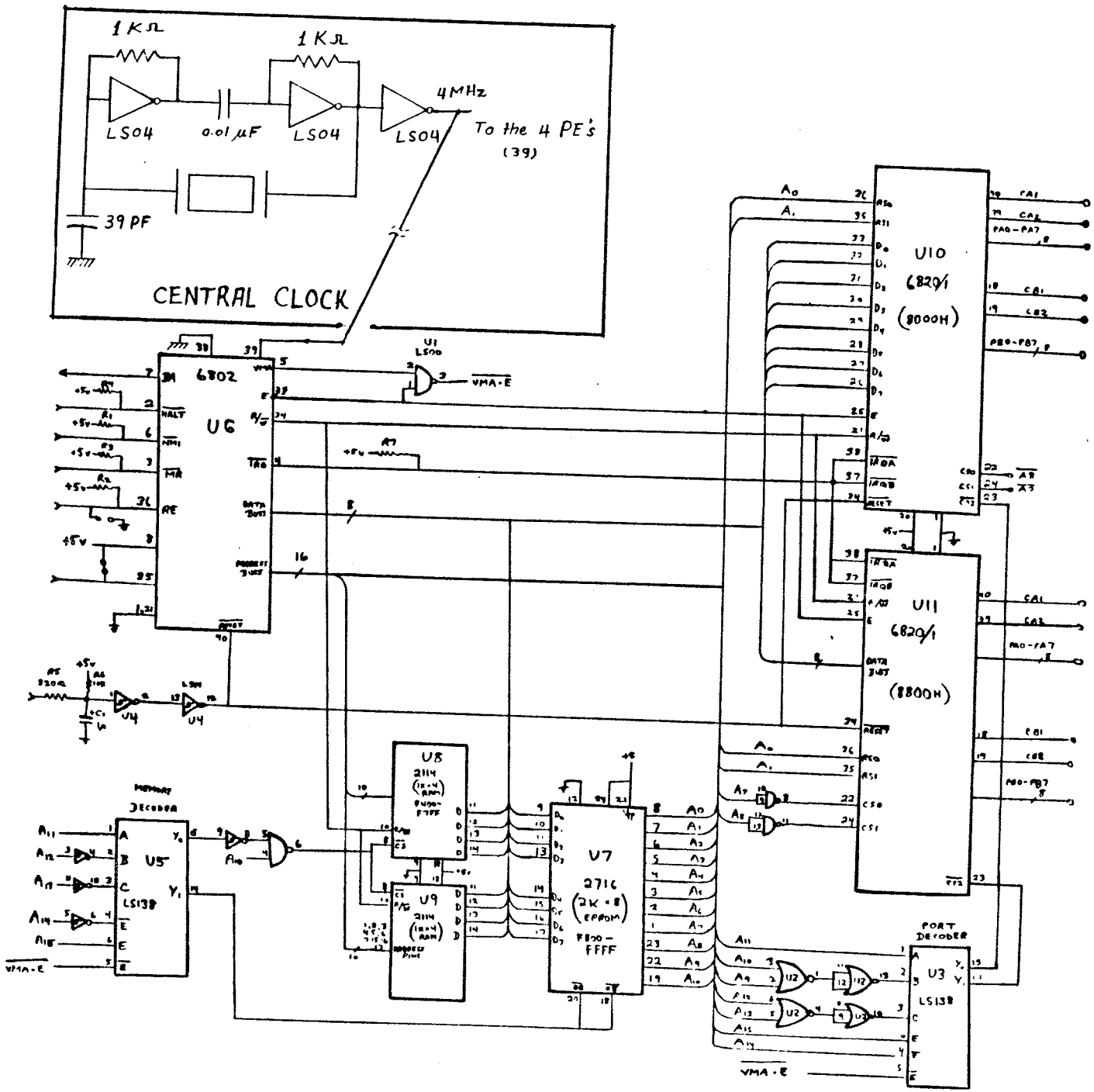



Fig.(B.1) Wiring diagram of the U.M. SBC used

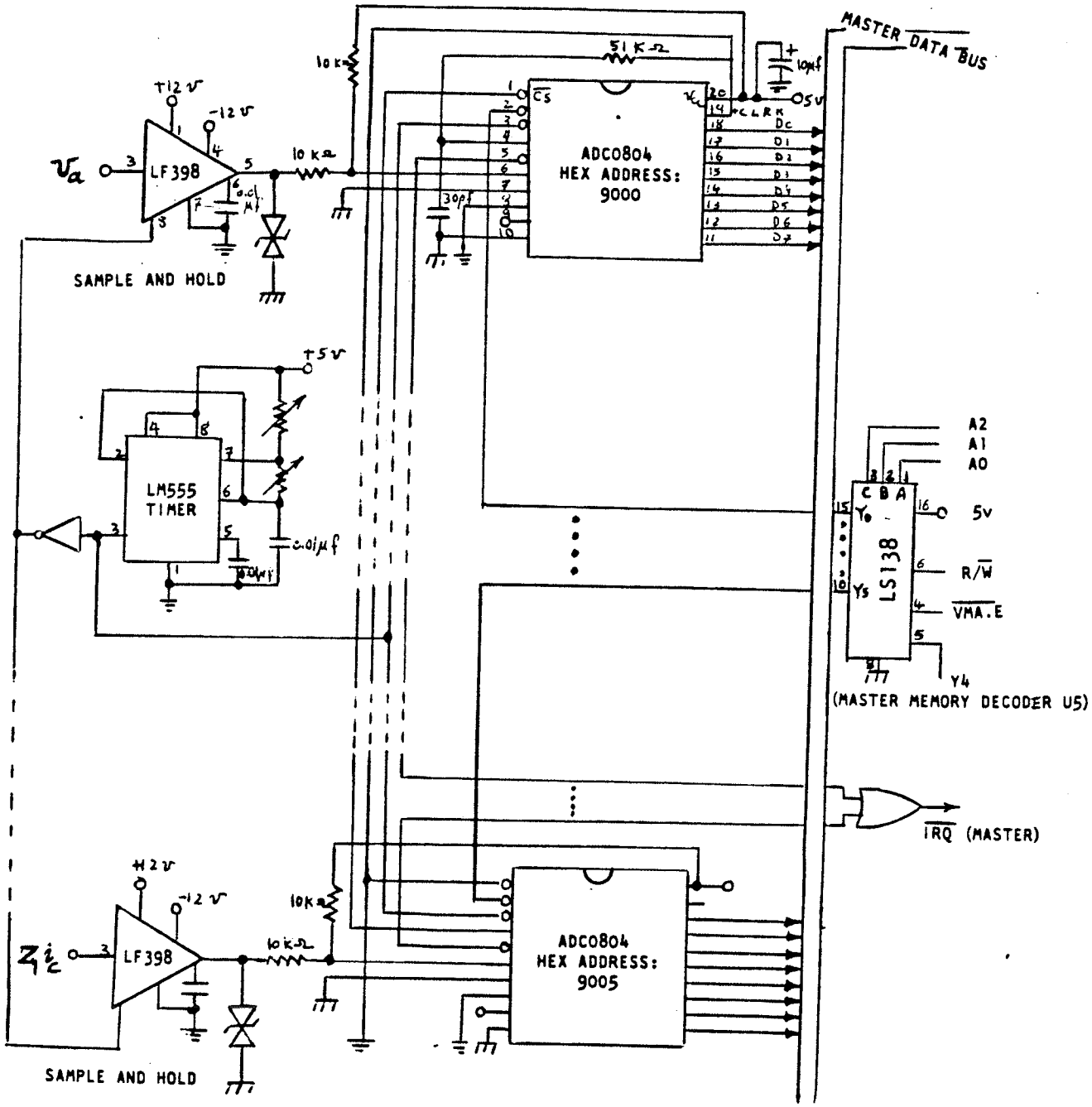



Fig. (B.2) Wiring diagram of the data acquisition board

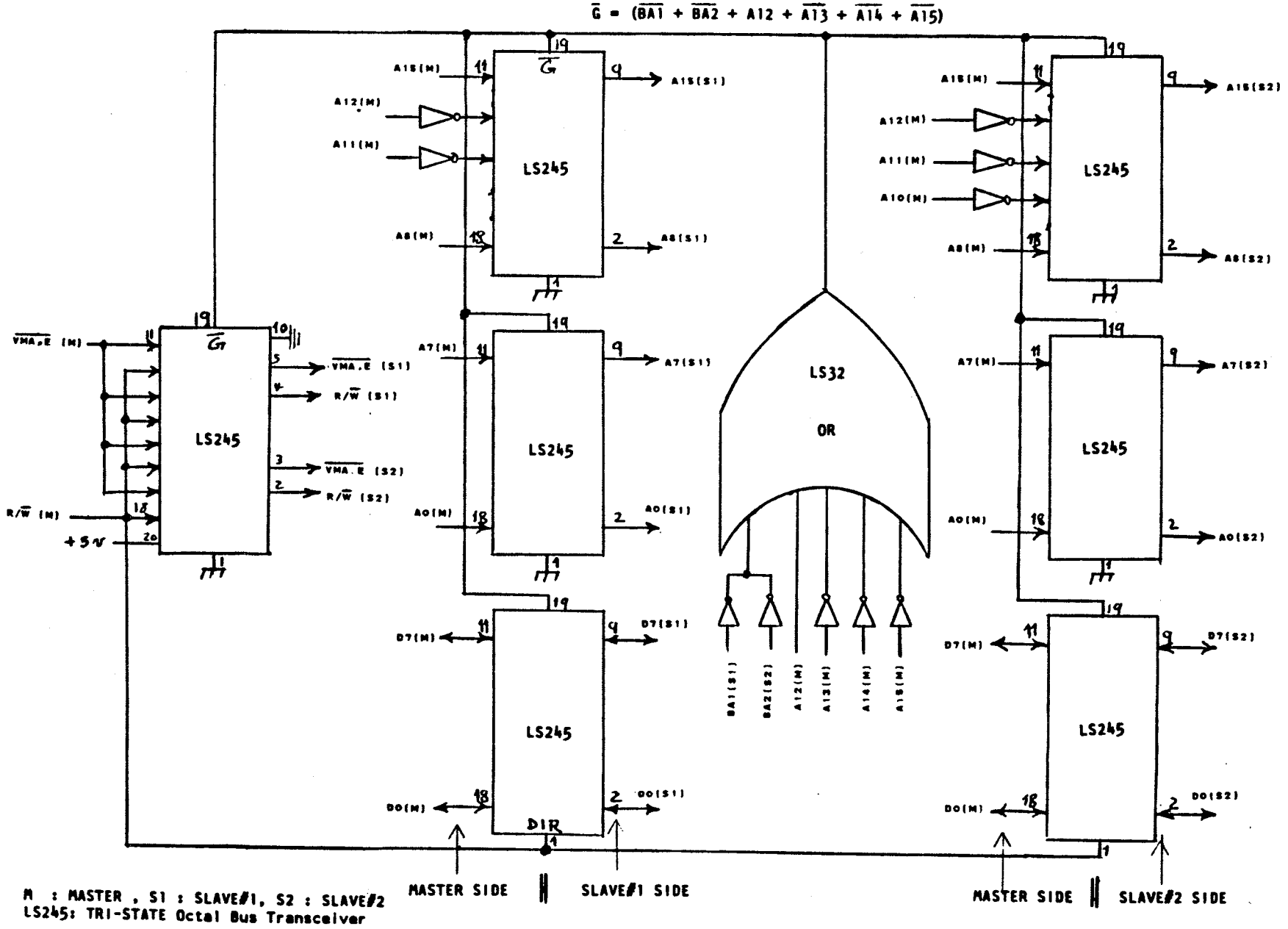



Fig. (B.3) Wiring diagram of the interfacing board (between master and S1 & S2)

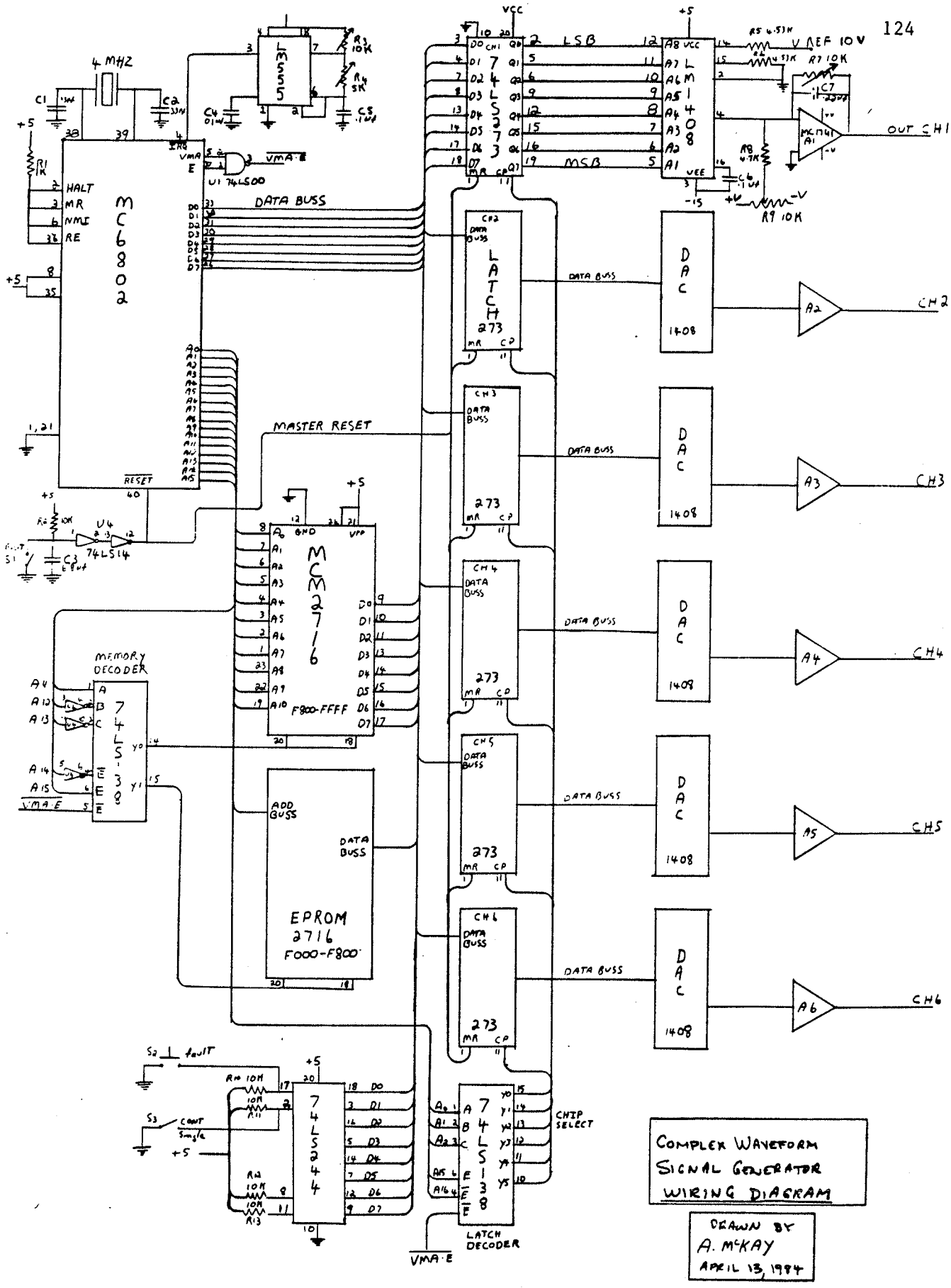



Figure B.4: Wiring diagram of the CWSG board

## Appendix C

## FORMULATION OF THE DISCRIMINANT COMPONENTS

In this appendix the formulae used for calculating the involved discriminant components are derived and the linear magnitude approximation technique used within the implemented prototype for calculating these components is explained.

### C.1 THE DISCRIMINANT COMPONENTS FORMULAE

Recalling equation (6.1), the implemented discriminant function can be defined as

$$D^{(k)}(n) = \sqrt{\{[d^{(k)}(n)]^2 + [K(d^{(k)}(n)-d^{(k)}(n-1)]^2\}} \qquad (C.1)$$

where $d^{(k)}(n)$ is the k-th component of the wave characteristic at the sample number 'n'. $K = 1/(T\ \omega)$ where T is the sampling period in seconds and $\omega$ is the power frequency in radians/second. This means that a first order difference equation is used for differentiation.

In the following the wave characteristic components ($d^{(k)}(n)$) for the different discriminant components used with our Karrenbauer-transform-based prototype are formulated in terms of the sampled and reference signals.

$\underline{d_F^{(1)}}$ with respect to phase "a"

This belongs to the 'master' "normal system condition" task and and 'S1' forward fault task.

In this case we can write

$$d_F^{(1)}(n) = \Delta v^{(1)}(n) - \Delta I^{(1)}(n) \qquad (C.2)$$

where

$$I = Z_l\, i \qquad (C.3)$$

Now by using the Karrenbauer-transform we can write

$$\Delta v^{(1)} = \Delta v_a - \Delta v_b$$

$$\Delta I^{(1)} = \Delta I_a - \Delta I_b \qquad (C.4)$$

(with the factor (1/3) omitted).

The signal changes mentioned above can be expressed as follows

$$\Delta v_a(n) = v_a(n) - v_a(n-N),$$
$$\Delta I_a(n) = I_a(n) - I_a(n-N),$$

(C.5)

$$\Delta v_b(n) = v_b(n) - v_b(n-N) \text{ and}$$
$$\Delta I_b(n) = I_b(n) - I_b(n-N)$$

where 'N' is the number of samples/cycle .

Hence through equations (C.2) to (C.5) we can write

$$d_F^{(1)}|_a(n) = [v_a(n)+v_b(n-N)+I_a(n-N)+I_b(n)] - [v_a(n-N)+v_b(n)+I_a(n)+I_b(n-N)] \qquad (C.6)$$

$\underline{d_F^{(2)}}$ with respect to phase "a"

This belongs to the 'forward fault' task for 'S2'. In this case the the corresponding wave characteristic is

$$d_F^{(2)}(n) = \Delta v^{(2)}(n) - \Delta I^{(2)}(n) \qquad (C.7)$$

where

$$\Delta v^{(2)}(n) = \Delta v_a(n) - \Delta v_c(n)$$

$$\Delta I^{(2)}(n) = \Delta I_a(n) - \Delta I_c(n) \qquad (C.8)$$

Hence

$$d_F^{(2)}|_a(n) = [v_a(n)+v_c(n-N)+I_a(n-N)+I_c(n)] - [v_a(n-N)+v_c(n)+I_a(n)+I_c(n-N)] \qquad (C.9)$$

$\underline{d_F^{(1)}}$ with respect to phase "b"

This belongs to the 'D' assigned to 'S3' all the time. The corresponding wave characteristic is formulated by replacing "a" with "b" in the previous equation (eq. C.9),

$$d_F^{(1)}|_b(n) = [v_b(n)+v_c(n-N)+I_b(n-N)+I_c(n)] - [v_b(n-N)+v_c(n)+I_b(n)+I_c(n-N)] \qquad (C.10)$$

$\underline{d_B^{(1)}}$ with respect to phase "a"

This belongs to 'S1' in the fault detection stage.

$$d_B^{(1)}|_a(n) = \Delta v^{(1)}(n) + \Delta I^{(1)}(n) \qquad (C.11)$$

$$d_B^{(1)}|_a(n) = [v_a(n)+v_b(n-N)+I_b(n-N)+I_a(n)] - [v_a(n-N)+v_b(n)+I_b(n)+I_a(n-N)] \qquad (C.12)$$

$\underline{d_B^{(2)}}$ with respect to phase "a"

This belongs to 'S2' in the fault detection stage. In the same way as above it can be written as

$$d_B^{(2)}|_a(n) = \Delta v^{(2)}(n) + \Delta I^{(2)}(n) \qquad (C.13)$$

$$d_B^{(2)}|_a(n) = [v_a(n)+v_c(n-N)+I_c(n-N)+I_a(n)] - [v_a(n-N)+v_c(n)+I_c(n)+I_a(n-N)] \qquad (C.14)$$

$\underline{d_F^{(0)}}$ with respect to any phase

This belongs to the 'forward fault' task for the master.

$$d_F^{(0)} = \Delta v^{(0)}(n) - \Delta I^{(0)}(n) \qquad (C.15)$$

where

$$\Delta v^{(0)}(n) = \Delta v_a + \Delta v_b + \Delta v_c = \{v_a(n) + v_b(n) + v_c(n)\} - \{v_a(n-N) + v_b(n-N) + v_c(n-N)\} \qquad (C.16)$$

Assuming the nearly balanced condition we can write

$$\Delta v^{(0)}(n) = v_a(n) + v_b(n) + v_c(n) \qquad (C.17)$$

Following the same procedure with $I^{(0)}(n)$ we can write

$$d_F^{(0)} = \{v_a + v_b + v_c\} - 3\{I_a(n) + I_b(n) + I_c(n)\} \qquad (C.18)$$

This presupposes a typical ratio of $Z_0/Z_1$ to be '3'.

## C.2 LINEAR MAGNITUDE APPROXIMATION

In reference [45], and based on a previous idea in [47], a piece-wise linear magnitude approximation of vector quantities expressed in rectangular coordinates is introduced and investigated for time-constrained systems of large dynamic range.

### C.2.1 Analysis [47]

The problem is to compute $R = \sqrt{I^2 + Q^2}$, where I and Q represent the quadrature signal pair. We begin by defining

$$x = \max(|I|, |Q|)$$
$$y = \min(|I|, |Q|) \qquad \text{(C.19)}$$

This transformation serves to rotate the complex point $z = I + j\,Q$ such that its argument lies between 0 and $\pi/4$. Thus,

$$R = \sqrt{x^2 + y^2} \qquad 0 < \theta < \pi/4 \qquad \text{(C.20)}$$

In this region, one approximates R as

$$R' = ax + by = R(a\cos\theta + b\sin\theta) \qquad \text{(C.21)}$$

and defines the relative error as

$$e(\theta) = (R-R')/R = 1 - a\cos\theta - b\sin\theta \qquad \text{(C.22)}$$

This method is called the 'one line method'.

To further improve the approximation, the $\pi/4$ arc is divided into two regions (the two line method). For the detailed analysis for this case refer to [47].

### C.2.2 Implementation

The one-line method chosen for implementation is

a = 1

b =1/4

These figures produce error no worse than 11.6% and a mean error of as low as 0.656% [45] besides being very simple to implement using integer arithmetic. The implementation steps could be summarized as follows:

1. The absolute values of the quadrature components are computed.
2. These magnitudes are compared and the larger value is placed in a register 'X' and the smaller value in a register 'Y'.
3. The contents of the Y register are shifted twice to the right, which approximates division by 4.
4. The resulting contents of the Y register are added to the contents of the X register to obtain the final result.

This same procedure is used within the software of the implemented prototype whenever any discriminant component is being calculated.

## Appendix D

## ASSEMBLY PROGRAMS

In this appendix, lists of the first pages of the 'master', slave #1, slave #2, and slave #3 programs are included. Complete program listings (32 pages) are on file in the Department of Electrical Engineering, University of Manitoba (through Prof. G.W. Swift).

132



MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.3
MODIFIED IAMC VER: 1.0

```
00001                    NAM   MASTER
00002                   ****************************************
00003                   * THIS  IS THE ASSEMBLED 'MASTER' PROG-*
00004                   * RAM IN THE MULTI-MICROPROCESSOR-BASED*
00005                   * TRAVELLING WAVE RELAY                *
00006                   * (PH.D THESIS , M.M.MANSOUR, 1984)    *
00007                   ****************************************
00008                   *
00009   0021    NMAX    EQU   33          NUM. OF SAM.'S/CYC.
00010   EE01    D1S1    EQU   $EE01       D1S1 AS SEEN BY MASTER
00011   EA02    D2S2    EQU   $EA02       D2S2 SEEN BY M.
00012                   *
00013                   * MASTER STORAGE DEFINITION >>>>>>>>>>>>>>>>>
00014                   *
00015                   * MESSAGE COMMUNICATION BUFFERS(PIA'S)
00016                   *
00017                   *--------------------
00018   8000    RBUF    EQU   $8000       READ BUFFER LOCATION
00019   8001    RSTAT   EQU   $8001       READ STATUS LOCATION
00020   8002    WBUF    EQU   $8002       WRITE BUFFER LOCATION
00021   8003    WSTAT   EQU   $8003       WR. STA. LOC."CB2-CA1'S(S1,S2
00022                   *
00023                   * DISPLAY BUFFER(PIA)
00024                   *
00025                   *--------------------
00026   8800    INSBF   EQU   $8800       INTERRUPT SLAVES BUFFER BYTE
00027   8801    INSST   EQU   $8801       TO INTERRUPT SLAVES -CA2
00028   8802    DWBF    EQU   $8802       DISPLAY BUFFER LOCATION
00029   8803    DWST    EQU   $8803       TO INTER. S3(NMI) THR. CB2
00030                   *
00031                   *---------------------------------------
00032                   * ADCS ADDRESSES
00033                   *
00034                   *
00035   9000    ADC0    EQU   $9000       FIRST ADC ADDR. VA
00036   9001    ADC1    EQU   $9001       VB
00037   9002    ADC2    EQU   $9002       VC
00038   9003    ADC3    EQU   $9003       IA
00039   9004    ADC4    EQU   $9004       IB
00040   9005    ADC5    EQU   $9005       IC
00041                   *---------
00042                   *
00043                   * SAMPLES ADDR.FOR SIG.'S
00044                   *
00045                   *-------
00046   001C    SAD1    EQU   $1C
00047   001D    SAD2    EQU   $1D
00048   0022    CON2    EQU   $22
00049   0024    VIHH    EQU   $24
00050   0025    VILL    EQU   $25
00051   0026    CON1    EQU   $26
00052                   *
00053                   * SLAVES(#1 & #2)TASKS FLAGS LOCATIONS
00054                   *
```

NOTE
Complete program listing.... (12 pages) is on file in the Dept. of E.E., U.M. ..
Contact Prof. G.W. Swift

---

133

MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.3
MODIFIED IAMC VER: 1.0

```
00001                    NAM   SLAVE1
00002                   ****************************************
00003                   * THIS  IS THE ASSEMBLED PROGRAM FOR   *
00004                   * SLAVE#1 IN THE MULTI-MICROPROCESSOR *
00005                   * -BASED TRAVELLING WAVE RELAY        *
00006                   * (PH.D THESIS , M.M.MANSOUR, 1984)   *
00007                   ****************************************
00008  0021     NMAX    EQU   33          NUM. OF SAM.'S/CYC.
00009  F601     D1FA    EQU   $F601       D1S1 SEEN BY MASTER
00010  0015     EPS     EQU   $15         THRESHOLD
00011                   *
00012                   *
00013                   * MESSAGE COMMUNICATION BUFFERS(PIA'S)
00014                   *
00015                   *--------------------
00016  8000     RBUF    EQU   $8000       READ BUFFER LOCATION
00017  8001     RSTAT   EQU   $8001       READ STATUS LOCATION
00018  8002     WBUF    EQU   $8002       WRITE BUFFER LOCATION
00019  8003     WSTAT   EQU   $8003       WRITE STATUS LOC.
00020                   *
00021                   *
00022                   *
00023                   *---------
00024                   *
00025                   * SAMPLES ADDR.FOR SIG.'S
00026                   *
00027                   *-------
00028  001C     SAD1    EQU   $1C
00029  0024     VIHH    EQU   $24
00030  0025     VILL    EQU   $25
00031  0026     CON1    EQU   $26
00032                   *
00033                   * TASKS FLAGS LOCATIONS
00034                   *
00035                   *---------
00036  F400     FCF1    EQU   $F400       SLAVE#1 FIRST CYCLE FLAG
00037  F401     FFF1    EQU   $F401       SLAVE#1 FORWARD FAULT FLAG
00038  F402     BF1     EQU   $F402       SLAVE#1 BACKWARD FAULT FLAG
00039                   *---------
00040                   *
00041                   * CURRENT SIGNAL S(N)
00042                   *
00043  0027     VAN     EQU   $27
00044  0028     VBN     EQU   $28
00045  0029     VCN     EQU   $29
00046  002A     IAN     EQU   $2A
00047  002B     IBN     EQU   $2B
00048  002C     ICN     EQU   $2C
00049                   *
00050                   * DISCRIMINAT COMPONENTS "N"&"N-1"  LOCATIONS
00051                   *
00052  002D     DSN     EQU   $2D
00053  002E     DSNM    EQU   $2E
00054  002F     ID      EQU   $2F         FIRST COMPONENT
```

NOTE
Complete program listing (7 pages) is on file in the Dept. of E.E., U.M.
Contact Prof. G.W. Swift

---

134

MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.3
MODIFIED IAMC VER: 1.0

```
00001                    NAM   SLAVE2
00002                    ****************************************
00003                    * THIS  IS THE ASSEMBLED PROGRAM FOR  *
00004                    * SLAVE#2 IN THE MULTI-MICROPROCESSOR *
00005                    * -BASED TRAVELLING WAVE RELAY        *
00006                    * (PH.D THESIS , M.M.MANSOUR, 1984)   *
00007                    ****************************************
00008  0021    NMAX      EQU   33          NUM. OF SAM.'S/CYC.
00009  F602    D2FA      EQU   $F602       D2S2 READ BY MASTER
00010  0015    EPS       EQU   $15         THRESHOLD
00011                    *
00012                    *
00013                    * MESSAGE COMMUNICATION BUFFERS(PIA'S)
00014                    *
00015                    *--------------------
00016  8000    RBUF      EQU   $8000       READ BUFFER LOCATION
00017  8001    RSTAT     EQU   $8001       READ STATUS LOCATION
00018  8002    WBUF      EQU   $8002       WRITE BUFFER LOCATION
00019  8003    WSTAT     EQU   $8003       WRITE STATUS LOC.
00020                    *
00021                    *
00022                    *
00023                    *---------
00024                    *
00025                    * SAMPLES ADDR.FOR SIG.'S
00026                    *
00027                    *-------
00028  001C    SAD1      EQU   $1C
00029  0024    VIHH      EQU   $24
00030  0025    VILL      EQU   $25
00031  0026    CON1      EQU   $26
00032                    *
00033                    * TASKS FLAGS LOCATIONS
00034                    *
00035                    *---------
00036  F400    FCF2      EQU   $F400       SLAVE #2 FIRST CYCLE FLAG
00037  F401    FFF2      EQU   $F401       SLAVE #2 FORWARD FAULT FLAG
00038  F402    BF2       EQU   $F402       SLAVE # 2 BACKWARD FAULT FLAG
00039                    *---------
00040                    *
00041                    * CURRENT SIGNAL S(N)
00042                    *
00043  0027    VAN       EQU   $27
00044  0028    VBN       EQU   $28
00045  0029    VCN       EQU   $29
00046  002A    IAN       EQU   $2A
00047  002B    IBN       EQU   $2B
00048  002C    ICN       EQU   $2C
00049                    *
00050                    * DISCRIMINAT COMPONENTS "N"&"N-1"  LOCATIONS
00051                    *
00052  002D    DSN       EQU   $2D
00053  002E    DSNM      EQU   $2E
00054  002F    ID        EQU   $2F         FIRST COMPONENT
```

NOTE
Complete program listing (7 pages) is on file in the Dept. of E.E., U.M.
Contact Prof. G.W. Swift

---

MOTOROLA M6800 CROSS ASSEMBLER, RELEASE 1.3
MODIFIED IAMC VER: 1.0

```
00001                    NAM   SLAVE3
00002                   ****************************************
00003                   * THIS  IS THE ASSEMBLED PROGRAM FOR  *
00004                   * SLAVE#3 IN THE MULTI-MICROPROCESSOR *
00005                   * -BASED TRAVELLING WAVE RELAY        *
00006                   * (PH.D THESIS , M.M.MANSOUR, 1984)   *
00007                   ****************************************
00008  0021     NMAX    EQU   33          NUM. OF SAM.'S/CYC.
00009  F601     D1FB    EQU   $F601       DISCRIM. LOCATION
00010                   *
00011                   *
00012                   * MESSAGE COMMUNICATION BUFFERS(PIA'S)
00013                   *
00014                   *--------------------
00015  8000     RBUF    EQU   $8000       READ BUFFER LOCATION
00016  8001     RSTAT   EQU   $8001       READ STATUS LOCATION
00017  8002     WBUF    EQU   $8002       WRITE BUFFER LOC.
00018  8003     WSTAT   EQU   $8003       WRITE STATUS LOC.
00019                   *
00020                   *
00021                   *
00022                   *---------
00023                   *
00024                   * SAMPLES ADDR.FOR SIG.'S
00025                   *
00026                   *-------
00027  001C     SAD1    EQU   $1C
00028  0024     VIHH    EQU   $24
00029  0025     VILL    EQU   $25
00030  0026     CON1    EQU   $26
00031                   *
00032                   * TASKS FLAGS LOCATIONS
00033                   *
00034                   *---------
00035  F400     FCF3    EQU   $F400       SLAVE#3 FIRST CTCLE FLAG
00036                   *---------
00037                   *
00038                   * CURRENT SIGNAL S(N)
00039                   *
00040  0027     VAN     EQU   $27
00041  0028     VBN     EQU   $28
00042  0029     VCN     EQU   $29
00043  002A     IAN     EQU   $2A
00044  002B     IBN     EQU   $2B
00045  002C     ICN     EQU   $2C
00046                   *
00047                   * DISCRIMINAT COMPONENTS "N"&"N-1"  LOCATIONS
00048                   *
00049  002D     DSN     EQU   $2D
00050  002E     DSNM    EQU   $2E
00051  002F     ID      EQU   $2F         FIRST COPONENT
00052  0030     QD      EQU   $30         SECOND COMPONENT LOCATION
00053  0031     XD      EQU   $31         THE GREATER VALUE OF ID&QD
00054  0032     YD      EQU   $32         THE SMALLER VALUE OF ID&QD
```

NOTE
Complete program listing (6 pages) is on file in the Dept. of E.E., U.M.
Contact Prof. G.W. Swift

---

## REFERENCES


1. Chamia,M. and Liberman,S. "Ultra high speed relay for EHV/UHV transmission lines-development design and application." IEEE Trans.,vol.PAS-96,No.6: Nov./Dec 1978,pp. 2104-2116.

2. Yee,M.T.and Esztergalyos,J "Ultra high speed relay for EHV/UHV transmission lines-installation -staged fault tests and operational experience" ibid,Vol.PAS-97,No.5: Sept./Oct. 1978,pp.1814 -1825.

3. Hodges,M.E. and Mathews,C.,A. Wilkinson,S.,B. "Ultra-high speed relaying for transmission line protection" Western Protective Relay Conference: Spokane,Washington,Oct.16-18 1979.

4. Hicks,K.L. and Butt,W.H. "Feasibility and economics of ultra-high-speed fault clearing" IEEE Trans.,Vol. PAS-99,No.6: Nov./Dec. 1980,pp.2138-2145.

5. Giuliante,A.T,..et al.. "A directional wave detector relay with enhanced application capabilities for EHV and UHV lines" ibid, Vol.PAS-102, No.9, Sept. 1983,pp.2881-92.

6. Dommel,H.W.and Michels,J.M. "High speed relaying using travelling wave transient analysis" IEEE PES Winter Meeting: N.Y.,A78 214-9, Jan./Feb. 1978

7. IEEE Tutorial Course, "Computer relaying", Chapter 5, pp.40-50, Course Text 79EH014-7PWR, 1979.

8. Johns,A.T. "New ultra-high-speed directional comparison technique for the protection of e.h.v. transmission lines" PROC.IEE,Vol.127 Pt.c,No.4: July 1980,pp.228-239.

9. Crossley,P.A. and McLaren,P.G., "Distance protection based on travelling waves", IEEE Trans., Vol.PAS-102, No.9: Sept.1983, pp.2971-2983.

10. Crossley,P.A., "Distance protection based on travelling waves" Ph.D. Thesis, University of Cambridge, January 1983.

11. Takagi,T. etal.. "Fault protection based on travelling wave theory-part I theory" IEEE PES Summer Meeting, A77,750-3,July 1977.

12. Takagi,T. etal.. "Fault protection based on travelling wave theory-part II sensitivity analysis and laboratory test" IEEE PES Winter Meeting,A78 220-6 Feb.1978.

13. Takagi,T. etal.. "Feasibility study for a current differential carrier relay system based on travelling wave theory" ibid A78 132-3.

14. Takagi,T. etal... "Digital differential relaying system for transmission line primary protection using travelling wave theory- its theory and field experience" IEEE PES Winter Meeting: A79 096-9,Feb. 4-9 1979.

15. Akimoto,Y., et al.., "Microprocessor based digital relays application in TEPCO" IEEE Trans., Vol.PAS-100, No.5, May 1981, pp.2390-2397.

16. Vitins,M. "A correlation method for transmission line protection" IEEE Trans.,Vol.PAS-97,No.5: Sep./Oct. 1978,pp.1607-1617.

17. Bignell,A.M. "Further thoughts on ultra high speed relaying of transmission lines." The 9th. Annual Western Protective Relay Conference: Spokane,Washington, Oct.26-28,1982.

18. Esztergalyos,J and Einarsson,E. "Ultra high speed protection of three-terminal lines". CIGRE paper 34-06,1982 Session 1-9 Sept.

19. Rajendra,S. and McLaren,P.G., "A high speed protection scheme for multi-terminal lines" Paper No. 12.6, 19th Universities Power Engineering Conference, University of Dundee, Dundee, Scotland, April 1984.

20. "Protection aspects of multi-terminal lines" Special Publication of the IEEE: 79 TH0056-2-PWR,pp.1-18,1979.

21. Dommel,H.W. "Digital computer solution of electro magnetic transients in single and multi-phase networks" IEEE Trans.,Vol.PAS-88,: April 1969,pp.388-399.

22. Dommel,H.W. and Meyer,W.S., "Computation of electromagnetic transients", Proc. of IEEE, Vol.62, No. 7, July 1974, pp.983-993.

23. Wedepohl,L.M. "Application of matrix methods to the solution of travelling -wave phenomena in polyphase systems" PROC.IEE,Vol.110,No.12 : Dec. 1963,pp.2200-2212.

24. Moore,R.K. "Travelling-wave engineering" (Book), Mc-Grew-Hill, N.Y. 1960.

25. Marti,J.R., "Accurate modelling of frequency-dependent transmission lines in electromagnetic transient simulations" IEEE Trans., Vol.PAS-101, January 1982, pp.147-155.

26. Semlyen,A. and Dabuleanu,A. "Fast and accurate switching transient calculations on transmission lines with ground return using recursive convolution", IEEE Trans., Vol.PAS-94, No. 2, March/April 1975, pp.561-571.

27. "Electromagnetic transients program EMTP" Rule Book: User's Manual,BPA,1980.

28. Swift,G.W. "The spectra of fault induced transients" IEEE Trans.,Vol.PAS No.3: May/June 1979,pp.940- 947.

29. Bornard,P.and Bastide,J.C. "A prototype of multiprocessor based distance relay" IEEE Tranns.,Vol.PAS-101,No.2 Feb.1982. pp.491-498.

30. Jeyasurya,B. and Smolinski,W.J. "Design and testing of a microprocessor-based distance relay" IEEE Trans., Vol.PAS-103, No.5, May 1984 pp.1104-1110.

31. Buttner,P., etal... "Development of a multiple microprocessor distance relay" IEE Second International Conference on Developments in Power System Protection 10-12 June 1980,pp.123-126.

32. St-Jacques,A.L. and Santerre,G. "A multiprocessor-based distance relay: design featuring and test results", IEEE Trans.,Vol.PAS-102,No.12: Dec. 1983 pp.3842-49.

33. Kapusniak,E. etal... "A master-slave multi-microprocessor system" International Journal of Mini and Microcomputers, Vol.3,No.2 1981,pp.25-29.

34. Kapusniak,E., "A microprocessor-based multiprocessing system", M.A.Sc. Thesis, Department of Electrical Engineering, University of Toronto, June 1979.

35. Fathi,E.T. and Butt,W.H. "Multiple microprocessor systems: what, why and when" IEEE Computer Magazine,March 1983,pp.23-32.

36. Fathi,E.T., "Task-driven multi-microcomputer system," Master's Thesis, University of Ottawa, 1981.

37. Bowen,B.A. and Buhr,R.J.A. "The logical design of multiple microprocessor systems" (Book), Prentiple-Hall, Englewood Cliffs, N.Y., 1980.

38. Pimentel,J.R. and Loeffler,M.T., "A real-time engine simulator using multiple microcomputers" IEEE Trans., Vol.IE-30,No.2: May 1983, pp.117-126.

39. Toda,A. etal.., "A parallel processing simulator for network system using multimicroprocessor", Microprocessor and Microsystems, Vol.6,No.1: Jan./Feb. 1982, pp.15-20.

40. Greenfield,J.D. and Wray,W.C., "Using microprocessors and microcomputers: the 6800 family", John Wiley & Sons, 1981.

41. "Motorola microprocessor data manual", 1981

42. "The TTL data book for design engineers", Texas Instruments Incorporated, Second Edition, 1976.

43. "Linear data book", National Semiconductor, 1980.

44. "Data conversion/acquisition data book", National Semiconductor, 1980.

45. Adams,W.T. and Brady,J., "Magnitude approximation for microprocessor implementation" IEEE MICRO: Oct. 1983, pp.27-31.

46. Schdel,H., "In-circuit emulation for multi-processor systems" Northcon/83, Portland, Oregon: May 10-12,1983, paper 20/2.

47. Filip,A.E. "Linear approximation to $\sqrt{x^2 + y^2}$ having equiripple characteristic" IEEE Trans., Vol.AU-21, No.3, 1973, pp. 554-556.