Electrostatic Force Sampling of Digital Waveforms Using Synchronous Time Domain Gating

by

Sunny Ping San Cheung

A thesis
submitted to the Faculty of Graduate Studies
in partial fulfillment of the requirements
for the degree of

Master of Science

Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Manitoba
Canada

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A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree of Master of Science

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Abstract

Non-Invasive internal testing of high speed microelectronics is essential for failure analysis and design verifications. With these advance and complex integrated circuits decreasing in dimensions and operating voltages, and increasing in speed, a non-contact technique with high spatial, temporal and voltage resolutions that can accomplish internal node measurements of integrated circuit over passivation with minimal calibrations is longed for by the microelectronics industry. Several internal test techniques are available but they often failed to compromise between these criteria.

The utilization of the electrostatic force microscope for measuring integrated circuits has been explored by diagnostic researchers over the last decade. This technique satisfies the above desired criteria except bandwidth which is restricted by the frequency response of a mechanical cantilever.

This thesis presents electrostatic force sampling of high speed digital waveforms with the method of synchronous time domain gating to overcome the inherent bandwidth limitation. By inputting synchronized input signals into various low cost switches and gates, a proper probe signal can be generated to allow high speed digital sampling with the electrostatic force microscope. Two special cases of synchronous time domain gating is examined: amplitude and pulse width modulation.

The performance of the proposed instrument using both modulation schemes is evaluated using theoretical characterizations and measurements on a ceramic transmission line, a passivated 0.5μm CMOS inverter chain, and a NT25 pulse generator. Non-invasive extractions of up to 1*Gb/s* digital patterns are demonstrated with a voltage sensitivity in the range of tenths of millivolts and a delay accuracy of less than 10*ps*. The current bandwidth of the instrument is up to 3-4*GHz* which can be improved by the speed of the time domain gating circuitry. This thesis vindicates that the presenting technique is a suitable diagnostic tool for sampling internal nodes of high speed microelectronic circuits.

Acknowledgements

Written by Sunny Cheung.
Patiently adviced and supervised by Dr. Greg Bridges.
Draft editing: Dr. Greg Bridges and Sunny Cheung
References search assisted by Engineering librarians and the people who compiled the "reference/publication folders" in the SPM lab.
Concept of synchronous time domain gating conceived by Dr. Greg Bridges, Dr. R.A. Said, and D.J. Thomson.
Understanding of all theoretical concepts assisted Dr. Greg Bridges, Dr. Doug Thomson, Dr. R.A. Said, Dharmand Noruttun, Tam Lam and Dave Shimizu.
Figure 2.1 appears courtesy of Darius Romanek.
Figure 2.2, 3.1, 3.5, 3.7, 3.12, and 3.13 appears courtesy of Dharmand Noruttun.
Figure 3.3, 3.8, 3.9, 4.6, 4.7, 4.8, 4.9, 4.10, 4.14, and 5.1 appears courtesy of Tam Lam.
Figure 6.17 appears courtesy of Duc-Thang Tran.
Micromachined cantilevers purchased by Dr. Greg Bridges.
Mounting of the cantilever onto a circuit board and the mechanical probing structures by Dr. Greg Bridges, Tam Lam and Sunny Cheung.
Optical Beam Deflection Sensor on the mechanical probing structures in figure 3.9 and 3.10 were designed and manufactured by Richard Qi and Micron Force Instruments (MFI), respectively.
Mechanical probing structure in figure 3.9 by Bill, Al Simmons and Richard Qi.
Mechanical probing structure in figure 3.10/3.11 by MFI.
Photographs in figure 3.10, 3.11, and 4.12 by Jen and Sunny Cheung.
All microphotographs supplied by Dr. Greg Bridges.
Computer Software for automating the experiments by Sunny Cheung, Dharmand Noruttun and Dr. R.A. Said.
All experimental implementations by Sunny Cheung.
All measurements performed by Sunny Cheung.
Transmission line filter designed by Dr. Greg Bridges and Sunny Cheung.
Equipments and commercial devices purchased by Dr. Greg Bridges with financial support by Natural Sciences and Engineering Research Council (NSERC), the Canadian Microelectronics Corporation (CMC), and Micronet.
Cadence and HspiceS managed by Guy Jonatschuk.
PCB for NEL GaAs AND logic circuit designed by Dr. Greg Bridges and Sunny Cheung
Soldering of NEL GaAs AND logic circuit by Al McKay.
Ceramic Transmission Line designed by Leili Shafai.
0.5μm CMOS inverter chain designed by Richard Qi and fabricated through CMC.
NT25 Pulse Generator designed by Duc-Thang Tran and fabricated through CMC.
Most information in section 7.2 supplied by Dr. Greg Bridges.

For all the above who contributed to this thesis, especially Dr. Greg Bridges and everyone who are and were involved with the SPM lab, thank you. Thanks for my family and friends for their engineering or philosophy related discussions, and their support and guidance to me in countless ways. Lastly but most importantly, I want to thank God for giving me life and for letting me to see the light in life.

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Chapter 1

Introduction

1.1 Motivation

The prominent microelectronics industry asks for more suitable diagnostic techniques to accommodate the continual progress of digital integrated circuits which are increasing in speed and decreasing in size and power consumption. The latest Semiconductor Industry Association Roadmap [1] suggests in the near future the emergence of microelectronic circuits with deep submicrometer structure numbers, several gigahertz clock rates, and only hundreds of millivolts of operating voltage. For design verification and potential failures analysis in modern microelectronics, diagnostic instruments that allow internal access to arbitrary nodes of integrated circuits become advantageous over conventional probing methods [2]. To effectively and conveniently perform internal testing of high frequency integrated circuits, a diagnostic instrument should be non-invasive while having a high bandwidth. Preferably it should allow internal measurement over passivation with minimal calibrations and preparations. High spatial resolution, voltage sensitivity, and delay accuracy are also among the merits of a diagnostic tool.

1.2 Outline

This thesis presents electrostatic force sampling of high speed digital signals using synchronous time domain gating. Following this introduction, a few alternatives to the presenting technique along with their working principles, capabilities, and disadvantages are surveyed in the next chapter. Chapter 3 expounds the operation of the various components in the electrostatic force probing instrument along with a review of a few existing schemes for measuring DC and high frequency analog signals. The method of synchronous time domain gating for producing a proper sampling signal for high speed digital signal probing is thoroughly discussed in Chapter 4. Chapter 5 theoretically characterizes the proposed sampling technique using the standards of spatial resolution, invasiveness, voltage sensitivity, bandwidth, and delay resolution. Chapter 6 presents the specific measure-

ment system used in this work as well as exhibits and examines measurements performed on matched transmission lines, a $0.5\mu m$ CMOS inverter chain, and a NT25 pulse generator using the suggested method to substantiate that the diagnostic instrument satisfies its aforementioned desirable criteria. Lastly, future considerations and conclusions are given in Chapter 7 to finalize this thesis.

Chapter 2

Review of Internal Testing Techniques

Many diagnostic tools are available for measuring internal signals of high frequency integrated circuits besides electrostatic force probing. This chapter explores some of the alternative techniques used in microelectronics testing.

2.1 On-Wafer Contact Probing

The common reason for employing on-wafer probing is to avoid the packaging of defective wafers. Performing on-wafer probing on a loose die before packaging is economically attractive because the cost of the package increases with circuit speed and pin counts. The prevalence of on-wafer probing is also earned from its relatively facile preparations. On-wafer probing requires direct contact of a probe onto an unpassivated pad in the circuit. Designers often have to add probing pads that accommodate the dimensions of the on-wafer probes into their designs. Various types of contact probes exist, and their functions, limitations and benefits of some of these probes will be discussed in the next few sections.

2.1.1 Low Impedance Passive Probes

For microwave applications, low impedance passive probes, which can provide high bandwidth measurements are frequently utilized. These probes have been utilized for FET, passive elements, monolithic microwave integrated circuits (MMIC), and lossy transmission line system characterization. They are recently used at frequencies beyond $100GHz$ [3]. A vector network analyzer is usually employed along with a passive probe to measure the S-parameters of a device under test (DUT). Figure 2.1 demonstrates a typical implementation. The S-parameters reveal the operation and matching properties of a device or circuit. Most network analyzers customarily provide calibration procedures to compensate errors created by the probes, cables, and connectors for more accurate measurements. These calibrations can be performed on a calibration substrate prior to wafer testing.

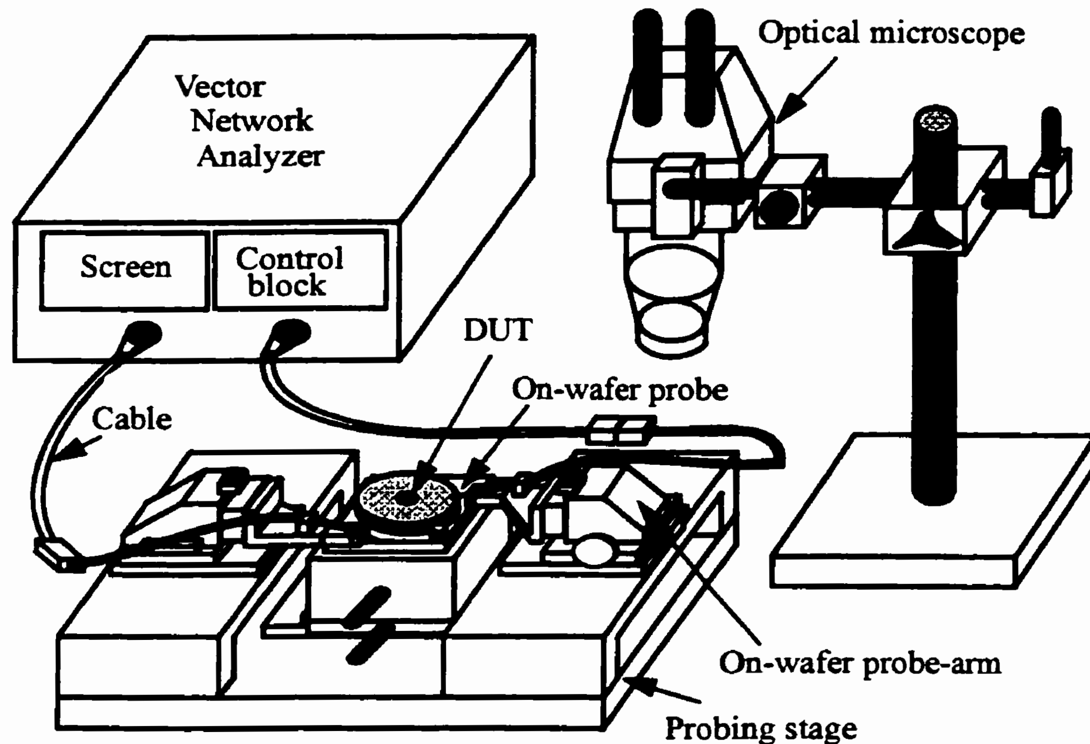


Figure 2.1: Typical implementation for microwave on-wafer probing.

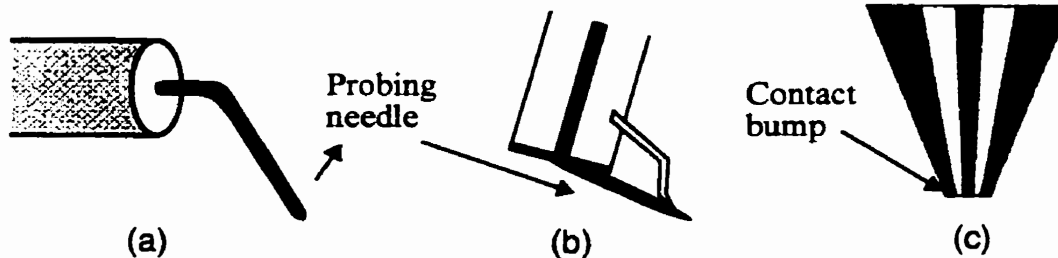


Figure 2.2: Common types of microwave on-wafer probes: (a) coaxial, (b) microstrip, and (c) coplanar [4].

Since these are contact probes, they should offer 50Ω characteristic impedance down to their tips. Three different types of these microwave probes are often used [4], and they are illustrated in Figure 2.2. The coaxial and the microstrip styles offer a 50Ω characteristic impedance terminated at the tiny probing needle. The major flaws of these probes are high parasitics and their lack of proper grounding near the test point.

The coplanar probe is fed by a waveguide which contains a signal line between two grounds on the same side of the substrate. Contact bumps are added at the end of the probe

for touching onto the wafer. Distance between the contact bumps is referred to as the pitch which is typically 150μm [5]. This is a popular probe because it provides efficient grounding near the test point, and it has low parasitics and radiation properties. Figure 2.3 depicts an example of relative probe placement on a circuit. To accommodate on-wafer probing using the coplanar probe, the pads at the test points must be in a ground-signal-ground configuration, as displayed in figure 2.3. Hence, the obvious disadvantage is its size. Probing becomes restricted to only a few locations on the circuit because of limited wafer space, probe accessibility, and addition of parasitics by placing large pads onto the design. In most cases, measurements can only be conducted at the input and output ports of a circuit.

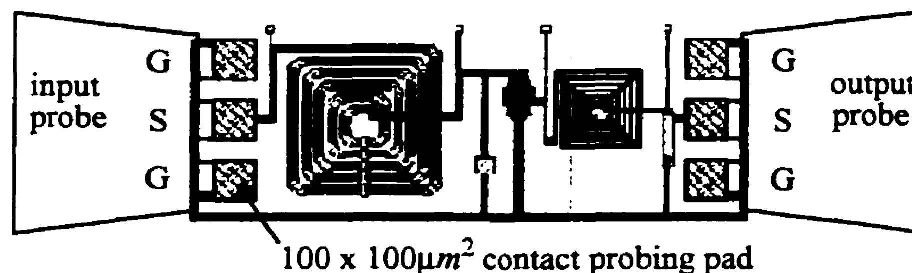


Figure 2.3: Diagram exemplifying probe positioning for measuring on a MMIC using the coplanar on-wafer probe.

These passive probes may also be used to feed high speed or direct current (DC) excitation signals to the wafer. Measurement setup can sometimes be tedious when a DUT requires DC biasing as multiple probes may be accessing the circuit simultaneously.

2.1.2 Resistive Divider Probes

The resistive divider probe is a passive contact probe that can be applied in both analog and digital signal testing. Typically the probe is connected to a 50Ω scope or other test instruments with 50Ω loads. This probe has near its tip, a resistor which provides a large resistance to the circuit test point to minimize loading. This resistor in the probe forms a voltage divider with the 50Ω load, thus resulting in an attenuation of the measured signal. A 450Ω resistor divider, for instance, causes a 10:1 attenuation of the measured signal in a 50Ω system. Commercial versions of these probes are capable of measuring beyond

10*GHz* [5]. One of the major disadvantages lies in its large parasitic loading onto the test circuit. Since there exists a trade off between resistive loading and the attenuation of the measured signal, poor voltage sensitivity is resulted when a large resister divider is used.

2.1.3 High Impedance Active Probes

High impedance active probes are often employed, together with oscilloscopes for testing internal nodes of analog or digital integrated circuits. This probe gives a very high input impedance but suffer in bandwidth, which is determined by an active element near the tip of the probe. Commercial active probes have bandwidths of less than 10*GHz*, but typically only 3*GHz*. The active probe used in this research is from Picoprobe [6], and it has a MOS transistor which limits the 3*dB* bandwidth of the probe at 1*GHz*. The probe makes direct contact onto the wafer using a sharp probing needle which is made of tungsten. It is very static sensitive because of the direct coupling to the gate of the transistor that acts as a buffer between the needle and a coaxial transmission line. The Picoprobe used has a loading of 0.04*pF* which is mostly contributed by the gate of the transistor. This loading increases with the size of the transistor, indicating a trade off between non-invasiveness and bandwidth. For example, a 3*GHz* active probe with a tip radius of 0.1μm is also available from Picoprobe, but it has a larger loading of 1*pF*. Another apparent limitation of using this probe is that measurement is impossible over passivation.

2.2 Electron Beam and Photoemission Probing

Electron beam potential probing permits measurement at internal nodes of high frequency integrated circuits. Branched from scanning electron microscopy, it has been commercially available and widely utilized by the microelectronics industry for the past two decades [7].

Figure 2.4 shows a diagram explaining the method. The technique uses an electron gun to supply a primary electron beam which focuses onto a test point. The primary beam causes secondary electrons to volley back from the circuit. The energy of these secondary electrons, collected by a detector, are analysed by a retarding grid spectrometer. The voltage at the test node is dependent on the number and kinetic energy of the electrons

received. A feedback mechanism can be utilized to maintain a fixed detector signal by tuning the grid potential of the spectrometer, thereby tracing the node voltage [8].

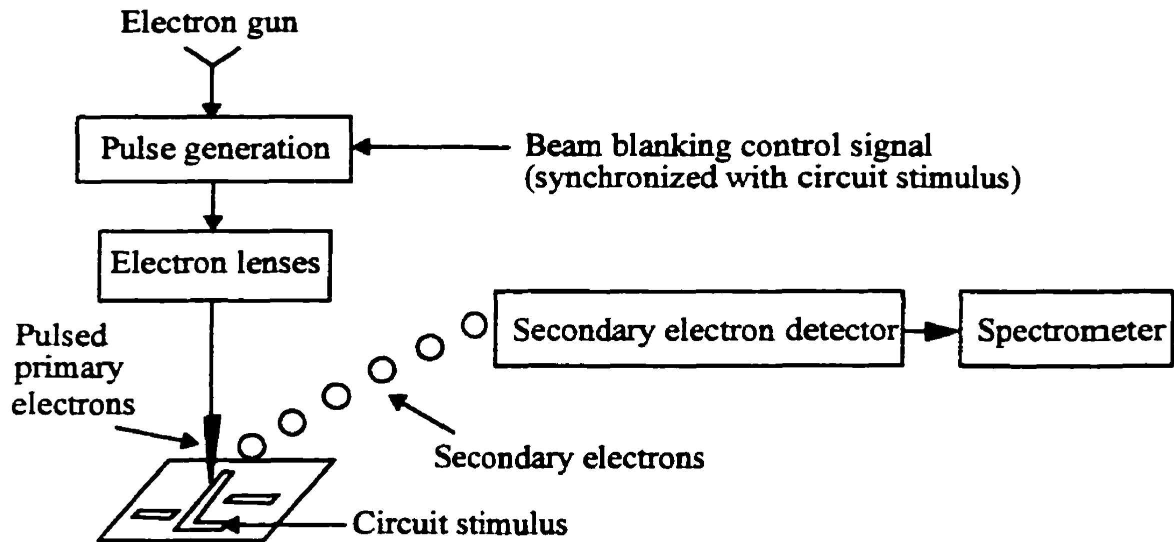


Figure 2.4: Sketched implementation of high-speed electron beam testing.

High frequency sampling is enabled by providing short duration electron pulses as the primary beam. These pulses are synchronized with the repetitive circuit excitation signal to assure proper sampling. Several mapping schemes are available for electron beam testing. In waveform mapping, a slow phase scan between the circuit signal and the electron beam pulses gives a mapping of the signal waveform at a single point of interest on the circuit. A logic state map is accomplished by executing a 1-D cross section scan with the beam-circuit signal phase shift increasing linearly. Voltage contrast provides a spatial scan, or logic image of the entire surface of a circuit at a fixed phase difference between the pulsed beam signal and the circuit stimulus [8].

Due to the relatively wide primary electron sampling pulses of about $40ps$ and the transit time effect of the secondary electrons [9], the frequency capability of electron beam probing is limited at $8GHz$ [10]. For a rather low primary electron beam energy, the technique is non-invasive to normal circuit operation. A voltage sensitivity of $160mV/\sqrt{Hz}$ is achievable [11]. Although this is a powerful diagnostic tool with a high temporal resolution and a $0.5\mu m$ spatial resolution [11], the technique has its fair share of disadvantages [12]. The testing system is very complex and expensive since measurement must be done

in a vacuum. Wearisome calibrations cause the method to grapple with passivated circuits.

The operation of photoemission probing [13] almost resembles electron beam testing. The major point of departure is the usage of a laser beam in photoemission probing rather than an electron beam for improving the bandwidth. A $5ps$, $0.5\mu m$, and $5mV$ temporal, spatial, and voltage resolution, respectively, using a $1ps$ duration laser pulse were purported for photoemission sampling [13,14]. Poor stability and reliability when measuring air-exposed circuits are among the disadvantages.

2.3 Electro-Optic Probing

The electro-optic probing technique is based on the Pockels Effect [15], which is due to a rotation of optical polarization that is imposed by an electric field across an optical crystal. Applications of this method include internal measurement of high frequency digital integrated circuits [16] and field mapping in MMICs [17].

The characteristics of the electric field is related to the voltage on a circuit. By monitoring the change in the polarization of light passing through a crystal within this field, information of the electric field and circuit voltage can be obtained.

The two general techniques are direct and indirect electro-optic probing [18,19]. Direct probing is performed on circuits that are fabricated on electro-optic substrates such as GaAs. Indirect probing must be practiced on devices which are built on non-electro-optic materials such as silicon. A probe with an electro-optic crystal tip is used in indirect probing. This probe situates at a close distance above the circuit test point at where the electro-optic crystal tip senses the electric stray field lines induced by the desired voltage. Figure 2.5 shows the difference in configurations between direct and indirect probing. In direct probing, the optical laser beam is transmitted through the electro-optic substrate inside which the electric field is coupled with the beam. The sampled voltage is proportional to the alteration in the optical polarization. If the ground plane is not present as in the case of a coplanar waveguide, the optical beam can be directed into the electro-optic substrate from the back side of the circuit. In external electro-optic probing, the laser beam is directed down to the bottom of the crystal probe tip at where the beam is reflected back for voltage evaluation.

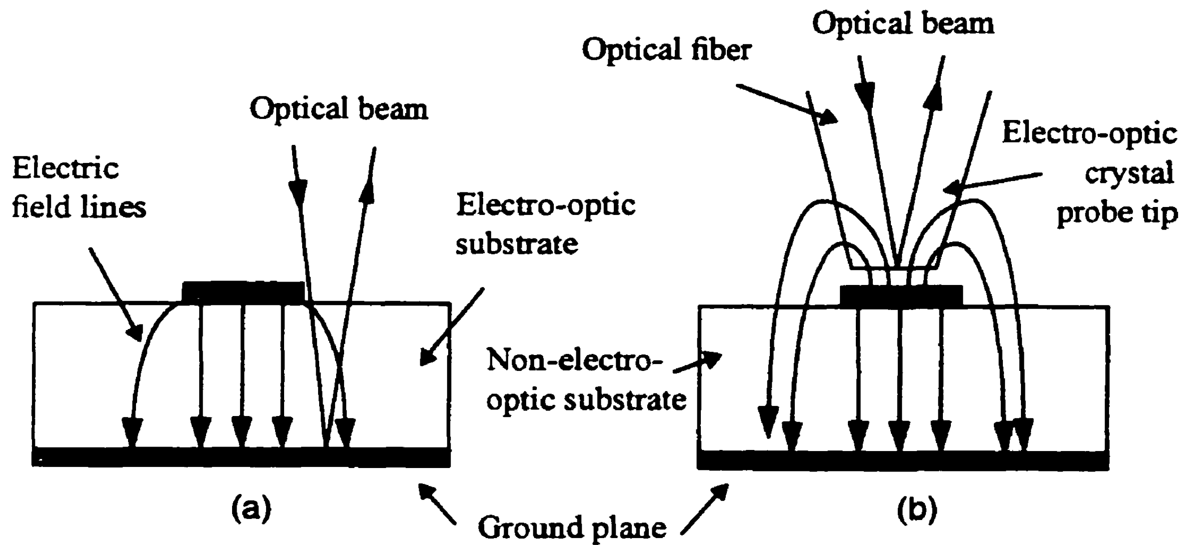


Figure 2.5: Configurations for (a) direct and (b) indirect (external) electro-optic probing over microstrip interconnect.

Sampling at extremely high frequencies is made possible by using as short as sub-picosecond duration optical pulses as the optical source. Analog measurements of $60GHz$ in direct probing and $100GHz$ in indirect probing have been reported [11]. Measurement of a $20Gb/s$ digital pattern on an integrated circuit was also performed [20]. The voltage resolution is in the order of tens of millivolts [11]. Spatial resolution which relies on the size of the focused laser beam in direct probing, is approximately $0.5\mu m$ in diameter [21].

Electro-optic probing also possesses similar weaknesses as in electron beam probing such as cost, complexity and irritating calibrations. Circuits with passivation are almost impossible to be measured. Invasiveness is not a large concern in direct probing. For indirect probing, the capacitive loading introduced by the dielectric crystal probe may disturb normal operation. Perhaps the largest disadvantage is the poor spatial resolution when measuring circuits with non-electro-optic substrates due to the size of the external probe. In addition, indirect probing only deals with weak fringing fields in cases such as the microstrip line, as demonstrated in figure 2.5(b). Hence, circuit density and positioning of the crystal probe become significant factors as the method is more prone to crosstalk effect.

2.4 Photoconductive Sampling

Photoconductive sampling uses a photoconductive switch to measure high frequency integrated circuits. The physical switch is simply a slit between two metallic electrodes fabricated on a doped semiconductor material such as GaAs, which has a small energy-band gap to allow a fast electron-hole recombination time. To enable high speed sampling, picosecond width laser pulses which are synchronized with the circuit signal are directed onto the slit to create extra carriers in the semiconductor, thus temporary conducting the two electrodes and causing short-duration electrical shorts.

These photoconductive switches are typically built in as circuit elements and consequently limit the quantity of internal test points. Very recently, high speed in-circuit sampling using a micromachined photoconductive probe was successfully achieved [22]. The probe contains near its tip a photoconductive switch which attaches to a single mode optical fiber for coupling with the laser pulses, thereby creating a high speed pulse generator on the probe. The probe makes direct contact with the test point to measure absolute voltages on passivated microwave and digital integrated circuits [23]. The micromachined probe in [22] has a bandwidth that exceeds $100GHz$, a $1\mu m$ spatial resolution and a voltage sensitivity of $100nV/\sqrt{Hz}$. The circuitry on this micromachined cantilever unfortunately may present a large capacitive loading, which depends on the size and geometry of the photoconductive switch of the probe in [22]. These probes also often need very high power laser sources.

2.5 Reactive Coupling Probing

Reactive probing is a contactless technique that utilizes electromagnetic probes for coupling near fields from a test circuit or device. Two types of coupling: capacitive and inductive exist for near field probing. Reactive probing is mainly used in MMIC and antenna imaging [24]. Micromachined probes are recently employed for small MMIC circuits to improve spatial resolution [25].

Chapter 3

Electrostatic Force Probing

This chapter studies the electrostatic force microscope (EFM) in the application of circuit probing, or electrostatic force probing. The origin of EFM along with its other siblings in the scanning probe microscope (SPM) family will be presented first in a cursory fashion, follow by the explanation of the operating principle of electrostatic force probing and its integral components. Lastly, a few existing schemes for probing DC and high frequency analog signals using EFM will be reviewed.

3.1 Scanning Probe Microscopy

Since the early 80's, SPM [26] has been used for extracting topographical, mechanical, thermal, optical, electrical, and magnetic properties of microscopic materials. The attractiveness of the instrument is mainly on its capability of measuring in atomic scale which is not achievable by optical microscopes and scanning electron microscopes (SEM). The SPM utilizes a small mechanical probe to measure its near-field interaction with the object under test. Properties of a material can be obtained by scanning the probe over the entire surface of interest. The spatial resolution is mostly defined by the radius of curvature of the probe's tip and the tip-surface spacing which are typically in the order of nanometers.

Atomic resolution was first achieved by Binnig and Rohrer when the scanning tunnelling microscope (STM) was brought to fruition in 1982 [27]. In this instrument, a voltage difference is applied between a sharp conducting tip and a conducting surface separated by a few Angstroms. This induces the tunnelling of electrons through the tip-surface gap, thus forming a current which gives information about the gap distance. As illustrated in figure 3.1, the tip scans through the surface in a constant current mode in which a feedback system is used to control a piezoelectric that maintains a constant tip-surface separation. By monitoring the voltage that controls the vertical piezoelectric positioner, a topographical image of the surface is extracted.

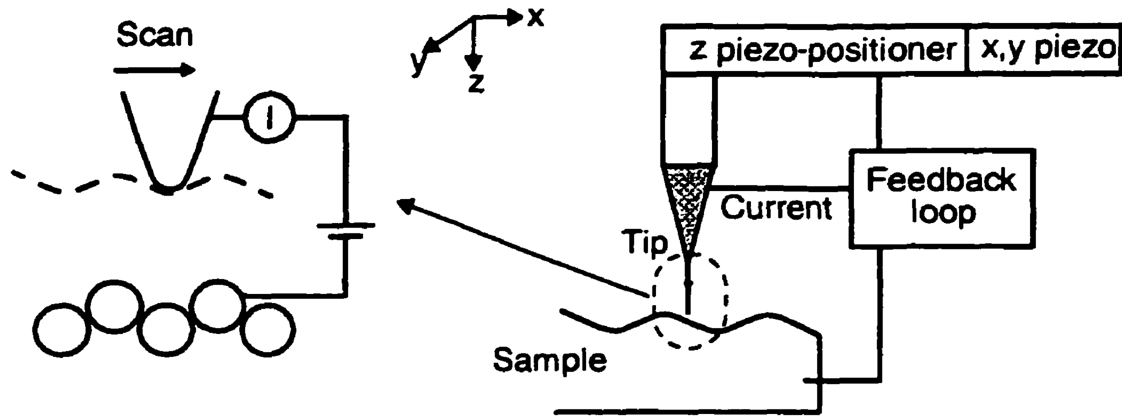


Figure 3.1 Illustration of the scanning tunnelling microscope operating in constant current mode [27].

The success of this initial STM experiment has propelled and conceptualized many other scanning probe microscopes which paved a new line of testing and imaging techniques. This section briefly situates the works and applications of many of these microscopes in the SPM family.

A slight modification of STM was emerged to measure electric potential distribution in semiconductors. This revised instrument, known as the scanning tunnelling potentiometer, enables measurement of surface potential and topography simultaneously [28]. This technique has been used for obtaining potential characteristics of P-N junctions, Schottky barriers, and heterostructures [28].

Measurements with STM can only be performed on conducting materials. However, STM served as a foundation for the development of atomic force microscope (AFM) which overcomes this restriction, hence allowing the imaging of insulators, semiconductors and conductors with atomic resolution [29]. In the AFM, a cantilever with a sharply spiked tip is placed in contact with the surface of the material under investigation. The designated contact force is typically in the order of nano-Newtons. The repulsive force, resulted from the overlapping of electron clouds of atoms between the tip and the surface, is monitored rather than the tunnelling current. As the tip is scanned over the sample, the interacting atomic forces deflect the cantilever. The optical beam detection technique [30] is often used for measuring these cantilever deflections. A feedback system is used to preserve a constant repulsive force during the scan to track the topography of the sample.

Scanning thermal microscope [26] was evolved from AFM for mapping temperature variations on material surfaces. Application of this method can be found in failure detection of microelectronics [31]. Undesired open and short circuits are detected by resolving the thermal pattern on the surface of the circuit. The microscope has a resolution of ten-thousandth of a degree [26].

The scanning capacitance microscope (SCM) [32] and scanning resistance microscope (SRM) [33] are contact microscopes that permit the profiling of carrier and dopant concentrations in semiconductors with nanometer spatial resolution. Both microscopes use contact capacitance and resistance, respectively, to trace dopant levels in semiconductor devices. These microscopes are very useful for the verification of sub-micron device fabrications.

For non-invasive testing on samples and microelectronics, microscopes which operate in non-contact mode are desired to minimize deformation of surfaces and disturbance of normal operation on circuits. With these non-contact instruments, its tip is held above the sample at a typical distance of 10-100nm away at where forces such as Van Der Waals, Coulomb, and magnetic forces between the tip and the sample endures [34]. The laser force microscope (LFM) [29] is one of the few that operates without the tip contacting the surface. It employs the attractive forces due to surface tension by moisture that condenses at the tip-surface gap, as well as Van Der Waals forces. Surface profiling of semiconductors is one of the application of LFM.

The idea of AFM also indirectly inspired the magnetic force microscope (MFM) which uses a magnetic tip to detect magnetostatic forces [35]. This non-contact microscope uses a sharp magnetic tip which is usually iron or nickel for their strong magnetic dipole moments, and the tip is placed usually a few nanometers above to the sample. With a piezoelectric attaching to a cantilever that holds the tip, the cantilever is excited with an oscillating signal at a frequency close to its mechanical resonance. Due to the interactions between the tip and the sample, the force gradient on the magnetic tip modifies the resonance frequency of the cantilever. The shift in resonance can be detected by observing the change in amplitude, phase or frequency of the cantilever vibration. MFM can image topography and magnetic domains in a wide range of materials, and it is most suitable for imaging magnetic recording medium which produces strong stray magnetic fields. Lateral

resolution is in the order of 10*nm* [36]. An interesting application of MFM is internal current probing of integrated circuits [37]. Utilizing Ampere's law, magnetic fields radiating from current carrying conductors were imaged by scanning a magnetic tip over an integrated circuit in [37]. Current directions and magnitudes were examined from the resulted images with reported sensitivities of 1*mA* DC and 1μA AC (alternating current).

An important long-ranged forces yet unmentioned is the electrostatic force. Electrostatic force microscopy [38] has excited the microelectronic testing field. This novel instrument measures the localized surface potential by monitoring the electrostatic force between a conducting probe and the sample. Applications of EFM has been in imaging and depositing localized surface charges [39], dopant profiling of semiconductors [40], imaging ferroelectric domains [41], measuring contact potential difference between various types of materials [42], and the main focus of this research: measuring signals in integrated circuits [43,44,45,46,47,48,49,50,51].

3.2 Operation Principle

The basic operation of the electrostatic force probing involves mechanical deflections of a conducting cantilever with a sharp tip under the influence of a electrostatic force formed by a potential difference between the tip and the circuit. The objective is to measure a localized potential on a circuit under test.

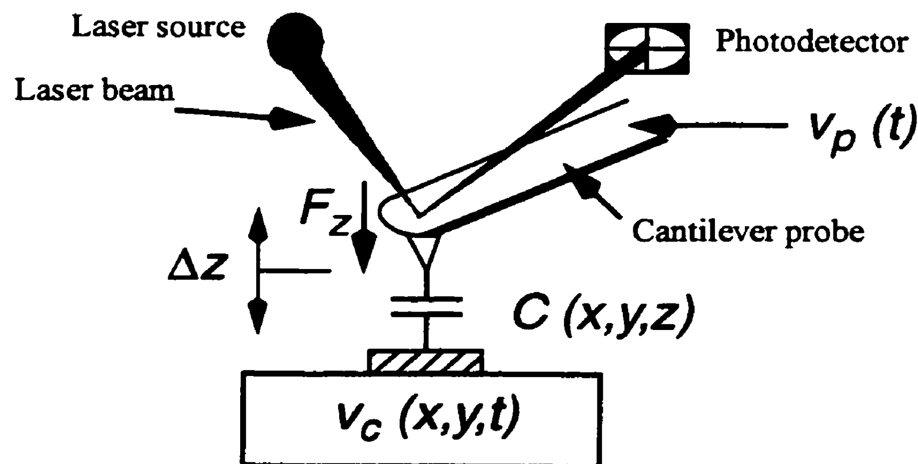


Figure 3.2 The operation principle of electrostatic force probing.

As demonstrated in figure 3.2, a cantilever is situated at a small distance above the test point to measure the desired signal $v_c(x,y,t)$ on the circuit. The cantilever is supported in a way such that it can be deflected by an applied force. A specified $v_p(t)$ is sent to the conducting cantilever to produce a potential difference with the signal $v_c(x,y,t)$, thereby forming a virtual localized capacitance $C(x,y,z)$ between the tip of the cantilever and the test point. The energy required to charge up this capacitor can be translated to an attractive force that induces a cantilever deflection. The force is expressed as:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)[v_p(t) - v_c(x,y,t)]^2 \tag{3.1}$$

where $C(x,y,z)$ is dependent on the physical geometry and relative positions of the cantilever and the circuit. The term $C(x,y,z)$ also includes unwanted coupling and fringing capacitances which affect the assorted resolutions of the instrument.

Under actual conditions, the vertical force in (3.1) also depends on DC offset effects such as surface charges [52], and these effects are represented by the term $\Delta\Phi(x,y)$. The force in (3.1) should therefore be:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)[v_p(t) - v_c(x,y) + \Delta\Phi(x,y)]^2 . \tag{3.2}$$

By sensing the deflections of the cantilever induced by the force in (3.1), information about the circuit signal $v_c(x,y,t)$ can be obtained. An optical beam detection technique [30] was used to measure the deflections in this research.

To explore the capabilities and limitations of electrostatic force probing, characterizations must be performed on the components of the instrument. The next few sections will contain a detailed study of the cantilevers and the deflection sensing mechanism used in the experiments.

3.3 Cantilever Characterization

The cantilever deflection by the electrostatic force F_z relies on the mechanical properties of the cantilever. Attributes of the cantilever plays an essential role in characterizing the spatial, voltage, and delay resolutions of the probing instrument. These crucial properties of the cantilever are the spring constant and the frequency response.

3.3.1 Spring Constant

Like a spring, the spring constant of the cantilever, k, defines the rigidity of its vibration, and is given by [38]:

$$k = \frac{3EI}{l^3} \tag{3.3}$$

where l is the length of the cantilever, and E is the modulus of elasticity which is dependent on the material composition of the cantilever. The moment of inertia, I is different for various cross sections of the cantilever. A cantilever with a rectangular cross section of width w and thickness t has a moment of inertia $I=wt^3/12$. The spring constant of this cantilever is then:

$$k = \frac{Ewt^3}{4l^3} \ . \tag{3.4}$$

3.3.2 Frequency Response

The deflection of the cantilever is a function of the mechanical frequency response of the cantilever. A cantilever has the propensity to vibrate at a frequency called the natural resonant frequency. The vibration amplitude of the cantilever is maximum if the frequency of the applied force on the cantilever is equal to the natural resonant frequency of the cantilever. At frequencies distant from the resonance, the amplitude of the cantilever deflection is relatively small. The fundamental resonant frequency of a vibrating cantilever with a rectangular cross section, ω_r, is given by [38]:

$$\omega_r \approx \sqrt{\frac{k}{0.24\rho wtl}}; \ \omega_r = 2\pi f_r \tag{3.5}$$

where k is the spring constant, and ρ is the mass density of the material composition of the cantilever. For a micromachined cantilever, the lumped mass of its tip is usually negligible as compared to the distributed mass of the cantilever. The mass of the tip is therefore disregarded in (3.5). Under an external force with a unit amplitude, the vibration of the cantilever as a function of frequency, i.e. the frequency response, is [38]:

$$|G(\omega)| = \frac{(Q/k)(\omega_r/\omega)}{\sqrt{1+Q^2\left(\frac{\omega_r}{\omega}-\frac{\omega}{\omega_r}\right)^2}}, \ \omega > 0; \ |G(\omega)| = 1/k, \ \omega = 0 \tag{3.6}$$

where Q is the quality factor, and it is defined as $\omega_r/\Delta\omega$, with $\Delta\omega$ being the $3dB$ bandwidth from resonance. The cantilever deflection due to the force F_z in (3.2) is:

$$\Delta z(\omega) = F_z(\omega)\frac{(Q/k)(\omega_r/\omega)}{\sqrt{1+Q^2\left(\frac{\omega_r}{\omega}-\frac{\omega}{\omega_r}\right)^2}}, \omega > 0; \; \Delta z = F_z/k, \omega = 0. \qquad (3.7)$$

By examining (3.7), it can be observed that when the driving frequency is equal to the resonance $\omega=\omega_r$, the cantilever deflection is:

$$\Delta z|_{\omega_r} = \frac{Q}{k}F_z|_{\omega_r} \qquad (3.8)$$

which is maximum among all other frequencies. The magnitude of vibration at ω_r is enhanced by Q from that at DC at where $\omega=0$. Other resonances at higher frequencies exist as well, but their corresponding quality factors are smaller.

3.3.3 Micromachined Cantilevers

Wire probes were used in the early development of electrostatic force probing. A competent cantilever for probing should have a high resonance frequency and quality factor, with a small mass and spring constant. A cantilever with higher resonant frequency is less susceptible to low frequency noises, and a smaller cantilever improves the spatial resolution of and parasitic loading by the instrument. With a reduction in the spring constant, the force needed to induce a cantilever deflection is lessened, thus elevating the measurement sensitivity. These are often the primary reasons for choosing fabricated micromachined cantilevers over wire probes.

Two types of micromachined cantilevers were employed in this thesis. One of them was a V-shaped silicon nitride (Si_3N_4) cantilever [53] as displayed in figure 3.3. The pyramidal tip in the bottom photograph of figure 3.3(b) was deposited at about $4\mu m$ from the end of the cantilever, and the tip has an estimated height of $4\mu m$. Radius of curvature is used to define the sharpness of the pyramidal tip, and it is approximately $300nm$. For better conduction and optical reflection, the cantilever was coated with a thin gold film.

Another type of micromachined cantilever utilized in this project, as shown in figure 3.4, was the sc12-E silicon cantilevers from NT-MDT [54] with W_2C coating.

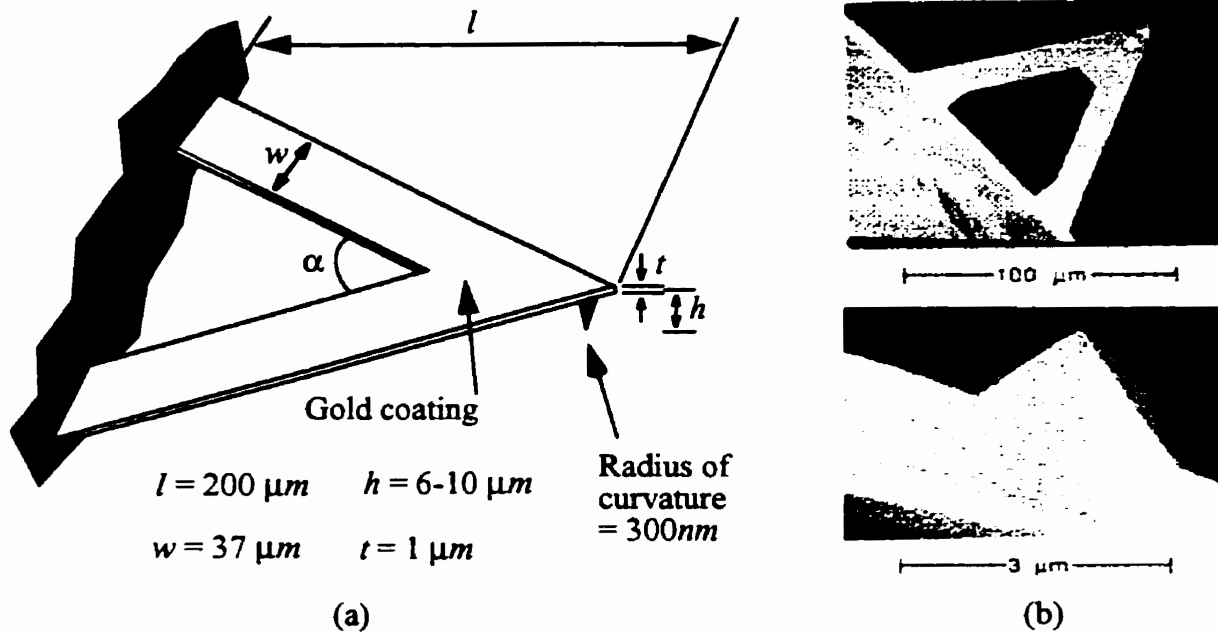


Figure 3.3: (a) Schematic diagram of the micromachined Si_3N_4 cantilever used with dimensions listed. (b) SEM microphotograph of the pyramidal tip located near the end of the cantilever [53,55].

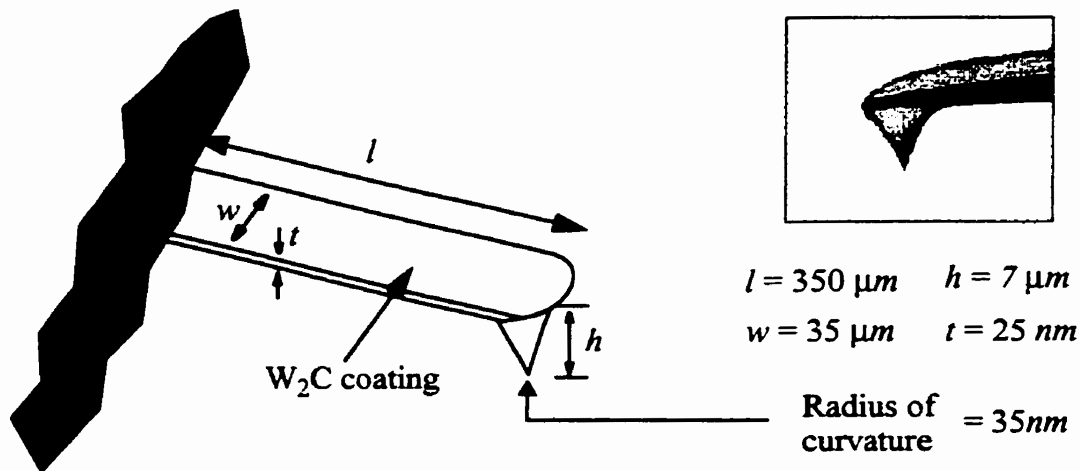


Figure 3.4: sc12-E silicon cantilever from NT-MDT with a picture of the pyramidal tip and manufacturer's specifications [54].

Because of the complicated geometry of the Si_3N_4 cantilevers, an accurate spring constant calculation is usually resorted to numerical or experimental techniques. The spring constant of the cantilever is 0.064*N/m* according to specifications [53], while the specified spring constant of the silicon cantilever in [54] is 0.050*N/m*.

Figure 3.5 exhibits the frequency response of the Si_3N_4 cantilever [56] while figure 3.6 shows the response of the silicon cantilever. Both experimental curves were extracted using the frequency spectrum of the intrinsic cantilever vibration by thermal noise which has a spectral property similar to that of white noise. A more detail account of this noise will be studied in section 5.3. The Si_3N_4 cantilever has an actual resonant frequency of 12.2750*KHz*. The resonance of the silicon cantilever was experimentally found to be 13.0625*KHz* using a spectrum analyzer. The respective theoretical frequency responses for both cantilevers were obtained by plotting (3.6). The method used for determining the experimental values of the cantilevers' quality factors was by substituting the most appropriate value of Q into (3.6) to match the corresponding experimental frequency responses. The Si_3N_4 cantilever has a Q=32, and the silicon cantilever has a Q=30. The minor discrepancy between the theoretical and the experimental curves is mostly due to the background noise that exists in the environment.

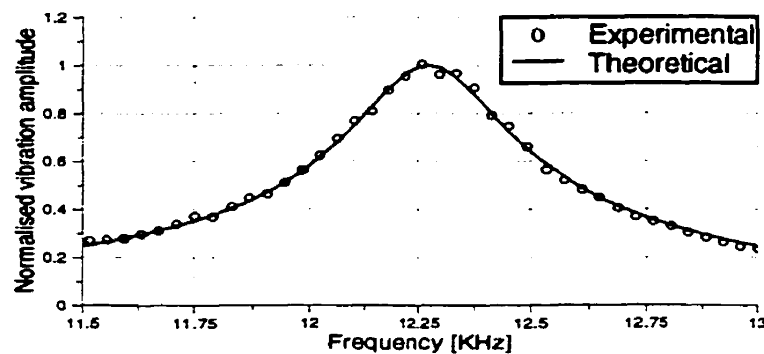


Figure 3.5: Normalized mechanical frequency response of the selected Si_3N_4 micromachined cantilever for this project. It has a fundamental resonance of 12.275*KHz*, Q=32, and k=0.064*N/m* [56].

Using equation (3.4) and (3.5), the spring constant and the resonant frequency of the micromachined rectangular silicon cantilevers can be theoretically approximated from their given dimensions and material properties. Using ρ=2330 kg/m^3 and E=1.79x10^11N/m^2, the theoretical values of k and f_r for the silicon cantilever are determined and compared with specifications by the manufacturers and experimental findings in table 3.1. The experimental value of the spring constant is computed by algebraically solving (3.5) for k and substituting 13.0625*KHz* as the resonant frequency f_r.

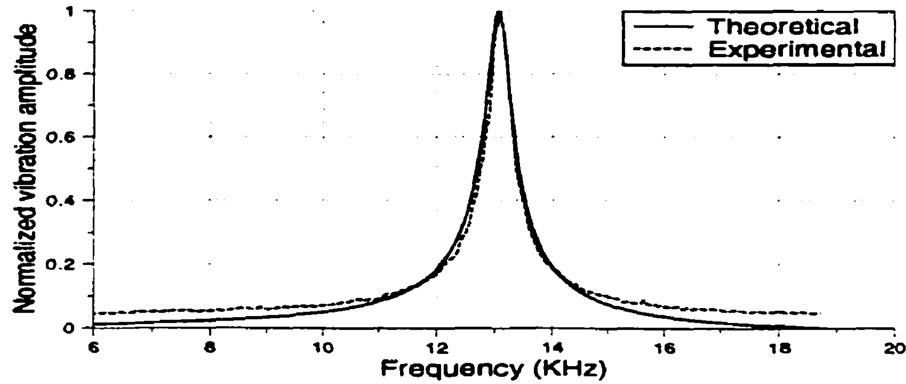


Figure 3.6: Normalized mechanical frequency response of the silicon cantilever with a resonant frequency of 13.0625*KHz*, Q=30, and k=0.055*N/m*.

	k (N/m)	f_r(KHz)
Specifications	0.050	13.0000
Theoretical	0.063	13.9300
Experimental	0.055	13.0625

Table 3.1: Comparisons between the theoretical calculations, experimental findings, and specifications for the spring constant and resonant frequency of the silicon cantilever.

3.4 Optical Beam Deflection Sensor

The typical magnitude of cantilever deflection in electrostatic force probing is very small. A rough calculation of the force using a capacitor plate model [38] was performed and found to be in the order of pico-Newtons [57]. Assuming that the amplitude of the applied force on a cantilever with k=0.055*N/m* and Q=30 at its fundamental resonance is 1*pN*, then, the corresponding deflection by using (3.8) is about 0.5*nm*. Hence, the detection technique used should be as or more sensitive. A laser beam-bounce detection system [30] was employed in this work. The diagram in figure 3.7 depicts the method. A laser source with a focused laser beam is directed onto the end of the cantilever. The reflected laser beam from the cantilever is captured by a carefully positioned bi-cell photodiode.

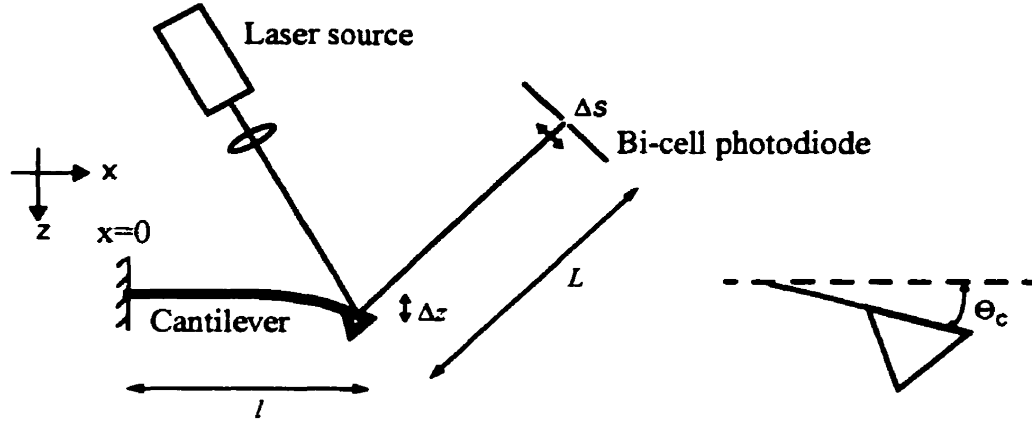


Figure 3.7: Diagram illustrating laser beam-bounce detection for sensing cantilever deflections.

The following is a derivation of the relationship between the received optical signal at the bi-cell photodiode and the cantilever deflection. When a cantilever with a rectangular cross section is under an applied vertical force F, the deflection of the cantilever is [58]:

$$z(x) = \frac{F}{6EI}(3lx^2 - x^3) \tag{3.9}$$

where l is the length of the cantilever, E is the modulus of elasticity, and I is the moment of inertia of the cantilever. Since the deflection magnitude is small, the angle of deflection Θ_C at the end of the cantilever, $x=l$, can be approximated using small angle approximation:

$$\Theta_c \approx \left.\frac{dz}{dx}\right|_{x=l} = \frac{Fl^2}{2EI}. \tag{3.10}$$

Using (3.3) and $F=k\Delta z$, equation (3.10) becomes:

$$\Theta_c \approx \frac{3}{2}\frac{\Delta z}{l}. \tag{3.11}$$

The cantilever deflection Δz displaces the reflected laser beam by Δs at the bi-cell photodiode as illustrated in figures 3.7 and 3.8. Using similar triangles, it can be found that $\Theta_C \approx \Delta s/L$ [57] where L is the distance between the cantilever and the centre of the bi-cell photodiode. Therefore:

$$\Delta s \approx \frac{3L\Delta z}{2l}. \tag{3.12}$$

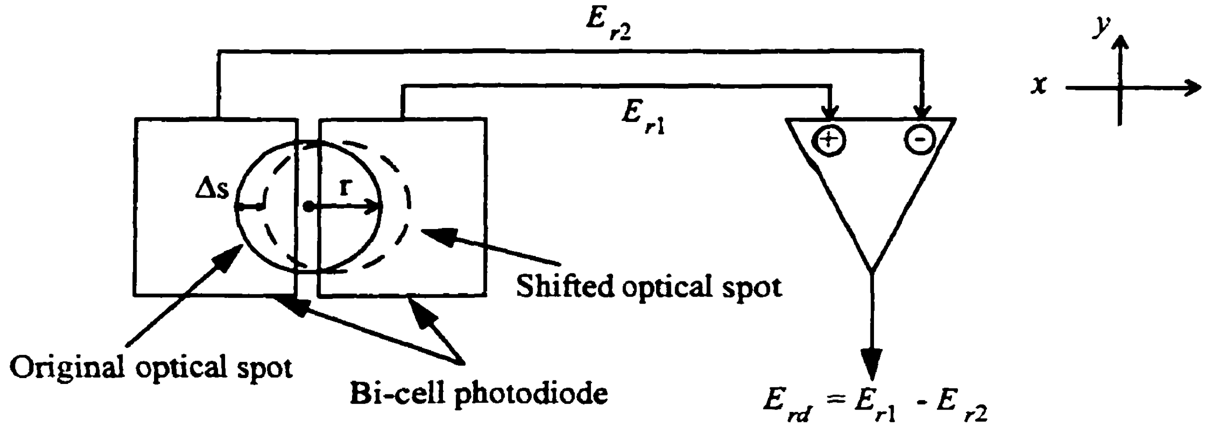


Figure 3.8: Diagram demonstrating the shifting of the reflected laser beam Δs at the bi-cell photodetector due to a cantilever deflection. The difference between the optical signals received by the two cells of the photodiode is related to Δs and the cantilever deflection Δz.

Originally, the bi-cell photodiodes are placed such that the reflected laser beam is incident on both photodiodes with equal optical power. When a deflection Δz causes a shift Δs in the reflected beam, more optical signal is accepted by one cell of the photodiode than the other. The deviation in optical signals absorbed between the two photodiodes should give information about the deflection Δz.

A laser diode was used as the optical source in the experiments. It can be assumed that the laser beam is monochromatic, and possesses a Gaussian power distribution. The optical power per unit area, or the irradiance of the reflected laser beam is [59]:

$$E_r = E_o e^{\frac{-2r^2}{r_o^2}} = E_o e^{-\frac{2}{r_o^2}(x^2 + y^2)} \quad (3.13)$$

where E_o is the irradiance at the centre of the laser beam, and r_o is the distance from the centre of the beam at which the irradiance falls to $1/e^2$ from E_o. Lets assume the photodiode is ideal so that the total optical power received by the photodiode is completely converted into electrical power. The accumulated photocurrent must then be equal to the total number of photons per second, N entering the photodiode multiplied by the unit charge q. Neglecting the small spacing between the two cells in the photodiode, the gained current by one cell due to a deflection is the same amount lost by its neighbour. The difference in

photocurrent between each cell, I_d, can be evaluated by integrating the normalized Gaussian laser beam over the gained area in one of the cells due to the shift Δs [57]:

$$I_d = 2Nq\int_0^{\Delta s}\int_{-Y}^{Y}\frac{e^{-\frac{2}{r_o^2}(x^2+y^2)}}{(\pi/2)r_o^2}dxdy \tag{3.14}$$

where Y is the size in the y dimension of the gained area. For $Y >> r_o$, (3.14) can be approximated as:

$$I_d \approx \frac{4Nq}{r_o^2\pi}\int_0^{\Delta s} e^{\left(-\frac{2}{r_o^2}\right)x^2}dx\int_{-\infty}^{\infty} e^{\left(-\frac{2}{r_o^2}\right)y^2}dy\,. \tag{3.15}$$

From the mathematical table in [60]:

$$\int_{-\infty}^{\infty} e^{\left(-\frac{2}{r_o^2}\right)y^2}dy = \frac{\sqrt{\pi}}{2}r_o^2, \tag{3.16}$$

then,

$$I_d \approx \frac{2Nq}{\sqrt{\pi}}\int_0^{\Delta s} e^{\left(-\frac{2}{r_o^2}\right)x^2}dx\,. \tag{3.17}$$

Using a change in variable and let $t=\sqrt{2}x/r_o$, then (3.17) can be written as:

$$I_d \approx \frac{2Nq}{\sqrt{\pi}}\int_0^{\sqrt{2}\Delta s/r_o} e^{-t^2}dt\,. \tag{3.18}$$

The integral can now be solved by referring to the mathematical table in [60], and (3.18) is now:

$$I_d \approx Nq\,erf\left(\frac{\sqrt{2}\Delta s}{r_o}\right) \cong \frac{2\sqrt{2}Nq}{\sqrt{\pi}}\frac{\Delta s}{r_o}\,. \tag{3.19}$$

Using (3.12), the photocurrent I_d can finally be expressed as a function of cantilever deflection Δz:

$$I_d \approx \frac{3\sqrt{2}NqL}{\sqrt{\pi}r_o l}\Delta z\,. \tag{3.20}$$

The result in (3.20) infers that relative changes in the difference output signal from the detection system can be conveniently interpreted as a corresponding change in cantilever deflection. Variables in (3.20) may serve as amplification factors to the deflection. The only sensible change, however, is to decrease the spot size of the laser beam r_o, and this is often difficult to achieve [57].

Similar to other optical deflection sensors, the performance of the laser beam-bounce system is limited by mostly shot noise but it is insensitive to $1/f$ noise since it is a differential system [57]. Shot noise is created by the random photon arrival at the detector, and it can be minimized by compromising the geometry of the detection system. The sensitivity of the laser beam-bounce system was purported to be $7.9\times10^{-6} nm/\sqrt{Hz}$ in [61]. This finding is later discovered to be insignificant for determining the voltage sensitivity of electrostatic force probing since other noise sources are dominant.

3.5 Mechanical Probing Structures

The cantilever and the optical detection system used in electrostatic force probing must be physically integrated onto a mechanical structure. The instrument structure should be designed with high rigidity so that the noise due to inherent mechanical vibration is minimized. Two mechanical stages were utilized for probing in this work.

One of the physical stage used is shown in figure 3.9. The stage is supported by an anodized aluminium structure which holds the circuit, the cantilever, a 3-D piezoelectric positioner for positioning the circuit, and the components of the optical beam-bounce system. The base of the stage is supported by four vibration absorbers in its corners which acts as a damper for better vibration isolation. The adjustments of the circuit piezoelectric positioner can be done manually using micrometer-pitched screws or a piezoelectric controller. The stage also includes a manual positioning system for aligning the laser source and the photodector to direct the optical beam onto the cantilever, and to collect the maximum optical signal from the reflected beam, respectively. The cantilever is mounted onto the end of a 50Ω coplanar transmission line on a printed circuit board which is screwed securely onto the aluminium stage.

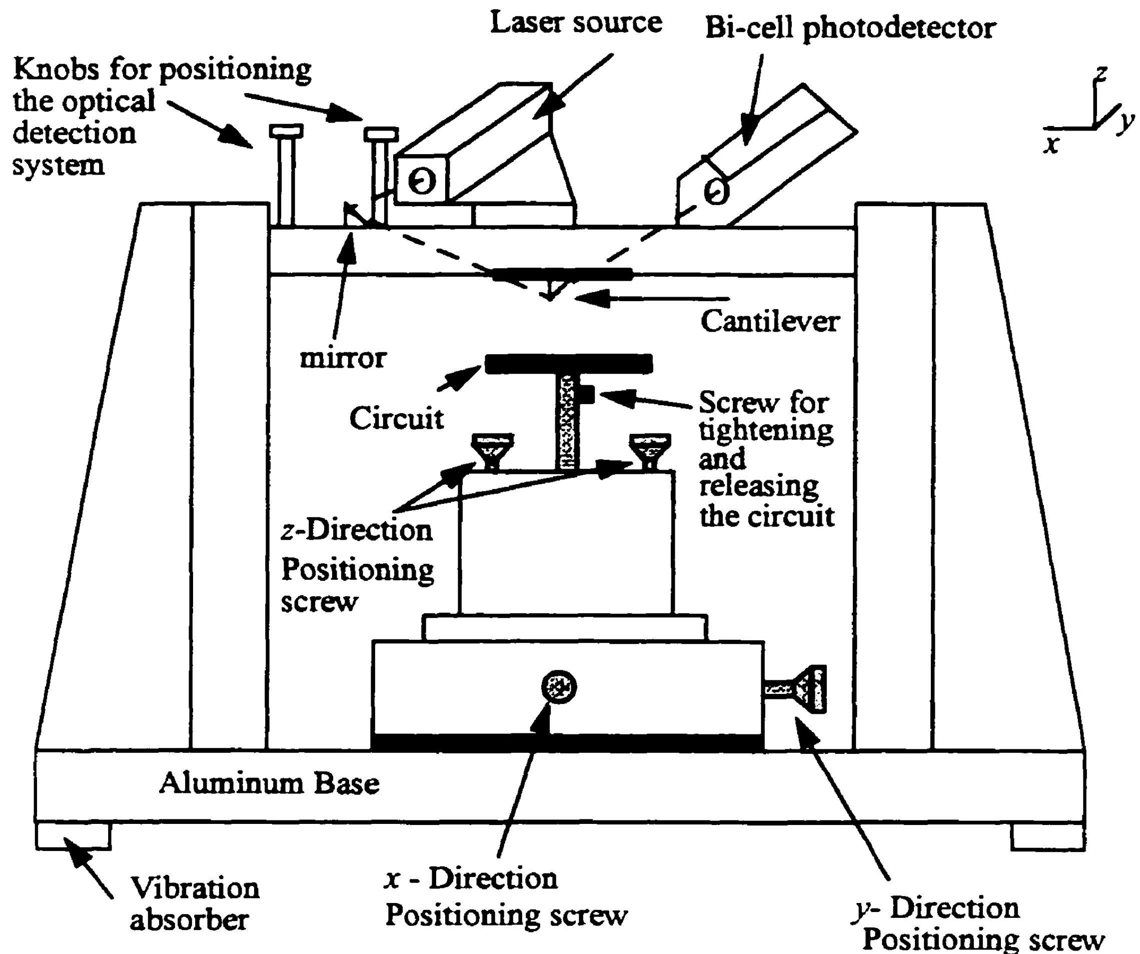


Figure 3.9: A drawing of the mechanical structure for electrostatic force probing using a manual aligning mechanism for the optical detection system.

Another physical probing structure used in this work was designed by Micron-Force Instruments (MFI) [62] to automate the alignment of the optical beam-bounce system. Figure 3.10 shows a photograph of the aluminium probing structure which contains the cantilever and the parts of the optical detection system. This structure uses a magnetic positioner to firmly mount on a probing station which includes an optical microscope and a 3-D manual circuit positioner. Vibration absorbers were used at the base of the probe station. The laser source on the structure focuses its beam through a prism onto a mirror which directs the beam to the cantilever. The reflected beam off the end of the cantilever travels back to the prism which acts as a polarized light beam splitter, and the optical signal is captured by a bi-cell photodector. A computer with a software provided by MFI was

used to receive and display the signals from the optical detection system. Depending on the geometry and original positions of the components in the beam-bounce system, this software may also automatically calibrate their positions by driving electrical motors on the structure. These parts can also be adjusted using manual knobs and screws. Similar to the previous setup, a 50Ω coplanar line with the cantilever at its end was screwed onto the structure.

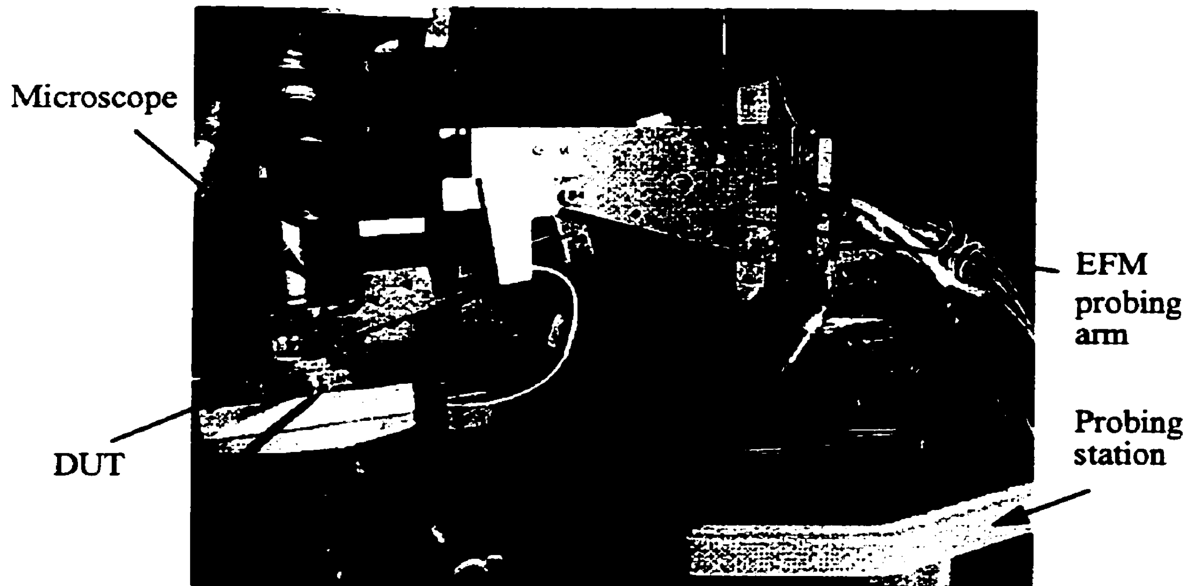


Figure 3.10: The aluminium probing structure designed by MFI [62]. It holds the cantilever, the optical beam-bounce system, as well as electrical motors and manual knobs for positioning the above components. It is magnetized onto a probing station that contains a microscope and a circuit positioner.

Figure 3.11: A zoomed view of figure 3.10 showing the cantilever and DUT.

3.6 DC and Analog Signal Measurement Schemes

Signals on devices and circuits can be DC or time-varying. Often, the absolute voltage and relative phase at an arbitrary location on the circuit is required. Before discussing digital signal extraction, several measurement schemes using electrostatic force probing for measuring DC and analog signals is reviewed in this section. The DC measurement scheme using force nulling is introduced, follow by a theoretical presentation of vector voltage measurement which is used to measure high frequency sinusoidal signals.

3.6.1. DC Measurement

A DC signal on the circuit, $V_c(x,y)$, is constant in time, and the electrostatic force between the cantilever and the circuit produced by this DC signal with reference to (3.2) is:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)(v_p(t) - V_c(x,y) + \Delta\Phi(x,y))^2 \quad (3.21)$$

If this electrostatic force is to be evaluated, knowledge of the mutual capacitance between the tip and the circuit must be calculated. This requires precise and bothersome cantilever positioning. The concept of force nulling is conceived for conquering this problem, and is accomplished by driving the cantilever with the following signal [43]:

$$v_p(t) = A + K\cos(\omega_p t) \quad (3.22)$$

where A is a DC bias, and K is an arbitrary positive non-zero value. Both parameters are adjustable during the experiment. The frequency ω_p is chosen near the fundamental resonance of the cantilever, ω_r. Using (3.22), equation (3.20) can be expressed as:

$$\begin{aligned} F_z &= \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)(A + K\cos(\omega_p t) - v_c(x,y) + \Delta\Phi(x,y))^2 \\ &= \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\left\{\left[(A - v_c(x,y) + \Delta\Phi(x,y))^2 + \frac{K^2}{2}\right]\right. \\ &\quad \left. + 2[A - v_c(x,y) + \Delta\Phi(x,y)]K\cos(\omega_p t) + \frac{K^2}{2}\cos(2\omega_p t)\right\} \end{aligned} \quad (3.23)$$

which suggests that the force possesses only frequency components at DC, ω_p, and $2\omega_p$. The DC component translates into a static deflection. At frequency ω_p, the force is:

$$F_z\big|_{\omega_p} = \frac{\partial}{\partial z}C(x,y,z)[A - v_c(x,y) + \Delta\Phi(x,y)]K\cos(\omega_p t) \qquad (3.24)$$

which vibrates the cantilever at the frequency ω_p. By selecting ω_p equal to the resonance of the cantilever, ω_r, the deflection improves by the quality factor of the cantilever, Q, from DC. Using (3.8), the deflection is:

$$\Delta z\big|_{\omega_r} = \frac{\partial}{\partial z}C(x,y,z)\frac{Q}{k}[A - v_c(x,y) + \Delta\Phi(x,y)]K\cos(\omega_r t) \ . \qquad (3.25)$$

Equation (3.25) reveals that the cantilever deflection can be nulled by adjusting A such that it is equal to $[V_c(x,y)+\Delta\Phi(x,y)]$, and the assessment of the mutual capacitance $C(x,y,z)$ becomes unnecessary. For relatively small DC offset effects $\Delta\Phi$, the voltage on the circuit can be found by reading the parameter A when the deflection is zero.

The implementation of the DC measurement scheme is presented in figure 3.12 [63]. The cantilever is placed at a close distance above a test point on the circuit. The cantilever oscillations are detected by a deflection sensing system and a lock-in amplifier which only monitors the deflection amplitude at the resonant frequency of the cantilever. The output of the lock-in amplifier is directed through a feedback system at where it is integrated and summed by an AC signal generator, thereby allowing the parameter A to be controlled to achieve a nulled deflection.

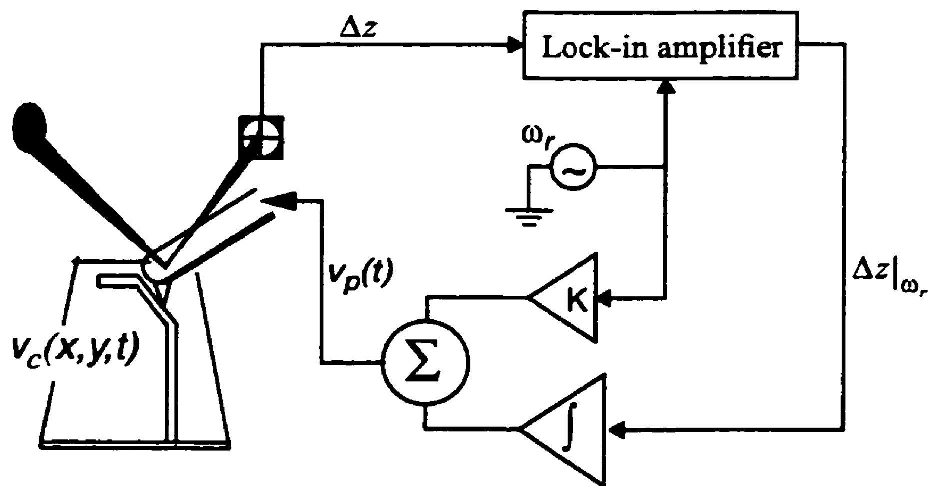


Figure 3.12: Block diagram illustrating the DC measurement scheme using electrostatic force probing for obtaining absolute DC voltages [63].

3.6.2. Vector Voltage Measurement

The objective of vector voltage measurement is to acquire the magnitude V_c and relative phase ϕ_c of a high frequency sinusoidal signal on a circuit:

$$v_c(x, y, t) = V_c \sin(\omega_0 t + \phi_c) \tag{3.26}$$

where ω_0 is usually much higher than the resonant frequency of the cantilever. Electrostatic force probing depends on the frequency response of the cantilever used in the instrument. Without proper manipulation of the signal to the cantilever, high frequency measurement is unfeasible. A modulation concept is implemented to downconvert a high frequency signal to a frequency near the resonance for amplifying the cantilever deflections. This idea will be expounded in the next chapter. In the next two subsections, two amplitude modulation schemes for measuring high speed analog signals will be presented.

3.6.2.1. Sinusoidal Modulation

The specified signal applied to the cantilever for sinusoidal modulation is [47]:

$$v_p(t) = (A + K\cos(\omega_r t))\sin(\omega_0 t + \phi_p) \tag{3.27}$$

where A, K, and ϕ_p are adjustable parameters. Under such excitation, the electrostatic force in (3.2) acting on the cantilever is:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x, y, z) \tag{3.28}$$
$$([A + K\cos(\omega_r t)]\sin(\omega_0 t + \phi_p) - V_c\sin(\omega_0 t + \phi_c) + \Delta\Phi(x, y))^2$$

Expanding the square term in (3.28) yields components at DC, ω_r, $2\omega_r$, ω_0, $2\omega_0$, $\omega_0 \pm \omega_r$, $2\omega_0 \pm \omega_r$, and $2\omega_0 \pm 2\omega_r$. Using (3.8), the induced cantilever deflection by the force component at ω_r is:

$$\Delta z|_{\omega_r} = \frac{1}{2}\frac{\partial C}{\partial z} \cdot \frac{Q}{k} \cdot K[A - V_c\cos(\phi_p - \phi_c)]\cos(\omega_r t) \ . \tag{3.29}$$

Since $\Delta z|_{\omega_r} \propto [A - V_c\cos(\phi_p - \phi_c)]$, equation (3.29) hints that the nulling idea should once again be employed here. By cleverly adjusting the parameters A and ϕ_p, the deflection can be nulled, thereby revealing the magnitude and phase of $v_c(x,y,t)$ without deter-

mining *C(x,y,z)*, *Q*, *k*, and $\Delta\Phi(x,y)$. As a matter of fact, this method is independent of DC offset effects because $\Delta\Phi(x,y)$ is absent from (3.29).

The nulling procedure must require an optimization algorithm because the phase cannot be determined without the knowledge of magnitude, and vise-versa. To understand this algorithm, a plot of cantilever deflection amplitude versus the phase difference ϕ_p-ϕ_c is exhibited in figure 3.13 [56].

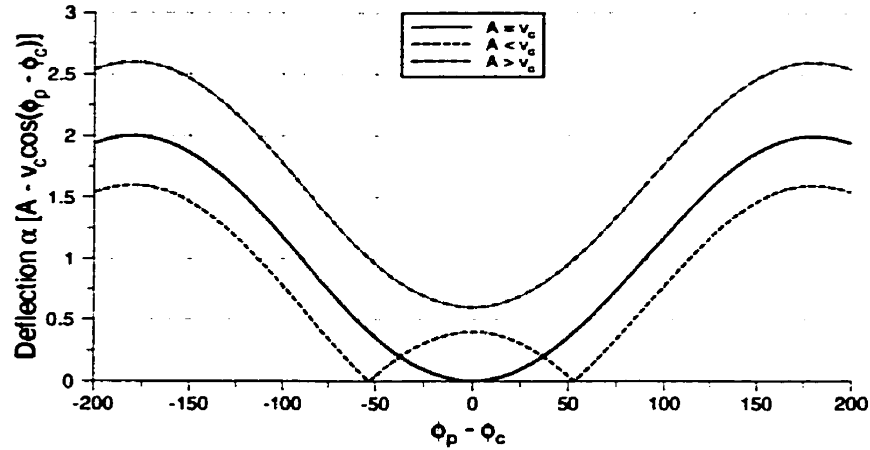


Figure 3.13: Relative cantilever deflection $|\Delta z|$ as a function of cantilever-circuit phase difference ϕ_p - ϕ_c for the cases of $A=V_c$. $A<V_c$, and $A>V_c$ [56].

In the case of $A>V_c$, the deflection is never nulled, and therefore, this case is not considered. When $A=V_c$, the deflection is only nulled when there is no cantilever-circuit phase difference. Since V_c is unknown originally, the remaining case $A<V_c$ is chosen. In this case, the deflection can be nulled at two distinct phase differences. The mean of these two is where ϕ_p-ϕ_c is zero. The two nulls can be located by scanning the phase ϕ_p, and the phase of the circuit signal is at the centre of these nulls. With the knowledge of ϕ_c, magnitude of $v_c(x,y,t)$ can be determined by setting $\phi_p=\phi_c$, and then adjusting the parameter A until the deflection is nulled.

In reality, the nulled value of A may not be exactly equal to the circuit magnitude V_c. This is due to cantilever mismatch which becomes a more significant issue at higher frequencies; though the value of A is off only by a linear scaling factor from V_c. A calibration curve measurement of V_c against A can be easily performed using a microstrip line [64].

3.6.2.2 Square Wave Modulation

Sinusoidal modulation is often very difficult to implement at radio frequencies (RF) for where square wave modulation becomes a more viable scheme. The cantilever signal used in square wave modulation is [64]:

$$v_p(t) = [A + KG_s(t)]\sin(\omega_0 t + \phi_p) \quad (3.30)$$

where A, K, and ϕ_p are controllable parameters. The term $A+KG_s(t)$ is a square wave with offset A and amplitude K. The term $G_s(t)$ is a unit square wave with a fundamental frequency of ω_r, and it has a Fourier series representation of:

$$G_s(t) = \frac{4}{\pi} \sum_{n=1,\,odd}^{\infty} \frac{1}{n}\cos(n\omega_r t) \,. \quad (3.31)$$

Substituting (3.31) into (3.2) gives a force with components at DC, ω_0, $2\omega_0$, $n\omega_r$, $\omega_0 \pm n\omega_r$, and $2\omega_0 \pm n\omega_r$. The cantilever deflection by the force at the resonance ω_r is:

$$\Delta z|_{w_r} = \frac{1}{2}\frac{\partial C}{\partial z} \cdot \frac{Q}{k} \cdot K \cdot \frac{4}{\pi}[A - V_c\cos(\phi_p - \phi_c)]\cos(\omega_r t) \quad (3.32)$$

The obtained expression in (3.32) is identical to that in (3.29) except for the factor $4/\pi$. Hence, the nulling algorithm discussed for sinusoidal modulation can be utilized without modifications to extract magnitude and phase of the circuit signal. Calibration curve measurement can be performed to compensate any discrepancies between A and V_c due to the mismatch by the tip of the cantilever at where it is modelled as an open circuit.

Figure 3.14 shows a block diagram of the square wave modulation implementation [63]. A high frequency source excites the circuit and triggers the probing signal $v_p(t)$. The phase shifter adjusts the parameter ϕ_p. The signal $v_p(t)$ is then modulated to the resonance of the cantilever, usually using a mixer. Matching circuitry is added to deal with any possible reflections that may be present in the probing signal. The vibrations of the cantilever by the electrostatic force are detected by a deflection sensor such as the beam-bounce detection system. The lock-in amplifier acts as a narrow bandpass filter at the resonance ω_r to allow reading of the cantilever deflections.

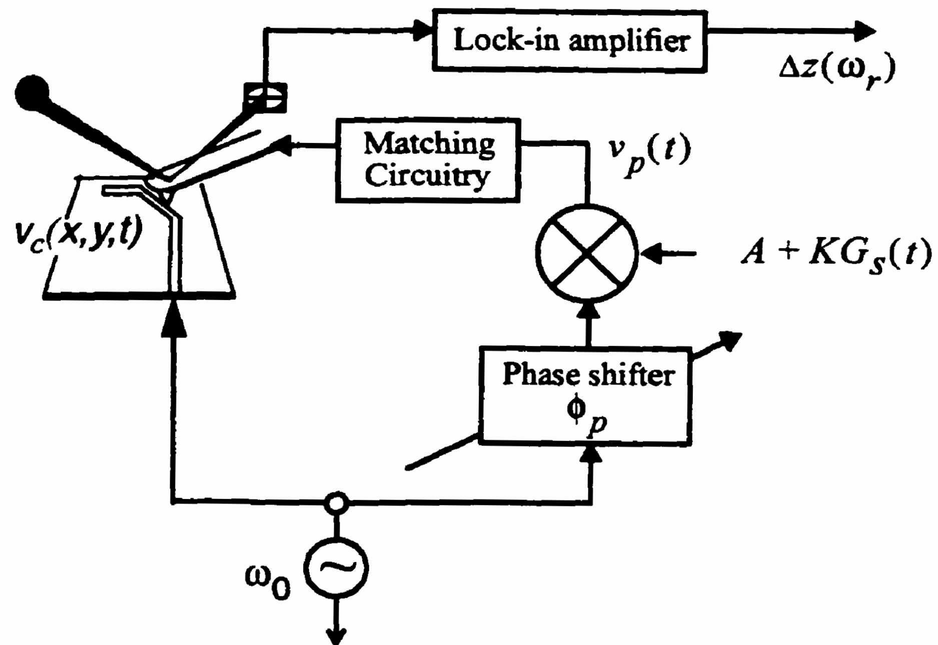


Figure 3.14: Implementation of the square wave modulation scheme for vector voltage measurement [63].

Chapter 4

Synchronous Time Domain Gating

This chapter introduces the methodology of synchronous time domain gating in conjunction with electrostatic force probing to permit arbitrary waveform sampling at high frequencies. The general implementation technique will first be expounded follow by the theoretical analyses and experimental realizations of the two special cases of synchronous time domain gating: amplitude and pulse width modulation.

4.1 Introduction

The methods for measuring magnitude and phase of DC and RF analog signals using electrostatic force probing were briefly reviewed in the section 3.6. In digital microelectronics, the waveshape, relative levels, voltage transitions, and delay characteristics of digital signals are often the major interests to be investigated besides exact signal magnitudes. Possible dynamic failure caused by those such as clock skew or power supply bounce in integrated circuits can considerably mutate the shapes and affect the latencies of digital signals. To enable detailed extraction of the desired features of a digital signal on an integrated circuit, the diagnostic instrument used must be able to perform measurements with a high bandwidth.

The EFM has been explored by test researchers so far as an instrument that can accomplish non-invasive internal diagnosis on passivated integrated circuits with high spatial and voltage resolution. As discovered in section 3.3.2, the EFM must comply to the frequency response of the cantilever. The cantilever deflection is maximum at its fundamental mechanical resonance which is typically in the kilohertz range. For probing signals on common microelectronic circuits in the range of megahertz or gigahertz, a sampling signal of the same frequency range must be sent to the cantilever to acquire proper measurements of the wanted circuit waveform. However, driving the cantilever at these frequencies which are much higher than the resonance results in a diminutive deflection. The EFM instrument becomes unfeasible at high frequencies without proper implementation.

A mixing concept was discussed in section 3.6.2 for conducting vector voltage measurements of high frequency sinusoidal signals. The technique is implemented by modulating the probing signal with a low frequency carrier using a mixer to accommodate the frequency response of the cantilever. In fact, this mixing idea has previously incorporated into EFM to perform measurements of high frequency analog [46,47,50,65,66] and digital signals [48,49,51,67,68,69]. These suggested techniques use the idea of frequency offset or amplitude mixing. In the frequency offset method, a high frequency circuit signal is sampled by a signal with a slight offset frequency, and the difference in frequency which is usually in the intermediate frequency (IF) range, is related to the harmonics of the resonance of the cantilever. In the amplitude mixing method, the high speed probing signal is modulated with an IF signal near or at the resonance of the cantilever using a high speed mixer. Both means presented in the associated literatures are subjected to many inconveniences such as tedious calibrations, low frequency noises, poor signal to noise ratio (SNR) when measuring long-bit patterns, and the requirement of expensive components.

Synchronous time domain gating is a generalized amplitude modulation based method to produce the proper signal at the cantilever and to allow electrostatic force sampling (EFS) of high frequency digital patterns at internal nodes of integrated circuits. The technique synchronizes the circuit stimulus and the sampling signal at the same frequency, and then modulates the high speed sampling signal at the resonance of the cantilever to enhance the deflections with relatively low cost time domain gating components such as ultra-wide-band switches, RF MUXs or high speed logic components. The bandwidth limitation of EFS becomes restricted only by the capabilities of the high speed pulse or step generators. In this thesis, two specific cases of synchronous time domain gating are implemented: amplitude and pulse width modulation. They will be expounded in section 4.3 and 4.4, respectively. The understanding of the technique will be presented next by explaining its general implementation.

4.2 Implementation Method

This section presents the implementation and analysis of synchronous time domain gating for EFS [70]. A block diagram of the measurement method is shown in figure 4.1. The operating principle of electrostatic force probing aforementioned in section 3.2 is uti-

lized. To summarize here, a conducting micromachined cantilever is placed at a small distance above a desired circuit test point. An electrostatic force is induced on the cantilever due to a potential difference between the cantilever signal $v_p(t)$ and the circuit waveform $v_c(x,y,t)$. The deflection of the cantilever Δz due to this force is sensed by the optical beam detection system.

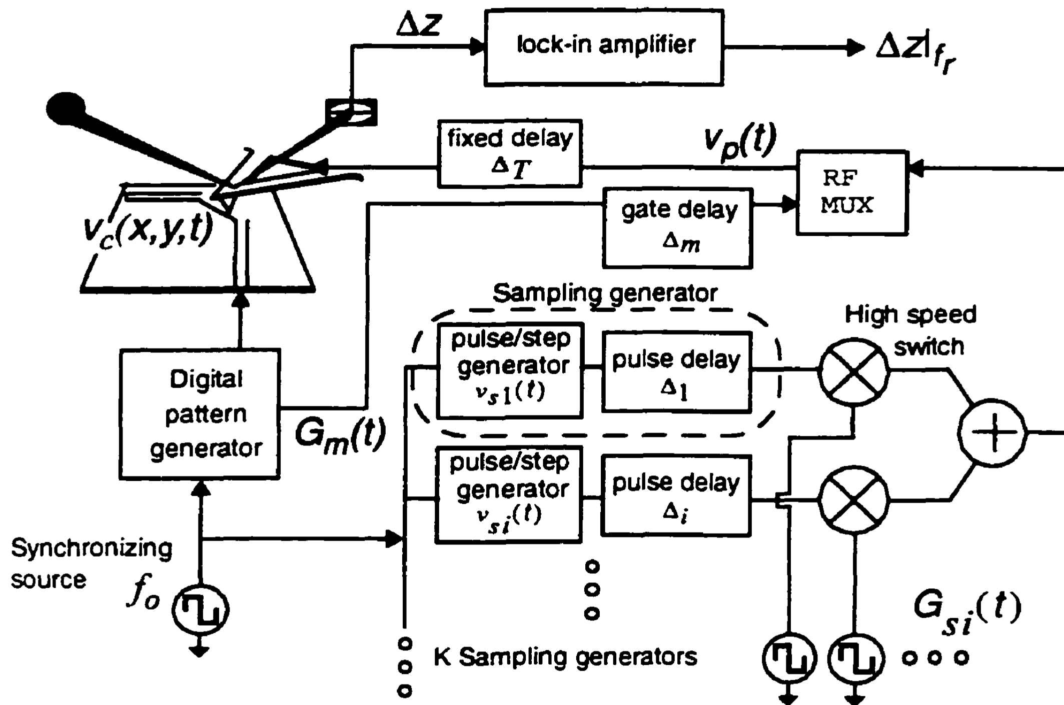


Figure 4.1: Block diagram of the general implementation for synchronous time domain gating [70].

The following is the description of the synchronous time domain gating realization for the production of a suitable sampling signal $v_p(t)$ to conform with the mechanical response of the cantilever. In figure 4.1, a synchronizing source at frequency $f_o=1/T$ drives a digital pattern generator which sends out a set of N_b-bit long test vectors with a bit rate $f_b=N_b/T$ to the circuit under test. The source at f_o also synchronously triggers a row of K sampling generators, each of these creates a signal $v_{si}(t-\Delta_i)$ where $i=1,2..K$, and Δ_i is an adjustable delay. These K waveforms are alternately selected at a lower frequency f_l using high speed switches with switch control signals $G_{si}(t)$. This modulating frequency f_l is chosen close to or at the mechanical resonance of the cantilever f_r to increase SNR. The K switches should

have a high bandwidth to allow high speed inputs, but their switching speeds do not have to be as fast since f_r is usually in the kilohertz range. The signals $v_{si}(t-\Delta_i)$, $i=1,2,..K$ are then summed together. The high frequency synchronizing source in figure 4.1 also triggers the digital vector generator to activate a gating signal $G_m(t)$ with a time delay Δ_m. Using a RF-MUX, the signal $G_m(t-\Delta_m)$ can be used to gate out in time domain the undesired components of the summation from the K high speed waveforms to form the desired sampling signal $v_p(t)$. In practice, various parts of the system in figure 4.1 can be realized through a single or combination of devices and components. Figure 4.2 displays some typical examples of $v_c(t)$, $v_{si}(t-\Delta_i)$, $G_m(t-\Delta_m)$ and $G_{si}(t)$.

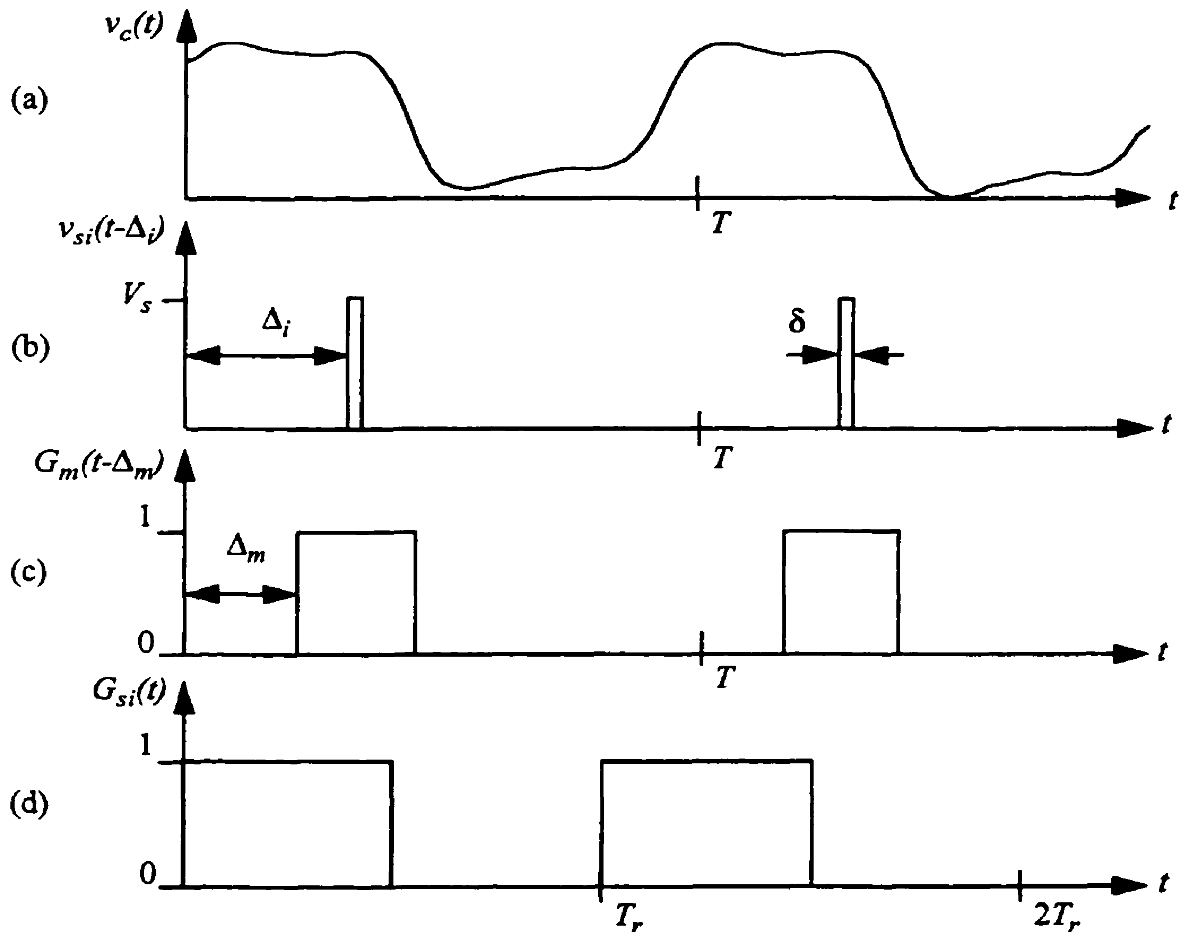


Figure 4.2: Sketches of some example waveforms in synchronous time domain gating: (a) circuit signal $v_c(t)$, (b) sampling generator signal $v_{si}(t-\Delta_i)$, (c) gate signal $G_m(t-\Delta_m)$, and (d) switch control signal $G_{si}(t)$. The synchronizing source frequency is $f_o=1/T$, while the modulating frequency is the fundamental resonance of the cantilever, $f_r=1/T_r$

Since the cantilever does not insert a large load onto the circuit, the end of the cantilever can be modelled as an open circuit. An optional fixed delay Δ_T can be applied to $v_p(t)$ for matching against possible multiple signal reflections in case that the RF-MUX does not fully absorb the reflection of the sampling signal from the open-ended cantilever.

Neglecting Δ_T, the signal at the cantilever, $v_p(t)$, can be expressed mathematically as [70]:

$$v_p(t) = \left(\sum_i^K v_{si}(t-\Delta_i) G_{si}(t)\right) G_m(t-\Delta_m) \tag{4.1}$$

where the control signal $G_{si}(t)$ is usually a square wave with its fundamental frequency chosen at the resonance of the cantilever, f_r, a 50% duty cycle, and only two phases $(0,\pi)$, represented by s_i [70]:

$$G_{si}(t) = \frac{1}{2} + s_i\left(\frac{2}{\pi} \sum_{n=1,\,odd}^{\infty} \frac{1}{n}\sin(n\omega_r t)\right) \ , \ s_i \in \{1,-1\} \ , \ \omega_r = 2\pi f_r . \tag{4.2}$$

Combining (4.2) and (4.1), $v_p(t)$ can be written as follows:

$$\begin{aligned} v_p(t) = &\left(\frac{1}{2}\sum_i^K v_{si}(t-\Delta_i)\right. \\ &\left. + \sum_i^K s_i v_{si}(t-\Delta_i)\frac{2}{\pi} \sum_{n=1,\,odd}^{\infty} \frac{1}{n}\sin(n\omega_r t)\right) G_m(t-\Delta_m) \end{aligned} . \tag{4.3}$$

Recalling that (3.2) is the electrostatic force that includes the DC offset effects $\Delta\Phi(x,y)$. This force can also be expressed as:

$$\begin{aligned} F_z = &\frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)(v_p^2(t) + v_c^2(x,y,t) - 2v_p(t)v_c(x,y,t) \\ &+ 2v_p(t)\Delta\Phi(x,y) - 2v_c(x,y,t)\Delta\Phi(x,y) + \Delta\Phi^2(x,y)) \end{aligned} . \tag{4.4}$$

Lets expand the terms in (4.4) at $\omega_r = 2\pi f_r$ by substituting (4.3) into it:

$$v_p{}^2(t)\big|_{\omega_r} = \left\langle\left(\sum_i^K v_{si}(t-\Delta_i)\sum_i^K s_i v_{si}(t-\Delta_i)\right) G_m^2(t-\Delta_m)\right\rangle \frac{2}{\pi}\sin(\omega_r t) \tag{4.5}$$

$$v_p(t)v_c(x,y,t)\big|_{\omega_r} = \left\langle\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right) G_m(t-\Delta_m) v_c(x,y,t)\right\rangle \frac{2}{\pi}\sin(\omega_r t) \tag{4.6}$$

$$v_p(t)\Delta\Phi(x,y)|_{\omega_r} = \Delta\Phi(x,y)\langle\sum_i^K s_i v_{si}(t-\Delta_i)G_m(t-\Delta_m)\rangle\frac{2}{\pi}\sin(\omega_r t) \quad (4.7)$$

where $\langle x(t)\rangle$ is the DC component of $x(t)$, or an average of $x(t)$ over its period T:

$$\langle x(t)\rangle = \frac{1}{T}\int_0^T x(t)dt\ . \quad (4.8)$$

Notice that also $v_c(x,y,t)\Delta\Phi(x,y)$, $v^2_c(x,y,t)$, and $\Delta\Phi^2(x,y)$ have no components at ω_r. Using (4.5) through (4.7), the force on the cantilever in (4.4) at the monitored frequency ω_r is:

$$\begin{aligned} F_z|_{\omega_r} = \frac{\partial}{\partial z}C(x,y,z)\Bigg\{&\langle\left(\sum_i^K v_{si}(t-\Delta_i)\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m^2(t-\Delta_m)\rangle \\ &-2\langle\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m(t-\Delta_m)v_c(x,y,t)\rangle \\ &+2\Delta\Phi(x,y)\langle\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m(t-\Delta_m)\rangle\Bigg\}\frac{1}{\pi}\sin(\omega_r t)\end{aligned} \quad (4.9)$$

Although (4.9) is a complicated expression, the first and third terms are independent of the desired circuit voltage $v_c(x,y,t)$. For extracting waveshapes of digital signals only, these terms contribute an offset voltage as they are constant terms at ω_r. For simplicity, these terms can be manipulated and lumped together to form a term called A which depends on the capacitance $C(x,y,z)$, the characteristics of the sampling signal, the DC offset effects $\Delta\Phi$, and the gating signal $G_m(t-\Delta_m)$.

By carefully examining the inner product that contains the circuit signal $v_c(x,y,t)$ in (4.9):

$$\begin{aligned}&\langle\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m(t-\Delta_m)v_c(x,y,t)\rangle \\ &= \int_0^T\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m(t-\Delta_m)v_c(x,y,t)dt\end{aligned}, \quad (4.10)$$

it can be observed that the force at ω_r is in fact a convolution between the effective sampling signal $\left(\sum_i^K s_i v_{si}(t-\Delta_i)\right)G_m(t-\Delta_m)$ and the circuit signal $v_c(x,y,t)$, if Δ_i is a varia-

ble. This observation promotes the following simplification to further comprehend the technique. If $\left(\sum_{i}^{K} s_i v_{si}(t-\Delta_i)\right) G_m(t-\Delta_m)$ is a train of sharp rectangular sampling pulses with amplitudes of V_s, a pulse width of $\delta << T$, and each pulse having infinite rise and fall times identical to that in figure 4.2(b), then (4.10) becomes:

$$\left\langle \left(\sum_{i}^{K} s_i v_{si}(t-\Delta_i)\right) G_m(t-\Delta_m) v_c(x, y, t) \right\rangle \approx \frac{\delta}{T} V_s v_c(x, y, t = \Delta) \qquad (4.11)$$

where Δ is the initial delay of the sampling signal $\left(\sum_{i}^{K} s_i v_{si}(t-\Delta_i)\right) G_m(t-\Delta_m)$. The expression for the magnitude of the cantilever deflection at ω_r using the above assumptions and (3.8) can be written as:

$$\Delta z|_{\omega_r} = -\frac{\partial}{\partial z} C(x, y, z) \frac{2}{\pi} \frac{Q}{k} \frac{\delta}{T} V_s V_c(x, y, t = \Delta) + A \qquad (4.12)$$

where A, as defined earlier, is a constant deflection at ω_r, and is independent of the circuit voltage $v_c(x,y,t)$. Measurement of the deflection at ω_r can be accomplished using a lock-in amplifier as presented in figure 4.1. As Δ is scanned over the entire period T, the monitored deflection magnitude changes proportionally to the circuit voltage $v_c(x,y,t)$, thereby permitting waveform extraction. Since Δ is subjected to the sampling generator signals $v_{si}(t-\Delta_i)$ and the gate signal $G_m(t-\Delta_m)$, the sweeping of Δ requires the delays Δ_i and Δ_m to be synchronously scanned across the period T.

Note that when calculating the deflection in (4.12), it must be realized that V_s should in fact be two times the amplitude of the sampling pulse because it is an open circuit at the end of the cantilever, assuming that precautions for multiple reflections are taken into consideration. The forward wave of the sampling signal adds onto the reflected to double the signal amplitude at the end of the cantilever.

To extract the circuit waveform with the proper polarity, it is important to realize the several factors that affect the polarity of the measurements: the polarity of the sampling pulse, and the phase of the signal at the synchronized frequency set by the lock-in amplifier. It should also be noticed that the capacitance derivative in (4.12) is negative.

If the absolute voltages of the circuit signal $v_c(x,y,t)$ are not required, the DC offset effects and the rest of the contributing factors in A become unimportant. This means that calibrations for determining the loading capacitance and DC offset effects are unnecessary for circuit pattern or waveshape extraction. However, this also implies that expensive electronics are needed for calibration when absolute voltages of $v_c(x,y,t)$ are desired. This thesis only concerns with measuring signal transistion times, propagation delays, overshoots and other ringing effects of digital signals.

By employing synchronous time domain gating to generate a suitable $v_p(t)$ for high frequency EFS, the bandwidth of the instrument is no longer restricted by the frequency response of the cantilever, but only by the sharpness and non-idealities in the sampling signal. In reality, the approximation that the effective sampling signal $\left(\sum_{i}^{K} s_i v_{si}(t-\Delta_i)\right) G_m(t-\Delta_m)$ is a train of prefect rectangular pulses similar to that in figure 4.2(b) is often void due to the non-ideal electronics that produce these pulses. To accurately examine the effects of these non-idealities on the measurements, a convolution between the circuit signal and the effective sampling pulse signal should be performed to yield a predicted waveform of the cantilever deflections.

4.3 Amplitude Modulation

Various modulation schemes can be realized using the general implementation in figure 4.1 by choosing the quantity of the sampling generators K, and the waveshapes of $v_{si}(t-\Delta_i)$ created by each of these sampling generators. One of the special cases of synchronous time domain gating is pulse amplitude modulation in which K=2, $v_{s1}(t)=v_a(t)$, and $v_{s2}(t)=0$. Though, this is commonly implemented with K=1 by modulating $v_{s1}(t)$ at the cantilever resonance using a high speed switch. The idea of this technique is analogous to a conventional repetitive sampling oscilloscope, except that the sampling is accomplished directly at the tip of the cantilever. For high speed sampling, $v_a(t)$ is desired to be a train of narrow pulses similar to that in figure 4.2(b). There exist several techniques for producing high speed narrow width pulses. Prior to discussing some of the popular means for gener-

ating these sampling pulses, including the realization assembled in this thesis, a conceptual explanation through the mathematics of amplitude modulation is next.

4.3.1 Theory

The two sampling generator signals $v_{s1}(t-\Delta_1)$ and $v_{s2}(t)=0$ are periodically chosen at the frequency f_r using a high speed switch with control signals $G_{si}(t)$, $i=1,2$, $s_1=1$, $s_2=-1$. Assuming an all pass gate signal $G_m(t)=1$ and a delay $\Delta_T=0$, the probing signal $v_p(t)$ in (4.1) becomes:

$$v_p(t) = v_a(t-\Delta_1)G_{s1}(t) = v_a(t-\Delta)\left(\frac{1}{2}+\frac{2}{\pi}\sum_{n=1,odd}^{\infty}\frac{1}{n}\sin(n\omega_r t)\right) . \quad (4.13)$$

Figure 4.3 illustrates a plot of the sampling signal $v_p(t)$. The signal can be simply interpreted as the multiplication product of a high speed pulse train $v_a(t-\Delta)$ with a low frequency carrier signal $G_{s1}(t)$. The pulse train signal only appears for half of the modulating period $T_r=1/f_r$, while the other half is zero. For a modulating frequency $f_r=13KHz$, there are $N_r=0.5*T_r/T=4808$ sampling pulses if the period T is $8ns$, which is typical in the high frequency measurements in this work.

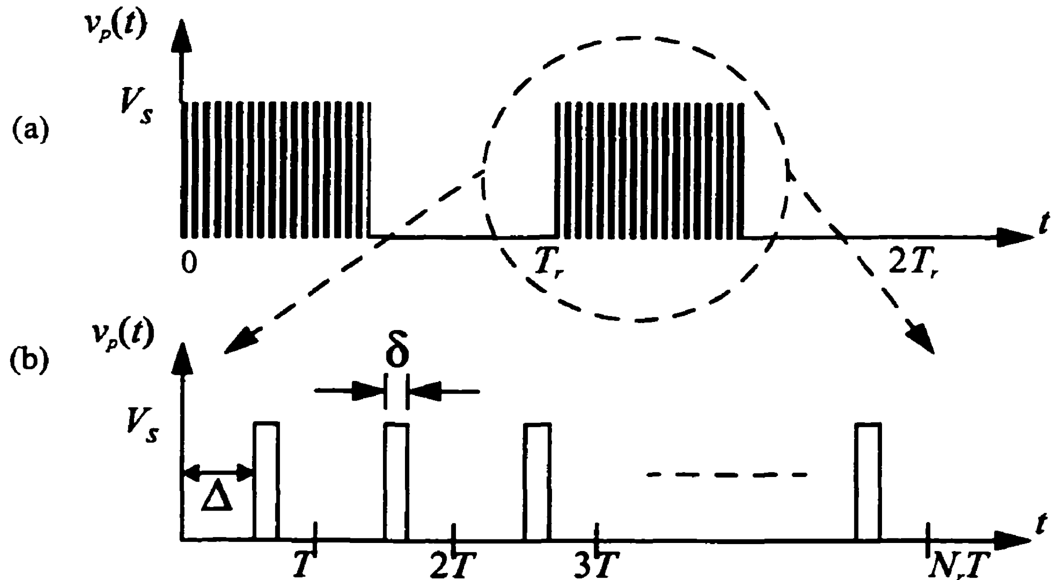


Figure 4.3: (a) The sampling signal $v_p(t)$ in amplitude modulation. (b) A zoom-in version of $v_p(t)$ revealing the sampling pulse train.

According to (4.9) and (3.8), the deflection of the cantilever at its resonance frequency $\omega_r=2\pi f_r$ due to the probing signal in (4.13) is:

$$\Delta z|_{\omega_r} = \frac{\partial}{\partial z}C(x,y,z)\frac{Q}{k}\left\{\frac{1}{2}\langle v_a^2(t-\Delta)\rangle - \langle v_a(t-\Delta)v_c(x,y,t)\rangle + \Delta\Phi(x,y)\langle v_a(t-\Delta)\rangle\right\}\frac{2}{\pi}\sin(\omega_r t) \quad (4.14)$$

The waveform of this deflection magnitude can be anticipated by convoluting the sampling pulse in $v_a(t-\Delta)$ and the circuit signal $v_c(x,y,t)$. When the effective sampling pulse $v_a(t-\Delta)$ is a sequence of ideal rectangular sampling pulses with the same features as those in figure 4.3(b), the mathematical expression of the deflection is exactly as (4.12).

4.3.2 Narrow Pulse Generation

Pulse generators are used to produce the high speed pulse train $v_a(t-\Delta)$ in amplitude modulation. The idealities of the effective sampling pulses, and in turn the bandwidth of EFS with synchronous time domain gating seriously depends on the performance of these pulse generators. This section is dedicated to a few popular pulse generators and techniques for generating narrow width pulses for sampling.

4.3.2.1 Vector Generator

Commercial high speed vector generators are capable of producing bit rates in the range of *Gb/s*. These sources can generate pulses with widths about a few hundreds of picoseconds. The vector generator used in this thesis was the multi-channel 1*GHz* HP80000 data generator from Hewlett-Packward which is capable of producing 1*ns* width pulses with 10-90% rise and fall times of less than 150*ps* [70]. However, to be compatible with the speed of many commercial microelectronics, pulses with widths in the picosecond range are preferred. This data generator was used as the synchronizing source for generating excitations for the test circuit and the pulse generation systems in this work.

Vector generators that produce sharper pulses are commercially available but they are expensive (>$100K). Since cost is usually an immediate factor to be considered, pulse generation is usually accomplished by other means.

4.3.2.2 Transmission Line Filter

High pass filters are perhaps the most economical solution for sharp pulse generation because they can be simply made of 50Ω transmission lines [72]. Figure 4.4 shows the filter designed and constructed using 50Ω coplanar transmission lines [73] for this thesis. The filter was built by placing two short-circuited 50Ω coplanar stubs at the same location of another 50Ω coplanar line, thus forming a cross-shaped circuit as depicted in the figure. The stub lengths can be varied by taping pieces of copper onto the stub lines as short circuit terminations at any locations. This method allows the optimum pulses to be experimentally and quickly determined to escape complicated simulations of the filter.

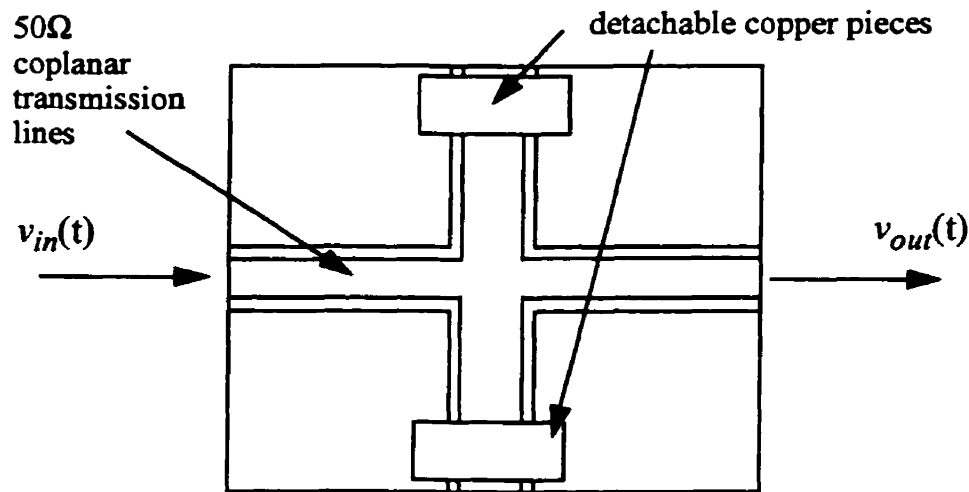


Figure 4.4: The transmission line filter for narrow pulse generation constructed in this thesis. Two detachable copper pieces are used to search for the corresponding stub lengths to optimise the output pulses v_{out}(t).

Once the optimum stub lengths are found, the output v_{out}(t) should be a derivative of the input v_{in}(t). By applying a relatively wide pulse with finite rise and fall times into the filter, two narrower pulses with opposite polarities at the transition points of the input is formed at the output. The widths of these output pulses are dictated by the sharpness of the input signal transitions. The extra unwanted pulse can be eliminated using a RF-MUX with a proper gate signal $G_m(t-\Delta_m)$.

It was found that the best length for both stubs is the same as half the length of the transmitting 50Ω coplanar line. Figure 4.5 shows the signals associated with the filter above for pulse generation.

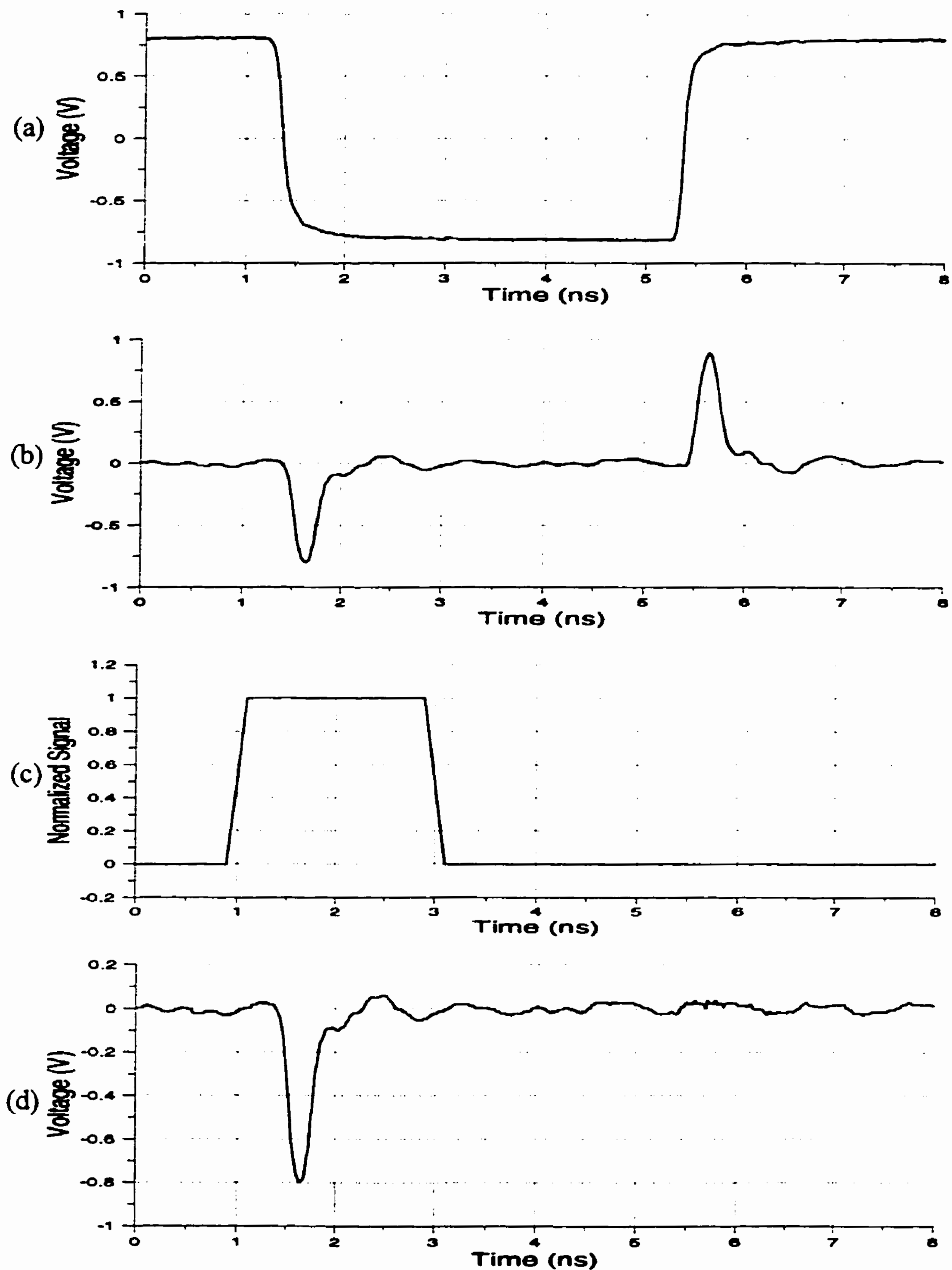


Figure 4.5: (a) An input to the transmission line filter in figure 4.4, v_{in}(t); (b) output of the filter, v_{out}(t); (c) sketch of the gate signal $G_m(t\text{-}\Delta_m)$ for gating out the undesired pulse; and (d) the desired sampling pulse.

The filter input signal in figure 4.5(a) is a 4*ns* pulse generated by the HP80000 data generator. A DC-5*GHz* RF-MUX was employed to gate out the extra pulse from the dual pulse signal in figure 4.5(b) with a gate signal $G_m(t\text{-}\Delta_m)$ sketched in figure 4.5(c). The actual logic levels of the gate signal into the MUX was 0 and 2.25*V* (4.5*V* at the switching logic input at where it is an open circuited load) [74]. A DC-20*GHz* Tektronic 11801B digital sampling oscilloscope which was utilized throughout this thesis, was used to capture the signals in figure 4.5(a), (c), and (d). The pulse has an amplitude of 800*mV*, and a full width at the half amplitude, or full width half maximum (FWHM) of 250*ps*. The magnitude of the pulse is mostly determined by the filter input signal level and losses introduced by the RF-MUX. This type of pulse generator was not utilized for any measurements in this work, but was used in [56] and [63].

4.3.2.3 Non-Linear Transmission Line

A non-linear transmission line [75] is an ordinary transmission line with the addition of a non-linear element to purposely distort the input signal of the line. For fast pulse generation, a non-linear transmission line is realized by placing varactor diodes periodically in shunt with a transmission line. Figure 4.6 shows a single section of this non-linear transmission line.

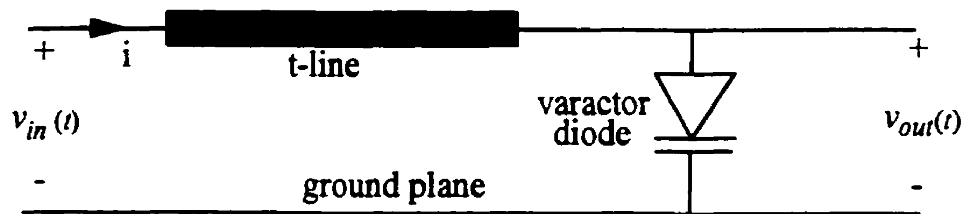


Figure 4.6: A single section of a non-linear transmission line for high speed pulse generation.

Since a varactor diode behaves as a voltage dependent capacitor [76], these diodes in a non-linear transmission line cause the capacitance of the original transmission line to be a function of input voltage. Because the phase velocity of the line γ_{ph} is affected by the line capacitance, γ_{ph} also becomes a function of voltage V:

$$\gamma_{ph}(V) = \frac{1}{\sqrt{L_l C_l(V)}} \tag{4.15}$$

where L_l and C_l denotes the total inductance and capacitance of the non-linear transmission line, respectively, and V is the instantaneous voltage of an analog input signal $v_{in}(t)$.

The capacitances of the varactor diodes rise and drop in concert with the input voltages. According to (4.15), the phase velocity of the line should therefore be higher when the input voltage is large. Reversely, a lower input voltage slows down the phase velocity. With a time-varying input, the higher instantaneous voltages in the signal travel faster down the non-linear transmission line than the lower instantaneous voltages. Using a sinusoid as an input, a non-linear transmission line can compress the input sine wave and develop unbalanced transitions at the output as displayed in figure 4.7 [77,78].

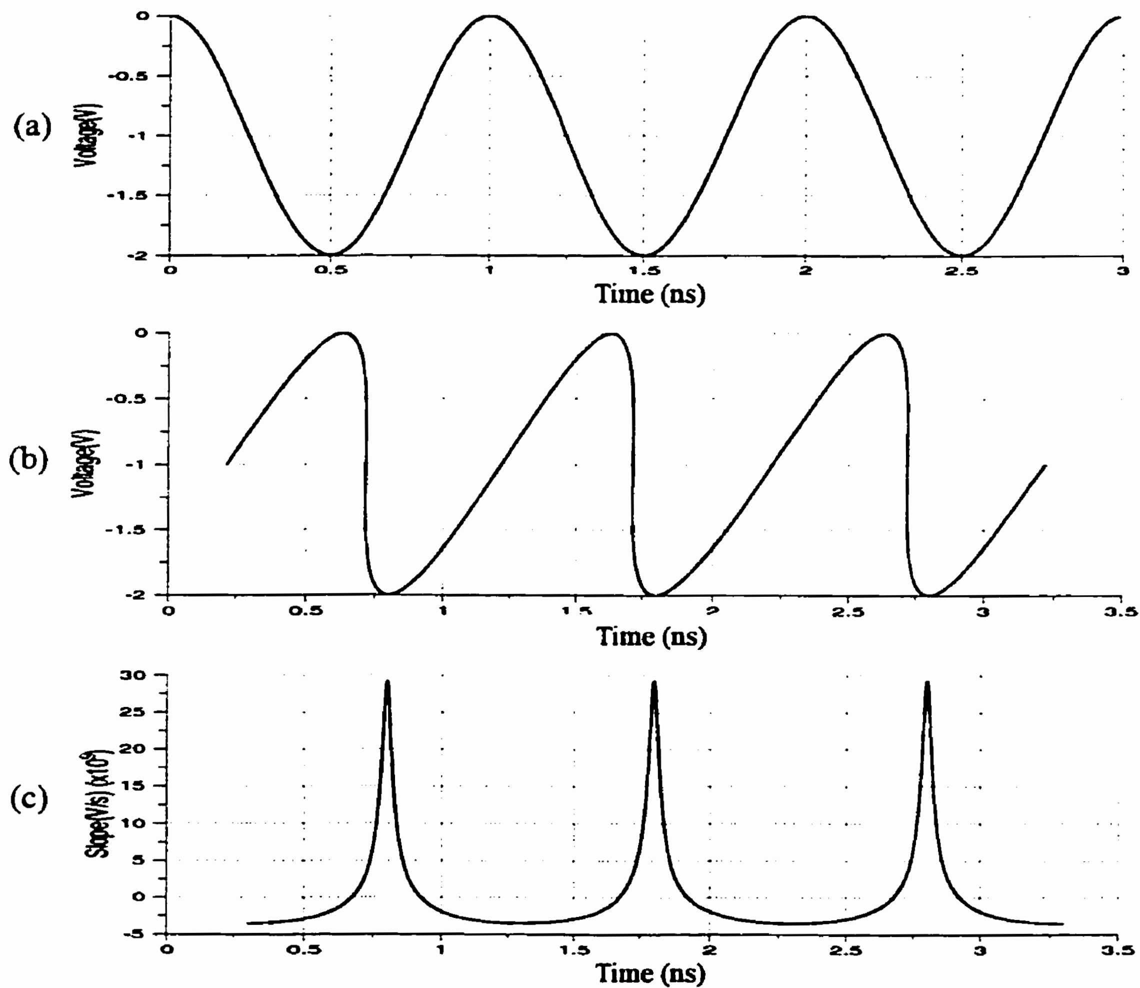


Figure 4.7: Simulations of input and output waveforms of a non-linear transmission line for fast pulse generation: (a) a $1GHz$ sinusoidal input, (b) distorted sine wave at the output with sharp transitions at the falling edges, and (c) narrow periodic pulses yielded after differentiating the output waveform in (b) [78].

A narrow pulse generator can be formed by adding a differentiator such as a high pass filter at the output of the non-linear transmission line. Figure 4.7(c) shows the pulses obtained by taking a derivative of the output signal in figure 4.7(b). The generator can be implemented on a printed circuit board or fabricated on a substrate as an integrated circuit.

4.3.2.4 Step Recovery Diode

Like the non-linear transmission line, a few other pulse generators utilize non-linear elements to produce narrow width pulses from a sinusoidal input. One of the often used non-linear components is a step recovery diode (SRD) which acts as a charge storage diode [79]. The capacitance of the SRD is large under forward bias and is small under reverse bias. Hence, the SRD stores charge during the positive half cycle of a sine wave input, and a negative current produced by the negative half cycle of the input discharges the SRD before it accumulates charge again. The rate of discharge for the SRD is quite high, thereby forming a fast step typically of only picoseconds. This transition time is defined by the *RC* time constant of the SRD, where *R* is the parasitic resistance, and *C* is the reverse bias capacitance. Figure 4.8 shows the ideal response of the SRD under a sine wave excitation.

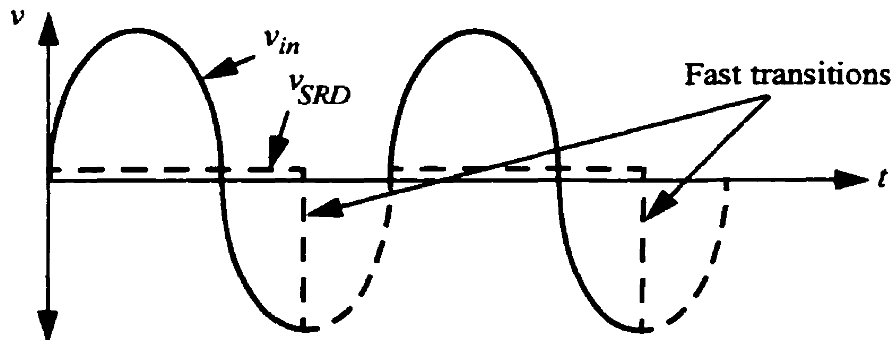


Figure 4.8: The output of an ideal step recovery diode due to an input sine wave.

An impulse generator can be built by adding a matched filter network and a DC return to a SRD as depicted in figure 4.9. The filter network is used to match a 50Ω source drive, while the DC return is for providing a self-biasing return current for the SRD. Figure 4.10 shows a sketched output of the impulse generator. The matching network is resonant at a specific frequency and thus, the repetition rate, f_{in}, is fixed which may cause difficulties

when this is used to sample a signal with an arbitrary period. Commercial impulse generators are available among which the bandwidth can be up to $50GHz$ [79].

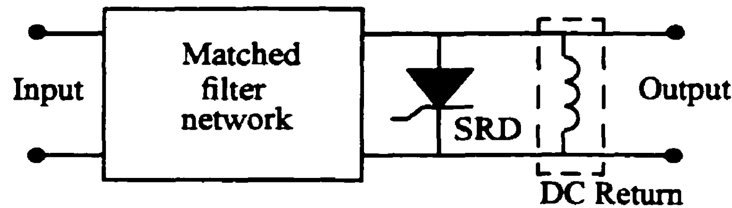


Figure 4.9: An example of an impulse generator made with a step recovery diode.

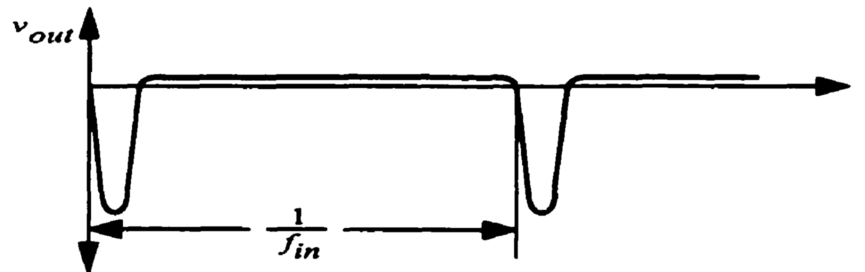


Figure 4.10: Sketch of a typical output waveform of an impulse generator in figure 4.9. The pulse periodically repeats at the frequency of the input sine wave, f_{in}.

4.3.2.5 High Speed Logic Switches

Pulse generation can simply be achieved by a single high speed digital switch or an AND/NAND logic circuit. A wide variety of these devices can be purchased at reasonable prices. Although the switch and the AND logic circuit distinctively have their own array of applications, there exists a common arrangement of input signals when using these devices for pulse generation. Figure 4.11 shows the production of narrow pulses using switching circuitry. All sketched signals in this figure are ideal for demonstration here.

The device in figure 4.11(a) can be a digital switch/MUX or an AND logic circuit. For a digital switch, v_{sw1} is one of the high speed input terminals to the device. The input port to the switch driver is represented by S_{cntl}, and v_{com} is the common signal output port of the switch. In a typical two-input switch, two high speed inputs at v_{sw1} and v_{sw2} are enabled or disabled at the output port v_{com} by the signal at S_{cntl}. For instance, v_{sw1} is selected when the logic level of S_{cntl} is high, and v_{sw2} is chosen when S_{cntl} is logic low. The input to the switch driver at S_{cntl} dictates the turn on duration time of the switch inputs. By supply-

ing the specific synchronized input signals v_{in1} and v_{in2}, as exemplified in figure 4.11, fast pulses can be generated at v_{com}. The pulse widths or duty cycles of the inputs δ_{in1} and δ_{in2} are rather trivial as the only significant factor is the delay τ_a between v_{in1} and v_{in2}. Assuming the inputs have infinite rise and fall times, the width of the generated ideal pulse v_{out} at v_{com} is δ_{in1}-τ_a. The actual rise and fall times of the output pulse are mostly governed by the transistion speed of the switch control circuitry. The transistion times of the output should not depend on the rise and fall times of the switch input signals because the switch triggers at a specific threshold between the high and low logic levels of the control signal at S_{cntl}. However, jitter from the source generator and the switch circuitry may affect the transistion times of generated pulse.

If the device in figure 4.11(a) is a two-input AND logic circuit, then v_{AND1} and v_{AND2} are the two inputs ports of the logic gate. Since the AND logic function states that its output is logic high only when both of its inputs are logic high, the delay τ_a can be adjusted so that the time during both inputs are high is very short for fast pulse production. The ideal width of the pulses produced at v_{AND} by the gate is δ_{in1}-τ_a. The bandwidth of the resulted pulse is solely determined by the device because the transistion time of the generated signal v_{out} is conditional on the switching speed of the circuit. A commercial logic AND gate is usually equipped with a complementary logic output v_{NAND}, giving the circuit AND and NAND functions for versatility. Either ports can be chosen as the output for pulse generation, but the unselected output port is usually match terminated to avoid possible reflections.

An 8*Gb/s* two-input AND/NAND circuit (NL4519-2) was purchased from NEL [80], and utilized as a pulse generator in this thesis. The circuit was fabricated with 0.5μm GaAs MESFETs. The circuit has a high logic level of 0*V*, a low logic level of -0.9*V*, and it is specified to have both rise and fall times of typically 65*ps* (maximum 95*ps*). It requires a bias supply of -3.7*V*, and its threshold switching level was set to be -0.5*V* using an external voltage divider. The chip was mounted on a low-loss printed circuit board which has a dielectric constant ε_r=10.8, and a thickness of 0.64*mm*. The high speed input/output pins were soldered onto 50Ω microstrip lines [62] which eventually connect to 50Ω SMA semi-rigid coaxial cables for signal transfer in and out of the chip. Capacitors of 1*nF* were

added in shunt with the bias supply lines to divert possible AC signals exist in the DC supply for reducing power supply fluctuations. Figure 4.12 shows a photograph of the mounted chip.

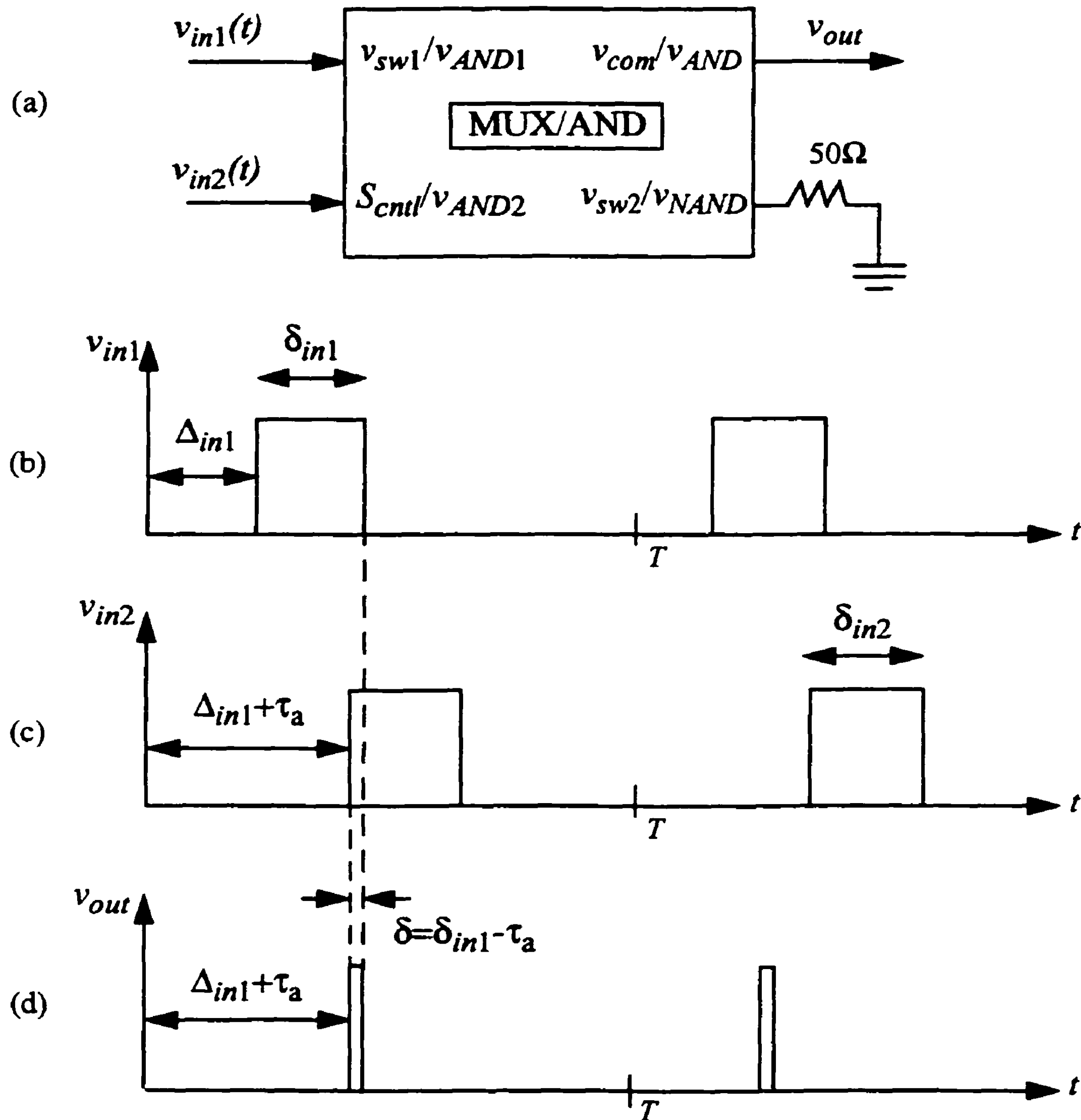


Figure 4.11: Designations of input and output signals for a switch/AND circuit for generating fast pulses. (a) A device which can be a digital switch/MUX or an AND logic circuit; (b) input signal v_{in1}; (c) input signal v_{in2}; and (d) output of the device v_{out}. δ_{in1} and δ_{in2} denotes the pulse widths of the input signals v_{in1} and v_{in2}, respectively. The time delay between v_{in2} from v_{in1} is τ_a. The width of the output pulse is $\delta=\delta_{in1}-\tau_a$. Other high speed input/output ports of the device in (a) are 50Ω match terminated. All example signals are synchronized, and has a period T.

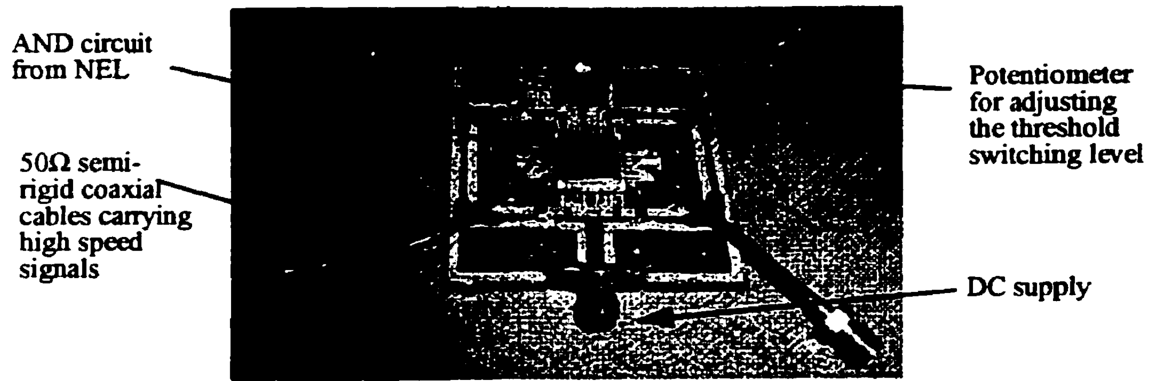


Figure 4.12: Photograph of the 2-input AND/NAND gate from NEL mounted on a low-loss printed circuit board.

The HP80000 data generator was used to supply a 125*MHz* signal with 1*ns* pulses at an amplitude of -1.25*V* into a sampling generator containing the NEL logic gate in figure 4.12 as displayed in figure 4.13. In general, the repetition frequency of the outputs by the HP generator to the sampling generator can be set at any values between 8*MHz* to 500*MHz*. A simple BNC splitter and cables with different designated lengths were utilized to obtain a delay τ_a of 840*ps* between the two input signals v_{in1} and v_{in2} which are displayed in figure 4.14(a). The reflections caused by the splitter is not a concern since both input ports of the logic circuit and the output terminals for each channel of the HP generator have 50Ω terminations.

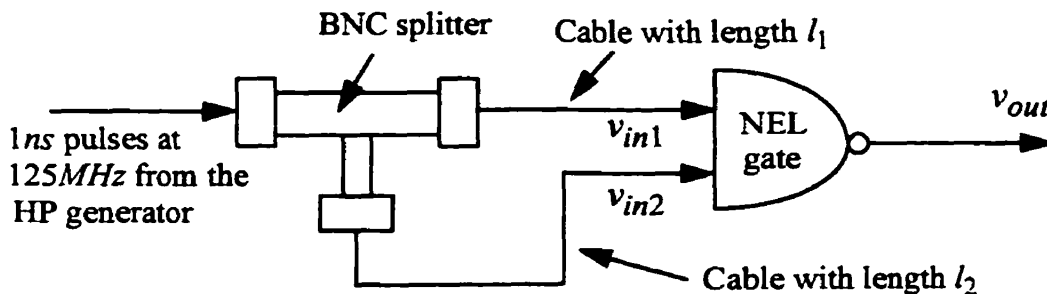


Figure 4.13: The sampling generator constructed for amplitude modulation using the 8*Gb/s* AND/NAND gate from NEL. Specified cable lengths l_1 and l_2 are used for a suitable delay τ_a between v_{in1} and v_{in2}.

The output of the NEL gate, which was taken from the NAND logic output of the circuit was measured using the DC-20*GHz* Tektronic 11801B digital sampling oscilloscope.

The output measured has an amplitude of 1*V*, a FWHM of 120*ps*, and rise and fall times (10-90%) of 78*ps* and 84*ps*, respectively, was as exhibited in figure 4.14(b). Both transition times of the output falls under the expected maximum of 95*ps* [80].

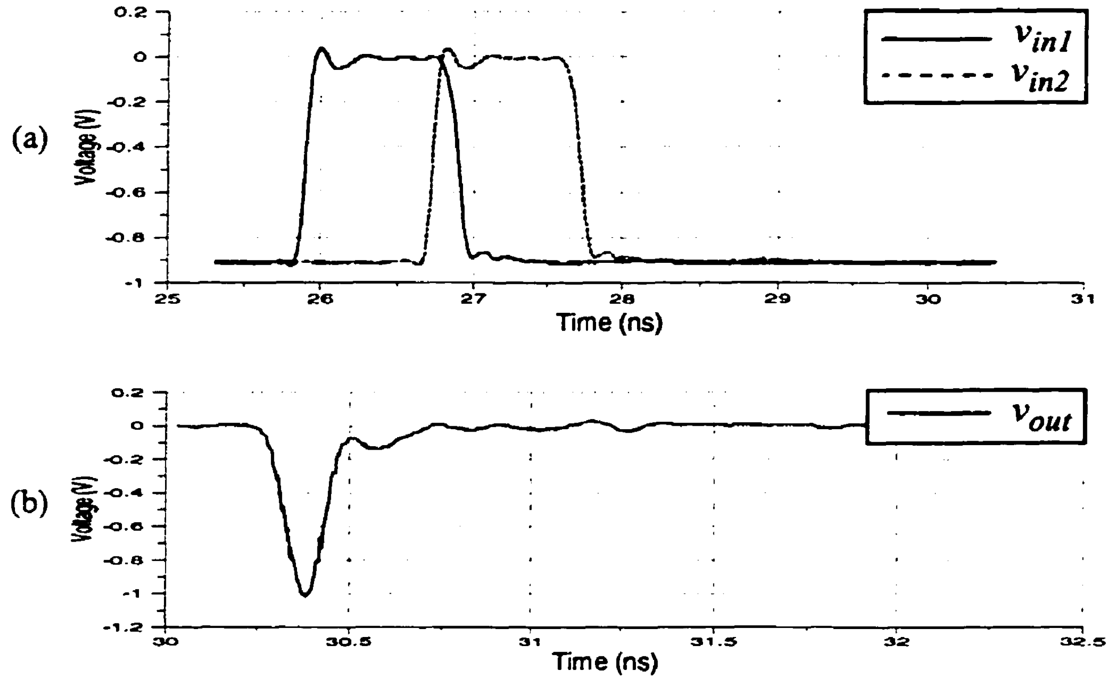


Figure 4.14: (a) Input and (b) output signals of the 8*Gb/s* AND/NAND gate from NEL.

4.3.3 Experimental Implementation

This section describes the implementation of the amplitude modulation technique that is undertaken in this thesis. To produce the proper probing signal for EFS using amplitude modulation, the arrangement of the utilized components as displayed in figure 4.15 was cultivated.

The HP80000 data generator was used as the synchronizing source which has four output channels. Two channels provided the test circuit pattern $v_c(t)$ and the triggering signal to the DC-20*GHz* Tektronic 11801B digital sampling oscilloscope for monitoring the sampling signal $v_p(t)$, respectively. The remaining two channels of the HP generator were inputs to the synchronous gating system for generating $v_p(t)$. The delays, magnitude and logic patterns of the generator output signals were defined and controlled by a computer program using a general purpose interface board (GPIB) [81]. The software automates the

experiment by monotonically scans the associated signal delays for sampling. This program is part of the measurement system used in this work that will be described in further detail in section 6.1. The generator has a maximum delay range of $2ns$ with a resolution of $2ps$.

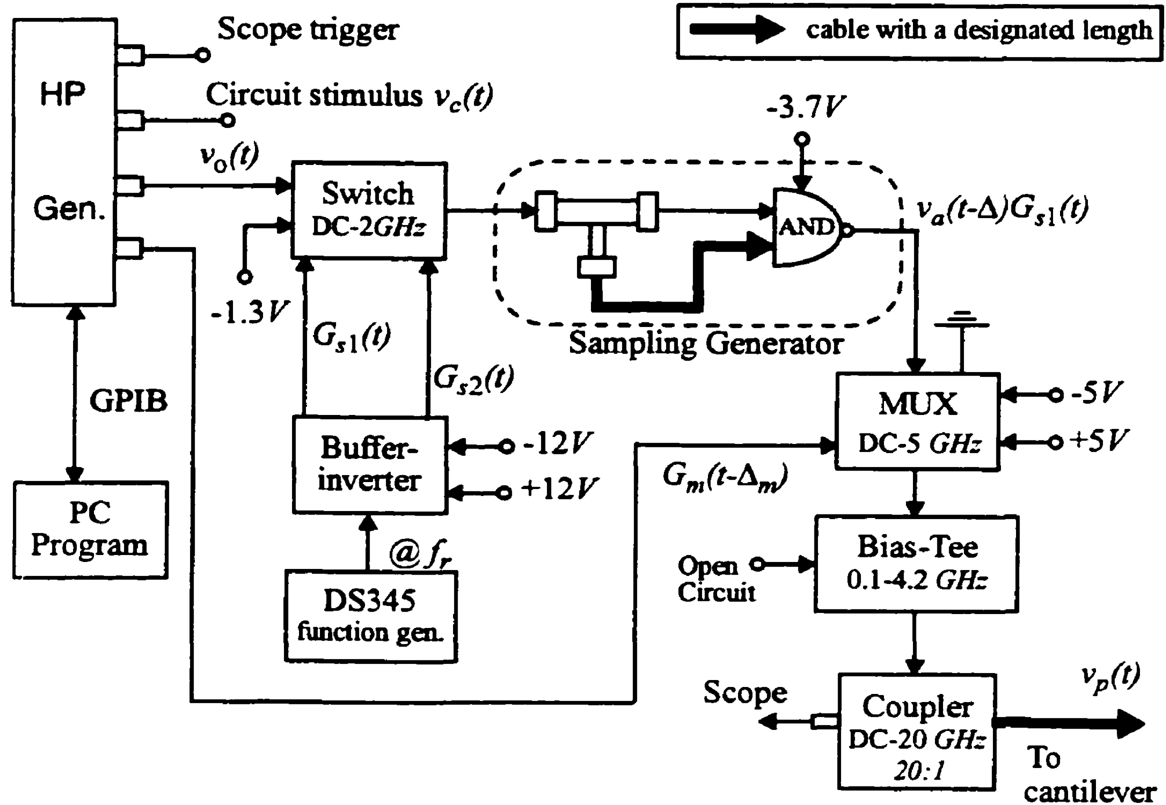


Figure 4.15: Implementation of the sampling pulse generation system for EFS using amplitude modulation.

The signal $v_0(t)$ in figure 4.15 is a $125MHz$ signal with $1ns$ pulses which enters into a MSWA-2-20 absorptive switch with a bandwidth of $2GHz$ [74]. The logic levels of the $1ns$ pulses were chosen to be $-1.3V$ and $0V$ so that the inputs to the AND gate have the appropriate logic levels of $-0.9V$ and $0V$. This signal attenuation is mostly by the BNC splitter.

The DC-$2GHz$ switch acts as a modulator which downconverts the $1ns$ pulses to the resonant frequency of the cantilever, f_r. A DS345 function generator was used to supply the control signals $G_{si}(t)$ at logic levels of $0V$ and $-8V$ to the switch with the aid of a simple buffer-inverter circuit. A DC voltage of $-1.3V$ was served as the second input to the switch to define the logic level of the base of the pulses, i.e. the voltage level when the pulses in

the sampling signal are turned off by the switch. The output of the switch was fed into the sampling generator described in figure 4.13. Compared to figure 4.1, the orientation of the modulating switch and the sampling generator is reversed in this implementation. This is because the switch has a bandwidth of only $2GHz$ while the AND/NAND gate has a higher bandwidth of about $5GHz$. Nonetheless, this setup performs the same functionality as intended in figure 4.1. The output of the sampling generator within the ensemble in figure 4.15 is a modulated version of the signal in figure 4.14(b).

A DC-$5GHz$ MUX was used to eliminate some of the non-idealities that exist in the output signal of the sampling generator. A carefully aligned gate signal $G_m(t-\Delta_m)$ was supplied by the HP generator to the MUX for turning on its high frequency input $v_a(t-\Delta)G_{s1}(t)$ when this sampling signal was logic low, i.e. the duration of the pulses, and to select its grounded input when the sampling signal was at the high logic level of $0V$.

A bias tee was inserted into the realization to eliminate possible damage to the cantilever from a large current that could be formed if the cantilever contacted a high voltage DC supply or bias on a test circuit, and thus protecting the cantilever from over heating. The DC-$20GHz$ coupler was used to divide 1/20th of the power from the sampling signal to the sampling oscilloscope for monitoring the shape of the sampling pulse and its reflections from the tip of the cantilever, which is essentially an open circuit. As a result, the cable length between the coupler and the cantilever was carefully selected so that the reflected pulses were absorbed by the DC-$5GHz$ MUX. Using the coupler and the sampling oscilloscope, the required cable length which corresponds to a correct delay Δ_T for matching was experimentally found through trial and error. After the appropriate cable length was appointed, the signal at the scope only consisted of two distinct pulses with similar amplitudes within the period T: the incident sampling pulse to the cantilever, and the reflected from the cantilever.

Figure 4.16 shows an effective sampling pulse belonging to the probing signal $v_p(t)$ generated using this implementation. The MUX and the bias tee slightly degraded the signal amplitude and bandwidth from the output of the sampling generator. The pulse has an amplitude of $750mV$ and a FWHM of $140ps$ at a frequency of $125MHz$. It also possesses some non-idealities which may be eliminated by using a MUX with a faster switching

time. The influence of these imperfections due to the sampling pulse on the measurements will be explored in section 5.4. The actual sampling signal is a modulation of the pulse in figure 4.16 at the resonant frequency of the cantilever, f_r.

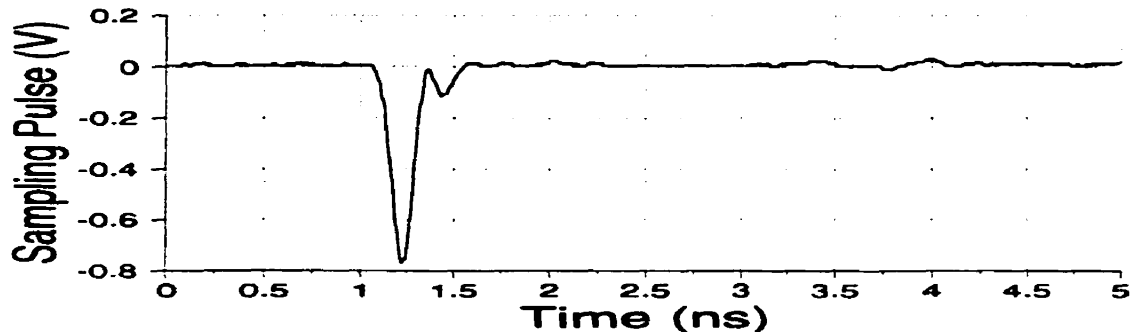


Figure 4.16: A pulse within the sampling signal generated by the amplitude modulation implementation in figure 4.15 captured by a sampling oscilloscope.

4.4 Pulse Width Modulation

Another specific case of synchronous time domain gating that can be implemented for EFS is pulse width modulation. In contrast to amplitude modulation in which a pulse generator is required, pulse width modulation can forego the use of a pulse generator by using a fast step generator instead to achieve high speed measurements. This has a couple of potential advantages. First, it is perhaps easier to produce a signal with a sharp rise or fall time and a large duty cycle, then to create an impulse with both sharp rise and fall times and a narrow duty cycle. The second possible benefit is bandwidth versatility because the effective sampling pulse width can easily be adjusted by the inter-delay between the input signals to the modulating switch(es). High bandwidth can be obtained by minimizing this inter-delay. The pulse width modulation approach [82], can be implemented using time domain gating described in section 4.2. A more detailed theoretical concept of pulse width modulation is explained next.

4.4.1 Theory

Referencing the general case of synchronous time domain gating described in section 4.2, the pulse width modulation scheme can be implemented by selecting the number of sampling generators K=2, $v_{s1}(t)=v_{pwm}(t)$, and $v_{s2}(t)=v_{pwm}(t-\tau)$, where $v_{pwm}(t)$ is usually a

train of pulses with its frequency matched to the circuit signal, and τ is called the modulation depth or the inter-delay between the signals $v_{s1}(t)$ and $v_{s2}(t)$. A larger duty cycle of the signal $v_{pwm}(t)$ than that of $v_a(t)$ in amplitude modulation may be allowed without sacrificing the bandwidth, since the bandwidth in pulse width modulation is determined by only one of the signal transistion times in $v_{pwm}(t)$ and the modulation depth. Therefore, it does not require the gating signal $v_{pwm}(t)$ to possess both fast rise and fall times, and the duty cycle of $v_{pwm}(t)$ is absolutely trivial. This is quite practical because devices may not produce signals with equal rise and fall times. Figure 4.17 helps to discern the concept of pulse width modulation by exemplifying a few sketches of the associated typical signals.

Figure 4.17(a) shows an example of $v_{pwm}(t)$ created by a generator which produces a pulse with a faster fall time than its rise time. Both input signals in figure 4.17(a) to the sampling generators are identical except for the phase difference of τ. The boundary of the effective modulated portion is defined by the transition edges of the signals after these signals are downconverted, and the size of this modulated portion is controlled by the modulation depth τ. In amplitude modulation, high frequency sampling pulses created by a pulse generator is modulated by a lower carrier frequency f_r, whereas in pulse width modulation, the sampling pulses are created by the modulation process rather than using a pulse generator. Mathematically, it can be proven that the effective sampling signal in pulse width modulation is deduced by a filtered subtraction between $v_{s1}(t\text{-}\Delta_1)$ and $v_{s2}(t\text{-}\Delta_2)$, i.e. $v_{pwm}(t\text{-}\Delta_1)\text{-}v_{pwm}(t\text{-}\Delta_1-\tau)$. Using (4.9) and (3.8), with also the observation that $\langle v_{pwm}(t\text{-}\Delta_1)\ \text{-}v_{pwm}(t\text{-}\Delta_1-\tau)\rangle$ is zero, the cantilever deflection at the resonance $\omega_r=2\pi f_r$ is:

$$\begin{aligned}\Delta_z\big|_{\omega_r} &= -\frac{\partial}{\partial z}C(x,y,z)\frac{Q}{k} \\ &\left\{\langle[v_{pwm}(t-\Delta_1)-v_{pwm}(t-\Delta_1-\tau)]G_m(t-\Delta_m)v_c(x,y,t)\rangle\right\}\frac{2}{\pi}\sin(\omega_r t)\end{aligned} \quad .(4.16)$$

Lets examine the inner product in (4.16) by setting $v_s(t)=v_{pwm}(t)\text{-}v_{pwm}(t-\tau)$: i.e. $-\langle v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)v_c(x,y,t)\rangle$. This is also a convolution between the effective sampling signal $v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)$ and the circuit signal under investigation $v_c(x,y,t)$, if the time delay of $v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)$, Δ, is a varying parameter. By performing this convolution, the waveform of the measured deflection signal by EFS can be predicted.

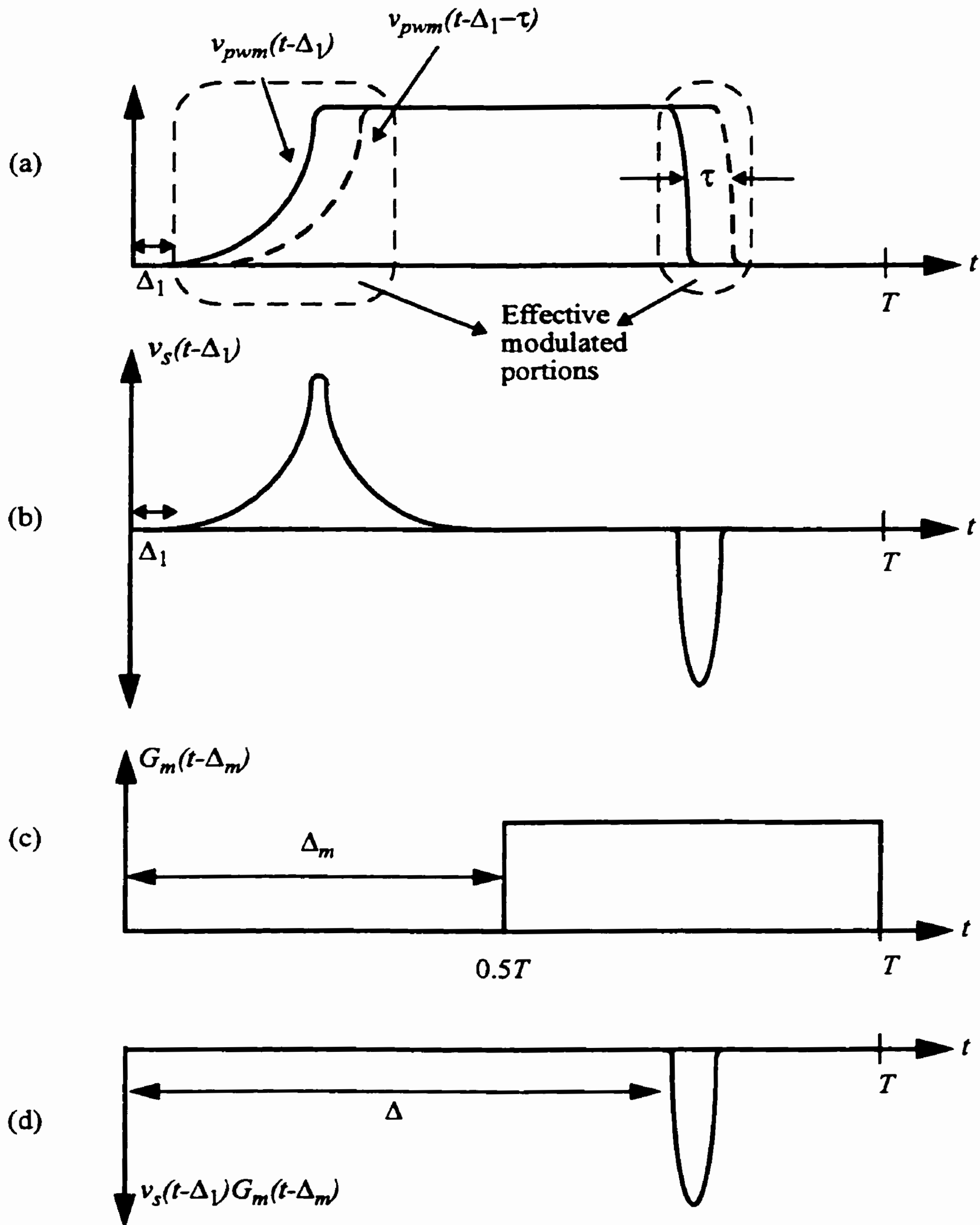


Figure 4.17: Sketched waveforms of example signals in pulse width modulation: (a) $v_{pwm}(t-\Delta_1)$ and $v_{pwm}(t-\Delta_1-\tau)$, (b) the dual pulse signal $v_s(t-\Delta_1)=v_{pwm}(t-\Delta_1)-v_{pwm}(t-\Delta_1-\tau)$, (c) the gate signal $G_m(t-\Delta_m)$ with a 50% duty cycle, and (d) the effective sampling signal $v_s(t-\Delta_1)G_m(t-\Delta_m)$ with an effective initial delay Δ.

The subtraction $v_s(t\text{-}\Delta_1)$ between $v_{pwm}(t\text{-}\Delta_1)$ and $v_{pwm}(t\text{-}\Delta_1-\tau)$ contains a positive and a negative pulse within a period T as displayed in figure 4.17(b). The signal $G_m(t\text{-}\Delta_m)$ is used to filter out in time either the positive or the negative pulse using a RF-MUX. A typical signal $G_m(t\text{-}\Delta_m)$ is sketched in figure 4.17(c). Usually, the sharper transition which corresponds to a narrower effective pulse is chosen. For instance, if the fall time of $v_{pwm}(t)$ is faster than the rise time, the positive pulse, i.e. the rising edge of $v_{pwm}(t)$, can be gated out and only the negative pulse remains for sampling, as depicted in figure 4.17(d).

The gate signal $G_m(t\text{-}\Delta_m)$ contributes to the making of the desired sampling signal. Sampling must therefore be achieved by synchronously scanning the time delay Δ_1 and Δ_m through the entire period T, or by sweeping the circuit signal delay while maintaining both Δ_1 and Δ_m constant. The term Δ in figure 4.17(d) is the initial delay of the effective sampling signal $v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)$.

Although there is an absence of $\Delta\Phi$ in (4.16), EFS using pulse width modulation is still affected by DC effects as the DC component of the effective sampling signal is non-zero.

4.4.2 Experimental Implementation

This section presents the realization of the pulse width modulation technique engineered in this work. A block diagram of this implementation is illustrated in figure 4.18. The synchronizing source used was the HP8000 data generator, and its outputs were defined by a computer program through a GPIB connection. Two channels of the generator were used to provide the triggering signal to the 20*GHz* Tektronic scope, and the signal to the test circuit, respectively. Another channel supplies the input $v_0(t)$ which is a 125*MHz* signal with 4*ns* pulses and logic levels -1.3*V* and 0*V* to a BNC splitter. The modulation depth was set by appointing two cables with different lengths for the inputs to a MSWA-2-20 absorptive switch. The DC-2*GHz* switch modulates the two input signals by alternating them at the resonance of the cantilever, f_r. A DS345 function generator and a buffer-inverter circuit identical to those in section 4.3.3 was utilized for providing the control signals $G_{si}(t)$ to the switch. The 8*Gb/s* two-input NEL AND/NAND circuit was employed as a step generator to accelerate the transition times of the modulated signal.

Again, the order of the step generator and the modulation switch was reversed as compared to figure 4.1 due to the bandwidth inferiority of the MSWA-2-20 switch. The gate signal $G_m(t-\Delta_m)$ with period T and a 50% duty cycle was generated by the HP generator, and was coaxed into the DC-5GHz MUX for filtering out one of the transition edges of the modulated signal. Finally a DC-20GHz coupler was used to monitor the reflected sampling signal by the cantilever for determining the suitable cable length for matching.

The bias tee was not used here because that would eliminate the DC component in the effective sampling signal, which in turn would have deformed the sampling signal to give a more distorted measurement of the signal under test.

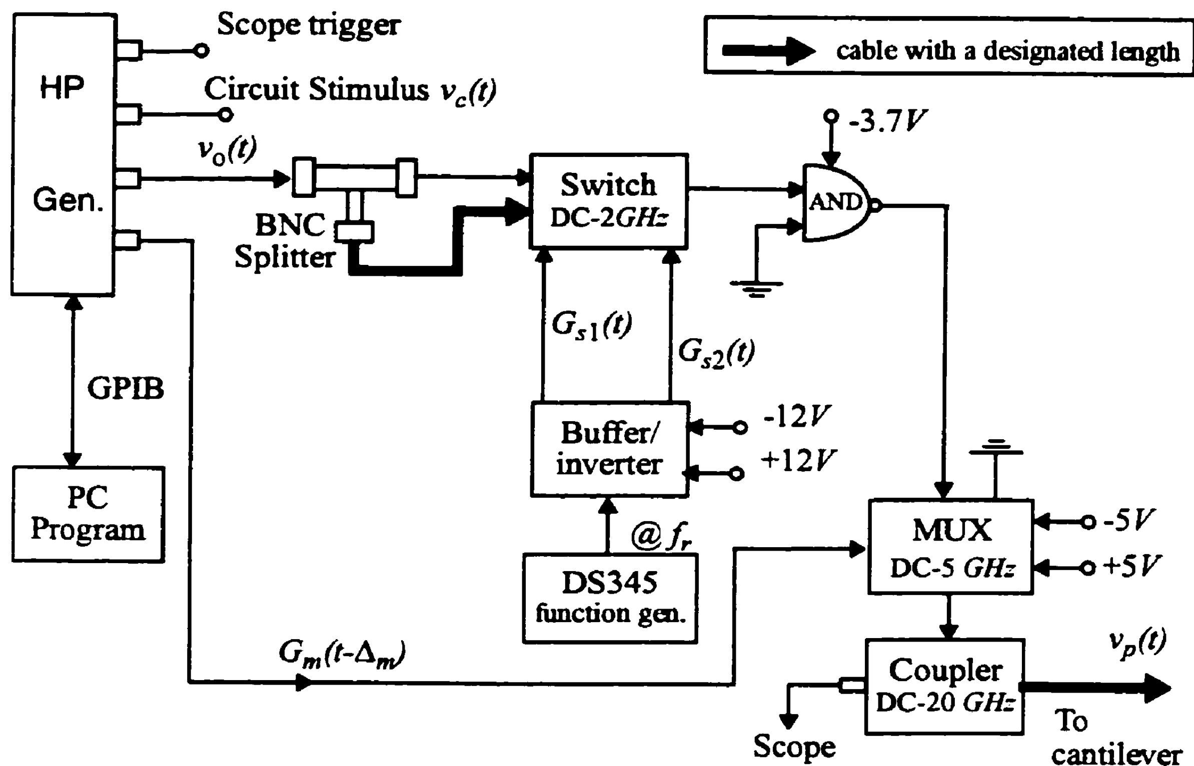


Figure 4.18: Realization of the sampling pulse generation system for EFS using pulse width modulation.

Pragmatically speaking, the polarity of the effective sampling pulse cannot be recognized by a sampling oscilloscope because the pulse is virtual using this specific ensemble. The 'subtractor' and 'subtractee' of the subtraction between $v_{pwm}(t)$ and $v_{pwm}(t-\tau)$ is indeterminable, and therefore, proper control experiments may be required to select the correct transistion edge for sampling if the polarity of the measured signal pattern is desired.

Because the shape of the effective sampling pulse for pulse width modulation in this work is similar to that for amplitude modulation, the measured waveforms of the 0.5 μm CMOS circuit using both modulation techniques were compared to determine the appropriate polarity of the pulse width modulation method. This procedure should be valid since the CMOS inverter chain used in this work gives signals with non-identical rise and fall times.

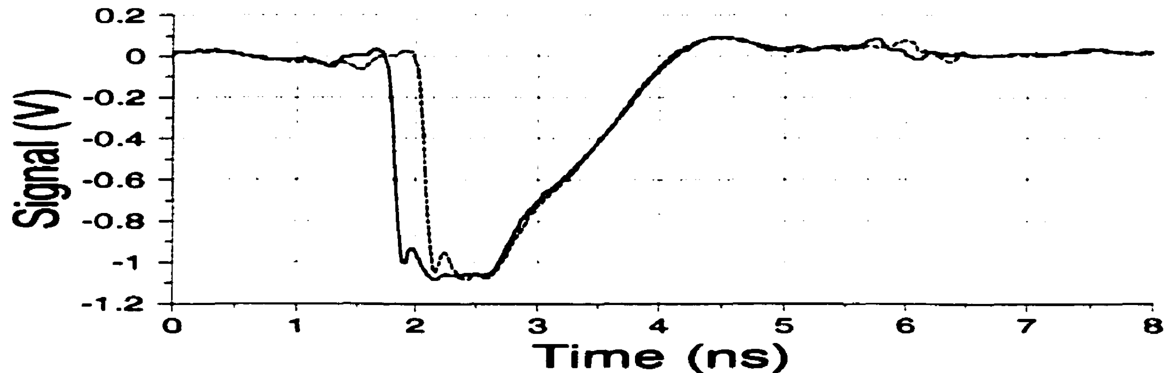


Figure 4.19: The two modulated sampling signals in the pulse width modulation scheme in this work. These signals are captured by a sampling oscilloscope. The delay between these signals is 250*ps*, which is the modulation depth.

Figure 4.19 shows the two modulated signals in $v_p(t)$ in the pulse width modulation implementation in figure 4.18. The delay between these two signals at the falling edges corresponds to the modulation depth, which is 250*ps* for the case shown in the figure. The rising edges of the signals in figure 4.19 shows the switching speed of the DC-5*GHz* MUX, which is about 2*ns*.

Figure 4.20 shows the effective sampling pulse $v_s(t-\Delta_1)G_m(t-\Delta_m)$, which was mathematically deduced by subtracting the two modulating sampling signals showed in figure 4.19. The modulation depth is 250*ps*, as indicated in figure 4.19. This pulse has an amplitude of 880*mV* and a FWHM of 250*ps* at a frequency of 125*MHz*. The signal contains a few non-idealities near the pulse which are quite difficult to eliminate. They are caused by the inherent overshoots and ringing that exist in the signals generated by the HP generator and the employed electronics. The FWHM is not necessary identical to its corresponding modulation depth. This is shown in the next example. However, their values should be very similar when the modulation depth is large.

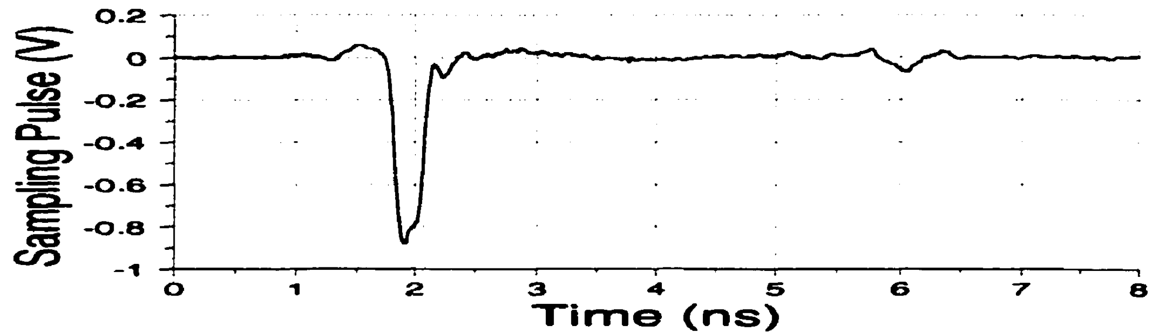


Figure 4.20: The effective sampling pulse generated by pulse width modulation (modulation depth of 250*ps*) obtained by subtracting the two modulating signals in figure 4.19.

Figure 4.21 shows the virtual sampling pulse obtained by subtracting the two signals in figure 4.19, but using a modulation depth of 50*ps*. The modulation depth can be changed by changing the length of one of the cables that connects from the BNC splitter to the input of the MSWA-2-20 switch. This pulse has an amplitude of 450*mV* and a FWHM of 100*ps* at a frequency of 125*MHz*.

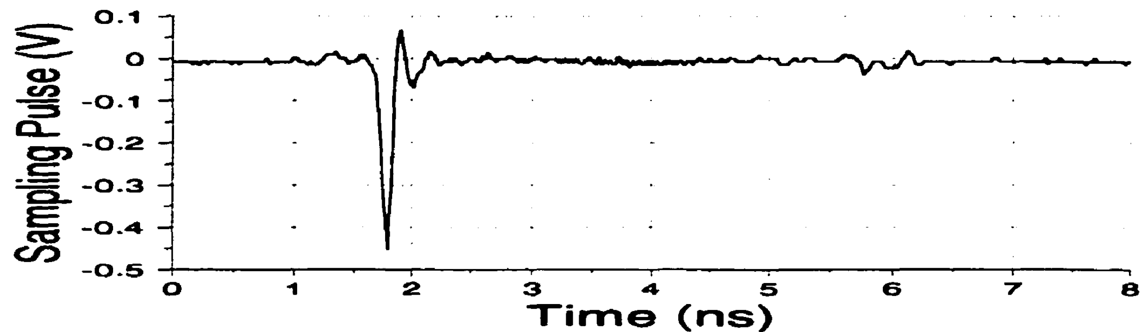


Figure 4.21: The effective sampling pulse generated by pulse width modulation (modulation depth of 50*ps*) obtained by subtracting the two modulating signals in figure 4.19, but with a 50*ps* delay between them instead.

Chapter 5

Theoretical Characterization

This chapter contains a preliminary performance evaluation of EFS. The proposed instrument will be characterized by the criteria of spatial resolution, invasiveness, sensitivity, bandwidth and delay resolution using which the standards of a competent diagnostic tool are defined.

5.1. Spatial Resolution

Spatial resolution generally indicates the locality of the measurements performed by an instrument. This is an important parameter to be considered for electrostatic force probing when circuit density is currently increasing drastically. To resolve the spatial resolution of EFS, its definition of must first be carefully and precisely defined.

Spatial resolution depends on the tip-circuit geometry and the interactions between the cantilever and the circuit. Specifically, the force on the cantilever is derived from the capacitive coupling between itself and the entire circuit. The magnitude of this force is in fact, a complicated average of electrostatic forces induced by all points on the surface of the circuit. It is then logical to define the electrical spatial resolution as a size of a region on the circuit that bounds a certain fraction of the total electrostatic force on the tip of the cantilever. Since the tip-circuit geometry is also associated with spatial resolution, this specification must not be forgotten when stating the spatial resolution for an instrument.

The interactions between a micromachined Si_3N_4 cantilever and a coplanar waveguide fabricated on a GaAs substrate were modelled to determine the spatial resolution of the instrument [83]. Figure 5.1 shows a graph of force density at three different tip-circuit separations versus horizontal distance away from the test point. The spatial resolution was defined in [83] as the diameter of the circle at where the force density decreases to 1/e from its maximum, with the centre of this circle being the desired test point. The spatial resolution for a 100*nm* tip-circuit spacing was resolved to be 300*nm*. Resolution was worse when the tip is further above from the circuit. Yet, with a vertical tip-circuit gap of

500*nm*, resolution remained near 1μ*m* or less. This finding suggests that EFS using the Si_3N_4 cantilever should perform accurate measurements of a 1μ*m* interconnect line on a typical integrated circuit. Thus, this cantilever should be sufficient for reliably measuring the circuits in this work.

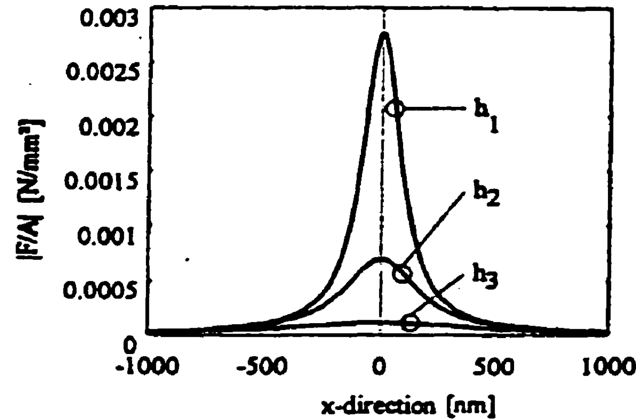


Figure 5.1: The force density on a micromachined cantilever versus horizontal distance (x-direction) of a GaAs coplanar waveguide at different vertical tip-surface distances, h_1=100*nm*, h_2=200*nm*, and h_3=500*nm* [83]. The circles indicate the 1/e points from the maximum of each corresponding curve.

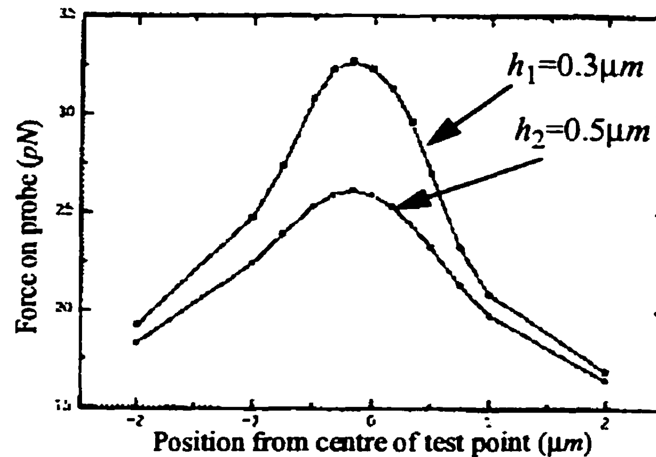


Figure 5.2: Simulations of the normalized vertical force experienced by the NT-MDT sc12-E cantilever at h_1=0.3μ*m* and h_2=0.5μ*m* above a 1μ*m* wide interconnect line on a 500μ*m* thick GaAs substrate [84].

The spatial resolution using the sc12-E silicon cantilever introduced in section 3.3.3 is predicted by simulations of the electrostatic force above a microstrip line on a GaAs substrate [84]. Figure 5.2 shows the simulated vertical force experienced by the silicon canti-

lever situated at 0.3 and 0.5μm over a 1μm wide interconnect line on the 500μm high GaAs substrate with an infinite ground plane. By defining the spatial resolution as the radius of the area in which the electrostatic force drops to 1/2 from its maximum, the spatial resolution suggested by figure 5.2 is about 2μm under static conditions, but this may be inadequate for integrated circuit measurements. However, the radius of curvature of the cantilever's tip specified in the simulation in [84] was 100nm while the specification in [54] is 35nm. The actual resolution may therefore be better than the calculated value.

5.2. Invasiveness

Invasiveness translates to a disturbance of normal circuit operation due to loading or crosstalk by a mechanical conducting probe. The parasitic loading on the circuit consists of three types. Resistive loading becomes apparent when the input resistance of the probe is comparable to circuit impedance. It results in attenuation of the test signal, and can perturb the DC bias of the DUT. Inductive loading introduces overshoots and other distortions of the circuit signal. The most destructive effect is perhaps capacitive loading, which alters the transitions and latency of the test signal. The input capacitance for a minimum size gate is currently about 10fF which is comparable with or much less than most loadings by commercial contact probes which are typically 0.01-0.1pF [5,6]. A physical probe inserts an extra capacitance C_{probe} parallel to the existing load on the circuit, $C_{circuit}$, thereby adding these two capacitances to form a larger loading on the circuit test point, $C_{total} = C_{probe} + C_{circuit}$. The signal transistion time of an integrated circuit is mostly governed by the speed of charging and discharging a capacitive load, i.e. $i = C_{total} dV/dt$. When additional capacitive loading is introduced by probing, the voltage transition time dt increases for the same amount of driving current i on the circuit. This may decrease the operating frequency of the circuit, or even fail digital devices when voltage levels at certain timings are not satisfied for switching certain transistors [63].

Electrostatic force probing is a non-contact technique which depends on the capacitive coupling between the cantilever's tip and the test point. The value of this mutual capacitance should be calculated to determine the impact it has on the circuit signals. The coupling capacitance between a Si_3N_4 micromachined cantilever and a 3μm microstrip line

was simulated to be $0.24fF$ when the cantilever was situated $1\mu m$ above the line [85]. At $100GHz$, the parasitic shunt impedance $1/2\pi fC_{probe}$ is $6.6K\Omega$. This means the capacitive coupling is practically nonexistent when measuring 50Ω systems. When the sc12-E silicon cantilever is $0.5\mu m$ above a $1\mu m$ wide interconnect line on a $500\mu m$ thick GaAs substrate, the capacitance C_{probe} added to the circuit was simulated to be $1.25fF$ [84]. The realistic loading by the cantilever may be lower than the simulated value due to the incompatibleness between the radius of curvature of the cantilever's tip used in the simulation in [84] and that specified by the manufacturer.

EFS may cause another form of invasiveness by crosstalk or radiation. The signal at the cantilever or the feed to the cantilever may interfere with the circuit signal perturbing normal operation. For investigating the severity of this crosstalk, the cantilever can be placed at a typical measuring distance from the circuit test point with the circuit signal running, and observe the induced crosstalk signal at the cantilever using an oscilloscope or examine the S-parameters of the path to the cantilever. At the operating frequencies in this work, this is not a concern. However, the crosstalk effect should be considered as one of the limiting factors for EFS at very high frequencies.

5.3 Voltage Sensitivity

Voltage sensitivity is defined as the minimum root-mean-square (RMS) detectable voltage that can be sensed by an instrument. Noise is the obvious limit since voltages cannot be extracted if the signal level is buried in the noise range. In EFS, any signal detected by the deflection sensor that is not induced by the electrostatic force between the cantilever and the circuit is considered as noise. This section performs the formulations for the SNR and the voltage sensitivity of EFS.

The beam-bounce system used in this thesis provides shot noise as discussed in section 3.4. Other contributing noise factors include mechanical vibrations from the probing structure, electrical noises coupled to the cantilever by external sources, and thermal noise. Mechanical noise can easily be minimized by installing the mechanical probing instrument onto a vibration isolated structure, or by using vibration absorbers. Electrical noise can be eliminated by shielding the probing signal path with proper grounding. The una-

voidable noise factor is thermal noise.

Thermal noise vibrates the cantilever simply because of the existence of temperature as random air molecules crash onto the cantilever. The RMS deflection of the probe as a function of frequency due to thermal noise can be expressed as [71]:

$$\left[\Delta z_{th}^2(\omega)\right]^{1/2} = \sqrt{\frac{4Qk_BT_mB}{k\omega_r}} \cdot \frac{\omega_r/\omega}{\sqrt{1+Q^2\left(\frac{\omega_r}{\omega}-\frac{\omega}{\omega_r}\right)^2}} \tag{5.1}$$

where k_B is the Boltzman constant, T_m is the medium temperature and B is the measurement bandwidth. The shape of the spectrum in (5.1) is identical to the frequency response of the cantilever because the intrinsic response of thermal noise is constant. The maximum probe vibration is at the resonance of the cantilever, ω_r, and is given by:

$$\left[\Delta z_{th}^2(\omega_r)\right]^{1/2} = \sqrt{\frac{4Qk_BT_mB}{k\omega_r}}\,. \tag{5.2}$$

For the Si_3N_4 micromachined cantilever with Q=32, k=0.064*N/m*, and a resonance of f_r=12.275*KHz*, the maximum deflection due to thermal noise at room temperature is $0.01 nm/\sqrt{Hz}$ which is also the same for the silicon cantilever (Q=30, k=0.055*N/m*, f_r=13.0625*KHz*). Comparing this to the deflection of $8\times10^{-6} nm/\sqrt{Hz}$ contributed by the shot noise, it is cogent to state that thermal noise is the dominating noise factor in determining the SNR and the sensitivity of EFS.

The SNR of the instrument can be defined as the following:

$$SNR = \frac{\left|\left[\Delta z_F^2(\omega_r)\right]^{1/2}\right|}{\left[\Delta z_{th}^2(\omega_r)\right]^{1/2}} \tag{5.3}$$

where $\left[\Delta z_F^2(\omega_r)\right]^{1/2}$ is the RMS deflection by the electrostatic force on the cantilever, which is derived from (4.9) and (3.8). The voltage sensitivity can be determined by equating the maximum RMS deflection due to thermal noise to the maximum RMS deflections by the induced force:

$$\left[\Delta z_{th}^2(\omega_r)\right]^{1/2} = \left|\left[\Delta z_F^2(\omega_r)\right]^{1/2}\right|\,. \tag{5.4}$$

Lets explore the two special cases of synchronous time domain gating for EFS implemented in this thesis project: amplitude and pulse width modulation.

5.3.1 Amplitude Modulation

In amplitude modulation, with the assumption that $G_m(t-\Delta_m)$ is an all pass gate signal and the DC offset effects $\Delta\Phi$ is negligible for simplicity, the RMS deflection at the resonance of the cantilever $\omega_r=2\pi f_r$ deduced from (4.14) is:

$$\left[\Delta z_F^2(\omega_r)\right]^{1/2} = \left|\frac{\partial}{\partial z}C(x,y,z)\frac{Q}{k}\frac{\sqrt{2}}{\pi}\left\{\frac{1}{2}\langle v_a^2(t-\Delta)\rangle - \langle v_a(t-\Delta)v_c(x,y,t)\rangle\right\}\right|. \quad (5.5)$$

The SNR for amplitude modulation can be found by dividing (5.5) with the deflection by thermal noise in (5.2):

$$SNR = \left|\frac{\partial}{\partial z}C(x,y,z)\right|\frac{1}{\pi}\sqrt{\frac{Q\omega_r}{2kk_BT_mB}} \cdot \left|\frac{1}{2}\langle v_a^2(t-\Delta)\rangle - \langle v_a(t-\Delta)v_c(x,y,t)\rangle\right| \quad (5.6)$$

Using a rectangular pulse approximation for the pulses in $v_a(t-\Delta)$, the inner products become:

$$\langle v_a(t-\Delta)v_c(x,y,t)\rangle = \frac{\delta}{T}V_a v_c(x,y,t=\Delta), \quad (5.7)$$

and

$$\langle v_a^2(t-\Delta)\rangle = \frac{\delta}{T}V_a^2, \quad (5.8)$$

where V_a is the amplitude of the rectangular sampling pulse. If the value in (5.8) is usually very small compared to (5.7), the SNR in (5.6) is then:

$$SNR \approx \left|\frac{\partial}{\partial z}C(x,y,z)\frac{1}{\pi}\frac{\delta}{T}\sqrt{\frac{Q\omega_r}{2kk_BT_mB}}V_a v_c(x,y,t=\Delta)\right|. \quad (5.9)$$

Using the sampling pulse in figure 4.16 and the silicon cantilever, the SNR for the measurements using amplitude modulation in this work can be approximated from (5.9). The ill-conditioned factor in (5.9) is the capacitance derivative $\partial C(x,y,z)/\partial z$ because this value changes with the unpredictable tip-circuit geometry during measurement. For approximation, it can be assumed that this value is roughly $80pF/m$ for both microma-

chined cantilevers [84]. With Q=30, f_r=13.0625KHz, k=0.055N/m, $\delta \approx$FWHM=140ps, T=8ns and V_a=2x750mV (V_a is 2 times the signal amplitude due to reflection from cantilever), the SNR is found to be 50 $\sqrt{Hz}/V$ at room temperature. For the Si_3N_4 cantilever with (Q=32, k=0.347N/m, f_r=12.275KHz), this SNR is estimated to be 20 $\sqrt{Hz}/V$.

The mathematical expression of the voltage sensitivity for amplitude modulation is derived by substituting into (5.4) with (5.5) and (5.2), and then solving for the minimum circuit voltage. In general, the minimum voltage detectable is represented by the inner product between the sampling signal and circuit waveform:

$$\langle v_a(t-\Delta)v_c(x,y,t)\rangle = \left|\frac{1}{2}\langle v_a^2(t-\Delta)\rangle - \frac{\pi}{\partial C(x,y,z)/\partial z}\sqrt{\frac{2kk_BT_mB}{Q\omega_r}}\right| . \quad (5.10)$$

Neglecting the relatively diminutive term $1/2\langle v_a^2(t-\Delta)\rangle$ and employing rectangular pulse approximation for the pulse in figure 4.16, the voltage sensitivity is:

$$\Delta V_{RMS} \approx \left|\frac{\pi \cdot T}{\delta V_a \partial C(x,y,z)/\partial z} \cdot \sqrt{\frac{2kk_BT_mB}{Q\omega_r}}\right| . \quad (5.11)$$

Using the parameters above for the SNR calculation, the minimum RMS voltage detectable using the silicon cantilever is $20mV/\sqrt{Hz}$ and $50mV/\sqrt{Hz}$ for the Si_3N_4 cantilever.

The derivative of the mutual tip-circuit capacitance must be found to theoretically calculate the minimum detectable voltage. Therefore, both SNR and voltage sensitivity are subjected to the uncertain tip-circuit geometry.

Neither the SNR nor voltage sensitivity is a function of frequency or bit rate of the signal under test. Yet, through the rectangular pulse approximation for the sampling pulse, it shows clearer that the SNR and voltage sensitivity are dependent on the duty cycle of the sampling pulse. This suggests a trade off between bandwidth and voltage sensitivity. In fact, using the silicon cantilever and a unit rectangular sampling pulse at 125MHz, the pulse width δ cannot be narrower than 42ps, if $100mV/\sqrt{Hz}$ is the required sensitivity.

5.3.2 Pulse Width Modulation

The RMS deflection of the cantilever for pulse width modulation can be easily

obtained from (4.16):

$$\left[\Delta z_F^2(\omega_r)\right]^{1/2} = -\frac{\partial}{\partial z}C(x,y,z)\frac{Q}{k}\frac{\sqrt{2}}{\pi}\langle v_s(t-\Delta_1)G_m(t-\Delta_m)v_c(x,y,t)\rangle \quad (5.12)$$

where $v_s(t)=v_{pwm}(t)-v_{pwm}(t-\tau)$ is the dual pulse signal described in section 4.4.1. The SNR for pulse width modulation can be found by dividing (5.12) with (5.2):

$$SNR = \left|\frac{\partial}{\partial z}C(x,y,z)\frac{1}{\pi}\sqrt{\frac{Q\omega_r}{2kk_BT_mB}}\langle v_s(t-\Delta_1)G_m(t-\Delta_m)v_c(x,y,t)\rangle\right|. \quad (5.13)$$

The gate signal $G_m(t\text{-}\Delta_m)$, which is synchronized with $v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)$ at the same frequency T, is typically a unit square wave with a 50% duty cycle. Using a rectangular pulse approximation for the effective sampling pulse, the inner product transforms to:

$$\langle v_s(t-\Delta_1)G_m(t-\Delta_m)v_c(x,y,t)\rangle = \frac{\delta}{2T}V_sv_c(x,y,t=\Delta), \quad (5.14)$$

where V_s is the amplitude of the effective sampling pulse, and Δ is the effective initial delay of the pulse. The SNR in (5.13) becomes:

$$SNR \approx \left|\frac{\partial}{\partial z}C(x,y,z)\frac{1}{2\pi}\frac{\delta}{T}\sqrt{\frac{Q\omega_r}{2kk_BT_mB}}V_sv_c(x,y,t=\Delta)\right|. \quad (5.15)$$

Utilizing the pulse in figure 4.19 with $\delta \approx$FWHM=100*ps*, T=8*ns*, V_a=2x450*mV*, and again approximating $\partial(C(x,y,z)/\partial z \approx 80pF/m$, the SNR is found to be $10.7\sqrt{Hz}/V$ for the silicon cantilever which is used for all enclosed measurements using pulse width modulation in this thesis.

The minimum voltage detectable is in general, defined by the inner product:

$$\langle v_s(t-\Delta)G_m(t-\Delta_m)v_c(x,y,t)\rangle = \frac{\pi}{\partial C(x,y,z)/\partial z}\sqrt{\frac{2kk_BT_mB}{Q\omega_r}} \quad (5.16)$$

With the rectangular pulse approximation for the effective sampling pulses in the signal $v_s(t\text{-}\Delta_1)G_m(t\text{-}\Delta_m)$, the RMS voltage sensitivity is:

$$\Delta V_{RMS} \approx \left|\frac{2\pi\cdot T}{\delta V_s\partial C(x,y,z)/\partial z}\cdot\sqrt{\frac{2kk_BT_mB}{Q\omega_r}}\right|. \quad (5.17)$$

Using the same parameters as in the SNR calculation of (5.15), the minimum RMS voltage detectable with the silicon cantilever is $93mV/\sqrt{Hz}$. Under the same conditions, the

voltage sensitivity for a modulation depth of $250ps$ with the corresponding effective pulse displayed in figure 4.20 is $19mV/\sqrt{Hz}$.

5.4 Bandwidth

Since the working principle of EFS is very similar to that of a sampling oscilloscope, the definition of bandwidth for EFS should follow those set for the oscilloscopes. The definition of bandwidth for a sampling instrument [86] is:

$$BW = \frac{0.44}{FWHM} \tag{5.18}$$

where FWHM is the full width of a Gaussian shaped sampling pulse at its half amplitude. It was stated that the measured signal using EFS is a convolution between a sampling pulse and the actual circuit signal. Intuitively, an accurate mapping of the circuit signal can be obtained by a very narrow sampling pulse; the narrower the sampling pulse, the higher the bandwidth, which is consistent with (5.18). Assuming the shape of the sampling pulse in figure 4.16 and figure 4.19 are Gaussian, the bandwidth of the EFS instrument calculated by (5.18) is $3.14GHz$ for amplitude modulation and $4.4GHz$ for pulse width modulation with a modulation depth of $50ps$.

To experimentally determine the bandwidth from the rise times of the digital signals measured by the EFS instrument, The following formula can be used, based on the assumption that both the transitions of the digital test signal and the sampling pulse has the same shape as the rise of a Gaussian function [87]:

$$BW = \frac{0.35}{\sqrt{tr_{meas}^2 - tr_{intr}^2}} \tag{5.19}$$

where tr_{meas} is the 10-90% rise time of the measured signal using the sampling instrument, and tr_{intr} is the 10-90% rise time of the actual signal being measured. Since the measured signal can be foreseen by convoluting the sampling pulse and the circuit signal, lets first speculate the bandwidth for amplitude modulated EFS.

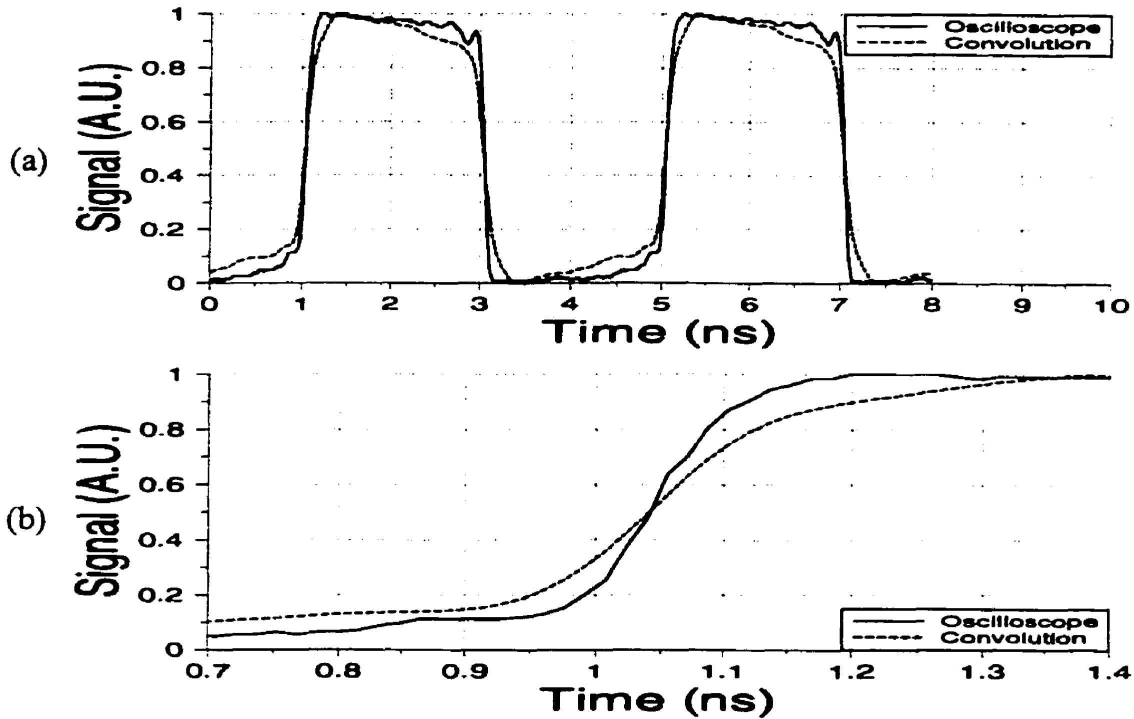


Figure 5.3: (a) A $0.5Gb/s$, $250MHz$ digital signal on a matched microstrip transmission line observed from an oscilloscope versus its convolution with the sampling pulse used in amplitude modulation. Both signals are normalized to [0,1]. (b) Zoomed view for observing rise times of the signals in (a).

The amplitude of the signals in figure 5.3 were normalized and labelled in arbitrary units ($A.U.$). The signal was supplied to a matched 50Ω microstrip transmission line by the HP80000 generator, and the output of the line was measured by a sampling oscilloscope. The HP generator signal has a 10%-90% rise time of tr_{intr}=128ps if the low and high logic levels are defined as $A.U.$=0.1 and $A.U.$=1, respectively. The rise time of the convoluted waveform between the sampling pulse in figure 4.16 and the generator signal is approximated at tr_{meas}=255ps. Using equation (5.19), the bandwidth is estimated to be 1.6GHz which is much worse than 3.14GHz calculated by (5.18). The discrepancy between these two values is mostly caused by the non-idealities of the sampling pulse. By closely examining the signal in figure 4.16, a small pulse of amplitude 0.1V exists immediately after the main sampling pulse. This undesired component of the sampling signal introduces unwelcome overshoot in the convolution product between the pulse and the test signal. The normalization of the convoluted waveform presented in figure 5.3 is therefore invalid. Proper

scaling of the convolution is needed for comparing with the signal being measured. The scaling factor should be selected according to the level of overshoot by the sampling signal. The transistion time and bandwidth is very sensitive to the scaling of the convolution and sampled signals by EFS. A method to fittingly account for this overshoot is to scale the convoluted waveform such that the signal levels at the beginning of the fall transitions (at $3ns$ and $7ns$ in figure 5.3) matches with those of the signal measured by the oscilloscope. Figure 5.4 suggests this new scaling, and the bandwidth is re-examined.

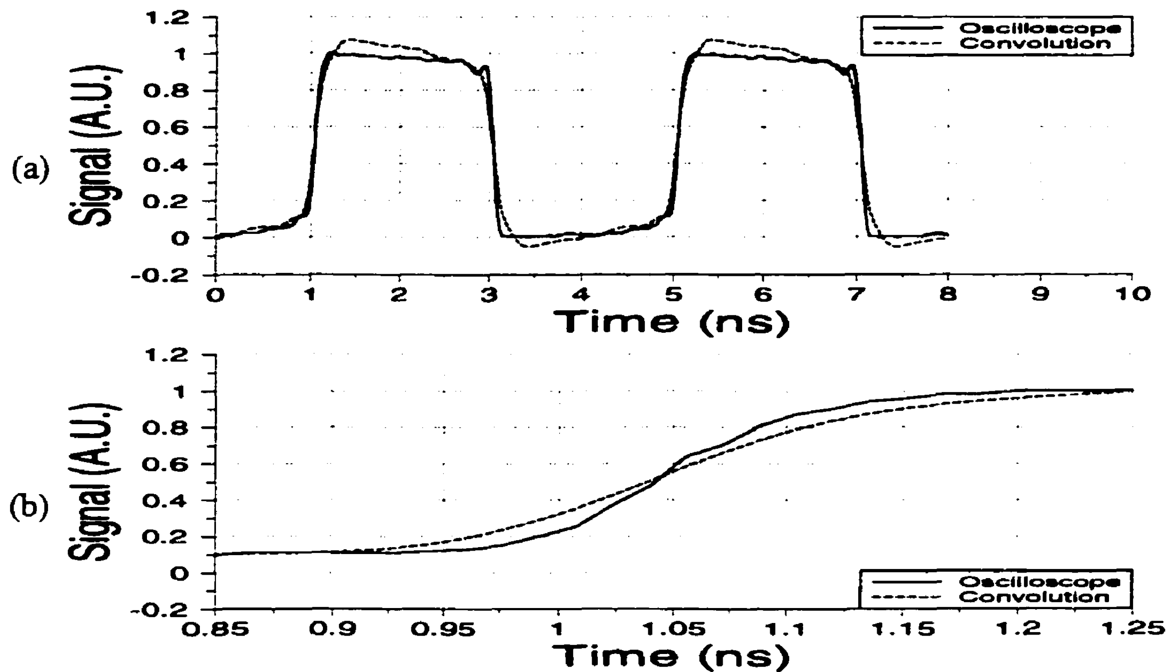


Figure 5.4: (a) A normalized $0.5Gb/s$, $250MHz$ digital signal at the output of a matched microstrip line observed from an oscilloscope versus the convoluted signal with proper scaling to compensate for the overshoot introduced by the non-idealities of the sampling pulse in figure 4.16; (b) zoomed view for observing rise times of the signals in (a).

By specifying the low logic as $A.U$=0.1 and high logic as $A.U.$=1, the rise time of the scaled convolution as seen in figure 5.4(b) is tr_{meas}=172ps. The corresponding bandwidth calculated using (5.19) is 3.04GHz which is in excellent agreement with 3.14GHz calculated by (5.18).

The theoretical bandwidth of pulse width modulated EFS with a modulation depth of 50ps is determined next. The circuit being investigated is a matched 50Ω ceramic trans-

mission line. Figure 5.5 shows the $0.5Gb/s$ digital signal at the output of the ceramic line measured using an oscilloscope. Using the scaling method proposed previously, the convolution between the signal at the oscilloscope and the effective sampling pulse in figure 4.19 was imposed onto the actual ceramic line signal for comparison.

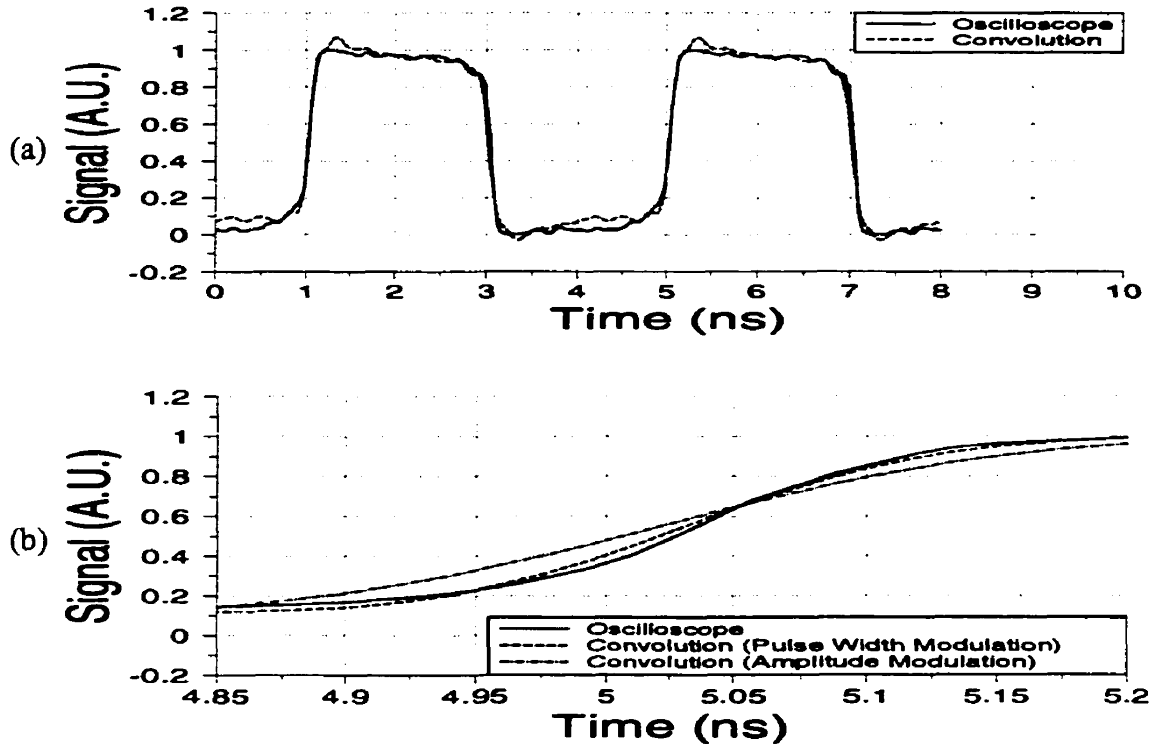


Figure 5.5: (a) A normalized $0.5Gb/s$, $250MHz$ digital signal at the output of a ceramic transmission line observed from an oscilloscope versus its scaled convolution with the effective sampling pulse generated by pulse width modulation using a modulation depth of $50ps$; (b) zoomed view of (a) with the addition of a scaled convolution between the ceramic line signal and the pulse in figure 4.16 for amplitude modulation.

Figure 5.5(b) indicates the oscilloscope signal and its convolution with the pulse for pulse width modulation (modulation depth of $50ps$) are almost indistinguishable. With a designated low logic of $A.U$=0.1 and high logic of $A.U.$=1, the 10%-90% rise time of the justly scaled convolution is $176ps$ in figure 5.5(b), while the rise time of the ceramic line signal in the figure is $174ps$. Bandwidth for pulse width modulation cannot be deduced from the corresponding rise times since they are essentially identical. In fact, this difference in rise times between the actual sampled signal and the test signal is less than the temporal noise which will be discussed in section 5.5.

The convolution produced by the ceramic line signal and the pulse for amplitude modulation in figure 4.16 is also shown in figure 5.5(b). The rise time of this scaled convolution is $256ps$, and is higher than that of the convolution by the pulse in figure 4.19, which has a smaller FWHM. This insinuates that for some cases such as those in which the width of the pulse produced by the impulse generator implemented cannot be adjusted, higher bandwidth may be conveniently achieved by using the impulse generator in a pulse width modulation setup with a modulation depth which corresponds to an effective modulated sampling pulse with a smaller FWHM than that of the amplitude modulated pulse produced by the same impulse generator. In these cases, pulse width modulation provides better bandwidth versatility.

Although in this research, the width of the amplitude modulated sampling pulse can be increased by selecting a smaller delay τ_d between the two signals entering the AND circuit described in section 4.3.2.5. As a matter of fact, if high speed switches or AND gates are served as pulse generators, the width of the pulses at their outputs can easily be changed. Thus, both amplitude and pulse width modulation schemes in this work possess equal bandwidth versatility. With the premise that the implementation for both modulation schemes produce sampling pulses with flexible widths using the same equipments, both modulation techniques have the same bandwidth capability.

The effective sampling pulse width is usually chosen at a minimum while maintaining a maximum amplitude possible, such as in the case of the amplitude modulation implementation in this work. If the effective sampling pulse width can further be decreased, the bandwidth of the EFS instrument can be improved but with the sacrifice of pulse amplitude. Consequently, higher bandwidth is obtained in the expense of voltage resolution, not only on the account of the shrinkage in the duty cycle of the sampling pulse, but also of a reduction in pulse amplitude. The large decrease in pulse amplitude from $880mV$ for a modulation depth of $250ps$ to $450mV$ for a modulation depth of $50ps$ in the pulse width modulation scheme is due to this phenomenon, which is explained with figure 5.6. This figure shows two sketched effective sampling pulses A and B, using a triangular approximation for the pulses, as the sampling pulses in figure 4.16, 4.19 and 4.20 are not Gaussian. Both pulses possess the same transistion slopes as they are produced by the same pulse generation device(s). Pulse A has a FWHM of W_A and an amplitude of V_A, and pulse

B is obtained by decreasing the delays between the input signals into the pulse generation device(s), i.e. τ_a in the amplitude modulation scheme, or the modulation depth τ in pulse width modulation. This new pulse B has a smaller FWHM of W_B, but also a smaller amplitude of V_B. Based on a Gaussian approximation, EFS has higher bandwidth if pulse B is utilized, but it has a poorer voltage sensitivity. Though, on a cautionary note that a triangular approximation is made here instead, thus one must consider carefully when assuming the validity of W_B yielding a higher bandwidth for EFS in general.

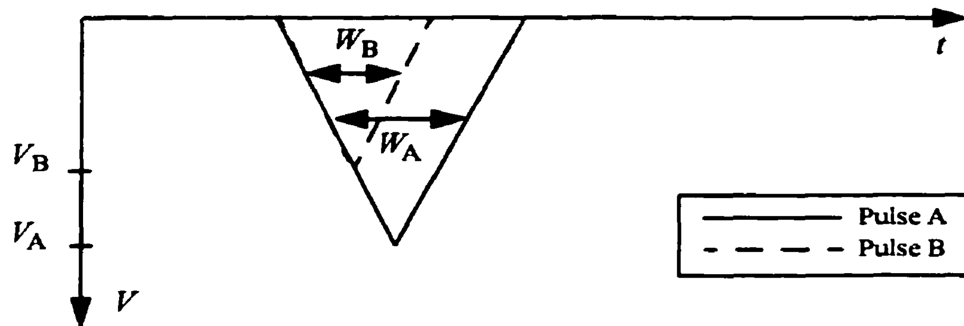


Figure 5.6: The trade off between bandwidth and amplitude of the effective sampling pulse. Pulse A has an amplitude of V_A and a FWHM of W_A, while pulse B has a smaller amplitude of V_B and FWHM of W_B.

5.5 Delay Resolution and Temporal Noise

Delay resolution is the minimum propagation delay detectable in signals under test. There are two factors that limit the delay resolution in EFS. The first factor is the inherent time jitter in the electronics that produce the sampling signal. This timing inconsistency may cause EFS to sample at an incorrect time. In the presenting experimental setups for both modulation schemes, the dominant source of this factor of inaccuracy is the HP generator which has a typical RMS jitter of $10ps$ [61].

The second major factor that bounds the delay resolution of EFS is amplitude noise which is thermal noise. The effect of amplitude noise on temporal error is illustrated in figure 5.7. The voltage sensitivity and the slope of the signal transistion times can be utilized to formulate the relationship between amplitude noise and timing ambiguity [86]:

$$\Delta T = \varepsilon \times \frac{dt}{dv} \tag{5.20}$$

where ΔT is the resulted RMS jitter from the RMS amplitude error ε, and dt/dv is the inverse slope of the signal transition.

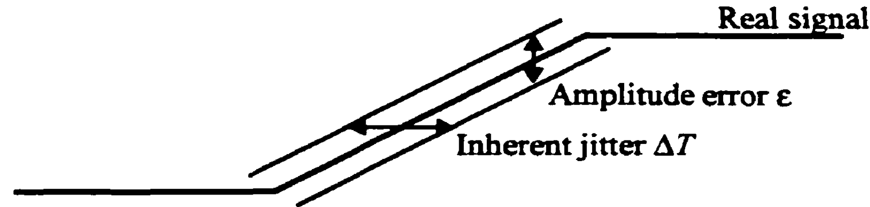


Figure 5.7: Effect of amplitude error on temporal inaccuracy [86].

The term ΔT can also be interpreted as the temporal noise exerted by the EFS instrument, provided that the jitter by the pulse generation electronics is much less than ΔT. The temporal noise decides the precision of the signal transitions measured by EFS. Lets assume the maximum slope measured by EFS is $dt+\Delta T$. Consequently, a more suitable representation of the delay resolution or temporal noise ΔT by amplitude noise is:

$$\Delta T = \varepsilon\left(\frac{dt+\Delta T}{dv}\right) = \frac{\varepsilon \times dt/dv}{1-\varepsilon/dv} . \quad (5.21)$$

Using the rise times of the scaled convolutions on the ceramic transmission line in figure 5.5 for computing dt/dv, and the voltage sensitivities calculated in section 5.3 as ε, the theoretical RMS error ΔT for both amplitude modulation and pulse width modulation (modulation depth of $50ps$) can be determined from (5.21), and are found to be $6.6ps/\sqrt{Hz}$ and $23.2ps/\sqrt{Hz}$, respectively, for a circuit signal amplitude of $1V$ if the silicon cantilever is employed. The actual delay resolution of the EFS measurements in this work should be an accumulation of the RMS jitter ΔT as calculated above, and the RMS jitter from the HP generator.

The bandwidth of EFS is subjected to temporal noise ΔT, which can modify the measured signal transistion times by EFS. Because temporal and amplitude noise are related, the values computed by (5.21) show the price of pulse width modulation also pays for higher bandwidth in this work, is temporal accuracy besides SNR or voltage sensitivity. To calculate the minimum bandwidth of EFS using the proposed setups, the measured rise time tr_{meas} in (5.19) becomes $tr_{meas}+\Delta T$, which is likely to be the typical worse scenario. This will be explored further in section 6.2.1.3 and 6.2.2.

Chapter 6

Measurements using Electrostatic Force Sampling

This chapter exhibits and analyse measurements conducted by EFS with synchronized time domain gating, specifically using the two special implementations of amplitude and pulse width modulation. Performance of EFS will be evaluated and compared with theoretical findings through the measurements obtained over transmission lines, a 0.5μm CMOS inverter chain and a NT25 pulse generator.

6.1 The Measurement System

The block diagram in figure 6.1 presents the experimental setup for the measurements. A computer with a home-written software using a Turbo Pascal language interface (NI-488 DOS Handler) by National Instruments [81,88] automates the experimental procedures by commanding the HP vector generator and reading the measured deflections. Utilizing a GPIB, the software inquires the experimenter to input the signal levels, pattern and timing of the signals from each channel of the generator. These user-specified signals are the inputs to triggering the sampling oscilloscope, the test circuit, and the sampling pulse generation system for producing the proper probing signal, as presented in section 4.3.3 and 4.4.2. For the convenience of the software programmers, the software automates the sampling process by ordering the generator to shift the delay of the circuit signal over its entire period, while holding the sampling signal delays $\Delta_1$and Δ_m constant. The user of the program can specify this incremental delay shift of the circuit signal, which will be referred to as the sampling resolution in this document. The software also allows the user to assign the number of deflection readings at each sampling location for averaging before shifting to another sampling time location. The software stores these deflection averages to a computer text file for analysis and processing.

The sampling pulse generation system in figure 6.1 is the implementation described in figure 4.15 and figure 4.18 for generating a sampling signal $v_p(t)$ either by amplitude or pulse width modulation.

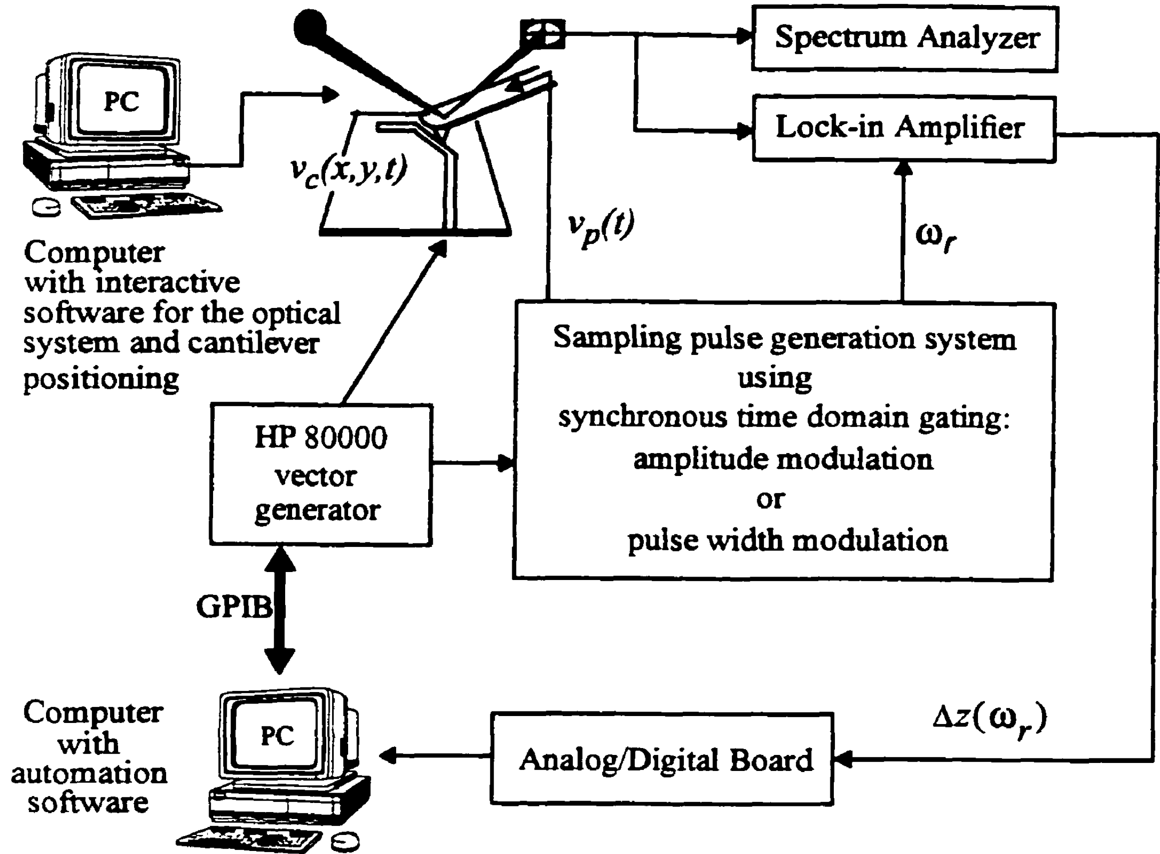


Figure 6.1: Block diagram of the measurement system.

Another computer with a software provided by MFI was used for positioning the cantilever and the components of the optical detection system in the probing structure in figure 3.10. The measured deflections of the cantilever were monitored by a spectrum analyzer and a Stanford Research Systems SR510 lock-in amplifier. The lock-in amplifier acts as a narrow-band filter to collect the deflections at the resonant frequency of the cantilever ω_r. An analog to digital converter was used to direct the measured signal into the computer containing the automation software which stores the received data.

For the measurements conducted using the anodized aluminium stage sketched in figure 3.9, only the Si_3N_4 cantilever was employed. The parameters of the lock-in amplifier for this cantilever was set with the following: sensitivity=$100\mu V$, time constant=$30ms$, and the phase of the square wave reference signal at ω_r is -32.9°. The silicon cantilever was the only cantilever installed onto the stage in figure 3.10. For this cantilever, the sensitivity of

the lock in amplifier was set to $1mV$ and the time constant remained at $30mV$. The reference signal phase of the lock-in amplifier was adjusted to -39.7°. The Si_3N_4 cantilever was only used for the measurements in section 6.2.1.1. Other measurements herein were performed using the silicon cantilever.

Since absolute voltage measurement is extraneous to this work, the amplitude of all measured signals by EFS are normalized to [0,1] in arbitrary units ($A.U.$) unless stated otherwise.

6.2 Measurements on Transmission Lines

This section verifies the principle of and performance by EFS using 50Ω transmission lines as test circuits. Measurements of a feed-through 50Ω microstrip line on a printed circuit board and a ceramic 50Ω transmission line are presented. Both lines were matched with 50Ω terminations to eliminate unwanted reflections. All signals on these lines were supplied by the HP vector generator which had a high and low logic of $1.5V$ and $0V$, respectively.

6.2.1 Amplitude Modulation

This section demonstrates measurements of signals on using amplitude modulation. All enclosed measurements were obtained using the sampling pulse in figure 4.16.

6.2.1.1. Pattern Extraction

Figure 6.2 exhibits measurements of $1Gb/s$ digital signal patterns on the feed-through microstrip line. The sampling resolutions (i.e. the incremental probe-circuit signal delay between each sampling time) were set to be $10ps$ for the measurement in figure 6.2(a) and $50ps$ for that in figure 6.2(b). Knowing that a measurement by EFS can be forecasted by the convolution product between the actual circuit signal and the sampling pulse, the corresponding convolutions were scaled and plotted with the measured signals by EFS in figure 6.2. The real microstrip line signals were obtained by connecting the output of the feed-through line to a sampling oscilloscope. Figure 6.2(a) shows a digital pattern [0100] repeated at $250MHz$, while figure 6.2(b) contains the pattern [01100101] at $125MHz$.

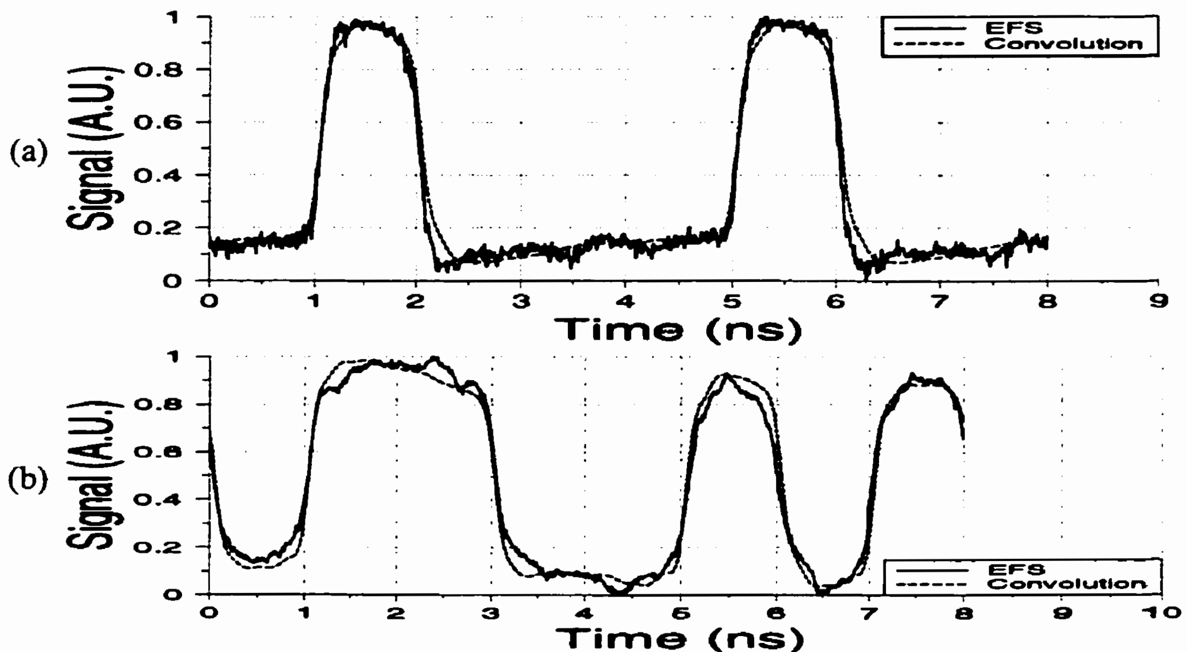


Figure 6.2: (a) A 1*Gb/s* digital pattern [0100] at 250*MHz* and (b) a 1*Gb/s* digital pattern [01100101] at 125*MHz* on a feed-through microstrip line measured by amplitude modulated EFS. The corresponding convolutions between the respective applied signals and the sampling pulse in figure 4.16 are also shown for comparison.

The slight discrepancies between the measured signals by EFS and the convoluted signals in figure 6.2 are mostly due to noise and cantilever mismatch. This noise will be examined in detail in the section 6.2.1.2. Minor mismatch against the multiple signal reflections initiated at the end of the Si_3N_4 cantilever causes disagreement in shapes of the measured signal from that of the respective convoluted waveforms.

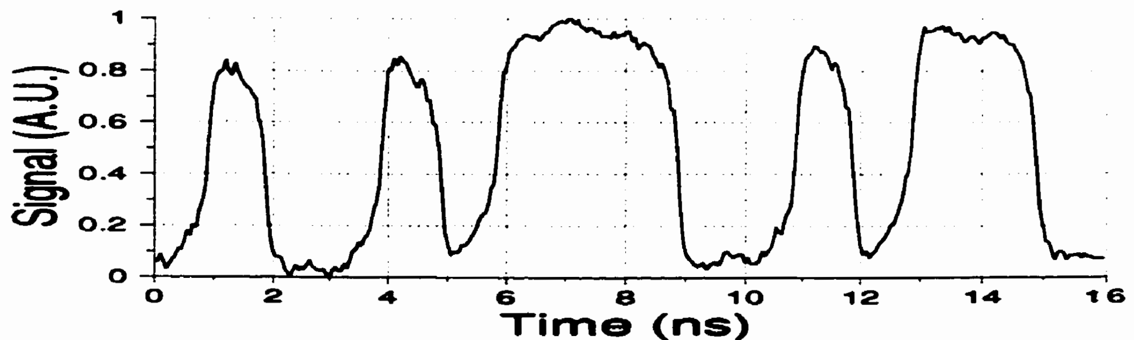


Figure 6.3: A 1*Gb/s* digital pattern [0100101110010110] at 62.5*MHz* on a ceramic transmission line measured by amplitude modulated EFS.

Measurement of the $1Gb/s$ signal on the ceramic microstrip line in figure 6.3 was obtained by changing the repetitive rate of the sampling pulse in figure 4.16 from $125MHz$ to synchronize with the signal under test at $62.5MHz$. The cable after the $20GHz$ coupler (see figure 4.15) was also changed for matching. The sampling resolution used was $100ps$.

6.2.1.2 Voltage Sensitivity

To experimentally determine the RMS noise in the instrument, a rising edge of a $125MHz$ digital signal on the ceramic transmission line is being studied.

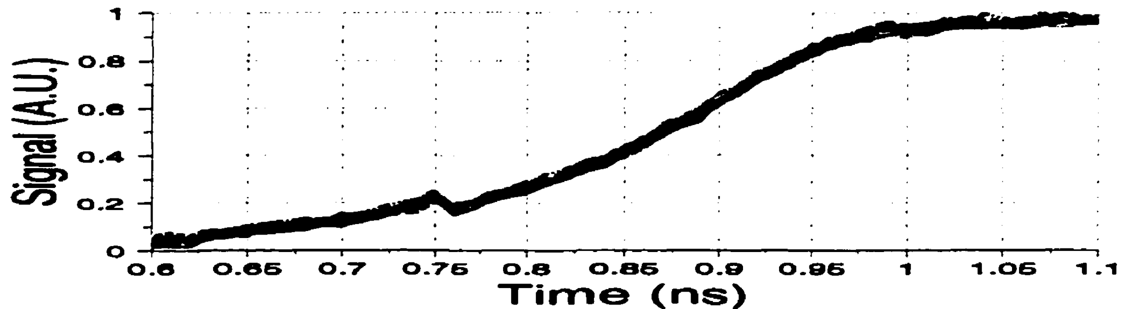


Figure 6.4: Measurement of a digital signal rising edge at $125MHz$ on a ceramic transmission line using amplitude modulated EFS is repeated 10 times under the same conditions.

Figure 6.4 shows the signal of interest reproduced 10 times using amplitude modulated EFS with all variables in the experiments being held constant. The sampling resolution was selected to be $10ps$. The experimental RMS noise was obtained by first collecting in total, 120 measured values from 12 different sampling locations: ($0.6ns$,$0.65ns$,$0.7ns$,$0.75ns$,$0.8ns$,$0.85ns$,$0.88ns$,$0.9ns$,$0.95ns$,$1ns$,$1.05ns$,$1.1ns$), with 10 values at each sampling time. The set of these 10 measured values at each of the sampling locations were then subtracted by their mean. Finally the RMS value of these 120 data points were calculated, which can equivalently estimate the experimental voltage sensitivity which was found to be $13mV$. Recalling from section 5.3.1, the theoretical voltage sensitivity was $20mV/\sqrt{Hz}$ with a rectangular pulse approximation for the sampling puise. Since the automation software averaged the data 1000 times over $1.25s$ at a sampling location, the measurement bandwidth B was $1/1.25s = 0.8Hz$. Thus, the expected voltage sensitivity is $18mV$. This is in excellent agreement with the experimental resolution of $13mV$,

considering that there are quite a few uncertainties or assumptions in the theoretical calculation. The obvious one is the capacitance derivative $\partial C(x, y, z)/\partial z$ which depends on the uncertain cantilever-circuit geometry. Another major cause of the minor disagreement from theory is the non-idealities of the sampling pulse, since the pulse was modelled as an ideal rectangular pulse in the theoretical computations. The last and somewhat hidden factor is the DC offset effects symbolized by $\Delta\Phi$, which was neglected in the derivations.

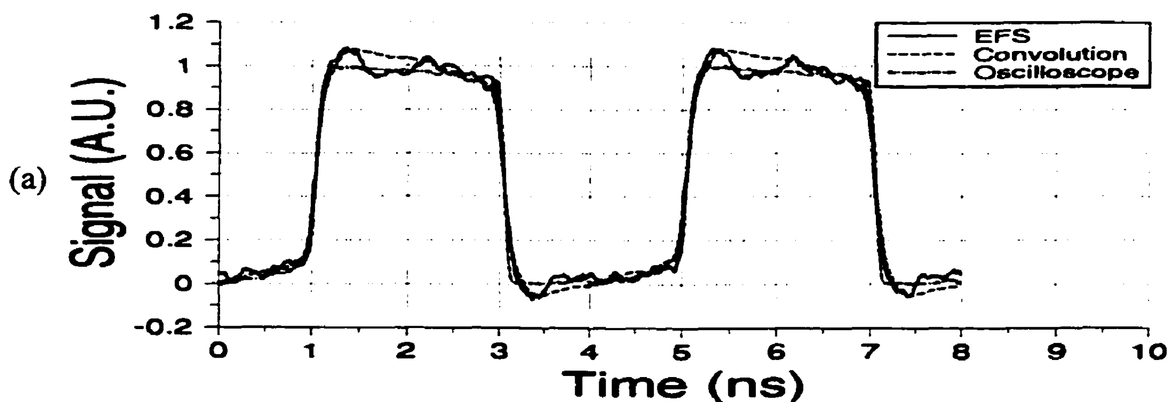
The experimental SNR is computed by dividing the amplitude of the signal in figure 6.4 with the experimental RMS noise, SNR=1/0.013=77. Since the signal under test had an amplitude of $1.5V$, the SNR is theoretically $50*1.5V/\sqrt{0.8Hz}$=84 using the calculations from section 5.3.1.

Figure 6.4 also shows impressive repeatability of the measurements using EFS. The 'bump' at $0.75ns$ reflects an error by the signal delay production of the HP generator.

6.2.1.3 Bandwidth

Figure 6.5(a) shows a measurement of a $0.5Gb/s$ digital signal at $250MHz$ on the feed-through microstrip line using EFS with a sampling resolution of $10ps$. This result was scaled and imposed onto figure 5.4 which displays the output of the line signal measured using a sampling oscilloscope and the convolution product between the sampling pulse in figure 4.16 and the signal at the oscilloscope. To resolve the bandwidth, the rising edges of these signals are examined in a zoomed view in figure 6.5(b). The EFS measured waveform was scaled to match its convolution counterpart.

(a)



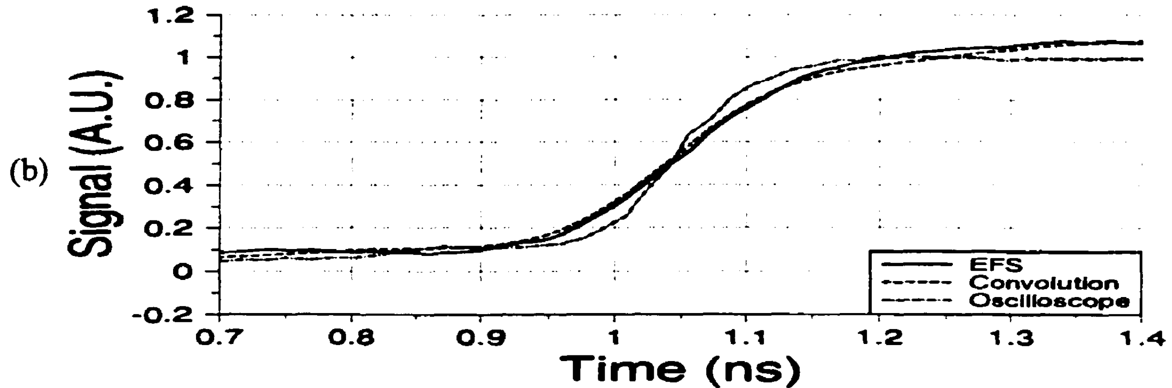


Figure 6.5: (a) A $0.5Gb/s$, $250MHz$ digital pattern on a ceramic transmission line measured by amplitude modulated EFS and a sampling oscilloscope. The convolution product between the applied signal and the sampling pulse is also shown for comparison. (b) Expanded version of (a) featuring the rising edges. The EFS result in (b) was processed with 7-pt smoothing.

Figure 6.5(b) shows a remarkable resemblance between the prediction by the convolution and the measured signal using EFS with a 7-point (pt) smoothing routine (provided by the graphing software RPlot). In fact, the 10-90% smoothed rise time measured by EFS is identical to the hypothesized rise time of $172ps$ if the low and high logic levels are defined as $A.U.=0.1$ and $A.U.=1$, respectively. Using equation (5.21), the experimental temporal noise ΔT is $1.9ps$ with $\varepsilon=13mV$, $dt=172ps$, and $dv=80\%\times1.5V$. Thus, evaluating (5.19) with $tr_{meas}=tr_{meas}+\Delta T$, the minimum bandwidth using amplitude modulation is about $3GHz$.

The noise is reduced in figure 6.5(a) from that in figure 6.2(a), although the same sampling resolution of $10ps$ was used. This is because the result was obtained using a Si_3N_4 cantilever in 6.2(a), while the silicon cantilever, which corresponds a better voltage sensitivity, was used for the measurement in figure 6.5(a).

6.2.1.4 Delay Resolution

By using the HP80000 data generator to introduce delays of 0, 10, 20, 50 and $100ps$ to a $125MHz$ digital signal on a ceramic transmission line, measurements of the leading edges of the signals with these initial delays using EFS at a sampling resolution of $10ps$ are shown in figure 6.6. These waveforms were processed with a 10-pt smoothing routine.

As discussed in section 5.5, the RMS amplitude noise can contribute to jitter. The

equivalent RMS jitter ΔT calculated earlier is only 1.9*ps*. The repeatability measurement in figure 6.4 suggests a peak-to-peak jitter of 11*ps*, which is indicated by the diameters of the circles in figure 6.6(b). It can be concluded that the dominant cause of this timing inaccuracy is the typical RMS jitter of 10*ps* by the HP generator.

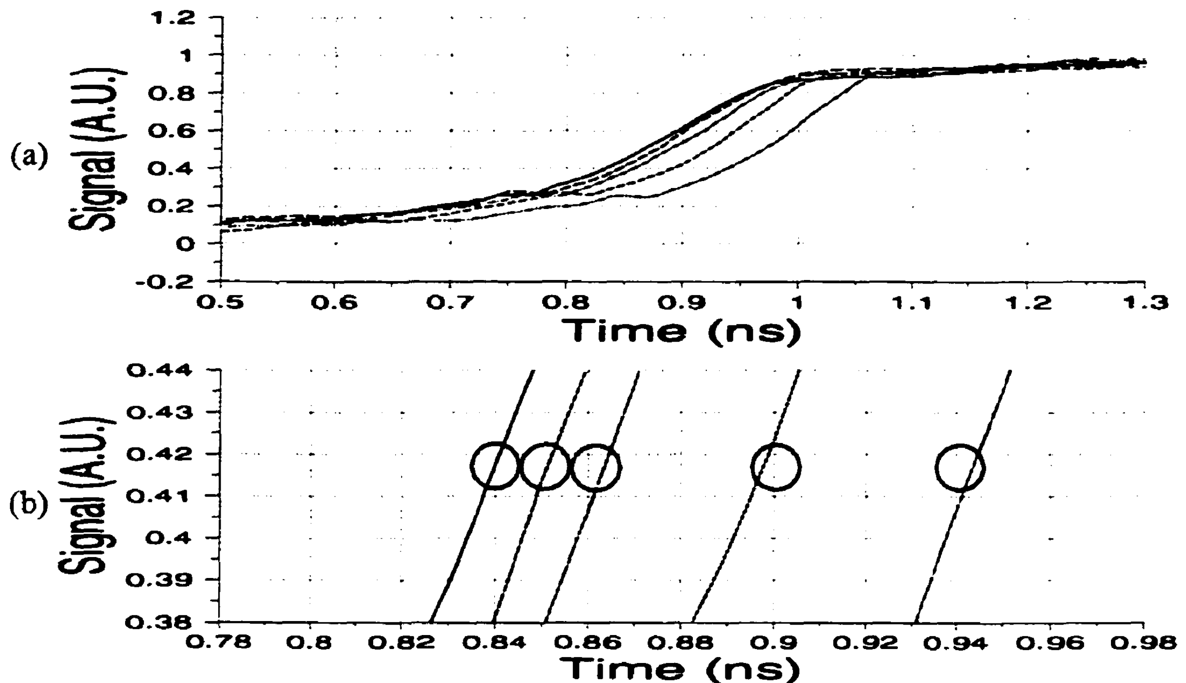


Figure 6.6: (a) Rising edges of 5 digital signals on a ceramic transmission line at 125*MHz* with delays of 0, 10, 20, 50 and 100*ps*, respectively, measured by using amplitude modulated EFS. (b) Expanded version of the delays in (a). The centres of the circles in (b) indicate the expected delay, and the diameter of the circles represents peak to peak jitter suggested by figure 6.4.

6.2.2 Pulse Width Modulation

Two 1*Gb/s* digital patterns were measured on the ceramic transmission line using pulse width modulated EFS. These measurements displayed in figure 6.7 are compared with their corresponding scaled convolutions between the respective actual ceramic line signals and the virtual sampling pulse in figure 4.21 produced using a modulation depth of 50*ps*. The sampling resolution used was 10*ps* in figure 6.7(a) and 100*ps* in figure 6.7(b). The disparities between the convoluted signals and the corresponding EFS measurements are mostly due to noise and minor cantilever mismatch.

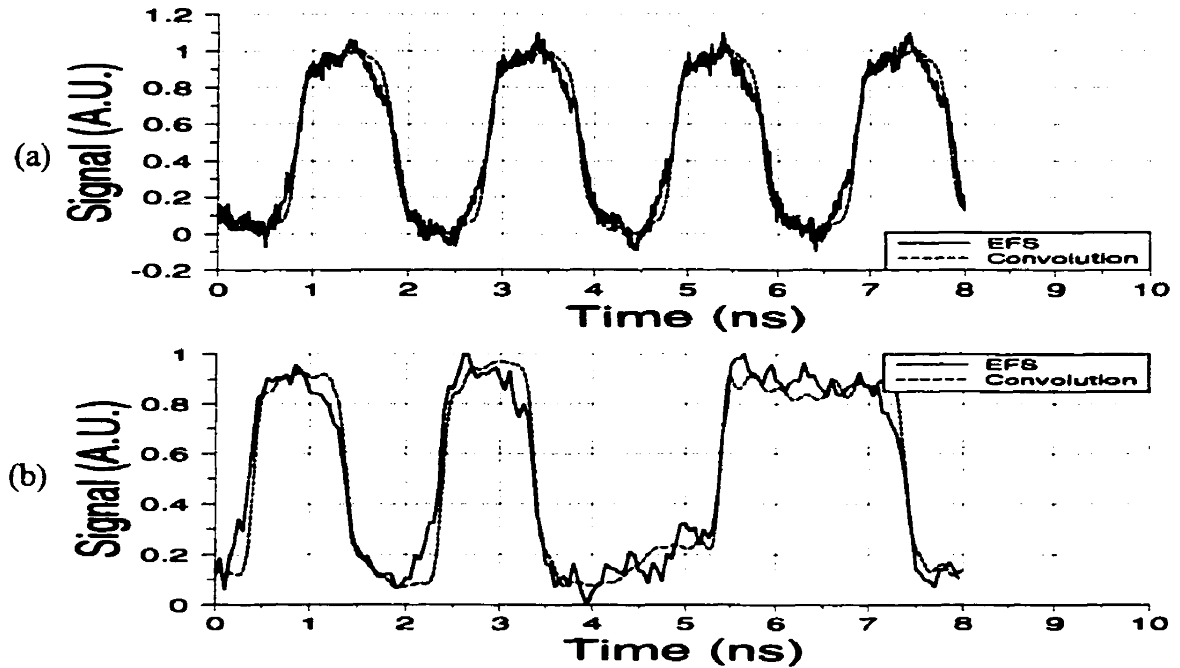


Figure 6.7: (a) A $1Gb/s$, $500MHz$ digital pattern, and (b) a $1Gb/s$ digital pattern [10100110] at $125MHz$ on a ceramic transmission line measured by pulse width modulated EFS with a modulation depth of $50ps$. The corresponding convolutions between the respective applied signals and the effective sampling pulse in figure 4.21 are also shown for comparison.

Figure 6.8 presents a measurement of a $0.5Gb/s$, $250MHz$ digital pattern using a modulation depth of $250ps$ and a sampling resolution of $50ps$. The slight disagreement with the supposedly matching convolution between the effective sampling pulse in figure 4.20 and the actual signal on the ceramic line is mostly due to minor probe mismatch.

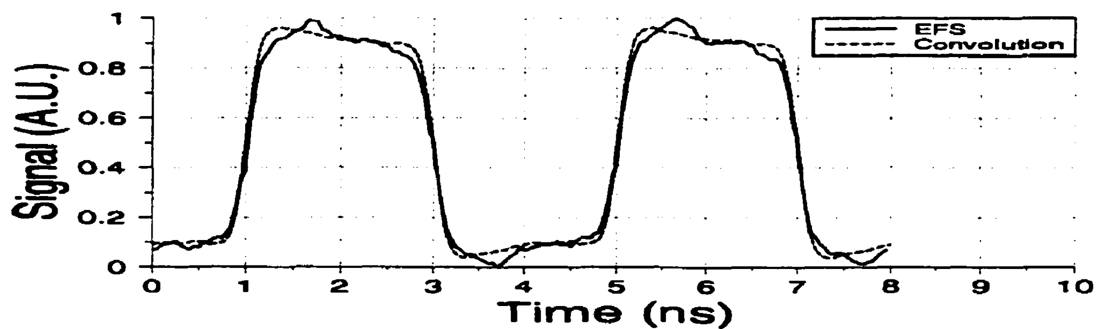


Figure 6.8: A $0.5Gb/s$, $250MHz$ digital pattern on a ceramic transmission line measured by EFS (pulse width modulation with modulation depth of $250ps$). The convolution product between the applied signal and the effective sampling pulse in figure 4.20 is also shown for comparison.

The calculations in section 5.3 foretold the poorer SNR and voltage sensitivity for pulse width modulation than those for amplitude modulation in this work. This fact is apparent when the results in figure 6.7(a) and figure 6.5(a) are being compared. This increase in amplitude error for pulse width modulation also damages the temporal accuracy of the EFS instrument, ΔT.

Similar to the methodology in section 6.2.1.3, the bandwidth for pulse width modulation is explored by studying the rising edge of a 0.5*Gb/s* digital signal at 250*MHz*. Figure 6.9 demonstrates EFS measurement of this signal using a modulation depth of 50*ps*. A sampling resolution of 10*ps* was used.

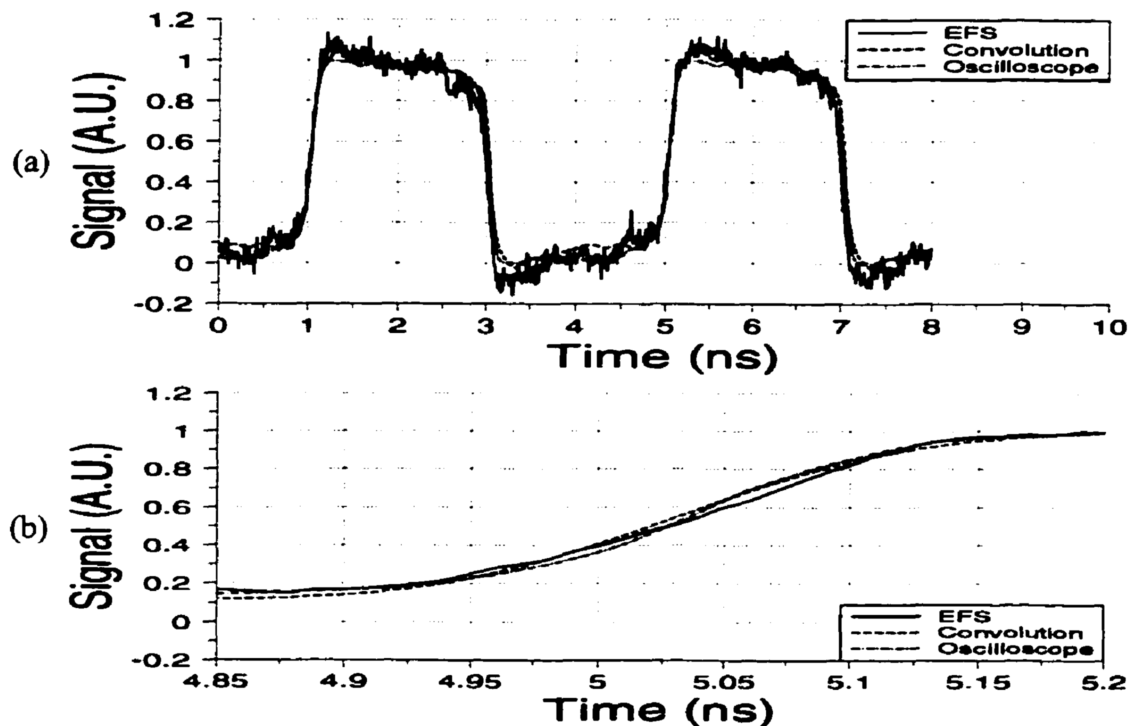


Figure 6.9: (a) A 0.5*Gb/s*, 250*MHz* digital pattern on a ceramic transmission line measured by pulse width modulated EFS with a modulation depth of 50*ps*, and a sampling oscilloscope. The convolution product between the applied signal and the sampling pulse in figure 4.21 is also shown for comparison. (b) Expanded version of (a) featuring the rising edges. The EFS result in (b) was processed with 14-pt smoothing.

The signal measured by EFS in figure 6.9 obeys both the actual applied signal and the convolution between the real signal and the effective sampling pulse after proper scaling. The rise time of the 14-pt smoothed EFS signal in figure 6.9(b) is 180*ps* if the low logic is

$A.U.$=0.1 and the high logic is $A.U.$=1. This transistion time may however be sensitive to the temporal noise as noted in section 5.5. With a measurement bandwidth of B=0.8Hz, the theoretical voltage sensitivity is $93mV(\sqrt{0.8Hz})=83mV$. Using the measured 10%-90% rise time of 180ps by EFS for a 1.5V signal, the expected temporal noise calculated by equation (5.22) is 13ps. The difference between the rise time measured by EFS and the rise time of the actual or convoluted signal is less than this noise. Nonetheless, the bandwidth can be deteriorated by this timing uncertainty. Suppose that the maximum rise time measured by pulse width modulated EFS is $tr_{meas}+\Delta T=180ps+13.0ps=193ps$, the minimum bandwidth of EFS using pulse width modulation in this work is approximately 4.15GHz using equation (5.19) for a modulation depth of 50ps. This is consistent with the estimation of 4.4GHz by equation (5.18).

6.3 Measurements on a 0.5µm CMOS Circuit

To investigate more practical capabilities of the proposed technique, measurements were performed on a 0.5μm CMOS inverter chain. A photograph and the equivalent schematic of the integrated circuit is shown in figure 6.10.

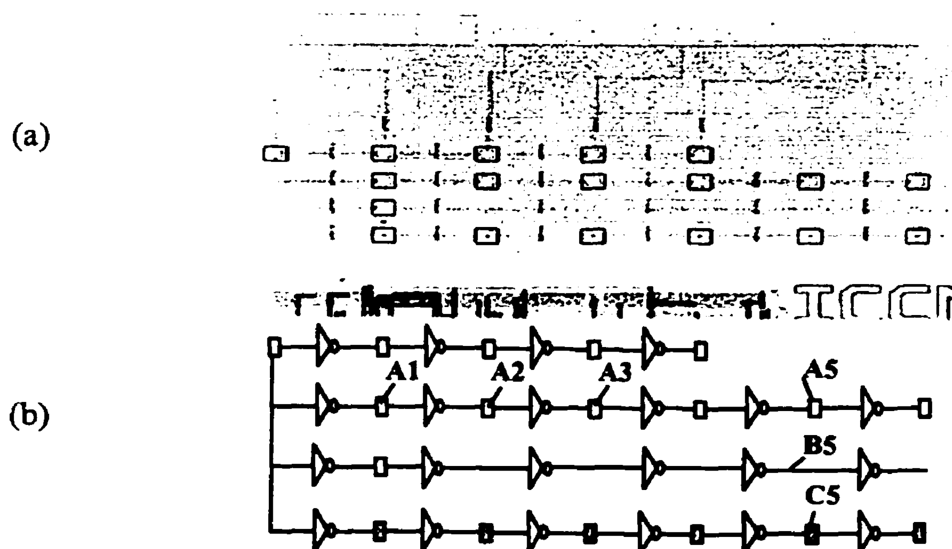


Figure 6.10: (a) A microphotograph and (b) a schematic diagram of the 0.5μm CMOS inverter chain. Measurements were conducted at sites A1, A2, A3, A5, B5, and C5. Sites A1, A2, A3, and A5 are 20x20μm^2 unpassivated probing pad. Site B5 is a 1.2μm passivated interconnect, and site C5 is a 20x20μm^2 passivated probing pad.

The circuit contains four rows of inverter chains. All inverters are connected with 1.2μm interconnects. The top two rows have 20x20μm^2 unpassivated probing pads between every two inverters. The third and fourth row of inverters are mostly passivated. Passivated 20x20μm^2 probing pads are between inverters in the bottom chain. The power supply of the CMOS circuit is 3.3*V* and 0*V*. The packaged circuit was mounted onto a printed circuit board with a 50Ω microstrip line [72] to transport the high speed digital input signal into the chip.

6.3.1 Pattern Extraction

Using a sampling resolution of 100*ps*, measurement of a 125*MHz* signal at site A3 indicated in figure 6.10(b) using amplitude modulated EFS is exhibited in figure 6.11(b).

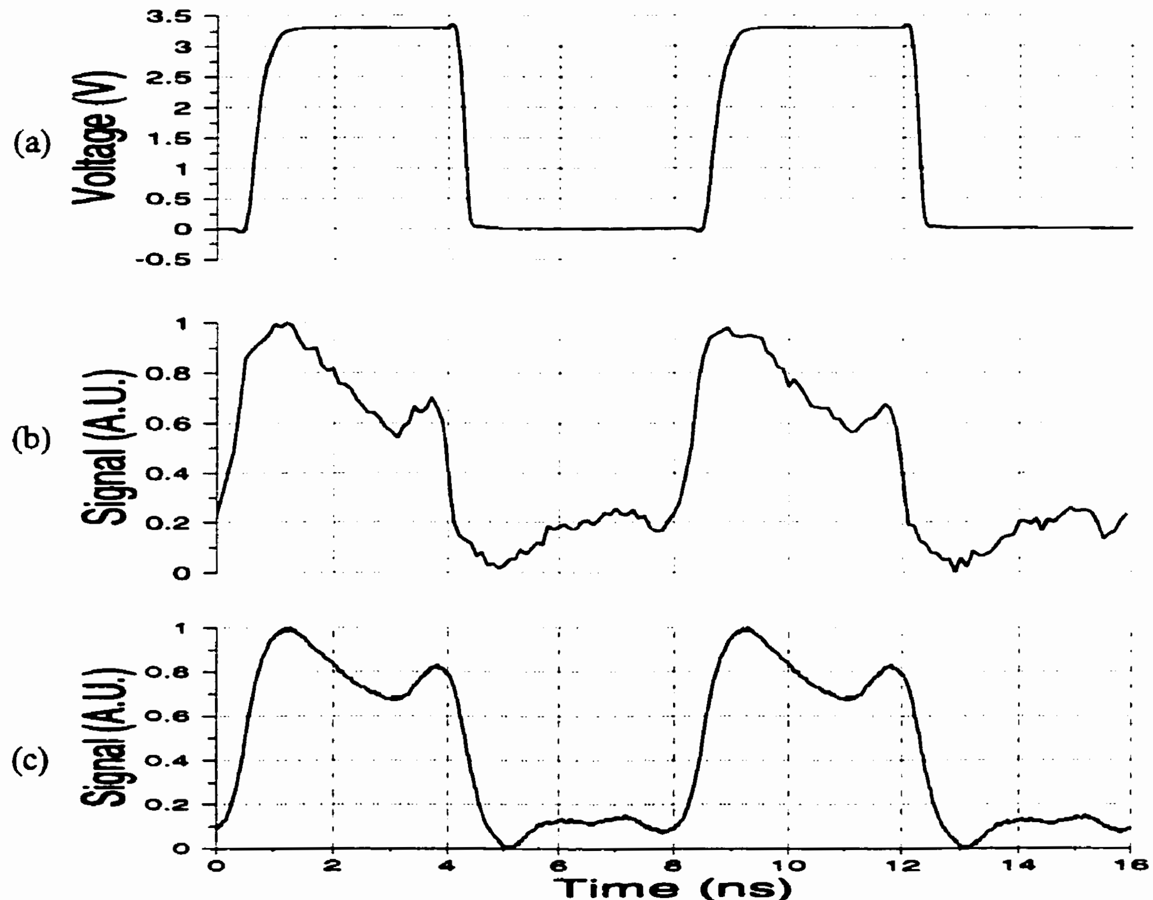


Figure 6.11: (a) Simulation of a 250*Mb/s*, 125*MHz* digital signal at site A3 of the 0.5μm CMOS inverter chain using Cadence HspiceS. (b) Measurement of the 125*MHz* signal by amplitude modulated EFS and (c) contact probe.

The simulated waveform of the 125*MHz* signal from the circuit schematic with in-circuit parasitics at site A3 using Cadence HspiceS is also provided in figure 6.11(a) along with the measurement of the digital signal using the 1*GHz* contact Picoprobe described in section 2.1.3. The congruity of the signals measured by EFS and the contact probe in figure 6.11(b) and (c), respectively, suggests the actual waveshape of the digital signal in the circuit. These measurements are quite different from simulation because the 50Ω output drivers of the inverter chain attempt to pull down the power supply, but they were not included in the schematic used by simulation. It is also primarily because of non-idealities of the sampling signal, the absence of a shunt capacitor in the power supply path, and the parasitics introduced by the bondwires in the circuit package.

The 10%-90% rise and fall time of the simulated signals are 230*ps* and 115*ps*, respectively, while EFS estimated these transitions to be approximately twice the simulated values. Even though the Cadence HspiceS simulation included parasitics inherited by those such as interconnect lines and probing pads, the 50Ω drivers excluded in the simulation may affect the rise and fall times of the circuit signals. The length of the bondwires in the packaging is possibly the major cause for limiting the signal bandwidth. Assessment of the true signal transition times from the measured signals involve conjecture because of the severity of the non-idealities present in these waveforms. Thus, signals in this CMOS inverter chain cannot be used to accurately deduce the bandwidth of the EFS instrument. In addition, convolution between the simulations and the sampling pulse cannot predict the measured signals in the intermediate stages of the inverter chain by EFS due to the non-idealities caused by the incompatibility between the simulation and actual circuitry.

One of the most practical advantages of EFS over many other internal diagnostic techniques is its ability to measure integrated circuits over passivation. To demonstrate this, EFS measurements were performed at sites A5, B5, and C5, with sites B5 and C5 being passivated sites. The signals at these three sites should have similar waveshapes because of circuit geometry. Since the third row of the inverter chain has 4 fewer probing pads than the second and fourth rows, the signal should arrive earlier at site B5 than at sites A5 and C5. Yet, HspiceS simulations revealed this timing difference to be only 20*ps*. In another words, the extra delay introduced by a $20 \times 20 \mu m^2$ probing pad can be assumed negligible. Figure 6.12 presents measurements of a 250*MHz* digital signal at the three designated sites

using amplitude modulated EFS with a sampling resolution of 50*ps*. A 5-pt smoothing routine was applied to these results. Seeing that the signal at site B5 has approximately the same transistion characteristics as those at sites A5 and C5, the extra loading introduced by the probing pads is also insignificant.

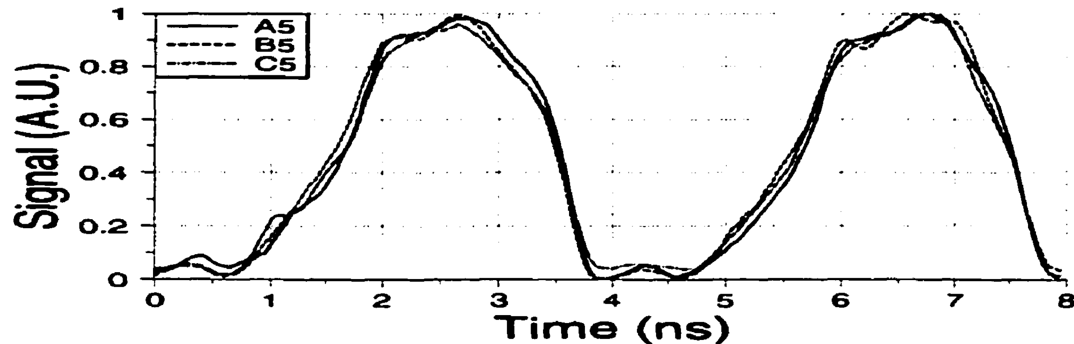
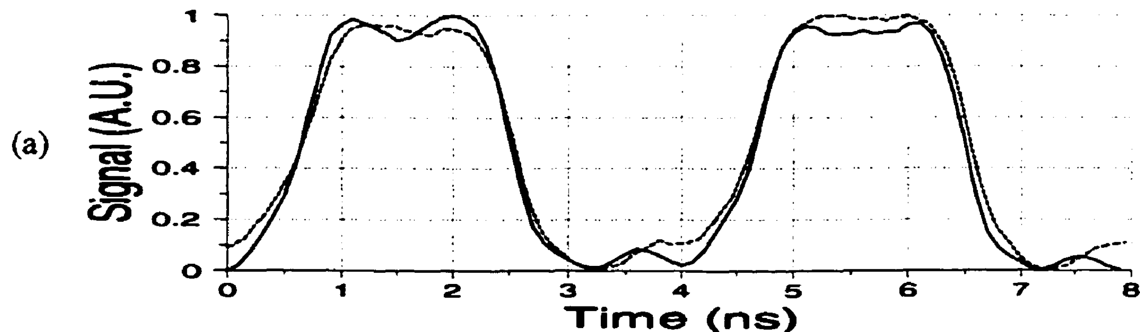


Figure 6.12: Digital signals of 0.5*Gb/s* at 250*MHz* measured using amplitude modulated EFS at sites A5, B5, and C5 of the CMOS inverter chain. Site A5 is unpassivated, and sites B5 and C5 are under passivation.

Figure 6.12 also gives partial information about spatial resolution. The signal transitions and waveshape measured on a 1.2μm passivated interconnect by EFS is found to be similar to those measured on the 20x20μm^2 unpassivated pad. This implies that the EFS instrument in this work is capable of measuring a stand-alone 1μm interconnect line on a passivated CMOS circuit.

Two separate packaged dies of the identical CMOS inverter design were measured to demonstrate the consistency of measurements, design, and fabrication. Figure 6.13 shows measurement of a 250*MHz* digital signal at sites A1 and A2 using amplitude modulated EFS with a sampling resolution of 100*ps*. The signal at A1 was inverted to that at A2 by an inverter. A 5-pt smoothing routine was applied to the waveforms in figure 6.13.

(a)



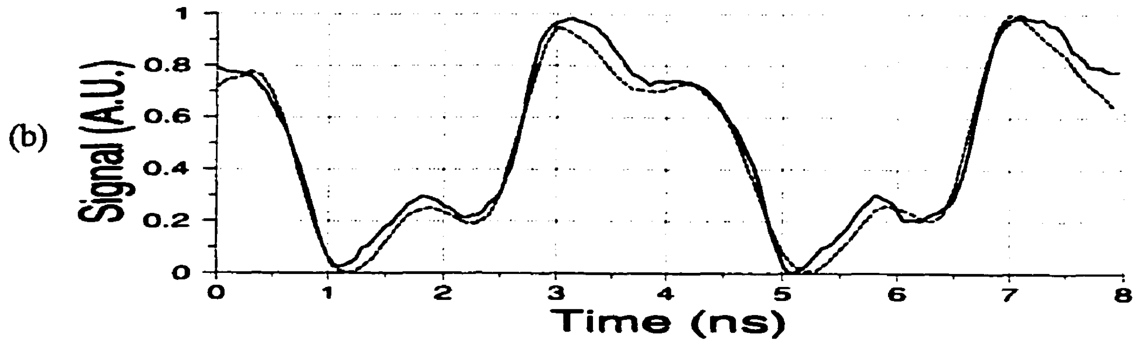


Figure 6.13: Measurement of a 0.5*Gb/s*, 250*MHz* digital signals at sites (a) A1 and (b) A2 on two different packaged dies with identical designs of the CMOS inverter chain using amplitude modulated EFS.

To determine the impact of an AC draining capacitor in the power supply path, a 1*nF* surface-mount capacitor was added in shunt with the positive DC bias path on the printed circuit board, which holds the packaged CMOS circuit. Figure 6.14 shows 'before and after' measurements with 5-pt smoothing of a 250*MHz* digital signal at sites A1 and A2 using pulse width modulation, with both the modulation depth and the sampling resolution being 50*ps*. The measurements of the circuit with the 1*nF* capacitor show slight improvements from the signals in the circuit without the extra capacitor.

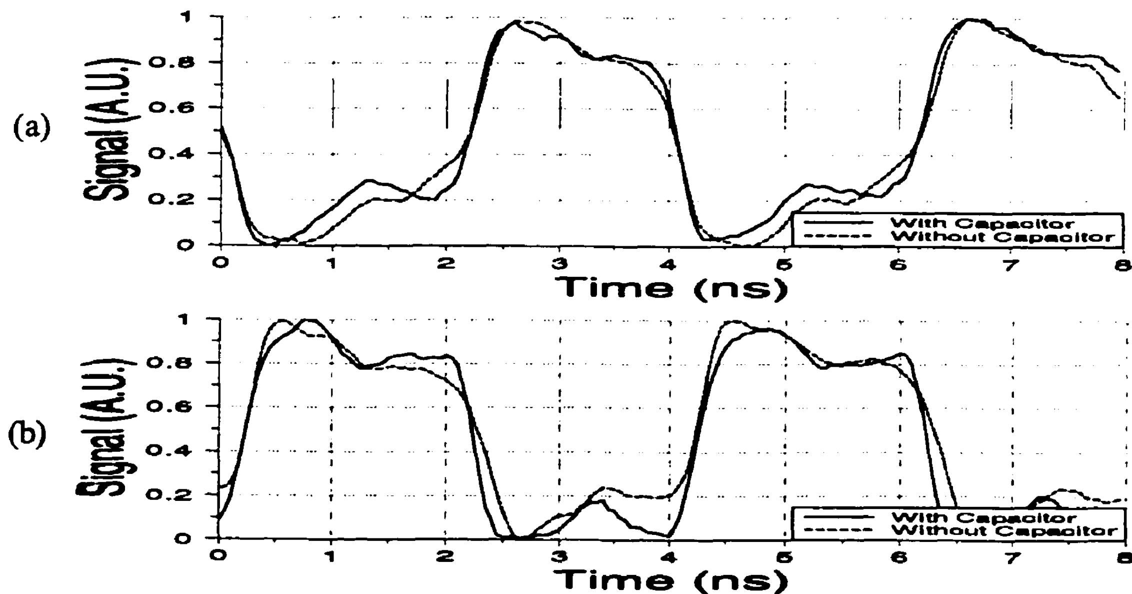


Figure 6.14: Measurement of a 0.5*Gb/s*, 250*MHz* signal at sites (a) A1 and (b) A2 of the CMOS inverter chain with and without a bias capacitor using pulse width modulated EFS with a modulation depth of 50*ps*.

6.3.2 Voltage Sensitivity

The experimental noise in the measurements of the CMOS integrated circuit using EFS is evaluated following a similar fashion as in section 6.2.1.2. Figure 6.15 demonstrates measurement of a *0.5Gb/s*, *250MHz* digital pattern repeated 10 times at site A1 of the CMOS inverter chain without the $1nF$ bias capacitor using amplitude modulated EFS. A sampling resolution of $100ps$ was used.

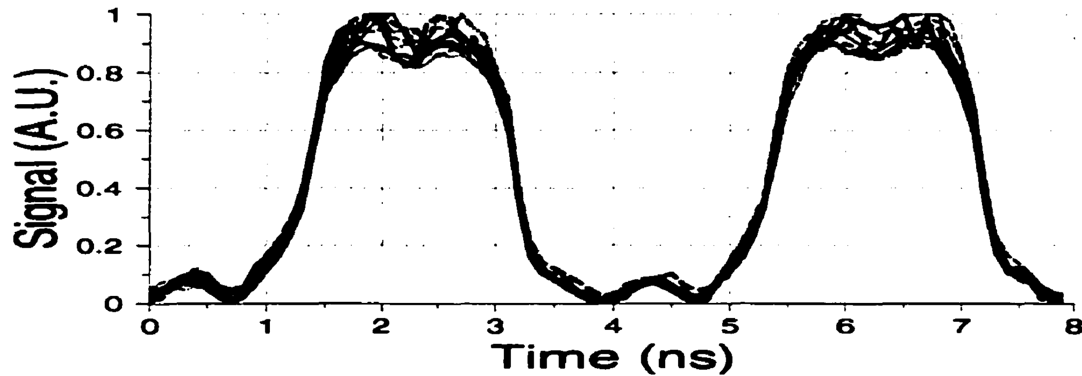


Figure 6.15: Measurement of a *0.5Gb/s*, *250MHz* digital pattern at site A1 of the CMOS inverter chain repeated 10 times using amplitude modulated EFS under the same conditions.

A set of 10 measured values were collected and are subtracted by the mean of these values from each of the 10 different sampling locations selected from the results in figure 6.15: ($1ns$,$1.4ns$,$2ns$,$3ns$,$3.2ns$,$4ns$,$5ns$,$6ns$,$7ns$). Thus, 100 data points were gathered to determine the RMS noise from the measured waveforms. This noise was found to be $32mV$ which is worse than $13mV$ obtained from the ceramic transmission line. There are two important factors that are different when measuring integrated circuits as supposed to measuring the ceramic transmission line. The first is the capacitance derivative $\partial C(x, y, z)/\partial z$ which is a doubtful parameter. In fact, using a parallel plate capacitor model, $\partial C(x, y, z)/\partial z$ is proportional to the area under test ($20 \times 20 \mu m^2$ unpassivated pad) which is much smaller than the area of the transmission lines used in section 6.2. Accordingly the voltage resolution should be poorer when measuring the integrated CMOS inverter chain, as proposed by equation (5.11) or (5.17).

Another factor which was omitted for simplicity in the theoretical derivation of the voltage sensitivity, but is an essential element to consider for probing integrated circuits is

the DC offset effects represented by the term $\Delta\Phi$. Signals on the adjacent interconnects can interfere with the signal being measured by parasitic coupling, and by changing the local surface charge on the circuit, and both affects the term $\Delta\Phi$. This surface charge is also subjected to environmental conditions such as humidity, surface defects, and contamination. As a result, $\Delta\Phi$ is perhaps more unpredictable than $\partial C(x, y, z)/\partial z$. This also implies that absolute voltage measurements are extremely difficult using EFS because of these surface charging effects. Due to these predicaments associated with the two factors $\partial C(x, y, z)/\partial z$ and $\Delta\Phi$, the voltage resolution for measuring integrated circuits is expected to be worse than the one obtained from the measurements of the transmission lines.

The erratic term $\Delta\Phi$ changes rapidly during the initial charging of the integrated circuit surface by the power supply. Such charging may cause the amplitude levels of the measured waveforms by EFS to drift. Therefore, it is desired to grant time for this surface charging to complete before conducting any measurements. The automation software used for these experiments commands the HP generator to supply the circuit signal for a period of time before sampling to avoid measurement during the charging.

The noise appears to be larger at the high logic level of the measured signal than that at the low logic level. This may be related to unstable fluctuations in the $3.3V$ power supply caused by the 50Ω output drivers and the DC offset effects $\Delta\Phi$.

6.3.3 Propagation Delay

Figure 6.16 demonstrates the propagation delay through the second row of the CMOS inverter chain by presenting normalized measured signals at sites A1, A3, and A5 with a $250MHz$ input. The CMOS circuit used did not have the $1nF$ AC draining shunt capacitor at the power supply path. The sampling resolution used was $50ps$, and a 5-pt smoothing routine was applied to all EFS waveforms. Delay between each of the two signals is for two inverters, and they are taken from the fall times of the signals at $A.U.$=0.4. Table 6.1 displays the propagation delays estimated by the various testing techniques, and these delays are compared with simulation. The simulated delays were acquired from the fall transitions at the half amplitude of $1.65V$ in figure 6.16(a).

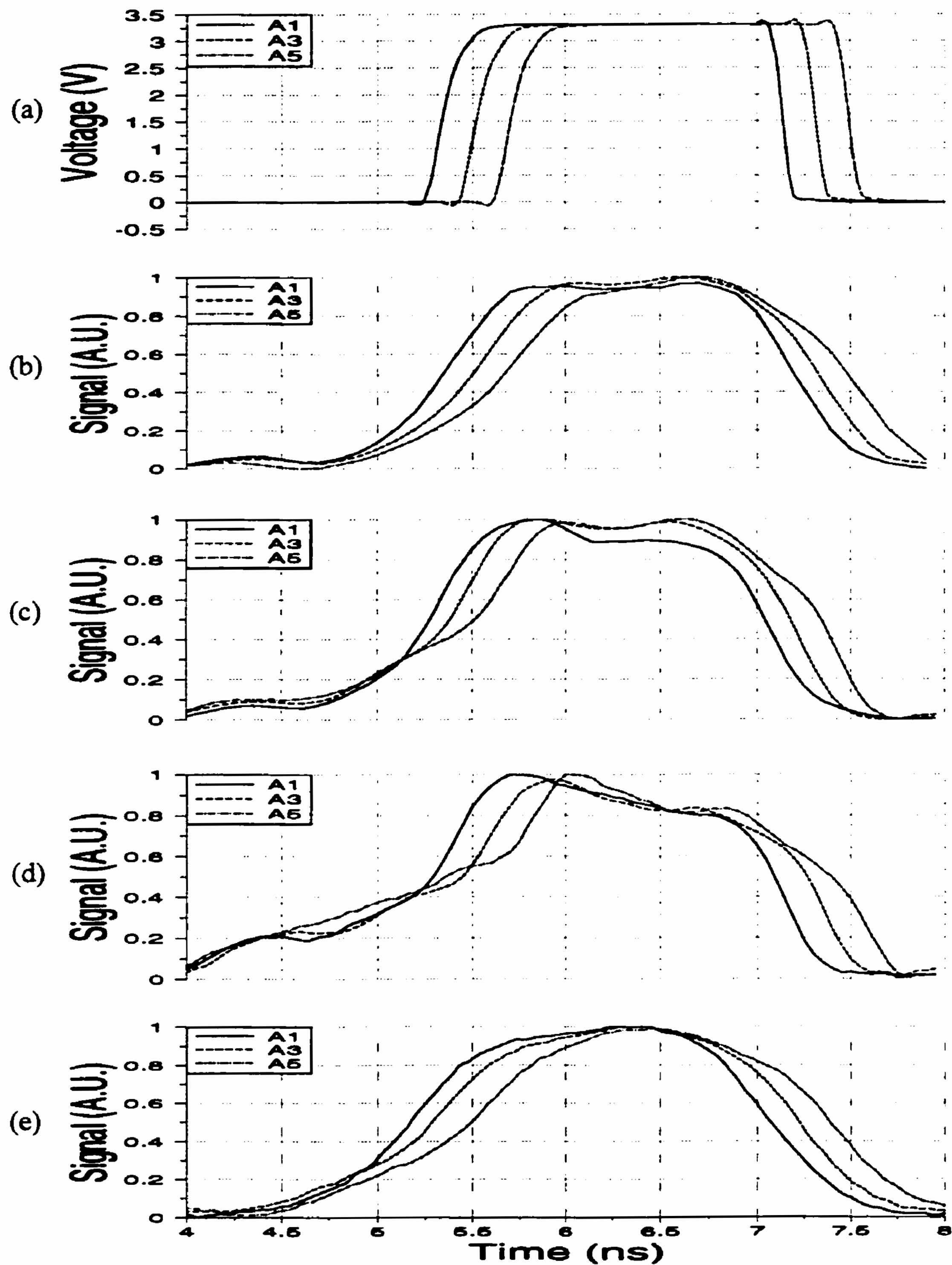


Figure 6.16: Measurements of a 0.5*Gb/s*, 250*MHz* digital pattern at sites A1, A3 and A5 of the CMOS inverter chain. Results were obtained from (a) Cadence HspiceS simulation, (b) amplitude modulated EFS, (c) pulse width modulated EFS with a 250*ps* modulation depth, (d) pulse width modulated EFS with a 50*ps* modulation depth, and (e) contact probe.

	A1 to A3	A3 to A5	Average for 2 inverters	Average for 1 inverter
Simulations	175*ps*	175*ps*	175*ps*	88*ps*
Amplitude modulation	175*ps*	170*ps*	172*ps*	86*ps*
Pulse width modulation (250*ps* modulation depth)	140*ps*	160*ps*	150*ps*	75*ps*
Pulse width modulation (50*ps* modulation depth)	175*ps*	175*ps*	175*ps*	88*ps*
Contact probe	140*ps*	165*ps*	152*ps*	76*ps*

Table 6.1: Estimations of the propagation delays in the second row of the CMOS inverter chain by various measurement techniques versus the simulated values.

The measurements by pulse width modulation with a 50*ps* modulation depth in figure 6.16(d) possess the most non-idealities likely because of the violent ripples adjacent to the effective sampling pulse in figure 4.21. The minor inconsistency between these measured propagation delays are largely due to temporal noise in the EFS instruments and jitter from the HP generator as both should contribute a combined error of at least 10*ps*.

6.4 Measurements on a NT25 Pulse Generator

This section presents and examine measurements of a pulse generator fabricated in Nortel's NT25 technology. The schematic and layout of the NT25 circuit are displayed in figure 6.17. This circuit generates pulses using NAND circuitry. Inverters before the NAND gate are for adjusting the delays of the two signals entering the gate to produce a narrow pulse. Inverters after the NAND gate are for driving the signal to a 50Ω load. Measurements were performed at four different locations within the NT25 circuit which was match terminated at its output. Sites A and B are 3μm passivated interconnects that carries the signals into the NAND gate. Sites C and D are 10x10μm^2 unpassivated probing

pads at the output of the NAND gate and at the end of the three inverter-drivers, respectively. The input of the NT25 circuit can be a square wave signal at any frequencies between 100 to 500*MHz*.

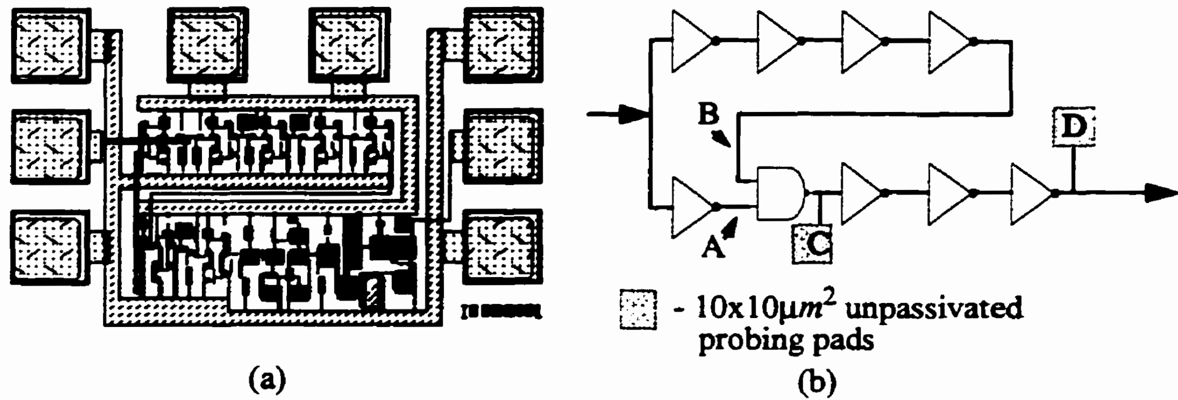
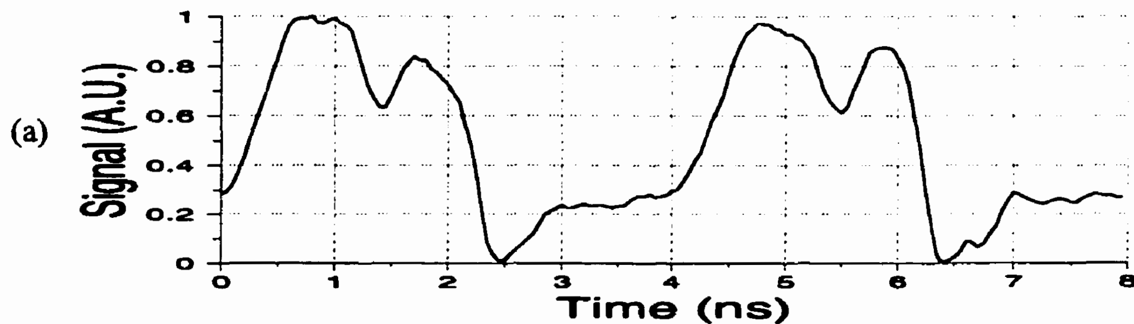


Figure 6.17: (a) Layout and (b) schematic of the NT25 pulse generator. Various measurements were performed on passivated interconnects at sites A and B, and on 10x10μm^2 unpassivated pads at sites C and D.

Figure 6.18(a) and 6.19(a) shows the measured signals at 250*MHz* on passivated sites A and B using amplitude modulated EFS, respectively. To reassure the waveshapes of these signals, measurements were conducted at these locations with a square wave input of 125*MHz* driven into the circuit, as exhibited in figure 6.18(b) and figure 6.19(b). A sampling resolution of 100*ps* was used for these measurements, and a 5-pt smoothing routine was applied to these waveforms to reduce noise. The non-idealities in these measured waveforms may be caused by power supply bounces induced by bondwire parasitics and other design related issues. Large inductances from the bondwires can cause large overshoot after a signal transistion (i.e. $v=Ldi/dt$). The bondwires in the actual packaged circuit have lengths of 4*mm*, while the designer anticipated these lengths to be only 2*mm*.



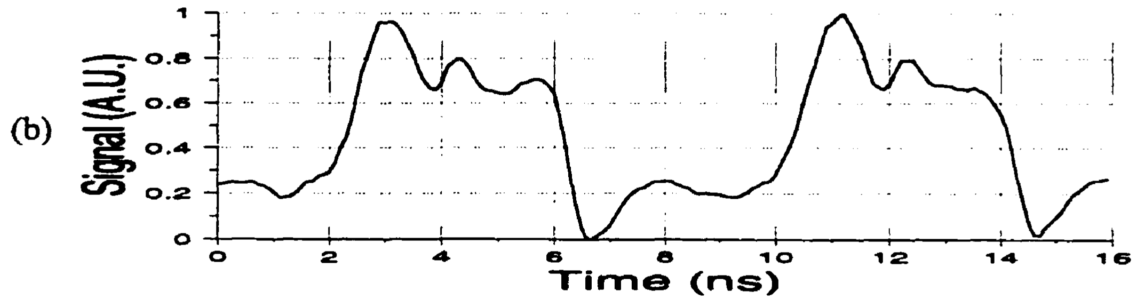


Figure 6.18: Measurements on site A of the NT25 pulse generator at a frequency of (a) 250*MHz* and (b) 125*MHz* using amplitude modulated EFS.

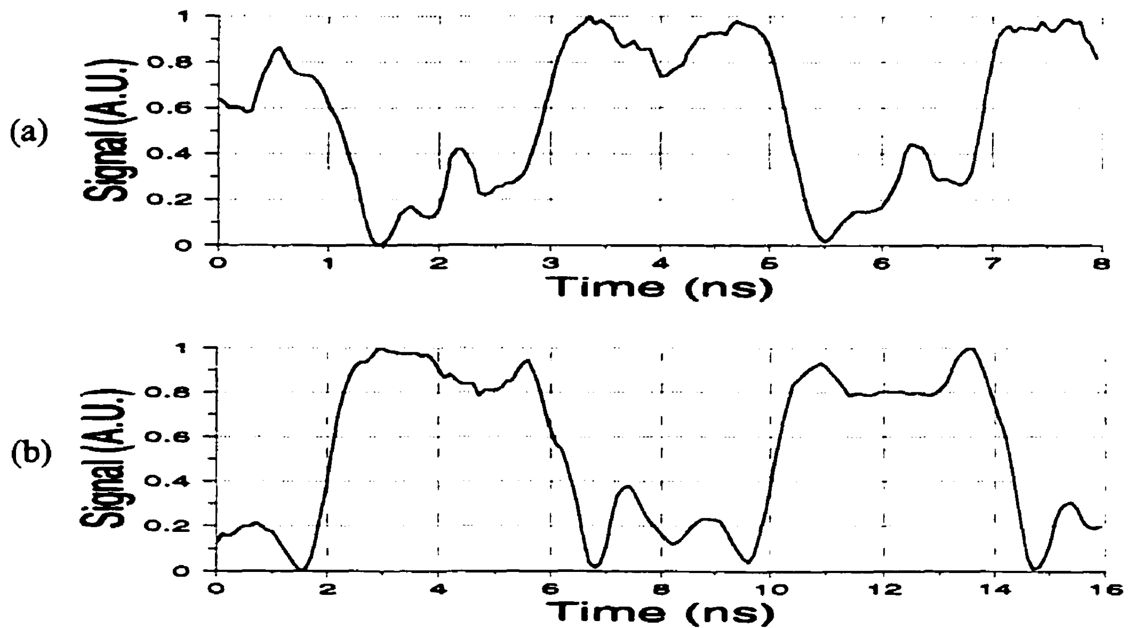


Figure 6.19: Measurements on site B of the NT25 pulse generator at a frequency of (a) 250*MHz* and (b) 125*MHz* using amplitude modulated EFS.

The immediate output of the NAND circuitry is examined by measuring site C on the NT25 circuit. Figure 6.20 compares the measurements of the 250*MHz* signal conducted using amplitude modulated EFS and pulse width modulation EFS with a modulation depth of 50*ps*. The sampling resolution of 100*ps* was used, and the resulted signals were refined by 5-pt smoothing. The two measured waveforms by both methods were scaled such that their logic levels coincides with one another. Both modulation schemes concluded with the same rise and fall times of 200*ps* using a low logic level of $A.U.=0$ and a high logic level of $A.U.=0.8$.

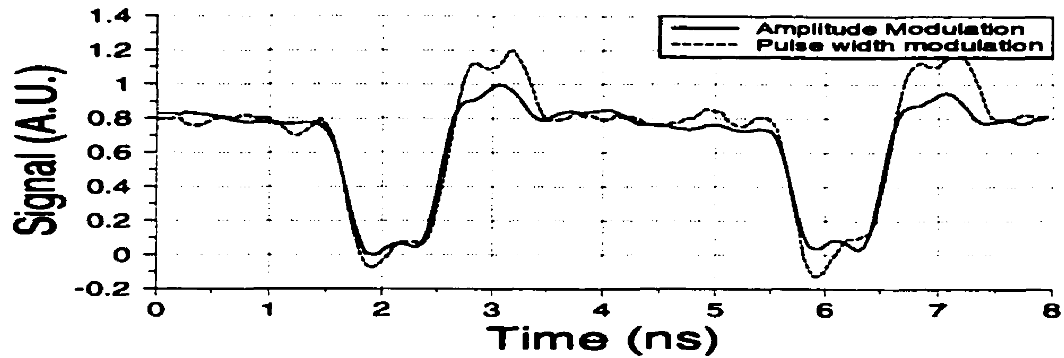


Figure 6.20: Measurements on site C of the NT25 pulse generator at a frequency of 250*MHz* using amplitude modulated EFS and pulse width modulated EFS with a modulation depth of 50*ps*.

Lastly the output of the pulse generator is determined and displayed in figure 6.21(a) which contains EFS measurements of the NT25 circuit on site D at an operating frequency of 250*MHz*. Measurement using the contact probe on site D, and the sampling oscilloscope at the output of the packaged circuit are also provided in figure 6.21(b). The FWHMs of the pulse generated by the NT25 circuit approximated by each technique are collected into table 6.2. The measured waveforms by both modulation schemes of EFS were scaled to each other according to their logic levels which are *A.U.*=0.2 and *A.U.*=1. The FWHMs of the measured signals are estimated at *A.U.*=0.6. The bandwidth of the signals are mostly limited by the bondwires in the package.

	10-90% rise	10-90% fall	FWHM
Amplitude modulation	250*ps*	300*ps*	465*ps*
Pulse width modulation (mod. depth=50*ps*)	300*ps*	235*ps*	455*ps*
Contact probe	400*ps*	400*ps*	800*ps*
Sampling scope	244*ps*	220*ps*	470*ps*

Table 6.2: Estimations for the FWHM and transition times of the generated pulses by the NT25 pulse generator using various measurement techniques.

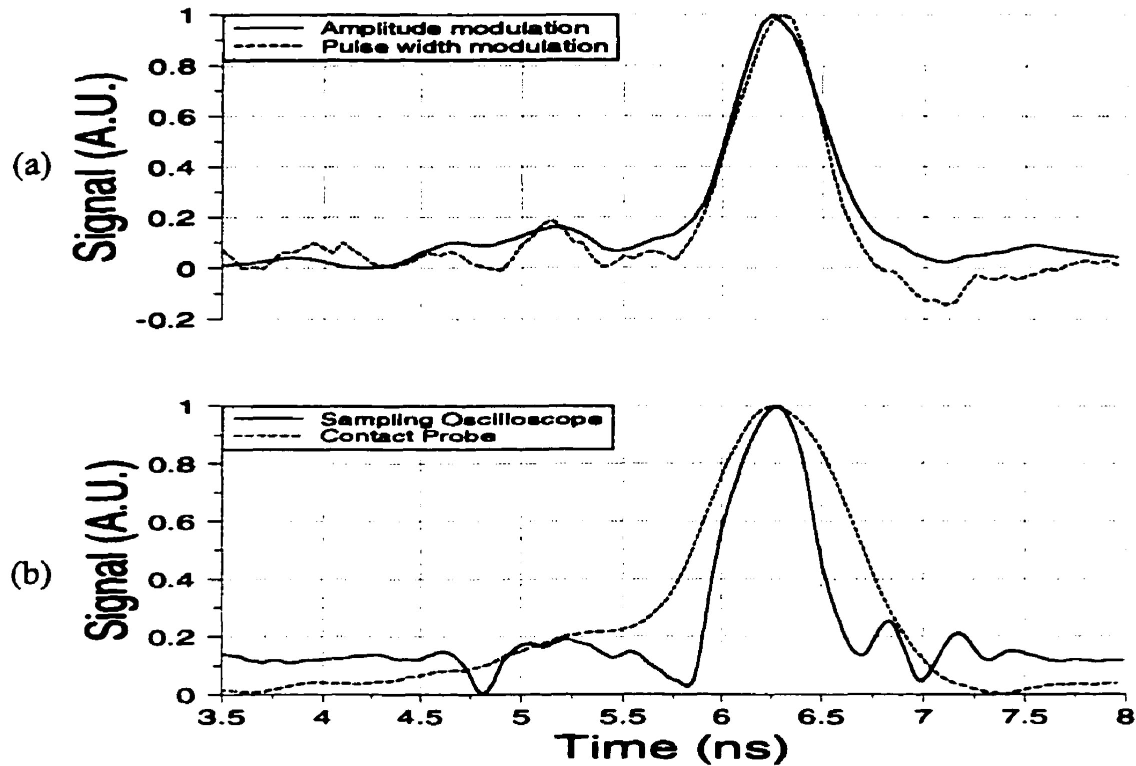


Figure 6.21: Measurements on the output of the NT25 pulse generator at an operating frequency of $250MHz$. Results were obtained at site D using (a) amplitude modulated EFS and pulse width modulated EFS with a $50ps$ modulation depth. (b) Measured waveforms by contact probe at site D and a sampling oscilloscope measured at the output of the packaged circuit.

The EFS estimations of the transition times and FWHM displayed in table 6.2 almost replicated with those measured by a sampling oscilloscope. The cause of the small discrepancies is the thermal noise in the EFS instrument and the non-idealities of the effective sampling pulses. The contact probe fails to give an accurate portrayal of the actual generated waveform by the circuit since it only has a bandwidth of $1GHz$.

Because the sampling oscilloscope measurement was not performed concurrently with the EFS measurements, the near conformity between the pulses measured by EFS and the sampling oscilloscope validates the non-invasiveness of the EFS technique on this circuit as the cantilever did not introduce significant loading.

Chapter 7

Conclusions and Future Challenges

7.1 Conclusions

Electrostatic force sampling of digital waveforms using synchronous time domain gating was presented by implementing two modulation schemes to produce a suitable probing signal to sample high speed digital signals: amplitude and pulse width modulation. EFS using both modulation techniques have been characterized through theoretical predictions and various experiments. Internal measurements over transmission lines and two passivated circuits: a $0.5\mu m$ CMOS inverter chain and a NT25 pulse generator were performed to confirm the competence of the submitting EFS instrument.

The spatial resolution and capacitive loading of the EFS instrument was found to be about $1\mu m$ and $1fF$, respectively, through several references. One of the major factors that is needed to be considered for improving these criteria is the size and geometry of the cantilver.

The voltage sensitivity and SNR of the EFS instrument were theoretically derived and compared with the findings deduced from the measurements. The experimental RMS voltage resolution was $13mV$ on a ceramic transmission line for amplitude modulation while the corresponding theoretically approximated value was $18mV$. A poorer resolution was discovered when measuring the CMOS integrated circuit because of the decrease in the spatial derivative of the coupling capacitance and the increase in DC offset effects.

The bandwidths for both implementations of amplitude and pulse width modulation engineered in this work were defined and experimentally determined to be $3GHz$ and $4GHz$, respectively. Yet, it was concluded that both modulation schemes have equal bandwidth capability. The measured and the convolution counterpart must be carefully scaled when comparing with the actual signal under test to deduce the proper bandwidth. The bandwidth is also sensitive to temporal noise which is just another version of amplitude noise. The delay resolution is also dependent on this temporal noise as well as the jitter possessed by the electronics and generators employed.

7.2 Future Challenges

The bandwidth of the EFS instrument is mostly limited by the sharpness sampling pulse since the measured waveform is essentially a convolution between the sampling pulse and circuit signal. Few commercial impulse generators are adequate but they are often subjected to cost. Since bondwires reduces the bandwidth of signals, the concept of attaching a micromachined cantilever to the die of a pulse generator circuit is currently under development in the EFS laboratory at the University of Manitoba.

Most of the attention has been devoted to increasing the speed of the circuits in the microelectronics industry. Unfortunately, the bandwidth of the diagnostic instrument should ideally be better than that of the circuits under test. EFS generates impulses electrically, which also relies on state of the art circuitry. In the long run, 'a dog cannot catch its own tail', and optical pulses may have to be utilized eventually.

In fact, the overwhelmingly advancing industry has many tricks up its sleeves to better the performance of microelectronics. However, these innovations also puzzle and challenge diagnostic and failure analysis researchers. For instance, the number of levels of metal interconnect in microelectronic circuits are currently up to seven and is still increasing. Desired interconnects under test could be buried under $10\mu m$ of passivation. This working distance is too large for EFS to operate at.

Another invention in integrated circuit engineering that makes EFS impossible is the flip chip packaging technology. This packaging technique eliminates the need of bondwires for improving the bandwidth of integrated circuits. The top side of the circuit is placed upside down towards the routing board. Measurements must be performed from the backside of chip, and this abolishes the accessibility of EFS and many other existing diagnostic techniques. Possible future solutions for measuring these circuits may have to resort to optical means such as using infared beams.

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