Characterization of Electronically Active Defects in Hafnium Dioxide High-κ Gate Dielectrics

BY

DANIEL FELNHOFER

A Thesis submitted to
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Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Manitoba, Canada

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Abstract

The trapping behaviour of electronic defects in high-κ, HfO_2, metal-oxide-semiconductor (MOS) capacitors was investigated using capacitance-voltage and photocurrent-voltage (photo IV) measurements. The tested capacitors had a semi-transparent aluminum gate, HfO_2 deposited by metal-organic chemical vapour deposition, a SiO_x intermediate layer, and a lightly doped (1×10^{15} cm^{-3}) p-type silicon substrate. Internal photoemission was used to inject electrons from the gate and substrate electrodes for the charge injection study. The centroid of the oxide trapped charge was extracted from photo IV measurements, which confirmed that electrons are readily trapped by and detrapped from a large density of pre-existing defects (> 10^{12} cm^{-3}) in the bulk HfO_2 layer. The effective density of trapped charge was highly dependent on stress voltage and was modeled using first-order trapping kinetics with two defects having different capture cross-sections. The results from this work validate the use of the photo IV technique for high-κ MOS characterization.

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List of Nomenclature

α	extinction coefficient of thin film transmission probability (m^{-1})
ΔV	voltage shift in CV response due to oxide charge
ΔV_{FB}	flat-band voltage shift
ΔV_{g}	voltage shift in the photo IV response at negative biases, i.e., gate injection
ΔV_{mg}	mid-gap voltage shift
ΔV_{sub}	voltage shift in the photo IV response at positive biases, i.e., substrate injection
ε_{∞}	relative electronic permittivity
ε_{HfO2}	relative dielectric permittivity of hafnium dioxide
$\varepsilon_{high\text{-}\kappa}$	relative dielectric permittivity of high permittivity dielectric
ε_{i}	image force permittivity (F/m)
ε_{o}	permittivity of free space (8.854×10^{-12} F/m)
ε_{ox}	relative dielectric permittivity of silicon dioxide (3.9)
ε_{rel}	relative dielectric permittivity
ε_{si}	relative dielectric permittivity of silicon (11.7)
ϕ_{B}	bulk silicon potential (eV)
Φ_{ms}	metal-semiconductor workfunction difference (V)
ϕ_{ms}	metal-semiconductor workfunction difference (eV)
ϕ_{s}	silicon surface potential or amount of silicon band bending (eV)
κ	dielectric permittivity

λ	wavelength (m)
σ_c	capture cross-section for oxide defects (cm^2)
σ_p	photoionization cross-section for oxide defects (cm^2)
ν	optical frequency (Hz)
ψ_B	bulk silicon potential (V)
ψ_s	silicon surface potential or amount of silicon band bending (V)
A	area (m^2)
c	speed of light (2.998 m/s)
C	capacitance (F)
C_d	depletion capacitance due to majority carriers (F)
C_{HF}	high frequency capacitance (F)
$C_{HF,min}$	high frequency capacitance at its minimum value in strong inversion (F)
C_{it}	capacitance due to interface states (F)
C_{inv}	inversion capacitance due to minority carriers (F)
C_{LF}	low frequency capacitance (F)
C_{ox}	oxide capacitance (F)
C_p	capacitance using the parallel equivalent circuit model (F)
C_s	capacitance using the series equivalent circuit model (F)
D_{it}	interface state density ($cm^{-2}eV^{-1}$)
e-	electron (charge of -q)
E	energy (eV)
E_b	effective barrier height (eV)

E_{bo}	full barrier height from the Fermi level in the emitter to the conduction band of the injecting medium (eV)
E_c	conduction band edge (eV)
E_g	band-gap energy (eV)
E_{ph}	energy per single photon (J)
E_T	oxide trap depth (eV)
E_v	valance band edge (eV)
E_x	potential energy as a function of distance (eV)
f	frequency of the AC test signal for HFCV measurements (Hz)
F	electric field (V/m)
$F_{high-\kappa}$	electric field with the high-κ dielectric layer (V/m)
F_{ox}	electric field within the oxide (V/m)
F_p	localized photon flux
G	conductance (S)
h	Plank's constant (6.626×10^{-34} Js)
h+	hole (charge of +q)
I_{ph}	photocurrent (A)
k_B	Boltzman's constant (1.381×10^{-23} J/K)
n	volume density of oxide charge (cm^{-3})
N	total oxide trap density (cm^{-3})
N_a	acceptor dopant concentration per unit volume (cm^{-3})
n_c	conduction band electron density (cm^{-3})

N_c	density of states in the conduction band (cm^{-3})
N_e	hot electron distribution (electrons per absorbed photon per eV)
N_{eff}	effective density of oxide traps (cm^{-3})
n_i	intrinsic carrier density ($\sim 10^{10}$ cm^{-3} for silicon at room temperature)
n_t	volume density of filled oxide traps (cm^{-3})
N_T	total oxide trap density (cm^{-2})
P	probability of surmounting an energy barrier
P_T	transmission probability of photons for thin films
q	fundamental unit of charge (1.602×10^{-19} C)
Q	total oxide charge density at the centroid of charge (C/cm^2)
Q_{inj}	injected charge into oxide (C/cm^2)
Q_{ox}	equivalent oxide charge density at the oxide/substrate interface (C/cm^2)
R_p	resistance using the parallel equivalent circuit model (Ω)
R_s	resistance using the series equivalent circuit model (Ω)
T	temperature (K)
$t_{high-\kappa}$	dielectric thickness of a high permittivity dielectric (m)
t_{ox}	oxide thickness (m)
v_d	drift velocity of electrons in the conduction band (cm/s)
V_{FB}	flat-band voltage (V)
V_g	potential applied to the gate electrode (V)
V_{mg}	mid-gap voltage (V)
V_{ox}	electrostatic potential within the oxide (V)

V_{sub}	potential applied to the substrate (V)
v_{th}	thermal velocity of electrons in the conduction band (cm/s)
W_{max}	maximum depletion width of majority carriers (m)
$\bar{x}$	centroid of oxide charge distribution (m)
x_o	distance to the zero field point for IPE (m)
Y	quantum yield (over-barrier electrons per absorbed photon)

List of Abbreviations and Acronyms

AC	alternating current
CV	capacitance-voltage
DC	direct current
DI	de-ionized
DUT	device under test
FET	field-effect transistor
FWHM	full width at half of maximum
HFCV	high frequency capacitance-voltage
IPE	internal photoemission
ITRS	international technology roadmap for semiconductors
IV	current-voltage
GPIB	general purpose interface bus (the IEEE 488 standard)
LCC	leadless chip carrier
MOS	metal-oxide-semiconductor
Photo IV	photocurrent-voltage
QSCV	quasi-static capacitance-voltage
RPM	rotations per minute
UV	ultra-violet

Chapter 1 Introduction

In this chapter an introduction to this dissertation on the characterization of electronically active defects within hafnium dioxide high-κ gate dielectrics is presented. Firstly, the motivation for this research is presented. As part of the motivation, a discussion pertaining to the current state of MOS technology and device scaling is given. This discussion naturally progresses into an introduction of high-κ dielectrics and the justification for their use in MOS devices, which may in the future be a potential solution for limitations encountered from device scaling. The use of a hafnium dioxide gate dielectric, for future MOS devices, is mentioned in particular, as the analysis of oxide charge trapping in this dielectric is the main thesis of this research work. An outline of the goals of this work and the characterization techniques used to accomplish these goals is given in the problem description section of this chapter. An overview of this dissertation is then given at the end of this chapter.

1.1 Motivation

Moore's Law states that the density of devices of an integrated circuit doubles every two years [1]. This "law" has governed the semiconductor industry for the past 40 years. This scaling trend has driven the development of metal-oxide-semiconductor (MOS) based devices (i.e., metal-oxide-semiconductor field-effect transistors, MOSFETs) to continually decreasing physical dimensions as outlined by the International Technology Roadmap for Semiconductors (ITRS) which is published by the Semiconductor Industry Association.

Traditionally, MOS devices consisted of a highly-doped polycrystalline silicon as the metallic gate, silicon dioxide (or nitrided variations thereof [2, 3]) as the insulator, and silicon as the semiconductor. The scaling of these devices, in accordance with Moore's Law, was governed by a single scaling factor used to concurrently scale many physical dimensions and parameters. These parameters include the gate length, the oxide thickness, metallization wire thickness, bias voltage and substrate doping concentration [4]. As a result, each subsequent generation of technology has had substantial economic benefits (i.e., lower cost per device) as well as increased performance (higher speed per circuit) all without suffering from increased power dissipation [4]. However, traditional scaling theory eventually led to certain physical limitations, some of which were and are economic, (i.e., capital investment costs) while others are technological (finite physical dimension of the atomic scale).

One major feature of device scaling has been the thinning of the gate dielectric thickness where, in the most current technology, film thicknesses are only a few atomic layers. As such, current technology has reached the point where thinning of the oxide is causing three notable concerns: a) the leakage current through the oxide has dramatically increased due to increased direct tunneling current which is exponentially dependent on oxide thickness [5], b) coulombic scattering of inversion charge in the channel of a MOSFET due to charge within the gate which degrades carrier mobility and therefore performance [6], and c) ultrathin gate dielectric films suffer from reliability issues that include higher operating electric fields, larger leakage currents, and even the penetration of dopant atoms from the poly-silicon gate [2]. The large gate dielectric leakage current

is of particular concern for systems with low operating power (i.e., mobile and battery operated) devices in which high power dissipation is unacceptable.

One possible solution for combating oxide thinning due to scaling is to replace the traditional SiO_2 dielectric with a higher permittivity (high-κ) dielectric. The use of such a dielectric allows for traditional scaling to be used all the while reducing the gate leakage current. One metric used to compare high-κ devices to conventional SiO_2 devices is the equivalent oxide thickness, EOT, as given by

$$\mathrm{EOT} = \frac{\varepsilon_{ox}}{\varepsilon_{high-\kappa}} \cdot t_{high-\kappa} + t_{ox} \tag{1.1}$$

where ε_{ox} is the relative permittivity of silicon dioxide, $\varepsilon_{high\text{-}\kappa}$ is the relative permittivity of the high-κ dielectric, $t_{high\text{-}\kappa}$ is the thickness of the high-κ dielectric, and t_{ox} is the thickness of any intermediate oxide layer between the high-κ dielectric and silicon substrate. Therefore, the main benefit of using a high-κ dielectric is that, for given constant dielectric capacitance, a physically thicker dielectric can be used to achieve similar electrical characteristics as a thinner SiO_2 dielectric layer. A thicker dielectric film, at first glance should alleviate some of the previously mentioned concerns relating to leakage currents. The assumption made by this argument is that the replacement high-κ material has a similar band structure and therefore comparable insulating properties as SiO_2, which is generally not the case. Band-gap energy tends to decrease with increasing permittivity, and tunnelling current depends on material properties like band offsets and tunnelling effective masses [7]. These properties are of great importance since tunnelling currents are exponentially dependent upon thickness as well as the barrier height [5].

The last term in equation (1.1), the intermediate, underlying oxide thickness and its role on the EOT must be emphasized. The formation of an intermediate layer reduces the benefit of using a high-κ material, but in most cases, to some extent, it is desirable because the native oxide for silicon, SiO_2, results in a low defect density at the substrate interface [8], which is a necessity for reasonable MOSFET performance.

There are several candidates for replacing SiO_2 as the gate dielectric. These include hafnium dioxide, zirconium dioxide, the silicates/aluminates thereof, as well as some lanthanum and yttrium based oxides [9, 10]. According to the ITRS, it is expected that high-κ dielectrics will make their entry into the current technology roadmap for low operating power devices by 2006 and will feature a dielectric with a sub 15Å EOT [9]. However, before any material is chosen as the successor to SiO_2, a whole host of issues (material, electrical, or process related) must be addressed [10].

The high-κ dielectric investigated in this research work is hafnium dioxide. Hafnium dioxide has been found to be one of the more promising alternatives for SiO_2 because of properties such as, a) a high relative dielectric permittivity of ~20 [11], b) appropriate band structure and band offsets relative to silicon [12], and c) better thermal stability at rapid thermal annealing (RTA) temperatures of ~1000°C [10, 13]. Devices fabricated using HfO_2 as opposed to those with a conventional dielectric, have been found to have gate leakage current 3-5 decades of magnitude less than that found for SiO_2 films with a similar EOT [11, 14]. The silicates and aluminates of HfO_2 have been shown to have even better thermal stability [13, 15] than the pure oxide, but unfortunately also suffer from a reduced permittivity. Despite the previously mentioned advantages of

using HfO_2, there are still many unanswered questions regarding the integration of this dielectric into the MOS system.

One of the largest technological drawbacks to the incorporation of hafnium dioxide into today's technology is that the devices fabricated with this material are known to suffer from significant oxide charge trapping [11, 14, 16]. Large concentrations of charge trapped within the gate dielectric are significant as they cause degradation in device performance (i.e., threshold voltage shifts [16, 17], mobility degradation [11], etc.). Significant charge trapping is unacceptable for large integrated circuits where millions of devices are expected to operate for desired 10 year lifetimes. Therefore, it is necessary to ascertain knowledge of the oxide charge trapping mechanisms and properties of the defects (electron traps) within hafnium dioxide prior to their incorporation into future MOS technology. It is this desire to understand the trapping behaviour of HfO_2 defects that is the motivation and main focus of this work.

1.2 Problem Description

The motivation for this work is to obtain an understanding of the charge trapping nature of defects within hafnium dioxide dielectrics. This is done by investigating the trapping of electrons at defects in high-κ HfO_2 MOS capacitors. There are several measurement techniques that are sensitive to oxide charge trapping; the ones specifically used for this work were the high-frequency capacitance-voltage (HFCV) and photocurrent-voltage (photo IV) techniques. As will be discussed in the course of this dissertation, both techniques are responsive to trapped oxide charge within an MOS

capacitor. It was the goal of this work to demonstrate that the photo IV technique can be used for high-κ MOS characterization, specifically to obtain knowledge of the spatial location of these defects and the quantity of these defects within the dielectric stack.

1.3 Overview

This dissertation is divided into several chapters beginning with the current chapter, which is an introduction into the motivation for this research work. The background theory of MOS device physics is presented in chapter 2. The experimental apparatus and measurement techniques used for MOS device characterization is discussed in chapter 3. In chapter 4, a detailed description of the fabrication steps used to create the HfO_2 MOS capacitors is given. The chapters 5 to 8 are dedicated to experimental results and their discussion. The deposition and optical transmission of thin film aluminum is presented in chapter 5, while barrier height measurements for both gate and substrate electron injection are presented in chapter 6. In chapter 7, the characterization of the high-κ capacitors is discussed in terms of results from current-voltage, and high- and low-frequency capacitance-voltage measurements. The main results of this research with respect to the injection of charge into the MOS capacitors are given in Chapter 8. The final chapter is devoted to the conclusions of this work.

Chapter 2 Theory

The device physics for MOS capacitors is well understood and has been published in numerous papers and books, such as those written by Nicollian and Brews [18], Sze [19], Taur and Ning [20], and Wolf [21] to name a few. The role of this chapter is to introduce and review the physics underlying the characterization of the high-κ capacitors within this research work. This chapter begins with a brief review of MOS capacitors, their regimes of operation, and the determination of key characterization parameters for traditional and high-κ devices. Internal photoemission theory is then presented, and its use for barrier height determination. This is followed by a discussion about various techniques for stressing MOS devices and defects within the MOS system, such as a) interface trap defects and the use of the combined high-low capacitance method for their measurement, and b) oxide defect types and the measurement of oxide charge via capacitance-voltage (CV) shift and photocurrent-voltage (photo IV) shift methods.

2.1 The MOS Capacitor

The MOS configuration used by the semiconductor industry for the past few decades has been the metal (poly-Si), SiO_2, silicon system as shown in Figure 2.1. This technology is well understood and the basic operating regimes of a simple capacitor structure and equivalent circuit models are shown in Figure 2.2 for the p-type silicon substrate capacitor in Figure 2.1.

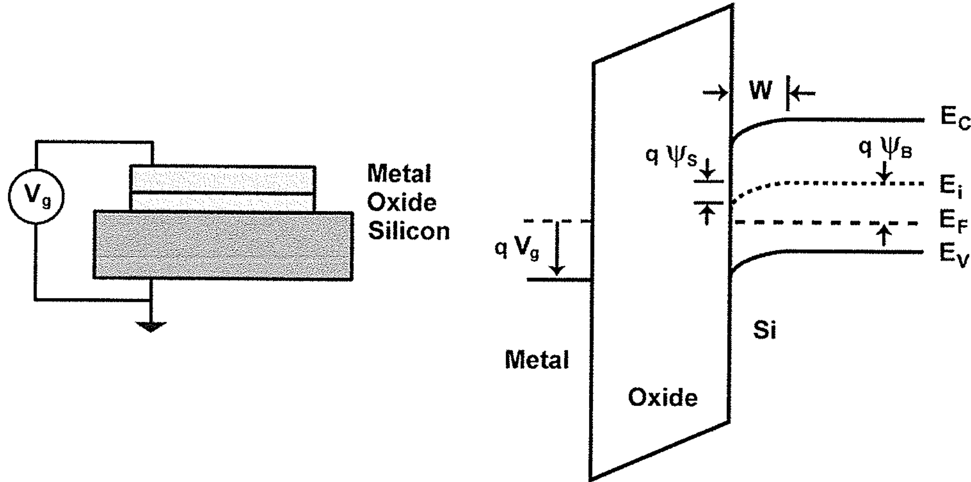


Figure 2.1: The MOS capacitor and energy band diagram. The silicon is p-type (after [20]).

The regime on the left side of Figure 2.2 is called accumulation because the gate bias (negative) is such that majority carriers (holes in this case) "accumulate" at the surface to form a sheet charge at the interface. Therefore, the corresponding capacitance within the silicon, C_{si}, is very large as illustrated by the equivalent circuit model. Thus, the measurement of capacitance in accumulation is in fact a measurement of the oxide capacitance, C_{ox} and can be related to capacitor area, A, dielectric thickness, t_{ox}, and relative permittivity, ε_r, by

$$C_{ox} = \frac{\varepsilon_r \cdot \varepsilon_o \cdot A}{t_{ox}} \tag{2.1}$$

where ε_o is the free space permittivity, and $\varepsilon_r = \varepsilon_{ox} = 3.9$ for silicon dioxide as the dielectric. As mentioned in the introduction of this dissertation and in (1.1), the use of a high-κ dielectric allows for smaller EOTs while using physically thicker films. However, this additional dielectric layer also complicates the extraction of parameters like the dielectric permittivity for each of the films.

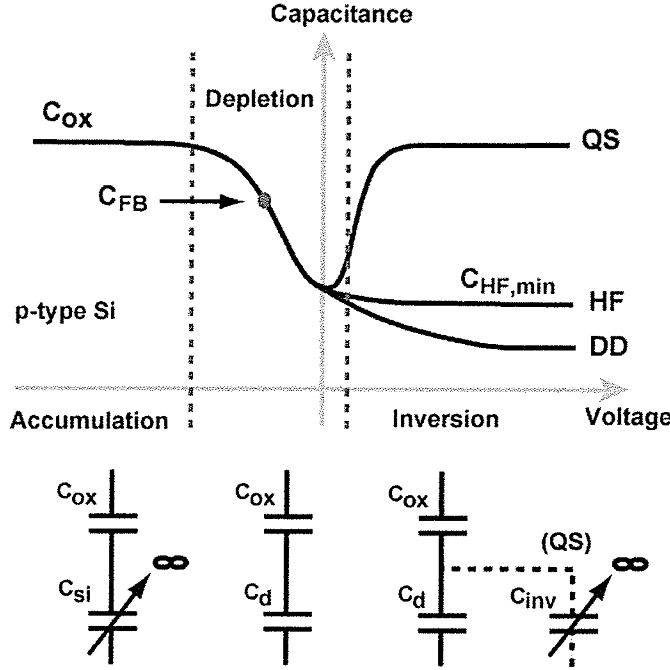


Figure 2.2: The CV response of a p-type silicon MOS capacitor and equivalent circuit models for three regimes of operation: accumulation, depletion and inversion (after [18]).

The central regime in Figure 2.2 is depletion, appropriately named for the depletion of majority carriers from the silicon surface due to band bending caused by the gate potential. The point labelled as the flat-band capacitance (C_{FB}) is the point where the gate potential balances out any metal-semiconductor workfunction difference, Φ_{ms}, and charge within the oxide. The applied bias required for the flat-band condition is given by,

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} = \Phi_m - \Phi_s - \frac{Q_{ox}}{C_{ox}} \tag{2.2}$$

where Q_{ox} is the equivalent oxide charge density located at the oxide/substrate interface, Φ_m is the workfunction of the metal gate, and Φ_s is the workfunction of the silicon (as determined from the Fermi energy, E_F, within the bulk silicon) [20].

The third regime illustrated in Figure 2.2 is inversion. In this regime, the increasing gate potential (positively increasing in the case for p-type silicon) causes minority carriers (electrons) to collect at the silicon surface. The three separate curves shown in Figure 2.2 in this regime are a direct result of the testing method used. If testing at low frequencies, the uppermost quasi-static, QS, curve results because the slower responding minority carriers are able to respond to the test signal (usually a slowly varying voltage ramp) and thereby the inversion charge is measured. Thus, the equivalent circuit model can be approximated to the C_{ox} because the inversion capacitance, C_{inv}, becomes very large due to the density of minority carriers located at the silicon surface. If the capacitor is tested at higher frequencies (usually by a small AC signal superimposed on a DC signal) then the inversion charge is no longer measured (assuming an external source does not provide a minority carrier reservoir, e.g., the source and drain contacts of a transistor, or decrease minority carrier generation time, e.g., with the use of illumination) and only the depleted majority carriers in the silicon are able to respond, thus the measured capacitance is a function of C_{ox} in series with depletion capacitance, C_d, as shown by the equivalent circuit model in Figure 2.2. Also, deep depletion, DD, can result when majority carriers are not able to respond to a very fast bias change (such as a voltage step measurement) as seen by the lower curve in Figure 2.2.

High frequency capacitance-voltage (HFCV) measurement in the inversion regime is a measure of depletion capacitance and oxide capacitance by the relationship given by [22]

$$C_{HF,min} = \frac{C_{ox} \cdot C_d}{C_{ox} + C_d}. \qquad (2.3)$$

Also, since the capacitor is in strong inversion, C_d is minimized and can be related to maximum depletion width of majority carriers in the silicon, W_{max}, by

$$C_d = \frac{\varepsilon_o \cdot \varepsilon_{si} \cdot A}{W_{max}} \tag{2.4}$$

where

$$W_{max} = \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_{si} \cdot \psi_s}{q \cdot N_a}}, \tag{2.5}$$

ε_o is the free space permittivity constant, ε_{si} is the relative permittivity of the silicon, ψ_s is the silicon surface potential, q is the elementary charge constant, and N_a is the uniform acceptor concentration within the depletion region [22]. The band bending approximation given by

$$\psi_s \cong 2 \cdot \psi_B + \left(\frac{k_B \cdot T}{q}\right) \cdot \ln\left(\frac{2 \cdot q \cdot \psi_B}{k_B \cdot T} - 1\right) \tag{2.6}$$

where the bulk silicon potential, ψ_B, can be determined from the relationship,

$$\psi_B = \left(\frac{k_B \cdot T}{q}\right) \cdot \ln\left(\frac{N_a}{n_i}\right) \tag{2.7}$$

where n_i is the intrinsic carrier density ($\sim 1 \times 10^{10}$ for silicon at room temperature), k_B is Boltzmann's constant, and T is temperature can be used [18]. The band bending approximation in (2.6) is suitable for the strong inversion regime where band bending can be approximated as constant. Therefore, using equations (2.3) through (2.7), N_a can be related to the measured C_{ox} and $C_{HF,min}$ values by the expression [18]

$$\frac{N_a}{\ln(N_a / n_i) + 0.5 \cdot \ln[2 \cdot \ln(N_a / n_i) - 1]} = \frac{4 \cdot k_B \cdot T \cdot C_{ox}^2}{q^2 \cdot \varepsilon_o \cdot \varepsilon_{si} \cdot A^2} \cdot \left(\frac{C_{ox}}{C_{HF,min}} - 1\right)^{-2} \tag{2.8}$$

or by use of the empirical relation for silicon at room temperature given by [22]

$$\log(Na) = 30.38759 + 1.68278 \cdot \log(C) - 0.03177 \cdot [\log(C)]^2 \quad (2.9)$$

where

$$C = \frac{C_{HF,min}}{A \cdot \left(1 - C_{HF,min} / C_{ox}\right)} \quad (2.10)$$

Therefore, the HFCV measurement is an effective measurement for obtaining the uniform doping concentration within the silicon, or the average doping concentration over the entire depletion width if the actual doping profile is depth dependent.

2.2 Internal Photoemission

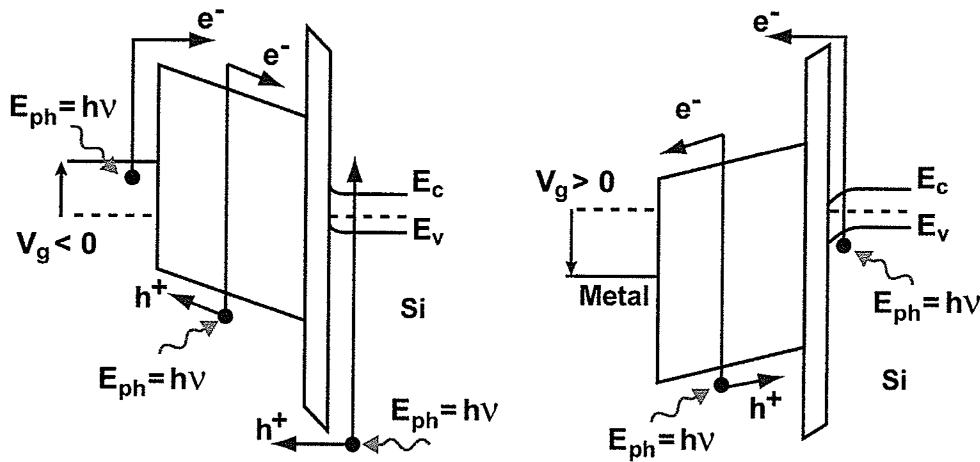


Figure 2.3: Optical excitation of carriers occurring in a high-κ MOS capacitor under negative and positive gate biases and illumination.

The use of internal photoemission (IPE) in a MOS device is a valuable technique for exciting carriers in the gate or substrate with enough energy to inject them into the oxide conduction or valance band without the use of large electric fields. The various optical excitations of carriers are shown within Figure 2.3 for both gate electron injection (negative gate bias) and substrate electron injection (positive gate bias). Electron-hole

pair (EHP) creation results in either a) an over-barrier current due to injected electrons or holes from the gate or substrate, or b) photoconductivity if the photon energy, E_{ph}, exceeds the band-gap energy, E_g, of the oxide. Therefore, both E_{ph} and material properties are important in interpreting IPE measurements and the source of injected current. In this chapter and throughout this research work it is assumed that electrons, not holes, are being injected into the oxide at the photon energies being used. This point is discussed in more detail within Section 4.1.

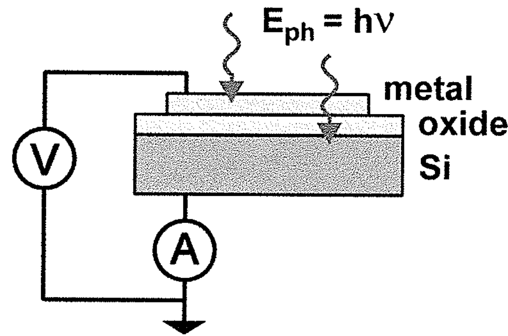


Figure 2.4: The basic schematic of using a MOS capacitor for IPE measurements. A semi-transparent metal gate is required since illumination can only be directed from above.

One requirement for the use of IPE for MOS measurement purposes is that both the substrate and gate must be illuminated as shown in Figure 2.4. This is accomplished by using a semi-transparent metal gate [18, 23]. The transmission of light through thin metallic films is given by [24]

$$P_T = e^{-\alpha \cdot z} = e^{-\frac{4 \cdot \pi \cdot k}{\lambda} \cdot z} \tag{2.11}$$

where P_T is the transmission probability, α is the extinction coefficient, z is the thickness of the film, λ is the photon wavelength, and k is the absorption coefficient (the imaginary

part of the complex refractive index). Typically aluminum or gold films on the order of 100-150Å are used [23, 25]. Absorption of light is not a concern within the dielectric because of the large band-gap energy, but interference effects could affect the measurement when dielectric thickness is on the same order as photon wavelength [18, 23, 26]. However, current technology uses thin dielectric films that are significantly less than 100 nm, thereby dismissing interference effects as a concern [26].

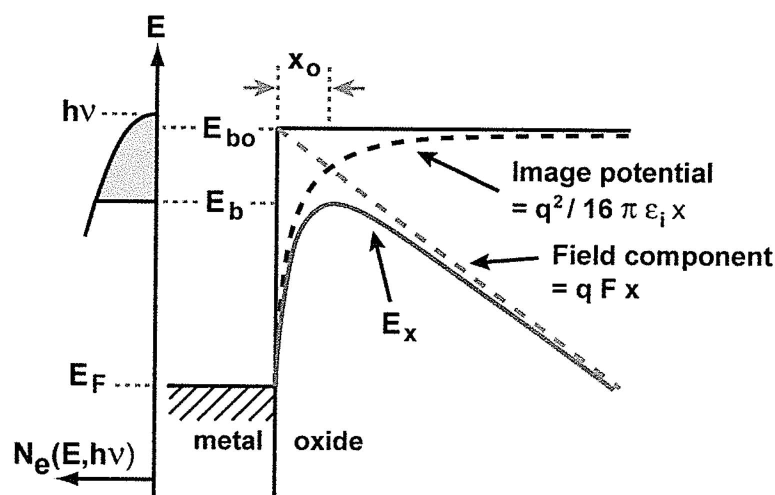


Figure 2.5: The energy band diagram of a metal emitter and oxide conduction band indicating the role of the image force potential and external applied field on determining the effective barrier height. Also shown is the hot electron distribution within the emitter as a function of energy and illumination energy. After [19] and [27].

The primary applications for IPE in MOS characterization are for barrier height determination (as discussed in the following section), injecting hot (energetic) electrons (as discussed in Section 2.3), and oxide charge studies (as discussed in Section 2.5.2). Before discussing these applications, it is important to gain a theoretical understanding of the photoinjection of electrons into an oxide, especially the role of the effective barrier height. As shown in Figure 2.5, the effective barrier height for a hot electron is governed

by the Schottky effect that consists of an image force term and the applied field across the oxide [19]. The image force is the electrostatic force resulting from the induced positive charge in the emitter (metal) as an electron is moved a distance, x, from the metal/oxide interface [19]. This theory results in a potential energy barrier, E_x, for electrons to overcome in order to be considered as current. Therefore,

$$E_x = \frac{q^2}{16 \cdot \pi \cdot \varepsilon_i \cdot x} + q \cdot F \cdot x \tag{2.12}$$

where F is the external electric field applied and ε_i is the permittivity of the insulator [19]. The permittivity used for image force contributions is lower than the static permittivity value because the oxide cannot fully screen the image force interaction by the time the electron is injected [18]. For SiO_2, it has been shown to correspond to the dynamic value of $2.2\varepsilon_o$ [18]. From (2.12), the distance within the oxide from the emitter that corresponds to an effective electric field of zero for an injected carrier, known as the zero field point distance, x_o, is given by

$$x_o = \left(\frac{q}{16 \cdot \pi \cdot \varepsilon_i \cdot F} \right)^{1/2} \tag{2.13}$$

and the effective barrier height for photoinjection, E_b, is

$$E_b = E_{bo} - 2 \cdot F \cdot x_o = E_{bo} - K \cdot F^{1/2} \tag{2.14}$$

where E_{bo} is the full barrier height as shown in Figure 2.5, and the constant K corresponds to

$$K = \left(\frac{q}{4 \cdot \pi \cdot \varepsilon_i \cdot x_o} \right)^{1/2} . \tag{2.15}$$

From (2.13), it is important to note that as the electric field is increased, the zero field point gets closer to the injecting surface (e.g., $x_o \sim 9$Å when a 2 MV/cm electric field is applied). This makes IPE a viable technique for characterizing even the very thinnest of films.

Another aspect of this theory to consider is that it assumes that the zero field point is a function of the uniform external field applied to the oxide and the image force contribution. However, the presence of oxide charge will also affect the field locally within the oxide and thus affect the effective barrier for photoinjection. The effect of oxide charge is discussed within the photo IV shift measurements section of this chapter (Section 2.5.2) and it is assumed that no oxide charging occurs when determining barrier height.

2.2.1 Barrier Height Determination

The measurement of barrier height via IPE requires a model to account for the current as a function of electric field (according to the Schottky effect theory described above) and illumination energy. In order to accomplish this, consider the measurable quantity called quantum yield, Y. Quantum yield is defined as the ratio of the number of electrons surmounting the energy barrier to the number of absorbed photons in the emitter. Therefore, this quantity effectively incorporates all the processes involved in IPE, such as the photoexcitation of electrons, the transport of hot electrons to the emitter surface, and the escape of electrons over the energy barrier [18]. The quantum yield can be expressed as

$$Y(h\nu, E_b) = \int_{E_b}^{h\nu} N_e(E, h\nu) \cdot P(E) \cdot dE \qquad (2.16)$$

where N_e is the hot (energetic) electron distribution at the interface in units of electrons per absorbed photon per eV as shown in Figure 2.5, and P(E) is the surface transmission probability of a hot electron surmounting the barrier [28]. The hot electron distribution in the emitter is determined by a) the density of initial occupied states, b) the density of unoccupied states, c) the optical transition probabilities, and d) electron scattering effects [28]. Despite these complications, Powell has shown that (2.16) can be modelled as

$$Y \propto (h \cdot \nu - E_b)^p \qquad (2.17)$$

where p is the power term of the model that is dependent on emitter type as shown in Table 2.1. A more detailed table incorporating optical transitions and scattering processes is shown in [29]. As shown in Table 2.1, photoemission from a metal emitter; an emitter that has a step distribution of hot electrons determined by the Fermi level, E_F (at 0K), is best modelled by p = 2. For silicon, where the distribution of hot electrons is best modelled by a ramp distribution, p = 3. Therefore, the model in (2.17) directly relates photon energy, and barrier height to quantum yield.

Table 2.1: Correlation between the IPE yield model parameter, p, and the emitter hot electron distribution. After [28].

p	Hot Electon Distribution, N_e	Emitter Example
1	Impulse, δ(E)	Narrow filled band
2	Step, u(E)	Metals
3	Ramp, E	silicon

The quantum yield can be experimentally measured using the relation [26],

$$Y = \frac{I_m \cdot h \cdot \nu}{P_a \cdot q} \tag{2.18}$$

where I_m is the measured photocurrent of the MOS capacitor and P_a is the absorbed power of photons in the emitter. Thus, (2.17) and (2.18) can be combined to obtain

$$\left(\frac{I_m \cdot h\nu}{P_a \cdot q}\right)^{1/p} \propto h\nu - E_b \propto h\nu - \left(E_{bo} - K \cdot F^{1/2}\right) \tag{2.19}$$

Therefore, the effective barrier height, E_b, can be measured at varying electric fields by plotting $Y^{1/p}$ versus photon energy and determining the $Y = 0$ intercept. These values can in turn be plotted as a Schottky plot (E_b versus $F^{1/2}$) and the $F = 0$ intercept can be extrapolated to obtain the band offset, E_{bo}.

One assumption underlying this theory that has not been discussed in detail is the role of the dielectric. When injecting into an oxide one must consider that not all carriers with sufficient energy ($E > E_b$) will reach and surmount the barrier within the oxide [18]. There is a probability that some hot electrons will scatter back to the emitter. It has been shown that this change in current can be taken into account with an exponential term dependent on scattering length, s_L, and the zero field point since it is theorized that elastic scattering is occurring in the region $x < x_o$ and the probability of scattering backwards from beyond this region is small [30]. Therefore, (2.17) becomes [18],

$$Y \propto (h \cdot \nu - E_b)^p \cdot \exp(-x_o / s_L) \tag{2.20}$$

This additional field dependent term will have a greater influence on yield at lower fields where x_o is larger (often referred to as barrier position mode) than at higher fields where Schottky barrier lowering tends to dominate (barrier height mode) [26].

The latter "barrier height mode" measuring technique is the one most commonly used in practice today [12, 31, 32]. An alternative IPE technique based on the same theory measures current as a function of applied field at several illumination energies [28]. However, this technique is impractical for low leakage current devices because IV sweep measurements must be taken, i.e., measurement time would be too long since displacement current is much larger than particle currents. In general, IPE barrier height measurements are very accurate and preferable to other methods such as CV and IV [22].

2.3 Stressing Devices

In order to investigate oxide charging within a MOS capacitor structure, one must stress devices by injecting either electrons into the conduction band or holes into the valence band. Several stressing techniques can be used, such as avalanche injection, photoinjection, Fowler-Nordheim tunnelling, and direct tunnelling [18]. These techniques are shown in Figure 2.6

In this research work, photoinjection is used because it has several advantages over other techniques. Firstly, photoinjection uses photons to excite electrons within the gate or substrate over the energy barrier between the corresponding electrode and dielectric. This is in contrast to avalanche injection, a method that can only inject carriers from the silicon substrate, albeit at higher densities but only for a limited applied field

range [18]. Secondly, the use of photoinjection also has the added benefit of requiring much smaller electric fields, since the electric field only needs to collect photo-excited carriers. A much larger electric field is needed to accelerate carriers for avalanche injection, and to achieve Fowler-Nordheim tunnelling. The smaller electric field is beneficial in minimizing perturbation of charge within the oxide due to field assisted detrapping mechanisms [25], which is important when characterizing oxide charge. A disadvantage of photoinjection is that one must also consider the photoionization of existing oxide charge while stressing devices [25].

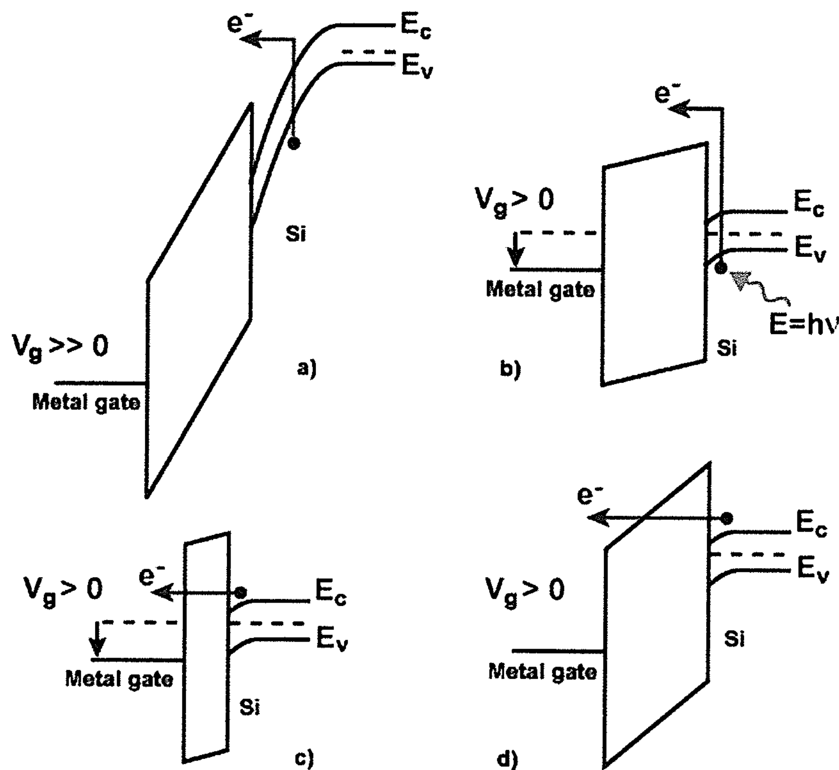


Figure 2.6: Stressing techniques for MOS capacitors, including a) avalanche injection, b) photoinjection, c) direct tunnelling, and d) Fowler-Nordheim tunnelling.

2.4 Interface State Defects and Measurement

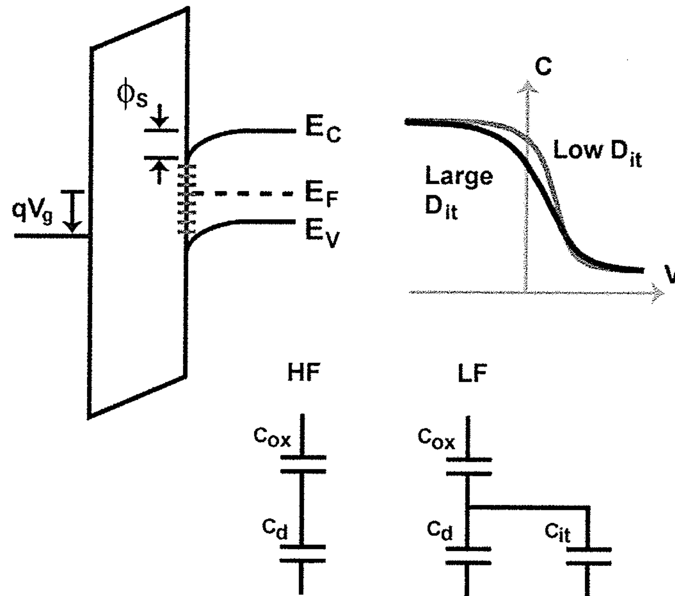
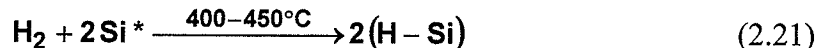


Figure 2.7: The location of interface states within an energy band diagram and corresponding CV stretchout as a result of high interface state density. Also shown is the equivalent circuit model of HF and LF CV measurements.

One type of electrically active defect in MOS devices is the interface state. These acceptor (accepts an electron) and donor (donates an electron) states are situated at the oxide/silicon interface at energies within the band-gap of silicon as shown in Figure 2.7 [19]. These states are the result of dangling bonds (unfulfilled silicon bonds) at the silicon interface due to the change in material and structure from a silicon crystal lattice to an amorphous oxide. These defects are also known as P_b centers because the unpaired electron is highly localized on the p-character orbital of the silicon atom [8]. The type of P_b center has also been shown to depend on the crystal orientation of silicon [8]. It is well published in the literature that the passivation of these bonds by a hydrogen atom occurs according to the reaction [33],



$$H_2 + 2\,Si^* \xrightarrow{400-450^\circ C} 2(H - Si) \quad (2.21)$$

where Si* refers to the dangling bond. The temperature dependence is of importance because this reaction is also known to reverse at temperatures lower than 400°C [33]. For this reason, a forming gas anneal (FGA), a mixture of hydrogen and nitrogen, is often required to reduce interface state density, D_{it}. Several groups have also shown that similar dangling bond defects (P_b-like centers) occur for other high-κ/silicon interfaces as well [8, 34, 35] and that a FGA still results in the desired reduction in D_{it} [36]. However, this is less of a concern for a capacitor with a relatively thick intermediate SiO_x layer where the interface appears more SiO_2-like in character [34].

The effect of interface states on MOS device operation is significant because they are situated within the band-gap of silicon. Therefore, these states fill or empty (i.e., trap or de-trap electrons) depending on the occupancy and location of the interface state with respect to the Fermi level at the silicon surface, which is a function of applied bias. It is often assumed for high frequency capacitance measurements that interface states fail to respond to the high frequency due to their long response time. However, they will respond to the slower varying DC bias of the HFCV measurement by affecting the amount of silicon band bending. This results in the stretch-out of the CV curve as shown in Figure 2.7. Therefore, a primary indicator for high interface state density is a reduced slope of the HFCV measurement as the capacitor is swept from accumulation to inversion or vice versa, corresponding to the Fermi level at the interface moving through the band-gap.

2.4.1 D_{it} Calculation by using the High-Low Capacitance Method

The calculation of interface state density can be made using a high frequency measurement (Terman method), a low frequency measurement, or a combination of both [18]. The equivalent circuit of a HF and LF measurement is shown in Figure 2.7. The HF case consists of the depletion capacitance in series with the oxide capacitance since the interface states do not respond to the high frequency AC signal. Therefore,

$$C_{HF} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}. \tag{2.22}$$

However, the equivalent circuit model for a low frequency measurement requires an additional interface state capacitance in parallel with the depletion capacitance, resulting in the relation,

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_d + C_{it}}. \tag{2.23}$$

The difficulty with the Terman method and low frequency measurement is that no direct calculation of C_{it} can be made from the measurements. In the Terman method, the C_{HF} measurement is compared to a theoretical calculation of C_{HF} curve, thereby, determining the D_{it} from the stretchout of the CV response [18]. The LF measurement on the other hand requires the theoretical calculation of C_d in order to calculate C_{it}. A better approach that removes errors associated with theoretical calculations is to solve (2.22) and (2.23) for C_{it} to obtain the expression [18],

$$C_{it}(V_g) = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}. \tag{2.24}$$

The benefit of this expression is clearly evident since C_{it} is directly obtained from the low and high frequency measurements. However, D_{it} is expressed in terms of silicon band banding, so an expression relating band bending within the silicon, ψ_s, in terms of applied voltage, V_g is required. To obtain an expression, consider Gauss's law for charge equality within an MOS capacitor [18]

$$C_{ox} \cdot (V_g - \psi_s) = -(Q_{it}(\psi_s) + Q_d(\psi_s)) \tag{2.25}$$

where Q_{it} is the charge associated with interface states, and Q_d is the depletion charge within the silicon. Rearranging (2.25) and assuming a very slow applied voltage change; an infinitesimal change in gate voltage, dV_g, results in a change in band bending, $d\psi_s$, given by [18]

$$C_{ox} \cdot dV_g = [C_{ox} + C_{it}(\psi_s) + C_d(\psi_s)] \cdot d\psi_s . \tag{2.26}$$

Integrating (2.26) results in the expression,

$$\psi_s = \psi_{so} + \int_{V_{go}}^{V_g} \frac{C_{ox}}{C_{ox} + C_{it} + C_d} dV_g \tag{2.27}$$

where ψ_{so} is the band bending corresponding to the applied voltage V_{go}. Therefore, rearranging this equation and using (2.23) results in the expression

$$\psi_s = \psi_{so} + \int_{V_{go}}^{V_g} 1 - \frac{C_{LF}}{C_{ox}} dV_g . \tag{2.28}$$

Thus, using the low frequency measurement and a value for ψ_{so} at a V_{go} value within accumulation can determine the band bending within the silicon as a function of applied voltage. A voltage in accumulation is used to minimize error associated with using a ψ_{so}

value because within this regime ψ_s is a weak function of V_g and the Fermi level is close to a known position, either the conduction (n-type silicon) or valence band edge (p-type silicon).

To determine the interface state density, (2.24) and (2.28) are used with the relation,

$$D_{it}(q \cdot \psi_s) = \frac{C_{it}}{q \cdot A}. \tag{2.29}$$

The advantages of using the combined high-low capacitance method is that C_d is measured so theoretical calculations are not required and errors associated with the calculation of capacitances and band bending discrepancies between calculated and measured capacitances are avoided. However, there still are several other sources of error that account for the typically "U" shape of a D_{it} measurement [37]. One source of error is the difficulty in obtaining a real HF measurement without any interface state response. Even at a high frequency of 1 MHz, some interface state response may occur, especially those closer to the band edges, and will limit how close to the band edges that they can be probed [22]. Also, since inversion charge is not accounted for in the HF measurement, probing near the onset of inversion is limited and can be erroneous. The error is larger for lower substrate doping concentrations because this results in lower depletion capacitance, thus, the inversion capacitance will have a larger overall effect [18]. Overall, the combined high-low capacitance measurement is known to have a lower limit of $\sim 10^{10}$ $cm^{-2}eV^{-1}$.

2.5 Oxide Charge and Measurement

Generally, oxide charge is divided up into three basic types of charge: fixed, mobile, and oxide trapped charge. Fixed charge, as the name implies, is immobile and does not change in quantity as a result of normal device operation, i.e., changes in applied bias. This charge is generally modelled as being located near the silicon/oxide interface for the SiO_2/Si system [20]. Mobile charge, alkali metal ions, is oxide charge that is able to respond to changes in applied electric field by drifting across the oxide. The amount of drift is a function of temperature, applied voltage, and time. Generally, these charges are a result of device contamination. The third type of oxide charge and the type of charge relevant to this work is oxide trapped charge. As a device is stressed, electrons (holes) are trapped and de-trapped at defects located within the oxide [19].

The characterization of oxide charge is important because any oxide charge detrimentally affects the operation of MOS devices by influencing the CV response and by acting as a charge scattering center [20]. In the following two sections, oxide charge characterization by CV and photo IV measurements is discussed.

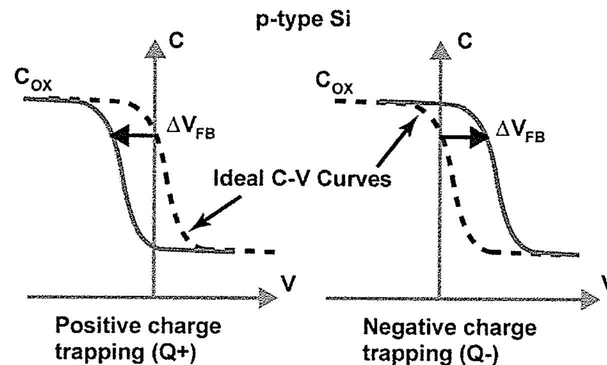


Figure 2.8: The shift in CV response due to oxide charge within a p-type silicon MOS capacitor.

2.5.1 The CV Measurement

The CV response of a MOS capacitor is dependent on the band bending within the silicon substrate. Any presence of oxide charge will affect the electric field within the oxide, thereby altering the silicon band bending and CV response. In Figure 2.8 it is shown that the presence of oxide charge shifts the CV response of a p-type silicon MOS capacitor by a voltage determined by

$$\Delta V = -\frac{Q_{ox}}{C_{ox}} = -\frac{q}{\varepsilon_{ox} \cdot \varepsilon_o} \int_0^{t_{ox}} x \cdot n(x) \cdot dx \tag{2.30}$$

where Q_{ox} is the total oxide charge density located at the silicon/oxide interface, and n(x) is the volume density of oxide charge within the oxide, and x is the distance measured from the metal/oxide interface [19]. The previous equation is a direct result of integrating Poisson's equation within the oxide

$$\frac{d^2 V_{ox}}{dx^2} = -\frac{q \cdot n(x)}{\varepsilon_{ox} \varepsilon_o} \tag{2.31}$$

where V_{ox} is the electrostatic potential within the oxide [18]. Equation (2.30) can be rewritten in terms of the centroid of oxide trapped charge, $\bar{x}$, given by

$$\bar{x} = \frac{\int_0^{t_{ox}} x \cdot n(x) \cdot dx}{\int_0^{t_{ox}} n(x) \cdot dx} \tag{2.32}$$

where the total oxide charge density at the centroid of charge, Q, is given by

$$Q = \int_0^{t_{ox}} n(x) \cdot dx \tag{2.33}$$

Therefore,

$$\Delta V = -\frac{q \cdot \bar{x} \cdot Q}{\varepsilon_{ox} \cdot \varepsilon_o}. \tag{2.34}$$

The important result of (2.34) is that the shifts seen in Figure 2.8 can be directly related to a change in oxide charge. If negative oxide charge is trapped, a positive shift in CV response occurs, and vice versa.

The use of a CV measurement and (2.34) is the most commonly used method in determining the charge density within dielectrics because of its simplicity [18]. However, a key assumption made in its use is that the centroid of charge density is known independently. This assumption must be made because the CV measurement will only determine the first moment of the charge distribution, $\bar{x}Q$. Most often it is assumed that the oxide charge is located at the oxide/silicon interface, $\bar{x} = t_{ox}$, or evenly distributed in the oxide, $\bar{x} = t_{ox}/2$. Modelling the oxide charge as a fixed charge sheet at the interface has been shown to be suitable for thermally grown oxides, but remains open to discussion for newer dielectrics and gate stacks, like high-κ dielectrics.

Most often in oxide charge trapping/de-trapping studies, the flatband voltage shifts, ΔV_{FB}, of a device are measured as a function of injected charge, Q_{inj}, which is defined as

$$Q_{inj} = q \cdot \frac{\text{total stress current}}{\text{total time}} \tag{2.35}$$

An alternative approach is to relate the flatband voltage shifts to the effective density of oxide traps at the silicon/oxide interface, N_{eff},

$$N_{eff} = -\frac{\Delta V_{FB} \cdot \varepsilon_{ox} \cdot \varepsilon_o \cdot A}{q^2} \tag{2.36}$$

where A is the area of the capacitor. These parameters are vital in determining the nature of the oxide traps and modelling their behaviour as seen in past trapping studies, such as [33, 38].

2.5.2 Photo IV Measurement

Another method to characterize oxide charge is photo IV measurements. The basic principle underlying the photo IV technique is IPE, which has been discussed in Section 2.2. Charge within a dielectric layer of a MOS device will alter the internal electric field and therefore change the effective barrier height and the injected current. As a result, the photocurrent is a direct indicator of the presence of oxide charge. To prove this argument, Poisson's equation within the oxide, (2.31), must be solved according to the boundary conditions

$$V_{ox}(0) = 0, \quad \text{and} \quad V_{ox}(t_{ox}) = V_g - \Phi_{ms} - \psi_s \tag{2.37}$$

where V_{ox} is the potential within the oxide, V_g is the applied voltage, Φ_{ms} is the metal-semiconductor workfunction difference, and ψ_s is the silicon band bending potential [39]. This solution is differentiated and solved for the electric field at the zero field point, x_o, as shown in Figure 2.5, to yield,

$$F_{ox}(x_o) = \frac{(V_g - \Phi_{ms} - \psi_s)}{t_{ox}} + \frac{q}{\varepsilon_o \cdot \varepsilon_{ox}}\left[\int_{x_o}^{t_{ox}} n(x') \cdot dx' - \int_0^{t_{ox}} \frac{x'}{t_{ox}} \cdot n(x') \cdot dx'\right] \tag{2.38}$$

where F_{ox} is the electric field within the oxide at x_o, x is the distance from the injecting surface, and n(x) is the volume density of oxide charge [18]. It should be noted that equation (2.38) is a generic solution for the electric field within the oxide due to an

applied field and oxide charge. Therefore, this field is not equal to zero at the zero field point because no consideration of the image force potential, as described in Section 2.2, is given. For MOS devices, photoinjection can occur from both the metal ($x = 0$) and substrate ($x = t_{ox}$) electrodes. Therefore, equation (2.38) can be rewritten using the centroid of oxide charge, $\bar{x}$, given in (2.32) and the total oxide charge density, Q, given in (2.33) to obtain

$$F_{ox}\left(x_o^-\right) = \frac{\left(V_g^- - \Phi_{ms} - \psi_s^-\right)}{t_{ox}} - \frac{1}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot \left(1 - \frac{\bar{x}}{t_{ox}}\right) \cdot Q + \frac{q}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot \int_0^{x_o^-} n(x) \cdot dx \tag{2.39}$$

where the superscript "-" denotes gate injection (negative biases) and

$$F_{ox}\left(x_o^+\right) = \frac{\left(V_g^+ - \Phi_{ms} - \psi_s^+\right)}{t_{ox}} + \frac{1}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot \frac{\bar{x}}{t_{ox}} \cdot Q - \frac{q}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot \int_{x_o^+}^{t_{ox}} n(x) \cdot dx \tag{2.40}$$

where the superscript "+" denotes substrate injection (positive biases). In order to derive equations (2.39) and (2.40), it is assumed that negative charge (electron) injection results in negatively trapped oxide charge (i.e., n(x) is the magnitude of trapped negative charge).

The third terms in equations (2.39) and (2.40) are insignificant if the zero field point is close to the injecting surfaces and most of the charge is located away from the interface, thus limiting the effect of the oxide charge close to the interface. Therefore, the applied electric field should be relatively high (>1MV/cm) according to (2.13) so that the measurement is in the barrier height mode, where scattering within the oxide is not a concern.

Now consider the photocurrent as a function of electric field prior to, and after, oxide charge is trapped. If the photocurrent before, $I_{ph,b}$, equals the photocurrent after, $I_{ph,a}$, then it stands to reason that the effective barrier is the same for both currents. Therefore, the electric fields within the oxide at the zero field points (the point determining the effective barrier) should be equal, $F_{ox,b}(x_o) = F_{ox,a}(x_o)$. In this case, (2.39) can be written into the form

$$\left(V_{\bar{g},b} - \Phi_{ms} - \psi_{\bar{s},b}\right) - \frac{t_{ox} - \bar{x}_b}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot Q_b = \left(V_{\bar{g},a} - \Phi_{ms} - \psi_{\bar{s},a}\right) - \frac{t_{ox} - \bar{x}_a}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot Q_a \tag{2.41}$$

where the subscripts "b" and "a" denote before and after values. If one assumes that the oxide is initially free of charge, then

$$\Delta V_g = V_{\bar{g},b} - V_{\bar{g},a} = \psi_{\bar{s},b} - \psi_{\bar{s},a} - \frac{t_{ox} - \bar{x}_a}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot Q_a \approx -\frac{t_{ox} - \bar{x}}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot Q \tag{2.42}$$

where ΔV_g is the shift in photo IV response due to gate injection. The assumption made in (2.42) is that the change in silicon band bending is negligible for degenerate silicon substrates or changes little due to oxide charge for non-degenerate silicon [25]. The expression on the far right side of (2.42) can also represent a change in oxide charge density, ΔQ, as long as it is assumed that the distribution of charge as given by the centroid, $\bar{x}$, has not changed. If the above arguments are made for substrate injection, the expression

$$\Delta V_{sub} = -\frac{\bar{x}}{\varepsilon_o \cdot \varepsilon_{ox}} \cdot Q \tag{2.43}$$

can be derived, where ΔV_{sub} is the shift in photo IV response due to substrate injection. The implication of the above theory is that the expected photo IV response due to trapped oxide charge is a parallel voltage shift. A deviation from a parallel shift could indicate the significant presence of interfacial charge, charge that was assumed negligible in the previous arguments. An oxide charge profiling technique based on non-uniform charge distributions close to the interface is not discussed in this dissertation, but can be found in [18]. Solving (2.42) and (2.43) for the oxide charge density and centroid results in the expressions

$$Q = -\frac{\varepsilon_o \cdot \varepsilon_{ox}}{t_{ox}} \cdot \left(\Delta V_g - \Delta V_{sub}\right) \tag{2.44}$$

and

$$\frac{\bar{x}}{t_{ox}} = \left[1 - \frac{\Delta V_g}{\Delta V_{sub}}\right]^{-1} . \tag{2.45}$$

Therefore, measuring photo IV shifts and using equation (2.44) and (2.45) results in the independent determination of both the effective oxide charge density and the centroid of its distribution. Both parameters are significant in characterizing oxide charge within MOS devices. One other word of caution with this measurement technique is that photocurrents typically have electron fluences orders of magnitude larger than dark currents and these measurements are taken at significant fields (~ 1 MV/cm), a combination which may perturb oxide charge and must be considered [25].

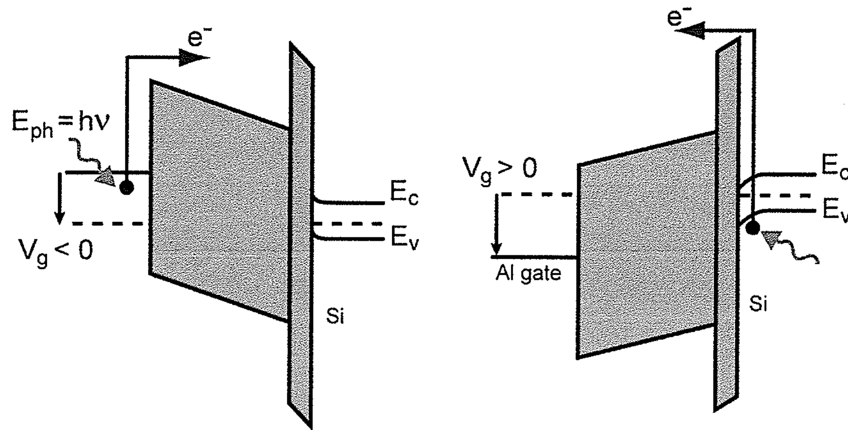


Figure 2.9: Schematics of electron injection from the gate and substrate electrodes by IPE.

The previously discussed theory has been formulated for traditional MOS devices with one dielectric layer. The use of photo IV measurements for high-κ dielectrics results in additional complications. Typically, an intermediate SiO_x layer is used as shown in Figure 2.9. In this case, the role of the interfacial oxide on photocurrent for both substrate and gate injection must considered. Fortunately, intermediate oxide layers tend to be as thin as possible (< 8Å) due to the EOT requirements of state of art technology, as defined in (1.1) [9]. As a result, the intermediate layer is typically only a fraction of the gate stack thickness. The asymmetry in the gate stack and its role on photoinjection is discussed below.

Before discussing photoinjection, it is prudent to perform a simple calculation of the electric fields and potential voltage drops for the two dielectric structures used in this research. Firstly, the electric field across the intermediate layer is larger than the field across the high-κ dielectric because they scale with relative permittivity as defined by Gauss' law

$$F_{ox} = F_{high-k} \cdot \frac{\varepsilon_{high-k}}{\varepsilon_{ox}} \tag{2.46}$$

where F_{ox} is the electric field across the oxide, $F_{high\text{-}\kappa}$ is the field across the high-κ dielectric, $\varepsilon_{high\text{-}\kappa}$ is the permittivity of the high-κ dielectric, and ε_{ox} is the permittivity of the intermediate layer. This equation assumes a uniform field throughout the oxide (i.e., no oxide charge). Also, the applied voltage, V_g, can be related to the voltage drop across the high-κ dielectric layer, $V_{high\text{-}\kappa}$, and the intermediate layer, V_{ox}, by the relation

$$V_g - W_{ms} - \psi_s = V_{high-k} + V_{ox} \tag{2.47}$$

where W_{ms} is the metal-semiconductor workfunction difference, and ψ_s is the amount of silicon band bending. Solving equations (2.46) and (2.47) with the use of equation (1.1) results in the expressions

$$V_{ox} = \frac{t_{ox}}{EOT} \cdot \left(V_g - W_{ms} - \psi_s\right) \tag{2.48}$$

and

$$V_{high-\kappa} = \left(1 - \frac{t_{ox}}{EOT}\right)\left(V_g - W_{ms} - \psi_s\right) \tag{2.49}$$

An outcome of equations (2.48) and (2.49) is that the electric field across the intermediate layer is substantially larger than the field across the thicker high-κ dielectric layer. These equations were used, along with equations (2.13) and (2.14) to determine the photoinjection barriers shown in Figure 2.10 and 2.11. The band structure in these two figures was calculated based on a 15Å thick SiO_2 layer, a 90Å thick HfO_2 layer, a 3.1 eV barrier height for the SiO_2 layer [20], a 2 eV barrier height for the HfO_2 layer [12], a

1.2 eV offset between dielectric conduction bands [12], a ratio of dielectric permittivity between HfO_2 and SiO_2 of 4:1, and a relative dynamic permittivity of 2.2 for SiO_2 [18] and 5.4 for HfO_2 [37].

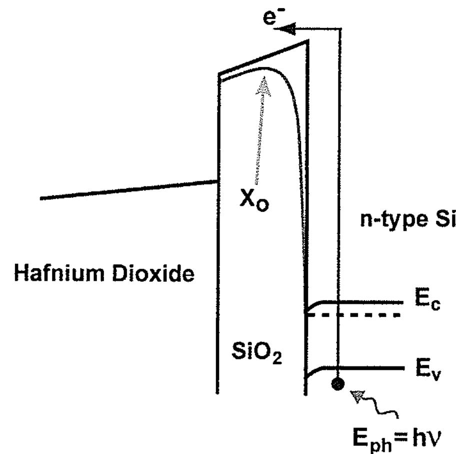


Figure 2.10: The photoinjection barrier for substrate injection. The band structure was calculated based on a 1V potential drop across the oxide layers, 15Å SiO_2 layer, 90Å HfO_2 layer, 3.1 eV barrier height for the SiO_2 layer, a 1.2 eV offset between dielectric conduction bands [12], a ratio of dielectric permittivity of 4:1, and a relative dynamic permittivity of 5.4 [37]. This results in a zero field distance of 7.8Å and effective barrier height of 2.7 eV.

The substrate injection of electrons is shown in Figure 2.10, assuming a 1V potential drop across the dielectric layers. Therefore, the zero field distance is calculated to be 7.8Å, and the effective barrier height is 2.7 eV. The implication on substrate photoinjection for this research work is that the intermediate layer is thicker than the zero point field distance for the applied voltages used. Therefore, oxide charge within the intermediate layer and interfacial charge between the high-κ and intermediate layer will be probed by substrate injection. In any case, substrate photoinjection will continue to be dependent on oxide charge because trapped charge within either dielectric will alter the electric field within the intermediate layer and therefore the effective barrier height. It is

also important to note that tunnelling into the high-κ dielectric conduction band does occur at higher applied biases.

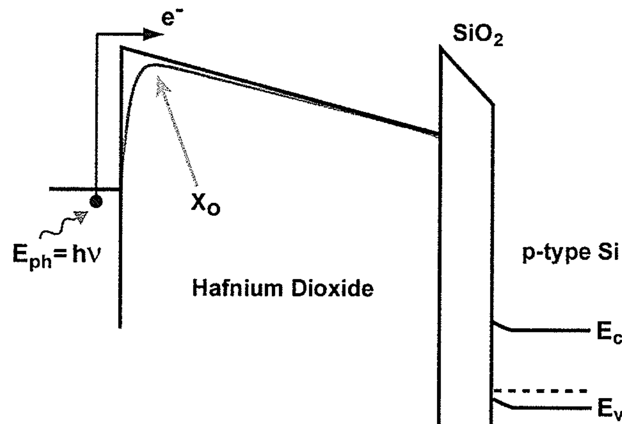


Figure 2.11: The photoinjection barrier for gate injection. The band structure was calculated based on a 2V potential drop across the oxide layers, 15Å SiO_2 layer, 90Å HfO_2 layer, 2 eV barrier height for the HfO_2 layer, a 1.2 eV offset between dielectric conduction bands [12], a ratio of dielectric permittivity of 4:1, and a relative dynamic permittivity of 5.4 [37]. This results in a zero field distance of 7Å and effective barrier height of 1.8 eV.

The calculated band structure for gate electron injection with a 2V potential drop across the dielectric layers is shown in Figure 2.11. In this case, a zero field distance of 7Å and effective barrier height of 1.8 eV were calculated. At the applied biases and dielectric thicknesses used in this research, tunnelling currents are not appreciable. Also shown in Figure 2.11, is the thin intermediate layer that is potential barrier for gate electron injection. Electrons injected into the HfO_2 could potentially scatter and lose energy enough to not overcome the potential barrier at the intermediate oxide layer. However, the tunnelling probability is large for electrons in the high-κ dielectric conduction band to tunnel through the thin (15Å) intermediate layer [5]. Therefore, it is unlikely that intermediate layer acts as a barrier for photoinjected electrons. Also, it is

unlikely that the intermediate layer consists purely of SiO_2, so a reduced barrier height is also plausible.

An additional point to note is that the zero point fields are closer to the injecting surface for high-κ capacitors than traditional SiO_2 MOS capacitors because a) the higher electric fields within the thin intermediate layer for substrate injection, and b) the higher dynamic permittivity of high-κ dielectrics ($\varepsilon_\infty = 5.37\varepsilon_o$ for cubic HfO_2 and $\varepsilon_\infty = 5.74\varepsilon_o$ for ZrO_2 as calculated by [37] versus $\varepsilon_\infty = 2.2\varepsilon_o$ for SiO_2) for gate injection.

All of the above arguments would lend credence to the use of photo IV measurements for high-κ oxide charge characterization. Of course, a correction to the relative dielectric permittivity in the above equations would have to be made. One important aspect of these photo IV shift measurements to note is that they only provide an effective oxide charge density and centroid value, and provide no detailed profile information. However, they do help discriminate whether a significant number of bulk oxide charges are located within the dielectric in question, or whether they are primarily at the interface.

As mentioned before, the advantage of using a photo IV shift measurement in characterizing oxide charge is that the charge density and charge centroid can be determined independently, which is not possible for CV measurements. However, the CV measurement is most often utilized because of a) its simplicity, since special test structures, like a transparent gate, are not needed, and b) the charge distribution of oxide charge in traditional SiO_2 devices was well approximated as a charge sheet located near the silicon/oxide interface ($\bar{\mathbf{x}} = t_{ox}$) [38 , 40].

Chapter 3 Experimental Set-up and Techniques

In this chapter a discussion on the various apparatus used for experimental measurements is described. The connectivity of devices under test (DUTs), the test equipment and the interfacing of test equipment to a computer are discussed. The measurement techniques for characterizing high-κ dielectrics, including interfacial barrier height measurements, current- and capacitance-voltage techniques, and stress measurements, are also discussed in terms of voltage sweep and stress parameters.

3.1 Measurement Set-up

Several different measurement set-ups were used, including: a) photo-detector measurements for obtaining the optical spectra of the light source and for measuring the optical transparency of thin metallic films, b) electrical probe station measurements for metal-oxide-semiconductor (MOS) capacitor characterization under dark conditions, and c) photoinjection measurement techniques for MOS capacitor characterization under illumination. For all tests, the equipment was connected to the device under test (DUT) or routed through a switch matrix (Keithley 7001), which was used to control which measurement equipment was to be used during any given experiment. The switch matrix was used to switch between the different test equipment used for the automated testing of the capacitors. All test equipment was interfaced to a personal computer using either (or both) the GPIB (IEEE 488) and/or RS232 bus systems.

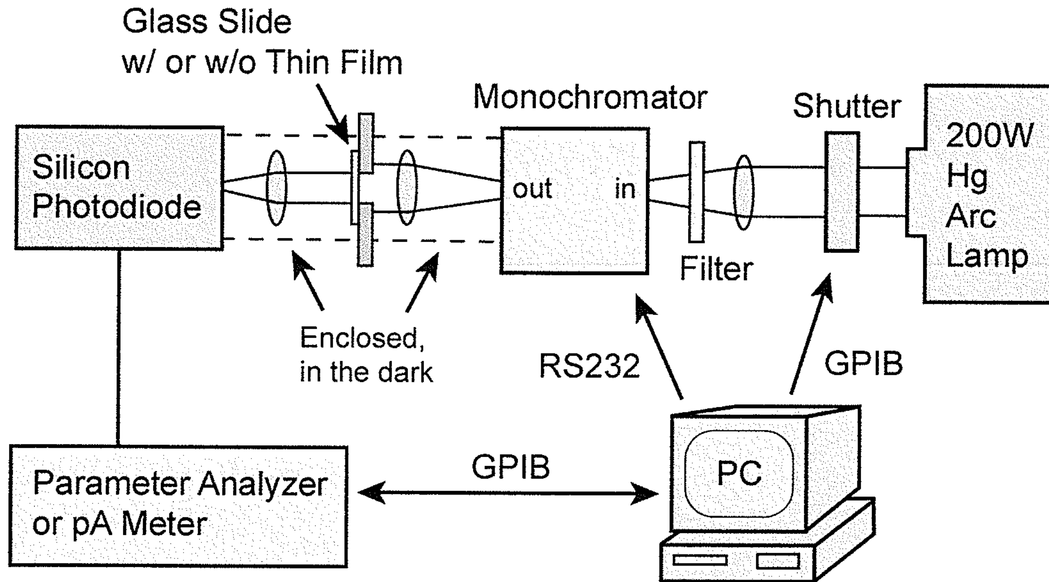


Figure 3.1: The apparatus for photodetector based measurements such as the thin metal films optical transparency tests. The optical spectra of the light source was obtained when the glass slide was omitted.

3.1.1 Photo-detector Measurements

The apparatus used for photo-detector measurements is shown in Figure 3.1. This system consists of a 200W Hg arc lamp (Oriel 6823) as the UV light source, a computer controlled shutter, a monochromator, optical filters and lenses, a photodiode, and a current measuring unit (either a HP 4140B pico-ammeter (pA) or an Agilent 4156C semiconductor parameter analyzer). The use of a calibrated silicon photodiode (Newport 818-UV) was used to measure the optical spectra (the intensity of the light source as a function of wavelength, which is described in Section 6.1). Optical transparency measurements were performed to assess the thickness of the thin metal gates used. A glass slide with and without the thin aluminum film was placed between the monochromator and photodiode and the optical transmission as a function of wavelength

was obtained by comparing measured photocurrents between the two regions of the slide; i.e., with and without the thin metal film. All photodetector measurements were shielded from ambient illumination to reduce errors associated with undesirable signals.

3.1.2 Probe Station Measurements

The use of a probe station for MOS characterization facilitated the ease in which test structures are probed and aided in the reduction of electrical and optical noise. For this research, the probe station was used for both CV and IV tests performed in the dark. The measurement set-up for these tests is shown in Figure 3.2. The probe station used was an Alessi REL 6100 from Cascade Microtech.

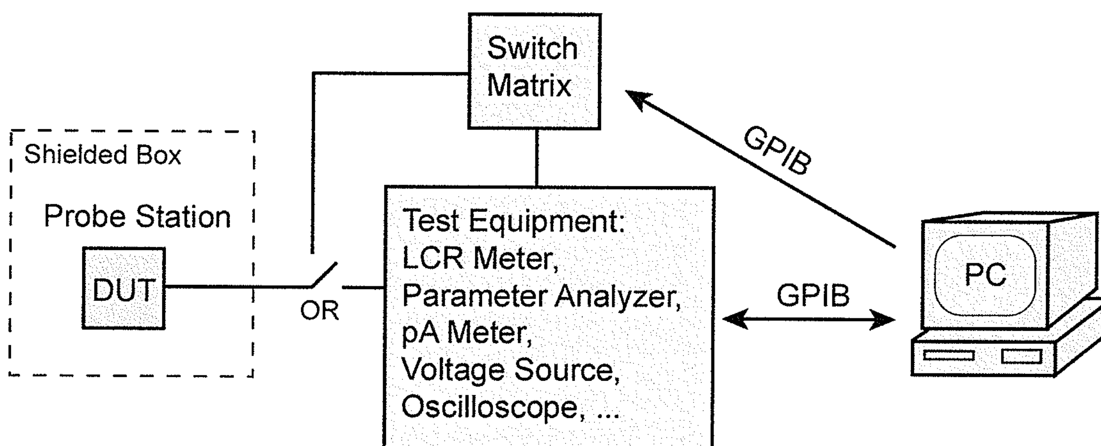


Figure 3.2: The apparatus used for probe station measurements. The DUT was connected to the test equipment or routed through a switch matrix to allow for the different types of measurements.

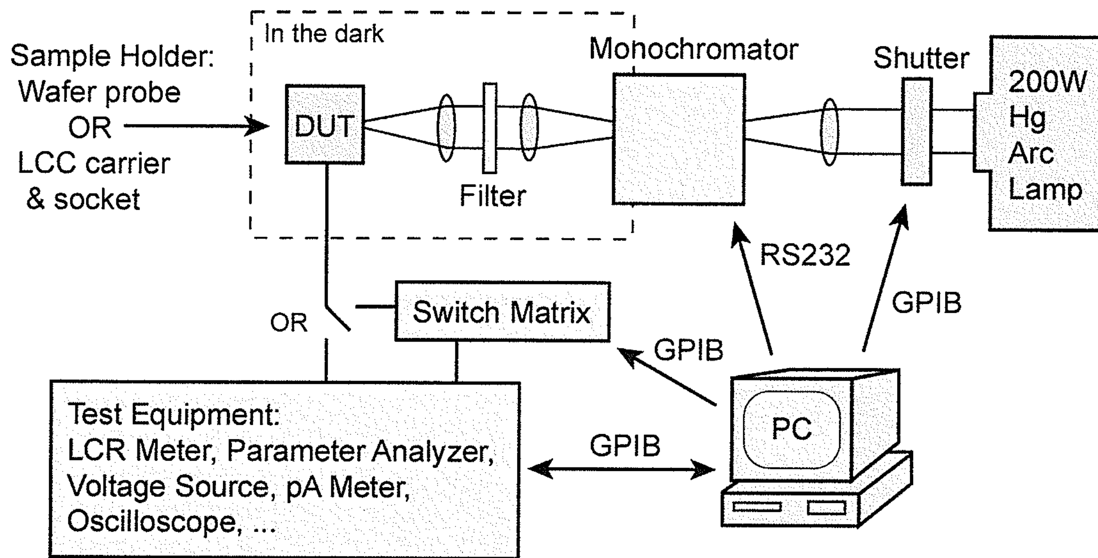


Figure 3.3: The apparatus used for photoinjection measurements.

3.1.3 Photoinjection Measurements

Photoinjection techniques were used primarily for the characterization of the high-κ gate dielectrics. For such photoinjection measurements an external light source was used, requiring the use of the experimental apparatus shown in Figure 3.3. These measurements consisted of the previously mentioned arc lamp, monochromator, shutter, filters and lenses, as well as a sample holder for electrically contacting the DUT. Two separate types of sample holders were used in this research. The first consisted of a leadless chip carrier (LCC) socket and carrier as shown in Figure 3.4a. The capacitor under test was mounted to the chip carrier and then placed into the socket for testing. The second holder consisted of a constructed test fixture that used an aluminum vacuum chuck and copper plate to make contact to the substrate and a probe with a tungsten needle to contact the gate (see Figure 3.4b). The use of the tungsten probe facilitated the

measurement of devices with much smaller contact areas allowing smaller area capacitors to be tested. In Section 4.6, a complete discussion of the details of the techniques used for electrically contacting the DUT is included. Both experimental set-ups used electrical shielding to reduce noise and the DUT was kept in the dark to minimize exposure to background illumination.

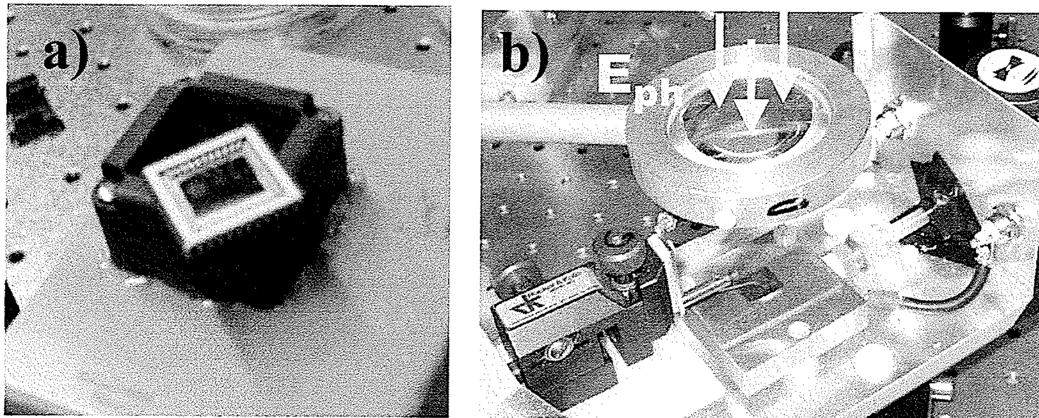


Figure 3.4: The two sample holders used for photoinjection tests, a) a capacitor bonded to a leadless chip carrier and the matching socket, and b) the constructed test fixture for probing capacitors.

3.2 Testing Procedure

The measurement techniques used in this research work were controlled via a number of computer programs that ran the automated tests, which include photocurrent measurements as a function of photon energy, current-voltage (IV), and quasi-static (QS) and high frequency (HF) capacitance-voltage (CV), as well as charge injection studies.

3.2.1 Photocurrent Versus Wavelength Measurements

In order to obtain the barrier height between a dielectric and a metallic contact or silicon substrate using internal photoemission (IPE), a measurement of the photocurrent as function of photon energy must be obtained and analyzed using equation (2.19). Similar measurements are also necessary to calibrate the light source where a calibrated photodetector is used. The measurement procedure for such tests is shown schematically in Figure 3.5 where a sweep in either the photon energy, E_{ph}, or wavelength, λ, steps is required. At every photon energy step, multiple measurements and subsequent averaging can be performed if necessary to increase the signal to noise ratio.

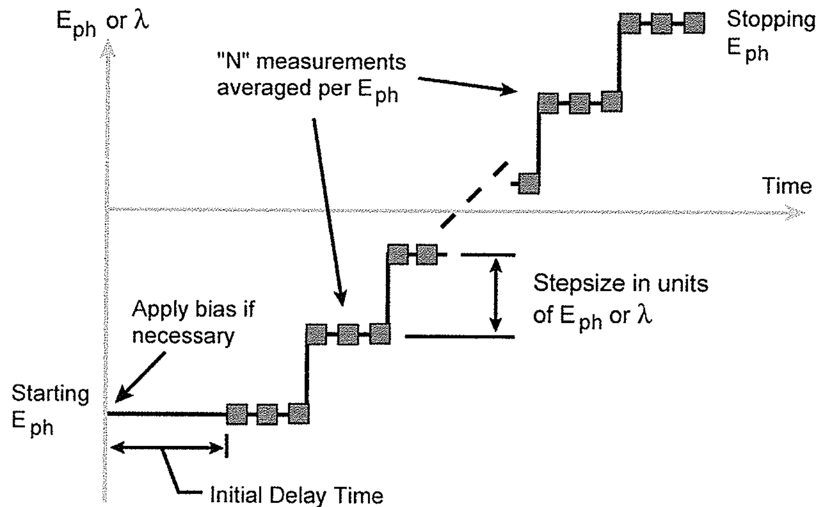


Figure 3.5: The measurement procedure for obtaining the photocurrent as a function of photon energy.

For measuring energy barriers, a constant bias was applied to an MOS capacitor for the duration of the measurement in order to measure the particle current and avoid measuring displacement current. A thorough discussion of particle and displacement

currents is given in Section 7.3. An initial delay time is used prior to the measurement sweep to allow the photocurrent to settle to a steady state value. The sweeps were run from a low to high photon energy, E_{ph}. During this photocurrent measurement, the HFCV response is monitored for any indication of oxide charging.

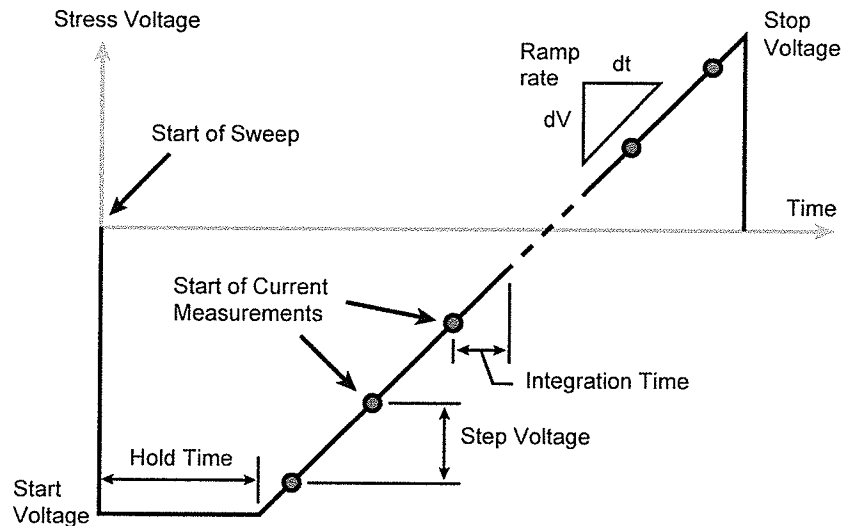


Figure 3.6: The measurement procedure for IV sweeps using a ramped voltage.

3.2.2 Current-Voltage Measurements (IV)

The use of current-voltage sweeps for characterizing MOS capacitors is very important because they are very sensitive to the quality of dielectric and as such to electronically active defects that could lead to current leakage paths. Typical IV measurements require a ramped voltage sweep (provided by the HP 4140B pA) where the leakage current is measured in real time. Such a measurement is shown schematically in Figure 3.6. When measuring leakage currents, typically two voltage sweeps (one for

negative biases and one for positive biases) are required where each sweep starts at zero voltage and is ramped to the desired bias.

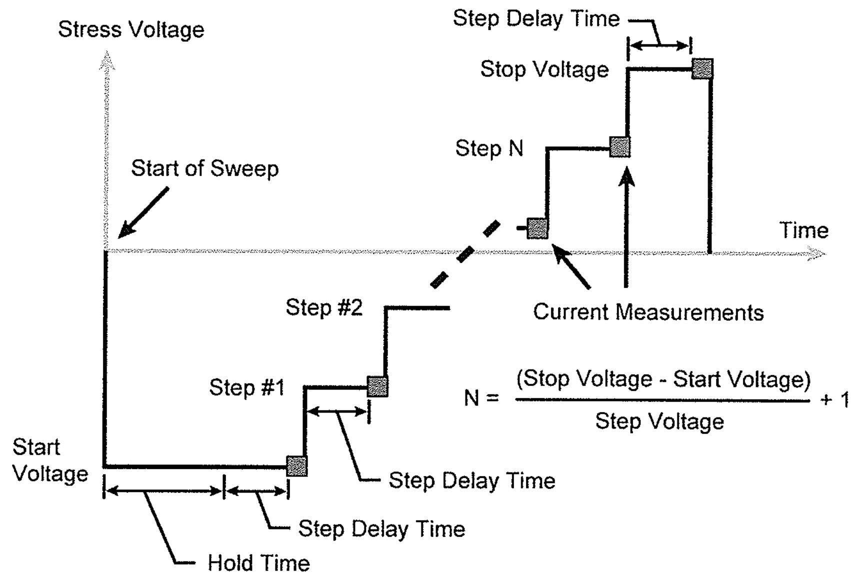


Figure 3.7: The measurement procedure for IV sweeps using voltage steps.

An additional procedure for measuring IVs is the use of a stepped voltage sweep, as opposed to a ramp. The procedure for these measurements is shown in Figure 3.7. These measurements were performed with an Agilent 4156C semiconductor parameter analyzer. In MOS capacitor IV measurements, with small leakage currents, it is vital that the ramp rates or step delay times are chosen effectively to minimize any displacement current as opposed to the actual particle (electron) current from gate to substrate or vice versa, depending upon the bias polarity. Issues surrounding the measurement of displacement current are discussed in the following section. It should also be noted that the photocurrent-voltage measurements described in this dissertation were IV measurements using voltage steps with an external illumination.

3.2.3 Quasi-Static Capacitance-Voltage (QSCV)

The measurement of the low frequency or quasi-static CV response is identical to the ramped IV measurement shown in Figure 3.6. When a displacement current is measured, the QSCV response can be determined from measured current, I_m, and the voltage ramp rate, dV/dt and is given by the expression

$$C = \frac{dQ}{dV} = \frac{I_m}{dV/dt} \tag{3.1}$$

The difference between the QSCV measurement and a typical IV measurement is that QSCV measurements are taken by sweeping the voltage from the inversion to the accumulation regime. Since these sweeps start at a bias in the inversion regime, illumination is generally required during the initial hold time (the time prior to the sweep after which when a bias is applied) to generate the necessary minority carriers. This is necessary because the purpose of the QSCV measurement is to measure the response of both majority and minority carriers (Section 2.1), as well as any interface states (see Section 2.4). Once a sufficient density of minority carriers is generated, the voltage sweep is done in the dark. Since the measurement of quasi-static capacitance is a result of a displacement current, other contributions to the current can lead to erroneous results. Therefore if the capacitors under test are "leaky", i.e., have a particle current leaking from gate to substrate through the gate dielectrics, a correction to the capacitance is required. This is discussed in more detail in Section 7.2.

3.2.4 High-frequency Capacitance-Voltage (HFCV)

The procedure for measuring the HFCV response of a capacitor is shown schematically in Figure 3.9. For this measurement, the Agilent 4284A LCR meter was used and a small AC signal (typically 30 mV) was applied with a DC bias and the impedance of the DUT was measured. The capacitor is typically modeled using either a parallel or series combination of a capacitor and resistor as discussed in Section 7.1. In this case, voltage sweeps are generally taken from the inversion regime into the accumulation regime and then back into inversion if desired. Typically, there is a hold time between inversion-to-accumulation and accumulation-to-inversion sweeps to test for any hysteresis of a HFCV response.

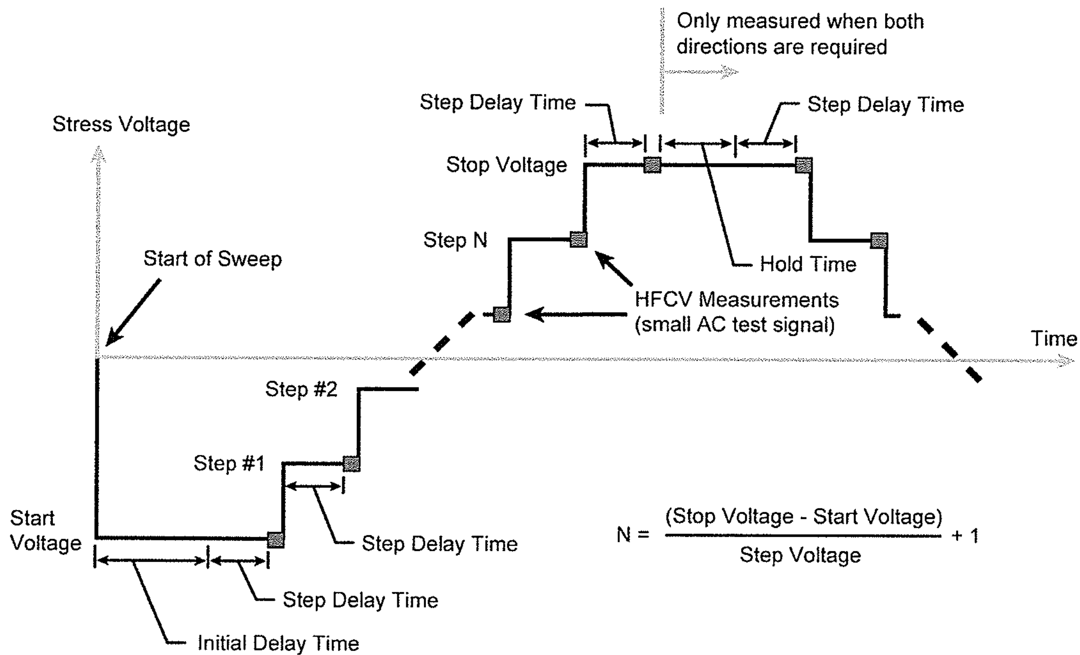


Figure 3.8: The measurement procedure for HFCV sweeps.

3.2.5 Charge Injection Tests

Charge injection is required in order to perturb the state of oxide charge within MOS capacitors to characterize the density and location of the electronically active defects. Other defect and trapping parameters such as capture cross-section and emission and/or captures rates may also be determined. The basic stressing procedure used in this research was the constant voltage stressing (CVS) technique shown in Figure 3.9. During the constant stress voltage pulses, the duration of which increased exponentially with time, illumination is applied to the DUT to assist in the injection of charge (electrons, for this work) into the oxide via photoinjection. The leakage current within the device is measured during the stress pulses and summed over stress time to obtain the total injected charge (i.e., the total over barrier charge minus trapped charge), Q_{inj}. In between the applied voltage pulses, HFCV, QSCV, or IV measurements were taken to monitor oxide charging as a function of stressing as discussed in Section 2.5.

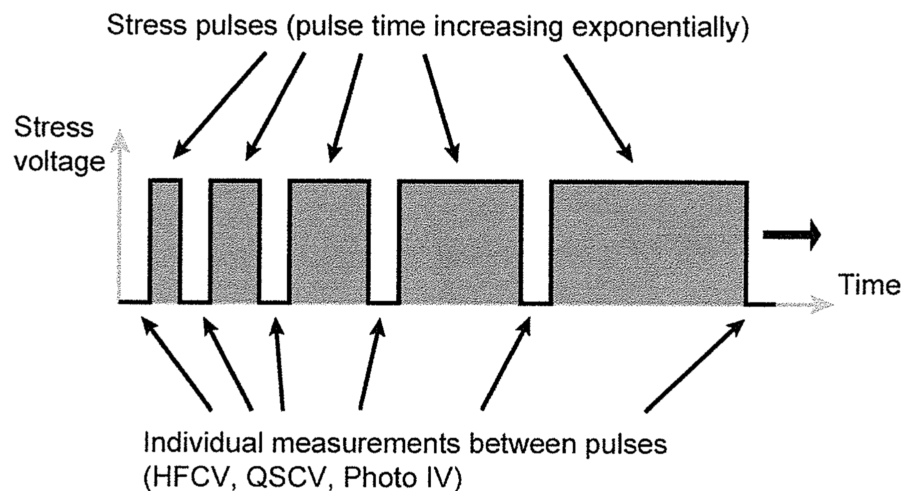


Figure 3.9: The measurement procedure for stressing capacitors.

Chapter 4 Device Fabrication

In this chapter the fabrication steps of the high-κ MOS capacitors studied are discussed. This work used previously fabricated <100> p-type silicon wafers with metal-organic chemical vapour deposited (MOCVD) HfO_2. The actual device fabrication for this work began with the deposition of aluminum, and subsequent patterning. The devices also underwent a backside etch. A discussion of the formation of electrical contacts to the fabricated devices used for testing is included at the end of this chapter.

4.1 Initial Hafnium Dioxide Coated Wafer

The high-κ dielectric that was studied in this research was hafnium dioxide, HfO_2. These films were deposited using the MOCVD process at IBM's T.J. Watson Research Center in Yorktown Heights, New York. These wafers consisted of a lightly doped p-type silicon substrate, a thin intermediate SiO_2 layer and the HfO_2 film. Four different samples of HfO_2 with varying thickness were used for this work. The thicknesses of the HfO_2 films were 30Å, 50Å, 90Å, and 115Å. The intermediate SiO_2 layer was 15Å thick and was common to all wafers. These wafers were fabricated entirely at the T.J. Watson Research Center and transported to the University of Manitoba for use within this research. The wafers were cleaned with de-ionized (DI) water and blown dry with N_2 gas before further processing steps were taken.

4.2 Aluminum Gate Deposition

In order to create the test MOS capacitors a metal gate deposition is required onto the HfO_2 dielectric. Before discussing the deposition of the gate it is prudent to discuss the rationale for using aluminum as the metal gate. The energy band diagram for gold, aluminum, silicon dioxide and p-type silicon is shown in Figure 4.1, including work functions, band-gaps, and electron affinities for these materials. These energies are commonly related to the vacuum level, where an electron is free from the material [20]. A work function is the energy difference between the Fermi level and the vacuum level whereas electron affinity is the kinetic energy required by an electron to move it from the conduction band to the vacuum level [20]. It is shown in Figure 4.1 that the work function of aluminum (4.1 eV [18]) is very similar to the electron affinity of silicon; or in other words, the work function of n-type degenerately doped poly-Si (4.05 eV [20]). It is this material property and the fact that electron injection is desired for this research that aluminum is a better choice as a gate metal than other metals with higher work functions, such as gold (5.0 eV [18]). However, this discussion must be related to hafnium dioxide because it is this material, and not SiO_2, that is in direct contact with the deposited metal. The work function difference between aluminum and the HfO_2 conduction band has been determined theoretically [41] and experimentally [32, 42, 43] to be 1.5 eV and between 1.2 and 2.5 eV respectively. Since the band-gap of HfO_2 has been calculated and measured to be between 5.6 and 6 eV, [41, 42, 43, 44] the choice of aluminum is suitable since the injection of electrons from the metal gate into the oxide conduction band would be (and was) accomplished at lower illumination energy thus avoiding simultaneous hole

injection from the substrate [31, 42]. Aluminum is also an appropriate choice for the metal gate because these test structures require a semi-transparent (for the UV and visible portions of the spectrum, ~300nm to ~ 800nm) gate for photo-injection studies. Aluminum is available and can be reliably deposited by thermal evaporation or sputtering to have a suitable optical transmission as discussed in Section 5.1 [45]. The requirements discussed above prevent the use of a poly-Si gate since such a gate material is highly absorbent at the ultra-violet (UV) and visible wavelengths, requires additional fabrication steps for dopant implantation and high temperature activation anneals [46], and has been shown to suffer from Fermi-level pinning effects when deposited on HfO_2 [47].

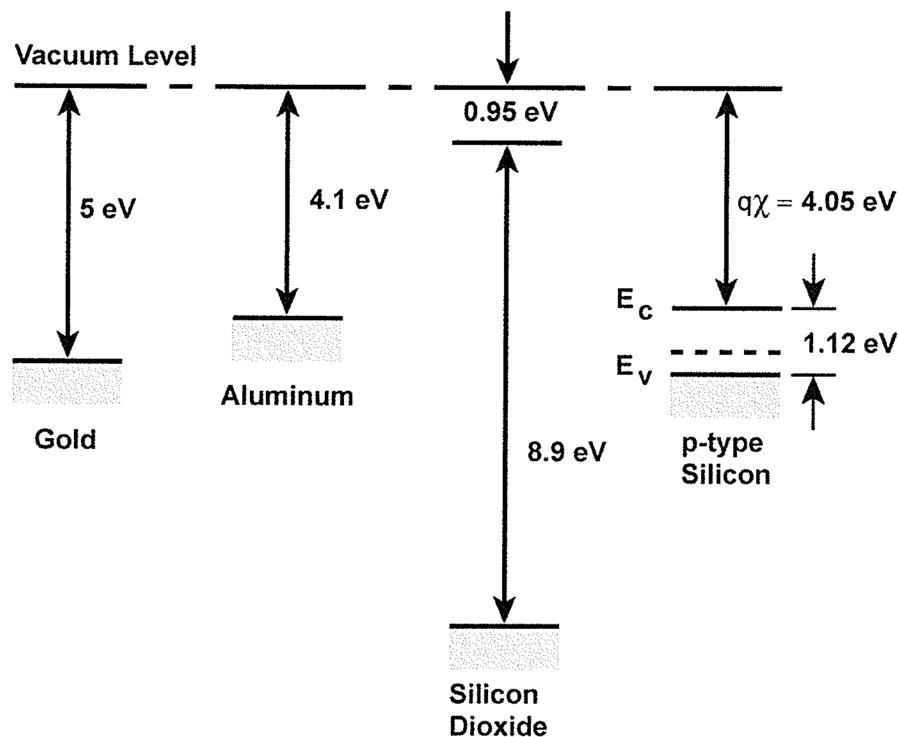


Figure 4.1: The energy band diagram of gold, aluminum, silicon dioxide, and p-type silicon related to vacuum level. After [18, 19, 20].

Aluminum can be reliably deposited by thermal evaporation or DC sputtering and both methods were used to fabricate test devices for this work. For thermal evaporation, the HfO_2 covered wafers were placed into the evaporation chamber which was evacuated to a pressure of $\sim 5\times10^{-7}$ to 1×10^{-6} Torr. The source material (aluminum wire) was wrapped onto a tungsten rod from which it was evaporated and subsequently deposited on a wafer at a rate of ~1-1.5Å/s as measured by a crystal oscillator thickness monitor. The total thickness evaporated was ~140Å, as measured. A more detailed description of the rational for using such an aluminum thickness is presented in Chapter 5. The coated wafers were then removed from the chamber and made ready for the next fabrication step. All devices were fabricated with a blanket aluminum deposition followed by gate patterning steps (described in the following section) rather than using a shadow mask deposition of aluminum. This was done because the shadow mask did not provide a well-defined (high aspect ratio) gate edge for capacitors, and because milling a mask for capacitor structures with areas below 5×10^{-3} cm^2 is difficult.

The alternative aluminum deposition technique used was DC sputtering. The wafers were loaded into the sputtering chamber and evacuated to a pressure of $\sim 1\times10^{-6}$ Torr to purge contaminants prior to the introduction of argon gas into the chamber. Sputtering requires a plasma to excite argon gas to bombard an aluminum target. The released aluminum was deposited on the HfO_2 covered wafers [46]. The deposition conditions used, as discussed in Chapter 5.2, were an argon pressure of 8 mTorr and a DC power setting of 100W. These settings were used to deposit 150Å aluminum films at

a rate of ~7.8 Å/s. Fabrication continued with gate patterning after these blanket depositions.

4.3 Gate Patterning

Patterning the aluminum gate began with the spinning of HPR 506 positive photoresist onto the aluminum covered wafers at a velocity of 3500 RPM for 35 seconds. The spin cycle was immediately followed by a soft bake at 110°C for 1 minute. After a short wait of a few minutes the sample was exposed to UV light for 1.5 minutes within the Karl Suss MJB3 mask aligner. The mask used for lithography featured squares and circles with areas of 1×10^{-5}, 2×10^{-5}, 5×10^{-5}, 1×10^{-4}, 2×10^{-4}, 5×10^{-4}, 1×10^{-3}, 2×10^{-3}, 5×10^{-3}, 1×10^{-2}, 2×10^{-2}, and 5×10^{-2} cm^2. The photoresist was then developed in a Microposit™ 352 developer for ~40 seconds. The wafer was immediately rinsed with DI water and blown dry with N_2 gas before undergoing a hard bake at 120°C for 20 minutes.

The patterned photoresist formed the mask for etching aluminum. The aluminum etchant used was composed of 60% phosphoric acid and 2% nitric acid. The wafer was etched at room temperature for ~50 seconds. This etch was immediately followed with a DI water rinse and N_2 blow dry. The hardened photoresist was removed when the wafer was placed in an acetone bath for a few minutes. The leftover acetone residue was then removed by rinsing the wafer with DI water and a final N_2 gas blow dry completed the gate patterning.

4.4 Backside Etch

Devices that required a backside etch underwent this process after the forming gas anneal or gate patterning process. The role of the backside etch was to remove any oxide that had grown on the silicon substrate in order to form a better back contact during characterization. The etchant used to accomplish this was hydrofluoric acid, HF. The solution was deposited on the backside of the wafer for a minute, then rinsed off using DI water and blown dry with N_2 gas.

4.5 Electrical Contacts

In order to test devices, good ohmic contacts must be made to the gate and substrate of the fabricated MOS capacitors. In this work, electrical contact to test devices was made by a) probing, or b) bonding to a chip carrier.

Probing capacitors was done within a probe station or constructed test fixture as discussed in Chapter 3.1 entitled "Measurement Set-up". Both measurement set-ups required that a tungsten needle make contact to the aluminum gate while a small vacuum held the wafer on a copper substrate. To promote a better (ohmic) backside contact between the copper and silicon wafer, an aluminum-gallium eutectic alloy was used.

If the MOS capacitor required bonding to a leadless chip carrier, LCC, a Kulicke & Soffa 423 Wedge Bonder was used. Before bonding, the test device would be mounted on the gold chip carrier with a conductive silver epoxy to make electrical contact to the substrate. The MOS capacitor on the LCC was then rinsed with DI water and blown dry with N_2 gas to remove any remaining silicon particles from the surface of

device after breaking the fabricated wafer into manageable pieces using a scribe. The wedge bonder was then used to bond a 1 mil (1/1000th of an inch) aluminum wire from the LCC to the aluminum gate of the test capacitor. Electrical contact and damage to the capacitor (in terms of additional leakage current) due to bonding was tested with an IV sweep in the dark.

Chapter 5 The Deposition of Thin Film Aluminum

The use of the internal photoemission (IPE) technique for MOS characterization requires the deposition of a thin semi-transparent aluminum film (< 200Å) for the gate electrode (see Section 2.2). Thermally evaporated aluminum films are discussed, including their deposition thickness and optical transmission. The deposition of aluminum by DC sputtering is also mentioned briefly, including the optimal deposition settings for the thin-film depositions.

5.1.1 Thermally Evaporated Aluminum Films

A brief introduction to the thermal evaporation process was given in Section 4.5. A crystal oscillator thickness monitor measures the deposition thickness of these films during the process. For the purpose of this research, verification of this thickness was done using a profilometer (Tencor Alpha-Step 500 Surface Profiler). The deposition thickness of various aluminum films deposited on glass slides as measured by the crystal oscillator monitor and the profilometer are shown in Table 5.1. For accurate step height measurements using the profilometer, the blanket depositions of aluminum were etched to create a high-aspect ratio step between the glass substrate and the deposited film. As a result, the profilometer required only a short sweep (< 500 μm) to obtain the step height. The deposition rate for all samples was in the range of 1-1.5 Å/s.

Table 5.1: The measured deposition thickness of several thermally evaporated aluminum thin films. The thickness of the films was measured during deposition with a crystal oscillator thickness meter and after deposition with a profilometer.

Sample	A	B	C	D	E	F	G	H
Crystal Oscillator Thickness (Å)	100	120	125	140	150	150	160	240
Profilometer Thickness Data (Å)	78	110	112	181	167	149	181	197
	45	101	121	132	177	177	209	206
	86	93	98	152	157	154	178	223
	87	120	105	143	142	166	164	189
	107	86	120	172	151	175	186	215
	99	103	102	123	166	134	205	191
	95	100	89			178	172	210
	87	101	127					197
	103							199
Average (Å)	87.4	101.8	109.3	150.5	160.0	161.9	185.0	203.0
Std. Dev. (Å)	18.7	10.2	13.0	22.6	12.6	16.7	16.6	12.0

The primary reason for measuring the aluminum deposition thickness is to verify that the films are optically transparent. The measured transmission probability, P_T, for the samples A through H of Table 5.1 are shown in Figure 5.1. As expected from equation (2.11), the thinner films are more optically transparent. The wavelengths used for these measurements (550 to 750 nm) are in the visible portion of the electromagnetic spectrum. Lower wavelengths (UV wavelengths) were not used as the glass slides used for these measurements have impurities that prevent optical transmission at wavelengths

below 350 nm and the transmission data at those wavelengths is more noisy due to peaks in the Hg spectrum. It can be shown, using known optical constants for evaporated aluminum, that the transmission probability is constant for wavelengths between 200 nm and 800 nm [45], which is confirmed in part by the optical transmission measurements in Figure 5.1.

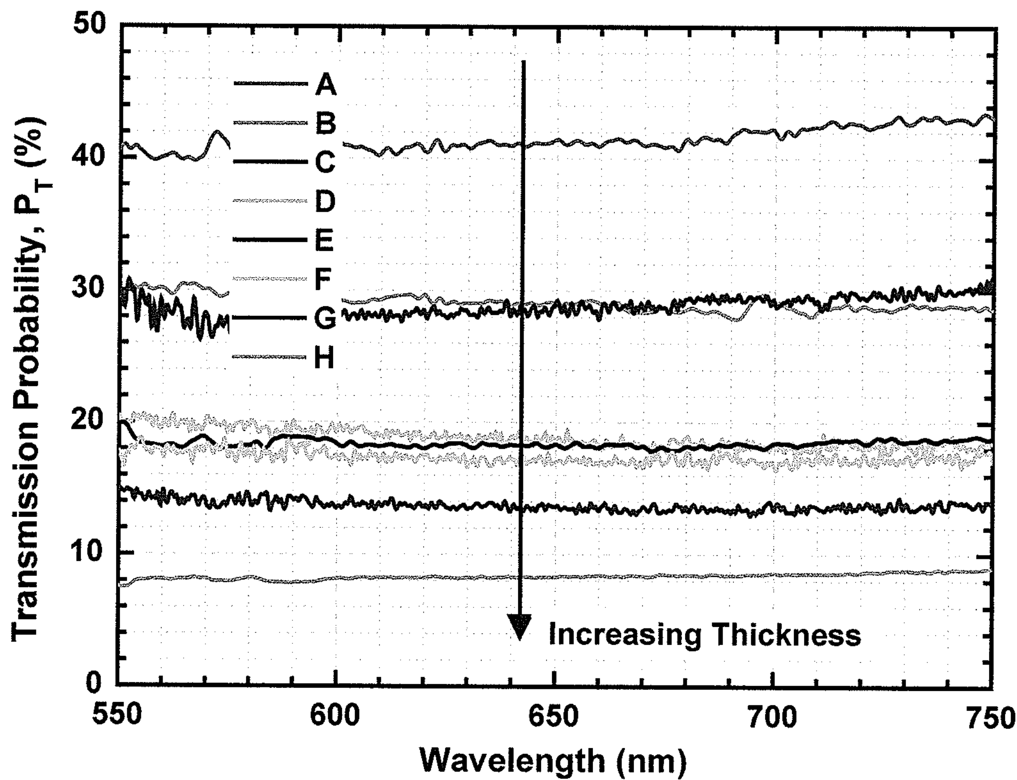


Figure 5.1: The transmission probability of thermally evaporated aluminum thin films over a portion of the visible electromagnetic spectrum, 550 to 750 nm. As the thickness of the films decreases, transmission probability increases. The samples that were measured are those shown in Table 5.1.

Since the transmission probability is approximately constant over the wavelengths shown in Figure 5.1, an average value was calculated, as given in Table 5.2. The samples

listed in Table 5.2 correspond to the samples in Table 5.1 and Figure 5.1. The average transmission probability, P_T, and the film thickness values, z, can be used to obtain the extinction coefficient, α, as given by equation (2.11) and shown in Figure 5.2. The linear fit of the data results in an extinction coefficient value of 0.11 ± 0.01 nm^{-1}. This value is in good agreement with the calculated value of ~0.15 nm^{-1} which was obtained using a table of optical constants for aluminum [45].

Table 5.2: The transmission probability, P_T, averaged over a portion of the visible spectrum, 550 to 750nm, shown in Figure 5.1.

Sample	A	B	C	D	E	F	G	H
P_T Average	0.415	0.290	0.288	0.184	0.188	0.173	0.137	0.083
P_T Std. Dev.	0.009	0.006	0.009	0.003	0.007	0.004	0.004	0.003

For the purpose of this work, it is sufficient to assume that deposited films of aluminum below ~160Å of thickness provided reasonable transmission probabilities (> ~15%) for testing purposes. From the published optical constants it is also known that the transmission probability does not decrease until wavelengths are below ~200 nm, which is lower than the range of energies that are of interest for this work (wavelengths greater than 300 nm). These results imply that thermally deposited films with thickness of 140Å are suitable for photoinjection experiments that require substrate illumination through a transparent gate.

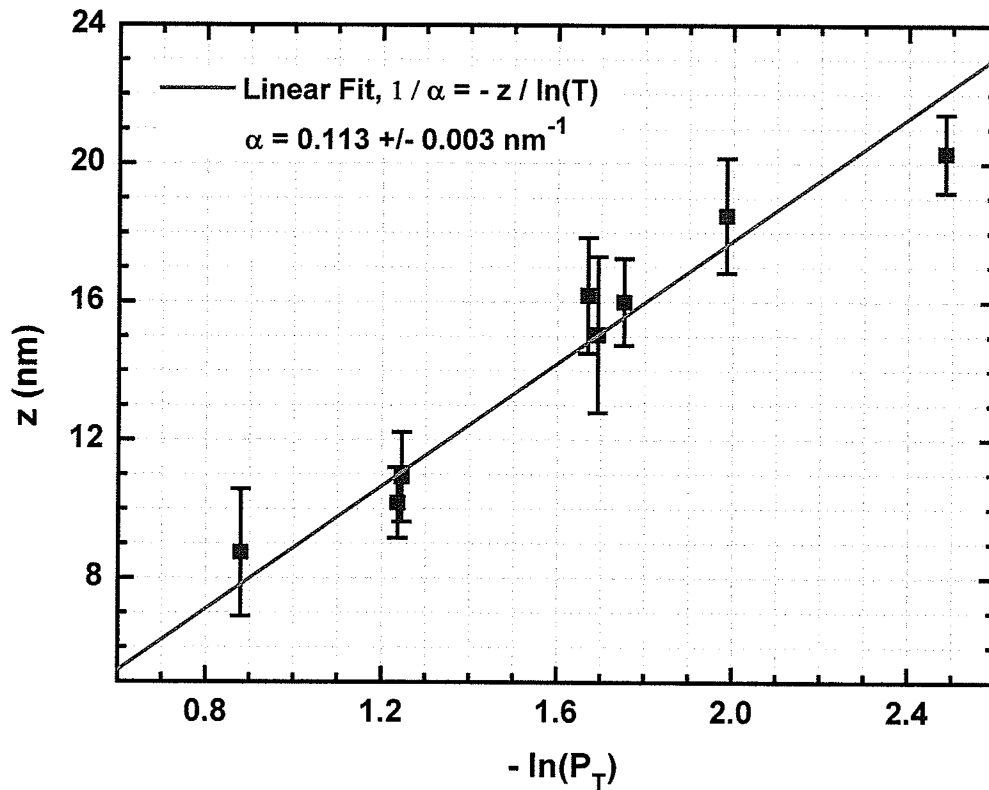


Figure 5.2: The extinction coefficient, α, extracted from a linear fit of thermally evaporated thin film thickness, z, and the natural logarithm of the transmission probability, P_T, as given by equation (2.11)

5.1.2 DC Sputtered Aluminum Films

The deposition of aluminum by DC sputtering is complicated by the inability to monitor thickness in real-time. Therefore, the optimal settings for the DC sputtering process must be determined in advance for consistent depositions. The deposition thicknesses of various sputtered films as measured using a profilometer are listed in Table 5.3.

Table 5.3: The average deposition thicknesses of aluminum sputtered thin films as measured with a profilometer.

Wattage (W)	Argon Pressure (mTorr)	Time (s)	Profilometer Step Heights				
			# 1 (Å)	# 2 (Å)	# 3 (Å)	Average (Å)	Std. Dev. (Å)
100	8	600	3495	3490	3470	3485	13
100	16	600	2738	2814	2744	2765	42
100	25	600	2376	2287	2354	2339	46
100	8	26	192	200	206	199	7
100	8	15	122	116	121	120	3
100	8	16	124	119	121	121	3
100	8	20	164	140	155	153	12
50	8	30	123	120	124	122	2

The samples listed in Table 5.3 were all sputtered at or below the 100W DC power setting, which was necessary to limit the deposition rate. At higher power setting, the deposition rate is much too high for controllable thin films due to the increased bombardment of the aluminum target by argon ions. The first three samples listed in Table 5.3 underwent long deposition times (5 minutes) to obtain an accurate measurement of surface roughness that was needed to differentiate between possible argon pressure settings. The surface roughness of thin films (i.e., films thinner than 100 nm) was more indicative of the surface roughness of the underlying substrate (glass slide) than of the deposited film. The surface roughness data is shown in Table 5.4. From these

data, it is clear that the lower pressure setting, 8 mTorr, for argon represented the best pressure setting for the desired film condition.

Table 5.4: The average surface roughness of aluminum sputtered thin films as measured with a surface profilometer.

Wattage (W)	Argon Pressure (mTorr)	Time (s)	Profilometer Roughness				
			# 1 (Å)	# 2 (Å)	# 3 (Å)	Average (Å)	Std. Dev. (Å)
100	8	600	20.5	21.1	25.5	22.37	2.73
100	16	600	69.6	83.5	63.9	72.33	10.08
100	25	600	57.6	54.3	52.5	54.80	2.59

The five samples listed last in Table 5.3 have deposition thickness that is suitable for transparent gate electrodes (thickness less than 200Å). These samples also had deposition times that were reasonable for controlling thickness reliably (i.e., a long enough time to shutter the sample away from the sputtering area). The deposition rates for these samples are shown in Table 5.5. The deposition rates for thin films deposited at the 100W DC power setting and the 8 mTorr argon pressure setting were very consistent for the thin films measured. The average deposition rate for those settings was 7.7 ± 0.3 Å/s. As a result, these settings were used for all DC sputtered aluminum films. The 50W DC power setting also provided suitable films, but was not used because of reliability (several depositions at this power setting failed to sputter any aluminum).

Table 5.5: The average deposition rate of aluminum sputtered thin films as determined from the average aluminum thicknesses given in Table 5.3.

Wattage (W)	Argon Pressure (mTorr)	Time (s)	Rate Average (Å/s)	Rate Std. Dev. (Å/s)
100	8	600	5.8	0.1
100	16	600	4.6	0.1
100	25	600	3.9	0.1
100	8	26	7.7	0.3
100	8	15	8.0	0.2
100	8	16	7.6	0.2
100	8	20	7.7	0.6
50	8	30	4.1	0.1

Average
7.7 +/- 0.3 Å/s

The optical transmission curves for three films listed in Table 5.3, the 120Å, 199Å, and 122Å films, are shown in Figure 5.3. The two films with similar thickness, 120Å and 122Å, but deposited at different DC power settings, 100W and 50W, have equal optical transmission probabilities. The thicker film, on the other hand, has a much lower transmission probability, as expected. The transmission probabilities of these sputtered films are very similar to those in Figure 5.2 for thermally evaporated films with similar thickness, which would imply that these are also suitable for gate electrode deposition.

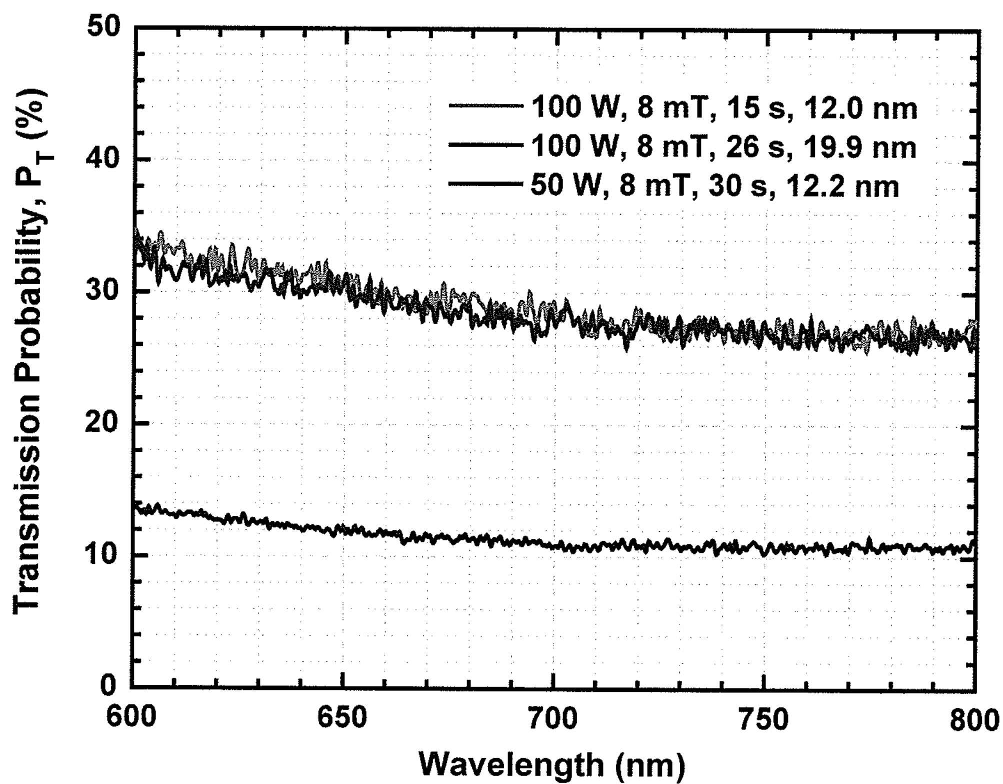


Figure 5.3: The transmission probability of DC sputtered aluminum thin films over a portion of the visible electromagnetic spectrum, 600 to 800 nm. The thin films measured are shown in Table 5.3, 5.4 and 5.5.

Chapter 6 Barrier Height Measurements

In this chapter the extraction of interfacial barrier heights using internal photoemission measurements is discussed for high-κ hafnium dioxide capacitors. In this research work, the barrier height refers to the energy difference between the Fermi level in the metal, or the conduction band of silicon, and the conduction band of the insulator. These measurements are important in determining the photon energy, E_{ph} required for both photocurrent and charge injection measurements. Barrier height measurements also provide necessary information pertaining to the electronic structure of the MOS devices under test. Before discussing barrier height measurements for gate and substrate electron injection, a brief discussion is given regarding the optical system used for these measurements.

6.1.1 Optical Measurements

A requirement for any optical measurement is that the optical apparatus must be fully characterized for spectral response, bandwidth and/or transmission. In this research work, an Hg arc lamp was used as a light source. The spectrum of an Hg arc lamp, as measured by the optical system set-up described in Section 3.1.1, is shown in Figure 6.1. The Hg spectrum has numerous peaks at wavelengths corresponding to transitions between energy states in the Hg gas. The peaks labelled from A to G in Figure 6.1 are listed in Table 6.1, along with their known wavelengths and photon energy. These peaks in the optical spectrum of the light source complicate optical measurements, specifically when sweeps of photon energy are required, because these peaks must be adequately

resolved. For this reason, sweeps of photon energy are actually taken using sweeps of wavelength steps. This is due to the linearity of the peaks to wavelength as opposed to the inverse relation between photon energy, E_{ph}, and wavelength, λ, which is given by

$$E_{ph} = h \cdot \nu = \frac{h \cdot c}{\lambda} \tag{6.1}$$

where h is Planck's constant, ν is the optical frequency, and c is the speed of light.

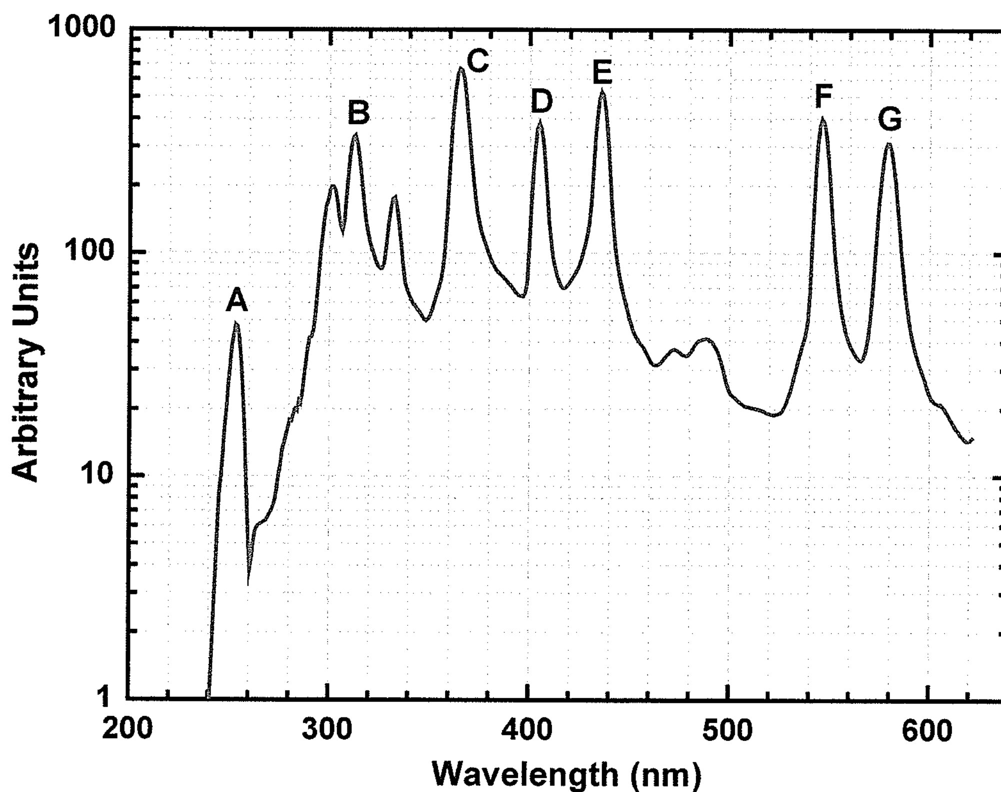


Figure 6.1: The Hg arc lamp spectra as measured with the use of a monochromator and calibrated silicon photodetector (the measurement set-up is discussed in Section 3.1.1).

One important parameter to consider when discussing an optical system is wavelength resolution. For MOS photoinjection studies, appreciable currents are required; therefore, a higher transmission is preferred rather than resolution. However,

for barrier height measurements spectral resolution is more desirable. For this research, the input and output slits of the high-resolution monochromator were set to their widest setting (~2 mm) for increased transmission. Assuming that an error of ± 0.1 eV would be acceptable for the photoinjection measurements, at the shortest wavelength peak (peak A in Figure 6.1), the resolution of the optical system would need to be 103.8 Å, as shown by the error window in Figure 6.2. The same calculation for peak B (the shortest wavelength used in this research) results in a required resolution of 158 Å. As wavelength increases, the acceptable resolution also increases due to the inverse relationship given by equation (6.1). As an upper bound to the resolution of the optical system used in this research, consider the measured Hg spectrum in Figure 6.1. The full-width at half-maximum, FWHM, values for peaks A-G are listed in Table 6.1. The FWHM values for all peaks are significantly less than the calculated values for a ± 0.1 eV energy resolution. This is illustrated by Figure 6.2, in which the ± 0.1 eV error window is wider than the FWHM of the peak at the short wavelength of 2536.52 Å. These calculations imply that bandwidth for optical measurements in this research work are within an error of ± 0.1 eV, despite the monochromator being set-up for transmission rather than spectral resolution.

One important point to note in this dissertation is that most photoinjection studies requiring the use of illumination use photon energies of either 3.4 eV or 4 eV. These energies correspond to the Hg arc lamp peaks at the wavelengths 3650.15Å and 3129Å as shown in Table 6.1. These peaks are chosen specifically for their high photon fluxes.

Table 6.1: The wavelengths and photon energies of the most dominate peaks in the Hg arc lamp spectra and the measured FWHM of these peaks from the data shown in Figure 6.1.

Known Peak (Figure 5.4)	Known λ [see ref. 48] (Å)	E_{ph} at Known λ (eV)	Max. λ at HM (Å)	Min. λ at HM (Å)	FWHM (Å)
A	2536.52	4.89	2569	2493	76
B	3129.00	3.96	3173	3081	92
C	3650.15	3.40	3700	3610	90
D	4046.57	3.06	4085	4011	74
E	4358.33	2.84	4397	4321	76
F	5460.74	2.27	5503	5426	77
G	5787.00	2.14	5840	5743	97

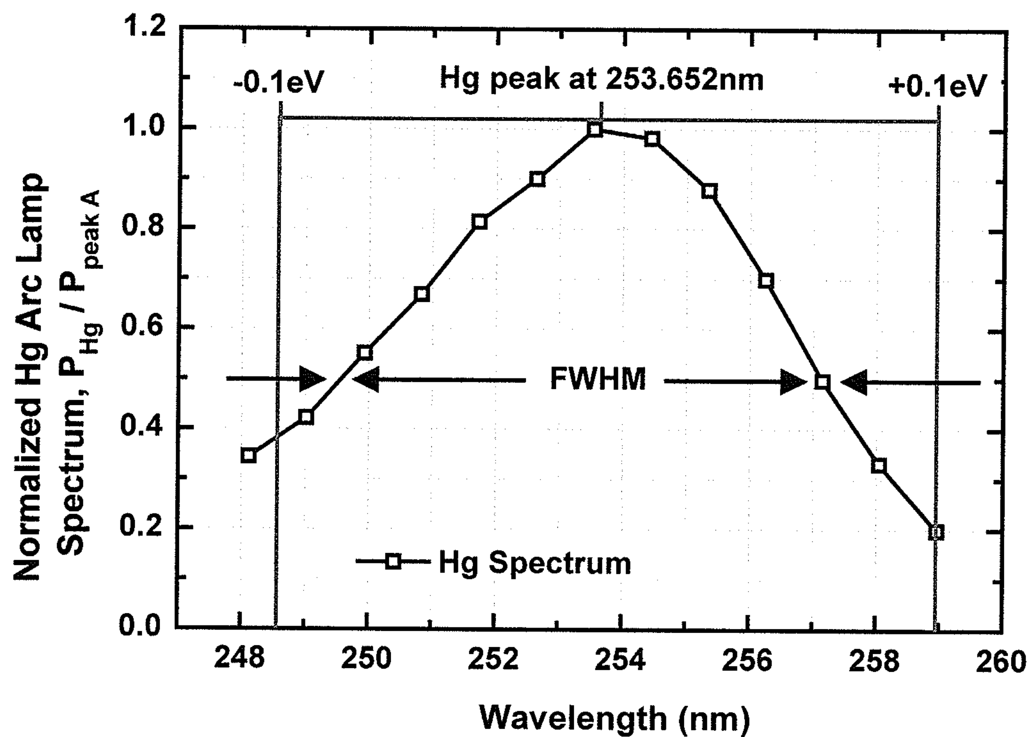


Figure 6.2: The measured Hg arc lamp spectrum shown in Figure 6.1 normalized to peak A (λ = 2536.52Å). The measured FWHM value for this peak is within the calculated ± 0.1 eV error window for the peak (shown as a red line).

6.1.2 Gate Injection

To determine the barrier height between the gate electrode, aluminum, and the insulator, hafnium dioxide, a spectral measurement of photocurrent (leakage current) is required. Such a measurement for a 5×10^{-4} cm^2 and a 5×10^{-3} cm^2, 90 Å HfO_2 capacitor is shown in Figure 6.3. The applied bias used for this measurement was –1.5 V. The lower plot in Figure 6.3 represents the relative number of photons incident on the gate as provided by the optical system (i.e., the Hg arc lamp spectrum after transmission through a monochromator, a filter and lenses). A comparison of the two plotted curves reveals that an increase in leakage current occurs at photon energy greater than 2.5 eV, due to the optically excited electrons overcoming the interfacial energy barrier. Unfortunately, the sensitivity of this measurement depends on several factors, such as the amount of dark leakage current for the device, the noise level for low (i.e., less than 1 pA) DC current measurements and other optical considerations that can determine the photon flux density. The capacitor with the 10× larger area in Figure 6.3 has correspondingly ~10× greater leakage current. If the photocurrent does not scale with capacitor area, as is the case in Figure 6.3, the detectable limit of the photocurrent contribution is at higher photon energy (~2.7 eV for the larger capacitor, compared to less than 2.4 eV for the smaller capacitor). The reason for less photocurrent density can be attributed to issues relating to the focusing of the light source and variations in aluminum gate thickness, both of which affect the number of photons absorbed by the gate.

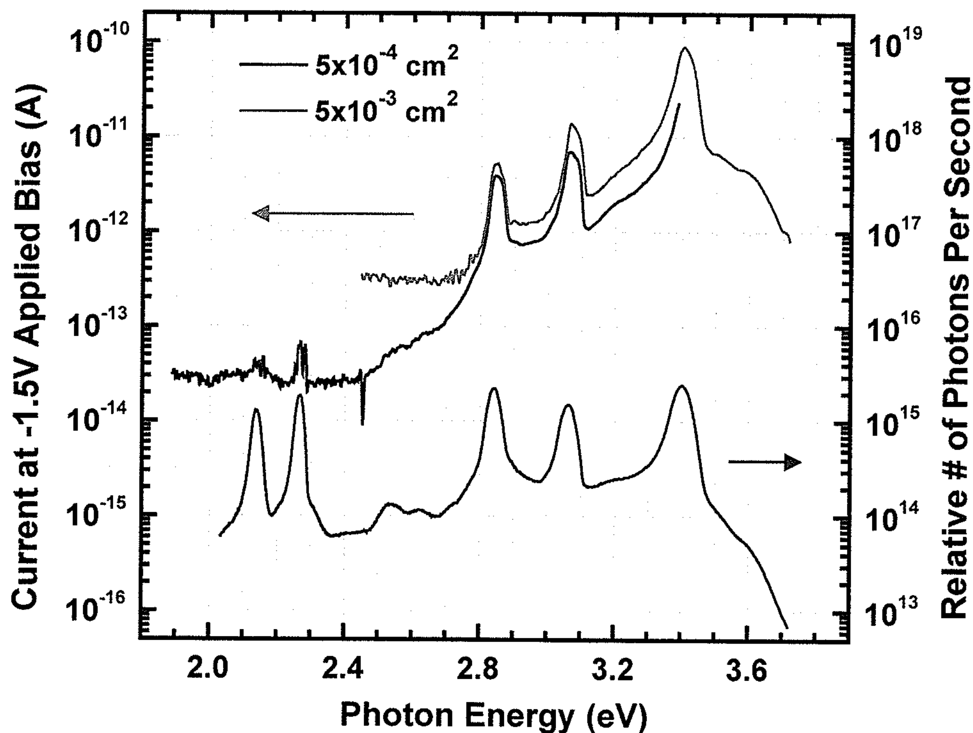


Figure 6.3: The measured leakage current of a 5×10^{-4} cm^2 (black line) and a 4×10^{-3} cm^2 (red line), 90Å HfO_2 capacitor as a function of photon energy of illumination. An applied bias of -1.5 V was used for these DC measurements. The relative number of photons per second for the optical system is also shown.

To determine the effective barrier height, the measured photocurrent and relative number of photons is used to calculate the relative yield, as given in Section 2.3.1. The square root of relative yield is plotted versus photon energy in Figure 6.4 because the best model to use for an injecting electrode that is a metal is the square root of the relative yield as shown in Table 2.1. As shown in the Figure 6.4, a linear fit cannot be made over the entire range of photon energy displayed. At photon energies less than 2.8 eV the photocurrent measured is attributable to leakage current, so the data below this energy are not relevant for the barrier height measurement. At ~3.2 eV an observable increase in relative yield occurs. This is consistent with the internal photoemission results from [12]

where an increase in relative yield was also noted ~3.2 eV. In that study, electrons were also injected from an aluminum electrode into HfO_2 and a barrier height of 2.5 ± 0.1 eV was determined by a linear fit of the data over the photon energy range of ~2.6 to ~3.1 eV. If a similar energy range is used in this work, the linear fits of Figure 6.5 can be used to extrapolate the effective barrier height. One should note that the "noise" in the relative yield data plotted in Figures 6.4 and 6.5 corresponds to the peaks in the Hg arc lamp spectrum. The peaks in the spectrum are large in comparison to the remainder of the spectra and have a finite width, which accounts for the "noise" in the relative yield calculation.

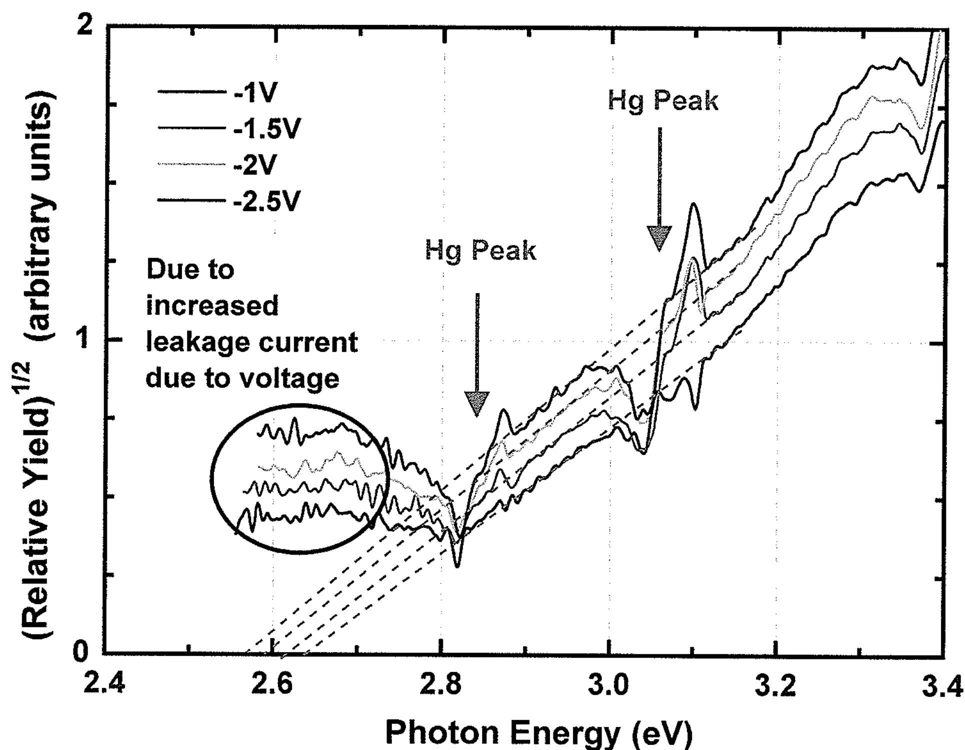


Figure 6.4: The square root of relative yield plotted as a function of photon energy for a 5×10^{-3} cm^2, 90Å HfO_2 device. The locations of peaks in the Hg spectrum are also shown.

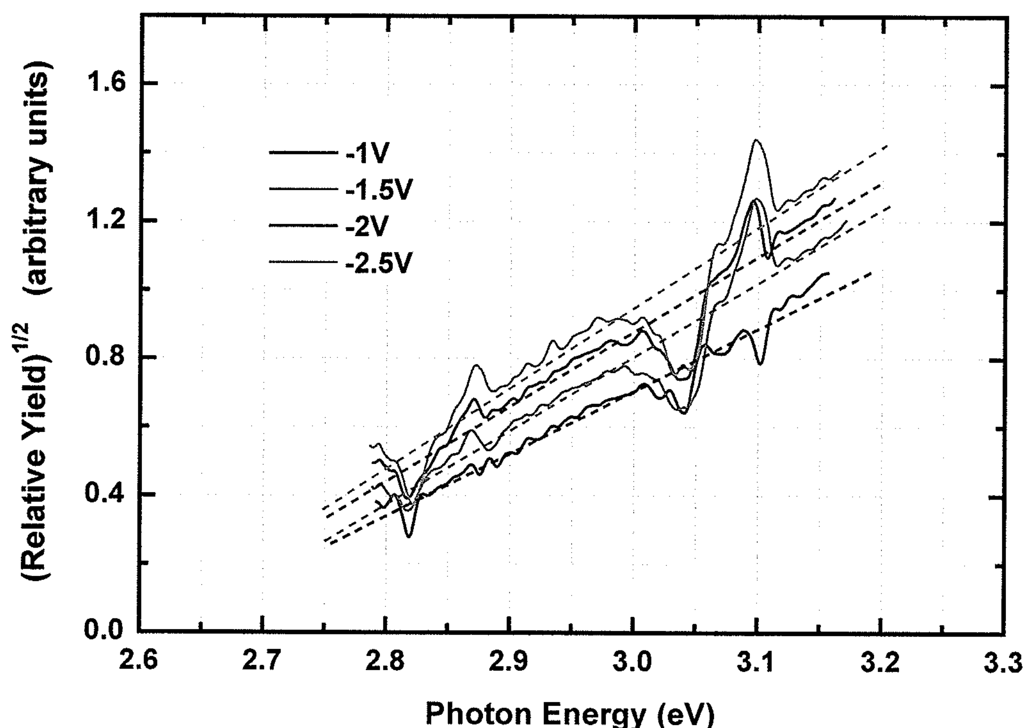


Figure 6.5: The square root of relative yield plotted as a function of useful photon energy for effective barrier height extrapolation. The dashed lines are linear fits to the relative yield data over the shown energy range.

The extrapolations of linear fits shown in Figure 6.5, yield the effective barrier heights shown in Figure 6.6, where the effective barrier height is plotted versus applied bias. From this plot it is clearly evident that the effective barrier height is independent of the applied bias and therefore the electric field. An average barrier height, for all values of applied bias results in an effective barrier height of 2.6 ± 0.1 eV. If the same methodology is used to determine the effective barrier height for the smaller area (2×10^{-4} cm^2) device shown in Figure 6.3, a barrier height with 2.6 ± 0.1 eV is also obtained. These barrier heights are consistent with the current knowledge of the HfO_2 band

structure [12] where previous values have been calculated to be ~2 eV [41] and measured to be 2.5 ± 0.1 eV [12].

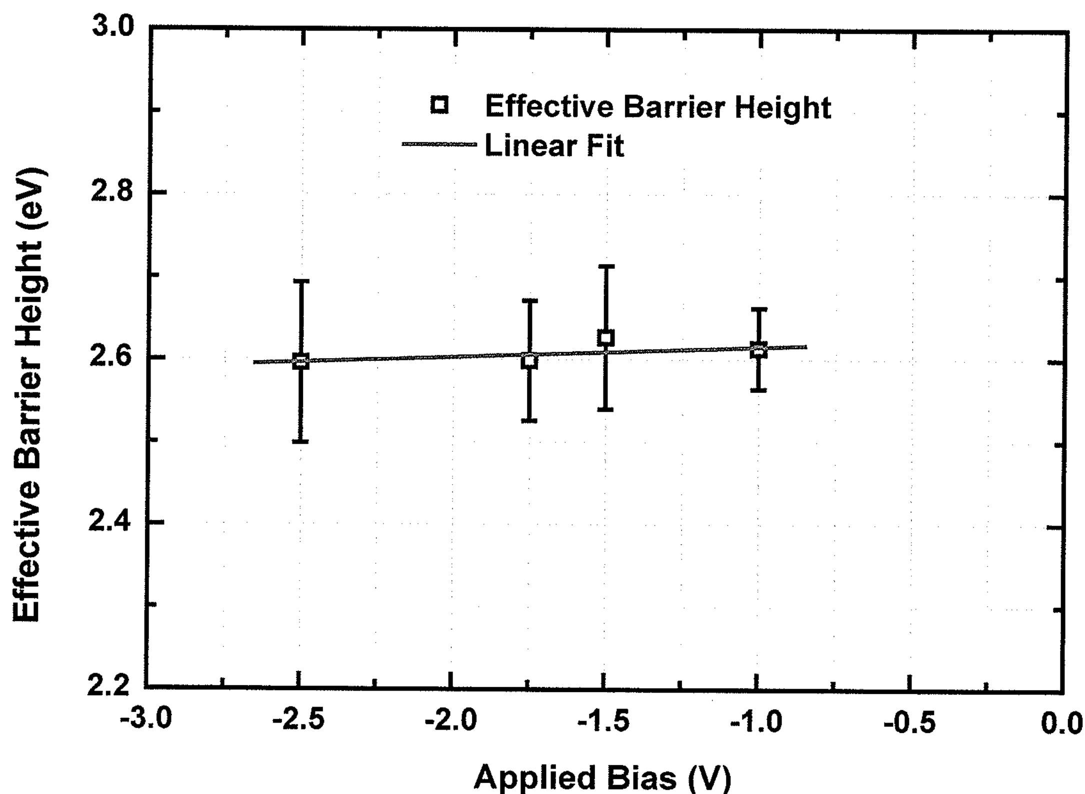


Figure 6.6: The extrapolated effective barrier heights as a function applied bias for the linear fits shown in Figure 6.5.

As briefly mentioned above, no field dependence can be extracted for the barrier height measurements as shown in Figure 6.6. A possible explanation for this observation can be made if the amount of oxide charge trapped in these films is considered, because the effective barrier height also depends on the amount of charge within the insulator, as discussed in Section 2.6.2. To observe the electric field dependence, it is assumed that oxide charge is not within the dielectric and that photoinjection is purely a function of

applied field. However, this is not the case for the samples used in this research. As discussed in Chapter 7, these MOS capacitors readily trap electrons under negative applied biases. During the measurements used to extrapolate the effective barrier height trapped oxide charge has been noted. This is known because the high-frequency capacitance-voltage response before and after the measurement has a shift of at least 0.35 V for all applied biases, indicative of oxide charge trapping (see Section 2.5.1). The trapping of negative charge in these films is unavoidable, since a DC leakage current measurement must be made for extracting photocurrent. Therefore, the length of measurement time and the negative applied bias always resulted in charge trapping. To minimize the effect of oxide charge on the measurement, all devices were detrapped to some initial state (i.e., similar HFCV responses as discussed in Section 8.1) before the photocurrent sweep began.

The role that trapped oxide charge plays on the effective barrier height extraction is best demonstrated by the data shown in Figure 6.7. These photocurrent measurements were all taken at –1.5 V applied bias on a 2×10^{-3} cm^2, 90Å HfO_2 device, but the initial charged state of the device was varied. The HFCV responses prior to the measurement of photocurrent are shown in Figure 6.8. The observable decrease in relative yield as a function of increased trapped charge is expected because the trapped charge will lower the effective electric field near the injecting surface, which increases both barrier height and zero field distance (Section 2.3.1). The barrier height dependence on trapped charge is evident by the linear fits of relative yield shown in Figure 6.7 (i.e., the barrier height increases from ~2.6 to ~2.7 to ~2.8 eV). It should be noted that the HFCV responses following the photocurrent sweeps were indicative of similar levels of trapped oxide

charge. This is evident from the relative yield data at photon energy greater than ~4eV, where the photocurrents measured are approximately equal.

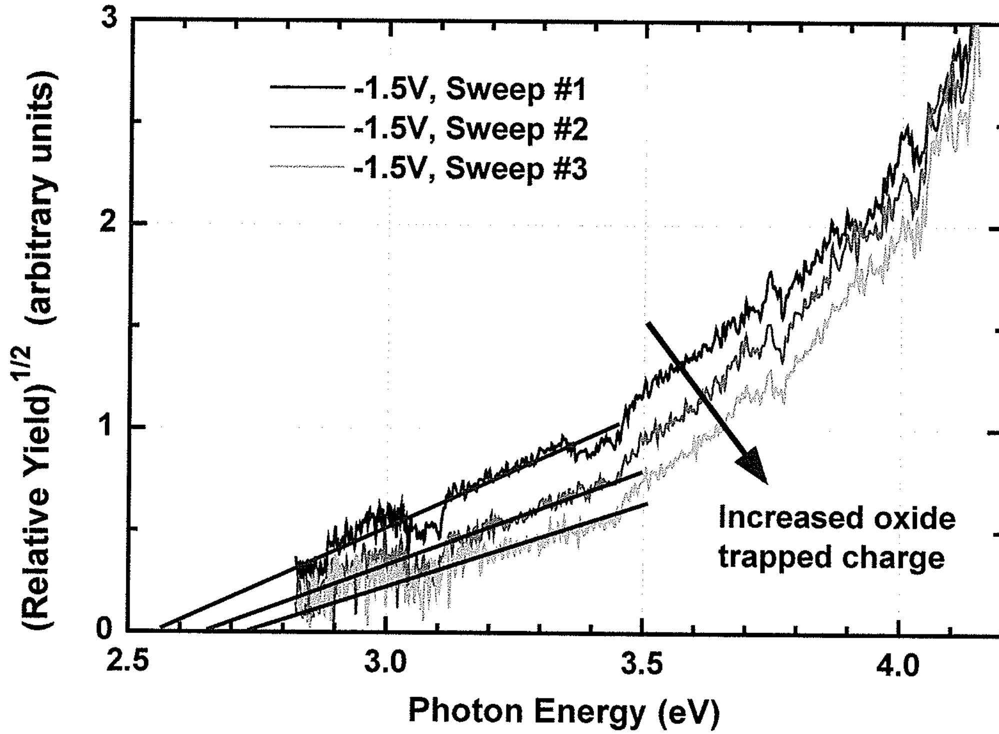


Figure 6.7: The effects of trapped oxide charge on photoinjection and barrier height determination. The test device was a 2×10^{-3} cm^2 90Å, HfO_2 capacitor. The initial charged state of the capacitor, as given by a HFCV measurement, prior to each wavelength sweep is shown in Figure 6.8.

For the purposes of this research, the actual barrier height (i.e., the zero field barrier height extracted from the electric field dependence) is less of a concern. It is more important that internal photoemission of electrons is possible at photon energies greater than the effective barrier height of 2.6 eV. For MOS characterization, reasonable injection rates (i.e., large photocurrents) are desired, therefore, photoinjecting electrons at

the photon energies greater than 2.8 eV corresponding to the peaks in the Hg spectra is desirable.

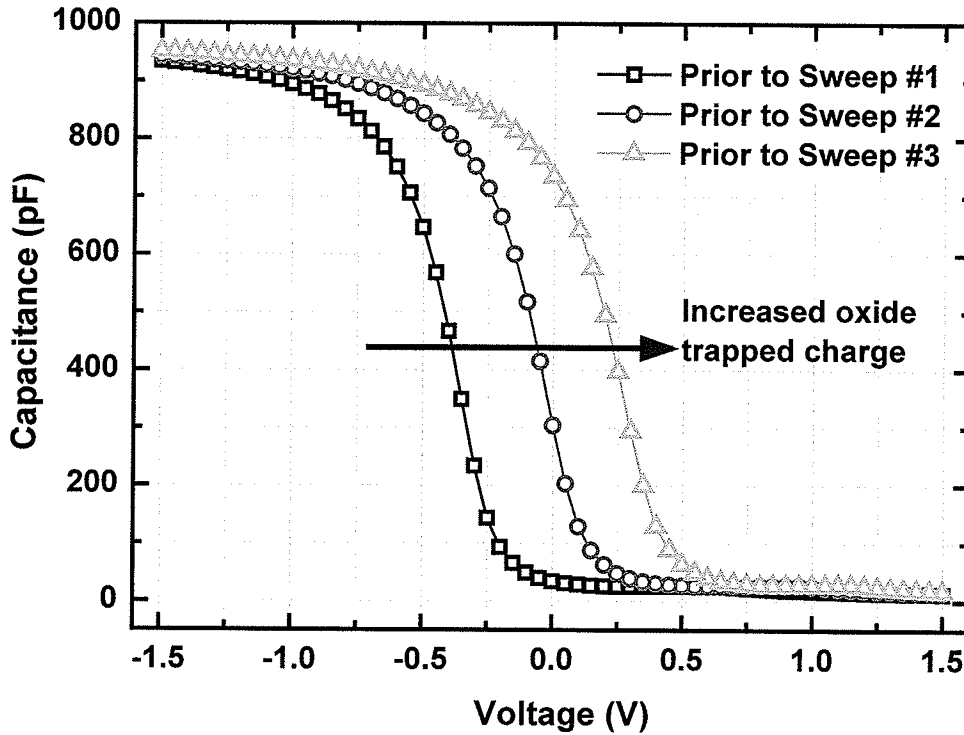


Figure 6.8: The initial HFCV response of a 2×10^{-3} cm^2 90Å HfO_2 capacitor prior to the start of the wavelength scans shown in Figure 6.7.

6.1.3 Substrate Injection

The determination of an effective barrier height for substrate electron injection is very limited for the MOS devices used in this research for several reasons. Firstly, the substrate being used for these devices is very lightly doped p-type silicon, which is not ideal for substrate injection. Under positive applied biases, the capacitor is in the inversion regime, as shown by Figure 6.9. As a result, a large amount of band bending

occurs which means that the effective barrier height varies with depth and quantization of minority carriers occurs, which also affects photoinjection [26]. Secondly, as applied bias increases, the leakage current contributions due to tunnelling get larger because of the asymmetry in the band structure, as shown in Figure 6.9. As bias increases, the conduction band of the high-κ layer is lowered with respect to the silicon substrate. Therefore, as bias is increased the tunnelling distance decreases. So, the electrons within the conduction band of the silicon have an increased probability of tunnelling through the thin intermediate layer. This is illustrated in Figure 6.9, where the band structure for the 90 Å HfO_2 devices used in this research is shown with a 2 V bias applied across the entire dielectric stack. The increased tunnelling current is problematic for the determination of barrier height because it will mask any photocurrent that is generated.

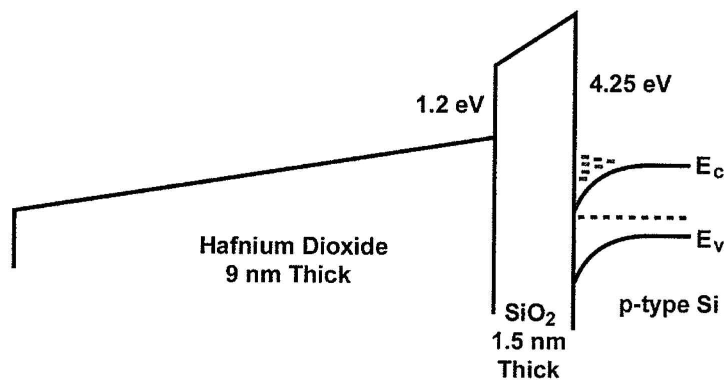


Figure 6.9: The band structure of the 90Å HfO_2 devices with a 2 V voltage drop across the dielectrics. The diagram is drawn to scale. A 4.25 eV SiO_2 barrier is assumed for the silicon valence band, and a 1.2 eV conduction band offset between the dielectrics. It is also assumed that the $\varepsilon_{Si} = 3.9 = \varepsilon_{high\text{-}\kappa}/4$.

The measured current is shown in Figure 6.10 as a function of photon energy for a 2×10^{-3} cm^2, 90 Å HFO_2, device for applied biases of 0.75, 1.25, and 1.75 V. From these

data it is evident that the current has a large voltage dependence (i.e., ~1 decade increase in current for every 0.5V increase in bias at ~2.5 eV). Despite this, the measurements for all three applied biases showed evidence of a photocurrent (i.e., the peaks in the Hg spectrum (the top curve shown in Figure 6.10) correspond to the peaks in the measured current).

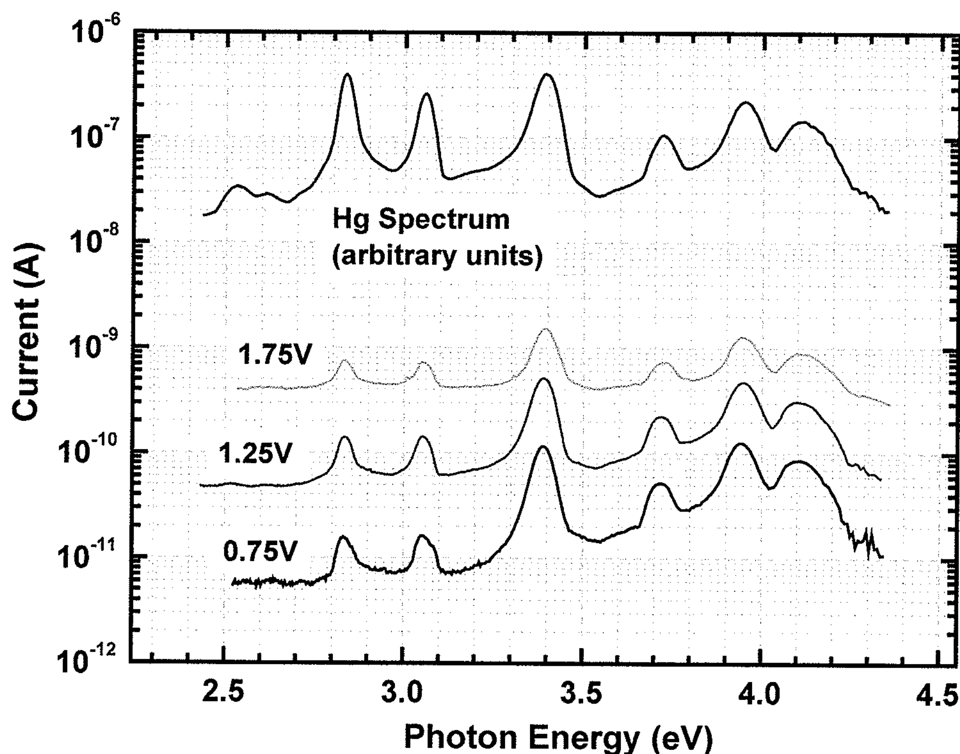


Figure 6.10: The measured leakage current of a 2×10^{-3} cm^2, 90Å HfO_2 capacitor as a function of photon energy of illumination using positive applied biases of 0.75, 1.25, and 1.75 V. The spectrum of the illumination is also shown.

The argument that is made in the following section is that there is no possibility of extracting an effective barrier height from these measurements. At the lowest applied voltage (0.75V) the measured current most resembled a photoinjected current (i.e., an

increase in measured current with increasing photon energy). This trend was observable when comparing the relative heights of the peaks in the measured current to the relative heights of the peaks in the Hg spectrum. At higher applied bias, this was not the case. As a result, obtaining an effective barrier height from these measurements is not possible. However, it should be noted that the magnitude of the measured current at the peak located at 3.4 eV is much larger in relation to the peaks at lower photon energy (perhaps indicative of the onset of photoinjection from the silicon valence band into the device). For the purposes of this work, tests requiring substrate injection used the 3.4 eV peak, or peaks at greater photon energies, thereby, assuring higher injected current levels.

Chapter 7 High-κ Capacitor Characterization

In this chapter hafnium dioxide high-κ MOS capacitors are characterized using high-frequency capacitance-voltage (HFCV), current-voltage (IV), and quasi-static capacitance-voltage (QSCV) measurements. The HFCV techniques are discussed, including a) the justification of the choice of the measurement parameters, b) the measurement of the oxide capacitance and its relationship to device area, and c) the extraction of the substrate doping concentrations. Subsequently, dark IV measurements are presented and the difference between particle and displacement currents is introduced. Lastly, a discussion of the measurement of displacement currents is included. These measurements were performed with ramped voltage sweeps and/or stepped voltages using a parameter analyzer for obtaining the QSCV response of the high-κ capacitors.

7.1 High-Frequency Capacitance-Voltage Characterization

The HFCV response of high-κ MOS capacitors is important for characterizing devices and provides vital material and device information, including the effective oxide capacitance of a gate stack, the substrate doping concentration, and the quantity of oxide trapped charge. In the following sections, the HFCV response of the HfO_2 devices to various measurement parameters is discussed, including extraction of the oxide capacitance, and substrate doping concentration.

7.1.1 Selection of Measurement Parameters

The typical HFCV response of an HfO_2 device is shown in Figure 7.1. This measurement began at an applied gate voltage of 1.5V, was swept to a gate voltage of –2V, and then swept back into inversion to a gate voltage of 1.5V after a 2-second hold time in accumulation. The measurement was taken using a step voltage of 50mV, the value used for all HFCV measurements presented in this dissertation. This step voltage was chosen since it provided enough data points in the depletion regime where the measured capacitance changes the greatest as a function of gate voltage (~-400 pF/V as shown in Figure 7.1). This step voltage was also chosen to minimize the number of data points in an effort maintain a short measurement time. The latter justification is primarily a concern for HFCV measurements during the charge injection tests discussed in Section 8.1 where measurement time/delays is crucial. In an effort to explore the effect of step delays, in Figure 7.1, four HFCV responses are shown with varying step delay times. The change in measurement time from ~17 to ~60 seconds did not affect the HFCV response of the device to any measurable degree.

The measurements plotted in Figure 7.1 were taken using a 100 kHz, 30 mV peak-to-peak AC test signal. The 30 mV peak-to-peak value was chosen because similar tests using 10 mV and 50 mV peak-to-peak signals produced the same HFCV response, and a 30 mV signal was smaller than the step voltage used, which is important when measuring large changes in capacitance with a small change in gate bias. For these reasons, all HFCV measurements in this dissertation were measured using a 30 mV peak-to-peak AC signal.

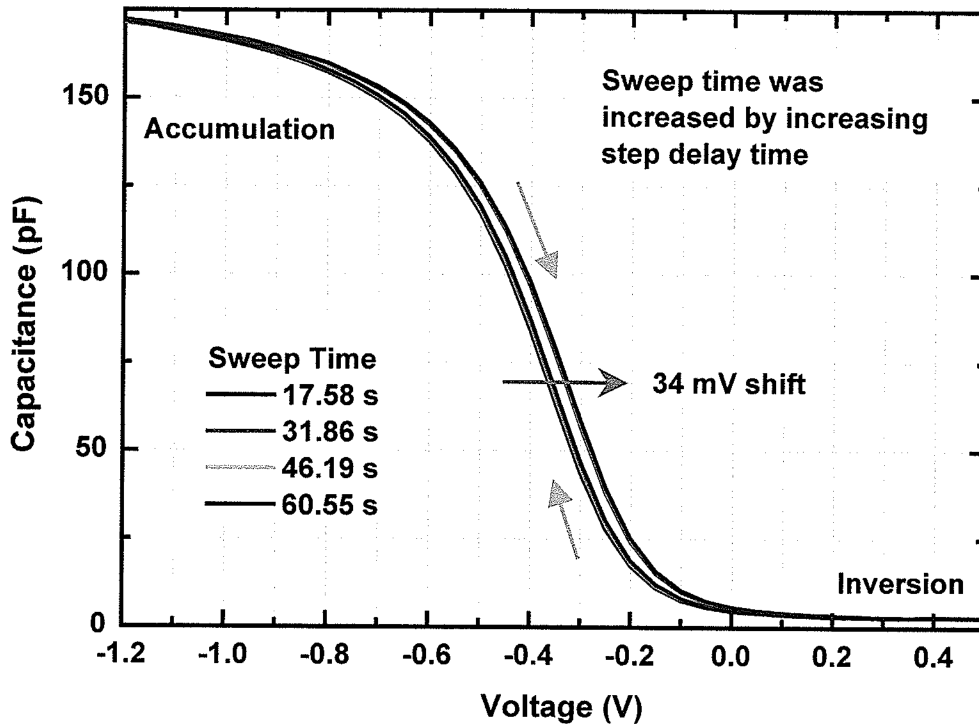


Figure 7.1: The HFCV response of a 5×10^{-4} cm^2, 50Å HfO_2 capacitor. The total measurement time was varied by adjusting the step delay time of the sweeps. A hysteresis of ~34 mV was measured for all the sweeps.

The devices, from which the measurements shown in Figure 7.1 were taken, all had a measured hysteresis which showed a shift to larger positive voltages of ~34 mV. This shift in HFCV response is very typical of these high-κ HfO_2 samples. The shift was parallel to the original HFCV response, which indicates a change in oxide trapped charge, rather than interfacial trapped charge which usually leads to a stretch-out of the CV characteristic [19]. With changes in the accumulation hold time, which was varied from 2 to 5 and then 10 seconds, the measured hysteresis became larger as shown by the inset plot of Figure 7.2. Such behaviour is indicative of negative oxide charge trapping during negative bias conditions [18].

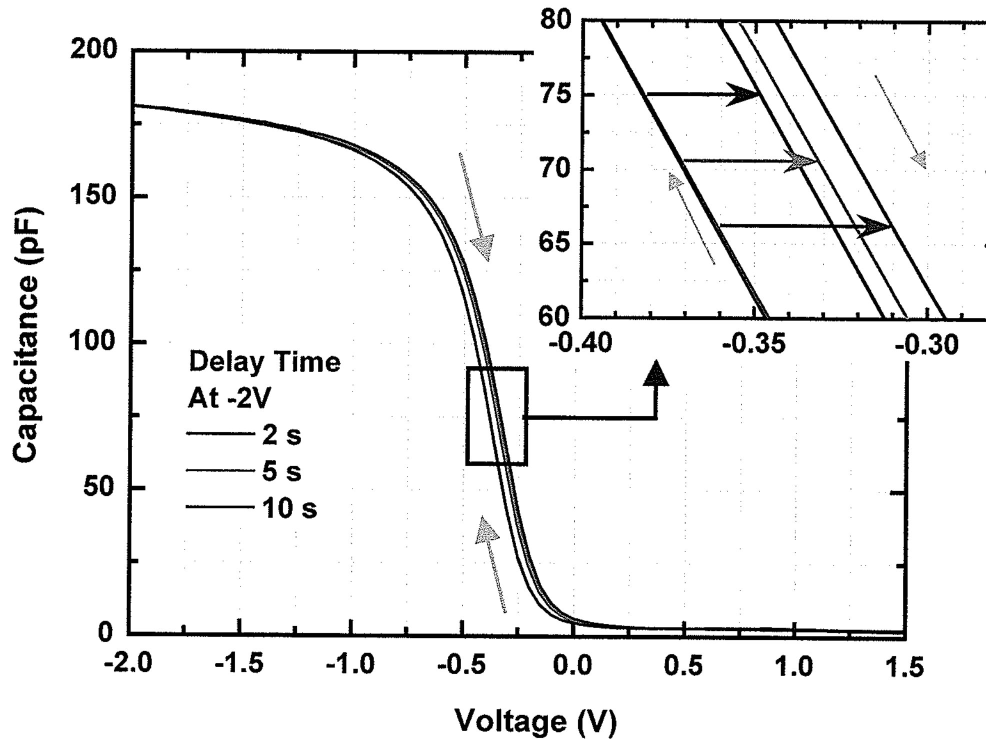


Figure 7.2: The HFCV response a 2×10^{-4} cm^2, 50Å HfO_2 capacitor using a test frequency of 100 kHz. The capacitor was swept from 1.5V to –2V and back to 1.5V. Before the device was swept back into inversion, a 2 (black line), 5 (red line), or 10 (blue line) second hold time at -2V occurred resulting in the hysteresis shown in the inset.

The HFCV measurements shown in Figure 7.2 were taken on a device where gate voltage was swept from inversion to accumulation and back into inversion, which resulted in the positive voltage shift. For HFCV measurements taken in the reverse order (i.e., from accumulation to inversion and back), the measured hysteresis was found to be negative. Examples of such shifts are shown in Figure 7.3 for HFCV measurements performed on a 2×10^{-3} cm^2 HfO_2 device. In one measurement, the black curve, the gate voltage was swept from a start bias of -1.5 V to a stop bias of 0.3 V and after a two second delay back to the start bias of -1.5V. The measured hysteresis for this sweep was -17 mV. The reverse sweep, shown in red, resulted in a 47 mV shift.

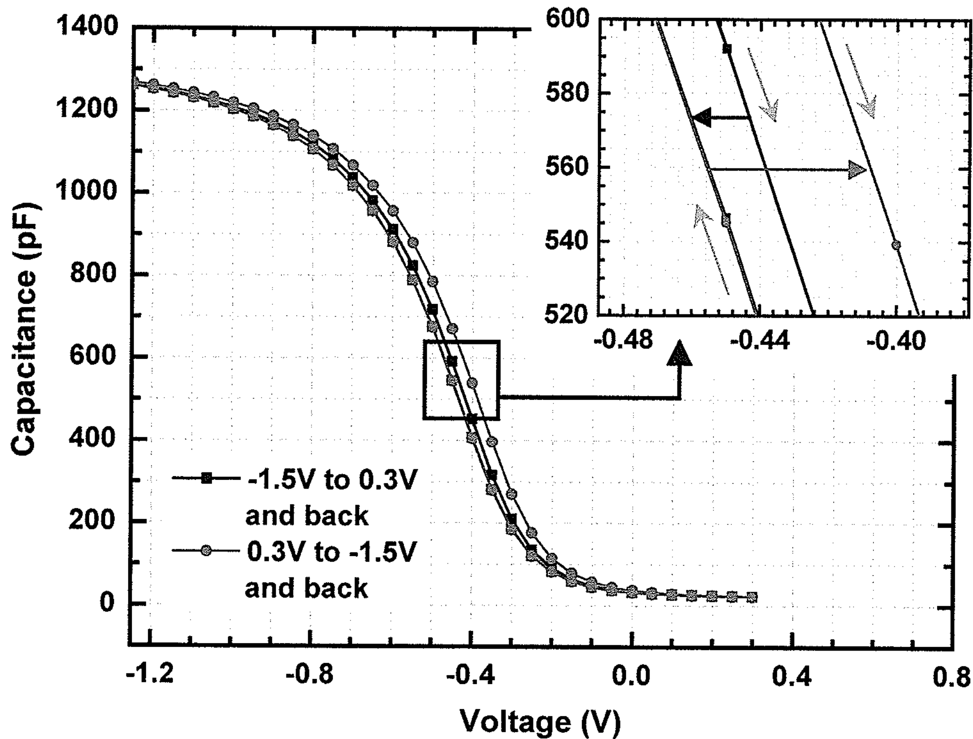


Figure 7.3: The HFCV response of a 2×10^{-3} cm^2, 90Å HfO_2 capacitor. The device was swept from a) -1.5V to 0.3V and back to -1.5V after a 2 second delay (black squares), and b) 0.3V to -1.5V and back to 0.3V after a 2 second delay (red circles). The measured hystereses shown in the inset for both curves are –17 mV and 47 mV.

The behaviour shown in Figure 7.2 and 7.3 was characteristic of all HfO_2 samples. If the stop bias was more negative (regardless whether the stop bias was in accumulation or inversion) the measured hysteresis was greater. This can be explained by an influx of net negative charge into the dielectric (i.e., more electron trapping or less detrapping of negative charge), resulting in a positive shift in the flat-band voltage. If the stop bias was more positive the measured shift was more negative, indicative of more detrapping of negative charge within the dielectric or less trapping of electrons. Due to the asymmetry (relative to the bias polarity) in the band structure of the HfO_2 devices,

(i.e., a stacked, two layer dielectric) a possible explanation for this HFCV behaviour is the presence of energetically shallow bulk defects within the hafnium dioxide layer [16, 17, 53, 54]. In theory, such defects could communicate with the metal electrode readily, which would account for the negative trapping behaviour at negative applied bias (electrons trapped by the defects), and detrapping behaviour at positive biases (detrapping of electrons). Electron trapping under positive bias conditions would not be expected since direct communication is prevented via a relatively thick (~15Å) intermediate oxide layer between the bulk HfO_2 defects and the silicon substrate.

One parameter of HFCV measurements that is very important for the extraction of capacitance values from the measured data is the choice of equivalent circuit model used. Since HFCV measurements are impedance measurements, an equivalent circuit model is necessary for determining capacitance. Typically, MOS capacitor measurements use the parallel equivalent circuit model (Figure 7.4a) that consists of the MOS capacitor in parallel with a resistance. This is typically a good fit for MOS capacitors because of the high impedance for these devices, but for leaky devices, a series resistance model may be desirable [49]. In any case, either model should result in the same measured capacitance if leakage is not a large concern.

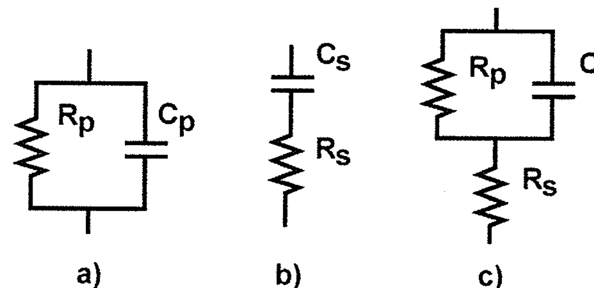


Figure 7.4: The a) parallel, b) series, and c) combined equivalent circuit models for modelling capacitor measurements.

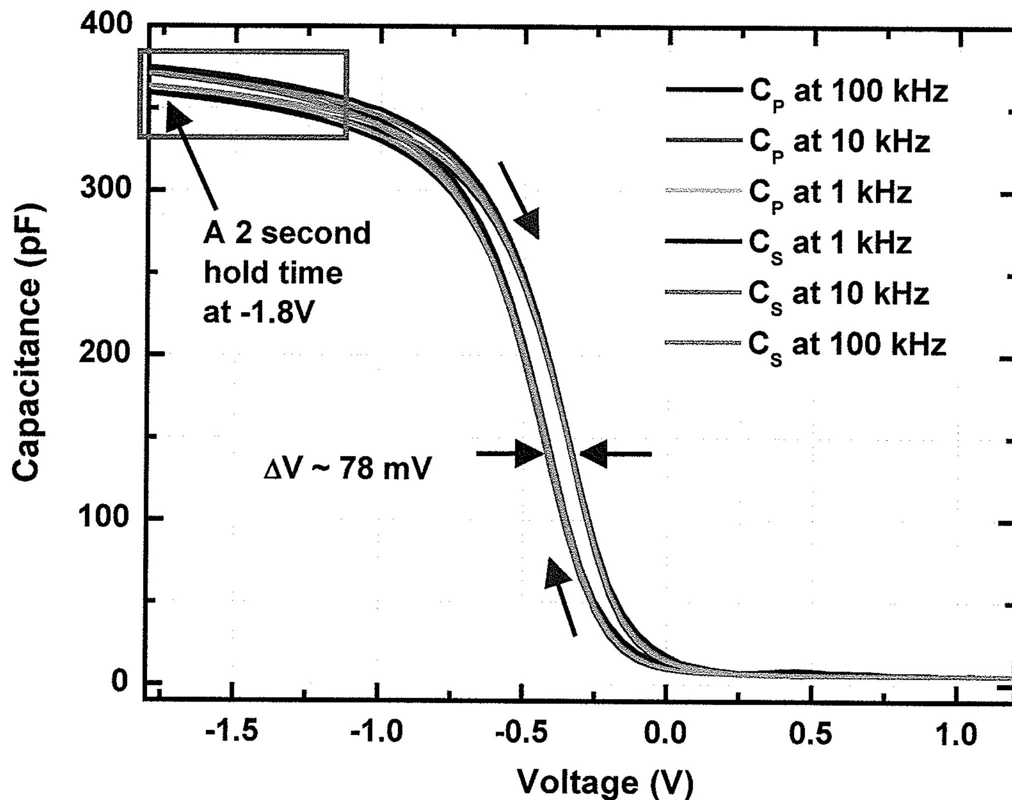


Figure 7.5: The HFCV response of a 5×10^{-4} cm^2, 90Å HfO_2 capacitor without a FGA. The AC test signal had a frequency of 1 kHz, 10 kHz, or 100 kHz, and a peak-to-peak voltage of 30 mV. Measurements were taken using the parallel and series equivalent circuit models.

The HFCV measurement of 90Å HfO_2 devices using both the parallel, C_p, and series, C_s, equivalent circuit models are shown in Figures 7.5 and 7.6. The measured responses for both models at frequencies of 1 kHz, 10 kHz, and 100 kHz are very similar in the inversion and depletion regimes of operation, as shown in Figure 7.5. All measured HFCV responses even have similar 78 mV shifts. The largest difference in response is in accumulation where measured capacitance is the largest, as shown in Figure 7.6. At the frequencies of 1 kHz and 10 kHz, both the parallel and series models

result in equivalent measured capacitance. For this reason and because measured capacitance does not decrease at larger negative biases (further into the accumulation regime), these HfO_2 devices do not suffer from leakage currents that could affect HFCV measurements.

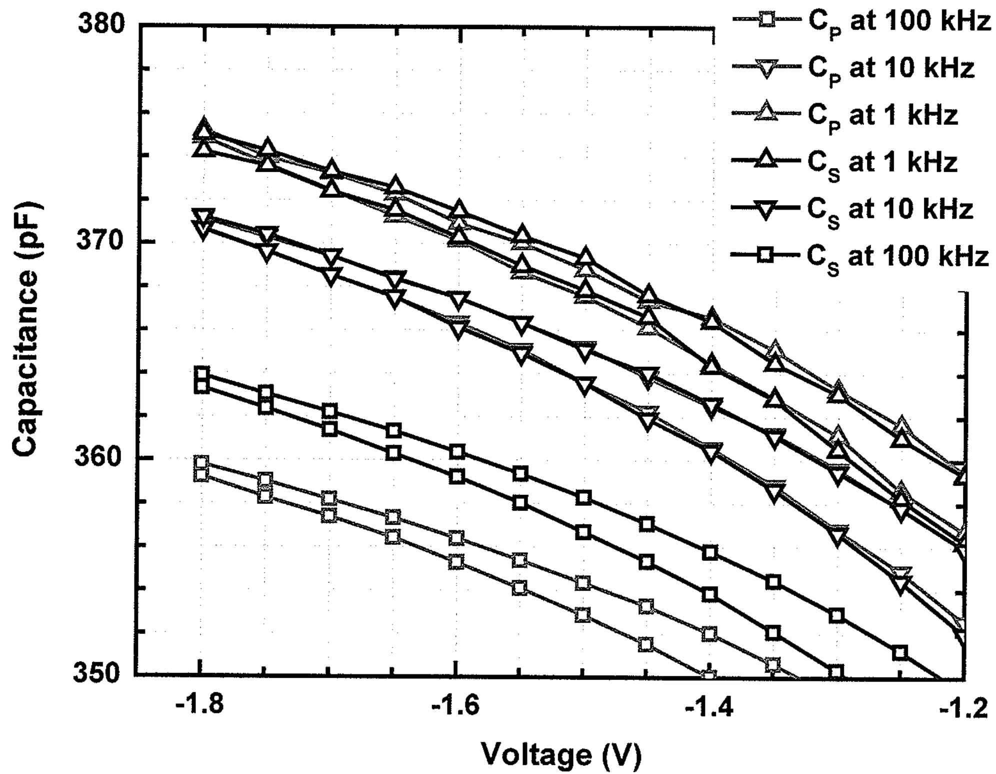


Figure 7.6: The measured capacitance in accumulation for a 5×10^{-4} cm^2, 90Å HfO_2 capacitor (the entire CV response is shown in Figure 7.5). The measured capacitance was based on the series or parallel equivalent circuit model, and test frequencies were 1 kHz, 10 kHz, and 100 kHz.

The decrease in measured oxide capacitance with increasing frequency for both the series and parallel models is explained by taking into account the impedance for the equivalent circuit models. Solving the series equivalent circuit results in a total measured impedance, Z_s, given by,

$$Z_s = \frac{1}{j 2 \pi f C_s} + R_s \tag{7.1}$$

where f is the frequency, and C_s and R_s are the MOS capacitance and series resistance terms respectively as shown in Figure 7.4b. As frequency increases, the impedance associated with the MOS capacitor is reduced and the series resistance term affects the measurement substantially. The same reasoning applies to the parallel capacitance model, but in that case the effect is greater because no series resistance is taken into account by the model. For this reason, the use of a parallel capacitance model results in a lower measured oxide capacitance in accumulation than a series model at 100 kHz as shown in Figure 7.6. The reduced measured accumulation capacitance for higher AC test frequencies for HFCV measurements using the parallel equivalent circuit model are shown in Figure 7.7. To account for this phenomenon a correction has been derived [18]. However, for the purposes of this research work, frequencies were limited to $\leq$ 100 kHz where this effect is negligible.

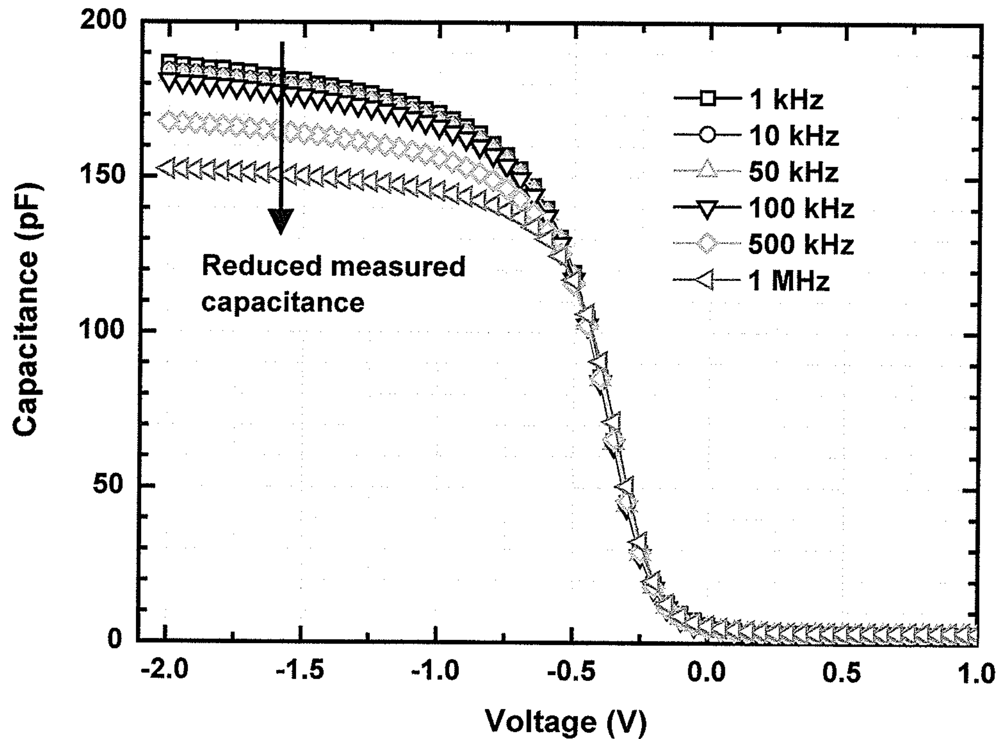


Figure 7.7: The HFCV response for a 2×10^{-4} cm^2, 50Å HfO_2 capacitor. The measurements were taken in parallel mode at frequencies ranging from 1 kHz to 1 MHz. The measured C_{ox} values decrease with measurement frequency.

The measurement of oxide capacitance for HfO_2 devices is also subject to an area dependence. The measured capacitance density for a set of capacitors with areas ranging from 2×10^{-5} to 5×10^{-3} cm^2 is shown in Figure 7.8. The capacitance density should be constant for all the capacitors, but it is not. As area increases, a reduced capacitance density was observed. In this case the measurement frequency was 100 kHz and the parallel equivalent circuit model was used. The dissipation factor, D, which was measured at the same time as the capacitance data from Figure 7.8, is shown in Figure 7.9. The dissipation factor is a measure of the device quality factor and is related to the

real, R, and imaginary, X, parts of the measured impedance of the device by the expression,

$$D = \frac{1}{2\pi f R_p C_p} = \frac{R}{X} \tag{7.2}$$

where f is the AC test frequency, and R_p and C_p are the parallel resistance and capacitance values, respectively, from the parallel equivalent circuit model. Therefore, as the dissipation value in Figure 7.9 increases, the larger devices appear more resistive than capacitive, resulting in the lower measured oxide capacitance.

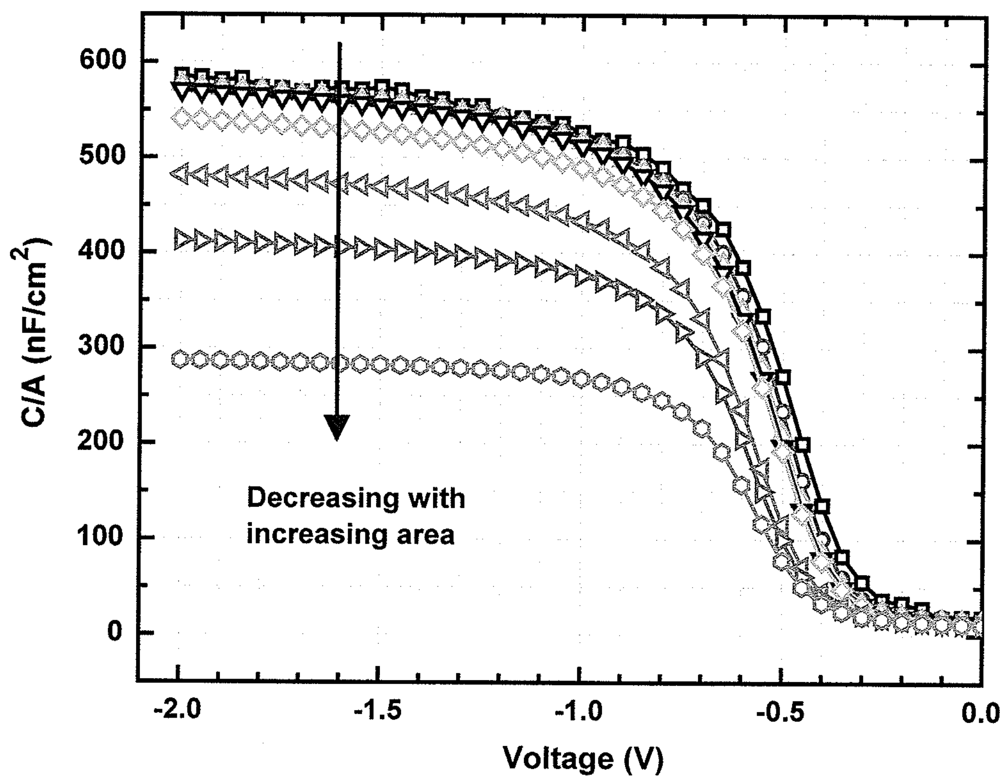


Figure 7.8: The HFCV response normalized to area for 90Å HfO_2 capacitors. The measurement was taken in parallel mode at a frequency of 100 kHz.

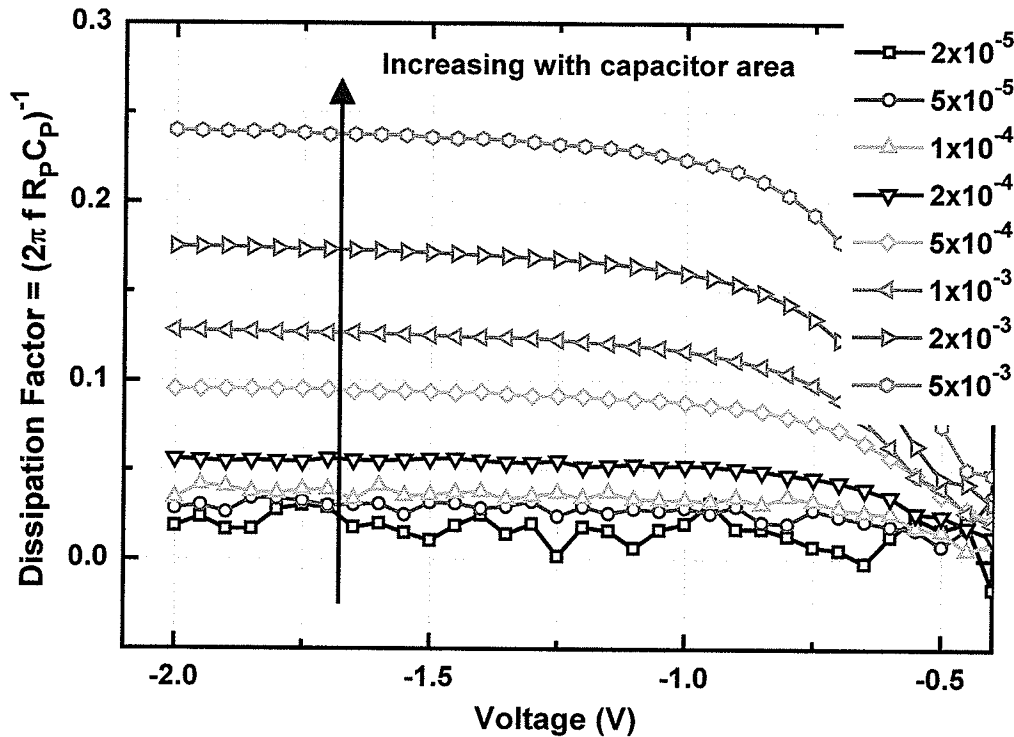


Figure 7.9: A plot of the measured dissipation factor as a function of voltage for the 90Å HfO_2 capacitors shown in Figure 7.8.

Solving equation (7.2) for the conductance, G_p, where $G_p = 1/R_p$ (the inverse of the parallel resistance) and plotting it as a function of device area results in the data shown in Figure 7.10. This plot of conductance (in accumulation), versus area results in a linear fit with a value of $4.42\times10^{-2} \pm 7\times10^{-4}$ S/cm^2. Plotting the conductance versus capacitor area for another (different) set of 90Å HfO_2 capacitors resulted in the plot shown in Figure 7.11. The second set of data was obtained using an AC test frequency of 1 kHz and a linear fit to the data resulted in a value of $1.14\times10^{-4} \pm 2\times10^{-6}$ S/cm^2. The conductance measured at the lower frequency is two orders of magnitude less. Therefore,

for testing HfO_2 devices with HFCV measurements it is preferential to use lower AC test frequencies and smaller area devices when possible.

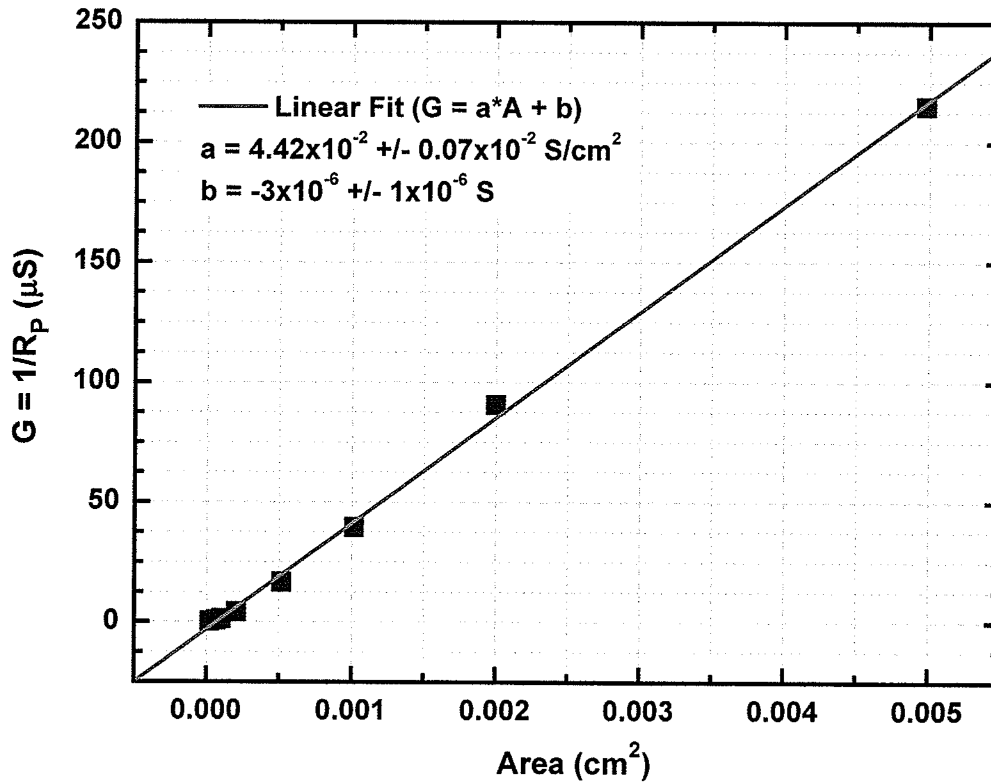


Figure 7.10: The calculated conductance as a function of device area from the 90Å HfO_2 capacitor data shown in Figures 7.8 and 7.9. The linear fit (red line) to the data is 0.04 S/cm^2.

7.1.2 The Scaling of Oxide Capacitance

In this section, the details of the HFCV measurements used for obtaining oxide capacitance values, for the various HfO_2 samples, are presented. To measure oxide capacitance, HFCV measurements were taken using a 30 mV peak-to-peak AC test signal with a frequency of 1 kHz as discussed previously.

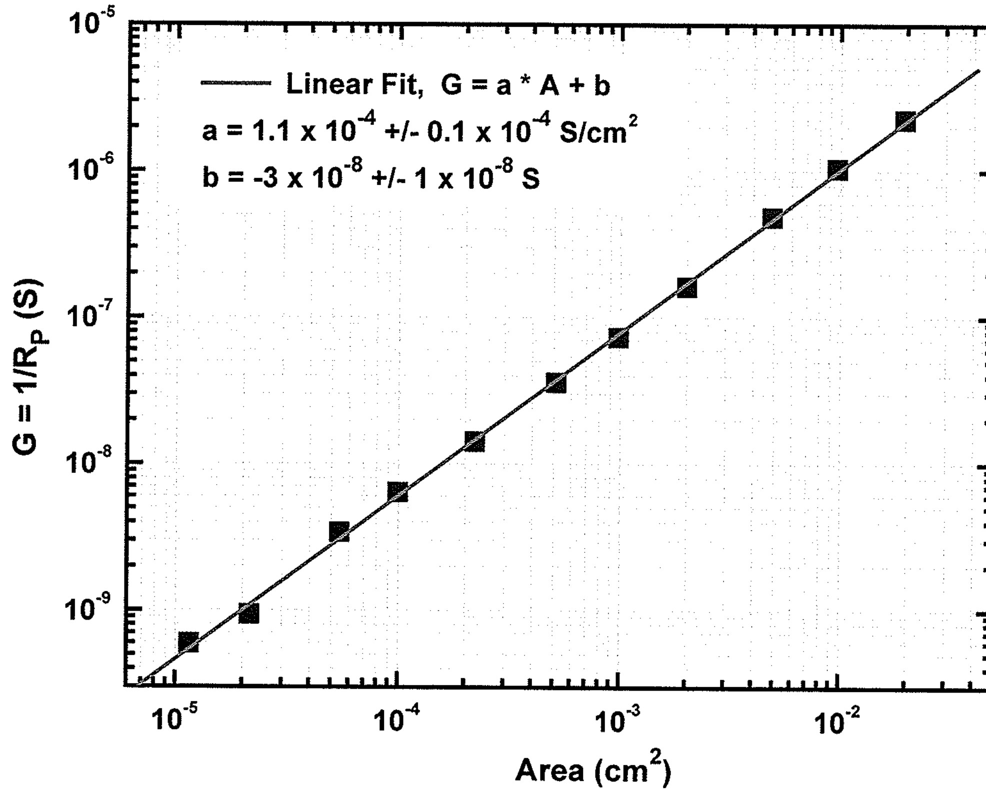


Figure 7.11: The conductance as a function of capacitor area for the 90Å HfO_2 devices shown in Figure 7.12. An AC test frequency of 1 kHz and the parallel capacitance model were used. The linear fit (red line) to the data is calculated to be 1.1×10^{-4} S/cm^2.

The HfO_2 thicknesses for the capacitors used to measure the area dependence were nominally 50Å, 90Å, 115Å, and 680Å. The linear fit to the HFCV measurement data for each of these thicknesses is shown in Figure 7.12 and listed in Table 7.1.

The accumulation capacitance for the 90Å HfO_2 devices, the capacitors most frequently discussed in this dissertation, was measured at an applied bias of –3V is 8.55×10^{-7} F/cm^2. The same capacitors were also measured at a gate voltage of –4V and produced a linear fit with the slope of 8.65×10^{-7} F/cm^2. Therefore, the 1V difference in applied bias (~1 MV/cm change in electric field averaged over both dielectrics) only

resulted in a marginal 0.1×10^{-7} F/cm^2 change in the normalized oxide capacitance. This small error (~1.2 %) associated with the change in applied field justifies the use of a linear fit for only one applied voltage. In order to reduce errors, the capacitor area was measured after device fabrication with a microscope and software measurement tools provided with the probe station (~2% error). Therefore, with some measure of certainty the error associated with obtaining oxide capacitance values (C_{ox}/A) is ~3.2%.

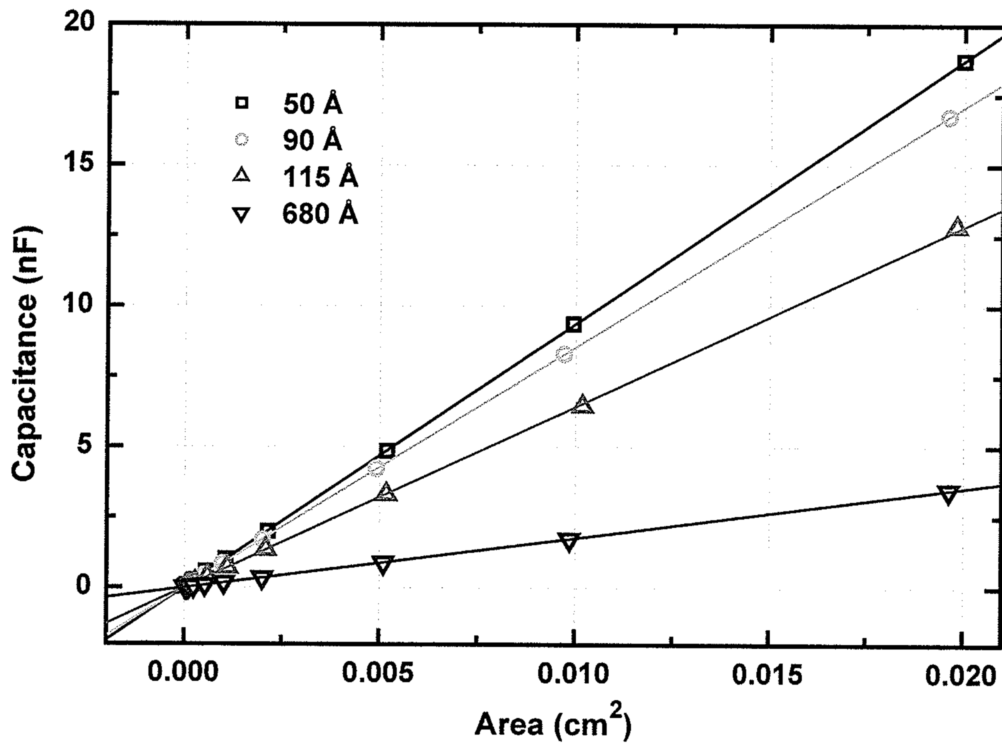


Figure 7.12: The linear C_{ox} versus area relationship for the 50Å, 90Å, 115Å, and 680Å HfO_2 capacitors.

Table 7.1: The C_{ox}/A values obtained from the linear fits shown in Figure 7.12.

Nominal HfO_2 Thickness (Å)	C_{ox}/A ($\mu F/cm^2$)	C_{ox}/A Error ($\mu F/cm^2$)
50	0.94	0.03
90	0.86	0.03
115	0.64	0.02
680	0.18	0.01

For conventional SiO_2 devices, the oxide capacitance values can be used to determine an effective, relative permittivity of the dielectric. However, the films used in this work consisted of two dielectrics in a stack, which, without physical characterization of thickness and material composition is very difficult to relate to an effective relative permittivity value for the high-κ dielectric. Fortunately, specific knowledge of the relative permittivity and thickness for each dielectric layer is not needed for the oxide charge trapping analysis presented in this work. Instead, the measured accumulation capacitance, C_{ox}/A, is used as discussed in Chapter 8.

7.1.3 Substrate Doping Concentration

The measurement of the HFCV response of MOS capacitors in inversion, $C_{HF,min}$, and in accumulation, C_{ox}, provides a method for determining a uniform substrate doping concentration, as discussed in Section 2.1. In this research, p-type silicon substrates were used and therefore the average activated "acceptor" doping concentration, N_a, was calculated. In Figure 7.13 a plot of the calculated minimum high-frequency capacitance,

$C_{HF,min}$, as a function of substrate doping concentration is plotted for a 6.5×10^{-5} cm^2, 90Å HfO_2 capacitor with a measured oxide capacitance of 46.9 pF. The theoretical minimum capacitance (blue curve) is calculated based on equation (2.8). The doping concentration is then determined by the intersection of the calculated, and the measured (0.78 pF) minimum capacitance values. In this example, the substrate doping concentration is $\sim1.0\times10^{15}$ cm^{-3}.

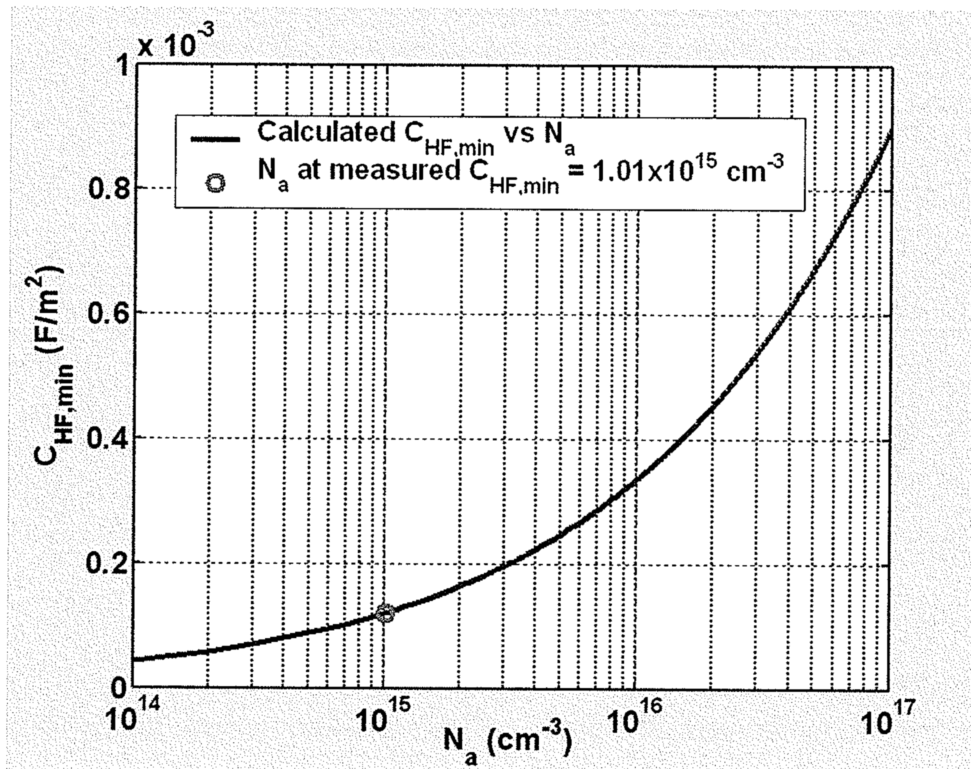


Figure 7.13: The calculated minimum high-frequency capacitance, as determined by (2.8), as a function of substrate doping concentration, N_a, for a 90Å HfO_2 device with an area of 6.5×10^{-5} cm^2, and measured C_{ox} of 46.9 pF. The substrate doping concentration corresponding to the measured capacitance of 0.78 pF is 1.01×10^{15} cm^{-3}.

Table 7.2: The measured C_{ox} and $C_{HF,min}$ values of several 90Å HfO_2 devices used to calculate substrate doping concentration, N_a, as given by Equation (2.8).

Area (10^{-8} m^2)	C_{ox} (pF)	$C_{HF,min}$ (pF)	N_a (10^{14} cm^{-3})
2205	12.9	0.38	22.8
2205	15.5	0.27	10.5
2397	16.9	0.29	10.2
5324	43.0	0.71	12.6
5616	36.2	0.65	9.3
6399	36.9	0.84	12.4
6478	46.9	0.78	10.0
10300	59.4	1.20	9.5
10300	75.5	1.24	9.9
10580	78.3	1.33	11.1
10608	66.6	1.14	7.9
10843	73.6	1.05	6.2
20154	157.0	2.48	10.6
20735	118.0	2.06	6.6
20880	150.3	2.51	10.1
22152	145.0	2.20	6.6
22156	143.0	2.60	9.6
51528	278.0	5.05	6.5
51754	374.7	6.21	10.0
54300	366.0	7.30	13.0
102000	490.0	9.12	5.3
102100	683.0	12.20	10.0
102940	706.0	11.50	8.6
104329	695.0	11.00	7.5
105000	743.4	12.56	10.0
200000	825.0	18.00	5.4
201000	1420.2	24.13	10.0
498000	1430.0	51.00	7.4
508000	3280.6	61.00	10.1

Average N_a	10×10^{14} cm^{-3}
Standard Deviation	3×10^{14} cm^{-3}

The substrate doping concentration calculated for several 90Å HfO_2 devices with varying capacitor area is shown in Table 7.2. Averaging these calculated values results in an acceptor doping concentration of $10\times10^{14} \pm 3\times10^{14}$ cm^{-3}. Data obtained for the 50Å HfO_2 capacitors is shown in Table 7.3 and results in an average doping concentration of $12\times10^{14} \pm 3\times10^{14}$ cm^{-3}, which agrees well with the previous value.

Table 7.3: The measured C_{ox} and $C_{HF,min}$ values of various 50Å HfO_2 devices used to calculate substrate doping concentration, N_a, as given by Equation (2.8).

Area (10^{-8} m^2)	C_{ox} (pF)	$C_{HF,min}$ (pF)	N_a (10^{14} cm^{-3})
2121	16.4	0.30	14.4
5210	46.5	0.81	17.7
10128	74.0	1.40	13.7
21036	145.0	2.84	13.1
53128	334.0	6.60	10.9
103000	584.0	12.50	10.4
202500	915.0	23.30	9.3
504000	1427.0	58.50	9.9

Average N_a	**1.2×10^{15} cm^{-3}**
Standard Deviation	**0.3×10^{15} cm^{-3}**

The calculated doping concentration of ~ 1×10^{15} cm^{-3} is relatively low and corresponds to a substrate resistivity of ~13 Ω-cm with boron as the dopant atom [19]. This doping concentration also enables a calculation for the Fermi level energy, E_F, in the bulk substrate by the equation

$$E_i - E_F = k_B \cdot T \cdot \ln\left(\frac{N_a}{n_i}\right) \tag{7.4}$$

where E_i is the intrinsic Fermi level for silicon (center of the silicon band-gap), k_B is Boltzmann's constant, T, is temperature, n_i is the intrinsic carrier concentration at that temperature [20]. Using the previous values for N_a, the bulk Fermi level is found to be ~0.29 eV below the intrinsic Fermi level.

A low substrate doping concentration is evident from the HFCV responses of the HfO_2 devices as demonstrated by a C_{min} value very close to zero (~1/100th of the value of C_{ox}), which results in large depletion width and subsequently a very small depletion capacitance. Intuitively, this also means that the flat-band capacitance of these devices is much smaller than the oxide capacitance because at flat-band the capacitance of a MOS device is a series combination of oxide capacitance and depletion capacitance. A calculation of flat-band capacitance, C_{FB}, can be derived from the one dimensional Poisson equation for the MOS capacitor as shown in references [19] and [20], which results in the expression

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_d} = \frac{1}{C_{ox}} + \sqrt{\frac{k_B \cdot T}{\varepsilon_{Si} \cdot \varepsilon_o \cdot q^2 \cdot N_a}} \quad (7.5)$$

where ε_{Si} is the relative permittivity of silicon (~11.9), ε_o is the free space permittivity, q is the electronic charge, N_a is the substrate doping concentration and all capacitance values are normalized to capacitor area [20]. Using equation (7.5), the flat-band capacitance normalized to C_{ox}, i.e., C_{FB}/C_{ox}, for the 90Å and 50Å HfO_2 capacitors are ~0.10 and ~0.08 respectively. As such the flat-band capacitances for these capacitors are relatively small. The use of this calculated C_{FB} value for monitoring shifts in the HFCV response due to oxide charge trapping is discussed in Section 8.1.

In conclusion, the HFCV technique has been applied to high-κ HfO_2 device characterization, has been discussed. The optimal HFCV measurement parameters for testing are an AC signal with test frequency ≤ 100 kHz and a 30 mV peak-to-peak amplitude. Also, it is desirable to test smaller area devices. Finally, values for substrate doping concentration, flat-band capacitance, and the accumulation capacitance versus area were obtained.

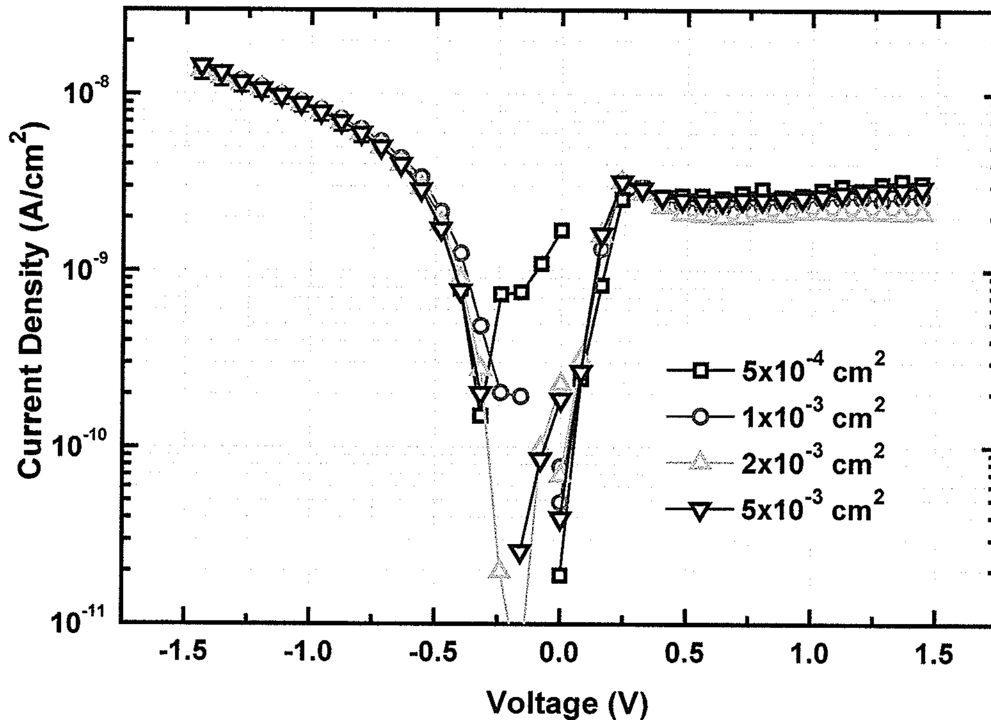


Figure 7.14: The dark IV response for 50Å HfO_2 capacitors.

7.2 Current-Voltage (IV) Characterization

The current-voltage response of a 50Å HfO_2 device is shown in Figure 7.14. In this plot the current density for a series of devices with areas of 5×10^{-4}, 1×10^{-3}, 2×10^{-3}, and 5×10^{-5} cm^2 are shown to overlap. The saturation in the measured current in the inversion regime (positive biases) is due to the lack of minority carriers being generated in the substrate. The rate at which minority carriers are being drawn out from the inversion layer (leakage current) exceeds the capacity of the silicon to generate them, so leakage current is saturated.

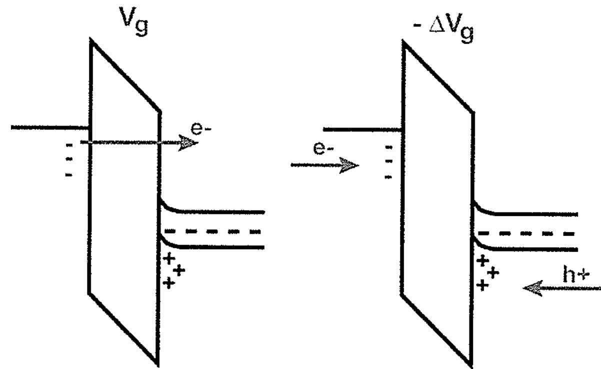


Figure 7.15: A schematic illustrating the difference between particle (diagram on the left) and displacement (diagram on the right) currents for a conventional MOS structure. The particle current shown in this example is a direct tunnelling leakage current.

The IV measurements displayed in Figure 7.14 were taken with a stepped voltage sweep (see Section 3.2.2) using a parameter analyzer. The question that requires answering is whether this measured leakage current is actually a particle current or a displacement current. A particle current, as shown in Figure 7.15, is the result of an electron, or hole, travelling from one electrode to another, either by excitation over the insulator energy barriers, through trap assisted mechanisms, or by tunnelling. A leakage

current that passes completely through a dielectric is a particle current. A displacement current on the other hand is the result of the displacement of charge to and from the electrodes of a capacitor due to a potential change across the capacitor, i.e a rearrangement of charge.

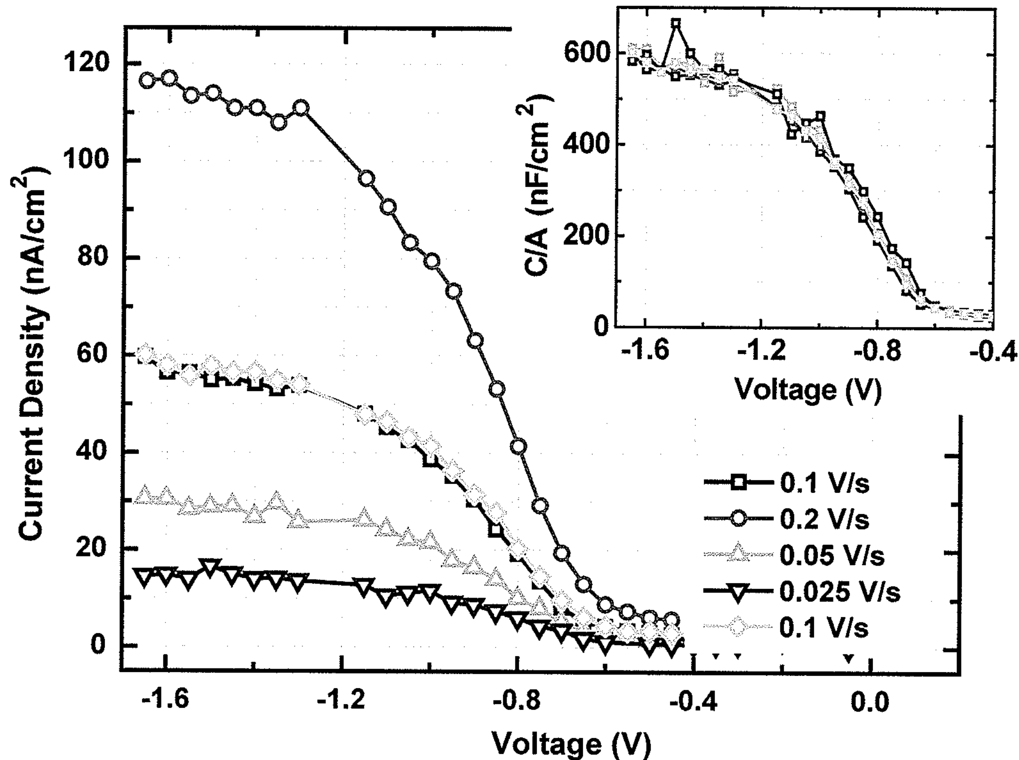


Figure 7.16: The measured displacement current in the dark of a 2×10^{-3} cm^2, 115Å HfO_2 capacitor using a ramped measurement. The four ramp rates used were 200 (red), 100 (black and cyan), 50 (green), and 25 (blue) mV/s. Shown in the inset is the capacitance value, normalized to area, of the device.

To distinguish between leakage current (particle current) and displacement current, ramped voltage sweeps are used. If a capacitor is measured with a ramped voltage sweep, the current measurement and ramp rate can be used to obtain a low

frequency capacitance value, given by equation (3.1). If the same measurement at a different ramp rate results in an equivalent capacitance, then a displacement current is being measured. A dark IV measurement using a ramped voltage sweep is shown in Figure 7.16. The IV measurement of the 2×10^{-3} cm^2, 115Å HfO_2 device at four different ramp rates (200, 100, 50, and 25 mV/s) resulted in a measurement of the low frequency capacitance using equation (3.1), which is shown in the inset of Figure 7.16. The measurement of the displacement current, rather than leakage current, is common for large area, thin dielectric, or high permittivity capacitors since oxide capacitance per unit area is large. For measurement of leakage current, either insulator quality must be low or the dielectric very thin (i.e., leaky capacitors), or the voltage ramp rate must be small. For the HfO_2 devices in this research, dark IV measurements always measure displacement current because the measurement of leakage current would require sweep rates too small for practical measurements (at least for small biases, e.g., $< \sim 4V$).

The typical dark IV response for all HfO_2 devices is similar to the measurement of the 2×10^{-5} cm^2, 90Å device shown in Figure 7.17. In this plot, the current density (current/area) is show as a function of the applied bias where the ramp rate was obtained from the displacement capacitance. At lower negative biases, $-4 < V_g < 0$, the displacement current dominates the IV measurement. This is shown by the multiple sweeps with different ramp rates resulting in the same capacitance values. Eventually, the applied bias results in large enough electric field to produce an appreciable leakage/particle current that begins to dominate the measured current. For the case of this 90Å HfO_2 device, the applied bias of -4V was large enough to result in leakage

current by Fowler-Nordheim tunnelling, which is shown schematically in the band diagram of Figure 7.18. Therefore, the increase in leakage current at ~-4V is expected since electrons in the aluminum gate electrode have a higher probability of tunnelling into the HfO_2 conduction band. As the bias was increased even further, dielectric breakdown of one of the dielectric layers occurred, resulting in the sudden spike in measured current.

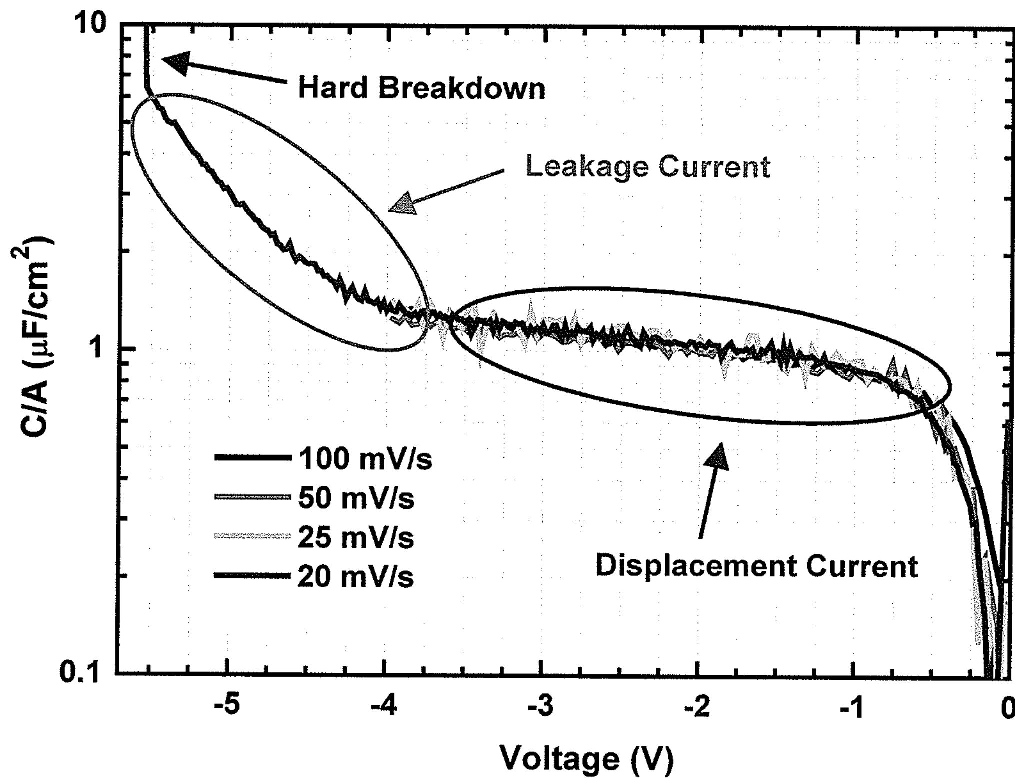


Figure 7.17: The QSCV response of a 2.2×10^{-5} cm^2 90Å HfO_2 capacitor measured in the dark at voltage ramp rates of 20, 25, 50, and 100 mV/s.

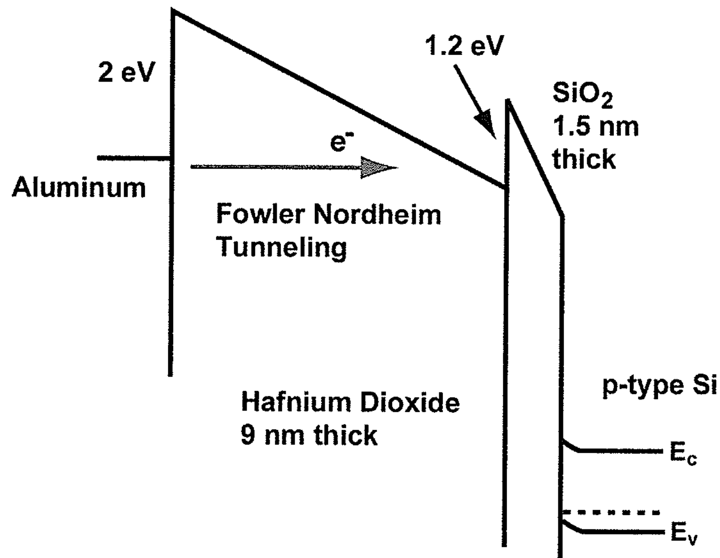


Figure 7.18: The band structure of the 90Å HfO_2 devices used in this research when a -4V bias is applied across the two dielectric layers. The figure is drawn to scale. A 2 eV aluminum barrier is assumed for the aluminum gate, and 1.2 eV conduction band offset between the dielectrics. It is also assumed that the $\varepsilon_{ox} = 3.9 \approx \varepsilon_{high\text{-}\kappa} / 4$.

In this section, only the negative bias IV measurement is shown because dark IV measurements at positive biases suffer from the lack of minority carrier generation as previously discussed. So in concluding, current measurements in the dark at positive applied biases (inversion) are small due to the saturation of current due to the lack of minority carrier generation. Under negative bias (the accumulation regime), displacement current is measured under dark conditions, due to minimal leakage current through the HfO_2 dielectric. However, under even larger negative bias conditions, leakage current becomes appreciable because of Fowler-Nordheim tunnelling.

7.3 Quasi-Static Capacitance-Voltage (QSCV) Characterization

The quasi-static capacitance-voltage (QSCV) response was briefly discussed in terms of dark IV measurements in the preceding section (7.2) and in Section 3.2.3. This measurement relies on an IV measurement of the displacement current and subsequent use of equation (3.1) to obtain the low frequency CV response. In this work, two methods for measuring QSCV responses were available, (see Section 3.2.3); the measurement of displacement current due to a ramped voltage sweep, and the measurement of the transient current resulting from a voltage step. The ramped voltage/current was performed using a 4140B HP pico-ammeter and the step voltage current was measured using a parameter analyzer. The CV responses of a 1×10^{-3} cm^2, 90Å HfO_2 device are shown in Figure 7.19. The QSCV measurements were taken using a parameter analyzer and were taken in the dark (the red circles) and with background illumination (the black squares). The difference between the HFCV and QSCV measurements is an offset in measured capacitance in the accumulation and the depletion regimes. This offset is a result of the test equipment not fully compensating for the parasitic capacitances associated with cabling and the measurement set-up. Such parasitic capacitances are effectively in parallel with the device under test if an equivalent circuit model is considered. Therefore, any measurement that does not fully compensate for these parasitic capacitances or leakage currents will suffer from a measured offset. The HFCV measurements are less susceptible to such errors because the impedance meter has open- and short-circuit corrections for parasitic capacitances and series resistances. If the measured QSCV responses, in Figure 7.19, are offset by 39 pF, the

plot in Figure 7.20 results. From this plot it is evident that both CV methods provide consistent CV responses with respect to one another once the parasitic capacitances and leakage currents are taken into account.

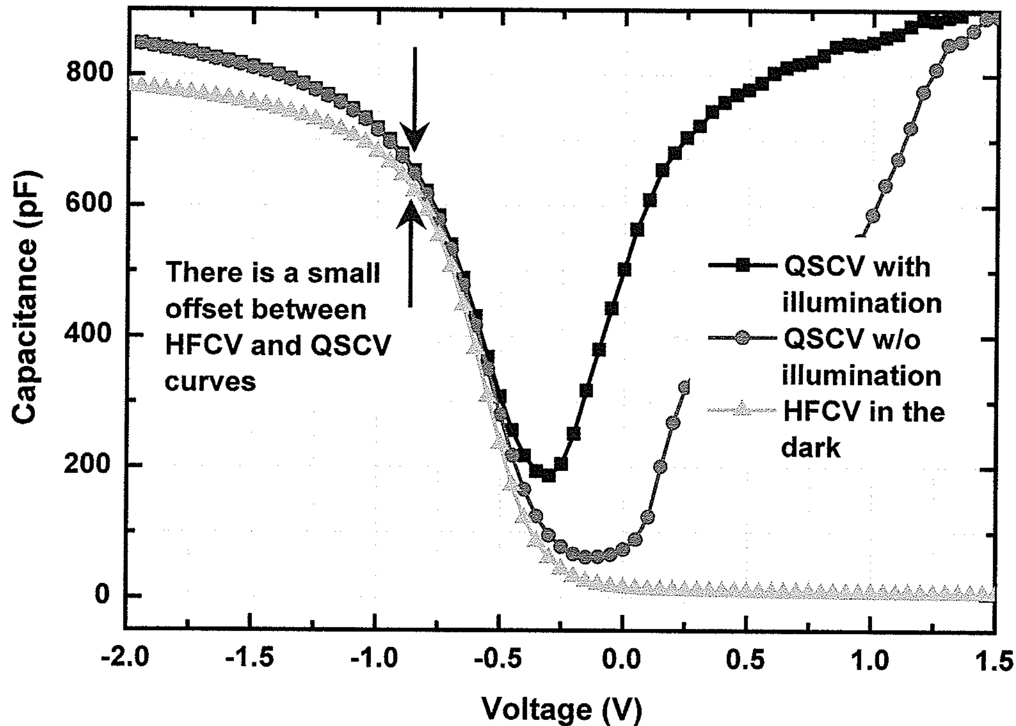


Figure 7.19: The measured QSCV and HFCV responses of a 1×10^{-3} cm^2, 90Å HfO_2 capacitor. The QSCV measurements were taken in the dark (red dots) and under illumination (black squares). The HFCV measurement (green triangles) was taken in the dark at a test frequency of 10 kHz.

The most noticeable deviation in the HFCV and QSCV responses is in the accumulation regime. In the QSCV response, there is discernible slope of the measured capacitance with increasing negative gate voltages. This slope is a function of leakage current and is discussed in more detail below.

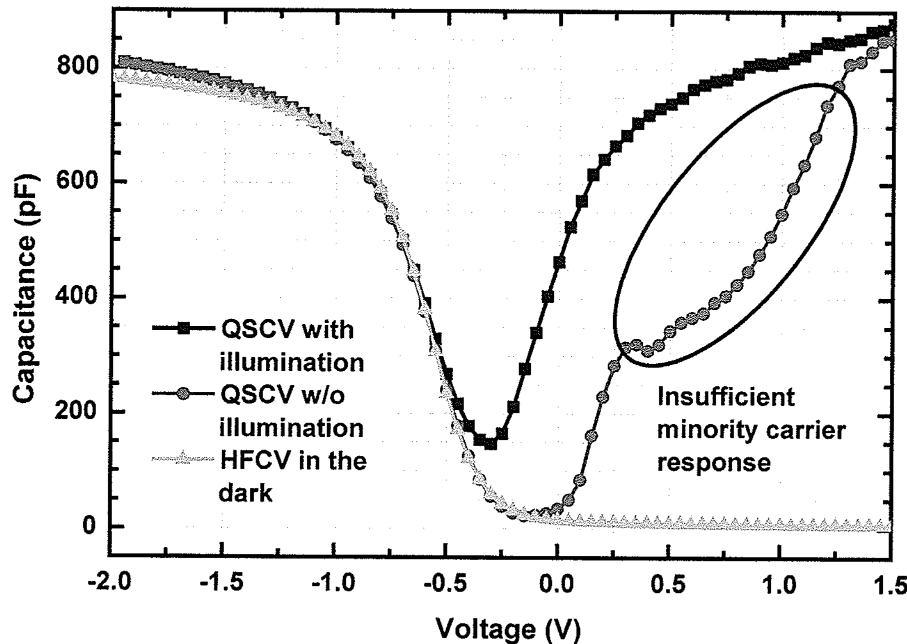


Figure 7.20: The corrected QSCV curves (the measured curves are shown in Figure 7.19) compared to the HFCV response for a 1×10^{-3} cm^2, 90Å HfO_2 capacitor. The QSCV measurements were taken in the dark (red dots) and under illumination (black squares).

The QSCV response without illumination that is shown in Figure 7.20 also has a distorted shape at applied biases greater than +0.25V (in inversion). The QSCV response under background illumination (white light), shown in Figure 7.20, appears normal and has the characteristically narrow CV response. The narrow response is due to the generation of minority carriers (electrons) in the depletion regime, where carriers are typically not generated in the dark with such abundance. One possible explanation for the distorted response is that the minority carrier generation and recombination time is inadequate for the parameter analyzer measurement, which relies on stepped voltage sweeps. The QSCV response for a 90Å HfO_2 device without any illumination, even during the hold time before the sweep, is shown in Figure 7.21. Comparing Figure 7.20

to 7.21 confirms that minority carrier response is the likely reason for the distorted QSCV response under positive bias, dark conditions.

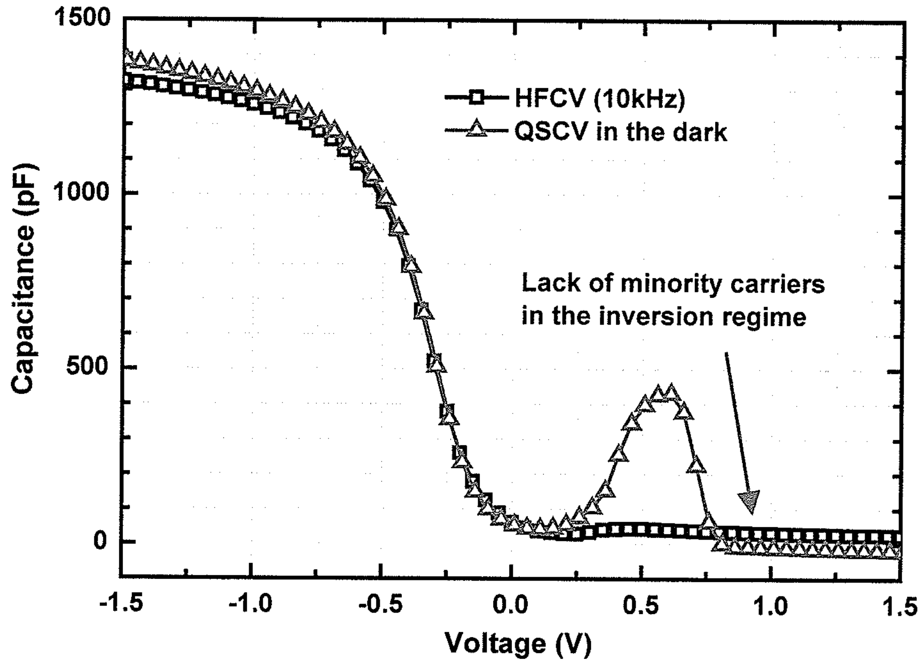


Figure 7.21: The measured HFCV and QSCV responses for a 2×10^{-3} cm^2 90Å HfO_2 capacitor. The HFCV measurement (black squares), taken at a test frequency of 10 kHz, and the QSCV measurement (red circles) were taken in the dark.

With the use of a parameter analyzer to obtain the QSCV response of the high-κ devices, and the resulting distorted data under positive biases, the accuracy of the extracted interface state densities may be limited (Section 2.4). Therefore, QSCV measurements were also made using a ramped voltage sweep to check and confirm results taken with the stepped voltage technique using the parameter analyzer. A comparison of these two methods is shown in Figure 7.22. These measurements were taken on a 1×10^{-3} cm^2, 90Å HfO_2 device. The ramped voltage measurement is compared

with compensated and uncompensated measurements from the parameter analyzer. The parameter analyzer allows for compensation of a (non-displacement) leakage current which, when turned off, results in a QSCV response very similar to the ramped voltage measurement. These observations suggest that ramped voltage measurements are consistent with the parameter analyzer measurements and with the appropriate compensation of parasitic leakage currents accurate interface state density information may be acquired. The difference between the various measurements shown in Figure 7.22 also confirms that a leakage current is the cause for the difference between the high frequency and quasi-static CVs in accumulation, as shown in Figure 7.19.

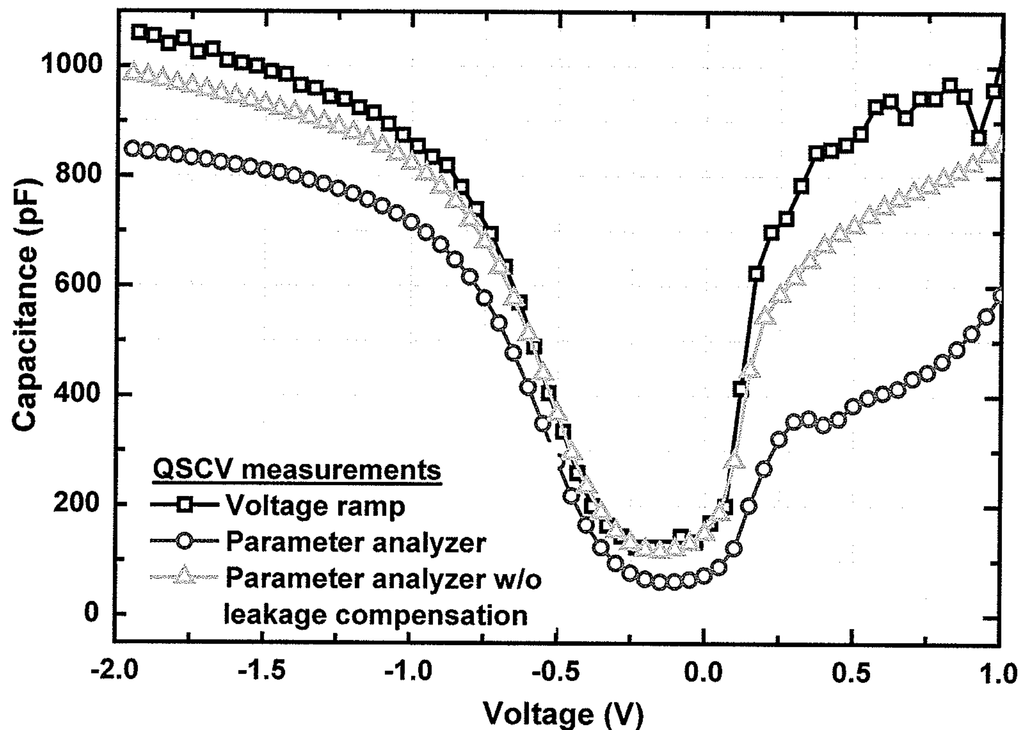


Figure 7.22: A comparison between QSCV measurements taken with the parameter analyzer and those taken with a ramped voltage measurement for a 1×10^{-3} cm^2 90Å HfO_2 device.

Chapter 8 Charge Injection Results

In this chapter the results of charge injection measurements are presented. Both qualitative analysis of the oxide charge trapping behaviour and quantitative analysis of the location and number of defects within high-κ HfO_2 MOS capacitors are discussed. The techniques used to monitor the oxide charge are the measured voltage shifts in the high-frequency capacitance-voltage (HFCV) and photocurrent-voltage (photo IV) curves. Initially, the application of each technique for the characterization of the high-κ devices used in this research is discussed. Following the introduction of these techniques, both gate electron and substrate electron injection are discussed in detail. This chapter is concluded with a discussion of the main results from this charge injection study.

8.1 High-Frequency Capacitance-Voltage (HFCV) Shifts

A commonly used technique for investigating oxide charge trapping in MOS dielectrics is the HFCV technique [11, 40, 50, 51, 52]. As discussed in Section 2.5.1, the shift in HFCV response is a direct indicator of oxide charge trapping. A typical HFCV shift for the HfO_2 devices is shown in Figure 8.1. In this figure, the HFCV response of a fresh device (i.e., not previously electrically stressed) is shown between two other HFCV measurements that demonstrate the trapping and detrapping nature of these films. With the application of a small positive bias, 1V for an extended period of time (at least several minutes) to the fresh device resulted in a shift in the HFCV curve to lower voltages (to the left in Figure 8.1). In this dissertation this is referred to as the "detrapped" state for

the device because it is assumed that electron trapping and detrapping were the cause for the change in oxide trapped charge. Therefore, the negative shift in HFCV response due to a 1V applied bias corresponds to a detrapping of electrons from defects within the oxide. Similarly, a positive shift corresponds to electron trapping.

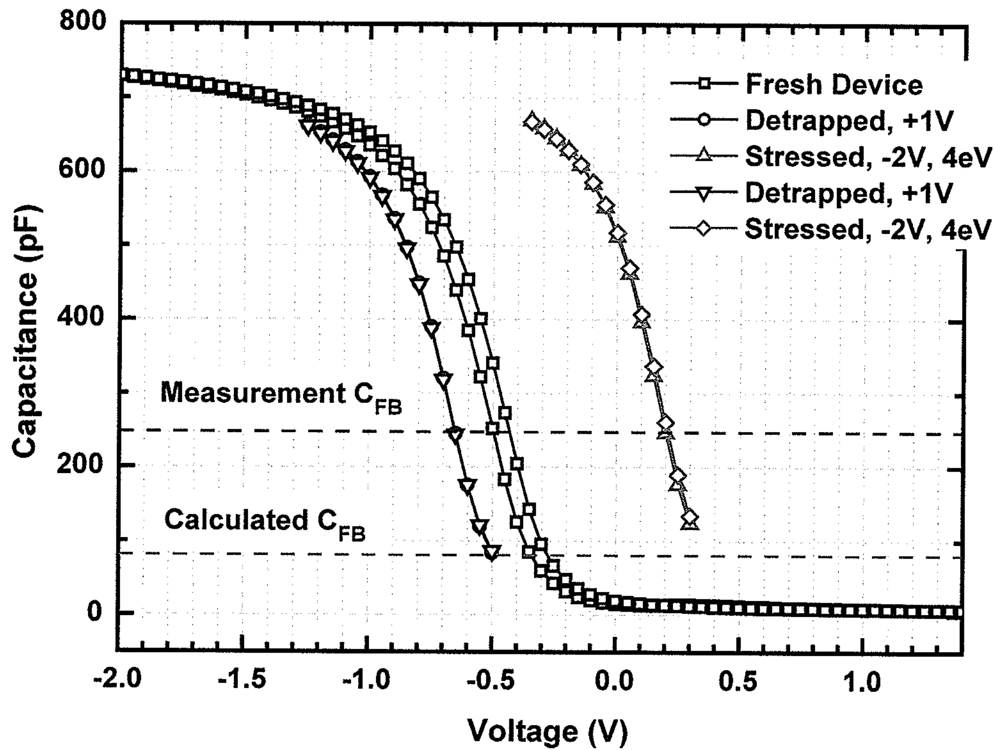


Figure 8.1: The HFCV response of a 1×10^{-3} cm^2, 90Å HfO_2 device. The HFCV response of a fresh device (black squares) is shifted positively versus the detrapped (after 1V applied stress in the dark) HFCV response, and negatively with respect to the stressed device (2V stress under 3.4 eV illumination).

The choice of a small positive applied bias for detrapping is appropriate when considering the MOS band structure, the dark IV tests discussed in the previous chapter, and the published literature on high-κ HfO_2 defects. It is commonly theorized in the

published literature that bulk defects in HfO_2 are energetically shallow traps (defects with an energy state between the Fermi level of aluminum and the conduction band of HfO_2) [16, 17, 53, 54]. If that were the case, a small positive bias would be most effective at detrapping these defects because such defects would readily communicate with the gate, as shown in Figure 8.2. The limited number of minority carriers (assuming the detrapping stress is done in the dark) in inversion (for these p-type substrates) also prevents further trapping of charge due to the limitation on the source of electrons for injection from the substrate. In Figure 8.2 it is shown that the gate communicates with the bulk HfO_2 defects by tunnelling.

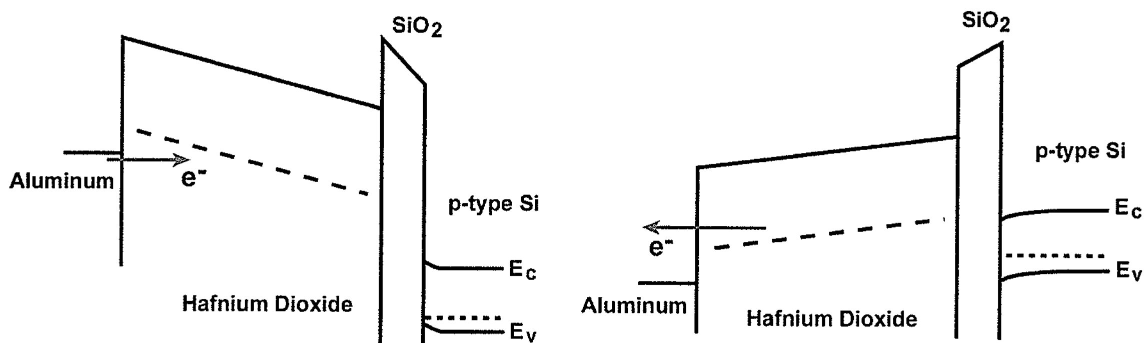


Figure 8.2: The trapping (left) and detrapping (right) of defects in the bulk HfO_2 layer.

Once charge was injected into the oxide during the "stress" pulse, shown schematically in Figure 3.9, the HFCV response shifted to higher voltages (towards the right in Figure 8.1) indicating the presence of trapped "net" negative charge. In order to inject greater quantities of charge into the dielectric during the stress pulse, in this case electrons into the HfO_2 conduction band, photoinjection was used. Illumination was used

for all charge injection tests within this research work to enhance the small dark, leakage currents of these devices (see Section 8.1), except for the electron detrapping pulses at small positive bias. It is important to inject a significant number of electrons into the oxide because trapping kinetics dictate that oxide charge trapping is exponentially dependent on electron fluence (the quantity of charge injected per unit area) [38]. The benefit of using a HFCV measurement to monitor oxide charging between stress pulses is that this technique is typically faster and less likely to perturb charge than a similar photocurrent measurement.

As mentioned previously, the flat-band capacitance normalized to oxide capacitance (i.e., C_{FB}/C_{ox}) for 90Å HfO_2 devices is very small and found to be ~0.1 (Section 7.1.3) shown by the red dashed line in Figure 8.1. The calculated flat-band voltage is dependent on the work function difference between aluminum and the p-type silicon substrate, which is calculated from the work function of aluminum (4.1 eV), electron affinity of silicon (4.05 eV), the band-gap of silicon (1.1 eV) and the Fermi level of the p-type silicon substrate (the valence band energy, E_v, plus ~0.3 eV). (These values were obtained from the band diagram shown in Section 4.2 and Section 7.1). Therefore, the flat-band voltage for these devices should be ~-0.75V. The detrapped V_{FB}, as determined from the intersection of the C_{FB} value with the HFCV response in Figure 8.1, yields a value of ~0.5V. These two values can be approximated as being within experimental error as a) there may be negatively trapped charge within the high-κ capacitor that is difficult to detrap (i.e., energetically deep traps), and b) the work function difference calculation is only an approximation (i.e., work function values for

aluminum are also given as high as 4.25 eV depending on the source of reference [18, 19]).

For ease of discussion, the HFCV response and the shift in HFCV response are commonly referred to the as the flat-band voltage, V_{FB}, and flat-band voltage shift. However, in reality, to monitor the shift in the HFCV curve, a value other than the actual flat band capacitance was used. As such, a value different form the actual V_{FB} was extracted. However, since the shifts are, for the most part, parallel, this is not only appropriate, but makes the measurements easier due the monitoring of a more linear portion of the curve. Therefore, the values referred to as flat-band voltages in this chapter were actually measured at capacitances larger than the calculated flat-band, as illustrated by the blue dashed line in Figure 8.1. This was necessary for measurement purposes because a) it allowed for a more robust algorithm for automated tests since a large change in capacitance per unit voltage is easier to track when shifted, b) it reduced the measurement time in between stress pulses since less measurement points were required and c) interface states were more readily detected since stretch-out in the HFCV response [19] is easier to detect when capacitance change per unit voltage is greatest. Fortunately, trapped oxide charge shifts the HFCV response in a parallel fashion so the actual capacitance used to measure relative voltage shifts can be somewhat arbitrary. However, comparisons of V_{FB} shifts between two or more capacitors required that identical capacitance/area values were used (when not using the actual C_{FB}) as a common reference point.

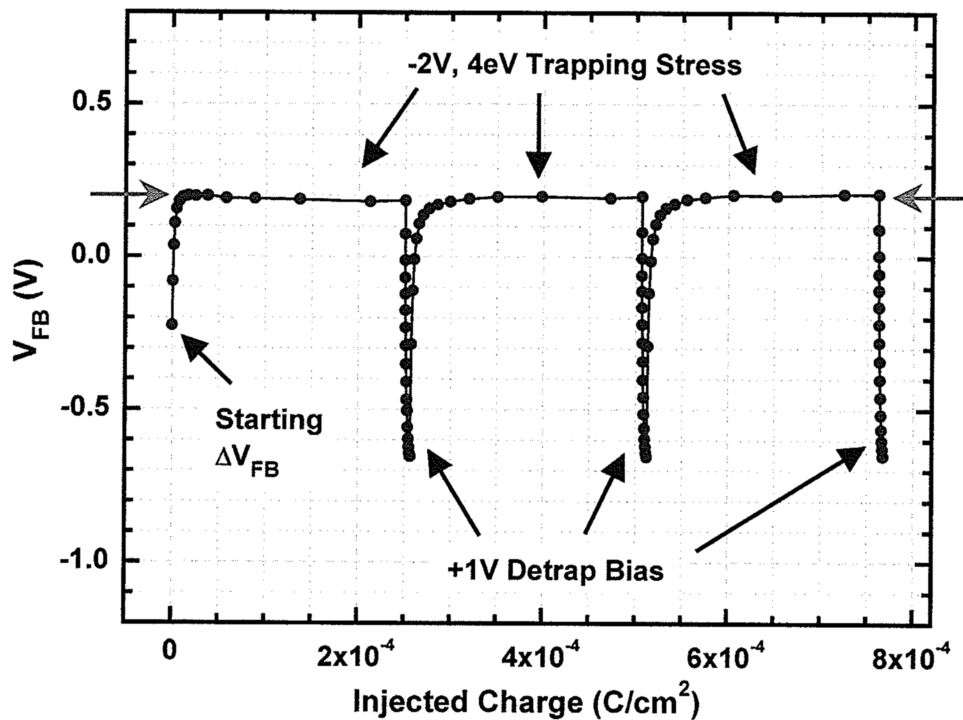


Figure 8.3: The V_{FB} versus injected charge response of a 1×10^{-3} cm^2, 90Å HfO_2 capacitor when subjected to three -2V, 4 eV stresses. After each stress, a +1V detrapping bias was applied until a V_{FB} of ~-0.65V was reached. The saturation V_{FB} measured for each of the stress pulses is ~0.2V.

The typical HFCV response of an HfO_2 device when subjected to stressing and detrapping conditions is shown in Figure 8.3, where V_{FB} is plotted as a function injected charge per unit area. In this figure, the V_{FB} was measured as a 90Å HfO_2 capacitor, and was continually stressed at a voltage of –2V under illumination of 4 eV, and detrapped at +1V. One observation to note in Figure 8.3 is that the detrapping portions of the curve only inject a small amount of charge into the film as expected from the discussion above, and the –2V stresses injected much more charge through the use of photoinjection. Since photoinjection was used for stressing devices, it is expected that the current measured

(during stressing pulses) as a function of stress time will decrease because of the increase in effective barrier height and zero field point distance due to the increase in oxide trapped charge, as discussed in Section 2.5.2. This effect is shown in Figure 8.4 where measured stress current (photocurrent) is plotted for eight stress pulses. With each successive stress pulse, the measured current decreases which is consistent with oxide charging.

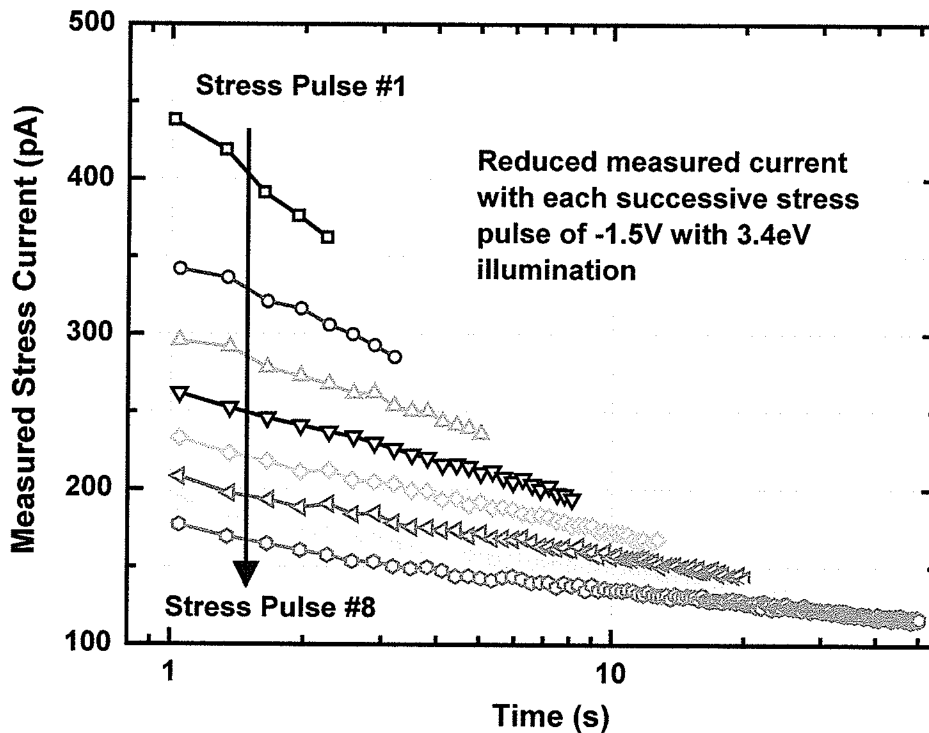


Figure 8.4: The reduction in measured photocurrent during as a function of time during each successive stress pulse. This 1×10^{-3} cm^2, 90Å HfO_2 capacitor was stressed at applied bias of -1.5V and under 3.4 eV illumination.

The most important characteristic of the V_{FB} response shown in Figure 8.3 is the reproducibility of the measurement. The ΔV_{FB} is related to an effective density of traps, N_{eff}, within the oxide by equation (2.36). Therefore, the consistent saturation of V_{FB} at a

value ~0.2V is evidence that trap creation is not occurring within these films, i.e., only existing defects are trapping electrons. Further evidence of this is given in Figure 8.5 where V_{FB} is plotted versus injected charge, but the injected charge axis is logarithmic. From this figure, it is clear that the trapping and detrapping rates are consistent with each stress condition applied. The trapping stress that deviated from the others is the initial stress applied to the fresh device (the black squares). In that case, the V_{FB} saturated earlier (less injected charge needed) because of the initial charged state of the dielectric prior to stressing.

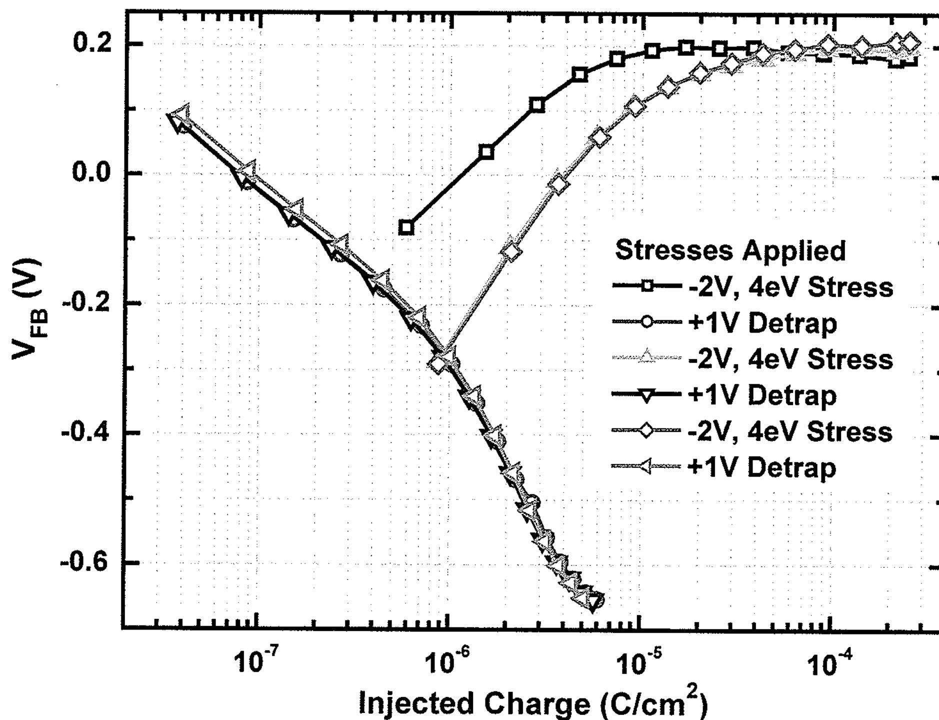


Figure 8.5: The measured V_{FB} versus injected charge for the trapping and detrapping stress pulses shown in Figure 8.3.

Whereas the data in Figure 8.5 has shown that a single device was consistently trapped and detrapped, the ΔV_{FB} shown in Figure 8.6 provides evidence that the trapping and detrapping behaviour is also consistent between different devices. In this case, three capacitors with different areas (2×10^{-4}, 5×10^{-4}, and 1×10^{-3} cm^2) were stressed at –1V and/or –2V, and under 3.4 eV illumination. The trapping behaviour for all three devices was consistent with one another. The stress voltage dependence of the saturation ΔV_{FB} is discussed in Sections 8.4 and 8.5.

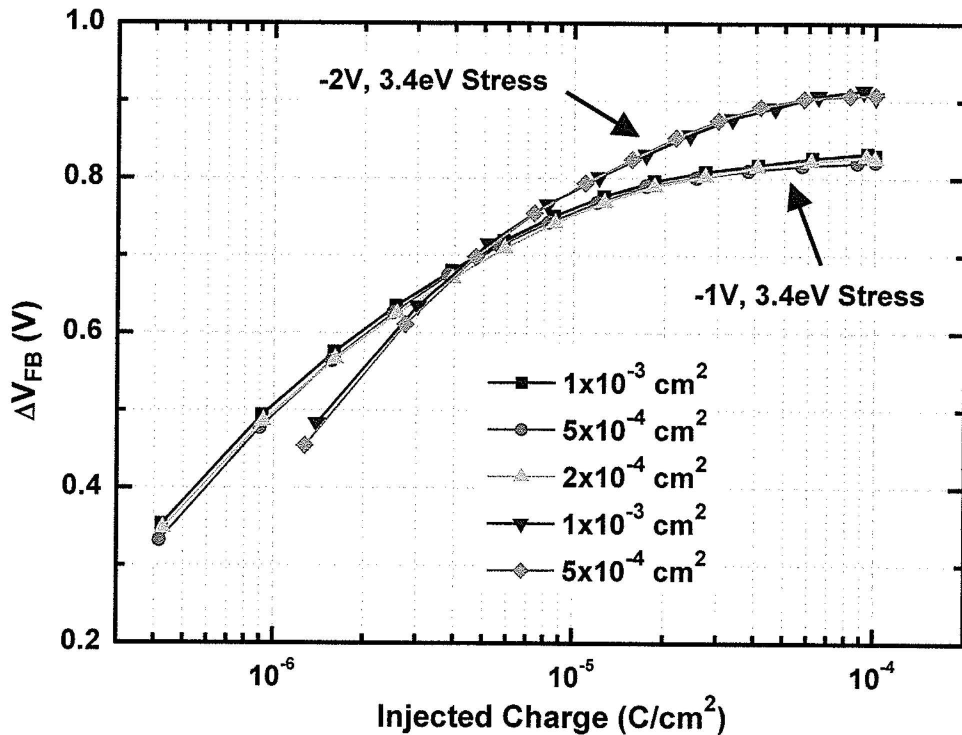


Figure 8.6: The measured ΔV_{FB} as a function of injected charge for 90Å HfO_2 capacitors. The devices measured had areas of 1×10^{-3}, 5×10^{-4}, and 2×10^{-4} cm^2. These devices were stressed at -1V and/or -2V, with a 3.4 eV illumination.

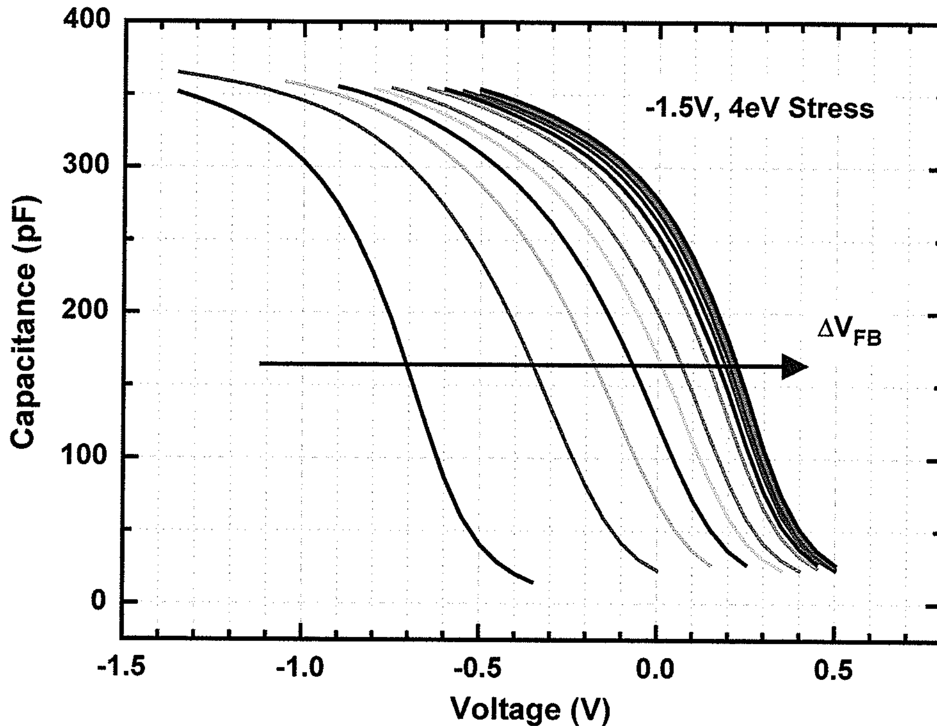


Figure 8.7: The HFCV response of a 5×10^{-4} cm^2, 90Å HfO_2 capacitor as it is being stressed at -1.5V with a 4 eV illumination. The HFCV curves shift to higher voltages. This stress measurement was preceded by a +1V stress in the dark for detrapping purposes.

The measurement of V_{FB} is taken between stress pulses using the HFCV technique mentioned previously. The visual confirmation that the HFCV response is actually shifting in a parallel manner is shown in Figure 8.7. In this figure, the HFCV responses for a 90Å HfO_2 device stressed at –1.5V with 4 eV illumination are shown. From these curves it is evident that the initial and final HFCV responses due to the stress are indeed shifted parallel to one another. However, several of the HFCV responses taken early on in the stress, primarily the second curve shown in Figure 8.7, do have a small change in maximum slope as compared to the initial and final curves. This is an artifact of the HFCV measurement rather than an indicator of interface states because the

final HFCV curve showed no indication of interface traps nor did the quasi-static capacitance-voltage (QSCV) measurements, taken directly after such stresses, show any indication of increased density of interface states.

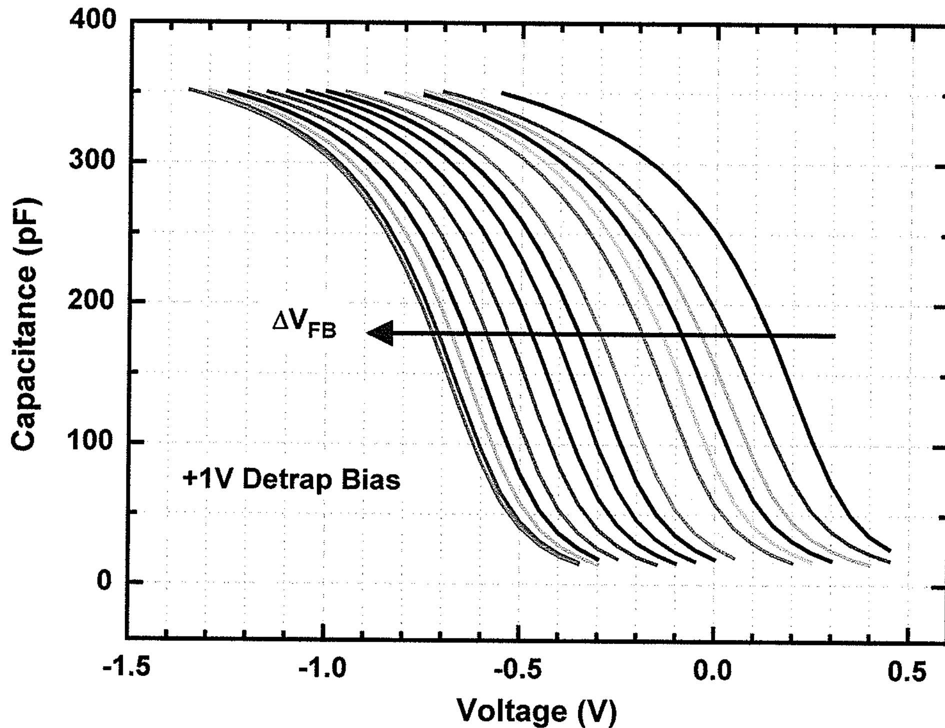


Figure 8.8: The HFCV response of a 5×10^{-4} cm^2, 90Å HfO_2 capacitor as a +1V bias is applied in the dark. The HFCV curves shift to lower voltages. The +1V bias was applied after the device was stressed at -1V with a 4 eV illumination.

A possible explanation for non-parallel shifts is that since the second HFCV measurement corresponded to a change in voltage sweep direction (for V_{FB} tracking purposes), the applied bias prior to sweeping will have changed from a "detrapping" voltage (positive with respect to the V_{FB}) to a "trapping" voltage (negative with respect to the V_{FB}). This coupled with the fact that more measurement points were required to

obtain the V_{FB} (i.e., longer period of time with the “trapping” polarity applied) may result in the observed effect. A similar change in slope can be shown for one of the final HFCV measurements (i.e., one that is parallel to the 1st measurement) if more capacitance measurements are taken at the “trapping” polarity. A similar observation was made for the case of detrapping stress pulses, as shown in Figure 8.8, where the stress bias was +1V. The previous explanation also holds true for this observation as long as polarities are reversed. The overall effect that these shifts had on charge injection measurements was minimal because it only occured for the first few stress pulses.

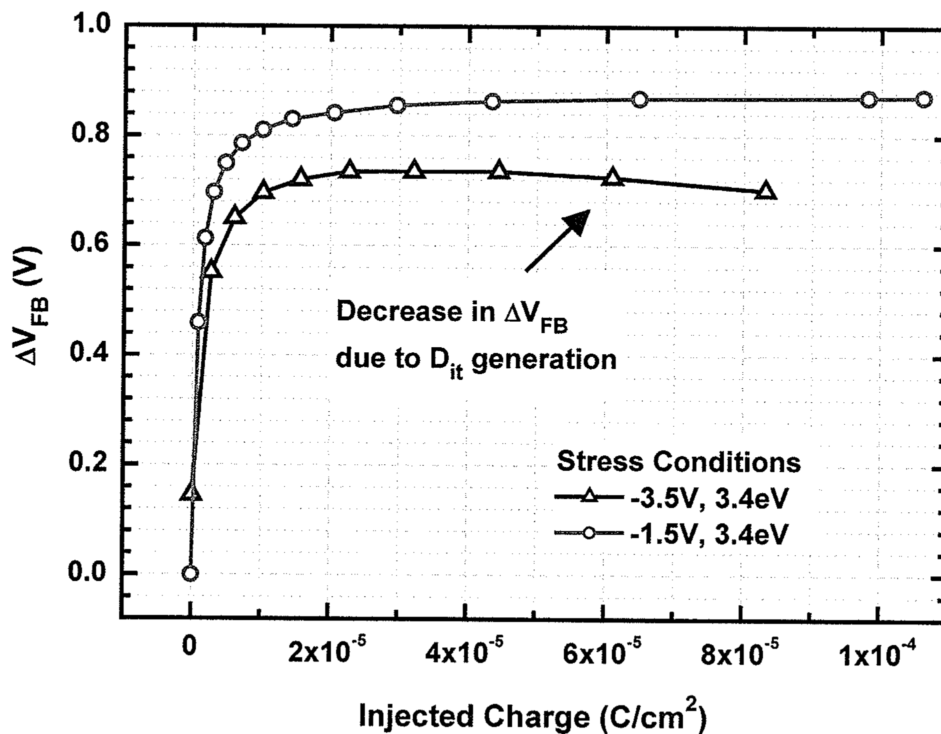


Figure 8.9: The measured ΔV_{FB} as a function of injected charge. The device tested was a 1×10^{-3} cm^2, 90Å HfO_2 capacitor. First, a -1.5V, 3.4 eV stress (red circles) was applied, then a -3.5V, 3.4 eV stress (blue triangles) after detrapping.

In the previous results, the measured V_{FB} saturated at a particular injected charge level and remained at that saturated level as all the trapped become filled, or at least a steady state condition is met (see Sections 8.3 and 8.4). This trapping behaviour is consistent at low applied biases (≤ -2.5V) as shown in Figure 8.9 for a stress condition of –1.5V (the red circles). However, at larger biases (> 2.5V), the measured V_{FB} voltage no longer remained at a saturated level. Instead, the voltage shift decreased with further injected charge. This behaviour may be explained by the generation of interface states. At these biases, as the density of interface states increases, the amount of CV "stretch-out" increases, which in turn reduces the measured ΔV_{FB}. Evidence of interface state generation for the –3.5V stress shown in Figure 8.9 is shown in Figure 8.10. In this figure, both the HFCV and QSCV responses, before and after (the -3.5V stress) were measured. The measured responses have been shifted on the voltage axis for the sake of clarity. After stressing, the HFCV response had a considerable CV stretch-out, and subsequently the QSCV response clearly shows an increase in interface state density. The calculation of interface state density (see Section 2.4) resulted in an approximate increase in interface state density from $\sim 1\times10^{11}$ to 7×10^{11} $cm^{-2}eV^{-1}$. The field dependence for the formation of interface states seen in this work is consistent with the published literature on the topic, which generally attributes the generation of interface states at the SiO_2/Si interface to the existence of "hot" electrons (electrons with high kinetic energy relative to the conduction band resulting from acceleration by the high electric fields applied) [33]. For the purposes of this work, applied biases were limited to value below –2.5V, for negative bias stress, to prevent such interface state generation.

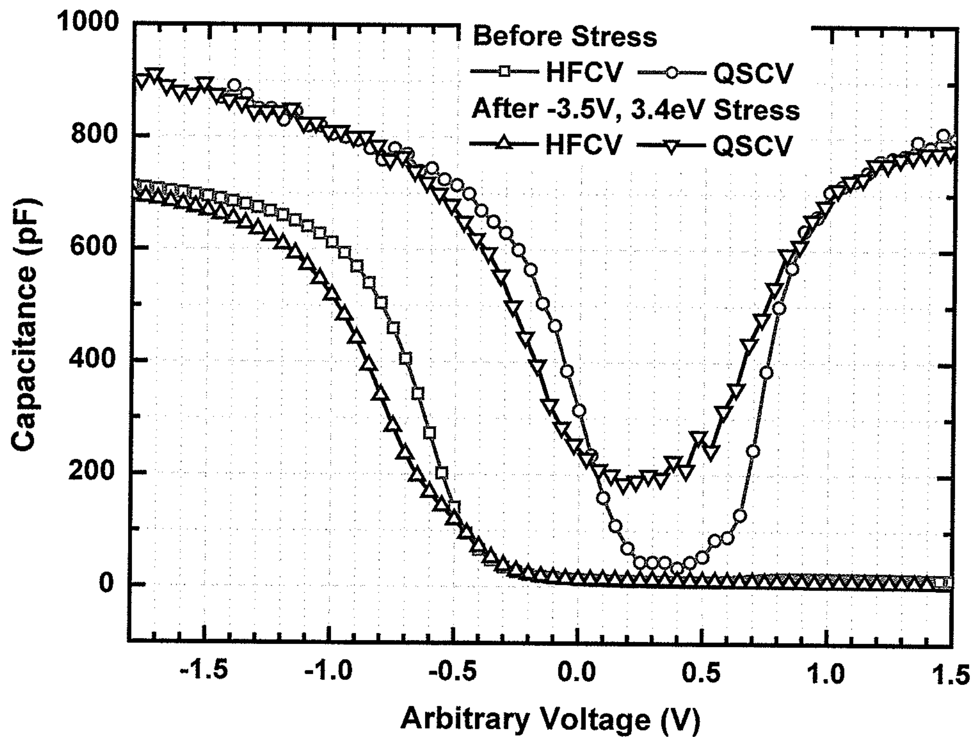


Figure 8.10: The HFCV and QSCV responses before and after the -3.5V, 3.4 eV stress shown in Figure 8.9. The CV curves were translated along the voltage axis for clarity.

In summary, the application of the HFCV technique for measurement of oxide trapped charge has been discussed including a description of the typical trapping and detrapping behaviour of high-κ HfO_2 capacitors as measured through the monitoring of the flat-band voltage shift as a function of injected charge. It was also noted that in this work, the interface state generation was minimized by using low applied fields.

8.2 Photocurrent-Voltage (Photo IV) Shifts

The benefit of using photocurrent measurements for characterization of oxide charge is that information may be obtained to distinguish not only the density of trapped charge within the oxide but also its location. In the following section an introduction to the measurement of photo IVs is given, including the basic photocurrent response of the HfO_2 devices. A discussion of the more subtle requirements for very accurate measurement of oxide trapped charge is also included. The application of the photo IV technique to gate and substrate injection is presented in Sections 8.3 and 8.4, respectively.

For the purposes of this work, initial photocurrent-voltage measurements were made at an initial "detrapped" state, and finally once again when charge has been injected into the oxide. Therefore, the voltage shift in the photocurrent response was then used to obtain the centroid of oxide trapped charge and total charge density. An example of photocurrent voltage measurements for HfO_2 capacitors is given in Figure 8.11. The photocurrent densities and dark current responses of these devices, shown in Figure 7.14, demonstrate that the photocurrent is more than 10× larger than the dark currents. This is expected with the applied photon energies (3.4 and 4 eV) inducing appreciable photocurrents as was discussed in Chapter 6.

In Figure 8.11, the photo IV response of a stressed device (red circles) is shifted with respect to the photo IV response at a detrapped state (black squares). It should be noted for the higher biases, the shifts are parallel. The photo IV response at negative biases shifts negatively (left) due to the presence of trapped oxide charge. At positive

biases, the shift is positive. It should be noted (as shown in Figure 8.11) that the shift for positive biases is only parallel at biases greater than ~1.5V. This is expected because the applied bias must be large enough so that the zero field distance is close to the injecting surface (see Section 2.5.2). Otherwise, the assumption that the quantity of oxide charge before the zero field point is negligible would be inaccurate. The parallel shifts seen in the photocurrent response validates the theory developed in Chapter 2.5.2, which predicts the parallel voltage shifts in photo IV response, and bodes well for the use of photo IV techniques to characterize the trapped charge in these high-κ HfO_2 capacitors.

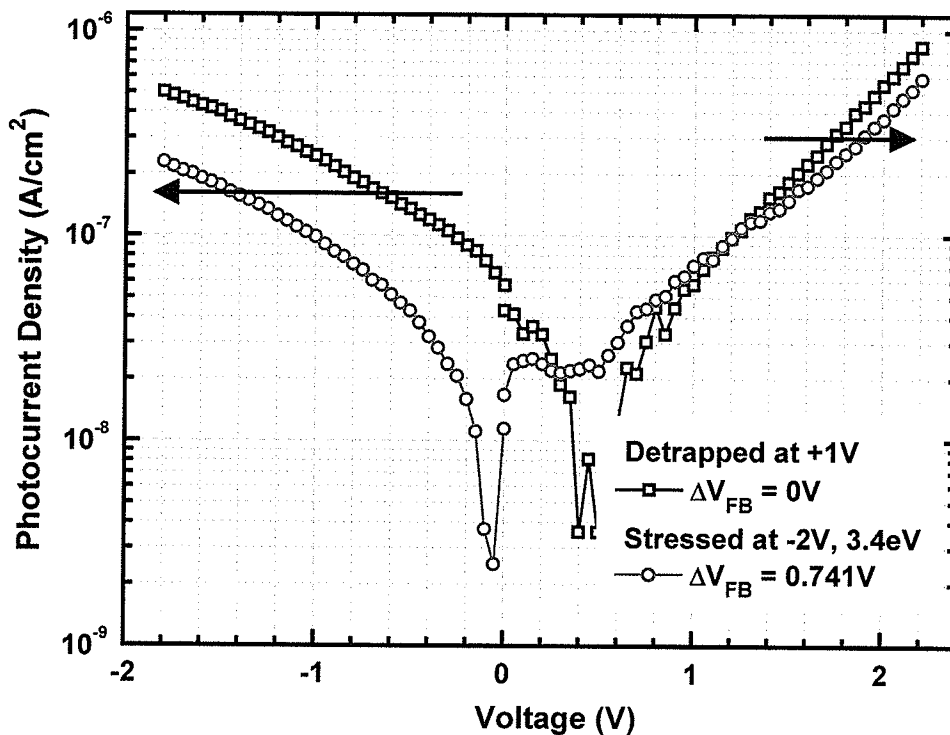


Figure 8.11: The photo IV measurement of a 1×10^{-3} cm^2, 90Å HfO_2 capacitor at fully detrapped, and stressed conditions.

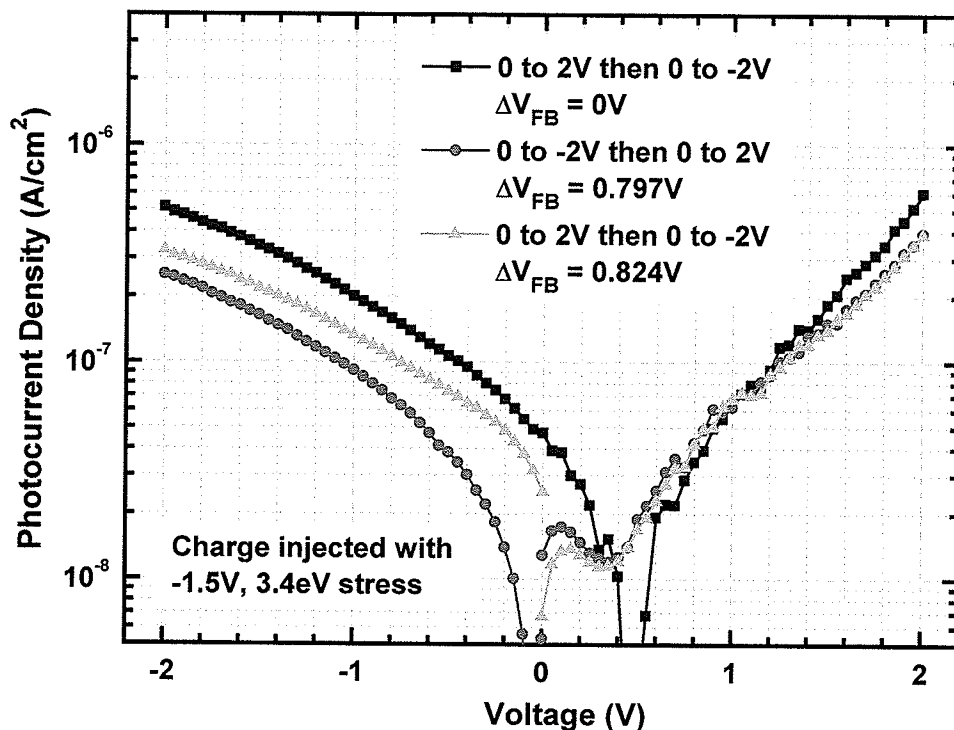


Figure 8.12: The effect on measured photo IV shifts due to the order of voltage sweeps. These measurements were taken using a 2×10^{-3} cm^2, 90Å HfO_2 device.

One important consideration when taking photo IV measurements is the perturbation of the trapped charge density the measurement itself may have. The photo IV technique can potentially disturb a significant portion of the trapped charge because a) the same illumination is provided to the sample during stress pulses is used, and b) both positive and negative applied bias sweeps require that applied electric fields are ~1-2 MV/cm (i.e., an applied bias greater than ~1V for a 90Å device). Therefore, consideration was given to the measurement conditions, such as measurement time and the order of voltage sweeps.

The effect that the order of sweeps has on photo IV response is shown in Figure 8.12 using a 2×10^{-3} cm^2, 90Å HfO_2 device. In this case the initial, "detrapped", response

is measured by sweeping positive polarities prior to the negative bias case. This is reasonable because the applied bias prior to photo IV measurement (the detrapping bias of +1V) is also positive. The other two photo IV responses were measured using different sweep order, but at similar V_{FB} values. From the figure, it is clear that the photo IV response at positive bias is virtually independent of which polarity is swept first. However, this is definitely not the case for the negative bias photo IV response. In that case, the photo IV shift when sweeping positive polarity first is ~1/2 of shift obtained when sweeping negative bias first. One explanation for this trapping behaviour is the presence of energetically shallow defects in the HfO_2 layer. As mentioned in Section 7.1, these defects would readily communicate with the gate electrode and not the substrate. Therefore, it is preferable to sweep negative bias polarities prior to the positive biases.

8.3 Gate Injection

In the following section, results of both the high-frequency capacitance-voltage (HFCV) and photocurrent voltage techniques are presented. These techniques were used for investigating the oxide trapped charge and monitoring the trapping behaviour of HfO_2 devices resulting from electron injection from the gate electrode. Firstly, the observed voltage dependence on the measured effective density of trapped charge is discussed. This is followed by the results from photocurrent measurements that were used to calculate the oxide trapped charge centroid and charge density. Lastly, the calculation of capture cross-sections based on first order trapping kinetics and the measured shifts in HFCV response are presented.

It is shown in Figure 8.13 that the saturation level of the V_{FB} has a dependence on the applied bias during stressing. These data were measured using a 5×10^{-4} cm^2, 90Å HfO_2 capacitor that was under 3.4 eV illumination. This device was stressed multiple times at the applied biases shown (-1.25 to -2.5V). In between the individual stresses, a +1V bias was used to detrap electrons from the oxide.

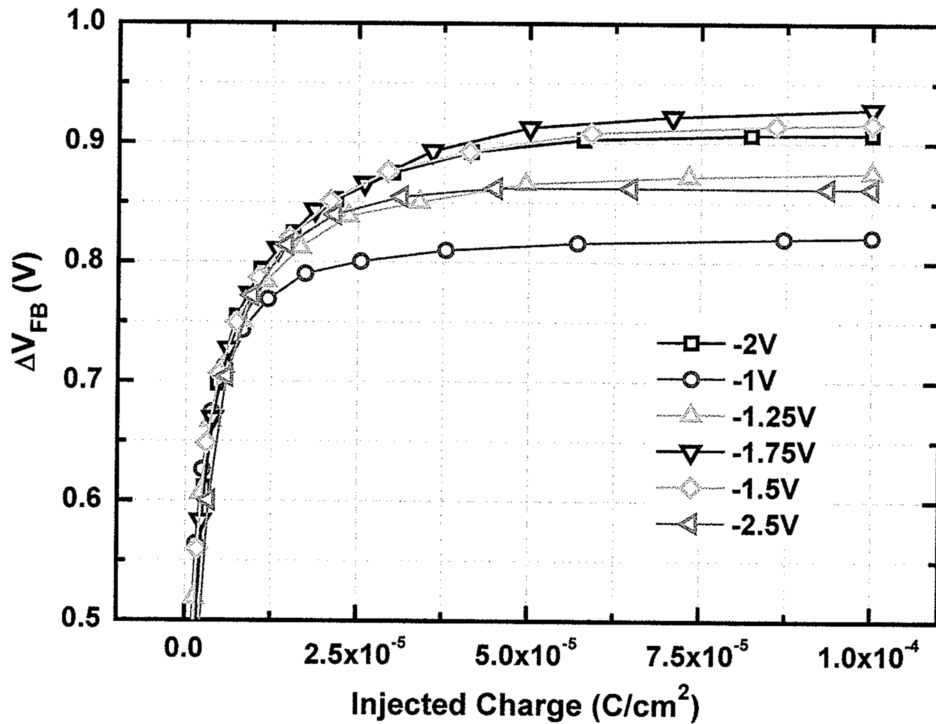


Figure 8.13: The ΔV_{FB} as function of injected charge for a 5×10^{-4} cm^2, 90Å HfO_2 device stressed at -2V, -1V, -1.25V, -1.75V, -1.5V, and -2.5V and under 3.4 eV illumination. Between stresses, a 1V bias in the dark was applied to detrap the device.

It is expected that the V_{FB} will saturate as a function of injected charge when all of the defects are filled, assuming no trap generation and no detrapping. The electron

trapping rate for charge in the oxide is not only dependent on the number of available traps in the film but also the probability of trapping an electron. However, should it exist, the detrapping (rate) of already-trapped charge [38] must also be accounted for. The detrapping of oxide charge can occur through thermal excitation of trapped electrons, photoexcitation of trapped electrons (i.e., due to the use of illumination during stressing), or by field-assisted mechanisms (i.e., direct tunnelling out of traps) [38]. Therefore, the net effective trapped charge (as measured by the saturation in V_{FB}) is a result of trapping and detrapping rates implying that a saturated V_{FB} level is likely to be bias dependent.

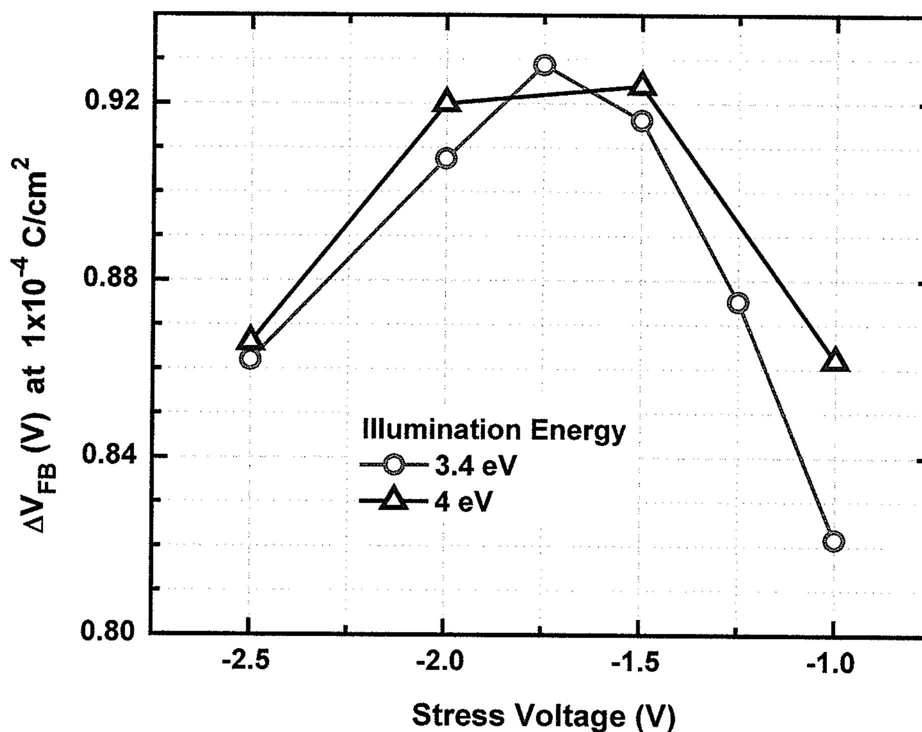


Figure 8.14: The measured ΔV_{FB} as a function of the stress voltage. The ΔV_{FB} was measured after 1×10^{-4} C/cm^2 of charge was photoinjected.

To investigate the dependence of the oxide charge trapping on stress voltage, the ΔV_{FB} at an injected charge level of 1×10^{-4} C/cm^2 was extracted as a function of stress voltage and is shown in Figure 8.14 where the red circles data were extracted from Figure 8.13. On the other hand, the blue triangles data were measured on a different 90Å HfO_2 capacitor stressed using a higher photon energy of 4 eV. These results indicate that a turnaround in the "effective" density of trapped oxide charge in these devices as a function of stress voltage occurred. The decrease in ΔV_{FB} at stress voltages greater than ~-1.75V was the result of field-assisted detrapping of oxide charge.

To extract the centroid of the distribution of trapped charge, photo IV measurements were also taken and some of the results are shown in Figure 8.15. These measurements were taken after injecting 1×10^{-4} C/cm^2 of electrons (i.e., after V_{FB} saturation). The reference photo IV response (indicated by black squares) used for voltage shift measurements was taken after normally complete detrapping at an applied bias of +1V. From this figure it is clear that parallel shifts in photocurrent response were measured, and that the voltage shifts at negative applied bias were much larger than at positive biases.

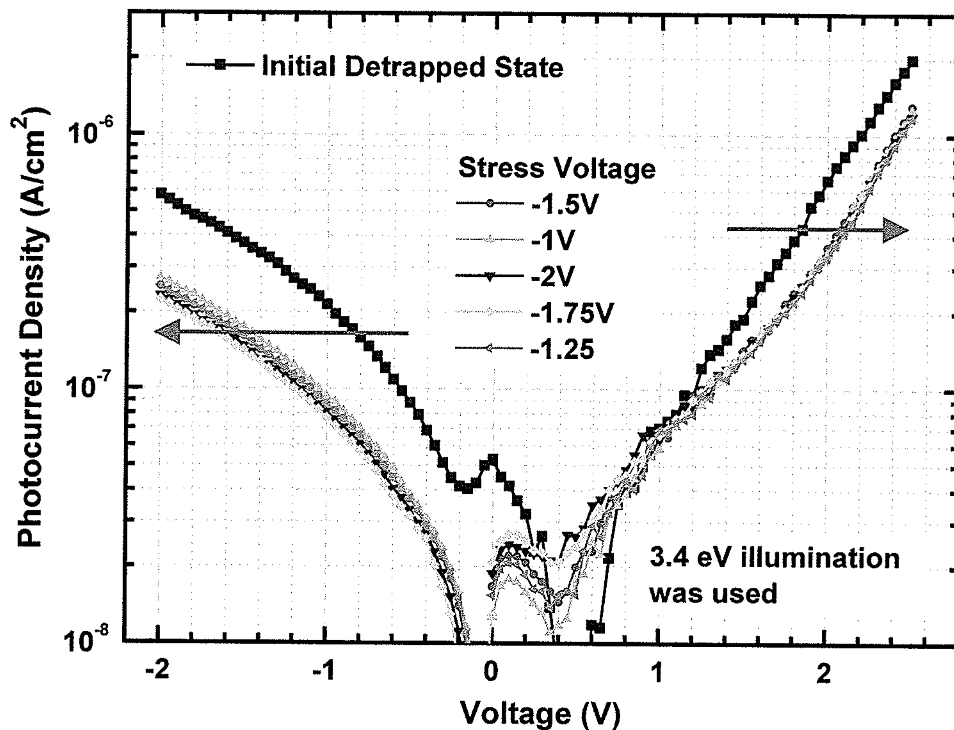


Figure 8.15: The measured photo IV response of a 2×10^{-3} cm^2, 90Å HfO_2 capacitor before and after stressing at negative biases and with a 3.4 eV illumination.

In order to investigate the photocurrent-voltage shifts in more detail, select portions of the photo-IV responses, at both negative and positive biases, are shown in Figures 8.16 and 8.17, respectively. In Figure 8.16, it is clearly shown that the photo IV shifts measured at negative biases show a small but measurable dependence on the applied stress voltage. This was not the case for the photo IV responses measured at positive biases, as shown in Figure 8.17 where all measured responses taken after charge injection were very similar to one another, and little if any stress voltage dependence is evident.

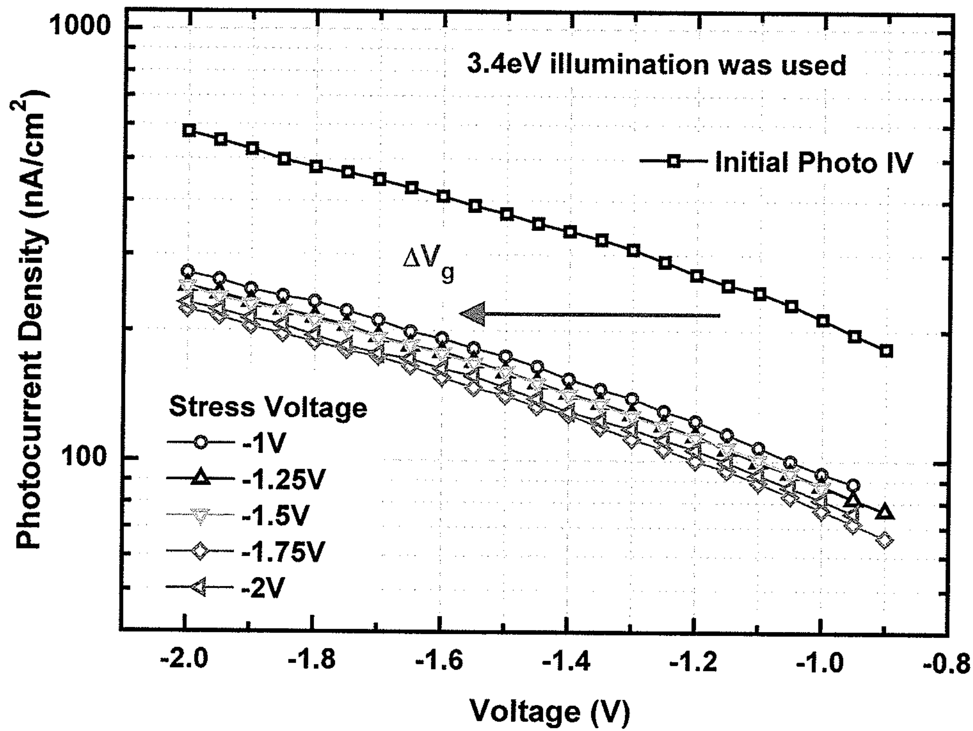


Figure 8.16: The negative bias photo IV response of the measurements shown in Figure 8.15.

The oxide trapped charge parameters obtained from both the HFCV and photo IV techniques are shown in Table 8.1. In this table, the calculated centroid of oxide trapped charge, $\bar{x}/L$, is given. This value was calculated using equation (2.45) and the measured voltage shifts in the photo IV response. These shifts all result in a centroid between ~0.19 to ~0.24, which is much closer to the gate electrode than the substrate. Therefore, these measurements suggest that electrons are primarily trapped at bulk defects within HfO_2 and not at the interfaces closer to the silicon substrate.

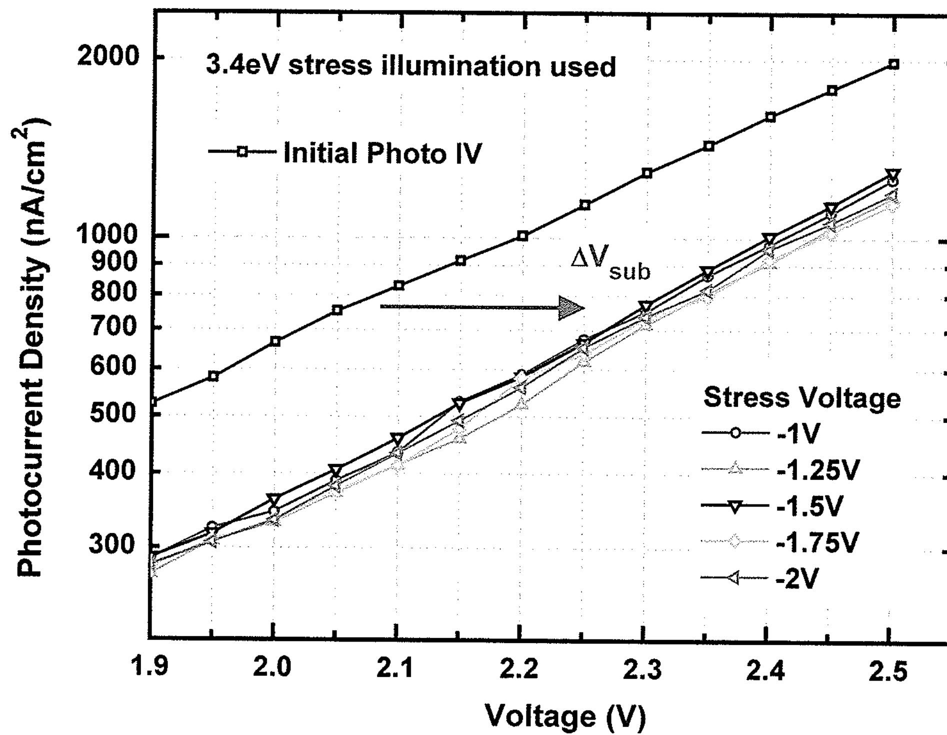


Figure 8.17: The positive bias photo IV response of the measurements shown in Figure 8.15.

Table 8.1: The calculated effective oxide trap density and charge centroid from HFCV and photo IV measurements.

Stress Voltage (V)	HFCV N_{eff} ($\times10^{12}$ cm^{-2})	$\bar{x}/L$ Centroid	$\bar{x}/L$ Error	Photo IV N_{eff} ($\times10^{12}$ cm^{-2})	Error for Photo IV N_{eff} ($\times10^{12}$ cm^{-2})
-2	4.62	0.20	0.02	6.46	0.15
-1.75	4.99	0.19	0.02	6.72	0.15
-1.5	4.60	0.22	0.03	6.07	0.15
-1.25	4.51	0.22	0.03	5.90	0.15
-1	4.48	0.24	0.03	5.47	0.15

In Table 8.1, the calculated values for the effective trapped charge, N_{eff}, are listed. These values were determined from the measured voltage shifts of the HFCV response, using Equation (2.36), and from the photo IV response using Equation (2.44). In all calculations, the measured C_{ox}/A value of 8.55×10^{-7} F/cm^2 for 90Å HfO_2 devices (see Section 7.1) was used instead of using the specific values for the relative permittivity of the insulator stack, ε_o, and its thickness, t_{ox}.

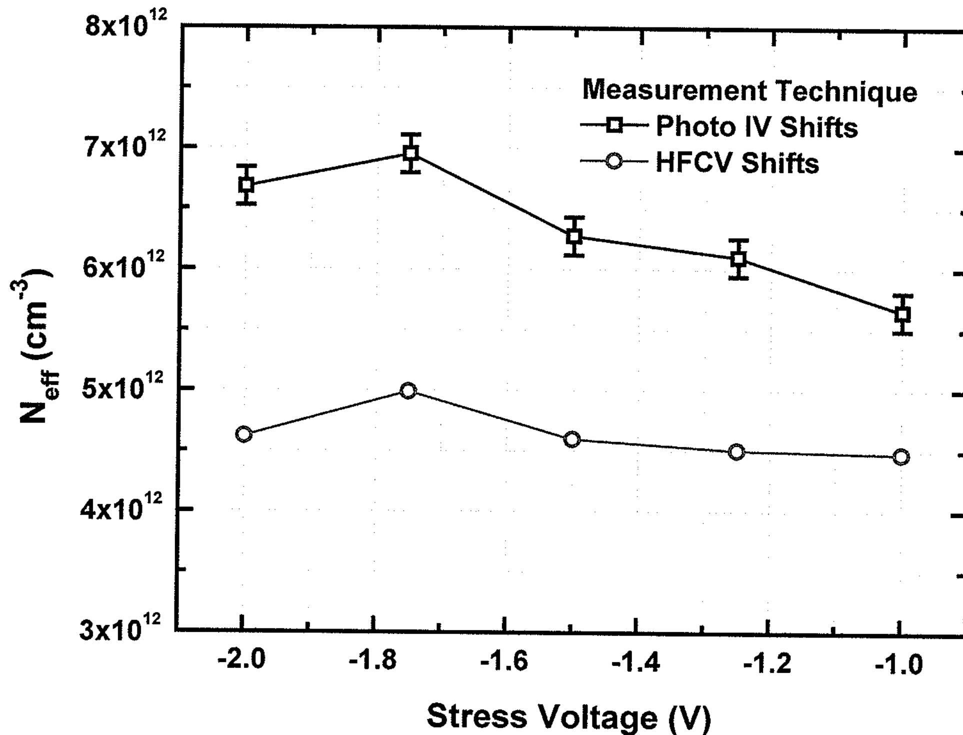


Figure 8.18: The effective density of trapped charge obtained from the photo IV and HFCV shift measurements shown in Table 8.1.

The calculated effective trap densities are shown in Figure 8.18 as function of stress voltage for both measurement techniques. These effective charge densities

extracted from both measurements (photo IV and HFCV) agree considerably well because there was similar stress voltage dependence (i.e., the N_{eff} was largest for –1.8V, and smallest for –1V). However, the photo IV values are ~40% larger than the corresponding HFCV values because of the assumptions made for the N_{eff} calculation in Equation (2.36). In the case of the HFCV measurement it is implicitly assumed that all the trapped oxide charge is located at the interface near the silicon substrate (i.e., $\bar{x} = 1$). If the distribution of trapped charge is away from that interface, as it is for these device as is evident from the shift in photocurrent response, the effective density value determined using the ΔV_{FB} will underestimate the actual effective density of defects, hence leading to a lower value of N_{eff}.

When considering electron trapping within dielectrics, first-order trapping kinetics is often used as a simple model to extract information pertaining to the nature of the defects, specifically capture cross-section of the trap [38]. The basis of the model is a rate equation for the filling of traps within the dielectric, as given by

$$\frac{dn_t}{dt} = n_c v_{th} \sigma_c (N - n_t) - F_p \sigma_p n_t - N_c v_{th} \sigma_c \exp\left(-\frac{E_T}{k_B T}\right) \quad (8.1)$$

where n_t is the volume density of filled traps, n_c is the conduction band electron density, v_{th} is thermal velocity, σ_c is the capture cross-section of the trap, N is the total trap density, F_p is the localized photon flux, σ_p is the photoionization cross-section, N_c is the density of states in the conduction band, E_T is the trap depth, k_B is Boltzmann's constant, and T is temperature [38]. This equation relates the electron trapping rate to a) the rate in which conduction band electrons are captured, b) the rate at which trapped electrons are

photodetrapped, and c) the rate at which trapped electrons are thermally detrapped. For the sake of this argument it is assumed that the defects are energetically deep enough that thermal detrapping can be neglected (i.e., trap depth >> k_BT). Another simplifying assumption is that the photoionization cross-section of the defects, and/or the photon flux of the illumination are sufficiently small so that photodetrapping can also be neglected [40]. In such a case, equation (8.1) can be solved to obtain the expression,

$$N_{eff}(t) = N_T\left(1 - \exp\left(\frac{t \cdot J}{q}\sigma_c\right)\right) \tag{8.2}$$

where N_{eff} is the density of filled traps (n_T integrated over the thickness of the dielectric), N_T is the total trap density (N integrated over the thickness of the dielectric), and J is the current density through the dielectric [38]. The assumption being made in equation (8.2) is that,

$$J = n_c v_d \approx n_c v_{th} \tag{8.3}$$

where v_d is the drift velocity of carriers in the conduction band [38]. Therefore, it is assumed that the current measured by the external circuit, J, by way of a current continuity argument, is representative of the current within the conduction band. For the sake of this argument, this is assumed to be a valid assumption. There is, however, a possibility that it may not be entirely true for HfO_2 dielectrics where electron transport has been suggested that current transport through the dielectric could be trap mediated (i.e., Frenkel-Poole hopping or trap-assisted tunnelling) [40, 54]. In this case, slight modifications of Equation 8.3 would be required. Nonetheless, the data will bear out the validity of this assumption.

Applying equation (8.2) to the data shown in Figure 8.13 results in a relatively poor fit to these simple 1st-order trapping kinetics. However, if it is assumed that there are two types of defects within these devices, a more reasonable fit to the data was obtained as shown in Figure 8.19. In the two defect case, the appropriate fit is of the form

$$N_{eff}(t) = N_{T1} + N_{T2} - \exp\left(\frac{t \cdot J}{q}\sigma_1\right) - \exp\left(\frac{t \cdot J}{q}\sigma_2\right) \tag{8.4}$$

where N_{T1} and N_{T2} are total trap densities of the two defects, and $\sigma 1$ and $\sigma 2$ are the capture cross-sections for the two defects.

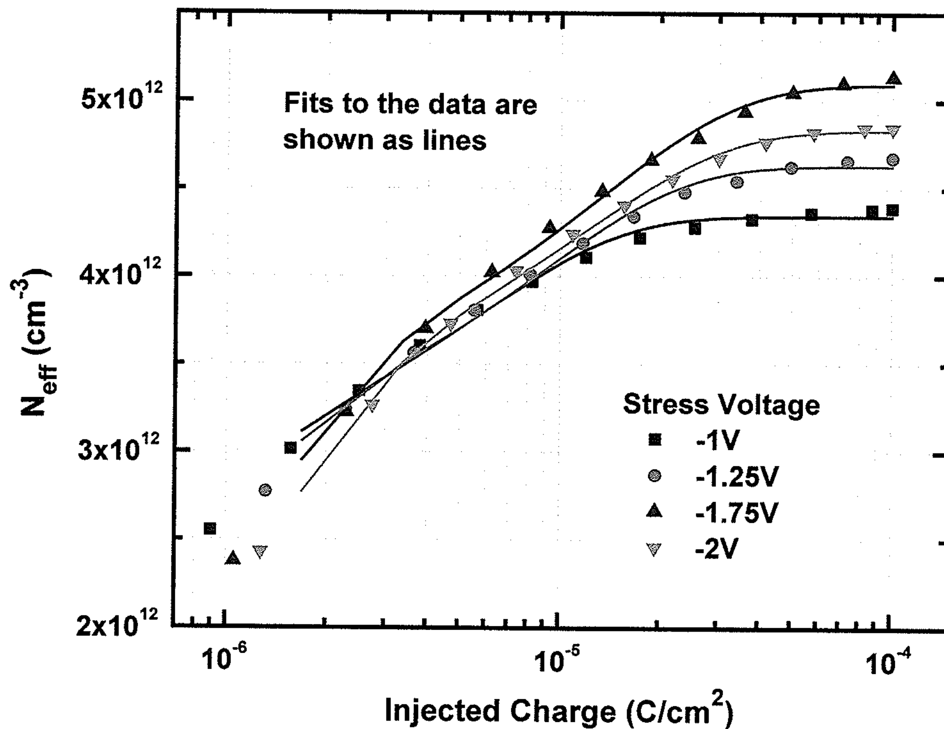


Figure 8.19: The effective density of trapped oxide charge versus injected charge for the gate injections shown in Figure 8.13. The data (shown as symbols) was fitted (shown as lines) using equation (8.4).

The plots in Figures 8.20 and 8.21 contain the parameters, the total trapped defect density and capture cross-section for both type of defects extracted from the measured HFCV shift due to electron injection. The total trapped defect density for each of these defects is shown in Figure 8.20. In this figure, the total defect density for both types of traps exhibit the same response as a function of the stress bias. However one of the defects has a concentration twice that of the other. The extracted capture cross-sections for these two defects are shown in Figure 8.21 and were averaged to be $\sim 2.2\times10^{-13}$ cm^2 and $\sim 1.9\times10^{-14}$ cm^2. Due to their relatively large size, these capture cross-sections would imply that these defects are coulombic in nature [38, 55]. It should be noted that the defects with the larger cross-section, shown in Figure 8.21, seems to have a slight voltage dependence (i.e., a decrease in capture cross-section with increasing electric field). According to published literature [38, 55], there is a voltage dependence for such coulombic centers. However, a larger sample size (with a wider range in applied bias) is required to make any definitive assertions about this dependence. For that reason, an average cross-section value was taken, as shown by the linear fit in Figure 8.21.

In summary, both the HFCV and photo IV techniques were used to access the effective density of traps and centroid of oxide trapped charge within these HfO_2-based dielectrics arising from electron injection from the gate. In all tests performed on these dielectrics, the centroid was located nearer to the gate electrode, indicative of trapping at bulk HfO_2 defects. Also, trapping kinetics were used to model gate electron injection and a reasonable fit of the measurement data to a two defect model was obtained, resulting in the calculation of capture cross-sections.

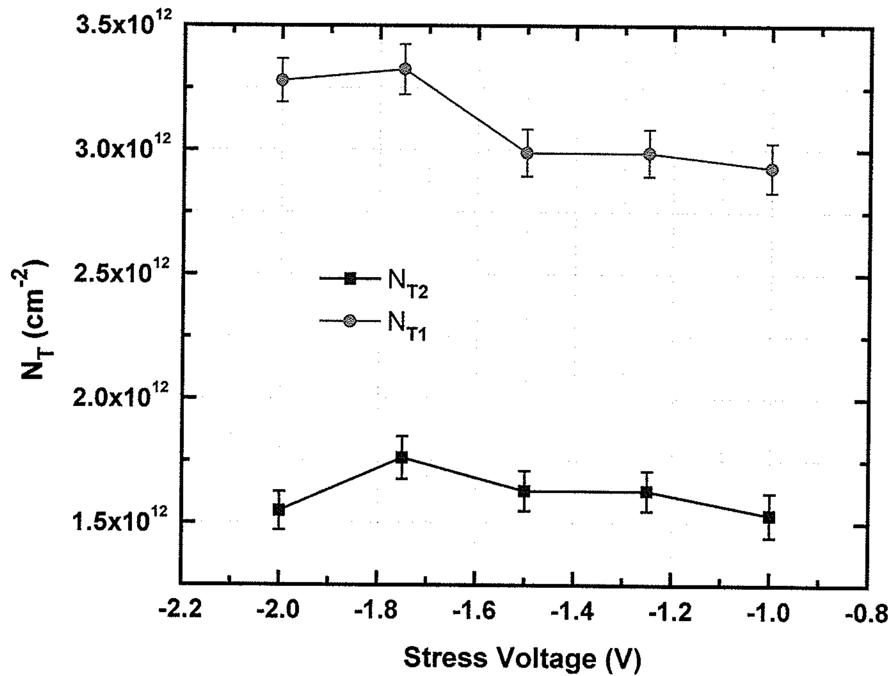


Figure 8.20: The values for the total trap density parameters of equation (8.3) as a result of fitting the measurement data from Figure 8.13.

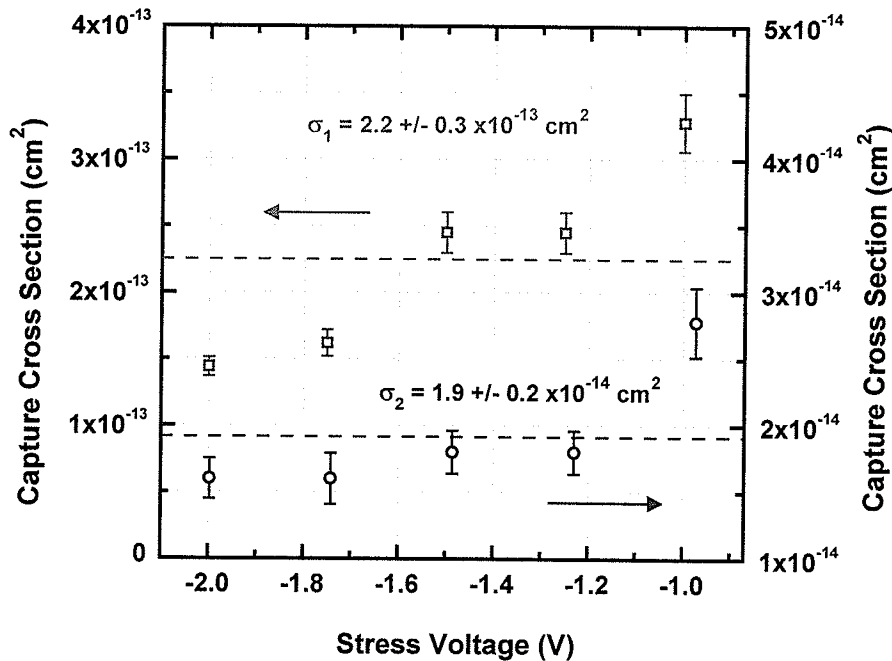


Figure 8.21: The values obtained for the capture cross-section when equation (8.3) is used to fit the measurement data from Figure 8.13.

8.4 Substrate Injection

In this section, electron injection from the substrate and subsequent trapping of oxide charge is discussed. Similar to the previous section, both HFCV and photo IV techniques were used to obtain the oxide trapped charge centroid and a net effective density of trapped charge.

The typical HFCV response due to the injection of electrons from the substrate is shown in Figure 8.22. The trapping rate of electrons within the dielectric is largely dependent on the applied bias. The largest shift in HFCV response was measured at the lowest applied bias, 0.75V, indicated by the black squares. The key feature to note at that low stress bias is that very little charge was injected into the dielectric ($\sim 2\times10^{-7}$ C/cm^2). The trapping probability, P_{TR}, which is the ratio of number of electrons trapped to the number of electrons injected, is determined using the expression,

$$P_{TR} = \frac{q \cdot N_{eff}}{Q_{inj}} \tag{8.4}$$

where Q_{inj} is the total charge injected into film, and N_{eff} is the effective density of oxide traps. The trapping probability for the 0.75 V stress bias shown in Figure 8.22 was ~1, meaning that almost every injected electron becomes trapped. For such a small applied bias two explanations are possible. The applied bias was too small to inject a significant number of carriers. This could occur, as the applied bias was only slightly larger than the work-function difference between aluminum and silicon. It is also possible that the bias is so low that detrapping of (already) trapped electrons is non-existent. As the applied field increases, field-assisted detrapping increases and subsequently the effective trapping

probability decreases resulting in a lower saturation V_{FB} (i.e., a lower effective density of net trapped charge). At applied biases greater than or equal to 1.5V, the injection rate increases with voltage resulting in an increase in the net effective density of trapped charge. The dependence of the ΔV_{FB} on applied positive bias is shown in Figure 8.22 for a 1×10^{-3} cm^2, 90Å HfO_2 device (black squares in Figure 8.23) and for another device with an area of 2×10^{-4} cm^2 (red circles in Figure 8.23). The small difference in the V_{FB} shifts measured (~20 mV) can be associated with inconsistencies in determining the exact initial V_{FB} for the two capacitors (i.e., a small error due to oxide charge that is not fully detrapped prior to stressing). However, both devices do have similar HFCV responses as a function of applied bias.

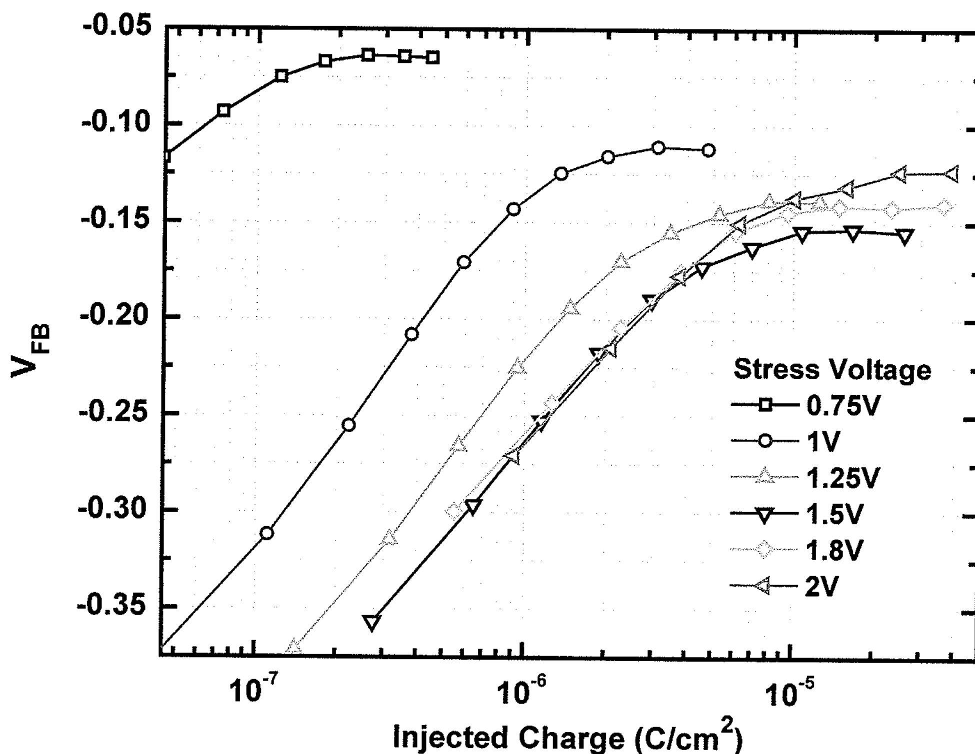


Figure 8.22: The V_{FB} versus injected charge for positive bias stress voltages using illumination with a photon energy of 3.4 eV. The device was a 1×10^{-3} cm^2, 90Å HfO_2 device.

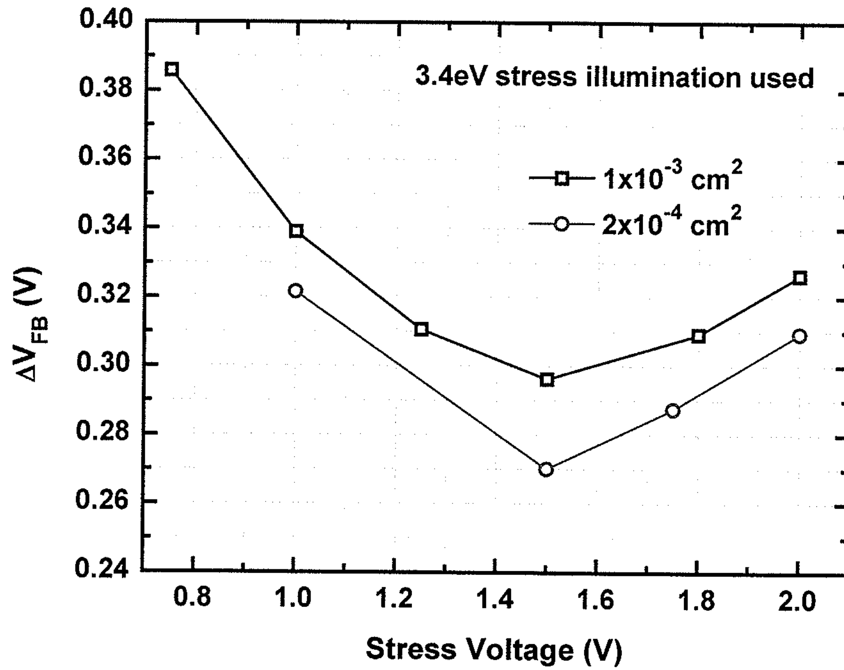


Figure 8.23: The measured ΔV_{FB} as a function of the stress voltage. The ΔV_{FB} was measured at saturation.

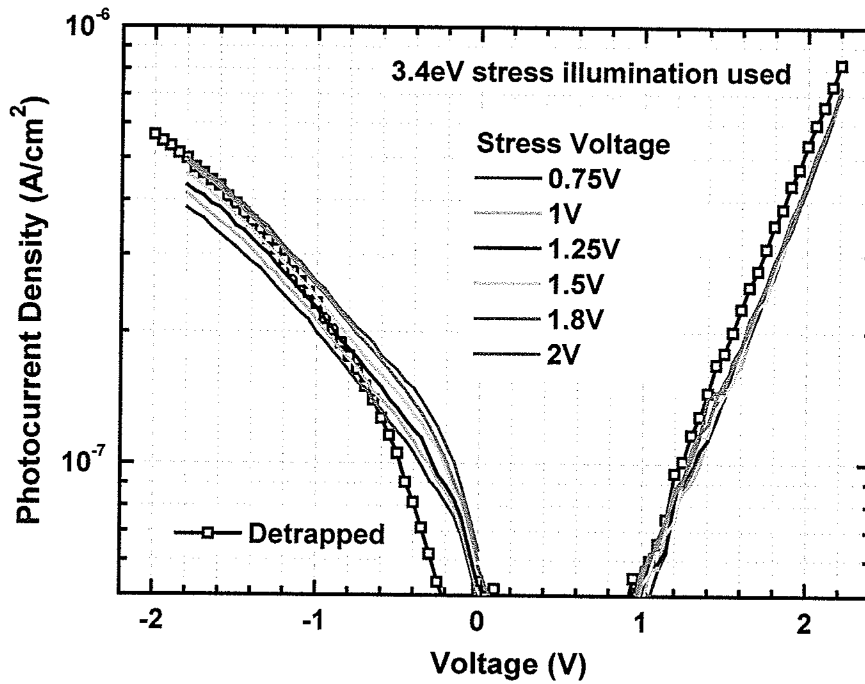


Figure 8.24: The measured photo IV response of a 1×10^{-3} cm^2, 90Å HfO_2 capacitor before and after stressing at positive biases and 3.4 eV illumination.

The typical response in photocurrent due to the electron injection from the substrate is shown in Figure 8.24 for applied biases ranging from 0.75V to 2V. One observable feature in these photo IV measurements that differs from the gate injection case (Figure 8.15) is the lack of voltage shift for the negative biases photo IV. For larger applied stress biases (1.8V and 2V) the negative bias photocurrent is identical to the photocurrent response of the device when fully detrapped. It should also be noted (from the data in Figure 8.25) the negative bias photo IV shifts negatively with decreasing applied bias. Such a response is indicative of field assisted detrapping of electrons from the bulk HfO_2 layer near the gate electrode. As bias increases, charge trapped near the gate electrode is readily detrapped resulting in the shifts observed in Figures 8.24 and 8.25.

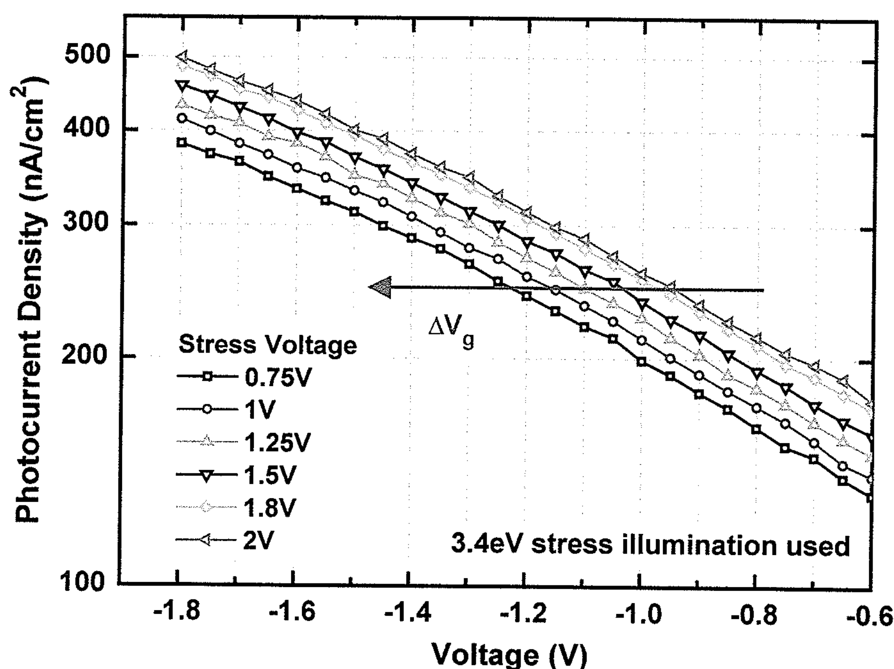


Figure 8.25: The negative bias photo IV response of the measurements shown in Figure 8.22

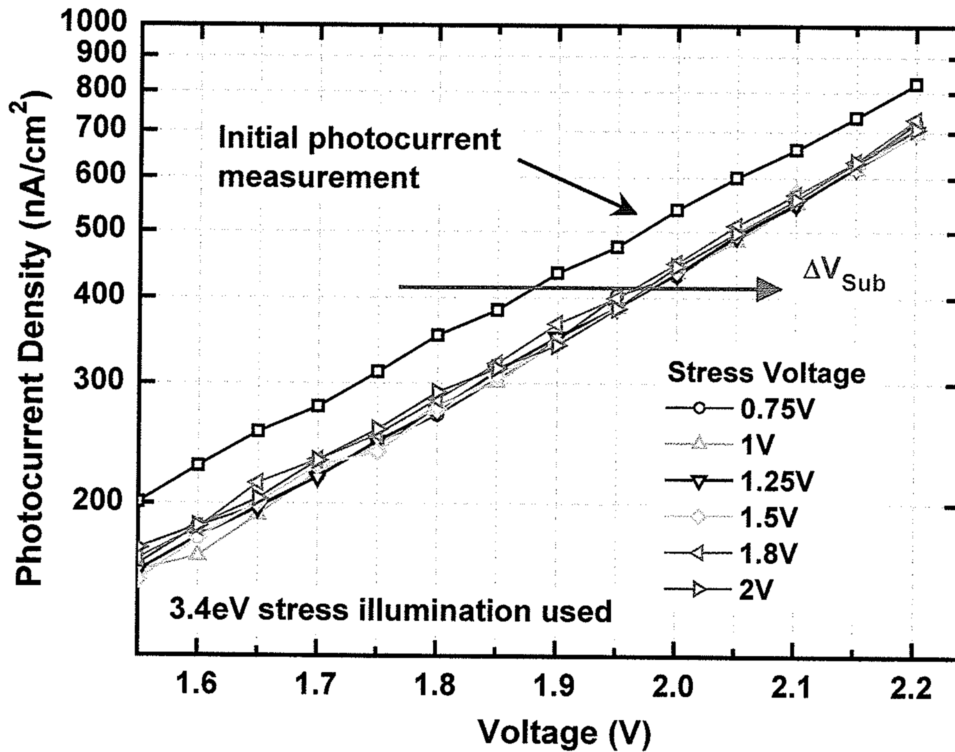


Figure 8.26: The positive bias photo IV response of the measurements shown in Figure 8.24.

The photo IV response at positive biases (for substrate injection) is shown in Figure 8.26. This response is similar in nature to the photo IV measurements taken for gate injection in that there is no clear indication photo IV shift dependence on the applied stress bias. Therefore, it may be assumed that the density of trapped charge near the substrate does not alter appreciably with change in the stress bias. Evidence of this is given in Table 8.2, where the measured shifts in V_{FB} and photo IV response are listed. The measured shifts in positive bias photo IV remains approximately equal, (~0.1 V), for all stress conditions. This is not the case at negative bias photo IV shifts which range from ~–0.35 to 0V. The oxide charge centroids for each these measured shifts are shown

in Table 8.3. As expected the centroid of charge distribution ranges from near that aluminum gate ($\bar{x}/L \sim 0.22$) to that approximately at the silicon interface ($\bar{x}/L \sim 1$) indicative of the increased detrapping of trapped charge near the gate at higher applied fields.

Table 8.2: The measured shift in HFCV and photo IV responses from substrate injection of electrons.

Stress Voltage (V)	HFCV ΔV (V)	ΔV_g (V)	ΔV_{sub} (V)
0.75	0.507	-0.349	0.099
1	0.461	-0.258	0.100
1	0.484	-0.275	0.100
1.25	0.432	-0.171	0.095
1.5	0.418	-0.115	0.089
1.5	0.456	-0.122	0.100
1.8	0.431	-0.036	0.081
2	0.448	0.000	0.093
2	0.485	0.000	0.100

In Table 8.3 the effective density of trapped charge for both the HFCV and the photo IV measurements is presented. The use of photocurrent measurements for this calculation is somewhat misleading due to the large detrapping effect discussed previously. However, the ΔV_{FB} measurements used to determine N_{eff} are at least self-consistent and yield values for N_{eff} range between 2.23×10^{12} and 2.71×10^{12} cm^{-2}.

Table 8.3: The calculated effective trap density and the centroid of charge distribution extracted from the measured shifts in HFCV and photo IV response.

Stress Voltage (V)	HFCV N_{eff} ($\times10^{12}$ cm^{-2})	$\bar{x}/L$ Centroid	$\bar{x}/L$ Error	Photo IV N_{eff} ($\times10^{12}$ cm^{-2})	Error for Photo IV N_{eff} ($\times10^{12}$ cm^{-2})
0.75	2.71	0.22	0.06	2.39	0.15
1	2.46	0.28	0.08	1.91	0.15
1	2.59	0.27	0.08	2.00	0.15
1.25	2.31	0.36	0.11	1.42	0.15
1.5	2.23	0.44	0.16	1.09	0.15
1.5	2.44	0.45	0.15	1.19	0.15
1.8	2.30	0.69	0.45	0.63	0.15
2	2.39	1.00		0.50	0.15
2	2.59	1.00		0.53	0.15

In summary, substrate injection results for both HFCV and photo IV measurements have been presented. The average effective density of trapped oxide charge, as determined from the ΔV_{FB}, was found to be $2.5\times10^{12} \pm 0.2\times10^{12}$ cm^{-2}. It was also found that as the applied stress bias increases, the oxide trapped charge centroid was shifted away form the gate contact, towards the dielectric/silicon interface.

8.5 Discussion of Results

This analysis of the measured voltage shifts in HFCV and photo IV response has provided information pertaining to the nature of defects within the HfO_2-based dielectric stack. The results from electron gate injections, where it was determined that the oxide

trapped charge centroid is located near the gate electrode, $\bar{x} / L \sim 0.2$, is evidence that a significant portion of the electrons traps within these dielectric stacks is located at pre-existing defects within the bulk HfO_2 layer. This is not uncommon for similar HfO_2 based dielectrics [16, 56, 57]. However, these data do not suggest that electron trapping near the HfO_2/SiO_x or SiO_x/HfO_2 interfaces does not occur as well. Photocurrent measurements in the positive bias side, for both gate and substrate injection, indicate that electron trapping near the substrate electrode is also occurring, however to a much lesser degree (i.e., lower density of trapped charge) than that nearer to the gate electrode.

One experimental observation in this work is that defects within these dielectrics readily communicated with the gate electrode. This was evident when devices were under illumination (i.e., the shifts in photo IV response at negative biases that indicate readily trapped and detrapped oxide charge), and in the dark (i.e., the measured hysteresis in the HFCV response that was dependent on applied bias). Such characteristic behaviour lends credence to the theory that bulk HfO_2 defects are situated energetically at shallow (at an energy level between the Fermi level of the aluminum gate and the conduction band of HfO_2) trap depths. However, it was previously assumed that thermal detrapping of charge is not a concern (i.e., the assumption made within the first order trapping kinetics argument in order to obtain a reasonable fit of the trapping results). This assumption would limit the possible trap energy of the defect to an energy state near the Fermi level of aluminum, where thermal detrapping of charge is improbable (i.e., $E_T \gg k_B T$). Therefore, it is suggested that the presence of bulk HfO_2 defects with a trap depth near the aluminum Fermi level provides a reasonable explanation for both the

oxide charging behaviour measured in the dark and with illumination. In the dark, electrons could tunnel in and out of the bulk HfO_2 defects depending on the applied bias. Under illumination, electrons are photoinjected into the conduction band of the HfO_2 and subsequently get trapped at these defects.

The previous argument for the energy level of HfO_2 defects relied upon the validity of using first order trapping kinetics to fit the trapping data. Some researchers have suggested that the conduction within HfO_2 is not electron drift limited (which is the case for SiO_2 and assumed in equation (8.3)), but Frenkel-Poole hopping dependent (the capture and emission of electrons from shallow traps) [54]. If that is in fact the case, the fit provided by equation (8.2), despite fitting the data well, would be inaccurate. Also, in such a case, it could be argued that energetically shallow traps (i.e., close to the conduction band of HfO_2) were the defects present in these films. However, for this work, it was assumed that first order trapping kinetics do apply, and the very reasonable fits to measured trapping data is validation of this assumption.

Evidence of two distinctive traps within these dielectrics, as extracted using first-order trapping kinetics, is also not uncommon for HfO_2-based capacitors and has been suggested in other oxide charge studies as well [8, 56, 57]. The large extracted capture cross-sections of $\sim 2\times10^{-13}$ and $\sim 2\times10^{-14}$ cm^2 are indicative of the readily trapped defects in the films used in this research.

Chapter 9 Conclusion

The nature of electronically active defects in high-κ HfO_2-based dielectrics was investigated in this research, including the use of the photocurrent-voltage technique for obtaining the centroid of the oxide trapped charge distribution. The high-κ HfO_2 dielectrics used in this study were fabricated within an MOS capacitor structure. The defects under investigation were electron traps primarily within, but not limited to, the HfO_2 dielectric layer and were responsible for negative oxide charge trapping.

The hafnium dioxide dielectrics obtained for these studies were deposited using a metal-organic chemical vapour deposition (MOCVD) and had thicknesses of 50Å, 90Å, 115Å, and 680Å thick. These dielectrics were deposited on a p-type silicon substrate with an intermediate silicon dioxide dielectric with a thickness of ~15Å. The fabrication of the test capacitor structures from these provided samples was done with the blanket deposition of an aluminum gate electrode by thermal evaporation or DC sputtering, which was followed by lithographic and aluminum etching steps to define the device areas. The photocurrent measurement techniques used in this work required the production of a semi-transparent gate electrode, which was achieved with a deposition of ~140Å of aluminum. The thickness was verified to have an optical transmission > 15%.

Effective barrier height measurements were taken for both gate electron photoinjection and substrate electron photoinjection. The effective barrier height measured for electron photoinjection from the aluminum gate to the HfO_2 conduction band was 2.6 ± 0.1 eV, whereas no distinctive barrier height was obtained for substrate injection.

The characterization of the high-κ MOS capacitors in the dark was performed using high-frequency capacitance-voltage (HFCV), quasi-static capacitance-voltage (QSCV) and current-voltage (IV) techniques. The information obtained from these measurements included the oxide capacitance versus area relationship (i.e., $C_{ox}/A = 8.55\times10^{-7}$ F/cm^2 for 90Å HfO_2 capacitors), the "activated" substrate doping concentration (~1×10^{15} cm^{-3}), and the calculated (normalized) flat-band capacitance (i.e., $C_{FB}/C_{ox} = 0.1$ for 90Å HfO_2 capacitors).

The charge trapping analysis of the HfO_2 based devices was done using the "stress" and "sense" technique. The capacitors were "stressed" with the use of constant applied voltage and illumination at suitable energies. Subsequently, the charge in these devices was "sensed" with the use of either an HFCV or photocurrent-voltage (photo IV) measurement. The applicability of the photo IV technique for high-k characterization was shown in this work.

For gate electron injection (i.e., negative applied bias), the effective density of trapped oxide charge, N_{eff}, as measured using flat-band voltage shifts, ΔV_{FB}, was found to be between 4.5×10^{12} and 5×10^{12} cm^{-2} and had a measurable field dependence. A similar field dependence was found from the calculation of the N_{eff} from the photo IV shifts, where the N_{eff} was found to be between 5.5×10^{12} and 6.7×10^{12} cm^{-2}. The calculated centroid of oxide charge distribution was determined to be between 0.19 and 0.24, indicating that a large portion of trapped charge was located near the gate electrode (i.e., at bulk HfO_2 defects).

A similar trapping study was also performed for substrate electron injection, where N_{eff} was determined using ΔV_{FB} and found to be in the range of 2.3×10^{12} to 2.7×10^{12} cm^{-2}. The photo IV response following substrate injection resulted in the trapped oxide charge centroid that shifted from 0.22 to 1 for stress bias ranging from 0.75V to 2V. This shifting centroid was found to be indicative of the increased field-assisted detrapping of oxide charge at the pre-existing defects within the bulk HfO_2 under these bias conditions.

A first-order trapping kinetics model was used to fit the N_{eff} values extracted from the measured ΔV_{FB} for electron gate injection in order to obtain a capture cross-section for these electronically active defects. The analysis and fit suggest that two defects exist with cross-sections of $2.2\times10^{-13} \pm 0.3\times10^{-13}$ cm^2 and $1.9\times10^{-14} \pm 0.2\times10^{-14}$ cm^2.

The charge trapping analysis of high-κ MOS capacitors presented in this work has revealed spatially, the abundant, readily trapped defects that exist in the bulk HfO_2 layer. The nature of these electron traps jeopardizes the integration of such dielectrics into future MOS devices and further research is required to determine the origin of these defects and their energetic distribution.

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