Apparatus for Asynchronously Linking a Variable-Speed Self-Excited Induction Generator to an Isolated ac Electrical Load

by
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Submitted to the Faculty of Graduate Studies
in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy

The Department of
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BY

TREVOR L. MAGUIRE

A Thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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Abstract

This thesis describes the development of a novel apparatus for supplying an isolated ac load through a dc link from a self–excited induction generator. The generator is operable at variable speed. Machine voltage magnitude, load voltage magnitude, and load voltage frequency are simultaneously regulated to rated values during steady running and during changes in both load power and machine speed.

The self–excited induction machine supplies a controlled Graetz bridge rectifier in the dc link. A voltage–sourced inverter is used to supply the ac load. A voltage–boost converter interfaces the variable dc output voltage which is produced by the rectifier to the relatively fixed dc input voltage which is required by the voltage–sourced inverter.

A prototype electromagnetic transients program is described which is based on a modified Dommel algorithm. The prototype program is used to study the apparatus and associated controls. The program is particularly adapted for the simulation of power electronic apparatus at a system level. Individual switching devices are represented according to simple characteristic curves. The modified algorithm includes iteration of a time–step when required to provide solutions on the curves. Two time–step sizes are used in the program to permit events to be located to within the resolution of the small time–step. A technique is described for suppressing numerical oscillations in the solutions for currents in capacitive loops and voltages at inductive nodes. Modifications to the induction machine model are implemented in the prototype program in order to more accurately simulate the dynamics of self–excitation.

A control system for the apparatus was developed using the prototype simulation program. The control system is mainly feed–forward in nature but in-

cludes slower–acting feed–back control loops which provide correction of the feed–forward control error.

A test apparatus has been built and tested in the laboratory. The test apparatus includes a control system based on a digital signal processor. The apparatus is observed to operate generally as predicted by the electromagnetic transients simulation program. The apparatus operates well during both transient and steady–running conditions.

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List of Symbols

The following list contains symbols which are used frequently in the text. Other symbols which are rarely used in the text are defined where used.

α	the rectifier firing delay angle.
β	the voltage–boost converter duty–cycle order. The duty–cycle order describes the ordered fraction of the voltage–boost converter period during which the GTO device is turned off.
β^*	the signal describing the actual voltage–boost converter duty–cycle.
ρ	the angle of the main flux linkage vector with respect to the q–axis in the description of the induction machine.
ΔT	the duration of an integration time–step.
ϕ	the phase error signal produced by the phase comparator in the phase locked oscillator.
$[\lambda_{dq}]$	the vector of machine flux linkages in the dq model of the induction machine.
λ_d	the d–axis armature flux linkage in the induction machine model.
λ_{kd}	the d–axis amortisseur flux linkage in the induction machine model.
λ_q	the q–axis armature flux linkage in the induction machine model.
λ_{kq}	the q–axis amortisseur flux linkage in the induction machine model.
λ_{md}	the d–axis mutual flux linkage in the induction machine model.
λ_{mq}	the q–axis mutual flux linkage in the induction machine model.
λ_{sd}	the d–axis armature leakage flux linkage in the induction machine model.

λ_{rd} the d–axis rotor leakage flux linkage in the induction machine model.

λ_{sq} the q–axis armature leakage flux linkage in the induction machine model.

λ_{rq} the q–axis rotor leakage flux linkage in the induction machine model.

ν machine speed expressed generally in p.u. machine speed

θ the output angle from the phase locked oscillator. The phase locked oscillator tracks the positive–sequence fundamental–frequency (sine wave) component of the monitored three–phase voltages.

σ a complex number of magnitude 1 and angle 120°.

ω frequency expressed generally in radians per second.

B_t susceptance looking into the induction machine terminals.

C_s the capacitance of wye–connected self–excitation capacitors.

C_x the integrator gain in the Machine Voltage PI Control Loop.

C_y the proportional gain in the Machine Voltage PI Control Loop.

E(i) the current–dependant voltage source used in representing a device characteristic at a given device current.

f frequency expressed generally in p.u. frequency.

g the conductance of a given resistor.

[G] the conductance matrix used in the Dommel algorithm for nodal admittance circuit analysis.

$[G_{dq}]$ the machine generation matrix.

G_t conductance looking into the induction machine terminals.

i current

$[I]$ the vector of total current injection used in the Dommel algorithm for nodal admittance circuit analysis.

I_c the rms current in a wye–connected self–excitation capacitor

I_d the average dc current in the Graetz bridge rectifier.

I_d' the d–axis armature current in the induction machine model.

$[I_{dq}]$ the vector of machine winding currents in the dq model of the induction machine.

$I_d(ord)$ the final dc current order obtained by adding components of the order in the Rectifier Current Controller.

$I_d^*(ord)$ the basic dc current reference provided as output from the Look–up Tables.

$I_h(t-\Delta T)$ the history current term used as an injection in representing a particular branch in the Dommel algorithm for nodal admittance circuit analysis.

I_{kd} the d–axis amortisseur current in the induction machine model.

$I_{km}(t-\Delta T)$ the history current term used as an injection in representing a branch in the Dommel algorithm for nodal admittance circuit analysis.

I_q the q–axis armature current in the induction machine model.

I_{kq} the q–axis amortisseur current in the induction machine model.

I_L the dc current provided to the inverter or dc load.

I_{md} the d–axis magnetizing current causing the d–axis mutual flux linkage in the induction machine model.

I_{mq} the q–axis magnetizing current causing the q–axis mutual flux linkage in the induction machine model.

$I_{m'}$ the net vector of magnetizing current causing the main flux linkage in the induction machine model.

I_m the rms magnetizing current for the induction machine.

I_R the rms magnitude of the current into the Graetz bridge rectifier.

I_{react} the rms magnitude of the reactive current into the Graetz bridge rectifier.

I_{real} the rms magnitude of the real current into the Graetz bridge rectifier.

I_{XL} a constant magnitude of rms reactive current into the Graetz bridge rectifier.

K a constant.

K# gains in the control system where # equals 1 to 6.

K_I the integral gain in the phase locked oscillator.

K_p the proportional gain in the phase locked oscillator.

L an inductance.

L_c the inductance of the commutating inductors.

L_{inc} the incremental inductance at the operating point on the induction machine magnetizing curve. This represents the slope of a line which is tangent to the curve.

L_{inst} the instantaneous inductance of the induction machine magnetizing curve at the operating point. This represents the slope of a line which passes through the origin and the operating point.

L_{md} the inductance of the d–axis mutual flux linkage in the induction machine model.

L_{mq} the inductance of the q–axis mutual flux linkage in the induction machine model.

L_s the inductance of the armature leakage flux linkage for both the d and q axes in the induction machine model.

L_r the inductance of the rotor leakage flux linkage for both the d and q axes in the induction machine model.

$p(t)$ an independent time varying voltage source.

P_{base} the base power selected for the power transfer apparatus.

P_t the power out of the induction machine terminals.

p.u. per unit.

$R(i)$ the current–dependant series resistance used in representing a device characteristic at a given device current.

R_c the equivalent commutation resistance.

$[R_{dq}]$ the winding resistance diagonal matrix used in the dq induction machine model.

R_I the resistance used to represent a device according to the linear part of a simple v–i characteristic curve for positive current.

R_{iron} the resistance used in the phasor equivalent circuit of the induction machine to represent the iron losses.

R_{off} the off resistance of a simple characteristic curve for a device.

R_r the rotor resistance used in the phasor equivalent circuit of the induction machine.

R_{rotor} the resistance used in the phasor equivalent circuit of the induction machine to represent the quantity R_r/s.

R_s the stator resistance used in the phasor equivalent circuit of the induction machine.

s the slip of the induction machine.

S_f the factor by which the resistance R(i) is allowed to change in one iteration of the electromagnetic transients simulation time–step.

$T_{\#}$ time constants in the control system where # equals 1 to 6.

T_{off} the time that the GTO device in the voltage–boost converter is off during a period of the voltage–boost converter.

T_{vbc} the period of the voltage–boost converter.

T_w the time constant of the low–pass real–pole filter in the phase locked oscillator.

T_x the time constant of the low–pass real–pole filter which filters the magnitude of the ac load voltage in the ac Load Voltage PI Controller.

T_y the time constant of the integrator in the ac Load Voltage PI Controller.

v a voltage.

V_α the α voltage produced in the abc to $\alpha\beta$ transform of input voltages in the phase locked oscillator.

V_β the β voltage produced in the abc to $\alpha\beta$ transform of input voltages in the phase locked oscillator.

[v(t)] the node voltage solution vector used in the Dommel algorithm for nodal admittance circuit analysis.

V_a an A–phase voltage.

V_a(load) the A–phase load voltage.

V_{ac}(load) the rms magnitude of the load voltage.

V_b a B–phase voltage.

V_b(load) the B–phase load voltage.

V_c a C–phase voltage.

V_{comp} the compensation voltage provided by the Voltage–boost Converter Controller to the Rectifier Current Controller. The signal represents the present value of the voltage at the load end of the dc inductor. The signal improves the speed with which the Rectifier Current Controller can respond to sudden changes in voltage which would affect the dc current.

V_c(load) the C–phase load voltage.

V_d the average dc output voltage of the rectifier.

V_d(adj) the component of the final dc voltage order in the Rectifier Current Controller which arises out of the dc current error.

V_d(ord) the final dc voltage order obtained by adding components of the order in the Rectifier Current Controller.

V_d*(ord) the basic dc voltage reference provided as output from the Look–up Tables.

V_{d0} the average dc output voltage of a Graetz bridge rectifier fired with zero firing delay angle and disregarding the commutation drop.

$[V_{dq}]$ the vector of voltages applied to the windings in the dq model of the induction machine.

V_g the airgap voltage in the phasor equivalent circuit of the induction machine.

V_I the voltage on the dc capacitor at the output of the voltage–boost converter. This voltage is used to supply the inverter in the full apparatus and to supply the dc load in the laboratory apparatus.

V_{Iref} the intermediate reference value produced by the ac Load Voltage PI Controller for the voltage on the dc capacitor which is located at the output of the voltage–boost converter.

V_{on} the radius of the arc that makes up part of the simple characteristic curve for a switching device. This voltage basically describes the forward voltage drop on the device.

V_m the rms magnitude of the machine terminal voltage.

V_{mref} the rated machine terminal voltage which is used as a reference in the apparatus.

V_t the rms magnitude of the machine terminal voltage.

V_+ the positive–sequence fundamental–frequency voltage component.

X_r the rotor leakage inductance used in the phasor equivalent circuit of the induction machine expressed in units of Ohms per p.u. frequency.

X_s the stator leakage inductance used in the phasor equivalent circuit of the induction machine expressed in units of Ohms per p.u. frequency.

X_m the magnetizing inductance used in the phasor equivalent circuit of the induction machine expressed in units of Ohms per p.u. frequency.

X_L the reactance of the commutation inductors expressed in units of Ohms per p.u. frequency.

Chapter One

Introduction

1.1 General Introduction

This thesis describes the development of an apparatus for supplying an isolated ac load from an induction generator operable at variable speed. The ac voltage supplied to the load is well regulated in frequency and magnitude.

Induction generators have certain advantageous features which promote their use. The main feature is that an induction machine can include a robust squirrel–cage rotor rather than a wound rotor. The use of the sturdy squirrel–cage rotor obviates the need for brushes and a separate source of dc excitation current which are required for a synchronous machine. Another advantage is that an induction generator typically has lower unit cost and maintenance costs than a synchronous generator.

In isolated operation, the excitation current for an induction generator can be supplied by capacitors connected at the terminals of the machine. Such a configuration is known as a self–excited induction generator. However, the output voltage and frequency of a self–excited induction generator are highly dependant on rotor speed, terminal capacitance and load [1,2,3]. Significant variation in either load or shaft speed during operation of the self–excited induction generator thus dictates the need for additional apparatus to control and condition the output. This thesis describes power electronic apparatus which provides the required control and conditioning.

1.2 Background and Scope of the Thesis

Considerable prior work has been done in researching the use of self–excited induction machines.

Several investigators have looked at supplying load directly from the three phase induction machine terminals [4,5,6,7]. In such a configuration frequency is regulated using precise machine speed control and voltage magnitude is regulated using an arrangement of switched capacitors [4,7] or a static compensator [4,5,6] for excitation control.

Alternatively several other investigators [8,9,10] have looked at supplying a dc load from the rectified output of a self–excited induction machine. These investigators relied on the reactive power absorbed by a Graetz bridge rectifier to help control machine voltage. However no mechanism remains for machine voltage control when dc load and thus the rectifier current go to zero. Furthermore these techniques can only regulate dc output voltage for narrow ranges of load resistance and machine speed.

Yet other investigators [11,12,13] have looked at asynchronously linking the output of a self–excited induction generator to an existing ac system through a dc link. These latter schemes are unable to supply isolated ac load.

This thesis develops apparatus as illustrated in Figure 1 for supplying isolated ac load from a self–excited induction generator through a dc link. A voltage–boost converter is used in the apparatus between the Graetz bridge rectifier and the voltage–sourced inverter. This arrangement of power equipment enables the apparatus to be designed for operation in a specified range of machine speed (e.g. 1.0 to 1.4 p.u. speed) with 0.0 to 1.0 p.u. load. In these operating ranges machine voltage is regulated to 1.0 p.u. and the output voltage is well–regulated in frequency and magnitude. In the event that the load requires regulated dc voltage rather than ac voltage then the supply can be provided directly from the regulated output of the voltage–boost converter. The controls which have been developed respond quickly and accurately to transient load conditions

including application and rejection of full load at any speed in the specified operating range. The controls have been experimentally tested for dc loads.

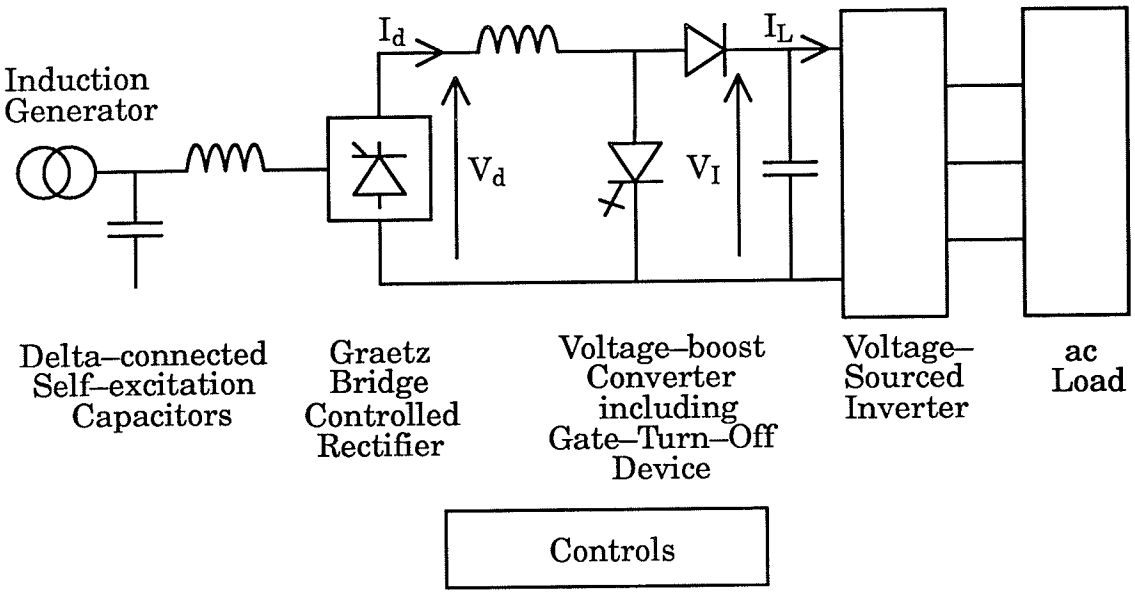


Figure 1 – Configuration of Developed Apparatus

1.3 The Choice of Apparatus Configuration

The apparatus is made up of four main power system components. They are, as illustrated in Figure 1, the induction generator; the Graetz bridge rectifier; the voltage–boost converter; and the voltage–sourced inverter.

Various authors [1,2] have listed the beneficial attributes of a squirrel–cage induction generator. The use of a squirrel–cage induction generator eliminates the need for slip rings and a separate source of dc excitation current which are required when a synchronous generator is used. Also unit costs and maintenance costs for induction generators are generally lower than those for synchronous generators.

In order to permit variable speed operation of the induction generator it is necessary to provide an asynchronous link between the generator and the load.

Provision of the dc link thus requires the selection of a suitable rectifier and inverter. The rectifier type is chosen to satisfy the requirements of operating the induction generator. The self–excitation capacitors on the terminals of the induction generator provide excitation current for the machine. However, at higher speeds these capacitors provide more VARS (volt–amperes reactive power) than the machine requires for operation at 1 p.u. terminal voltage. The rectifier in the apparatus is required to absorb the excess reactive power. The rectifier must also absorb sufficient real power to supply the load. The need to simultaneously absorb certain levels of real and reactive power into the rectifier dictates that a rectifier should be chosen which permits control of the input power factor. The well–known controlled Graetz bridge rectifier has been chosen because it is a very simple bridge and because power factor control can be accomplished through control of the firing delay angle. The choice of inverter is based primarily on the need for acceptable transient response during complete rejection of the ac load. The selected voltage–sourced inverter can be modelled as a voltage source behind a reasonably small (e.g. 0.1 p.u.) reactance. Therefore rejection of the ac load will result in only small changes in the load voltage. The change is related to the on–load voltage drop across the inverter transformer reactance. A schematic for a six–pulse voltage–sourced inverter is illustrated in Figure 2.

The Graetz bridge rectifier is chosen to meet the needs of the self–excited induction generator and the voltage–sourced inverter is chosen to meet the needs of the ac load. However, the variable dc output voltage of the rectifier is not compatible for directly supplying the required relatively fixed dc voltage needed at the input of the voltage–sourced inverter. This is evident from a consideration of operation at light load. At light load the rectifier must absorb almost no real power from the induction machine while continuing to absorb reactive power to control the induction machine voltage. The rectifier must therefore be operated

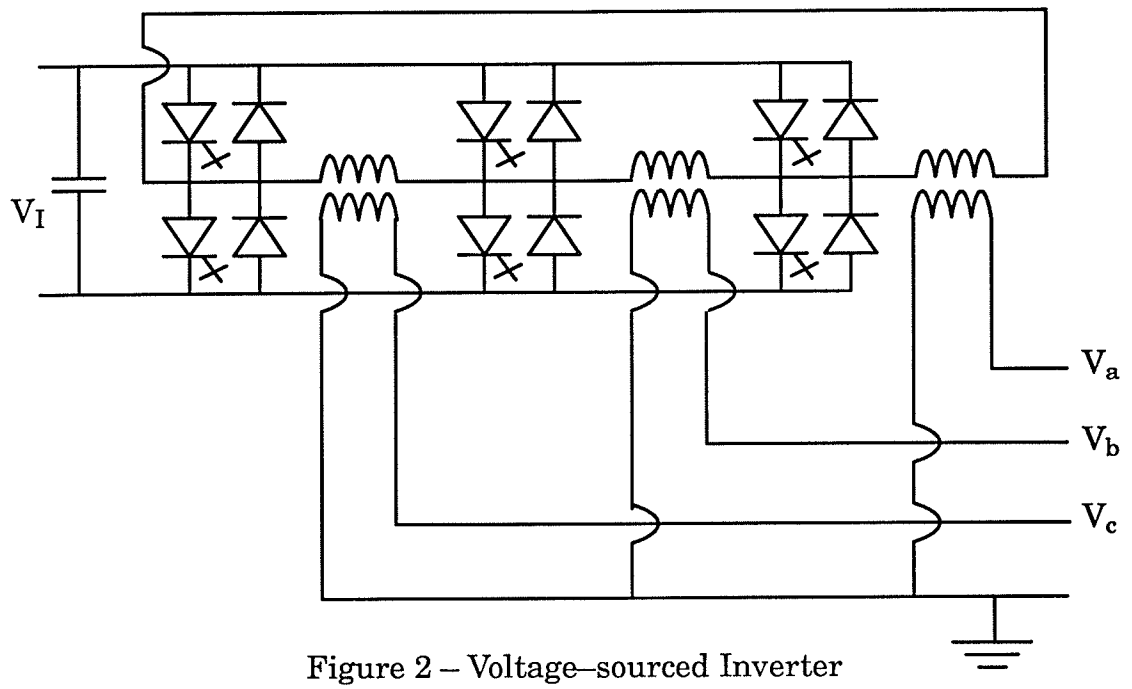


Figure 2 – Voltage–sourced Inverter

with a delay angle of approximately 90 ^{o} in order to have the proper power factor for absorbing the reactive power. Operation at approximately 90 ^{o} corresponds with almost zero average rectifier output voltage. The very low output voltage will not sustain current flowing from the output of the rectifier to the higher voltage on the capacitor at the input of the voltage–sourced inverter. Without the presence of rectifier current the rectifier cannot regulate the machine voltage and even the small ac load will not be supplied. It is therefore apparent that the output of the Graetz bridge rectifier cannot be directly connected to the input of the voltage–sourced inverter.

It is shown in this thesis that a voltage–boost converter can be successfully used as an interface between the output of the controlled Graetz bridge rectifier and the input to the voltage–sourced inverter. The voltage–boost converter operates properly only when it is called upon to boost voltage. The minimum reference level for the voltage on the capacitor at the input of voltage–sourced invert-

er is thus chosen to be higher than the maximum output of the rectifier for 1.0 p.u. machine voltage. A voltage–boost converter is illustrated in Figure 3.

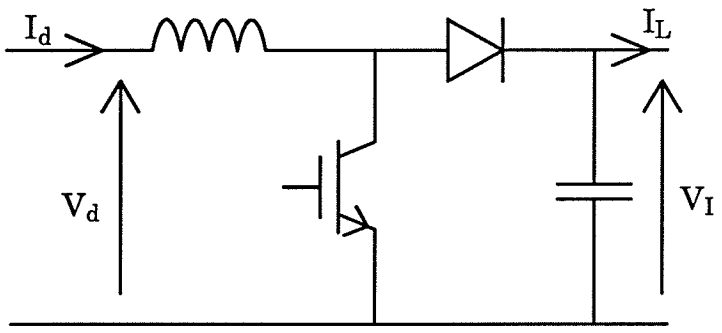


Figure 3 – Voltage–boost Converter

It will be noted that the voltage–boost converter is a simple apparatus which includes only one GTO (gate–turn–off) device and one diode device in addition to the dc smoothing inductor and dc smoothing capacitor normally used with the Graetz bridge rectifier and the voltage–sourced inverter. The symbol for the GTO device illustrated in Figure 3 is the symbol for the insulated gate bipolar transistor (IGBT) used in the experimental apparatus. In steady running the output voltage V_I of the voltage–boost converter is related to the average input voltage V_d according to $\frac{V_d}{V_I} = \beta$ where duty cycle β is the fraction of the period of the GTO device during which the device is "off". Controls are developed in this thesis which simultaneously control the duty–cycle order to the voltage–boost converter and the delay angle order to the rectifier so as to provide acceptable steady running and transient operation.

1.4 Outline of the Thesis

The thesis contains seven chapters.

The first chapter provides a brief description of the apparatus and techniques used by earlier investigators and then proceeds to give a brief description of the apparatus which has been developed in the thesis. The choice of converters in the apparatus is explained.

The second chapter describes a non–linear search technique for producing characteristic curves descriptive of operation of the apparatus with the induction machine voltage regulated to 1.0 p.u. voltage. Curves are produced for machine speeds between 0.95 and 1.6 p.u. speed and for load power between 0.0 and 1.0 p.u. power. These curves disclose the steady operating characteristics of the apparatus. Characteristic curves for average rectifier output voltage V_d and current I_d are used as a model in a feed–forward control system described later in this thesis. The feed–forward control system is supplemented by feed–back control loops to correct for small errors between the model and the real system.

The third chapter describes simulation techniques which have been implemented in a prototype transients simulation program written as part of the thesis work. The program is particularly adapted to the simulation of GTO and other power–electronic devices at a system level. Two time–step sizes are used in the program. Individual switching devices are represented according to simple characteristic curves. The modified algorithm includes iteration of a time–step when required to provide solutions on the curves. A technique is described for suppressing numerical oscillations in solutions for currents in capacitive loops and for voltages at inductive nodes. Nodes are termed inductive nodes when the incident branches are inductive. A brief description is given of an improvement in the transients simulation modelling of saturation of the main flux path in an

induction machine. The improvement in representation of saturation has also been developed by others [14]. The effectiveness of the improvement is demonstrated by comparison of simulation results to laboratory results.

The fourth chapter describes the development of a control system for coordinated control of the voltage–boost converter duty cycle and the controlled rectifier delay angle.

The fifth chapter presents simulation results which demonstrate the good steady running performance and transient response of the apparatus which is provided by the control system. The simulated disturbances include instantaneous full–load rejection. It is demonstrated through simulation that the output ac voltage of a twelve pulse voltage–sourced inverter can be filtered using a reasonable amount of filter apparatus so as to be acceptable for most loads.

The sixth chapter describes an experimental apparatus which has been built and tested in the laboratory to confirm the simulated operation of the apparatus. The apparatus includes a self–excited induction machine; a controlled Graetz bridge rectifier; a voltage–boost converter; a dc load; and a digital control system. The induction machine is a high power factor squirrel–cage induction motor described in Appendix I. A high power factor machine is used in order to keep the required self–excitation capacitors as small as possible. The reduced capacitor size reduces the level of excess VARS produced during high speed operation. This in turn reduces the current ratings of the rectifier; the dc smoothing inductor; and the voltage–boost converter. The voltage–boost converter includes a 50 Amp 1000 Volt IGBT (insulated gate bipolar transistor). An IGBT gate firing card including fibre optic isolation was designed and built as part of the thesis work. The digital control system is based on a 33 MHz Texas Instruments TMS320C30 floating–point DSP (digital signal processor) chip. The control sys-

tem was also designed, built, and programmed by the author. The transient responses observed in the laboratory generally correlate well with the responses predicted by transients simulation. Minor differences between simulated and actual responses are discussed and explained.

Chapter seven presents conclusions and contributions from the work.

Chapter Two

Steady–state Characterization of the Apparatus

2.1 Description of the Steady State Characterization

Certain data must be calculated using a steady state equivalent circuit of the induction machine prior to building the apparatus illustrated in Figure 1. Different models of induction machines have different saturation curves. Therefore, it will be necessary to calculate the capacitance of the self–excitation capacitors C_S whenever a different machine is included in the apparatus design. This chapter describes a method for the calculation of capacitance C_S. In addition, the apparatus design must enable operation of the apparatus within specific ranges of machine speed and output power. Therefore, for any permitted combination of speed and load, it is useful to know the values of average rectifier voltage V_d and current I_d which will supply the load power and properly regulate the machine voltage. This chapter describes a method for calculating curves of V_d and I_d required for specified ranges of machine speed and load power. Curves for the test apparatus are illustrated in Figures 7 and 8.

A non–linear search procedure for obtaining curves which characterize the operation of the self–excited induction machine at 1.0 p.u. voltage is described in section 2.3. The characterization of the induction machine enables the calculation of required capacitance C_S and the curves of V_d and I_d described above. The curves of V_d and I_d are ultimately used as a model in the feed–forward part of a control system described in chapter 4.

A choice has been made to operate the machine at constant 1.0 p.u. terminal voltage during variations in speed rather than operate at constant flux. This is beneficial because it eliminates continuous overvoltage on stator insulation at

high speed. It also is suitable because it was decided to generate the same maximum power at maximum speed as can be generated at minimum speed. The output power capability remains essentially constant at 1.0 p.u. machine voltage with an increase in speed because the speed increase balances the decrease in the maximum possible torque which is associated with reduced flux due to operation at constant machine voltage and increased frequency.

2.2 The Steady–State Equivalent Circuit for the Induction Machine

Earlier investigators [1,2] have confirmed the acceptability of a steady–state equivalent circuit representation of the induction machine. The equivalent circuit is illustrated in Figure 4.

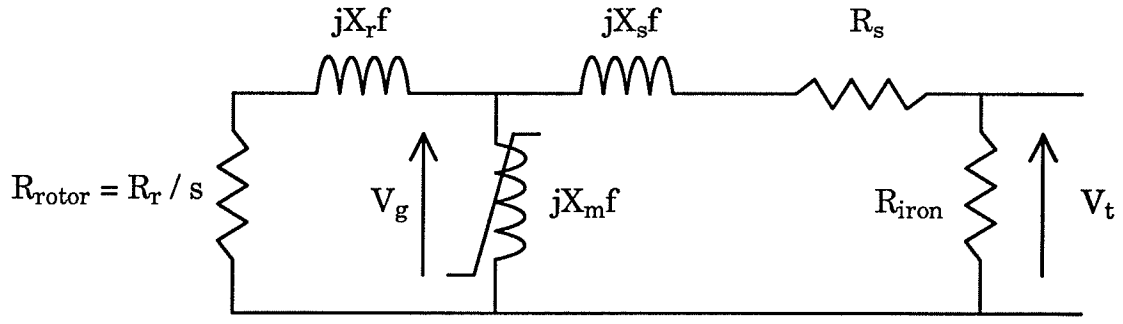


Figure 4 – Induction Machine Equivalent Circuit

In order to slightly improve the accuracy of the model, a representation of iron losses has been added through the inclusion of the iron–loss resistor at the terminals of the equivalent circuit. The iron–loss resistor was included at the terminals of the machine rather than at the magnetizing branch because of convenience of modelling. Positioning the iron–loss resistance on the terminal side of the stator leakage impedance rather than parallel to the magnetizing branch typically will not cause significant error in simulating a self–excited induction machine because R_{rotor}, X_m, and R_{iron} are typically much larger in magnitude

than R_s and X_s. The iron loss resistance appropriate for the machine described in Appendix I is R_{iron} = 32.3 p.u.

In Figure 4, the reactances X_m, X_r, and X_s are descriptive of reactance at 1 p.u. frequency. Therefore, as illustrated in Figure 4, it is necessary to multiply these reactances by p.u. frequency "f" in order to obtain true reactances at frequencies other than 1.0 p.u. frequency. In accordance with existing practise [1,2], the relation between air–gap voltage and magnetizing reactance is expressed according to a curve $\frac{V_g}{f}$ versus X_m. The curve for the test machine, based on the data in Appendix I, is illustrated in Figure 5. This curve is used in the non–linear search procedure to include the effect of saturation of the main flux path.

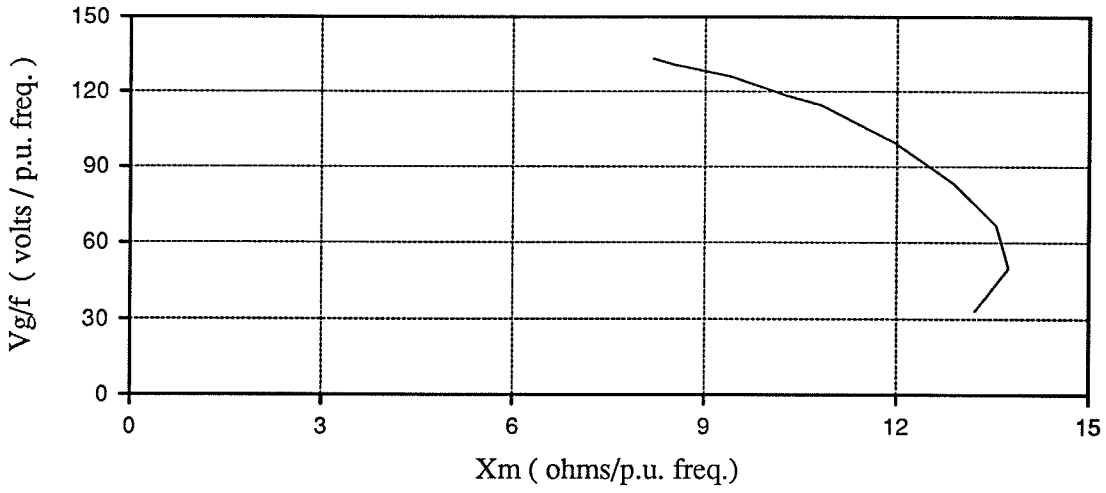


Figure 5 – V_g/f versus Xm Saturation Curve

2.3 The Non–linear Search Procedure

In order to characterize the operation of the overall apparatus shown in Figure 1, it is first necessary to characterize the operation of the machine at 1.0 p.u. voltage over the speed and power ranges of interest. Characterization of the machine allows selection of the size of the self–excitation capacitors (section 2.4)

and generation of curves of I_d and V_d in Figures 7 and 8 descriptive of the operation of the overall apparatus (section 2.5).

The objective of this section is to provide a method of characterizing the operation of the induction machine alone at 1.0 p.u. voltage over the desired operating ranges of machine speed and load power. A non–linear search procedure has been developed to provide a solution for slip s; frequency f; saturated magnetizing impedance X_m; admittance looking into the machine terminals $G_t + jB_t$; and current (real and reactive) into the machine for a given combination of output power P_t and speed ν. In order to characterize the machine for the speed and power ranges of interest, the non–linear search procedure was conducted at 45 combinations of output power and machine speed to determine the steady–state operating characteristics of the machine. However, for the purposes of explaining the search procedure, it is sufficient to describe the procedure for finding a single steady–state solution at a given machine speed ν and output power P_t.

It is necessary first of all to select the search variables for the search procedure. The terminal voltage V_t and the real power P_t out of the machine represented in Figure 4 are dependant solely upon the saturation X_m and the frequency f for a given machine speed ν. The effective rotor resistance R_{rotor} (R_{rotor} is equal to $R_r / s.$) is related directly to frequency "f" at a given speed ν because slip s is equal to $(1 - \nu / f)$. In addition, the dependence of air–gap voltage V_g upon X_m and f according to the curve in Figure 5 can alternatively be treated as a dependence upon X_m and R_{rotor}. It is therefore possible to use X_m and R_{rotor} as the search variables rather than X_m and f.

The objective is to search over X_m and R_{rotor} until $V_t = 1.0$ p.u. and the desired power P_t is obtained at the given speed ν. However, the objective P_t can be transformed into a more convenient form. At the solution point (X_m,R_{rotor}) the voltage

V_t will be equal to 1 p.u. and therefore the desired power P_t at the solution point can be transformed into a desired conductance G_t looking into the terminals of the machine.

The search is thus carried out over R_{rotor} and X_m and the objective is to obtain both V_t equal to 1.0 p.u. voltage and the desired conductance G_t looking into the machine terminals. However it is useful to note that terminal conductance G_t is strongly dependant on R_{rotor} and only weakly dependant on X_m. Conversely, terminal voltage V_t is strongly dependant on saturation in X_m and only weakly dependant on R_{rotor}.

The strong dependance of V_t on X_m and the strong dependance of G_t on R_{rotor} forms the basis for the selection of the search routine. The search routine begins with an initial estimate of R_{rotor} and X_m. R_{rotor} is then searched until G_t is at the desired value. A single change to X_m is then made to improve V_t. The change in X_m is followed by a search of R_{rotor} to again bring G_t to the desired value. The pattern of single changes to X_m each followed by a search of R_{rotor} is repeated until X_m has been searched and both V_t and G_t are at their desired values. In the case of V_t the desired value is always 1 p.u. voltage. The weak dependance of G_t on X_m and the weak dependance of V_t on R_{rotor} assures that convergence occurs quite rapidly.

Sufficiently accurate initial estimates for R_{rotor} and X_m can be obtained by ignoring R_s, X_s, and X_r in Figure 4. In that case, R_{rotor} can be estimated from $(1 / R_{rotor}) = (G_t - 1 / R_{iron})$. The estimate of R_{rotor} allows an estimate of slip s to be calculated from $R_{rotor} = R_r / s$. An estimate for slip at a given speed v allows an estimate of frequency f to be calculated. Ignoring stator inductance X_s and resistance R_s indicates that air–gap voltage V_g should be estimated as $V_g = V_t = 1.0$ p.u. Finally, the estimates for V_g and f allow an estimate of X_m from the

V_g / f versus X_m curve in Figure 5. In this manner, adequate initial estimates for R_{rotor} and X_m can be obtained.

The non–linear search procedure was conducted at nine values of power between 0 and 1 p.u. power for each of five different values of machine speed v between 0.95 and 1.6 p.u. speed. For each combination of P_t and v, a record was made of the solution for s, f, X_m, G_t, susceptance B_t, and current (real and reactive) into the machine. By this method a record was made of the operating characteristics of the machine at 1.0 p.u. voltage for the speed and power ranges of interest. The solution for the 45 combinations of v and P_t required a few minutes of computer time.

2.4 Calculation of the Required Self–excitation Capacitance

The self–excitation capacitors must produce reactive current sufficient to supply the needs of the induction machine and the rectifier. In determining the capacitance C_S, for operation of the machine at 1.0 p.u. voltage, it is necessary to note that the maximum reactive power is absorbed by the machine when it is operated at the minimum machine speed and the maximum load. Furthermore, operation of the machine at minimum speed and 1.0 p.u. load causes operation at the minimum frequency f . Operation at the minimum frequency f causes the minimum reactive power to be produced by the self–excitation capacitors at 1 p.u. voltage. Operation at minimum speed and maximum power therefore represents the case that determines a lower limit for the capacitance C_S of the self–excitation capacitors.

As noted above, the self–excitation capacitors must provide the reactive current for both the rectifier and the machine. The non–linear search procedure described in section 2.3 gives the reactive current absorbed by the machine at all speeds and output powers of interest at V_t = 1.0 p.u. voltage. This section de-

scribes the calculation of the reactive current absorbed by the rectifier at minimum speed and maximum load. Determination of the reactive current absorbed by the machine and rectifier leads directly to the calculation of the required capacitance C_S of the self–excitation capacitors..

The rectifier should be forced to absorb as little reactive power as possible at minimum speed and maximum load so that the capacitance C_S can be kept to a minimum. Maximum loading dictates that the rectifier must simultaneously absorb 1.0 p.u. real power. Therefore, at minimum speed and maximum load, the rectifier should be operated at minimum delay angle α (e.g. $\alpha = 5^{\circ}$) so that the power factor of the current into the rectifier can be maintained as high as possible.

With reference to Figure 6, several quantities are known for the purpose of selecting the self–excitation capacitors. The ac machine voltage V_t is 1.0 p.u. voltage. The commutation reactance X_L (defined at 1 p.u. frequency) is a physical parameter which is known. The frequency f for steady–state operation at minimum speed (i.e. 0.95 p.u. speed) and maximum power (i.e. 1.0 p.u. power) was found during the non–linear search procedure described in section 2.3. The delay angle α should be minimum (e.g. $\alpha = 5^{\circ}$). In addition, the product of V_d and I_d is 1.0 p.u. power for purposes of selecting capacitance C_S.

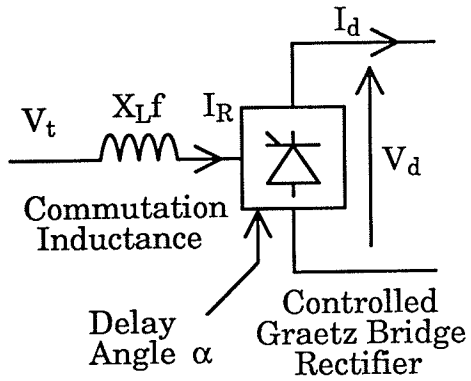


Figure 6 – Controlled Graetz Bridge Rectifier

In the analysis of the Graetz bridge rectifier it is often assumed that the commutation reactance and the bridge are lossless. Based on that assumption, standard approximate equations [15] are available with respect to the circuit in Figure 6. They are as follows:

$$V_d = V_{d0} \cos\alpha - R_c\ I_d \qquad \text{Eqn. 1}$$

$$V_{d0} = \frac{3\sqrt{6}\,V_t\ (\ rms\ )}{\pi} \qquad \text{Eqn. 2}$$

$$R_c = \frac{3\ f\ X_L}{\pi} \qquad \text{Eqn. 3}$$

Multiplying both sides of Eqn. 1 by I_d gives:

$$V_d\ I_d = V_{d0}\ I_d\ \cos\alpha - R_c\ {I_d}^2 \qquad \text{Eqn. 4}$$

A review of the list of known quantities (V_t, X_L, f, α, and $P_d = V_d I_d$) described above reveals that the only unknown quantity in Eqn. 4 is I_d. Thus the dc current I_d at minimum speed and maximum power can be obtained by solving for I_d in Eqn. 4. Eqn. 4 is in quadratic form and therefore the solution is

$$I_d = \frac{K_B - \sqrt{{K_B}^2 - \frac{4P_d}{R_c}}}{2}$$

$$\text{where} \quad K_B = \frac{V_{d0}\ \cos\alpha}{R_c} \qquad \text{Eqn. 5}$$

The magnitude of the ac current I_R into the rectifier for the selection of the self–excitation capacitor can subsequently be found using the following approximate [15] equation with reference to Figure 6:

$$I_R\ (\ rms\ ) = \frac{\sqrt{6}\ I_d}{\pi} \qquad \text{Eqn. 6}$$

The real component of current into the rectifier is given by the equation $I_{real} = P_t / (3\ V_t)$. Finally the reactive power into the rectifier for selecting the capacitors is obtained using

$$I_{react} = \sqrt{I_R{}^2 - I_{real}{}^2} \qquad \text{Eqn. 7}$$

The reactive current into the machine at minimum speed and maximum power (from section 2.3) can be added to the reactive current into the rectifier to give the total reactive current I_C that the self–excitation capacitors must provide at minimum speed and maximum load.

The final step in determining capacitance C_S is accomplished by using I_C obtained as described above; the p.u. frequency f at minimum speed and maximum power obtained as described in section 2.3; and recalling that V_t is equal to 1.0 p.u. voltage. The appropriate equation is $C_S = | I_C | / (2\pi f V_t)$.

2.5 Obtaining Characteristic Curves for Operation of the Apparatus

The complex current into the rectifier is the sum of the complex currents out of the machine and the self–excitation capacitors. Section 2.3 describes a method for obtaining the frequency f and the induction machine current (real and reactive) for combinations of speed v and power P_t at 1.0 p.u. machine voltage. Section 2.4 describes the method for determining the required capacitance C_S for the self–excitation capacitors. Given f and C_S, the reactive current I_C produced by the self–excitation capacitors is thus also readily obtained for the al-

lowable combinations of speed and power at $V_t = 1.0$ p.u. voltage. Consequently, the real and reactive currents into the rectifier and the corresponding magnitudes I_R of the ac current can be obtained for the allowable combinations of speed and power.

The magnitude of ac current I_R into the rectifier approximately determines I_d according to Eqn. 6. Rectifier output voltage V_d for a given power P_d is then available from $V_d = P_d / I_d$. Families of curves describing required I_d and V_d as functions of speed v and power P_d are presented in Figures 7 and 8 respectively. At a given speed and power both I_d and V_d must be at approximately the values indicated in the curves in order to regulate the machine voltage to the proper level and to cause the correct power to be delivered.

The capacitance C_S and the curves in Figures 7 and 8 are sufficient for the design of the apparatus and control system as described in chapter 4.

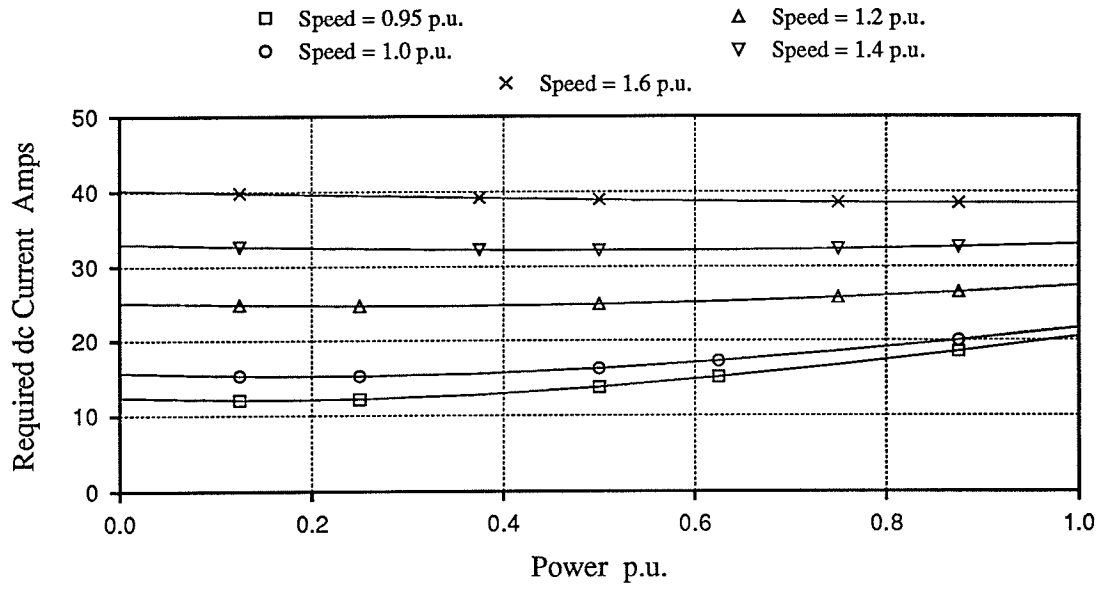


Figure 7 - Required Rectifier Operating Current I_d*(ord)

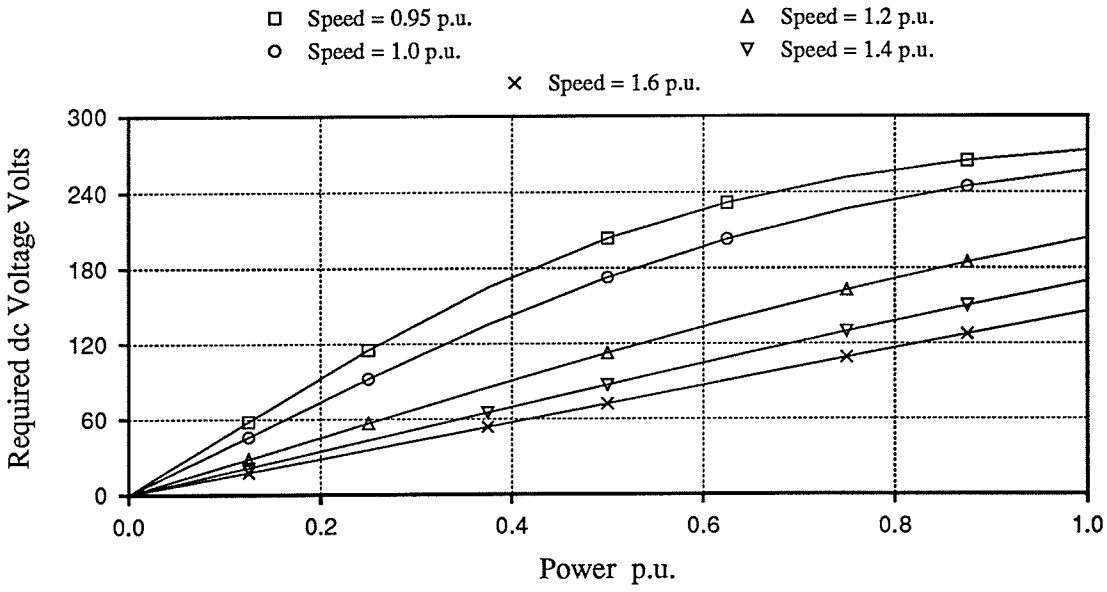


Figure 8 - Required Rectifier Operating Voltage V_d*(ord)

Chapter Three

Transients Simulation Techniques for Power Electronic Apparatus

3.1 Outline of the Chapter

This chapter describes special modifications for adapting a transients simulation program based on the trapezoidal algorithm of Dommel [16]. The modifications facilitate the simulation of systems which include arbitrarily specified configurations of power–electronic switching devices such as diodes, thyristors, and GTO devices.

The modifications are based on three techniques. The three techniques when combined in the simulation program result in shortened preparation time for simulating new power electronic apparatus. In addition, the techniques remove certain difficulties normally encountered in simulating switching events. A technique is described for representing devices according to simple characteristic curves. This approach provides for automatic coordination in the switching of devices which are in close proximity in the simulated circuit. A technique of using two time–step sizes provides benefits which will be described. In addition, a technique is described for modifying the normal trapezoidal algorithm to remove certain numerical oscillations from solutions.

An improved method is briefly described for representing saturation of the main flux path in an induction machine in a transients simulation program. The improvement in representing saturation has also been developed by other investigators [14].

3.2 Motivating Factors for Modification of the Transients Simulation Algorithm

It was found necessary, as part of the thesis work, to investigate some new and unusual configurations of power–electronic devices arranged as components in power system apparatus. However, difficulties were encountered in attempting to simulate the new arrangements of power electronic devices using existing techniques. This led to the development of novel modifications to the simulation algorithm particularly suited to facilitating simulation of novel power electronic apparatus.

Traditionally, the trapezoidal algorithm of Dommel [16] has been used for the simulation of power system transients. A primary feature of the Dommel algorithm is that a computer program can readily be prepared to automatically formulate the admittance matrix used in the solution method. Also of note is the ease with which travelling–wave transmission line models [16] and machine models can be interfaced to the main network solution [17]. These features make the Dommel algorithm the method of choice when simulating large electrical power systems.

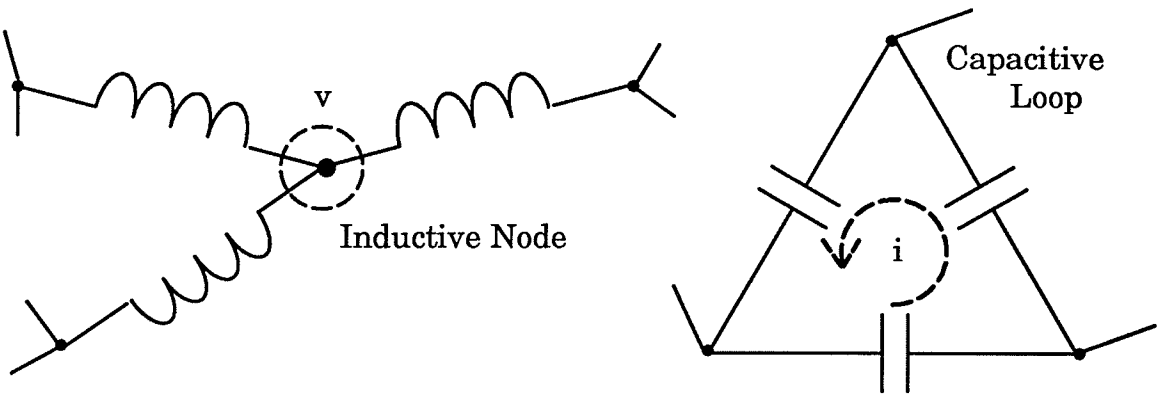


Figure 9. Inductive Nodes and Capacitive Loops

There are of course limitations to any numerical method. One limitation of this type of nodal admittance matrix analysis becomes apparent when the network to be simulated contains capacitive loops or nodes which are connected to the rest of the network only through inductive branches as illustrated in Figure 9. In the case of capacitive loops a numerical oscillation of two time–step period can arise in the solution for currents in the capacitive loop. A similar numerical error can appear in the voltage solution for inductive nodes at which only inductors are incident [18]. The oscillations often arise at discontinuities in the solutions which in turn occur because of device switchings.

One technique available to reduce these numerical oscillations is to make slight changes to the resistive nature of the network in question in order to damp out the oscillations. However, this method of adding small resistances does have an effect on the accuracy of the solution. If fast damping of the numerical oscillations is desired then the damping resistances can have a significant effect on solution accuracy.

Another technique for suppressing numerical oscillations involves making a temporary modification to the solution technique when numerical oscillations arise [18][19][20][21]. The temporary modification includes using the results of a half–size time–step based on the backward Euler method [18]. The half–size time–step is taken following a discontinuity in the solution such as can be expected when a switch operates. The time–step length for the backward Euler method is advantageously chosen to be equal to one–half that for the trapezoidal rule because then the same conductance matrix can be used [18].

A modification to the solution technique is described in this chapter which allows for the continuous use of the trapezoidal rule but which also eliminates numerical oscillations. The trapezoidal algorithm is used exclusively for the de-

scribed solution technique because it it known to be more accurate than the backward Euler method [18]. The more accurate trapezoidal algorithm is employed in the described solution technique because the oscillation suppression technique is used in every time–step rather than only at expected discontinuities.

Special care is required when simulating the switching of devices such as GTO (gate–turn–off) thyristors or IGBT (insulated gate bipolar transistor) devices in a power system electromagnetic transients simulation program. A GTO, for example, can be ordered to turn off when still carrying full load current which is not the case with conventional thyristors. Also, the coordinated switching of two devices in close proximity that are made to switch in the same time interval (a common occurrence in several power–electronic circuit topologies) is difficult to handle when devices are represented as controlled on–off switches as is the practise in most power system simulation packages in use today. To handle such situations two basic modifications to the traditional Dommel algorithm are implemented in the prototype program which has been used for the thesis work.

Firstly, the device characteristic is represented as a simple v–i characteristic curve and not as a resistance changed in one abrupt on–off step. In the case of diodes the characteristic curve is fixed. However, for GTOs and thyristors there are two characteristic curves, one being for the blocked state and the other being for the forward conducting state. The main intention here is not to represent the characteristic accurately but to improve the numerical performance of the program when devices in close proximity are switched simultaneously. Iteration of the solution within the same time–step is carried out to ensure that the solution always falls on the v–i characteristic. However the program has an automatic selection criterion that only iterates the solution when required and no iteration takes place in the period between device switchings.

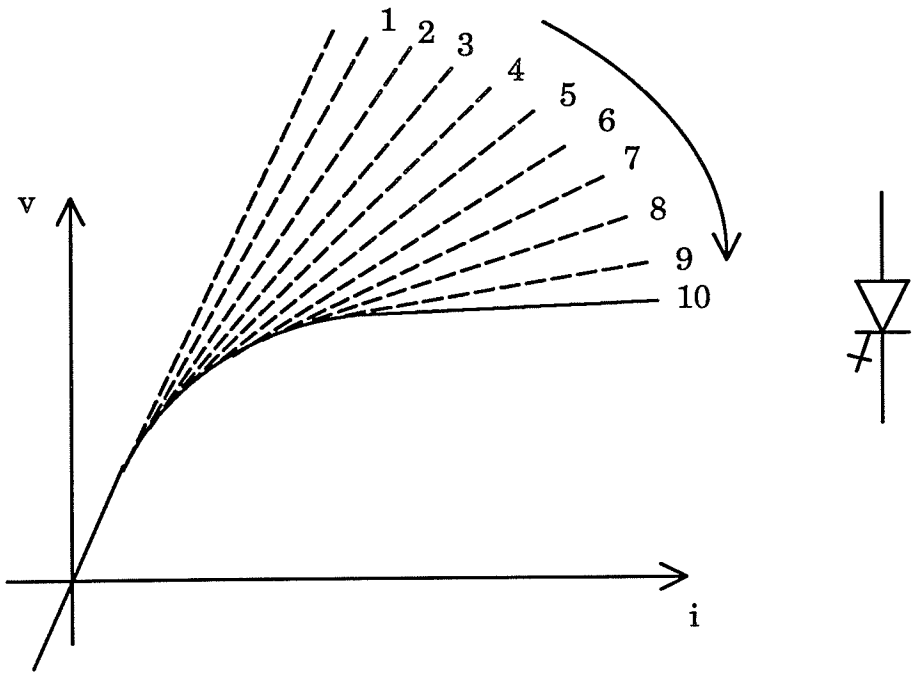


Figure 10. Modifying a Device Characteristic Using Small Time–steps

Secondly, the program permits the use of two time–step sizes during a simulation. A specifiable large time–step size is the default. However, when it is necessary to change the characteristic for a device between the "on" and "off" characteristics as illustrated in Figure 10 then the change can be carried out gradually during a sequence of small time–steps.

3.3 Representation of Switching Devices in the Prototype Program

In developing the prototype program a number of levels of complexity were available for consideration with respect to the representation of device switching.

At the lowest level of complexity is what will be referred to as a binary type switching. In binary switching a diode branch is represented by a simple resistor which is given a high resistance in the next time–step following the detection of $i \leq 0$ and is given a low resistance in the next time–step following detection

of i > 0. For thyristors, the change to a low resistance is delayed until there are both a small forward current and an "on" pulse at (t–ΔT), the beginning of the time–step. Such "binary" switching is prone to errors when simulating arbitrary power–electronic topologies. In the prototype program an alternative "iterative" approach is used as described below.

Each switching device such as a diode, thyristor, or gate–turn–off (GTO) device is represented in the network by a resistance R and a series voltage source E. As illustrated in Figure 11, the voltage source E and resistance R translate into a straight line segment in the v–i plane with slope R and voltage axis intercept E. The values of R and E are changed with the current i through the device in order to cause the device to be represented according to a simple characteristic curve such as the solid curve illustrated in Figure 11. In particular, when it is necessary to represent the characteristic curve at a given current i, then the values of E and R are chosen to cause the line segment to be tangent to the characteristic curve at the current i.

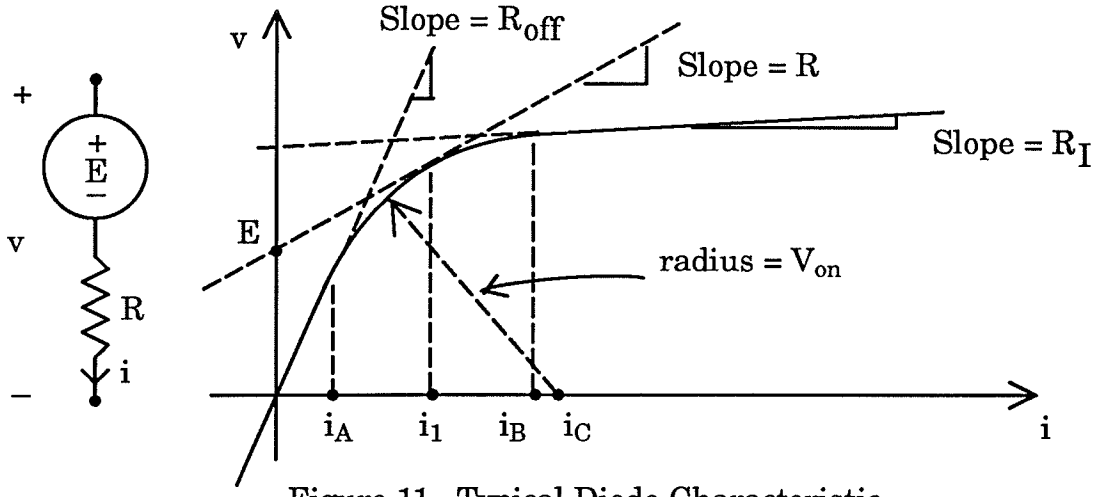


Figure 11. Typical Diode Characteristic

The characteristic illustrated in Figure 11 consists of two straight line segments which are tangent to an arc of a circle. The line segment extending into

quadrant III with slope R_{off} represents the reverse–voltage blocking state of the device. The slope R_I of the line segment in quadrant I can be set to a small value to represent the loss of forward blocking capability. Conversely, slope R_I can be adjusted gradually toward slope R_{off} to represent the recovery of forward blocking capability for a thyristor.

In order to represent the characteristic properly for a given current such as i_1 in Figure 11 it is necessary to be able to obtain voltage source E and slope R as functions of the device current i. Equations for E(i) and R(i) are readily derived using basic trigonometry for characteristic curves specified in terms of R_{off}, R_I, and V_{on} defined in Figure 11. The relevant equations are given in Appendix II. The curved portion of the characteristic between i_A and i_B in Figure 11 is referred to as the switching zone because changes to E and R are required only within this zone in order to properly represent the characteristic for varying i.

The iterative aspect of the switching algorithm is described below with reference to Figure 12.

It is assumed that i_1 in Figure 12 is the solution for a device current at the beginning of a time–step during the switching of the device. The solution for the end of the time–step (i_S, v_S) (i.e. point X in Figure 12) is first computed representing the device as a resistance R(i) and series voltage source E(i) evaluated with $i = i_1$. However, the solution (i_S, v_S) (i.e. point X) is not on the actual characteristic. Solution (i_S, v_S) may still be acceptable if the ratio $R(i_S)/R(i_1)$ is not too different from unity. A ratio close to unity (e.g. $0.33 < \text{ratio} < 3.0$) indicates that the solution is not far off the characteristic. If the solution is unacceptable then the equivalent branch parameters R and E are changed to $R(i_R)$ and $E(i_R)$ where $i_R = (i_1 + i_S)/2$. This represents picking the tangent point of the line segment (defined by E and R) on the characteristic curve for the next itera-

tion to be one–half way on the current axis from the tangent point in the last iteration toward the

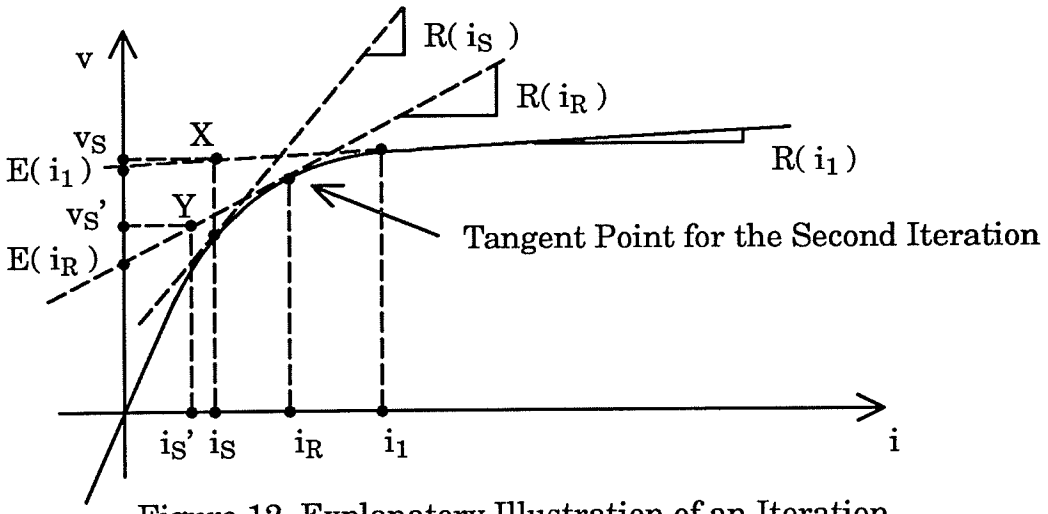


Figure 12. Explanatory Illustration of an Iteration

solution current in the last iteration. The value of i_S as the candidate end of time–step solution is discarded and new solution (i_S', v_S') (i.e. point Y) is calculated by repeating the simulation time–step from i_1. It can be noted from Figure 12 that (i_S', v_S') (i.e. point Y) now falls closer to the characteristic than (i_S, v_S) (i.e. point X). If the solution is still unacceptable a further iteration is conducted using R(i_R') and E(i_R') with $i_R' = (i_S' + i_R)/2$ in order to arrive at a new solution (i_S", v_S"). Iterations are continued until the attainment of the desired convergence criterion.

Under some circumstances, the tangent point for the next iteration (e.g. i_R) is not chosen to be midway between the tangent point and solution current from the last iteration (e.g. i_1 and i_S respectively) but rather closer to the tangent point from the last iteration (e.g. i_1). This is to ensure that the slope R of the tangent point is changed gently from iteration to iteration (e.g. slopes R(i_1) and R(i_R) at consecutive tangent points are not too different). Appendix II includes an equation defining the maximum movement of the tangent point

along the current axis in an iteration in order to limit the change in resistance R(i) to a specifiable factor S_f (e.g. $S_f = 3.0$). The limitation on the change in the tangent–point–current based on the specifiable slope factor S_f is applied in every iteration.

On rare occasions the tangent–point–current moves back and forth on the current axis during the iterations for a time–step. However, when reversals in search direction do occur for a device, the program counts the number of reversals and iteration for the device is terminated after a specifiable number of reversals. The permitted number of reversals is placed quite high (e.g. 8) so that this exit criterion for the search is rarely used (e.g. perhaps never in given simulation run). It is possible to use this exit criterion on the rare occasions when it is met because the solution is always acceptable. The solution is acceptable because a large number of reversals (e.g. 8) is seen to occur only when there are several reversals in consecutive iterations and because the change to R(i) permitted between consecutive iterations is limited according to the factor S_f. Under those circumstances R(i) will be correct to within the factor S_f.

This 'iterative' procedure is found to give accurate results in the modelling of device switching and particularly in the coordination of the characteristics of two devices switching simultaneously. A simple circuit is illustrated in Figure 13 to aid in the further explanation of the switching algorithm used in the program.

For the circuit in Figure 13, it is assumed that a simulation has been underway for a sufficient number of large time–steps with thyristor T1 blocked so that the current i_1 through diode D1 has become steady at 10 Amps. In the blocked state the thyristor has a characteristic curve with $R_I = R_{off}$ in Figure 11.

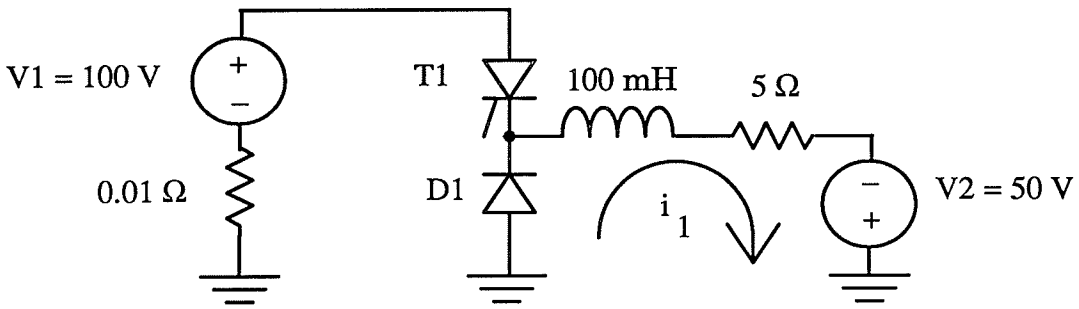


Figure 13. Circuit for Describing Switching Operation

At the end of each large (e.g. 50 μS) time–step the program checks to see whether a change in the characteristic of the thyristor has been signalled by controls in a user–supplied subroutine called DRIVER. When the main program receives a signal to change the thyristor characteristic to represent forward conduction, the main program can only tell that the switching was called for sometime in the large time–step. The program therefore takes action to identify the time of switching more precisely.

Upon receiving a signal to change the thyristor characteristic, the program rejects the results of a large time–step completely and resets the simulation to the condition that existed at the beginning of the rejected step. The simulation then proceeds with a scheduled number of small (e.g. 1 μS) time–steps in order to relocate the switching event. In this manner, the commencement of the "on" switching of the thyristor characteristic can be identified to within one small time–step.

Binary type switching as mentioned in the opening paragraph of this section does not work very well for circuits such as illustrated in Figure 13. It is assumed for demonstration purposes that a new "on" pulse for a blocked thyristor T1 appears while current i_1 is flowing through diode D1. In that circumstance, diode D1 will continue to be represented by a low resistance in the next time–step be-

cause $i_1 = 10.0$ Amps is flowing at $(t - \Delta T)$. As well, thyristor T1 will be switched to a low resistance for the time–step because of the existence of forward voltage and an "on" pulse at $(t - \Delta T)$. The result of this binary device logic is that both diode D1 and thyristor T1 will be represented by low resistances for the time–step and the solution at t will include an erroneous one time–step 10000 Amp spike of current backward through diode D1.

Of course, in a circuit as simple as that in Figure 13, it is very easy to devise overriding logic (referred to as circuit level logic) to cause the simulation to work properly. One only needs to note that as soon as thyristor T1 is turned "on" diode D1 needs to be turned "off". This circuit level logic can be arranged so that in the very same time–step that thyristor T1 is changed to a low–resistance representation, diode D1 can be changed to a high–resistance representation (even though at $(t - \Delta T)$ the current i_1 will still be forward through the diode). This logic arranged for switching diode D1 represents a case where circuit level logic needs to be given priority over device level binary logic in order to make the simulation work properly.

As noted above, circuit level logic is very readily devised for a circuit as simple as that shown in Figure 13. On the other hand, if the circuit for a simulation contains a large number of devices, then the circuit level logic required to make the simulation work properly could conceivably be very complex. It was therefore decided to provide more complex device logic in the program so that the user of the program would not need to implement any circuit level logic.

The erroneous result of the switching operation described in relation to Figure 13 is corrected without the use of circuit level logic when the iteration algorithm discussed above is employed. The erroneous current spike through diode D1 is still calculated at the end of the first solution of the time–step. However,

the solution is not accepted as final because iteration of the time–step is triggered by the diode D1. This iteration is triggered due to the fact that the representation of the diode characteristic during the time–step (i.e. a low resistance R) is clearly inappropriate with a large reverse current through the diode. Continuing iteration of the time–step occurs with adjustment of the diode resistance $R(i_R')$ and source voltage $E(i_R')$ until the characteristic is represented by a large R which is appropriate for a reverse biased diode. With a large R the current through the diode D1 will be correct at the end of the time–step. The currents through devices D1 and T1 in Figure 13 as computed using the prototype program are illustrated in Figure 14.

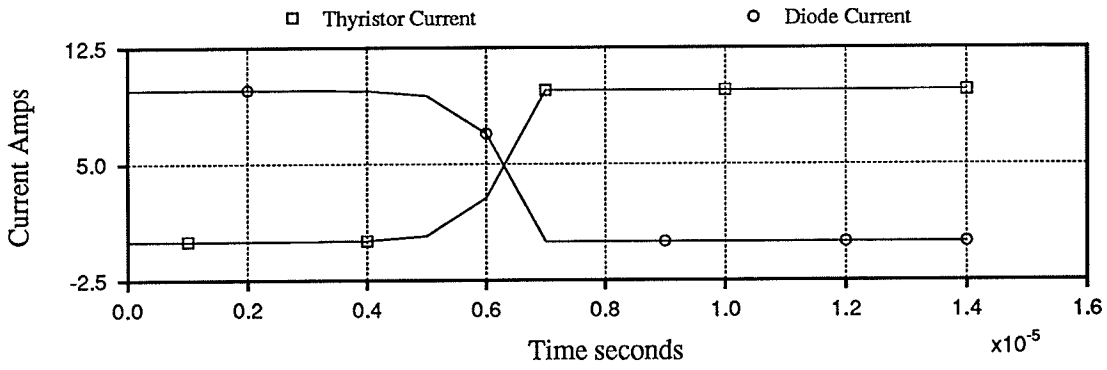


Figure 14. Device Currents During a Simple Switching Operation

A further enhancement used in the program involves extending the modification of device forward–resistance (R_I in Figure 11) over a sequence of small time–steps. For example, R_I can be decreased exponentially over 10 small time–steps to model the non–zero duration of the turn–on process as illustrated in Figure 10. Likewise, the turn–off process can be extended over 20 small time–steps to model a non–zero duration of the turn–off process. This method adds accuracy to the solution as is demonstrated by simulation of the example circuit

illustrated in Figure 15. Small time–steps rather than large are always used during modifications to device forward resistance R_I in order that the modification to the device characteristic is not extended over an unacceptably long time.

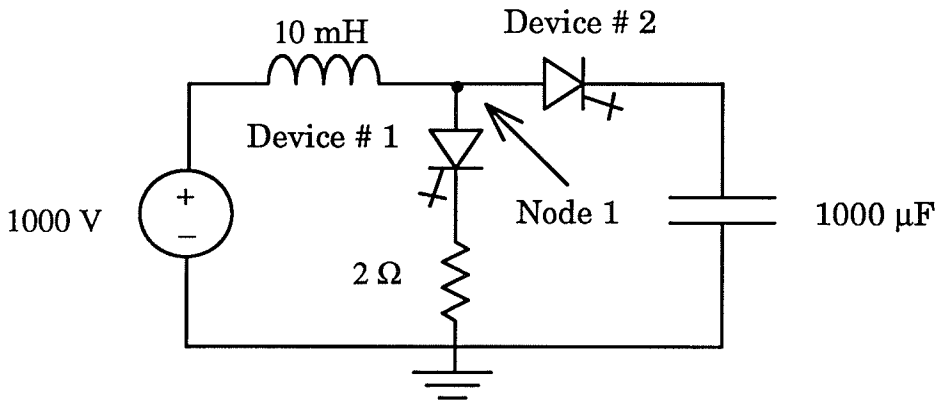


Figure 15. Circuit for Demonstrating GTO Device Turn–off Switching Operation

Figure 15 contains an example power–electronic circuit which contains two GTO devices. The circuit has been simulated in order to demonstrate the effectiveness of modifying forward–resistance R_I slowly over 20 small time–steps in order to simulate the turn–off of GTO devices. Both devices are initially "off" but are switched "on" at t = 0.05 seconds. By t = 0.35 seconds a current of 500 Amps is established in the 0.01 H inductor. The number of volt–seconds applied to the inductor in establishing the current is 5 Volt–seconds. Thus 5 Volt–seconds applied in the opposite direction is required to block the current.

When both GTO devices are turned "off" over 20 small time–steps a quasi–impulse of voltage is simulated at node 1 as illustrated in Figure 16. Integration of the impulse shows that the area under the impulse is approximately correct at 5.196 Volt–seconds. This accuracy is good given the ratio of event duration (essentially 10 μs) to small time step size (1 μs). The accuracy would not be

as good with a one time–step turn–off of the GTO devices. In fact, with a one–step turn–off the solution can be completely wrong. While practical GTO devices would certainly fail from the impulse plotted in Figure 16, the example does demonstrate the ability of the simulation method to handle unusual situations with accuracy.

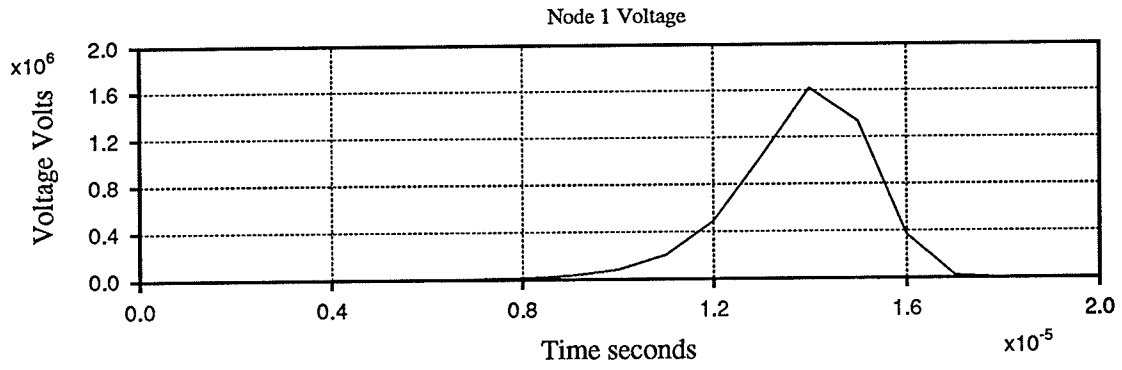


Figure 16. Node 1 Voltage Impulse for Figure 15 Circuit

For many simulation cases it is adequate to have an on/off binary representation for the switching device instead of using the characteristic curve to represent the device. The program allows for this simpler representation as well. Utilizing this feature often leads to a significant reduction in simulation time. Savings in simulation time of about 40% have been obtained in some simulations where the feature was used. The user can identify which devices can be modeled as binary switches and which devices require detailed representation. For instance, a Graetz bridge rectifier fed from a low impedance source and supplying a dc smoothing inductor might be modelled as binary switches because it's operation is well understood and it is somewhat isolated from fast transients in the remainder of the system. On the other hand, less well understood apparatus will often require representation of the devices according to the characteristic

curves. The use of two time–step sizes to accurately locate switching events is used whether devices are represented according to characteristic curves or as binary on/off switches.

3.4 Modification of the Conventional Algorithm for Suppression of Numerical Oscillations

The prototype program is based on the Dommel algorithm [16] for nodal–admittance circuit analysis.

In the Dommel [16] [22] algorithm, the branch equations for resistors, inductors and capacitors can be written in the form

$$i(\ t\ ) = g\ v(\ t\ ) + I_{km}(\ t - \Delta T\ ) \qquad \text{Eqn. 8}$$

by the application of the trapezoidal rule of integration. This form is clearly recognizable as a conductance and parallel current source as shown in Figure 17.

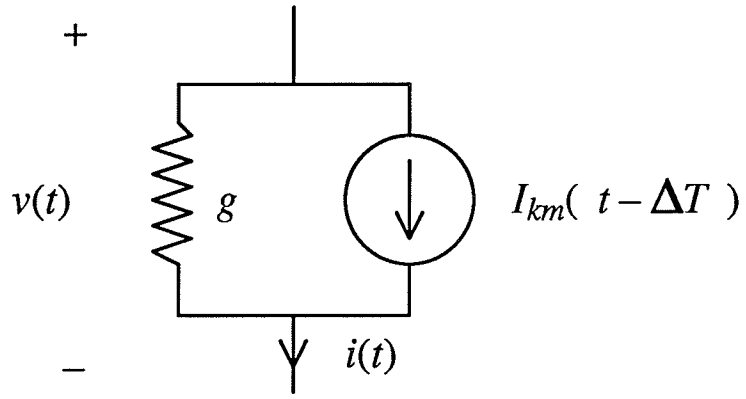


Figure 17. The Branch Equivalent in the Dommel Algorithm

Similar matrix equations can be developed for mutually coupled branches such as transformers and other elements such as transmission lines. Terms with the

suffix ($t-\Delta T$) represent (or are entirely derived from) branch voltages and currents known at the beginning of a time–step of duration ΔT. Node voltages at the end of a time–step from ($t-\Delta T$) to t are obtained by solving for the node voltages in a network consisting of conductances g and parallel current sources $I_{km}(t-\Delta T)$. The solution for the node voltages at t involves the solution of the matrix equation

$$[G] [v(t)] = [I] \qquad \text{Eqn. 9}$$

where [G] is the conductance matrix; [v(t)] is the vector of unknown voltages at t; and [I] is the vector of total current injections into each node. These injections include injections from machines or other state equation based models interfaced to the main network solution. [I] can also include terms corresponding to voltage and current sources defined for time t. Once node voltages v(t) are obtained, the application of Eqn. 8 for each branch will yield i(t), the branch currents at the end of the time–step.

In the conventional Dommel algorithm the solution at t is complete at this point and the solution of the next time–step can begin. However, this chapter describes a modification which can be implemented in order to eliminate the two time–step numerical oscillations which are sometimes observed in the pure Dommel algorithm for capacitive loops and inductive nodes [18]. This technique for suppression of numerical oscillations consists of additional action at the end of the conventional time–step described above.

The first prescribed action is to interpolate all node voltages and branch currents at ($t-\Delta T$) with corresponding quantities at t in order to estimate branch currents [$i(t-\Delta T/2)$] and node voltages [$v(t-\Delta T/2)$]. All series voltage sources are also interpolated to obtain sources $p(t-\Delta T/2)$. It is also necessary to obtain

the capacitor voltages at (t – ΔT/2) for branches consisting of a series inductor and capacitor.

A time–step is next taken from (t – ΔT/2) to t using an additional [G] matrix maintained for time–steps of length ΔT/2. One advantage of this technique is that current injections from machines and other state variable type models interfaced for the (t – ΔT) to t solution are the same for the (t – ΔT/2) to t solution and need not be recalculated. The limited involvement of machines and other models in the numerical oscillation suppression technique is acceptable because adequate methods exist [17] and have been used for suppression of two time–step numerical oscillations between the model solutions and main network solution.

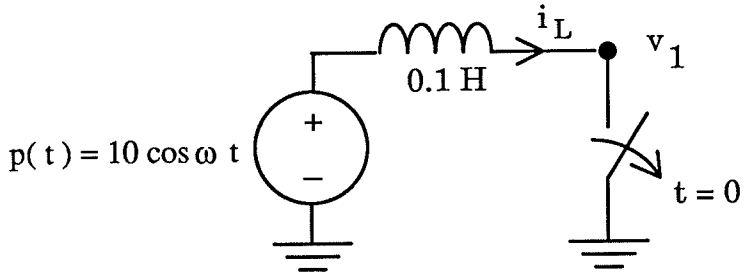


Figure 18. Circuit for Illustration of Numerical Oscillation

Figure 18 illustrates a very simple network which can be used to demonstrate the effectiveness of the numerical oscillation suppression technique. It consists of a 10 V cosine voltage source driving current through an inductor and a switch connected in series. The switch is initially closed but is opened at exactly the instant that current goes through zero. For discussion purposes, this time is referred to as t = 0.0 seconds. In the open condition the switch is represented by a resistance of 10^6 Ohms. Application of the basic Dommel trapezoidal rule

to the inductive branch with a series independent voltage source yields conductance

$$g_L = \Delta T / 2\,L \qquad \text{Eqn. 10}$$

and history current

$$I_h(t - \Delta T) = i_L(t - \Delta T) + g_L [\, p(t) + p(t - \Delta T) - v_1(t - \Delta T) \,] \qquad \text{Eqn. 11}$$

Opening the switch at t = 0, corresponding to a current zero, gives initial conditions of $i_L(0 -)$ and $v_1(0 -)$ both equal to 0 and a pre–existing voltage source of $p(0 -)$ equal to 10 volts. Under those circumstances the conventional solution method will produce an erroneous numerical oscillation in the node 1 voltage. The voltage oscillates around the true solution of 10 volts as illustrated in Figure 19.

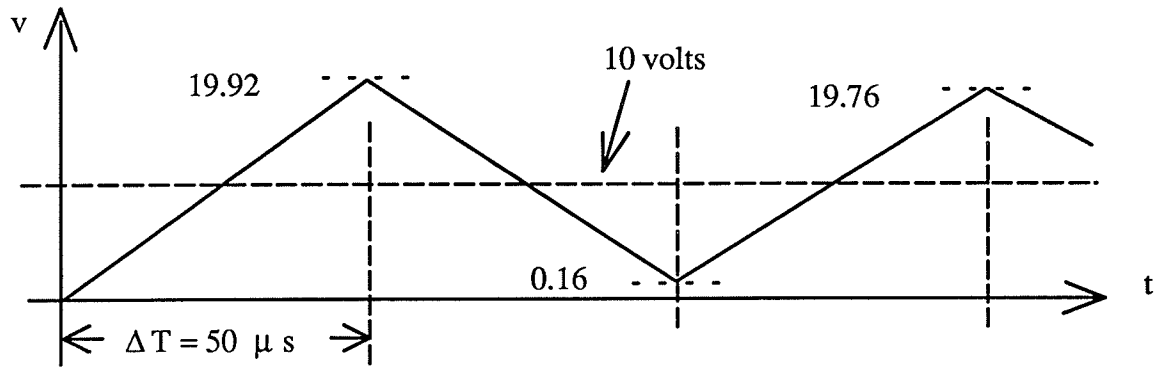


Figure 19. Numerical Oscillation of Node 1 voltage in Figure 18

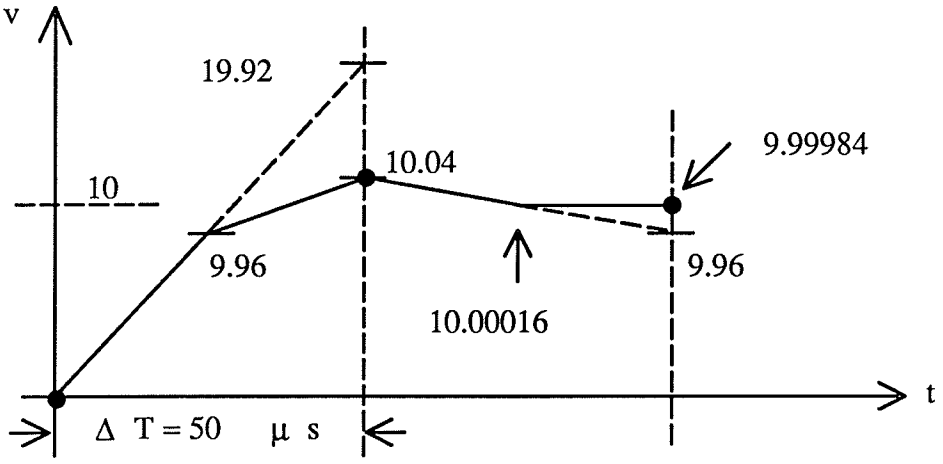


Figure 20. Effect of the Numerical Oscillation Elimination Technique

On the other hand, when the numerical oscillation suppression technique is used, the erroneous numerical oscillation is removed from the solution very quickly as illustrated by the curve in Figure 20 (not to scale). In Figure 20, the voltage solution closely approaches the true solution of 10 volts in two time–steps.

The numerical oscillation suppression technique is similarly effective for capacitive loops. Chapter 5 presents simulation results for the thesis apparatus. No numerical oscillations exist in solutions for the capacitive loops and inductive nodes in that larger apparatus.

3.5 Structure of the Overall Program

A simplified flow chart for the prototype program is shown in Figure 21. The inclusion of the simulation techniques into the program is described below with reference to the flow chart. The main program loop in the flow chart (shown as a wider line in Figure 21) corresponds to the processing of one time–step of size ΔT_1 of the simulation solution from ($t - \Delta T_1$) to t.

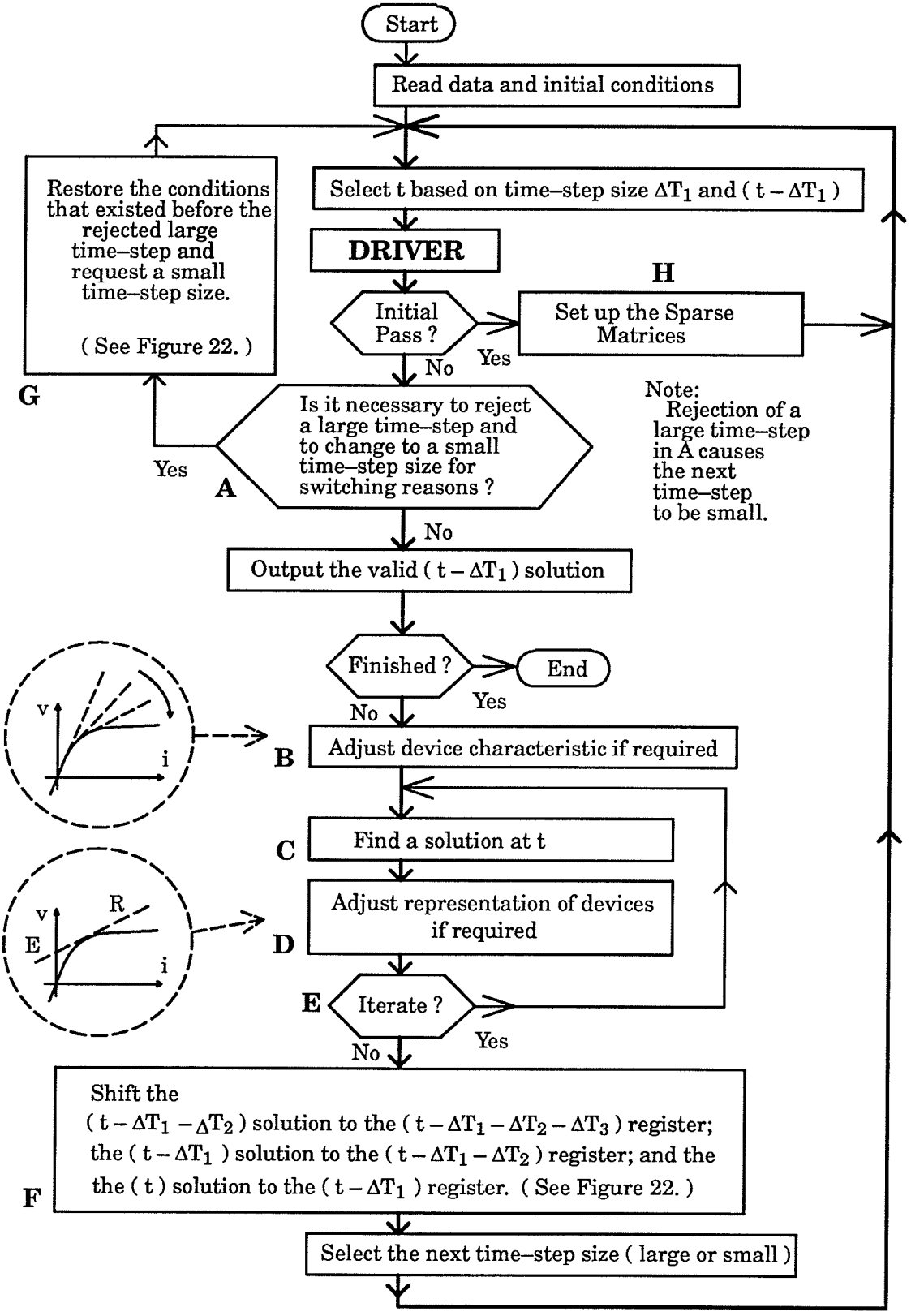


Figure 21. Flow Chart for the Prototype Simulation Program

The operation block labelled **DRIVER** in the flow chart is a user–supplied FORTRAN subroutine which makes calls to existing subroutines for modelling control blocks, machines, phase–locked–oscillators, bridge–firing logic, and breaker logic. The **DRIVER** subroutine has access to a FORTRAN COMMON block of memory shared with the main program. **DRIVER** uses the memory block to monitor the system condition; to signal switching events; and to define sources.

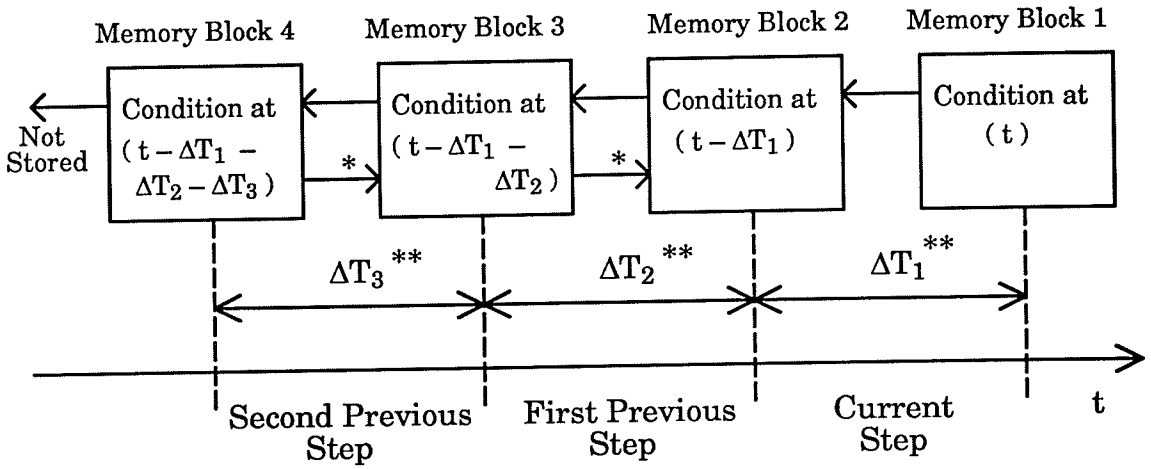
Reference to Figure 21 shows that the **DRIVER** subroutine is called once prior to processing the block labelled **H.** The block labelled **H** finalizes the list of filled positions in the sparse [G] matrix which is used in solving for node voltages in Eqn. 9 [23]. This sequence of processing provides the opportunity for the first call to a subroutine within **DRIVER** to enter branches into the network to be simulated. Accordingly, the bridge–firing subroutines in **DRIVER** can be made to enter the branches required to represent the bridge without the need for any entry in the data file. A similar approach is taken with respect to entering the interface conductances required [17] by the machine state–variable model which is called in **DRIVER** and interfaced to the main network solution.

When the characteristic curve for a device needs to be adjusted as shown in Figure 10 then the adjusting is done in the block labelled **B** in the flow chart illustrated in Figure 21. Changes to device characteristics are initiated in response to signals from the **DRIVER** subroutine.

The actual solution for the $(t-\Delta T_1)$ to t time–step occurs in the block labelled **C**. The process conducted in block **C** includes the numerical oscillation elimination procedure described in Section 3.4.

Immediately after the solution at t is obtained in the block labelled **C**, the code in the block labelled **D** determines which devices are not being properly rep-

resented in the network according to their characteristic curves. An adjustment to the device representation (i.e. source E and resistance R in Figure 11) is requested for any device which is not properly represented for the current through the device. If any adjustments are made then the block labelled **E** requests an iteration of the solution in block **C** followed by another check of device representation in block **D**. When no further iteration is requested then the solution at t is tentatively accepted.



* Restoration operation after rejection of a large step.

** Time–steps ΔT_1, ΔT_2, and ΔT_3 need not be the same size.

Figure 22. Storage of a Sequence of Solutions in the Program

Figure 22 illustrates memory blocks used for recording the network solution obtained in earlier time–steps. When the time–step ΔT_1 from $(t - \Delta T_1)$ to t gives a new solution at t then the former solutions are shifted one memory block to the left in Figure 22. This is done in the operation block labelled **F** in Figure 21. When a large time–step steps over a switching event then the program rejects the large time–step in favour of small time–steps to locate the event more accurately. These rejections are triggered in the block labelled **A** in the flow chart. When the large time–step is rejected then the condition of the system is restored to that which existed prior to the large time–step. In Figure 22 the restoration

corresponds to shifting earlier solutions one memory block to the right. This occurs in the operation block labelled **G** in the flow chart.

The above discussion of the flow chart in Figure 21 serves to identify the general sequence of processing employed in the prototype program.

The prototype program is intended to simulate power electronic circuits in power systems and potentially large systems have to be handled. The larger of two time–step sizes is the default step size for the simulation. Small time–steps are used to locate and carry out changes to device characteristics and iteration is used to assure that solution points fall on the device characteristics. The approach of using small time–steps only during switching events and not during the entire simulation greatly reduces the computational effort. Computation is further reduced by obtaining the solution for node voltages [v(t)] in Eqn 9 by forward triangularization and back substitution rather than by inversion. A sparse matrix technique has been implemented which is similar to one which has been used in the popular EMTP program [23]. In addition, the most effective method of "near optimal" node numbering suggested by Tinney and Walker [23] has been implemented in order to maintain sparsity in the forward triangularization process. Row elimination is practised in the forward triangularization [16], [23] so that when a branch is changed triangularization can be started at the row number associated with the smallest node number for the branch.

A further technique, not yet implemented, is to break larger networks into subsystems connected by travelling–wave transmission lines as is done in the program EMTDC [17]. Time–step solutions in each subsystem would be solved independently using Eqn. 8 separately prepared for each subsystem. This independent solution of the subsystems would permit one to choose the most appro-

priate time–step size for the next time–step in a subsystem regardless of the time–step size chosen for the other subsystems. Travelling–wave transmission line models typically include a vector to store the profile of the travelling–wave of current incident on a subsystem. Subsystems connected by a travelling–wave transmission line model do not need to use simultaneous time–steps of the same size because the current injections for a subsystem solution can be obtained by interpolating between the points in the vector. Solving a large network as several subsystems permits using a single large time–step in most subsystems simultaneously with the use of small time–steps in any subsystem that requires the small time–step size for switching. The ability to split the network into subsystems and to choose the most appropriate time–step size for each subsystem becomes very important when the number of devices in the network becomes large.

The importance of splitting a network containing a large number of power electronic devices into subsystems can be made clear by considering the consequences of continuing to add devices to a network solved as a single subsystem. By continuing to increase the number of devices in the single subsystem the situation would arise where there would almost always be a switching event being located or a characteristic curve being modified throughout the duration of the simulation. Locating a switching event or changing a characteristic curve requires the use of small time–steps. Consequently, the benefit of having a large time–step size available would be virtually lost because the small time–step size would be used for nearly the entire simulation of the large network. On the other hand, splitting a network containing many devices into smaller subsystems would reduce the number of devices in each subsystem. The reduced number of devices in each subsystem would allow the simulation of the subsystems to proceed more quickly because the small time–steps would be needed for a smaller fraction of the simulation time in each subsystem.

3.6 Modelling Interaction of d and q Axis Mutual Fluxes in Round Rotor Induction Machines Due to Saturation

An improved method of representing the saturation of the main flux path in a round rotor induction machine was developed as part of the thesis work. Much of this aspect of the work has been anticipated in a paper [14] presented at the 1988 IEEE Power Engineering Society Winter Meeting. Unfortunately the paper was not published in the IEEE Transactions on Energy Conversion until June, 1991. The presentation of the method below with laboratory verification will thus serve as a confirmation of the technique described by Hallenius et al [14].

Self–excitation of the induction machine described in Appendix I was conducted in the laboratory with three 170 μF capacitors connected in delta configuration on the machine terminals. The dynamic voltage build–up observed is as illustrated in Figure 23. The unmodified transients simulation model for the induction machine first employed gave a voltage build–up during transients simulation of self–excitation as illustrated in Figure 24. It can be seen that the original simulation model did predict the correct final operating voltage of approximately 420 volts line–to–line peak. One p.u. voltage is 294 volts line–to–line peak. However, there are two notable differences in the dynamics of the voltage build–up to be noticed when comparing the original simulation results and the actual voltage build–up.

The most important difference in dynamics relates to the rate of build–up of voltage once saturation of the main flux becomes a significant factor. The laboratory measured voltage in Figure 23 rises from 1.0 p.u. voltage (294.0 volts line–to–line peak) to approximately the final voltage level in approximately 6 cycles. However, the voltage build–up from 1.0 p.u. voltage using the original transients simulation model extended over about 15 cycles as illustrated in Figure

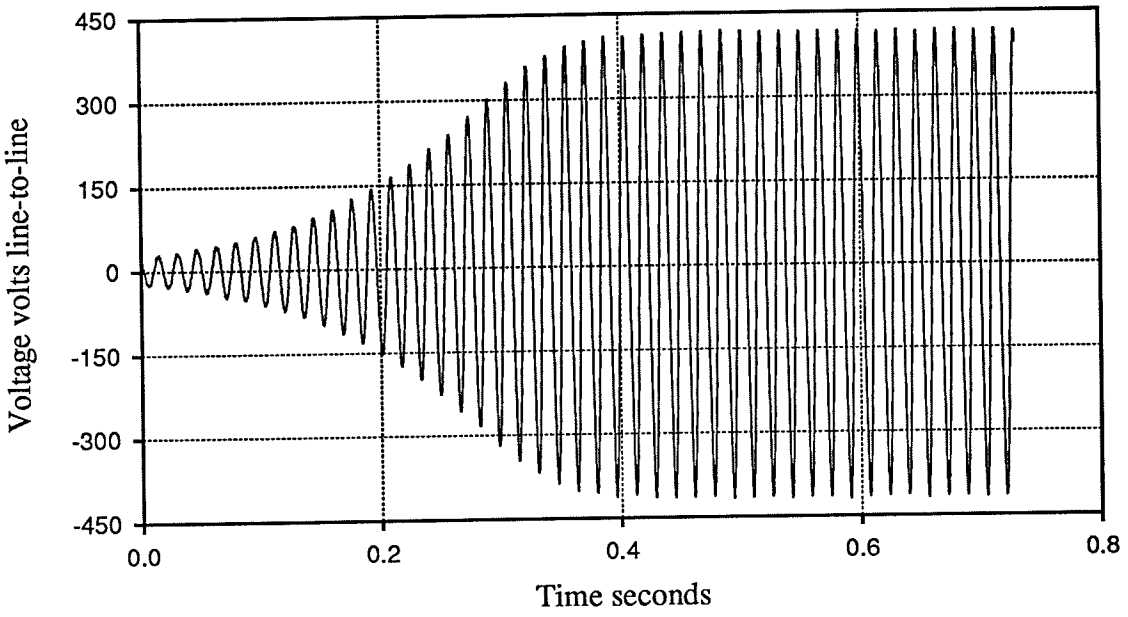


Figure 23. Laboratory Self–Excitation of the Appendix I Machine

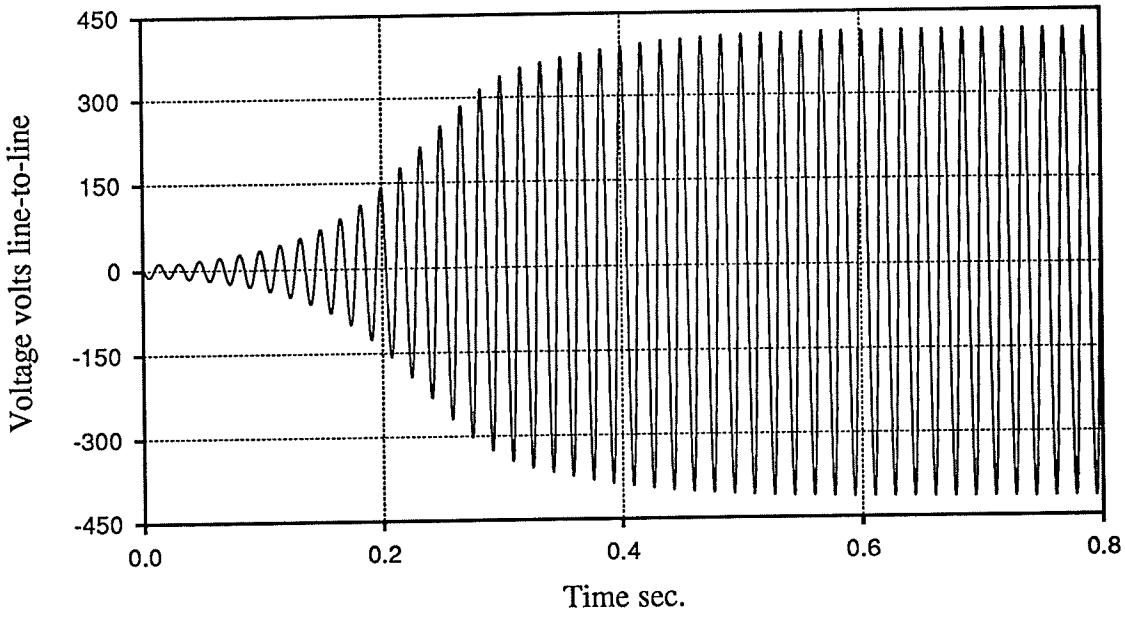


Figure 24. Self–Excitation According to the Original Machine Model

24. This difference in dynamics is significant and is discussed below following the disposal of the second difference.

A second and less significant difference in the dynamics of voltage build–up relates to the rate of voltage build–up at lower levels of saturation. It can be seen that at lower levels of voltage the build–up predicted by the transients simulation model and illustrated in Figure 24 occurs more quickly than the actual build–up illustrated in Figure 23. This difference at low voltage is less important to the thesis work because the machine is operated at 1.0 p.u. voltage in the thesis apparatus. The difference is very likely at least partially related to the simple representation of the saturation curve in the transients simulation model of the machine. In Appendix I a table is given for measured p.u. magnetizing reactance versus p.u. air–gap voltage. It can be seen that the largest magnetiz-

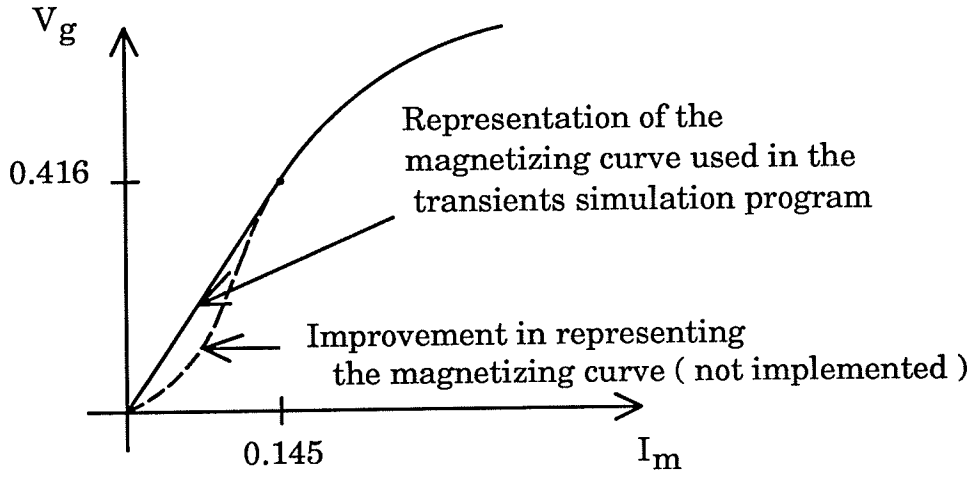


Figure 25. A Detail of a Magnetizing Curve at Low Voltage

ing reactance is 2.86 p.u. which occurs at 0.416 p.u. air–gap voltage. In the transients simulation model the magnetizing curve below 0.416 p.u. voltage is represented by a straight line through the origin with slope X_m = 2.86 p.u. as illustrated in Figure 25 by the solid curve. However, authors Elder, Boys, and

Woodward [24] have shown that the magnetizing curve is more properly represented according to a curve such as the dashed line in Figure 25. This more detailed representation of the saturation curve at low levels of voltage has not been implemented because the dynamics of the voltage build–up at such low levels of voltage is not a significant factor in designing the control system for the thesis apparatus.

The original transients simulation model for the induction machine was reviewed and modified to better simulate the dynamic build–up of voltage for a self–excited induction machine at higher levels of voltage where saturation of the main flux path is significant. In the dq axis representation of an induction machine the state–variable description of d and q axis current derivatives are given by matrix Equations 12 and 13.

$$\left[\frac{d\lambda_{dq}}{dt}\right] = \left[V_{dq}\right] - \left[R_{dq}\right]\left[I_{dq}\right] - \nu\left[G_{dq}\right]\left[I_{dq}\right] \qquad \text{Eqn 12}$$

$$\left[\frac{dI_{dq}}{dt}\right] = \left[L\right]^{-1}\left[\frac{d\lambda_{dq}}{dt}\right] \qquad \text{Eqn 13}$$

The components in the right hand side (R.H.S.) of Eqn. 12 represent respectively voltages externally applied to the d and q axis windings, $[V_{dq}]$; resistive voltage drops in the windings, $[R_{dq}][I_{dq}]$; and generation voltages for the windings, $\nu[G_{dq}][I_{dq}]$. The left hand side (L.H.S.) of Eqn. 12 thus represents the

rates of change of flux linkages in the windings on the d and q axes. Eqn. 13 can be re–written as Eqn. 14.

$$\left[\frac{d\lambda_{dq}}{dt}\right] = \left[\quad L \quad\right]\left[\frac{dI_{dq}}{dt}\right] \qquad \text{Eqn 14}$$

The transients simulation model of a single cage induction machine includes a stator (armature) winding and a rotor winding on the d axis and a stator winding and a rotor winding on the q axis. In that case, the L.H.S. of Eqn. 14 can be expanded as shown in Eqn. 15. In Eqn. 15 the mutual d–axis flux linkage has subscript "md" and the mutual q–axis flux linkage has subscript "mq".

$$\begin{bmatrix} \frac{d\lambda_d}{dt} \\ \frac{d\lambda_{kd}}{dt} \\ \frac{d\lambda_q}{dt} \\ \frac{d\lambda_{kq}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} + \begin{bmatrix} \frac{d\lambda_{sd}}{dt} \\ \frac{d\lambda_{rd}}{dt} \\ \frac{d\lambda_{sq}}{dt} \\ \frac{d\lambda_{rq}}{dt} \end{bmatrix} \qquad \text{Eqn 15}$$

The stator d–axis winding flux linkage is given the subscript "d" and the stator q–axis winding flux linkage is given the subscript "q". Similarly, the rotor d–axis winding flux linkage is given the subscript "kd" and the rotor q–axis winding

flux linkage is given the subscript "kq". The second vector on the R.H.S. of Eqn. 15 represents the vector of rates of change of leakage flux linkages.

If one assumes no interaction between the d and q axis flux linkages due to saturation then the vector of rate of change of mutual flux linkages in Eqn. 15 can be expressed according to Eqn. 16. The winding currents in Eqn. 16 have the same subscripts as are assigned above to the winding flux linkages. Similarly, the mutual inductances have the same subscripts as are assigned above to the mutual flux linkages. The vector of rates of change of leakage flux linkages in Eqn. 15 is expressed in Eqn. 17. Inductance L_s and L_r are respectively the stator and rotor leakage inductances.

$$\begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} = \left[\begin{array}{cc|cc} L_{md} & L_{md} & 0 & 0 \\ L_{md} & L_{md} & 0 & 0 \\ \hline 0 & 0 & L_{mq} & L_{mq} \\ 0 & 0 & L_{mq} & L_{mq} \end{array}\right] \begin{bmatrix} \frac{dI_d'}{dt} \\ \frac{dI_{kd}}{dt} \\ \frac{dI_q}{dt} \\ \frac{dI_{kq}}{dt} \end{bmatrix} \quad \text{Eqn 16}$$

$$\begin{bmatrix} \frac{d\lambda_{sd}}{dt} \\ \frac{d\lambda_{rd}}{dt} \\ \frac{d\lambda_{sq}}{dt} \\ \frac{d\lambda_{rq}}{dt} \end{bmatrix} = \left[\begin{array}{cc|cc} L_s & 0 & 0 & 0 \\ 0 & L_r & 0 & 0 \\ \hline 0 & 0 & L_s & 0 \\ 0 & 0 & 0 & L_r \end{array}\right] \begin{bmatrix} \frac{dI_d'}{dt} \\ \frac{dI_{kd}}{dt} \\ \frac{dI_q}{dt} \\ \frac{dI_{kq}}{dt} \end{bmatrix} \qquad \text{Eqn 17}$$

Eqn. 16 will certainly be true if there is no saturation of the mutual inductances. However, if there is saturation, then Eqn. 16 needs to be modified to account for interaction between the d and q axes. The d–axis and q–axis magnetizing currents which produce the d–axis and q–axis mutual flux linkages are respectively:

$$I_{md} = I_d' + I_{kd} \qquad \text{Eqn 18}$$

and

$$I_{mq} = I_q + I_{kq} \qquad \text{Eqn 19}$$

The original induction machine model accounted for saturation by finding the net magnetizing current as

$$I_m' = \sqrt{I_{md}^2 + I_{mq}^2} \qquad \text{Eqn. 20}$$

and then using $I_{m'}$ to look–up the instantaneous magnetizing inductance L_{inst} at the operating point on the saturation curve as illustrated in Figure 28. The value of L_{inst} obtained at a given instant in the simulation was then assigned to L_{md} and L_{mq} in Eqn. 16. These inductances are shown below to be correct for

constant ac voltage magnitude on the machine. However, such an approach is too simple for representing the dynamics of voltage magnitude change.

The definitions for I_{md} and I_{mq} contained in Eqns. 18 and 19 allow Eqn. 16 to be collapsed to Eqn. 21.

$$\begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} = \left[\begin{array}{c|c} L_{md} & 0 \\ \hline 0 & L_{mq} \end{array}\right] \begin{bmatrix} \frac{dI_{md}}{dt} \\ \frac{dI_{mq}}{dt} \end{bmatrix} \qquad \text{Eqn 21}$$

The collapse of Eqn. 16 into Eqn. 21 reduces the task of representing interaction of d–axis and q–axis mutual flux linkages to the task of providing a more realistic replacement for Eqn. 21. In order to develop the modified version of Eqn. 21 one can commence with a simple system of two perpendicular sinusoidally distributed windings "d" and "q" on a round magnetic core as illustrated in Figure 26. It is assumed that I_{md} flows in winding d in Figure 26 and I_{mq} flows in winding q. Referring to Figure 27, the main flux λ_m will fall on the same angle ρ with respect to the q–axis as the net magnetizing current $I_{m'}$ because of the symmetry of the round core.

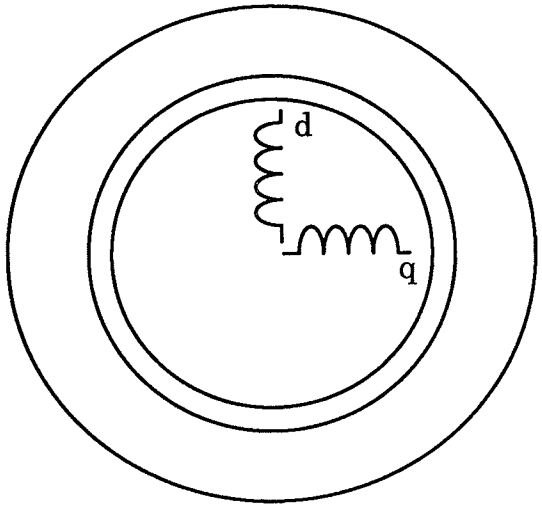


Figure 26. Perpendicular D and Q Axis Windings on a Core

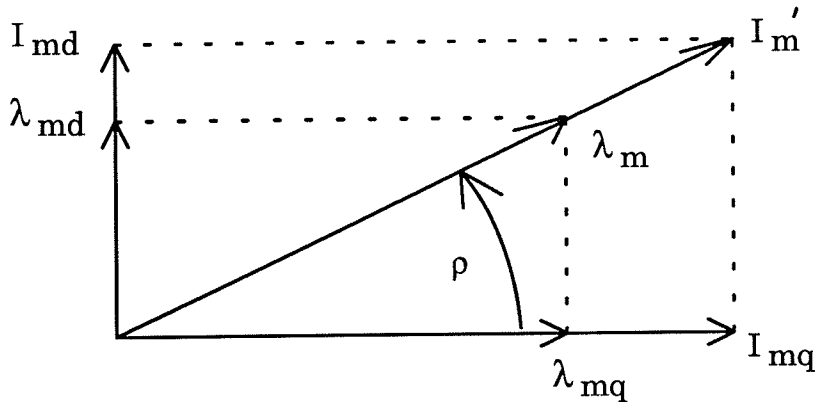


Figure 27. Alignment of the Main Flux and Net Magnetizing Current

It is clear from Figure 27 that

$$\lambda_{md} = \lambda_m \sin \rho \qquad \text{Eqn. 22}$$

and

$$\lambda_{mq} = \lambda_m \cos \rho \qquad \text{Eqn. 23}$$

Taking the derivative of Eqn. 22 and 23 with respect to time yields

$$\frac{d\lambda_{md}}{dt} = \frac{d\lambda_m}{dt}\sin\rho + \lambda_m \cos\rho \frac{d\rho}{dt} \qquad \text{Eqn. 24}$$

$$\frac{d\lambda_{mq}}{dt} = \frac{d\lambda_m}{dt}\cos\rho - \lambda_m \sin\rho \frac{d\rho}{dt} \qquad \text{Eqn. 25}$$

Figure 27 also illustrates that

$$\sin\rho = \frac{I_{md}}{I_{m'}} \qquad \text{Eqn. 26}$$

and

$$\cos\rho = \frac{I_{mq}}{I_{m'}} \qquad \text{Eqn. 27}$$

With reference to Eqn. 20 and Figure 27 it can be determined that

$$\frac{\delta I_{m'}}{\delta I_{mq}} = \frac{I_{mq}}{I_{m'}} \qquad \text{Eqn. 28}$$

and

$$\frac{\delta I_{m'}}{\delta I_{md}} = \frac{I_{md}}{I_{m'}} \qquad \text{Eqn. 29}$$

In Figure 27 the main flux λ_m is related to the net magnetizing current $I_{m'}$ according to a saturation curve such as illustrated in Figure 28. At the operating point in Figure 28

$$\lambda_m = L_{inst}\, I_{m'} \qquad \text{Eqn. 30}$$

and

$$\frac{d\lambda_m}{dt} = L_{inc} \frac{dI_{m'}}{dt} \qquad \text{Eqn. 31}$$

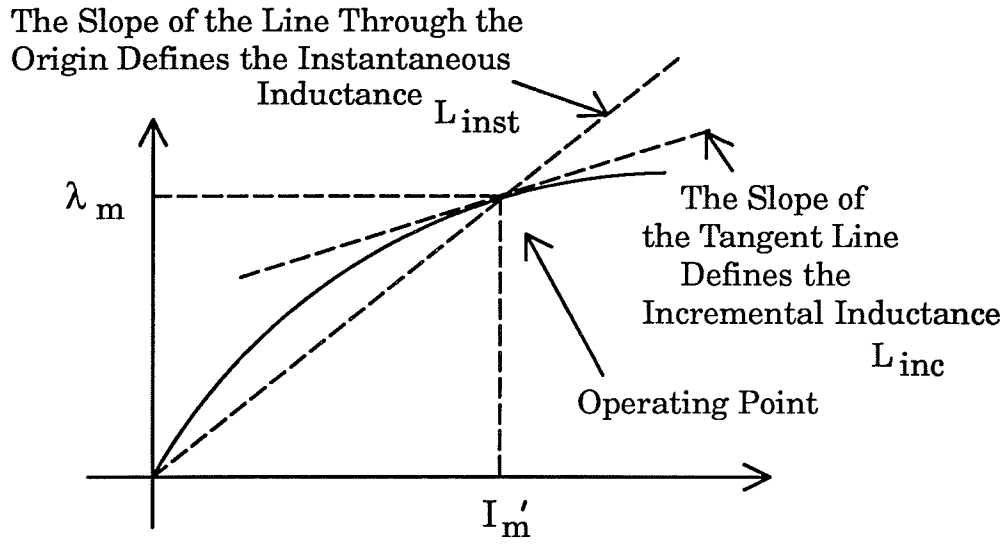


Figure 28. Inductances Defined on a Saturation Curve

Eqns. 28 and 29 allow Eqn. 31 to be expanded to Eqn. 32.

$$\frac{d\lambda_m}{dt} = L_{inc}\frac{I_{md}}{I_m'}\frac{dI_{md}}{dt} + L_{inc}\frac{I_{mq}}{I_m'}\frac{dI_{mq}}{dt} \qquad \text{Eqn. 32}$$

With further reference to Figure 27

$$\rho = \tan^{-1}\left[\frac{I_{md}}{I_{mq}}\right] \qquad \text{Eqn. 33}$$

Eqn. 33 can be used to develop Eqn. 34.

$$\frac{d\rho}{dt} = \frac{I_{mq}}{I_m'^2}\frac{dI_{md}}{dt} - \frac{I_{md}}{I_m'^2}\frac{dI_{mq}}{dt} \qquad \text{Eqn. 34}$$

Substituting Eqns. 26, 27, 32, and 34 into Eqns. 24 and 25 gives a replacement for Eqn. 21, namely:

$$\begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} = \left[\begin{array}{c|c} L_1 & L_3 \\ \hline L_3 & L_2 \end{array}\right] \begin{bmatrix} \frac{dI_{md}}{dt} \\ \frac{dI_{mq}}{dt} \end{bmatrix} \qquad \text{Eqn. 35}$$

where

$$L_1 = L_{inst}\left[\frac{I_{mq}}{I_m'}\right]^2 + L_{inc}\left[\frac{I_{md}}{I_m'}\right]^2 \qquad \text{Eqn. 36}$$

$$L_2 = L_{inst}\left[\frac{I_{md}}{I_m'}\right]^2 + L_{inc}\left[\frac{I_{mq}}{I_m'}\right]^2 \qquad \text{Eqn. 37}$$

$$L_3 = \left[L_{inc} - L_{inst}\right]\frac{I_{mq}\, I_{md}}{I_m'^{\,2}} \qquad \text{Eqn. 38}$$

Substituting Eqns. 18 and 19 into Eqn. 35 allows an expansion of Eqn. 35 to give Eqn. 39. Eqn. 39 provides a replacement for Eqn. 16 and describes mutual inductance terms between the d and q axes.

$$\begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} = \left[\begin{array}{cc|cc} L_1 & L_1 & L_3 & L_3 \\ L_1 & L_1 & L_3 & L_3 \\ \hline L_3 & L_3 & L_2 & L_2 \\ L_3 & L_3 & L_2 & L_2 \end{array}\right] \begin{bmatrix} \frac{dI_d'}{dt} \\ \frac{dI_{kd}}{dt} \\ \frac{dI_q}{dt} \\ \frac{dI_{kq}}{dt} \end{bmatrix} \qquad \text{Eqn 39}$$

Finally, a new expression for [L] in Eqn. 13 is obtained by adding the leakage inductance matrix in Eqn. 17 to the mutual inductance matrix in Eqn. 39. Fig-

ure 29 illustrates the simulated build–up of voltage obtained using the the mutual inductance matrix of Eqn. 39. Comparison of Figure 29 with the actual voltage in Figure 23 shows that the build–up of voltage using the new simulation model correctly continues until a few cycles before the final ac voltage is reached. This contrasts with the slow approach to the final operating voltage illustrated in Figure 24 for the old induction machine model.

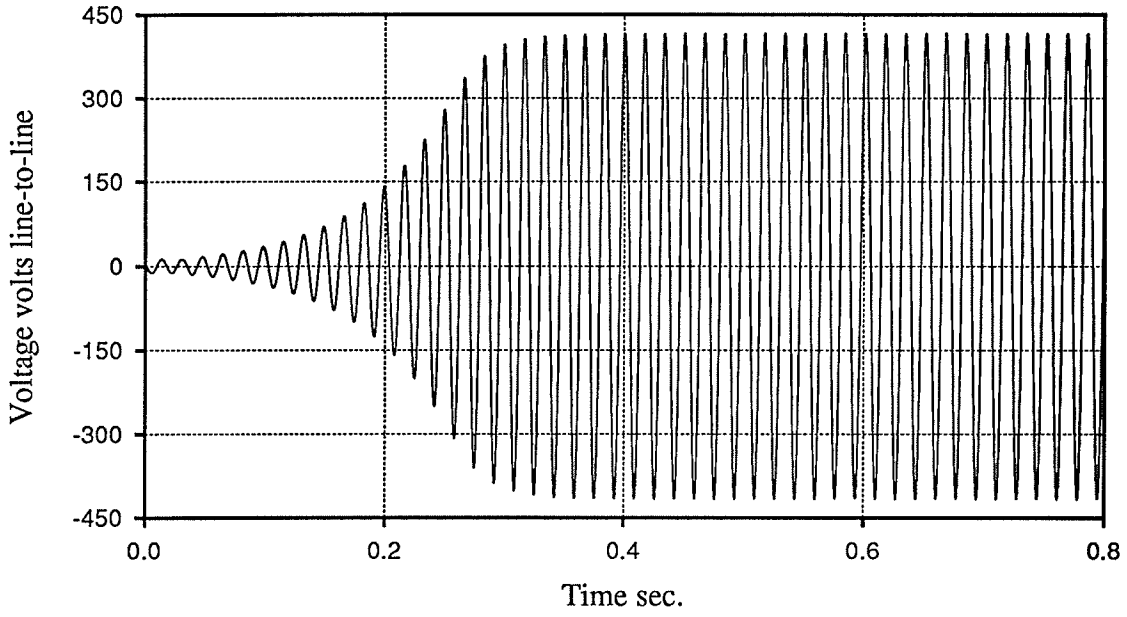


Figure 29 Self–Excitation According to the Modified Machine Model

In closing the discussion of the induction machine model it should be noted that the old and new induction machine models both predict the same final level of self–excitation voltage. In this regard compare Figures 24 and 29. This correlation is easily explained by the fact that at constant λ_m the mutual inductance matrix for the new model in Eqn. 39 can be reduced to the mutual inductance matrix in Eqn. 16 which is used for the old induction machine model. This result is readily obtained having regard to two points. As a first point, when λ_m is constant any term in Eqns. 36, 37, and 38 containing L_{inc} drops out because the rate of change of $I_{m'}$ will also be zero. As a second point, when $I_{m'}$ is constant the rate

of change of I_{md} can be expressed in terms of the rate of change of I_{mq} and vice versa. In this regard see Eqn. 20. When these points are considered Eqn. 35 can be written as

$$\begin{bmatrix} \frac{d\lambda_{md}}{dt} \\ \frac{d\lambda_{mq}}{dt} \end{bmatrix} = \left[\begin{array}{c|c} L_{inst} & 0 \\ \hline 0 & L_{inst} \end{array}\right] \begin{bmatrix} \frac{dI_{md}}{dt} \\ \frac{dI_{mq}}{dt} \end{bmatrix} \qquad \text{Eqn. 40}$$

which is the same as for the original model.

This chapter has described the preparation of simulation tools. A prototype transients simulation program has been described which is particularly adapted for the simulation of switching devices in power system networks. A description has also been given of modifications to an induction machine model implemented to facilitate the more correct simulation of self–excitation dynamics. Chapter 4 describes the control algorithm developed for the thesis apparatus. The prototype transients simulation program was instrumental in developing and testing the control algorithm prior to building the apparatus.

Chapter Four

The Control System Design

4.1 Introduction

This chapter describes a control system for the apparatus illustrated in Figure 30. The control system provides a duty–cycle order β to the voltage–boost converter and a firing delay–angle α to the rectifier. The described control system consists of a feed–forward control for quick response to sudden load changes combined with a feed–back control to correct for any error in the feed–forward control. Some error in the feed–forward control can be expected because of the errors and simplifications in the model used in the feed–forward control. A simplified schematic of the apparatus and a condensed block diagram of the control system are illustrated in Figure 31.

The control system outlined in Figure 31 is designed to meet the control requirements of the apparatus during both steady running and transient conditions. The Load Voltage PI Controller shown in Figure 31 monitors error in ac load voltage and produces a dc capacitor voltage reference signal, V_{Iref}. V_{Iref} is passed to the Power Order Control Block in the Main Control. The Main Control responds to V_{Iref} and controls the dc capacitor voltage V_I so as to obtain the requested ac load voltage.

The Power Order Control Block shown in Figure 31 receives V_{Iref} and creates a p.u. power order. The power order is essentially the measured load power (V_I times I_L) plus additional (typically smaller) components of power to regulate V_I according to V_{Iref}. These additional components of power (described in a later section) compensate for expected errors in the measurement of the load power as well as providing correction of V_I during start–up and other transient conditions.

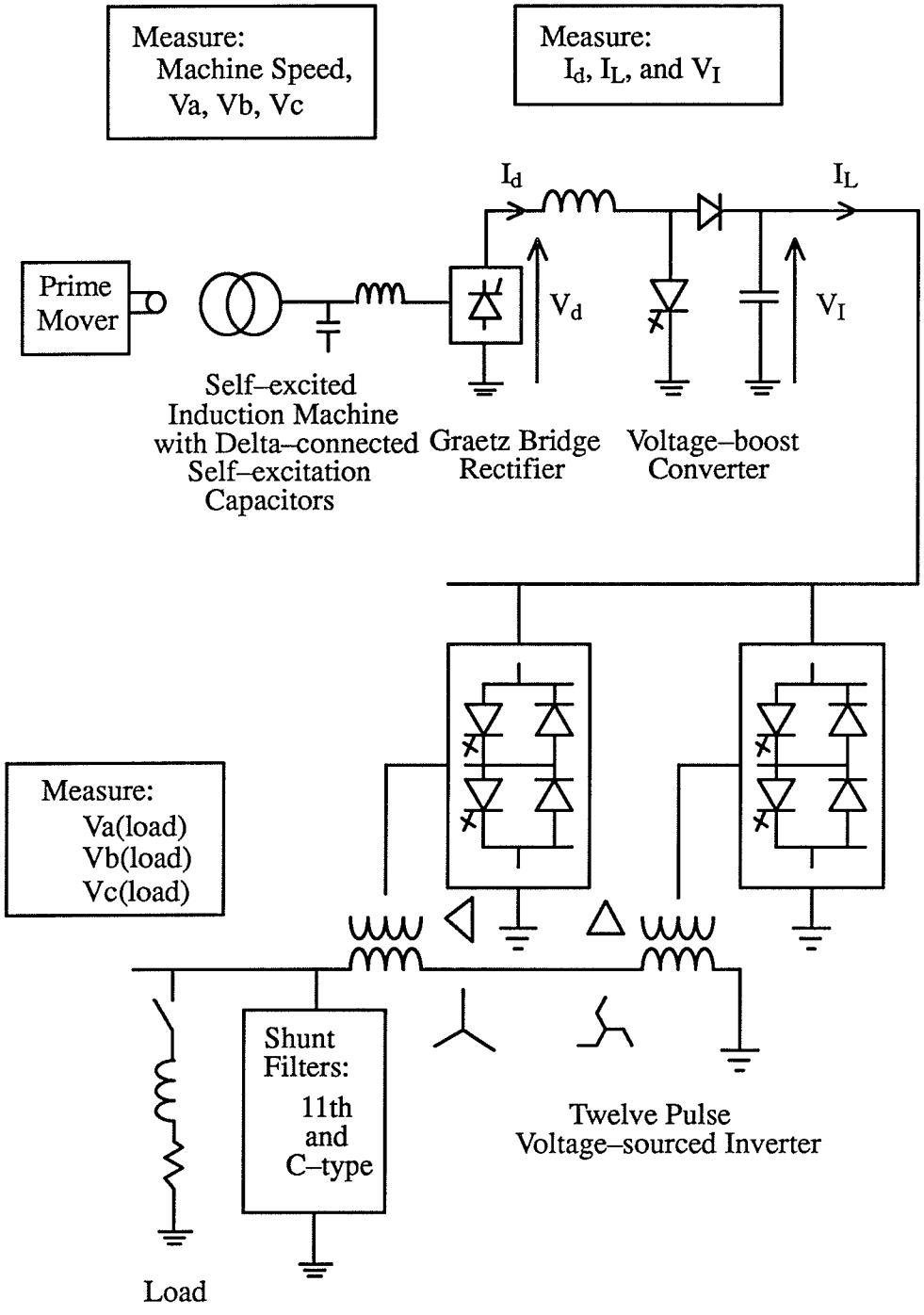


Figure 30. A Single–Line Diagram of Apparatus for Supplying Isolated ac Load

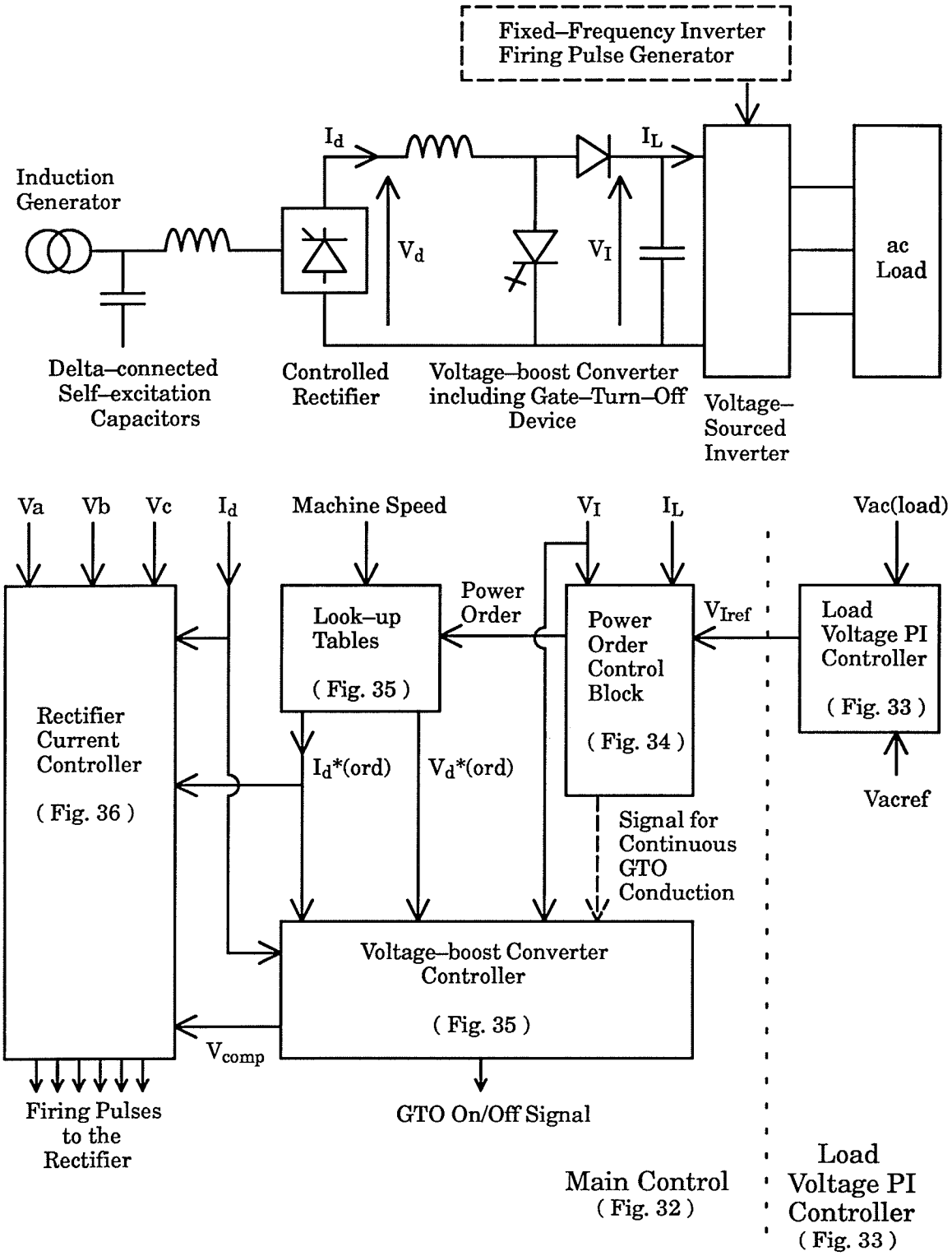


Figure 31. A Condensed Schematic of the Apparatus with Associated Controls

The power order is implemented by passing it along with machine speed to the Look–up Tables shown in Figure 31. The tables provide basic reference values for dc current I_d*(ord) and dc voltage V_d*(ord). The Look–up Tables are based on curves such as illustrated in Figures 7 and 8. The value of I_d*(ord) provided by the tables is equal to a pre–calculated magnitude of dc current I_d intended to provide operation of the machine at approximately 1.0 p.u. voltage for the given combination of machine speed and power order. The product of I_d*(ord) and V_d*(ord) provided by the tables is always equal to the input power order. I_d*(ord) and V_d*(ord) are provided in an essentially open–loop feed–forward manner because they depend mainly on measured machine speed and load power.

The Voltage–boost Converter Controller receives the basic dc voltage order V_d*(ord) and (after minor adjustments described in a later section) produces a Target Voltage which is the reference for controlling the average voltage at the load end of the dc inductor. The Voltage–boost Converter Controller controls the voltage–boost converter by means of a duty–cycle order β. The duty–cycle order β specifies the time T_{off} that the GTO device is turned "off" during a period of the voltage–boost converter according to $T_{off} = \beta \times T_{vbc}$ where T_{vbc} is the period of the voltage–boost converter. The dc capacitor voltage V_I is only applied to the load end of the dc inductor when the GTO device is turned "off". The average voltage at the load end of the dc inductor is therefore equal to β times V_I during a period of the voltage–boost converter. The Voltage–boost Converter Controller accordingly selects β in order to provide the Target Voltage voltage at the load end of the dc inductor as closely as possible having regard to the available dc capacitor voltage V_I. The Voltage–boost Converter Controller also creates a signal V_{comp} representing the actual average voltage at the load end of the dc inductor by multiplying the actual duty–cycle β* times V_I. The signal V_{comp} is then passed to the

Rectifier Current Controller where it forms the main component of the final dc voltage order V_d(ord).

The Rectifier Current Controller receives the basic dc current order I_d*(ord) and adjusts it to provide a final dc current order for controlling I_d. The adjustments to I_d*(ord) (described in a later section) remove oscillations in machine voltage magnitude V_m and also overcome errors in steady running so as to cause V_m to settle to 1.0 p.u. voltage. The Rectifier Current Controller supplements V_{comp} received from the Voltage–boost Converter Controller by adding a component V_d(adj) in order to produce the final dc voltage order V_d(ord). The resultant final dc voltage order V_d(ord) controls the rectifier output voltage V_d so as to adjust I_d to the necessary level.

The control action briefly described above regulates V_d and I_d during steady running so that the machine voltage is regulated to 1.0 p.u. voltage and the necessary power is supplied to the load. As part of this action the inverter dc capacitor voltage V_I is also regulated. However, the control system also responds quickly and accurately during transients such as those which occur after a sudden large load change. The rapid response of the control system is attributable to the fact that changes in the measured load power are carried through the control signal paths described above in a feed–forward manner and cause changes in both the final dc current order I_d(ord) and the final dc voltage order V_d(ord) to occur within approximately one period of the voltage–boost converter (e.g. 1.0 msec.).

The selection of the dc inductor and dc capacitor sizes is described in this chapter. The twelve pulse voltage–sourced inverter illustrated in Figure 30 is of standard design and is described with filters in Appendix III.

The schematic for the Main Control is illustrated in detail in Figure 32. For explanation purposes the schematic illustrated in Figure 32 is divided into three parts illustrated in Figures 34, 35, and 36. A slightly more detailed description of the parts and their interaction is given in the next section. Detailed explanations of the schematics in Figures 34, 35, and 36 are given in later sections of this chapter. It is suggested that readers refer to Figures 34, 35, and 36 to study the individual parts of the control and that Figure 32 should only be used as an overall connection diagram.

4.2 A General Description of the Control System

This section describes the basic control loops and their interaction. Transients simulation has been used to develop and test the operation of the control system. In addition to transients simulation, the Main Control illustrated in Figure 32 has also been tested on digital control hardware built in the laboratory. The laboratory verification is described in Chapter 6. The general description presented in this section consists of brief descriptions of the Power Order Control Block, the Look–up Tables and Voltage–boost Converter Controller, and the Rectifier Current Controller illustrated respectively in Figures 34, 35, and 36.

Chapter 1 describes the choice of apparatus configuration illustrated in Figure 30 and explains the function of the voltage–boost converter. The voltage–boost converter acts as a interface for matching the variable dc output voltage of the Graetz bridge rectifier to the relatively–fixed dc voltage V_I on the inverter dc capacitor. V_I is not actually fixed but in fact must be regulated over a range of about 10 percent in order to offset an ac voltage drop in the inverter transformers which varies with the ac load current. In transient simulations of the example system V_I is regulated in the range between 310 and 340 volts. The dc capaci-

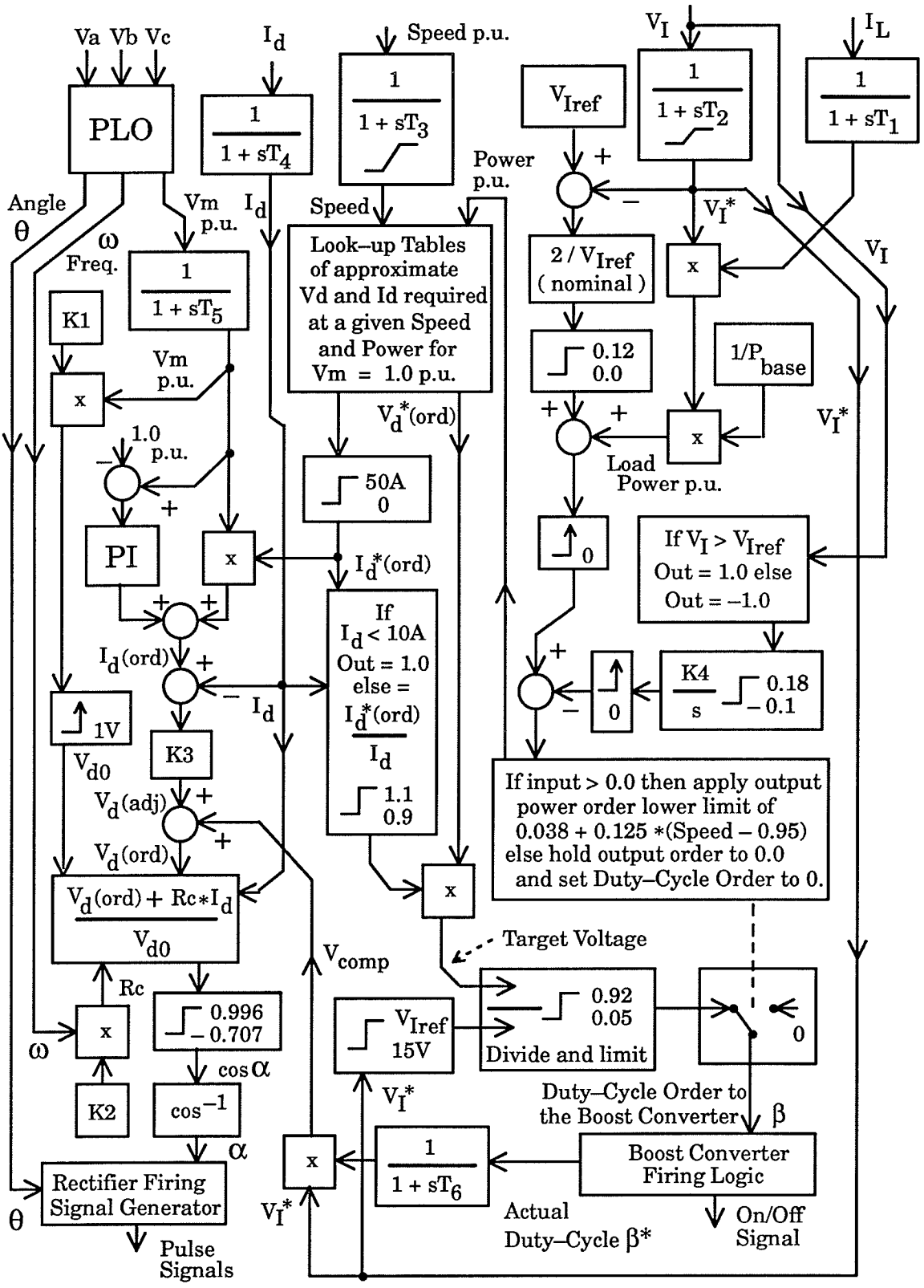


Figure 32. The Main Control Schematic

tor voltage order V_{Iref} is developed by the Load Voltage PI (proportional–integral) Controller illustrated in Figure 33 which responds to error in the ac

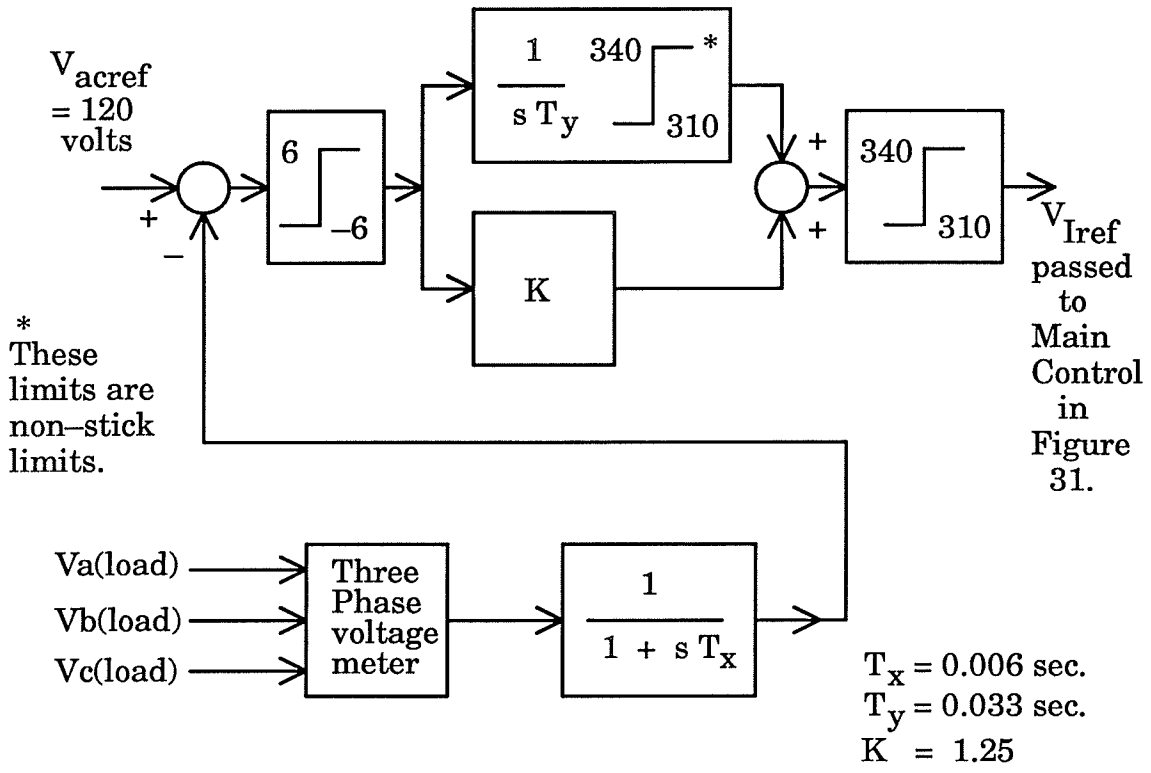


Figure 33. The ac Load Voltage PI Controller

load voltage. V_{Iref} is passed to the Main Control illustrated in Figure 32. The Load Voltage PI Controller changes V_{Iref} so as to obtain the necessary dc capacitor voltage V_I to maintain rated ac load voltage.

The Power Order Control Block schematic illustrated in Figure 34 is an excerpt from the Main Control illustrated in Figure 32. The Power Order Control Block develops a power order for the power which must be supplied from the voltage–boost converter to the inverter dc capacitor and the inverter in Figure 31 in order to regulate the capacitor voltage V_I according to V_{Iref}. This power order is developed essentially by measuring the power to the load and adding a component of power to correct V_I toward V_{Iref}. With reference to Figures 31 and 34,

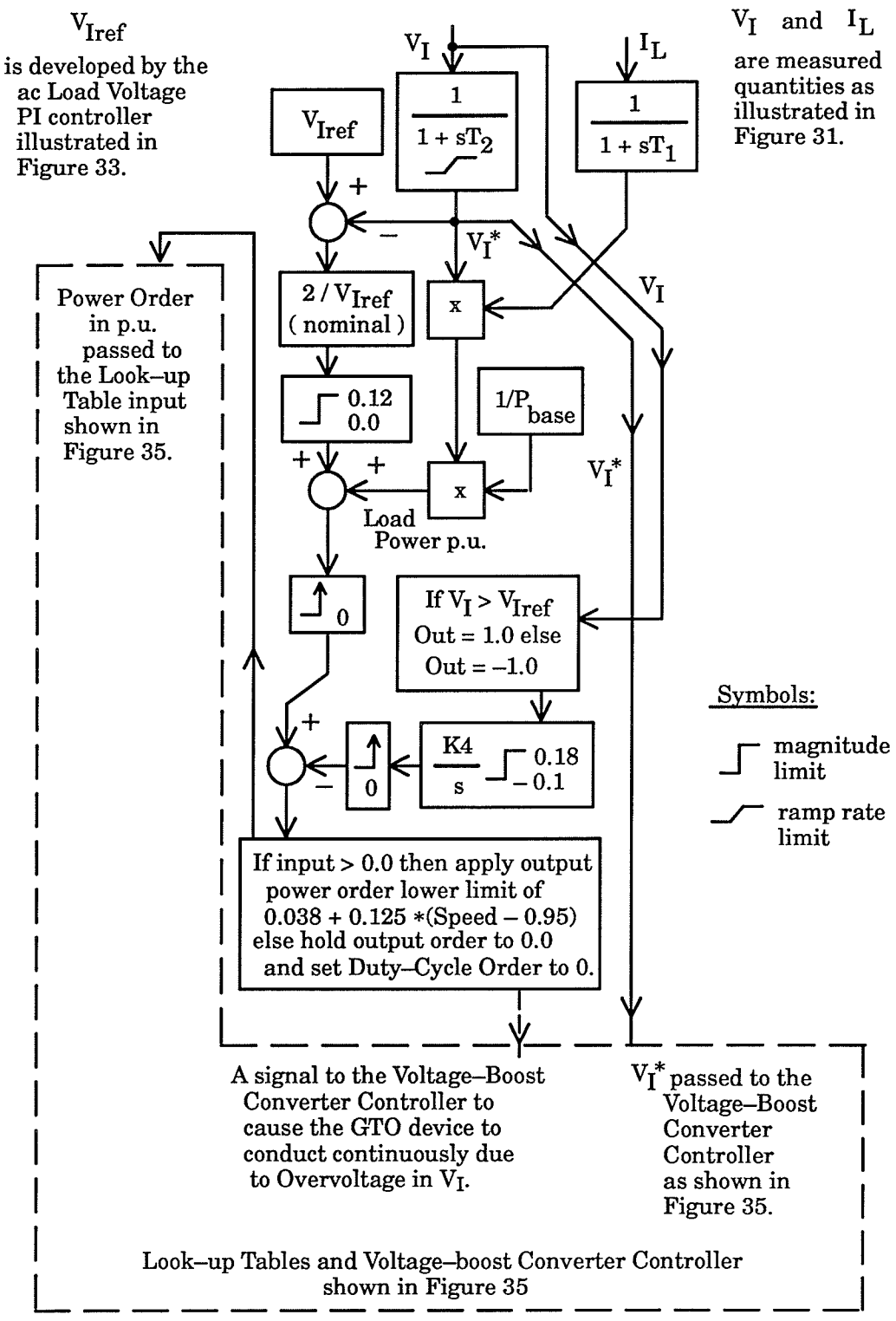


Figure 34. The Power Order Control Block

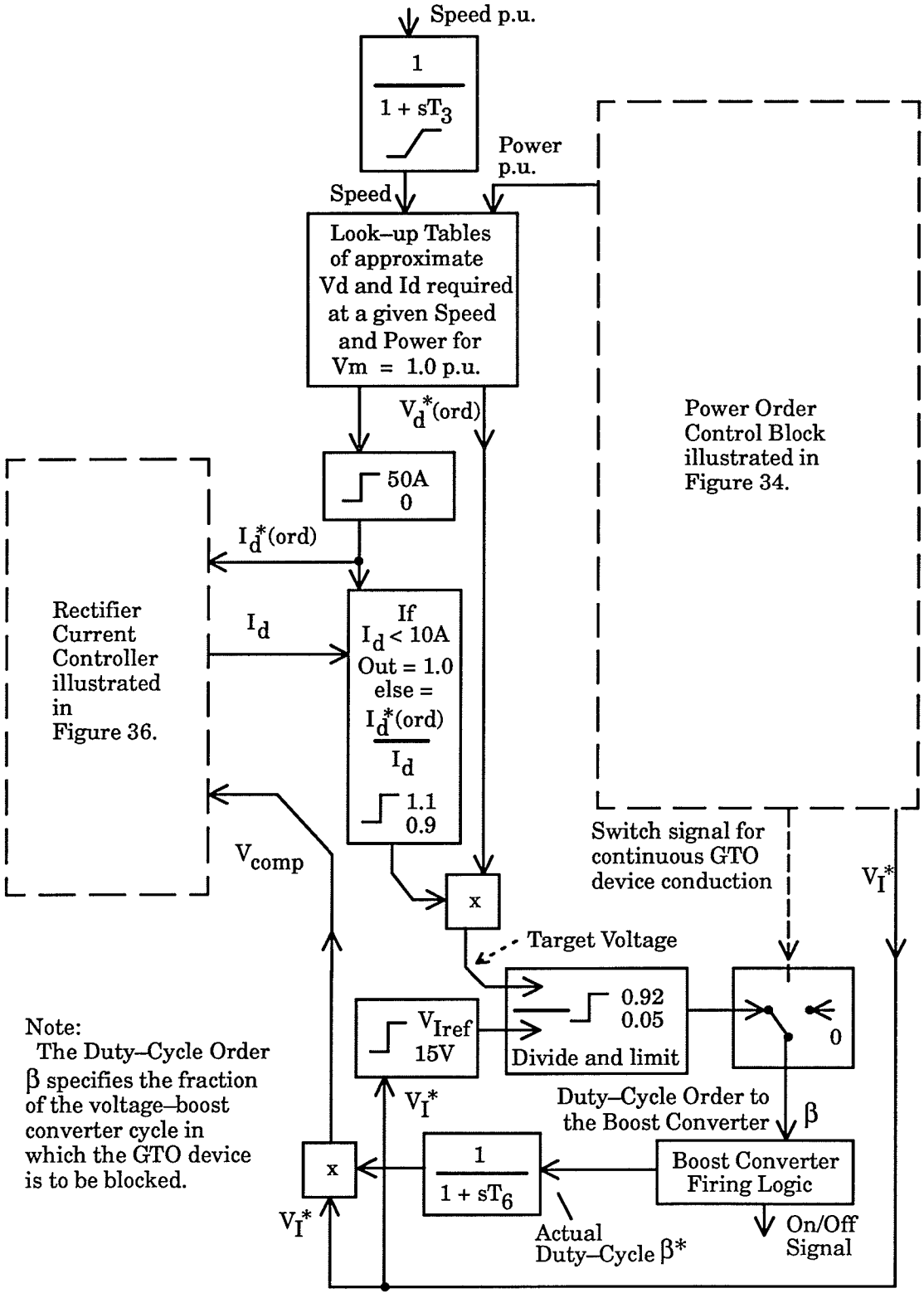


Figure 35. Look–up Tables and Voltage–Boost Converter Controller

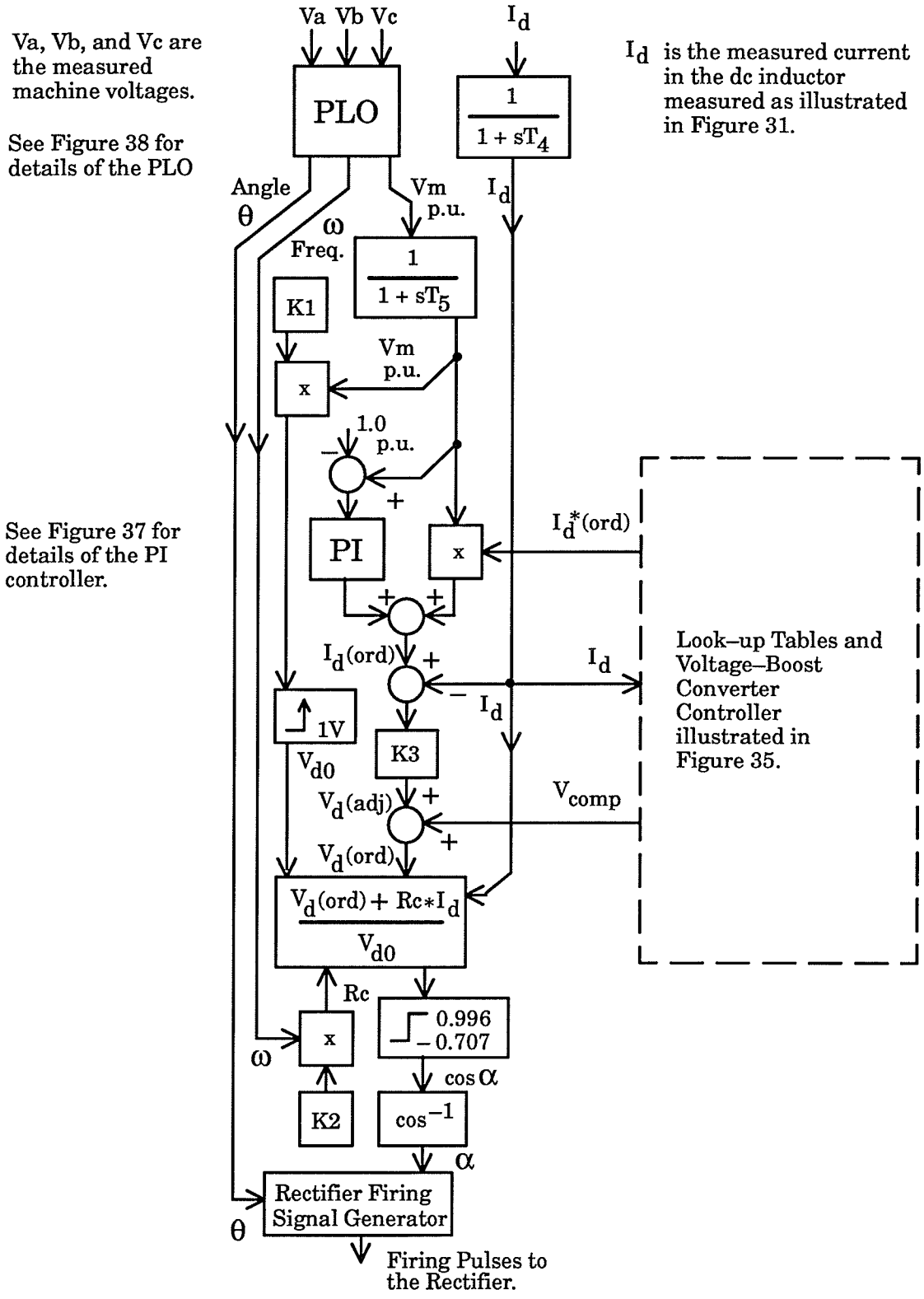


Figure 36. The Rectifier Current Controller

the load power is the product of filtered signals for V_I and I_L. The schematic for the Power Order Control Block is explained in detail in section 4.3.

Basic reference values for rectifier current order I_d*(ord) and rectifier voltage order V_d*(ord) are obtained by the control system from Look–up Tables as illustrated near the top of Figure 35. Measured machine speed and the developed power order are used as the input arguments to the Look–up Tables. The power order is provided by the Power Order Control Block as briefly described above and machine speed is measured. The Tables are based on curves of I_d*(ord) and V_d*(ord) developed as described in Chapter 2 and illustrated as in Figures 7 and 8. The Look–up Tables provide the model for the feed–forward part of the control system. The look–up of V_d*(ord) and I_d*(ord) in the digital control built for the test apparatus was accomplished by two–dimensional interpolation between points in the curves. The schematic for the Look–up Tables and Voltage–boost Converter Controller shown in Figure 35 is integrated into the Main Control schematic as shown in the center of Figure 32.

The values of I_d*(ord) and V_d*(ord) change very quickly during a sudden load change because they are both directly developed from the measured load power. In turn, the feed–forward part of the control system responds very quickly to these sudden changes in I_d*(ord) and V_d*(ord).

The current order I_d*(ord) from the Look–up Table in Figure 35 is passed to the Rectifier Current Controller as the basic dc current order. The schematic for the Rectifier Current Controller illustrated in Figure 36 is taken from the left hand side of the Main Control schematic illustrated in Figure 32. The Rectifier Current Controller is described in detail later in section 4.5.

The Voltage–Boost Converter Controller is illustrated in the lower part of Figure 35. The basic dc voltage order V_d*(ord) and the measured inverter capac-

itor voltage V_I are used by the Voltage–boost Converter Controller to develop the duty–cycle order β for the voltage–boost converter. This Controller selects the duty–cycle order β so as to cause the average voltage at the load end of the dc inductor in Figure 31 to be equal to the Target Voltage which is approximately equal to $V_d^*(ord)$. The average voltage at the load end of the inductor can be controlled in steady running because it is the product of measured V_I and the specifiable duty–cycle order β. The Target Voltage is adjusted with respect to $V_d^*(ord)$ by a factor ($I_d^*(ord) / I_d$) when the actual dc current I_d is not equal $I_d^*(ord)$. The adjustment is described in detail in section 4.4.

The Voltage–boost Converter Controller illustrated in Figure 35 also multiplies the actual duty–cycle β^* times the inverter capacitor voltage V_I to produce a compensation signal, V_{comp} for the Rectifier Current Controller. V_{comp} provides the Rectifier Current Controller with a smooth compensation signal for the actual average voltage at the load end of the dc inductor. V_{comp} is up–dated once per cycle of the voltage–boost converter (i.e. each msec. in the test apparatus). The Rectifier Current Controller, illustrated in Figure 36, uses V_{comp} as the main component of the final rectifier voltage order, $V_d(ord)$. Therefore, a sudden change in average voltage at the load end of the dc inductor due to load change will be quickly represented in V_{comp} and cause a corresponding prompt and accurate change to $V_d(ord)$. The rapid and accurate adjustment of $V_d(ord)$ prevents a large overshoot or undershoot in the dc current I_d following a sudden load change.

The two most severe load changes are full–load rejection and sudden switching on of full–load from an initially unloaded condition. Load rejection must be promptly followed by essentially continuous conduction of the GTO device in the voltage–boost converter in Figure 31 to avoid an overvoltage in V_I.

The inductance of the dc inductor is chosen to limit excursions of dc current during sudden load changes. Sudden continuous conduction of the GTO device following a load rejection causes the average voltage at the load end of the dc inductor in Figure 31 to suddenly drop to essentially zero. For the test apparatus, Figure 8 shows that the average voltage at the rectifier end of the inductor is approximately 255 volts prior to a full–load rejection (assuming operation at 1.0 p.u. speed). Load rejection therefore causes an approximate step–voltage of 255 volts to be applied to the dc inductor due to the removal of the voltage at the load end of the dc inductor. This step–voltage lasts until the rectifier output voltage is brought down by the effect of V_{comp} as described above. V_{comp} is updated every msec. in the test apparatus. However, a new firing pulse is generated for the six–pulse rectifier at 60 Hz on average only every 2.77 msec. The discrete firing times of the rectifier can thus cause delay in the reduction of the rectifier output voltage V_d.

The inductance of the dc inductor in the test apparatus was chosen so as to limit the transient change in I_d following full load rejection. As indicated in Figure 7, the dc current I_d in the test apparatus is approximately 22 Amps before full load rejection at 1.0 p.u. speed. A 100 mH dc inductor was chosen so that a nominal 255 volt step–voltage lasting 2.77 msec. would change I_d by only about 7.1 Amps. This represents an anticipated change in I_d of about one–third following full load rejection at 1.0 p.u. speed. The prompt effect of the compensation signal V_{comp} in helping the Rectifier Current Controller to control I_d makes it unnecessary to choose a larger inductance to limit the transient change in I_d. The selected 100mH inductance is also adequate for limiting dc current ripple even when rectifier delay angle approachs 90 degrees. Chapters 5 and 6 present simulation results backed up by actual test results illustrating the control of I_d during large load changes.

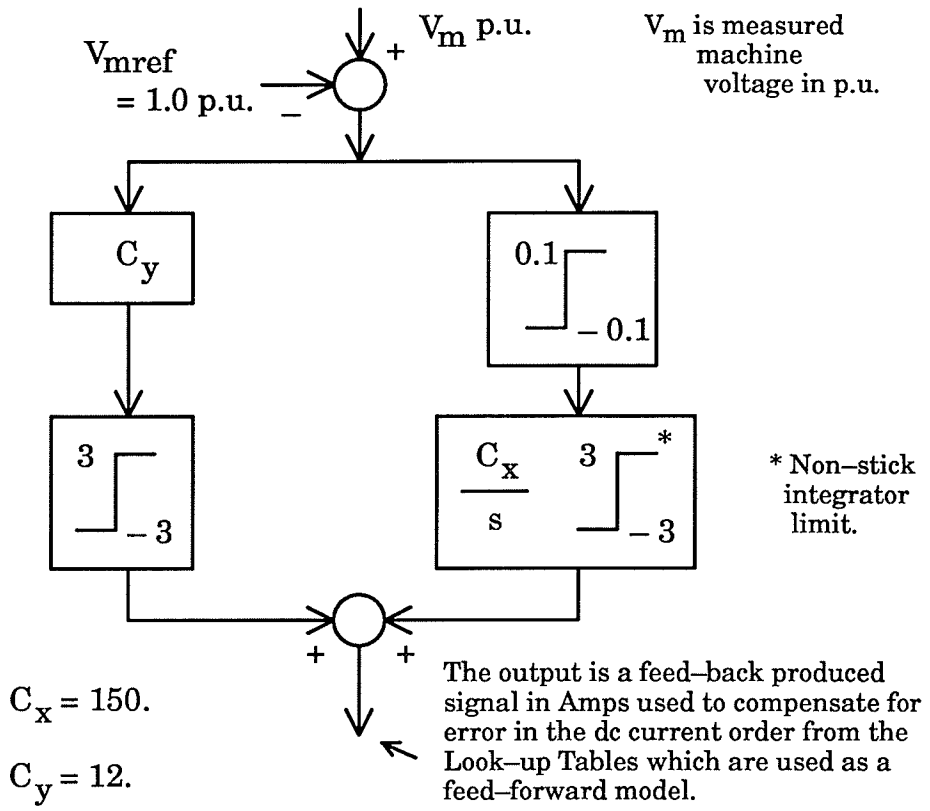
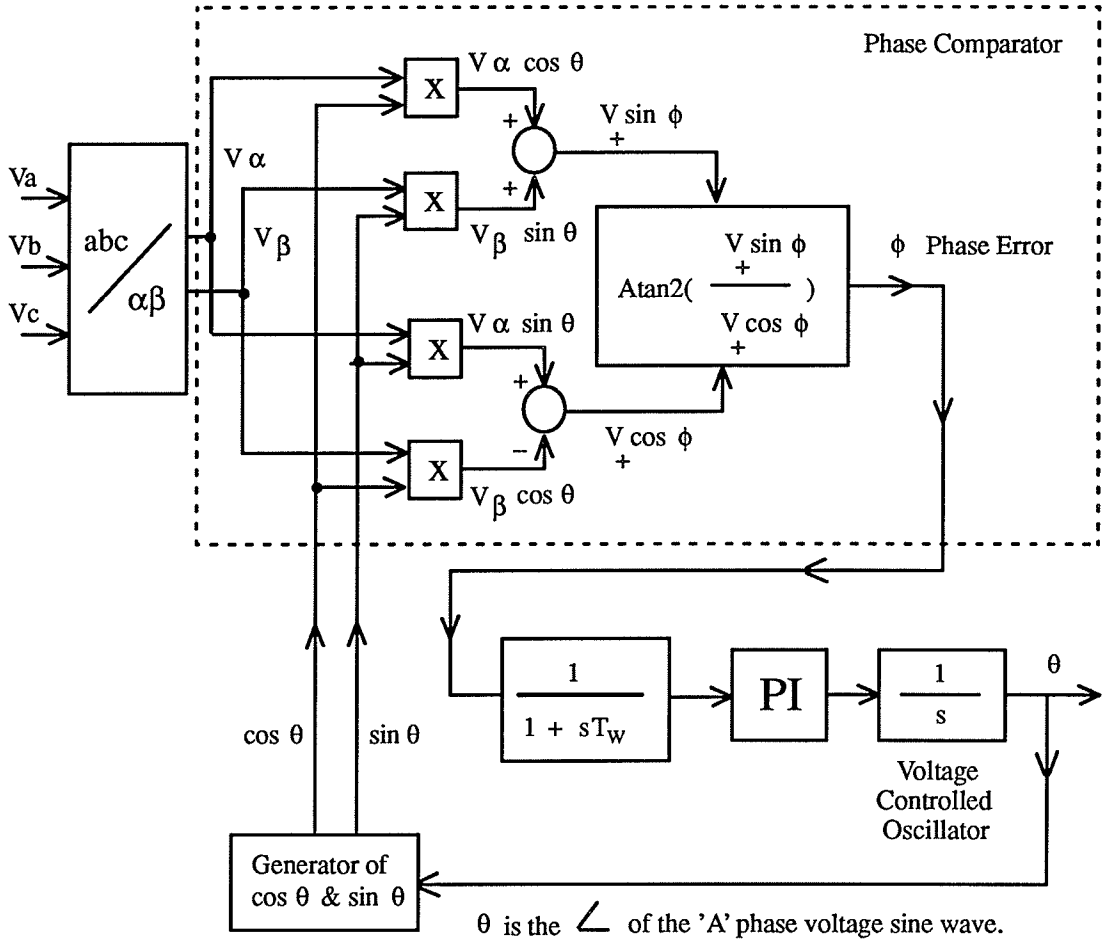


Figure 37. Machine Voltage PI Control Loop

The inverter input capacitor selected for the test apparatus is rated at 7.2 mF, not for ripple control, nor for transient response, but rather in order to select an electrolytic capacitor large enough to be rated for the large ripple current carried by the capacitor. In simulations, capacitances as low as 1.6 mF were used without degrading the system transient response.

The Rectifier Current Controller, illustrated in Figure 36, monitors the machine voltages and fires the rectifier to control dc current so as to maintain 1.0 p.u. machine voltage magnitude. The Rectifier Current Controller accepts the basic current order I_d*(ord) from the tables and modifies it to account for machine undervoltage or overvoltage as will be described in section 4.5. The modifications to the current order include adjusting the dc current order by adding a



Gains used in the test apparatus:

$T_w = 0.0015$ sec. $K_I = 1364.8$ (integral gain) $K_p = 170.6$ (proportional gain)

Characteristic Equation assuming an ideal phase comparator:

$$S^3 + A_1 S^2 + A_2 S + A_3 = 0$$

where $A_1 = 1 / T_x$

$A_2 = K_p / T_x$

$A_3 = K_I / T_x$

Roots:

$S_1 = S_2 = -329.1 + j\,0$

$S_3 = -8.41 + j\,0$

Figure 38. Flow Diagram for the Phase Locked Oscillator

component provided by a slow–acting integrator in the PI controller illustrated in Figure 37 in the Rectifier Current Controller. The added feed–back component eliminates steady running errors in machine voltage V_m which occur when the feed–forward control alone is used to determine the final dc current order.

Figure 38 contains the schematic for the phase–locked–oscillator (PLO) located at the top of Figure 36. The PLO is used to synchronize the rectifier firing pulses with the variable frequency machine voltages. The PLO and other components are described in more detail in sections 4.3 through 4.5.

4.3 The Power Order Control Block

This section gives a detailed description of the Power Order Control Block illustrated in Figure 34. The Power Order Control Block provides a power order to control the power delivered by the voltage–boost converter to the inverter dc capacitor and the inverter in Figure 31. The power order, developed for passing to the Look–up Tables in Figure 35, is determined by four contributing factors as follows:

i) the p.u. power measured in the load current branch (i.e. filtered V_I times filtered I_L in Figure 31);

ii) a contribution to the power order in p.u. developed in the proportional signal path in Figure 34 having gain $2 / V_{Iref}$(nominal), for correcting undervoltage in V_I;

iii) a contribution to the power order in p.u. developed in the integral signal path in Figure 34 having gain K4, for reducing the power–order due to overvoltage in V_I; and

iv) a speed–dependant lower limit on the power order, for preventing a final power order which would result in an duty–cycle order β between 0 and 0.05 for the voltage–boost converter.

The net power to be delivered to the inverter dc capacitor and the inverter must supply the required power to the load (i.e. I_L times V_I in Figure 31) and also regulate V_I according to V_{Iref}. As discussed above, some error between V_I and V_{Iref} is acceptable during steady running because V_{Iref} is only an intermediate signal whose value is controlled by a feedback PI controller attempting to regulate ac load voltage. The Load Voltage PI Controller is illustrated in Figure 33.

In order to develop the power order it is first necessary to measure the power to the load. Signals for V_I and I_L are filtered using low–pass single–pole filters with 2 msec. time constants (i.e. $T_1 = T_2 =$ 2 msec. in Figure 34). The purpose of filtering is to attenuate the ripple on the measured values of V_I and I_L caused by the 1.0 kHz voltage–boost converter and the twelve–pulse 60 Hz inverter. In addition to this normal low–pass filtering the maximum ramp rate of the output of the V_I filter has been limited to 75 volts/msec. This additional step is accomplished by dynamically limiting the filter input V_I to a band within plus or minus 150 Volts of the present value of the filter output V_I*, as illustrated in Figure 39. A normal ripple on V_I, which is well within the plus or minus 150 Volt band, is

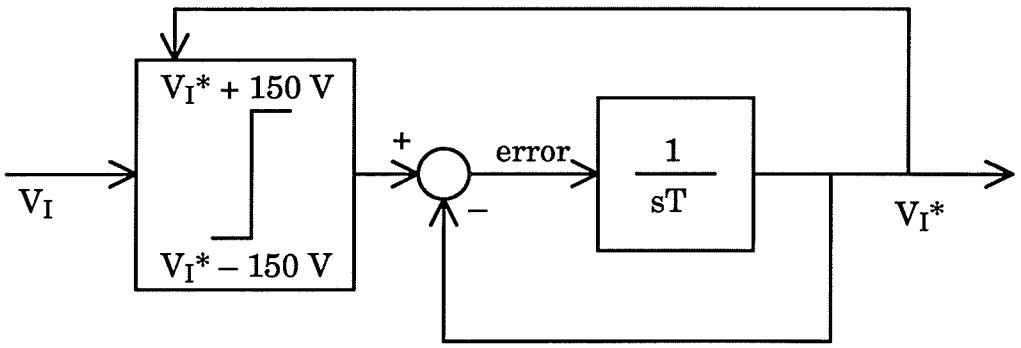


Figure 39. The V_I Filter with a Ramp–Rate Limit

filtered without any effect due to the ramp rate limit. The ramp rate limit was implemented in the V_I filter to moderate the consequences of a possible error in

analog–to–digital (A/D) conversion of V_I in the test apparatus. The benefit of the ramp–rate limit in the test apparatus is that one bad A/D conversion for V_I can cause no more than 4.2 volts of error in the filter output V_I* in the 56 μsec. before the next correct A/D conversion. The ramp–rate limit was placed on the V_I filter because the A/D converter for V_I was originally more vulnerable to electrical noise than the other A/D converters. The vulnerability to noise of the A/D converter for V_I was subsequently corrected in the test apparatus by routing the analog signal for V_I through a linear opto–isolator to separate the control system ground from the power system neutral. However, ramp–rate limiting remains a useful technique for moderating the effect of an A/D converter error for a slowly varying quantity that is sampled at a relatively high rate. In addition to V_I, the machine speed signal is also conditioned by a ramp rate limiter as described in section 4.4. Having obtained the filtered capacitor voltage V_I* and the filtered load current I_L, the measured load power in p.u. is obtained by multiplying V_I* by I_L and subsequently by the inverse of the power base as illustrated in Figure 34.

The second factor, listed above, which contributes to the power–order is the proportional signal developed in the path having gain 2 / V_{Iref} (nominal). As illustrated in Figure 34, the input to the proportional path is inverter capacitor voltage error and the output is positive when V_I is lower than V_{Iref}. The proportional gain 2 / V_{Iref} (nominal) was chosen after laboratory testing so that the power order is increased by 0.02 p.u. when V_I is 0.01 p.u. low. The contribution due to this factor is limited to between 0 and 0.12 p.u. power. The 0 limit allows a contribution only when V_I is too low. The limit of 0.12 p.u. power helps smooth the start–up transient by preventing the basic power order from being more than 0.12 p.u. larger than the actual power measured in the load.

The third factor listed above, which contributes to the power order is a power order reduction signal developed in the integrator in Figure 34 having gain K4 equal to 40. As illustrated in Figure 34, the input to the integrator is –1.0 when no overvoltage exists in V_I and the integrator output is then driven against the lower non–stick integrator limit of –0.1 p.u. power. When an overvoltage in V_I is sensed the integrator will receive an input of 1.0 and in 2.5 msec. the output of the integrator will go positive and begin to reduce the power order. The lower limit of 0 positioned after the integrator prevents a negative power order reduction. The integrator plays an important role when the load drops to a low level such as 0.02 p.u. power. This role is described below after an explanation of the fourth factor listed above.

The fourth factor listed above, which contributes to the power order is a speed–dependant lower limit on the power order. This limit, shown in Figure 34, prevents a final power order which would result in an duty–cycle order β between 0 and 0.05 for the voltage–boost converter. If the power order before the limit is negative then there is no reason to turn the GTO device "off" and in that case the duty–cycle order β and the final power order are both set to 0. Avoiding duty–cycle orders between 0 and 0.05 ensures that when the voltage–boost converter GTO device is turned "off" it will not be turned back on for at least 0.05 periods of the voltage–boost converter. This allows plenty of time for the turn–off of the GTO device to be complete before the turn–on begins regardless of the type of GTO device. A speed–dependant lower limit to the power order in the test apparatus of 0.038 + 0.125 (Speed p.u. – 0.95) avoids duty–cycle orders less than approximately 0.05.

The equation for the speed–dependant lower limit is developed for the apparatus by considering the Required Rectifier Operating Voltage curves in Figure

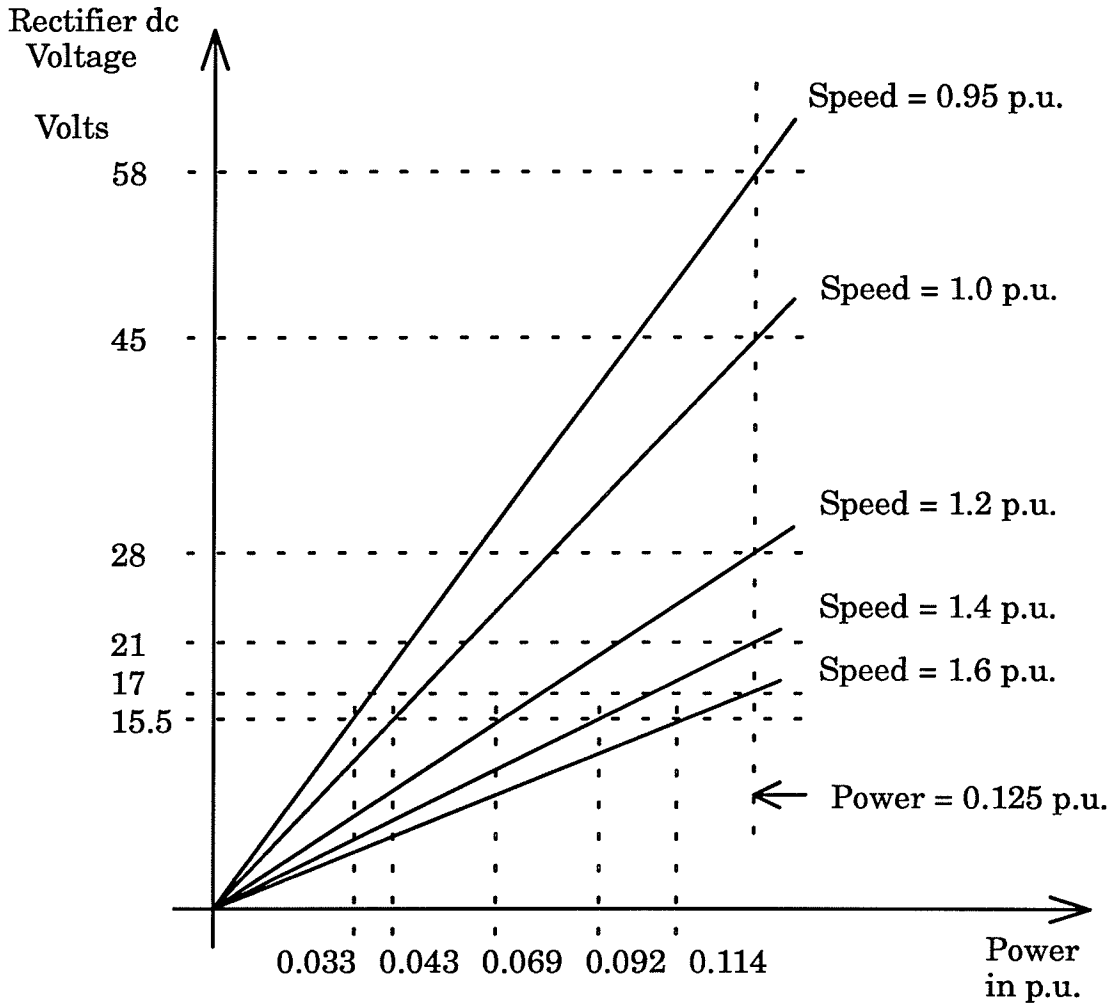


Figure 40. Required Rectifier Operating Voltages at Low Power Levels

8 at low levels of power. Average dc rectifier voltage during steady running is approximately V_I times the actual duty–cycle β^* of the voltage–boost converter. Therefore, avoiding duty–cycle orders less than 0.05 for a nominal V_I of 310 Volts corresponds to avoiding rectifier operating voltages less than 15.5 Volts during steady running. Figure 40 shows a close–up of the low–power portion of Figure 8. For each speed curve in Figure 40, the power order should be maintained sufficiently high so as to to avoid the portion of the curve below 15.5 Volts. The appropriate minimum power level for each speed curve is marked on the power axis in Figure 40. Figure 41 illustrates a curve of the minimum desired power order

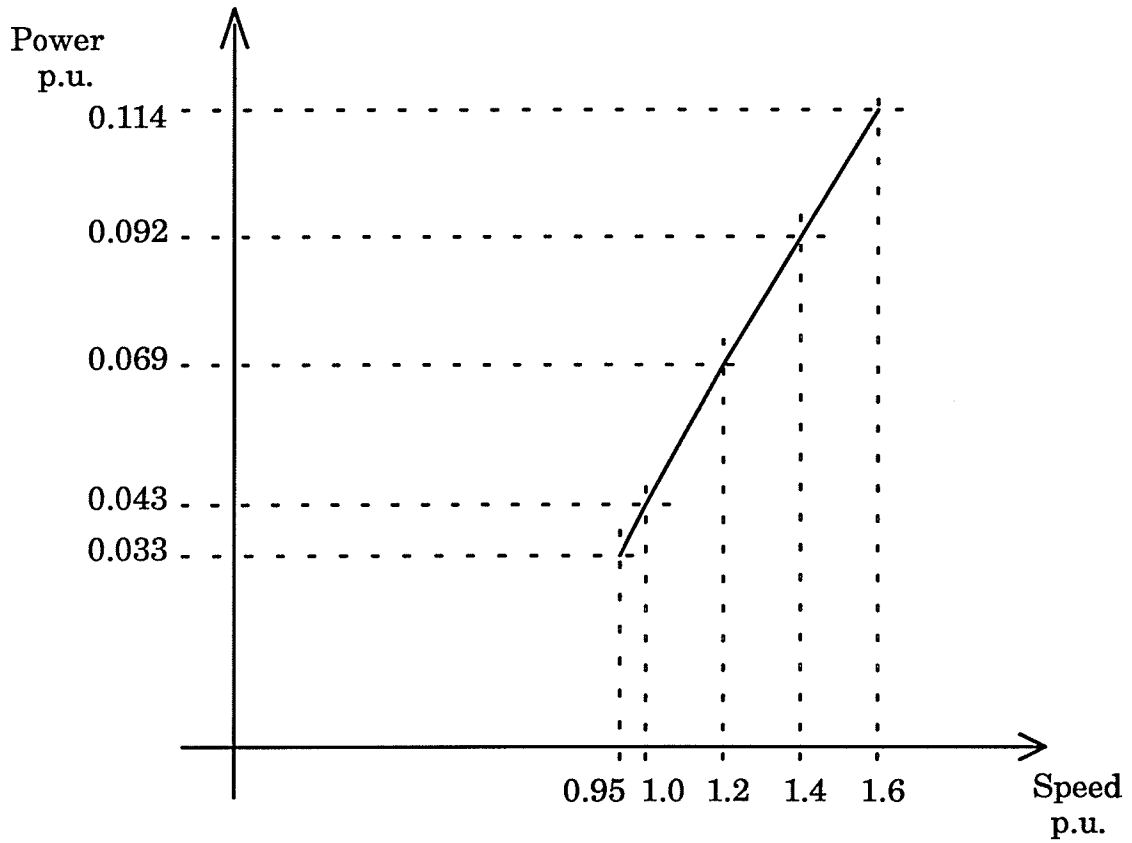


Figure 41. Minimum Desired Power Order versus Speed

versus speed for the test apparatus. The expression for the power order lower limit, 0.038 + 0.125 (Speed p.u. – 0.95), is a straight line approximation to the curve in Figure 41 derived from Figure 40 by plotting minimum desired power versus speed. Using this expression as the speed–dependant lower limit for the power order avoids rectifier operating voltages less than 15.5 Volts and thus duty–cycle orders between 0 and 0.05. Hard limits are placed on the duty–cycle order in the Voltage–boost Converter Controller so as to prevent duty–cycle orders between 0 and 0.05 during transient conditions.

As mentioned above, the integrator with gain K4 illustrated in Figure 34 plays an important role when the measured load power drops to low levels such as 0.02 p.u. power. The lower limit on the power order is then generally active

and holds the power order slightly higher than the measured load power. That higher power order can cause the inverter capacitor voltage V_I to slowly drift upward. The integrator intervenes to prevent the overvoltage in V_I which otherwise could occur.

The most rapid drift upward in V_I occurs for the highest I_d which in turn occurs during operation at the highest speed. In the test apparatus the highest I_d of 40 Amps occurs at low power and high speed as shown in Figure 7. The average current passed to the inverter capacitor is equal to the actual duty–cycle β^* times I_d. If the load current I_L is negligibly small then the maximum average current charging the capacitor in the test apparatus in these circumstances is 0.05 times 40 Amps or 2 Amps. The dc capacitor in the test apparatus is rated at 7.2 mF and therefore the fastest drift upward in V_I is 2 Amps / 7.2 mF = 0.277 Volts/msec.

As discussed above the integrator responds to overvoltage in 2.5 msec. and begins to create a power order reduction. The integrator response time of 2.5 msec. is very acceptable in view of the rather slow maximum drift rate for V_I of 0.277 Volts/msec. For low load powers (e.g. 0.02 p.u.), the power order reduction created by the integrator eventually causes a negative power order to exist ahead of the lower limit (e.g. 0.038 + 0.125 (Speed p.u. – 0.95)) applied to the power order. The Rectifier Current Controller replaces such a negative power order with a zero final power order and a zero duty–cycle order β as noted above. The zero duty–cycle order β causes the GTO device in the voltage–boost converter to conduct continuously.

The integrator (gain K4 = 40 in Figure 34) can also cause a power order reduction to remove overvoltage in V_I during operation when the power order is

above its lower limit. Such a reduction may be required if the measurement of load power is erroneously higher than the actual load power.

The function of the Power Order Control Block illustrated in Figure 34 is summarized briefly as follows. The Power Order Control Block creates a power order, for passing to the Look–up Tables, which specifies the power required to supply the load and regulate V_I. The control avoids power orders which would lead to duty–cycle orders between 0 and 0.05. When the voltage–boost converter GTO device should not be turned "off" then the power order is set to zero and a signal is sent to the Voltage–boost Converter Controller to cause continuous conduction of the GTO device.

4.4 The Look–up Tables and Voltage–boost Converter Controller

This section gives a detailed description of the Look–up Tables and the Voltage–boost Converter Controller illustrated in Figure 35. The Look–up Tables are located at the top of the schematic in Figure 35 and the Voltage–boost Converter Controller is located below the tables.

The Look–up Tables provide outputs I_d*(ord) and V_d*(ord) based on the power order provided by the Power Order Control Block and the measured machine speed. In the test apparatus, machine speed is determined by measuring the time required for the machine shaft to turn one–quarter turn. Speed is the inverse of the quarter–turn rotation time multiplied by an appropriate scaling factor. A slotted disk and an light beam are used to sense the quarter turns. The speed signal is filtered, as illustrated in Figure 35, using a filter with a time constant of T_3 = 33.0 msec. A ramp rate limit of 1.5 p.u. speed/sec. is included in the machine speed filter in the test apparatus using the method illustrated in Figure 39. This ramp rate limit limits the possible introduction of error to 1.25

percent in 8.333 msec. which is the time it takes the shaft to turn a quarter turn at 1.0 p.u. speed.

Extracting I_d*(ord) and V_d*(ord) from the Look–up Tables requires two–dimensional interpolation between points in the curves illustrated respectively in Figures 7 and 8. The quantities I_d*(ord) and V_d*(ord) are approximate values for the required average rectifier dc current and dc voltage which would supply the ordered power and cause the machine voltage to be held at 1.0 p.u. voltage. I_d*(ord) is provided to the Rectifier Current Controller as the basic dc current order. Similarly V_d*(ord) provides the basis for the duty–cycle order β produced by the Voltage–boost Converter Controller. The duty–cycle order β is selected so as to control the voltage at the load end of the dc inductor to a Target Voltage. In steady running the rectifier output voltage is approximately equal to the voltage at the load end of the dc inductor.

The product of I_d*(ord) and V_d*(ord) out of the Look–up Tables is always equal to the required power order used as an input to the Look–up Tables. If I_d*(ord) differs from the measured I_d then the Target Voltage for the voltage at the load end of the dc inductor is V_d*(ord) multiplied by a limited proportional factor I_d*(ord)/I_d, as illustrated in Figure 35. The adjustment to V_d*(ord) is made so that the ordered power can reach the load. The value of I_d during steady running may be slightly different from I_d*(ord) due to error in Figure 7 and 8 curves. The Rectifier Current Controller (discussed in detail in section 4.5 below) contains a PI controller which adjusts I_d to correct for steady running errors and bring machine voltage V_m to 1.0 p.u. voltage. The limits of 0.9 and 1.1 for the I_d*(ord)/I_d factor, illustrated in Figure 35, reflect a maximum acceptable error in the curves of plus or minus 10 percent. Laboratory test results presented in

Chapter 6 verify that the limits of 0.9 and 1.1 provide good operation for the full range of steady running conditions.

As illustrated in Figure 35, the duty–cycle order β is determined by dividing the Target Voltage (i.e. V_d*(ord) times a limited value I_d*(ord)/I_d) by the measured inverter capacitor voltage V_I* in the Divide and Limit block. Calculation of the duty–cycle order β in this way causes the average voltage at the load end of the dc inductor to be equal to the Target Voltage when limits are not active. In steady running the upper limit of 0.92 in Figure 35 will not be active in the test apparatus because the highest rectifier output voltage in Figure 8 (270 Volts) divided by the nominal inverter capacitor voltage (310 Volts) is only 0.87. The corresponding lower limit of 0.05 will not be active in steady running because the Power Order Control Block avoids power orders which would result in duty–cycle orders between 0 and 0.05 as discussed in the preceding section. The upper limit of 0.92 p.u. on the duty–cycle order prevents very short GTO device conduction times.

A selector for the final duty–cycle order β is located after the Divide and Limit block. As discussed in section 4.3, when the Power Order Control Block sets the final power order to zero then it also sends a signal to the Voltage–boost Converter Controller to select a final duty–cycle order β which is also equal to zero. In any other case the selected duty–cycle order β remains the quotient from the Divide and Limit block.

The Voltage–boost Converter Firing Logic block, illustrated in Figure 35, converts the duty–cycle order to an on/off square wave signal. The on/off signal is provided by a fibre optic link directly to the GTO gate–firing board in the test apparatus to control the GTO device conduction state. In the test apparatus the voltage–boost converter frequency was chosen as 1.0 kHz in order to provide a

design which could accommodate a broad range of GTO devices. The period of the voltage–boost converter in the test apparatus is thus about 1.0 msec. The digital signal processor (DSP) in the test apparatus performs all calculations indicated in the Main Control schematic (Figure 32) at least once each 56 μsec. which is the control calculation time–step. However, the on/off square wave signal for the boost converter is adjusted six times in each 56 μsec. control time–step in order to provide increased accuracy in the on/off GTO device firing times. The maximum error in firing times introduced by up–dating the on/off signal at this rate is therefore plus or minus 1/12 of 56 μsec.

As discussed above in the General Description, the Voltage–boost Converter Controller also provides a compensation signal V_{comp} to the Rectifier Current Controller. V_{comp} is approximately equal to the average voltage at the load end of the dc inductor. This signal is developed by multiplying the filtered dc capacitor voltage V_I* times the filtered value of the actual duty–cycle β*. The actual duty–cycle β* is used because it is essentially a dc quantity which is updated once per period of the voltage–boost converter. The 2.0 msec. filter (T_6 = 2 msec.) on the β* signal is included to smooth step changes in the β*signal. The smoothing of the β* signal also gives persistence to the V_{comp} signal when the apparatus is very lightly loaded. For very light loads the actual duty–cycle β* is non–zero only occasionally and then only for one voltage–boost converter period at a time. Providing added persistence to the V_{comp} signal causes it to participate more effectively in determining rectifier valve firing times at these low power levels.

The function of the Look–up Tables and Voltage–boost Converter Controller are summarized briefly as follows. The Look–up Tables accept inputs of machine speed and power order and provide I_d*(ord) and V_d*(ord). I_d*(ord) is an approxi-

mation of the required dc current at the given speed and power. I_d*(ord) is passed to the Rectifier Current Controller as an approximate dc current order. V_d*(ord) is an approximation of the required dc voltage at the given speed and power. The Voltage–boost Converter Controller controls the duty–cycle order of the voltage–boost converter so as to cause the voltage at the load end of the dc inductor to be equal to the Target Voltage which is equal to approximately V_d*(ord). The Voltage–boost Converter Controller also provides the Rectifier Current Controller with a signal V_{comp} which represents the actual voltage at the load end of the dc inductor. The Rectifier Current Controller described in the next section uses I_d*(ord) and V_{comp} in controlling I_d so as to control machine voltage V_m to 1.0 p.u. voltage and provide the necessary power to the load.

4.5 The Rectifier Current Controller

This section gives a description of the Rectifier Current Controller illustrated in Figure 36. The reasoning behind the multiplication of the basic dc current order I_d*(ord) by V_m in Figure 36 is given in detail in Subsection 4.5.1. Subsection 4.5.2 gives a full explanation of the gains and limits of the PI controller. Subsection 4.5.3 describes the details of the phase–locked–oscillator (PLO).

The Rectifier Current Controller as implemented requires certain information from the system in order to function. The PLO (discussed in section 4.5.3) located as shown near the top of Figure 36 provides a signal describing the angle θ of the positive–sequence A–phase sine–wave of machine voltage. The angle θ is used by the Rectifier Current Controller as a reference angle for firing the rectifier. The PLO also provides a measurement of frequency ω in radians/sec. which is used in Figure 36 to calculate the commutation resistance R_c in ohms according to Eqn 41. The PLO also provides a measurement of machine voltage V_m in p.u. ac voltage. The machine voltage is filtered using a low–pass

$$R_c = \omega \times (K2) \qquad \text{Eqn. 41}$$

where $K2 = 3\ L_c / \pi$

and L_c is the commutation inductance in Henries.

single–pole filter with time constant T_5 = 4 msec. as shown in Figure 36. The dc current I_d is also measured and filtered using a low–pass single–pole filter with time constant T_4 = 4 msec. as shown.

It may be possible to substitute cosine firing control in place of the PLO based rectifier firing system. Cosine firing control also provides a control which implements a dc voltage order such as V_d(ord) in order to control the rectifier output voltage. This alternate approach has not been tested. It may also be possible to use a PLO based on detection of zero crossings of voltage. This approach has also not been tested. The Transvektor [25][26] type PLO used in this apparatus is discussed in section 4.5.3.

The Rectifier Current Controller creates a final dc current order I_d(ord) consisting of two parts. The first part is the product of V_m times the basic current order I_d*(ord) from the Look–up Tables. The second part is the output of a PI controller located as shown in Figure 36. The creation of these two components of the final dc current order is the topic of sections 4.5.1 and 4.5.2.

When the measured dc current I_d is subtracted from the final dc current order I_d(ord) the resulting error is multiplied by the proportional factor K3 in Figure 36 and added to V_{comp} to provide the final dc voltage order V_d(ord). V_{comp} is provided by the Voltage–boost Converter Controller as discussed above and represents the average dc voltage at the load end of the dc inductor. K3 is chosen as 7.5 volts/amp in the test apparatus in order that the rectifier dc voltage order V_d(ord) will be 7.5 volts higher than V_{comp} for each Amp of dc current error. The

resulting voltage applied to the 100 mH dc inductor in the test apparatus removes dc current error with a time constant of 13.3 msec. The final dc voltage order V_d(ord) is used to determine the rectifier firing delay angle α.

The Rectifier Current Controller functions by solving Eqn. 1 for cos(α) as shown in Figure 36. All other quantities in Eqn. 1 are obtained for this purpose. I_d is measured as mentioned above. Commutation resistance R_c is developed from ω as described above. V_{d0} is obtained from V_m according to Eqn. 2. The final dc voltage order V_d(ord) is obtained as described above. Limits are applied so as to limit cos α between cos 5 degrees and cos 135 degrees. An arccosine look–up table is used to provide α in the test apparatus. The Rectifier Firing Signal Generator shown in Figure 36 uses θ and α to determine which thyristors receive firing pulses at a given time. In the test apparatus firing pulses are adjusted twice in each 56 μsec. calculation time–step period. In addition, the angle θ is phase advanced by an angle equal to 1/4 of the calculation time–step times the VCO frequency. This phase advance causes the firing time error due to the discrete time–step size to be at worst between 14 μsec. early and 14 μsec. late rather than between 0 μsec. early and 28 μsec. late. The next three subsections give necessary details for explaining and implementing the Rectifier Current Controller.

4.5.1 Multiplication of the Basic Current Order by p.u. Machine Voltage

As illustrated in Figure 36, the basic current order I_d*(ord) received by the Rectifier Current Controller is multiplied within the controller by p.u. machine voltage V_m. The basis for this multiplication is explained below.

Arrillaga and Watson [8] have provided a diagram for estimating the voltage of a self–excited induction machine under no load at a given frequency as illustrated in Figure 42. In Figure 42 I_c is the self–excitation capacitor characteris-

tic; I_m is the machine magnetizing characteristic; and point A is a stable operating point. Arrillaga and Watson have also illustrated the effect caused by loading a self–excited induction machine with a constant magnitude purely reactive ac current I_{XL} as shown in Figure 43. A purely reactive ac current I_{XL} of essentially constant magnitude is drawn by an unloaded rectifier under constant current control as illustrated in Figure 44. The slope of the capacitor characteristic I_c in Figure 43 is reduced as compared to the slope in Figure 42 because a larger capacitor is chosen to also supply the purely reactive ac current I_{XL}. Arrillaga and Watson have noted that point D in Figure 43 is inherently unstable as an operating point. As part of the present research it has been noted that

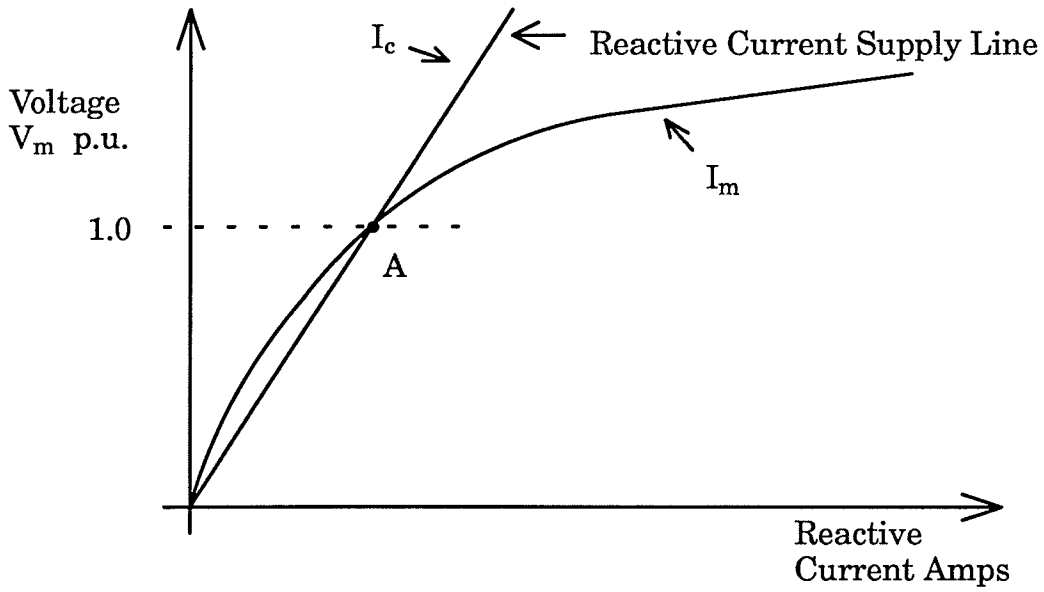


Figure 42. Curves for an Induction Machine Excited by Capacitors

point D can be made stable if the purely reactive ac current I_{XL} (determined originally for 1.0 p.u. machine voltage) is not held constant but is instead multiplied by p.u. machine voltage V_m. The effect of the multiplication is illustrated in Figure 45. The scaling of the reactive ac current I_{XL} according to V_m causes the Effective Reactive Current Supply Line in Figure 45 to be the same as the Reactive

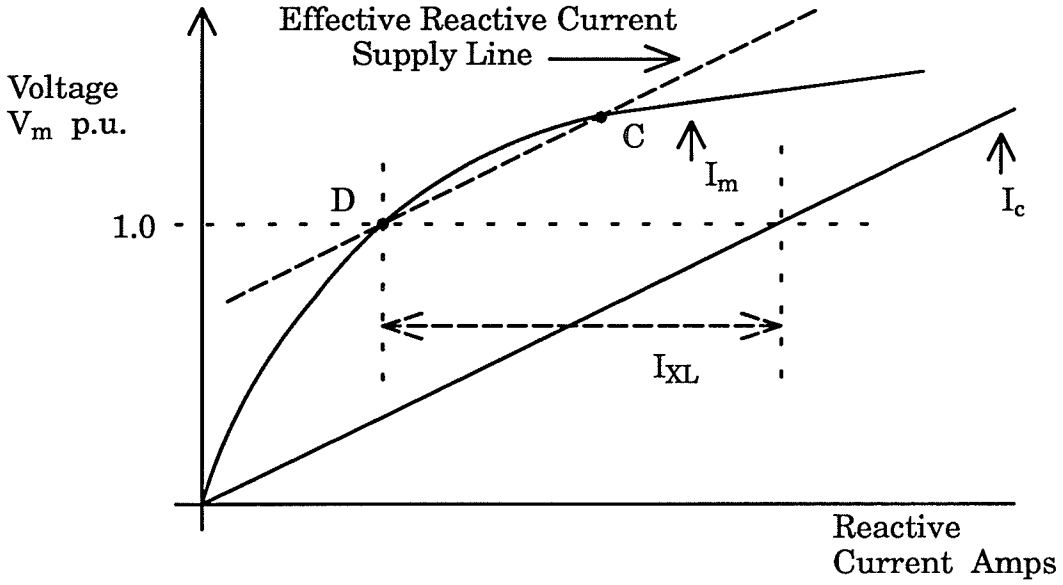


Figure 43. Curves for an Induction Machine Excited by Capacitors and Loaded with a Constant Reactive Load Current

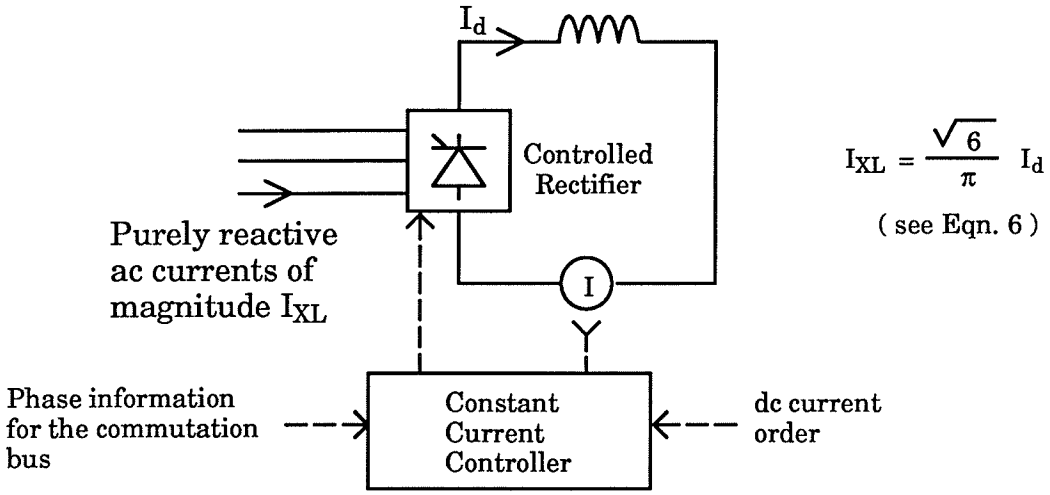


Figure 44. A Rectifier Providing Constant Magnitude ac Current Loading

Current Supply Line in Figure 42. Point B in Figure 45 is therefore a stable operating point for the same reasons that point A in Figure 42 is described by Arrillaga and Watson as a stable operating point.

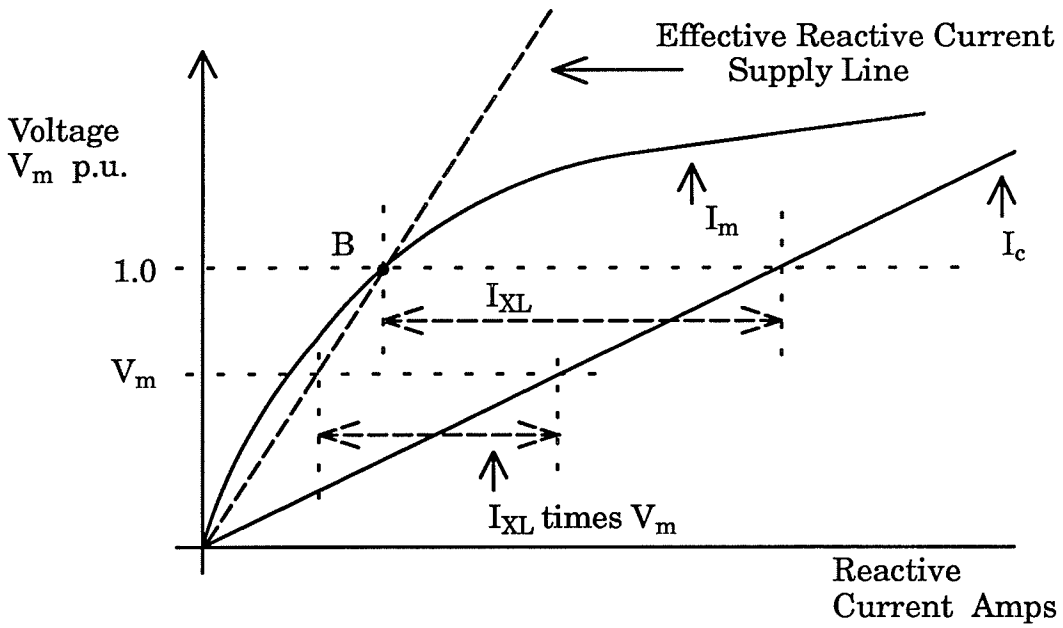


Figure 45. Curves for an Induction Machine Excited by Capacitors and with a Voltage Scaled Reactive Load Current

In the thesis apparatus the ac current drawn by the rectifier under no load conditions is almost purely reactive ac current. I_d*(ord) from the Look–up Tables describes the required rectifier dc current at 1.0 p.u. machine voltage as explained in chapter two. In turn, the purely reactive ac current I_{XL} in Figure 45 corresponds to 0.780 times I_d*(ord) for the unloaded thesis apparatus according to Eqn. 6. Therefore, an Effective Reactive Current Supply Line and operating point B are established for the unloaded thesis apparatus as shown in Figure 45 when I_d is controlled according to I_d*(ord) times V_m p.u. machine voltage.

On the other hand, when the rectifier draws both real and reactive ac current, then multiplication of I_d*(ord) by V_m p.u. voltage causes the rectifier reactive component of ac current I_{react} to change by more than the factor V_m p.u. voltage. Figure 46 illustrates the increase in I_{react} from $I_{react}(1)$ to $I_{react}(2)$ that occurs when I_d is increased according to a factor K during constant–power operation with constant V_m. As shown in Figure 46, the multiplication of I_d by the factor K causes the reactive current $I_{react}(2)$ to be larger than K times $I_{react}(1)$.

When the factor K is the voltage V_m then an increase in V_m during constant-power operation causes I_{real} to decrease rather than hold constant as shown in Figure 46. Therefore the change in I_{react} due to multiplication of I_d by V_m p.u. voltage is even more pronounced than when I_d is multiplied by a constant factor K.

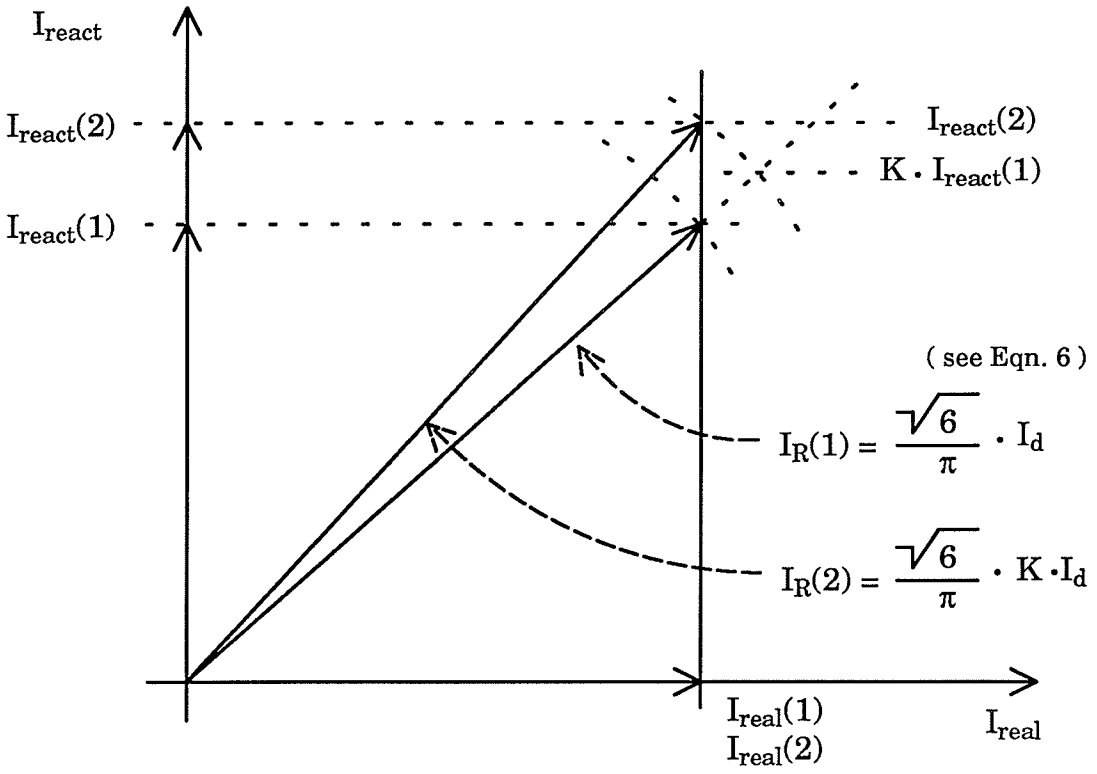


Figure 46. The Effect of Scaling dc Current by a Factor K for Constant Real Load

As explained above with reference to Figure 46, multiplication of I_d*(ord) by V_m p.u. machine voltage in the presence of real rectifier ac current causes the reactive current I_{react} drawn by the rectifier to change by more than the multiplying factor V_m. The effective reactive current supply line can thus qualitatively be represented as illustrated in Figure 47 for a given combination of real power and machine speed. The Effective Reactive Current Supply Line in Figure 47 intersects the Machine Magnetizing Characteristic at an angle closer to the

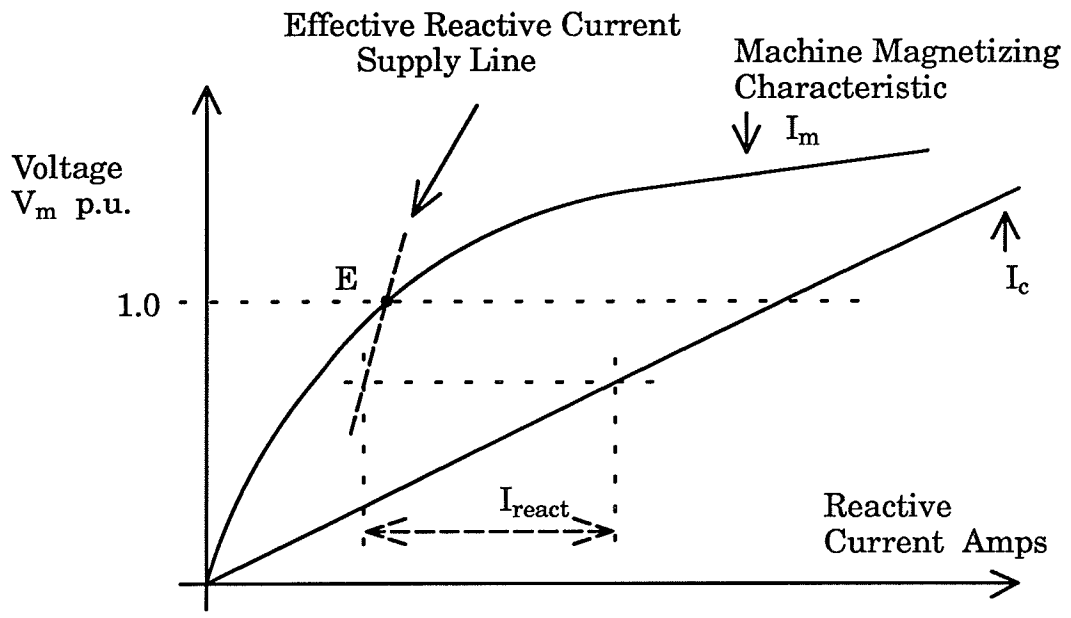


Figure 47. The Qualitative Change to the Effective Reactive Current Supply Line due to Constant Real Load

perpendicular than in Figure 45. The presence of a real component of rectifier ac current is therefore a stabilizing influence on the magnitude of V_m when I_d*(ord) is multiplied by V_m.

The stabilizing influence of real rectifier ac current was demonstrated in the laboratory. The apparatus was tested using a dc current order of V_m times I_d*(ord). In the test the PI block in the Rectifier Current Controller was not permitted to contribute to the final dc current order I_d(ord). V_m remained stable in magnitude for speeds below about 1.2 p.u. speed during no–load operation with the final dc current order I_d(ord) developed in this way. However, small oscillations in both V_m and I_d began at approximately 1.2 p.u. speed during operation under no load. These oscillations occur because at high speed the operating point, such as point B in Figure 45, moves into a very lightly saturated portion of the magnetizing curve and the operating point starts to become unstable. The oscillations at 1.2 p.u. speed were eliminated by applying approximately 0.35 p.u. load to the apparatus. A further increase in speed brought the oscillations

back and a subsequent increase in load again eliminated the oscillations. These laboratory observations support the conclusion drawn above that real load stabilizes the machine voltage V_m when V_m is used as a multiplier for I_d*(ord).

The use of V_m p.u. times I_d*(ord) as the final dc current order is by itself inadequate because it results in steady state error in V_m and the oscillations described above. The PI controller illustrated in Figure 37 adds a component to the current order in the Rectifier Current Controller so as to bring V_m to a stable 1 p.u. voltage. The component added by the integrator in the PI controller is able to correct for both error in I_d*(ord) obtained from the Tables as well as steady running error between the final dc current order I_d(ord) and actual I_d. The PI controller in the Rectifier Current Controller is described in the next subsection.

4.5.2 The PI Controller in the Rectifier Current Controller

The PI controller illustrated in Figure 37 has been designed for two purposes. The proportional part of the PI controller modifies the Effective Reactive Current Supply Characteristic discussed above so as to remove oscillations in the magnitude of V_m in the full ranges of speed and power. The slow acting integral part of the PI controller responds to steady running error in V_m so as to cause an I_d which will bring V_m to 1 p.u. voltage. The limits on the output of the proportional and integral parts of the PI controller make sure that neither part can create a component of dc current order larger than about 10 % of the maximum dc current order.

As noted in the preceding subsection, when the PI controller in the Rectifier Current Controller is disabled, the machine voltage magnitude V_m oscillates when the apparatus is operated at high speed and no load. Reduction of speed or increase in load tends to stabilize V_m for reasons also discussed above. The most unstable condition of high speed (e.g. 1.4 p.u. speed) and no–load is there-

fore used as the base case for designing the proportional part of the PI controller illustrated in Figure 37. The operating point E in Figure 47 was concluded in the preceding subsection to be a more stable operating point than point B in Figure 45 because in Figure 47 the Effective Reactive Current Supply Line intersects the machine magnetizing curve at an angle closer to the perpendicular. The approach taken in designing the proportional part of the PI controller is therefore to cause an Effective Reactive Current Supply Line which similarly intersects the machine magnetizing curve at an angle closer to the perpendicular for high–speed no–load conditions.

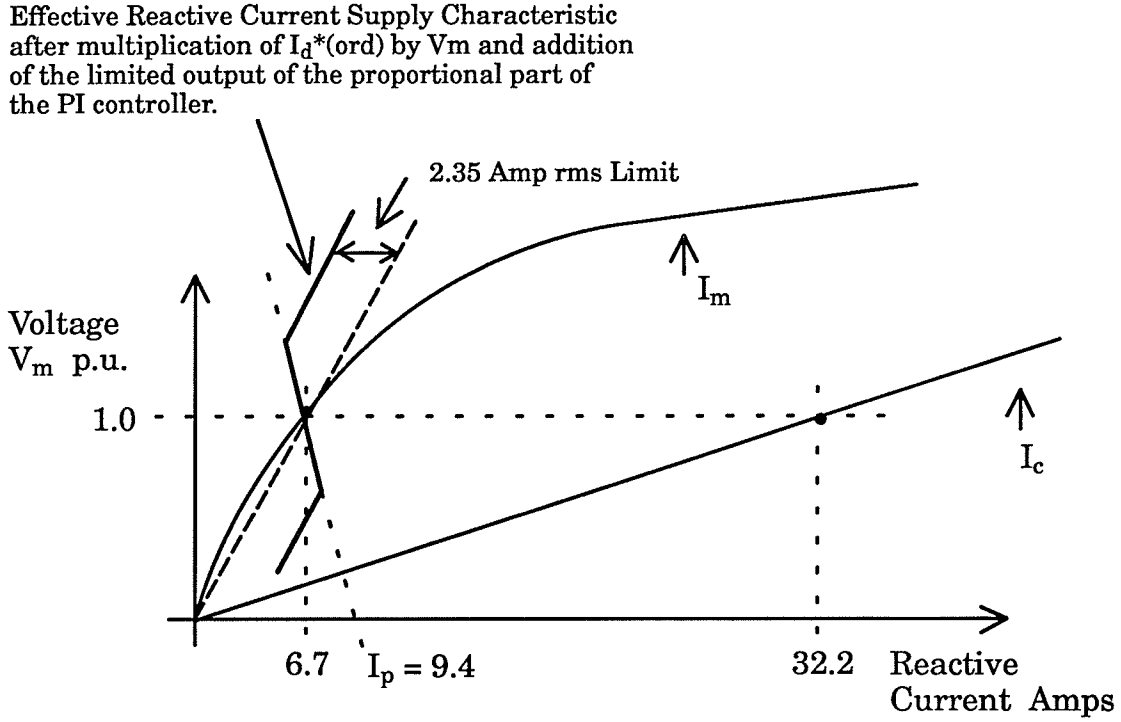


Figure 48. The Effect of the Limited Proportional Control on the Effective Reactive Current Supply Characteristic

Based on the data developed for the test apparatus in chapter two, it is known that the ac frequency of the machine is 1.397 p.u. during operation at 1.4 p.u. machine speed, 1 p.u. voltage V_m, and no load. The excitation capacitor reac-

tance and machine magnetizing reactance at this frequency are respectively about 3.72 ohms and 18.0 ohms. These reactances correspond to a line current to the delta–connected excitation capacitors of 32.2 Amps and a magnetizing current to the machine of 6.7 Amps for operation at 1 p.u. machine voltage as illustrated in Figure 48.

In Figure 45 the Effective Reactive Current Supply Line passes through the operating point B and the origin due to multiplication of I_d*(ord) by V_m in p.u. voltage. The proportional part of the PI controller in Figure 37 further modifies the reactive current supply characteristic as illustrated in Figure 48. Proportional gain C_y shown in Figure 37 is calculated as follows for the value of I_p illustrated in Figure 48.

$$C_y = \frac{I_p \text{ Amps rms}}{(0.78)(1 \text{ p.u. voltage error})}$$

$$= 12.0$$

An I_p of 9.4 Amps shown in Figure 48 causes a large increase in the angle that the Effective Reactive Current Supply Characteristic makes with the Machine Magnetizing Characteristic. The factor of 0.78 above (from Eqn. 6) converts the necessary change in rectifier reactive ac current illustrated in Figure 48 into the corresponding change in the dc current order. The 3.0 Amp limit on the output of the proportional branch in Figure 37 is the dc limit corresponding to the maximum permitted change in rectifier reactive ac current due to the proportional branch of 2.35 Amps as illustrated in Figure 48.

The integrator in Figure 37 is provided to modify the final dc current order to correct steady running error in V_m. As mentioned above it is anticipated that steady running errors could cause I_d*(ord) from the Tables to differ by approxi-

mately 10 % from the final dc current order I_d(ord). The limits of +3.0 and –3.0 Amps on the integrator output in Figure 37 correspond to plus or minus 10 % of the dc current order at 1.4 p.u. speed. The limits of plus or minus 0.1 p.u. voltage on the input to the integrator and the integrator gain of 150.0 allow the integrator to slowly adjust the dc current order to eliminate errors in V_m. The integrator input limits and the gain allow the integrator output to move from zero to an output limit in 200 msec. when an input limit is active.

The magnitude of the output limits on the proportional part of the PI controller have been chosen to be equal to the limits on the output of the integral part. The magnitude of these identical limits is chosen so that during transients a 0.1 p.u. change in V_m can cause the proportional part of the PI controller to completely offset the output of the integrator. Such an offset is appropriate in the event that the integrator output needs to recover from being close to a wrong limit.

The PI controller was added to the Rectifier Current Controller after the apparatus was implemented in the laboratory and tested. In earlier transients simulations machine voltage V_m remained very close to 1 p.u. voltage without the presence of the PI controller during operation over the full range of machine speed. The very accurate feed–forward control of V_m in the transients simulations can be attributed to the fact that the apparatus in the simulations is exactly that specified by the apparatus parameters used for calculating the curves in Figures 7 and 8. The curves therefore provide a nearly ideal feed–forward control model when used in the transients simulations. It is therefore to be expected that the feed–forward control operates very well by itself in transients simulations. However, the actual apparatus differs to a minor degree from the theoretical model described by the parameters and the curves. For instance, the actual machine hysterisis is only approximately modelled by a constant resistance at

the machine terminals. Furthermore, the model used for calculating the curves in Figures 7 and 8 is based on one saturation curve measured at a single frequency of 60 Hz. Many other possible sources of minor inaccuracy could be listed. In the actual apparatus the error in V_m was very small at 1 p.u. speed even without the PI controller. However, the error in V_m became significant in the actual apparatus without the PI controller when the machine speed was increased to higher speeds. For instance, the machine voltage V_m oscillated slightly in magnitude around 0.82 p.u. voltage during operation at 1.4 p.u. speed under no load. This steady running error in V_m confirms that an integrator is required in the Rectifier Current Controller in order to produce a final dc current order which causes V_m to settle to 1.0 p.u. voltage.

In summary, the PI controller in the Rectifier Current Controller stabilizes V_m in two ways. The proportional part of the PI controller removes oscillations in V_m by essentially modifying the Effective Reactive Current Supply Characteristic as illustrated in Figure 48. The integral part of the PI controller provides a component to the final dc current order I_d(ord) to overcome steady running errors and cause V_m to settle to 1.0 p.u. voltage.

4.5.3 The Phase–Locked–Oscillator

The signal flow diagram for the phase–locked–oscillator (PLO) used in the test apparatus and in the simulations is illustrated in Figure 38. The PLO is based on the Transvektor type PLO [25]. Three minor modifications have been made as compared to the PLO described in reference [26].

In reference [26] the error signal ϕ, describing the angle by which the voltage Va leads the VCO angle, is approximated by $V_+ \sin\phi$. In the present apparatus $V_+\cos\phi$ is also developed and an arctangent type function is used to determine ϕ from $V_+ \sin\phi$ and $V_+\cos\phi$. In the test apparatus the arctangent is evaluated

using look–up tables stored in memory. There are two exceptions for which the arctangent is not evaluated using the look–up tables. If Eqn. 42 is true then ϕ

$$\sqrt{V_\alpha^2 + V_\beta^2} \quad < \quad 0.1 \text{ p.u.} \qquad \text{Eqn. 42}$$

is set to zero and the arctangent is not evaluated. This eliminates the evaluation of the arctangent when both $V_+ \sin\phi$ and $V_+\cos\phi$ are small. In addition the magnitude of the error ϕ is set at $\pi/2$ in the test apparatus when Eqn. 43 is true. The

$$| V_+ \sin\phi | \; > \; 10 \times | V_+ \cos\phi | \qquad \text{Eqn. 43}$$

sign of ϕ is taken from the sign of $\sin\phi$ when Eqn. 43 is true. This second exception eliminates the evaluation of the arctangent when $V_+\cos\phi$ is zero which otherwise would result in division by zero. Figure 49 illustrates the output of the phase comparator in the test apparatus as a function of actual error assuming purely positive sequence voltages which are free of harmonics.

The second modification to the PLO consists of providing a low–pass single pole filter ahead of the PI controller so as to attenuate higher harmonics. Choosing T_w equal to 1.5 msec. in Figure 38 causes significant attenuation of noise introduced by the second and higher harmonics in the error signal.

The third modification is not shown in Figure 38 but was implemented to remove an error due to the discrete integration time–step ($\Delta T = 56$ μsec.) used in calculations for the low–pass filter, PI block, and VCO. The modification consists of phase advancing the angle θ out of the VCO from the last time–step by ΔT times the VCO frequency before providing the adjusted θ to the generator of $\sin\theta$ and $\cos\theta$ and hence to the input of phase comparator in Figure 38. When θ is adjusted in this way the error ϕ in a new time–step remains zero if the VCO

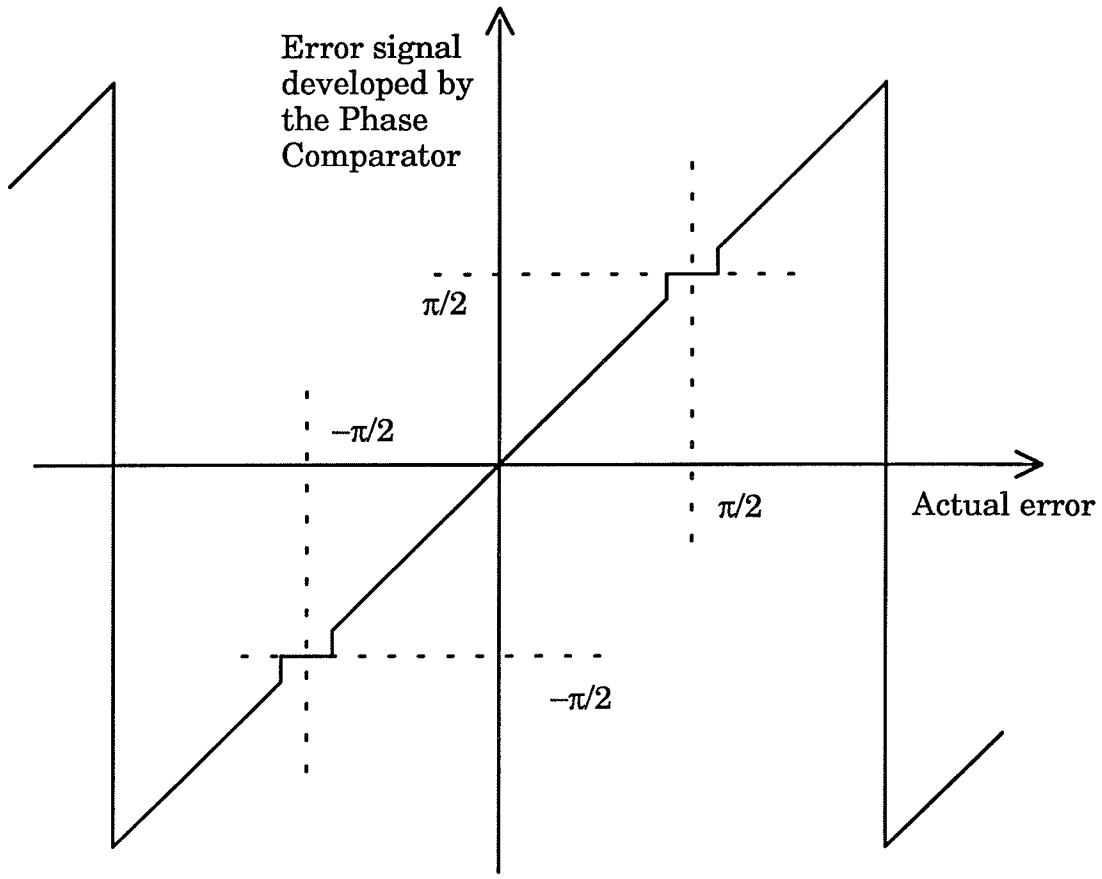
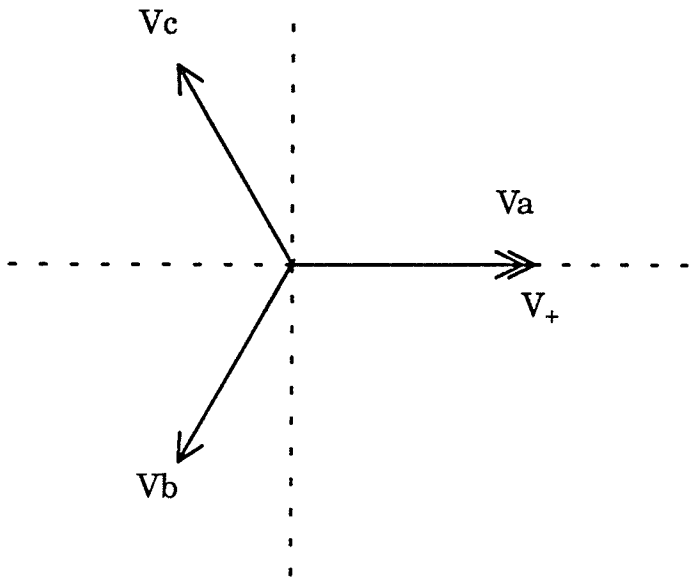


Figure 49. Phase Comparator Output versus Actual Phase Error

was perfectly locked in frequency and phase during the last time–step. This technique eliminates an error in θ which otherwise would be of the order of ΔT times the VCO frequency.

It was experimentally verified that the output θ of the PLO is the angle of the A–phase positive–sequence sine–wave voltage. Two sets of voltages were applied to the PLO. The first set of voltages is shown in Figure 50 as an approximately balanced set of three phase voltages. The saw–tooth wave shown in the photograph in Figure 50 represents θ and θ drops from 2π to 0 radians as expected at approximately the time that the A–phase sine wave of voltage goes positive. The second set of voltages is shown in Figure 51 as a very unbalanced set of voltages. In this laboratory test the C–phase voltage Vc was set to zero and



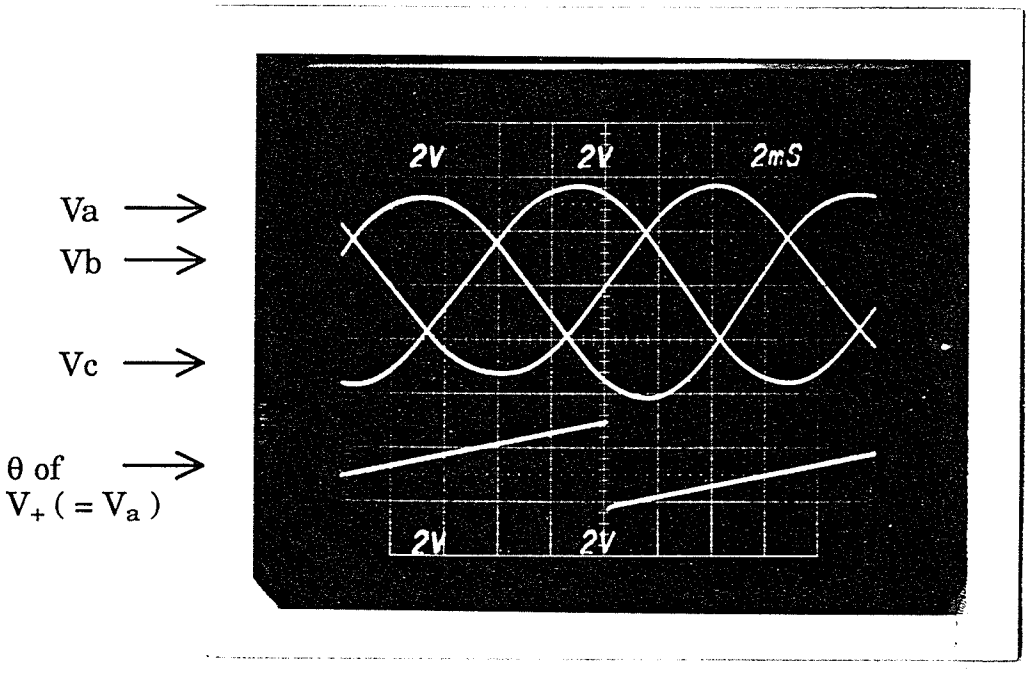
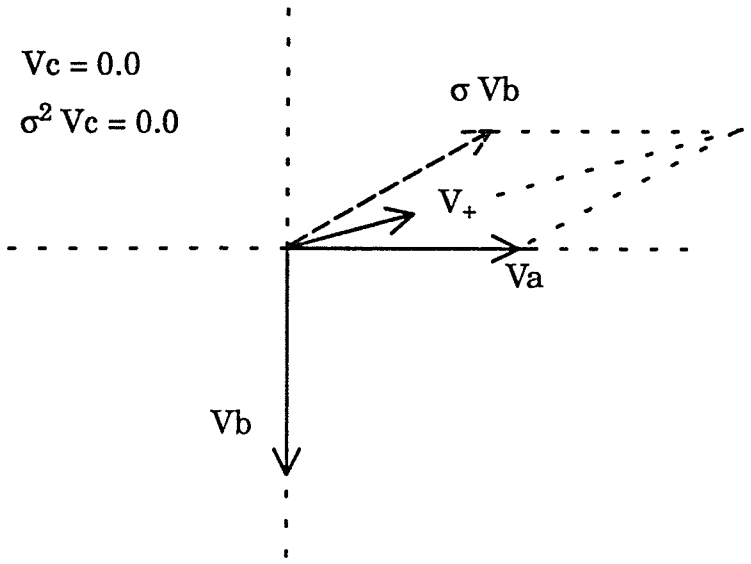
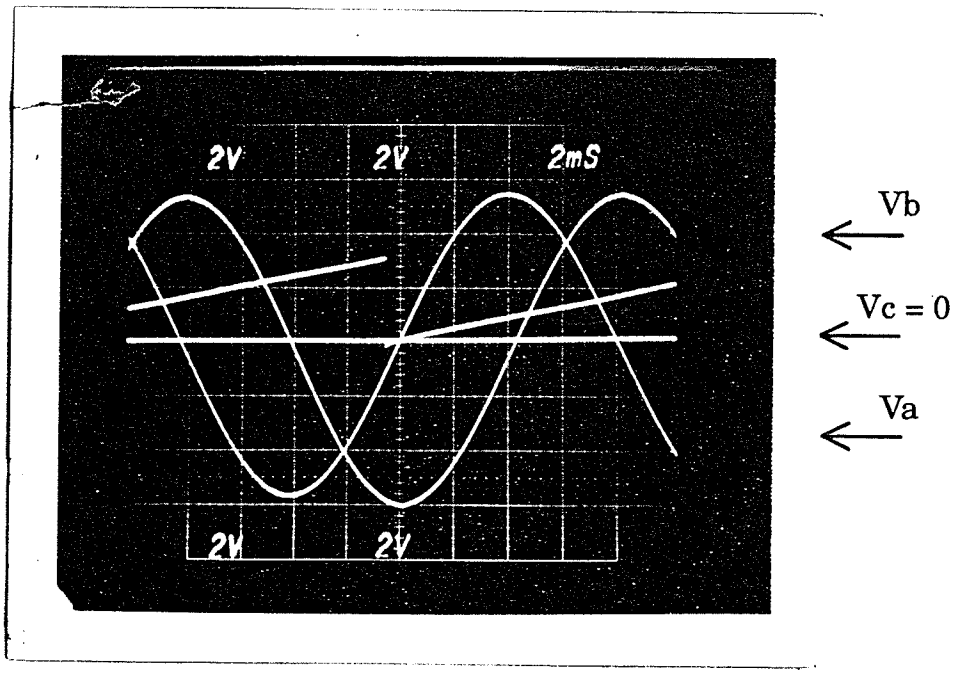


Figure 50. PLO Response to Approximately Balanced Three Phase Voltages.





The ramp shown in the photograph represents θ.

Figure 51. PLO Response to Very Unbalanced Three Phase Voltages.

Vb was made to lag Va by 90 degrees rather than by 120 degrees. For this set of voltages the positive–sequence A–phase voltage leads the A–phase voltage by approximately 15 degrees as shown by the phasor diagram in Figure 51. Reference to the photograph in Figure 51 shows that the θ saw–tooth wave dropped from 2π to zero as expected at approximately 15 degrees before the A–phase voltage went positive.

The gains of the PI block in the PLO are as illustrated in Figure 38. A ratio of integral to proportional gain equal to 8.0 performs satisfactorily. The proportional gain is as high as possible consistent with maintaining the roots of the characteristic equation purely real. Even with these relatively high gains the PLO works properly for very unbalanced sets of voltages such as illustrated in Figure 51.

The Texas Instruments TMS320C30 digital signal processor (DSP) used in the control hardware for the test apparatus required 13.5 μsec. of the 56 μsec. control calculation time–step in order to execute the PLO assembly code.

4.6 Summary for the Control System

The Power Order Control Block; Look–up Tables and Voltage–boost Converter Controller; and Rectifier Current Controller described in this chapter control machine voltage to 1.0 p.u. and control the inverter capacitor voltage V_I to the required level during steady running. The control system is primarily a feed–forward control which gives fast and reasonably accurate control during large load changes. Feed–back loops are provided in the control to correct the steady running errors.

The operation of the apparatus including controls is demonstrated by transients simulation results presented in Chapter 5. Laboratory verification of the apparatus with dc load substituted for the inverter is presented in Chapter 6.

Chapter Five

System Performance Demonstrated through Transients Simulation

5.1 Introduction

The prototype transients simulation program described in Chapter 3 was used to simulate the power apparatus illustrated in Figure 30 including controls as illustrated in Figures 31, 32, and 33. The simulated apparatus includes the test machine described in Appendix I; delta–connected 170 μF self–excitation capacitors; a controlled six–pulse Graetz bridge rectifier with 1 mH commutation inductors; a 1 kHz voltage–boost converter with 100 mH dc inductor and 7.2 mF electrolytic dc capacitor; and a twelve–pulse voltage–sourced inverter with shunt filtering as described in Appendix III.

The simulated apparatus was designed for operation over a speed range between 1.0 and 1.4 p.u. speed. Simulation results are presented from four cases. Case 1 results show performance during a sequence of events at 1.0 p.u. machine speed including a start–up with ac load disconnected; a subsequent application of 1.0 p.u. load; and a later load rejection. Case 2 is the same as Case 1 except that Case 2 is for operation at 1.4 p.u. machine speed. Cases 3 and 4 show performance at 1.0 and 1.4 p.u. speed during start–up with a pre–connected ac load impedance corresponding to 1.0 p.u. ac load. Load voltage waveshapes and associated harmonic contents are included with Case 3 results.

The four cases demonstrate the dynamic and steady running performance of the system for the full ranges of machine speed and loading. Laboratory test results are compared with simulation results in Chapter 6.

5.2 Case 1 – Simulated Performance at 1.0 p.u. Machine Speed with ac Load Applied after Start–up

The simulated result presented in this section shows performance of the apparatus at the lowest designed operating speed of 1.0 p.u. machine speed. The simulated result shows performance during a sequence of events including start–up with ac load disconnected; application of 1.0 p.u. ac load at t = 1.05 seconds; and load rejection at t = 1.35 seconds. Control signal plots are presented for:

i) the power order (Figure 57) from the Power Order Control Block (Figure 34);

ii) the basic dc current reference I_d*(ord) (Figure 52) from the Look–up Tables (Figure 35);

iii) the signal representative of the average voltage at the load end of the dc inductor V_{comp} (Figure 58) from the Voltage–boost Converter Controller (Figure 35);

iv) the rectifier delay angle order α (Figure 55) from the Rectifier Current Controller (Figure 36);

v) the voltage–boost converter Duty–Cycle Order β (Figure 56) from the Voltage–boost Converter Controller (Figure 35); and

vi) the inverter dc capacitor voltage reference V_{Iref} (Figure 54) from the ac Load Voltage PI Controller (Figure 33).

In addition to control signals, plots are presented for

i) dc current I_d (Figure 52);

ii) machine voltage magnitude V_m (Figure 53);

iii) inverter dc capacitor voltage V_I (Figure 54);

iv) ac load voltage magnitude V_{ac}(load) (Figures 59 and 60) and

v) waveshapes of the ac load voltage (Figure 60).

Case 1 is treated as the base case simulation in this chapter. Cases 2, 3, and 4 are briefly compared and contrasted to Case 1. The plots for Case 1 are provided in Figures 52 through 60. These plots are described below according to the time periods shown in Figure 52 as follows:

i) Prior to deblocking the rectifier at t = 0.23 seconds;

ii) Between deblocking the rectifier and subsequently connecting ac load at t = 1.05 seconds;

iii) Between connecting the ac load and subsequently causing ac load rejection by opening the ac load breaker at t = 1.35 seconds; and

iv) After the ac load rejection.

The explanation of Case 1 plots includes a detailed description of the interaction of the various parts of the control system.

5.2.1 Case 1 – Prior to Deblocking the Rectifier

There are a number of events which occur in the simulation prior to deblocking the rectifier at t = 0.23 seconds. The induction machine is driven at 1.0 p.u. speed from the beginning of the simulation with the self–excitation capacitors connected.

Residual magnetism in the induction machine causes the induction machine to act like a permanent magnet machine during the earliest stages of self–excitation [24]. The small voltages caused by the residual magnetism initiate the build–up of current in self–excitation. The growing machine currents subsequently overcome the original residual magnetism. The machine then operates as an induction machine with slip. The rectifier remains blocked until the ma-

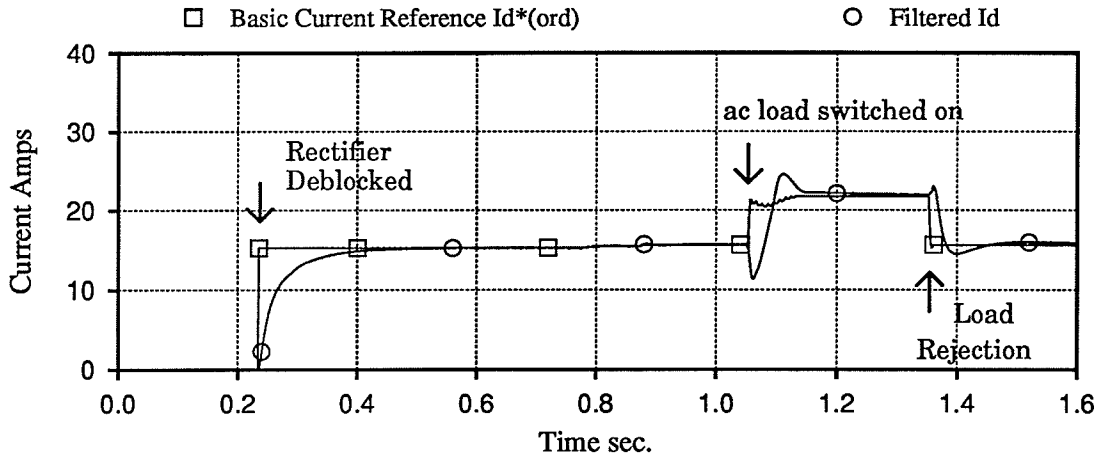


Figure 52. Case 1 – dc Currents I_d*(ord) and I_d

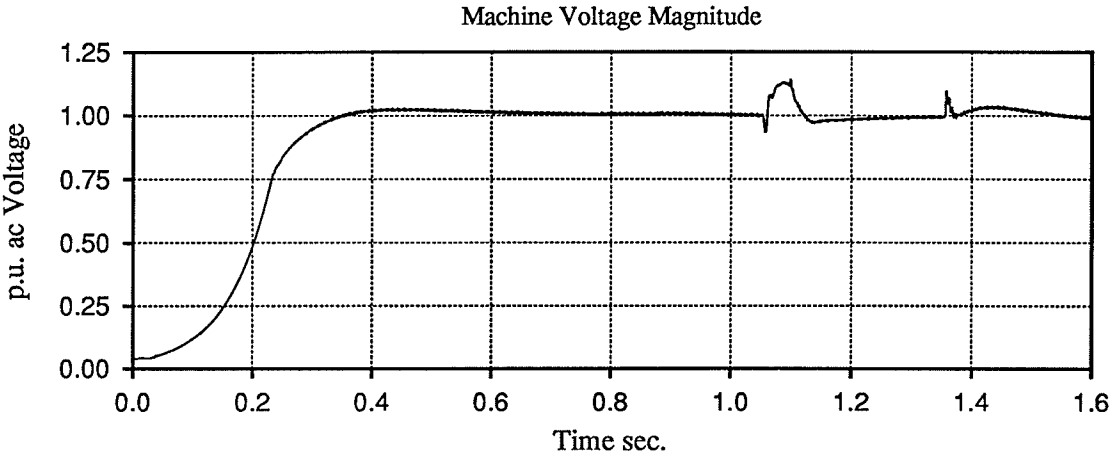


Figure 53. Case 1 – Machine Voltage V_m

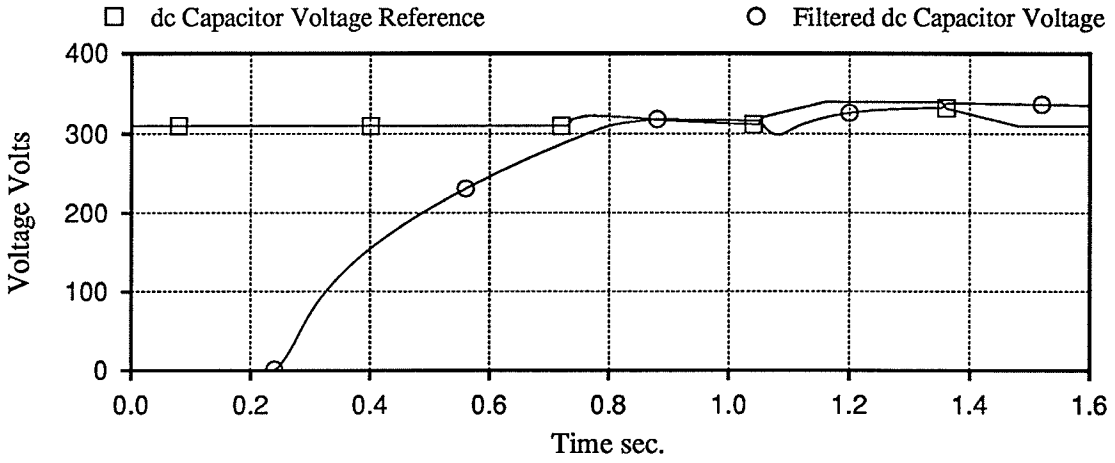


Figure 54. Case 1 – dc Capacitor Voltages V_{Iref} and V_I

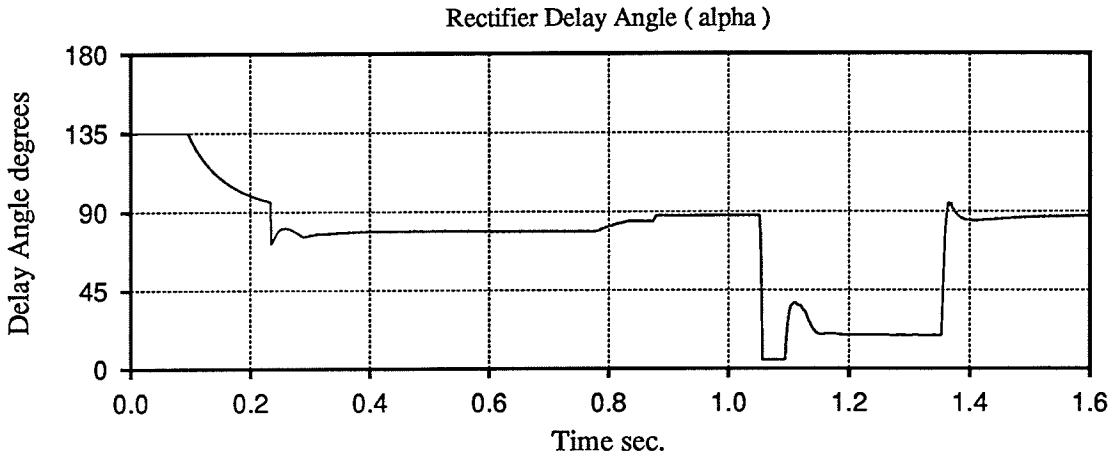


Figure 55. Case 1 – Rectifier Delay Angle α

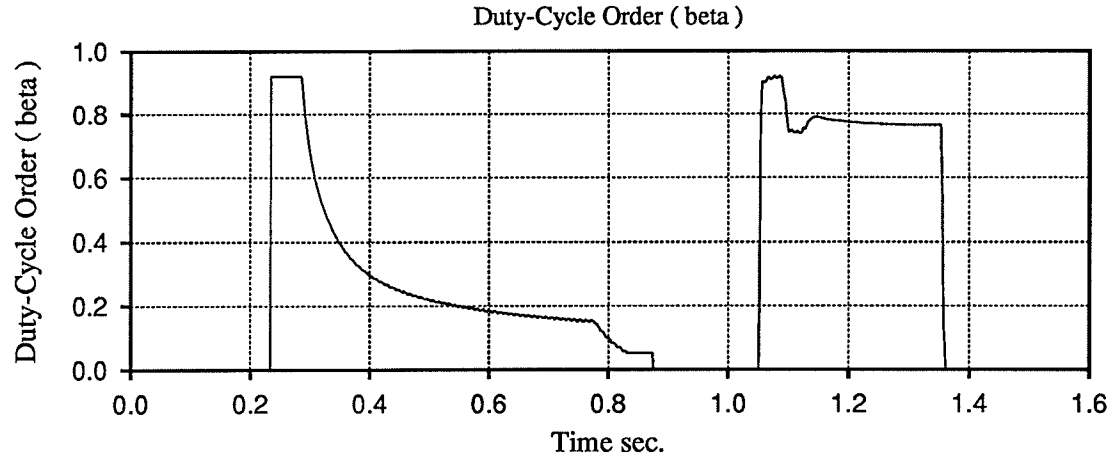


Figure 56. Case 1 – The Duty–Cycle Order β for the Boost Converter

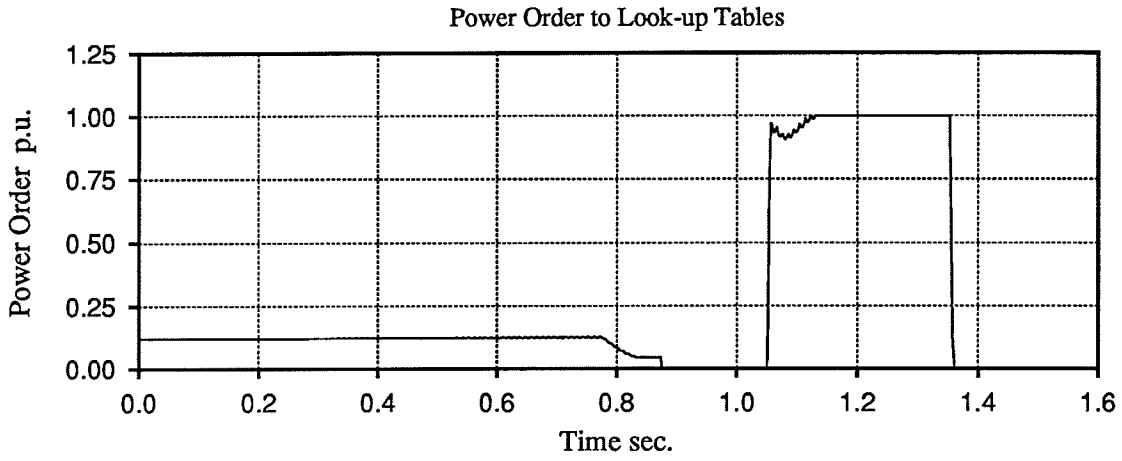


Figure 57. Case 1 – Power Order in Per Unit

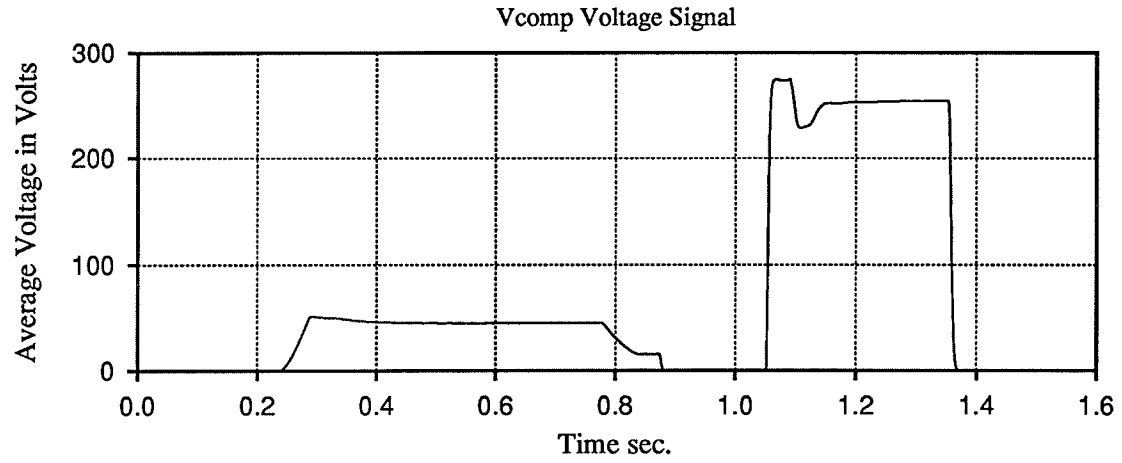


Figure 58. Case 1 – V_{comp} Voltage Signal from the Voltage–boost Converter Controller

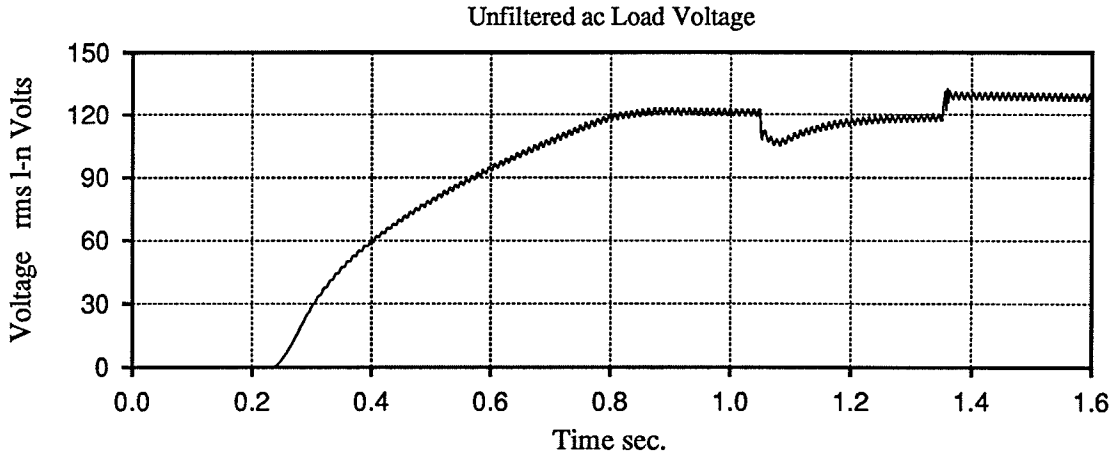


Figure 59. Case 1 – Measured ac Load Voltage

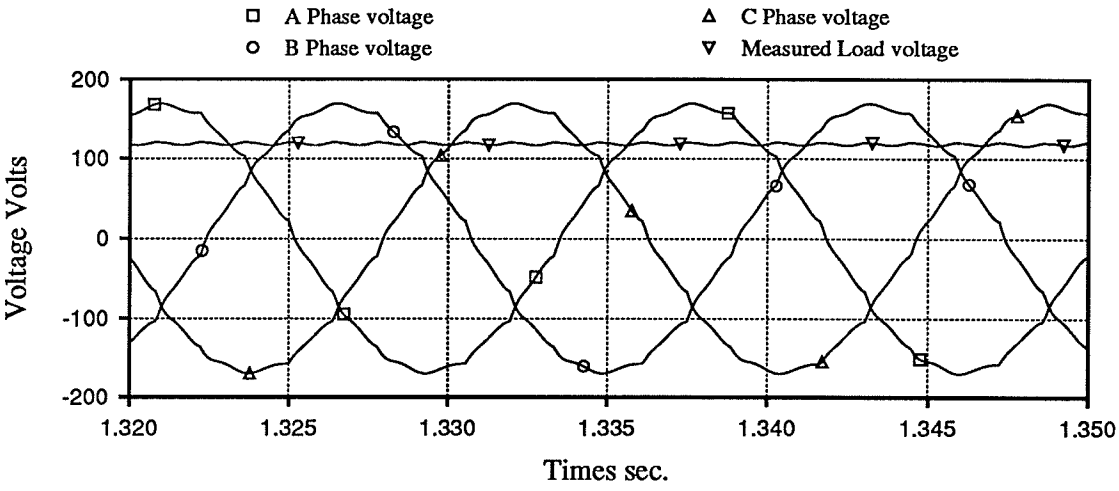


Figure 60. Case 1 – Load Voltage Waveshapes

chine ac voltage magnitude V_m rises to 0.75 p.u. voltage so that the load will not impede the build–up of voltage V_m.

Residual magnetism has not explicitly been represented in the model. However its effect is simulated by impressing small initial ac voltages on the machine during the first 30 milliseconds of the simulation.

Once the machine voltage V_m begins to rise it is necessary for the control to be initialized in anticipation of deblocking the rectifier. The first required action consists of initializing the frequency of the voltage–controlled–oscillator (VCO) in the phase–locked–oscillator (PLO) shown in Figure 38. It is important for the output angle θ of the PLO to track the positive–sequence voltage before the rectifier is deblocked because the rectifier firing delay angle α is applied with reference to the PLO output angle. Machine speed ν and voltage V_m are measured from the beginning of the simulation. The frequency of the VCO is initialized with the measured machine speed ν when unfiltered machine voltage V_m rises above 0.1 p.u. voltage. As a result of VCO frequency initialization, the VCO frequency needs to change only slightly before the rectifier is deblocked at approximately 0.23 seconds. The minor required change in VCO frequency permits the VCO output angle θ to track the positive –sequence voltage before the rectifier is deblocked. The effectiveness of this technique for initializing the VCO has also been verified during laboratory testing of the apparatus described in Chapter 6.

Although the VCO is initialized at an early stage the remainder of the controls remain inoperative until unfiltered machine voltage V_m rises above 0.75 p.u. voltage. At that time the remainder of the controls are activated and the voltage–boost converter and inverter shown in Figure 30 are deblocked. The rec-

tifier remains blocked for two more milliseconds to assure sufficient time for properly initializing the controls prior to deblocking the rectifier.

Preparing the remainder of the controls consists of initializing the outputs of all remaining integrators and low–pass single–pole filters. The balance of this paragraph lists the various initializations carried out. This information may be of interest to any persons wishing to build the control system. The filters for machine speed ν and machine voltage V_m (in Figure 32) are not initialized at this time because they are active from the beginning of the simulation. The filter outputs for I_d, V_I, and I_L in the Main Control (Figure 32) are initialized with present filter input values. The integrator in the Power Order Control Block (gain = K4 in Figure 32) is initially set to a neutral value of zero. The output of the integrator in the ac Load Voltage PI Controller (Figure 33) is initially set at the minimum V_I reference order of 310 volts and is held there until V_I rises to be close to the 310 volt order. Initializing the above noted filters and integrators in this sequence assures that the Boost Converter Firing Logic (Figure 32) immediately receives a valid Duty–Cycle Order β (Figure 56) having regard to the present machine speed ν, dc current I_d, dc capacitor voltage reference V_{Iref}, dc capacitor voltage V_I, and dc load current I_L. The output of the low–pass filter for actual duty–cycle β^* in Figure 32 is also initialized to its present input value. Finally the integrator in the Machine Voltage PI Control Loop (Figure 37) is initialized to a neutral value of zero. The same initialization sequence is carried out in the actual controls that were tested in the laboratory as described in the next chapter.

The rectifier can be deblocked at about t = 0.23 seconds once the control integrators and low–pass filters are initialized as described above. The basic current reference I_d^*(ord) as illustrated in Figure 52 begins to be passed to the Rectifier

Current Controller at that time. A valid rectifier delay angle order α exists prior to deblocking the rectifier as illustrated in Figure 55. The duty–cycle order β for the voltage–boost converter which is illustrated in Figure 56 is also valid. The Duty–Cycle Order β represents the fraction of each period of the boost converter during which the GTO device is blocked. The GTO device in the voltage–boost converter is blocked to cause the dc current I_d to flow through the diode to the dc capacitor (Figure 31).

5.2.2 Case 1 – Between Deblocking the Rectifier and Application of ac Load

This section explains the plots for Case 1 (Figures 52 through 60) in the period between deblocking the rectifier at approximately t = 0.23 seconds and connection of the ac load at t = 1.05 seconds.

In Case 1 the rectifier deblocks at t = 0.23 seconds as indicated in Figure 52 by the presence of dc current I_d beginning at that time. The control system deblocks the rectifier 2 msec. after sensing machine voltage larger than 0.75 p.u. voltage (see Figure 53). The 2 msec. delay provides sufficient time for completing the control initialization described above before deblocking the rectifier. The presence of the dc current I_d immediately begins to decrease the growth rate of machine voltage V_m as illustrated in Figure 53. The control of V_m provided by the rectifier causes V_m to arrive at the desired 1.0 p.u. operating voltage without significant overshoot. The dc capacitor voltage V_I is zero when the rectifier deblocks as illustrated in Figure 54.

Figure 57 illustrates the power order which is supplied to the Look–up Tables in Case 1. The power order is limited to 1.0 p.u. power which is the maximum value which will be accepted by the tables. Changes in the power order are discussed as a basis for explaining changes in the rectifier order α and the voltage–boost converter order β as illustrated in Figures 55 and 56.

The Power Order Control Block (Figure 34) develops the power order based on four factors as explained in section 4.3. The measured load power is zero when the rectifier deblocks because V_I is zero. Measured load power also remains essentially zero for Cases 1 and 2 until the ac load is connected at t = 1.05 seconds. Therefore measured load power does not contribute to the power order when the rectifier deblocks. The integrator (gain = K4) in the Power Order Control Block (Figure 34) only provides a power order reduction signal when there is an overvoltage in V_I. However, there is no overvoltage in V_I when the rectifier deblocks. Therefore, the integrator does not contribute to the power order when the rectifier deblocks. The proportional branch (gain = $2 / V_{Iref}$ (nominal)) in the Power Order Control Block (Figure 34) provides a contribution to the power order due to undervoltage in V_I. The undervoltage in V_I is 1.0 p.u. when the rectifier deblocks. However, the limit on the proportional branch contribution is 0.12 p.u. power as illustrated in Figure 34. In summary, the power order consists entirely of the limited output of the proportional branch when the rectifier deblocks. Therefore the power order remains constant on the 0.12 p.u. power limit until t = 0.77 seconds as shown in Figure 57 until the magnitude of the undervoltage in V_I drops below the threshold level of 0.06 p.u. voltage.

The Look–up Tables (Figure 35) receive machine speed v and power order and provide I_d*(ord) and V_d*(ord) as basic references for current I_d and voltage V_d. It is noted above that the power order is constant at 0.12 p.u. power until t = 0.77 seconds. A power order of 0.12 p.u. power at 1.0 p.u. machine speed causes the Look–up Tables to provide output for V_d*(ord) of about 40 Volts and output for I_d*(ord) of about 15 Amps as indicated in Figures 7 and 8. The signal for I_d*(ord) is illustrated in Figure 52. Normally the Voltage–boost Converter Controller tries to cause a voltage at the load end of the dc inductor (hereinafter referred to as the Target Voltage) which is equal to the reference V_d*(ord) from

the tables. However, if I_d differs from I_d*(ord) the Voltage–boost Converter Controller (Figure35) changes the Target Voltage at the load end of the dc inductor by a limited factor I_d*(ord) / I_d in an effort to obtain the ordered power. Further explanation of this measure is given in section 4.4 which describes the Voltage–boost Converter Controller. In steady running the average rectifier output voltage V_d is essentially the average voltage at the load end of the dc inductor caused by the voltage–boost converter.

When the rectifier deblocks at t = 0.23 seconds the Voltage–boost Converter Controller produces a Duty–Cycle Order β equal to 0.92 (Figure 56). The order β is calculated in the Voltage–boost Converter Controller (Figure 35) as described in section 4.4 by first dividing the Target Voltage (i.e. approximately V_d*(ord) = 40 Volts) by the maximum of V_I and 15 Volts (i.e. 15 Volts) and then limiting the quotient (i.e. 2.66) to between 0.92 and 0.05. In this way the Voltage–boost Converter Controller tries to cause the voltage at the load end of the dc inductor to be equal to the Target Voltage to the extent that V_I is adequate for this purpose. The Duty–Cycle Order β remains fixed at the 0.92 limit in the period between 0.23 and 0.28 seconds as shown in Figure 56 because the voltage V_I is small until about t = 0.28 seconds as illustrated in Figure 54. The Duty–Cycle Order β of 0.92 causes the maximum permitted fraction of I_d to be passed to the dc capacitor to raise the capacitor voltage V_I.

Figure 56 shows that β remains on the 0.92 limit in the period between 0.23 and 0.28 seconds. The order β drops from the 0.92 limit only when the quotient of the Target Voltage divided by V_I drops below 0.92 due to increasing dc capacitor voltage V_I. The timing of this event is indicated in Figure 56 by the decrease in β at t = 0.28 seconds. The Target Voltage for the voltage at the load end of the dc inductor remains at approximately V_d*(ord) (≈ 40 Volts) until 0.77 sec-

onds. The movement of order β from the 0.92 limit at t = 0.28 seconds signifies that the voltage V_I is sufficient to enable the voltage–boost converter to provide the requested average Target Voltage at the load end of the dc inductor. The requested Target Voltage results in a V_{comp} signal for the Rectifier Current Controller commencing at t = 0.28 seconds as illustrated in Figure 58. The relatively constant V_{comp} signal lasts until the power order begins to decrease at t = 0.77 seconds.

The Rectifier Current Controller (Figure 34) develops a delay angle order α after the rectifier deblocks at t = 0.23 seconds. The rectifier order α which is plotted in Figure 55 varies until t = 0.4 seconds because it depends (see Figure 36) on machine voltage V_m, dc current I_d, and V_{comp} all of which change until t = 0.4 seconds. However in the period between 0.4 and 0.77 seconds α remains essentially constant as illustrated in Figure 55. The order α remains constant because the quantities which determine α namely I_d, V_m, I_d*(ord), and V_{comp} all remain essentially unchanged during the period as shown in Figures 52, 53, and 58.

The increasing dc capacitor voltage V_I illustrated in Figure 54 causes the magnitude of the undervoltage in V_I to decrease below the threshold level of 0.06 p.u. voltage after t = 0.77 seconds. The decrease in V_I undervoltage after t = 0.77 seconds causes the Power Order Control Block (Figure 34) to decrease the power order below the 0.12 p.u. power limit as shown in Figure 57. This decreasing of the final power order continues until approximately t = 0.83 seconds. At that time the power order reachs the speed–dependant lower limit on power order located as shown in the Power Order Control Block (Figure 34).

The decreasing power order after t = 0.77 seconds causes the output V_d*(ord) from the tables to undergo a corresponding decrease according to Figure 8. The

decreasing V_d*(ord) decreases the Target Voltage (Figure 35) in the period between 0.77 and 0.83 seconds. The decreasing Target Voltage in turn causes the Duty–Cycle Order β produced by the Voltage–boost Converter Controller to decrease as illustrated in Figure 56 in the period between 0.77 and 0.83 seconds. In response to the decreasing β order the average voltage at the load end of the dc inductor represented by V_{comp} decreases as shown in Figure 58. The decreasing V_{comp} signal in turn causes the Rectifier Current Controller (Figure 36) to decrease the final dc voltage order V_d(ord) in the period between 0.77 and 0.83 seconds. The decreasing V_d(ord) signal causes a corresponding increase in α between 0.77 and 0.83 seconds as illustrated in Figure 55.

At t = 0.83 seconds the decreasing power order (Figure 57) reaches the speed–dependant lower limit located as shown in the Power Order Control Block (Figure 34). After the power order arrives against the limit the Look–up Tables (Figure 35) again provide a constant value for V_d*(ord). In response to constant V_d*(ord) the Voltage–boost Converter Controller produces a Duty–Cycle Order β which remains essentially fixed at 0.05 as illustrated in Figure 56. The constant β order causes a constant V_{comp} signal after t = 0.83 seconds as illustrated in Figure 58. The constant V_{comp} signal in turn causes the order α to remain essentially constant beginning at t = 0.83 seconds as illustrated in Figure 55.

The undervoltage in V_I is replaced by a slight overvoltage at about t = 0.87 seconds as illustrated in Figure 54. The integrator (gain K4) in the Power Order Control Block (Figure 34) responds to the overvoltage in V_I by producing a power order reduction signal. The reduction signal causes the power order ahead of the speed–dependant lower limit to go quickly negative at t = 0.87 seconds. The Power Order Control Block (Figure 34) responds to the negative value by providing a zero power order as illustrated in Figure 57 and by signalling for con-

tinuous conduction of the GTO device. Figure 56 indicates that continuous conduction of the GTO device begins at t = 0.87 seconds. The zero power order lasts until the ac load is connected at t = 1.05 seconds.

Continuous conduction of the GTO device is indicated commencing at t = 0.87 seconds by the Duty–Cycle Order β of 0.0 which begins at that time as illustrated in Figure 56. Continuous conduction of the GTO device avoids further charging of the dc capacitor. The voltage at the load end of the dc inductor represented by V_{comp} drops to zero when the GTO device begins to conduct continuously at t = 0.87 seconds as illustrated in Figure 58. The rectifier delay angle order α approaches 90 degrees as shown in Figure 55 in response to the drop in V_{comp}. The rectifier and voltage–boost converter orders remain unchanged after t = 0.87 seconds until the ac load breaker is closed at t = 1.05 seconds.

The ac load voltage magnitude approaches the ordered value of 120 Volts (rms line–to–neutral) as illustrated in Figure 59 prior to the application of ac load at t = 1.05 seconds. The sampled signal for the magnitude of the ac load voltage is provided using the following simple equation. The result produced by

$$\text{Vac(load) (rms)} = \sqrt{\frac{V_a(\text{load})^2 + V_b(\text{load})^2 + V_c(\text{load})^2}{3}}$$

this equation is correct and smooth for balanced ac voltages which are also free of harmonics. However, the ac load voltage waves shown in Figure 60 are not free of harmonic voltages. The harmonic voltages cause a 720 Hz ripple on the Measured Load voltage signal plotted in Figure 60. The frequency of the ripple on the ac load voltage magnitude shown in Figure 59 is deceptive because it is caused by aliasing due to under–sampling. The ripple on the measured ac load voltage is shown correctly in Figure 60 because the blown–up plot is based on 20 samples per millisecond. The voltage plotted in Figure 59 is referred to as

"measured" ac load voltage because within the simulation it is determined by monitoring the ac voltage wave and applying the simple equation given above.

5.2.3 Case 1 – Between Application of Load and Load Rejection

At t = 1.05 seconds the ac load breaker is closed to connect the ac load. The ac load impedance is selected to draw 1.0 p.u. power (5.6 kW) at 0.8 power factor lagging when the ac load voltage reaches 1.0 p.u. voltage (120 Volts rms line–to–neutral).

When the ac load is connected at t = 1.05 seconds the dc capacitor voltage V_I dips approximately 7 percent as illustrated in Figure 54. On the other hand, the ac load voltage Vac(load) dips by approximately 12 percent as illustrated in Figure 59. The difference in the voltage drops is caused by a drop in the voltage across the inverter transformer leakage inductance due to flow of current to the inductive load. Before ac load is connected there is an ac voltage rise from source to load terminals in the inverter transformer. The voltage rise is due to the capacitance of shunt–connected ac filters on the load bus. The filters are described in Appendix III. On the other hand when the ac load is connected onto the load bus the overall nature of the load plus filters turns inductive thereby causing an ac voltage drop. The ac Load Voltage PI Controller (Figure 33) responds to the low ac voltage by increasing V_{Iref} as illustrated in Figure 54. The Main Control (Figure 32) adjusts V_I according to the increased V_{Iref} to restore the ac load voltage to 1.0 p.u. by about t = 1.35 seconds as illustrated in Figure 59.

The power order in the period between 1.05 and 1.35 seconds is the sum of the measured load power plus a limited proportional component of power order introduced by the undervoltage in V_I. The power order increases abruptly when the ac load is connected at t = 1.05 seconds as illustrated in Figure 57. The small dip in the power order immediately after t = 1.05 seconds shown in Figure 57 is

caused by the short term drop in ac load voltage shown in Figure 59 occurring after connection of the ac load.

The approximate step increase in the power order at t = 1.05 seconds which is illustrated in Figure 57 causes a similar step increase in the basic dc current reference I_d*(ord) at t = 1.05 seconds as illustrated in Figure 52. Conversely, the actual dc current I_d momentarily dips when the ac load is connected as also shown in Figure 52. The dip in I_d is due to an increase in the Duty–Cycle Order β which causes the average voltage at the load end of the dc inductor to increase before the Rectifier Current Controller can respond by increasing the voltage at the rectifier end of the dc inductor. The rectifier responds more slowly in part because the V_{comp} signal illustrated in Figure 58 rises slightly more slowly at t = 1.05 seconds than the boost converter Duty–Cycle Order β illustrated in Figure 56. The discrete firing times of the rectifier also cause possible delay in the response of the rectifier.

Normally the Voltage–boost Converter Controller (Figure 35) tries to control the voltage at the load end of the dc inductor to the Target Voltage. As mentioned above the Target Voltage is V_d*(ord) from the tables multiplied by the limited quotient of I_d*(ord) / I_d. The limits for the quotient are 0.9 and 1.1. At t = 1.05 seconds I_d is significantly less than I_d*(ord) as illustrated in Figure 52. Therefore the Voltage–boost Converter Controller creates a Target Voltage of 1.1 times V_d*(ord) for the voltage at the load end of the dc inductor. The resultant increased voltage at the load end of the dc inductor is represented by V_{comp} after t = 1.05 seconds as illustrated in Figure 58. The corresponding order β is illustrated in Figure 56. The increased V_{comp} signal when added to the voltage component V_d(adj) developed in the Rectifier Current Controller (Figure 36) results

in a rectifier delay angle α as illustrated in Figure 56 which is pinned against the 5 degree lower limit until approximately t = 1.09 seconds.

The machine voltage magnitude V_m shown in Figure 53 abruptly increases immediately after the application of the ac load for two reasons. On the one hand, the dc current I_d decreases when load is applied and therefore the ac current magnitude into the rectifier also decreases. In addition the abrupt change in α from approximately 88 degrees down to 5 degrees as illustrated in Figure 55 causes the power factor of the current into the rectifier to approach unity. Consequently, the rectifier absorbs very little reactive power until after the difference between I_d and I_d*(ord) is eliminated at t = 1.09 seconds as illustrated in Figure 52. The machine voltage therefore climbs until that time.

At t = 1.09 seconds the dc current I_d has risen to match the basic dc current reference I_d*(ord) as shown in Figure 52. The increase in V_{comp} due to the factor I_d*(ord) / I_d is therefore eliminated at t = 1.09 seconds as illustrated in Figure 58. After t = 1.09 seconds I_d grows larger than I_d*(ord) as illustrated in Figure 52. This causes some undershoot in V_{comp} as also illustrated in Figure 58. The corresponding change to order β is illustrated in Figure 56. It is necessary that I_d must overshoot I_d*(ord) after t = 1.09 seconds in order to control the machine voltage V_m which has risen to about 1.1 p.u. by t = 1.09 seconds. The multiplication of the basic dc current reference I_d*(ord) by machine voltage V_m in p.u. in the Rectifier Current Controller (Figure 36) facilitates the appropriate final dc current order I_d(ord) for causing machine voltage V_m to recover from an overvoltage condition (section 4.5.1).

After t = 1.13 seconds the fast transient due to the application of 1.0 p.u. ac load is essentially complete. The slow transient associated with the change in

V_{Iref} continues until the ac load voltage is brought to approximately 1.0 p.u. voltage at t = 1.35 seconds as illustrated in Figure 59.

5.2.4 Case 1 – After Load Rejection

At t = 1.35 seconds the ac load breaker opens to cause ac load rejection.

When full load rejection occurs the voltage drop on the inverter transformer reverts to being a voltage rise, as discussed above, due to a second reversal in the direction of reactive power flow through the inverter transformer. The return of the voltage rise causes an immediate overvoltage in ac load voltage V_{ac}(load) of approximately 10 percent as illustrated in Figure 59. This overvoltage occurs even though the immediate change in the dc capacitor voltage V_I is very small as illustrated in Figure 54.

After full load rejection it is important that the GTO device should quickly commence continuous conduction to prevent an increase in V_I which would add to the overvoltage in V_{ac}(load). Continuous conduction is accomplished by dropping the power order to zero at t = 1.35 seconds as illustrated in Figure 57. The power order drops to zero for two reasons. On the one hand the measured load power component of the power order drops to approximately zero. In addition the integrator in the Power Order Control Block (Figure 34) integrates to provide a power order reduction signal because V_I is larger than V_{Iref}. V_I is certain to be larger than V_{Iref} very shortly after rejection of a normal inductive load. Capacitor voltage V_I can only rise because current cannot flow backward through the diode in the voltage–boost converter. Also the proportional part of the ac Load Voltage PI Controller (Figure 33) causes an immediate drop in V_{Iref} due to the overvoltage in V_{ac}(load). The maximum limit of 0.18 p.u. power on the power order reduction signal (Figure 34) allows a sufficiently large reduction in the power order to positively assure that the final power order will drop to zero

upon load rejection. When the power order drops to zero the Power Order Control Block (Figure 34) also signals the voltage–boost converter to go to continuous conduction. The result is that β and V_{comp} both drop to zero at t = 1.35 seconds as illustrated in Figures 56 and 58. The Rectifier Current Controller (Figure 36) then acts alone to adjust I_d and thereby bring machine voltage V_m to 1.0 p.u. voltage as illustrated in Figures 52 and 53. The overvoltage in load voltage V_{ac}(load) illustrated in Figure 59 is reduced within a few seconds by losses in the inverter and ac load voltage filters.

To summarize Case 1, the above described performance demonstrates that a control system can be provided to effectively control both machine voltage and ac load voltage during both steady running and during the largest load changes at 1.0 p.u. speed. Figures 53 and 59 show that the machine voltage and ac load voltage are both controlled to essentially 1.0 p.u. voltage during steady running. These figures also show that the machine voltage and ac load voltage are both controlled to between plus and minus 12 percent of 1.0 p.u. voltage during both instantaneous connection of full load and instantaneous rejection of full load. Case 2, briefly described in the next section, shows that the control system also provides acceptable performance at the maximum designed operating speed of 1.4 p.u. speed.

5.3 Case 2 – Simulated Performance at 1.4 p.u. Machine Speed with ac Load Applied after Start–up

Case 2 is similar to Case 1 except that the machine is driven at the maximum designed operating speed of 1.4 p.u. speed in Case 2 rather than at 1.0 p.u. speed. Case 2 is similar to Case 1 in that full load is instantaneously applied at 1.05 seconds followed by a full load rejection at 1.35 seconds. The faster speed of operation in Case 2 causes some noticeable differences between the plots for Case

2 (shown in Figures 61 through 66) and the plots for Case 1 (shown in Figures 52 through 60).

In Case 2 the basic dc current reference I_d*(ord) which is shown in Figure 61 changes only slightly when the ac load is connected at t = 1.05 seconds. This reflects that I_d*(ord) is essentially independent of power order at 1.4 p.u. speed and thus essentially constant as shown in Figure 7.

An additional difference between Case 1 and Case 2 is the more rapid build up of machine voltage V_m in Case 2 at the beginning of self–excitation. In that regard compare plots of V_m in Figures 62 and 53. The plot of V_m in Case 2 (Figure 62) also shows a machine overvoltage of about 18 percent that results from full load rejection at 1.4 p.u. speed at t = 1.35 seconds. This compares to an overvoltage of about 12 percent after a similar load rejection at 1.0 p.u. speed as shown in Figure 53. In general V_m is subject to more rapid and larger changes at 1.4 p.u. speed as compared to changes at 1.0 p.u. speed.

The rectifier delay angle α generally increases as speed increases at a given load. The increase in α at higher machine speeds allows the rectifier to absorb the increase in the surplus VARS which are supplied by the self–excitation capacitors but which are not required by the machine. Comparison of α in Case 2 (Figure 65) with α in Case 1 (Figure 55) at 1.0 p.u. ac load confirms the increase in α at higher speeds for a given load. In both cases 1.0 p.u. load exists immediately prior to t = 1.35 seconds. Figure 65 shows an α of about 50 degrees at 1.4 p.u. speed prior to t = 1.35 seconds. In comparison Figure 55 shows an α of about 20 degrees at 1.0 p.u. speed. The generally higher α for higher speeds reflects the lower dc voltages shown in Figure 8 for operation at higher speeds.

Conversely, the boost converter Duty–Cycle Order β generally decreases as speed increases at a given load. The order β for Case 2 is about 0.5 prior to t =

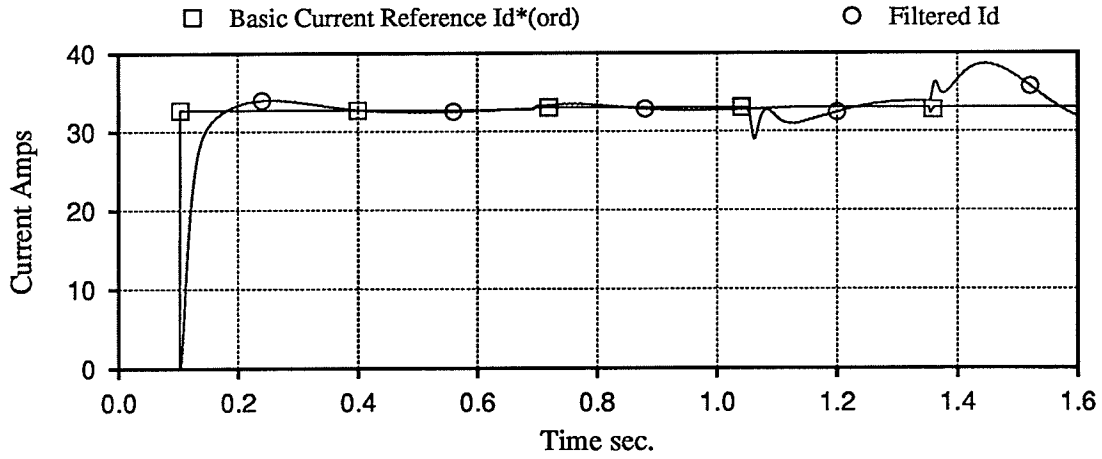


Figure 61. Case 2 – dc Currents I_d*(ord) and I_d

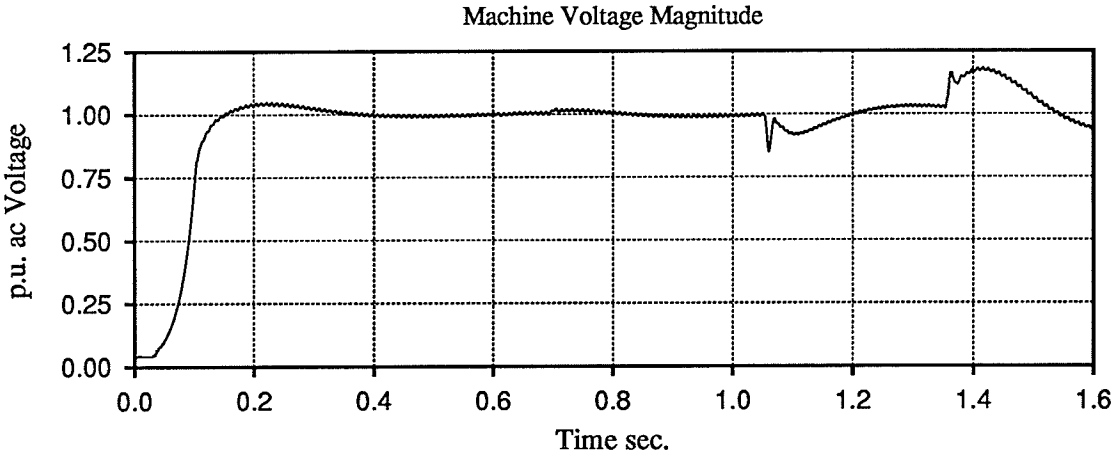


Figure 62. Case 2 – Machine Voltage V_m

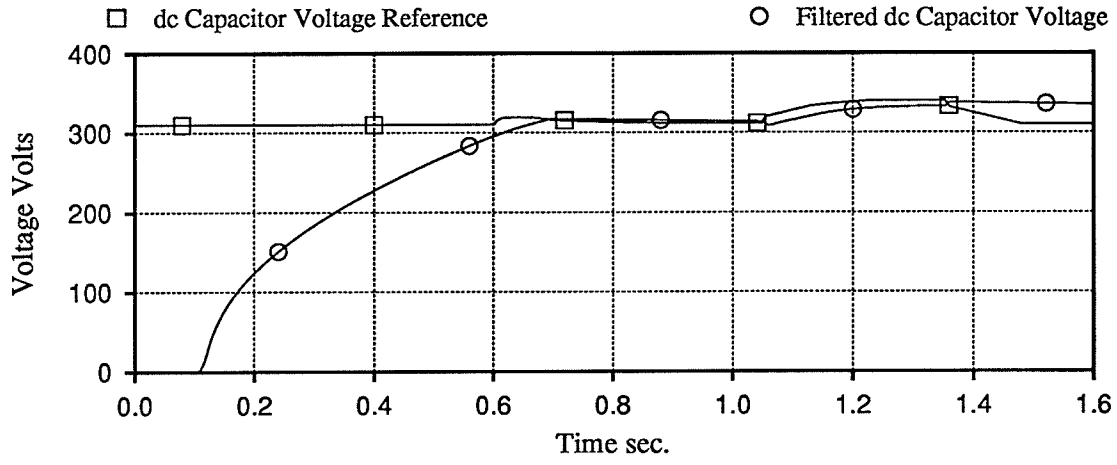


Figure 63. Case 2 – dc Capacitor Voltages V_{Iref} and V_I

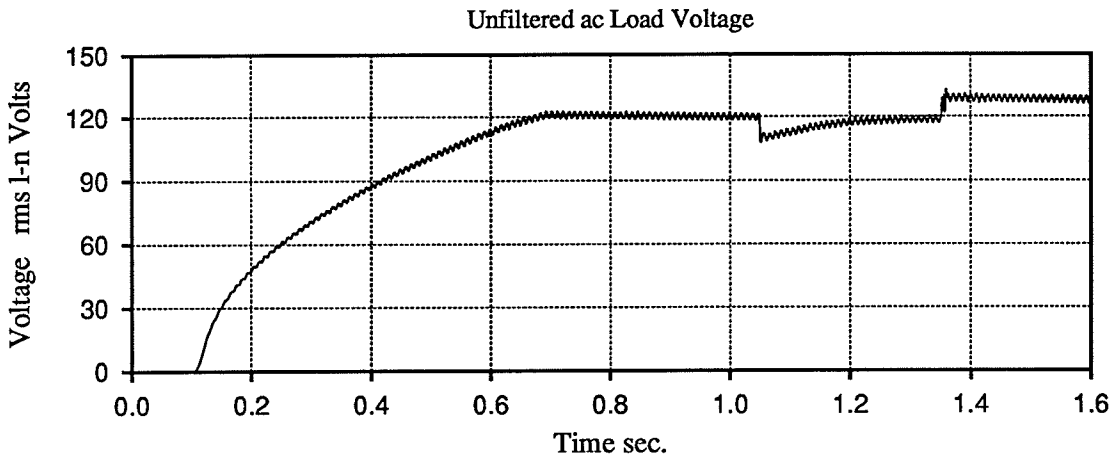


Figure 64. Case 2 – Measured ac Load Voltage

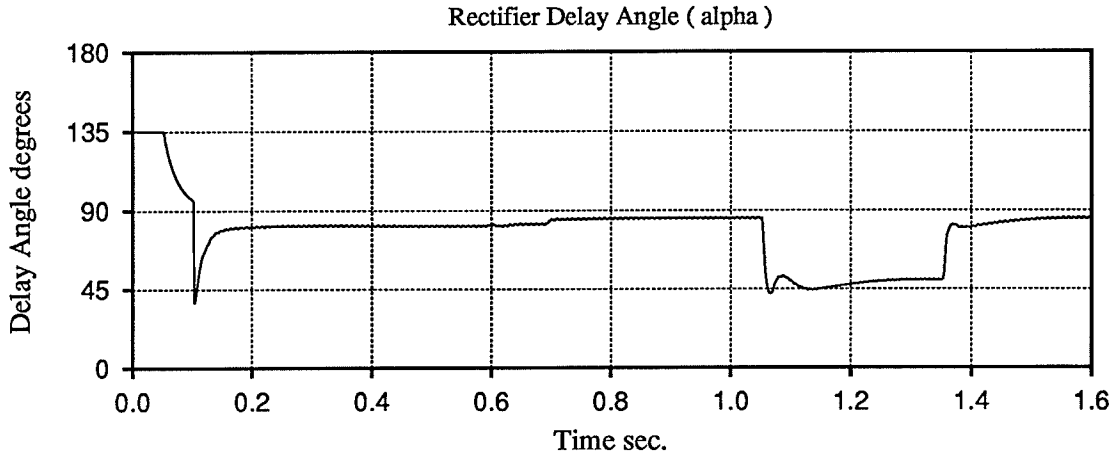


Figure 65. Case 2 – Rectifier Delay Angle α

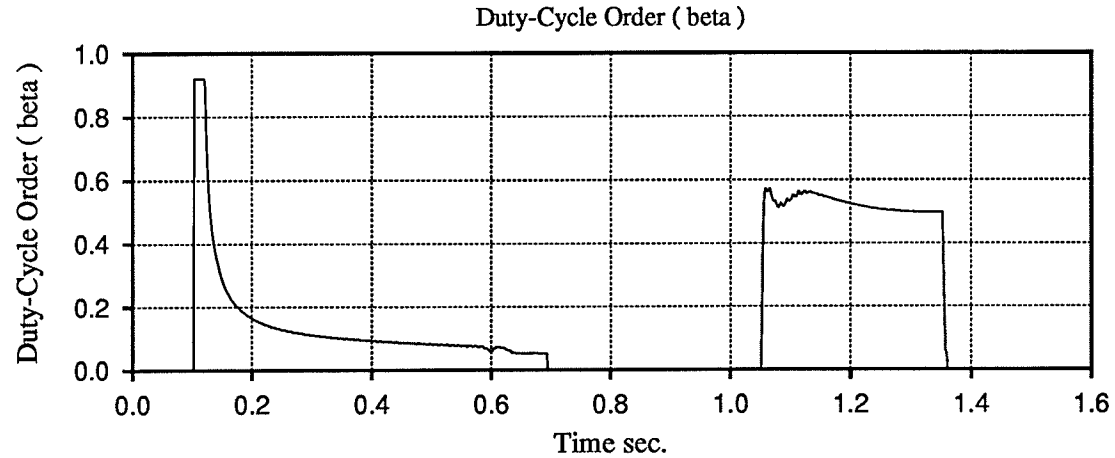


Figure 66. Case 2 – The Duty–Cycle Order β for the Boost Converter

1.35 seconds as shown in Figure 66. For similar load the order β for Case 1 is about 0.75 prior to t = 1.35 seconds as shown in Figure 56. The lower β order occurs at the higher speed because dc current I_d increases with speed as shown in Figure 7. The higher dc current I_d at higher speeds means that the order β need not be as large in order to supply the necessary average current I_L to the inverter.

A comparison of the plots of V_{ac}(load) in Figure 64 and Figure 59 shows that an increase in the machine speed from 1.0 p.u. to 1.4 p.u. speed does not degrade the ability of the control system to control the ac load voltage during large changes in load.

The plots for Case 2 are presented above to demonstrate that the control system also performs satisfactorily at 1.4 p.u. speed which represents the high end of the range of permitted machine speeds.

5.4 Case 3 – Simulated Performance at 1.0 p.u. Machine Speed during Start–up with Pre–connected ac Load

In Cases 1 and 2 the machine voltage V_m and ac load voltage V_{ac}(load) are allowed to stabilize at essentially 1.0 p.u. voltage before connection of the ac load at t = 1.05 seconds. Conversely, in Cases 3 and 4 described here, the ac load is switched in prior to the start of self–excitation. In all four cases the ac load impedance is selected to draw 1.0 p.u. power with 0.8 power factor lagging at 1.0 p.u. ac load voltage. The results from Cases 3 and 4 all demonstrate that the control system is quite capable of starting the apparatus under load and stabilizing V_m and V_{ac}(load) at essentially 1.0 p.u. voltage.

Plots for Case 3, which are illustrated in Figures 67 to 72, show the control system performance at 1.0 p.u. machine speed during start–up under load. Additional plots for Case 3, which are illustrated in Figures 73 to 76, show the per-

formance of the shunt filtering connected on the ac load bus. The shunt filtering is described in Appendix III as part of the description of the twelve–pulse voltage–sourced inverter. Further Case 3 plots which are illustrated in Figures 77 and 78 show simulated voltages at inductive nodes. A node is referred to as an inductive node when only inductive branches are incident on the node. Finally the plots in Figure 79 show the simulated currents in a capacitive loop formed by the delta–connected self–excitation capacitors.

As mentioned above, Case 3 demonstrates that the control system can start the apparatus at 1.0 p.u. speed with full load connected to the inverter and then regulate both V_m and V_{ac}(load) to essentially 1.0 p.u. voltage. Plots of machine voltage V_m, dc capacitor voltage V_I, and ac load voltage V_{ac}(load) during start–up at 1.0 p.u. speed with load are shown respectively in Figures 68, 69, and 70. Plots of corresponding quantities for Case 1 are shown in Figures 53, 54, and 59. Comparing the Case 3 plots to the Case 1 plots shows that the control system controls the main system quantities V_m, V_I, and V_{ac}(load) equally well whether or not ac load is connected during start–up.

Case 3 plots of I_d, α, and β which are illustrated in Figures 67, 71, and 72 differ from Case 1 plots because the ac load power increases gradually in Case 3 according to the gradual increase in V_{ac}(load) plotted in Figure 70. The gradual change in power order is reflected in I_d*(ord) and I_d plotted in Figure 67 and angle α plotted in Figure 71. The Duty–Cycle Order β which is plotted in Figure 72 remains high throughout the start–up in order to utilize I_d during a large fraction of each period of the boost converter to charge the dc capacitor and supply the inverter.

The Case 3 load voltage V_{ac}(load) which is plotted in Figure 70 stabilizes at essentially 1.0 p.u. voltage prior to ac load rejection at t = 1.35 seconds. Figure

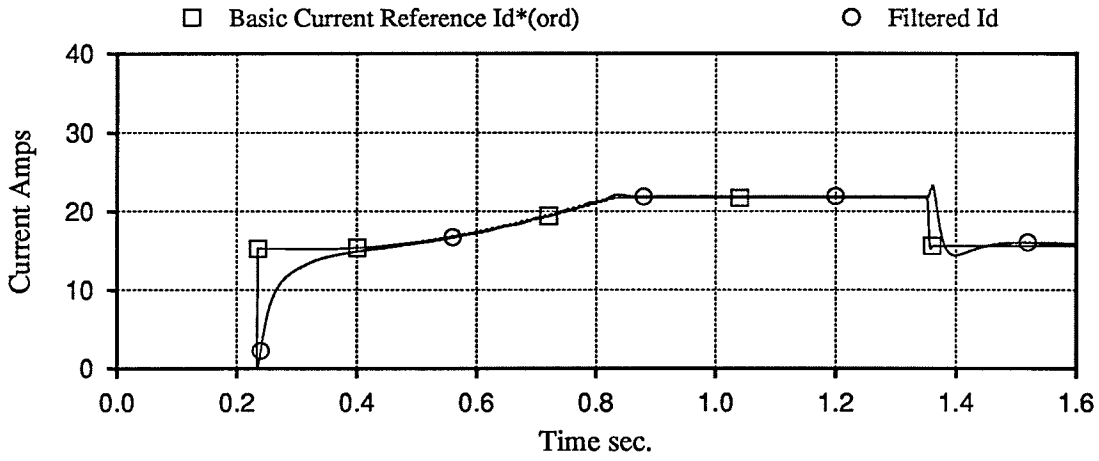


Figure 67. Case 3 – dc Currents I_d*(ord) and I_d

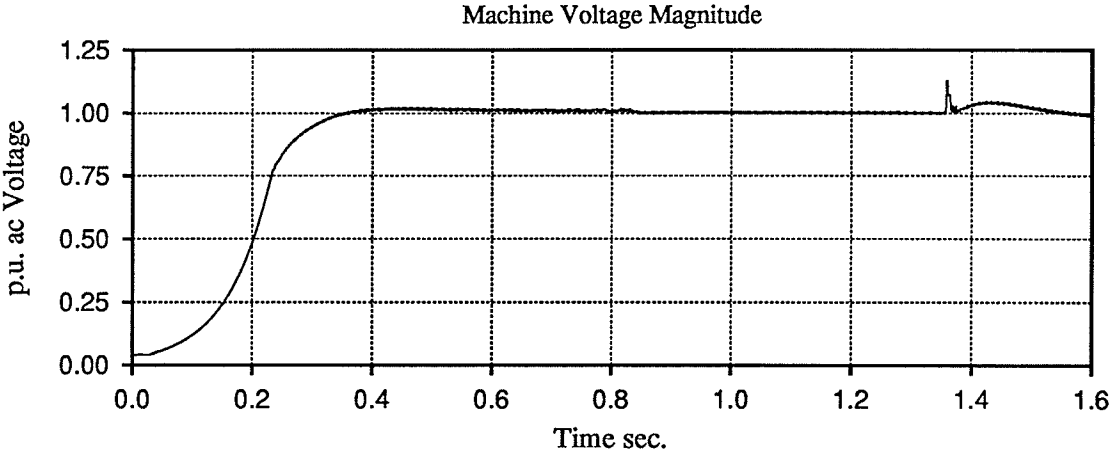


Figure 68. Case 3 – Machine Voltage V_m

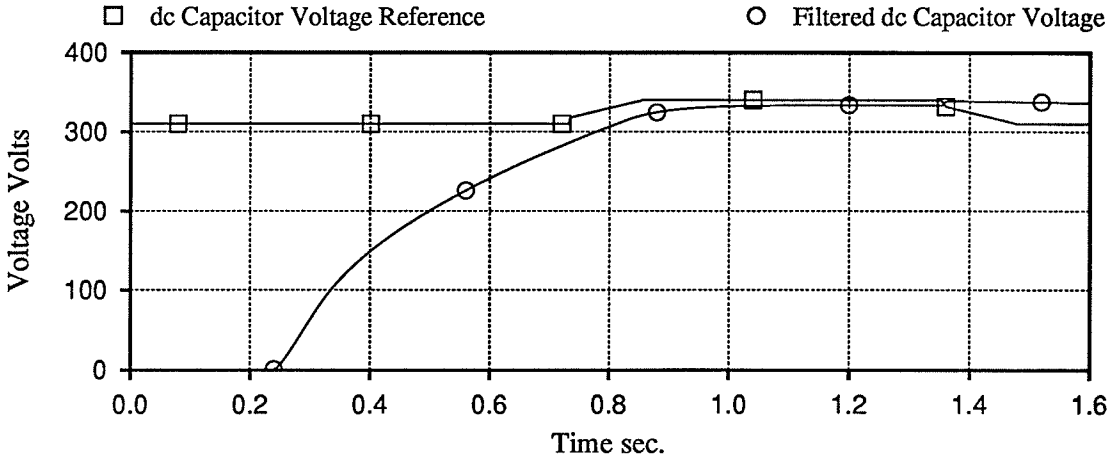


Figure 69. Case 3 – dc Capacitor Voltages V_{Iref} and V_I

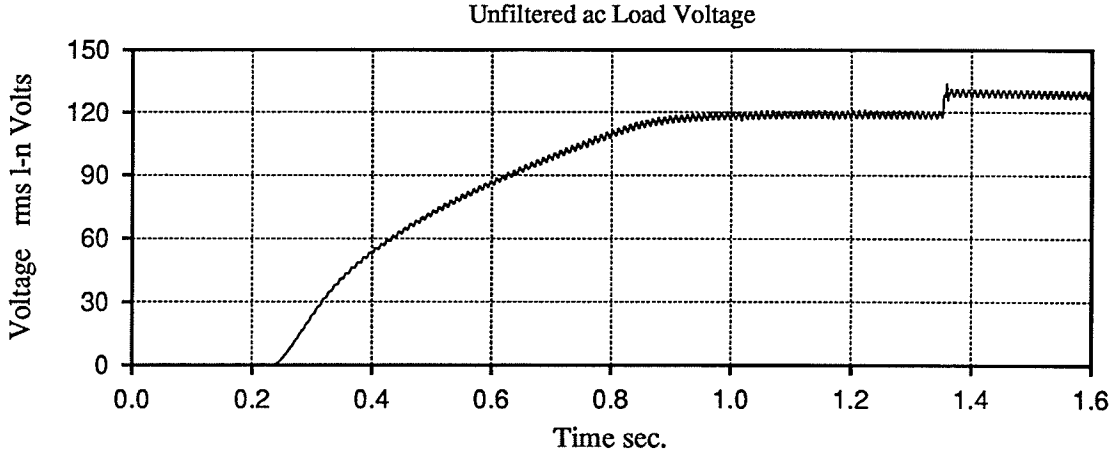


Figure 70. Case 3 – Measured ac Load Voltage

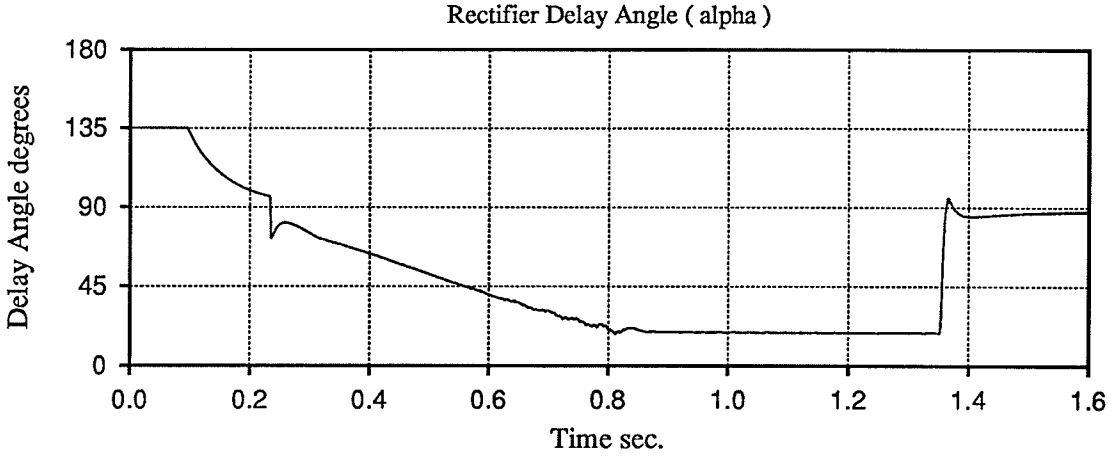


Figure 71. Case 3 – Rectifier Delay Angle α

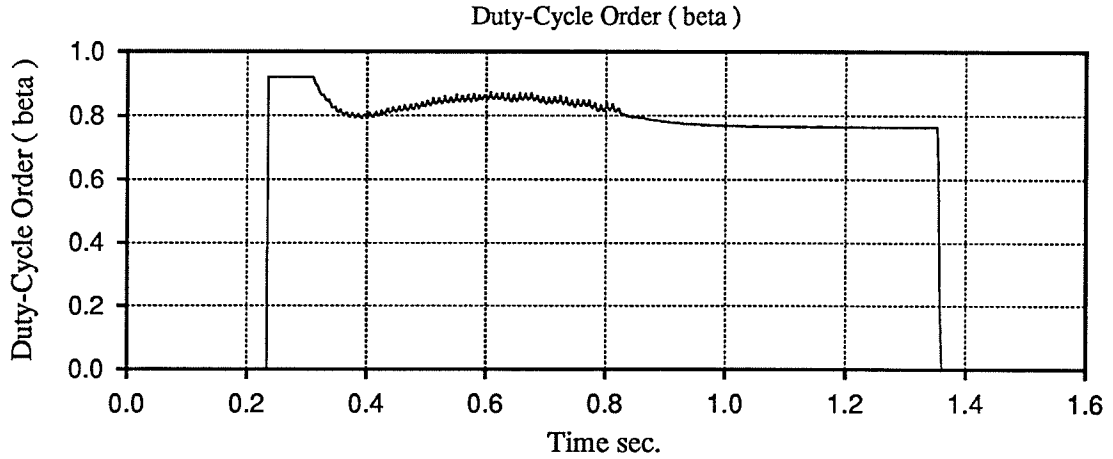


Figure 72. Case 3 – The Duty–Cycle Order β for the Boost Converter

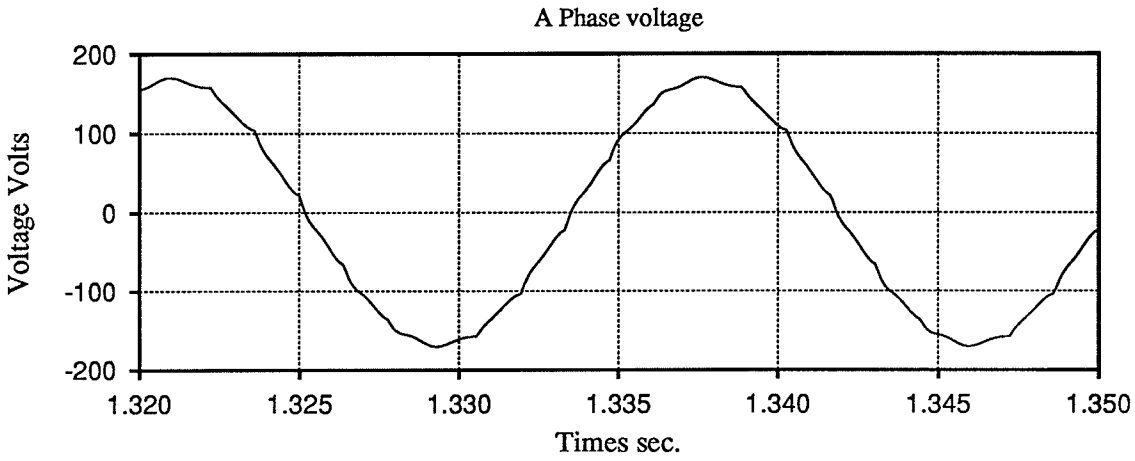


Figure 73. Case 3 – Load Voltage at Full Load

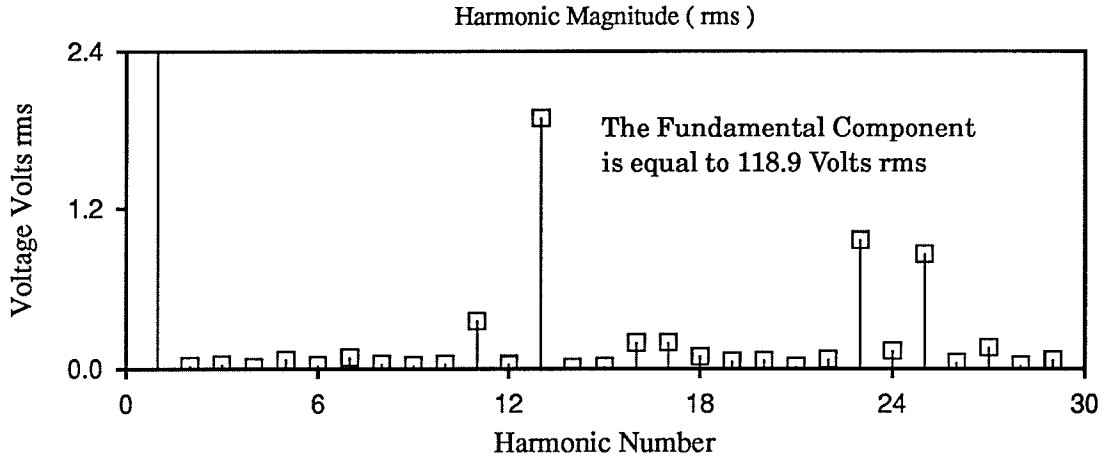


Figure 74. Case 3 – Harmonics of Full Load Voltage

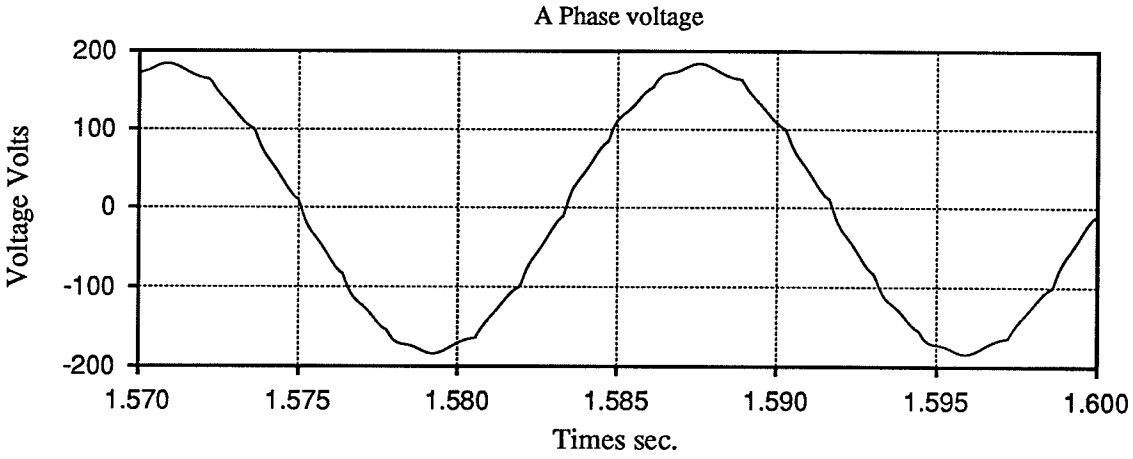


Figure 75. Case 3 – Load Voltage at No Load

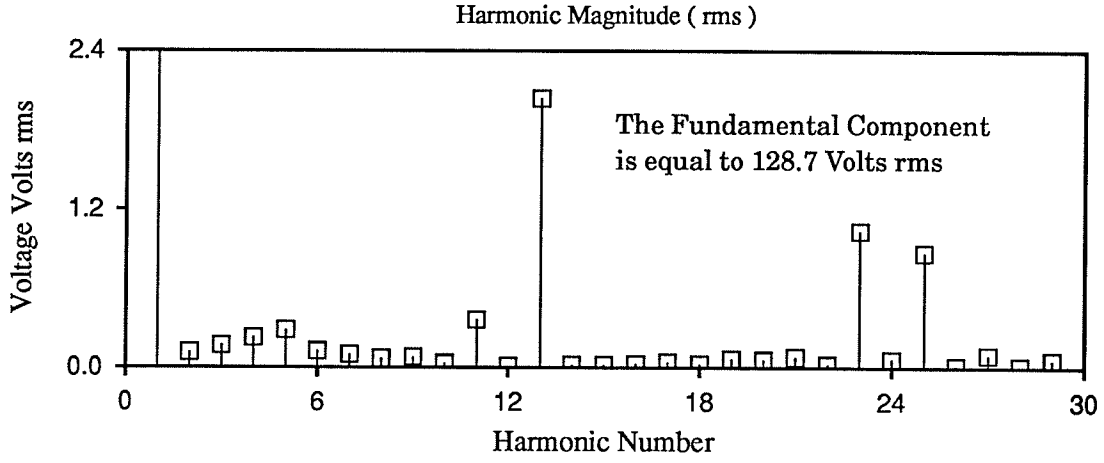


Figure 76. Case 3 – Harmonics of No Load Voltage
(during overvoltage following load rejection)

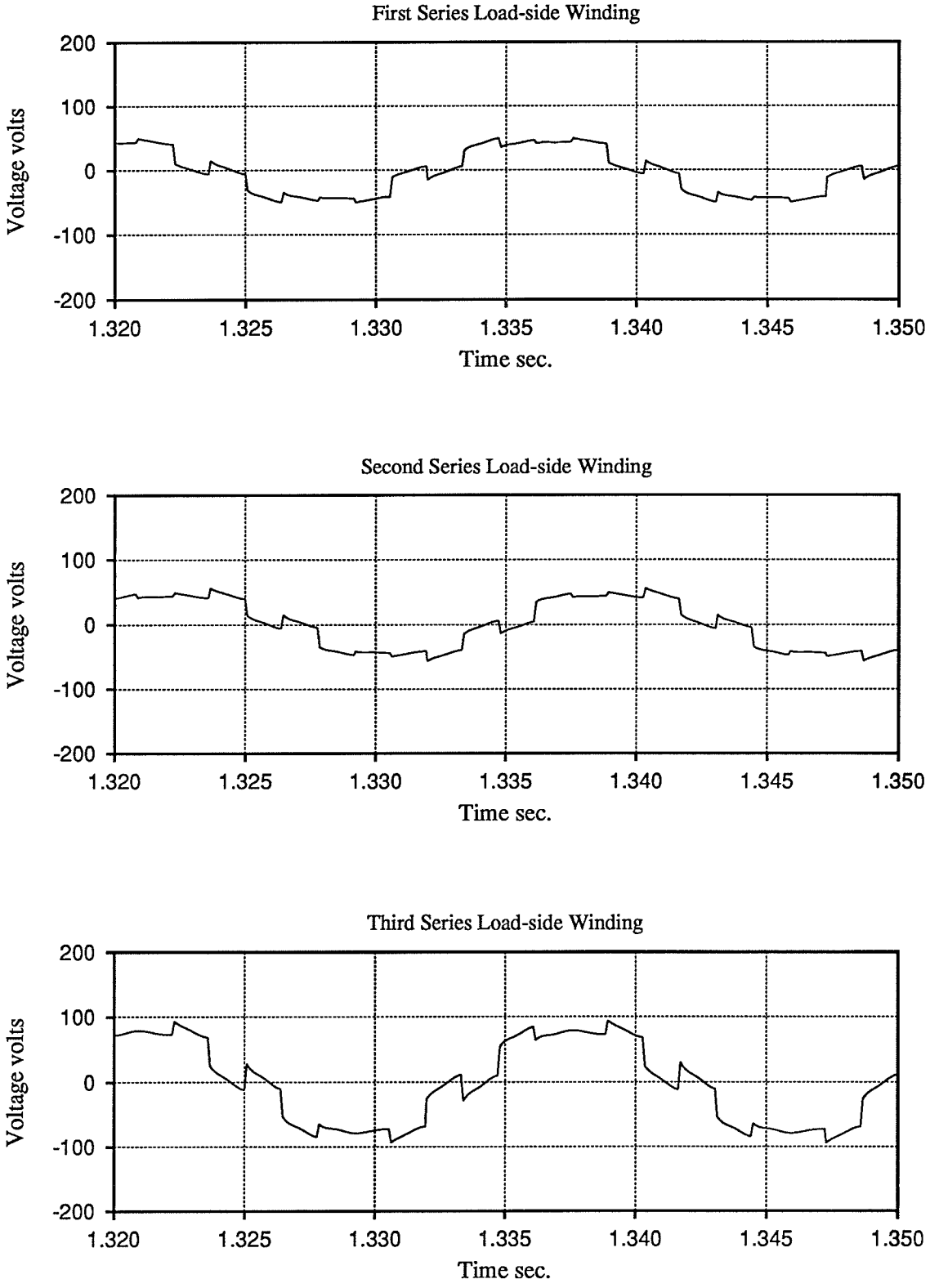


Figure 77. Case 3 – Transformer Contributions to A Phase Load Voltage

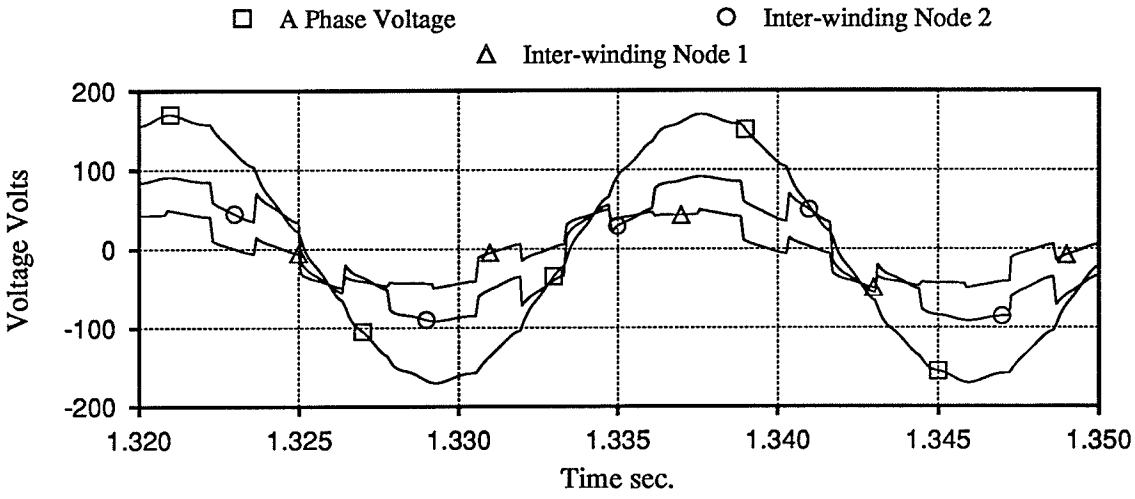


Figure 78. Case 3 – Composition of Load Voltage

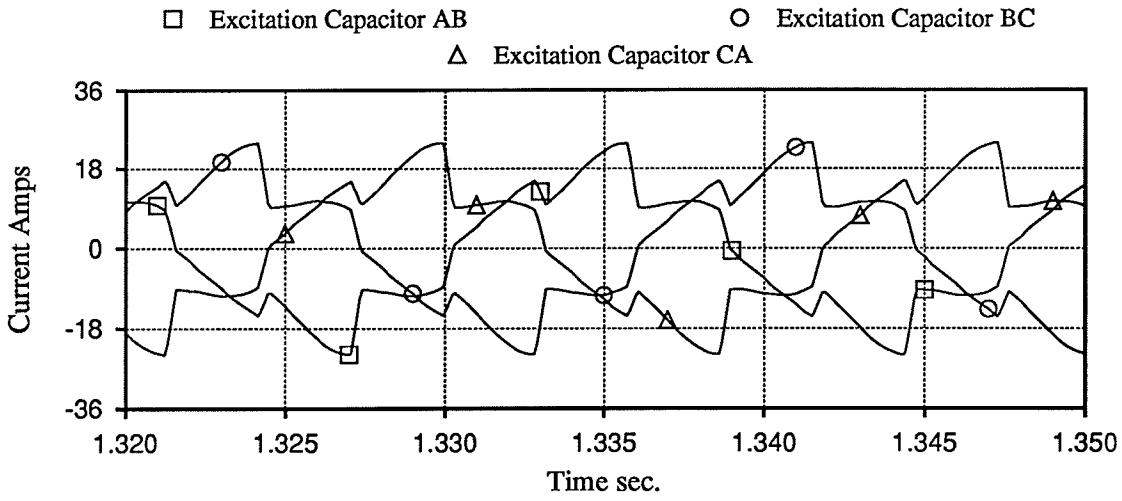


Figure 79. Case 3 – Currents in a Capacitive Loop

73 contains a plot of a cycle of load voltage prior to load rejection. Fourier analysis was performed on the wave to determine the magnitudes of the harmonic components. The magnitudes are given in Figure 74. Figure 74 indicates that the arithmetic sum of the characteristic harmonics below the 30th is approximately 2.9 percent. This level of harmonic content is achieved by using a shunt C–type filter and a shunt tuned 11th harmonic filter located on the ac load bus as shown in Figure 30. The filters are described in Appendix III. A shunt tuned 13th harmonic filter could be added if necessary to further reduce the 13th harmonic voltage illustrated in Figure 74. Figures 75 and 76 illustrate that the ac load voltage waveshape contains approximately the same harmonic content after ac load rejection.

5.4.1 Numerical Oscillation Suppression in the Simulations

Each phase of the ac load voltage in the Case 3 simulation is supplied by three series–connected load–side windings in the inverter transformers as illustrated in Figure 30. Plots of the voltage components provided by the windings are shown in Figure 77. In addition the voltages at the nodes between the series–connected windings are shown in Figure 78. These inter–winding nodes are referred to as inductive nodes because the only branches which are incident on these nodes are the inductive transformer windings. In conventional transients simulation algorithms solutions for voltages at such inductive nodes are often subject to numerical oscillations of two time–step period as described in chapter three. However the plots of the inter–winding node voltages produced by the prototype transients simulation program are free of such numerical oscillations as illustrated in Figure 78. It is therefore apparent that the simulation technique described in chapter 3 does not introduce numerical oscillations in voltages at inductive nodes. In a similar manner, capacitive loops are often subject

to numerical oscillations of two time–step period in the solutions for the currents. Figure 79 contains plots of the currents in the capacitive loop consisting of the delta–connected self–excitation capacitors. It is apparent that the simulation technique described in chapter three does not introduce numerical oscillations of current in the capacitive loop.

5.5 Case 4 – Simulated Performance at 1.4 p.u. Machine Speed during Start–up with Pre–connected ac Load

The conditions for Case 4 are the same as the conditions for Case 3 except that the start–up under ac load occurs at 1.4 p.u. speed in Case 4 rather than at 1.0 p.u. speed. Plots for Case 4 are shown in Figures 80 to 85. Comparison of plots of V_m, V_I, and V_{ac}(load) in Case 4 to corresponding plots in Case 2 make it apparent that having ac load connected during start–up has little impact on the ability of the control system to control the quantities V_m, V_I, and V_{ac}(load). The corresponding Case 2 plots are shown in Figures 62, 63, and 64.

5.6 Conclusions

The main conclusion to be drawn from the simulations is that an effective control system can be implemented to control the thesis apparatus illustrated in Figure 30.

The simulations demonstrate acceptable performance of the control system for load powers ranging between 0.0 and 1.0 p.u. power and for machine speeds in the design range between 1.0 and 1.4 p.u. speed. The ac load voltage during steady–running is regulated to essentially 1.0 p.u. voltage at 60 Hz in these ranges of power and speed. The machine voltage is similarly regulated to essentially 1.0 p.u. voltage.

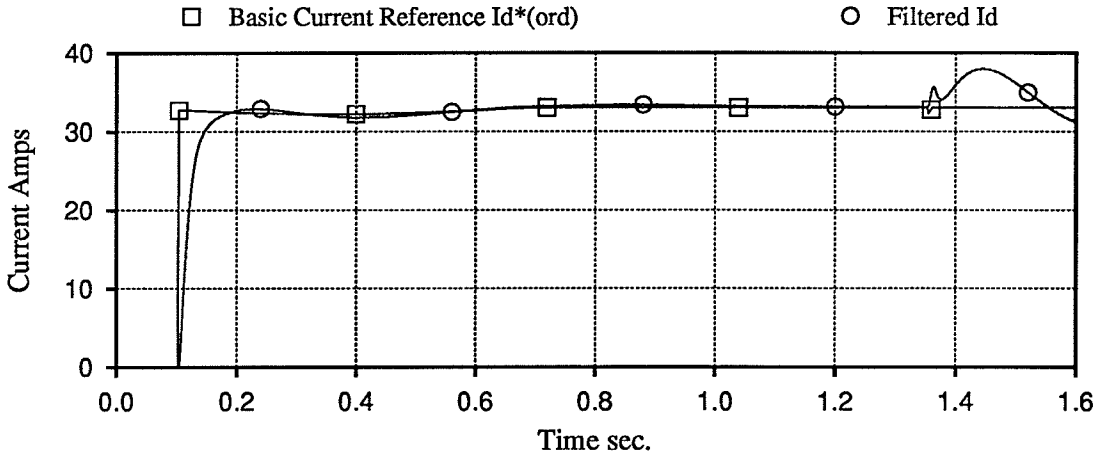


Figure 80. Case 4 – dc Currents I_d*(ord) and I_d

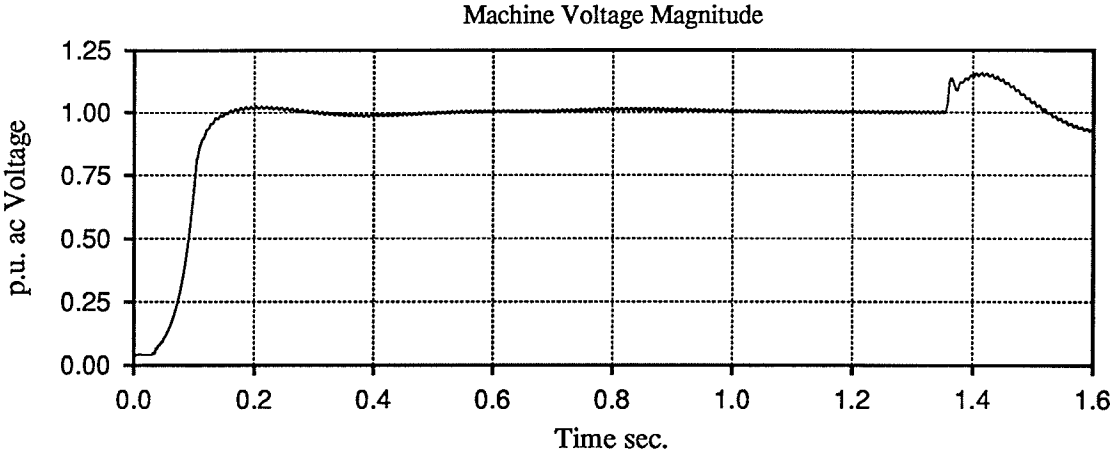


Figure 81. Case 4 – Machine Voltage V_m

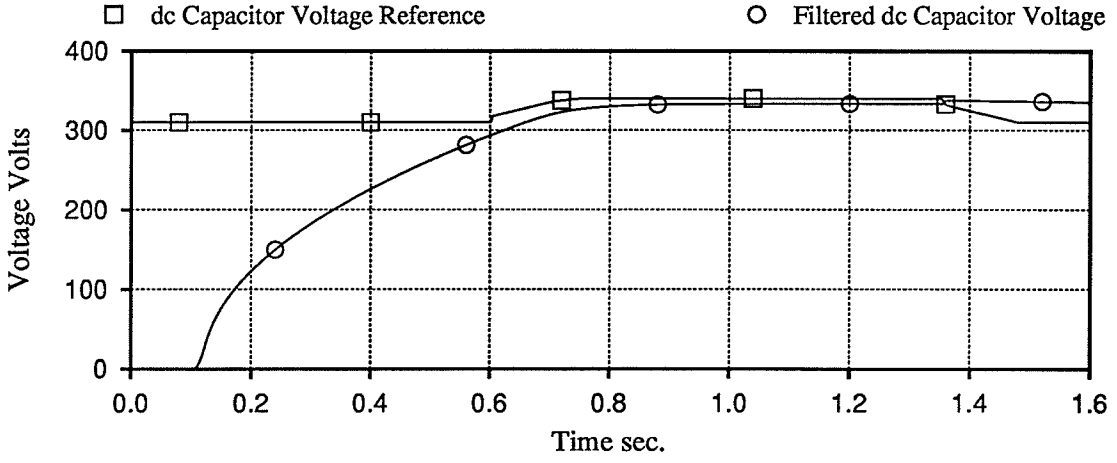


Figure 82. Case 4 – dc Capacitor Voltages V_{Iref} and V_I

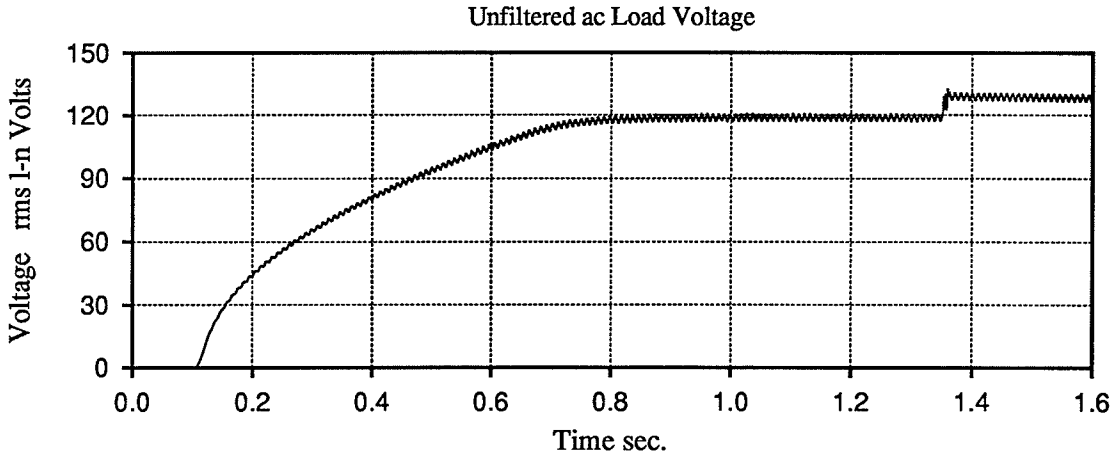


Figure 83. Case 4 – Measured ac Load Voltage

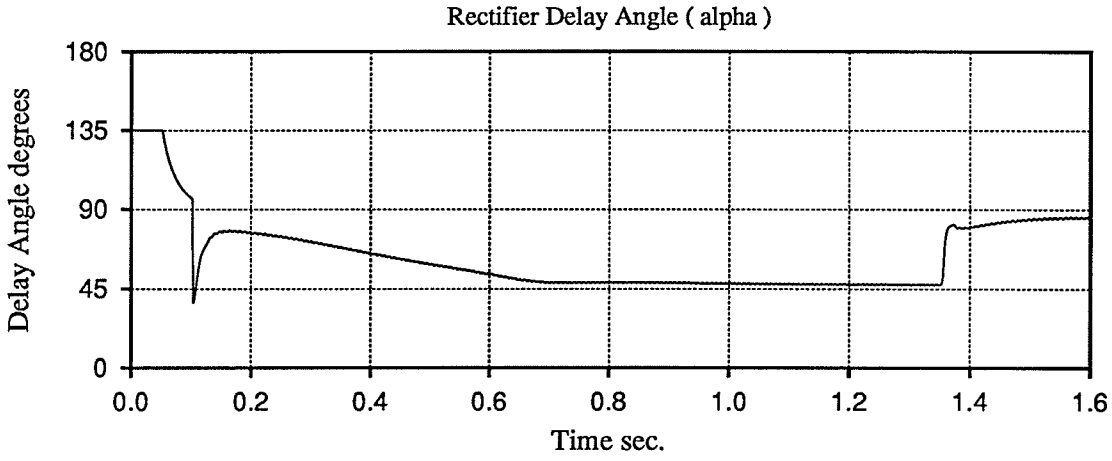


Figure 84. Case 4 – Rectifier Delay Angle α

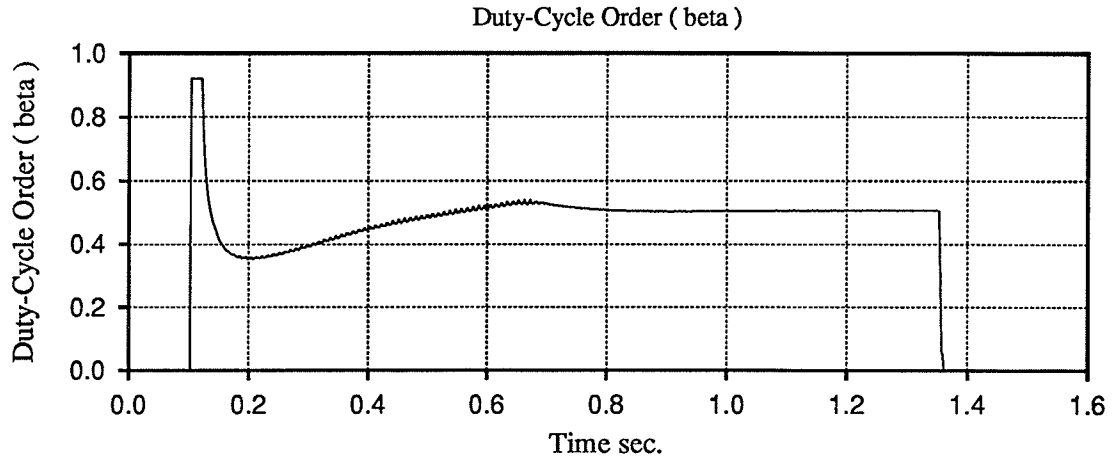


Figure 85. Case 4 – The Duty–Cycle Order β for the Boost Converter

The control system also provides dynamic regulation of the ac load voltage to within plus or minus 12 percent during either instantaneous connection or rejection of full ac load while running at either the minimum or maximum design speed. The control system similarly provides regulation of machine voltage to within plus or minus 18 percent during either instantaneous connection or rejection of full ac load while running at either the minimum or maximum design speed.

An additional conclusion to be drawn from the simulations is that a twelve–pulse voltage–sourced inverter can provide ac load voltage of generally acceptable harmonic content when shunt filtering is provided such as described in Appendix III.

The simulation results presented in this chapter also demonstrate that the simulation techniques described in chapter 3 can be used in simulating a system of moderate size which includes a machine, controls, three different converters, transformers, breakers, lumped elements, filters and ac load.

The efficacy of the simulation techniques and the expected operation of the thesis apparatus are confirmed in the next chapter by comparing laboratory test results to simulation results.

Chapter Six

System Performance Demonstrated through Laboratory Testing

6.1 Introduction

This chapter describes tests conducted on an apparatus that was built in the laboratory for testing as illustrated in Figure 86. The test apparatus is the appa-

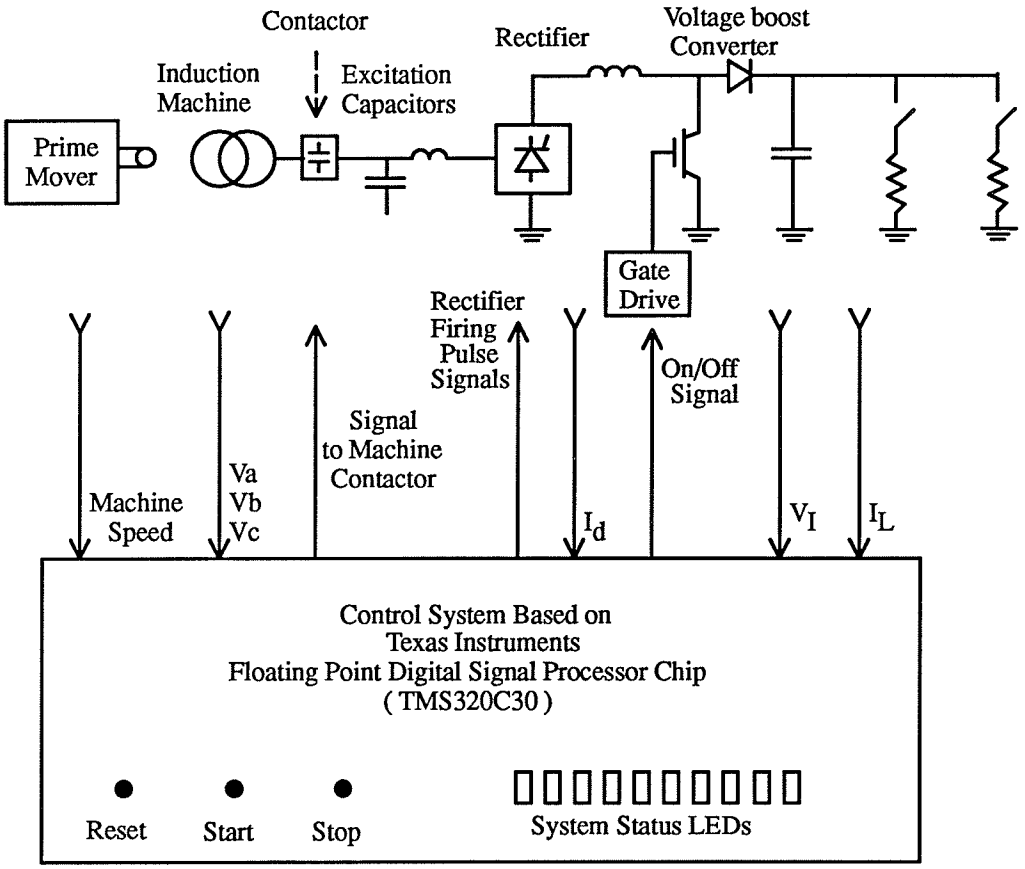


Figure 86. Laboratory Test Apparatus

ratus simulated in chapter five with the exception of the load. The voltage–sourced inverter which is simulated in chapter five tends to appear as a dc load on the voltage–boost converter due to the effective voltage smoothing provided by the dc capacitor. Therefore, a dc load is used in the test apparatus instead

of the voltage–sourced inverter in order to simplify the test apparatus. The experimental control system illustrated in Figure 86 consists essentially of the Main Control illustrated in Figure 32. The test control system does not include the ac Load Voltage PI Controller (Figure 33) because the inverter and ac load are not included in the test apparatus. The ac Load Voltage PI Controller can be omitted from the test apparatus because it is mainly intended to correct for the significant variations in voltage drop across the inverter transformer. The other errors corrected by the ac Load Voltage PI Controller are comparatively minor.

The apparatus testing described below confirms the ability of the Main Control to control the rectifier and voltage–boost converter in the desired coordinated manner. In that regard, the control regulates machine voltage V_m to 1 p.u. voltage and causes the apparatus to supply the dc load according to a fixed reference voltage V_{Iref} of 310 Volts. In the test results presented below there is very little error in the load voltage V_I even without the error correcting action of the ac Load Voltage PI Controller. In the full apparatus the ac Load Voltage PI Controller produces V_{Iref} as an intermediate signal which is adjusted by the Controller to remove all error in the load voltage.

Figure 87 contains a photograph of the laboratory apparatus. The induction machine is shown at the center left of the photograph. A high power factor machine as described in Appendix I is used in order to keep the capacitance of the self–excitation capacitors as small as possible. The resulting smaller capacitance reduces the level of excess VARS produced by the capacitors during high speed operation. The reduction in output of excess VARS in turn reduces the current ratings of the rectifier; the dc smoothing inductor; and the voltage–boost converter. A contactor is provided between the machine and the self–excitation capacitors as illustrated in Figure 86. The control system opens and closes the

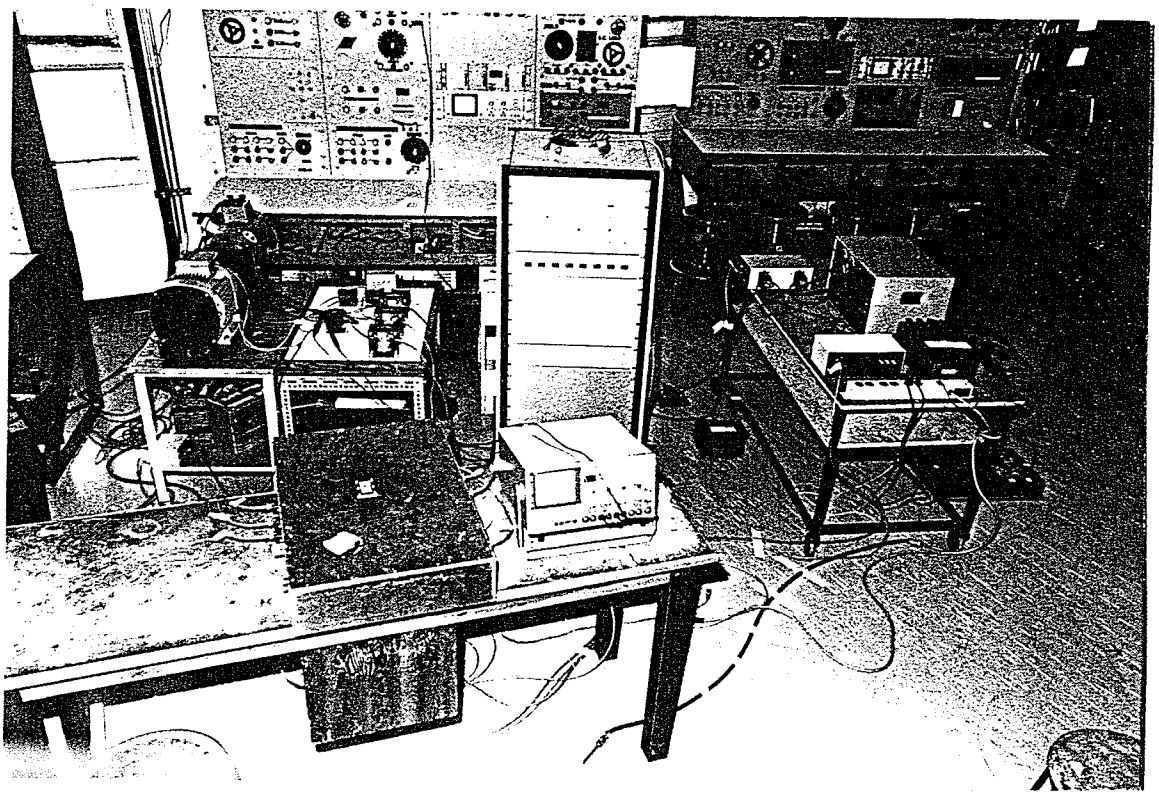


Figure 87. A Photograph of the Laboratory Test Apparatus.

contactor to start and stop the operation of the apparatus. The rectifier in the test apparatus is included in the upright cubicle shown in the center of Figure 87. The rectifier was available in the laboratory due to an earlier research project. The voltage–boost converter is in the large box on the table shown in the right–hand side of Figure 87. Figure 88 contains a photograph looking into the back of the voltage–boost converter enclosure. The voltage–boost converter includes a 50 Amp 1000 Volt IGBT (insulated gate bipolar transistor) device. An IGBT gate firing card including a fibre optic isolation link was designed and built as part of the thesis work. The digital control system is housed in the box on the table in the foreground of Figure 87. Figure 89 contains a photograph looking into the top of the control enclosure.

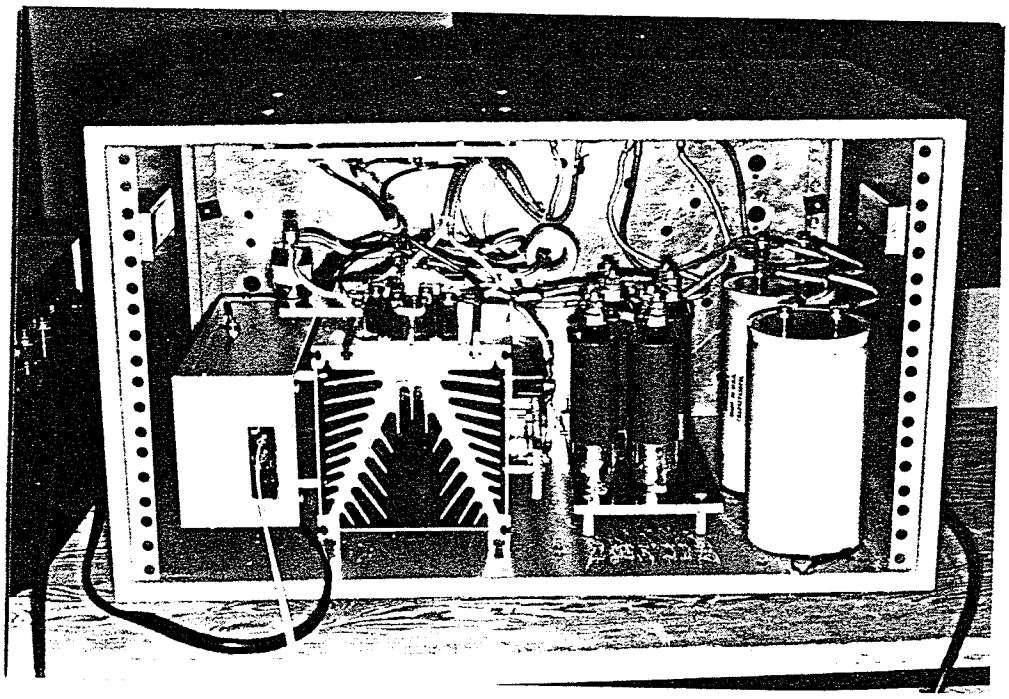


Figure 88. A Photograph of the Voltage–boost Converter

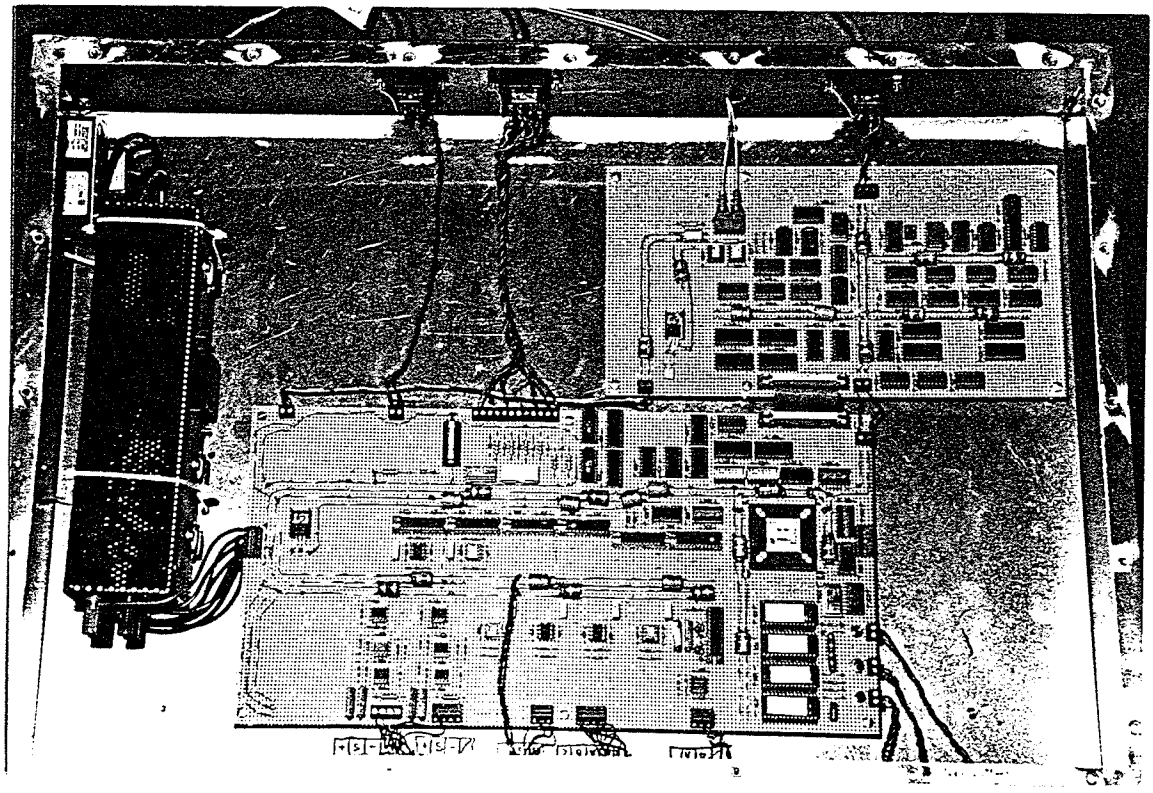


Figure 89. A Photograph of the Apparatus Control System

The control system illustrated in Figure 89 is based on a 33 MHz Texas Instruments TMS320C30 DSP (digital signal processor) chip. The control system was fabricated on a wire–wrap board for the tests. The basic architecture of the control system is illustrated in Figure 90. The control system also implements four protective functions as indicated by labelling on the LEDs (light emitting diodes) in Figure 90. The control system acts to shut–down the apparatus if it senses unacceptable machine overvoltage; dc inductor overcurrent; machine overspeed; or dc capacitor overvoltage. The control system effects shut–down by opening the machine contactor to disconnect the machine from the self–excitation capacitors and the rectifier. Shutdown action includes continuous conduction of the GTO device in the boost converter and firing of the rectifier at 90 degrees.

The prime mover in the test apparatus is a 10 horsepower induction machine supplied from a variable frequency machine drive.

The next five sections of this chapter present the test results from five groups of tests conducted on the apparatus. The laboratory results are compared to simulation results for each test. One purpose of presenting the comparisons is to demonstrate how well the simulation results represent the performance of the actual hardware. Differences between actual responses and simulated responses are discussed. The five groups of tests illustrate good performance for:

1. start–up of the apparatus with and without connected load at both high and low speed;
2. application of approximately full load in one step at both high and low speed;
3. waveshapes during steady–running;
4. rejection of approximately full–load at both high and low speed; and
5. application of and recovery from overload.

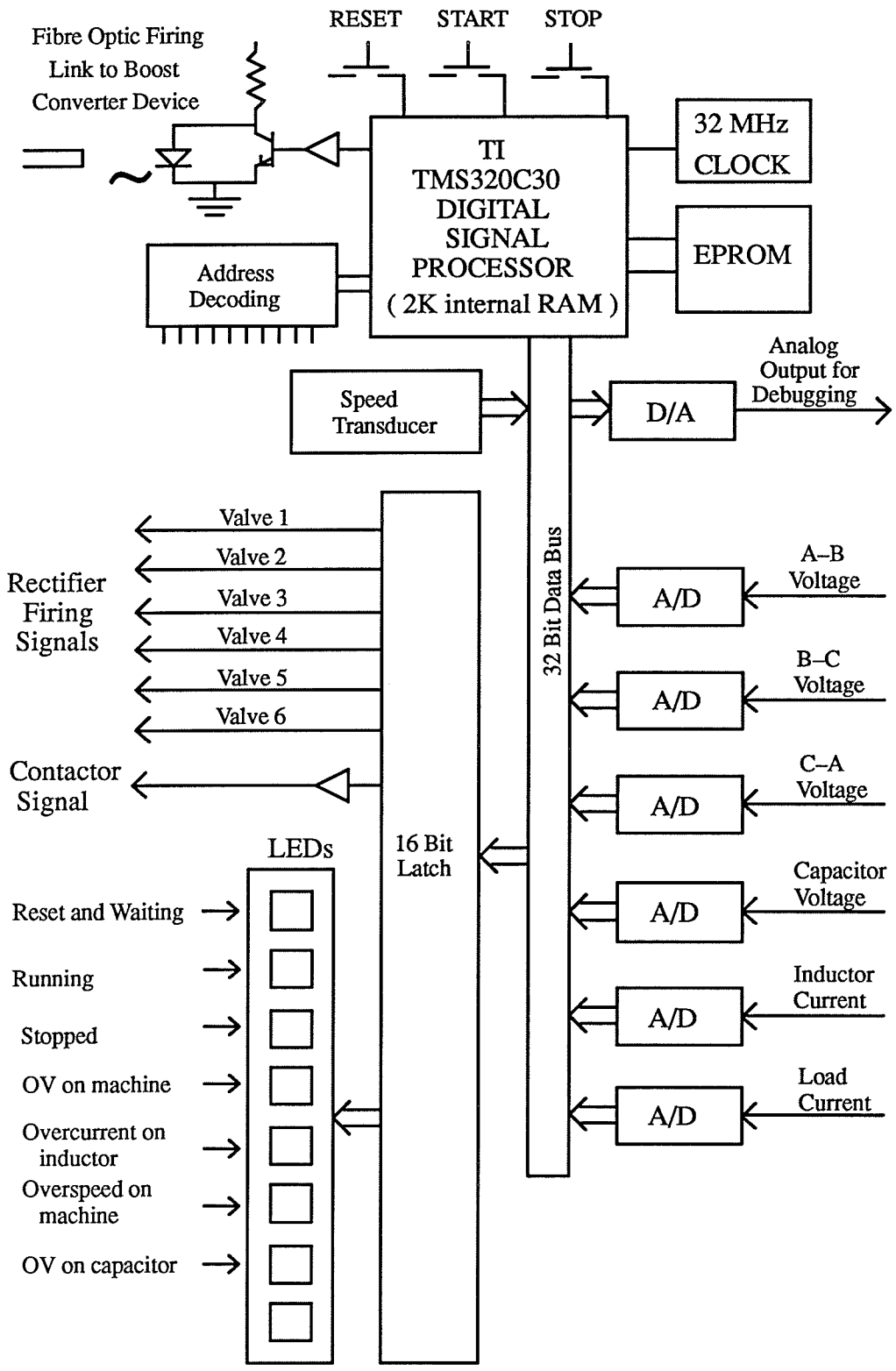


Figure 90. The Basic Architecture of the Digital Control

6.2 Demonstration of the Apparatus during Start–up

The first group of four tests involves starting the apparatus at various speeds and with different connected loads.

The start–up conditions in Tests 1 to 4 correspond respectively to the start–up conditions simulated in Cases 1 to 4 in chapter five with only minor differences. The first minor difference is that the dc load resistance in Tests 3 and 4 is selected to draw 0.95 p.u. power while the load simulated in Cases 3 and 4 in chapter five is selected to draw 1.0 p.u. power. In addition the load in Tests 3 and 4 is a dc load while the load in Cases 3 and 4 in chapter five includes a voltage–sourced inverter supplying an ac load.

Test 1 involves starting the apparatus at 1.0 p.u. machine speed with no dc load connected.

Test 2 involves starting the apparatus at 1.38 p.u. machine speed with no dc load connected.

Tests 3 and 4 are respectively repeats of Tests 1 and 2 except that a dc load is connected during start–up. The dc load resistance is such that it draws 0.95 p.u. power at 1.0 p.u. dc capacitor voltage (i.e. 5.32 kW at 310 Volts).

In Tests 1 to 4 the laboratory results are compared to results obtained from transients simulations of the laboratory apparatus.

6.2.1 Test 1 – No Load Start at 1.0 p.u. Speed

Test 1 compares laboratory results and simulation results for starting of the laboratory apparatus at 1.0 p.u. machine speed with no dc load connected. Figure 91 shows plots of dc inductor current, machine voltage, and dc capacitor voltage obtained during starting of the real laboratory apparatus. The plots shown in Figure 91 begin slightly after the machine contactor shown in Figure 86 is

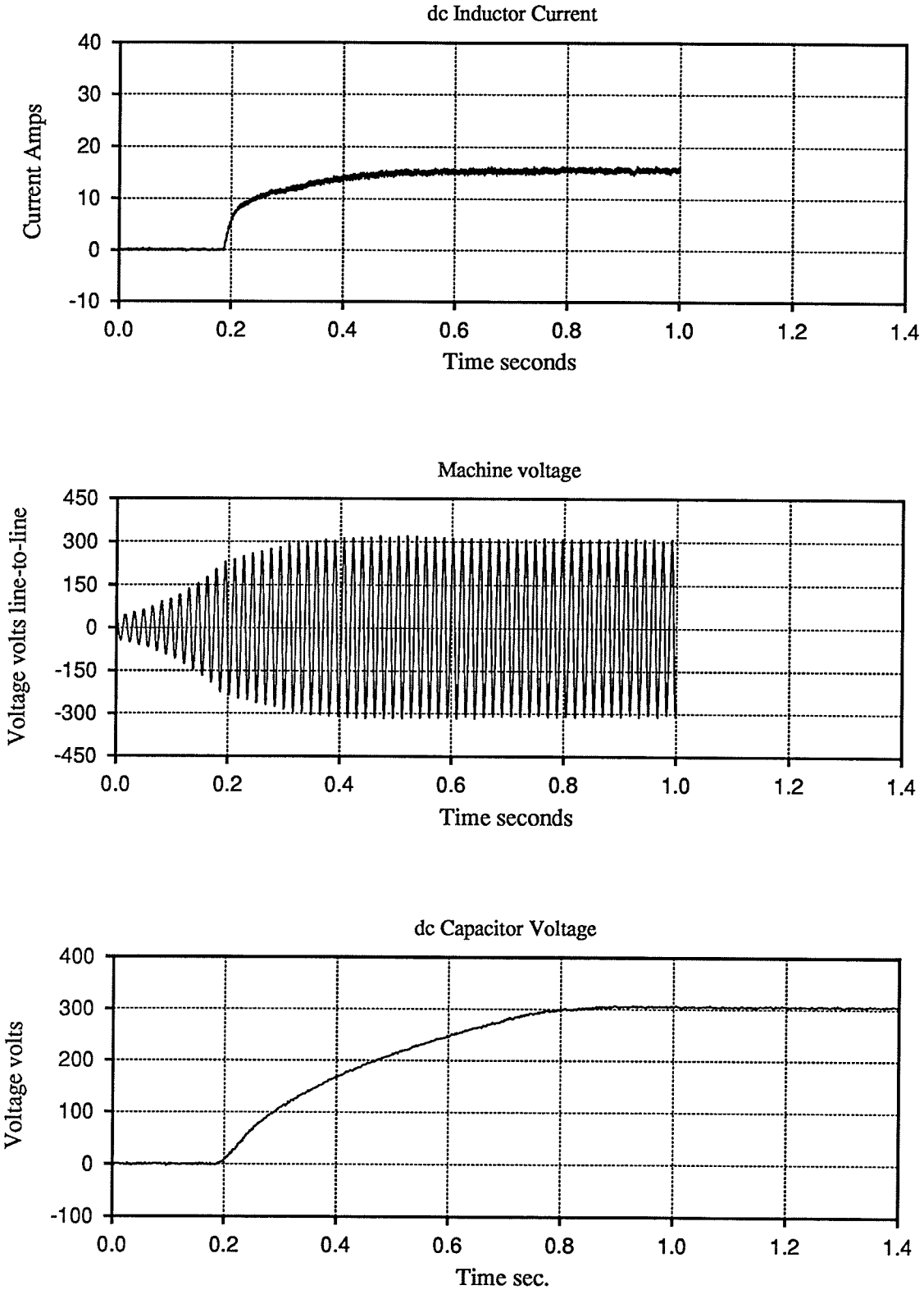


Figure 91. Test 1 – Laboratory Test Results for a No Load Start at 1.0 p.u. Speed

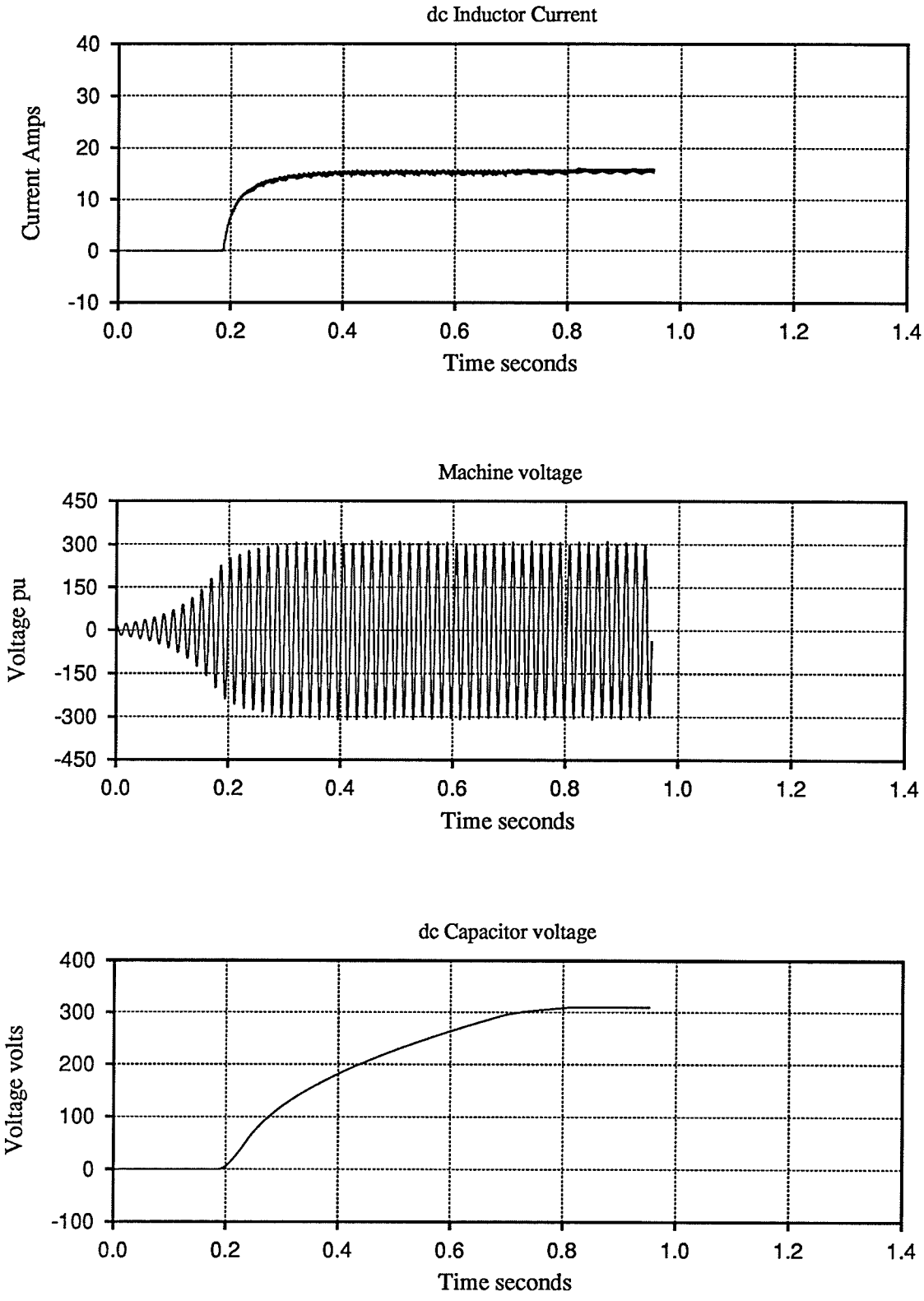


Figure 92. Test 1 – Simulation Results for a No Load Start at 1.0 p.u. Speed

closed and end only after all plotted magnitudes have become steady. Figure 92 shows corresponding simulation results for starting of the laboratory apparatus in Test 1 starting conditions. Some small differences exist because the growth of self–excitation voltage is very sensitive to the dc current order and the actual non–linear magnetizing current curve for the machine.

The test results (Figure 91) show that the dc capacitor voltage is controlled to a stable voltage of about 307 Volts (measured using a dc voltmeter). The small error between V_I and V_{Iref} (i.e 310 Volts) is of no consequence in the full apparatus described in chapter five. In the full apparatus, the ac Load Voltage PI Controller produces V_{Iref} as an intermediate signal and adjusts V_{Iref} as required in order to obtain the requested ac load voltage. The simulation result shown in Figure 92 and the laboratory result shown in Figure 91 illustrate approximately the same transient response for the dc capacitor voltage during starting with the Test 1 starting conditions.

The rated machine voltage is 120 Volts RMS line–to–neutral or 294 Volts peak line–to–line. Both Figures 91 and 92 show that the machine voltage peak line–to–line magnitude is about 305 Volts which is larger than the rated value of 294 Volts. The plotted machine voltage waveshapes exhibit peak values higher than expected only due to harmonic distortion of the voltage waveshape. The distortion of the machine voltage waveshape is shown in detail in the plots for Test 8 below (Figure 106).

The plot of dc inductor current obtained from laboratory testing shown in Figure 91 compares well with the plot obtained from simulation shown in Figure 92. The final values of dc current compare well. The differences in the plotted transient responses are minor. Similar differences in transient responses are discussed in more detail during discussion of Test 2 results below.

6.2.2 Test 2 – No Load Start at 1.38 p.u. Speed

Test 2 compares laboratory results to two separate simulation results for starting of the apparatus with no dc load connected as in Test 1 but at 1.38 p.u. machine speed. Figure 93 shows plots obtained during starting of the real laboratory apparatus. As in Test 1, the plots shown in Figure 93 begin slightly after the machine contactor is closed. Figure 94 shows simulation results for Test 2 starting conditions. Figure 95 shows results from an additional simulation for Test 2 starting conditions but with the PI controller in the Rectifier Current Controller initialized to 1.5 Amps instead of zero Amps. The simulation results and laboratory results show that the control system regulates machine voltage and the output dc capacitor voltage to desired steady levels.

The plot of dc capacitor voltage (Figure 94) obtained by transients simulation for Test 2 starting conditions compares well with the corresponding plot (Figure 93) obtained during laboratory testing.

It is useful to note the close correspondence between the plot of dc inductor current and the shape of the envelope of machine voltage magnitude shown in Figure 93. The similar shape exists because the basic dc current reference I_d*(ord) is multiplied by machine voltage magnitude V_m in the Rectifier Current Controller as discussed in chapters four and five. The influence of machine voltage magnitude V_m on dc current I_d exists in every laboratory and simulation result.

There are notable differences between the plot of dc inductor current I_d obtained by simulation (Figure 94) as compared to the corresponding plot obtained during laboratory testing (Figure 93) for Test 2 starting conditions. The steady–running level of I_d in the simulation result (Figure 94) closely matches the basic dc current reference I_d*(ord) provided by the Look–up Tables of about

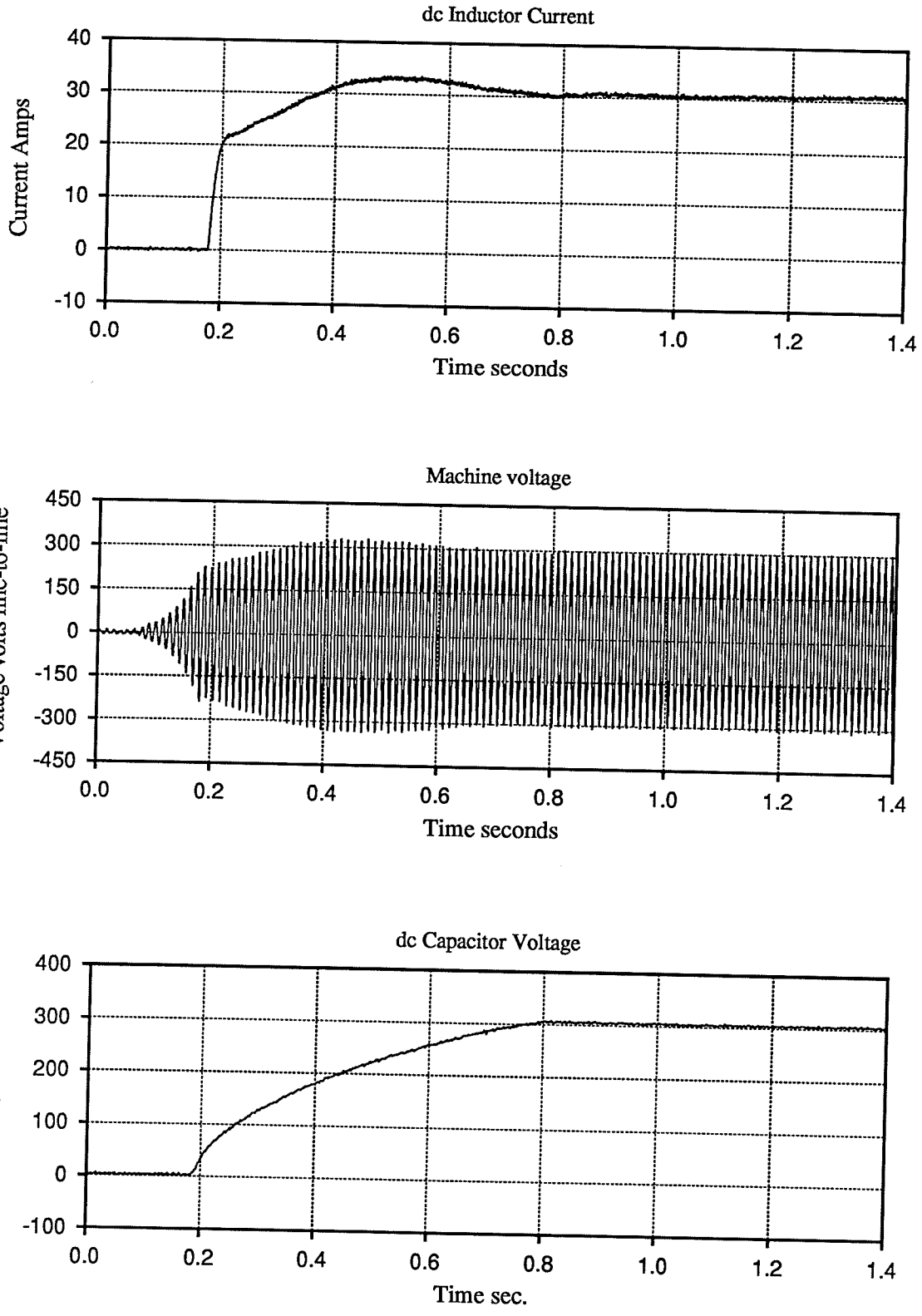


Figure 93. Test 2 – Laboratory Test Results for a No Load Start at 1.38 p.u. Speed

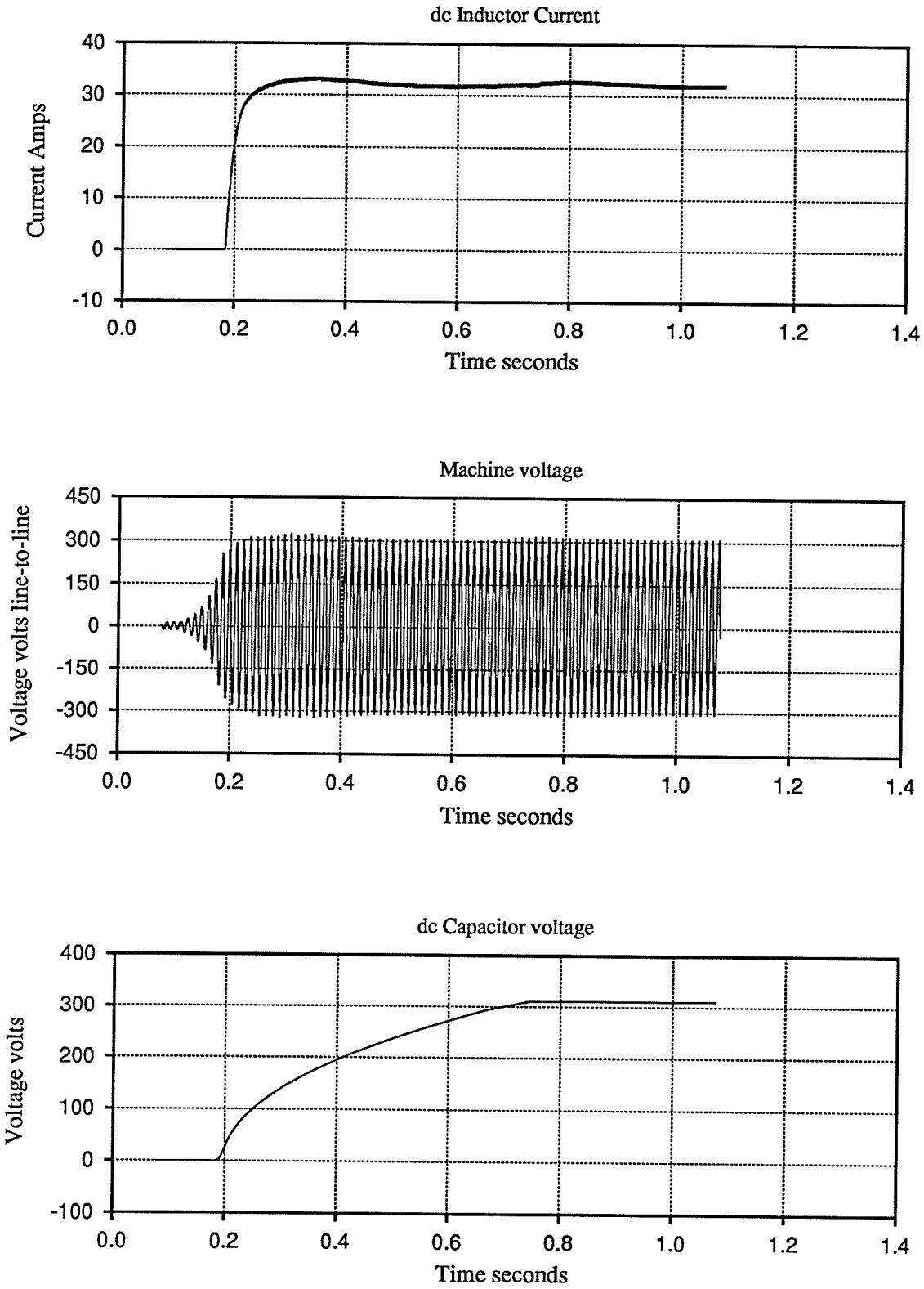


Figure 94. Test 2 – Simulation Results for a No Load Start at 1.38 p.u. Speed

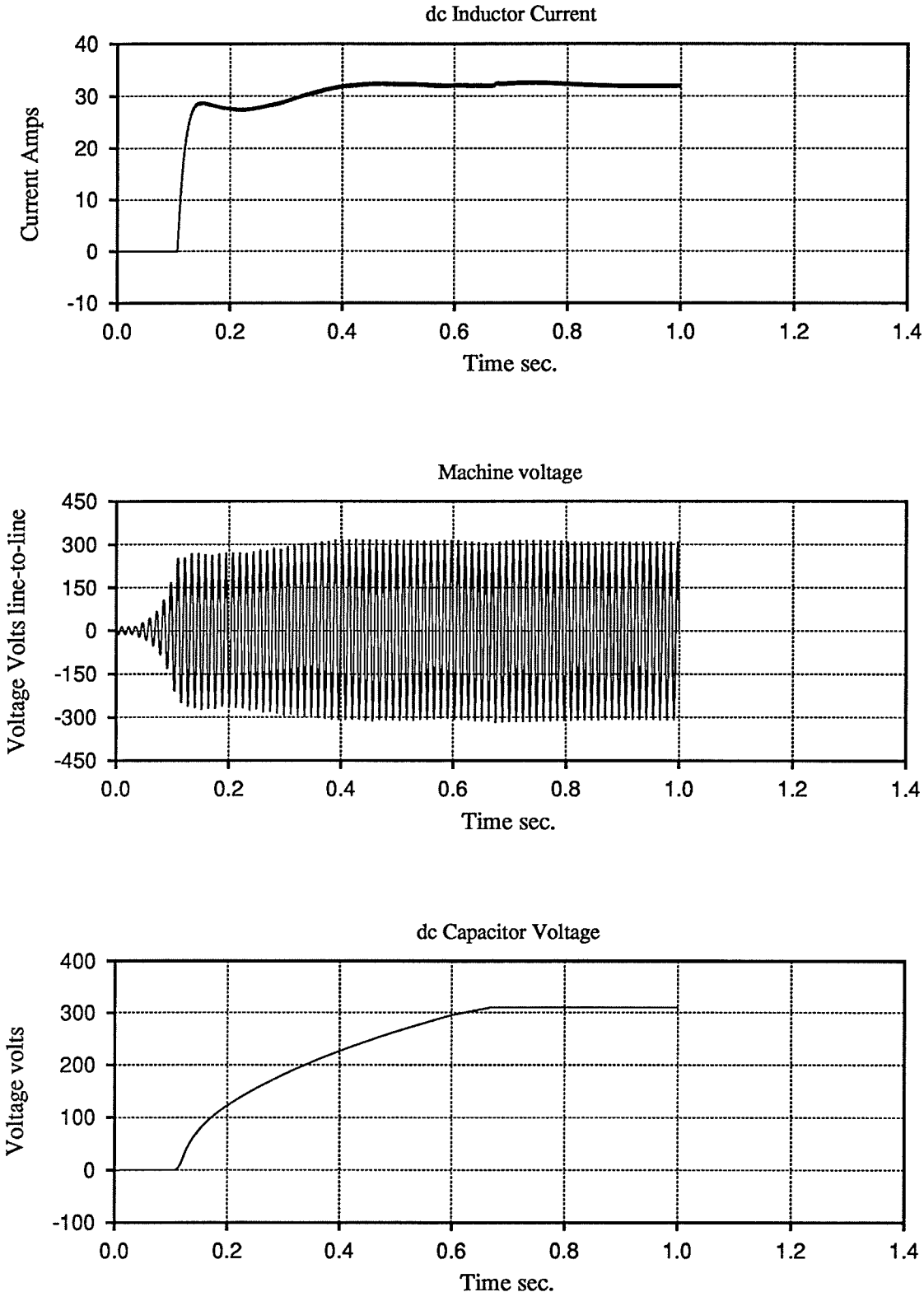


Figure 95. Test 2 – Simulation Results for a No Load Start at 1.38 p.u. Speed with an Altered Integrator Initial Condition

32 Amps as illustrated in Figure 7 for 1.38 p.u. speed and no load. The Look–up Tables therefore provide an output I_d*(ord) which closely matches the Figure 94 simulation result. The Look–up Tables can be expected to give the correct output in the simulation because the machine model used in developing the Look–up Tables uses precisely the same parameters and magnetizing curve as the transients simulation model of the machine.

However, the steady–running level of I_d in the corresponding laboratory result (Figure 93) is about 6% (i.e. 2 Amps) less than I_d*(ord). The Look–up Tables are therefore in error for the actual apparatus in that the tables provide a value of I_d*(ord) which is about 2 Amps too high.

As noted above, the Look–up Tables provide output which is almost ideally suited for controlling the model of the simulated apparatus. However, in actual service, the Look–up Tables do not represent the real apparatus with the same level of precision. For that reason, a PI controller is provided in the Rectifier Current Controller which forces small adjustments in I_d relative to I_d*(ord) in order to regulate V_m to the desired level of 1.0 p.u. machine voltage. The output of the slow–acting PI controller must adjust in the real apparatus to correct for the noted error in the Look–up Tables. A corresponding adjustment does not occur during the simulation. The needed activity of the slow–acting PI controller in the real laboratory apparatus indicates that the laboratory responses must differ to some degree from the corresponding simulated responses.

It is noted above that the Look–up Tables provide a value of I_d*(ord) which is about 6% (i.e. 2 Amps) too high as compared to the steady–running level of I_d which was measured in the laboratory for Test 2 conditions. Therefore the Look–up Tables contribute somewhat too much to the dc current order I_d(ord) when the actual rectifier deblocks in Test 2. The slightly excessive dc current

order existing when the actual laboratory apparatus deblocks can be expected to suppress the growth rate of machine voltage V_m as compared to the growth rate of V_m in the simulation. Figure 93 illustrates that the growth rate of machine voltage V_m after the rectifier deblocks in the laboratory test is in fact suppressed as compared to the simulated growth rate illustrated in Figure 94.

An additional transients simulation was run for Test 2 starting conditions in order to confirm the effect of a slightly excessive dc current order I_d(ord) on the growth rate of machine voltage V_m. The dc current order I_d(ord) is made initially larger in the additional simulation by initializing the integrator in the PI controller in the Rectifier Current Controller to 1.5 Amps instead of to 0 Amps. The plots for the additional simulation result are illustrated in Figure 95. The integrator adjusts generally downward during the modified additional simulation because the dc current I_d in Figure 95 settles to match the component of current order provided by the Look–up Tables (i.e. I_d*(ord) = 32 Amps). The envelope of the machine voltage V_m obtained in the additional simulation and plotted in Figure 95 exhibits a suppression in the growth rate of the machine voltage. The suppression in the growth rate of the machine voltage has a general resemblance to the suppression exhibited in the plot of machine voltage obtained from laboratory testing as illustrated in Figure 93. The additional simulation therefore verifies the general magnitude of the effect that can be caused by a slightly excessive dc current order brought on by error in the Look–up Tables.

The Test 2 results point out a difficulty which can be encountered in simulating apparatus which is controlled by the combination of a fast–acting feed–forward control which is based on a model and a slow–acting feed–back control loop which corrects for errors in the model. The simulated response plotted in Figure 94 is too close to ideal because the model used in feed–forward control is almost precisely correct for the simulated model of the apparatus. In a simulation an

overly precise feed–forward type control can obviate any significant activity by the slow–acting feed–back control loop. If the feed–forward control model does not match the real apparatus as well as the model matches the simulated apparatus then the slow–acting feed–back control loop will have a larger role in the real apparatus. A larger role for the slow–acting feed–back control loop in the real apparatus means the response of the real apparatus will be less close to ideal than the response obtained from simulation.

6.2.3 Test 3 - Start Under Load at 1.0 p.u. Speed

Test 3 is similar to Test 1 except that a dc load is connected during start–up at 1.0 p.u. speed in Test 3. The dc load is such that it draws 0.95 p.u. power at 1.0 p.u. dc capacitor voltage. Plots of actual and simulated dc inductor current I_d are shown respectively in Figures 96 and 97. The control system is able to bring the apparatus to steady–running operation at desired levels of machine voltage V_m and output dc capacitor voltage V_I commencing with no machine voltage at 1.0 p.u. machine speed and with a connected dc load of 1.05 p.u. resistance.

6.2.4 Test 4 - Start Under Load at 1.38 p.u. Speed

Test 4 is similar to Test 2 except that a dc load is connected during start–up at 1.38 p.u. speed in Test 4. The dc load has a resistance of 1.05 p.u. as in Test 3. Plots of actual and simulated dc inductor current I_d are shown respectively in Figures 98 and 99. The control system is able to bring the apparatus to steady–running operation at desired levels of machine voltage V_m and output dc capacitor voltage V_I commencing with no machine voltage at 1.38 p.u. machine speed and with a connected dc load of 1.05 p.u. resistance.

Tests 1 to 4 utilize laboratory apparatus to demonstrate that the control system can start the apparatus and regulate machine voltage V_m and output volt-

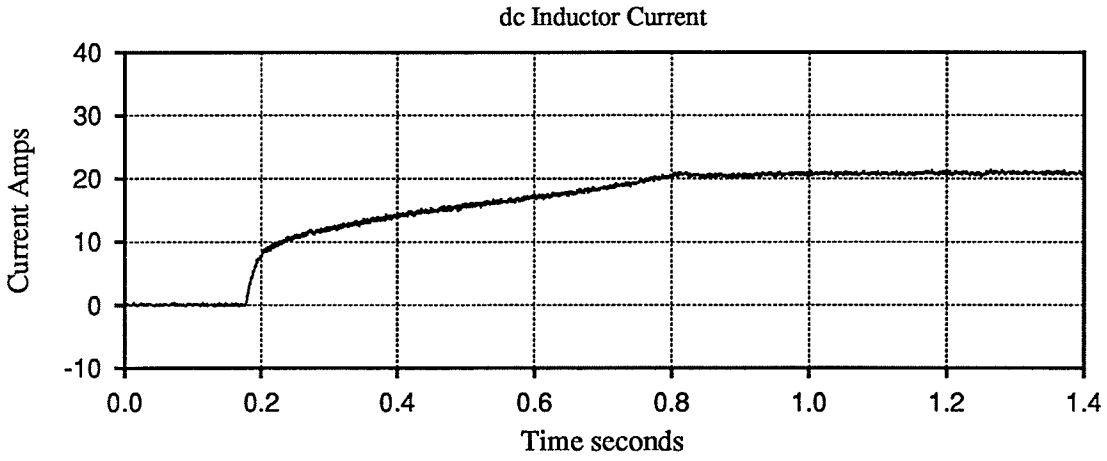


Figure 96. Test 3 – Laboratory Result for Start–up Under Load at 1.0 p.u. Speed

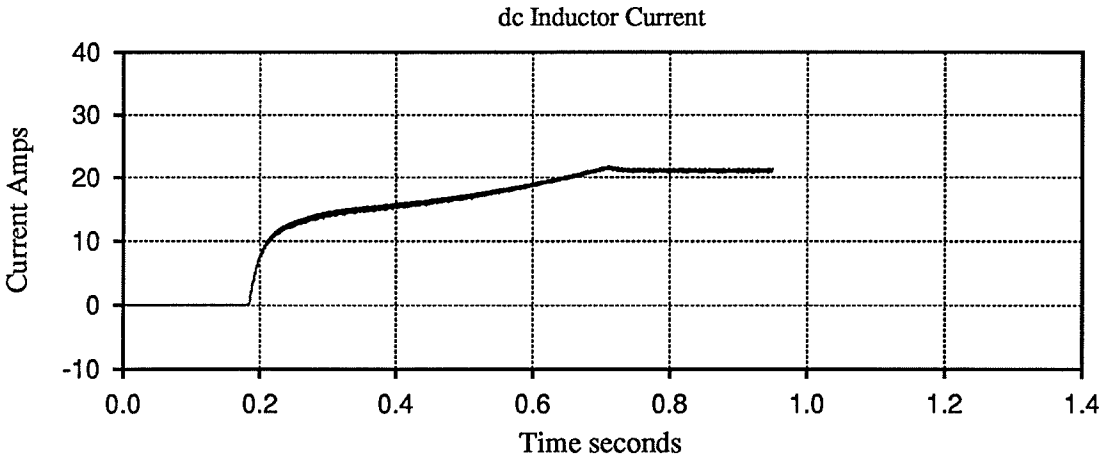


Figure 97. Test 3 – Simulation Result for Start–up Under Load at 1.0 p.u. Speed

age V_I to desired steady levels during operation in specified ranges of both machine speed and load power.

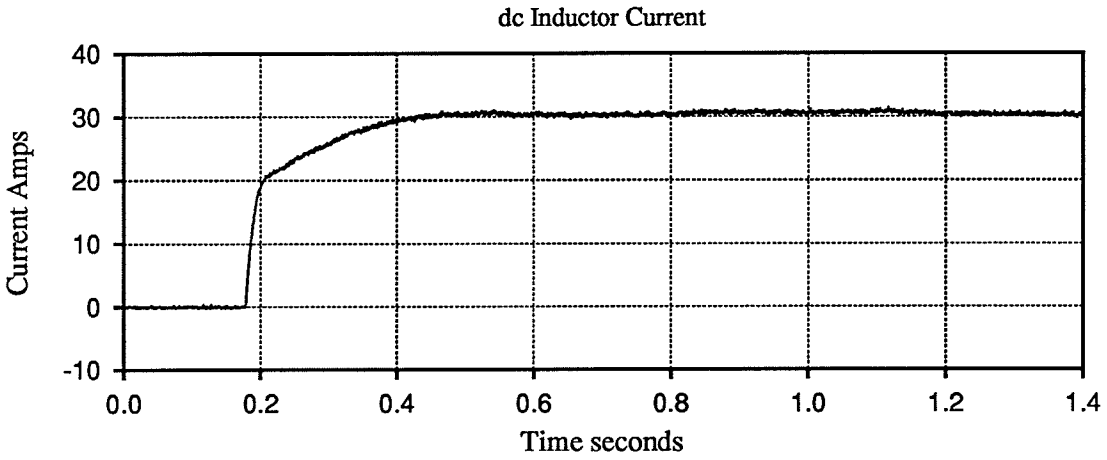


Figure 98. Test 4 – Laboratory Result for Start–up Under Load at 1.38 p.u. Speed

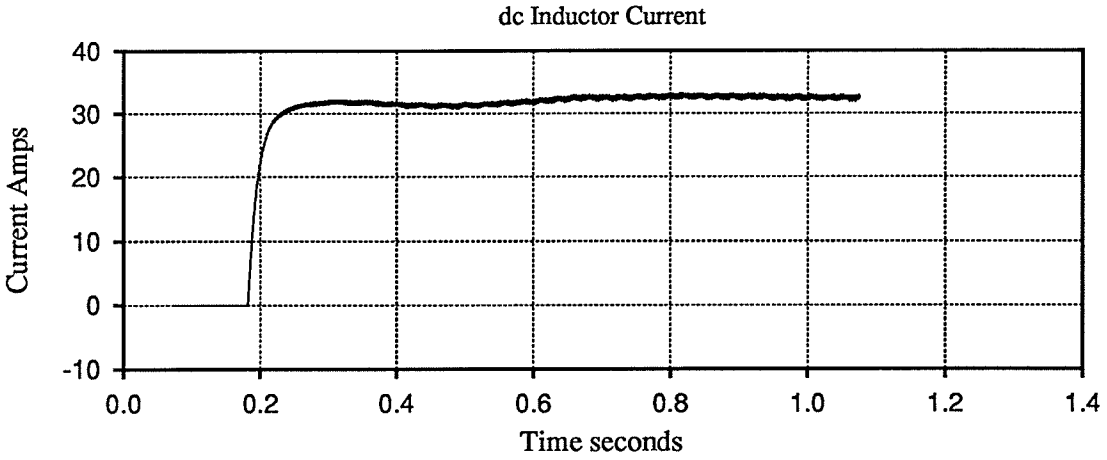


Figure 99. Test 4 – Simulation Result for Start–up Under Load at 1.38 p.u. Speed

6.3 Demonstration of Application of Load during Steady Running

6.3.1 Test 5 – Applying 0.95 p.u. Load at 1.0 p.u. Speed

Test 5 shows the response of the system to application of 0.95 p.u. dc load in one step while the apparatus is running at 1.0 p.u. machine speed with machine voltage steady at 1.0 p.u. voltage. Figure 100 shows plots of laboratory responses for I_d, machine voltage, and output voltage V_I. Figure 101 shows corresponding plots for simulated responses. The load is applied slightly after 0.4 seconds in the plots. The agreement between simulated responses and actual responses is quite good for operation at 1.0 p.u. speed.

6.3.2 Test 6 – Applying 0.95 p.u. Load at 1.38 p.u. Speed

Test 6 shows the responses of the system to application of 0.95 p.u. dc load in one step while the apparatus is running at 1.38 p.u. machine speed with the machine voltage steady at 1.0 p.u. voltage. Figure 102 shows plots of laboratory responses for I_d, machine voltage, and output voltage V_I. Figure 103 shows corresponding plots for simulated responses. The load is applied slightly after 0.4 seconds in the plots. The agreement between simulated responses and actual responses is again quite good at 1.38 p.u. speed.

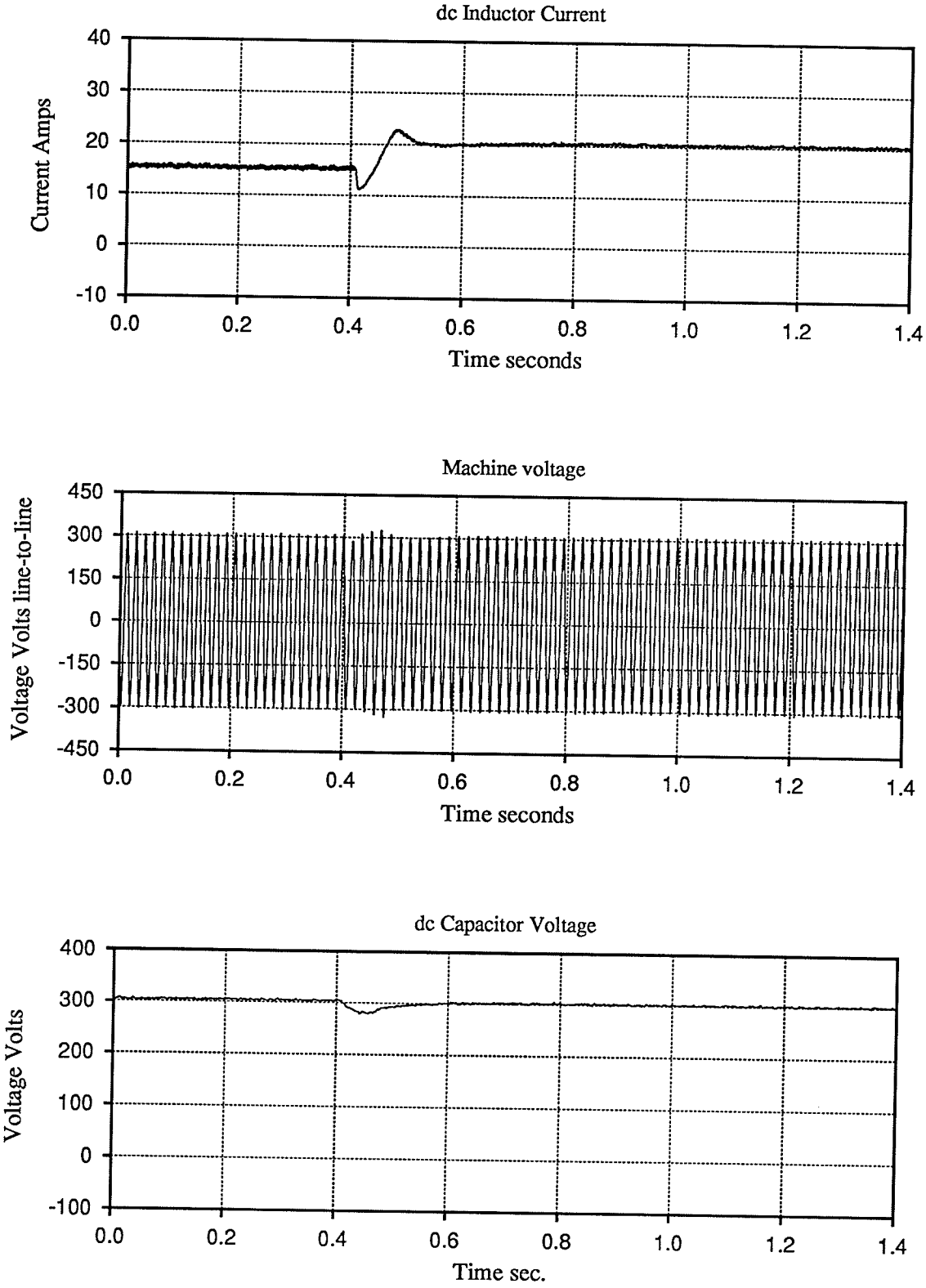


Figure 100. Test 5 – Laboratory Result for Applying 0.95 p.u. Load at 1.0 p.u. Speed

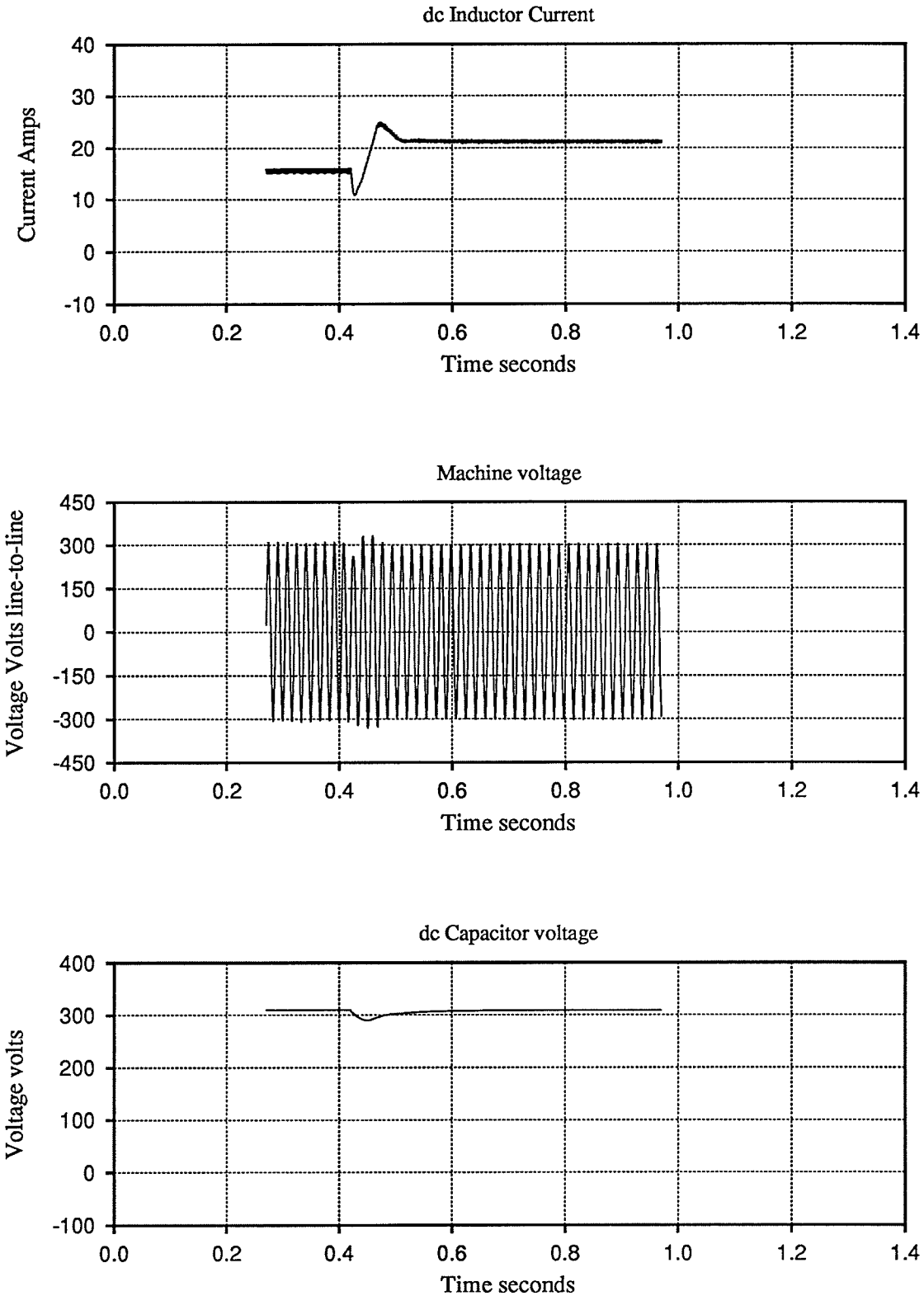


Figure 101. Test 5 – Simulation Result for Applying 0.95 p.u. Load at 1.0 p.u. Speed

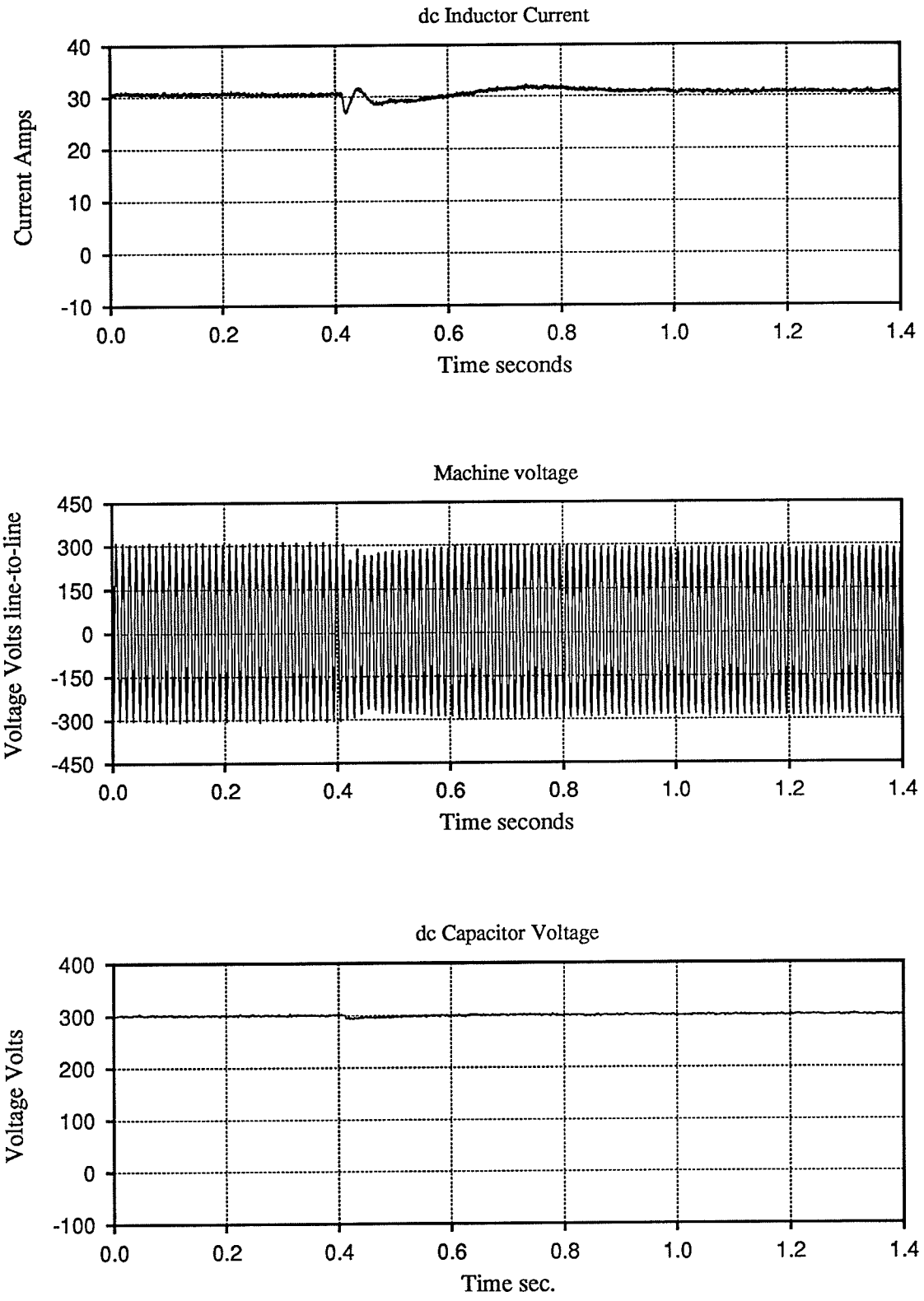


Figure 102. Test 6 – Laboratory Result for Applying 0.95 p.u. Load at 1.38 p.u. Speed

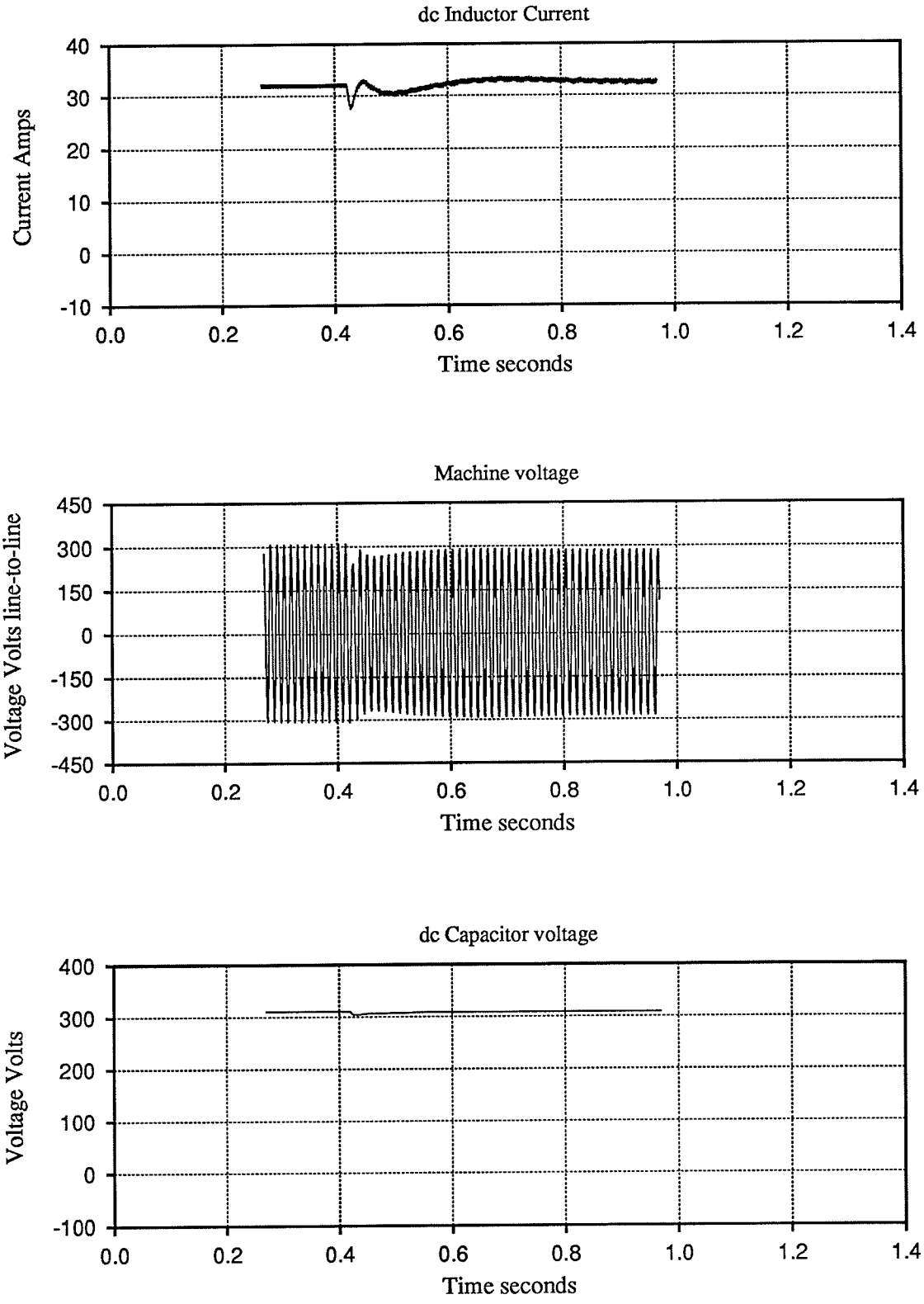


Figure 103. Test 6 – Simulation Result for Applying 0.95 p.u. Load at 1.38 p.u. Speed

6.4 Illustrations of Waveshapes During Steady Running

The results of Tests 7 through 10 provide waveshapes of system quantities during steady–running at 1.0 and 1.38 p.u. speeds with loads of 0.0 and 0.95 p.u. load at each speed.

6.4.1 Test 7 – Steady Running with 0.95 p.u. Load at 1.0 p.u. Speed

Plots from Test 7 show steady–running operation at 1.0 p.u. machine speed with 0.95 p.u. load. Figure 104 illustrates waveshapes of I_d; machine voltage; A–phase machine current; A–phase excitation capacitor current and A–phase rectifier current obtained from laboratory testing. The reference directions for the phase currents are into the machine, capacitor, and rectifier. Figure 105 illustrates the corresponding waveshapes obtained from simulation. In Test 7 there is excellent agreement between the actual machine voltage waveshape (Figure 104) and the simulated machine voltage waveshape (Figure 105). The ripple on the dc inductor current compares well in the simulated and actual plots of I_d. The Test 7 waveshapes of machine current and excitation capacitor current obtained in laboratory testing (Figure 104) agree in general shape with corresponding curves obtained from simulation (Figure 105). However, the waveshapes of machine current and capacitor current obtained in laboratory testing (Figure 104) include an additional component of low magnitude current ripple.

The current ripple noted above in the actual machine current and capacitor current (Figure 104) occurs in part due to the existence of snubber circuits in the actual rectifier apparatus. The snubber circuits were not represented in the simulated apparatus. The actual snubber circuit time constant is quite short and it was decided to omit the snubber circuit from the simulation rather than

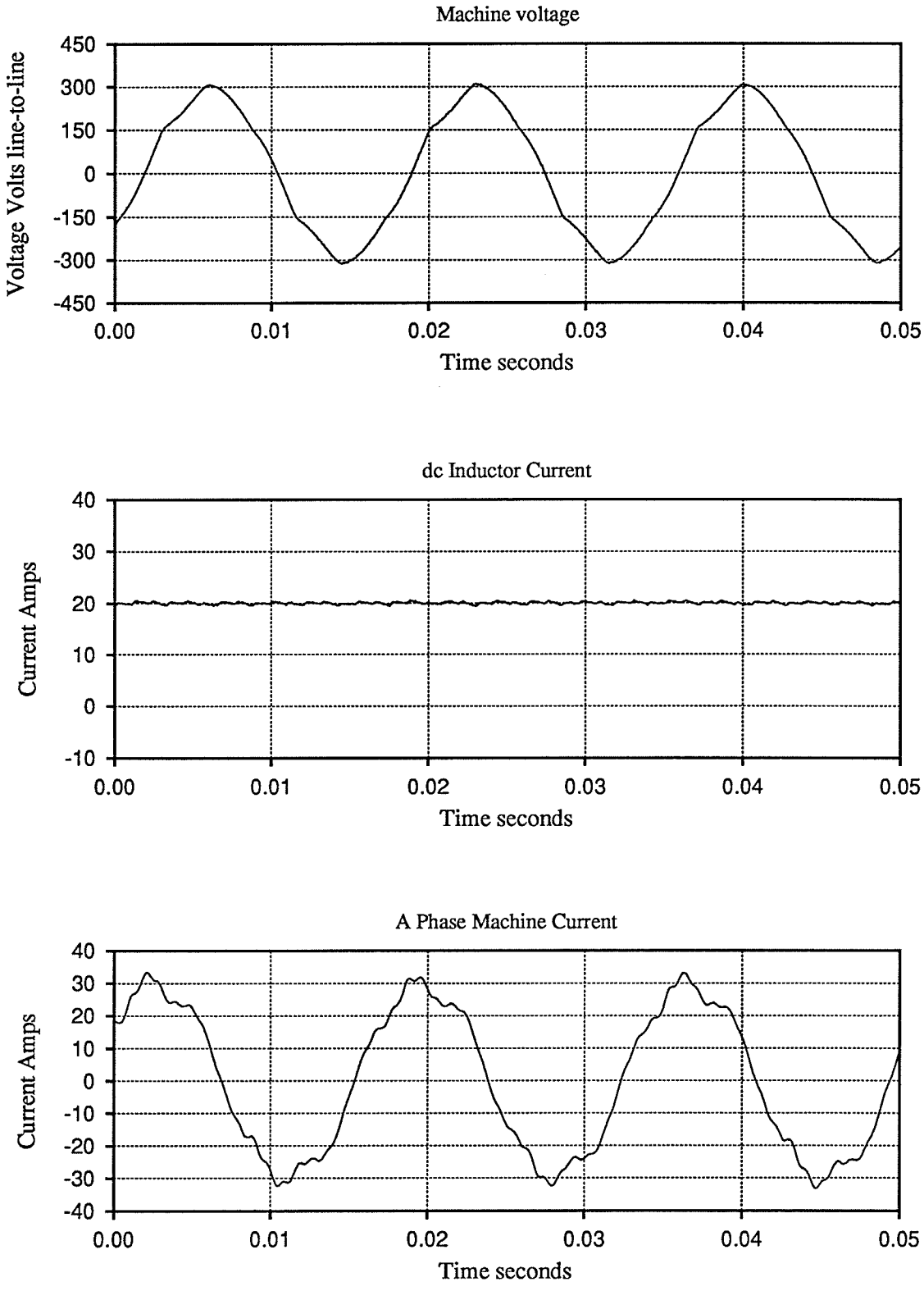


Figure 104. Test 7 – Waveshapes from Laboratory Testing during Steady–running at 1.0 p.u. Speed with 0.95 p.u. Load

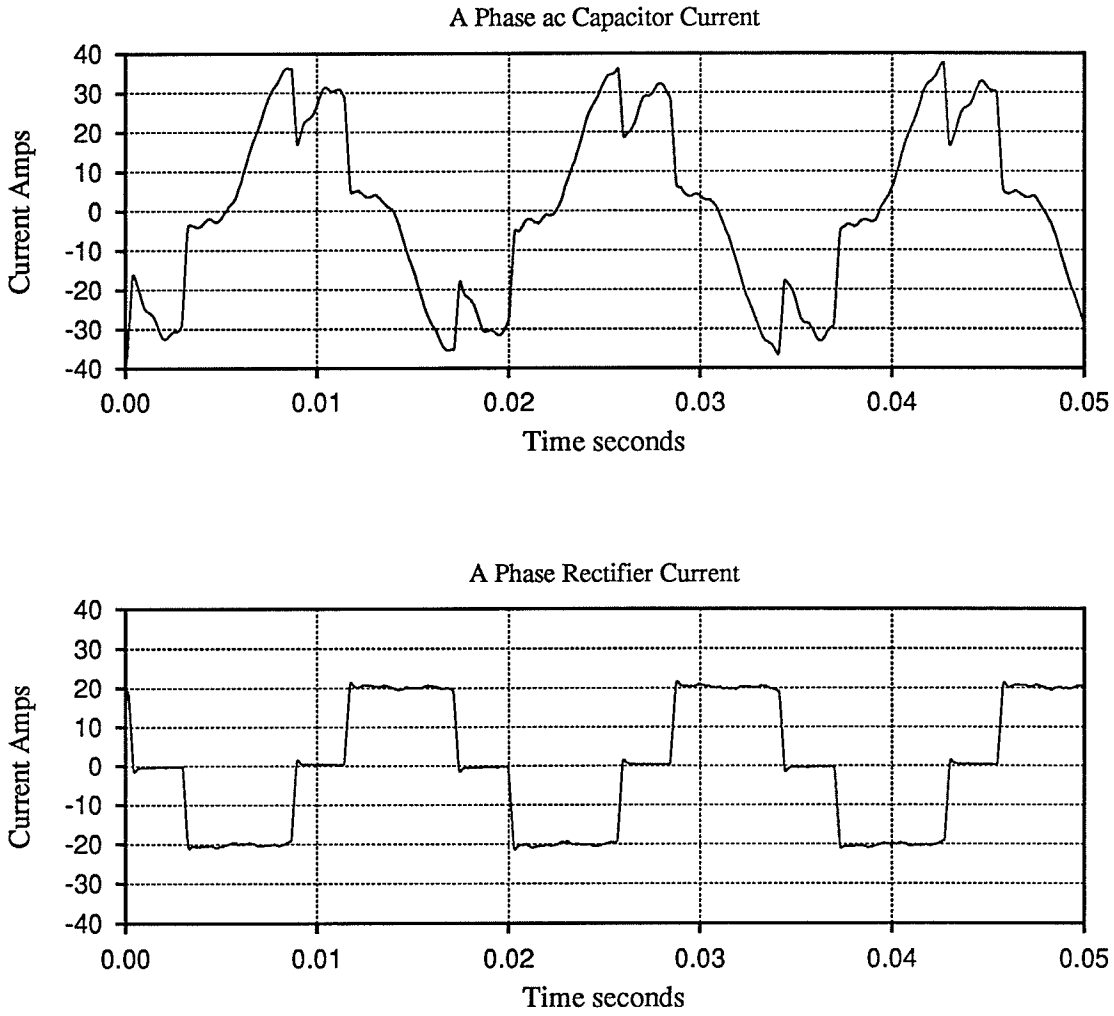


Figure 104. Test 7 – Waveshapes from Laboratory Testing during Steady–running at 1.0 p.u. Speed with 0.95 p.u. Load (continued)

represent it poorly. Therefore, the simulated turn–off of the A–phase rectifier current shown in Figure 105 is much closer to an ideal turn–off than is the actual turn–off of A–phase rectifier current illustrated in Figure 104. The simulation (Figure 105) does not account for reverse recovery current in the thyristors or reverse conduction in the snubber circuits during application of reverse voltage.

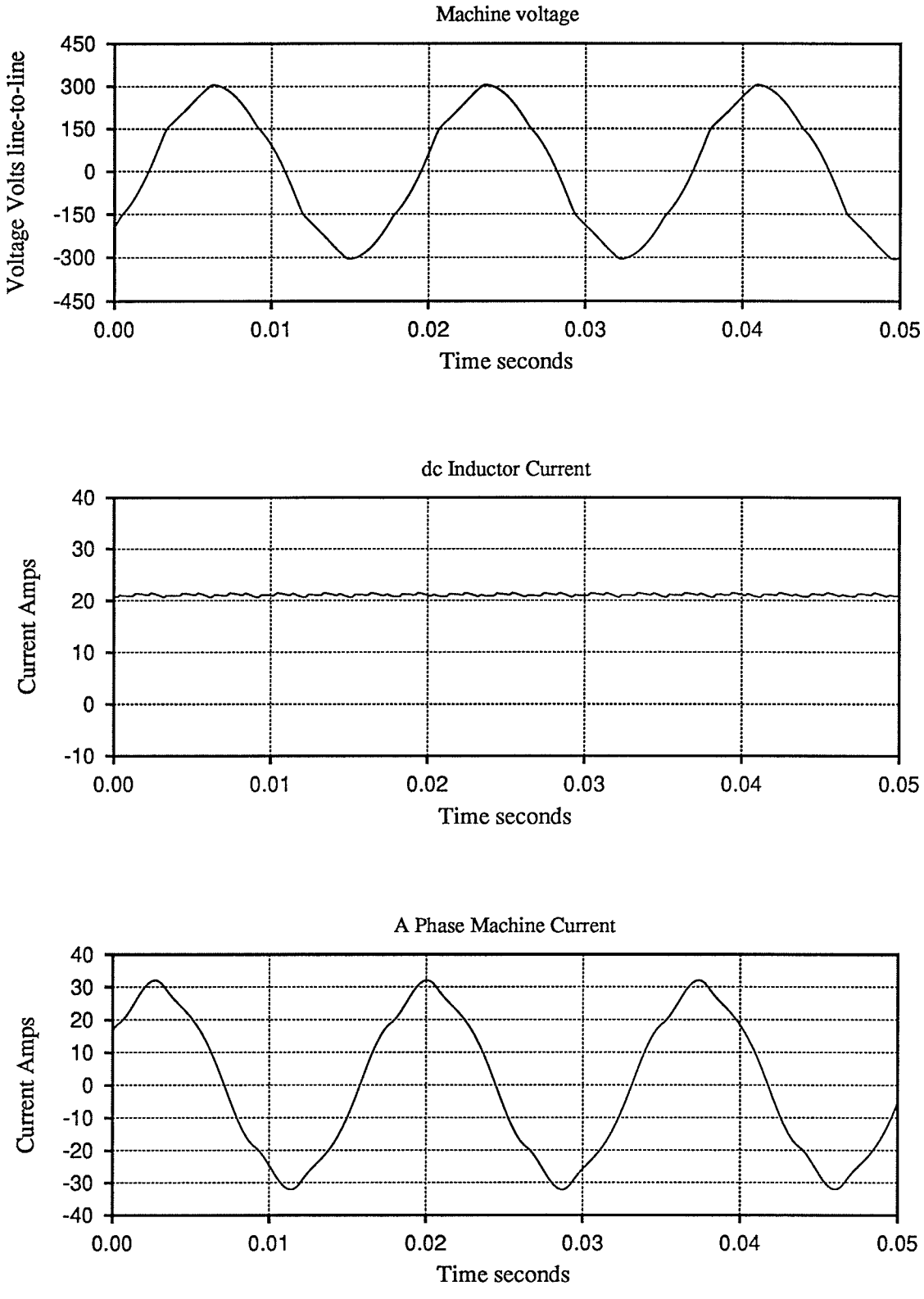


Figure 105. Test 7 – Waveshapes from Simulation of Steady–running at 1.0 p.u. Speed with 0.95 p.u. Load

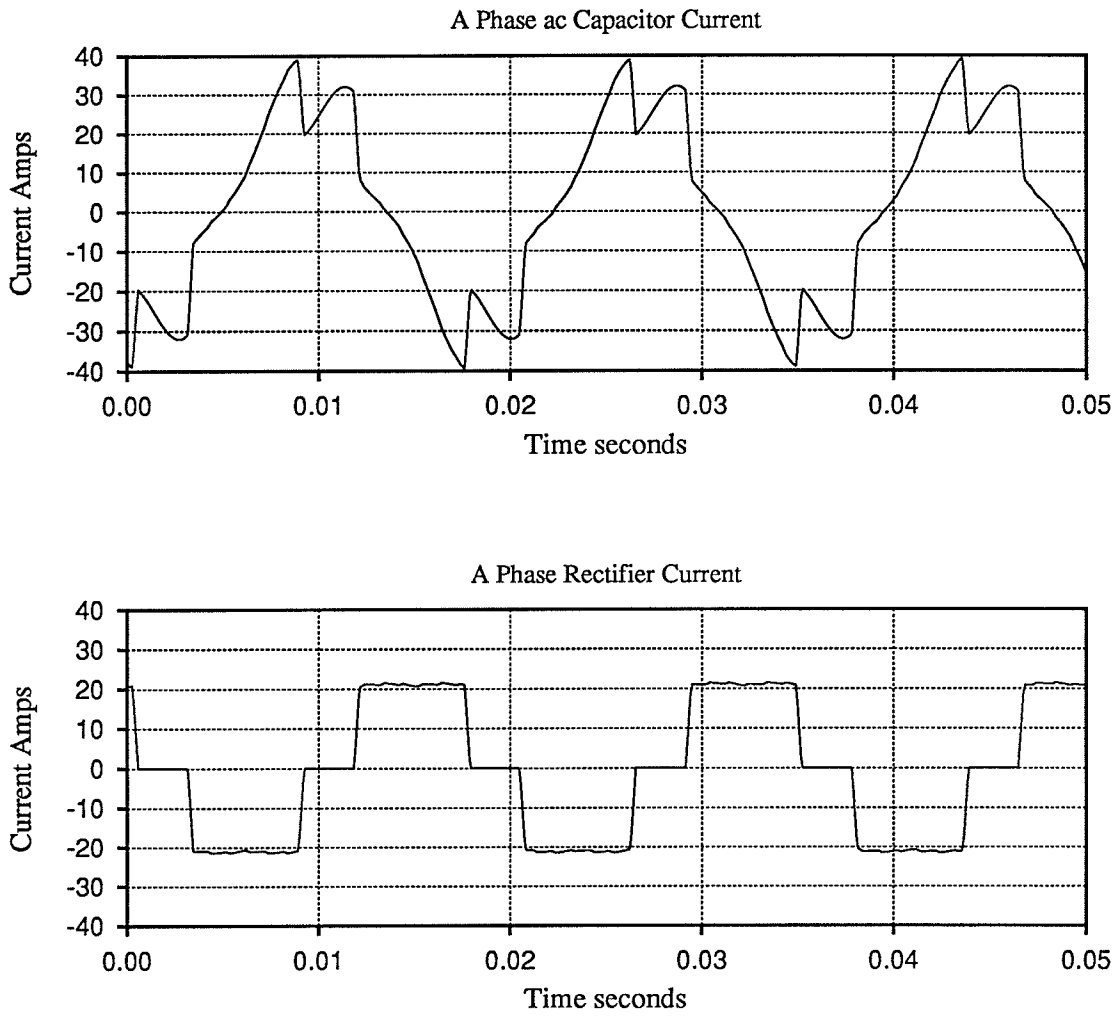


Figure 105. Test 7 – Waveshapes from Simulation of Steady–running at 1.0 p.u. Speed with 0.95 p.u. Load (continued)

Such reverse currents can be seen in the laboratory waveshape for A–phase rectifier current shown in Figure 104. The illustrated small spikes of reverse current can only come from the machine and the excitation capacitors. The spikes of reverse current in the rectifier current therefore must contribute to some de-

gree in producing the current ripple on the waveshapes of machine current and ac capacitor current shown in Figure 104.

6.4.2 Test 8 – Steady Running with No Load at 1.0 p.u. Speed

Plots from Test 8 show operation again at 1.0 p.u. machine speed but with no load. Figure 106 illustrates waveshapes of machine voltage and dc inductor current I_d obtained during laboratory testing. Figure 107 illustrates corresponding waveshapes obtained from simulation. As in Test 7 there is good agreement between the actual waveshapes of machine voltage and I_d (Figure 106) and the corresponding simulated waveshapes (Figure 107).

6.4.3 Test 9 – Steady Running with 0.95 p.u. Load at 1.38 p.u. Speed

Plots from Test 9 show machine voltage at 1.38 p.u. machine speed with 0.95 p.u. load. Figure 108 illustrates the waveshape of machine voltage obtained during laboratory testing. Figure 109 illustrates the corresponding waveshape of machine voltage obtained from simulation. There is excellent agreement between the actual and simulated waveshapes of machine voltage in this test.

6.4.4 Test 10 – Steady Running with No Load at 1.38 p.u. Speed

Plots from Test 10 show machine voltage again at 1.38 p.u. machine speed but with no load connected. Figure 110 illustrates the waveshape of machine voltage obtained during laboratory testing. Figure 111 illustrates the corresponding waveshape of machine voltage obtained from simulation. As in Test 9, there is good agreement between the actual and simulated waveshapes of machine voltage in this test.

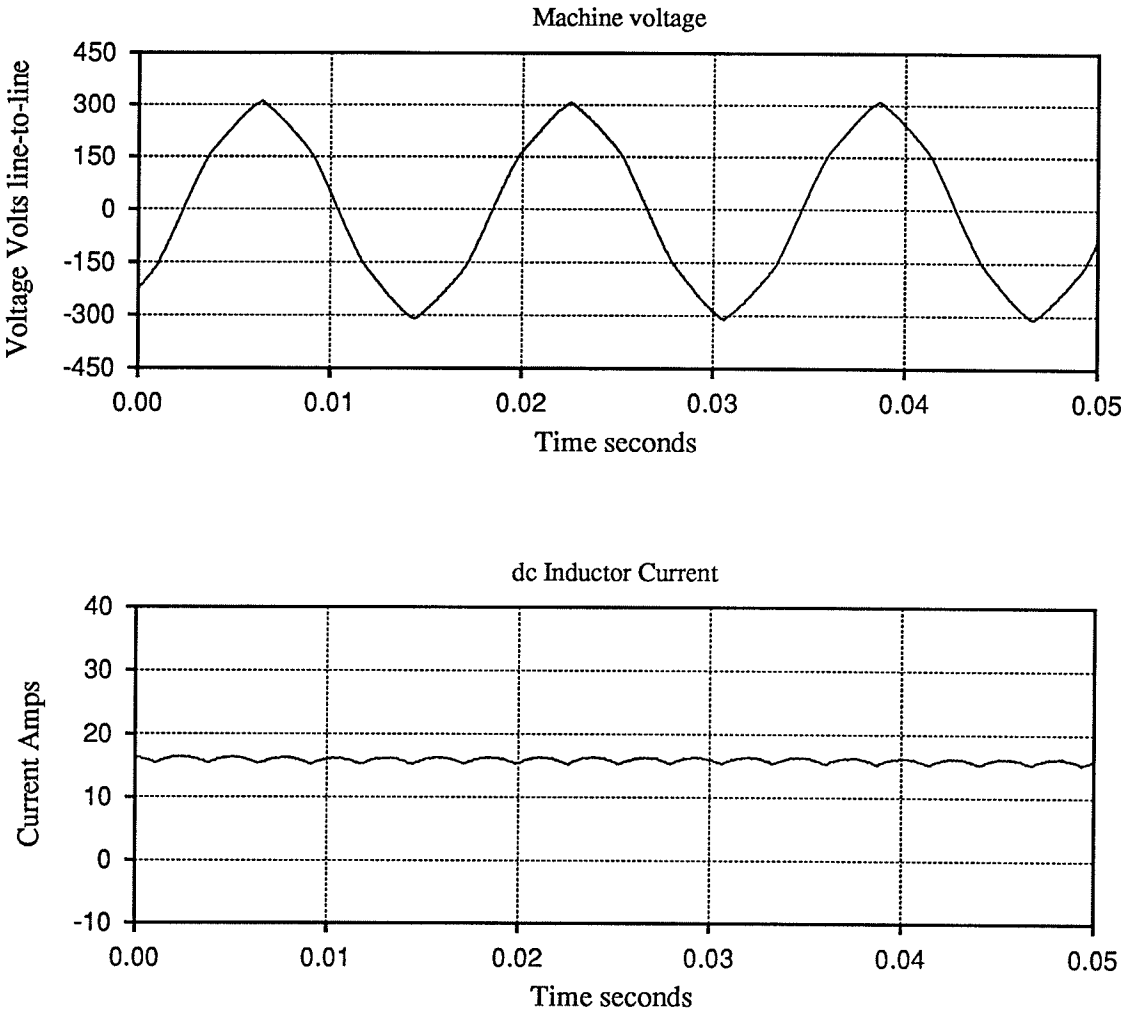


Figure 106. Test 8 – Waveshapes from Laboratory Testing during Steady–running at 1.0 p.u. Speed with No Load

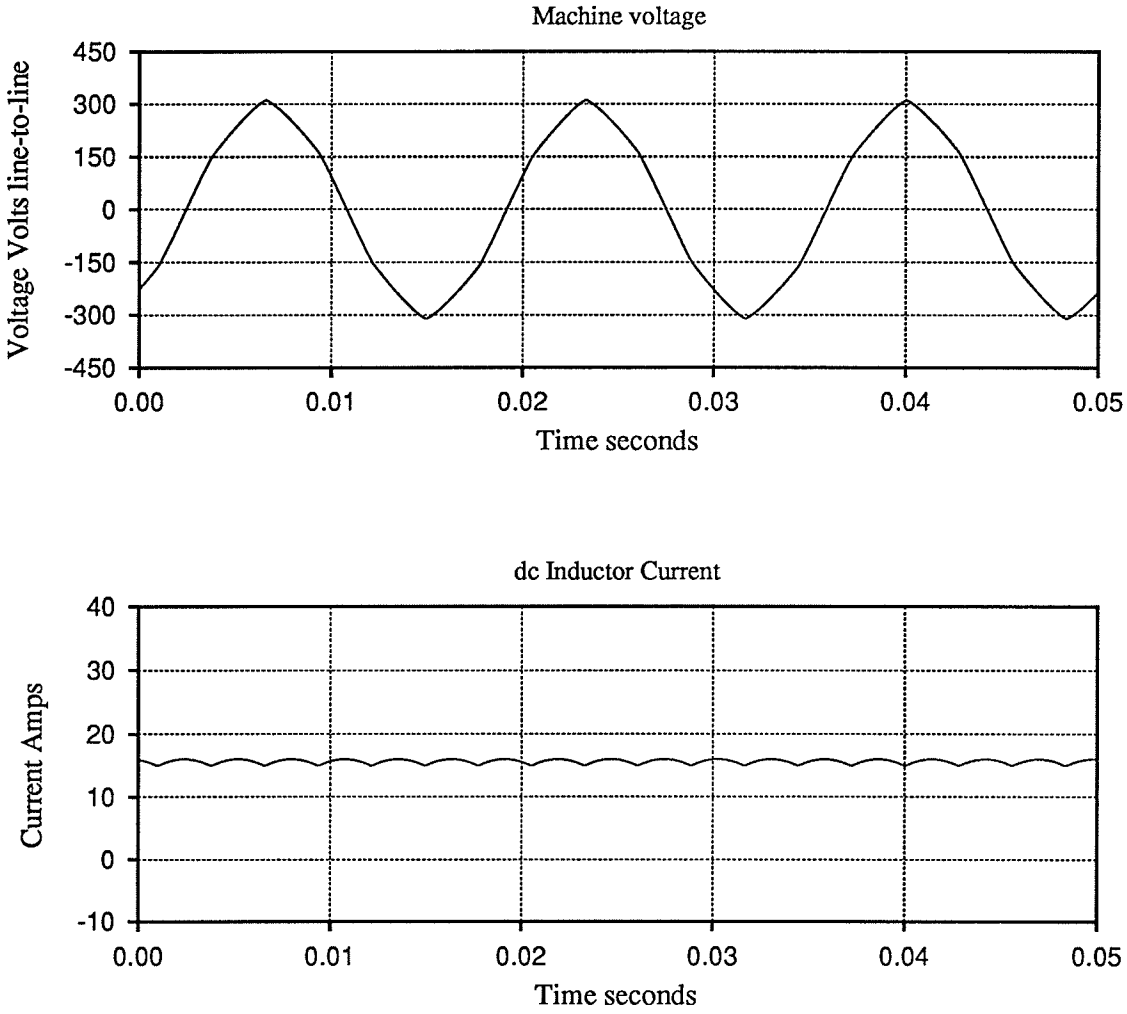


Figure 107. Test 8 – Waveshapes from Simulation of Steady–running at 1.0 p.u. Speed with No Load

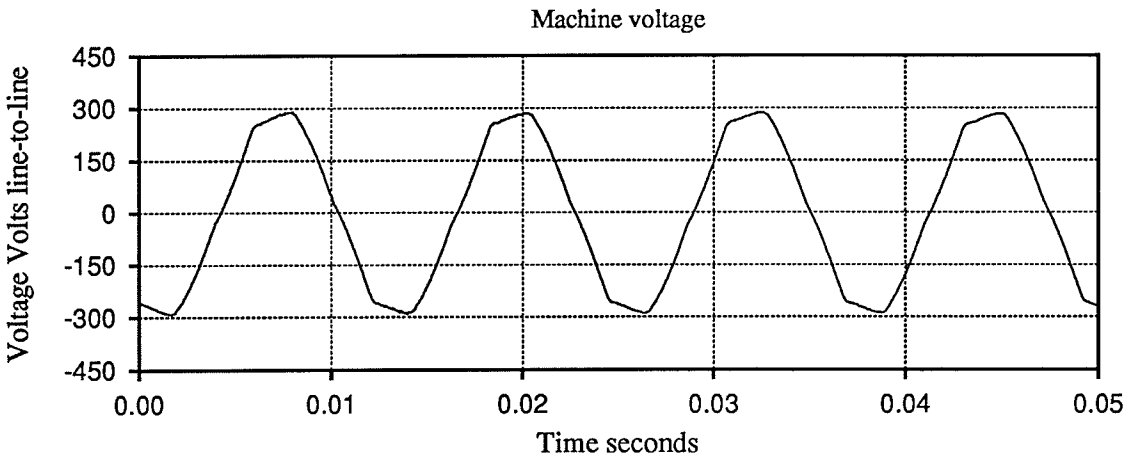


Figure 108. Test 9 – Machine Voltage Wave from Laboratory Testing during Steady–running at 1.38 p.u. Speed with 0.95 p.u. Load

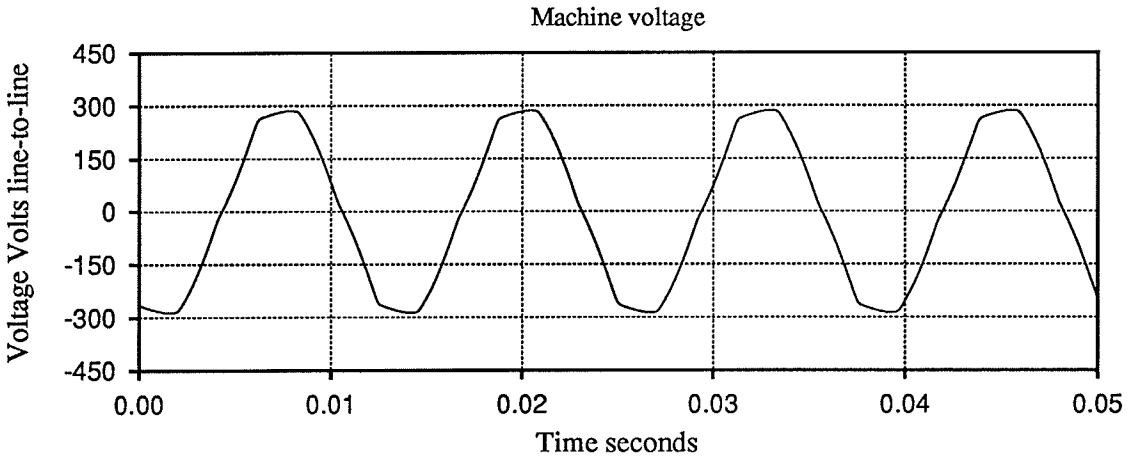


Figure 109. Test 9 – Simulated Machine Voltage Wave for Steady–running at 1.38 p.u. Speed with 0.95 p.u. Load

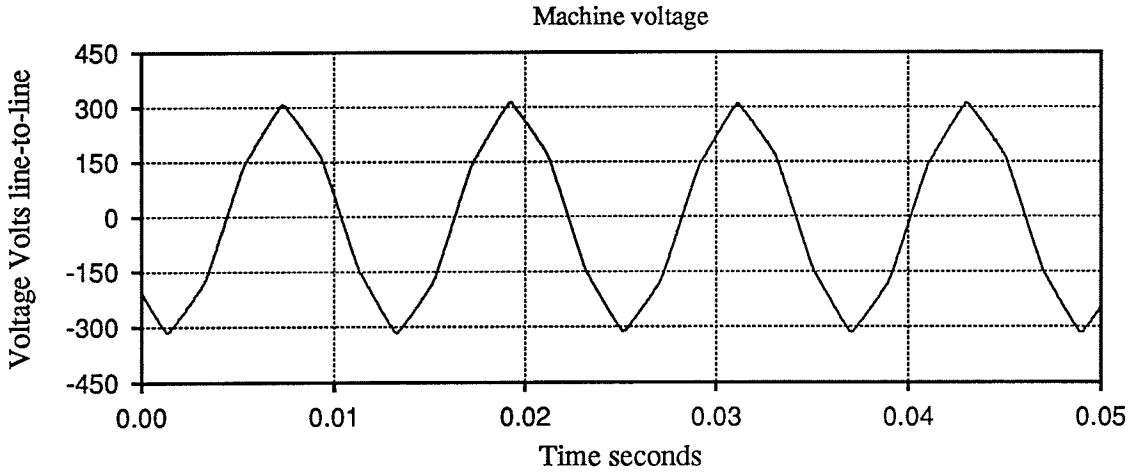


Figure 110. Test 10 – Machine Voltage Wave from Laboratory Testing during Steady–running at 1.38 p.u. Speed with No Load

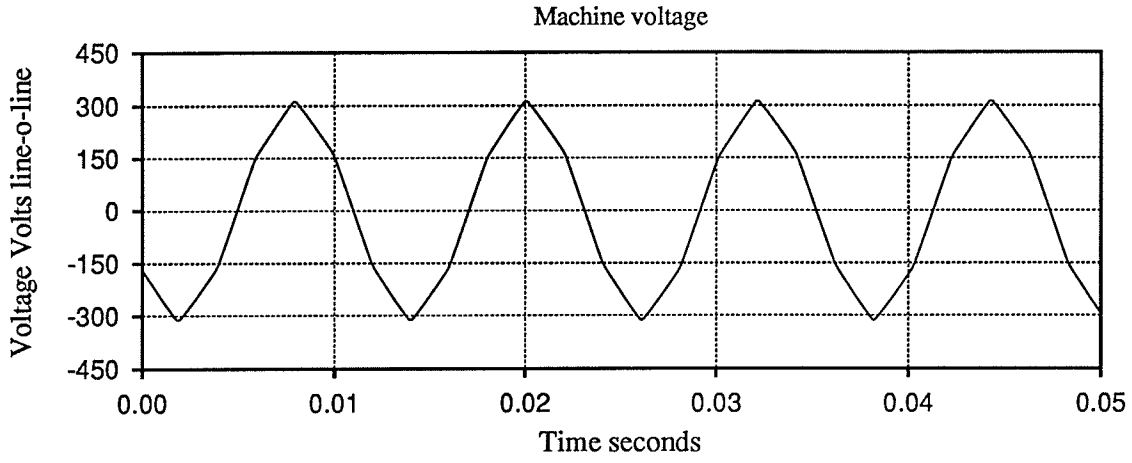


Figure 111. Test 10 – Simulated Machine Voltage Wave for Steady–running at 1.38 p.u. Speed with No Load

6.5 Demonstration of Load Rejection Performance

6.5.1 Test 11 – Load Rejection of 0.95 p.u. Load at 1.0 p.u. Speed

Plots from Test 11 show load rejection of 0.95 p.u. load during steady–running at 1.0 p.u. machine speed. Figure 112 illustrates plots of I_d and machine voltage obtained during laboratory testing. Figure 113 illustrates corresponding plots obtained from simulation. Both the simulated and actual results show that the control system controls I_d well during a load rejection of 0.95 p.u. load at 1.0 p.u. speed.

A valid comparison of the simulated and actual transient responses at the instant of load rejection is not possible because the load current does not drop to zero instantly in the laboratory apparatus when the load switch is opened. Arcing of the actual load switch can extend the reduction in dc load current over a period of about 0.03 seconds as illustrated in the plot of dc load current shown in Figure 118. The simulation does not model the arcing that occurs in the actual apparatus. Therefore the load current can drop abruptly in the simulation when the load switch opens as shown in the plot of load current shown in Figure 119. The arcing of the load switch in the laboratory apparatus must cause minor differences in the dynamics of the simulated and actual load rejections.

6.5.2 Test 12 – Load Rejection of 0.95 p.u. Load at 1.38 p.u. Speed

Plots from Test 12 show load rejection of 0.95 p.u. load during steady–running at 1.38 p.u. machine speed. Figure 114 illustrates plots of dc current I_d and machine voltage obtained during laboratory testing. Figure 115 illustrates corresponding plots obtained from simulation. Both the simulated and actual results show that the control system controls dc current well during a load rejection at 1.38 p.u. speed.

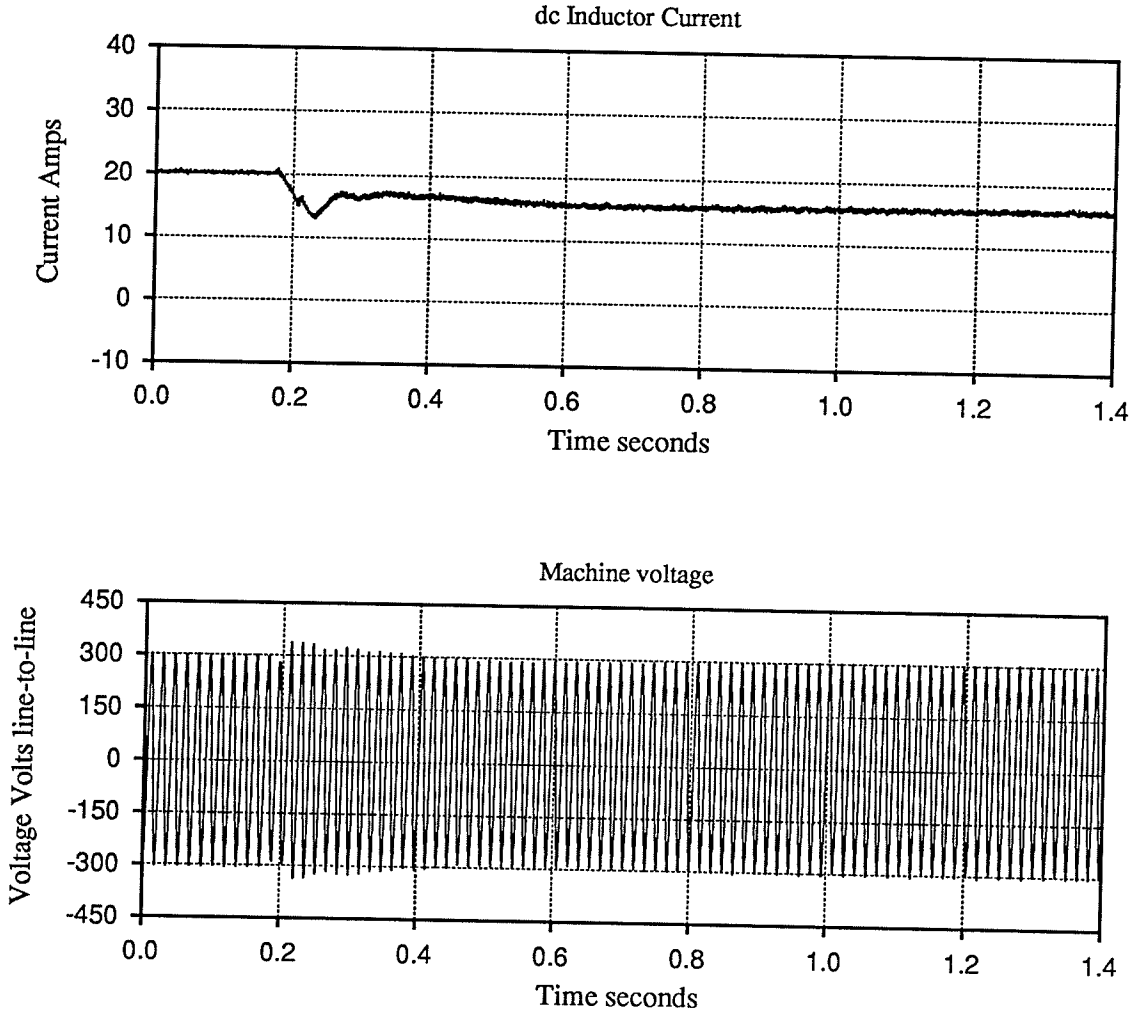


Figure 112. Test 11 – Laboratory Results for Load Rejection of 0.95 p.u. Load at 1.0 p.u. Machine Speed

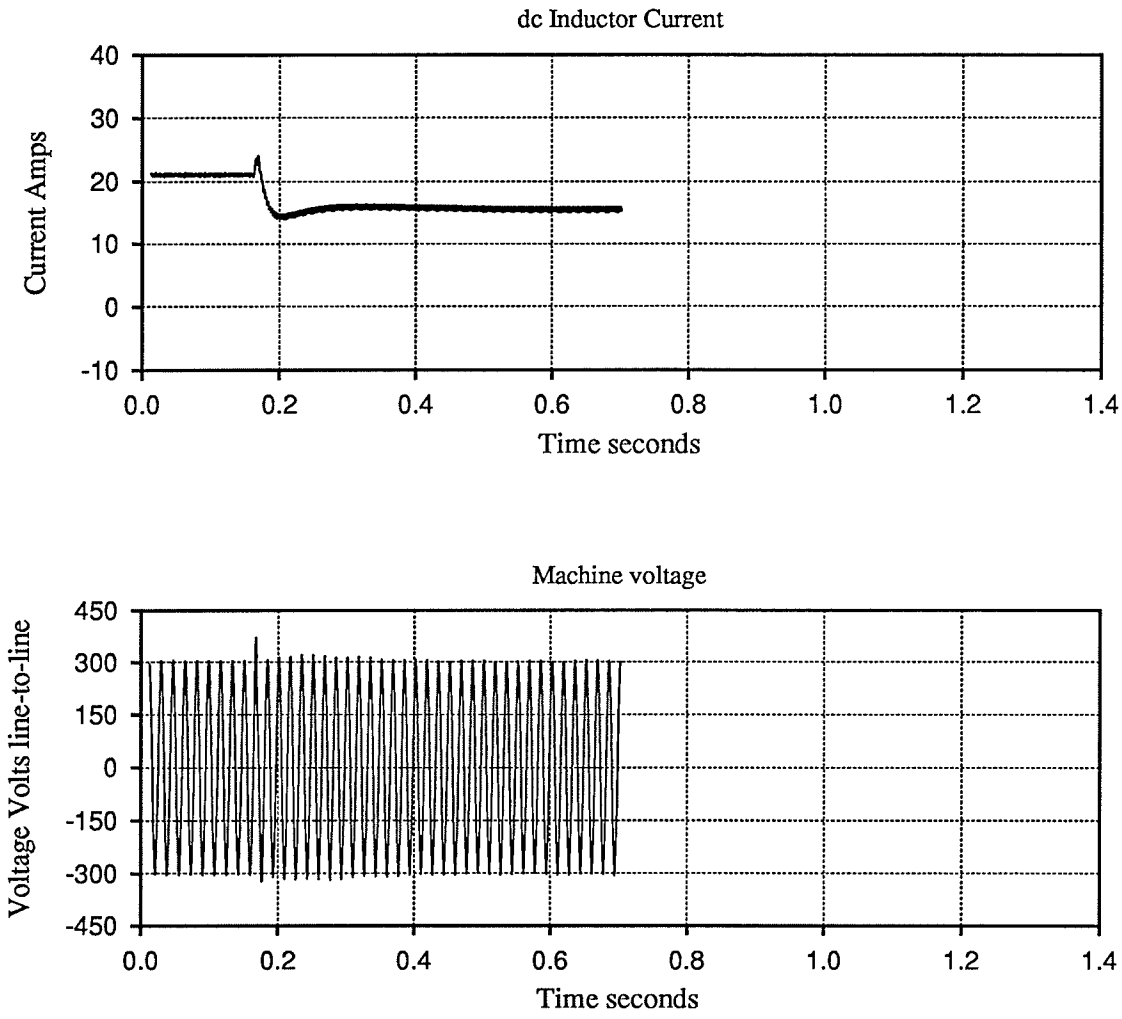


Figure 113. Test 11 – Simulation Results for Load Rejection of 0.95 p.u. Load at 1.0 p.u. Machine Speed

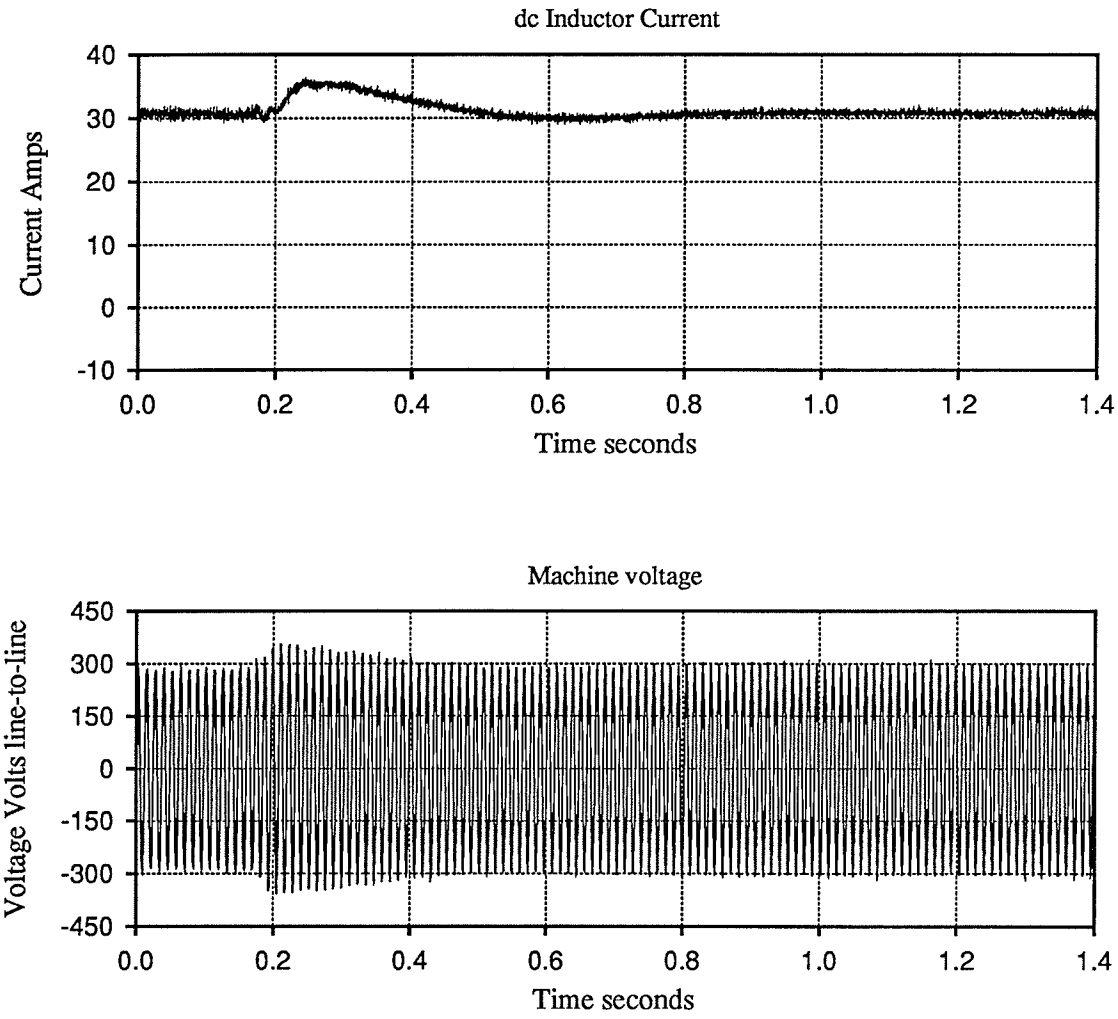


Figure 114. Test 12 – Laboratory Results for Load Rejection of 0.95 p.u. Load at 1.38 p.u. Machine Speed

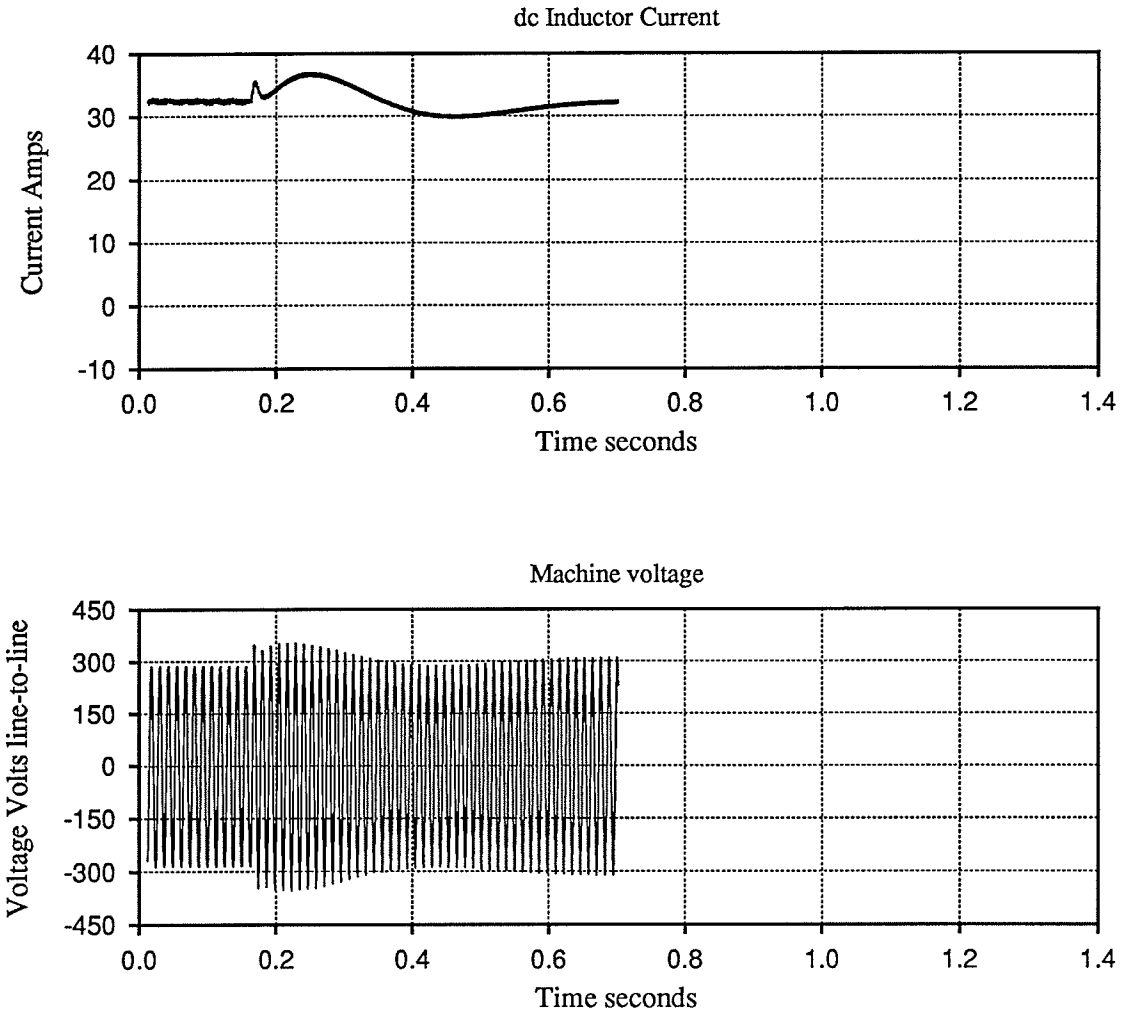


Figure 115. Test 12 – Simulation Results for Load Rejection of 0.95 p.u. Load at 1.38 p.u. Machine Speed

6.6 Demonstration of Application and Removal of Overload

6.6.1 Test 13 – Application of Overload

Plots from Test 13 show application of overload to the apparatus during steady–running at 1.2 p.u. machine speed. Two resistances were arranged for connection as dc load in the laboratory apparatus. The two resistances were respectively load boxes set for 1.08 p.u. resistance and 1.29 p.u. resistance. The 1.08 p.u. resistance was connected as load prior to the application of the overload. The apparatus was therefore operating at about 0.93 p.u. power before the second resistance was connected in parallel to provide the overload. Figure 116 illustrates the responses obtained during laboratory testing when the dc load resistance was dropped to 0.59 p.u. resistance at about t = 0.2 seconds in the plots. Figure 117 illustrates the corresponding plots obtained from simulation. The plots agree very well.

Figure 116 illustrates plots of the dc capacitor voltage V_I, the dc load current I_L, and the machine voltage obtained during application of the overload in laboratory testing. The plot of V_I (which is the load voltage) and the plot of I_L illustrated in Figure 116 show that the control protects the apparatus to some extent when an overload is applied. In particular, the control system causes the dc output voltage V_I to drop when the overload is applied as illustrated in Figure 116. The machine voltage sees no disturbance during the application of the overload as illustrated also in Figure 116. The capacity for self–protection exists because the Look–up Tables do not accept a power order larger than 1.0 p.u. power as discussed in chapter four. The power actually supplied to the load resistance of 0.59 p.u. resistance during the attempted overload is limited to about 0.97 p.u. power.

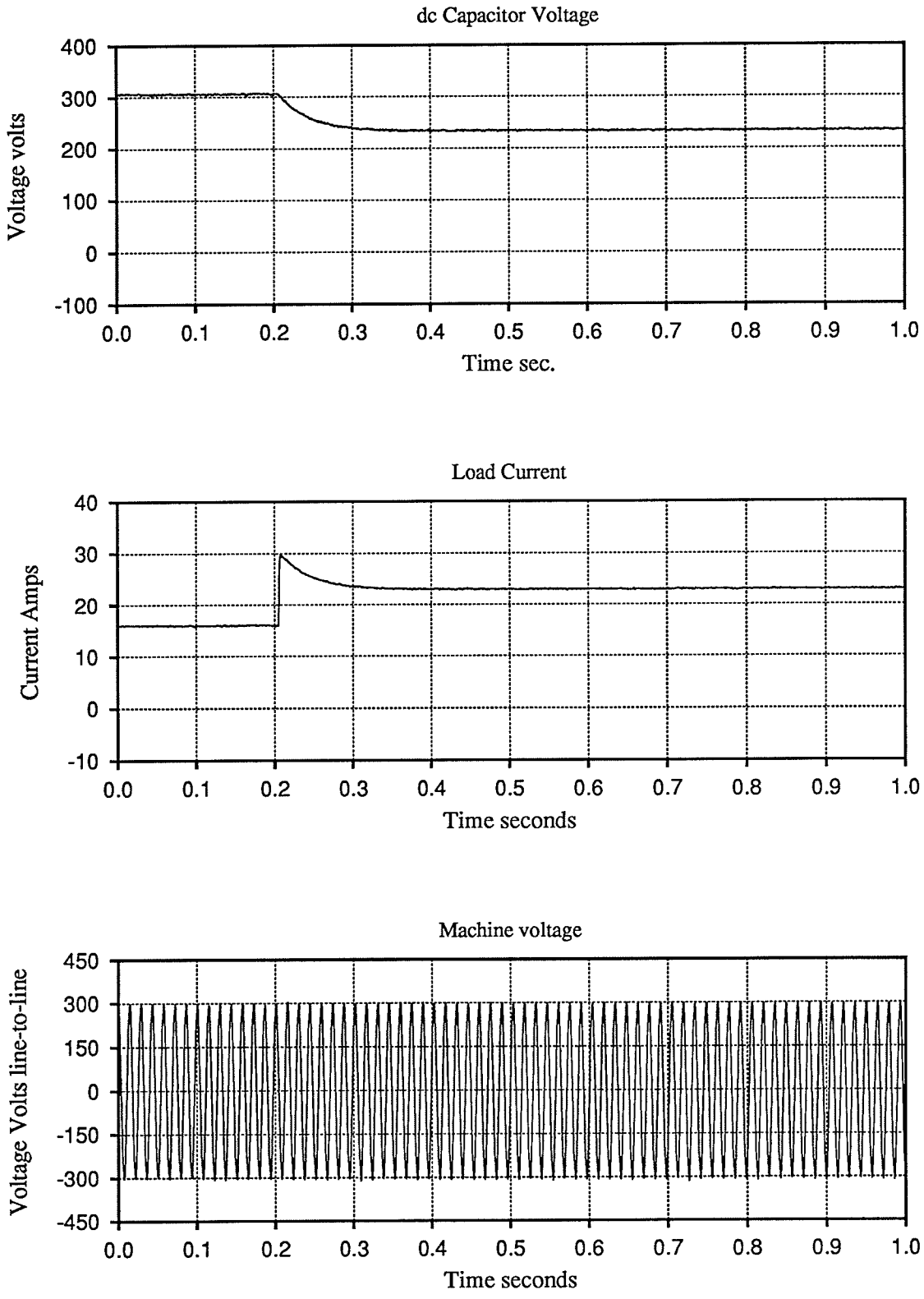


Figure 116. Test 13 – Laboratory Results for Application of Overload at 1.2 p.u. Speed

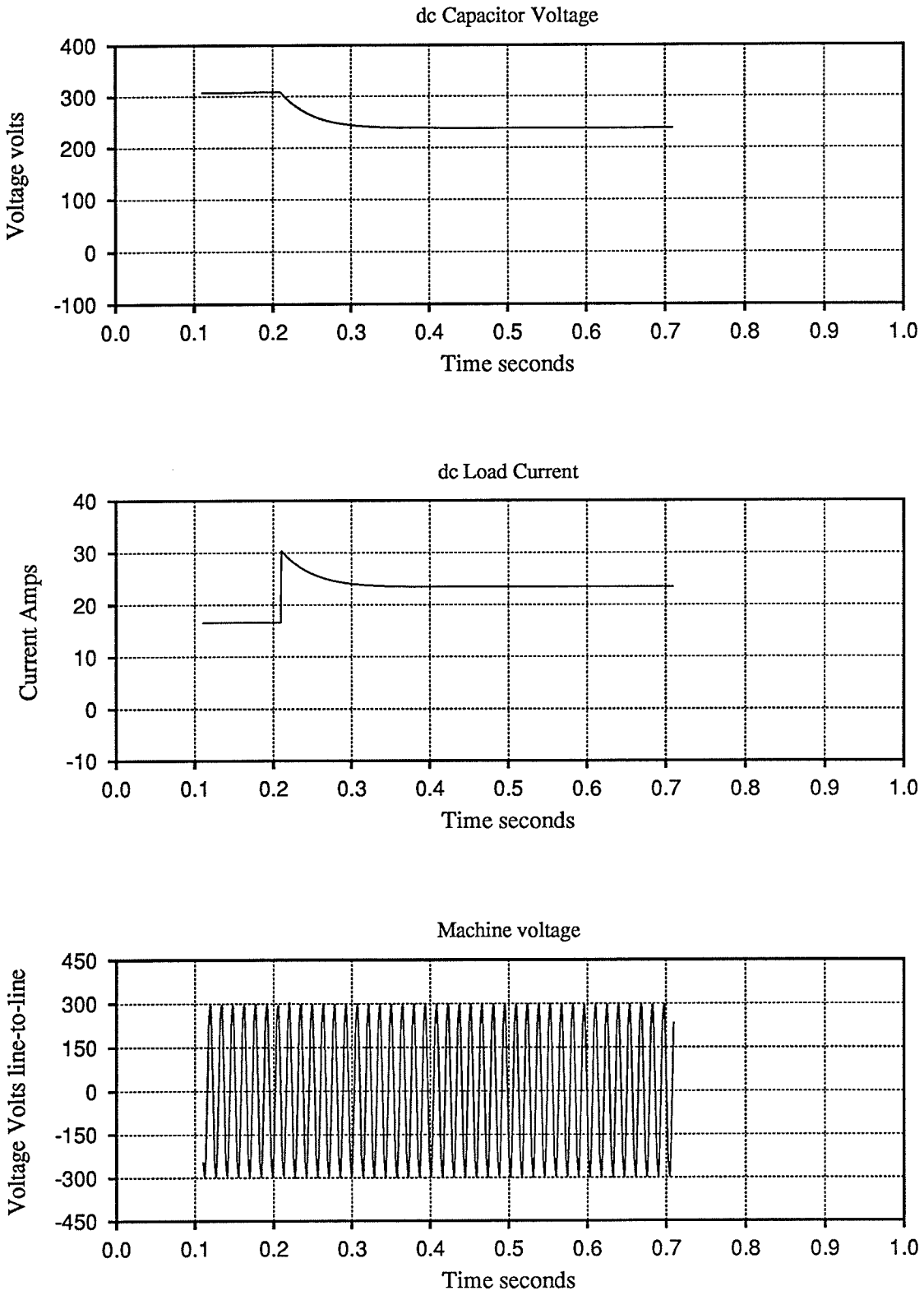


Figure 117. Test 13 – Simulation Results for Application of Overload at 1.2 p.u. Speed

6.6.2 Test 14 – Recovery from Overload

Plots from Test 14 show removal of the overload on the apparatus at 1.2 p.u. speed which was applied in Test 13. Figure 118 illustrates plots of the dc capacitor voltage V_I, the dc load current I_L, and the machine voltage obtained during removal of the overload in laboratory testing. Figure 119 illustrates corresponding plots obtained from simulation. The switch connecting the 1.08 p.u. load resistance is opened to remove the overload at about t = 0.2 seconds in the plots.

When the overload is removed the control system promptly restores the dc output voltage (dc capacitor voltage) to the desired level of about 310 Volts as illustrated in Figure 118. The plot of the actual dc load current in Figure 118 illustrates the effect of arcing which occurs when the knife switch is opened to disconnect the 1.08 p.u. resistance load bank. The dc current in the arc drops to zero over a period of about 0.03 seconds. The simulated result illustrated in Figure 119 does not include modelling of the arc and thus the load current drops immediately when the load switch is opened in the simulation.

6.7 Conclusions from Laboratory Testing

There are several conclusions that can be drawn from the laboratory testing of the apparatus.

The control system and power apparatus built in the laboratory performs generally as predicted by simulation. In fact, simulation made possible the development of the control strategy to the point where laboratory testing could begin.

The control system can start the apparatus with or without full load connected at any speed between the minimum and maximum design speeds of 1.0 and 1.4 p.u. speed.

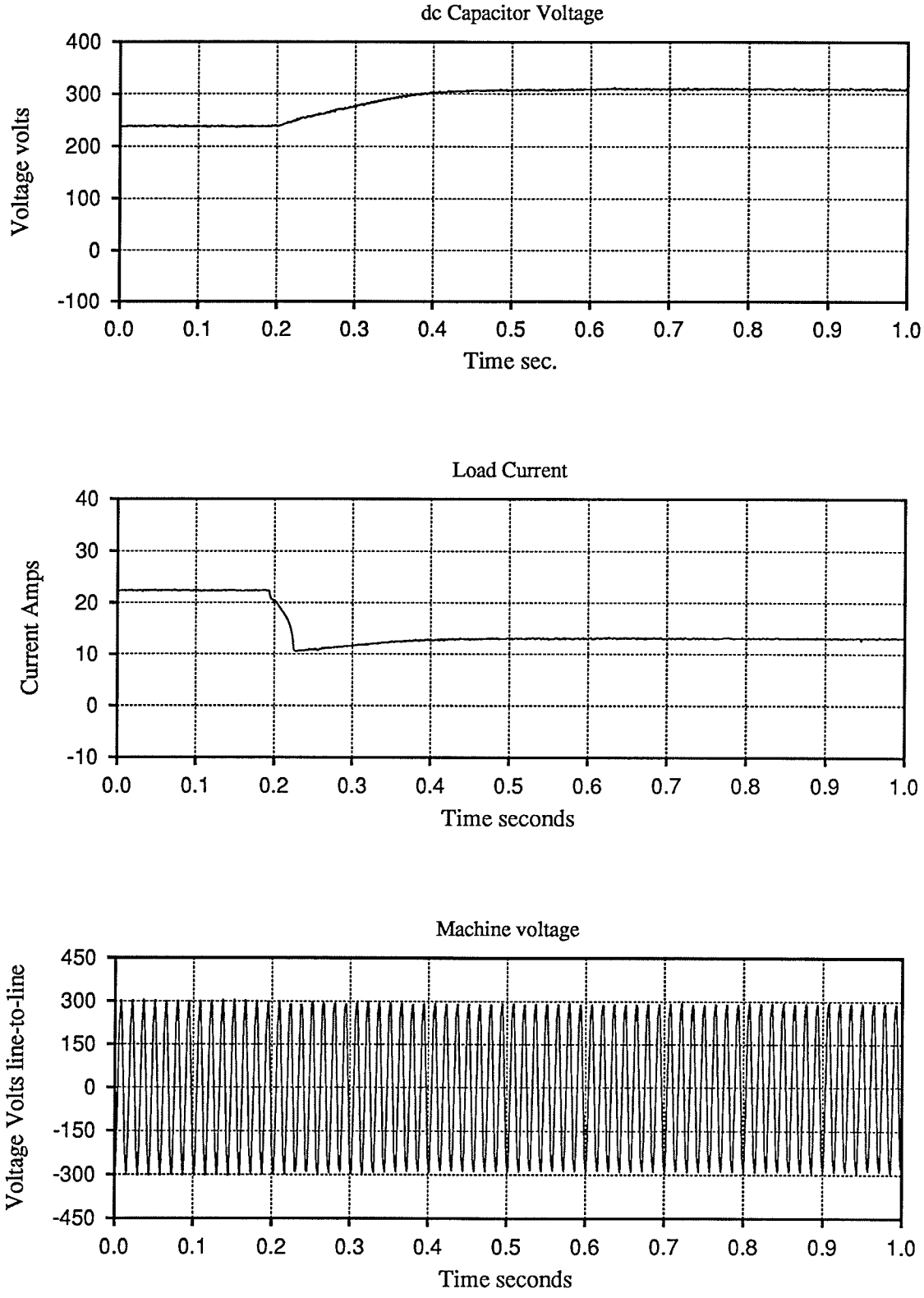


Figure 118. Test 14 – Laboratory Results showing Recovery from Overload at 1.2 p.u. Speed

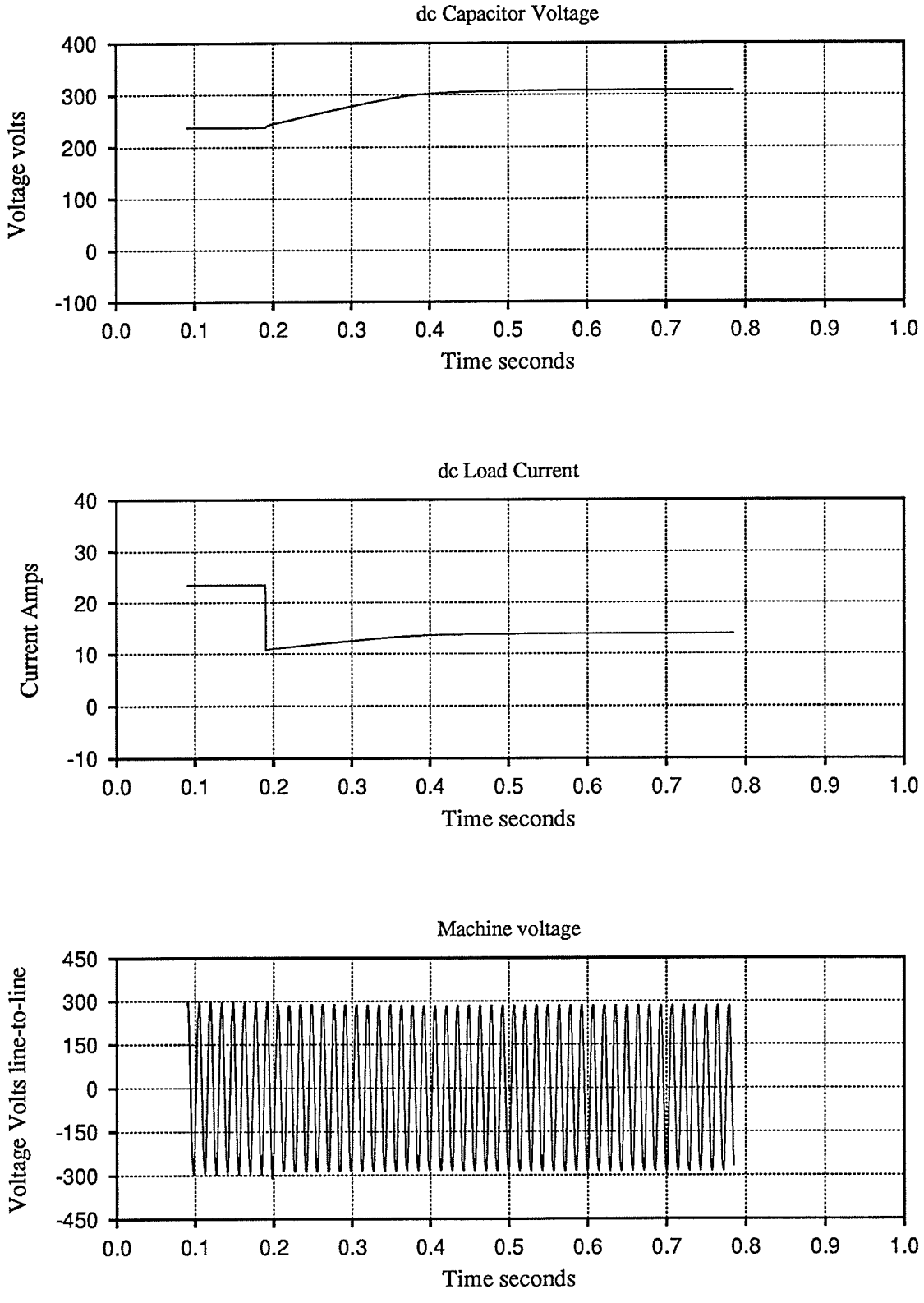


Figure 119. Test 14 – Simulation Results showing Recovery from Overload at 1.2 p.u. Speed

Full load can be applied or removed in one step in the specified range of machine speed.

It is necessary to model the rectifier snubber circuits in the simulations in order to see the ripple on the machine and self–excitation capacitor currents which is caused by the snubbers.

The apparatus output voltage will "brown out" to prevent overloading the apparatus in circumstances where the load resistance drops too low.

The laboratory testing in Test 2 demonstrates that the PI controller in the Rectifier Current Controller is necessary to overcome the minor error in the Look–up Tables. The contents of the Look–up Tables could be improved by updating the tables based on measured values of actual I_d obtained during operation of the actual apparatus at various combinations of speed and power order. A method therefore exists for improving the Look–up Tables. However, the effect of inaccuracy in the Look–up Tables on the response of the apparatus is mainly confined to the period during starting of the apparatus at higher speeds (such as 1.38 p.u. speed). In addition, the actual apparatus was not overstressed during starting. Therefore, improvement of the Look–up Tables is only of peripheral interest.

Chapter seven provides overall conclusions based on the thesis work.

Chapter Seven

Conclusions and Contributions

This thesis describes the development of a novel apparatus for supplying an isolated ac load from a self–excited induction generator operable at variable speed. The ac voltage supplied to the load is well regulated in frequency and magnitude.

7.1 Conclusions from Chapter 1 – Introduction

A novel configuration of apparatus is specified. The selected power apparatus consists of a self–excited induction machine supplying an isolated ac load through an asynchronous dc link. In the dc link, a voltage–boost converter interfaces the variable dc output voltage from a controlled Graetz bridge rectifier to the relatively fixed dc input voltage of a voltage–sourced inverter. The asynchronous nature of the dc link permits the induction machine to be operated at variable speed.

7.2 Conclusions from Chapter 2 – Steady State Characterization of the Apparatus

A method is described for obtaining the entire steady state solution for the apparatus at a given machine voltage as a function of machine speed and load power. The method provides for the selection of the required self–excitation capacitance and also provides characteristic curves for use as a model in a feed–forward control system.

A simplified non–linear search procedure is described for obtaining the stator current and frequency of an induction machine at 1.0 p.u. machine voltage

V_t for ranges of machine speed ν and output power P_t. The search variables are magnetizing reactance X_m expressed in ohms per p.u. frequency and effective rotor resistance R_{rotor} equal to R_r/s in ohms. The objectives at each combination of machine speed ν and output power P_t are to obtain V_t equal 1.0 p.u. and to obtain the conductance G_t looking into the machine terminals which is appropriate for the given output power P_t. The search procedure converges quickly and reliably because V_t is strongly dependant on X_m and weakly dependant on R_{rotor} while G_t is strongly dependant on R_{rotor} and weakly dependant on X_m.

A method is described for selecting the size of the self–excitation capacitors for the apparatus based on operation at minimum speed (e.g. 0.95 p.u. speed), maximum load, minimum rectifier firing delay angle (e.g. 5 degrees) and V_t equal to 1.0 p.u. voltage.

A method is also described for developing families of curves which define the average outputs of the rectifier I_d and V_d which are required for maintaining machine voltage at 1.0 p.u. voltage and providing the necessary power to the load. The curves of I_d and V_d are given as functions of machine speed ν and power P_t.

7.3 Conclusions from Chapter 3 – Electromagnetic Transients Simulation

The third chapter describes special modifications for adapting an electromagnetic transients simulation program based on the trapezoidal algorithm of Dommel [16]. The modifications facilitate the simulation of systems which include arbitrarily specified configurations of power–electronic switching devices such as diodes, thyristors, and GTO devices. A technique is also described for improved simulation of self–excited induction machines. The techniques have

been incorporated into a prototype program which was instrumental in developing and testing the control methods described in chapter 4.

The modifications to the conventional algorithm are based on three techniques. The three techniques when combined in the prototype simulation program result in shortened preparation time for simulating new power electronic apparatus.

A technique is described for representing devices according to simple v–i characteristic curves. The main benefit here is not to represent the characteristics accurately but to improve the numerical performance of the program when devices in close proximity are switched simultaneously. Iteration of the solution within the same time–step is carried out to ensure that the solution always falls on the v–i characteristic. However, the program has an automatic selection criterion that only iterates the solution when required and no iteration takes place in the periods between device switchings.

The prototype program permits the use of two time–step sizes during a simulation. A specifiable large time–step size is the default. However, a sequence of small time–steps can be used either to accurately locate a switching point or to gradually change the characteristic for a device between the "on" and "off" characteristics. The available choice of a large time–step size allows the simulation to progress at an increased rate when switching is not in progress.

A modification to the conventional Dommel simulation algorithm is described for eliminating numerical oscillations from the solutions for capacitive loops and inductive nodes. The modification allows for the continuous use of the trapezoidal integration method but also eliminates the numerical oscillations. The more accurate trapezoidal integration method is preferred as a component in the modified algorithm rather than the backward Euler method because the

modified algorithm is used in ever time–step rather than only at expected solution discontinuities.

A modified induction machine model is implemented in the prototype simulation program which provides a more accurate simulation of the dynamics of self–excitation. The modification has also been suggested by Hallenius et al [14]. The effectiveness of the modification to the induction machine model is confirmed by comparison of simulation results to laboratory test results.

7.4 Conclusions from Chapter 4 – Control System Design

A control system for the apparatus has been developed consisting of a feed–forward control which provides quick response to sudden load changes combined with a feed–back control which corrects for error in the feed–forward control.

The model used in the feed–forward control is provided in Look–up Tables containing the curves of I_d and V_d developed as functions of machine speed ν and power P_t. The curves are developed using non–linear search techniques as described in Chapter 2.

The contribution to the dc current order $I_d(ord)$ produced by the feed–forward control consists of the basic dc current reference $I_d^*(ord)$ from the Look–up Tables multiplied by p.u. machine voltage magnitude V_m. The multiplication of $I_d^*(ord)$ by machine voltage magnitude V_m adjusts the feed–forward component of the current order $I_d(ord)$ to stabilize and correct V_m during temporary undervoltages and overvoltages in V_m.

The PI controller in the Rectifier Current Controller responds to error in V_m so as to correct and stabilize V_m. Steady running error in V_m is removed by the contribution to the dc current order provided by the integrator in the PI control-

ler. Minor oscillations in machine voltage magnitude V_m during operation at high speed and no load are eliminated by the proportional output of the PI controller.

The control system regulates both machine voltage and load voltage to 1.0 p.u. voltage during steady running. The frequency of the load voltage is fixed at fundamental frequency by the inverter firing logic while the speed of the machine is permitted to vary.

The operation of the Transvektor [26] type phase locked oscillator (PLO) is demonstrated using a laboratory apparatus. It is confirmed to within the accuracy of the laboratory apparatus that this type of PLO tracks the angle of the positive sequence of the input voltages.

7.5 Conclusions from Chapter 5 – Simulated Performance of the Apparatus

The prototype simulation program was used to simulate the full apparatus including the self–excited induction machine; the controlled rectifier; the voltage–boost converter; the voltage–sourced inverter; the control system; and the shunt filters on the load bus. The main conclusion to be drawn from the simulations is that the control system is effective in controlling the apparatus during steady running and transient conditions.

The simulations show that the control system provides acceptable control of the apparatus for load powers ranging between 0.0 and 1.0 p.u. power and for machine speeds in the design range between 1.0 and 1.4 p.u. speed. The ac load voltage during steady running is regulated to essentially 1.0 p.u. load voltage

at fundamental frequency in these ranges of speed and power. The machine voltage is similarly regulated to 1.0 p.u. machine voltage.

The control system also provides dynamic regulation of the ac load voltage to within plus or minus 12 percent of rated voltage during sudden application or rejection of full ac load while running at either the minimum or maximum design speed. The control system similarly provides regulation of machine voltage to within plus or minus 18 percent of rated voltage during these extreme load changes.

An additional conclusion to be drawn from the simulations is that a twelve–pulse voltage–sourced inverter can provide ac load voltage of generally acceptable harmonic content when shunt filtering is provided on the load bus.

The simulation results for the thesis apparatus demonstrate that the numerical oscillation suppression technique described in chapter three is effective in suppressing numerical oscillations in the solutions for capacitive loops and inductive nodes in a practical simulation.

7.6 Conclusions from Chapter 6 – Performance of the Laboratory Apparatus

An apparatus was built and tested in the laboratory to confirm the operation of the main control system. For each laboratory test a corresponding electromagnetic transients simulation was conducted. The laboratory testing generally confirms the operation predicted by the transients simulations.

The laboratory testing shows that the control system can initiate self–excitation in the apparatus and subsequently stabilize the machine voltage and load voltage at desired levels. This start–up performance is demonstrated with full

load either connected or disconnected during starting at any speed between the minimum and maximum design speeds of 1.0 and 1.4 p.u. speed.

The laboratory testing shows that the control system provides acceptable control of the apparatus during sudden full load rejection as expected based on the simulations. The control system also controls the apparatus well during sudden application of full load commencing from no load. This performance is demonstrated for any speed between the minimum and maximum design speeds.

The laboratory testing points out a difficulty which can be encountered in simulating apparatus which is controlled by the combination of a fast–acting feed–forward control which is based on a model and a slow–acting feed–back control loop which corrects for errors in the model. The simulated response can be too close to ideal if the feed–forward control model does not match the real apparatus as well as the feed–forward model matches the simulated apparatus. The simulated apparatus can show a better response than the real apparatus because the feed–forward model and the simulation model of the apparatus are often based on precisely the same parameters whereas there may be more discrepancies between the feed–forward control model and the real apparatus.

The laboratory testing confirms that the PI controller in the Rectifier Current Controller is a necessary supplement to the feed–forward control and removes error and small oscillations in machine voltage V_m during steady running.

The laboratory testing also confirms that the control system will reduce the load voltage to prevent overload of the apparatus in circumstances where the load resistance drops too low.

Finally, the laboratory testing demonstrates that a practical and effective high performance control system can be implemented for the apparatus based on a single digital signal processor (DSP) chip.

7.7 Summary

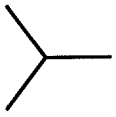
This thesis describes the development of an apparatus for supplying an isolated ac load from a self–excited induction generator operable at variable speed. A novel and synergistic configuration of apparatus is specified. New simulation techniques are implemented in a prototype electromagnetic transients simulation program in order to provide an effective tool for developing the apparatus. A control method is described for the apparatus based on a developed understanding of the characteristics of the apparatus. The control system is implemented in a laboratory apparatus in order to demonstrate the practical nature of the control method. The satisfactory dynamic and steady running performance of the apparatus is demonstrated through transients simulation and laboratory testing.

Appendix I

Induction Machine Data

Appendix I – Induction Machine Data

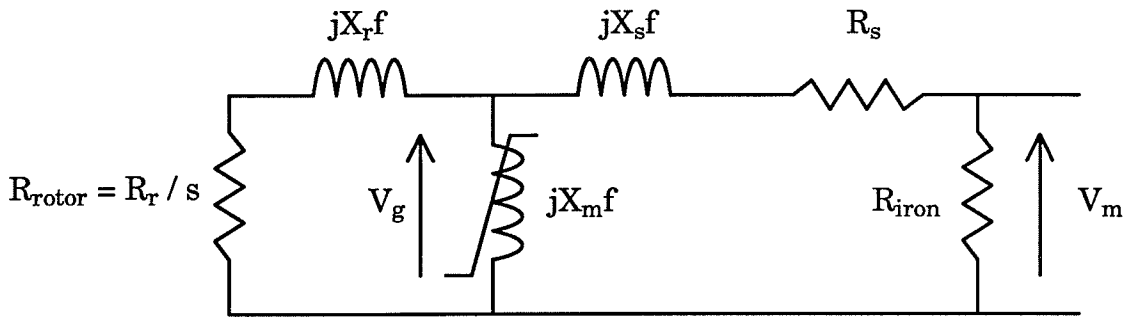
This appendix contains the parameters of the induction machine simulated as described in Chapter five and used in the test apparatus as described in Chapter six.

ASEA	Made in Sweden
Motor MBT 132S	IEC 34 – 1
Three Phase 60 Hz.	No. 7523528
6.3 kW	1725 r.p.m.
0.84 p.f.	Cl. F
 360 Volts 14.4 Amps	 208 Volts 25.0 Amps IP 54 40 kg

Name Plate Data

The machine is connected in delta. The appropriate base quantities are therefore as follows:

I_{base} = 25.0 Amps
V_{base} = 120 Volts (line to neutral)
Z_{base} = 4.8 Ohms



Induction Machine Equivalent Circuit

The leakage reactances and resistances of the machine at 1.0 p.u. frequency are as follows:

X_s	=	0.101 p.u.
R_s	=	0.056 p.u.
X_r	=	0.097 p.u.
R_r	=	0.056 p.u.
R_{iron}	=	32.8 p.u.

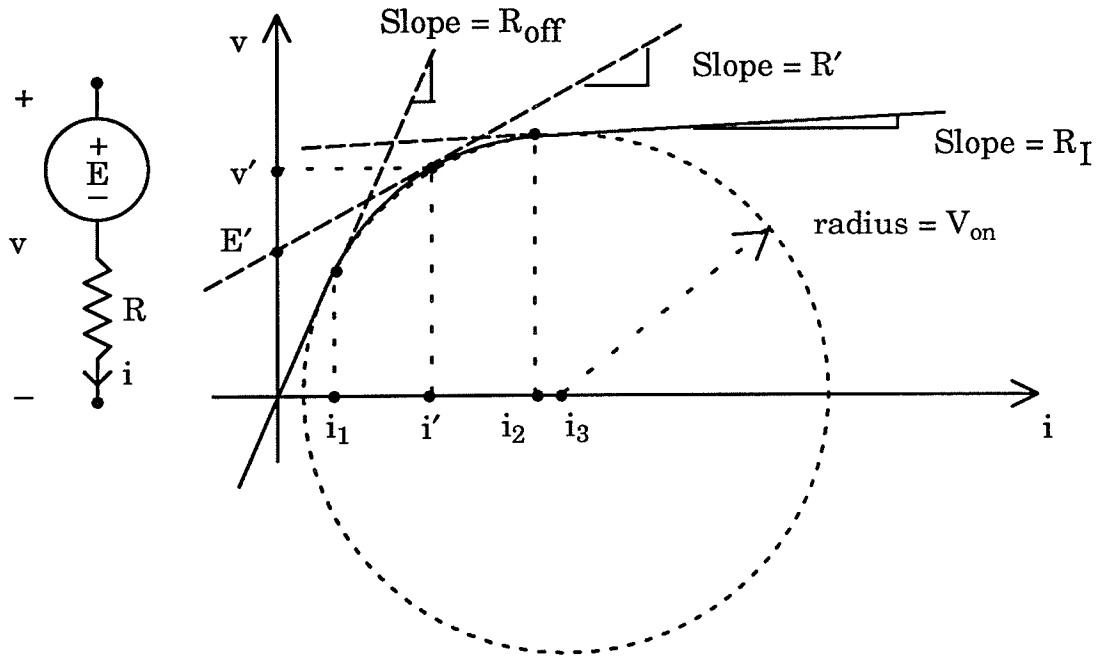
The induction machine magnetizing curve is as follows:

V_g (p.u.)	I_m (p.u.)	X_m (p.u.)
0.276	0.100	2.76
0.416	0.145	2.86
0.556	0.197	2.83
0.694	0.258	2.69
0.830	0.333	2.50
0.898	0.380	2.36
0.955	0.423	2.26
0.986	0.459	2.15
1.00	0.476	2.10
1.05	0.535	1.96
1.09	0.614	1.77
1.11	0.650	1.71

Appendix II

Representation of a Simple Characteristic Curve

Appendix II – Representation of a Simple Characteristic Curve



The simple characteristic curve used to represent a device consists of two straight lines tangent on the arc of a circle as illustrated above. The characteristic curve defines the voltage source E′ and resistance R′ used to represent the device for a given i′.

The projections i_1 and i_2 from the two tangent points onto the current axis as well as the center i_3 of the circle can all be calculated based on R_I, R_{off}, and V_{on} using basic trigonometry. In the simulations described in Chapter 5 the values defining the "on" characteristic are

V_{on} = 1.0 Volts

R_{off} = 1.0×10^6 Ohms

R_I = 0.01 Ohms

Note:
$i_2 \approx$ 1.0 Amp

The corresponding magnitudes i_1, i_2, and i_3 are specified as follows:

$$i_1 = \frac{V_{on}\ x^2}{\sqrt{1 + x^2}} \qquad \text{Defn: } x = 1 / R_{off}$$

$$i_3 = V_{on}\sqrt{1 + x^2}$$

$$i_2 = i_3 - \frac{V_{on}\ R_I}{\sqrt{1 + R_I^2}}$$

The characteristic curve for $i \leq i_1$ is of course represented by the following equations:

$$R = R_{off} \qquad v = R_{off}\ i$$

$$E = 0.0 \qquad i = v / R_{off}$$

In the region $i_1 < i < i_2$ the magnitudes of v and i on the characteristic curve are related according to the following equations:

$$v = \sqrt{V_{on}^2 - (i_3 - i)^2}$$

$$i = i_3 - \sqrt{V_{on}^2 - v^2}$$

The equations take this form because mathematically they describe a circle of radius V_{on} centered at i_3 on the current axis. The current axis could be scaled to cause full forward voltage drop to occur at a higher or lower level of current.

The resistance R and series voltage source E representing the device in the region $i_1 < i < i_2$ are given by the following equations:

$$R = \frac{dv}{di} = \frac{i_3 - i}{v} \qquad \text{and} \qquad E = v - Ri$$

In the region $i \geq i_2$ the the device can again be represented by a constant resistance $R = R_I$ and a constant series voltage source $E = E_2$ where E_2 is given by the following equation:

$$E_2 = \sqrt{V_{on}^2 - (i_3 - i_2)^2} - R_I i_2$$

In the region $i \geq i_2$ the magnitudes of v and i on the characteristic curve are related according to the following equations:

$$v = E_2 + R_I i \qquad\qquad i = \frac{v - E_2}{R_I}$$

The resistance R and the voltage source E representing the device branch are varied in a controlled manner during the iteration procedure which is carried out in the switching zone $i_1 < i < i_2$. The appropriate resistance and series voltage source are respectively R′ and E′ at a given current i′ as shown in the above diagram. It is useful to be able to calculate the change Δi in i′ which will cause R′ to be changed in an iteration by a factor S_f. The equations for the characteristic curve in the switching zone $i_1 < i < i_2$ can be used to show that

$$\Delta i = y \left[1.0 - \sqrt{\frac{V_{on}^2 S_f^2}{(S_f^2 - 1.0) y^2 + V_{on}^2}} \right]$$

where $y = (i_3 - i')$

Appendix III

Data for the Voltage–sourced Inverter

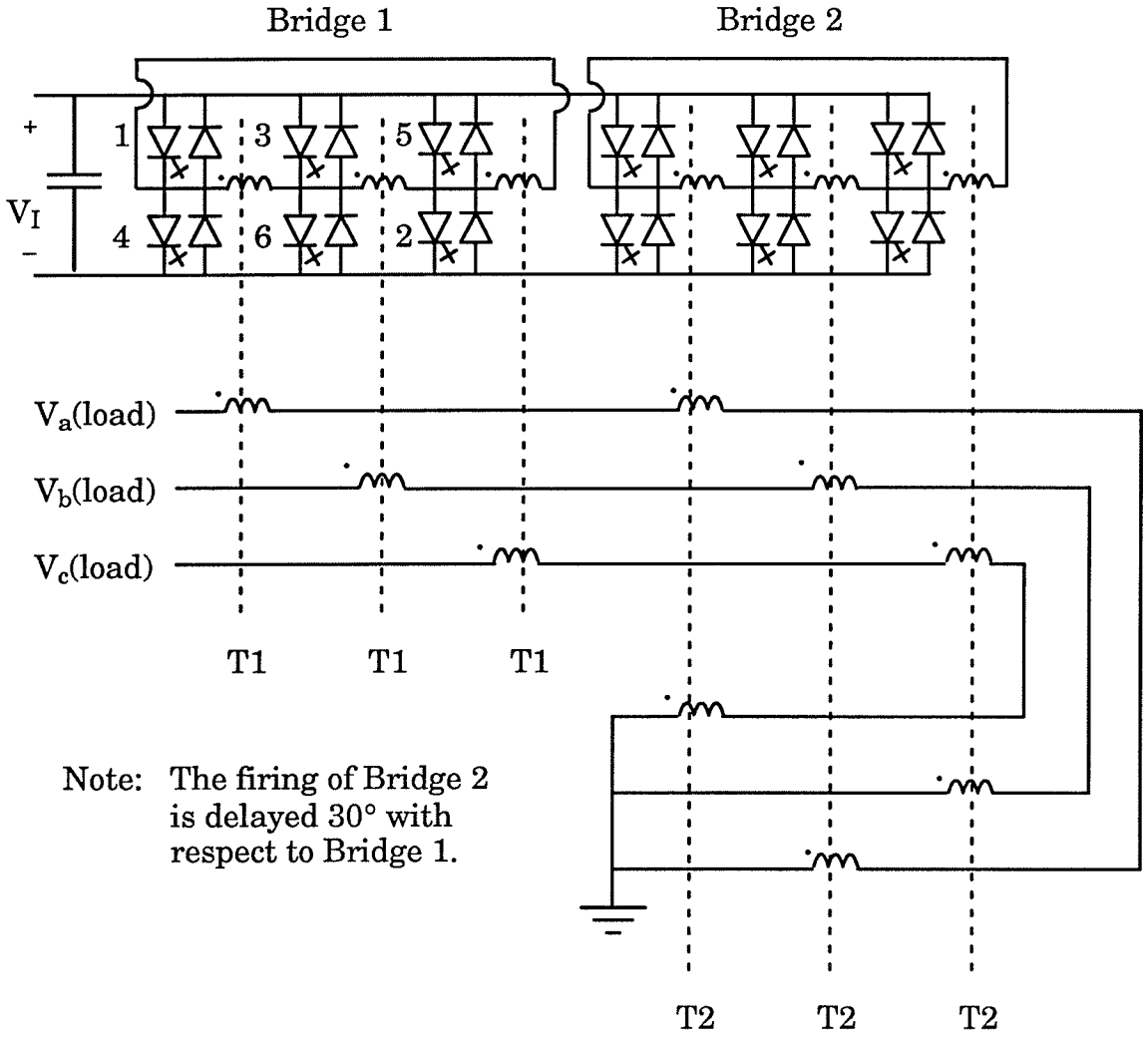
and

Shunt Filtering

Appendix III – Data for the Voltage–sourced Inverter and Shunt Filtering

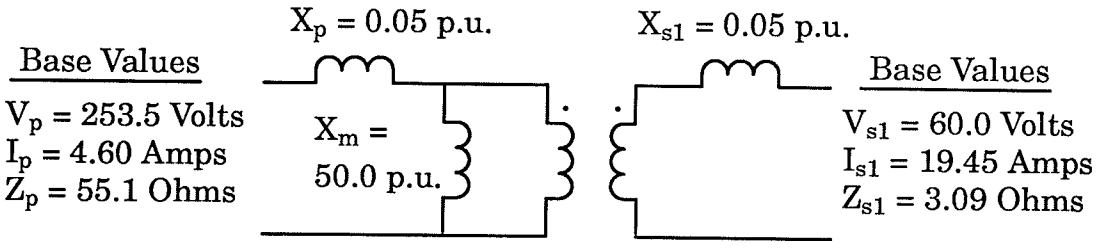
The Voltage–sourced Inverter

The transformer connection diagram for a twelve–pulse voltage–sourced inverter simulated in Chapter 5 is illustrated below. The voltage–sourced inverter is designed for 5.6 kW at 0.8 p.f. lagging. The total rating of the transformer is therefore 7.0 kVA (based on fundamental–frequency components only).

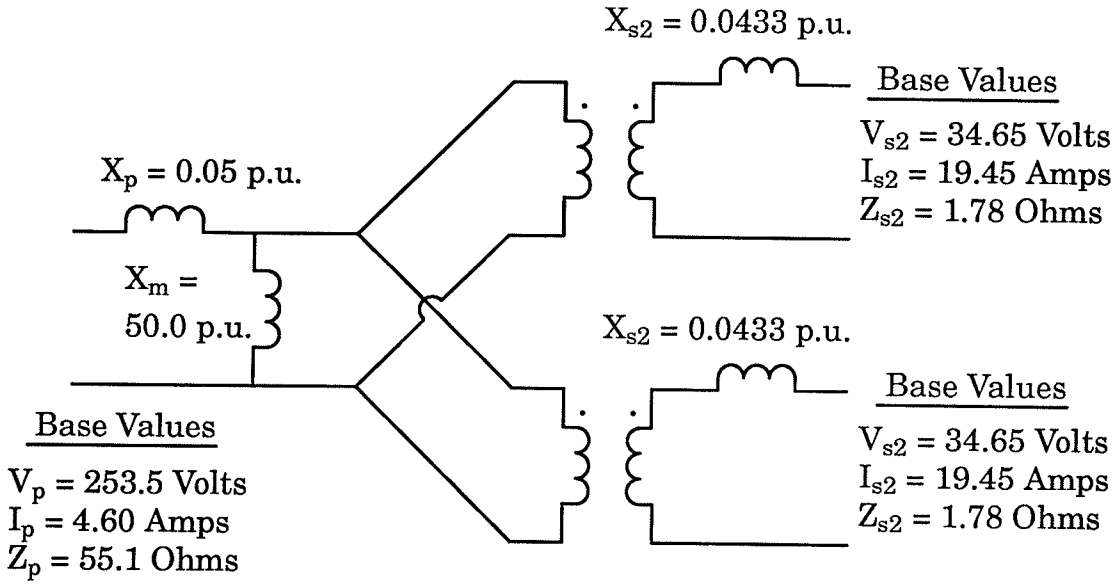


Transformer Connection Diagram for a Twelve–pulse Voltage–sourced Inverter

The twelve–pulse inverter bridge consists of two six–pulse inverter bridges as illustrated in the above diagram. The firing sequence for the GTO thyristors in Bridge 1 is 1–2–3–4–5–6 as marked in the diagram. Each GTO goes "on" for 180° and then "off" for 180°. The firing sequence of Bridge 2 is the same as Bridge 1 except that the firing of Bridge 2 is delayed 30° with respect to Bridge 1. Bridge 1 contains 3 two–winding transformers (each referred to as type T1) while Bridge 2 contains 3 three–winding transformers (each referred to as type T2). The ratings and parameters of the transformer types are shown in the diagram below and are selected according to the discussion which follows:

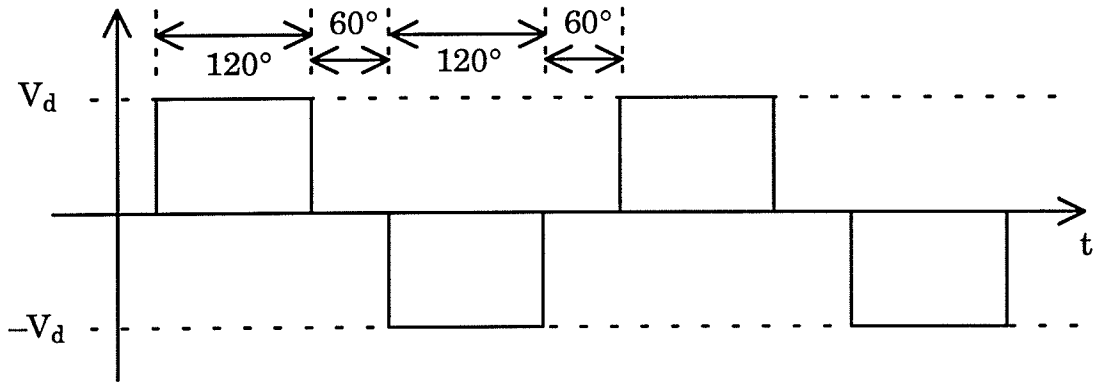


Equivalent Circuit of Transformer Type T1



Equivalent Circuit of Transformer Type T2

The primary (converter side) windings of transformer types T1 and T2 each have the following waveshape applied by the inverter bridges:

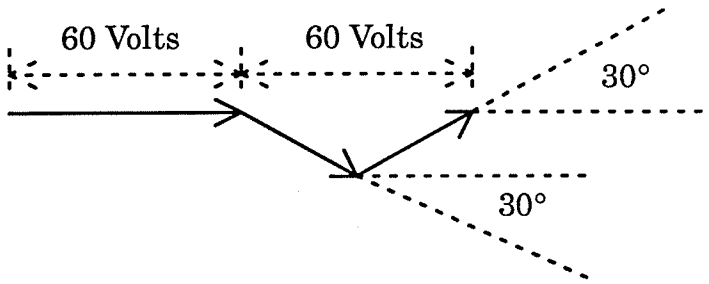


The RMS magnitude of the fundamental component of voltage applied to the primary windings is therefore

$$V_p = 0.78\, V_d$$

The limits on the dc capacitor voltage reference V_{Iref} shown in Figure 33 are 310 and 340 Volts. The transformer types T1 and T2 are therefore designed for the average voltage of 325 Volts. The rated voltage of the primary windings is therefore V_p equal 253.5 Volts.

Bridge 1 contributes 50% of the rated load voltage of 120 Volts RMS. Therefore the rated secondary voltage of T1 is V_{s1} equal to 60 Volts RMS. The transformers T1 and T2 contribute to each phase of the load voltage according to the following phasor diagram:



Based on the above phasor diagram the voltage rating of each of the secondary windings in a type T2 transformer is therefore:

$$V_{s2} = (1/2)(2 / \sqrt{3}) 60 \text{ Volts} = 34.65 \text{ Volts}$$

The primary windings of transformer types T1 and T2 and the secondary winding of transformer type T1 are each rated at $S_p = 7 \text{ kVA} / 6 = 1167 \text{ VA}$. Therefore in the above equivalent circuits:

$$I_p = 4.60 \text{ Amps}$$

$$Z_p = 55.1 \text{ Ohms}$$

$$I_{s1} = 19.45 \text{ Amps}$$

$$Z_{s1} = 3.09 \text{ Ohms}$$

The secondary windings of T2 must carry the same current as the secondary winding of T1. Therefore:

$$I_{s2} = 19.45 \text{ Amps}$$

$$Z_{s2} = 1.78 \text{ Ohms}$$

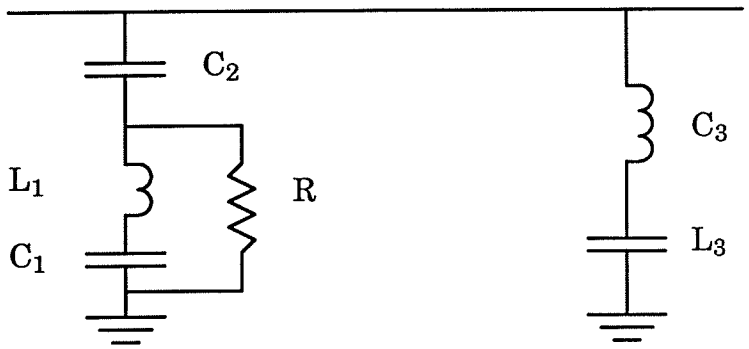
The leakage reactances X_p and X_{s1} are each selected as 0.05 p.u. on the respective base impedances Z_p and Z_{s1}. For a given phase it is desired to have the same total fundamental–frequency voltage drop in the two T2 secondaries as occurs in the one secondary of T1. Therefore:

$$X_{s2} = \frac{Z_{s1} \, X_{s1}}{2 \, Z_{s2}}$$

$$X_{s2} = 0.0433 \text{ p.u.}$$

Shunt Filtering

A C–type filter and a 11th harmonic tuned filter are connected as shunt filters on each phase of the load bus in the apparatus simulated in Chapter 5.



C–type Filter Tuned Filter

Each phase of the load bus is rated as follows:

$$S = 2334 \text{ VA}$$

$$V = 120 \text{ Volts}$$

$$I = 19.45 \text{ Amps}$$

$$Z = 6.167 \text{ Ohms}$$

C–type Filter

The C–type filter used in Chapter 5 places 0.25 p.u. of capacitive support on the load bus and has a Q of 2 at the 5th harmonic.

In the C–type filter L_1 and C_1 in series are tuned to pass fundamental frequency current without voltage drop. Therefore C_2 is selected to provide the desired kVAR rating. Therefore

$$C_2 = 0.25 / (\omega_o Z) = 107.5 \ \mu F$$

In the C–type filter the series connection of C_2, L_1, and C_1 are tuned to the 5th harmonic. Therefore:

$$C_1 = \left[\left(\frac{f_n}{f_o} \right)^2 - 1 \right] C_2$$

where $f_n = 300$ Hz and $f_o = 60$ Hz.

or $C_1 = 2.58$ mF

As noted above L_1 and C_1 in the C–type filter are tuned to the fundamental frequency. Therefore:

$$L_1 = 1 / (4 \pi^2 f_o^2 C_1) = 2.728 \text{ mH}$$

In the C–type filter a Q of 2 means the impedance of L_1 is twice R at the tuned (fifth) harmonic, f_n. Therefore:

$$R = 2 \pi f_n L_1 / Q = 2.571 \text{ Ohms}$$

The 11th Harmonic Tuned Filter

One tuned filter is provided on each phase of the load bus. The filter is tuned to the lowest characteristic harmonic which is the 11th harmonic and places 0.1 p.u. of capacitive support on the load bus. Therefore:

$$C_3 = 0.1 / (\omega_o Z) = 43 \mu\text{F}$$

$$L_3 = 1 / (\omega_n^2 C_3) = 1.352 \text{ mH}$$

References

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