SIMULATION AND CONTROL OF ACTIVE FILTER

BY

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A Thesis
Submitted to the Faculty of Graduate Studies
In Partial Fulfillment of the Requirements for the Degree of

MASTER OF SCIENCE

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THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

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ACKNOWLEDGEMENTS

I gratefully acknowledge my advisor Prof. A. M. Gole for his excellent guidance. It is a great opportunity for me to share Dr. Gole's expertise in the HVDC and power electronics in these years.

Special thanks and grateful acknowledge extend to Dr. Athula Rajapakse and Dr. Kwok-Wai Louie for their patient review, suggestion and correction for this thesis.

I also like to express my thanks to Prof. Menzies and Prof. Annakkage for their excellent lectures and patient discussion on the wide variety of power engineering topics to improve my knowledge on power electronics and power system.

I am grateful to my employer, Manitoba HVDC Research Centre, for the support of this work.

Special thanks are extended to my parents and my husband Yi Zhang, for their support and patience during the time I worked on this thesis.

ABSTRACT

Active filters are electronic devices that absorb the harmonic contents in power systems, which are produced by nonlinear loads or apparatus such as High-voltage-direct-current (HVDC) systems. This thesis investigates the basic control philosophy of active filter systems. According to their control strategies active filters can be of two types: the direct control and the indirect control. The direct method detects harmonics in the loads and injects current through an active filter to cancel the harmonics. On the other hand, the indirect method senses the harmonics in an AC network, and injects harmonic currents using feedback control to reduce the harmonics. Both analytical and simulation methods are used for the study. The ideal compensation is analyzed based on circuit theory. Both the direct and the indirect control approaches are investigated by numerical simulation. The effect of time delay on the performance of the direct method is studied in detail by both the theoretical analysis and the numerical simulation technique. By implementing a numerical simulation example, it has been demonstrated that the direct method is not robust enough when the time delay in the control circuits is considered, and the indirect method is more reliable. All the simulations in the thesis are performed by the power system simulation tool PSCAD/EMTDC.

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--Chapter 1--

INTRODUCTION

1.1 BACKGROUND

Harmonics in power systems have received increased attention in recent years with the widespread application of solid state power switching devices and microprocessor controlled technology. Three phase ac power systems have a substantial number of harmonics generating devices. For example, static power converters and adjustable speed drive systems draw non-sinusoidal load currents primarily composed of the odd harmonics. High-voltage-direct-current (HVDC) converter stations, due to their high level of ac- and dc-side harmonic generation, have traditionally required the installation of shunt passive filters on both sides. However, shunt passive filters have many problems that discourage their applications. In recent years, active power filters have been widely investigated for the compensation of harmonics in the electric power system. The active filters are power electronic devices that can be designed to absorb the harmonic currents in a network, which are produced by nonlinear loads or apparatus such as HVDC systems. Therefore, active filters enable an ac system to be free of harmonic currents. The basic concept of an active filter can be shown in Figure 1.1. The active filter operates by injecting harmonic currents into the utility system with the same magnitudes as the harmonic currents generated by a given non-linear load, but with opposite phases. The active filter can be a controlled current source or a controlled voltage source, which are realized by using pulse-width-modulation (PWM) technique. With the widespread use of

harmonic generating power electronic-based devices, the control of harmonic currents is becoming increasingly important. Thus, the main focus of this thesis is to investigate the control strategies of active filters.

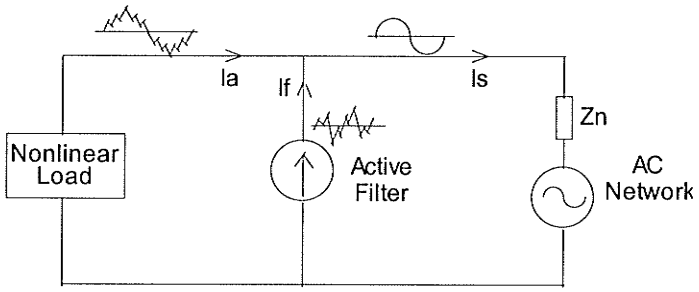


Figure 1.1 Basic concept of an active filter

Comparisons between passive and active filters have been discussed in many papers. The following are the major advantages and disadvantages of passive filters and active filters:

Advantages of passive filters:

1. Shunt filters have the advantage of providing the reactive compensation needed by the network for supporting voltage.

2. The single tuned filters and high-pass filters are the simplest to design and least expensive to implement.

Disadvantages of passive filters:

1. The source impedance influences the compensation characteristics of the LC filters.

2. At specific frequencies, there can exist an anti-resonance between source impedance and LC filters. In addition, the harmonic currents generated by the distorted non-sinusoidal source voltage, flow into the LC filters from the source.

3. Frequency variation of the power system and tolerances in filter components affect the compensation characteristics of the LC filters. As a result, the size of the components in each tuned branch becomes impractical if the frequency variation is large.

4. Overload occurs when the load harmonics increase.

The following are the major advantages and disadvantages of the active filters:

Advantages of active filters:

1. Harmonic current of any frequency can be reduced by the same equipment.

2. Their capacity is decided by harmonic current magnitude only.

3. Active filters constantly monitor the load current and continuously adapts to changes in load harmonics.

Disadvantages of active filters:

1. Because of the use of electronic devices, it is difficult to realize these devices in large ratings, and yet, preserve a good frequency response with low losses.

2. The initial and running costs of the active filters can be high compared to those of LC filters. [2]

1.2 LITERATURE SURVEY

Numerous studies have been carried out to investigate the application of active filters in power systems. Most of the published studies can be classified into one of the following four categories:

1. Comparison of active and passive filters;

2. New configuration of active filters;

3. Control of active filters;
4. Application of active filters.

The main contributions and developments of these papers are summarized as follows.

1. Comparison of active and passive filters.

Reference [1] evaluates the technical and economic feasibility for active filtering of the dc-side voltage harmonics and the ac-side current harmonics produced by a HVDC converter. The designs for the active filter are compared with the existing ac-side and dc-side passive filters used at the Dickinson terminal of the CU HVDC transmission line project in the USA. A cost comparison is made between these active filter designs and the cost of the existing passive filters supplied by the United Power Association (UPA).

Reference [2] provides a brief review of the various conventional passive harmonic filters that are used in many industrial power systems. It discusses the fundamental principals of active filters. Two particular types of active filters, one based on analog signal control and the other on Pulse Width Modulation (PWM) control, are implemented.

2. Circuit topologies of active filters

A new hybrid topology and its control are presented in [4] to prevent harmonic currents from entering the power system. Analysis shows that in the proposed filter, the power electronic converter has a smaller rating when compared to the converter rating in other active filter systems. The control of this filter under transient conditions, such as start up and during steady state, is demonstrated by means of simulations.

Reference [8] proposes a similar combined system of a passive filter and a small-rated active filter, both connected in series with each other. The active filter plays a role in

improving the filtering characteristics of the passive filter. This results in significantly reducing the required rating of the active filter and eliminating the limitations faced by using only a passive filter. The combination system leads to a practical and economical system.

Reference [10] also introduces a combination filter system comprised of a shunt passive filter and a series active filter. The compensation principle is described and some interesting filtering characteristics are discussed in detail.

Reference [15] presents a new three-phase series resonant active filter. The proposed approach employs a series resonant LC tank tuned to a high frequency along with PWM rectifier topology to cancel lower order harmonics (5th, 7th, 11th, and 13th) generated by nonlinear loads. The PWM control of the active filter allows for independent control of several lower order harmonics (5th, 7th, 11th, and 13th) both in amplitude and in phase. As well, it effectively cancels load generated harmonics under varying load conditions.

Reference [16] presents an active filter for single-phase system, which comprised of multiple nonlinear loads. The active filter is based on the standard H-bridge inverter. The ac side of the inverter is connected in parallel with other nonlinear loads through a filter inductance; the dc side of inverter is connected to the filter capacitor. The inverter switches are controlled to shape the current through the filter inductor such that the line current is in phase with, and the same shape as the input voltage. Sliding-mode control is used to perform the active modification of the wave shape of the current.

3. Control methods in active filter systems

In fact, control is the most important issue in implementation of active filters and attracts the attention of most literature.

Reference [3] presents a method for reducing higher harmonic current using an active filter on the ac side. The active filter is connected in parallel with the rectifier. Here the system employs an optimum servo controller with dead time compensation.

Reference [5] describes an active filter using quad-series voltage source pulse-width-modulation (PWM) converters. These converters suppress ac harmonics by injecting compensation currents into the ac system. The current calculations for the compensation current references, the compensation characteristics, and the capability of the dc capacitor are discussed theoretically and experimentally. A new control circuit for the dc capacitor voltage is proposed. These discussions focus on transient states, based on the instantaneous reactive power theory. Finally, a passive LC filter is designed to remove the switching voltage and current ripples caused by PWM converters on the ac side.

Reference [6] proposes an active filter with a neural network control using a fixed frequency with variable slope control method to obtain training data. Simulations of the proposed active filter are performed and the results are compared to those with other means of control including constant frequency control, tolerance band control, sliding mode control and PWM control. The results show that the proposed active filter has lower current total harmonic distortion (THD), better power factor and less switching power loss than that with other control methods.

In reference [7] a control technique for active power filter is proposed which not only eliminates the harmonics in the current but also controls the reactive power on the ac side of the inductive drive system. The active filter injects current to completely remove the harmonic components of orders not greater than the pulse number per half cycle. It also controls the input fundamental power factor to become unity.

Reference [9] introduces the harmonics cancellation of a hybrid converter consisting of a line commuted current source converter and a voltage source converter. Inside the hybrid converter, the voltage sourced converter (VSC) is used as an active filter to compensate the harmonics generated on the ac side from the current source converter. By applying both feed forward and feedback controls, an efficient control system is designed so only a small passive ac filter will be needed.

Reference [14] presents a DSP controlled active filter for power conditioning. The active filter is designed to cancel lower order harmonics generated by nonlinear loads using a PWM rectifier topology. The PWM control of the active filter allows for independent control of low order harmonics both in amplitude and in phase. In the mean time, a series of high pass passive filters are used to remove the higher order harmonic currents.

A neural network predictive control strategy for active filters is presented in reference [17]. By predicting the fundamental line current, the active power filter cancels the harmonic distortion currents produced by a motor drive. The predictions are based on readily available signals such as the bridge phase angle, motor armature voltage and rectifier ac side current.

A novel current source active power filter is presented in [20]. It is based on a multi-modular converter with phase shifted Sinusoidal Pulse Width Modulation (SPWM) technique. With this technique, the effect of equivalent high switching frequency devices is obtained with low switching frequency devices, which is very promising for large power equipment, such as active power filters. The pole-placement control on the ac side and proportional integral (PI) control on the dc side are implemented in the active filter system.

4. Application of active filters in HVDC systems or other real engineering systems.

Reference [11] discusses the application of an ac side active filter in HVDC schemes involving capacitor commutated converters. Suitable topology and control algorithms are selected to achieve the necessary objective of filtering the lower order characteristic harmonics. The dependence of the filter's rating on parameters, such as the extent of de-tuning of its passive elements, is investigated.

An active dc filter installed in the Konti-Skan HVDC link in Sweden is described in reference [12]. The active dc filter is connected at the bottom of an existing passive dc filter at the Lindome station. The active dc filter has small physical size and occupies small ground area.

Reference [13] introduces the basic conceptions and design principles of an active filter for ac side at HVDC converters. It proposes an active filter topology that decouples the reactive power supplying and filtering tasks that have been characterizing the traditional HVDC passive ac filters. Exclusive devotion to the filtering function offers several advantages that might compensate for the potentially higher initial costs.

1.3 OBJECTIVE OF THIS THESIS

The objective of this thesis is to investigate the application of active filters in power networks that include other power electronic systems such as controlled rectifiers, HVDC systems etc. Such systems are one of the major harmonic sources in power systems. Traditionally, passive filters were used for harmonic absorption. Typically, tuned passive filters account for about 15% of the cost of a converter station [2]. The potential application of active filters provides improved performance and may reduce the overall system cost. The active filter performance is not affected by aging of devices. Also, the active filter performance does not depend on the utility system impedance and system frequency changes, because the harmonic cancellation currents from the active filter are actively generated by a control system. Although, numerous studies have been done on active filters, there are several important issues that need to be further investigated for their successful practical implementation. This thesis targets one of these important issues: how to achieve efficient control of active filters under the presence of component variations and measurement / control delays.

Specifically, we hope to understand the mechanism by which the active filters eliminate harmonics in the electrical systems. Various types of active filters (voltage source or current source) and various types of harmonic injections (voltage source or current source) need to be investigated.

Secondly, we hope to identify the advantages and disadvantages of the direct control and the indirect control in active filter systems. According to their control strategies, the active filters can be of two types: the direct control and the indirect control. The direct method measures the harmonics in the loads and injects currents through active filters to

cancel the harmonics, such that the AC system is free of harmonic currents. The indirect method senses harmonic current/voltage on AC network bus, and injects active filter currents using feedback control that reduces this harmonic current/voltage to zero. Among the direct and indirect methods, we hope to find out which one is more suitable for real active filter systems. We will recommend one control approach based on the detailed comparison between the direct and indirect control philosophies.

Thirdly, we hope to further investigate the operating characteristics of the recommended control approach by implementing it using the electromagnetic transient simulation program PSCAD/EMTDC.

1.4 THESIS OUTLINE

The thesis is organized as follows:

In chapter 2, a simple system with ideal compensation of the active filter is analyzed based on circuit theory. The purpose of this investigation is to seek a systematic understanding of the performance and the influence of the active filters in power systems.

Preliminary studies on control systems are conducted in chapter 3. The direct and indirect control approaches are compared.

Chapter 4 investigated the effects of control circuit time delay to the performance of direct harmonic elimination.

In Chapter 5, the proportional-integrator (PI) based indirect control approach is tested with realistic active filter circuits through PSCAD/EMTDC simulation.

Finally, the conclusions are presented in chapter 6.

In this thesis, only voltage source converters (VSC) are considered to represent actual active filter since VSC is much more popular than current source converters (CSC) in real system applications. Also only current controlled PWM (CRPWM) type VSCs are used to generate the injection current in this thesis. Such converters form a large class of the converters used in active filter applications. Voltage controlled PWM (SPWM) are not considered in the thesis and their further investigation is recommended for future work.

1.5 THESIS MOTIVATION AND CONTRIBUTION

Although the direct and indirect control methods are reported in literature, a detailed comparative analysis of their performance has previously not been reported, with a view to critically investigating their suitability for practical implementation. Investigation into this aspect is the main focus of the thesis. The primary contributions of this thesis are:

- Investigation of delay on the performance of the direct and indirect controls using analytical and simulation methods.
- Development of detailed transient simulation models for active filters.

--Chapter 2--

THEORETICAL STUDY OF HARMONICS COMPENSATION WITH IDEAL ACTIVE FILTERS

2.1 INTRODUCTION

This chapter examines the essential properties of ideal harmonic compensation on a theoretical basis. The purpose of this investigation is to seek a systematic understanding of the performance and influence of an active filter in a power system.

2.1.1 Topology of active filters

First, we will introduce the background of installing an active filter at a major harmonic source such as in an HVDC system. There are several issues need to be considered in selecting the topology, converter, power source, and control philosophy.

The first concern is the location of the active ac filter. The primary winding of the converter transformer is the only place where the filter would be independent of tap changer operation, and of possible resonance between the ac system and the converter transformer impedance. This is in fact, the most common point of connection of the passive filter.

The next issue is the type of connection to the power system: series or parallel connection. In the series connection shown in Figure 2.1, the active filter would act as a "harmonic isolator", impeding the ac harmonic current from the ac system by means of

presenting high harmonic impedance. This type of connection has some disadvantages in HVDC applications. The filter would have to carry the fundamental current and its insulation level would have to be the same to that of that point in the system. Therefore, harmonic filters are usually parallel connected in HVDC systems as shown in Figure 2.2. A parallel-connected active filter operates as an active harmonic-current "diverter".

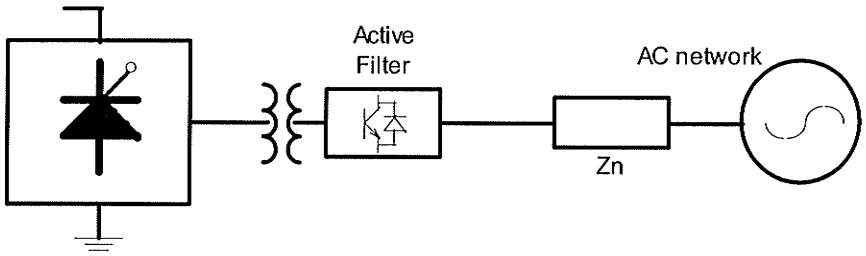


Figure 2.1 Topology of series connected active filter

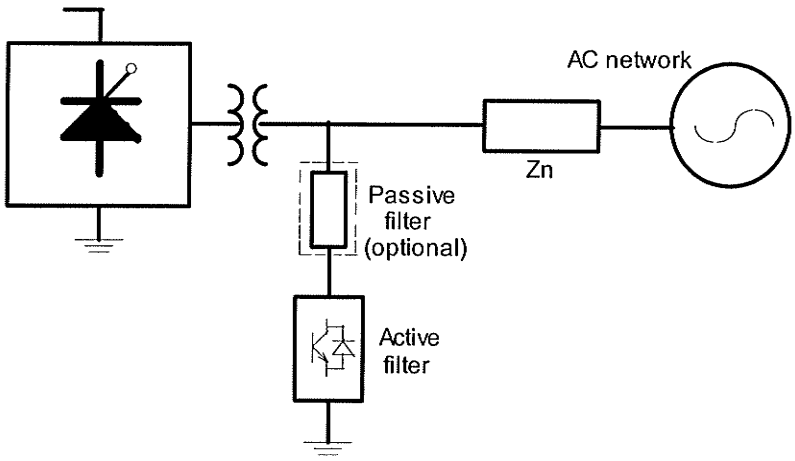


Figure 2.2 Topology of parallel connected active filter

Sometimes, the active filter is connected to the ac system through an impedance. It is shown in Figure 2.2 with the dotted block of optional passive filter. This impedance should meet certain requirements. It should present sufficiently high impedance at the fundamental frequency, so that it effectively reduces the ac fundamental frequency

component of voltage and current at the active source, thereby, resulting in lower rating; it should also offer a low impedance at the harmonic frequencies being injected by the active filter, so as to reduce the required voltage level on the active source. This impedance can be referred to as "path impedance". Sometimes the path impedance is modeled to allow a slightly higher value of fundamental frequency ac current so as to provide a small amount of reactive power support.

The active filter can be implemented as a current source converter (CSC) as shown in Figure 2.3 or as a voltage source converter (VSC) as shown in Figure 2.4 together with its dc-power source. A low-power rectifier can be connected to the ac bus to supply the dc-voltage. Due to the high cost and weight of inductors, and also the advantage of VSC technology, the VSC is the more popular choice and only this is considered further in this thesis.

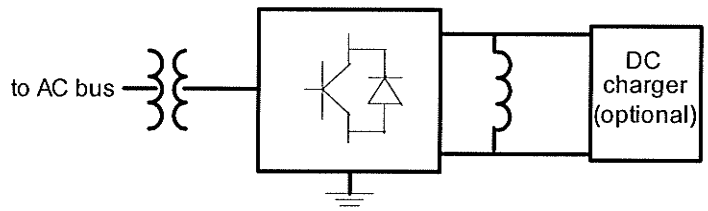


Figure 2.3 CSC type active filter

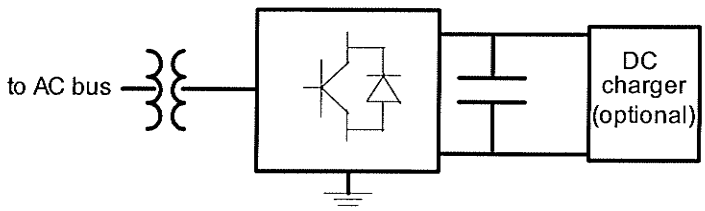


Figure 2.4 VSC type active filter

The control of the output current of the active filter could be of either the voltage referenced sinusoidal pulse-width-modulation (SPWM) or of the current referenced pulse-width-modulation (CRPWM) types. The SPWM controlled active filter operates as a voltage source which provides harmonic voltages on the ac bus, while the CRPWM controlled active filter acts as a current source which injects harmonic current to ac network.

For SPWM, the voltage-reference signal, which would be supplied by the control system of the active filter, is compared to a high frequency triangular wave or carrier in Figure 2.5(a). When the reference waveform is larger than the carrier, the VSC connects the output to the positive dc-voltage, and when smaller, to the negative dc-voltage, as shown in Figure 2.5(b). Thus, the average magnitude of the reference over one period of the carrier is represented in the pulse-width of the output waveform. The switching frequency of the SPWM inverter is determined by the frequency of the triangular carrier waveform.

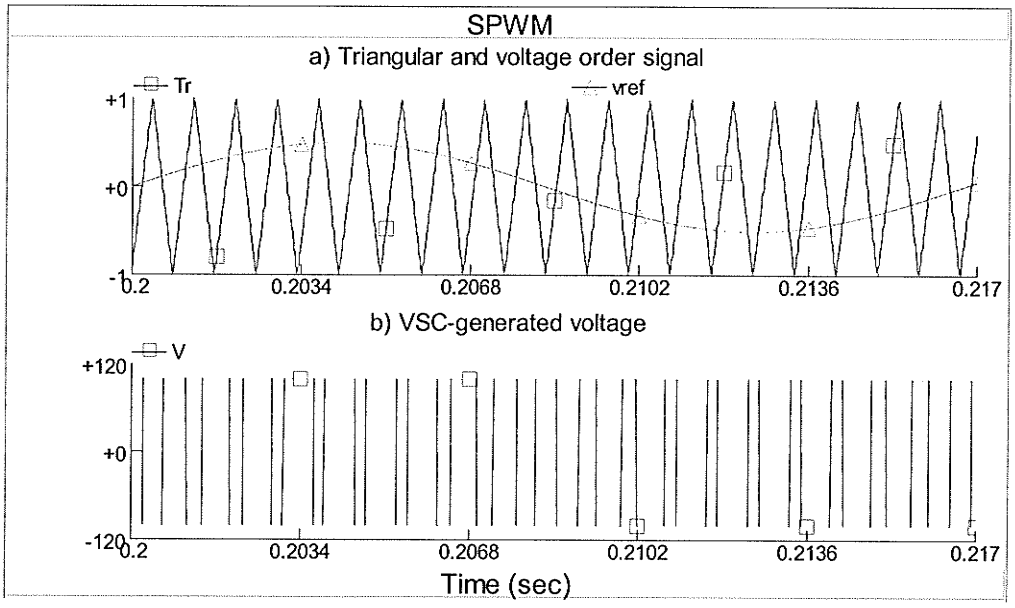


Figure 2.5 SPWM control

For CRPWM, the current signal, which would be supplied by the control system of the active filter, is forced to remain within the pre-specified hysteresis band around the current-reference value by controlling the inverter switches, as shown in Figure 2.6(a). When the current is larger than the upper band of the hysteresis waveform, the VSC connects the output to the negative dc-voltage, and when smaller, to the positive dc-voltage, as shown in Figure 2.6(b). Because the switching is in response to the load current behavior, the CRPWM inverter varies its switching frequency depending on the load condition. The switching frequency is thus not known easily and hence the power electronic device losses are not easily calculated. An upper band on the harmonics targeted for removal is imposed by the maximum allowable switching frequency.

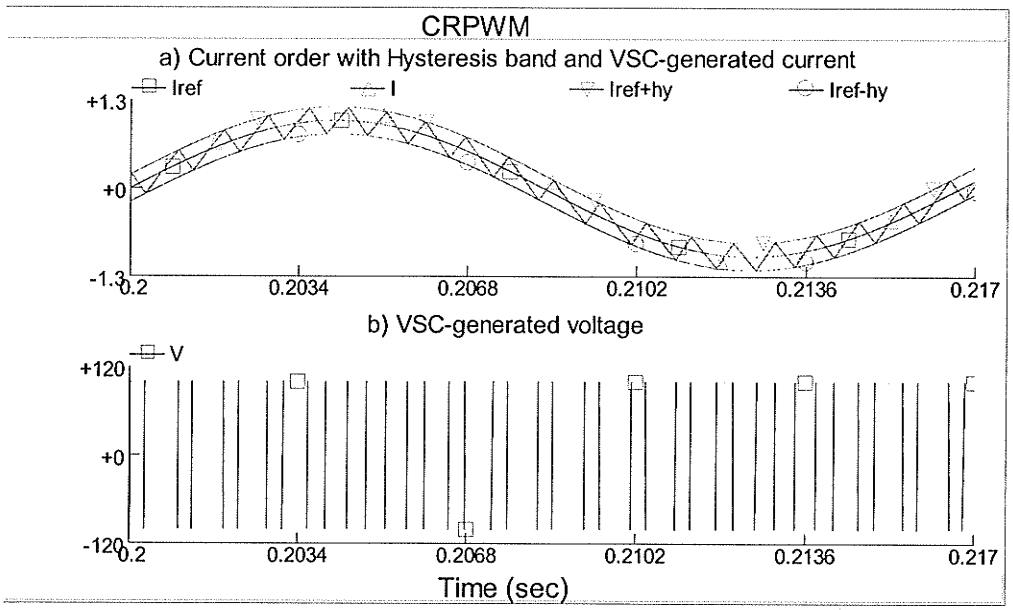


Figure 2.6 CRPWM control

2.1.2 Ideal source representation of the active filter

As we see from the previous section, with different control strategies, the active filter can operate either as a current source or as a voltage source. Therefore, in a simplified analysis a controlled current / voltage source can be used to represent an active filter.

In order to examine the performance of an active filter in a power system, we use a simple circuit with a non-linear load and a source as in Figure 2.7. The block of non-linear load can be an HVDC converter or any other harmonic source. We assume that the simple circuit consists of a non-linear load with fundamental and a harmonic current, such as 11^{th} or 13^{th} harmonic current. The reason we use the 11^{th} or 13^{th} harmonic is that the 11^{th} or 13^{th} harmonic is one of the main characteristic harmonics of 12-pulse converter.

The power system is represented as a Thevenin equivalent circuit, which contains a voltage source E_s and an internal impedance Z_s. The block of the active filter is a controllable current / voltage source that can be considered as the ideal model of an active filter. The basic idea of the harmonic current compensation is to extract the harmonic components from the load current, then let the controllable current / voltage source produces this same current with opposite phases. Therefore the harmonics are cancelled and do not flow into the source side of the power system.

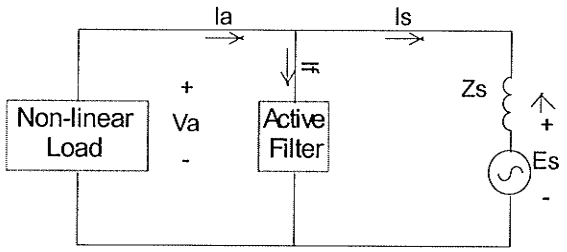


Figure 2.7 test circuit

Basic circuit theory is employed to analysis the circuits. We hope to understand the behavior of active filters by analyzing the circuit in Figure 2.7. Detailed circuit studies will be conducted in the next section. As a result, the basic concepts of control strategies are also discussed.

2.2 ANALYTICAL STUDY

Four typical cases are studied in this section. They are listed as follows:

Case 1) The load is a harmonic current source, the active filter is a current source;

Case 2) The load is a harmonic current source, the active filter is a voltage source;

Case 3) The load is a harmonic voltage source, the active filter is a current source;

Case 4) The load is a harmonic voltage source, the active filter is a voltage source;

2.2.1 The load is a harmonic current source; the active filter is a current source

The circuit diagram for case 1 is shown in Figure 2.8, which is a representation of Figure 2.7 only for harmonic frequency. The circuit of Figure 2.8 can be solved by superposition of the solution to sub-circuits of Figure 2.9(a) and 2.9(b). Figure 2.9(a) and (b) represent the equivalent circuits for the harmonic frequencies. In the following case studies, all the impedances in the harmonic frequency equivalent circuits are calculated at harmonic frequencies. Z_L and Z_S denote the load and the system Thevenin equivalent impedances respectively, while Z_f denotes the internal impedance of the active filter at the harmonic frequency. I_{sh}, I_{ah} and V_{ah} denote the harmonic components of source side current I_s, load side current I_a and bus A voltage V_a of Figure 2.7 respectively.

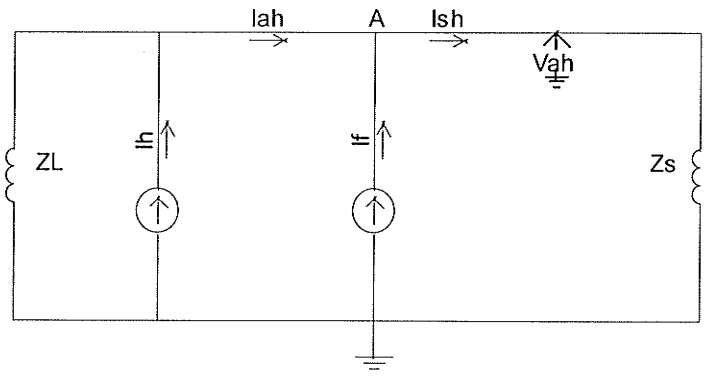


Figure 2.8 Circuit diagram of case 1

(a) *(b)*

Figure 2.9 Sub circuits of case 1

Using the Kirchhoff's Current Law (KCL), we can obtain harmonic component of source side current I_{sh} and load side current I_{ah} as follows

$$I_{sh} = I_f \cdot \frac{Z_L}{Z_L + Z_S} + I_h \cdot \frac{Z_L}{Z_L + Z_S} \tag{2.1}$$

$$I_{ah} = -I_f \cdot \frac{Z_S}{Z_L + Z_S} + I_h \cdot \frac{Z_L}{Z_L + Z_S} \tag{2.2}$$

In the view of the source side, the objective of the filtering is that the harmonics in current flowing to the source equals to zero as

$$I_{sh} = 0 \tag{2.3}$$

If we turn on the active filter, in order to satisfy (2.3), we can get the current order of the active filter as

$$I_f = -I_h \tag{2.4}$$

Therefore, from (2.1) we can get the load side harmonic current with

$$I_{ah} = I_h \tag{2.5}$$

In the view of the load side, the objective of the filtering is to absorb all the harmonics in the load current, so that the current entering the ac source is free of harmonics. This leads the active filter current as

$$I_f = -I_{ah} \tag{2.6}$$

In fact, equation (2.6) can be derived from (2.5) and (2.4). This confirms that the filtering objectives from the source side and the load side are consistent.

If all the harmonics are eliminated, the harmonics voltage at bus A should no longer exist and we have

$$V_{ah} = 0 \tag{2.7}$$

Also by simple circuit analysis, we can know the harmonic current before the active filter is connected as

$$I_{ah} = I_{sh} = I_h \cdot \frac{Z_L}{Z_L + Z_S} \tag{2.8}$$

Compare (2.5) with (2.8), we can see that the load side harmonic current normally increases after the active filter is applied. In the meantime we can check the harmonic voltage at the bus between the load and the system. The harmonic voltage before the active filter is connected is

$$V_{ah} = I_h \cdot \frac{Z_L \cdot Z_s}{Z_L + Z_S} \tag{2.9}$$

2.2.2 The load is a harmonic current source; the active filter is a voltage source

The circuit diagram for case 2 is shown in Figure 2.10, which is a representation of only for harmonic frequency. The circuit of Figure 2.10 can be solved by superposition of the solution to sub-circuits of Figure 2.11(a) and 2.11(b). Figure 2.11(a) and (b) represent the equivalent circuits for harmonic frequencies.

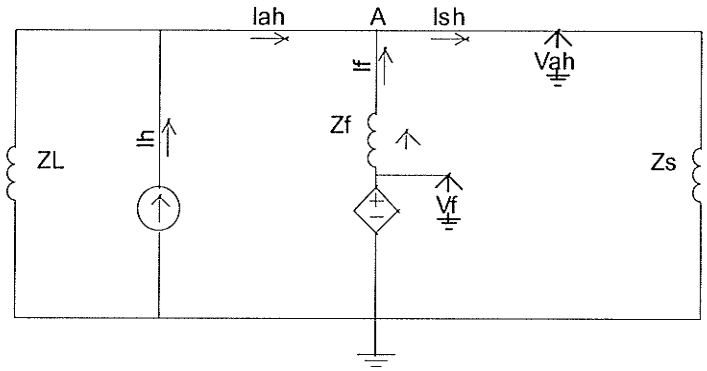


Figure 2.10 Circuit diagram of case 2

(a) *(b)*

Figure 2.11 Sub circuits of case 2

Using the KCL we can obtain

$$I_{sh} = V_f \cdot \frac{Z_L}{Z_L Z_f + Z_S Z_L + Z_f Z_S} + I_h \cdot \frac{Z_f Z_L}{Z_L Z_f + Z_S Z_L + Z_f Z_S} \tag{2.10}$$

$$I_{ah} = -V_f \cdot \frac{Z_S}{Z_L Z_f + Z_S Z_L + Z_f Z_S} + I_h \cdot \frac{Z_L Z_f + Z_L Z_S}{Z_L Z_f + Z_S Z_L + Z_f Z_S} \quad (2.11)$$

In the view of the source side, the objective of the filtering is that the harmonics in current flowing to the source equals to zero as. That is

$$I_{sh} = 0 \quad (2.12)$$

If we want source side free of harmonic current after turning on the active filter, from (2.10) we can get the voltage order of the active filter as

$$V_f = -I_h \cdot Z_f \quad (2.13)$$

Substitute (2.13) to (2.11), the load side harmonic current becomes

$$I_{ah} = I_h \quad (2.14)$$

In the view of the load side, the objective of the filtering is to absorb all the harmonics in the load current. This leads the active filter voltage as

$$V_f = -I_{ah} \cdot Z_f \quad (2.15)$$

If all harmonics are eliminated, the harmonics voltage should no longer exist and we get

$$V_{ah} = 0 \quad (2.16)$$

Also by simple circuit analysis, we can know the harmonic currents before the active filter is connected

$$I_{ah} = I_{sh} = I_h \cdot \frac{Z_L}{Z_L + Z_S} \quad (2.17)$$

It is indicated in (2.17) that the load side current normally increases after the active filter is connected. In the meantime we can check the harmonic voltage at the bus between the load and the system. The harmonic voltage before the active filter is connected is

$$V_{ah} = I_h \cdot \frac{Z_L \cdot Z_s}{Z_L + Z_S} \tag{2.18}$$

2.2.3 The load is a harmonic voltage source; the active filter is a current source

The circuit diagram for case 3 is shown in Figure 2.12., which is a representation of only for harmonic frequency. The circuit of Figure 2.12 can be solved by superposition of the solution to sub-circuits of Figure 2.13(a) and 2.13(b). Figure 2.13(a) and (b) represent the equivalent circuits for harmonic frequencies.

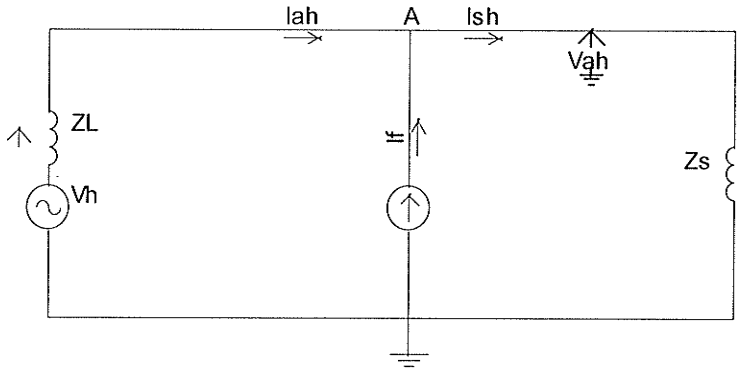


Figure 2.12 Circuit diagram of case 3

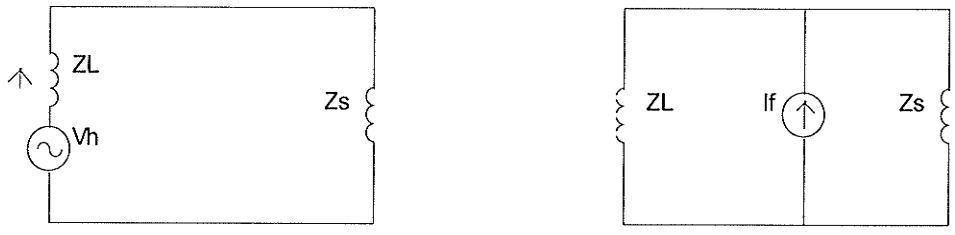


Figure 2.13 Sub circuits of case 3

Using the KCL we can obtain

$$I_{sh} = V_h \cdot \frac{1}{Z_L + Z_S} + I_f \cdot \frac{Z_L}{Z_L + Z_S} \tag{2.19}$$

$$I_{ah} = V_h \cdot \frac{1}{Z_L + Z_S} - I_f \cdot \frac{Z_S}{Z_L + Z_S} \tag{2.20}$$

In the view of the source side, the objective of the filtering is that the harmonics in current flowing to the source equals to zero as. That is

$$I_{sh} = 0 \tag{2.21}$$

If we want total harmonic free in source side after turning on the active filter, we can get the current order of active filter from (2.19)

$$I_f = -V_h \cdot \frac{1}{Z_L} \tag{2.22}$$

Thus from (2.20), the load side harmonic current is

$$I_{ah} = \frac{V_h}{Z_L} \tag{2.23}$$

In the view of load side, the objective of the filtering is to absorb all the harmonics in the load current. This leads the active filter current as

$$I_f = -I_{ah} \tag{2.24}$$

After the active filter is connected, the harmonics voltage should no longer exist:

$$V_{ah} = 0 \tag{2.25}$$

Also by simple circuit analysis, we can know the harmonic current before the active filter is connected as

$$I_{ah} = I_{sh} = \frac{V_h}{Z_L + Z_S} \tag{2.26}$$

In the meantime we can check the harmonic voltage at the bus between the load and the system. The harmonic voltage before the active filter is connected is

$$V_{ah} = V_h \cdot \frac{Z_s}{Z_L + Z_S} \tag{2.27}$$

2.2.4 The load is a harmonic voltage source; the active filter is a voltage source

The circuit diagram for case 4 is shown in Figure 2.14, which is a representation of only for harmonic frequency. The circuit of Figure 2.14 can be solved by superposition of the solution to sub-circuits of Figure 2.15(a) and 2.15(b). Figure 2.15(a) and (b) represent the equivalent circuits for harmonic frequencies.

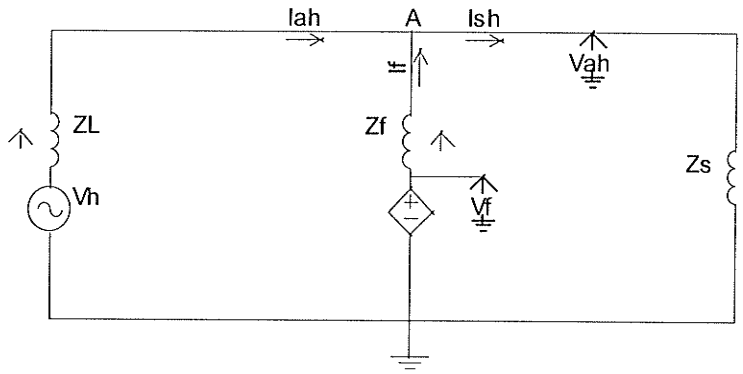
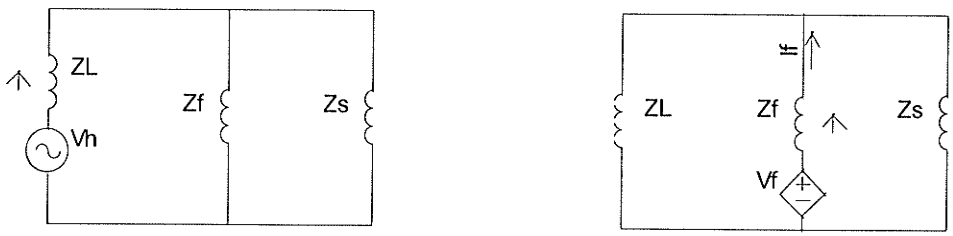


Figure 2.14 Circuit diagram of case 4



(a) *(b)*

Figure 2.15 Sub circuits of case 4

Using the KCL we can obtain

$$I_{sh} = V_h \cdot \frac{Z_f}{Z_L Z_f + Z_L Z_S + Z_S Z_f} + V_f \cdot \frac{Z_L}{Z_L Z_f + Z_f Z_S + Z_S Z_L} \tag{2.28}$$

$$I_{ah} = V_h \cdot \frac{Z_f + Z_S}{Z_L Z_f + Z_L Z_S + Z_S Z_f} + V_f \cdot \frac{Z_S}{Z_L Z_f + Z_f Z_S + Z_S Z_L} \tag{2.29}$$

In the view of the source side, the objective of the filtering is that the harmonics in current flowing to the source equals to zero as. That is

$$I_{sh} = 0 \tag{2.30}$$

After turning on the active filter, in order to satisfy (2.30), from (2.28) we can get the voltage order of active filter as

$$V_f = -V_h \cdot \frac{Z_f}{Z_L} \tag{2.31}$$

Also, we can get the load side harmonic current from (2.29) as

$$I_{ah} = V_h \cdot \frac{Z_f + Z_S - Z_f Z_s / Z_L}{Z_L Z_f + Z_L Z_S + Z_S Z_f} \tag{2.32}$$

In the view of load side, the objective of the filtering is to absorb all the harmonics in the load current. This leads the active filter voltage as

$$V_f = -Z_f \cdot I_{ah} \tag{2.33}$$

Also by simple circuit analysis, we can know the harmonic current before the active filter is connected as

$$I_{ah} = I_{sh} = \frac{V_h}{Z_L + Z_S} \tag{2.34}$$

In the meantime we can check the harmonic voltage at the bus between the load and the system. The harmonic voltage before the active filter is applied is

$$V_{ah} = V_h \cdot \frac{Z_s}{Z_L + Z_S} \tag{2.35}$$

2.3 CONTROL SIGNAL MEASUREMENT OF ACTIVE FILTER

From the above circuits analysis, we observe that certain signals could be used in the control system designs of active filters in different system configurations. This information is useful for further researches in the active filter control. We would like to summarize the results for future use. As we know there are two typical control strategies as direct control and indirect control:

- The direct control is to use the measured load side current to set the active filter current to eliminate the harmonic current directly. The signals required for the direct control are shown in the middle column of Table 2.1.

- The indirect control is realized by approaching a control objective such as the system harmonic current I_{sh} or harmonic voltage V_{ah} being zero, by dynamically adjusting the compensation current or voltage. The signals required for the indirect control are shown in the right column of Table 2.1.

Table 2.1 Control System Signal Measurements

Circuit Type	Direct Control		Indirect Control	
	Objective	Measurement	Objective	Measurement
The load is a harmonic current source The active filter is a current source	$I_f = -I_{ah}$	I_{ah}	$I_{sh}=0$	I_{sh}
			$V_{ah}=0$	V_{ah}
The load is a harmonic current source The active filter is a voltage source	$V_f = -Z_f I_{ah}$	I_{ah}	$I_{sh}=0$	I_{sh}
			$V_{ah}=0$	V_{ah}
The load is a harmonic voltage source The active filter is a current source	$I_f = -I_{ah}$	I_{ah}	$I_{sh}=0$	I_{sh}
			$V_{ah}=0$	V_{ah}
The load is a harmonic voltage source The active filter is a voltage source	$V_f = -Z_f I_{ah}$	I_{ah}	$I_{sh}=0$	I_{sh}
			$V_{ah}=0$	V_{ah}

It is noticed that either current or voltage signals can be used to conduct the indirect control. This is because the objective of the indirect control is to remove harmonics in the circuit, which will result in both the harmonic voltage and harmonic current in the ac systems being zero. On the other hand, the direct control can only be realized by using the load side harmonic current.

2.4 DISCUSSION OF ACTIVE FILTER RATING

The rating of an active filter is a very important concern in designing the filtering systems. Basically we would hope to estimate the size of the active filter based on the information such as the measurements of harmonic current and harmonic voltage or the de-tuning degree of passive filters . It is expected that the size of the active filter depends

not only on the harmonic components amount but also on the electrical system configuration. In this section we will discuss how to estimate the rating of active filters .

Based on the circuit analysis in the previous sections, we can summarize the harmonic voltage and current before the active filter is connected and the corresponding current and voltage orders of active filters in Table 2.2.

Table 2.2 harmonics current and voltage before active filters connected and orders of active filters

Circuit Type	Load side harmonics current (I_{ah})	Harmonic voltage (V_{ah})	Order of active filters
The load is a harmonic current source The active filter is a current source	$I_h Z_L/(Z_L+Z_S)$	$I_h Z_S Z_L/(Z_L+Z_S)$	$I_f=-I_h$
The load is a harmonic current source The active filter is a voltage source	$I_h Z_L/(Z_L+Z_S)$	$I_h Z_S Z_L/(Z_L+Z_S)$	$V_f=-I_h Z_f$
The load is a harmonic voltage source The active filter is a current source	$V_h/(Z_L+Z_S)$	$V_h Z_S/(Z_L+Z_S)$	$I_f=-V_h/Z_L$
The load is a harmonic voltage source The active filter is a voltage source	$V_h/(Z_L+Z_S)$	$V_h Z_S/(Z_L+Z_S)$	$V_f=-V_h Z_f/Z_L$

When the source harmonics are known, the active filter rating can be obtained directly according to Table 2.2 if the active filter is a harmonic current source. However, when the active filter is a voltage source, the actual rating of the active filter is dependent primarily on the level of harmonics to be removed and on the impedance of the active filter. If the active filter is in series with a passive filter, the impedance of the active filter is closely associated with the de-tuning degree of the passive filter. An important design issue is the selection of the correct "path impedance" described in section 2.1.1. If the capacitor C_f is very small (small MVar), the changing in capacitor size is also very small

so that no any detuning can be problematic. On the other hand, if the capacitor C_f had a large value (more MVar), detuning could affect the rating of the active filter largely. In this section, we will investigate the relationship between the active filter rating and the detuning of the passive filter. Let us use the circuit in case 2 studied in section 2.2 as an example. Figure 2.16 show the case circuit with $Z_L = \infty$ as in the case with HVDC converter.

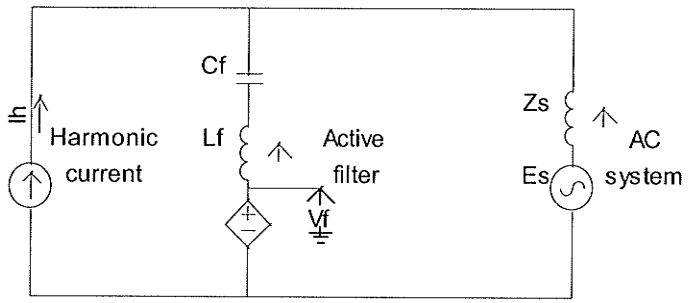


Figure 2.16 An example circuit

In Figure 2.16, we assume the source harmonic current I_h is known, which contains only 11^{th} harmonic current. The active filter is a voltage source, its magnitude is V_f. The path impedance consists of an inductance L_f and a capacitance C_f, which tuned as a passive filter for 11^{th} harmonic. The purpose of the active filter is to provide harmonic voltage compensation in case that the passive filter is de-tuned. If there is no de-tuning in the passive filter, the voltage output of the active filter is zero and the 11^{th} harmonic current will be removed by the passive filter alone. If there is de-tuning in the passive filter, the rating of the active filter is determined by its harmonic voltage output V_f. Besides, the fundamental current will flow through the active filter, so that this type of active filter should have a rating for fundamental current I_{f1}. These two ratings are not independent as will be shown. The relationship between the V_f and I_{f1} is analyzed as follows.

When there is no de-tuning, the fundamental frequency impedance Z_1 and the 11^{th} harmonic frequency impedance Z_{11} of the passive filter are

$$Z_1 = j\left(\omega L_f - \frac{1}{\omega C_f}\right) \tag{2.36}$$

$$Z_{11} = j\left(11\omega L_f - \frac{1}{11\omega C_f}\right) = 0 \tag{2.37}$$

Substitute the (2.37) in to (2.38), we get the magnitude of the fundamental impedance as

$$Z_1 = 120\omega L_f \tag{2.38}$$

Assuming the fundamental bus voltage is 1.0 per unit, the fundamental current rating of the active filter can be represented as

$$I_{f_1} = \frac{1}{120\omega L_f} \tag{2.39}$$

Now let us assume there is de-tuning on the passive filter, the C_f changes x percent to

$$C_f' = (1.0 - x\%)C_f \tag{2.40}$$

Then the magnitude of 11^{th} harmonic impedance of the passive filter will be

$$Z_{11} = 11\omega L_f - \frac{1}{11\omega C_f'} \tag{2.41}$$

The magnitude of active filter voltage output can be calculated as

$$V_f = Z_{11} \cdot I_h \tag{2.42}$$

Substitute (2.40) and (2.41) into (2.42) we get

$$V_f = \frac{x}{100 - x} \cdot 11\omega L_f \cdot I_h \tag{2.43}$$

For simplicity we assume that the 11th harmonic current to be removed $I_h=1.0$, then substitute (2.39) into (2.43), we obtain the relationship between the V_f and I_{f1} as

$$V_f = \frac{11x}{120 \cdot (100 - x) \cdot I_{f1}} \tag{2.44}$$

The relationship between the fundamental current rating I_{f1} and the harmonic voltage rating V_f can also be shown graphically in Figure 2.17. Figure 2.17 shows three curves with detuning level of 1%, 2% and 4%, or capacitor size changing of 2%, 4% and 8%. Figure 2.17 shows the lower the active filter fundamental current rating; the higher the active filter harmonic voltage rating. Thus the two ratings should be traded off when choosing active filters.

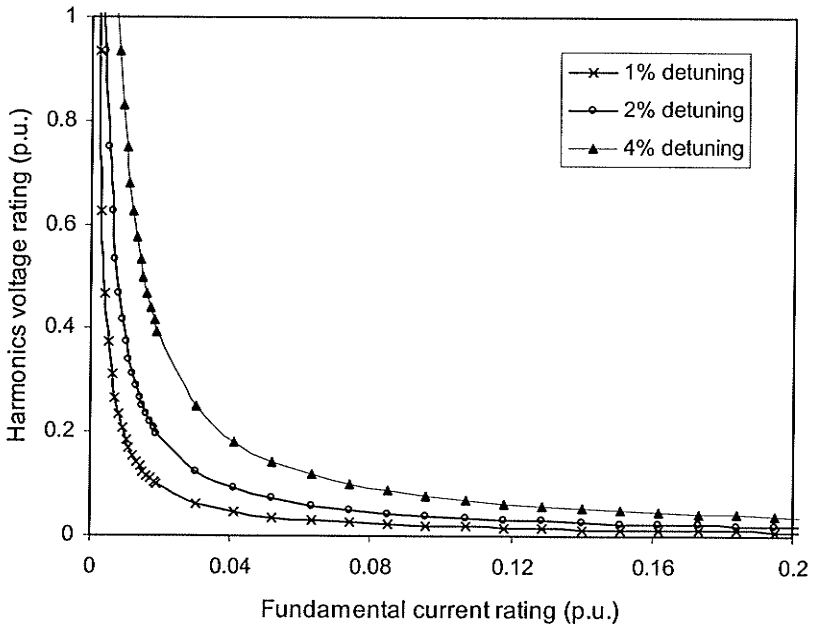


Figure 2.17 Relationship between fundamental current rating and harmonic voltage rating

2.5CONCLUSION

The ideal harmonics compensation has been studied in the chapter. Various types of harmonic source and active filter models are investigated using circuit theory. Based on the circuit analysis, the possible control signal measurements are discussed. The relationship between required ratings of active filters and the electrical system parameters are discussed.

The results of the theoretical investigation demonstrate that active filter can successfully remove the harmonics produced by any non-linear load. It also leads to some basic guidelines for how to choose control signals and how to estimate the rating of a required active filter.

--Chapter 3 --

STUDY OF IDEAL ACTIVE FILTER CONTROL

3.1 INTRODUCTION

In chapter 2, the mechanism of ideal active filers in removing the harmonics in the circuits has been explained. The next step will consider how to implement the control strategy of the active filter so that it can work properly and efficiently. This is the topic of this chapter.

3.2 TWO BASIC CONTROL APPROACHES

Let us use the test system diagram Figure 3.1 as an example. In Figure 3.1, the active filter is installed between the power source and the load that produces harmonics.

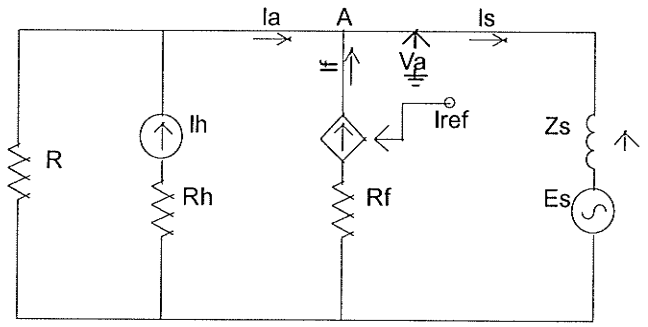


Figure 3.1 Example circuit

The parameters in Figure 3.1 are listed as follows:

Source side voltage source:

E_s=110KV, Frequency=60Hz, Inductance Z_s=0.05H

Load side harmonic current source:

I_{11}=0.15KA, Frequency=660Hz, Resistance R_h=0.01Ohm

Load:

R=100 Ohm

Active filter:

Controllable current source, Resistance R_f=0.01Ohm

As the active filter is modeled as a controlled ideal current source, a straightforward idea is to design a control algorithm based on current signals. Two basic control approaches are studied in this thesis. The first one is in the most straightforward way that uses active filter to cancel all the harmonic components in the load side current. A convenient way to find the fundamental component is to use a discrete Fourier transform (DFT). Subtracting the fundamental component from the total current measurement, the difference is the harmonic current, which we must cancel using the active filter. As in Figure 3.2, the harmonic components can be obtained by using DFT with the load current I_a as its input signal. The output signal of the DFT is the fundamental frequency component I_{a1} that is further subtracted by the total load side current I_a. Then we can get harmonic components I_{ah}, which needs to be removed. If we set the reference current of the active filter I_{ref} to be equal to this harmonic signal, based on the KCL, the current injecting to the system will be free of harmonics.

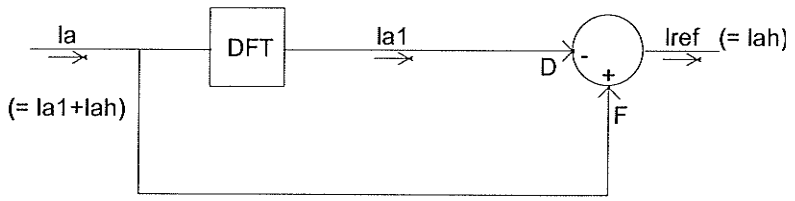


Figure 3.2 Control diagram of direct harmonics control

The other control method is to design a closed loop feedback control for the active filter to drive the harmonics in the system side current or voltage to zero. The proportional integral (PI) regulators or other regulators can be used in the control system design. In our example case the harmonic to be removed is the 11^{th} harmonic current. The DFT extracts the magnitude I_{s_11} and phase $phase\_11$ of 11^{th} harmonic current from the source side current I_s. The control system recalculates harmonic current into a real part and an imaginary part, each of which being controlled to zero by a PI controller. The outputs from the two PI controllers are converted back to time domain quantities and then added to form the current order I_{11_ref} of the active filter. This current will be the injecting current of the active filter I_f.

The control algorithm can be seen from the control system diagram as in Figure 3.3. Because of the feedback nature of the controller, by properly setting parameters of the PI controller, the delay in the system current measurement can be automatically compensated. If there are other harmonic components, for example, the n^{th} harmonic to be eliminated in the power system, a similar control system shown in the lower part of Figure 3.3 is used to calculate current order of the related n^{th} harmonic component. Finally all the harmonic current orders are added together to form the current order of the active filter.

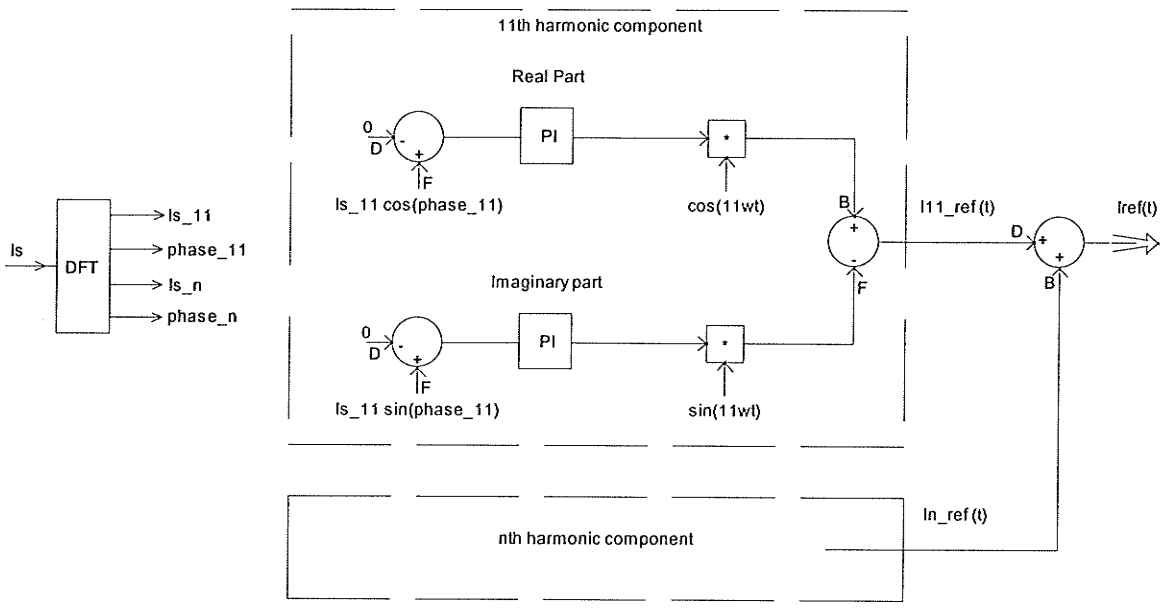
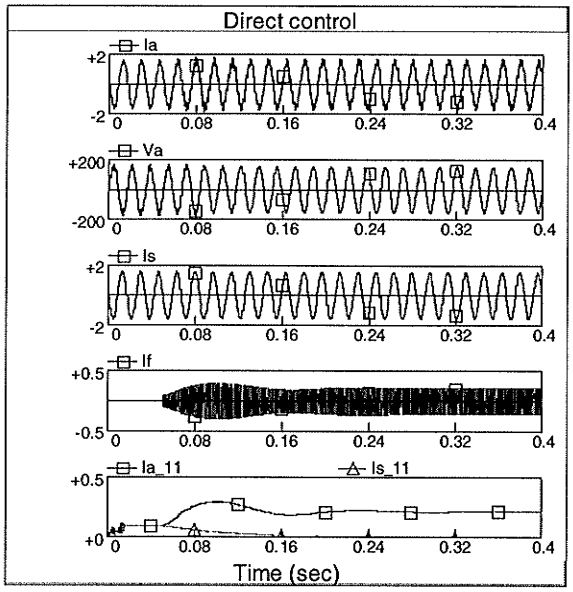


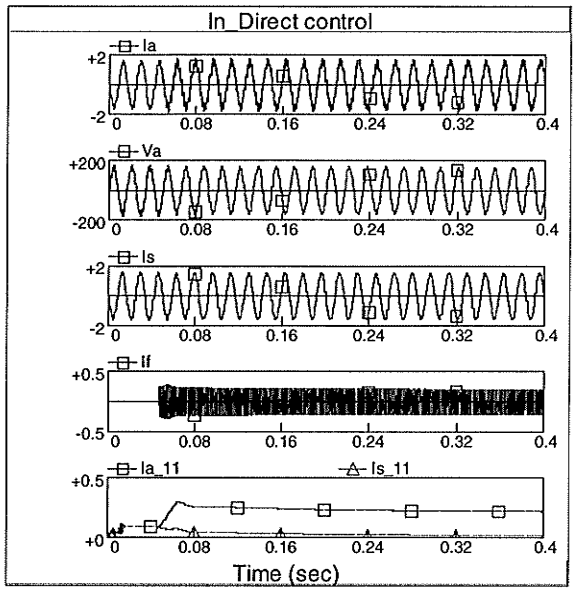
Figure 3.3 Control diagram of PI control

3.3 SIMULATION RESULTS OF THE TWO CONTROL APPROACHES

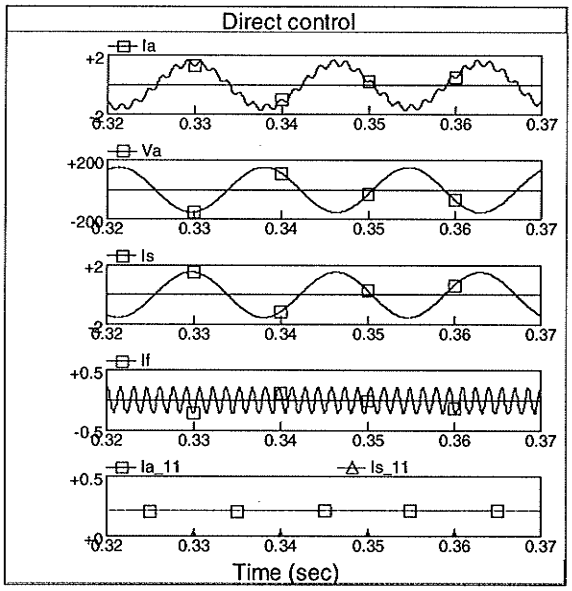
Both of these two control approaches are tested using simulation tool PSCAD/EMTDC to verify their performances. Some sample results are shown in the following figures. Firstly we assume there are no measurement errors and control system time delays in both control methods. A simulation time step of 1 microsecond is used to minimize simulation error. The maximum simulation induced delay is then 1 microsecond, which is very small compared to the period (1.03456ms) of highest simulated harmonic (order 11). In both cases, the active filter was turned on during run time in order to show the turning on transient. In the following figures, I_{a_11} donates the magnitude of 11^{th} load harmonic current and I_{s_11} denotes the magnitude of 11^{th} harmonic current remaining in the source side.



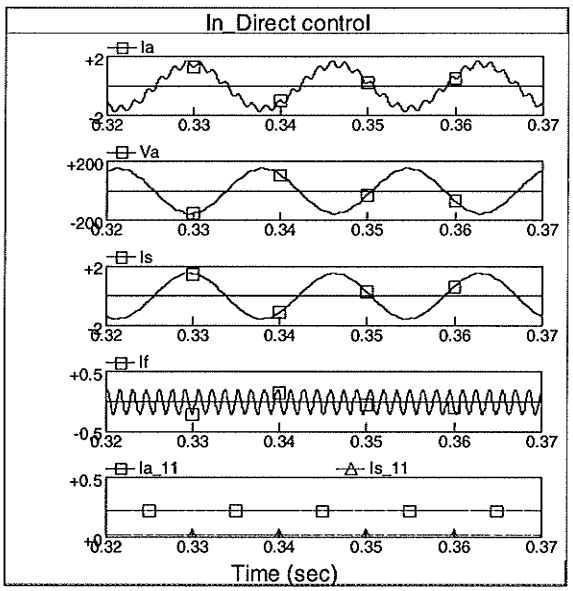
(a) Results of entire simulation time scope (direct)



(b) Results of entire simulation time scope (indirect)



(c) after transients (direct)



(d) after transients (indirect)

Figure 3.4 Simulation results of direct and PI harmonics control

Figure 3.4 shows the simulation results of the direct and the in-direct harmonics control. From Figure 3.4(a), we can see the magnitude of the harmonic current component in load side I_{a_11} becomes larger and the bus voltage V_a becomes smoother after turning on the active filter. This is because before turning on the active filter, some harmonic currents

can flow through load impedance R, which results in higher harmonic components in V_a. When the active filter is in use, all harmonic currents will go through the active filter branch. So I_{a_11} becomes higher and V_a becomes smoother. This may not clear from the actual voltage/current waveform, but the measured harmonic frequency magnitude in the bottom wave demonstrates this clearly. This confirmed what we got from Chapter 2 that load side currents increase after the active filter is connected.

From Figure 3.4(a) we also can observe that the active filter has a turning on transient period. Within this period, harmonic current cannot be filtered effectively. This period is about 0.1 second in this case. The length of the transient period depends on the system parameters. For instance the higher the system impedance, the longer the transient period. Figure 3.4(c) is the waveforms after transient, from which we can see the resultant source current I_s is in good sinusoidal. This indicates that the direct control method works well if there are no measurement error and control device time delay.

Figure 3.4(b) and (d) are the simulation results when indirect control method is used. We can see the indirect control approach with PI regulator also works well to remove the harmonic current in the circuit. In addition, the turning on transient of the indirect method as shown in Figure 3.4(b) decays much faster than that in the direct control as in Figure 3.4(a). However, active filters are mainly used to eliminate the harmonics in steady state, so that the turning on transient duration is not of a major concern. Generally, if the control circuit is ideal, the performances of the direct and the indirect methods are so close that the difference is hard to be observed.

3.4 COMPARISON OF THE DIRECT CONTROL AND THE INDIRECT CONTROL

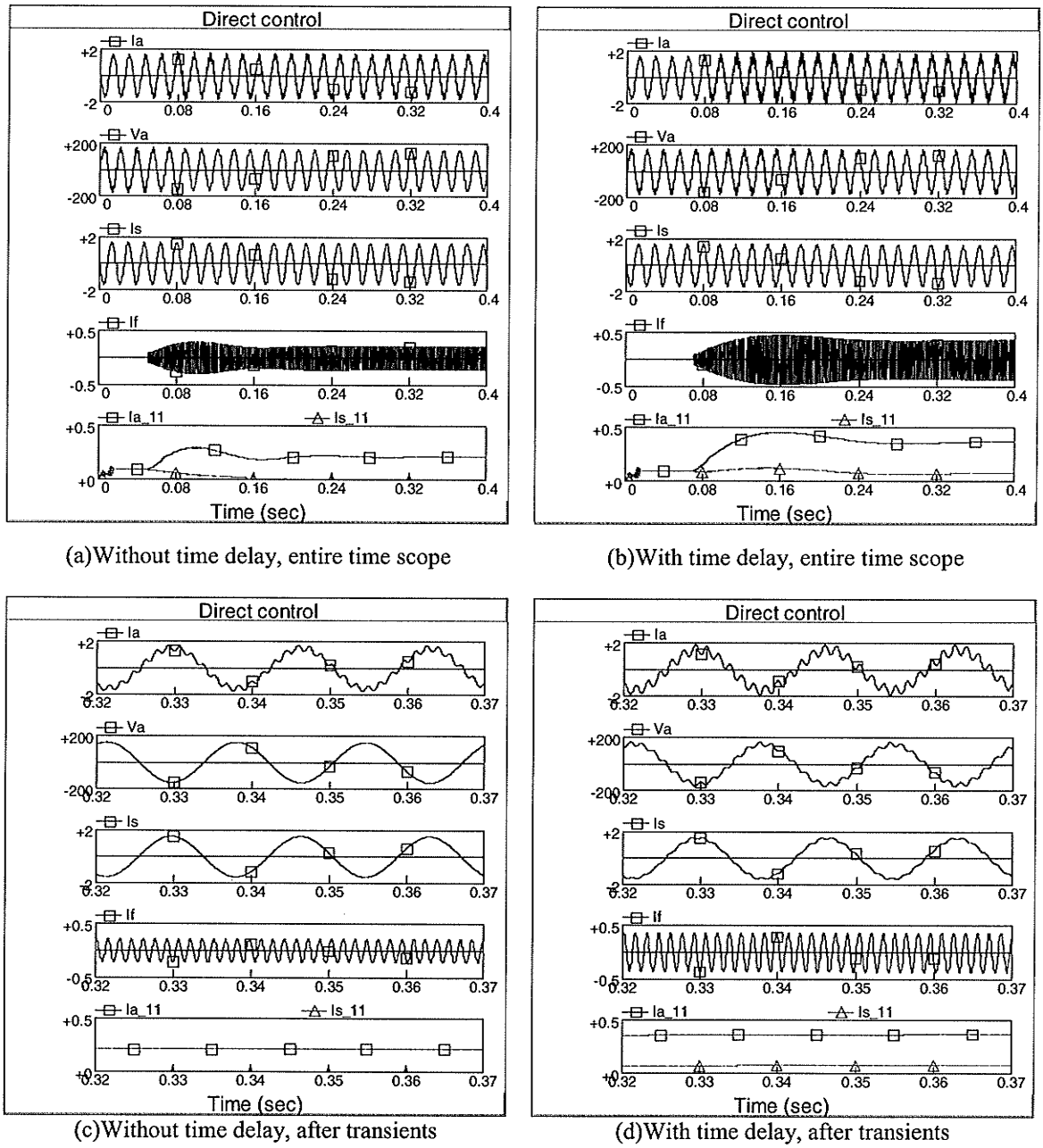
As we discussed in chapter 2, theoretically we are able to cancel all the harmonics directly if we give the active filter a proper reference value. However, this is not always true when the control elements are not ideal and have delays and tolerances. The phenomenon will be demonstrated in this section.

Let us assume a delay between the active filter injected current and its current order. Such a delay could arise because of the electronic hardware used to generate the current or due to the control circuit delay. A delay value of 50 microsecond is used in the following simulation studies.

Firstly we apply direct control approach as in section 3.3 to control the active filter. The simulation results are shown in Figure 3.5(a) and (c), which is fairly good. However, when we introduce 50 microsecond time delay in the control loop, the simulation results are totally different as in Figure 3.5 (b) and (d). By comparing the Figure 3.5(c) and Figure 3.5(d), we can observe that the filtering performance become worse when there is time delay in the control system. Besides, the rating of active filter will become much larger due to the time delay exists in the control system.

One the other hand, if we use the indirect control, the error due to delay of the control device can be avoided automatically. In the same case, the results of the indirect control is showed in Figure 3.6, which shows that the indirect control system can filter the harmonics very effectively although the delay exists in the control system. In the mean time, the time delay will not cause large increase of rating current of active filter. From this example we notice the indirect method with PI regulator is more forgiving and more

robust than the direct control, so that it is a better choice in designing the control system of an active filter.



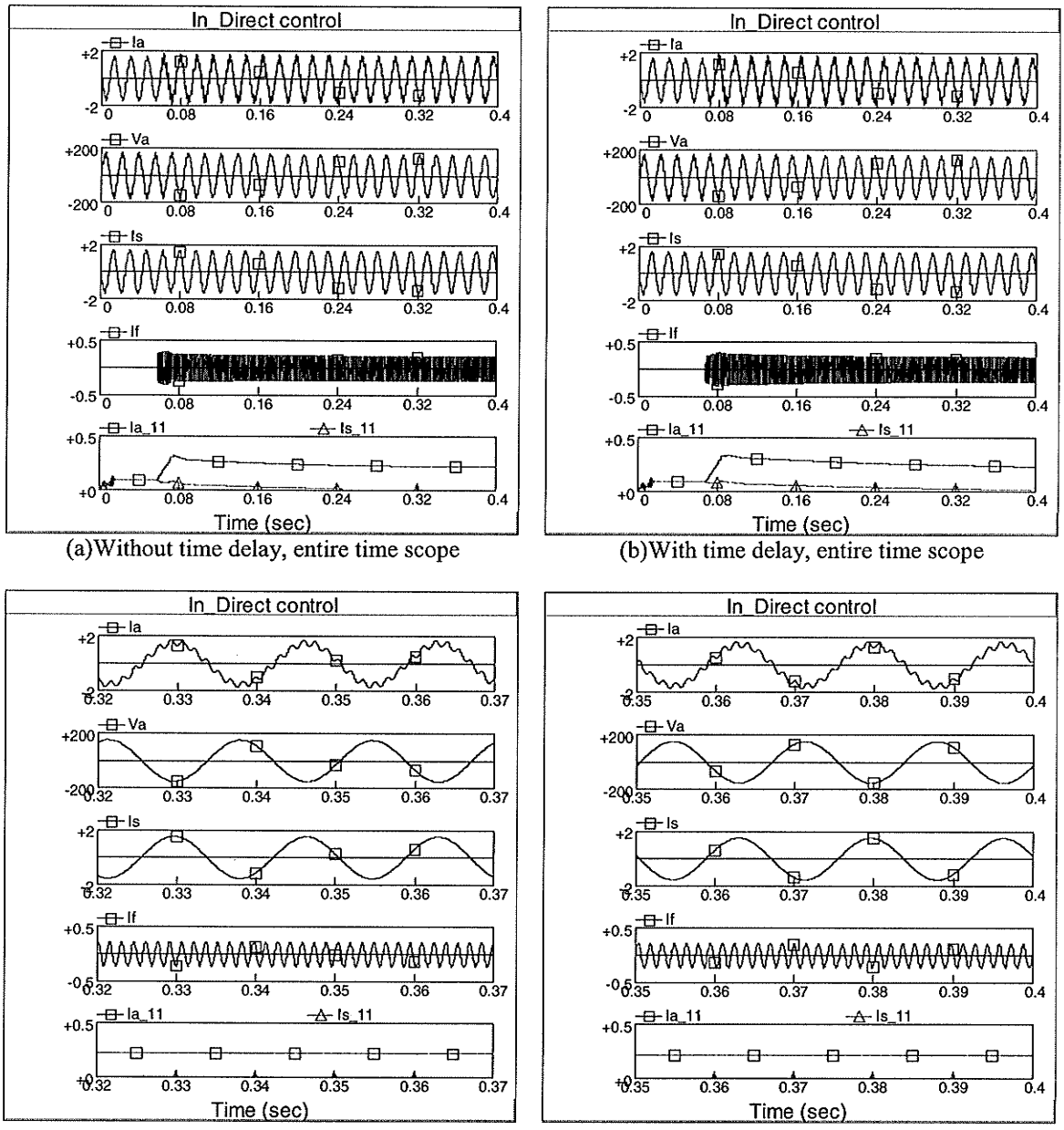
(a)Without time delay, entire time scope

(b)With time delay, entire time scope

(c)Without time delay, after transients

(d)With time delay, after transients

Figure 3.5 The effects of delay in the direct control system



(a)Without time delay, entire time scope

(b)With time delay, entire time scope

(c)Without time delay, after transients

(d)With time delay, after transients

Figure 3.6 The effects of delay in indirect PI control system

In order for the indirect method to work well, the control system parameters such as the P&I gains and the limits must be proper selected. Selecting the improper gains may result in highly oscillation and unstable response. Similarly the limits must be selected to

slightly higher than the active filter current rating so as to prevent overloading or chopping of the waveform.

We simulate the test case with different parameters of PI controllers. For the ideal active filter, the results show the control system is easy to tune to a stable point. While gain and time constant are fairly flexible to select in PI regulator, its output limits must be selected carefully. For the case in Figure 3.3, we selected the PI regulator output limits to be 0.22KA and –0.22KA respectively. This value should be set as close to the active filter rating. If the limits are either too large or too small, the PI controller will not work as expected. This case shows with PI controller, the active filter is more robust and withstands disturbances and noises. Thus, with appropriate parameters for the PI controller, the transient is almost gone and the filter current matches harmonic current almost at the very moment of switching on of the active filter.

The advantage of the direct control method is that it can cancel all the harmonics directly. It is very easy to implement as the control circuit is very simple. On the other hand, by using indirect control method, only selected order of harmonics can be eliminated. Every order of harmonic has to be reconstructed one by one. However, the real power system is far beyond ideal where parameter tolerance in both main circuit and in control system is inevitable. The direct current control of the active filter cannot compensate harmonics effectively when some noise and time delay in measurement and control occur. Therefore, the indirect control method seems to be more recommended due to its robustness. In fact, it is of critical significant to understand how the time delay affects the behavior of the direct control system of the active filter. This property will eventually

determine whether the direct control approach is able to be used in the real control system. This problem will be further investigated in next chapter.

3.5 CONCLUSION

1. DFT can be used to subtract harmonic components, by which the signal of the control order can be reconstructed.
2. Direct control approach does not work well in the real active filter system where tolerance of parameter and delay are inevitable. Indirect control with PI controller is more forgiven to the system tolerance. It is quite robust in the real active filter system.

--Chapter 4--

EFFECTS OF CONTROL CIRCUITS TIME DELAY ON THE PERFORMANCE OF DIRECT HARMONICS ELIMINATION

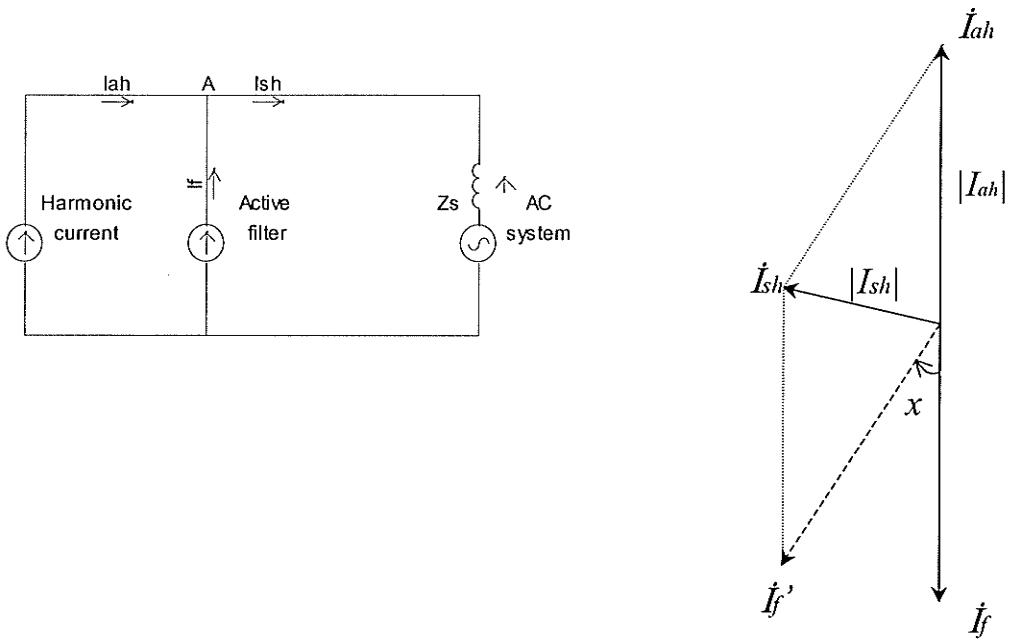
4.1 INTRODUCTION

Chapter 3 showed the negative impact of excessive delay on filtering performance of the direct controlled active filter through a simulation example. This chapter further investigates the impact of the delay on filtering performance of the direct control in detail, using mathematical analysis

4.2 THEORETICAL STUDY

The tolerance of ideal filtering due to the time delay in control circuits can be analyzed using the phasor diagram. In the harmonic equivalent circuit of Figure 4.1(a), we can draw the phasor diagram of the currents for the harmonic frequency at bus A in Figure 4.1(b). According to the KCL the harmonic current following into the system side I_{sh} is equal to the vector sum of the harmonic current I_{ah} from the load side and the current generated by the active filter I_f:

$$I_{ah} + I_f = I_{sh} \tag{4.1}$$



(a) Test circuit (b) Phasor diagram

Figure 4.1 The test circuit and the phasor diagram

The objective of the filtering is to prevent the harmonic current from flowing into the ac system. Hence the active filter current I_f should be the exact opposite the load side harmonic current I_{ah} as shown on the phasor diagram Figure 4.1(b), i.e., the magnitude of the I_{ah} and I_f are equal and the phase difference is 180°. Because of the control delays in measurement and/or implementation, the current I_f is not exactly in opposite to I_{ah} as shown by the dotted vector I_f' in Figure 4.1(b). In fact, I_f' is delayed by the angle x with respect to its desired value I_f. Hence, the resultant I_{sh} is no longer zero and so the filtering is sub-optimal. The tolerance of the filtering can be reflected by analyzing the relationship between I_{sh} and the time delay, or I_{sh} and the phase deviation of I_f.

In the phasor diagram Figure 4.1(b), we assume the magnitude of load harmonic current I_{ah} is $|I_{ah}|$, the phase deviation due to the delay is x, then the magnitude of resultant harmonic current in source side $|I_{sh}|$ can be calculated as (4.2) using trigonometry on

Figure 4.1(b).

$$|I_{sh}| = |I_{ah}| \cdot \sqrt{2 - 2\cos(x)} \tag{4.2}$$

We define y as the fraction of the total load harmonic current that enters the ac network or the harmonic current level entering to the ac network. If y=1, it means that all the load harmonic currents enter the ac system; y=0, it means that there are no harmonic currents enter the ac system. The relationship between y and x is given in (4.3) and shown graphically in Figure 4.2.

$$y = \frac{|I_{sh}|}{|I_{ah}|} = \sqrt{2 - 2\cos(x)} = 2 \cdot \sin\left(\frac{x}{2}\right) \tag{4.3}$$

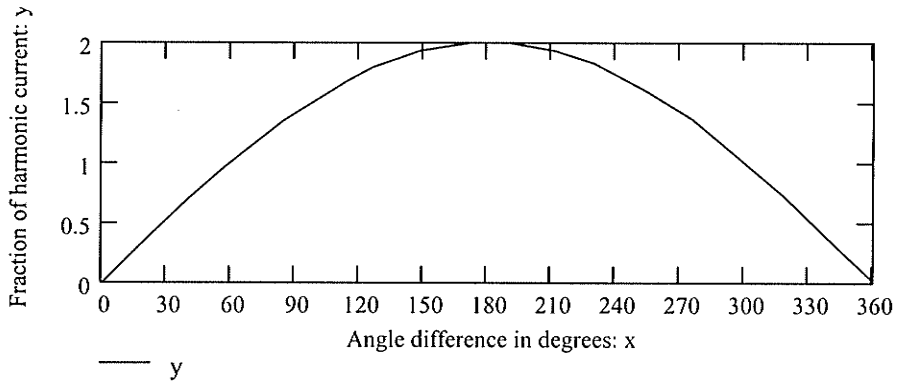


Figure 4.2 Relationship between tolerance and delay angle

Figure 4.2 demonstrates the remaining harmonic level in an ac system due to the delay angle x between I_f' and I_f. We can see when the delay angle is 0° or 360°, i.e., when the time delay is zero or exactly one cycle or integer multiple of the studied harmonic cycle, the harmonic will be fully removed. On the other hand, we see that when the angle deviation is between 60° and 300°, the harmonic level will become worse. The worst condition happens when the angle deviation is 180°, which leads to double the amount of

the harmonic current in the source side.

For example, for the 11th harmonic of 60 Hz system, the worst situation happens when the time delay τ is one half cycle of the 11th order harmonic (τ = ½*1/60*1/11 second = 757μs, or odd multiple of τ). In the same way, when the delay is between 60° (τ = 253μs) and 300° (τ = 1265μs), the harmonic will become worse after connecting the active filter.

One alternative way to represent the information in equation (4.3) is shown below. We derive the inverse function of (4.3) to get (4.4), where y is the harmonic current level entering to the ac network.

$$x(y) = \cos^{-1}\left(\frac{2-y^2}{2}\right) \tag{4.4}$$

$$x(0.1) = 5.732\,deg \tag{4.5}$$

Figure 4.3 shows a plot of the maximum allowable delays to limit the harmonic levels in the ac system below a certain level of "y". For example, if we wish to allow no more than 10% of a particular harmonic current order to enter the ac network, i.e., $y = 0.1$, the maximum allowable delay is 5.732° of this harmonic order. This is clear from Figure 4.4, which shows an enlargement of the area around the origin of Figure 4.3. In the meantime, we can conclude that the higher the harmonic order, the lower the allowable delay time. For instant, if we wish harmonic level in ac system no more than 10%, when the considered harmonic order is 11th harmonic current, the delay is no more than 24.11μs. The corresponding value for 13th harmonic current is 20.4μs.

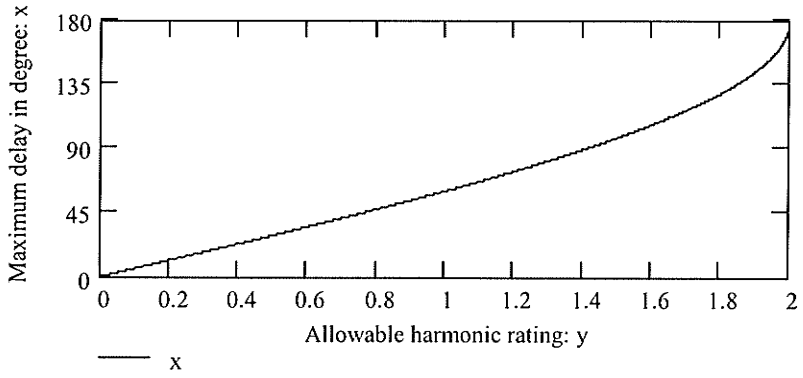


Figure 4.3 Maximum angle delay v.s. allowable harmonic rating

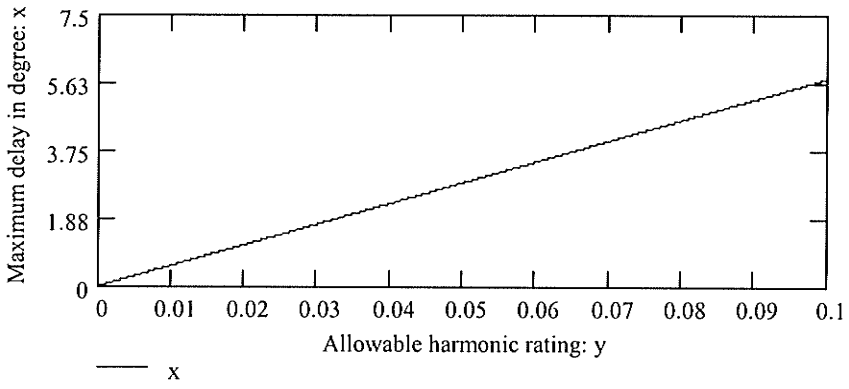


Figure 4.4 Enlargement of Figure 4.3

So far we can summarize the above analysis to the following conclusion:

Considering the N^{th} harmonic, and with fundamental frequency f, we desire to install an active filter to reduce this harmonic to the range of fraction or tolerance y, the delay time in second should be less than τ which is given in (4.6)

$$\tau = \frac{1}{2\pi Nf}\cos^{-1}\left(\frac{2-y^2}{2}\right) \tag{4.6}$$

Since the N^{th} harmonic cycle is $1/Nf$, if the delay τ_1 is larger than 60° with respect to the N^{th} harmonic. That is

$$\tau_1 \geq \frac{1}{6Nf} \tag{4.7}$$

The filter will increase the harmonic amount instead of reducing it. In the same way when the delay τ_2 is equal to 180°. Thus we have

$$\tau_2 = \frac{1}{2Nf} \tag{4.8}$$

The harmonic amount will become 2 times of that without filter. However when the time delay is larger than τ_2, the harmonic level starts to decrease and will reduce to zero when the time delay reaches 1 cycle of this harmonic frequency.

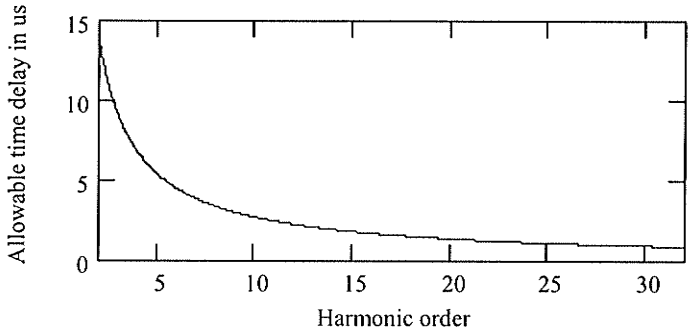
In order to show the relationship between the time delay and different harmonic order, we plot required delay time both in μs and in degrees in 60Hz system for keeping any given harmonic below 1% level as a function of the harmonic order. Equation (4.9) and (4.10) are used to plot Figure 4.5. Here we only plot harmonic orders up to the 30th. The limit of 30 is sufficient with respect to most power system applications. The higher frequencies are usually important if radio frequency interference is being considered.

$$\tau(N) = \frac{1000000}{2\pi Nf} \cos^{-1}\left(\frac{2-y^2}{2}\right) \tag{4.9}$$

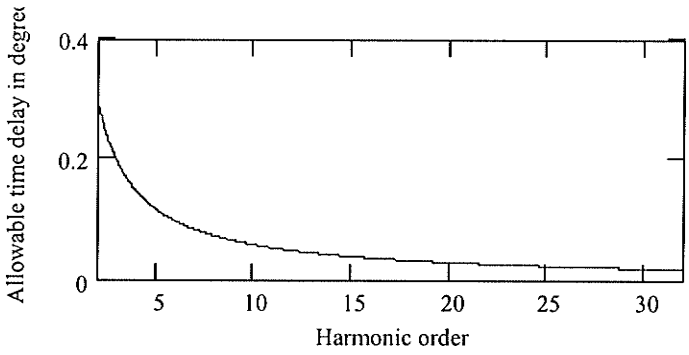
$$\tau_{deg}(N) = \frac{1}{N} \cos^{-1}\left(\frac{2-y^2}{2}\right) \tag{4.10}$$

As can be seen, it takes a much smaller delay time or angle to ensure adequate removal of the harmonic as the frequency increases. For example if the considered highest harmonic frequency is 13th, the time delay must be less than $\tau\,(13) = 2.04\mu s$ or $\tau_{deg}\,(13) = 0.044^o$ in 60 Hz system. Therefore, we can see the allowed time delay for keeping the required

level of harmonics in an ac network is so small that is not easily implemented in the real system. In theory, one could add additional delay to make the total time delay exactly 1 fundamental cycle. However, the tolerance would be limited to a very small range, i.e, $1/60s \pm 2.04\mu s$ if 13^{th} Harmonic is considered. Therefore, the performance of direct control is almost impossible to be achieved in an actual active filter system.



(a) Delay in time



(b) Delay in Angle

Figure 4.5 Permitted Delay v.s. harmonics order

When the load current contains more than one harmonic, the tolerance of each harmonic can be understood by the above analysis. One approach that can be considered is to set the time delay to a common multiple of all the harmonic cycles. The least common multiple is not easy to obtain, because the harmonic components in the load current can

vary at any time. But we do know that one fundamental cycle must be one of the common multiples. If the system operates in steady state, one fundamental cycle delay could be a possible solution to design the control circuits, however, as we discussed previously, the "one fundamental cycle" must be "exactly one fundamental cycle", which is not easily implemented in actual control system. In fact, in the case of several harmonics existing in the circuit, the maximum time delay should be calculated based on the Total demand distortion *(TDD)* that takes into account several harmonics simultaneously. Equation 4.9 can be used at each frequency to calculate TDD.

4.3 NUMERICAL SIMULATION TOWARDS IDEAL CURRENT SOURCE

4.3.1 Introduction

Time delay is inevitable in the control circuits of the active filter. The question is whether this time delay is excessive and degrades filter performance. We have answered the question theoretically in above section, now we confirm this approach via digital simulation.

The following three harmonic measuring indices are used to evaluate the performance of the active filter.

1. Individual harmonic distortion:

$$D_n = I_n / I_1 \tag{4.11}$$

Here I_n is the root-mean-square (r.m.s.) value of the nth harmonic and I_1 is the r.m.s. value of the fundamental current.

2. Arithmetic Sum of Harmonic Current:

$$D = \sum_{n} (I_n / I_1) \tag{4.12}$$

3. Total Demand Distortion (*TDD*): The ratio of the root-mean-square (r.m.s.) of the harmonic current to the r.m.s. values of the rated or maximum demand fundamental current.

$$TDD = \frac{\sqrt{\sum_{n=2,N} I_n^2}}{I_{rate}} \tag{4.13}$$

N is the number of harmonics in the measurement. In the following simulation study we will only consider 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonics.

Some typical interference limits used by modern utilities are presented below. However, each utility and scheme has its own particular values, which may differ from these typical values.

$$D_n < 1\%$$

$$D < 4\%$$

$$TDD < 2\%$$

We use PSCAD/EMTDC to simulate a simple circuit as in Figure 4.6. The time delay of the control system is varied and the performance of the harmonic elimination is monitored and assessed. We expect to confirm the results of section 4.2 by evaluating the harmonics flowing into source side under different time delay in the control system.

4.3.2 Simulation Study

In this section we will study three typical types of cases. In the first case we assume the

harmonic source contains only the 11^{th} harmonic component. In the second case the harmonic source is assumed to contain two harmonic components, 11^{th} and 13^{th} harmonics. The third case deals with the general circumstance, in which the harmonic source is square waveform, containing all odd harmonics. Our purpose is to observe the filtering performance while varying the time delay. The simulation is conducted on PSCAD/EMTDC.

A simulation time step of $1\mu s$ is used to minimize simulation error. The maximum simulation induced delay is then $1\mu s$, which is very small compared to the periods of simulated harmonics, so that the time delay induced by EMTDC algorithm is negligible. In order to see the effects of delay on the harmonic elimination, we use delay function in CSMF of master library in PSCAD/EMTDC to introduce the different delays.

Case 1. The harmonic source contains only 11^{th} harmonic

The system configuration is shown in Figure 4.6. The parameters in Figure 4.6 are listed as follows:

Source side voltage source: E_s=*132.79KV, Freguency=60Hz, Inductance* Z_s=*0.01H*

Load side harmonic current source: I_{11}=*0.12KA, Frequency=660Hz, R=100 Ohm*

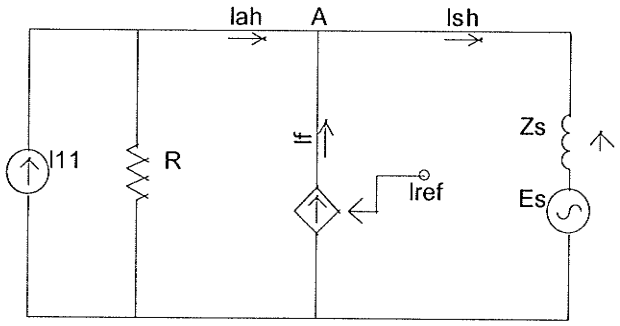


Figure 4.6 Circuit diagram of case 1

Figure 4.7 shows the relationship between the time delay and the harmonic current level

entering to the ac system. The value y is the fraction of the total load harmonic current that enters the ac network. y is calculated from following equation as described in above section

$$y=I_{s11}/I_{a11} \tag{4.14}$$

where I_{s11} and I_{a11} are source side and load side 11^{th} harmonic current respectively. Delay in Figure 4.7 is expressed in the range of 11^{th} harmonic period. This figure confirms what we got in the previous section that the harmonic level in source side will increase as the delay increases, will be equal to load side harmonic if delay is 60° and will reach double the value of the load side harmonic if delay is 180°. It is expected that the trends in Figure 4.7 will periodically appear 11 times per fundamental frequency cycle. The results are plotted in Figure 4.8.

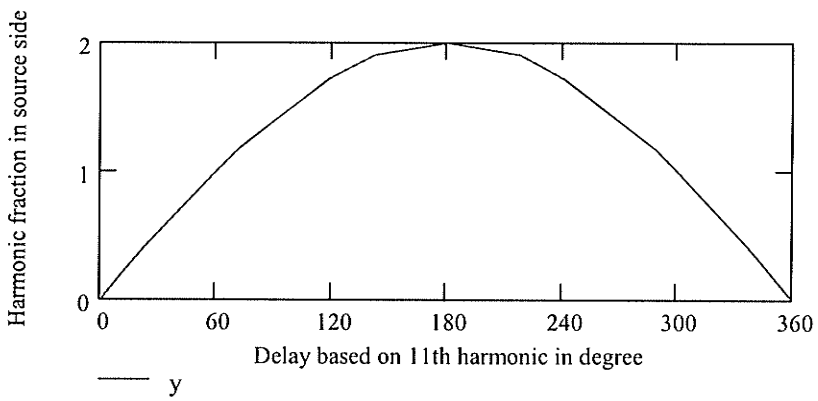


Figure 4.7 Relationship between the harmonic fraction in source side and the time delay

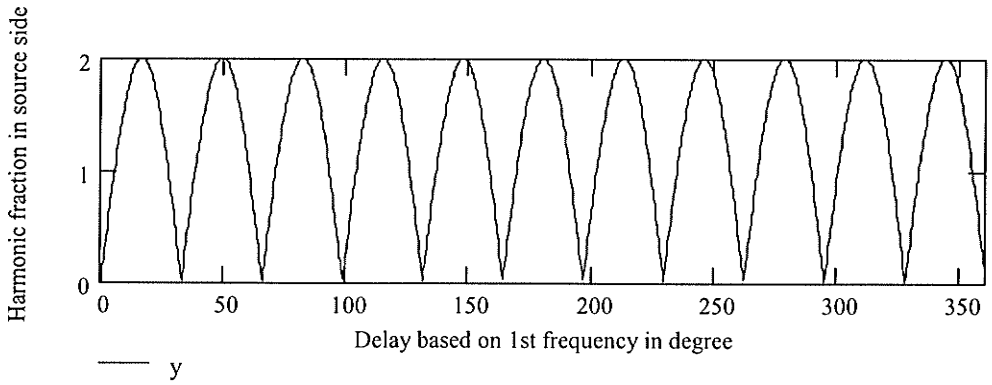


Figure 4.8 Relationship between the harmonic fraction in source side and the time delay in 1 cycle

We also plot the relationship between the delay (degree based on 11th harmonic period) and the individual harmonic distortion. Here D_{11} is the individual harmonic distortion introduced in the section 4.3.1 and is given by

$$D_{11}=I_{s11}/I_{s1} \tag{4.15}$$

where I_{s11} is the remaining 11th harmonic current in source side and I_{s1} is the fundamental current in source side.

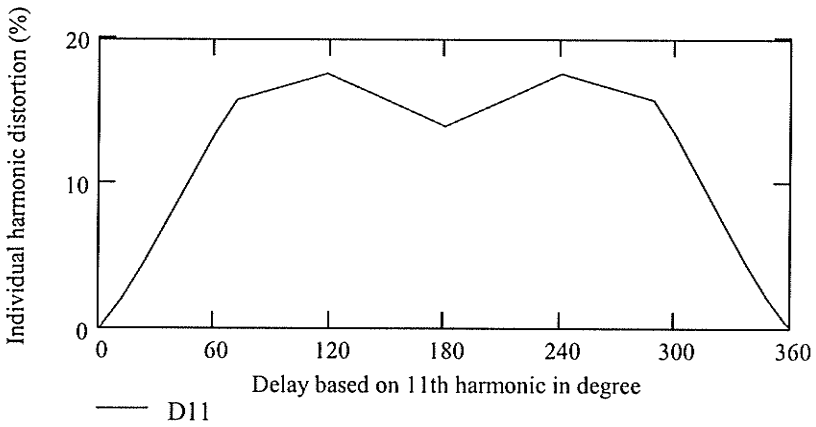


Figure 4.9 Relationship between the individual harmonic distortion and time delay

Comparing the curves in Figure 4.9 and Figure 4.7, we can see the curve shapes are different. Theoretically, when delay is half cycle of individual harmonic period, the

source side harmonic current level would be the double of load side harmonic current, which is the maximum value in the Figure 4.7. However, a maximum value for y does not necessaryly mean I_{s11} is maxmium, because I_{a11} is not a constant. Figure 4.7 is based on Equation 4.15, whereas Figure 4.9 is based on Equation 4.14, which has a different demenator.

From Figure 4.7 and Figure 4.8, we can see the performance of the filter reaches optimum when the time delay is the integer multiples of the 11th harmonic cycle. This result indicates if we apply a time delay at certain time, the high quality filtering is possible to achieve. However, in order to achieve higher quality filtering, the permitted time delay is restricted in a very small range. For instance, the typical value of the individual harmonic distortion is less than 1%, the correponding permitted delay time in Figure 4.9 is very close to the origin. In fact almost all entire curve except the very small region around the origin and the point of 360° do not satisfy the typical value of 1%.

Case 2. The harmonic source contains only 11th and 13th harmonics

The system configuration is shown in Figure 4.10. The parameters in Figure 4.10 are the same as those in case 1 except the load side harmonic current source contains two harmonics simultaneously with 13th harmonic current source magnitude as I_{13}=0.1KA.

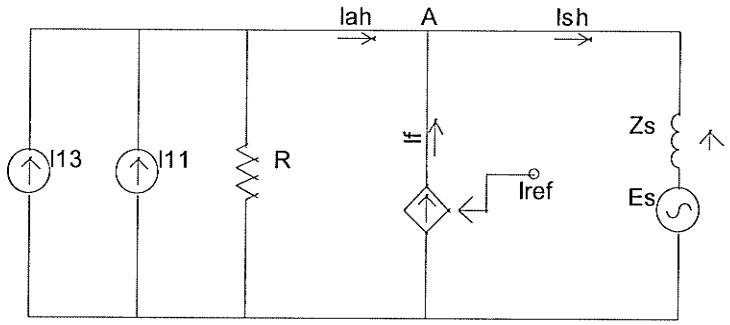


Figure 4.10 Circuit diagram of case 2

Figure 4.11 shows the relationship between the time delay and the remaining harmonic level at the system side, in which the fraction of the total load harmonic current entering the ac system y can be calculated with the following equation

$$y = \frac{\sqrt{I_{s11}{}^2 + I_{s13}{}^2}}{\sqrt{I_{a11}{}^2 + I_{a13}{}^2}} \tag{4.16}$$

In Figure 4.11, delay is in electrical degree of fundamental frequency. From Figure 4.11 we can see the curve does not reach zero at any cycle point of either the 11th harmonic or 13th harmonic other than at the fundamental cycle point. This indicates to us that, if we would specify any time delay, one fundamental cycle is a good option. In addition, the curve does not repeat either 11 or 13 times in one fundamental cycle.

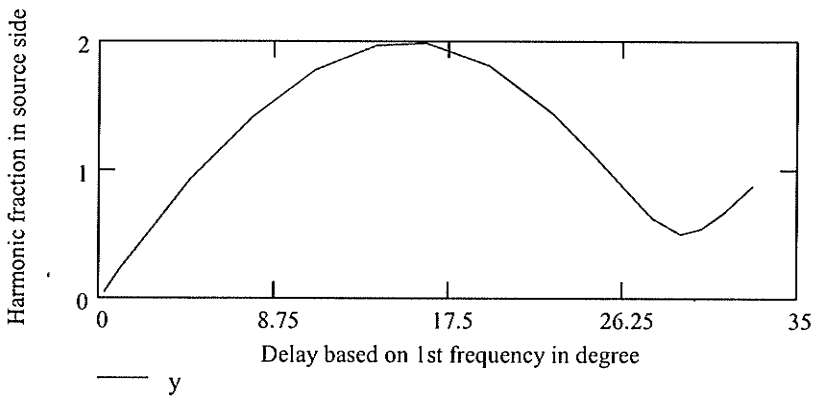


Figure 4.11 Relationship between the system side harmonic and the time delay in case 2

Equation (4.17) represents the relationship between the delay and Arithmetic Sum of harmonic current. This relationship can also be illustrated graphically as shown in Figure 4.12.

$$D=I_{s11}/I_{s1}+I_{s13}/I_{s1} \tag{4.17}$$

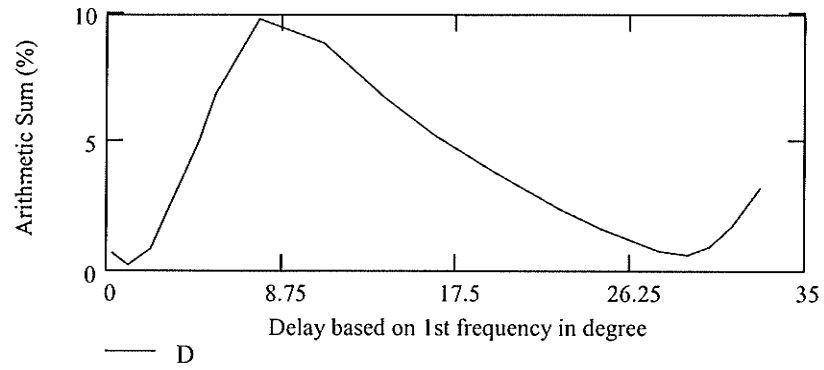


Figure 4.12 Relationship between the Arithmetic Sum of harmonic current and delay

Similarly, equation (4.18) represents the relationship between delay and the total demand distortion. Again, the same relationship can be demonstrated as shown in Figure 4.13.

$$TDD = \frac{\sqrt{I_{s11}^{\ 2} + I_{s13}^{\ 2}}}{I_{s1}} \tag{4.18}$$

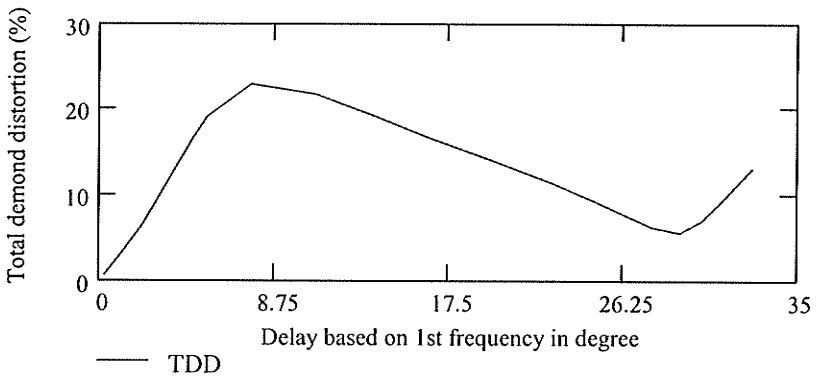


Figure 4.13 Relationship between the TDD in Is and time delay

Figure 4.12 and 4.13 confirmed that the harmonic level does not reach zero at any cycle point of either the 11^{th} harmonic or 13^{th} harmonic other than at the fundamental cycle point. It is indicated that, if there are more than one harmonics in the system, we have to limit the time delay strictly to exact one fundamental cycle. Any deviation of the time delay from the exact one or multiple fundamental cycle will significantly degrade the

performance of the active filter. In fact, in order to satisfy those harmonic indices, the permitted time delay is far too smaller than what we can achieve in actual active filter systems.

Case 3. The harmonic source is a square waveform

The purpose to use a square waveform current sorce as the harmonic source is because many power electronic loads (i.e., dc converter) exhibt this waveform. The spectrum of a sequare wave contains all odd harmonic orders with decreasing magnitude as the harmonic order increases.

The system configuration is shown in Figure 4.14. The parameters in Figure 4.14 are the same as those in case 1 except the load side harmonic current source is replaced by a square waveform current source with its magnitude to be 1.0KA.

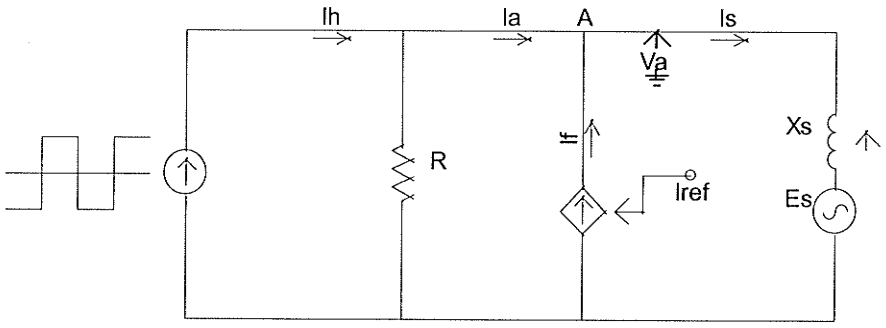


Figure 4.14 Circuit diagram of case 3

Some simulation results are shown in Figure 4.15. We can see the effects of time delay on the performance of active filters varied with the orders of the filtering harmonic. If the delay time is proportional to a certain harmonic cycle, this order of harmonic will be eliminated; if the delay time is an odd number multiple of half cycle of one harmonic, the active filter will result doubling this harmonic in source side. Figure 4.15 shows the harmonics level when the time delay of control systems varies from 50μs-5500μs. The

harmonic level without filter is also plotted in the same figure for comparison. It can be seen that with the time delay, the active filter degrades the filtering performance for some orders of harmonics.

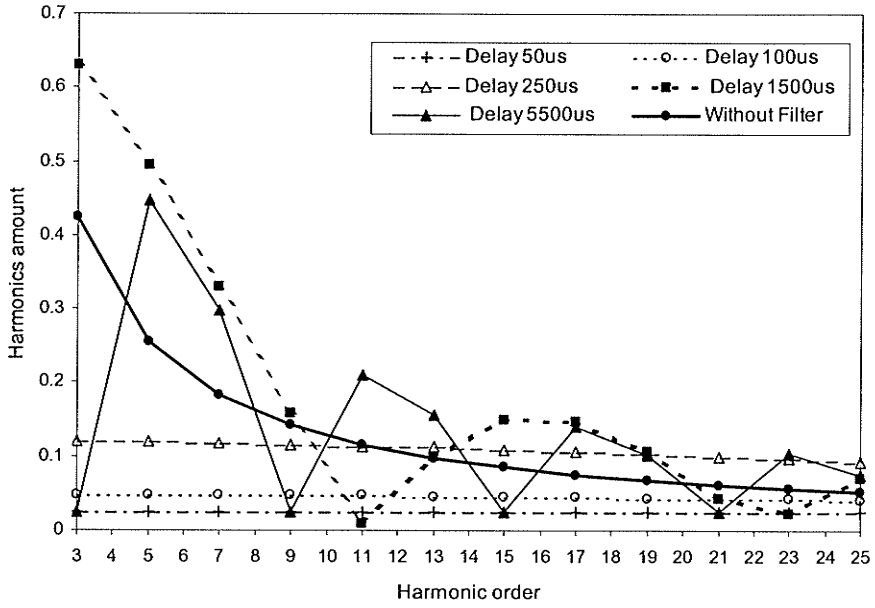


Figure 4.15 Relationship between the harmonics in I_s and time delay

The relationship between TDD and time delay is plotted in Figure 4.16. Here we consider the harmonics up to the 25th order and plot up to *1/3* cycle of fundamental frequency. We know at 1/3 of fundamental cycle delay, the 3rd harmonic and other 3N order harmonics no longer exist. Since the 3rd harmonic is the highest harmonic in square wave current source, we can expect 1/3 and/or 2/3 cycle delay give lower TDD in one fundamental cycle. Figure 4.16 shows how TDD changes along with the time delay. The TDD is about 13% at 1/3 cycle, which is much higher than permitted level, so that it is not necessary to do more simulation beyond 1/3 cycle. The curve should increase after 1/3 cycle delay and decrease to about same level as 1/3 cycle delay when delay time is 2/3 of fundamental cycle. Finally, at one fundamental cycle delay the curve should reach zero again.

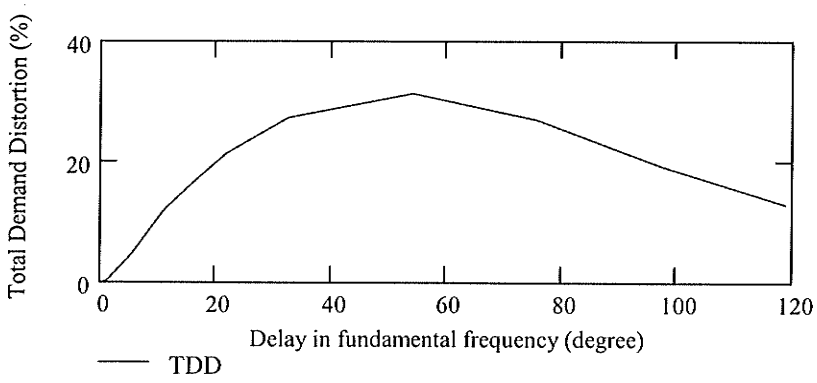


Figure 4.16 Relationship between the TDD in I_s and time delay in 1/3 cycle

From this result we can see the permitted time delay is very small if we need to satisfy the TDD ≤ 2% requirement. Although theoretically it would be possible to achieve high performance with direct harmonics elimination if we make the time delay of the control circuit to exactly one fundamental cycle, it is really difficult to achieve in the real world.

4.4 NUMERICAL STUDIES OF THE ACTIVE FILTER USING A DETAILED REPRESENTATION OF THE POWER ELECTRONIC CIRCUIT

4.4.1 Introduction

In the previous sections, the effects of control circuit time delay to the performance of direct harmonic elimination has been investigated in the circuit where an active filter is represented by an ideal current source. In this part, the study is extended to the electrical system in which the active filter is modeled using detail electronic circuit.

The main circuit of the simulation case is shown in Figure 4.17. The source is modeled using a simple three-phase 200 V, 50 Hz source. The harmonic load is modeled by a six-phase converter bridge of rating 20kVA, in which the dominant harmonics are the 5^{th} and

the 7th. This is a very common type of rectifier load used in power distribution system. The active filter is modeled as a voltage source inverter parallel connected to the main circuit via a 20 kVA, Y-Y transformer. The circuit of active filter is shown in Figure 4.18.

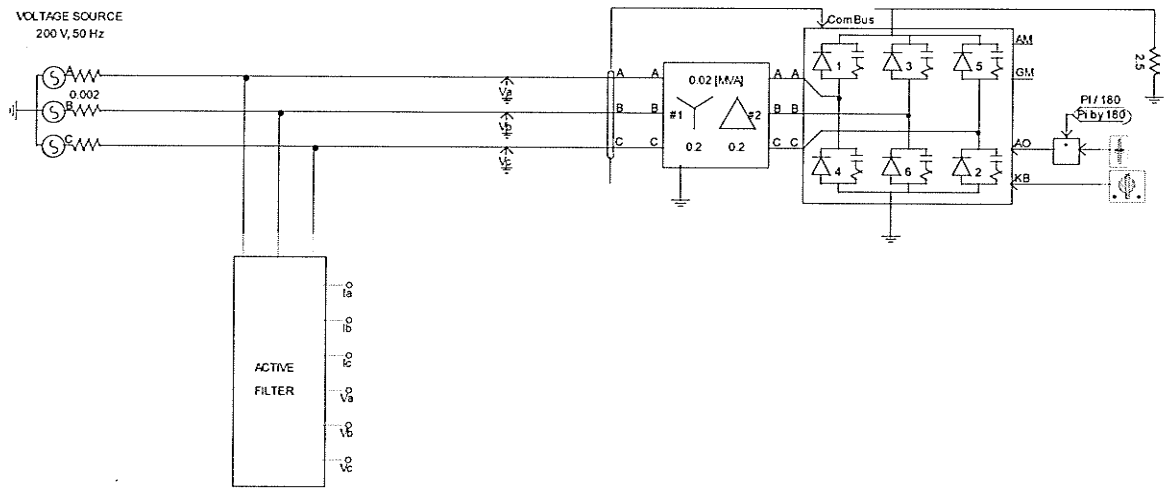


Figure 4.17 Main circuit of the simulation case

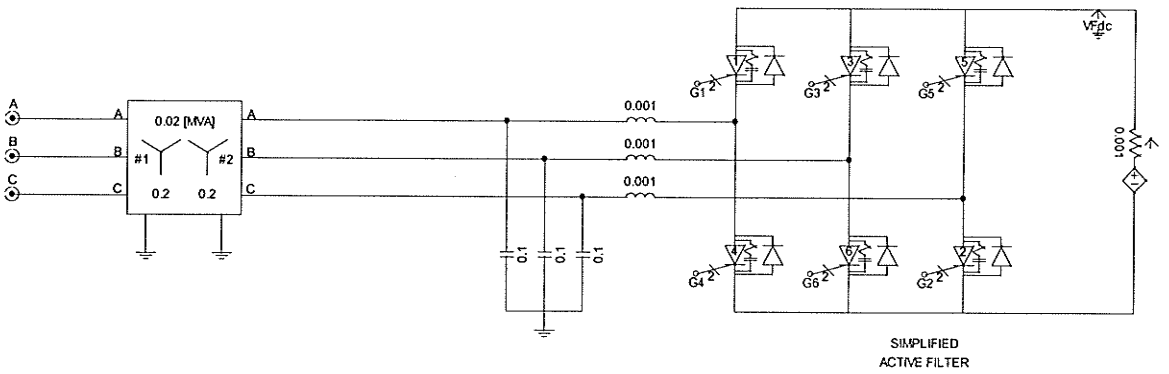


Figure 4.18 Circuit of active filter

The purpose of a small-rated LC filter is to suppress high frequency switching ripples generated by the active filter. In order to simplify the control, the dc source of the active filter is a constant dc voltage source in this case. We did not separate DC source into two

in this case which indicates this configuration only works with positive /negative sequence of harmonics and not with the zero sequence.

4.4.2 Control strategy

The objective of the direct control of an active filter is to use the active filter to cancel the entire harmonic component in the load side current. The control system is shown in Figure 4.19 and Figure 4.20. As described in chapter 3, Figure 4.19 shows that the harmonic components can be obtained by using DFT with the load current I_a as its input signal. The output signal of the DFT is the fundamental frequency component I_{a1}. The total harmonic currents can be obtained by subtracting I_{a1} from the total load side current I_a, which is referred as the phase A injection current order I_{aref} of the active filter in Figure 4.19. Control for phase B and C are identical. The delay function in Figure 4.19 is used to model control system delay. By setting different parameters, different control system delays can be introduced to the system. Here we assume all the delays are the same for three phases and the system is balanced. Current referenced PWM (CRPWM) is used to control the output current of the active filter, in which the error between the actual harmonic current order and the active filter injection current is forced to remain within the pre-specified tolerance band by controlling the inverter switches. This control method is described in chapter 2 and again is shown in Figure 4.20.

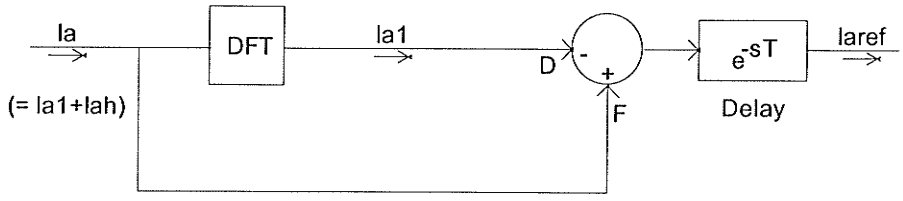


Figure 4.19 Direct control for current order

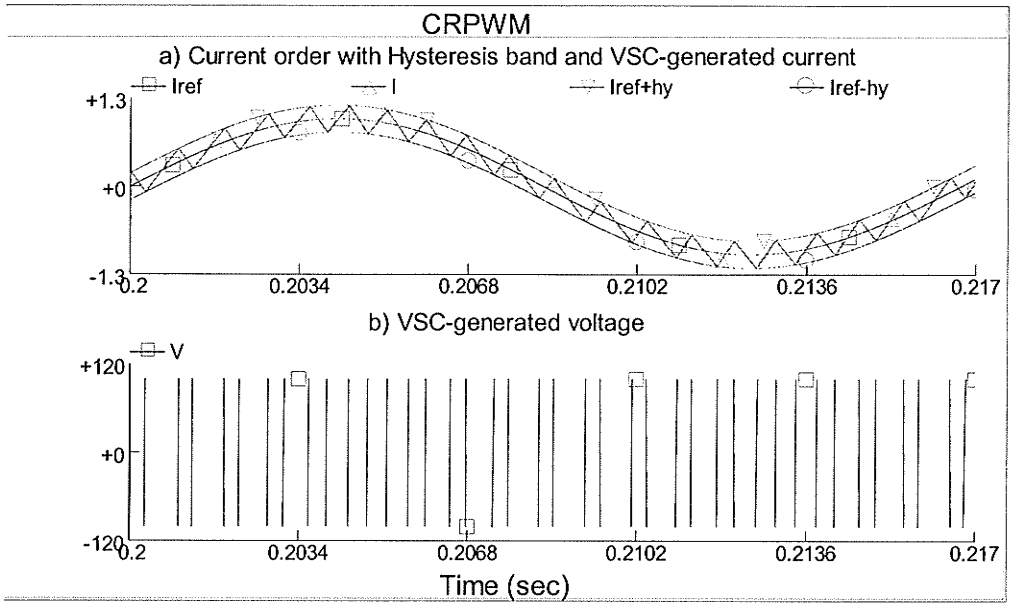


Figure 4.20 CRPWM control

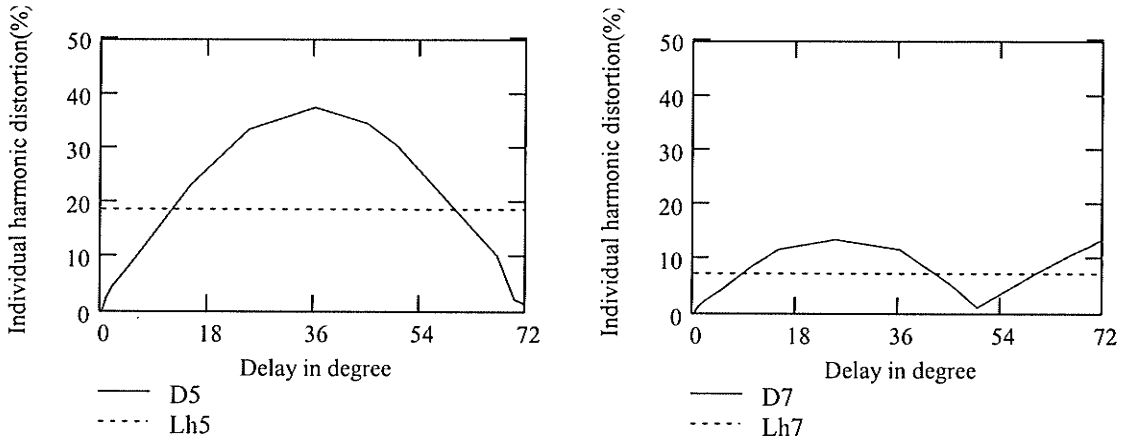
4.4.3 Simulation results and analysis

4.4.3.1 Individual harmonic distortion

Figure 4.21 is the relationship of delay (in degree) and individual harmonic distortion (in percentage). D_5 and D_7 are the individual harmonic distortion for the 5th and the 7th harmonics in source side; Lh_5 and Lh_7 are the original individual harmonic distortion for the 5th and the 7th harmonics in load side, which are exactly the original harmonic levels of the both harmonics before the active filter is connected. The waveforms will repeat 5 times for the 5th harmonic and 7 times for the 7th harmonic.

The intersection of D_5 and Lh_5 is about 12° which means when the delay is greater than 60° under the 5th harmonic period, the harmonic will become worse after turning on the active filter. The worst situation would be delaying 36° in fundamental or 180° in the 5th harmonic cycle. The harmonic in source side will be double instead of being eliminated. This result is also applied to the 7th harmonic period. The intersection of D_7 and Lh_7 is

about 8.5° in fundamental cycle or 60° in the 7th harmonic cycle. The worst situation is 25.7° in fundamental cycle or 180° in the 7th harmonic cycle.



(a) 5th harmonic (b) 7th harmonic

Figure 4.21 Relationship of delay and individual harmonic distortion

4.4.3.2 Arithmetic Sum of Harmonic Current

Figure 4.22 is the relationship of delay (degree) and arithmetic sum. *D* is arithmetic sum in source side and *Lh* is arithmetic sum in load side, which is original arithmetic sum before active filter is connected. We just consider the 5th, 7th, 11th, 13th harmonics in this study.

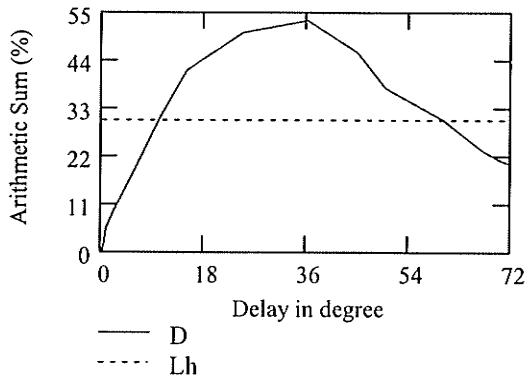


Figure 4.22 Relationship of delay and arithmetic sum

4.4.3.3 Total Demand Distortion

Figure 4.23 is the relationship of delay (degree) and the total demand distortion *TDD* (%), where *TDD* is the total demand distortion in source side and L_{tdd} is total demand distortion in load side before active filter applied.

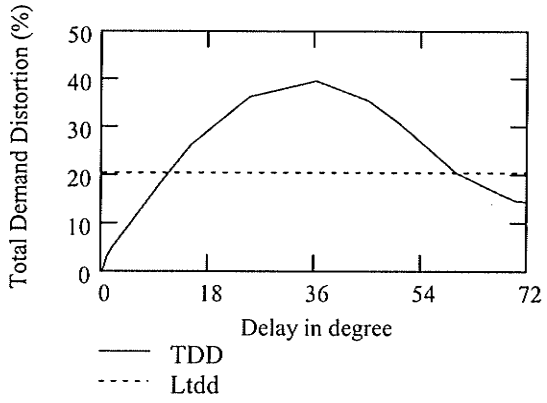


Figure 4.23 relationships of delay and total demand distortion

Table 4.1 lists the simulation results when time delay is 1°. None of these results can meet the requirement of typical limits listed in section **4.3.1**. This again emphasizes that the permitted time delay is very small in order to meet the requirement of harmonic indices.

Table 4.1 Comparison of the simulation results and the typical harmonic limits

Indices		Simulation Result when delay is 1° (%)	Typical Limits (%)
Individual Harmonic Distortion (D_n)	D_5	2.083	1.0
	D_7	1.085	
	D_{11}	1.062	
	D_{13}	1.042	
Arithmetic Sum (D)		5.208	4.0
Total Demand Distortion (TDD)		2.756	2.0

4.5 CONCLUSION

In section **4.2**, the theoretical analysis shows that the performance of the active filter depends on the delay time. If the delay time is an integer multiple of one harmonic cycle, this order of harmonic will be eliminated; if the delay time is an odd number multiple of a half harmonic cycle, the control signal will be opposite to this particular harmonic, which results doubling the harmonic in the source side. The only way to eliminate all the harmonics is to let the delay time to be a common multiple of the harmonic cycles, such as one fundamental cycle, ensuring the control signal is identical to the harmonics in the load side current. We also give the relationship of the distortion tolerance and the delay time. The permitted delay time is very tiny typically of the order of 10 μs or about 0.2° of the fundamental frequency.

In section **4.3**, simulation studies are conducted to verify the effect of time delay on the performance of the active filter. Three types of harmonic sources are tested in the circuit: a single harmonic source, a source with 2 simultaneous harmonic sources and a square waveform source. This section confirms the theoretical study in section **4.2**. Finally, in section **4.4**, an actual active filter topology is used to eliminate harmonics from a fully modeled six-bridge rectifier load. The results confirm what we get from sections **4.2** and **4.3**.

Above investigation shows that, even though theoretically exactly one or more fundamental cycle delay could ensure all the harmonics being eliminated, it is very difficult to be implemented in an actual system. The permitted delay time is so small that any small interference will cause large deviation of the filtering results. This intolerant

property of the direct harmonics elimination will significantly reduce the reliability of the directly controlled active filter and eventually restrict its application in the real active filter system.

--Chapter 5--

SIMULATION STUDY OF AN INDIRECT CONTROLLED ACTIVE FILTER IN A REALISTIC OPERATING ENVIRONMENT

5.1 INTRODUCTION

In the previous chapters, we have discussed the ideal harmonics filtering and the control approaches of the active filter. The purpose of previous work is to provide a preparation for designing the control systems of actual active filters. It is concluded in the previous chapters that the indirect control approach such as PI control is more appropriate than the direct control approach in designing the control systems for active filters. In this chapter, the indirect method of control is applied to an active filter, which is modeled to clean up the harmonic pollution from a full wave diode rectifier – a common load in electrical distribution systems. Current referenced PWM (CRPWM) control is applied to realize the current order by controlling the firing angle of the voltage source converter (VSC).

5.2 VSC WITH CRPWM CONTROL

5.2.1 System configuration

We use the same rectifier load simulation case as in chapter 4. The main circuit is shown in Figure 5.1. The circuit of the active filter is also shown in Figure 5.2 for convenience.

Firstly we consider the dc source of the active filter as a constant dc voltage source. In the next section we will investigate replacing the dc voltage source with a capacitor, which is more economical.

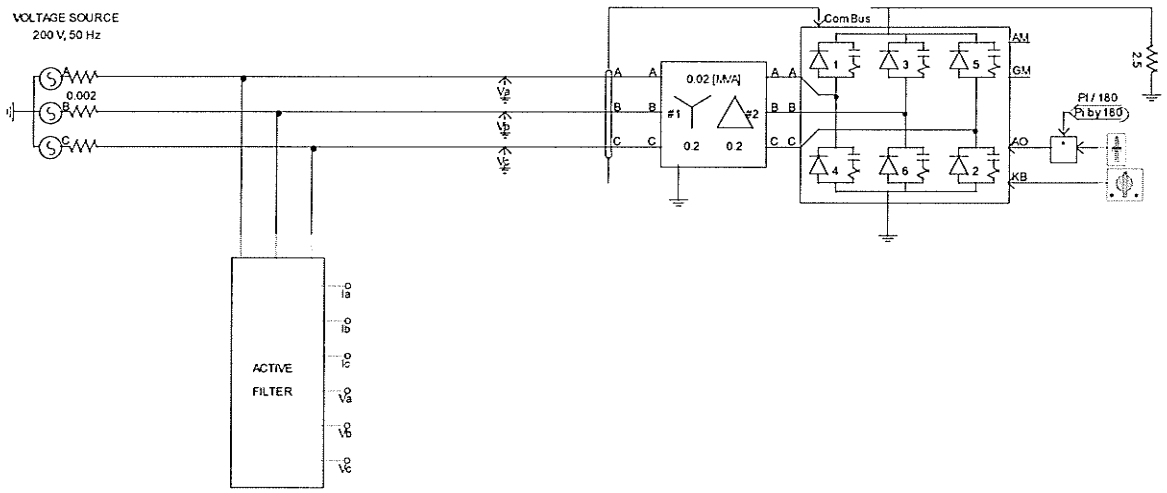


Figure 5.1 Main circuit of the simulation case

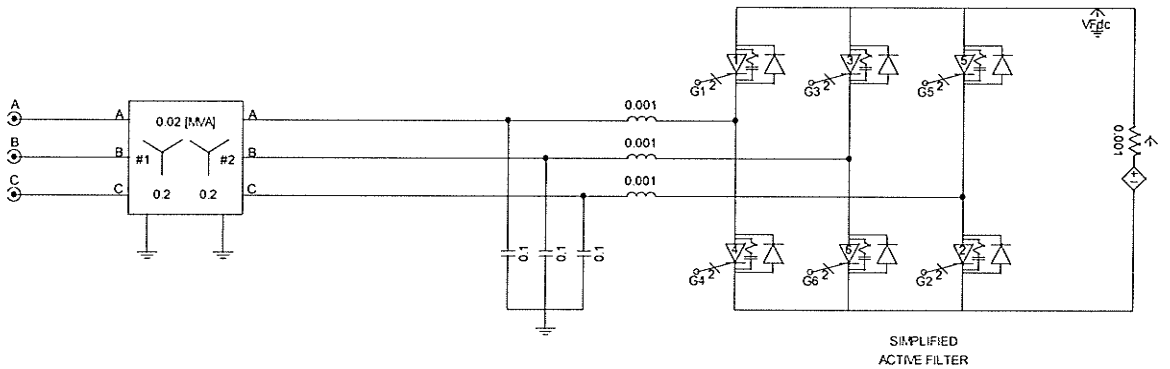


Figure 5.2 Circuit of active filter

5.2.2 Control strategy

The control system is shown in Figure 5.3 and Figure 5.4. The indirect control method was introduced in chapter 3. As we know, because of the feedback nature of the PI controller, the delay in the control system and the error in current measurement are automatically compensated. The dominant harmonic current components of the six-pulse rectifier load are the 5^{th} and the 7^{th}. Figure 5.3 shows the indirect control method to generate the active filter current order. Similar control system is used to calculate the current order for the 5^{th} and the 7^{th} harmonic currents. Then the current orders are added together to form the total active filter current order. Figure 5.4 shows the CRPWM control strategy, which forces the error between the active filter current order and injection current to remain within the pre-specified tolerance band by controlling the inverter switches. CRPWM is described in chapter 2.

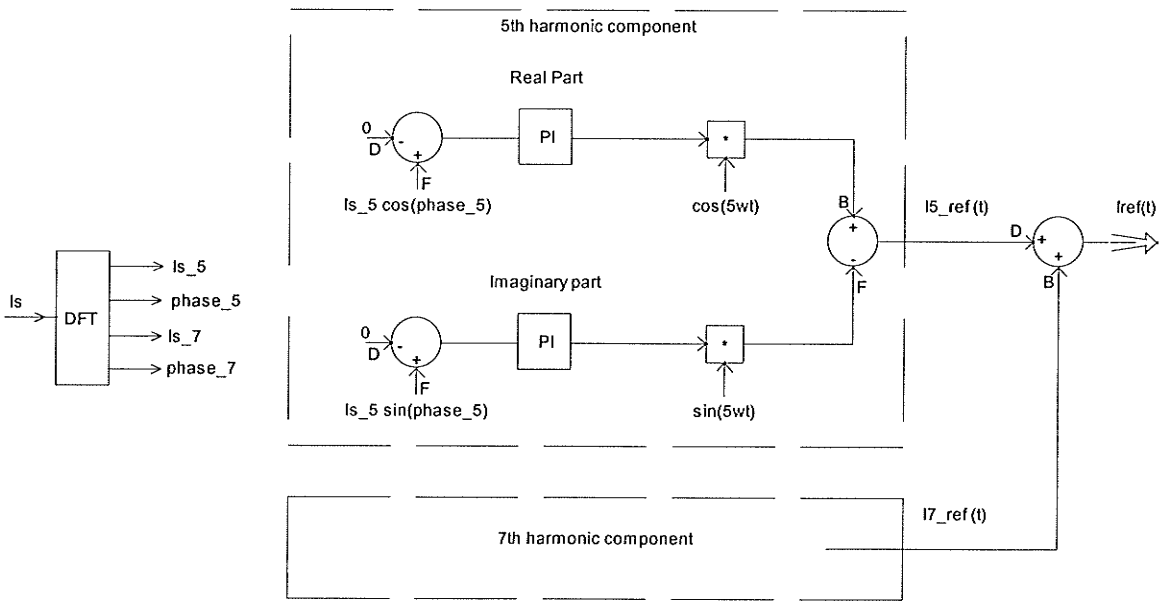


Figure 5.3 Indirect control loop for current order

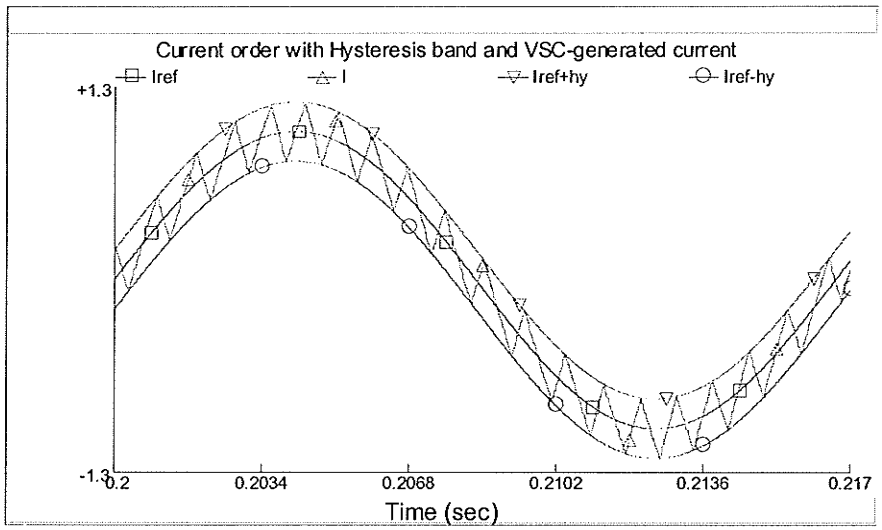


Figure 5.4 CRPWM control

5.2.3 Simulation results

The phase reference used in discrete Fourier transform (DFT) as well as the signal reconstruction can be obtained using a phase locked loop (PLL). The Figure 5.5(a) below is the simulation results without PLL, while Figure 5.5 (b) is the result with PLL. The approach of considering frequency dynamics can improve the accuracy when the system has frequency fluctuations. We can see that both the results, with and without PLL are acceptable in this particular case. However we expect the application of PLL increase the robustness of the control system as the frequency in the source would have some small fluctuation.

We also tested the indirect control method when different delays are applied in the control system as we have done in the same case with direct control method in Chapter 4. Figure 5.6 is the results when 200μs delay is applied in the signal measurements. Simulation results showed that with indirect control method, the delay is automatically compensated and will not introduce error to the system.

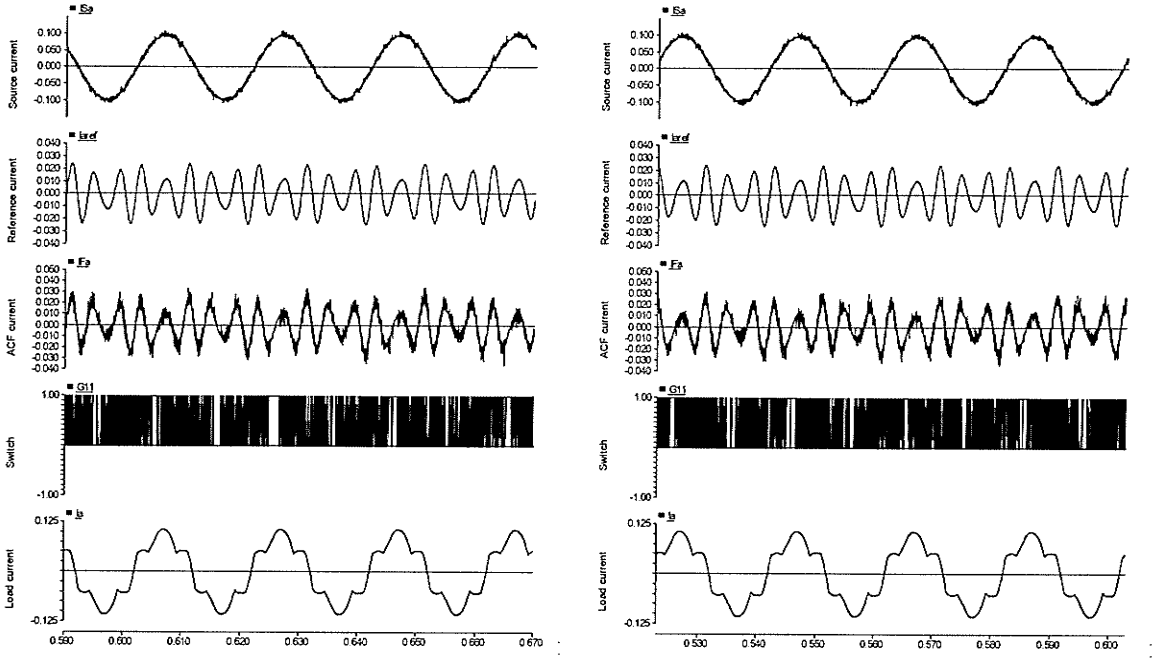


Figure 5.5 Simulation results of without and with PLL

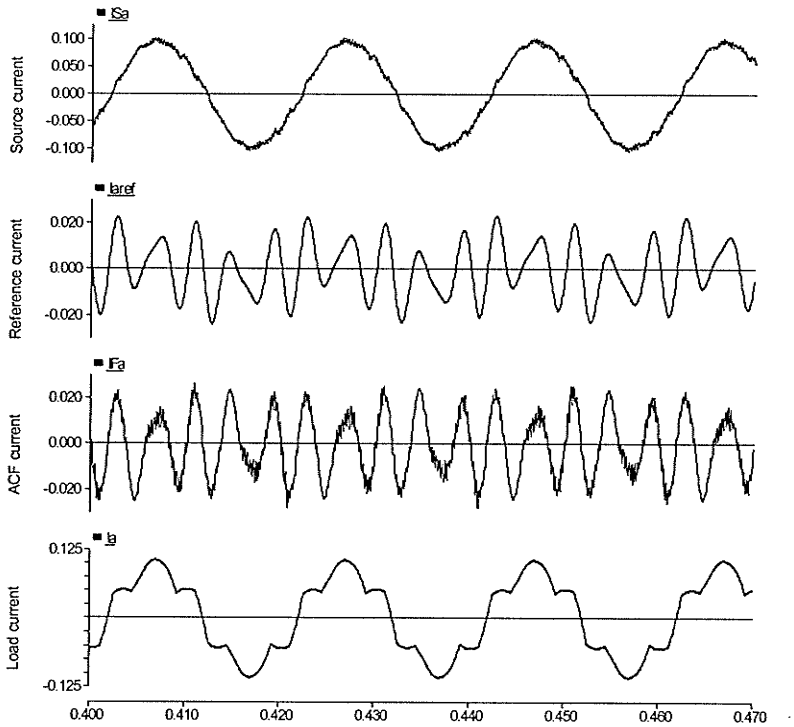


Figure 5.6 Simulation results with 200μs control delay

In Figure 5.5 and 5.6, *Isa* and *Ia* are the phase A source side current and the non-linear load side current respectively. *Iaref* is the reference current reconstructed from indirect PI controller in phase A, and *IFa* is the active filter current injection. G11 is switch pattern. A hysteresis width of 0.002KA for current referenced PWM is set in this case.

5.2.4 Consideration of replacing constant DC source with a capacitor

In this section, we investigate the performance of proposed control system when the constant dc source in the active filter circuit is replaced by a capacitor that is more economical. In order to control dc capacitor voltage so as not to exceed its limit, an appropriate dc voltage control needs to be implemented.

As we know, with voltage reference controlled PWM in a STATCOM, the direct voltage of capacitor is directly or indirectly controlled. The dc capacitor voltage can be increased by momentarily changing the firing reference to make the Voltage Sourced Converter behave as a rectifier, thereby transferring energy from the ac-side onto the dc capacitor. Similarly, by a transitory inverter-mode operation, the capacitor voltage can be reduced. This signal is required to modify the angle between the system voltage and the voltage generated by STATCOM. This shift angle determines the direction and amount of real power flow through STATCOM.

However, when we use current reference controlled PWM, the reference signal is directly obtained from source side current, which contains only harmonic components. This reference current thus cannot be used to adjust DC capacitor voltage. In order to regulate dc voltage and avoid exceed the limit; the dc capacitor voltage does need to be controlled. As we know, the charging and discharging of the dc capacitor should be realized by fundamental current flowing into the active filter with in phase or opposite phase to

fundamental voltage. In this section, we modified the active filter reference current by adding a fundamental signal. This signal is in phase with fundamental frequency voltage. The magnitude of this signal is obtained from a dc voltage regulator. When dc voltage is different from dc voltage set point, the modulation signal is used to reconstruct a current reference, which is in phase with fundamental voltage signal and then added to harmonic components current reference. The magnitude of the output voltage of the active filter is proportional to the dc capacitor voltage. The rating of the dc capacitor is decided by the injecting harmonic current components and system voltage.

Figure 5.7 shows the regulated DC capacitor voltage and the corresponding modulation index *mod*. The *mod* is then used to add one fundamental frequency current signal to active current order in order to regulate the dc capacitor voltage. This fundamental frequency current is in phase with fundamental frequency voltage of the ac bus.

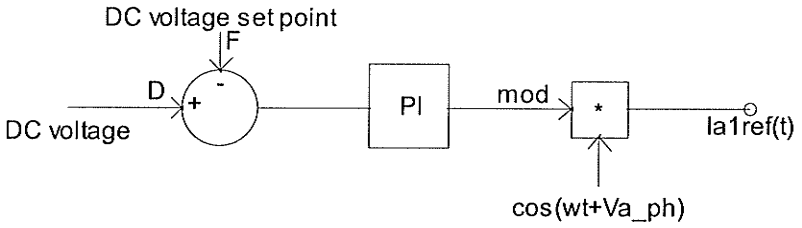


Figure 5.7 DC voltage controller

In the following simulation, we replace the dc source with a 500μF capacitor. It is shown in Figure 5.8 that the proposed control system works well when the dc voltage source is replaced by the capacitor. Figure 5.9 shows the regulated DC capacitor voltage and the corresponding modulation index.

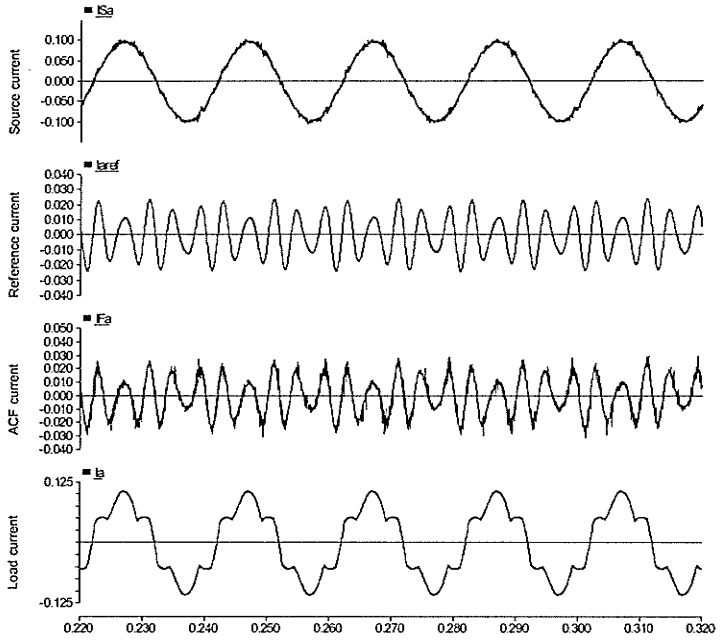


Figure 5.8 Simulation results with dc capacitor

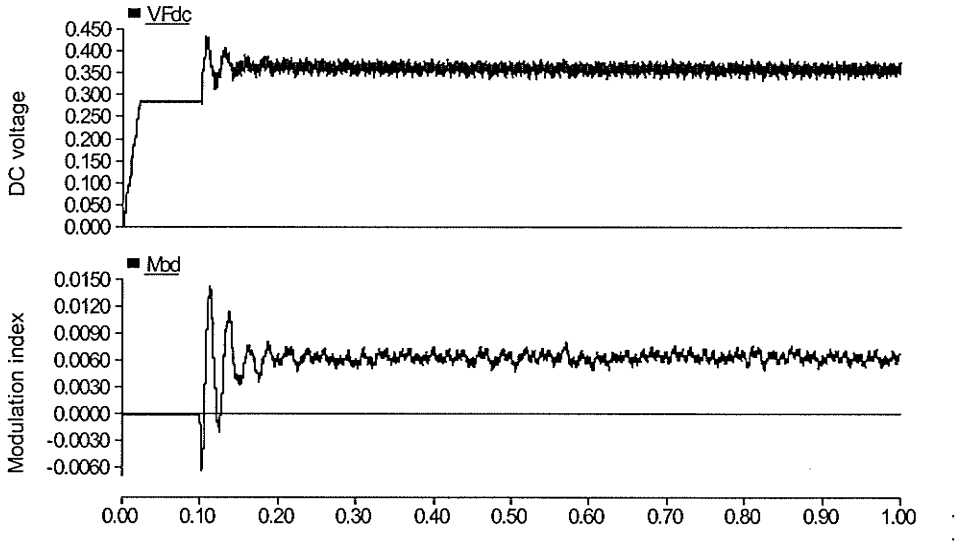


Figure 5.9 DC capacitor voltage and modulation index

Figure 5.10 and 5.11 is the simulation results when changing dc bus load from 2.5Ω to 1Ω during runtime. We can see the dc capacitor voltage keeps constant with the dc

voltage control. The current produced by the active filter contains fundamental frequency component, which is used to charge and discharge the dc capacitor.

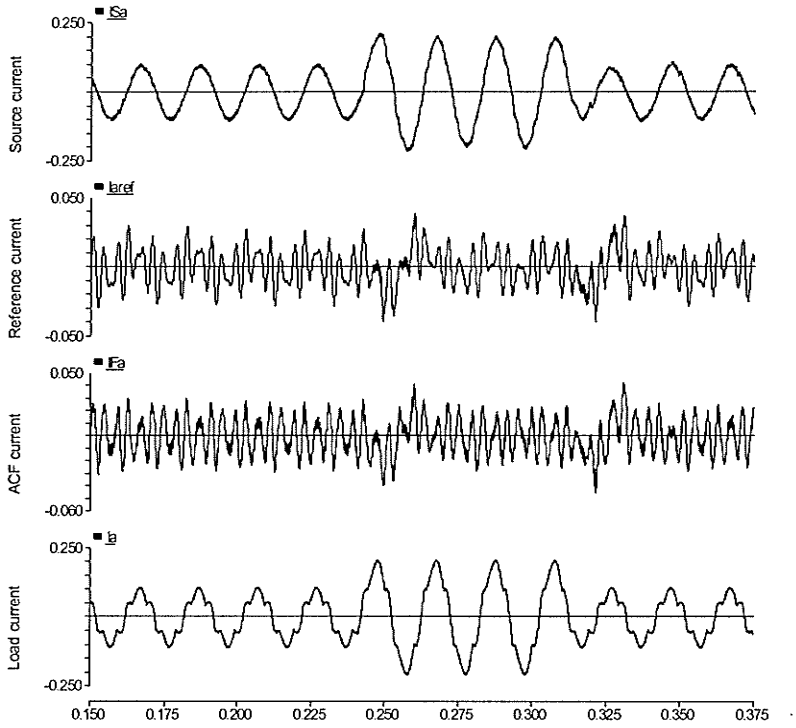


Figure 5.10 Simulation results with load change during run

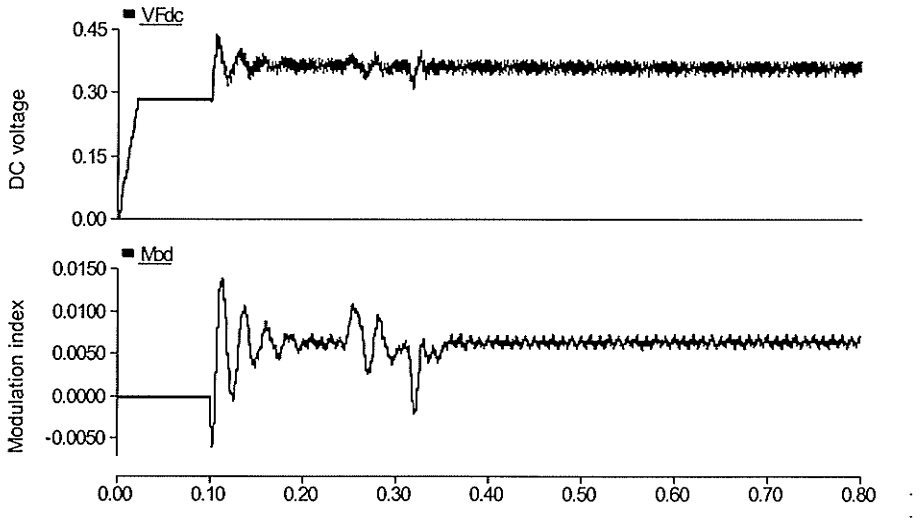


Figure 5.11 DC capacitor voltage and modulation index with load change during run

5.2.5 RL-type equivalent source with SCR study

In the previous sections, we only concern the resistive source. It is more practical that the ac source is a RL-type equivalent network. In this section, we will examine the performance of active filters in a RL-type equivalent network. The steady state performance of the active filter is studied. However, the transient performance is not stated in this thesis and will leave for the future study.

The relative strength of the ac system is often parameterized by an index called the short circuit ratio or SCR. The SCR is defined as the short circuit MVA of the ac bus divided by the dc power as in (5.1). Lower the SCR means the network impedance is higher, and thus the system is weaker; higher the SCR means the network impedance is lower, and thus the system is stronger.

$$SCR = \frac{V_{lp}^{\ 2}}{P_d \cdot |Z_s|} \tag{5.1}$$

In order to examine if the control method is applicable in a weak system, we tested this case with a SCR of 1 and a damping angle at fundamental frequency of 75 degrees (which is typical). We also tested this case for a strong system with a SCR of 5 and a damping angle of 75 degrees. The RL type equivalent source in Figure 5.1 consists of the series-connection of a resistance and an inductance. The equivalent impedance Z_s is calculated from (5.1) where V_{lp} and P_d are the ac-bus line voltage and the rectifier load rating, respectively. In this case V_{lp} is 0.2KV and P_d is 0.02MVA. From (5.1), we can get $Z_s = 0.5176 + j1.9319$ when SCR is 1 and $Z_s = 0.1035 + j0.3864$ when SCR is 5. The simulation results are shown in Figure 5.12 and 5.13, respectively.

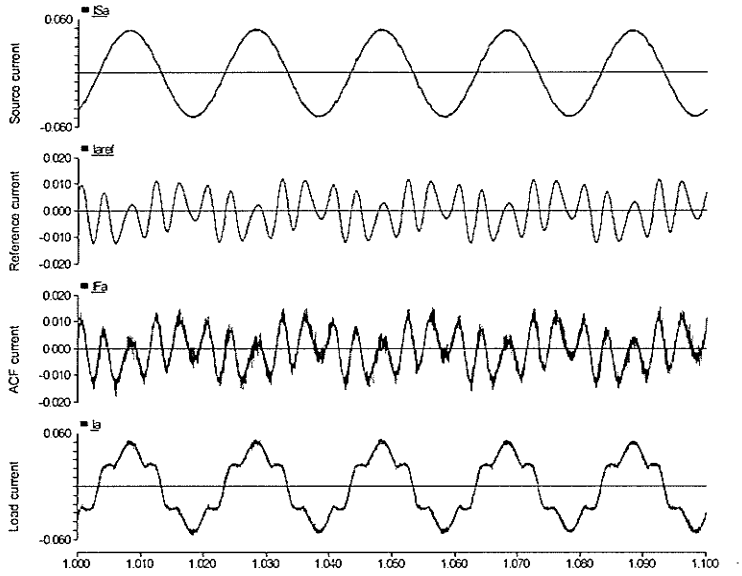


Figure 5.12 Simulation results when SCR=1

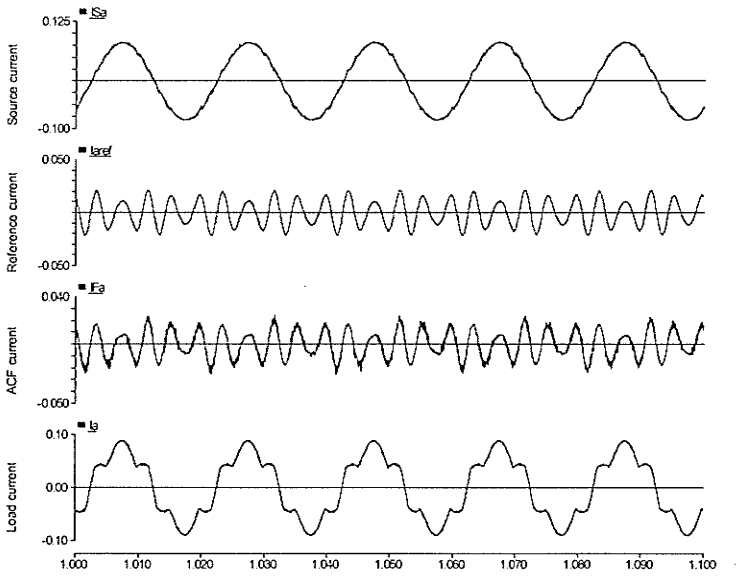


Figure 5.13 Simulation results when SCR=5

The simulation results indicate that the proposed control method works well for both weak and strong systems in steady state. For a weak system as in Figure 5.12, the active filter injection current contains the fundamental component, which flows into or out of the active filter in order to keep the dc capacitor voltage constant. On the other hand, for

a strong system as shown in Figure 5.13, there is very little variation in the ac busbar voltage and consequently the dc capacitor voltage in active filter keeps constant.

Figure 5.14 summarizes the control system of phase A, which is an extension of re-approach shown in Figure 5.3 and 5.7. The active filter generates an output current that is derived with the objective of controlling the real and imaginary parts of the harmonic current to zero, and DC voltage difference to zero. The measurement of bus voltage *Va* and system side current *Isa* in phase A are supplied to a Discrete Fourier transform (DFT) block, which extracts the magnitude and phase of both the 5^{th} (*Is5a, ph5a*) and the 7^{th} (*Is7a, ph7a*) harmonic currents. The DFT block also outputs the fundamental frequency and voltage phase angle. The control system re-calculate each harmonic current to a real and an imaginary parts [i.e. *Is5a cos(ph5a)* and *Is5a sin(ph5a)*], each of which is controlled to zero by a PI-controller. The output from each of the two PI-controllers is transformed back to time-domain quantities and then added to form the ordered current *Ia5ref(t)* to the active filter. A similar control system, shown in the middle part of Figure 5.12, is used to calculate the current order *Ia7ref(t)* related to the 7^{th} harmonic current. The DC voltage control signal is obtained by the voltage regulator and is in phase with voltage *Va*. The modulation index *mod* from the DC voltage regulator is the magnitude of the control signal. Finally, these three current orders are added together to form the total current order *Iaref(t)* for phase A. The phase reference [i.e. *cos(5wt)* and *sin(5wt)*] used in signal reconstruction is obtained from a phase looked loop. An identical algorithm is used to calculate the current order both in phase B and C.

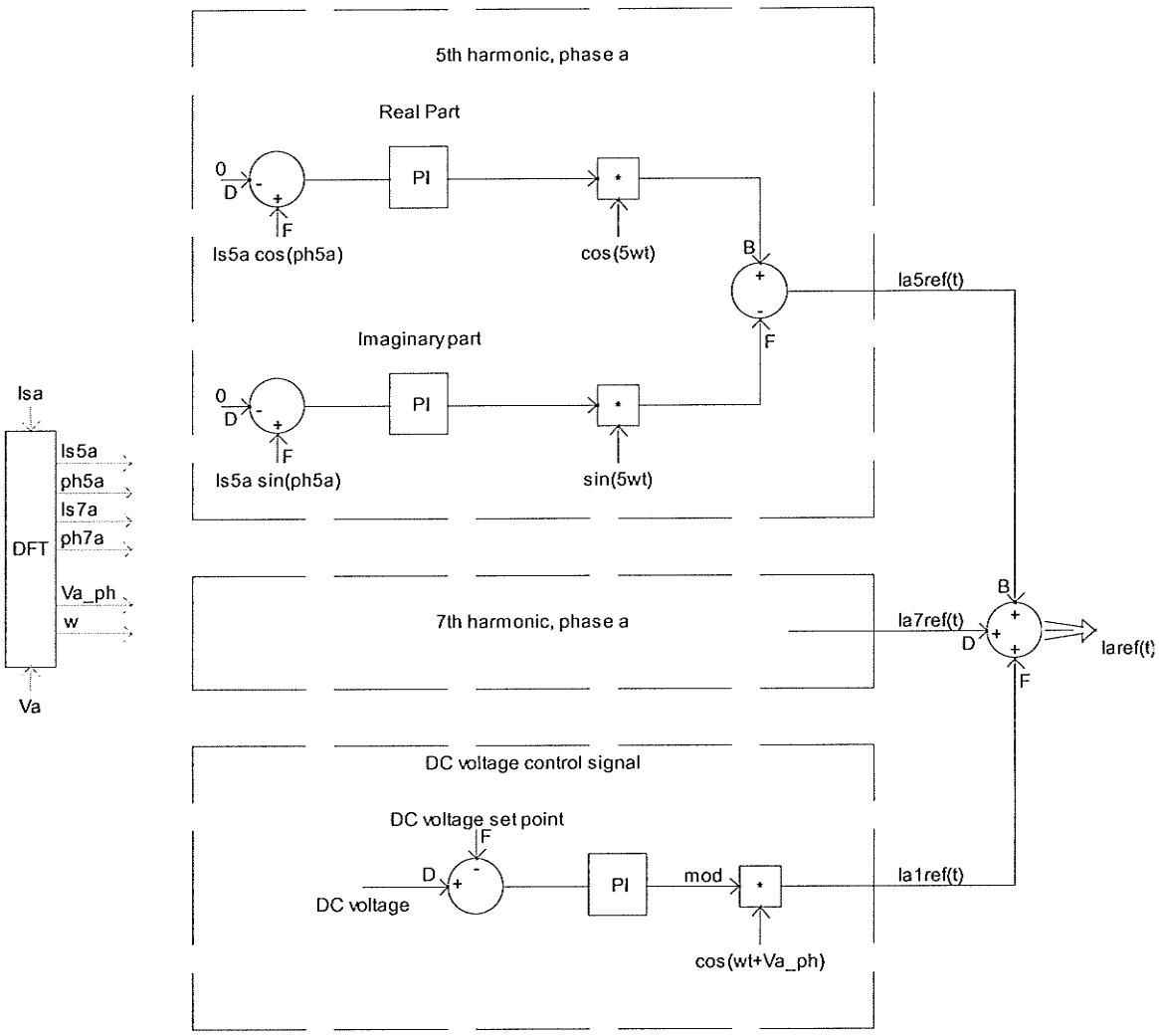


Figure 5.14 The control system of phase A

5.3 CONCLUSION

The indirect control approach to the active filter on a realistic circuit has been investigated using the transient simulation program PSCAD/EMTDC. The static state and transient performance seemed to be adequate. The active filter with dc capacitors was studied and a method of the dc voltage control is implemented.

--Chapter 6--

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

This thesis focuses on the control strategies of active filter systems. The ideal harmonic compensation was studied. Various types of harmonic sources and active filter combinations were investigated using circuit theory. Then two basic control approaches, the direct control and the indirect control were compared based on analytical and simulation studies. Furthermore, the impact of the time delay on the filtering performance of the direct control method is investigated in detail using mathematical analysis and simulation study. Finally, the indirect control approach to the active filter of a realistic electronic system was investigated using the transient simulation program PSCAD/EMTDC.

Based on the circuit analysis and numerical simulation, the following conclusions are made:

1. An active filter can successfully remove the harmonics produced by non-linear loads. Filters ratings can be selected using a circuit analysis approach.
2. The Discrete Fourier Transform (DFT) can be used to extract harmonic components for the use of control system. The direct control approach does not work well in the actual active filter systems where the variations of parameters and measurement / control delays are inevitable. On the other hand, the indirect control is more tolerant to the system parameters change. It is quite robust in real active filter systems.

3. The performance of the direct harmonic elimination approach is highly dependent on the control system time delay. If the delay time is an integer multiple of one cycle of certain harmonic, this order of harmonic will be eliminated. On the other hand, if the delay time is an odd number multiple of half cycle of certain harmonic, the filter current will be in-phase with this particular harmonic, resulting in increased harmonics in the source side. The possible way to eliminate all the harmonics is to let the delay time to be equal to one fundamental cycle to ensure that the control signal is identical to harmonics in the load side. However, when using the direct control method, the permitted delay time is very tiny. For example, for the 13^{th} harmonic, in order to filter out 99% harmonic current, the permitted control time delay is 2.04 microsecond, in the range of ten microseconds or much less than 1 degree based on the fundamental frequency. The permitted delay time is so small that any small interference will cause large deviation of the filtering results. This unforgiving property of the direct harmonic elimination will significantly reduce the reliability of the active filter and eventually prevent its application in actual active filter systems.
4. The indirect control approach can be used in realizing CRPWM control for the active filter to remove the harmonics generated from a six-pulse converter.

6.2 FUTURE WORK

In this thesis, only current controlled PWM (CRPWM) are used to generate injection current in simulation models of actual active filters, as harmonic currents form a large class of injection signals of active filters. Voltage controlled PWM (SPWM) are not considered in the thesis and further investigation is recommended for future work.

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APPENDICES

Listing of the Variables

I_s: *system current.*

I_{sh}: *system harmonic current component.*

I_a: *non-linear load current.*

I_{a1}: *non-linear load fundamental frequency current component.*

I_{ah}: *non-linear load harmonic current component.*

I_h: *current source load harmonic current.*

I_f: *filter current.*

I_{ref}: *filter reference current.*

E_s: *system voltage.*

V_a: *bus A voltage.*

V_{ah}: *bus A harmonic voltage component.*

V_h: *voltage source load harmonic voltage.*

V_f: *filter voltage.*

Z_S: *system equivalent impedance.*

Z_L: *load equivalent impedance.*

Z_f: *filter equivalent internal impedance.*

L_f: *filter inductance.*

C_f: *filter capacitance.*

x: *delay angle.*

y: *fraction of harmonic current entering ac network.*

τ: *delay time.*

Listing of the Figures and Tables