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THE USE OF ADVANCED STATIC VAr COMPENSATORS FOR LOAD COMPENSATION

By

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THE USE OF ADVANCED STATIC VAr COMPENSATORS

FOR LOAD COMPENSATION

BY

BRIAN ANDREW S. ARCHER

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ABSTRACT

Previous researchers have proved that Advanced Static VAr Compensators (ASVCs) with GTO thyristors are capable of providing effective, balanced reactive power compensation with several advantages over current Static VAr Compensators (SVCs). Researchers have also proved that load compensators with Thyristor Controlled Reactors and Fixed Capacitors (TCRs/FCs) are capable of fast and accurate load compensation of three–phase unsymmetrical loads. This investigation capitalizes on the advantages of the ASVC, to design a compact load compensator capable of effectively compensating three–phase unsymmetrical loads and possessing several advantages over the TCR/FC type load compensator.

The load compensation problem is first represented in terms of variable susceptances and the presence on the ac system of undesirable positive– and negative–sequence current components. The function of current load compensators, which utilize feedforward, direct calculation type controls are studied. The ability of Current Sourced Inverter (CSI) type ASVCs with firing angle control and Voltage Sourced Inverter (VSI) type ASVC with phase shift angle control for providing the necessary positive–sequence currents for the elimination of those which are present in the ac system, due to the unsymmetrical loads, are explored. A novel inverter Pulse Width control (PW) method using sinusoidal modulation is introduced. When applied to the CSI the system is capable of generating appropriate negative–sequence currents for satisfying the second part of load compensation. The PW control cannot be successfully applied to a VSI. A dual bridge load compensator which comprised a firing angle controlled positive–sequence bridge and a PW control negative–sequence bridge, both of the CSI type was designed, modelled, and simulated on an Electromagnetic Transient program for DC simulation (EMTDC). Finally a Sinusoidal Pulse Width Modulation (SPWM) scheme is applied to a VSI, resulting in a compact load compensator capable of simultaneously providing both

correct positive– and negative–sequence current components for fast and accurate load compensation. This system is designed, modelled, and simulated on EMTDC.

Results from the digital simulations of the dual bridge compensator and the SPWM–VSI compensator are presented for various degrees of load imbalance.

The conclusion drawn is that while the dual bridge load compensator possessed neither the response speed nor the compensation range for operation as a practical and effective ASVC type load compensator, the SPWM–VSI load compensator proved to be fast and accurate and therefore capable of operating as a practical ASVC type load compensator. The SPWM–VSI possessed certain advantages over the TCR/FC type load compensator such as: response speed, decreased size, decreased use of passive components, better harmonic performance, and the use of less calculations in its control structure. However, the feedback method of control used proved to be more complicated than that of the TCR/FC type load compensator. Proposals are made for changing the controls of the SPWM–VSI from a feedback type to a feedforward, direct calculations type.

ACKNOWLEDGEMENTS

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LIST OF SYMBOLS AND ABBREVIATIONS

Some of the most frequently occurring abbreviations and symbols used in the text are presented below. Other symbols which occur in one place only are explained where they appear.

SYMBOL	REPRESENTATION
Ac	amplitude of carrier waveform
Ar	amplitude of reference waveform
ASVC	advanced static VAr compensator
B	susceptance
Cd, C_{DC}	dc capacitor
CSI	current sourced inverter
(d, q)	two–axis transformation
EMTDC	electromagnetic transient program for dc simulation
F	filter
Fc	frequency of carrier waveform
Fo	frequency of output waveform
Fr	frequency of reference waveform
FC	fixed capacitor
G	conductance
GTO	gate turn off
HP	high pass
Hz	hertz, cycle per second
Ic	compensator current
Id	inverter dc side current
In	magnitude of nth harmonic current
Is	system supply current

I_0	zero–sequence current component
I_1	positive–sequence current component
I_2	negative–sequence current component
Ld	dc smoothing reactor
$L\delta$	transformer inductance
M	modulation magnitude control
m	modulation index
max.	maximum
meas.	measured
min.	minimum
P	real power
p	pulse number
pf	power factor
PI	proportional integral
PLL	phase locked loop
pu	per unit
PW	pulse width control
PWM	pulse width modulation
Q	reactive power
ref.	reference
SPWM	sinusoidal pulse width modulation
SVC	static VAr compensator
t	time
TCR	thyrisor controlled reactor
TN	thyristor # N
TSC	thyristor switched capacitor
uF	micro–farads

VCO	voltage controlled oscillator
Vd	dc voltage
VI	vector identifier
vo	output voltage
Vrms	root mean square voltage
VSI	voltage sourced inverter
Xt, Xδ	transformer leakage reactance
Y	admittance
α	firing delay angle
(α, β)	two–phase transformation
ψ,β	sinusoidal modulation phase shift angle
δ	modulation phase shift control angle
$\Delta\alpha$	firing angle difference
ϕ	phase shift angle
w	frequency in radians per second

Chapter 1

Introduction

1.1 Purpose

The objective of this thesis is to investigate the possibility of using Advanced Static VAr Compensators (ASVCs) for cancelling the unbalanced currents due to the presence of unsymmetrical loads in three–phase ac power systems. The application of various methods of control to Voltage Sourced Inverters (VSIs), Current Sourced Inverters (CSIs) and combinations thereof will form the foundation of this investigation. Two possible methods of solution will be simulated on an Electromagnetic Transients program for DC simulation (EMTDC) [1] and their performance compared with present types of load compensators.

1.2 Motivation

Due to the recent advances in the development of high power thyristors with fast switching capabilities, such as the Gate Turn Off Thyristor (GTO), the focus of reactive power compensation is changing from that of using combinations of Fixed Capacitors (FCs), Thyristor Switched Capacitors (TSCs) and/or Thyristor Controlled Reactors (TCRs), which comprise devices referred to as Static VAr Compensators (SVCs), to configurations which comprise either single– or three–phase GTO converters which are called ASVCs. The potential advantages are projected to be in the form of reduced compensator size, increased compensation ranges with better transient performance, decreased costs, more precise reactive power control and improved harmonic performance. A few

relatively small prototypes of these ASVCs are currently performing satisfactorily in distribution systems. One such example includes a ± 1 MVAr ASVC which was developed by Edwards and Nannery and which has been in operation at the Orange and Rockland Utilities Inc., Spring Valley, NY, since October 1986 [2]. In their present application these ASVCs are required to provide reactive power compensation in the form of voltage control to balanced three–phase systems.

As opposed to system compensators, load compensators are usually much smaller devices which are required to provide reactive power compensation for unsymmetrical three–phase loads. This usually demands that the load compensator generate unbalanced currents in order to cancel the effects of those which result from the presence of the unsymmetrical load on the power system. Current load compensators use TCRs and FCs for providing the required unbalanced currents, however this method of load compensation essentially treats the three–phase system as three separate single phases and concentrates on compensating each phase separately. When designed with accurate, high speed controls, such as the design by Gueth, et. al. [3] where a Programmable High Speed Controller (PHSC) [4] was used, these load compensators perform satisfactorily. However, there has been no research to date on the concept of a solid state load compensator which would utilize fewer passive components and less complicated controls, and be less costly than current load compensators and which would possess the increased effective operating range, improved transient performance and compactness of the ASVC.

1.3 Thesis Outline

Chapter 2 takes a more indepth look at the requirements for and current trends in load compensation. Current state of the art load compensators are examined and their control structures explained. In Chapter 3 the possibility and

advantages of using solid state GTO converters for power–factor correction are discussed. A comparison is made between the suitability of the CSI and the VSI for controlling the reactive power. The last section in this chapter examines the fault performance of GTO thyristor converters as opposed to conventional thyristor converters. Chapter 4 looks at the concept of Pulse Width Control (PW) for achieving unbalanced operation in GTO converters and the application of these as part of a dual bridge load compensator. The dual bridge compensator combines the concepts of Chapter 3 with those of the earlier sections of Chapter 4. In this chapter the results from the simulation of the dual bridge load compensator on EMTDC are presented. In the fifth chapter the concept of utilizing Sinusoidal Pulse Width Modulation (SPWM) in a VSI for the development of a compact load compensator is presented. A SPWM–VSI type load compensator is designed and the results from the EMTDC simulation presented. Chapter 6 commences with a comparative analysis of the performance of all the load compensators which were presented in previous chapters and concludes with recommendations for improving their performance.

Chapter 2

Load Compensation

2.1 The Requirement and Objectives for load Compensation

The basic objectives which are associated with load compensation are power factor correction and load balancing. The aim being to correct the power factor of the load to unity and to balance the unbalanced currents which result from the presence of an unbalanced load in the supply system. When the above objectives are realized, only in–phase balanced currents will flow in the supply system. Generally the requirement is for the load compensation to be accomplished within two to four cycles of the system's fundamental frequency and for all undesirable harmonics which result from the load compensation scheme to be eliminated. Load compensation, which can also be thought of as the cancellation of the reactive power or VAr demand of large and fluctuating industrial loads, should not be confused with system compensation or voltage support of transmission lines. With system compensation (voltage support) the objective is to regulate or control the voltage at the specific terminal which is being compensated by inducing an appropriate voltage across the ac system impedance at that terminal.

Ideally, that is if both effective load as well as system compensators are present, an ac power system would: possess constant voltage and frequency at every supply point; have unity power factor; and be free from harmonics. In particular, these parameters would be independent of the size and characteristics of the consumers' loads. Also, there could be no interference between different loads as a result of variations in the current taken by each one. However, most

industrial loads add to the imperfections of the power system since they invariably possess lagging power factors, hence they absorb reactive power, and the resulting current which is drawn by the load will be larger than is required for real power consumption only. From the supply utility point of view, transmission of unnecessary reactive power means that the transmitted currents will be much greater requiring higher rating utility feeders and transformers which result in higher than necessary capital costs. The penalty to the consumer is the increased billing by the supply utility in order to compensate for the increased costs. To reduce this problem, dynamic static var compensators are increasingly being used. Here the term load compensation is used where the reactive power management is effected for a single load (or group of loads) and the compensating equipment is usually located adjacent to large cyclic or intermittent loads. The proper application of such compensators can allow for substantial expansion of an existing plant without the necessity of increasing the rating of the utility feeders and transformers supplying the plant.

2.1.1 Power Factor Correction

Power factor correction usually entails generating reactive power as close as possible to the load which requires it, rather than supplying the reactive power from a remote power station. Due to the nature of industrial loads, the aim is to compensate the load such that it appears to the remainder of the power system as a purely resistive load, that is, one which neither absorbs nor generates reactive power and whose power factor is unity. This results in the transfer of only real power between the generating bus and the load. To illustrate this concept: suppose a single phase lagging power factor load with admittance $Y_L = G_L + jB_L$ is supplied from a bus with r.m.s voltage V, as shown in Figure 2.1(a) below,

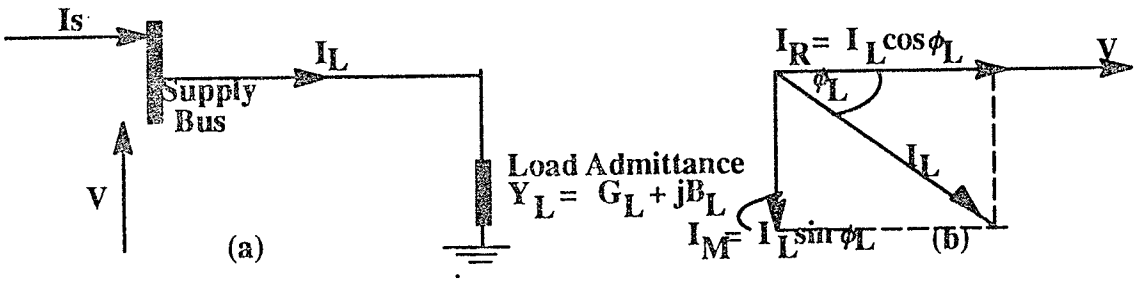


Figure 2.1: (a) supply bus with lagging power factor load; (b) phasor diagram representing system

then the current which must be supplied to the lagging power factor load I_L can be expressed as:

$$\begin{aligned} I_L &= VY_L \\ &= V\ (G_L + jB_L) \\ &= VG_L + jVB_L \end{aligned} \tag{2.1}$$

which shows that the load current has a real component I_R and an imaginary component I_M and

$$I_L = I_R + jI_M \tag{2.2}$$

Now the apparent power supplied to the load is

$$\begin{aligned} S_L &= VI_L^* \\ &= V^2G_L - jV^2B_L \\ &= P_L + jQ_L \end{aligned} \tag{2.3}$$

showing that the apparent power has a real component P_L and a reactive component Q_L. Therefore the current I_S supplied by the power system is larger than is necessary for real power transfer alone. According to the phasor diagram in Figure 2.1(b), I_S is larger by a factor of

$$\frac{I_L}{I_R} = \frac{1}{\cos\phi_L} = \frac{1}{pf} \tag{2.4}$$

If the load compensator, consisting of a purely reactive admittance which is equal and opposite to that of the load, is connected in parallel with the load, then the current supplied by the power system to both load and compensator will now be:

$$\begin{aligned} I_S &= I_L + I_C \\ &= V(G_L + jB_L) - V(jB_L) \\ &= VG_L = I_R \end{aligned} \tag{2.5}$$

The power factor of the system is now unity and the power system supplies only the current necessary for real power consumption, while the reactive power required by the load is supplied locally by the compensator.

The load compensation scheme as presented above is no doubt incapable of providing power factor correction to loads which vary their demand for reactive power since the principle involved fixed admittances. In later sections, the concept of a load compensator which is capable of following variations in the reactive power requirement of loads is presented.

2.1.2 Load Balancing

Generally most ac power systems are three phase and are designed for balanced operation. Unbalanced operation gives rise to unbalanced currents which result in negative– and zero– sequence components of current being present in the system. These sequence components can have undesirable effects, including additional losses in motors and generating units, oscillating torque in ac machines, increased ripple in rectifiers, malfunction of several types of equipment, saturation of transformers, and excessive neutral currents. Certain types of equipment, including several types of compensators, depend also on balanced operation for the suppression of triplen harmonics. Under unbalanced conditions, these would appear in the power system and harmonic elimination

problems are increased. These undesirable harmonics are usually eliminated by using appropriately tuned filters. However the problems of harmonic elimination are usually directly associated with compensation problems and in some cases can be used as a basis for accepting or rejecting a particular compensator configuration, since in some cases compensators themselves generate harmonics. In fact the study of harmonics and their elimination and/or suppression will be dealt with in this thesis, since solid state ASVCs generate undesirable harmonics.

2.2 Load Compensation with Admittance Networks for Unsymmetrical Loads

An indepth examination of the utilization of phase balancing and power factor correction of unsymmetrical loads can be obtained in [5, 6]. Briefly, the approach to load compensation is summarized in the following important principles:

1) Any unbalanced linear ungrounded three phase load can be transformed into a balanced, real three–phase load without changing the real power exchange between source and load, by connecting an ideal compensating network in parallel with it.
2) The ideal compensating network can be purely reactive.
3) If the load admittances vary, then an ideal compensating network should also possess varying susceptances if the compensation is to remain perfect.
4) The ideal load compensator is conceived as any passive three–phase admittance network which, when connected in parallel with the load, will present a real and symmetrical load to the supply.

Figure 2.2 below incorporates the four rules listed above in order to design the three–phase, delta connected ideal compensating network. This design is attributed to C.P Steinmetz and is developed in its entirety in [5, 6]. In this case

balanced supply voltages are assumed. The aim of the compensating network is to cancel the reactive power in each branch of the load.

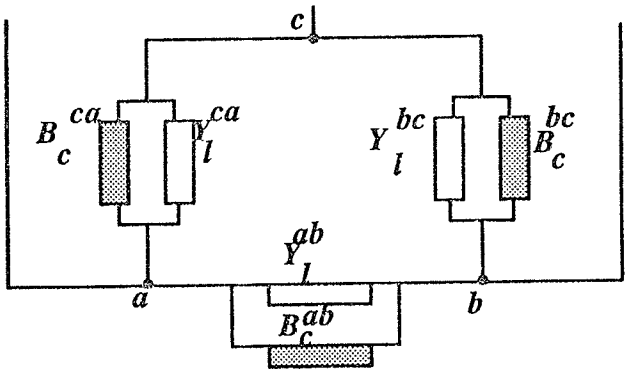


Figure 2.2: An ideal compensating network

Consider the three–phase delta–connected unbalanced load in Figure 2.3, here

$$Y_l^{ab} \neq Y_l^{bc} \neq Y_l^{ca} \tag{2.6}$$

where the subscript *l* represents load and the superscripts (*ab*, *bc* and *ca*) represent the particular phase of the delta in which the admittance is connected. Now in order to compensate such a load the requirement is for an admittance network which, when combined with the unbalanced three–phase load, presents to the supply terminal a real, balanced load. With reference to Figure 2.3 each load admittance can be compensated separately as if it was a single phase load.

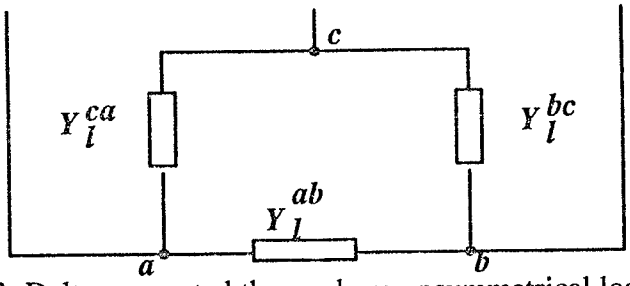


Figure 2.3: Delta connected three–phase unsymmetrical load

Consider the admittance Y_l^{ab} in phase *ab* to be made up of a conductance G_l^{ab} and a susceptance B_l^{ab}, that is

$$Y_l^{ab} = G_l^{ab} + jB_l^{ab} \tag{2.7}$$

Now in order to reduce Y_l^{ab} to a conductance, a susceptance which is capable of cancelling the susceptance jB_l^{ab} is required, this can be accomplished by connecting a susceptance $-jB_c^{ab}$ (c representing the compensator) in parallel with Y_l^{ab}. Therefore equation (2.7) becomes

$$Y_l^{ab} = G_l^{ab} \tag{2.8}$$

If similar susceptances are placed in parallel with the conductances in each phase then the load will now appear as shown in Figure 2.4.

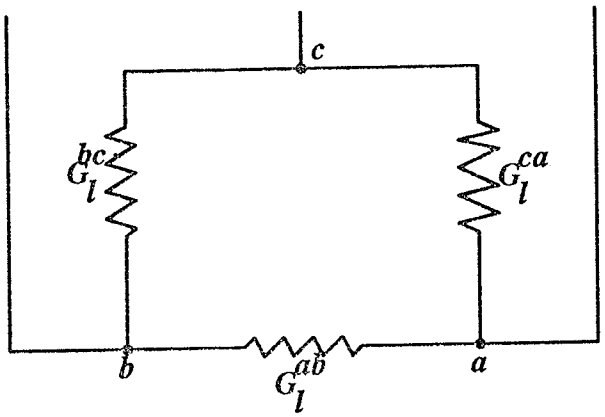


Figure 2.4: Unbalanced unity power factor load

This load is now purely resistive, which means that it presents a unity power factor system to the supply. The load however remains unbalanced. If phase *ab* is again selected, then in order to maintain a real but balanced load, Steinmetz suggested that a capacitive susceptance

$$B = \frac{G_l^{ab}}{\sqrt{3}} \tag{2.9}$$

must be connected in phase *bc* and an inductive susceptance

$$B = \frac{-G_l^{ab}}{\sqrt{3}} \tag{2.10}$$

must be connected in phase *ca*. Similar steps are performed on the admittances in phases *bc* and *ca* resulting in the ideal compensating network of Figure 2.2 which presents a real and balanced three–phase load to the supply. Now for each phase the total susceptance required by the compensation network which is in parallel with the unbalanced three–phase load is,

$$\begin{aligned} B_c^{ab} &= -B_l^{ab} + \frac{(G_l^{ca} - G_l^{bc})}{\sqrt{3}} \\ B_c^{bc} &= -B_l^{bc} + \frac{(G_l^{ab} - G_l^{ca})}{\sqrt{3}} \\ B_c^{ca} &= -B_l^{ca} + \frac{(G_l^{bc} - G_l^{ab})}{\sqrt{3}} \end{aligned} \tag{2.11}$$

The load conductances are therefore balanced (load requires same power in all three phases), and the load power factor is unity.

The above ideal compensating network is a very effective theoretical illustration which is hardly ever used in practical systems due to the difficulty which is involved in measuring the load admittances, and the system's inability to compensate rapidly varying loads. It is generally much easier to measure the separate line currents and voltages which can then be utilized in order to accurately calculate the susceptances which are required in each phase for load compensation. In Section 2.3 load compensation systems which are currently in use are presented.

2.3 Current Trends in Load Compensation

Most of the load compensation schemes which are presently in use utilize some appropriate control structure in order to realize appropriate susceptances or currents needed for compensating fluctuating loads in a relatively short time (two to four cycles of the power system's fundamental frequency). Most of these

compensating systems use direct computation or 'feedforward' control methods, although some use a combination of 'feedforward' and 'feedback' control depending on the complexity of the problem at hand [7]. Usually in direct computation type systems, a set of steady state equations are repeatedly solved using an appropriately predetermined algorithm. These equations in most cases, represent the variable susceptances as functions of load characteristics which are available, and which can be easily and accurately measured and/or calculated, such as the line currents and voltages or the symmetrical component representation of these. To realize the variable susceptances, TCRs with FCs are predominantly used. TCRs with TSCs are hardly ever used since these are more suitable for system compensation (See Section 2.3.2). Section 2.3.3 examines some of the 'feedforward' control methods which are currently used.

2.3.1 The Symmetrical Component Description of Load Compensation

In this thesis, load compensation will be realized by employing solid state static power converters. The basis for their use in existing prototypes, as presented in [8, 9, 10], requires the accurate measurement and control of both the required and generated reactive power. Alternatively the 'state' of the load which requires compensation can be effectively described in terms of the three–phase symmetrical components of its line currents thus eliminating the need for reactive power measurement and control. In terms of three phase symmetrical components, a measure of the negative–sequence load current gives an indication of the degree of load imbalance. Unbalanced loads give rise to unbalanced currents which result in the presence of components of load current in the wrong phase sequence, namely the negative– and zero– sequence. In three wire system however, the sum of the line–to–neutral voltage phasors is always

zero, hence the zero–sequence component is never present. Therefore the compensated load will be balanced if its negative–sequence current is zero, requiring that,

$$I_2(l) + I_2(c) = 0 \tag{2.12}$$

where the subscripts *l* and c have been added to emphasize the load and compensator currents respectively. This equation applies to both the real and imaginary components of the negative sequence load and compensator currents. Likewise a measure of the positive–sequence current in the load is an indication of the power factor of the load. Therefore in order to realize the requirements stated above for effective load compensation, namely that the power factor of the load should be unity, this requires that the imaginary part of the positive–sequence line current should be zero. That is,

$$\text{Im} \; [\; I_1(l) + I_1(c) \;] = 0 \tag{2.13}$$

2.3.2 The Thyristor Controlled Reactor with Fixed Capacitors for Realizing Variable Susceptances

The TCR/FC arrangement is shown in Figure 2.5(a) and consists of a fixed capacitor in parallel with a thyristor–controlled inductor. In this arrangement the conduction interval of the thyristor switches are varied thereby controlling the flow of current in the inductor (L), this is achieved by delaying the closing of the thyristor switches by an angle α in each half cycle with respect to the peak of the applied voltage. The two oppositely poled thyristors conduct on alternate half–cycles of the supply frequency. Figure 2.5(b) shows the fundamental inductor current (I_{L1}) as a function of α whilst Figure 2.5(c) shows the TCR/FC control process. Here the controlled inductor current, $i_L(\alpha)$ is shown along with

the applied voltage, v, as the firing delay angles of the thyristor switches are varied from 0° to 90°. The assumption is that the gating is delayed by equal amounts for both thyristors (symmetrical firing or balanced gating). If the thyristors are gated into conduction precisely at the peaks of the supply voltage, full conduction results in the reactor and the current is the same as if the thyristor controllers were shorted. The current lags the voltage by nearly 90° and is almost purely reactive due to the fact that there exists a small in–phase current component which results from the power losses in the reactor. A TCR with FC cannot have a lagging current unless the TCR's reactive power absorption rating exceeds that of the capacitors, that is X_L must be smaller than X_C. When this condition is satisfied a variable susceptance with a range of control in both the inductive and capacitive domains can be realized.

According to Figures 2.5(b) and 2.5(c) the current in the inductor can be varied from zero to a maximum value corresponding to firing delay angles of 90° and 0° respectively meaning that the effective impedance of the inductor is varied from an infinite value (zero inductor current with no thyristor conduction) to a value equal to X_L (maximum inductor current with full thyristor conduction).

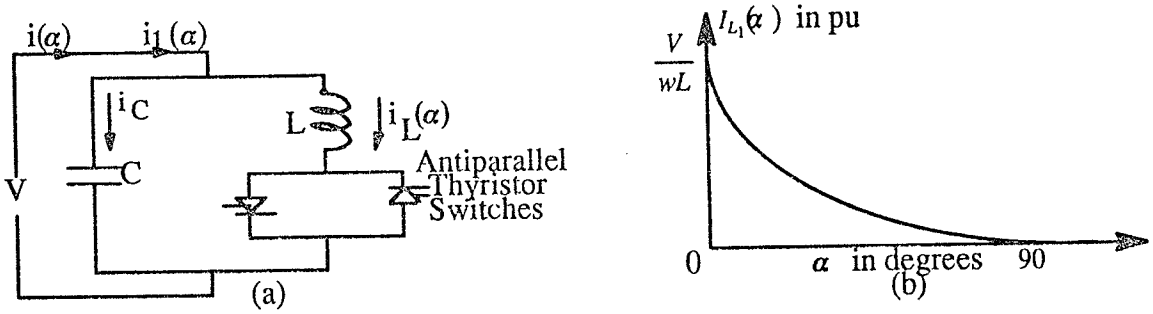


Figure 2.5 (a) Single–phase TCR/FC type compensator (b) fundamental inductor current vs thyristor firing delay angle α

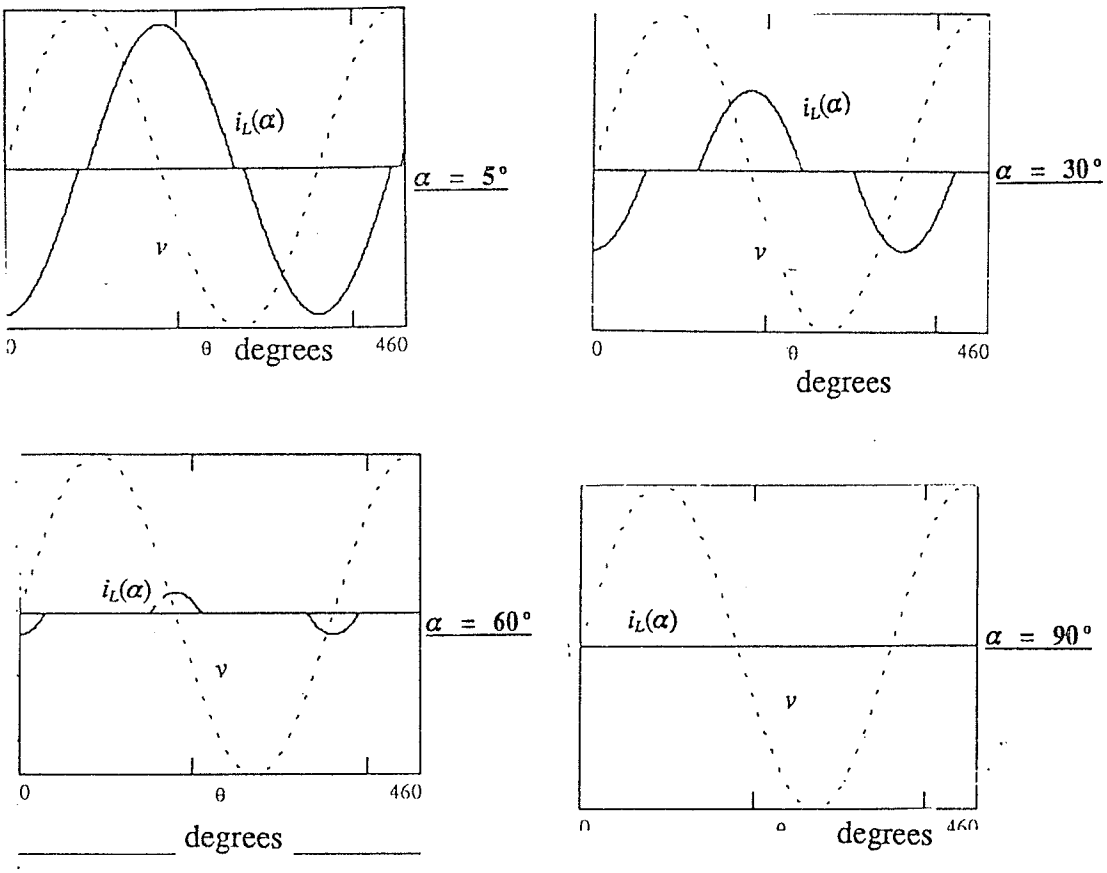


Figure 2.5: (c) current and voltage waveforms as a function of α

By controlling α the total current i(α) can be controlled from varying magnitudes of purely inductive to purely capacitive, and in terms of the fundamental component of current, the TCR/FC arrangement represents a controlled susceptance. In practice, the effective impedance and compensating current can only be adjusted in discrete instants of time, not more than once in each half cycle and the net reactive power absorption rating with the capacitors connected is equal to the difference between the ratings of the TCR and the FC. The main disadvantage of using TCRs is that they generate undesirable harmonics. For identical positive and negative current half-cycles (symmetrical or balanced thyristor firing) only odd harmonics are generated. For a three-phase system, the single-phase TCRs are usually connected in delta, thus when the thyristor firing is balanced, all odd harmonics (n = 5, 7, 11, 13, . . .), with the exception of the triplen harmonics (n = 3, 9, 15, . . .), must be filtered. The triplen harmonics circulate in the closed delta and are absent from the line currents. The other odd

harmonics are usually kept out of the line currents by replacing the fixed capacitors with a filter network which draws the same fundamental current at the system frequency and provides a low impedance shunt path at the harmonic frequency. Under unbalanced firing conditions all harmonics including even harmonics along with dc components are produced underlining the importance of symmetrical thyristor firing.

With the TCR/FC arrangement only one set of antiparallel high voltage thyristor switches in series with the inductor is required in each phase. Depending on the total rating of the compensated system, the TCR can be connected directly to the ac system without the need for step–down transformers. The response of the TCR/FC type load compensator is much faster than older systems which utilized switched inductor and capacitor banks, this renders the TCR/FC scheme more advantageous for compensating electric arc furnaces [11] which present to the power system a rapidly varying, generally unbalanced load with a poor lagging power factor. In general the TCR/FC type load compensator offers excellent performance and high reliability at a fairly acceptable cost. However, later chapters will show how the rapid development of high power thyristor switches such as Gate Turn Off thyristors (GTOs) and their use in static power converters, present the potential for even cheaper and more compact methods of load compensation.

Section 2.3.3 shows one method for developing the control equations which can be used in a 'feedforward' type control system and Section 2.3.4 examine some of the control methods which are currently used in variable susceptance type load compensators.

2.3.3 Development of Control Equations for Variable Susceptance Type Load Compensators

In a paper by Gueth, et. al. [3] an algorithm is developed which is based on

equations (2.12) and (2.13) and which encorporates fast and accurate measurement of the sequence component currents along with accurate control of a TCR's firing instants in order to provide rapid load compensation without the need for feedback. In fact the control methodology which is presented in that paper results in effective load compensation within two cycles. For increased speed and accuracy a PHSC is proposed. Figure 2.6 demonstrates the use of a delta connected load compensator which is based on the general concepts presented in Sections 2.3.1–3 and [3, 7]. Here B*ab*, B*bc* and B*ca* represent variable susceptances in phases *ab*, *bc* and *ca* respectively, these can be either capacitive(+) or inductive(–). If the unbalanced load is assumed to be supplied by a balanced three–phase set of voltages with positive phase sequence, then the rms line–to–neutral voltages will be: Va = V; Vb = a^2V; and Vc = aV, where a = –0.5 + j0.866

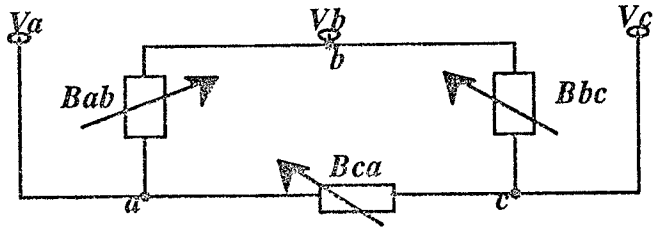


Figure 2.6: Delta connected load compensator with variable susceptances

Therefore

$$\begin{aligned} Vab &= Va - Vb = (1 - a^2)V = \sqrt{3}\,V\angle 30^o \\ Vbc &= Vb - Vc = (a^2 - a)V = \sqrt{3}\,V\angle -90^o \\ Vca &= Vc - Va = (a - 1)V = \sqrt{3}\,V\angle -30^o \end{aligned} \qquad (2.14)$$

and

$$\begin{aligned} Iab &= jBab\ Vab = j\sqrt{3}\,V\angle 30^o\ Bab \\ Ibc &= jBbc\ Vbc = j\sqrt{3}\,V\angle -90^o\ Bbc \\ Ica &= jBca\ Vca = j\sqrt{3}\,V\angle -30^o\ Bca \end{aligned} \qquad (2.15)$$

and the line currents in the compensating network can be expressed in matrix form by the subtraction of the phase currents as

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = j3V \begin{bmatrix} 1\angle 30^{\circ} & 0 & 1\angle -30^{\circ} \\ 1\angle -150^{\circ} & 1\angle -90^{\circ} & 0 \\ 0 & 1\angle 90^{\circ} & 1\angle 150^{\circ} \end{bmatrix} \begin{bmatrix} Bab \\ Bbc \\ Bca \end{bmatrix} \tag{2.16}$$

The symmetrical component transformation is now applied to the three line currents which results in expressions for I_1, I_2, and I_0 representing the positive–, negative–, and zero–sequence current components respectively, in terms of the susceptances. Therefore

$$\begin{bmatrix} I_1 \\ I_2 \\ I_0 \end{bmatrix} = V \begin{bmatrix} 1\angle 90^{\circ} & 1\angle 90^{\circ} & 1\angle 90^{\circ} \\ 1\angle 150^{\circ} & 1\angle -90^{\circ} & 1\angle 30^{\circ} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} Bab \\ Bbc \\ Bca \end{bmatrix} \tag{2.17}$$

With reference to equations (2.12) and (2.13) it should be noted that the compensator, under balanced voltage conditions, can receive only imaginary components of the positive sequence current ($\mathrm{Im}\{I_1\}$), both real and imaginary components of the negative–sequence current ($\mathrm{Re}\{I_2\}$ and $\mathrm{Im}\{I_2\}$) an no zero–sequence component. This implies that,

$$\begin{bmatrix} \mathrm{Im}\{I_1\} \\ \mathrm{Re}\{I_2\} \\ \mathrm{Im}\{I_2\} \end{bmatrix} = V \begin{bmatrix} 1 & 1 & 1 \\ -\sqrt{3} & 0 & \sqrt{3} \\ \frac{1}{2} & -1 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Bab \\ Bbc \\ Bca \end{bmatrix} \tag{2.18}$$

Therefore the susceptances *Bab*, *Bbc*, and *Bca* which are required for load compensation can be calculated by inverting the matrix which contains the coefficients of the variable susceptances. This results in an equation for accurately calculating the compensator susceptances from the measured sequence components of current as shown below.

$$\begin{bmatrix} Bab \\ Bbc \\ Bca \end{bmatrix} = \frac{1}{V}\begin{bmatrix} 1 & -\sqrt{3} & 1 \\ 1 & 0 & -2 \\ 1 & \sqrt{3} & 1 \end{bmatrix}\begin{bmatrix} \mathrm{Im}[I_1] \\ \mathrm{Re}[I_2] \\ \mathrm{Im}[I_2] \end{bmatrix} \tag{2.19}$$

2.3.4 Methods of Control for Variable Susceptance Type Load Compensators

Section 2.3 stated that direct computational or 'feedforward' control was the main form of control which is currently used in load compensators. According to the above discussions on the derivation of the variable susceptances, by using TCR/FC type load compensators, it is apparent that for accurate load compensation the required controller must be able to:

1) accurately interpret the 'state' of the load, that is by measuring the load currents or voltages in each phase;
2) apply the information from 1) to a set of steady state equations which represent the susceptances as functions of the measured quantities, such as equation (2.19) ;
3) derive from the susceptances the correct value of the reactor current which is required to flow in each phase of the TCR/FC compensator; and
4) convert the desired reactor current into a corresponding firing angle, where the relationship between the fundamental reactor current and the firing angle is given by equation (2.20) [7, 12] .

$$I_{L_1} = \frac{V}{wL}\left(1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin 2\alpha\right)$$
$$0 \le \alpha \le \frac{\pi}{2} \tag{2.20}$$

This control approach is based on the fundamental presumption that the load is in steady state between any two consecutive instants of time at which the current in the compensating susceptances is changed. Since the operation of each TCR/FC

is synchronized to the line–to–line voltage to which it is connected, the above calculations for each phase must be carried out over time intervals which are mutually displaced by a third of the periodic time of the ac system voltage [7]. Figure 2.7(a) shows a schematic of the compensation scheme and emphasizes the fact that the three compensating currents are independently controlled for each phase of the compensated load. Figure 2.7(b) summarizes steps 1) to 4) above . It is important to note that if the above arrangement is used with a transformer, the calculations must be appropriately adjusted in order to take into consideration the transformer's leakage reactance.

The 'feedforward' control in practical applications, differ only by the choice of controllers for processing the steady state equations, and the equations which are used in order to describe the 'state' of the load. Most times these two choices are governed by the speed and accuracy with which a particular quantity could be measured and processed and by the other functions which are required of the control system, that is apart from load compensation: for example [3] specifies that apart from load compensation within two cycles, the control system should be capable of regulating the voltage to a selected range within four cycles and maintaining the negative sequence voltage within a selectable maximum limit within four cycles. Also in this case the control system is required to allow voltage regulation to take priority over load compensation.

In [3] the controller is of the PHSC type and the variable compensating susceptances are represented as functions of the symmetrical current components and the positive–sequence phase reference phasor voltage. The values of the required susceptances are calculated using equation(2.19) which is represented in the PHSC by adders (See Figure 2.8).

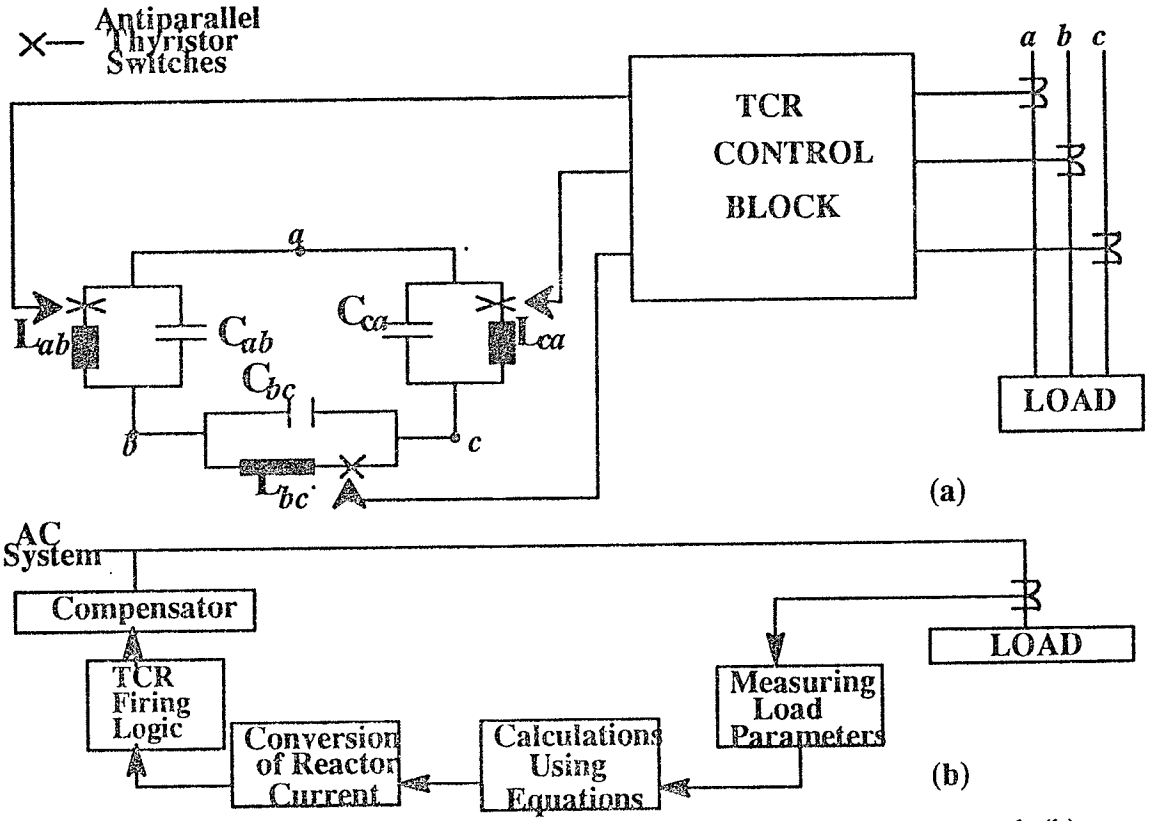


Figure 2.7: (a) Load compensation scheme using 'feedforward' type control (b) TCR control block

A function generator is then used to convert the susceptance values to the required firing angle for the antiparallel thyristors in each phase .

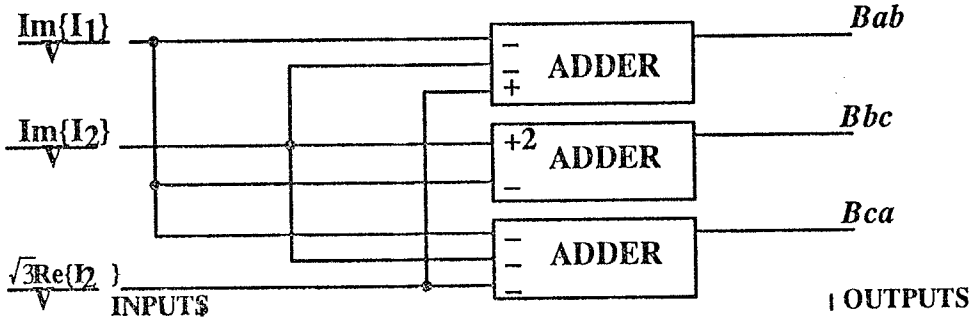


Figure 2.8: Adder blocks for implementing equation (2.19) with a PHSC type load compensator

The presented results show that among other advantages, the use of the PHSC

significantly reduces the amount of system parameters which must be measured; increases the accuracy of the firing angle calculation and eliminates the need for feedback control.

2.4 Chapter Summary

This chapter presented a brief overview of the requirements and objectives for load compensation. Load compensation was explained in terms of power factor correction and load balancing, and the required response speed of load compensators was said to be in the range of 2–4 cycles of the system's fundamental frequency. The principles for designing load compensators by way of admittance networks was explored. However since these networks did not possess variable admittances it was concluded that they cannot compensate varying unsymmetrical loads. Compensators with the ability to compensate rapidly varying unsymmetrical loads and based on the measurement of symmetrical component currents were presented. It was observed that most of these compensators were of the TCR/FC type with feedforward, direct calculation type controllers. The development of the control equations for such load compensators was presented and the performance of a load compensator based on the use of a PHSC was examined.

Other conclusions which can be drawn from this chapter includes:

1. The objectives of load compensation are quite different from those of system compensation. Load compensators are required to correct the power factor and balance unsymmetrical loads whilst system compensators are required to regulate or control the voltage at the specific terminal which is being compensated;
2. The power factor of a load can be corrected to unity if:

    i) a purely reactive admittance which is equal and opposite to that of the

load is connected in parallel with the load; or

ii) the imaginary part of the positive–sequence current component due to the load is eliminated.

3. An unsymmetrical load can be balanced by:

i) connecting appropriate susceptances in parallel with the impedances in each phase of the load. These impedances can be chosen based on the ideal compensating network attributed to C.P.Steinmetz:

ii) eliminating both the real and imaginary parts of the negative–sequence current component due to the presence of the load.

4. Controlling the firing instants of the thyristors, thereby controlling the period of conduction, in a TCR/FC compensator arrangement can result in the establishment of appropriate variable susceptances in order to compensate an unsymmetrical load. If the firing of the thyristors is balanced (symmetrical firing) only odd harmonics are generated and for a three–phase system the TCRs are usually connected in delta which results in the elimination of the triplen harmonics. All other odd harmonics are still present and must be filtered out. Usually the FCs are replaced by filter networks which provide low impedance shunt paths at the harmonic frequencies.

Chapter 3

Solid State Converters for Power Factor Correction

3.1 Advanced Static Var Compensators with GTO thyristors

In this chapter the power factor correction aspect of load compensation will be addressed whilst the load balancing aspect of load compensation will be addressed in Chapter 4. In the first case the ability of static power converters with GTO thyristors to provide adequate balanced reactive power compensation or purely imaginary positive–sequence currents for power factor correction will be exploited, whilst in the second case the GTO thyristor converter's ability to provide the unbalanced currents or correct values of the negative sequence currents which are needed for load balancing will be examined.

In a paper by Gyugyi [5], the idea of using power converters for reactive power control was presented, however this idea was more of a conceptual one, possessing potentially many advantages over the SVC, than a practical one since the performance of power converters in high power applications were questionable, this due to the unavailability of appropriate high power switches. With the development of the GTO thyristor small prototypes of the ASVC came into operation. Although GTOs are currently available with ratings of 4500V and 2500A [13] and higher, the use of GTO based ASVCs for high power utility applications have not found acceptance due to their complexity [14]. However, because of the potential advantages which can be derived from the use of such systems and with more research, the prediction is that ASVCs will eventually

replace conventional SVCs in reactive power control. In Section 3.1.1 the function of GTO thyristor switches in inverters will be examined.

3.1.1 GTO Thyristor Switches in Inverters

There are basically two types of inverters: the voltage sourced inverter; and the current sourced inverter. These two types of inverters derive their names from the dc source which is applied to the dc end of the inverter. Conventional thyristor converters are usually restricted to line commutated circuits usually of the current sourced type whilst GTO thyristor converters can be self commutated and are generally of both the current sourced and voltage sourced type. Usually a VSI has a capacitor connected directly across the dc terminals, with no intervening impedance apart from snubbers and wiring, and a CSI has an inductor in series with the dc terminals, preceded by no shunt impedance apart from snubbers and stray capacitance.

In this thesis the use of both VSIs and CSIs along with combinations of the basic configurations, in order to realize a practical load compensator, will be investigated. Section 3.2 presents a brief look into the operation of the CSI type var controller and Section 3.3 examines the VSI type var controller.

3.2 Current Sourced Inverters

3.2.1 The Operational Characteristics of Current Sourced Inverters

In a conventional 6–pulse, line commutated GTO thyristor inverter in normal operation and connected to a balanced three phase load, each valve conducts 120° per cycle. Since the conducting periods of the six valves are evenly distributed, the resulting current waveform is a quasi–square one. See Figure 3.1.

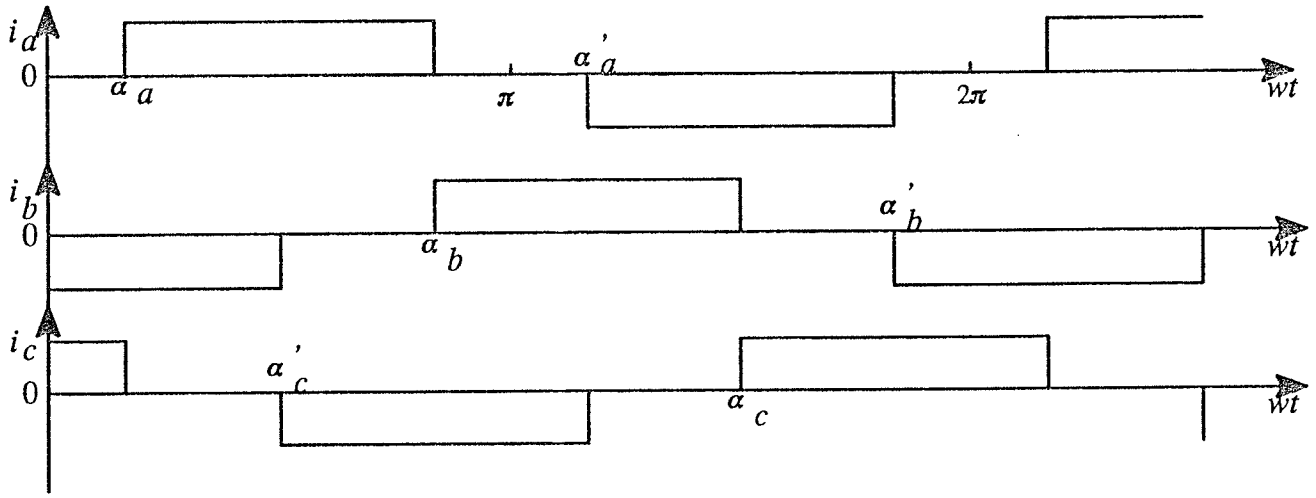


Figure 3.1: Inverter current waveforms in normal operation

The firing angles are equally displaced between the three phases as α_a, α_b and α_c for phases a, b and c respectively. In normal balanced operation

$$\begin{aligned} \alpha'_a &= \alpha_a + 180^o \\ \alpha'_b &= \alpha_b + 180^o \\ \alpha'_c &= \alpha_c + 180^o \end{aligned} \tag{3.1}$$

The dc supply of a 6–pulse current sourced inverter is supposed to be an ideal current source which in practice is a regulated rectifier with filters and sufficient inductance. In normal operation the current is interrupted by the outgoing valve of one phase and diverged to another phase by the incoming valve. The fast switching causes high stress on the outgoing valve due to the inductance in the circuit. The capacitors which are connected across the inverter's output terminals serve to absorb the energy which is released from the inductance. A GTO CSI is shown in Figure 3.2.

On the ac side there are normally harmonic filters in parallel with the load. In normal operation, the output current for phase a can be expressed using Fourier analysis as :

$$i_a = [\frac{2\ I_d\sqrt{3}}{\pi}] \sum_{n=0}^{n=\infty} \frac{1\ (-1)^k\ \sin\ nwt}{n}$$

$$n = 6k \pm 1,\quad k = 0,\ 1,\ 2,\ \ldots \tag{3.2}$$

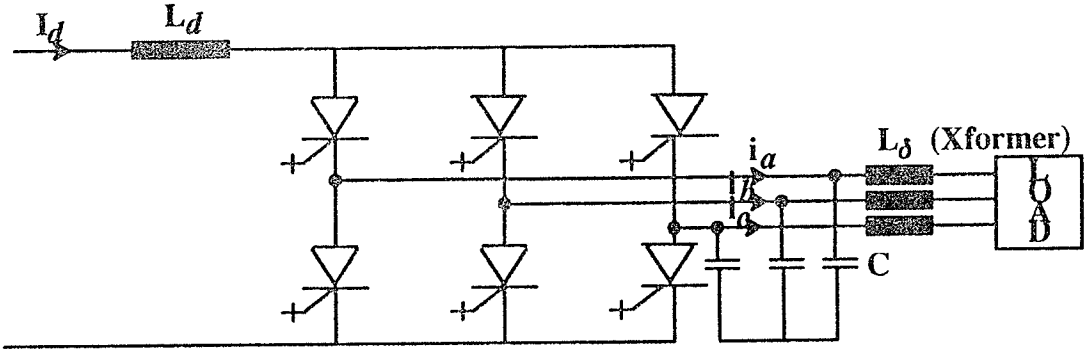


Figure 3.2: Current Sourced 6–pulse GTO thyristor inverter

hence the magnitude of the rms fundamental current component in phase *a* can be expressed as

$$I_a = \frac{\sqrt{2}\ I_d\sqrt{3}}{\pi} \tag{3.3}$$

and the nth current harmonic as

$$I_n = \frac{I_a}{n} \tag{3.4}$$

Usually single–tuned filters for 5th, 7th, 11th and 13th harmonics are required in order to eliminate these harmonics, and a damped high pass filter is required in order to suppress the 17th and higher order harmonics.

3.2.2 The Current Sourced Inverter for Reactive Power Control

A current sourced type var generator can be realized by utilizing an

inductively loaded ac/dc GTO converter as shown in Figure 3.3 (taken from [5]).

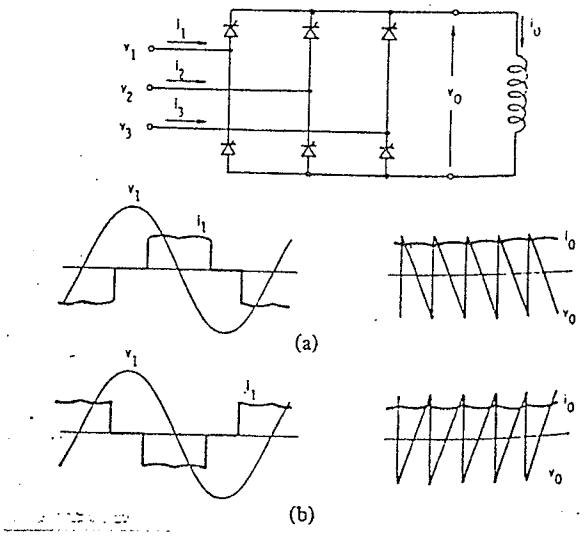


Figure 3.3: CSI as a var generator (a) lagging operation (b) leading operation

Since a naturally commutated converter can only provide lagging vars, it is common practice to use the self commutated converter since it provides both lagging and leading vars. In terms of the power factor correction aspect of load compensation, this self commutated inverter can correct for both leading as well as lagging power factor loads.

A naturally commutated converter can only operate if the thyristor switches are fired at such delay angles where the dc current is 'naturally' transferred from one pair of thyristors to the next pair. Hence there is a general restriction on the angle of delay to the range 0° to about 160°, measured from the earliest point of natural commutation. The phase of the ac line current lags the corresponding

voltage by an angle which is equal to the firing delay angle. Therefore when the CSI is used as a reactive power source, the firing delay angle is 90°, as shown in Figure 3.3(a). The effective operation of this system requires establishment and maintenance of the required dc current in the inductor. To do this the firing delay angle must in practice be slightly less than 90° so that there is just enough dc voltage to overcome the thyristor voltage drops and the resistances of the inductor and the ac system. The magnitude of the dc current and consequently the amplitude of the ac line currents can therefore be effectively controlled by adjusting the firing delay angle. Hence a naturally commutated converter can be viewed at the ac lines as a continuously variable balanced three–phase inductor. In order to supply controllable leading reactive power, the converter inputs must be shunted by three capacitor banks of appropriate rating. This is to ensure that the combined current drawn from the ac system becomes leading as the converter current is decreased.

In order to make the converter input currents leading, it is necessary to advance the firing angles by 90° with respect to the first point of natural commutation. The mean dc output voltage is zero and the converter input currents lead the corresponding input voltages by 90° as shown in Figure 3.3(b). Again the practice of advancing the firing angle slightly less than 90° is used in order to establish and maintain the required dc current. The self commutated GTO converter is thus a four–quadrant converter capable of operating over the total firing angle range of 0° to 360°.

The rating of the CSI reactive power controller can be approximately one–half the rating of some other SVC approaches for a given application. Details are given in [8].

In terms of symmetrical components and in keeping with the theory developed in Chapter 2, the CSI when operating as a source of reactive power can

be viewed as a source of imaginary positive sequence current. Basically when the CSI is made to operate at a firing delay angle of 90° relative to the corresponding system voltage phase angle, variation of the magnitude of the dc input current can result in the production of lagging positive sequence current of varying magnitudes. In fact the result is an linear relationship between the magnitudes of I_{dc} and I_1. Similarly when the firing delay angle is –90° relative to the corresponding system voltage phase angle, leading positive sequence current of varying magnitudes can be produced. Figure 3.4 shows the relationship between I_{dc} and I_1.

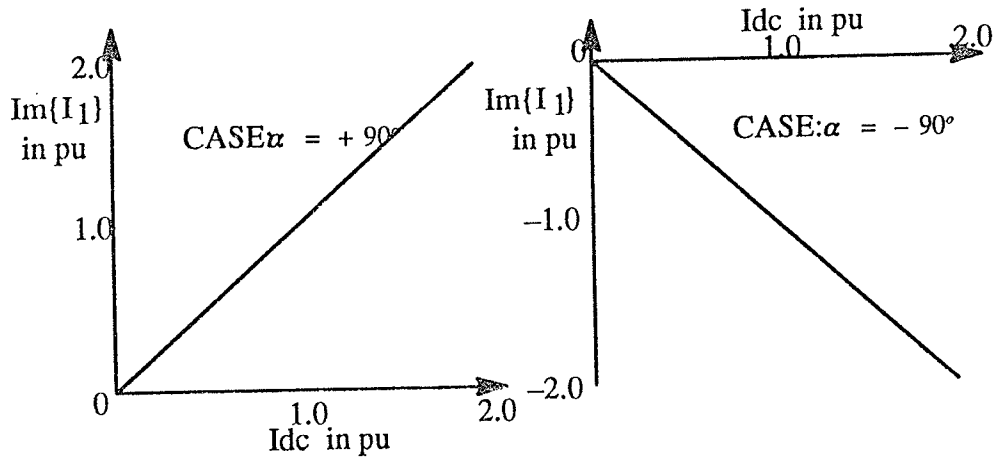


Figure 3.4: Positive sequence current vs Idc

3.3 Voltage Sourced Inverters

3.3.1 Operational Characteristics of Voltage Sourced Inverters

The voltage sourced inverter is the dual of the current sourced inverter. The line–to–line voltage of a VSI is similar to the line current of a CSI. Figure 3.5 illustrates the fact that gating the thyristors in the sequence T1, T2, T3, T4, T5 and T6 every cycle and leaving each conducting for 180° of the output cycle will produce voltages with respect to the negative terminal, *Van, Vbn* and *Vcn* at the

output terminals *a*, *b* and *c*. The capacitor which is connected across the inverter's dc terminals is assumed to behave like an ideal voltage source when charged. The inverter can therefore produce a set of quasi–square output voltage waveforms of a given frequency by connecting the capacitor sequentially to the three output terminals of the appropriate GTO switches. The output waveforms at the centre of the switch poles are shown in Figure 3.6 as *Van*, *Vbn* and *V cn*.

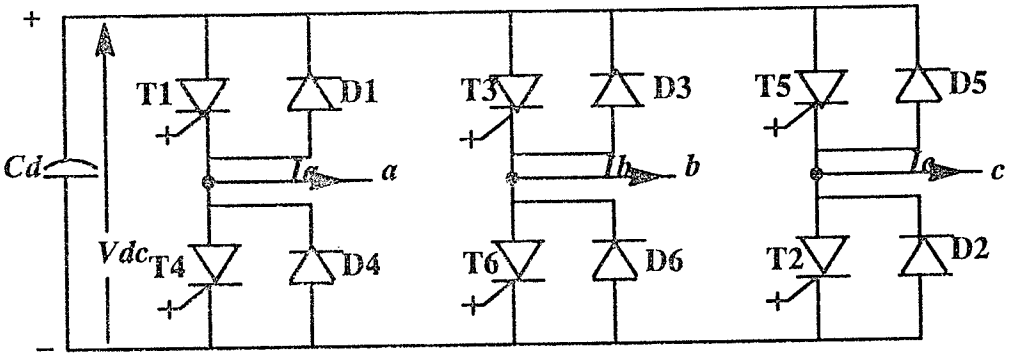


Figure 3.5: VSI firing sequence

The line–to–line voltages *Vab*, *Vbc* and *Vca* are obtained by subtraction as follows:

$$\begin{aligned} Vab &= Van - Vbn \\ Vbc &= Vbn - Vcn \\ Vca &= Vcn - Van \end{aligned} \qquad (3.5)$$

and are displaced 120° from each other as shown in Figure 3.6. Application of Fourier analysis in a similar manner as with the current sourced inverter, results in the following line–to–line voltages.

$$Vab = \sum_{n=1,3,5\ldots}^{n=\infty} \frac{4V_d}{n\pi} \cos\left(\frac{\pi}{6}\right) \sin n \left(wt + \frac{\pi}{6} \right)$$

$$Vbc = \sum_{n=1,3,5\ldots}^{n=\infty} \frac{4V_d}{n\pi} \cos\left(\frac{\pi}{6}\right) \sin n \left(wt - \frac{\pi}{2} \right)$$

$$Vca = \sum_{n=1,3,5\ldots}^{n=\infty} \frac{4V_d}{n\pi} \cos\left(\frac{\pi}{6}\right) \sin n \left(wt + 5\frac{\pi}{6} \right)$$

(3.6)

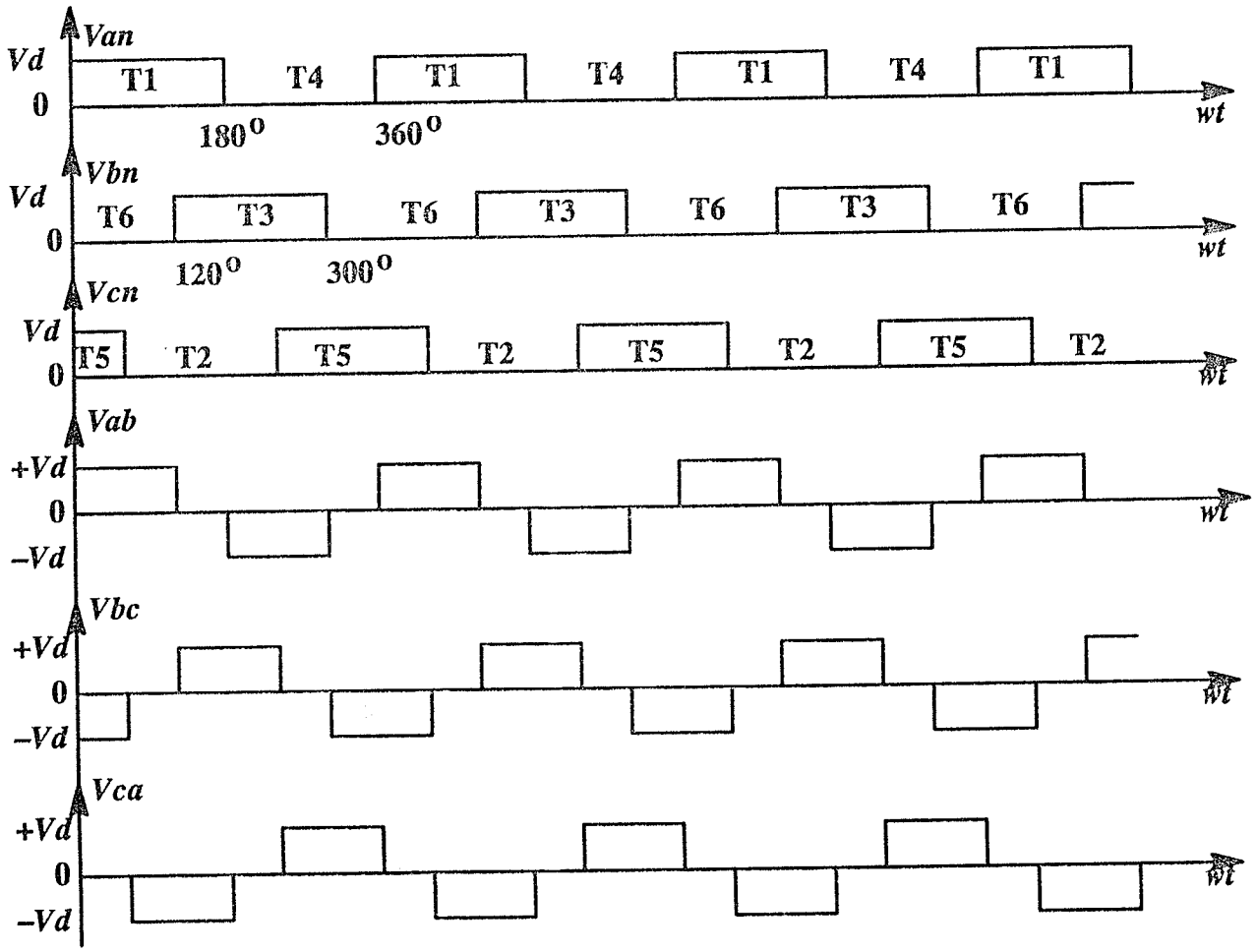


Figure 3.6: VSI output voltage waveforms

3.3.2 The Voltage Sourced Inverter for Reactive Power Control

The basic use of voltage sourced inverters for reactive power generation and control is discussed extensively in [2, 5, 10], and will only be summarized here.

The shunt connected dc/ac voltage sourced inverter can be represented at its output terminals as an ac voltage source. This inverter when connected to the ac line through a relatively small reactance (usually provided by the per phase leakage inductance of the coupling transformer) displays the general characteristics of a conventional rotating synchronous condenser. For purely reactive power flow the inverter output voltages *Va, Vb* and *Vc* must be kept synchronized and in phase with the ac system voltages *VAN, VBN* and *VCN*. By controlling the amplitudes of the inverter fundamental output voltages, the reactive power can be controlled from full leading to full lagging. When the inverter's fundamental output voltage is higher than that of the line, leading reactive current is drawn from the line (vars are generated or capacitive current is drawn from the ac system). When the inverter's fundamental output voltage is lower than that of the line, lagging reactive current is drawn from the line (vars are absorbed or inductive current flows out of the ac system).

The operation can be viewed from another perspective by considering the relationship between the output and input powers of the inverter. The important fact being that the net instantaneous power at the ac output terminals must always be equal to the net instantaneous power at the dc input terminals. This of course is based on the assumption that the losses in the semiconductor switches are negligible (ideal switches assumed). Since in the ideal case the line current is purely reactive then no real power is required. Practically however, some real power is required in order to compensate for inverter losses. This real power can be supplied in two ways:

1) The losses are replenished by utilizing a separate dc supply as shown in Figure 3.7. However this method is uneconomical and therefore hardly ever used.
2) The losses can be replenished by using a suitable dc reservoir capacitor as shown in Figure 3.8, and each inverter output voltage is made to slightly lag

the corresponding ac system voltage. A real component of the current will then flow from the ac system to the inverter, and the losses will be compensated for.

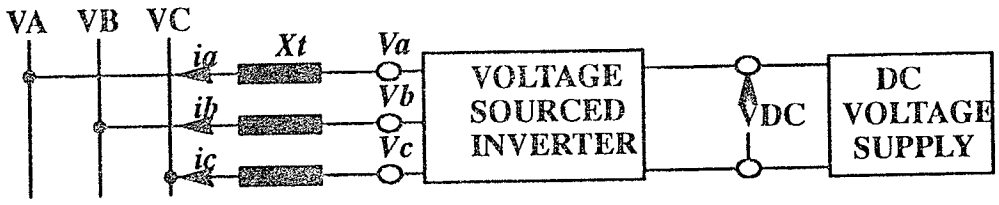


Figure 3.7: VSI var generator with separate dc supply

The dc reservoir capacitor is required to maintain a smooth dc voltage while carrying the ripple current drawn by the inverter. This ripple current is a function of the type of circuit configuration and operating mode of the inverter used.

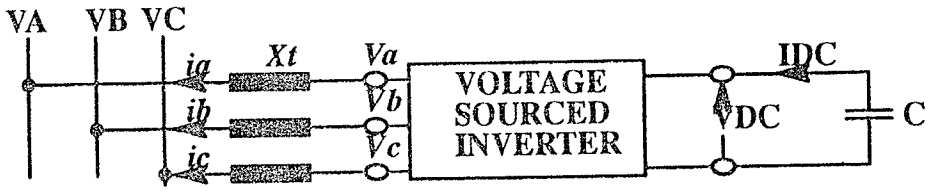


Figure 3.8: VSI var generator without separate dc supply

To control the reactive current, the magnitude of the dc voltage is raised or lowered by adjusting the phase angle of the inverter's output voltage so that in addition to the losses, some real power flows in or out of the dc capacitor as required.

Yet another way of examining this system is to investigate, as outlined in Chapter 2, the control of the imaginary component of the positive–sequence current which flows in the transformer reactance. If effective control of the imaginary component of the positive–sequence current can be realized, then the possibility of generating imaginary components of the positive–sequence current

which are equal in magnitude and opposite in polarity to that flowing in a particular load, can in effect result in the presence of only the real component of the positive–sequence current flowing into the load. This results in a unity power factor system. Therefore the load will appear to be resistive to the other parts of the power system. From a fundamental current component standpoint, this can be developed as shown below. .

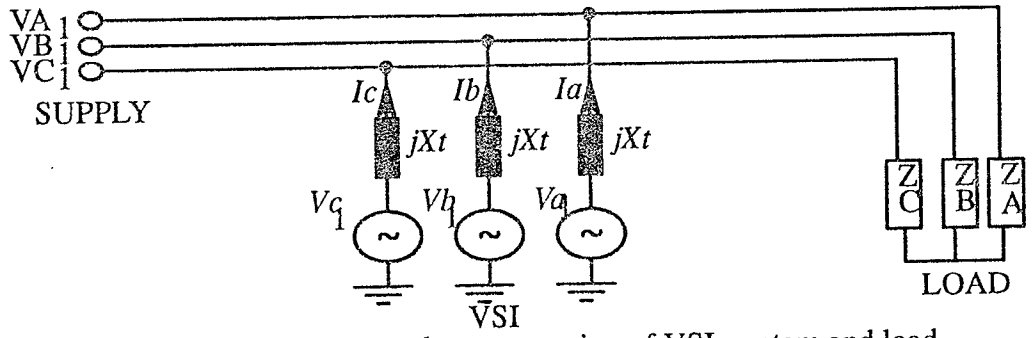


Figure 3.9: Modelled fundamental representation of VSI, system and load

Suppose the system is represented as shown in Figure 3.9, where balanced three–phase operation is assumed, and the rms value of the fundamental component of the system voltage is V = 1.0 pu, $a = -0.5 + j0.866$ and the rms value of the fundamental component of the inverter output voltage is Vi then

$$Ia = \frac{Va_1 - VA_1}{jXt}$$
$$Ib = \frac{Vb_1 - VB_1}{jXt}$$
$$Ic = \frac{Vc_1 - VC_1}{jXt} \qquad (3.7)$$

$$VA_1 = V \quad VB_1 = Va^2 \quad VC_1 = Va$$
$$Va_1 = Vi \quad Vb_1 = Via^2 \quad Vc_1 = Via \qquad (3.8)$$

and for balanced operation

$$Ii_2 = Ia + a^2Ib + aIc$$
$$Ii_1 = Ia + aIb + a^2Ic \qquad (3.9)$$

then by varying the amplitude Vi of the inverter's fundamental three phase output voltage, for the ideal case (no losses), the imaginary component of the positive sequence current flowing in the small transformer reactance Xt can be controlled from –90° to +90°. Figure 3.10 shows results for Xt = 0.2 pu and V = 1.0 pu.

In Section 3.4 a comparison is made between the VSI– and CSI– types of reactive power controllers whilst the potential advantages which can be derived from using solid state GTO power converters instead of conventional thyristor power converters for reactive power control will be examined in Section 3.5.

3.4 A Comparison of VSI and CSI Types of Reactive Power Controllers

. Required GTO valves

The GTO valves which are required in CSI and VSI reactive power controllers are different. In the case of the CSI the requirement is for power switches which possess symmetrical bidirectional voltage blocking capability.

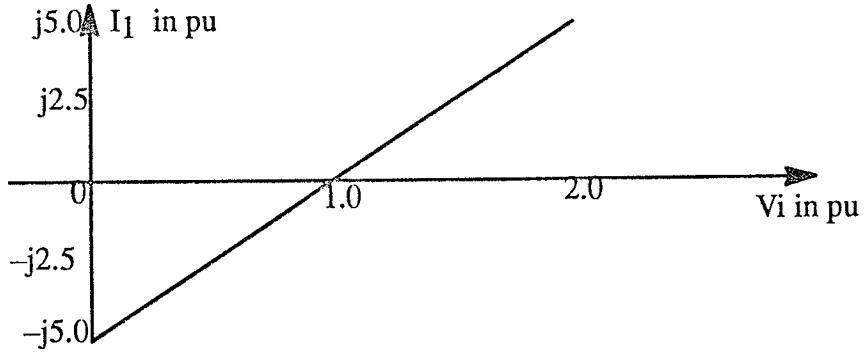


Figure 3.10: Positive– sequence current control in the VSI

With the VSI type reactive power controller the requirement is for power devices

which possess only unidirectional voltage blocking capability. The limited availability of power switching devices with symmetrical bidirectional voltage blocking capability is one of the reasons why VSI type var controllers are predominantly used.

. Principle of Operation

For the CSI type var controller in order to supply controllable lagging reactive power the firing delay angle must be set to 90^{o} and in order to supply leading reactive power the converter inputs must be shunted by three capacitor banks of appropriate rating. Effective operation of the CSI requires the establishment and maintenance of the dc current in the inductor. To do this the firing delay angle, in practice, is made to be slightly less than 90^{o}. Reactive power control is achieved by controlling the firing delay angle which controls the magnitude of the dc current and hence the amplitudes of the ac line currents. With the VSI type var controller a small tie–reactance links the inverter to the ac system and the inverter's fundamental output voltages are kept in–phase with the ac system voltages. For lagging operation the amplitudes of the inverter's fundamental output voltages are made to be lower than that of the line and for leading operation they are made to be higher than that of the line. In practice reactive power control is achieved by adjusting the phase angle of the inverter's output voltages so that in addition to losses some real power flows in or out of the dc capacitor.

. Freewheeling Diodes

Feedback diodes in parallel with the thyristors in the VSI are required in order to provide for reactive current flow. However these are not required in a CSI since the inductance L_d maintains a continuous flow of current from the dc supply.

. The Generation of Undesirable Harmonics

In both types of var controllers, without the application of any harmonic reduction and/or elimination techniques, undesirable harmonics are dumped unto the compensated system or load. With the VSI these harmonics will be of the voltage type and with the CSI they will be of the current type. In the case of the VSI the undesirable harmonics are easily eliminated by either Pulse Width Modulation (PWM), the use of tuned filters and/or the use of increased pulse number operation. However in the case of the CSI the application of PWM is not as simple as in the VSI case and the techniques differ in a number of important aspects. For example, the CSI does not lend itself well to subharmonic modulation techniques. In fact a popular subharmonic technique which can be easily applied to the VSI is the sinusoidal PWM technique. This technique derives proper firing pulses for the GTO switches by comparing a triangular carrier wave to a sinusoidal reference wave. However, this modulation cannot be used for a CSI because the PWM current waveform has to satisfy certain special symmetry constraints. Also, the commutation times involved in the CSI are longer and hence the minimum pulsewidth of the current PWM waveform has to be more carefully controlled.

- **Speed of Operation**

The dynamic performance of both the VSI and CSI type var controllers would approximate that of the fastest SVCs available, which is in the order of 2 to 4 cycles of the power system's fundamental frequency.

In Chapter 4 the ability of these systems to provide the necessary unbalanced currents for the load balancing aspect of load compensation will be studied.

3.5 Potential Advantages in Using Solid State GTO Thyristor Converters for Reactive Power Control

In this section some of the potential advantages which can be derived from the use of solid state power converters with GTOs in the context of both system compensation (voltage support) as well as load compensation will be presented. The findings which will be presented here is a summary of several comparative studies which were performed and whose results are available in the published literature.

In recent times dynamic static var compensators were realized by using large passive components controlled by power switching devices. Such systems, apart from being bulky and prone to resonance effects, are lossy due to the large passive components utilized. The use of solid state power converters for providing dynamic static var compensation is not without its problems, but such systems are being recognized by large scale users of electric power as possessing many potential advantages over conventional SVCs. Such advantages include potential size, weight and cost reduction of associated reactive components, precise and continuous reactive power control with fast response times, avoidance of inrush currents, and avoidance of resonances created by peripheral low frequency current sources [13]. Size reductions in the order of 65% and cost reductions in the order of 30% are predicted with capacitor rating estimated to be approximately 1/8th of that which would be used in a conventional SVC of equal rating [2].

The sensitivity of the ASVC's terminal voltage to external power system conditions is much lower [14]. Normally a SVC will become unstable when the external system capacity is comparable in rating to it, but the ASVC can maintain

a stable voltage on a system having only enough strength to supply its losses. Due to the fact that the voltage regulation of an ASVC can be designed for faster response than that of a SVC, the ASVC will perform much better during major transients, and as such will generally be of a lower rating than a SVC for a given performance objective. Both the SVC and ASVC configurations will generate undesirable harmonics, but the harmonics for GTO–based converters are expected to be lower than for the SVC of comparable rating. The reason being that converters are utilized in high–pulse–order applications, 24–pulse configurations are not uncommon. According to a recent EPRI–sponsored study [14], ASVC systems of high rating would benefit from even higher pulse orders.

In terms of the V–I characteristics of both types of devices of identical rating, the ASVC is capable of supplying full capacitive current at any system voltage down to the value of the small coupling reactance. This ability to support the system voltage is superior to that obtained with a conventional SVC system, which at full output becomes an uncontrollable capacitor bank, for which the current decreases in proportion to the voltage. The conventional system is not capable of increasing the var generation transiently since the maximum capacitive current it can draw is exclusively determined by the size of the capacitor and magnitude of the system voltage. Figure 3.11 illustrates the superiority of the ASVC in the transient rating in both inductive and capacitive operating regions over the conventional SVC. The system shown in Figure 3.11 is using GTO thyristors as the power switching devices.

It is evident from Figure 3.11 that the limitations for the magnitude and duration of the obtainable overcurrent in the inductive and capacitive regions are different. In the capacitive region the maximum continuous current is determined by the selected operating junction temperature and the corresponding current rating of the GTO thyristors.

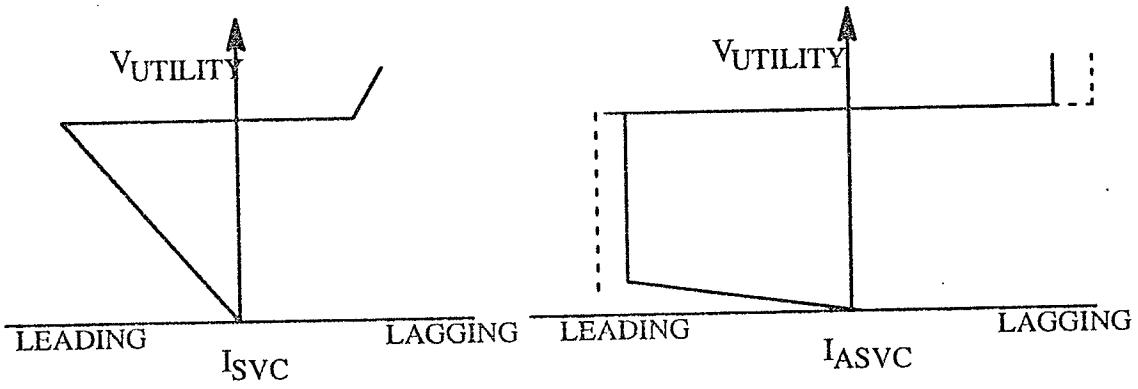


Figure 3.11: Comparison of V–I characteristics for SVC versus ASVC

The maximum transient capacitive overcurrent is determined by the maximum current turn–off capability of these devices. In the inductive region the GTO thyristors are naturally commutated and thus the transient current rating of the ASVC is limited only by the junction temperature at which the voltage blocking capability of the devices would begin to deteriorate. However, similar to the use of forced commutated converters for reactive power control, the use of GTO based systems for high power utility applications have not found acceptance due to their complexity [14]. With more research, and in view of the potential advantages which can be derived from the use of ASVCs, the prediction is that such systems will in time replace conventional SVCs. Other advantages include: unbalanced control; energy storage capacity; improved performance characteristics and limits; and improved performance during large power swings.

See [14] for more details.

3.6 Fault Performance and Protection Considerations in GTO Thyristor Converters

A careful study of the GTO thyristor's characteristics [15] will highlight the

fact that should a GTO converter be used in high power applications several protective features must be included in the controls in order to ensure proper performance and realize the advantages of Section 3.5. From the GTO's switching characteristics it is evident that some form of instantaneous overcurrent protection is necessary. Usually the instantaneous overcurrent in any GTO valve is controlled by monitoring the voltage drop across a small resistor in series with the GTO cathode lead, shown as rc in Figure 3.12, such that when this voltage exceeds a predetermined level (determined by the rating of the GTO valve) the gate drive circuit will take immediate action to turn the GTO off. An electric shutdown sequence will then follow, which causes all the GTO thyristors to turn off. The GTOs are prevented from receiving further on pulses until some manual re–set action is implemented. With a current sourced GTO converter in the case of an overcurrent all the GTO valves will be continually pulsed.

Control of the rate–of–rise of the GTO currents under fault conditions is also extremely important. In this case a fault current–limiting reactor, which consists of a free–wheeling diode in parallel with an inductor of proper rating, is placed in the dc side of the converter configuration before the switches. In normal operation the current in the inductor assumes the peak value of the ripple current in the dc capacitor and has no effect on the operation of the converter during this period. However should there be a sudden required increase in the GTO currents, the inductor will limit the rate of rise of these currents, providing adequate time for the overcurrent protection circuits to act and limit the maximum current (see Figure 3.12).

Since the GTO converter is a 3–wire device line–to–ground faults are of no major concern, however line–to–line fault protection must be considered. The path for a possible line–to–line fault current is shown in Figure 3.12. These line–to–line fault currents will cause high currents to flow through two GTOs in

series, hence the overcurrent protection circuitry and controls will act to interrupt the circuit.

With an ASVC a dc precharging circuit, shown in Figure 3.12, is used during the start–up sequence in order to prevent large transients when the line voltage is first applied. The dc precharging circuit is usually connected across the dc capacitor.

In [15] the GTO switches are protected from excessive heat sink temperatures by mounting a bimetal switch on the heat sink of the lower GTO in each pole. This acts in conjunction with the alarm signal circuit which is associated with the gate drive of the upper GTO thus ensuring that practically no dielectric stress is applied to the bimetal sensor although the heat sink voltage changes very rapidly with respect to ground.

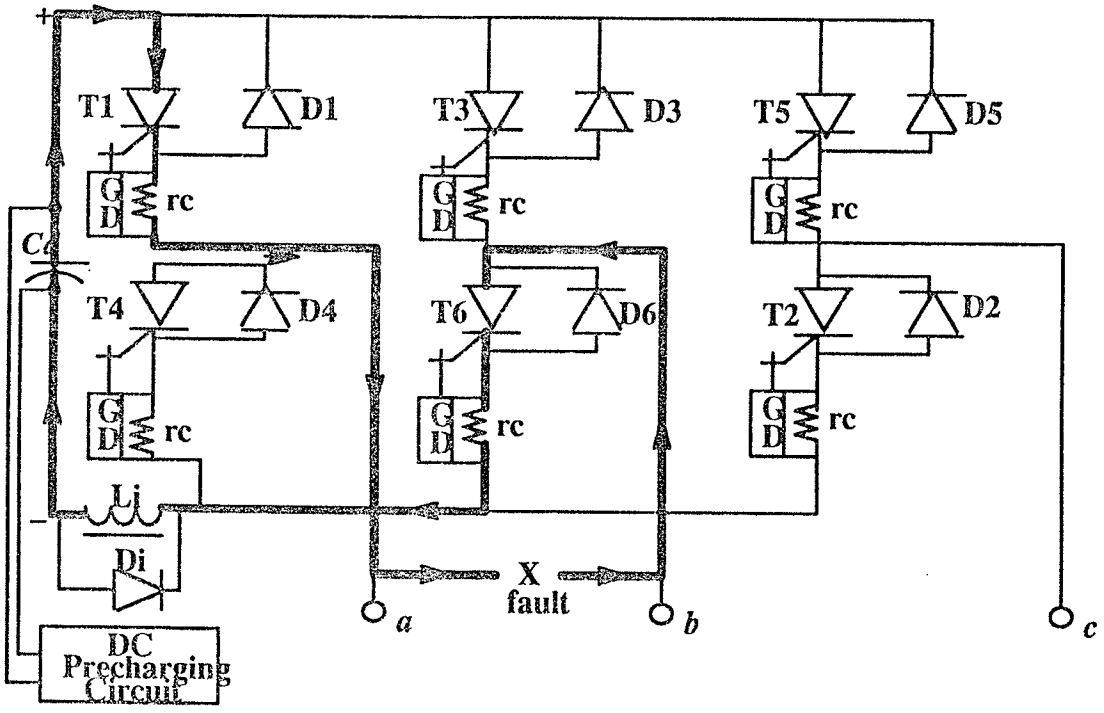


Figure 3.12: 6–pulse GTO converter showing current limiting reactor; the path of a typical line–to–line fault; and the dc precharging circuit

3.7 Chapter Summary

This chapter examines the use of ASVCs with GTO thyristors for balanced reactive power control. A few of the advantages derived from the use of GTOs as opposed to conventional thyristors, such as the increased switching speeds and no commutation circuitry requirements, are explored. The operation of both the CSI and VSI were examined and the observation was that the CSI can be viewed at the ac bus as a controlled current source whilst the VSI approximates a controlled voltage source. Connected to the dc side of the CSI is a large inductor whilst a dc capacitor is connected across the dc terminals of the VSI. Both inverters produced odd harmonics however the VSI lends itself more easily to PWM harmonic elimination techniques than the CSI because of the waveform symmetry stipulations in the CSI. A comparison is made between the operation of these two types of inverters when used as reactive power generators. The chapter concludes with a brief examination of the projected advantages of using ASVCs over SVCs and the fault performance of GTO based inverters.

Other conclusions which can be derived from this chapter includes:

1. For proper operation of a 6–pulse GTO VSI, freewheeling diodes are required antiparallel to each GTO valve. Freewheeling diodes are not required for the CSI but in order to avoid high stress across the GTOs at switching, capacitors must be connected across its ac output terminals;
2. The GTO switches used in each type of inverter are different. For the CSI the GTO switches should possess bidirectional voltage blocking capabilities whilst for the VSI they are required to possess only unidirectional voltage blocking capabilities;
3. For reactive power control both inverters must be synchronized to the ac system voltages. The amount of lagging or leading reactive power output from the CSI is controlled by setting the firing delay angle to either -90° or $+90^{\circ}$.

However the lagging or leading reactive power output of the VSI is controlled by varying the phase shift between the inverter's output voltages and those of the ac system;

4. For power factor correction both the CSI and the VSI can control the output imaginary positive–sequence current component linearly. Therefore they can both produce any magnitude of imaginary positive–sequence current in order to eliminate those due to the non–unity power factor load;

5. The VSI can be supplied on the dc side by a separate dc voltage supply or by a dc side capacitor. The first method is hardly ever used in reactive power control since it is uneconomical. The latter is predominantly used;

6. The projected advantages of using GTO based ASVCs as opposed SVCs were as follows:

i) decreased size and weight (approx. 65%) due to the replacement of large passive components with electronic chips:

ii) decreased costs (approx. 30%) as the cost of producing and successfully operating GTOs decrease with time:

iii) better harmonic performance due to the possibility of utilizing increased pulse number operation:

iv) the ASVC's ability to better support the system voltage since a conventional SVC at full output becomes an uncontrollable capacitor bank for which the current decreases in proportion to the voltage, whereas the V–I characteristic of the ASVC shows that it is capable of supplying full capacitive current at any system current down to the value of the small transformer reactance; and

v) the possibility of unbalanced control.

Chapter 4

GTO Converters with Pulse Width Control for Load Balancing and a Dual Bridge Load Compensation Scheme

4.1 Load Balancing

The concept of load balancing was introduced in Section 2.1.3 where it was stated that for an unbalanced three–phase load connected to a three–phase ac power system, the unbalanced operation results in unbalanced currents which results in components of current in the negative phase sequence. In an attempt to solve this problem, a load balancing device will be connected in parallel with the unbalanced load, resulting in this load appearing to the remainder of the power system, to be a balanced three–phase load. This chapter will utilize as the basis for load balancing, a method whereby the load balancing equipment will be capable of generating unbalanced currents which will produce a negative–sequence current component of an equal magnitude and opposite polarity to that which results from the presence of the unbalanced load on the system. The vector sum of these should result in balanced three–phase currents and hence zero negative–sequence current.

The general techniques such as Pulse Width Control (PW) which are useful in the application of load balancing control along with their associated limitations and implementation problems will be examined. Due to the fact that the value of the negative–sequence load currents are critical, a method for effectively

measuring these currents will be examined along with the necessary controls. Finally, a system will be simulated for the purpose of confirming the proposed theories and potential limitations.

4.2 The Application of Pulse Width Control to a GTO Current Sourced Inverter

In examining the operational characteristics of a GTO current sourced inverter (Section 3.2.1), it was observed that in normal operation, that is with self commutation, the inverter produces well balanced three–phase currents. The PW control is designed to modulate these inverter output currents such that the fundamental frequency negative–sequence current in the load is brought to zero, leaving only the positive–sequence current. With the utilization of the power factor correction techniques which were developed in Chapter 3, the imaginary component of the positive–sequence current can be eliminated. Therefore the supply bus is called upon to deliver only real positive–sequence currents to the now apparently balanced and purely resistive load.

4.2.1 Modulation of the Firing Angles of the Current Sourced Inverter

With reference to Figure 3.1, it was observed that in normal operation of a GTO–based CSI, the firing angles are equally displaced between the three phases as α_a, α_b, and α_c for phases a, b, and c respectively. Normally

$$\alpha_a = 30^o \qquad \alpha_b = 150^o \qquad \alpha_c = 270^o \tag{4.1}$$

and α_a', α_b', and α_c' are given by equation (3.1). For the modulation of the firing angles, a sinusoidal modulating signal of the form

$$\Delta\alpha = M \sin (2wt + \delta) \tag{4.2}$$

where M is the magnitude, w is the system radian frequency and δ is the phase shift, is proposed. Under this modulation scheme the new firing angle becomes

$$\alpha = \alpha_o + \Delta\alpha \tag{4.3}$$

In a practical system the firing pulses to the six valves are given in a sequence of α_a, α_c', α_b, α_a', α_c, α_b', displaced by 60°. If α_o is assumed to be 30° for phase a, then in one cycle the six produced firing angles can be expressed as

$$\begin{aligned}
\alpha_a &= 30^o + M \sin (0^o + \delta) \\
\alpha_c' &= 90^o + M \sin (120^o + \delta) \\
\alpha_b &= 150^o + M \sin (240^o + \delta) \\
\alpha_a' &= 210^o + M \sin (0^o + \delta) \\
\alpha_c &= 270^o + M \sin (120^o + \delta) \\
\alpha_b' &= 330^o + M \sin (240^o + \delta)
\end{aligned} \tag{4.4}$$

This method of modulation enables the production of the necessary unbalanced three–phase currents which results in the availability of a variable negative sequence current component.

The firing angle is modulated by the second harmonic of the system frequency for the purpose of ensuring that the positive and negative current pulses are identical, therefore no even harmonics are produced. By modulating α_a, α_b, and α_c with different values of $\Delta\alpha$ the imbalance necessary to generate the negative–sequence currents can be produced. With a source of negative–sequence current in parallel with the load, unique combinations of M and δ can produce a negative–sequence current which is equal and opposite to

that which is caused by the load imbalance. $\Delta\alpha$ for the different phases can be obtained at the zero crossings of the respective phase.

By the application of Fourier analysis, the relationship between the negative–sequence current and the modulation variables M and δ can be found (see Appendix A). Results show that the phase angle ϕ_2 of the negative–sequence inverter current can be controlled by varying δ (M = constant) whilst the magnitude $|I_2|$ is controlled by varying M (δ = *constant*). Figure 4.1(a) shows the relationship between ϕ_2 and δ and Figure 4.1(b) shows the relationship between $|I_2|$ and M.

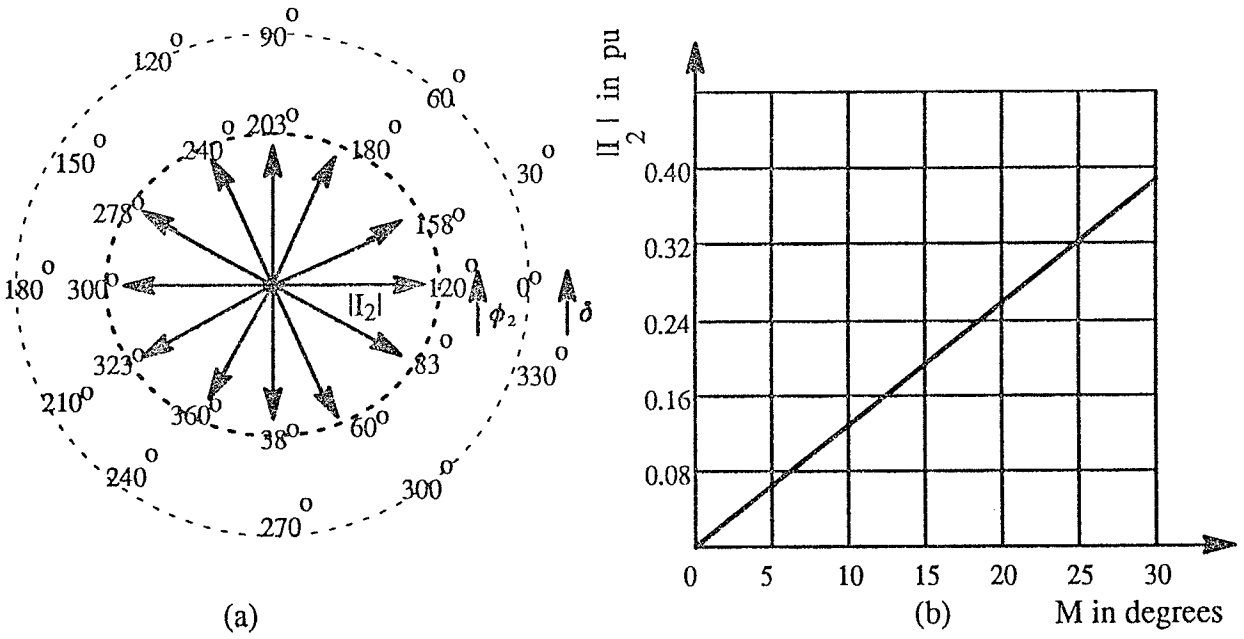


Figure 4.1: Produced negative–sequence current due to the PW–controlled CSI (a) ϕ_2 vs δ (M = constant) (b) $|I_2|$ vs M (δ = constant)

Results show that ϕ_2 can be varied from 0° to 360° by varying δ while keeping M constant and there is a linear relationship between $|I_2|$ and M with δ kept constant. There is also a slight variation in ϕ_2 as M changes and likewise in $|I_2|$ as δ is varied, although this is not reflected in the presented results and will not

seriously affect the performance of the system. The practical limit on the modulation variable M is 30°. Figure 4.2 is an illustration of the effect the modulation control has on the CSI's switching waveforms as compared to that of Figure 3.1 in Chapter 3 where there is no sinusoidal modulation (M = 0°, δ = 0° and I_2 = 0 pu). Figure 4.2(a) illustrates the case where the load imbalance, defined as the ratio of the magnitude of the negative sequence current on the load to the magnitude of the positive–sequence current on the load expresses as a percentage, is 10% with the required negative–sequence current being $0.12\angle 5.6°$ pu. To generate the required unbalanced currents the value of M and δ derived from the sinusoidal modulation scheme is –8.013° and 65.075° respectively. In Figure 4.2 (b) the percentage load imbalance is 20% , the required negative–sequence current is $0.28\angle 46.415°$ pu and for this case the value of the modulation variables are M = –22.574° and δ = –70.375°.

4.2.2 The Modulation Control Scheme

The control scheme in such a system would require a speedy method by which the three–phase load currents can be sampled, transformed into their symmetrical components, the information then fed to a control system which can apply the appropriate modulation to the inverter's firing logic control structure such that the load imbalances can be rapidly eliminated. An example of such a closed–loop control scheme is shown in Figure 4.3. The controller can be divided into a Modulation Control block and a Measurement block. In this section the Modulation Control block will be discussed whilst the Measurement block is the subject of Section 4.2.3.

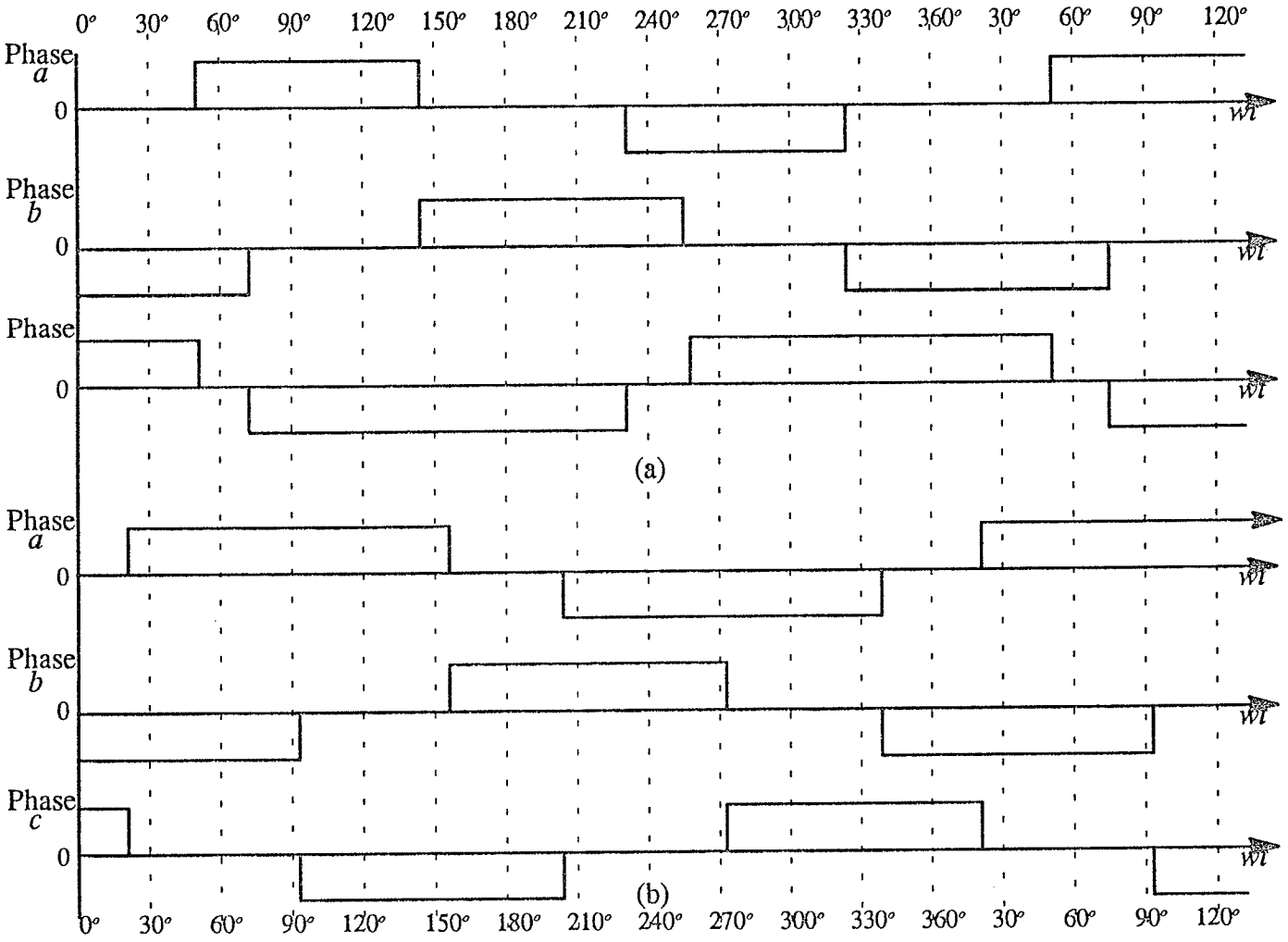


Figure 4.2: Switching waveforms for the PW–controlled CSI (a) Load imbalance = 10%, $I_2 = 0.12\angle 5.6°$ pu, M = –8.013° and $\delta = 65.075°$ (b) Load imbalance = 20%, $I_2 = 0.28\angle 46.415°$ pu, M = –22.574° and $\delta = -70.375°$

The modulation control block consists of one real–pole type filter and one Proportional Integral (PI) type regulator for each dc component representation of the real and imaginary parts of the measured negative sequence current phasor, and the necessary controls for generating the modulation signal $\Delta\alpha$ from the output of the regulators. The real pole type filter is not necessary to eliminate ripple, but allows for averaging the measured signal over several cycles. This is beneficial when the dc component is the control parameter. The regulator outputs

CRE = $M\cos\delta$ and CIM = $M\sin\delta$ represent the real and imaginary parts respectively of the modulation signal phasor. These signals along with the auxiliary signals sin $(2wt)$ and cos $(2wt)$ which are derived from the phase locked loop, can be used to generate the modulation signal which will be of the form shown in equation (4.2). The reference values for the PI regulators are set to zero, therefore the feedback system will force both real and imaginary negative–sequence current components to zero.

4.2.3 The Sequence Component Measurement Block

In order to achieve effective PW control the negative sequence current components must be measured in instantaneous values. According to measurement techniques introduced by Mausel and Waldman [16] and Menzies and Mazur [12] this can be achieved with the use of two coordinate transformations: the three–phase (A, B, C) to two–phase (α, β); and the symmetrical component ((α, β)–to–(0, 1, 2)) transformation. The (A, B, C)–to–(α, β) transformation is a scalar transformation and as such applies to instantaneous values of current and voltage as well as phasor values. But the symmetrical component transformation is a vector transformation, therefore in order to apply it to instantaneous signals, the (α, β) component must be transformed into their phasor or stationary vector equivalents. In [16] the transformation is accomplished in two stages. The first stage uses a Vector Identifier block (VI), usually realized in an analog circuit by a time delay circuit, which transforms the instantaneous (α, β) components into rotational vectors. In the second stage the rotational vector is converted into its stationary vector equivalent by multiplying the rotational vector by the complex conjugate of the reference positive–sequence voltage.

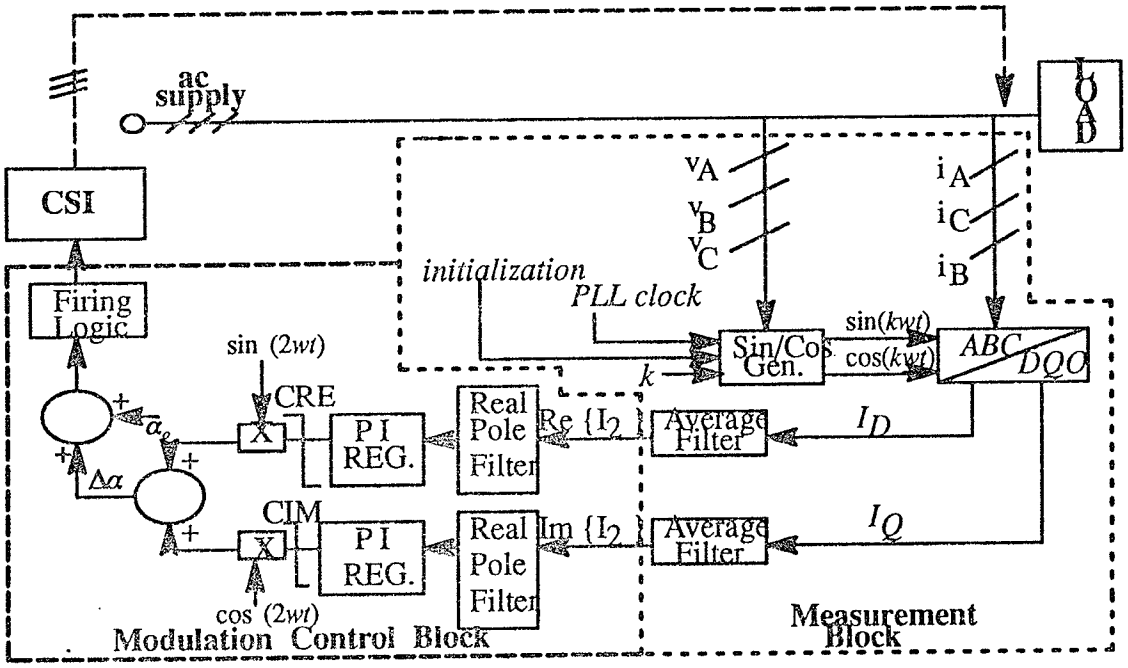


Figure 4.3: Closed loop control with Modulation Control block and Measurement block

The logic of these two stages is that should an observer be rotating with the reference vector he would measure the similarly rotating vectors $i_\alpha(t)$ and $i_\beta(t)$ in the forms of $\sqrt{2}\ I_\alpha$ and $\sqrt{2} I_\beta$ respectively. The phasor representations can then be transformed easily into the symmetrical components representation using equation (4.5) below.

$$I_2 = \frac{1}{2}\left[I_\alpha - j\, I_\beta \right] \tag{4.5}$$

However, with this method of vector identification the measurement is based on the assumption of constant fundamental frequency and will produce inaccurate results in the existence of frequency fluctuation. The method used in Figure 4.3 and presented in [12] proposes a method of vector identification which can operate effectively even in cases of frequency variation. Here a Phase Locked

Loop (PLL) is locked to the fundamental positive–sequence system voltage which is used as the phasor reference. The PLL will follow fundamental frequency excursions. With this method of vector identification the controller can use the PLL reference in order to produce other reference phasors at harmonic frequencies. The equivalent negative–sequence phasor is given as:

$$\begin{bmatrix} \mathrm{Re}[I_2] \\ \mathrm{Im}[I_2] \end{bmatrix} = \begin{bmatrix} \cos(kwt) & -\sin(kwt) \\ -sin(kwt) & -cos(kwt) \end{bmatrix} \begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} \tag{4.6}$$

where for both methods $i_\alpha(t)$ and $i_\beta(t)$ are obtained from the instantaneous values of the three–phase line currents according to the relationship shown below:

$$\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{4.7}$$

Here the ground phase component is neglected because no zero–sequence current components exist in the systems which are being considered in this thesis. The integer k determines the harmonic component that is measured. If $k = 0$ the dc component is measured. If $k = 1$ the fundamental component is measured and so on. Here w is the system's angular frequency. Equation 4.6 is equivalent to the (A, B, C)–to–(D, Q, O) transformation in electric machines analysis, which resolves three–phase currents of frequency w in fixed–axis windings into equivalent direct currents in commutator windings. The sequence components which are measured can be represented as I_D and I_Q which represents the in–phase and quadrature components respectively of the line currents. I_D and I_Q require filtering as they contain sinusoids of various frequencies as well as the values of $\mathrm{Re}\{I_2\}$ and $\mathrm{Im}\{I_2\}$ as dc values. An averaging filter using samples over a complete fundamental frequency cycle is used to eliminate all sinusoidal components. The remaining dc values can then be used as the input control

variables for the respective PI regulators. A similar measurement block can also be used for positive–sequence current components except for the fact that inputs i_B and i_C to the A,B,C–to–D,Q,O block must be interchanged. Usually the reference inputs to the PI regulators are set to zero thereby rapidly forcing the measured sequence current components to zero.

4.3 Problems Associated with the Use of Pulse Width Control in a CSI for Load Balancing

4.3.1 The Third Harmonic Problem

The phase currents as defined for the three–phase inverter are the same as those in a single–phase inverter, and include a third harmonic component of one–third the amplitude of the fundamental component. The third harmonic does not appear however, in the interphase output currents, since these currents are composed of pairs of phase currents added with a phase displacement of $\frac{\pi}{3}$ at the fundamental frequency and therefore of π at the third–harmonic frequency. The whole series of triplen harmonics is similarly eliminated.

The characteristic harmonics produced by three–phase converters were discussed, however in performing the calculations for their determination several assumptions were made. These included the assumption of equal spacing of the firing pulses and a smooth dc current which is achieved by assuming the existence of an infinite inductance connected to the dc terminals of the inverter. Since the implementation of PW control involves unbalanced CSI operation, the above assumptions can no longer aid in the determination of the harmonic content of the output current waveforms of such a non–ideal system. In [17] several

non–ideal conditions along with their effects on the output waveforms of the power converter are examined, results show that with the presence of an unbalanced three–phase ac load, the converter will supply into the load, large amounts of third harmonic current. Also it can be shown that the magnitude of the characteristic harmonics which are generated, are different from those generated under ideal conditions.

In this thesis only the third harmonic problem will be considered in any detail, since results obtained from simulations of the PW control scheme show that the third harmonic current increases linearly with the degree of imbalance as well as with the increase in size of the converter. Now even if the third harmonic current which is generated is only part of a percentage, it would probably be unacceptable within normal limits of harmonic tolerance and would definitely affect any ac harmonic filter design. Since the PW scheme produces unbalanced inverter currents as previously explained, the third harmonic currents in the three phases do not have the same magnitude and phase angle and as such are not eliminated during normal operation. For the same reason, delta–connected transformers prove ineffective in eliminating the third harmonic currents.

Physically, the PW control scheme used here effectively 'compacts' and 'expands' the three–phase output current waveforms of the CSI by a different value of $\Delta\alpha$ in each phase. The degree of modulation, which is proportional to the net difference between the width of the pulse after modulation and the width before modulation (during balanced operation), can be expressed as $(\Delta\alpha_b - \Delta\alpha_a)$ for phase a. Similar expressions will represent the modulation degree for phases b and c. Table 4.1 shows the ratio of the magnitude of the 3rd, 5th, 7th, 11th, 13th, 17th and 23rd current harmonics to the fundamental (assumed equal to 1.0 pu) as the absolute value of the degree of modulation is varied from 0° to 30°. The effects of varying the degree of modulation on the magnitude of the third

current harmonic is presented in graphical form in Figure 4.4.

Results confirm the linear relationship between the 3rd harmonic and

$(\Delta\alpha_b - \Delta\alpha_a)$.

4.3.2 Establishment and Maintenance of the Input DC Current Level in the CSI

In normal balanced operation, that is with no modulation of its firing angles ($\Delta\alpha = 0$), the current sourced inverter produces no negative–sequence current only a real positive–sequence current which is proportional to the dc side input current.

Table 4.1: Ratio of the magnitude of the current harmonics to the fundamental as a function of $|(\Delta\alpha_b - \Delta\alpha_a)|$

$\lvert(\Delta\alpha b - \Delta\alpha a$ degrees	I3 (pu)	I5 (pu)	I7 (pu)	I11 (pu)	I13 (pu)	I17 (pu)	I23 (pu)
0	0	0.2	0.14	0.09	0.08	0.06	0.04
4.33	0.04	0.22	0.12	0.11	0.05	0.07	0.05
8.66	0.09	0.24	0.09	0.10	0.01	0.05	0.02
12.99	0.14	0.25	0.04	0.08	0.04	0.01	0.03
17.32	0.19	0.25	0.00	0.05	0.08	0.03	0.05
21.65	0.24	0.24	0.05	0.00	0.10	0.07	0.04
25.98	0.29	0.22	0.1	0.05	0.10	0.08	0.00
30.00	0.34	0.20	0.15	0.09	0.07	0.06	0.05

This is not surprising since the total output power from the ac side of the inverter must be equal to the total input power from the dc side less the I^2R losses in the switching devices.

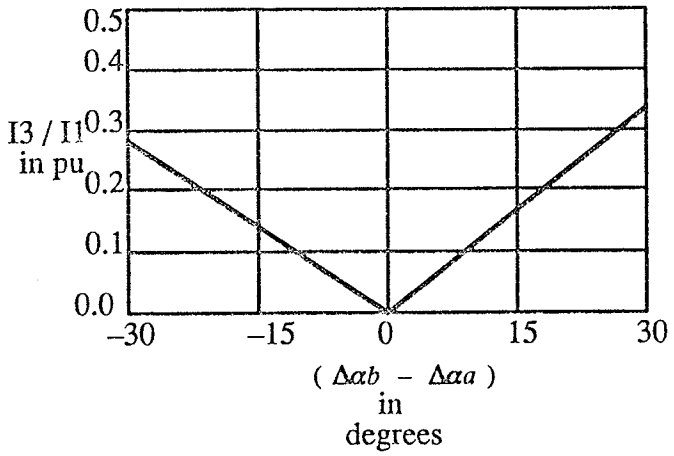


Figure 4.4: Magnitude of the third current harmonic vs ($\Delta\alpha_b - \Delta\alpha_a$)

During load balancing operation however, no real power transfer is required between the load and the PW–controlled CSI, and similar to its operation in providing balanced reactive power control, the mean output dc voltage of the CSI is theoretically zero.

When the CSI is operating as a purely reactive power source in the case of a balanced three–phase load, the required dc current in the inductor is maintained by adjusting the firing delay angle to be slightly less than 90°, so that apart from the required reactive power there is adequate dc voltage established across the inductor. In a practical system the firing delay angle is adjusted even further in order to establish just enough dc voltage to overcome the thyristor voltage drops and resistances of the inductor and the ac system. In the PW–controlled CSI the establishment and maintenance of the required dc current levels in order to derive appropriate amplitudes of the unbalanced inverter output currents for load balancing, is more complicated. Due to the nature of the modulation control scheme where the firing angle α in each phase is modulated by a different value of $\Delta\alpha$, it is much simpler to maintain the input dc current level in the inductor and compensate for inverter losses by utilizing a separate dc current controller.

In Chapter 2 the theory of load compensation dictated that enough reactive

current must be generated in order to improve the power factor of the compensated load to unity and appropriate unbalanced currents for balancing the load. Since the PW–controlled CSI at this stage will be used for load balancing (negative–sequence bridge) only, the inclusion of a separate bridge for establishing and maintaining the dc current levels in the negative–sequence bridge along with the power factor correction (positive–sequence bridge) will result in a fairly large system which would be uneconomical. One possible solution to the problem of controlling the dc current levels could be realized by employing the positive–sequence bridge. The possibility of utilizing such a system will be examined in Section 4.5.)..

4.4 Application of Pulse Width Control to Voltage Sourced Inverters

It is the aim of this section to briefly examine the suitability of the PW control scheme to VSIs. The PW control algorithm will be identical to that which was presented in Section 4.2.1. In this case however, the VSI must be tied to the ac system by a suitable tie–reactance as explained in Chapter 3. The unbalanced currents I*a*, I*b*, and I*c* can be represented by equation (3.7) except for the fact that in this case PW control will be applied to the GTO voltage sourced inverter. Measurement of the positive– and negative–sequence currents will be done according to the method presented in Section 4.2.2. The evaluation of the VSI with PW control as an effective load balancing system will be based on two factors: (1) whether control of the output currents can be achieved for a full cycle as is the case with the PW controlled CSI; and (2) the effect such a system will have on the power factor of the load if used along with a power factor correction system in load compensation.

4.4.1 Controlling the Output Currents in the VSI

If the method of current control in both the GTO CSI and GTO VSI are examined, the observation is that the degree of controllability, that is the ability to exercize effective control over the currents in each phase, will be much less for the VSI than for the CSI. In the GTO CSI, because there must be a continuous flow of current from the input current source, two GTO valves must be in conduction at all times, one from the upper set and one from the lower. In the event that the current is to be switched from one phase to another, it is interrupted by the outgoing valve of the conducting phase and diverted to the other phase by the incoming valve. Since the switching is done at very high speed, the capacitors which are usually connected across the inverter's output terminals serve as energy absorbers thus relieving the stress on the outgoing valve due to the inductance in the circuit. Therefore because the valves can be gated at any instant of time irrespective of the existing voltage, the application of PW control to the GTO CSI results in an extremely high degree of controllability for the full range of inverter operation.

Unlike the CSI, the switching of the GTO valves and hence the flow of current in each phase of the VSI is not independent of the existing voltages. This means that the GTO valves in the VSI cannot be switched at any time as determined by the controls. In this case, with reference to Figure 3.5, the antiparallel free–wheeling diodes are required to carry the phase currents for periods of the conduction cycle. Figure 4.5 illustrates the current conduction sequence for phase *a* of the VSI, usually the conduction period for each GTO valve is 120°. Initially the current in phase *a* is carried by thyristor T1, when T1 switches off, because of the inductance in the circuit, the current is positive and lags the voltage and is therefore carried by diode D4 until T4 is gated into conduction .

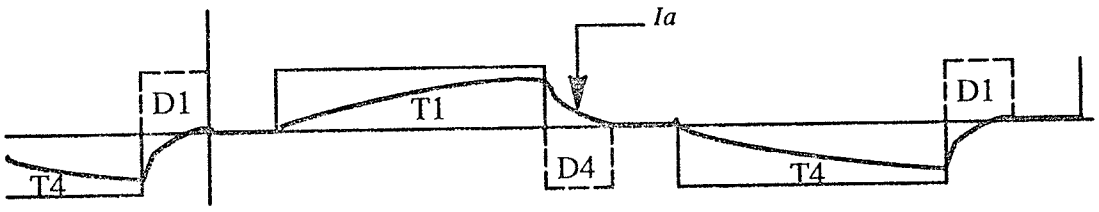


Figure 4.5: Current control in the GTO VSI

When T4 is switched off the current is now carried by diode D1 until T1 is switched on again. When PW control is applied to the GTO VSI, the degree of controllability is much less, this due to the period where the current is carried by the free–wheeling diodes and as such cannot be controlled by firing angle modulation. Since the unbalanced currents in the VSI cannot be controlled for the full range of operation this system will prove to be inadequate for balancing unbalanced three–phase loads.

4.4.2 The Generation of Imaginary Positive–Sequence Currents

According to Chapter 2 an effective load balancing system should produce only the necessary unbalanced currents which are required in order to produce the correct levels of negative–sequence currents required for the cancellation of those which are present on the load. With the PW controlled VSI for every level of required negative–sequence current which is produced a purely imaginary component of positive–sequence current which is directly proportional to the amplitude of the output voltage of the inverter is also produced. Figure 4.6 (a) shows the magnitude of the imaginary positive–sequence current $\mathrm{Im}\{I_1\}$ produced as a function of δ and Figure 4.6 (b) shows the magnitude of the

produced imaginary positive–sequence current $\mathrm{Im}\{I_1\}$ as a function of M. It is evident that although $\mathrm{Im}\{I_1\}$ is directly proportional to the amplitude of the output voltages of the VSI, modulation variable δ also has a small effect and M an even greater effect.

The presented results show that a PW controlled VSI cannot be used for load balancing since it worsens the power factor of the load and compensator. Alternatively if the imaginary positive–sequence current from the PW controlled VSI could be controlled by other means, then the VSI will be capable of both load balancing and power factor correction which will eliminate the requirement for separate positive–sequence and negative–sequence current controllers.

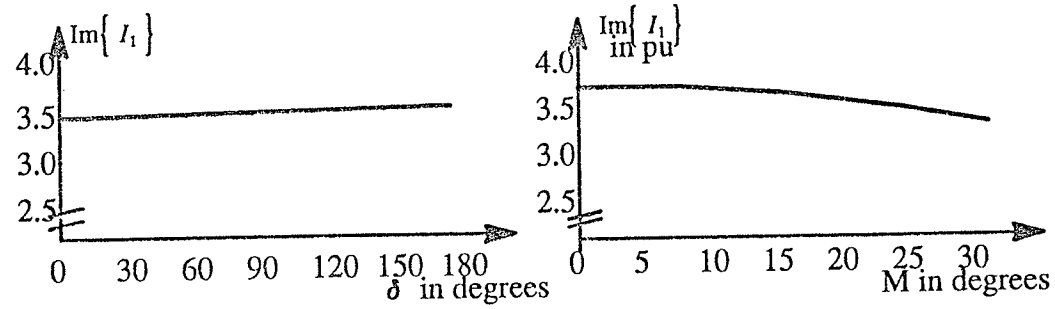


Figure 4.6: (a) $\mathrm{Im}\{I_1\}$ as a function of δ (b) $\mathrm{Im}\{I_1\}$ as a function of M

The operation of such a system will be similar to the load compensation systems which were presented in Section 2.3.

In Chapter 3 when the VSI was considered for balanced reactive power control, it was evident that unlimited control of the imaginary component of the positive–sequence current required only that the amplitude of the inverter's output phase voltages be appropriately increased or decreased with respect to the amplitude of the corresponding system's line–to–neutral voltages and that these voltages be in phase. Therefore if a single 6–pulse VSI is to be considered for compensating a three–phase unsymmetrical load, the required controller must be capable of appropriately adjusting the amplitude and phase shift angle of the

VSI's output voltage in each phase by unequal amounts thus producing purely reactive power and unbalanced currents in the transformer reactances for balancing the three–phase load. In Chapter 5 such a system is presented. This system uses SPWM control of the VSI's output voltages.

4.5 A Load Compensator with Separate Positive– and Negative–Sequence Current Controllers

In this section the practical usefulness of a load compensator which utilizes separate power–factor correction (positive–sequence bridge) and load balancing systems (negative–sequence bridge) will be determined. The aim is to determine if this load compensator arrangement can satisfy the load compensator requirements as outlined in Chapter 2 in terms of effectively compensating various types of loads and accomplishing this within two to four cycles of the systems fundamental frequency. Here the positive–sequence current controller will be of the configuration presented in Chapter 3 whilst the negative–sequence current controller will be of the configuration presented in the earlier sections of this chapter. With such an arrangement there exists four possibilities which are summarized in Table 4.2.

Table 4.2 ; possible combinations for the dual bridge load compensator

Arr. #	Positive–sequence bridge	Negative–sequence bridge
1	VSI	VSI
2	CSI	VSI
3	VSI	CSI
4	CSI	CSI

According to the discussion of Section 4.4 the VSI with PW–control is unsuitable

for load balancing therefore arrangements #1 and #2 of Table 4.2 are eliminated and because of the requirement outlined in Section 4.3.2 where the positive–sequence bridge is required to establish and maintain the appropriate levels of dc current in the negative–sequence bridge the third possibility is impractical. Therefore the only possibility worth exploiting is case 4 where both bridges are of the current sourced type.

4.5.1 The Concept of Operation

The load compensator arrangement will be as shown in Figure 4.7 and component values are given in Appendix B. In normal operation the firing angle in the positive sequence bridge will be 90° and for providing lagging vars the inverter's input ac current will lag the corresponding ac system voltage by 90°. For providing leading vars the inverter's output current must lead the corresponding ac voltage by 90° and the outputs of the inverter must be shunted by three–capacitor banks. In both cases the mean output dc voltage is theoretically zero since no real power transfer is involved. However in order to establish and maintain the required dc current in the inductor for both bridges the firing delay angle must, in practice, be slightly less than 90° so that there is just enough dc voltage to overcome the thyristor voltage drops and the resistances of the inductor and the ac system. Therefore the magnitude of the dc current and the corresponding amplitude of the resultant ac line currents in both bridges can be controlled by an adjustment in the firing delay angle around 90°. Filters for the characteristic harmonics along with a third–harmonic filter is required at the ac terminals of the negative–sequence bridge according to the discussions of Section 4.3.1

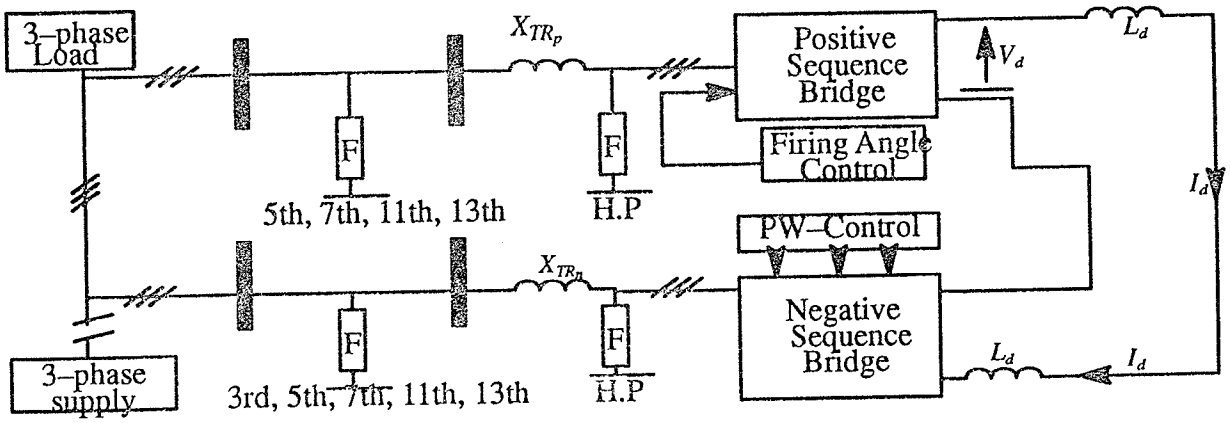


Figure 4.7: Dc current control with positive–sequence bridge

4.5.2 The Control Structure

The simulated control structure for the dual bridge load compensator is presented in Figure 4.8. Here the PW–control block for the negative–sequence bridge is similar to that of Figure 4.3 except that the operation of the measurement block in this case is represented by calculations in the digital simulation using EMTDC and is therefore excluded. The controls for the positive–sequence bridge consists of a PI regulator whose measured input signal is the imaginary positive–sequence current and whose reference signal is set to zero. Adjusting the firing delay angle α around 90° by PI control establishes appropriate levels of dc current in both bridges and forces the imaginary positive–sequence current components to zero . In a similar manner the PI controls for both components of the negative–sequence current will force these components to zero.

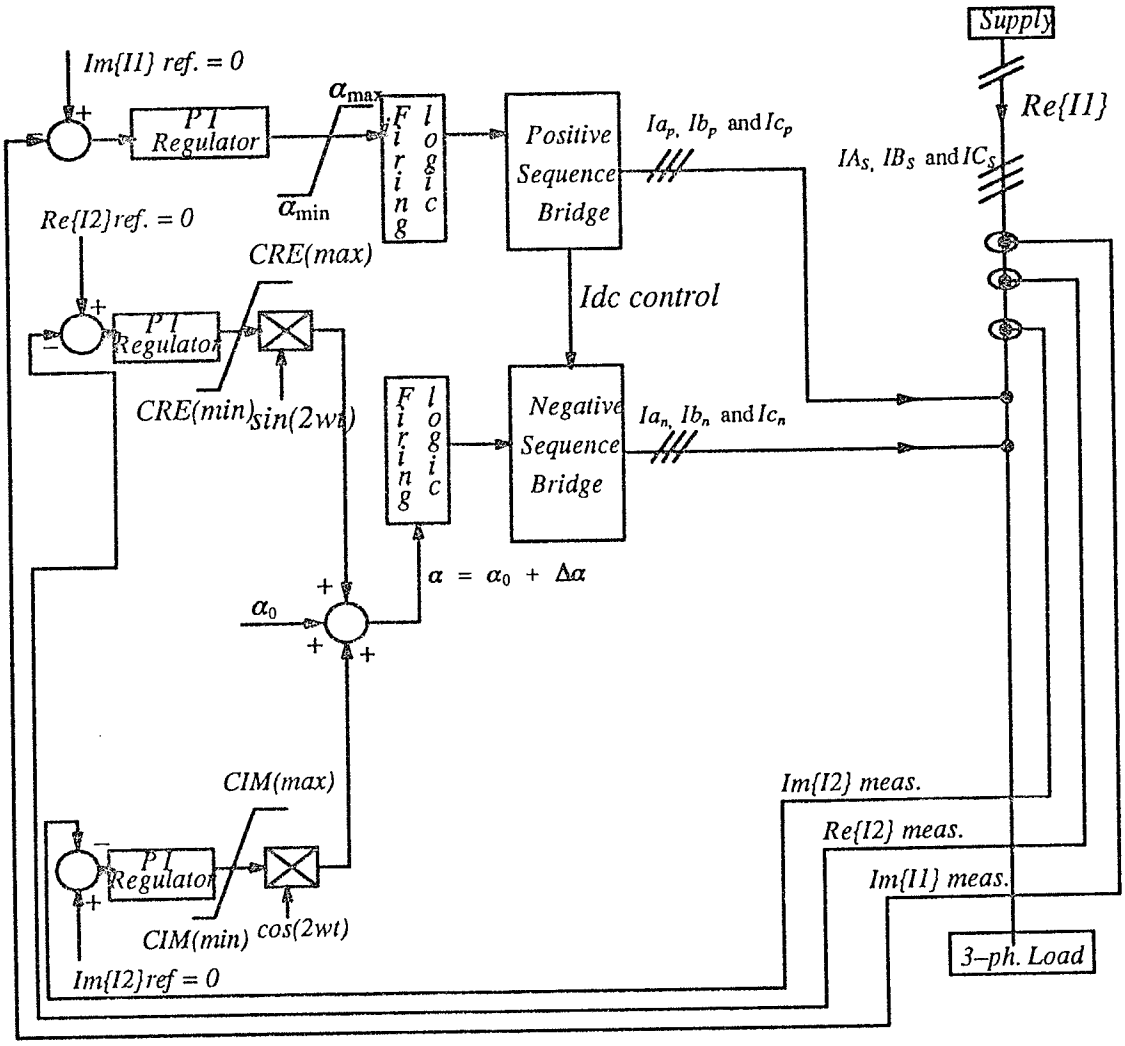


Figure 4.8: Control Scheme For Dual Bridge Load Compensator

4.5.3 Digital Simulations

The modulation control scheme for the negative–sequence bridge and the firing angle control scheme for the positive–sequence bridge are validated by the EMTDC simulation program on the simple system shown in Figure 4.9.

In this case the supply system voltages are assumed balanced and star–connected. The three–phase load is simulated as delta–connected with each phase represented by an impedance which consists of a variable resistive and a variable reactive component. Each CSI is modelled as three controllable current sources which produce only fundamental output currents (all harmonics are assumed to be

well filtered).

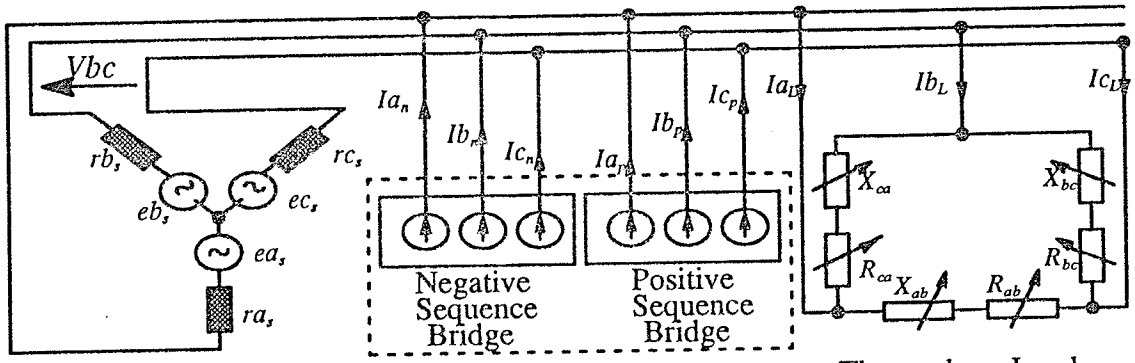


Figure 4.9: Simulated System

The simulation involved switching the load from a balanced unity power factor load to an unbalanced load with either a leading or lagging power factor and testing the ability of the controls to cause the bridges to generate appropriate unbalanced currents (negative–sequence bridge) and balanced currents (positive–sequence bridge) in order to :

a) eliminate the negative–sequence currents caused by the unbalancing effect on the system's line currents by the unbalanced load, and

b) the positive–sequence currents caused by the non–unity power factor load's demand for leading or lagging reactive reactive power.

In the steady–state the effects on the system of the unbalanced non–unity power factor load should be eliminated and the system should return to its pre–disturbance state.

CASE I

The load is switched from a balanced unity power factor one to a 20% unbalanced 0.8 p.f lagging three–phase load at time = 0.3 seconds. This time was chosen so that at the time of disturbance the system would have reached its steady state. The results for this case are presented in Figure 4.10.

CASE II

Here the load is switched at time = 0.3 seconds from its balanced unity power factor state to a 20% unbalanced 0.9p.f leading three–phase load. Results are shown in Figure 4.11.

In addition to the above two cases the system was simulated for case of a 40% load imbalance and 0.8 p.f lagging, and a 10% load imbalance with 0.9 p.f leading. Results for these cases are not presented since the performance of the load compensator under these circumstances was much similar to that of CASE I .

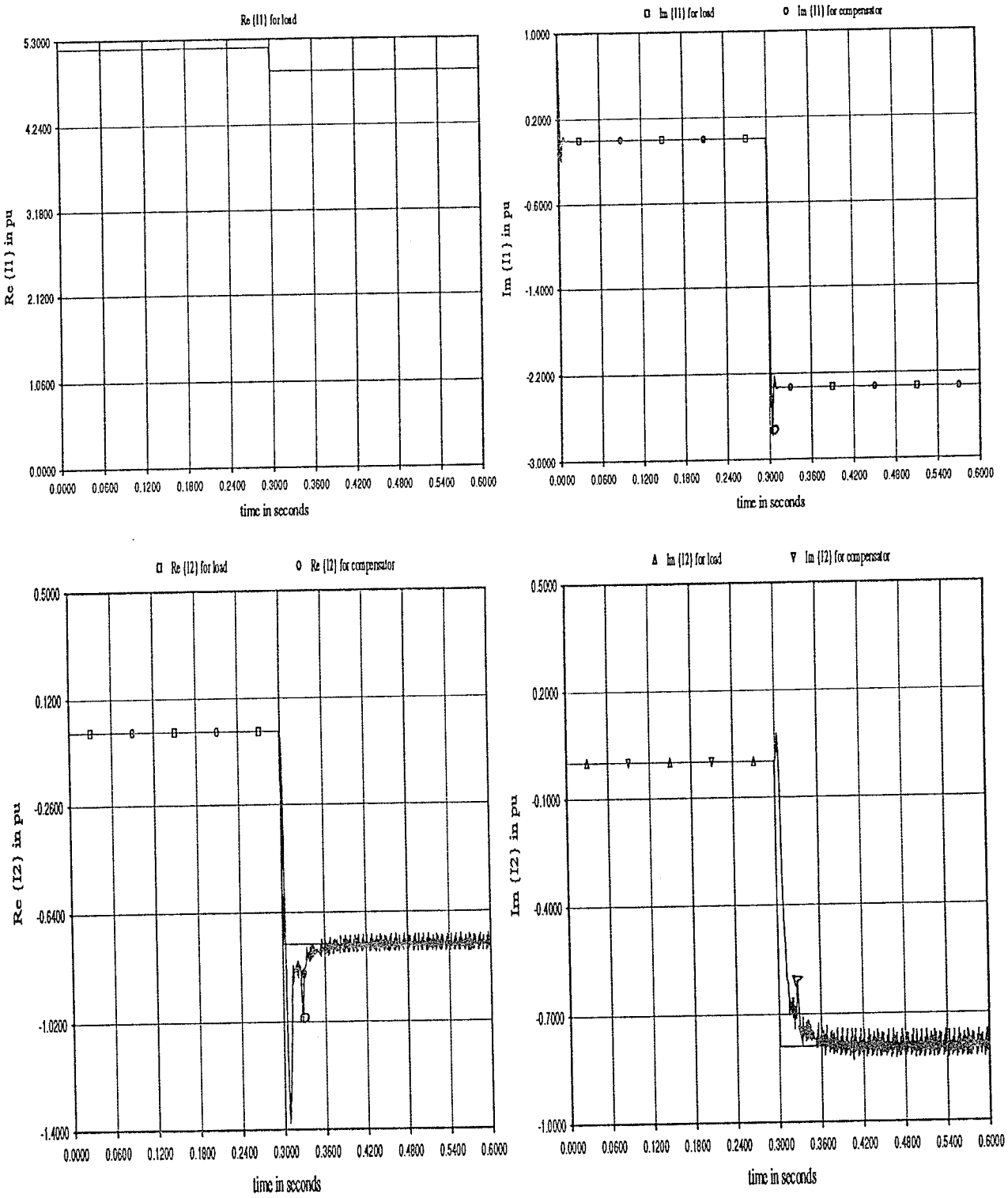


Figure 4.10: Operation of dual bridge load compensator for CASE I

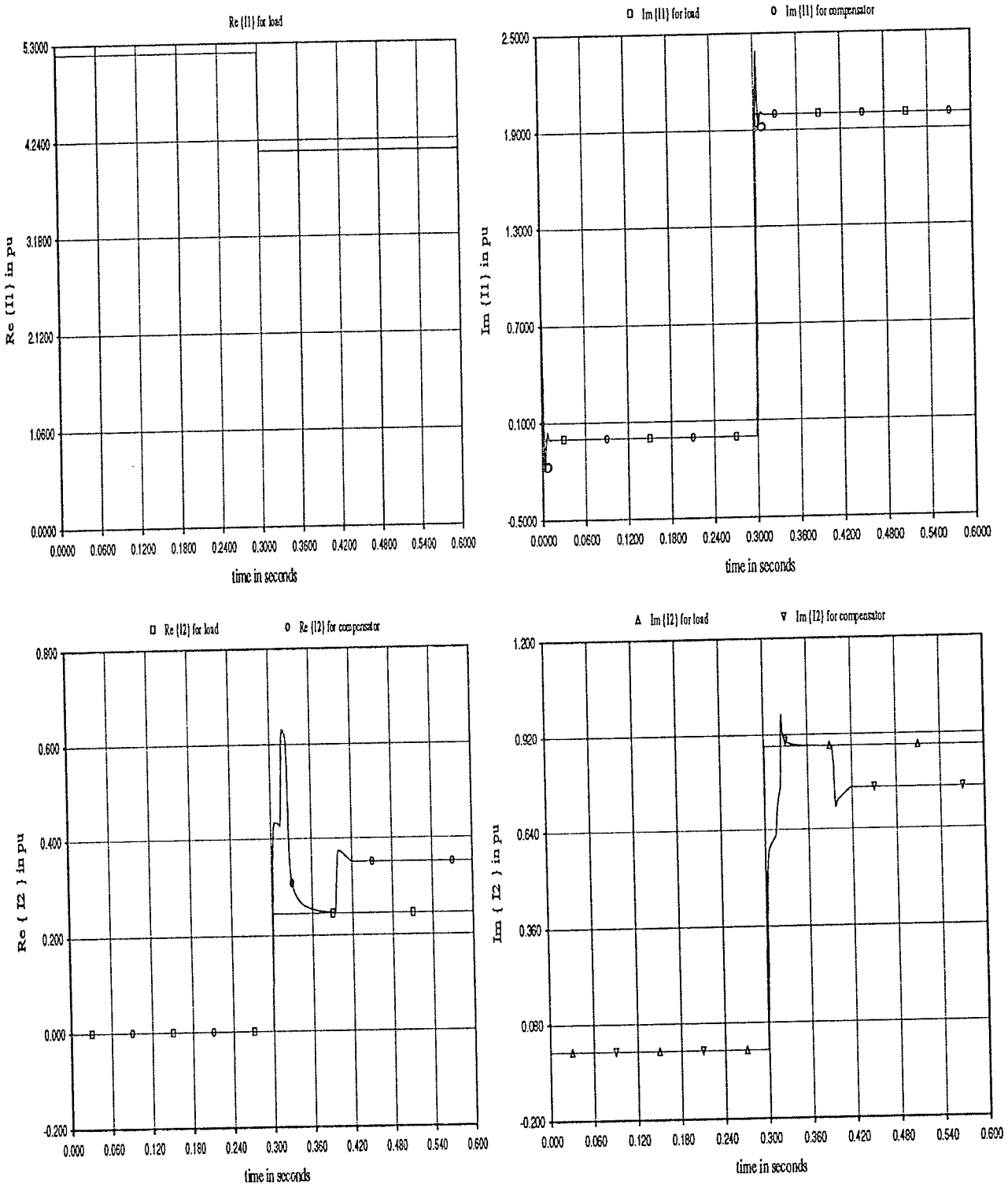


Figure 4.11: Operation of dual bridge load compensator for CASE II

4.5.4 Analysis and Discussion

- **Response Speed**

The results which were presented in section 4.5.3 show that the power factor correction aspect of the load compensation is accomplished fairly quickly (within 2 to 4 cycles) this due to the fact that the balanced reactive power control basically involved adjusting the firing delay angle of the positive–sequence bridge by means of a PI regulator. However the ability of the load compensator to balance the unbalanced load was a much slower process. In CASE I the load balancing is accomplished in about 7 to 8 cycles. The overall response time of this system will be much slower if the two bridges were to be modelled such that the firing times of the thyristors and the inherent delay in the inverter circuitry are taken into consideration. Also non–ideal switches will increase the dc losses and therefore the firing delay angle of the positive–sequence bridge will have to be adjusted even further in order to compensate for these losses. In CASE II the load compensator does not succeed in balancing the unbalanced load since the available dc input current is insufficient.

- **Range of Operation**

Due to the series connection on the dc side of the dual bridge compensator the required level of dc current in the negative–sequence bridge affects that of the positive–sequence bridge and therefore the range over which this system is operational is limited. The results from Figure 4.11 supports this fact and in this case instead of successfully compensating the load as in CASE I the load never balances, thereby proving that the range of operation of the dual bridge load compensator is quite limited.

From the above discussions it is fair to conclude that according to the definitions of an effective load compensator as outlined earlier, the load compensator which comprises separate positive– and negative–sequence bridges of the current sourced type is not effective over the desired range nor is its response speed fast enough in order to serve as a practical load compensator.

In Chapter 5 a load compensator which involves the use of PWM in a 6–pulse three–phase inverter of the voltage sourced type, will be designed, modelled and simulated.

4.6 Chapter Summary

In this chapter a novel modulation scheme for controlling the pulse widths in each phase of the CSI was introduced. The PW control scheme was based on the use of a sinusoidal modulating signal of the form $M \sin (2wt + \delta)$ and it was found that the magnitude of the output negative–sequence current component for load balancing could be controlled linearly by varying the modulation variable M whilst the phase angle could be controlled from 0^o to360^o by varying δ. Modulation with the second harmonic of the system frequency ensured no even harmonics were produced. Also the use of VIs for accurately measuring the sequence current components from the instantaneous system quantities was explained. The need for two transformations was stressed. The first transformation, referred to as the three–phase–to–two–phase transformation, is a phasor transformation and could therefore be applied directly to the instantaneous quantities. The second transformation, referred to as the symmetrical components transformation, is a vector transformation which required the transformation of the instantaneous quantities first into their rotational vector equivalents then into the equivalent stationary vector or phasor quantity. These two stages were accomplished by using a VI.

The PW control scheme was then applied to a VSI and the result showed that full control for the entire range could not be achieved. Finally a load compensator which is based on a combination of a positive–sequence current controller of Chapter 3 and a negative–sequence current controller of this chapter was designed and simulated on EMTDC and the results presented for two cases. This load compensator is referred to as the dual–bridge compensator.

Other conclusions which can be derived from this chapter includes:

1. For the PW control scheme, the use of separate PI regulators to adjust CRE ($M \cos\delta$) and CIM ($M \sin\delta$) resulted in independent control of the real and imaginary components respectively of the negative–sequence current;
2. The PW control when applied to the CSI resulted in the presence on the compensated system of a third harmonic current which is directly proportional to the net difference between the pulse width before and after modulation;
3. Due to the fact that for a period of its conduction cycle the currents in the VSI flow through the freewheeling diodes, the PW control could not be successfully applied to the VSI;
4. The dual–bridge load compensator proved to be quite limited in its compensation range. In this system the mean dc output voltage was theoretically zero since no real power transfer was involved. However in order to establish and maintain the required dc current levels, the firing delay angle of the positive–sequence bridge was appropriately adjusted;
5. The response speed of the dual–bridge load compensator is much slower than the TCR/FC type load compensators of Chapter 2.

Chapter 5

Analysis and Design of a Load Compensator using a PWM Voltage Sourced Inverter

5.1 Application of PWM to VSIs

5.1.1 The concept of operation

In Chapter 3 the basic operating principles of a VSI type ASVC for providing reactive power control to balanced three–phase loads was presented. A brief summary of those principles are as follows:

1) In order to generate or absorb purely reactive power it is necessary that the output voltage for each phase of the VSI be in phase with the corresponding system's line–to–neutral voltage and be tied to it via a small tie–reactance which is usually the leakage inductance of the transformer.

2) If leading reactive power is required the amplitude of the VSI's output voltage in each phase must be greater than that of the system by an appropriate amount as determined by the required reactive power demand.

3) If lagging reactive power is required the amplitude of the VSI's output voltage in each phase must be less than that of the system by an appropriate amount as determined by the required reactive power demand.

4) In normal operation with ideal power switching devices assumed, the inverter is operated strictly as a reactive power source and therefore absorbs no real

power from the ac system. In order to raise or lower the amplitude of the ac output voltages the dc voltage across the dc side capacitor is raised or lowered by adjusting the phase angle of the inverter's output voltage so that enough real power flows in or out of the capacitor thus charging or discharging it to the correct value of Vdc and hence the required voltage amplitude.

5) In the case of non–ideal power switching devices the losses are replenished by adjusting the inverter's output voltage to slightly lag the corresponding ac system voltage and therefore a real component of current will flow from the ac system to the inverter.

In this section where the VSI is required to provide reactive power compensation to an unbalanced three–phase load the principles of operation will differ slightly from those outlined in 1) – 5) above. Here the load compensator is required to fulfill the requirements of Chapter 2 where the load must be balanced and its power factor corrected to unity within two to four cycles of the fundamental frequency. Now in addition to providing purely reactive power to the power system the load compensator is also required to supply unbalanced currents. This is necessary in order to generate the appropriate negative–sequence and positive–sequence current components in order to eliminate those caused by the presence of the unsymmetrical load.

The proposed system is based on the idea that if the three VSI output voltages are of unequal amplitudes and different phase shifts with respect to the corresponding system voltages then it is possible to generate appropriate levels of both imaginary positive– and negative–sequence currents for load compensation. The proposed method for controlling these output voltages is to modulate each one by a different modulation index which is based on the comparison of a triangular carrier signal with three sinusoidal reference waves which represent the

VSI's output voltage in each phase. This method of PWM is referred to as Sinusoidal Pulse Width Modulation (SPWM) and will be discussed in Section 5.1.3. Due to the speed with which the modulation index for each phase can be adjusted, this method of load compensation has the potential to fulfil the response speed requirements and therefore perform better than the systems of Chapter 4 and comparable to or better than those of Chapter 2. Comparisons will be made in Chapter 6.

5.1.2 Study of a Steady–State Model of the SPWM VSI type Load Compensator

In the steady–state model shown in Figure 5.1 the power system and load are represented as in Section 3.3.2. However the unbalanced non–unity power factor three–phase load is represented by a delta connected system whose arms consists of a variable resistive impedance and a variable reactive impedance and similar to the simulated systems of Chapter 4 these impedances are adjusted in order to simulate loads with various power factors and degrees of unbalance.

The supply voltages are assumed to be balanced. In this model the VSI is represented by three controlled voltage sources connected to the respective system voltages by a 0.2 pu inductive reactance which represents the leakage reactance of the Y / Δ transformer used to match the VSI to the line. The aim is to examine the effects of adjusting the amplitudes and shifting the phase angles of the VSI's output voltages with respect to the system voltages by unequal amounts, on the elimination of the imaginary positive–sequence current and the negative–sequence current components due to the unbalanced non–unity power factor load.

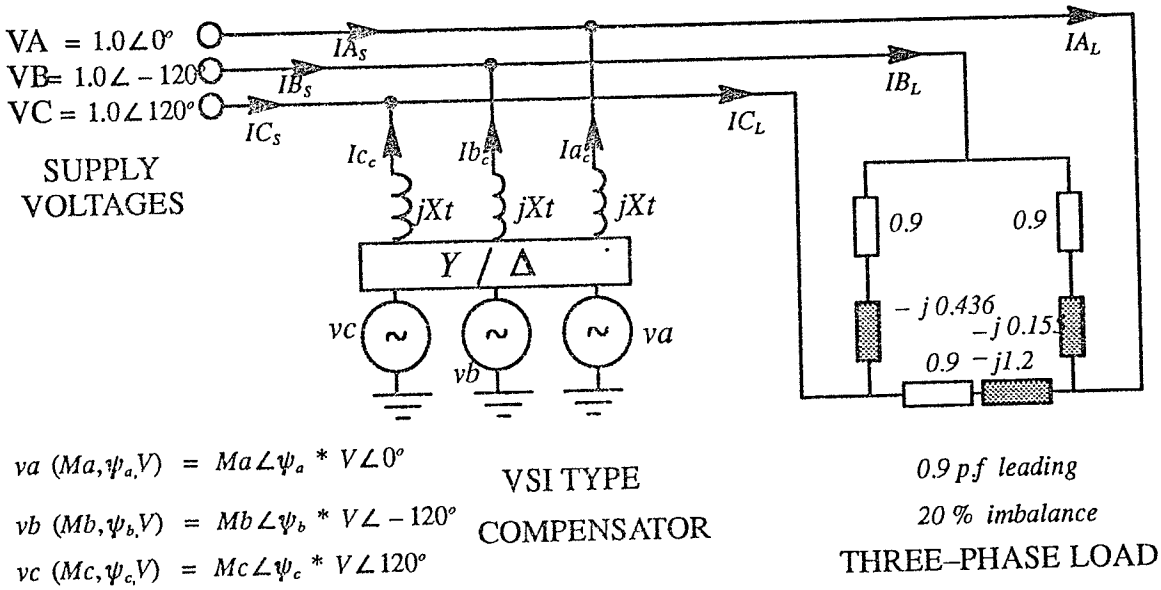


Figure 5.1: Steady–State Model of VSI type load compensator

For this system the resulting positive–sequence and negative–sequence current components of the load currents (IA_L, IB_L & IC_L) due to the load imbalance are:

$$I_{1L} = 4.121 + j\,2.001 \quad \text{and} \quad I_{2L} = 0.243 + j\,0.866$$

For effective load compensation the compensator is required to generate positive– and negative–sequence current components:

$$I_{1C} = +j\,2.001 \quad \text{and} \quad I_{2C} = 0.243 + j\,0.866$$

where C represents the compensator, and the system currents (IA_S, IB_S & IC_S) are represented by equation (5.1).

$$\begin{aligned} IA_S &= IA_L - Ia_c \\ IB_S &= IB_L - Ib_c \\ IC_S &= IC_L - Ic_c \end{aligned} \qquad (5.1)$$

The zero–sequence current component is zero according to the explanations of Chapters 2 and 3. The VSI output currents which are required to flow in the 20% transformer reactances are easily calculated using the well known symmetrical components transformation formula given in equation (5.2).

$$
\begin{aligned}
Ia_C &= I_{0_C} + I_{1_C} + I_{2_C} \\
Ib_C &= I_{0_C} + a^2 I_{1_C} + a I_{2_C} \\
Ic_C &= I_{0_C} + a I_{1_C} + a^2 I_{2_C}
\end{aligned}
\tag{5.2}
$$

Therefore,

$$Ia_C = 2.897\angle 85.19^o \qquad Ib_C = 1.494\angle -55.64^o \qquad Ic_C = 1.980\angle -123.31^o$$

By using equation (5.3), the values of Ma, Mb, Mc, ψ_a, ψ_b, and ψ_c which represent the modulation variables for each phase, can be found.

$$
\begin{aligned}
Ia_C &= \frac{Ma\angle\psi_a^o * V\angle 0^o - VA}{Xt\angle 90^o} \\
Ib_C &= \frac{Mb\angle\psi_b^o * V\angle -120^o - VB}{Xt\angle 90^o} \\
Ic_C &= \frac{Mc\angle\psi_c^o * V\angle 120^o - VC}{Xt\angle 90^o}
\end{aligned}
\tag{5.3}
$$

For this steady–state model the VSI's output voltages Va, Vb, and Vc which in the practical ASVC will assume an equal rms value V that is directly proportional to the voltage across the dc capacitor are assumed equal to 1.2 pu. This value was chosen such that when the load compensator is supplying a maximum leading capacitive power output of 1.0 pu, the current flowing through the transformer reactances will be 1.0 pu (see Section 5.2). By calculation the established values of the modulation variables which are required to generate the correct positive– and negative–sequence current components are as follows:

$$
\begin{aligned}
Ma &= 0.354 \qquad Mb = 0.618 \qquad Mc = 0.559 \\
\psi_a &= 6.59^o \qquad \psi_b = 10.027^o \qquad \psi_c = -15.41^o
\end{aligned}
$$

A summation of the load currents and those of the compensator results in the phasor representation of the system after load compensation as shown in Figure 5.2 (c). Again the subscript S represents the system's line currents. The load

currents and line–to–neutral voltages before compensation along with the required compensator currents are presented in Figure 5.2(a). Figure 5.2(b) shows the vectorial representation of equation (5.1) for phase A of the system. The results show that the three–phase unbalanced non–unity power factor load now appears to the supply to be a balanced unity power factor load which requires only real power, represented by the presence of the real component of the positive–sequence current only.

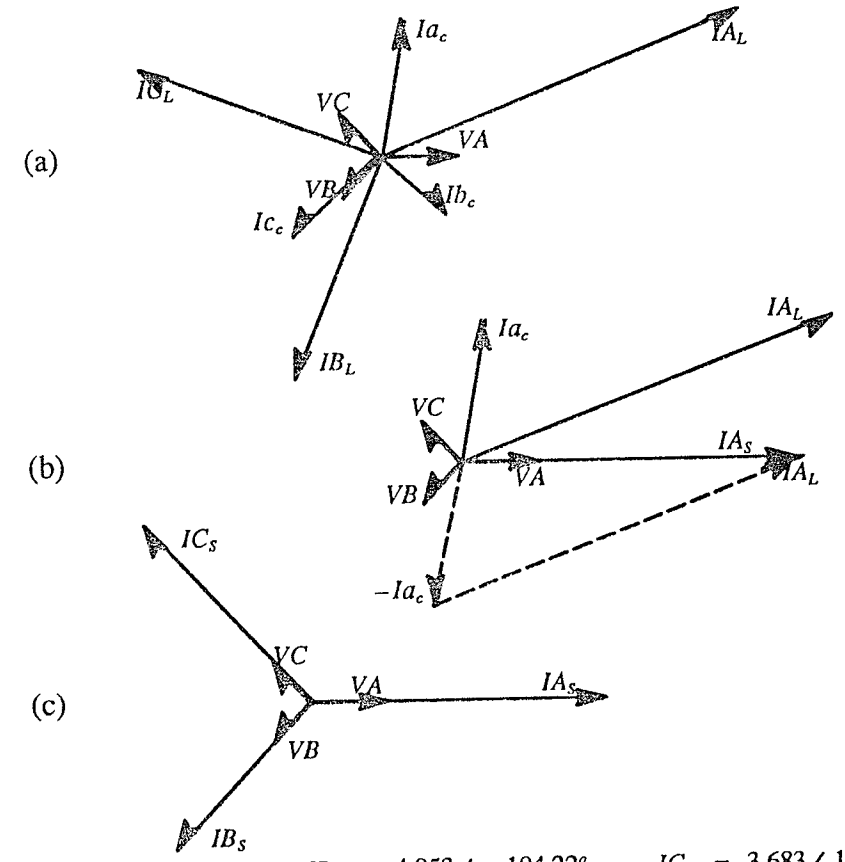
With the basic principles of the PWM–VSI load compensation scheme established, the next step is to determine exactly how the PWM techniques will be applied to the VSI. The aim is to develop a suitable controller.

5.1.3 PWM techniques for Voltage Control in VSIs

In many industrial applications, such as in load compensation, relatively fast and accurate control of the output voltages of three phase inverters is required. In this section a few of the techniques which are based on single–phase inverters will be presented. These techniques can be readily applied to three–phase inverters since the three–phase inverter can be considered as three single–phase inverters with their outputs shifted by 120°. There are quite a few PWM techniques by which the necessary voltage control can be accomplished such as Single–Pulse–Width Modulation where the inverter's gating signals are generated by comparing a rectangular reference signal of amplitude Ar with a triangular carrier wave of amplitude Ac.

The ratio of Ar to Ac is the control variable and is defined as the modulation index. The modulation index,

$$m = \frac{Ar}{Ac} \tag{5.4}$$



$IA_L = 5.23\angle 33.49^\circ$ $IB_L = 4.953\angle -104.22^\circ$ $IC_L = 3.683\angle 148.69^\circ$

$Ia_c = 2.897\angle 85.19^\circ$ $Ib_c = 1.494\angle -55.64^\circ$ $Ic_c = 1.980\angle -123.31^\circ$

$IA_S = 4.121\angle 0^\circ$ $IB_S = 4.121\angle -120^\circ$ $IC_S = 4.121\angle 120^\circ$

$VA = 1.0\angle 0^\circ$ $VB = 1.0\angle -120^\circ$ $VC = 1.0\angle 120^\circ$

Figure 5.2: phasor representation of system a) before load compensation; b) after load compensation.

By varying *Ar* from 0 to *Ac* the modulation index can be controlled from 0 to 1. In a single–pulse–width modulation system, there is only one pulse per half–cycle and the width of this pulse is varied in order to control the inverter's output voltage. Also the frequency of the carrier wave determines the frequency of the output voltage. This type of modulation is however not suitable for the three–phase VSI of this chapter since along with voltage control, the chosen PWM technique is usually used to eliminate the undesirable harmonics which are present in the inverter's output voltage, and the amount of harmonics which are eliminated are usually proportional to the amount of pulses generated per

half–cycle. Since the single–pulse–width modulation technique produces only one pulse per half–cycle and the distortion factor increases significantly at lower output voltages, it is unsuitable for the type of load compensator required here.

Another form of PWM which is used is referred to as Uniform Pulse Width Modulation (UPWM) this due to the fact that the widths of the generated pulses are the same. Here the reference signal which is a square–wave as is the case with the single–pulse width modulation, sets the output frequency Fo. The carrier frequency Fc determines the number of pulses per half–cycle. The number of pulses per half cycle,

$$p = \frac{Fc}{2Fo} \tag{5.5}$$

The variation of the modulation index from $m = 0$ to 1 in this case will vary the pulse width from 0° to $180°/p$ and the output voltage amplitude from zero to its maximum value. In the UPWM system due to the large number of switching, the switching losses would increase. The lower–order harmonics would be lower with larger values of p but the amplitudes of some higher–order harmonics would increase. Since higher–order harmonics produce negligible ripple and can be easily filtered out, this form of PWM is more practical than the single–pulse width modulation.

A third method of PWM is referred to as Sinusoidal Pulse Width Modulation (SPWM) and compares a sinusoidal reference signal of frequency Fr with a triangular carrier wave of frequency Fc. With SPWM the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the center of the same pulse. Therefore the width of all pulses are not the same as with UPWM and both the distortion factor and lower–order harmonics are significantly reduced. Here the inverter's output frequency Fo is determined by Fr and the

peak amplitude of the reference signal *Ar* controls the modulation index *M*, and the rms output voltage *Vrms*. The carrier frequency *Fc* determines the number of pulses per half–cycle. Figure 5.3 shows the gating signals *g1* and *g4* for a single–phase VSI along with the instantaneous output voltage *vo*. This result is based on the constraint that two thyristors of the same branch, say T1 and T4, cannot conduct at the same time. In this case the rms output voltage can be varied from 0 to *Vs* by varying the modulation index from 0 to 1. If δ_m is the width of the *m*th pulse then the rms output voltage is

$$Vrms = Vs \left\{ \sum_{m=1}^{p} \left(\frac{\delta_m}{\pi}\right)^2 \right\}^{\frac{1}{2}} \tag{5.6}$$

The three–phase VSI which will be used in this section as the main component of the ASVG load compensator will be subjected to SPWM in each phase in order to control the output voltage in each phase. Although charging or discharging the dc capacitor to the correct voltage is relatively slow, establishing the correct modulation variables in each phase can be accomplished much faster. The accumulative effect will be that of rapidly adjusting the peak value and phase shift angle of the sinusoidal reference voltage (inverter output voltage) in each phase to the appropriate value.

In Section 5.2 the SPWM–VSI type load compensator will be analysed and designed.

5.2 Load Compensator Design

The SPWM–VSI type load compensator configuration which will be designed in this Section is shown in Figure 5.4 . The compensator is connected to the ac system and load via a 13.2kV / 762V Y/Δ transformer whose leakage reactance is assumed equal to 20%. Similar to the steady–state model of Section 5.1.2 the system's line–to–neutral voltages are assumed balanced. The load is again

simulated as delta–connected resistances and reactances with a maximum leading reactive power requirement of 1.0 MVAr. The modulation variables *Ma*, *Mb* and *Mc* are restricted to the range of 0.1 to 1.0. In a practical situation the load to be compensated must be carefully studied and the maximum leading reactive power requirement determined for the worst case. This is important since the leading reactive power generating capability of the load compensator is determined by the maximum dc voltage to which the available capacitor can be charged when the range restrictions on the modulation variables are taken into account.

If the capacitor is assumed to charge up to its maximum voltage then the response speed of the load compensator would essentially depend on the speed with which the modulation variables *Ma*, *Mb*, *Mc*, ψ_a, ψ_b, and ψ_c can be controlled by PI control.

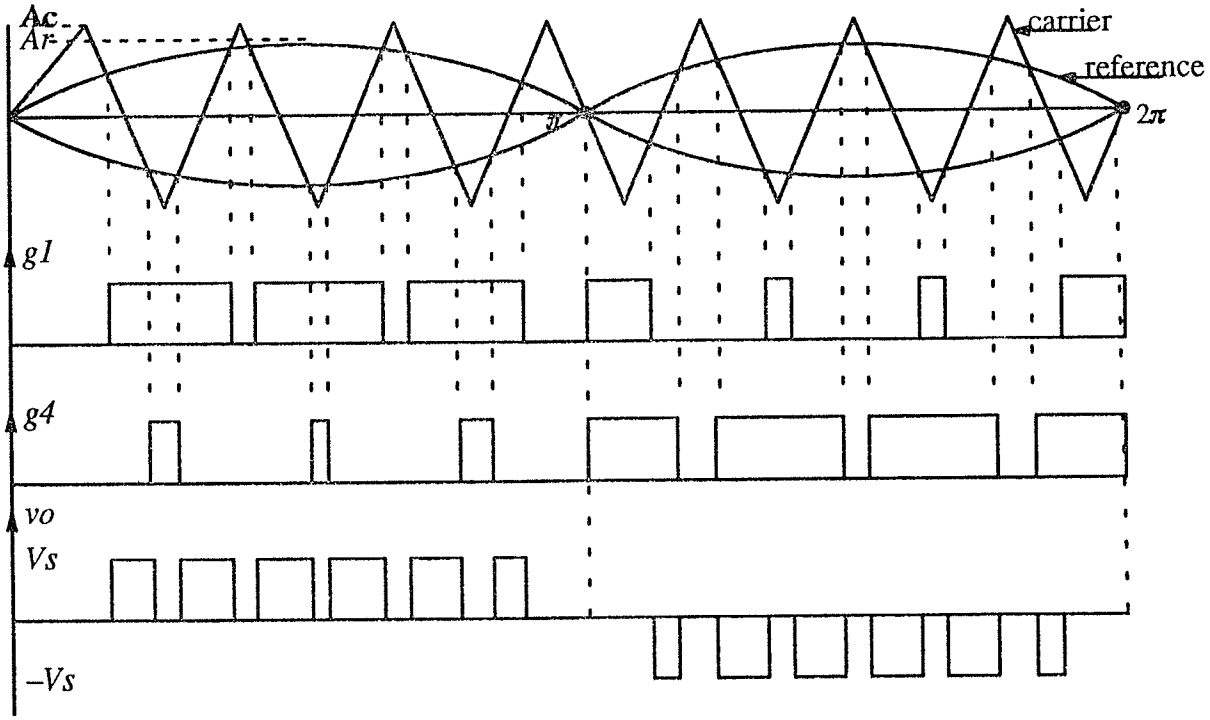


Figure 5.3: SPWM in a single–phase VSI

For this system the base quantities are as follows:

Primary (Y) side of transformer

S_{BASE} = 1.0 MVA V_{BASE} = 13.2 KV I_{BASE} = 43.74 A Z_{BASE} = 174.23 Ω

Secondary (Δ) side of transformer

S_{BASE} = 1.0 MVA V_{BASE} = 0.762 KV I_{BASE} = 757.68 A Z_{BASE} = 0.581 Ω

All system quantities are summarized in Appendix C.

In this section the load compensator will be designed to compensate loads in the range of 0.6 p.f lagging and 5% imbalance to 0.9 p.f leading and 40% imbalance. A high pass filter will be used on the primary side of the transformer in order to eliminate those characteristic harmonics which are not eliminated by the SPWM harmonic control technique. The control block consists of both the SPWM controls and the DC voltage controls along with blocks for measuring and calculating the required control variables. In Section 5.2.1 the dc capacitor is designed while the control block is designed in Section 5.3.

5.2.1 DC Capacitor Design

The main component of the VSI which needs to be designed is the dc capacitor since it is the voltage to which this capacitor is charged which determines the rms value of the compensator's output voltages. During operation of the SPWM–VSI load compensator the voltage across the dc capacitor will be at its maximum value when the capacitor is fully charged and the compensator is producing a maximum of 1.0 MVAr capacitive power with a maximum leading output current I_{Cp} (p denotes primary side of transformer) of 1.0 pu flowing through the 20% transformer reactance. Therefore I_{Cp} = 43.74 A and the rms value of the secondary line current I_{Cs} = 757.68 A. Now the magnitude of the required rms output voltage of the VSI referred to the primary, Vi = 15.84 KV (1.2 pu) (by equation (5.7))

(5.7)

$$I_{C_p} = \frac{Vi - 1.0}{0.2}$$

Therefore the required rms output voltage of the VSI referred to the secondary is 914.30 V.

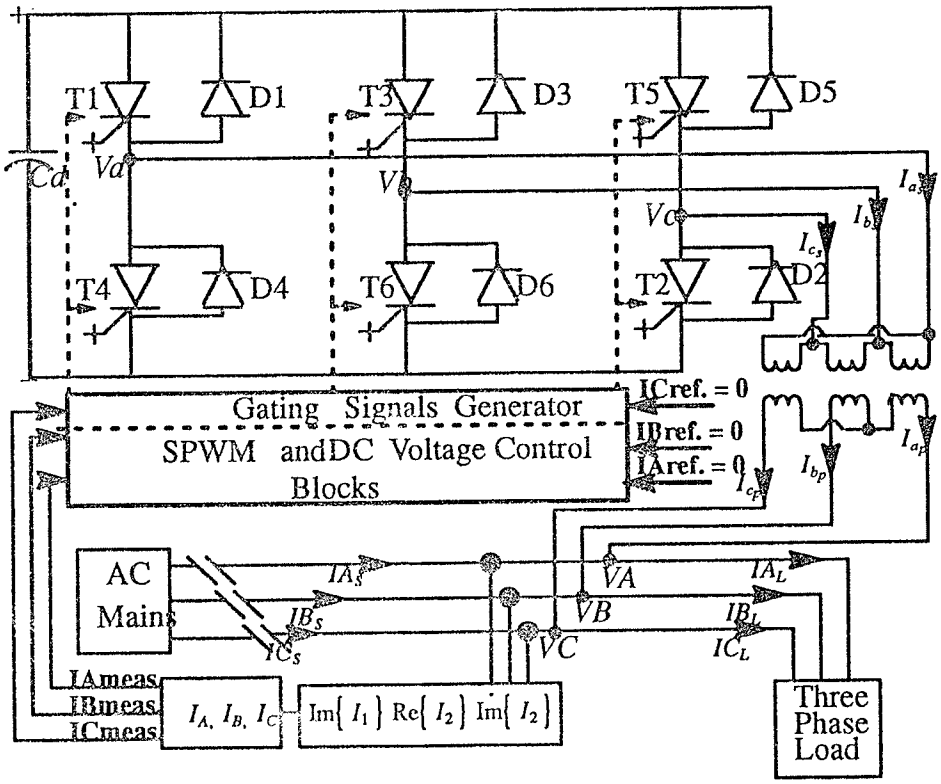


Figure 5.4: Configuration of PWM–VSI type load compensator

The next step is to calculate the required maximum dc capacitor voltage. However in order to accomplish this, consideration must be given to the harmonic content of the VSI's output voltage waveform. With reference to the analysis of the VSI's output voltage waveforms under normal operation (without any harmonic filtering) which was developed in Chapter 3 , the observation is that the output voltage waveform in each phase will contain odd harmonics. Due to reasons which were mentioned in that chapter the triplen harmonics are not present.

As mentioned briefly in Section 5.1.3 some of the harmonics generated can be

eliminated by the use of PWM where the output voltage waveforms are divided into p pulses per half–cycle and the remaining ones are eliminated by high–pass filtering. Indepth analyses on the use of PWM harmonic elimination techniques are available in [18, 19, 21, 22]. It is worth noting here that there is a practical limit to the number of pulses which can be generated per half–cycle and hence the number of voltage harmonics which can be eliminated by this method. The reasons being that:

a) the commutation of a GTO thyristor takes a definite time which establishes a practical limit on the pulse frequency; and

b) each switching of the GTO thyristor is accompanied by some energy loss and a high pulse number will lower the efficiency of the inverter.

Generally, with any PWM switching scheme with large numbers of pulses per half–cycle, the amplitudes of the lower–order harmonics would be lower but those of some higher–order harmonics would increase. However as mentioned earlier, the higher order harmonics are easier to eliminate by tuned filters. In fact Moran, et. al. [13] suggests that with a three–phase VSI the distortion factor and switching losses can be kept within acceptable limits by using an optimized stored PWM voltage waveshaping pattern in which a set of nonlinear transcendental equations, obtained from the Fourier representation of the inverter's output waveforms, are solved by utilizing an iterative technique. In this case if the number of pulses per half–cycle are maintained at $p = 11$ then the rms values of the first ten characteristic harmonics will be significantly reduced. Another advantage associated with increased pulse number operation is the reduction in the size of the dc capacitor. Therefore in designing a suitable load compensator, all the advantages and disadvantages mentioned above must be taken into consideration such that an optimized model which is best suited to the application at hand is developed.

Since the method of output voltage control used here is SPWM then to increase the pulse number of the inverter and hence reduce the harmonics produced would require that the frequency of the triangular carrier signal be appropriately adjusted according to the requirements of Section 5.1.3. For the load compensator being designed here the undesirable characteristic harmonics up to the seventh will be eliminated by utilizing 4 pulses per half–cycle ($p = 4$). This is due to the fact that the sinusoidal modulation eliminates all harmonics less than or equal to $2p - 1$. Higher order harmonics will be eliminated by using a high pass filter which is tuned to the eleventh voltage harmonic. This filter will be connected to the primary (system) side of the Y/Δ transformer. Ideally only an inductive reactance should be connected between the inverter's output voltages and the system's voltages and if filters are connected to the secondary side of the transformer an additional phase–shift will be created. Therefore the reactive power control is achieved more easily if the filters are connected directly to the system which is being compensated. The output voltage is therefore assumed to contain only the fundamental component and hence the dc voltage across the capacitor Vdc = 914.40 V.

In order to choose the proper value for the dc capacitor, Edwards and Nannery [2] suggests that an appropriate value of capacitance will limit the peak–to–peak ripple to 10% of the dc voltage when the system is providing maximum leading output current. The dc capacitor for the SPWM–VSI load compensator will be based on the above criteria. Now according to the above stipulations, when the load compensator is providing maximum leading reactive power, the peak–to–peak value of the ripple voltage will be 91.44 V (by equation (5.8)).

$$Vpp = 0.1\ Vdc \tag{5.8}$$

The equivalent rms value of the peak–to–peak ripple voltage is given by

$$Vr = \frac{Vpp}{2\sqrt{2}} \tag{5.9}$$

from which Vr = 32.33 V (0.00245 pu). From this result the required reactance value of the capacitor Xc can be calculated according to equation (5.10) where I(pu) = 1.0 as stated earlier in this section.

$$Xc\ (pu) = \frac{Vr\ (pu)}{I\ (pu)} \tag{5.10}$$

Now $Xc\ (pu)$ = 0.00245 on a base of 174.27 Ω. Therefore on a base of 0.5806 Ω, $Xc = 0.427\,\Omega$ (0.7352 pu). The value of the required dc capacitor is 6212.14 uF according to equation (5.11).

$$C_{DC} = \left\{\frac{1}{w\ Xc}\right\}$$
$$where\ w = 120\ \pi \tag{5.11}$$

Also for a FC/TCR type compensator fulfilling similar reactive power compensation requirements the rating of the required capacitor would be approximately 32 times the above value.

5.2.2 The Response Speed

In Section 3.3.2 the proposed method for controlling the charging and discharging of the dc capacitor, thereby controlling the dc voltage across it and hence the amplitude of the VSI's output voltage waveforms was to slightly adjust the phase shift between the system and inverter voltages such that for a relatively short period of time real power flows from the system to the inverter and vice

versa. This method of output voltage control will be used in order to maintain the the charge on the capacitor at its peak voltage of 1.2 pu. The SPWM will be continually applied to each phase of the VSI to further adjust the voltage amplitudes and phase shift angles by different amounts in order to produce the necessary unbalanced currents for load compensation. A practical illustration of this method of capacitor voltage control will now be presented.

The general expression for the apparent power flow between the ac system and the VSI can be expressed in terms of fundamental components by equation (5.12)

$$S = \left\{ \frac{VA\ Va\ \sin(\phi)}{Xt} \right\} - j \left\{ \frac{VA\ Va\ \cos(\phi)}{Xt} - \frac{Va^2}{Xt} \right\}$$

$$\phi = phaseshift \qquad (5.12)$$

From this familiar form of expressing S it is clear that the real part represents the real power transfer (P) and the imaginary part the reactive power transfer (Q). Also equation (5.12) further emphasizes the fact that if the two voltages are in phase ($\phi = 0^{o}$) only reactive power is transferred between the VSI and system and that real power flow is bilateral going from VA to V*a* for lagging ϕ and vice versa for leading ϕ.

An ideal capacitor does not dissipate any of the energy supplied to it, but stores that energy in the form of an electric field. In fact a plot of the voltage across, current through and power to the capacitor during the charging phase is shown in Figure (5.5) and the power curve is obtained by finding the product of the voltage and currents at selected instants of time and connecting the points obtained. The energy stored is represented by the shaded area under the power curve.

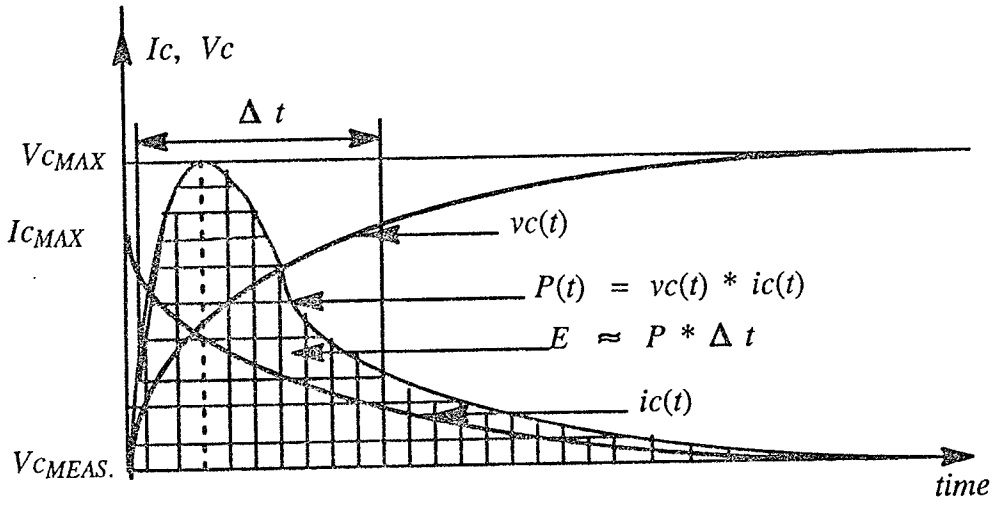


Figure 5.5: Charging characteristic of dc capacitor

With the SPWM–VSI type load compensator, with a practical (non–ideal) capacitor the capacitor voltage must be maintained at 1.2 pu ($Vc_{MEAS} = Vc_{MAX}$). Now suppose for some reason the measured voltage (Vc_{MEAS}) drops to the value shown in Figure 5.5 then for a short period of time the controls must charge the capacitor back to its original value of Vc_{MAX}. With refertence to Figure 5.5 and using calculus methods, the shaded area under the curve can be determined. This area represents the amount of energy required to charge the capacitor up to Vc_{MAX} and can be expressed as

$$E = \frac{C}{2}\left\{Vc_{MAX}^2 - Vc_{MEAS}^2\right\} \tag{5.13}$$

referring again to Figure 5.5 the observation is that most of the energy is concentrated in the area Δt and therefore the area of the rectangle $P * \Delta t$ usually serve as a good approximation of the total energy change. Therefore

$$E \approx P * \Delta t \tag{5.14}$$

In the simulations the value of Δt will be stipulated for the worst case difference between the peak and measured capacitor voltages. Therefore the required real

power transfer P can be found. A substitution into equation (5.12) can produce the correct phase–shift angle ϕ .

Initially, when the load is balanced and has a power factor of unity, the modulation variables will assume values such that the system line currents are equal and in phase with the corresponding system line–to–neutral voltages, thereby maintaining the compensator output currents at zero. Should there be a change in the state of the load then the modulation variables will be appropriately adjusted by PI control until the correct compensator output currents are flowing through the transformer reactances thereby forcing the components of system currents, due to the undesirable symmetrical components, to zero. Hence the system is returned to the pre–disturbance state and the load is compensated.

In view of the above explanations, one can conclude that the overall response speed of the SPWM–VSI type load compensator will be governed predominantly by the speed with which the correct modulation variables can be established. As mentioned earlier the modulation variables can be adjusted fairly rapidly and with a very high degree of accuracy. Therefore the response speed and overall performance of this compensator should be much better than the dual–bridge compensator of the previous chapter. This compensator is expected to compensate the load within 2–3 cycles of the system's fundamental frequency.

The GTO switches in the SPWM–VSI load compensator arrangement must be capable of blocking a forward voltage equal to the dc capacitor voltage. Therefore the GTO switches which are chosen must block a maximum forward voltage of 914.40 V. As was explained in Section (3.4) only unidirectional blocking capability is required.

5.3 Operation and Control

The controls for the PWM–VSI load compensator is of the feedback type, and

is shown in Figure 5.6. This block is made up of three segments: the measurement and calculations segment; the dc voltage control segment and the SPWM control segment. The purpose of the controls is to measure the system's line currents I_{A_S}, I_{B_S} and I_{C_S} extract from these the undesirable symmetrical components $\mathrm{Im}\{I_1\}$, $\mathrm{Re}\{I_2\}$ and $\mathrm{Im}\{I_2\}$ due to the unsymmetrical load, transform these into currents which are referred to in Figure 5.6 as $\mathrm{IA_{meas.}}$, $\mathrm{IB_{meas.}}$ and $\mathrm{IC_{meas.}}$ The real and imaginary components of these currents are forced to zero by the SPWM control block. In the three sections which follow, the operation of these control blocks will be examined in detail. However prior to this, a brief analysis on how the modulation variables can be adjusted by PI control, as shown in Figure 5.6, in order to control separately the real and imaginary components of the measured currents, will be presented.

The method of controlling the modulation variables $Ma, Mb, Mc, \psi_a, \psi_b,$ and ψ_c in this case is different from that which was presented in Section 5.1.2. In this case both the real and imaginary components of the currents which are due to the undesirable symmetrical current components (termed measured currents in Figure 5.6) are brought to zero, thereby ensuring that in the simulations which follow, the compensator will produce accurate output currents.

Consider the modulation variable $M\angle\psi$ (where the absence of a subscript suggests consideration of the general case) which was presented in Section 5.1.2. This can be expressed in another form as shown in equation (5.15)

$$M\angle\psi = M\cos(\psi) + jM\sin(\psi) \tag{5.15}$$

where the real part of the modulation variable (Re {M}) is expressed as $M\cos(\psi)$ and the imaginary part (Im {M}) as $M\sin(\psi)$. If similar arguments are applied to the expressions for the compensator output currents in Section 5.1.2, equation

(5.2), then the following applies for each phase:

phase *a*

$$Ia_c = \left\{ \frac{\left(Ma\cos(\beta_a) + j\,Ma\sin(\beta_a)\right) * \left(V\cos(0) + j\,V\sin(0)\right) - \left(1.0\left(\cos(0) + j\sin(0)\right)\right.}{j\,Xt} \right\}$$

$$where\ VA = 1.0\angle 0^\circ \text{ and } \beta_a = \psi_a + 0^\circ$$

(5.16)

Hence the real and imaginary components of the output compensator current I_{ac} can be represented as follows:

$$\mathrm{Re}[Ia_c] = \left\{ \frac{V\,Ma\sin(\beta_a)}{Xt} \right\} = F\,(Ma\sin(\beta_a))$$

$$\mathrm{Im}[Ia_c] = \left\{ \frac{1.0 - V\,Ma\cos(\beta_a)}{Xt} \right\} = F\,(Ma\cos(\beta_a))$$

(5.17)

If similar arguments are applied to phases b and c, and if by definition:

$$\beta_b = \psi_b - 120^\circ,\ \beta_c = \psi_c + 120^\circ,\ VB = 1.0\angle -120^\circ \text{ and } VC = 1.0\angle 120^\circ$$

then for:

phase b

$$\mathrm{Re}[Ib_c] = \left\{ \frac{V\,Mb\sin(\beta_b) - (1.0\sin(-120^\circ))}{Xt} \right\} = F\,(Mb\sin(\beta_b))$$

$$\mathrm{Im}[Ib_c] = \left\{ \frac{1.0\cos(-120^\circ) - V\,Mb\cos(\beta_b)}{Xt} \right\} = F\,(Mb\cos(\beta_b))$$

(5.18)

phase c

$$\mathrm{Re}\{Ic_c\} = \left\{ \frac{V\,Mc \sin(\beta_c) - (1.0 \sin(120^\circ))}{Xt} \right\} = F\,(Mc \sin(\beta_c))$$

$$\mathrm{Im}\{Ic_c\} = \left\{ \frac{1.0 \cos(120^\circ) - V\,Mc \cos(\beta_c)}{Xt} \right\} = F\,(Mc \cos(\beta_c))$$

(5.19)

Therefore according to the above analysis, in the simulations which follow the real components of the compensator currents, Re{I} are controlled by controlling the imaginary part of the modulation variable, Im{M} whilst the imaginary components of the compensator currents, Im{I} can be controlled by controlling the real component of the modulation variable Re {M}. From the results which are obtained the required values of Ma, Mb, Mc, ψ_a, ψ_b, and ψ_c can be calculated quite easily and to a very high degree of accuracy.

5.3.1 The Measurement and Calculations Block

The measurement and calculations segment of the load compensator's control system is shown in Figure 5.7. It is based on the principle whereby a three–phase unsymmetrical rms phasor current system ($I_A\angle\phi_A$, $I_B\angle\phi_B$, $I_C\angle\phi_C$) can be transformed into the symmetrical components I_0, I_1 and I_2 .

In the digital simulations the measurement is performed by calculations and the above rms phasor representation of the currents may be transformed directly into the sequence components via the well known transformation matrix.

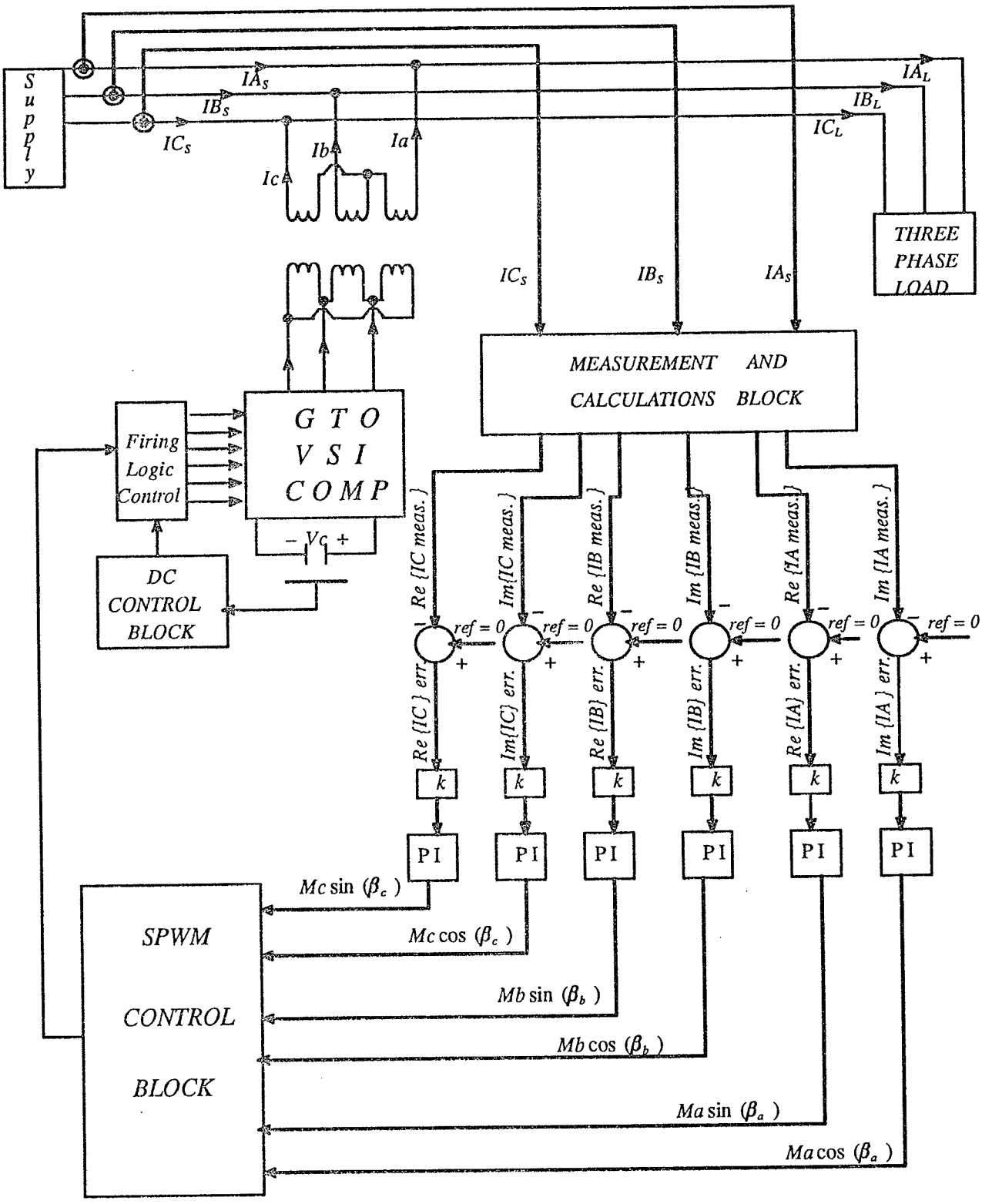


Figure 5.6: Controls for the SPWM–VSI type load compensator

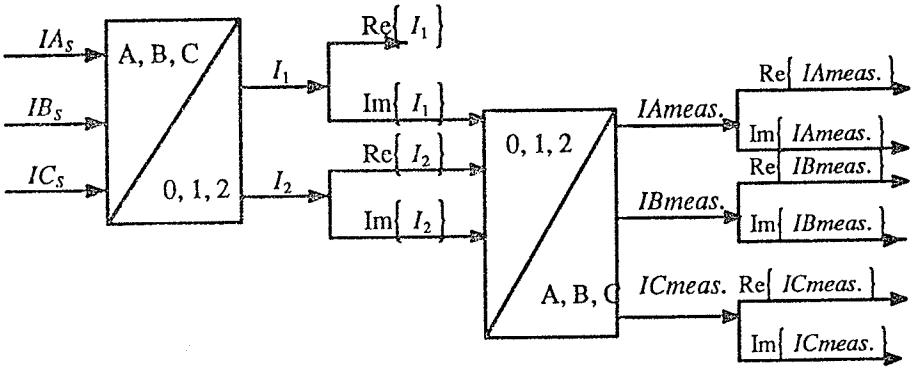


Figure 5.7: Measurement and Calculations Block

Due to the non–unity power factor and unbalanced state of the load which is being compensated, it is assumed in this section that the currents in the three phases are sinusoidal but do not constitute a symmetrical three–phase system. Therefore

$$
\begin{aligned}
i_A\ (t) &= \hat{i}_A \cos\left(wt + \phi_A\right) \\
i_B\ (t) &= \hat{i}_B \cos\left(wt + \phi_B - \frac{2\pi}{3}\right) \\
i_C\ (t) &= \hat{i}_C \cos\left(wt + \phi_C + \frac{2\pi}{3}\right)
\end{aligned}
\tag{5.20}
$$

where $\hat{i}_{A,B,C}$ represent the peak value of the sinusoidal currents. In terms of phasor notation representation the above currents can be represented as shown in equation (5.21)

$$
I_A = \frac{\hat{i}_A}{\sqrt{2}} e^{j\phi_A}, \quad I_B = \frac{\hat{i}_B}{\sqrt{2}} e^{j\left\{\phi_B - 2\frac{\pi}{3}\right\}}, \quad I_C = \frac{\hat{i}_C}{\sqrt{2}} e^{j\left\{\phi_C + 2\frac{\pi}{3}\right\}}
\tag{5.21}
$$

Since the interest here is in controlling the imaginary positive–sequence and the real and imaginary negative–sequence current components only, the real part of

the positive–sequence current is not a control variable in this control system. Therefore all sequence current components, excluding the real positive–sequence current component are used as inputs to the 1,2–to–A,B,C transformation block. The outputs from this block will contain all the information required by the controls to compensate the unsymmetrical load. These currents constitute the measured inputs to separate PI regulators. The reference inputs to these PI regulators are set to zero. The function of the controls is to bring the error signal, which is essentially the measured inputs, to zero.

5.3.2 The DC Voltage Controls

During the load compensation start–up process in order to prevent large transients when the line voltage is first applied to the VSI a dc precharging circuit (not shown) is normally used [2]. This circuit will charge the capacitor to its peak dc voltage. In some of the cases where the VSI was used for system compensation [10,20] where the dc capacitor was charged to a nominal voltage which is equivalent to the peak of the transformer secondary voltage, the dc precharging mechanism usually consisted of breakers. These are initially closed, and with the gate drives to the GTOs blocked, the capacitor is charged through the diodes of the inverter. After the capacitor is charged to its nominal voltage the gate drives are deblocked in order to operate the inverter.

The dc controls are expanded in Figure 5.8. Here the Phase Locked Loop (PLL) which consists of a phase detector with an error integrator and a Voltage Controlled Oscillator (VCO) will serve to establish synchronism between the VSI and the ac system voltages. The function of these controls which will be slower than the SPWM controls, is to maintain the dc voltage across the capacitor at its peak value of 1.2 pu.

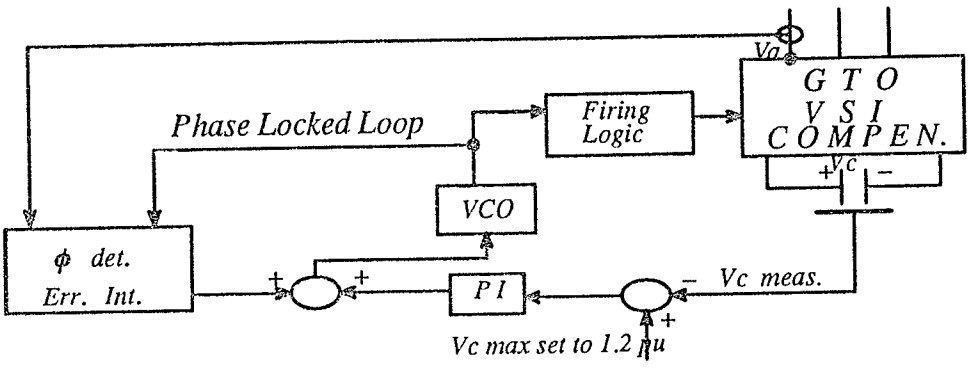


Figure 5.8: Expanded dc voltage controls

The input signal to the PI regulator is the resulting error signal derived from the difference between the dc capacitor peak or maximum voltage and the measured capacitor voltage, this error indicates the dc voltage demand. The voltage demand signal is then summed with the output of the phase detector/error integrator which serves as the input to the VCO. The reason for this is that if the measured capacitor voltage is not equal to Vc max. then the voltage demand signal will force the PLL to produce the correct phase angle difference ϕ which is required to charge or discharge the capacitor to Vc max., thereby changing the magnitude of the measured signal to Vc max. (1.2 pu).

5.3.3 The SPWM Controls

The SPWM control block of Figure 5.6 is expanded in Figure 5.9. First the inverter output voltages *va*, *vb* and *vc* are transformed into their two–phase representation v_α and v_β according to equation (5.22).

$$v_\alpha = \frac{2}{3}v_a - \frac{1}{3}v_b - \frac{1}{3}v_c$$
$$v_\beta = 0v_a + \frac{1}{\sqrt{3}}v_b - \frac{1}{\sqrt{3}}v_c \qquad (5.22)$$

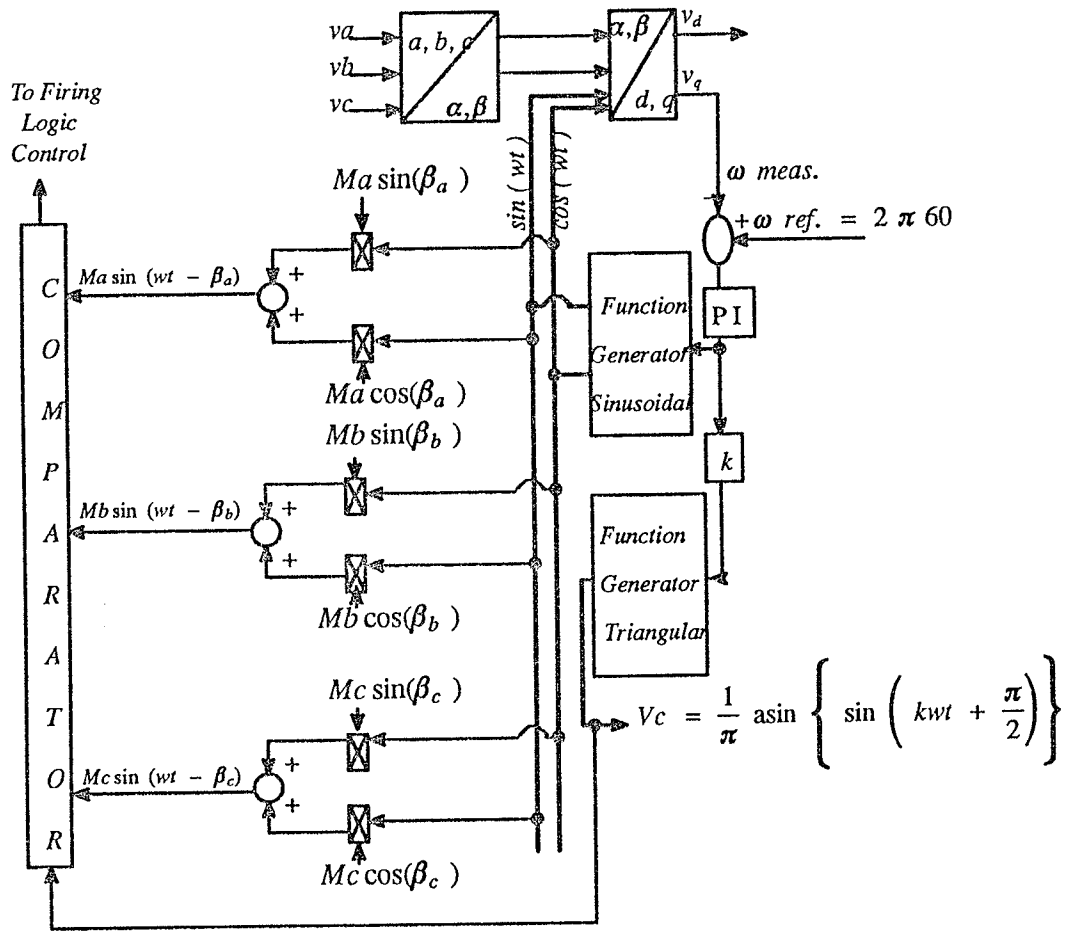


Figure 5.9: Expanded SPWM controls

These are then transformed into the two axis– or d, q– representation according to the following matrix transformation which was introduced in Section 4.2.3 and is used extensively in electric machines analysis in order to transform three–phase currents of frequency w in fixed axis windings to equivalent direct currents in commutator windings.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos\ (\ wt\ ) & \sin\ (\ wt\ ) \\ \sin\ (\ wt\ ) & -\cos\ (\ wt\ ) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{5.23}$$

The difference between the frequency w of the quadrature component and the

reference frequency, which is 60 Hz in this case, serve as the input to the PI regulator thereby controlling the frequencies of both the triangular carrier wave and the three sinusoidal reference signals for the SPWM process. Should there be a change in the reference frequency, the PI regulator would shift the frequency of the SPWM controls such that the controller will continue to generate appropriate carrier and reference waveforms at the new frequency. Therefore this system can operate effectively in situations where frequency excursions are expected. The above controller is based on a measurement technique which was proposed by Gueth, et al. [3] for measuring the sequence components for the compensation of a railway electrification project in which the voltages were often unbalanced and the frequency experienced frequent and large excursions.

Results from the digital simulations of the three–phase SPWM–VSI load compensator are presented in Section 5.4.

5.4 Results from the Digital Simulations

In this section the results from simulations of the SPWM–VSI load compensator using EMTDC will be presented and analysed. The results which are shown in Figures 5.10 and 5.11 represent two cases respectively:

CASE I

Here the load is switched from a unity power factor, balanced load to a 35% unbalanced 0.9 pf leading load at time=0.05 seconds.

CASE II

At time=0.05 seconds the load is switched from a unity power factor, balanced state to a 20% unbalanced 0.6 p.f lagging state.

In all simulations the capacitor is assumed charged to its peak voltage of 1.2 pu and to be maintained at this voltage by way of the dc controls.

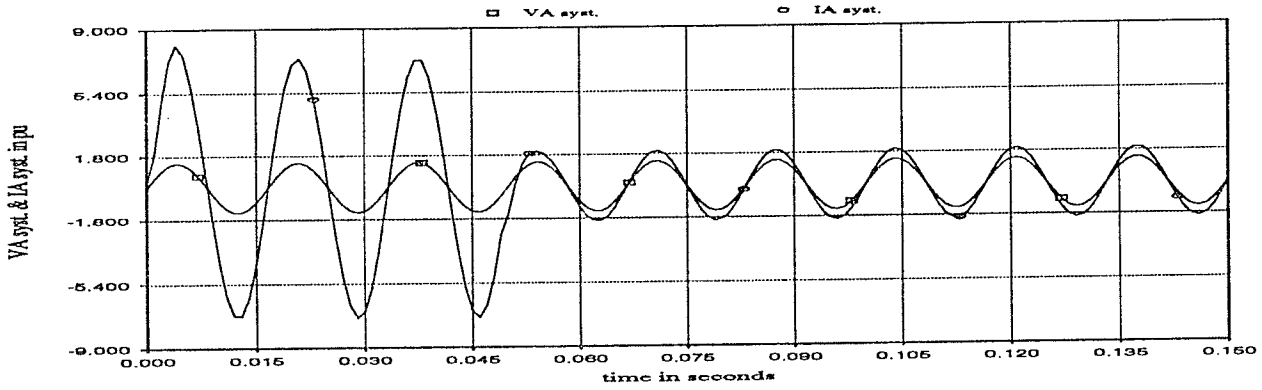
The modulation variables in each case will assume values such that the output currents from the load compensator are zero whenever the three–phase load is balanced and has a power factor of unity, that is when the system's line currents are in phase with their respective line–to neutral voltages and all components of the measured currents are equal to zero. Should the controls detect a change in the state of the load, manifested by a change in the above control parameters, the PI regulators would appropriately adjust the modulation variables until the system returns to its pre–disturbance state.

In CASE I the constant gain k is set at unity whilst it is set at 1.3 for CASE II.

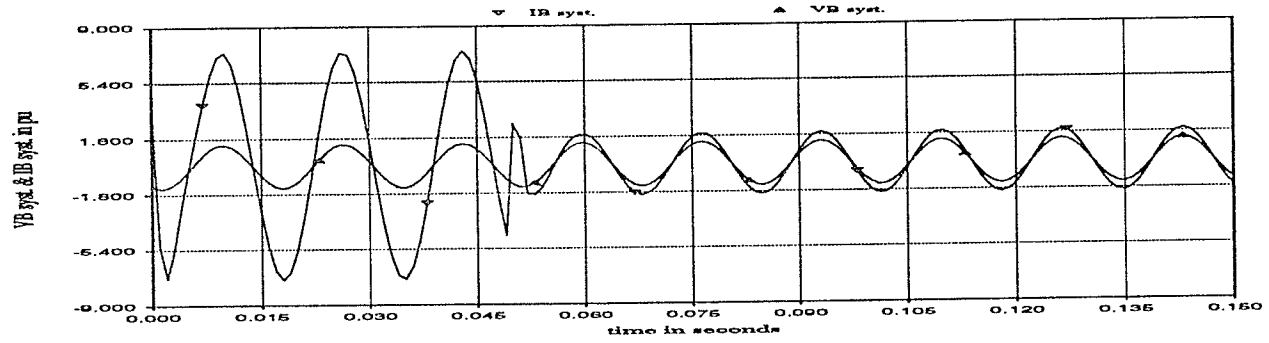
All undesirable harmonics are assumed to be effectively filtered and as such the results will reflect only fundamental components.

CASE I : 35% load imbalance & 0.9 p.f leading

(a)



(b)



(c)

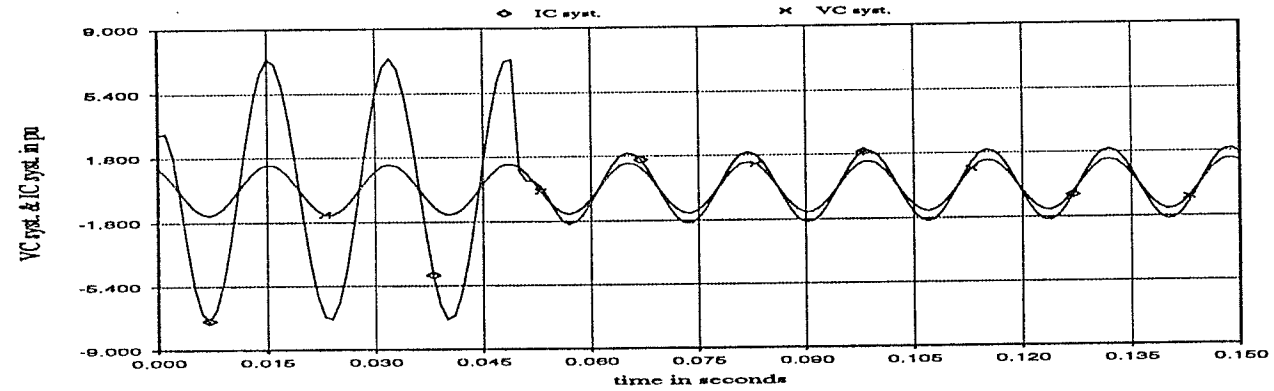
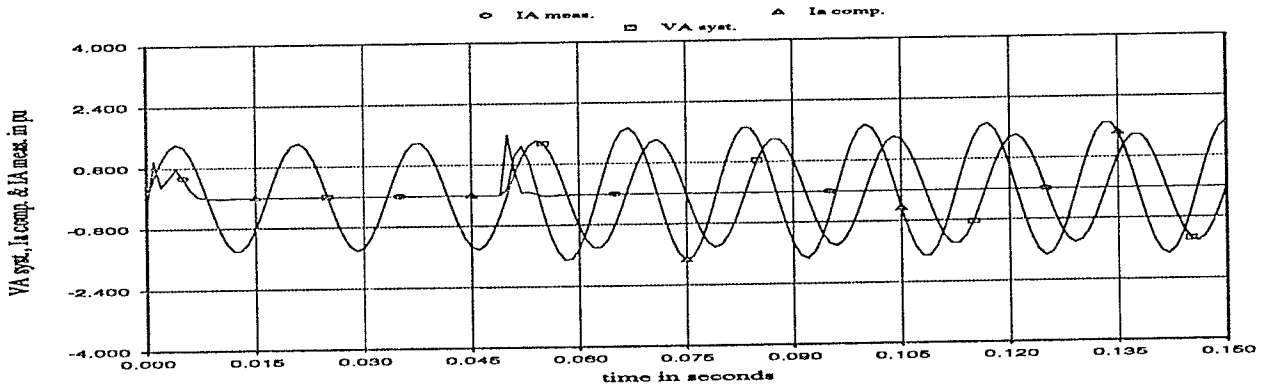
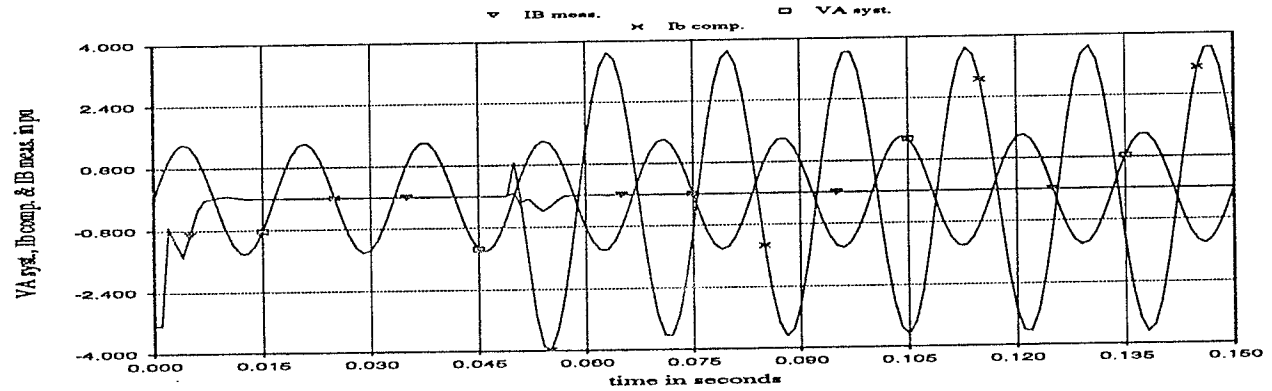


Figure 5.9: (a), (b) and (c) for CASE I

(d)



(e)



(f)

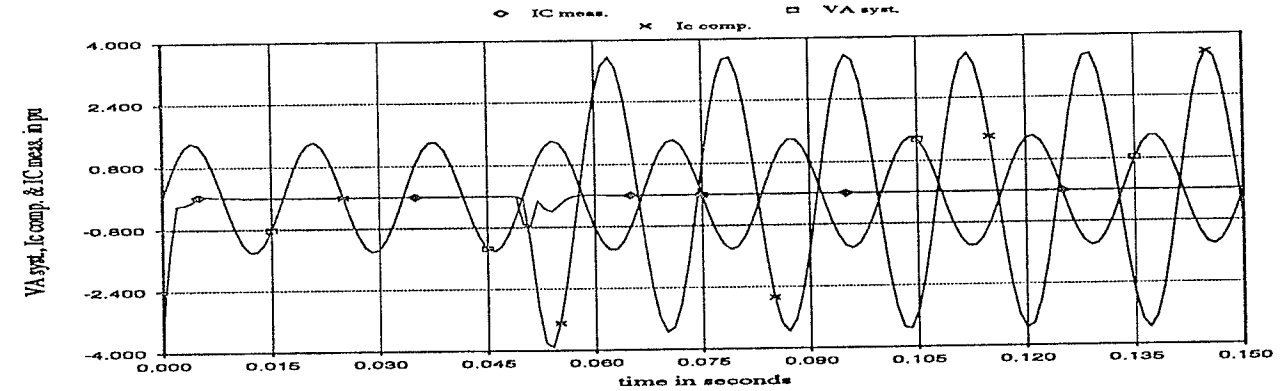
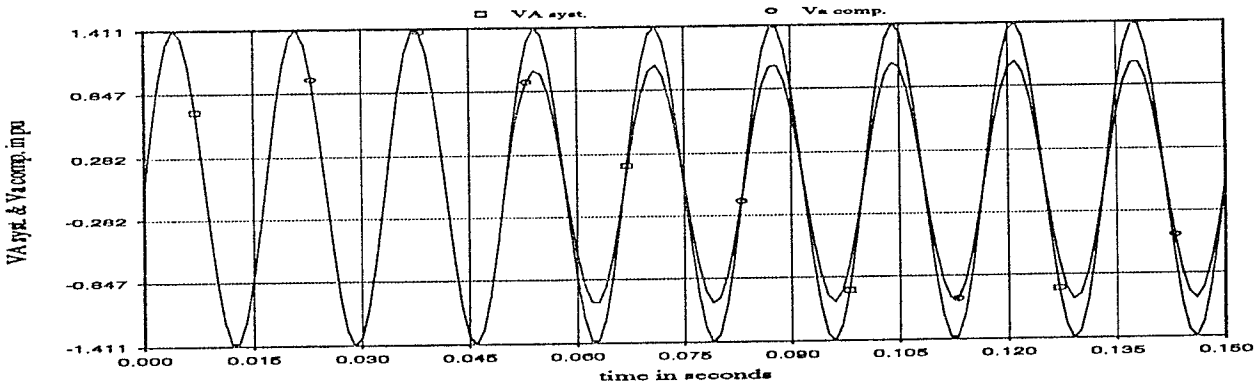
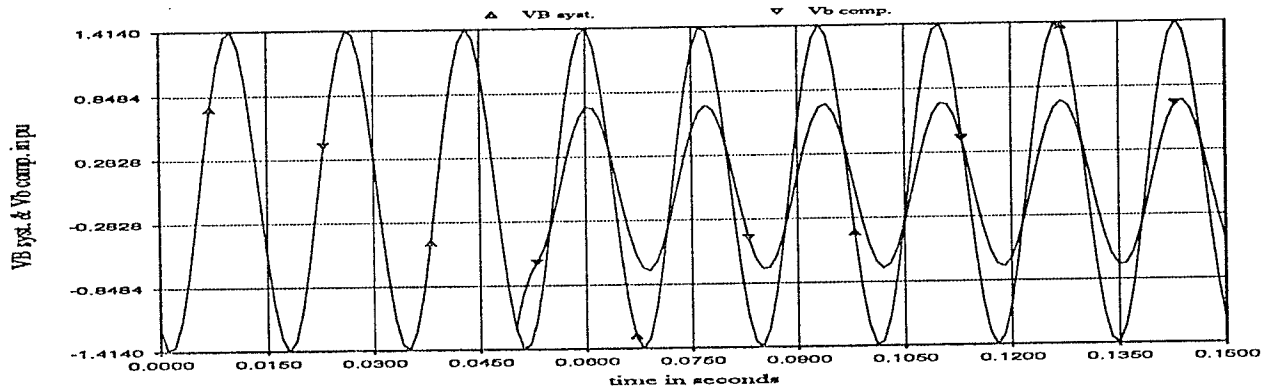


Figure 5.10: (d), (e) and (f) for CASE I

(g)



(h)



(i)

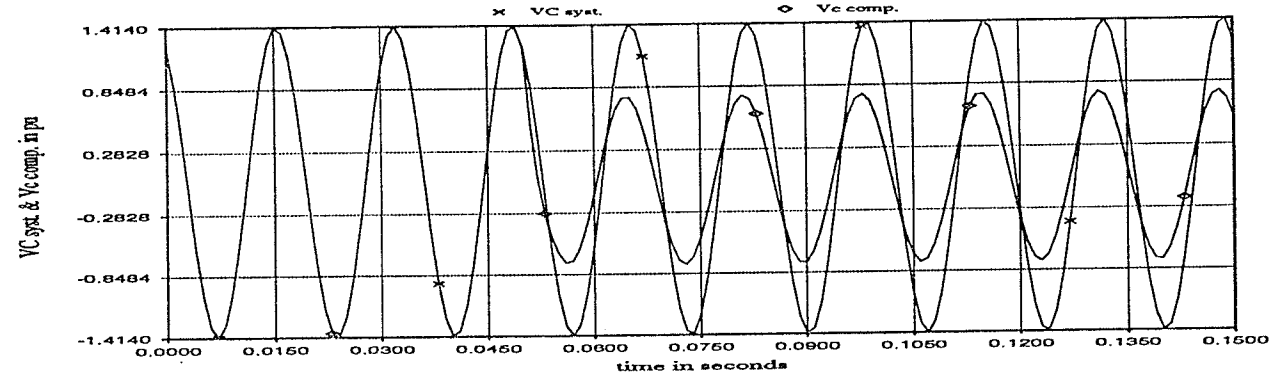
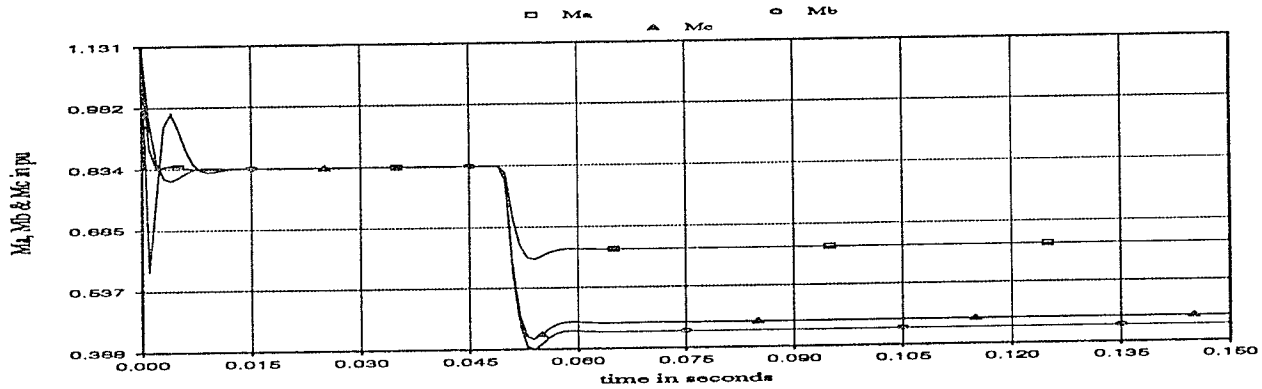
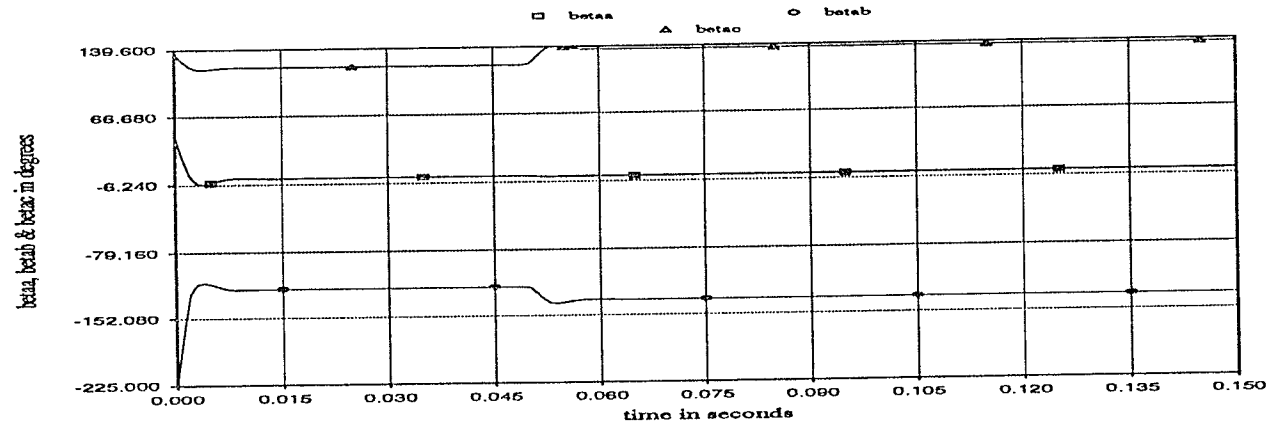


Figure 5.10: (g), (h) and (i) for CASE I

(j)



(k)



(l)

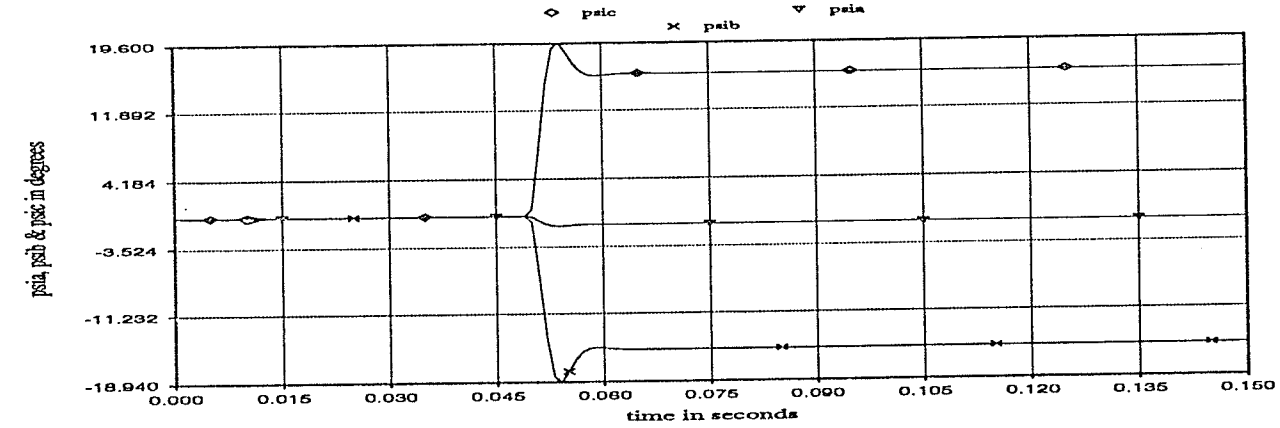


Figure 5.10: (j), (k) and (l) for CASE I

(m)

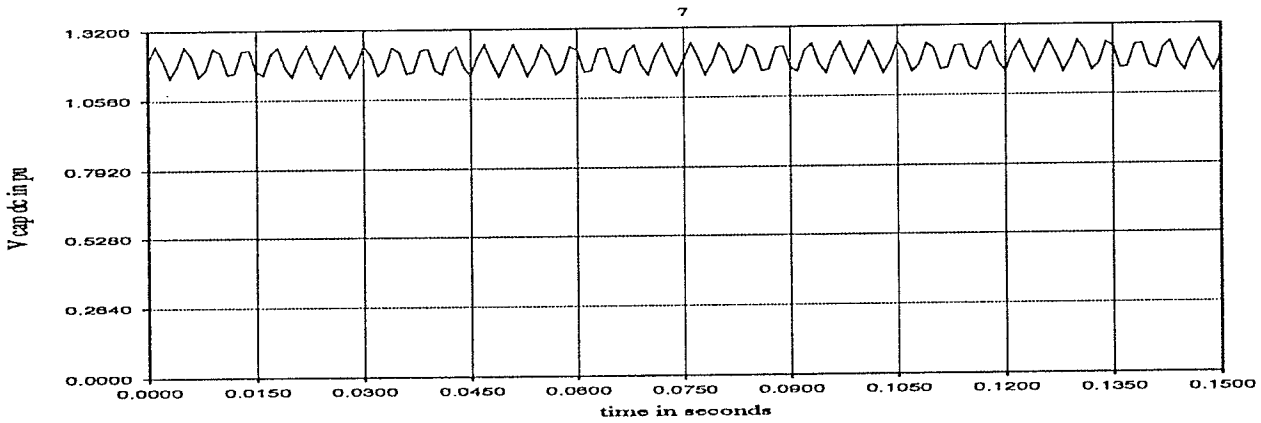


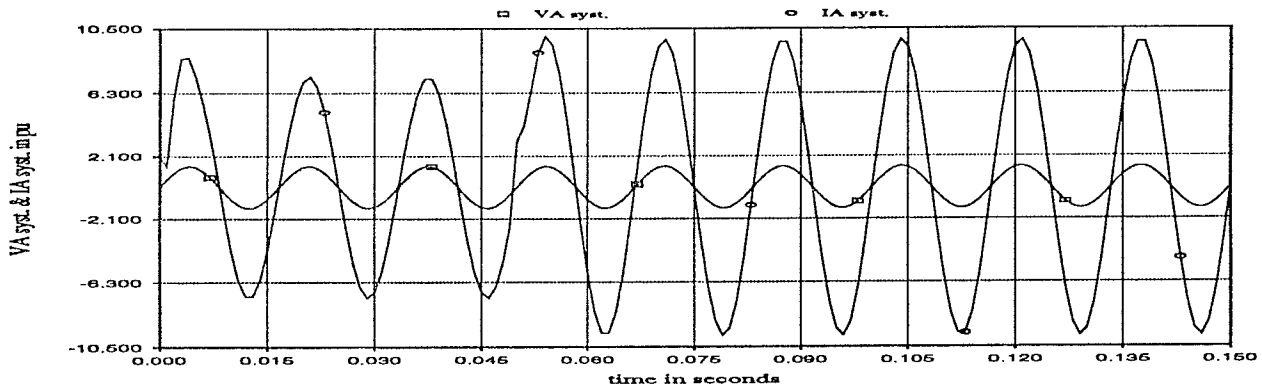
Figure 5.10: (m) dc capacitor voltage

Results from Figure 5.10 (a), (b) and (c) show that prior to the disturbance the system's line currents are of equal magnitude and are in phase with the corresponding line–to–neutral voltages indicating that the load has a power factor of unity and is balanced. When the disturbance is initiated the currents are no longer of equal magnitudes and are now out of phase with the corresponding voltages. In this case where the switched load is 0.9 p.f leading and 35% imbalanced the compensator is capable of compensating it within 1 cycle. This would probably increase to about 2–3 cycles when practical time delays in all control blocks and in the GTO–VSI are taken into consideration. Figure 5.10 (d), (e) and (f) show that the output compensator currents are of unequal amplitudes and experience difference phase relationships with the corresponding system voltages. These results also show how the measured system currents, IA meas., IB meas. and IC meas., which are due to the undesirable sequence current components are rapidly reduced to zero. In 5.10 (g), (h) and (i) the required inverter output voltages which result in load compensation are of unequal

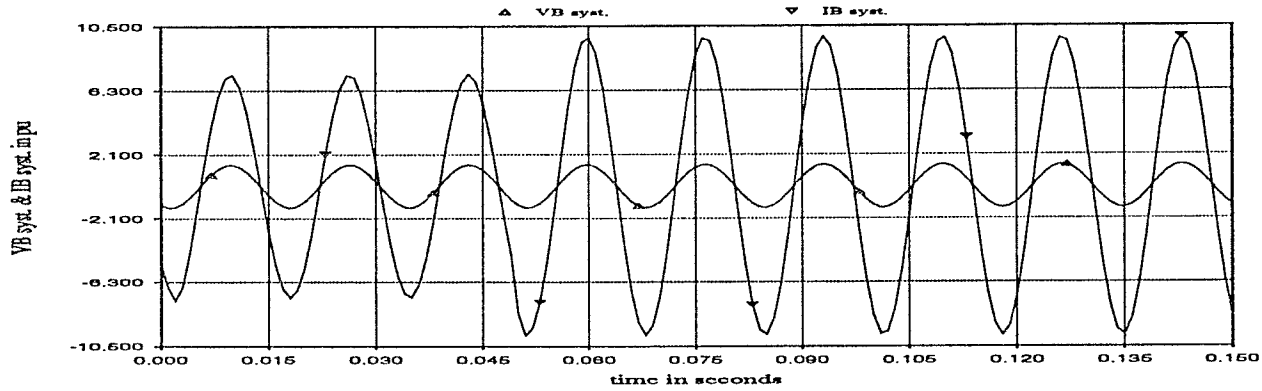
amplitudes and are phase shifted by different amounts with reference to the corresponding system voltages. Figure 5.10 (j), (k) and (l) show the modulation variables Ma, Mb, Mc, β_a, β_b, β_c, ψ_a, ψ_b, and ψ_c. The dc capacitor voltage is shown in Figure 5.10 (m). As is explained by the considerations of Section 5.2.1 this voltage is dc with a ripple component.

CASE II : 20% load imbalance & 0.6 p.f lagging

(a)



(b)



(c)

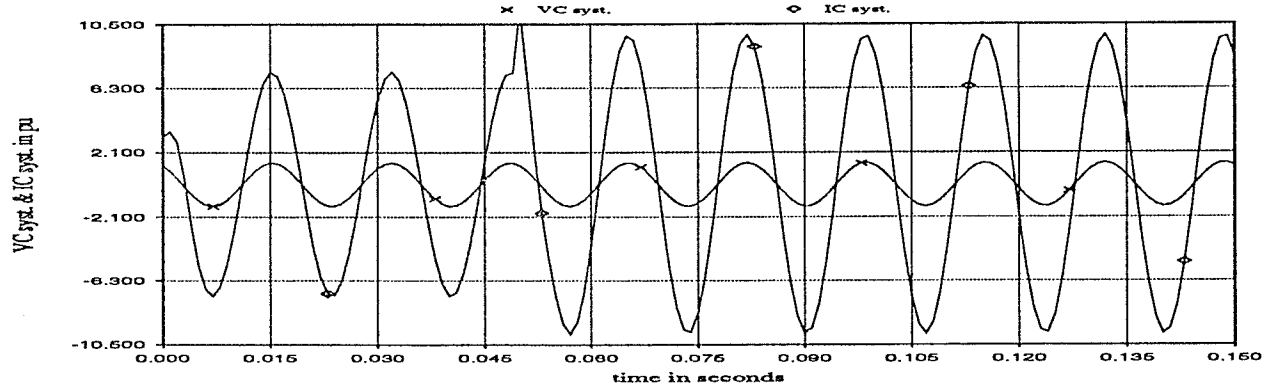
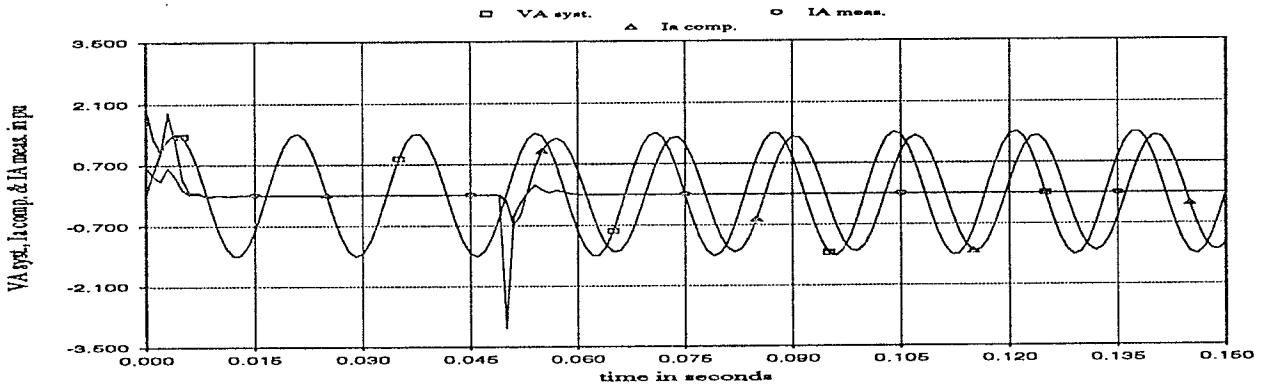
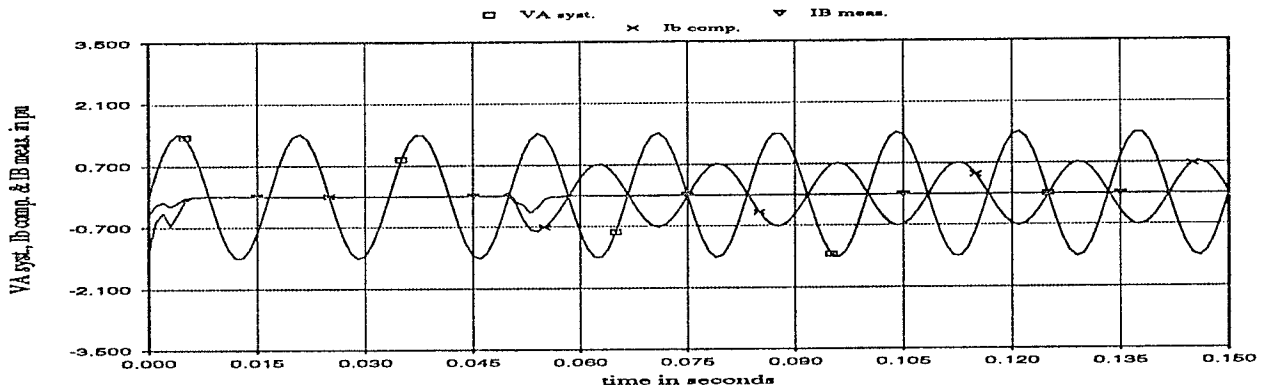


Figure 5.11: (a), (b) and (c) for CASE II

(d)



(e)



(f)

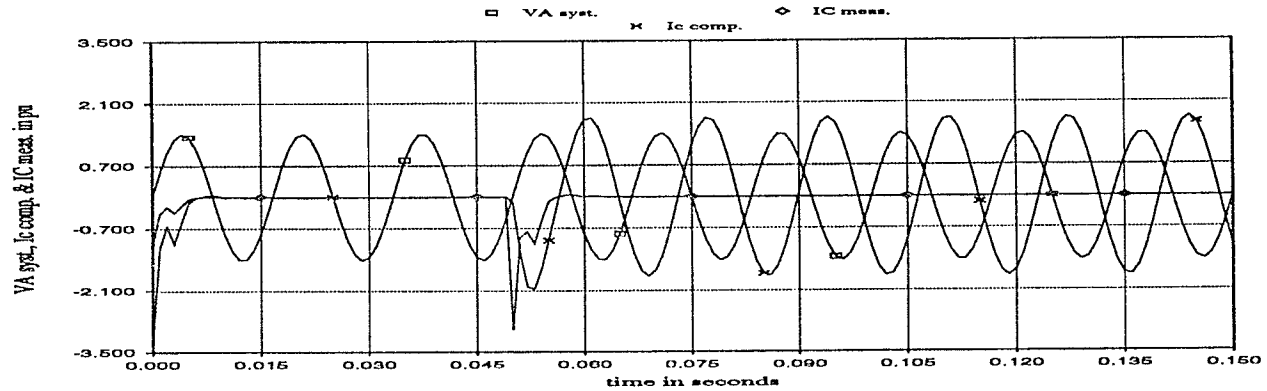
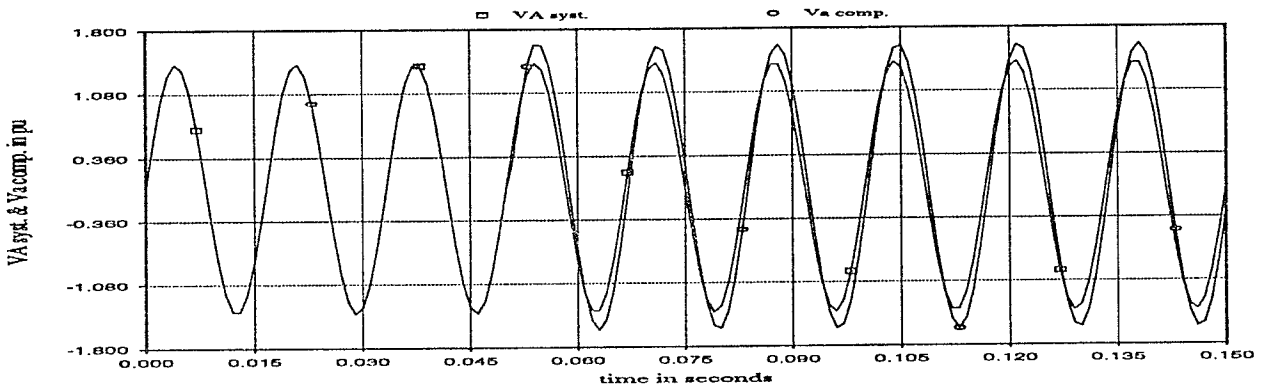
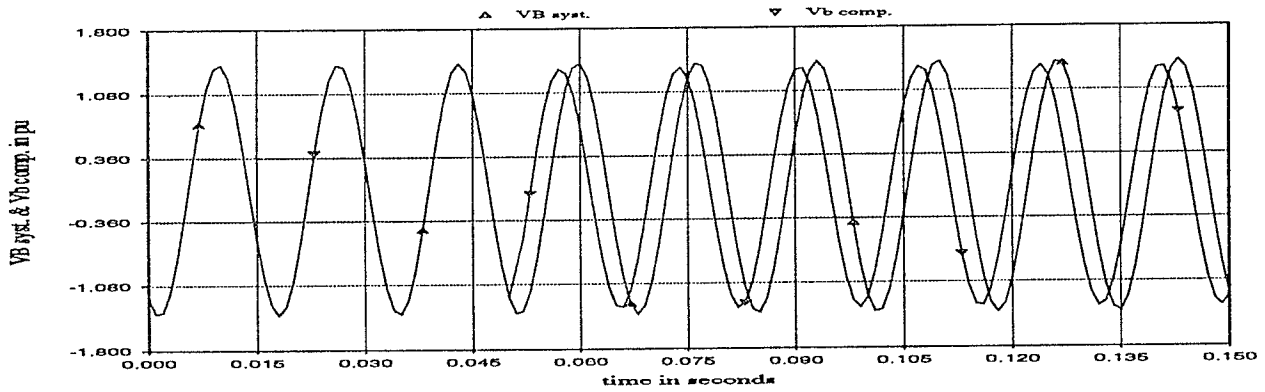


Figure 5.11: (d), (e) and (f) for CASE II

(g)



(h)



(i)

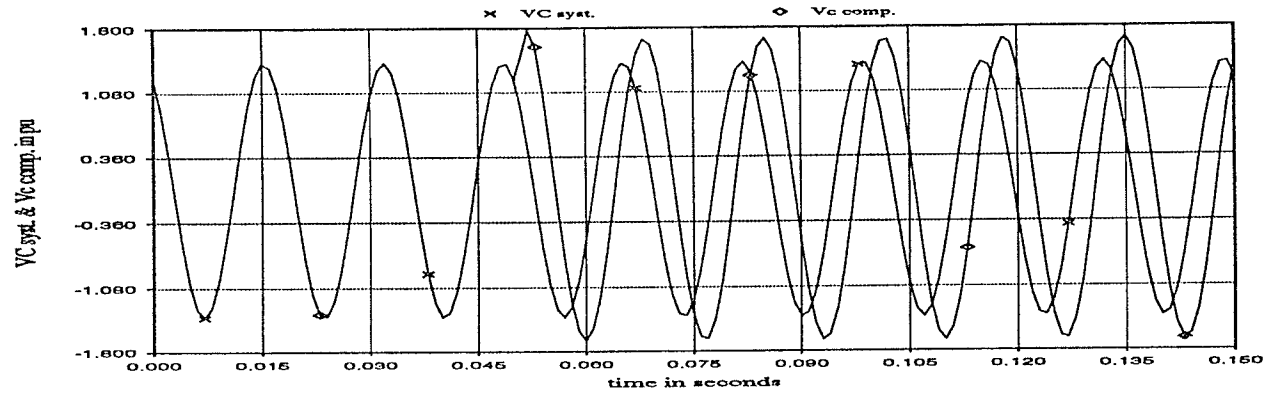
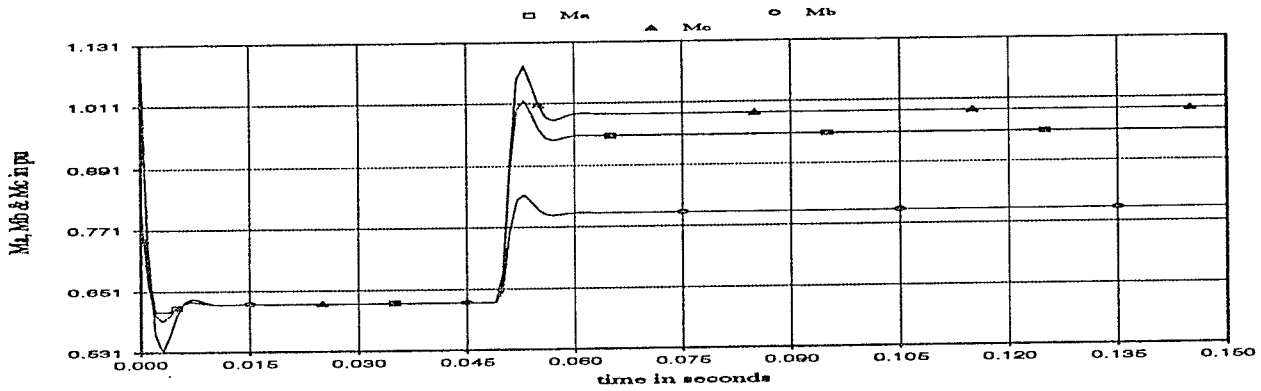
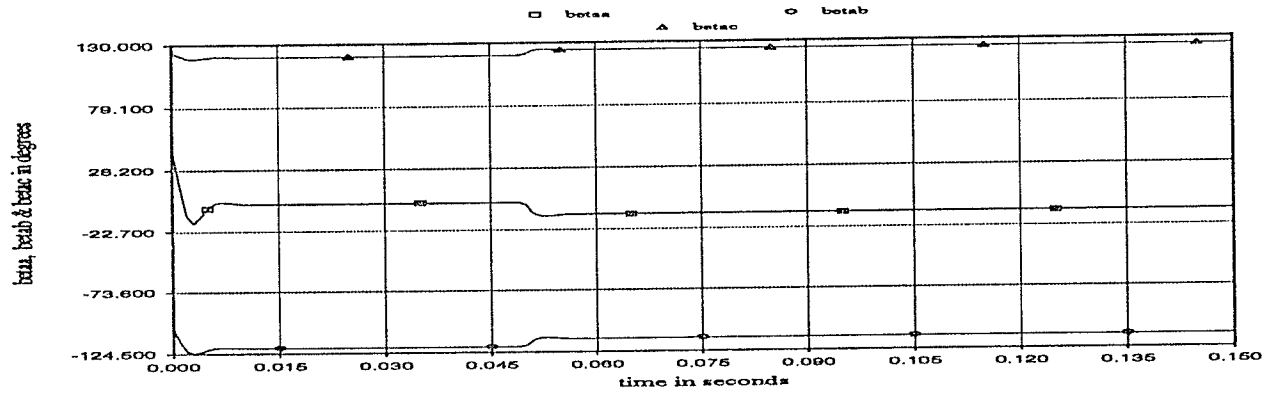


Figure 5.11: (g), (h) and (i) for CASE II

(j)



(k)



(l)

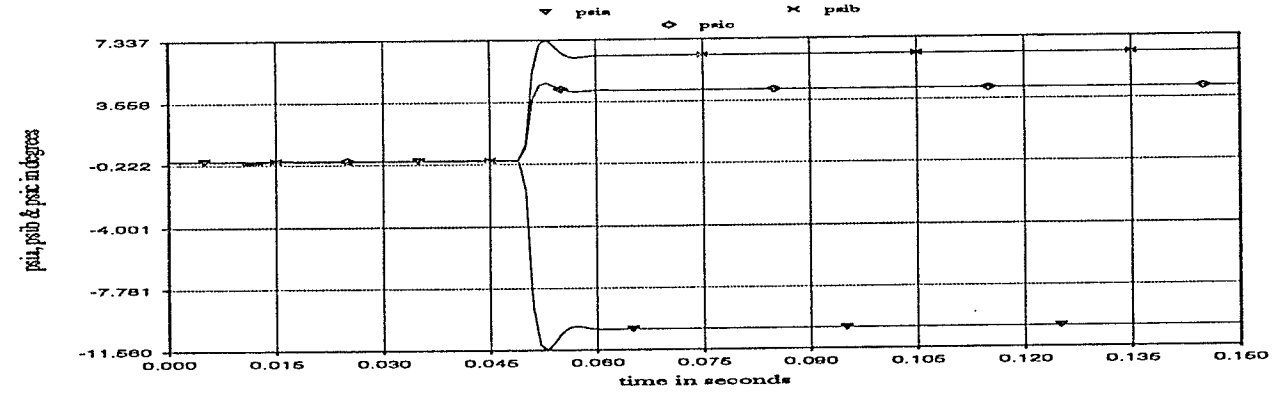


Figure 5.11: (j), (k) and (l) for CASE II

For CASE II the load is again fully compensated in about 1 cycle of the system's fundamental frequency. In this case however the amplitudes of the VSI's output voltages are in general greater than those of the system whereas in Figure 5.10 they were smaller. This result is expected according to the compensation equations (5.1 and 5.3) which were derived for the steady state compensator model. The results in Figure 5.11 are presented in a similar manner to those of Figure 5.10.

A proposed method for reducing the complication of the controls of this SPWM–VSI load compensator could be that of using a feedforward type control structure much like the compensators of Chapter 2. In this case the control equations which were developed in Section 5.3, namely equations 5.16–19 could represent a set of steady–state equations which could be continually solved in order to derive the appropriate modulation variables. These could then be applied directly to the SPWM control block which would send the appropriate signals to the VSIs firing logic thereby eliminating the need for feeding back the system currents and in the process eliminating the need for PI regulators. In such a compensator the calculations could be performed by a PHSC. Harmonic elimination could be performed by using tuned filters as in [2] or by using an optimized PWM switching pattern as in [13].

The chapter which follows will be devoted to brief comparisons of all the methods of load compensation which were presented in this thesis along with a few recommendations for improving their performance.

5.5 Chapter Summary

In this chapter a load compensator which is based on the use of SPWM of a VSI was analysed, designed and simulated on EMTDC. The results proved that

the SPWM–VSI type load compensator is the only ASVC arrangement which will satisfy the objectives of this thesis. However before designing the actual SPWM–VSI a steady–state model was studied and the results proved that if the magnitudes and phase shift angles of the output voltages of the VSI are unequal with respect to the corresponding ac system voltages, then it is possible to generate varying amounts of both imaginary positive–sequence and negative–sequence currents to compensate any rapidly varying three–phase load. A few existing PWM voltage control techniques were studied and the SPWM was found to be the most suitable for the load compensator.

The controls for the load compensator were designed to be of the feedback type with four main control blocks, namely: a measurement and calculations block responsible for measuring and converting the system currents into currents due only to the undesirable symmetrical components; a set of PI regulators with reference input signals set to zero thereby forcing the measured currents from the measurement and calculations block to zero; a SPWM control block which converted the outputs from the PI regulators into appropriate reference and carrier signals thereby deriving proper gating signals for the six GTO switches and which was capable of performing satisfactorily in the event of frequency fluctuations; and a DC control block which utilized PI control in order to maintain the dc capacitor voltage at its peak value by controlling the phase shift angle between the VSI's output voltages and the corresponding system's line–to–neutral voltages. Finally the designed SPWM–VSI load compensator was simulated on EMTDC and the results presented and analysed. The chapter concludes with recommendation for simplifying the controls of the load ASVC type load compensator.

Other conclusions which can be drawn from this chapter includes:

1. The SPWM switching scheme can also be used for harmonic elimination. In

this case a pulse number of 4 (4 pulses per half–cycle) resulted in the elimination of the 5th. and 7th. characteristic voltage harmonics. This resulted from the fact that the SPWM technique can eliminate all harmonics less than or equal to $2p - 1$;

2. The size of the capacitor used in this design is 4 times smaller than a design utilizing a pulse number of 1 and approximately 32 times smaller than a TCR/FC of equivalent rating;

3. The response speed of the simulated load compensator is better than the TCR/FC type compensators of chapter 2 and about 7 times better than the dual–bridge design. Also the compensation range of the SPWM–VSI load compensator is far better than the dual–bridge system and similar to the TCR/FC type load compensators. The controls for the SPWM–VSI were however more involved than those of the TCR/FC type compensator.

4. The simulated SPWM–VSI load compensator compensated all loads within 1 cycle. This is expected to increase to about 2–3 cycles when practical time delays in all the control blocks and in the GTO–VSI are taken into consideration.

Chapter 6

Conclusions and Recommendations

6.1 Conclusions

The main objective of this thesis, as stated in Chapter 1, was to explore the possibility of using ASVCs for load compensation and to compare the findings with current types of load compensators. After investigating the use of firing angle control in CSIs and phase shift angle control in VSIs for positive–sequence current control, the use of PW control in CSIs and VSIs for negative–sequence current control, the analysis, design and digital simulation of a combination of a PWcontrolled CSI and a firing angle controlled CSI in the form of a dual–bridge load compensator, and the analysis, design and digital simulation of a SPWM–VSI type load compensator, the conclusion reached was that the SPWM–VSI type load compensator is the best practical method of utilizing an ASVC for speedy and accurate load compensation.

Each chapter of this thesis contains a summary of the conclusions which were drawn in the course of this study. Some of the other major conclusions which resulted from this study are stated below:

1. The SPWM–VSI load compensator is capable of compensating loads within 1 cycle of the system fundamental frequency.
2. The dual–bridge load compensator cannot serve as a practical load compensator since its compensating speed is slower than both the TCR/FC type compensators and its compensation range is limited.
3. The VSI and CSI type ASVCs can perform equally well for power factor correction if they are synchronized to the ac system and if firing angle control is

used in the CSI and phase shift angle control is used in the VSI.

4. The GTO based ASVC is projected to possess over the SVC advantages which include: a reduction in size and weight (approx. 65%); increased compensation with better transient performance; decreased costs (approx. 30%): the use of smaller sized capacitors (approx. 1/8th); improved harmonic performance due to increased pulse number operation; and better unbalanced reactive power control.

5. The application of a novel method of pulse width control using a sinusoidal modulation of the form $M \sin (2wt + \delta)$ to a CSI renders the CSI capable of generating unbalanced currents for balancing three–phase unsymmetrical loads. The magnitude of the modulating signal, M, controls linearly the magnitude of the resulting negative–sequence current components due to the unbalanced output currents. The phase shift angle δ of the modulating signal controls from 0^{o} to 360^{o} the phase of the resulting negative–sequence current components due to the unbalanced output currents. The third harmonic output current is directly proportional to the difference between the width of the pulse before and after modulation and cannot be eliminated by delta connected transformers or normal inverter operation. The PW control scheme cannot be successfully applied to a VSI since for a period of the control cycle the current flows through the freewheeling diodes.

6. A control scheme which involves the use of a PI regulator, a VCO and a phase detector/error integrator can be used in order to derive appropriate phase shift angles between the VSI's and ac system's voltages thereby maintaining the voltage across the dc capacitor in the SPWM–VSI type load compensator at a predetermined value.

7. A suitable SPWM control scheme which operates effectively in load compensation situations where large frequency fluctuations are expected can be

realized by utilizing two transformations and PI control. The first transformation is used to transform the instantaneous voltages into two–phase (α, β) quantities and the second transforms the two–phase quantities into their equivalent two–axis (d,q) components. The PI controller is used in order to generate appropriate sinusoidal reference signals and a triangular carrier waveform at a measured frequency which is set equal to whatever the reference frequency is. Therefore variations in the reference frequency will be followed by equal variations in the frequencies of the generated SPWM waveforms.

6.2 Recommendations

Since the SPWM–VSI load compensator utilized GTO thyristors whose costs are projected to decrease with time, more research should be done with regards to establishing actual capital and operating costs of the SPWM–VSI type load compensator when compared to the TCR/FC type load compensator.

The use of feedforward, direct calculations type controls with a PHSC for the SPWM–VSI load compensator should be the focus of further research and its performance compared with the feedback system which was designed in thesis.

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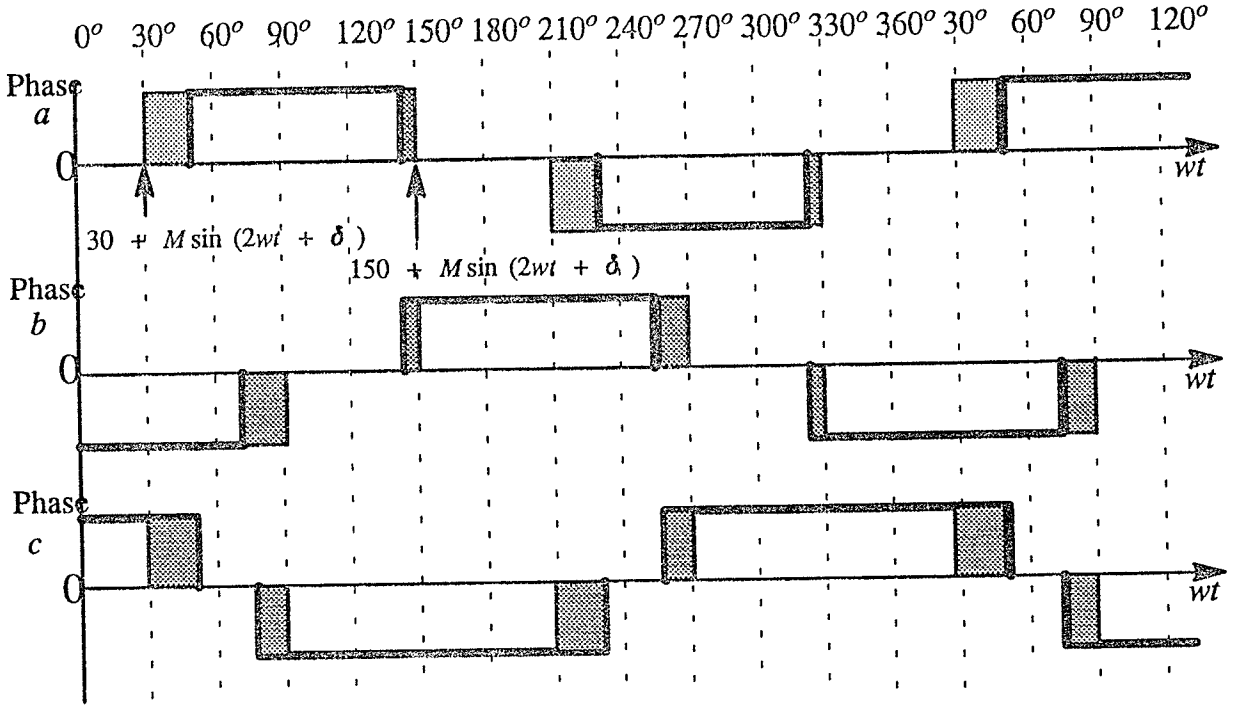
APPENDICES

APPENDIX A

Calculations involving the use of PW control with the sinusoidal modulation variable $M \sin (2wt + \delta)$ applied to a CSI for negative–sequence current control.

Below is an example of the CSI's output current waveforms after the sinusoidal modulation of the form $\alpha = \alpha_o + M \sin (2wt + \delta)$ is applied to each phase. Here the bold lines represent the waveforms after modulation and the shaded areas represent the change in the pulse width with respect to the pre–modulated current waveform.



If we apply Fourier analysis to phase *a* then the resulting expressions for the coefficients of the Fourier cosine and sine series based on the fundamental components only can be calculated as follows :

$$Aa = \frac{2I_d}{\pi} \int_{30^o + M\sin\delta}^{150 + M\sin(240^o + \delta)} \cos(wt)\ dwt \tag{A.1}$$

and

$$Ba = \frac{2I_d}{\pi} \int_{30^o + M\sin\delta}^{150 + M\sin(240^o + \delta)} \sin(wt)\ dwt \tag{A.2}$$

If similar calculations are carried out in the three phases of the inverter and the firing angles are read in the following order,

$$\begin{aligned}
\alpha_a &= 30^o + M \sin (0^o + \delta) \\
\alpha'_c &= 90^o + M \sin (120^o + \delta) \\
\alpha_b &= 150^o + M \sin (240^o + \delta) \\
\alpha'_a &= 210^o + M \sin (0^o + \delta) \\
\alpha_c &= 270^o + M \sin (120^o + \delta) \\
\alpha'_b &= 330^o + M \sin (240^o + \delta)
\end{aligned} \tag{A.3}$$

then for

Phase *a*

$$\begin{aligned}
Aa &= 2\frac{I_d}{\pi} \left\{\sin (150^o + M\sin (240^o + \delta)) - \sin (30^o + M\sin (\delta))\right\} \\
Ba &= 2\frac{I_d}{\pi} \left\{\cos (30^o + M\sin (\delta)) - \cos (150^o + M\sin (240^o + \delta))\right\}
\end{aligned} \tag{A.4}$$

Phase *b*

$$\begin{aligned}
Ab &= 2\frac{I_d}{\pi} \left\{\sin (270^o + M\sin (480^o + \delta)) - \sin (150^o + M\sin (240^o + \delta))\right\} \\
Bb &= 2\frac{I_d}{\pi} \left\{\cos (150^o + M\sin (240^o + \delta)) - \cos (270^o + M\sin (480^o + \delta))\right\}
\end{aligned} \tag{A.5}$$

Phase c

$$Ac = 2\frac{I_d}{\pi}\left\{\sin(30^o + M\sin(\delta)) - \sin(270^o + M\sin(480^o + \delta))\right\}$$
$$Bc = 2\frac{I_d}{\pi}\left\{\cos(270^o + M\sin(480^o + \delta)) - \cos(30^o + M\sin(\delta))\right\}$$

(A.6)

From the above coefficients, expressions for the fundamental current component in each phase, as a function of the modulation variables M and δ, can be found.

$$Ia = Aa\cos wt + Ba\sin wt$$
$$Ib = Ab\cos wt + Bb\sin wt$$
$$Ic = Ac\cos wt + Bc\cos wt$$

(A.7)

where the magnitude of Ia is given by the expression

$$|Ia| = \sqrt{Aa^2 + Ba^2}$$

(A.8)

and the phase angle of Ia is given by the expression

$$\phi_a = \text{atan}\left\{\frac{Aa}{Ba}\right\}$$

(A.9)

The currents in phases b and c can be expressed in a similar manner.

If the symmetrical component transformation is now applied to these currents as shown below:

$$I_2 = \left\{ Ia + a^2Ib + aIc\right\}\frac{1}{3}$$

(A.10)

then it is possible to calculate any magnitude and phase for the resulting negative–sequence current as a function of M and δ. An example is given below.

Example

Suppose $M = 10^{\circ}$ and $\delta = 120^{\circ}$. If for ease of calculation we assume that $\frac{2I_d}{\pi} = 1.0\ pu$, then by equations (A.4–6), the following are obtained:

$Aa = -0.1247$, $Ba = 1.647$, $Ab = -1.49$, $Bb = -0.715$, $Ac = 1.613$ and $Bc = -0.931$

and from equations (A.8,9),

$Ia = 1.652\angle -4.33^{\circ}$, $Ib = 1.653\angle -115.63^{\circ}$ and $Ic = 1.863\angle 120^{\circ}$

If the symmetrical component transformation is now applied according to equation (A.10), then the output negative–sequence current which could be derived is given by $I_2 = 0.144\angle 240^{\circ}$ •

APPENDIX B

List of Components for the simulated dual–bridge load compensator:

Positive–sequence Bridge

5th filter: C = 80 uF, L = 3.52 mH, R = 0.133 Ω

7th filter: C = 80 uF, L = 1.795 mH, R = 0.095 Ω

11th filter: C = 40 uF, L = 1.454 mH, R = 0.12 Ω

13th filter: C = 40 uF, L = 1.04 mH, R = 0.102 Ω

H.P filter: C = 70 nF, L = 0.348 mH, R = 4.46 Ω

Ld = 23.28 mH

Xtr = 40%

Negative–sequence Bridge

3rd filter: C = 80 uF, L = 9.77 mH, R = 0.22 Ω

5th filter: C = 8o uF, L = 3.52 m H, R = 0.133 Ω

7th filter: C = 80 uF, L = 1.795 mH, R = 0.095 Ω

11th filter: C = 40 uF, L = 1.454 mH, R = 0.12 Ω

13th filter: C = 40 uF, L = 1.04 mH, R = 0.102 Ω

H.P filter: C = 70 uF, L = 0.348 mH, R = 4.46 Ω

Xtr = 20%

APPENDIX C

List of parameters for the simulated SPWM–VSI load compensator

Y/Δ transformer: 13.2 KV / 762 V with Xt = 20 %

Dc side capacitor, Cd = 1553.92 uF

Base Quantities for Y–side

S_{BASE} = 1.0 MVA V_{BASE} = 13.2 KV I_{BASE} = 43.74 A Z_{BASE} = 174.23 Ω

Base Quantities for Δ–side

S_{BASE} = 1.0 MVA V_{BASE} = 0.762 KV I_{BASE} = 757.68 A Z_{BASE} = 0.581 Ω

Peak capacitor voltage = 1.2 pu = 914.40 V(dc) ref. to secondary side

H.P filter from 11th harmonic: C = 40 uF, L = 1.454 mH, R = 0.12 Ω

GTO switches required to block forward voltage of 914.40 V.