INVESTIGATION OF SERIES COMPENSATION OF DC CONVERTER STATION

by

Fei Zheng

A Thesis
Submitted to the Faculty of Graduate Studies
in Partial fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

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ABSTRACT

The application of series capacitors (SCD) in an AC transmission line to provide reactive power compensation had been attempted as early as in late 1920s. Recently, using a series capacitor to compensate a DC converter station in HVDC transmission system was found to be much more attractive than other compensation methods, not only because the SCD is most economic, but also because the SCD can effectively increase the short circuit capacity of a weak AC system leading to the possibility of enhanced system performance and voltage control. However, an interchange of energy between charge in the SCD and magnetic energy in the inverter transformer (TR) will seriously inhibit the AC/DC system performance, even to an unacceptable level. This is so called ferro-resonance, which occurs at a subharmonic frequency.

This thesis systematically investigates the ferro-resonance performance in an AC/DC system, and analyses the different effects of system elements on ferro-resonance. Basically, the transformer saturation and the load rejection are the prerequisites of a ferro-resonance.

This thesis presents the results of several mitigative methods of the digitally-simulated performance of the following schemes:

1. Shunt or series subharmonic filter
2. Metal oxide varistor (MOV)
3. C-type filter
4. Series damping filter scheme
5. Parallel damping filter scheme
6. Shunt 2nd harmonic filter
7. With optimal control parameters in the DC system
8. Switching resistor scheme
9. Thyristor controlled resistor
10. Fundamental blocking filter
11. Protective bypass together with Pre-insertion resistor

These methods can effectively eliminate the ferro-resonance in different fault recovery processes of AC/DC systems. Now the only concern is that subsynchronous damping schemes may increase the cost. Economic evaluation at the last of the thesis shows that the economic solution for ferro-resonance does exist. It seems that the series compensation for DC converter station is passable in both a technology aspect and an economic aspect.

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Finally, the author expresses sincere thanks to her parents and her younger sister. Although they are as far as the other end of the earth, their love is with the author all the time. Every evening, immersing in the Winnipeg's bloody sunset, the author always thinks of that in the sun-rising country, three nostalgic hearts are blessing her. Blood is thicker than water. Their love gives the immense magic power in their prayers. This blesses the author spend every day and night peacefully.

SUMMARY OF THE THESIS

With HVDC transmission as it becomes more and more widespread, the rather detailed research, even in the very specific topic, appears more and more attractive and necessary. Series compensation used in long-distance AC transmissions is not a novel idea. But only in recent years, an increasing interest has been shown in using series capacitor (SCD) to compensate the DC converter station to possibly provide a lower cost but reliable alternative even to static compensators. When an SCD is used at the HVDC converter station feeding into a weak AC system, a ferro-resonance problem, which is a special kind of subsynchronous oscillation caused by the remanence flux in the converter transformer, leads to a persistent saturation distortion state. Fourier analysis shows quite different harmonic components in a single-phase model (no HVDC representation) and three-phase model (with HVDC representation).

For the investigation in the single phase test system, the ferro-resonance effect, associated with the fault clearing near an unloaded transformer, is initiated by the remanent flux on the transformer and the residual voltage on the series capacitor left by the fault current. The subharmonic depends on initial conditions and L-C oscillation time constant (where, the non-linear element plays a key role). Subharmonic filters in different positions are recommended. A C-type filter (tuned at 60 HZ and 120 HZ) can also help the AC system to recover to steady state. An MOV (metal oxide varistor) can decrease the effect of ferro-resonance. The R + SWITCH method, the thyristor controlled resistor method and the fundamental blocking filter method can successfully eliminate the ferro-resonance in the fault recovery process of the single phase system.

The ferro-resonance phenomenon occurs in the HVDC system starting process and almost all kinds of AC/DC line to ground fault recovery processes, which seriously affects the stability of the HVDC system. To solve this problem, two basic ideas can be considered: one way is to lower 2nd and 3rd harmonic AC impedance by filters. Sometimes it is possible to get harmonic damping of 2nd and 3rd harmonics by DC link controls: Another way is to remove subsynchronous energy from the series capacitor and magnetic circuit. Based on these two points, some methods are tried and several of them have been proven can be used to solve this problem successfully, such as the series/parallel damping filter method, the 2nd harmonic filter method, the R + SWITCH method, the thyristor controlled resistor method, and the fundamental blocking filter method. In order to get a good balance of reactive power at the rated state of 810 MW, the filters supply approximately 200 MVAR of reactive power. AC filters are redesigned to add non-characteristic harmonic damping. The rating of new filters is 217 MVAR. By calculating

the harmonic distortion constant, it shows new filters didn't increase the telephone interference. So the design of new filters is reasonable both in system operation and telephone interference. The multiple run feature in the computer simulation tools used (known as EMTMR) supplies a good tool to get optimal control parameters for improved fault recovery.

The economic evaluation of the SCD with the corresponding subsynchronous damping scheme shows that except the SCD with MOV + THYRISTOR method which is much more expensive, the costs of the other methods are only a little bit higher than the SCD itself. So even with the subsynchronous damping scheme, series compensation is still an economic way for DC converter compensation.

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LIST OF SYMBOLS

Tabulated below are some of the more frequently occurring symbols used in the text. Other symbols, which occur say only once, have been explained where used.

CS	Norton Source
DOV	Dynamic Overvoltage
DOC	Dynamic Overcurrent
EMTDC	Electromagnetic Transient Program for DC System
EMTFS	EMTDC Snapshot Handler
EMTMR	EMTDC Multiple Run Analysis Program
EMTSP	EMTDC Function Synthesis and Fourier Analysis Program
Es	Equivalent AC Source
G	Conductance
HBP	Hard Bypass
MOV	Metal Oxide Varistor
P_{AC}	Active Power Flow At The AC Bus Bar
P_{DC}	Active Power Flow At The DC Bus Bar
PIR	Pre-insertion Resistor
Q_{AC}	Reactive Power Flow At The AC Bus Bar
Q_C	AC Reactive Power Flow Through The Series Capacitor
Q_{DC}	Reactive Power Flow At The DC Bus Bar
Q_F	AC Reactive Power Supplied By The AC Filter Group
SCD	Series Capacitor Device
SCR	Short Circuit Ratio
SEGN11	EMTDC Harmonic Spectrum Generator Function
SLG	Single LIne to Ground
SLGF	Single Line to Ground Fault
3LG	Three Line to Ground
3LGF	Three Line to Ground Fault
TIF	Telephone Interference Factor
TR	Transformer
UNIPLOT	A Computer Plotting Program
V_{AC}	AC Bus Bar Voltage
VCD	Voltage Control Device
V_{DC}	DC Bus Bar Voltage

VDCL	Voltage Dependent Current Limit
Xc	The Reactance Of The Series Capacitor
Xs	AC System Equivalent Reactance
Y_F	The Equivalent Conductance Of The AC Filter Group

Chapter 1

INTRODUCTION

1.1 THE PROBLEM OF USING SERIES COMPENSATION

Whether a converter operates as an inverter or a rectifier, it absorbs a large amount of reactive power from the AC system (for rectifier: Q = 30-50% P; for inverter: Q = 40-60% P). This brings some new problems for the AC system, especially, the stability problem for the weak AC system (SCR < 1.5). To solve this problem, use can be made of various compensating devices. Among several compensation methods, series compensation (a series capacitor SCD between the converter and the AC system) appears attractive because it effectively increases the short circuit capacity of the AC system leading to the possibility of enhanced system performance and voltage control. It shows the series capacitor can provide almost a constant commutation voltage in both light load and heavy load cases.

However, a ferromagnetic resonant interchange of energy between charge in the series capacitor and magnetic energy in the converter transformer will seriously inhibit AC/DC system performance, even to an unacceptable level. The Manitoba HVDC Research Centre undertook previous research in which indicated that the ferro-resonance problem can be readily overcome. Based on this encouraging result, several cases and methods are tried and compared in this thesis.

1.2 THE ADVANTAGES OF USING SERIES COMPENSATION

1.2.1 Economics

Table 1.1 shows the economic evaluation of several compensation devices [2]. From it, we know: using the SCD is much cheaper than other devices.

Table 1.1 Voltage Control Device Economic Evaluation

Device	Economic Evaluation (% of station capital cost) Capital Cost	Capitalized Operational Costs	Total Lifetime Costs
*Synchronous Compensator (2 units)	40	15	55
" " (1 unit)	21	11	32
Thyristor controlled reactor	17	6	23
Thyristor switched capacitor	18	5	23
Metal oxide varistor	14	negligible	14
Series capacitor device	13	1	14

*Study criteria are met with one unit, but two are provided for reliability.

1.2.2 Limit Dynamic Overvoltage

HVDC system's load rejection will affect the voltage at the commutation bus. The series capacitor can maintain this voltage at nearly 1 p.u.

1.2.3 Supply Reactive Power

For a shunt capacitor, when the reactive power isn't enough in the system, the bus voltage will drop, then the shunt capacitor will supply less reactive power ($Q \infty V^2$); oppositely, for a series capacitor, when the reactive power isn't enough in the system, the system current will become larger, then the series capacitor will supply more reactive power ($Q \infty I^2$). So the series capacitor has a better characteristic for reactive power supply in a dynamic system.

1.2.4 Increase The Short Circuit Ratio (SCR)

The definition of the short circuit ratio (SCR) is:

$$SCR = \frac{S_{ac} \cdot Q_{filt}}{P_{dc}} = \frac{V_{l\text{-}l}^2}{P_{dc}} \left(\frac{1}{|Z_s|} \frac{1}{|Z_f|}\right) \quad \text{.....(1.1)}$$

where:

Sac = short circuit ratio of the AC system
Qfilt = reactive power supplied by AC filters
Pdc = rated DC power
Vl-l = commutating voltage at rms (rated mean square) value
Zs = the AC system impedance
Zf = the AC filter impedance

For our simulation system, Vl-l = 230.0 KV, Pdc = 810.0 MW, |Zf| = 263.44 Ω.

No SCD, |Zs| = 37.39 Ω,

$$SCR_1 = \frac{230.0^2}{810.0} \left(\frac{1}{37.39} \frac{1}{263.44}\right) = 1.5 \quad \text{.....(1.2)}$$

With SCD, |Zs| = 22.37 Ω,

$$SCR_2 = \frac{230.0^2}{810.0} \left(\frac{1}{22.37} \frac{1}{263.44}\right) = 2.67 \quad \text{.....(1.3)}$$

From above calculation, it can be seen that SCD increases the AC system's SCR from 1.5 to 2.67.

1.3 SCOPE OF THE THESIS

1.3.1 Mitigative Methods Studied In This Thesis

This thesis presents the results of several mitigative methods of the shunt or series digitally-simulated performance of the following schemes:

1. Shunt or series subharmonic filter
2. Metal oxide varistor (MOV)

3. C-type filter
4. Series damping filter scheme
5. Parallel damping filter scheme
6. Shunt 2nd harmonic filter
7. With optimal control parameters
8. Switching resistor scheme
9. Thyristor controlled resistor
10. Fundamental blocking filter

Simulation results show that the above methods can effectively eliminate the ferro-resonance in an AC or DC system.

1.3.2 Simulation Program Used In This Thesis

In order to investigate the comparative behaviour of the mitigative methods in various system disturbances, it was considered necessary to undertake comprehensive time domain simulation studies that fully considered the effects of harmonics and imbalances as well.

EMTDC (Electromagnetic Transient Program For DC System)[1] was used to perform digital simulation. This program has been developed at Manitoba Hydro and is available through the Manitoba HVDC Research Centre.

In EMTDC, power system dynamics are simulated in time domain with 3 phase representation of the AC network. It includes frequency dependent distributed transmission models, generalized 6 pulse bridge arrangements with associated damping circuits, dc pole and valve group control models, electric machine models, governor and exciter models, transformer saturation, metering and control devices, etc.

1.3.3 Economic Evaluation

One of the advantages to use the series capacitor for DC compensation is its economics. Even with the subsynchronous damping circuit, we don't want to destroy its economics. So it is necessary to look at the economic evaluation for SCD corresponding to every ferro-resonance mitigative method.At the end of the thesis, an economic evaluation is given. From the economic evaluation, it can be seen that the economic solutions of the ferro-resonance problem do exist.

Chapter 2

EXPLANATION OF FERRO-RESONANCE PHENOMENON

2.1 TRANSFORMER INRUSH CURRENT

Fig. 2.1 shows how the transformer inrush current is produced when the transformer is re-energized or its terminal voltage recovers following a fault. Because of the iron core remanence flux at the "worst case" switching, the axis of flux has $2\emptyset_0$ offset ($\emptyset_0$ is the remanence flux) after "switching on" time t_2, i.e., the first time switch operation (switching on) causes flux axis to have $\emptyset_0$ offset, the second time switch operation (switching off) causes flux axis to have another $\emptyset_0$ offset.

Let

$$e=N\frac{d\emptyset}{dt}=E_m\sin(wt) \qquad \text{.....(2.1)}$$

Then

$$\emptyset = \frac{1}{N}\int e\,dt$$

$$=\frac{1}{N}\int E_m \sin(wt)\,dt + C$$

$$= -\frac{E_m}{w\,N}\cos(wt) + C$$

$$= -\emptyset_m \cos(wt) + C \qquad \text{.....(2.2)}$$

Where

$$\emptyset_m = \frac{E_m}{w\,N}$$

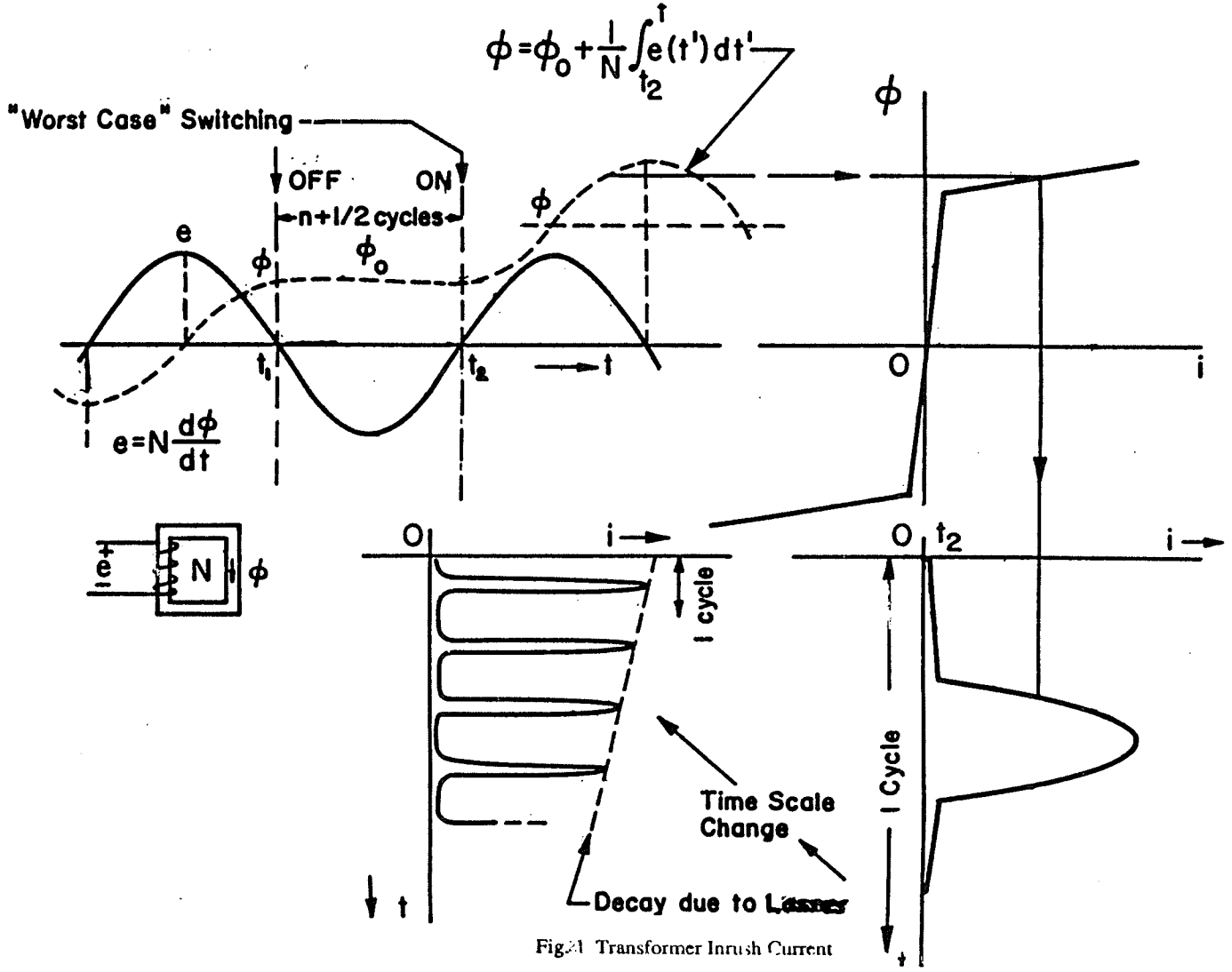


Fig. 1 Transformer Inrush Current

2.1.1 $0 \leq t \leq t_1$

$$\emptyset = -\emptyset m \cos(wt) + C_1 \text{.....(2.3)}$$

When $t = 0$, $\emptyset = -\emptyset m$

From (2.3)

$$\emptyset = -\emptyset m = -\emptyset m \cos 0 + C_1 = -\emptyset m + C_1$$

$$\therefore C_1 = 0 \text{.....(2.4)}$$

Substitute (2.4) into (2.3):

$$\emptyset = -\emptyset m \cos(wt) \text{.....(2.5)}$$

This shows the remanence flux is affected by "switching off" time.

Let's choose the "worst case switching off" time: $w t_1 = \pi$.

From (2.5):

$$\emptyset = \emptyset_0 = -\emptyset_0 \cos\pi = \emptyset m$$

$$\emptyset_0 = \emptyset m \text{.....(2.6)}$$

Substitute (2.6) into (2.5)

$$\emptyset = -\emptyset_0 \cos(wt) \text{.....(2.7)}$$

2.1.2 t > t2:

$$\emptyset = -\emptyset_0 \cos(wt) + C_2 \text{.....(2.8)}$$

It shows the increasing of flux is affected by the "switching on" time.

Choose the "worst case switching on" time: $w\, t_2 = 2\pi$.

From (2.8)

$$\emptyset = \emptyset_0 = -\emptyset_0 \cos(2\pi) + C_2 = -\emptyset_0 + C_2$$

$$\therefore C_2 = 2\,\emptyset_0$$

$$\emptyset = -\,\emptyset_0 \cos(2\pi) + 2\,\emptyset \text{.....(2.9)}$$

Compare (2.7) and (2.9), it is obviously that the flux axis in (2.9) has $2\,\emptyset_0$ offset.

The excessive flux can exceed the knee point of transformer saturation. This causes inrush current which contains a large 2nd harmonic. Transformer inrush current can decay with losses.

2.2 THE FERRO-RESONANCE PROBLEM

As early as in 1937, W. Butler and C. Concordia found the ferro-resonance problem in the series capacitor application[11]. In 1966, S. V. Vonsovskii theoretically analysed the ferro-resonance phenomenon[12]. In 1968, G. W. Swift presented his analytical approach[7].

The definition of ferro-resonance given by G.W. Swift [7] is:

Ferro-resonance is the special case of jump resonance in which the nonlinearity is iron-core magnetization. Jump resonance refers to a condition in a sinusoidally excited system: if an incremental change in the amplitude or frequency of the input to the system causes a sudden jump in signal amplitude somewhere in the system, jump resonance is said to have occurred.

Look at a simplified ac system Fig. 2.2.

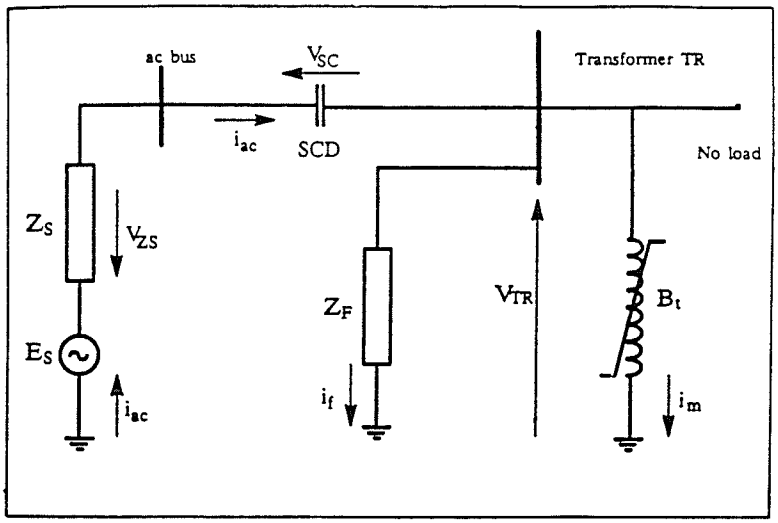


Fig. 2.2 A Simplified Representation Of The AC System At The Inverter End

Let

$$V_{TR}(t) = Vm \sin(wt)$$

$$\emptyset\,(t) = \frac{V_m}{w}\cos\,(wt)$$

$$Im\,(t) = K_1\,\emptyset(t) + K_2\,\emptyset^7(t) + AV_m(t).....(2.10)$$

Where

$$K1 = 10^{-2}$$

$$K2 = 10^{-7}$$

$$A = 10^{-3}$$

The central I-Ø curve is obtained by using

$$I_m(t) = K_1\,\emptyset(t) + K_2\,\emptyset^7(t).....(2.11)$$

During the system fault recovery process, the transformer core would be driven into saturation when the flux Ø exceeds the saturation level Øs. The non-linear reactance Bt in Figure 2.2 represents transformer saturation characteristic which, in general, can be

described by the saturated inductance Ls, non-saturated inductance Ln, and flux value at the knee point Øs. Since Ln is much bigger than Ls, thus an approximate expression for the inrush current is given by:

$$Im(t) = \begin{cases} (Ø-Øs)/Ls & \text{when } Ø>Øs \\ Ø/Ln & \text{otherwise} \end{cases} \quad \cdots\cdots\cdots(2.12)$$

At fault clearing, which is assumed to occur at zero-crossing of the short circuit current, the transformer terminal voltage Vtr recovers at the maximum of its fundamental component. But according to the fundamental circuit law, the voltage at the series capacitor Vsc and the transformer flux Ø can't be changed immediately. So these two offsetting values Ø (ton) and Vsc (toff) determine the initial conditions of the system after fault clearing.

The transformer voltage Vtr is determined by the source voltage Es, system impedance voltage drop Vzs, and the capacitor voltage Vcs according to

$$Vtr(t) = ES(t) - Vzs(t) - Vsc(t) \quad \cdots\cdots\cdots(2.13)$$

Because capacitor voltage Vsc can be offset, thus the transformer voltage Vtr can also be offset. Constant offset of the transformer voltage would then cause a continuous, proportional to the offset level, increase of the transformer core flux Ø. This causes the ferro-resonance.

The following investigation shows that the ferro-resonance phenomenon appears a quite different performance in the single phase circuit which doesn't contain a HVDC model and the three-phase circuit which contains a HVDC representation.

2.3 FERRO-RESONANCE IN SINGLE-PHASE CIRCUIT (NO HVDC REPRESENTATION)

The AC system for the single-phase study is shown in Fig. 2.3 [2].

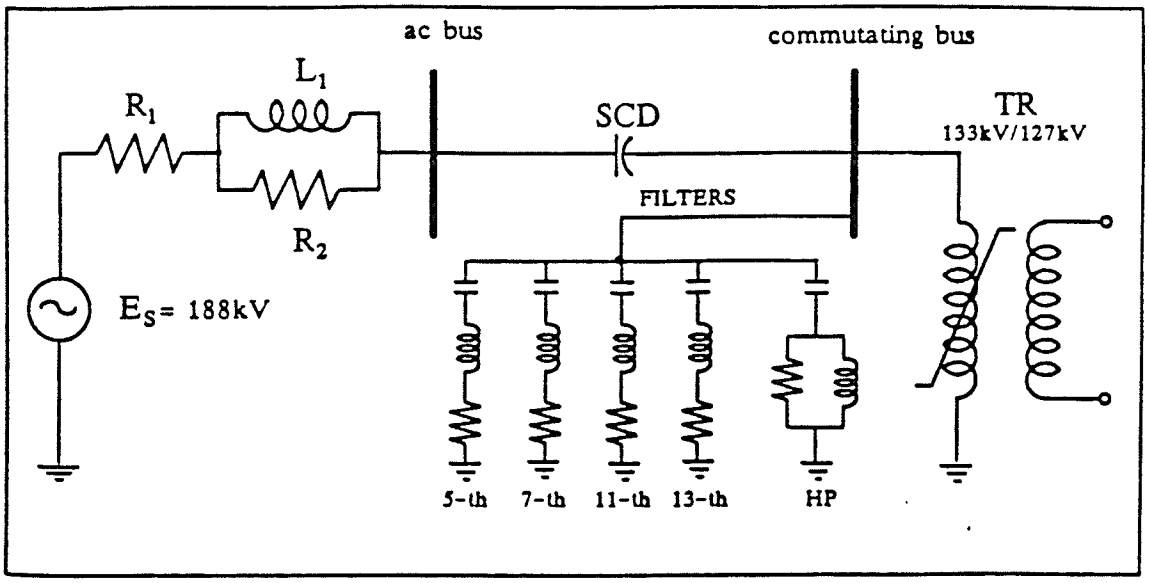


Fig. 2.3 AC System For Single-phase Study

When a fault occurs in the AC system and the saturation of the transformer TR (which is modelled using the subroutine TSAT21 in EMTDC simulation program), the AC system can't recover from the fault. Instead of the rated steady state voltage and current, the ferro-resonance steady state voltage and current persist (see Fig. 2.5).

Using EMTFS support program to Fourier analyse the distorted waveform, it is shown: there is a significant 20 HZ subharmonic (see Fig. 2.4).

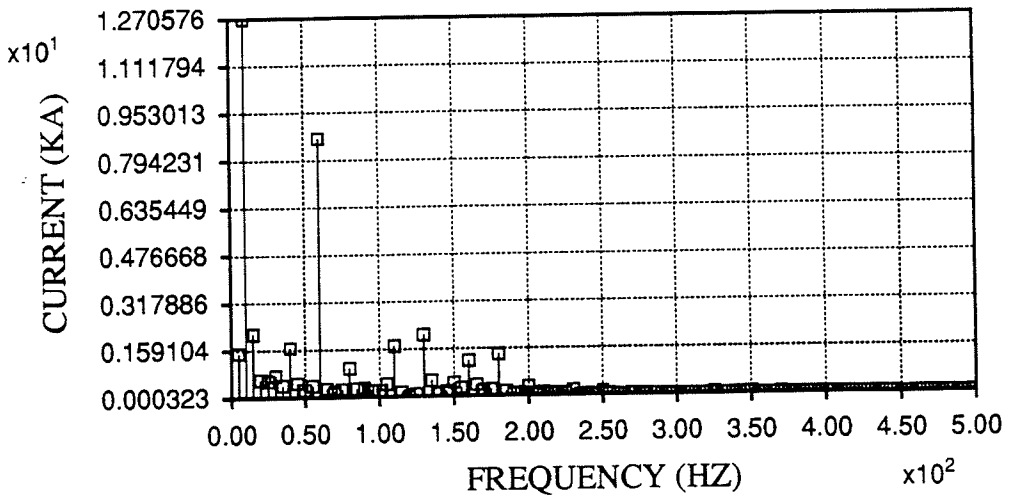


Fig. 2.4 Fourier Analysis Of AC Current In Single Phase Circuit Fault Recovery Process

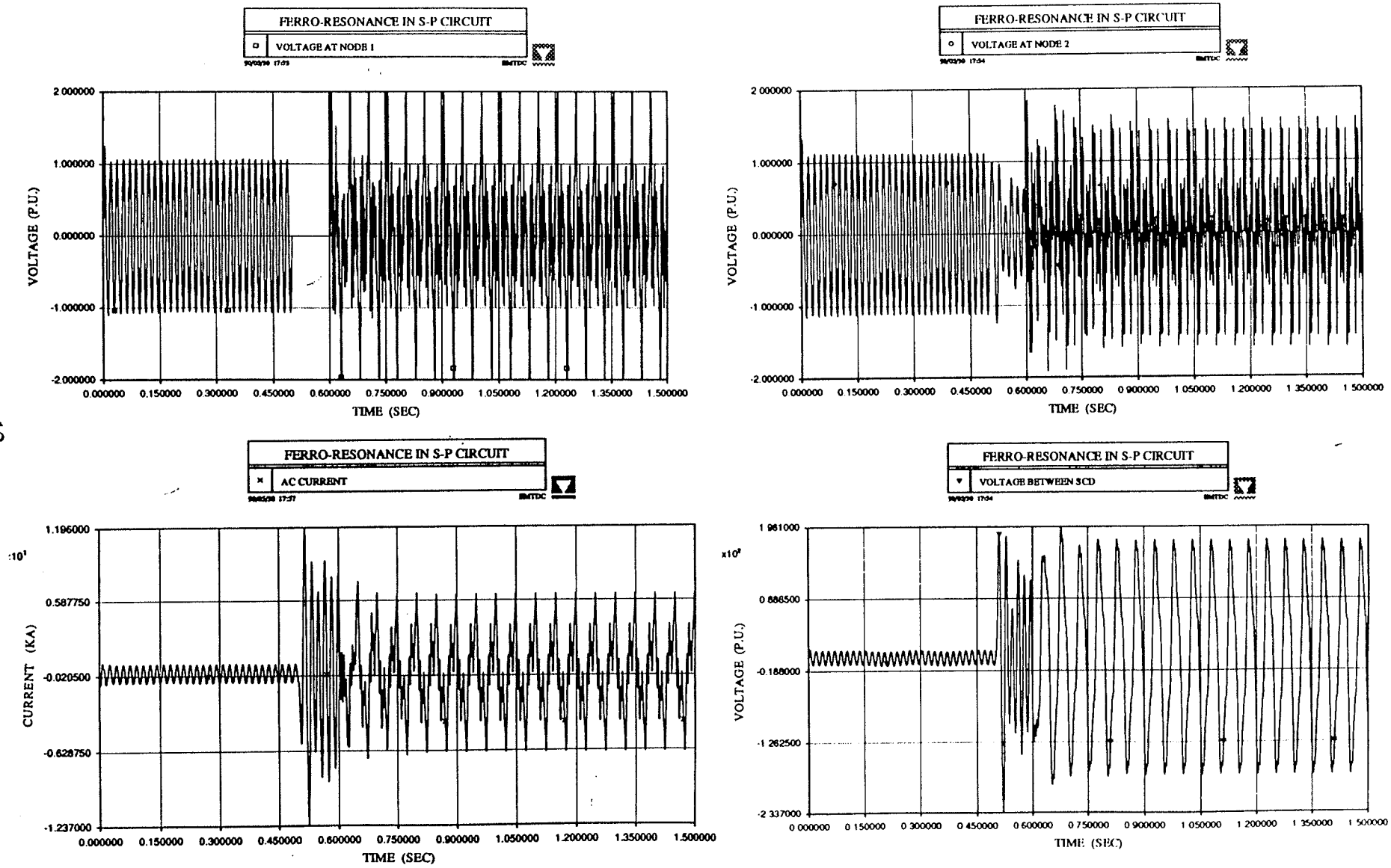


Fig. 2.5 Ferro-resonance In Single-phase Circuit

2.4 FERRO-RESONANCE IN THREE-PHASE CIRCUIT (WITH HVDC REPRESENTATION)

The test system consisting a point-to-point DC transmission system with the SCD connected to the inverter commutating bus is shown in Fig. 2.8. The DC system is a monopolar, six pulse, rated 810 MW (1800 A, 450 KV) at the inverter. The receiving end and sending end AC systems are separated by a 556 mile transmission line.

The AC network, both at the rectifier and inverter ends, are modelled as infinite sources separated from their respective commutating buses by system impedances. The impedances are represented as an R-RL network having the same damping at the fundamental and the second harmonic frequencies. The impedance angles of the receiving end and the sending end systems are selected to be 78 and 85 degrees respectively.

The magnitude of the impedances are selected to provide SCD of 4.0 at the sending end. Please note that the SCD can increase the short circuit ratio of the receiving end from 1.5 to 2.67.

Fig. 2.9 shows the ferro-resonance in HVDC system starting process. Fourier analysis shows there is not a dominate subharmonic or a dominate harmonic in this case (see Fig. 2.6). The 60HZ fundamental frequency is still the main component. This is different from the AC system case.

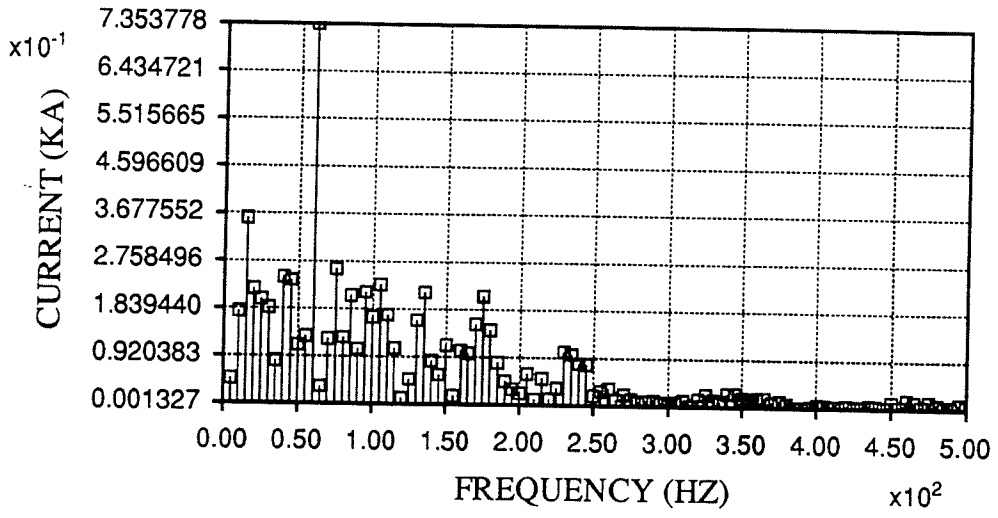


Fig. 2.6 Fourier Analysis Of AC Current In HVDC System Starting Process

2.5 EXPLANATION OF FERRO-RESONANCE PHENOMENON

Because the transformer inductance is non-linear, the time constant of energy interchanging between capacitor and transformer inductance is changable. This causes the uneven oscillation of transformer flux. The frequency of the oscillation depends on the fundamental system frequency and occurs at subharmonic frequencies. The subharmonic also depends on transformer remanence flux and the time constant of energy interchange as well as the knee point of I-Ø curve, the parameters of SCD and transformer TR inductance.).

For the ac system Fig. 2.3, ferro-resonance contains a large 20HZ subharmonic. The process can be shown in Fig. 2.10.

Obviously, transformer saturation is the key to both ferro-resonance and inrush current. The difference between two cases is: without series capacitor,the remanence energy in TR inductance (caused by remanence flux $Ø_0$) decays with losses. When remanence flux $Ø_0$ decays to $Ø_0 = 0$, the inrush current will disappear. The system will recover to rated steady state voltage. This causes that the inrush current can only appear on one side, containing a lot of ripples. Fourier analysis shows that every ripple contains an amount of 2nd harmonic. It is widely accepted that inrush current contains lots of 2nd harmonics. When a series capacitor exists, it can absorb or release energy to the TR inductance. This may destroy the regular arrangement of current ripples. The DC component of the TR inrush current charges the series capacitor with a DC component, which as it discharges through the transformer, causes the transformer flux to migrate to the opposite polarity, reaching one sided saturation. The resulting inrush current with its DC component causes the series capacitor to charge resulting in a continuation of the ferro-resonance (Fig. 2.7).

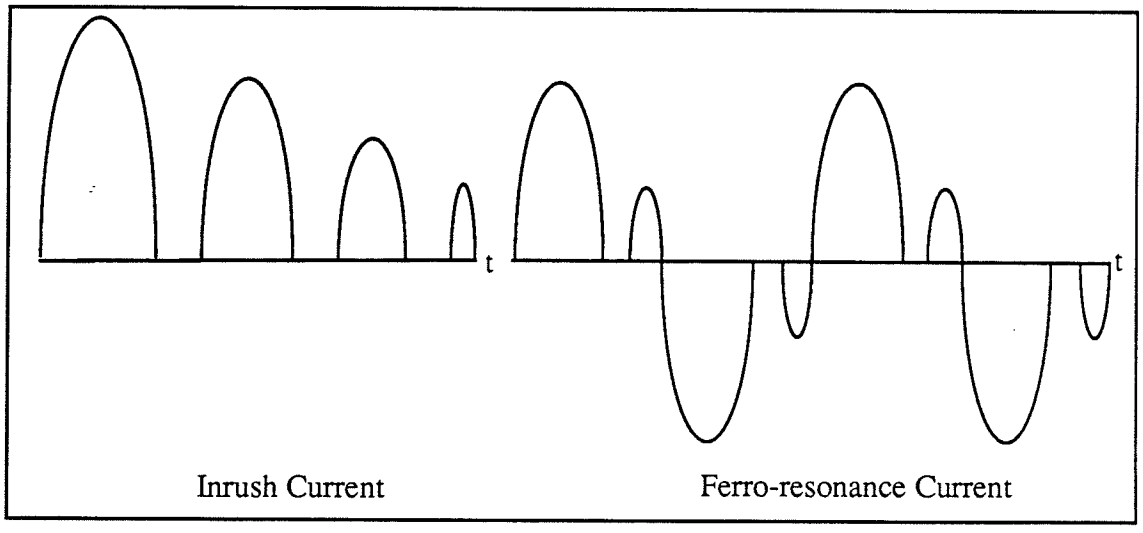


Fig. 2.7 A Comparison Of Inrush Current And Ferro-resonance Current

This causes a ferro-resonance to generate a subharmonic which is not definite. It depends on the structure of system and parameters on linear and non-linear elements. This assumption is proved by the previous investigation, i.e., in HVDC system, where the ferro-resonance current contains a large range of harmonics, but there is no a dominant subharmonic in this case. This is different from the AC system case.

2.6 CONCLUSIONS

The ferro-resonance is a special kind of energy oscillation between the series capacitor device and the transformer non-linear inductance. Quite different from the transformer inrush current, the ferro-resonance current occurs at a subharmonic frequency, which depends on the system structure and the system parameters. Digital simulation shows that the ferro-resonance seriously affects the AC system fault recovery process and the HVDC system starting process. So the series compensation couldn't be used until this problem can be successfully overcome.

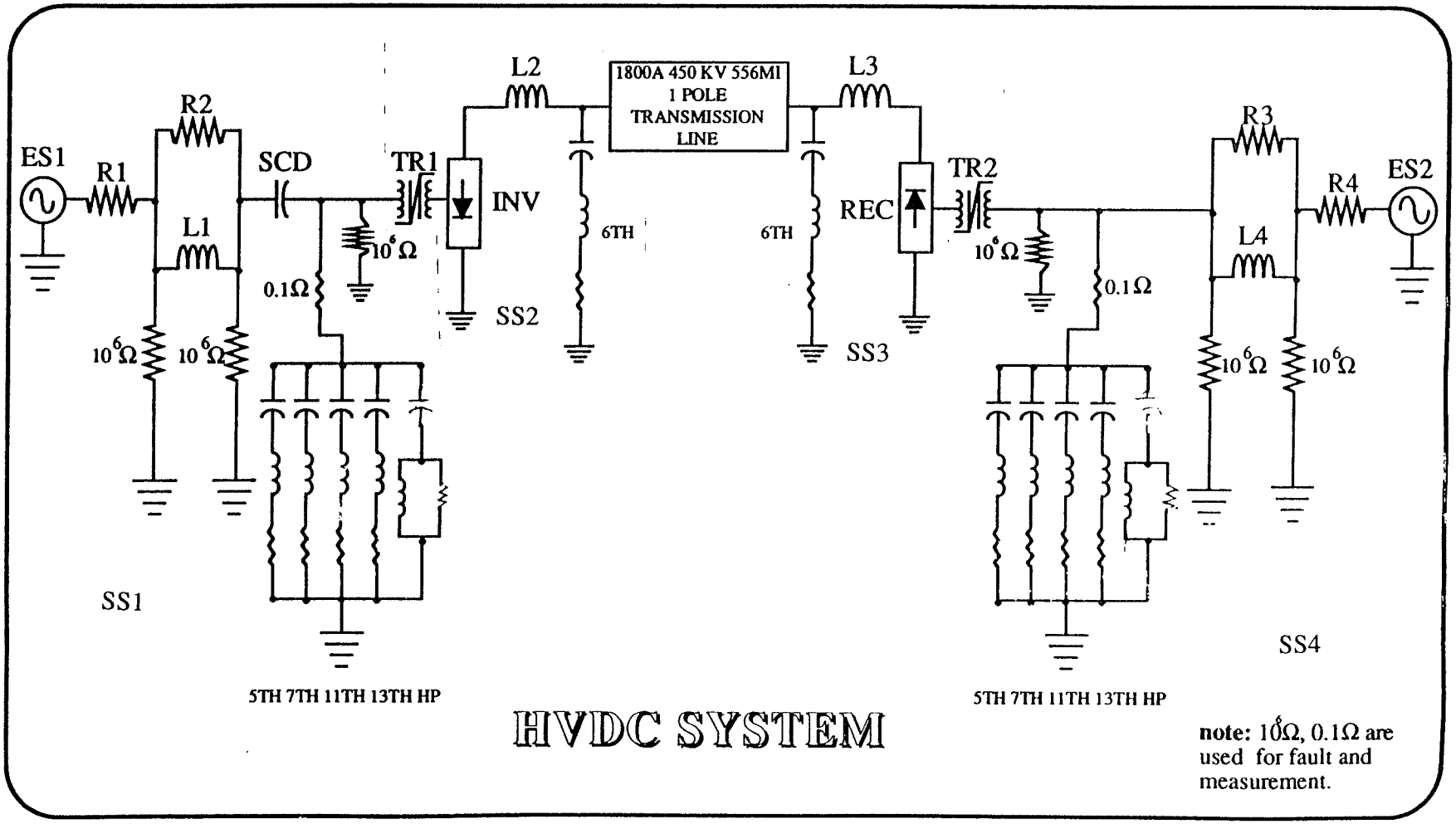


Fig. 2.8 HVDC System

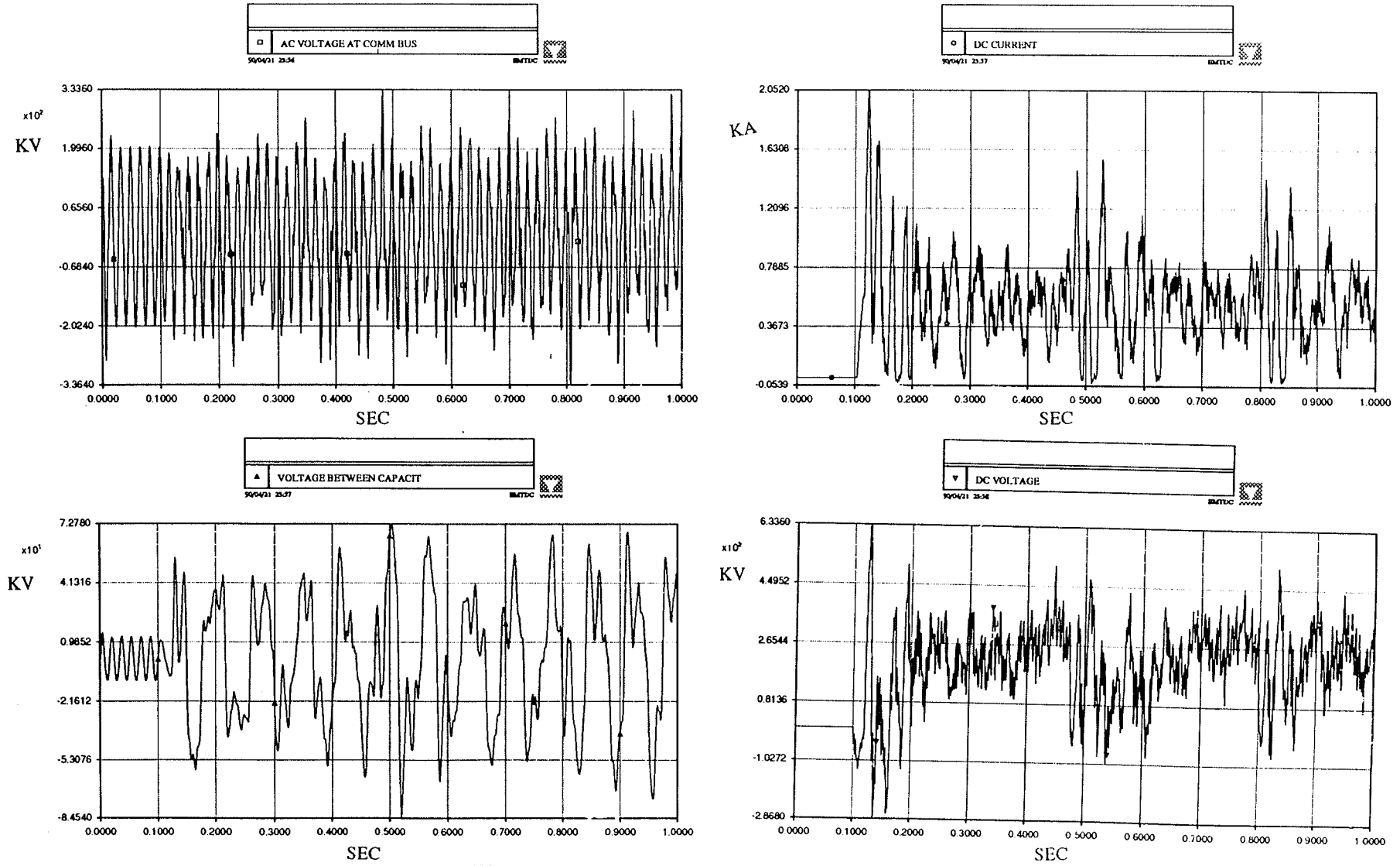
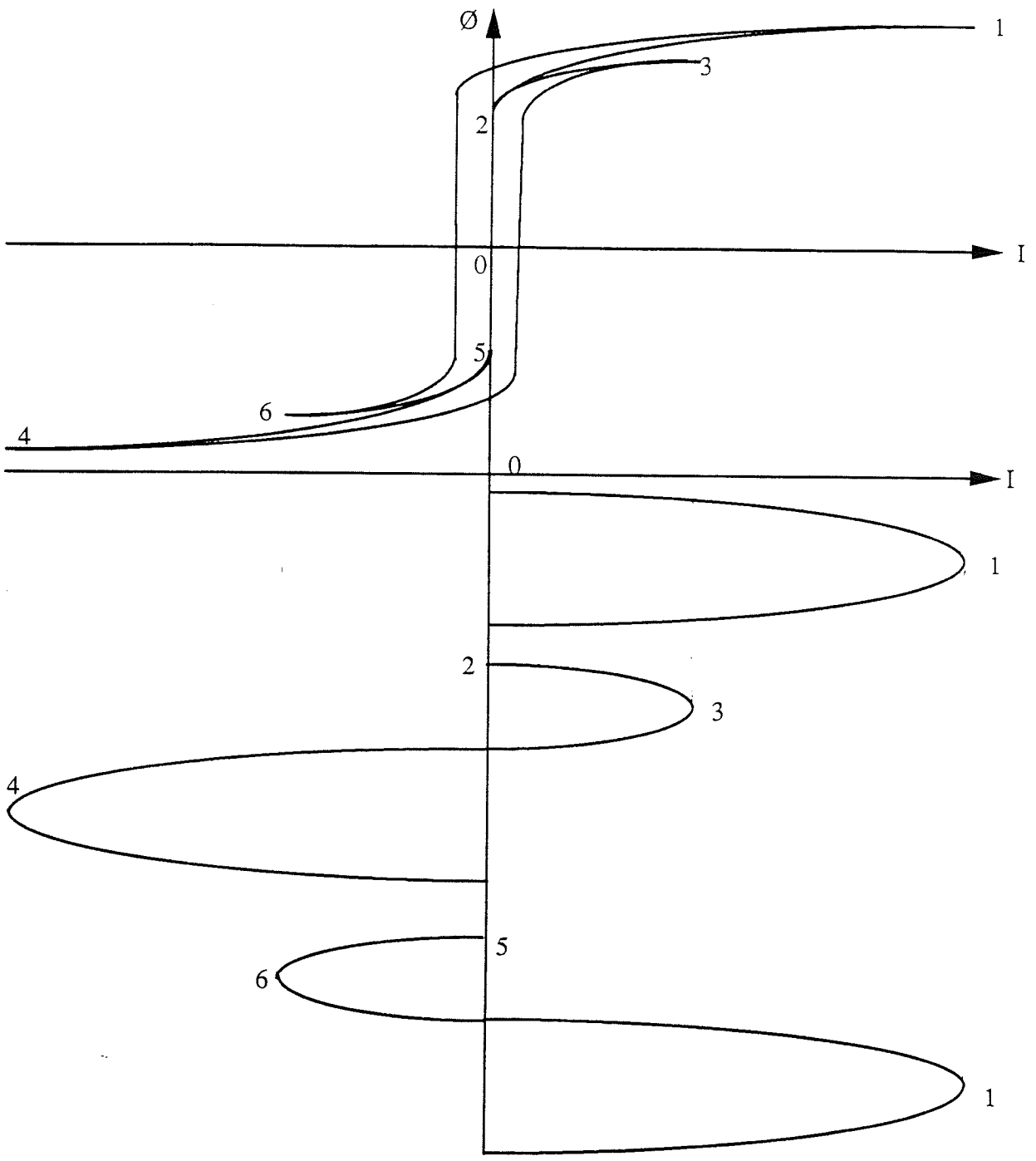


Fig. 2.9 Ferro-resonance In HVDC System Starting Process



Path of the flux changes: 1_____2_____3_____4_____5_____6_____1

60 HZ 60 HZ 60 HZ

20 HZ

Fig. 2.10 The Process Of Ferro-resonance

Chapter 3

INVESTIGATION WITH SINGLE-PHASE TEST SYSTEM (NO HVDC REPRESENTATION)

The previous analysis (system is in Fig. 2.3) shows that the AC system fault recovery initiates the ferro-resonance. In order to investigate this phenomenon further, different system structures and different system parameters are studied in this chapter. Also, several mitigative methods are presented and compared later.

3.1 TESTS WITH VARIOUS SYSTEM HARMONIC IMPEDANCES

The behaviour and performance of a DC system depends heavily on the AC system at each end. The strength of these systems, the amount of damping, the filtering and the impedance characteristics all can have a great impact. Now, we want to look at how the impedance characteristics affect the ferro-resonance phenomenon.

For many DC applications, the combined generation or load in the AC system can be represented by a voltage source behind an R, L and C impedance. The order of this equivalent is chosen as a second order. The higher frequency characteristic are generally dependant on the filtering used.

The R, L and C parameters can be determined if the system MVA, the voltage rating, and the damping angle at two frequencies are known. The magnitude and phase of E are selected to match load flow information.

Five kinds of systems are considered below:

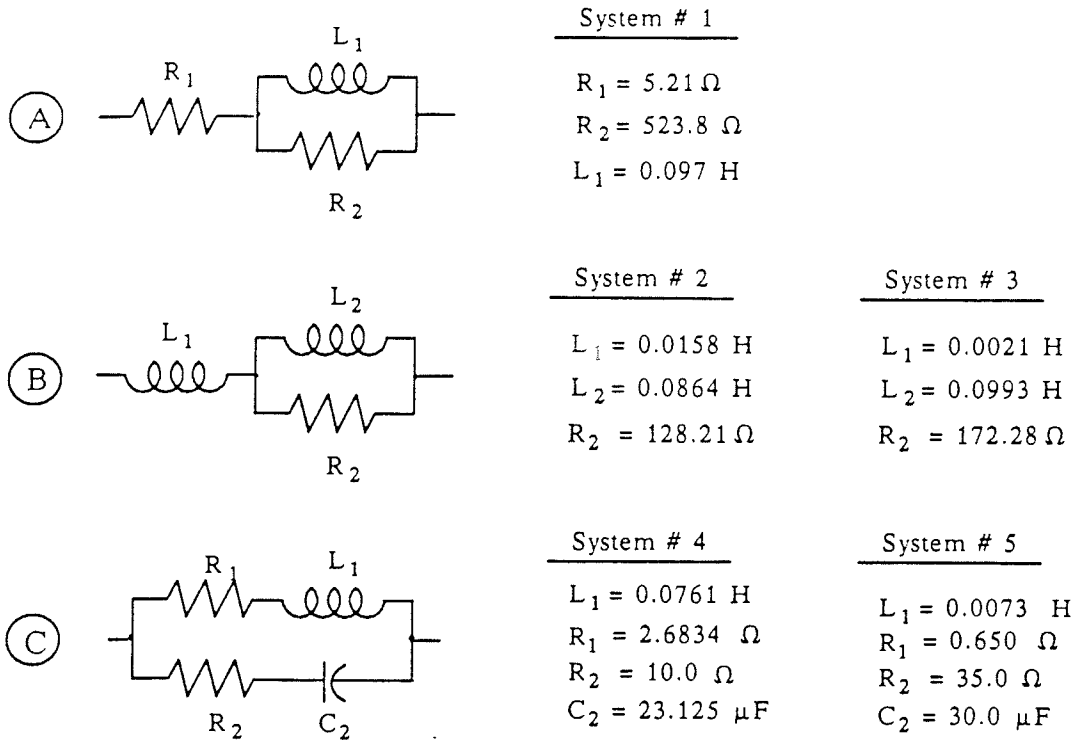


Fig. 3.1 Five kinds of systems to be studied

In order to measure the equivalent impedance vs harmonic for the five kinds of systems, three methods can be used:

3.1.1 Using EMTDC-UNIPLOT To Measure The Equivalent Impedance Vs Harmonic

The circuit used for this purpose is designed in Fig. 3.2.

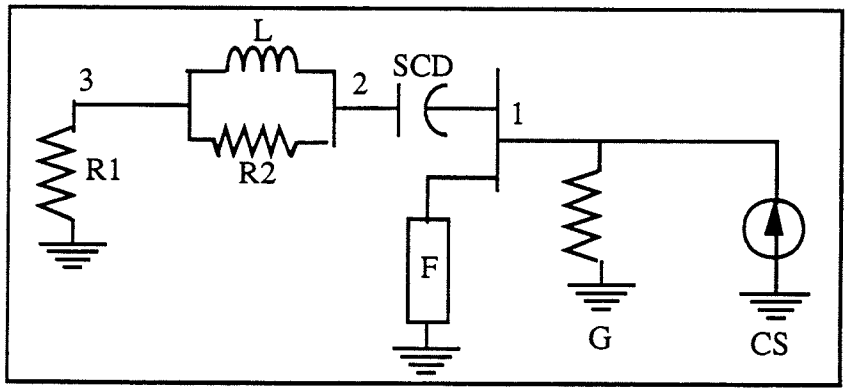


Fig. 3.2 Circuit used for measuring the system harmonic impedance

In the computer simulation program, the Norton source CS defined with a conductance G of 10^{-6} Ω. The Norton source is simulated by EMTDC Harmonic Spectrum Generator Function SGEN11.

Note that in order to keep the accuracy, we define the highest frequency period to include at least 10 print steps.

i.e., if the harmonic number is 200, the fundamental frequency is 5.0 HZ,then the highest frequency is 1000.0 HZ.

Then with the highest frequency period 0.001 second, the print step is taken as 0.0001 second.

To calculate the ratio:

$$Z_{equ}=\frac{V_1}{CS} \quad \text{.....(3.1)}$$

Then we get the equivalent impedance vs harmonic.

3.1.2 Using Fourier Analysis Program EMTFS To Determine The Harmonic Impedance

The EMTFS program can undertake Fourier analysis of any two columns in the one EMTDC output file such that if one column is designated an input and the other an output, the frequency response of output/input can be determined. This can enable transfer functions and impedances to be evaluated as a function of frequency.

Now, we designate the input as the Norton current source CS, the output is the node voltage V1. In EMTFS, with composite frequency analysis, Fourier analyse the input first (i.e., the Norton current source CS), then repeat with the output (i.e., the node voltage V1). Then look at the gain:

$$\therefore \text{Impedance}=\frac{\text{Output}}{\text{Input}}=\frac{\text{Voltage V1}}{\text{Current CS}}$$

$$\therefore \text{Harmonic Impedance}=\frac{\text{Harmonic Voltage}}{\text{Harmonic Current}} \quad \text{.....(3.2)}$$

From (3.2), we can obtain an output file suitable for plotting with UNIPLOT which is a computer plotting program. The output file will include the harmonic number, the frequency, the magnitude, and the angle.

3.1.3 Using Electric Circuit Formulas To Calculate The Equivalent Impedance Directly.

This method is to use the basic electric circuit formula to calculate the harmonic impedance directly.

The short circuit ratio SCR of an AC system is used as a measure of the relative strength of the AC system to the connected converter capacity. Low SCR implies higher sensitivity of the AC voltage loads. So a calculation of SCR for every system is very useful for the analysis of the dynamic characteristic of each system. Even though the strength of an AC system (fault level) is a well defined parameter, there is often confusion whether the effect of reactive sources (such as filters) connected at the converter bus have been taken into account or not. For the purpose of this research, SCR is defined taking into account the reactive power supplied by the AC filters.

The short circuit ratio SCR corresponding to each system is defined below:

$$SCR=\frac{S_{ac}-Q_f}{P_d}$$

$$=\frac{V_c^2}{P_d}\left(\frac{1}{|Z_s|}\frac{1}{|Z_f|}\right) \quad \text{.....(3.3)}$$

Where: Sac = short circuit capacity of AC system
Pd = rated HVDC power
Qf = reactive power supplied by AC filters
Vc = rated AC voltage
Zs = the impedance of AC equivalent system
Zf = the impedance of AC filters

According to formula (11), the SCR of the system #1 is:

$$SCR_1=\frac{230.0^2}{810}\left(\frac{1}{37.39}-\frac{1}{263.44}\right)=1.5 \quad \text{.....(3.4)}$$

The SCR of the system #2 is:

$$SCR_2=\frac{230.0^2}{810}\left(\frac{1}{37.37}-\frac{1}{263.44}\right)=1.5 \quad \text{.....(3.5)}$$

The SCR of the system #3 is:

$$SCR_3=\frac{230.0^2}{810}\left(\frac{1}{37.36}-\frac{1}{263.44}\right)=1.5 \quad \text{.....(3.6)}$$

The SCR of the system #4 is:

$$SCR_4=\frac{230.0^2}{810}\left(\frac{1}{38.16}-\frac{1}{263.44}\right)=1.46 \quad \text{.....(3.7)}$$

The SCR of the system #5 is

$$SCR_5=\frac{230.0^2}{810}\left(\frac{1}{2.90}-\frac{1}{263.44}\right)=22.27 \quad \text{.....(3.8)}$$

The comparison of these impedances in five different systems is shown in Fig. 3.3.

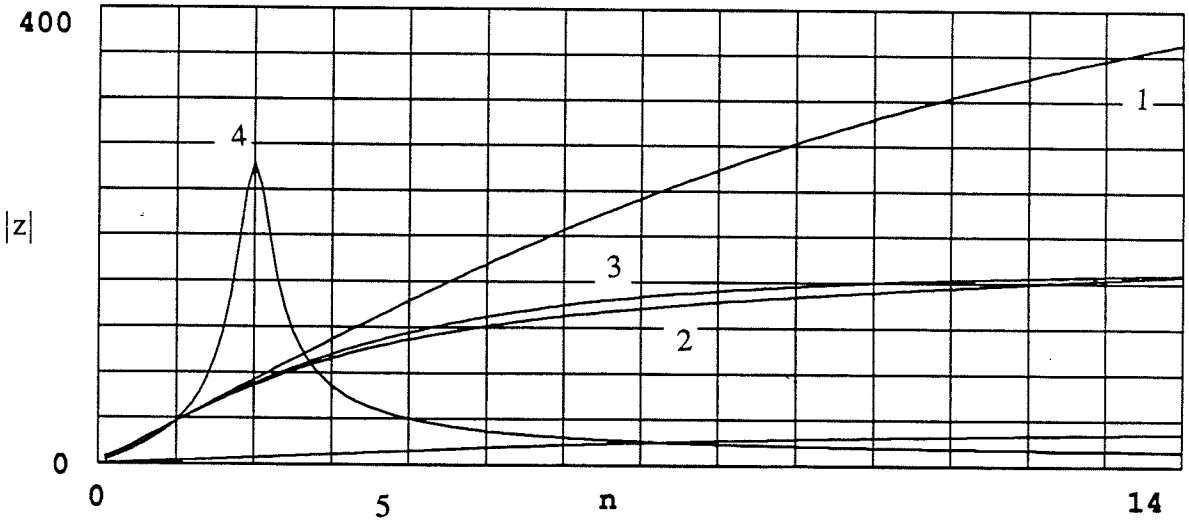


Fig. 3.3 The comparison of the impedances in five different systems

From the previous calculation, it can be seen that the systems #1--#3 give the same SCR = 1.5, the system #4 gives the SCR = 1.46. They are all the weak AC system. The system #5 gives the SCR = 22.27, it is a strong AC system.

The following impedance-harmonic curves in figures 3.4 and 3.5 give the characteristics of the harmonic impedance in the AC system as seen from the converter transformer through the series capacitor. In these figures, (a) gives the calculation process; (b) gives the impedance-harmonic curve, where $Z_{tot1}(n \cdot 60)$ means that the filter group includes the 5th, the 7th, the 11th, the 13th, and the high pass filters, $Z_{tot2}(n \cdot 60)$ means that the filter group includes the 2nd, the 5th, the 7th, the 11th, the 13th, and the high pass filters. From these curves, the filter tuned-points can be seen clearly.

Fig. 3.4, the system #1 harmonic impedance (while the system #2, #3 and #4 are similar with the system #1, so the graphs are omitted).

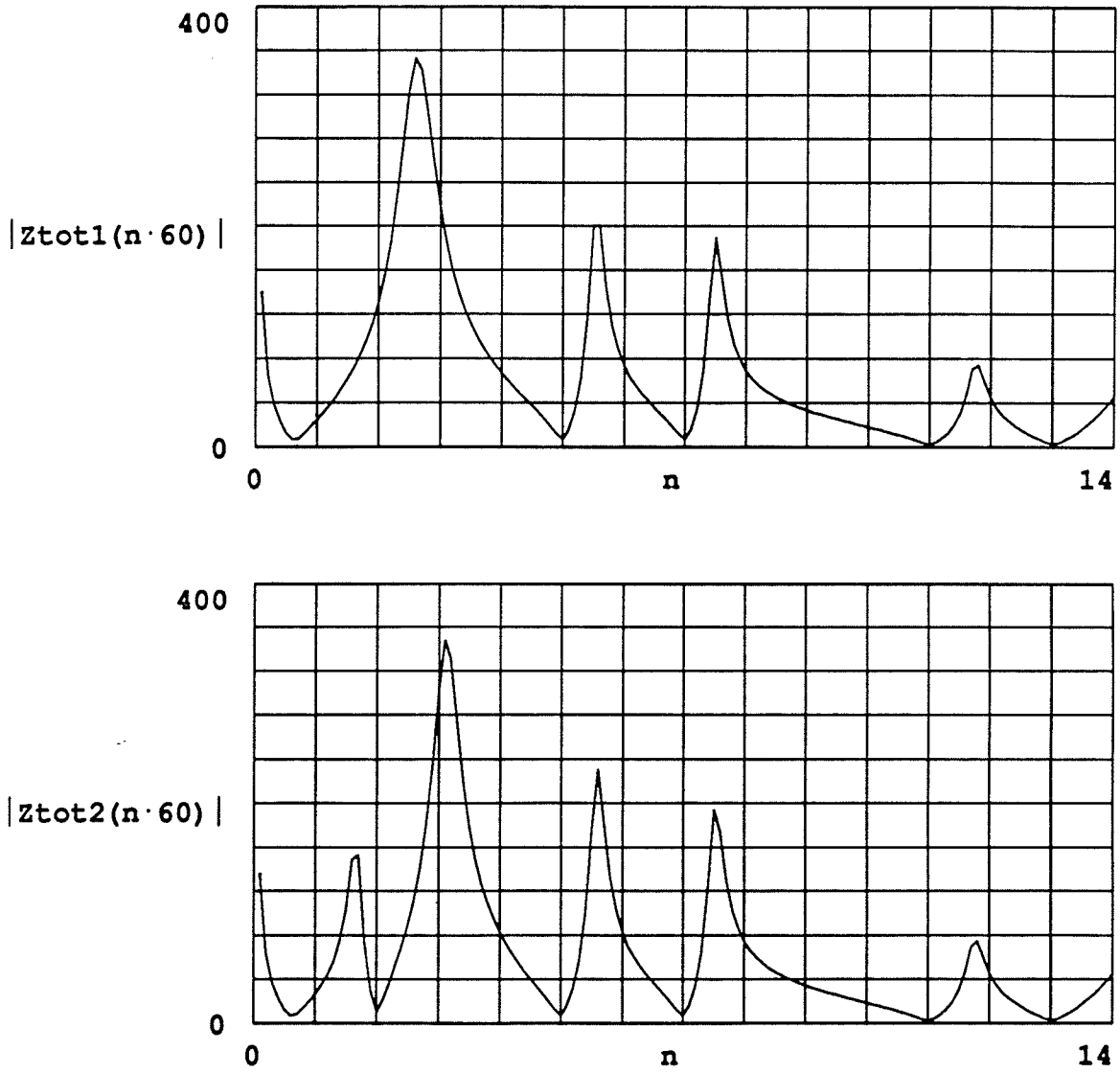


Fig. 3.4 The Harmonic Impedance In System #1

Fig. 3.5 is the system #5 harmonic impedance:

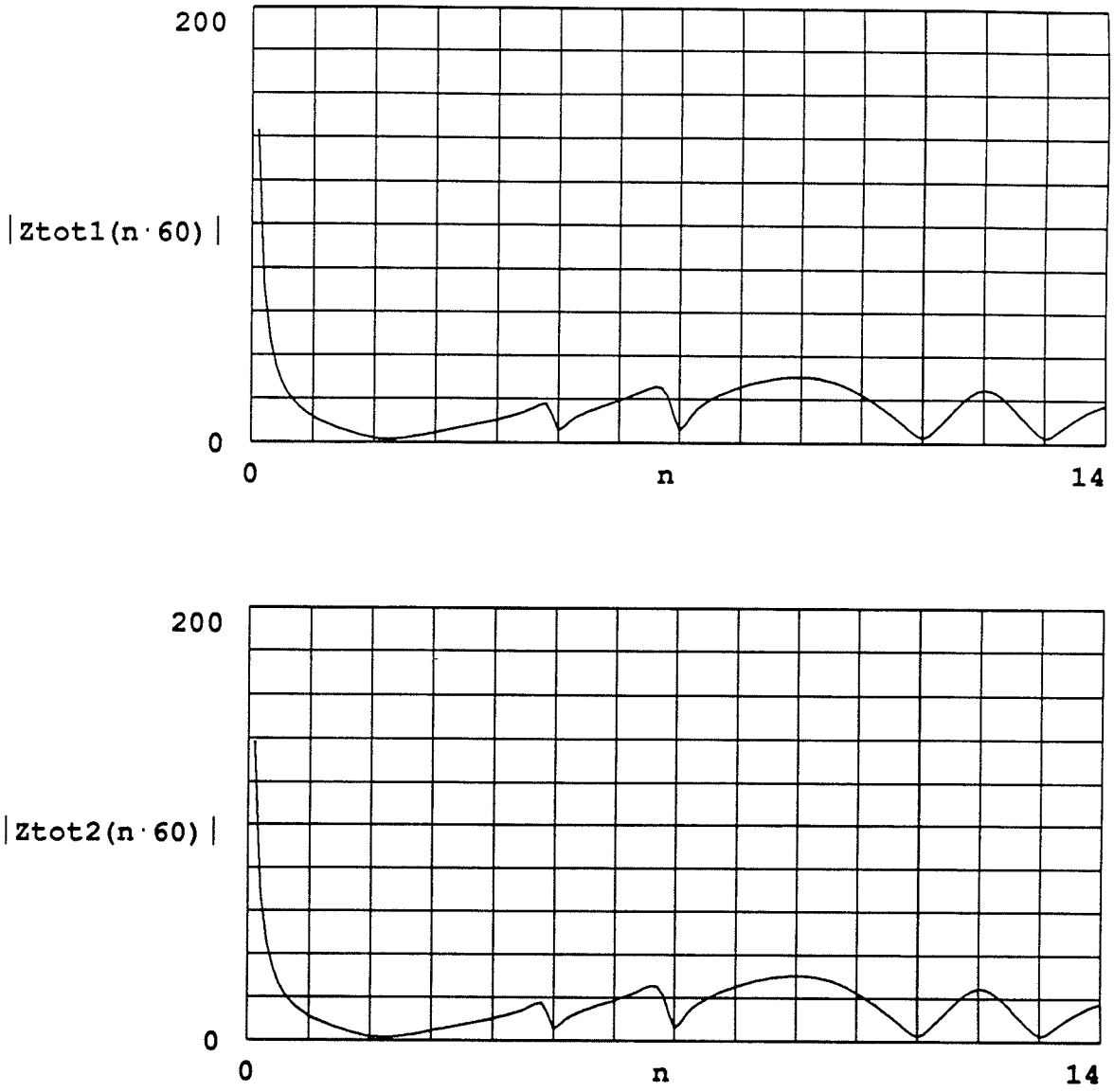


Fig. 3.5 The Harmonic Impedance In System #5

In the system #1--#4, there is a high impedance appearing between the 2nd and the 3rd harmonic. Particularly, the system #1 shows the highest impedance between the 2nd and the 3rd harmonic. The system #5 has a very high short circuit capacity.

Harmonic current, coincident with the resonant frequency, can generate a large harmonic voltage component due to the parallel resonance impedance. Severe harmonic distortion of the fundamental frequency voltage waveforms can result.

So ferro-resonance can be produced in the system #1--#4. Because of the lower 2nd and 3rd harmonic impedance, ferro-resonance never occurs in the system #5. It is obvious that the AC system with the highest harmonic damping will give the best result. But unfortunately, we can't expect to get the system #5 all the time.

Using 2nd harmonic filter can lower the impedance between the 2nd and the 3rd harmonic. This will give some help in the fault recovery process.

Single phase tests corresponding to five different system harmonic impedances have been taken. Fig. 3.6 shows the test of system #1, while tests of system #2, #3 and #4 are similar with Fig. 3.6. So graphs for these systems are omitted. Fig. 3.7 shows the test of system #5.

For each specified system condition, the following variables are recorded:

(1) Instantaneous node 1 voltage in P.U.

(2) Instantaneous node 2 voltage in P.U.

(3) Instantaneous node 3 voltage in P.U.

(4) SCD voltage instantaneous value in KV

(5) AC current in KA

Because there are no mitigative measures in each system after fault clearance, ferro-resonance persists in systems #1 -- #4. Because of the lower harmonic impedance in system #5, there is a good recovery waveform.

From the observations of the severe distortion of the voltage waveforms in the system #1--#4, the following analysis can be given: fundamental-frequency overvoltages are caused either by too small load current or by the fundamental component of the inrush current; harmonic overvoltages are created by injection of the harmonic currents into the AC system; subharmonic overvoltages are due to slowly changing voltage at the capacitor.

In order to observe the effect of different system components on the transformer terminal voltage waveform, the following elements are varied within the given ranges (system #1 is chosen to be studied):

(1) Transformer air core reactance Xs=0.15, 0.4, 0.65 P.U.

(2) Transformer current at rated flux Im= 1, 5, 10, 15%

(3) SCD value varied SCD = 176 μF, 100 μF, 50 μF

For each case, the observation variables are the same as on the previous page.

General observation is the ferro-resonance persists in every fault recovery process.

From tests in (1), it can be seen that the effect of the transformer air core reactance Xs is: with the smaller Xs, the transformer saturation is deeper, so the ferro-resonance is much worse.

From tests in (2), it can be seen that the effect of the transformer current at rated flux Im is: with the larger Im, the ferro-resonance becomes much worse.

From tests in (3), it can be seen that the effect of the SCD value is: with the SCD value larger, the ferro-resonance is much worse.

So the worst case occurs at Xs = 0.15, Im = 15%, SCD = 176.0 μF.

Based on the above observations, it is clear that the AC system harmonic impedance decides the fault recovery performance. The transformer air core reactance Xs, the transformer current at rated flux Im and the SCD value are also affect the shape of the system voltage during ferro-resonance. The ferro-resonance effect, associated with fault clearing near an unloaded transformer, is initiated by remanent flux on the transformer and the residual voltage on the series capacitor left by the fault current.

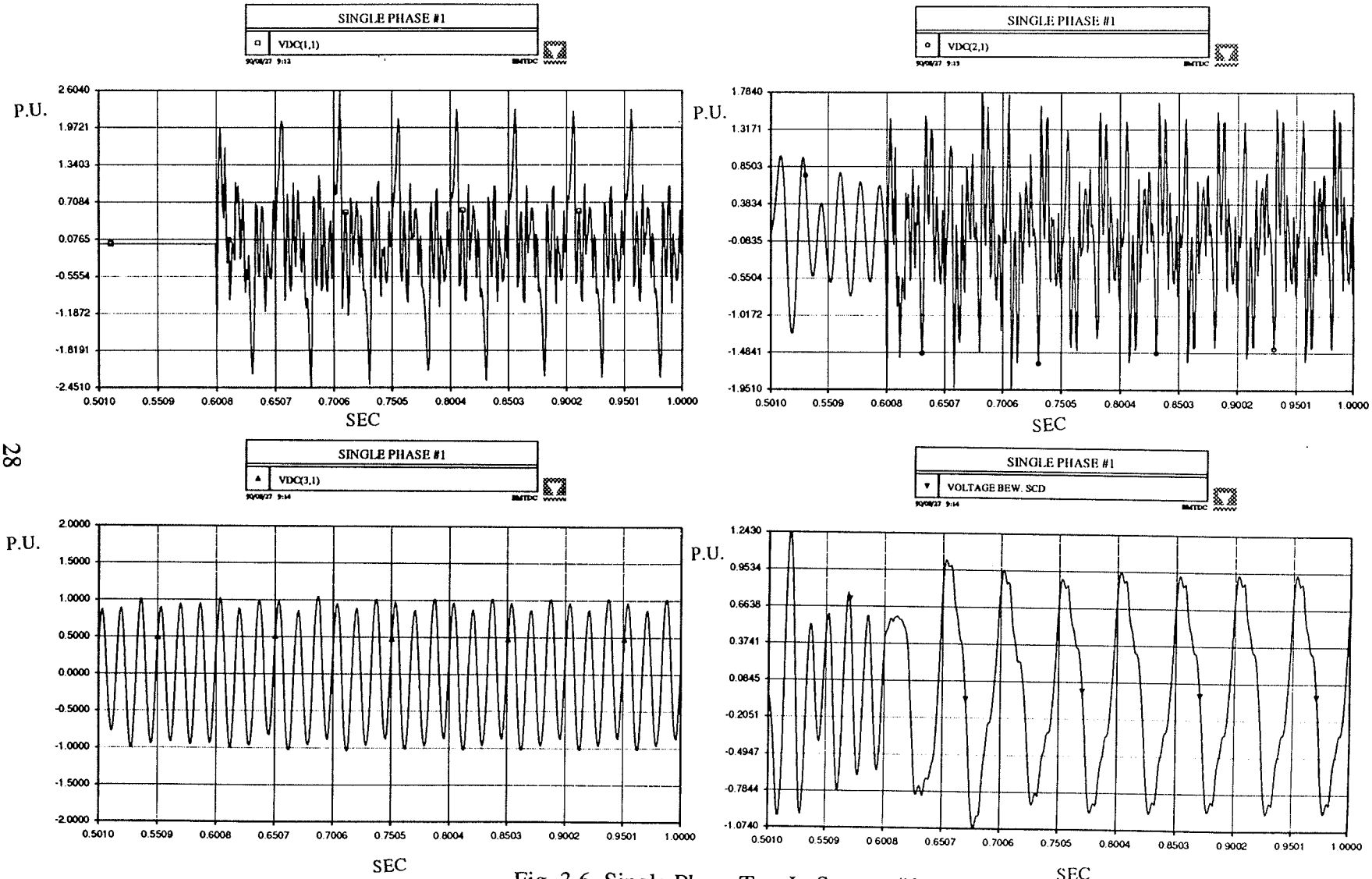


Fig. 3.6 Single Phase Test In System #1

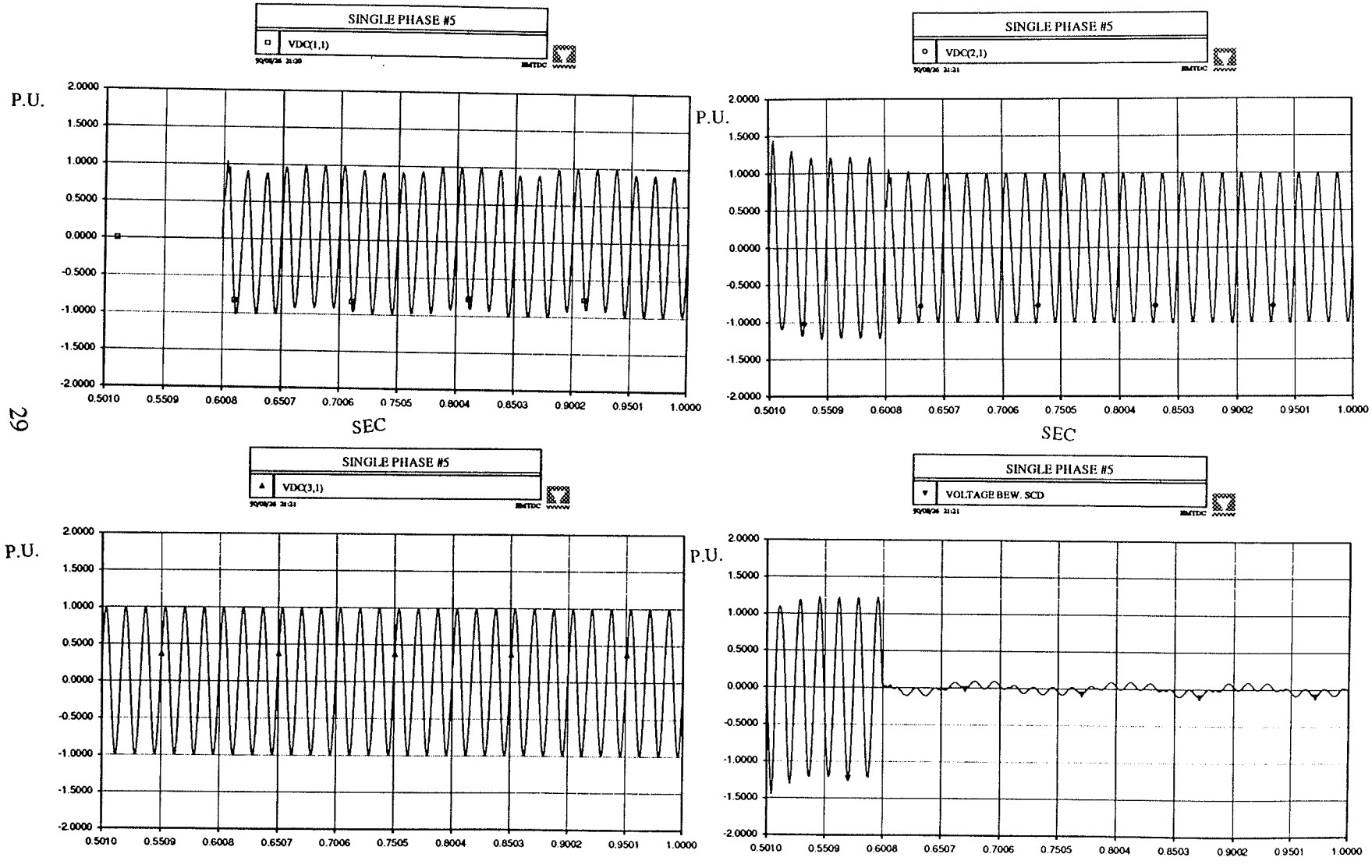


Fig. 3.7 Single Phase Test In System #5

3.2 TEST SYSTEM

The diagram of test system has been shown in Fig. 2.3.

The tests were made for the following data:

Table 3.1 AC System Data

DATA	TR	BASE
R1 = 5.21 Ω R2 = 523.81 Ω L1 = 0.097 H SCD = 176.00 μF	MVA = 320 MVA Xl = 20% Xs = 40%	Vb = 188 KV peak Pb = 269 MW Ib = 2026 A

Table 3.2 AC Filter Data

Types / Elements	5 TH	7 TH	11 TH	13 TH	HP
R (Ω)	7.11	7.11	2.66	2.66	47.4
L (H)	0.1493	0.1493	0.0393	0.0393	0.0036
C (μF)	1.885	0.9618	1.479	1.056	4.559
MVAR (Total 200)	39.20	19.60	29.70	21.20	90.30

The transformer connected in the system is modeled with saturation effects as shown in Fig. 3.8. The saturation is taken into account by adding an additional flux dependent saturation current to the current computed by the linear part of the model. The V-I characteristic of the transformer is modelled with a knee-point voltage of 1.20 P.U. and air core reactance of twice the leakage reactance.

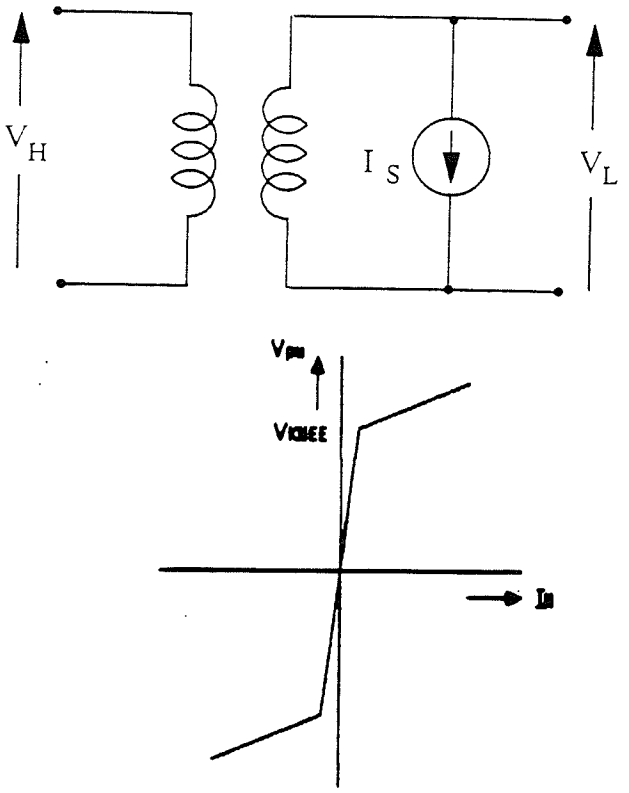


Fig. 3.8 Transformer Model

3.3 MITIGATIVE METHODS

3.3.1 Subharmonic Filter

Since the ferro-resonance waveform contains a lot of 20 HZ harmonic, so a 20 HZ filter is designed in several positions:

(1) The series capacitor and the insert inductance compose the parallel subharmonic filter, tuned at 20 HZ.

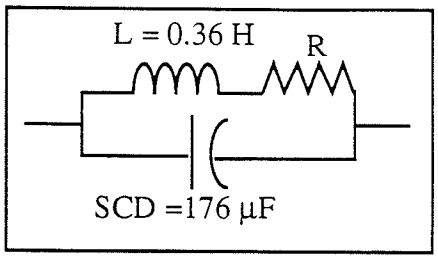


Fig. 3.9 Parallel 20 HZ Filter

(2) The series subharmonic filter, tuned at 20 HZ.

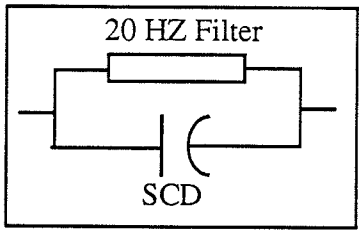


Fig. 3.10 Series 20 HZ Filter

(3) The shunt subharmonic filter, tuned at 20 HZ.

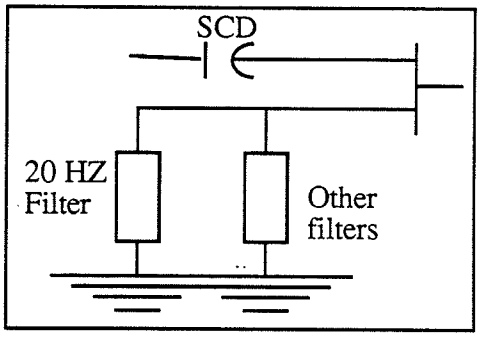


Fig. 3.11 Shunt 20 HZ Filter

Simulation results show either one of the three kinds of subharmonic filter can successfully eliminate the ferro-resonance in fault recovery process (Fig. 3.16)

3.3.2 SCD With MOV Protection Bypass

The arrester is modelled in EMTDC package as a non-linear resistor: a resistive branch

and a voltage source. The resistance of the MOV is changed in a piece-wise linear fashion to represent the slope of the arrester characteristic[1].

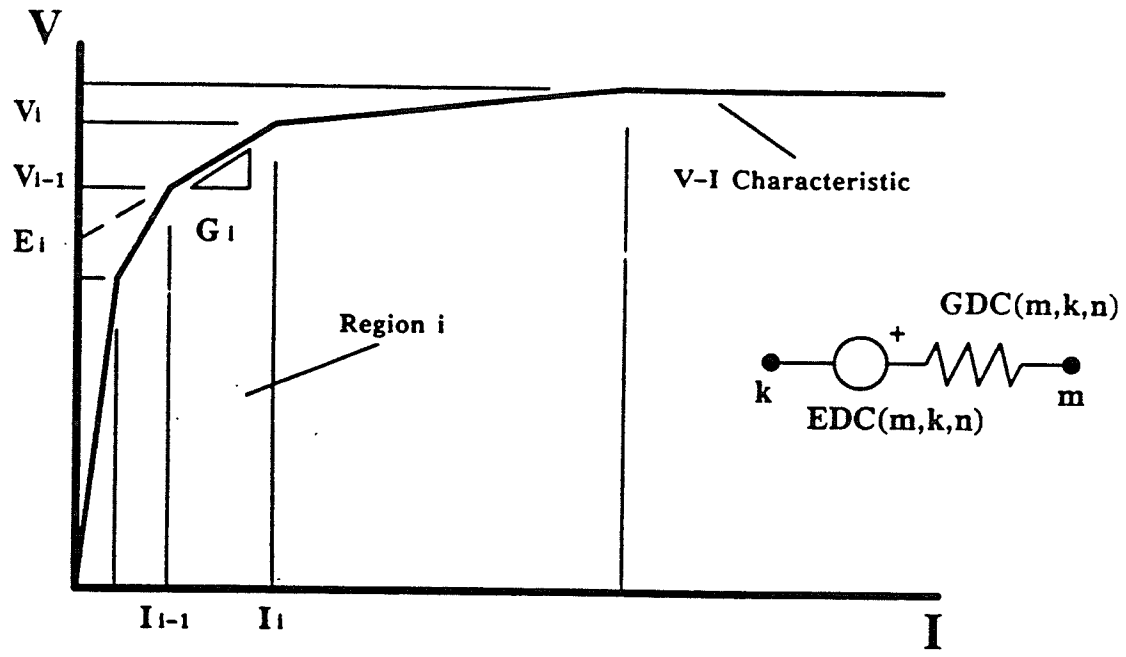


Fig. 3.12 The Characteristic Of An MOV

Energy in the surge arrester is limited by the temperature the ZnO material reaches. For each stack or column of ZnO discs, there is a limit of 3 to 13 Kilojoule/KV(energy absorbed by the arrester in kilojoule assuming that volts across the arrester is in KV) which the arrester can absorb in energy.

For example, consider an arrester rated at 12 KV (VSCL = 12.0, where VSCL is the argument in EMTDC surge arrester subroutine ZNO to define arrester voltage rating.). If WSES = 4.0, where WSES is the output argument in surge arrester subroutine ZNO defining energy accumulated in the arrester, then energy is 4/12 = 0.3333 (KJ/KV).

If WSES = 200.0 and VSCL = 12.0 KV, then arrester energy = 200/12 = 16.6667 (KJ/KV).

Several cases are simulated in Fig. 3.17 (The AC bus voltage is recorded).

When the load current is small, the voltage on the SCD is small and may not exceed the arrester rated volts. The MOV doesn't operate and looks like an open circuit. At the high

load current, the voltage on the SCD may exceed the MOV rated level when the MOV operates, the voltage on the SCD is limited to its protective level. Tests show that the MOV can help the system recovery from faults.

3.3.3 C-type Filter[5]

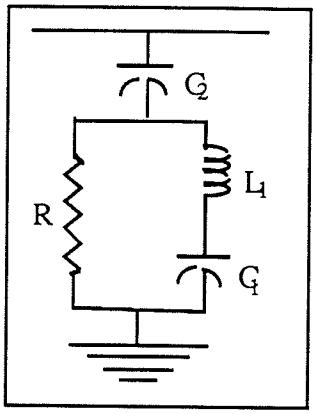


Fig. 3.13 C-type filter

The series inductance-capacitance L_1 and C_1 are tuned at the system fundamental frequency F_0, so that

$$F_0=\frac{1}{2\pi\sqrt{L_1C_1}}\ (HZ) \qquad .....(3.9)$$

L_1, C_1 and C_2 are tuned at a specific harmonic (such as 120 HZ), then

$$F_n=\frac{1}{2\pi\sqrt{L_1\frac{C_1C_2}{C_1+C_2}}}\ (HZ) \qquad .....(3.10)$$

Assume C_2 = 4.559 μF,

$$C_1=C_2[(\frac{F_n}{F_0})^2-1]$$

$$=4.559*(2^2-1)=13.667\ (\mu F) \qquad .....(3.11)$$

$$L_1=\frac{1}{(2\pi F_0)^2 C_1}$$

$$=\frac{1}{(2\pi*60.0)^2*13.667*10^{-6}}$$

$$=0.5145\ (H) \qquad .....(3.12)$$

Select Q = 3:

$$R=\frac{2\pi F_n L_1}{Q}$$

$$=\frac{2\pi*120.0*0.5145}{3}$$

$$=129.2965\ (\Omega) \qquad .....(3.13)$$

The characteristic of C-type filter is:

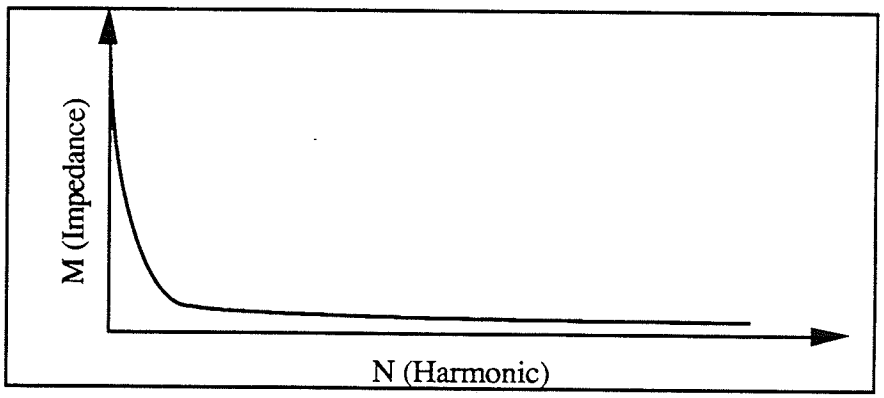


Fig. 3.14 The characteristic Of C-type Filter

It looks like a high pass (H-P) filter. But if a H-P filter is tuned at 120 HZ, it has large losses. Using a C-type filter can successfully overcome this shortcoming.

Digital simulation shows the C-type filter can successfully eliminate the ferro-resonance.

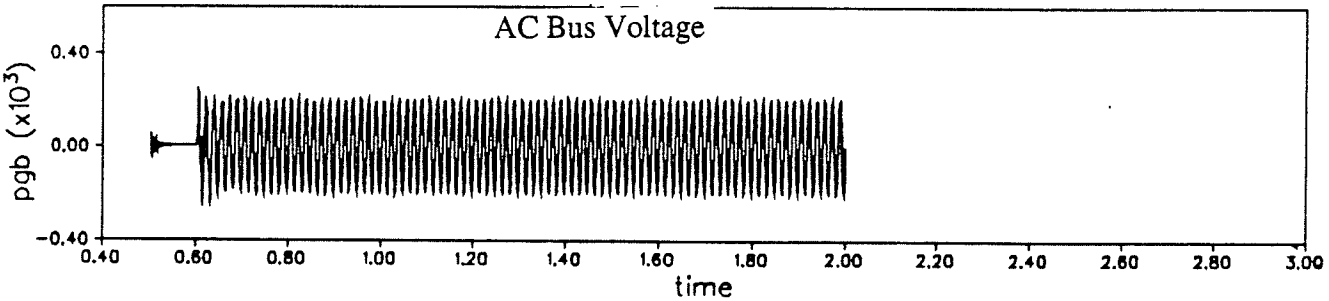


Fig. 3.15 The test with C-type filter

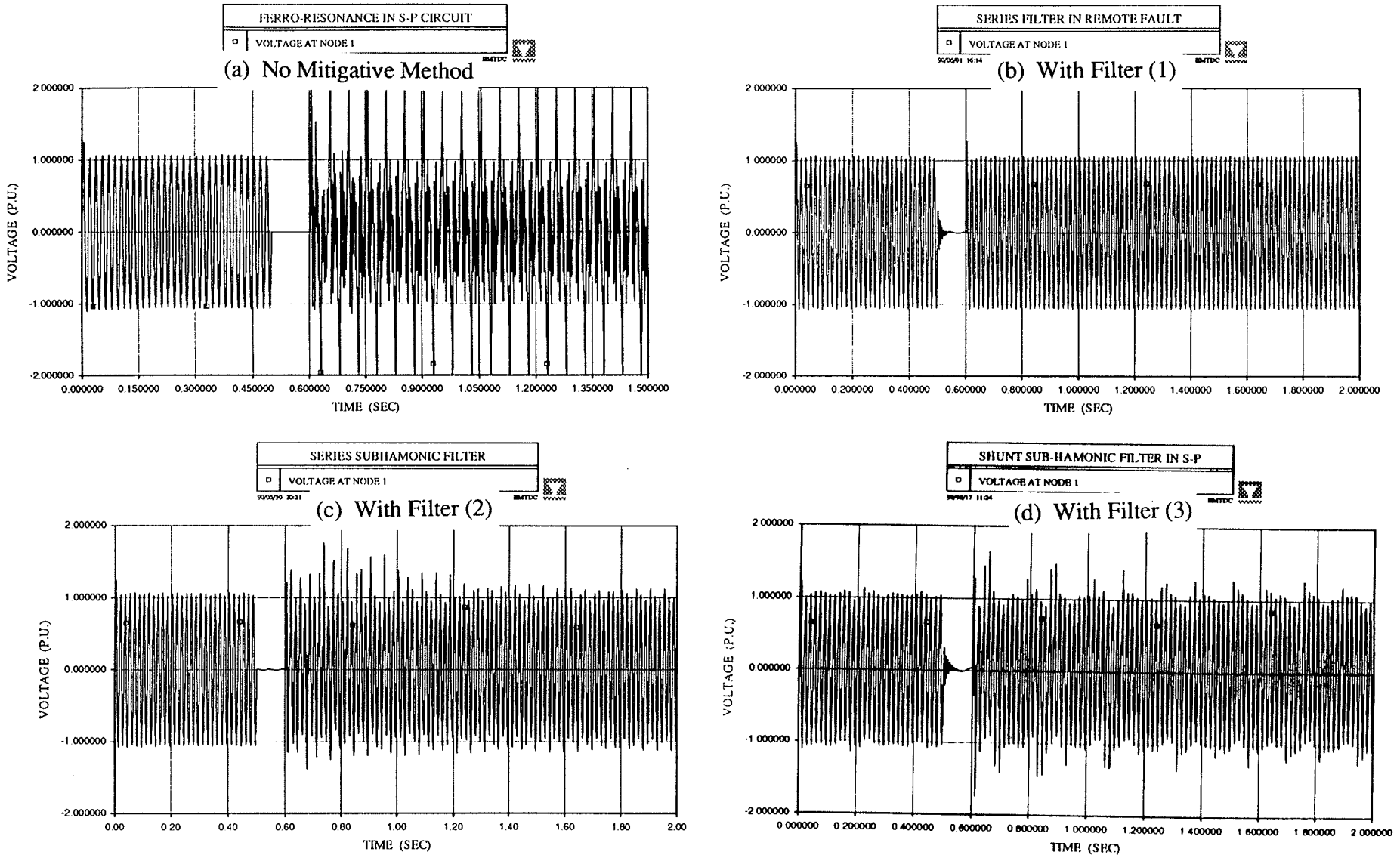


Fig. 3.16 Some Tests (AC Bus Volts)

A comparison is given in Fig. 3.17. Without the mitigative method, the AC voltage cannot recover from the SLGF (see Fig. 3.17(a)). With the MOV protection bypass method, choosing different rated voltages, such as VSCL=20.0 KV (Fig. 3.17(b)), VSCL=40.0 KV (Fig. 3.17(c)), VSCL=80.0 KV (Fig. 3.17(d)), the AC voltage can successfully recover from the SLGF.

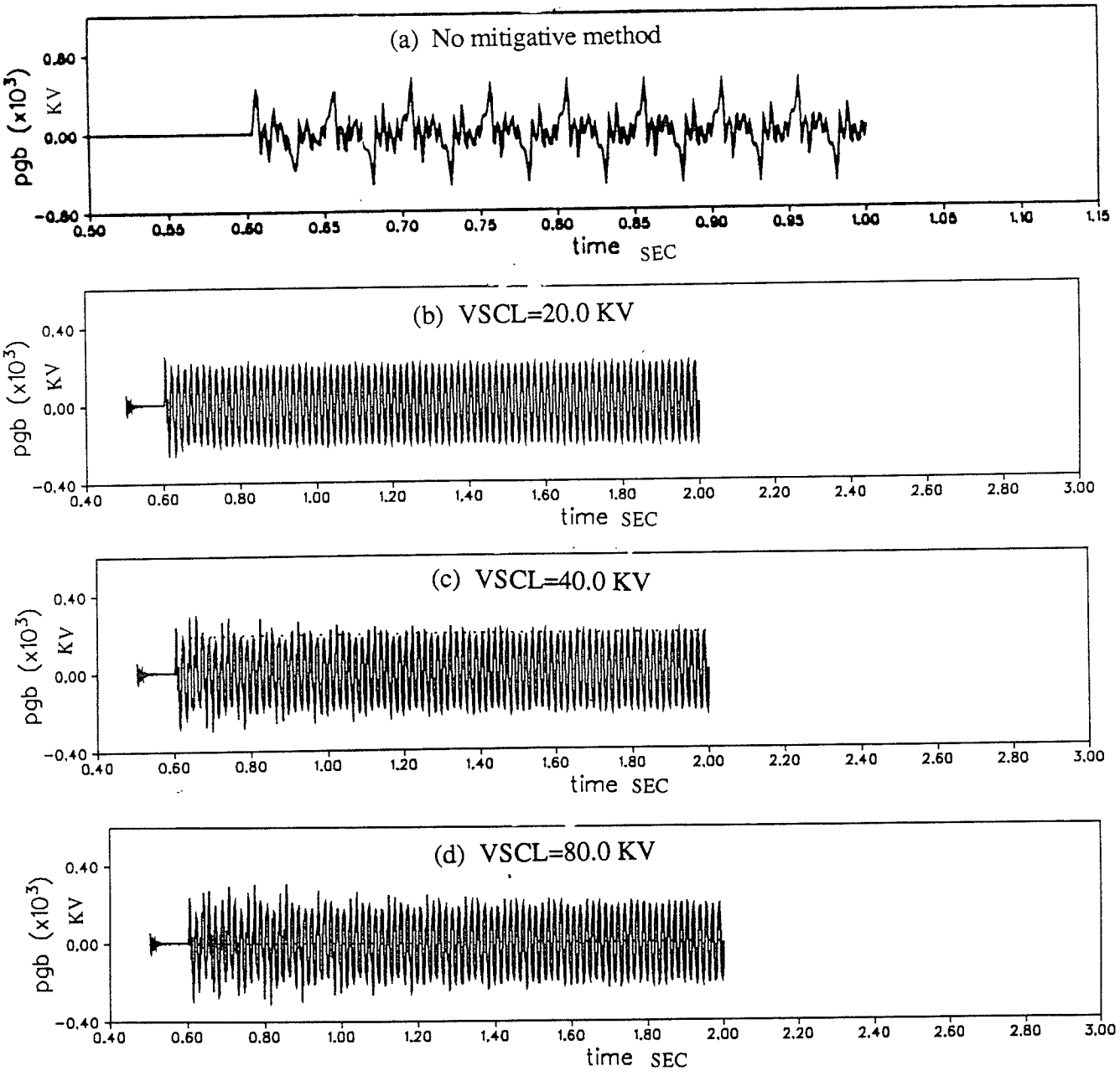


Fig. 3.17 A Comparison Of AC Bus Voltage

3.3.4 R + SWITCH

The diagram is shown in Fig. 3.18.

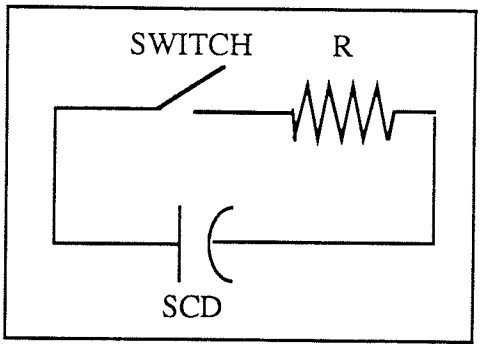


Fig. 3.18 The diagram of R + SWITCH

Switch is closed immediately after fault clearance. After 300 ms, it is opened. Because the dissipation resistor can absorb the ferro-resonance energy, so the system can easily recover from faults.

In EMTDC program, the switch is simulated by subroutine SWTCH5. The capacity of the switch depends on the value of resistor. So in an economic view, the larger R the better. However, simulations show that the system has a better recovery waveform with a smaller R. Summarizing these two aspects, R = 100.0 Ω is selected.

In system steady state, all the node voltages are approximately 1.0 P.U. Due to normal magnetization current in the transformer, AC current fluctuates a small amount. This causes the fluctuation in the SCD voltage. Because the switch is off in the system steady state, therefore no energy accumulates in the damping resistor R.

After fault clearance, the switch is closed. Fault current flows through R. The dissipation resistor R can absorb the ferro-resonance energy. So after 300 ms, when the switch opens again, the system can successfully recovery from the fault (Fig. 3.25). This is a good method to eliminate the ferro-resonance phenomenon.

3.3.5 Thyristor Controlled Resistor (Thyristor Is Simulated By EMTDC Subroutine THYR4)

The diagram is shown in Fig. 3.19.

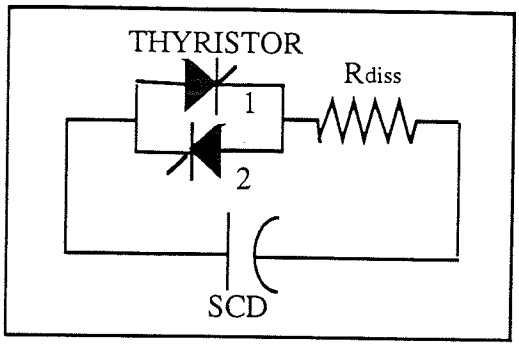


Fig. 3.19 The diagram of thyristor controlled resistor

The thyristor is a special kind of switch. Its on or off state is controlled by the firing angle **a.** If $\mathbf{a = 180^0}$, for the normal AC voltage, the thyristor will be blocked all the time. If $\mathbf{a = 0^0}$, the thyristor will be on or off naturally, like a diode. The following tests correspond to these two cases.

(1) $\mathbf{a = 180^0}$

When the SCD voltage has no distortion, both thyristors will be blocked all the time. Only when the SCD voltage has a distortion, thyristors can be switched on and R_{diss} will be inserted to remove subsynchronous energy from the series capacitor and magnetic circuit. (see Fig. 3.27 -- Fig. 3.28).

Fig. 3.27 shows the fault recovery process with R_{diss} = 1.0 Ω. Fig. 3.28 shows the fault recovery process with R_{diss} = 100.0 Ω. Again, it can be seen that Fig. 3.27 has a better recovery waveform than Fig. 3.28. But in the former case, the thyristors have to prepare to switch off a much larger fault current than the later case. So the choice of the dissipation resistor depends not only on the system fault cases, but also on the capacity of the thyristors.

(2) $\mathbf{a = 0^0}$

After the fault clearance, the thyristors are deblocked, and the thyristor firing pulses are applied at $\mathbf{a = 0^0}$. One thyristor will be always on. So the dissipation resistor will be inserted to remove the ferro-resonance energy. 300 ms later, the thyristors will be blocked. This case is exactly the same as SWITCH + R case (Fig. 3.18).

Naturally, from the thyristor controlled resistor method, we think of the thyristor controlled inductor method (Fig. 3.20). Based on the idea of that the inductor may absorb

the extra reactive power during the system fault recovery period, so it may keep the capacitor from accumulating dc energy.

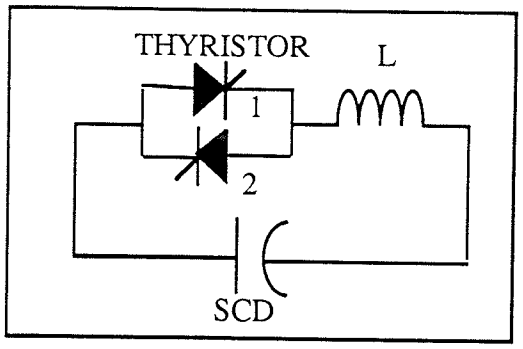


Fig. 3.20 The diagram of thyristor controlled inductor

As expected, the simulation results show an oscillation at Fn $=1/\sqrt{LC}$. To avoid this oscillation, the thyristor deblocked time has to be chosen at the zero-crossing point of the voltage across the SCD. Then the inductor inserted time is controlled by the SCD voltage, not by the requirement of the balance of the AC system reactive power. This will lose our first purpose. Due to this contradiction, this method has to be given up.

3.3.6 Fundamental Blocking Filter

The diagram is shown in Fig. 3.21.

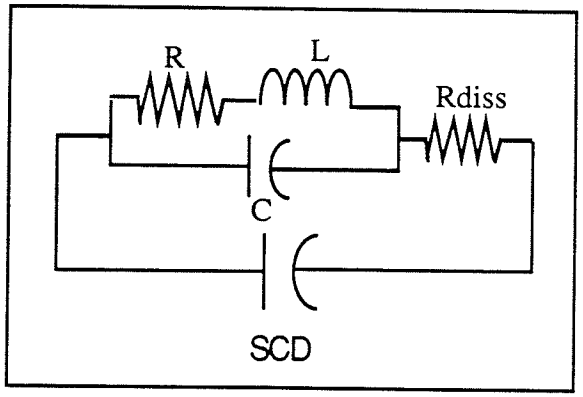


Fig. 3.21 The diagram of fundamental blocking filter

L and C are tuned at fundamental frequency. So at the system steady state, for the fundamental frequency, the fundamental blocking filter branch is opened. For the subsynchronous frequency and the other harmonic frequencies, the filter shows a low

impedance (Fig. 3.22). The filter quality is determined by the resistor R. A very undamped impedance versus frequency characteristic maybe unrealistic. So choosing suitable filter quality Q becomes important (A detailed research is given in Chapter 4 respond to the HVDC system).

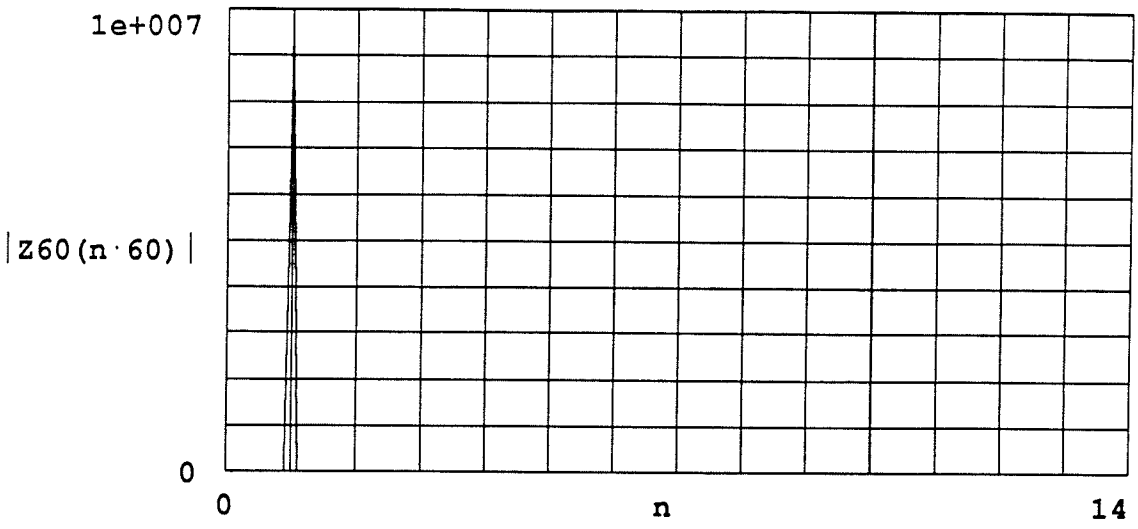


Fig. 3.22 The characteristic of fundamental blocking filter (R=0.1Ω)

As the same as the method (1) and (2), Rdiss (=100.0 Ω) will absorb the subsynchronous energy. In the system steady state, all the node voltages maintain approximately 1.0 P.U. The voltage across the SCD is 10.0 KV. The AC current is 0.8 KA . Because the fundamental blocking filter shows a high impedance for the system fundamental frequency, so the current through the Rdiss and the voltage between the Rdiss are both quite small, around zero. So the voltage across the fundamental blocking filter is the same with the SCD voltage.

When there is a SLGF at node 2 (node 2 is the node between the AC system equivalent impedance and the SCD), the node voltage drops to zero (Fig. 3.26). In the transient state after the fault clearance, there are lots of harmonic currents in the AC current. The fundamental frequency blocking filter exhibits a low impedance for these harmonic currents. Then the current through the Rdiss and the voltage across the Rdiss are increased. After the dissipation resistor Rdiss absorbs the harmonic and the subsynchronous energy, the system recovers to the original steady state. As soon as the system is dominated by the fundamental frequency again, the fundamental frequency blocking filter branch will effectively remove the energy dissipation resistor. This method shows a better performance than the R + SWITCH or the R + THYRISTOR method in both the system steady state and the fault recovery process.

A suppression circuit can successfully eliminate the ferro-resonance in the capacitive voltage transformer (CVT)[33]. The circuit is shown as follows:

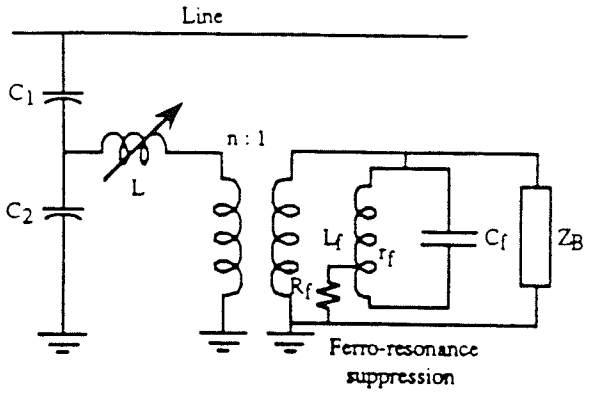


Fig. 3.23 CVT incorporating ferro-resonance suppression

Based on the author's design, the suppression filter capacitance = 8.0 μF; the suppression filter inductance = 230.0 VA; the suppression filter resistor = 40.0 Ω.

Because the values of C, L and R in the ferro-resonance suppression circuit were designed for a CVT, that doesn't mean the same values will work on a power transformer of 900 MVA rating. So several sets of C, L and R are tried in our simulation system. But unfortunately, the ferro-resonance hasn't been suppressed (see Fig. 3.24).

From the above test, it can be seen that the effect of a mitigative measures depends highly on the particularly system itself. Which method is the best method to solve the ferro-resonance problem? The answer remains unknown until a large number of tests are done.

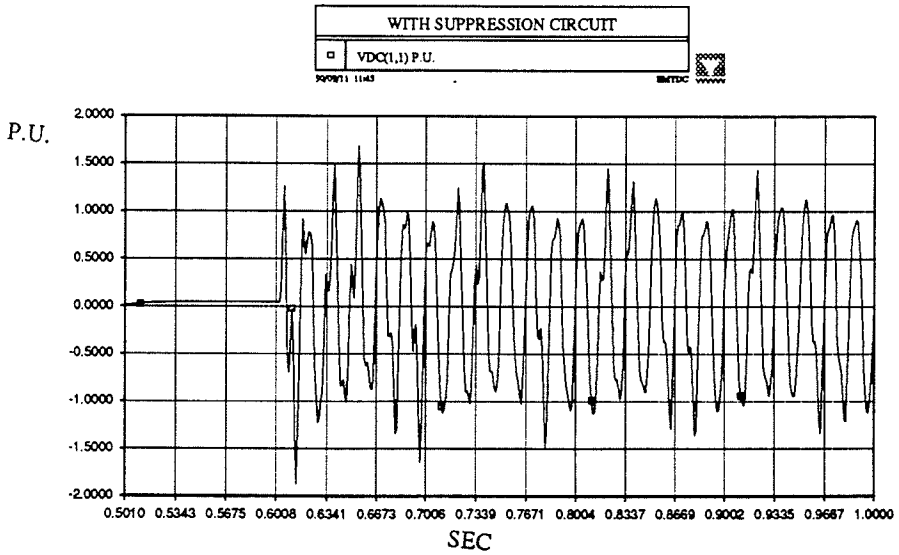


Fig. 3.24 Test With The Suppression Circuit

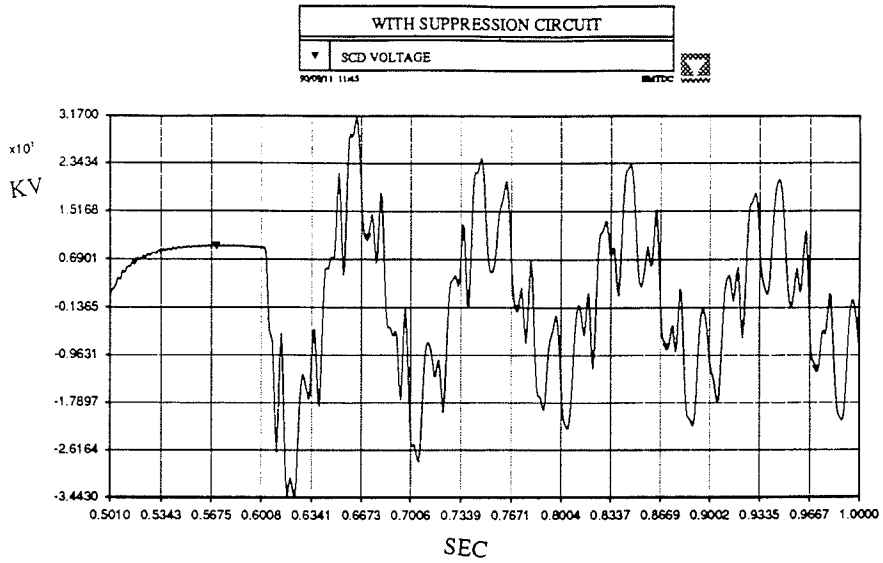


Fig. 3.24 (continue) Test With The Suppression Circuit

3.4 CONCLUSIONS

For the single phase test circuit, the following conclusions can be drawn down regarding suppression of ferro-resonance between the series capacitor and the transformer:

(1) The ferro-resonance effect, associated with the fault clearing near an unloaded transformer, is initiated by the remanent flux on the transformer and the residual voltage on the series capacitor left by the fault current. The subharmonic current resulting from the ferro-resonance depends on initial conditions and the L-C oscillation time constant (where, the non-linear element plays a key role).

(2) Subharmonic filters are recommended. Among three types of such filters [(1), (2) and (3) in 3.3.1], (1) appears best.

(3) A C-type filter (tuned at 60 HZ and 120 HZ) can also help the AC system to recover to the steady state.

(4) An MOV can give some assistance for decreasing the effect of ferro-resonance (Note: Within the possible selection area, the lower rated voltage is the better. But there is a problem with too low a rating MOV. Too low an MOV rating will cause the arrester to overheat in steady state. So a safety margin must be considered).

(5) Three methods of harmonic and subharmonic damping (the R + SWITCH method, the thyristor controlled resistor method, and the fundamental blocking filter method) can successfully eliminate the ferro-resonance in the fault recovery process of the single phase system.

(6) Another two methods (the thyristor controlled inductor method and the suppression circuit method) failed to solve the ferro-resonance problem in the simulation system.

Fig. 3.25 Single Phase Test With R+SWITCH

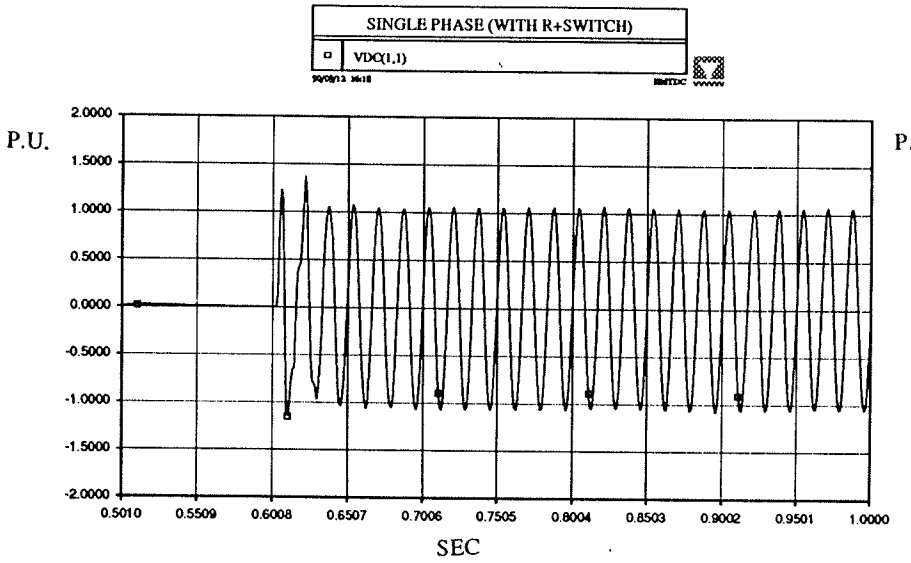
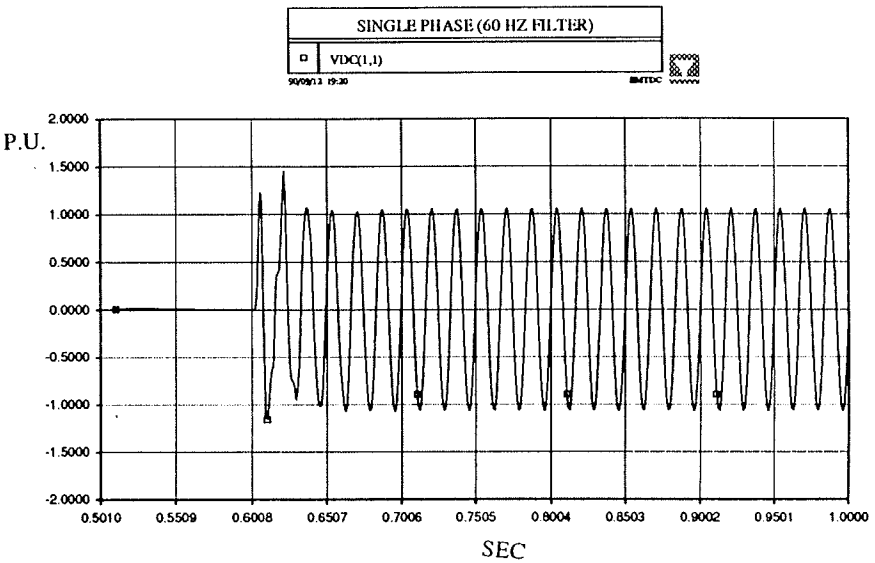


Fig. 3.26 Single Phase Test With Fundamental Blocking Filter



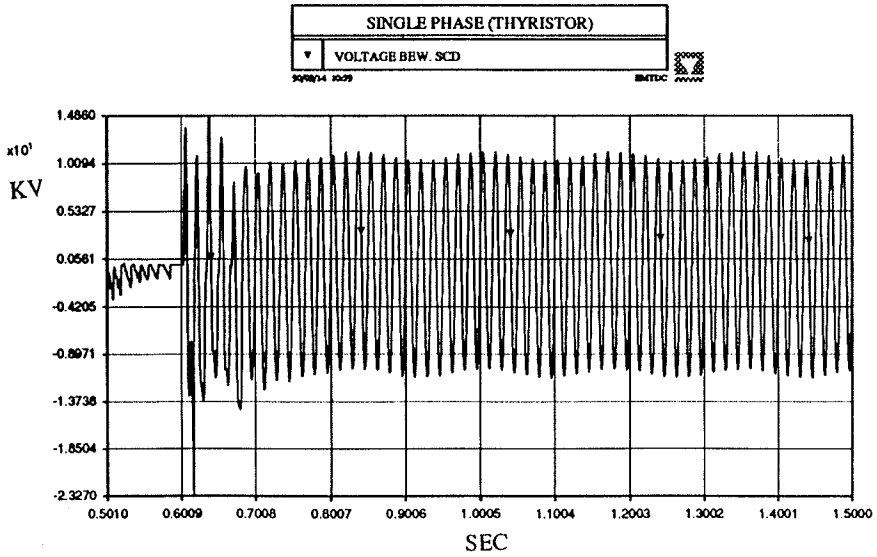


Fig. 3.27 Single Phase Test With Thyristor Controlled Resistor (R=1.0Ω)

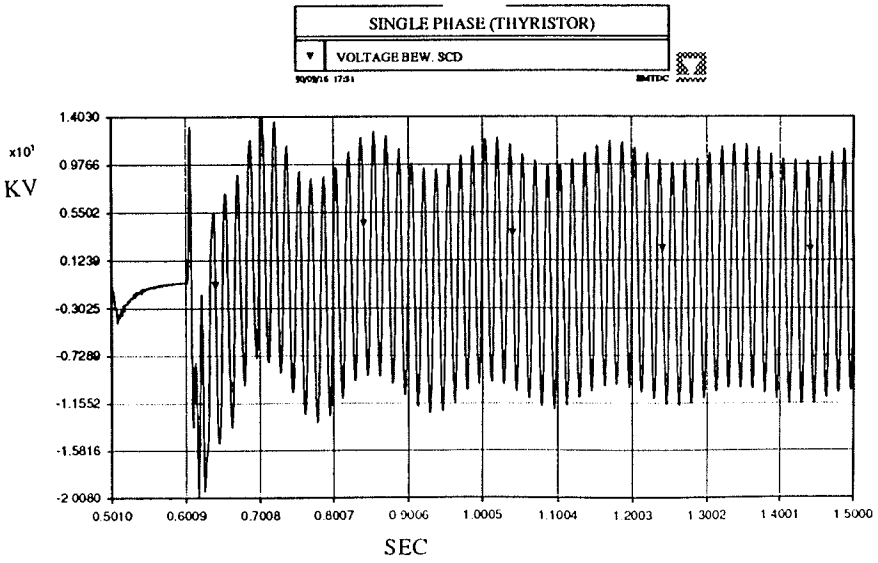


Fig. 3.28 Single Phase Test With Thyristor Controlled Resistor (R=100.0Ω)

Chapter 4

INVESTIGATION WITH THREE-PHASE TEST SYSTEM (WITH HVDC REPRESENTATION)

The previous chapter shows that the ferro-resonance can be readily overcome in the single-phase test system. Since the ferro-resonance response may be different in different AC/DC systems, the previously tested and some new mitigative methods are examined here for the HVDC test system in a three phase AC network.

4.1 TEST SYSTEM

The test system has been shown in Fig. 2.8. The summarized system data are given in Appendix A (Table A.1). It is a monopolar six pulse system with rated load (Pdc) of 810 MW (1800 A, 450 KV) measured at the inverter. Selection of six-pulse monopolar operation was selected to minimize the computation time. The receiving end and sending end AC system are separated by an 895 KM (556 miles) transmission line. The line details are also given in Appendix A (Table A.2). The component values of AC and DC filters are given in Appendix A (Table A.3). The effective short circuit ratio at the inverter is set at 1.5 without the series capacitor with the system impedance of 37 Ω $<78^0$. The 15 Ω series capacitor represents 225 MVAR series compensation at full DC load which increases the effective short circuit ratio from 1.5 to 2.67.

4.1.1 System Modelling

EMTDC was used to model and simulate the system dynamic behaviour. In order to minimize storage requirement and computation time, the system has been divided into 4 subsystems as shown in Fig. 2.8.

Subsystem 2 and 4 represent inverter and rectifier stations respectively. Each converter consists of:

(1) Three six-pulse valve groups per pole, each rated at 150 KV, 1.8 KA

(2) Converter transformers with leakage reactance of 13% on their own base

(3) Smoothing reactors of 0.75 H

(4) DC filters (6th and 12th harmonic)

A generalized six pulse valve group subroutine B6P110, available in EMTDC is used to represent the valve groups and converter transformer at sending end. Separate G6P110 valve group model, three-phase star-star-delta transformer, and TSAT21 transformer saturation model were used to represent converter at the receiving end.

In order to connect valve group model G6P110 to the AC source, another subroutine called ACINT4 is used [3] [4]

The inverter side transformer simulation is as follows:

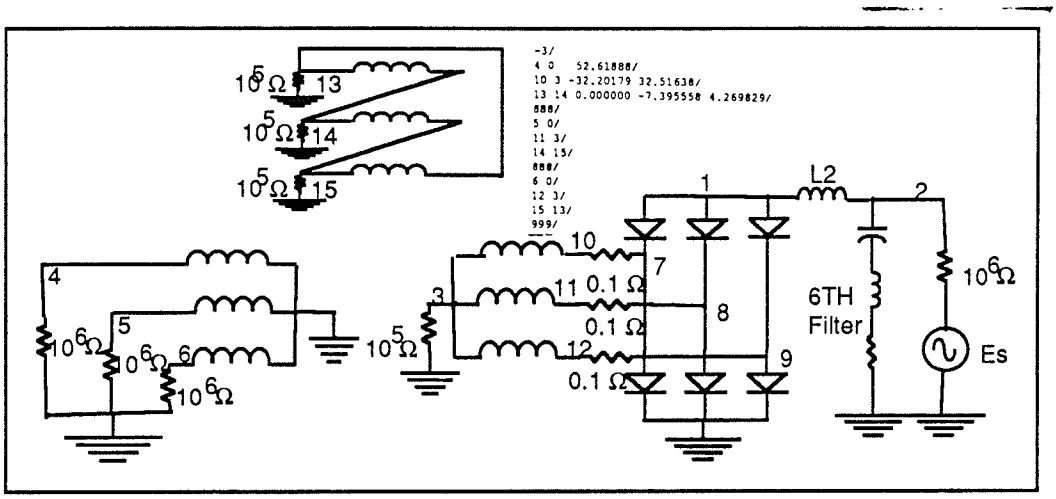


Fig. 4.1. Inverter Side Transformer Simulation

The condition is considered when the zero sequence impedance is less than the positive sequence impedance. This requires the addition of a delta winding to provide a parallel path for zero sequence current. Adding a neutral reactance to the star point in the secondary side of the transformer can increase the transformer's zero sequence reactance.

The transformer saturation is simulated the same as in Fig. 3.8.

The 895 Km long DC transformer line, connecting the two converters, is modelled as a frequency dependent, distributed parameter line.

Subsystems 1 and 4 (shown in Fig. 2.8) represent the receiving end and sending end

AC systems. The AC sources, both at the inverter end and rectifier end are modelled as infinite systems separated from their respective commutating buses by the system impedances. The AC system impedances are represented by R-RL networks having the same damping at fundamental and 2nd harmonic frequency. AC filters comprising of 5th, 7th, 11th, 13th harmonics and high pass are connected at the converter buses.

4.1.2 DC Controls

The DC system is assumed to be operating in constant current mode without any high level controller. Under steady-state conditions, the rectifier operates in constant current control and the inverter in constant extinction angle control. Besides these general control methods, the subroutine VDCL3 is also used at the rectifier (VDCL3 is a voltage dependent current limiting control subroutine)[1].

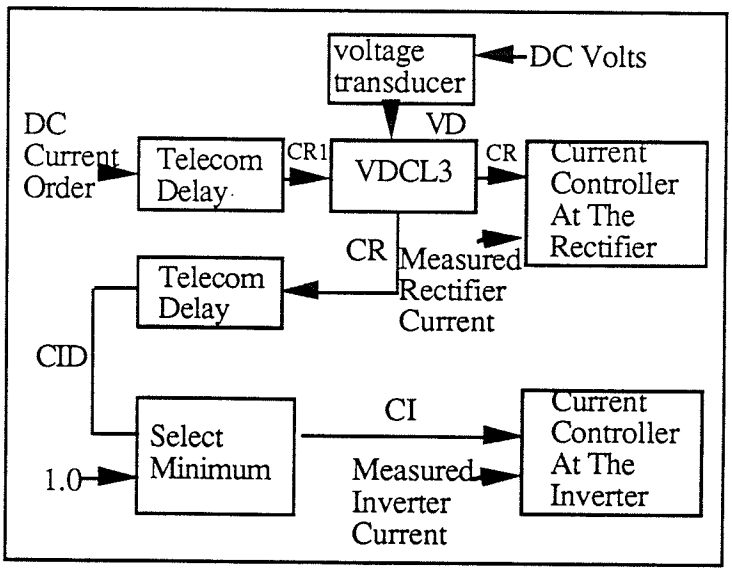


Fig. 4.2 Control Diagram Of Current Controls

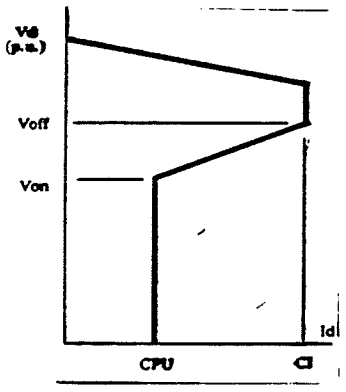


Fig. 4.3 Characteristic For VDCL3 (Straight Line Function)

VDCL3 can improve the HVDC system starting process excellently and can also help the HVDC system recovery from faults.

4.1.3 Fault Recovery Strategy

Evaluate the various ferromagnetic resonance damping methods on recovering from faults at the inverter side, by determining

(1) Time to recover 90% Id.

(2) Fault energy loss in MW-SEC (Fig. 4.4)

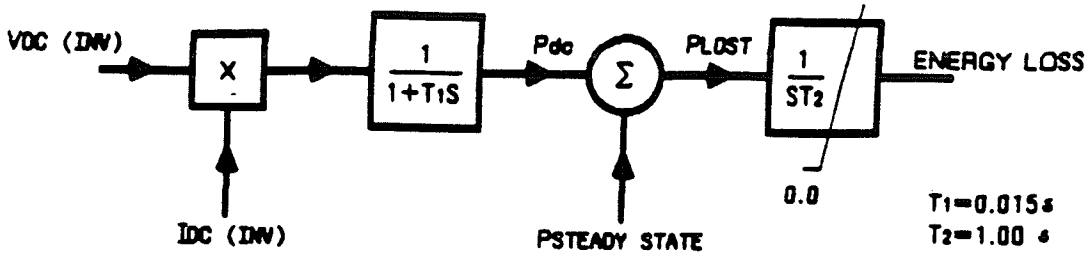


Fig. 4.4 Block Diagram Of Energy Meter

The block diagram for the measurement of the energy loss by the receiving end AC network due to the temporary loss of HVDC, following a disturbance is shown in Fig. 4.4. The DC power fed to the AC system through the HVDC link is computed by passing the product of DC voltage and DC current at the inverter through a lag function with a time constant T1 of 15 ms. Following a disturbance, any difference from the steady state power 'Ploss' is integrated over the rest of the simulation period to give the energy loss.

In all cases, the fault period is applied for 3 1/4 cycles. The fault starts from the maximum value of the AC voltage, clearing from the zero-crossing point of the AC voltage.

4.1.4 System Steady State

A single line diagram with a DC line compensated with series capacitor is shown in Fig. 4.5.

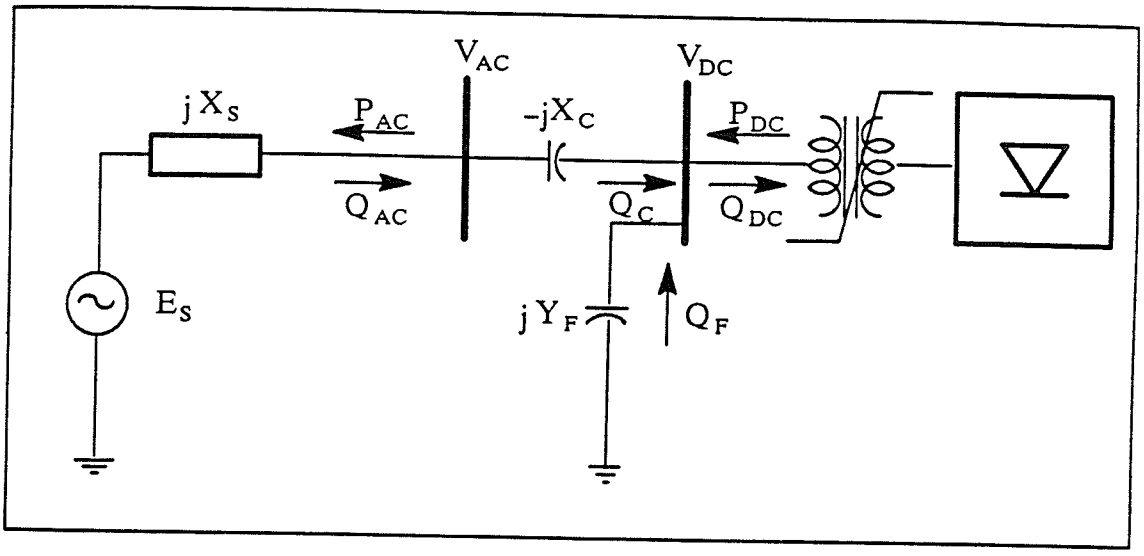


Fig. 4.5 Schematic Diagram Of DC Link Series Compensation

Rules for operating system are established as follows:

(1) When operating in steady state:

$$0.95 < V_{AC} < 1.05 \text{ P.U.}$$
$$\text{and } 0.95 < V_{DC} < 1.05 \text{ P.U.} \quad \text{.....(4.1)}$$

Adjusting the magnitude of ES or tap changer on the converter transformer can obtain the above conditions.

(2) ES can only be realistically changed between:

$$0.8 < ES < 1.2 \text{ P.U.} \quad \text{.....(4.2)}$$

(3) Filter reactive power Q_F should be less than full load DC reactive power Q_{DC}:

$$Q_F < Q_{DC} \quad \text{.....(4.3)}$$

In the steady state, the system satisfies above conditions at both inverter and rectifier sides.

The advantage of the series capacitor SCD is that the commutating voltage V_{DC} will not change too much between light load (Id = 0.3 P.U.) and full load (Id = 1.0 P.U.).

The Load Flow Program available in Manitoba HVDC Research Centre shows the consistence with EMTDC Program for the rated steady state of the HVDC system (Fig. 4.6).

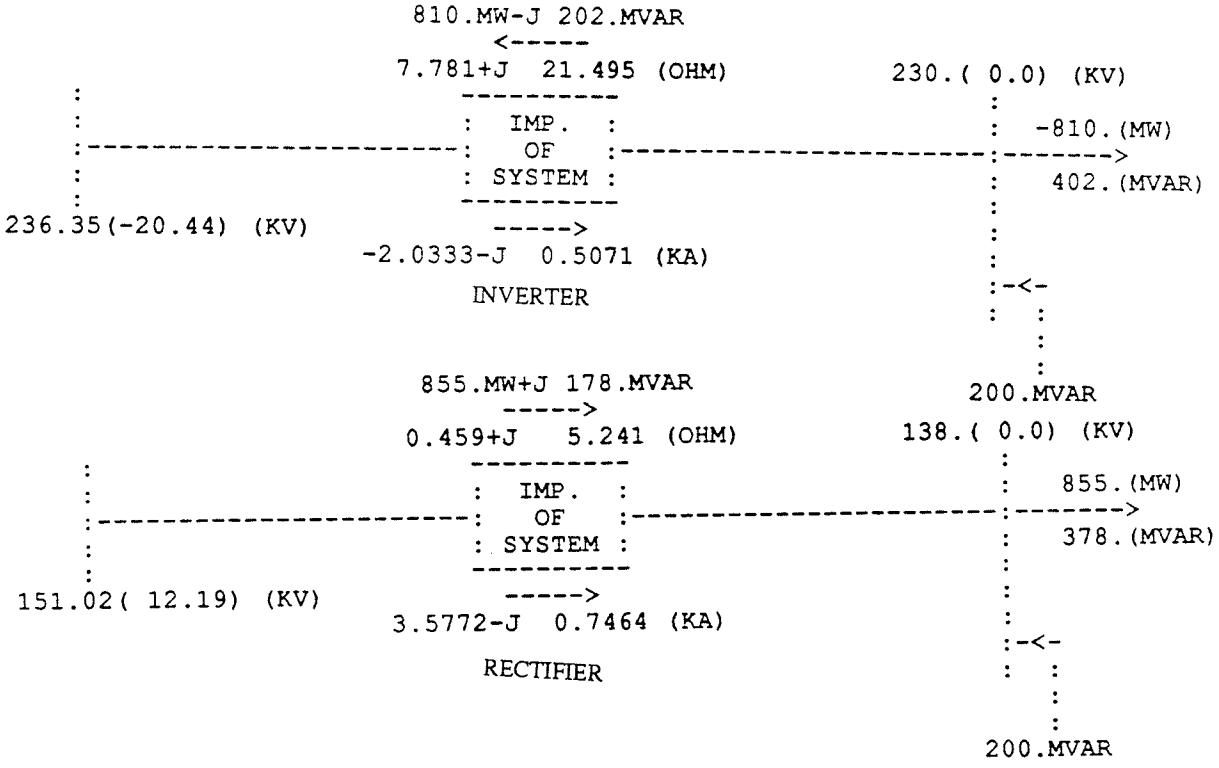


Fig. 4.6 The HVDC System Steady State

4.2 MITIGATIVE METHODS

We have already known that the ferro-resonance seriously affect the HVDC system's starting process and fault recovery process. The Ferro-resonance In HVDC system is different from in the single phase system which we have already studied in Chapter 3. So some methods which can effectively used in the single phase system will not suit the three-phase test system, such as the subharmonic filter and C-type methods. Some methods can still be effectively used to eliminate the ferro-resonance in the three-phase test system, such as R+SWITCH method, thyristor controlled resistor method, and the fundamental blocking filter method. Several new methods are also developed in this chapter.

4.2.1 Series Damping Filter Scheme[9]

The basic idea is that the combination is chosen such that their frequency characteristics give equal reactance at the power frequency and unequal reactance at the other frequencies. Because the ferro-resonance oscillations drive unsymmetrical three phase current, a two-phase modified circuit can compensated the unsymmetry. With the series damping filter scheme, in addition to the equal compensating capacitor banks on the three phases (C) in Fig. 4.7, two phases are modified by connecting in series with them two series resonance circuits (La, Ca, and Lc, Cc), as shown in Fig. 4.8.

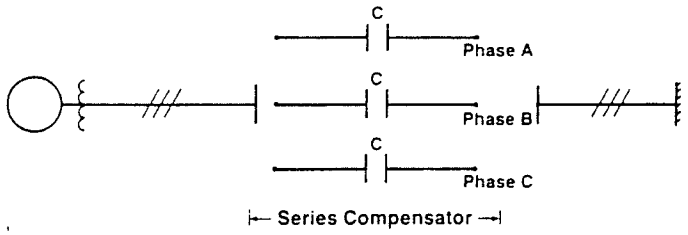


Fig. 4.7 Conventional Series Compensation Scheme

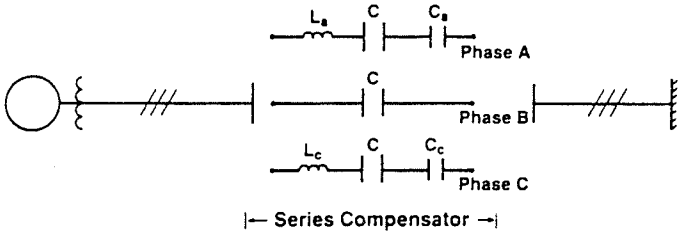


Fig. 4.8 Series Resonance Compensation Scheme

L and C of each resonance circuit are given by:

$$w0 = \sqrt{1/LaCa} = \sqrt{1/LcCc} \quad \text{.....(4.4)}$$

where w0 is the system fundamental frequency.

The ratio C/Ca and C/Cc are considered as degree of asymmetry between the three phases. After the comparison, C/Ca = 0.25 and C/Cc = 0.5 are chosen.

The tests of HVDC system starting-up and fault recovery for this scheme show that the series damping filter scheme can only improve recovery for the light load case (such as Id = 0.3 P.U.)

Fig. 4.11 shows the HVDC system light load starting process with this scheme. Fig. 4.12 shows the HVDC system light load SLGF recovery process.

4.2.2 Parallel Damping Filter Scheme[9]

The basic idea is as the same as the series damping filter scheme, With the parallel damping filter scheme, two phases are modified by shunting a part of the compensating capacitor banks (C) in Fig. 4.7 with parallel resonance circuits as shown in Fig. 4.9.

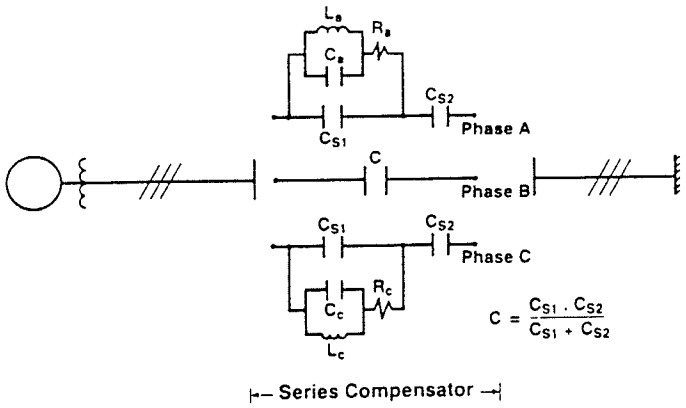


Fig. 4.9 Parallel Resonance Compensation Scheme

Again, L, C in each of the resonance circuit are governed by formula (4.4). Rc & Rs is selected as 1.0 Ω.

Fig. 4.13 shows the HVDC system full load starting process with this scheme. Fig. 4.14 shows the HVDC system light load SLGF recovery process. From these simulation results, it can be seen that the ferro-resonance can be completely eliminated in these cases.

4.2.3 2nd Harmonic Filter

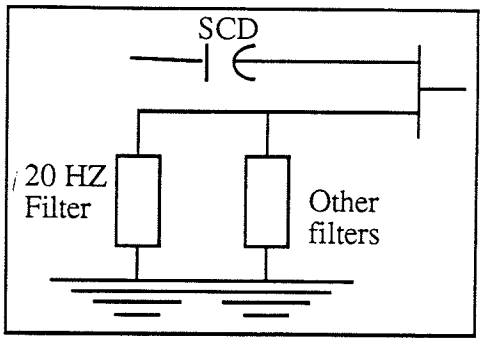


Fig. 4.10 Shunt 2nd Harmonic Filter

The 2nd harmonic filter can successfully eliminate the ferro-resonance, so it can help the HVDC system to start-up and to recover from faults. Fig. 4.15 shows the HVDC system full load starting process with the 2nd harmonic filter. Fig. 4.16 shows the HVDC system full load SLGF recovery process with the 2nd harmonic filter.

Table 4.1--4.4 are the summaries of above three method.

These tables show: comparing the several filters, the 2nd harmonic filter is the most effective method to eliminate the ferro-resonance, but a voltage dependent current limit control is also very important.

Table 4.1 Light Load Starting Process

Cases / Parameters	No Transformer Saturation	With Transformer Saturation And No Damping	Series Damping Filter	Parallel Damping Filter
Starting Time (Second)	With VDCL3 0.267	———	0.48	0.45
Steady State Filter Losses (MW)	With VDCL3 1.5	———	1.6	3.0

Table 4.2 Light Load Faults

Cases / Parameters	No Transformer Saturation	With Transformer Saturation And No Damping	Series Damping Filter	Parallel Damping Filter
Starting Time (Second)	0.176	———	0.4	0.28
Energy Losses During Fault (MW. SEC)	30.0	———	72.5	50.0

Table 4.3 Full Load Starting Process

Cases / Parameters	No Transformer Saturation	With Transformer Saturation And No Damping	2nd Harmonic Filter	Series Damping Filter	Parallel Damping Filter
Starting Time (Second)	With VDCL3 0.47 Without VDCL3 1.13	———	With VDCL3 0.68 Without VDCL3 ———	———	0.73
Steady State Filter Losses (MW)	With VDCL3 6.86 Without VDCL3 6.86	———	With VDCL3 10.3 Without VDCL3 ———	———	6.90

Table 4.4 Full Load Faults

Cases / Parameters	No Transformer Saturation	With Transformer Saturation And No Damping	2nd Harmonic Filter	Series Damping Filter	Parallel Damping Filter
Starting Time (Second)	With VDCL3 0.47 Without VDCL3 ———	———	With VDCL3 0.394 Without VDCL3 0.395	———	———
Energy Loses During Fault (MW. SEC)	With VDCL3 147.4 Without VDCL3 ———	———	With VDCL3 227.9 Without VDCL3 172.3	———	———

Fig. 4.11 Test With Series Damping Filter In Starting Process

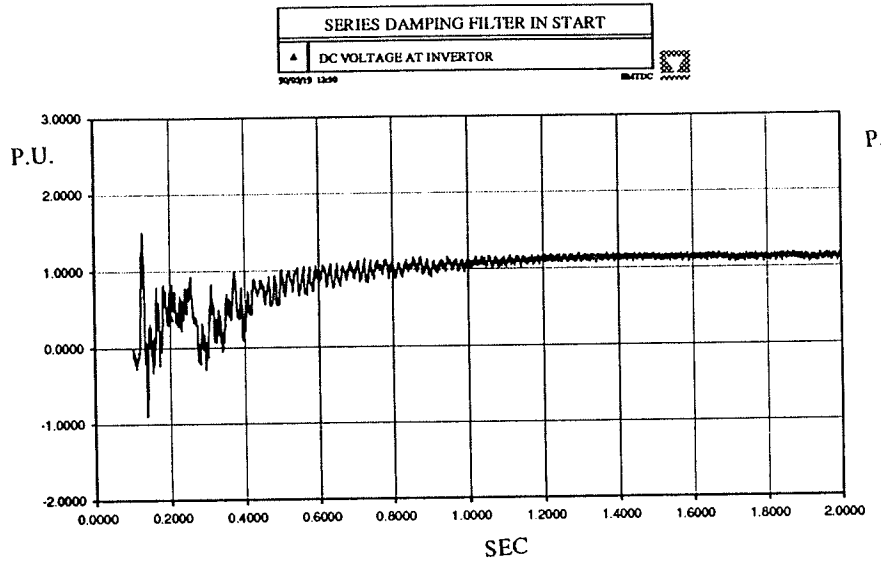
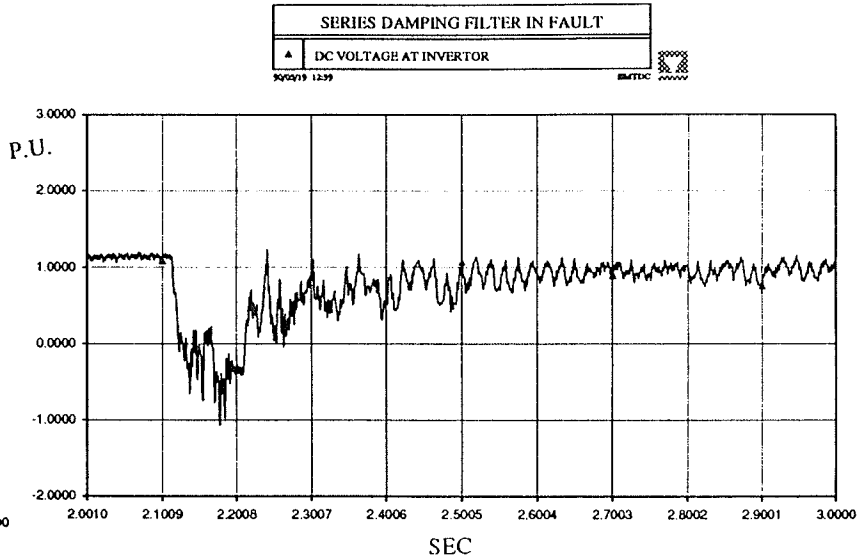


Fig. 4.12 Test With Series Damping Filter In Fault Process



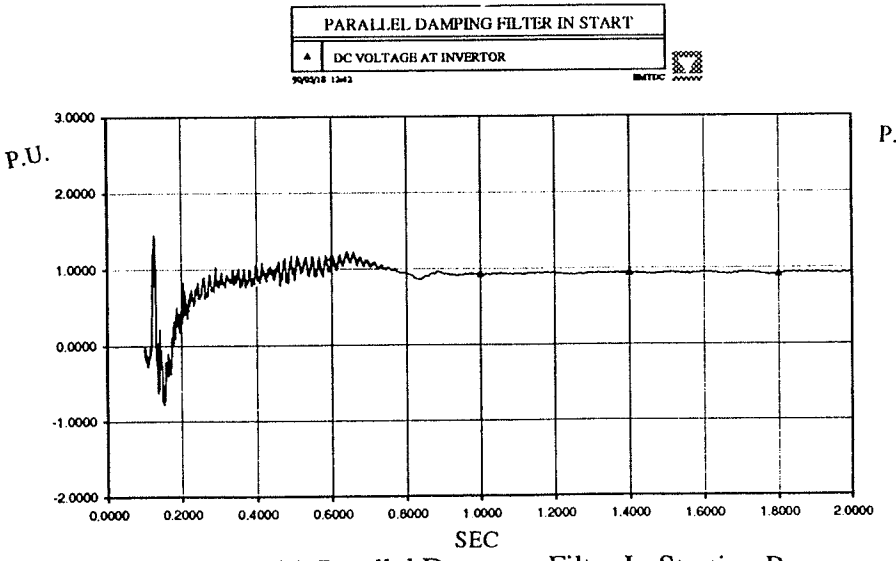


Fig. 4.13 Test With Parallel Damping Filter In Starting Process

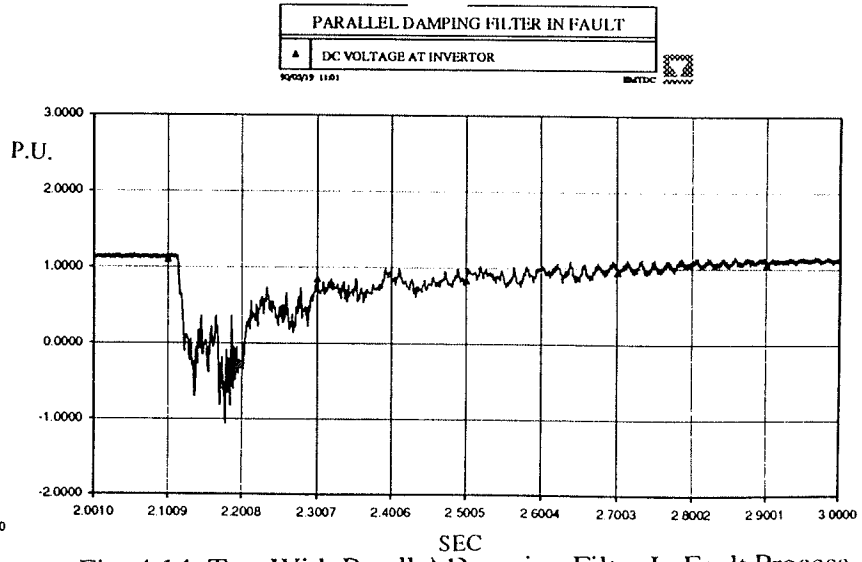
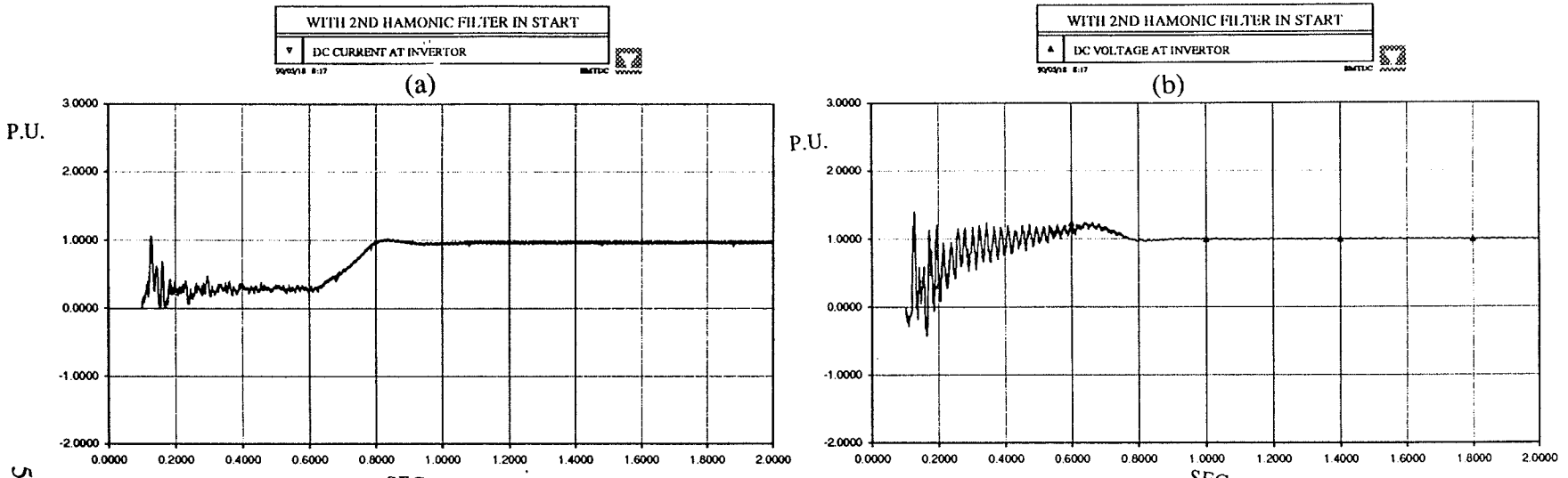


Fig. 4.14 Test With Parallel Damping Filter In Fault Process

Fig. 4.15 Test With 2nd Harmonic Filter In Starting Process



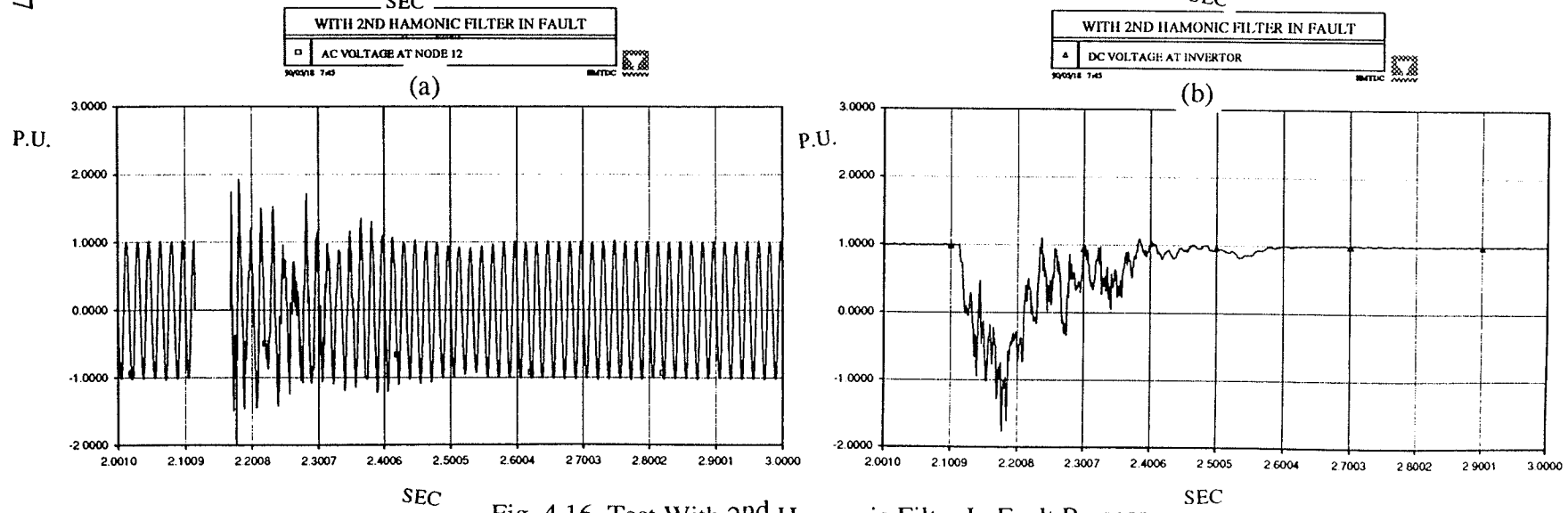


Fig. 4.16 Test With 2nd Harmonic Filter In Fault Process

4.2.3.1 Redesign The Capacity Of Filters

From the previous analysis, it can be seen that the 2nd harmonic filter provides a good solution of the ferro-resonance problem in the HVDC system. With the 2nd harmonic filter, the HVDC system can recover from various AC or DC faults successfully. But when a 2nd harmonic filter is added in the original system, we don't want to change the total reactive power of the filters, and we don't want to increase the harmonic distortion level. So we need to test this further with the following tests:

Test 1. Select different sizes of filter in different MVAR ratings of filter

The size of a filter is defined as the reactive power that the filter supplies at fundamental frequency. It is substantially equal to the fundamental reactive power supplied by the capacitors. For example, look at a tuned filter in Fig. 4.17.

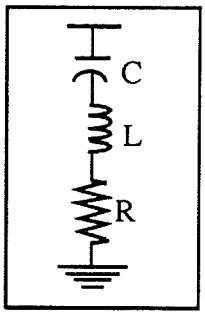


Fig. 4.17 A tuned filter

Using the 2nd harmonic filter (4.4 μF, 0.4 H, 10.7 Ω), which is the minimum rating to eliminate the ferro-resonance in the HVDC system, (i.e. with a smaller rating, the HVDC system couldn't recover from faults), then

$$Q = 3\,[I^2/(W\,C) - I^2\,W\,L] = V_{l\text{-}l}{}^2/(3\,W\,L) = 117.0\ (MVAR) \quad \text{.....(4.5)}$$

For the selected test system, the total rating of 5th, 7th, 11th, 13th, and HP filters is 200 MVAR, the reactive power required at the invertor bus Qdc is 425 MVAR. At rated state, the series capacitor is chosen to supply 225 MVAR reactive power, see Fig. 4.18.

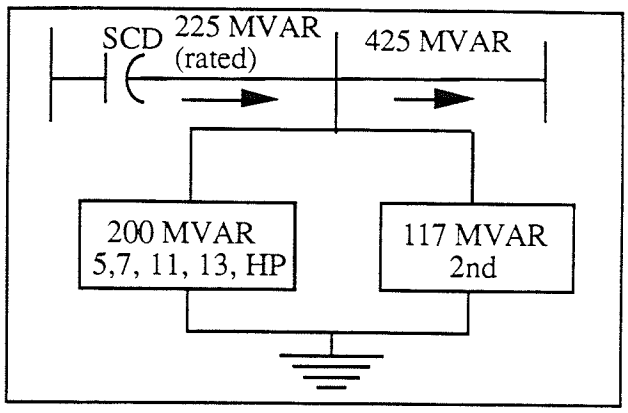


Fig. 4.18 The reactive flow in HVDC system

From Fig. 4.18, it can be seen obviously that there is a reactive power unbalance in this system. Because of the added second harmonic filter, the system will adjust its rated state to another operating state itself. But we don't want to change the original steady state. Can we reduce the total rating of these filters to 200 MVAR? Several preconditions must be considered in the redesign process:

(1) Do not increase total filter losses. For original filters, the filter losses are 10.3 MW/810.0 MW = 1.3%. Filter losses depend on the filter resistors. So for the new filter design, if we don't increase the value of filter resistors, the filter losses won't be increased.

(2) Ensure that filter resistance is not too high at tuned frequency, since it will cause some harmonic currents to enter the system, and particularly add to telephone interference. So we need to check the harmonic distortion constant (see test 2).

(3) If there is no filter resistance, we will have undamped filters. The volts across reactor or capacitor components will get too high during disturbances. The filter quality is selected to achieve optimal filter operation, i.e. the selected value should inject minimum harmonic current into the network for the network condition that is assumed. A large Q reduces the filter losses and the harmonic voltage (when the filter is correctly tuned), but it increases the risk of parallel resonance between the filters and the network by reducing damping.

Based on these three points, a group of new filters are designed as 217.0 MVAR, while the rating of original filters plus 2^{nd} harmonic filter is 317.0 MVAR.

The structure of both the filter groups is the same, see Fig. 4.19, which includes the 2nd, 5th, 7th, 11th, 13th and high-pass filter.

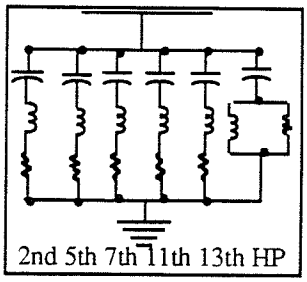


Fig. 4.19 The AC filters at the inverter side

The elements of original filters and new filters are as follows respectively:

The original filters with the second harmonic filter added are:

Table 4.5 Data of original filters

Types / Elements	2 ND	5 TH	7 TH	11 TH	13 TH	HP
R (Ω)	10.7	7.11	7.11	2.66	2.66	47.4
L (H)	0.4	0.1493	0.1493	0.0393	0.0393	0.0036
C (μF)	4.4	1.885	0.9618	1.479	1.056	4.559

The 5th, 7th, 11th, 13th and HP filters can supply 200.0 MVAR reactive power. The 2nd harmonic filter can supply 117.0 MVAR reactive power. So the total rating is 317.0 MVAR.

The new filters are designed as:

Table 4.6 Data of new filters

Types / Elements	2 ND	5 TH	7 TH	11 TH	13 TH	HP
R (Ω)	10.7	7.11	7.11	2.66	2.66	63.6
L (H)	0.4	0.2986	0.2986	0.0786	0.0786	0.0072
C (μF)	4.4	0.9425	0.481	0.7395	0.528	2.2795

The rating of the 5th, 7th, 11th, 13th and HP filters is decreased a half than original filters, i.e. 100.0 MVAR. The rating of 2nd harmonic filter remains the same value as the original filter, i.e. 117.0 MVAR which is already the minimum value. So the total rating of new filters is 217.0 MVAR. Because the filter resistors are not changed, the filter losses will remain the same as before.

Test 2. Calculation of harmonic distortion constant

An ideal in filter design is the elimination of all the detrimental effects caused by waveform distortion, and particularly telephone interference. However, this ideal criterion is unrealistic because of the difficulty of estimating in advance the harmonic flow throughout the AC system. It is also uneconomic and, in the case of telephone interference, the problem can normally be solved more economically by taking some of the preventive action in the telephone system itself.

A more practical solution is the reduction of harmonic current to an acceptable level in the AC system. With new filters, we don't want to increase the harmonic distortion constant. So the comparisons between original filters and new filters are given in two simulation cases:

(1) Ground return in the DC line model

In this case, because of ground losses at high frequency, there is more damping. So in DC system start period or AC & DC fault periods, the waveforms of DC current and DC voltage have less oscillations than the metallic return case.

Using EMTDC Fourier analysis program EMTFS, we can analyse AC current. The output gives the harmonic No., the frequency, the magnitude and the angle. In order to be convenient in calculation, the magnitude is used as percentage number, designated 100 at the fundamental frequency. Fig. 4.20 shows the comparison of magnitude vs harmonic corresponding to both original filters and new filters. In Fig. 4.20, there is a little smaller magnitude versus frequency with new filter group than with original filter group.

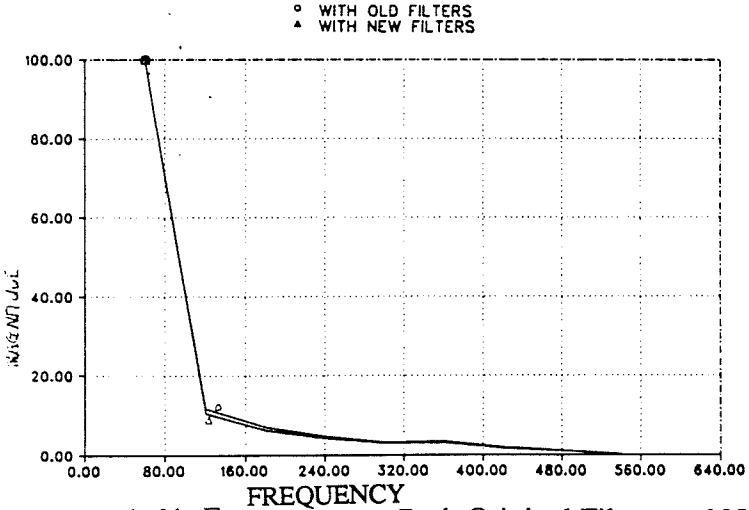


Fig. 4.20 Magnitude Vs Frequency For Both Original Filters and New Filters

The total harmonic current distortion is calculated as follows:

For original filters:

$$\frac{\sqrt{\sum_{f=2}^{9} I_f^2}}{I_1} = \sqrt{\sum_{f=2}^{9} \left(\frac{I_f}{I_1}\right)^2}$$

$$= \sqrt{0.1133^2 + 0.06875^2 + 0.04999^2 + 0.03061^2 + 0.03189^2 + 0.01990^2 + 0.01149^2 + 0.0009616^2}$$

$$= 0.1502 \qquad (4.6)$$

For new filters:

$$\frac{\sqrt{\sum_{f=2}^{9} I_f^2}}{I_1} = \sqrt{\sum_{f=2}^{9} \left(\frac{I_f}{I_1}\right)^2}$$

$$= \sqrt{0.1050^2 + 0.06259^2 + 0.04321^2 + 0.03076^2 + 0.03108^2 + 0.01707^2 + 0.01082^2 + 0.002609^2}$$

$$= 0.1383 \qquad (4.7)$$

where: I_1--the fundamental current

I_f--the current corresponding the frequency f

From calculation (4.6) and (4.7), it can be seen that new filters have less harmonic current distortion than original filters.

In Canada and United States, the multiplication of ***I*T is*** usually used to evaluate the disturbance of electric transmission line to telephone line. The multiplication of ***I*T*** is the root square of the sum of every harmonic current (KA) multiplied by the corresponding TIF (Telephone Interference Factor), i.e.

$$I*T = \sqrt{\sum (I_f * T_f)} \qquad \text{.....(4.8)}$$

where: I_f--the rms current corresponding the frequency f

T_f--the TIF corresponding the frequency f (see table 4.7)

According to the suggestion of "EHV AC/DC Inductive Coordination and Electric

Protection" working group of the United States Communication Association, the value of ***I*T*** should be below 10 KA, then there will be no disturbance problem for the telephone line[21].

Table 4.7. gives the TIF value in the Bell Telephone System (B.T.S)--Edison Electric Institute System (E.E.I).

Table 4.7 TIF in B. T. S--E. E. I

n	f (HZ)	TIF
1	60	0.5
2	120	10
3	180	30
4	240	105
5	300	225
6	360	400
7	420	650
8	480	950
9	540	1320

According to (4.8), calculations for both original filters and new filters are written in formula (4.11), (4.12), respectively (see p.65).

Obviously, new filters give smaller disturbance than original filters for telephone line interference. But both groups do not satisfy the criterion of ***I*T < 10 KA***. So, preventive action in the telephone system itself is required. This is much more realistic and economic than using ideal filters which satisfy the condition ***I*T < 10 KA.***

(2) Metallic return in the DC line model

In general, the use of ground as a permanent conductor is rarely permitted and a bipolar arrangement is used with equal current in the two metallic lines. The disturbance level in the metallic line return case is higher than in the ground return case, because of the less damping at high frequency.

Fourier analysis of the AC current is done with a metallic mode DC line. Fig. 4.21

shows the comparison of current magnitude vs harmonic corresponding to both original filters and new filters. In Fig. 4.21, there is a little smaller harmonic magnitude with the new filter group than with the original filter group.

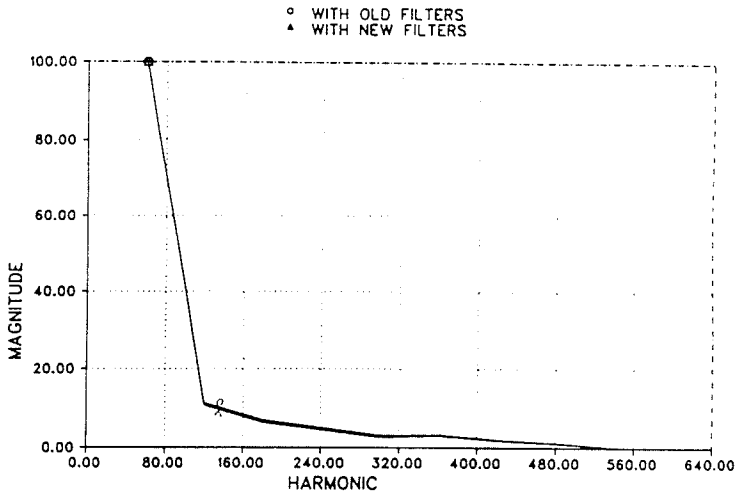


Fig. 4.21 AC Current Magnitude Vs Harmonic For Both Original Filters And New Filters

The total harmonic distortion is calculated as follows:

For original filters:

$$\frac{\sqrt{\sum_{f=2}^{9} I_f^2}}{I_1} = \sqrt{\sum_{f=2}^{9} \left(\frac{I_f}{I_1}\right)^2}$$

$$= \sqrt{0.1172^2 + 0.07029^2 + 0.04749^2 + 0.03238^2 + 0.03430^2 + 0.01938^2 + 0.0110^2 + 0.002909^2}$$

$$= 0.1538 \qquad (4.9)$$

For new filters:

$$\frac{\sqrt{\sum_{j=2}^{9} I_f^2}}{I_1}$$

$$= \sqrt{0.1074^2 + 0.06325^2 + 0.04579^2 + 0.0270^2 + 0.02985^2 + 0.01870^2 + 0.01168^2 + 0.0006025^2}$$

$$= 0.1405 \qquad (4.10)$$

Where, I_1 and I_f have the same definition as before.

$$I * T = \sqrt{\sum_{i=0}^{9} (I_f * T_f)^2}$$

$$= \sqrt{(1*0.5)^2+(0.1133*10)^2+(0.06875*30)^2+(0.04999*105)^2+(0.03061*225)^2+(0.03189*400)^2+(0.0199*650)^2+(0.01149*950)^2+(0.00096*1320)^2}*2.$$

$$=46.11 \text{ (KA)} \qquad (4.11)$$

The formula (4.11) shows the calculation of TIF for original filters with ground return case.

$$I * T = \sqrt{\sum_{i=0}^{9} (I_f * T_f)^2}$$

$$= \sqrt{(1*0.5)^2+(0.105*10)^2+(0.06259*30)^2+(0.04321*105)^2+(0.03076*225)^2+(0.03108*400)^2+(0.01707*650)^2+(0.01082*950)^2+(0.002609*1320)^2}*2$$

$$=43.29 \text{ (KA)} \qquad (4.12)$$

The formula (4.12) shows the calculation of TIF for new filters with ground return case.

$$I * T = \sqrt{\sum_{i=0}^{9} (I_f * T_f)^2}$$

$$= \sqrt{(1*0.5)^2+(0.1172*10)^2+(0.07029*30)^2+(0.04749*105)^2+(0.03238*225)^2+(0.03430*400)^2+(0.01938*650)^2+(0.011*950)^2+(0.002909*1320)^2}*2.$$

$$=47.11 \text{ (KA)}$$

The formula (4.13) shows the calculation of TIF for original filters with metallic return case.

$$I * T = \sqrt{\sum_{i=0}^{9} (I_f * T_f)^2}$$

$$=\sqrt{(1*0.5)^2+(0.1074*10)^2+(0.06325*30)^2+(0.04579*105)^2+(0.027*225)^2+(0.02985*400)^2+(0.0187*650)^2+(0.01168*950)^2+(0.0006*1320)^2}*2.0$$

$$=43.78 \text{ (KA)} \qquad (4.14)$$

The formula (4.14) shows the calculation of TIF for new filters with metallic return case.

From calculation (4.11) and (4.12), it can be seen that new filters have less harmonic current distortion than original filters (see p.65).

Calculations of I^*T value according formula (4.8) are given in formula (4.13) and (4.14), corresponding to original filters and new filters respectively (see p.65).

The total rating of AC filters has been successfully decreased to 217.0 MVAR from the original 317.0 MVAR, then near unity power factor can be maintained at the commutation bus at full load. The new filter group doesn't increase the filter losses and telephone interference level.The next step is to check the fault recovery ability corresponding to both filter group cases.

4.2.3.2 Tests Of Various Fault Cases In HVDC System (With The 2nd Harmonic Filter)

A further comparison between original filters and new filters under various fault cases is undertaken. We use 0.3 P.U. DC current to simulate the light load case, while the 1.0 P.U. DC current represents the full load case. Because there is a less damping in the metallic return in the DC line model, the metallic return case is more oscillatory than the ground return case. In the following simulations, we only consider the metallic mode DC transmission line.

The following faults are simulated to study the recovery ability for both original filter group and new filter group:

(1) SLGF at the inverter commutating bus

(2) 3LGF at the inverter commutating bus

(3) SLGF near the inverter commutating bus

(4) 3LGF near the inverter commutating bus

(5) Single phase AC source loss fault at the inverter side AC system

(6) Three phase AC source loss fault at the inverter side AC system

(7) DC line fault at the inverter end

Simulations are performed for a duration of 1.0 second. All the faults are applied between 2.114---2.168 second (for a duration of 3.25 cycles), from a steady state condition. In order to simulate the worst case, every AC fault which is near the inverter commutating bus is initiated at the maximum value of the AC voltage, and cleared at the zero-crossing point of the AC voltage.

Note that these faults are applied to both AC and DC circuits with the former being balanced as well as unbalanced. The ac faults are applied only at the inverter, because the ferro-resonance phenomena only happened at the inverter system where the series capacitor is located.

As the precondition, the following parameters are recorded in appropriate tables:

(1) The integral gain (GI) in extinction angle controller (VG6P18) at the inverter side

(2) The integral gain (GI) in DC current controller (POLPI5) at the inverter side

(3) The proportional gain (GP) in DC current controller (POLPI5) at the inverter side

HVDC control parameters are found to influence the speed of recovery of the DC system from faults. The optimal parameters depend not only on the AC system but also on the type of disturbance. Therefore, for each given simulation case, optimization of these parameters is also required.

An example is given as a SLGF case at the inverter commutating bus. The fault starts from light load steady state. Fig. 4.23(a) shows the variation of DC power for integral gain GI equal to 75.0 in the extinction angle controller. Fig. 4.23(b) is the variation of DC power under the condition of GI equals 55.0. With GI = 75.0, after fault clearance, the system can recovery to the steady state successfully. But with GI = 55.0, the system is unstable with the same disturbance. This shows the DC control parameter plays a key role in fault recovery.

Usually, in real HVDC systems, a start up ramp is used for the current order to bring the DC system into steady state as shown in Fig. 4.22. A value of 200.0 ms for 'Tramp' enables smooth system start up.

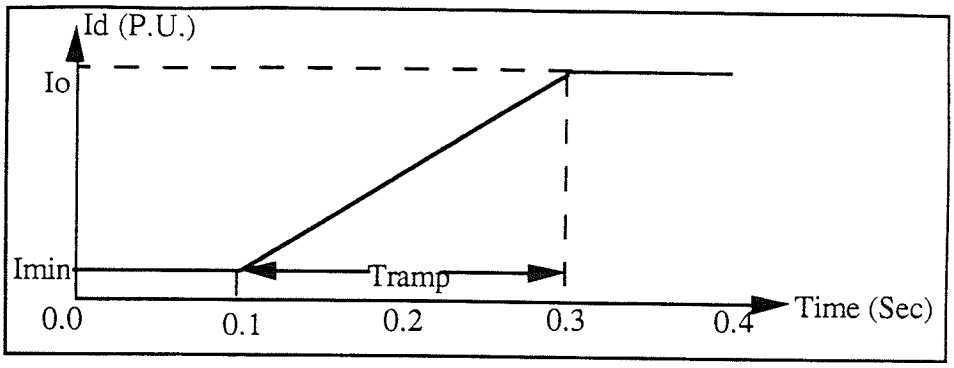
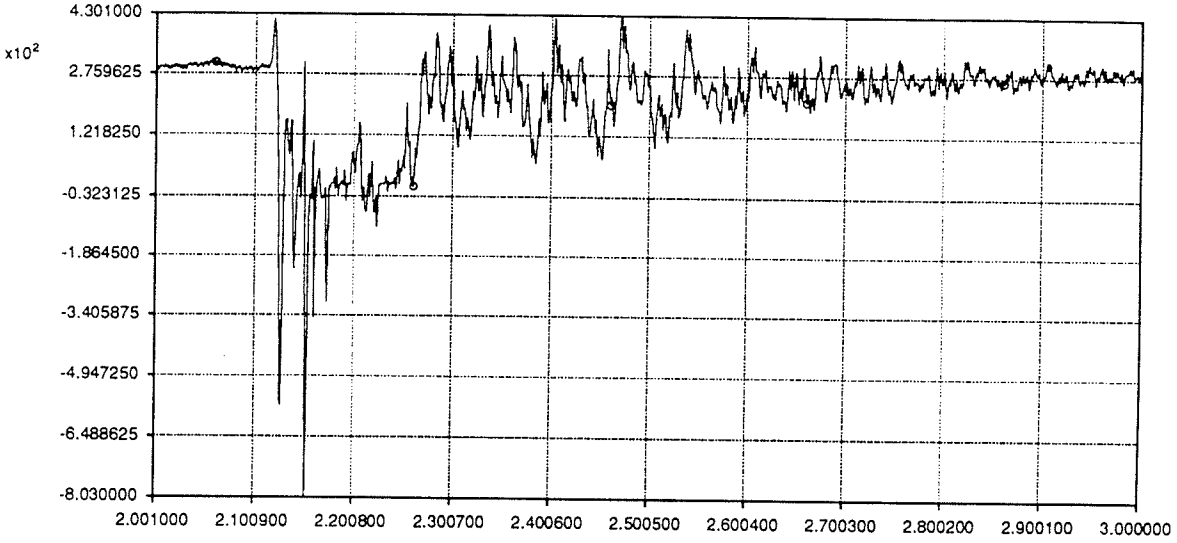
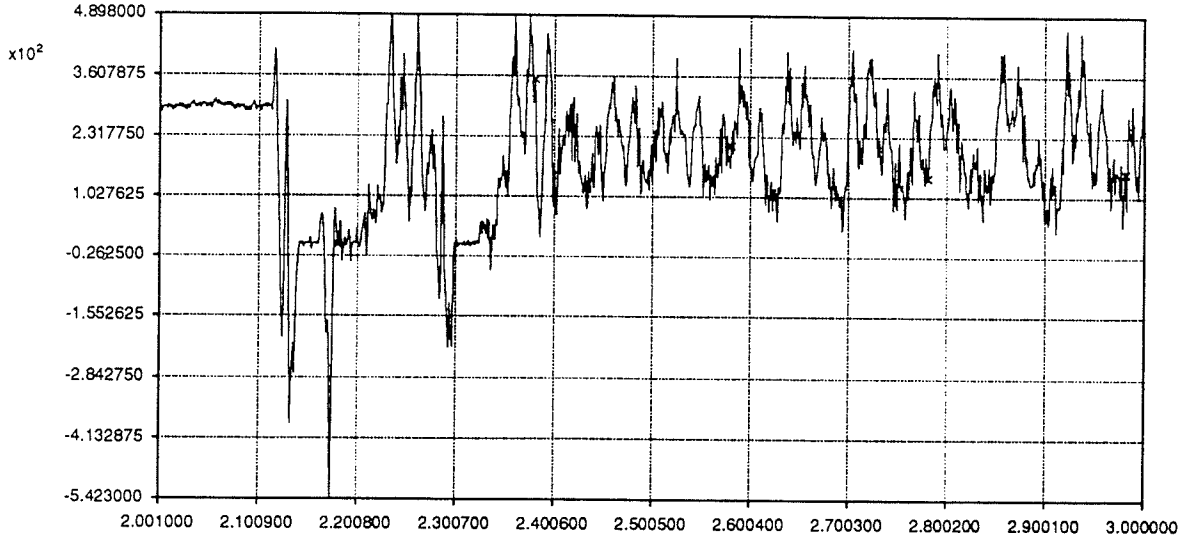


Fig. 4.22 Starting-up ramp used in real system



(a) DC Power With GI = 75.0



(b) DC Power With GI = 55.0

Fig. 4.23 A Comparison Of Control Parameter

In most digital simulation cases, the worst case is considered. In order to get the largest disturbance in the start up process, a step current order is used as shown in Fig. 4.24. This indicates how robust the method is in eliminating the ferro-resonance during system start up process.

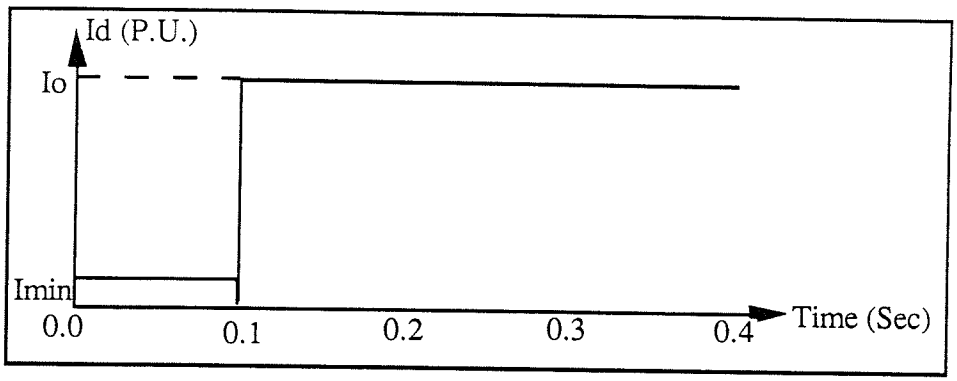


Fig. 4.24 Starting-up current order used in digital simulation system

The smoothing start up current order is shown in Fig. 4.25.

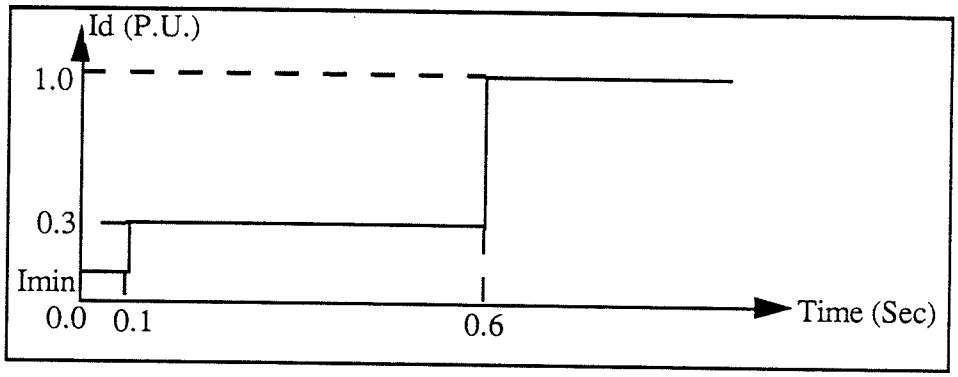


Fig. 4.25 Smoothing Starting-up current order used in digital simulation case

DC system is deblocked at Time=0.1 second, then DC current order is given as two step functions: At Time=0.1 second, Io1=0.3 P.U.; At Time=0.6, Io2=1.0 P.U. This is shown in Fig. 4.26. This can smooth the system start up process.

1. The light load case (0.3 P.U. DC current)

(1) With original filters (include 2nd harmonic filter, the total rating is 317.0 MVAR)

Table 4.8 is a summary of inverter DC control parameters corresponding to the disturbance in the light load case with original filters. The table also gives the time to get

the system steady state. In this table, GI means the integral gain; GP is the proportional gain; VG6P18 means the inverter extinction angle controller; POLPI5 is the inverter DC current controller. The Multiple Run[1] can be used to select the gain values.

(a) For DC system start up, from Fig. 4.26 and Table 4.8, some observations are made:

(1) Under the condition of GI in VG6P18 equals 35.0, GI in POLPI5 equals 2.0, GP in POLPI5 equals 0.15, the system can successfully start up.

(2) During the transient state, the system suffered dynamic overvoltage and overcurrent. By smoothing the start up process as shown in Fig. 4.25, the dynamic overvoltage and overcurrent is reduced. Because the purpose in this thesis is to eliminate ferro-resonance, the worst case is simulated here (see Fig. 4.26).

From Fig. 4.26, it can be seen that the 2nd harmonic filter can effectively eliminate ferro-resonance in light load HVDC system start up process.

(b) For a SLGF at the inverter commutating bus, from Fig. 4.27 and Table 4.8, the following observations are made:

(1) Under the condition of GI in VG6P18 equals 75.0, GI in POLPI5 equals 2.0, GP in POLPI5 equals 0.015, the system can successfully recover from this unbalanced AC fault.

(2) A SLGF at the commutating bus is a severe fault, which can cause inverter commutation failure. Because of AC system unbalance, additional characteristic and non-characteristic harmonics are produced. The whole loss (include the filter loss) is increased.

(c) For a 3LGF at the inverter commutating bus, from simulation graphs and Table 4.8, the following observations are given:

(1) Under the condition of GI in VG6P18 equals 15.0, GI in POLPI5 equals 2.0, GP in POLPI5 equals 0.015, the system can recover from this kind of fault successfully.

(2) 3LGF at the commutating bus causes the inverter to have multiple commutation failures. This is the most severe AC fault in HVDC system. In this case, the DC energy loss is 85.0 MJ.

(3) Although during the fault period a 3LGF is much worse than a SLGF, the balanced AC fault is easy to recover from than the unbalanced AC fault (compare (b) and (c)). It seems that more ferro-resonance exists in an unbalanced system. This is because a unbalanced fault gives more severe distortion in system current and voltage than a balanced fault.

(d) For a SLGF remote to the inverter commutating bus, from simulation graphs and Table 4.8, the following observations are made:

(1) Under the condition of GI in VG6P18 equals 25.0, GI in POLPI5 equals 5.88, GP in POLPI5 equals 0.15, the system can successfully recover from this kind of fault.

(2) Since the fault occurs remote to the inverter commutating bus, so the AC voltage at the inverter commutating bus doesn't drop to zero. This case is less severe than a SLGF at the inverter commutating bus. Fault recovery in this case is also faster.

(e) For a 3LGF remote to the inverter commutating bus, from simulation graphs and Table 4.8, the following observations are made:

(1) Under the condition of GI in VG6P18 equals 35.0, GI in POLPI5 equals 2.0, GP in POLPI5 equals 0.015, the system can successfully recover from this kind of fault.

(2) Comparing with (d) (which is simulated for 2.0 second) and (e) (which is simulated for 1.0 second), it can be seen it is easier to recover from a balanced fault than an unbalanced fault. In a balanced fault, there is only the positive sequence existing; while in an unbalanced fault, the negative sequence and the zero sequence also exist. This makes an unbalanced fault much more complicated than a balanced fault.

(f) For single phase AC source loss fault in the inverter AC system, from simulation graphs and Table 4.8, the following observations are made:

(1) Under the condition of GI in VG6P18 equals 15.0, GI in POLPI5 equals 5.88, GP in POLPI5 equals 0.15, the system can successfully recover from this kind of fault.

(2) During fault period, AC voltage at the commutating bus has a slightly drop. This case is not as severe as SLGF at the inverter commutating bus.

(3) Since this fault occurs far away from the inverter commutating bus, the commutation failure may not occur. Usually, when the inverter commutating voltage drops to 44.0%, the commutating failure becomes unavoidable. In this fault case, the AC voltage

at the commutating bus is higher than 0.5 P.U.

(g) For the 3 phase AC source loss fault in the inverter AC system, from simulation graphs and Table 4.8, the following observations are given:

(1) Under the condition of GI in VG6P18 equals 15.0, GI in POLPI5 equals 2.88, GP in POLPI5 equals 0.15, the system can successfully recover from this kind of fault.

(2) Since all the AC sources are lost during fault period, the AC voltage at the inverter commutating bus drops to zero. Because of the energy release from capacitors or inductors, the AC voltage at the inverter commutating bus is not constant zero. But the voltage swing from zero is very slight, so this case is quite similar with 3LGF at the inverter commutating bus (see (c)). Compared with the single phase AC source loss fault, this fault is worse both in fault period and in fault recovery period.

(h) For the inverter end DC fault, from simulation graphs and Table 4.8, the following observations are given:

(1) Under the condition of GI in VG6P18 equals 35.0, GI in POLPI5 equals 2.0, GP in POLPI5 equals 0.15, the system can successfully recover from this kind of fault.

(2) The inverter end DC fault doesn't affect the inverter commutating voltage much. Because of DC voltage drops to zero during fault period, the DC power also drops to zero. Total transmission energy is lost during the fault.

(3) This kind of fault can recover very easily. After fault clearance, DC voltage returns smoothly to steady state. No overvoltage is produced in this period. The system suffers from overcurrent during the fault period.

Note that associated with GP in POLPI5 equal to 0.15, the DC voltage has much more oscillation than when GP in POLPI5 equals 0.015. Because of the larger proportional gain of the former case, DC voltage is more prone to oscillate than the latter case. Due to the function of the smoothing inductor, the oscillations do not reflect in the DC current.

The conclusion is: With the original filter group, for light load case, the system can successfully escape from the ferro-resonance in various AC & DC faults.

(2) With new filters (include 2nd harmonic filter, the total rating is 217.0 MVAR)

Table 4.9 is a summary of inverter DC control parameters corresponding to the disturbance in the light load case with new filters. The table also gives the time to get the system steady state. In this table, only the integral gain in the inverter extinction angle controller is changed. The other DC control parameters are kept constant (the integral gain and the proportional gain in the inverter DC current controller are 2.0 and 0.15, respectively).

(a) For DC system start up, from Fig. 4.28 and Table 4.9, the following observations are made:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 25.0, the system can start up successfully.

(2) As the same as in Fig. 4.26, the DC system is deblocked at Time=0.1 second, then DC current order is given as a step function. At Time=1.0 second the system starts up. The whole process lasts 0.9 second, while in Fig. 4.26, the system start up process only lasts 0.7 second. So the original filter group with a large filter rating can speed up the start up process.

(b) For SLGF at the inverter commutating bus, from Fig. 4.29 and Table 4.9, the following observations are given:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 35.0, the system can successfully recover from this kind of fault.

(2) In this case, the fault is simulated for 2.0 second. Comparing with Fig. 4.27 which is simulated for only 1.0 second, it can be seen that the original filter group shows a better recovery property than the new filter group in this fault. There is a hint that the smaller GP in POLPI5 assists in the original filter case. With the same GP in POLPI5 (0.15), the original filter case can't recover from this fault.

(c) For 3LGF at the inverter commutating bus, from simulation graphs and Table 4.9, the following observations are made:

(1) Under the condition of the integral gain in the inverter extinction angle controller

equals 35.0, the system can successfully recover from this kind of fault.

(2) In this case, the fault is simulated for 2.0 second. Comparing with the original filter group case which is simulated for only 1.0 second, it can be seen that the original filter group shows a better recovery property than the new filter group.

(3) Comparing SLGF and 3LGF at the inverter commutating bus with the new filter group,there is no significant difference in fault recovery time. But with the original filter group, 3LGF is a smoother recovery than SLGF

(d) For SLGF near the inverter commutating bus, from simulation graphs and Table 4.9, the following observations are made:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 35.0, the system can successfully recover from this kind of fault.

(2) The recovery time is almost the same as with the original filter group case.

(e) For 3LGF near the inverter commutating bus, from simulation graphs and Table 4.9, the following observations are given:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 15.0, the system can successfully recover from this kind of fault.

(2) The fault is simulated for 1.0 second. Compare with the original filter group case, the fault recovery time is almost the same.

(f) For single phase AC source loss fault in the inverter system, from simulation graphs and Table 4.9, the following observations are made:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 15.0, the system can successfully recover from this kind of fault.

(2) Comparing with the original filter group case, it can be seen that the new filter group case can speed up the fault recovery process.

(g) For the 3 phase AC source loss fault in the inverter AC system, from simulation graphs and Table 4.9, the following observations are given:

(1) Under the condition of the integral gain in the inverter extinction angle controller

equals 5.0, the system can successfully recover from this kind of fault.

(2) The fault recovery process is quite similar with the original filter group case. The DC voltage shows a smoothing characteristic in the recovery period.

(h) For the inverter end DC fault, from simulation graphs and Table 4.9, the following observations are made:

(1) Under the condition of the integral gain in the inverter extinction angle controller equals 35.0, the system can successfully recover from this kind of fault.

(2) The fault recovery process is a little worse than with the original filter group case. There is still no overvoltage produced in this case. But the system suffers from the overcurrent during the fault period.

Note that with the new filter group, the DC control parameters can remain relatively consistent through various faults. With the original filter group, three DC control parameters (i.e., GI in VG6P18 at the inverter; GI and GP in POLPI5 at the rectifier) must be adjusted for recovery from different disturbances. But with the new filter group, only one control parameter's change (i.e., GI in VG6P18 at the inverter) satisfies the fault recovery requirement. So the new filter group is more robust than the original filter group in fault recovery process.

The conclusion is: With the new filter group, the system can successfully recover from the ferro-resonance instigated by various AC & DC faults. Although the original filter group with adopted control gains shows a better recovery property in both SLGF and 3LGF at the inverter commutating bus, controls with the new filter group are more robust for various disturbances.

2. The full load case (1.0 P.U. DC current)

(1) With original filters (include 2nd harmonic filter, the total rating is 317.0 MVAR)

Table 4.10 is a summary of inverter DC control parameters corresponding to the disturbance in the full load case with original filters. The table also gives the time to get the system steady state. In this table, three DC control parameters (i.e., GI in VG6P18 at the

inverter; GI and GP in POLPI5 at the rectifier) are changed.

Various fault cases have been tested. The typical graphs are shown below:

Fig. 4.30--DC voltage in the system start up process with the original filter group (full load Id=1.0 P.U. case).

Fig. 4.31--DC voltage in the SLGF fault at the inverter commutating bus with the original filter group (full load Id=1.0 P.U. case).

The conclusion is: With the original filter group, for full load case, the system can successfully recover from the ferro-resonance in various AC & DC faults.

Table 4.11 is a summary of inverter DC control parameters corresponding to the disturbance in the full load case with new filters. The table also gives the time to get the system steady state. In this table, only the integral gain in the inverter extinction angle controller is changed. The other DC control parameters keep constant (the integral gain and the proportional gain in the inverter DC current controller are 2.0 and 0.15 respectively).

The typical tests are showing below:

Fig. 4.32--DC voltage in the system start up process with the new filter group (full load Id=1.0 P.U. case).

Fig. 4.33--DC voltage in the SLGF fault at the inverter commutating bus with the new filter group (full load Id=1.0 P.U. case).

The conclusion is: With the new filter group, the system can successfully recover from the ferro-resonance resulting from AC & DC faults which occur at full load steady state operation. Only one inverter DC control parameter need be adjusted for various faults to satisfy the fault recovery requirement with new filters, while 3 inverter DC control parameters have to be adjusted with the original filter in service. That means the new filter group is more robust than the original filter group for various AC and DC disturbances

Both filter groups can eliminate the ferro-resonance in various AC & DC fault recovery processes, because they both include the same 2nd harmonic filter. Although the capacity of the new filter group is only a half of the original filter group, the fault recovery of the DC system with the smaller capacity filters is superior.

From the summarized tables of different simulation cases, it is obvious that DC control parameters play a key role in each disturbance. So looking for optimal DC control parameters become an consideration.

The previous simulations are made from a rough optimization of DC control parameters (i.e., re-run one case many times with different DC control parameters, then choose the best ones). Can we use a computer optimization program to look for the exact optimized parameters? The EMTDC's utility program EMTMR supplies a useful tool to help determine optimum settings of control parameters.

Table 4.8 Light load case with original filters

Cases / Fig. / Subroutines	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLGF near Comm. Bus	3LGF near Comm. Bus	Single Phase Source Loss	3 Phase Source Loss	DC Fault
GI in VG6P18	35.0	75.0	55.0	25.0	35.0	15.0	15.0	35.0
GI in POLPI5	2.0	2.0	2.0	5.88	2.0	5.88	2.88	2.0
GP in POLPI5	0.15	0.015	0.015	0.15	0.015	0.15	0.15	0.15
Time to get steady state (second)	0.50	0.60	0.55	0.70	0.69	0.49	0.45	0.14

Table 4.9 Light load case with new filters

Cases / Fig. / Subroutines	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLGF near Comm. Bus	3LGF near Comm. Bus	Single Phase Source Loss	3 Phase Source Loss	DC Fault
GI in VG6P18	25.0	35.0	35.0	35.0	15.0	15.0	5.0	35.0
GI in POLPI5	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
GP in POLPI5	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
Time to get steady state (second)	0.70	0.65	0.68	0.70	0.60	0.40	0.35	0.39

Note: GI--Integral gain
GP--Proportional gain
VG6P18--Inverter extinction angle controller
POLPI5--Rectifier DC current controller

Table 4.10 Full load case with original filters

Cases / Fig. / Subroutines	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLGF near Comm. Bus	3LGF near Comm. Bus	Single Phase Source Loss	3 Phase Source Loss	DC Fault
GI in VG6P18	35.0	25.0	35.0	25.0	35.0	35.0	35.0	35.0
GI in POLPI5	2.0	2.0	2.0	2.0	2.0	7.88	2.0	2.0
GP in POLPI5	0.15	0.15	0.015	0.15	0.15	0.15	0.15	0.15
Time to get steady state (second)	0.70	0.45	0.65	0.55	0.75	0.50	0.80	0.40

Table 4.11 Full load case with new filters

Cases / Fig. / Subroutines	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLGF near Comm. Bus	3LGF near Comm. Bus	Single Phase Source Loss	3 Phase Source Loss	DC Fault
GI in VG6P18	25.0	45.0	25.0	35.0	35.0	25.0	35.0	55.0
GI in POLPI5	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
GP in POLPI5	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
Time to get steady state (second)	0.55	0.45	0.90	0.70	0.55	0.35	0.60	0.65

Note: GI--Integral gain
GP--Proportional gain
VG6P18--Inverter extinction angle controller
POLPI5--Rectifier DC current controller

Fig. 4.26--4.29 Some Tests With Light Load Case (Id=0.3 P.U.)

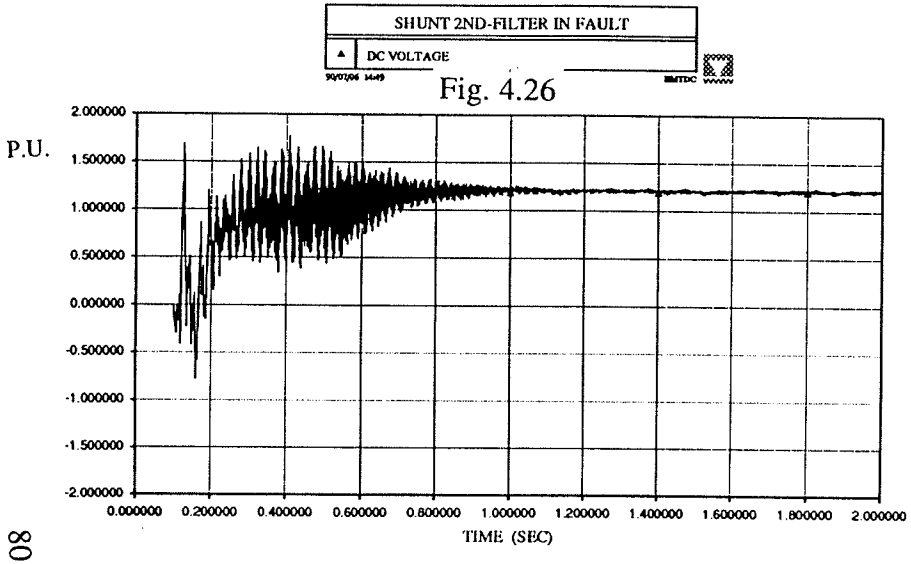


Fig. 4.26

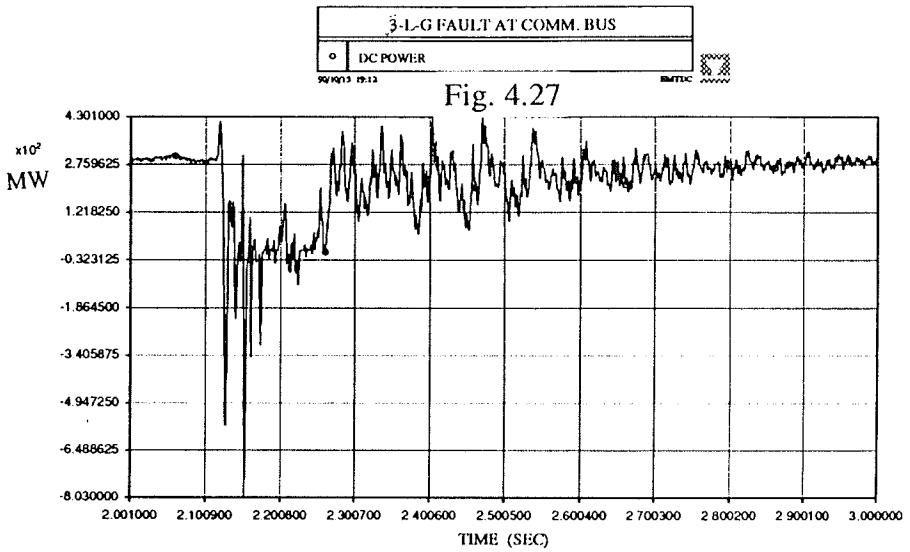


Fig. 4.27

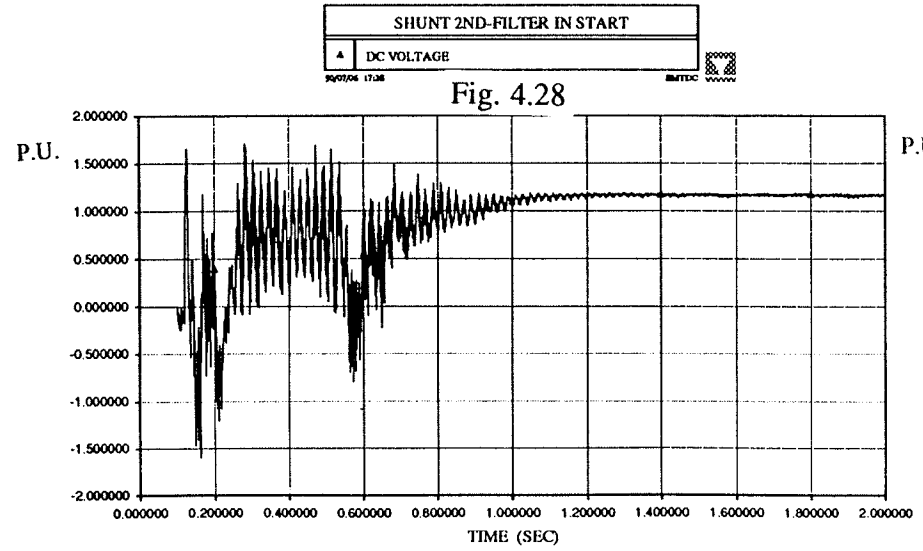


Fig. 4.28

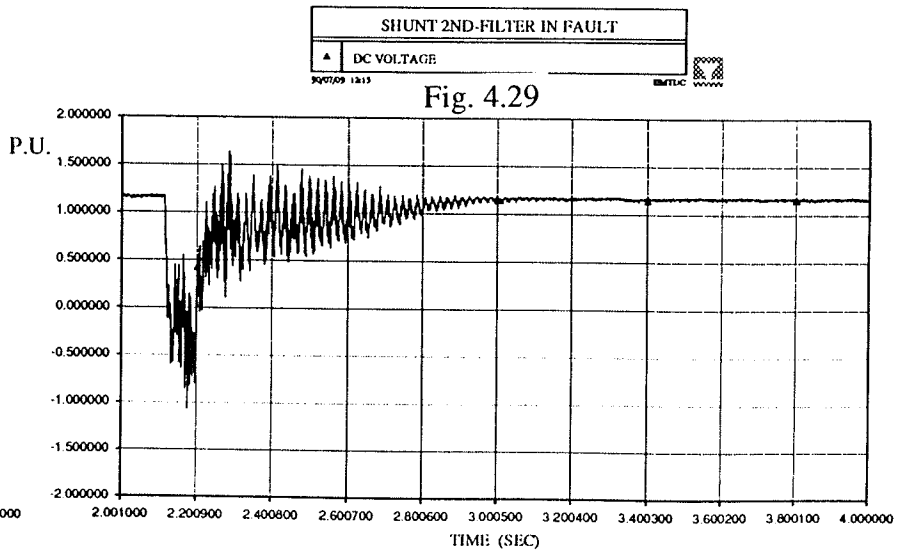


Fig. 4.29

Fig. 4.30--4.33 Some Tests With Full Load Case (Id=1.0 P.U.)

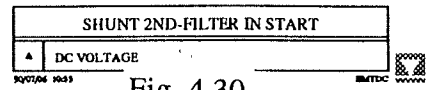
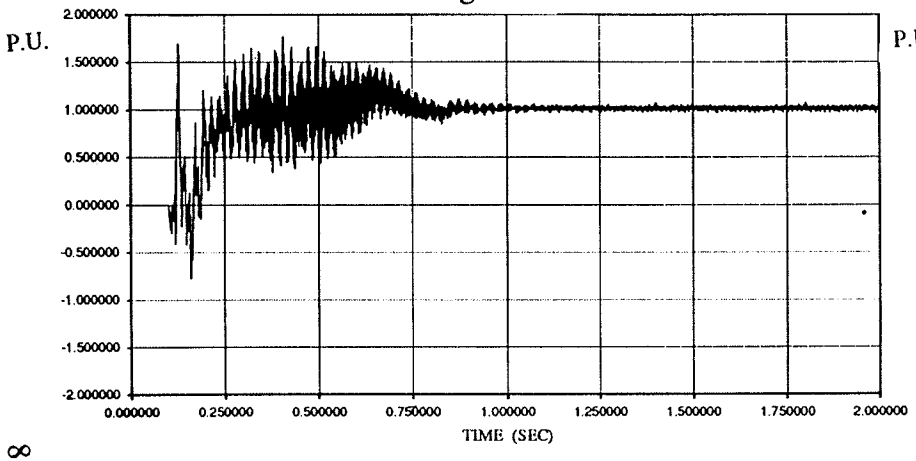


Fig. 4.30



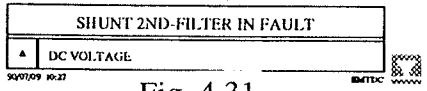
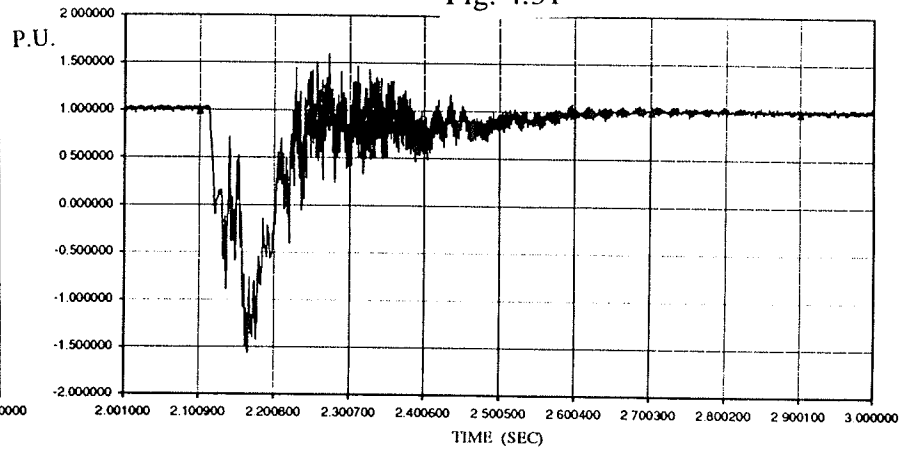


Fig. 4.31



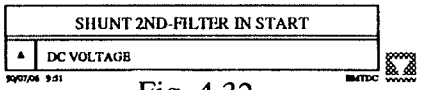
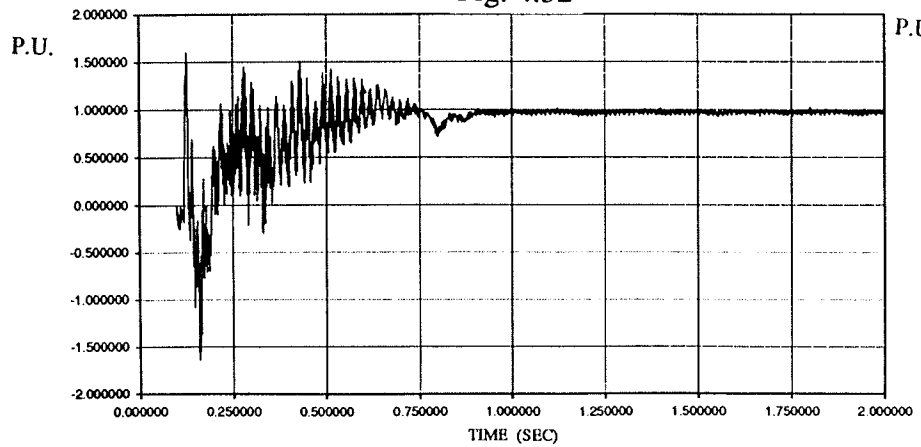


Fig. 4.32



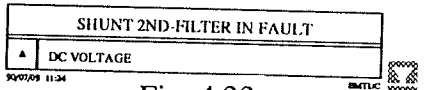
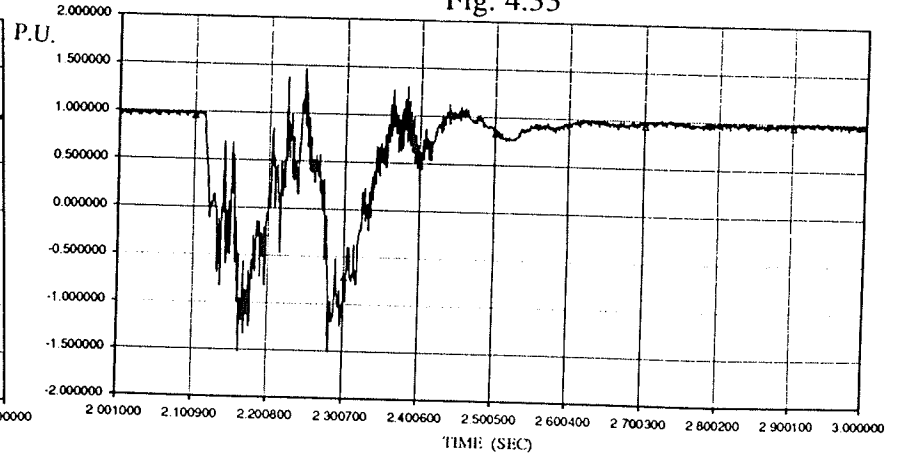


Fig. 4.33



4.2.3 Adaptive Gain Control

In a DC control system, the PI (proportional and integral) controller is the most popular. There are two control parameters in each PI controller: One is the proportional gain GP, the other is the integral gain GI. The purpose of the adaptive gain control is to choose the optimal GP and GI values for each PI controller according to the system structure and the type of the disturbance. In our simulation system, three PI controllers are used: the extinction angle controller at the inverter and the DC current controllers at both the inverter and rectifier. So there are totally six control parameters need to be optimized.

In general, the methods of adaptive control are divided into two cases:

(1) Using an on-line optimal parameter program

When the system disturbance occurs (which may include the HVDC system start and different kinds of AC/DC faults), the optimal control parameter program begins to run immediately. According to the objective function, it looks for the optimal control parameters. Because this process usually takes a long time and the control parameters change within a large range before they reach the optimal setting, this will difficult to achieve in the real power system.

(2) Using off-line optimal parameter program

When the system disturbance occurs, the disturbance detector is used to recognize the type of the disturbance. The computer then chooses suitable control parameters according to the optimal parameter table which is deposited in computer by off-line computation.

The diagram of the adaptive gain control is as follows:

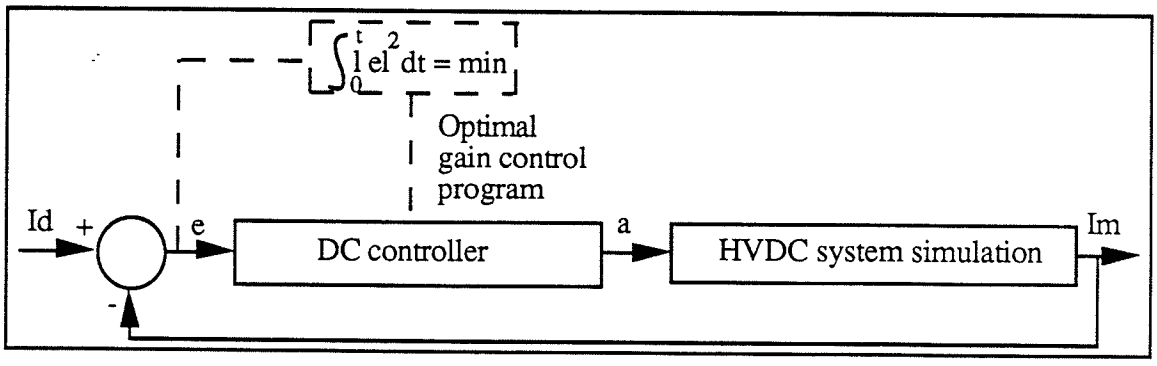


Fig. 4.34 The diagram of adaptive gain control

In Fig. 4.34, **Id** means the DC current order, **Im** means the measured DC current. **a** is the firing angle order which output from the DC controller. **e** is the error between **Id** and **Im.** The objective function is the minimum of the sum of the error's square, i.e., e^2. To minimize this, the optimal control parameters are selected. The dashed line means the optimal control parameter program is separated with the main simulation program.

The objective function $\int_0^t |e|^2 dt$ is calculated using an integral function available in EMTDC. The block diagram is shown in Fig. 4.35.

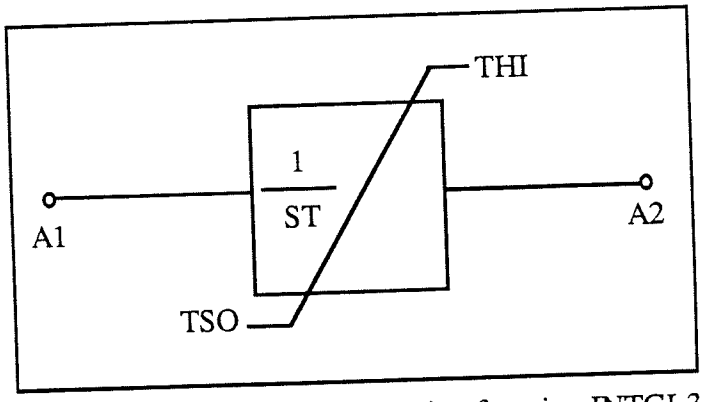


Fig. 4.35 Block diagram describing function INTGL3

In Fig. 4.35, **A1** is the input, i.e., the square of the DC current error e^2. **A2** is the output, i.e., the objective function. **T** is the integral time constant which can speed or slowly the integration output. It is chosen as 1.0 second in this case. Note that the definition of the integral time constant **T** is the inverse of the integral gain **GI** in proportional-integral controller, i.e., **T = 1/GI. THI** and **TLO** are the high limit and low limit respectively. Because we don't want the application of limits to affect the response of the input **A1**, so **THI** is given as **999.0**, while **TLO** is given as **-999.0**.

Of the two kinds of methods for adaptive control, the off-line optimal parameter program is the more popular method. It can avoid the disturbance which may be caused by the parameter optimization process. On the other hand, it can save time in a real time simulation.

The key for the adaptive gain control is to set up a detector which can recognized the various AC & DC disturbances. A diagram of such a subroutine known as **DETECTOR** is shown in Fig. 4.36.

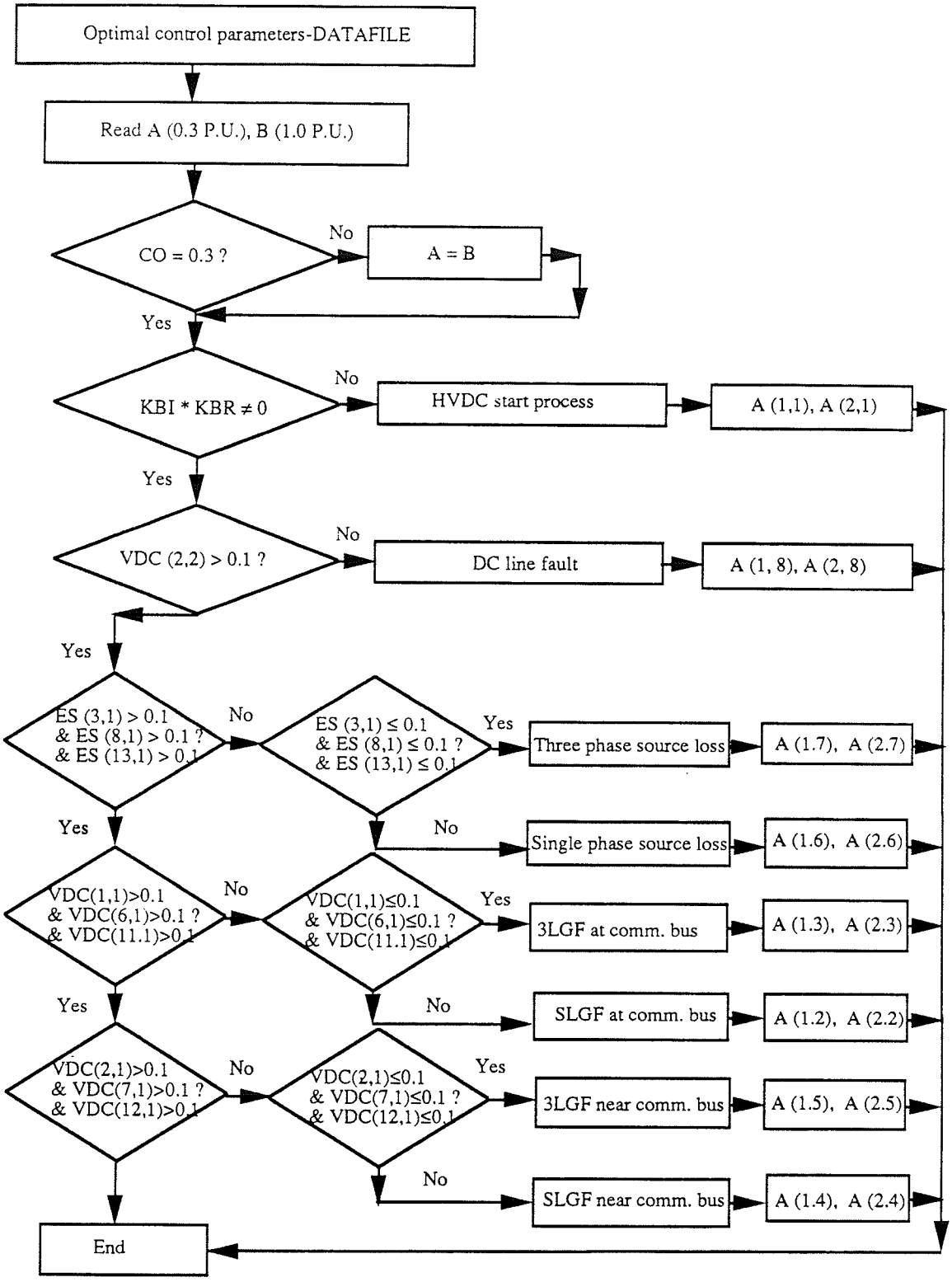


Fig. 4.36 The diagram of the subroutine DETECTOR

Note that the DETECTOR must provide:

(1) The ability to recognize different starting cases and different fault cases correctly and rapidly.

(2) The optimal control parameter table must be available for all the types of disturbances which may happen in the system. The parameters must be optimal for each disturbance.

(3) The DETECTOR must recognize the difference between a fault disturbance, a start disturbance and an adjustment disturbance (i.e., these disturbances are caused by the DC control system's adjustment, not by another fault. The DETECTOR should recognize this.)

The DETECTOR which is shown in Fig. 4.36 is only a preliminary one. It doesn't include every fault case which may happen in the system. The fault cases considered in Fig. 4.36 are only typical ones matched with the fault tests in the previous section. The detector in Fig. 4.36 only demonstrates an idea for the adaptive gain control. Further work is needed to perfect the optimal control parameter table DATAFILE.Sometimes the fault will not be as severe as a line to ground fault, so the voltage will not drop to zero. This also is need to be considered in the fault recognition.

In Fig. 4.36, the rms (root mean square) value of the voltage is measured using a metering function RMS3 available in EMTDC. This function RMS3 calculates the rms value of any single variable using an approximation of the expression:

$$\sqrt{1/T\int_0^T X^2 dt} \qquad \text{.....(4.15)}$$

Where T = specified period of time
X = input variable

Using the DETECTOR, the computer can select the suitable control parameters from the optimal parameter table corresponding to the fault case automatically. Now how to establish this table needs to be considered.

To establish the optimal parameter table, a utility program called EMTMR can be used. EMTMR is the EMTDC Multiple Run Analysis Program. It can be used both for single variable and two variables. For single and two variable control parameters, multiple run capability on EMTDC can be undertaken with sequential or random variation of the control parameters to search for optimum settings.

In the HVDC simulation system, there are six control parameters:

Invertor: GI (= A1) and GP (= A2) in the valve group controls VG6P18; GI (= A3) and GP (= A4) in the pole current controls POLPI5.

Rectifier: GI (= A5) and GP (= A6) in the pole current controls POLPI5.

Now we want to optimize them, and then get the optimal control parameter group.

The optimization process is as follows:

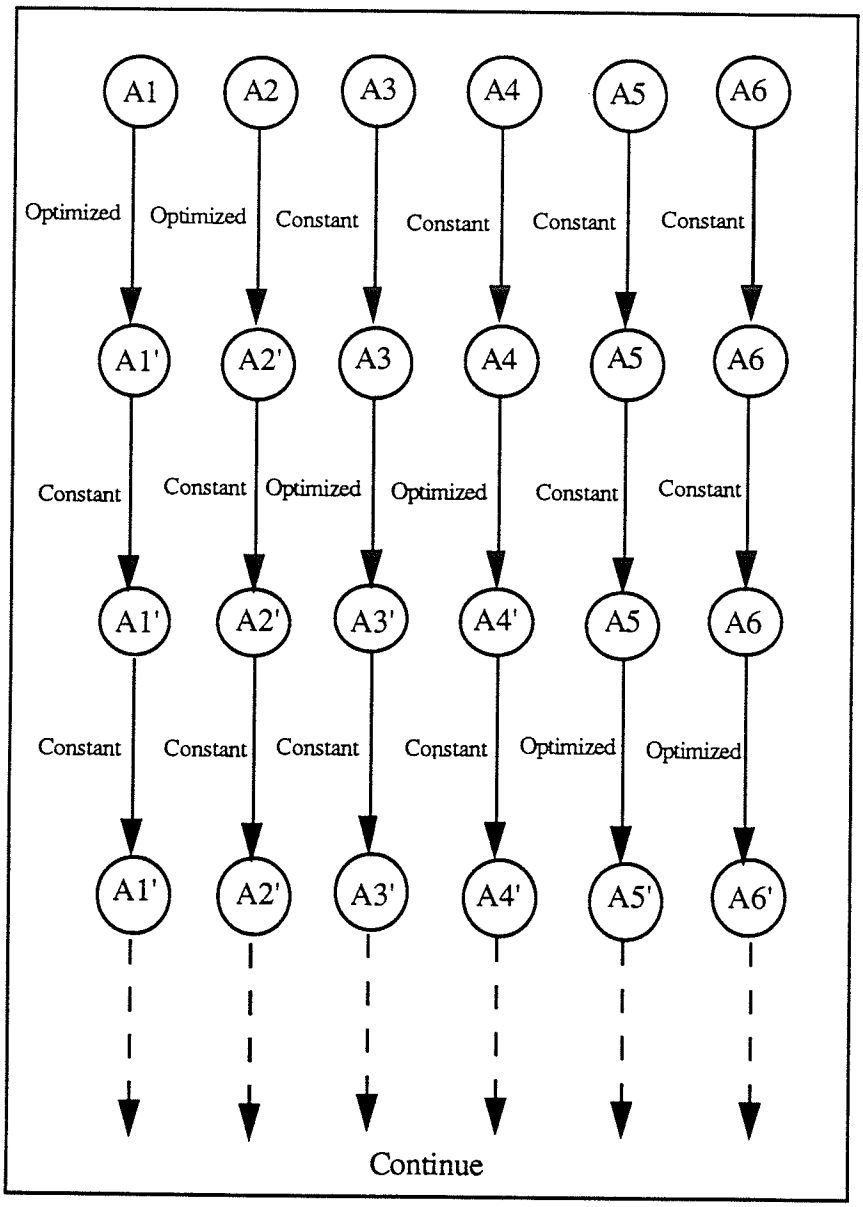


Fig. 4.37 The optimization process

This process continues until six constants get their final optimal values.

The objective function of this optimization is the minimum value of integration of the current error's square which was mentioned before.

Table 4.12 also gives the time to get the system steady state and the figure number corresponding to each simulation case.

The following cases are simulated:

(1) Light load (0.3 P.U. DC current) and full load (1.0 P.U. DC current) HVDC system start up with original filters, no 2nd harmonic filter (Fig. 4.39). The ferro-resonance exists in both cases and the HVDC system is incapable of starting as a consequence.

(2) Light load HVDC system start up with new filters, the 2nd harmonic filter, transformer saturation and without optimal control parameters (Fig. 4.40). This is a basis for comparison.

(3) Light load HVDC system start up with new filters, the 2nd harmonic filter, transformer saturation and with the optimal control parameters (Fig. 4.41). In Fig. 4.40, at T = 0.8 second, the system reaches steady state, and the whole start-up process lasts 0.7 second. while In Fig. 4.41 with optimum control parameters, at T = 0.25 second, the system reaches steady state, and the whole start-up process only lasts 0.15 second. Comparing Fig. 4.40 and Fig. 4.41, it can be seen that the optimal control parameters can speed up the system starting process significantly.

(4) Light load HVDC system start with original filters, no 2nd harmonic filter, without the transformer saturation, with the optimal control parameters (Fig. 4.42). Because the transformer saturation isn't considered, so there is no ferro-resonance produced in this case. With the optimal control parameters, the system gives a good start-up characteristic.

(5) Light load HVDC system start with the original filter group, no 2nd harmonic filter, with the transformer saturation and the optimal control parameters (Fig. 4.43). Note that even without the 2nd harmonic filter, the ferro-resonance can be suppressed. This is a good example where optimal control parameters can overcome the ferro-resonance.

(6) Full load HVDC system start with the original filter group, no 2nd harmonic filter, without the transformer saturation and with the optimal control parameters (Fig. 4.44). Because there is no transformer saturation, ferro-resonance is not present in this case.

(7) Full load HVDC system start with the original filter group, no 2nd harmonic filter, with the transformer saturation and with the optimal control parameters (Fig. 4.45). The system starting process is as good as in Fig. 4.44. This is an another example where use of optimal control parameters overcomes the ferro-resonance phenomenon.

(8) Light load SLGF near the inverter commutating bus with the original filter group, no 2nd harmonic filter, with the transformer saturation and with the optimal control parameters (Fig. 4.46). From the simulation results, it can be seen that optimal control parameters can also help the system recover from the ferro-resonance in the fault case.

From the above analysis, it can be seen that the DC control parameters of both the inverter side and the rectifier side play a key role in HVDC system starting process and in the fault recovery process.

For each optimization process, we use the same symbols as before:

A1: the integral gain of the inverter extinction angle controller;

A2: the proportional gain in the inverter extinction angle controller;

A3: the integral gain in the inverter DC current controller;

A4: the proportional gain in the inverter DC current controller;

A5: the integral gain in the rectifier DC current controller;

A6: the proportional gain in the rectifier DC current controller.

The general optimization process has already been shown in Fig. 4.35. As the convergence condition, we define the optimization process will stop if the next optimization step gives a larger objective function than the previous one. Sometimes, we can use

$\int_0^t e^2 dt < £$ .....(4.16) where £ is a value according to the requirement of the accuracy as the convergence condition.

Because the highly non-linear nature of the model makes it difficult to reach the convergence condition, every optimization process takes a long time.

Now to look at a optimization process (Fig. 4.38). This is the first optimization step in light load HVDC system start up process with new filters, 2nd harmonic filter, transformer saturation. The most optimum value is designated by "S". The best 10% of optimum is designated by a "1", the next best 10% by a "2", etc. The largest output is defined by "B".

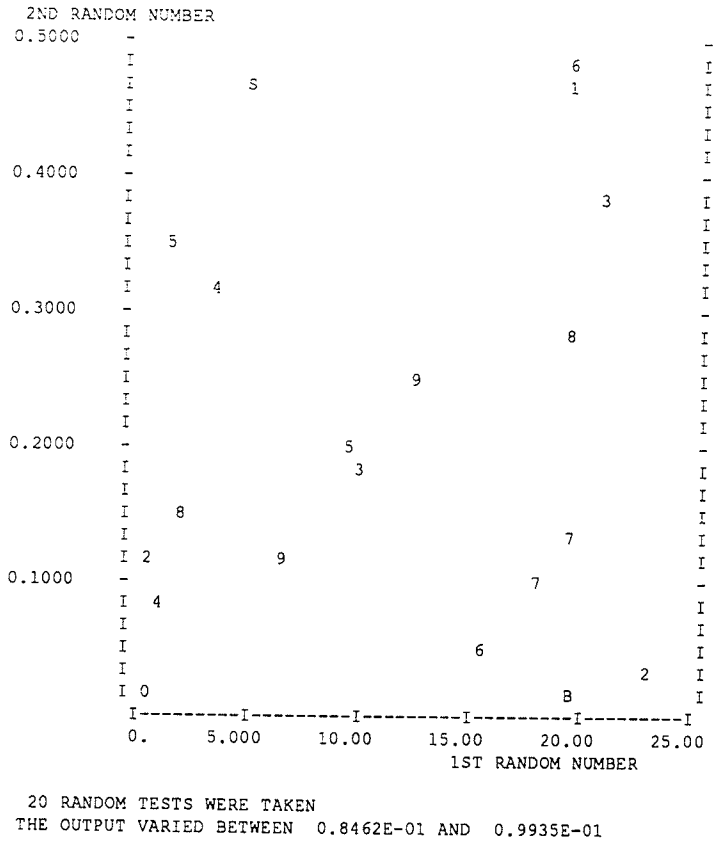


Fig. 4.38 An Optimization Process where A1, A2 are optimized as 5.75 and 0.475 (A3=2.0, A4=0.015, A5=5.88,and A6=0.0136 are constants)

Fig. 4.12 gives all the optimal control parameters corresponding to various system conditions.

The optimization process is undertaken on a SUN Workstation. Every optimization step includes 20 multiple runs and can only determine two optimal parameters. Every optimization process include several optimization steps, taking approximately 3 hours or more for one step. If one case includes 6 steps, then it needed 18 hours to finish each case. The control parameters' optimization process is a time-consuming work. From this, it can be seen that off-line optimization is an reasonable method.

The adaptive gain control is designed in this chapter. The principle of the adaptive gain control uses DETECTOR to detect a fault. According to the fault case, compile the optimal control parameters into a table which is deposited in the computer. EMTMR supplies a good tool to compose the optimal control parameter table. However, this is a time-consuming work.

The optimal control parameters did influence the system start up process and fault recovery process. An amazing observation is: in some cases, even without the 2nd harmonic filter and only with the optimal control parameters, the ferro-resonance can be eliminated completely. This suggests doing something with DC controls to dampen ferro-resonance oscillations.

Table 4.12 Some Tests With Optimal Control Parameters

Cases / Fig. / Subroutines	Light load & full load start with original control parameters (Ferro-resonance exists)	Light load start with new filters (with saturation; with 2nd filter; no optimization)	Light load start with new filters (with saturation; with 2nd filter; with optimization)	Light load start with original filters (no saturation; no 2nd filter; with optimization)	Light load start with original filters (with saturation; no 2nd filter; with optimization)	Full load start with original filters (no saturation; no 2nd filter; with optimization)	Full load start with original filters (with saturation; no 2nd filter; with optimization)	Light load SLG remote fault with original filters (with saturation; no 2nd filter; with optimization)
VG6P18 GI (INV)	15.0	25.0	20.0	20.4	21.4	15.6	7.92	0.96
VG6P18 GP (INV)	0.3	0.3	0.55	0.295	0.435	0.315	0.405	0.0984
POLPI5 GI (INV)	2.0	2.0	1.45	4.64	4.35	7.0	7.0	4.35
POLPI5 GP (INV)	0.15	0.15	0.042	0.0295	0.0385	0.01504	0.01504	0.0385
POLPI5 GI (REC)	5.88	5.88	8.2	8.2	8.2	2.07	2.07	7.5
POLPI5 GP (REC)	0.0136	0.0136	0.0295	0.0295	0.0295	0.0595	0.0595	0.0425
Fig.	Fig. 4.39	Fig. 4.40	Fig. 4.41	Fig. 4.42	Fig. 4.43	Fig. 4.44	Fig. 4.45	Fig. 4.46
Time to get steady state (Second)	——	0.70	0.15	0.12	0.13	0.45	0.30	0.25

Fig. 4.39--4.42 Some Tests With Optimal Control Parameters

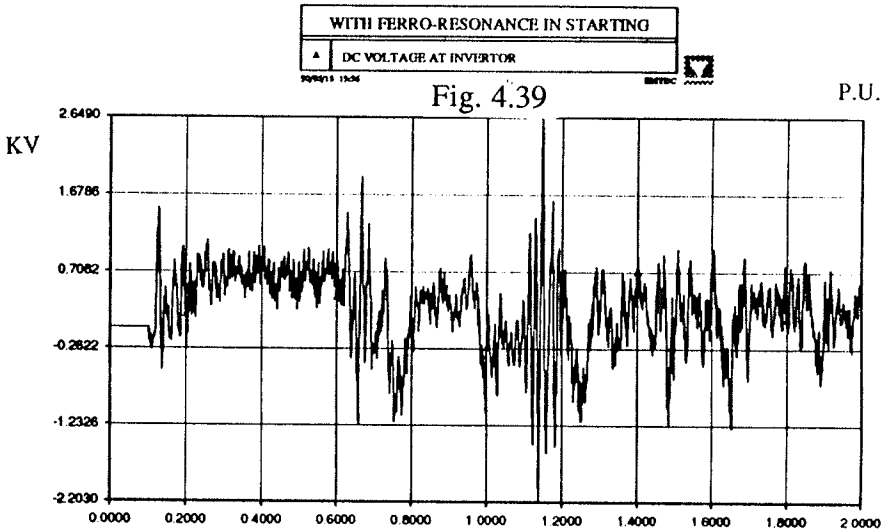


Fig. 4.39

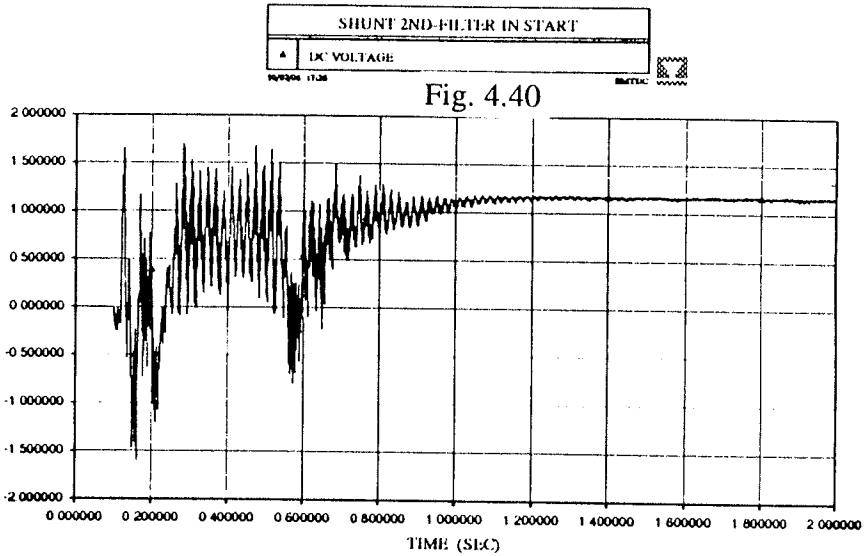


Fig. 4.40

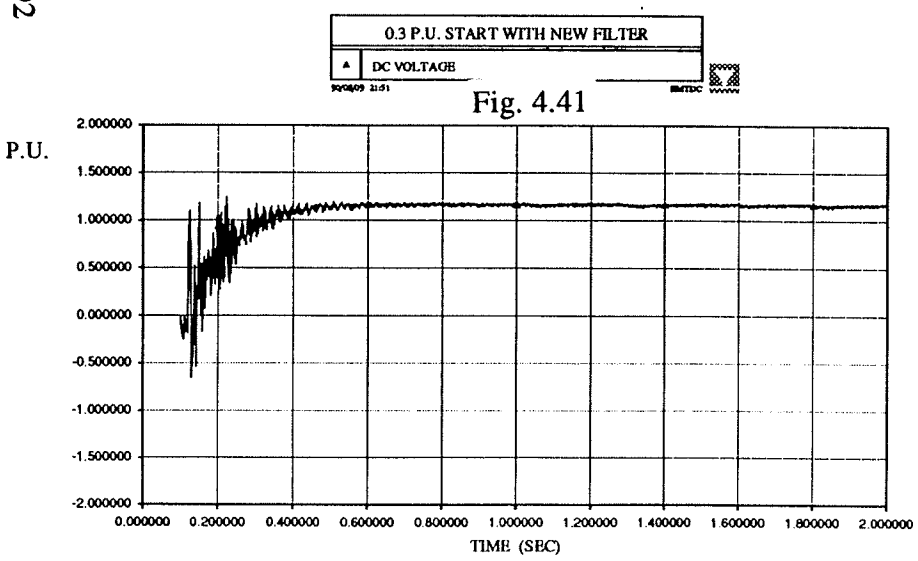


Fig. 4.41

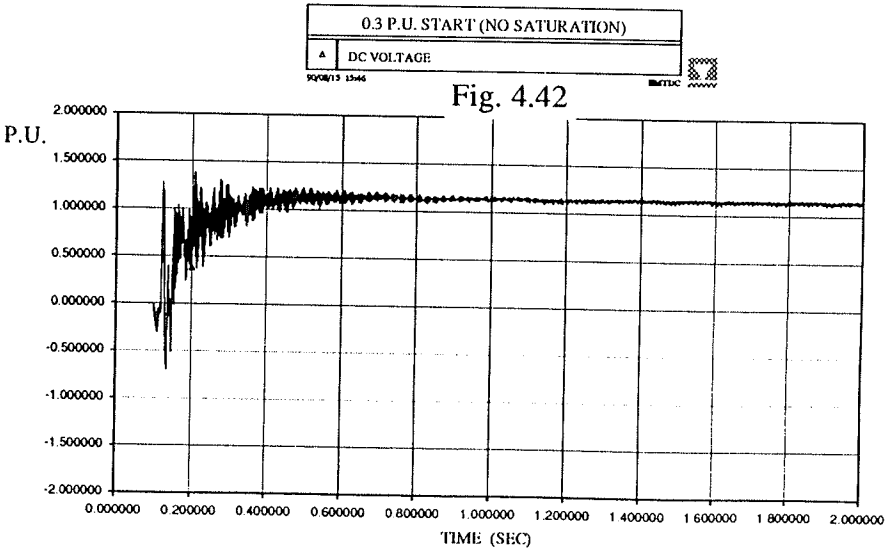


Fig. 4.42

Fig. 4.43--4.46 Some Tests With Optimal Control Parameters

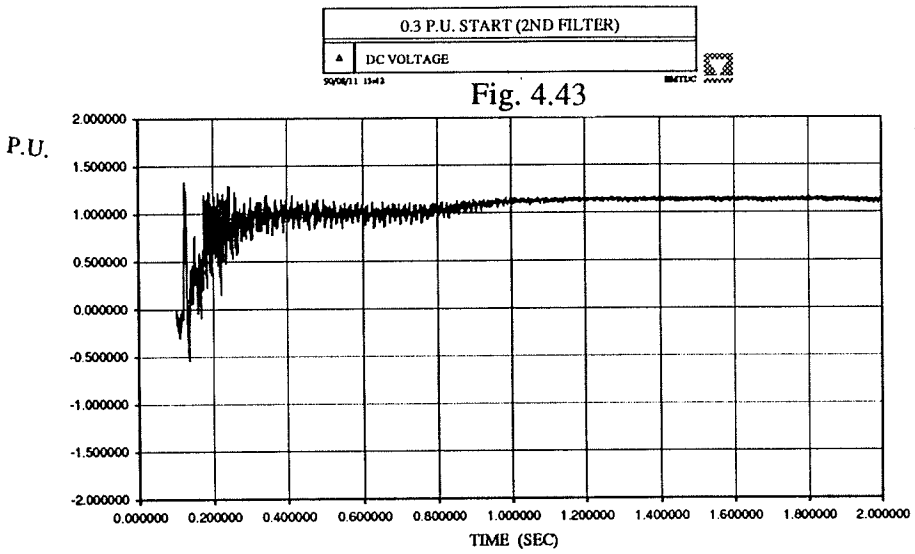


Fig. 4.43

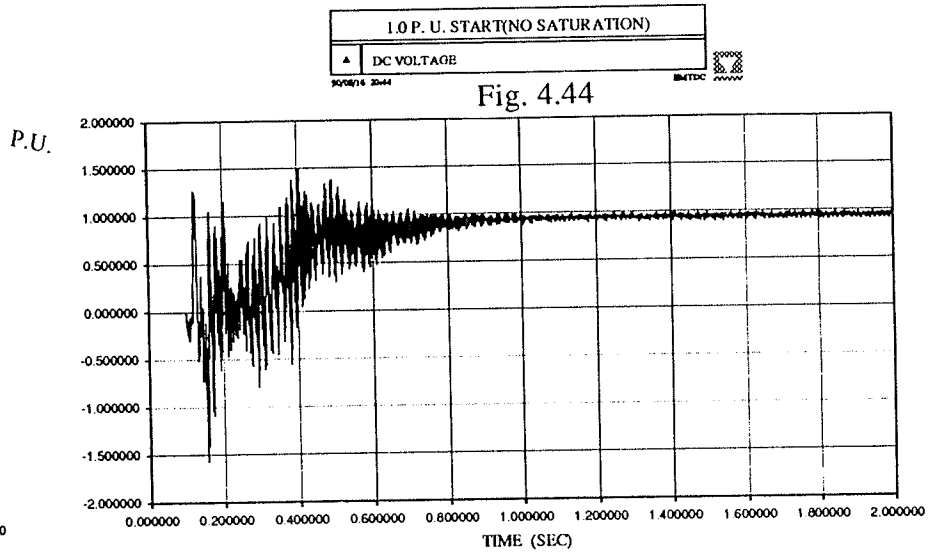


Fig. 4.44

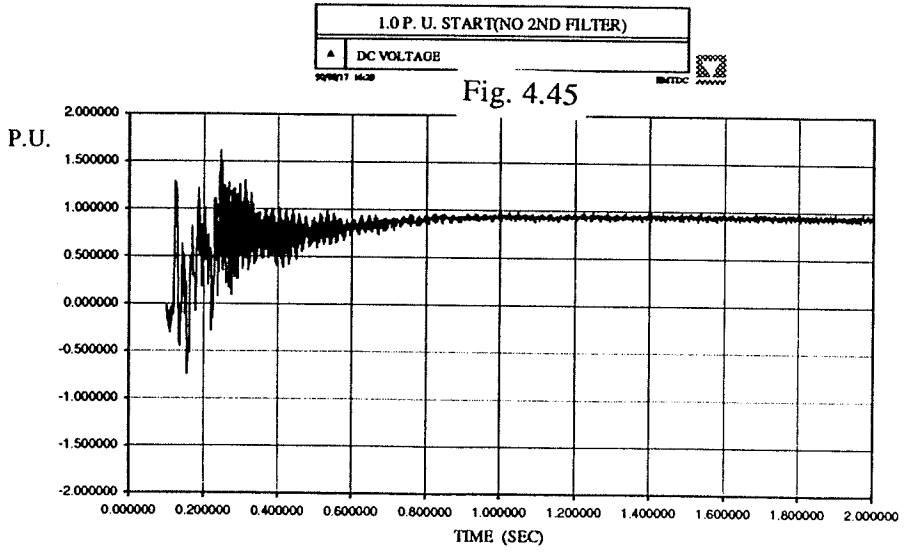


Fig. 4.45

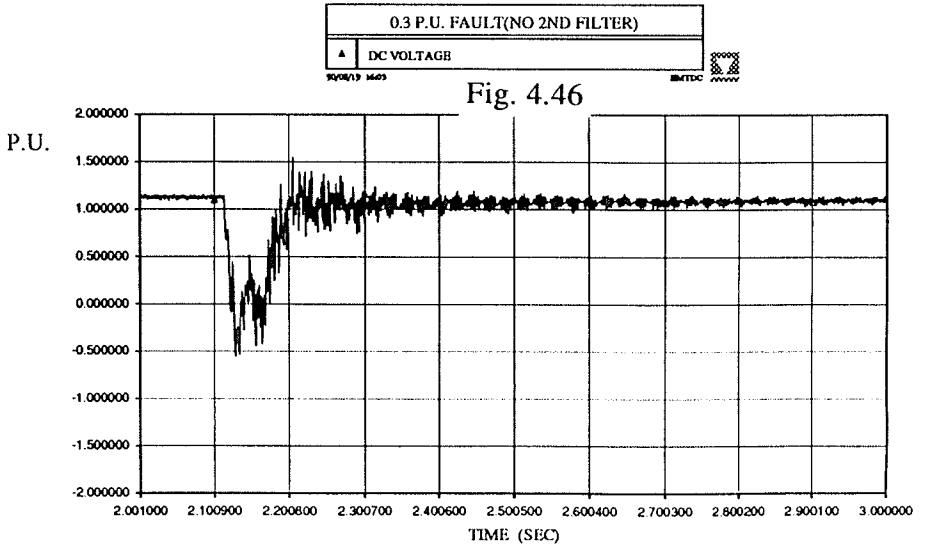


Fig. 4.46

From single phase tests (Chapter 3), we have already shown that the R + SWITCH method, the thyristor controlled resistor method, and the fundamental blocking filter method can eliminate ferro-resonance in a single phase circuit. Based on this encouraging result, tests are undertaken with these three methods in the three phase HVDC system. Because studying the HVDC system is our main objective, so the much more detailed tests are studied in this chapter than in the single phase system.

4.2.4. R + SWITCH

The diagram is the same as in Fig. 3.18.

In the start process, the switch is open T < 1.0 second. After the HVDC system finished the start up process, the switch is closed when T > 1.0 second. The simulation shows the HVDC system can successfully start up.

An AC system fault is applied between 2.115--2.169 second (3 1/4 cycles). The dissipation resistor can completely remove the subsynchronous energy. Then the switch opened again. The system can successfully recover from the AC fault (see Fig. 4.56).

4.2.5 Thyristor Controlled Resistor Method

The diagram is the same as in Fig. 3.19.

1. The firing angle a = 180^0

The same variables are recorded in each test as in the previous case.

Results from a SLGF near the inverter commutating bus is shown in Fig. 4.57.

The simulation results show that the HVDC system can successfully start up and recover from the AC fault. This method is a good solution for the ferro-resonance problem not only in the single phase system, but also in the HVDC system.

2. The firing angle a = 0^0

Detailed tests are given in this case. Because the thyristor can be easily destroyed by the excessive reverse voltage and the extended overcurrent, it is very important to know the dynamic overvoltage (DOV) across the thyristor and the dynamic overcurrent (DOC) through the thyristor for each disturbance case. Table 4.14 is a summary of such DOV and DOC corresponding to every fault case. The table also gives the time to reach the system steady state for each disturbance.

(a) For DC system start up process: At the system steady state, the rated AC voltage between the thyristor is ±44.26 KV, and the rated AC current through the thyristor is ±0.44 KA.

(b) For SLGF at the inverter commutating bus, see Fig. 4.58. The DOV is between +209.8 KV and -182.0 KV; while the DOC is between +1.09 KA and -0.46 KA. The system can successfully recover from this kind of fault.

(c) For 3LGF at the inverter commutating bus: The DOV is between +209.8 KV and -182.0 KV; while the DOC is between +1.09 KA and -0.48 KA. The system can successfully recover from this kind of fault.

(d) For SLGF near the inverter commutating bus: The DOV is between +121.9 KV and -221.4 KV; while the DOC is between +1.025 KA and -0.914 KA. The system can successfully recover from this kind of fault.

(e) For 3LGF near the inverter commutating fault: The DOV is between +97.2 KV and -109.7 KV; while the DOC is between +0.62 KA and -0.76 KA. The system can successfully recover from this kind of fault.

(f) For a single phase AC source loss fault at the inverter side: The DOV is between +119.6 KV and -50.7 KV; while the DOC is between +0.47 KA and -0.92 KA. The system can successfully recover from this kind of fault.

(g) For the three phase AC source loss fault at the inverter side: There is no DOV and DOC produced in this case. The AC voltage between the thyristor is changed between ±44.26 KV, and the AC current through the thyristor is changed between ±0.44 KA. The system can successfully recover from this kind of fault.

(h) For the DC line to ground fault at the inverter end: There is no DOV and DOC

produced in this case. The AC voltage between the thyristor is changed between ±44.26 KV, and the AC current through the thyristor is changed between ±0.44 KA.

From all the simulation cases, it can be see that with the thyristor controlled resistor method, there will be no problem for the system fault recovery. A surge arrestor can be used to limit voltage across the capacitor in some severe fault cases.

4.2.6 Fundamental Blocking Filter

The diagram is the same as in Fig. 3.21.

The fundamental blocking filter is designed to block the fundamental frequency and bypass harmonic frequencies. There are no fundamental frequency energy losses and the dissipation resistor Rdiss can absorb the harmonic energy.

Consider the variation of AC system frequency and the variation of filter inductance or capacitance (e.g., due to temperature), the filter is usually designed as a de-tuned filter. Selecting a suitable filter quality factor Q (Q depends on the filter resistor R, see Fig. 3.21) is a key in the filter design.

Simulation results show that the filter quality factor Q has an significant effect to the HVDC system's fault recovery process.

Several cases are compared in Table 4.13.

Table 4.13 The comparison of the filter quality factor Q

$Q = \infty$	$Q = 200$	$Q = 150$	$Q = 128$	$Q = 100$
$R = 0.0\ \Omega$	$R = 1.325\ \Omega$	$R = 1.77\ \Omega$	$R = 2.0\ \Omega$	$R = 2.65\ \Omega$
Fig. 4.48	Fig. 4.49	Fig. 4.50	Fig. 4.51	Fig. 4.52

Fig. 4.48 ($Q = \infty$) and Fig. 4.49 ($Q = 200$) show a better fault recovery waveform than

Fig. 4.50 (Q = 150), Fig. 4.51 (Q = 128) and Fig. 4.52 (Q = 100). The first three cases make little difference. It seems there will be no problem if Q = 150 is chosen.

Based on Q = 150, Table 4.15 is a summary of the fault cases corresponding to the figures. The dynamic overvoltage across the fundamental blocking filter and the dynamic overcurrent through the fundamental blocking filter are also given in this table.

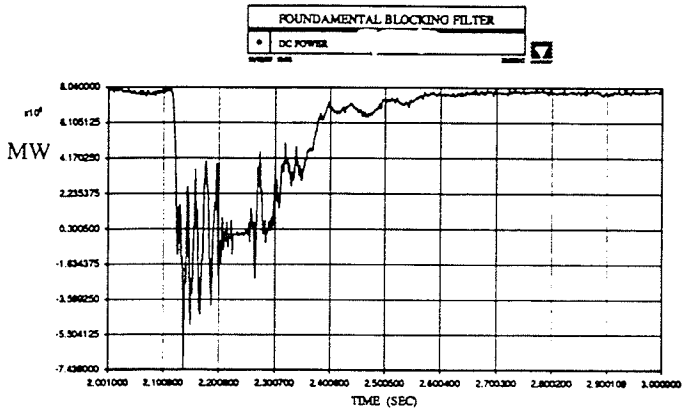


Fig. 4.48 Fundamental Blocking Filter With Q=∞

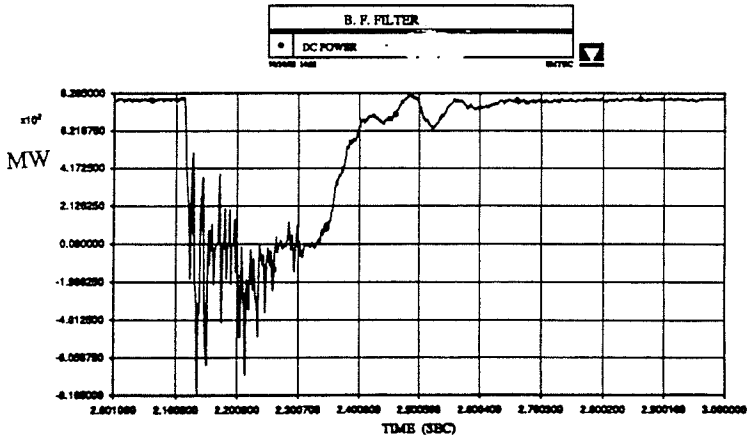


Fig. 4.49 Fundamental Blocking Filter With Q=200

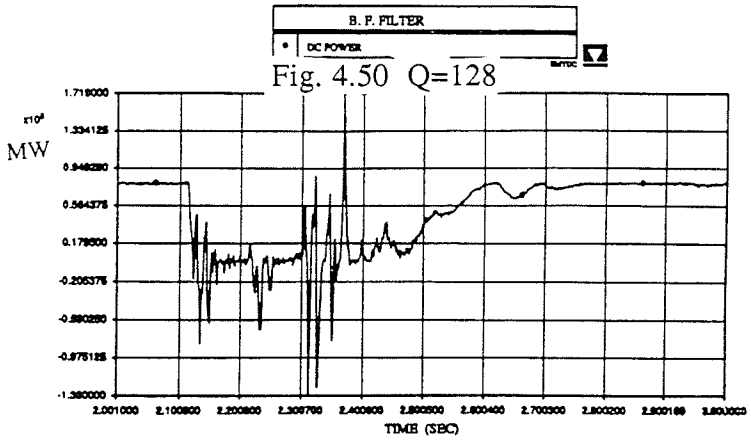


Fig. 4.50 Q=128

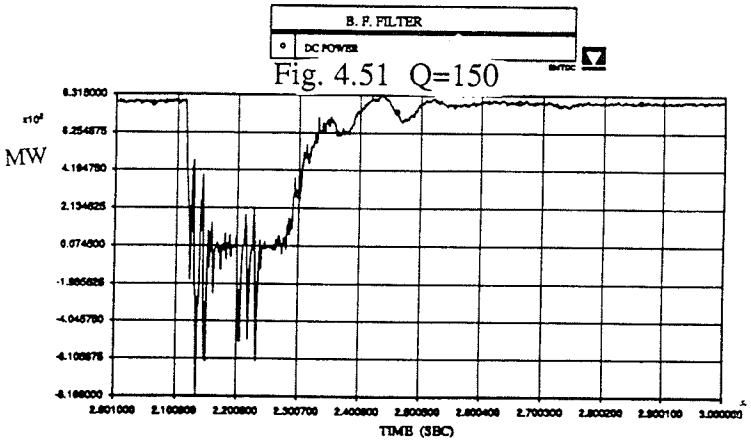


Fig. 4.51 Q=150

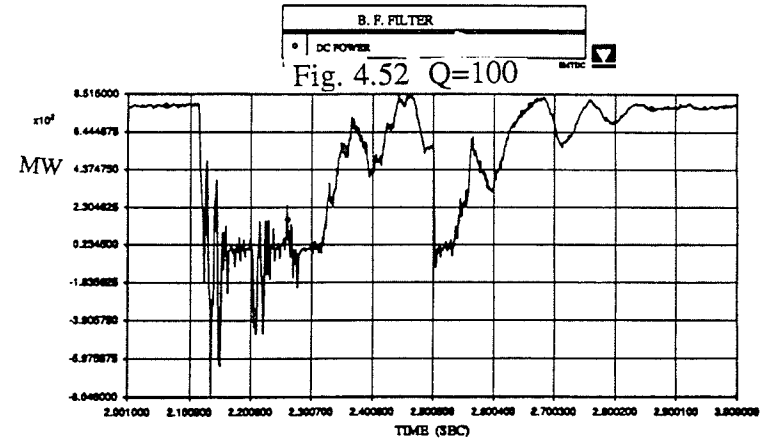


Fig. 4.52 Q=100

Fig. 4.50--4.52 Fundamental Blocking Filter With Different Q

(a) For DC system start up process: At the system steady state, the rated AC voltage between the fundamental blocking filter is ±45.0 KV, and the rated AC current through the fundamental blocking filter is ±0.175 KA.

(b) For SLGF at the inverter commutating bus: The DOV is between +187.8 KV and -196.3 KV; while the DOC is between +0.91 KA and -0.784 KA. The system can successfully recover from this kind of fault.

(c) For 3LGF at the inverter commutating bus, see Fig. 4.59. The DOV is between +187.8 KV and -196.3 KV; while the DOC is between +0.91 KA and -0.784 KA. The system can successfully recover from this kind of fault.

(d) For SLGF near the inverter commutating bus: The DOV is between +127.4 KV and -178.7 KV; while the DOC is between +0.764 KA and -0.941 KA. The system can successfully recover from this kind of fault.

(e) For 3LGF near the inverter commutating bus: The DOV is between +114.7 KV and -112.9 KV; while the DOC is between +0.507 KA and -0.634 KA. The system can successfully recover from this kind of fault.

(f) For a single phase AC source loss fault at the inverter side: There is no DOV produced in this case. The AC voltage between the fundamental blocking filter is changed between ±45.0 KV. The DOC is between +0.292 KV and -0.345 KA. The system can successfully recover from this kind of fault.

(g) For the three phase AC source loss fault at the inverter side: There is no DOV in this case. The AC voltage between the fundamental blocking filter is changed between ±45.0 KV. The DOC is between +0.222 KA and -0.236 KA. The system can successfully recover from this kind of fault.

(h) For the DC line to ground fault at the inverter end: There is no DOV and DOC produced in this case. The AC voltage between the fundamental blocking filter is changed between ±45.0 KV, and the AC current through the fundamental blocking filter is changed between ±0.175 KA.

From all the simulations cases, it can be seen that the fundamental blocking filter method will provide good system fault recovery.

A kind special modification of the DC control is also tried in our simulation system.

This idea comes from the Manitoba HVDC Research Center's research work, which can successfully damping the harmonic instability in their test system[5]. The diagram of the DC control is shown below:

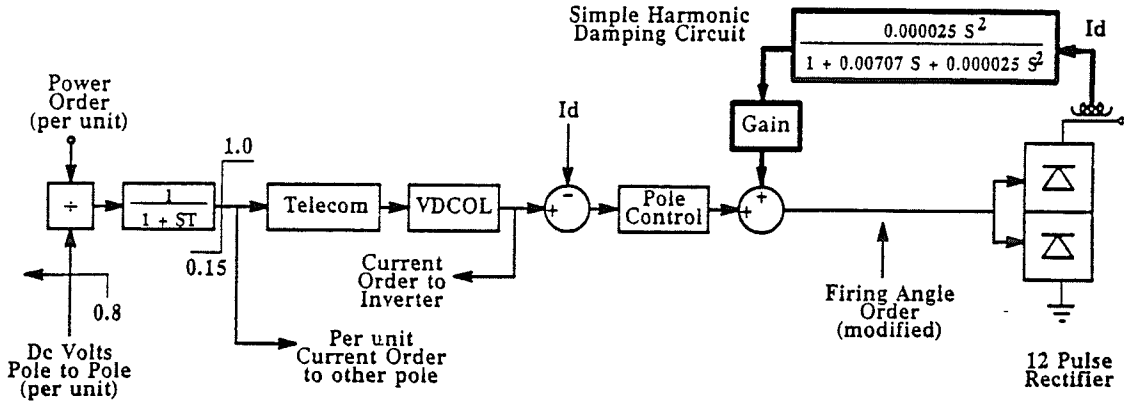


Fig. 4.53 Simple harmonic damping circuit modulating firing angle order at rectifier valve group in response to DC current (Id = per unit DC current)

It use the re-injection of harmonic distortion for damping the harmonic instability. Fig. 4.53 shows a simple addition of taking the output from a fast response DC current transducer and passing it through a high pass filter and a gain to add to the firing angle order to each rectifier valve group. This method is used in our HVDC system start process (Fig. 4.54). But unfortunately, it failed to mitigate the ferro-resonance. Further research is needed on this technique. A new research project is being undertaken an the Manitoba HVDC Research Center. So this thesis will not deal with this method any further.

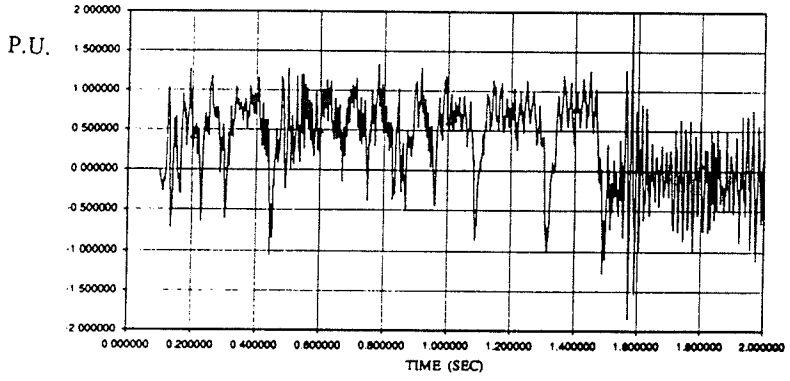


Fig. 4.54 The Test With Special Control Method (DC Voltage)

Another failure we observed is to add damping in the neutral of the converter transformer. Since the two places we have added damping have been at the AC filters and at the series capacitor, it is reasonable to consider adding damping at the converter transformer. The diagram is shown in Fig. 4.55.

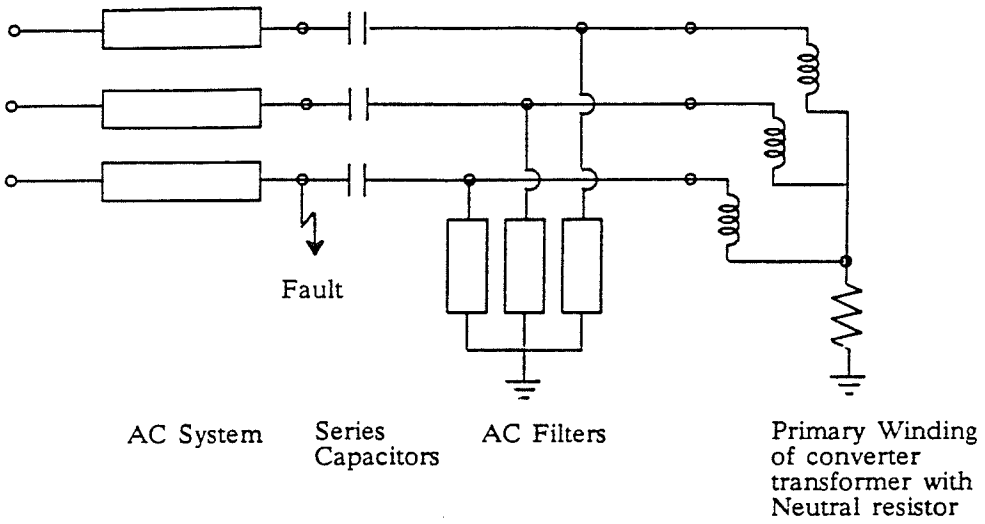


Fig. 4.55 The diagram of using the neutral resistor for damping

The basic idea of this method is to use the zero sequence current for damping ferro-resonance. Based on this idea, simulation tests are observed. The results show this method has a strong selectivity to the DC control parameters. Combined with the optimal DC control parameters, the HVDC system can successfully start up (Fig. 4.60) and recover from 3LGF near the inverter commutating bus (Fig. 4.61). But the other fault tests all failed to recover. Since optimal control parameters do help to eliminate the ferro-resonance, so It would seem the neutral resistor does not play a key role in the only two successfully cases. To clarify this further, the neutral current and the energy consumed by the neutral resistor are recorded in Fig. 4.62(a) and Fig. 4.62(b). From Fig. 4.62(a), it can be seen that the neutral current in the transient state is composed of many impulses. In mathematics, this kind of impulse is called a ∂ function, but its limitation is not infinite. As we know, the integration the the ∂ function with the infinite limitation is ***1***, while the integration of the ∂ function with the finite limitation is ***0***. Using this mathematical knowledge to our simulation system, the integration means the energy consumed by the neutral resistor, which is almost zero (Fig. 4.62(b)). So the neutral resistor does not absorb the ferro-resonance energy and is unsuccessful for damping ferro-resonance.

Although the above two methods failed to eliminate the ferro-resonance, they do give help understand the ferro-resonance phenomenon further.

4.2.7 Hard Bypass And Pre-insertion Resistor (HBP+PIR)

The diagram of this method is shown in Fig. 4.55-1.

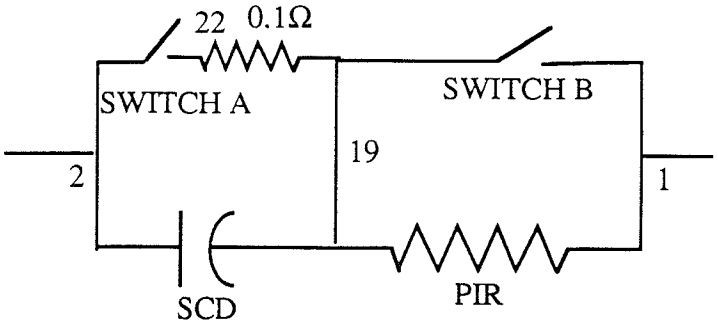


Fig. 4.55-1 The diagram of HBP+PIR method

The insertion of the 0.1 Ω resistor is for the computer simulation of the SWITCH A. SWITCH B is normally closed, i.e., resistor PIR not in but bypassed. Because the transformer remanent flux causes most of the problems prior to re-insertion of SCD the PIR resistor is used to centre flux in the transformer core. In order to limit the energy losses, SWITCH B is never open for more than 0.02 seconds.

The sequence of events for recovering from faults is illustrated in Fig. 4.55-2.

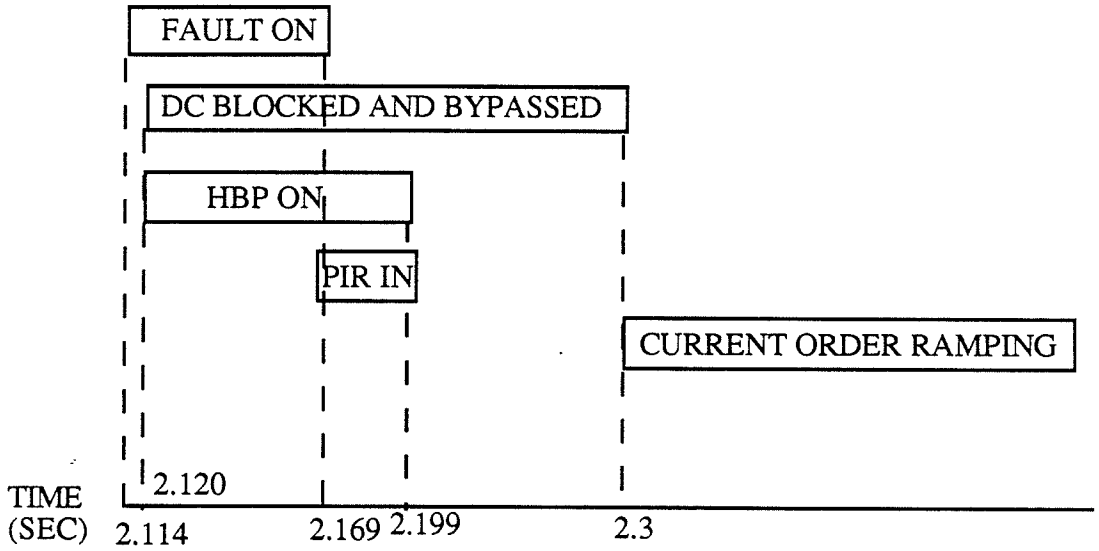


Fig. 4.55-2 The sequence of events

It is more likely that faults will occur on the system outside the station -- at node 2. If faults happen inside the station (at node 1 or node 19), we will take a longer time to recover, or leave the dc shunt down.

It should only be necessary to use the HBP across the capacitor when faults are at node 1 or node 19.

Based on this method, various kinds of AC/DC faults are tested and compared in Table 4.13-1.

Another idea is to change the position of the filters. Because the filters can also supply the current to the transformer core which may effect the transformer saturation, so changing the filter group position to the system side of the SCD side may help to centre the flux between the knee point (the knee point is ±1.2 P.U.). EMTDC was used to examine this idea. The simulation shows a good fault recovery performance.

4.3 CONCLUSIONS

1. The ferro-resonance phenomenon occurs in the HVDC system high speed starting process and almost all kinds of AC/DC line to ground fault recovery processes, which seriously affects the stability of the HVDC system.

2. To solve this problem, two basic ideas can be considered:

(1) Lower 2nd and 3rd AC impedance by filters. Sometimes it is possible to get harmonic damping of 2nd and 3rd harmonics by DC link controls.

(2) Remove subsynchronous energy from the series capacitor and magnetic circuit.

3. On the basis of these two points, some methods are tried and several of them have been proved can be used to solve this problem successfully, such as the series/parallel damping filter method, the 2nd harmonic filter method, the R + SWITCH method, the thyristor controlled resistor method, and the fundamental blocking filter method.

4. In order to get a good balance of reactive power at the rated state of 810 MW, the filters supply approximately 200 MVAR of reactive power. AC filters are redesigned to add additional harmonic damping. The rating of new filters is 217 MVAR. By calculating the harmonic distortion constant, it shows new filters didn't increase the telephone interference. So the design of new filters is reasonable both in system operation and telephone interference.

5. A multiple run procedure of time simulation supplies a good tool to get optimal control

parameters for improved fault recovery.

6. Some failure cases are also recorded, such as the CVT suppression method, the thyristor controlled inductor method, the modification of DC control method, and the neutral resistor method. They do help understand the ferro-resonance phenomenon further.

Table 4.13-1 (HBP+PIR method R=1000.0 Ω) The three phase peak flux in transient process

Cases / Three phase flux	Normal	SLGF at Comm. Bus	3LGF at Comm. Bus	SLGF near Comm. Bus	3LGF near Comm. Bus	Single Phase Source Loss	3 Phase Source Loss	DC Fault
Phase A (P.U.)	+1.0	+1.4	+1.6	+1.7	+1.7	+1.5	+1.6	+1.4
	-1.0	-1.6	-1.5	-1.7	-1.6	-1.6	-1.6	-1.5
Phase B (P.U.)	+1.0	+1.0	+1.4	+1.5	+1.7	+1.25	+2.0	+1.5
	-1.0	-1.5	-1.6	-1.8	-1.7	-1.6	-2.0	-1.5
Phase C (P.U.)	+1.0	+2.0	+1.4	+1.5	+1.4	+1.6	+1.8	+1.7
	-1.0	-1.7	-1.4	-1.6	-1.5	-1.5	-1.7	-1.7

Fig. 4.55-3 Test With HBP+PIR Method

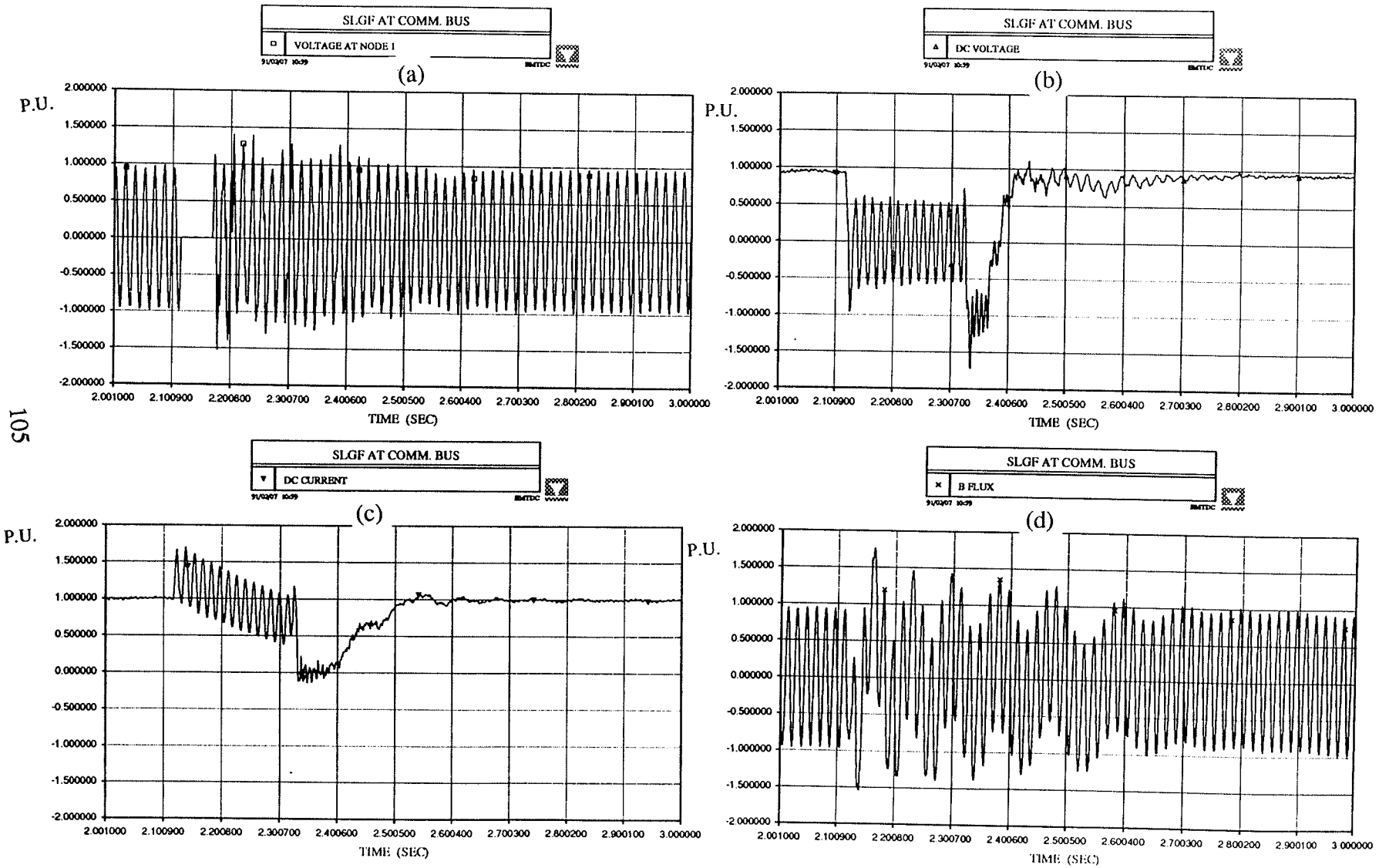


Table 4.14 Dynamic Overvoltage And Dynamic Overcurrent In Thyristor Controlled Resistor Case (The Same With R+SWITCH Case)

Cases / Fig. / Vmax, Imax	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLG Remote Fault	3LG Remote Fault	Single Phase Source Loss	3 Phase Source Loss	DC Fault
DOV(KV)	+44.26	+209.8	+209.8	+121.9	+97.2	+119.6	+44.26	+44.26
	-44.26	-182.0	-182.0	-221.4	-109.7	-50.7	-44.26	-44.26
DOC(KA)	+0.44	+1.09	+1.09	+1.025	+0.62	+0.47	+0.44	+0.44
	-0.44	-0.46	-0.48	-0.914	-0.76	-0.92	-0.44	-0.44
Time to get steady state (Second)	0.2	0.55	0.5	0.63	0.45	0.35	0.45	0.44

Table 4.15 Dynamic Overvoltage And Dynamic Overcurrent In Fundamental Blocking Filter Case

Cases / Fig. / Vmax, Imax	Start	SLGF at Comm. Bus	3LGF at Comm. Bus	SLG Remote Fault	3LG Remote Fault	Single Phase Source Loss	3 Phase Source Loss	DC Fault
DOV(KV)	+45.0	+187.8	+187.8	+127.4	+114.7	+45.0	+45.0	+45.0
	-45.0	-196.3	-196.3	-178.7	-112.9	-45.0	-45.0	-45.0
DOC(KA)	+0.175	+0.91	+0.91	+0.764	+0.507	+0.292	+0.222	+0.175
	-0.175	-0.784	-0.784	-0.941	-0.634	-0.345	-0.236	-0.175
Time to get stedy state (Second)	0.40	0.25	0.55	0.45	0.42	0.40	0.30	0.40

Fig. 4.56 Test With SWITCH+R Method

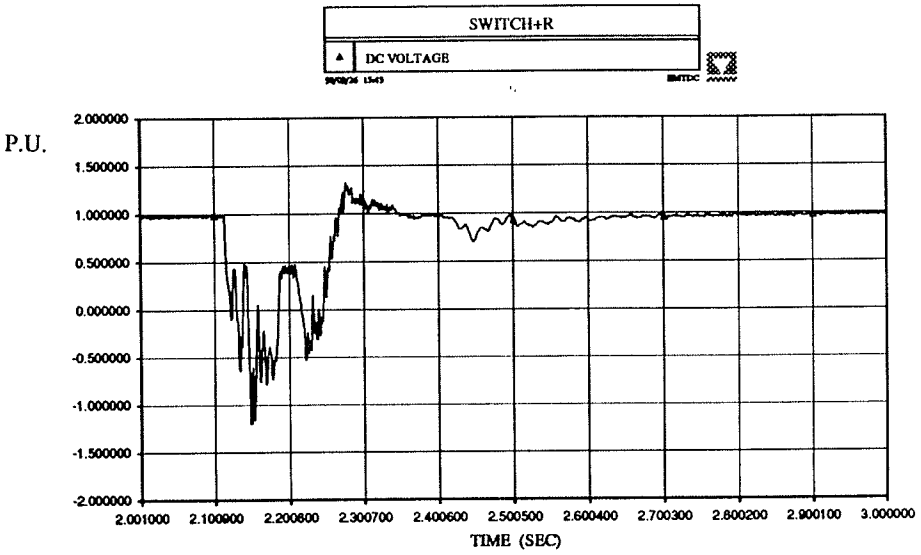
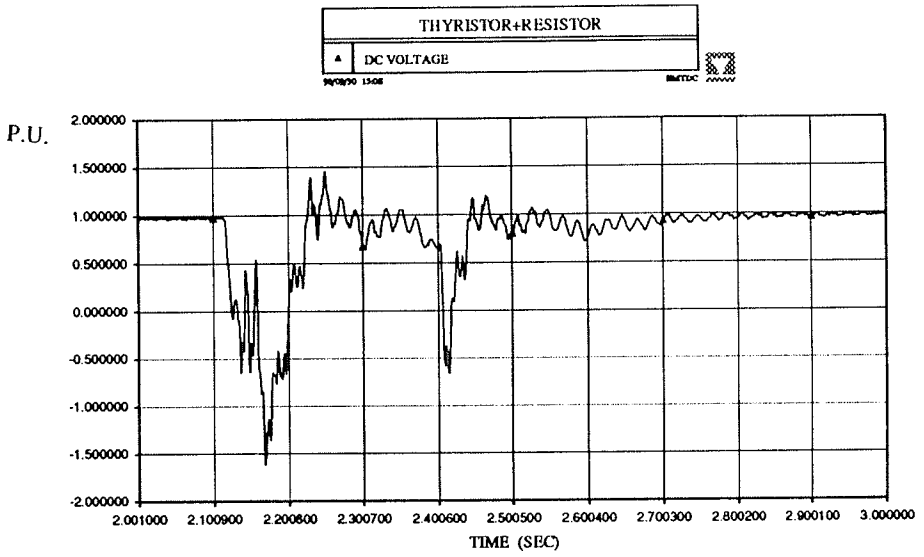


Fig. 4.57 Test With THYRISTOR+R Method



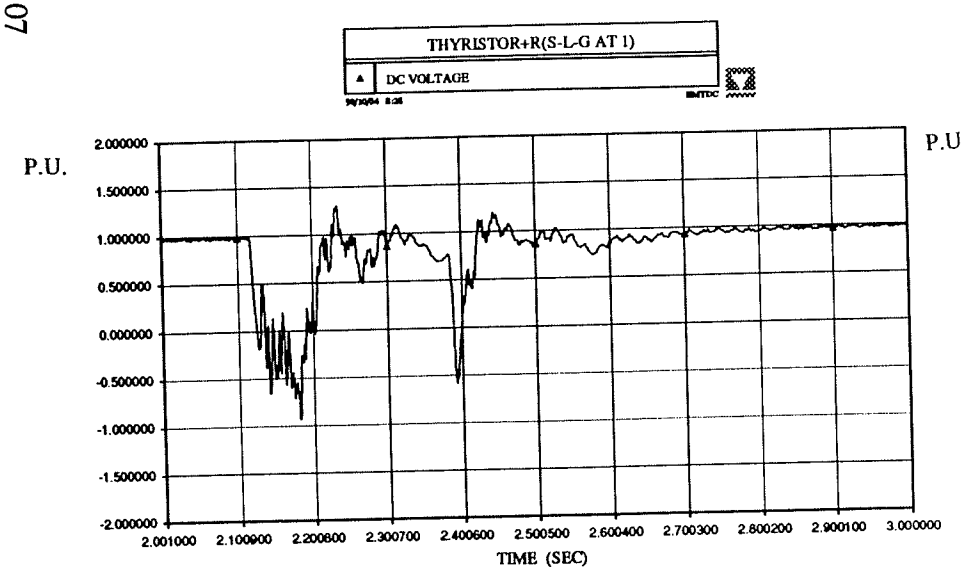


Fig. 4.58 Test With THYRISTOR+R Method

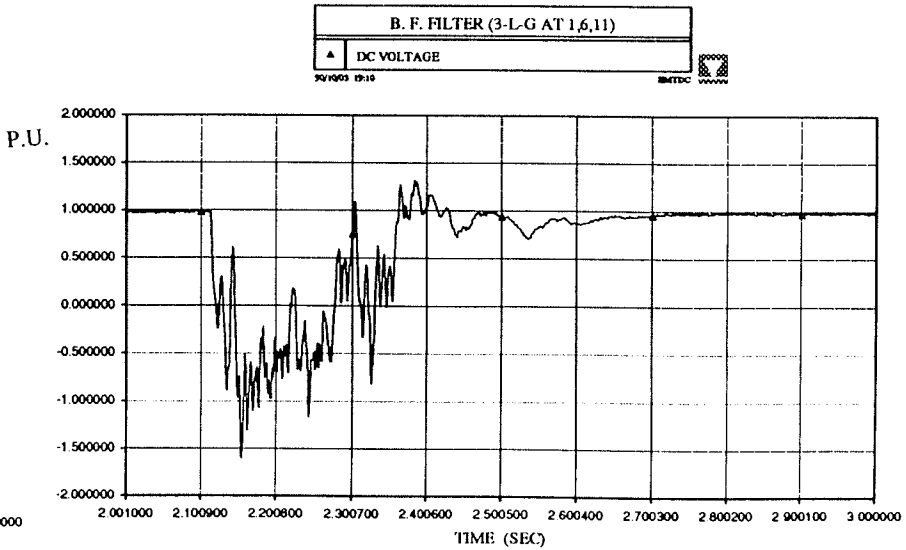


Fig. 4.59 Test With F. B. Filter Method

Fig. 4.60--4.62 Test With Neutral Resistor

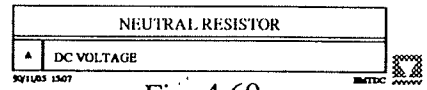
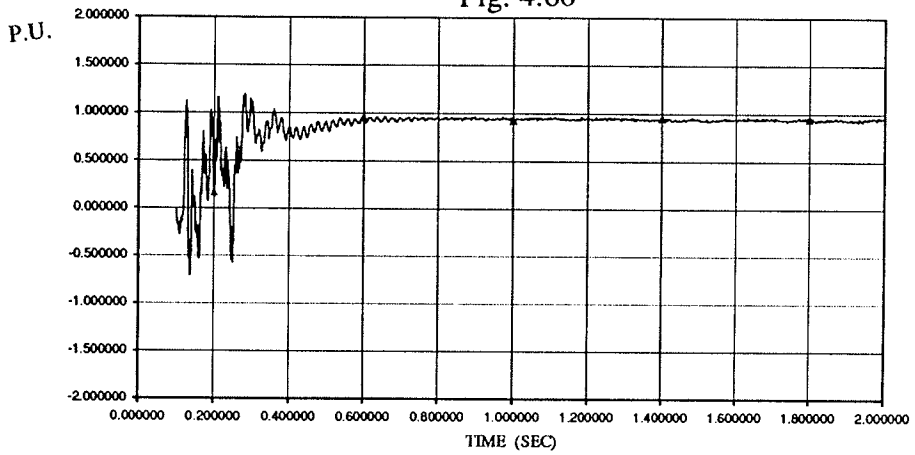


Fig. 4.60



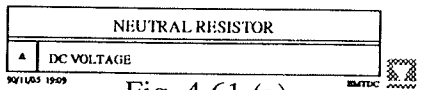
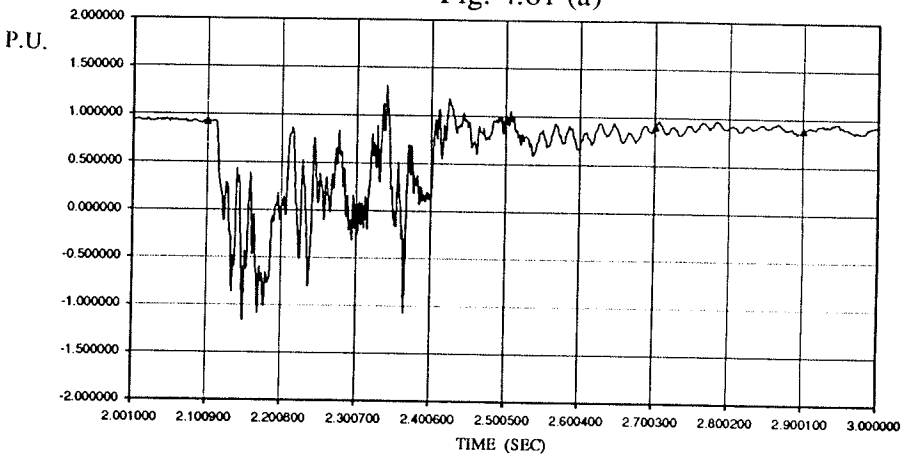


Fig. 4.61 (a)



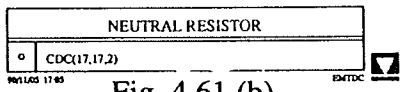
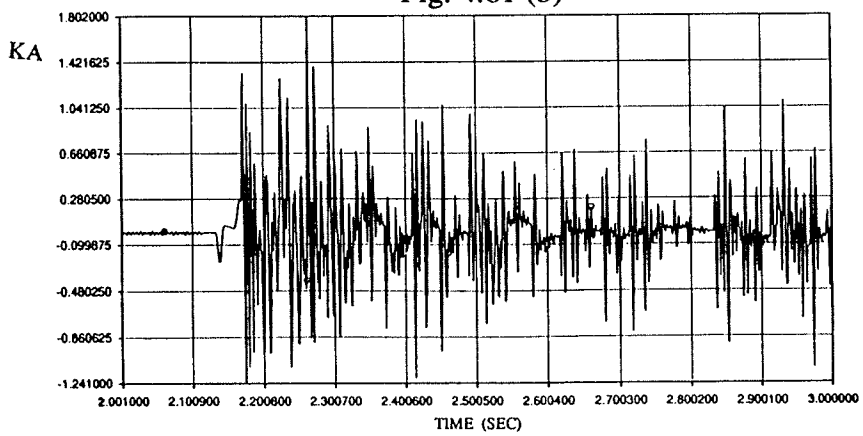


Fig. 4.61 (b)



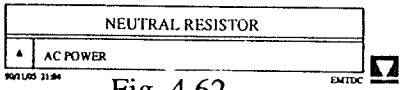
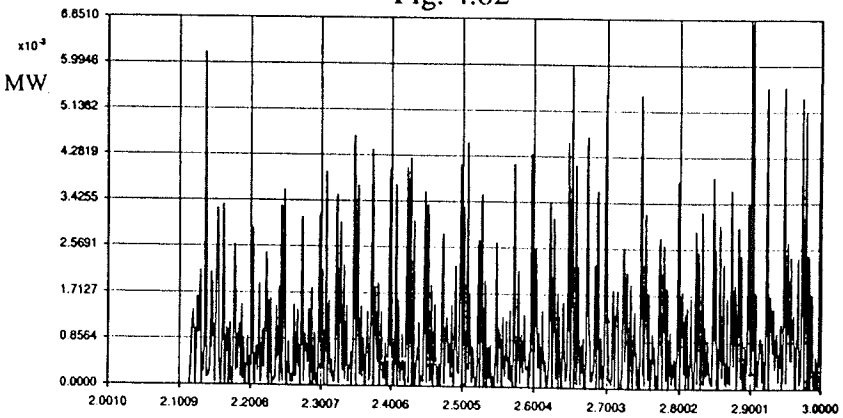


Fig. 4.62



Chapter 5

ECONOMIC EVALUATION

One advantage using series capacitor for DC compensation is its economics. Even with the subsynchronous damping circuit, an economical is to be maintained if possible. It is necessary to look at the economic evaluation for a SCD corresponding and each ferro-resonance mitigative methods. Because it's difficult to get the precise data, all the figures got below are the approcimate figures.

5.1 THE ECONOMIC EVALUATION OF EACH VOLTAGE CONTROL DEVICE (VDC)

Table 1.1 gives the cost of each VCD as a percentage of the HVDC converter station cost, not including cost of the device of itself. From this table, it can be seen that the SCD scheme is the most economical.

5.2 THE ECONOMIC EVALUATION OF THE REACTIVE POWER EQUIPMENT

A converter station costs about $100,000/MW. For an 810 MW station, the cost is $81,000,000 (which includes station installation). From table 1.1, it can be seen that SCD takes 13% of the converter station total cost. Then the cost of the SCD is: 81,000,000 * 13%=$10,530,000. The 176.0 μF SCD can supply 225.0 MVAR reactive power at the system rated state, the cost of SCD per KVA will be about 10,530,000 /(225.0*1000)=$46.8/KVA.

5.3 THE ECONOMIC EVALUATION OF THE CIRCUIT BREAKER[25]

Table 5.1 gives the cost of each kind of circuit breaker. The breaker we used in the SWITCH + R scheme is only 45.0 KV rated voltage. It is enough to chose the $150,000's

breaker.

Table 5.1 The economic evaluation of the circuit breaker

VOLTAGE (KV)	COSTS ($1000)
345.0	700--800 /per breaker
500.0	1400--1600 /per breaker
765.0	1800--2000 /per breaker

5.4 THE ECONOMIC EVALUATION OF THE RESISTOR

In our ferro-resonance damping scheme, 100 Ω resistor is used to remove the subsynchronous energy from series capacitor and magnetic circuit. From the system condition and the AC voltage across the resistor and the AC current through the resistor (see Table 4.17), $200,000 resistor can be chosen.

5.5 THE ECONOMIC EVALUATION OF THE THYRISTOR

In order to reduce the DOV between the thyristor and the DOC through the thyristor, MOV is used to combine with the thyristor. From the previous analysis and simulations, MOV takes 14% of the total HVDC converter cost. Thyristor is chosen as $3,750,000. This scheme is much more expensive than the others.

5.6 THE ECONOMIC EVALUATION OF FILTERS

Based on the 200 MVAR filter cost 7.5% of the 810MW converter station, the economic evaluation of 2nd harmonic filter and the fundamental blocking filter (+SCD) is given as 17.39% and of the total HVDC converter cost.

5.7 SUMMARY

Based on above the economic evaluation of each components, the economic evaluation of SCD with the corresponding subsynchronous damping scheme is given in Table 5.2.

Table 5.2 The economic evaluation of SCD with the corresponding subsynchronous damping scheme

Devices / Economic Evaluation	SCD	SCD with Fundamental Blocking Filter + R	SCD with SWITCH + R	SCD with PIR+HBP	SCD with shunt 2nd harmonic filter	SCD with Thyristor +R + MOV
% of station capital cost	13.0	14.67	14.81	15.89	17.39	55.0

Of these four methods, except the SCD with MOV + THYRISTOR method which is much more expensive, the costs of the other four methods are only a little higher than the SCD itself. So an economic solution for ferro-resonance does exist. It appears that the series compensation for DC converter is passable in both a technology aspect and an economic aspect.

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APPENDIX A

DATA USED IN DIGITAL SIMULATIONS

Given below is a list of system data, filter data and machine data used in the digital simulations.

Table A.1

INPUT DATA

DC SYSTEM DATA

CONFIGURATION	=	6 PULSE - MONOPOLE
POWER RATING	=	810.0 MW at INVERTER (1800A, 450kV)
REACTIVE POWER REQUIRED	=	425.0 Mvar
NOMINAL ALPHA	=	15°
NOMINAL GAMMA	=	18°
MODE OF OPERATION	=	CONSTANT CURRENT
CONVERTER TRANSFORMER;		
RATING	=	960.0 MVA
CONNECTION	=	STAR -STAR
REACTANCE	=	13% (on own base)
AIR CORE REACTANCE	=	26%
KNEE POINT VOLTAGE	=	1.2 pu

AC STSTEM DATA

L-L VOLTAGE AT RECTIFIER	=	138 kV
SCR AT RECTIFIER	=	4.0
L-L VOLTAGE AT INVERTER	=	230 kV
SCR AT INVERTER	=	1.5
FILTER RATING;		
AT RECTIFIER	=	200 Mvar
AT INVERTER	=	200 Mvar

Table A.2

SYSTEM IMPEDANCE DATA

Receiving End AC System Data

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z mag. (Ohms)	Z angle (deg)	SCP mag. (MVA)	SCP angle (deg)
1.5	5.0274	523.81	0.0975	37.385	78	1415	78

Sending End AC System Data

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z mag. (Ohms)	Z angle (deg)	SCP mag. (MVA)	SCP angle (deg)
4.0	0.3059	180.16	0.0139	5.261	85	3620	85

DC Line Data

Length	=	895 km
Line Resistance	=	0.115 ohm/km at steady state (5.0 Hz)
	=	0.019 ohm/km at 90 Hz
Mode travelling Time	=	3.037 ms
Characteristic Impedance	=	300.0

Table A.3

FILTER DATA

AC FILTER DATA

Harmonic	Nos	Inverter R (Ohms)	Inverter L (Henry)	Inverter C (μF)	Inverter Mvar	Rectifier R (Ohms)	Rectifier L (Henry)	Rectifier C (μF)	Rectifier Mvar
5	2	14.22	0.2986	0.9425	39.20	5.37	0.1094	2.5725	38.5
7	2	14.22	0.2986	0.4810	19.60	5.37	0.1094	1.3130	19.2
11	2	5.32	0.0786	0.7395	29.70	3.56	0.0270	2.1570	31.2
13	2	5.32	0.0786	0.5280	21.20	3.56	0.0270	1.5440	22.3
HP	2	94.80	0.0072	202795	90.30	47.20	0.0026	6.1790	88.8
					200.0				200.0

DC FILTER DATA

Harmonic	Nos	Inverter R (Ohms)	Inverter L (Henry)	Inverter C (μF)	Rectifier R (Ohms)	Rectifier L (Henry)	Rectifier C (μF)
6	1	24.0	0.2444	0.80	24.0	0.2444	0.80
12	1	12.0	0.1222	0.40	12.0	0.1222	0.80