A Solid State Voltage Control Device for Distribution System Applications

by
David Jacobson

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Abstract

Voltage control devices currently in use on single phase distribution feeders are not adequate to correct for the rapid fluctuations in voltage caused by intermittent loads such as motor startings and welding. Recently, static var compensators have been examined by manufacturers and researchers for their suitability of being installed at distribution level voltages. To date, a compact single phase device that is comparable in size and cost to a step voltage regulator while being able to correct voltage flicker has not been developed.

In order to study this problem, phase A of St. Agathe feeder SA-1 was modelled. The possibility of voltage flicker exists on this feeder due to farming loads. A thyristor switched capacitor and voltage source inverter were modelled with an electro-magnetic transient program (EMTDC), to test the suitability of each device as a voltage regulator. It was shown, through digital simulations, that the thyristor switched capacitor (TSC) is the best choice for a single phase voltage regulator. Further verification was provided via a real time analog simulator. Results showed the TSC does not produce harmonics, produces minimal transients during startup and fault recovery and voltage flicker can be effectively eliminated.

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List of Symbols

Tabulated below are some of the more frequently occurring symbols and acronyms.

ABB	Asea Brown Boveria
B_c	capacitive susceptance
B_s	susceptance of coupling transformer
B_{svs}	total TSC susceptance
E	equivalent system voltage
EMTDC	Electromagnetic Transient Program for DC systems
FC/TCR	fixed capacitor/ thyristor controlled reactor
GTO	gate turn off
Hz	hertz
I_{svs}	compensator current (RMS)
kVA	kilovoltampere
kVAr	kilovar
kW	kilowatt
pf	power factor
PI	proportional integral
PWM	pulse width modulated
RMS	root mean square
SVC	static var compensator
TCUL	tap changing under load
TSC	thyristor switched capacitor
VMF	voltage magnification factor
VSI	voltage source inverter
V_{svs}	compensator primary bus voltage (RMS)
V_{2RMS}	RMS voltage of transformer secondary
X_e	equivalent system reactance

Chapter 1
Introduction

1.1 Purpose

The objective of this thesis is to design and test a single phase voltage control device suitable for controlling the fast fluctuations in voltage associated with loads such as spot welding, motor starting and scrap melting. Candidate devices were simulated digitally on the electromagnetic transients program EMTDC [41] with final testing of the most suitable device being performed on an analog simulator.

1.2 Motivation

The voltage control device most commonly used in a distibution feeder is a step voltage regulator or mechanically switched capacitor. These devices, while correcting for the change in voltage caused by the slow changes in daily load demand, cannot correct for fast fluctuations in voltage. Recently, much interest has been shown towards applying static VAr compensators to distribution systems [16-21]. Various kinds of static VAr compensators (SVC) have been evaluated including thyristor switched capacitors (TSC) [16,17,39], fixed capacitor/thyristor controlled reactor (FC/TCR) [19], and voltage source inverters (VSI) [20,21]. All of the compensators descibed in the literature are three phase devices with ratings exceeding 2 MVAr. There has been no research to date on a compact single phase device which will be able to directly replace step voltage regulators and mechanically switched capacitors while providing the voltage regulation performance of a large SVC.

1.3 Outline of the Thesis

Chapter 2 provides background information on single phase distribution voltage. The first section descibes characteristics of various single phase loads which cause voltage fluctuation problems. This is followed by a description of the most recent state of the art in distribution voltage control devices. In Chapter 3, the essential components and control algorithms are designed for a thyristor switched capacitor and voltage source inverter. Chapter 4 contains the test results. Each compensator is simulated digitally followed by analog simulations of the TSC. Finally, Chapter 5 provides conclusions and recommendations for further studies.

Chapter 2
Single Phase Distribution Voltage

2.1 Introduction

There are many thousands of miles of single phase feeders in a utility's distribution system. Connected to these feeders are customers who have a variety of loads including: lighting, power, heating and electronic. It is the utility's responsibility to maintain an adequate quality of supply to these consumers. Voltage fluctuations, if not corrected, will cause customers to complain about damage to sensitive electronic equipment and about annoying light flicker. The purpose of this chapter is to describe several types of single phase loads which cause voltage fluctuations and the state of art in utility's compensation devices.

2.2 Voltage Fluctuation Problem

A single phase distribution feeder can have a variety of loads each having its own unique effects on the system voltage. Effects that must be corrected include: reduced power factor, voltage depression, and voltage flicker. Characteristics of several troublesome loads will be described in this section including their particular effect on the voltage.

Voltage dips can be caused by the high inrush current required during motor starting. Most single phase motors in domestic homes have ratings which are low enough not to cause problems on the distribution system. However, heat pump compressor motors have ratings of 3 - 4 Kilowatts at 0.8 power factor lagging. There can be several starts per hour depending on weather conditions. Voltage dips in excess of 1% can be expected with the situation becoming worse if several homes in an area have heat pumps and the compressor motors are starting simultaneously [6]. Small industrial installations such as farms or saw

mills could have single phase motors rated as high as 7.5 kW.

Frequent voltage dips will cause the light output of incandescent lamps to flicker. The eye is sensitive to light flicker in the range of 0.01 to 10 Hz and the degree of perception and objection is determined by the magnitude of voltage change. The range of observable and objectionable flicker is graphed in Figure 2.1 [8].

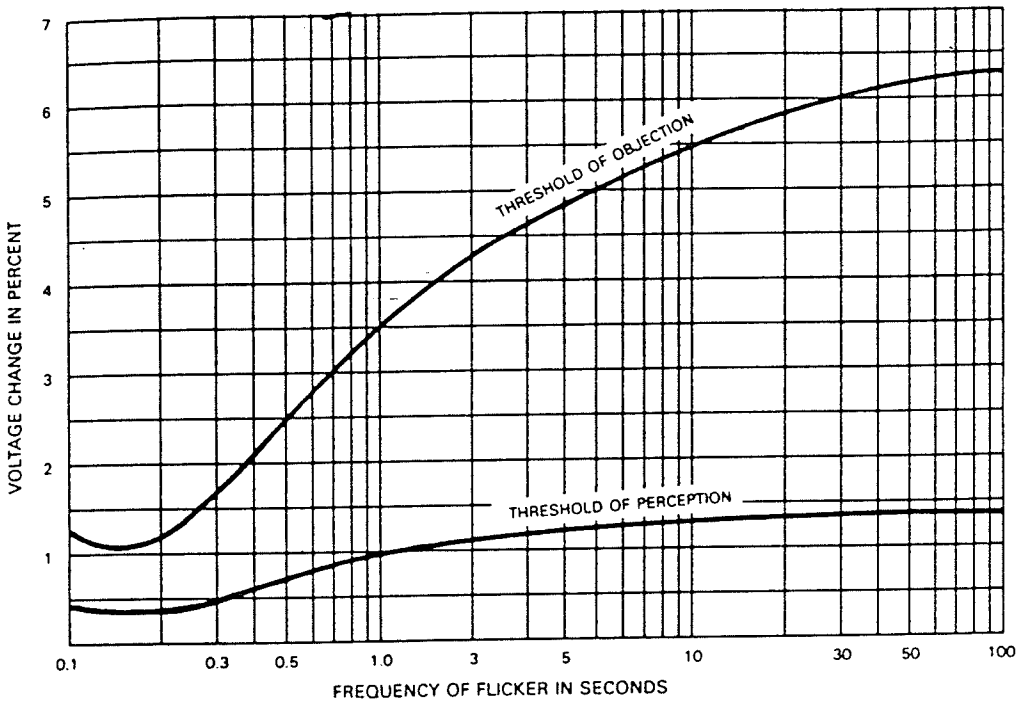


Figure 2.1: *Observable and objectionable flicker range[8]*

A common source of voltage flicker in rural feeders is from farm welding. The welding process can be divided into two types:

1. Arc welding
2. Resistance welding

Arc welding is used when the thickness of metal and length of weld becomes large. Spot welding of thin metals is the normal application of resistance welding.

Single phase arc welders are rated up to 36 kVA with approximately a 0.35 lagging power factor (pf). Current is not highly fluctuating but can last from several seconds to a

few minutes depending on the length of the weld. A circuit diagram of an arc welder is shown in Figure 2.2 [3].

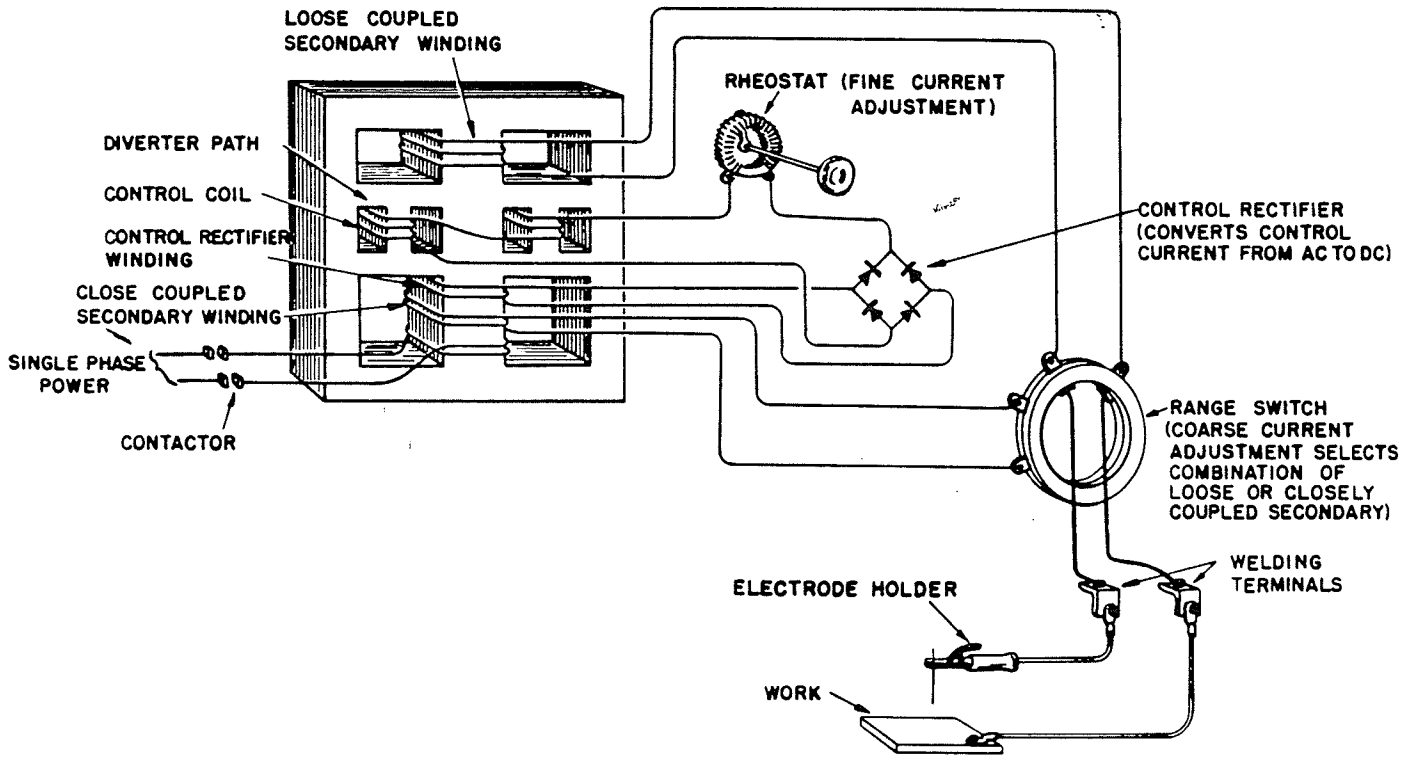


Figure 2.2: *Arc welder schematic diagram [3]*

Three factors are used in making a resistance weld:

1. Amount of current that passes through work
2. Pressure the electrodes transfer to the work
3. Time the current passes through the weld

Resistance welders are characterized by short welding times (as low as a fraction of a second) and very high currents. Unit ratings can vary from 5 to 500 kVA depending on the application. Ratings larger than 100 kVA are normally limited to use in factory production

lines. Power factor is also low and can vary from 0.2 to 0.5 lagging. A schematic of a spot welding process is shown in Figure 2.3 [3].

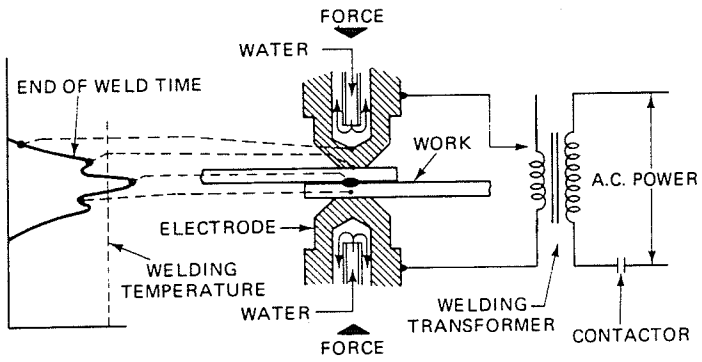


Figure 2.3: *Resistance (spot) welding process schematic [3]*

Single phase industrial heating is another cause of voltage fluctuations on distribution feeders. Although not as common as three phase units, single phase units do have applications.

There are two different forms of industrial heating:

1. Electro-magnetic induction heating
2. Arc furnace

In induction heating, the material to be heated is placed inside a coil and connected to the power supply. The high frequency (60Hz) magnetic field induces eddy currents. These induced currents, in turn, heat the material. Induction heating causes the problem of low power factor (0.2) and of creating voltage unbalance between the phases of a three phase supply.

The arc furnace in contrast, relies on the high temperatures occurring in the ionized atmosphere between electrodes to melt the material. Small installations have one carbon electrode and a scrap metal electrode, in contrast to large installations which employ three carbon electrodes. During the melt down period, the current is very large and fluctuates rapidly creating severe voltage flicker problems.

2.3 Voltage Control Devices

Several devices are currently used on single phase distribution systems to control the

voltage. These devices can be classified under the two distinct headings of regulators and capacitors. There are three types of regulators being used today: the induction regulator, the no load tap changer or autobooster and the tap-changing-under-load (TCUL) or step voltage regulator. Capacitors can be connected in either series or shunt and be either fixed or switchable. Each of these devices will be described in the following sections.

2.3.1 Autobooster

An autobooster is a no load tap changing autotransformer that can be used to either boost or buck the line voltage. Figure 2.4 [9] indicates the single phase connections.

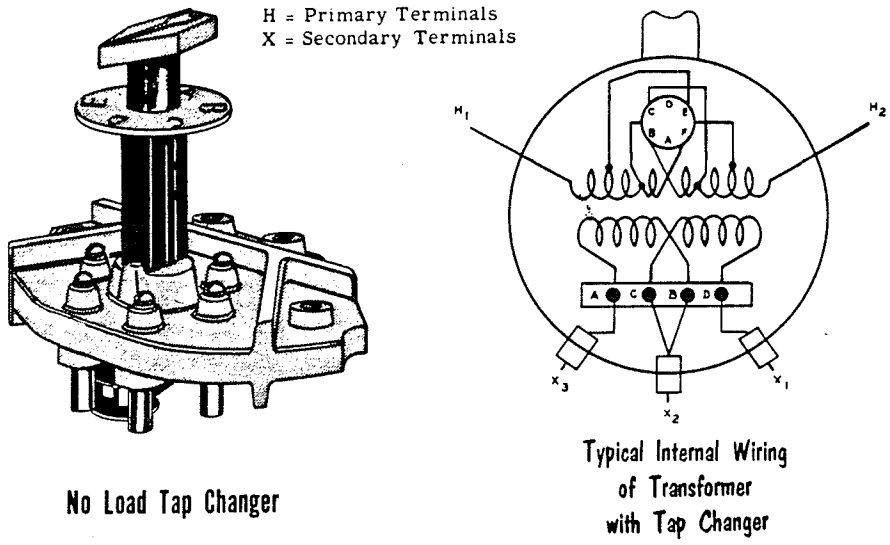


Figure 2.4: *Autobooster single phase connections [9]*

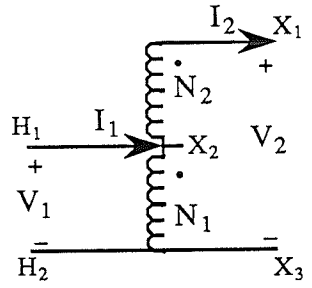
The voltage and current output from an autobooster can be determined by the example on the following page.

The winding ratio of the transformer is adjusted manually to compensate for the voltage drop in the feeder. Autoboosters have lower leakage reactance, lower losses, smaller exciting currents and lower cost than 2-winding transformers as long as the voltage ratio does not vary much from 1:1. Disadvantages include loss of electrical isolation and disconnection from service if a tap change is required.

Example

Given: primary current $I_1 = 1.0$ pu
primary voltage $V_1 = 1.0$ pu
primary # of turns $N_1 = 400$

Want 5% boost in voltage.
Find # of turns on secondary and resulting secondary current.



$$\frac{I_1}{I_2} = \frac{V_2}{V_1} = 1 + \frac{N_2}{N_1} \qquad (2.1)$$

Solution:

$$1.05 = 1 + \frac{N_2}{N_1} \quad \therefore N_2 = 20$$

$$I_2 = 1.0 / (1 + 20/400)$$
$$= 0.9524 \text{ pu}$$

2.3.2 Induction Regulator

A transformer which makes use of a rotatable coil arrangement to achieve a variable transformer ratio is known as an induction regulator. Induction regulators have been constucted in single, two and three phase units.

The operation of an induction regulator can be understood by examining an equivalent circuit of a three phase device shown in Figure 2.5 [11].

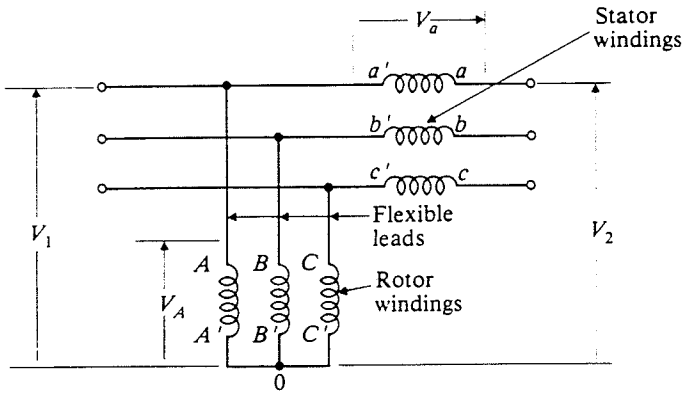


Figure 2.5: *Induction regulator equivalent circuit [11]*

By making use of equation 2.2 and 2.3 a circular locus may be drawn on the phasor diagram shown in Figure 2.6 [11].

$$V_a \approx \frac{N_{se}}{N_{re}} V_A \angle \beta_{oe} \tag{2.2}$$

$$V_2 = V_a + V_A \tag{2.3}$$

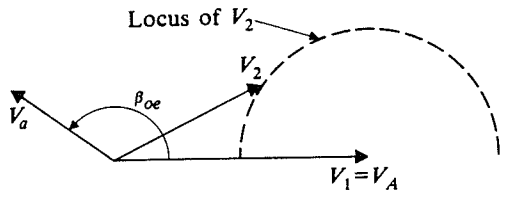


Figure 2.6: *Phasor diagram of induction regulator [11]*

The input voltage (V_1) can be assumed to be constant in the steady state. By varying the rotor angle (manually or automatically), the output voltage (V_2) will vary by an amount depending on the turns ratio and winding impedance. A control system based on the voltage regulating relay (described in the next section) is used to determine the desired rotor angle.

The induction regulator has the advantage of being able to continuously vary the output voltage. However, disadvantages of being limited to circuits of 5000 kV or less and having higher leakage inductance and magnetizing currents as compared with conventional autotransformers [5,11] are some reasons why the induction regulator is rapidly being replaced. A cross section of a typical induction regulator is shown in Figure 2.7 [5].

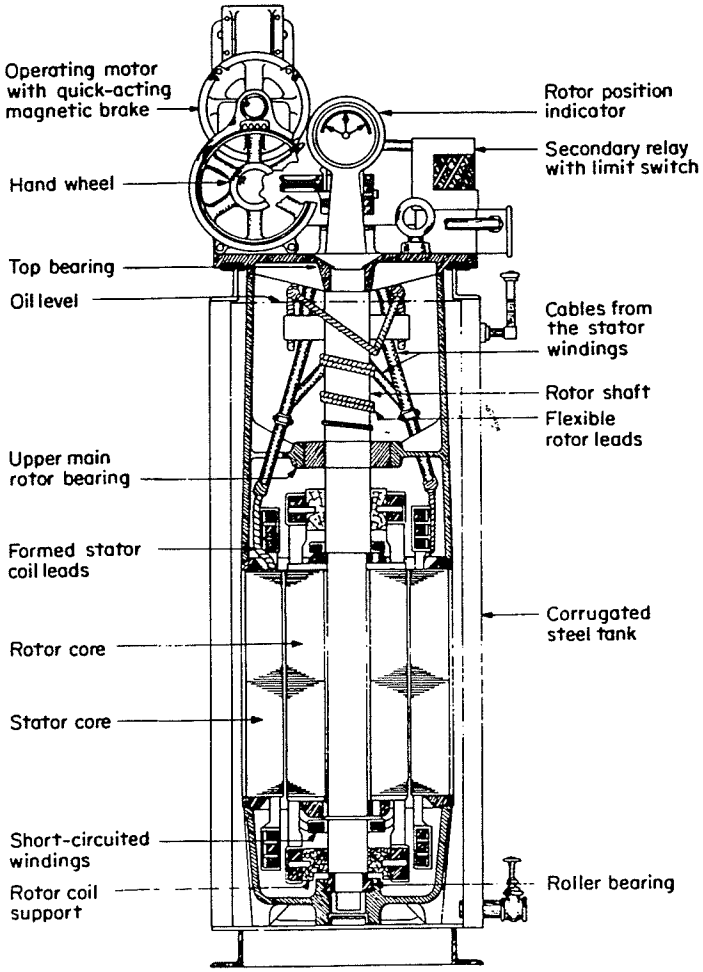


Figure 2.7: *Induction regulator cross section [5]*

2.3.3 Step Voltage Regulator

The step voltage regulator is essentially the same as an autobooster except it has the ability to tap change under load. Quite often the device is referred to as a TCUL regulator.

The taps are kept separate from the primary coil and are so arranged that the connections can be reversed so as to boost or buck the primary voltage. Figure 2.8 indicates the sequence of operation of a regulator with four taps.

The output voltage of a step voltage regulator is continuously monitored. Once the voltage exceeds the maximum set output voltage a contact is made to cause the regulator to lower the output voltage. Similarily, if the output voltage becomes too low, another contact

is made which results in the regulator increasing the output voltage. Older regulators used a contact making voltmeter to make the connections whereas today, solid state relays are used.

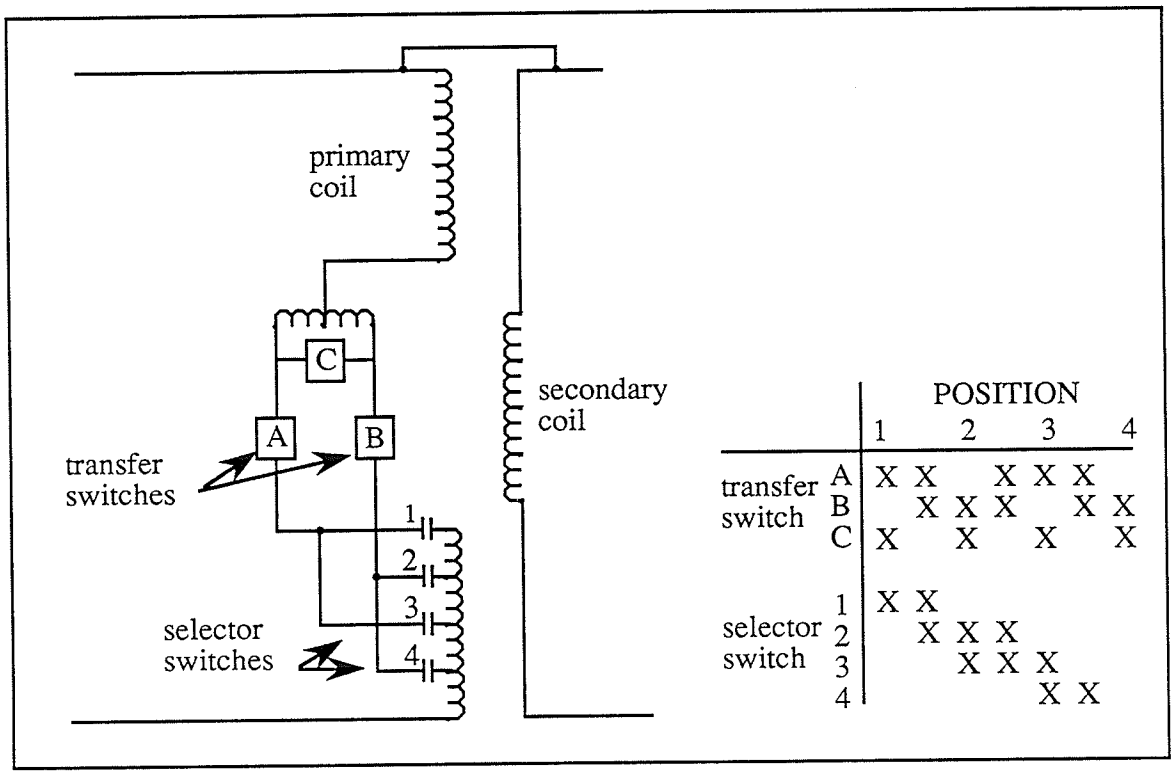


Figure 2.8: *Sequence of step voltage regulator operation*

A General Electric type ML32 [7] single phase step voltage regulator has a reference voltage level continuously adjustable between 105 and 135 volts (120 corresponds to 1 p.u.). The voltage can be held within predetermined bands of 1.5, 2, 2.5 and 3 volts (±1.25% - ±2.5% at 1.0 p.u. voltage).

It is possible to regulate the voltage at some other point further out on the feeder by employing a line drop compensator. A line drop compensator is an electrical minature of the transmission line to the point where voltage regulation is desired. Proportional values of transmission line resistance and reactance are set on the regulator. A current transformer installed inside the regulator causes a proportional voltage drop to be subtracted from the line voltage at the regulator terminals. A schematic diagram is shown in Figure 2.9 [5].

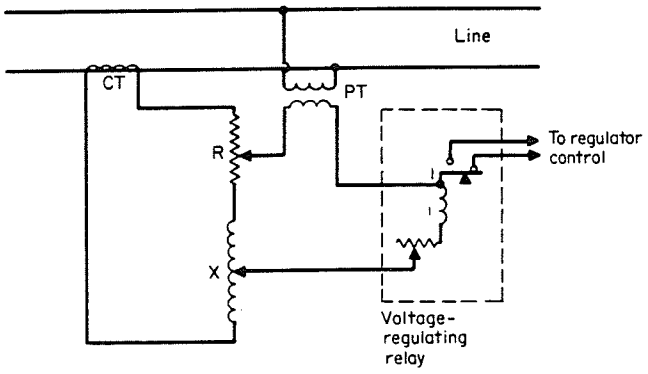


Figure 2.9: *Schematic of line drop compensator and voltage regulating relay [5]*

A time delay of 10 to 90 seconds is provided between energizing the voltage relay and operating the tap changing equipment. A 30 second delay is recommended by the manufacturer for the ML32. Some voltage variations are self correcting so the time delay is employed to increase the life of the apparatus by avoiding unnecessary switchings.

The ML32 is a popular regulator currently being used on Manitoba Hydro's distribution system. Analog controls are used in this device to determine desired tap changes. A state of the art microcomputer control system is described by Harlow and LaPlace [13].

2.3.4 Capacitor

Capacitors are also used to improve voltage regulation on distribution feeders. However, their operation is different from the previously described regulators. Most loads in a power system such as welders and motors have a low lagging power factor. The power factor can be calculated from the following equation:

$$\text{power factor} = \frac{\text{useful power (kW)}}{\text{apparent power (kVA)}} \tag{2.4}$$

Utilities are required to supply more power than necessary when a load is operating at a low power factor. A capacitor installed in shunt has the capability of cancelling the inductive (lagging) nature of the circuit or, in other words, is providing power factor correction. A cir-

cuit with an improved power factor requires less current for a given load and, therefore, reduces power losses in the transmission line.

Capacitors have been connected in shunt and series in distribution systems [4,14]. A shunt capacitor can be thought of as correcting the component of current due to the inductive reactance, whereas a series capacitor corrects for the reactive voltage drop of the line. Series capacitors are rarely installed in distribution systems. They suffer from many problems such as overvoltages due to large fault currents and ferro-resonance with transformers. Elaborate protection schemes have been developed [15] but the shunt capacitor is by far the most popular form of installation and will be described further here.

Shunt capacitors are normally installed in three phase banks and are either fixed in size or are assembled in a number of smaller units that can be mechanically switched on and off. There are a number of controls available today which can automatically switch capacitors, including:

1. Time switch
2. Temperature
3. Voltage
4. Current
5. VAr
6. Combination: power factor, voltage override

In residential and commercial areas where the load can be predicted by a utility, time switched controls can be used. Due to today's technology, time controls are able to recognize holidays, weekends and daylight saving for 20 years of operation as well as accommodate up to 5 daily load switchings operations.

Temperature controls can be applied, similarily, if a good correlation exists between temperature change and heating and air conditioner loads. The control must be able to respond to the true temperature and have an adequate time delay. Shielding of the temperature sensing element from direct sunlight and a delay of one hour to compensate for the lag of electrical load to temperature change is required.

Using measured electrical quantities to control capacitor switching is more accurate than the previously described methods but also more expensive. Voltage control is the most popular and is used to improve voltage regulation in areas where there are large voltage swings. Current controls are useful when the capacitor is located in the compensating region of a voltage regulator. Several operational problems occur with controls responding to VAr

levels only. They include:

1. Poor voltage profile during periods of large resistive circuit loading unless a low voltage override is provided in the controls.
2. Not being able to detect a low lagging power factor during periods of light to moderate circuit loading.
3. Causing overvoltages during heavy circuit loading while the power factor is acceptable due to the VAr level exceeding the control setting.

Power factor control can alleviate the above problems, however, during light loading with low power factor, power factor control will cause capacitor banks to be switched on, resulting in overvoltages and increased losses. Advanced capacitor control relays have been developed which use a combination of power factor, voltage override and undercurrent detection [4].

Electronic controls have an adjustable time delay of 15 to 120 seconds with 60 being used most commonly. The electrical signal being monitored must exceed the ON or OFF setting for at least the length of time of the time delay before a switching operation occurs.

2.3.5 Static Var Compensator

A static var compensator is a shunt connected device employing solid state switches in conjunction with capacitors and/or reactor banks. Various configurations have been proposed and installed on distribution systems including:

1. Thyristor Switched Capacitor (TSC) [16,17]
2. Fixed Capacitor/Thyristor Controlled Reactor (FC/TCR) [18,19]
3. Voltage Source Inverter (VSI) [20,22]

The principle of operation behind a TSC and VSI are descibed in Section 3.3 and 3.4 respectively. A TCR consists of an inductor in series with an anti-parallel thyristor pair. The current through the inductor can be varied from full conduction to zero by modifying the firing angle of the thyristors. Fixed or thyristor switched capacitors are normally used to remove the odd current harmonics generated by the TCR as well as to bias the TCR's control characteristic into the desired compensation region. In summary, the TSC can provide leading reactive power in discrete steps. Both the VSI and FC/TCR are capable of providing a continuous source of leading and lagging reactive power at the expense of harmonic production. A FC/TCR produces odd current harmonics while a VSI produces odd voltage

harmonics. Recommended reading for further understanding of the basic characteristics of each device can be found in [26,27,28].

The response time of a SVC is in the range of 2-4 cycles which makes it ideally suited for applications where fast voltage control is required. In the past, SVC's have been installed on transmission lines and near large loads to meet any or all of the following requirements:

1. Improved voltage regulation
2. Enhancement of steady state and dynamic stability
3. Reduction of overvoltages
4. Reduction of voltage flicker
5. Damping of subsynchronous oscillations
6. Reduction of voltage or current unbalances

Recently [16-20], SVC's have been considered for distribution systems. The SVC descibed by Wong, Osborn and McAvoy [16] is a three phase device rated 2.5 MVAr and is manufactured by Asea Brown Boveria (ABB). Keene et al. [18] descibe a three phase fixed capacitor, thyristor controlled reactor, identical to the minicomp-compact static var compensator manufactured by ASEA [19]. This device can continuously control the reactive power up to 2 MVAr. Edwards and Nannery [20] describe a three phase 1.0 MVAr advanced static var generator (voltage source inverter) which is manufactured by Westinghouse Electric Corporation.

2.4 Chapter Summary

The devices described in Sections 2-4 of this chapter were designed to correct for the slow changes in daily load demand. All of the SVC's that have been developed for distribution system applications, while being more compact than their counterparts at higher voltages [32,33], are limited to applications at substations or at the terminals of medium sized industrial plants. Other methods of improving voltage regulation which have been used but are not described here include motor starters and reconductoring or strengthening the supply system. Motor starters, while attempting to reduce the starting voltage dip, can introduce dips of their own [16]. Strengthening the supply is a very expensive alternative and is not guaranteed to work. A smaller less expensive single phase device is required for the fluctuation problems described in this chapter. Two proposed single phase compensators will be designed and tested in the next two chapters.

Chapter 3
Compensator Design

3.1 Introduction

Two single phase compensators will be designed in this chapter. The reactive power requirements of a typical single phase feeder is calculated first from load flow studies. Components and control algorithms for a thyristor switched capacitor and voltage source inverter are designed next.

3.2 Reactive Power Requirements

Capacitors are rated according to their nominal voltage and kVAr rating. A quick method of determining the amount of capacitance required at a particular location is found by using equation (3.1).

$$\text{capacitor kVAr} = \text{kW}(\tan\Phi_1 - \tan\Phi_2) \qquad (3.1)$$

Φ_1 = uncorrected angle of lag

Φ_2 = corrected angle of lag

kW = size of load in kilowatts

For example, say we have a load of 271 kW at a lagging power factor of 0.8 and we wish to add capacitance to bring the power factor to unity.

$\Phi_1 = 36.87°$ $\Phi_2 = 0.00°$

$$\text{Cap kVAr} = 271.0\ (\tan 36.87° - \tan 0.00°)$$
$$= 203.25 \text{ kVAr}$$

A capacitor of 203.25 kVAr is required to bring the power factor to unity. Slightly more capacitance may be required to regulate the voltage to 1.0 pu.

In order to determine how much additional capacitance is needed, the equivalent reactance between the source and compensator and the desired voltage change must be known. Equation 3.2 can then be used to determine the amount of capacitance needed.

$$\text{capacitor kVAr} = \frac{I_c}{k} = \frac{\delta E / X_l}{k} \qquad (3.2)$$

I_c = capacitor current
X_l = source reactance
k = amps per kVAr

In the previous example, the source reactance is 16.6 Ω and during heavy loading the voltage drops to 0.925 pu. If the feeder is operating at 7200 volts, the amount of capacitance required is 232.36 kVAr or an additional 29 kVAr is needed to regulate the voltage (from the previous example).

k = 1000/7200 = 0.14 Amps/kVAr
I_c = (7200 - 6660)/16.6 = 32.53 Amps
capacitor kVAr = 32.53/0.14 = 232.36 kVAr

Mr. Paul Wilson of Manitoba Hydro supplied us with several possible locations for our compensator. These locations are listed below along with the type of regulation device currently being used and size of load served:

1. St. Agathe: NW23-7-1E, 50A autobooster 16 Farms
2. Morris: SW11-4-1W, 66A Reg. Town of Sewell
3. Lettelier: SE36-1-1E, 66A Reg. 23 customers
4. Lowe Farm: SW20-4-1W, 33A Reg. 12 customers
5. Manitou: NW2-1-8W, 50A auto 18 customers
6. Manitou: NW30-2-8W, 50A auto 13 customers
7. Manitou: NW9-4-9W, 100A Reg. 14 customers

In each case the load served is between 150 and 300 kVA. Information was not provided on the type of load or power factor, therefore, a worst case of 0.8 pf lagging was assumed. The St. Agathe location was chosen to be studied in detail because of its close proximity to Winnipeg, the possibility of flicker problems due to farming loads and its representative nature of a typical single phase feeder.

Phase A of St. Agathe feeder SA-1 is shown in Figure 3.1. The compensator is replacing a 50 Amp autobooster which was located at bus 30. Also, an upline 100 Amp step voltage regulator was removed for these studies. A number of assumptions and simplifications have been made in the modelling of the St. Agathe feeder:

1. All loads are at 0.8 power factor lagging
2. There are a number of loads (150 kVA) upline of the compensator which have been removed
3. The voltage at the substation is constant at 1.0 per unit
4. The transmission line is modelled as lumped parameter resistance and inductance elements

A program was written in order to analyze the voltages at the different buses on the feeder under various load conditions. Details of the program are included in Appendix A.

The program allows the user to assume all the loads are either of the constant impedance or constant power variety. Constant current is another type of load which is not included in the program. There is a fundamental difference between each load variety as indicated in Figure 3.2. The constant kVA model is associated with motor loads, constant impedance represents loads such as electrical resistance heating and constant current is a combination of the two. The voltages resulting from each load assumption do not vary significantly. Since the constant impedance load model requires only one calculation (constant power is iterative) and will better model the loads on the analog power system simulator (see Chapter 4) as well as the loads on the feeder, the remainder of this section will refer to loads of this type.

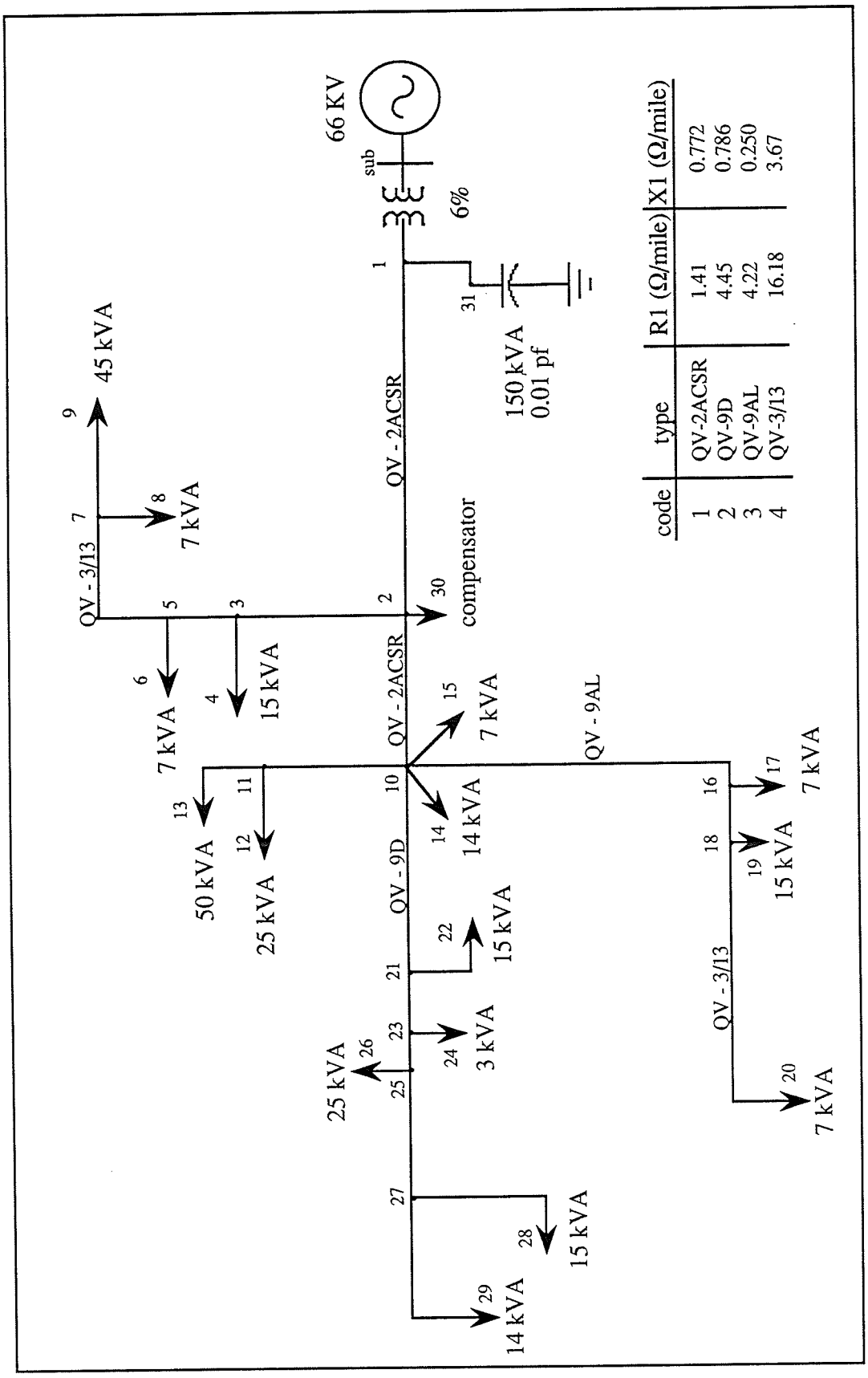


Figure 3.1: *St. Agathe feeder SA-1*

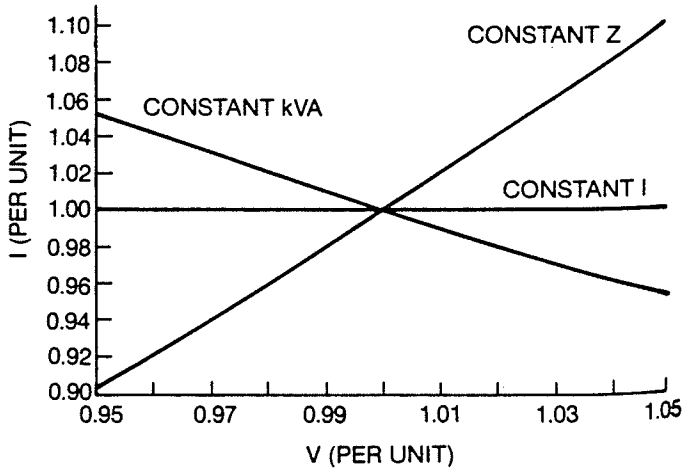


Figure 3.2: *Current as a function of voltage and load [15]*

Many load flow studies were performed on the St. Agathe feeder. A compensator of 250 kVAr was found to regulate the voltage at bus 30 to 1.0 per unit. Appendix A contains computer printouts of voltages and currents without compensation and with 250 kVAr compensation. Figure 3.3 is a voltage profile along buses substation-1-2-3-5-7-9 where bus 9 has the lowest voltage in the feeder. The effects of compensation can clearly be seen in this graph.

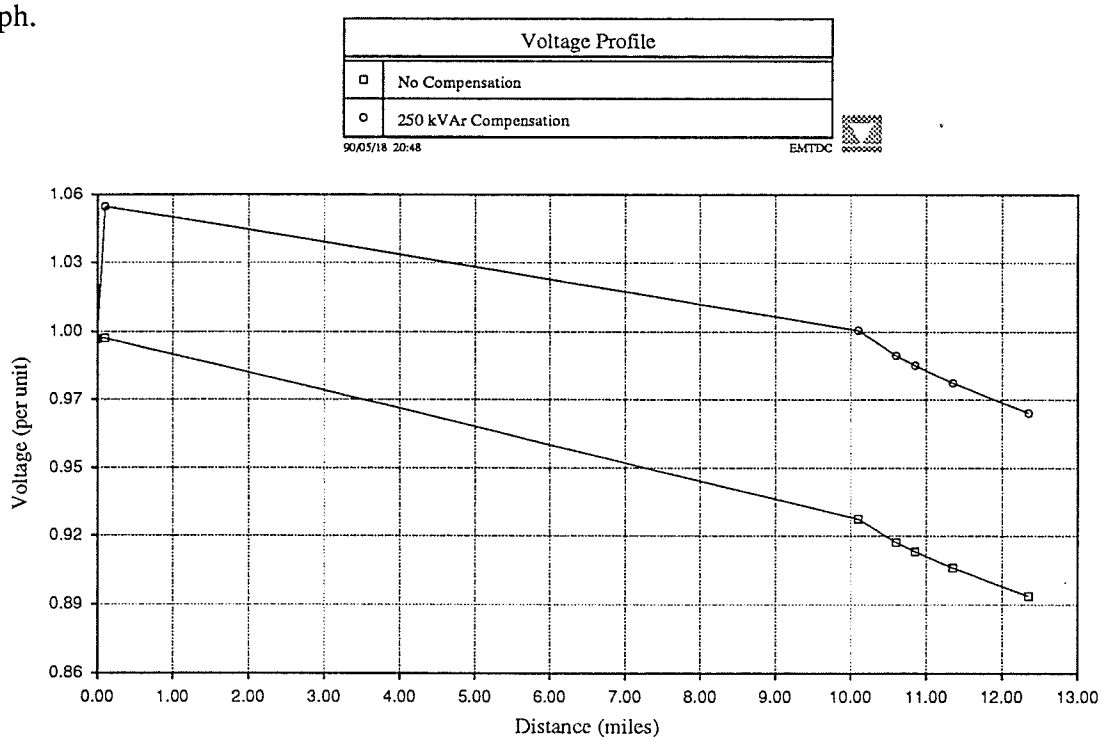


Figure 3.3: *St. Agathe voltage profile*

A simplified feeder model is required for analog and digital simulations to be performed later. The simplified model is shown in Figure 3.4. All loads to the left of the compensator are lumped together as one 197 kVA load. The feeder connected to bus 9 is modelled by one transmission line segment and two loads. The 29 kVA load is the sum of the loads at bus 4, 6 and 8 while the 45 kVA load remains unchanged. Characteristics such as the voltage at the 45 kVA load and the voltage at the compensator remain approximately the same when compared with the more complex model.

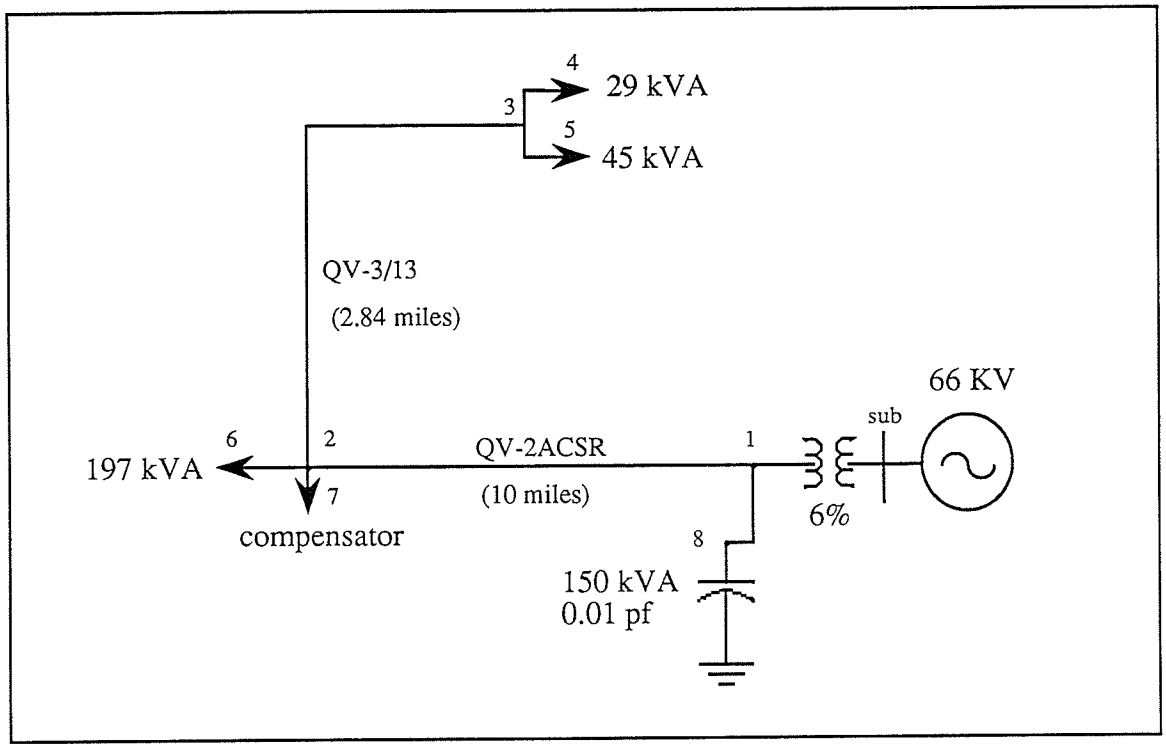


Figure 3.4: *Simplified feeder model*

Three studies were performed on the simplified feeder model. The first was to determine the transmission line losses as a function of the amount of compensation with various load configurations. Load lines for various load conditions were derived next (see Figure 3.12). Finally, the effect of having a more complex load between the compensator and substation was examined.

Figure 3.5 is a graph of transmission line losses (Table 3.5 contains a listing of actual numerical values). Losses are at a minimum when the power factor of the load and compensator approach unity. Once the power factor becomes leading, the losses start to increase.

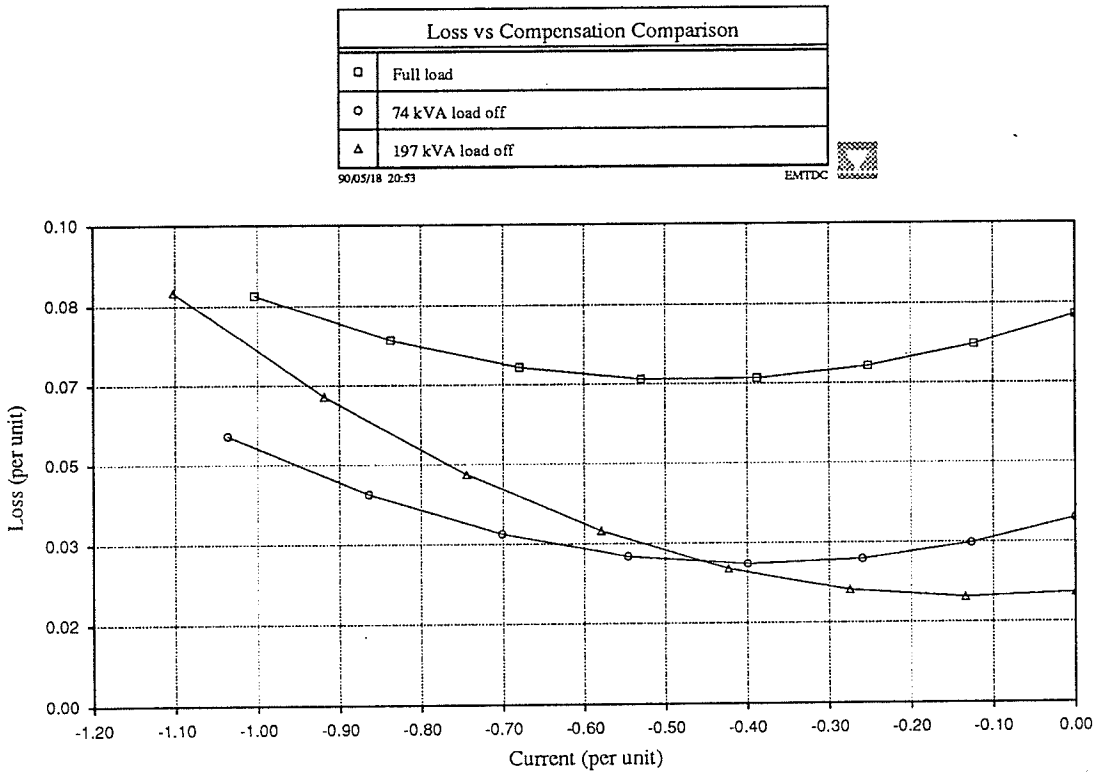


Figure 3.5: *Transmission line loss evaluation*

There are several branch feeders between the compensator and the source which are not represented in the simple system containing an additional 150 kVA of load. If all the loads are included and assumed to be 0.8 pf lagging, the voltage drop at the compensator busbar drops by an additional 5%. More capacitance would be required to regulate the voltage to 1.0 pu. However, if the loads are modified to be 0.95 pf lagging (as is probably the case since most of the loads are electric heating), the voltages at the nodes corresponding to the simplified feeder model are approximately the same with and without compensation.

3.3 Thyristor Switched Capacitor (TSC)

The main components of a TSC are given in Figure 3.7. A reactor is included in series with the capacitor and thyristor-diode switch to limit switching transients, to damp inrush and outrush currents, to protect the thyristor-diode from large di/dt and to detune any harmonic resonance that may occur between the compensator and the system. ON-OFF control of the thyristor-diode switch is used to control the number of capacitor banks which are on and hence, the amount of shunt capacitive reactance.

The voltage at the compensator busbar (V_{svs}) is determined by the intersection of the system load line and the particular compensator characteristic (dashed line) as shown by the operating points in Figure 3.6. Superposed on this figure is the control characteristic of the compensator. The control characteristic indicates the amount of compensation current required to regulate the system voltage for a particular load line.

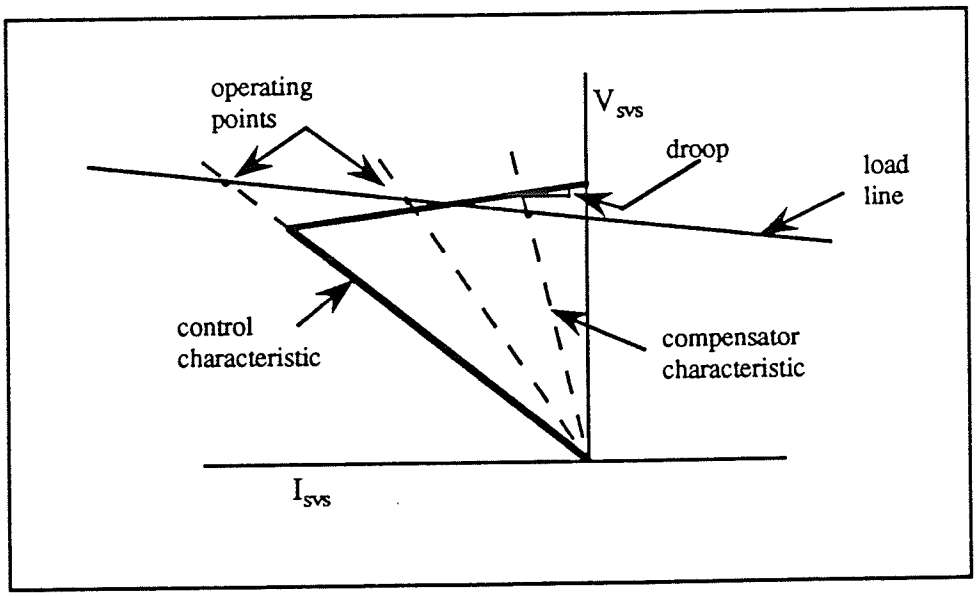


Figure 3.6: *TSC compensator characteristic*

A small positive slope (0%-2.5%) or droop is included in the control characteristic for several reasons. The load line has a negative slope with magnitude depending on the strength

of the system. If the load line is relatively flat and the compensator has a slope of similiar magnitude, a small change in the load line will cause a large jump in compensator current resulting in an unstable operating point. Droop is used to alleviate this unstable situation. It is anticipated that only one compensator will be required on an individual single phase feeder. However, the droop characteristic can be modified to prevent the possibility of two distant compensators from becoming unstable because of their effects on one another. Finally, as was noted in the previous section, the transmission line losses increase once the power factor becomes leading. A small droop will help to reduce the increased losses which develop as a result of voltage regulation.

Now that the basic operating principle of a TSC has been explained, the remaining two sections will describe component selection and control algorithms. Recommended reading for further understanding of the material presented can be found in [27,28].

3.3.1 Component Design

From load flow studies done on the St. Agathe feeder, it was determined that a shunt compensator of 250 kVAr will keep the voltages along the feeder within ± 5 % of nominal. There are many possible combinations of capacitors that will provide the required compensation. Some possibilities are:

1. 7 banks: 35.7 kVAr each
2. 3 banks: 35.7, 71.4, 142.8 kVAr
3. 4 banks: 16.7, 33.4, 66.8, 133.6 kVAr

Most TSC installations use a number of capacitor banks of the same rating. In high voltage applications, the number of shunt capacitor banks is limited to 3 or 4 [31,32] because of the high cost of thyristor switches, whereas at distibution level voltages the number of banks can exceed 12 [17]. Due to space and cost, it is much more economical to use fewer banks of different ratings. The table below illustrates the compensation gained with an 8 step binary design.

Table 3.1:

Compensation of 8 Step Compensator

Capacitor bank # 3	2	1	Comp. (kVAr)
0	0	0	0.0
0	0	1	35.7
0	1	0	71.4
0	1	1	107.1
1	0	0	142.8
1	0	1	178.5
1	1	0	214.2
1	1	1	250.0

Bank #	(kVAr)
1	35.7
2	71.4
3	142.8

If the transformer has a sufficiently high kVA rating, the compensation level of the 3 bank scheme can be doubled by the addition of one more capacitor. However, in order to double the compensation of the first scheme 7 banks must be added.

The three bank scheme will be designed and studied in detail because it meets the reactive power requirements and has approximately a 1% voltage change per step (from Eqn. 3.2 and load flow studies). If more dynamic range and finer voltage steps are required, a 4 or 5 bank capacitor may be designed following the same procedure.

The primary and secondary base values that will be used on the St. Agathe system are summarized below:

Primary Base Values	Secondary Base Values
S_1 = 250 kVAr	S_2 = 250 kVAr
V_1 = 7200 V	V_2 = 600 V
I_1 = 34.72 A	I_2 = 416.67 A
Z_1 = 207.36 Ω	Z_2 = 1.44 Ω
B_1 = 0.00482 S	B_2 = 0.6944 S

A one line diagram of the three bank TSC compensator is shown in Figure 3.7.

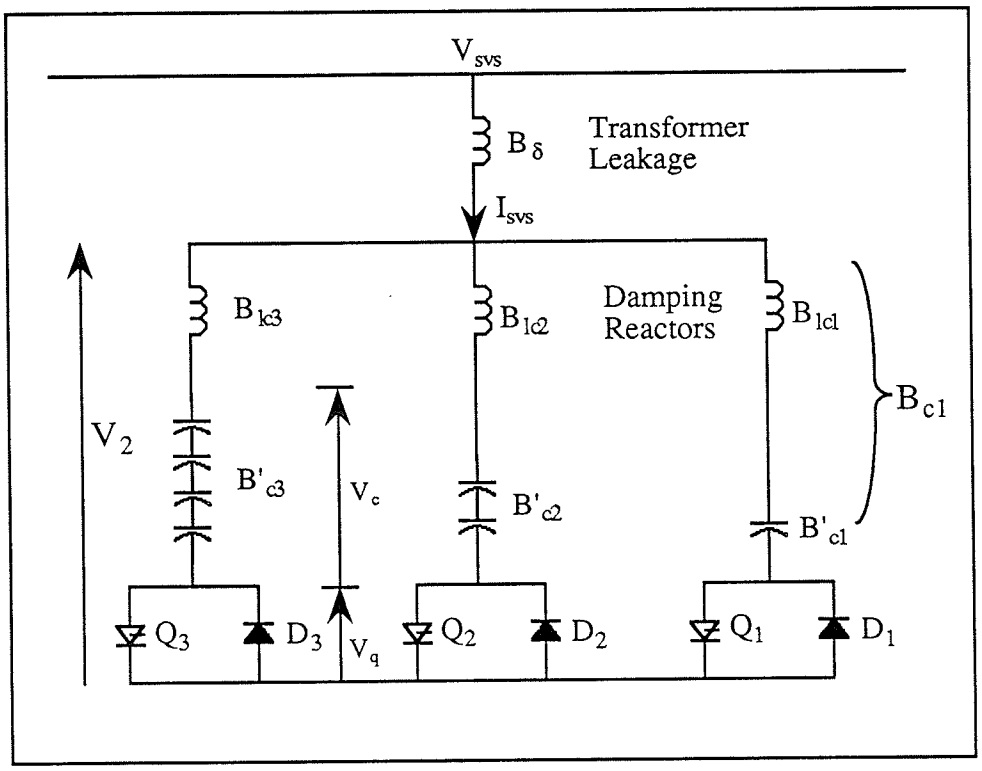


Figure 3.7: *TSC one line diagram*

The transformer leakage is a variable that must be known accurately before proceeding with the design. Typical values of leakage are between 1% and 25%. The larger the leakage the larger the secondary voltage, and therefore the reverse voltage blocking capability of the thyristor must be higher. A leakage of 10% is assumed in the calculations which follow.

Using the value of assumed leakage and a value of 1.0 pu for the total system susceptance (B_{svs}), the total shunt susceptance of the capacitor branches (B_c) can be calculated by using Equation 3.4. The resulting susceptance is 0.90909 per unit (pu).

$$B_{svs} = B_\delta B_c / (B_\delta + B_c) \quad (3.3)$$

$$B_c = - B_{svs} B_\delta / (B_{svs} - B_\delta) \quad (3.4)$$

There are two possible ways of proceeding. One approach is to assume equal total compensation (B_{svs}) per step and the other is to assume equal capacitor bank (B_c) steps. The susceptances are summarized in the following table.

Table 3.2:

Compensator Susceptance Summary

(a)

Bsvs	Bc Eqn 3.4	Total Comp.
0.00000	0.00000	0.000
0.14286	0.14085	35.715
0.28572	0.27778	71.430
0.42858	0.41095	107.145
0.57144	0.54054	142.860
0.71430	0.66667	178.575
0.85716	0.78947	214.290
1.00000	0.90909	250.000

(b)

Bc	Bsvs Eqn 3.3	Total Comp.
0.00000	0.00000	0.000
0.12987	0.13158	32.895
0.25974	0.26667	66.668
0.38961	0.40540	101.350
0.51948	0.54794	136.985
0.64935	0.69444	173.610
0.77922	0.84507	211.268
0.90909	1.00000	250.000

Using the equal total compensation assumption (Table 3.2a) results in capacitor bank steps which are unequal, and therefore there is no way of having a simple 3 bank switching scheme. A much better approach is to assume equal capacitor bank steps. The control logic will be simpler with the only drawback being the slight variance in the size of each compensation step. (An effect that will be hardly perceptible as demonstrated by Fig. 2.1)

A damping reactor is required in each capacitor branch to protect the thyristor-diode from excessive rate of change of current (di/dt). On startup or after fault clearing, an infinite rate of change of current can be expected through the diode without any inductance in the circuit. The reason being the capacitors are not charged and therefore appear as a short circuit, initially, to the power supply. Some protection is offered against excessive di/dt by the transformer leakage in this case. However, switching a capacitor bank can cause large di/dt in adjacent capacitor branches rendering the protective influence of the transformer leakage ineffective.

The minimum amount of inductance required to limit di/dt to 100 A/μs when the secondary voltage (V) is equal to 600 volts is found using Equation 3.5. An inductance of at least 0.22% is required.

$$\sqrt{2}\ V = L\ di/dt \qquad (3.5)$$

The value of inductance should not be too large because as indicated earlier the voltage magnification factor increases with increasing inductance, thereby, increasing the required reverse blocking voltage capabilty of the thyristors. In addition, for transient free switching, the thyristors must be gated when the supply voltage is at its peak and the capacitor is precharged to this voltage multiplied by the voltage magnification factor [25,28]. A small value of inductance will reduce the capacitor precharge requirement.

The strategy used to keep the capacitor precharged to a specific voltage crest is to employ a diode in antiparallel with the thyristor. Antiparallel or back-to-back thyristors are available commercially as single packaged units. The gating pulse of one of the thyristors simply has to be tied high in order for the device to emulate a diode. As well, antiparallel thyristor-diodes are now commercially available.

Switching a capacitor with series inductance will result in transient currents composed of fundamental and natural frequencies. The amplitude of the fundamental component is given by Equation 3.6 [25].

$$\hat{i} = \hat{V} B_c \frac{n^2}{n^2 - 1} \qquad (3.6)$$

where; $B_c = \omega C$, $n = \sqrt{\frac{X_c}{X_l}}$ (3.7)

The term $n^2/(n^2-1)$ is a magnification factor (VMF) due to the series tuning of the L-C circuit. Capacitor voltage is equal to the magnification factor multiplied by the peak voltage (3.7).

$$V_c = \hat{i}\, X_c = \hat{V} \frac{n^2}{n^2 - 1} = \hat{V}\,(\mathrm{VMF}) \qquad (3.8)$$

The largest voltage across the capacitors occurs when all of the capacitor banks are switched in. The strategy used in this study is to limit the VMF in this case to 1.125 or in other words the capacitor must be pre-charged 12.5% larger than the primary voltage for transient free switching. Table 3.3 summarizes the effects of various values of natural frequency (n) on the magnification factor and total series inductance (transformer leakage and parallel combination of damping reactors). It should be noted that Table 3.3 is only to

be used for the case of full capacitance (all banks switched in). As each capacitor bank is switched off, the amount of capacitance is reduced, hence the per unit natural frequency of the total current increases thereby decreasing the voltage magnification factor. Figure 3.8 (b) serves to illustate.

In order to limit the VMF to 1.125, the total series inductance must be limited to 12.5% (Table 3.3). Given a transformer with 10% leakage will result in the parallel combination of damping reactors being equal to 2.5%. By setting Xl equal to this value, the per unit natural frequency of current in each branch is calculated to be 6.7 (Eqn. 3.6).

Table 3.3:

Summary of Resonant Frequency Variation on Voltage Magnification Factor and Total Inductance

n	VMF Eqn 3.7	Xl % Eqn 3.8
2	1.33333	33.333
3	1.12500	12.500
5	1.04166	4.160
7	1.02080	2.080
9	1.01250	1.250

The remaining components may be designed using equations 3.9 to 3.12. A summary of the component values is contained in Table 3.4.

$$B_c' = [(n^2 - 1)/n^2]\ B_c \qquad (3.9)$$

$$C = B_{2base}\ B_c' / w \qquad (3.10)$$

$$B_{lc} = -n^2\ B_c' \qquad (3.11)$$

$$L = 1 / (w\ B_{lc}\ B_{2base}) \qquad (3.12)$$

where: n = 6.7
w = 376.99 rad/second

Table 3.4:

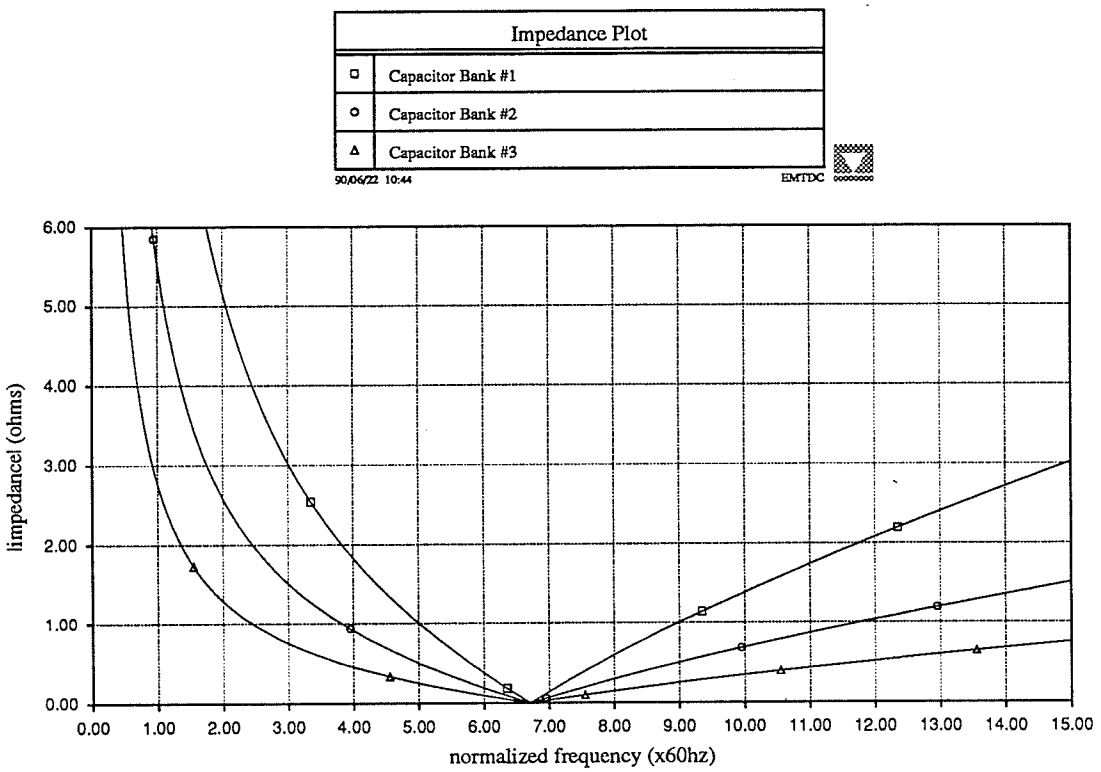
Summary of Component Values

Bank #	Bc (pu) Tab 3.2b	Bc' (pu) Eqn 3.9	C (uF) Eqn 3.10	Blc (pu) Eqn 3.11	L (mH) Eqn 3.12
1	0.12987	0.12698	233.893	-5.7143	0.66850
2	0.25974	0.25397	467.786	-11.428	0.33425
3	0.51948	0.50794	935.572	-22.857	0.16712

Using the values calculated in Table 3.4, a harmonic analysis was performed as a check for accuracy. The compensator was designed so that the lowest tuned frequency seen by the system would be the third with all capacitor banks switched in. In order to achieve this, each capacitor bank was tuned to the normalized frequency of 6.7. Figure 3.8(a) clearly shows that each bank is tuned to the correct frequency. Resonance at the third harmonic with all capacitor banks switched in is verified in Figure 3.8(b). The resonant frequency increases to approximately the fifth as the number of banks is reduced to one.

The rating of the thyristor-diode switch shown in Figure 3.7 may be determined next. By examining the theoretical waveforms of voltage and current drawn in Figure 3.9, with the thyristor blocking and conducting, the device ratings may be found. At time t_1, the thyristor Q_3 (chosen from Fig. 3.7 as an example) turns off because the current has become negative. Due to the orientation of the thyristor-diode switch, the diode allows current to conduct in the negative direction. Finally, at time t_2, the diode becomes reverse biased and the switch is open. The current (I_{svs}) may or may not be reduced to zero depending on the conducting state of the other two capacitor branches. However, the current definitely ceases to conduct through branch 3. At this time the capacitor is charged to the RMS value of -1.125 pu. The thyristor-diode must be able to block the difference between the secondary voltage and capacitor voltage which can be as high as [(1.1+1.125)*$\sqrt{2}$ pu] or 1888 volts. If all of the banks are blocking, as is the case in Figure 3.9, then the secondary voltage is equal to the primary voltage (in pu values) and the required blocking ability is reduced to 1800 volts. The capacitor voltage decays according to the RC time constant of the circuit. Once the capacitor voltage decays slightly below the secondary voltage, the diode will conduct to keep the capacitor precharged.

(a)



(b)

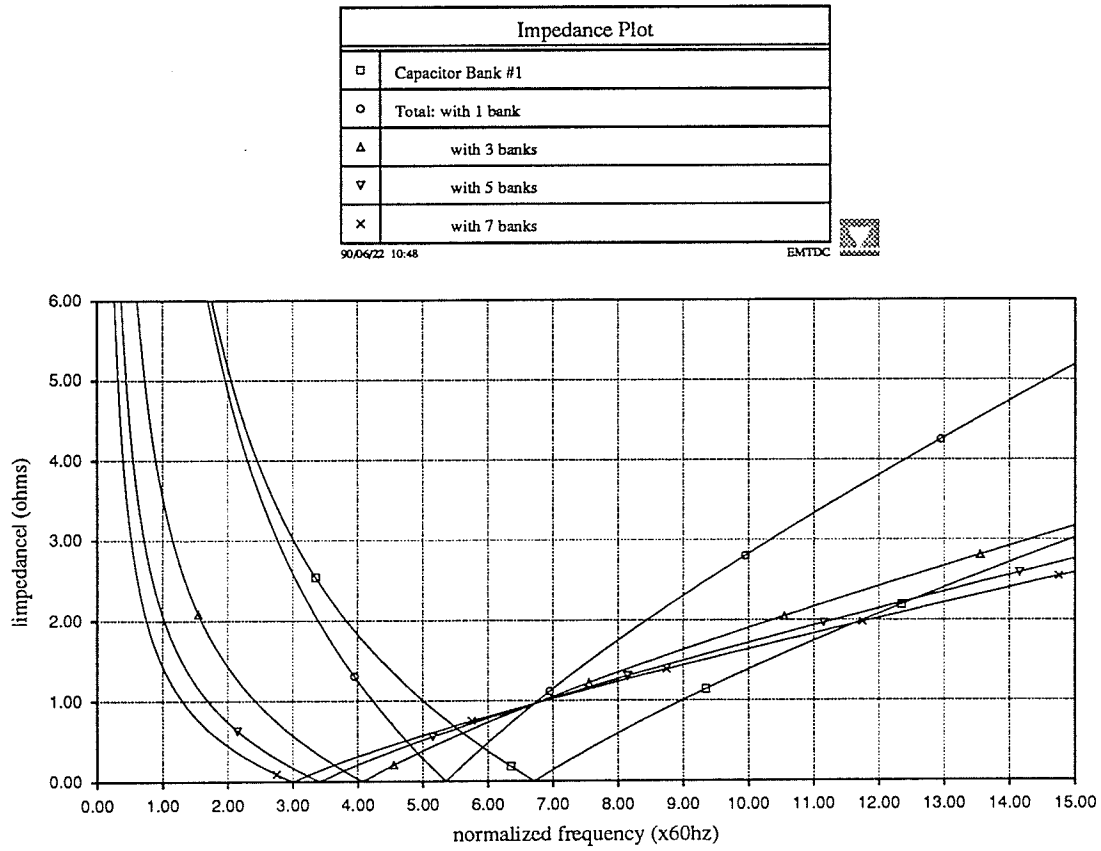


Figure 3.8: *Harmonic analysis of (a) capacitor branches, (b) entire compensator*

Assuming the system voltage is 1.0 pu and all of the thyristor-diode switches are blocking, the thyristor must be capable of blocking 3 pu (2.125*√2) or 1800 volts as indicated in Figure 3.9. A safety margin of 0.5 pu will be added to insure voltage blocking capability in case of system overvoltage or capacitor overcharging. Therefore, the peak repetitive voltage rating for each thyristor switch is 2100 Volts.

Each shunt branch carries a different portion of the total system current. Three different thyristor switches can be designed based on different current ratings, however designing only one thyristor switch having maximum current rating is advantageous. Some advantages are that fewer spare parts need to be stocked and there is less chance of failure due to errors in manufacturing (i.e. the wrong capacitor bank-switch matchup). The current rating of each thyristor switch is 0.51948 pu plus 15% for safety or 250 Amps. More detailed design specifications as well as an economic evaluation are included in the CEA Project 247-D-681 final report.

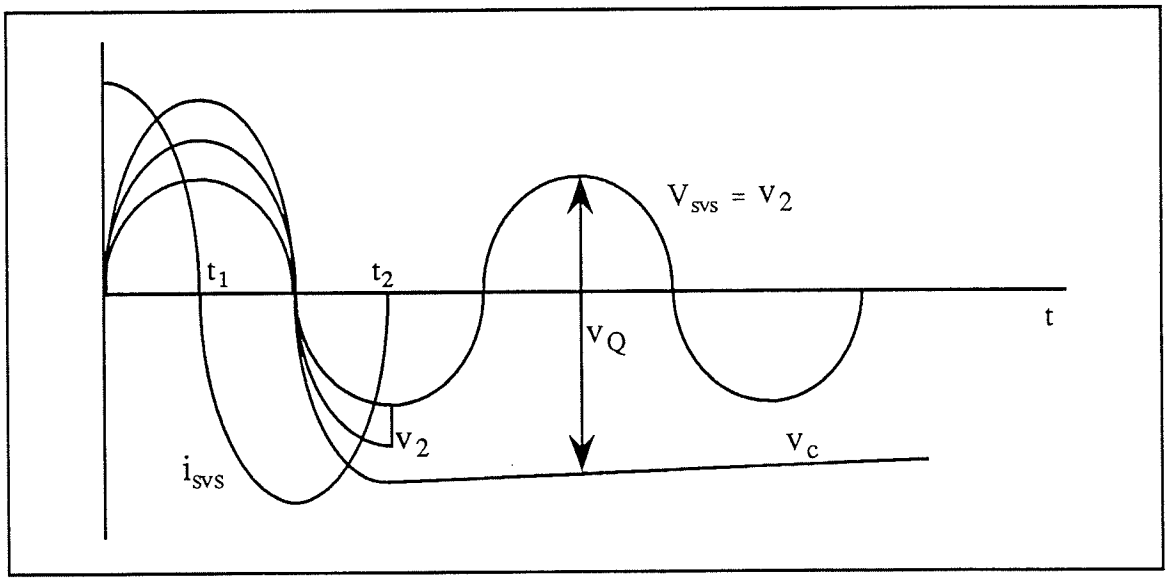


Figure 3.9: *Theoretical current and voltage*

3.3.2 Control Algorithm

There are two basic control strategies which may be used in the design of a compensation device for a power system. The strategies are a closed loop or feedback type and an open loop or feedforward type.

A feedforward scheme is mainly used in 3 phase load compensation. The required individual phase currents are calculated directly and the appropriate shunt reactance added. For balancing loads which vary rapidly and asymmetrically such as arc furnaces, a fast feedforward scheme is the only practical solution [34].

Feedback schemes are typically used to regulate terminal voltage. The voltage is measured and compared with a reference. The resulting error is reduced to a minimum by adding or reducing the shunt reactance. A feedback scheme is very accurate and not susceptible to changes in system or control elements. Figure 3.10 shows a block diagram comparing the feedforward and feedback control schemes.

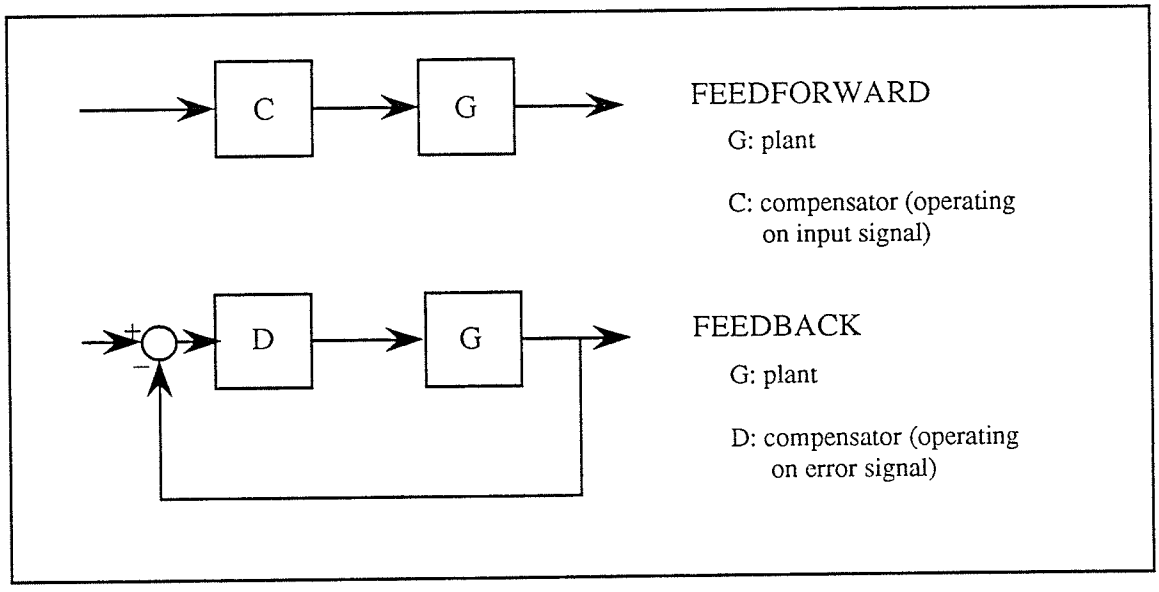


Figure 3.10: *Feedback and feedforward comparison*

The main purpose of the compensation device being described in this report is to replace the currently used step voltage regulators, autoboosters and switched capacitors. A significant voltage variation is allowed by these devices due to the time delay between voltage sensing and control action. Typical time delays are between 30 and 90 seconds for a step voltage regulator and between 15 and 120 seconds for a switched capacitor. Under normal system conditions our compensator should regulate the system voltage to some predetermined reference level. A feedback control system is perfectly adequate in this case. However, under certain system conditions such as machine starting or arc welding the addition of a faster feedforward scheme may be required to be added to reduce voltage flicker.

A simple model of the power system is needed in order to test the control algorithm and associated parameters. The power system is represented by a source voltage (E) in series with an equivalent system reactance (X_e) as shown in Figure 3.11.

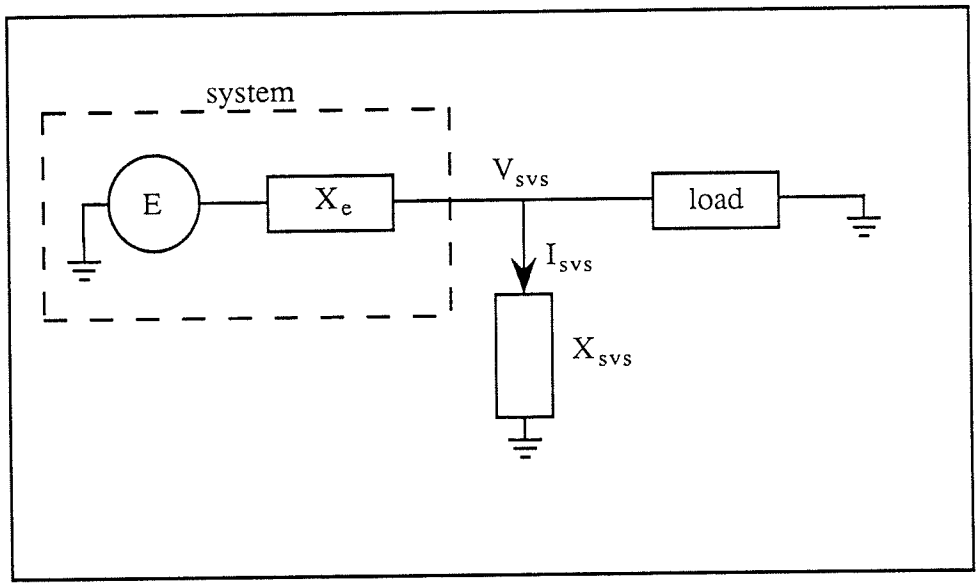


Figure 3.11: *Equivalent model of system*

A load flow program was developed (Appendix A) and may be used to determine E and X_e for various load conditions. With reference to the Simplified Feeder Model reproduced in Figure 3.12, the three load conditions are:

1. Full Load

2. Switch 3 Open (74 kVA load off)
3. Switch 4 Open (197 kVA Load off)

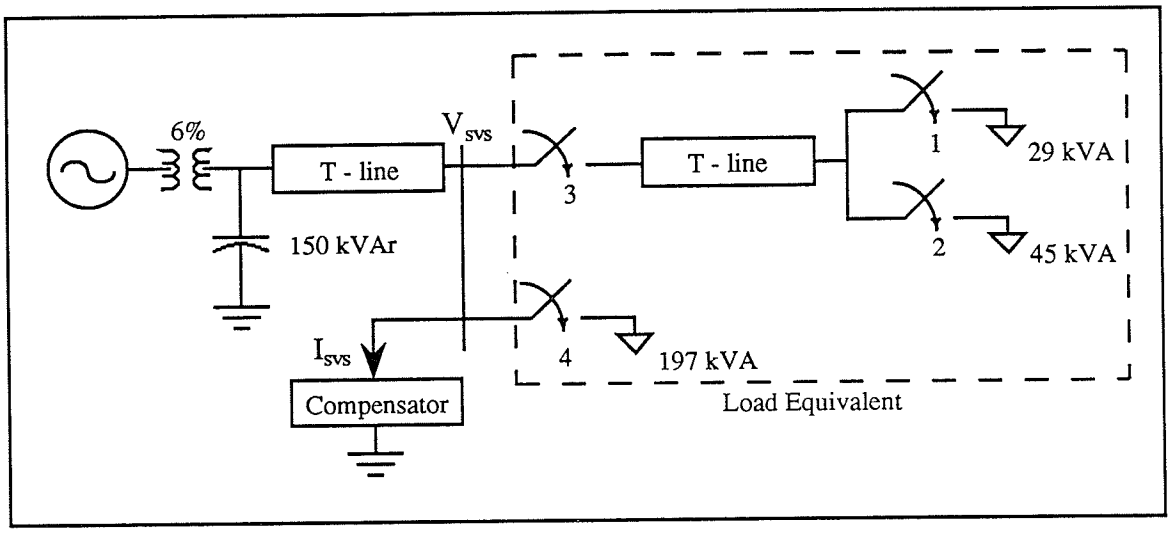


Figure 3.12: *Simplified feeder model*

Steady state voltage on the busbar (V_{svs}), compensator current (I_{svs}), and total system losses are recorded for each capacitor bank being switched into the system during each load condition. Table 3.5 summarizes the results. The equivalent system voltage and reactance (in pu) found for each load condition are:

1. Full load: E = 0.924367 X_e = 0.07897
2. 74 Kva off: E = 0.951401 X_e = 0.08196
3. 197 Kva off: E = 1.005587 X_e = 0.08782

Each load line, as well as the compensator characteristic, is graphed in Figure 3.13. It is instructive to examine this diagram carefully. For example, say we are operating with 197 kVA load off (condition 3) and suddenly the load is switched on. One can observe from the diagram that the initial voltage is 1.0 pu and will immediately dip to 0.925 pu since the compensator current is zero. The controls will take effect and gradually switch on 7 banks of capacitors bringing the voltage back up to 1.0 pu.

Table 3.5:

Load Flow Analysis on Simplified Feeder

Comp. (kVA)	Full Load			74 kVA off			197 kVA off		
	Vsvs	Isvs	Loss	Vsvs	Isvs	Loss	Vsvs	Isvs	Loss
0.00	.924	.000	.081	.951	.000	.038	1.01	.000	.023
32.90	.934	.123	.075	.962	.127	.033	1.02	.134	.022
66.67	.944	.252	.070	.973	.260	.030	1.03	.275	.023
101.35	.956	.387	.068	.985	.399	.029	1.04	.423	.028
136.99	.967	.530	.068	.997	.546	.031	1.06	.579	.036
173.61	.979	.680	.070	1.01	.701	.035	1.07	.744	.048
211.27	.991	.837	.076	1.02	.864	.044	1.08	.918	.064
250.00	1.00	1.00	.085	1.04	1.04	.056	1.10	1.10	.086

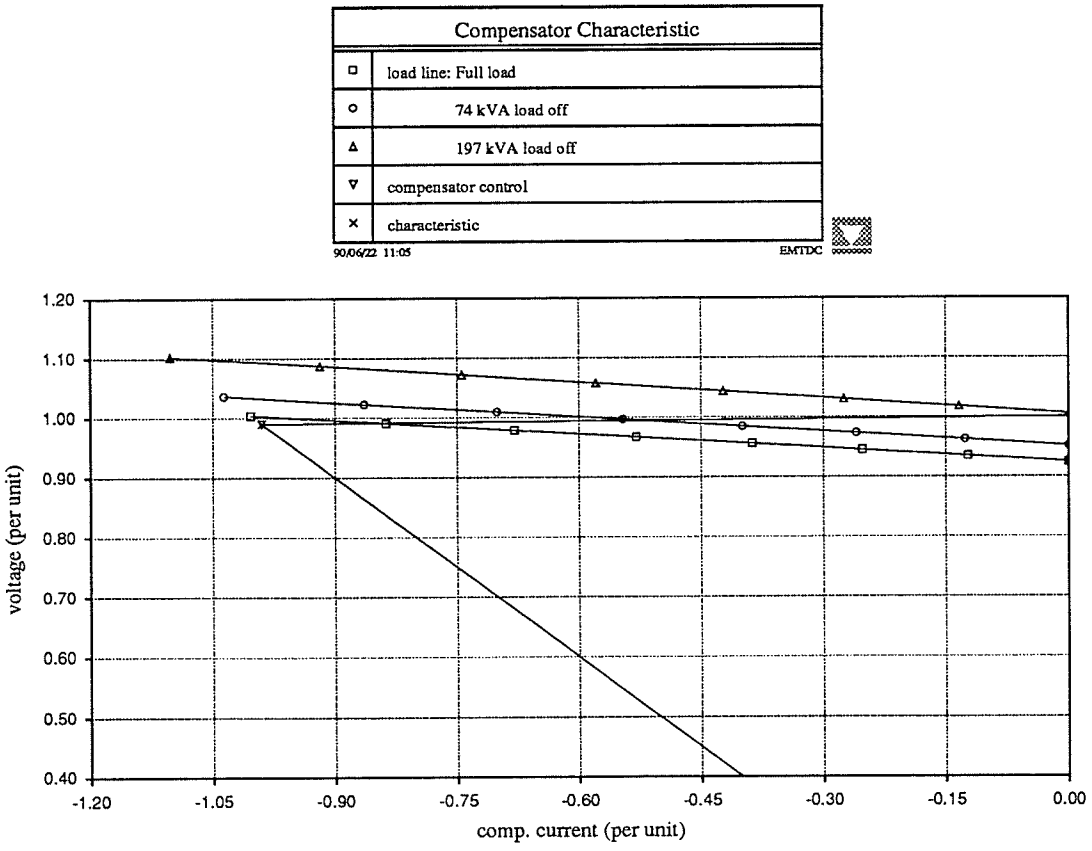


Figure 3.13: *Compensator characteristic*

A simple feedback control scheme is shown in block diagram form in Figure 3.14. Proportional Integral (PI) control was chosen to convert the voltage error signal into compensator current (I_{svs}). A desirable feature of PI control is the ability to reduce the steady state error to zero. The discrete capacitor switching events are not included in the simple model.

TUTSIM [42], a control system modelling program, was used to test the operation of the system. Using a droop of 0.1%, proportional and integral gains of 4 and 400 respectively (found by trial and error), and a system reactance of 0.0819, a disturbance (δE) was applied to the system. The disturbance is attempting to model a motor starting. A 5% dip in voltage lasting for 0.5 seconds occurs at the instant time is equal to 2.0 seconds. System voltage (V_{svs} or channel 1) and compensator current (I_{svs} or channel 2) following the disturbance are shown in Figure 3.15. The voltage returns to the reference setting as expected.

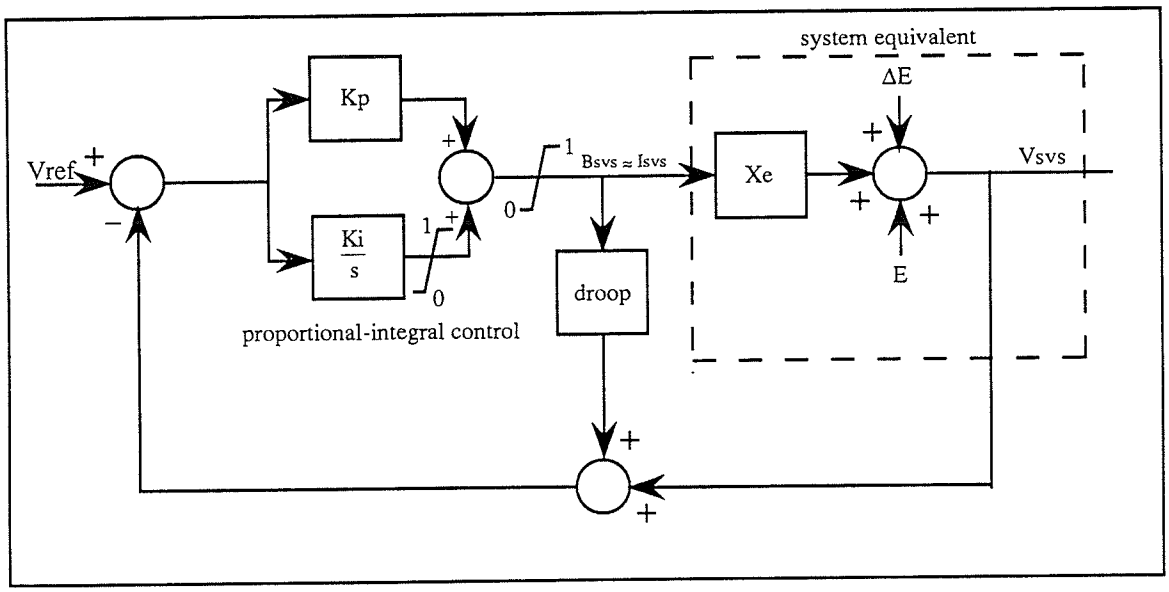


Figure 3.14: *Control block diagram of simple system*

Now that the concept has been shown to work, a more detailed model needs to be described that more accurately represents the real system. Specifically, the following points will be discussed: measurement, control and protection.

The quantities that need to be measured are the system voltage (V_{svs}) and system current (I_{svs}). If the transformer leakage reactance and the impedance of each branch of shunt

reactance are known accurately, only the secondary voltage (V_{2rms}) will need to be measured. Using Kirchoff's current law, equation 3.13 may be derived.

$$V_{svs} = (1 + B_o/B_\delta)\ V_{2rms} \tag{3.13}$$

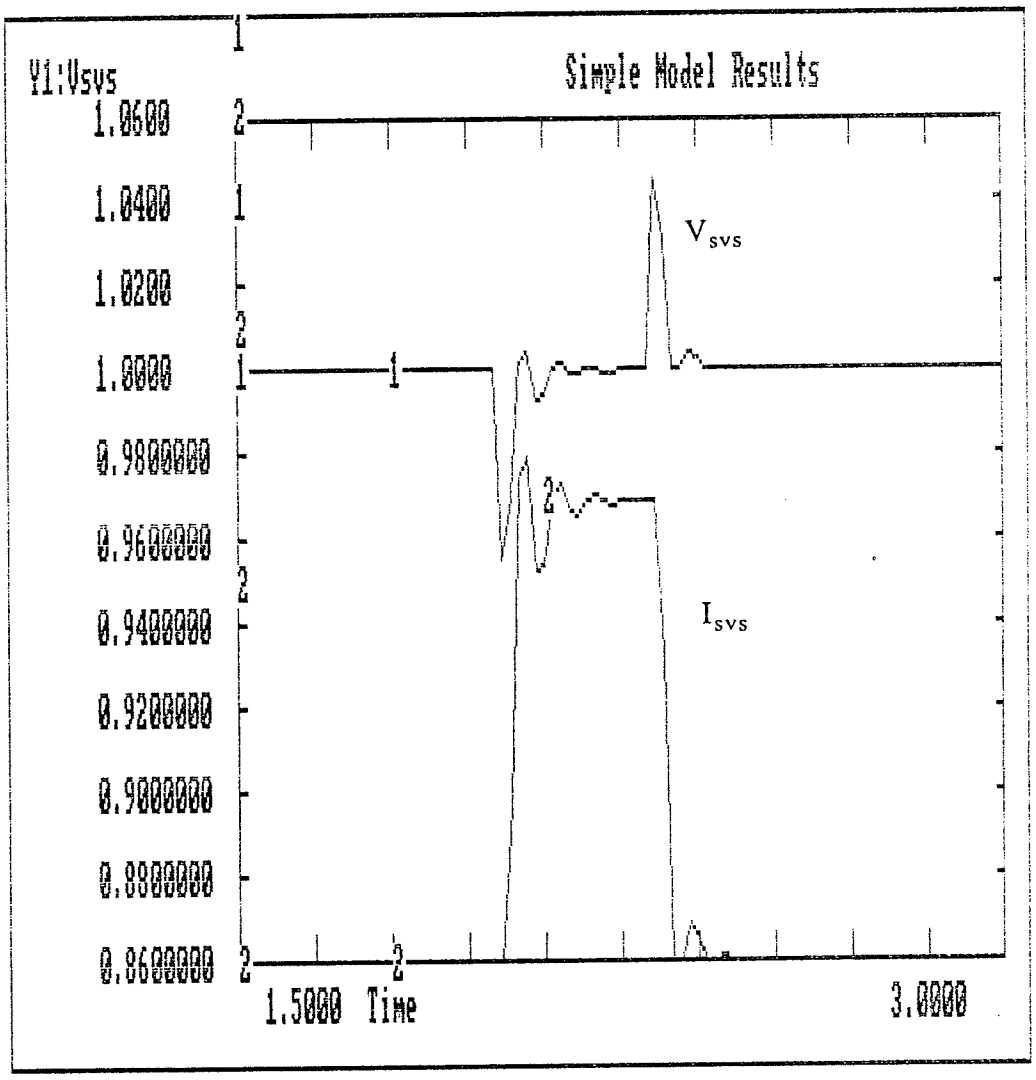


Figure 3.15: *TUTSIM simulation of simple control system*

The advantage of only measuring the secondary voltage is the reduction in total cost. Primary voltage and current could be measured at the expense of adding instrument transformers and analog-to-digital converters.

Since a TSC's control characteristic is discontinuous or stepwise, it is very likely the system load line will lie between two possible operating points. The control system as described earlier will switch back and forth between capacitor banks or hunt around the operating point possibly creating a voltage flicker problem. One solution is to add a deadzone. The worst case condition exists if the load line lies exactly in the middle of two operating points. The error will remain constant at 0.5% while switching back and forth between capacitor banks. In order to alleviate the problem of hunting, the deadzone should be set to a value between 0.5% and 1%. If the error is within the preset limit (0.8% for example), a zero is sent to the PI controller. The capacitor banks which are currently on will be locked on until the error exceeds the set threshold.

The output of the PI controller is the desired total susceptance (B_{svs}). Desired capacitance must be calculated using the value of transformer leakage, after which the desired capacitance is discretized and the number of capacitor banks determined. From the number of capacitor banks (0-7), it is quite easy to come up with a binary signal which may be used to fire the thyristors.

The control algorithm must be able to react accordingly to conditions of severe under- and overvoltage. If the system voltage exceeds the reference setting, the compensator will shut itself off (0.0 kVAr compensation) through control action. However, if a low impedance line-to-ground fault occurs somewhere between the compensator and the substation, an undervoltage condition will exist. Upon clearing of the fault, the compensator will have all of its banks switched on and a large overvoltage will result. The reason being the voltage error signal is large (1 pu). A solution to this problem is to monitor the secondary voltage before a firing order is given. If the voltage falls below 0.7 pu, a fault must have occurred. All banks will be switched off and remain off for 2 cycles following the fault clearing. In order for the current to ramp up slowly, the integrator must be zeroed or cleared and the error signal must be set to zero.

A conceptual design of the controller that more closely represents the real system is displayed in Figure 3.16.

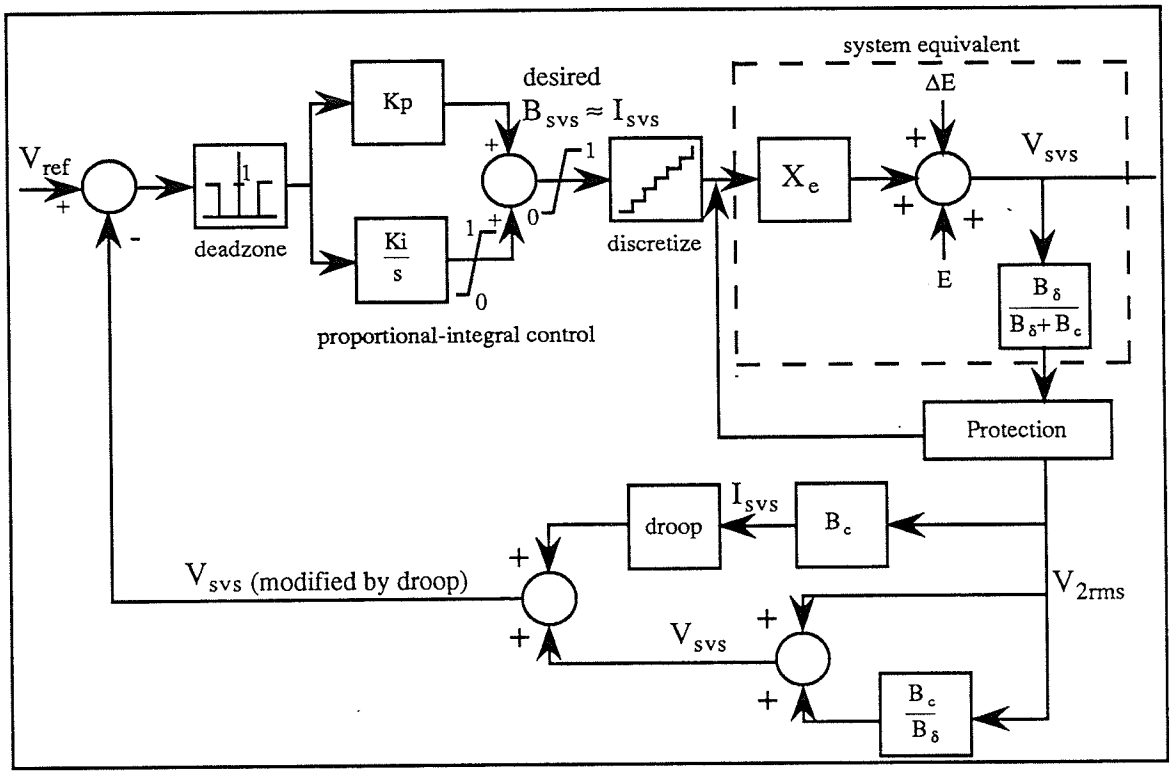


Figure 3.16: *Conceptual block diagram of real system*

Additional control signals have been proposed and adopted in the field for a number of purposes including:

1. Control instability detection
2. Reactive power control and co-ordination
3. Power oscillation damping
4. Subsynchronous resonance damping

The last two control problems are applicable to large installations (hundreds of MVAr) only, however, the first two problems deserve further explanation. If the distribution system is subject to frequent and wide variations in system impedance, the preset proportional and integral gains may lead to unwanted control oscillations [27]. In this case a detection circuit

may be added which will automatically adjust the gains until the compensator is stable. Field measurements on the real system would have to be performed to determine whether or not this feature is required.

Our compensator is designed to replace the step voltage regulators, autoboosters and mechanically switched capacitors currently in use. Due to the speed of response and prevailing system conditions, our compensator can operate at the extremes of its compensation range. In such a case, the compensator is not capable of correcting small or large disturbances in voltage. A slow acting VAr control loop can be incorporated to bring the compensator to a set reference VAr output [30] (middle of the control characteristic, for example). The resulting change in voltage can be corrected for by slower devices still in use on the feeder.

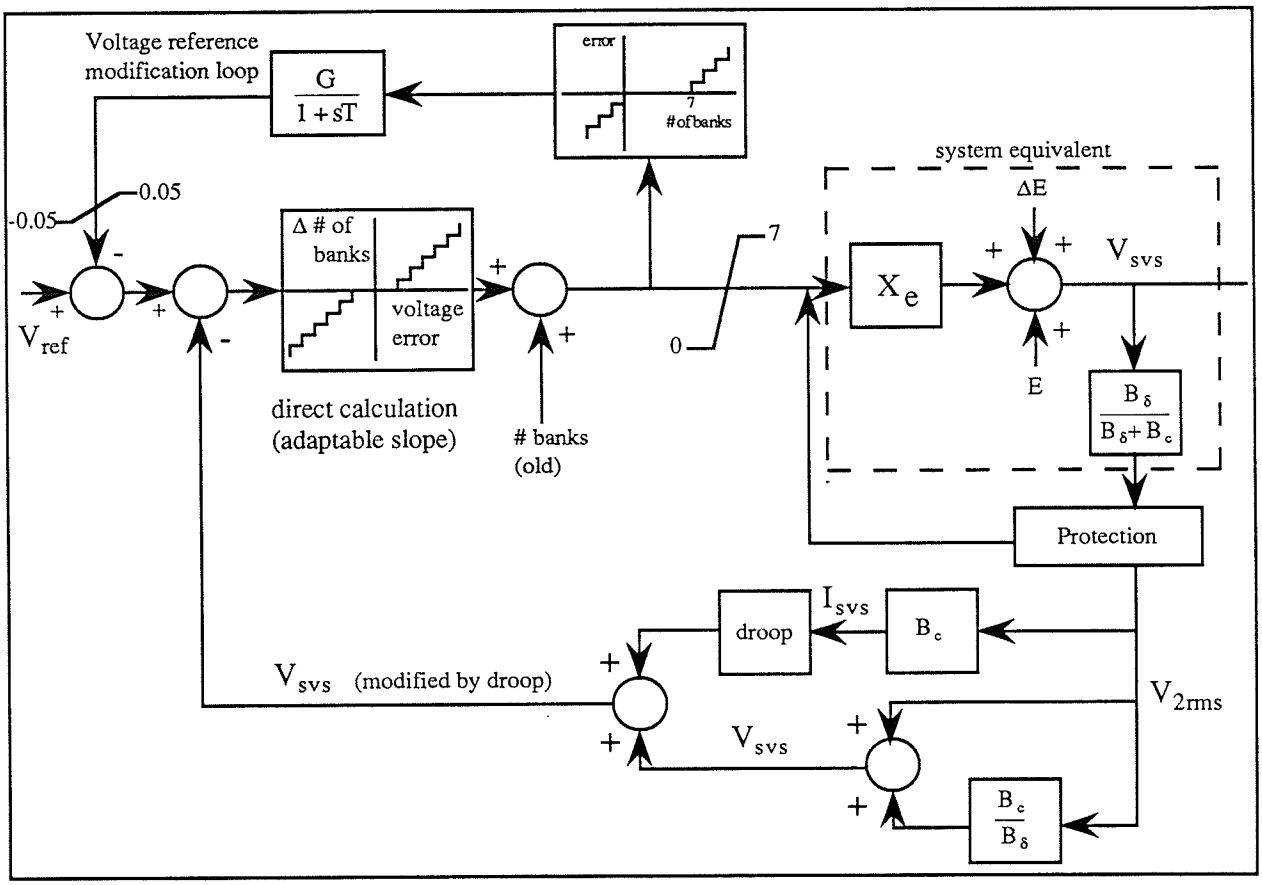


Figure 3.17: *Block diagram of "direct calculation" control algorithm*

An alternative to proportional-integral control that will be better able to compensate for voltage flicker is shown in Figure 3.18. The new "direct calculation" method is similiar in structure to the PI controller in Figure 3.16 except for the direct calculation block and extra feedback loop for reference voltage modification. From load flow studies, it was determined that each capacitor bank step will produce approximately a 1% voltage change. Therefore, a voltage deviation of up to 7% can be corrected directly in two cycles as compared with 4 to 10 cycles with PI control. Also, if flicker is occurring outside of the compensator's normal regulation range, the reference voltage can be automatically raised or lowered to correct for flicker, as an alternative to reactive power co-ordination. Once the flicker condition no longer exists, the reference voltage will return to the preset value.

3.4 Voltage Source Inverter (VSI)

A voltage source inverter consists of a transformer, filters, a dc-ac force commutated inverter and a capacitor (see Fig. 3.18). The operating principle of a VSI is significantly different from the thyristor switched capacitor described in Section 3.3. The output voltage from the inverter is kept in phase with the system voltage. By varying the magnitude of the inverter voltage, a leading or lagging current flows through the leakage reactance of the transformer. In other words, the VSI can be made to absorb or supply VArs in a manner conceptually similar to that of a synchronous condensor.

Continuous control of the system voltage can be achieved by using a VSI at the expense of producing harmonics (harmonics will be fully described in the next section covering component selection). Figure 3.19 contains the control characteristic of a VSI. The operating point is determined by the intersection of the system load line with the particular constant current characteristic of the compensator. Current is continuously variable even though only a discrete number of constant current lines are shown. Constant current is maintained by keeping a constant voltage difference between the inverter output voltage and the system voltage.

For system voltages below that of the per unit leakage reactance of the transformer, the compensator can no longer generate maximum current. The current falls in proportion to the voltage with a slope equal to the transformer leakage. The ability to support the voltage during conditions of severe undervoltage is much better when using a VSI as opposed to a TSC (compare Fig. 3.19 with Fig. 3.6).

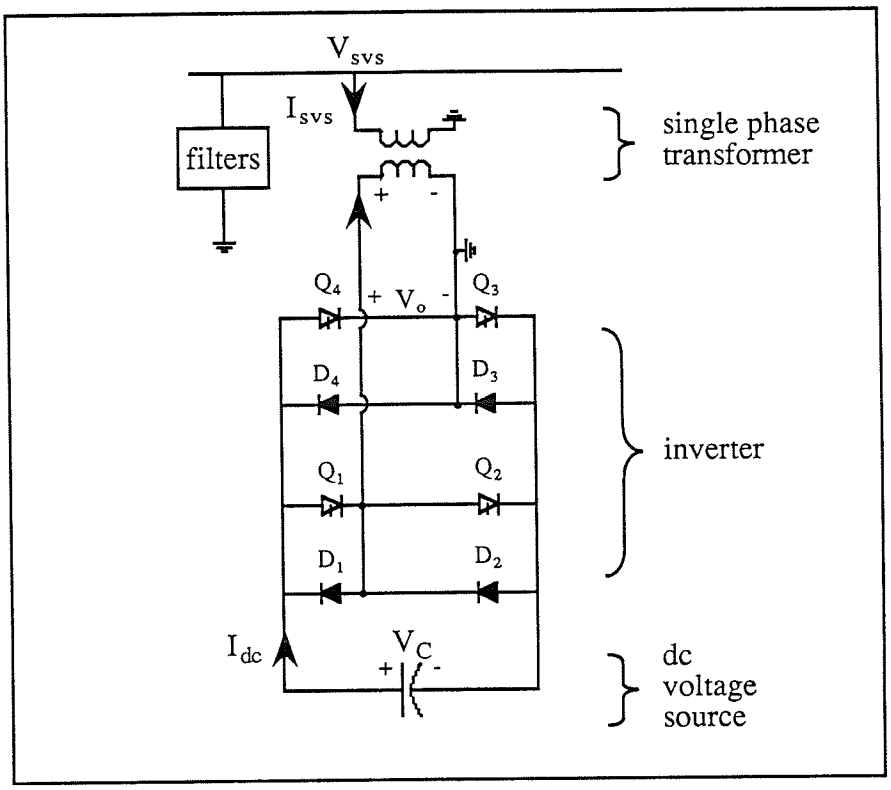


Figure 3.18: *Equivalent circuit of single phase VSI*

Recommended reading for further understanding of the basic characteristics of a VSI can be found in [20,21,27]. In the next two sections, component design and control algorithms for the voltage source inverter will be discussed.

3.4.1 Component Design

The major components of a single phase voltage source inverter are included in Figure 3.18.

In order for comparisons to be made between the TSC and VSI, base values, compensation requirements and transformer rating will be made to be identical. A 250 kVAr capacitive compensator is required on the St. Agathe feeder. A VSI provides both capacitive and inductive compensation, therefore, the compensator must be biased by 125 kVAr of shunt capacitors. The capacitors will contain enough series inductance to eliminate the appropriate harmonics. A ±125 kVAr voltage source inverter will then provide the remaining VAr requirement.

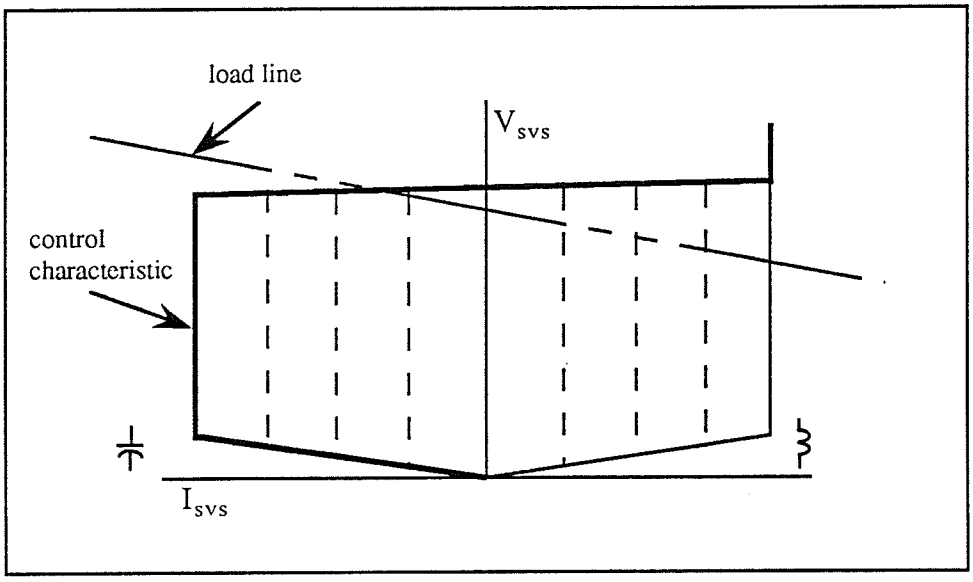


Figure 3.19: *VSI compensator characteristic*

The first component that needs to be designed is the dc capacitor. A method used to choose the proper value of capacitance is to find a value which will limit the peak ripple to 10% of the dc voltage at maximum leading output current [20]. Using Equations 3.14 and 3.15 (with the knowledge that I is 0.5 pu, V is equal to $0.1/\sqrt{2}$ and two pulses or steps of voltage occur per cycle), a 6513 μF capacitor will be required to limit the voltage ripple. Increasing the pulse number reduces the size of capacitor needed, however, special transformers are needed to take advantage of this fact in single phase applications. The cost of additional inverter bridges and special transformer outweigh the benefit of reduced filter requirements and smaller dc capacitor.

$$Z\ (pu) = V/I \tag{3.14}$$

$$C = 1\ /\ (w\ Z\ Z_{base}) \tag{3.15}$$

where $w = 120\pi$ x pulse number

The basic operating principle of a VSI, as descibed in the introduction of Section 3.4, is to keep the inverter output voltage in phase with the system voltage and to control the reactive power required by controlling the inverter output voltage. The inverter output voltage can be controlled by having a fixed dc supply and employing the technique of pulse width modulation (PWM) to control the amplitude of the fundamental component [37]. Harmonic content changes depending on the particular method of PWM chosen. The technique of voltage control used in this study is dc voltage control. By adjusting the phase angle between the system voltage and inverter voltage, a small component of real power will flow into or out of the capacitor, increasing or decreasing the energy stored, thus adjusting the voltage magnitude. A fixed amount of harmonics will be produced at all voltages using this technique of voltage control. PWM could be used to reduce the level of harmonics rather than to control the voltage. However, a large number of commutations per cycle are required which increase the losses and reduce the magnitude of the fundamental component. For these reasons, PWM will not be used on the single phase VSI.

Figure 3.20 shows the theoretical output voltage and gate pulses.

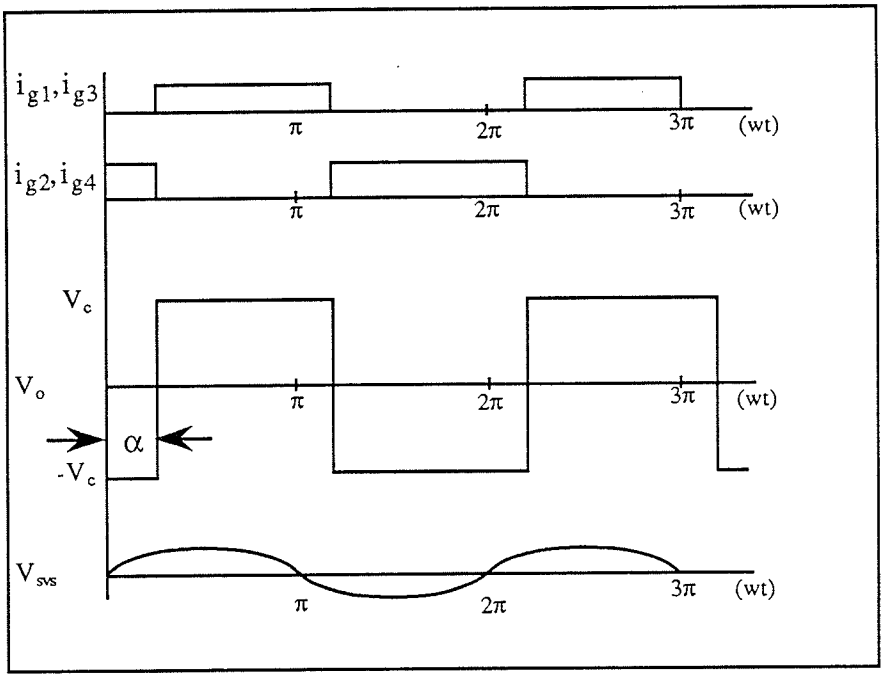


Figure 3.20: *VSI output voltage and gate pulses*

The output voltage harmonics can be calculated using Equation 3.16.

$$V_O = \sum_{n=1}^{\infty} ß_n \sin(n\,\omega_0\,t) \qquad (3.16)$$

where:

$$ß_n = \frac{2}{T/2}\int_0^{\frac{T}{2}} V_c \sin(n\,t)\,dt \qquad \omega_0 = \frac{2\pi}{T}$$

$$= \frac{4\,V_c}{n\,\pi} \qquad T = 2\pi$$

therefore:

$$V_O = \frac{4\,V_c}{\pi}\{\sin(t) + \frac{\sin(3t)}{3} + \frac{\sin(5t)}{5} + \ldots\}$$

The voltage is composed of all odd harmonics. Harmonics up to the eleventh should be eliminated by filters. A challenging problem is to design a filter which will eliminate the harmonics and also provide 125 kVAr of reactive power. Schemes that could be studied include:

1. A low pass filter on the secondary
2. Tuned filters on the secondary
3. Tuned filters on the primary

The third filtering scheme will be used in this thesis. Ideally, only an inductive reactance should be connected between the inverter output voltage and system voltage. An additional phase shift will be created by any filters connected to the secondary. The reactive power supplied to the system can be controlled more easily if the filters are connected directly to the bus which is being controlled.

The 125 kVAr of shunt capacitors can be divided into 5 banks by using a small series tuned inductor added to eliminate a particular harmonic. The filters can be designed using the same equations given for the TSC. Table 3.6 summarizes the component values of each filter.

Table 3.6:

Summary of Filter Component Values

n	Bc'	C (uF)	Blc	L (H)
3	0.08889	1.1360	-0.80	0.6879
5	0.09600	1.2270	-2.40	0.2293
7	0.09800	1.2530	-4.80	0.1146
9	0.09877	1.2630	-8.00	0.0688
11	0.09917	1.2680	-12.00	0.0459

Now that the filter requirements have been determined, the valve ratings can be found. Gate turn off (GTO) thyristors are being used, as opposed to conventional thyristors, in order to eliminate additional commutation circuitry. The GTO's must be capable of blocking a forward voltage equal to the dc voltage on the capacitor. The maximum RMS secondary voltage is 600 V plus 20% for overvoltages or 720 volts. Therefore, the maximum capacitor voltage required is 800 volts (from Eqn. 3.17)

$$4\ V_d/\pi = V_2\ \sqrt{2} \qquad (3.17)$$

The GTO's must be capable of blocking this amount (note: only unidirectional blocking ability is required). The current rating should be 0.5 pu plus 15% or 250 amps since the compensator is supplying only half the required VArs.

As mentioned briefly, the inverter output voltage is controlled by controlling the phase angle difference between the system voltage and inverter voltage. The dc voltage on the capacitor can then be modified by the small amount of real power which flows into or out of the inverter. Figure 3.21 serves to illustrate the idea. The initial system voltage is 1.0 pu and the capacitor is charged to its nominal value. No real power is required to flow into or out of the capacitor, therefore, the dc current is zero. At time t_1, a load is switched on causing the system voltage to dip. The dc voltage on the capacitor needs to be increased to the correct value within four cycles to compensate for the dip in system voltage. By creating a phase angle difference between the inverter and system voltages, an amount of power will flow for a length of time supplying the required change in energy on the capacitor. The

change in energy required can be found by using equation 3.19.

$$I = (V_o - V_s) / X \tag{3.18}$$

$$E = 1/2\ C\ (V_2^2 - V_1^2) \tag{3.19}$$

$$E \approx P\Delta t \tag{3.20}$$

$$P = [V_s\ V_o\ \sin(\alpha)] / X \tag{3.21}$$

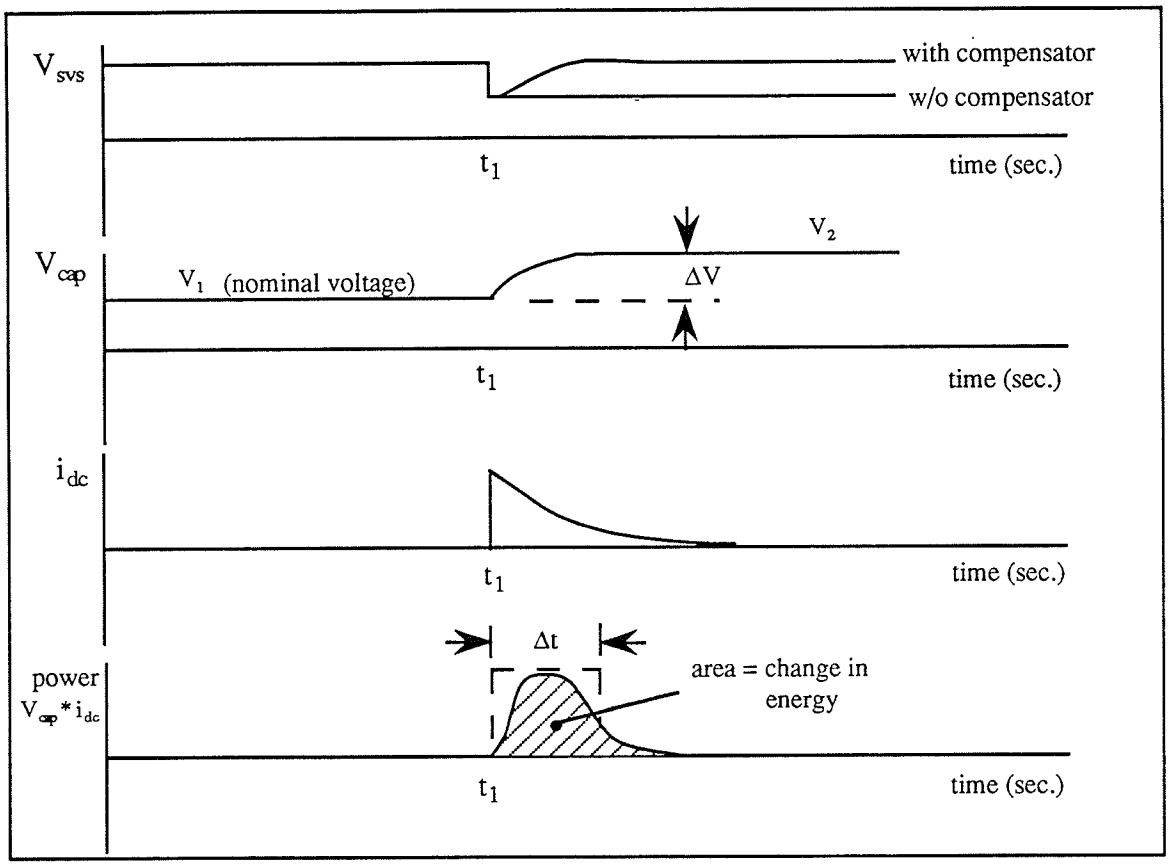


Figure 3.21: *VSI energy storage*

As a first order approximation to the required phase angle difference, Equations 3.18-3.21 can be used. The maximum capacitor voltage occurs when maximum leading current is required while the system voltage is controlled to 1.0 pu (neglecting overvoltage conditions). Using Eqn. 3.18 and a 10% leakage reactance, the required capacitor voltage is 1.05 pu or 700 volts (nominal capacitor voltage is 666 volts from Eqn. 3.17). The required energy needed to increase the capacitor voltage from 666 volts to 700 volts is 151.255 joules (Eqn. 3.19). A power flow of 2161 watts for 0.07 seconds (4 cycles) will provide the required

energy. Using the familiar power transfer equation for a transmission line (Eqn. 3.21) results in a required phase angle difference of 0.05°. A phase angle of this magnitude cannot be controlled realistically in a digital simulation program. A time step of 25 μs or 0.5° is normally used. It is possible to reduce the time step but this will result in longer simulation times and possible numerical problems. The solution adopted for this study was to increase the inductor and capacitor component values until a realistic phase difference of 5-10° was achieved.

The first step is to determine the maximum inductance which can be placed in the circuit. The GTO's must be capable of blocking a forward voltage equal to the capacitor voltage. If a practical limit of 1000 volts is placed on the blocking capability then the capacitor voltage must be limited to 1000 volts. The corresponding RMS value of the fundamental component of the inverter output voltage is 900 volts. The maximum leakage, assuming 1.0 pu system voltage and maximum leading current, is calculated to be 1.0 pu.

Let us assume the system voltage and inverter voltage are initially equal to 1.0 pu and are in phase. If a 4% drop in voltage now occurs, the capacitor voltage will have to be charged from nominal to maximum in 4 cycles.

A phase difference of 10° will cause 43400 watts of power to flow into the capacitor (Eqn. 3.21 and X=1.0 pu). The change in energy stored in the capacitor will be 3038 joules after 4 cycles. The corresponding capacitor will have to be 11000 μF to experience the required voltage change.

It will actually take longer than 4 cycles to charge the capacitor due to the control system. As the capacitor begins to charge, the system voltage increases due to the reactive power now flowing into the system. The error between V_{svs} and V_{ref} is decreasing, hence, the phase angle difference is decreasing and the capacitor is, therefore, charging more slowly. A solution is to decrease the capacitor size (by one half), thereby decreasing the charging time, while controlling the phase angle within the original limits of ±10°.

In summary, a minimum size capacitor of 6513 μF is required to keep the voltage ripple to a minimum, however, the size is reduced to 5500 μF in order to achieve realistic phase angle differences. In addition, 3.438 mH (0.9 pu) of inductance is added in series with the 10% transformer leakage, also for the purpose of achieving realistic phase angles.

3.4.2 Control Algorithm

Over the past ten years, a lot of interest has been shown in the applications of force-commutated reactive power compensators (VSI) [20,21,22,23]. Sumi and Yano et al [21] describe a 36 pulse, 20 MVAr compensator installed at Kitaosaka substation in Osaka, Japan. The feedback method of control is used in this installation to convert the error between VAr reference and actual VAr output to desired phase angle. VAr reference is changed according to the daily cyclic load demand. Walker [23] describes a 3 phase, 12 pulse current source inverter. The compensator is rated ±2.5 MVAr and is biased with 2.5 MVAr of capacitors. A feedforward control scheme is used to calculate the desired firing angle for a specific VAr demand. This method of control is suitable for compensating balanced cyclic loads such as motors. Cox and Mirbod [22] describe a voltage source inverter composed of 3 individual single phase bridges. Gate turn off (GTO) thyristors are used in this design to eliminate the commutation circuitry required with thyristors. Each bridge is controlled independently in order to supply the unbalanced reactive current requirements of an arc furnace. Edwards and Nannery [20] also use GTO technology in their 3 phase, ±1 MVAr voltage source inverter. Their compensator was installed at Orange and Rockland Utilities in Spring Valley, New York in 1986 and was manufactured with the help of Westinghouse Electric Corporation. Details on the control algorithm are not provided in this paper but it appears the compensator is being used as a voltage regulator.

With the exception of the last device, all of the compensators described above have been used for load compensation as opposed to voltage regulation. A suitable control algorithm will be developed in this section which will be able to control the voltage as well as or better than that designed for the thyristor switched capacitor.

A feedback control scheme was chosen for the VSI for the same reasons given in Section 3.3 for the TSC. PI control, however, will not be used. The required phase difference is only needed as long as a voltage error signal exists. If the phase difference is kept fixed, the capacitor will either continue to charge without limit or discharge to zero. Therefore, proportional control, with the ability to set the phase angle to zero once the capacitor voltage or compensator current criteria are exceeded, will be used.

A conceptual block diagram of the VSI's control system is shown in Figure 3.22.

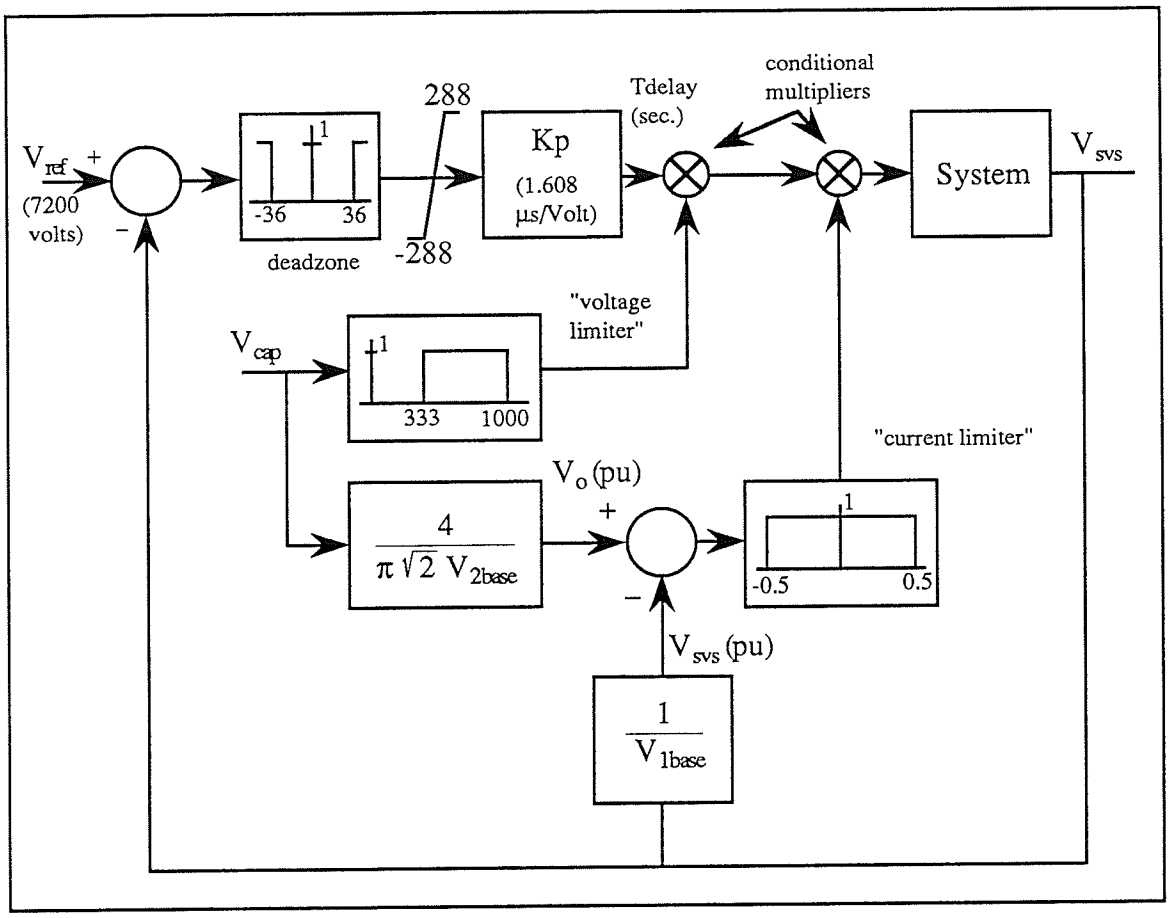


Figure 3.22: *VSI control block diagram*

A deadzone of ±36 volts (±0.5%) is included to prevent constant charging and discharging of the capacitor while the system voltage is near the reference setting. The voltage error signal is limited to ±288 volts (±4%) corresponding to the voltage change expected from ±125 kVAr compensation (as determined by load flow). Firing angle delay or phase angle difference is found by multiplying the voltage error by the factor Kp. Maximum voltage error corresponds to 10° or 0.000463 seconds, therefore Kp is set to 1.608×10^{-6}. Charging or discharging the capacitor is stopped as soon as either the limits of the capacitor voltage or the compensator current are exceeded.

An algorithm for prevention of overvoltages after fault clearing will not be studied in this thesis.

3.5 Chapter Summary

In this chapter, after the reactive power requirements of the St. Agathe feeder were determined, the appropriate component values and control algorithms for a TSC and VSI were designed. From this chapter, a number of conclusions can be made:

1. 250 kVAr of capacitive shunt compensation is required to regulate the voltage on the St. Agathe feeder.

2. A TSC employing binary switching has advantages over fixed size capacitor bank switching in terms of size and cost.

3. Voltage regulation can be accomplished by means of feedback control.

4. PI control will be used to determine desired shunt susceptance in a TSC, however, the new "direct calculation" method may be quicker and, therefore, better able to correct for flicker.

5. Out of range compensation can be achieved by voltage reference modification instead of reactive power co-ordination.

6. Proportional control, with appropriate delay angle modification once limits of capacitor voltage and compensator current are reached, will be used on the VSI.

7. Due to the amount of harmonics produced in a single phase VSI, filters are required. Therefore, little advantage is realized in terms of component sizes, when comparing a VSI with a TSC.

The next chapter will test the designs digitally using EMTDC with the most technically suitable choice being further tested on an analog simulator.

Chapter 4
Design Testing

4.1 DIGITAL SIMULATION

The compensators are simulated digitally using an electromagnetic transient program, EMTDC [41], developed at Manitoba Hydro by D. Woodford. EMTDC has many advantages over other transient programs. The ability to subdivide a system into smaller subsystems decreases the computational time due to the fact that smaller matrices are inverted. Also, there are many models of systems in the form of subroutines which may be interfaced together to simulate a more complex system.

As part of the chapter on design testing, this section will test the operation of each compensator digitally. Digital modelling of the St. Agathe feeder is presented. Several methods of single phase RMS voltage measurement techniques are evaluated next, followed by the development of detailed compensator models. Finally, simulation results are presented including startup, transient reaction to load variations and fault recovery.

4.1.1 Description of Test System

The St. Agathe feeder was chosen to be modelled. Extensive load flow tests were done in Section 3.2 and it was found that a simplified model of the feeder could be used to model the voltage variation on the compensator bus. Since it is computationally more efficient to use a system with fewer nodes and our objective is to verify compensator operation, the simplified feeder model will be used in EMTDC simulations. The transformer at the substation will be modelled by its leakage reactance. Added to the model will be two small resistances to represent a normally closed switch and a large resistance to ground at node 9 to be used in simulating line to ground faults. The complete model, which is referred

to as subsystem 1 when placed in EMTDC's Data file, is shown in Figure 4.1.

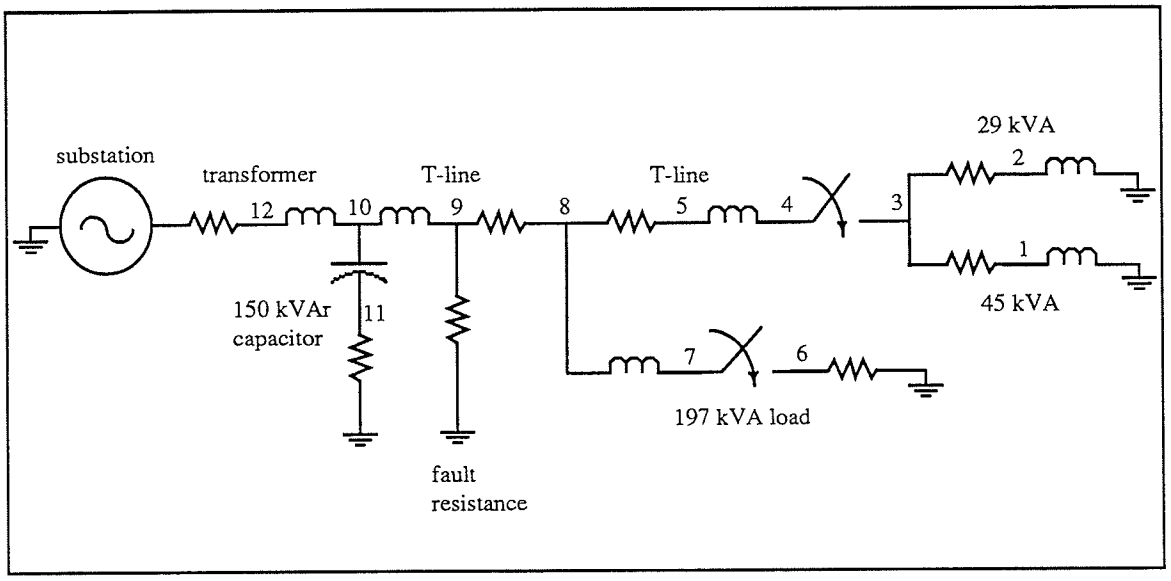


Figure 4.1: *EMTDC model of St. Agathe feeder*

Component values are given in the program listing of Appendix B. All values are in per unit. Inductances are entered in per unit henries and capacitance in per unit microfarads.

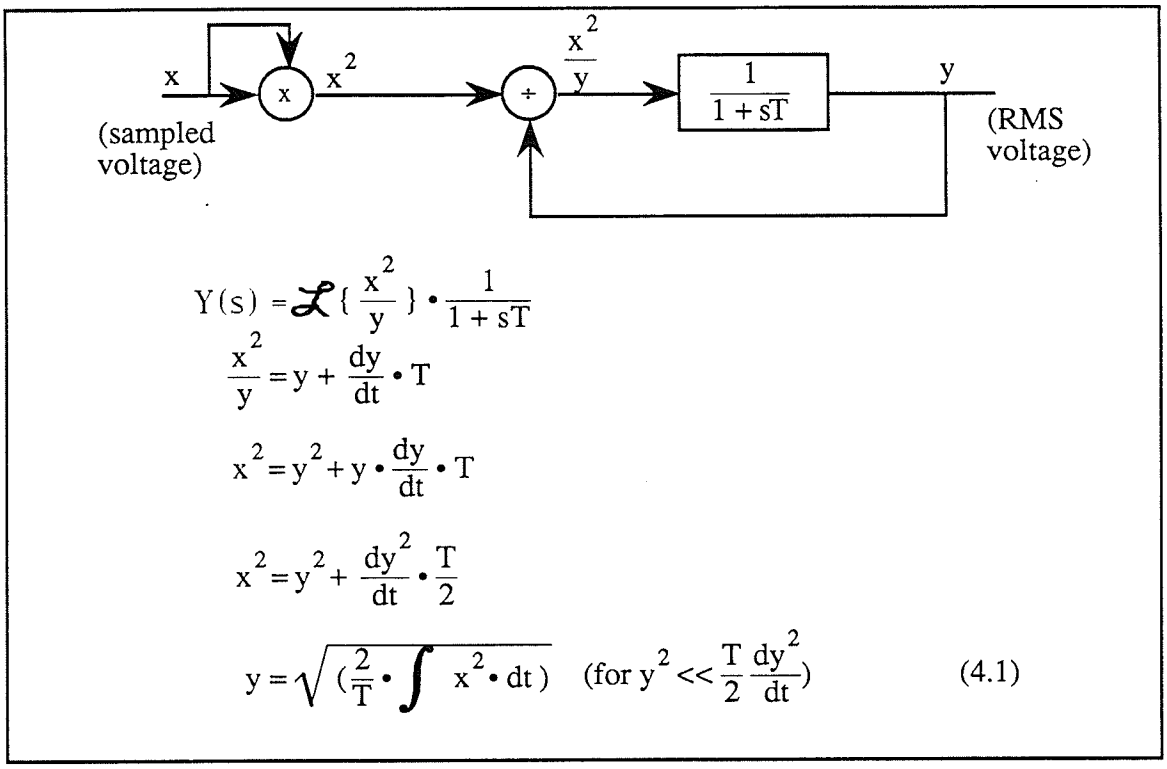
4.1.2 Single Phase Voltage Measurement

In order to control bus voltage quickly, a fast and accurate RMS voltage measurement technique must be used. Four measurement techniques were evaluated:

1. EMTDC subroutine RMS3
2. Peak Detection
3. Half cycle integration (V2RMS)
4. EMTDC subroutine VRMS10

Each technique will be described in turn followed by simulations. The best method will then be selected.

The method used in subroutine RMS3 is outlined below.



$$Y(s) = \mathcal{L}\{\frac{x^2}{y}\} \cdot \frac{1}{1+sT}$$

$$\frac{x^2}{y} = y + \frac{dy}{dt} \cdot T$$

$$x^2 = y^2 + y \cdot \frac{dy}{dt} \cdot T$$

$$x^2 = y^2 + \frac{dy^2}{dt} \cdot \frac{T}{2}$$

$$y = \sqrt{(\frac{2}{T} \cdot \int x^2 \cdot dt)} \quad (\text{for } y^2 << \frac{T}{2}\frac{dy^2}{dt}) \qquad (4.1)$$

Figure 4.2: *RMS3 algorithm*

If the time constant T is very large, the output will be the RMS voltage but will approach the true value very slowly. As T decreases in size response time increases but a large 2nd harmonic component is superposed on the RMS voltage. Filters, which further decrease the response time, are required to remove the 2nd harmonic.

Peak detection is used to find the RMS voltage in the second method. During the positive half of the voltage waveform, the voltage is sampled to find the absolute peak. The RMS voltage is calculated by dividing the absolute peak voltage by $\sqrt{2}$. This value is held constant for one cycle until the next positive peak voltage is found. Detection only takes place during the positive half of the waveform since the thyristors are gated during the negative half in our TSC compensator. A transient overvoltage might occur which would cause an error in peak detection and a corresponding error in RMS voltage. Errors could also arise due to noise, harmonics or voltage spikes due to breaker switching and faults. Due to

the large number of error sources, the method of peak detection will be eliminated from further evaluation.

The next method is entitled half cycle integration. The positive half voltage is sampled, squared and numerically integrated using the rectangular method of integation. More sophisticated methods such as trapazoidal integration or Simpson's rule could be substituted for rectangular integration. However, a small sampling period (25 μs) is being used in the simulations, therefore, very little error is introduced by a simpler method of integration. RMS voltage is calculated by dividing by the period and taking the square root. As with peak detection, the RMS voltage is held constant for one cycle until the positive half voltage can be integrated again.

Finally, EMTDC's subroutine VRMS10 can be described. The basic idea behind this method lies in the following picture and equation.

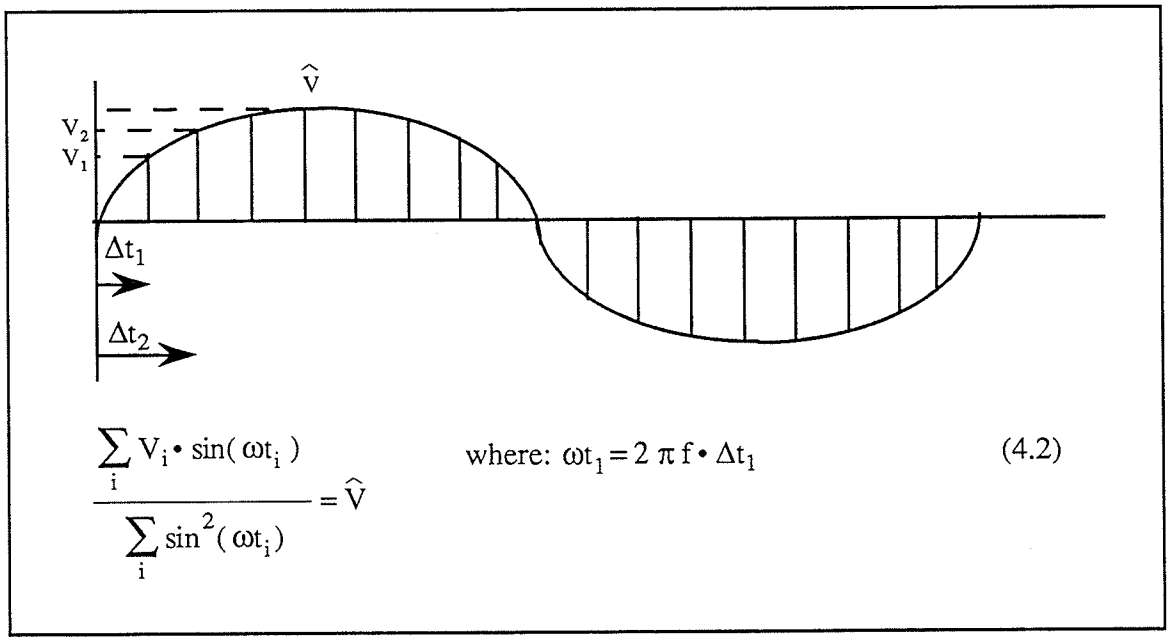


Figure 4.3: *VRMS10 description*

The peak voltage can be estimated by the first term in Equation 4.2. The sampled voltage (V_i) is multiplied by the sine of the angle from the zero crossing and divided by sine squared. As more and more terms get added, the estimate of peak voltage becomes

more accurate. RMS voltage is updated every sample instant by dividing the most recent peak voltage estimate by $\sqrt{2}$. After each zero crossing, the sum in the numerator and denominator are cleared to prevent the numbers from becoming too large. Some smoothing of the voltage is required around the zero crossings to prevent inaccurate zero crossing detection.

Each method, other than peak detection, was tested by simulating a ramping load and measuring the resulting compensator current. The results are shown in Figure 4.4. Subroutine RMS3 has a very poor response. The settling time is very long (0.1 seconds). The other two methods have similiar responses. Subroutine VRMS10 has the disadvantage of having a large 120 Hz ripple superposed on the RMS value. Since the method of integration has the best response, it will be used exclusively in the digital model.

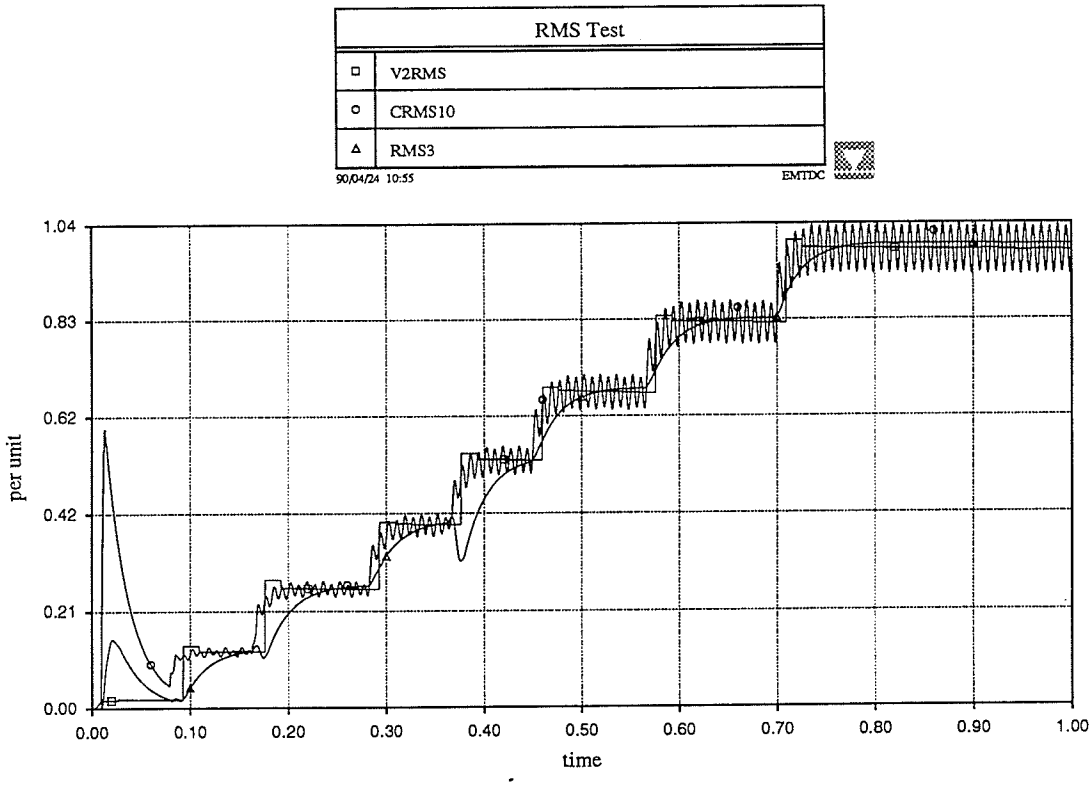


Figure 4.4: *Single phase RMS evaluation*

4.1.3 Compensator Modelling

There are no subroutines available in EMTDC which model a single phase TSC or

VSI. Subroutines are developed in this section by making use of the components designed in Chapter 3 as well as the control algorithm.

4.1.3.1 TSC Modelling

A model of a back-to-back thyristor-diode switch is required before the complete TSC is simulated. A simple circuit was used to develop the model. Figure 4.5 is a representation of the components of this simple circuit.

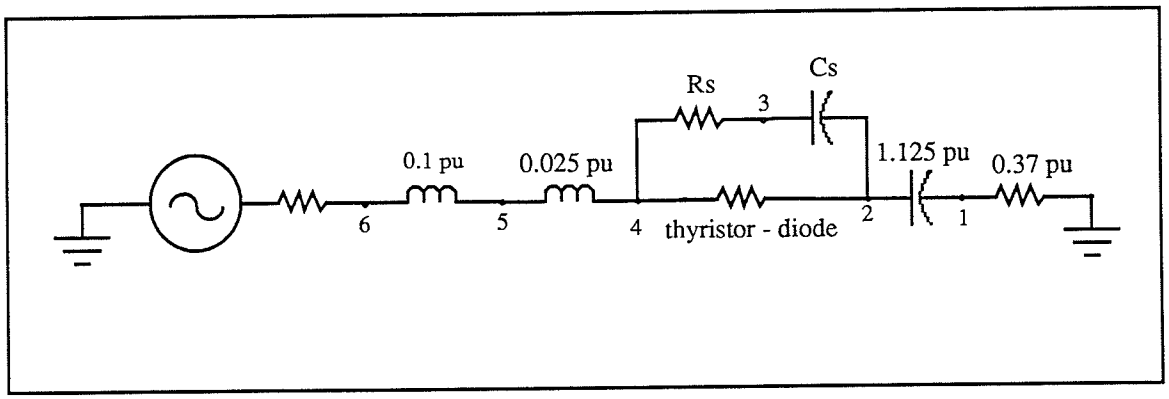


Figure 4.5: *Simple model*

The transformer leakage, inductance and capacitance developed in Chapter 3 are used in the model. The thyristor-diode is represented by a resistance. A large resistance indicates the thyristor is blocking while a small resistance indicates conduction. The resistance can be changed dynamically in a user written subroutine according to system conditions. The algorithm for changing the resistance value will be developed later in this section.

A large resistance (0.37 pu) is added to damp current transients and also to model resistance that would occur in the real system. The time constant of a current transient is given by:

$$T = \frac{L}{R} = \frac{0.0002653 + 0.0000663}{0.37} = 0.000896 \text{ sec.} \qquad (4.2)$$

Transients will die out in approximately 10*T seconds or 1/2 a cycle. A realistic amount of

resistance corresponds to the amount contained in the inductors. A Q-factor or X/R ratio of at least 40 is specified for most inductors. The inrush current decay time constant is another indicator of proper resistance values. Typical current decay time constants vary from 0.5 - 2.0 seconds. A more realistic value of resistance is therefore 0.003125 pu. Current transients will die out in 0.5 seconds. The larger resistance value will be used in the simulations in order to reduce the simulation time required to reach steady state conditions.

Proper values of snubber resistance and capacitance need to be calculated next. With the thyristor blocking, dv/dt should be limited to less than 250 V/μs. The upper limit of snubber resistance is found using Equation 4.3.

$$R_s/L \leq 250 \text{ V}/\mu\text{s} \qquad (4.3)$$
$$R_s \leq (0.41667 \text{ pu}/\mu\text{s} * 596.6 \ \mu\text{H})$$
$$R_s \leq 248.71 \text{ pu}$$

The voltage across the capacitor (1.125 pu) should remain constant for 1 second in order to minimize the number of times the diode must conduct to keep the capacitor charged. The lower limit of thyristor resistance is therefore:

$$5T = 5 \ R_s \ C \geq 1.0 \qquad (4.4)$$
$$R_s \geq 1.0 / (5 * 2357.79 \ \mu\text{F})$$
$$R_s \geq 84.825 \text{ pu}$$

A snubber resistance of 150 is chosen which satisfies both conditions.

The impedance of the snubber capacitor should be greater than 1000 pu in order to limit the current flowing through the snubber while the thyristor and diode are blocking. Acceptable values of capacitance are:

$$1.0 / (w \ C_s) \geq 1000.0 \qquad (4.5)$$
$$C_s \leq 1.0 / (1000.0 * 377.0)$$
$$C_s \leq 2.7 \ \mu\text{F}$$

A 1 μF snubber capacitor was chosen.

An additional constraint placed by EMTDC is that the RC time constant should not be less than the calculation step to prevent numerical instability. A calculation step of 25 μs will be used in the simulations. The RC time constant of the snubber is 150 μs and therefore will not cause an instability problem.

The algorithm used to model a thyristor-diode switch is outlined in the flowchart of Figure 4.7. The previous state of the thyristor is determined first. If the thyristor was off, it

may only be turned on if the voltage is at its negative peak and a firing pulse is detected. The thyristor may be turned off as soon as the current is negative. However, the diode allows conduction in the negative direction. The branch resistance will not be made large, therefore, until the diode is reverse biased. The branch resistance is held constant for 3 to 5 calculation steps to prevent numerical instability due to frequent switching. Numerical instability can occur for a number of reasons in electromagnetic transient programs. For instance, voltage chatter can develop at a node which has only large resistors or inductors connected to it. The chatter can be made worse by having diodes turned off and on at every calculation step. The number of calculation steps can also be related to the turn off time of a thyristor which is approximately 40 μs. Therefore, the branch conductance should remain constant for at least 2 calculation steps (each is 25 μs) to realistically model the turn off time with an additional 1 to 3 steps being added if numerical problems result.

Figure 4.6 shows the voltage and current waveforms with the thyristor blocking and conducting. The waveforms agree with what was theoretically predicted in Section 3.3.

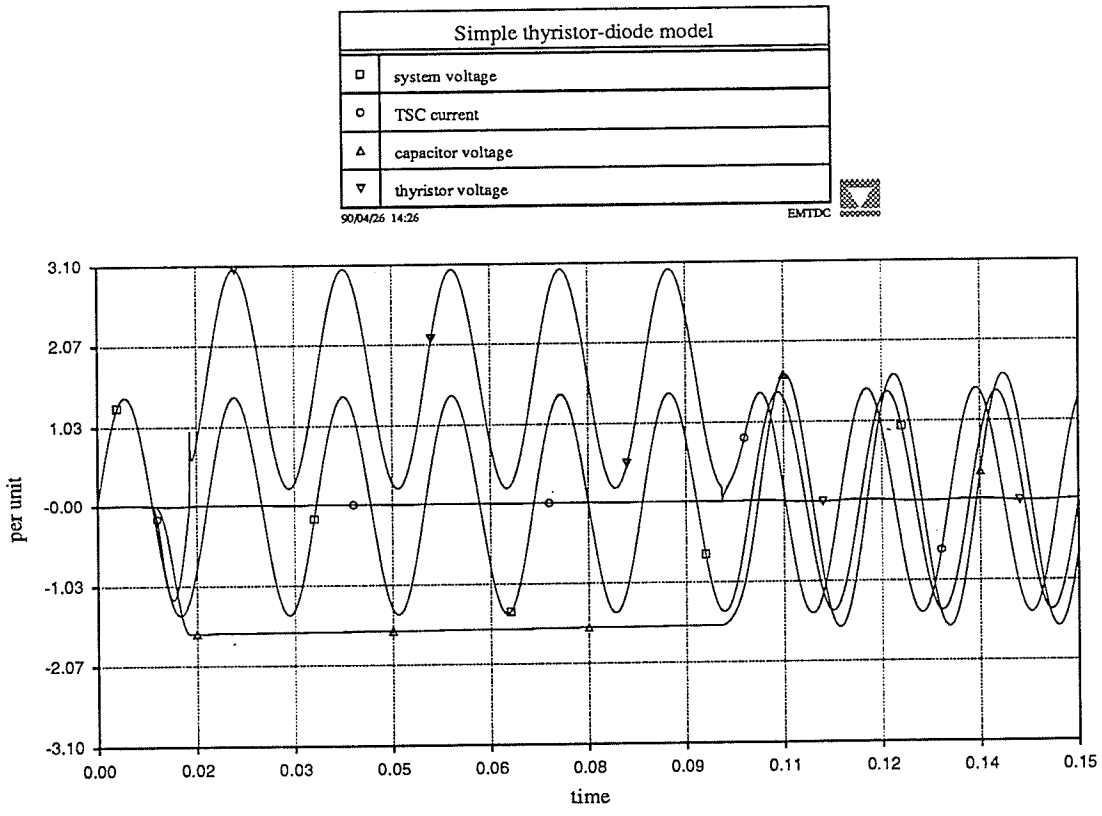


Figure 4.6: *Thyristor-diode model results*

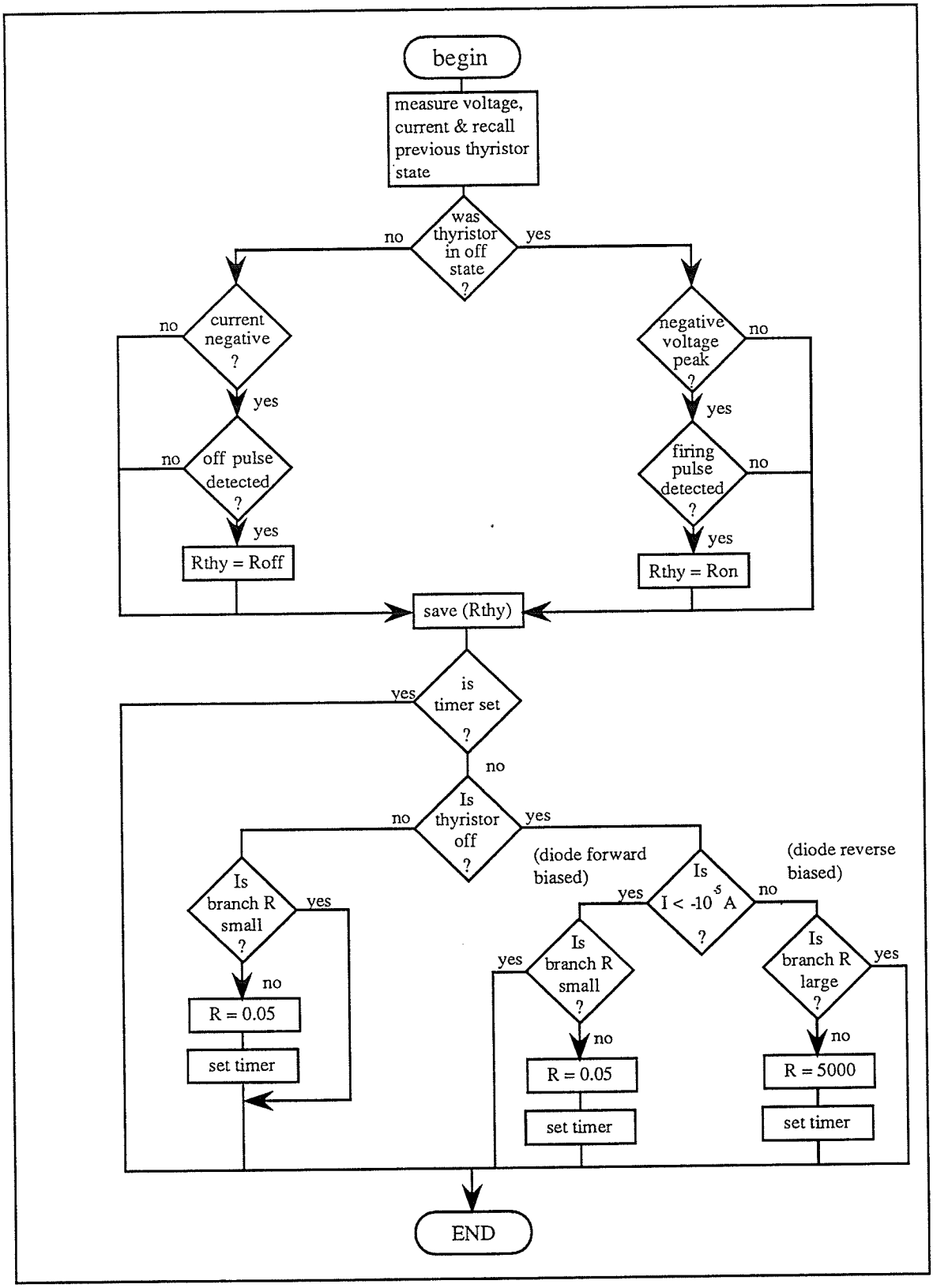


Figure 4.7: *Flowchart of thyristor-diode algorithm*

Since the thyristor-diode model is working, the next step will be to simulate all three capacitor banks, single phase transformer and appropriate controls. The thyristor switched capacitor compensator is also to be interfaced to the St. Agathe feeder model. The circuit diagram of the compensator is shown in Figure 4.8.

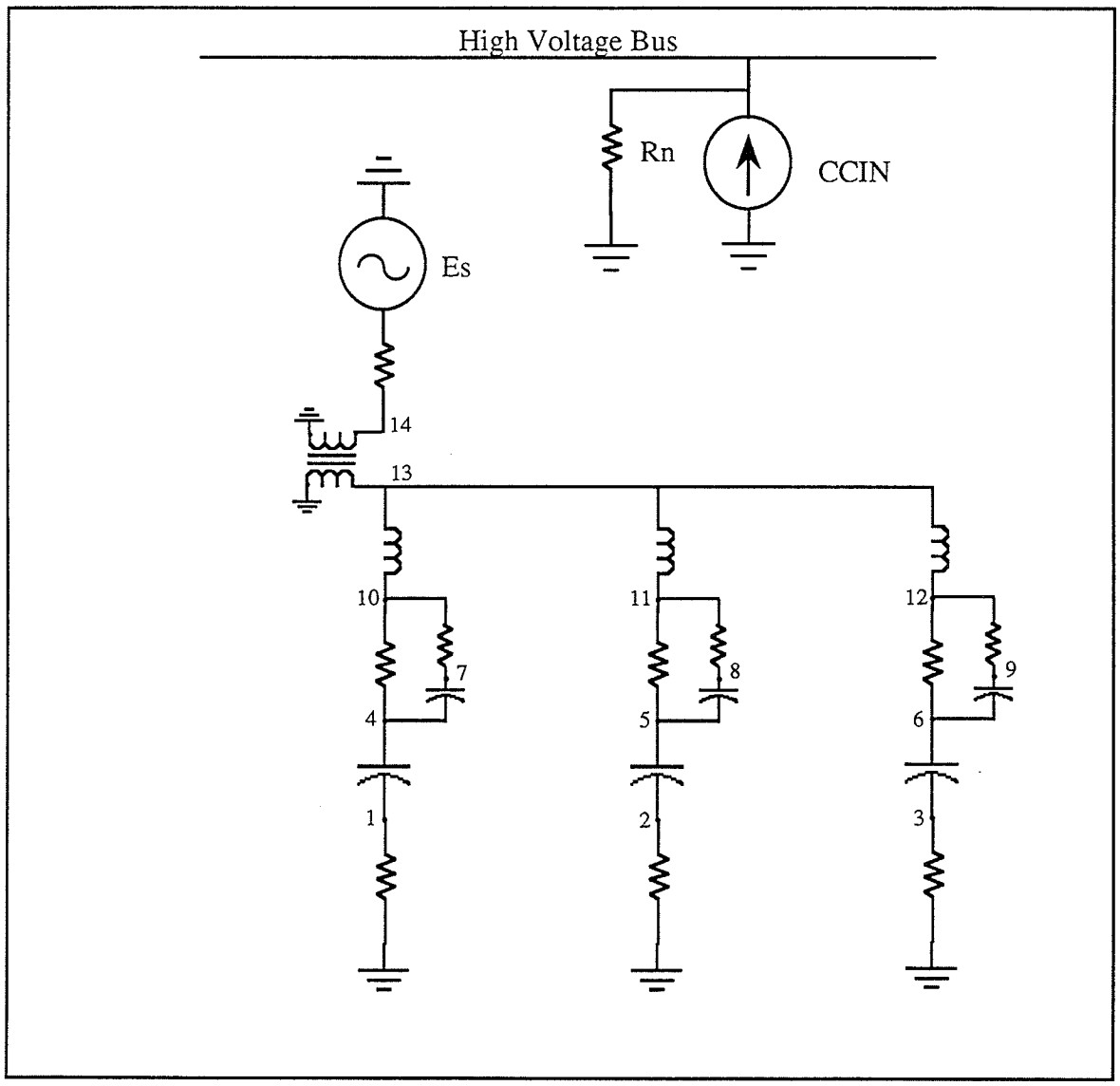


Figure 4.8: *Complete TSC model*

The algorithm of the complete thyristor switched capacitor is shown in block diagram form in Figure 4.9. The primary voltage is converted to a square wave for timing purposes. Counters are used to prevent inaccurate zero crossings. For example, during a fault the concept of a zero crossing does not exist, however, by employing counters, the positive and negative voltage half routines will still be executed. Digital simulations require proper timing during faults to get an accurate representation of RMS voltages.

During the positive half of the system voltage, the voltage is sampled at every time step, squared and added to itself. Several calculations are performed once during the negative half. First, the secondary RMS voltage is calculated by dividing by the number of samples and taking the square root. Secondly, the system voltage is then calculated by making use

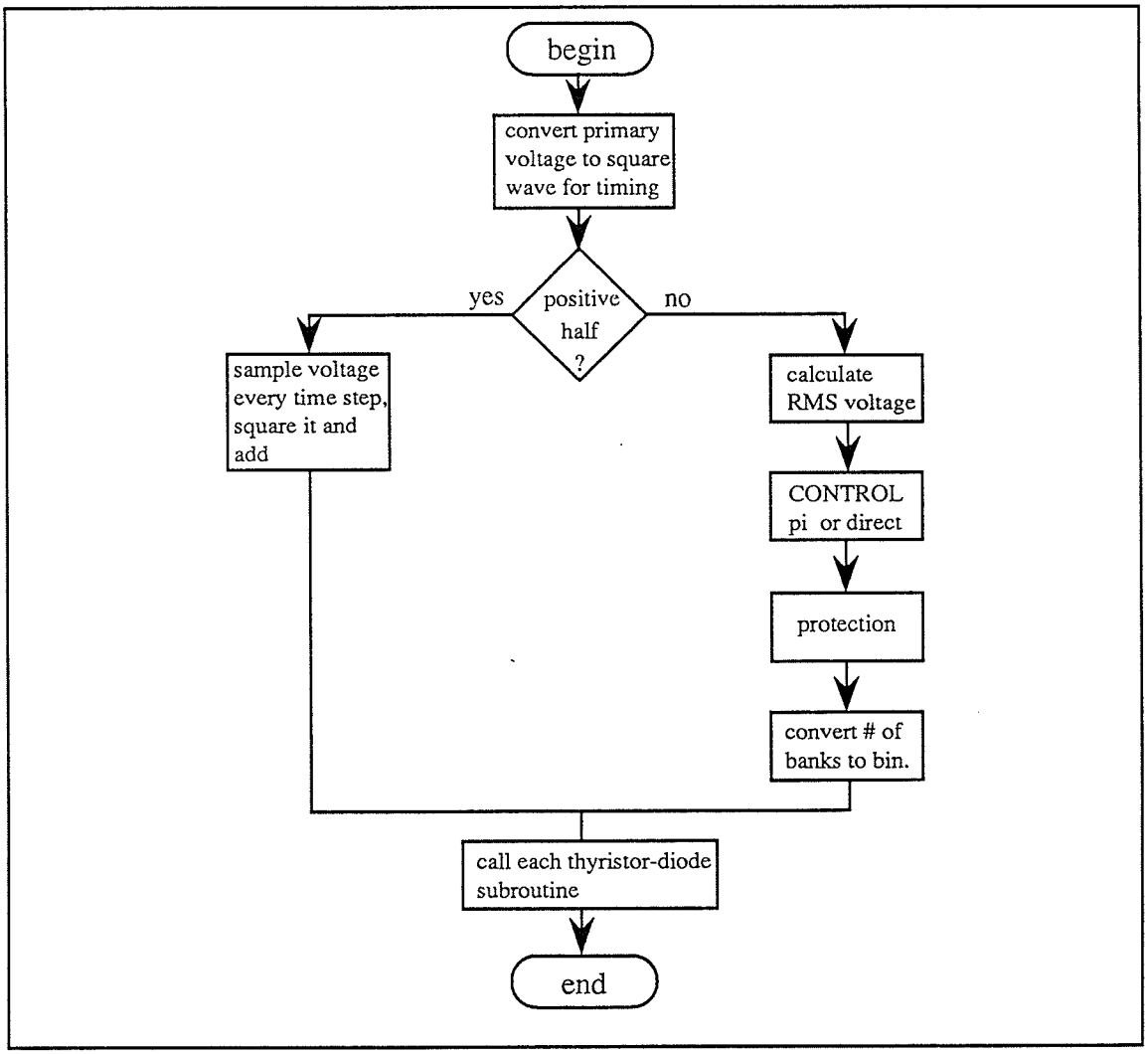


Figure 4.9: *TSC subroutine algorithm*

of Equation 3.13. The control systems described in Section 3.3.2 are implemented digitally. Conversion of the desired number of capacitor banks to a binary signal takes place next followed by a check of the measured voltage for protection purposes. If the voltage is below 0.7 pu, the binary signal is changed to 0 (no banks on) and a 2 cycle timer is initiated once the fault has cleared. Finally, a call is made during each time step to the thyristor-diode subroutine. The thyristor-diode subroutine described earlier models one branch, therefore, three subroutine calls are made in order to control the three thyristor-diode switches. Only one call statement needs to be added and a slight modification to the data file needs to be made for each additional capacitor bank. Section 4.1.4 contains results from digital simulations of the TSC model.

4.1.3.2 VSI Modelling

A prototype power system simulator developed by Mr. T.L. Maguire, of the Department of Electrical and Computer Engineering, University of Manitoba, has been used to model a single phase voltage source inverter. Switching devices such as diodes, thyristors and GTO's are represented in a novel manner that allows the user to simply connect the devices where required without having to worry about circuit level logic. An example of circuit level logic that had to be written for EMTDC is the thyristor-diode switching algorithm for a TSC which is shown in the flowchart of Figure 4.7. The prototype simulator has the advantage over EMTDC in this case, since the user only has to supply the desired turn on times rather than provide the complete switching logic. Another advantage the prototype simulator has is that numerical oscillations resulting from capacitive loops and inductive nodes are eliminated. Information on the program, as well as simulation results from a low-power dc-transmission link example can be found in reference [40] (note: the publishing of this paper is forthcoming).

The prototype simulator is still in the developmental stages and has yet to include the features of snapshots and subsystems. Therefore, the entire compensator and load network are modelled as a complete system. (In addition, simulation results will show the initial startup transients due to the absence of a snapshot feature). Figure 4.10 contains the complete simulation model including the node numbers used in the program. Component values are listed in the data file included in Appendix B.

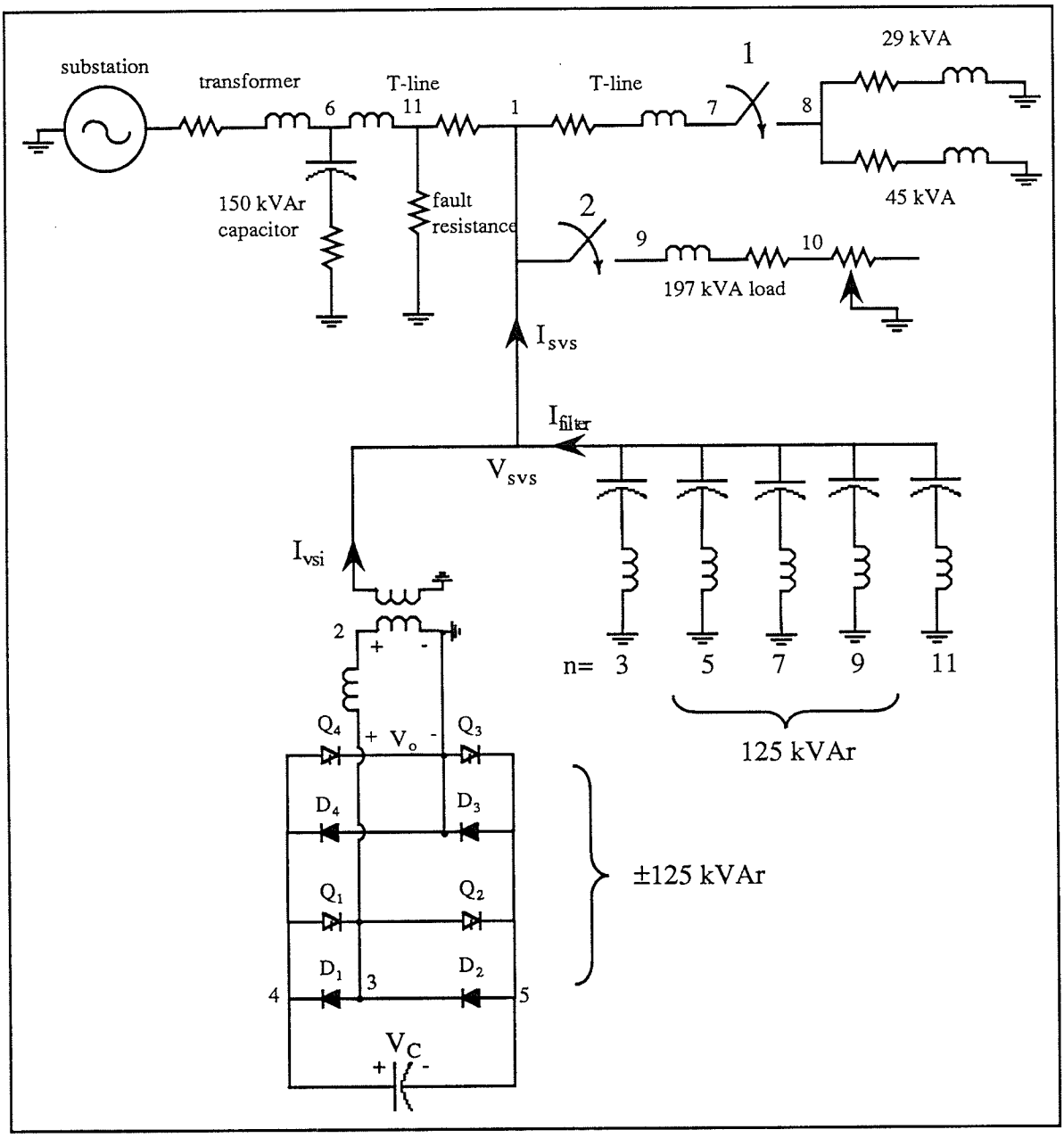


Figure 4.10: *VSI simulation model*

The algorithm used to control the voltage source inverter is similiar to that of the TSC (see Fig. 4.9). The primary voltage is converted to a square wave for timing purposes. During the positive half, the voltage is squared and integrated. The true RMS value of the system voltage is calculated during the negative half (at time Tset, see Fig. 4.11). From the error between the RMS voltage and reference voltage, an estimate of the required time delay is calculated.

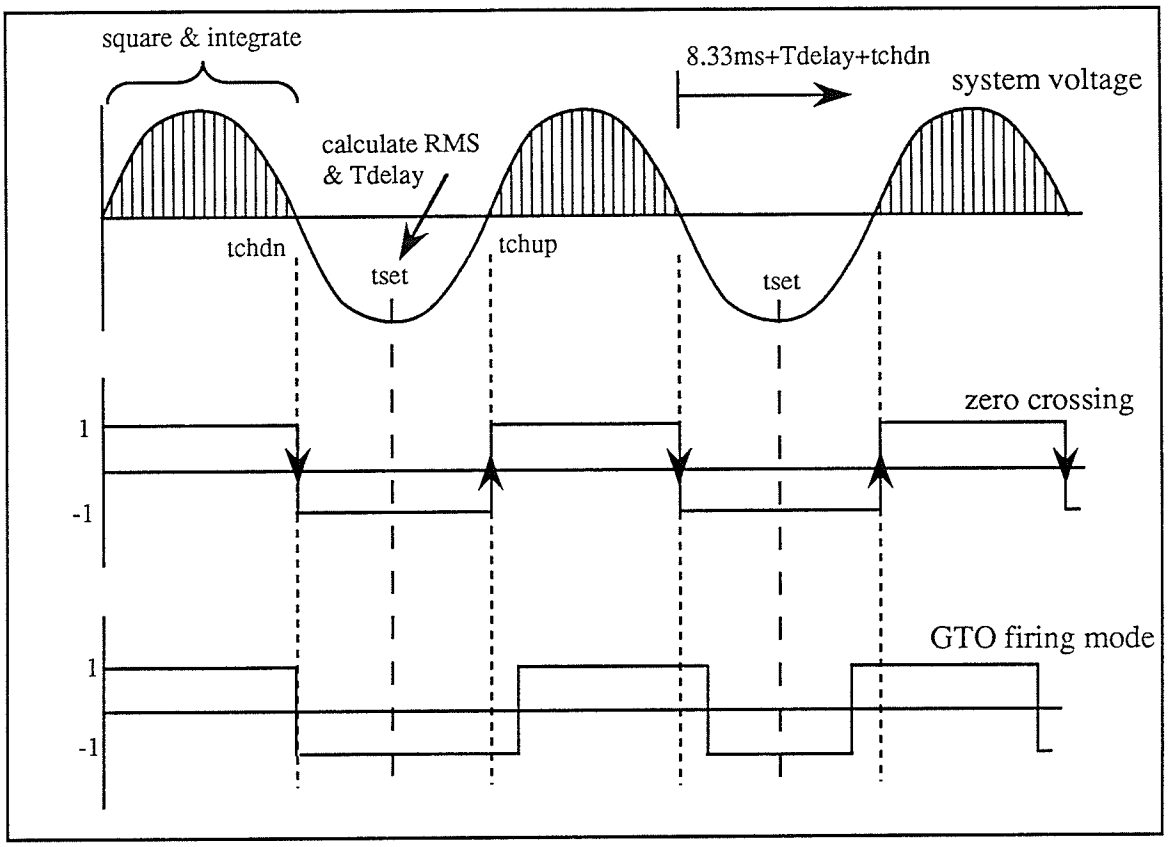


Figure 4.11: *GTO firing mode timing*

Symmetrical firing of the GTO's is required in order to eliminate noncharacteristic even harmonics from appearing in the voltage. Figure 4.11 shows the timing involved in controlling GTO firing. At the first Tset in Figure 4.11, a positive Tdelay is calculated, whereas at the second Tset a negative Tdelay is calculated. The GTO firing resulting from these Tdelays is shown in the third curve of Figure 4.11.

The actual times (tchdn and tchup) of the two most recent transitions in the zero crossing signal are stored in memory. GTO firing is synchronized with the negative transition. The time delay, calculated at time Tset, is added to the time of the negative transition (tchdn) plus 0.083 milliseconds (0.5 cycle). At this new time, the firing mode is changed to one. A firing mode of one corresponds to GTO 1 and 3 being turned on and GTO 2 and 4 being turned off. Similarily, the time delay is added to the time of the positive transition

(tchup) plus 0.0833 ms, at which time the firing mode is changed to minus one. Corresponding to this new firing mode, GTO 1 and 3 will be turned off and GTO 2 and 4 will be turned on.

Results from digital simulations of the VSI model are presented in Section 4.1.4.2.

4.1.4 Simulation Results

4.1.4.1 TSC Results

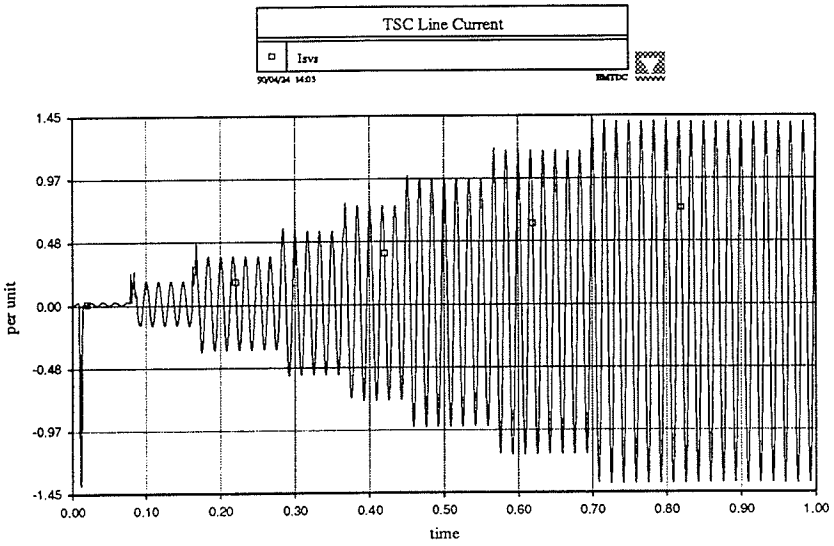
The thyristor switched capacitor model was tested by subjecting it to various load conditions. The conditions that were tested include:

1. Startup with increasing (ramping) load
2. Machine start
3. Flicker
4. Fault

When applicable, comparisons will be made between PI control and the direct calculation method.

The first test performed on the model was startup on light load with the load increasing by 7% continuously in one second. The load is ramped by having the resistance between nodes 6 and 7 (see Figure 4.1) vary exponentially from four per unit to zero. Figure 4.12 shows the resulting current supplied by the compensator and the RMS line voltage. An initial negative current spike is required to charge the capacitors. Depending on the value of leakage reactance, the capacitors overcharge on startup between 12.5% and 32%. Figure 4.13 contains a graph of capacitor voltages for different leakage reactances when the compensator is designed for 10% leakage. The overcharging causes a slight current transient to occur when bank1 (at 0.09 sec.), bank2 (at 0.18 sec.) and bank3 (at 0.38 sec.) are initially switched in. The switchings are transient free thereafter.

a)



b)

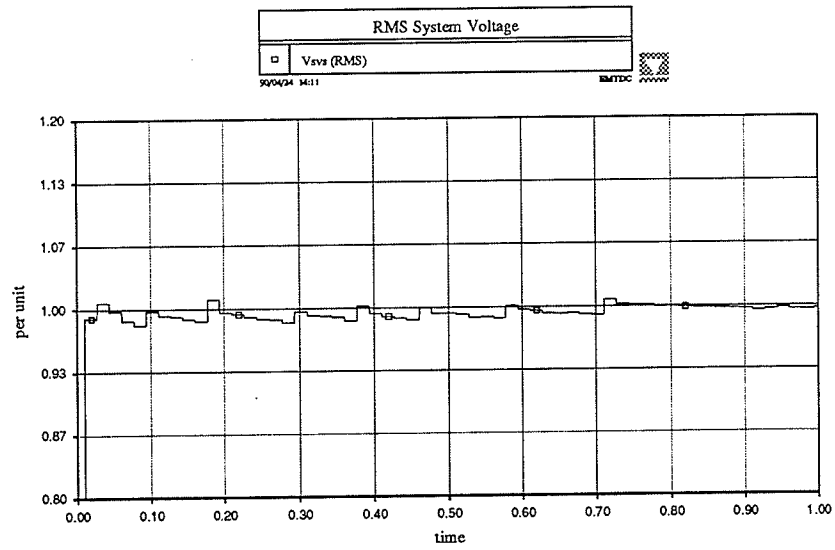


Figure 4.12: *Startup with ramping load, a) TSC current, b) RMS primary voltage*

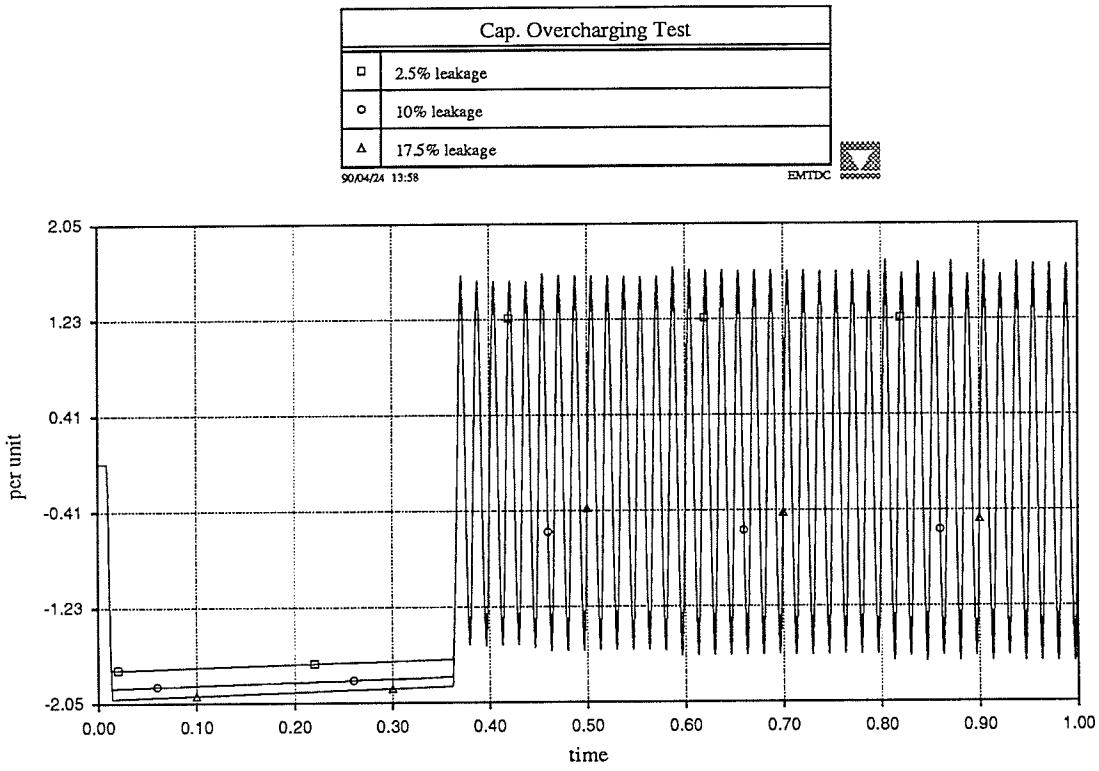
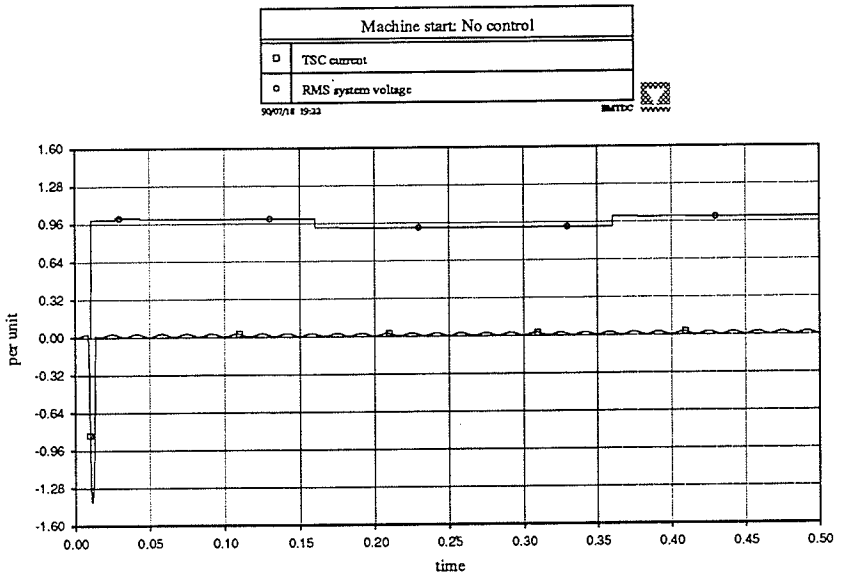


Figure 4.13: *Capacitor overcharging test*

The next test subjected the compensator to a load which caused the voltage to dip by 8% for 0.2 seconds. Machine starting or arc welding could be the cause of this type of voltage depression. A comparison of the compensator current resulting from PI control and the direct calculation method is shown in Figure 4.14. The compensator current is slowly ramped in and out with PI control, whereas the correct amount of compensation is immediately switched in or out using direct calculation. The effect is further dramatized by comparing RMS voltages (included in each graph).

a)



b)

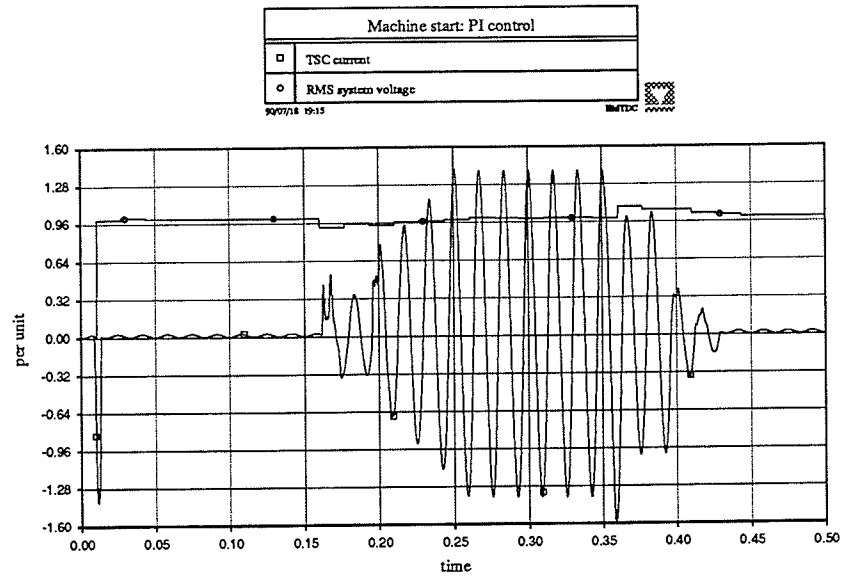


Figure 4.14: *Machine start results, (a) No control, (b) PI control, (c) direct*

c)

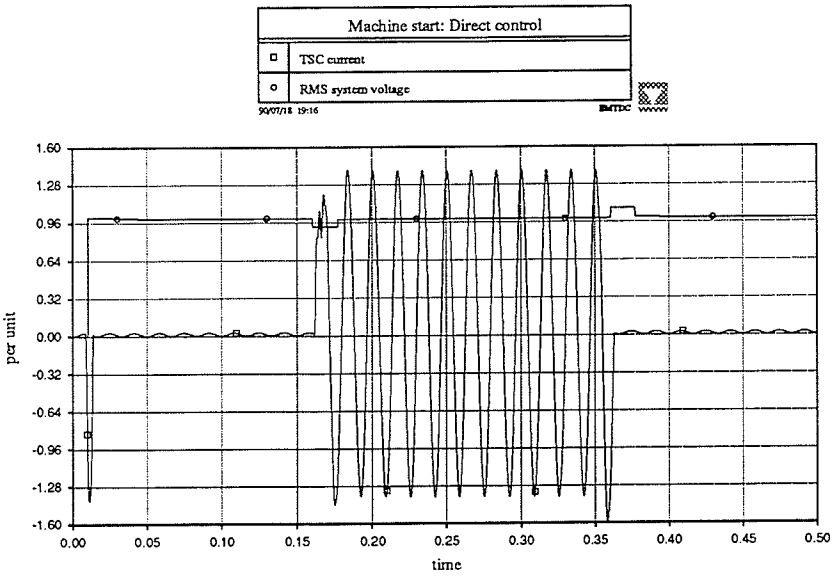
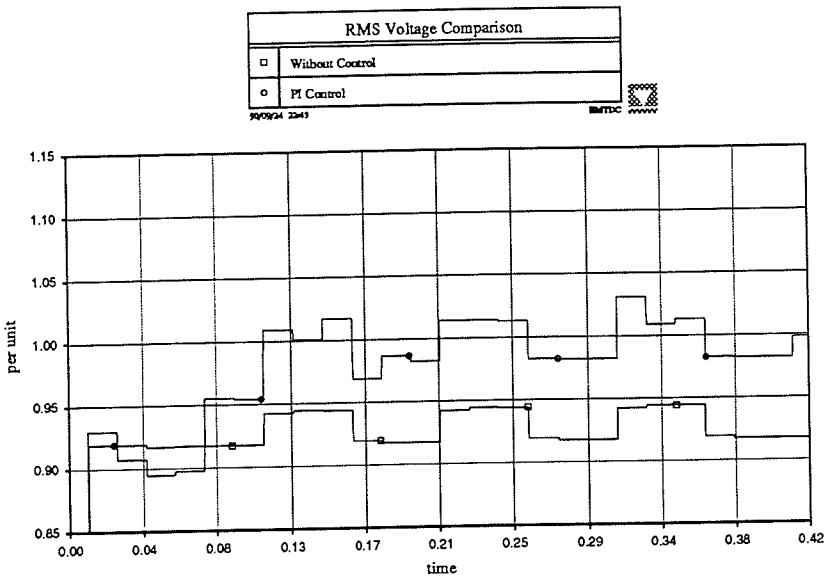


Figure 4.14 cont.: *Machine start results, (a) No control, (b) PI control, (c) direct*

Arc furnaces or spot welding could cause the fast voltage fluctuations (flicker) being modelled next. A 3% change in voltage at a flicker frequency of 0.1 seconds is being caused by switching switch #3 (see Fig. 3.12). The results are shown in Figure 4.15. Again, the direct calculation method is found to outperform the PI control method in terms of voltage regulation. In fact, at this frequency the PI control is too slow to react. The flicker has essentially become biased around 1.0 per unit. If the frequency is increased to 0.2 seconds, the PI control is able to respond but the voltage variation has doubled making the flicker problem worse (see Fig. 4.16).

a)



b)

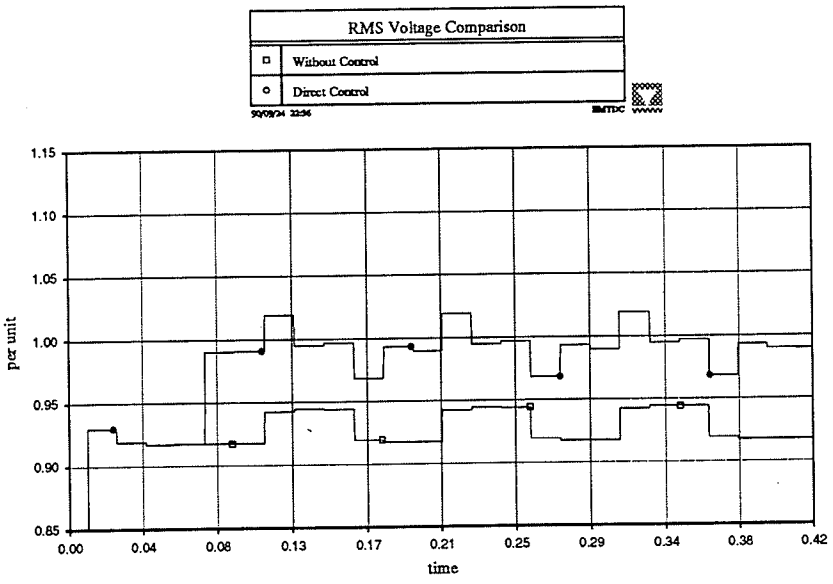
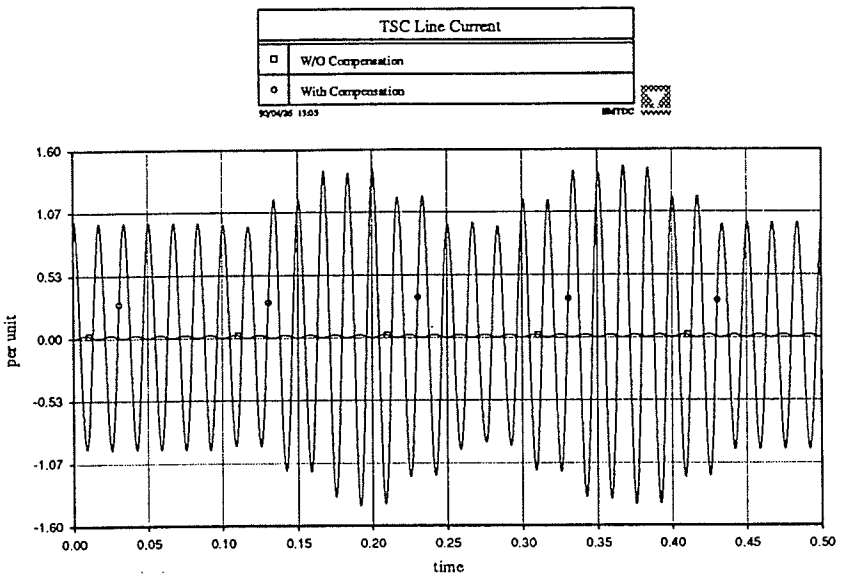


Figure 4.15: *Flicker simulation results, a) RMS voltage (PI control), b) RMS voltage (Direct control)*

a)



b)

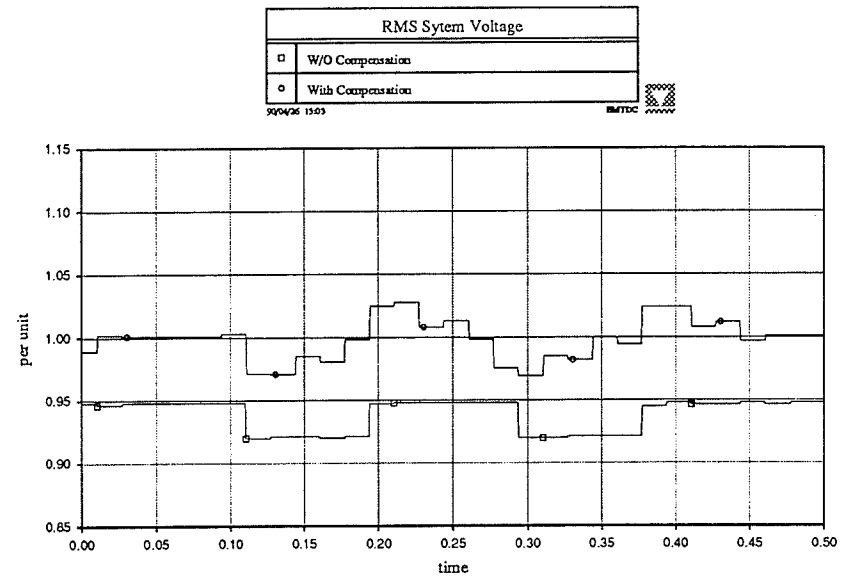
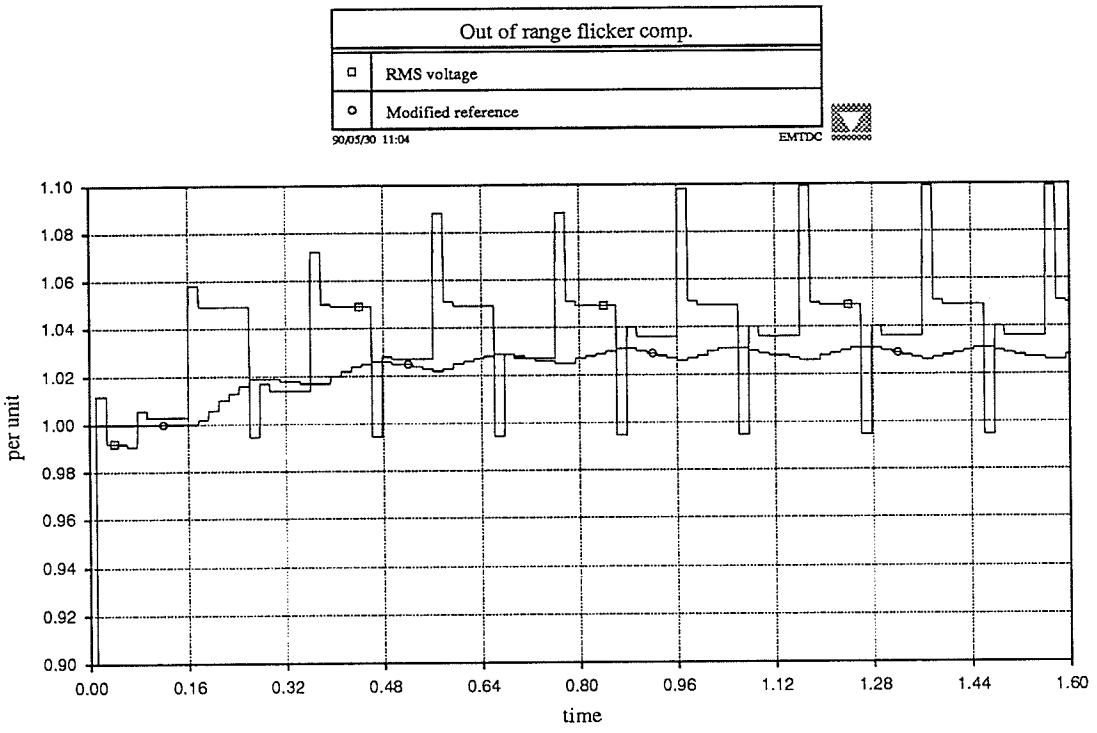


Figure 4.16: *PI control at 0.2 frequency, a) TSC current, b) RMS voltage*

During conditions of light or heavy loading, the compensator may not be able to correct for flicker because it is happening outside of the compensation range. However, by having a variable reference voltage, flicker compensation may still take place under these conditions. In order to illustrate, a 6% voltage change occurring every 0.2 seconds during light load conditions was simulated. A variable reference voltage reduced the voltage change to 1.5%. Figure 4.17 contains RMS voltages with and without the control modification as

a)



b)

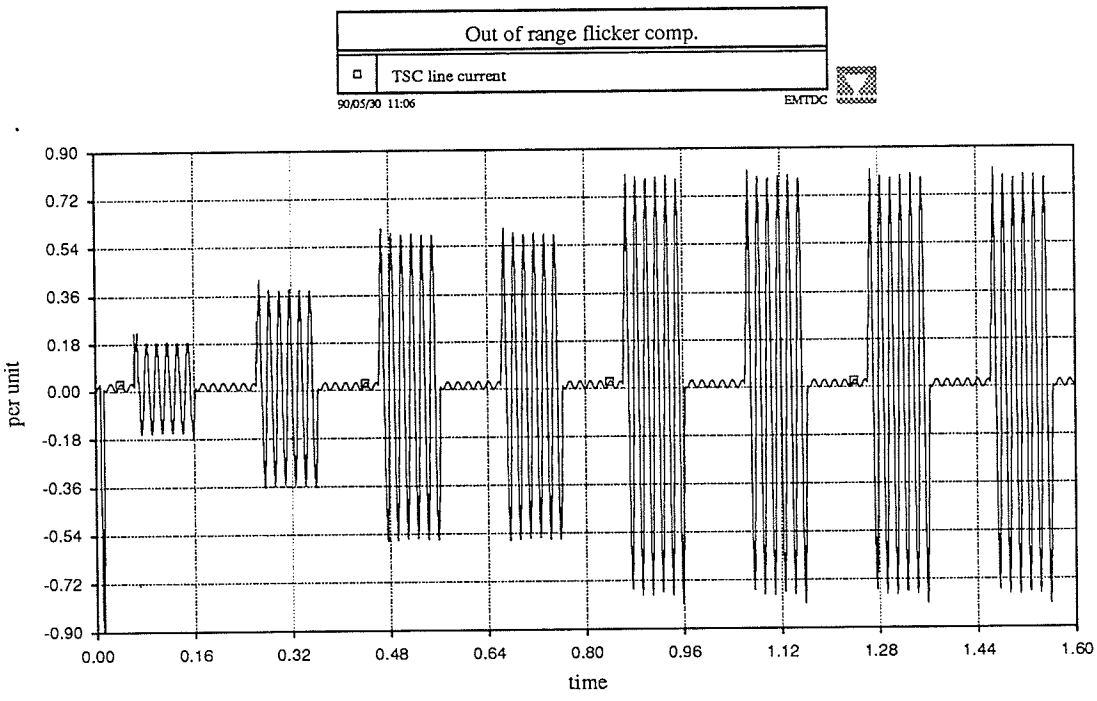


Figure 4.17: *Out of range flicker compensation, a) voltages, b) TSC current*

well as TSC line current and the modified reference voltage. Through simulations, it was discovered that the new reference voltage approaches the midpoint between the original reference setting (1.0 pu) and the steady state "out of range" system voltage. The error signal after the ±0.05 limiting block (Figure 3.15) must be multiplied by 2 in order to better compensate for flicker. The reason for this is that the new reference voltage will be the average between the upper and lower limits of system voltage variation. The compensator will then have plenty of dynamic range for flicker correction.

Protection systems are installed on distribution feeders for the purpose of detecting large currents due to short circuits and the subsequent isolation or de-energization of the faulted portion of the feeder. Radial distribution faults are normally detected by inverse-time overcurrent relays. When a high current is detected, the relay signals a circuit breaker to open and isolate the fault. As the current flowing through the breaker passes through zero, the space between the circuit breaker's contacts becomes a dielectric, thereby preventing fault current from flowing. The entire process from fault initiation until its final clearance takes between 30 and 100 milliseconds (2 - 6 cycles).

Most faults that occur are temporary in nature. Automatic reclosing relays are used to signal a circuit breaker to reclose a few seconds after fault detection. Reclosing can take place instantaneously in contrast to circuit breaking which must occur at a current zero.

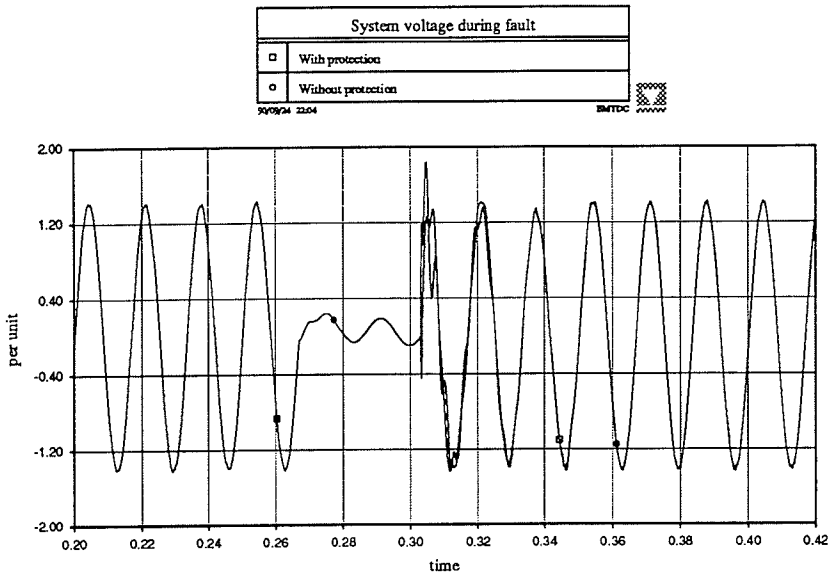
Keeping the aforementioned information in mind, the final load variation to test the TSC model is a low impedance single-line-to-ground fault occurring between the compensator and substation. The fault can take place at any point on the voltage waveform. A fault current of approximately 10 pu results from the short circuit. In a real system, as described previously, overcurrent relays would detect the large fault current and the feeder would be de-energized. Overcurrent relays are not included in the digital model, therefore fault clearing must take place at a current zero, otherwise, large unrealistic transient overvoltages result.

Figures 4.18 a) and b) contain simulation results of the TSC model during a fault when the "direct calculation" control algorithm is used while Figure 4.18 c) shows the waveforms resulting from PI control. PI control and "direct calculation" yield similar results except for the fact that 2 cycles after the fault clears, when the compensators are brought back on line, the TSC line current slowly ramps up to the proper value with PI control, whereas the direct method immediately switches in the correct amount of capacitance.

The system voltage decays to zero in an oscillatory manner after the fault occurs. Since the capacitor voltage follows the system voltage (without considering the magnification

factor), the capacitors become almost completely discharged (depending on factors such as system damping). After fault clearing, a large negative current spike, similar to the one required during startup, is used to charge the capacitors. Capacitors which are charged before a fault remain charged during the fault. After fault clearing, the charge lost because of natural RC decay is restored by the spike of diode current.

a)



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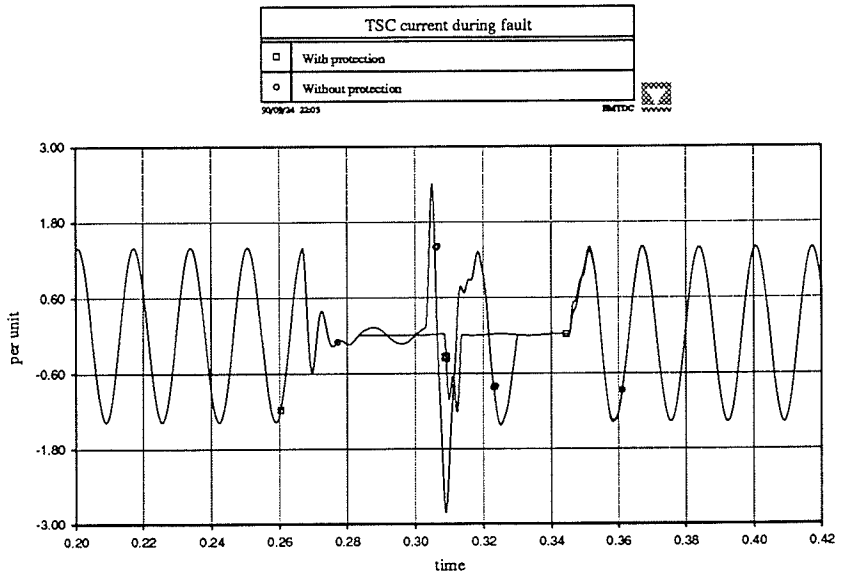


Figure 4.18: *TSC model response following fault, a) system voltage(direct), b) TSC current(direct), c) PI control*

c)

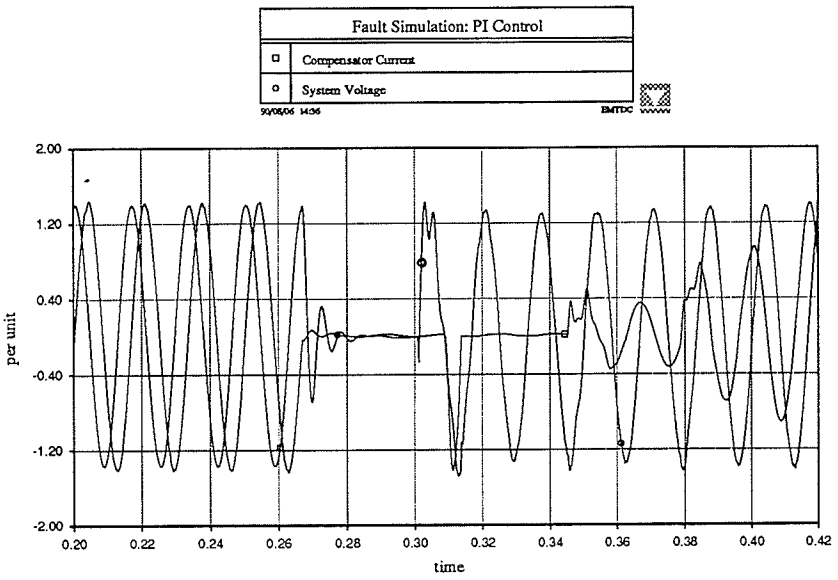


Figure 4.18 cont.: *TSC model response following fault, a) system voltage(direct), b) TSC current(direct), c) PI control*

4.1.4.2 VSI Results

The voltage source inverter model was tested by subjecting it to the same load variations as the TSC was in the previous section. The conditions include:

1. Machine start
2. Single-line-to-ground fault
3. Ramping load

Initial transients are included in all simulations due to the absence of the snapshot feature in the prototype simulation program. Flicker response was not tested after examining the model's response to machine start. It was determined that component sizes and control gains would have to be optimized in order to achieve very fast response times. The optimization problem will not be studied in this thesis.

The simulation results are organized differently in this section as compared with the previous one. Since each load variation was described in some detail in the previous section, all that remains is to comment on the model's response. Therefore, once the appropriate comments have been made, the simulation results will be presented.

The simulation results are presented in Figures 4.19-4.24. In each figure, specific output voltages and currents are given for each load variation. The output variables include:

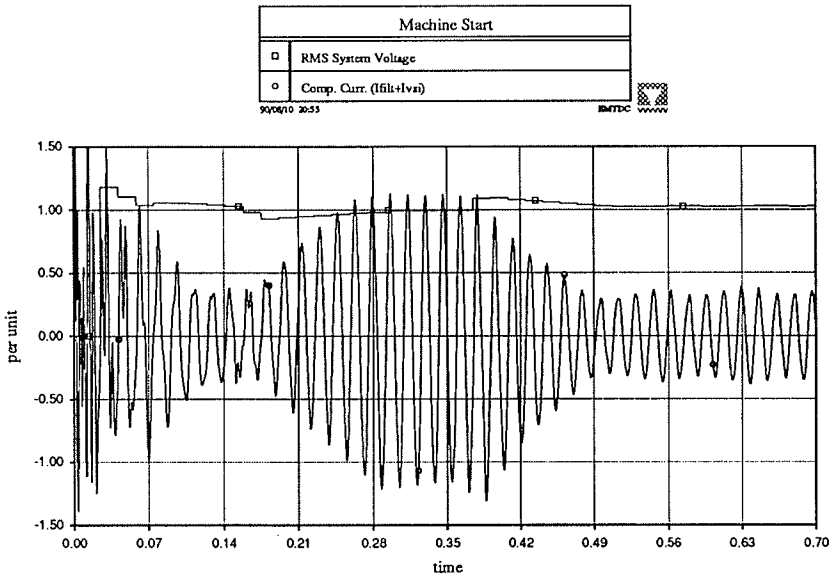
1. RMS system voltage
2. Compensator current (filter + inverter)
3. Capacitor voltage (on inverter)
4. Inverter output voltage
5. VSI output current
6. System voltage
7. Capacitor charging current

Figure 4.19 clearly shows that the single phase voltage source inverter can act as a voltage regulator. After each disturbance, the RMS system voltage returns to the 1 pu reference setting. It should be noted that after a machine start (Fig. 4.19a), the reference does not return to 1 pu as expected. The reason being that the control system is acting on the actual magnitude of capacitor voltage. Actually, the capacitor voltage has a certain percentage of ripple superposed on the dc component (due to charging current). A more accurate control system response would be realized if the capacitor voltage were first sent through a smoothing or averaging filter.

During a fault, the compensator current is not reduced to zero (Fig. 4.19b). The inverter is trying to support the voltage much like a synchronous condensor would be. A large voltage difference exists between the inverter output and system voltage immediately after fault occurrence, hence large 2.0 pu currents result. The GTO's must be capable of withstanding the large currents. A possible sequence of protection that should be employed on the real system to reduce transient currents, overvoltages upon fault clearing and GTO current stress include [21]:

1. Suppress GTO firing pulses
2. Open breaker switch connecting VSI to system (disables large currents flowing while maintaining charge on capacitor)
3. Open breaker switch connecting filters to system (minimize overvoltages upon fault clearing)

The above outlined protection sequence is not included in the model but should be considered for the real system.



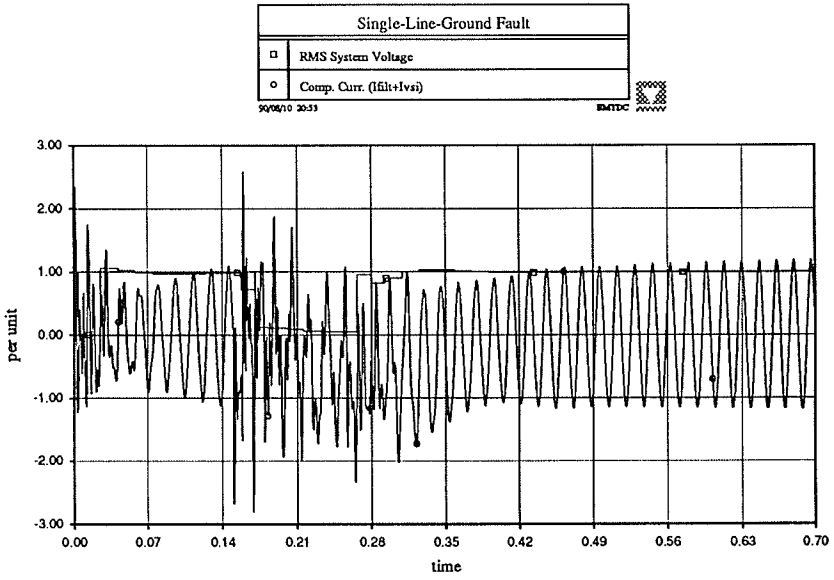
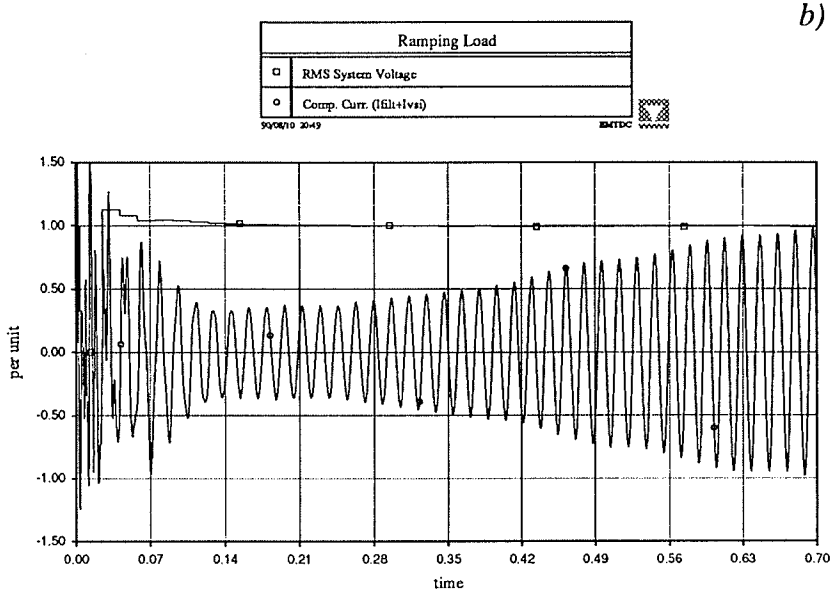
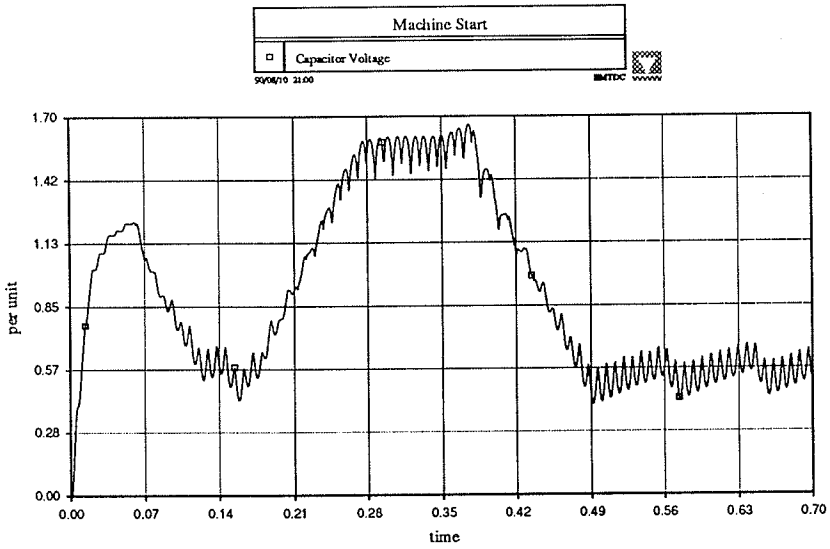


Figure 4.19: *VSI results; RMS voltage, compensator current, a) machine start, b) S-L-G fault, c) ramping load*





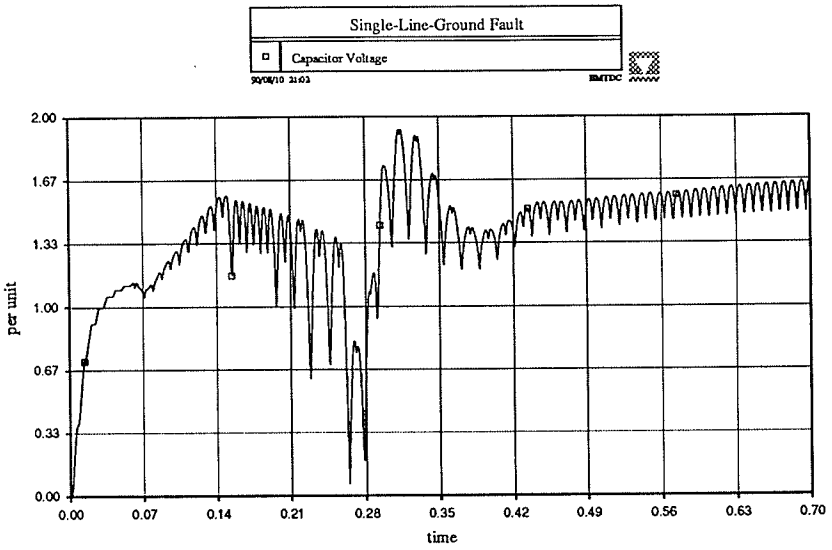
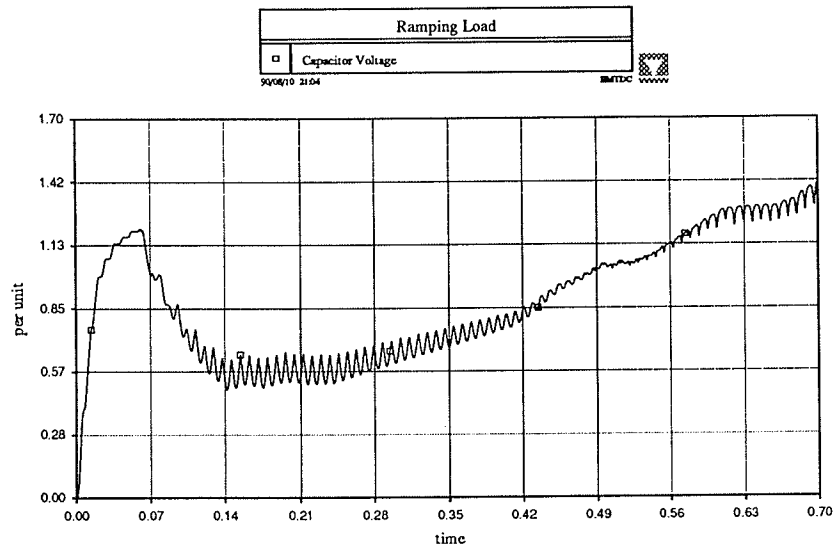
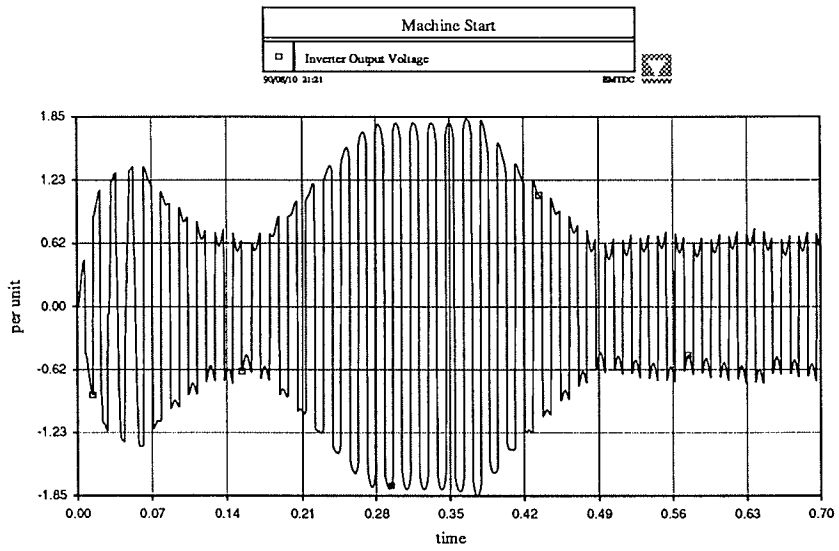


Figure 4.20: *VSI results; capacitor voltage, a) machine start, b) S-L-G fault, c) ramping load*





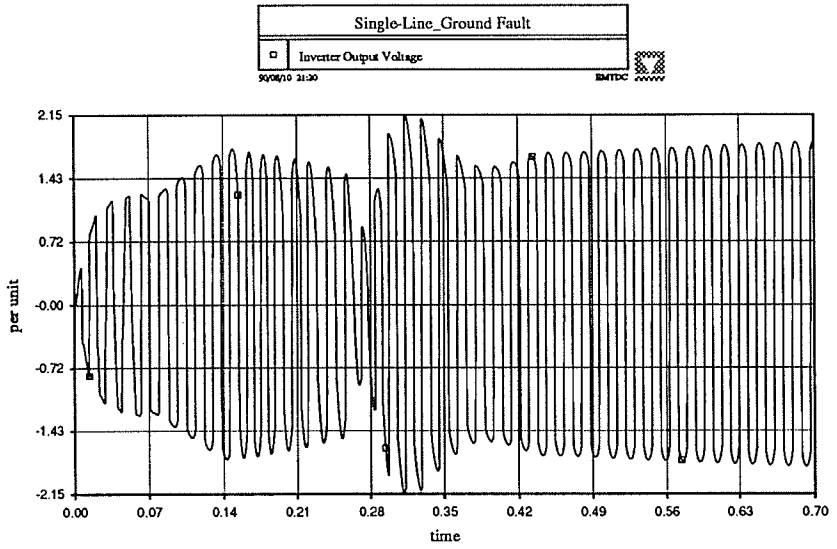
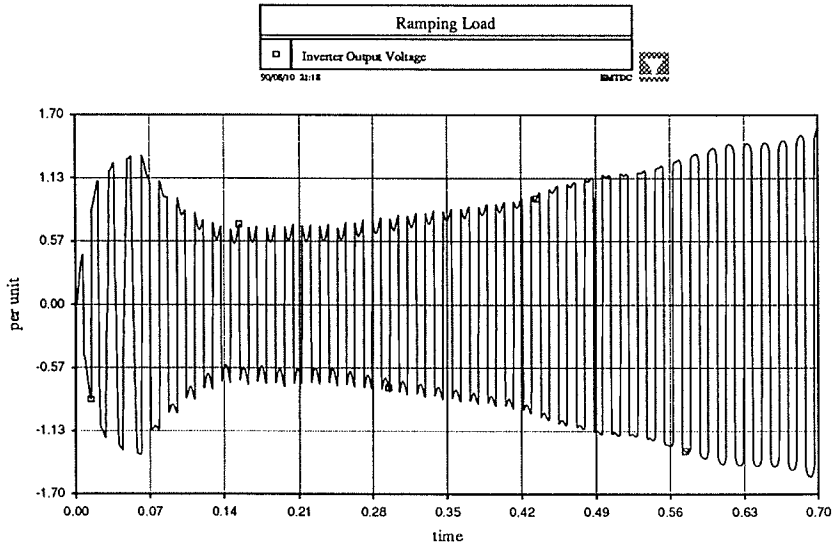
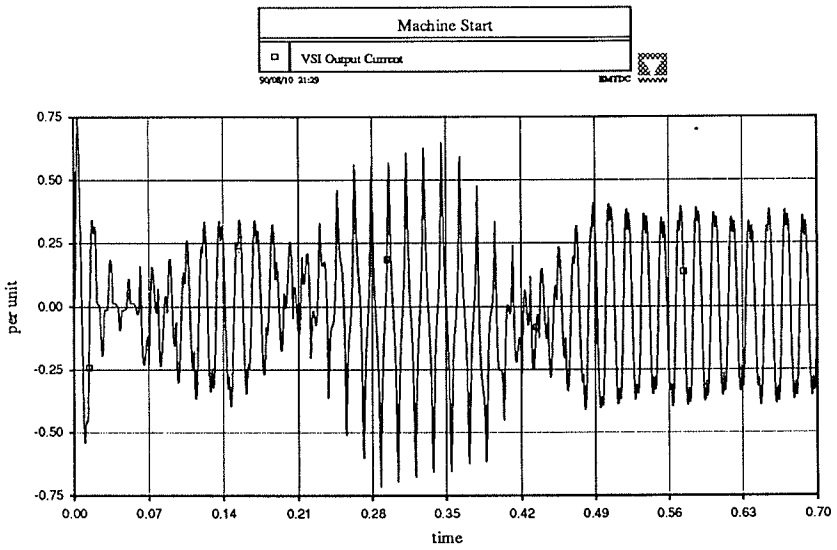


Figure 4.21: *VSI results; inverter output voltage, a) machine start, b) S-L-G fault, c) ramping load*





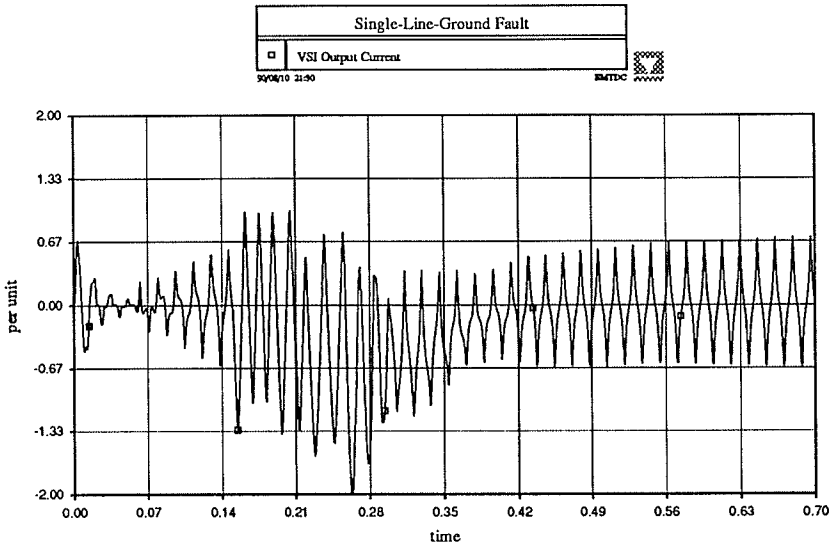
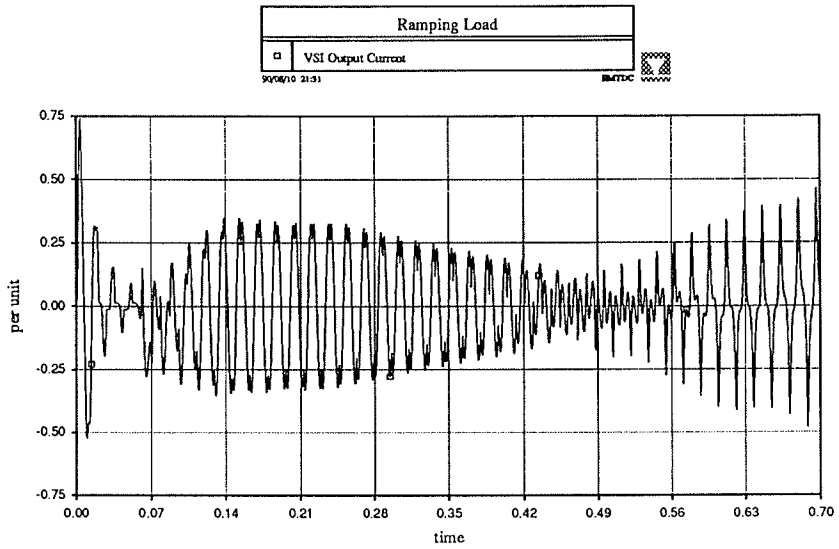
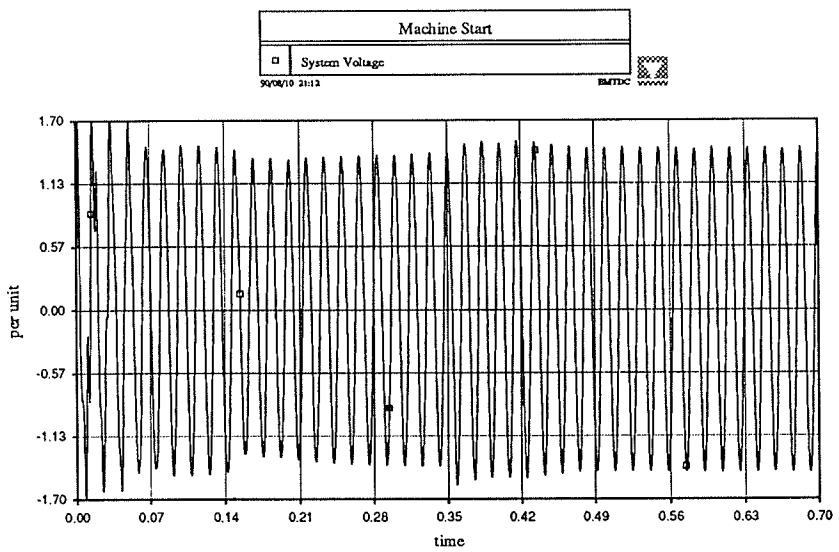


Figure 4.22: *VSI results; inverter output current, a) machine start, b) S-L-G fault, c) ramping load*





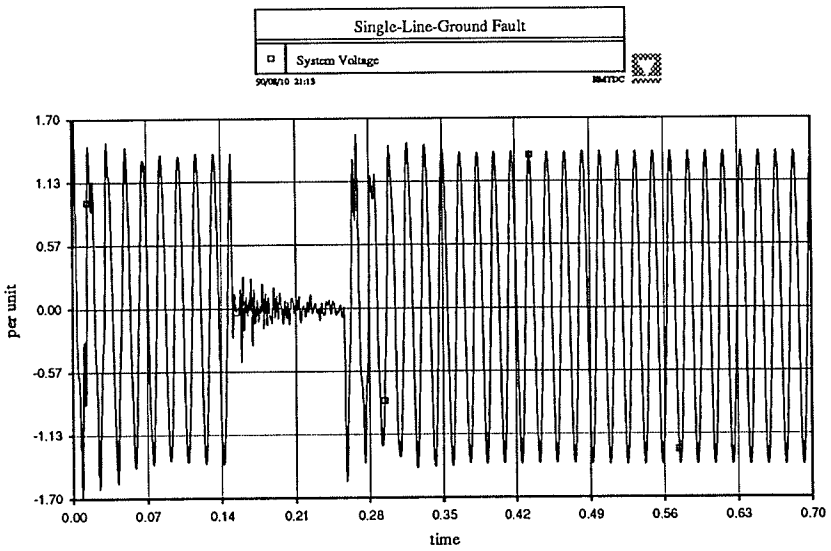
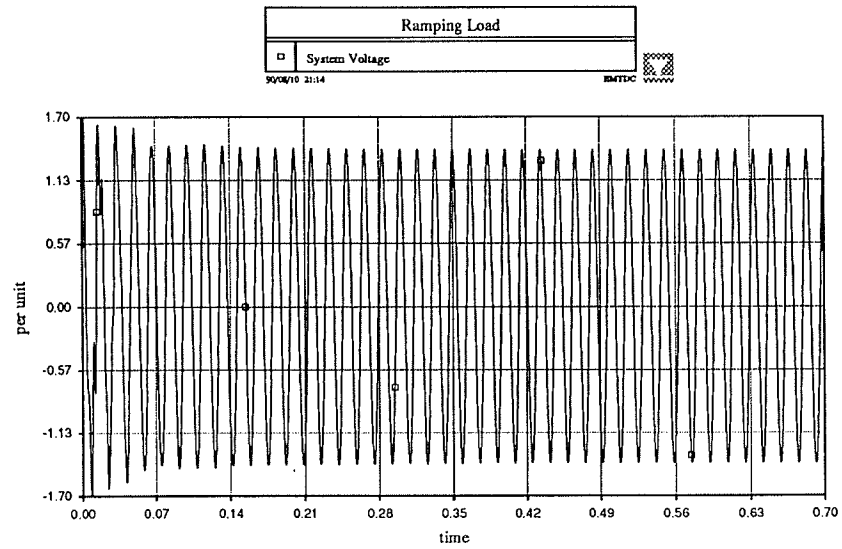
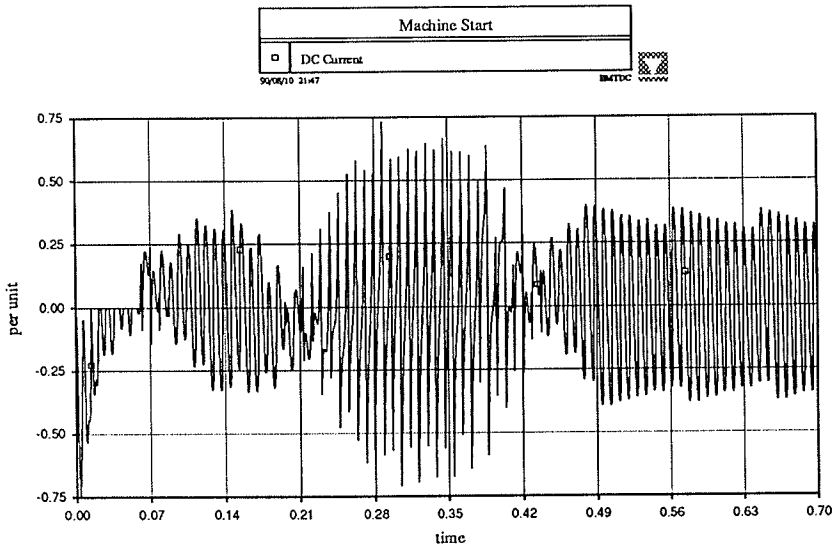


Figure 4.23: *VSI results; system voltage, a) machine start, b) S-L-G fault, c) ramping load*





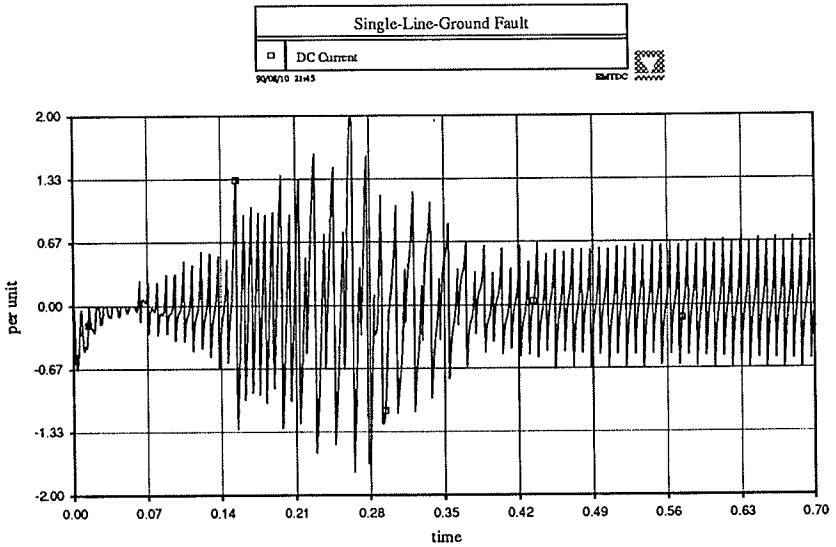
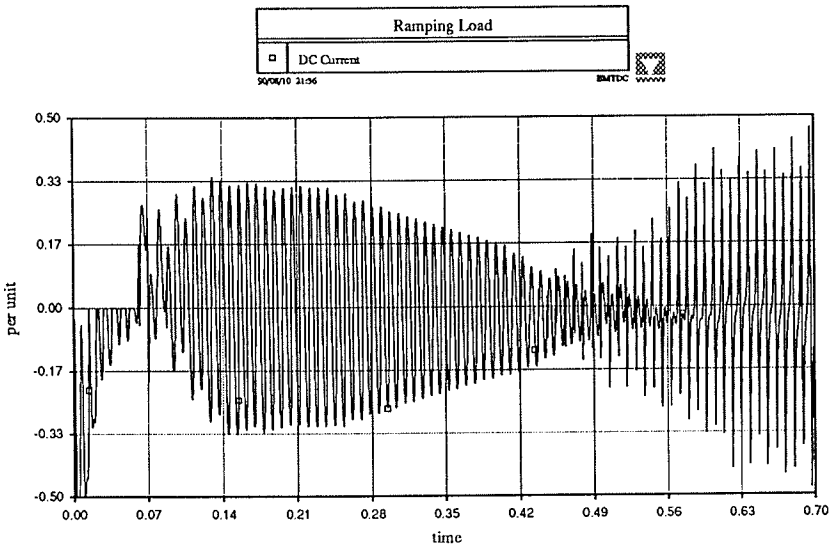


Figure 4.24: *VSI results; dc current, a) machine current, b) S-L-G fault, c) ramping load*



4.2 COMPARITIVE EVALUATION OF TSC AND VSI

A comparison between the two possible candidate single phase compensators must be made at this time before further evaluation takes place (ie. analog simulation). Since the two devices are identical in terms of compensation range and transformer specifications, the following points will be compared and summarized:

1. Inductor and capacitor requirements
2. Switching device requirements
3. Voltage regulating ability during transient load variations

By examining Table 4.1, clearly more components are required to build a single phase VSI. Reducing the need for filters, through various inverter configurations and transformer connections, will reduce the filter requirement and dc capacitor size. However, more inverter bridges and complex transformer connections are required, the cost of which may reduce the advantage of reduced component sizes.

In terms of performance, the TSC utilizing PI control and the VSI have similiar response times. The VSI is able to control the voltage more closely because of its continuous control ability, however. Utilizing the "direct control" method with the TSC produces the fastest response times. Perhaps, with further study, the direct control method could also be applied to the VSI.

The TSC model responds much better, transiently, to faults than does the VSI model. Even with the protection algorithm outlined for the VSI in the previous section, the VSI will still experience large overcurrents and long delays to recover from the fault (6-10 cycles, due to breaker dynamics, as compared with 1-2 with a TSC).

Based on the aforementioned arguments, the thyristor switched capacitor is the best choice for a single phase compensator and will be further evaluated on an analog simulator in the next section.

Table 4.1:

Comparison of Component Requirements

Components	Thyristor Switched Capacitor	Voltage Source Inverter
Capacitors	Bank1: 233.893 µF Bank2: 467.786 µF Bank3: 935.572 µF Total: 1637.251 µF 250 kVAr (secondary)	Filters: n=3 1.136 µF 5 1.227 µF 7 1.253 µF 9 1.263 µF 11 1.268 µF Total: 6.147 µF 150 kVAr (primary) DC Capacitor: 4400 µF 735 kVAr (secondary)
Reactors	Bank1: 0.6685 H Bank2: 0.3343 H Bank3: 0.1671 H Total: 1.17 mH 30.63% (secondary)	Filter Tuning Reactors: n=3 0.6879 H 5 0.2293 H 7 0.1146 H 9 0.0688 H 11 0.0459 H Total: 1.1465 H 200% (primary) Phase Modifier: 3.438 mH 90% (secondary)
Switching Devices	3 - Thyristor-Diodes 2100 Volts 250 Amps	4 - GTO-Diodes 1150 Volts 250 Amps

4.3 ANALOG SIMULATION

The University of Manitoba Real-Time Power System Simulator was used to validate the digital simulations of the thyristor switched capacitor, as well as to provide credibility to the design, since the compensator is operating under near field conditions.

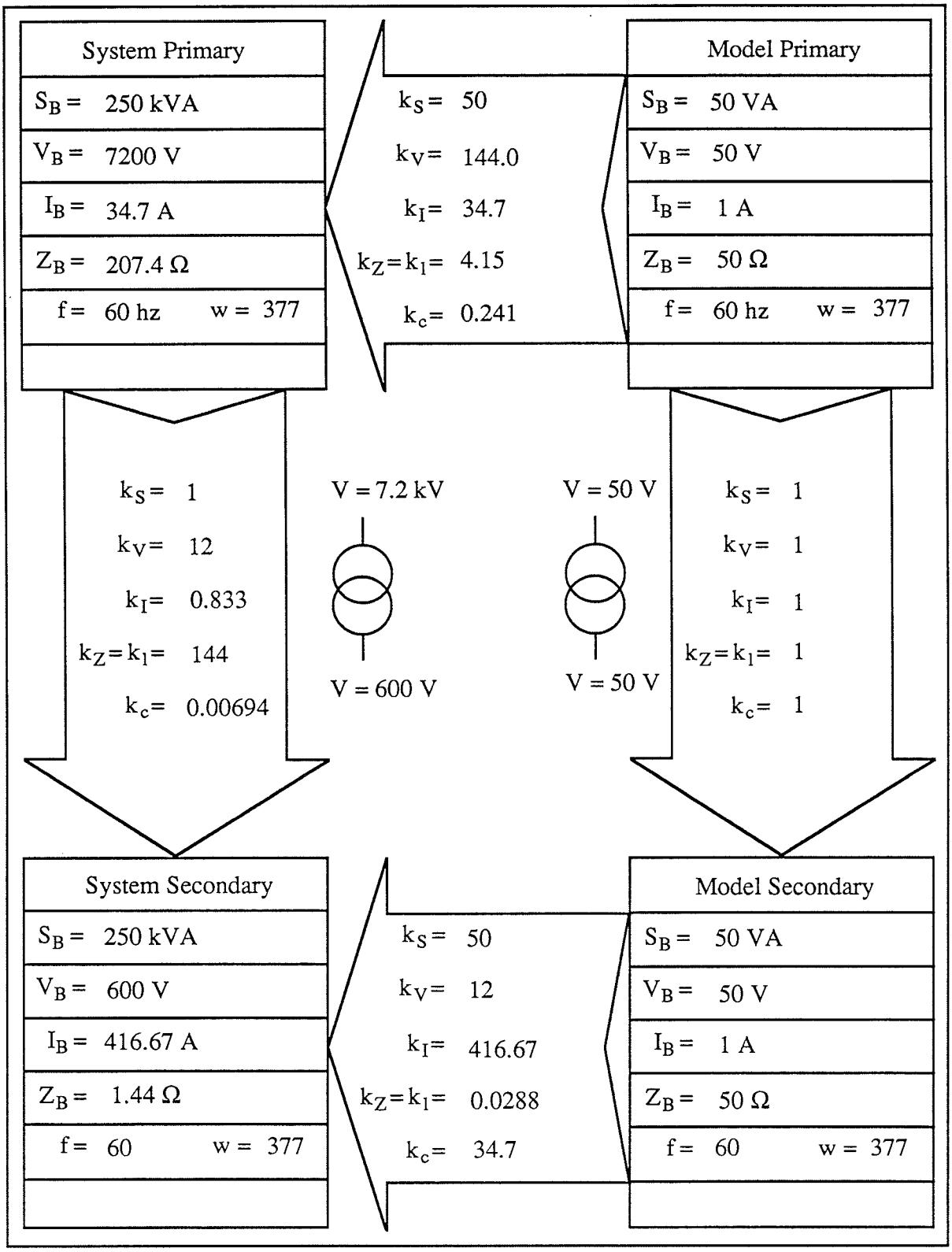
The simulator is composed of programmable and fixed voltage power supplies. Filters, loads and transmission lines can easily be constructed by connecting together scaled down passive components. Section 4.3.1 contains a description of the analog component description. A set of BBC (Brown Boveria Corporation) analog controls are built into the simulator capable of controlling a six or twelve pulse back-to-back dc convertor or thyristor controlled reactor. For this study, a BBC programmable high speed controller (PHSC) is being used to control the compensator [34,35]. A detailed description of the control implementation is included in Section 4.3.2 followed by the results from the analog simulation.

4.3.1 Description of Test System

The simplified St. Agathe feeder model (Fig. 3.12) was used as the test system for analog simulations. Real component values must be converted to equivalent values on the simulator. The base voltage on the simulator is 50 volts as compared with 7200 volts on the real system. Table 4.1 summarizes the base values of the simulator and system. The scaled down passive component values of the test system and compensator are included in Figure 4.25. A TIC106M reverse-blocking triode thyristor is used on the simulator. This device is capable of blocking 600 volts peak and has a continuous current rating of 5 amps. The ratings are much higher than required for this study. The thyristor card was designed previously with adequate protection margins so that it may be applied in circuits with higher base voltages (up to 100 volts RMS) and for use in a variety of applications.

Table 4.2:

Summary of Analog Simulator Base Values



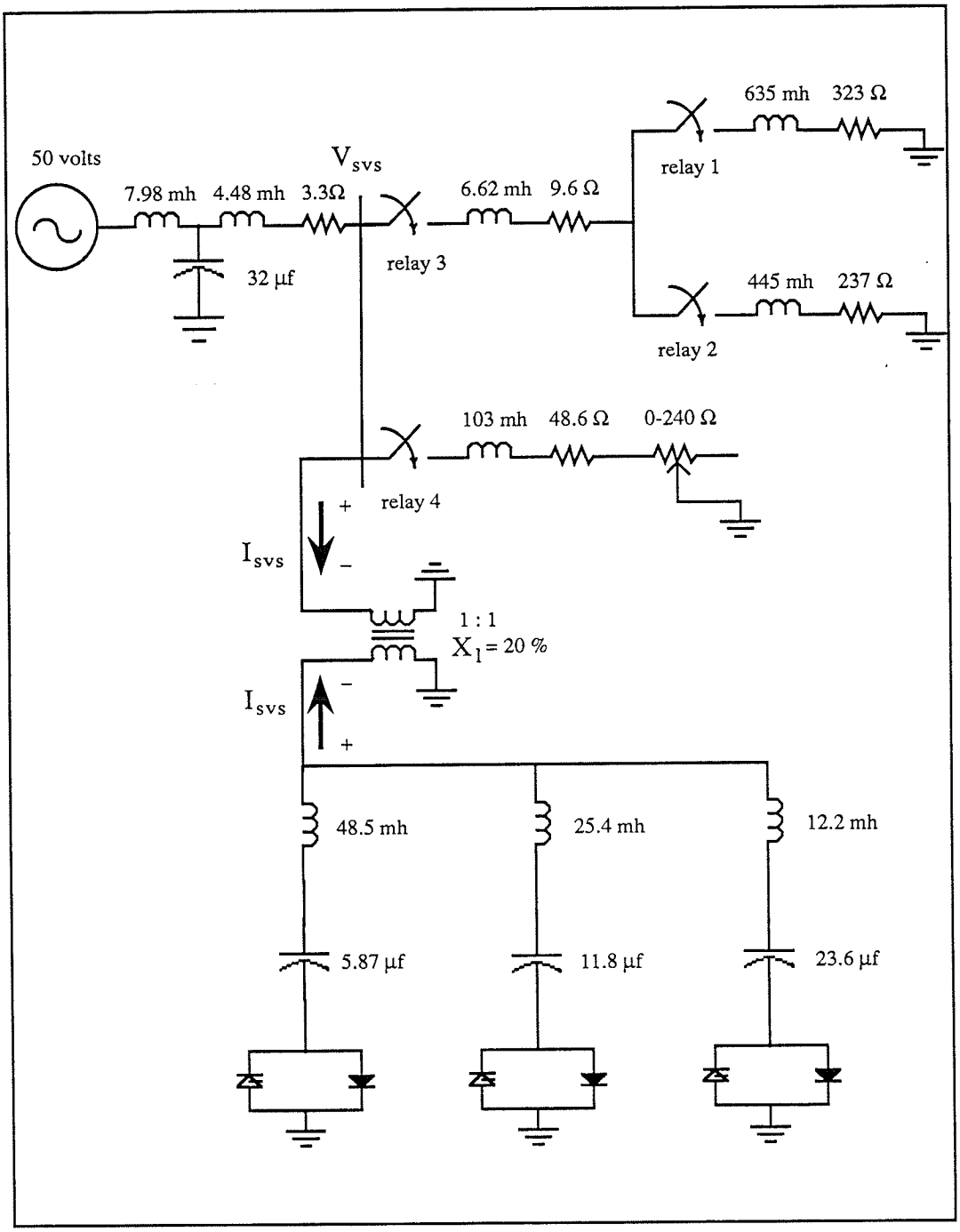


Figure 4.25: *Analog simulation model*

4.3.2 Program Implementation

As mentioned earlier, BBC's programmable high speed controller was used to control the compensator. The PHSC is based on bit-slice microprocessor technology which provides very high control speeds and a user-friendly function block programming language [34,35]. The PHSC consists of a number of hardware modules as shown in Figure 4.26. The two most important are the processing and combined input/output modules [35].

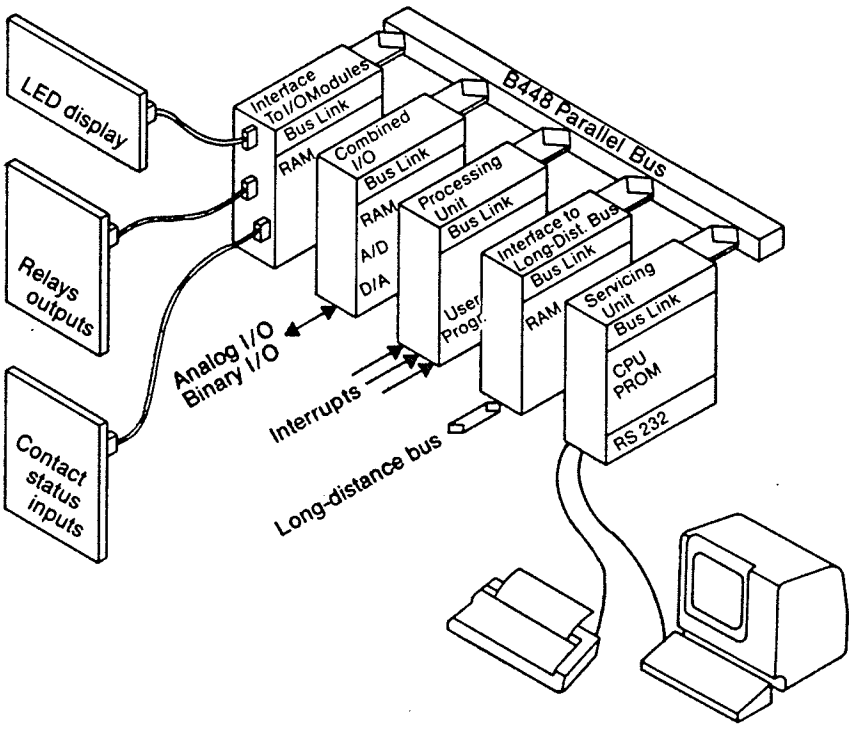


Figure 4.26: *PHSC hardare modules [35]*

The I/O device can process 16 digital inputs, 16 digital outputs, 15 analog outputs and 15 analog inputs. LED's are provided for monitoring the digital outputs while test jacks are provided for monitoring the analog outputs. The analog inputs are fed to an A/D device via a multiplexor. Once the conversion process is complete, an end of conversion signal is generated and the data is loaded into RAM. Similarily, an analog output is first processed by a D/A convertor and then demultiplexed to the appropriate sample and hold location.

The main purpose of the processing module is to process the user written progam in the proper sequence and to react accordingly to interrupt commands. A user program can be divided into at most 8 parts with a choice of 5 levels of priority. A summary of the allowable number of program parts per priority level is included below:

# of Parts		Priority Level
2	-	level 3 (highest priority)
3	-	level 2
1	-	level 1
1	-	level 0
1	-	background (lowest priority)

An interrupt of higher priority will interrupt the processing of a program at a lower priority while interrupts at the same or lower priority will not cause a processing interruption. Other modules which are used but are not shown in Figure 4.26 include phase locked loop, zero crossing detector, pulse logic, comparitor and gamma-measuring. These additional modules are useful in generating firing pulses for an HVDC convertor or TCR compensator.

Three program parts or interrupt routines were found to be necessary to control the thyristor switched capacitor. Each was assigned a different priority and labelled accordingly (INT10-interrupt level 1).

The first program part (INT10) is used to calculate the RMS voltage during the positive half of the supply voltage waveform. The secondary voltage is scaled down by some external circuitry from 50 volts to 10 volts for analog-to-digital conversion. A start conversion signal is supplied by a 120 μs clock signal derived from the processing module. An end of conversion signal initiates INT10. The sampled voltage is squared and integrated. INT21, the next interrupt routine, makes use of this signal in calculating the RMS voltage. The integrator output is set to zero during the negative half of the system voltage immediately following the completion of program INT21.

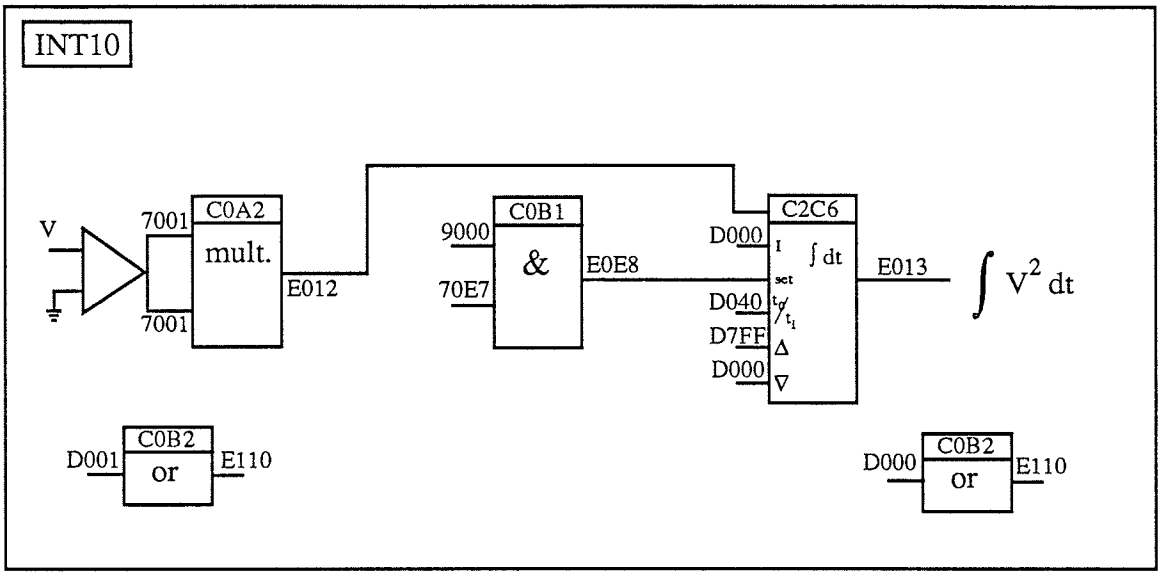


Figure 4.27: *INT10 block diagram*

A positive transition of the zero crossing signal will cause the second interrupt routine (INT21) to begin processing. As mentioned, this routine makes use of the output of INT10 in deriving the RMS value of the secondary voltage. The functional blocks shown in Figure 4.28 are implementing the control algorithm described in Chapter 3. The secondary voltage is initially converted to the system voltage and then compared with the reference setting. The resulting error is converted to desired susceptance by means of PI control. Once the desired capacitive susceptance is calculated, the conversion to binary takes place by function block C0A6. This block is a nonlinear staircase function which converts the input to the desired output. The input varies continuously from 0 - 0.8 pu (note: the value is not 0.90909 pu as expected because the transformer leakage is 20%). The output will vary from 0 to 0.875 pu or 87.5%. The output makes more sense if one examines the data format used by the PHSC. The data format is shown below for direct input.

Dabc D - hex prefix indicating direct input
a,b,c - hex data

generated word:

a	b	c	0

For example, the output corresponding to 80% (all banks on) input will be 87.5% or D380. D380 corresponds to the binary number:

	3	8	0	0
	0 0 1 1	1 0 0 0	0 0 0 0	0 0 0 0
bit location	f e d c	b a 9 8	7 6 5 4	3 2 1 0

The binary signal in bit locations b, c and d are used to fire the thyristors.

To protect against overvoltages upon fault clearing, the secondary voltage is tested before the desired capacitance is converted to binary. A simple test was used in the digital model. A fault was assumed to have taken place if the voltage fell below 0.7 pu. A slightly more detailed protection scheme is used in the analog model. Hysteresis, with a bandwidth of ±4% around 0.7 pu, is being included to prevent inaccurate fault detection due to measurement errors. Once the fault clears, the compensator remains inactive for 2 cycles.

In addition to PI control, the "direct calculation" control algorithm was implemented on the PHSC. The functional blocks in Figure 4.28 are modified and replaced by those in Figure 4.29. Out of range compensation is also included in this block diagram.

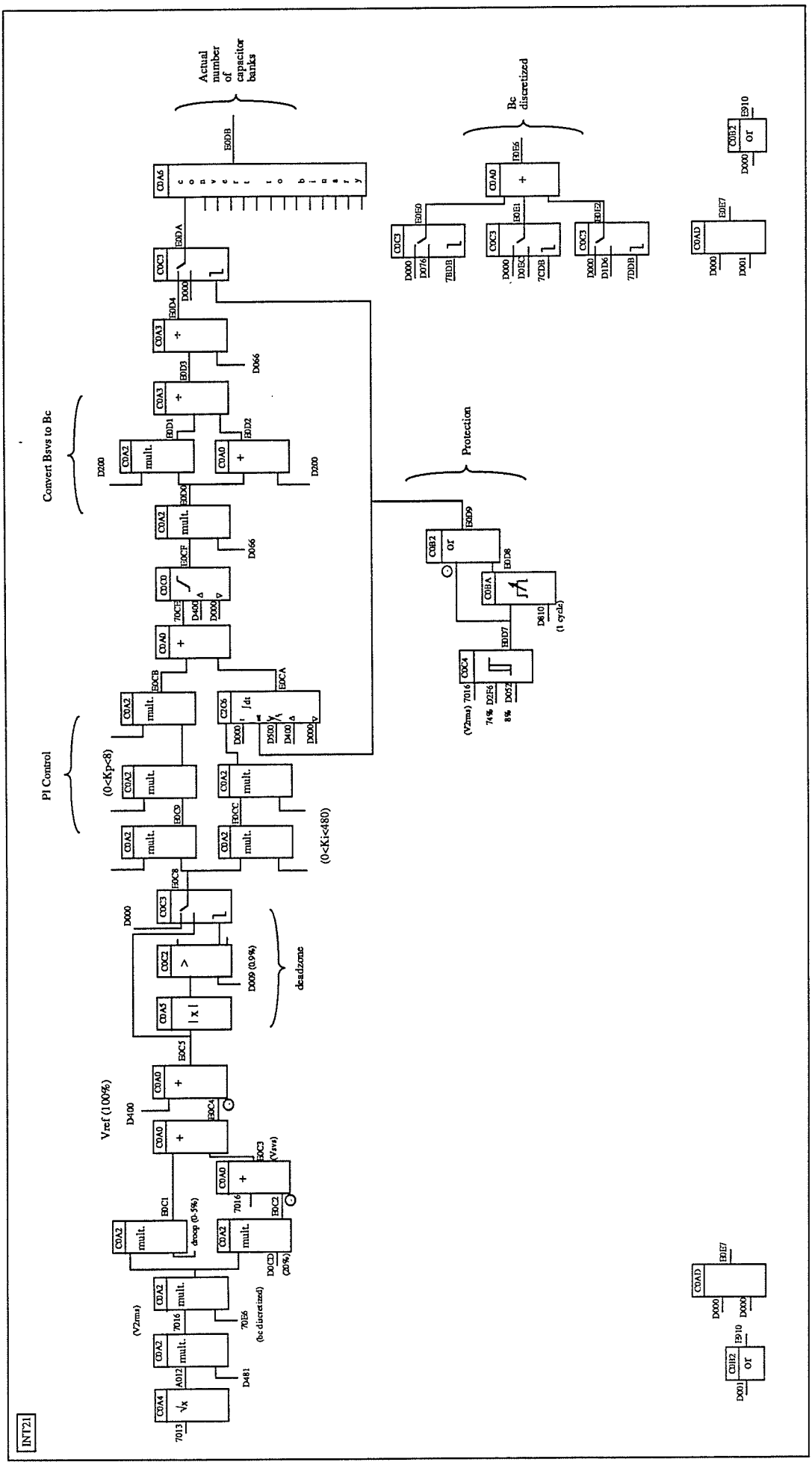


Figure 4.28: *INT21 block diagram*

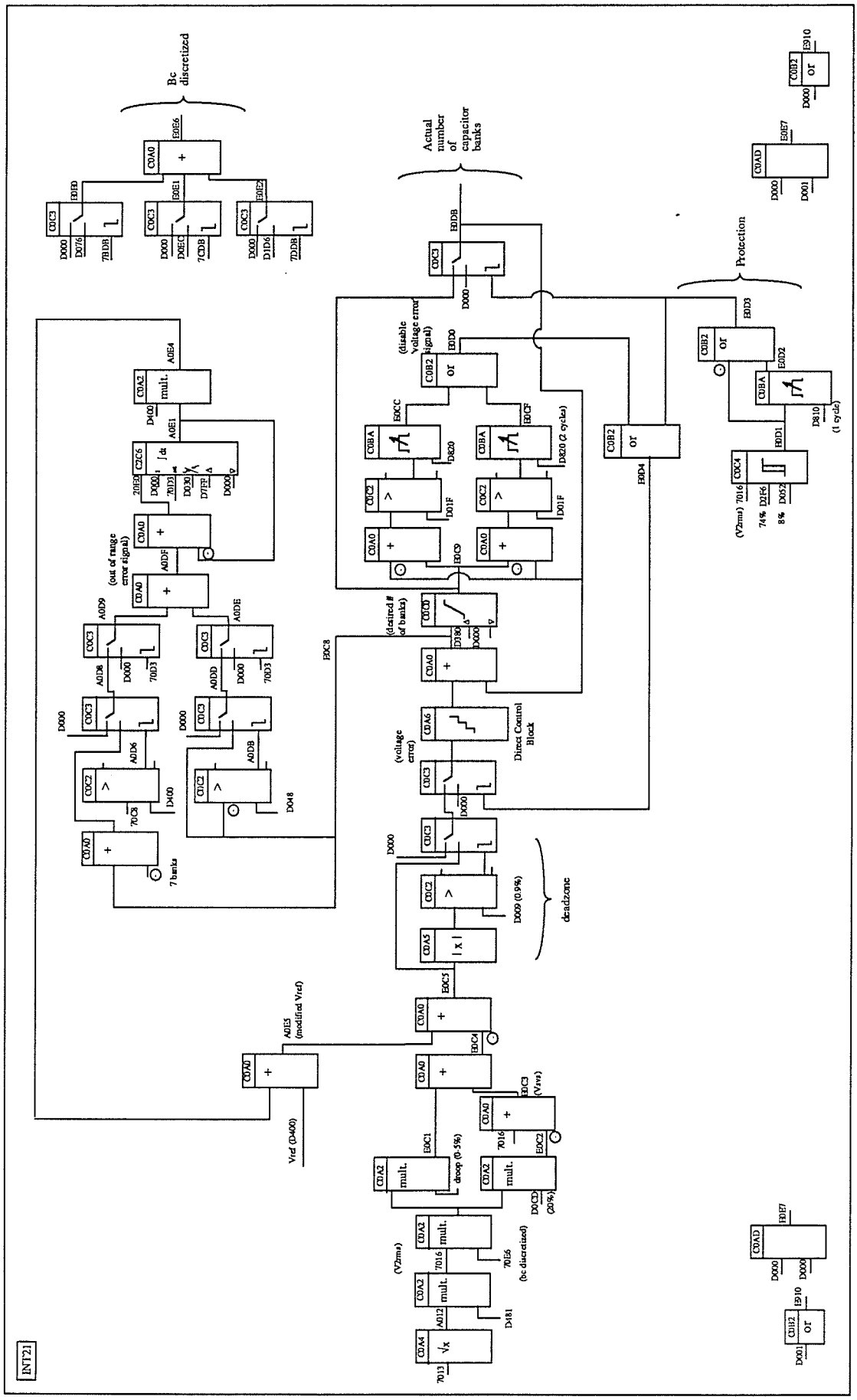


Figure 4.29: *INT21 function block modification*

The final interrupt routine (INT30) is used to determine the appropriate time to fire the thyristors. The routine is processed every clock cycle (120 μs). Once the system voltage becomes negative, a 4 millisecond monostable is triggered. After this monostable has timed out, another 2 ms monostable is triggered. During this time, the thyristors receive the firing pulses which were calculated in INT21. Figure 4.30 contains the functional block diagram.

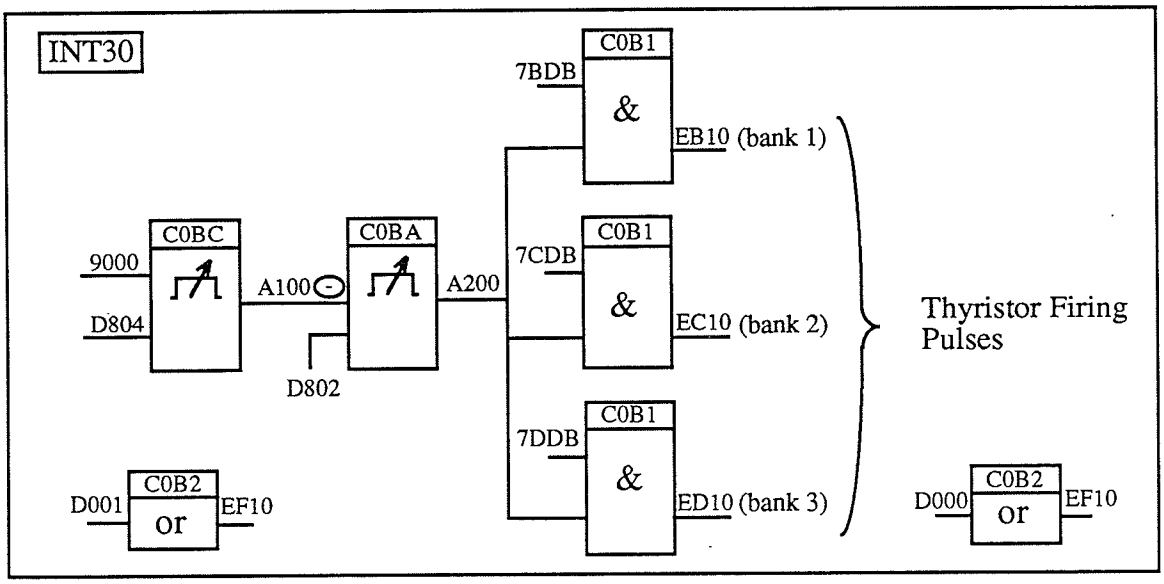


Figure 4.30: *INT30 block diagram*

Correct operation of the controls is very dependent on accurate zero crossing detection. For example, voltage spikes due to breaker switching can cause multiple zero crossings of the system voltage. If the false zero crossing is detected during the negative half of voltage, routine INT21 will read in the value of 0.0 from INT10 since the integrator has been cleared. The compensator will wrongly assume a fault has occurred and will switch off all capacitor banks for 2 cycles. Smoothing of the voltage by low pass filters has been used to correct for inaccurate zero crossing detection.

4.3.3 Simulation Results

The analog model of a thyristor switched capacitor was subjected to the same tests as the digital model was in Section 4.1.4.1. Before presenting these results, program timing will be looked at briefly. Oscillographs of the zero crossing signal, interrupt routine INT21 execution time and the output of INT10 are shown in Figure 4.31. During the negative half of the zero crossing signal, INT10 integrates the square of the system voltage. The positive transition of the zero crossing signal initiates routine INT21. INT21 takes 100 μs to complete, after which, the output of INT10 is immediately set to zero. The programs all work as expected.

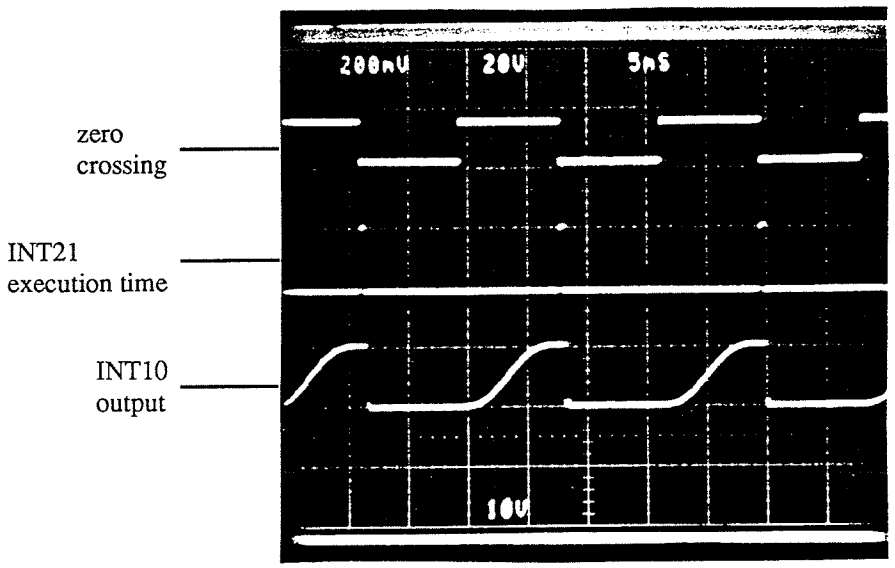


Figure 4.31: *Program timing*

The first load condition tested on the analog model was a slowly increasing or ramping load. In order to simulate such a load, the variable resistance shown in Figure 4.17 was increased from 0 to 240Ω. Figure 4.32 b) contains oscillographs of system voltage and compensator current. For comparison purposes, Figure 4.32 also contains system voltage and load current without compensation. One can observe the smooth, transient free switching of the capacitor banks from this test.

The second test the compensator was subjected to was a simulated motor starting. A 9.5% voltage dip lasting for 0.15 seconds was initiated by switching breaker 4 (Fig. 4.32) on

and off. Within 4 cycles, the compensator reduced the steady state variation to 2%. Figure 4.33 contains the results with and without compensation.

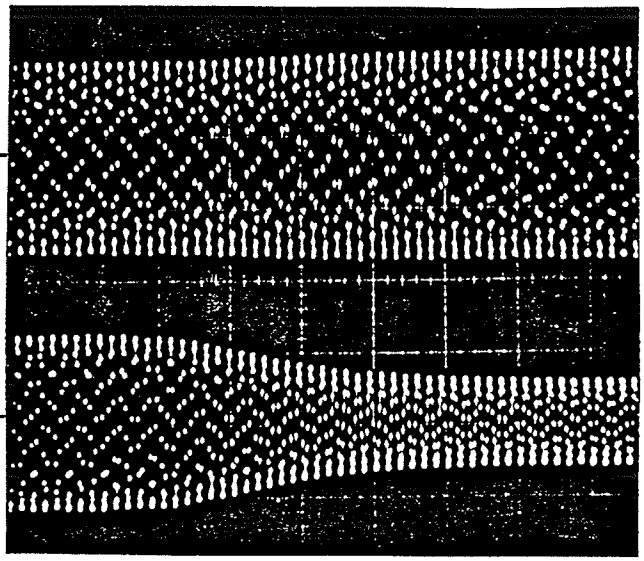
Voltage flicker correction was verified by the third test. Breaker 3 was switched on and off at a frequency of 0.167 seconds, creating a 3.8% change in voltage. With compensation, the change in steady state voltage is 1.19% as shown in Figure 4.34.

Out of range flicker correction was also tested with the results presented in Figure 4.35. The digital signals of the RMS system voltage and the desired change in the number of capacitor banks is presented rather than actual voltage and current as shown in the previous figures. Figure 4.35 a) clearly shows that four or five capacitor banks should be switched off when the load is switched off. After a change in reference voltage has been made, the controller no longer attempts to switch off a large number of capacitor banks, as well the RMS system voltage has become smoother (ie. the flicker condition has been lessened). The RMS voltage is not perfectly symmetrical because of measurement errors and because the point on the wave where switching of the relays takes place is not consistent (resulting in different voltages seen by the compensator).

Finally, the compensator was tested during and after a fault. A single-line-to-ground fault was impractical to simulate. The large fault currents would trip a circuit breaker making high speed reclosing or fault clearing difficult. A more convenient fault to simulate is an open circuit occurring between the main supply and substation transformer. Figure 4.36 contains oscillographs of compensator current and system voltage. The results closely match those predicted during digital simulations (Fig. 4.18c). After fault clearing, a negative current spike through the diode is required to recharge the capacitors. After 2 cycles, PI control slowly switches the correct number of capacitors back on.

The effects of various point on wave fault occurrences and fault clearing are shown in the plots of Figure 4.37. A fault can take place at any time during the cycle without causing any severe voltage transients. The voltage decays to zero in an oscillatory manner, reducing the charge on any capacitors which were on, to a small value. Fault clearing at negative and positive voltage peaks are shown in Figure 4.37 a) and b) respectively. The shape of the current spike is directly related to the time of fault clearing. In each case, the capacitor charging effect is the same, however, less time is available for charging when the fault clears during the negative half of voltage, hence, a larger current spike can be anticipated.

a)



b)

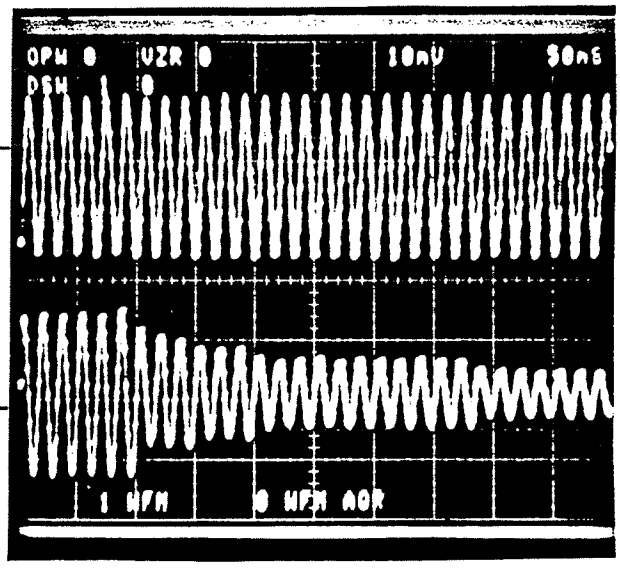
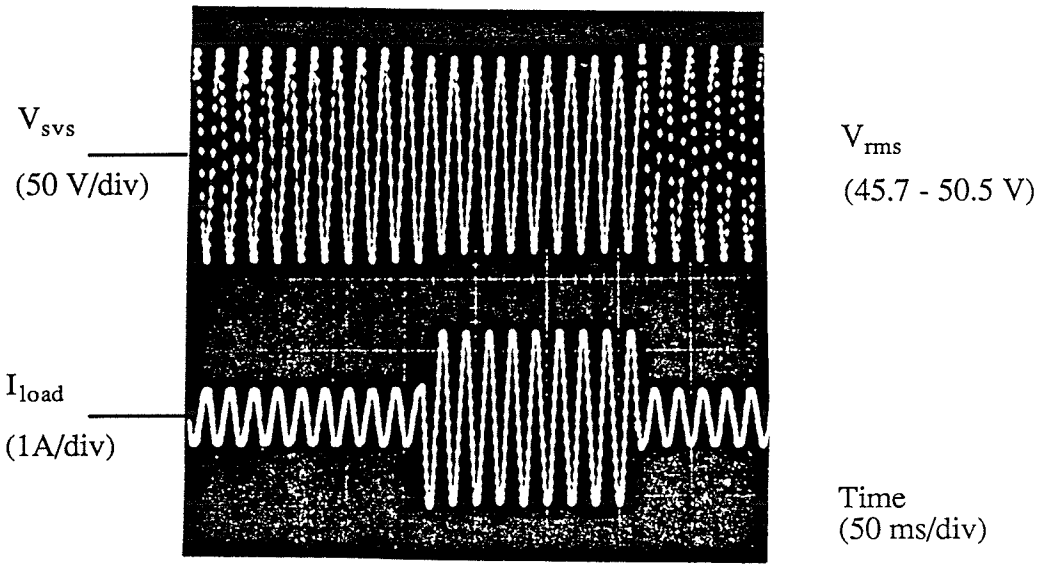


Figure 4.32: *Ramping of load, a) ramping down without compensator, b) ramping down with compensator*

a)



b)

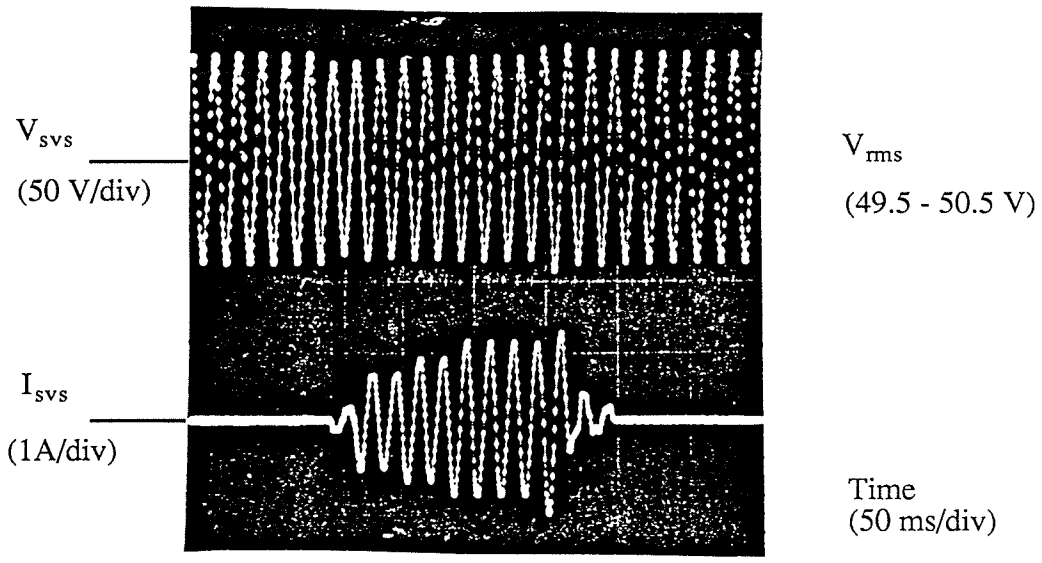


Figure 4.33: *Motor start simulation, a) without compensator, b) with compensator (PI control), c) with compensator (direct control)*

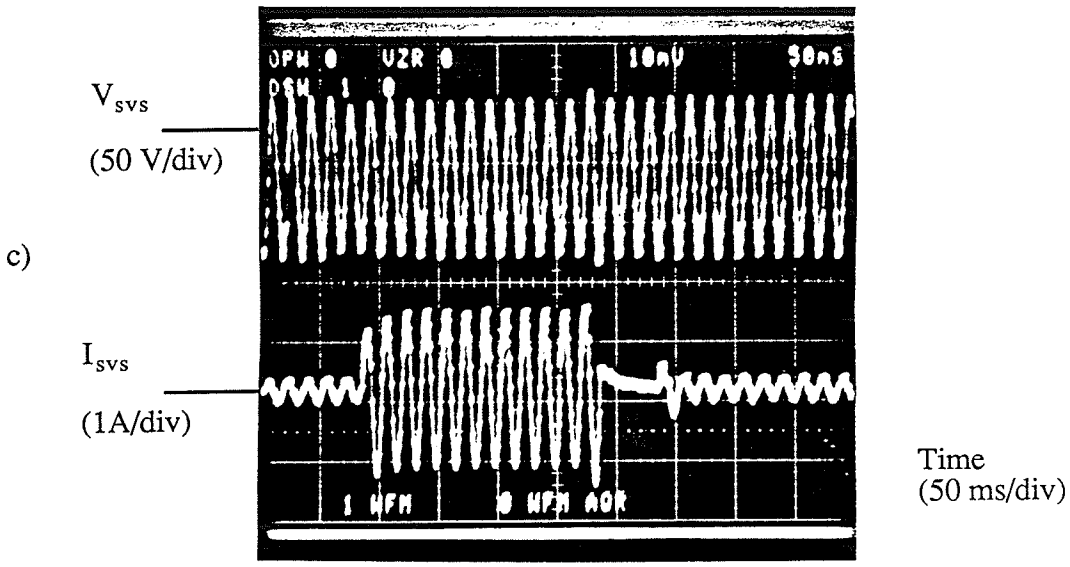


Figure 4.33 cont.: *Motor start simulation, a) without compensator, b) with compensator (PI control), c) with compensator (direct control)*

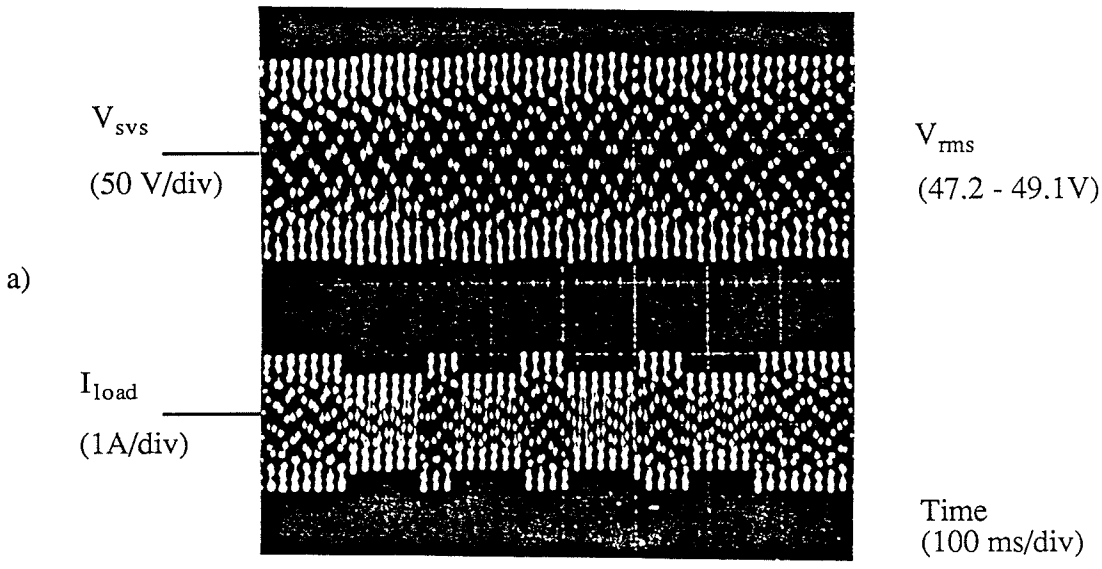
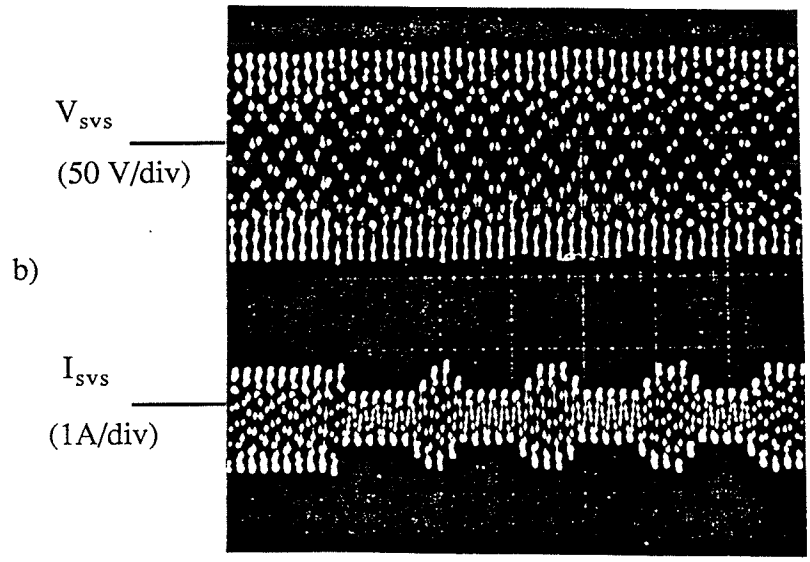


Figure 4.34: *Flicker control, a) without compensator, b) with compensator (PI control), c) with compensator (direct control)*



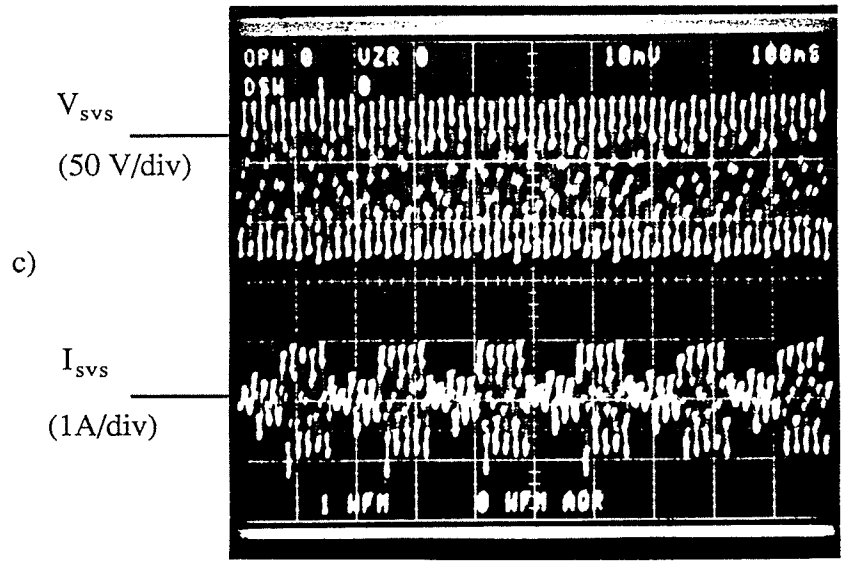


Figure 4.34 cont.: *Flicker control, a) without compensator, b) with compensator (PI control), c) with compensator (direct control)*

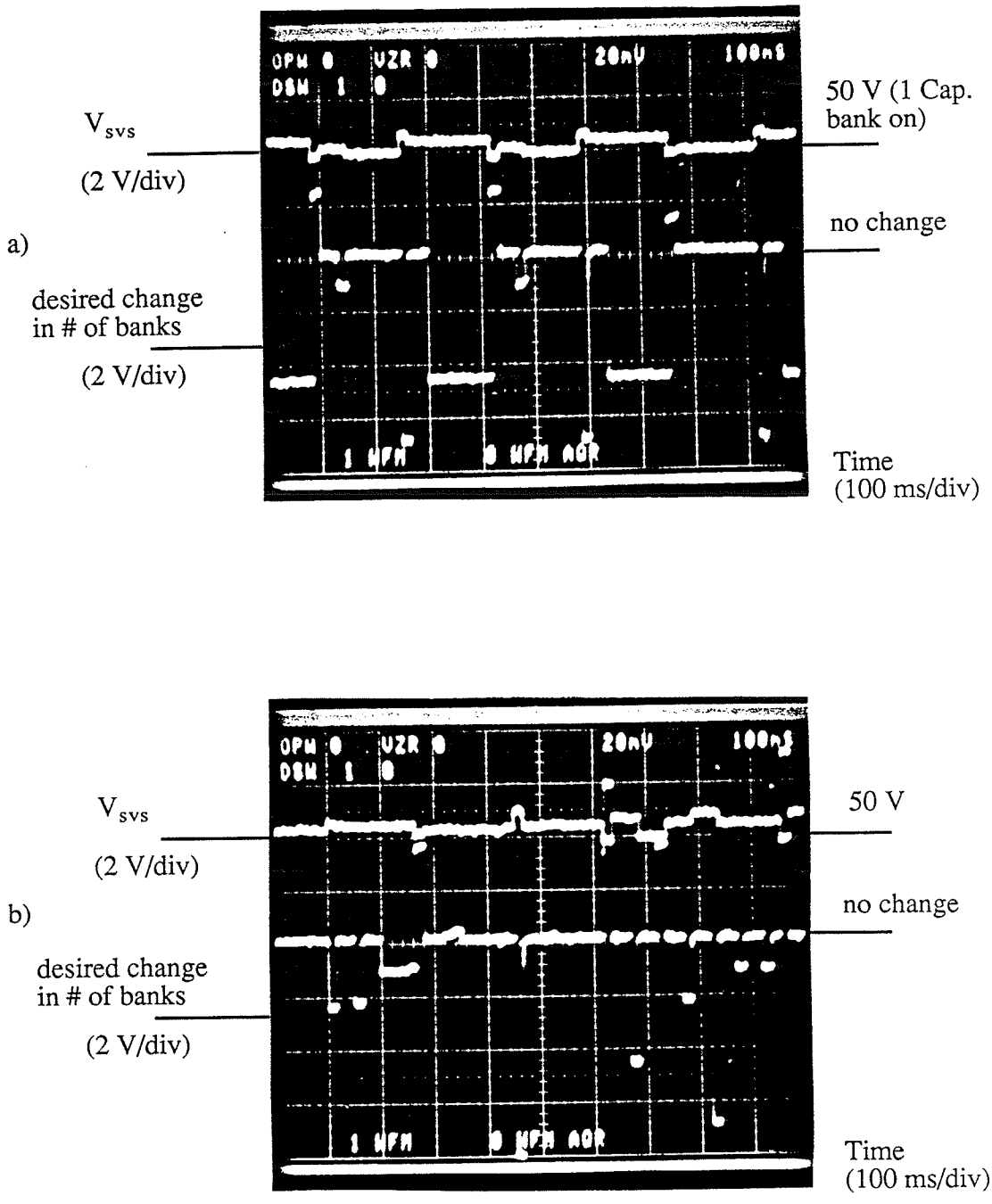


Figure 4.35: *Out of range flicker compensation, a) without modifying reference voltage, b) with modification of reference voltage*

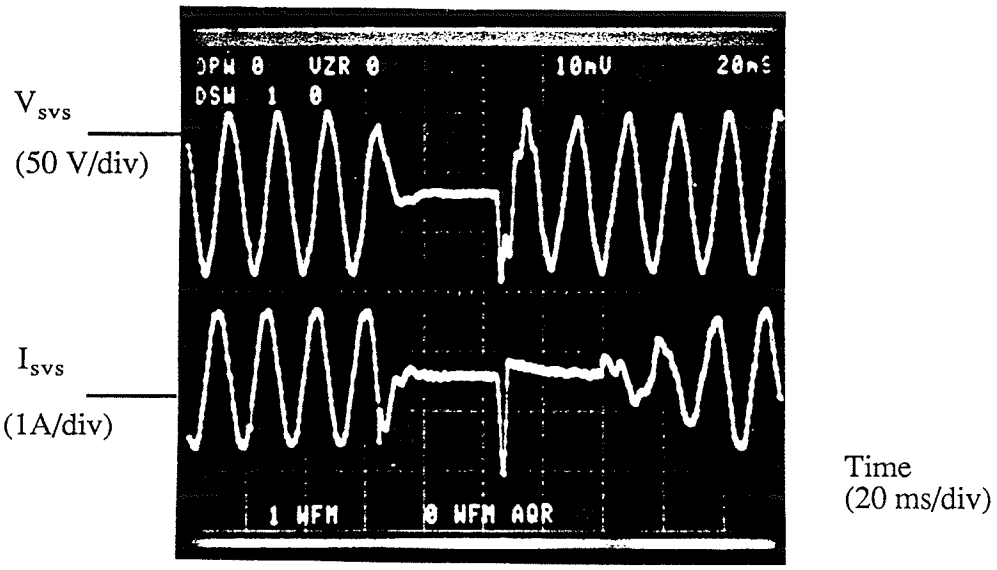
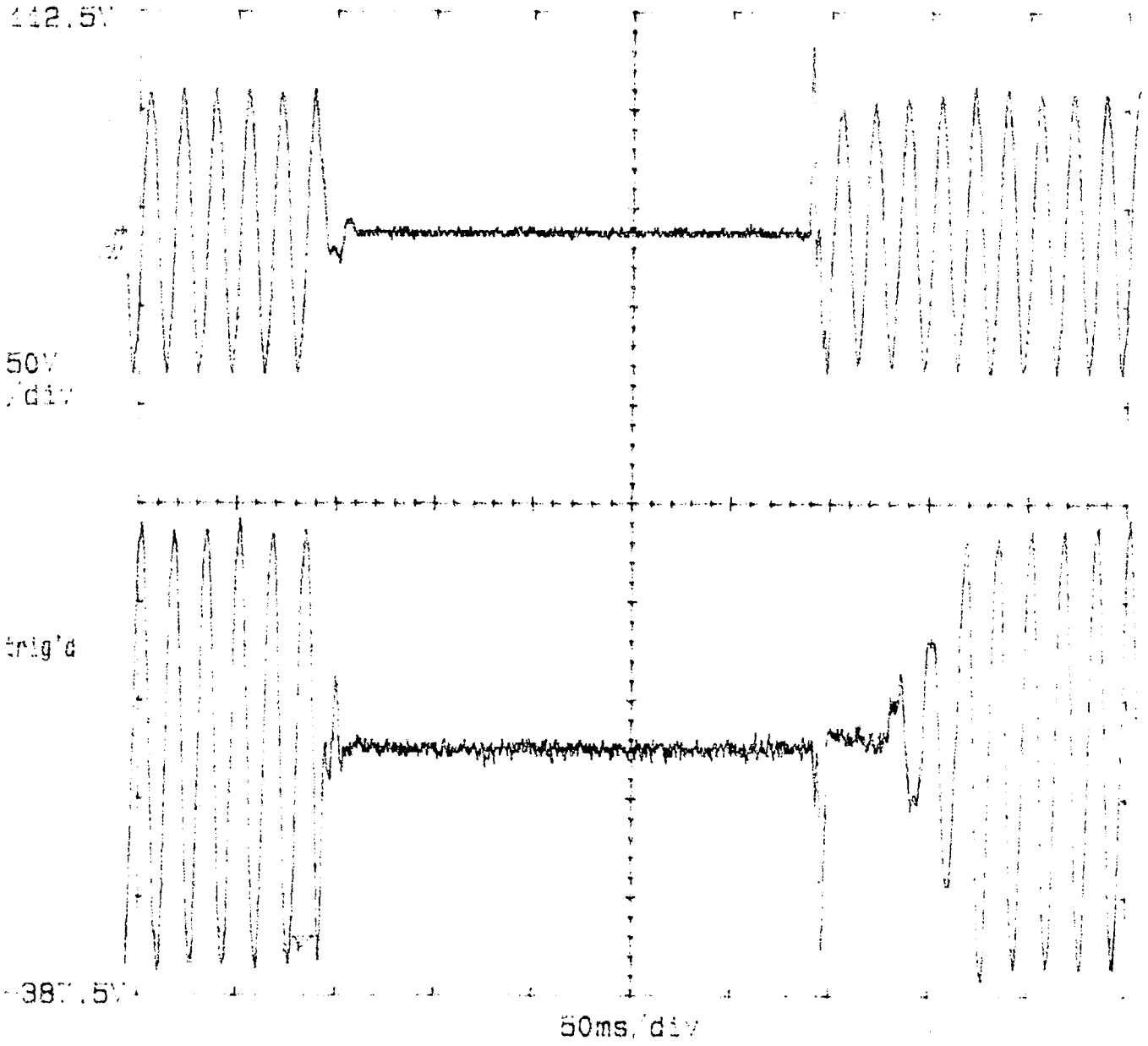
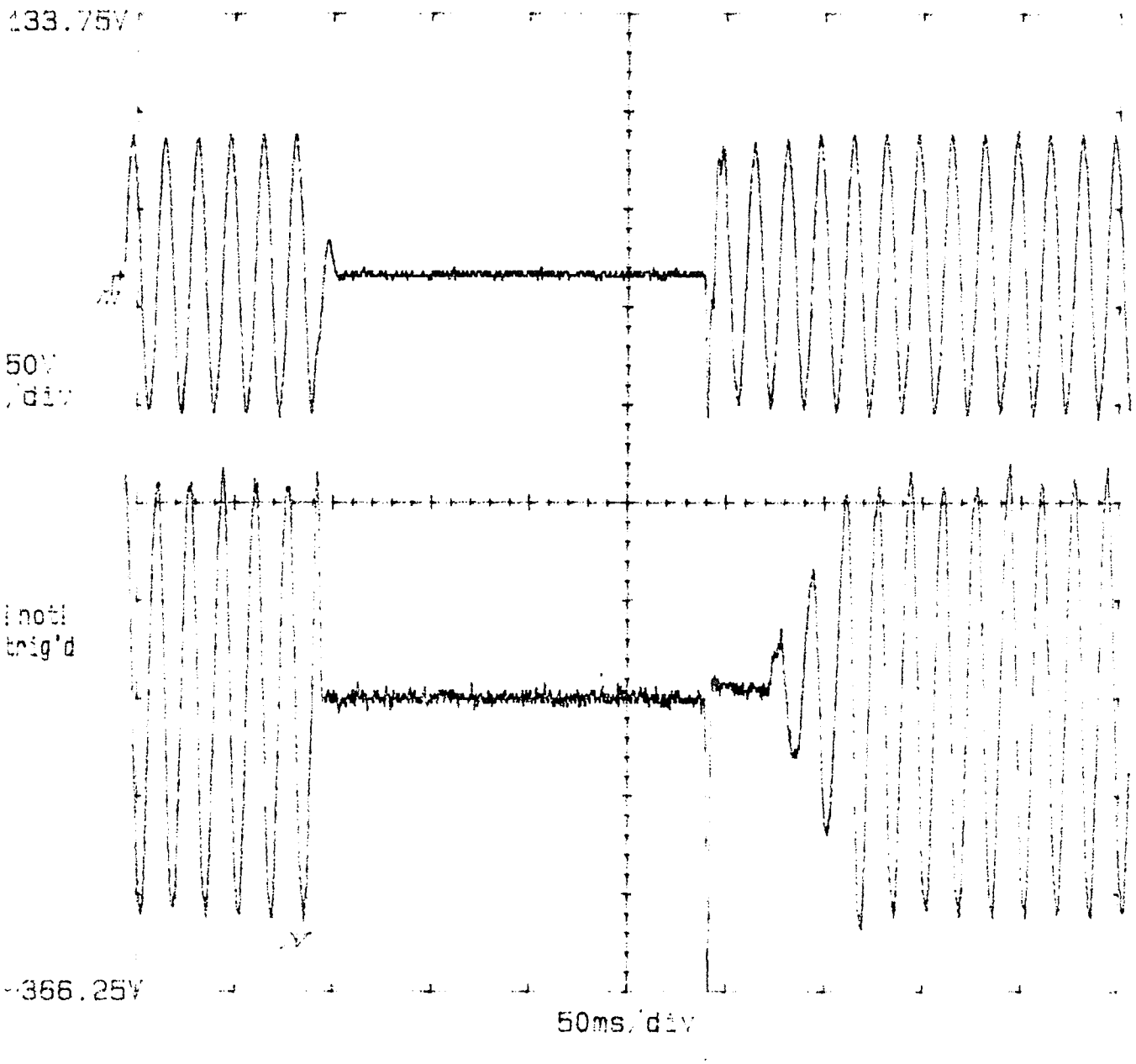


Figure 4.36: *Fault simulation*



a)

Figure 4.37: *Fault analysis, a) fault cleared during positive voltage peak, b) fault cleared during negative voltage peak*



b)

Figure 4.37 cont.: *Fault analysis, a) fault cleared during positive voltage peak, b) fault cleared during negative voltage peak*

4.4 CHAPTER SUMMARY

The thyristor switched capacitor and voltage source inverter, designed in Chapter 3, were tested in this chapter. Both compensators were simulated digitally on electromagnetic transient programs. The TSC was simulated using EMTDC while the VSI was simulated on a prototype power system transient program. While both devices are able to regulate voltage, the TSC was chosen for further study on an analog simulator. Results from the simulations indicate that the TSC is able to regulate the system voltage, as well as correct voltage flicker. Consequently, the major objective of this thesis has been met.

Other conclusions, which can be drawn from this chapter include:

1. Half cycle integration is a fast and accurate method of determining single phase RMS quantities.
2. Switching of capacitor banks in a TSC is transient free except upon startup and immediately after fault recovery.
3. Digital simulations of the TSC show that the "direct" method of control is much faster than PI control. Analog simulation further verifies this point. However, the system impedance needs to be known accurately in order to choose the correct number of capacitor banks for each variation in voltage. A possible adaptive control scheme may be required if large variations in system impedance exist.
4. The VSI control system requires that the capacitor voltage is filtered or averaged in order to reach accurate limits of compensator current.
5. Some optimization of the VSI's component values is required to realize fast response times. By reducing the capacitor size, the time required for charging is reduced. However, more ripple will be superposed on the capacitor voltage which will increase the need for filtering. Filtering slows the response time, therefore, the optimization problem is not straightforward.
6. A VSI requires an adequate protection sequence during faults. One was outlined in Section 4.1.4.2. Even with the protection sequence, the GTO's must be able to handle 300% overcurrent for several cycles.

Chapter 5
Conclusions and Recommendations

5.1 Conclusions

The main objective of this thesis, as stated in Chapter 1, was to design a solid state voltage control device capable of correcting fast voltage fluctuations and thereby replacing the currently used step voltage regulators and mechanically switched capacitors. After observing digital and analog simulations, the conclusion reached was that the thyristor switched capacitor is the best choice for a single phase solid state voltage control device. The TSC requires fewer components and responds more favorably to faults as compared with a voltage source inverter. Also, the TSC responds faster to transient load variations than both the VSI and step voltage regulator are able to, thereby enabling voltage flicker to be eliminated.

Each Chapter of this thesis contains a summary of the conclusions which were drawn during the course of this study. The major conclusions are now stated below:

1. The TSC binary switching scheme has advantages over conventional fixed capacitor switching in terms of number of components and size. By making all of the thyristor-diode switches equal in rating enables fewer spare parts to be stocked and also makes the possibility of switching components in case of device failure. For instance, if the switch for the large capacitor bank fails, one of the other switches being used can be substituted, thereby minimizing the reactive power loss until another switch can be installed.
2. "Direct" control has been shown through digital and analog simulations to outperform PI control in terms of response time. In a real system, however, an accurate knowledge of system impedance variation is needed in order to determine the correct amount of desired compensation.

3. Reference voltage modification is an effective means of compensating for flicker occurring outside of the compensator's normal regulation range.
4. Electromagnetic transient simulation is an effective means of simulating power systems. The new prototype power system simulator, developed by T.L. Maguire, has shown to be quite useful in accurately modelling a single phase VSI.
5. A unique control scheme has been developed for the VSI, utilizing proportional control to convert the voltage error signal to desired phase angle difference. The VSI is now able to operate as an accurate voltage regulator.

5.2 Recommendations

Since the thyristor switched capacitor is found to be the most technically suitable device for correcting single phase voltage flicker, it is recommended that a prototype device be built and field tested. However, field measurements should be carried out at the proposed compensator location before the design is finalized. Variations in voltage and current should be measured over 24 hour periods during expected yearly minimum and maximum loading. Also, the voltage variation allowed with and without a step voltage regulator should be recorded. The purpose of field measurements would be to verify reactive power rating and also for fine tuning of control gains and structure.

The VSI should be studied in more detail. Component values can be optimized with consideration given to alternative filter designs and inverter configurations. A more suitable fault protection scheme than the one outlined in the thesis could also be developed. The control structure provided could be modified to include the "direct" controllability feature. Finally, the possibility of connecting three single phase VSI's together, to act as a single three phase voltage regulator employing individual phase control, should be investigated.

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Appendix A:

Load Flow Program Description

There are various methods that could be used to solve the problem of determining voltages and currents in a radial feeder. The methods include:

1. Newton Raphson
2. Guass Seidal
3. Matrix Inversion
4. Guass Jordan
5. New method proposed by Cespedes [38]

Newton Raphson and Guass Seidal solution methods are both iterative, capable of handling complex networks with automatic tap changers, switched shunt capacitors, multiple generation sources et cetera. A radial load flow can take advantage of simpler solution techniques such as methods 3-5 above.

The Guass Jordan method was chosen for this program. It is more efficient than matrix inversion and contains more information than the new method proposed in [38].

The flow chart in Figure A.1 outlines the structure of the load flow program. Data that must be entered by the user include:

1. Substation voltage and reference angle
2. Leakage reactance of substation transformer (pu)
3. Transmission line type and length
4. Load kVA and power factor

The equivalent impedance of the load is calculated from the input data and an equivalent bus voltage of 1.0 pu. Once the data is entered, a main menu allows the user to make various changes to the input data for contingency studies. Constant power loads are accomodated by feeding back the calculated bus voltages and recalculating the load impedances.

Included in this Appendix is a listing of the computer output from two cases performed on the St. Agathe feeder SA-1. The two cases are:

1. Full load no compensation
2. Full load 250 kVAr compensation

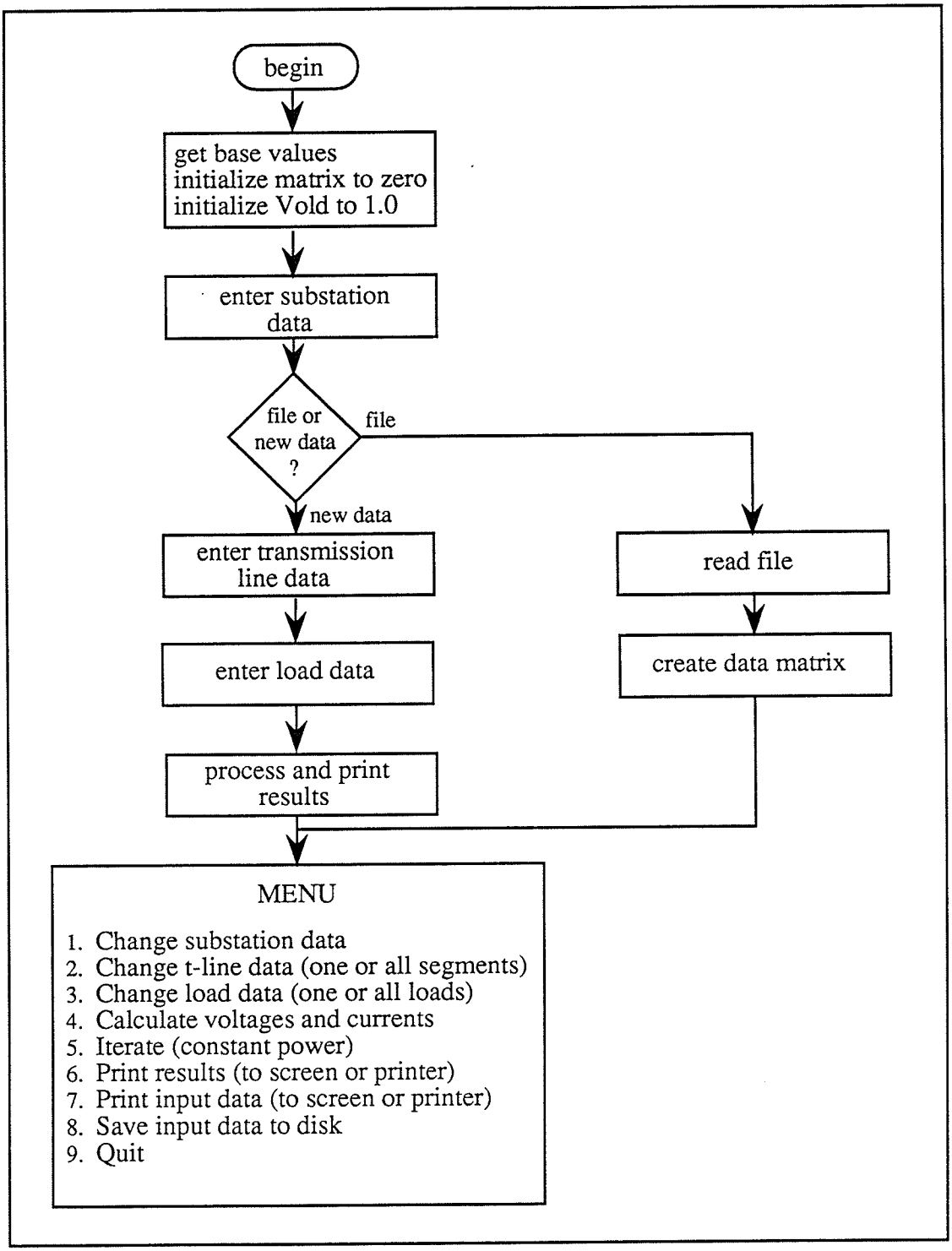

Figure A.1: *Flow chart of load flow program*

Full load: No compensation .

BUS VOLTAGE

Bus	Real	Imaginary	Magnitude	Phase(degrees)
1	0.9989270	-0.0482874	1.0000934	-2.7674811
2	0.9236141	-0.0349971	0.9242769	-2.1699838
3	0.9140088	-0.0304010	0.9145143	-1.9050240
4	0.9130231	-0.0299210	0.9135133	-1.8769871
5	0.9101918	-0.0285830	0.9106405	-1.7986861
6	0.9098799	-0.0284317	0.9103240	-1.7897824
7	0.9034753	-0.0253921	0.9038321	-1.6098719
8	0.9031652	-0.0252430	0.9035179	-1.6009682
9	0.8918664	-0.0198879	0.8920881	-1.2774348
10	0.9181171	-0.0340139	0.9187469	-2.1216948
11	0.9163870	-0.0330596	0.9169832	-2.0661103
12	0.9158101	-0.0327411	0.9163952	-2.0475101
13	0.9149195	-0.0322504	0.9154877	-2.0188111
14	0.9178612	-0.0338309	0.9184845	-2.1108727
15	0.9180318	-0.0339529	0.9186594	-2.1180867
16	0.9143676	-0.0313500	0.9149048	-1.9636727
17	0.9138154	-0.0310802	0.9143438	-1.9479644
18	0.9134433	-0.0308994	0.9139658	-1.9374251
19	0.9129310	-0.0306493	0.9134454	-1.9228383
20	0.9106901	-0.0295595	0.9111697	-1.8590761
21	0.9131011	-0.0312623	0.9136361	-1.9608997
22	0.9127035	-0.0310437	0.9132313	-1.9480461
23	0.9123072	-0.0308271	0.9128279	-1.9353002
24	0.9122653	-0.0308041	0.9127853	-1.9339467
25	0.9119312	-0.0306209	0.9124451	-1.9231608
26	0.9115827	-0.0304296	0.9120904	-1.9118851
27	0.9104984	-0.0298364	0.9109871	-1.8768742
28	0.9097155	-0.0294077	0.9101907	-1.8515161
29	0.9095243	-0.0293032	0.9099962	-1.8453242
30	0.9236141	-0.0349971	0.9242769	-2.1699838
31	0.9989470	-0.0483294	1.0001154	-2.7698314

Full Load: No compensation

BUS CURRENT

Bus			Real	Imaginary	Magnitude	Arg(degree)	Loss
sub	-	1	0.8047898	-0.0178829	0.8049885	-1.2729348	0.0000000
1	-	2	0.7697999	-0.6169311	0.9865069	-38.7092954	0.0661751
2	-	3	0.2087393	-0.1651519	0.2661715	-38.3506051	0.0027641
3	-	4	0.0427480	-0.0343050	0.0548108	-38.7468847	0.0000586
3	-	5	0.1659913	-0.1308469	0.2113623	-38.2478421	0.0008715
5	-	6	0.0199037	-0.0159229	0.0254891	-38.6596798	0.0000086
5	-	7	0.1460877	-0.1149240	0.1858740	-38.1913669	0.0013479
7	-	8	0.0198068	-0.0157386	0.0252985	-38.4708660	0.0000085
7	-	9	0.1262809	-0.0991854	0.1605759	-38.1473325	0.0020119
2	-	10	0.5610606	-0.4517792	0.7203426	-38.8418320	0.0035284
10	-	11	0.2138174	-0.1725183	0.2747370	-38.8982814	0.0005345
11	-	12	0.0713003	-0.0575679	0.0916395	-38.9174077	0.0000595
11	-	13	0.1425171	-0.1149504	0.1830975	-38.8887088	0.0003022
10	-	14	0.0399835	-0.0323558	0.0514351	-38.9807701	0.0000162
10	-	15	0.0199935	-0.0161835	0.0257225	-38.9879835	0.0000027
10	-	16	0.0825675	-0.0663467	0.1059211	-38.7834507	0.0004863
16	-	17	0.0199473	-0.0160483	0.0256016	-38.8178620	0.0000153
16	-	18	0.0626202	-0.0502984	0.0803195	-38.7724825	0.0000805
18	-	19	0.0427173	-0.0343367	0.0548067	-38.7927360	0.0000305
18	-	20	0.0199029	-0.0159617	0.0255128	-38.7289738	0.0000762
10	-	21	0.2046988	-0.1643749	0.2625275	-38.7647715	0.0014791
21	-	22	0.0426922	-0.0343474	0.0547939	-38.8179435	0.0000245
21	-	23	0.1620066	-0.1300275	0.2077337	-38.7507468	0.0001852
23	-	24	0.0085360	-0.0068640	0.0109534	-38.8038439	0.0000005
23	-	25	0.1534706	-0.1231635	0.1967802	-38.7477915	0.0000831
25	-	26	0.0711008	-0.0571293	0.0912090	-38.7817827	0.0000357
25	-	27	0.0823698	-0.0660341	0.1055712	-38.7184248	0.0001698
27	-	28	0.0426077	-0.0341613	0.0546114	-38.7214138	0.0000480
27	-	29	0.0397621	-0.0318728	0.0509598	-38.7152218	0.0000557
2	-	30	-0.0000001	0.0000001	0.0000001	152.4920029	0.0000000
1	-	31	0.0349897	0.5990483	0.6000693	86.6572160	0.0000245

total loss: 0.0804845

Full Load: No compensation

CALCULATED POWER AT LOADS

bus	Kwatts	Kvars	Kva	pf
4	9.5009	-8.1501	12.5176	-0.7590
6	4.4143	-3.7634	5.8008	-0.7610
8	4.3729	-3.6786	5.7144	-0.7652
9	27.6633	-22.7429	35.8120	-0.7725
12	15.8532	-13.7639	20.9945	-0.7551
13	31.6711	-27.4417	41.9059	-0.7558
14	8.9012	-7.7627	11.8106	-0.7537
15	4.4513	-3.8839	5.9075	-0.7535
17	4.4323	-3.8213	5.8522	-0.7574
19	9.4864	-8.1641	12.5157	-0.7580
20	4.4134	-3.7811	5.8116	-0.7594
22	9.4748	-8.1686	12.5099	-0.7574
24	1.8939	-1.6312	2.4995	-0.7577
26	15.7690	-13.5604	20.7977	-0.7582
28	9.4391	-8.0825	12.4267	-0.7596
29	8.8077	-7.5386	11.5933	-0.7597
31	15.9761	149.1816	150.0346	0.1065

total power:374.5046061

Full load: 250 kVAr compensation at bus 30

BUS VOLTAGE

Bus	Real	Imaginary	Magnitude	Phase(degrees)
1	1.0532182	-0.0605254	1.0549559	-3.2890032
2	0.9970352	-0.1138612	1.0035156	-6.5149390
3	0.9870145	-0.1080953	0.9929160	-6.2499793
4	0.9859868	-0.1074945	0.9918292	-6.2219423
5	0.9830317	-0.1058132	0.9887102	-6.1436413
6	0.9827065	-0.1056237	0.9883665	-6.1347376
7	0.9760228	-0.1018062	0.9813180	-5.9548272
8	0.9756994	-0.1016192	0.9809769	-5.9459235
9	0.9639076	-0.0948923	0.9685672	-5.6223900
10	0.9911649	-0.1123446	0.9975115	-6.4666500
11	0.9893705	-0.1111692	0.9955965	-6.4110656
12	0.9887720	-0.1107769	0.9949581	-6.3924653
13	0.9878482	-0.1101724	0.9939729	-6.3637664
14	0.9909030	-0.1121254	0.9972266	-6.4558279
15	0.9910776	-0.1122715	0.9974165	-6.4630420
16	0.9873248	-0.1091522	0.9933400	-6.3086279
17	0.9867492	-0.1088147	0.9927309	-6.2929197
18	0.9863613	-0.1085883	0.9923205	-6.2823804
19	0.9858272	-0.1082755	0.9917554	-6.2677935
20	0.9834908	-0.1069113	0.9892847	-6.2040314
21	0.9859609	-0.1089531	0.9919626	-6.3058549
22	0.9855484	-0.1086837	0.9915230	-6.2930013
23	0.9851372	-0.1084166	0.9910850	-6.2802555
24	0.9850938	-0.1083882	0.9910388	-6.2789019
25	0.9847471	-0.1081625	0.9906694	-6.2681161
26	0.9843855	-0.1079267	0.9902843	-6.2568403
27	0.9832605	-0.1071953	0.9890865	-6.2218294
28	0.9824482	-0.1066668	0.9882217	-6.1964714
29	0.9822498	-0.1065379	0.9880106	-6.1902795
30	0.9970595	-0.1139351	1.0035481	-6.5189749
31	1.0532388	-0.0605699	1.0549790	-3.2913535

Full load: 250 kVAr compensation at bus 30

BUS CURRENT

Bus			Real	Imaginary	Magnitude	Arg(degree)	Loss
sub	-	1	1.0087561	0.8869699	1.3432440	41.3242265	0.0000000
1	-	2	0.9660965	0.2554216	0.9992911	14.8093087	0.0679013
2	-	3	0.2123985	-0.1959652	0.2889905	-42.6955603	0.0032583
3	-	4	0.0434576	-0.0406553	0.0595098	-43.0918399	0.0000691
3	-	5	0.1689409	-0.1553100	0.2294825	-42.5927974	0.0010273
5	-	6	0.0202381	-0.0188754	0.0276743	-43.0046350	0.0000102
5	-	7	0.1487028	-0.1364345	0.2018091	-42.5363221	0.0015889
7	-	8	0.0201485	-0.0186680	0.0274674	-42.8158211	0.0000100
7	-	9	0.1285543	-0.1177665	0.1743421	-42.4922877	0.0023717
2	-	10	0.5702483	-0.5352513	0.7820979	-43.1867873	0.0041593
10	-	11	0.2172902	-0.2043578	0.2982904	-43.2432366	0.0006301
11	-	12	0.0724551	-0.0681885	0.0994958	-43.2623630	0.0000701
11	-	13	0.1448350	-0.1361694	0.1987946	-43.2336640	0.0003562
10	-	14	0.0406250	-0.0383176	0.0558447	-43.3257254	0.0000190
10	-	15	0.0203140	-0.0191650	0.0279277	-43.3329396	0.0000032
10	-	16	0.0839310	-0.0786193	0.1150017	-43.1284060	0.0005733
16	-	17	0.0202751	-0.0190148	0.0277965	-43.1628174	0.0000181
16	-	18	0.0636559	-0.0596045	0.0872053	-43.1174377	0.0000949
18	-	19	0.0434218	-0.0406870	0.0595053	-43.1376912	0.0000359
18	-	20	0.0202341	-0.0189175	0.0277000	-43.0739290	0.0000898
10	-	21	0.2080881	-0.1947917	0.2850341	-43.1097268	0.0017435
21	-	22	0.0433937	-0.0406966	0.0594914	-43.1628987	0.0000289
21	-	23	0.1646944	-0.1540951	0.2255428	-43.0957020	0.0002183
23	-	24	0.0086765	-0.0081332	0.0118925	-43.1487979	0.0000006
23	-	25	0.1560179	-0.1459619	0.2136503	-43.0927467	0.0000980
25	-	26	0.0722752	-0.0676973	0.0990284	-43.1267379	0.0000421
25	-	27	0.0837426	-0.0782646	0.1146219	-43.0633800	0.0002002
27	-	28	0.0433175	-0.0404881	0.0592933	-43.0663690	0.0000566
27	-	29	0.0404251	-0.0377765	0.0553286	-43.0601771	0.0000657
2	-	30	0.1834496	0.9866383	1.0035481	79.4670469	0.0000685
1	-	31	0.0426594	0.6315484	0.6329875	86.1356949	0.0000272

total loss: 0.0848363

Full load: 250 kVAr compensation at bus 30

CALCULATED POWER AT LOADS

bus	Kwatts	Kvars	Kva	pf
4	9.6196	-11.1893	14.7559	-0.6519
6	4.4736	-5.1717	6.8381	-0.6542
8	4.4405	-5.0655	6.7362	-0.6592
9	28.1848	-31.4287	42.2155	-0.6676
12	16.0220	-18.8623	24.7485	-0.6474
13	32.0182	-37.6179	49.3991	-0.6482
14	8.9898	-10.6310	13.9225	-0.6457
15	4.4953	-5.3187	6.9639	-0.6455
17	4.4843	-5.2423	6.8986	-0.6500
19	9.6002	-11.2030	14.7537	-0.6507
20	4.4694	-5.1921	6.8508	-0.6524
22	9.5859	-11.2062	14.7468	-0.6500
24	1.9164	-2.2381	2.9465	-0.6504
26	15.9601	-18.6102	24.5166	-0.6510
28	9.5596	-11.0995	14.6487	-0.6526
29	8.9207	-10.3532	13.6663	-0.6528
30	73.8307	240.7089	251.7772	0.2932
31	20.7958	165.6468	166.9471	0.1246

total power:683.3319191

Appendix B

EMTDC Program Listings

In this Appendix, listings of the relevant simulation programs are provided. The listings include:

1. TSC compensator model with PI control
    a) Dynamics subroutine
    b) Data file

2. TSC compensator model with "Direct" control
    a) Dynamics subroutine
    b) Data file

3. TSC compensator output file

4. VSI compensator model
    a) Dynamics subroutine
    b) Data file

```
      subroutine dsdyn
c
c ************************************************************
c Purpose: Main dynamics subroutine which models a single phase
c          thyristor switched capacitor compensator employing
c          PI control
c
c Author: David Jacobson July 15, 1990 University of Manitoba
c ************************************************************
c
      real limit, intgl3,ldlag2,newtm,rnew
      include 'EMT.E'
      common /s1/time,delt,ich
      common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
      common /s4/var(100),con(100),pgb(25)

c
c ------------------------------
c Variable (1..100) Definitions: tsc1.dyn
c ------------------------------
c
c       Var(1): subsystem interface conductance
c       Var(2): current level below which diode conducts
c       Var(3): kp
c       Var(4): ki
c       Var(5): time load (2) switched in
c       Var(6):  "             "       out
c       Var(7): time load (2) switched in
c       Var(8):  "             "       out
c       Var(9): time load (2) switched in
c       Var(10):  "             "       out
c       Var(11): leakage susceptance of transformer
c       Var(12): compensator deadzone

      next=nexc
      nexc = nexc+2

c     define subsystem voltage

      if (time .gt. 0.0 ) vpeak=1.414214
        es(12,1) =vpeak*sin(6.2832*time*60.0)

c     ramp load up to 200 kva
      goto 50
      if (time .gt. 0.05) then
       stor(next+1)=stor(next+1)+0.5
       if(stor(next+1) .ge. 100) then
        stor(next+1)=0.0
        stor(next+2)=4.0*exp(-5.0*(time-0.05))
        rnew=stor(next+2)
        gdc(7,6,1)=1.0/rnew
        gdc(6,7,1)=gdc(7,6,1)
       end if
      end if
50    continue

c     switch 1 off/on for 5 cycles

      call prll2(var(5),1,3,4,10000000,1,1)
      call prll2(var(6),1,3,4,1,10000000,0)
      call prll2(var(7),1,3,4,10000000,1,1)
      call prll2(var(8),1,3,4,1,10000000,0)
      call prll2(var(9),1,3,4,10000000,1,1)
      call prll2(var(10),1,3,4,1,10000000,0)
```

```
c       define compensator

        call stsc28(1,8,2,1.00,0.000,var(12),var(3),var(4),0.7,var(11))

        return
        end

        subroutine stsc28(ms1,n1,ms2,vref,droop,dedzone,kp,ki,fault,bd)
c
c ****************************************************************
c Purpose: To model three banks of single phase thyristor switched
c          capacitors.
c ****************************************************************

        real limit, intgl3,int3,ldlag2,bank(3),nbank,nbank1,i2rms
        real vref,droop,dedzone,kp,ki,fault,bd,flag
        include 'EMT.E'
        common /s1/time,delt,ich
        common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
        common /s4/var(100),con(100),pgb(25)
c
c ----------------
c Input Arguments:
c ----------------
c
c       ms1: subsystem containing distribution network
c       n1: node which is to be compensated
c       ms2: subsystem containing compensator
c       vref: reference voltage p.u.
c       droop: compensator droop(.01-.05) p.u.
c       dedzone: compensator deadzone where no switching ocurrs
c       kp: proportional gain
c       ki: integral gain
c       fault: voltage level when if detected will turn off compensator
c              for 2 cycles after recovery
c       bd: leakage susceptance of transformer in per unit
c
c ----------------------
c Con(1.100) Definitions:
c ----------------------
c
c       con(1): v2rms
c       con(2): bsvs desired
c       con(3): Vsvs(rms)
c       con(4): i2rms
c       con(5): #banks desired
c       con(6): bank1 indicator
c       con(7): bank2 indicator
c       con(8): bank3 indicator
c       con(9): timer for thyristor firing
c       con(10): thyristor3 resistance
c       con(11): thydio 3 branch conductance
c       con(12): delta Vsvs
c       con(13): bc
c       con(14): b1=kp*deltv
c       con(15): b2=ki/s*deltv

c
c --------------
c Program begins
c --------------
c

        next=nexc
        nexc = nexc+20
```

```
        if (time .le. delt) ggin(n1,ms1) = ggin(n1,ms1) + var(1)

c       interface two subsystems togethor

        es(14,ms2)=vdc(n1,ms1)

c       measure secondary voltage

        v1=vdc(13,ms2)

c       convert to square wave for timing

        if (v1 .gt. 0.0) then
          stor(next+7)=1.0
          stor(next+3)=0.0
          stor(next+2)=stor(next+2)+0.5
        else
          stor(next+7)=-1.0
        end if


c
c positive half of cycle
c

        if (stor(next+7) .gt. 0.0) then
          nexc=nexc+3
          stor(next+3)=0.0

c        rms meter

          v2=v1*v1
          stor(next+1)=stor(next+1)+v2*delt
          stor(next+2) = stor(next+2) + 0.5
          count = 200.0

        end if

c
c       negative half of cycle
c

        if (stor(next+7) .le. 0.0) then

c         calculate rms voltage

         if (stor(next+3) .eq. 20.0 .and. stor(next+2) .gt. 164.) then
          stor(next+1) = sqrt(stor(next+1)/((stor(next+2)+1)*delt))
          v2rms=stor(next+1)
          stor(next+5)=stor(next+1)
          stor(next+1)=0.0
         end if


c
c         control data
c

         if (stor(next+3) .eq. 40.0 .and. stor(next+2) .gt. 164.) then
          stor(next+2)=0.0
          bc=stor(next+4)*0.12987
          stor(next+16)=bc
          vsvs=stor(next+5)-stor(next+5)*abs(bc/bd)
          stor(next+6)=vsvs
          i2rms=bc*stor(next+5)
```

```
            stor(next+14)=i2rms
            deltv=vref-(i2rms*droop+vsvs)
            stor(next+15)=deltv
            if (abs(deltv) .le. dedzone) deltv=0.0

c           determine number of capacitor banks to be on

            flag=stor(next+20)
            b1 = kp*deltv
            stor(next+17)=b1
            tc=1.0/ki
            b2 = int3(0.0,0.0,1.0,tc,0.01667,flag,deltv)
            stor(next+18)=b2
            b3 = b1+b2
            bsvs = limit(0.0,1.0,b3)
            stor(next+13)=bsvs
            bcnew = bd*bsvs/(bd+bsvs)
            nbank = aint(bcnew/.12987)
            dummy = bcnew/.12987 - nbank
            if (dummy .ge. 0.5) nbank=nbank+1.0
            nbank1=limit(0.0,7.0,nbank)
            stor(next+12)=nbank1
            tbank1=nbank1
            do 10 n=1,3
              temp=tbank1/2.0 - aint(tbank1/2.0)
              if (temp .gt. 0.0) then
                bank(n) = 1.0
              else
                bank(n) = 0.0
              end if
              tbank1 = aint(tbank1/2.0)
10          continue

c
c           detection of a.c. fault
c

            if (stor(next+5) .lt. fault) then
              stor(next+9)=0.0
              stor(next+10)=0.0
              stor(next+11)=0.0
              stor(next+19)=time+2.0*0.0167
              stor(next+20)=1.0
            else
              if (time .gt. stor(next+19)) then
                stor(next+9)=bank(1)
                stor(next+10)=bank(2)
                stor(next+11)=bank(3)
                stor(next+20)=0.0
              else
                stor(next+9)=0.0
                stor(next+10)=0.0
                stor(next+11)=0.0
                stor(next+20)=1.0
              end if
            end if

c
c  initialization
c

            if (time .lt. 0.05) then
               stor(next+9)=0.0
               stor(next+10)=0.0
               stor(next+11)=0.0
               stor(next+20)=1.0
```

```
            else
               stor(next+9)=bank(1)
               stor(next+10)=bank(2)
               stor(next+11)=bank(3)
               stor(next+20)=0.0
            end if
           else
            nexc=nexc+3
           end if

c          increment counter

           stor(next+3)=stor(next+3)+0.5
           count = stor(next+3)

           if (count .ge. 77.0 .and. count .le. 88.0) then
             stor(next+4) = stor(next+12)
           end if

         end if

         con(1)=stor(next+5)
         con(2)=stor(next+13)
         con(3)=stor(next+6)
         con(4)=stor(next+14)
         con(5)=stor(next+12)
         con(6)=stor(next+9)
         con(7)=stor(next+10)
         con(8)=stor(next+11)
         con(12)=stor(next+15)
         con(13)=stor(next+16)
         con(14)=stor(next+17)
         con(15)=stor(next+18)

         call thydio2(2,4,10,stor(next+9),5,count)
         call thydio2(2,5,11,stor(next+10),5,count)
         call thydio2(2,6,12,stor(next+11),5,count)

         ggin(n1,ms1)=ggin(n1,ms1)+var(1)
         ccin(n1,ms1)=ccin(n1,ms1)+cs(14,ms2)+vdc(n1,ms1)*ggin(n1,ms1)
         return
         end

      real function int3(yo,tlo,thi,t,del,flag,x)

c
c     ***************************************************************
c     Purpose: non-sticking saturating integral with limits
c     yo = output at time 0-, tlo,thi = low and high limits of output,
c     t = time constant with default = 1.0 secs, x = input
c     trapezoidal integration based on state variable method.
c     - modification to existing EMTDC subroutine: inclusion of 'del'
c       for modelling integration occurring once per cycle and not once
c       per time step
c     ***************************************************************
c

      real yo,tlo,thi,t,del,x,flag
      include 'EMT.E'
      common /s1/time,delt,ich
      common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
      common /s4/var(100),con(100),pgb(25)

c     set initial conditions

      if (time .le. del .or. flag .gt. 0.0) then
```

```
          stor(nexc+2)=yo
          stor(nexc+3)=0.5*del
          stor(nexc+1)=x*stor(nexc+3)
        end if
        at=t
        if (at.eq.0.0) at=1.0
        a1=x*stor(nexc+3)/at
        a2=stor(nexc+2)+a1+stor(nexc+1)
        stor(nexc+1)=a1
        ai1=a2
        if (a2.gt.thi) ai1=thi
        if (a2.lt.tlo) ai1=tlo
        int3=stor(nexc+2)
        stor(nexc+2)=ai1
        nexc=nexc+3
        return
        end

          subroutine thydio2(ms,nto,nfrom,puls,idk,timer)

c
c  ***************************************************************
c  Purpose:To model an anti-parallel
c          thyristor-diode switch
c  ***************************************************************
c

        real roff,ron,gnew,curr,rt,puls
        integer ms,nto,nfrom,idk
        include 'EMT.E'
        common /s1/time,delt,ich
        common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
        common /s4/var(100),con(100),pgb(25)

        ron = 0.001
        roff = 10000.0

        if (time .lt. delt) then
          stor(nexc + 1) = roff
          stor(nexc + 2) = 0.0
          gnew = 0.0002
        end if
        rt = stor(nexc + 1)
        curr = cdc(nto,nfrom,ms)
        g = gdc(nfrom,nto,ms)
c
c Determine if thyristor is on/off
c

        con(9)=timer
          if (abs(rt-roff) .lt. 1.0) then
c   thyristor is in off state
            if (timer .ge. 73.0 .and. timer .lt. 93.0) then
               if (puls .gt. 0.5) rt = ron
c   turn on thyristor
            end if
          else
c   thyristor in the on state
            if (curr .lt. 0.00 .and. puls .lt. 0.5) then
c   turn off thyristor
                     rt = roff
            end if
          end if
          stor(nexc + 1) = rt
          con(10)=stor(nexc+1)
c
```

```
c  use thyristor info to determine branch conductance
c

        if (time .ge. stor(nexc + 2)) then
          if (abs(rt - roff) .lt. 1.0) then
c  thyristor is in off state
            if (curr .lt. var(2)) then
c  diode is forward conducting
              if (g .le. 1.0) then
                 stor(nexc + 2) = time + idk * delt
                 gnew = 20.0
                 gdc(nto,nfrom,ms) = gnew
                 gdc(nfrom,nto,ms) = gnew
              end if
            else
c  diode is reverse biased
              if (g .gt. 1.0) then
                 stor(nexc + 2) = time + idk * delt
                 gnew = 0.0002
                 gdc(nto,nfrom,ms) = gnew
                 gdc(nfrom,nto,ms) = gnew
              end if
            end if
         else
c  thyristor is in the on state
           if (g .le. 1.0) then
              stor(nexc + 2) = time + idk * delt
              gnew = 20.0
              gdc(nto,nfrom,ms) = gnew
              gdc(nfrom,nto,ms) = gnew
           end if
          end if
        end if

        con(11)=gnew
        nexc = nexc + 2
        return
        end
```

```
tsc data /
0.000025 0.6 0.0005 /
2 / # of subsystems
12 / # of nodes in subsystem 1
0.0 /
12 10 0.0 0.0001592 /
10 11 0.0 0.0 1591.62 / 150 kvar capacitor
11 0 0.0167 /
10 9 0.0 0.0000981 /
9 0 200.0 / large Impedance to ground
9 8 0.068 /
8 7 0.0 0.0020196 / 197 kva load
7 6 0.001 / closed switch 2 (machine start)
6 0 1.0152 /
8 5 0.221 /
5 4 0.0 0.0001334 /
4 3 0.01 / closed switch 1 (flicker)
3 2 6.897 / 29 kva load
2 0 0.0 0.013721 /
3 1 4.445 / 45 kva load
1 0 0.0 0.008841 /
999 /
12 0.0001 /
999/ end of source data
999/ end transformer data
14 /
0.0 / caps initially charged
13 10 0.0 0.000464 / filter inductance 0.1750 pu
13 11 0.0 0.000232 /                   0.0875 pu
13 12 0.0 0.000116 /                   0.04375 pu
10 4 5000.0 / thyristor initially off
11 5 5000.0 /
12 6 5000.0 /
10 7 800.00 / snubber resistance (rs1)
11 8 400.00 /                    (rs2)
12 9 200.00 /                    (rs3)
7 4 0.0 0.0 0.50 / snubber capacitor  (.5 uf)
8 5 0.0 0.0 0.50 /
9 6 0.0 0.0 0.50 /
4 1 0.0 0.0 336.83 / 35 kvar capacitance
5 2 0.0 0.0 673.66 / 70 kvar capacitance
6 3 0.0 0.0 1347.32 / 140 kvar capacitance
1 0 0.39 / stabalizing resistance
2 0 0.25 /
3 0 0.18 /
999 /
14 0.0001 /
999/
2 / # mutually coupled windings
14 0         0.    0.2652583    /hv - side wndng
13 0         0.    0.2651256          0.    0.2652583    /lv - side wndng
999/ end tform data
999/
-5 5 /
10 /
0.001 -0.1e-4 3.00 250.0 0.1 0.15 0.2 0.25 0.3 0.35 10.0 0.0075  /
999/
```

```
      subroutine dsdyn
c
c ***********************************************************
c Purpose: Main dynamics subroutine which models a single
c          phase thyistor switched capacitor compensator
c          employing direct control
c
c Author: David Jacobson July 15,1990 University of Manitoba
c ***********************************************************
c
      real limit, intgl3,ldlag2,newtm,rnew
      real error
      include 'EMT.E'
      common /s1/time,delt,ich
      common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
      common /s4/var(100),con(100),pgb(25)

c
c -------------------------------
c Variable (1..100) Definitions: tscff.dyn
c -------------------------------
c
c       Var(1): subsystem interface conductance
c       Var(2): current level below which diode conducts
c       Var(3): not used
c       Var(4): not used
c       Var(5): time load (2) switched in
c       Var(6):  "              "       out
c       Var(7): time system voltage has fault
c       Var(8): time fault clears
c       Var(9): time load (1) switched in
c       Var(10): "              "       out
c       Var(11): leakage susceptance of transformer
c       Var(12): deadzone

      next=nexc
      nexc = nexc+2

c     define subsystem voltage

      if (time .gt. 0.0 ) vpeak=1.414214
        es(12,1) =vpeak*sin(6.2832*time*60.0)

c
c     ramp load up to 200 kva
c

c     if (time .gt. 0.05 .and. time .lt. 0.8) then
c      stor(next+1)=stor(next+1)+0.5
c      if(stor(next+1) .ge. 100) then
c       stor(next+1)=0.0
c       stor(next+2)=4.0*exp(-5.0*(time-0.05))
c       rnew=stor(next+2)
c       gdc(7,6,1)=1.0/rnew
c       gdc(6,7,1)=gdc(7,6,1)
c      end if
c     end if

c
c     switch 1 off/on for 5 cycles (flicker)
c

      call prll2(var(5),1,3,4,10000000,1,1)
      call prll2(var(6),1,3,4,1,10000000,0)
```

```
c
c       fault
c

c       call prll2(var(7),1,9,0,1.0,20000.0,0)
c       call prll2(var(8),1,9,0,20000.0,1.0,1)

c
c       define compensator
c

        call stsc32(1,8,2,1.00,0.000,var(12),0.7,var(11))

        return
        end


        subroutine stsc32(ms1,n1,ms2,vref,droop,dedzone,fault,bd)
c
c ****************************************************************
c Purpose: To model three banks of single phase thyristor switched
c          capacitors.
c ****************************************************************
c

        real limit, intgl3,int3,ldlag2,bank(3),nbank,nbank1,i2rms
        real vref,droop,dedzone,kp,ki,fault,bd,flag
        real nbankt1,dbnk,dbnkpi,dbnkff,nbankt,vsvsold,nbnkold,error
        real error,e1,e2,rlp2
        include 'EMT.E'
        common /s1/time,delt,ich
        common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
        common /s4/var(100),con(100),pgb(25)
c
c ----------------
c Input Arguments:
c ----------------
c
c       ms1: subsystem containing distribution network
c       n1: node which is to be compensated
c       ms2: subsystem containing compensator
c       vref: reference voltage p.u.
c       droop: compensator droop(.01-.05) p.u.
c       dedzone: compensator deadzone where no switching ocurrs
c       fault: voltage level when if detected will turn off compensator
c              for 2 cycles after recovery
c       bd: leakage susceptance of transformer in per unit
c
c -----------------------
c Con(1.100) Definitions:
c -----------------------
c
c       con(1): v2rms
c       con(2): modified Vref; for out reg. range flicker comp.
c       con(3): Vsvs(rms)
c       con(4): i2rms
c       con(5): #banks desired
c       con(6): bank1 indicator
c       con(7): bank2 ind.
c       con(8): bank3 ind.
c       con(9): timer for thyristor firing
c       con(10): thyristor3 resistance
c       con(11): thydio 3 branch conductance
c       con(12): delta Vsvs
c       con(13): susceptance of capacitor banks
```

```
c       con(14): not used
c       con(15): not used
c       con(16): # of banks (actual)
c       con(17): change in # of banks (desired)
c       con(18): error (voltage)
c       con(19): e1 (out of range)
c       con(20): flag (fault indication)
c       con(21): e1 after limiting

c
c --------------
c Program begins
c --------------
c

        next=nexc
        nexc = nexc+26

        if (time .le. delt) then
         ggin(n1,ms1) = ggin(n1,ms1) + var(1)
         stor(next+23)=0.05
         stor(next+8)=vref
        end if

c       interface two subsystems togethor

        es(14,ms2)=vdc(n1,ms1)

c       measure secondary voltage

        v1=vdc(13,ms2)

c       convert to square wave for timing

        if (v1 .ge. 0.0 .or. stor(next+7) .ge. 0.0) then
            if (stor(next+2) .ge. 336.0) then
              stor(next+7)=-1.0
            else
              stor(next+7)=1.0
              stor(next+3)=0.0
            end if
        else
            if (stor(next+3) .ge. 168.0) then
              stor(next+7)=1.0
            else
              stor(next+7)=-1.0
            end if
        end if


c
c positive half of cycle
c

        if (stor(next+7) .ge. 0.0) then
          nexc=nexc+2
          stor(next+3)=0.0

c        rms meter

          v2=v1*v1
          stor(next+1)=stor(next+1)+v2*delt
          stor(next+2) = stor(next+2) + 1.0
          count = 200.0

        end if
```

```
c
c       negative half of cycle
c

        if (stor(next+7) .le. 0.0) then

c         calculate rms voltage

         if (stor(next+3) .eq. 20.0 .and. stor(next+2) .gt. 328.) then
          stor(next+1) = sqrt(stor(next+1)/((stor(next+2)+1)*delt))
          v2rms=stor(next+1)
          stor(next+5)=stor(next+1)
          stor(next+1)=0.0
         end if


c
c         control data
c

         if (stor(next+3) .eq. 40.0 .and. stor(next+2) .gt. 328.) then
          stor(next+2)=0.0
          bc=stor(next+21)*0.12987
          stor(next+16)=bc
          vsvs=stor(next+5)-stor(next+5)*abs(bc/bd)
          stor(next+6)=vsvs
          i2rms=bc*stor(next+5)
          stor(next+14)=i2rms
          deltv=stor(next+8)-(i2rms*droop+vsvs)
          stor(next+15)=deltv
          flag=stor(next+20)
          if (stor(next+5) .le. fault) then
             deltv=0.0
             flag=1.0
          end if
          if (time .le. stor(next+19)) then
             deltv=0.0
             flag=1.0
          end if
          if (abs(deltv) .le. dedzone) deltv=0.0


c
c         determine number of cap banks to be on
c

c         Direct Calculation of # of banks

          if (time .gt. stor(next+23)) then
            dbnkff=aint(deltv*100.0)
            dummy=deltv*100-aint(deltv*100)
            if (dummy .ge. 0.5) dbnkff=dbnkff+1.0
            stor(next+24)=dbnkff

            nbnkold=stor(next+21)
            if (flag .gt. 0.5) nbnkold=0.0
            nbankt=nbnkold+dbnkff
            stor(next+12)=nbankt

            nbankt1=limit(0.0,7.0,nbankt)
            dbnk=nbankt1-nbnkold

            if (dbnk .ge. 1.0) then
              stor(next+23)=time+2.0*0.0166667
            end if
```

```
          stor(next+21)=nbankt1
        end if

c       modify Vref if flicker occurring out of reg. range

        nbankt=stor(next+12)
        if (nbankt .gt. 7.0) then
          error=nbankt-7.0
        else
          if (nbankt .lt. 0.0) then
            error=nbankt
          else
            error=0.0
          end if
        end if

        if (time .le. 0.05) error=0.0
        if (stor(next+5) .le. fault) error=0.0

        stor(next+13)=error
        e1=rlp2(0.04,1.0,0.01667,stor(next+13))
        stor(next+17)=e1
        e2=limit(-0.1,0.1,e1)
        stor(next+26)=e2
        vrefn=vref-e2*2.0
        stor(next+8)=vrefn

c       save old value of Vsvs

        stor(next+22)=vsvs

c
c       Convert number of banks to binary
c

        tbank1=stor(next+21)
        do 10 n=1,3
          temp=tbank1/2.0 - aint(tbank1/2.0)
          if (temp .gt. 0.0) then
            bank(n) = 1.0
          else
            bank(n) = 0.0
          end if
          tbank1 = aint(tbank1/2.0)
10      continue

c
c       detection of a.c. fault
c

        if (stor(next+5) .lt. fault) then
          stor(next+9)=0.0
          stor(next+10)=0.0
          stor(next+11)=0.0
          stor(next+19)=time+2.0*0.0167
          stor(next+20)=1.0
        else
          if (time .gt. stor(next+19)) then
            stor(next+9)=bank(1)
            stor(next+10)=bank(2)
            stor(next+11)=bank(3)
            stor(next+20)=0.0
          else
            stor(next+9)=0.0
            stor(next+10)=0.0
```

```
                stor(next+11)=0.0
                stor(next+20)=1.0
              end if
            end if

c
c  initialization
c

            if (time .lt. 0.05) then
               stor(next+9)=0.0
               stor(next+10)=0.0
               stor(next+11)=0.0
               stor(next+20)=1.0
            else
               stor(next+9)=bank(1)
               stor(next+10)=bank(2)
               stor(next+11)=bank(3)
               stor(next+20)=0.0
            end if
           else
            nexc=nexc+2
           end if

c          increment counter

           stor(next+3)=stor(next+3)+0.5
           count = stor(next+3)

           if (count .ge. 77.0 .and. count .le. 88.0) then
             stor(next+4) = stor(next+21)
           end if

         end if

         con(1)=stor(next+5)
         con(2)=stor(next+8)
         con(3)=stor(next+6)
         con(4)=stor(next+14)
         con(5)=stor(next+12)
         con(6)=stor(next+9)
         con(7)=stor(next+10)
         con(8)=stor(next+11)
         con(12)=stor(next+15)
         con(13)=stor(next+16)
         con(16)=stor(next+21)
         con(17)=stor(next+24)
         con(18)=stor(next+13)
         con(19)=stor(next+17)
         con(20)=stor(next+20)
         con(21)=stor(next+26)



         call thydio2(2,4,10,stor(next+9),10,count)
         call thydio2(2,5,11,stor(next+10),10,count)
         call thydio2(2,6,12,stor(next+11),10,count)

         ggin(n1,ms1)=ggin(n1,ms1)+var(1)
         ccin(n1,ms1)=ccin(n1,ms1)+cs(14,ms2)+vdc(n1,ms1)*ggin(n1,ms1)
         return
         end

         subroutine thydio2(ms,nto,nfrom,puls,idk,timer)
```

```
c ************************************************************
c Purpose: To model an anti-parallel
c          thyristor-diode switch
c ************************************************************
c

        real roff,ron,gnew,curr,rt,puls
        integer ms,nto,nfrom,idk
        include 'EMT.E'
        common /s1/time,delt,ich
        common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
        common /s4/var(100),con(100),pgb(25)

        ron = 0.001
        roff = 10000.0

        if (time .lt. delt) then
          stor(nexc + 1) = roff
          stor(nexc + 2) = 0.0
          gnew = 0.0002
        end if
        rt = stor(nexc + 1)
        curr = cdc(nto,nfrom,ms)
        g = gdc(nfrom,nto,ms)
c
c Determine if thyristor is on/off
c

        con(9)=timer
          if (abs(rt-roff) .lt. 1.0) then
c   thyristor is in off state
            if (timer .ge. 73.0 .and. timer .lt. 93.0) then
               if (puls .gt. 0.5) rt = ron
c   turn on thyristor
            end if
          else
c   thyristor in the on state
            if (curr .lt. 0.00 .and. puls .lt. 0.5) then
c   turn off thyristor
                      rt = roff
            end if
          end if
          stor(nexc + 1) = rt
          con(10)=stor(nexc+1)
c
c  use thyristor info to determine branch conductance
c

        if (time .ge. stor(nexc + 2)) then
          if (abs(rt - roff) .lt. 1.0) then
c  thyristor is in off state
            if (curr .lt. var(2)) then
c  diode is forward conducting
              if (g .le. 1.0) then
                 stor(nexc + 2) = time + idk * delt
                 gnew = 20.0
                 gdc(nto,nfrom,ms) = gnew
                 gdc(nfrom,nto,ms) = gnew
              end if
            else
c  diode is reverse biased
              if (g .gt. 1.0) then
                 stor(nexc + 2) = time + idk * delt
                 gnew = 0.0002
                 gdc(nto,nfrom,ms) = gnew
                 gdc(nfrom,nto,ms) = gnew
```

```
              end if
            end if
          else
c  thyristor is in the on state
           if (g .le. 1.0) then
              stor(nexc + 2) = time + idk * delt
              gnew = 20.0
              gdc(nto,nfrom,ms) = gnew
              gdc(nfrom,nto,ms) = gnew
           end if
          end if
         end if

         con(11)=gnew
         nexc = nexc + 2
         return
         end

      FUNCTION RLP2(G,T,DEL,X)
C
C *********************************************************************
C Purpose: To model a first order lag control function block
C
C G = GAIN,  T = TIME CONST, X = INPUT.  0- OUTPUT = G*X
C    NOTE:  G AND T CAN BE CHANGED DURING THE SOLUTION
C
C           DEL included to model calling function once per
C               cycle rather than once per time step
C *********************************************************************
C
      REAL A1,A2,A3,A5
      REAL DELT,DEL
      REAL G
      INTEGER ICH
      INTEGER NEXC
      REAL REALP2
      REAL STOR
      REAL T,TIME
      REAL X
      INCLUDE 'EMT.E'
      COMMON /S1/TIME,DELT,ICH
      COMMON /S2/STOR(5000),NEXC

      IF (TIME.GE.DEL) GO TO 10
      STOR(NEXC+2)=X*G
      STOR(NEXC+1)=0.0
   10 CONTINUE
      IF (T.NE.0.0) GO TO 15
      REALP2=X*G
      GO TO 20
   15 A3=0.5*DEL/T
      A1=X*G
      A5=A3*( A1+STOR(NEXC+1) )
      A2=STOR(NEXC+2) + A5
      A2=A2 / ( 1.0 + A3 )
      STOR(NEXC+1)=A1-A2
      RLP2=STOR(NEXC+2)
      STOR(NEXC+2)=A2
   20 NEXC=NEXC+2
      RETURN
      END
```

```
tscff data /
0.000025 0.45 0.0003 /
2 / # of subsystems
13 / # of nodes in subsystem 1
0.0 /
12 10 0.0 0.0001592 /
10 11 0.0 0.0 1591.62 / 150 kvar capacitor
11 0 0.0167 /
10 13 0.0 0.0000981 /
13 9 0.034 /
9 0 100.0 / large Impedance to ground
9 8 0.034 /
8 7 0.0 0.0020196 / 197 kva load
7 6 0.001 / closed switch 2 (machine start)
6 0 1.0152 /
8 5 0.221 /
5 4 0.0 0.0001334 /
4 3 200.0 / closed switch 1 (flicker)
3 2 6.897 / 29 kva load
2 0 0.0 0.013721 /
3 1 4.445 / 45 kva load
1 0 0.0 0.008841 /
999 /
12 0.0001 /
999/ end of source data
999/ end transformer data
14 /
0.0 / caps initially charged
13 10 0.0 0.000464 / filter inductance 0.1750 pu
13 11 0.0 0.000232 /                   0.0875 pu
13 12 0.0 0.000116 /                   0.04375 pu
10 4 5000.0 / thyristor initially off
11 5 5000.0 /
12 6 5000.0 /
10 7 800.00 / snubber resistance (rs1)
11 8 400.00 /                    (rs2)
12 9 200.00 /                    (rs3)
7 4 0.0 0.0 0.50 / snubber capacitor  (.5 uf)
8 5 0.0 0.0 0.50 /
9 6 0.0 0.0 0.50 /
4 1 0.0 0.0 336.83 / 35 kvar capacitance
5 2 0.0 0.0 673.66 / 70 kvar capacitance
6 3 0.0 0.0 1347.32 / 140 kvar capacitance
1 0 0.39 / stabalizing resistance
2 0 0.25 /
3 0 0.18 /
999 /
14 0.0001 /
999/
2 / # mutually coupled windings
14 0         0.    0.2652583    /hv - side wndng
13 0         0.    0.2651256          0.    0.2652583    /lv - side wndng
999/ end tform data
999/
-5 5 /
10 /
0.001 -0.1e-4 3.00 250.0 0.1335 0.306 0.2 0.25 0.3 0.35 10.0 0.0075  /
999/
```

```
      subroutine dsout
      real limit,intgl3,ldlag2
      include 'EMT.E'
      common /s1/time,delt,ich
      common /s2/stor(5000),nexc/s3/gvlv(4,4,24),nvlv
      common /s4/var(100),con(100),pgb(25)
c
      pgb(1)=0.0-cs(14,2)
      pgb(2)=vdc(8,1)
      pgb(3)=cdc(9,8,1)
      pgb(4)=con(3)
      pgb(5)=con(21)
      pgb(6)=con(13)
      pgb(7)=cdc(13,9,1)
      pgb(8)=vdc(4,2)-vdc(1,2)
      pgb(9)=vdc(6,2)-vdc(3,2)
      pgb(10)=con(2)

      return
      end
```

```
      SUBROUTINE DRIVER
C-----------------------------------------------
C  DECLARATIONS
C
C        - THE FOLLOWING NUMBERS ARE GIVEN IN DRIVER
C            FOR INFORMATION ONLY.
C        - IF YOU CHANGE ONE IN DRIVER
C            THE PROGRAM WILL NEVER SEE THE CHANGE.
C        --------------------------
C
       DOUBLE PRECISION TIME,TMDT,DELT(4)
       DOUBLE PRECISION TM2D
       DOUBLE PRECISION DELTC,DELTS
       DOUBLE PRECISION CBRMDT(500),PTMDT(500),VCPMDT(500),
      &             VXNMDT(300)
       DOUBLE PRECISION CBRM2D(500),PTM2D(500),VCPM2D(500),
      &             VXNM2D(300)
       DOUBLE PRECISION STRM2D(3000)
       INTEGER NSTPSZ
       INTEGER NSWM2D(500)
       INTEGER NFR(500),NTO(500)
       INTEGER INITPS
       INTEGER INITZC
       INTEGER NBLKRS
       DOUBLE PRECISION CBTMDT(30,6)
       DOUBLE PRECISION CBTM2D(30,6)
       DOUBLE PRECISION TMGMDT(30)
       DOUBLE PRECISION TMGM2D(30)
       INTEGER ITER
       DOUBLE PRECISION CTPMDT(2,6,8),CTPM2D(2,6,8)
C
C        - THE FOLLOWING NUMBERS CAN BE CHANGED IN
C            DRIVER AND THE PROGRAM WILL SEE THE CHANGE.
C        --------------------------
C
       DOUBLE PRECISION PT(500),CINJXN(300)
       INTEGER NXT
       DOUBLE PRECISION STRT(3000),STRMDT(3000)
       INTEGER NSWMDT(500)
       INTEGER NRJLRG
       INTEGER NCHNL1,NCHNL2,NCHNL3,NCHNL4
       REAL CHANL1(10),CHANL2(10),CHANL3(10),CHANL4(10)
       INTEGER NXTFIX
       DOUBLE PRECISION STRFIX(3000)
C
C-------------------------------------------------------------
C  THE FOLLOWING ARE VARIABLES WHICH ARE LOCAL TO DRIVER.
C
       DOUBLE PRECISION TCHUP,TCHDN,TSTATZ(4),VS
       INTEGER IWAVE,INOJIT,MODEF,NSTAT(4),IFIRE
C
       INTEGER IFRTMP,INTRST,NMODCH
       DOUBLE PRECISION VRMSMS,VERR,TDELAY,TNWUP,TSET
       DOUBLE PRECISION V2,TINT,YMNLM8,YMXLM8,YINIT
       DOUBLE PRECISION TDIFF,XOUT,VREF
       INTEGER MODE
       INTEGER NBRKR1,NBRKR2
       DOUBLE PRECISION TBRKR1,TBRKR2,RVARLD,RLAST
       INTEGER NDUM9
       DOUBLE PRECISION CLIM,VCAP
       INTEGER NBRKR3
C-------------------------------------------------------------
       COMMON /XGB130/ TIME,TMDT,DELT,TM2D,DELTC,DELTS,
      &  CBRMDT,PTMDT,VCPMDT,VXNMDT,CBRM2D,PTM2D,VCPM2D,VXNM2D
       COMMON /XGB135/  STRM2D,NSTPSZ,NSWM2D,NFR,NTO,INITPS,INITZC,
      &  NBLKRS,CBTMDT,CBTM2D,TMGMDT,TMGM2D
```

```
      COMMON /XGB141/ ITER
      COMMON /XGB226/ CTPMDT,CTPM2D
C---------------------------------
      COMMON /GBL015/ PT,CINJXN
      COMMON /GBL032/ NXT,STRT,STRMDT
      COMMON /XGB081/ NSWMDT
      COMMON /XGB111/ NRJLRG
      COMMON /GBL023/ NCHNL1,NCHNL2,CHANL1,CHANL2
      COMMON /GBL23X/ NCHNL3,NCHNL4,CHANL3,CHANL4
      COMMON /GBL32A/ NXTFIX,STRFIX
C---------------------------------
      SAVE /XGB130/
      SAVE /XGB135/
      SAVE /XGB141/
      SAVE /XGB226/
      SAVE /GBL015/
      SAVE /GBL032/
      SAVE /XGB081/
      SAVE /XGB111/
      SAVE /GBL023/
      SAVE /GBL23X/
      SAVE /GBL32A/
C*****************************************************************
C  USER AREA
C---------------------------------
C  SOURCE
C
      PT(9) = 10182.34*DCOS(376.991*TIME)
C---------------------------------
C  NOTE:- FOR EVERYTHING EXCEPT INDEPENDANT
C    SOURCES USE TMDT AS YOU WOULD USE TIME IN EMTDC.
C---------------------------------
C  SET REFERENCE VOLTAGE
C
      VREF = 7200.0
C-------------------------------------
C  PROVIDE 3 CYCLES TO CHARGE THE CAP
C  ( AND ASSURE A LOCK ONTO IWAVE ).
C
C    NOTE: FIRING MODE:-   MODE = 1
C          BLOCKED MODE:-  MODE = 0
C
      IF(TMDT.GT.0.05)THEN
        MODE = 1
      ELSE
        MODE = 0
      END IF
C-------------------------------------
C  ARRANGE TO CLOSE BREAKERS
C
      TBRKR1 = -1.0
      IF(TMDT.GT.TBRKR1)THEN
        NBRKR1 = 1
      ELSE
        NBRKR1 = 0
      END IF
C---
      TBRKR2 = 0.15
      IF(TMDT.LT.TBRKR2)THEN
        NBRKR2 = 1
      ELSE IF(TMDT.LT.0.35)THEN
        NBRKR2 = 1
      ELSE
        NBRKR2 = 1
      END IF
C---
```

```
C       IF(TMDT.LT.0.15)THEN
         NBRKR3 = 0
C       ELSE IF(TMDT.LT.0.25)THEN
C         NBRKR3 = 1
C       ELSE
C         NBRKR3 = 0
C       END IF
C
C-----------------------------------
C  ARRANGE TO VARY RESISTANCE FOR
C     THE VARIABLE LOAD AS A FUNCTION OF TIME. USE TMDT AS
C     YOU WOULD TIME IN EMTDC.
C
       IF(TMDT.LT.0.075)THEN
          RVARLD =  1000.0
       ELSE
          RVARLD = 1000.0*DEXP(-5.0*(TMDT-0.075))
       END IF
C*****************************************************************
C  TURN ON DIODE CHARACTERISTICS
C
       NSWMDT(5) = 1
       NSWMDT(6) = 1
       NSWMDT(7) = 1
       NSWMDT(8) = 1
C       NSWMDT(21) = 1
C---------------------------------
C  BRING FORTH THE LAST RESISTANCE USED FOR
C     THE VARIABLE LOAD
C
       IF(INITZC.EQ.1)THEN
         RLAST = 1000.0
       ELSE
         RLAST = STRM2D(NXT+16)
       END IF
C---------------------------------
C  KEEP REQUESTED RVARLD WITHIN BOUNDS.
C
       IF(RVARLD.LT.5.0)     RVARLD = 5.0
       IF(RVARLD.GT.1000.0) RVARLD = 1000.0
C---------------------------------
C  CHANGE THE BRANCH RESISTANCE IF IT
C     IS SIGNIFICANTLY DIFFERENT FROM
C     THAT ORDERED.
C
       IF(RVARLD.GT.RLAST*1.1 .OR.
      &    RVARLD.LT.RLAST*0.9)THEN
          NDUM9 = 20
          CALL CHANGR(NDUM9,RVARLD)
          RLAST = RVARLD
       END IF
C
       STRMDT(NXT+16) = RLAST
C---------------------------------
C  BREAKER CALLS
C     INPUT IS BRANCH NUMBER AND
C           A 1 FOR CLOSED CONTACTS AND
C           A 0 FOR OPEN   CONTACTS.
C                CLEARS ON CURRENT ZERO.
C
       NDUM9 = 15
       CALL BREAKR(NDUM9,NBRKR1)
C
       NDUM9 = 18
       CALL BREAKR(NDUM9,NBRKR2)
C
```

```
      NDUM9 = 22
      CALL BREAKR(NDUM9,NBRKR3)
C---------------------------------
C  SET UP A FEW INITIAL CONDITIONS
C   OR BRING IN PRIOR VALUES FROM MEMORY.
C
      IF(INITZC.EQ.1)THEN
        TCHUP = -100.0
        TCHDN = -100.0
        TSTATZ(1) = 0.0
        TSTATZ(2) = 0.0
        TSTATZ(3) = 0.0
        TSTATZ(4) = 0.0
        INOJIT = 0
        MODEF = 0
        VRMSMS = VREF
        VERR = 0.0
        TDELAY = -1.0E-5
        TNWUP = 0.0
        TSET = -100.0
      ELSE
        TCHUP = STRM2D(NXT+1)
        TCHDN = STRM2D(NXT+2)
        TSTATZ(1) = STRM2D(NXT+3)
        TSTATZ(2) = STRM2D(NXT+4)
        TSTATZ(3) = STRM2D(NXT+5)
        TSTATZ(4) = STRM2D(NXT+6)
        INOJIT = IDNINT(STRM2D(NXT+7))
        MODEF = IDNINT(STRM2D(NXT+8))
        VRMSMS = STRM2D(NXT+9)
        VERR = STRM2D(NXT+10)
        TDELAY = STRM2D(NXT+11)
        TNWUP = STRM2D(NXT+12)
        TSET  =  STRM2D(NXT+13)
      END IF
C---------------------------------
C  LOOK AT THE LINE VOLTAGE AND CREATE AN INDICATOR
C   WAVE WHICH MAY HAVE NOISE AT THE ZERO CROSSINGS.
C
      VS = VXNMDT(1)
C
      IF(VS.GT.0.0)THEN
        IWAVE = 1
      ELSE
        IWAVE = -1
      END IF
C---------------------------------
C  TAKE OUT POSSIBLE JITTER AT ZERO CROSSINGS
C   AND MAKE AN INDICATOR WAVE WITH NO JITTER.
C    NOTE: CHANGE IS ALLOWED 0.375 CYCLES AFTER
C          PRIOR CHANGE.
C
C SET UP A MARKER FOR RESETTING THE INTEGRATOR.
      INTRST = 0
C
      IF(IWAVE.GT.0 .AND.
     &   (TMDT-TCHDN).GT.0.0066)THEN
C
        IF(INOJIT.LT.1)THEN
          INOJIT = 1
          TCHUP = TMDT
C RESET THE INTEGRATOR IN THE TIME-STEP THAT THE
C  INOJIT WAVE GOES POSITIVE.
          INTRST = 1
        END IF
C
```

```
      ELSE IF(IWAVE.LT.0 .AND.
     &    (TMDT-TCHUP).GT.0.0066)THEN
C
        IF(INOJIT.GT. -1 )THEN
          INOJIT = -1
          TCHDN = TMDT
        END IF
C
      END IF
C
C SQUARE THE VOLTAGE WHEN INOJIT EQUALS 1
C   FOR INPUT TO THE INTEGRATOR.
      IF(INOJIT.EQ.1)THEN
        V2 = VS*VS
      ELSE
        V2 = 0.0
      END IF
C
C  INTEGRATOR WILL INTEGRATE SQUARED
C   POSITIVE HALF WAVE.
      TINT = 1.0
      YMNLM8 = -1.0E20
      YMXLM8 =  1.0E20
      YINIT = 0.0
C
      NXT = NXT + 13
C
      CALL XINT2(V2,
     &           TINT,
     &           YMNLM8,YMXLM8,
     &           YINIT,INTRST,
     &           XOUT)
C
      NXT = NXT - 15
C
C  PREPARE A MARKER FOR WHEN THE BRIDGE CAN BE
C   BLOCKED OR DEBLOCKED.
      NMODCH = 0
C
C  SET CERTAIN NUMBERS AT 270 DEGREES IN THE SIN WAVE.
      IF((TMDT-TCHDN).GT.0.00405 .AND.
     &    (TMDT-TCHDN).LT.0.00420)THEN
C
        NMODCH = 1
C
        TDIFF = TCHDN - TCHUP
        IF(TDIFF.LT.0.0042) TDIFF = 0.0042
C
        VRMSMS = DSQRT(XOUT/TDIFF)
C
        VERR = VREF - VRMSMS
        IF(ABS(VERR).LT.36.0) VERR = 0.0
        IF(VERR.GT. 288.0) VERR = 288.0
        IF(VERR.LT.-288.0) VERR = -288.0
C
C        TDELAY = 0.643E-6*VERR - 1.0E-5
        TDELAY = 1.608E-6*VERR - 1.0E-5
        VCAP = VXNMDT(4) - VXNMDT(5)
        IF(VCAP.GT.1000.0 .AND. TDELAY.GT.0.0)
     &       TDELAY = 0.0
        IF(VCAP.LT.333.0 .AND. TDELAY.LT.0.0)
     &       TDELAY = 0.0
        CLIM = VCAP*0.001501 - VRMSMS/7200.0
        IF(CLIM.GT.0.5 .AND. TDELAY.GT.0.0)
     &       TDELAY = 0.0
        IF(CLIM.LT.-0.5 .AND. TDELAY.LT.0.0)
```

```
     &        TDELAY = 0.0
         TNWUP = TCHDN + 8.33333333D-3 + TDELAY
         TSET = TMDT
C
       END IF
C
       IF(TSET.LT.-1.0)THEN
         IFRTMP = 0
       ELSE
         IFRTMP = 1
         IF(TMDT.LT.TNWUP) IFRTMP = -1
         IF(TCHUP.GT.TSET .AND.
     &      TMDT.GT.(TCHUP + 8.3333333D-3 + TDELAY))THEN
           IFRTMP = -1
         END IF
       END IF
C
C-----------------------------------
C  FIRE FROM THE SHIFTED WAVEFORM.
C
       IFIRE = IFRTMP
C
C      IFIRE = INOJIT
C-----------------------------------
C  DEBLOCK ONLY WHEN PERMITTED AT 90
C   AND 270 DEGREES.
C
C    NOTE: FIRING MODE:-   MODEF = 1
C          BLOCKED MODE:-  MODEF = 0
C
       IF(NMODCH.EQ.1) MODEF = MODE
       IF(MODE.EQ.0)   MODEF = 0
C-----------------------------------
C  DECIDE DESIRED STATES ACCORDING TO MODE OF FIRING
C   AND THE FIRING INDICATOR WAVE.
C
       IF(MODEF.EQ.0)THEN
         NSTAT(1) = 0
         NSTAT(2) = 0
         NSTAT(3) = 0
         NSTAT(4) = 0
         TSTATZ(1) = TMDT
         TSTATZ(2) = TMDT
         TSTATZ(3) = TMDT
         TSTATZ(4) = TMDT
       ELSE IF(IFIRE.EQ.1)THEN
         NSTAT(1) = 1
         NSTAT(2) = 0
         NSTAT(3) = 1
         NSTAT(4) = 0
         TSTATZ(2) = TMDT
         TSTATZ(4) = TMDT
       ELSE
         NSTAT(1) = 0
         NSTAT(2) = 1
         NSTAT(3) = 0
         NSTAT(4) = 1
         TSTATZ(1) = TMDT
         TSTATZ(3) = TMDT
       END IF
C--------------------------------------
C  ALWAYS DELAY TURN-ON BY 15 MICROSECONDS TO
C   ALLOW FOR THE SHORTER TURN-ON TIME
C   AS COMPARED TO TURN-OFF TIME.
C
       IF(NSTAT(1).EQ.1 .AND.
```

```
     &    (TMDT-TSTATZ(1)).GT.1.5E-5)THEN
            NSWMDT(1) = 1
          ELSE
            NSWMDT(1) = 0
          END IF
C
          IF(NSTAT(2).EQ.1 .AND.
     &    (TMDT-TSTATZ(2)).GT.1.5E-5)THEN
            NSWMDT(2) = 1
          ELSE
            NSWMDT(2) = 0
          END IF
C
          IF(NSTAT(3).EQ.1 .AND.
     &    (TMDT-TSTATZ(3)).GT.1.5E-5)THEN
            NSWMDT(3) = 1
          ELSE
            NSWMDT(3) = 0
          END IF
C
          IF(NSTAT(4).EQ.1 .AND.
     &    (TMDT-TSTATZ(4)).GT.1.5E-5)THEN
            NSWMDT(4) = 1
          ELSE
            NSWMDT(4) = 0
          END IF
C---------------------------------
C  STORE INFO IN MEMORY FOR NEXT PASS
C
          STRMDT(NXT+1)  = TCHUP
          STRMDT(NXT+2)  = TCHDN
          STRMDT(NXT+3)  = TSTATZ(1)
          STRMDT(NXT+4)  = TSTATZ(2)
          STRMDT(NXT+5)  = TSTATZ(3)
          STRMDT(NXT+6)  = TSTATZ(4)
          STRMDT(NXT+7)  = DBLE(INOJIT)
          STRMDT(NXT+8)  = DBLE(MODEF)
          STRMDT(NXT+9)  = VRMSMS
          STRMDT(NXT+10) = VERR
          STRMDT(NXT+11) = TDELAY
          STRMDT(NXT+12) = TNWUP
          STRMDT(NXT+13) = TSET
C---------------------------------
C  ADJUST STORAGE BASE
C
          NXT = NXT + 16
C-------------------------------------------------
C  PRINTER OUTPUT
C-----
C NUMBER OF CHANNELS
          NCHNL1 = 10
C
C TMDT
          CHANL1(1) = TMDT
C
          CHANL1(2) = VXNMDT(1)/7200.
          CHANL1(3) = VXNMDT(2)/600.
          CHANL1(4) = VXNMDT(3)/600.
          CHANL1(5) = VXNMDT(4)/666.0
          CHANL1(6) = VXNMDT(5)/666.0
          CHANL1(7) = (VXNMDT(4)-VXNMDT(5))/666.0
          CHANL1(8) = CBRMDT(10)/416.64
          CHANL1(9) = -CBRMDT(11)/416.64
          CHANL1(10) = REAL(INOJIT)
C-----
C NUMBER OF CHANNELS
```

```
      NCHNL2 = 10
C
C TMDT
      CHANL2(1) = TMDT
C
      CHANL2(2)   = VRMSMS/7200.
      CHANL2(3)   = VERR/7200.
      CHANL2(4)   = TDELAY
      CHANL2(5)   = CBTMDT(1,1)/34.72
      CHANL2(6)   = ( CBRMDT(23) + CBRMDT(24) +
     & CBRMDT(25) + CBRMDT(26) + CBRMDT(27))/34.72
      CHANL2(7)   = REAL(IFRTMP)
      CHANL2(8)   = CBTMDT(1,2)/416.64
      CHANL2(9)   = -CBRMDT(10)/416.64
      CHANL2(10)  = CHANL2(5) + CHANL2(6)
C-----
      NCHNL3 = 0
      NCHNL4 = 0
C-------------------------------------------------------------
      RETURN
       END
```

```
0.0 0.7 1.5E-6 30 1 / BGNTIM FINTIM DTSMAL NSUBST NSTPSI
2 / NUMBER OF OUTPUT FILES
0.0 0.7 0.5E-3 /
OUT1
0.0 0.7 0.5E-3 /
OUT2
9999 / END OF PRINTER DATA
9999 / END OF INITIAL NODE VOLTAGE DATA
9999 / END OF BRANCH IC DATA
9999 / END OF ALT BRC DATA
```

```
TEST52
11 /
4  3  1 1.0E6 0.0 0.0 3 / VALVE 1
3  5  1 1.0E6 0.0 0.0 3 / VALVE 2
0  5  1 1.0E6 0.0 0.0 3 / VALVE 3
4  0  1 1.0E6 0.0 0.0 3 / VALVE 4
3  4  1 1.0E6 0.0 0.0 3 / DIODE 1
5  3  1 1.0E6 0.0 0.0 3 / DIODE 2
5  0  1 1.0E6 0.0 0.0 3 / DIODE 3
0  4  1 1.0E6 0.0 0.0 3 / DIODE 4
0  6  1 0.0 0.033  / SOURCE    - BR 9
2  3  1 0.0 3.4E-3 / INDUCTOR
4  5  1 0.0 0.0 4.4E-3 / CAPACITIOR
6  0  1 0.0 0.0 7.674E-6 / CAP AT SOURCE
6  11 1 14.1 / LINE FROM SOURCE TO SVS
1  7  1 45.91  0.02765 /  LINE TO BREAKER 1
7  8  1 1.0E6 0.0 0.0 4 / BREAKER 1   - BR 15
8  0  1 1430.0 2.845 / SMALL LOAD OFF BREAKER 1
8  0  1 921.616 1.833 / LARGER LOAD OFF BREAKER 1
1  9  1 1.0E6 0.0 0.0 4 / BREAKER 2   - BR 18
9 10  1 210.49  0.41875 / FIRST BRANCH OFF BRKR 2
10 0  1 1000.0 / VARIABLE RESISTANCE OFF BREAKER 2  - BR 20
11 1  1 0.0 0.0205 / LINE FROM SOURCE TO SVS
11 0  1 1.0E6 0.0 0.0 4 / BREAKER 3   - BR 22
1  0  1 0.0 0.6879 1.136E-6 / FILTER N=3
1  0  1 0.0 0.2293 1.227E-6 / FILTER N=5
1  0  1 0.0 0.1146 1.253E-6 / FILTER N=7
1  0  1 0.0 0.0688 1.263E-6 / FILTER N=9
1  0  1 0.0 0.0459 1.268E-6 / FILTER N=11
9999 / END OF BRANCH DATA
1 / ONE TRANSFORMER IND MAT
2 0.0833333 / 2 WINDING, RATIO 2:1
1 55.27898 /
2 4.5836638 0.38388 /
9999 / END OF TRF IND MATRICES
9999 / END OF TRF RES MATRICES
1 / ONE ACTUAL TRANSFORMER
1 0 1 / TRF NUM, RES TYPE, IND TYPE
1 0 /
2 0 /
9999 / END OF TRF SPECS
9999 / END OF TLINE TYPE DATA
9999 / END OF TLINE SPECIFICATION
```