

**DEVELOPMENT OF A LOW COST
SPREAD SPECTRUM RADIO LINK**

BY

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A Thesis
Submitted to the Faculty of Graduate Studies
in Partial Fulfillment of the Requirements
for the Degree of

MASTER OF SCIENCE

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ABSTRACT

The purpose of the project described in this thesis is to design, implement and test a low cost spread spectrum radio system for operation in the 900 MHz band in order to demonstrate the feasibility of a low cost wireless data link which does not require licensing.

Recently introduced radio frequency emissions regulations allow civilian applications of spread spectrum systems which do not require licensing, and which can operate with up to one watt of output power with loose frequency stability requirements. This has made wireless data link technology suitable for applications which require flexible and economical communications capability.

This paper describes some common spread spectrum techniques and proposes a number of possible configurations for a low cost spread spectrum system. A novel synchronization and tracking technique is developed and used in the design of a general purpose system which is useful for a number of wireless data link applications such as low cost remote control, locating and recovery, and personal computer data links. Schematics, cost summary and performance of the prototype system are given.

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1. INTRODUCTION

Spread spectrum systems have historically been used for military applications where strategic communication links are required for interference rejection ability, low probability of detection and interception, or navigational capabilities. New radio frequency (RF) emissions regulations allow use of unlicensed spread spectrum radio links for commercial use. This has resulted in a new market for low cost unlicensed radio links.

This paper begins with a discussion of the traditional reasons for using spread spectrum. It then describes some potential applications for low cost and unlicensed commercial systems. A summary of common spread spectrum techniques and issues is given in chapter 2. Chapter 3 proposes and evaluates various low cost system configurations. A low cost synchronization and tracking technique was developed for this project and is described. This leads to the design of a general purpose system which can be used for a number of low cost wireless data link applications. A circuit description and schematics are given, as well as a parts cost summary. Performance measurements for various aspects of operation are also provided. The paper concludes with an evaluation

of the prototype system with respect to performance and required optimizations. Also presented are future design possibilities for further operational enhancements and cost reduction.

1.1 HISTORY AND TRADITIONAL REASONS FOR USING SPREAD SPECTRUM

The major push for the development of spread spectrum technology has historically been the requirement for secure defense communications. Various communication systems were developed to provide high performance strategic links and tended to use expensive equipment. Some of these strategic links are listed below:

- JTIDS (Joint Tactical Information Distribution System)
 - used by NATO for data networking
- TDRSS (Tracking and Data Relay Satellite System)
 - satellite tracking system
- SPIN (Systeme Protege d'Information Numerique)
 - French ship to shore radio
- HAVE QUICK 2
 - NATO voice communication
- SINCGARS (Single Channel Ground Airborne Radio System)

- voice and data communication
- HYDRA/V (Hybrid Defense Radio in UHF Range)
- Army communication

A good review of events leading to the development of spread spectrum communication systems is given in [3].

A common question that arises when first discussing spread spectrum radio links is "why increase the bandwidth of a radio channel when there is an ever increasing demand for spectrum space?" Some of the benefits of using spread spectrum are outlined below:

a) interference rejection

The most common reason for using spread spectrum has historically been for operation in the presence of channel jammers or intentional interferers. The relationship between channel capacity and bandwidth in the presence of noise is given by C. E. Shannon [20] as:

$$C = W \log_2(1 + S/N)$$

where C = channel capacity in bits per second

W = bandwidth in Hz

S = received signal power

N = received noise power (channel jammers or other)

This equation shows that for a given signal to noise ratio in a channel, a higher error free data rate is obtainable with an increase in channel bandwidth. This relationship is reflected in the definition of processing gain for a spread spectrum system. From [4],

$$G_p = BW_{RF}/BW_{data}$$

for a typical direct sequence spread spectrum system

where G_p = processing gain

BW_{RF} = spread spectrum channel bandwidth

BW_{data} = data bandwidth.

Processing gain denotes the reduction in the effect of an interfering jammer signal. Performance of spread spectrum systems in jamming environments is given in [7] and [4].

b) secrecy

Spread spectrum systems are capable of a low probability of detection. The transmitted signal power is spread over a broad bandwidth so that the peak power spectral density is low and therefore less detectable in noise. [8]

c) multiple access

Code division multiplexing and message privacy are

possible over the same channel by using codes with good cross correlation properties [9]. Cross correlation properties will be discussed in Section 2.2.2.

d) navigational ranging

When the relative phase delay between a direct sequence transmitter code and receiver code is found, an indication of transmitter to receiver distance can be calculated from the propagation velocity of the signal. This technique is used for ranging and position location. [10] [11] [12]

e) multipath rejection

Some of the effects of multipath propagation can be reduced by using spread spectrum. A small delayed signal component will look like interferer noise to the receiver and its effect can be reduced by as much as the processing gain of the system. [13]

1.2 APPLICATIONS OF LOW COST SPREAD SPECTRUM SYSTEM

In May 1985 the Federal Communications Commission (FCC) changed its rulings to allow commercial applications of spread spectrum systems. The regulations permit using spread spectrum

links in the ISM bands, for Amateur Radio Service and for Police Radio Service. The FCC also allows commercial use of unlicensed spread spectrum systems provided that the output power does not exceed 1 watt. Previously, unlicensed radiators were only allowed -80dBw output for frequencies between 216 MHz and 960 MHz. Appendix A discusses these FCC policies in great detail.

The authorization of wireless spread spectrum links for unlicensed commercial use has created a new commercial market for low cost data radio communications. Higher data rates and longer distance links are now possible which do not require FCC licensing procedures. The additional benefits of interference rejection, secrecy, and multipath rejection are also obtained by the use of spread spectrum. Some potential consumer and industrial uses are described below.

a) Remote control

Inexpensive wireless remote control systems can be implemented using low cost spread spectrum links. These systems perform well using slower data rates and packet type transmissions.

Remote control networks can be set up for power management by computer or for central switch control of lighting

spread over a large area.

Wireless consumer domestic control bus implementation is possible using spread spectrum. Various HOME BUS type systems are presently being introduced for home automation and entertainment in the consumer electronics field.

Factory automation and remote control of robots is another area that can benefit from spread spectrum links. The processing gain afforded by the use of spread spectrum provides resistance to interference and multipath effects which occur in factory environments.

b) Locating and recovery

The recovery of stolen vehicles is an application where an inexpensive and compact transmitter is required. A network of receivers could be set up to locate a transmitter which was triggered by a break-in alarm. The market for stolen vehicle recovery systems is rapidly expanding and the FCC has just recently allocated the 173.075 MHz frequency specifically for radio-based vehicle recovery systems. The transmitter for this type of network is a high volume item and must be concealable while those constraints do not exist for the receiver. The spread spectrum transmitter designed in this

paper is an extremely low cost method of radiating up to 1 watt of RF power at a frequency of 900 MHz. The radiated spectrum has a power spectral density with peaks 24 dB lower than a similar powered CW spectrum and this decreases the probability of detection by unwanted parties.

The same system could be used to locate persons who have left the confines of a designated area.

c) Data communications

A low cost, wireless remote communication modem that does not require licensing is an extremely attractive alternative to cabled computer links. A spread spectrum link can provide these properties and at the same time operate well in an indoor multipath environment.

2. PRESENT SPREAD SPECTRUM TECHNIQUES

This chapter presents the common spread spectrum techniques generally used for generation of the wideband signal and for synchronization and tracking in a spread spectrum receiver. The principle of operation for direct sequence and frequency hopping spreading systems is described first. Pseudo-random codes used in spread spectrum generation are then discussed and it is shown how spread spectrum system properties are a direct result of the code characteristics. The requirement in the spread spectrum receiver for code synchronization and tracking is introduced and methods for performing this function are shown. Included are sliding correlator, sequential estimation and transmitted reference synchronization techniques and delay lock loop tracking technique.

2.1 SPECTRUM SPREADING METHODS

This section will discuss general principles of some common spectrum spreading methods. The common methods used to generate the wide bandwidth spread spectrum signal are direct sequence spreading and frequency hopping spreading.

2.1.1 Direct sequence

A typical direct sequence spread spectrum system is shown in Figure 1.

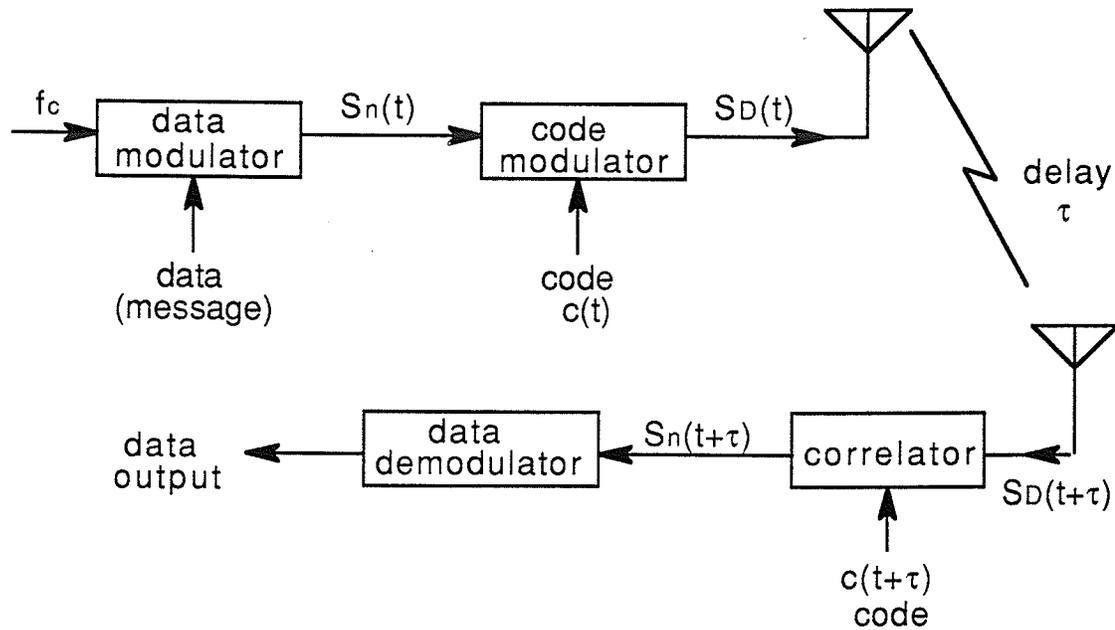


Figure 1: Direct sequence spread spectrum system

The signal is generated by first modulating a carrier f_c by a data (or message) signal. The resulting message signal $S_n(t)$ is then modulated by a high speed spreading code $c(t)$ to produce a final spread spectrum signal $S_D(t)$. The digital spreading code is at a much higher frequency than the data rate. This spreads the signal

$S_n(t)$ over a wide bandwidth to permit a system processing gain as described in Section 1.1a. The data modulator and the code modulator can in general perform any type of modulation. The code used is a pseudo-random code that will be discussed in Section 2.2. The output spectrum bandwidth is a function of the code rate. Most systems have a 3dB bandwidth close to the code rate frequency, depending on the code modulator type. The receiver despreads the signal by correlating with a time delayed replica of the transmitter code $C(t+\tau)$. The despread or correlated signal $S_n(t+\tau)$ is then demodulated as if the signal $S_n(t)$ had never been spread.

To illustrate operation of such a system, we consider a commonly used biphasic phase shift key (BPSK) code modulator. For BPSK spread spectrum a digital bipolar code directly multiplies a message signal $S_n(t)$. This is shown in Figure 2a and b where the message signal $S_n(t)$ is equal to S_n over the time interval shown. Assuming a transmitter to receiver link with propagation delay τ and no attenuation or added noise or distortion, the received signal is $S_D(t+\tau)$. If the receiver multiplies this signal with an in phase replica of the transmitter code delayed by τ , the time shifted

original signal $S_n(t+\tau)$ is recovered (Figure 2 c,d,e). The message signal is then recovered by demodulating $S_n(t+\tau)$ as if it had never been spread.

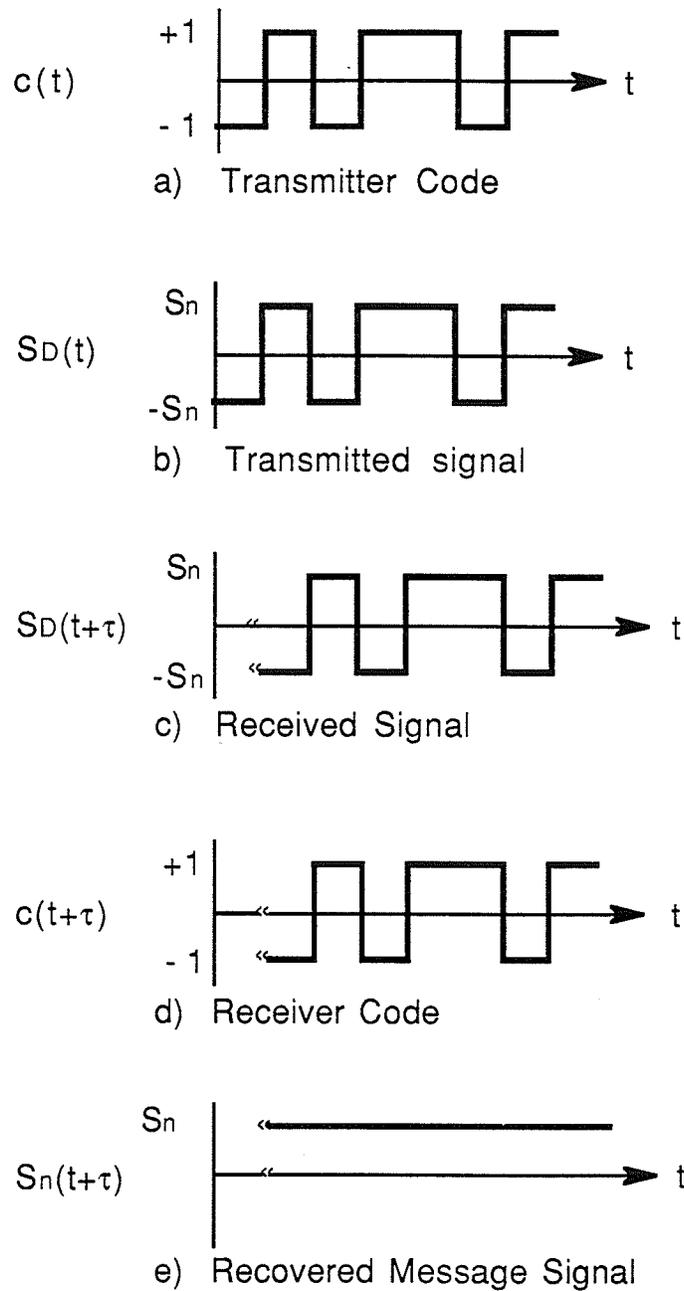


Figure 2: Operation of a direct sequence BPSK system

2.1.2 Frequency hopping

A typical frequency hopping spread spectrum system is shown in Figure 3.

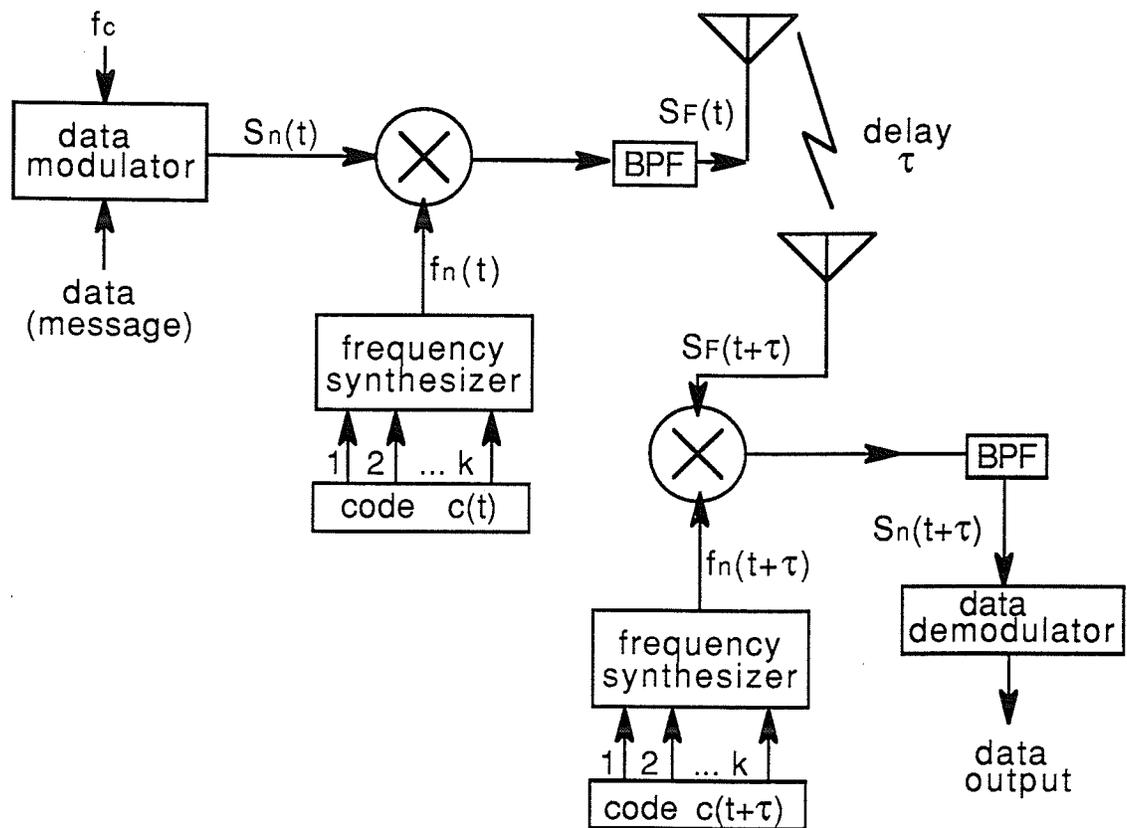


Figure 3: Frequency hopping spread spectrum system

The transmitter for the system modulates a carrier frequency f_c by a message signal, and shifts this output spectrum up in frequency by an amount f_n . The code $c(t)$ determines the synthesizer output

frequency f_n . This transmitter output $S_F(t)$ can be viewed as a typical data transmitter that periodically switches channels or "hops". The numerous frequencies used (2^k) effectively spread the spectrum of the modulator output. A slow hopping system transmits several data bits before hopping to a new channel, while a fast hopping system transmits one or fewer data bits between hops.

Assuming the same transmission link as in Section 2.1.1, the receiver input $S_F(t+\tau)$ is a time delayed version of the transmitter output. The receiver uses a time delayed replica of the transmitter code $c(t+\tau)$ to set its frequency synthesizer. The spectrum of $S_F(t+\tau)$ is thus downconverted by the same amount that $S_n(t)$ was upconverted. The signal $S_n(t+\tau)$ is then demodulated as if it had never been spread.

2.1.3 Others

Spread spectrum techniques presently allowed by FCC for commercial radio links are direct sequence and frequency hopping. Other types of systems include:

- Pulsed FM or CHIRP modulation which uses matched filters to spread and then despread;
- Time hopping which uses a code to key the transmitter on and off;
- Hybrid forms which use a combination of all the above, i.e. a direct sequence system which hops between channels. Dixon [2] gives a more detailed discussion of CHIRP, time hopping, and Hybrid.

2.2 PSEUDO-RANDOM CODE PROPERTIES

The characteristics of pseudo-random or pseudo-noise (PN) codes give spread spectrum systems their unique properties. This section will present a code generation technique, discuss useful code properties, and illustrate how the power spectral density is affected by the code parameters. This section will concentrate on linear maximal sequences since they are well known and easy to generate. Most other codes are based on linear maximal codes.

2.2.1 Code generation

A PN code is a periodic signal; within each period is a random alternation of 1's and 0's. Reference [6], page 336, gives a full

definition of a PN code. A common form of a PN generator is the linear simple shift register generator (SRG). This generator consists of a shift register with feedback that is the modulo-2 sum of the shift register state, Figure 4.

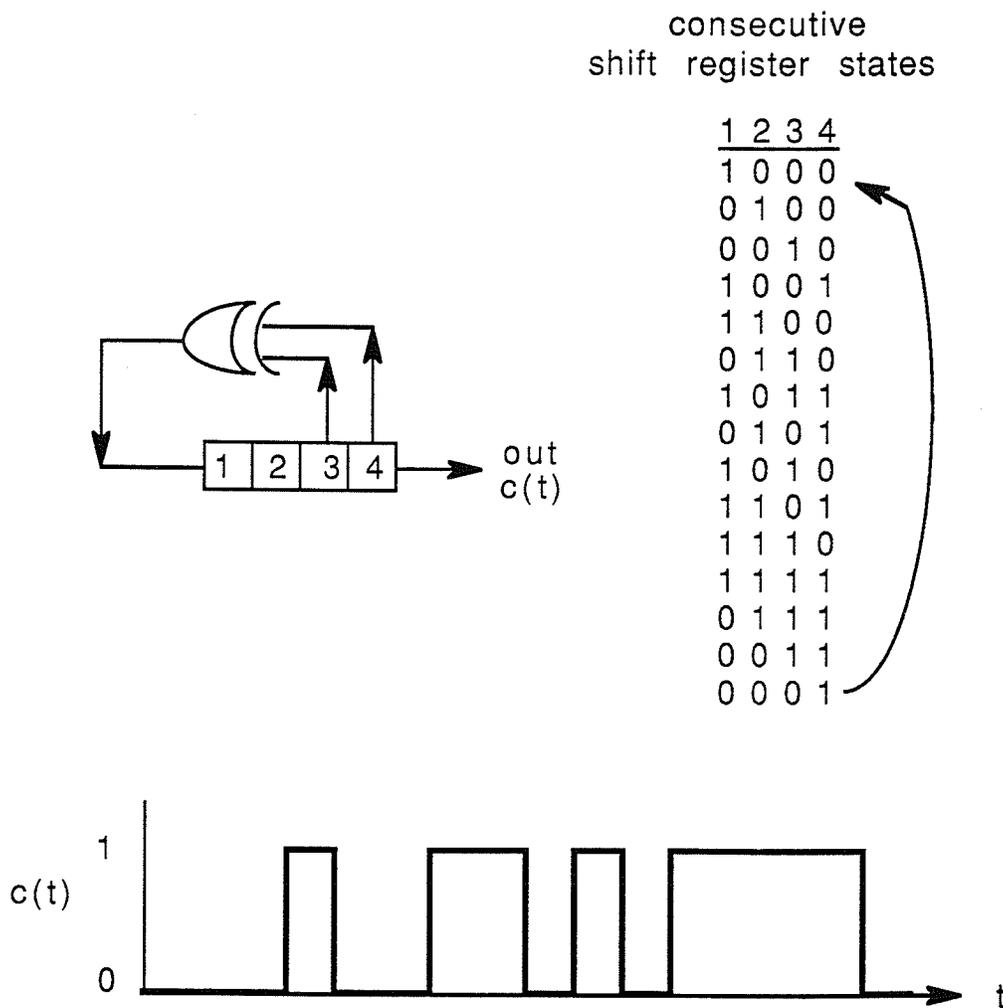


Figure 4: 4-bit simple shift register generator

The position of the feedback taps determines whether the generator is maximal. For all maximal sequences, if the SRG has an n bit shift register, then the code length is $2^n - 1$ bits (or "chips" when referring to spread spectrum systems). The code period T_c is then $(2^n - 1)/R_b$ where R_b is the bit rate of the generator. The simple SRG, as in Figure 4, is denoted by the feedback taps [4,3] or by polynomial representation $1 + x^3 + x^4$. For a maximal sequence SRG, feedback always includes the last bit, there is an even number of feedback taps and the shift register cannot contain all 0's. Appendix A shows some feedback connections for generating linear maximal sequences of lengths $2^2 - 1$ to $2^8 - 1$.

2.2.2 Correlation properties

The correlation properties of a maximal code allow the receiver to synchronize its locally generated code to the received code, and to distinguish between multiple users as in code division multiplexing.

The normalized autocorrelation function of a linear maximal PN code $c(t)$ is

$$R_{cc}(\tau) = \frac{1}{NT_c} \int_0^{T_c} c(t) c(t+\tau) dt$$

where $N =$ sequence length $(2^n - 1)$

$T_c =$ code period (N/R_b) .

The autocorrelation function is well defined for this type of sequence. It is a periodic triangular function as shown in Figure 5. A receiver searching for synchronization can use this property and calculate the autocorrelation function for different relative phase differences between the received code and its locally generated code.

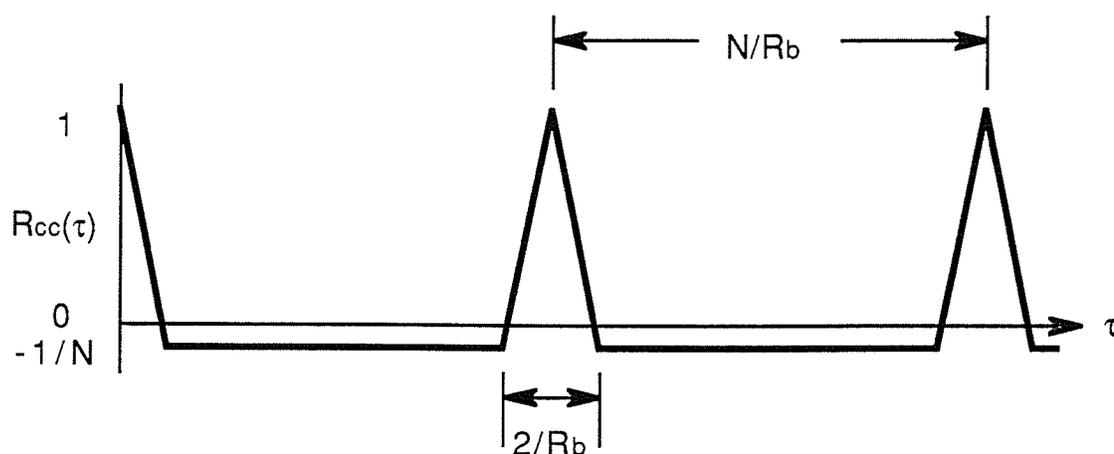


Figure 5: Autocorrelation function of linear maximal PN code

As Figure 5 shows, the autocorrelation function varies between 1 and $-1/N$ to give the receiver an index of discrimination of

$$\left[(1 + 1/N) / (1/N) \right] \quad \text{or} \quad 10 \log (N+1) \text{ dB}$$

between synchronized and unsynchronized signals. Figure 4 also indicates that synchronization can only be measured to ± 1 chip from perfect synchronization. High "minor" correlation peaks occur if the autocorrelation function is not evaluated over an entire code period.

The normalized crosscorrelation of a code $c(t)$ and another code $c'(t)$ with the same code length and bit rate is

$$R_{cc'}(\tau) = 1/(NT_c) \int_0^{T_c} c(t) c'(t+\tau) dt$$

The crosscorrelation properties between different codes allow a receiver to differentiate between distinct transmitters; however, crosscorrelation of linear maximal sequences is not well defined. For example, crosscorrelation of codes [5,3] and [5,4,3,2] has a value that varies between $7/31$ and $-9/31$ while crosscorrelation of codes [5,3] and [5,2] has a value that varies between $11/31$ and $-9/31$

(page 77, [2]). If codes [5,3] and [5,4,3,2] were used in the same link, the receiver would have to differentiate between a peak autocorrelation value of 1 and a peak crosscorrelation value of 7/31. The index of discrimination when operating with these 2 codes is

$$\left[(1 - 7/31)/(1/31) \right] = 24$$

while the index of discrimination when using only one of the codes is 32. This relates to a reduction in discrimination of 25%. By comparison, the reduction in discrimination when using codes [5,3] and [5,2] is 38%. When using a number of codes for a multiple access application, the crosscorrelation properties of all pairs must be investigated. Table 1 gives the number of possible linear maximal sequences for a given generator length n .

Some composite codes, or codes made up of a combination of linear maximal codes, have bounded crosscorrelation properties. That is, crosscorrelation peaks for a set of codes can be calculated without considering each pair separately. An example of such a class of codes is Gold codes ([2] page 81).

Table 1: Number of possible linear maximal PN codes from n bit generators (from [2])

n	Number of Codes
3	2
4	4
5	6
6	4
7	18
8	16
9	48
10	60
11	176
12	96
13	630
14	756
15	1,800
16	2,048
17	7,710
18	1,728
19	27,594
20	19,200
21	72,576
22	120,032
23	356,960
24	184,320
25	1,296,000
26	1,719,900
27	4,260,864
28	4,741,632
29	18,407,808
30	11,880,000
31	69,273,666
61	31,800,705,069,076,960
89	6,954,719,320,827,979,072,466,990

2.2.3 Power spectral density

The power spectral density of a PN code is calculated from its autocorrelation function. (The normalized autocorrelation function of a linear maximal PN code was presented in Section 2.2.2 and plotted

in Figure 5). The power spectral density $G_c(f)$ is calculated from the Fourier transform of the autocorrelation function $R_{cc}(\tau)$. From [6] we obtain the normalized power spectral density:

$$G_c(f) = (1/N^2) \delta(f) + [(N+1)/N^2] \sum_{\substack{m=-\infty \\ m \neq 0}}^{\infty} \text{sinc}^2 [(m\pi/N) \delta(f + m/NT_b)]$$

where $T_b = 1/R_b =$ chip length (period). This is plotted in Figure 6 for an $n=3$ bit linear maximal sequence generator.

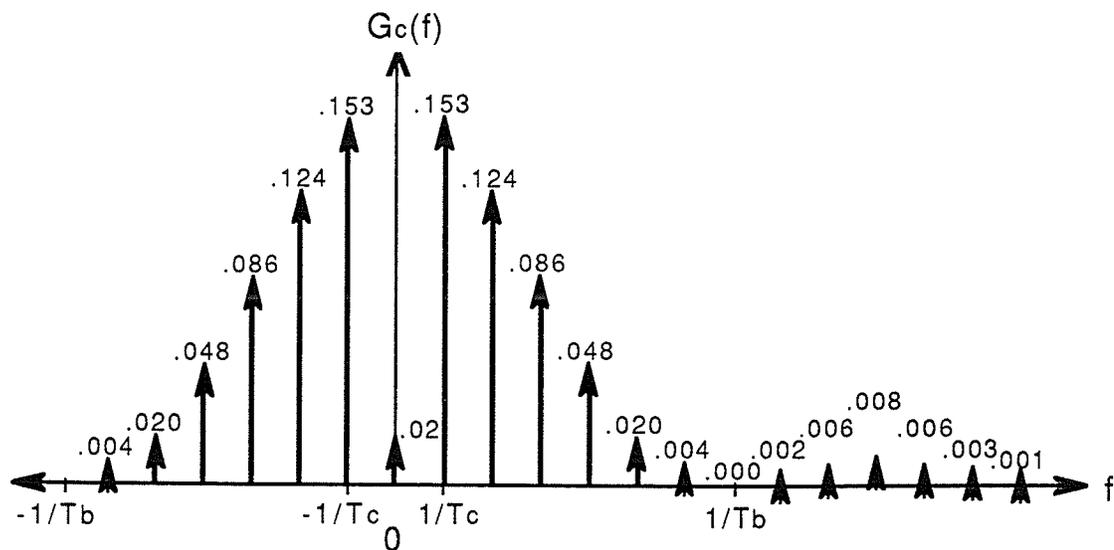


Figure 6: Power spectral density of 3-bit linear maximal SRG

The code length N is $2^3-1=7$ bits. The spacing between spectral components is $1/(NT_b) = 1/T_c$. The spacing between main lobe nulls is $2/T_b = 2R_b = 2 \times \text{bit rate} = 2 \times \text{SRG clock rate}$. Therefore, a longer code length N will reduce the spectral separation, and a higher chip rate will increase the null to null bandwidth. The total power in the signal S_c is

$$S_c = \int_{-\infty}^{+\infty} G_c(f) df.$$

From this we can determine that 90% of the signal power is contained in the main lobe of the spectrum.

2.3 SYNCHRONIZATION

The receiver for the spread spectrum systems presented in section 2.1 requires a locally generated coherent replica of the received transmitter code. The receiver knows which PN code to generate, but it needs to synchronize the code to the incoming code. This section will describe the sliding correlator, sequential estimation and transmitted reference synchronization techniques.

2.3.1 Sliding correlator

The simplest synchronization technique is the sliding correlator. The receiver clock operates at a different rate than the transmitter, giving the effect of the relative code phases changing (or sliding) with respect to each other. The receiver's synchronization detector performs an autocorrelation calculation at each new phase position. This autocorrelation value determines whether or not the receiver has obtained synchronization.

The maximum allowable difference between transmit and receive code clocks during synchronization is limited by the bit rate and code length of the system. The correlation detector must integrate over one entire code period (T_c) in order to have the autocorrelation properties described in Section 2.2.2. (i.e., high discrimination between synchronization and non-synchronized). For a code transmitted at 1 Mbps, and of length $N = 2^8 - 1 = 255$ bits, the code period is $T_c = 255\mu\text{s}$ and the bit period is $T_b = 1\mu\text{s}$. A reasonable limit for clock slip per integration period T_c is $T_b/2 = 0.5\mu\text{s}$. This ensures obtaining more than half the peak autocorrelation value available. For a transmitter clock f_1 equal to

1.000 MHz, the receiver clock must be within $.5\mu\text{s}/255\mu\text{s} \times f_1 = 0.2\%$ of f_1 . The time required for the synchronization detector to check all $N=255$ possible bit positions or phases at this maximum slipping rate is then

$$T_{\text{sync}} = T_c \times \left[T_c / (T_b / 2) \right] = 130 \text{ ms.}$$

T_{sync} is the worst case (all 255 bit positions checked before synchronization is found) minimum (slipping at maximum rate $T_b/2$ in T_c) synchronization time for the above conditions. For a particular application, T_{sync} would be longer or shorter to optimize system requirements of synchronization time, probability of false synchronization detection and probability of missed synchronization.

Faster synchronization is possible by shortening the PN code length T_c at the beginning of a transmission, since T_{sync} is proportional to T_c^2 . The code length can then be increased once synchronization is found. This method does however reduce the system G_p during the synchronization procedure. The technique is often referred to as a synchronization preamble.

2.3.2 Sequential Estimation

Sequential estimation can give a great reduction in synchronization time over the sliding correlator. It is used for direct sequence type spread spectrum systems. Again this is at the expense of further degrading G_p during the synchronization procedure.

The receiver uses a coherent demodulator to decode the received spreading code in order to find the exact phase of the PN sequence. For an n -bit code generator, this would require n demodulated code chips. Once the phase is known, the receiver's code generator can start at that point, and the receiver switches to its despreading mode. As there is no system processing gain during the phase position search, it can take a long time to synchronize in a noisy environment. Using more than n data bits to find the correlation position will improve operation in noisy environments.

[18]

Similar to sequential estimation is the matched filter synchronizer. An example of one such device is the Surface Acoustic Wave Convolver. [17]

2.3.3 Transmitted Reference

A technique that does not require a search for synchronization at the receiver is the transmitted reference method. The transmitter's PN code modulates two separate carrier frequencies separated by f_s . One of the carriers is modulated by the data and both are spread by the PN code. The receiver separates the two channels and multiplies the signals together. The result is an IF frequency equal to f_s and modulated by the data. This is shown in Figure 7.

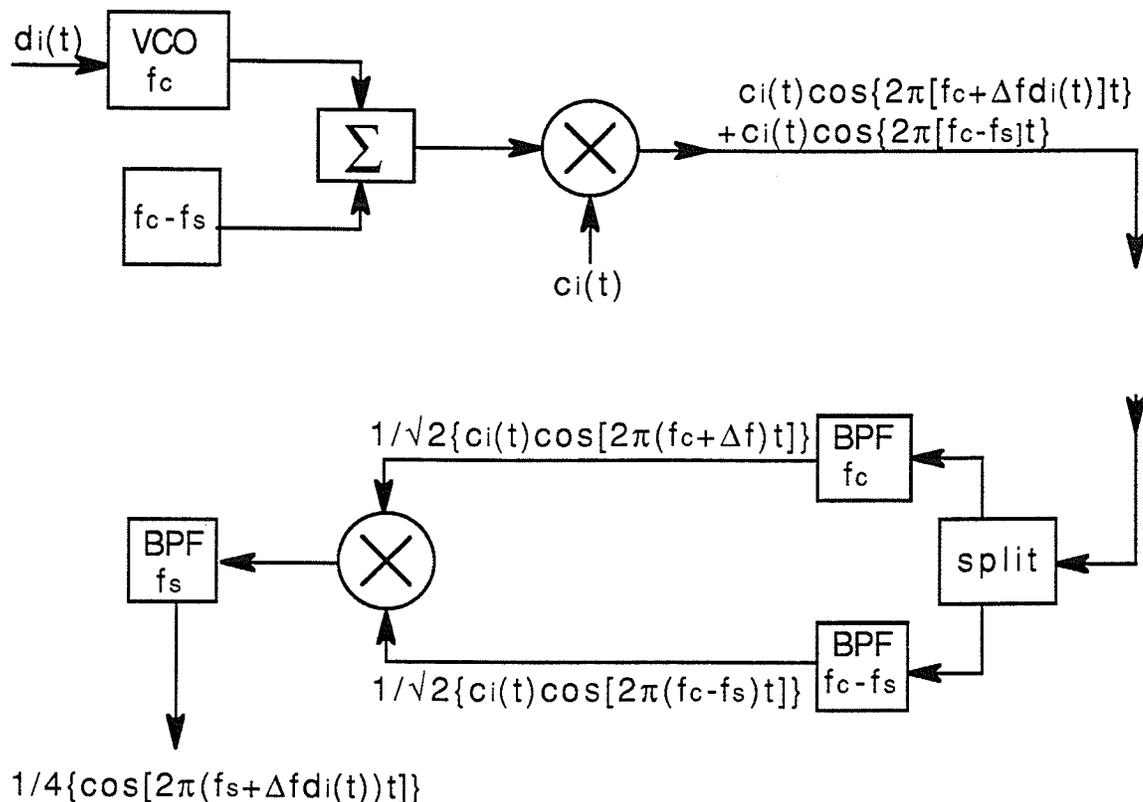


Figure 7: Transmitted reference method

2.4 TRACKING

Once a receiver synchronizes its locally generated code with the received code, it must maintain this coherency for variations in transmitter and receiver code clocks (The obvious exception to this requirement is for a transmitted reference system where the receiver does not generate its own code). For example, a code generated at 1 Mbps with a ± 5 ppm clock stability at transmitter and receiver can move one bit from perfect synchronization in

$$1 / [10^6 \text{ bps} \times [(5+5) \text{ bits} \times 10^{-6}]] = 0.1 \text{ s.}$$

A common method of performing the required tracking function is the use of a delay lock loop. This technique uses two correlators, one with its code delayed up to two bits, to produce a tracking error signal which in turn controls the receiver code clock rate. The tracking error signal is generated by subtracting autocorrelation functions of two offset correlators as in Figure 8.

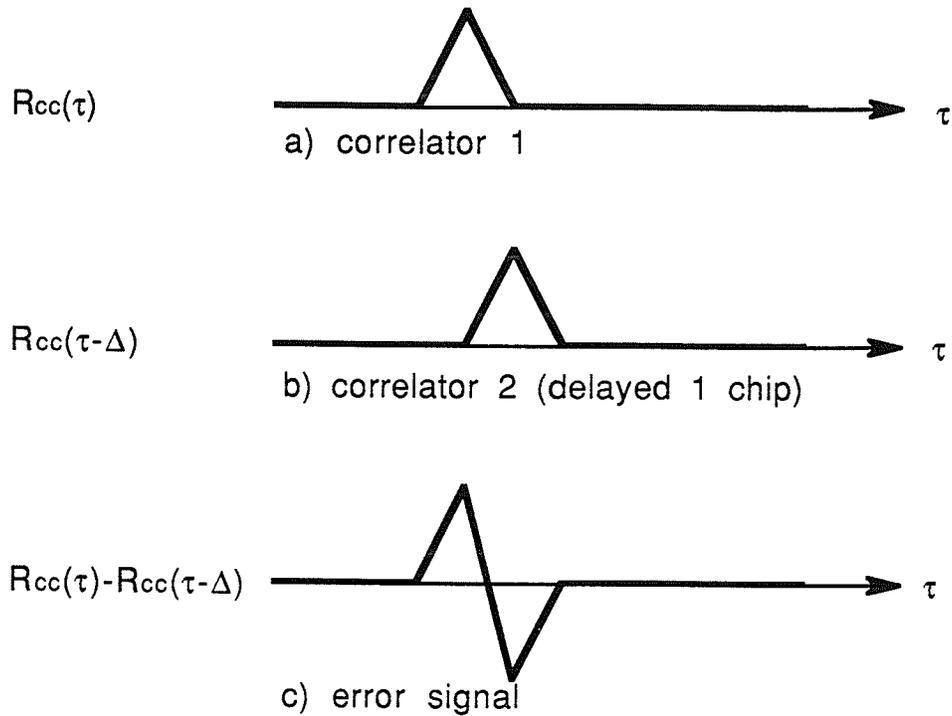


Figure 8: Delay lock error signal generation (for 1 chip delay loop)

If the delayed code driving channel 2 has a higher correlation than channel 1, the error signal goes negative which slows the code clock. The code clock speeds up for higher correlation on channel 1. The tracking loop is shown in Figure 9.

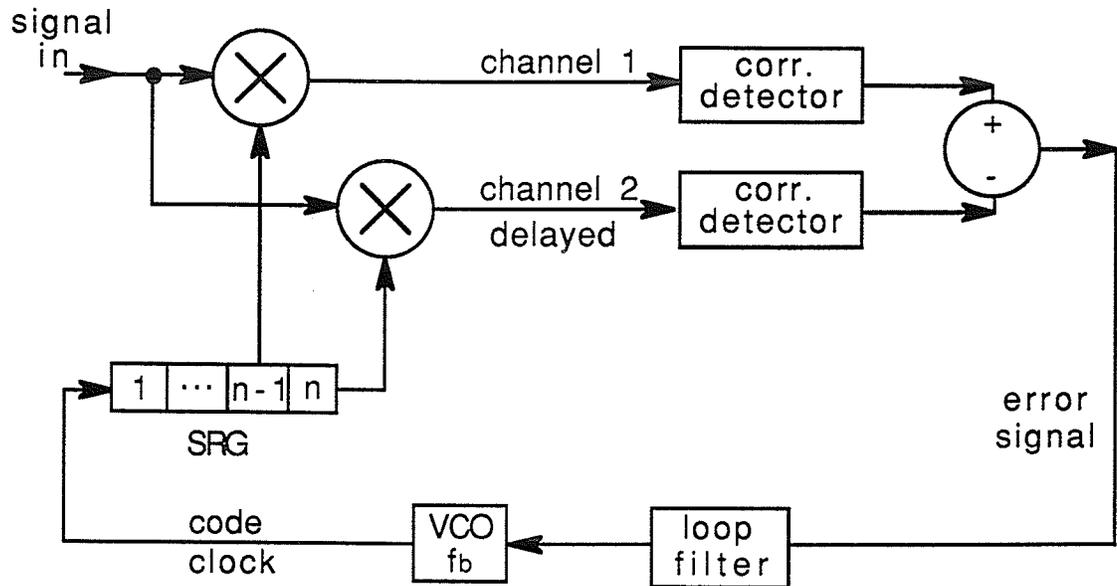


Figure 9: Delay lock tracking loop

Another tracking loop similar to the delay lock loop is the Tau-Dither tracking loop. The Tau-Dither loop requires only one channel and "dithers" the code clock rate in order to generate an error signal [19].

3. LOW COST SPREAD SPECTRUM IMPLEMENTATION

The previous chapter showed various spread spectrum techniques. This chapter will discuss a number of economical implementation options and evaluate the relative performance of the various configurations. Included is a novel tracking technique developed for this project, which makes use of the synchronization detector circuit. A final system is arrived at which provides a simple transmitter and receiver that form a low cost spread spectrum data link. The actual circuits for the system are designed and the resulting system can provide an inexpensive solution to a wide range of applications which require modest data rates, up to 1 watt output power and resistance to interference and multipath effects. A circuit description, schematics and parts costs are given. Performance measurements are made on the prototype system to demonstrate various operational characteristics and capabilities.

3.1 LOW COST SPECTRUM SPREADING TECHNIQUE

Frequency hopping and direct sequence are the only techniques considered for this project since they are the only ones presently allowed by FCC for commercial use.

In terms of development time required for this project, frequency hopping synthesizer design is more involved than the frequency source required for a direct sequence system. The synthesizer must have well defined and fast locking characteristics over a large number of frequencies. Attention must also be given to phase coherency upon frequency hops. In general, the frequency stability requirement is also more stringent for frequency hopping. Parts cost of a hopper synthesizer would similarly be higher.

Due to the availability of specific test equipment and the less stringent frequency source requirements, direct sequence is the candidate chosen for this experimental system.

3.2 COMPARISON OF MODULATOR TECHNIQUES

The demonstration system that will be investigated from here forth is direct sequence spread spectrum with a linear maximal PN code. The reasons for this were presented in Section 3.1. From the block diagram in Figure 1, the data modulator and code modulator techniques need to be determined. This section will discuss some code modulator techniques and show their effects on system complexity and performance. Some data modulator techniques and

their associated receiver possibilities are then presented. The final choice of modulation techniques pursued is presented. The focus again is on low cost implementation and complexity.

3.2.1 Code modulators and effect on performance

The major modulator techniques commonly used are Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Biphasic Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK) and Minimum Shift Keying (MSK).

ASK has a main lobe null to null bandwidth of $2xR_b$, but the signal contains at most half the power per symbol as FSK or BPSK. ASK has poor performance under signal jamming conditions and is extremely sensitive to system nonlinearities.

FSK has a main lobe null to null bandwidth equal to $3xR_b$ for orthogonal tone spacing ($\Delta f = R_b/2$), and development of the code modulator and correlator is more difficult than for BPSK.

BPSK has a main lobe bandwidth of $2xR_b$, and has a signal to noise performance about 3dB better than orthogonal FSK. BPSK modulators and correlators can simply be balanced mixers which are readily available.

QPSK has a main lobe bandwidth of $1xR_b$ that contains the same signal power as BPSK, with minimal signal to noise degradation. The modulator and correlator however have at least twice the complexity as BPSK.

MSK has a main lobe bandwidth of less than $2xR_b$, dependent upon the format used. MSK has low sidelobe energy and can better tolerate system nonlinearities [2]. Modulator and correlator complexity is similar to that of QPSK.

BPSK is the simplest, most inexpensive to implement and components are readily available. It gives good overall performance since the bandwidth restriction for this application is easily met. For these reasons the code modulator and correlator chosen are BPSK, implemented with balanced mixers.

3.2.2 Data modulator tradeoff between cost and performance

This section will consider the implications of ASK, BPSK and FSK data modulators on system implementation. This analysis uses the BPSK code modulator decided upon in Section 3.2.1. Digital data

modulation is assumed. Section 3.2.2c will illustrate the effects of an interferer on a direct sequence system.

3.2.2 a) ASK carrier

Figure 10 shows an ASK carrier BPSK direct sequence transmitter for the extreme case of On-Off keying (OOK).

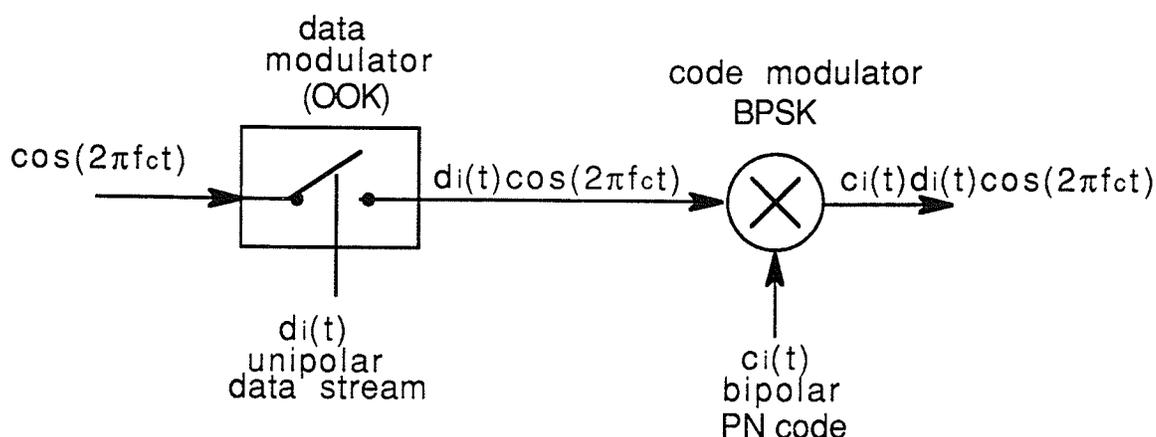
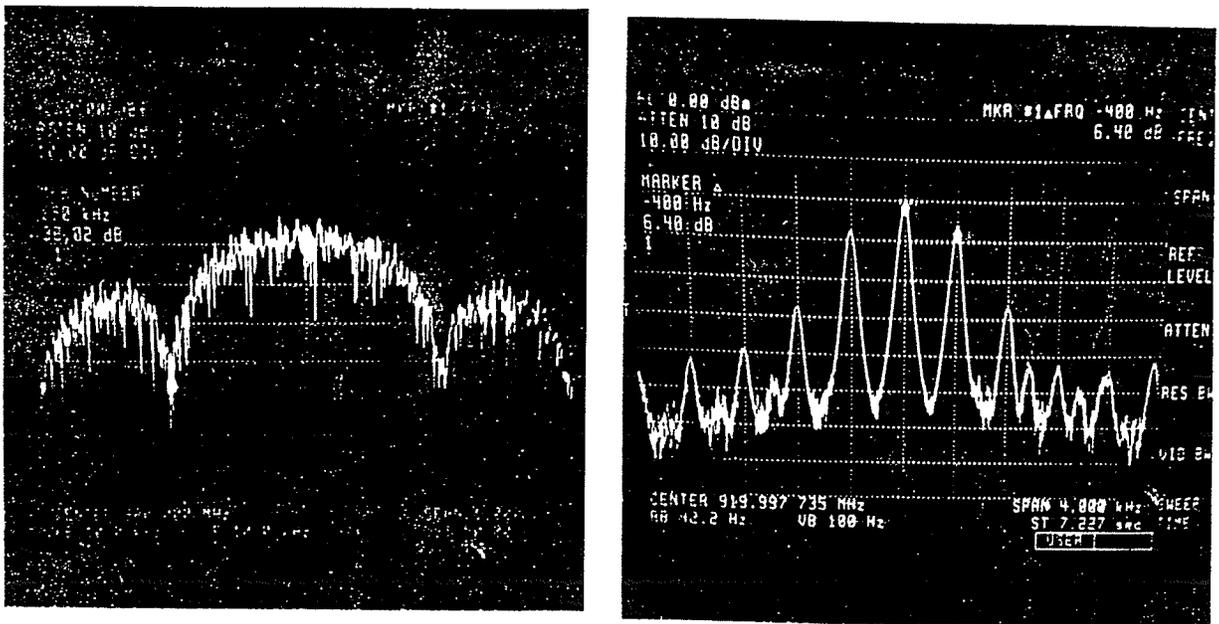


Figure 10 : ASK carrier BPSK transmitter

In Figure 10, f_c is the carrier frequency, $d_i(t)$ is a unipolar data stream (1 or 0 valued), and $c_i(t)$ is a bipolar (+1 or -1 valued) linear maximal PN code. In this case the data modulator is as simple as a switch, and the code modulator is a balanced mixer. The output spectrum of such a system is shown in Figure 11a.



a) Transmitter output spectrum b) Correlator output spectrum

1 MHz span

4 kHz span

$$f_c = 920 \text{ MHz}$$

$$d_i(t) = 400 \text{ Hz sine wave}$$

99% modulation

$$c_i(t) = 250 \text{ kbps}$$

$$2^8 - 1 \text{ chip code}$$

Figure 11: ASK carrier BPSK spectrum

A receiver for this system consists of a correlator (despreader) which is followed by a data demodulator. The despreading stage is shown in Figure 12.

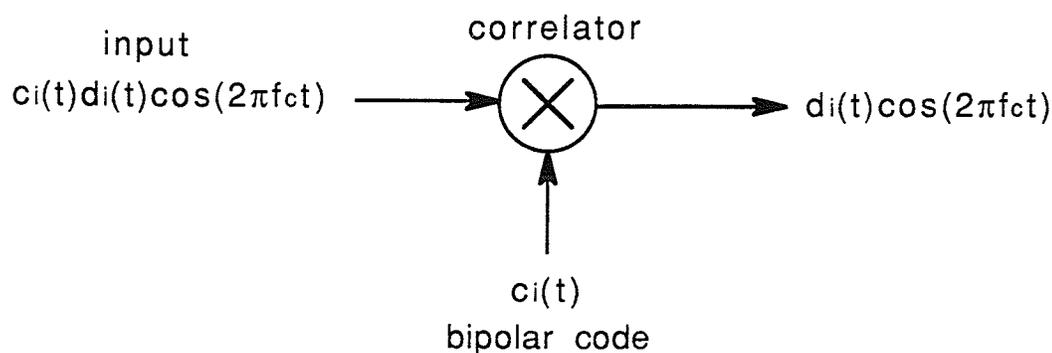


Figure 12: Coherent ASK carrier BPSK receiver correlator

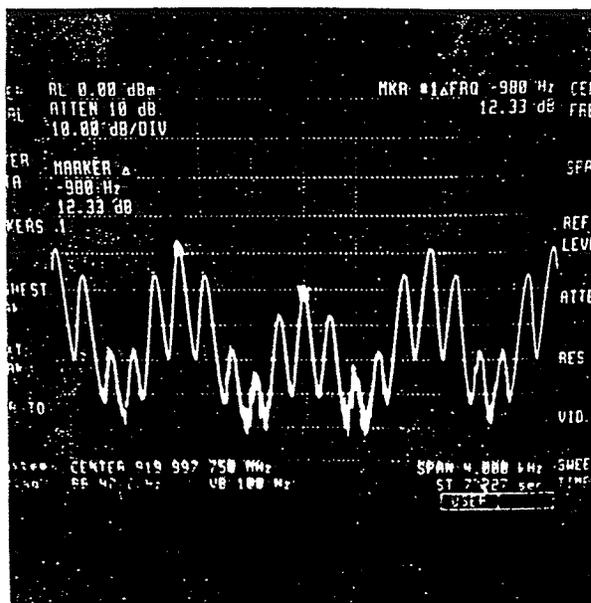
As shown earlier in Figure 2, $c_i(t) c_i(t) = 1$ and so the correlator effectively despreads the signal. The despread spectrum is shown in Figure 11b. A regular ASK demodulator is then used to recover the data stream.

The major difficulty with the above receiver is the fact that the correlator is required to generate the same PN code as the transmitter with an exact phase relationship or delay (Figure 2). A receiver which does not need an exact code reference is possible. By rewriting the receiver input signal (Figure 12) we get $[d_i(t)] [c_i(t) \cos(2\pi f_c t)]$. This shows that the entire spectrum is being amplitude modulated by the data stream. That is, the spectrum

looks like the PSD function of $c_i(t)$ (e.g. Figure 6) centered at f_c .

Each spectral line of this spectrum is amplitude modulated by $d_i(t)$.

This can be seen in Figure 13, which is actually the same spectrum as Figure 11a but with a 4 kHz frequency span and 200 Hz data modulation.



$f_c = 920 \text{ MHz}$	span=4 kHz span
$d_i(t)=200 \text{ Hz sine wave}$	$c_i(t)=250 \text{ bps}$
99% modulation	28 - 1 chip code

Figure 13: ASK carrier BPSK transmitter output spectrum

A simple ASK detector circuit with an input filter covering a portion, or all of the spectrum, could recover the data signal $d_i(t)$. This

however would be impractical for most applications. Firstly, the signal to noise performance with no interferers would be degraded by an amount equal to the normally defined system processing gain G_p . Secondly, the link would be extremely susceptible to interferers; that is, any variations in received signal strength will add directly to the data signal.

3.2.2 b) BPSK carrier

A BPSK carrier BPSK direct sequence transmitter involves first multiplying the carrier frequency with a bipolar data stream, and then multiplying this result with a bipolar PN code. Since the order of multiplication does not matter, the code and data could first be multiplied in a low frequency multiplier, and this result multiplied by the carrier in a high frequency multiplier. Multiplication of two bipolar data streams has the same effect as modulo-two addition of two unipolar data streams. This process is referred to as code modified direct sequence. Figure 14 shows the modification process where $c_i'(t)$ and $d_i'(t)$ represent the unipolar versions of $c_i(t)$ and $d_i(t)$.

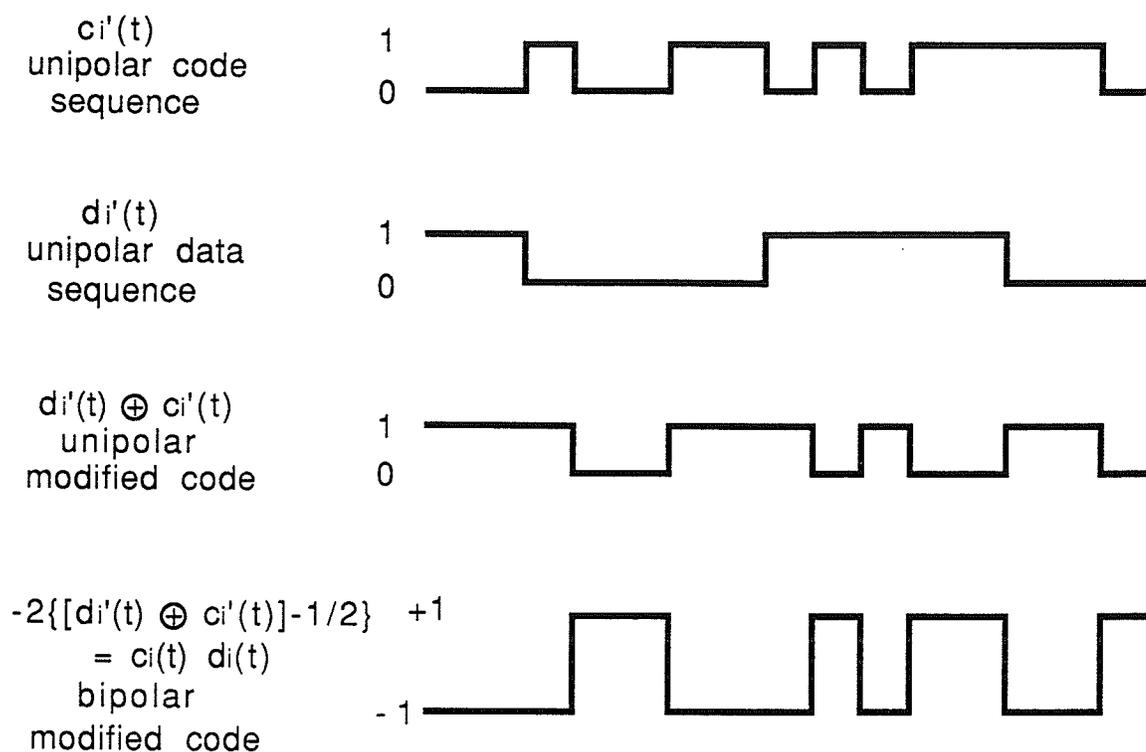


Figure 14: Code modification technique

One further note is the fact that the data and code streams must have synchronous transitions. This modified code can now be used to modulate the carrier, Figure 15. As the figure shows, only one logic gate and one balanced mixer are required.

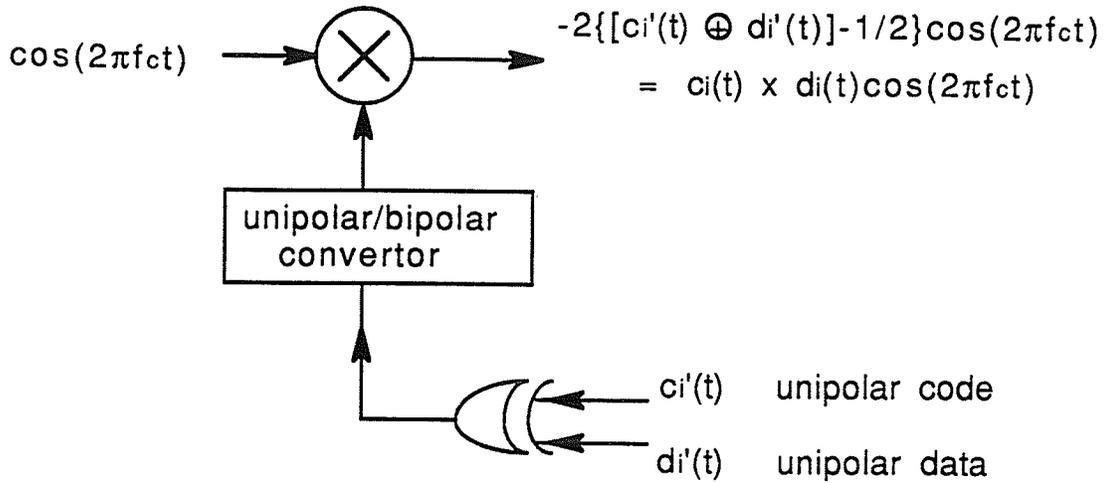


Figure 15: BPSK carrier BPSK (code modified) transmitter

The receiver again uses an in-phase replica of the received transmitter code to despread the signal. That is,

$$[c_i(t) d_i(t) \cos(2\pi fct)] \times [c_i(t)] = d_i(t) \cos(2\pi fct)$$

similar to Figure 12. The data demodulator now recovers the data from the BPSK coded signal. The data demodulator for BPSK requires coherent detection.

3.2.2 c) FSK carrier

In a FSK carrier BPSK direct sequence transmitter, a bipolar data signal sets the output frequency of a voltage controlled

oscillator (VCO) as in a typical FSK transmitter. The VCO output is then multiplied by a bipolar PN code as in Figure 16.

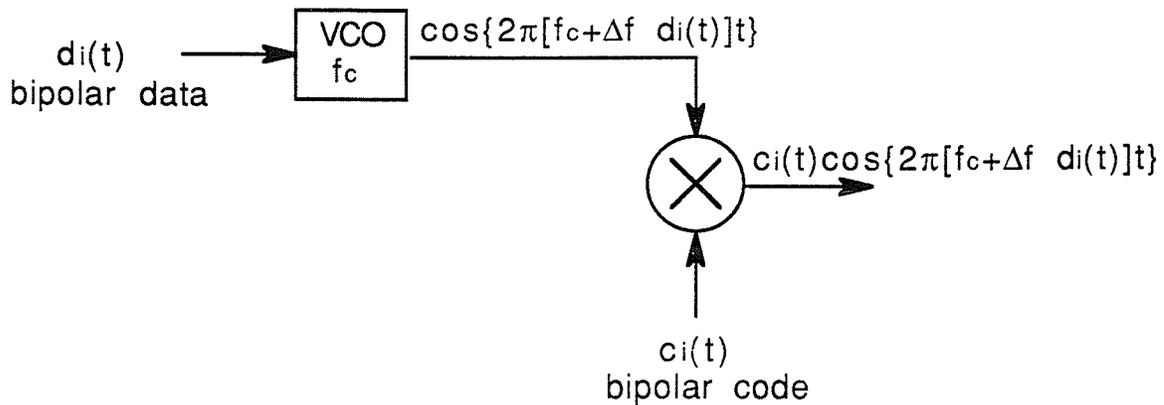


Figure 16: FSK carrier BPSK transmitter

With an equal amplitude CW interferer added to the transmitter output, the receiver input will be

$$c_i(t) \cos[2\pi [(f_c + \Delta f d_i(t)) t] + \cos(2\pi f_i t)]$$

where f_i is the interferer frequency. A typical receiver uses a coherent correlator to despread the message signal (similar to Figure 12). The output of the correlator is then

$$\cos[2\pi [f_c + \Delta f d_i(t)] t] + c_i(t) \cos(2\pi f_i t)$$

which is a despread message signal combined with a spread interferer signal as in Figure 17.

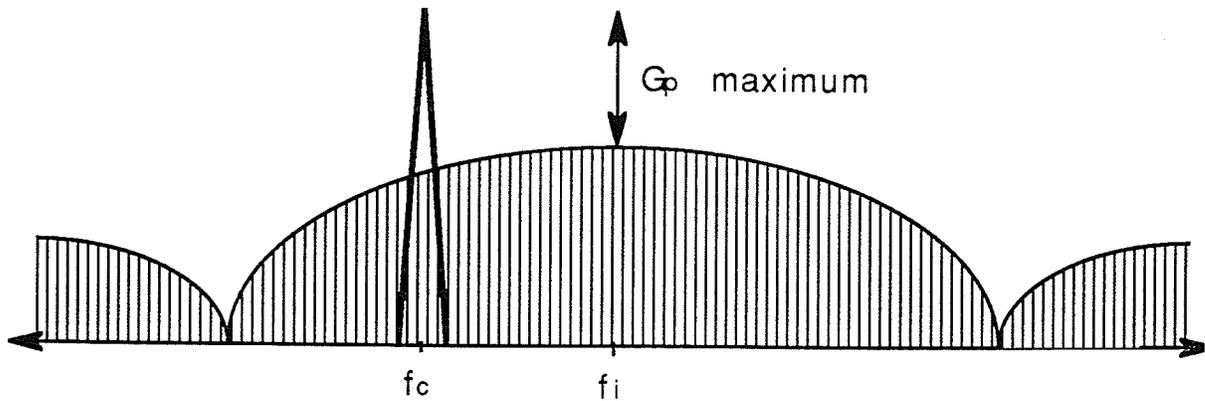


Figure 17: Coherent receiver correlator output spectrum

As Figure 17 shows, the effect of the interferer is reduced by approximately G_p for an interferer close to f_c . The receiver next filters out the despread message signal and recovers the data signal in an FSK detector.

A simple receiver that does not require a coherent replica of $c_i(t)$ uses a squaring demodulator in place of the coherent correlator. The output of the squaring circuit will be,

$$\begin{aligned}
& \{ c_i(t) \cos[2\pi (f_c + \Delta f d_i(t)) t] + A \cos(2\pi f_i t) \}^2 \\
= & \frac{1}{2} [1 + \cos[2\pi (2f_c + 2\Delta f d_i(t)) t]] + \frac{A^2}{2} [1 + \cos(2\pi 2f_i t)] \\
& + A c_i(t) \cos[2\pi (f_c + f_i + \Delta f d_i(t)) t] + A c_i(t) \cos[2\pi (f_c - f_i + \Delta f d_i(t))t]
\end{aligned}$$

where A is the relative amplitude of the interferer. The PSD of the output spectrum is plotted in Figure 18 for the frequency span of interest.

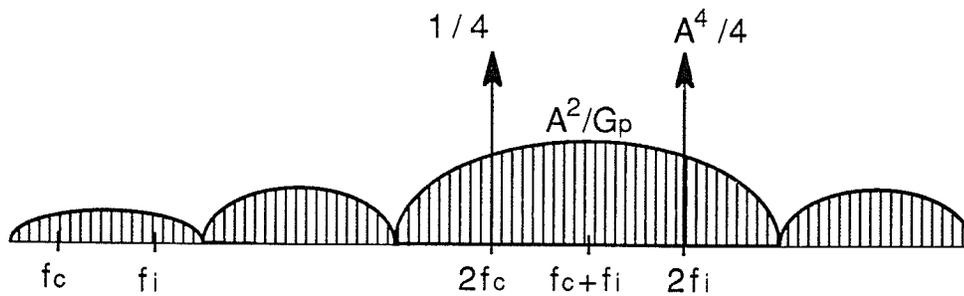


Figure 18: FSK carrier BPSK squaring receiver output

This spectrum consists of frequency components:

- $2f_c$ modulated by the data
- $2f_i$
- PSD of $c_i(t)$ centered at $f_c + f_i$, modulated by the data

The effect of the interferer is not reduced by G_p as it was for the coherent correlator. For an interferer far from the carrier frequency the new system processing gain G'_p is

$$G'_p = (1/4) / (A^2/G_p) = G_p/4A^2$$

For equal received message power and interferer power, $G'_p = G_p - 6\text{dB}$.

The interferer frequency must be sufficiently far from the carrier frequency so that the receiver IF filtering eliminates the $2f_i$ frequency component. Another drawback of this method is that the receiver must now work at $2f_c$.

3.2.3 Modulation techniques chosen

Section 3.2.1 already presented the reasons for choosing BPSK for the code modulator. Several data modulator techniques for the transmitter were presented and a comparison is given below.

The ASK carrier technique provides another possibility for a receiver which does not require a coherent code reference, but its poor signal to noise performance and susceptibility to interference rule it out as a candidate for a general purpose data link.

The transmitter for a transmitted reference type system

(Section 2.3.3) is more costly than the other methods presented since it has more stringent filtering requirements and uses two RF oscillators. A general purpose data link for applications discussed in Section 1.2 requires a very low cost transmitter as one of its most crucial components. Therefore, the transmitted reference technique will not be considered further.

Assuming filtering requirements are the same for all cases, the lowest cost transmitter implementation is the BPSK carrier or code modified technique (Figure 15). Signal-to-noise performance for BPSK is better than for the other techniques, but a coherent demodulator is required. The receiver also requires a locally generated coherent despreading code.

The many FM integrated circuits available on the market today would ease receiver design. Compared to BPSK, a lower cost and a non-coherent data demodulator is possible for FSK with only marginally worse signal-to-noise operation. FSK carrier BPSK also gives greater flexibility in demonstration system experimentation. For these reasons FSK carrier BPSK was chosen as the candidate for a low cost general usage design.

The FSK carrier technique is promising for a receiver implementation that does not require coherent code generation. However, the link is inoperable with strong interferers near the transmitter center frequency making it unreliable for a number of potential applications. The remainder of this project will therefore develop an FSK carrier BPSK direct sequence technique with a coherent correlator due to its increased performance and reliability.

3.3 LOW COST SYNCHRONIZATION AND TRACKING

Common synchronization and tracking techniques were presented in Sections 2.3 and 2.4. The synchronization and tracking techniques developed for this low cost system implementation are presented here. The synchronization technique uses a digital implementation of the sliding correlator method presented in Section 2.3. A novel tracking technique is also described which uses the synchronization detector and code clock offsets in order to retain code coherency. This method allows operation without the need for a separate tracking loop but at the expense of signal-to-noise performance.

3.3.1 Synchronization

The receiver required for a synchronization preamble technique or sequential estimation adds complexity. The receiver would need to either switch to a long code at a critical point in time, or would require a coherent BPSK demodulator for the high code rate. Both of these techniques do offer a faster synchronization time, but at reduced G_p during the acquisition process. A simple sliding correlator technique is therefore chosen for the demonstration system.

The actual sliding correlator implemented is somewhat different than described in Section 2.3.1. The method involves delaying the receiver code in discrete one bit increments instead of using a gradual slip produced by clock offsets. The circuit is shown in Section 3.5.2. This paper will refer to this delay technique as "bit jumping".

3.3.2 Tracking

The tracking method developed for this demonstration system is different than delay lock tracking in that it uses the synchronization circuit to help retain tracking. It simplifies the

design so that a separate tracking loop is not needed in addition to a synchronization loop. This benefit is of course at the cost of signal-to-noise performance. The tracking configuration is shown in Figure 19.

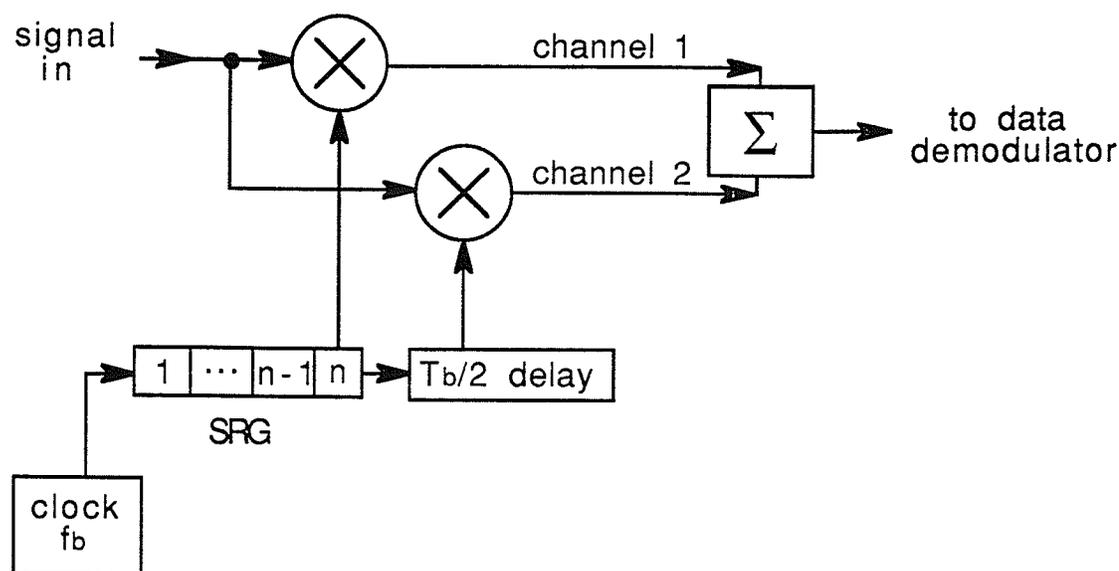


Figure 19: Demonstration system correlator

The above circuit does not actually perform a tracking function on its own. It does however despread the received signal when the receiver and received codes are synchronized to within one chip.

Figure 20 illustrates the operation over one period T_c of a $2^4-1 = 15$ chip code.

adds in phase. For a long code, 75% of the signal is correctly correlated and 25% is phase cancelled in one code period. At no time does the summed signal cancel for more than $T_b/2$. This high frequency short duration signal cancellation can effectively be removed in the data demodulator of the receiver. System signal-to-noise performance is therefore degraded by at least 25% or 1.25 dB in this position.

If the transmitter code clock is slightly slower than the receiver code clock, the relative phase between codes will eventually move to phase 2 in Figure 20d. The summed output will be the same as in phase 1. As the relative phase slips from phase 2 to phase 3, another signal component appears. The portions of time where phase cancellation occurs is followed by short durations of 180° out of phase carrier (represented by the light hatched portions - Figure 20). This has the effect of reducing correlation in the despread signal. The power spectral density of the BPSK PN code spectrum increases in relation to the coherent carrier component. System signal to noise performance cannot be better than $\approx G_p$ in this position.

The rapid increase in system noise, during movement from

phase 2 to phase 3, is monitored by the correlation detector. When phase position 3 is approached, the correlation detector circuit indicates an out of synchronization condition and causes the code to delay one chip. This returns synchronization to phase 1. Phase 1 now has a reduced system noise level and the correlation detector will indicate an in-synchronization condition.

3.4 CHARACTERIZATION OF COMMUNICATION CHANNEL

The spread spectrum system designed in this project is meant to achieve the lowest practical cost and to remain applicable to a wide range of uses. Some proposed applications for the system are described in Section 1.2. The system will provide modest data rates, operation in the 902-928 MHz band, up to 1 watt of output power, some degree of detectability reduction and resistance to interference and multipath effects.

The receiver synchronization time must be held low for use in short data packet applications while at the same time providing a reasonable level of multipath and interference suppression. Both of these opposing characteristics must be obtained and implemented in a low cost data link. In order to achieve this, a relatively short

spreading code of 255 chips is used as a trade off. The specifics of the design are given in Section 3.5. Here it suffices to say that the link provides 2kbps data rate, 32ms synchronization time, and a processing gain of 24 dB.

a) Interference rejection

Since the RF channel is an unlicensed shared portion of spectrum, this spread spectrum system must provide some level of interference rejection. The specific amount of interference rejection required for a particular application depends upon the anticipated signal strength of an interferer at the receiver. The effect of an interferer is reduced in the receiver by an amount equal to the system processing gain which is about 24 dB for this system. This does not mean that the link will operate with an interferer signal strength 24dB higher than the desired signal, but rather that the interference signal is reduced relative to the desired signal by 24 dB. Section 3.6 gives a measurement of the system's interference rejection capability. This level of interference suppression capability will comfortably work in an environment with equal output power interferers (positioned a similar distance from the receiver as the transmitter) and there will still be margin for a fading channel.

b) Secrecy

Referring to Section 2.2.3 it can be seen that the normalized PSD of the transmitter output has peak spectral components of amplitude $(N+1)/N^2$ or -24dB for this system. Thus, the signal is less detectable to an observer, especially when it is desired to conceal operation of the transmitter as with stolen vehicle recovery systems (Section 1.2b).

c) Multiple access

The use of an 8 bit L.M. spreading code gives the ability to set up a network with 16 different codes (Table 1). The receiver could potentially distinguish between 16 different transmitters operating at the same frequency. High cross correlation between pairs of the 16 code set can also reduce the index of discrimination substantially causing the synchronization detector to miss or falsely detect synchronization. (See Section 2.2.2). Cross correlation between all pairs of the 16 code set could be investigated and codes showing poor cross correlation properties removed from the set. However, the relatively short 255 chip code does not allow significant distinction between any pairs of codes. Longer codes provide greater

distinction between each other and are thus more suited to a code division multiple access approach. For these reasons, it is advisable that a multiple user application such as a data communications network rely on separation by frequency, by address or by time.

d) Multipath rejection

Indoor office environments are characterized by a Rayleigh-fading multipath channel and a signal strength that decays with distance as approximately d^{-4} [21]. Scattering and reflection of electromagnetic waves occur due to the various rooms, objects and people inside the building. Reflected waves from various surfaces arrive at the receiver at different points in time causing multipath fading and multipath distortion.

The multipath fading is due to equal amplitude signals arriving at the receiver antenna out of phase and cancelling each other. This effect can be substantially reduced by using antenna diversity [22].

The multipath distortion is due to a delayed signal arriving at the receiver and adding in phase with the direct path signal. This makes the phase transition point ambiguous for a phase modulated signal [23]. The spread spectrum system described in this paper is relatively immune to this type of interference. This spread spectrum

system uses a code rate of 10^6 chips per second, and a signal delay of one chip length corresponds to $1 \mu\text{s}$. A signal with large delay (greater than one chip) must travel a path which is

$3 \times 10^8 \text{ metres/second} \times 10^{-6} \text{ seconds} = 300 \text{ metres}$ longer than that of the direct path signal. At an attenuation factor of d^{-4} , the delayed signal is attenuated 100 dB more than the direct signal. In addition, the receiver correlator reduces the influence of a code delayed more than one chip by an amount equal to the system processing gain. For a signal delay of $0.1 \mu\text{s}$ (10% of a chip) the path length difference is 30 metres and the signal strength is still 60 dB less than a direct signal. In addition, the code tracking technique used in the receiver (Section 3.3.2) uses a delayed code correlator which can tolerate code phase variations of $\pm 1/2$ chip. Figure 25 (Section 3.6.2) shows that a worst case phase variation of $\pm 1/2$ chip adds only a 20% AM component to the correlator output which is then further reduced in the IF limiting amplifier. The smaller phase variations will produce an even less significant effect. Turin [24] further investigates suppression of multipath effects with the use of spread spectrum.

3.5 CIRCUIT DESCRIPTION

This section will restate the techniques used for the selected spread spectrum system, and present the system properties for the prototype receiver and transmitter. The bench setup will be detailed and the transmitter and receiver circuits that were designed will be presented. Parts used for the RF, analog and digital sections are included. A system cost estimate for a transmitter/receiver link (in small quantities) is given.

The previous sections presented general system issues in spread spectrum link design and discussed the reasons behind choosing the particular configuration. The system arrived at is FSK modulated carrier with direct sequence BPSK spreading. The receiver uses a bit jumping routine to implement a sliding correlator for initial synchronization. A two channel delayed code technique was developed to be used in conjunction with the bit jumping routine to perform code tracking. The other system properties chosen for the demonstration system are as follows:

PN code → 8 bit linear maximal shift register generator, 1 Mbps
chip rate

Code Period $T_c \rightarrow (1 \times 10^6)/(2^8-1) = 3.92 \text{ kHz} = \text{spectral line spacing}$
of code PSD function

RF bandwidth \rightarrow null to null = 2 MHz, 3dB bandwidth $\approx 1 \text{ MHz}$

Data modulation $\rightarrow 2 \text{ kbps}$, 1 kHz deviation, 3dB bandwidth $\approx 4 \text{ kHz}$

Processing Gain $G_p \rightarrow$ defined as $BW_{RF}/BW_{data} = 1 \times 10^6/4 \times 10^3 \rightarrow$
24 dB

The system was set up on a test bench with a 900 MHz transmitter center frequency. Department of Communications regulations on transmitter operation and spurious output had to be adhered to, so a coaxial line was used for the RF channel. This allowed setting up the system without a transmitter power amplifier or output filter, and no receiver input filter (no external interference introduced into the system). The system parts cost worked out in Section 3.5.3 takes the above factors into consideration, and cost of components required for a real world environment is included in the cost summary. Circuit schematics and discussion however only show the actual bench setup.

3.5.1 Transmitter

The transmitter block diagram is shown in Figure 21.

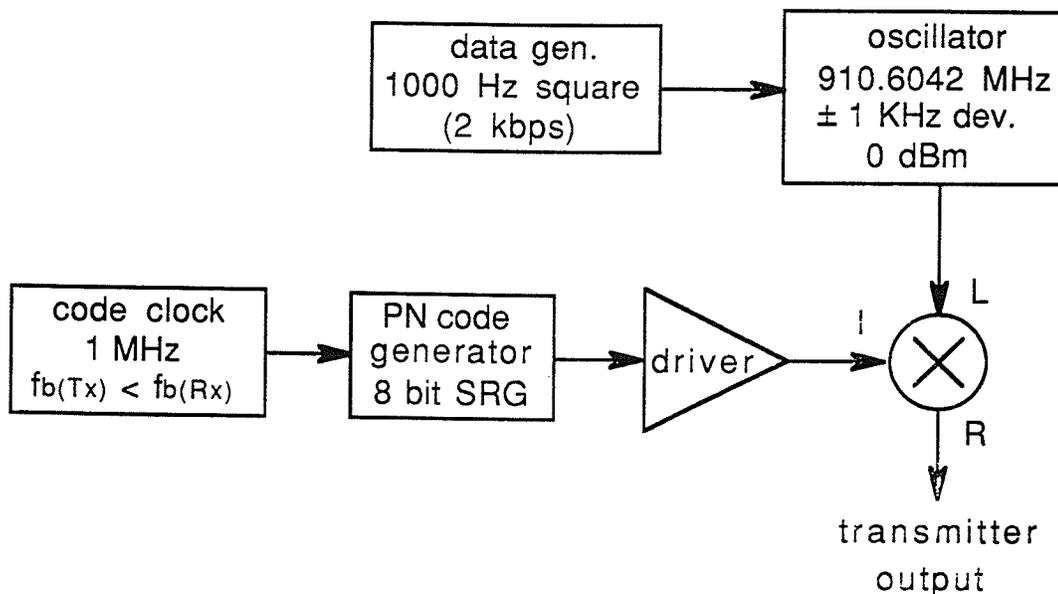


Figure 21: Transmitter block diagram

The transmitter is simply a conventional FM transmitter whose output is modulated by a PN code through a double balanced mixer. The output of Figure 21 would require a filter and power amplifier for actual transmitter operation. The actual circuit schematics will not be presented here since all functional blocks are repeated at the receiver. The clock, code generator, driver and mixer circuits can be extracted from the receiver schematics.

As noted in Figure 21, the transmitter code clock runs slightly

slower than the receiver code clock. This is a requirement for proper operation of the synchronization and tracking circuits of the receiver. A typical crystal oscillator specification is less than ± 15 ppm over 10°C for one year. Transmitter and receiver clocks must therefore be offset a minimum of $30\text{ppm} \times 1 \text{ Mbps} = 30 \text{ Hz}$ from each other to ensure the transmitter clock always runs slower than the receiver clock.

3.5.2 Receiver

The receiver block diagram is shown in Figure 22. The receiver has been broken down into RF, analog, and digital sections as shown. The receiver uses a conventional dual conversion limiter discriminator FM receiver circuit with an RF despreading front end as described in Section 3.3.2. The input to Figure 22 would require an input filter and post correlation filter for operation in an uncontrolled noisy environment.

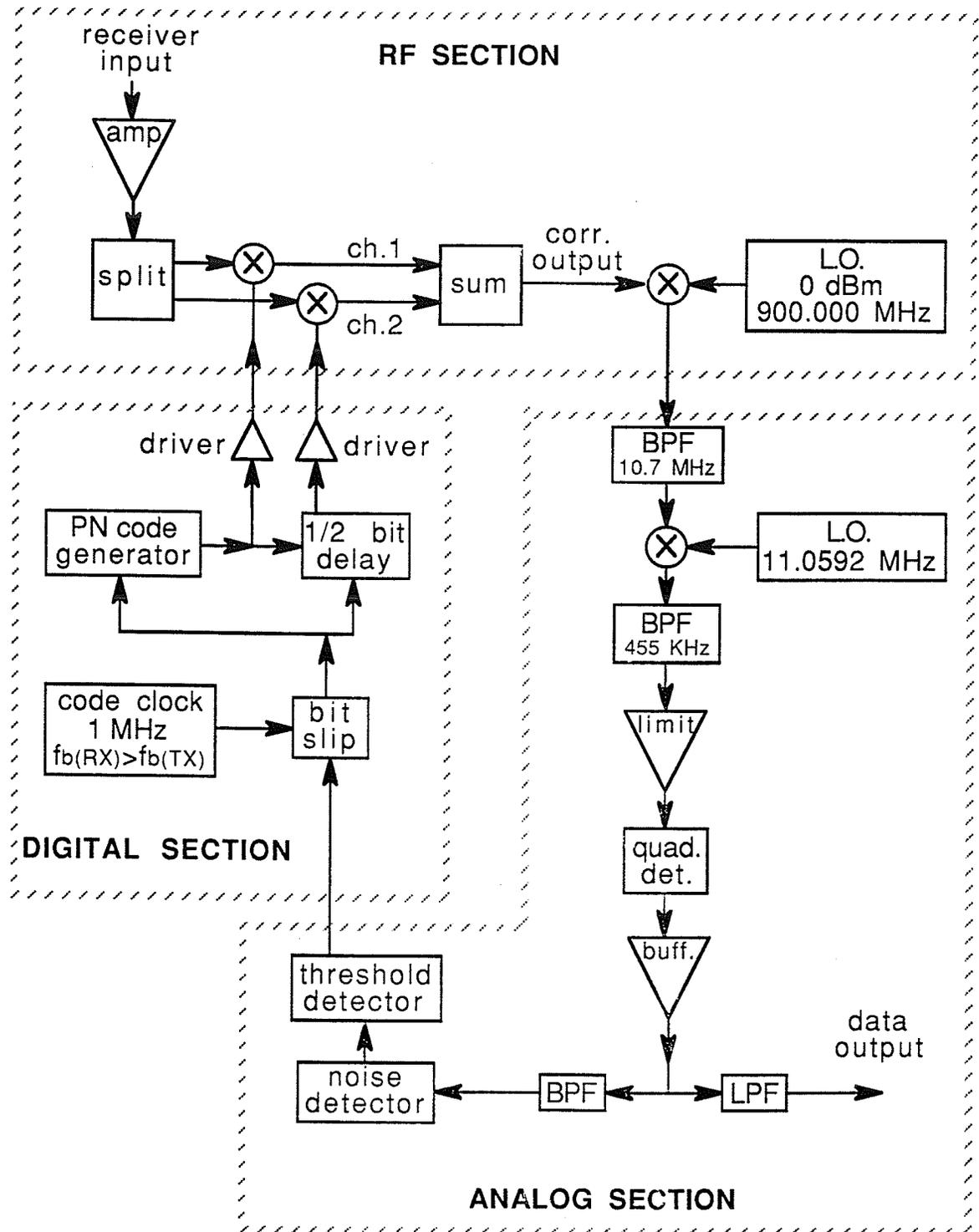


Figure 22: Receiver block diagram

Section 3.5.1 already mentioned the fact that the receiver code clock must run faster than the transmitter code clock. The effect of the bit jumping routine in the receiver tracking circuit is that the carrier output from the correlator is amplitude modulated at the rate $f_b(\text{RX}) - f_b(\text{TX})$. This is shown later in Section 3.6.2, Figure 25. Since the data modulation is FSK, the detected data is relatively immune to this AM component. The other effect of the bit jumping/tracking routine is that system noise level increases. Measurements showing the noise level change are also documented in Section 3.6.2.

3.5.2 a) RF section description

The receiver RF section schematic is shown in Figure 22. Data sheets for the parts used are included in Appendix C.

Referring to Figure 22, the receiver RF section consists of three doubled balanced mixers, two power dividers (combiners), one preamplifier and a 900.000 MHz oscillator source. The RF section of the receiver makes possible the code tracking method described in Section 3.3.2, and then downconverts the correlated signal to the first IF of 10.7 MHz.

3.5.2 b) Analog section description

The circuit schematic and data sheets for the analog section shown in Figure 22 can be found in Appendix C. The analog section consists of a narrowband FM single conversion receiver and correlator synchronization detection circuitry.

The receiver downconverts the 10.7 MHz output from the correlator to a second IF of 455 kHz. The second IF is then passed through a limiting amplifier and then to a phase quadrature multiplier that demodulates the data signal. The FM receiver circuit that performs these functions consists of a common 16 pin IC, an 11.0592 MHz crystal, two ceramic filters, a tunable inductor and various resistors and capacitors. The data output is 0.6 volts peak to peak with the stated data input of 2000 bps, 1 kHz deviation and a 10.7 MHz carrier frequency. Sensitivity is $7\mu\text{V}$ for 12dB Sinad.

The synchronization detector circuit is made up of an active band pass filter using an on chip op-amp, a rectified envelope detector circuit using an external op-amp, and an on chip comparator. The limiting amplifier of the receiver IC references output signal components relative to the carrier level (or other strongest frequency component). A bandpass filter passes the high

frequency (out of data band) components of the limited signal. A noise level detection circuit measures this out of band noise and drives a Schmitt trigger which indicates an in synchronization or out of synchronization condition. A variable potentiometer is used to set the Schmitt trigger threshold.

3.5.2 c) Digital section description

The circuit schematics and data sheets for the digital section of Figure 22 can be found in Appendix C. The digital section consists of an eight bit code generator, a half bit delay circuit, output drivers for the two receiver channels, and a clock cycle disable circuit (bit slip).

The linear maximal PN code generator is made up of a 1 MHz clock and two digital ICs. The clock is a 1 MHz digital output crystal oscillator module that is pulled to run faster than the transmitter clock. The generator uses an eight-bit serial in/parallel out digital shift register and three dual input exclusive-OR gates used as linear feedback elements. The code used is [8,4,3,2] or $1+x^2+x^3+x^4+x^8$ (see Section 2.2.1).

The half bit delay circuit is simply an inverter and a D flip flop. The flip flop advances the shift register output one code bit on the

rising clock edge after its input is set. Therefore, inverting the clock input effectively delays the sequence by half a bit.

The output drivers are used to drive the channel one and two 50 ohm inputs to the RF section. Each driver is made up of four transistors configured in a manner to reduce deadband crossover effects.

The clock cycle disable circuit consists of a binary ripple counter, a D flip flop, and three inverters. This bit slip circuit performs synchronization acquisition of the sliding correlator, and assists in the code tracking function. The counter sets the integration period for the synchronization detector circuit which is 255 μs for one code period. Once the counter reaches a count of 256 μs it disables one single clock cycle and starts its count again. This missed clock cycle delays the receiver generated code by one chip with respect to the transmitter generated code. Once the synchronization detector circuit indicates a synchronized condition, the counter is reset and it cannot disable any more clock pulses. When the fast running receiver clock advances its code one chip with respect to the synchronized position, the synchronization detector circuit indicates loss of synchronization. The counter again disables one clock pulse to

keep the receiver code tracking the transmitter code.

3.5.3 System parts cost

The parts cost shown in this section is based on the preceding system setup shown in Figures 21 and 22 and in Appendix C. As stated earlier, the transmitter and receiver were implemented for test bench operation using coaxial cable as the transmission medium in order to meet emissions regulations and using connectorized components for ease and flexibility of configuration. In order to use this system as a real radio link, some changes to the test bench setup would be required. The reasons for the changes that would be required are discussed below.

Transmitter

A similar performance surface mount double balanced mixer is substituted (in Appendix C) for the connectorized version used during testing. A RF power amplifier and filter are also included for the transmitter output stage to extend the radio link range and to ensure compliance with radiated emissions regulations.

Receiver

Additions to the schematics included in Appendix E are an input

filter and a post correlation filter. The correlator mixers and down converter included in the pricing are surface mount versions similar in performance to the connectorized versions used during testing. Cost of the power splitters/combiners in the RF section is assumed to be negligible since the circuits can easily be included on a printed circuit board as part of the surface mount mixer feed. It can also function as a post correlator band pass filter.

This parts cost summary therefore includes the non-connectorized components, filters and amplifier that would be required for a real radio link setup. The specific devices are shown in Appendix D along with the price of each.

Pricing used in Appendix D is the cost of small quantities of the components (less than 10) through Canadian distributors. The only exceptions are the helical and ceramic filters. Pricing on these components is taken from U.S. distributors with a currency exchange rate applied. In most cases, prices stated are those paid by the author. Some of the parts however were obtained as samples. Cost of resistors, capacitors and circuit boards are not included.

From Appendix D:

Total transmitter parts cost is \$ 62.71

Total receiver parts cost is \$ 112.70

A combined transmitter/receiver module could be implemented as a half-duplex system where the local oscillator, 1 MHz clock module, and frequency converter of the receiver could also be used for the transmit function. The combined parts cost would be approximately:

	Receiver	\$ 112.70
	Transmitter	62.71
less	L.O.	- 30.33
less	Clock	- 9.24
less	Frequency Converter	<u>- 11.12</u>
		\$ 124.72

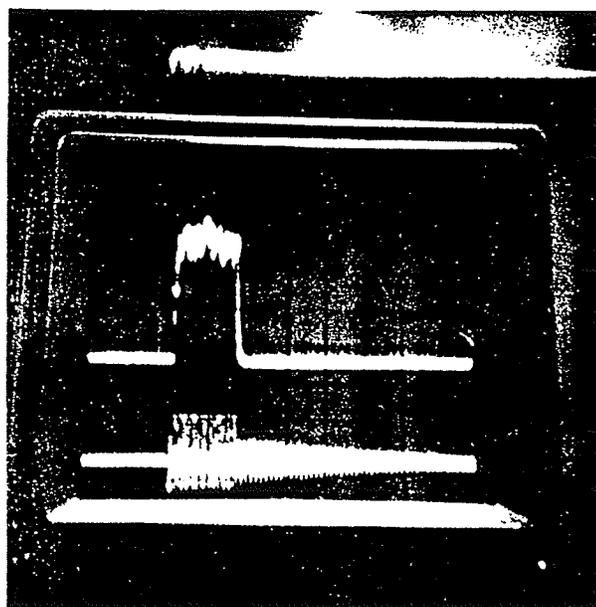
Large volume purchase of components would significantly reduce these amounts further. Ordering parts in quantities of only 100 pieces would bring the combined cost below \$100.

3.6 SYSTEM PERFORMANCE MEASUREMENTS

This section will present some system performance measurements and describe some operational limitations. The topics discussed are receiver lock time, receiver tracking performance and system operational performance with and without CW interference.

3.6.1 Lock time

Synchronization acquisition time was discussed in Section 2.3.1. The bit jumping synchronization technique used for this paper (Section 3.3.1) is a discretely stepped sliding correlator. For this system, the minimum worst case synchronization time is $T_{\text{sync}} = T_c \times N$. This is assuming the correlation detector takes full advantage of the available index of discrimination (integrates over an entire code) and that it must check all N phase positions before synchronization is found. Reducing the integration period of each phase state reduces the discrimination between synchronized and unsynchronized conditions, but also reduces T_{sync} . It was found that the system acquired synchronization quite reliably with the integration period reduced to $T_c/2$ (actually $128\mu\text{s}$ was used). Figure 23 illustrates a T_{sync} measurement.



a b

20ms/div.

$$\text{lock time} = 128\mu\text{s} \times 255 \text{ positions} = 32.64 \text{ ms}$$

Figure 23: Synchronization time measurement

This worst case synchronization time is simulated by operating the receiver clock slower than the transmitter clock; thus forcing loss of synchronization (point a in Figure 23). Since the synchronization routine further delays the receiver code to obtain synchronization, all N phase positions must be tried before synchronization is regained (point b). The top trace in the figure is the unfiltered data output line, and the bottom trace is the noise detector circuit input (pin 11 of U1 on the analog section - Appendix C). No data modulation was

used for this photograph. Figure 23 shows the synchronization time of 32.64 ms.

3.6.2 Tracking

The synchronization tracking technique used was discussed in Section 3.3.2. Figure 24 illustrates the operation described in Figure 20.

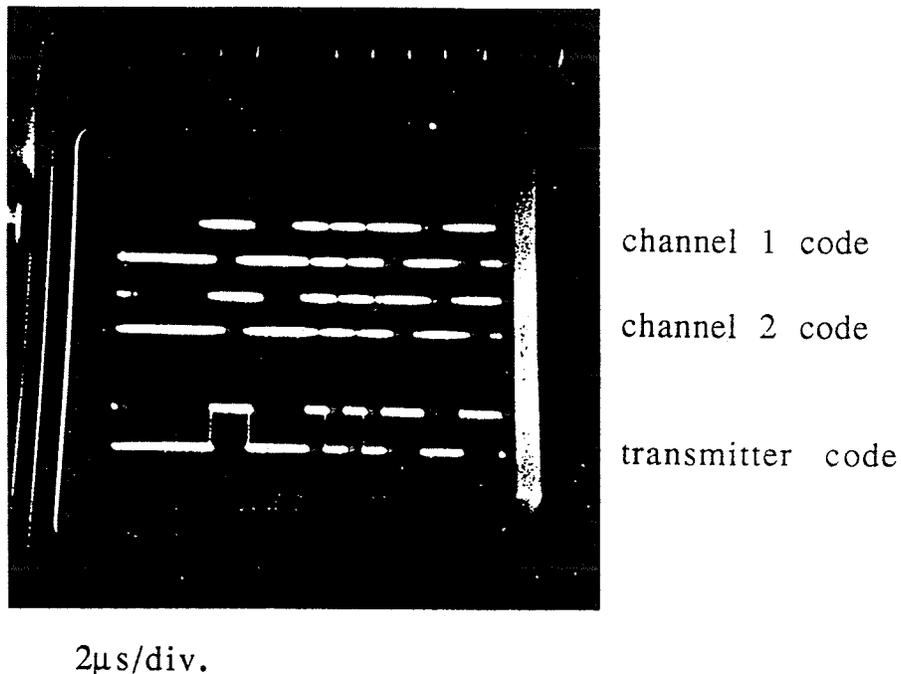
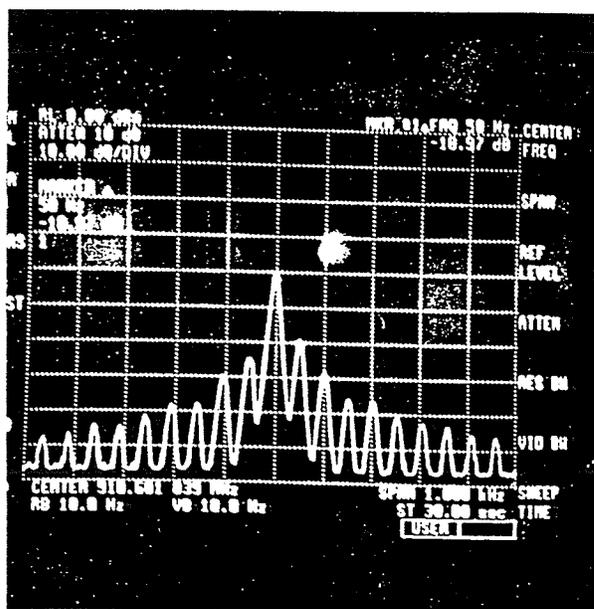


Figure 24: Receiver code tracking

It shows the phase tracking of the two receiver channels with respect to the transmitter signal. The relative phase slips due to the offset between the transmitter and receiver clocks, and then jumps

back using the bit jumping routine to retain synchronization.

Section 3.5.2 described system operation with respect to transmitter and receiver clock offset. The despread correlator output ends up being amplitude modulated due to the tracking technique. Figure 25 shows the correlator output in synchronized condition with a 50 ppm clock offset. The despread carrier is found to be amplitude modulated by about 20% at the frequency $f_{b(RX)} - f_{b(TX)} = 50\text{Hz}$.

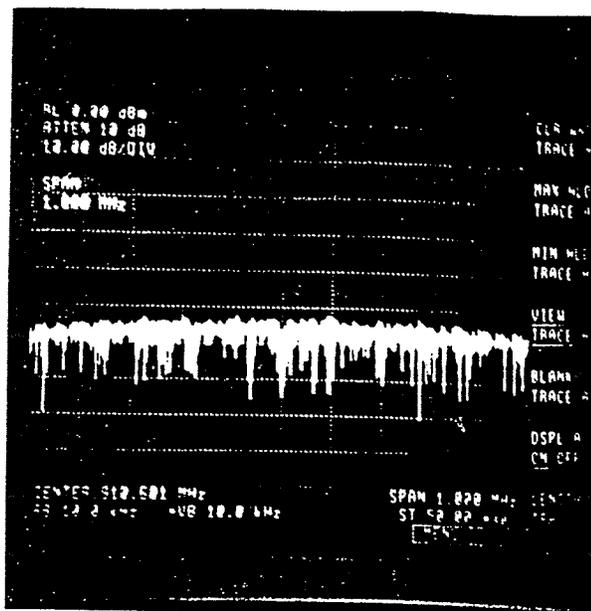


$f_c = 910.6 \text{ MHz}$
 span = 1 kHz
 meas. filter = 10 Hz
 10 dB/div.

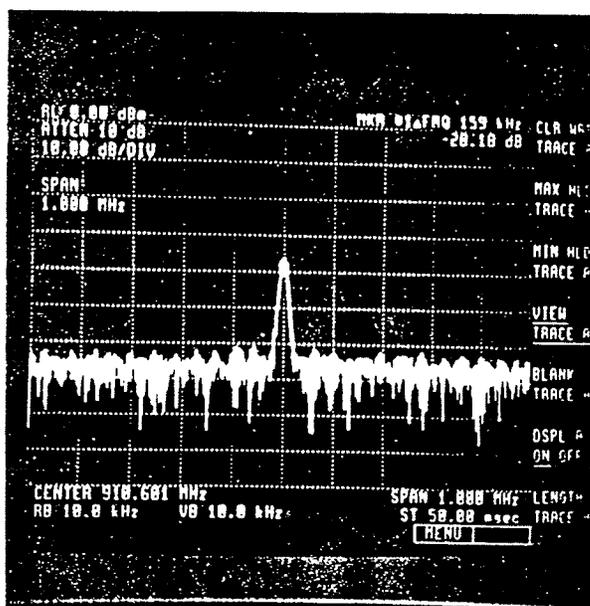
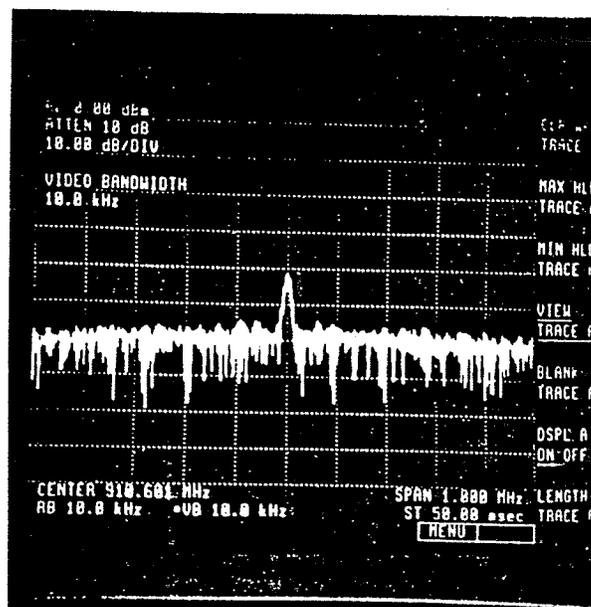
bit tracking effect at 50 Hz clock offset

Figure 25: Correlator output spectrum (unmodulated)

Besides the amplitude modulation effect described above, the synchronization tracking technique causes the level of correlation to change. Correlation is high when in phase position 1 and 2 (Figure 20) and lower when in phase position 3. Figure 26 shows the output of the correlator at different transmitter/receiver code phase positions. Figure 26a shows the output spectrum for the uncorrelated condition that occurs before initial synchronization. Figure 26b shows the spectrum for phase position 1 and 2. Figure 26c shows the spectrum for phase position 3. The photographs illustrate the type of signal differences that the synchronization detector circuit "watches" for. During initial synchronization the data carrier pops up out of the background "noise". During phase tracking, the background noise level rises in relation to the carrier level. It should be pointed out that since the filter bandwidth for spectrum measurements was 10 kHz, the background noise appears higher in the photographs than it actually is.



a) unsynchronized

b) best tracking condition
(position 1 and 2)c) worst tracking condition
(position 3)

$f_c = 910.6 \text{ MHz}$
 span = 1 MHz
 meas. filter = 10 kHz
 10 dB/div.

Figure 26: Correlator output spectrum

3.6.3 Operational performance

System performance was measured using a SINAD test. SINAD is the ratio of signal, noise and distortion voltage to noise and distortion voltage expressed in dB. A CW interferer was injected into the channel, 500 kHz offset from transmitter center frequency, at a level of 10 dB above transmitter total output power of 10 μ W. SINAD measurements of 19 dB and 17 dB were obtained with the relative transmitter/receiver code in phase position 1 (Figure 26b) and phase position 3 (Figure 26c) respectively. The codes were externally held at the stated phase positions to perform the measurement. At 100 Hz transmitter/receiver clock offset (100 ppm) the SINAD measurement drops to 16.5 dB.

The analog card narrowband FM receiver circuit is characterized in order to evaluate its influence on system performance. Input signal for the test setup is a 1 kHz sinewave, giving 1 kHz FM deviation of a carrier at frequency 10.6042 MHz.

Receiver sensitivity is -90 dBm for 12 dB SINAD

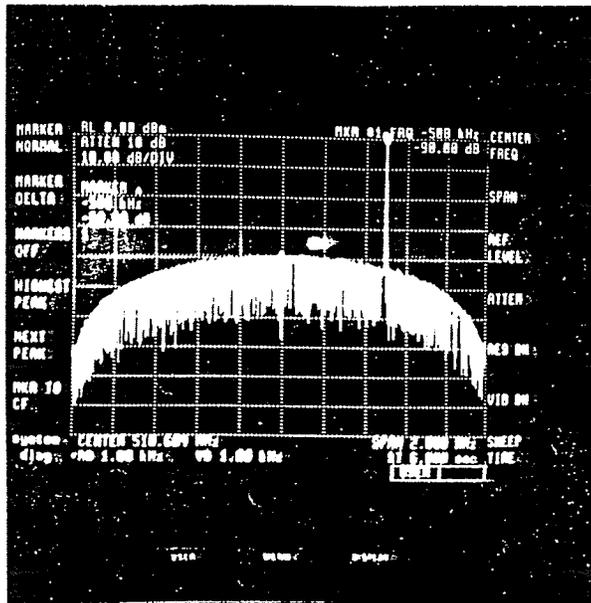
60 dB IF bandwidth is 8.4 kHz

6 dB noise detector filter bandwidth \rightarrow passes 2 kHz to 11 kHz

The entire spread spectrum receiver sensitivity is -100 dBm

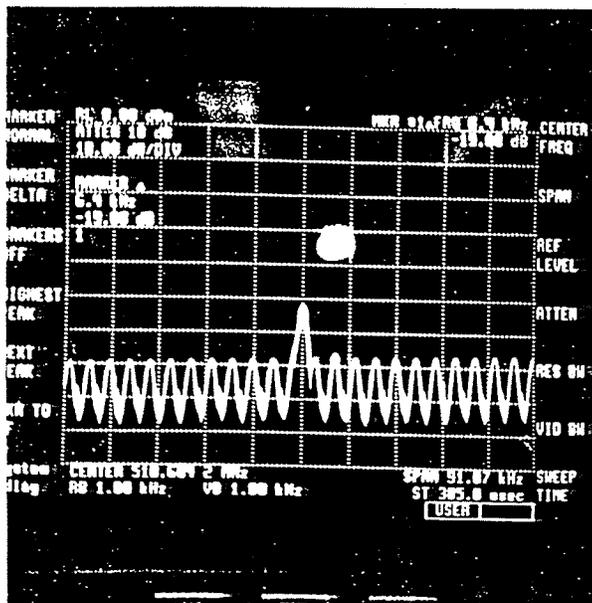
for 12 dB SINAD (with no interferers).

A measurement showing interference suppression capability is documented as follows: The CW interferer power is 16 dB above total transmitter power of $25\mu\text{W}$ for a 12 dB SINAD measurement at the receiver. The receiver input signal is shown in Figure 27a. The spectrum measurement filter is 1 kHz wide to show the actual level of the transmitter spectral components. Figure 27b shows the correlated signal output with carrier modulation turned off to resolve the residual code spectral components. This residual "noise" is made up of the interferer power spread by the receiver's correlator (discussed in Section 3.2.2c).



a) receiver input spectrum
2 MHz span

$f_c = 910.6$ MHz
reference level = 0 dBm
meas. filter = 1 kHz
10 dB/div.



b) correlator output spectrum
90 kHz span

Figure 27: Interference suppression

4. CONCLUSION

In conclusion of this project, this chapter will discuss some design improvements for optimizing the system, as well as point out some of the operational deficiencies at the time of writing. The topics discussed relate to filtering, synchronization and tracking. Also discussed are further design possibilities for operation at higher data rates, and operation without the need for stable RF oscillators at the transmitter and receiver.

4.1 SYSTEM EVALUATION

4.1.1 Synchronization

The bit jumping technique used to implement the sliding correlator maintains high system processing gain during synchronization acquisition. However, this acquisition technique is relatively slow. The worst case ideal synchronization time was shown in Section 3.6.1 to be about 30 ms. In order to obtain 90% time efficiency in a packet data environment, 300 ms packets are required. This may or may not be acceptable for the particular application.

The portion of this spread spectrum system requiring the most optimization is the synchronization detector circuit. The probability of false synchronization detection decreases if the detector filter response time is increased. An increased response time however increases the probability of the detector missing a synchronization event. Increased response time can also dictate a longer synchronization detector integration period, and thus a longer synchronization time. The tradeoff between the probabilities of false alarm and of missed synchronization, and synchronization time can be alleviated by the use of a bank of detector filters, each with a different response time. This technique is commonly referred to as a multiple dwell detector [4]. Each filter has a progressively longer response time. This is used to decrease the probability of false alarm while the first fast filter holds the probability of missed synchronization low and the synchronization time low.

The type of synchronization detector filter(s) and the integration time must be optimized as well as traded off with the probabilities of false alarm and of missed synchronization for each particular application.

4.1.2 Tracking

The following discussion of the code tracking technique developed for the spread spectrum receiver relates to optimization and implementation cost benefits.

In this system design the code tracking performance is tied closely to the synchronization detector circuitry which also detects loss of synchronization. The bit jumping hardware is set up so that the loss of synchronization threshold must be exceeded over the entire synchronization detector integration period in order for the code to slip one bit. This effectively sets the synchronization loss detector response time. Probability of false detection and probability of missed detection of synchronization loss are traded off by adjusting detector response time. This is analogous to the initial synchronization tradeoffs presented in the last section. However, missing a synchronization loss detection is not as detrimental to system performance as missing initial synchronization detection. Missing synchronization loss degrades receiver signal to noise performance for one integration period ($128 \mu\text{s}$) while missing initial synchronization requires an additional $128 \mu\text{s} \times 255 \text{ bits} = 33 \text{ ms}$ to obtain synchronization. By adding separate integration time and filter response circuits for the tracking function, probability of false

and missed synchronization loss can be optimized separately from probability of false and missed initial synchronization. When tracking, integration time and filter response for the tracking function would take over from the synchronization circuits once initial synchronization is achieved.

This system delays the receiver code exactly one chip for every bit jump interval. System noise performance can be greatly improved by reducing the code delay to less than one chip. Referring to Figure 20, the receiver correlation level drops off rapidly from phase position 2 to phase position 3, but remains constant between phase position 1 and 2. However, reducing the code delay to a value less than one chip increases synchronization time and reduces the probability of detecting synchronization loss. The solution is to use a better synchronization loss detection circuit.

The cost benefit for using this tracking technique rather than a conventional delay lock loop is one less RF channel and two less RF processing circuits, at the expense of stable code rate clocks at the transmitter and receiver. This relates to approximately a 20% saving in parts cost over a delay lock loop. Design time for the delay lock tracking technique is also substantially greater but results in better

system performance if properly designed.

4.2 FUTURE WORK

4.2.1 Higher data rates

The system was designed to work at a low data rate of 2000 bps. Many potential applications (e.g. personal computer modems) would be more attractive with substantially higher data rates. The major system design changes to accommodate a higher data rate and maintain a similar processing gain are IF bandwidth, code rate and code length.

The IF bandwidth requirement increases with increasing data rate for a given modulation. Using a more spectrally efficient modulation scheme allows a higher data rate with the same bandwidth, but will require a more complex data modulator and demodulator.

System processing gain is determined in part by the IF bandwidth. G_p was defined earlier in Section 1.1 for a typical spread spectrum system as $G_p = BW_{RF}/BW_{data}$. For a short code length spread spectrum system, the processing gain is limited, however. A CW interferer signal is spread in the receiver to give a power

spectral density with spectral peaks reduced by approximately $10 \log N$ dB (actually $10 \log [N+1/N^2]$ dB as shown in Section 2.2.3) below its received level. The number of these components in the data bandwidth determines the interferer power in the data bandwidth. For this reason, processing gain can be more accurately expressed as $G_p = N/(\text{number of spectral components in the data bandwidth})$. Maximizing G_p therefore means holding the spacing between code spectral lines equal to the data bandwidth for a short code length system. Code rate and length are determined therefore by the data rate requirements to hold G_p to its maximum value of $10 \log N$ dB.

4.2.2 Stable carrier

The spread spectrum system described in this paper requires stable oscillators for the transmitter and receiver, since the post correlation circuit uses a narrowband quadrature FM detector. The major area of future investigation for this project is to further reduce system cost by relaxing the stable oscillator requirement.

Replacing the narrowband FM receiver with a phase locked loop type receiver would allow operation with a less stable oscillator.

A simple FM click detection circuit could easily be added to the phase locked loop to give an accurate measure of receiver S/N ratio [20]. Synchronization detector integration period could also be easily set. As well, this circuit could be used for improved synchronization and tracking functions.

4.3 SUMMARY

Federal Communications Commission (FCC) rulings now allow commercial applications of spread spectrum radio links. This makes possible the use of radio equipment on unlicensed channels with up to 1 watt output power, high data rates and loose carrier stability requirements, thus opening the way for many low cost, relatively unregulated radio link applications.

The general principle of operation for direct sequence and frequency hopping systems has been shown, and a direct sequence system was found to be the most attractive candidate for a low cost implementation. Several transmitter and receiver configurations were presented and an FSK carrier BPSK direct sequence system was chosen for implementation in order to demonstrate operation of such a system. It uses a discretely stepped sliding correlator to obtain

initial synchronization and a two channel delayed code technique to perform code tracking. Circuit descriptions and schematics are given for transmitter and receiver functional blocks. The parts cost for small quantities of a transmitter/receiver module is found to be less than \$100. The demonstration system uses an 8-bit code generator, 1 Mbps spreading code and a 2 kbps data rate. The link is capable of 12 dB SINAD performance with a 16 dBc CW interferer.

The areas of operational enhancements for the demonstration system include better synchronization detection and synchronization loss detection circuitry, operation at higher data rates, and operation with a less stable carrier frequency.

APPENDIX A

Shift register generator feedback connections for
linear maximal PN codes (from [2])

Number of Stages	Code Length	Maximal Taps
2 ^a	3	[2, 1]
3 ^a	7	[3, 1]
4	15	[4, 1]
5 ^a	31	[5, 2] [5, 4, 3, 2] [5, 4, 2, 1]
6	63	[6, 1] [6, 5, 2, 1] [6, 5, 3, 2]
7 ^a	127	[7, 1] [7, 3] [7, 3, 2, 1] [7, 4, 3, 2] [7, 6, 4, 2] [7, 6, 3, 1] [7, 6, 5, 2] [7, 6, 5, 4, 2, 1] [7, 5, 4, 3, 2, 1]
8	255	[8, 4, 3, 2] [8, 6, 5, 3] [8, 6, 5, 2] [8, 5, 3, 1] [8, 6, 5, 1] [8, 7, 6, 1] [8, 7, 6, 5, 2, 1] [8, 6, 4, 3, 2, 1]
9	511	[9, 4] [9, 6, 4, 3] [9, 8, 5, 4] [9, 8, 4, 1] [9, 5, 3, 2] [9, 8, 6, 5] [9, 8, 7, 2] [9, 6, 5, 4, 2, 1] [9, 7, 6, 4, 3, 1] [9, 8, 7, 6, 5, 3]
10	1023	[10, 3] [10, 8, 3, 2] [10, 4, 3, 1] [10, 8, 5, 1] [10, 8, 5, 4] [10, 9, 4, 1] [10, 8, 4, 3] [10, 5, 3, 2] [10, 5, 2, 1] [10, 9, 4, 2]
11	2047	[11, 1] [11, 8, 5, 2] [11, 7, 3, 2] [11, 5, 3, 5] [11, 10, 3, 2] [11, 6, 5, 1] [11, 5, 3, 1] [11, 9, 4, 1] [11, 8, 6, 2] [11, 9, 8, 3]
12	4095	[12, 6, 4, 1] [12, 9, 3, 2] [12, 11, 10, 5, 2, 1] [12, 11, 6, 4, 2, 1] [12, 11, 9, 7, 6, 5] [12, 11, 9, 5, 3, 1] [12, 11, 9, 8, 7, 4] [12, 11, 9, 7, 6, 5] [12, 9, 8, 3, 2, 1] [12, 10, 9, 8, 6, 2]
13 ^a	8191	[13, 4, 3, 1] [13, 10, 9, 7, 5, 4] [13, 11, 8, 7, 4, 1] [13, 12, 8, 7, 6, 5] [13, 9, 8, 7, 5, 1] [13, 12, 6, 5, 4, 3] [13, 12, 11, 9, 5, 3] [13, 12, 11, 5, 2, 1] [13, 12, 9, 8, 4, 2] [13, 8, 7, 4, 3, 2]
14	16, 383	[14, 12, 2, 1] [14, 13, 4, 2] [14, 13, 11, 9] [14, 10, 6, 1] [14, 11, 6, 1] [14, 12, 11, 1] [14, 6, 4, 2] [14, 11, 9, 6, 5, 2] [14, 13, 6, 5, 3, 1] [14, 13, 12, 8, 4, 1] [14, 8, 7, 6, 4, 2] [14, 10, 6, 5, 4, 1] [14, 13, 12, 7, 6, 3] [14, 13, 11, 10, 8, 3]
15	32, 767	[15, 13, 10, 9] [15, 13, 10, 1] [15, 14, 9, 2] [15, 1] [15, 9, 4, 1] [15, 12, 3, 1] [15, 10, 5, 4] [15, 10, 5, 4, 3, 2] [15, 11, 7, 6, 2, 1] [15, 7, 6, 3, 2, 1] [15, 10, 9, 8, 5, 3] [15, 12, 5, 4, 3, 2] [15, 10, 9, 7, 5, 3] [15, 13, 12, 10] [15, 13, 10, 2] [15, 12, 9, 1] [15, 14, 12, 2] [15, 13, 9, 6] [15, 7, 4, 1] [15, 4] [15, 13, 7, 4]

Number of Stages	Code Length	Maximal Taps
16	65, 535	[16, 12, 3, 1] [16, 12, 9, 6] [16, 9, 4, 3] [16, 12, 7, 2] [16, 10, 7, 6] [16, 15, 7, 2] [16, 9, 5, 2] [16, 13, 9, 6] [16, 15, 4, 2] [16, 15, 9, 4]
17 ^a	131, 071	[17, 3] [17, 3, 2, 1] [17, 7, 4, 3] [17, 16, 3, 1] [17, 12, 6, 3, 2, 1] [17, 8, 7, 6, 4, 3] [17, 11, 8, 6, 4, 2] [17, 9, 8, 6, 4, 1] [17, 16, 14, 10, 3, 2] [17, 12, 11, 8, 5, 2]
18	262, 143	[18, 7] [18, 10, 7, 5] [18, 13, 11, 9, 8, 7, 6, 3] [18, 17, 16, 15, 10, 9, 8, 7] [18, 15, 12, 11, 9, 8, 7, 6]
19 ^a	524, 287	[19, 5, 2, 1] [19, 13, 8, 5, 4, 3] [19, 12, 10, 9, 7, 3] [19, 17, 15, 14, 13, 12, 6, 1] [19, 17, 15, 14, 13, 9, 8, 4, 2, 1] [19, 16, 13, 11, 19, 9, 4, 1] [19, 9, 8, 7, 6, 3] [19, 16, 15, 13, 12, 9, 5, 4, 2, 1] [19, 18, 15, 14, 11, 10, 8, 5, 3, 2] [19, 18, 17, 16, 12, 7, 6, 5, 3, 1]
20	1, 048, 575	[20, 3] [20, 9, 5, 3] [20, 19, 4, 3] [20, 11, 8, 6, 3, 2] [20, 17, 14, 10, 7, 4, 3, 2]
21	2, 097, 151	[21, 2] [21, 14, 7, 2] [21, 13, 5, 2] [21, 14, 7, 6, 3, 2] [21, 8, 7, 4, 3, 2] [21, 10, 6, 4, 3, 2] [21, 15, 10, 9, 5, 4, 3, 2] [21, 14, 12, 7, 6, 4, 3, 2] [21, 20, 19, 18, 5, 4, 3, 2]
22	4, 194, 303	[22, 1] [22, 9, 5, 1] [22, 20, 18, 16, 6, 4, 2, 1] [22, 19, 16, 13, 10, 7, 4, 1] [22, 17, 9, 7, 2, 1] [22, 17, 13, 12, 8, 7, 2, 1] [22, 14, 13, 12, 7, 3, 2, 1]
23	8, 388, 607	[23, 5] [23, 17, 11, 5] [23, 5, 4, 1] [23, 12, 5, 4] [23, 21, 7, 5] [23, 16, 13, 6, 5, 3] [23, 11, 10, 7, 6, 5] [23, 15, 10, 9, 7, 5, 4, 3] [23, 17, 11, 9, 8, 5, 4, 1] [23, 18, 16, 13, 11, 8, 5, 2]
24	16, 777, 215	[24, 7, 2] [24, 4, 3, 1] [24, 22, 20, 18, 16, 14, 11, 9, 8, 7, 5, 4] [24, 21, 19, 18, 17, 16, 15, 14, 13, 10, 9, 5, 4, 1]
25	33, 554, 431	[25, 3] [25, 3, 2, 1] [25, 20, 5, 3] [25, 12, 5, 4] [25, 17, 10, 3, 2, 1] [25, 23, 21, 19, 9, 7, 5, 3] [25, 18, 12, 11, 6, 5, 4] [25, 20, 16, 11, 5, 3, 2, 1] [25, 12, 11, 8, 7, 6, 4, 3]
26	67, 108, 863	[26, 6, 2, 1] [26, 22, 21, 16, 12, 11, 10, 8, 5, 4, 3, 1]
27	134, 217, 727	[27, 5, 2, 1] [27, 18, 11, 10, 9, 5, 4, 3]
28	268, 435, 455	[28, 3] [28, 13, 11, 9, 5, 3] [28, 22, 11, 10, 4, 3] [28, 24, 20, 16, 12, 8, 4, 3, 2, 1]

Number of Stages	Code Length	Maximal Taps
29	536, 870, 911	[29. 2] [29. 20. 11. 2] [29. 13. 7. 2] [29. 21. 5. 2] [29. 26. 5. 2] [29. 19. 16. 6. 3. 2] [29. 18. 14. 6. 3. 2]
30	1, 073, 74, 1, 823	[30. 23. 2. 1] [30. 6. 4. 1] [30. 24. 20. 16. 14. 13. 11. 7. 2. 1]
31 ^a	2, 147, 483, 647	[31. 29. 21. 17] [31. 28. 19. 15] [31. 3] [31. 3. 2. 1] [31. 13. 8. 3] [31. 21. 12. 3. 2. 1] [31. 20. 18. 7. 5. 3] [31. 30. 29. 25] [31. 28. 24. 10] [31. 20. 15. 5. 4. 3] [31. 16. 8. 4. 3. 2]
32	4, 294, 967, 295	[32. 22. 2. 1] [32. 7. 5. 3. 2. 1] [32. 28. 19. 18. 16. 14. 11. 10. 9. 6. 5. 1]
33	8, 589, 934, 591	[33. 13] [33. 22. 13. 11] [33. 26. 14. 10] [33. 6. 4. 1] [33. 22. 16. 13. 11. 8]
61 ^a	2, 305, 843, 009, 213, 693, 951	[61. 5. 2. 1]
89 ^a	618, 970, 019, 642, 690, 137, 449, 562, 112	[89. 6. 5. 3]

APPENDIX B

FCC regulations regarding
spread spectrum use and unlicensed transmitters

In May 1985 the Federal Communications Commission (FCC) changed its rulings to allow commercial applications of spread spectrum [14], [15]. Previously spread spectrum had been forbidden for civilian applications. The regulations permit using spread spectrum links on the Industrial, Scientific and Medical bands on the frequencies 902-928 MHz, 2.4-2.5 GHz and 5.725-5.85 GHz. Frequency hopping and direct sequence systems are allowed, provided that the output power does not exceed 1 watt. Amateur Radio Service at all amateur bands above 420 MHz is allowed to use spread spectrum on a secondary basis. Frequency hopping or direct sequence can be used with 100 watts maximum output power. Police Radio Service is only authorized to use frequency hopping systems on frequencies between 37 and 952 MHz in the Public Safety Radio Service bands. Maximum output power is 2 watts.

FCC part 15 makes allowances for unlicensed intentional radiators. The First Report and Order in FCC General Docket 87-389 limits field strength from intentional radiators in 216-960 MHz bands to $200 \mu\text{V/m}$ at 3 meters which relates to about -80 dBw output power. FCC part 94 allows for transmitters with up to 20

watts output power on licensed channels in the 900 MHz frequency bands. Normally licenses are given for 12.5 kHz channels and transmitters require carrier stability of 1.5 ppm. FCC 87-3 section 15.247 allows 1 watt output power for an unlicensed frequency hopping or direct sequence spread spectrum systems on frequencies from 902-928 MHz, 2400-2483.5 MHz and 5.785-5.850 GHz.

In summarizing the above stated rules, spread spectrum systems offer an economical and accessible solution to radio links. Reasonable output power is permitted, the bandwidth is wide allowing for high data rates, carrier stability is not regulated, and unlicensed operation is permitted. These factors have instigated development of numerous new radio link applications.

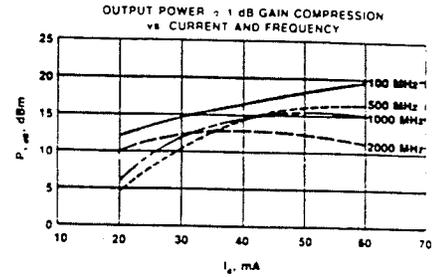
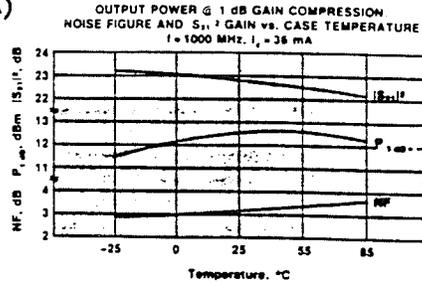
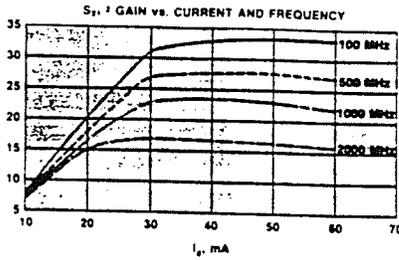
APPENDIX C

Circuit schematics and data sheets

Receiver RF section data sheets

S-parameter data and performance curves

MAR-8 ($T_A = 25^\circ\text{C}$, $I_d = 36\text{ mA}$)



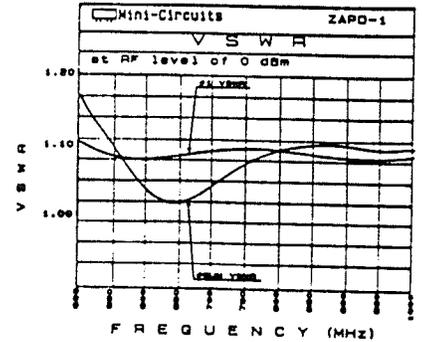
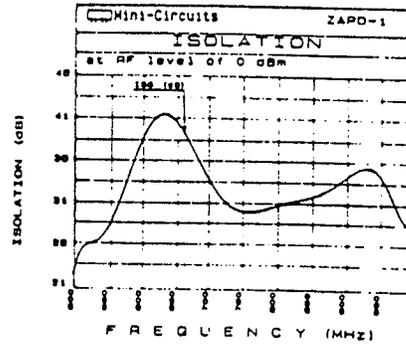
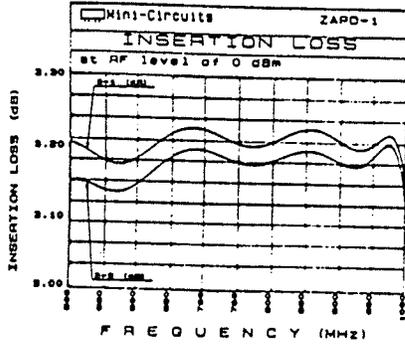
Freq. MHz	S_{11} (Input Return Loss)			S_{21} (Power Gain)		S_{12} (Isolation Out-In)			S_{22} (Output Return Loss)			K
	dB	Mag	Ang	dB	Ang	dB	Mag	Ang	dB	Mag	Ang	
100	-15.92	0.61	-21	33.0	162	-40.00	0.01	38	-4.73	0.58	-24	0.79
500	-8.18	0.39	-77	27.8	109	-27.96	0.04	52	-9.37	0.34	-96	0.75
1000	-11.37	0.27	-113	23.0	80	-24.44	0.06	51	-13.56	0.21	-147	0.89
1500	-11.70	0.26	-139	19.4	62	-21.94	0.08	46	-14.89	0.18	174	0.96
2000	-10.46	0.30	-155	16.9	47	-20.00	0.10	41	-15.39	0.17	153	0.97
2500	-9.63	0.33	-180	14.8	32	-18.42	0.12	32	-14.42	0.19	127	1.01
3000	-8.87	0.36	167	12.9	20	-17.72	0.13	27	-17.08	0.14	111	1.07
3500	-7.54	0.42	153	11.4	6	-17.08	0.14	21	-17.72	0.13	107	1.06
4000	-6.94	0.45	141	9.8	-5	-16.48	0.15	14	-19.17	0.11	106	1.10

2WAY-0° Power Splitter/Combiners

50 ohms

ZAPD-1

0.5 to 1GHz

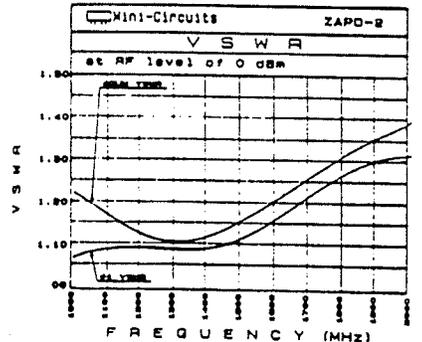
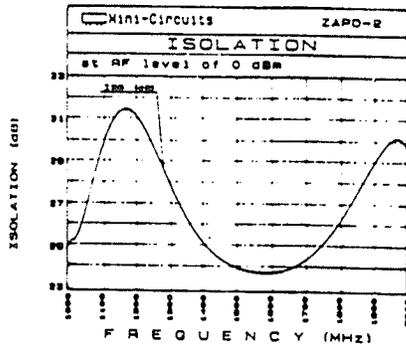
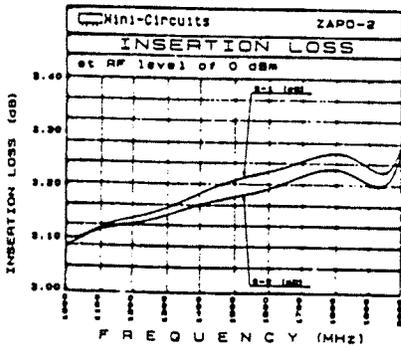


FREQUENCY (MHz)	INSERTION LOSS (dB)		AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
	S-1	S-2		
500.0	3.21	3.16	0.05	23.83
525.0	3.19	3.14	0.05	25.98
550.0	3.18	3.14	0.04	28.63
600.0	3.17	3.14	0.03	37.12
650.0	3.22	3.18	0.04	40.68
700.0	3.23	3.20	0.03	33.24
750.0	3.20	3.17	0.03	30.69
775.0	3.20	3.17	0.03	30.30
800.0	3.21	3.18	0.03	30.34
850.0	3.25	3.21	0.04	31.69
875.0	3.22	3.19	0.03	33.00
900.0	3.18	3.15	0.03	34.52
950.0	3.22	3.21	0.01	33.85
975.0	3.21	3.19	0.02	31.00
1000.0	3.18	3.16	0.02	28.08

FREQUENCY (MHz)	VSWR		
	S	1	2
500.0	1.16	1.10	1.09
525.0	1.13	1.09	1.08
550.0	1.10	1.08	1.07
600.0	1.03	1.08	1.07
650.0	1.02	1.08	1.07
700.0	1.04	1.09	1.07
750.0	1.08	1.10	1.07
775.0	1.09	1.10	1.07
800.0	1.10	1.09	1.07
850.0	1.10	1.09	1.06
875.0	1.10	1.09	1.06
900.0	1.10	1.08	1.06
950.0	1.10	1.08	1.06
975.0	1.10	1.08	1.06
1000.0	1.10	1.09	1.07

ZAPD-2

1 to 2GHz



FREQUENCY (MHz)	INSERTION LOSS (dB)		AMPLITUDE UNBALANCE (dB) 1-2	ISOLATION (dB)
	S-1	S-2		
1000.0	3.11	3.10	0.01	24.77
1050.0	3.10	3.10	0.00	27.28
1100.0	3.13	3.12	0.01	29.92
1200.0	3.15	3.14	0.01	31.18
1300.0	3.15	3.13	0.02	27.64
1350.0	3.18	3.16	0.02	26.24
1400.0	3.20	3.18	0.02	25.19
1450.0	3.21	3.18	0.03	24.48
1500.0	3.20	3.17	0.03	24.04
1550.0	3.21	3.18	0.03	23.83
1600.0	3.21	3.18	0.03	23.86
1725.0	3.25	3.22	0.03	24.95
1825.0	3.18	3.15	0.03	27.05
1875.0	3.33	3.30	0.03	28.60
2000.0	3.29	3.28	0.01	29.68

FREQUENCY (MHz)	VSWR		
	S	1	2
1000.0	1.22	1.07	1.06
1050.0	1.20	1.09	1.08
1100.0	1.17	1.09	1.08
1200.0	1.13	1.10	1.08
1300.0	1.11	1.09	1.07
1350.0	1.11	1.09	1.07
1400.0	1.13	1.10	1.06
1450.0	1.14	1.10	1.07
1500.0	1.16	1.12	1.08
1550.0	1.18	1.14	1.10
1600.0	1.21	1.17	1.12
1725.0	1.27	1.23	1.18
1825.0	1.32	1.28	1.22
1875.0	1.35	1.30	1.24
2000.0	1.40	1.32	1.26

Frequency Mixers Models

LEVEL 7 (+7dBm LO, up to +1dBm RF)

TFM-4
ZFM-4



computer-automated performance data
typical production unit / for data of other models consult factory

mixer conversion loss and isolation

RF MHz	LO MHz	Conversion Loss (dB)			Isolation L-R (dB)			Isolation L-I (dB)		
		LO -4dBm	LO -7dBm	LO -10dBm	LO +4dBm	LO +7dBm	LO +10dBm	LO +4dBm	LO +7dBm	LO +10dBm
5 000	35 00	7.39	7.08	6.85	> 64.00	> 67.00	66.97	> 64.00	62.10	59.80
20 000	50 00	7.19	6.84	6.61	> 64.00	> 67.00	62.16	> 64.00	59.11	57.53
50 000	80 00	6.97	6.64	6.45	52.06	50.64	50.62	51.15	49.95	48.63
100 000	70 00	6.76	6.48	6.32	45.63	44.54	44.61	45.08	43.90	42.67
138.390	108.39	6.81	6.51	6.38	39.91	38.97	39.28	39.15	38.26	37.49
227.320	197.32	6.85	6.59	6.41	38.18	37.28	37.71	37.26	36.56	36.05
271.780	241.78	6.66	6.44	6.26	35.39	34.49	34.87	34.59	34.10	33.61
360.710	330.71	6.68	6.47	6.34	33.51	32.40	32.45	33.15	32.75	31.86
449.640	419.64	6.84	6.57	6.40	33.30	31.70	31.37	31.47	31.16	30.26
538.570	508.57	6.69	6.45	6.29	33.34	31.48	30.96	31.22	30.87	29.94
583.030	553.03	6.76	6.54	6.40	31.94	30.37	29.93	31.03	30.53	29.24
671.960	641.96	7.12	6.82	6.56	30.92	29.62	29.36	29.85	29.00	27.48
760.890	730.89	7.16	6.83	6.56	30.46	29.45	29.56	28.21	27.36	25.98
849.820	819.82	7.34	6.86	6.54	30.45	29.60	29.84	27.33	26.76	25.43
894.280	864.28	7.67	7.01	6.57	30.77	30.37	30.69	24.95	25.36	24.55
983.210	953.21	7.85	7.24	6.72	30.24	29.78	30.11	23.37	23.67	22.94
1027.700	997.70	8.00	7.43	6.95	29.82	29.36	30.17	22.38	22.34	21.66
1116.600	1086.60	8.05	7.58	7.27	28.97	28.75	29.77	21.30	21.27	20.25
1200.000	1170.00	8.01	7.70	7.49	28.99	28.39	29.34	20.82	20.82	19.72
1250.000	1220.00	8.06	7.80	7.68	27.96	28.05	29.00	20.23	20.19	19.35

mixer VSWR

freq. MHz	VSWR, RF port			VSWR, LO port			VSWR, IF port		
	LO -4dBm	LO -7dBm	LO -10dBm	LO -4dBm	LO -7dBm	LO -10dBm	LO +4dBm	LO +7dBm	LO +10dBm
5 000	1.46	1.54	1.62	2.01	3.00	4.40	1.35	1.12	1.01
10 000	1.34	1.42	1.51	1.93	2.83	4.06	1.35	1.12	1.01
50 000	1.25	1.34	1.44	1.90	2.85	4.06	1.37	1.13	1.03
100 000	1.21	1.31	1.40	1.84	2.72	3.77	1.38	1.15	1.05
200 000	1.18	1.26	1.34	1.76	2.49	3.46	1.44	1.22	1.12
212 500	1.17	1.25	1.33	1.76	2.44	3.41	1.44	1.22	1.12
337 000	1.14	1.20	1.27	1.70	2.33	3.21	1.59	1.36	1.26
420 000	1.13	1.17	1.22	1.68	2.23	3.14	1.71	1.47	1.37
500 000	1.12	1.13	1.17	1.66	2.19	2.98	1.82	1.56	1.46
544 500	1.13	1.12	1.15	1.67	2.17	2.87	1.87	1.61	1.52
627 500	1.14	1.12	1.12	1.64	2.14	2.75	1.93	1.66	1.61
710 500	1.17	1.13	1.12	1.61	2.05	2.68	1.89	1.64	1.59
793 500	1.20	1.16	1.15	1.64	2.02	2.69	1.93	1.69	1.66
835 000	1.22	1.18	1.17	1.67	2.05	2.72	1.95	1.69	1.66
959 500	1.27	1.22	1.23	1.75	2.12	2.71	1.82	1.60	1.55
1000 000	1.30	1.24	1.26	1.76	2.11	2.76	1.75	1.54	1.49
1084 000	1.38	1.31	1.36	1.82	2.17	2.78	1.58	1.39	1.33
1167 000	1.53	1.43	1.52	1.96	2.24	2.92	1.39	1.23	1.17
1208 500	1.65	1.52	1.63	2.01	2.32	2.83	1.29	1.15	1.10
1250 000	1.79	1.62	1.75	2.14	2.36	2.99	1.20	1.07	1.08

ϕ detection

freq. (MHz)	max. DC output mV	DC offset mv
5.000	+218.12	+0.00
10.000	+219.36	+0.00
50.000	+216.50	+0.00
100.000	+219.70	+0.02
120.000	+223.77	+0.06
185.730	+226.90	+0.24
230.910	+226.80	+0.41
321.270	+233.26	+0.34
411.640	+207.81	+0.06
500.000	+211.13	+0.34
547.180	+219.10	+0.10
637.550	+216.95	-0.76
727.910	+198.44	-0.04
818.280	+191.82	-0.63
863.460	+189.28	+0.69
953.820	+174.32	+0.44
1000.000	+169.06	-0.67
1100.000	+167.29	+0.89
1200.000	+156.90	-2.15
1250.000	+152.76	-4.81

Measurements at RF & LO Power +7 dBm

Frequency Mixers

Models

LEVEL 10 (+10dBm LO, up to +5dBm RF)

TFM-150
ZFM-150



computer-automated performance data
typical production unit / for data of other models consult factory

mixer conversion loss and isolation

RF MHz	LO MHz	Conversion Loss (dB)			Isolation L-R (dB)			Isolation L-I (dB)		
		LO -7dBm	LO +10dBm	LO +13dBm	LO +7dBm	LO +10dBm	LO +13dBm	LO +7dBm	LO +10dBm	LO +13dBm
10 000	40 00	6 86	6 45	5 13	23 51	25 80	27 54	22 38	24 40	26 34
20 000	50 00	7 14	6 61	6 34	27 97	30 46	32 63	26 63	29 11	31 31
130 610	100 61	6 67	6 30	6 00	34 46	36 94	39 60	32 59	35 84	38 84
251 210	221 21	6 94	6 42	6 17	35 54	37 51	39 45	34 37	37 82	39 94
432 120	402 12	6 84	6 38	6 09	35 30	36 22	37 73	36 99	37 58	36 81
500 000	470 00	7 12	6 61	6 25	34 85	35 79	37 53	36 86	36 42	35 18
552 730	522 73	6 97	6 47	6 11	34 54	35 50	37 47	36 16	35 14	35 44
673 330	643 33	7 02	6 53	6 27	33 75	34 67	36 91	34 23	33 34	33 16
793 940	763 68	7 22	6 64	6 26	33 34	34 16	36 05	32 63	31 81	31 03
914 550	884 43	7 46	6 57	6 23	30 90	32 34	34 63	30 74	30 81	32 29
974 850	944 91	6 89	6 11	5 73	30 08	31 59	34 71	29 97	30 10	31 00
1035 200	1005 40	7 68	7 04	6 58	29 48	30 74	33 95	29 59	29 56	29 88
1155 800	1125 60	7 87	7 24	6 86	29 06	30 26	33 04	30 57	30 08	29 66
1276 400	1246 50	7 25	6 75	6 45	28 54	29 72	32 56	30 95	30 93	30 95
1397 000	1366 80	7 13	6 57	6 29	27 77	28 85	31 02	31 65	31 94	31 72
1517 600	1487 50	7 13	6 59	6 31	27 47	28 61	30 81	31 07	31 80	31 80
1638 200	1608 00	7 27	6 63	6 41	26 64	27 94	31 04	28 51	29 65	29 86
1758 800	1728 70	7 54	6 91	6 69	27 21	28 39	31 71	26 22	26 17	26 74
1879 400	1849 50	7 63	7 01	6 70	29 18	30 98	33 15	26 60	26 61	26 54
2000 000	1970 00	8 00	7 24	7 00	30 21	32 51	39 43	25 08	24 79	24 71

mixer VSWR

φ detection

freq. MHz	VSWR, RF port			VSWR, LO port			VSWR, IF port			freq. (MHz)	max. DC output mV	DC offset mV
	LO -7dBm	LO +10dBm	LO +13dBm	LO -7dBm	LO +10dBm	LO +13dBm	LO -7dBm	LO +10dBm	LO +13dBm			
10 000	1 78	1 62	1 57	1 65	1 66	2 23	1 45	1 35	1 36	10 000	+210 73	2 85
50 000	1 43	1 29	1 21	1 10	1 49	2 18	1 34	1 15	1 09	20 000	+214 48	81
100 000	1 43	1 29	1 20	1 09	1 39	2 01	1 36	1 15	1 05	50 000	+212 90	+0 00
200 000	1 52	1 34	1 25	1 18	1 36	1 96	1 39	1 16	1 04	100 000	+210 61	+ 22
251 210	1 55	1 38	1 28	1 24	1 34	1 91	1 39	1 17	1 04	124 110	+210 10	+ 33
371 820	1 70	1 49	1 37	1 36	1 30	1 77	1 43	1 20	1 05	200 000	+216 58	+ 50
492 420	1 81	1 60	1 45	1 49	1 29	1 66	1 48	1 23	1 08	238 230	+221 12	+ 34
552 730	1 88	1 62	1 46	1 56	1 28	1 60	1 49	1 23	1 10	352 340	+223 97	- 50
673 330	1 98	1 70	1 53	1 66	1 26	1 48	1 50	1 24	1 14	428 420	+194 95	- 42
793 940	2 03	1 79	1 62	1 75	1 26	1 40	1 49	1 24	1 17	500 000	+185 02	+ 71
914 550	2 13	1 89	1 74	1 80	1 22	1 31	1 44	1 21	1 17	542 530	+191 96	- 74
1000 000	2 24	2 02	1 87	1 73	1 20	1 25	1 47	1 24	1 20	656 650	+223 05	+ 75
1095 500	2 35	2 07	1 93	1 90	1 20	1 20	1 49	1 25	1 20	770 760	+183 02	+1 43
1216 100	2 44	2 15	1 98	1 86	1 18	1 21	1 51	1 26	1 18	846 840	+171 52	+ 4 48
1336 700	2 43	2 13	2 00	1 86	1 13	1 30	1 51	1 27	1 15	922 910	+195 29	+1 61
1457 300	2 30	2 05	1 95	1 65	1 07	1 43	1 47	1 26	1 15	1000 000	+173 82	- 2 06
1577 900	2 12	1 88	1 79	1 41	1 12	1 88	1 41	1 23	1 18	1250 000	+177 10	- 2 00
1698 500	1 88	1 45	1 61	1 31	1 16	1 79	1 33	1 19	1 20	1500 000	+188 05	+3 99
1819 100	1 75	1 43	1 47	1 26	1 21	1 76	1 27	1 16	1 19	1750 000	+181 99	+ 4 17
2000 000	1 69	1 55	1 42	1 22	1 20	1 72	1 18	1 12	1 16	2000 000	+199 73	+ 4 20

Measurements at RF & LO Power +10 dBm

Receiver analog section schematic and data sheets



MOTOROLA

MC3357

Advance Information

LOW POWER NARROWBAND FM IF

... includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ $V_{CC} = 6.0$ Vdc)
- Excellent Sensitivity: Input Limiting Voltage - (-3.0 dB) = 5.0 μ V (Typ)
- Low Number of External Parts Required

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

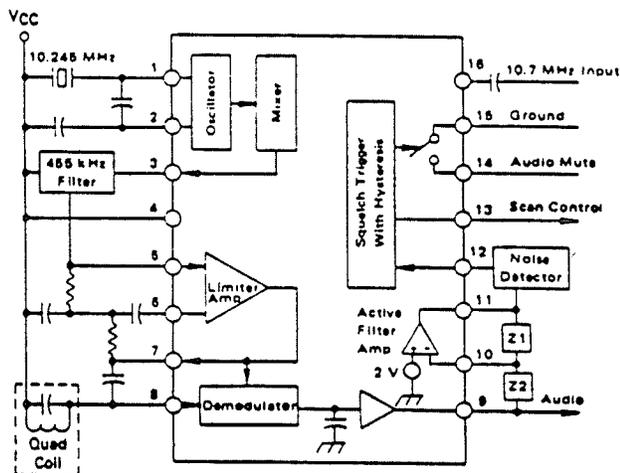


P SUFFIX PLASTIC PACKAGE CASE 648-06

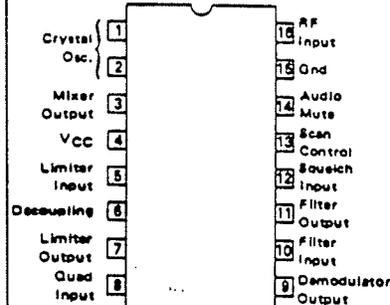


D SUFFIX PLASTIC PACKAGE CASE 751B-03 SO-16

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

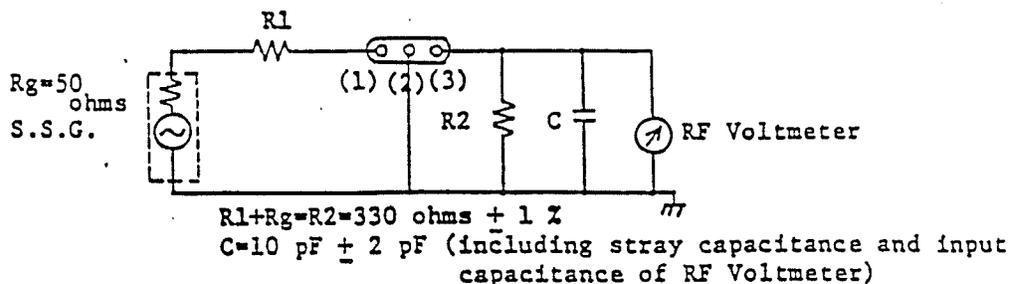
MURATA MANUFACTURING CO.,LTD.

Specification of Ceramic Filter

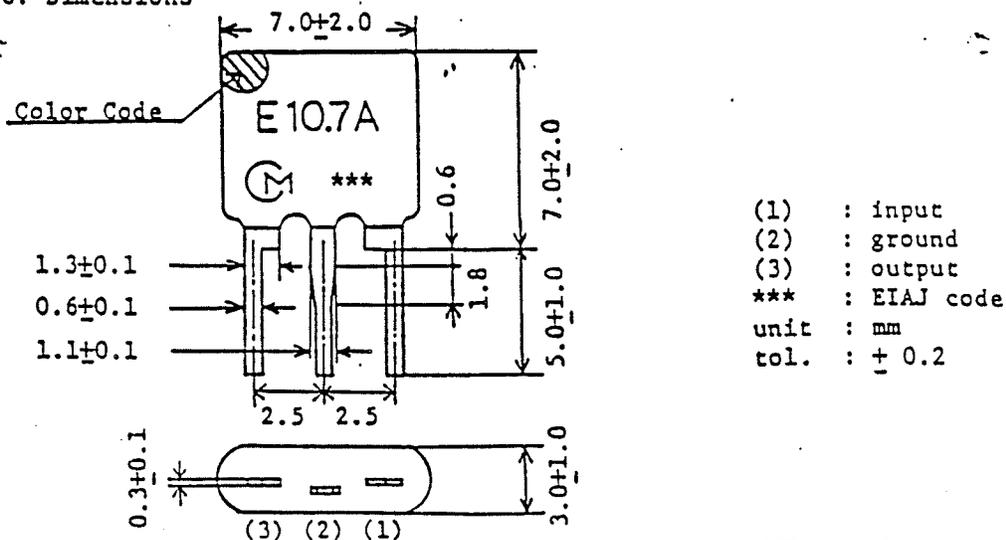
Type : SFE10.7MA5-A

26-10, 2-CHOME, TENJIN, NAGAOKAKYO-SHI,
KYOTO 617, JAPAN
PHONE: 075-921-9111
TELEX: 05429-901 MURATA J

- 1. Center Frequency : 10.700 MHz \pm 30 KHz (red)
- 2. 3 dB Band Width : 280 KHz \pm 50 KHz
- 3. 20 dB Band Width : 650 KHz max.
- 4. Insertion Loss : 6 dB max.
- 5. Ripple : 1 dB max.
- 6. Spurious Response : 30 dB min.
(8 to 12 MHz)
- 7. Temperature Coefficient of Center Frequency : \pm 50 ppm/ $^{\circ}$ C max.
Temperature Range : -20° C to $+80^{\circ}$ C
- 8. Input & Output Impedance : 330 ohms
- 9. Test Circuit



10. Dimensions



Approved by	Checked by	Drawn by	Issue Date	Spec. No.
<i>K. Togawa</i> K. Togawa	<i>E. Ohtsuka</i> E. Ohtsuka	<i>R. Koshizaki</i> R. Koshizaki	Apr. 3, 1981	SPC-F01 05009 (SPC-F-9008 A)

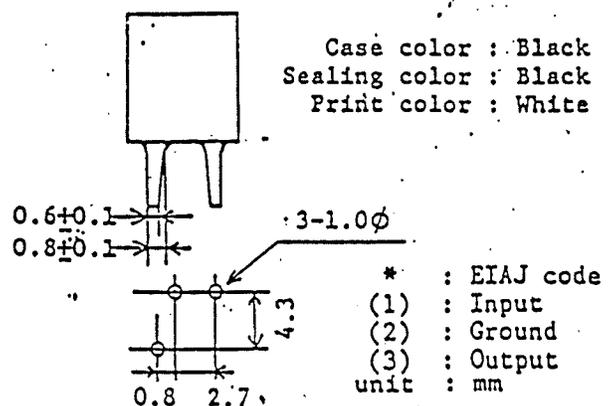
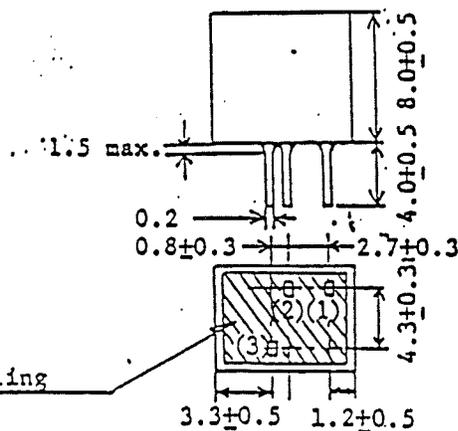
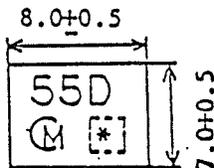
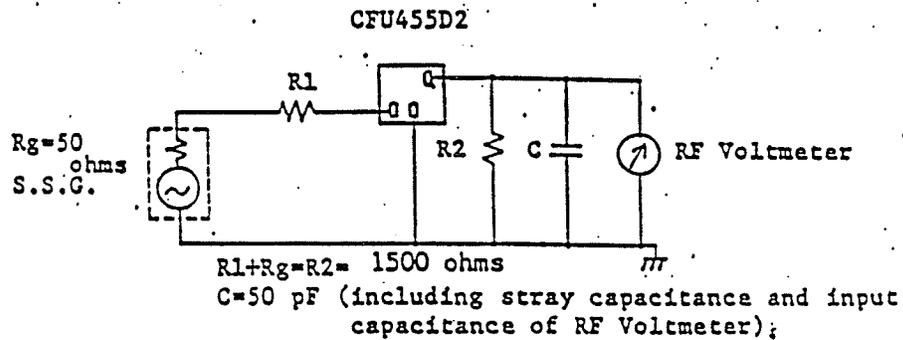
MURATA MANUFACTURING CO.,LTD.

Specification of Ceramic Filter

Type : CFU455D2

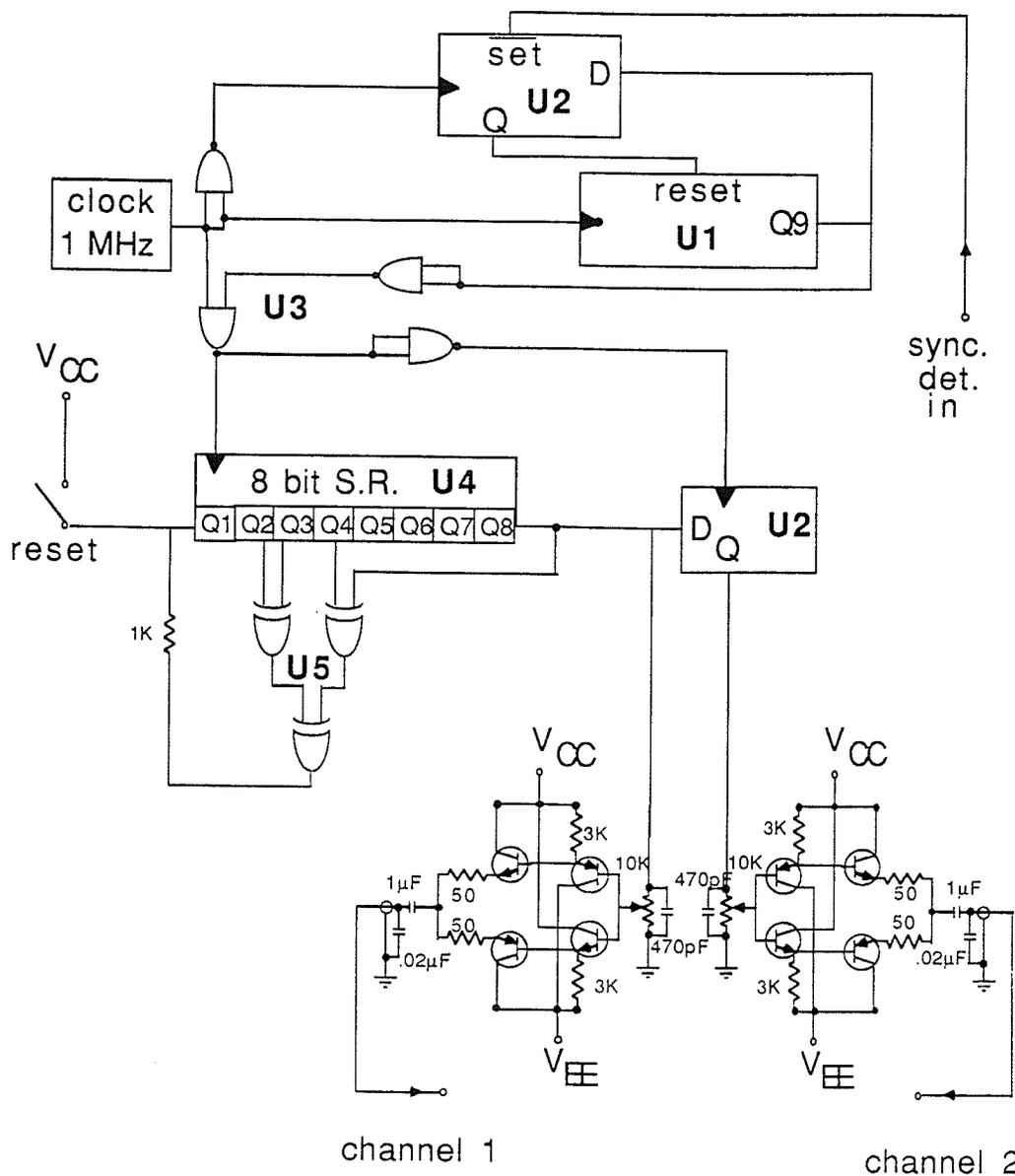
23-10, 2-CHOME, TENJIN, NAGAOKAKYU-SHI,
KYOTO 617, JAPAN.
PHONE: 075-921-3111
TELEX: 03429-901 MURATA J

- | | |
|--|-------------------------|
| 1. Center Frequency | : 455 KHz \pm 1.5 KHz |
| 2. 6 dB Band Width | : \pm 10 KHz min. |
| 3. 40 dB Band Width | : \pm 20 KHz max. |
| 4. Stop Band Attenuation(within 455 \pm 100 KHz) | : 27 dB min. |
| 5. Ripple (within 455 \pm 7 KHz) | : 2 dB max. |
| 6. Insertion Loss | : 4 dB max. |
| 7. Input & Output Impedance | : 1.5 Kohms |
| 8. Temperature Range | : -20°C to +80°C |
| 9. Test Circuit | |



Approved by	Checked by	Issued by	Drawn by	Issue Date	SPC No.
<i>K. Togawa</i> K. Togawa	<i>H. Kuronaka</i> H. Kuronaka	<i>M. Higashiyama</i> M. Higashiyama	<i>Y. Shimizu</i> Y. Shimizu	OCT.14,1986	SPC-F14-00013A

Receiver digital section schematic



	V _{CC}	G	PN
U1	16	8	74HC4040
U2	1,10,13,14	7	74HC74
U3	1,10,13,14	7	74HC00
U4	1,9,14	7	74HC164
U5	13,14	7,12	74HC86

DIGITAL SECTION SCHEMATIC

APPENDIX D

System parts cost

Transmitter

1 MHz crystal clock module	FOX-1.00000	1	\$9.24	\$9.24
Shift register	74 HC 164	1	.72	.72
EX-OR gates	74 HC 86	1	.41	.41
Driver transistor	MMBT 2222A	2	.21	.42
Driver transistor	MMBT 2907A	2	.21	.42
Upconverter	SBL - 1Z	1	11.12	11.12
FM'ed PLL Source	CMEH-A-0555	1	30.33	30.33
Output filter	5HW-88560A-914	1	5.40	5.40
Power amplifier	UPC 1677C	1	4.65	<u>4.65</u>

TOTAL**\$62.71**

ReceiverRF section

Input filter	5HW-88560A-914	1	\$ 5.40	\$ 5.40
Preamp	MAR8	1	3.52	3.52
Correlator mixers	TFM-2	2	19.12	38.24
Down convertor	SBL-1Z	1	11.12	11.12
PLL source	CMEH-A-0555	1	30.33	<u>30.33</u>
				\$88.61

Analog section

FM receiver chip	MC 3357	1	\$3.66	\$3.66
Crystal	MP-1-11.059200	1	1.93	1.93
10.7 MHz ceramic filter	SFE 10.7 MA5-A	1	1.05	1.05
455 kHz ceramic filter	CFU 455D2	1	1.95	1.95
Noise detection diodes	1N914	2	.21	.42
Quadrature coil	RMC-2A6597HM	1	1.05	1.05
Buffer	LM 358	1	.57	<u>.57</u>
				\$10.63

Digital section

1 MHz crystal clock module	FOX 1.00000	1	\$9.24	\$9.24
Ripple counter	74 HC 4040	1	.72	.72
Dual D Flip Flop	74 HC 74	1	.41	.41
Quad. NAND	74 HC 00	1	.28	.28
8 bit shift register	74 HC 164	1	.72	.72
Quad. X-OR	74 HC 164	1	.41	.41
Driver transistor	MMBT 2222A	4	.21	.84
Driver transistor	MMBT 2907A	4	.21	<u>.84</u>

\$13.46

TOTAL**\$112.70**

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