A PRACTICAL ANALYSIS OF A DIGITAL PHASE LOCK LOOP FOR USE WITH POWER ELECTRONIC CONVERTERS

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In Partial Fulfillment

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MASTER OF SCIENCE

Electrical Engineering Department

by

Glenn K. Rosendahl

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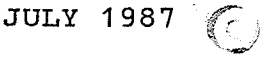

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ABSTRACT

Power Electronic Converters (rectifiers, inverters, and static compensators) use a Phase Lock Loop (PLL) to provide a steady reference for firing controls. This report gives an overview of PLLs and compares a prototype PLL with a commercially available unit.

A Digital Phase Lock Loop (DPLL) prototype was designed and constructed for comparison tests with a commercial zero crossing type PLL. These comparisons emphasize system disturbance recovery time and tracking of system unbalances.

It was found that the prototype design resynchronized in half the time that the commerical unit did, following major system disturbances. However in steady state the commerical PLL proved to be more stable than the prototype design.

ACKNOWLEDGEMENT

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LIST OF SYMBOLS

Ea,Eb,Ec	phase voltages of simulator
Va,Vb,Vc VA,VB,VC	phase voltages
Vd	direct voltage
Vd'	quadrature voltage derived from Vd
Vq	quadrature voltage
Vq'	direct voltage derived from Vq
V1,V2,V0	positive, negative, and zero sequence component voltage
S1,S2, etc.	switches
Sn-1,Sn, etc.	phase error samples
K1,K2,Ka,Kb	gain constants
W	angular frequency
Θ (theta)	angle of system or reference quantities
Φ	phase error of reference with respect to the positive sequence component

CHAPTER 1

INTRODUCTION

1.1 NATURE OF PHASE LOCK LOOPS

Three basic components are present in all analog phase lock loops namely (see Fig. 1.1.1);

-A Phase Detector (PD)

-A loop filter

-A Voltage Controlled Oscillator (VCO), where the frequency is controlled by an external voltage, vc.

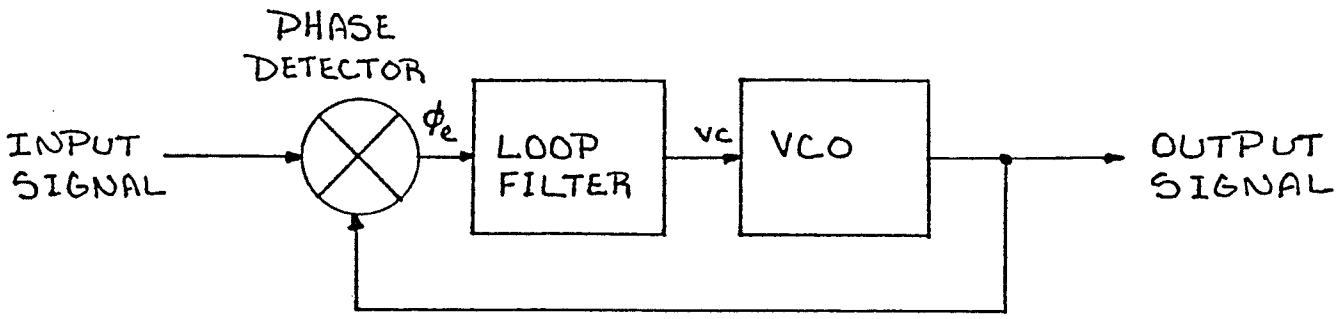

Figure 1.1.1: Basic Phase Locked Loop.

The Phase Detector extracts the phase error between the input signal and the local oscillator (VCO) output. This phase error is then filtered by the loop filter yielding a control voltage. The control voltage vc represents the phase error as well as the direction in which the oscillator frequency must move in order to keep pace. The control voltage is applied to the VCO adjusting the frequency such as to decrease the phase error between the input signal and the local oscillator.

Simply, the phase lock loop just tracks the frequency and phase of the input signal. Why then is their function important? The answer is that the input signal may be subject to corruption by additive noise and the task of the phase lock loop is to reproduce the input signal free of all such noise.

1.2 BACKGROUND AND HISTORY

Phase Lock Loop (PLL) techniques were first examined for synchronization of radio signals in the early nineteen thirties. But the first wide spread use for PLLs came with television to synchronize the horizontal and vertical sweep oscillators to transmitted synchronization pulses. Today narrow band versions are used in tracking weak satellite signals.

To date the most apparent uses of PLLs has been in communications. One of the primary reasons for this is its superior noise immunity. It was this immunity and its ability to track signals accurately that led to applications in Power Electronic equipment.

Power electronic converters (rectifiers ,inverters ,and static compensators) are particularily sensitive to the phase of ac sources. PLLs are used in High Voltage Direct Current (HVDC) transmission schemes, where they provide an accurate reference for converter firing controls. This reference helps to minimize harmonic instability and reactive power requirements of the converters. Several companies manufacture PLLs for power industry converter controls. In the following Section three PLL schemes are discussed.

1.3 PHASE LOCKING SCHEMES CURRENTLY IN USE

In ac systems the three-phase voltages can contain harmonics and be unbalanced. From these unclean waveforms Phase Lock Loops (PLL) have to extract the positive sequence component and track it both in frequency and phase. This extracted information then provides a stable reference for valve firing controls of HVDC inverters and rectifiers. Some methods for generating references for these controls are presented here.

1.3.1 NELSON RIVER BIPOLE I HVDC TRANSMISSION SCHEME

A block diagram of the phase lock oscillator is shown in Fig. 1.3.1. The main element of this controller is the Voltage Controlled Oscillator (VCO). The VCO produces short pulses with the frequency dependent on an input voltage Vc. These pulses are used as input to the ring counter which supplies the firing pulses to converter valves. This provides equidistant firing of valves (providing Vc remains constant). Having equidistant firing pulses is very important. Since converters produce harmonics which for a six pulse converter with equidistant firing pulses, generate the following ac side harmonics of order H, where;

$$H = 6n +/- 1 \ , n = 1,2,3,... \qquad 1.3.1$$

These harmonics are called Characteristic Harmonics for a Six Pulse Converter. They must be filtered out of the ac system. A set of filters are tuned for these characteristic harmonics on the ac side. But when the firing pulses are not of equal distance the converters produce harmonics in the full spectrum, not just the characteristic ones. Hence not all the generated harmonics are filtered from the ac system ,and these non-characteristic harmonics can cause such problems as harmonic instability in the

system and additional losses in machine loads.

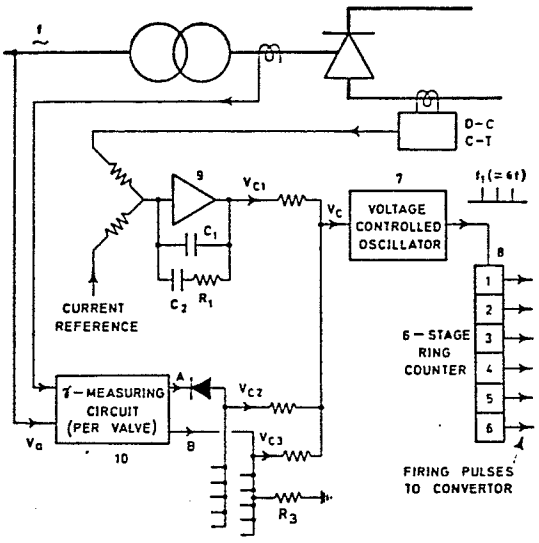

Figure 1.3.1: Principle of the Phase Locked Oscillator Control System. (reproduced from IEEE paper by J.D. Ainsworth, 1968)

The control voltage Vc is supplied by a negative feed back control loop. As shown in Fig. 1.3.1 (block 9), the constant current control uses an integrator to provide Vc. The negative terminal is connected to the direct current transducer on the line, while the current order is connected to the positive terminal. Then if the Direct current is less than ordered value, voltage Vc increases. This speeds the VCO up and in turn advances firing angle, alpha, thereby increasing the direct current. Alpha is similarily retarded for an increase in direct current above ordered value. There is no evidence that this scheme follows the positive sequence component of the ac system voltages; but, it has worked well for Manitoba Hydro's Nelson River Bipole I HVDC Transmission System for a number of years. More information is available in reference number 1.

1.3.2 BROWN BOVERI'S ZERO CROSSING METHOD

The particular zero crossing method to be discussed is the one used by Brown Boveri Co. (BBC). This method integrates the error in zero crossings between the incoming waveforms (the ac system) and the generated (PLL) zero crossings. As an example let the input waveforms contain both positive and negative sequence components as follows;

POSITIVE SEQUENCE COMPONENTS:

VA1 = 1.0 / 0 degrees P.U.

VB1 = 1.0 / 240 degrees P.U.

VC1 = 1.0 / 120 degrees P.U.

NEGATIVE SEQUENCE COMPONENTS:

VA2 = 0.5 / 0 degrees P.U.

VB2 = 0.5 / 120 degrees P.U.

VC2 = 0.5 / 240 degrees P.U.

The input waveforms are formed by the addition of all the components (as shown below);

INPUT WAVEFORMS:

VA = VA1 + VA2 = 3/2 / 0 degrees P.U.

VB = VB1 + VB2 = $\sqrt{3}/2$ / 210 degrees P.U.

VC = VC1 + VC2 = $\sqrt{3}/2$ / 150 degrees P.U.

It should be noted that the negative sequence component used in this example is about 10 times that normally found in ac systems. This value was chosen for simplicity of calculations and to exemplify the principle used.

The BBC system creates a positive error (P+) for early zero crossings and a negative error (P-) for late zero crossings (system waveforms with respect to generated reference). This is

shown graphically in Figs. 1.3.2 and 1.3.3 below.

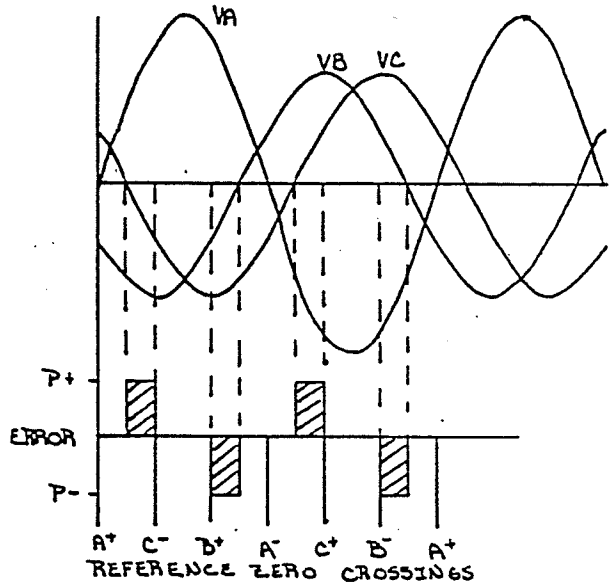

Figure 1.3.2: Reference in synchronism with Positive Sequence.

In the above case, reference zero crossings match the positive sequence components zero crossings. Note that shaded areas of P+ and P- are equal, hence zero average error exists. The zero average error is presented to the VCO through an integrator with a large time constant, ensuring only the average of P+ and P- reaches the oscillator. In addition the VCO operates at a frequency of 3072 times that of the system, producing clock pulses for timing purposes (approximately 0.1 electrical degrees). This also serves to reduce the sensitivity to minor changes in P+ and P-. Now shifting the reference zero crossings ahead by 30 degrees a net error is produced (see Fig. 1.3.3).

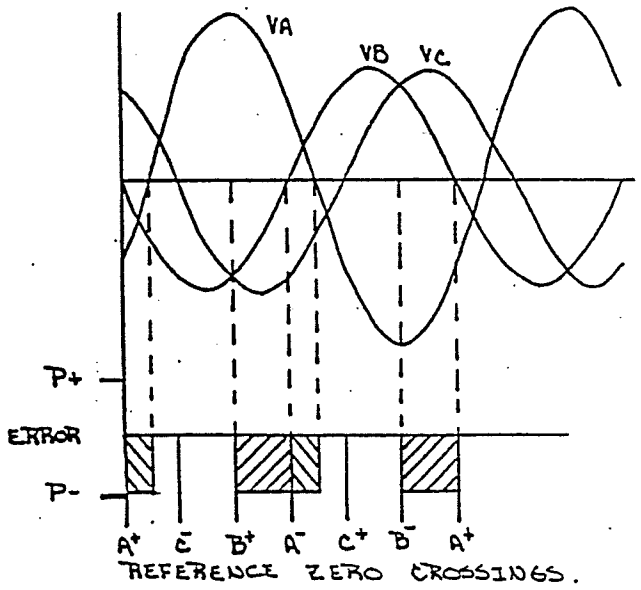

Figure 1.3.3: Reference 30 degrees ahead of Positive Sequence.

As seen above a negative overall error is created. This error informs the controller that the reference zero crossings are leading the positive sequence. This negative error is supplied to the integrator, and in effect lowers the integrators output voltage, which in turn slows the VCO correcting the error. A similar positive net error is created for a lagging zero crossing reference.

1.3.3 A CONTINUOUS PHASE COMPARISON TECHNIQUE

As of late there has been great interest in phase lock loops (PLL) which use continuous phase comparison (CPC) techniques. This Section will present the basic principles of continuous phase comparison and will focus in particular on an IEEE paper from Japan (see reference 2), which makes use of this principle.

In order to extract positive sequence components, the three-phase input must undergo a three-to two-phase conversion. If the ac systems three-phases are balanced this will produce two orthogonal phasors as shown in Fig. 1.3.4.

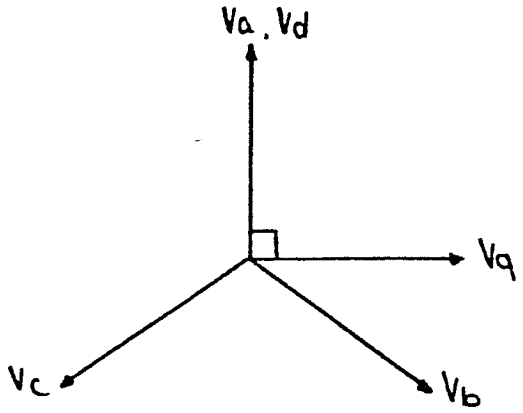

Figure 1.3.4: Ac system phasors Va,Vb,Vc before and after (Vd and Vq) three-to two-phase transformation.

$$Vd = Va \qquad 1.3.2$$

$$Vq = (Vb-Vc)/\sqrt{3} \qquad 1.3.3$$

The PLL generates two orthogonal reference phasors of unity length. Sine and Cosine waveforms are generated to form the reference phasors. Fig. 1.3.5 below shows both system and reference phasors.

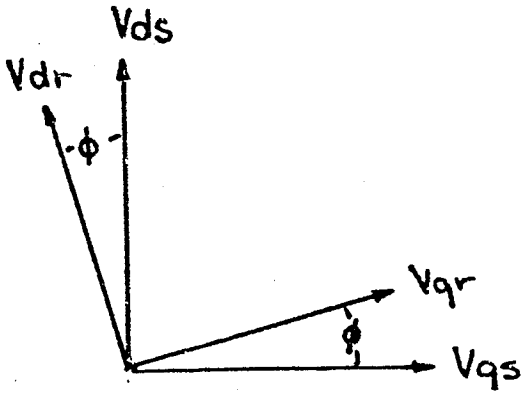

Figure 1.3.5: System and reference orthogonal phasors.

Two orthogonal sets of phasors now exist (for balanced systems only) where each is represented by;

$$Vds = V \cos(\text{theta system}) \qquad 1.3.4$$

$$Vqs = V \sin(\text{theta system}) \text{ ,where } V = (Vb-Vc)/\sqrt{3} = Va \qquad 1.3.5$$

$$Vdr = \cos(\text{theta reference}) \qquad 1.3.6$$

$$Vqr = \sin(\text{theta reference}) \qquad 1.3.7$$

The phase difference of these two sets (Φ) represents the phase error between reference and ac system, given by.

$$\Phi = \arcsin((VqsVdr - VdsVqr)/ U) \qquad 1.3.8$$

where;

$$U = \sqrt{(VqsVdr - VdsVqr)^2 + (VdsVdr + VqsVqr)^2} \qquad 1.3.9$$

This method extracts phase information very well for balanced three-phase waveforms. But, when unbalanced waveforms are presented (a negative sequence component is added) a second harmonic is generated in addition to the phase information. This second harmonic must be removed to enable tracking of the positive sequence waveform.

In the IEEE paper "HVDC TRANSMISSION CONTROL EQUIPMENT WITH HIGH RELIABILITY" [2], this second harmonic component is removed by a low pass filter (LF) within the control loop shown in Fig. 1.3.6.

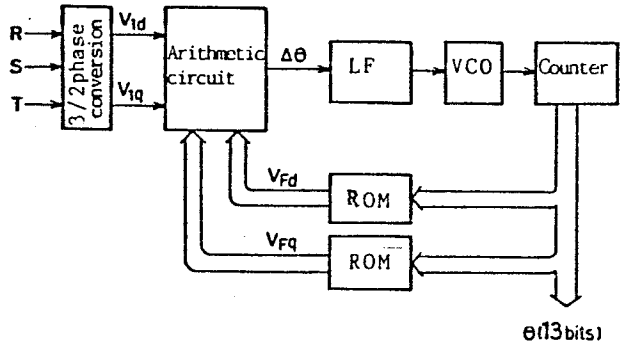

Figure 1.3.6: A PLL using a continuous phase comparison technique. (reproduction from IEEE paper by M.Ishikawa, S.Horiuchi, S.Hirose, T.Sakai, and T.Horisuchi,1985)

This configuration is very similar to the standard PLL architecture and makes use of both analog and digital components. In the following Section the above methods will be discussed and from this a suitable configuration will be selected.

1.4 SELECTION OF METHOD

One common aspect of the three methods discussed is that they are mainly analog. In using analog components, the power supplies must be of high quality; free of noise induced by transients on ac lines or temperature effects. This is where digital designs have an advantage, as they are not sensitive to power supply fluctuations. If the digital design makes use of a microprocessor it becomes very flexible as well.

Of the three methods BBC's and the Continuous Phase Comparison (CPC) PLLs measure the best performance, with fast tracking capability for system transients and slow modes to enhance stability. A decision was made to use a CPC technique and to implement it in a microprocessor based environment. This combination would give the PLL speed, flexibility, and greater immunity to power supply noise. The CPC technique employed is a modification of the one presented previously. An overview of this modification is presented below (a more detailed proof is presented in Appendix A).

1.4.1 METHOD DESCRIPTION

Every system may be to some degree unbalanced (contains negative sequence components). When an unbalanced three-phase system is subjected to the three-to two-phase transform the resulting two phasors are not orthogonal. Using the CPC technique

as outlined before, the unbalance produces a second harmonic as well as the desired phase information. In order to extract this phase information a low pass filter has to be employed. But if two additional phasors are generated orthogonal to these, the low pass filter may be eliminated from within the loop. By generating two sets of orthogonal vectors and applying them to the orthogonal reference phasors all second harmonic components will be removed from the phase information. In Fig. 1.4.1 below two phasors from an unbalanced system are shown with their respective generated orthogonal partners.

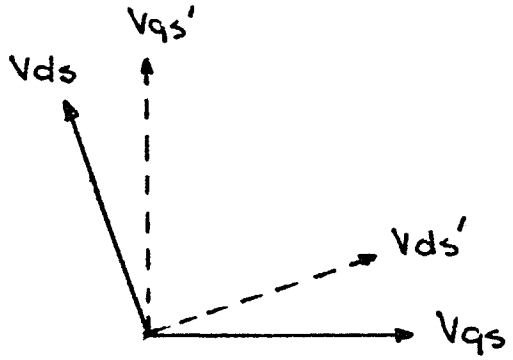

Figure 1.4.1: Unbalanced system phasors Vqs and Vds with their generated orthogonal partners Vqs' and Vds'.

These generated phasors are orthogonal and equal in absolute magnitude of their respective counter parts. These phasors are represented mathematically as;

Vqs = Vq sin(theta q) Vds = Vd cos(theta d) 1.4.1

Vqs'= Vq cos(theta q) Vds'= Vd sin(theta d) 1.4.2

And the orthogonal reference phasors are as before;

Vqr = sin(theta reference) 1.4.3

Vdr = cos(theta reference) 1.4.4

now we let;

$$X = VqsVdr - Vqs'Vqr + Vds'Vdr - VdsVqr \qquad 1.4.5$$

$$Y = VqsVqr + Vqs'Vdr + Vds'Vqr + VdsVdr \qquad 1.4.6$$

Then as before the phase error ,Phi, of the reference phase to the positive sequence phase is;

$$\Phi = \arcsin(X/\sqrt{X^2 + Y^2}) \qquad 1.4.7$$

This method is especially well suited for an all digital PLL design. This is because a digital averaging filter is particularly sensitive to signal sample rate. If the frequency of an unbalanced system is changing, a digital averaging filter would produce unacceptable errors, since it needs to know the frequency of incoming signals in order to filter properly. The modified continuous phase comparison technique (from above) is independent of sample rate. By taking three consecutive samples at a set sample rate; phase, frequency, and acceleration errors can be determined and corrected simultaneously.

Therefore as fast as three samples can be taken and processed this becomes the transient response time.

The major set back of this method is in generating these orthogonal phasors. Since it is implemented digitally a sine/cosine table is used with the sign determined by a derivative. This creates an additional problem. In order to be able to use tables, the incoming waveforms can only contain the systems fundamental frequency (no harmonics are allowed!). To circumvent this, a programmable low pass filter is inserted in each incoming signal line. These filters have constant phase delays at any programmed frequency. This constant phase delay can be taken into account by the digital PLL. This modification

offers desirable advantages over previous designs, by enhancing transient response time and stability.

1.5 OUTLINE OF THESIS

The selected method to my knowledge has not been examined previously. Therefore, this thesis aims to provide a base for further study. The following aspects of the method were examined;

1. Develop a computer model to examine the transient nature as well as possible control algorithms.
2. Examine the effect of step changes in phase and frequency, as well as composite errors of phase, frequency, and acceleration.
3. Develop versatile hardware allowing real time evaluations of the technique and control algorithms developed in software simulations.
4. Test this PLL on the Univeristy of Manitoba's HVDC Simulator for a limited number of cases. Tests will include a 180 degree phase shift as well as unbalanced voltage waveforms.

The next chapter discusses the analytical aspects of the problem and develops a computer model reflecting these concerns. Chapter 3 examines the actual hardware and software construction/integration performed and its short comings. Chapter 4 continues with an examination of the hardware and software when subjected to transients by the University of Manitoba's HVDC Simulator, detailing the results obtained. Finally, Chapter 5 contains the conclusions and recommendations.

CHAPTER 2

SOFTWARE SIMULATIONS

2.1 INTRODUCTION

The aim of this Chapter is to present the software simulations that were performed. This entails a description of the basic model, assumptions made, model operation, control algorithm, and tests performed including results.

2.2 THE BASIC MODEL

Through out this Section reference will be made to Fig. 2.2.1 below. The model is based on a double orthogonalization technique presented in Section 1.4.1. The model accepts two input phasors Va and Vbc, which are the same phasors produced by the 3 to 2 transforms described in Section 1.3.3, where Va=Vd and Vbc=Vq (see formulas 1.3.2 and 1.3.3). By projecting an orthogonal phasor for each of the input phasors Va and Vbc, phase error can be determined instantaneously irrespective of system unbalances. The following Section will list the assumptions made in applying this model in the simulations.

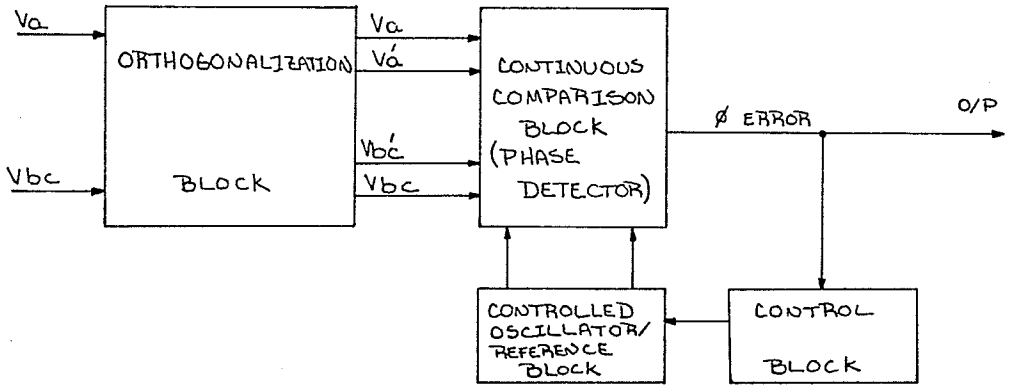

Figure 2.2.1: Simulation block diagram.

2.2.1 ASSUMPTIONS MADE

A number of assumptions have been made below noting that number 2 is generally untrue. This assumption has been made to simplify the model, but not to detract from the overall accuracy of the model.

1) The input phasors Va and Vbc have no zero sequence components and are free of harmonics.

2) Both measured values of Va and Vbc as well as their respective orthogonal components are free of error.

3) The Digital Controlled Oscillator has high resolution, a large range, and negative frequency capability (allows theta to decrease).

2.2.2 DESCRIPTION OF OPERATION

This simulation program is based on constant time increments where the simulation always starts at time zero and ends at the specified time, 'Finish'. 'Stept', defines the sample period or constant increment taken at each step. The results of every time step is recorded.

The three phase ac system is modelled by two phasors namely Va and Vbc. This allows unbalanced and/or faulted systems to be represented by specifying the absolute magnitudes and initial phase shifts (from a balanced system) of Va and Vbc. The frequency of these two phasors is controlled by WS, which generates a radian order for the phasors.

From this radian order, the phasor absolute magnitude and the intial phase the respective orthogonal phasors are constructed (see orthogonalization block of Fig. 2.2.1).

The simulation program allows one transient to be introduced, where the following may be specified;

a) The transient starting and ending times.

b) A new system frequency and/or an acceleration.

c) New values for absolute magnitude and phase of Va and Vbc.

No provisions presently exist to reinstate the orginal conditions prior to the transient. This could be a worth while future addition.

After the desired input file has been constructed the program is run. The program yields a phase error at the end of each time step. This phase error is presented to the control block, it is acted upon, and a control order is made. This in turn up dates the subsequent phase errors through the controlled oscillator. Samples of the phase error and/or any other parameters are taken every time step and recorded in a performance file. After time 'Finish', this performance file may be plotted or analyzed as desired.

2.3 MODELLING OF PHASE LOCK LOOP CONTROL

In this Section reference will be made to Fig. 2.3.1 throughout (this is an enlargement of the control block of Fig. 2.2.1). Phase error is measured while frequency and acceleration errors can be calculated. From this and a constant sample rate, a control routine was derived based on predicting and correcting errors. An assumption was made to limit the equations involved. This assumption is, that the system does not accelerate at an appreciable rate. Therefore the acceleration component need not be included.

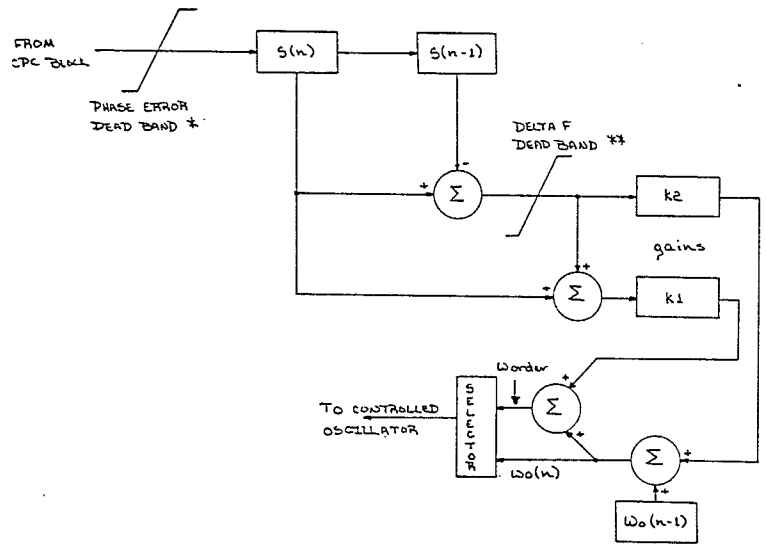

Figure 2.3.1: Enlargement of control block

* - This dead band sieve determines if the phase error is great enough to start the control routine. If it is not the process is reset and awaits an error that is larger than the dead band limits.

** - This sieve determines if an appreciable velocity error exists. If not, the frequency component is set to zero.

2.3.1 THE CONTROL ROUTINE

The control routine is based on phase and frequency errors only. The composite error is formulated as follows. Let Sn represent the present phase error sample and Sn-1 as the previous one and so on. The sample period is represented by delta T. Then,

$$\text{delta F} = (Sn - Sn\text{-}1)K2 \qquad 2.3.1$$

where,

$$K2 = 1/\text{delta T}$$

gives the frequency error. After the present frequency error (delta F) is calculated it passes through a dead band filter. If the value of delta F is within the dead band limits it is set to

zero, otherwise it passes unmodified (see Fig. 2.3.1). The predicted phase error for Sn+1 is;

$$Sn+1 = Sn + (Sn - Sn-1)$$

$$= 2Sn - Sn-1 \qquad 2.3.2$$

These two components and the steady state frequency order (Wo) are combined to form the correction order (Worder), and is as follows;

$$Wo = Wo + \text{delta } F \qquad 2.3.3$$

$$Worder = Wo + (Sn+1)K1 \qquad 2.3.4$$

where,

$$K1 = 1/\text{delta } T$$

This Worder is calculated between samples Sn and Sn+1. At the time Sn+1 is due to be taken Worder is delivered to the controlled oscillator for one sample period delta T. The controlled oscillator (through the selector) is set to Wo during the sample periods Sn-1 to Sn and Sn to Sn+1. Therefore upon Sn+2 Wo is substituted for Worder, this continues until the error extends beyond the phase error dead band limits and then for an additional two sample periods. Allowing error samples Sn+2 and Sn+3 to be taken to formulate the following Worder.

This procedure is repeated ad infinitum. A visual example is shown below in Figure 2.3.2.

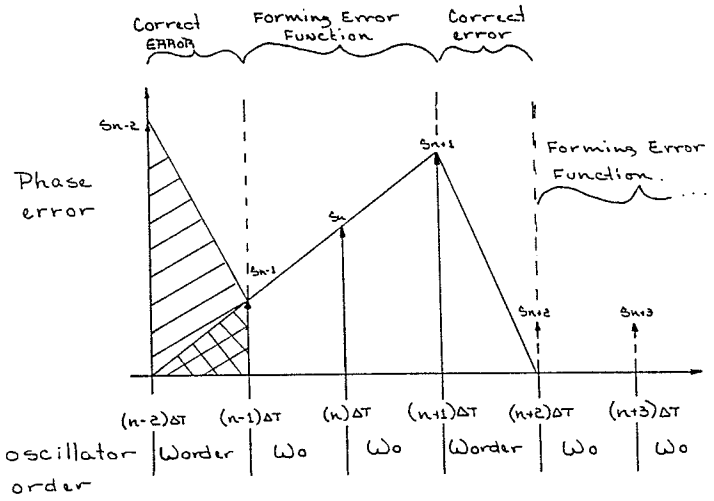

Figure 2.3.2: A visual representation of the control routine used.

In the above figure we see the phase error growing in samples Sn-1 through Sn+1. Note the hatched marks of Fig. 2.3.2; this represents a 'gray' area where errors could have existed and therefore represents the previous control action. This error could begin at any time after sample S(n-2) to S(n-1), or no error existed in this sample period where in the last two cases no control action would have taken place. Samples Sn-1 and Sn form the error function as previously discussed. Correction happens between samples Sn+1 and Sn+2. This proceedure is repeated continuously. Therefore this control routine has a maximum transient response time of 4delta T (from the time the error is linear to the time it is corrected). The program listings are contained in Appendix 'B'.

2.4 TESTS PERFORMED

Four distinct tests were performed. They are briefly described below;

1) To a balanced system a balanced phase error is applied.

2) To a balanced system a balanced frequency error is introduced.

3) To a balanced system a balanced composite error is applied (includes phase, frequency, and acceleration errors).

4A) To a balanced system a voltage unbalance is introduced.

4B) To a balanced system a unbalanced composite error is introduced (error includes phase, frequency, and acceleration).

This Section will describe these tests and results in detail.

It should be noted that no standard for testing and recording the performance of power system Phase Lock Loops (PLL) exists.

2.4.1 PLL TEST 1

This test is comprised of a balanced steady state system in lock, upon which a +/- 180 degree (+/- π radians) step phase error is introduced. The first case is 1A and is a step phase shift of +180 degrees. The input data is displayed below. Note, to represent a balanced system both the absolute magnitude and initial phase shifts of Va and Vbc must be equal (see Va and Vbc in the input file below).

FINISH,STEPT	:	0.05,0.001	(SECONDS)
INITIAL SYSTEM PARAMETERS			
FREQUENCY	:	377	(RADS/S)
VA, PHASE A	:	1.0,0.0	(P.U.,RADS)
VBC, PHASE BC	:	1.0,0.0	(P.U.,RADS)
TRANSIENT SYSTEM PARAMETERS			
START,END	:	0.01,0.03	(SECONDS)
FREQ.,ACCEL	:	377,0.0	(RADS/S,RADS/S^2)
VA, PHASE A	:	1.0,3.14159	(P.U.,RADS)
VBC, PHASE BC	:	1.0,3.14159	(P.U.,RADS)
DEAD BAND TOLERANCES			
PHASE, FREQ.	:	0.0001,0.00002	(RADS,RADS/S)

The output plot of this test is shown in Fig. 2.4.1A. Notice the error of +180 degrees appears at 10ms and is corrected at 13ms. The response is 3ms and is as expected. Note in reference to Fig.s 2.4.1A and 2.4.1B the slope at the errors leading edge does not exist; This is a peculiarity of the plotting routine (dot to dot plot). But the declining edge of the error is an accurate representation of the control action taken. The above is true for all tests involving step phase errors. Test 1B is similar except the phase step error is -180 degrees.

The input file of test 1B is exactly the same as for test 1A except the phase shifts of Va and Vbc in the transient data is negative (phase shift is -180 degrees). For this reason all further input data for tests that are similar will not be shown but differences will be explained. The output plot of test 1B is shown in Figure 2.4.1B. Again, the error is corrected in 3ms as expected.

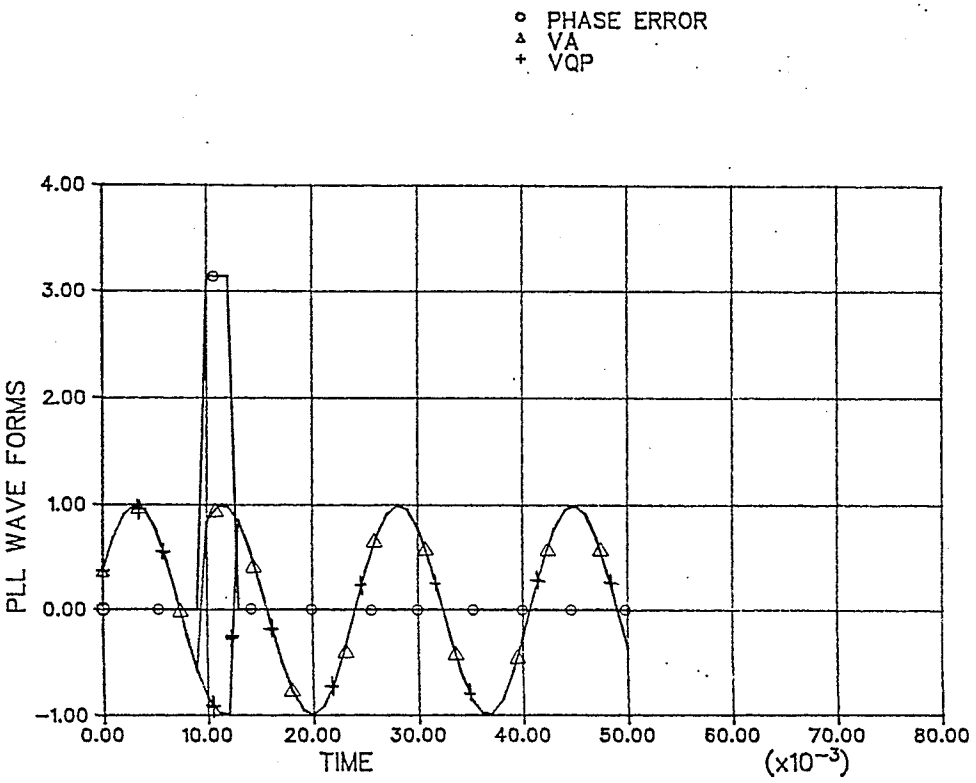

Figure 2.4.1A PLL test 1A

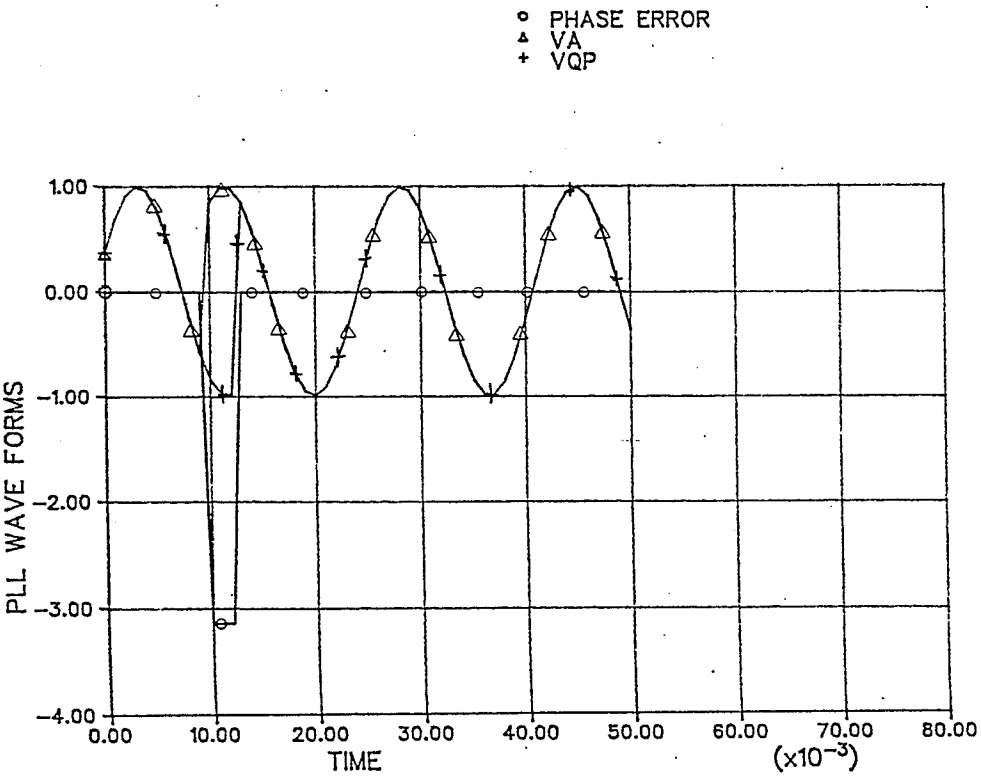

Figure 2.4.1B PLL test 1B

2.4.2 PLL TEST 2

In this test a balanced system is in lock, upon which a step frequency change is introduced. There are two parts to this test (2A and 2B). In the first case 2A the system frequency is increased by 30 Hz (60 Hz to 90 Hz). The following input data was used for test 2A;

FINISH,STEPT	:	0.05,0.001	(SECONDS)
INITIAL SYSTEM PARAMETERS			
FREQUENCY	:	377	(RADS/S)
VA, PHASE A	:	1.0,0.0	(P.U.,RADS)
VBC, PHASE BC	:	1.0,0.0	(P.U.,RADS)
TRANSIENT SYSTEM PARAMETERS			
START,END	:	0.01,0.03	(SECONDS)
FREQ.,ACCEL	:	565.4867,0.0	(RADS/S,RADS/S^2)
VA, PHASE A	:	1.0,0.0	(P.U.,RADS)
VBC, PHASE BC	:	1.0,0.0	(P.U.,RADS)
DEAD BAND TOLERANCES			
PHASE, FREQ.	:	0.0001,0.00002	(RADS,RADS/S)

The output plot is shown in Figure 2.4.2A. Notice the phase error ramping upwards linearly indicating a step frequency error. This error begins at time = 9ms and is corrected by time = 13ms. Therefore the error is corrected in 4ms. Test 2B is similar except the step frequency change is from 60 Hz to 30 Hz. Again error is corrected in 4ms as shown in Fig. 2.4.2B. From Tests 1 and 2 it is seen that phase and frequency errors are corrected within the maximum limits, of 4 delta T. Test 3 will examine the effect of a composite error being imposed.

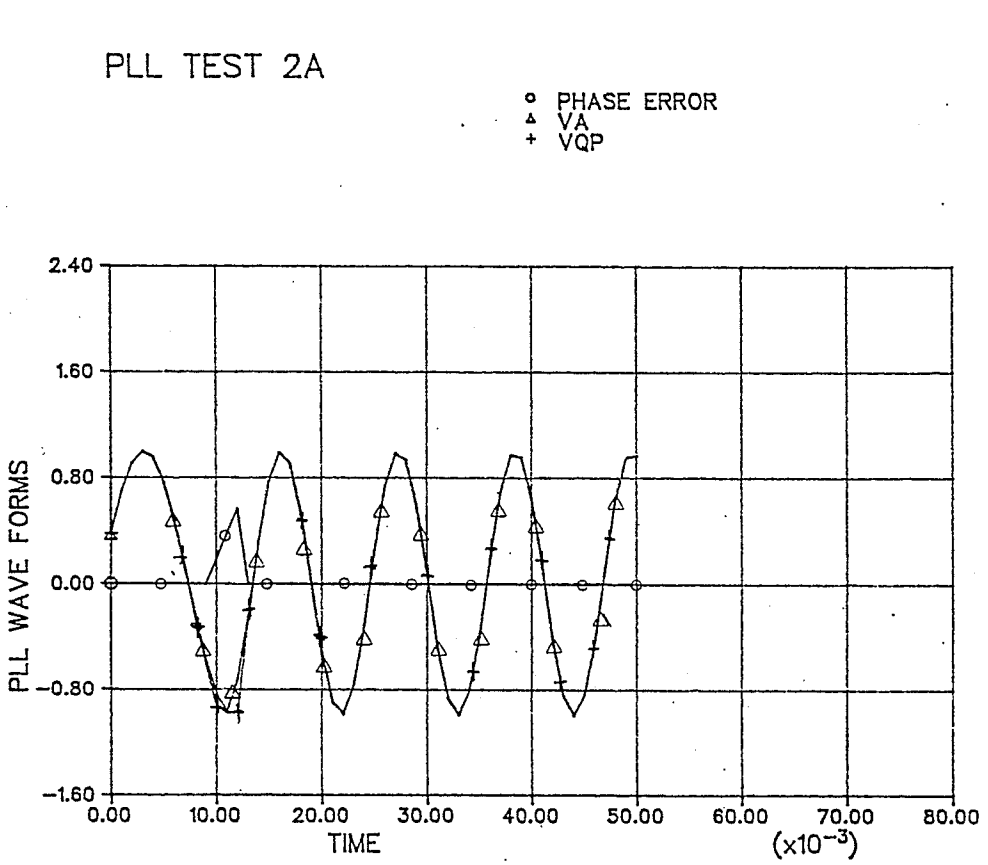

Figure 2.4.2A: PLL test 2A

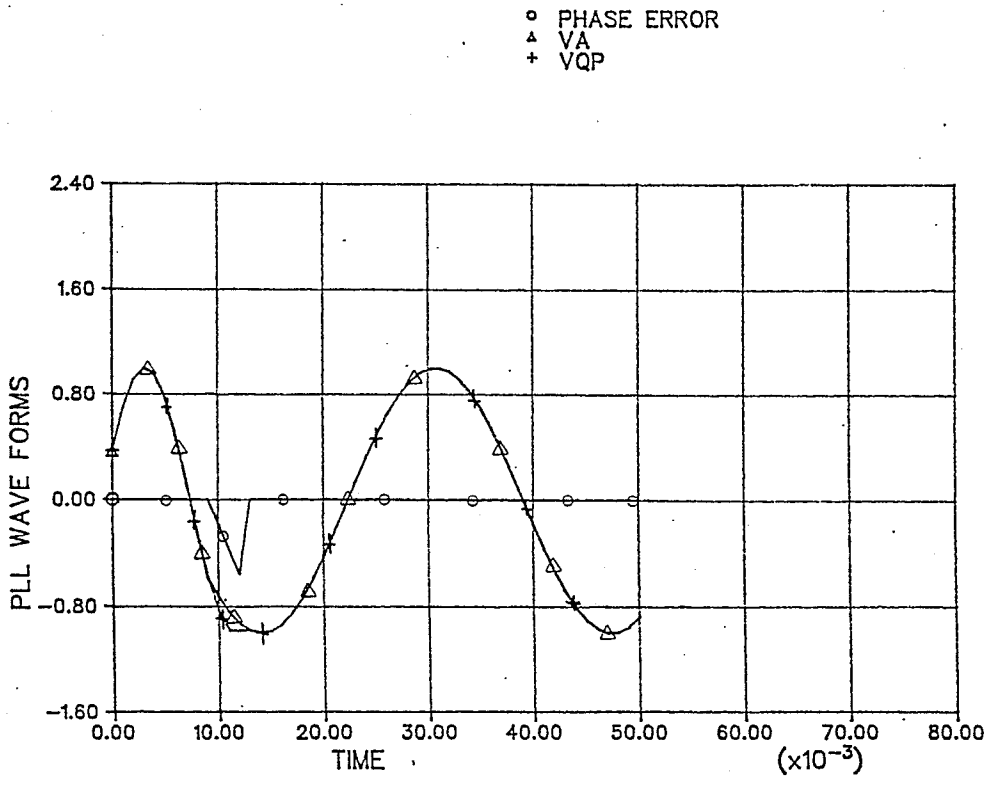

Figure 2.4.2B: PLL test 2B

2.4.3 PLL TEST 3

This test has only one part, Test 3A. A balanced system in lock is subjected to an error containing phase, frequency, and acceleration errors. The errors are a phase step of -180 degrees, frequency is increased by 30Hz (90 Hz), and a positive acceleration of 10 Hz/s is also included. The input file is detailed below;

FINISH,STEPT	:	0.05,0.001	(SECONDS)
INITIAL SYSTEM PARAMETERS			
FREQUENCY	:	377	(RADS/S)
VA, PHASE A	:	1.0,0.0	(P.U.,RADS)
VBC, PHASE BC	:	1.0,0.0	(P.U.,RADS)
TRANSIENT SYSTEM PARAMETERS			
START,END	:	0.01,0.03	(SECONDS)
FREQ.,ACCEL	:	565.4867,31.4159	(RADS/S,RADS/S^2)
VA, PHASE A	:	1.0,-3.14159	(P.U.,RADS)
VBC, PHASE BC	:	1.0,-3.14159	(P.U.,RADS)
DEAD BAND TOLERANCES			
PHASE, FREQ.	:	0.0001,0.00002	(RADS,RADS/S)

Looking to Figure 2.4.3A it is seen that this composite error is corrected in 4ms. From the above three tests it is apparent that the control algorithm works well and as predicted. Though tests 1 through 3 have only been concerned with balanced systems, the following two cases in test four will concern themselves with unbalanced errors (tests 4A and 4B).

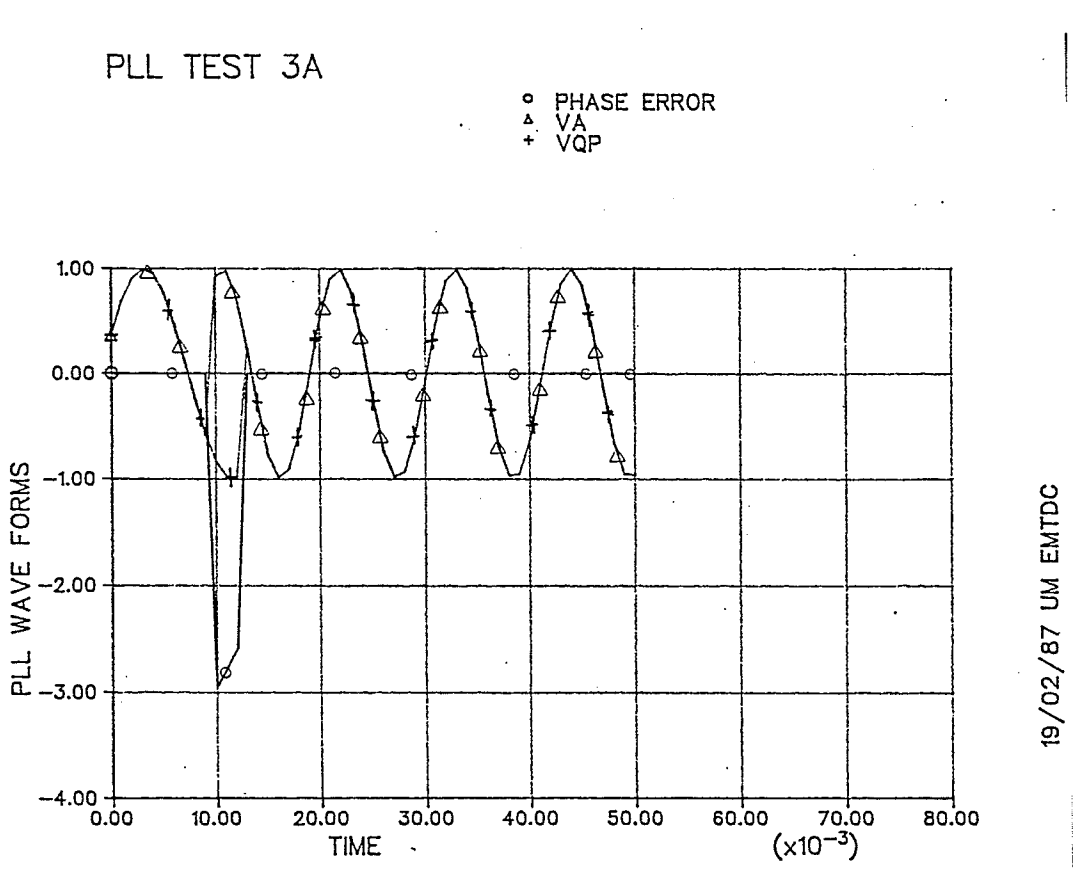

Figure 2.4.3A: PLL test 3A

2.4.4 PLL TEST 4

The power system is never ideally balanced, since loads on various phases are being switched in and out continuously. Given this it is safe to assume that the degree of unbalance in a system changes constantly. From this, test 4A was devised in which a balanced locked system is subjected to a large unbalance at time = 9ms. The positive sequence component shall remain the same but a large negative sequence component is added. The unbalance used is the same as the one used to demonstrate BBC's PLL concepts, that is a 50% negative sequence component. The input file for the test follows;

```
FINISH,STEPT    :    0.05,0.001                (SECONDS)
INITIAL SYSTEM PARAMETERS
FREQUENCY       :    377                       (RADS/S)
VA, PHASE A     :    1.0,0.0                   (P.U.,RADS)
VBC, PHASE BC   :    1.0,0.0                   (P.U.,RADS)
TRANSIENT SYSTEM PARAMETERS
START,END       :    0.01,0.03                 (SECONDS)
FREQ.,ACCEL     :    377,0.0                   (RADS/S,RADS/S2 )
VA, PHASE A     :    1.5,0.0                    (P.U.,RADS)
VBC, PHASE BC   :    0.86603,0.0                (P.U.,RADS)
DEAD BAND TOLERANCES
PHASE, FREQ.    :    0.0001,0.00002            (RADS,RADS/S)
```

One would expect if the double orthogonalization technique is valid, no phase error will occur during the course of the run. This is the case as shown in Figure 2.4.4A.

One additional test was performed. Test 2B begins with a balanced locked system and introduces the unbalance of test 4A and the composite error of test 3A. The input file is as follows;

```
FINISH,STEPT    :    0.05,0.001                (SECONDS)
INITIAL SYSTEM PARAMETERS
FREQUENCY       :    377                       (RADS/S)
VA, PHASE A     :    1.0,0.0                   (P.U.,RADS)
VBC, PHASE BC   :    1.0,0.0                   (P.U.,RADS)
TRANSIENT SYSTEM PARAMETERS
START,END       :    0.01,0.03                 (SECONDS)
FREQ.,ACCEL     :    565.4867,31.4159          (RADS/S,RADS/S2 )
VA, PHASE A     :    1.5,-3.14159               (P.U.,RADS)
VBC, PHASE BC   :    0.86603,-3.14159           (P.U.,RADS)
```

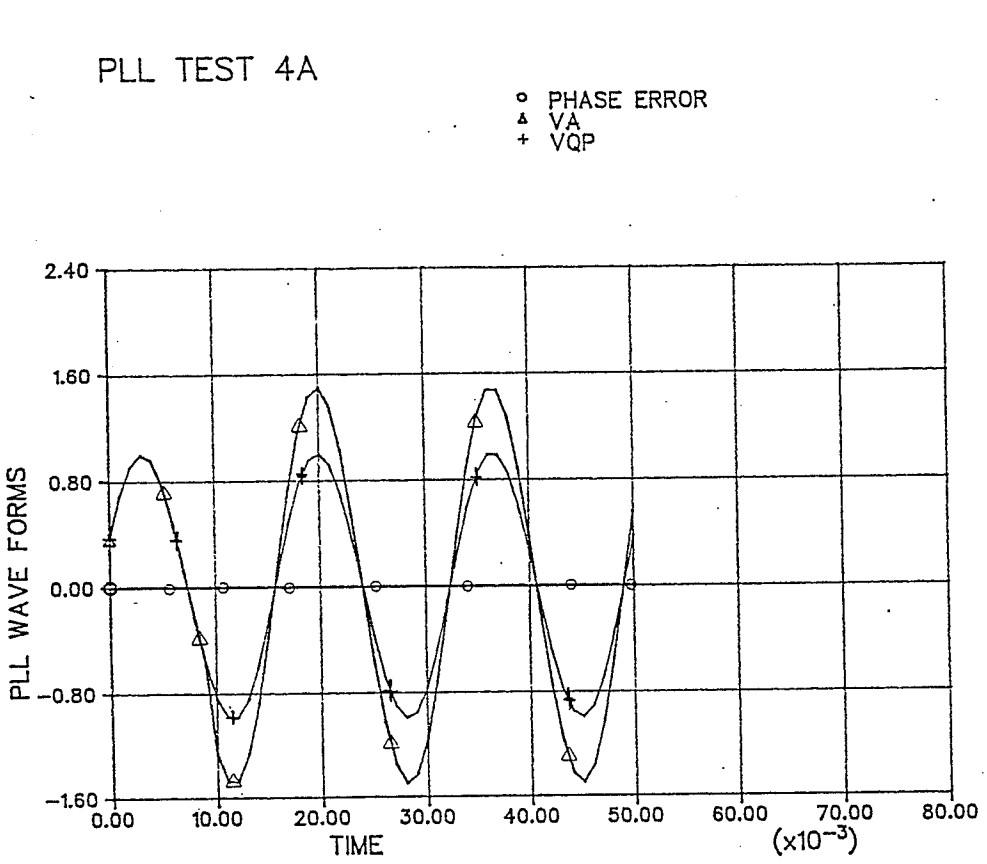

Figure 2.4.4A: PLL test 4A

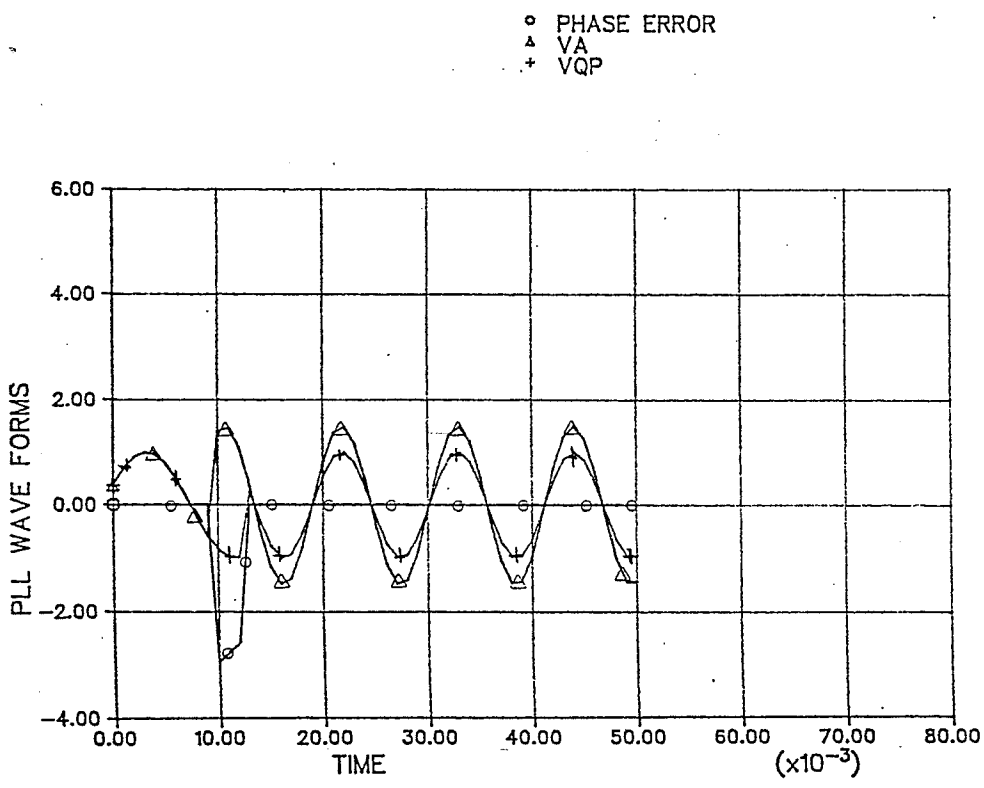

Figure 2.4.4B: PLL test 4B

DEAD BAND TOLERANCES

PHASE, FREQ. : 0.0001,0.00002 (RADS,RADS/S)

Again the error is corrected in 4ms as seen in Figure 2.4.4B. From the above four tests performed the control algorithm is shown to perform exceptionally well under ideal circumstances. In the following Chapter 3 hardware and software is constructed and integrated, which enables further tests to be performed on the University of Manitoba's Analog HVDC Simulator.

CHAPTER 3

HARDWARE AND SOFTWARE DEVELOPED

3.1 INTRODUCTION

This Chapter will present the construction of hardware and software used to implement the Digital Phase Lock Loop (DPLL). Due to the complexity of these components the DPLL will be broken up into blocks which will each be explained briefly (see Fig. 3.1.1 below). A more detailed explanation is contained in the "DPLL TECHNICAL MANUAL" (see reference 3).

During the course of this Chapter continued reference will be made to Fig. 3.1.1. An overall description of the block diagram is followed by: a detailed explanation of each block, a description of the developed software routines, a list of the hardware/software tests performed, tests results, and an overview of the realized DPLL.

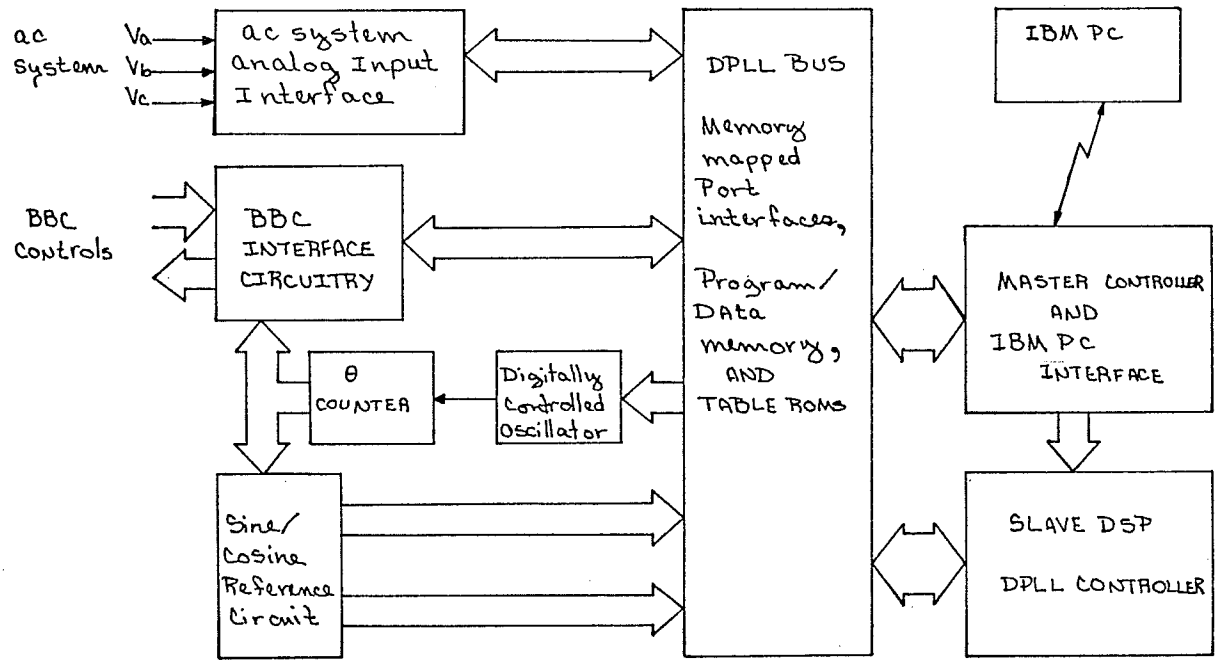

Figure 3.1.1: System block diagram

3.2 SYSTEM HARDWARE CONSIDERATIONS

This Section describes the system blocks and how they are associated with each other. An explanation will be presented as to why this configuration was selected.

The ac system analog input block conditions the analog voltage signals to be processed digitally. Inputs and outputs provided by the BBC interface match those of BBC's Phase Lock Loop. The Theta counter, Digitally Controlled Oscillator (DCO), and Sine/Cosine reference form the loop's main components. All the above blocks including the DPLL bus are lumped together as the DPLL's resources. A human interface to these resources is provided through the Master Controller and IBM PC interface block. Through this block DPLL programs and data are down loaded into the DPLL's main memory (DPLL bus block). It also allows all of the system resources to be tested or modified. A Digital Signal Processor (DSP) is used to execute the actual phase lock loop algorithms and is a slave to the Master Controller. When running PLL programs the DSP has full control of all the system resources, except those of the Master Controller. This configuration allows flexibililty in debugging and commissioning of programs and hardware.

The DSP was selected to run these programs because of its execution speed and the fact that a hardware multiplier is integrated on the same chip. Due to its speed and limited addressing capability an additional microprocessor was added to provide liaison between the DPLL and an IBM PC. It is interfaced to the IBM PC to facilatate the human interface as well as to allow the DSP's cross assembled files (programs assembled on the

IBM PC) to be down loaded into the DSP's memory.

The BBC interface was selected to allow comparison testing of the DPLL and BBCs PLL. In addition this interface will allow operation of this DPLL within BBC controls. The following Sections take a closer look at each individual block of Fig. 3.1.1.

3.2.1 AC SYSTEM ANALOG INTERFACE

The ac system analog input interface is shown in Fig. 3.2.1. The three ac system voltages Va, Vb, and Vc are input at the left. The first step of conditioning involves the removal of any zero sequence components that may be present. This is followed by an analog three-to two-phase transformation. The two voltage signals Va and Vbc are filtered by programmable switching capacitor filters, which remove any system harmonics. Each voltage signal is fed to a sample and hold circuit feeding a 12 bit Analog to Digital Converter (A/D or ADC). Both signals are then fed to slope and peak detecting circuits, which provide the necessary information to perform the waveform orthogonalization required. These programmable switching capacitor filters are programmed by an input frequency that is 100 times the desired cutoff frequency (FCO) provided by the FCO DCO. The cut off frequency is matched to the system frequency and is measured by a zero crossing detector and timer circuit. The bus interface maps these signals into the DPLL resources.

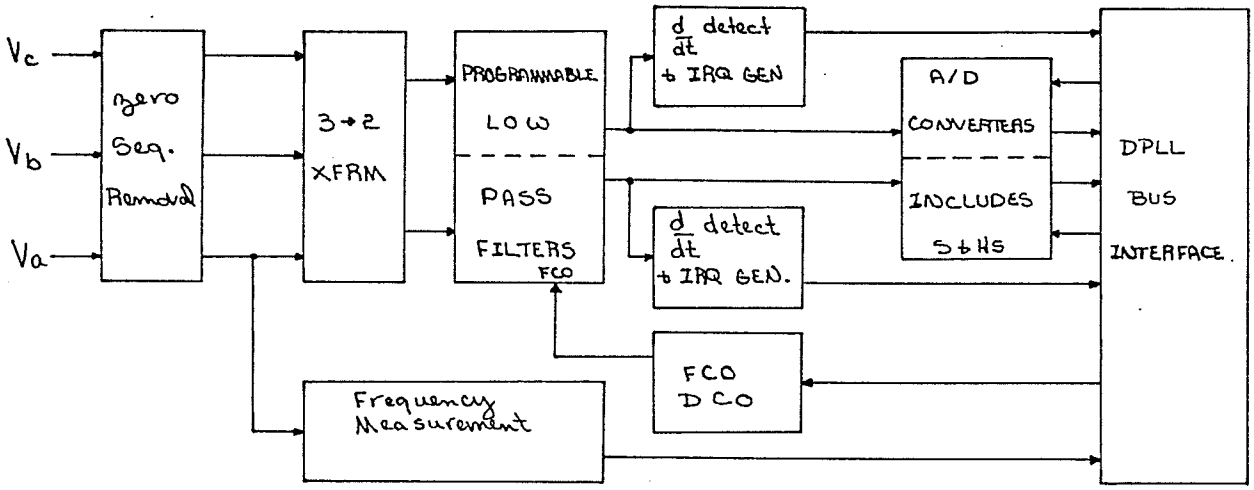

Figure 3.2.1: Analog input interface.

3.2.2 THE BBC INTERFACE

The BBC interface circuit is a simple one providing input and output control signals matching those of BBCs PLL (See Fig. 3.2.2). The design provides for four input signals: Freeze, Fast, Slow, and Ensync. These signals are directly interfaced on the DPLL bus. The outputs consist of Fast and Syn for control and the full spectrum of synchronization signals: A0+/-, A30+/-, B0+/-, B30+/-, C0+/-, and C30+/-. The control outputs are directly interfaced to the bus. The synchronization signals are derived from the most significant four bits of the 12 bit Theta counter through a pattern rom decoder. In addition all input and output signals are level translated to match BBCs signal levels.

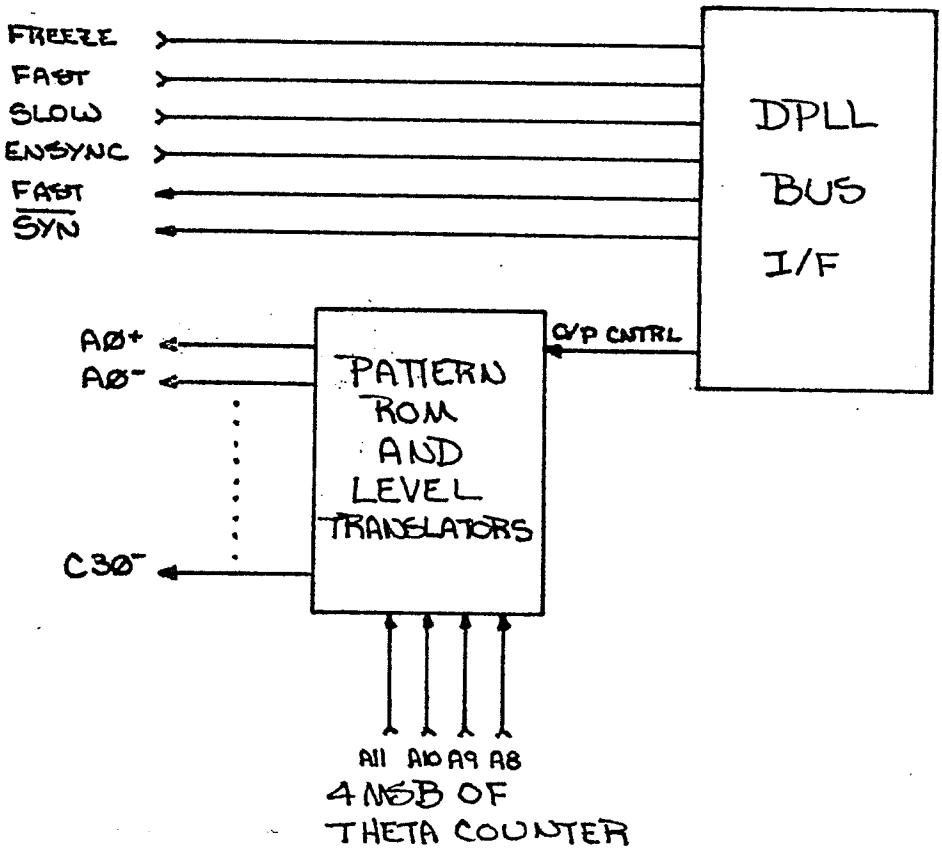

Figure 3.2.2: The BBC Interface

3.2.3 THE MAIN LOOP COMPONENTS

The main loop components consist of the Theta counter, PLL DCO, and Sine/Cosine reference. These components form the heart of the DPLL. In Fig. 3.2.3 below these blocks are expanded.

The Theta counter accepts count pulses from the PLL DCO. It is a 12 bit counter that divides by 3072 to provide easy three-phase waveform decoding. This 12 bit counter provides an address for the Sine/Cosine reference roms (equates to theta) and the BBC synchronization decoder rom. The Sine/Cosine data patterns are 12 bit resolution and feed seperate digital samplers.

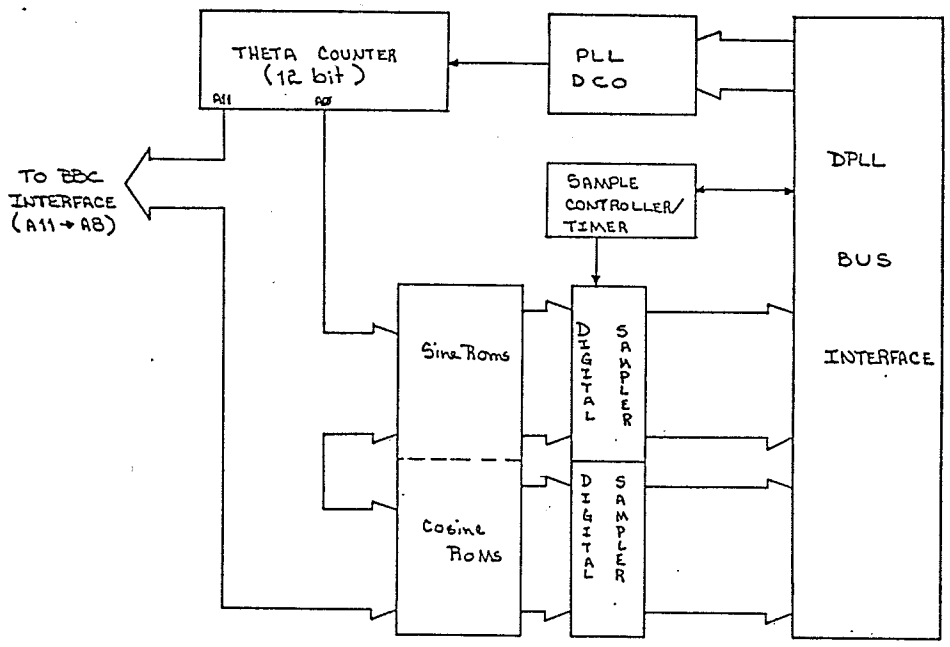

Figure 3.2.3: The main loop components

The sample controller/timer provides a constant sample rate of 1 millisecond and synchronizes data sampling throughout the system. The rom data sampled is then fed to the DPLL bus interface. The PLL DCO makes use of a high frequency crystal oscillator (18.432 MHz). By dividing this frequency it provides the desired result. Being digital the input/output characteristic is not linear nor continuous (See Fig. 3.2.4). The output frequency can be selected in steps of 0.01 Hz (the error varies with each selected frequency).

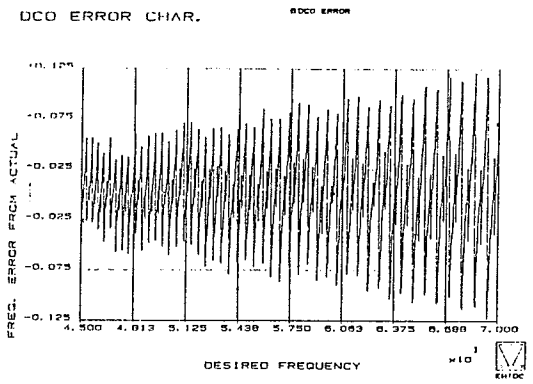

Figure 3.2.4: Input/Output characteristic of DCO

Futher information on this oscillator is contained in the "DPLL Technical Manual". This oscillator is interfaced through software and the DPLL bus interface.

3.2.4 THE DPLL BUS INTERFACE

This block contains the DPLL's system memory, port decoding, table ROMs, and interupt logic (See Fig. 3.2.5). The system memory is organized as 4096 by 16 bit wide words. Eight 16 bit wide input and output ports are decoded, which provides the interface to the previously described blocks and the data table ROMs. The interrupt logic decodes eight priorized interrupt levels.

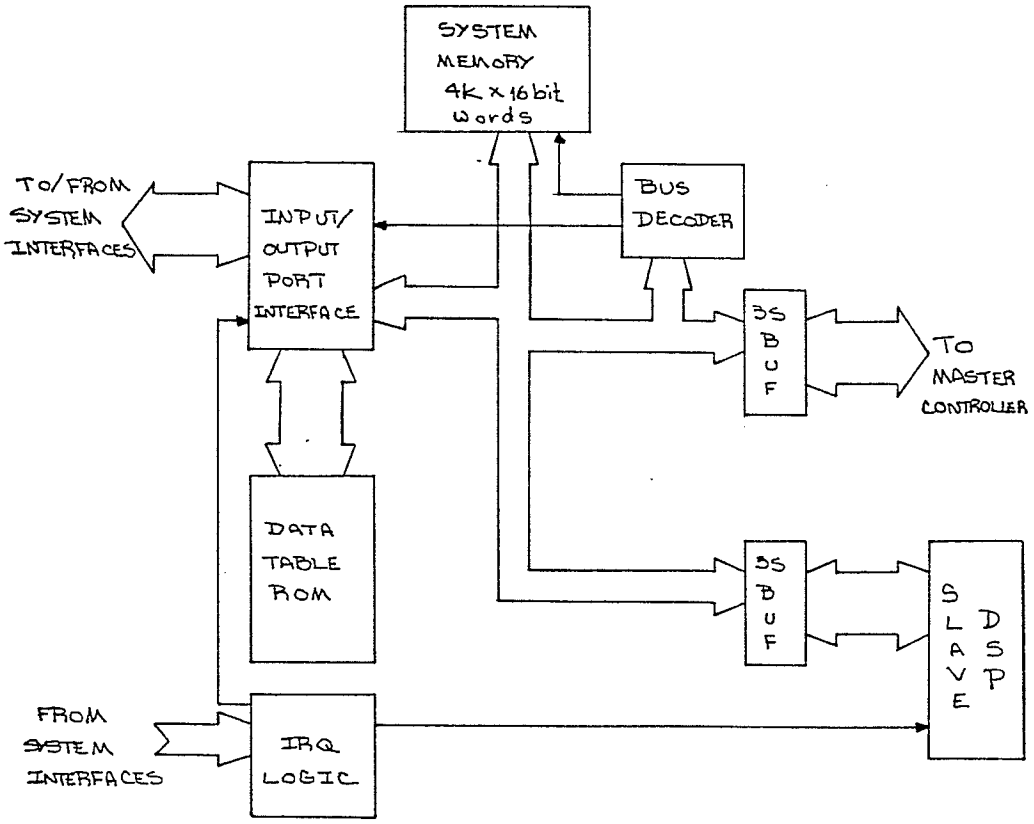

Figure 3.2.5: DPLL Bus Interface components

This block is seperated from the Master Controller and Slave DSP by a set of tri-state buffers to ensure that only one of them has control of these resources at any one time.

3.2.5 THE MASTER CONTROLLER

The Master Controller and IBM PC interface block is expanded in Fig. 3.2.6 below. The Master Controller determines which processor (DSP or Master Controller) has control of the DPLL bus.

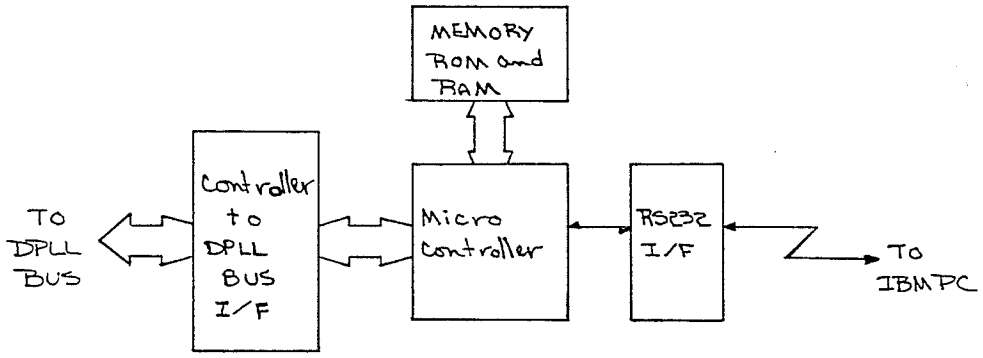

Figure 3.2.6: The Master Controller

It is a small system providing an optically coupled RS-232 port to the IBM PC and an 8 to 16 bit bus interface to the DPLL bus. The assembler coded translator program is stored in EPROM. This firmware can be configured to talk to an IBM PC or to a terminal. The program and more details are contained in the "DPLL TECHNICAL MANUAL" [3].

3.2.6 THE SLAVE DIGITAL SIGNAL PROCESSOR

This is a simple block consisting of the processor clock, DSP, and tri-state buffers separating the DSP from the DPLL bus. The Master Controller controls these buffers as well as

the DSP reset pin. Hence the DSP becomes a slave to the Master Controller and is used solely to run DPLL programs. The following Section describes the software modules that consolidate the above hardware into a system.

3.3 SYSTEM SOFTWARE CONSIDERATIONS

The system software can be broken up into three parts the IBM PC, Master Controller, and DPLL software. Each of these software modules will be briefly explained in the following Sections.

3.3.1 IBM PC SOFTWARE

The IBM PC software interface to the Master Controller was written in Pascal for simplicity. This enabled disk files to be accessed easily and down loaded through the Master Controller via an RS-232 serial link. The IBM PC helped create a pleasant human interface. This software allows the following commands:

T - TEST MEMORY

V - VIEW MEMORY

M - MODIFY MEMORY

R - READ A PORT

W - WRITE A PORT

G - GO (RUN A PROGRAM)

L - DOWN LOAD A XASM FILE

Q - QUIT

Test Memory ('T') - Verifies that the DPLL's memory is functioning properly.

View Memory ('V') - Allows 64 words of the DPLL's memory to be displayed at one time.

Read a Port ('R') - Enables any one port of the eight to be read.

Write a Port ('W') - Enables any one port of the eight ports to be written to with a specified hex value.

Go ('G') - Transfers control of the DPLL's resources to the slave DSP.

Down Load a file ('L') - Allows files created by the cross assembler installed on the IBM PC to be loaded into the DPLL's memory.

Quit ('Q') - Returns control to the IBM PC's operating system.

This software proved to be most helpful for developing and debugging software for the DPLL.

3.3.2 MASTER CONTROLLER SOFTWARE

This software is written in assembler code and provides the basic routines used to implement the commands set out in Section 3.3.1. The core routines involve the following: translate ASCII characters to hex and hex to ASCII, routines to time memory accesses to and from the DPLL's memory, and routines to manipulate the DPLL's memory. This monitor can be assembled for either IBM PC or terminal operation. In the following Section the support subroutines for the DPLL are described.

3.3.3 DIGITAL PHASE LOCK LOOP SUPPORT SUBROUTINES

In this Section only the subroutines common to all PLL will be presented. These subroutines consist of the routines used to interface the hardware and software as well as math functions such as divide and square root. These routines can be thought of

as PLL building blocks which allow the user to modify PLL characteristics. Each of these routines will be briefly explained here. For details see the "DPLL TECHNICAL MANUAL" [3].

The main subroutines are listed below with an accompanying description.

PORT INITIALIZATION ('PRTINIT'): This routine is designed to initialize all the ports and hardware interfaces.

CONSTANT INITIALIZATION ('CONINIT'): Initializes all the constants that are used by the support subroutines (eq π , $\pi/2$, etc.).

INTERUPT SERVICE SUBROUTINE ('IRQSRV'): This subroutine contains all the routines required to service the interupt service requests and synchronize the software to the hardware. These routines interface the sample timer (1 ms clock), analog to digital converters, peak/slope detectors, zero crossing detector, and the BBC interface signals Freeze and Fast.

SQUARE ROOT SUBROUTINE ('SQROOT'): This routine accepts a 30 bit positive number and by successive approximation determines the square root to the nearest least significant bit (15 bit result).

DIVIDE SUBROUTINE ('DIVIDE'): This routine allows a 16 bit number to be divided by another 16 bit number producing a result with a user defined accuracy.

OMEGA OUT ('WOUT'): 'WOUT' Allows the PLL DCO to be interfaced by passing a frequency to this routine. The corresponding values for the PLL DCO are calculated. These values represent the closest frequency to the actual.

ORTHOGONALIZATION (ORTHO): This routine takes a value from one of the ADC's and its slope and produces the equivalent orthogonal component.

SINE/COSINE ('SINCOS'): This subroutine reads the PLL reference roms and adjusts them to be processed.

DATA PREPERATION ('PREPDAT'): It makes use of 'ORTHO' and 'SINCOS', to prepare all the vectors for calculation of the phase error.

CPC SUBROUTINE ('PHERR'): This routine accepts the data prepared by 'PREPDAT' and produces a phase error in radians.

The above routines provide the interface software to the system hardware as well as some common PLL building blocks. Several other blocks that were developed are not mentioned here, but can be found in the "DPLL TECHNICAL MANUAL".

3.4 HARDWARE AND SOFTWARE COMMISSIONING

Several tests and calibration procedures have been performed to ensure proper operation. These commissioning procedures will be outlined with results.

3.4.1 MASTER CONTROLLER COMMISSIONING

The Master Controller was first commissioned by connecting it to a terminal. This verified that the RS-232 serial link was working properly. The DPLL's memory was installed and tested, as were the ports. Both the memory and port tests were successful which completed the Master Controller commissioning. Later it was interfaced to an IBM PC and that software was verified. This now allowed full control of the DPLL resources.

3.4.2 ANALOG INPUT CIRCUITRY COMMISSIONING

The zero sequence removal circuits were calibrated first. Then the three-to two-phase conversion operational

amplifiers were calibrated and were verified correct. The programmable low pass switching filters were tested. Here problems arose. These particular filters from National worked fine in preliminary bench tests; but, when they were inserted in the circuit an abnormal amount of DC drift was experienced. A host of possible solutions were attempted, but these yielded no satisfactory results. It was decided at this time to exclude these filters. This would have an impact of being unable to tolerate harmonics in the input waveforms.

The ADC and Sample and Hold (S/H) circuits were inserted and calibrated successfully. The next crucial task was to install and calibrate the peak and slope detectors. These have worked marginally well but problems arose in detecting the exact peak and slope repetitively. Part of this problem is attributed to the filters that could not be installed. The peak/slope detector is essentially a differentiator which is sensative to noise spikes. The absence of the filters and the instability of the peak/slope detectors has been the main cause of concern throughout this project.

One possible solution to these problems could be to implement the filters and peak/slope detectors in software.

3.4.3 THE DIGITALLY CONTROLLED OSCILLATORS

The first one tested was the FCO DCO, which is a simple programmable counter/divider. This circuit worked the first time. The PLL DCO had one minor problem with propagation delays, but it was quickly corrected with software. Both oscillators work fine and posed no problems to the DPLL's operation.

3.4.4 SAMPLE TIMER COMMISSIONING

This circuit was first tested ignorant of the problems with the PLL DCO. So it was initially thought to be in error. After the PLL DCO was corrected it worked fine. This commissioned the last of the main loop components.

3.4.5 SLAVE DIGITAL SIGNAL PROCESSOR COMMISSIONING

In this test small programs were written, inserted into the DPLL's memory, and run. Proper operation was verified the first time through. From here numerous cases were run to verify that all the above mentioned subroutines (Section 3.3.3) worked properly.

3.4.6 BBC INTERFACE COMMISSIONING

No problems in commissioning this block was experienced. However a programming error in the pattern rom was discovered and corrected.

3.5 OVERVIEW OF DPLL REALIZED

The overall hardware and software components work reasonably well. The peak and slope detectors have created stablility problems, with momentary jitters that affect tracking (once every three to five cycles). The selected Digital Signal Processor uses integer arithmetic which has posed some problems. It limited the range of possible gains and produced rounding errors. It should be noted that floating point DSPs were not available at the time of conception. These would have been the best choice in implementing the DPLL. They would have simplified the software and increased the possible performance of the DPLL.

CHAPTER 4

SIMULATOR TESTS

4.1 INTRODUCTION

This Chapter will present two DPLL algorithms tested on the University of Manitoba's HVDC Simulator. These tests and their apparatus will first be explained, followed by a description of the two algorithms. The Chapter ends with a detailed discussion of the results obtained.

4.2 TESTS AND APPARATUS

In this Section the two tests performed on the University of Manitoba's HVDC simulator are explained. In addition the apparatus used to implement these tests is described.

4.2.1 BASIC CONFIGURATION OF TEST APPARATUS USED

It was decided that the BBC PLL should be wired in parallel with the prototype DPLL, enabling comparison testing. The comparison will be made using the positive going zero crossing of the positive sequence component of phase A. This is represented by the output A0+ on both circuits. The results of these tests were recorded by an Ultra Violet light (UV) recorder. The input waveforms Va, Vb, and Vc as well as the output waveform A0+ from both the BBC PLL and the DPLL under test (five waveforms in total) were recorded. The UV recorder is triggered by a programmable switch. This switch triggers the UV recorder approximately one cycle before the transient is applied and disables the recorder several cycles after the transient is removed. A block diagram of this configuration is shown in Fig. 4.2.1.

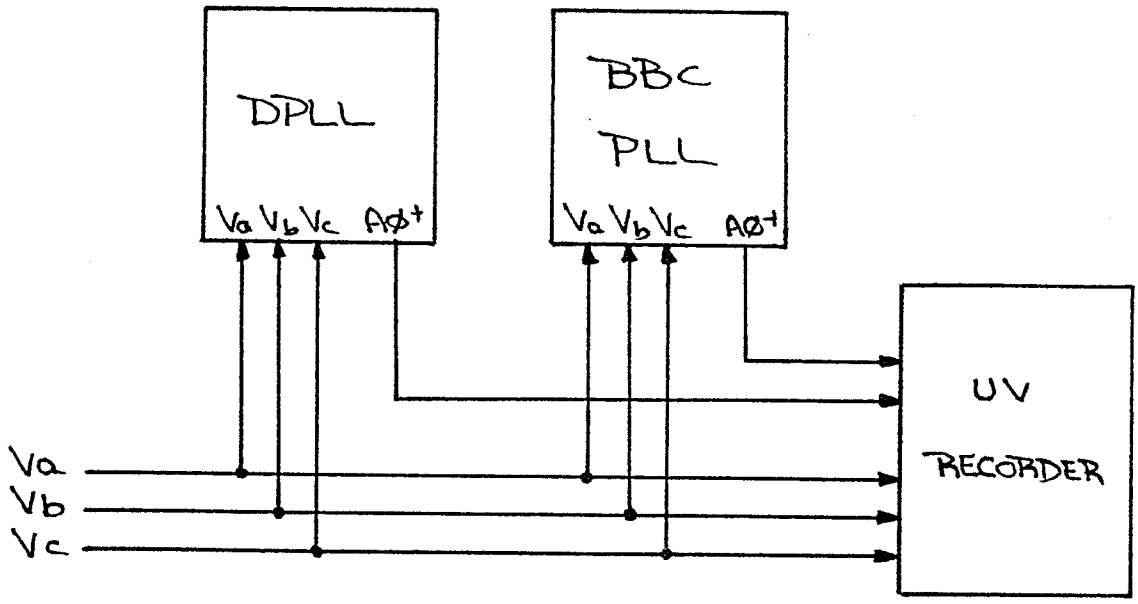

Figure 4.2.1: Block diagram of test apparatus

The two transient tests performed are as follows;

1]. A 180 degree phase shift

2]. A step unbalance is applied

The apparatus for each of the above tests is discussed in the following Sections.

4.2.2 THE 180 DEGREE PHASE SHIFT TEST

The apparatus for this test is very simple and is shown in Fig. 4.2.2 below.

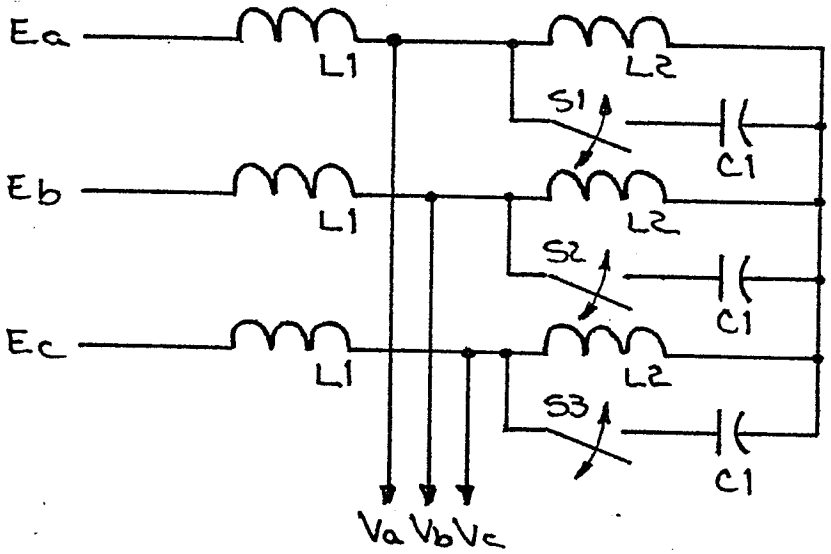

Figure 4.2.2: Configuration of 180 degree phase shift test

This circuit is supplied by a balanced three phase waveform (Ea, Eb, and Ec). The three switches S1, S2, and S3 are closed initially. At time To these switches are opened simultaneously creating a 180 degree phase shift (in steady state). The switches are held open for a time Tc and are reclosed at time To + Tc. The effect of closing and opening these switches is shown in the calculations below;

Let L1= 4H
L2= 2H
C1= 10uF

and X1= jwL1
X2= jwL2
X3= -j/wC1

,where w= 377 rad./s.

Then for the switches open;

$$Va = EaX2/(X1+X2) = Ea/3 \angle 0^{\circ}$$

Similarily for Vb and Vc;

$$Vb = Eb/3 \angle -120^{\circ}$$

$$Vc = Ec/3 \angle 120^{\circ}$$

And for the switches closed;

$$Va' = Ea(X2||X3)/((X2||X3) + X1) = 0.3724\ Ea \angle 180^{\circ}$$

Similarily for Vb and Vc;

$$Vb' = 0.3724\ Eb \angle 60^{\circ}$$

$$Vc' = 0.3724\ Ec \angle -60^{\circ}$$

4.2.3 THE UNBALANCED VOLTAGE TEST

The apparatus for this test is shown in Fig. 4.2.3.

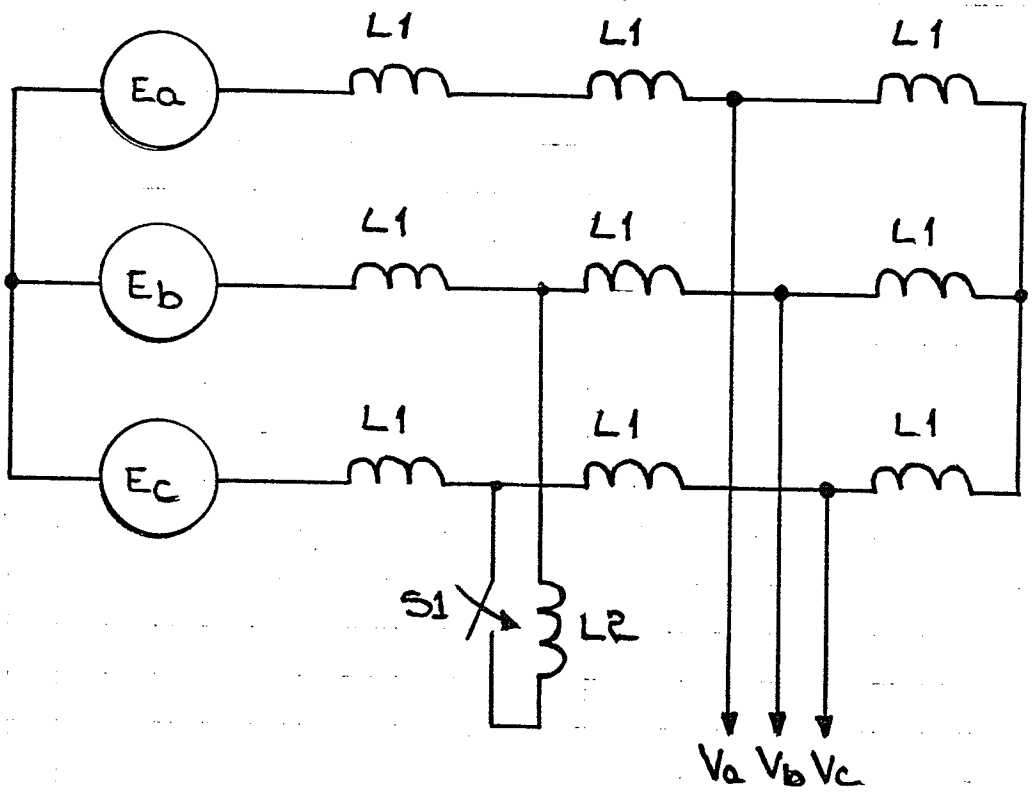

Figure 4.2.3: Unbalance test apparatus

This circuit is supplied by a balanced three-phase source (Ea, Eb, and Ec) and differs from Fig. 4.2.2 in that the source impedance has been divided equally and the load impedance is not switched. One switch (S1) is used to introduce the unbalance by shorting phases b and c through an inductor (L2). The switch is initially open creating a balanced three phase voltage waveform on the outputs Va, Vb, and Vc. At time To the switch is closed creating an unbalance on the voltage outputs. This switch (S1) is held closed for a time Tc, and at time To + Tc the switch is reopened.

The UV recorder is triggered with an additional programmable switch (St). This trigger switch starts the UV recorder approximately two cycles before time To and stops the UV recorder several cycles after time To + Tc. This ensures that all of the test waveforms are captured.

The effect of closing and opening switch S1 is calculated below.

Let L1 = 2H
L2 = 5H

and X1 = jwL1
X2 = jwL2

,where w = 377 rad./s.

Now for switch S1 open; we have as before Va = Ea/3, Vb = Eb/3, and Vc = Ec/3. When switch S1 is closed the mesh equations derived from Fig. 4.2.4 can be solved, yeilding with respect to the neutral of the supply:

Va = 0.3332 $\angle 0^{\circ}$ p.u. voltage

Vb = 0.2516 $\angle -131.6^{\circ}$ p.u. voltage

Vc = 0.2514 $\angle 131.5^{\circ}$ p.u. voltage

And finally extracting the positive and negative sequence components;

V+ = 0.2754 $\angle 0^{\circ}$ p.u. voltage

V- = 0.0581 $\angle 0^{\circ}$ p.u. voltage

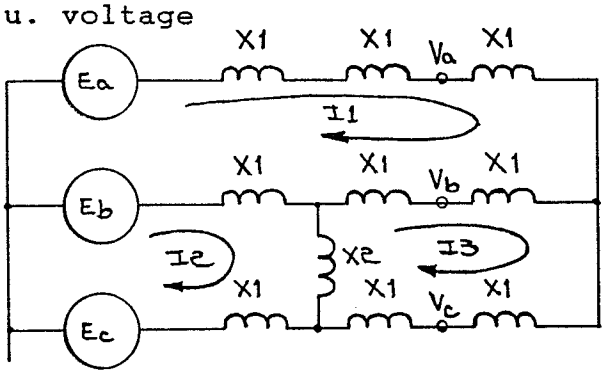

Figure 4.2.4: Mesh equations equivalent circuit

As seen from above the positive sequence component (V+) is only changed in magnitude when switch S1 is closed. Therefore the positive sequence component can still be tracked by the output A0+ of both PLLs (BBCs and the DPLL).

4.3 DPLL ALGORITHMS TESTED

This section will present the two DPLL algorithms selected for testing on the HVDC Simulator. The first is the algorithm discussed in Section 2.3. Followed by an algorithm based on a digital integration technique.

4.3.1 PREDICTOR CORRECTION ALGORITHM

During the course of this discussion continual reference to Section 2.3 will be made. This algorithm is the same as the one presented previously with one minor modification. The gains K1 and K2 are now variable. The program listings of the algorithm can be found in the "DPLL TECHNICAL MANUAL" under Predictor Correction Method ("FSTTST1.ASM").

This algorithm posed some serious stability problems during the tests due in part to the hardware problems discussed in Chapter 3. It tracks the input waveform very poorly. Typically having violent oscillations about the tracking point, regardless of the remedies attempted. It is for these reasons that this algorithm is dropped from further discussion.

4.3.2 INTEGRATING PLL ALGORITHM

This algorithm is closer to the standard PLL techniques used presently. It is a second order feedback control system. A block diagram of the control loop is shown in Fig. 4.2.1.

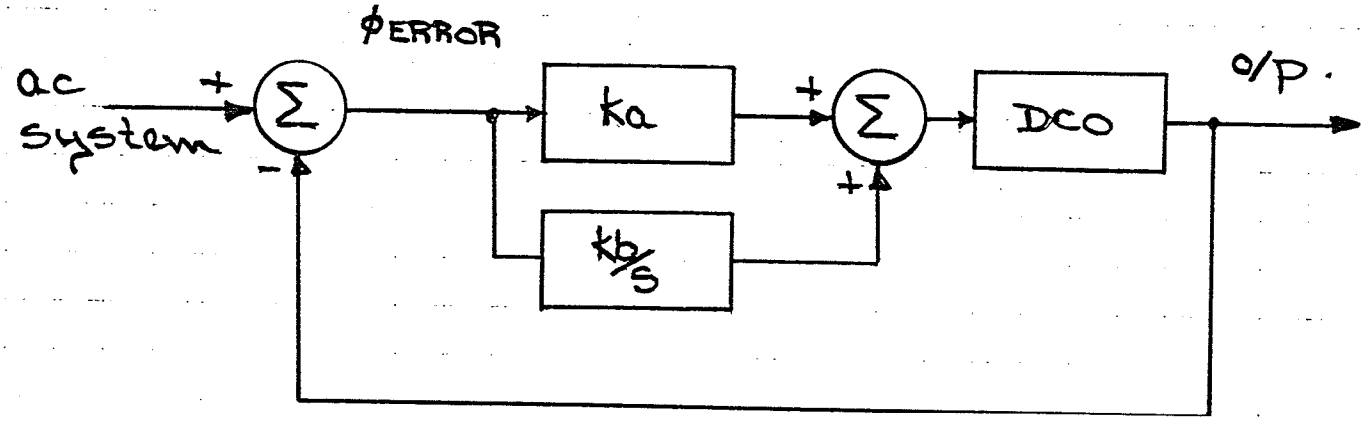

Figure 4.3.1: Integrating PLL block diagram

The phase error (ϕ error) is determined as before with the "Double Othogonalization" technique described in Section 1.4. This error feeds both a digital integrator with variable gain Kb and an all-pass filter with variable gain Ka. The output of these two branches is then summed. This sum provides an input to the PLL Digitally Controlled Oscillator (DCO). The output frequency is fed (through the theta counter) back to the phase detector completing the loop.

The integrator uses the trapezoidal rule which is simple and stable that is:

$$Kb/s = \left[\sum_{n=1}^{i} (Sn + Sn-1)/2 \right] Kb \qquad 4.3.1$$

,where Sn = present error

Sn-1 = the previous error

This algorithm is very fast and stable (see "FSTTST.ASM" in the "DPLL TECHNICAL MANUAL" [3]).

4.4 TESTS PERFORMED

The apparatus and basic tests to be performed have been outlined in Section 4.2. This Section will discuss the results obtained using the Integration technique and compare its performance with that of the BBC PLL. The tests will be discussed in the following order;

1] A 180 degree phase shift

2] A step unbalance

4.4.1 THE 180 DEGREE PHASE SHIFT TEST

In this test the BBC PLL is locked into the fast mode of operation. The phase shift error is introduced to the PLLs as described in Section 4.2.2. The UV recordings of each test will first be presented followed by a discussion of the results. In Fig. 4.4.1 a phase shift of 180 degree is introduced to a balanced and locked system. This figure records the performance of both PLLs.

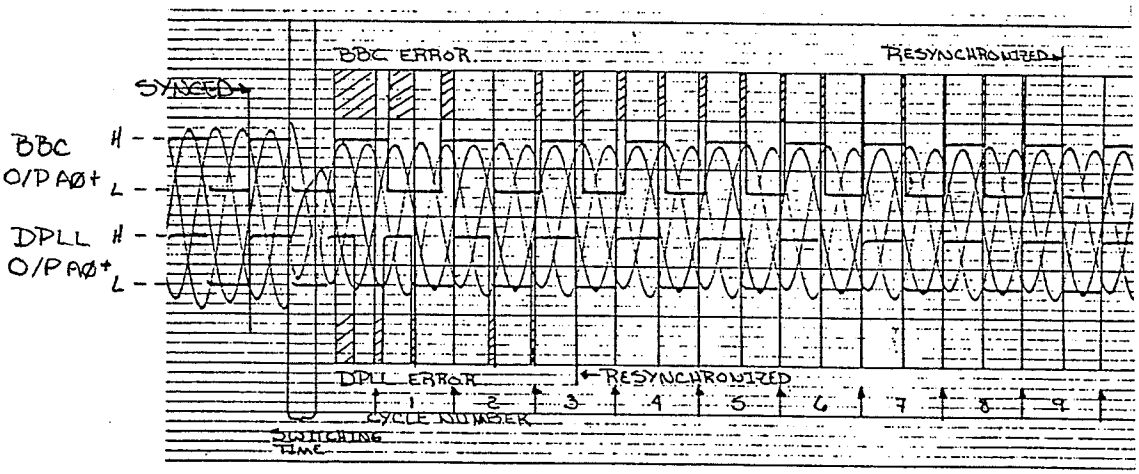

Figure 4.4.1: A 180 degree phase shift is introduced

The DPLL's A0+ is the bottom square wave while the BBC A0+ is the top square wave recording. From this figure the DPLL resynchronizes to the shifted waveforms in approximately 4 cycles and while the BBC PLL takes 9 cycles. This is measured from the time the disturbance becomes stable until the PLL tracks with zero error.

The UV recording of Fig. 4.4.2 shows an interesting characteristic of both PLLs. Notice the square wave outputs for both PLLs in the first two cycles after the disturbance. The frequency of the two square waves is somewhat less than that of the system. This is due to the architecture of these loops. They both employ a theta counter which counts in only one direction. Given this we see the local oscillators are slowing down to allow the system to "catch up", producing a slower transient response time. If one used a theta counter that could count down as well as up the transient response time could be improved significantly. In other words the PLL could back up to catch the system waveforms, instead of having to wait for them.

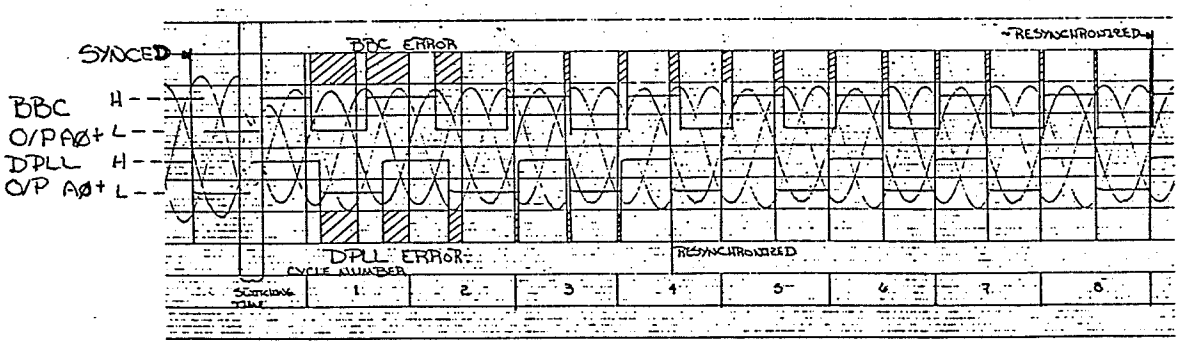

Figure 4.4.2 A 180 degree phase shift being applied

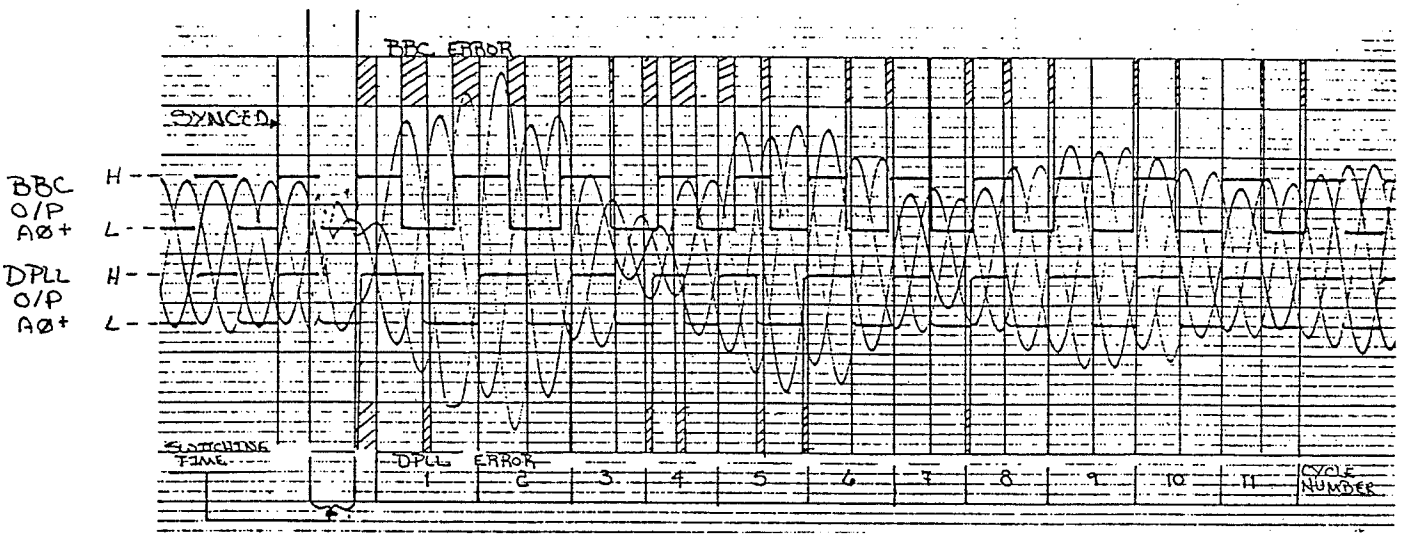

Figure 4.4.3: A 180 degree phase shift being removed

In Fig. 4.4.3 the 180 degree phase shift of Fig. 4.4.1 is removed. The over voltage experienced is due to the parallel capacitors being reinstated. This figure is presented to demonstrate how each PLL handles these over voltages.

Notice cycle number 3, of Fig. 4.4.4 where the voltages dip to a low level. The DPLL has trouble in this area, because of the double orthogonalization technique employed. Since it requires the peak and slope of the waveforms. When the peaks dip to such a low level only a small percentage of the 12 bit ADC resolution can be used, and this introduces error.

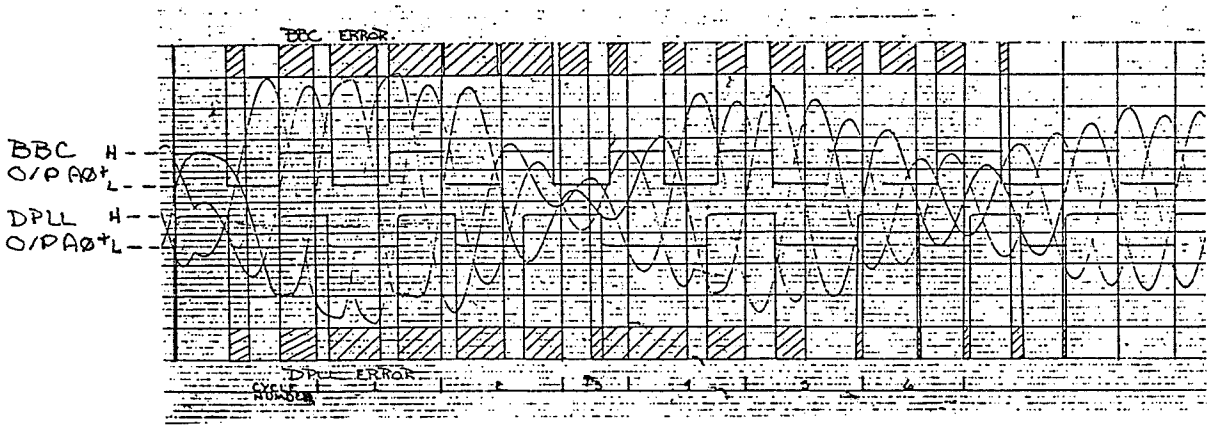

Figure 4.4.4 A 180 degree phase shift removed.

Overall the DPLL performance is quite good in comparison to the BBC PLL.

4.4.2 THE UNBALANCED VOLTAGE TEST

In this test the BBC PLL is again locked into the fast mode of operation. The unbalance is introduced to the PLLs as descibed in Section 4.2.3. As in Section 4.4.1 the UV recordings will be presented first followed by a discussion. In Fig. 4.4.5 below an unbalance of 21% negative sequence voltage is introduced and the performance of both PLLs is displayed.

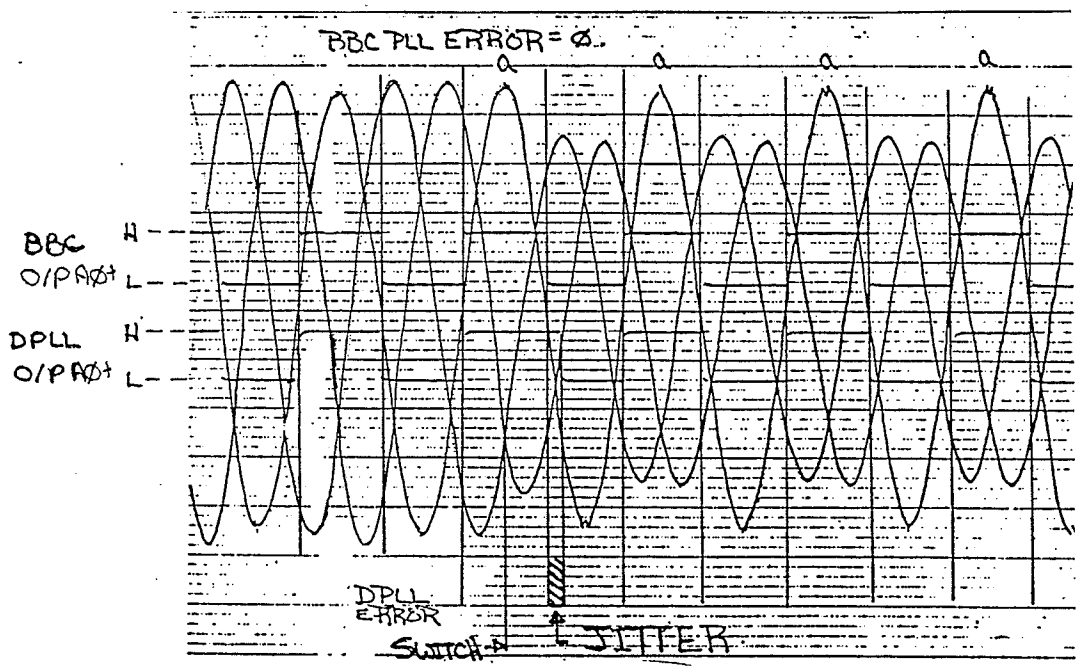

Figure 4.4.5: Introduction of an unbalance

Again the DPLL A0+ waveform is on the bottom while the BBC A0+ is the top one. In theory neither waveform should move (see Section 4.2.3) during this test. Notice that the DPLLs waveform has a slight jitter at the introduction of the unbalance. This is attributed to errors created by the peak and slope detectors. But aside from a slight jitter it performs quite satisfactorily. The BBC circuit had no trouble with this test what so ever. The unbalance is removed in Fig. 4.4.6 below.

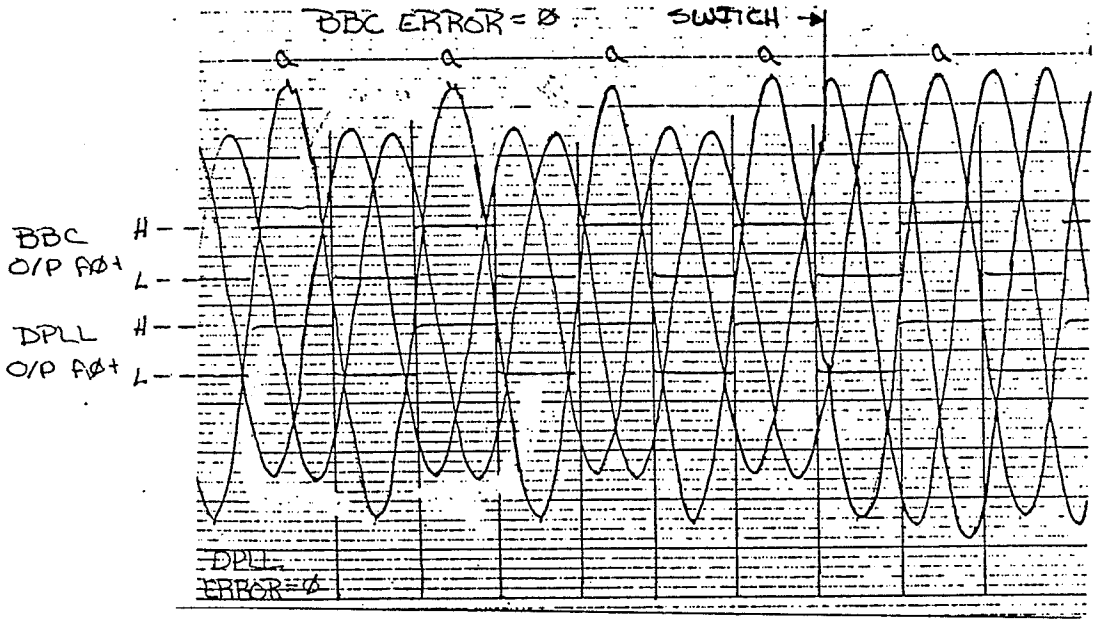

Figure 4.4.6: removal of the unbalance

The first thing to be noticed is that the DPLL did not jitter during this transition. From this test it is clear that the "Double Orthogonalization" technique is working as predicted.

4.4.3 OVERALL TEST RESULTS

The DPLL has demonstrated a transient response time of about half that of the BBC PLL. With the addition of an up/down theta counter and a variable gain curve it is thought that a better performance could be achieved. The DPLL has also demonstrated its ability to track the positive sequence component using the novel technique presented.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

Listed here are the important conclusions of the thesis, and recommendations for carrying on from where this project leaves off.

5.1 CONCLUSIONS

1. The "Double Orthogonalization" technique works well. It allows the phase of the positive sequence component to be determined at any instant of time independent of system imbalances. For proper operation harmonics must be removed prior to processing.
2. The standard PLL control technique, using continuous phase comparison worked well. Comparison with the performance of a commerical zero crossing type PLL indicated resynchronization times of less than half following major system disturbances for the prototype design.
3. The commerical PLL in steady state was more stable than the prototype design.

5.2 RECOMMENDATIONS

1. A more accurate and stable peak/slope detector is required for further study to be possible. It is thought that, the inclusion of programmable switching capacitor filters in the incoming signal lines would help this problem.
2. A floating point DSP should be used in any future design. This would allow gains to be dynamically varying and span a large range. In addition this would simplify the programming required in implementing a PLL.

3. The theta counter used to generate the reference waveforms should be able to count up as well as down. This would enhance tracking speed.

APPENDIX 'A'

PROOF OF "DOUBLE ORTHOGONALIZATION TECHNIQUE

This technique extracts the positive sequence component phase with respect to a set of reference phasors, independent of any system unbalances. Where a "snap shot" of the system waveforms and reference phasors is taken (at any instant of time) and forms a basis for the calculations.

PROOF

Let a three-phase system contain the following positive and negative sequence components (no harmonics or zero sequence components):

Positive Sequence;

$$Va = P\,Cos(wt) \qquad A1.1$$

$$Vb = P\,Cos(wt-120^{o}) \qquad A1.2$$

$$Vc = P\,Cos(wt+120^{o}) \qquad A1.3$$

Negative Sequence;

$$Va' = N\,Cos(wt+\theta offset) \qquad A1.4$$

$$Vb' = N\,Cos(wt+\theta offset\ +120^{o}) \qquad A1.5$$

$$Vc' = N\,Cos(wt+\theta offset\ -120^{o}) \qquad A1.6$$

,where $\theta offset$ is a constant angular offset with respect to the positive sequence component.

Then the system three-phase waveforms would be;

$$VA = Va + Va' \qquad A1.7$$

$$VB = Vb + Vb' \qquad A1.8$$

$$VC = Vc + Vc' \qquad A1.9$$

Now a three-to two-phase conversion is performed as follows;

$$Vds = VA \qquad \text{A2.1}$$

$$Vqs = (VB - VC)/\sqrt{3} \qquad \text{A2.2}$$

and solving;

$$Vds = P\,Cos(wt) + N\,Cos(wt+ \theta offset) \qquad \text{A3.1}$$

$$Vqs = P\,Sin(wt) - N\,Sin(wt+ \theta offset) \qquad \text{A3.2}$$

Now if an orthogonal vector is projected to each of the above;

$$Vds' = P\,Sin(wt) + N\,Sin(wt+ \theta offset) \qquad \text{A3.3}$$

$$Vqs' = P\,Cos(wt) - N\,Cos(wt+ \theta offset) \qquad \text{A3.4}$$

Now creating a reference set of orthogonal vectors with some angular offset , Φ , with respect to the positive sequence component:

$$Vdr = Cos(wt+\Phi) \qquad \text{A3.5}$$

$$Vqr = Sin(wt+\Phi) \qquad \text{A3.6}$$

(this Φ is the angular error that needs to be extracted)

Now let:

$$X = VqrVds - VdrVds' + VqrVqs' - VdrVqs \qquad \text{A4.1}$$

$$Y = VqrVds' + VdrVds + VqrVqs + VdrVqs' \qquad \text{A4.2}$$

X and Y reduce to the following;

$$X = 2P\,Sin(\Phi) \qquad \text{A5.1}$$

$$Y = 2P\,Cos(\Phi) \qquad \text{A5.2}$$

Now from equations A5.1 and A5.2 the following error function is derived;

$$\Phi = \arcsin\left(X / \left(\sqrt{X^2 + Y^2}\right)\right) \qquad \text{A6.1}$$

,where

$$\sqrt{X^2 + Y^2} = \sqrt{4P^2} = 2P$$

and hence;

Φ = arcSin(2P Sin(Φ)/2P)

= arcSin(Sin(Φ)) = Φ

Hence the offset error , Φ , is extracted from the unbalanced waveforms. In order to extract the phase error with respect to the negative sequence component substitute the following three-to two-phase transformation equations for equations A2.1 and A2.2.

V_{ds} = VA A7.1

V_{qs} = (VC - VB)/ $\sqrt{3}$ A7.2

APPENDIX 'B'

COMPUTER SIMULATION PROGRAM LISTINGS

```
C
C  DEFINE I/O ASSIGNMENTS
C
      DIMENSION PHIE(3)
      IOF=52
      IOC=6
      IIC=5
C
C  READ SIMULATION PARAMETERS
C
      OPEN(IOF,FILE='PERF')
      WRITE(IOF,400)
      WRITE(IOC,100)
      READ(IIC,*)FINISH,STEPT
      WRITE(IOC,110)
      WRITE(IOC,120)
      READ(IIC,*)WS
      WRITE(IOC,130)
      READ(IIC,*)UA,PHIA
      WRITE(IOC,140)
      READ(IIC,*)UBC,PHIBC
      WRITE(IOC,150)
      WRITE(IOC,160)
      READ(IIC,*)TSTRT,TEND
      WRITE(IOC,170)
      READ(IIC,*)WS1,ACCEL
      WRITE(IOC,180)
      READ(IIC,*)UA1,PHIA1
      WRITE(IOC,190)
      READ(IIC,*)UBC1,PHIBC1
      WRITE(IOC,200)
      WRITE(IOC,210)
      READ(IIC,*)TOL0,TOL2
C
C  INITIAL CONSTANT DEFINITION
C
      SKEW=STEPT/10.
      WV=0.0
      WT=0.0
      PI=3.141592654
      PI2=2*PI
      WO=WS
      PHI=0.0
      THP=0.0
      THA=0.0
      THBC=0.0
      I=0
      DELT=0.0
C
C  RESTRICTIONS:
C
C  TIMES TSTRT AND TEND MUST FALL ON INCREMENTS OF STEPT.
C
C
C  MAIN LINE LOOP
C
      DO 10 TIME=0.0,FINISH,STEPT
C
C
C  SYSTEM TRANSIENT ?
C
      IF(TIME.LT.TSTRT-SKEW.OR.TIME.GT.TEND+SKEW)GOTO 20
C
      UA=UA1
      UBC=UBC1
C
      PHIA=PHIA1
      PHIBC=PHIBC1
C
      WS=WS1
C
      DELT=TIME-TSTRT
      PHI=ACCEL/2*DELT**2.
C
C   IS TRANSIENT OVER ?
C
20    IF(TIME.LE.TEND+SKEW)GOTO 30
C
      DELT=TEND-TSTRT
      WS=WS+ACCEL*DELT
      ACCEL=0.0
```

```
C
C  INSTANTANEOUS VALUES ARE READ
C
30    W=WO+WT
      WT=0.0
      THA=THA+STEPT*WS
      IF(THA.GT.PI2)THA=THA-PI2
      THBC=THBC+STEPT*WS
      IF(THBC.GT.PI2)THBC=THBC-PI2
      THP=THP+STEPT*W
      IF(THP.GT.PI2)THP=THP-PI2
      THQ=THA+PHI+PHIA
      THD=THBC+PHI+PHIBC
C
      THITQ=INT(THQ/PI2)
      THITD=INT(THD/PI2)
C
      THQ=THQ-THITQ*PI2
      THD=THD-THITD*PI2
C
      VQ=UA*SIN(THQ)
      VQD=UA*COS(THQ)
C
      VD=UBC*COS(THD)
      VDQ=UBC*SIN(THD)
C
      VQP=SIN(THP)
      VDP=COS(THP)
C
C  FORMING ERROR FUNCTION
C
      X=VQ*VDP-VQD*VQP+VDQ*VDP-VD*VQP
      Y=VQ*VQP+VQD*VDP+VDQ*VQP+VD*VDP
C
      PHIER=ASIN(X/SQRT(X**2.+Y**2.))
      IF(Y.GE.0.0)GOTO 35
      IF(X.GE.0.0)THEN
        PHIER= PI/2.0-PHIER+PI/2.0
      ELSE
        PHIER= -PI/2.0-PHIER-PI/2.0
      END IF
C
35    IF(ABS(PHIER).LT.TOL0)GOTO 40
      I=I+1
      PHIE(I)=PHIER
C
      IF(I.LT.3-0.1)GOTO 40
C
C  PREDICT AND CORRECT ERROR
C
      V1=PHIE(2)-PHIE(1)
      IF(V1.LT.(0-PI))V1= V1+PI2
      IF(V1.GT.PI)V1= V1-PI2
C
C  RESET 3 SAMPLE COUNTER.
C
      I=0
C
C     APPRECIABLE VELOCITY?
C
      IF(ABS(V1).LT.TOL2)V1=0.0
C
C     PREDICT PHASE ERROR
C
      PHIE(3)=PHIE(2)+V1
C
C     VELOCITY CORRECTION.
C
      WV=(PHIE(3)-PHIE(2))/STEPT
      IF(ABS(WV).LT.TOL2/STEPT)WV=0.0
      WO=WO+WV
C
C     CORRECT PHASE ERROR IN ONE STEP.
C
      WT=PHIE(3)/STEPT
      IF(ABS(WT).LT.TOL0/STEPT)WT=0.0
40    A=3
C
C RECORD TIME STEP RESULTS.
C
10    WRITE(IOF,500)TIME,PHIER,VQ,VQD,VD,VDQ,VQP,VDP
```

```
C
C  FORMAT STATEMENTS
C
100   FORMAT(2X,'INPUT TIME OF: FINISH,STEP ')
110   FORMAT(2X,'INITIAL SYSTEM PARAMETERS ')
120   FORMAT(2X,'SYSTEM FREQUENCY ')
130   FORMAT(2X,'VA    : MAGNITUDE,PHASE ')
140   FORMAT(2X,'VBC   : MAGNITUDE,PHASE ')
150   FORMAT(2X,'TRANSIENT SYSTEM PARAMETERS ')
160   FORMAT(2X,'TIME: START,END ')
170   FORMAT(2X,'SYSTEM:FREQUENCY,ACCELERATION ')
180   FORMAT(2X,'VA    : MAGNITUDE,PHASE ')
190   FORMAT(2X,'VBC   : MAGNITUDE,PHASE ')
200   FORMAT(2X,'ERROR TOLORENCES')
210   FORMAT(2X,'PHASE,FREQ. ')
400   FORMAT(2X,'DOUBLE ORTHOGONALIZATION TECHNIQUE RESULTS/')
500   FORMAT(F8.5,10G11.4)
      END
```

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