STRESSED MEMS CPW CANTILEVERS FOR HIGH FREQUENCY SCANNING PROBE MICROSCOPY

By

Bingqing Liang

A Thesis
Submitted to the Faculty of Graduate Studies
in Partial Fulfillment of the Requirement
For the Degree of

Master of Science

Department of Electrical and Computer Engineering
University of Manitoba,
Winnipeg, Manitoba
Canada

@ Bingqing Liang
2004

THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

*****

COPYRIGHT PERMISSION

Stressed MEMs CPW Cantilevers for High Frequency Scanning Probe Microscopy

BY

Bingqing Liang

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirement of the degree

Of

MASTER OF SCIENCE

Bingqing Liang © 2004

Permission has been granted to the Library of the University of Manitoba to lend or sell copies of this thesis/practicum, to the National Library of Canada to microfilm this thesis and to lend or sell copies of the film, and to University Microfilms Inc. to publish an abstract of this thesis/practicum.

This reproduction or copy of this thesis has been made available by authority of the copyright owner solely for the purpose of private study and research, and may only be reproduced and copied as permitted by copyright laws or with express written authorization from the copyright owner.

Abstract

This thesis presents a novel stressed MEMS coplanar waveguide (CPW) cantilever to solve the limitations of conventional cantilevers in EFM measurements. The CPW structure creates a matched impedance and shields the signal conductor along the cantilever to improve bandwidth, reduce electromagnetic interference effects, and enable better access to IC test points. The designed CPW cantilever is mounted on a large Si substrate which acts as a holder. A tapered CPW connects a CPW line on the Si holder to the stressed CPW cantilever in air. This thesis focuses on selection considerations, theoretical calculation and analysis, design, modeling, simulation, fabrication, and testing of CPW cantilevers.

This thesis presents selection considerations of the designed CPW cantilevers according to electrical and mechanical requirements. It provides analytical expressions and experimental formulas to compute the characteristic impedance, effective dielectric constant, and attenuation of CPW lines. The theoretical calculations and analyses are used to obtain the optimum dimensions of CPW cantilevers. HFSS electromagnetic simulation results are used to modify and verify the performance of the designed CPW cantilevers.

The designed CPW cantilever was fabricated at the MEMS lab at the University of Manitoba. Materials used were conducting Al/Cu layers on a high-resistivity 1000 Ω-cm, 325 μm thick Si wafer covered with a thin SiO_2 insulating layer. A BOE etchant was used to remove unwanted SiO_2 regions and form openings. A KOH etch was used to form a preliminary cavity and V-grooves on the Si holder backside. Al/Cu metallization was evaporated and patterned on top of a remaining 0.36 μm SiO_2 layer to form the CPW lines on the frontside of the Si wafer. A XeF_2 etch was then used to remove a remaining 40 μm of Si substrate below the cantilever and release the cantilever structure.

A simple model is developed to explain the mechanical characteristics of stressed MEMS cantilevers. The stress, resonant frequency, spring constant, and quality factor are calculated by using the dimensions of the stressed cantilevers. As an example, stressed CPW cantilevers approximately 640 μm long result in a bending height of approximately 130 μm.

The electrical propagation properties of stressed CPW cantilevers are measured for the frequency range 0.04-40 GHz. Measured return loss of the CPW cantilevers was found to be dominated by the lossy CPW-on-Si holder section of the cantilever. This was approximately 3 dB at 20 GHz. The reflection loss of a 575 μm CPW cantilever in air was determined to be better than 0.7 dB at 20 GHz. Measured results are compared with both calculated results using an equivalent circuit model and simulated results using HFSS. Both the equivalent circuit model and HFSS simulation can approximately predict the S-parameters of the stressed CPW cantilevers.

Acknowledgements

I would like to acknowledge, and sincerely thank, my supervisor, Dr. Greg Bridges, who has been my supportive mentor throughout my study. I am grateful for the support and guidance he has offered and the patience he has shown in many insightful discussions. Greg is truly an exceptional supervisor, and I am fortunate for the opportunity to have been a part of his lab.

I would like to thank Dr.Cyrus Shafai for providing enormous help and guidance. Many of the experiments were done at his MEMS laboratory.

I would like to thank Dr.Ming Zhang and all members of SPM/MEMS group, the department's technical staff at University of Manitoba. I am grateful to everyone who contributed to this thesis.

Deeply thanks to my wife, Wanhong. Thanks for the endless love you give to me and all the happiness you created in our life. Your caring and understanding make me always feel that I have a peaceful harbor, our home, when I am tired outside. Finally, I greatly thank my parents. Their unconditional love have been supporting and encouraging me all the time.

Contents

Abstract I

Acknowledgements III

Contents IV

List of Figures VII

List of Tables X

Chapter 1 Introduction 1

1.1 IC probing techniques 1

1.2 Electrostatic force microscopy 2

1.2.1 EFM operation principle 2

1.2.2 Conventional EFM cantilever probe 4

1.3 Limitations of current commercial SPM cantilever probes 6

1.4 CPW transmission line and advantages 8

1.5 Motivation of the thesis 10

1.6 Outline of the thesis 11

Chapter 2 Design considerations and modeling of CPW cantilevers 12

2.1 Introduction 12

2.1.1 CPW cantilever 12

2.1.2 Stressed cantilever 14

2.1.3 Stressed CPW cantilever 15

2.2 Electrical and mechanical design considerations 17

2.2.1 Electrical design considerations 17

2.2.2 Mechanical considerations 23

2.2.3 Electrical and mechanical considerations 29
2.3 CPW dimension design considerations and simulation results 30
2.3.1 Basic theory of CPW transmission line 30
2.3.2 Characteristic and dimension considerations of CPW line 34
2.3.3 Simulation results of a CPW cantilever 41
Chapter 3 Basic principles and processes of MEMS CPW cantilever fabrication 47
3.1 Introduction 47
3.2 The main processes of MEMS fabrication 48
3.2.1 Surface treatment 48
3.2.2 Photolithography 49
3.2.3 Etching 52
3.2.4 Stripping 54
3.2.5 Inspection & Testing 54
3.3 Other issues in CPW cantilever fabrication 55
3.3.1 Mask design 55
3.3.2 Deposition films 57
3.3.3 Release cantilever 57
3.4 MEMS CPW cantilever fabrication 58
3.4.1 MEMS CPW cantilever fabrication parameters 58
3.4.2 Detailed MEMS fabrication steps of CPW cantilevers 59
Chapter 4 Characteristics of CPW cantilevers and discussion 65
4.1 Mechanical properties of stressed MEMS CPW cantilevers 65
4.1.1 Stress 65

4.1.2 Resonant frequency 68

4.2 Electrical properties of stressed MEMS CPW cantilevers 72

4.2.1 Computing the characteristic impedance and effective dielectric constant 72

4.2.2 The measured and simulated S-parameters 74

Chapter 5 Conclusions and future work 100

5.1 Conclusions 100

5.2 Future work 101

5.2.1 Fabrication the CPW cantilever tip 101

5.2.2 CPW cantilever tip in EFM 101

Reference 103

Appendix A: Masks for MEMS CPW cantilevers 108

List of Figures

Figure 1.1 Electrostatic force IC probing system and equivalent model. 3

Figure 1.2 A cantilever with tip. 5

Figure 1.3 A conventional cantilever and its equivalent circuit in EFM measurement. 7

Figure 1.4 A stressed CPW cantilever. 8

Figure 1.5 (a) Conventional CPW (top: left); (b) Conductor-backed CPW (top:right); (c) Typical micromachined CPW [19]. 9

Figure 2.1 A CPW cantilever with coaxial tip [25]... 13

Figure 2.2 A CPW cantilever in EFM measurement. 13

Figure 2.3 Stressed MoCr cantilevers on quartz [29].. 15

Figure 2.4 A stressed CPW cantilever. 16

Figure 2.5 A stressed CPW cantilever and equivalent circuit in EFM measurement. 16

Figure 2.6 CPW on a silicon wafer with a thin SiO_2 interfacial layer............................ 21

Figure 2.7 A stressed CPW cantilever in EFM voltage measurement............................ 25

Figure 2.8 Equivalent model of a stressed CPW cantilever in laser beam deflection system.. 25

Figure 2.9 A CPW transmission line on substrate [19]... 31

Figure 2.10 CPW cantilevers with (a) ground connected; (b) ground opened................. 35

Figure 2.11 Three parts of CPW cantilever with ground connected or ground opened.... 36

Figure 2.12 Computed losses (40 GHz) as a function of center strip conductor width S for a CPW with different resistivity of Si substrates as parameters. (a) Dielectric loss; (b) Total loss (ε_r = 11.9, b = 100 μm, t = 1 μm, h = 325 μm)................................ 37

Figure 2.13 Computed attenuation constant as a function of center strip conductor width S for a CPW with different frequencies. (a) Part 1: CPW line on Si holder, ε_{r1} = 11.9, b_1 = 100 μm, t = 1 μm, h = 325 μm; (b) Part 3: CPW cantilever in air, ε_{r3} = 1, b_3 = 55 μm, t = 1 μm. 38

Figure 2.14 Computed characteristics of CPW on Si wafer as a function of $S_1/(S_1+2W_1)=a_1/b_1$, with the normalized substrate h/b_1 as a parameter, ε_{r1} = 11.9, h = 325 μm. (a) Characteristic impedance; (b) effective dielectric constant.................. 39

Figure 2.15 Computed characteristic impedance of CPW cantilever in air..................... 40

Figure 2.16 Computed attenuation constant of CPW as a function of conductor thickness t with frequency as a parameter. (a) Part 1: CPW on Si wafer. ε_{r1} = 11.9, S_1 = 92 μm, W_1 = 54 μm, h = 325 μm; (b) Part 3: CPW cantilever in air. ε_{r3} = 1, S_3 = 40 μm, W_3 = 35 μm. 41

Figure 2.17 Dimensions of an entire CPW cantilever. 42

Figure 2.18 The photographs and S-parameters of three parts of a CPW cantilever. (a) Part 1: 5000 μm CPW on Si holder (Z_0 = 142 Ω); (b) Part 2: 200 μm transition on Si holder; (c) Part 3-1: ground connected 640 μm cantilever in air; (d) Part 3-2: ground opened 640 μm CPW cantilever in air (Z_0 = 142 Ω). 44

Figure 2.19 Photographs and simulated S-parameters of three cases. 46

Figure 3.1 Main processes of MEMS fabrication. 47

Figure 3.2 Draft and dimensions of a MEMS CPW cantilever with cavity and V-grooves. 48

Figure 3.3 A typical photolithography process. 49

Figure 3.4 Lithographic contact masks (glass). 56

Figure 3.5 Fabrication steps for CPW cantilevers: 1. Deposit photoresist on both sides of Si wafer covered with SiO_2 layers; 2. Use mask 1 to define the cavity and V-groove on the backside, expose and develop photoresist; 3. BOE etch exposed SiO_2 regions; 4. Backside KOH deep etch; 5. Use mask 2 to define cantilever beam regions and remove the unwanted SiO_2 regions on the frontside, expose and develop photoresist; 6. BOE etch SiO_2 at unwanted regions; 7. Deposit Al/Cu layers and then photoresist on SiO_2 layer; 8. Use mask 3 to apply and pattern the CPW transmission lines on the frontside; 9. Use chrome etchant etch Cu, and BOE etch Al and SiO_2 layers at unwanted regions; 10. Remove photoresist and use XeF_2 gas backside etch the remained Si wafer at membrane to release CPW cantilevers; 11. CPW cantilevers mounted by Si holder (a) CPW cantilever suspended in air; (b) CPW cantilever suspended by the thin SiO_2 layer. 60

Figure 3.6 Dimensions of a CPW cantilever on a SiO_2 membrane above a cavity. 62

Figure 3.7 Designed dimensions of a cavity and a V-groove after KOH deep etch. 62

Figure 3.8 Cross sectional view of the CPW line on Si holder. 63

Figure 3.9 Examples of fabricated CPW cantilevers. a) Cantilever on SiO_2 membrane; b) Cantilever in air; c) Ground connected cantilever on SiO_2 membrane; d) Ground connected cantilever in air; e) Cantilever in air; f) Ground connected cantilever in air). 64

Figure 4.1 (a) A stressed MEMS CPW cantilever; (b) Arrays of stressed MEMS CPW cantilevers on a Si wafer. 65

Figure 4.2 Stress gradients causing a bent cantilever [60]. 66

Figure 4.3 (a) Resonant frequency measurement set up; (b) Laser beam bounce deflection system for measuring mechanical properties. 69

Figure 4.4 Resonant frequency of cantilevers. 70

Figure 4.5 (a) Ground-connected side beams; (b) equivalent beam. 71

Figure 4.6 CPW transmission line on two-layer substrate. 72

Figure 4.7 S-parameter measurement set up. 75

Figure 4.8 (a) Ground connected CPW cantilever on SiO_2 membrane; (b) CPW transmission line on Si holder. 76

Figure 4.9 S-parameters (a) Ground connected CPW cantilever on SiO_2 membrane (part 3) mounted on a 3200 μm CPW transmission line on a Si holder (part 1); (b) A 3200 μm CPW transmission line (part 1). 77

Figure 4.10 Magnitude and phase of S21 for the 3200 μm CPW transmission line on Si holder (Figure 4.8 (b), case B). 78

Figure 4.11 Effective dielectric constant and attenuation constant per millimeter using measured S-parameters of Figure 4.10. 80

Figure 4.12 Simulation S-parameters (a) CPW cantilever (part3) mounted 3200 μm CPW line on a Si holder (part 1) in Figure 4.8 (a); (b) 3200 μm CPW line on a Si holder (part 1) in Figure 4.8 (b). 81

Figure 4.13 Effective dielectric constant and attenuation constant per millimeter using simulated S-parameter in Figure 4.12 (b). 82

Figure 4.14 S11 magnitude and phase of a 575 μm CPW transmission line in air 83

Figure 4.15 Attenuation constant and phase constant per millimeter using simulated S-parameters of 575 μm CPW cantilever in air. 84

Figure 4.16 Equivalent circuit model for a CPW cantilever mounted CPW line on Si holder 86

Figure 4.17 A ground connected stressed MEMS CPW cantilever (a) 3D view; (b) Top view. 89

Figure 4.18 Magnitude and phase of S-parameter of CPW cantilever mounted 5000 μm CPW on a Si holder in Figure 4.17 using (a) Measurement; (b) Equivalent circuit model; (c) HFSS simulation. 92

Figure 4.19 Ground connected for both ends of CPW cantilevers (a) on membrane; (b) in air. 93

Figure 4.20 Magnitude and phase of the reflection coefficients of CPW cantilever mounted 2600 μm CPW line on a Si holder using (a) Measurement; (b) Equivalent circuit model; (c) HFSS simulation. 95

Figure 4.21 A VNA in microwave measurement [64]. 96

Figure 4.22 Two-port and one-port VNA error models [64] 97

Figure 4.23 Magnitude and phase of short circuit and open circuit. 99

Figure 5.1 Fabrication steps for CPW cantilever with probe tip (Not to scale). 102

List of Tables

Table 1.1 Typical specifications of a contact cantilever [14] 6
Table 2.1 Dielectric substrates [34] 18
Table 2.2 Conductivity for selected bulk conductor materials [35] 20
Table 2.3 Electrical properties of some thin films [40][41] 22
Table 2.4 Deposition methods and typical applications of some thin films [42] 22
Table 2.5 Mechanical properties of some materials 24
Table 3.1 Comparison of example silicon etchants [40] 53
Table 3.2 Recommended process steps in MEMS CPW cantilever fabrication 59
Table 4.1 Calculated stresses in cantilevers 68
Table 4.2 Measured and calculated mechanical parameters of stressed cantilevers 71
Table 4.3 Three part dimensions and dc resistance of fabricated CPW cantilevers 76
Table 4.4 Propagation parameters per millimeter of 3200 μm CPW line on Si holder ... 80
Table 4.5 Propagation parameters per millimeter of 3200 μm CPW line on Si holder (part 1) using simulated S-parameter in Figure 4.11(b) 83
Table 4.6 Propagation parameters per millimeter of 575 μm CPW cantilever in air 84
Table 4.7 Three part dimensions and dc resistance of fabricated CPW cantilever 90
Table 4.8 ABCD and S-parameters of CPW cantilever mounted 5000 μm CPW line on Si holder using equivalent circuit model in an open circuit 91
Table 4.9 Three part dimensions and dc resistance of fabricated CPW cantilevers 93

Chapter 1 Introduction

Integrated circuit (IC) technologies are rapidly evolving towards smaller size and higher speed, and it is setting more difficult and the inability to measure the internal signals without disturbing the normal operation of a working device. A micro-electromechanical systems (MEMS) probe capable of measuring signals at the internal nodes of an IC would be an invaluable tool for design verification and failure analysis. Electrostatic Force Microscopy (EFM) is a technique that provides this capability. However, a conventional EFM cantilever has problems in measuring the high frequency signals of an IC, such as limited bandwidth. A novel CPW cantilever is proposed to overcome the limitations of a conventional cantilever.

1.1 IC probing techniques

Due to the importance of IC internal testing and its commercial potential, many diagnostic tools have been developed to measure the internal signals of an IC. They are broadly divided into two categories: contact probing and non-contact probing.

Contact probing is a simple way to measure signals of an IC by establishing an electrical contact with a small needle probe between test equipment and a test point of a sample. This on-wafer contact probing [1][2] is often organized into the following categories: low impedance such as matched impedance probes, medium impedance such as resistive divider probes, and high impedance such as active probes. These direct contact techniques face spatial resolution limitations when attempting to probe sub-micron line width, and in order to probe an arbitrary internal point the passivation must be removed. Contact probes are also limited due to the trade-off between bandwidth and loading and can disturb a circuit's normal operation due to parasitic loading at high frequency.

Non-contact probing usually has high spatial and temporal resolution, is non-invasive (small loading effect), has easy sample preparation, and is capability of arbitrary node probing without the need for predefined test points. Non-contact test techniques with high

resolution for device internal function and failure analysis include electron beam probing, electro-optic probing, photoconductive sampling, and scanning probe microscopy (SPM) [3][4].

1.2 Electrostatic force microscopy

1.2.1 EFM operation principle

Electrostatic force microscopy (EFM) [4]-[7] is a member of SPM. EFM is an extension of the non-contact atomic force microscopy (AFM). EFM uses the localized Coulomb force interaction between a non-contacting micromachined probe and a test point of a sample to provide internal voltage information, simultaneous topography, surface potential or charge, and capacitance variation. In EFM measurement, all information comes from the value of the voltage difference and the capacitance between a probe tip and a test point of the sample surface.

A diagram of the EFM voltage measurement system and its equivalent circuit are shown in Figure 1.1. A conducting probe tip is located above the test point of the sample surface where the localized signal $v_S(x,y,t)$ is to be measured. An adjustable voltage $v_p(t)$ is externally applied to an EFM probe. The voltage difference $V = v_p - v_S$ between the probe tip and the test point of the sample generates a small charge due to the capacitance (*C*) and it results in an attractive force proportional to the square of the voltage difference *V*. The conductive probe usually operates at 0.1-0.3 μm above the test point surface. This introduces a capacitive loading of less than 1fF [8], which is much lower than that of conventional contacting probes. By monitoring the deflection using a sensitive sensor, the electrostatic force and thus the voltage difference can be extracted. The electrical energy stored in a localized capacitor can be expressed as:

$$U = \frac{1}{2} C V^2 \tag{1.1}$$

The electrostatic force acting on an EFM probe is:

$$\vec{F} = \nabla U = \frac{1}{2}\nabla(CV^2) \tag{1.2}$$

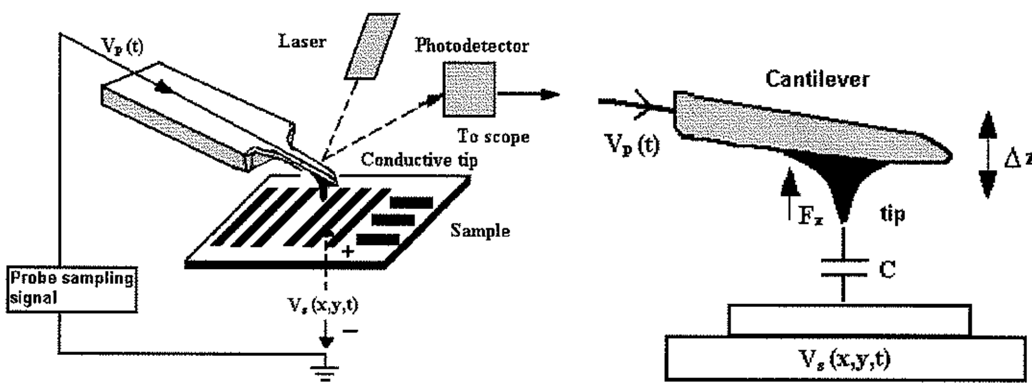


Figure 1.1 Electrostatic force IC probing system and equivalent model.

The main deflection of an EFM cantilever is in the *z*-axis and thus a deflection sensor detects *z*-direction deflection. The electrostatic force [9] in *z*-axis is given by:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)[v_P(t) - v_S(x,y,t) + \Delta\Phi]^2 \tag{1.3}$$

where z is the distance between the probe and test point of the circuit. The term $\Delta\Phi$ has been added to equation (1.3) to represent dc offset effects due to surface charge [10] and material work function differences.

The equivalent time sampling [11] and heterodyne [12] techniques have been introduced to measure high frequency voltage signals at the internal nodes of an IC. Both techniques employ the square-law force interaction between the probe and the sample for nonlinear mixing and sampling, where a high frequency electrical signal is converted to a low frequency mechanical signal that can easily be sensed by the probe cantilever.

The frequency response of the cantilever motion under an electrostatic force F_Z and near a resonance is [13]

$$|G(f)| = \frac{(Q/k)(f_r/f)}{\sqrt{1+Q^2(\frac{f_r}{f}-\frac{f}{f_r})^2}} \tag{1.4}$$

where k is the spring constant, f_r is resonant frequency, and Q the quality factor of the cantilever beam which is defined using the 3dB bandwidth from cantilever's resonance frequency. Then the cantilever deflection near resonance due to the electrostatic force F_Z is

$$\Delta z(f) = F_Z(f)|G(f)| = \frac{F_Z(f)(Q/k)(f_r/f)}{\sqrt{1+Q^2(\frac{f_r}{f}-\frac{f}{f_r})^2}} \quad (1.5)$$

When $f = 0$, $\Delta z = F_Z/k$.

When $f = f_r$ the deflection (1.5) becomes

$$\Delta z|_{f_r} = \frac{Q}{k}F_z(f) \quad (1.6)$$

Therefore, the maximum cantilever deflection occurs when the external driving frequency equals the resonant frequency f_r. Obviously, the magnitude of deflection at f_r is enhanced by a factor of Q over that of the static case where $f = 0$. Since the long-range electrostatic force is much smaller than the contact atomic force, an EFM probe is usually driven at its resonant frequency to increase the sensitivity of the deflection detection.

For high-speed IC testing driving frequencies much greater than f_r need to be used. However, the deflection will be very small at these frequencies and the direct use of equation (1.3) for high frequency probing is not possible. Several techniques which employ the non-linear voltage dependence have been proposed to overcome this limitation [4]-[6]. In all these cases an exciting force signal is produced where equation (1.5) is valid and thus this form is used for the response of the probe for the remainder of the thesis.

1.2.2 Conventional EFM cantilever probe

SPM techniques all depend on the use of small micromachined cantilever probes. Silicon and silicon nitride probes are mostly used for topography measurements. Solid metal,

metalized or highly doped probes are used for electrical measurements. These cantilevers are usually rectangular and tips are pyramidal or conical in shape. Current EFM measurements use a commercial scanning probe cantilever as shown in Figure 1.2, which consists of a long Si based beam with a sharp tip at its end mounted on a large Si block. In this structure the beam length is approximately 300 μm with a conical tip length of 10 μm. The entire structure is metalized to conduct signals to the probe tip. It is necessary to have a conductive probe since voltages must be applied to the probe tip, while in AFM it is not necessary.

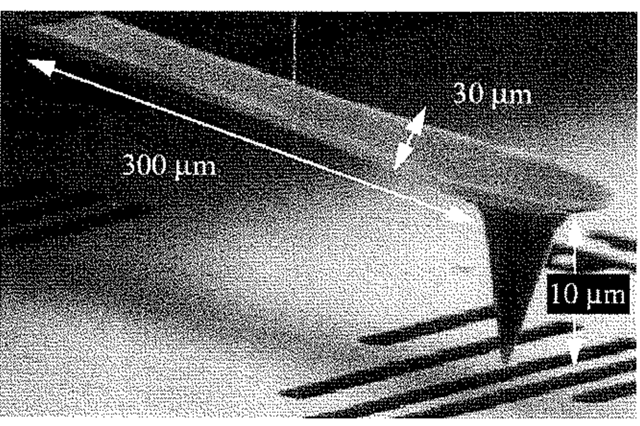


Figure 1.2 A cantilever with tip.

The characteristics of the probe play an important role in the resolution and sensitivity of EFM measurement. The spring constant k (N/m) of a rectangular cantilever structure fixed on one end is given by [13]:

$$k = \frac{Et^3 w}{4L^3} \quad (1.7)$$

where E (N/m^2) is Young's modulus, L, w, t are the length, width, and thickness of a cantilever, respectively. Small spring constant cantilevers are always desirable for EFM measurement since they provide more deflection per unit force.

The cantilever behaves very similar to that of a mass on a spring. The resonant frequency of a cantilever with end mass m and beam mass m_L on a spring is given by [13]:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m+0.24m_L}} \quad (1.8)$$

For quality factor Q, Q is defined from the cantilever frequency response as the ratio between the resonant frequency and the frequency span between the -3 dB points. A cantilever with high Q requires little energy to be excited at the resonant frequency and the sensitivity of the cantilever is proportional to the Q. Typical values of Q in a standard ambient probing environment may vary from 10 to 30, and in a vacuum to over 10000.

Typical geometries, spring constant, and resonant frequency of a micromachined silicon rectangular cantilever are listed below Table 1.1 [14]:

Table 1.1 Typical specifications of a contact cantilever [14]

	Typical value	Guaranteed range
Resonant frequency	13 KHz	+/- 4 KHz
Spring constant	0.2 N/m	0.07 N/m to 0.4 N/m
Length	450 μm	+/- 10 μm
Mean width	50 μm	+/- 5 μm
Thickness	2 μm	+/- 1 μm
Tip height	17 μm	+/- 2 μm
Tip radius	< 10 nm	
Tip geometry	Rotated	
Reflex coating	30 nm thick Aluminum	

1.3 Limitations of current commercial SPM cantilever probes

Conventional EFM techniques use commercially available scanning probe cantilevers. However, this commercial cantilever structure imposes limitations to high frequency probing:

1) It can not adequately transmit the very high frequency signals to a probe tip. A schematic of a conventional cantilever and its equivalent circuit in EFM voltage measurement are shown in Figure 1.3.

The high frequency signals from a cable will be affected by coupling to the side ground plane through the capacitance C_b. Since the impedance of capacitance $1/\omega C_b$ can be small at high frequencies they cannot be adequately transmitted to the probe tip. Thus, the conventional probe is limited in its ability to measure high frequency signals [15] [16].

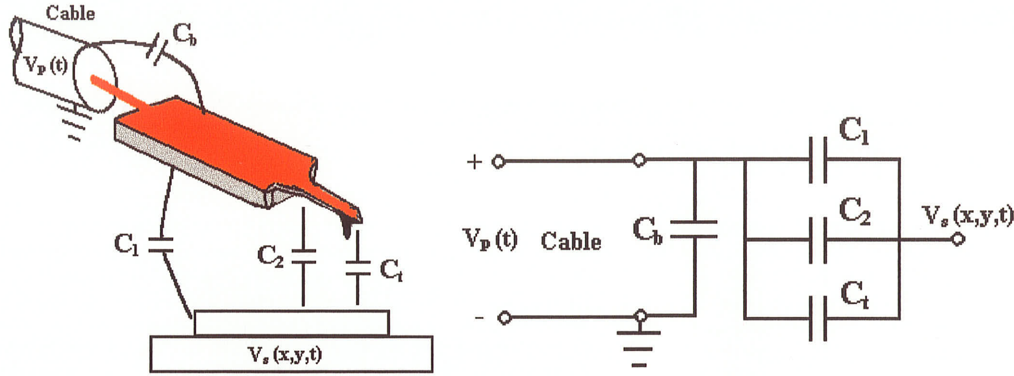


Figure 1.3 A conventional cantilever and its equivalent circuit in EFM measurement.

2) Lower spatial resolution due to parasitic coupling from signals other than at the IC test point. The localized probe tip-circuit interaction is degraded due to parasitic coupling to the cantilever and cantilever holder. In addition, high resolution EFM is difficult because the dithering amplitude is large (>10 nm) and the laser light may modulate the charge distribution due to the photoionization effect [17].

3) It is difficult to access to deep packages. The low tip height of a straight cantilever beam does not enable measurement of deep trenches, high step heights, or with local bond wires present. It is a serious problem to nondestructively measure the deep reactive ion etching and MEMS devices.

1.4 CPW transmission line and advantages

Since the conventional cantilevers have limitations to the measurement of high frequency signals, a novel stressed MEMS coplanar waveguide (CPW) structure cantilever, which incorporates a tapered CPW transmission line mounted on a Si holder, is developed as shown in Figure 1.4.

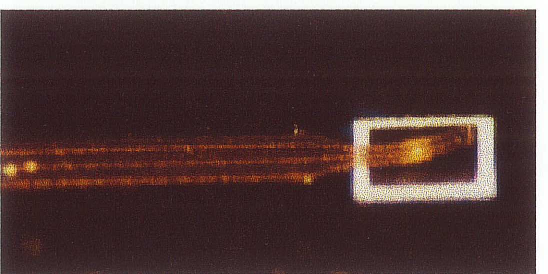


Figure 1.4 A stressed CPW cantilever.

A CPW fabricated on a dielectric substrate was first proposed by C.P.Wen in 1969 [18]. Now, the CPW structure is commonly used in monolithic microwave integrated circuit (MMIC), microwave integrated circuits (MICs) as well as in MEMS. CPW is a type of planar transmission line and can be broadly classified as follows: conventional CPW and conductor backed CPW with many variants when employing micromachined fabrication methods.

The basic structure, known as the conventional CPW, is shown in Figure 1.5 (a). A conventional CPW on a dielectric substrate consists of a center strip conductor with semi-infinite ground planes on either side. However, in a practical circuit the ground planes are made of finite extent. This kind of CPW structure was selected and studied in this thesis for its simplicity and easy fabrication. The conductor-backed CPW shown in Figure 1.5 (b) has an additional ground plane at the bottom surface of the substrate. The micromachined CPWs are of two types, the microshield line [20] shown in Figure 1.5 (c) and the CPW suspended by a silicon dioxide membrane above a micromachined groove.

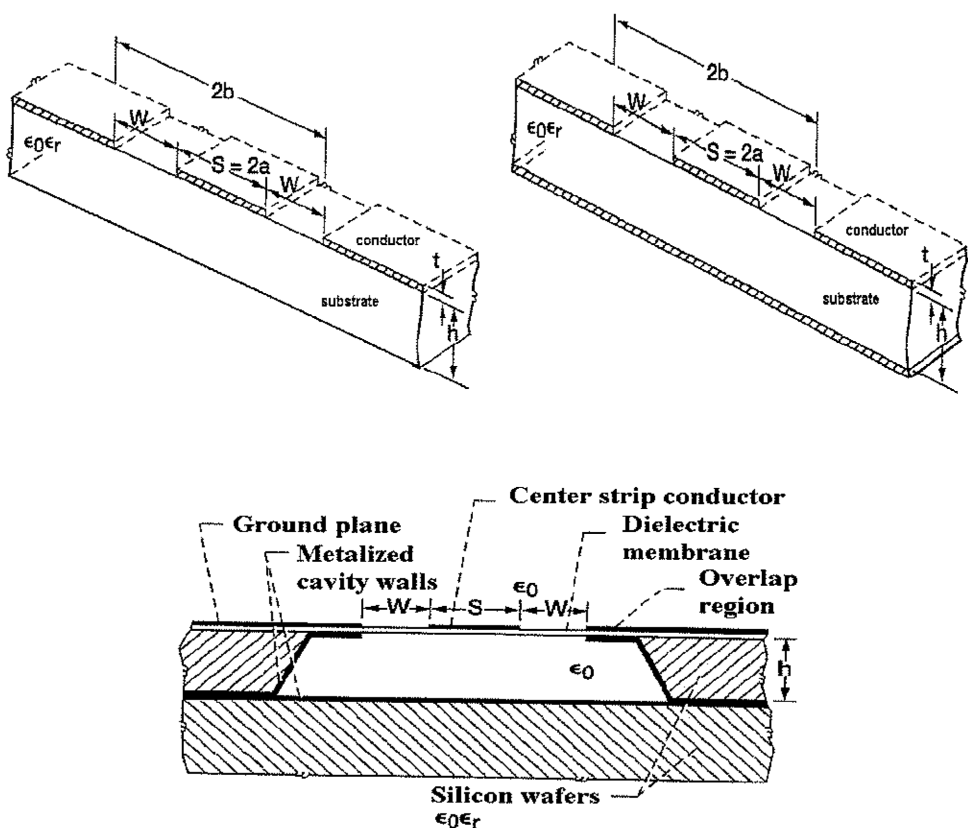


Figure 1.5 (a) Conventional CPW (top: left); (b) Conductor-backed CPW (top:right); (c) Typical micromachined CPW [19].

The conventional CPW structure shown in Figure 1.5 (a) offers several attributes:

1. It is uniplanar in construction, which implies that all of the conductors are on the same side of a substrate. This attribute simplifies manufacturing and allows fast and inexpensive measurements using non-contact or on-wafer probe techniques;
2. It can be readily accessed without drilling and plating holes in a substrate to reach the backside ground plane since CPW ground planes lie on top of the circuit board. Therefore, the CPW structure eliminates the need for wraparound grounding or via holes [21][22]. In CPW circuits, by eliminating via holes and its associated parasitic inductance, performance can be enhanced at high frequencies [23];
3. It facilitates easy shunt as well as series surface mounting of active and passive devices [21][22];

4. It reduces radiation loss [22]. It shields the signal conductor along the cantilever and will reduce coupling to the circuit being tested except right at the probing tip;
5. It can reduce cross talk effects between spatially separated transmission lines. A ground plane exists between any two adjacent lines and the high frequency electric fields are shielded by surrounding ground conductors, hence cross talk effects between adjacent lines are weak [22];
6. The characteristic impedance is determined by the ratio of a/b, so size reduction of CPW line is possible without limitations imposed by the substrate thickness, the only penalty being higher losses [24]. The CPW structure thus creates a matched impedance path that will have a very large bandwidth;
7. The CPW structure supports a quasi-TEM mode of propagation. The quasi-TEM mode of propagation on a CPW has low dispersion since a large percentage of the fields are in air and hence offers the potential to construct wide band circuits and components [23];
8. CPW circuits can be made denser than conventional microstrip circuits.

1.5 Motivation of the thesis

The CPW structure has many advantages over other types of transmission line especially at high frequency. A novel stressed CPW cantilever, which incorporates a tapered CPW transmission line to the probing tip, is proposed to overcome the limitations of conventional cantilevers. The stressed CPW cantilever can not only transmit the high frequency signals to the tip and get high spatial resolution in EFM measurements, but also non-destructively measure structures in deep trenches. The motivations of the thesis are design, modelling, simulation, fabrication, and testing of the designed MEMS CPW cantilevers in detail. In addition, the detailed design procedures of the MEMS CPW cantilever also will give us valuable experience in the implementation of the CPW structure in our in-house MEMS technology.

1.6 Outline of the thesis

Chapter 1 gave an overview of EFM operation principles and presented limitations of the conventional cantilever at high frequency. A stressed MEMS CPW cantilever to overcome the limitations was proposed. This chapter also presented the types and advantages of CPW construction and the motivations of the thesis.

Chapter 2 presents an overview of stressed cantilever design and proposes a novel stressed MEMS CPW cantilever. This chapter mainly focuses on selection considerations of designed MEMS CPW cantilevers according to electrical and mechanical requirements. It also provides analytical expressions and experimental formulas to compute the characteristic impedance, effective dielectric constant, and attenuation of CPW lines. To minimize the losses the HFSS electromagnetic simulation program is used to simulate, modify, and verify the designed CPW cantilevers.

After HFSS simulation, stressed MEMS CPW cantilevers are fabricated at the MEMS lab at the University of Manitoba. Chapter 3 presents the basic fabrication principles and the detailed fabrication procedures of MEMS CPW cantilevers on a silicon wafer.

The stress, resonant frequency, the spring constant, and quality factor are calculated in terms of the dimensions of the stressed cantilevers in chapter 4. A simple model is set up explaining the cases of the stressed MEMS cantilevers. The electrical propagation properties of stressed CPW cantilevers are measured. In comparison with calculated S-parameter using equivalent circuit model and simulated results using HFSS, the measured S-parameters are discussed and analyzed. They are almost the same in shape and in reasonable agreement with the measured S-parameters. The possible reasons for deviations are discussed and analysed. The reflection loss of a CPW cantilever in air is better than 0.7 dB at 20 GHz.

Chapter 5 gives the conclusions of this thesis and the suggestions for future related work.

Chapter 2 Design considerations and modeling of CPW cantilevers

This chapter presents an overview of the CPW cantilever and stressed cantilever in SPM. A novel stressed MEMS CPW cantilever is proposed to combine the advantages of the CPW cantilever and stressed cantilever in order to overcome the limitations of the conventional cantilevers in EFM. It also focuses on design considerations of MEMS CPW cantilevers. It then presents analytical expressions and experimental formulas for the characteristic impedance, effective dielectric constant, and attenuation of CPW lines. The theoretical calculations and analyses give the optimum dimensions of a CPW cantilever to minimize the losses and satisfy the design requirements. The HFSS program is used to simulate, modify, and verify the designed CPW cantilevers.

2.1 Introduction

2.1.1 CPW cantilever

In EFM measurement, it is necessary to have a conductive cantilever since input signals must be applied to a probe tip. The signals are required to travel along the conductive line on the wafer and cantilever in order to be applied at the probe tip. However, Si substrate is a rather lossy substrate at microwave frequencies, and due to this and mismatch effects, the conventional EFM cantilever cannot adequately transmit high frequency signals to the probe tip. The signals at the tip can be drastically different from the signals at the input cable, especially at high frequency. This makes it difficult to accurately measure the high frequency signals at the internal nodes in an IC chip using a conventional EFM cantilever.

A microscopic coaxial tip together with a CPW conductive line mounted by chip body was proposed [25] to overcome these limitations and used for near-field SPM probing as shown in Figure 2.1. A CPW cantilever consists of a center strip conductor with ground conductor lines on either side. The tip is built at the end of the center

conductive line of the CPW cantilever. The center signal line is placed between ground lines to reduce cross talk effect and to keep a constant impedance reducing the reflection loss. Coaxial waveguides have a twofold advantage in that there is a very high cutoff wavelength limit [26][27] and the outer conductor shields the signal, extended as close to the tip as possible to reduce noise levels [4]. Connections will be made between coaxial cables from a testing instrument and the transmission lines on the silicon substrate. A CPW cantilever used in EFM measurement, which incorporates a tapered CPW transmission line to the probing tip, is shown in Figure 2.2.

A tapered CPW multi-layer cantilever beams was fabricated on a silicon wafer [28]. It also summarized the mechanical and electrical characterizations of this probe card structure, based on numerical simulations.

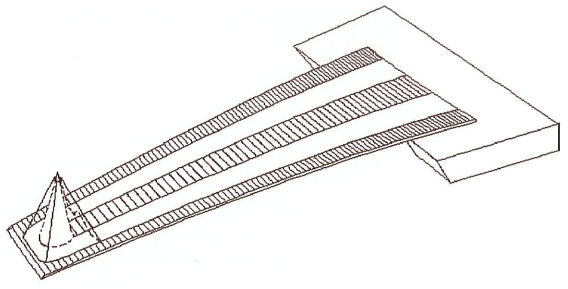


Figure 2.1 A CPW cantilever with coaxial tip [25].

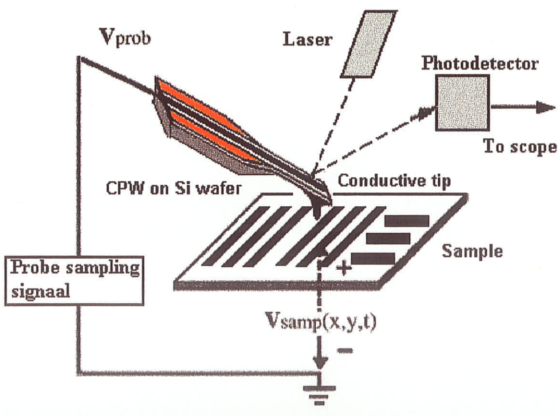


Figure 2.2 A CPW cantilever in EFM measurement.

2.1.2 Stressed cantilever

Straight cantilever beams with integrated probes are almost always employed in SPM. They can be mass fabricated and the best tips have a sharpness of only a few nanometers. Unfortunately, the low tip height of such probes is typically 1 to 15 μm and this does not allow for deep trenches or high step heights. This presents a problem for non-destructive measurements in step heights more than 100 μm, such as deep reactive ion etching (DRIE) and MEMS structures.

A technique has been developed to make use of highly stressed cantilevers instead of straight ones to overcome these problems [29]. A major issue in MEMS is the mechanical stress of thin films. Residual stress can be detrimental or advantageous depending on the applications and must be carefully considered during MEMS design process. Generally, the goal is to keep the stress as low as possible for providing durable and reliable film stacks. Alternatively, the stressed cantilever makes use of the residual stresses in a thin strip. The stressed cantilever probe can access deep, narrow, and high-topography structures for non-destructive measurements in an IC.

Figure 2.3 shows stressed MoCr cantilevers on a quartz substrate with a built-in stress profile resulting in the bending out from the substrate surface [29][30]. Refractory alloy MoCr has been chosen for the high stress. The films must change from compressive stress in their lower part, to tensile stress in the upper part in order to protrude from the substrate surface. Mechanical modeling and experimental tests on such stressed metal beams reveal that the force exerted by the spring tip can exceed many tens of milligrams.

The microstructure shown in Figure 2.3 curls up to relax the intrinsic stress, leaving a cantilever bending out of the substrate surface and thereby forming the microspring. Such springs can be made by introducing a stress gradient throughout its thickness in sputtered metal films. The stress gradient can be adjusted by the sputter pressure to make the metal beam bend away from the substrate surface after the release step. The release height can be controlled precisely by the deposition parameters. Cantilever length and bending determine the tip height which can be adjusted in a wide range from tens to hundreds of micrometers [29]. The tip heights increase with the increase of the corresponding cantilever lengths shown in Figure 2.3.

Figure 2.3 Stressed MoCr cantilevers on quartz [29].

2.1.3 Stressed CPW cantilever

The CPW line has the same advantages as conventional microstrip line, and offers several advantages over microstrip line. In EFM measurements, the additional advantage of using a CPW structure is that the ground shield can reduce interference from radiation and parasitic coupling to structure on the IC other than the test point while enabling a noncutoff transverse electromagnetic mode of wave propagation up to or away from the probe tip. Therefore, the high frequency signals from input cable can be transmitted to the probe tip with low losses. In addition, the stressed cantilever probe can non-destructively measure deep trenches and narrow structures. At present, however, the stressed cantilever can not measure signals with a large spatial resolution due to the use of a fairly low resolution lithography process used in our in-house fabrication facility.

By combining the advantages of the CPW cantilever with those of the stressed cantilever in EFM measurements, a novel stressed MEMS CPW cantilever is proposed as shown in Figure 2.4. The stressed CPW cantilever reduces the limitations of conventional microstrip cantilever. It can not only non-destructively measure deep trenches, but also measure the high frequency signals. Figure 2.5 is a simple model of a stressed CPW cantilever and its equivalent circuit as used in EFM measurements. The high frequency signals from a cable and along the CPW lines on the Si holder can easily be applied to the cantilever probe tip.

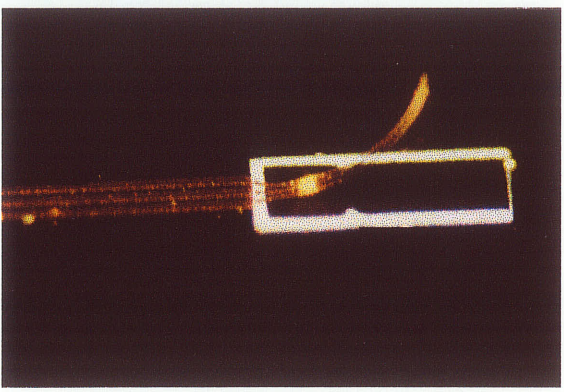


Figure 2.4 A stressed CPW cantilever.

In terms of spatial resolution, the stressed CPW cantilever should perform better than the conventional ones. The increased height of the stressed CPW cantilever and support block reduces interference from coupling through C_1 and C_2 in Figure 2.5 and increases spatial resolution. At present our probe tip is fairly large due to the lithography process used in our lab. However, the resolution of the probe could be improved by tapering the waveguide to reduce the probe tip size by sharpening the end of the inner conductor. This helps concentrate the fringing fields emanating from the probe apex and confine the interaction area between the probe and sample. Experiments with a sample between two sharpened coaxial transmission line tips resulted in $\lambda/10^6$ wavelength-relative resolution [31], where λ is the wavelength of the signal being measured.

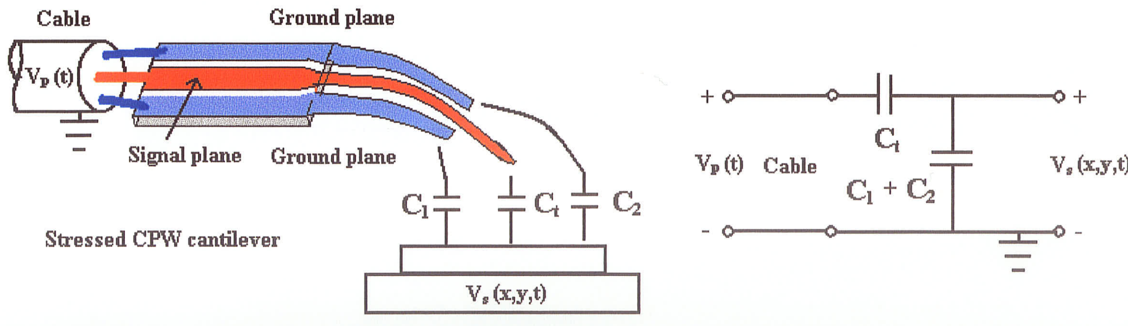


Figure 2.5 A stressed CPW cantilever and equivalent circuit in EFM measurement.

2.2 Electrical and mechanical design considerations

This section focuses on understanding the basis for selection considerations of CPW conductors and substrate materials in MEMS fabrication. Material selection has to be done according to the electrical and mechanical requirements which lead to tradeoffs between performance, cost, ease of manufacture, and lifetime.

2.2.1 Electrical design considerations

2.2.1.1 Impedance matched design

At RF frequencies, regular wires cannot be used to carry electrical signals. Transmission lines, such as a coaxial cable, are used instead to carry the energy from one end to another. To reduce unwanted reflections in high frequency circuits, the transmission lines have to be impedance matched. The transmission lines in almost all microwave components and test equipment are designed for 50 Ω characteristic impedance.

MEMS CPW transmission lines are widely used in microwave circuits. The important feature of the CPW line is that we can vary the width of center strip and slot to match components in outside circuits, while keeping the characteristic impedance (Z_0) constant. The characteristic impedance of a CPW line depends on its dimensions. The research shows that minimum attenuation occurs for CPW characteristic impedance close to 50 Ω [32] and in some cases, CPW has lesser losses and dispersion than microstrip for impedances near 50 Ω [33]. For maximum power transfer between circuits dictates that the CPW's impedance is set to 50 Ω. The dimensions of the CPW transmission line must be chosen so as to produce the lowest possible insertion loss and return loss. The insertion loss will be affected by mismatched loss, which comes from the characteristic impedance of CPW line on Si holder being different from 50 Ω as well as losses in the cantilever metallization and contact resistance loss.

2.2.1.2 Dielectric substrate selection

Dielectric materials, which have non-zero electrical conductivity, are used for the MEMS substrate. Electromagnetic waves experience larger losses when they propagate through a dielectric substrate with a larger conductivity. The loss tangent (tanδ) specifies the lossy nature of the dielectric. It is highly dependent on the purity of the material and defined as

$$\tan\delta = \frac{\sigma}{\omega\varepsilon_0\varepsilon_r} \qquad \textbf{(2.1)}$$

where σ is the electric conducitivity (S/m) and ε_0 is permittivity of vacuum and ε_r is relative dielectric constant of substrate.

The lower the conductivity, the lower the loss tangent. Hence the choice of a substrate with the appropriate conductivity becomes an important consideration in MEMS design. Table 2.1 lists the important properties of some common dielectric materials [34].

Table 2.1 Dielectric substrates [34]

Material	Electrical Conductivity (Sm^{-1})	Dielectric constant ε_r	tanδ x10^4 (at 10 GHz)	Thermal conductivity (W/cm °C)	Cost	Fracture
Alumina	10^{-10}	9.7	2	0.276	Low	Brittle, strong
Sapphire (crystal)	-	9.4	1	0.32	High	Brittle, strong
Quartz (fused)	10^{-17}	3.8	1	0.059	Middle	Brittle, fragile
Glass	10^{-12}	5	20	0.008	Low	Brittle, fragile
GaAs (high resistivity)	1×10^{-5}	12.3	16	0.591	High	Brittle, fragile
Si (high resistivity)	4×10^{-4}	11.9	50	0.9	High	Brittle, strong
Air	-	1	0	0.0003	Low	

(The data in the table can vary by different sources)

Silicon wafer is the most common material used as a substrate in MEMS and ICs because it has good electronic and mechanical properties. It is sensitive to stress,

temperature, magnetic fields, and radiation. It can also form a high quality insulating oxide, and it can be anisotropically etched with high selectivity by several etchants.

Gallium Arsenide (GaAs) is also used as a substrate in MEMS. Even though it is more expensive and difficult to process compared to Si, GaAs is still used since very high speeds in MEMS devices are possible.

Crystalline quartz is also used in some MEMS applications, particularly ones that utilize the piezoelectric effect of quartz. Quartz is more difficult to etch than silicon due to its high anisotropy. In addition, fused (amorphous) quartz is an excellent mechanical material and used as electrical isolation and thermal insulation.

MEMS cantilevers in EFM measurement will be fabricated on high resistivity Si substrate owing to its reduction losses and compatibility with MMICs. High resistivity Si with a resistivity of 1000 Ω-cm is used for fabrication CPW cantilevers in this thesis. Air is the best dielectric, having lowest loss, and lowest dispersion owing to low variation of dielectric constant with frequency.

2.2.1.3 Conductor selection

A conductive CPW cantilever provides an electrical path to the probe tip for the electrostatic accumulation of charge. Such charge can produce the electrostatic force between the cantilever probe and sample. EFM uses the localized electrostatic force to deduce the internal high frequency signals of an IC.

At higher frequency, the conductor currents are forced to crowd towards the outer surface of the conductor. This 'skin effect' reduces the effective cross-sectional area available for conduction of current resulting in the increase of conductor resistance. The skin depth is the depth from the outer surface of the conductor at which the current falls to '1/e' of its value. It can also be thought as the equivalent thickness of a conductor at dc current having the same resistance. The skin depth is defined as

$$\delta = \frac{1}{\sqrt{\pi f \sigma \mu}} \qquad \textbf{(2.2)}$$

where μ is permeability, σ the conducitivity of the metal.

The attenuation increases very rapidly once the conductor thickness t of CPW line becomes less than two to three times the skin depth δ. Thus, the conductor thickness should be designed to at least 3 times more than skin depth δ so as to minimize losses. The conductivity values and skin depth at 10 GHz for selected bulk conductor materials are given in Table 2.2 [35].

Table 2.2 Conductivity for selected bulk conductor materials [35]

Material	Conductivity S/m	Relative Permeability (μ_r)	Skin depth at 10 GHz ($\times 10^{-7}$m)
Poly-Si	1.3×10^{3}	1	1395.9
Au	4.1×10^{7}	1	7.86
Al	3.81×10^{7}	1	8.14
Cu	5.81×10^{7}	1	6.6
Ag	6.17×10^{7}	1	6.4
Ni	1.45×10^{7}	600	0.5

2.2.1.4 Insulator selection

The study in [36] indicates that there is no significant improvement in the attenuation constant beyond 2500 Ω-cm wafer resistivity. A Si wafer with a resistivity greater than 2500 Ω-cm is a viable substrate for MMIC applications because the measured attenuation constant of a CPW on Si wafer of resistivity 2500 Ω-cm is about the same as that of a CPW on a semi-insulating GaAs wafer. In order to get low attenuation, the resistivity of the Si wafer should be greater than 2500 Ω-cm.

When the CPW conductors are in direct contact with the high resistivity Si wafer, the signal suffers the least attenuation. However, a dc leakage current can flow between the CPW center strip conductor and the ground strip conductor, since the Si wafer is not a perfect insulator [37]. The leakage current is not a concern in the case of passive devices such as couplers and filters, but it can be a serious problem when active devices are integrated. A simple solution to block the leakage current is to deposit a thin insulator [19], such as SiO_2 or Si_3N_4 layer, between the silicon wafer and the metal conductors as shown in Figure 2.6. The thickness t_1 of the SiO_2 insulating layer is etched away in the

slot regions. The CPW attenuation is almost independent of the dc bias currents on the conductors and is about the same as when the metal is in direct contact with the high-resistivity silicon.

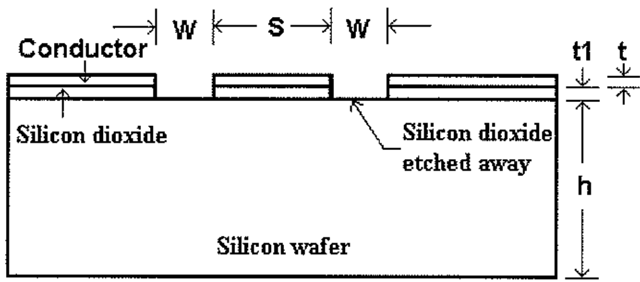


Figure 2.6 CPW on a silicon wafer with a thin SiO_2 interfacial layer.

However, the high-resistivity Si wafers are more expensive than the standard CMOS grade Si wafers. The standard CMOS process uses CMOS grade wafers with resistivity typically on the order of 0.5 to 20 Ω-cm. A simple solution is to use a thick insulating layer of SiO_2 or polyimide on low resistivity wafer [38][39].

2.2.1.5 Thin film selection

MEMS structures are made by depositing and patterning thin films on a substrate and by etching the unwanted films and substrate. Table 2.3 and Table 2.4 give the electrical properties [40][41] and the deposition methods and typical applications of some films in MEMS fabrication [42], respectively.

Although film selection for a stressed MEMS CPW cantilever is in accordance with the requirements discussed in the above section, there are still other issues we should consider, such as conductor film adhesion with substrate. Many metals adhere well to Si, but not to oxide. Highly oxidizable metals (Al, Ti, Cr) adhere well to oxide. It is necessary to deposit a thin adhesion layer of a reactive metal beneath a relatively non-reactive metal. This is absolutely necessary for Au, Pt, and other low-reactivity metals. Cu is an excellent thermal conductor and is commonly used in MEMS. It is a slightly

stronger material than pure Al. Al is always used because it is easy to etch, adheres to Si, and is chemically stable. In my research, CPW lines are fabricated using thermal evaporation to deposit a thin Al layer first and then a Cu layer on a thin SiO_2 insulating layer above the Si wafer. The Al layer promotes adhesion of the next Cu layer deposited above it.

Table 2.3 Electrical properties of some thin films [40][41]

Material	Dielectric constant ε_r	Resistivity (Ω-cm)	Relative Permeability (μ_r)
SiO_2	3.9	10^{12}	1
Si_3N_4	7.5	10^{15}	1
Poly-Si	11.9	7.5×10^{-4}	1
Polyimide	3.9	2.3×10^{16}	1
Au	1	2.44×10^{-6}	1
Al	1	2.82×10^{-6}	1
Cu	1	1.72×10^{-6}	1
Cr	1	12.9×10^{-6}	
Ag	1	1.63×10^{-6}	1
Ni	1	6.84×10^{-6}	500

(The data in the table can vary in different sources)

Table 2.4 Deposition methods and typical applications of some thin films [42]

Material	Deposition methods	Function
Photoresist	Spin coating	Etch mask, planarization
Polyimide	Spin coating	Electrical isolation, planarization, microstructure
SiO_2	Thermal oxidation, sputtering, CVD	Electrical and thermal isolation, etch mask, sacrificial layer, encapsulation
Si_3N_4	Sputtering, plasma CVD	Electrical and thermal isolation, etch mask, passivation layer, encapsulation
Polysilicon	CVD, sputtering, plasma CVD	Conductor, piezoresistor, microstructures
Au	Evaporation, sputtering, electroplating	Electrical conduction
Al	Evaporation, sputtering, plasma CVD	Electrical conduction
Cu	Evaporation, sputtering	Electrical conduction
Cr	Evaporation, sputtering, electroplating	Electrical conduction, adhesion layer
Pt	Sputtering	Electrical conduction

2.2.2 Mechanical considerations

2.2.2.1 Residual stress and fatigue

Films, such as metal materials, and SiO_2 or Si_3N_4 layers, are either grown or deposited at high temperatures. The residual stresses at room temperature are caused by the difference between the thermal expansion coefficients of the deposited film and substrate or other films shown in Table 2.5. Thermal mismatch is not the only source of the film stress. Intrinsic stresses usually result from the nonequilibrium nature of thin film deposition process. Chemical reaction, doping, lattice mismatch, rapid deposition (evaporation or sputtering), and film thickness can all lead to very highly stressed films.

Tensile forces pull on a surface and compressive stresses push on a surface. SiO_2 film is naturally compressively strained on silicon, while Si_3N_4 film is often highly tensile stressed on silicon. Refractory metals and their compounds generally have high stress, Cr and NiV in the tensile region, while TiW or TaN exhibit large compressive stress. Low melting point materials (Al, Au) tend to have lower stress and high melting point materials (Ti, W, TiN) tend to have high stress.

Residual stress can be detrimental or advantageous depending on the applications. Extreme stress levels can result in localized fracture of the film, and separation from the wafer. An additional anneal reduces the intrinsic stresses. In addition, usually coating the cantilever uniformly with the same amount of material, on the frontside and backside of a substrate, can compensate for this stress. In this thesis, choosing the conductor film makes use of the high stresses to fabricate the stressed CPW cantilevers. The residual stress must be carefully considered during the MEMS design process. The theoretical discussion will be given latter in section 4.1. Thus, the design of a stressed CPW cantilever is a compromise between stress and fatigue.

Fatigue reliability poses limitations on the lifetime of a MEMS CPW cantilever. For long life fatigue design, the structure must operate at a stress level that is considerably lower than the yield strength. When a material fatigues, tiny cracks appear as a result of local stress concentration and grow with etch cycle until the material breaks.

The fatigue life of the material for a cantilever can be improved by reducing defects such as cracks, number of grain boundaries, inclusions, and pores. In addition, the amorphous microstructures are better compared to polycrystalline microstructures for long life fatigue cycling, since grain boundaries create stress concentrations for crack initiated fatigue failures [43][44]. Silicon wafer with high purity crystalline structure has the desirable quality, defect free and is often used for high-quality microstructures.

Table 2.5 lists the mechanical parameters for some important materials [40][41][43].

Table 2.5 Mechanical properties of some materials

Material	Yield Strength (10^9 N/m^2)	Young's Modulus (GPa)	Density (g/cm^3)	Thermal Conductivity (W/cm °C)	Thermal expansion Coefficient (10^{-6} / °C)
SiO_2	8.4	73	2.2	0.014	0.5
Si_3N_4	14.0	385	3.1	0.2	0.8
Al_2O_3	15.4	530	4	0.5	5.4
SiC	21	700	3.2	3.5	3.3
Poly-Si	7	150	2.33	20-30	2.33
GaAs	2	85.9	5.32	0.46	6.86
Si	7	190	2.3	3.5	3.3
Au	0.32	80.0	19.4	3.2	14.3
Al	0.2	70.0	2.7	2.4	25.0
Cu	0.26	130	8.89	3.98	16.6
Ag		76	10.5	4.17	19.2
Ni	0.59	210.0	9.0	0.9	12.8
W	4	410	19.3	1.78	4.5
Pt		147	21.4	0.73	8.9
Steel	4.2	210.0	7.9	1.0	12.0
Diamond	53	1035	3.5	20	1

(The data in the table may vary in different sources)

2.2.2.2 Laser beam deflection detection system in EFM

Figure 2.7 shows a stressed CPW cantilever in EFM voltage measurement. In comparison with a straight conventional cantilever, it can measure deep trenches and reduce interference with structure such as bond wires. Figure 2.8 shows a stressed CPW cantilever mounted in a laser beam deflection system for EFM measurement. A laser

beam is focused and reflected off the end of the center cantilever beam. A photodetector can detect the deflection of the stressed cantilever resulting from an electrostatic force. The deflection is measured by the shift in the reflected spot at the detector caused by the change in the angle of reflection of the laser beam.

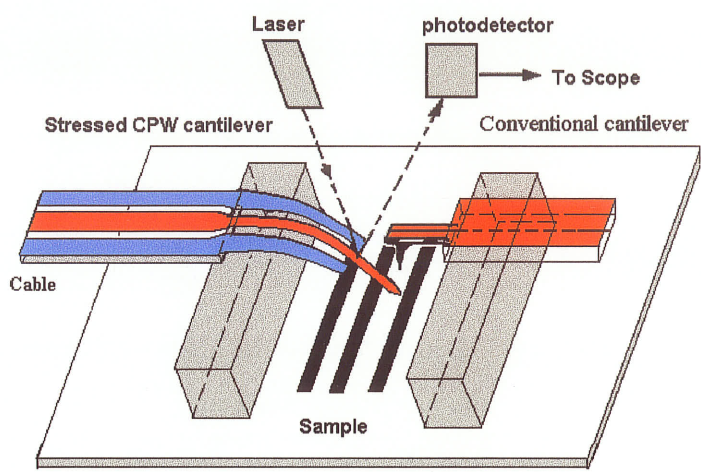


Figure 2.7 A stressed CPW cantilever in EFM voltage measurement.

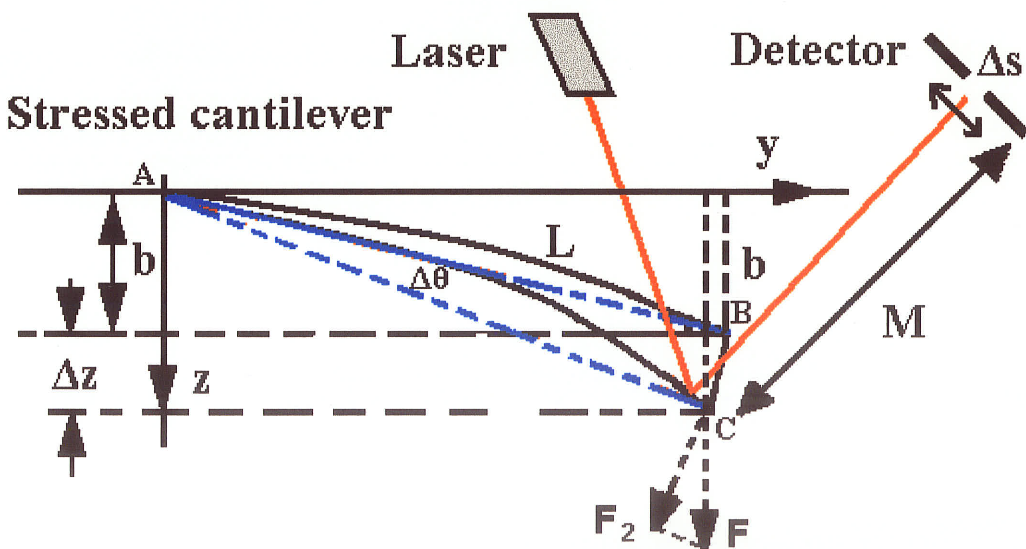


Figure 2.8 Equivalent model of a stressed CPW cantilever in laser beam deflection system.

The bending height of a stressed cantilever when it is a freestanding beam is b. The length of the cantilever is L and the lever-detector spacing is M. The lengths of straight

line between point A and point B and between point A and point C are assumed to be equal to the length L of the stressed cantilever when circular arc of the stressed cantilever is small. That is, circular arcs of AB and AC are equal to the length L of the straight line AB and AC, respectively. This assumption is not valid for large bending heights. Using the unbent beam formulation, the deflection due to a force $\bar{F}$ applied perpendicularly at the end of the stressed cantilever is given by [40]:

$$z(y) = \frac{F_2}{6EI}(3Ly^2 - y^3) \tag{2.3}$$

$$\Delta z + b = \frac{F_2}{6EI}(3Ly^2 - y^3)$$

where E is the Young's modulus, and I is the moment of inertia of the cantilever ($I = {wt^3}/{12}$ for a rectangular beam).

$$d(\Delta z) = \frac{F_2}{6EI}(6Ly - 3y^2)dy$$

$$y = \sqrt{L^2 - b^2}$$

$$d\Delta z = \frac{F_2}{6EI}(6L\sqrt{L^2 - b^2} - 3(L^2 - b^2))dy$$

$$d\Delta z \approx \frac{F_2}{2EI}\left[2L^2(1 - \frac{1}{2}\frac{b^2}{L^2} - \frac{1}{8}\frac{b^4}{L^4}) - L^2 + b^2\right]dy$$

The signal difference from the deflection detector measures the deviation angle from the initially stressed cantilever beam. For small deflection the angle at the end of the stressed cantilever is given by

$$\Delta z \approx L\Delta\theta$$

$$\Delta\theta \approx \frac{d\Delta z}{dy} = \frac{F_2 L^2}{2EI}(1 - \frac{b^4}{4L^4}) \tag{2.4}$$

Since the spring constant of a stressed cantilever is approximately equal to that of an unbent rectangular cantilever $k = 3EI/L^3$ and $F_2 = k\Delta z$, above equation becomes:

$$\Delta\theta \approx \frac{3\Delta z}{2L}(1 - \frac{b^4}{4L^4}) \tag{2.5}$$

Let Δs be the laser spot displacement when the end of the cantilever is deflected from 0 to Δz. Therefore, using small angle approximation ($\Delta s << M$), Δs can be given:

$$\Delta s \approx \frac{3M\Delta z}{L}(1-\frac{b^4}{4L^4}) \quad \textbf{(2.6)}$$

A factor of 2 is introduced since the angular deflection of the reflected beam is twice the angular deflection of the cantilever. If $b = 0$, the above equation becomes the deflection of the conventional straight cantilever due to an electrostatic force and gives as [13]

$$\Delta s \approx \frac{3\Delta z}{L}M \quad \textbf{(2.7)}$$

In order to find the relationship between the cantilever deflection Δz and the resulting difference signal i_d detected at the split photodetector, we model the laser as a Gaussian beam and estimate the difference photocurrent between two photo-cells when the reflected beam moves Δs. The i_d is given as [45]

$$i_d = \frac{2Nq}{\sqrt{\pi}}\left(\frac{\sqrt{2}\Delta s}{w}\right) \quad \textbf{(2.8)}$$

where N is the total number of photons in the incident beam on the detectors per unit time and q is the charge of an electron. The parameter w is a radius of beam power distribution and we assume the separation of the two photo diode cells is small compared to w. Substituting equation (2.6) into equation (2.8) gives

$$i_d \approx \frac{6\sqrt{2}NqM\Delta z}{\sqrt{\pi}Lw}\left(1-\frac{1}{4}\left(\frac{b}{L}\right)^4\right) \quad \textbf{(2.9)}$$

Since the magnitude of deflection Δz at resonant frequency f_r is enhanced by a factor of Q over that at other frequencies, the i_d at resonant frequency can be rewritten as

$$i_d\Big|_{f_r} \approx \frac{6\sqrt{2}NqMQ\Delta z}{\sqrt{\pi}Lw}\left(1-\frac{1}{4}\left(\frac{b}{L}\right)^4\right) \quad \textbf{(2.10)}$$

A minimum detected displacement of a typical straight beam deflection technique was reported as 7.9×10^{-6} nm / $\sqrt{Hz}$ [46].

This formula suggests that the output signal i_d from the laser deflection detection system is linearly proportional to the cantilever deflection Δz. The sensitivity of a cantilever is proportional to the Q and by increasing the lever-detector length M, the sensitivity can also be enhanced. It also suggests that if the bending height b is much less than cantilever length L, it can vary in a large scale and does not affect the sensitivity of the cantilever. This fact has produced the idea of using the stressed MEMS CPW cantilever to measure the deep trenches and narrow structures.

2.2.2.3 Important mechanical parameters in EFM

The important mechanical parameters in a cantilever system used in EFM are spring constant (k), resonant frequency (f_r), and quality factor (Q). The material parameters that determine the spring constant and resonant frequency are mainly the Young's modulus and cantilever dimensions.

In EFM measurement, the tip hovers a short distance from a sample. An ideal cantilever should have a low spring constant because the low spring constant makes the tip sensitive to force, while a high spring constant is preferable to avoid unwanted contact with the sample. For the rectangular beam, $k = 3EI/L^3$ as determined by cantilever's dimensions and Young's modulus.

The resonant frequency f_r, a very important parameter, is dependent on varying the cantilever dimensions. It must be high enough so that the cantilever can suppress noise efficiently. Cantilevers to be used in noncontact measurement have a resonant frequency of a few tens kHz. The formula of resonant frequency is $f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m+0.24m_L}}$ as previously stated in section 1.2.2.

The quality factor Q should be as high as possible for non-contact mode of operation because the sensitivity of EFM is proportional to the Q [47]. A cantilever with a low Q oscillates with lower amplitude for a given excitation energy. The lower the Q of the

cantilever, the lower the signal-to-noise ratio. Typical values of Q in a standard probing environment are 10-30. The Q for silicon cantilever can increase to over 20000 in a vacuum [47].

For the requirements of MEMS fabrication and EFM measurements, we hope to fabricate the properties of the stressed MEMS CPW cantilever as follows:

Geometry: $L = 600 \pm 100$ μm, $w = 40 \pm 5$ μm, $t = 1 \pm 0.1$ μm

Spring constant: $k = 0.005$- 0.01 N/m

Resonant frequency: $f_{r1} = 2$ kHz

Q factor: $Q = 10$

2.2.3 Electrical and mechanical considerations

The CPW cantilever is designed to meet the electrical and mechanical requirements as described above. The values of the mechanical and electrical properties of materials depend strongly on microstructure, such as whether the material is single crystal, polycrystal, or amorphous [43]. These process-sensitive material properties depend on the technology and process parameters used in the MEMS fabrication of CPW cantilever.

The cantilever tip hovers a short distance from a sample. If the coaxial open-ended waveguide is tapered to a tip, it can behave as a non-uniform, mismatched transmission line and may even exhibit antenna effects, which collects far-field radiation from interfering source. The input signals to the probe should be propagated undisturbed to the tip for EFM. Thus, the electrical properties require the lowest insert loss and lowest return loss along the transmission line path and must be considered in the CPW cantilever design. The insertion loss will be affected by losses in the beam metallization. At low frequencies the ohmic loss is dominant in the CPW cantilever, while at higher frequencies the skin losses are significant as discussed in section 2.2.1.3.

A trade-off exists between spring constant and resonant frequency. The mechanical properties require low spring constant which can be achieved using long cantilever beam. Both spring constant and resonant frequency vary inversely with cantilever length. A long cantilever, however, leads to lower resonant frequency. To increase resonance frequency

without increasing cantilever stiffness requires a reduction in mass, hence there is a trend towards less massive beams.

2.3 CPW dimension design considerations and simulation results

This section presents the CPW transmission line design. It focuses on selection considerations of CPW conductor and substrate dimensions and simulation of the designed CPW cantilever.

2.3.1 Basic theory of CPW transmission line

2.3.1.1 Characteristic impedance and effective dielectric constant

The cross-sectional view of a CPW ungrounded structure on a dielectric substrate is shown in Figure 2.9. The CPW center strip conductor width S is equal to $2a$ and the distance of separation between the two semi-infinite ground planes is $2b$. Consequently the slot width W is equal to $b-a$. The thickness of the CPW conductors is t. The dielectric thickness is h and the corresponding relative dielectric constant is ε_r. The CPW conductor and dielectric substrate are assumed to have infinite conductivity and a lossless dielectric constant, respectively. Hence the structure is considered to be lossless. Further, the dielectric substrate material is considered to be isotropic. Characteristic impedance and effective dielectric constant of the CPW in terms of the CPW dimensions can be expressed as the following closed form equations [48][49], respectively:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{reff}}} \frac{K(k_0^{'})}{K(k_0)} \quad \textbf{(2.11)}$$

$$\varepsilon_{reff} = 1 + \frac{(\varepsilon_r - 1)}{2} \frac{K(k_1)}{K(k_1^{'})} \frac{K(k_0^{'})}{K(k_0)} \quad \textbf{(2.12)}$$

Accurate expressions for the ratio $K(k)/K(k^{'})$ are given below:

$$\frac{K(k)}{K(k')} = \begin{cases} \frac{1}{\pi}\ln[2(1+\sqrt{k})/(1-\sqrt{k}), & (0.5 \le k^2 \le 1) \\ \pi / \ln[2(1+\sqrt{k'})/(1-\sqrt{k'}), & (0.0 \le k^2 \le 0.5) \end{cases} \quad \textbf{(2.13)}$$

The terms $K(k_1)$ and $K(k_0)$ are the complete elliptic integrals of the first kind with moduli k_1 and k_0 which are given by

$$k_1 = \frac{\sinh(\pi S / 4h)}{\sinh\{[\pi(S + 2W)]/4h\}} \quad \textbf{(2.14)}$$

and

$$k_0 = \frac{S}{S + 2W}, \quad \textbf{(2.15)}$$

The terms $K(k'_1)$ and $K(k'_0)$ are complementary moduli given by

$$k'_0 = \sqrt{1 - k_0^2}$$

$$k'_1 = \sqrt{1 - k_1^2} \quad \textbf{(2.16)}$$

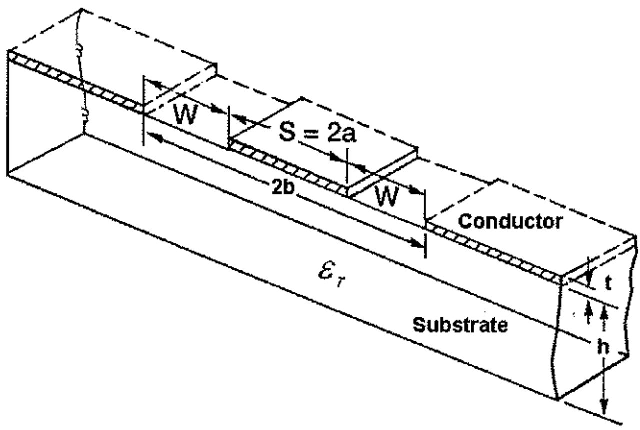


Figure 2.9 A CPW transmission line on substrate [19].

A study of CPW properties shows that when the substrate thickness (h) is less than twice the slot width (W), the deviation from the results of an infinitely thick dielectric substrate is about 10 to 15 percent [50]. In comparison with spectral domain method, the accuracy of the conformal mapping results is better than 1 percent for a wide range of

physical dimensions and available dielectric materials [51]. Although the above conformal mapping expressions are rigorously valid at zero frequency, they can also be used for design of MMICs at millimeter wave frequencies [51]. The CPW impedance has also been experimentally determined from time domain reflectometer or from scattering parameter measurements of through CPW lines [52].

2.3.1.2 Closed form equations for CPW attenuation constant

1) Conformal mapping method

Figure 2.9 shows the CPW structure with ground planes tending to infinity. In the conformal mapping method the total CPW attenuation is expressed as the sum of the attenuation due to dielectric losses in substrate and the attenuation due to the conductor losses in the center strip and the ground planes. The radiation losses are neglected since it begins to play a role at very high frequencies [53]. The attenuation constant due to dielectric loss is expressed as [54]

$$\alpha_d = \frac{\pi}{2\lambda_0}\frac{\varepsilon_r}{\sqrt{\varepsilon_{reff}}}\frac{K(k_1)}{K(k_1')}\frac{K(k_0')}{K(k_0)}\tan\delta \qquad \textbf{(2.17)}$$

where λ_0 is the free space wavelength in meters, $\tan\delta$ is the dielectric loss tangent, ε_r is the relative dielectric constant, and ε_{reff} is the effective dielectric constant of the substrate.

An expression for attenuation constant a_c due to conductor loss in the center strip conductor and ground planes of CPW is given below. The assumption made in deriving this expression is that the thickness t of the CPW conductors is far greater than the skin depth δ in the metal. Typically t would be greater than 5δ. The attenuation constant is given by

$$\alpha_c = \frac{R_c + R_g}{2Z_0} \qquad \textbf{(2.18)}$$

where R_c is the series resistance in ohm per unit length of the center strip conductor and is given by

$$R_c = \frac{R_s}{4S(1-k_0^2)K^2(k_0)}\left[\pi + \ln\frac{4\pi S}{t} + k_0 \ln\frac{1+k_0}{1-k_0}\right] \quad (2.19)$$

R_g is the distributed series resistance in ohm per unit length of the ground planes and is given by

$$R_g = \frac{k_0 R_s}{4S(1-k_0^2)K^2(k_0)}\left[\pi + \ln\frac{4\pi(S+2W)}{t} - \frac{1}{k_0}\ln\frac{1+k_0}{1-k_0}\right] \quad (2.20)$$

and Z_0 is the CPW characteristic impedance. The term R_s is the skin effect surface resistance given by

$$R_s = \frac{1}{\delta\sigma} \text{ Ohms} \quad (2.21)$$

where σ is the conductivity of the conductor in Siemens/meter and δ is the skin depth. The total attenuation constant α is

$$\alpha = \alpha_c + \alpha_d \text{ Nepers/meters} \quad (2.22)$$

2) Measurement-based design equations

The measured attenuation characteristics of CPWs fabricated on GaAs, InP and high-resistivity silicon wafers are used to obtain a closed form empirical equation to predict the attenuation constant α as follows [55]:

$$\alpha = pf^q \text{ (dB/cm)} \quad (2.23)$$

where

$$p = \sqrt{\frac{\varepsilon_r + 1}{2}}\left[\frac{45.152}{(SW)^{0.41} e^{2.127\sqrt{t}}}\right] \quad (2.24)$$

$$q = 0.183(t + 0.464) - 0.095k_t^{2.484}(t - 2.595) \quad (2.25)$$

$$k_t = \frac{S + \Delta t}{S + 2W - \Delta t} \tag{2.26}$$

$$\Delta t = \frac{1.25t}{\pi}\left[1 + \ln\frac{4\pi S}{t}\right] \tag{2.27}$$

and S, W, and t are in micrometer, f is in gigahertz.

The formulas are valid for $0.5 < t < 3$ μm, $0.2 < S/(S+2W) < 0.7$, $10 < S < 80$ μm, and $1 < f < 40$ GHz, which covers the range of parameters commonly used for MMIC design. They can be used to predict the optimum dimensions of our CPW cantilever in order to minimize the losses and satisfy the design requirements. In the experimental CPW formulas, the propagation parameters are made independent of the ground plane width g and the substrate height h by choosing g to be greater than $4S$ and h greater than $3(S+2W)$.

3) Accuracy of closed form equations

The attenuation constant predicted by the conformal mapping method underestimates the values at low frequencies. This is attributed to the thick metal assumption. The average error for the conformal mapping method is on the order of 13.6 percent. The measurement-based design equations result in an average error on the order of 4.7 percent [55]. The methods presented in [56] and [57] do not assume the metal to be thick and the difference between the measured and calculated attenuation constant is nearly independent of frequency. The average errors for these two methods are on the order of 10.8 and 11.0 percent, respectively. Thus among the above closed-form equations, the method of measurement-based design equations has the least average error.

2.3.2 Characteristic and dimension considerations of CPW line

Silicon and copper are selected as the substrate and conductor of our CPW cantilevers, respectively. The selection considerations of CPW dimensions will refer to the methods and observations discussed in the previous section.

The dimensions of the CPW center strip, the slot, the thickness and dielectric constant of substrate determine the CPW effective dielectric constant, characteristic impedance and attenuation and vice versa. The dimensions of the CPW transmission line must be chosen so as to produce the lowest possible insertion loss and the lowest possible mismatched loss. These come from the characteristic impedance of CPW line on Si holder being different from 50 Ω as well as losses in the cantilever metallization and contact resistance loss. In addition, increasing resonance frequency without increasing cantilever stiffness requires a reduction in mass, hence a trend towards smaller beams.

A tapered CPW cantilever is proposed to satisfy the mechanical and electrical design requirements. CPW cantilevers with ground connected and opened are mounted by a Si holder as shown in Figure 2.10. Both dimensions of the CPW line on Si wafer and CPW cantilever in air are different. The tip is fabricated at the end of the CPW central strip suspended in the air.

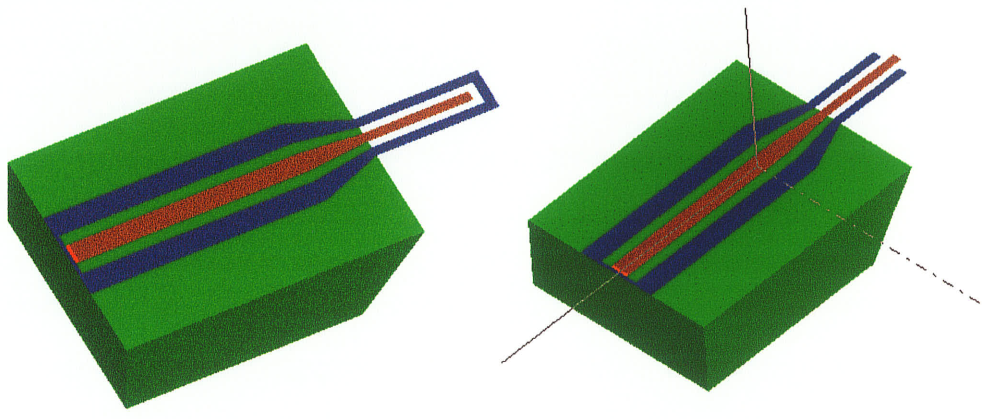


Figure 2.10 CPW cantilevers with (a) ground connected; (b) ground opened.

Since the CPW cantilever is fabricated on different substrates, to analyze the losses of the designed CPW cantilever, the CPW cantilever is divided into three parts and each part is treated as an individual CPW transmission line as shown in Figure 2.11.

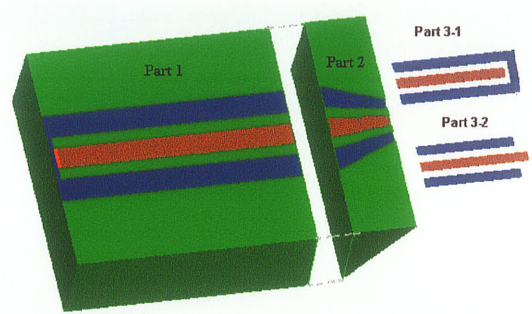
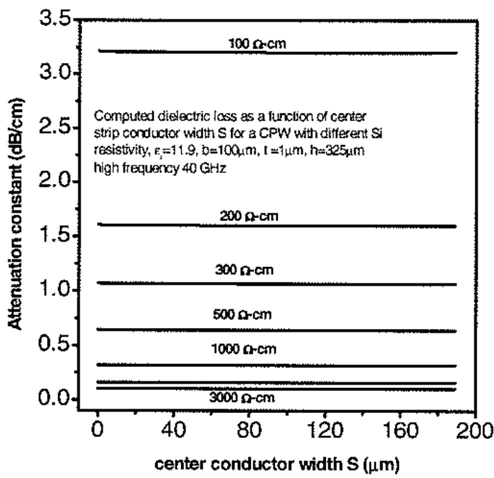


Figure 2.11 Three parts of CPW cantilever with ground connected or ground opened.

2.3.2.1 CPW attenuation constant

The total losses of a CPW line on Si wafer (holder) are mainly dielectric loss in the substrate and conductor loss in the center strip and ground strips. Figure 2.12 shows the computed dielectric loss and total losses using equations (2.17) and (2.22) at 40 GHz as a function of center strip width S for a CPW with different resistivity of the Si substrates, respectively. Referring to Figure 2.9, the thickness of Si wafer and conductor is about 325 and 1 μm, respectively. The losses are varied by changing the center strip width S, in which the separation width $2b = 200$ μm between the ground conductors is kept constant. Note for these cases, the impedance Z_0 is varying. The low resistivity of Si substrate causes considerable losses that affect the transmitted signals. In order to keep the high frequency losses at an acceptable level, the CPW line we will use Si substrate with 1000 Ω-cm resistivity.



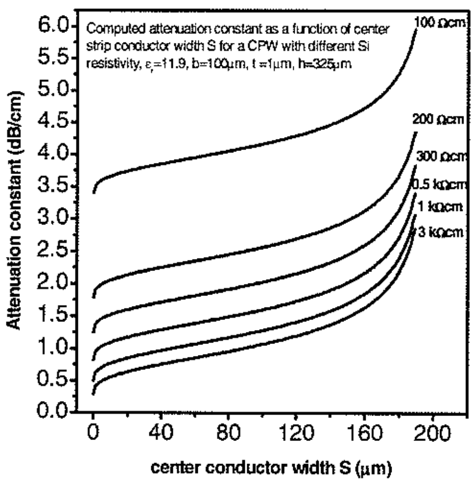
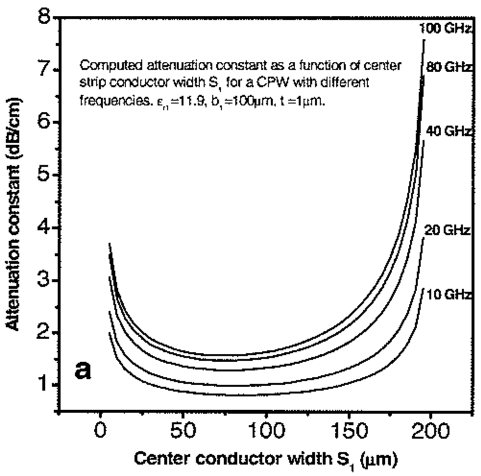


Figure 2.12 Computed losses (40 GHz) as a function of center strip conductor width S for a CPW with different resistivity of Si substrates as parameters. (a) Dielectric loss; (b) Total loss (ε_r = 11.9, b = 100 μm, t = 1 μm, h = 325 μm).

The computed losses of the CPW line on the Si holder and CPW cantilever suspended in air, as a function of center strip conductor width S for different frequencies using the equation (2.23), are shown in Figure 2.13, respectively. Although the computed data are rigorously valid for many limitations [55], they can be used to estimate the optimum dimensions of CPW cantilevers. Since substrate thickness is larger than $2b$ for all the lines, the results are independent of the substrate thickness [55][58]. The CPW line exhibits an acceptably low loss for S and b over a reasonable range. When the CPW center strip conductor becomes very narrow or the slot width becomes very small, the loss becomes very large. The loss of CPW increases with increase frequency. For a fixed frequency, the CPW loss initially decreases and later increases with the increase of the center conductor width S. For the requirements of our design, the width $2b_1$ is chosen as 200 μm. This is mainly due to test equipment probe and bond wire requirements for connecting to the structure. The CPW line on Si substrate (part 1) has low losses for a width S_1 range of 50-125 μm as indicated in Figure 2.13 (a).



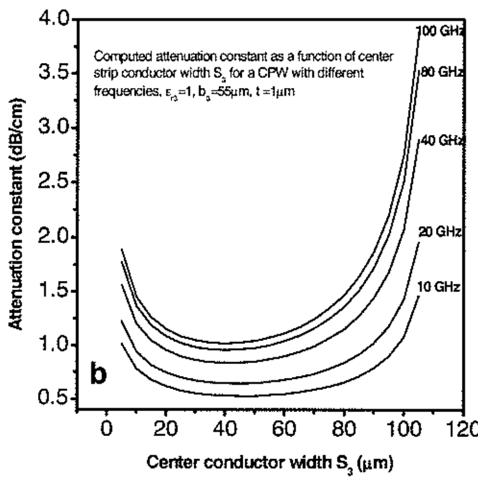


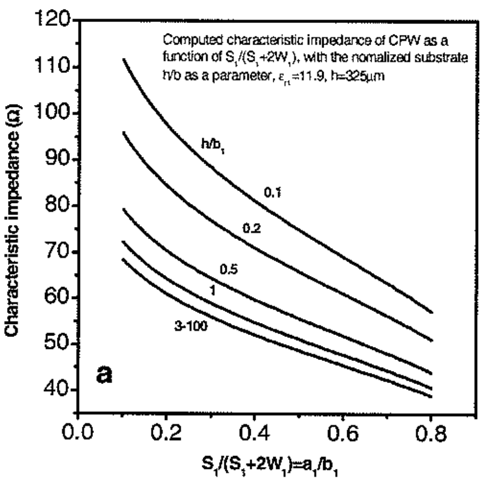
Figure 2.13 Computed attenuation constant as a function of center strip conductor width S for a CPW with different frequencies. (a) Part 1: CPW line on Si holder, $\varepsilon_{r1} = 11.9$, $b_1 = 100$ μm, $t = 1$ μm, $h = 325$ μm; (b) Part 3: CPW cantilever in air, $\varepsilon_{r3} = 1$, $b_3 = 55$ μm, $t = 1$ μm.

The CPW cantilever suspended in air (part 3) is exposed by using the backside KOH etch to remove the substrate material and leave only the desired CPW metal lines. It can be considered as being on high resistivity air-dielectric substrate [59] and reduces the effects of dielectric loss. The width $2b_3$ is chosen as 110 μm mainly due to lithographic resolution limitations of the masks we use in our lab. The CPW cantilever in air (part 3) has low losses in the width S_3 range of 30-70 μm in Figure 2.13 (b).

2.3.2.2 Characteristics and dimensions of CPW

For a given effective dielectric constant ε_{reff}, any variations in impedance are determined by the ratio of a/b. The calculated characteristics of the CPW on Si substrate using equations (2.11) and (2.12) are shown in Figure 2.14, respectively. It should be pointed out that when $h \geq 3b_1$, the characteristic impedance and effective dielectric constant are reasonably independent of the Si substrate thickness.

For the CPW structure, the study [32] showed that minimum attenuation occurs for a characteristic impedance close to 50 Ω. 50 Ω characteristic impedance in the h/b_1 = 3-100 curve for a CPW line on a 325 μm Si wafer corresponds to $a_1/b_1 \approx 0.46$ in Figure 2.14 (a). From the Figure 2.14 (b), the effective dielectric constant is about 6.8 at $a_1/b_1 \approx 0.46$ in h/b_1 = 3-100 curve. If the separation width $2b_1$ between ground strip conductors is 200 μm according to the design requirements, then $S_1 = 2a_1 = 92$ μm, $W_1 = 54$ μm. Since $h \geq b_1$ for all cases, the results are independent of the Si substrate thickness.



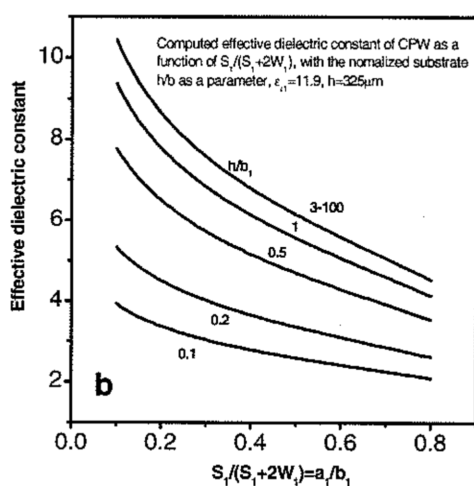


Figure 2.14 Computed characteristics of CPW on Si wafer as a function of $S_1/(S_1+2W_1)=a_1/b_1$, with the normalized substrate h/b_1 as a parameter, $\varepsilon_{r1} = 11.9$, $h = 325$ μm. (a) Characteristic impedance; (b) effective dielectric constant.

Figure 2.15 shows the characteristic impedance of a CPW line in air. The effective dielectric constant and the loss decrease as the material below the CPW cantilever is etched away. A lower effective dielectric constant results in a lower line capacitance that increases the characteristic impedance Z_0. Due to the requirements of mask resolution in our lab and for use in EFM measurements, the minimal slot width W_3 is 35 μm and a selected S_3 is approximately 40 μm. Therefore, the $2b_3$ between ground conductors is about 110 μm and a_3/b_3 is approximately 0.36. The value of $a_3/b_3 \approx 0.36$ corresponds to a

characteristic impedance of 141.8 Ω for the CPW line suspended in the air in Figure 2.15 with an effective dielectric of ε_{reff} =1. This will cause a mismatch at very high frequencies. A lower characteristic impedance may be achieved if a dielectric substrate is used under the CPW cantilever section.

Both attenuations of the CPW on Si holder and suspended in air are in the low range because the selected CPW dimensions are in the range of low losses, respectively, as studied in the section 2.3.2.1.

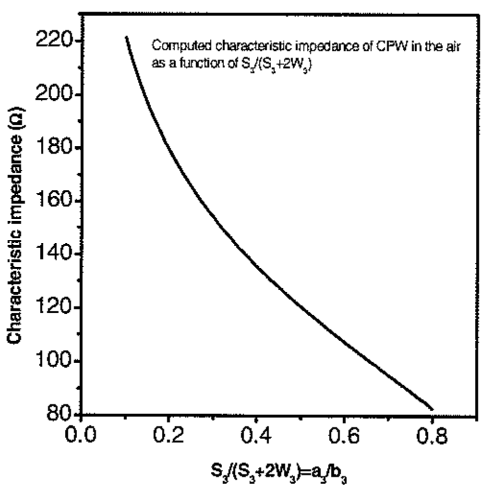
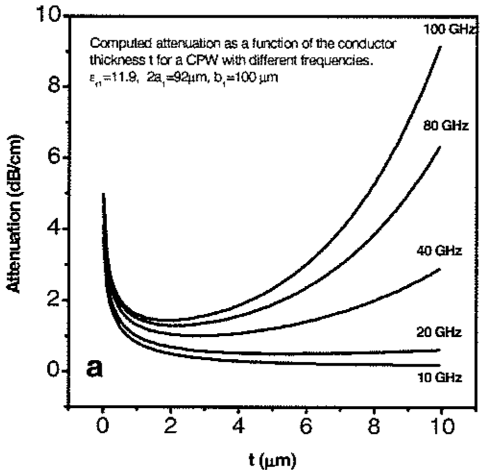


Figure 2.15 Computed characteristic impedance of CPW cantilever in air as a function of $S_3/(S_3+2W_3)$=a_3/b_3.

2.3.2.3 Conductor thickness

Figure 2.16 shows the effects of conductor thickness t on the calculated losses using equation (2.23) of a CPW on Si wafer and in air in the range of 10 to 100 GHz, respectively. For the two cases, the losses of CPW are minimal when the thickness of conductors is 1- 4 μm. The loss increases very fast when conductor thickness is below 1 μm. The attenuation increases very rapidly once the conductor thickness t becomes less than about two or three times the skip depth δ. To obtain a high resonance frequency

without increasing cantilever stiffness requires a reduction in conductor mass. Thus, we choose a 1 μm thick CPW conductor.



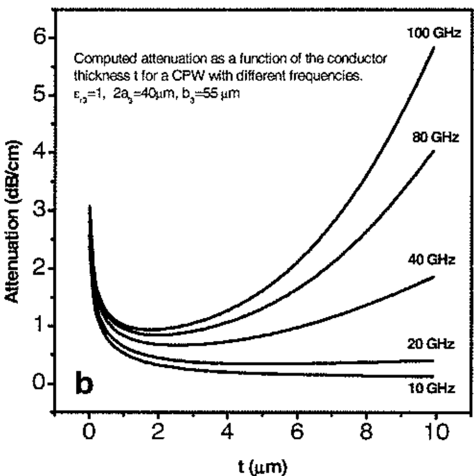


Figure 2.16 Computed attenuation constant of CPW as a function of conductor thickness t with frequency as a parameter. (a) Part 1: CPW on Si wafer. ε_{r1} = 11.9, S_1 = 92 μm, W_1 = 54 μm, h = 325 μm; (b) Part 3: CPW cantilever in air. ε_{r3} = 1, S_3 = 40 μm, W_3 = 35 μm.

2.3.3 Simulation results of a CPW cantilever

From the above theoretical calculations and analyses and the requirements of MEMS fabrication and EFM measurements, a draft of an entire CPW cantilever design is shown in Figure 2.17. It gives the dimensions of all three parts. To verify the electrical performance of the designed CPW cantilever, full electromagnetic simulation of its propagation properties is needed.

In following HFSS simulation, the effect of dc resistance is neglected and the loss tangent is assumed to be 0.02 in the frequency range 0.04-40 GHz. The HFSS method simulates the three parts of an entire CPW cantilever. The corresponding simulation results are compared to the theoretical analysis results. Using the HFSS program simulation, modification, and verification of the designed CPW cantilever is performed

until all requirements are satisfied. Finally we simulate the entirely designed CPW cantilever.

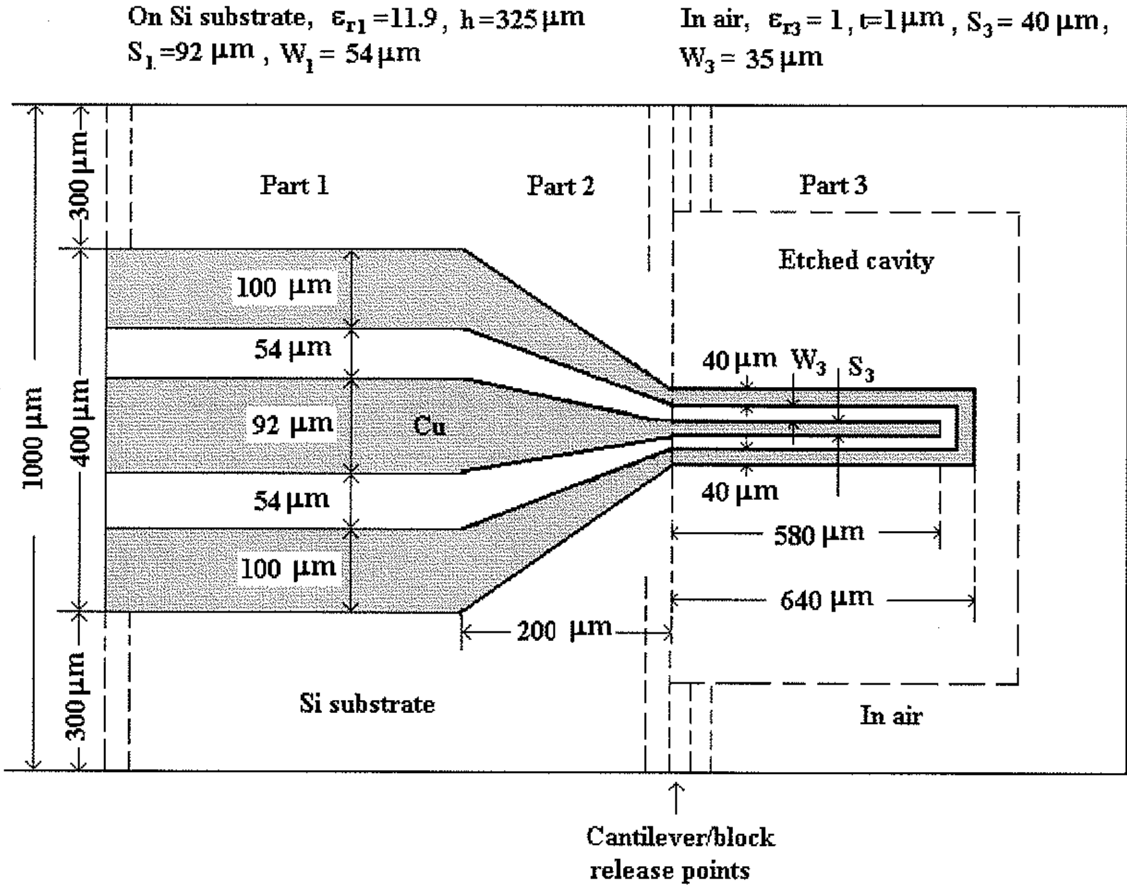


Figure 2.17 Dimensions of an entire CPW cantilever.

2.3.3.1 Part 1 –CPW on Si holder

Figure 2.18 (a) shows a photograph and HFSS simulation S-parameters of a 5000 μm CPW line on high resistivity 1000 Ω-cm Si. The maximum insertion loss S21 is less than 1.5 dB at 40 GHz, which is considered to be acceptable. The return loss S11 is observed to be better than 15 dB over the entire frequency range. It indicates that the designed CPW on Si substrate is well matched to 50 Ω characteristic impedance and the input signal can be maximally transferred to its output. Therefore, the propagation properties of

the CPW line based on the above calculated dimensions satisfy our designed requirements.

2.3.3.2 Part 2 –tapered CPW on Si holder

For the part 2 between part 1 and part 3, a 200 μm tapered CPW line as shown in Figure 2.18 (b) is necessary owing to different dimensions of CPW transmission lines. The correspondingly simulated reflection loss is 20 dB at the frequency range 0.04-40 GHz, which is very small. The transmission loss is almost equal to zero over the entire frequency range and it does not affect transmitted high frequency signals. Another method to calculate reflection and transmission losses is that the trapezoidal tapered CPW line is divided into very small rectangular sections, each of which is treated as an individual transmission line. The ABCD matrices for each transmission line are then cascaded to obtain the total ABCD matrix. From these matrices, the characteristics of the tapered CPW line are computed. The process is repeated at each frequency [28].

2.3.3.3 Part 3 –CPW cantilever suspended in the air

Figure 2.18 (c) and (d) show photographs and simulated reflection coefficients of ground opened and ground connected CPW cantilevers suspended in air. Both designs are almost the same except at the end of CPW cantilever. It is easy to understand that the HFSS simulation results show similar results. Reflection loss deduces a transmission loss ~0.004 dB at 40 GHz. They show the designed CPW suspended in air is almost lossless and has good propagation properties. It also shows that the effect of mismatch due to the line impedance Z_0 = 142 Ω and not 50 Ω does not have a significant effect up to 40 GHz. Therefore, the simulated results of the CPW in air based on calculated dimensions satisfy our requirements.

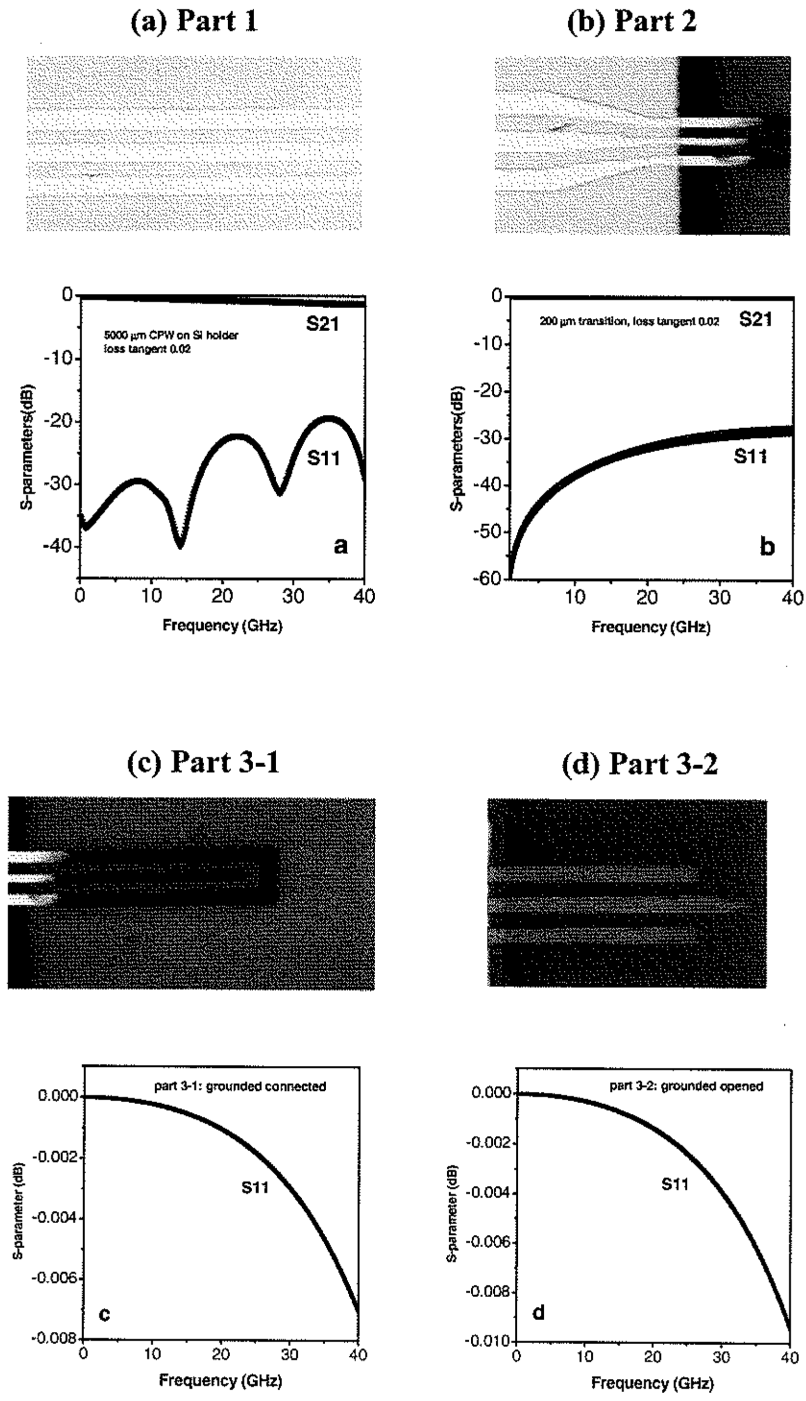


Figure 2.18 The photographs and S-parameters of three parts of a CPW cantilever. (a) Part 1: 5000 μm CPW on Si holder (Z_0 = 142 Ω); (b) Part 2: 200 μm transition on Si holder; (c) Part 3-1: ground connected 640 μm cantilever in air; (d) Part 3-2: ground opened 640 μm CPW cantilever in air (Z_0 = 142 Ω).

2.3.3.4 Simulation of entire CPW cantilever structure

The above HFSS simulation S-parameters of the three parts all satisfy the design requirements. They indicate that each part can maximize the power delivered to its output and minimize the reflected power. Now, we further simulate the entire CPW cantilever to test the design model.

Figure 2.19 (a) and (b) show the two entire CPW cantilevers, the ground connected and opened 640 μm CPW cantilevers mounted with a 5000 μm CPW line on a 1000 Ω-cm resistivity Si holder, and the corresponding simulation S-parameters at the frequency range from 0.04-40 GHz, respectively. The difference between S-parameters is small and is less than or equal to 4 percent. It is reasonable because the only difference between the two cases is that ground lines are connected or opened at the end of CPW cantilever in air. Thus, we will mainly focus on analyses of the ground connected CPW cantilever. Reflection loss results indicate a transmission loss ~1.5 dB at 40 GHz (-3 dB/2). High frequency input signals (>20 GHz) can be propagated to the tip for EFM probing.

Comparison with the simulated S-parameters for only the 5000 μm CPW transmission line on the Si holder (part 1) is shown in Figure 2.19 (c). The difference between the transmission losses deduced from reflection losses is very small and the loss of CPW cantilever suspended in air is very small. This indicates that the loss of CPW on Si holder (part 1) mainly decide the propagation properties of an entire CPW cantilever.

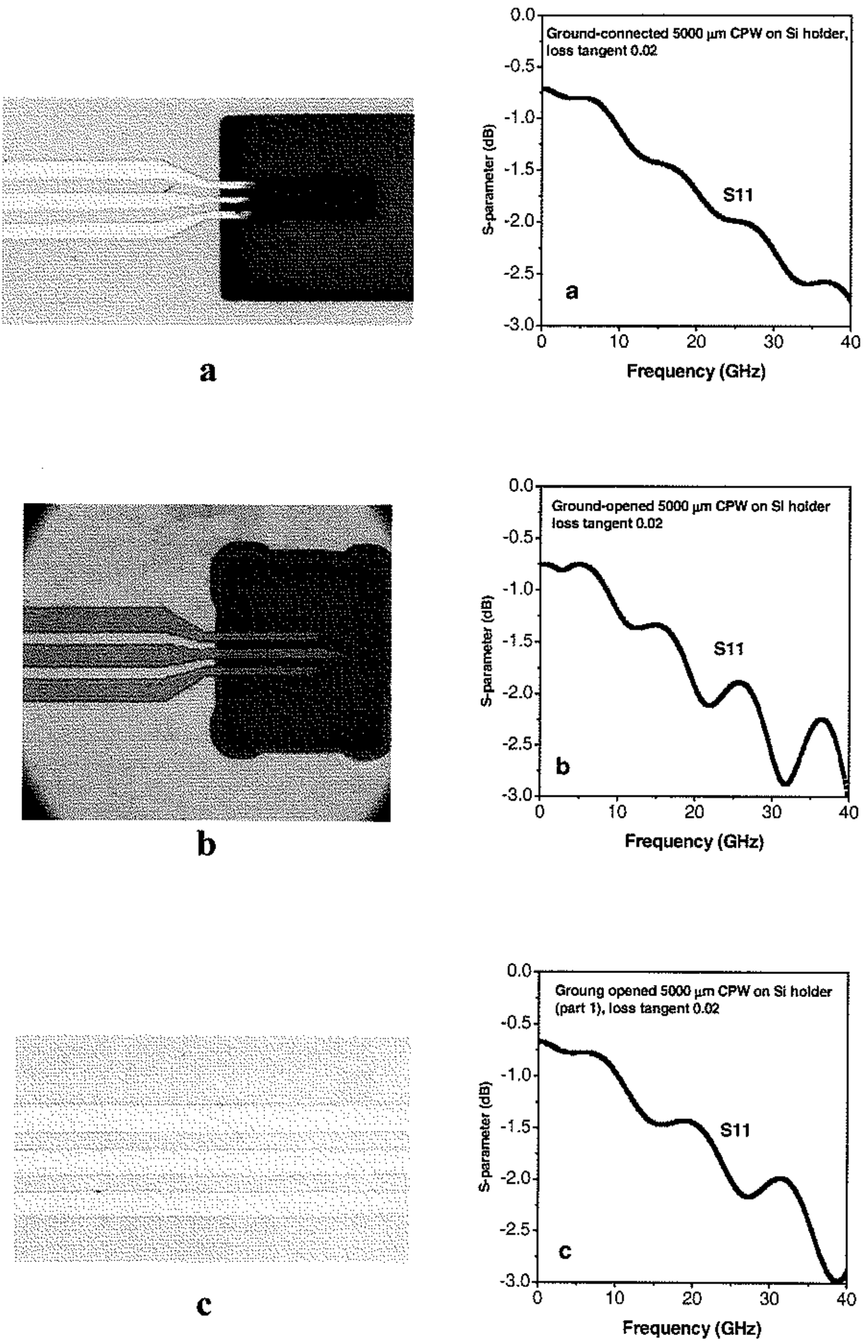


Figure 2.19 Photographs and simulated S-parameters of three cases.

(a) Ground connected CPW cantilever mounted on a 5000 μm CPW on a Si holder; (b) Ground opened CPW cantilever mounted on a 5000 μm CPW on a Si holder; (c) A 5000 μm CPW transmission line on a Si holder (part 1).

Chapter 3 Basic principles and processes of MEMS CPW cantilever fabrication

Accurate design modeling and efficient simulation, in support of greatly reduced development cycle time and cost, are the first step for the MEMS CPW cantilever fabrication. This chapter will focus on the basic principles and processes of MEMS fabrication and detailed fabrication procedures of stressed MEMS CPW cantilevers. Materials for section 3.2 are based on [40][41][42].

3.1 Introduction

MEMS are created by micromachining processes. The actual MEMS fabrication processes are comprised of several sequential steps, each of which may be repeated many times. Each of these steps adds or subtracts a single layer on a wafer. Figure 3.1 shows the main processes of a MEMS fabrication [41][42]. The MEMS fabrication can start on either a Si wafer or a Si wafer with SiO_2 insulating layers. No matter which kind of the wafer is used in MEMS fabrication, the processes of MEMS fabrication are almost the same. Figure 3.2 gives the draft of a MEMS CPW cantilever by using fabrication processes as shown in Figure 3.1. It also gives the dimensions of CPW cantilever, cavity, and V-groves on high-resistivity Si wafer.

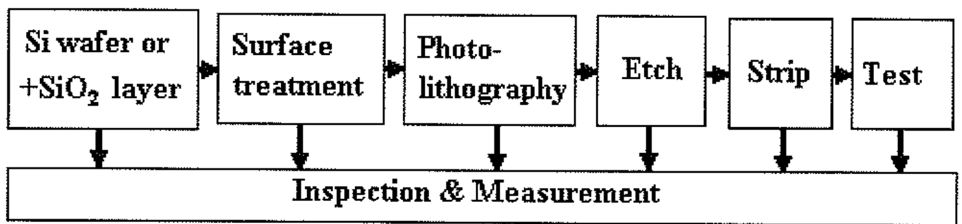


Figure 3.1 Main processes of MEMS fabrication.

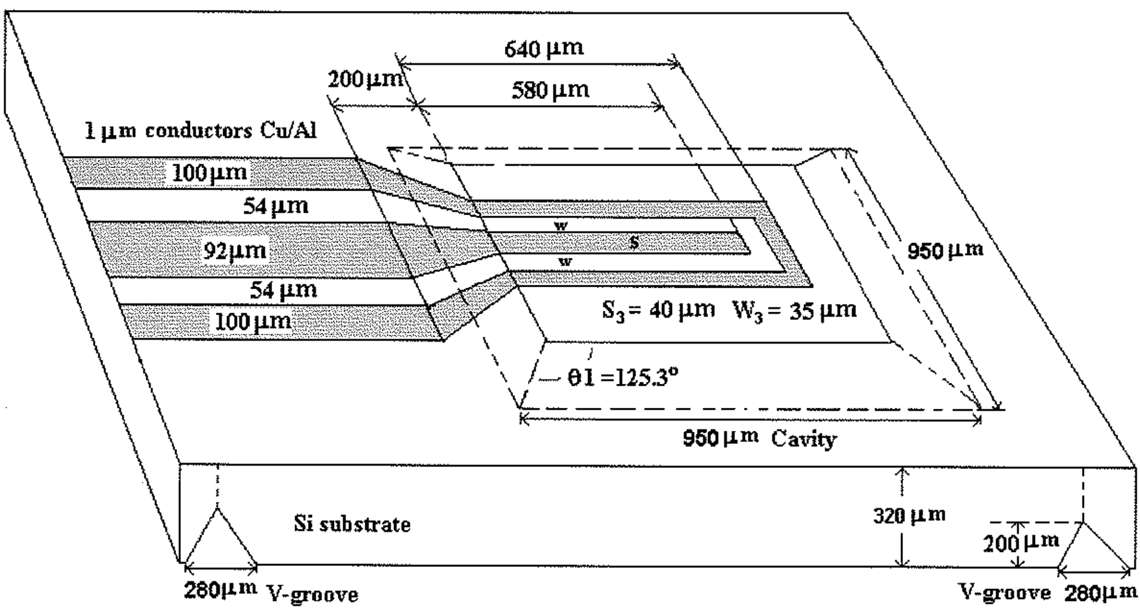


Figure 3.2 Draft and dimensions of a MEMS CPW cantilever with cavity and V-grooves.

3.2 The main processes of MEMS fabrication

3.2.1 Surface treatment

This is the most important step in MEMS fabrication and the success of lithography depends on its effectiveness. Before MEMS fabrication, a wafer must be thoroughly cleaned and free of contaminants to improve the resist adhesion to the wafer surface. Good adhesion is necessary in order to reduce the possibility of resist lifting or undercutting during the etch process.

Wafer contaminants can be broadly classified as:

- Particulates
- Organic residues
- Inorganic residues
- Unwanted oxide layers

Different cleaning methods can be used either independently or in combination with others to effectively clean a wafer surface. In general wet cleaning can be used to remove

all four types of contaminants. High pressure spraying and ultrasonic cleaning can be used to remove particulates. The RCA (popular wet chemical clean) cleaning is used to remove both organic and inorganic contaminants from the wafer surface. Acids, vapor phase cleaning and dry cleaning methods are often used to remove residues and unwanted oxide layers.

3.2.2 Photolithography

A MEMS structure always contains many elements, typically the size of a few micrometers. No physical tool is adequate for fabrication on this scale. Microelectronic patterning is performed by radiation using ultraviolet (UV) light or an electron beam. This process is called photolithography. It can transfer a pattern from a mask to a wafer surface by the application of a photosensitive film called photoresist or resist. It is not unreasonable to say that it is the most important step of the entire fabrication processes.

A block diagram of a photolithography process is shown in Figure 3.3. Photolithography brings the additive and subtractive processes together for the purposes of patterning the deposited layers on a wafer.

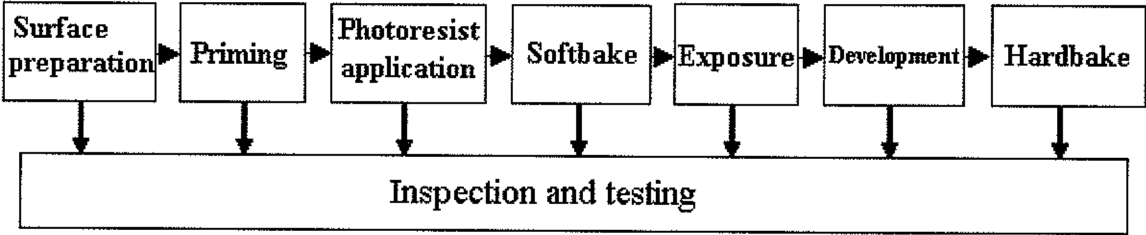


Figure 3.3 A typical photolithography process.

Priming

After the cleaning process and before application of resist, a wafer surface must be thoroughly dried and any remaining water or moisture must be removed.

Priming acts as an adhesion promoter by creating a moisture free surface and is usually done in conjunction with a dehydration bake. The wafer is dried using dry

nitrogen and a dehydration bake at about 200 °C for 2 hours can be done to further remove all of the adsorbed water attached to the wafer surface. Priming not only helps resist adhesion during the spin coat process but also decreases the likelihood of features lifting during the developing cycle. In addition, the wafer is not exposed to the environment for a long time between the cleaning process and the priming and, between the priming and resist application. This is to avoid re-deposition of contaminants on the wafer surface prior to resist application.

Photoresist

The next step is to coat the wafer with the resist or photoresist. The photoresist must adhere well to the surface, form a uniform, and defect free film on the wafer surface. Furthermore, the photoresist will resist attack by some etchants capable of removing the substrate material.

Resist is a sensitive substance whose physical and chemical properties change when exposed to UV radiation. Resist materials can be classified as positive or negative based on their radiation response. For a positive resist, the areas exposed to the UV light become solvable and are washed away in the developer solution. The unexposed regions will remain unchanged. Therefore, the pattern on wafer is the same as that on the mask. For a negative resist, the areas of the resist on the wafer exposed to UV light change from a soluble state to an insoluble state. The unexposed resist is not changed chemically and is simply rinsed away during the development step. The resulting pattern on the wafer is opposite to that on the mask.

In addition, the minimum geometries produced on the wafer using a negative resist are limited to 2 μm or larger due to swelling of the resist that occurs in the developer. However, positive processes produce minimum geometries of 0.35 μm or smaller. Therefore, positive resists are more common in MEMS fabrication because they offer higher resolution, thermal stability, and greater resistance.

The most common application method is spin coating. The resist is either dispensed statically or dynamically. The spindle is then spun rapidly at 3000-6000 rpm for 30-60 seconds. A typical resist layer varies from 0.5 μm to 4.5 μm in thickness. Resist thickness

and thickness uniformity are critical parameters in developing a good photolithography process.

Softbake

After spin coating the film contains 1 to 3 % of residual solvent and may contain built-in stresses caused by the shear forces during the spin process. Residual solvents in the film will effect the quality of the image obtained after the develop cycle. Stresses in the film lead to loss of adhesion. The wafer undergoes a softbake or prebake typically at 100-120°C for 1-2 minutes on a hot plate to drive off most of the solvent in the resist and anneal out any stress in the film. Softbake ensures that the resist film has uniform properties across the wafer. After a successful softbake, the resist film is very sensitive to light of specific wavelengths.

Exposure

To transfer a mask image to a surface of a resist-coated wafer, the radiation is shone through a transparent mask plate. For positive resist, the exposure is successful if the solubility in the exposed areas is high as compared with non-illuminated areas. The unexposed areas remain unaffected in solubility. The quality of the image depends on the tool, time, the radiation source, energy density and uniformity, and dose rate.

The exposure system consists of an UV lamp with or without lenses between the mask and the wafer. There are two main exposure systems: projection printing and contact printing. For projection printing, the mask is distant from the wafer, and lenses are used to focus the mask image onto the wafer. This method can get better resolution and minimize defect problems. For contact printing, the mask placed in physical contact with the wafer and the diffraction effects are minimized. The mask is pressed against the resist-coated wafer during UV exposure. Pressures ranging from 0.05 to 0.3 atm are used to push the mask into more intimate contact with the wafer. The primary advantage of contact printing is that small features can be made using comparatively inexpensive equipment.

The most common types of optical sources for photolithography are the high pressure arc lamps and mercury vapor lamps. Wavelengths of the light source used for exposure of

the resist coated wafer range from 150-300 nm to 350-500 nm. The resists are sensitive to light of 300-500 nm in wavelength, a range that includes visible violet and blue light. Therefore, resist process occurs under 'yellow light' conditions where wavelengths below 500 nm are filtered.

Development

The developing process has the greatest influence on the quality of the image. The resist-coating wafer with the exposed pattern is placed in developer solution for a fixed time. The developing process depends on the concentration solution and temperature. The developing temperature must be controlled to better than ±1°C. The wafer is washed with a solvent that preferentially removes the resist areas of higher solubility. Then the wafer is rinsed to stop development. Depending on the type of resist, the washed-away areas may be either the illuminated or shadowed regions of the coating. If exposure increases resist solubility, resist is washed away in the areas corresponding to the transparent zones of mask. The resist image is identical to the opaque image on the mask.

Hardbake

The last step in photolithography is hardbake or postbake. The wafer undergoes a hardbake typically at 120°C for 20 minutes. It is used to improve adhesion and harden the resist against further processing such as ion implantation and plasma etching. It is done at a higher temperature and longer time than softbake. However, resist is a polymer that softens and flows when heated. The hardbake temperature must be less than the flow point of the resist.

3.2.3 Etching

Materials are usually either removed or added during a process in MEMS fabrication. One of the most important subtractive processes is etching, which can be described as pattern transfer by selective, chemical or physical removal of a material from a substrate and its resident thin films. Etch process, like development, removes a film or layer from

the substrate in those areas not covered with protective layer called etch mask, such as photoresist, metal, or oxide layer. Different etchants need different etch masks. Table 3.1 gives some example silicon etchants.

Table 3.1 Comparison of example silicon etchants [40]

	HNA ($HF+HNO_3$ +Acetic Acid)	Alkali-OH	EDP (ethylene diamine pyrochat-echol	TMAH (tetramethyl-ammonium hydroxide)	XeF_2	SF_6 plasma	DRIE (Deep Reactive Ion etch)
Etch type	wet	wet	wet	wet	dry	dry	dry
Anisotropic	no	yes	yes	yes	no	varies	yes
Available	common	common	moderate	moderate	limited	common	limited
Si etch rate	1 to 3	1 to 2	1 to 30	≈1	1 to 3	≈1	>1
Si roughness	low	low	low	variable	high	variable	low
Nitride etch	low	low	low	1 to 10 nm/min	?	low	low
Oxide etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	≈1 nm/min	low	low	low
Al selective	no	no	no	yes	yes	yes	yes
Au selective	likely	yes	yes	yes	yes	yes	yes
P++ etch stop	no	yes	yes	yes	no	no	no
Electrochemical stop?	?	yes	yes	yes	no	no	no
CMOS compatible	no	no	yes	yes	yes	yes	yes
Cost	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate?	high	high

(The data in the table may vary by different sources)

There are two types of etching: wet and dry. Wet etching is a purely chemical process that can have serious drawbacks: poor process control and etch rate, and excessive particle contamination. However, wet etching can be highly selective and often does not damage the substrate. Dry etching is the removal or etching of solid material in the gas phase, physically by ion bombardment, chemically by a chemical reaction with a reactive species at the surface, or by both physical and chemical mechanisms. Dry etch rates are less accurate.

The two most important aspects of etching processes are selectivity and anisotropy. The selectivity of an etchant refers to how selective it is in etching one material over another. For example, buffered oxide etch (BOE, HF), a wet etchant, is extremely

selective between silicon and oxide; it will etch hundreds of microns of oxide before it etches one micron of silicon. The other important characteristic of etchants is the anisotropy. There are two main etch processes: isotropic and anisotropic. A completely isotropic etchant etches in all directions at the same rate, whereas completely anisotropic etchant will etch in one direction. Anisotropic etching etches at different rates in different directions of a crystal.

3.2.4 Stripping

This step involves the stripping of the resist and sacrificial layers. Stripping the resist always uses an acetone soak before the next process. To further remove any residual resist, a sample is sometimes treated in low-pressure oxygen plasma and may be accomplished by either a liquid or an oxidizing plasma process. This is followed by an inspection to make sure that the unwanted metal and resist have been stripped off completely. To remove a sacrificial layer, such as SiO_2, KOH etch is always used. Care must be taken not to alter the underlying thin film or wafer surface. It is also very important to keep the process free from any contamination that may adversely affect subsequent lithographic steps.

3.2.5 Inspection & Testing

Inspection and testing are ideally done after every process in photolithography before sending the wafers for the next process. The purpose of the inspection is to avoid three classes of problems: deviations in the pattern dimensions, surface problems, and resist problems, such as improper cleaning or leaving contaminants on the wafer surface, improper resist application, problems with resist adhesion, improper exposure or developing process, and unwanted oxide formation on the wafer surface before the next step. This method of inspection and testing after every step, rather than waiting until the final development step to inspect the wafers, saves time and money in case the wafers have to be processed again. These inspections can either be done by using the naked eye

or using a microscope. For example, after spin coating the film, variations in the resist film thickness are readily seen using the bare eye. Resist areas of different thickness are of different colours. A perfect spin coating results in a resist layer without colored patterns. Once a process has been rejected and a reason established for it, the process must be stopped in order to overcome problems before the next step is processed.

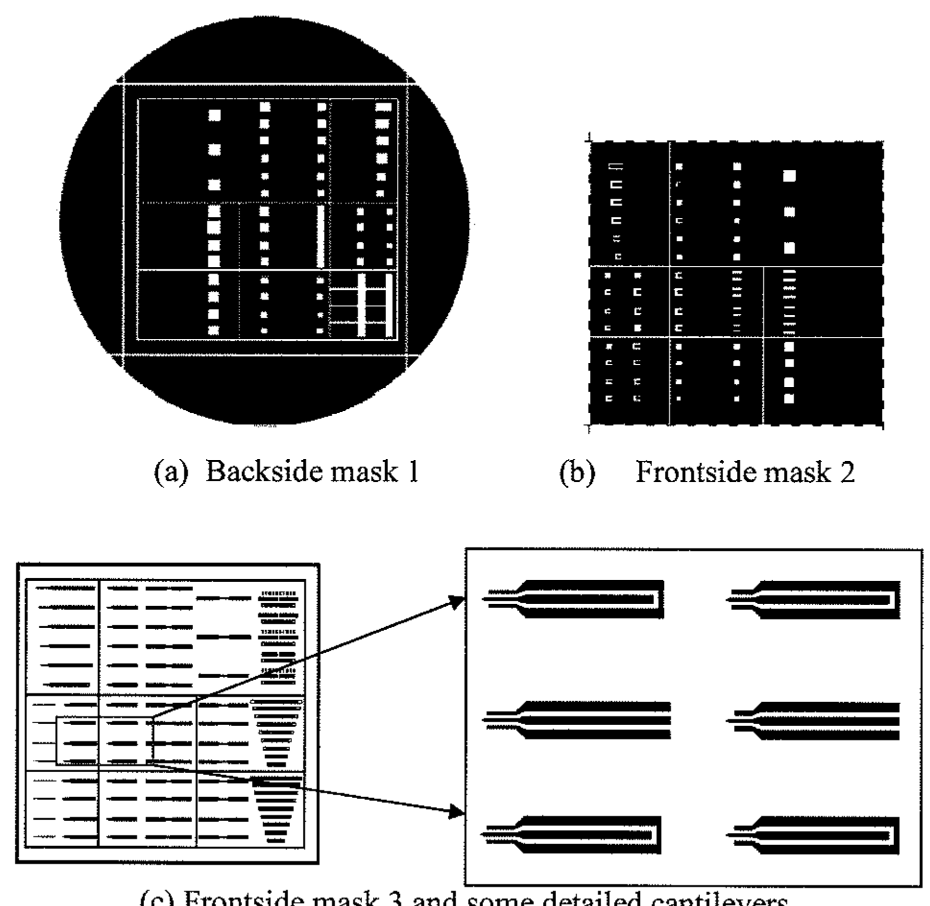
3.3 Other issues in CPW cantilever fabrication

3.3.1 Mask design

The first step of MEMS fabrication requires the design of lithographic masks. A mask must have a high optical transparency at the exposure wavelength, low coefficient of thermal expansion, and a flat, highly polished surface that reduces light scattering. The masks are then patterned by another lithographic process. Masks are usually fabricated on glass or mylar. On one surface is a patterned opaque layer. In most masks the opaque layer is chromium that can block the UV light when exposed. Any unwanted chrome can be removed by laser ablation.

In our work we drew the mask patterns using Adobe Illustrator 10.0 and then sent them off to a commercial photo/print shop to obtain the masks on transparent mylar sheet. Since the printer being used is 3600 dots-per-inch (dpi), the resolution is about 7.05 μm/dot. The reasonable resolution for a mask needs 3 dots. In addition, the ink spreads when it contacts the glass surface and errors may be caused in lithography and developing. The 28 μm and larger size prints are of very good quality. The dimensions for our CPW cantilever are set to larger than 28 μm as shown in Figure 3.2 in order to ensure good quality.

The designed masks for CPW cantilevers are shown in Figure 3.3. The image dimensions on the masks depend on the dimensions of the designed CPW cantilevers. A mask contains the pattern that can be transferred to a wafer. The masks may be the same size as the final image on the wafer or the image may be reduced during the exposure.



(a) Backside mask 1 (b) Frontside mask 2

(c) Frontside mask 3 and some detailed cantilevers

Figure 3.4 Lithographic contact masks (glass).

The pattern on the frontside must be aligned with the pattern on the backside of a wafer. The frontside masks should be flipped horizontally to align the backside masks. Aligning masks to a wafer is very important for MEMS fabrication to transfer the designed image from the contact masks to photoresist. It is very difficult and time-consuming, especially if many masks are used for a wafer.

A mask is placed above a wafer and then manually aligned to the wafer. The latter mask alignment for patterning images is more difficult than standard lithographic processing. The etch for cavity formation starts from the backside of the wafer, so the openings in the silicon oxide on Si wafer must be oriented properly relative to a CPW cantilever defined on the frontside of the wafer. If not, the CPW cantilever will not be

positioned at the locations of the cavity on the wafer backside, and may not even be on the membrane.

3.3.2 Deposition films

Thin films are always used as conductor, insulator, etch mask, diffusion mask, and sacrificial layers on the wafer surface. To deposit films for surface micromachining, many techniques are used: spin coating, evaporation, sputtering, chemical vapor deposition, and epitaxy. The thermal evaporation is selected due to its simple and inexpensive deposition equipment.

Thermal evaporation is a method to deposit high quality thin films of metals and other materials onto a wafer. The wafer is loaded into a high-vacuum chamber that is commonly pumped with a diffusion pump.

To obtain the best uniformity, the evaporator is usually operated at low rates, although operation at these rates requires high vacuums to avoid contamination of the film. The important parameters to control during evaporation are the deposition rate and film thickness. Both are measured using a quartz crystal rate monitor. The rate of material deposition is controlled by varying the charge temperature. The reasonable deposition rates are achieved with vapour pressure of at least 10 mtorr.

However, residual stresses are caused by the difference between the thermal expansion coefficients of the deposited film and substrate or other films. Intrinsic stresses usually result from the nonequilibrium nature of the thin film deposition process and deposition parameters. Thus, the residual stress must be carefully considered during MEMS CPW cantilever fabrication.

3.3.3 Release cantilever

Anisotropic etchant, such as KOH, etches silicon at different rates depending on the crystalline direction. The etch ratios for these two directions, [100] and [111], can be as

high as 400:1. The (111) planes are oriented at 54.7° relative to the (100) plane. An anisotropic KOH etches the crystalline structure of the [100] wafer and is used in our process to form the cavity and V-grooves. The walls of the cavity and V-groove slope at an angle of 54.7° from the surface plane.

The cavity and V-groove are fabricated to release a cantilever beam and to split off a piece of Si wafer, respectively. The difference is that they expose different SiO_2 openings in etchant resulting in different etch depths. For a small opening, the etch is terminated at an "etch stop" due to reaching the intersection of the (111) planes and then an inverted pyramid V-groove is formed. The depth of the V-grooves is designed to be half the thickness of the wafer and the Si wafer is easily cleaved. If the etch is terminated before the etch stop due to reaching the intersection of the (111) planes, then a truncated pyramidal cavity is formed. The remained thickness of the cavity (membrane) and V-groove must be strong enough to withstand successive photolithography steps on the Si wafer. Since KOH deep etching was used to fabricate the V-grooves and cavity below the CPW cantilever, the resultant profile was trapezoidal and the slope is 54.7° in Figure 3.2.

The phenomena of crystal cleavage and anisotropic etching stopping on certain crystal planes are commonly thought to result from the plane with the least surface density of atoms and surfaces with the highest bond density [41].

3.4 MEMS CPW cantilever fabrication

3.4.1 MEMS CPW cantilever fabrication parameters

The process parameters of MEMS CPW cantilever fabrication are determined empirically in conjunction with the above review of MEM fabrication processes. A recommended process is shown in Table 3.2. The process is for a Si wafer covered both sides with 1.5 μm SiO_2 insulating layers to fabricate MEMS CPW cantilevers.

Table 3.2 Recommended process steps in MEMS CPW cantilever fabrication

Process	Duration	Process temperature	Note
Oxidation	6 hours	1100 ° C	1.5 μm on both sides of Si wafer
Spinning coating resist	3000 rpm for 35 sec	Room temperature	2 μm of HPR 506
Softbake	1 min	110 °C	Quick cold for 5 sec
Exposure	1.5 min	Room temperature	UV light
Development	45 sec	Room temperature	HPRD 419
Hardbake	20 min	120 °C	Remove water
Stripping oxide	40 min for 1.5 μm	Room temperature	10:1 BOE (HF)
Etch silicon	4 hours	80 °C	KOH etch (≈1.1μm/min)
Stripping photoresist	10 sec	Room temperature	Acetone
Deposit Al film	Variable	Room temperature	0.21 μm (≈1.5 nm/s)
Deposit Cu film	Variable	Room temperature	0.92 μm (≈1.4 nm/s)
Stripping Cu	1-2 min	Room temperature	Chrome etchant
Stripping Al	1 min	Room temperature	10:1 BOE (HF)
XeF_2 gas etchant	Variable	Room temperature	In vacuum

3.4.2 Detailed MEMS fabrication steps of CPW cantilevers

The MEMS CPW cantilevers are in-house fabricated using 2-inch diameter, 325 μm thick, 1000 Ω-cm resistivity, and n-type Si wafer with (100) crystal orientation and both wafer sides covered with 1.5 μm SiO_2 insulating layers. The main steps in MEMS CPW cantilever fabrication are given as: BOE etch to remove unwanted SiO_2 regions and KOH deep etch to form a preliminary cavity (the remaining Si wafer thickness is approximately 40 μm) and V-grooves on the backside of the Si wafer; BOE etch to remove unwanted SiO_2 regions above the cavity on the frontside of the Si wafer; deposition and patterning of Al/Cu layers to form the CPW lines on the frontside; XeF_2 etch to remove the remaining 40 μm Si wafer at the cavity and release the CPW cantilever structure. The detailed fabrication steps for MEMS CPW cantilevers are shown schematically in Figure 3.5 and given as follows:

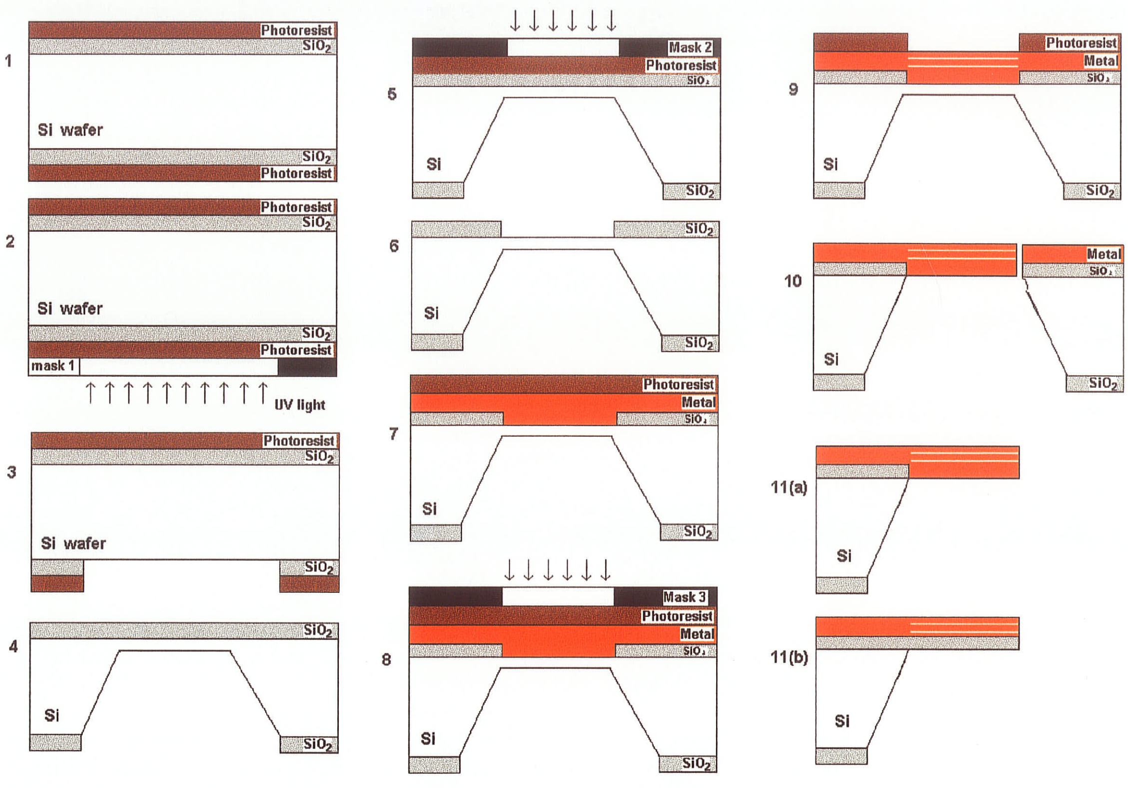


Figure 3.5 Fabrication steps for CPW cantilevers: 1. Deposit photoresist on both sides of Si wafer covered with SiO_2 layers; 2. Use mask 1 to define the cavity and V-groove on the backside, expose and develop photoresist; 3. BOE etch exposed SiO_2 regions; 4. Backside KOH deep etch; 5. Use mask 2 to define cantilever beam regions and remove the unwanted SiO_2 regions on the frontside, expose and develop photoresist; 6. BOE etch SiO_2 at unwanted regions; 7. Deposit Al/Cu layers and then photoresist on SiO_2 layer; 8. Use mask 3 to apply and pattern the CPW transmission lines on the frontside; 9. Use chrome etchant etch Cu, and BOE etch Al and SiO_2 layers at unwanted regions; 10. Remove photoresist and use XeF_2 gas backside etch the remained Si wafer at membrane to release CPW cantilevers; 11. CPW cantilevers mounted by Si holder (a) CPW cantilever suspended in air; (b) CPW cantilever suspended by the thin SiO_2 layer.

1. Initialization and oxidation: we bought the double side polished, 2 inch diameter, 325 μm thick, 1000 Ω-cm resistivity, and n-type Si wafers with (100) crystal orientation from International Wafer Service, Inc. (CA 94028, USA, www.siwafer.com). Each Si wafer is $7.5. The wafers were then sent to the NanoFab lab of the University of

Alberta, Canada to make insulator SiO_2 layers on the both sides of the Si wafers. The wet oxidation is usually done at 1100°C for 6 hours in a quartz furnace to form 1.5 μm oxidation on the both sides of a Si wafer.

For shallow etch, we usually use photoresist as a mask. For deep etch, however, the photoresist is useless and we usually use SiO_2 or Si_3N_4 layer as a mask. The SiO_2 insulating layers on both sides of a Si wafer can protect the unwanted etch regions as an etch mask and can also avoid a dc leakage current between CPW center strip conductor and the ground strip conductors. Both sides of the wafer are deposited with 2 μm photoresist (HPR506) using a spin coating process at 3000 rpm for 35 seconds. The wafer is then soft baked approximately 1 minute at 110 °C on a hot plate and the wafer is placed on an aluminium slab to cool for 5 seconds.

2. Cavity and V-groove: use mask 1 to contact the photoresist on the backside of the Si wafer using contact printing and define the openings of the cavity and V-grooves. Use UV light exposure about 90 seconds, and then develop the exposed wafer in HPRD419 approximately 45 seconds. The image of mask 1 is imprinted on the photoresist of the wafer surface. Then the wafer undergoes hardbake for 20 minutes at 120 °C to remove the attached water.
3. SiO_2 openings: use 10:1 BOE to overetch the exposed SiO_2 layer without protection of a photoresist layer for about 40 minutes. This process does not affect the Si wafer and unexposed SiO_2 regions.
4. Backside deep etch: use KOH anisotropic etch on the entire 320 μm thick Si wafer to form the cavity and V-grooves as shown in Figure 3.6. The difference between cavity and V-groove is that they expose different sized openings in an etchant resulting in different etch depths. The SiO_2 openings of the cavity and V-groove are about 950 and 280 μm as shown in Figure 3.7, respectively. After 4 hours in a 80 °C KOH etch, the remaining Si wafer becomes about 40 μm thickness on the exposed SiO_2 region of the cavity. The etch rate of KOH for silicon is approximately 1.1 μm/min. The SiO_2 layers on both sides of the Si wafer become 0.36 μm because the etch rate of KOH for oxide is about 0.25-0.3 μm/hour. For the small opening, the etch becomes very slow and usually stops at the intersection of the (111) planes to form the V-grooves.

The remained thickness of the cavity and V-grooves must be strong enough to withstand successive photolithography steps on the frontside of Si wafer.

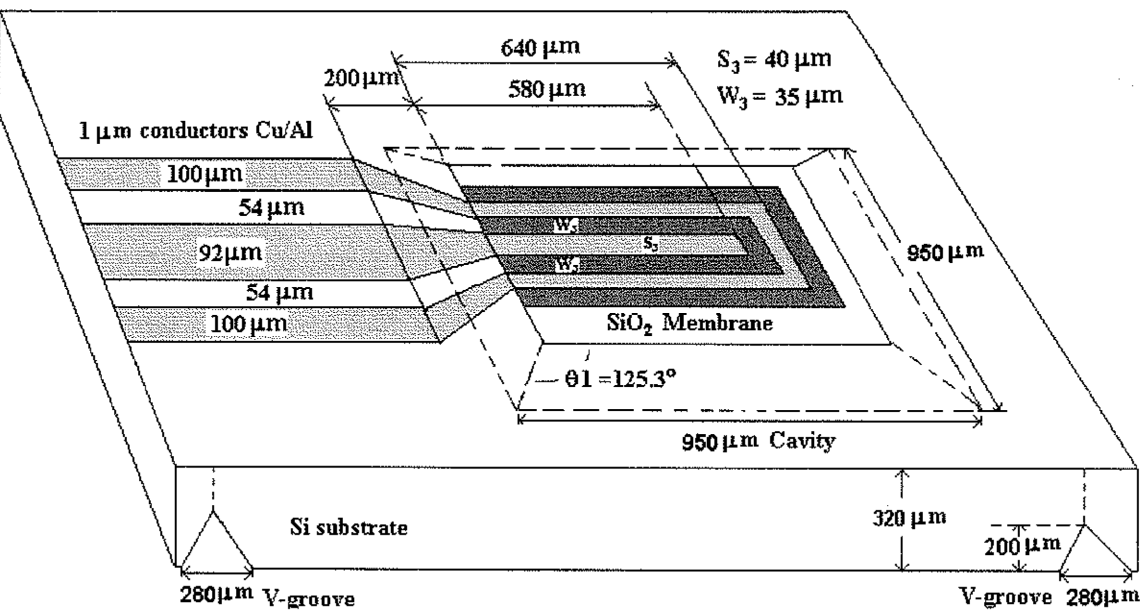


Figure 3.6 Dimensions of a CPW cantilever on a SiO_2 membrane above a cavity.

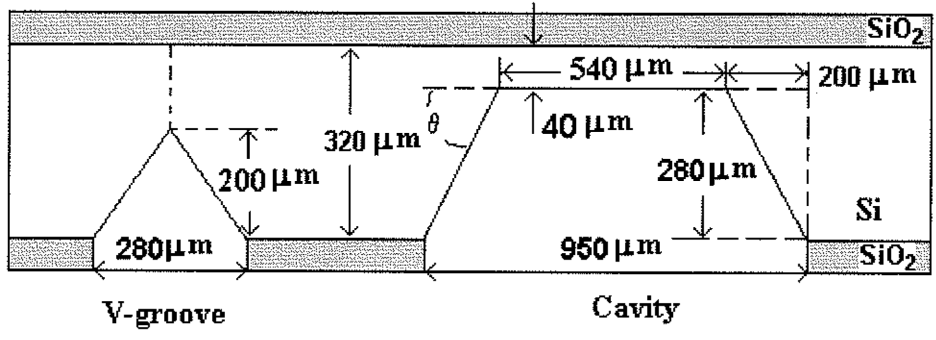


Figure 3.7 Designed dimensions of a cavity and a V-groove after KOH deep etch.

5. Use contact mask 2 to pattern the unwanted SiO_2 regions on the frontside of the Si wafer: deposit photoresist on the frontside of Si wafer over the cavity regions. The backside of the wafer is covered with wafer tape to avoid etching by the following BOE etch. Use contact mask 2 lithography, expose to UV light, and then develop photoresist.

6. BOE overetching removes the SiO_2 layer on unwanted SiO_2 regions. All photoresist is removed using acetone as above before the next step. Every time the wafer undergoes a softbake after deposited photoresist and hardbake after development.
7. Deposition metals: deposit 0.21 μm Al layer and then 0.92 μm Cu layer, which are measured by a quartz crystal monitor, on the remained SiO_2 layer of the frontside Si wafer by evaporation. The thin Al layer is deposited prior to the Cu layer deposition to enhance adhesion between Cu and silicon oxide. Then Deposit a photoresist layer on the Si wafer covered with Al/Cu layers.
8. Use contact mask 3 to pattern the CPW transmission lines on metal layers of the frontside Si wafer. The dimensions of one CPW cantilever are given in Figure 3.6. Pattern, expose and develop photoresist.
9. Metal etch: metal layers are patterned and removed in the unwanted areas to obtain the CPW transmission lines on the frontside of the Si wafer. Between the Si wafer and metal layers is the remained SiO_2 layer after KOH deep etch. The regions of CPW lines are protected by a covered photoresist layer. Use chrome etchant to remove the Cu layer and use BOE etchant to remove both the Al layer and the SiO_2 layer at uncovered photoresist regions. Then remove all photoresist. Now on the frontside, above cavities, the membranes are either the remaining Si wafer or the remaining SiO_2 layer on remaining Si wafer after KOH deep etch. The SiO_2 layers on Si holder are etched away at the slot regions of the CPW line on the Si holder as shown in Figure 3.8.

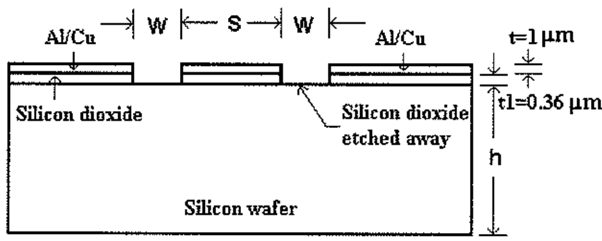


Figure 3.8 Cross sectional view of the CPW line on Si holder.

10. Release the CPW cantilever: 5 seconds BOE etch is used to remove any native oxide on the silicon wafer. Then an isotropic XeF_2 gas etch is used to remove the remaining Si wafer below the cantilever in order to release the conductive CPW cantilever with

or without a thin SiO_2 membrane. The XeF_2 etching is closely monitored using a microscope until the cantilevers are released.

11. CPW cantilever: Figure 3.9 shows examples of the fabricated CPW cantilevers mounted on a Si holder. The SiO_2 insulating layer on the CPW slot regions has been etched away. Some fabricated CPW cantilevers are suspended in air and others are suspended by a SiO_2 membrane.

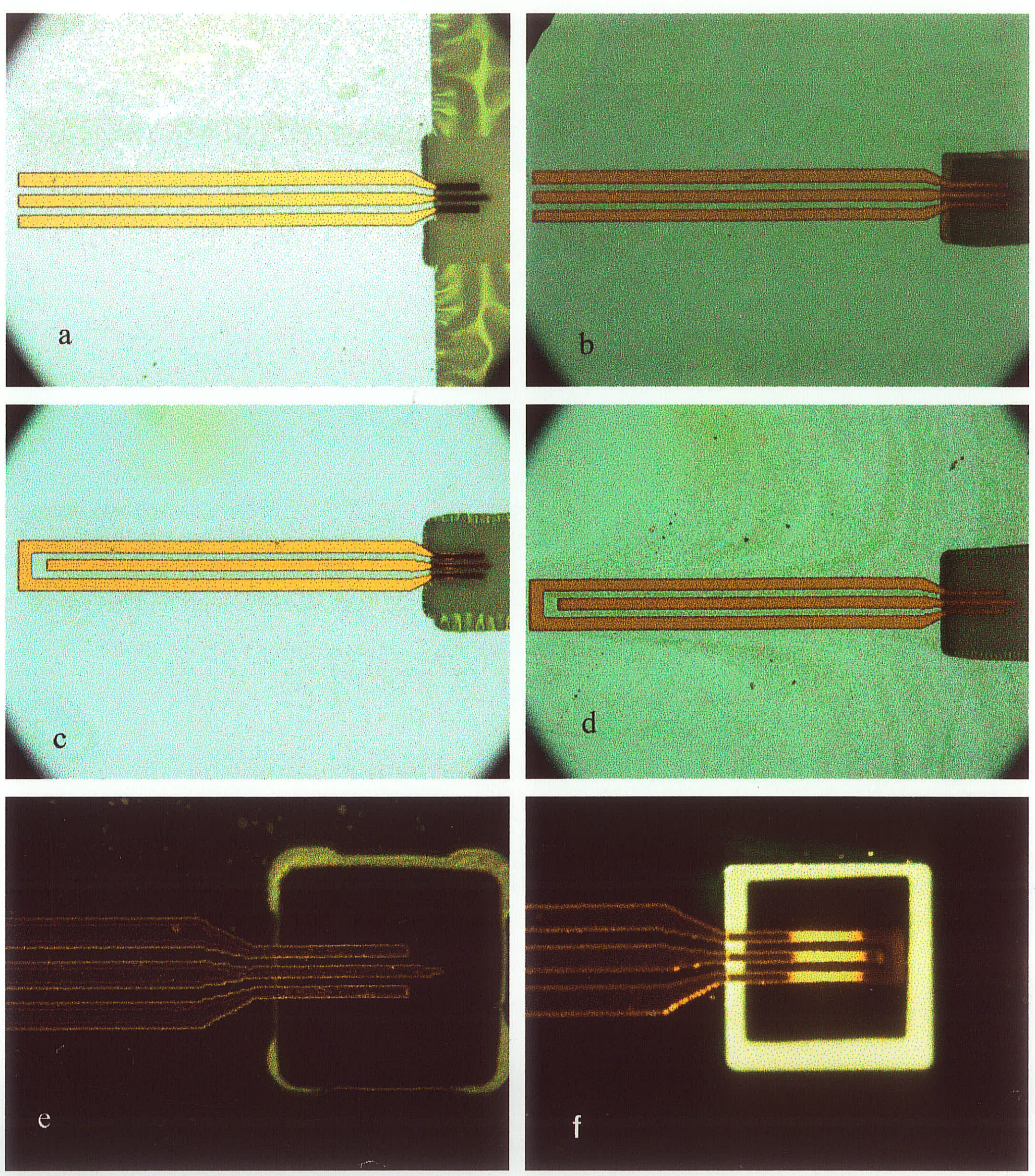


Figure 3.9 Examples of fabricated CPW cantilevers. a) Cantilever on SiO_2 membrane; b) Cantilever in air; c) Ground connected cantilever on SiO_2 membrane; d) Ground connected cantilever in air; e) Cantilever in air; f) Ground connected cantilever in air).

Chapter 4 Characteristics of CPW cantilevers and discussion

In this chapter, mechanical and electrical properties of the stressed CPW cantilevers are measured. S-parameters calculated using an equivalent circuit model and HFSS are compared with the measured S-parameters.

4.1 Mechanical properties of stressed MEMS CPW cantilevers

4.1.1 Stress

MEMS structures make extensive use of thin films, and the stress and strain of the films are often very important to the operation of MEMS devices and systems. A film under mechanical stress will deform. The stress in freestanding films will be zero, and stress gradients in thin films can be relaxed by the curvature of freestanding structures. A freestanding film with a stress gradient will curve towards the side that is in tensile stress. The stressed CPW cantilever makes use of these residual stresses. Figure 4.1 shows the fabricated MEMS stressed CPW cantilevers.

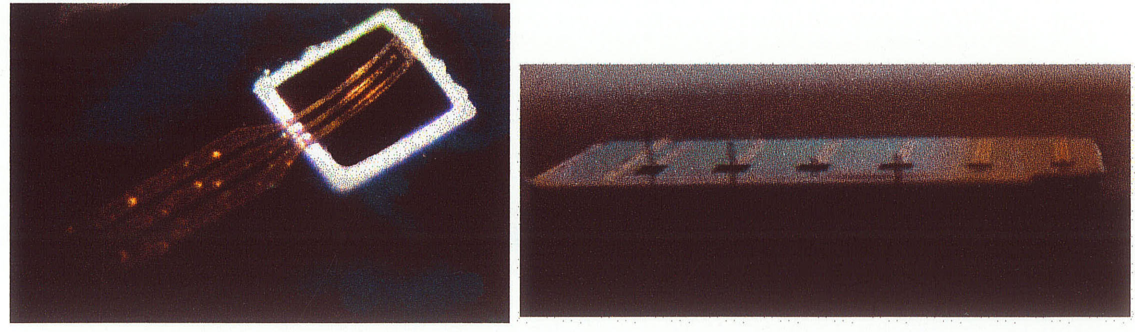


Figure 4.1 (a) A stressed MEMS CPW cantilever; (b) Arrays of stressed MEMS CPW cantilevers on a Si wafer.

Stress gradients result from variations of film composition caused by all the different effects that can cause intrinsic stress, i.e. chemistry, doping, structure, and surface states.

A typical situation is depicted in Figure 4.2. Assume a freestanding metal film that has the thickness t and width w. If it is bent by applying force F at the ends as shown in Figure 4.2 (a), a stress gradient $\Delta\sigma/t$ can be grown in the film, creating a restoring moment which just balances the bending moment of F. Similarly, if metal film is deposited on Si substrate with an intrinsic stress gradient as shown in Figure 4.2 (b), the gradient must be maintained by a sufficient bonding force F to the Si substrate. If a bonded cantilever beam is undercut-etched to release it for a length L as shown in Figure 4.2 (c), a portion of film curves up until the stress is completely relaxed.

Before the cantilever beam is released, there is both an average stress and a stress gradient in the thin film. The stress will go to zero when it is released, but the stress gradient remains if the film is constrained such that it is still flat. After release, the average stress is zero, but the stress gradient remains. This leads to bending of the freestanding structure. This will form a stressed CPW cantilever. The resulting curvature radius r may be decided by Hooke's law for biaxial stress.

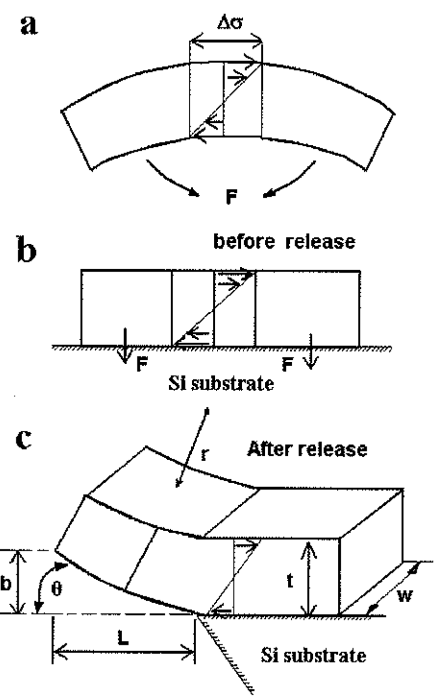


Figure 4.2 Stress gradients causing a bent cantilever [60].

The biaxial stress is given by Hook's law [40]:

$$\sigma_{x,y} = [E/(1-\nu)]\varepsilon_{x,y} \quad \textbf{(4.1)}$$

where the stress $\sigma_{x,y}$ and strain $\varepsilon_{x,y}$ are given the subscripts in which the first element refers to the surface and the second refers to the direction. E is the Young's modulus, and ν is Poisson's ratio. $E/(1-\nu)$ is the biaxial modulus. The change in strain from top to bottom across t is related to r by

$$\Delta\varepsilon_{x,y} = t/r \quad \textbf{(4.2)}$$

For moderate angles of lift ($\theta<50°$), the bending height can be approximated by

$$b \approx L^2/2r \quad \textbf{(4.3)}$$

Combining above three equations, stress can be given by mechanical parameters as

$$\Delta\sigma = 2t[E/(1-\nu)]b/L^2 \quad \textbf{(4.4)}$$

For stressed MEMS cantilevers, the conductive transmission lines are fabricated by Al(0.21 μm)/Cu(0.92 μm) layers. For approximate calculation, the stress is assumed to be caused by only the Cu layer. Therefore, E = 130 GPa (assuming bulk value), ν = 0.32, t = 0.92 μm. Table 4.1 shows measured bending height b and the calculated stress resulting in bent cantilevers. The cantilever bending height was measured with a microscope with a calibrated z-movement. A variation of stress is observed in Table 4.1, this possibly due to variation of E over the sample surface.

For the fabricated stressed CPW cantilevers, it is also noted that the springs are surprisingly tough, and have survived during rinsing off oxide and dust on the surface.

Table 4.1 Calculated stresses in cantilevers

Samples		Measured Bending height (μm)	Dimensions (μm)	Stress (GPa)
Single cantilever		60	$L = 360$, $w = 40$, $t = 0.92$	0.161
CPW cantilever (No.1)	Center beam	140	$L = 520$, $w = 40$, $t = 0.92$	0.180
	Side beams	140	$L = 600$, $w = 70$, $t = 0.92$	0.135
CPW cantilever (No.2)	Center beam	130	$L = 575$, $w = 40$, $t = 0.92$	0.137
	Side beams	130	$L = 643$, $w = 80$, $t = 0.92$	0.109

4.1.2 Resonant frequency

The resonant frequency of a cantilever was measured by the system shown in Figure 4.3 (a). Its operation principle is also shown in Figure 4.3 (b). A laser beam is focused on the end of a stressed cantilever probe and reflected back to a photodetector. The photodetector detects the variable position of the laser beam reflected from the cantilever through a splitter. The natural vibration of the cantilever due to thermal excitation is used to determine the cantilever resonance frequency. Using this laser beam deflection system,

the resonant frequency of three stressed cantilevers suspended in air is measured as shown in Figure 4.4.

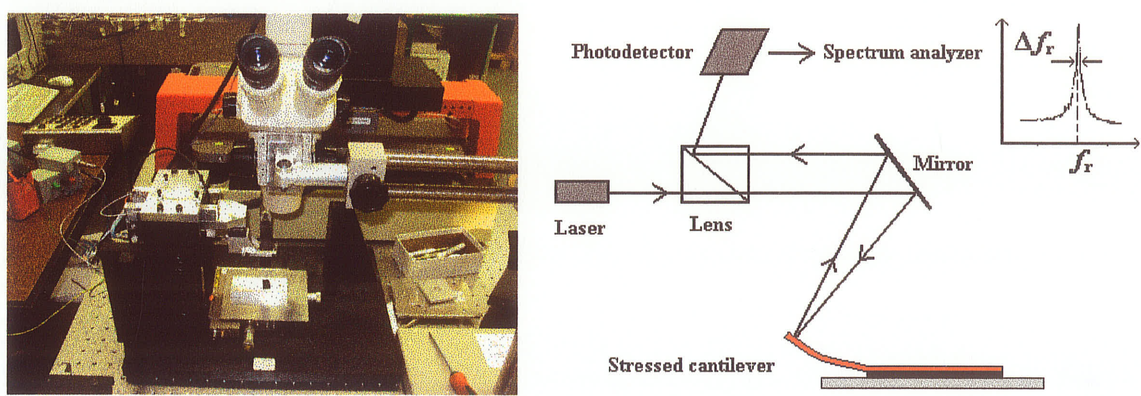


Figure 4.3 (a) Resonant frequency measurement set up; (b) Laser beam bounce deflection system for measuring mechanical properties.

The spring constant k of a rectangular cantilever structure fixed on one end is calculated using

$$k = \frac{Et^3 w}{4L^3} \tag{4.5}$$

where L, w, t are the length, width, and thickness of a cantilever, respectively. E is Young's modulus. For Cu cantilever, E = 130 GPa and ρ = 8.89 g/cm^3 is given from Table 2.5.

The center beam or side beam resonance frequency of the CPW cantilever with free ends is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{0.24 m_L}} \tag{4.6}$$

For the ground connected CPW cantilever as shown in Figure 4.5 (a) and its equivalent model in Figure 4.5 (b) has length L that does not change but its width w and mass m_L are equal to the sum of the two separated beams, respectively. The side beam resonance frequency of a ground connected CPW cantilever, with beam length L and mass m_L with an end mass m, can be computed using an equivalent mass $m + 0.24\ m_L$ as

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m + 0.24m_L}} \tag{4.7}$$

where $m_L = m_1 + m_2$, $m_L = \rho w L t$, $w = w_1 + w_2$, and the thickness of cantilever is t and ρ is the mass density of the cantilever material. The 2nd resonant frequency is theoretically calculated to be $f_{r2} = 6.26 f_{r1}$ [61].

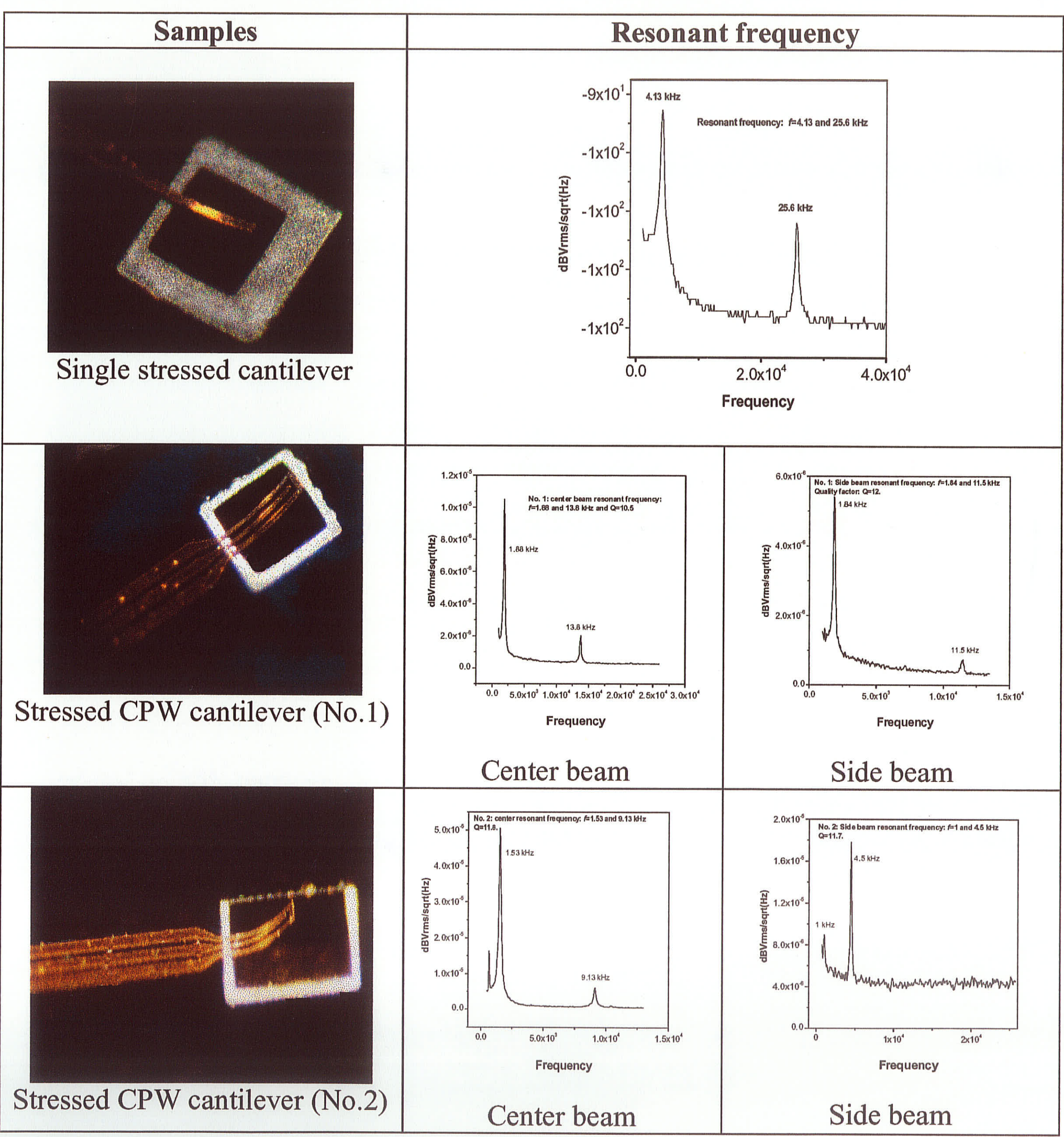


Figure 4.4 Resonant frequency of cantilevers.

The quality factor Q is defined as resonant frequency divided by its resonant width $Q = \frac{f_r}{\Delta f_r}$ of the 3dB bandwidth from resonant frequency or bandwidth Δf_r at 0.707 of the maximum amplitude. Table 4.2 gives the measured and computed mechanical parameters.

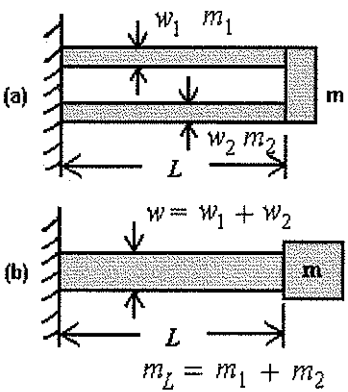


Figure 4.5 (a) Ground-connected side beams; (b) equivalent beam.

Table 4.2 Measured and calculated mechanical parameters of stressed cantilevers

Sample		Bending height (μm)	Dimensions (μm)	Measured results	Computed results
Single stressed cantilever		60	$L = 360$ $w = 40$ $t = 0.92$	$f_{r1} = 4.13$ kHz $f_{r2} = 25.6$ kHz	$f_{r1} = 4.125$ kHz $f_{r2} = 25.8$ kHz $k = 0.019340$ $Q = 46$
Stressed CPW cantilever (No.1)	Side beams	140	$L = 600$ $w = 70$ $t = 0.92$	$f_{r1} = 1.84$ kHz $f_{r2} = 11.5$ kHz	$f_{r1} = 1.364$ kHz $f_{r2} = 8.539$ kHz $k = 0.00976$ $Q = 12$
	Center beam	140	$L = 520$ $w = 40$ $t = 0.92$	$f_{r1} = 1.88$ kHz $f_{r2} = 13.8$ kHz	$f_{r1} = 2.088$ kHz $f_{r2} = 13.1$ kHz $k = 0.005225$ $Q = 10.5$
Stressed CPW cantilever (No.2)	Side beams	130	$L = 643$ $w = 80$ $t = 0.92$	$f_{r1} = 1.0$ kHz $f_{r2} = 6.56$ kHz	$f_{r1} = 1.226$ kHz $f_{r2} = 7.687$ kHz $k = 0.00894$ $Q = 11.7$
	Center beam	130	$L = 575$ $w = 40$ $t = 0.92$	$f_{r1} = 1.53$ kHz $f_{r2} = 9.13$ kHz	$f_{r1} = 1.708$ kHz $f_{r2} = 10.69$ $k = 0.003865$ $Q = 7.6$

The measured resonance frequency of the center and side beams of the stressed CPW cantilever (No.2) in Figure 4.4 is about 1.53 and 1.0 kHz which is in reasonable agreement with the theoretical value of 1.71 and 1.226 kHz based on the measured dimensions of CPW cantilever in air, respectively. The reason for the small difference may be the effect of the Al layer is neglected in calculation.

4.2 Electrical properties of stressed MEMS CPW cantilevers

4.2.1 Computing the characteristic impedance and effective dielectric constant

The cross section of a CPW is shown in Figure 4.6 above a thin SiO_2 film between a silicon wafer and the conductors. The SiO_2 layer can block a dc leakage current flowing between the CPW center strip conductor and the ground strip conductors since the Si wafer is not a perfect insulator. The leakage current is not a concern in the case of passive devices such as couplers and filters. But it can be a serious problem when active devices are integrated. Since there is a thin SiO_2 layer between the Si wafer and CPW conductor lines, the effect of the SiO_2 layer should be considered during calculations of the CPW characteristic impedance and effective dielectric constant.

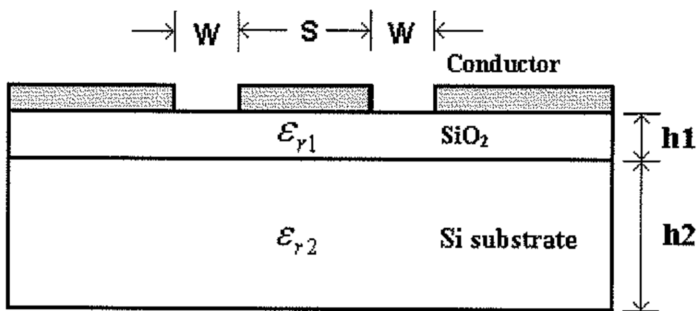


Figure 4.6 CPW transmission line on two-layer substrate.

The equations presented in section 2.3.1 assumed a zero thickness oxide and were used along with HFSS as the design equations for our CPW. However, to accurately compare measurements and theory, we will examine in more detail the effect of the oxide

layer. Figure 4.6 also gives the dimensions of CPW transmission line and the thickness and dielectric constants of the substrate layers where $h = h1+h2$.

The characteristic impedance Z_1 and effective dielectric constant ε_{reff} of the CPW are given as [19][62]

$$Z_1 = \frac{30\pi}{\sqrt{\varepsilon_{reff}}} \frac{K(k_0^{'})}{K(k_0)} \quad (4.8)$$

$$\varepsilon_{reff} = 1 + q_1(\varepsilon_{r1} - \varepsilon_{r2})/2 + q_2(\varepsilon_{r2} - 1)/2 \quad (4.9)$$

where the partial filling factors q_1 and q_2 are equal to

$$q_1 = \frac{K(k_1)K(k_0^{'})}{K(k_1^{'})K(k_0)} \quad (4.10)$$

$$q_2 = \frac{K(k_2)K(k_0^{'})}{K(k_2^{'})K(k_0)} \quad (4.11)$$

The modulus of the complete elliptic integrals $K(k_2)$, $K(k_1)$, and $K(k_0)$ are given as

$$k_2 = \frac{\sinh(\pi S/4h)}{\sinh\{[\pi(S+2W)]/4h\}} \quad (4.12)$$

$$k_1 = \frac{\sinh(\pi S/4h1)}{\sinh\{[\pi(S+2W)]/4h1\}} \quad (4.13)$$

and $$k_0 = \frac{S}{S+2W} \quad (4.14)$$

The complementary moduli is given by $k_i^{'} = \sqrt{1-k_i^2}$ (i=0, 1, 2).

If $h1$ tends to infinite, $k_2 = k_1 = k_0$ and $q_1 = q_2 = 1$, hence $\varepsilon_{reff} = (\varepsilon_{r1} + 1)/2$ which means that dielectric constant of an infinite thickness substrate is ε_{r1}.

If $h1$ tends to zero, $q_1 = 0$ and the above equation becomes

$$\varepsilon_{reff} = 1 + q_2(\varepsilon_{r2} - 1)/2 \quad (4.15)$$

If $h1$ tends to zero and $h2$ tends to infinite, $q_1 = 0$ and $q_1 = 1$, the ε_{reff} from above equation is given as

$$\varepsilon_{reff} = 1 + (\varepsilon_{r2} - 1)/2 \quad \textbf{(4.16)}$$

In our cantilevers, the thickness $h1$ of the SiO_2 insulating layer is approximately 0.36 μm, and the thickness $h2$ of Si wafer is approximately 325 μm. The approximate (no oxide) ε_{reff} is given as

$$\varepsilon_{reff} = 1 + (\varepsilon_{r2} - 1)/2 = 6.45$$

The ε_{eff} and Z_1 are calculated using equation (4.15) which includes oxide thickness effects and using the actual dimensions of the fabricated CPW lines on Si holder ($h1$ = 0.36 μm , $h2$ = 325 μm, w = 52 μm, and S = 96 μm) are given as

$$\varepsilon_{reff} = 6.36$$

$$Z_1 = \frac{30\pi}{\sqrt{\varepsilon_{reff}}} \frac{K(k_0')}{K(k_0)} = 48.92\ \Omega$$

Although the above calculated ε_{reff} and Z_1 using CPW dimensions are independent of the frequency, they are very useful for estimating the propagation parameters of the CPW line on Si holder based on an equivalent circuit model as described in the next section.

4.2.2 The measured and simulated S-parameters

Figure 4.7 shows an on-wafer scattering parameter measurement using an Anritsu (ME-7808A) vector network analyzer (VNA). S-parameters are measured after using an on-wafer short-open-load-thru (SOLT) calibration. Through a coaxial cable, the source drives the input of a conventional ground-signal-ground (GSG) microwave probe. This probe has a low loss and a characteristic impedance of 50 Ω.

The transmission coefficient is determined by connecting a second GSG microwave probe contacting the output of a CPW line on the silicon holder. The native oxide on the surface of the CPW conductor was removed immediately prior to the S-parameter measurements of the CPW cantilevers since the Cu can oxidize and cause poor probe contact. The electrical connection on-wafer from the GSG probe to the CPW line on Si holder is made by the means of pressure contact.

The following fabricated CPW cantilevers can be divided into three parts as described in chapter 2 as follows: part 1, a CPW line on Si holder; part 2: a transition on Si holder, a tapered CPW line between a CPW line on Si holder and a CPW cantilever in air; part 3: a CPW cantilever suspended in air. A CPW cantilever is mounted by a Si holder. Both dimensions of the CPW line on Si holder (part 1) and CPW cantilever in air (part 3) are different.

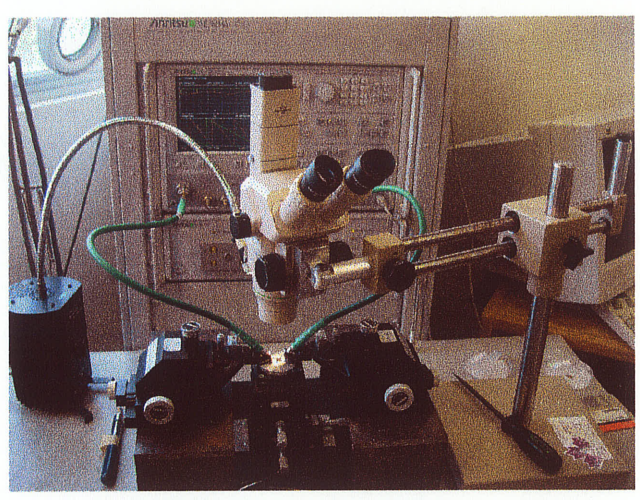


Figure 4.7 S-parameter measurement set up.

4.2.2.1 CPW line on Si holder with and without CPW cantilever

1) Measured S-parameters

A ground connected CPW cantilever on a thin SiO_2 membrane mounted by a CPW line on a Si holder is shown in Figure 4.8 (a). It consists of a 3200 μm long CPW transmission line (part 1) in conjunction with a transition (part 2) on a Si holder. Case A as shown in Figure 4.8 (a), includes the cantilever (part 3). In case B, Figure 4.8 (b), the cantilever (part 3) has been removed. The dimensions of the two cases are given in Table 4.3. Two-port S-parameters are measured with probes at the reference planes 1 and 2 as in Figure 4.8. The measured two-port S-parameters of the two cases are shown in Figure 4.9. Both return losses at port 1 and port 2 are non-reciprocal due to asymmetrical structures. The amplitude of return losses for the two cases is in the same range from 14 dB to 25 dB.

Since the measured return losses are better than 14 dB over the entire frequency range, they indicate that the fabricated CPW lines on Si holder are reasonably well matched.

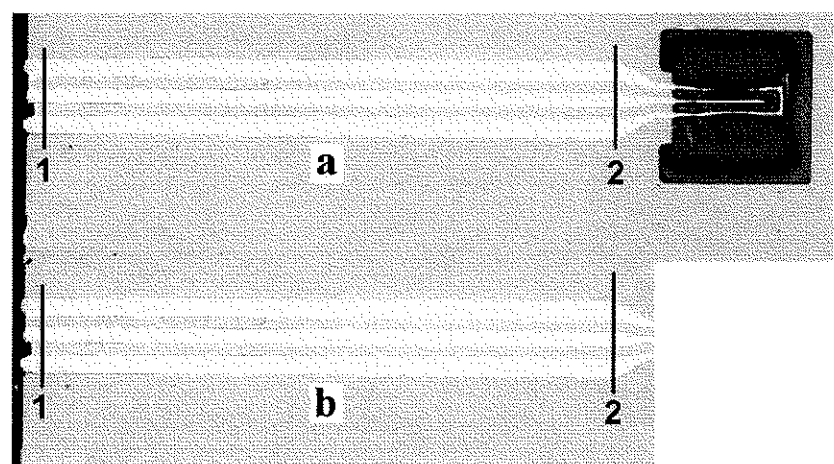


Figure 4.8 (a) Ground connected CPW cantilever on SiO_2 membrane; (b) CPW transmission line on Si holder.

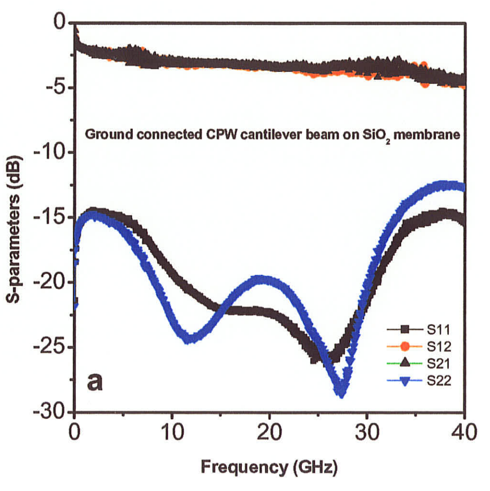
Table 4.3 Three part dimensions and dc resistance of fabricated CPW cantilevers

	a		b	
	Center beam	Side beams	Center beam	Side beams
Part 1: CPW line on Si holder	L = 3200 μm w = 97 μm	L = 3200 μm w = 97 μm	L = 3200 μm w = 97 μm	L = 3200 μm w = 97 μm
Part 2: transition on Si holder	200 μm		200 μm	
Part 3: CPW cantilever in air	L = 600 μm w = 35 μm	L = 635 μm w = 35 μm		
dc resistance	0.9 Ω		0.67 Ω	

(The thickness of copper and aluminum is about 0.92 and 0.21 μm, respectively)

The insertion losses of both cases are observed to increase slowly over the frequency range. For example, the insertion loss of the CPW line with cantilever as shown in Figure 4.9 (a) is about 2.9 dB and 3.5 dB at 10 and 20 GHz, respectively. Similarly, the insertion loss of the CPW transmission line without the CPW cantilever as shown in Figure 4.9 (b) is approximately 2.96 and 3.4 dB at 10 and 20 GHz, respectively. Comparing the

measured S-parameters of the two cases, it is observed that the insertion loss and return loss are almost insensitive to the existence of the CPW cantilever (part 3). It infers that the S-parameters of the part 1, CPW transmission line on Si holder mainly determine the S-parameters of entire CPW cantilever. It is reasonable that the losses of the CPW cantilever in air (part 3) are low due to its short line length and low dielectric constant. Therefore, the propagation properties of the stressed MEMS CPW cantilever are mainly determined from those of the CPW transmission line on Si holder (part 1). For detailed analyses of the insertion loss of the CPW line in Figure 4.9 (b), the measured magnitude and phase of S21 of the 3200 μm CPW transmission line on the Si holder shown in Figure 4.8 (b) are given in Figure 4.10.



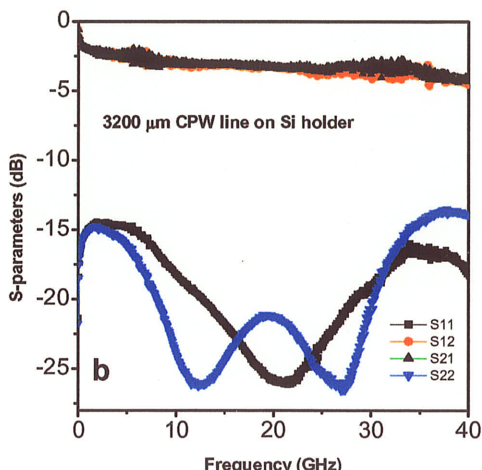


Figure 4.9 S-parameters (a) Ground connected CPW cantilever on SiO_2 membrane (part 3) mounted on a 3200 μm CPW transmission line on a Si holder (part 1); (b) A 3200 μm CPW transmission line (part 1).

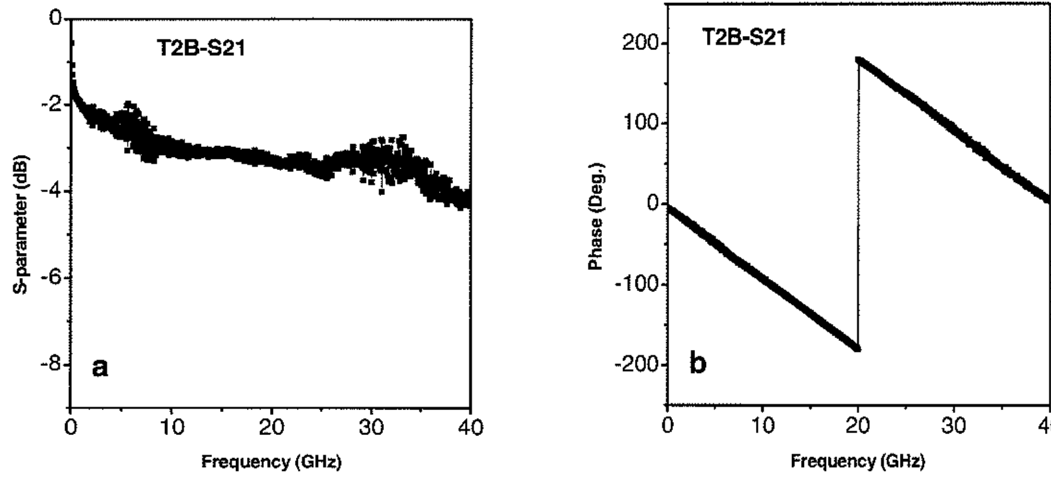


Figure 4.10 Magnitude and phase of S21 for the 3200 μm CPW transmission line on Si holder (Figure 4.8 (b), case B).

Using the phase shift θ (electrical length) of the measured S21 in Figure 4.10 (b), the effective dielectric constant ε_{reff} can be calculated. Note that the phase variation is fairly linear as a function of frequency. For example, the phase shift θ of 3200 μm CPW transmission line on Si holder changes 92.12 degree at 10 GHz, the phase constant β in radians per millimetre and ε_{reff} are initially estimated as follows:

$$\beta l = \theta(Deg.) = \frac{\theta}{180}\pi \quad (4.17)$$

$$\frac{2\pi}{\lambda_1} l = \frac{\theta}{180}\pi$$

$$\beta = \frac{\omega}{u} = \frac{2\pi f}{u_0}\sqrt{\varepsilon_{reff}} \quad (4.18)$$

$$\lambda_1 f = \frac{u_0}{\sqrt{\varepsilon_{reff}}} \quad (4.19)$$

$$\varepsilon_{reff} = \left(\frac{u_0}{\lambda_1 f}\right)^2 = \left(\frac{u_0\theta}{360lf}\right)^2 = \left(\frac{3\times10^8\times92.12}{360\times3200\times10^{-6}\times10\times10^9}\right)^2 = 5.76$$

where the speed of light is $u_0 = 3\times10^8\ m/s$ and the length of the CPW line on Si holder is $l = 3200\ \mu m$.

Using above equations, the effective dielectric constant and attenuation constant per millimeter of a CPW line on a Si holder (part 1) at frequency range 0.04-40 GHz are calculated as shown in Figure 4.11. The measured S-parameters of a total 3200 μm CPW line on Si holder given in Figure 4.10 were used. As seen in figures, the ε_{reff} becomes nearly level at frequencies above 10 GHz. The computed $\varepsilon_{reff} = 6.36$ using the equation (4.15) and dimensions of CPW line on Si holder as described in the last section is independent of the frequency. At very low frequencies of a few gigahertzes, the ε_{reff} in Figure 4.11 (a) is very large and decreases quickly. It is not valid due to offset error in measured S21 in Figure 4.10 (a).

A more valid method of determining ε_{reff} would be to use the local slope of Figure 4.10(b). At first, we smooth the phase curve in Figure 4.10(b) and take away the offset value at very low frequencies (suppose the phase starts at zero), and then calculate the local slope as follows:

$$\frac{\Delta\theta}{\Delta f} = \frac{\theta_2(f_2) - \theta_1(f_1)}{\Delta f}$$

$$V_P = \frac{u_0}{\sqrt{\varepsilon_{reff}}} = \frac{\partial\omega}{\partial\beta} = \frac{2\pi\Delta f}{\Delta\theta / l}$$

$$\varepsilon_{reff} = \left[\frac{u_0 \Delta\theta / l}{2\pi\Delta f}\right]^2 = \left[\frac{u_0}{2\pi l}\frac{\Delta\theta}{\Delta f}\right]^2 = \left[\frac{u_0}{2\pi\frac{180}{\pi}l}\frac{\Delta\theta}{\Delta f}\right]^2$$

$$\varepsilon_{reff} \approx \left[(\frac{u_0}{360 l})(\frac{\theta(f+\Delta f) - \theta(f)}{\Delta f})\right]^2$$

The attenuation constant a in nepers per millimeter using the measured S-parameters in Figure 4.10 (a) is calculated by [63]:

$$|Loss(dB)| = |10\log e^{-2al}| = 20al\log e = 8.686al$$

$$a = \frac{Loss}{8.686l} \tag{4.20}$$

The attenuation constant is also plotted in Figure 4.11 (b) and is low in entire frequency range. Table 4.4 gives the propagation parameters of CPW line on Si holder (part 1) at selected frequencies as calculated using equations (4.18), (4.19), and (4.20).

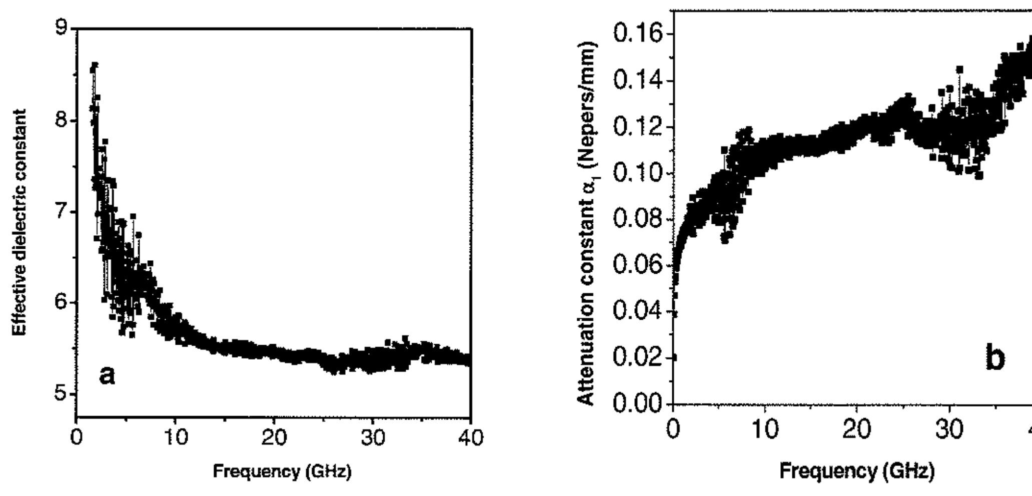


Figure 4.11 Effective dielectric constant and attenuation constant per millimeter using measured S-parameters of Figure 4.10.

Table 4.4 Propagation parameters per millimeter of 3200 µm CPW line on Si holder (part 1) using measured S-parameters in Figure 4.10

Frequency (GHz)	Loss (dB/mm)	Phase (Deg./mm)	Effective dielectric	Attenuation a_1 (nepers/mm)	Phase constant β_1 (rads/mm)	Propagation constant γ_1
10	0.936	28.79	5.76	0.108	0.502	0.108+0.502i
20	1.022	56.06	5.44	0.118	0.980	0.118+0.980i
30	1.130	83.66	5.39	0.124	1.462	0.124+1.462i
40	1.284	111.05	5.35	0.148	1.938	0.148+1.938i

2) HFSS simulation S-parameters

Since the CPW transmission line is not a perfect conductor, it has a dc resistance. In HFSS 9 simulation, the total losses should also consider the loss caused by dc resistance of the CPW line. A dc resistance can be used to compensate for the losses at low frequencies of a few gigahertzes in HFSS simulation. The calculated dc resistance of the

two case structures is 0.9 and 0.67 Ω as given in Table 4.3, respectively. Considering the effect of dc resistance, the HFSS simulation S-parameters of a 3200 μm CPW line on Si holder with and without a CPW cantilever (part 3) are shown in Figure 4.12. The simulated insertion losses are approximately 1 dB offset for both cases at 0.04 GHz. They match fairly well to the measured insertion losses as was previously shown in Figure 4.9. This indicates that the insertion loss at very low frequency is possibly caused by dc resistance. This also indicates the importance of the probe contact resistance when performing measurements.

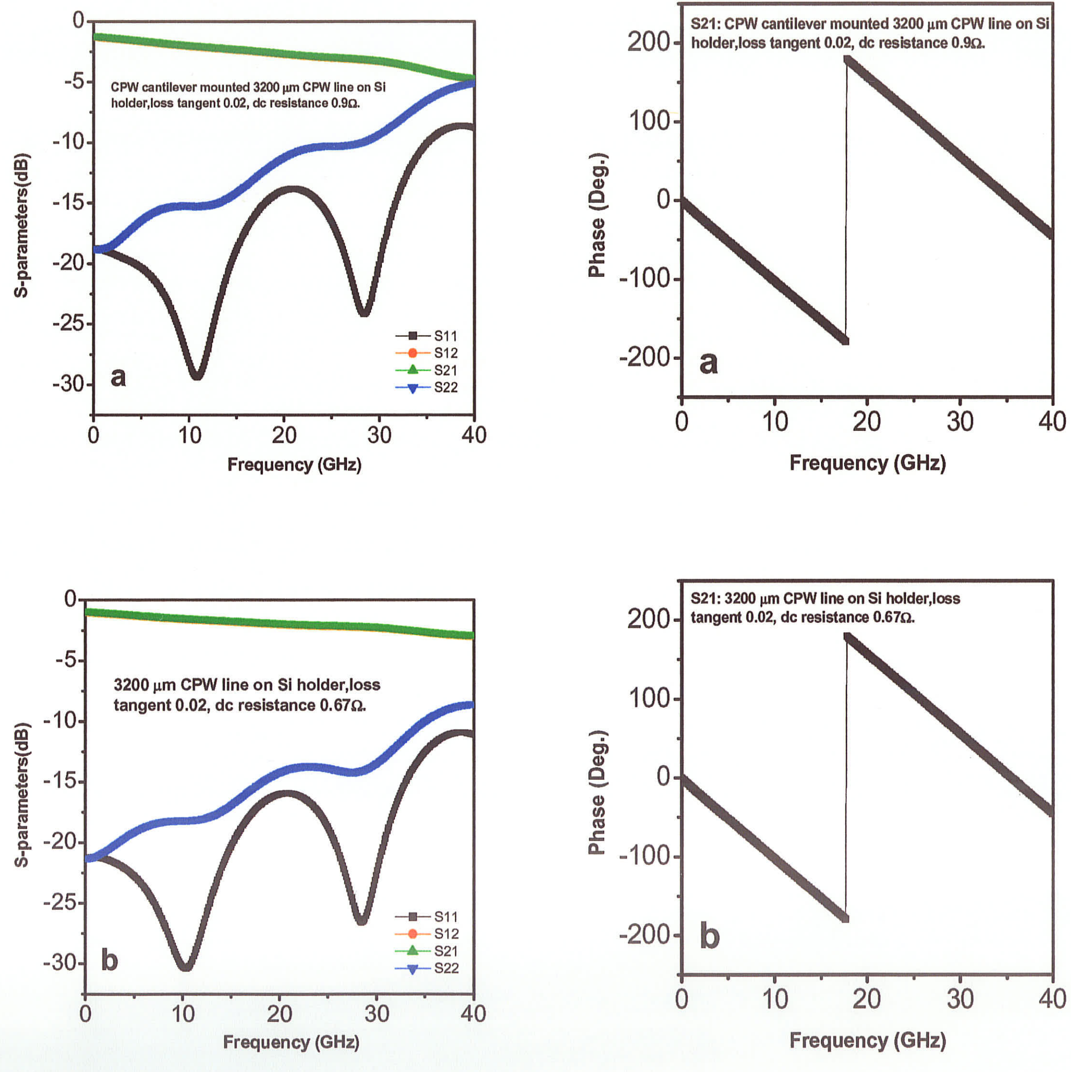
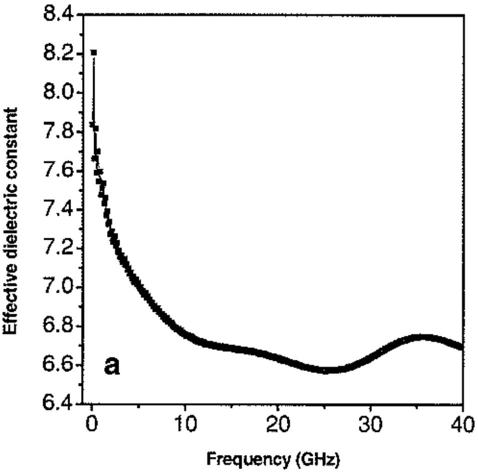


Figure 4.12 Simulation S-parameters (a) CPW cantilever (part3) mounted 3200 μm CPW line on a Si holder (part 1) in Figure 4.8 (a); (b) 3200 μm CPW line on a Si holder (part 1) in Figure 4.8 (b).

In addition, the simulated S-parameters in Figure 4.12 are in reasonable agreement with the measured S-parameters in Figure 4.9. There is particularly agreement for the case with no cantilever (Figure 4.9 (b), 4.10, 4.12 (b)). The simulated return losses at port 1 and port 2 for the two cases are different due to asymmetrical structure. The insertion losses of the two cases have almost the same range from 1 dB to 5 dB in the frequency range 0.04 - 40 GHz.

Similarly, using equations (4.18) and (4.19) and the simulation S-parameters of Figure 4.12 (b), the effective dielectric constant and attenuation constant per millimeter at frequency range 0.04-40 GHz are calculated and given in Figure 4.13. These results are compared with the measured ε_{reff} and attenuation per millimeter in the Figure 4.11 using measured S-parameters. The difference between calculated and measured ε_{reff} is about 1 at frequencies above 10 GHz and discrepancy in the attenuation may be due to the selected loss tangent 0.02 in HFSS simulation which is too low at low frequency and too high at high frequency. Table 4.5 gives the simulated propagation parameters of a CPW line on Si holder (part 1) at some selected frequencies.



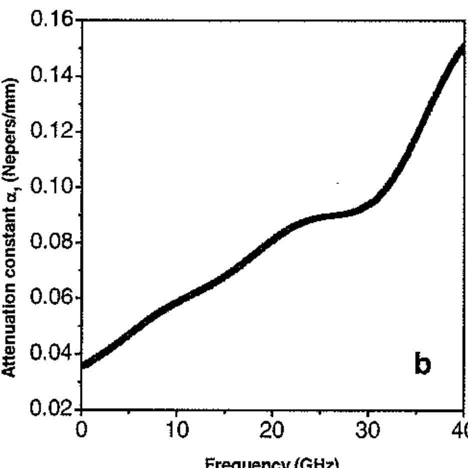
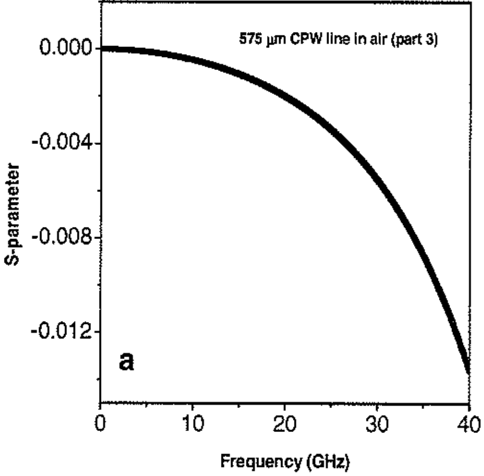


Figure 4.13 Effective dielectric constant and attenuation constant per millimeter using simulated S-parameter in Figure 4.12 (b).

Table 4.5 Propagation parameters per millimeter of 3200 μm CPW line on Si holder (part 1) using simulated S-parameter in Figure 4.11(b)

Frequency (GHz)	Loss (dB/mm)	Phase (Deg./mm)	Effective dielectric	Attenuation a_1 (nepers/mm)	Phase constant β_1 (rads/mm)	Propagation constant γ_1
10	0.506	31.2	6.76	0.058	0.545	0.058+0.545i
20	0.7	61.94	6.63	0.081	1.08	0.081+1.08i
30	0.813	92.70	6.64	0.094	1.618	0.094+1.618i
40	1.309	100.87	6.69	0.151	2.167	0.151+2.167i

For part 3, the simulated S-parameter magnitude and phase of the 575 μm CPW cantilever in air are given in Figure 4.14. The correspondingly simulated attenuation constant and phase constant per millimeter are calculated from the simulated S-parameter of the 575 μm CPW cantilever in air using equations (4.18) and (4.19) and are given in Figure 4.15. The ε_{reff} of the CPW cantilever in air is equal to 1. The attenuation constant shows the CPW cantilever in air is almost lossless. Table 4.6 gives the propagation parameters of CPW cantilever in air (part 3) at some selected frequencies.



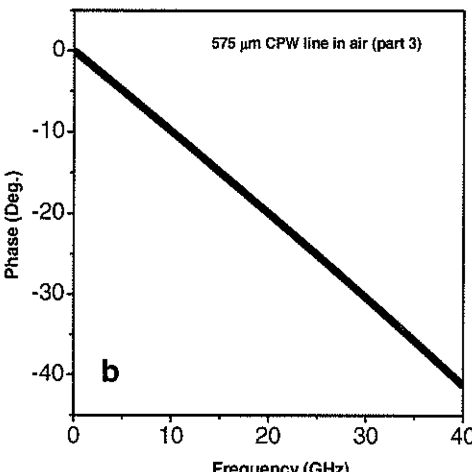
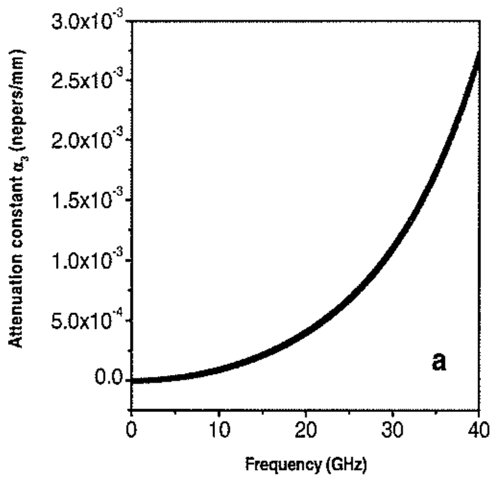


Figure 4.14 S11 magnitude and phase of a 575 μm CPW transmission line in air



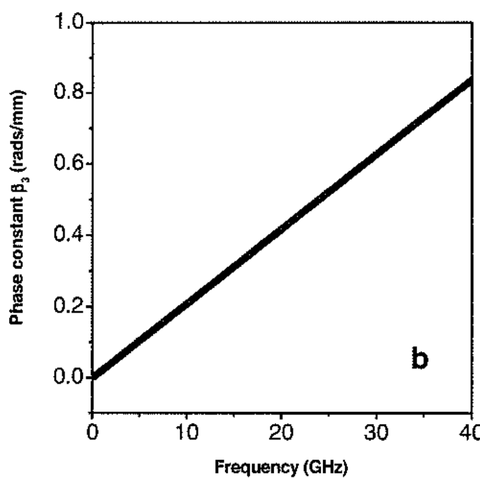


Figure 4.15 Attenuation constant and phase constant per millimeter using simulated S-parameters of 575 μm CPW cantilever in air.

Table 4.6 Propagation parameters per millimeter of 575 μm CPW cantilever in air (part 3) using simulated S-parameter

Frequency (GHz)	Loss (dB/mm)	Phase (Deg./mm)	Effective dielectric	Attenuation a_3 (nepers/mm)	Phase constant β_3 (rads/mm)	Propagation constant γ_3
10	3.63E-04	9.75	1	9.24E-05	0.210	9.24E-05+0.210i
20	1.73E-03	18.93	1	4.03E-04	0.419	4.03E-04+0.419i
30	4.93E-03	30.48	1	1.10E-03	0.628	1.10E-03+0.628i
40	1.17E-02	42.24	1	2.72E-03	0.838	2.72E-03+0.838i

3) Equivalent circuit model

In order to formulate a basic propagation equation of a MEMS CPW cantilever mounted by a Si holder, an ABCD matrix is selected. ABCD parameters are used because the overall results of a cascade of circuits can be easily determined by chaining the matrices from the individual circuits together. The three parts of the entire CPW cantilever can be considered as a two-port network shown in Figure 4.16 (a). The total ABCD matrix of entire CPW cantilever is given by

$$[ABCD_{total}] = [ABCD_{part\ 1}][ABCD_{part\ 2}][ABCD_{part\ 3}]$$

$$[ABCD_{total}] = [ABCD_{CPW\text{-}on\text{-}holder}][ABCD_{transition}][ABCD_{CPW\text{-}cantilever\text{-}in\text{-}air}]$$

Since the transition, a tapered CPW transmission line on Si holder, is small in length and is 50 Ω characteristic impedance, the above ABCD matrices can be merged and rewritten as

$[ABCD_{total}] = [ABCD_{CPW\text{-}transition\text{-}on\text{-}holder}][ABCD_{CPW\text{-}cantilever\text{-}in\text{-}air}]$

Therefore, ABCD matrices are easily written as

$$[ABCD_{CPW\text{-}transition\text{-}on\text{-}holder}] = \begin{bmatrix} \cosh \gamma_1 L & Z_1 \sinh \gamma_1 L \\ Y_1 \sinh \gamma_1 L & \cosh \gamma_1 L \end{bmatrix}$$

where $L = L_1 + L_2 = 3.0 + 0.2 = 3.2$ mm , $Z_1 = 48.92$ Ω, $Y_1 = 1/Z_1$, and propagation constant γ_1 per millimeter of CPW line on Si holder (part 1) was given in Figure 4.11 as based on measured results.

$$[ABCD_{CPW\text{-}cantilever\text{-}in\text{-}air}] = \begin{bmatrix} \cosh \gamma_3 L_3 & Z_3 \sinh \gamma_3 L_3 \\ Y_3 \sinh \gamma_3 L_3 & \cosh \gamma_3 L_3 \end{bmatrix}$$

where $L_3 = 600$ μm, $Z_3 = 141.8$ Ω, $Y_3 = 1/Z_3$, and propagation constant γ_3 per millimetre of CPW cantilever in air (part 3) as was given in Figure 4.15 based on simulated results.

Using ABCD approach, it is very easy to design different lengths of CPW line on Si holder (part 1) and CPW cantilever in air (part 3) and calculate its total ABCD parameters. The S-parameters of the final 2-port network, Figure 4.16 (b), can then be calculated using total ABCD parameters as follows:

$$S11 = \frac{+A + BY_0 - CZ_0 - D}{+A + BY_0 + CZ_0 + D} \quad (4.21)$$

$$S12 = \frac{2(AD - BC)}{+A + BY_0 + CZ_0 + D} \quad (4.22)$$

$$S21 = \frac{2}{+A + BY_0 + CZ_0 + D} \quad (4.23)$$

$$S22 = \frac{-A + BY_0 - CZ_0 + D}{+A + BY_0 + CZ_0 + D} \quad (4.24)$$

A CPW cantilever mounted with a CPW line on a Si holder can now be considered as shown in Figure 4.16 (a). In order to calculate its reflection coefficient of the entire structure for different terminations, the equivalent circuit model is inserted between the

unknown load and source impedance as shown in Figure 4.16 (b). The source and load impedance are assumed to Z_S and Z_T, respectively. To reduce unwanted reflections in high frequency circuits, the transmission lines have to be impedance matched. In most cases, the source impedance is always designed as 50 Ω.

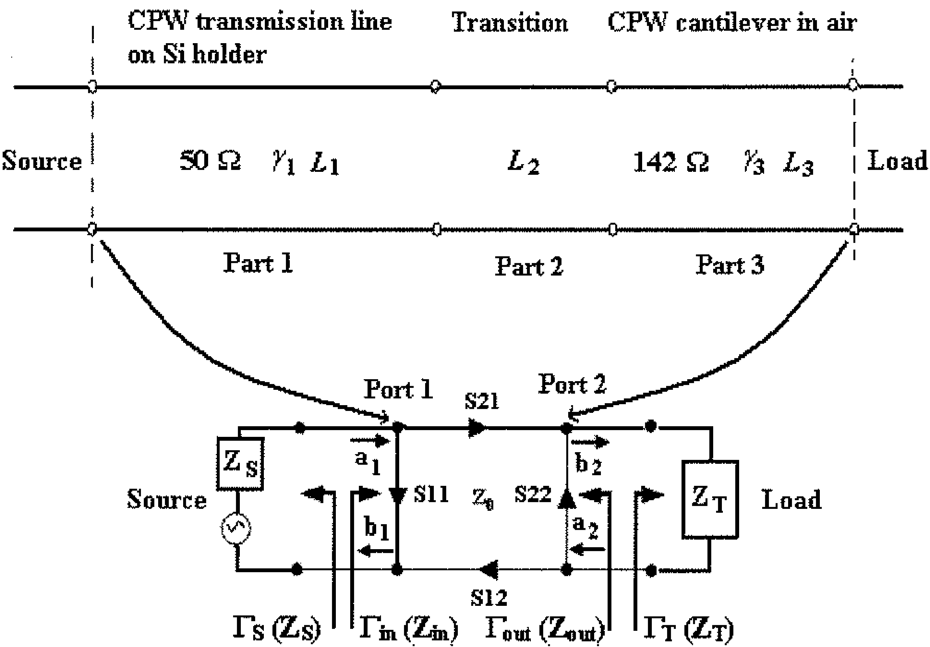


Figure 4.16 Equivalent circuit model for a CPW cantilever mounted CPW line on Si holder

(a) Cascade circuit; (b) S-parameter flow graph and equivalent model terminated in load Z_T.

In the equivalent circuit model, input reflection coefficient Γ_{in} can be calculated and determined in terms of the load reflection coefficient Γ_T, while output reflection coefficient Γ_{out} can be calculated and determined in terms of the source reflection coefficient Γ_S. The source and the output reflection coefficients have arrows pointing toward the left. They are related by the relationship.

$$a_2 = \Gamma_T b_2$$

$$b_1 = S11a_1 + S12a_2 = S11a_1 + S12\Gamma_T b_2$$

$$b_2 = S21a_1 + S22a_2 = S21a_1 + S22\Gamma_T b_2$$

$$b_2 = \frac{S21a_1}{1 - S22\Gamma_T}$$

$$b_1 = S11a_1 + S12\Gamma_T \frac{S21a_1}{1 - S22\Gamma_T}$$

$$\Gamma_{in} = \frac{b_1}{a_1} = S11 + \frac{S12S21\Gamma_T}{1 - S22\Gamma_T} = \frac{S11 - \Delta S\Gamma_T}{1 - S22\Gamma_T} \tag{4.25}$$

$$\Delta S = S11S22 - S12S21$$

$$\Gamma_T = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{\Gamma_{in} - S11}{\Gamma_{in}S22 - \Delta S} \tag{4.26}$$

Note the last equation is not valid when S12 is zero. When S12 is zero, Γ_{in} is always equal to S11. When S12 is not zero, then the Γ_{in} is not equal to S11.

Similarly, the Γ_{out} is related to the Γ_S. The relationship is as follows.

$$\Gamma_{out} = \frac{b_2}{a_2} = S22 + \frac{S12S21\Gamma_S}{1 - S11\Gamma_S} = \frac{S22 - \Delta S\Gamma_S}{1 - S11\Gamma_S} \tag{4.27}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} = \frac{\Gamma_{out} - S22}{\Gamma_{out}S11 - \Delta S} \tag{4.28}$$

It is important to point out that Γ_{in} is not equal to S11 and that Γ_{out} is not equal to S22. They have equality only when the opposite port is terminated in a zero reflection coefficient impedance or when S12S21 = 0.

When the load Z_T is changed, Γ_T changes. Changing load Z_T does not affect the Γ_{out} or the Γ_S. Similarity, the Γ_S does not affect the Γ_{in} or the Γ_T. The Γ_S does affect the Γ_{out}.

4) Different load conditions

(1) If a lossy CPW transmission line, which has dielectric and conductor loss, has a matched source and load, $Z_0 = Z_T = Z_S$, $\Gamma_T = \Gamma_S = 0$, then $S11 = S22 = 0$. The scattering matrix for the lossy CPW line is then given by

$$S=\begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix}=\begin{bmatrix} 0 & e^{-rl} \\ e^{-rl} & 0 \end{bmatrix}=\begin{bmatrix} 0 & e^{-al}e^{-j\beta l} \\ e^{-al}e^{-j\beta l} & 0 \end{bmatrix}=\begin{bmatrix} 0 & e^{-al}e^{-j\theta} \\ e^{-al}e^{-j\theta} & 0 \end{bmatrix}$$

where $e^{\gamma l}=\cosh(\gamma l)+\sinh(\gamma l)$, $\gamma=a+j\beta$ and the length of transmission line is l and phase shift θ is negative for a positive length line. α is the attenuation constant and β is the phase constant for the transmission line. The input reflection coefficient is given as

$$\Gamma_{in}=S11+\frac{S12S21\Gamma_T}{1-S22\Gamma_T}=0$$

For a lossless CPW line transmission line with a matched load and source, $\alpha=0$, $\Gamma_T=\Gamma_S=0$, and $S11=S22=0$. Therefore the S-parameter matrix becomes

$$S=\begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix}=\begin{bmatrix} 0 & e^{-j\theta} \\ e^{-j\theta} & 0 \end{bmatrix}$$

The input reflection coefficient is given as

$\Gamma_{in}=S11+S12S21\Gamma_T/(1-S22\Gamma_T)=0$

(2) If the equivalent circuit model is terminated in an open circuit, $Z_T=\infty$, then $\Gamma_T=1$. The input reflection coefficient is given as

$$\Gamma_{in}=S11+\frac{S12S21\Gamma_T}{1-S22\Gamma_T}=S11+\frac{S12S21}{1-S22} \tag{4.29}$$

3) If the equivalent circuit model is terminated in a short circuit, $Z_T=0$, then $\Gamma_T=-1$. The input reflection coefficient is given as

$$\Gamma_{in}=S11+\frac{S12S21\Gamma_T}{1-S22\Gamma_T}=S11-\frac{S12S21}{1+S22} \tag{4.30}$$

The input return loss can be expressed in dB as

$$\text{Return loss (dB)}=-20\log_{10}(\Gamma_{in}) \tag{4.31}$$

4.2.2.2 CPW cantilever mounted on a 5000 μm CPW line on Si holder

Figure 4.17 shows a ground connected stressed MEMS CPW cantilever. The measured dimensions are given in Table 4.7. In the previous section 4.1 we measured its mechanical properties, such as resonant frequency, quality factor, and spring constant and were given in Table 4.2 (No.2).

The measured magnitude and phase of the reflection coefficient are given in Figure 4.18 (a). The measured return loss is below 7.5 dB in the range 0.04-40 GHz. The reflection loss result is mainly due to insertion loss of the CPW line and the termination which is an open circuit at the end of the cantilever. The oscillations in Figure 4.18 (a) are due to the input impedance varying from high to low as the electrical length varies through 90 degrees. From the measured S-parameters in Figure 4.9 (b), the loss of a 3200 μm CPW transmission line on Si holder is about 3.4 dB at 20 GHz. The loss of the 5000 μm CPW transmission line on Si holder will be larger than that of 3200 μm CPW transmission line on Si holder. Note, the phase in Figure 4.18 (a) is already corrected using the phase compensation of open circuit in the same condition (we will discuss latter). The measured phase in Figure 4.18 (a) should begin at zero, but it is approximately 30° at very low frequency (we don't give in the thesis). The phase varies more rapidly due to a reference plane error.

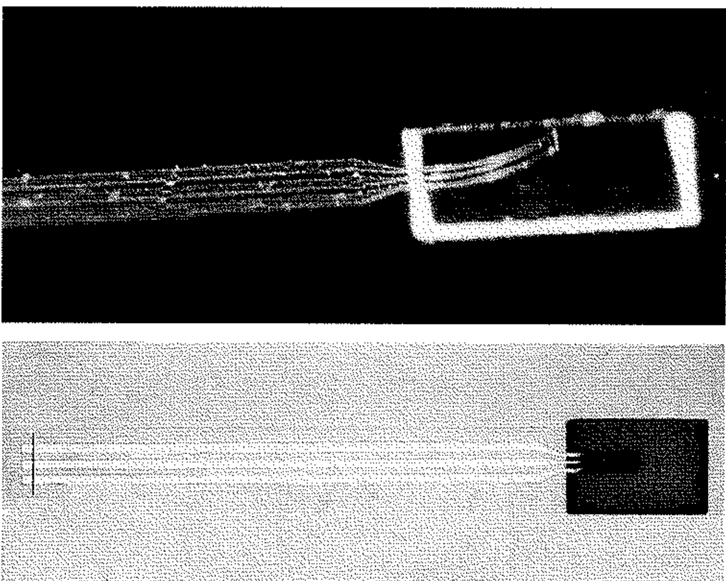


Figure 4.17 A ground connected stressed MEMS CPW cantilever (a) 3D view; (b) Top view.

Table 4.7 Three part dimensions and dc resistance of fabricated CPW cantilever

	Part 1: CPW line on Si holder	Part 2: transition on Si holder	Part 3: CPW cantilever in air	dc resistance
Center beam	L = 5000 μm w = 97 μm	200 μm	L = 575 μm w = 40 μm	1.2 Ω
Side beams	L = 5000 μm w = 97 μm		L = 643 μm w = 40 μm	

In addition, the one-port reflection coefficient can be calculated using the equivalent circuit model terminated in an open circuit. Therefore it is considered as a one-port network and its reflection coefficient is calculated as follows.

The total ABCD parameters of a CPW cantilever mounted a CPW line on a Si holder are given as

$$[ABCD_{total}] = [ABCD_{CPW\text{-}transition\text{-}on\text{-}holder}][ABCD_{CPW\text{-}cantilever\text{-}in\text{-}air}]$$

$$[ABCD_{CPW\text{-}transition\text{-}on\text{-}holder}] = \begin{bmatrix} \cosh\gamma_1 L & Z_1\sinh\gamma_1 L \\ Y_1\sinh\gamma_1 L & \cosh\gamma_1 L \end{bmatrix}$$

where $L = L_1+L_2 = 5.2$ mm, $Z_1 = 48.92\ \Omega$, $Y_1 = 1/Z_1$, and propagation constant γ_1 per millimeter based on measured results of part 1 and is given in Figure 4.11 and Table 4.4.

$$[ABCD_{CPW\text{-}cantilever\text{-}in\text{-}air}] = \begin{bmatrix} \cosh\gamma_3 L_3 & Z_3\sinh\gamma_3 L_3 \\ Y_3\sinh\gamma_3 L_3 & \cosh\gamma_3 L_3 \end{bmatrix}$$

where L_3 = 575 μm, Z_3 = 141.8 Ω, $Y_3 = 1/Z_3$, and propagation constant γ_3 in air per millimetre based on simulated results of part 3 is given in Figure 4.15 and Table 4.6.

Then, S-parameters can be calculated using total ABCD parameters. In this case of the equivalent circuit model terminated in an open circuit, $\Gamma_T = 1$, the input reflection coefficient in terms of equation (4.31) is given as

$$\Gamma_{in} = S11 + \frac{S12S21\Gamma_T}{1 - S22\Gamma_T} = S11 + \frac{S12S21}{1 - S22}$$

The magnitude and phase of the reflection coefficient of the ground connected CPW cantilever are calculated using the equivalent circuit model terminated in an open circuit and are given in Figure 4.18 (b). Table 4.8 gives total ABCD parameters, S-parameters,

and reflection coefficients using the equivalent circuit model terminated in an open circuit at selected frequencies. Figure 4.18 (c) gives the HFSS simulation reflection coefficient results.

In comparison with the measured results in Figure 4.18 (a), the curves of reflection coefficient using the equivalent circuit model and using HFSS simulation are similar. The possible reason causing the discrepancy of reflection coefficient is that there is a small capacitance at the end of CPW cantilever in air between the center beam and ground-connected side beams.

The phase error of reflection coefficient using the equivalent model is also about 30 degrees at very low frequency. The same result is given by the measured phase in Figure 4.18 (a) (before it is corrected). However they should begin at zero.

Table 4.8 ABCD and S-parameters of CPW cantilever mounted 5000 μm CPW line on Si holder using equivalent circuit model in an open circuit

	ABCD parameters	S-parameters	Reflection coefficient
10 GHz	A = -0.94608 + 0.28869i B = -26.462 +16.083i C = -0.09121 + 0.01251i D = -1.1467 + 0.15512i	S11=-0.055161+ 0.030434i S12 = -0.53955 - 0.24384i S21 = -0.53955 - 0.24384i S22 = 0.020526 + 0.15143i	0.13527 + 0.32852i
20 GHz	A = 0.29322+0.58064i B = 25.589+48.089i C = 0.0031455-0.02262i D = 0.99685-0.51622i	S11 = -0.072704 - 0.064795i S12 = 0.27962 + 0.45526i S21 = 0.27962 + 0.45526i S22 = 0.09471 + 0.27355i	0.28123 - 0.15343i
30 GHz	A = 0.42553+0.51454i B = -11.89+75.449i C = 0.004426+0.02065i D = -0.47683+0.78474i	S11 = 0.050738 - 0.11689i S12 = -0.0094475 - 0.52099i S21=-0.0094475 -0.52099i S22 = 0.20005 + 0.35162i	0.23807 + 0.23152i
40 GHz	A = -1.0456-0.31453i B = -20.065-96.264i C = -0.013446-0.0102i D = -0.64768-1.23886i	S11 = 0.097986 + 0.036138i S12 = -0.23482 + 0.33852i S21 = -0.23482 + 0.33852i S22 = 0.31743 + 0.38789i	0.1322 - 0.17734i

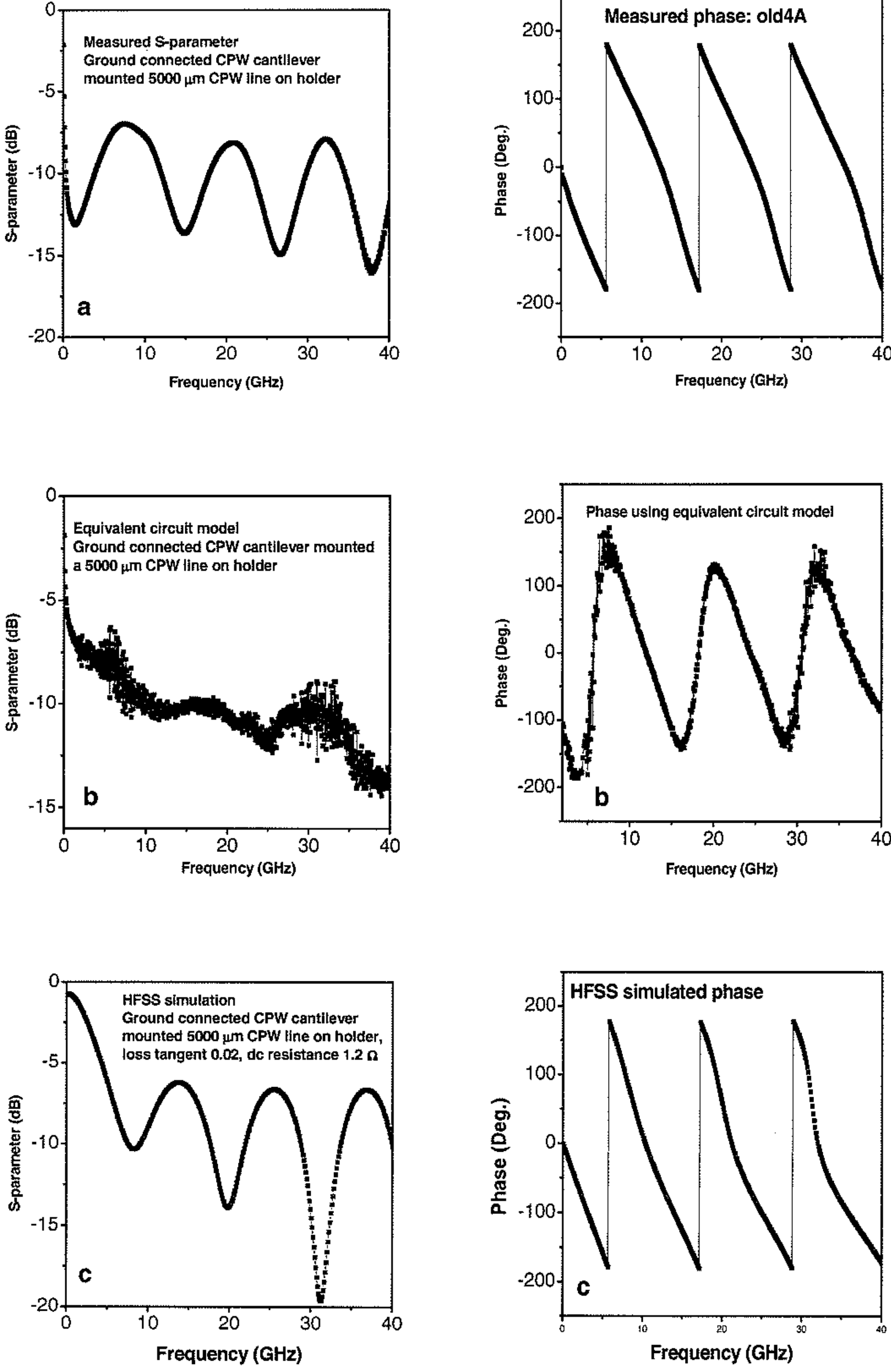


Figure 4.18 Magnitude and phase of S-parameter of CPW cantilever mounted 5000 μm CPW on a Si holder in Figure 4.17 using (a) Measurement; (b) Equivalent circuit model; (c) HFSS simulation.

Although the errors of the equivalent circuit model and HFSS simulation are very large, both methods can be used to estimate S-parameter of different lengths of CPW cantilever or CPW line on Si holder without complicated microwave equipment. The possible reasons for large errors are that the selected loss tangent 0.02 in HFSS simulation is too low at low frequencies and too high at high frequencies and the frequency shift is due to the method we used to estimate ε_{reff}.

4.2.2.3 CPW cantilevers with ground connected for both ends

Figure 4.19 shows the fabricated MEMS CPW cantilevers with ground connections at both ends. One is a CPW cantilever suspended by a thin SiO_2 membrane as shown in Figure 4.19 (a) and another is a CPW cantilever suspended in air as shown in Figure 4.19 (b). The membrane is the remained SiO_2 layer after backside KOH deep etch. Both CPW cantilevers have the same dimensions given in Table 4.9.

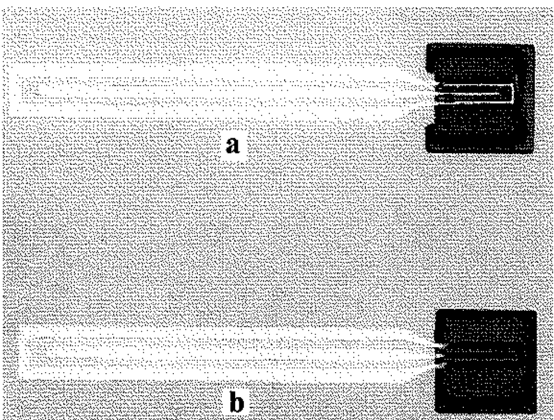


Figure 4.19 Ground connected for both ends of CPW cantilevers (a) on membrane; (b) in air.

Table 4.9 Three part dimensions and dc resistance of fabricated CPW cantilevers

	Part 1: CPW line on Si holder	Part 2: Transition on Si holder	Part 3: CPW cantilever with or without membrane	dc resistance
Center beam	$L = 2600$ μm $w = 97$ μm	200 μm	$L = 600$ μm $w = 35$ μm	0.80 Ω
Side beams	$L = 2800$ μm $w = 97$ μm		$L = 635$ μm $w = 37.5$ μm	

The measured reflection coefficients of the CPW cantilevers with and without thin SiO_2 membrane at frequency range from 0.04 to 40 GHz are shown in Figure 4.20 (a). (The phases are already corrected using the phase compensation of open circuit in the same condition.). The magnitude and phase curves of reflection coefficients are almost the same in shape, respectively. This demonstrates the repeatability of both the fabrication method and probing method. Comparing the two cases, the CPW cantilever either with or without a SiO_2 membrane shows it is not an important factor in electrical performance. It indicates the membrane below the CPW cantilever does not affect the reflection coefficient of CPW cantilever. The reflection losses indicate corresponding average transmission loss of approximately 3 dB over the frequency range. Therefore, the propagation properties of the stressed MEMS CPW cantilever with and without membrane are also mainly determined by those of CPW transmission line on Si holder. The amplitude of reflection loss for the two cases varies by approximately 4 dB from 4 dB to 8 dB. It is reasonable that its loss is less than that of the CPW cantilever mounted 5000 μm CPW line on Si holder in Figure 4.18 (a), where the amplitude of reflection loss varied by approximately 5 dB from 7.5 dB to 12.5 dB.

Using the equivalent circuit model, the magnitude and phase of the S11 of the CPW cantilever mounted 2600 μm CPW line on Si holder with ground connected for both ends are calculated and shown in Figure 4.20 (b). Since its length is shorter than the 5000 μm CPW line on Si holder in Figure 4.17, it is reasonable that the reflection loss in Figure 4.20 (b) is smaller than that in Figure 4.18 (b).

The HFSS simulation S11 of the 600 μm CPW cantilever mounted on a 2600 μm CPW transmission line on Si holder with ground connected for both ends is also shown in Figure 4.20 (c). The possible reasons for the large errors are that there is a small capacitance at the end of CPW cantilever in air between the center beam and ground-connected side beams.

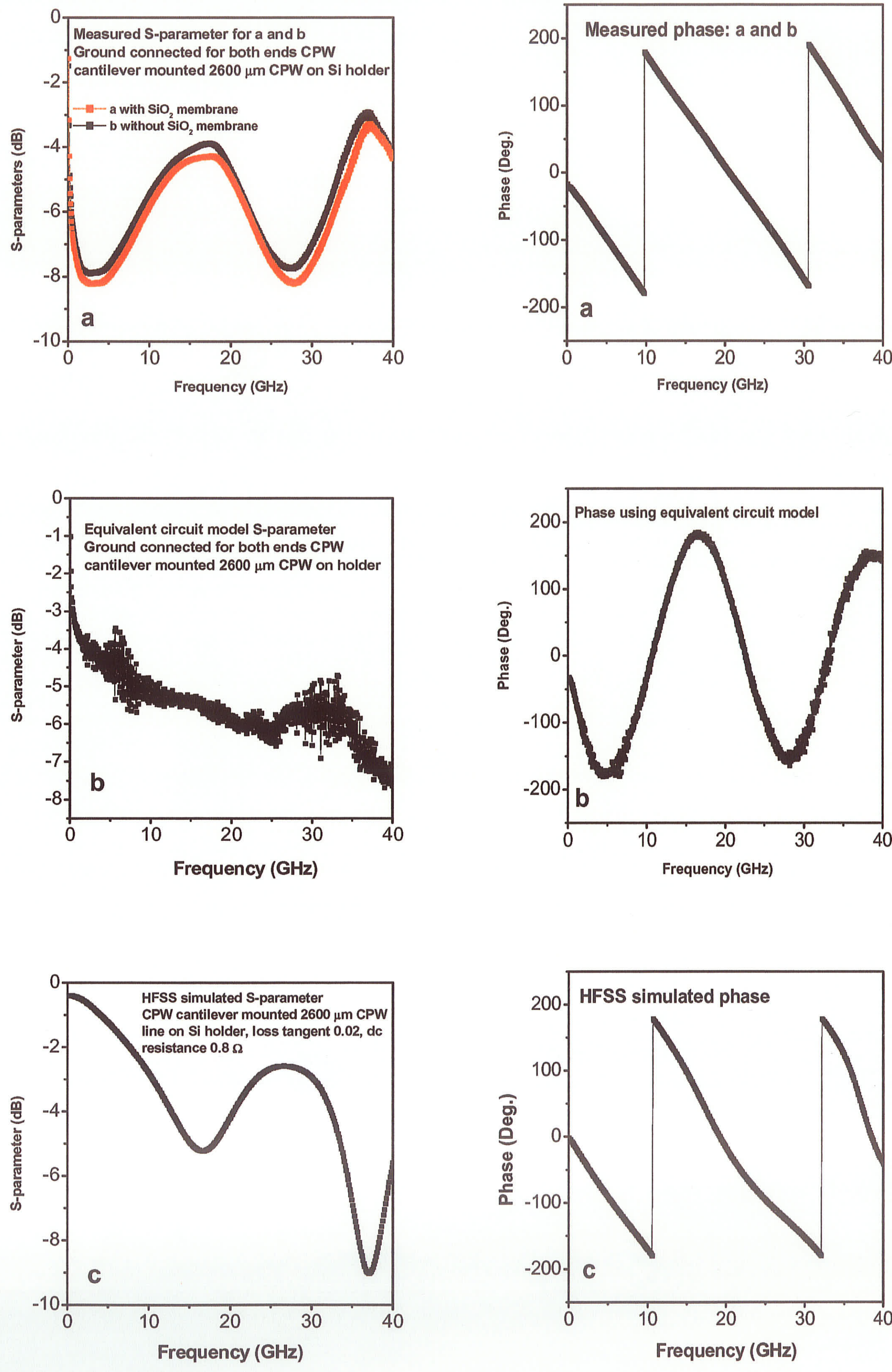


Figure 4.20 Magnitude and phase of the reflection coefficients of CPW cantilever mounted 2600 μm CPW line on a Si holder using (a) Measurement; (b) Equivalent circuit model; (c) HFSS simulation.

4.2.2.4 SOLT calibration

Figure 4.21 shows a simple block diagram of a vector network analyzer (VNA) in microwave measurement. The S-parameter measurement consists of a device under test (DUT) embedded in a fixture connected to the VNA with appropriate cables. The point at which the DUT connects with the measurement system is defined as the DUT reference plane. Measuring the characteristics of devices on a wafer level is achieved by connecting microwave probes directly to the wafer.

However, any measurement includes not only that of the DUT, but contributions from the fixture and cables as well. With increasing frequency, the electrical contribution of the fixture and cables becomes increasingly significant.

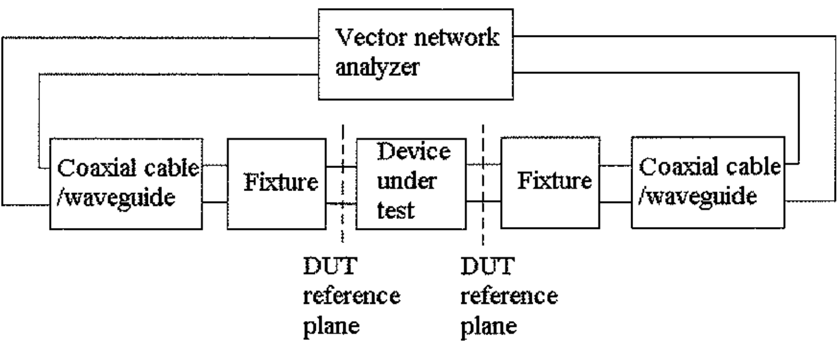
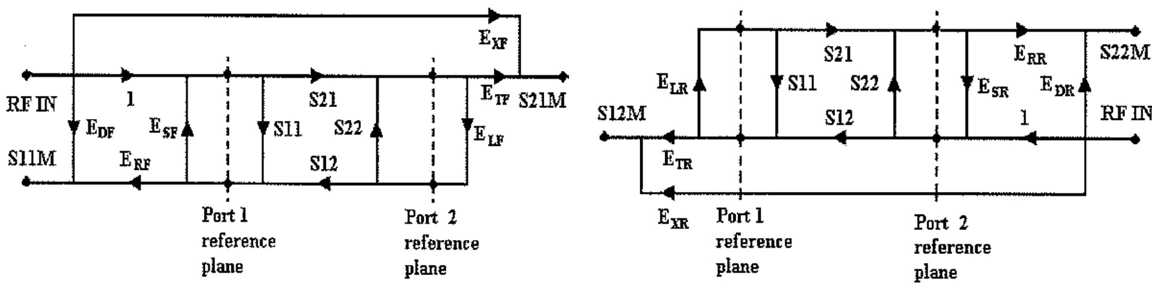


Figure 4.21 A VNA in microwave measurement [64].

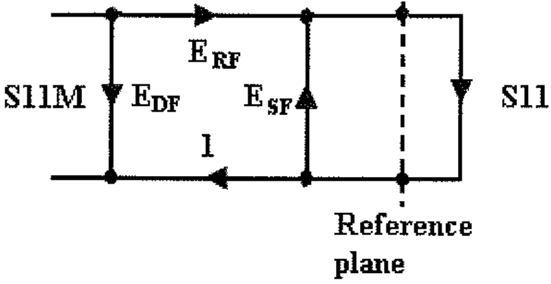
Sources of uncertainty or error in VNA measurements are primarily the result of systematic, random, and drift errors. The latter two effects tend to be unpredictable and therefore cannot be removed from the measurement. They are the results of factors such as system noise, connector repeatability, temperature variations, and physical changes within the VNA. Systematic errors are repeatable and can be largely removed through a process of calibration. Of the three, systematic errors are generally the most significant, particularly at RF and microwave frequencies. To lessen the contribution of systemic error, remove contributions of cabling and fixturing, and therefore enhance measurement

accuracy, the VNA must first be calibrated though a process of applying and measuring standards in lieu of the DUT. In calibration, such errors are quantified by measuring characteristics of known devices (standards). Hence, once quantified, systematic errors can be removed from the resulting measurement.

In this thesis, S-parameters are measured using on wafer short-open-load-thru (SOLT) calibration. Figure 4.22 shows two-port and one-port VNA error models. By measuring the full two-port S-parameters of a set of known references such as opens, shorts, matched loads, and known lengths of transmission lines, a system of equations can be derived that includes the error terms. The error terms can then be solved for and applied to the results of the measurement of an unknown two-port device to correct for measurement system deviations from the ideal. DUT parameters S11 and S21 can be described as functions of S11M, S21M, S12M, S22M and the six forward error terms in Figure 4.22 (a). Likewise, S12 and S22 are functions of the four measured S-parameters and six reverse error terms. Hence, when each error coefficient is known, the DUT S-parameters can be determined from uncorrected measurement. Therefore, SOLT calibration is essentially the process of determining these error coefficients.



(a) Typical two-port VNA error model: forward model (left) and reverse model (right).



(b) One-port VNA error model for reflection coefficient measurements

Figure 4.22 Two-port and one-port VNA error models [64]

In this thesis we used on-wafer calibration standard to measure the error terms. The Anritsu (ME-7808A) VNA then automatically applies these to produce actual DUT s-parameters.

Figure 4.23 (a) gives the S-parameter magnitude and phase of a short circuit done with the GSG probe contacting the CPW copper material on the Si holder. Figure 4.23 (b) gives the S-parameter magnitude and phase of an open circuit. It exhibits imperfections because fringing and radiated fields at the end of the transmission line result in phase and amplitude errors. The difference between the phase of a reflected wave of an open and a short circuit is approximately 180 degrees.

The measured phase deviation with frequency should be constant. However, Figure 4.23 (b) shows a variation of 500° over 40 GHz (corresponding to a physical length of 1 cm in air). This phase error would be evident in measured results of S11. A correction in phase of 500/40 GHz = 12.5 °/GHz was applied to the measured results in Figure 4.18 (a) and 4.20 (a) to compensate for this. Another method is to use the measured phases in Figure 4.18 (a) and 4.20 (a) subtract the phase of open circuit in Figure 4.23 (b) and we will get actual phase of the two cases.

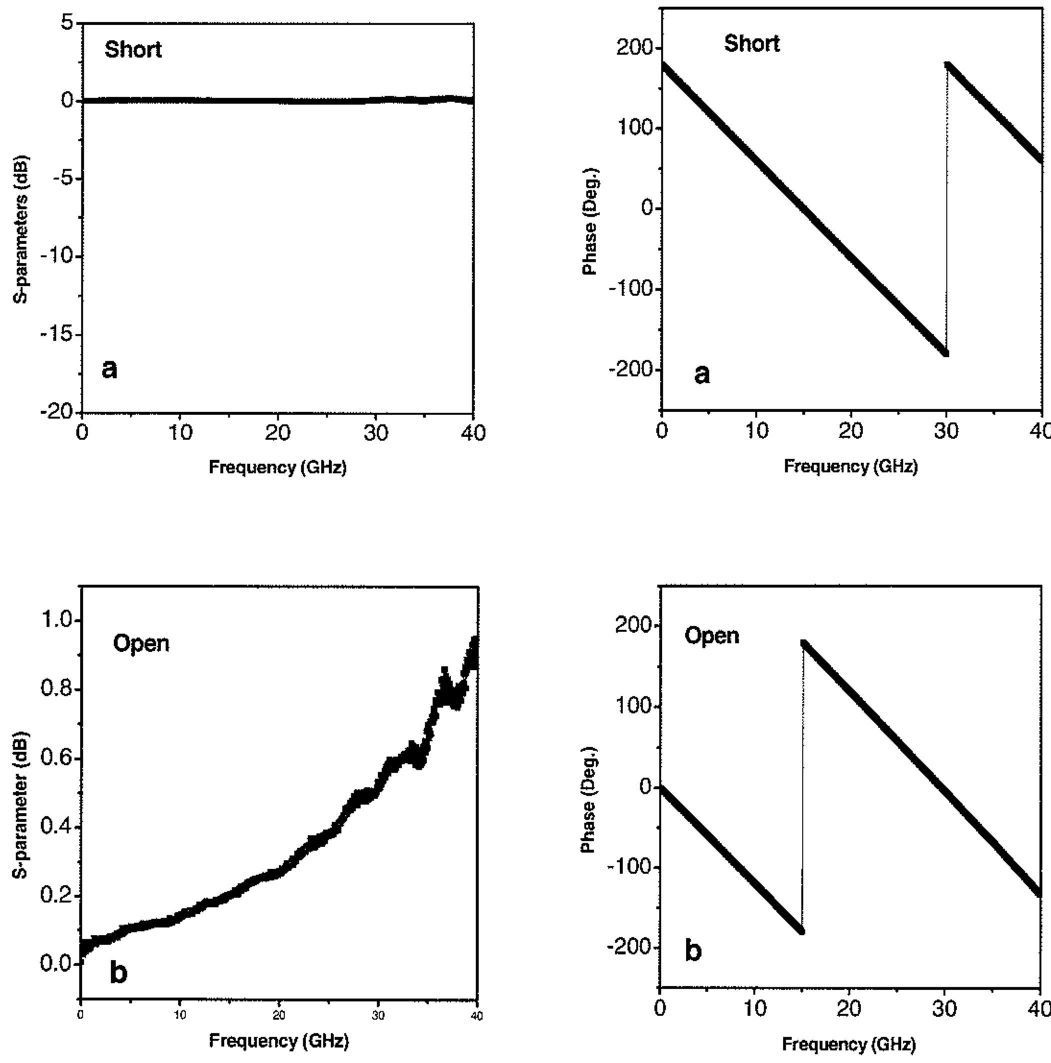


Figure 4.23 Magnitude and phase of short circuit and open circuit.

Chapter 5 Conclusions and future work

5.1 Conclusions

A new MEMS CPW cantilever was introduced in this thesis to overcome the limitations of conventional cantilevers in EFM. The detailed steps of design, modeling, simulation, fabrication, and testing the MEMS CPW cantilevers were presented.

Through analyzing the selection considerations for the design of CPW cantilevers, high-resistivity silicon and copper are selected as the substrate and conductor, respectively. Theoretical design equations give the relationship between the characteristic impedance, effective dielectric constant, attenuation, and dimensions of CPW lines and also give the optimum dimensions of CPW cantilevers to reduce losses. The HFSS numerical electromagnetic simulation program allowed for simulation, modification, and verification of the designed CPW cantilevers.

The stressed MEMS CPW cantilevers were fabricated on a high resistivity Si wafer at the MEMS lab of University of Manitoba. The stressed CPW cantilevers were approximately 640 μm long with a corresponding bending height of 130 μm. A simple model was developed to explain the reasons causing the bending in the stressed MEMS cantilevers. Using the measured dimensions of CPW cantilevers, the stress, resonant frequency, spring constant, and quality factor were calculated. Measured results of resonant frequency were consistent with computed results.

With respect to the electrical properties of CPW cantilevers, the measured return loss of the CPW cantilever was found to be dominated by the lossy CPW-on-Si holder section of the cantilever. This was approximately 3 dB at 20 GHz. In comparison with calculated S-parameter using an equivalent circuit model and simulated results using HFSS, the measured S-parameters were discussed and analyzed. Both the equivalent circuit model and HFSS simulation can approximately predict the S-parameters of the stressed CPW cantilever.

5.2 Future work

5.2.1 Fabrication the CPW cantilever tip

The next step in the development of high-speed cantilevers for application in dynamic EFM is to fabricate a probe tip at the end of central beam of the CPW cantilever. The detailed fabrication steps of a MEMS CPW cantilever which has an integrated probe tip is shown in Figure 5.1 and given as follows:

1. Deposit photoresist on both sides of Si wafer covered with SiO_2 insulating layers.
2. Use mask 1 to define the cavity and V-groove on backside of Si wafer, expose and develop photoresist.
3. BOE etch exposed SiO_2 regions at backside of Si wafer.
4. KOH deep etch for backside of Si wafer.
5. Use mask 2 to define cantilever beam regions and form the unwanted SiO_2 regions on frontside, expose and develop photoresist.
6. BOE etch SiO_2 at unwanted regions at frontside of Si wafer.
7. Deposit photoresist and use mask 3 to define cantilever tip.
8. Use XeF_2 etch to form the tip on the frontside of Si wafer and remove the photoresist.
9. Deposit the metals and then photoresist; use the mask 4 to apply and pattern the CPW transmission lines on frontside of Si wafer.
10. Metal etchant to remove metal at unwanted regions.
11. Remove photoresist and use XeF_2 gas backside etch the remained Si wafer at membrane to release CPW cantilever.
12. CPW cantilever with tip suspended in air. CPW cantilever is mounted by Si holder

5.2.2 CPW cantilever tip in EFM

Future research on this topic would involve implementing a stressed CPW cantilever with tip in an EFM configuration and analyzing its performance for the measurement of high frequency signals at the internal nodes of an IC.

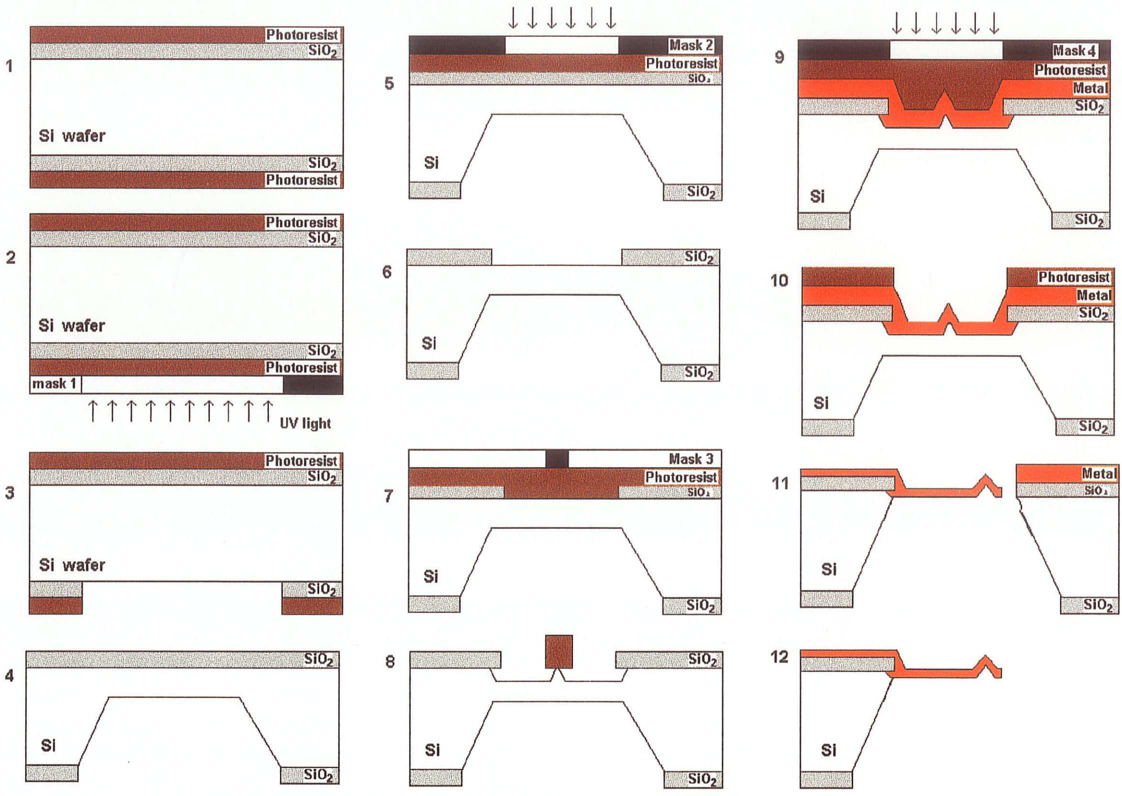


Figure 5.1 Fabrication steps for CPW cantilever with probe tip (Not to scale).

Reference

[1] GGB Industries Inc., (http://www.picoprobe.com).

[2] G. Rabjohn, J. Wolczanski, and R. Surridge, "High-frequency wafer-probing techniques," *Canadian Journal of Physics,* Vol. 65, No.8, pp. 850-855, 1987.

[3] W.Mertin, A.Leyk, U.Behnke, and V.Wittpahl, "Contactless gigahertz testing," *Test Conference, 1998. Proceedings. International*, 18-23, pp.843 –852, Oct. 1998.

[4] Björn Rosner, and Daniel van der Weide, "High-frequency near-field microscopy," *Rev. Sci. Instrum.*, Vol. 73, No.7, pp.2505-2525, July 2002.

[5] B.A.Nechey, F.Ho, A.S.Hou, and D.M.Bloom, "Application of an atomic force microscope voltage probe with ultrafast time resolution," *J.Vac.Sci.Technol.B*, Vol.13, No.3, pp.1369-1374, May 1995.

[6] R. A. Said, G. E. Bridges, and D. J. Thomson, "Non-invasive scanned probe potentiometry for integrated circuit diagnostics," *IEEE Trans. Instrum. Meas.*, Vol.43, No.3, pp.469-474, 1994.

[7] J.W.Hong, Z.G.Khim, A.S.Hou and Sang-il Park, "Noninvasive probing of high frequency signal in integrated circuits using electrostatic force microscope," *Rev.Sci.Instrum.*, Vol.68, No. 12, pp.4506-4510, Dec. 1997.

[8] G. E. Bridges and D. J. Thomson, "High frequency circuit characteristization using the AFM as a reactive near field probe," *J. Ultramicrosc.*, Vol. 42-44, pp.321-328, 1992.

[9] G.E.Bridges, R.A.Said, M.Mittal, and D.J.Thomson, "High-frequency pattern extraction in digital integrated circuits using scanning electrostatic force microscopy," *J.Vac.Sci.Technol.*, Vol.13, No.3, pp.1375-1379, May-June 1995.

[10] K.Domansky, Y.Leng, C.C.Williams, J.Janata, and D.Petelenz, "Mapping of mobile charges on insulator surfaces with the electrostatic force microscope" *Appl.Phys.Lett.*, Vol. 63, No.11, pp.1513-1515, 1993.

[11] A.S.Hou, F.Ho, and D.M.Bloom, "Picosecond electrical sampling using a scanning force microscope," *Electronics Letters*, Vol.28, No.25, pp.2302-2303, Dec.1992.

[12] G. E. Bridges, R.A. Said, and D. J. Thomson, "Heterodyne electrostatic force microscopy for non-contact high frequency integrated circuit measurement," *J. Vac. Sci. Technol.-A*, Vol.29, No.16, pp.1448-1449, Aug. 1993.

[13] A. D. Dimarogonas, *Vibration for Engineers*, Prentice-Hall, Inc., New Jersey, USA, 1996.

[14] http://www.nanoscience.com/products/budgetsensors_con.html

[15] Soonil Hong, Ken Lee and J.C.Bravman, "Design and fabrication of a monolithic high-density probe card for high frequency on wafer testing," *Electron Devices Meeting, 1989. Technical Digest. International*, pp. 289 –292, 1989.

[16] A.S.Hou, B.A.Nechay, F.Ho, D.M.Bloom, "Scanning probe microscopy for testing ultrafast electric devices," *Optical and Quantum Electronics*, Vol.28, pp.819-841, 1996.

[17] Y. Seo, W.Jhe, and C.S.Hwang, "Electrostatic force microscropy using a quartz tuning fork," *Appl. Phys. Lett.*, Vol.80, No.23, pp.4324-4326, June 2002.

[18] C.P.Wen, "Coplanar waveguide: a surface strip transmission line suitable for nonreciprocal gyromagnetic device applications," *IEEE Trans. Microwave Theory Tech.*, Vol. 17, No12, pp.1087-1090, Dec.1969.

[19] R.E.Simons, *Coplanar Waveguide Circuits, Components, and Systems*, Wiley-Interscience, 2001.

[20] T.M.Weller, L.P.B.Katehi, and G.M.Rebeiz, "High performance microshild line components," *IEEE Trans. Microwave Theory Tech.*, Vol.43, No.3, pp.534-543, March 1995.

[21] J.Browne, "Coplanar circuits arm limiting Amp with 100-dB gain," *Microwaves RF*, Vol.29, No.4, pp.213-220, April 1990.

[22] J.Browne, "Broadband amps sport coplanar waveguide," *Microwaves RF*, Vol.26, No.2, pp.131-134, Feb.1987.

[23] R.Majidi-Ahy, et al., "5-100GHz InP CPW MMIC 7-section distributed amplifier," *1990 IEEE Microwave millimetre-wave monolithic circuits symp. dig.*, pp.31-34, Dallas, Texas, May 7-8, 1990.

[24] R.E.Stegens and D.N.Alliss, "Coplanar microwave integrated circuit for integrated subsystems," *Microwave Sys. News Comm. Tech.*, Vol. 17, No. 11, pp.84-96, Oct. 1987.

[25] D. W. van der Weide and P. Neuzil, "The nanoscilloscope: combined topography and AC field probing with a micromachined tip," *J. Vac. Sci. Technol. B*, Vol. 14, No. 6, pp. 4144–4147, Nov. 1996.

[26] Björn Rosner, John Peck, and Daniel van der Weide, "Near-field antennas integrated with scanning probes for THz to visible microscopy: scale modeling and limitations on performance", *IEEE transactions on antennas and propagation*, Vol. 50, No.5, pp.670-675, May 2002.

[27] C. Böhm, M.Otterbeck, S.Lipp, L.Frey, R.Reuter, A.Leyk, W.Mertin, F.J.Tegude, and E.Kubalek, "Design and characterization of integrated probes for millimeter wave applications in scanning probe microscopy," *IEEE MTT-S Digest*, Vol.3, pp.1529-1532, June 1996.

[28] Soonil Hong, Ken Lee and J.C.Bravman, "Design and fabrication of a monolithic high-density probe card for high frequency on wafer testing," *Electron Devices Meeting, 1989. Technical Digest. International*, pp. 289 –292, 3-6 Dec. 1989.

[29] T.Hantschel, E.M.Chow, D. Rudolph, and D.K. Fork, "Stressed metal probes for atomic force microscopy," *Appl. Phys. Lett.*, Vol. 81, No. 16, pp.3070-3072, Oct 2002.

[30] D.L.Smith, D. K. Fork, R.L. Thornton, A.S. Alimonda, C.L. Chua, C. Dunnrowicz, and J.Ho, "Flip-chip bonding on 6-um pitch using thin-film microspring technology," *1998 Proceedings of the 48th Electronic Components and Technology Conference*, 1998 May 25-28; Seattle, WA. New York: IEEE, pp.325-329, 1998.

[31] F.Keilmann, D.W.van der Weide, T.Eickelkamp, r.Merz, and D.Stockle. Opt.Commun. "Extreme sub-wavelength resolution with a scanning radio-frequency transmission microscope," Vol.129, pp.15-18, 1996.

[32] T.Kitazawa and T.Itoh, "Propagation characteristics of coplanar-type transmission lines with tossy media," *IEEE Trans. Microwave Theory Tech.*, Vol.39, No.10, pp.1694-1700, Oct.1991.

[33] R.W.Jackson, "Coplanar waveguide vs. microstrip for millimetre wave integrated circuits," *1986 IEEE-S international microwave symposium digest*, Vol.34, No.12, pp.699-702, Dec. 1986.

[34] T.Koryu Ishii, *Handbook of Microwave Technology, Vol.1: Components and Device*, Academic press, 1995.

[35] F.T.Ulaby, *Applied Electromagnetics*, Prentice Hall, 1997.

[36] G.E.Ponchak, A.N.Downey, and L.P.B.Katehi, "High frequency interconnects on silicon substrates," *1997 IEEE radio frequency integrated circuits (RFIC) symp.dig.*, Denver, Co. Jun 8-11, pp.101-104, June 1997.

[37] Y.Wu, H.S.Gamble, B.M.Armstrong, V.F.Fusco, and J.A.C.Stewart, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line," *IEEE microwave guided wave lett.*, Vol.9, No.1, pp.10-12, Jan.1999.

[38] G.E.Ponchak and L.P.B.Katehi, "Measured attenuation of coplanar waveguide on CMOS grade silicon substrates with polyimide interface layer," *Electron. Lett.*, Vol. 34, No.13, pp.1327-1329, June 1998.

[39] J.N.Burghartz, D.C.Edelstein, K.A.Jenkins, and Y.h.Kwark, "Sprial inductors and transmission lines on silicon technology using copper-damascene interconnects and low-loss substrate," *IEEE Trans. Microwave Theory Tech.*, Vol. 45, No.10, pp.1961-1968, Oct.1997.

[40] G.T.A.Kovacs, *Micromachined Transducers Sourcebook*, McGraw-Hill, New York, 1998.

[41] S.A.Campbell, *The Science and Engineering of Microelectronic Fabrication*, 2nd ed., Oxford university press, New York, 2001.

[42] M.Madou, *Fundamentals of Microfabrication*, CPC press, 1997.

[43] H.J.De Los Santos, *Introduction to Microelectromechanical Microwave Systems*, Artech House, Boston, 1999.

[44] H.J.De Los Santos, Y.H.Kao, A.L.Kaigoy and E.D.Ditmars, "Microwave and mechanical considerations in design of MEMS switches for aerospace applications," *IEEE Aerospace conference*, Snowmass at Aspen, Co, USA, 1-8 Feb. pp.235-253, 1997.

[45] D.J. Thomson, "Experimental Methods for Electronic Materials," Lecture Notes, University of Manitoba, 2001.

[46] C. A. J. Putman, B. G. De Grooth, N. F. Van Hulst, and J. Greve, A detailed analysis of the optical beam deflection technique for use in atomic force microscopy, *Journal of Applied Physics*, vol. 72, No. 1, pp.6-12, 1992.

[47] Marco Tortonese, "Cantilevers and tips for atomic force microscopy," *IEEE engineering in medicine and biology*, Vol.16, No.2, pp.28-33, March 1997.

[48] G.Ghione and C.Naldi, "Coplanar waveguide for MMIC applications: effect of upper shielding, conductor backing, finite-extent ground planes, and line-to-line coupling," *IEEE Trans. Microwave Theory Tech.*, Vol.35, No.3, pp.260-267, March 1987.

[49] G.Ghione and C.Naldi, "Analytical formulas for coplanar lines in hybrid and monolithic MICs," *Electron. Lett.*, Vol. 20, No.4, pp.179-181, Feb.1984.

[50] M.E.Davis, E.W.Williams, and A.C.Celestini, " Finite-boundary corrections to the coplanar waveguide analysis," *IEEE Trans. Microwave Theory Tech.*, Vol.35, No.3, pp.260-267, March 1987.

[51] S.S.Bedair and I.Wolff, "Fast, accurate and simple approximate analysis formulas for calculating the parameters of supported coplanar waveguide for (M)MIC's," *IEEE Trans. Microwave Theory Tech.*,Vol.40, No.1, pp.41-48, Jan.1992.

[52] V.Milanovic, M.Ozgur, D.C.DeGroot, J.A.Jargon, M.Gaitan, and M.E.Zaghoul, "Characterization of broad-band transmission for coplanar waveguides on CMOS silicon substrates," *IEEE Trans. Microwave Theory Tech.*, Vol.46, No.5, pp.632-640, May 1998.

[53] T.Pfeifer, H.-M.Heiliger, E.Stein von kamienski, H.G.Roskos, and H.Kurz, "Charge accumulation effects and microwave absorption of coplanar waveguides fabricated on high-resistivity Si with SiO_2 insulation layer," *Appl.Phys.Lett.*, Vol.67, No.18, pp.2624-2626, Oct.1995.

[54] R.E.Collin, *Foundations for Microwave Engineering*, 2nd ed., New York: McGraw-Hill, pp.178-179, 1992.

[55] G.E.Ponchak, M.Matloubian, and L.P.B.Katehi, "A measurement based design equation for the attenuation of MMIC-compatible coplanar waveguides," *IEEE Trans. Microwave Theory Tech.*, Vol.47, No.2, pp.241-243, Feb.1999.

[56] W.Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor-loss effects," *IEEE Trans. Microwave Theory Tech.*, Vol.41, No.1, pp.45-52, Jan.1993.

[57] C.L.Howay and E.F.Kuester, "Edge shape effects and quasiclosed form expressions for the conductor loss in microstrip," *Radio science*, Vol.29, No.3, pp.539-559, May-June 1994.

[58] M.E.Davis, E.W.Willians, and A.C.Celestini, "Finite-boundary corrections to the coplanar waveguide analysis", *IEEE Trans. Microwave Theory Tech.*, Vol. 21, No.9, pp.594-596, Sept. 1973.

[59] S.-J.Yoon, S.-H. Jeong, J.-G. Yook, Y.-J. Kim, S.-G. Lee, O.-K. Seo, K.-S. Lim, D.-S.Kim, "A novel CPW structure for high-speed interconnects", *Microwave Symposium Digest, 2001 IEEE MTT-S International* , Vol. 2, pp. 771 -774, 20-25 May 2001.

[60] D. L. Smith, and A. S. Alimonda, "A new flip-chip technology for high-density packaging," *Proc 46th Electronic Components and Technology Conf.* Orlando, Florida, pp. 1069-1073, May 1996.

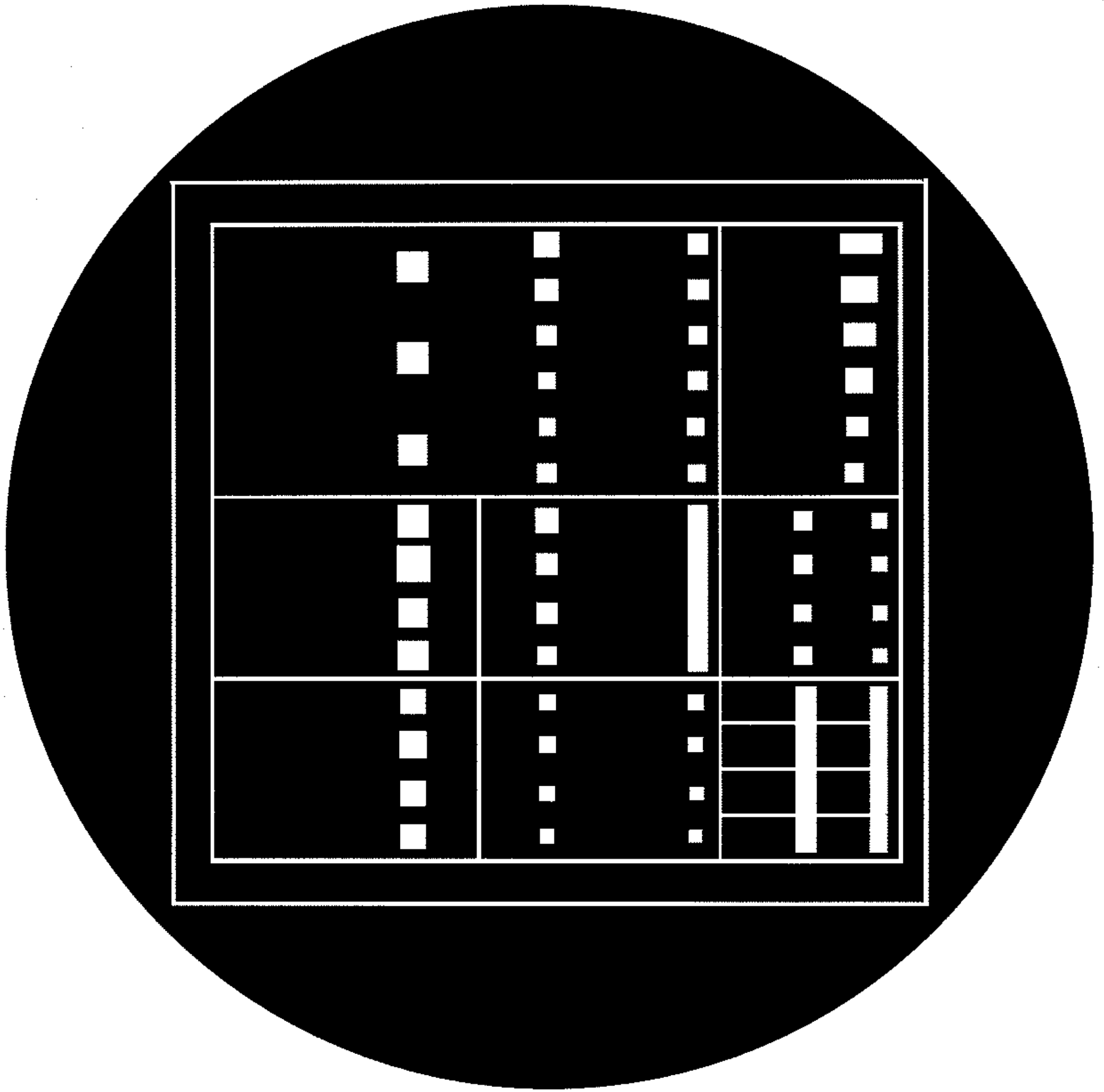
[61] Enrico Volterra, and E.C.Zachmanoglou, *Dynamics of Vibrations*, Charles E.Merrill Books, Inc., Columbus, Ohio. pp. 319-320, 1965.

[62] S.S.Gevorgian, "Basic characteristics of two layered substrate coplanar waveguides," *Electronics Letters*, Vol.30, No. 15, pp. 1236-1237, July 1994.

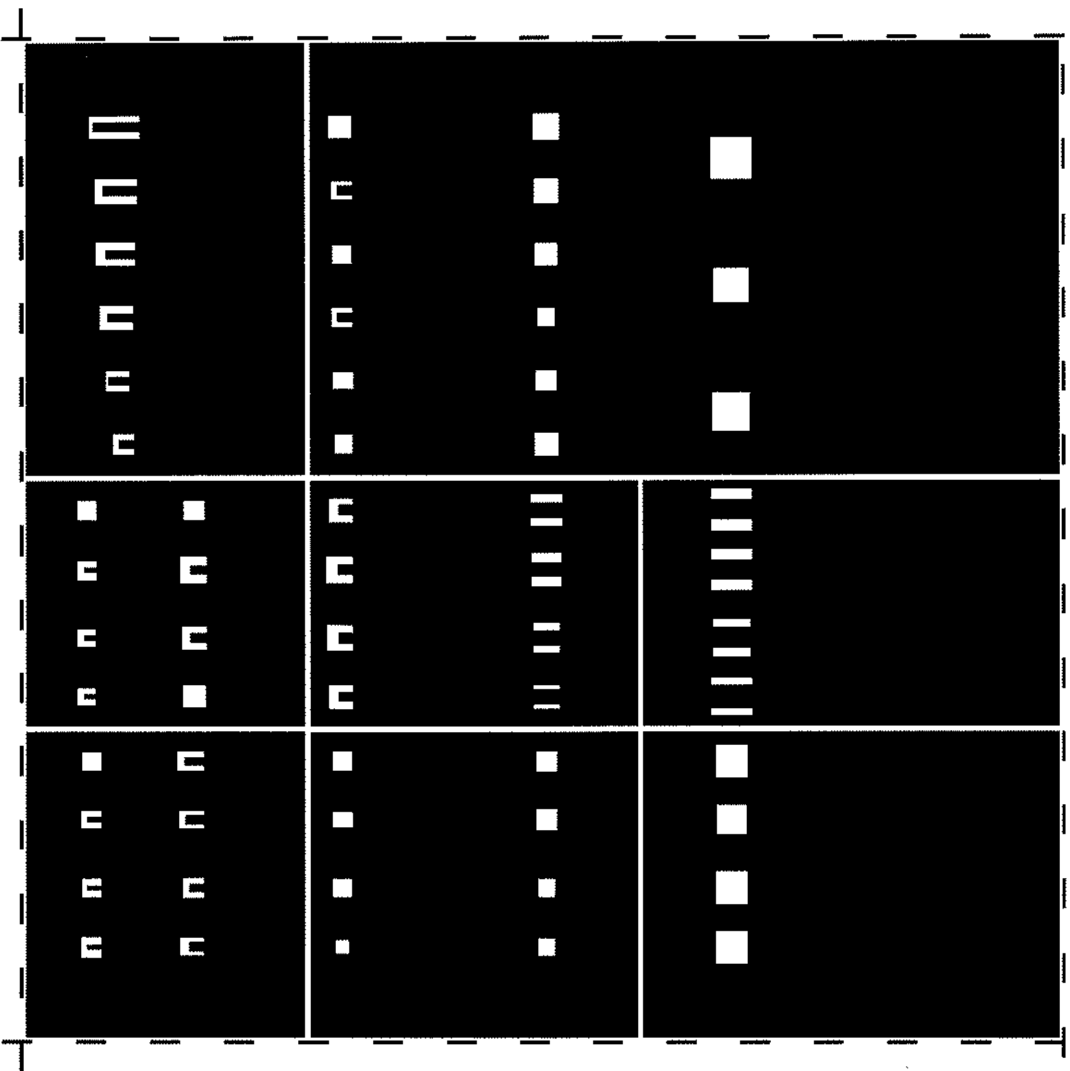
[63] E.Bridges, "24.439 Microwave engineering," course notes, 2003.

[64] Mike Golio, *The RF and Microwave Handbook*, CRC press, pp. 4-17 to 4-23, 2001.

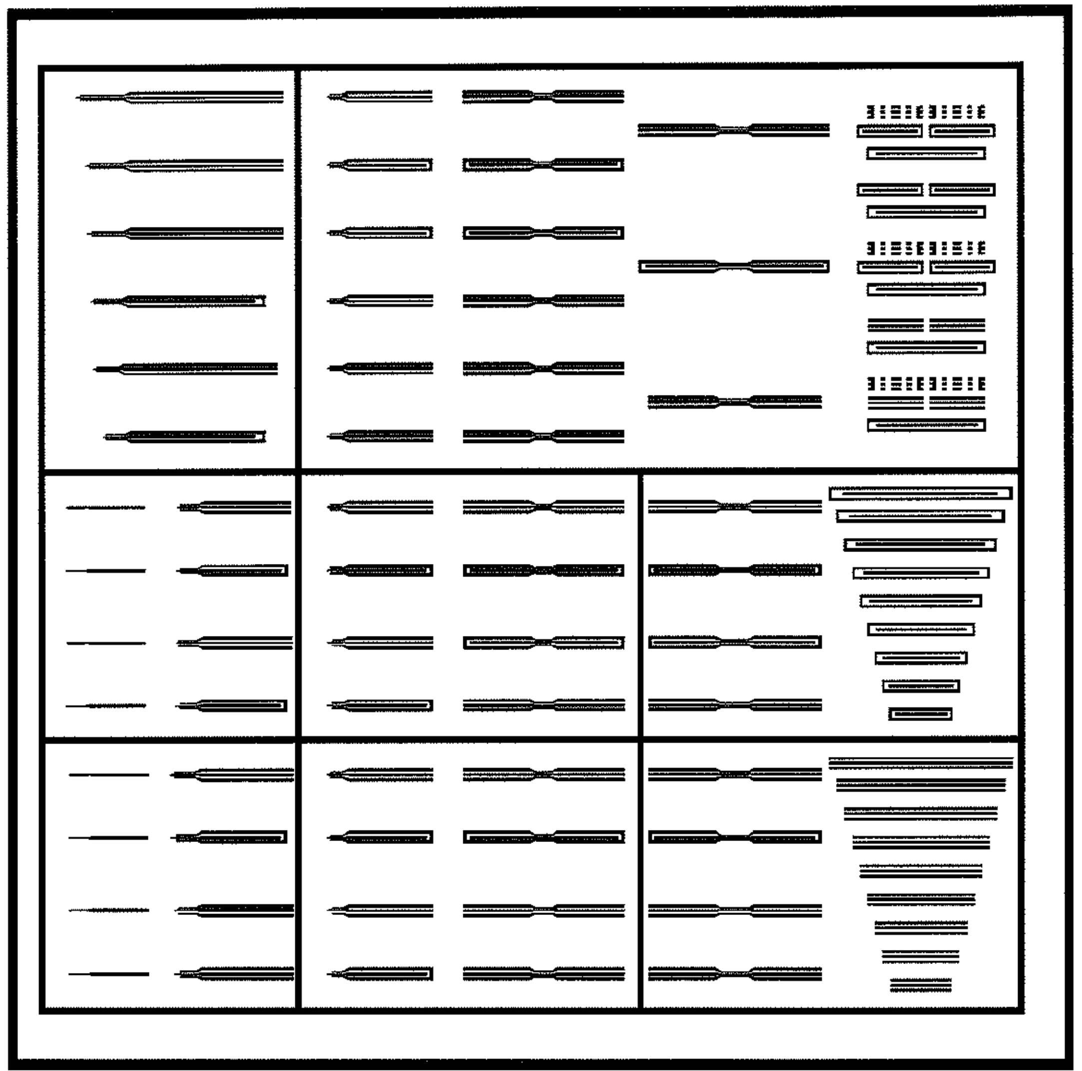
Appendix A: Masks for MEMS CPW cantilevers



Backside mask 1 (glass for 2 inch diameter Si wafer)



Frontside mask 2 (36x34.8 mm glass)



Frontside mask 3 (35×33.6 mm glass)