A Phase-Locked FM Demodulator for an Unconventional Current Transducer

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A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

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ABSTRACT

An unconventional current transducer (CT) based on a frequency modulated microwave oscillator generated the need for a very wide deviation FM demodulator possessing good linearity and frequency response. To satisfy this need, a phase-locked loop demodulator (PLD) was built around a phase frequency detector (PFD). The applicability of this demodulator for use in a current measuring system was evaluated through laboratory measurements and computer modeling of the loop in both the locked and unlocked mode of operation. The demodulator was found to meet the requirements of accuracy for revenue metering and it has the low frequency response and sensitivity for the measurement of geomagnetically induced currents (GIC). Limitations of the voltage controlled oscillator (VCO) in the loop limited its usefulness for protection service, however, the inevitable development of a frequency agile, ultra-linear VCO technology will enable improvements towards satisfying the demands of this application. The phase frequency detector was demonstrated to be an ideal choice as a phase detection device for this demodulator. As well, the computer loop simulator for design evaluation proved to be a useful analytical tool.

Keywords: phase frequency detector (PFD), phase-locked demodulator (PLD), FM demodulator, computer modeling, phase locked loop, acquisition, geomagnetically induced currents (GIC), unconventional current transducer, wide deviation.

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Chapter I

INTRODUCTION

1.1 UNCONVENTIONAL CURRENT TRANSDUCERS

Conventional methods of measuring current on high tension AC transmission lines employ an instrument grade iron core transformer (CT), suitably isolated from ground. These devices until now have adequately performed the tasks required of them. Although they suffer from limited frequency response and impaired accuracy during the presence of high frequency, high amplitude currents caused by major system disturbances, they have a long service life and are accurate under normal conditions [1],[2]. However with the higher transmission voltages in use today and even higher ones planned for the future, the conventional CT faces some difficulties, notably:

1. greatly increased expense for the bushing which is the primary isolation of the CT (these make up the main cost of the CT),
2. the CT becomes quite large resulting in a (mechanically) more complex installation,
3. the larger dimensions of the CT result in higher reactance to resistance ratios that further increase the expense required to achieve acceptable high frequency performance [4],

4. recently developed high speed protection schemes (necessary with the increased system voltages) put greater demand on CT designers for improved frequency response and fidelity of the waveform (which is in opposition to the previous point) and
5. normal CTs are incapable of measuring geomagnetically induced line currents and may be adversely affected by them.

The above requirements result in a highly expensive conventional CT and hence many unconventional current transducer designs have been proposed, developed and are presently undergoing field trials. These unconventional CTs (hereafter CT will stand for 'current transducer') usually consist of a transducer for monitoring current mounted in close proximity to the line (the high potential unit, HPU) together with some apparatus for transmitting this information to a unit on the ground (ground potential unit, GPU) for further processing. Among the possible advantages offered by these unconventional CTs over the conventional ones are: reduced cost especially above 230 kV; greater low and high frequency response; immunity to saturation by high frequency and direct currents; and reduced size resulting in easier installation and repair.

A CT system pioneered at the University of Manitoba exploits the property of ferrite resonance at RF and microwave frequencies. When the ferrite is immersed in a magnetic

field, the frequency of this resonance dependends in a highly linear fashion on the strength of the field. A Gallium Arsenide doped Yttrium Iron Garnet (YIG) crystal can serve as such a resonator in the frequency range of interest [3]. When a YIG resonator is installed in the feedback loop of an oscillator, the frequency of the output is linearly dependent on the magnetic field surrounding it. An oscillator of this type will be frequency modulated (FM) by the magnetic field produced by the current through a conductor in a transmission system if the resonator is placed in proximity of the conductor. If the oscillator output is fed to a broadband antenna which radiates a signal via a free space path to ground, this device than forms the HPU of an unconventional CT. An FM receiver forming part of the GPU demodulates the signal and processes it as required. Alternatively, the free space path could be replaced by a dielectric waveguide system mounted within a small bushing [10]. This necessitates selecting the transmitter's operating frequency sufficiently high to make the size of the waveguide reasonably small. The YIG oscillator frequency deviation produced by a given line current amplitude is dependent on the distance separating the YIG crystal from the current carrying conductor while its center frequency is maintained by a set of permanent bias magnets embedded in the oscillator casing. The University of Manitoba CTs operate with an oscillator center frequency of about 1.5 GHz and a total peak to peak frequency deviation of 300 MHz (center

frequency ±150 MHz) at the maximum expected line current. Three of these CTs (specifically referred to as AC-ECT for AC electromagnetic current transducer) were installed at three different substations for evaluation. The earliest of these was installed at a Manitoba Hydro site in August, 1975 [8]. The transmitter and receiver of this initial unit was designed to make the instrument useful for the purposes of protection and transient analysis. This was required to faithfully reproduce the waveform of a 20 per unit (pu) line current with good high frequency response but with lower constraints on accuracy. The two other units were designed for maximum sensitivity [7] (hence lower dynamic range) and good low frequency response in order to measure currents induced by a geomagnetic process. Long transmission lines associated with high voltage technology are susceptible to and hence generate the need for monitoring geomagnetically induced currents which are low frequency (periods greater than 10 seconds), low amplitude (typically under 100 amps) currents superimposed on the normal 60 Hz line current.

1.2 CT DISCRIMINATORS

All three of these CT systems made use of a delay line discriminator as a demodulator for the receiver in the GPU [9]. The delay line discriminator performed well in terms of its linearity (less than 0.5% maximum deviation from linearity at frequency deviations of less than 100 MHz), its frequency response and its start up time (demodulation commenced with-

in an extremely short span of time after initial reception of an input signal). In addition, the discriminator reliability is high owing to the fact that it primarily consists of passive components. Its dynamic range was reported to be poor in the units tested (less than 100:1). However there are both theoretical and practical tradeoffs between linearity and dynamic range and the option of maximizing the latter was not fully exercised. Work has yet to be carried out in quantifying the range achievable with this type of discriminator. Some of the shortcomings of the delay line discriminator are as follows.

1. The center frequency of the discriminator is fixed during its manufacture and cannot be electrically altered while operating. This limitation prohibits the electronic tracking of the transmitter's center frequency to accommodate drift due to temperature fluctuations, aging and initial transmitter misadjustment. This results in a shift of the operating point within the range of the discriminator and its subsequent dc offset and change in linearity.
2. The discriminator has poor rejection of amplitude modulation appearing at its input (caused by changes in path loss and transmitter power output with frequency). This requires the inclusion of a high performance microwave AGC (automatic gain control) ahead of the discriminator to level out the offending am-

plitude variations. Such an AGC is expensive and difficult to adjust.

3. The discriminator exhibits a high sensitivity to uncontrolled impedance variations associated with the components used in the construction of the device. These components must be hand picked to assure that the expected performance goals for linearity and dynamic range are realized.

Motivated by the above points, this thesis investigates the application of a phase locked loop demodulator (PLD) as an alternative to the delay line type employed in the existing ECTs. Existing technology will be exploited to construct a working demodulator and some key design tools applicable to this type of loop shall be assembled. This demodulator will be evaluated in terms of its suitability for metering, protection and its ability to monitor geomagnetically induced currents. The demands placed on the demodulator by these three classes of measurement is discussed with more detail in Appendix A.

The demodulator should be able to accept a peak to peak deviation of at least 200 MHz preferably as high as 400 MHz in order to fully realize the dynamic range inherent in the transmitter. This is particularly important in protection applications where the required range may exceed 1000:1 (60 dB). The phase delay for protection application should be less than 50 μs although a composite error in amplitude as

high as 5% is allowed (appendix A). The same device may also be employed for metering provided the linearity of the current measurement (at the fundamental frequency) is of metering grade in the range of 0.1 to 1.2 per unit (peak to peak deviations of 1.5 MHz and 18 MHz respectively).

Except for a small temperature dependence of the transmitter's tuning sensitivity [8] which could be compensated for in post detection signal processing, the transmitter seems to possess the qualifications necessary to meet the requirements of the above applications, even with metering and protection carried out by one unit. Assuming this to be the case, the task will be to ascertain whether or not the phase locked demodulator can complement the transmitter in a complete measuring system. Critical components will be identified and the limitations they impose on the system performance will be spotlighted. An attempt will be made to specify these components as required for the successful design of a demodulator.

A glossary of notation is included in Appendix D for the reader's convinience.

Chapter II

THE PHASE LOCKED DISCRIMINATOR- DESIGN PRINCIPLES

2.1 INTRODUCTION

This chapter provides the theoretical background and design techniques for a phase locked FM demodulator, the implementation of which shall be described in the following chapter. The phase locked demodulator will exhibit two distinct modes of operation ; the locked or linear mode where FM demodulation is taking place and the unlocked (non-linear) mode where the demodulator is either searching for or in the process of locking onto an FM signal. The former case has been dealt with analytically by many investigators. The next section of this chapter will bring together many of these ideas and design tools which are pertinent to the process of FM demodulation. This type of FM demodulator will prove ideally suited for application of a specific phase detection device namely the phase frequency detector. Techniques for extensively and accurately analyzing the operation of an FM demodulator built around this type of phase detector, particularly in the unlocked mode have not yet been published. The fourth section of this chapter will provide a detailed description of this phase detector (for readers not familiar with its operation) while the remainder of the chapter will

develop analytical and design tools that apply specifically to this detector-demodulator combination. The effectiveness of these tools in describing the operation of the demodulator in both the locked and unlocked mode of operation shall be demonstrated. Once the loop operation is clearly understood and hence accurately predictable, a design can be implemented with a high degree of confidence in its ability to perform the required tasks.

2.2 PHASE LOCK FM DEMODULATION

The concept of a phase locked[1] loop is well developed and treated extensively in the literature, hence any detailed theoretical treatment of the subject will be left to any one of the readily available references. Fundamental design equations and terminology relating to the loop employed in the service of FM demodulation will now be presented. Most of the material in this section applies to a very basic second order phase locked loop but serves as a starting point for the development of somewhat more sophisticated designs one of which is studied extensively in this thesis.

Figure 2.1 depicts the phase locked demodulator (hereafter referred to as PLD) in its most basic form. The input signal applied to the loop is a sinusoid with instantaneous frequency ω_i , that is

[1] The device has been referred to in the literature as any one of phase locked, phase locking and phase lock loop creating a curiously large amount of concern on the part of technical editors [11: 2221-2222]

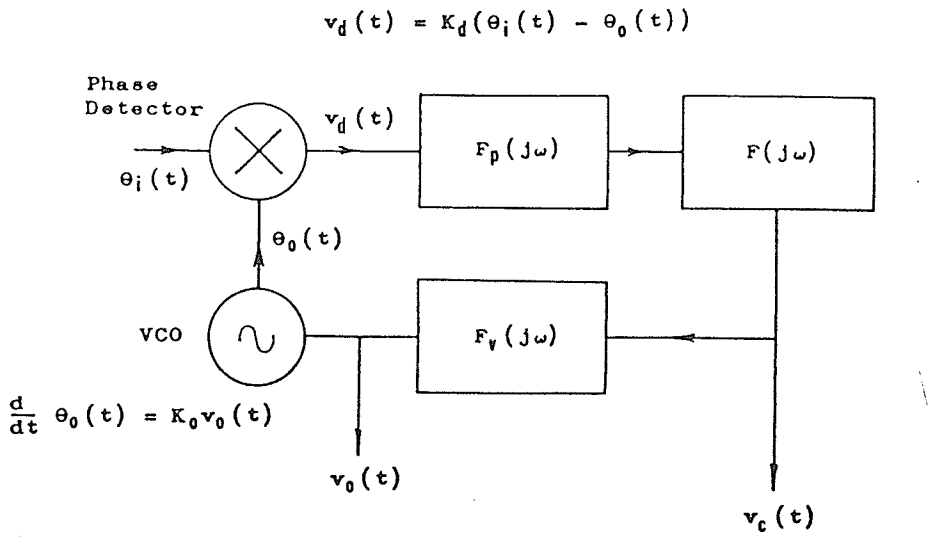


Figure 2.1: Basic Phase Locked Demodulator

$$\omega_i = \omega_c + \frac{d}{dt}\theta_i(t) \qquad \ldots(2.1)$$

where ω_c is the center frequency of the demodulator (i.e. the frequency of the input signal which results in a zero output of the demodulator) and $\theta_i(t)$ is the modulated component of the phase. The voltage controlled oscillator (VCO) provides an output with instantaneous frequency ω_0 determined by the control voltage $v_0(t)$. The output of the phase detector, v_d varies in proportion to the difference between the phase of the voltage controlled oscillator and that of the incoming signal. When in the locked condition, the feedback of the loop strives to minimize this difference by adjusting the VCO phase through small changes in the VCO frequency. Since the incoming frequency is a function of the modulation it is expected that the VCO frequency and hence the VCO control voltage will represent this modula-

tion. The average frequency of the VCO must be equal to that of the incoming signal if the loop is in the locked condition as described above. That is to say that for a period of consideration there must be a corresponding cycle of VCO output for every cycle of incoming signal. This is not true once lock is lost and the loop is attempting (or at least should be) to acquire the signal. For most loop designs the locked and unlocked conditions must be dealt with separately both from analytical and design points of view.

Once lock has been achieved and the transients have died away a straight forward, linear servo loop analysis may be employed. A very thorough treatment of this approach has been undertaken by Blanchard [12] et al and some of the resulting equations pertinent to the development of the system in this thesis will now be presented.

The phase detector output voltage is a function of the the phase difference between the input signal and VCO output. In practical loops this relation is approximately linear, thus

$$v_d(t) = K_d(\theta_i(t) - \theta_0(t)) \qquad \ldots(2.2)$$

where K_d is the phase detector gain in units of Volts/radian. The phase error may be defined as

$$\theta_e(t) \triangleq \theta_i(t) - \theta_0(t) \qquad \ldots(2.3)$$

The output frequency of the VCO is proportional to the control voltage, $v_0(t)$, which is to say,

$$\frac{d}{dt}\theta_0(t)=K_0 v_0(t) \qquad \ldots(2.4)$$

where K_0 is the VCO gain constant (usually in units of radians/Volt-sec). The loop filter transfer function F(jw/w) determines dynamic properties of the PLD such as transient response and tracking error. The transfer functions $F_p(j\omega)$ and $F_v(j\omega)$ represent parasitic elements in the open loop transfer function. These are respectively, the transfer function of the phase detector post filter (required in all practical phase detectors thus far developed to remove unwanted products of the detection process) and the inherent VCO response to the control signal (ultimately some sort of low pass filter). The VCO response is not usually under the control of the loop designer so that in most cases the loop filter F(jw/w) is chosen such that its effect on the loop performance overrides that of the VCO's response. If this is the case, $v_c(t)$ is proportional to $v_0(t)$ in Fig. 1. The response of the VCO will impose constraints on the design of the loop filter, particularly as to the upper frequency limit (based on considerations of stability [12],[13]). The designer has more control over the post detection filter and this is usually selected to have an upper frequency cut off several times that of the loop filter (again based on stability considerations).

A set of three basic loop equations that describe the closed loop (as depicted in Fig. 2.1) will now be developed. The quantities of ultimate interest are the VCO control voltage, $v_0(t)$ and phase error (2.3).

Begin by expressing (2.2) and (2.4) in the frequency domain[2] as follows

$$V_d(j\omega)=K_d(\Theta_i(j\omega)-\Theta_0(j\omega)) \qquad ...(2.5)$$

and

$$j\omega\Theta_0(j\omega)=K_0 V_0(j\omega) \qquad ...(2.6)$$

The phase detector output and VCO control voltage are related by the loop filter function as

$$V_0(j\omega)=F(j\omega)V_d(j\omega) \qquad ...(2.7)$$

Appropriate substitutions involving (2.5),(2.6) and (2.7) along with the definition of the linear closed loop transfer function $H(j\omega)$, results in

$$H(j\omega)=\frac{\Theta_0(j\omega)}{\Theta_i(j\omega)}=\frac{K_0 K_d F(j\omega)}{j\omega+K_0 K_d F(j\omega)} \qquad ...(2.8)$$

which relates the VCO phase to the input phase in terms of $H(j\omega)$ and,

$$V_0(j\omega)=\frac{j\omega}{K_0}\Theta_i(j\omega)H(j\omega) \qquad ...(2.9)$$

---

[2] An attempt will be made to consistently represent frequency domain quantities by upper case variable names and time domain quantities with lower case ones throughout this thesis.

The phase error may be expressed in terms of $H(j\omega)$ by applying the definition of phase error, (2.3) to (2.8). In the frequency domain, phase error is then

$$\Theta_e(j\omega)=(1-H(j\omega))\Theta_i(j\omega)=\frac{j\omega\Theta_i(j\omega)}{j\omega+K_0K_dF(j\omega)} \qquad ...(2.10)$$

The last three expressions comprise the set of basic loop equations on which the remaining design and analysis of the PLD is based. The choice of the loop filter function, $F(j\omega)$ will now be made.

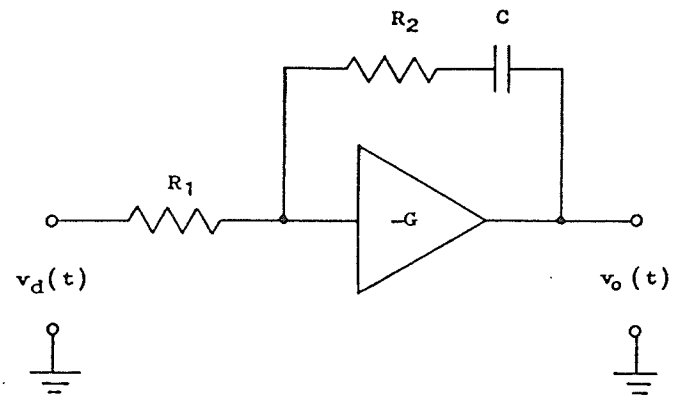


Figure 2.2: Circuit of the loop filter.

The most common and well understood loop filter functions in modern implementations is that of the form

$$F(j\omega)=\frac{-(1+j\omega R_2C)}{j\omega R_1C} \qquad ...(2.11)$$

and is realized by the circuit depicted in Figure 2.2. If the gain of the amplifier is very high it does not appear in the expression for the loop response. The sign of the

function in eqn. (2.11) is arbitrary in that its effect may be reversed by a complementary change in the sign of either the VCO or phase detector gain constants. The loop will function correctly providing the VCO phase moves in the direction appropriate to minimizing the phase error.

Substitution of (2.11) into (2.8) and (2.10) results in

$$H(j\omega) = \frac{\omega_n^2 + j2\zeta\omega_n\omega}{\omega_n^2 - \omega^2 + j2\zeta\omega_n\omega} \qquad \ldots(2.12)$$

and

$$1-H(j\omega) = \frac{-\omega^2}{\omega_n^2 - \omega^2 + 2j\omega_n\omega} \qquad \ldots(2.13)$$

where the parameter ω_n is the natural or loop frequency and ζ is the damping factor [13,14]. These parameters may be expressed in terms of the loop filter circuit elements as

$$\omega_n^2 = \frac{K_0 K_d}{R_1 C} \qquad \ldots(2.14\ (a))$$

and

$$2\zeta\omega_n = \frac{K_0 K_d R_2 C}{R_1 C} \qquad \ldots(2.14\ (b))$$

The underlying intent on developing this type of PLD is to enable tracking of a frequency modulated signal where the most significant component of the modulation is a sinusoid which is perhaps accompanied by several harmonically related terms but of much lower amplitudes. Therefore, it is reasonable to study the response of the loop to such a signal and relate this response to the loop parameters.

The relationship between the line current (the input to a current measuring system) and the VCO control voltage (considered to be the output of the PLD) shall now be developed in terms of the loop transfer function and loop parameters discussed above. Consider a current flowing past the YIG oscillator in the HPU of the form

$$i_L(t)=\mathrm{SIN}(\Omega t+\phi_i) \qquad \ldots(2.15)$$

where Ω is the line frequency and ϕ_i is an arbitrary phase constant. This current frequency modulates the instantaneous frequency of the oscillator about a center frequency ω_c. The transmitter output becomes the input to the PLD. Hence, the instantaneous input frequency to the loop is

$$\omega_i(t)=\Delta\omega_i \mathrm{SIN}(\Omega t+\phi_i) \qquad \ldots(2.16)$$

The quantity $\Delta\omega_i$ is defined as the peak frequency deviation (or simply frequency deviation) and is the maximum frequency displacement from ω_c. The center frequency of the transmitter and PLD as described earlier are assumed to be equal. The choice of ω_c is arbitrary at this point and for simplicity is set to zero, thus it does not appear in (2.16). Equating (2.16) and (2.1) yields

$$\frac{d}{dt}\theta_i(t)=\Delta\omega_i \mathrm{SIN}(\Omega t+\phi_i) \qquad \ldots(2.17)$$

In the frequency domain (2.17) becomes

$$\Theta_i(j\Omega)=\frac{\Delta\omega_i}{j\Omega} e^{j\phi_i} \qquad \ldots(2.18)$$

Substituting (2.18) into (2.9) results in an expression relating the output voltage of the PLD, $V_0(j\Omega)$ as a function of modulation frequency to the deviation (hence current magnitude) and input phase constant (current phase). Thus

$$\frac{\Delta\omega_0(j\Omega)}{\Delta\omega_i} e^{j(\phi_0-\phi_i)} = H(j\Omega) \qquad ...(2.19)$$

A useful definition is the demodulator gain, G_D which (in a linear system) relates the magnitude of the current $\Delta\omega_i$ to the magnitude of the output voltage when $H(j\omega)$ is at unity (its low frequency or dc value). Rewriting (2.19) with this new parameter gives

$$V_0(j\Omega)=\Delta\omega_i G_D e^{j\phi_i} H(j\omega) \qquad ...(2.20)$$

where $G_D=K_0^{-1}$. Plots of $H(j\Omega)$ for a specific loop design appear in a later chapter although generalized plots for a variety of loop types may be found in Blanchard [12]. These plots are unity at dc and low frequencies, then peak when $\Omega=\omega_n$ and roll off at 6 dB per octave with increasing frequency thereafter. The transfer function $H(j\omega)$ is determines the frequency response of the demodulator. For low modulation frequencies ($\Omega<0.1\omega_n$ or depending on accuracy requirements),

$$V_0(j\Omega)=\Delta\omega_i G_D \qquad ...(2.21)$$

The peak frequency deviation of the VCO, $\Delta\omega_0$ is defined in a manner similar to that of the input signal $\Delta\omega_i$ except

that it becomes a function of the modulating frequency Ω. An Equation relating these two quantities to the modulating frequency is found by substituting (2.6) into (2.9). Thus,

$$\frac{\Delta\omega_0(j\Omega)}{\Delta\omega_i} e^{j(\phi_0 - \phi_i)} = H(j\Omega) \qquad \ldots(2.22)$$

The above relation is useful in determining the maximum frequency swing that the VCO is required to provide in order for the loop to remain locked. In addition, the maximum difference between the instantaneous VCO and input frequencies will be given by $(\Delta\omega_0 - \Delta\omega_i \cos(|\phi_0 - \phi_i|)$ which will indicate a 'worst case' bandwidth requirement for an IF (intermediate frequency) stage should this be incorporated into the PLD (chapter 3).

Substituting (2.12),(2.13) into (2.22) the peak deviation ratio, $\Delta\omega_0 / \Delta\omega_i$ may be expressed (magnitude only) by

$$\frac{\Delta\omega_0}{\Delta\omega_i} = \sqrt{\frac{\omega_n^4 + 4\zeta^2\omega_n^2\Omega^2}{(\omega_n^2 - \Omega^2)^2 + 4\zeta^2\omega_n^2\Omega^2}} \qquad \ldots(2.23\ (a))$$

and phase by

$$\phi_0 = \phi_i + \text{TAN}^{-1}\left[\frac{2\zeta\Omega}{\omega_n}\right] - \text{TAN}^{-1}\left[\frac{2\zeta\Omega\omega_n}{(\omega_n^2 - \Omega^2)}\right] \qquad ..(2.23\ (b))$$

The loop phase error (2.3) will, like the VCO and input signal phase be sinusoidal with respect to time. The peak value of the phase error function will depend on the input frequency deviation and modulating frequency. The phase error function can be expressed in the frequency domain by substituting (2.18) into (2.10). Thus

$$\Theta_e(j\Omega)=\frac{\Delta\omega_i}{j\Omega}\ e^{j\phi_i}(1-H(j\Omega)) \qquad ...(2.24)$$

The phase error may be expressed in the time domain as $\theta_e(t)=\Delta\phi\cos(\Omega t+\phi_e)$ where the peak phase error is given by

$$\Delta\phi=\frac{\Delta\omega_i}{\Omega}\,|1-H(j\Omega)| \qquad ...(2.25)$$

and the phase error function phase is

$$\phi_e=\phi_i+\mathrm{TAN}^{-1}[1-H(j\Omega)] \qquad ...(2.26)$$

Substitution of (2.12) and (2.13) into (2.26) results in

$$\Delta\phi=\frac{\Delta\omega_i\,\Omega}{\sqrt{(\omega_n^2-\Omega^2)^2+4\zeta^2\omega_n^2\Omega^2}} \qquad ...(2.27\ (a))$$

and

$$\phi_e=\phi_i+\pi-\mathrm{TAN}^{-1}\left[\frac{2\zeta\Omega\omega_n}{\omega_n^2-\Omega^2}\right] \qquad ...(2.27\ (b))$$

Equation 2.27 (a) is primarily used to determine the dynamic range required by the phase detector in order to accommodate the modulation. When the condition $\Omega=\omega_n$ holds, (2.27 (a)) yields the maximum peak phase error for a given input signal frequency deviation. If $\Delta\phi_m$ is defined to be the maximum phase error that can be accepted by the phase detector (and still have it operate as a phase detector) then the maximum peak deviation $\Delta\omega_i$ is determined by substituting $\Omega=\omega_n$ for (2.27 (a)) and solving for $\Delta\omega_{i_{max}}$. Hence,

$$\Delta\omega_{i_{max}}=\Delta\phi_m\,2\zeta\omega_n \qquad ...(2.28)$$

Maximizing the loop frequency is seen to be advantageous as it increases the allowable deviation and therefore the amplitude of the current. A means of measuring the loop frequency is suggested as an excitation of the loop at this frequency produces maximum phase error which is a quantity that may be readily measured in many types of phase detectors.

2.3 PLD TRANSIENT RESPONSE

The time domain response of the PLD to a step change in input phase or frequency is an alternative method of specifying the loop's performance as opposed to the steady state frequency response method discussed in the last section. Percentage overshoot and settling time of some loop quantity, such as the phase error obtained either analytically or experimentally, can provide a measure of how closely the design meets the desired goals. Care must be taken during the testing procedure to assure that loop components such as the phase detector and VCO are not overdriven by the test signals as the loop will loose lock with resulting invalidation of the tests. The transient response of a second order loop is dealt with in a multitude of reference texts (examples include Gardner [13], Blanchard [12] and Geiger [14]) and further presentation here is inappropriate. However for completeness, the time domain response equations for phase step, frequency step and frequency ramp inputs applied to the type of loop used in this thesis work is included in Ap-

pendix B. These equations will be referred to in later chapters when comparisons of the response of such loops to the response of implemented designs are made.

2.4 THE PHASE FREQUENCY DETECTOR

The loop theory of the previous section was originally developed on the assumption that the phase detector provides an output voltage that is proportional to the instantaneous difference between the phase of two signals on a continuous basis. The phase detector employed in the PLD actually implemented belongs to a family of phase detectors known as sequential phase detectors; so called, because the phase difference is determined by observing the occurrence of one signal zero crossing with respect to the other. Other attributes of the signal such as amplitude, additive noise and harmonic content do not play a part in the output of the detector. The specific device under consideration is referred to as a phase-frequency detector (PFD), the phase frequency nomenclature arises from the ability of this detector to sense the difference in average frequency between the two signals should such a difference exist. These devices take the form of sequential logic circuits realized with either TTL technology for operating frequencies of a few MHz or ECL technology which may approach 100 MHz. They are produced by several major semiconductor manufacturers, examples types being the Motorola MC4044 and MC4344 and the Fairchild 11c44

The PFD possesses several features which makes it particularly attractive for this application.

1. The PFD has an extended phase range of ±360 degrees resulting from a small amount of memory associated with the logic, and is extremely linear throughout this range.
2. The response of the PFD to phase difference is non-periodic and unique to the range ±360 degrees; the antithesis being the common multiplier type phase detector whose sinusoidal transfer function [13] not only changes sign every 180, degrees but results in an identical response for phase differences occurring in multiples of 360 degrees. This non-periodic feature is useful in a PLD that contains an intermediate frequency (IF) stage as it will prevent the loop from locking onto the image frequency (a process that will be explored in greater detail further on).
3. The PFD's ability to provide frequency information allows for reliable acquisition of the signal should phase lock be lost. This is important if this demodulator is employed in a protection application (as discussed in the introduction) where recovery of the measurement system following signal interruption is mandatory.
4. Since the PFD is itself a logic circuit ,the incorporation of logic type frequency dividers (inexpensive

and readily available) may be employed in the loop to modify the transfer function of loop components.

5. The PFD provides a natural rejection to amplitude modulation appearing on the input signal since it is a transition sensitive device.

The PFD is an edge triggered logic device designed to change state (depending on the logic family) on either the rising or falling edge of two applied signals, commonly labeled as R for reference signal and V for the variable signal. The voltage levels are determined by the logic family to which the device belongs. Although the device operates with discrete logic levels it may still be embedded in an analog phase locked loop providing suitable interfacing to the PFD is in place. Two logical output lines, labeled pump-up (PU) and pump-down (PD) may be used as controls to an on chip charge pump integrator configured to yield a second order loop filter [15],[20],[16]. The charge pump integrator serves to interface the output of the detector to the analog control input of the VCO.

A conceptual demonstration of PFD operation within a PLD now follows. Assume that the PFD is used in the loop of Fig. 2.1 and that the R line of the PFD is the signal input to the PFD while the V line is fed by the VCO. The pump down line becomes active[3] at the occurrence of the active

[3] To avoid the specification of logic levels and voltage levels which are family dependent the term active is employed. The active state is one which effects some action

VCO signal (V signal) edge and remains in this state until the occurrence of the corresponding input signal (R signal) edge. By becoming active, the pump down signal signifies that the VCO signal edge is leading that of the input edge (i.e. the VCO phase leads that of the input signal). Furthermore, the duration of the pump down line activity is a measure of the phase difference between the two signals. If the pump down line decreases the charge on the integrator then the VCO frequency will decrease thereby retarding the phase of the VCO so as to meet the phase of the reference signal. Conversely, the pump up line becomes active when the input edge proceeds that of the VCO, thereby increasing the charge on the integrator and the VCO phase will be advanced towards the input signal phase. With proper design of the loop filter, a stable phase lock will occur.

Figure 2.3 demonstrates the action of the PFD. The active edges of the input and VCO signals are depicted as lines in the R and V tracks, respectively. The VCO frequency is slightly higher than that of the input signal thereby causing the phase error as defined earlier to decrease steadily. In the case of TTL PFDs, a logical zero represents the active state. These lines are shown this way on the same diagram. The pump down line is active in region A as expected, with decreasing duty cycle as the input signal phase catches up to the VCO phase while the pump-up line is active in re-

while the inactive state represents a 'no change' condition.

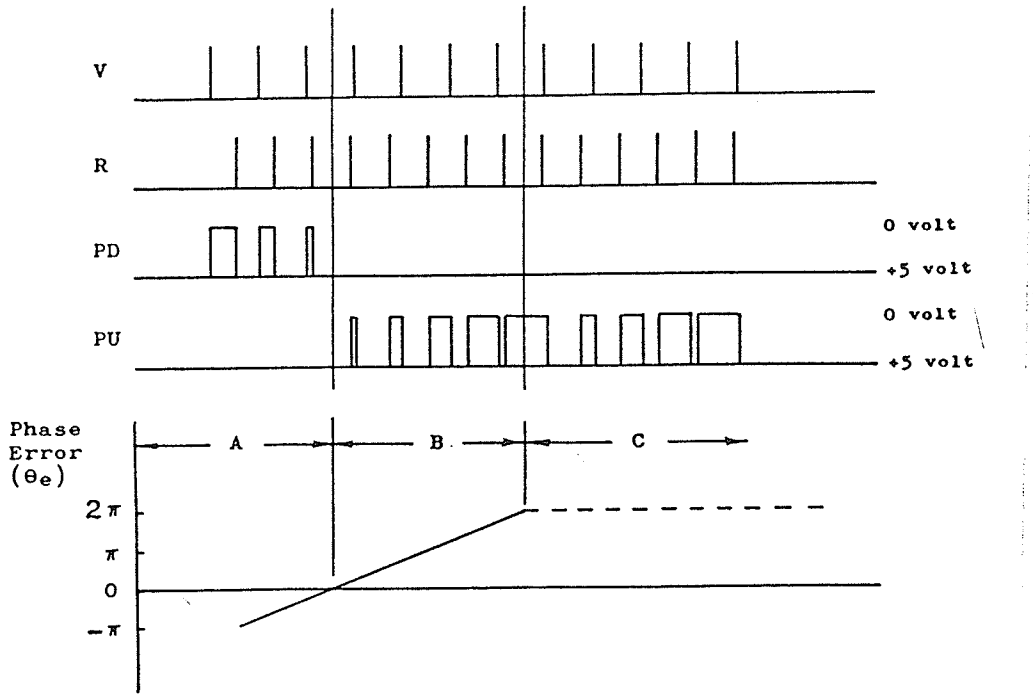


Figure 2.3: Demonstration of PFD operation.

gion B where the VCO phase begins to lag. The phase difference of 360 degrees is exceeded in region C and the pump up line begins to toggle in a seemingly erratic manner. This demonstrates the frequency sensitive behavior of the device since the line that toggles will indicate which frequency is higher and furthermore the duty cycle of this waveform will yield information as to the frequency difference.

The interval over which either the pump-up or pump-down is active shall be designated the pump time and will be represented by t_p. This time is basically the interval between corresponding active edges of the V and R waveforms. In

terms of the R and V phase (θ_R and θ_V respectively) the pump time is approximated by

$$t_p = \frac{|\theta_R - \theta_V|}{\omega_i} \qquad \ldots(2.29)$$

The average output voltage per unit cycle is then

$$v_d = \frac{v_p}{2\pi}(\theta_R - \theta_V) \text{ volts} \qquad \ldots(2.30)$$

where v_p is the magnitude of the pump voltage (output logic level) of the PFD. In order to apply the equations developed earlier to a loop using the PFD, the phase error as defined in (2.3) is applied to (2.29) and (2.30) above. Equation (2.29) becomes

$$t_p = \frac{|\theta_e|}{\omega_i} \qquad \ldots(2.31)$$

and (2.30) becomes

$$v_d = K_d \theta_e \qquad \ldots(2.32\ (a))$$

where

$$K_d = \frac{v_p}{2\pi} \qquad \ldots((b))$$

the phase detector gain as defined earlier and given here in units of volts/radian. The above quantity is valid for a periodic waveform over many cycles. When the conditions for continuous time approximation are met, the gain constant may be treated in the same way as that for a normal analog detector and be substituted in (2.14). The continuous time approximation is met when the input and VCO frequencies are

much larger than the loop frequency ω_n . Gardner [15] suggests that the minimum input frequency applied to the loop should be at least ten times that of the loop frequency if the continuous time approximation is to be applied. Operating with a smaller factor may also introduce potential stability problems.

Difficulties with the PFD arise from the presence of pump pulses at the input of the loop filter, especially when using an integrator built around a high gain amplifier as opposed to a charge pump integrator. These pulses are of high amplitude and may contain frequency components beyond that which the amplifier can deal with effectively. This may cause undesired operation of the device with effects such as offset, pulsewidth saturation and increased noise. Increased pulse feedthrough may occur with the pulses reaching the control input of the VCO. To circumvent these potential difficulties, post detection filters must be carefully placed in the loop to suppress unwanted pulse energy while at the same time assuring that the stability of the loop is not compromised. The need for additional filtering results in a loop which is not of the simple type so far assumed and is difficult to describe analytically.

2.5 ACQUISITION OF LOCK

This section deals with the loop when it is in the unlocked state, a condition that exists when the two applied frequencies to the phase detector are not equal. In this condition the phase detector behavior is not according to (2.2) with the result that the locked state behavior is no longer applicable. A successful unlocked loop design serves to bring the two frequencies close enough together for phase lock to occur. Further discussion of the acquisition problem will only be in the context of the PFD as the loop behavior in the unlocked state is primarily dependent on the type of detector employed.

The PFD behavior in a locked loop condition was found in a manner similar to that used for analyzing conventional types of phase detectors. However, its behavior in the unlocked loop condition requires a completely new approach, to the extent that non linear methods developed for conventional phase detectors cannot be applied. Fortunately the acquisition process of the PFD is much easier to understand than its analog counterparts, being more reliable and consistent in actual operation. A crude analytical model will be presented to aid in predicting the acquisition behavior for this particular loop. The discussion will then lead to a computer simulation of the process which is capable of exact results for any type of loop that employs the PFD.

If the frequency of the V signal applied to the PFD significantly exceeds that of the R signal (for a period of time long enough for the phase difference to exceed 360 degrees) then the pump-down line will toggle with a duty cycle proportional to the frequency difference between the two input signals. The pump-up line on the other hand, continues to remain inactive. Conversely, if frequency of the R signal exceeds that of the V signal, the pump-up line will toggle and the pump-down line will remain inactive. The exact duty cycle as a function of frequency difference may be

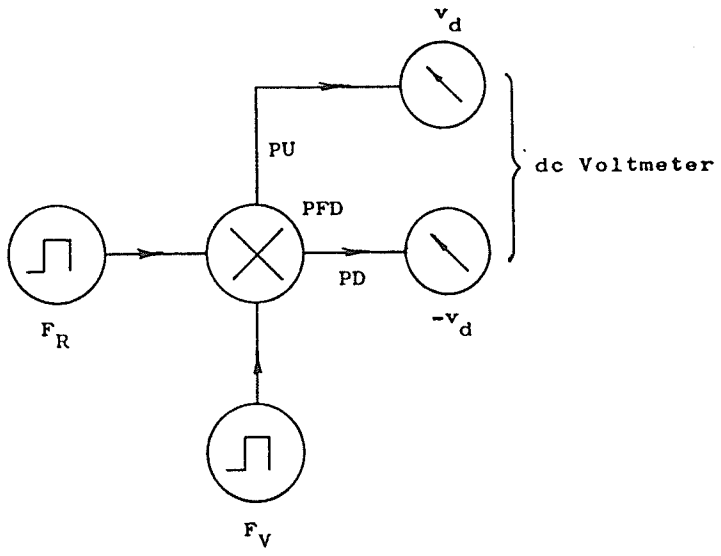


Figure 2.4: Frequency to voltage measurement set-up

found analytically [21],[16] or may be measured in the laboratory with the set up depicted in Fig. 2.4. This set up establishes an equivalent dc voltage for the waveform pres-

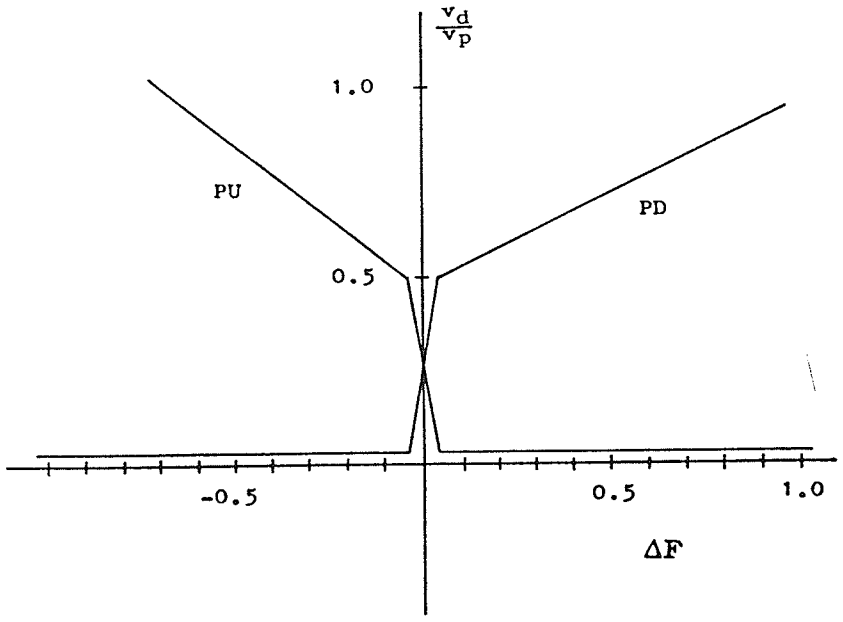


Figure 2.5: Duty cycle versus frequency (Mc4044)

ent at the PFD output for a given frequency difference between the two applied signals (R,V) to the PFD. This dc voltage shall be referred to as v_d and will be defined as positive for the pump up line and negative for the pump down line. The Y-axis of the plot shown in Fig. 2.5 presents the magnitude of v_d normalized to the PFD output voltage, v_p while the X-axis represents normalized frequency difference as given by

$$\Delta F = \frac{F_V - F_R}{F_R} \qquad \ldots(2.33)$$

The device tested was a Motorola MC4044 TTL PFD and the applied signal frequencies ranged from 20 kHz to 200 kHz.

An analytical technique for estimating the acquisition time will now be presented. For a frequency difference between the R and V signals applied at time t=0, the integrator output voltage will be

$$v_0(t) = \frac{v_d t}{R_1 C} + v_0(0) \qquad \ldots(2.34)$$

The VCO frequency as a function of time is proportionally related to v_d by the VCO gain constant K_0, thus,

$$\omega_0(t) = \frac{K_0 v_d t}{R_1 C} + K_0 v_0(0) \qquad \ldots(2.35)$$

A constant value for the magnitude of v_d is assumed to be $0.5v_p$ in keeping with a 'worst case' analysis. This can be justified by the results exhibited in Fig. 2.4. Applying this to (2.35) and differentiating yields

$$\frac{d}{dt}\omega_0(t) = \frac{K_0 v_p}{2R_1 C} \qquad \ldots(2.36)$$

which is an estimate of the rate at which the VCO frequency will be swept toward the R signal frequency. How (2.36) is applied to establishing acquisition time is not obvious as it gives no indication of how close together the two signal frequencies must be in order to establish phase lock. At this point it is assumed that the maximum frequency difference that can exist before lock is established is equal to the the maximum frequency step that may be applied to a locked loop without lock being lost. The maximum phase error for a given frequency step size (applied to a loop at

rest and locked) can be obtained from the solutions for the loop transient response given in Appendix B. The loop will remain in lock as long as the phase error does not exceed it s allowed maximum (±360 degrees for the PFD). Let $\Delta\omega_{smax}$ be the maximum frequency step that may be accepted by the PLD without loss of lock and $\Delta\omega_{sd}$ be the maximum frequency difference between the VCO output frequency in the unlocked condition and the input frequency signal applied at t=0. $\Delta\omega_{sd}$ will be the frequency difference between the upper and lower limits of the VCO tuning range for a 'worst case' analysis. The maximum expected acquisition time, T_a can be estimated from

$$T_a = \frac{2R_1C(\Delta\omega_{sd} - \Delta\omega_{smax})}{K_o V_p} \qquad \ldots(2.37)$$

The above approach to determining acquisition time is undoubtedly simplified, but no further effort will be expended in further refinement as techniques for accurately simulating the unlocked loop on a digital computer are described in the next section. Comparing the predictions of the above approach with the computer model shows reasonable agreement between the two methods thereby demonstrating that the simple analytic approach is useful as a rough guide to be used during the initial design process. (both pump lines are inactive).

2.6 COMPUTER BASED LOOP SIMULATOR

The PFD has been treated as a conventional analog phase detector insofar as analyzing its operation in a locked loop is concerned. The discrete nature of its output has been disregarded by assuming that conditions for continuous time approximation are in place. This approach was presented to serve as a guideline for the initial design of the loop. A computer simulation of the loop may be applied to cases where conditions for the continuous time approximations are not strongly met or when a more accurate determination of unlocked behavior is required. Simulation may offer other advantages over the analytical solutions. These may be summarized as follows:

1. The analog model for the PFD has difficulty providing accurate results when the frequency difference between the two inputs is small, such as during cycle slips which occur when the phase range of the device is exceeded. The simulator on the other hand, can represent behavior of the loop for a wide range of frequency differences such as those occurring from a few cycle slips to complete acquisition of the signal.
2. The simulator will include the pump pulses in the demodulator output which may be quite significant depending on the additional filtering provided.

3. The simulator is not restricted to a particular PFD as any combinational or sequential logic block may be included providing its operation is completely specified by the manufacturer.
4. The modeling of complex loop filters may be more easily analyzed. This feature becomes important when the cut off frequencies of the post detection filter, the loop filter and the VCO response are crowded together, a situation likely to occur in actual loop implementations.
5. Imperfections in the loop components such as nonlinearity in the VCO and either bounding or saturation in the integrator may be accounted for.

The loop simulator was written for a specific cascade of loop filters although the basic structure of the program may be retained for use with other types of open loop transfer functions. A combination of the integrator with phase lead correction, as discussed earlier, is cascaded with a single section low pass filter. The low pass section is required to prevent the high amplitude pump pulses from saturating the VCO control input. The filter also provides for a more predictable open loop response as opposed to that of the VCO control input. This configuration is shown in Fig. 2.6 and will be employed in the loop throughout the remainder of this thesis. The component values are not shown as the loop parameters have not yet been determined. The pump up and

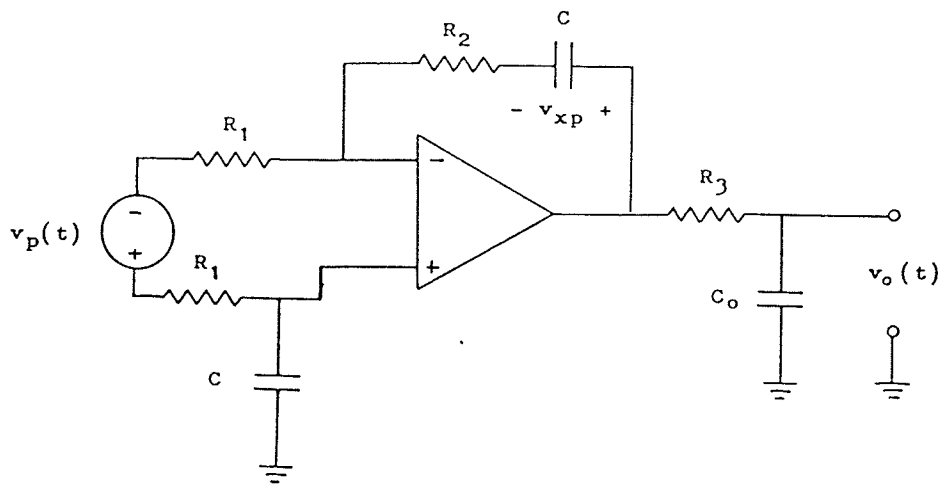


Figure 2.6: Filter cascade employed in the simulated loop

pump down lines are replaced by a single voltage source of magnitude v_p with positive polarity representing the pump up condition and negative for the pump down signal. It follows that the output of the integrator will increase for an active pump up and decrease for an active pump down. There will be no change of the integrator state if v_p is zero

The following discussion introduces expressions which form the heart of the loop simulator. These expressions define the state of the loop and are evaluated for each iteration of the program. Each iteration represents a small interval of time Δt. The discreet nature of the loop simulator vanishes if this interval is made small enough, a condition which is elaborated upon later. The simulation requires a solution to the output voltage $v_0(t)$ after some interval $t+\Delta t$. If V_{xp} is the voltage across the integrating capacitor, C at time t and $v_{0(t)}$ is the voltage across C_0 at time t, then at time $t+\Delta t$,

$$v_0(t+\Delta t) = v_0(t) - \frac{R_3 C_0 v_p}{R_1 C} + \frac{R_2 v_p C + R_1 C(v_{xp}(t) - v_0(t))}{R_1 C}$$

$$+ \frac{v_p \Delta t}{R_1 C} + \left[\frac{v_p R_3 C_0 - R_2 v_p C - R_1 C(v_{xp}(t) - v_0(t))}{R_1 C}\right] \exp[-\Delta t / R_3 C_0] \qquad (2.38\ (a))$$

or for the case when $V_p = 0$,

$$v_0(t+\Delta t) = v_{xp}(t) - (v_{xp}(t) - v_0(t)) \exp[-\Delta t / R_3 C_0] \qquad ...(2.38\ (b))$$

Both of the above equations require the assumption that V_p is constant over the interval Δt. The voltage on the integrating capacitor is given by [15]

$$v_{xp}(t+\Delta t) = v_{xp}(t) + \frac{v_p \Delta t}{R_1 C} \qquad ...((2.39))$$

The instantaneous input frequency is given by (2.1). The instantaneous VCO frequency will be of similar form to the input frequency, thus

$$\omega_0(t) = \omega_c + \frac{d}{dt}\theta_0(t) \qquad ...(2.40)$$

Substituting eqn. (2.4) into the above and integrating yields the phase

$$\theta_0(t+\Delta t) = \theta_0(t) + \omega_c \Delta t + K_0 \int_0^{\Delta t} v_0(\tau)\, d\tau \qquad ...(2.41)$$

which for very small Δt becomes

$$\theta_0(t+\Delta t) = \theta_0(t) + \omega_c \Delta t + K_0 \Delta t v_0(t+\Delta t) \qquad ...(2.42)$$

The input phase may be found from

$$\theta_i(t+\Delta t) = \theta_i(t) + \omega_i \Delta t + \theta_s(t+\Delta t)\mu(t-t_s) \qquad ...(2.43)$$

where θ_s is a test input applied to the loop at time t_s.

The PFD output V_p is generated by a subroutine referred to as a PFD emulator. This subroutine emulates the PFD based on flow and output tables provided by the manufacturer or generated from the logic equivalent which again must be provided by the manufacturer. The flow table is stored in an array where the row and column of this array will identify the present state of the PFD. The PFD output is then determined from an additional array, the output array, which provides an output given the present state of the device. The position in the flow table is determined by both PFD line levels (R and V) and the previous state. The subroutine maintains integer variables representing the row and column of the flow table in order to recall the previous state and updates these variables whenever a change of state occurs. Flow and output tables used by this PFD emulator are listed in appendix C. program. A brief description of the program follows. Once all the loop and simulation parameters are read into the program an initialization occurs where phase angles are set to zero and the VCO and input frequency made equal. The output voltage is made equal to the integrator capacitor voltage. The integrator voltage is set to provide the VCO control voltage necessary to result in the desired initial frequency (supplied as input to the program). This corresponds to a condition in which no pump pulse has yet occurred (ie $V_p = 0$). If the initial frequency of the VCO is equal to the VCO rest frequency (supplied as input) then the loop output voltage will initially be zero

as expected. The PFD is initialized by selecting the row and column of the flow table so that it's output is initially zero with the initial input levels. The loop will remain quiescent if the above initialization procedure is followed and there is no change to the input frequency or phase.

The time is incremented by Δt once the main loop of the program is entered. The phase of the VCO and input signals must be converted to logic levels before being applied to the PFD emulation routine. This conversion is done in a subroutine which generates a zero level for any phase value between 0 and 180 degrees and a logical 1 for the range 180 to 360. A separate subroutine resets the phase angles to the range ±360 degrees (modifications to the subroutine are needed for phase detectors with a greater range than this). If the phase angles are not restricted to some finite range then errors resulting from roundoff accumulate after many cycles and eventually destroys the simulation. The PFD emulator is invoked after the angle to logic level conversion takes place. The emulator produces a pump voltage V_p which is assumed constant over the interval t to $t+\Delta t$. Eqns. (2.38) are used to update the loop output and hence the VCO control voltage. The integrating capacitor voltage is calculated with (2.39) and kept for the next iteration. The phases of the VCO and input signal are then found through use of (2.42) and (2.43) respectively. The term in (2.43) which contains the test phase θ_s provides a means of apply-

ing a test input to the loop at some time t_s. The test input may be a phase step, a phase ramp (frequency step) or any function which generates a new phase value for each iteration. The phase error is calculated as a final step before looping back. Again, the phase error is restricted to the range ±360 degrees. This restriction of phase error allows the start of an out of lock condition to be easily identified. Once the required exit criteria are met, the phase error and output voltage arrays are written into a file for further analysis and plotting.

The iteration period Δt must be made small in order for the simulator to closely approximate its real life counterpart. Given that the pump voltage V_p is constant over the interval spanned by one iteration, the shortest pump pulse is of the length Δt. This results in an uncertainty of the phase error given by

$$|\Delta\theta_e| = \frac{2\pi\Delta t}{T_i} \text{ radian} \qquad \ldots(2.44)$$

where T_i is the period of the input signal. If the number of iterations per input cycle is given by $T_i/\Delta t$, then a phase error uncertainty of ±1 degree requires 360 iterations per cycle of input signal.

The resolution problem arises from the inability to accurately locate input transitions when large iteration intervals are used. Once two active transitions are located accurately, the pump pulse can be made as small as the time

interval separating them. For times removed from those of the input transitions, the interval need only be small enough to perform the integration in eqn. (2.41) with sufficient accuracy. In order to decrease the number of iterations per input cycle while still maintaining reasonable phase resolution, the interval Δt is allowed to vary in the simulator. An initial Δt is chosen small enough to allow for a satisfactory solution to eqns. (2.38) and (2.41) based on a desired output voltage resolution and phase integration accuracy. The simulator will function as previously described until an input transition occurs, after which the time is stepped back one iteration interval, the interval is halved and the process continued. This interval splitting will continue until such time that the minimum iteration interval specified is reached. At this point the PFD emulator is updated and the interval Δt is returned to its initial value so that the search for the next transition may begin. A decrease by a factor between five and eight in simulation time was found between the variable and constant interval approaches (for identical output plots).

Some discussion on integrator bounding is necessary at this point. A practical loop filter of the type described would require some means of maintaining the output of the operational amplifier within the limits of saturation. This effort is referred to as integrator bounding and is necessary because once driven into saturation, the circuit may

take a long and unpredictable period of time to recover after the input changes polarity. Saturation will occur in the loop filter during a zero signal condition or after loss of lock for an extended period of time. In subsequent experiments with a working loop (Chapter 3 and 4), the integrator output is artificially constrained to lie within bounds by close control of input signals, choice of operating voltages etc. Zener diodes were placed across the integrator capacitor in order to limit its voltage during acquisition experiments where the loop would remain out of lock for extended lengths of time.

The design of effective bounding circuits may be quite involved and are certainly dependent on the filter configuration chosen therefore such facilities were omitted from the simulator. Bounding can be approximated numerically by limiting the integrator capacitor voltage in (2.39) to within some range. This is only an approximation to true bounding as the integrator capacitor is also charged during execution of (2.38 a). However, the time constant associated with the integrator is large compared to the iteration interval so that the contribution to $v_0(t)$ by the charge accumulated during this calculation is expected to be minimal. Similar steps, as taken to prevent saturation of the loop filter were also taken in regard to the VCO control input. Limiting was provided for both the simulator and implemented designs in order to prevent saturation of the VCO modulation circuits.

2.7 SIMULATED LOOP OPERATION

The plots in the following section demonstrate the operation of the loop simulator and highlight differences between the transient response of the ideal loop filter and filter with parasitic elements.

The simulated filter is of the form shown in Fig. 2.6. All the runs were performed on a loop with natural frequency 10 kHz and center frequency 200 kHz. The VCO gain constant is 150 kHz/Volt. The component values were selected on the basis of (2.14) together with the damping factor, which was either 0.5 or 1.0 in all the tests performed. The PFD logic family was ECL with an output level of 1.0 Volt. The output filter cutoff frequency was made variable during the tests in order to ascertain its effect on the loop behavior. All the simulations used the interval splitting algorithm starting with an interval of 0.1 T_i and ending with a minimum of interval 1.25×10^{-9} seconds.

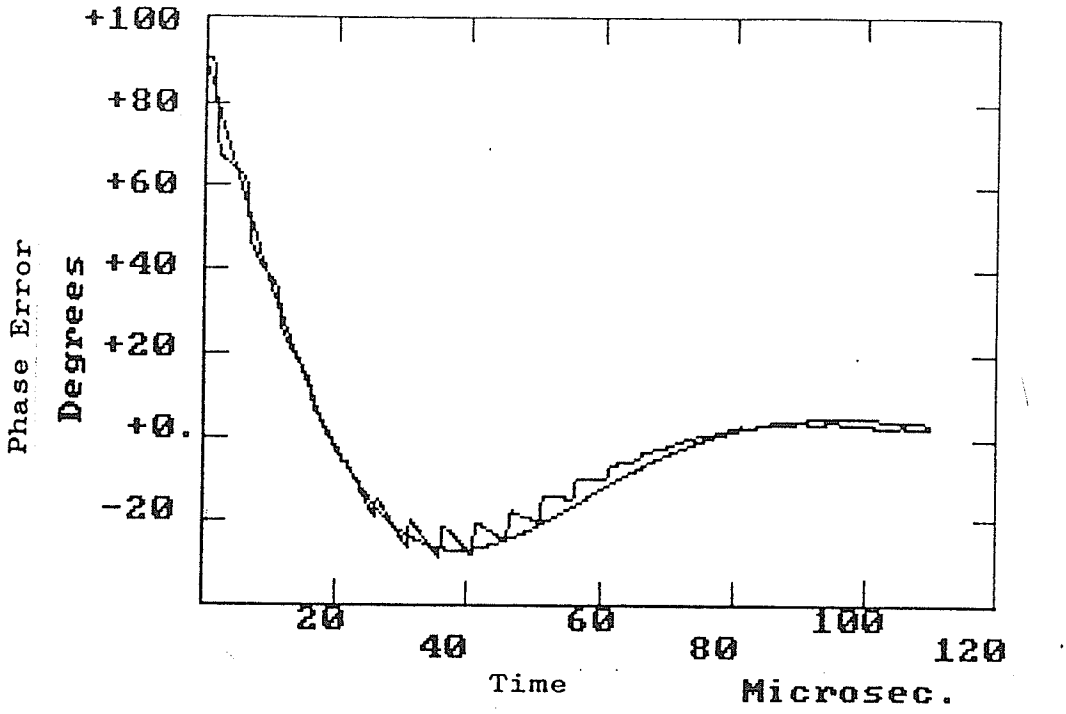


Figure 2.7: Phase step response- Damping factor=0.5

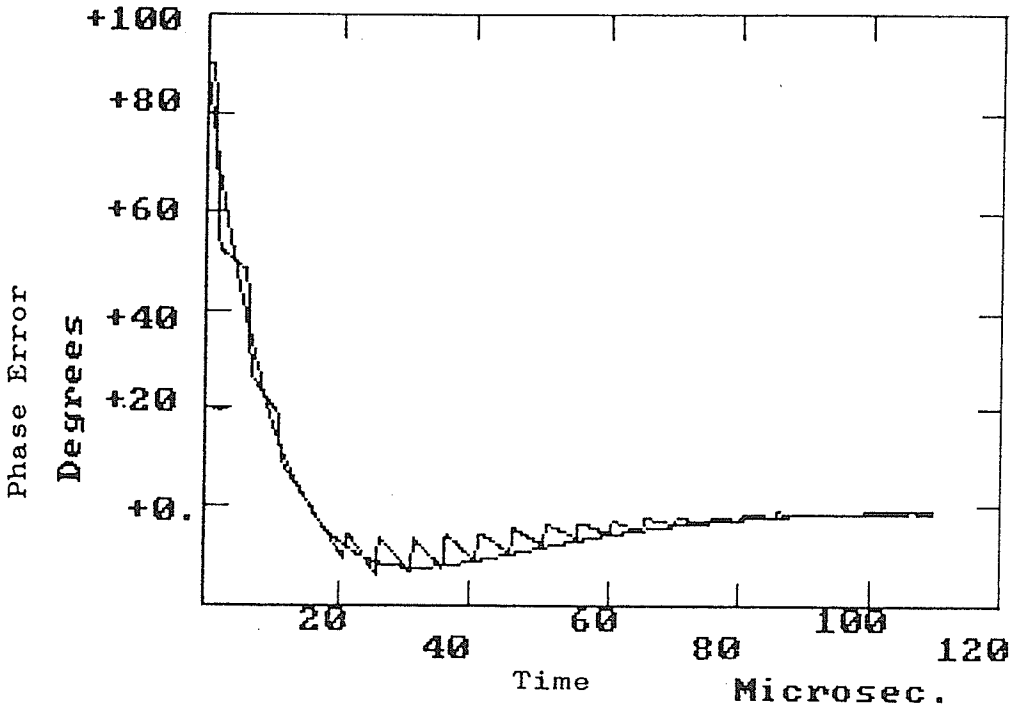


Figure 2.8: Phase step response- Damping factor=1.0

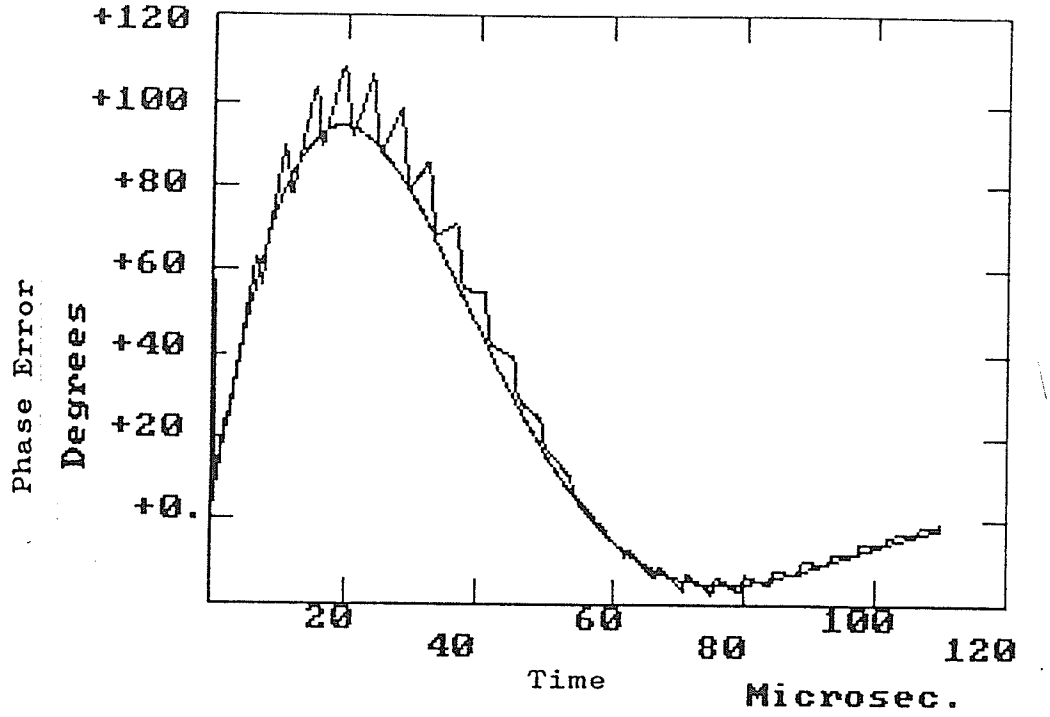


Figure 2.9: Freq. step response- Damping factor=0.5

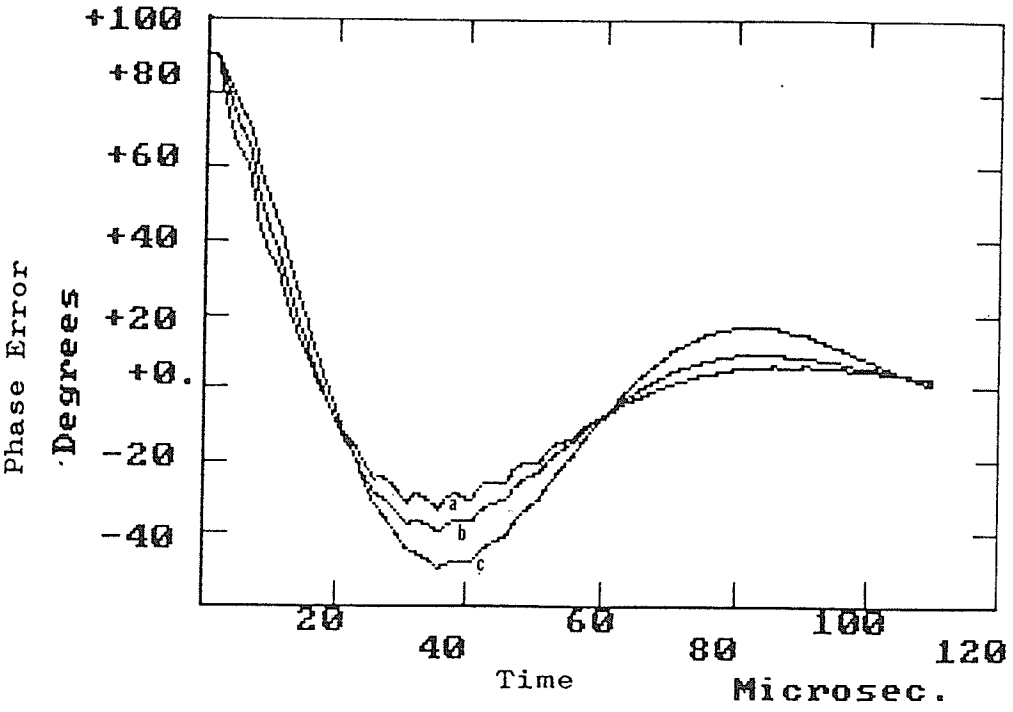


Figure 2.10: Effect of VCO filter on loop response

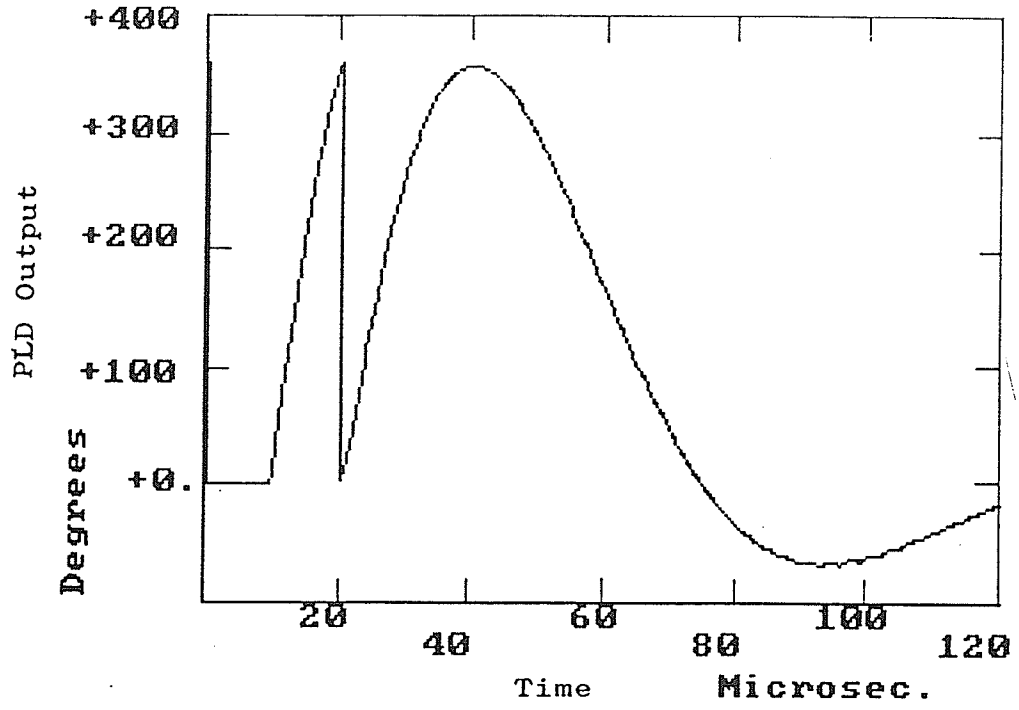


Figure 2.11: Phase error- Large freq. step

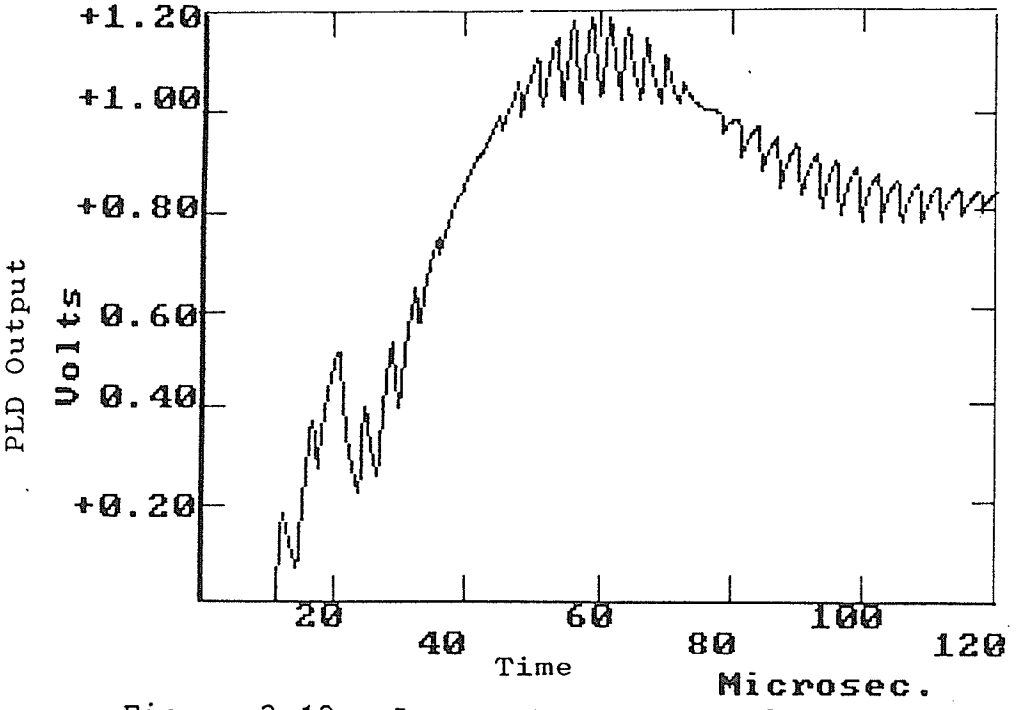


Figure 2.12: Loop output- Large freq. step

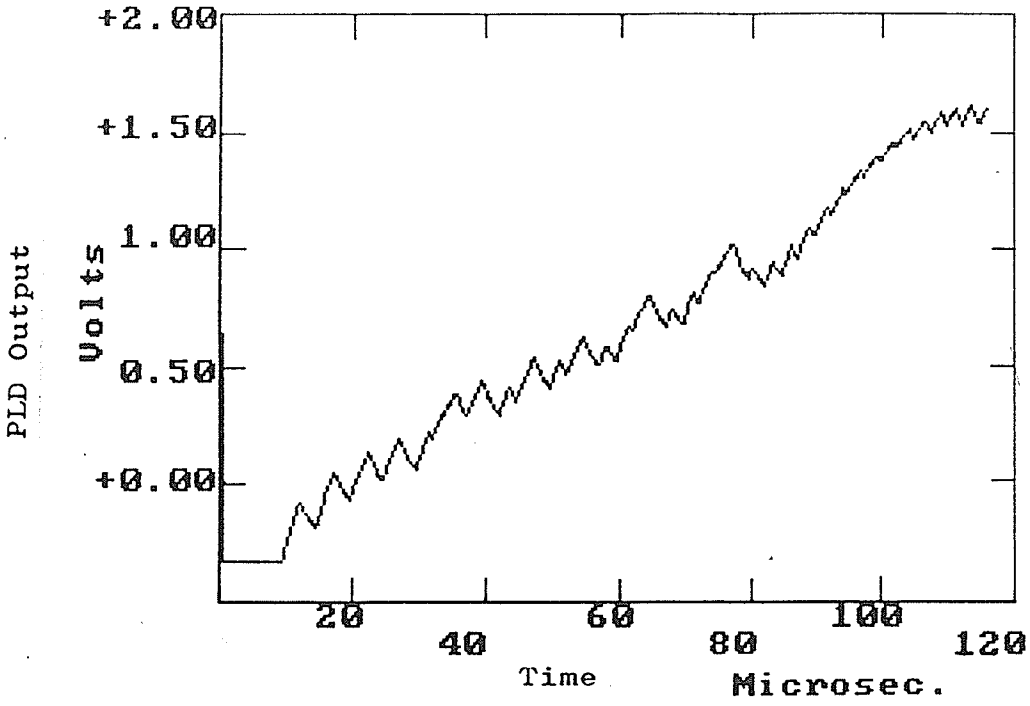


Figure 2.13: Acquisition- Damping factor=0.5

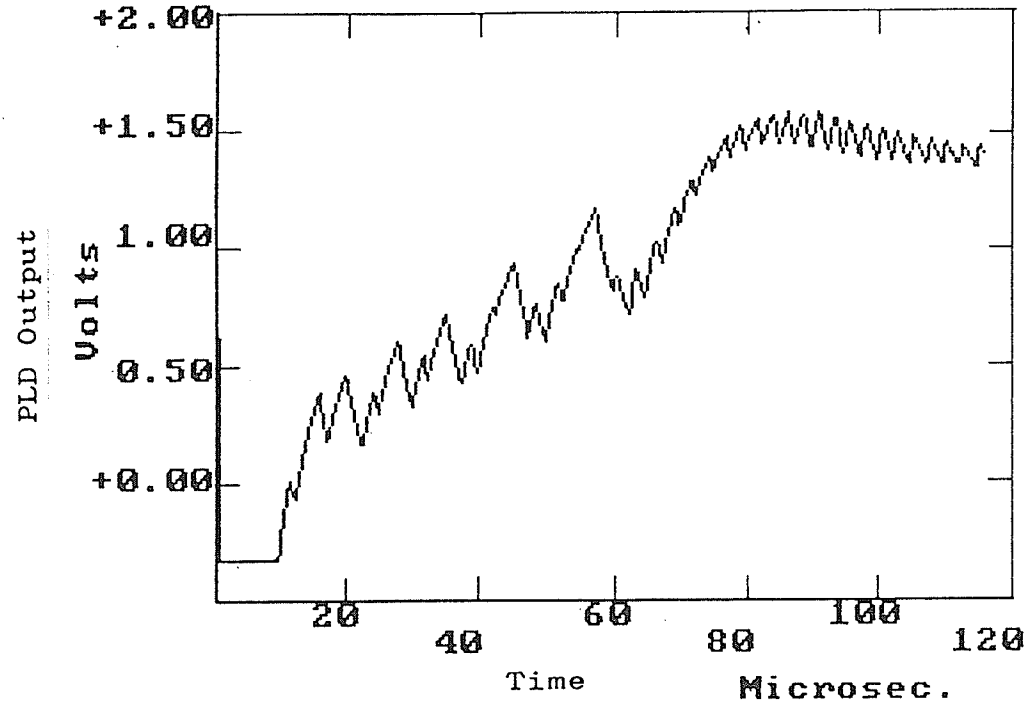


Figure 2.14: Acquisition- Damping factor=1.0

Figures 2.7 and 2.8 result from a 90 degree phase step applied at t=0 to a loop with damping factor ζ of 0.5 and 1.0 respectively. The smooth curve is generated from the analytical solution presented in Appendix B while the other curve is from the simulator. These two curves would be indistinguishable if it were not for the pump pulses present in the simulator case. The VCO filter cut-off frequency used is 1.4 MHz which is too far from the natural loop frequency to contribute significantly to the loop response.

Figure 2.9 shows the loop response (0.5 damping) to a 30 kHz frequency step applied at t=0. Again, theorectical and simulator solutions agree quite well.

Figure 2.10 demonstrates an increased overshoot in the phase step response as the VCO filter frequency is brought closer to the loop frequency. The curves a, b and c were generated with output cut-off frequencies of 100 kHz, 50 kHz and 30 kHz respectively. As expected, the residual pump pulse is lowest for case c.

Figures 2.11 and 2.12 are the phase error and loop output voltage respectively, resulting from a 130 kHz frequency step applied at t=10 μs. As predicted from the analytical solution, the phase error exceeds 360 degrees and the loop looses lock. This condition lasts for only a few cycles after which lock is restored. Loss of lock is easily identified by the appearance of large, long period pulses in the

output voltage waveform. These pulses seem to be characteristic of the out of lock condition.

Figures 2.13 and 2.14 demonstrate the acquisition behavior for a loop with damping factors of 0.5 and 1.0, respectively. The time R_1C constant is 38 μs for both cases. The integrator was bounded at -0.333 Volts (corresponding to a VCO frequency of 50 kHz). A 400 kHz input signal was suddenly applied at t=15 μs, consequently, the VCO frequency was swept toward the input signal at a rate of $3x10^9$ Hz/second. This rate is the same for both values of damping factor and is somewhat higher than the value $2x10^9$ Hz/second predicted by (2.36).

Acquisition (identified by the appearance of low frequency, high amplitude pulses in Fig.s 2.13 and 2.14) was delayed by 20 μs in the case of lower damping over that with higher damping. This is not surprising since the analytical solution predicts that a loop with a damping factor of 1.0 can remain locked with an applied frequency step of up to 170 kHz while only a 114 kHz step can be accepted in the case with lower damping. This difference of 56 kHz accounts for the 20 μs delay in acquisition, assuming that the the VCO sweep speed is $3x10^9$ Hz/second. These numbers support the concept (last section) that the frequency separation of the two signals required for acquisition to take place is similar in magnitude to the maximum allowable frequency step during lock. The above suggests that in general, the loop

with higher damping will acquire lock in the shorter amount of time even though the sweep rate may be similar for both damping factors. This observation may be important if acquisition time is a critical parameter in the loop design.

Chapter III

IMPLEMENTATION OF THE PLD

3.1 INTRODUCTION

This chapter describes the design and construction of a working PLD the performance of which is experimentally evaluated and reported in Chapter 4. The design is based on the requirements for demodulation of signals sent by the HPU of a current measuring system as described in Chapter 1. Although not a field ready unit, the PLD demonstrates the design principles in a laboratory setting.

3.2 LONG LOOP CONFIGURATION

The loop configuration known as the long loop or indirect loop [13],[12] was chosen for the PLD design. The block diagram of this loop is shown in Fig. 3.1. The motivation for choosing this design include;

1. the option of being able to track the VCO and incoming signal frequency drift through control of the reference frequency,
2. the freedom to choose the operating frequency of the detector, independent of the input signal frequency and

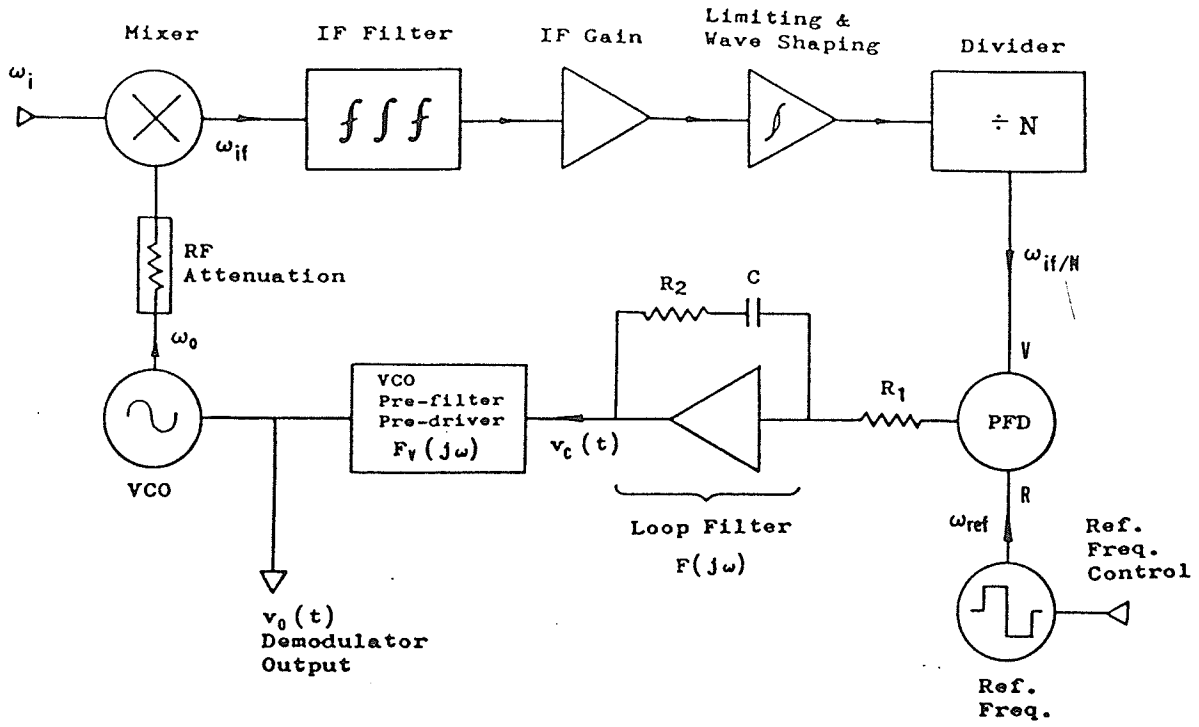


Figure 3.1: Long loop configuration

3. the ability to extend the operating range of the phase detector through frequency division.

This loop is expected to operate in much the same manner as the basic loop except that comparison of phase takes place at the reference frequency as opposed to the continuously varying input frequency. Wide band performance becomes a burden that must be borne by the mixer rather than the the phase detector. The VCO rest frequency is offset from the loop center frequency (either above or below) by some multiple of the reference frequency, $\omega_{ref.}$ Thus, for $\omega_0 > \omega_i$,

$$\omega_0 = \omega_c + N\omega_{ref} + \frac{d}{dt}\theta_0 (t) \qquad \ldots(3.1)$$

or, for $\omega_0 < \omega_i$,

$$\omega_0 = \omega_c - N\omega_{ref} + \frac{d}{dt}\theta_0 (t) \qquad \ldots(3.2)$$

The heterodyne process generates the usual set of signal products out of which the IF bandpass filter selects the signal whose frequency is the difference between that of the input and VCO. For the case where $\omega_0 > \omega_i$, the instantaneous IF frequency, ω_{if} is given by

$$\omega_{if} = \omega_0 - \omega_i \qquad \ldots(3.3)$$

or for the image response ($\omega_0 < \omega_i$),

$$\omega_{if} = \omega_i - \omega_0 \qquad \ldots(3.4)$$

Substituting (3.1),(2.1) and (2.3) into (3.3) yields

$$\omega_{if} = N\omega_{ref} - \frac{d}{dt}\theta_e (t) \qquad \ldots(3.5)$$

and similarly for the image response,

$$\omega_{if} = N\omega_{ref} + \frac{d}{dt}\theta_e (t) \qquad \ldots(3.6)$$

The following discussion assumes that a positive detector output v_p will cause the control voltage of the VCO to rise (i.e. there is inversion of sign in the loop filter). If the PFD is connected to the system as depicted in figure 3.1, the variable PLD input frequency, ω_v will be obtained by dividing (3.5) by N. Hence,

$$\omega_V = \omega_{ref} - \frac{d}{dt}\frac{\theta_e(t)}{N} \qquad \ldots(3.7)$$

The reference input to the PFD is obtained from an oscillator with instantaneous frequency, ω_{ref} . Thus,

$$\omega_R = \omega_{ref} + \frac{d}{dt}\theta_{ref} \qquad \ldots(3.8)$$

With the loop locked and the R and V signals of the PFD as in (3.7),(3.8), the PFD behaves as a phase detector with output given according to (2.30) as

$$v_d = K_d\left[\theta_{ref} + \frac{\theta_e(t)}{N}\right] \qquad \ldots(3.9)$$

The reference input phase, θ_{ref} will be constant and hence plays no further role in the loop dynamics. It will be set to zero for the remainder of the analysis. The PFD output of (3.9) becomes,

$$v_d(t) = \frac{K_d}{N}(\theta_e(t)) \qquad (\omega_0 > \omega_i) \qquad \ldots((3.10))$$

Following similar steps, but using (3.6) yields for the image response.

$$v_d(t) = \frac{K_d}{N}(-\theta_e(t)) \qquad (\omega_0 < \omega_i) \qquad \ldots((3.11))$$

A stable phase lock will occur with either the real or image response (depending on the sign of the loop filter transfer function and VCO gain constant) but not for both. Selection of the opposite response may be made by interchanging the R and V inputs of the PFD to oppose that depicted in figure 3.1.

The phase detector gain constant (as described for the basic loop) is effectively divided by N in loops with frequency division. By performing this division in (2.14a) and (2.14b), the loop equations as developed for the basic PLD remain valid for this new loop. The dynamic range of the PFD is multiplied by the factor N and as a result, the maximum frequency deviation as calculated from (2.28) is similarly multiplied by N.

3.3 LONG LOOP SIGNAL ACQUISITION

The process of signal acquisition in the long loop is similar to that of the more basic loop but involves the IF and reference frequencies as opposed to the VCO and input frequencies of the latter. The acquisition process is made somewhat more complicated by the dual response nature of the heterodyne configuration and by the presence of the IF bandpass filter. The assumption that the VCO frequency is constrained to lie within some range defined by limits is made and likewise, the input frequency must also remain within this range. The only exception will be the case where a loss of input signal occurs wherein the input frequency is considered to be zero. There are two situations which are likely to invoke the acquisition process: The first results from the loss of signal where the VCO frequency will have ample time to drift over to some rest position and all transients will die out. The input signal suddenly reappears within the frequency range of the VCO and acquisition com-

mences. The second situation results when lock is somehow lost but the input signal remains within the frequency range of the VCO. This differs from the first in that the VCO frequency may be anywhere within it /s tuning range as opposed to the limits.

Initially, the VCO frequency ω_0 must be swept toward some stable operating point if successful signal acquisition is to take place. It must now be determined if this action does occur for the two situations described above and if not, the offending conditions should be recognized and avoided. From the study of the unlocked loop behavior in Chapter 2, the sign of the filter transfer function and VCO gain constant may be picked so that

$$\omega_V > \omega_R \longrightarrow \frac{d}{dt}\omega_0(t) < 0 \qquad \ldots(3.12\ (a))$$

$$\omega_V < \omega_R \longrightarrow \frac{d}{dt}\omega_0(t) > 0 \qquad \ldots(3.12\ (b))$$

TABLE 3.1

Loop frequency relations-locked condition

Response	ω_V	ω_R	ω_0
1	$\frac{1}{N}\omega_{if}$	ω_{ref}	$\omega_{if} + \omega_i$
2	ω_{ref}	$\frac{1}{N}\omega_{if}$	$\omega_i - \omega_{if}$

TABLE 3.2

VCO sweep behavior

Response	$\lvert\omega_{if}\rvert$	VCO sweep direction
1	$>N\omega_{ref}$	down
1	$<N\omega_{ref}$	up
2	$>N\omega_{ref}$	up
2	$<N\omega_{ref}$	down

Table 3.1 lists the loop frequency interrelationships during the locked condition for the circuit environment specified by (3.12). This table provides information as to what signals are applied to the R and V inputs of the phase frequency detector for a given demodulator response. The terms 'real ' and 'image' response are replaced by the numerical nomenclature 1 and 2, respectively.

Consider the loop to be unlocked. The direction in which the VCO frequency will change given a particular PFD connection and instantaneous IF frequency, may be determined from (3.12) and table 3.1. The results are tabulated in table 3.2. and the five conditions describing the state of the loop immediately before acquisition begins, may be identified as follows:

1. ω_0 on the same side of ω_i as it would be during lock,

2. ω_0 on the opposite side of ω_i as it would be during lock,
3. $|\omega_{if}| > N\omega_{ref}$,
4. $|\omega_{if}| < N\omega_{ref}$,
5. $\omega_{if} = 0$ if $|\omega_0 - \omega_i| > \omega_{uif}$,and
6. $\omega_{if} = 0$ if $|\omega_0 - \omega_i| < \omega_{lif}$.

The last two conditions will be further elaborated upon. The last column in table 3.1 provides information on the frequency relationship between the VCO and input during lock. This information along with table 3.2 yields the conclusion that successful acquisition only occurs if condition (1) holds or if conditions (2) and (4) hold. Conversely, acquisition will be unsuccessful if ω_0 is on the opposite side of the lock point, concurrent with $|\omega_{if}| > N\omega_{ref}$.

Now consider the situation where the signal is lost. The VCO frequency will retreat to the bottom of its range in a loop with a response of type 1. For acquisition to occur in this case, the signal must reappear within a range $N\omega_{ref}$ of the VCO frequency. The same requirements hold for a loop with response of type 2 except that the VCO frequency retreats to the top of its allowed range. Hence the VCO frequency must be bounded so that its total range is less than or equal to $N\omega_{ref}$, otherwise, acquisition can not be guaranteed.

The bandwidth of the IF system was tacitly assumed to cover the entire range of VCO and input frequencies in the discussion up to this point. This is not necessarily the case, therefore, conditions 5 and 6 were added to the above list to take into account the finite bandwidth of the IF stage. The constants ω_{lif} and ω_{uif} are the lower and upper bandwidth limits respectively. Tables 3.1 and 3.2 in conjunction with these two conditions may once again be invoked to predict loop behavior during the unlocked state. Considering the loss of signal condition where $\omega_i = 0$ in condition 5, it may be seen that for a loop of response type 1 the VCO retreats to the top of its range as opposed to the bottom in the wideband IF case. After the signal reappears, acquisition will occur whenever the condition

$$|\omega_{0_{max}} - \omega_i| < \omega_{uif} \qquad \ldots(3.13)$$

is valid. Eqn. (3.13) suggests the following criteria for IF bandwidth selection:

$$R|\omega_{0_{max}} - \omega_{0_{min}}| < \omega_{uif} < \omega_{0_{min}} \qquad \ldots(3.14)$$

where R=1 (R is a dimensionless scale factor) will guarantee acquisition for an input signal appearing anywhere in the band, however, for realistic applications the signal will most probably be found near the band center so that any R value greater than 0.6 is adequate. The situation of having the IF bandwidth larger than suggested by (3.14) represents a transitional state between the narrow band design and the

wideband design initially addressed. A special study of this latter case would have to be undertaken. The IF bandwidth of a type 2 response loop follows the same design constraints as developed above for the type 1 response loop. Eqn. (3.14) is still applicable and also (3.13) if ω_{max} is replaced by ω_{min} .

A similar analysis as carried out for the upper IF frequency limit may be performed for the lower limit. It will be seen that establishing this limit is only of concern when the VCO frequency is very close to that of the input signal. This is not likely to happen in the case were loss of input signal occurs as the VCO will retreat to the band extremes where the input signal should never be found in a proper loop design. For the situation where lock is lost but the input signal remains within the range of the VCO, the situation will correct itself by forcing the VCO to sweep over to the band edge where the acquisition process will begin. In order to minimize potential delays in the process and the danger of the VCO becoming locked at its frequency limit, the above reasoning suggests making the lower frequency limit of the IF stage as low as possible.

In summary, if the IF bandwidth is designed with upper frequency limit according to (3.14), with R>0.6 and lower limit to be as low as possible, acquisition will be assured in a properly designed demodulator for complete loss of the input signal. Should the loop become unlocked for other

reasons, acquisition likewise occurs, however, the exact trajectory taken by the VCO frequency is not obvious and, hence, the acquisition time may be difficult to estimate.

3.4 LOOP COMPONENTS

The Phase locked demodulator as implemented for experimental evaluation consists of three distinct blocks each of which is described in detail in the following sections.

3.4.1 Frequency Conversion Block

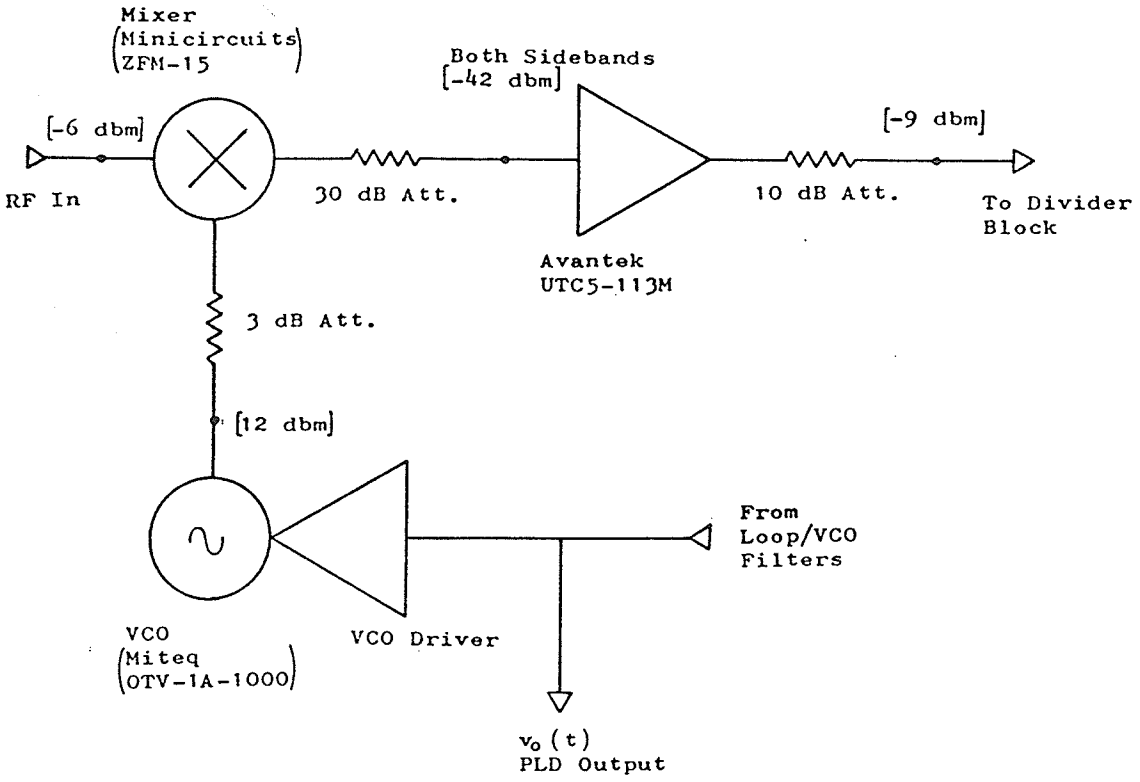


Figure 3.2: RF frequency conversion block

Figure 3.2 is a block diagram of the section involved in tracking the RF input signal and converting it to the IF frequency of 320 MHz.

The VCO utilized is a low cost, off-the-shelf unit manufactured by Miteq Inc. Its poor performance makes it only suitable for employment in a test system and its deficiencies will highlight some of the difficulties associated with VCOs, likely to be encountered in future loop designs. This unit consists of a single transistor oscillator (therefore, unbuffered) in a common collector configuration. Electronic tuning is accomplished by varying the reverse bias voltage to a varactor diode. The unit has no mechanical tuning adjustment. Over the specified operating frequency range of 1000 MHz to 2000 MHz there is a sudden change of VCO gain at 1400 MHz (its value below 1400 MHz being several times higher than that above) and a somewhat less dramatic decrease in the gain above 1900 MHz, confining the useful range to the limits 1500 and 1900 MHz. Furthermore, hysteresis was noted in the gain constant for frequencies below 1400 MHz.

It comes as no surprise that the frequency of the VCO is dependent on load impedance (especially to reactive components) as no buffering has been provided [17]. A frequency pulling test was conducted by terminating the VCO output through a 6 dB attenuator to a movable short circuit. This presents a load with VSWR of 1.7:1 and reflection coefficient with angle variable over 360 degrees. The VCO fre-

quency was monitored by a frequency counter, coupled via a 10 dB directional coupler. A frequency change from 1668 MHz 1734 MHz was noted at a constant tuning voltage for a phase change in the reflection coefficient of 110 degrees. This change is considered significant as it represents 17 % of the useful VCO tuning range and clearly demonstrates that the mixer VSWR at the local oscillator port plays a significant role in the overall transfer function of the demodulator.

The mixer is a wideband double balanced type manufactured by Mini-circuits with the model designation ZFM-15. This device operates with RF and LO (local oscillator) signals from 10 MHz to 3000 MHz and an IF response between 10 MHz and 800 MHz, with a single sideband conversion loss of 6.5

TABLE 3.3

Measured VSWR of LO port with LO drive.

VSWR (LO Port)	LO Drive (dBm)
1.9:1	4
1.5:1	5
1.4:1	6
1.2:1	>7

dB. The VSWR of the mixer LO port was measured with various LO drive levels and the results are tabulated in table 3.3. No dependence of the LO port VSWR on RF input (RF port) level was noted provided that the LO drive was greater than 6 dBm and the RF input level less than -2 dBm. The LO port VSWR did exhibit a change with temperature, the effect being minimal at high LO drive levels. With an LO drive of 5 dBm, the VSWR ranged from 1.8:1 at 0 degrees Celsius to 1.4:1 for temperatures above 40 degrees. For levels above 6 dBm the VSWR dropped to 1.3:1 over the same temperature range. The VSWR seen by the VCO when connected to the LO port of the mixer is minimized for LO drive levels of greater than 6 dBm and is independent of RF input levels to the loop.

The VCO gain constant cannot be measured with the VCO in isolation due to the effects discussed above. This parameter is best determined for the VCO-mixer as a single unit, therefore, the gain constant as a function of frequency is obtained with the VCO-mixer embedded in the loop. These results are presented in Chapter 4.

The VCO output was found to range between 11 and 13 dBm over the frequencies of interest allowing the installation of a 3 dB attenuator between the VCO and mixer and still permitting the minimum required drive of 6 dBm to be attained. This further isolates the VCO from variations in mixer VSWR. The VSWR of a given load as seen through an attenuator undergoes a reduction as given by

$$VSWR = \frac{VSWR_{LOAD}\,(A^{0.5}+1)-A^{0.5}+1}{VSWR_{LOAD}\,(1-A^{0.5})+A^{0.5}+1} \qquad \ldots(3.15)$$

where is A is the attenuation factor (0.5 for a 3dB attenuator).

The bandwidth of the VCO tuning input was specified to be in excess of 100 kHz and this was confirmed by monitoring the VCO output with a delay line frequency discriminator as a variable frequency signal was applied to the control input. Some dependence on input amplitude was noted.

The IF gain block was a pre-packaged assembly of microwave hybrid amplifiers manufactured by Avantek Inc., designated UTC5-113M. The frequency response is from 5 MHz to 500 MHz with an average gain of 45 dB. The amplifier and mixer in cascade had a frequency response sufficiently poor above 1000 MHz that the IF may be regarded as having a band pass response with upper frequency cut-off somewhere between 500 and 1000 MHz and a lower cut-off of 10 MHz (determined by the mixer). Since the loop is constrained to operate in the linear range of the VCO (which is only 400 MHz wide) acquisition should be guaranteed.

The attenuator installed between the mixer and amplifier serves to decrease the VSWR as seen by the mixer for frequencies above the specified range of the amplifier and also to adjust signal levels in the loop. The attenuator following the amplifier is required to lower the VSWR of the following divider stages as seen by the amplifier. The signal

level fed to the divider chain is limited to -9 dbm in order to operate the IF amplifier well under it s one db compression point (+7 dbm).

3.4.2 PFD - Filter block

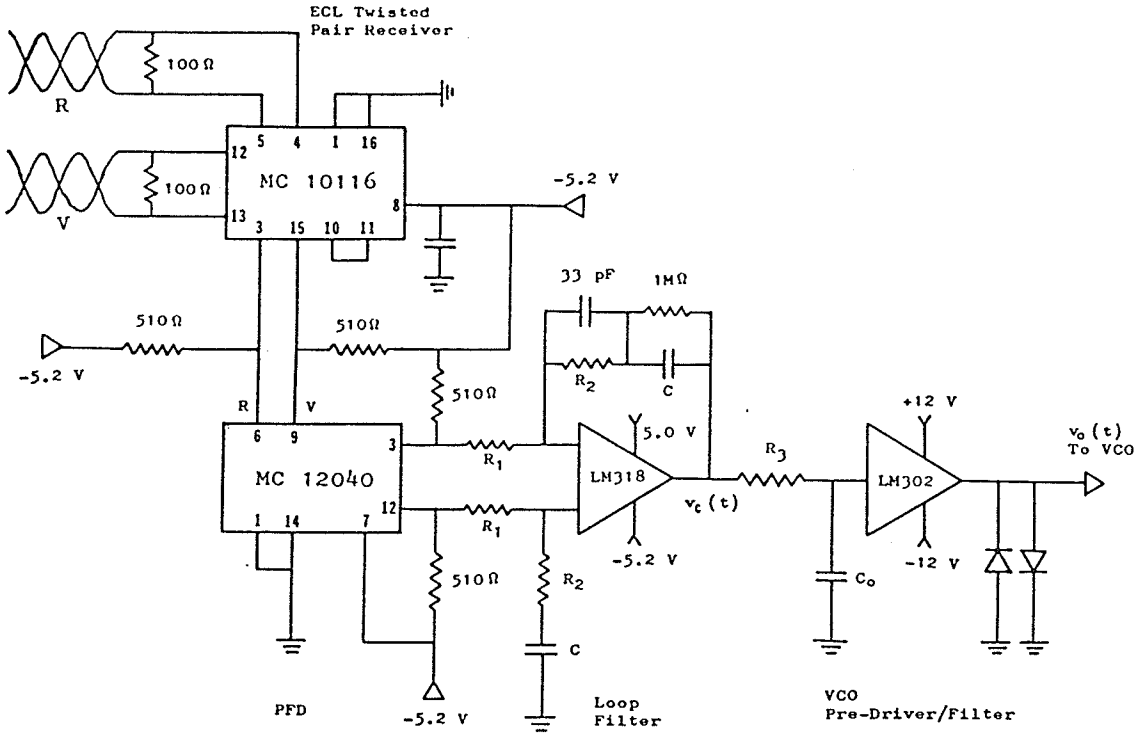


Figure 3.3: PFD - Filter block

Figure 3.3 is a schematic diagram of the block that contains the PFD and associated loop filters. ECL technology was chosen for the PFD primarily because of its low noise operation. Being a non-saturating logic device, the noise spikes and high frequency 'hash' associated with the switching operations of TTL are avoided. The attribute of distinct, noise free logic signals is particularly important in a circuit where the waveforms are to be studied and recorded. Furthermore, the gate delays of ECL type PFDs are an order of magnitude smaller than similar TTL devices, thereby removing the problems with propagation delay from this study. The phase detector block is isolated from the divider block (containing TTL) by use of separate power supplies and by using a differentially fed twisted pair transmission system to interconnect the two boards. All the gate and line terminations were selected according to the recommended ECL design practices set forth by the manufacturer [18].

The PFD outputs differentially drive an integrator built around an LM-318 operational amplifier. The open loop gain of this amplifier reaches unity gain at 10 MHz hence, this circuit should be able to deal effectively with any of the loop signals including several harmonics of the pump pulses. The 33 pF capacitor was needed for frequency compensation (removes high frequency ringing that follows a pump pulse edge) but plays no part in the loop transfer function. The filter design was based on the following list of assumptions:

1. The VCO gain constant is 280 MHz/Volt or 1.76×10^9 rad./volt-sec.
2. The VCO bandwidth is at least 100 kHz.
3. The reference frequency will be at least 10 times the loop frequency if the continuous time approximation is to hold (Ch. 2).
4. The upper IF bandwidth cut-off frequency is 500 MHz.
5. The maximum VCO frequency swing is 400 MHz.
6. A desired modulation bandwidth will be several kHz with a maximum deviation of 100 MHz (a protection application with a 10 per unit dynamic range). A one per unit signal will have a deviation of 10 MHz.
7. The frequency dividers will be decade dividers.
8. The PFD has a maximum phase range of $\pm 2\pi$ radians and a gain constant of 0.16 Volt/radian (assume $v_p = 1.0$ in (2.32 b)).

Following an a priori assumption that the loop frequency, ω_n will be around 10 kHz, and calling upon points 3,4 and 7, a frequency division factor of 1000 is chosen. Multiplying the maximum PFD range (point 8) by this factor and substituting the result into (2.28) will produce a relation between maximum input frequency deviation and loop frequency. A PLD with damping factor of one and loop frequency of 50×10^3 rad/sec. (8 kHz) will accept the required input deviation of 100 MHz. The loop should now remain locked even if driven by a signal of full deviation and frequency equal to 8 kHz, an unlikely extreme.

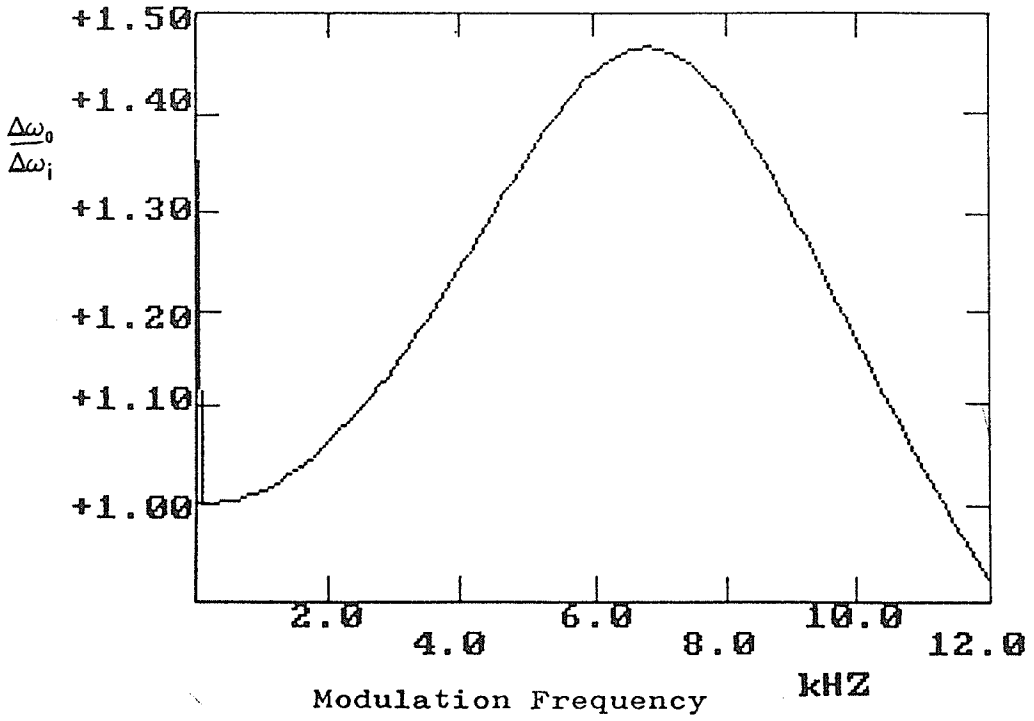
Figure 3.4 a an b are plots of the magnitude and phase respectively of the loop transfer function (2.23) with respect to modulating frequency for a loop with ω_n=8 kHz. The maximum VCO deviation for the extreme case where the loop is excited near its natural frequency and with a damping factor of 0.5 is seen to be approximately 1.4 times that of the input deviation. Given points 6 and 7, this should present no difficulties.

Using (2.23), an expression for the percentage error in amplitude of the demodulated waveform is

$$\%error=|1-H(j\Omega)|x100 \qquad ...(3.16)$$

Inspection of the plot of Fig. 3.4 (a) shows this to be under 5 % at 2 kHz thereby meeting the accuracy specifications for protection service and under 0.2 % at 60 Hz for metering considerations. Similar conclusions may be drawn from the plot of phase lag in the demodulated signal, Fig. 3.4 (b).

The following component values were chosen on the basis of (2.14): R_1=5200 Ω, C=22000 pF, R_2=820 Ω for ζ=0.5 and R=1700 Ω for ζ=1.0. In order to minimize pump pulse energy at the VCO control port, it is standard practice to follow the loop filter with additional low pass filtering which should have a cut-off frequency at least five times that of the loop frequency (in order not to disturb the loop dynamics) [20]. The components R_3 and C_0 in Fig. 3.3 were chosen to provide an upper frequency cut-off of between 40 kHz and



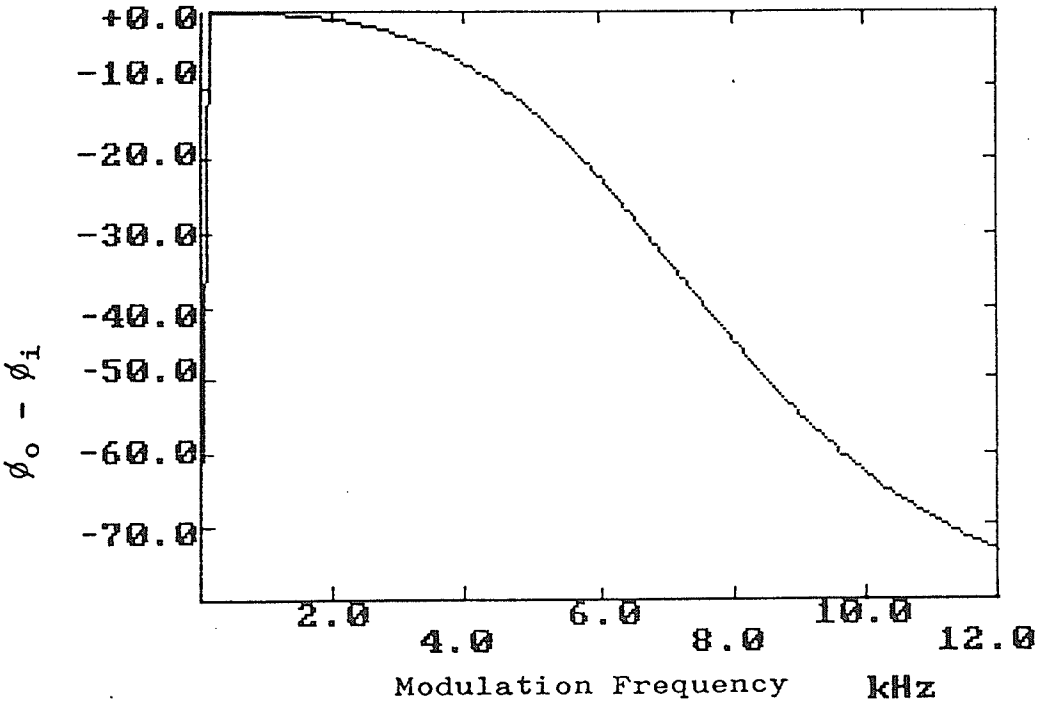


Figure 3.4: Plots of PLD transfer function

80 kHz. With a 40 kHz filter section, the additional phase lag (ϕ_{LPF}) was found to be 11.5 degrees at 8 kHz and 1.5 degrees at 1 kHz from the following expression [13].

$$\phi_{LPF}(\omega)=-TAN^{-1}(\omega R_3 C_0) \qquad ...(3.17)$$

The inclusion of this low pass filter section will in fact modify the loop dynamics as was demonstrated by the loop simulator in the previous chapter. Increased overshoot and longer settling times were noted as the filter cut-off frequency was lowered. The above calculations regarding accuracy of the demodulation process should be accepted with caution until experimental data or simulation results are obtained for this specific loop design.

3.4.3 Frequency divider block

The frequency divider block depicted in Fig. 3.5 contains the divide by 1000 chain for the V input to the PFD and the reference frequency clock. The diagram is self explanatory as conventional digital dividers are employed. The only critical stage involves the Fairchild 11c90 ECL prescaler which serves as the interface between the analog IF stage and the digital division and phase detection section. Little effort was expended in matching the input to the prescaler as its impedance varied widely with frequency and signal amplitude and the preceding IF stage produced ample power to allow attenuation to be inserted for isolation. The input impedance transformation ratio was chosen (from a

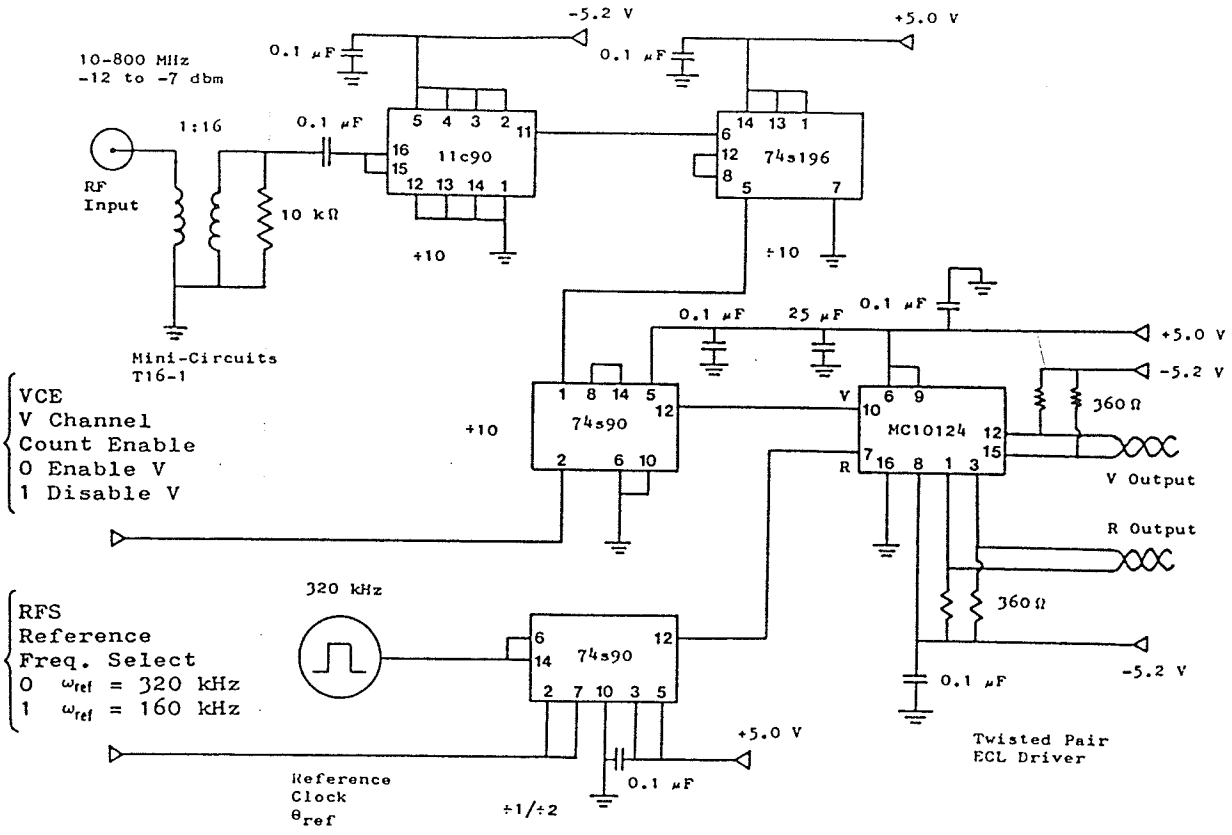


Figure 3.5: Frequency division block

selection of 1:2,4,8,16) so as to maximize the frequency and input signal range with the device still able to toggle. This impedance transformation must overcome parasitics (inductive) of the blocking capacitor as well as interconnections and is therefore specific to the actual construction. Typical input voltage levels were in the order of 200 mV at the upper frequency end (800 MHz). The dynamic range was minimal at the upper frequency end (about 6 dB) but increased quickly with decreasing frequency. By operating the

prescaler at some point near the middle of this toggling range, it was hoped that some rejection of amplitude modulation would occur (limiting).

The remaining dividers were all of TTL technology and a conversion to ECL levels takes place at the twisted pair driver. An input designated as VCE (V Channel Enable) was included for use in acquisition tests (described in Chapter 4). The divider operates only when a TTL low is applied to this line.

The reference clock (built around an available crystal oscillator) operates at 320 kHz resulting in an IF frequency during normal operation of 320 MHz. An input designated as RFS (Reference Frequency Select) was included for use in measurement of the loop's frequency step response. Applying a TTL high to low transition to this line shifts the reference frequency from 160 kHz to 320 kHz thereby applying a frequency step to the loop. Details will be covered in the next chapter.

Chapter IV

EXPERIMENTAL EVALUATION OF THE PLD

4.1 INTRODUCTION TO THE MEASUREMENT PROGRAM

This chapter describes experiments set up to determine the PLD transfer characteristics, bandwidth and acquisition behavior and compares the results to those predicted from the analytical tools introduced in earlier chapters.

During locked operation, (2.20) predicts the gain of the PLD to be inverse to the VCO gain constant and its frequency response dependent on the linear loop transfer function $H(j\omega)$. For the actual circuit the VCO gain is a function of its control voltage hence the PLD gain is no longer constant and must be replaced by a PLD transfer characteristic that relates the PLD output voltage to a given input frequency. Also, the frequency response is no longer represented by $H(j\omega)$ and consequently the transient response will not be as predicted. However, by providing a VCO transfer characteristic, the loop simulator developed earlier can accurately predict transient response and acquisition behavior for the actual loop.

In order to predict PLD dynamic behavior for any arbitrary input, including a steady state situation , a non-lin-

ear transfer function must be developed [22]. This transfer function could be developed experimentally through measurement of the PLD single and multi-tone frequency response, and harmonic distortion [22]. However, there was no test equipment available that had the capability of being modulated with large enough frequency deviations and with modulation frequency sufficiently high to perform these measurements. Rather than attempt to completely specify the loop's dynamic behavior, a comparison between measured and predicted performance is provided through measurement of the loop frequency step response since a frequency step can be readily applied to the PLD and the loop transient response can be readily simulated. Although the fidelity of an arbitrary input waveform is not predictable directly from this experiment, the PLD's ability to recover from severe input disturbances (such as the frequency step) is demonstrated. Furthermore, if the VCO transfer characteristic is approximately linear and there is reasonable agreement between experimental results and those obtained from equations of Appendix [B], predictions of loop frequency response can be made by cautiously applying linear loop theory.

For low modulation frequencies (far below the loop frequency), the PLD output is related to the instantaneous input frequency by the PLD transfer characteristic since the loop transfer function (2.23) becomes unity. Hence, fidelity predictions of the demodulation process at powerline fre-

quencies (metering applications) will be based on this characteristic. This is analogous to the linear (ideal) loop where the PLD gain (2.21) determines the low frequency steady state loop response.

Clarification of the term 'phase error' is required to prevent confusion surrounding its use in this chapter. The term phase error as applied to the long loop configuration refers to the phase difference between the input signal and VCO output as defined by (2.3), whereas the phase error between inputs R and V of the PFD is the phase difference divided by 1000 (the IF frequency division ratio). The phase error of a single loop PLD with no frequency division will be compared to that of the long loop PLD and the context in which the phase error is used will be obvious in relation to which side of the frequency divider the quantity refers.

The final task of this chapter will be to present the results of noise measurments on the PLD. By determining the noise floor of the PLD, the dynamic range of the device can be specified.

In summary , the experiments in this chapter will serve the following:

1. Determination of the PLD transfer characteristic.
2. Derivation of the VCO gain as a function of control voltage (from 1).

3. Provide a record of PLD transient response.
4. Provide a record of PLD acquisition behavior.
5. Permit simulations using the non-linear VCO to be compared to the recorded transient response.
6. Obtain the dynamic range of the PLD by measuring its noise floor.

4.2 FREQUENCY RAMP RESPONSE

4.2.1 Objectives

An experiment was undertaken to establish a transfer characteristic relating the input frequency of the applied signal to the demodulator output. In order to remain consistent with the development in chapter 2, the voltage output will represent a frequency difference between the PLD center frequency ω_c and the input signal frequency (the PLD output is zero when the input frequency is equal to ω_c). The variable ω_a represents this offset from center the center frequency and is introduced to simplify the equations in this chapter. By definition

$$\omega_a(t) \triangleq \omega_i(t) - \omega_c \qquad \ldots(4.1)$$

The static transfer characteristic was determined by monitoring the output of the PLD as an input signal of constant frequency (CW) was applied. This was repeated for a large number (approximately 400) equally spaced frequencies between 1300 and 1500 MHz. By keeping the IF frequency fixed at 320 MHz, the VCO transfer characteristic is obtained

since the frequency of the VCO is 320 MHz higher (response #1 in Chapter 3.2) than that of the input signal for each point. The differential VCO gain is defined as

$$K_0(v_0)=\frac{d}{dv_0}\omega_0(v_0) \qquad \ldots(4.2)$$

Which is to say the slope of the VCO transfer characteristic yields the VCO gain as a function of input voltage. For a linear VCO transfer characteristic the VCO gain is constant. The differential VCO gain function (as defined in 4.2) can be easily incorporated into the computer loop simulator to improve its accuracy over the use of a constant VCO gain (this will be discussed further in a later section).

A dynamic transfer characteristic is determined by sweeping the input frequency over the range in question at a constant rate and simultaneously recording the output voltage. This test demonstrates that the PLD is operational in that it can indeed track a time varying input signal. Furthermore, if the static and dynamic transfer characteristics prove to be almost identical, it shows that the static transfer characteristic is useful in predicting the fidelity of the demodulation process for signals having rates of change (at full deviation) comparable to that of the swept test input.

4.2.2 Experimental Method

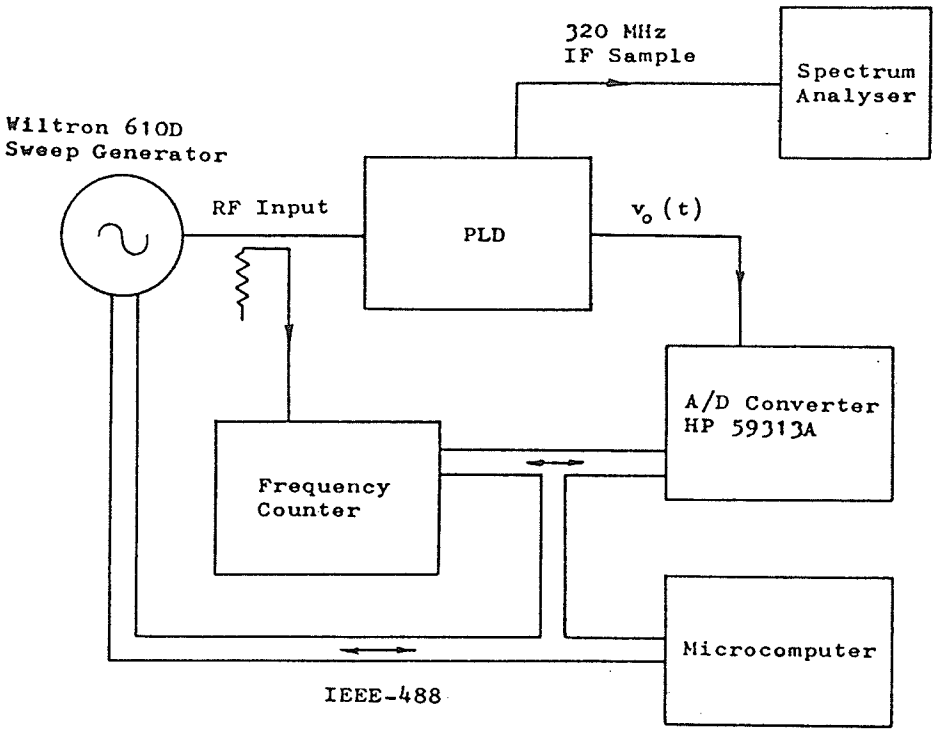


Figure 4.1: Test set-up for static measurements

The set-up in Fig. 4.1 was used to obtain the static loop transfer characteristic. A description of the measurement procedure follows. A microcomputer was instructed to step the frequency of a bus controlled generator from 1300 to 1500 MHz in approximately 0.5 MHz increments. At each point, a frequency counter and 10 bit A to D converter (10 bits plus sign bit) record input frequency and output voltage respectively. The majority of several voltage readings taken over the gate time of the counter was accepted as the true reading. The full scale voltage of the A/D converter

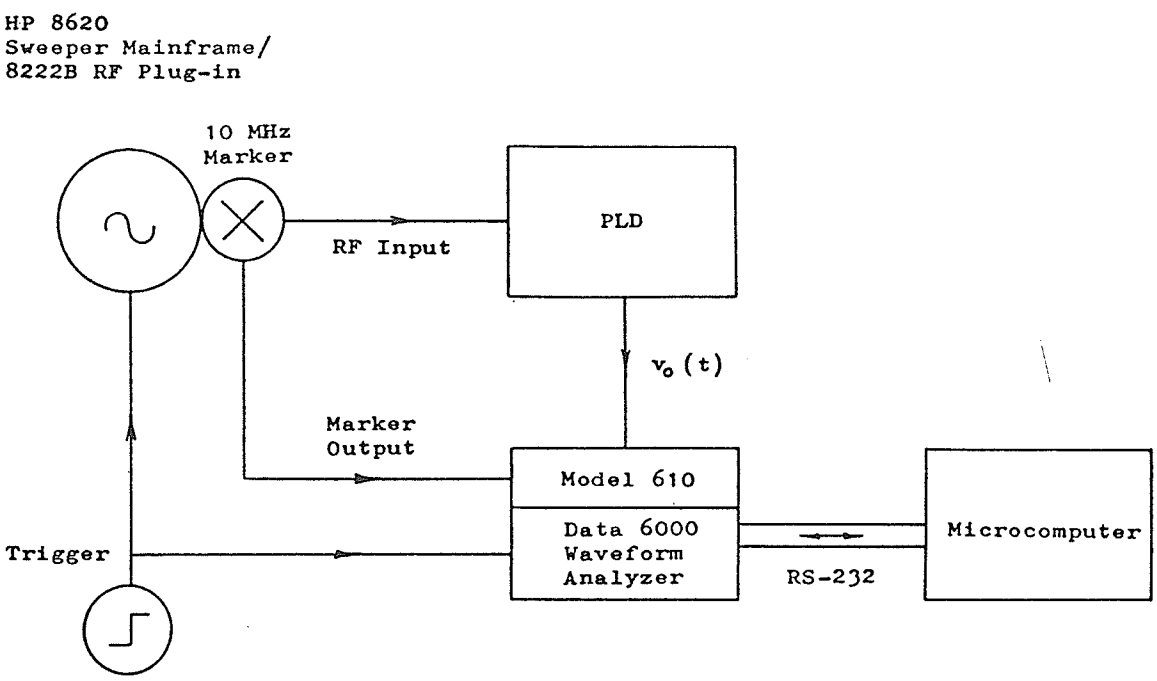


Figure 4.2: Test set-up for dynamic measurements

TABLE 4.1

Disagreement between static and dynamic tests

Point #	Frequency (MHz)
2	1300.5
4	1301.5
11	1305.0
137	1368.0
146	1372.5
365	1482.0
374	1486.5
378	1488.5
385	1492.0
389	1494.0
394	1496.5
396	1497.5
400	1499.5

was ±5 Volts with resulting resolution of 0.00488 Volts. The low frequency noise was well below the resolution of the converter and therefore did not impose any additional constraints on the accuracy or reliability of the measurements. A tolerance on the voltage measurement was set at ±2.5 mV in consideration of the A/D converter resolution. The confidence in the frequency measurement was high within the limits of ±0.1 MHz of the recorded value. The IF frequency was monitored over the entire duration of the experiment to assure that the loop remained locked with the VCO frequency 320 MHz above that of the input signal.

Figure 4.2 depicts the set-up used to determine the transfer characteristic for the dynamic situation. The frequency ramp is applied to the loop by an HP-8620 sweeper mainframe with accompanying 86222B plug-in RF unit. The output of a frequency marker generator (internal to the RF plug-in) was recorded during the ramp to provide accurate frequency information since a linear time-frequency relationship is not guaranteed by the sweeper. The marker generator provides a rectangular pulse (of width ±0.2 MHz about the center frequency) at every 10 MHz of output frequency. The frequency was swept over the range of 1300 to 1500 MHz at a rate of 10000 MHz/second which is the maximum rate allowed by this sweeper and marker generator combination. According to the transient response solutions of the ideal loop (appendix B) this particular loop should track an input frequency ramp with a constant phase error θ_e given by

$$\theta_e = \frac{R_t}{\omega_n^2} \qquad \ldots(4.3)$$

where R_t is rate of change of input frequency. The rate of change of frequency is limited by the maximum range of the phase detector (360×10^3 degrees in this case) which for this loop occurs for an R_t of 2.5×10^6 MHz/second. Since this predicted value is an order of magnitude higher than the frequency ramp applied in this test, there was little doubt that the loop would remain locked. The output voltage was sampled every 20 μs by one channel of a waveform analyzer with a voltage resolution of ±3 mV and an aperture uncertainty of 2 nsec. The second channel of the analyzer recorded the output of the marker generator. The frequency points between the 10 MHz markers were produced through linear interpolation after the data was collected. The frequency error (in measurement) was taken to be ±0.3 MHz after taking into account the total marker pulse width of 400 kHz and the analyzer sampling rate of one point every 20 μs (corresponding to frequency samples 200 kHz apart). The noise voltage at the PLD output spanned a range several times the 1/2 least significant bit (LSB) resolution of the waveform analyzer used for the dynamic measurements, but was well under that of the A/D converter used for the static measurements. Hence for purposes of comparison it is only necessary to assume the worst of the two accuracy limitations which is ±2.5 mV as determined for the static measurements. The center frequency (1478.2 MHz) was subtracted

from each frequency reading of the collected data for the remaining analysis of the results.

4.2.3 Results

In order to aid comparison between the two sets of data as described above, a dc offset between the curves was removed together with some scattered (non systematic errors) points in the dynamic data. A computer program was written to compare the two data sets by initially selecting (since the static test had higher frequency accuracy) a point from the static data set with frequency bounded by f_{LST} , the lower bound as set by the measurement error and f_{UST} , the upper bound. A search is undertaken for a corresponding point in the dynamic data set such that

$$f_{LDY} < f_{LST} \quad \text{and} \quad f_{UDY} > f_{UST} \qquad \ldots(4.4)$$

where f_{LDY} and f_{UDY} are the lower and upper bounds (of the frequency plus error limits), respectively. The voltage output of each set was assumed to have the same tolerance (±2.5 mV) and each point was compared within the constraints of this tolerance. The point number (out of 400) of the static test data set and frequency for each point of non-agreement is listed in table 4.1. These points of disagreement are scattered and no strong trend is seen with respect to frequency. If the tolerance on voltage is increased to ±4 mV then there is total agreement between the two sets of data. Since the disagreement is limited to a small number

of scattered points, the curves are considered identical (at least to the accuracy of these tests) for the remainder of this study.

The method of least squares fitting as discussed by James , Smith and Wolford [23] was applied to the data generated by the dynamic test in order to obtain a smooth fourth order polynomial fit to the data. For M data points selected from the entire set, the five coefficients (C_1 to C_5) of the fourth order polynomial are found by minimizing

$$\sum_{i=1}^{m}(r_i)^2=\sigma_T \qquad \ldots(4.5)$$

for the M residuals r_i as generated from

$$r_i = C_1+C_2v_{0_i}+C_3v_{0_i}^2+C_4v_{0_i}^3+C_5v_{0_i}^4-\omega_{a_i} \qquad \ldots(4.6)$$

where v_{0_i} and ω_{a_i} are the voltage and frequency, respectively, of the i^{th} point. A readily available computer program [23] was applied to 10 points of the data. As an additional constraint to (4.6), the data points selected for the fit were to agree within the specified tolerances of ±0.3 MHz for the input frequency and ±0.0025 volts for the output voltage of the PLD. The selection of the 10 points was made on the basis of best fit although an attempt was made to space them uniformly throughout the entire set of data. Coefficient C_1 was set to zero before the fitting procedure. The following polynomial fit resulted for ω_a in MHz and v_0 in volts.

$$v_0(\omega_a)=4.040\times10^{-3}\omega_a+6.813\times10^{-6}\omega_a^2 +2.938\times10^{-8}\omega_a^3+5.327\times10^{-11}\omega_a^4 \qquad \ldots(4.7)$$

All the points of the data set were checked for agreement with (4.7) and all but a scattered 1% were found to fit within the tolerances specified at the onset of the fitting procedure.

The IF frequency of 320 MHz was added to the loop input frequency for each point in the original (before subtracting ω_c) data set to yield the the VCO frequency as a function of control (PLD output) voltage. A similar fitting procedure to that just described is applied to this new set of points but now with the VCO frequency, ω_0 as a function of voltage. The resulting VCO transfer characteristic equation is

$$\omega_0(v_0) = 1798.2 + 259.77v_0 - 34.178v_0^2 + 31.632v_0^3 + 6.6676v_0^4 \quad ...(4.8)$$

with error of ±1.3 MHz if a 'worst case' VCO gain of 400 MHz/volt is assumed. Differentiating (4.8) with respect to voltage yields the VCO gain as a function of v_0 (as per (4.2))

$$K_0(v_0) = 259.77 - 68.356v_0 + 94.896v_0^2 + 26.670v_0^3 \quad ...(4.9)$$

This function is needed for the computer simulations. The PLD transfer characteristic equation (4.7) and VCO gain (4.9) are plotted over the test frequency range and are presented in Fig.s 4.3 and 4.4, respectively.

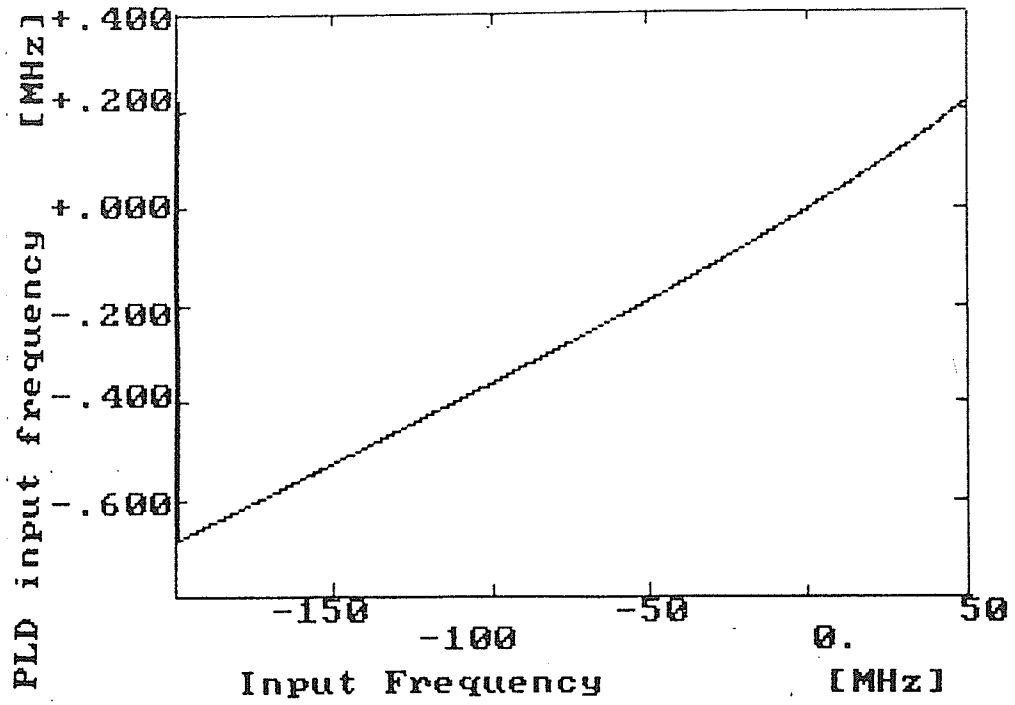


Figure 4.3: PLD transfer characteristic

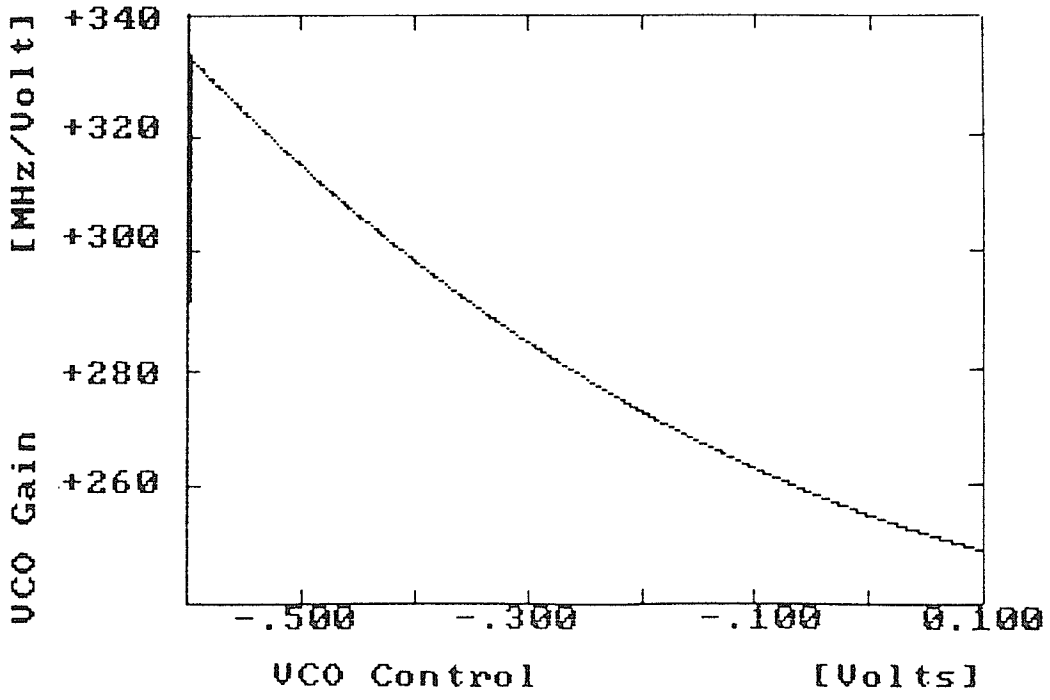


Figure 4.4: VCO gain as a function of control voltage

4.3 FREQUENCY STEP RESPONSE

4.3.1 Objectives

The measurements described in this section permit recording the PLD voltage output and loop phase error (θ_e) immediately following the application of an input frequency step. The ultimate objective will be to compare this response to that predicted by the computer based PLD simulator. Unfortunately, this particular PLD cannot remain locked following a frequency step of the minimum size available for this experiment with the result that the loop becomes unlocked at some point during the transient response. Rather than redesigning the loop to fit the experiment (increase ω_n) it was decided to record both the linear and non-linear (unlocked) portions of the response and continue with the planned comparison as described in section 4.4.

4.3.2 Experimental Method

The set-up shown in Fig. 4.5 was used to generate an ideal frequency step and record the subsequent response of the loop. A CW signal is applied to the input of the PLD and the reference frequency and hence IF frequency is set to 160 kHz by application of a TTL '1' to the RFS control line (as described in section 3.3.3). The abrupt frequency step of 160 kHz is obtained by changing the RFS control line from a logical '1' to a '0' thereby doubling the reference clock frequency. The applied frequency step is considered ideal insofar as the low frequency (PFD-filter) section of the

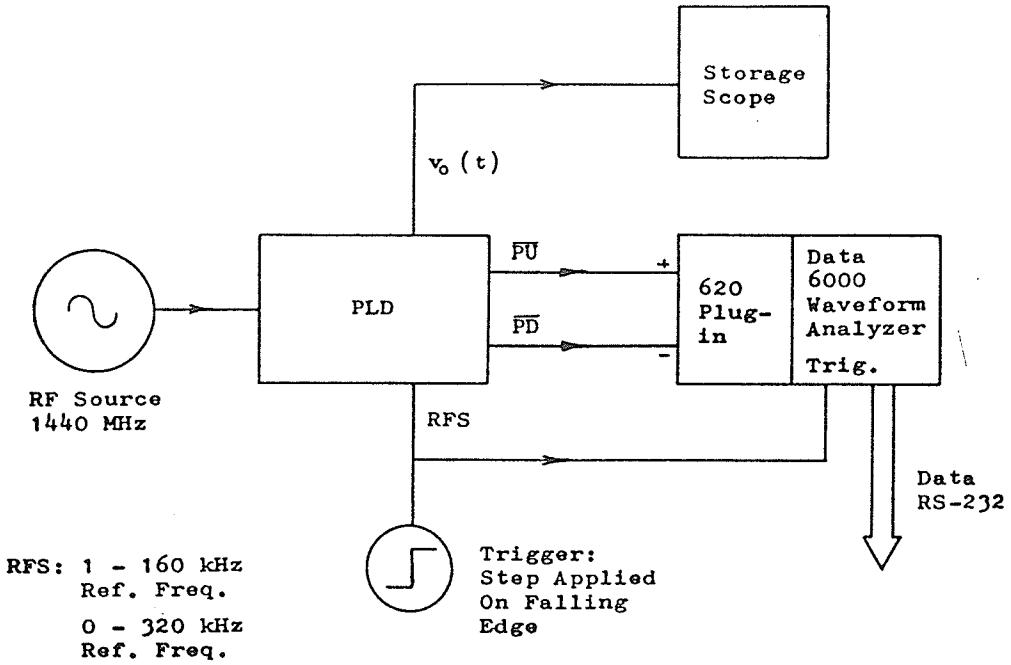


Figure 4.5: Set-up to measure frequency step response

loop is concerned since the step occurs over the period of one reference clock cycle (the smallest interval of time over which the phase is sampled). The transient response will be that of a loop operating at 320 kHz since the response is recorded after the frequency step has occurred. The input frequency remained at 1400 MHz during the test and the VCO frequency started at 1600 MHz (with v_0 =-0.7 Volt ±0.025 Volt) and tended toward 1760 MHz (v_0 =-0.15 Volt) as the transient response died out. The voltage output of the PLD was recorded on a storage oscilloscope and photographed. The phase error was indirectly obtained by measuring the differential voltage between the pump-up and pump-down lines

of the PFD on a waveform analyzer. This data was sent to a microcomputer and the relation

$$\frac{\theta_e}{N} = \frac{\text{active pump time}}{\text{period of reference signal}} \times 360 \qquad \ldots(4.10)$$

was used to calculate the phase error magnitude. The sign of the phase error is the same as the sign of the differential pump voltage. The model 620 plug-in was used with the Data 6000[4] to sample the pump lines over approximately 260 μs with points spaced 200 ns apart. The input voltage range to the analyzer was ±3.6 Volts with a 30 mV resolution. The signal was passed through an internal analyzer filter with a 20 MHz cut-off. The minimum phase error resolution of this arrangement is obtained by substituting 200 ns (the sample time) into (4.10) and is 23 degrees. The pump lines were also monitored by the storage scope and the traces photographed to further illustrate the operation of the PFD.

4.3.3 Results

[4] A waveform analyzer manufactured by the Data Precision Division of Analogic Inc.

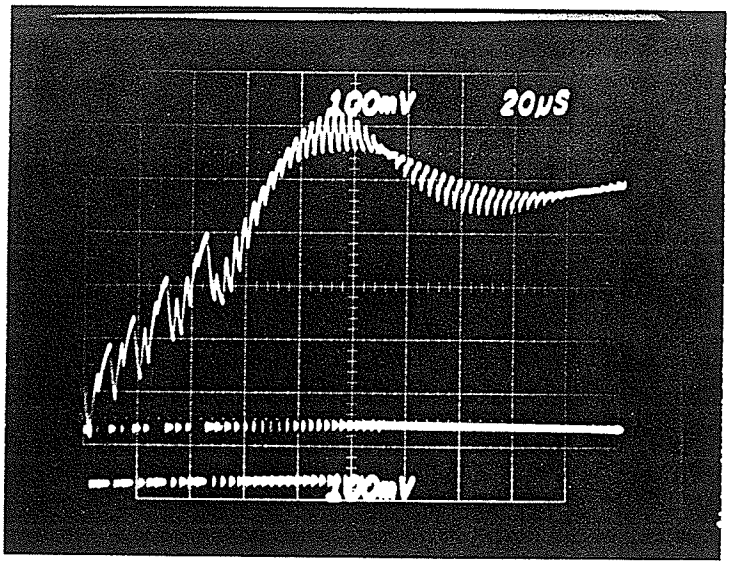


Figure 4.6 (a): PLD output (top), pump-up line (bot.)

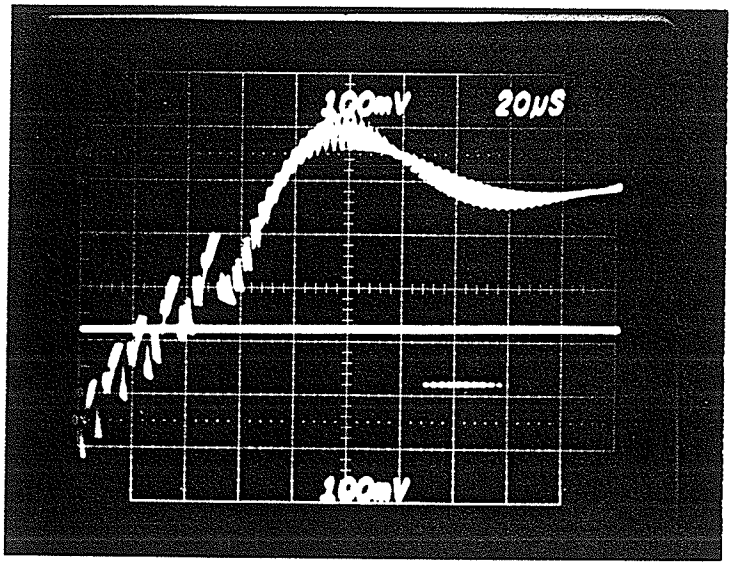


Figure 4.6 (b): PLD output (top), pump-down line (bot.)

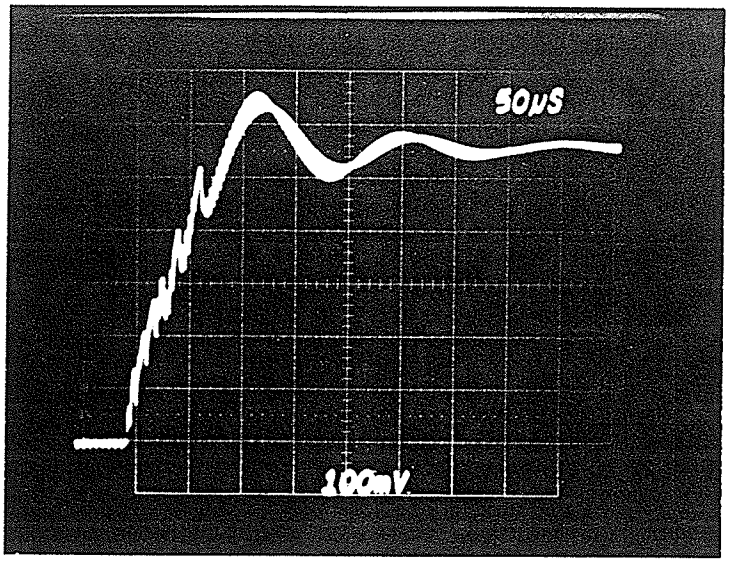


Figure 4.7 (a): PLD output, 0.5 damping

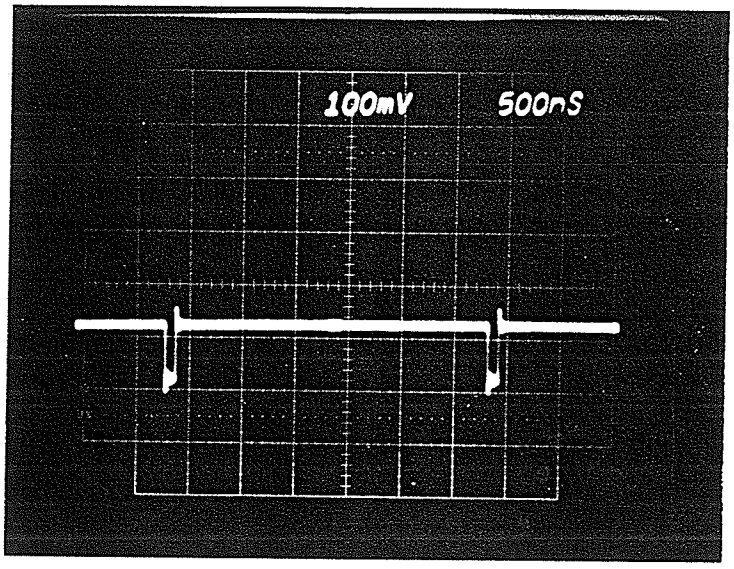


Figure 4.7 (b): pump-down signal for static lock

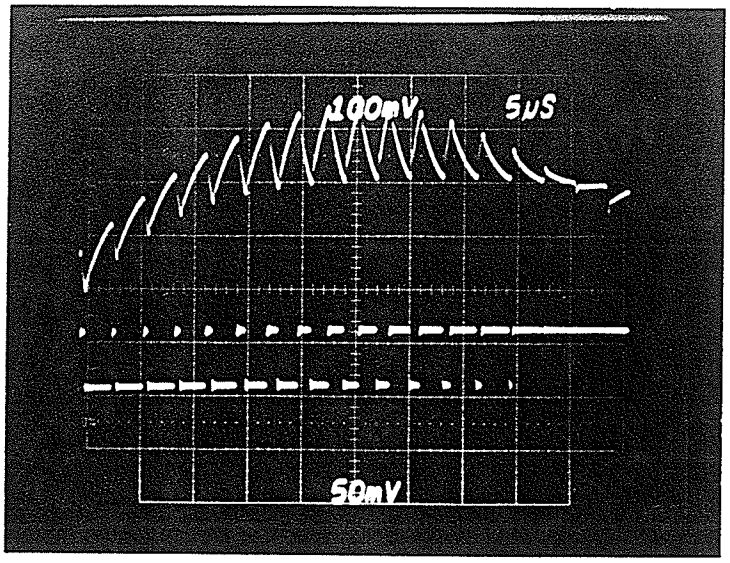


Figure 4.8 (a): PLD output (top), pump-up line (bot.)

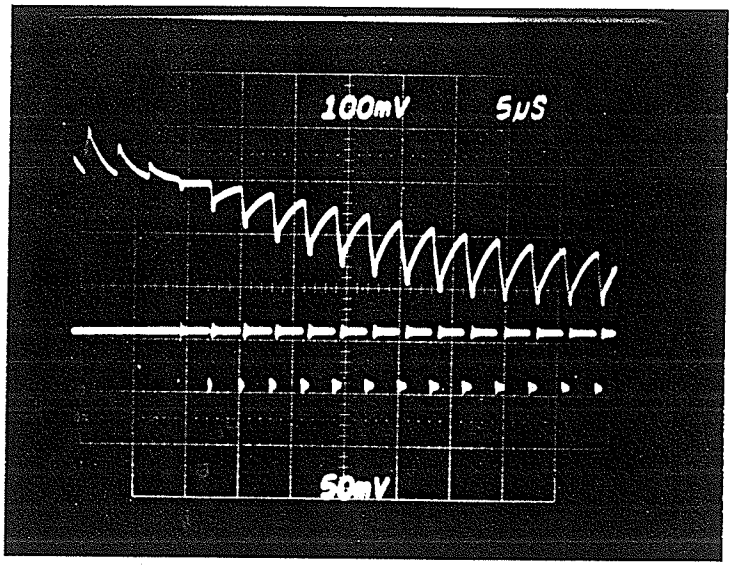


Figure 4.8 (b): PLD output (top), pump-down line (bot.)

The output waveforms of the PLD as recorded by the storage oscilloscope are displayed in Fig.s 4.6 to 4.8. The PLD output (top trace) of a loop with damping factor of 0.83 is shown along with the voltage waveform of the pump-up line (bottom trace) in Fig. 4.6 (a) and similarly for the pump-down line (bottom trace) in Fig. 4.6 (b). The zero volt reference for the top trace is set at the second grid line from the top. The step is initiated at the time represented by the leftmost edge of the oscilloscope grid but the loop does not return to lock until approximately 60 μs afterwards. The unlocked condition is recognized by the long width pulses observed during the rising edge of the voltage waveform (as demonstrated in ch. 2.6). The PLD output for a damping factor of 0.5 is shown in Fig. 4.7 (a). The zero volt reference is set at the top grid line in this case and the horizontal time scale was changed from that of Fig. 4.6.

Figure 4.7 (b) shows activity on the pump-down line (the pump-up line is inactive) as the loop remains locked on a CW input signal which means that a static phase error exists, causing the variable (V) input to the PFD to lead the reference (R) input. The magnitude of this error is 12 degrees from (4.10). This residual phase error is likely caused by a dc offset inherent in the loop filter [11],[19]. This error can be removed by applying bias to the operational amplifier [19], however, a small phase error offset does not seriously affect the operation of the PLD hence no such action was taken.

The photographs of Fig. 4.8 depict detailed views of the activity change from the pump-up (bottom trace of Fig. 4.8 (a)) to the pump-down line (bottom trace of Fig. 4.8 (b)) during the frequency step response for a loop with damping factor of 0.83.

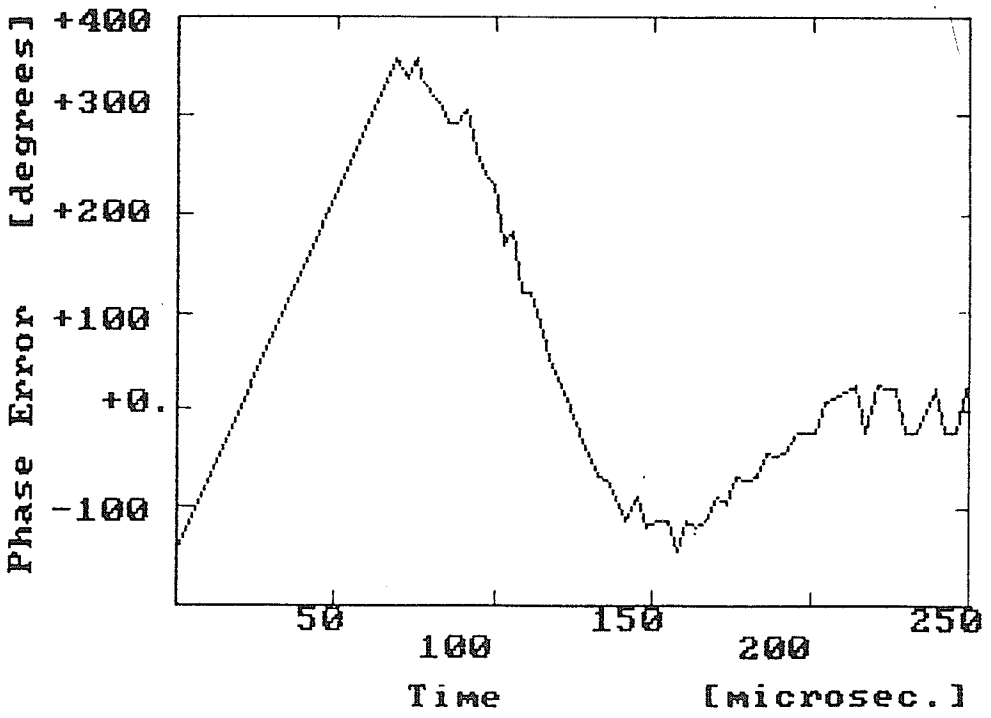


Figure 4.9: Phase error at the PFD for a frequency step

The phase error divided by the IF frequency division ratio N appears as a plot in Fig. 4.9. All points below about 60 μs are meaningless as the loop is unlocked during this phase of the response. The plot is rather crude owing to the 23 degrees resolution of the data but still yields information as to the approximate overshoot, zero crossings, etc.

4.4 EXPERIMENTAL AND SIMULATED RESPONSE COMPARISON

4.4.1 Introduction

This section compares results of the transient response tests reported in the last section to predictions of the computer based loop simulator as it emulates the experimental conditions and loop under test.

The loop was designed (section 3.3.2) on the assumption that the loop gain was a constant value of 280 MHz/Volt whereas according to Fig. 4.4, it varies from 270 to 345 MHz/Volt. In order to accurately model the frequency step response, the PLD simulator was modified to run with a non-constant VCO gain. The term $K_0 v_0 (t+\Delta t)$ in (2.42) is replaced by

$$K_0 v_0 (t+\Delta t) = \int_0^{v_0(t+\Delta t)} K_0 (v)\ dv \qquad \ldots(4.11)$$

where $K_0(v)$ is obtained from (4.9). The integration is performed analytically before insertion into the program.

The simulator will model the transient behavior of the long loop by emulating a basic single stage loop providing:

1. the natural loop frequency (ω_n) and damping factor of the two loop filters are identical and
2. the input frequency to the single loop immediately following the start of the step and after the transients have died out is identical to the IF frequency of the long loop for the respective times.

The VCO transfer characteristic of the long loop must be divided by a factor of 1000 (the IF frequency division ratio, N) before application to the basic loop in order to satisfy the above two conditions. Although the dynamic behavior of the two loops will be identical, the output waveform of the experimental loop will be inverted if the image response of the heterodyne front end (response #2 in section 3.2) is selected and a dc offset of the PLD output voltage may exist depending on the choice of VCO rest frequency for the simulated loop.

The loop filter component values selected for the simulation were identical to those for the loop under test in earlier sections (see section 3.3.2). The applied step to the simulated loop was 160 kHz which is the step size at the IF frequency seen by the experimental loop. The VCO rest frequency (359.85 kHz) was selected to provide identical dc offset between the simulated and measured outputs.

4.4.2 Results

The plots of Fig. 4.10 and Fig. 4.11 are of the demodulator output voltage (simulated) versus time for damping factors of 0.83 and 0.5 respectively, after the input frequency step was applied at t=0. The plot axis were chosen to be similar in magnitude to the respective photographs in Fig.s 4.6 (a) and 4.7 (a). Comparison between the simulator plots and corresponding photographs reveal excellent agreement between predicted and measured waveforms.

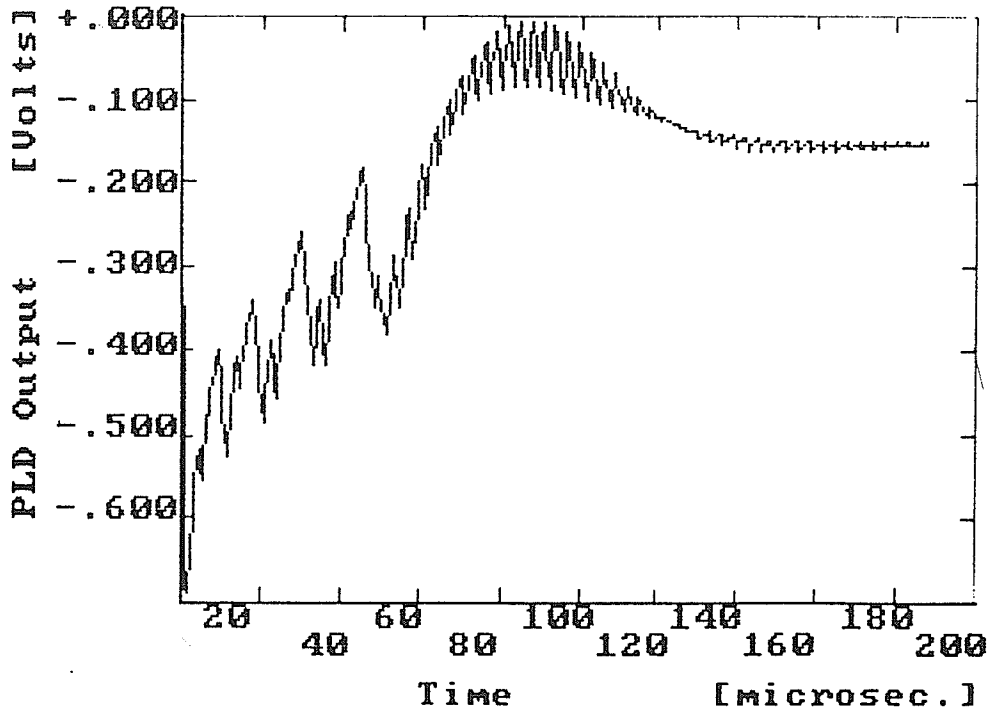


Figure 4.10: PLD voltage output, 0.83 damping

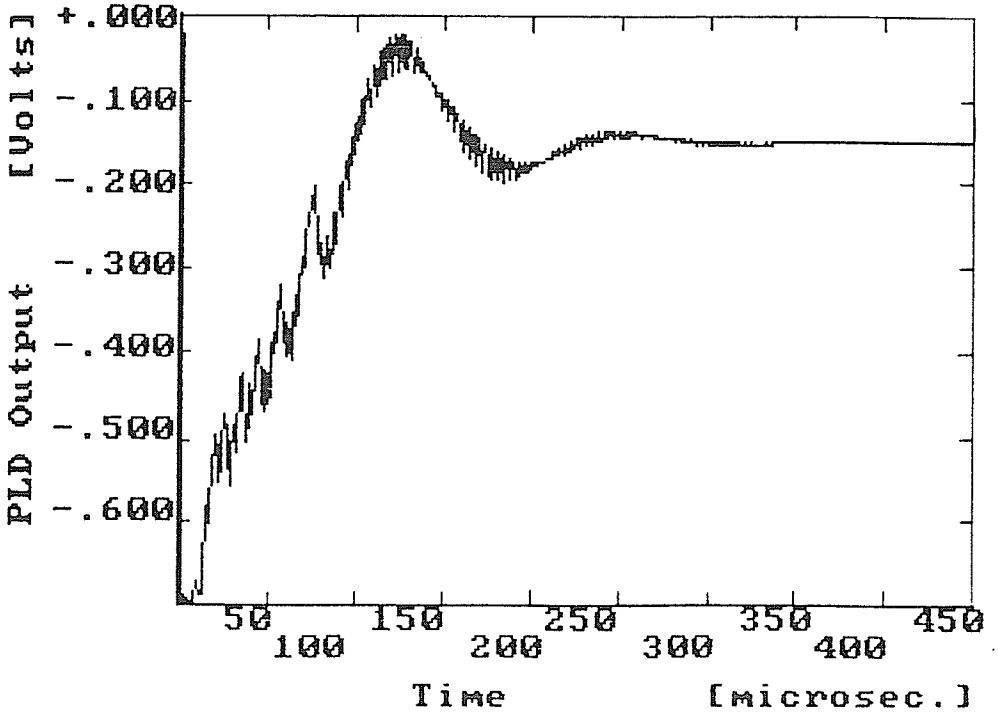


Figure 4.11: PLD voltage output, 0.5 damping

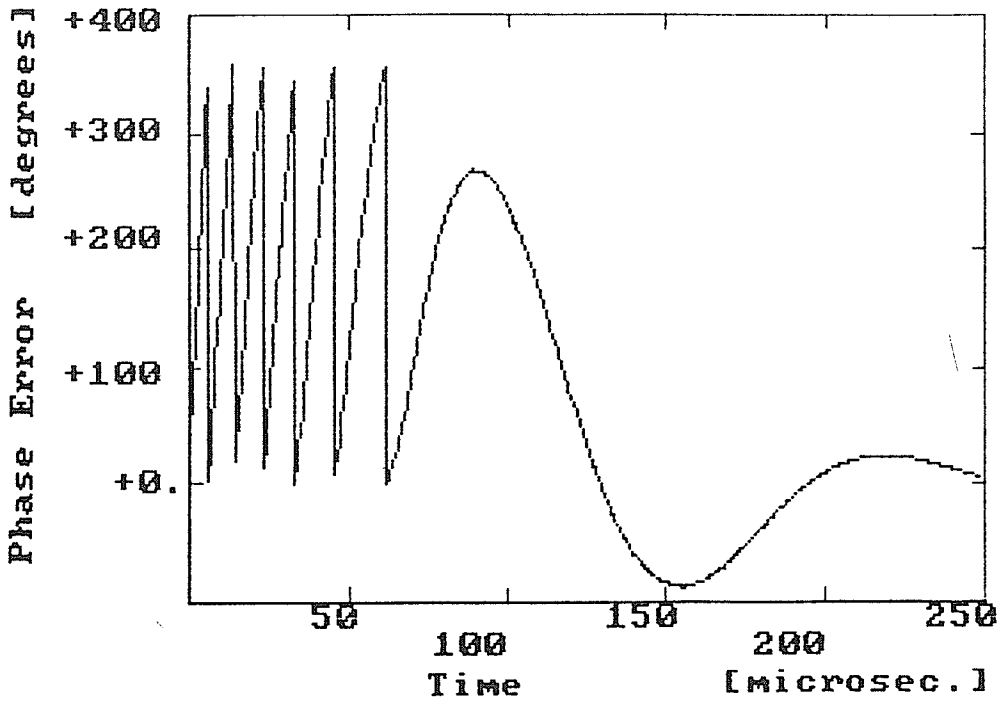


Figure 4.12: Phase error, 0.5 damping

The plot of Fig. 4.12 is the phase error for the simulated experiment. It must be kept in mind that the phase error of the basic loop is being compared to the phase error after frequency division as seen by the PFD within the long loop. The phase error at the PFD is one thousandth that of the phase error between input and VCO phases as defined in (2.3). It is difficult to compare the initial phase error maximum (at approximately 80 μs) to the corresponding measured phase of Fig. 4.9 because of the uncertainty in the exact phase error trajectory during the acquisition phase of the response. However, the two plots show good agreement well into the locked phase (after 100 μs).

4.5 SIGNAL ACQUISITION TEST

4.5.1 Objectives

Acquisition of lock was demonstrated in the section on transient response since the PLD became unlocked during the initial phase of its response to an input frequency step. A situation where the loop becomes unlocked but loss of input signal (LOS) does not occur was described in ch. 3.2. The experiments of this section further explore the PLD behavior by simulating an LOS condition and observing the action of the loop both during the LOS condition and immediately after the signal is re-applied. The loop behavior should follow predictions of section 3.2 regarding VCO sweep direction and of section 2.4 regarding VCO sweep rate. This acquisition sequence takes place over a longer period of time then during the step response thereby allowing a better examination of sweep behavior of the VCO during the acquisition process.

4.5.2 Experimental Method

The experimental set-up for simulating an LOS condition is shown in Fig. 4.13. Upon resetting the trigger circuit, the VCE control line (see section 3.3.3) is set to a TTL logical '1' (disabling the variable (V) channel to the PFD) thereby simulating the LOS condition. The trigger circuit maintains this state until it is set by the comparator after which time the VCE line voltage is returned to a logical '0', the V channel is restored and the acquisition process initiated. This sequence can be repeated only by resetting the trigger

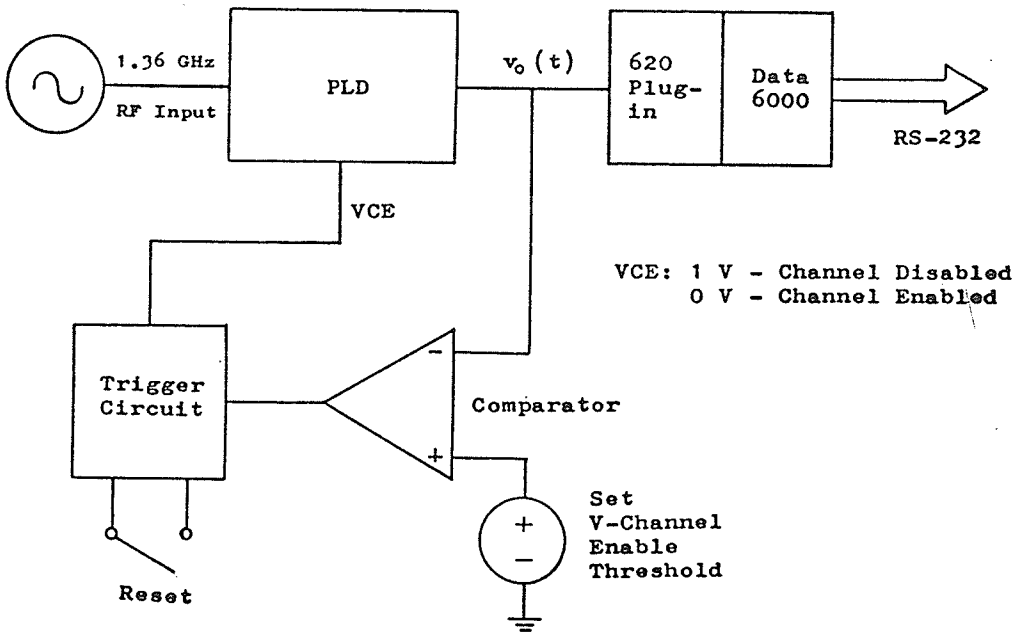


Figure 4.13: Test Set-up for Acquisition Study.

circuit. Once the LOS condition is generated (by resetting the trigger circuit), the integrator output voltage begins to rise and the VCO will sweeps in the direction predicted in section 3.2. The above scheme prevents integrator saturation by initiating the acquisition process before saturation occurs. A voltage comparator monitors the PLD output and sets the trigger circuit (initiates the acquisition process) when the output and hence VCO frequency reach a predetermined threshold. The comparator reference was set to approximately 4 Volts (corresponding to 1920 MHz).

The PLD output was sampled each 1.0 μs by the (model 620 plug-in) waveform analyzer. The input range of the analyzer was ±1.2 volt (10 mV resolution).

4.5.3 Results

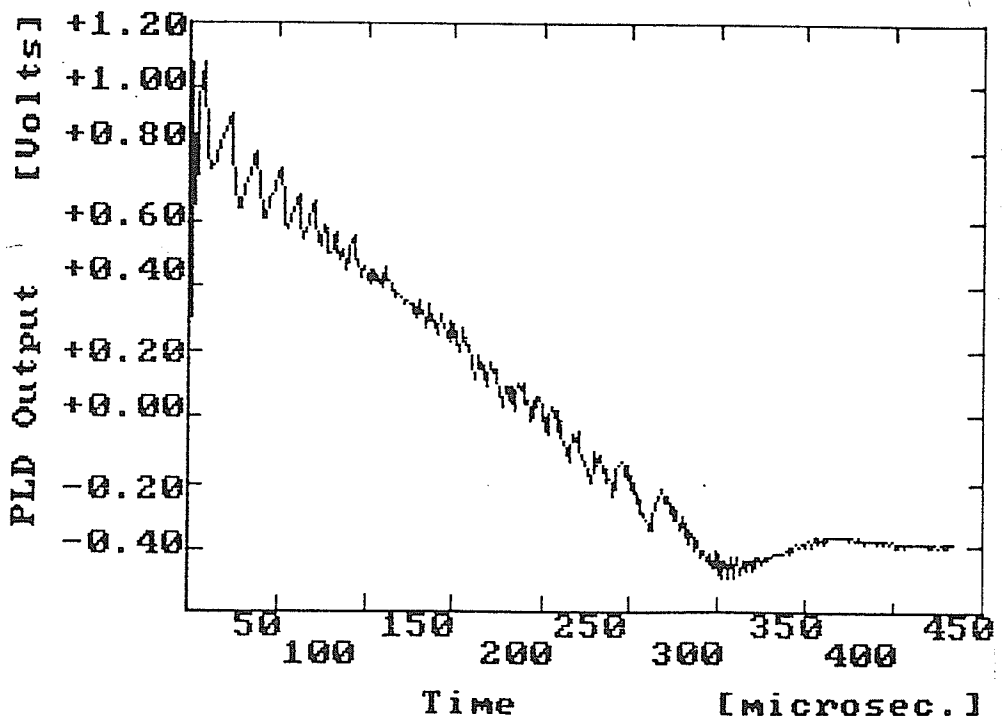


Figure 4.14: PLD output during acquisition test

The PLD output as recorded by the waveform analyzer is displayed in Fig. 4.14. The V channel is restored at t=0 in the plot. The PLD output continued to rise for a short interval of time after the signal was restored resulting in the overshoot above the 4 volt trigger level at t=0. It should be noted at this point that the VCO gain decreases

after 1900 MHz rendering the equations derived from curve fitting in the previous sections inaccurate at times near the onset of the acquisition process. As a result, no conclusion regarding the VCO frequency based on the PLD output voltage can be made (without further analysis of the VCO transfer characteristic) for times less than 100 μs corresponding to frequencies above 1920 MHz in Fig. 4.14.

Table 3.2 predicts correct VCO sweep direction during LOS conditions (on the basis of this experiment) given the PLD to be of response type 1 as in table 3.1. Upon return of the signal, the VCO sweeps toward its locked frequency with a rate of 1.2×10^6 MHz/second based on a VCO gain of 300 MHz/volt and slope as determined by points at 100 and 250 μs in Fig. 4.14. This value compares favorably with 1.31×10^6 MHz/second as predicted by (2.34) where a VCO gain of 300 MHz/volt was assumed.

4.6 DETERMINATION OF DYNAMIC RANGE

4.6.1 Objective

This section describes a simple experiment which provides rudimentary guidelines for the expected dynamic range of the PLD in a current measurement system. The dynamic range of a transducer is the ratio of the largest measurement possible over the smallest usable measurement and is often expressed in decibels. The largest current magnitude that can be monitored by this system is dependent on the current frequency

and is limited by the occurrence of unacceptable distortion of the waveform or loss of lock (determined by the maximum dynamic range of the phase detector and VCO). The maximum expected input current is specified at the onset of the design and therefore becomes the maximum limit to the system. The minimum useful current magnitude measurable by this system is taken to be 20 dB above the noise and is therefore determined by the noise floor of the PLD. This PLD noise level is the subject of this section.

4.6.2 Experimental Method

An RF signal generator is frequency modulated with a sine-wave of frequency 400 Hz and frequency deviation of 10 MHz. The generator output is applied to the PLD. The output of the demodulator is passed through a low noise amplifier-filter combination[5] to a HP 3400A true rms voltmeter. The signal plus noise over noise ratio [(S+N)/N] is found by recording the rms output of the PLD with modulation applied to the signal generator and then dividing this quantity by the rms output with zero modulation applied to the generator. This measurement assumes that the noise of the PLD is independant of the input signal frequency deviation.

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[5] The device was a low noise preamplifier manufactured by the Princeton Applied Research Corporation with the model designation PAR 113.

The filter has selectable lower and upper cut-off frequencies which shall be designated f_L and f_U respectively. The filter was also removed at one point to allow for a full 1 Hz to 10 MHz (limited by the voltmeter) band.

4.6.3 Results

TABLE 4.2

PLD noise measurement results

Damping	rms noise voltage (mV)	f_L	f_U	[(S+N)/N] (dB)
1.0	1.8	1 Hz	10 MHz	24
0.5	1.3	1 Hz	10 MHz	27
1.0	.055	1 Hz	3 kHz	54
0.5	.055	1 Hz	3 kHz	54
1.0	.030	10 Hz	3 kHz	59

The rms noise output of the PLD and corresponding [(S+N)/N] is shown in table 4.2 for selected filter cut-off frequencies and damping factors. The PLD output corresponding to the applied modulation is 27 mV rms.

The experiment reveals considerable noise above 3 kHz which is expected to be the pump pulse energy at 320 kHz and multiples thereof. The maximum expected deviation applied to this loop (Chapters 1 and 2) is 200 MHz (26 dB above the test signal level). It follows that the dynamic range of

this PLD for an output band bounded by 10 Hz and 3 kHz is 65 dB if a minimum usable output level is 20 dB above the noise.

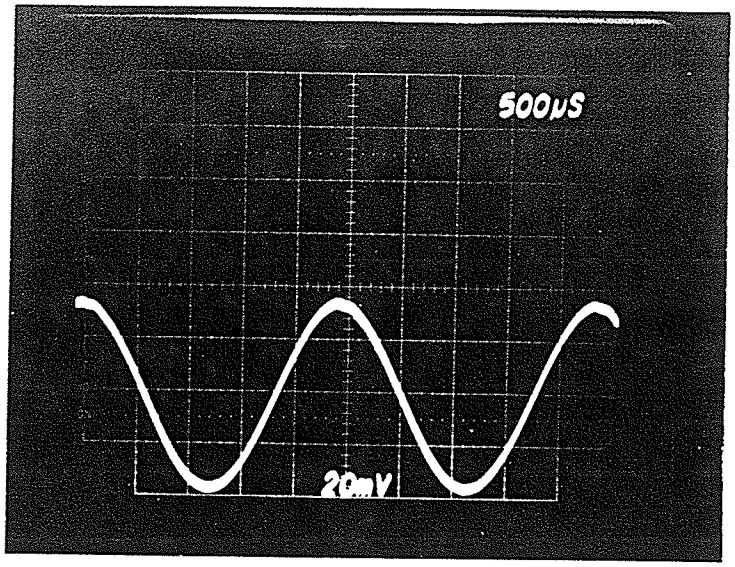

Figure 4.15 (a): unfiltered PLD output

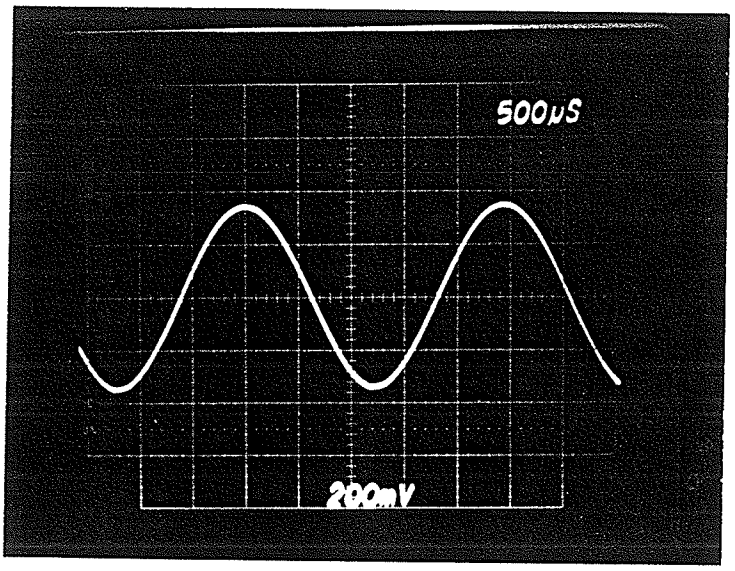

Figure 4.15 (b): PLD output after 3 kHz low-pass filter

Figure 4.15 is a photograph of the output waveform for both the filtered and unfiltered case (3 kHz and 10 MHz bandwidth respectively).

Chapter V

CONCLUSION

5.1 INTRODUCTION

The objectives of this thesis were to

1. evaluate the potential of the PLD to fulfill the requirements of its role within an unconventional CT employed in the service of
   a) metering
   b) protection and transient analysis
   c) monitoring GIC ;
2. compare its performance to the delay line discriminator of earlier implementations;
3. provide some design tools and suggestions to aid in further development of the PLD.

5.2 APPLICATION OF THE PLD

5.2.1 Metering service

The applicability of the PLD for use in a CT designed for revenue metering shall now be considered. Appendix A contains a summary of performance criteria required of a CT employed in this service and further discussion will be based on these specifications.

The metering class device is required to exhibit very high accuracy over a frequency range of 20 to 100 Hz (covering only the fundamental power line frequency). The accuracy of the PLD (for both phase and amplitude) is of prime importance in this service. Equation (2.23 (b)) (and Fig. 3.4) predicts that the PLD output will lag the phase of the modulating signal by less than 0.003' for a modulating (sinusoidal) frequency of 60 Hz. This is well under the allowed 10' maximum stated in the appendix. Similar performance is exhibited for amplitude as the loop transfer function (2.23 (a) and Fig. 3.4) shows no significant deviation from unity for modulating frequencies ranging from zero to 0.1 ω_n. Hence, the (ideal) loop design is fully capable of meeting the accuracy requirements of the metering service. The accuracy of the actual PLD will be determined by the transfer characteristic of the VCO which is reflected by the PLD transfer characteristic of (4.7).

The accuracy of a metering class CT is expressed in terms of the ratio correction factor (RCF in Appendix A). The coefficient labeled C_2 in (4.7) is analogous to the marked ratio (Appendix A) of a conventional CT and working on the assumption that this VCO is either typical or a worst case example, an expression for RCF in terms of the PLD transfer characteristic coefficients shall now be developed and a statement made regarding the accuracy of the PLD. Consider a signal of instantaneous frequency, $\omega_i(t)$ applied to the input to the PLD such as

$$\omega_a(t) = \Delta\omega_i \cos(\Omega t) \qquad \ldots(5.1)$$

Furthermore, it is assumed that the center frequency ω_c, (4.1) is fixed so that the VCO operates consistently over a well defined range of its transfer characteristic. Substituting (5.1) into (4.7) and considering only those terms involving the fundamental frequency yields

$$v_0(t) = \Delta\omega_i \left[C_2 + \frac{3C_4\Delta\omega_i^2}{4}\right]\cos(\Omega t) \qquad \ldots(5.2)$$

where C_2 and C_4 are coefficients of (4.6). The linear term coefficient, C_2 is analogous to the ideal secondary to primary current ratio (marked ratio) of a conventional CT The RCF is then given by

$$RCF = \frac{3C_4\Delta\omega_i^2}{4\ C_2} \qquad \ldots(5.3)$$

For a 1.2 per unit deviation of 12 MHz, (5.3) yields an RCF of .0008 or .08% (using the coefficients of (4.7)). This compares favorably with the 0.1 % RCF required for this application. Although the transfer characteristic was generated by a rather crude fit to the data (ch 4) it is assumed that the relative magnitudes of the coefficients of a smooth fit over the entire range of points collected will closely represent those of a true fit over the much smaller range considered here. This approach is partially justified by further knowledge of the mechanics of VCOs [17]. These devices (VCO) will typically exhibit a smooth, well behaved transfer characteristic (suitable for a polynomial fit) over a significant (30 to 60 %) part of their tuning range.

The treatment of accuracy has been superficial, however it can be stated that the PLD as designed in ch 3 will meet the requirements of metering service if

1. a VCO with a transfer characteristic similar (relative magnitudes of non-linear coefficients) to that of (4.7) is provided for the designer and
2. according to (5.3), the deviation at 1.2 per unit is selected to be no larger than necessary to satisfy S/N and range requirements.

5.2.2 Protection service

The PLD was found in Ch 4 to have a dynamic range of 55 to 60 dB (for a minimum S/N ratio of 20 dB and depending on the bandwidth) which compares favorably to the requirements of Appendix A (42 dB for a minimum S/N of 20 dB or a maximum current reading that is 62 dB above the noise floor). A large dynamic range is seen to be a feature of this measurement system.

The usable bandwidth for protection service is determined from (4.23 (a)) or Fig. 3.4. The upper frequency limit is met when the magnitude of the loop transfer function (4.23) deviates from unity by the allowed RCF (5%). This occurs for a modulating frequency of 2 kHz (transfer function of 1.05) for this loop. This bandwidth meets the minimum suggested for unconventional CTs. The allowed phase lag between the current and PLD output voltage waveforms at the maximum current frequency is given by

$$50\mu s > \frac{|\phi_0 - \phi_i|}{360\Omega} \qquad \ldots(5.4)$$

where Ω is the current frequency in Hz, ϕ_0 and ϕ_i are the output and input phases. The phase lag due to the VCO pre filter (RC filter) is found from [13]

$$\phi(\Omega) = -\text{TAN}^{-1}(\Omega RC) \qquad \ldots(5.5)$$

The phase lag of the ideal PLD output is found from (4.23 (b)) to be 1.3 degrees at 2 kHz and the lag due to the RC VCO pre-filter was found from (5.5) to be 1.9 degrees. The total phase lag is the sum of these two and easily meets the condition of (5.4). Hence, the PLD meets the bandwidth requirements of protection service.

A brief evaluation of accuracy as in the section on metering will now follow. Accuracy for a protection CT is specified in terms of the composite error (appendix A) which is the RMS value of the difference between the instantaneous values of the ideal and actual CT outputs. The composite error is expressed in percentage of the actual rms CT output. Neglecting phase lag, the composite error of the PLD transfer characteristic (4.7) is given by

$$E_c = \frac{100}{v_{0_{rms}}} \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (C_3 \Delta\omega_i^2 \text{COS}^2 t + C_4 \Delta\omega_i^3 \text{COS}^3 t C_5 \Delta\omega_i^4 \text{COS}^4 t)^2 \, dt} \qquad (5.6)$$

where $v_{0_{rms}}$ is the rms value of the actual PLD output. Equation (5.6) was evaluated numerically by use of the trapezoidal integration scheme and the coefficients were those

of (4.7). The composite error was found to be 17% for a frequency deviation of 100 MHz which is substantially greater than the allowed 3% error. Reducing the deviation to 50 MHz results in an 8% error. The specification can be met if the deviation is further reduced to 10 MHz resulting in a composite error of 1.5%. These results should be treated with caution as the effects of the loop transfer function (2.23) on linearity were not taken into account.

The specification proposed for maximum turn on time of the CT is 2 msec. This parameter is represented in the case of the PLD by the acquisition time following an LOS condition. The total time for acquisition to occur and the transients to have died away was found experimentally to be less than 0.4 msec. in ch 4 (Fig. 4.14). The acquisition time may vary depending on initial conditions (Ch 2) however the measured value above is still 1/5 of that allowed thereby providing the necessary headroom.

To summarize this subsection;

1. the PLD implemented exhibits adequate S/N and dynamic range performance for protection service,
2. the bandwidth of this loop meets the minimum requirements for protection but with no excess,
3. acquisition time is adequate and since it is decreases with increasing bandwidth (Ch 2), improvements in the bandwidth as suggested by the previous point will only improve the acquisition performance,

4. the accuracy requirements are not met with the PLD built around this particular VCO. A VCO with better linearity over a large tuning range is required. Some compromise is offered as the large dynamic range of this demodulator allows for a decrease in maximum deviation (perhaps to below 50 MHz) which in turn lessens the demand placed on the VCO design.

5.2.3 Geomagnetically induced current monitor

Standards for the monitoring of GIC neither exist nor have been proposed at this time making it difficult to assess the effectiveness of the PLD for this application. Specifications for past GIC monitoring programs [7] required an amplitude range of 10 Amp to 200 Amp with a frequency response of 1 mHz to 100 mHz. The lower frequency and amplitude limits are set by thermal drift associated with HPU components. Although the noise floor of the PLD was not measured below 1 Hz, it is expected that the low frequency noise (thermal drift) of the HPU will limit the dynamic range and bandwidth of the system. However, the effects of this noise are minimized by designing the HPU for maximum sensitivity (that is to say, maximum deviation is achieved for 1 per unit current) which contradicts the range requirements for protection and according to (5.2) threatens the accuracy for metering applications. Furthermore, the predictions of accuracy following (5.2) assume that the VCO is modulated about some center frequency which is held constant. A GIC

superimposed on the metered line current will shift operation of the VCO to a different section of its transfer characteristic with a resulting degradation of accuracy. Hence, for GIC measurement service,

1. The limitations on dynamic range and frequency response for a GIC monitor are determined by the HPU and not the PLD;
2. the functions of a GIC monitor and metering are not compatible as a single system on the level of the PLD (although both functions are possible by a single HPU);
3. it seems unlikely that the task of protection and GIC monitoring could be assumed by a single unit on the HPU level (although this is not a limitation of the PLD).

5.3 GENERAL CONCLUSIONS

Some general conclusions resulting from this program follow.

1. Performance of the PLD is ultimately determined by the VCO specifications, the most important of which are tuning bandwidth, tuning range and tuning linearity. Greater tuning bandwidth and wider linear tuning range over that of the VCO considered here is necessary for adequate protection performance.
2. The PFD functions well in the service of very wide deviation, strong signal (RF level well above the noise level) FM demodulation.

3. The computer based loop simulator introduced here is a useful design and analysis tool for this type of PLD. Although calculator programs [15] have been introduced to model the PFD in a locked loop, none have been found to rigorously emulate the loop under both locked and unlocked conditions. Moreover, the addition of the VCO pre-filter in a loop using a PLD has not been simulated elsewhere although programs for the third order locked loop are under development [15].
4. The PLD out performs the delay line discriminator in terms of dynamic range. This large dynamic range provide the option of combining the functions of protection and metering in one system.
5. The PLD exhibits similar linearity over a wide frequency range (large deviation) to the delay line discriminator. Furthermore, the large dynamic range and ability to control the center frequency of the PLD with respect to the VCO rest frequency (by control of the reference frequency) provides the designer with the option of choosing the range of the VCO transfer function with which to operate over. This greatly enhances the accuracy potential of the PLD for small deviation input signals (metering) over that of the discriminator.
6. The frequency response of the PLD is adequate but could use further improvement. The delay line dis-

criminator on the other hand has excellent frequency response and exhibits no significant turn on (acquisition) time. It is unlikely that the PLD will ever out perform the discriminator in this area.

5.4 RECOMMENDATIONS

The following points are recommendations to be considered if further development of this PLD is undertaken.

1. Employ the PFD as a phase detector. Its use simplifies the acquisition problem and its large dynamic range is essential to this application.
2. Use the ECL logic family for implementation. The resulting PLD will be quieter. Moreover, such an implementation is consistent with the next point.
3. A higher reference frequency (to that used here) is desirable as better pump pulse attenuation will be obtained with a possible reduction in the PLD noise floor. In addition, the loop frequency can subsequently be increased (depending on the VCO tuning bandwidth) thereby increasing the PLD bandwidth. If the IF frequency division ratio is to be maintained at 1000, an increase in operating (RF) frequency will be necessary. However such an increase is demanded by future systems which shall be using dielectric waveguides as opposed to the free space path (ch. 1).

4. The PLD should be fitted with an automatic frequency control (AFC) which will adjust the reference frequency of the loop as to maintain consistent operation of the VCO over a specified range of its transfer characteristic. That is to say, the defined VCO rest frequency will consistently represent a zero current condition. Such steps are necessary to ensure linearity for revenue metering and that the VCO remains in the center of its tuning range (important for large current conditions).
5. A more frequency agile and linear VCO should be located. Possible suggestions would include some of the recently developed PROM corrected, digital VCO s [24],[25]. These VCOs exhibit excellent linearity and good tuning bandwidth. Commercial availability and selection is limited at present. However, potential for their application in a future PLD design is high.
6. The VCO should contain an RF buffer stage to prevent frequency pulling by the mixer due to temperature variations.
7. The HPU and PLD should be evaluated together as a system before meaningful specifications can be written for the CT The very high performance criteria (accuracy and frequency response) make accurate assessment of the PLD performance (in isolation) difficult with existing laboratory equipment.

8. Revenue metering and GIC monitoring should not be attempted by a single PLD until an extremely linear (over the entire tuning range) VCO can be located.

5.5 EXTENSION OF RESEARCH

Below are listed some areas of further study in the development of the PLD based GPU.

1. A test bed should be developed which is capable of applying rated currents to the HPU and the entire system performance should be experimentally evaluated as suggested in the previous section.
2. An investigation into the mechanisms of noise generation within the PLD should be undertaken. Possible sources of PLD noise are
   a) VCO phase noise,
   b) phase jitter associated with frequency dividers,
   c) pump pulse feed through and
   d) noise associated with the low frequency stages (loop filter etc.).
   e) The noise measurements of Ch. 4 did not include frequencies below 1 Hz. Such data should be obtained before the PLD is developed for use in a GIC monitor.
3. The potential for AM to PM (amplitude to phase modulation) conversion was not investigated for this PLD. The analog to digital interface that occurs before

the first IF frequency divider is felt to be the point in the system most susceptible to these effects. AM to PM conversion should be measured [26] and a suitable interface designed if this effect is significant.

4. The effects of the IF amplifier frequency response should be studied.
5. Loop performance with higher order loop filters should be investigated.
6. Finally, the achievable performance of the HPU should be determined perhaps with the test bed of the first point in order to generate the ultimate performance specifications for a complementary PLD.

5.6 SUMMARY

The following points summarize the conclusions of this thesis.

1. The PFD is an excellent choice as a phase detection device for this application.
2. Computer simulation is a useful analysis tool for a PLD that employs the PFD as a phase detector.
3. The PLD exhibits improved performance over the delay line discriminator with regard to dynamic range and similar performance regarding linearity although it cannot compete with the discriminator in terms of frequency response.

4. The PLD can complement the HPU in a measuring system for revenue metering and GIC monitoring. These two functions cannot be performed together by a single PLD unless a VCO is found that exhibits extremely good linearity over its entire range.

5. The PLD must await the availability of a cost effective, frequency agile, linear (over a wide frequency range) VCO before it can adequately perform the task of protection current measurement. Such a device will ultimately become available due to demand from other applications such as electronic warfare and sophisticated navigation, wideband communication and test equipment. The appearance of a commercially available, high performance VCO will make the PLD an obvious choice (over the discriminator) for a GPU in a high performance, combined revenue metering and protection current measuring system.

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Appendix A

PERFORMANCE CRITERIA FOR CURRENT TRANSDUCERS

TABLE A.1

Proposed Performance Specifications

Item	Protection	Metering
RCF	Not exceeding IEC Class 5p	IEC Class 0.2
60 Hz Phase Error	3 degrees	10 minutes
Suggested S/N at Rated Current	Not Less than 60 dB	50 dB
Dynamic Range	1200:1	24:1 (0.05 to 1.2 pu)
Frequency Range	Not Less than 2 kHz	20 to 100 Hz
Maximum System Delay Time	50 sec.	n/a
System Turn-on Time	2 msec.	Not Longer than 1 sec.

The following definitions are required in the text of this thesis and are extracted from CSA standard C13 [27].

TABLE A.2

IEC Class Specifications

Class	Percentage RCF at percentage of Rated Current			Phase Displacement at Percentage of Rated Current Shown in minutes		
	10 up to 20	20 up to 100	100 up to 120	10 up to 20	20 up to 100	100 u/t 120
0.1	0.25	0.2	0.1	10	8	5
0.2	0.5	0.35	0.2	20	15	10
0.5	1.0	0.75	0.5	60	45	30
5p	---	---	1.0	--	--	60
10p	---	---	3.0	--	--	60

1. Marked Ratio: The expected or ideal Ratio of primary current to secondary current in a conventional CT This will be a constant, valid throughout the range of current over which the transformer is to be employed.
2. True Ratio: The measured (or actual) ratio of primary to secondary current.
3. Ratio Correction Factor (RCF): The ratio of the true ratio to the marked ratio. The primary current is equal to the secondary current multiplied by the marked ratio times the ratio correction factor.

4. Composite Error of a Current Transformer: Composite error shall be expressed as a percentage in accordance with

$$E_c = \frac{100}{I_{s_{rms}}} \sqrt{\frac{1}{T}\int_0^T (i_s - \frac{i_p}{K_n})^2 \, dt} \qquad \ldots(A1)$$

where E_c is the composite error, K_n is the nominal transformation ratio, $I_{s_{rms}}$ is the rms value of the secondary current, i_s is the instantaneous value of the secondary current, i_p is the instantaneous value of the primary current and T is the duration of one cycle.

Proposed performance specifications for unconventional CTs [6] are tabulated in A.1.

A sample of IEC class accuracy specifications were extracted from the GEC 'Protective Relay Application Guide' [A3] and listed in table A.2.

Appendix B

PHASE-LOCKED LOOP TRANSIENT RESPONSE

The second order loop response to three specific test input signals is taken from Gardner [13] and reproduced in this appendix.

The phase error $\theta_e(t)$ in radians resulting from an applied phase step of magnitude $\Delta\theta$ (in radians) is given by

$$\Delta\theta\left(\cos\left(\sqrt{1-\zeta^2}\,\omega_n t\right)-\frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(\text{B1 (a)}),\ \zeta<1$$

$$\Delta\theta(1-\omega_n t)e^{-\omega_n t} \quad \ldots(\text{B1 (b)}),\ \zeta=1$$

$$\Delta\theta\left(\cosh\left(\sqrt{\zeta^2-1}\,\omega_n t\right)-\frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(\text{B1 (c)}),\ \zeta>1$$

The phase error in radians resulting from an applied frequency step $\Delta\omega$ in radian/second is given by

$$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(\text{B2 (a)}),\ \zeta<1$$

$$\frac{\Delta\omega}{\omega_n}(\omega_n t)e^{-\omega_n t} \quad \ldots(\text{B2 (b)}),\ \zeta=1$$

$$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(\text{B2 (c)}),\ \zeta>1$$

The phase error in radians resulting from a frequency ramp $\Delta\dot{\omega}$ in radian/second^2 is given by

$$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}\left(\cos\sqrt{1-\zeta^2}\,\omega_n t + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(B3\ (a)) \qquad \zeta<1$$

$$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}(1+\omega_n t)e^{-\omega_n t} \quad \ldots(B3\ (b)) \qquad \zeta=1$$

$$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t + \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t} \quad \ldots(B3\ (c)) \qquad \zeta>1$$

The parameters ζ and ω_n are the damping factors and natural loop frequency, respectively as defined earlier. It assumed that the loop gain, $K_0 K_d >> \omega_n$. The above equations do not include the steady state phase error which is non-zero in (B2) and (B3).

Appendix C

DATA AND PROGRAM LISTING FOR LOOP SIMULATION

The program listing for the PLD simulator is reproduced in the latter part of this appendix. The input and output segments of the program have been removed for clarity. Input parameter values were passed to the PLD simulator from the the input routine via an array named PARX. The loop output voltage, phase error and time were stored in three separate arrays for output.

TABLE C.1

Flow table for the MC12040

R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0	OUTPUT
1	2	3	4	1
5	2	3	8	1
5	6	7	8	0
9	6	7	12	0
5	2	7	12	0
1	2	7	8	0
9	10	11	12	-1
5	6	11	12	-1

Table C.1 is the flow table for the Motorola MC12040 ECL PFD used in this simulator. This corresponds to the array,

TABLE C.2

Stability table for MC12040

R-V 0-0	R-V 0-1	R-V 1-1	R-V 1-0
1	0	0	1
0	1	1	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	1	0
1	1	0	0
0	0	1	1

IFLOW in the program. Stable states are identified by a '1' in the corresponding stability table, C.2 which is represented in the program by the array ISTABLE. The output column of table C.1 is provided by the array, IOUT in the program. These tables are based on data provided by the manufacturer [19].

This program was written in the BASIC language for the IBM[6] PCjr microcomputer. Two features are identified that may affect the operation of this program if applied to another computer. These are as follows: PCjr BASIC allows multiple statements to be associated with the THEN clause of an IF statement. For example, consider

```
10 IF X=A THEN GOTO 200 : PRINT "NOT EQUAL TO A" : STOP
```

[6] International Buisness Machines Corporation

```
20 REM CONTINUE WITH REMAINING PROGRAM
```

The statements "PRINT "NOT EQUAL TO A" " and "STOP" are considered as part of the THEN clause and in this particular example, can never be executed. If the statement is false, program execution continues with line 20. The second feature is in regard to the FOR-NEXT loop. Upon exiting from a FOR-NEXT loop in PCjr BASIC, the counter is set to the first unused value. For example,

```
10 FOR J=1 TO 10
20 NEXT J
30 PRINT J
```

will result in the value 11 printed for J.

```
10 REM********** PLD SIMULATOR - INTERVAL HALVING ALGORITHIM  (DEC. 14, 1985)
20 REM
30 REM    BY R. SMEGAL, DEPT. OF ELECTRICAL ENGINEERING, UNIVERSITY OF MANITOBA
40 REM
50 REM    INPUT AND OUTPUT PROGRAM SEGMENTS REMOVED, CONSTANT VCO GAIN VERSION
60 REM   PROGRAM IN IBM PCjr BASIC
70 REM
80 REM VARIABLES WITH NAMES BEGINNING WITH H-N ARE INTEGERS
90 CLEAR
100 OPTION BASE 0
110 DEFINT H-N
120 DIM IFLOW(4,8),ISTABLE(4,8),IN(2,2),IOUT(8),VOQ(600),ERROQ(600),QX(600),PARA
$(15),PARX(15),PX$(15),PIX$(15)
130 REM
140 REM    INPUT PARAMETERS IN ARRAY PARX AS FOLLOWS:
150 REM    PARX(0): NATURAL LOOP FREQUENCY IN HZ
160 REM    PARX(1): DAMPING FACTOR
170 REM    PARX(2): SPARE PARAMETER NAME
180 REM    PARX(3): INTEGRATOR CAPACITOR IN FARADS
190 REM    PARX(4): OUTPUT R-C FILTER, R3 IN OHMS
200 REM    PARX(4): OUTPUT R-C FILTER CAPACITANCE IN FARADS
210 REM    PARX(5): OUTPUT R-C FILTER CAPACITANCE IN FARADS
220 REM    PARX(6): VCO GAIN CONSTANT IN HZ/VOLT
230 REM    PARX(7): VCO REST FREQUENCY IN HZ
240 REM    PARX(8): PFD PUMP OUTPUT IN VOLTS
250 REM    PARX(9): APPROX. BASE INTERVAL- DELT  IN SECONDS (INITIAL TIME STEP)
260 REM    PARX(10): TOTAL NUMBER OF ITERATIONS
270 REM    PARX(11): MINIMUM INTERVAL BETWEEN ITERATIONS IN SECONDS
280 REM    PARX(12): TIME OF APPLIED INPUT STEP IN SECONDS
290 REM    PARX(13): PHASE STEP SIZE IN DEGREES  (ZERO FOR NO STEP)
300 REM    PARX(14): FREQ. STEP SIZE IN HZ  (ZERO FOR NO STEP)
310 REM    PARX(15): INITIAL INPUT FREQUENCY IN HZ
320 REM
330 REM    MISC NOTES:
340 REM    *  IS AND JS ARE THE ROW AND COLUMN LABLES FOR THE PFD FLOW TABLE
350 REM    *  TOTAL RUN TIME (APPROX)=BASE INT X TOTAL NO. OF ITERATIONS
360 REM    *  AN INPUT MATRIX , IN IS PROVIDED IN THE PFD EMULATION ROUTINE
370 REM       WHICH ALLOWS THE OPTION TO INVERT INPUT LOGIC LEVELS OF THE
380 REM       FLOW TABLE IN ORDER TO MATCH THE VARIOUS LOGIC FAMILIES
390 REM    *  CHANGES TO THE ORIGINAL PROGRAM THAT ALLOW FOR INTEGRATOR
400 REM       BOUNDING OCCUR IN THE FOLLOWING LINES; 530 540
410 REM       830 1160 1170 2380 2390
420 REM    *  THE OUTPUT TIME IN SECONDS APPEARS IN QX(IO), THE LOOP
430 REM       PHASE ERROR IN DEGREES APPEARS IN ERROQ(IO) AND THE
440 REM       LOOP OUTPUT VOLTAGE IN VOLTS IS STORED IN VOQ(IO).
450 REM    *  # AFTER VARIABLE OR CONSTANT INDICATES DOUBLE PRECISION
460 REM    *  ! AFTER VARIABLE OR CONSTANT INDICATES REAL SINGLE PREC.
470 REM    *  % AFTER VARIABLE OR CONSTANT INDICATES INTEGER
480 REM
490 REM ******* SET INTEGRATOR BOUNDS (IN VOLTS) ********
500 REM
510 REM     BOUNDL: LOWER BOUND    BOUNDU: UPPER BOUND
520 REM
530 BOUNDL=-.333
540 BOUNDU=1.667
550 REM
560 REM ***** LOAD PFD PARAMS. *****
570 REM
580 GOSUB 1520
590 REM
600 REM ***** THIS SEGMENT CALC. VARIOUS CONSTANTS FROM INPUT PARAMETERS *****
```

```
610 REM
620 PI2=6.283185
630 WN=PARX(0)*PI2
640 DAMP=PARX(1)
650 RSPARE=PARX(2)
660 C=PARX(3)
670 R3=PARX(4)
680 CO=PARX(5)
690 VKO=PARX(6)*PI2
700 FV=PARX(7)*PI2
710 VQ=PARX(8)
720 NSTOP=PARX(10)
730 DELTMIN=PARX(11)
740 REM  ADJUST INITIAL DELT TO A MULTIPLE OF TWO TIMES THE MIN. DELT.
750 REM  SET DELTEST SMALLER THAN DELMIN TO ASSURE ACCURATE TEST OF EXIT COND.
760 NINTV%=CINT(LOG(PARX(9)/PARX(11))/LOG(2!))
770 DELTINIT=(2!^NINTV%)*DELTMIN
780 DELTEST=.8*DELTMIN
790 TESTART=PARX(12)
800 PHSTEP=PARX(13)*PI2/360!
810 FRSTEP=PARX(14)*PI2
820 FI=PARX(15)*PI2
830 FO=BOUNDL*VKO+FV
840 TNOP%=NSTOP
850 R3CO=R3*CO
860 R2=2!*DAMP/(WN*C)
870 PDKA=VQ/PI2
880 R1=PDKA*VKO/(WN*WN*C)
890 R1C=R1*C
900 REM
910 REM *** THIS SEGMENT INITIALIZES VARIABLES AND STATE OF LOOP *****
920 REM
930 COLOR 3
940 H=1:HOP=1:IO=-1:JSTATUS=1:AUXFI=0
950 THETAI=0!:THETAO=0!:PHERR=0!
960 REM   SELECT IS,JS TO GIVE STABLE STARTING CONDITION (IE PUMP%=0)
970 IS=2:JS=4:TS=0
980 VXP=(FO-FV)/VKO
990 VO=VXP
1000 DELT=DELTINIT
1010 GOSUB 1950:GOSUB 2190
1020 CLS
1030 REM
1040 REM ***** MAIN LOOP BEGINS HERE *****
1050 REM
1060 ROLD%=R%:VOLD%=V%
1070 GOSUB 2840
1080 LOCATE 1,1
1090 PRINT "WORKING ON ITERATION ",H,"TOWARDS ",NSTOP
1100 TS=TS+DELT
1110 PRINT:PRINT "  IS  JS  PUMP"
1120 PRINT USING "####";IS,JS,PUMP%
1130 VP=PUMP%*VQ
1140 IF PUMP%<>0 THEN GOSUB 2330:GOTO 1180
1150 VO=VXP-(VXP-VO)*EXP(-DELT/R3CO)
1160 IF VO<BOUNDL THEN VO=BOUNDL:GOTO 1180
1170 IF VO>BOUNDU THEN VO=BOUNDU:GOTO 1180
1180 THETAO=THETAO+DELT*FV+VKO*VO*DELT
1190 GOSUB 2770
1200 THETAI=THETAI+DELT*FI+THETA
1210 GOSUB 2450
1220 GOSUB 1950
1230 IF R%<>ROLD% OR V%<>VOLD% GOTO 1340
```

```
1240 GOSUB 2670
1250 IO=IO+1
1260 QX(IO)=TS
1270 VOQ(IO)=VO
1280 ERROQ(IO)=PHERR*360!/6.283185
1290 H=H+1
1300 IF H<=NSTOP THEN 1070
1310 PRINT "DONE"
1320 END
1330 REM *** THIS SEGMENT SUCCESSIVELY HALVES DELT UNTIL EDGE IS LOCATED ***
1340 DELT=DELT/2!
1350 IF DELT<DELTEST THEN DELT=DELTINIT:GOSUB 2190:ROLD%=R%:VOLD%=V%:GOTO 1240
1360 GOSUB 2900
1370 TS=TS+DELT
1380 VP=PUMP%*VQ
1390 IF PUMP%<>0 THEN GOSUB 2330:GOTO 1430
1400 VO=VXP-(VXP-VO)*EXP(-DELT/R3CO)
1410 IF VO<BOUNDL THEN VO=BOUNDL:GOTO 1430
1420 IF VO>BOUNDU THEN VO=BOUNDU:GOTO 1430
1430 THETAO=THETAO+DELT*FV+VKO*VO*DELT
1440 GOSUB 2770
1450 THETAI=THETAI+DELT*FI+THETA
1460 GOSUB 2450
1470 GOSUB 1950
1480 IF R%<>ROLD% OR V%<>VOLD% GOTO 1340
1490 GOSUB 2840
1500 GOTO 1370
1510 REM ------------------------------------------------------------------------
1520 REM  THIS ROUTINE LOADS IN THE DATA          FOR THE PFD ROUTINE
1530 REM
1540 FOR J=0 TO 7
1550 FOR I=0 TO 3
1560 READ IFLOW(I,J)
1570 NEXT I
1580 NEXT J
1590 DATA 1,2,3,4
1600 DATA 5,2,3,8
1610 DATA 5,6,7,8
1620 DATA 9,6,7,12
1630 DATA 5,2,7,12
1640 DATA 1,2,7,8
1650 DATA 9,10,11,12
1660 DATA 5,6,11,12
1670 FOR J=0 TO 7
1680 FOR I=0 TO 3
1690 READ ISTABLE(I,J)
1700 NEXT I
1710 NEXT J
1720 DATA 1,0,0,1
1730 DATA 0,1,1,0
1740 DATA 1,0,0,0
1750 DATA 0,1,0,0
1760 DATA 0,0,1,0
1770 DATA 0,0,0,1
1780 DATA 1,1,0,0
1790 DATA 0,0,1,1
1800 FOR J=0 TO 1
1810 FOR I=0 TO 1
1820 READ IN(I,J)
1830 NEXT I
1840 NEXT J
1850 REM DATA FOLLOWS FOR ECL INPUT LOGIC LEVELS
1860 DATA 3,2
```

```
1870 DATA 4,1
1880 FOR K=0 TO 7
1890 READ IOUT(K)
1900 NEXT K
1910 REM OUTPUT DATA FOLLOWS FOR ECL LOGIC OUTPUT LEVELS
1920 DATA 1,1,0,0,0,0,-1,-1
1930 RETURN
1940 REM ------------------------------------------------------------------
1950 REM SUBROUTINE FOR CONVERSION OF PHASE TO LOGIC VALUES
1960 REM
1970 REM INPUT THETAI AND THETAO IN RAD.
1980 REM  OUTPUT CORR. INTEGERS R% AND       V%
1990 REM  ZERO PHASE YIELDS LOGIC ZERO
2000 REM
2010 TRUNC=FIX(THETAI/3.141593)
2020 RTR=TRUNC/2-FIX(TRUNC/2)
2030 IF RTR>.1 THEN R%=1:GOTO 2050
2040 R%=0
2050 TRUNC=FIX(THETAO/3.141593)
2060 VTR=TRUNC/2-FIX(TRUNC/2)
2070 IF VTR>.1 THEN V%=1:GOTO 2090
2080 V%=0
2090 RETURN
2100 REM
2110 REM ------------------------------------------------------------------
2120 REM PFD EMULATION ROUTINE
2130 REM
2140 REM THIS ROUTINE REQUIRES OPTION BASE OF 0
2150 REM INPUT INTEGER ARRAYS IFLOW,IN,ISTABLE,IOUT
2160 REM INPUT LOGIC STATES R%,V%, AND  PRESENT STATE IS,JS,KS
2170 REM RETURN WITH NEW STATES AND PUMP SIGNAL, PUMP%
2180 REM
2190 ISNEW=IN(R%,V%)-1
2200 IF ISNEW=IS THEN RETURN
2210 IS=ISNEW
2220 IFLOWT=IFLOW(IS,JS)
2230 JS=-1
2240 JS=JS+1
2250 IF ISTABLE(IS,JS)=1 THEN 2270
2260 GOTO 2240
2270 IF IFLOW(IS,JS)=IFLOWT THEN 2290
2280 GOTO 2240
2290 PUMP%=IOUT(JS)
2300 REM PUMP UP OCCURS FOR +1, DOWN FOR-1
2310 RETURN
2320 REM ------------------------------------------------------------------
2330 REM
2340 REM SUBROUTINE FOR THE CALCULATION OF LOOP OUTPUT & INTGR. VOLT.
2350 REM
2360 ZQ1=(R2*VP*C+R1C*(VXP-VO)-R3CO*VP)/R1C
2370 VO=-ZQ1*EXP(-DELT/R3CO)+VP*DELT/R1C+ZQ1+VO
2380 IF VO<BOUNDL THEN VO=BOUNDL:GOTO 2400
2390 IF VO>BOUNDU THEN VO=BOUNDU:GOTO 2400
2400 VXP=VXP+DELT*VP/R1C
2410 IF VXP<BOUNDL THEN VXP=BOUNDL:GOTO 2430
2420 IF VXP>BOUNDU THEN VXP=BOUNDU:GOTO 2430
2430 RETURN
2440 REM ------------------------------------------------------------------
2450 REM  SUBROUTINE FOR THE RENORMALIZATION OF THETAI AND THETAO
2460 REM
2470 REM ADJUST ANGLE WHEN 360.00084 DEG IS EXCEEDED
2480 REM THRESHOLD MUST BE GREATER THAN 360 DEG. TO ASSURE POSITIVE ANGLES
2490 REM
```

```
2500 PI2#=6.283185308#
2510 IF THETAO>6.2832 THEN 2540
2520 IF THETAI>6.2832 THEN 2600
2530 RETURN
2540 THETAON#=THETAO/PI2#
2550 THETAO=(THETAON#-FIX(THETAON#))*PI2#
2560 REM
2570 REM ADDITION ANGLE ADJUSTMENTS NOW.
2580 REM
2590 GOTO 2520
2600 THETAIN#=THETAI/PI2#
2610 THETAI=(THETAIN#-FIX(THETAIN#))*PI2#
2620 REM
2630 REM ADDITIONAL ADJUSTMENTS NOW.
2640 REM
2650 RETURN
2660 REM ------------------------------------------------------------
2670 REM SUBROUTINE FOR THE CALCULATION OF PHASE ERROR
2680 REM
2690 ERRORN=THETAI-THETAO
2700 COMPERR=ERRORN-SGN(ERRORN)*6.283185
2710 DELTERR=ABS(ERRORN-PHERR)
2720 DELTCOMP=ABS(COMPERR-PHERR)
2730 IF DELTCOMP<DELTERR THEN PHERR=COMPERR:RETURN
2740 PHERR=ERRORN
2750 RETURN
2760 REM ------------------------------------------------------------
2770 REM THIS SUBROUTINE GENERATES A TEST INPUT WITH INPUT PHASE
2780 IF TS<TESTART THEN THETA=0:RETURN
2790 THETA=PHSTEP*JSTATUS+FRSTEP*DELT
2800 JSTATUS=0
2810 RETURN
2820 REM
2830 REM ***** SUBROUTINE FOR SAVING STATE OF LOOP *****
2840 TSOLD=TS
2850 THETAOOLD=THETAO
2860 THETAIOLD=THETAI
2870 VOOLD=VO
2880 VXPOLD=VXP
2890 RETURN
2900 REM **** SUBROUTINE FOR RECALLING PAST STATE OF LOOP ****
2910 TS=TSOLD
2920 THETAO=THETAOOLD
2930 THETAI=THETAIOLD
2940 VO=VOOLD
2950 VXP=VXPOLD
2960 RETURN
```

Appendix D

GLOSSARY OF NOTATION

symbol	description	main page ref.
CT	current transducer	1
HPU	high potential unit	2
GPU	ground potential unit	2
RF	radio frequency	
IF	intermediate frequency	
FM	frequency modulation	
AM	amplitude modulation	
TTL	transistor-transistor logic	
ECL	emitter coupled logic	
YIG	Yttrium Iron Garnet	3
GIC	geomagnetically induced currents	4
PLD	phase locked demodulator	9
VCO	voltage controlled oscillator	10
PFD	phase frequency detector	21
PU	pump-up	23
PD	pump-down	23
VCE	V channel enable	72
RFS	reference frequency select	72
ω_i	instantaneous input frequency to the demodulator	10
ω_c	center frequency of the demodulator	10

ω_0	instantaneous VCO frequency	10
ω_n	natural loop frequency	15
ω_{ref}	loop reference frequency	51
ω_V	instantaneous frequency of the signal applied to the V input of the PFD	52
ω_R	instantaneous frequency of the signal applied to the R input of the PFD	52
ω_{if}	instantaneous IF frequency	52
ω_a	instantaneous offset from the PLD center frequency	76
θ_i	instantaneous input phase to the PLD	10
θ_0	instantaneous VCO phase	11
θ_e	instantaneous loop phase error	11
θ_V	phase of the signal applied to the V input of the PFD	26
θ_R	phase of the signal applied to the R input of the PFD	26
ϕ_i	phase of the monitored line current	16
ϕ_0	phase of the demodulated signal	18
$\Delta\phi_m$	maximum phase error limit of the loop phase detector	19
$\Delta\omega_i$	peak input frequency deviation	16
$\Delta\omega_0$	peak VCO frequency deviation	18
v_0	instantaneous PLD output voltage and VCO control voltage	12
v_d	phase detector output voltage;	11
	PFD output in the locked mode;	26
	PFD output in the unlocked mode	30

V_p	magnitude of the PFD pump voltage	26
V_{xp}	voltage across the integrator capacitor	35
T_i	input signal period	39
T_a	estimated acquisition time	32
t_p	pump time	25
N	IF frequency division ratio	52
ζ	loop damping factor	15
Ω	line current frequency	16
G_D	demodulator gain	17
$H(j\omega)$	closed loop transfer function	13
$F(j\omega)$	loop filter function	12
K_0	VCO gain constant	12
K_0	phase detector gain	11

Note: Frequencies designated by ω will have units of radian/second unless stated otherwise.