APPLICATION OF STATIC COMPENSATORS AT HVDC-TERMINALS

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David T. Flueckiger

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APPLICATION OF STATIC COMPENSATORS AT HVDC-TERMINALS

BY

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ABSTRACT

HVDC-Terminals need reactive power supply during normal operation. This has been achieved until now with fixed capacitors and synchronous compensators.

Large faults in the DC system which are followed by sudden load rejections cause a surplus in reactive power generation at the terminals. This can give rise to overvoltages at the converter bus until the Var generation can be adapted to the new demand.

In order to minimize those dynamic overvoltages a fast control of the reactive power sources is desirable.

In this study various types of modern static Var compensators are compared with the traditionally used synchronous compensators. The Nelson River HVDC-scheme has been simulated using a digital stability program and the response of static and synchronous compensators to dynamic overvoltages under the above mentioned fault conditions has been investigated.

The tests demonstrated that static compensators, like saturated reactors or thyristor controlled devices, can handle those overvoltages much better than synchronous compensators or fixed capacitor banks. Also the combination of static and synchronous compensation can result in a noticeable improvement.

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LIST OF SYMBOLS AND ABREVIATIONS

AC	Alternating Current
B	Susceptance
BP	Bipole
C	Capacitance, Capacitor
DC	Direct Current
DOV	Dynamic Overvoltage
f	Frequency
FC	Fixed Capacitor
G	Conductivity
HSVS	Regulator Output of SVS
HVDC	High Voltage Direct Current
Hz	Hertz
I	Current
K	Gain, Constant
L	Inductance
LF	Load-Flow
M	Mega (prefix)
ms	Milliseconds
P	Active Power
PI	Proportional-Integral (- Regulator)
pu	Per Unit
Q	Reactive Power
R	Resistance, Resistor
S	Apparent Power

SC	Synchronous Compensator
SCP	Short Circuit Power
SCR	Short Circuit Ratio
SR	Saturated Reactor
SVS	Static Compensator (here with thyristor controlled devices)
T	Time Constant
t	Time
TCR	Thyristor Controlled Reactor
TCSR	Thyristor Controlled Saturated Reactor
TSC	Thyristor Switched Capacitor
V	Voltage, Volts
V_S, V_K	Knee Voltage
VA	Volt-Ampere
Var	Var (reactive power unit)
W	Watt
X	Reactance
X(s)	Input Variable (Laplace transform)
x(t)	Input Variable (time domain)
Y	Admittance
Y(s)	Output Variable (Laplace transform)
y(t)	Output Variable (time domain)
Z	Impedance
α	Firing Angle
γ	Extinction Angle
ξ	Damping Coefficient

1. INTRODUCTION

1.1 Motivation and Background

Reactive power compensation is generally required in AC power transmission systems in order to improve the static and dynamic stability.

With the control of the reactive power flow the voltage at an AC-bus can be stabilized effectively since a change in the reactive power balance affects directly the bus voltages (Fig. 1.1).

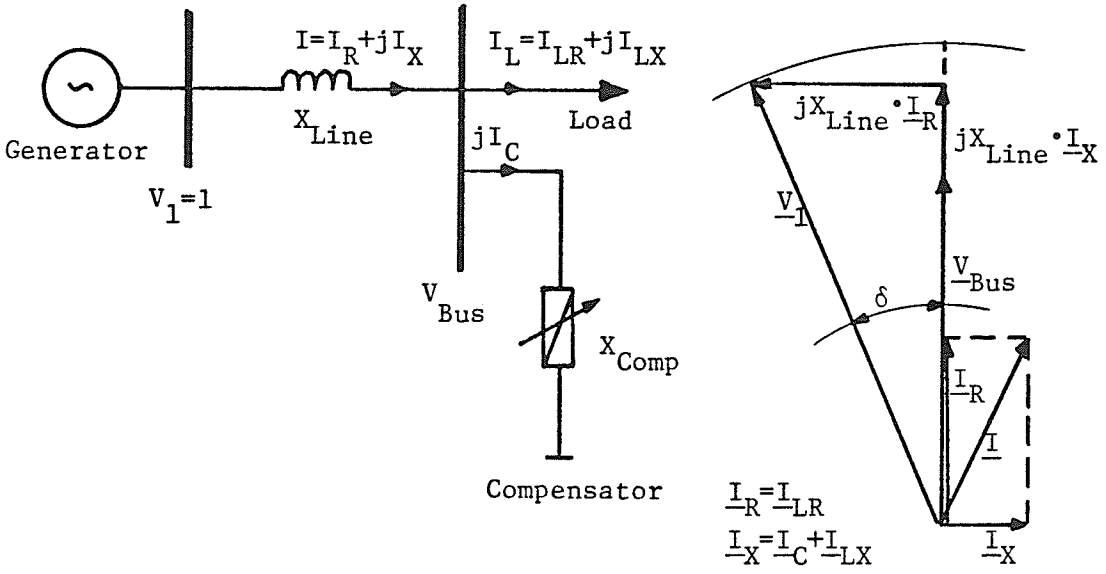


Fig. 1.1: Voltage Control with a Reactive Power Compensator:
A change in X_{Comp} or I_{LX} causes a change in I_X which results in a voltage change. A change in I_{LR} causes only a change in δ, the magnitude of the voltage is practically not affected. Changes in V_{Bus} can be compensated by controlling X_{Comp}.

In combined AC/DC system the additional problem of supplying reactive power to the HVDC converters has to be handled.

The amount of reactive power required by a converter station depends on the active power flow in the terminals. Hence it is not possible to meet these Var requirements by fixed sources only; the installation of controllable Var compensators is necessary. Until now the problem has been approached by combining fixed reactive power sources, such as filters or capacitor banks, with synchronous compensators.

The filters, which are usually permanently connected, supply a constant amount of reactive power at fundamental frequency while the synchronous compensators can fill the gap between this fixed amount of Vars and the changing requirements of the converter.

Synchronous compensators can meet very well the variable demand of reactive power at a converter-terminal and they also help improving the strength of the connected AC-system by increasing the total short circuit ratio (SCR) of the system. But some significant disadvantages are associated with the operation of synchronous compensators (SC). SC's call for high costs of operation and maintenance. For example, there are six SC installed at the Dorsey inverter terminal of the Nelson River system of which only four are usually in operation.

In addition the response time of the exciter system of a SC is very slow (in the range of several hundreds of milliseconds), a fact which makes them unable to react to fast changes in reactive power demand as for example in case of a sudden load rejection.

Therefore it appears very desirable to search for a better alternative to synchronous compensation.

Static Var compensators (or static Var systems, SVS) have been used successfully in the last few years instead of synchronous compen-

sators. Their high reliability and their fast regulating system with response times of only a few cycles have made them highly competitive to synchronous compensators. But until now SVS have not been used in connection with an HVDC Station, the first HVDC system with only SVS is now under construction near Montreal (Chateauguay back to back system, Hydro Quebec).

In a few years, when both bipoles of the Nelson River HVDC system of Manitoba Hydro are complete and additional generating capacity will be installed at the north end of the system, additional reactive power of 300 to 400 MVar will be required at the Dorsey inverter station. This means that more synchronous compensators will be installed or static Var compensators will be added in place.

The aim of this study was to examine some of the aspects of integrating SVS with synchronous compensators with emphasis on the handling of dynamic overvoltages due to load rejections. This is a characteristic situation where a fast change in the reactive power supply at the converter is required.

If an HVDC converter is blocked suddenly, a surplus of capacitive power is fed from the Var compensators. This causes overvoltages in the system if the reactive power generation cannot be reduced immediately. These overvoltages are dependent on the short circuit ratio of the system and are especially high with low SCR and with the converters operating at full power.

1.2 Previous Work, Literature Search

During the preliminary investigation for this study, namely literature search and classification of the already available material it

appeared that not much work has yet been done on the subject of this study - integration of static Var sources in HVDC-systems.

The following sources were used to collect, classify and study the published information on reactive power compensation and overvoltage problems at HVDC converter terminals:

1. General books on power systems and HVDC
2. Results from computer aided literature search
3. Papers from conferences on HVDC as:
   - Manitoba Conference EHV-DC, Winnipeg, 1971
   - D.O.E. sponsored Symposium, Phoenix, Arizona, 1980
   - IREQ/EPRI Symposium on Controlled Reactive Compensation, Montreal, 1979
   - Conference on Overvoltages and Compensation on Integrated AC-DC Systems, Winnipeg, 1980
   - IEE-Conference on Thyristor and Variable Static Equipment for AC and DC Transmission, London, 1981.
4. Reference lists in the above papers
5. Bibliography of Cigre Study Committee 14, working group 03, Filters and Reactive Compensation, 1981.

A collection of the most relevant papers from the above mentioned sources is given in the reference list in Appendix A. Examination of the literature reveals that very few papers are dealing directly with the question of static or synchronous compensation in HVDC-systems. The only relevant paper found which compares the behaviour of different types of compensators in an AC-DC-scheme is [3.2]. It shows the results of a study carried out by Furnas for the Itaipu HVDC project. The advantages of both static and synchronous compensation as well as mixed compensation

are shown. The preference was finally given to the all synchronous compensator alternative for the Itaipu application mainly because of stability problems with static compensators, although the mixed mode was shown to be a suitable solution too. Some of the other papers contain interesting information about possible disturbances in AC-DC systems and their impact on the systems behaviour.

1.3 Methodology

The study was carried out as a digital simulation on computer. A load-flow and stability program was used for the tests after some modification had been implemented. A description of the program as well as of the changes made follows in Chapter 2, and in Chapter 3 a new model for static Var compensators is illustrated.

In order to obtain a representative palette of various types of compensators an evaluation of the available schemes had to be done. Basically three types of static Var sources had to be considered:

- Saturated reactors
- Thyristor controlled saturated reactors
- Thyristor controlled linear reactors with thyristor switched capacitors.

A more detailed description of these will follow in Chapter 3.

Since the study was of interest for Manitoba Hydro the Nelson River HVDC scheme with two parallel DC links was modelled for the study. All the system data were obtained from Manitoba Hydro or found in [2.1].

As already mentioned, the investigation of dynamic overvoltages following a converter blocking was the main purpose of the tests.

In order to compare the performance of the various combinations of compensators, all tests have been done with the same system configuration and with the same sequence of faults. With those tests it could be shown that static compensators show advantages in their performance over synchronous compensators. Also the combination of existing synchronous compensators with static compensators can bring substantial improvement of the system behaviour, it even seems that such a combination is optimal from the point of view dynamic overvoltages, as illustrated in Chapter 6.

2. DESCRIPTION OF THE STABILITY PROGRAM, CHANGES AND DEBUGGING

2.1 General

A load-flow and transient stability program has been used to carry out the study. The program was written by A.E. Hammad and is now in use at Manitoba Hydro, in Brown Boveri Baden, Switzerland and at the University of Manitoba. The program enables the simulation of power systems with multiterminal HVDC schemes and is very useful for studies of slower transient phenomena like dynamic overvoltages which are the subject of these tests. The program is written in Fortran IV. The program consists of two sections: a load-flow part and a stability part. The data from a load-flow study can be used to initialize the stability run. The electrical quantities are represented as phasors and not with their actual waveform. Therefore fast transients can not be analyzed and some of the results presented in this report have to be used with discretion. It is not the purpose of this paragraph to provide a complete description of the program, for more details see [6.6], [6.7], [6.8].

A brief description of the changes made in the program is given below. Some additional explanations will follow in Appendix C.

2.2 Debugging of the Program

Since the use of the Nelson River system as base for the modelling gave rise to several problems in connection with the program, a fair amount of time had to be invested in debugging the stability program. Fortunately we obtained considerable help from Manitoba Hydro.

A list of the major corrections is given below:

- Some errors in the load flow data input have been corrected.
- A problem with the data initialization for the stability run could only be settled after switching to a new version of the program.
- A few wrong statements in the subroutine for the initialization of the saturated reactor had to be corrected.
- The control loops of the saturated reactor tended to be unstable for small droops. This was a software and not a system problem. It could be resolved by adding a lag function into the loop whose time constant was short enough not to affect the overall response of the saturated reactor (for more details see Chapter 3) and by changing the iteration step for the stability run to a faster value.

2.3 Other Changes

Besides the above mentioned corrections some other modifications had to be made for this study:

- A new compensator model has been written which can be used to simulate any type of thyristor controlled shunt compensator. This new subroutine replaces the former two models for thyristor controlled reactors and thyristor switched capacitors. The two major improvements to the old version are the redesigned control loop for the compensator and the rearrangement of the input data. The input parameters are now closely related to the data usually available from a real system and the whole model gains much in its versatility. This new subroutine was implemented in a way which required changes in a minimum number of subroutines only. A description of a general compensator representation upon which the model is based follows in Chapter 3.

- In order to model the static compensator a new subroutine for simulating a PI-regulator had to be written. It is based on the same algorithm as all the other analogue function blocks which are written by A. Hammad and are described in [6.8].

The simulation of the PI - transfer function was done in the following way:

Analogue transfer function: $G(s) = \frac{Y(s)}{X(s)} = \frac{1 + sT}{sT} = 1 + \frac{1}{sT}$ (2.1)

or in time domain: $y(t) = x(t) + \frac{1}{T} \int x(t)\, dt$ (2.2)

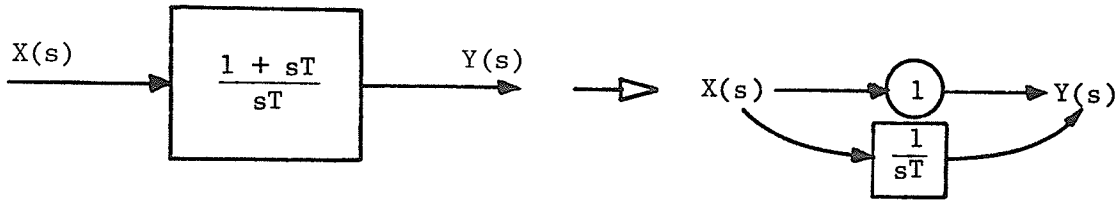


Fig. 2.1: Representation of PI - Regulator function

Equation (2.2) for discrete time steps Δt:

Increment $y(t) - y(t-1) = x(t) - x(t-1) + x(t) \cdot \frac{\Delta t}{T}$

or $$y = y_o - x_o + x \cdot \frac{\Delta t}{T} + x \qquad (2.3)$$

with $y(t) = y \quad y(t-1) = y_o$

$x(t) = x \quad x(t-1) = x_o$

and with $$c = y_o - x_o + x \cdot \frac{\Delta t}{T} \qquad (2.4)$$

we obtain

$$\boxed{\begin{aligned} c &= c_o + x \cdot \frac{\Delta t}{T} \\ y &= c + x \end{aligned}} \qquad (2.5)$$

with the initial condition $c_o = y_o - x_o$

- A new feature has been added to print the integral over the square of one bus voltage to be able to estimate the thermal stresses of a device like for example a surge arrester.

  The function is

$$\int_{t_F}^{t} V_B^2 \, dt \qquad (2.6)$$

  and is printed at each time step the system is monitored.

  The starting point of the integration can be chosen (usually identical with a fault time) and after a specified interval the value can either be kept or set back to zero. This feature can only be used for one bus at a time but it should be no problem to expand its use over all busses if necessary.

- All the stability data used for plotting can now be saved on tape or disk for further processing.

3. EVALUATION OF REACTIVE POWER COMPENSATORS

3.1 Requirements from Var Compensators in an AC-DC-System

For the application of reactive power compensators there is a basic difference in the requirements for a system with HVDC transmission to a system with AC transmission only.

Reactive power compensators in AC transmission systems are generally used to improve the transient and dynamic stability of the system.

In addition to this, reactive power has to be supplied to the converter station in a system with HVDC schemes.

A summary of duties for a Var compensator is given in Table 3.1.

System \ Main Tasks	Static	Dynamic
System with AC Transmission only	- Stabilization of System Voltage in steady state - Control of Reactive Power Flow - Improving Power Transmission Capability - Improving Voltage Profile	- Reduction of Overvoltages - Stabilizing System after Faults
System with AC and HVDC Transmission	- Reactive Power Supply to HVDC Terminal - Increasing Short Circuit Ratio at HVDC-Terminal - Stabilization of System Voltage in Steady State	- Reduction of Overvoltages - Stabilizing Systems after a Fault

TABLE 3.1: System Requirements from a Var Compensator

As it can be seen from Table 3.1, the main difference in the requirements from a reactive power compensator are found for steady state operation. All those tasks can be met by relatively slow compen-

sators like synchronous compensators (SC) or fixed capacitor banks (FC) as it was done until now. But if dynamic problems are taken into consideration, especially for weaker AC systems, fast compensation is essential and the problems become similar to those in a purely AC system. In the following chapters a more detailed comparison of various types of compensators is carried out. In this study only shunt compensation is considered.

3.2 Comparison of Various Types of Var Compensators

In order to compare the dynamic behavior of static compensators with synchronous compensators (SC), a number of characteristic types of SVS had to be evaluated for the study. Besides the SC there are basically three types of SVS currently in operation or under development by manufacturers:

- Saturated reactors (SR)
- Thyristor controlled reactors (TCR) combined with thyristor switched capacitors (TSC) or fixed capacitors (FC)
- Thyristor controlled saturated reactors (TCSR)

In the following comparison all numerical values have been taken from literature and do not necessarily correspond with the results we actually obtained in the study. They are dependent on the system and on the compensator design.

3.2.1 Synchronous Compensators (SC)

The synchronous compensator is basically an idling synchronous machine connected to a bus such that the active power output is zero (i.e. no prime mover). With the excitation the amount of absorbed

(inductive) or generated (capacitive) reactive power can be controlled. The dynamic response of the exciter is quite slow (several hundred milliseconds) and the machine shows the same dynamic behaviour as a synchronous generator.

Until now the SC was the only type of compensator used at HVDC terminals besides fixed capacitor banks because it has some important advantages for this application. The SC is able to improve the short circuit ratio at an HVDC terminal since it acts dynamically as a reactance in parallel to the AC-system even when supplying capacitive power. This is also of special importance during overvoltages when the SC can respond immediately to a large demand of reactive power without waiting for the exciter action. But because of its slow exciter response the SC is not able to add much to the dynamic stability of the system besides the subtransient effect in the first moment after fault. In addition SC are very costly in operation and maintenance.

3.2.2 Saturated Reactors (SR)

The SR is basically a shunt reactor which operates in saturation. This type of compensator needs no thyristors or electronic regulators. The control characteristic is achieved by adjusting the slope of the saturation part with series capacitors which is shown in Fig. 3.1.

A typical value for the intrinsic slope of the saturated reactor is about 15%. With the series capacitor the slope of the compensator is usually adjusted to a value between 3 and 10%. The lack of any thyristors or other electronic circuits results in a very fast response time of the SR (about 15 ms at 60 Hz) to a voltage change. Furthermore the SR will reduce large overvoltages immediately due to its direct

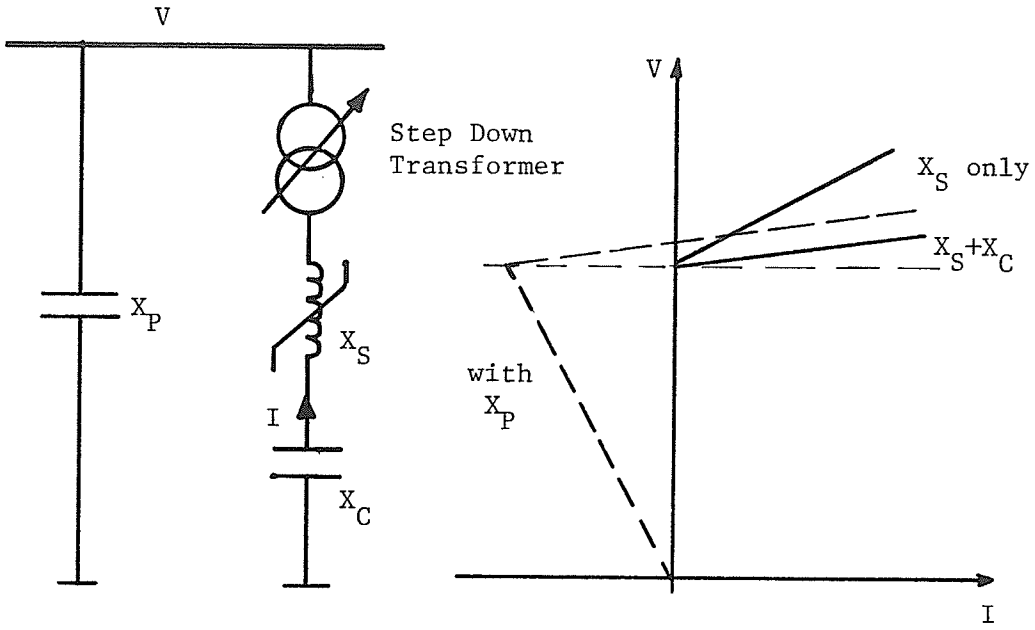
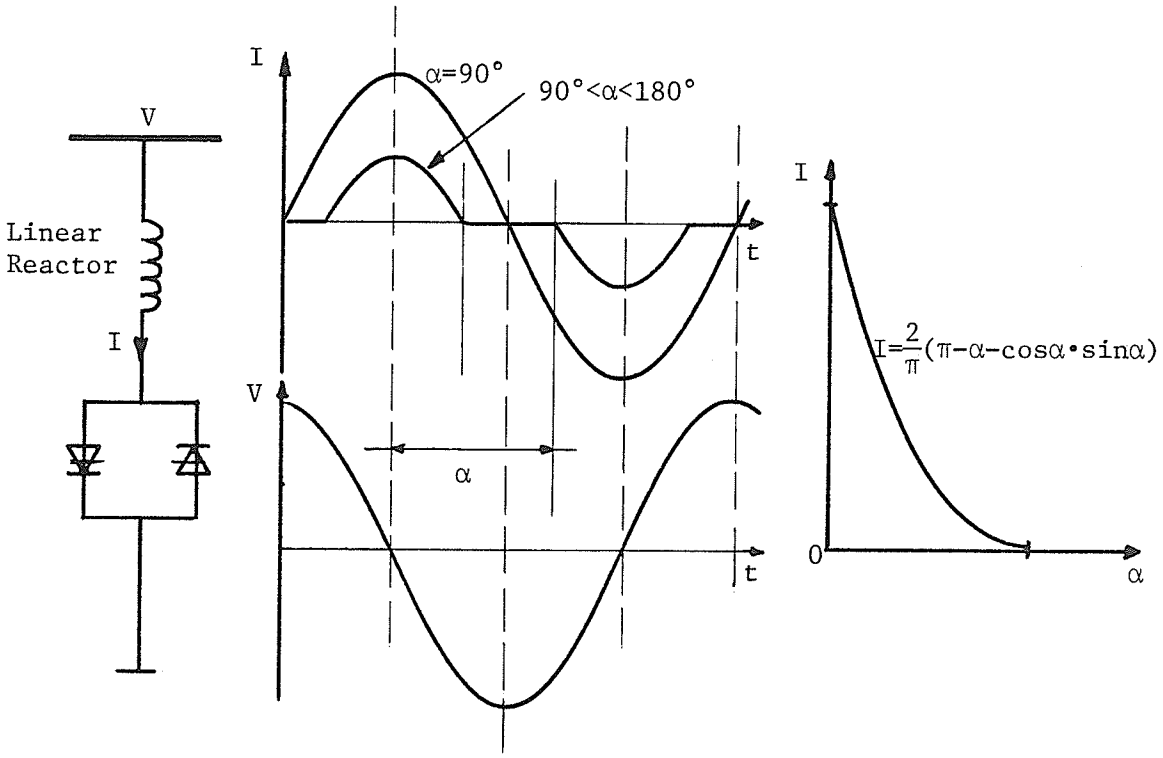


Fig. 3.1: Saturated Reactor, Single Line Diagram and V-I-Characteristic



Single Line Diagram | Current and Voltage Waveforms | α-I-Characteristic

Fig. 3.2a: Thyristor Controlled Reactor

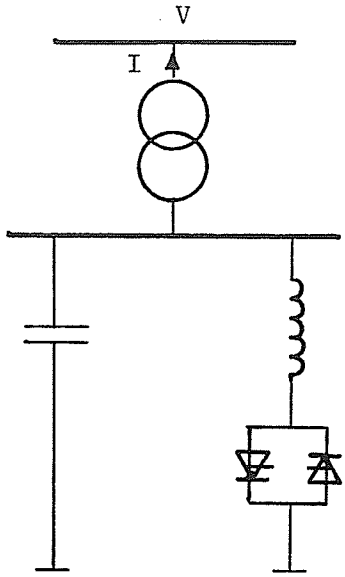


Fig. 3.2b: Compensator with TCR + FC

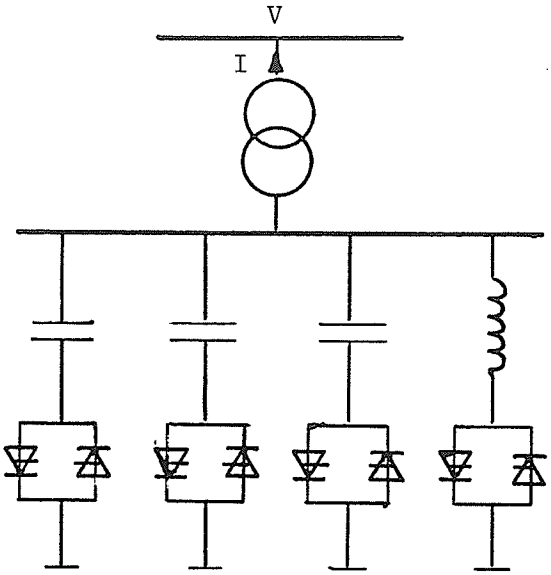


Fig. 3.2c: Compensator with TCR + 3 TSC

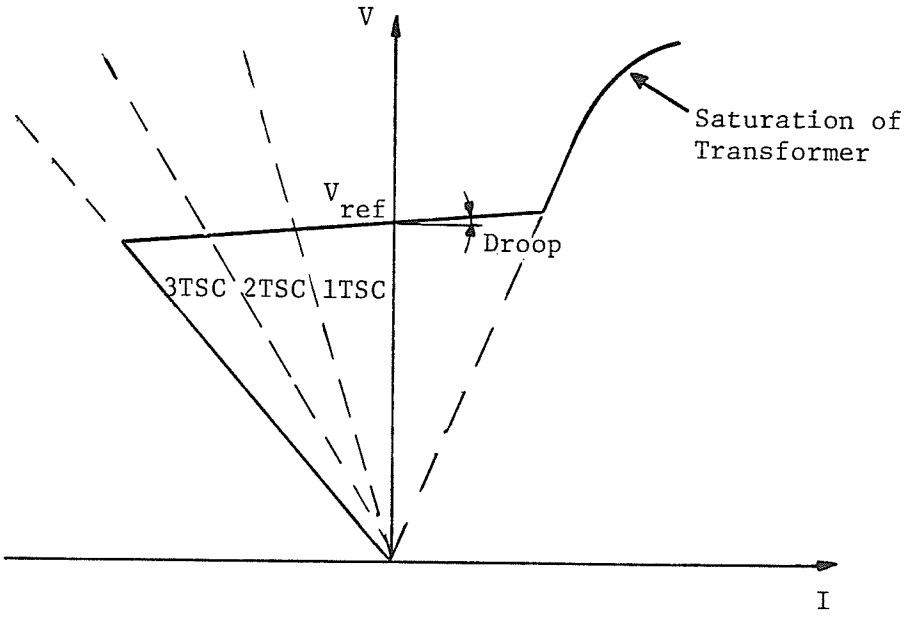


Fig. 3.3: Typical V-I-Characteristic of SVS with TCR and 3 TSC as Shown in Fig. 3.2 c

reaction. The second big advantage of the SR is its large overload capability of 3 to 4 pu.

On the other hand, a SR can create a large amount of harmonics in the current which results in complicated designs in order to reduce them. Besides that an SR can only be connected to the system over a step down transformer with on-load tapchangers to allow adjustment of its operating range according to the system conditions.

3.2.3 Thyristor Controlled Reactors (TCR) with Thyristor Switched Capacitors (TSC) or Fixed Capacitors (FC)

Modern static compensators (SVS) operate with linear, thyristor controlled reactors and capacitors. The TCR is a device which allows a continuous control of reactive power from 0 MVar to a maximum value according to its impedance (Fig. 3.2a). Together with a parallel capacitor the characteristic can be extended into the capacitive range. This capacitor can either be permanently connected to the bus (FC) as in Fig. 3.2b or it can be switched by thyristor valves (TSC, Fig. 3.2c). The advantage of TSC over FC is the fast switching on and off (average delay < 1/6 cycle) of the capacitors without large transients in the current which results in smaller TCR units and therefore smaller losses and harmonic currents in steady state. They allow also better transient response since the large capacitors which sustain overvoltage can be switched off immediately by blocking the thyristors in case of a fault.

Combined TCR-TSC compensators are very flexible in operation since both operating point and slope can be controlled electronically. A typical V-I-characteristic of such a SVS is shown in Fig. 3.3. Typical response time of a thyristor controlled SVS is around 25...30 ms (1.5...2

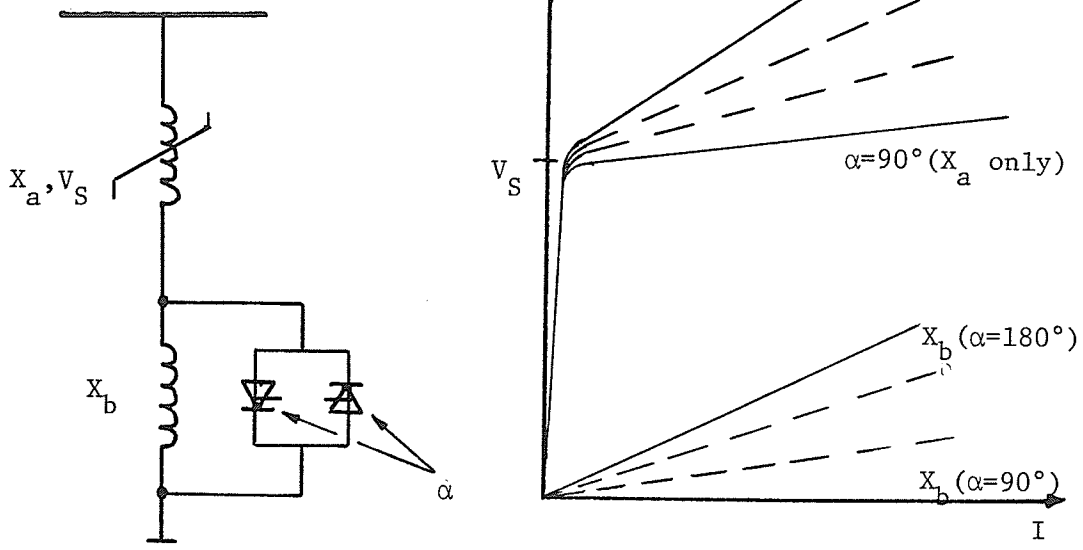
cycles), somewhat slower than that of the SR. The reason for this is the response of the electronic regulator which has to be added to the delay of the TCR/TSC. But the response can be improved very easily for large disturbances by instantaneous switching of the thyristor valves. More details about the regulator are given in Chapter 3.3. Due to the electronic regulator the SVS can be very easily optimised to specific system conditions, especially to improve the steady-state stability. One example will be shown in a following chapter (see also References [6.1], [6.2].

One disadvantage of the SVS to the SR is its smaller overload capability since the thyristor valves have to be dimensioned for the large overcurrents. The reliability of the SVS is comparable to the SR and naturally much higher than with synchronous compensators.

3.2.4 Thyristor Controlled Saturated Reactors (TCSR)

The TCSR is a relatively new device and has not yet been tested in practical operation. The principle is similar to that of an SR. But with the TCSR the knee-voltage level and saturation slope can be controlled electronically by means of thyristor circuits.

Until now two manufacturers have presented papers on this subject. AEG [6.4] proposes a linear thyristor controlled reactor in series with the saturable reactor (Fig. 3.4a) in order to control the saturation level of the compensator. But there seems to be an error in their conclusions: With the proposed scheme it is not possible to vary the knee level of the SR without changing the saturation slope (Fig. 3.4b). To obtain a considerable shift of the knee point one has to choose the impedance of the linear reactor X_b in the range of the



a) Single Line Diagram

b) V-I-Characteristic

Fig. 3.4: AEG Proposal for a TCSR

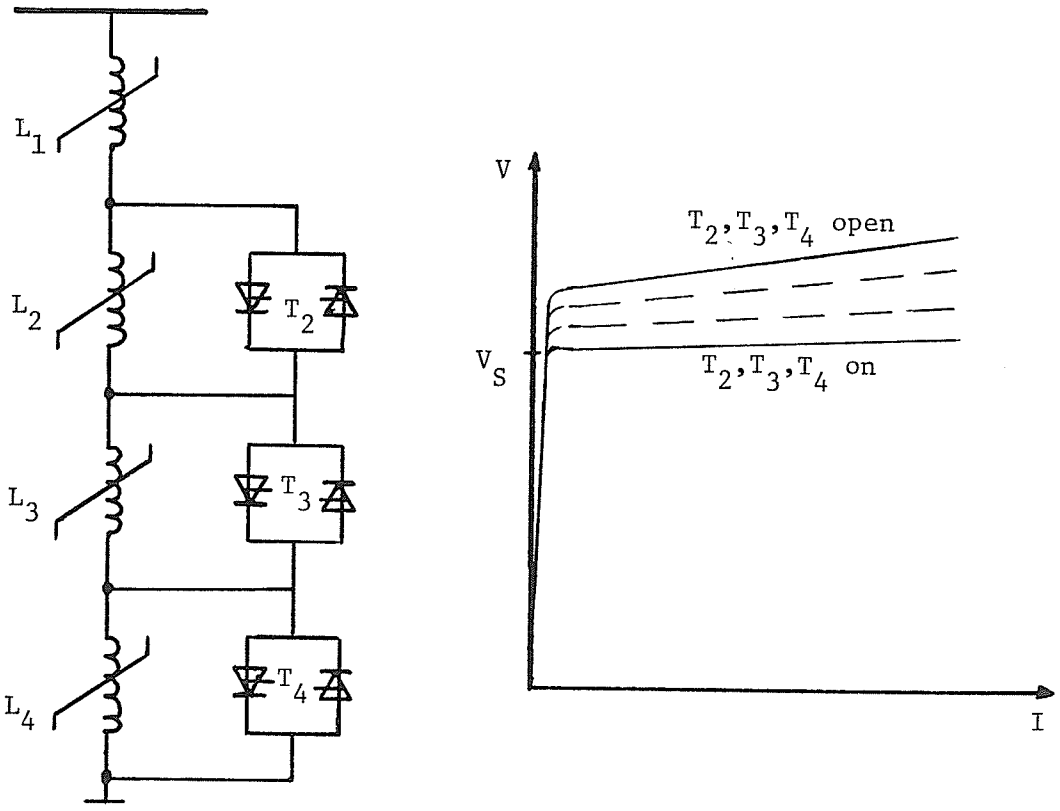


Fig. 3.5: GEC Proposal for a TCSR

impedance of the unsaturated SR, which is very high. This results in rather high droops in the operating (saturated) area of the device and therefore it is not very interesting.

On the other hand, if the impedance of X_b is chosen to be of a value which results in reasonable droops (maybe 5 to 15%), the impact on the knee voltage is negligibly small. This makes the system, as described, not very advantageous over the existing ones.

A second proposal by GEC [6.3] with several saturated reactors with graded knee levels in series is more interesting (Fig. 3.5). To give an example, the reactor L_1 can be chosen with a saturation level of 95%, while L_2 to L_4 can range between 1 and 10%. In this case both knee level and saturation slope can be controlled by thyristor valves if one reactor is chosen to be linear.

The TCSR has the same overload capability as the simple SR although the thyristors have to be dimensioned for the large over-currents (but not for the full voltage stresses).

Theoretically the TCSR could be an interesting alternative to the compensator with linear TCR, in practice its good performance has not been proven yet.

3.2.5 Comparison of Previously Described Compensators

In the following table a preliminary overview is given how the various types of compensators can meet the problem in application at an HVDC terminal connected to an AC-system.

Compensator Type / System requirements	Synchronous Compensator SC	Saturated Reactor SR	TCR/ TSC	Thyristor Controlled Saturated Reactor TCSR
Supply of cap. MVars to HVDC-converter	yes	no (only together with capacitors)	yes	no (only together with capacitors)
Improving short circuit ratio in steady state	yes	no	no	no
Fast action in case of DOV	yes (only in first moment)	yes	yes	yes
Large overload capability	yes	yes	no	limited
Improvement of dynamic and transient stability	limited	yes	yes	yes
Supply of cap. and react. power	yes	no	yes	no
Flexibility in choosing operating point	yes	limited	yes	yes
Maintenance cost	high	low	low	low

Table 3.2: Comparative Overview of Previously Discussed Compensators

3.3 Modelling Techniques for Compensators

3.3.1 Synchronous Compensators

For the synchronous compensators the same model as for the generators could be used in the tests. This model, a subtransient representation of the synchronous machine together with exciter and turbine model was already available in the stability program. To use it for SC's, simply the turbine data had to be omitted. The representation is not treated in detail here. For more information see reference [4.3].

3.3.2 Static Compensators

In the stability program all types of static compensators can be modelled with a voltage source behind a reactance as shown in Fig. 3.6. The angle of the voltage source is always kept the same as the one of the connected bus. The magnitude is modulated according to the Var-requirements at the bus. This model was originally described in [4.1] and [4.2]

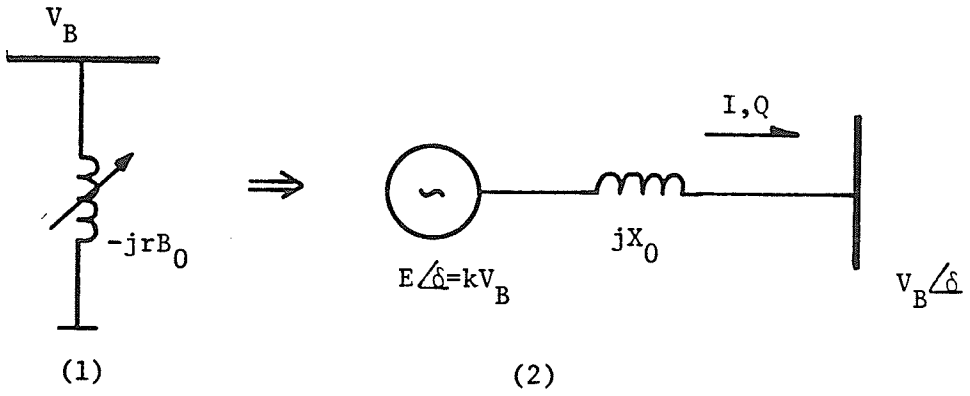


Fig. 3.6: Static Compensator Representation in the Stability Program

Reactive power in circuit (1): $S = -jB_o V_B^2 r$ (3.1)

Reactive power in circuit (2): $S = -jB \cdot V^2 \cdot (1 - k)$

$$\text{with } \underline{E} = k \cdot \underline{V}_B \tag{3.2}$$

In order to represent (1) by (2) k must be chosen as

$$k = 1 - r \tag{3.3}$$

Thus

to obtain 0 MVar: $r = o,\ k = 1$ and $\underline{E} = \underline{V}_b$

to supply MVar: $r < o,\ k > 1$ and $|\underline{E}| > |\underline{V}_B|$

to absorb MVar: $r > o,\ k < 1$ and $|\underline{E}| < |\underline{V}_B|$

Special cases:

r	E	S
-1	$2\underline{V}_B$	$j\ B_o V_B^2$
1	0	$-j\ B_o V_B^2$

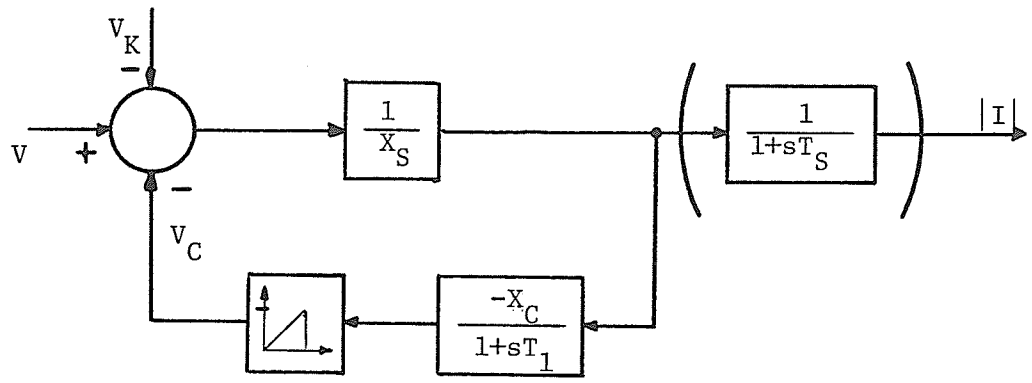
3.3.2.1 Saturated Reactor

The model of the simple saturated reactor was already existing in Hammad's program and could be used as it was after some debugging. Since the representation of a SR might not be commonly known, a short description of the modelling technique is given here: The basic representation was taken from a CIGRE Report on modelling of static Var systems [6.5] and is shown in Fig. 3.7a with the corresponding V-I-characteristic in Fig. 3.7b.

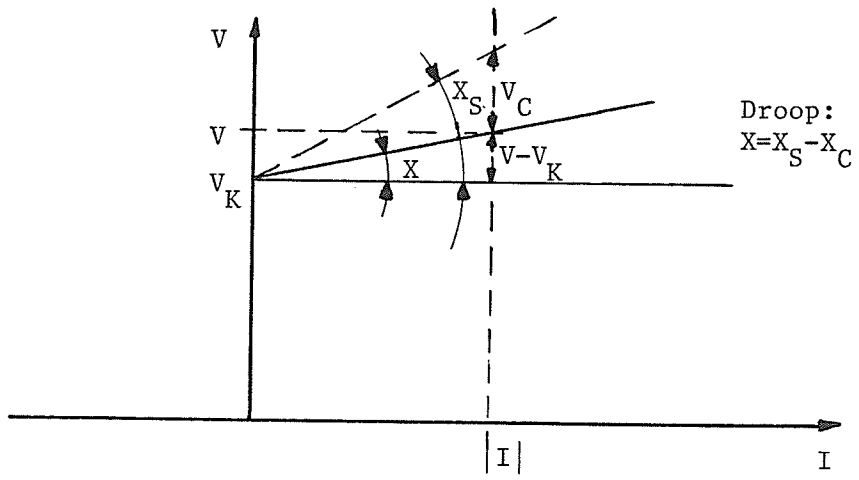
The SR is represented as a saturable inductance with differential impedance X_s in series with the slope correcting capacitor. The capacitor is paralleled by a damping circuit.

In steady state the total impedance of the SR is:

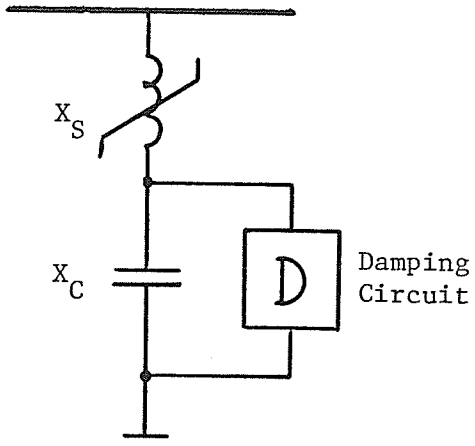
$$\frac{\Delta V}{|I|} = \frac{V - V_k}{|I|} = X_s - X_c = X \tag{3.4}$$



a) Block Diagram



b) Corresponding V-I-Characteristic



c) Single Line Diagram of the SR-Model

Fig. 3.7: CIGRE Representation of an SR

Considering a steplike change in the bus voltage, in the first moment only X_s has an influence on $\frac{\Delta V}{|I|}$. X_c with the damping circuit is approximated in the model with a first order lag function in the feedback loop. A nonlinear function simulates the short-circuiting of X_c if the voltage rises above a certain protection level.

The time constant of the lag function depends on the damping circuit and is suggested to range between 10 and 25 ms. In the linear range the total transfer function for the SR results in a lead lag function:

$$\frac{|I|}{\Delta V} = \frac{1}{X_s - X_c} \cdot \frac{1 + sT_1}{1 + sT_2} \tag{3.5}$$

$$T_2 = \frac{X_s}{X_s - X_c} T_1 \tag{3.6}$$

The system in Fig. 3.7a is actually a positive feedback system but it can be seen that it remains stable for $X_c < X_s$ (T_2 in eq. (3.6) positive). This means, it is stable as long as the droop of the SR has a positive value. On the other hand, the overall loop including the power system still has a negative feedback.

With very small values of X_c our SR model was unstable. This effect was independent of the system and seemed to be a problem of the digital model of the SR. After adding a lag function outside the primary loop (Fig. 3.7a) and after increasing the iteration speed in the program the instability disappeared.

This lag-function did not affect very much the response of the SR. In the example of Fig. 3.8 which shows the response of the SR to a load rejection on a simple L-equivalent (Fig. 3.12), the difference in the voltage after 5 ms is only 0.6% compared to the case without lag

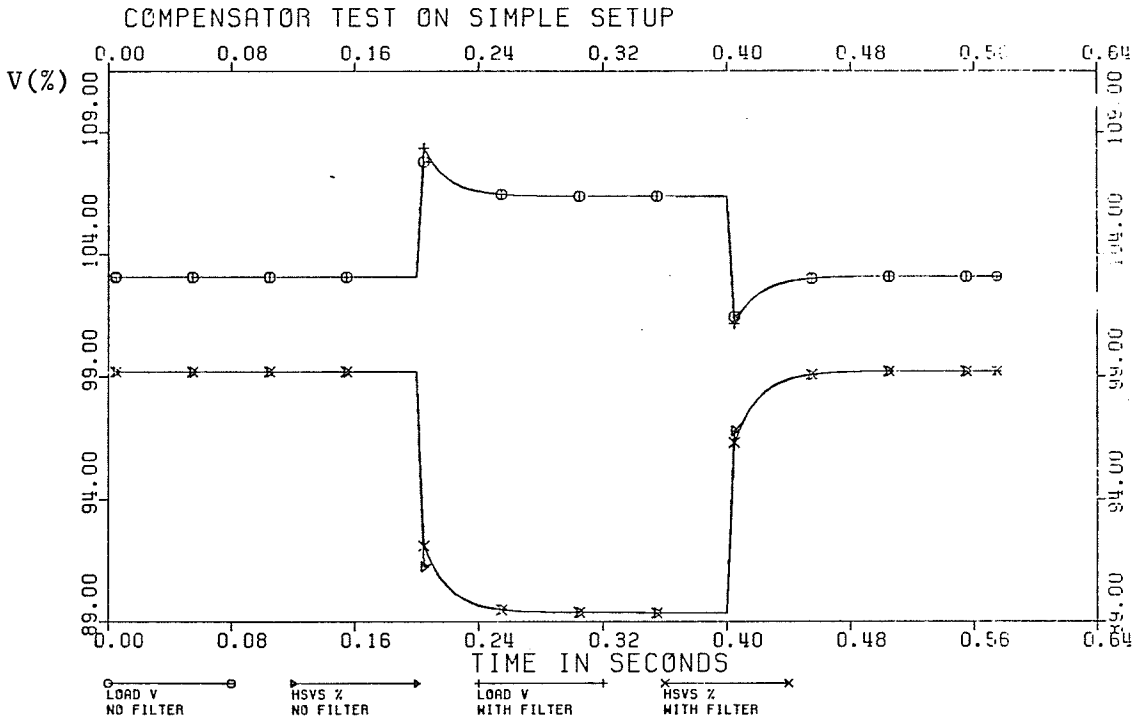


FIG.3.8:SATURATED REACTOR WITH AND WITHOUT FILTER,DROOP=3%

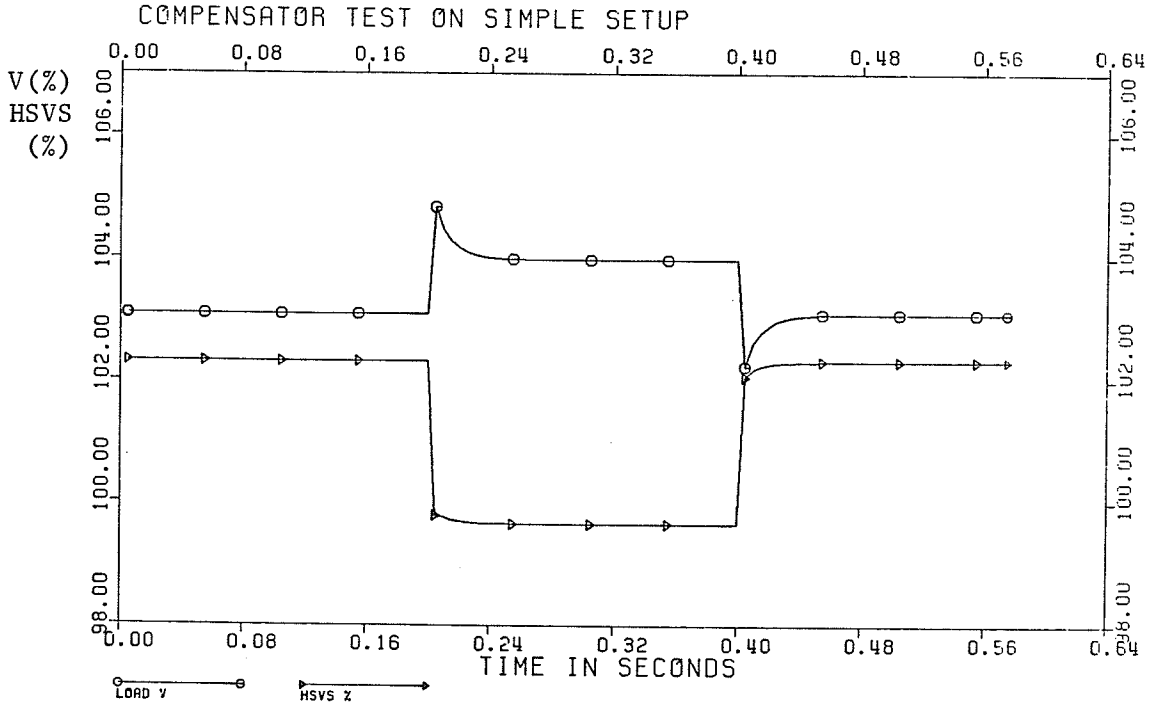


FIG.3.9:STEP RESPONSE OF SR,DROOP=0.625%(3% BASED ON 480 MVA

function. For the test a high X_S had to be taken in order to obtain a stable response in both cases.

The response with lag and low droop (ca. 0.5% based on 100 MVA, 3% based on 480 MVA) is shown in Fig. 3.9. The compensator is able to respond within 25 ms. The difference in the voltage before and after the fault is due to the droop.

3.3.2.2 Universal Model for SVS with TCR and TSC

Although the model of the saturated reactor could be used after minor modifications, the model for the thyristor controlled SVS had to be rewritten completely. This was necessary because the existing model did no more correspond to the modern technology of SVS.

A new SVS model which is based on the same principle of a controlled voltage source behind a constant reactance was implemented. Unlike the existing one, this new model permits simultaneous control of TCR and TSC devices from one single regulator. This is more realistic than the old model which provided two different routines for TCR and TSC since these devices are rarely used independently.

The principle for the regulator scheme was taken from [6.1]. It is a generalized representation of the Brown Boveri design of an SVS. A simplified block diagram of the control loop consisting of SVS and power system is shown in Fig. 3.10. The SVS acts as a voltage controller at the connected bus. The bus voltage is measured, rectified and filtered (G_M) and finally compared with a reference voltage. G_M is represented in [6.1] by a second order low-pass filter. The error signal is then fed into the regulator, usually a proportional-integral-regulator (PI-regulator). The regulator output is proportional to the total admit-

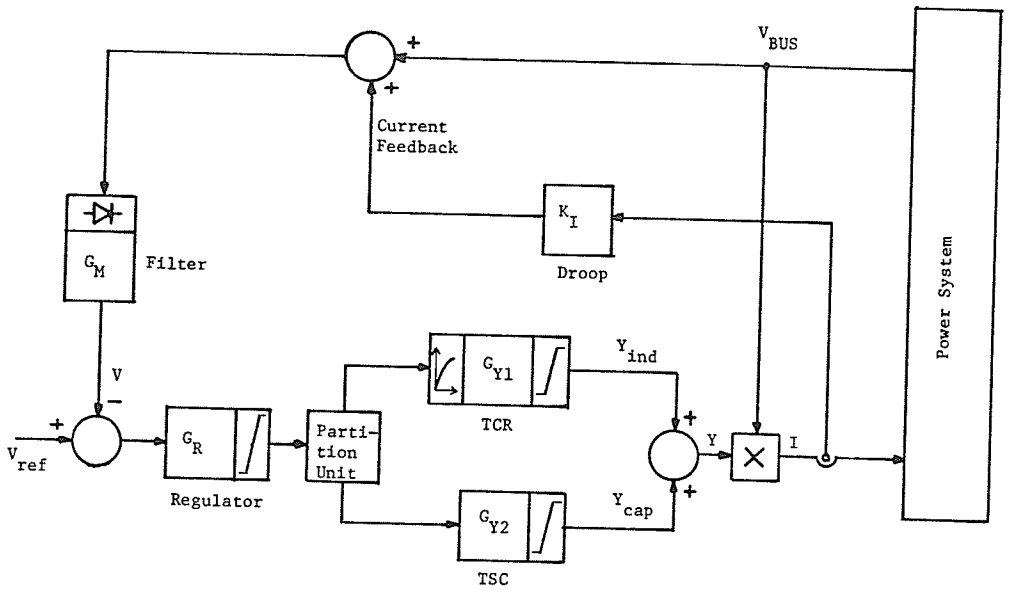


Fig. 3.10: Simplified Block Diagram of SVS with TCR/TSC Connected to a Power System

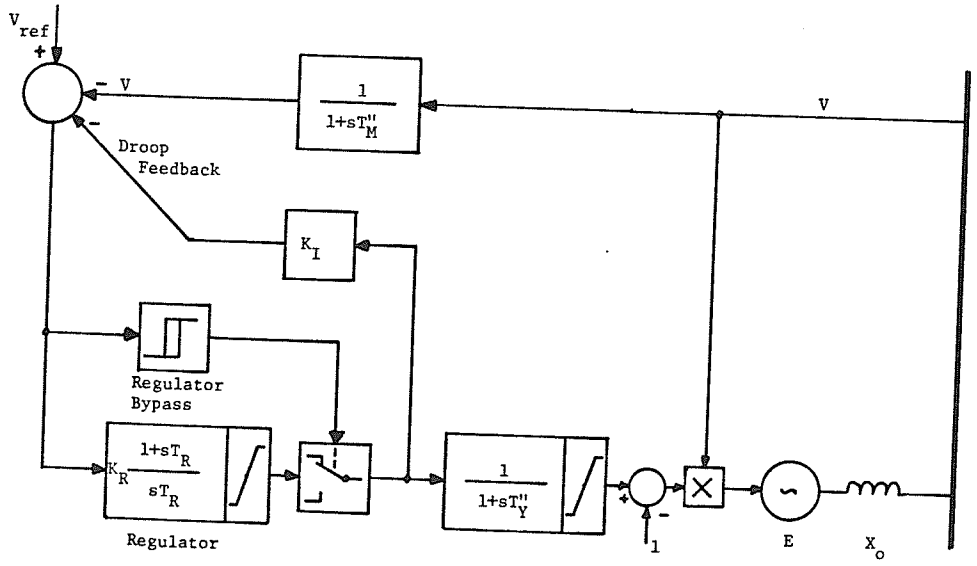


Fig. 3.11: Block Diagram of SVS Adapted to Voltage Source Behind Reactance Model

tance of the SVS and under assumption of only small voltage fluctuations also proportional to the totally required reactive power output. This signal is then split into a reactive and capacitive part. These correspond to the firing angle for the TCR and to the number of TSC steps respectively (for an SVS according to fig. 3.2c).

The TCR Model consists of a linearizer circuit to compensate the nonlinear α vs. I characteristic and of a transfer function G_{y1} which represents the variable admittance. G_{y1} is a lag function of the form:

$$G_{y1} = \frac{e^{-sT_{d1}}}{1 + sT_{y1}} \tag{3.7}$$

T_{d1}: dead time of the TCR, 1/12 cycle in average

T_{y1}: lag time constant which was found experimentally in the paper (4 ms for 60 Hz).

In the TSC path no linearizer is necessary and the transfer function G_{y2} is of the same form as for the TCR. The average dead time of the TSC is somewhat bigger than T_{d1} ($T_{d2} < 1/6$ cycle). But for our purpose it is reasonable to set $G_{y2} = G_{y1}$, since the TSC banks are not switched during each regulator action. The total admittance of the SVS is obtained by adding the capacitive and reactive contributions. The SVS current can then be determined by multiplication with the bus voltage. The droop in the control characteristic of Fig. 3.3 is obtained via a current feedback signal.

For our model of the SVS some simplifications could be made: First the nonlinearity of the variable reactance (α-I-characteristic) was not modelled since it is directly compensated by the linearizing function. The error due to this simplification is negligible. Since the

stability program operates only with phasors, it is not necessary to distinguish between TCR and TSC circuits. They can be concentrated in one transfer function of the form:

$$G_y = \frac{e^{-sT_d}}{1 + sT_y} \tag{3.8}$$

This way the simulation of various compensators can be accomplished simply by changing the maximum specified values of supplied or absorbed reactive power.

The transfer function (3.8) can be further simplified. The dead-time e^{-sT_d} can be approximated by a first order lag function:

$$G_y' = \frac{1}{(1 + sT_y)\,(1 + sT_d)} \tag{3.9}$$

with the value Td = 1.4 ms

Ty = 4.2 ms

for 60 Hz.

Since T_d is much smaller than T_y, both time constants were combined into one first order lag function. Equation (3.9) can be written as

$$G_y' = \frac{1}{1 + s(T_y + T_d) + s^2 \cdot T_y \cdot T_d} \tag{3.10}$$

This expression can be reduced to a first order lag by Chen & Shie's method (see [1.5]) which results in

$$G_y'' = \frac{1}{1 + s(T_y + T_d)} \tag{3.11}$$

$$T_y'' = T_y + T_d = 5.6 \text{ ms for 60 Hz.}$$

In a similar way the second order filter function G_M was simplified since there is no need for filtering the voltage in the model, only the delay of the signal is of importance. The complete filter function in [6.1] is

$$G_M = \frac{1}{1 + 2s\,\xi\,Tm + (sT_M)^2} \qquad (3.12)$$

$$\text{with } T_M = 1.85 \text{ ms}$$

$$\xi = 0.69$$

The first order approximation is:

$$G_M = \frac{1}{1 + sT_M'} \qquad (3.13)$$

$$\text{with } T_M' = 2.55 \text{ ms}$$

In addition to this the voltage rectification causes another deadtime which is 1/12 cycle in average. This deadtime has to be added to the filter time constant and we obtain finally for the measurement transfer function

$$G_M'' = \frac{1}{1 + sT_M''} \qquad (3.14)$$

$$Tm'' = Tm' + 1.2 \text{ ms} = 3.75 \text{ ms}$$

The current feedback for the droop is done with the regulator output signal which is proportional to the current in the active range of the regulator. G_y has been neglected since this way of feeding the droop signal is also used in practice. Although the SVS regulator with current feedback could be combined and expressed by a single lead-lag function as it was done in the old version, some advantages arise when modelled with a PI-regulator plus feedback loop. With the latter scheme for example the regulator output can be held at any value simply by forcing the input to zero, a feature which made the implementation of an override function much easier. Furthermore it is much easier to reconstruct the signal path during a test, the lead-lag function would consist of parameters which are hard to relate to a real system.

Some other features have been added to the model:

- The filter G_M can easily be changed to more complex structures; sufficient space for input parameters is already provided.
- The regulator can be overridden in case of large disturbances in the system to improve the response of the compensator. An application is described in [6.2] and the device has been used in some of the tests.

This new compensator model has been tested on the simple setup of Fig. 3.12. The obtained results were as expected and the model has been assumed to work properly. Some of the results are shown in Fig. 3.13 and 3.14. In Fig. 3.13 a reactor was disconnected at the compensator bus and reconnected after 200 ms. The voltage is settled to a stationary value after 25 ms which corresponds to 1.5 cycles. In Fig. 3.13 the response with changing gain is shown. With low gain the response is slow and aperiodically damped, while the system starts oscillating with too high gains.

In [6.1] the dimensioning criteria for the regulator gain setting has been given as:

$$G_R = \frac{K_R * (1+ sTy)}{sTy} \tag{3.15}$$

and

$$K_R = \frac{1}{2(K_I + k_{N\,max})} \tag{3.16}$$

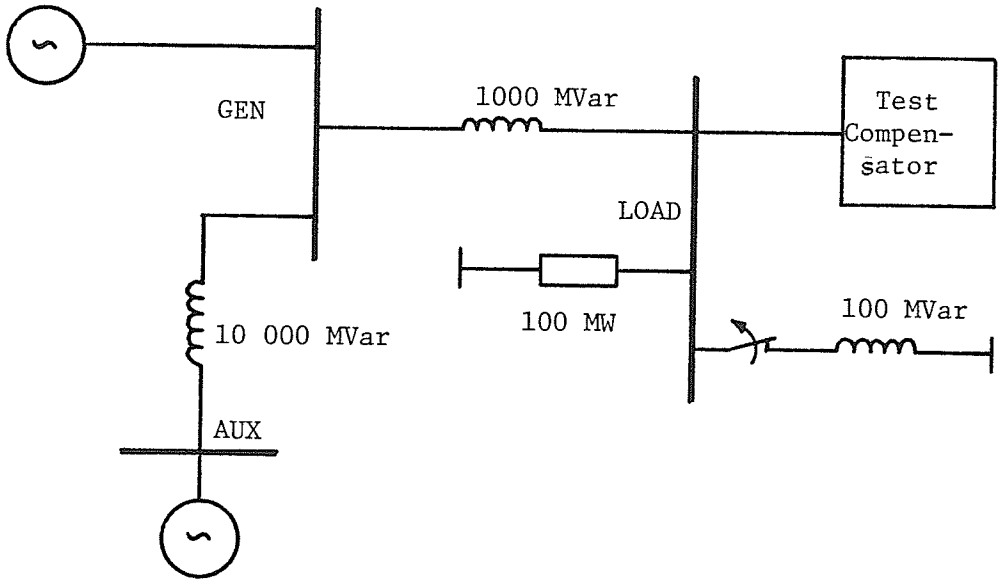
where K_I is the current feedback droop and K_N the system impedance based on the compensator power limits.

This choice of K_R is based on a phase margin of about 70° in the system of fig. 4.10.

In our test setup the short circuit power of the system was about 10 pu. With a droop setting of 3%, K_R came out to be

$$K_R = \frac{1}{2(0.03 + 0.1)} = 3.85$$

In the test we obtained an optimum response of the compensator with K_R = 4.0 which is sufficiently close to 3.85.



Compensator Range:

SR: -100:0 MVar
SVS:-100:100 MVar

Fig. 3.12: Simple Setup for Compensator Tests

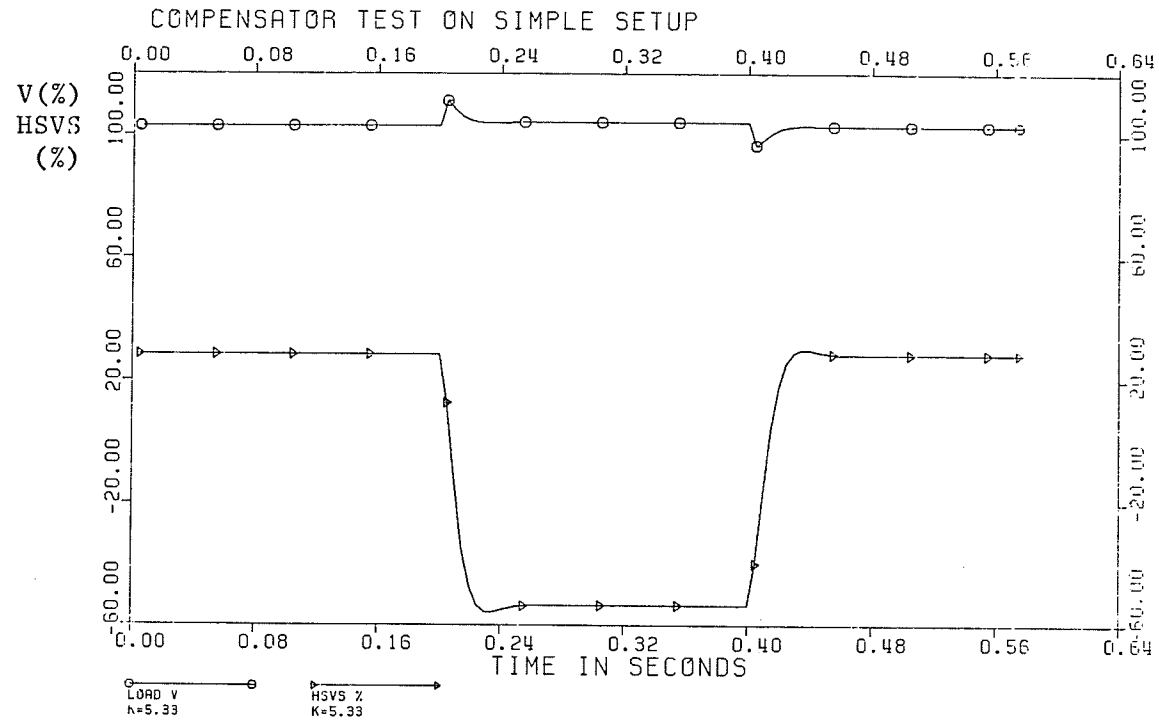


FIG. 3.13: STEP RESPONSE OF SVS, REG. GAIN = 5.33 (OPTIMUM)

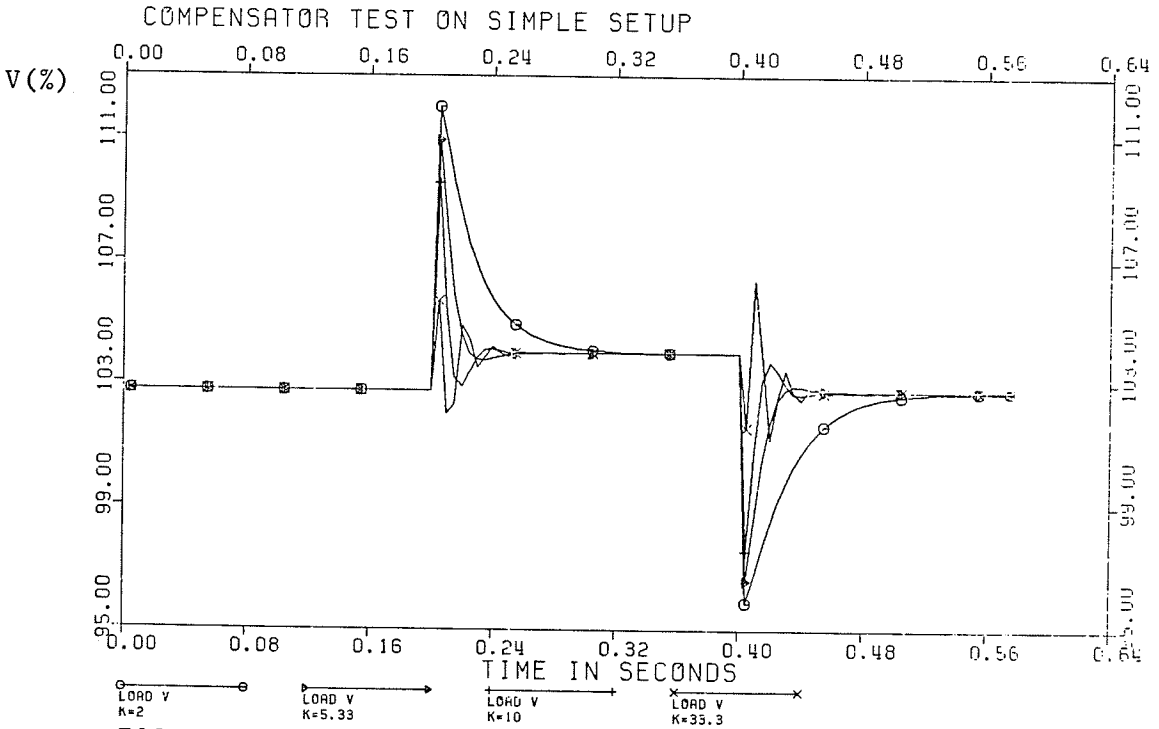


FIG. 3.14: STEP RESPONSE OF SVS WITH CHANGING GAIN K

4. SYSTEM DATA AND SIMULATION

4.1 System Configuration

The Nelson River system with its characteristic parameters had to be modelled for this study. Although some preliminary tests have been done with the present system configuration, here called "reduced system", the final model has been based on the configuration expected for 1990 ("complete system").

A diagram of this complete system is shown in Fig. 4.1. All names and bus or line numbers used in the following discussion are referred to this figure.

The layout consists basically of an HVDC-transmission system with two parallel bipoles of 1700 MW and 2000 MW capacity. On the rectifier side (North end) three generating stations are connected through a short AC-transmission system to the converters. The south or inverter side (Dorsey, DOR) has been approximated by a crude model consisting of an R-L equivalent of a relatively weak AC-system in parallel with a local load, representing Winnipeg. The main differences between the reduced and the complete system representations are summarized in Table 4.1.

The rest of this paragraph is dedicated mainly to the complete system, the same data have been used for the reduced model.

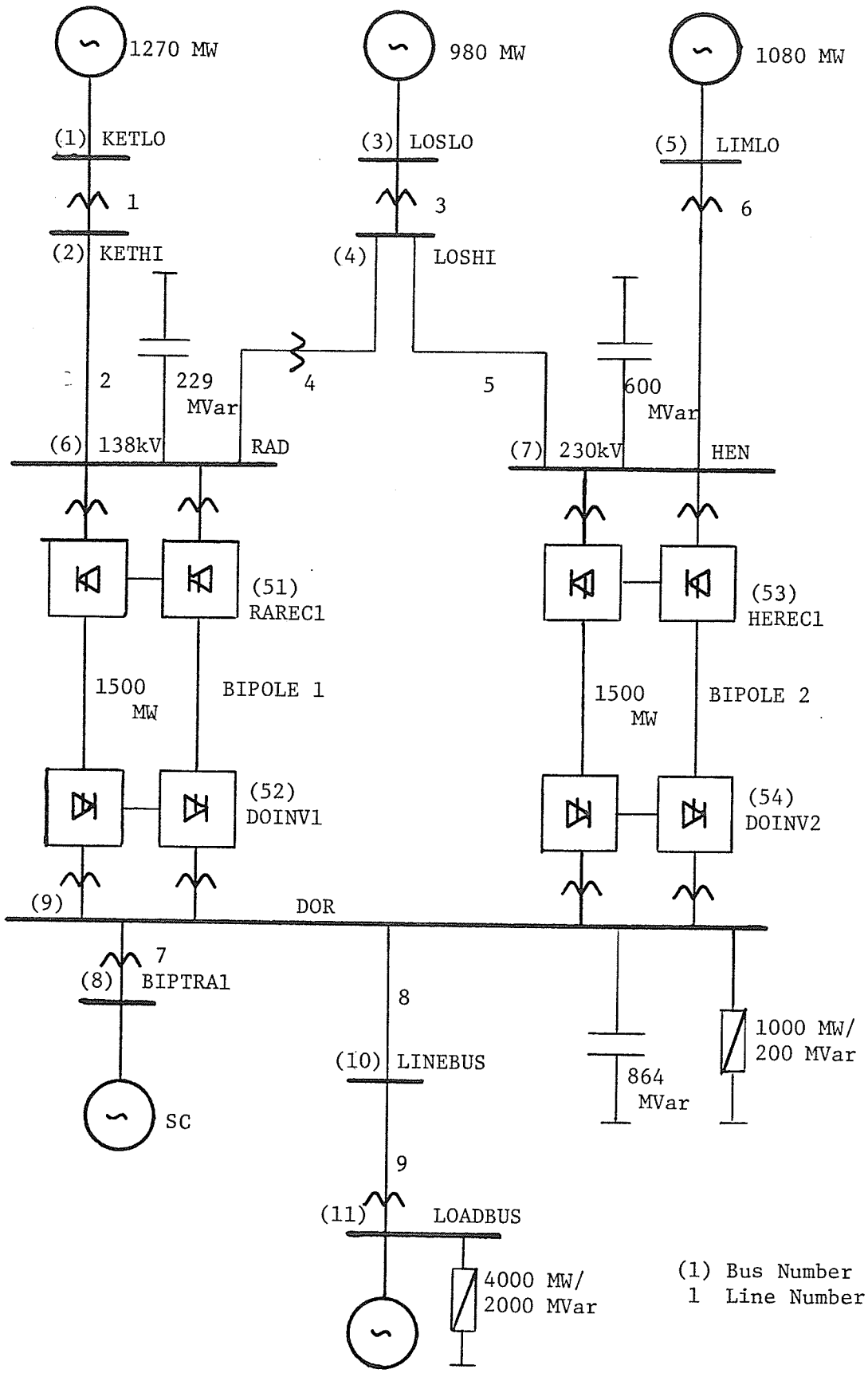


Fig. 4.1: System Configuration ("Complete System")

	Reduced System	Complete System
Generation	2 stations (Kettle and Longspruce) Total max 2250 MW	3 stations (Kettle, Longspruce and Limestone Total max 3330 MW
HVDC-Transmission System	Bipole 1 complete (1620 MW) Bipole 2 first stage (1000 MW)	Bipole 1 and 2 complete (1620 and 2000 MW)
Receiving AC-System	No local load R-L-equivalent for AC-system, SCR = 2.5	Local load 1000 MW/ 200MVar R-L equivalent for AC-System SCR = 2.5...4.5
Reactive Power Generation at Rectifier Bus	Bipole 1: Filters 229 MVar Bipole 2: Filters 600 MVar	same
Reactive Power Generation at Inverter Bus	Bipole 1 & 2: Filters 864 MVar Sync,. Comp. - 320... 640 MVar (4 machines in operation)	Bipole 1 & Bipole 2: Filters 864 MVar Other compensators: - 480...960 MVar (various combinations of SVS and SC, max. 6 machines)

Table 4.1: Basic Differences Between Reduced and Complete Nelson River System Models (Refer to fig. 4.1). All MW Values Shown for Maximum Capacity of the Device.

4.2 System Parameters

This chapter should give a summary of the principal parameters used for the system model according to Fig. 4.1. A detailed list of all model parameters can be found in Appendix B.

All voltages and impedances are given in per unit values with base S_B = 100 MVA and V_B = nominal voltage on the corresponding bus. With this selection all scaling problems for the different voltage levels in the AC-system could be eliminated. DC quantities had to be entered into the program with their actual units. Therefore no per unit representation was used for DC.

4.2.1 Load-Flow

The steady-state behaviour of the complete system can be seen from the results of the load-flow calculation.

Voltage profile as well as generated and absorbed power at each AC-bus are listed in Table 4.2a which shows the computer output for the AC-load-flow. One slack bus on each side of the DC-system was chosen, KETLO on the rectifier side, LOADBUS for the receiving system.

At the inverter bus (DOR) a local load of 1000 MW/200 MVar is connected. The synchronous condensers which are actually connected to the tertiary winding of the converter transformer of Bipole 1 (BP1) had to be connected to an auxiliary bus in the model since the direct representation of a three winding transformer was not possible (see Appendix B).

Six synchronous compensators were assumed to be in service for the load-flow. For the actual stability runs some or all of them could be replaced by static compensators of any type (Chapter 5). As mentioned earlier, the receiving system was approximated by an R-L-equivalent with an impedance angle of 75°.

```
REPORT OF LOAD-FLOW CALCULATION
TOTAL ITERATIONS        7
SWING BUS       11 -LOADBUS         1 -KETLO


X---------------------------- B U S - D A T A ----------------------------X

 BUS     NAME     VOLTS   ANGLE     GENERATION          LOAD          CAP-REAC  REG
                                     MW      MVAR      MW      MVAR    MVAR    BUS

  1   KETLO      1.050    0.0     945.51   589.76     0.0      0.0      0.0
                1.050*
                      TO BUS -    2 KETHI            945.51   589.77    0.980   TAPS

  2   KETHI      1.012   -5.91      0.0      0.0      0.0      0.0      0.0
                      TO BUS -    1 KETLO           -945.51  -462.12
                      TO BUS -    6 RAD              945.50   462.06

  3   LOSLO      1.050    2.89    980.00   462.95R    0.0      0.0      0.0       3
                1.050*
                      TO BUS -    4 LOSHI            980.00   462.95    0.980   TAPS

  4   LOSHI      1.015   -5.03      0.0      0.0      0.0      0.0      0.0
                      TO BUS -    3 LCSLO           -980.00  -306.38
                      TO BUS -    6 RAD              558.67   178.69
                      TO BUS -    7 HEN              421.33   127.70

  5   LIHLO      1.050    1.23   1080.00   608.14R    0.0      0.0      0.0       5
                1.050*
                      TO BUS -    7 HEN             1080.00   608.14    0.980   TAPS

  6   RAD        1.001   -6.92      0.0      0.0      0.0      0.0    229.46
                      TO BUS -    2 KETHI           -943.33  -440.88
                      TO BUS -    4 LCSHI           -556.65  -168.87
                      TO D.C -    51 RAREC1         1500.00   839.31   395.47 KV RMS

  7   HEN        1.002   -6.81      0.0      0.0      0.0      0.0    301.43
                      TO BUS -    5 LIHLO          -1080.00  -422.13
                      TO BUS -    4 LOSHI           -420.00  -126.81
                      TO D.C -    53 HEREC1         1500.00   850.36   426.06 KV RMS

  8   BIPTRA1    1.050   31.57      0.0    825.82R    0.0      0.0      0.0       8
                1.050*
                      TO BUS -    9 DCR               -0.02   825.84

  9   DOR        1.044   31.57      0.0      0.0    1000.00   200.00   942.60
                      TO BUS -    8 BIPTRA1           0.02  -821.51
                      TO BUS -    10 LINEBUS        1865.85  -141.40
                      TO D.C -    52 DOINV1        -1430.79   835.05   365.32 KV RMS
                      TO D.C -    54 DOINV2        -1435.06   870.30   398.03 KV RMS

 10   LINEBUS    1.032   15.36      0.0      0.0      0.0      0.0      0.0
                      TO BUS -    9 DOR            -1731.05   648.49
                      TO BUS -    11 LOADBUS        1731.05  -648.50

 11   LOADBUS    1.100    0.0    3403.74  3655.59  5000.00  2500.00     0.0
                1.100*
                      TO BUS -    10 LINEBUS       -1596.26  1155.59
```

Table 4.2a: Load-Flow Output, AC Solution

AC BUS	DC BUS	NAME	SETTING	NO. BRDG	P DC MW	V DC KV	I DC AMP	THETA DEG	THETA MIN	THETA MAX	XC % /BRG (100 MVA)	E BASE KV	TAP SET	TAP MIN	TAP MAX
9	52	DOINV1													
	INVR	VOLT CONT	890.00	2	-1430.79	890.00	1607.63	18.00	18.00	80.00	2.02	381.0	0.959	0.930	1.280
				TO BUS -	51	RAREC1	-1430.78	MW	-1607.62	AMP					
6	51	RAREC1													
	RECT	POWR CONT	1500.00	2	1500.00	933.05	1607.63	14.26	5.00	80.00	2.08	402.0	0.984	0.930	1.200
				TO BUS -	52	DCINV1	1499.99	MW	1607.62	AMP					
9	54	DOINV2													
	INVR	VOLT CONT	960.00	2	-1435.06	960.00	1494.86	18.00	18.00	80.00	2.10	424.0	0.939	0.950	1.320
				TO BUS -	53	HEREC1	-1435.05	MW	-1494.85	AMP					
7	53	HEREC1													
	RECT	POWR CONT	1500.00	2	1500.00	1003.44	1494.86	14.24	5.00	80.00	2.00	448.0	0.951	0.950	1.320
				TO BUS -	54	DOINV2	1499.99	MW	1494.85	AMP					

D.C LINE DATA

FROM	TO	R OHM
51	52	26.78
53	54	29.06

Table 4.2b: Load-Flow Output, DC-Solution

In order to obtain a correct value for a given SCR, all the impedances of filters and synchronous compensators at DOR had to be considered. The equivalent of the DOR-bus was given as follows:

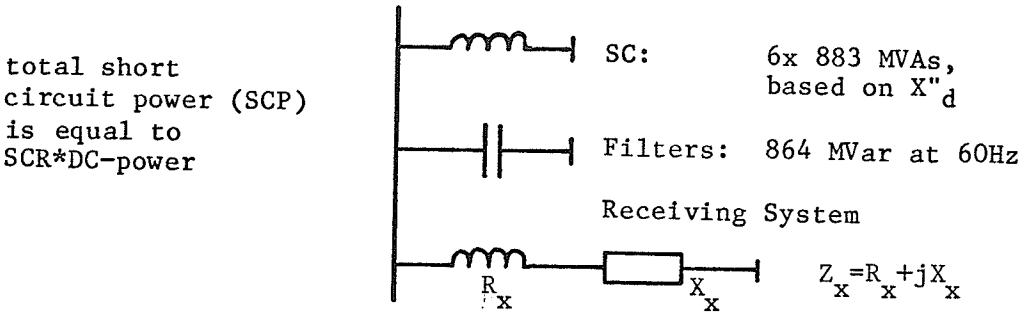


Fig. 4.2: Equivalent at DOR-Bus for Calculation of line Parameters.

While the SC added to the strength of the system, the impedance of the filter banks had the opposite effect.

The impedance of the receiving system was calculated as follows:

$$Z_x\ (\%) = \frac{100\ \text{MVA} \cdot 100\%}{\text{SCP} + 864\ \text{MVA} - 6 \cdot 883\ \text{MVA}} \qquad (4.1)$$

$$R_x = Z_x \cdot \cos 75°$$

$$X_x = Z_z \cdot \sin 75°$$

In Table 4.3 the impedance values for various SCR as used in the following tests are given:

SCP(MVA)	SCR	Z_x (%)	R_x(%)	X_x(%)	
7500	2.5	3.26	0.84	3.16	Values for LF in Fig. 4.2
9000	3	2.19	0.56	2.12	
13500	4.5	1.10	0.28	1.26	

Table 4.3: Receiving End Parameters in Function of SCR and Based on 3000 MW Transmitted DC Power

The results of the DC-load-flow are shown in Table 4.2b. All important DC parameters can be taken from this table. The total transmitted power

was chosen as 3000 MW, by allocating 1500 MW on each of the two bipoles (1500 MW and 500 MW for the reduced system).

4.2.2 Machine and Compensator Modelling

On the north end of the system are three generator stations. The machines of each station have been condensed into one equivalent machine. The parameters of the three resulting generator equivalents have then been adapted to the subtransient machine model available in the program.

For details about machine, exciter and governor data please refer to Appendix B.

The same machine model has been used for the synchronous compensators at the inverter bus. In the same way as for the generators, one equivalent machine with averaged parameters was used. In Table 4.4 parameters are shown for the equivalent of 1 to 8 synchronous compensators.

The static compensators were also connected to the inverter bus, the power ratio (Q max cap)/(Q max ind) was 2; the same value as for the SC. Saturated reactors absorbed, in steady state, 0 MVar with the same nominal power as the SVS.

Machine Data

All reactances in %, based on 100 MVA. Time constants in seconds. Calculation based on assumption of 50% ASEA and 50% English Electric machines.

Parameters		Number of Units				
		1	2	4	6	8
X_d	%	99.31	49.66	24.83	16.46	12.41
X_q	%	65.53	32.77	16.38	10.9	8.19
X'_d	%	19.72	9.86	4.93	3.28	2.47
X''_d	%	10.91	5.46	2.73	1.8	1.36
X''_q	%	14.72	7.36	3.68	2.45	1.84
H	%	2.72	5.44	10.88	16.33	21.76
X_o	%	7.66	3.83	1.92	1.27	0.96
T'_{do}	%	10.25	10.25	10.25	10.25	10.25
T''_{do}	%	0.11	0.11	0.11	0.11	0.11
T''_{qo}	%	0.32	0.32	0.32	0.32	0.32

Table 4.4: Equivalent Parameters of SC Model

5. DYNAMIC OVERVOLTAGE TESTS

5.1 Summary

In the previous chapters the aim of the study has been outlined, and a description of the HVDC system on which our simulation was based as well as a comparison of various types of reactive power compensators have been given. In the actual tests the response of the system with all evaluated types of Var compensators had to be investigated. In order to find a representative disturbance for studying dynamic overvoltages (DOV) we made use of the experiences of Manitoba Hydro from previous tests. It appeared that the blocking of one or two bipoles was a representative fault. Hence for the whole study two fault cases were used:

1) Blocking of bipole 1

2) Blocking of both bipole 1 and 2

The tests were started directly with those two large disturbances because of the following reasons: Firstly the response of the present system with SC was already known. This enabled us to check the validity of the obtained results. Secondly the compensators have already been tested on a simple setup as described in the previous chapter and only the regulator gain had to be set for the new system. This had to be done by trial because of the complex system configuration. The results are presented in section 5.8.

As criterion to test the effectiveness of each compensator type the dynamic overvoltages created at the Dorsey-bus have been looked at. DOV gives a good understanding of the dynamic performance of the

compensators, especially by looking at the system behaviour in the moment of the fault and some time after the disturbance.

The overvoltages are characterized by three criteria in order to find a base for the valuation of each compensator type:

1) The peak voltage is measured in each test, which supplies information about the insulation level required for the application.
2) The shape of the voltage curve is discussed as a visual criterion to compare stability and regulation speed.
3) In order to determine the stresses in surge arresters and other equipment which could not be modelled in the tests, some information about the heat dissipation to be expected in such a device has to be found. Such information could be obtained by integrating the bus voltage over a certain time. This integration could give a good idea about the energy to be absorbed for example by a surge arrester. The integral was chosen as

$$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt \qquad (5.1)$$

V = bus voltage at time t

V_o = prefault bus voltage, was subtracted in order to compare tests on common base

t_F = fault time

For the systematic performace evaluation of the various Var systems it was decided to use the same tests with all combinations of Var sources. The implication was to use constant system parameters for all compensator types. This resulted in much lower SCR than the original value of 2.5 for some tests with static compensators. This point should be kept in mind when studying the performance of static compensators.

The purpose of this chapter is only to describe each test and to show the results in a systematic form. A comparative analysis follows in Chapter 6. Table 5.1 gives a summary of the cases studied here. In the last section of this chapter some results with small disturbances are presented to illustrate the compensator performance under normal operating conditions.

Test	System Configuration	Compensator Type	Section
Large disturbances (Blocking of one or two Bipoles)	reduced system	4 SC	6.2
	complete system	6 SC	6.3
	complete system	SR	6.4
	complete system	SVS	6.5
	complete system	SC & SR	6.6
	complete system	SC & SVS	6.7
Small disturbances	complete system	SC & SVS	6.8
	complete system	SC & SR	6.8

Table 5.1: Summary of Tests Cases

5.2 Tests with SC on Reduced System

The main purpose of these tests was to check the validity of the system modelling and to assure the proper function of the simulation program. The system configuration has already been described in Chapter 4. For this test only 4 SC were in operation at Dorsey bus which resulted in a total maximum reactive power supply of +640 MVar from the machines.

The results of a blocking of both poles of BP1 are shown in Fig. 5.1 to 5.5. The DC fault was applied at t = 200 ms. This loss of 1500 MW causes an immediate rise of the AC-voltage at Dorsey to a value of 1.23 pu (see Fig. 5.1). This is followed by a slower rise of up to a maximum of 1.32 pu, 80 ms. after BP1 has been blocked. The second curve in Fig. 5.1 shows the voltage at the SC-terminal which is connected to the tertiary winding of the converter transformer of BP1.

In Fig. 5.2 of the same run the first curve corresponds to the reactive power of the SC's. Initially supplying about 370 MVars, the SC's absorb a large amount of reactive power (ca. - 550 MVars) immediately after the overvoltage appears at the bus, due to the subtransient reactance X''_d of the machines and due to the change in the bus angle (Fig. 5.3). Q follows the bus voltage for some time and then the influence of the exciter control takes over and increases the reactive power absorption. It can also be seen from Fig. 5.2 that the real power P of the SC is zero in steady state and starts oscillating due to the machine inertia after the disturbance in the bus angle.

The DC-power on BP1 drops to zero while BP2 keeps its original power as a result of the power regulator at the rectifier (see also change in HEN ALPH, the angle α at Henday; curve 5 in Fig. 5.3). The extinction angle γ of BP2 (DOR2 GAM) stays on its minimum value of 18° over the whole run.

The DC voltages and currents in Fig. 5.4 look reasonable as well as the AC-Voltages on the generator side which are shown in Fig. 5.5. It should be noted that on the generator end the frequency is not stable after the fault and therefore the bus angles drift away. This effect is not shown in a figure since the results are not considered realistic

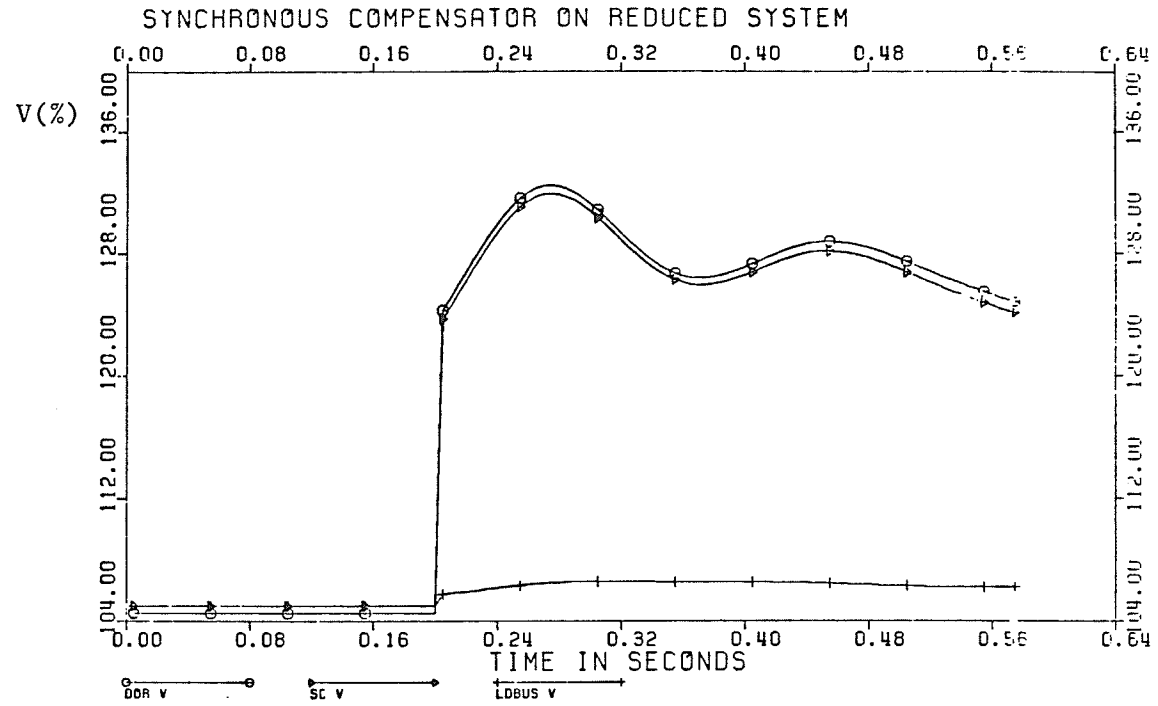


FIG.5.1:SC ON REDUCED SYSTEM,BIPOLE 1 BLOCKED

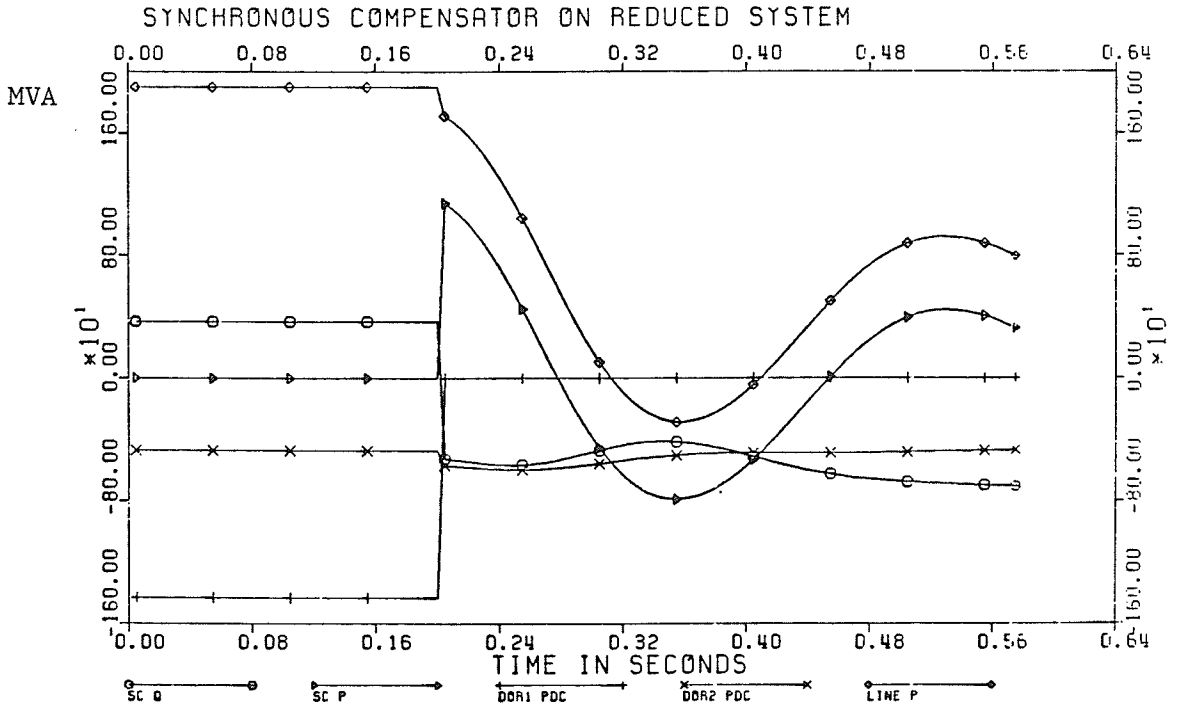


FIG.5.2:SC ON REDUCED SYSTEM,BIPOLE 1 BLOCKED

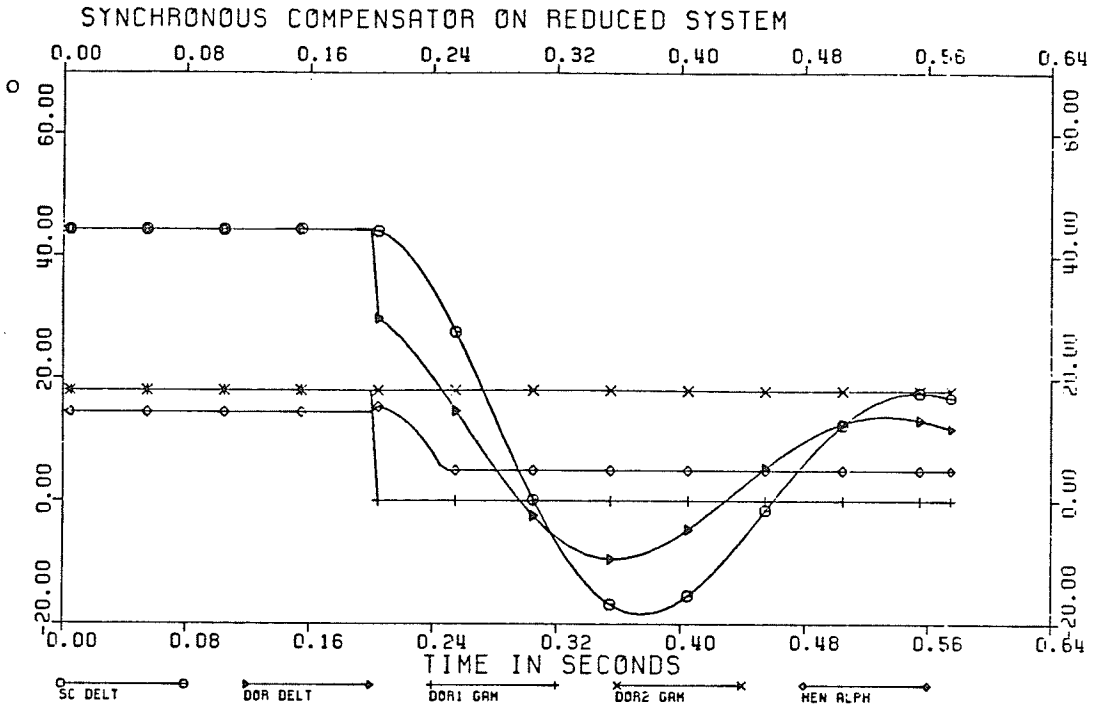


FIG.5.3:SC ON REDUCED SYSTEM,BIPOLE 1 BLOCKED

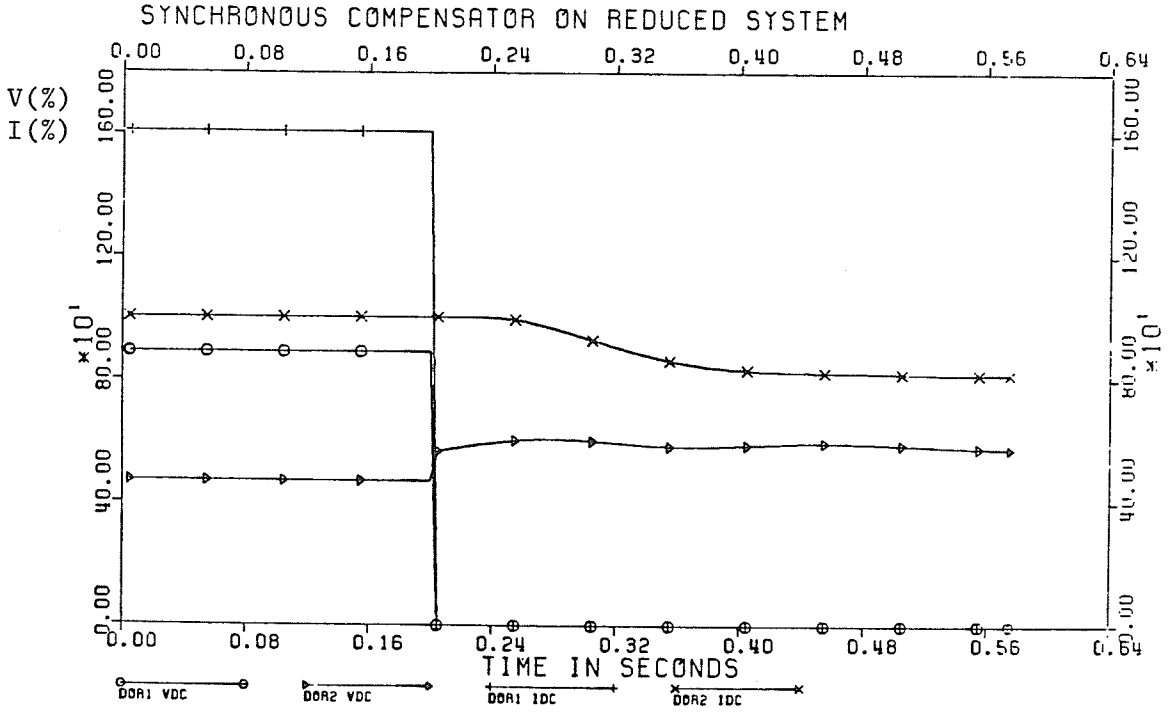


FIG.5.4:SC ON REDUCED SYSTEM,BIPOLE 1 BLOCKED

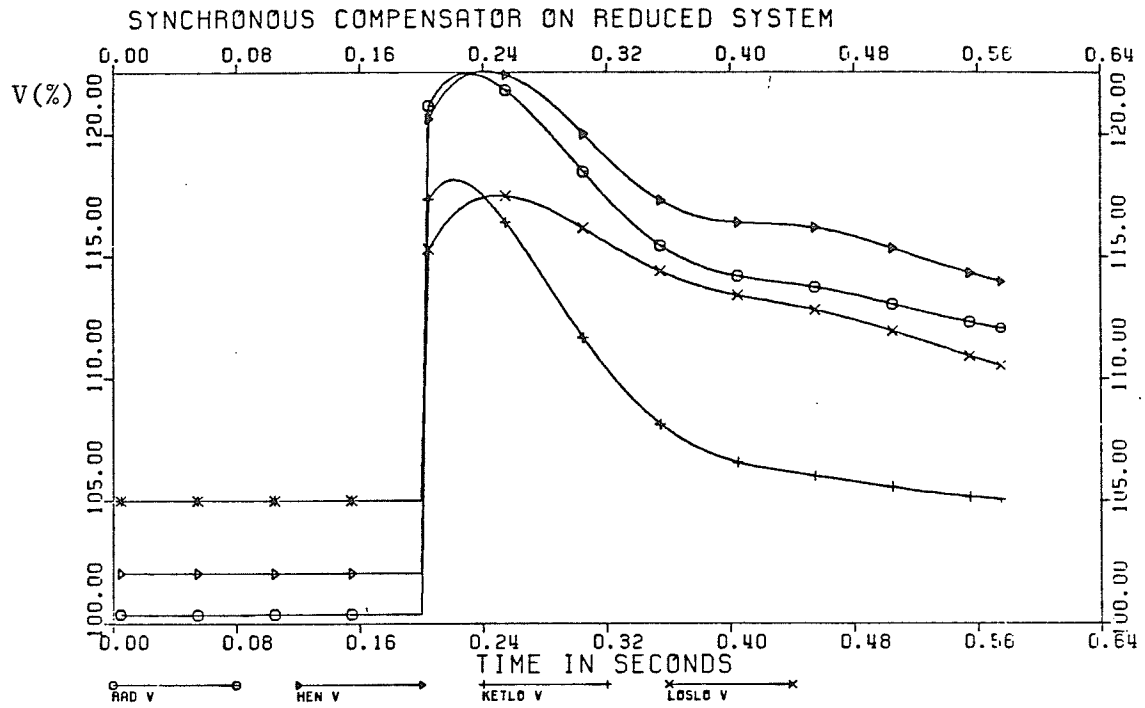


FIG.5.5:SC ON REDUCED SYSTEM,BIPOLE 1 BLOCKED

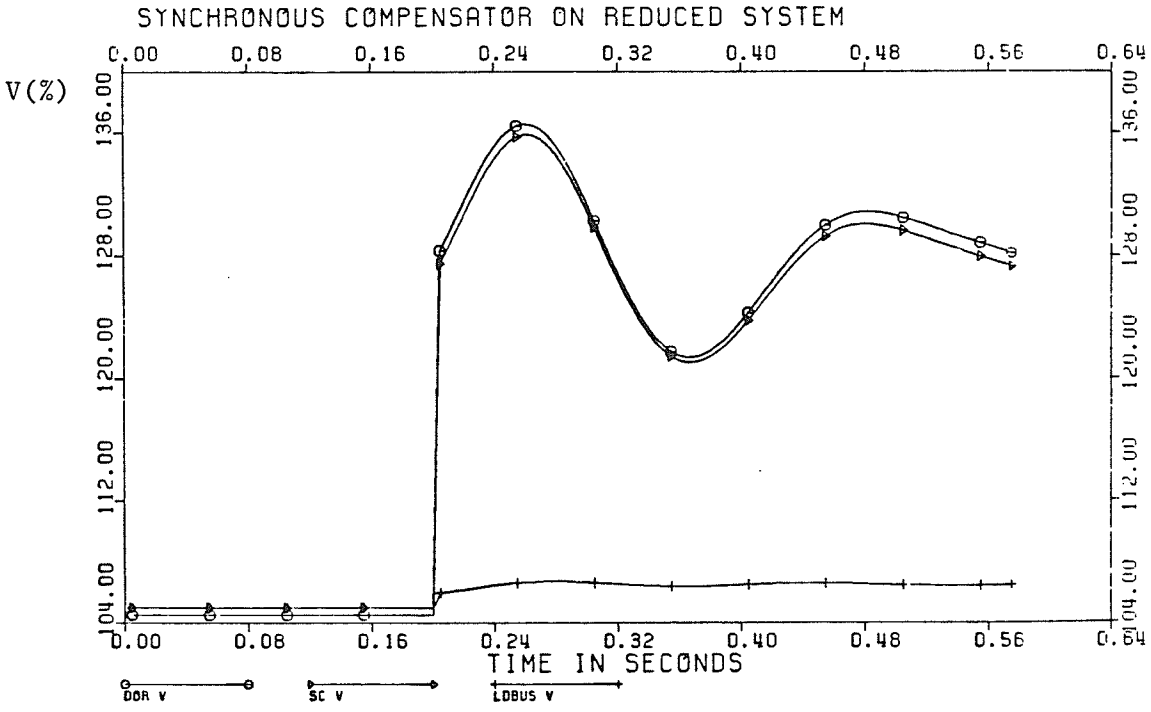


FIG.5.6:SC ON REDUCED SYSTEM,2 BIPOLES BLOCKED

after 100 to 200 ms after fault application because no protective actions were simulated in this study.

But these results in the first 100 to 200 ms after fault, when compared with the data given by Manitoba Hydro, seem to be valid and confirm the proper function of the system representation and of the stability program itself. An overvoltage of 1.3 pu was expected for this case, the value actually obtained is very close to this.

Similar results were obtained with the blocking of both bipoles as shown in Fig. 5.6. The voltage at the inverter bus rises up to about 1.36 pu, somewhat higher than in the previous case and the waveform is very similar.

5.3 Tests with SC on Complete Systems

The same tests as described in the previous section have been performed with the complete system. In order to meet the additional Var requirements at Dorsey, 2 SC had to be added. The total installed controllable reactive power was therefore 960 MVar capacitive to -480 MVar reactive, with 6 SC. The filters remained unchanged (864 MVar).

In Fig. 5.7 the response of the DOR bus to the blocking is very similar to the case with the reduced system. The maximum overvoltage is somewhat lower than with the reduced system since the rejected load is still 1500 MW but the AC system was dimensioned substantially stronger in order to obtain an SCR of 2.5. The bus voltage immediately after the fault rises up to 1.16 pu and reaches its maximum value of 1.2 pu after about 75 ms. The SC's respond in the same way as with the reduced system although they still supply a small amount of capacitive power after the

fault (Fig. 5.8). The energy integral W is listed in Table 5.2 for some characteristic time steps.

$t-t_F$	5	10	25
$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt$	$1.25 * 10^{-3}$	$2.49 * 10^{-3}$	$6.63 * 10^{-3}$

50	150	ms
$14.45 * 10^{-3}$	$45.3 * 10^{-3}$	pu

V_o = pre fault voltage

Table 5.2: One Bipole Blocked with SC: Energy Integral W.

For the test in Fig. 5.9, the same setup has been used but both bipoles have been blocked. The maximum overvoltage obtained in this case was 1.28 pu after 50 ms.

A comparison of the voltage behaviour has been done for changing SCR at Dorsey and with one blocked bipole. the results are illustrated in Fig. 5.10 and Table 5.3 which shows the voltage at DOR for SCR 2.5, 3, 4.5.

SCR	2.5	3.0	4.5	
VMax	1.20	1.15	1.11	pu
at time	75	55	50	ms

Table 5.3: Maximum Overvoltage with Changing SCR

The results show very clearly that the overvoltage to be expected is the highest with lowest short circuit ratio. Therefore all subsequent tests have been performed with a SCR of 2.5 to determine the worst

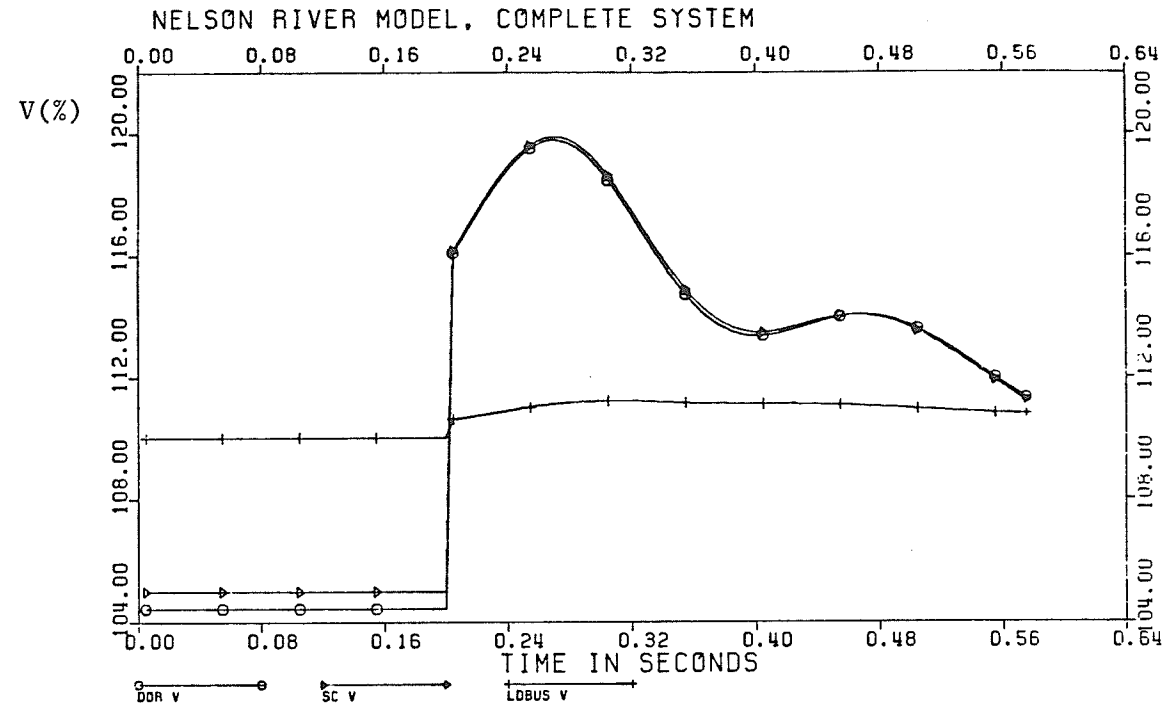


FIG.5.7:SC ON COMPLETE SYSTEM, BIPOLE 1 BLOCKED

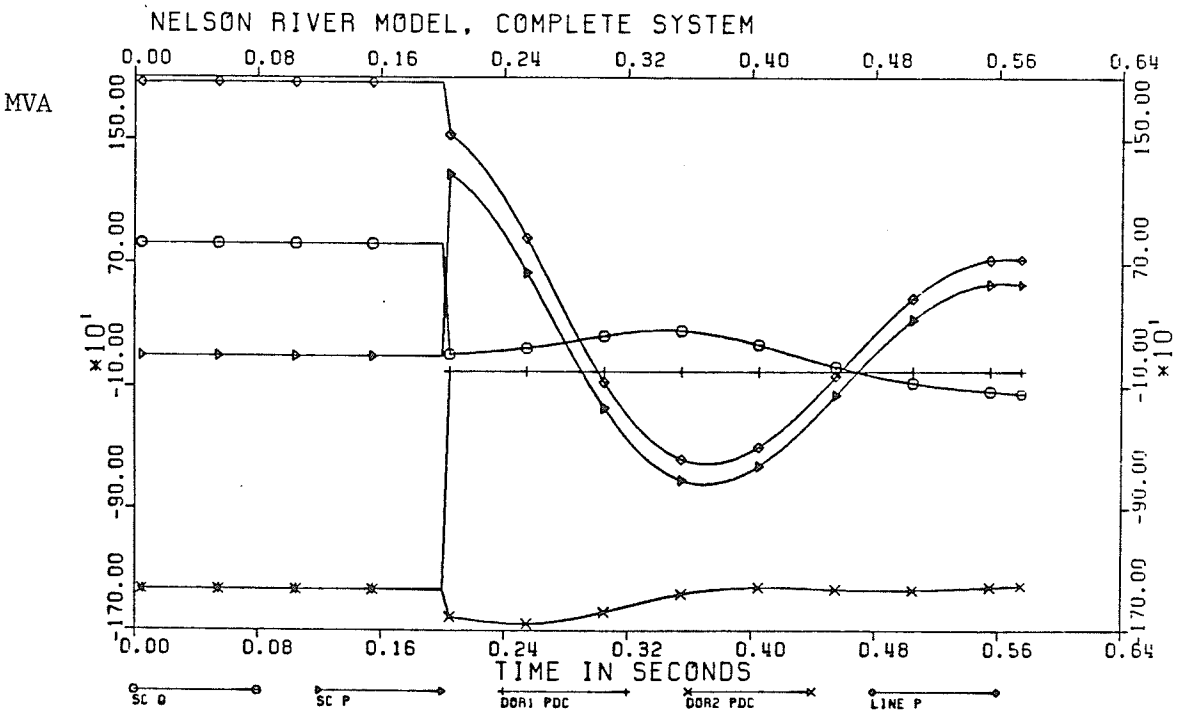


FIG.5.8:SC ON COMPLETE SYSTEM, BIPOLE 1 BLOCKED

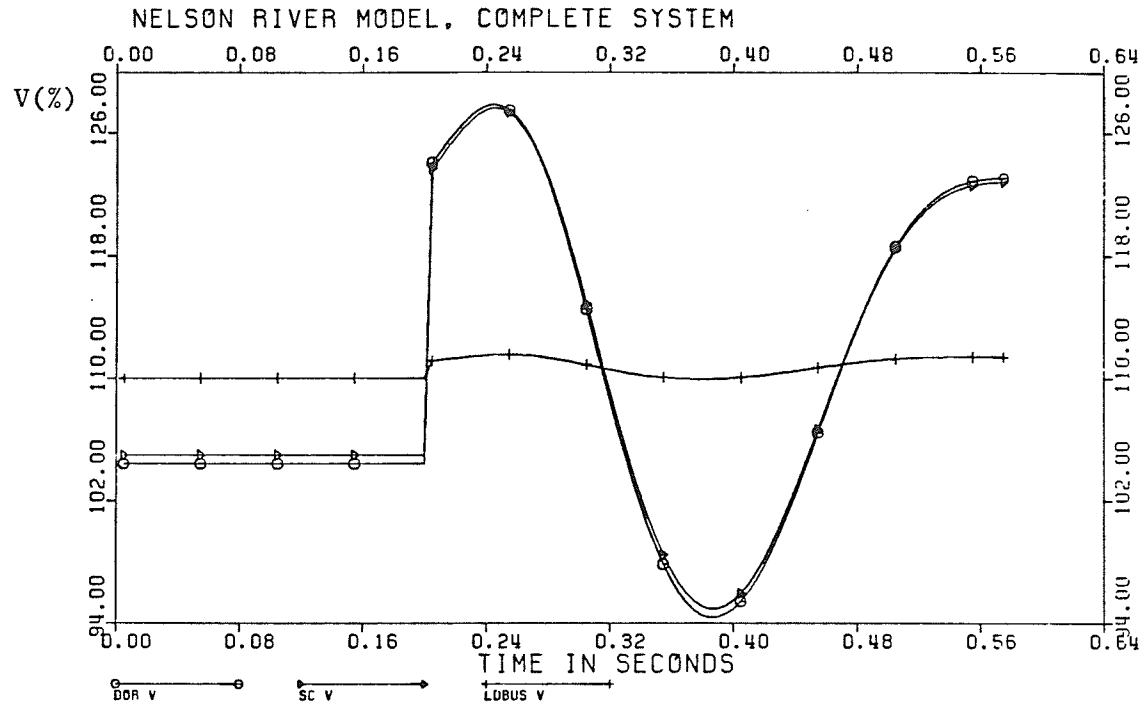


FIG.5.9:SC ON COMPLETE SYSTEM, 2 BIPOLES BLOCKED

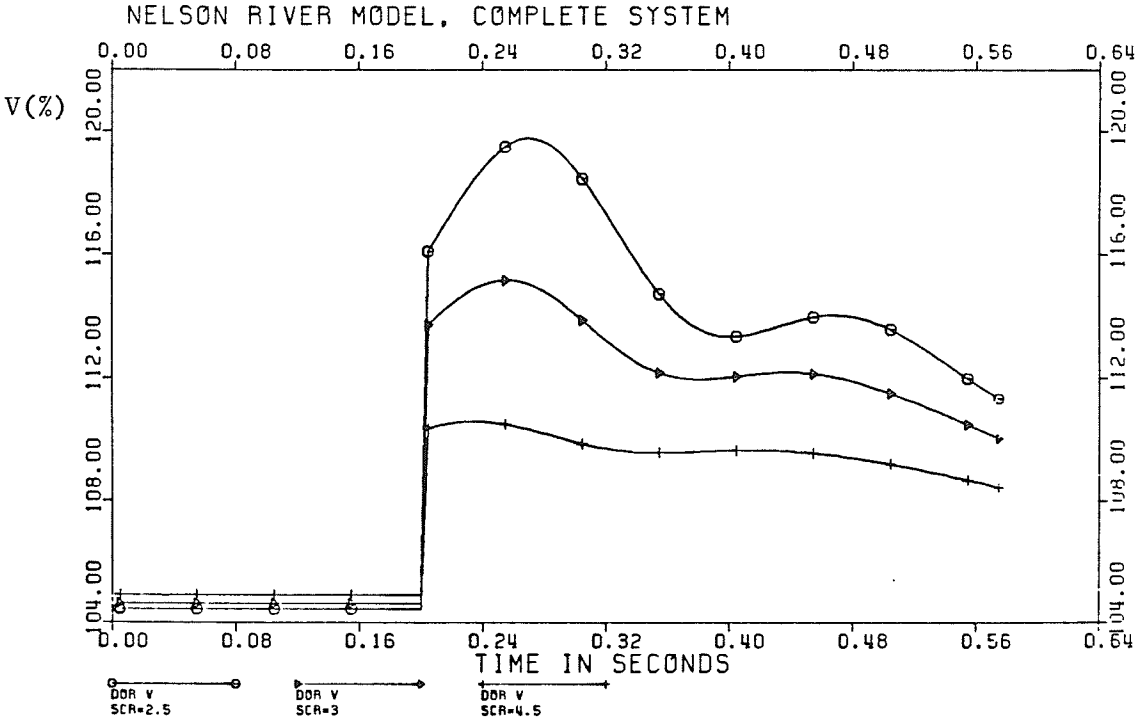


FIG.5.10:SC ON COMPLETE SYSTEM, BIPOLE 1 BLOCKED,

situation. It is interesting to note that the instant when the maximum peak occurs depends on the SCR, the frequency of the angle oscillation increases with a stronger system.

5.4 Tests with Saturated Reactors on Complete System

For this series of tests the only controllable Var source was a saturated reactor with a nominal power of 480 MVars. Additional fixed capacitors (765 MVar) supplied sufficient capacitive power to the inverter stations.

With SR the behaviour of the system was completely different from the last cases with SC. Now the voltage shows a higher but short duration peak immediately after the fault, which decreases to a much lower value depending upon the droop of the SR. Fig. 5.11 shows the voltage at DOR for a SR with a droop of 3% (based on 480 MVar). The maximum overvoltage lies around 1.18 pu and after about 45 ms the voltage is resettled to 1.09 pu.

The value of the first peak can not exactly be determined since the program does not give correct results for the first iteration after the fault. The way the program works is that at first it computes a new load-flow balance for the disturbed case and prints it out. Only after this all the controller settings are recalculated. This does not correspond with the nature of the SR which reacts immediately after going into saturation.* It is to be noted that no more oscillations, as with

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*The nonlinear impedance of the SR is simulated by a control function in order to use a linear reactance in the system matrix.

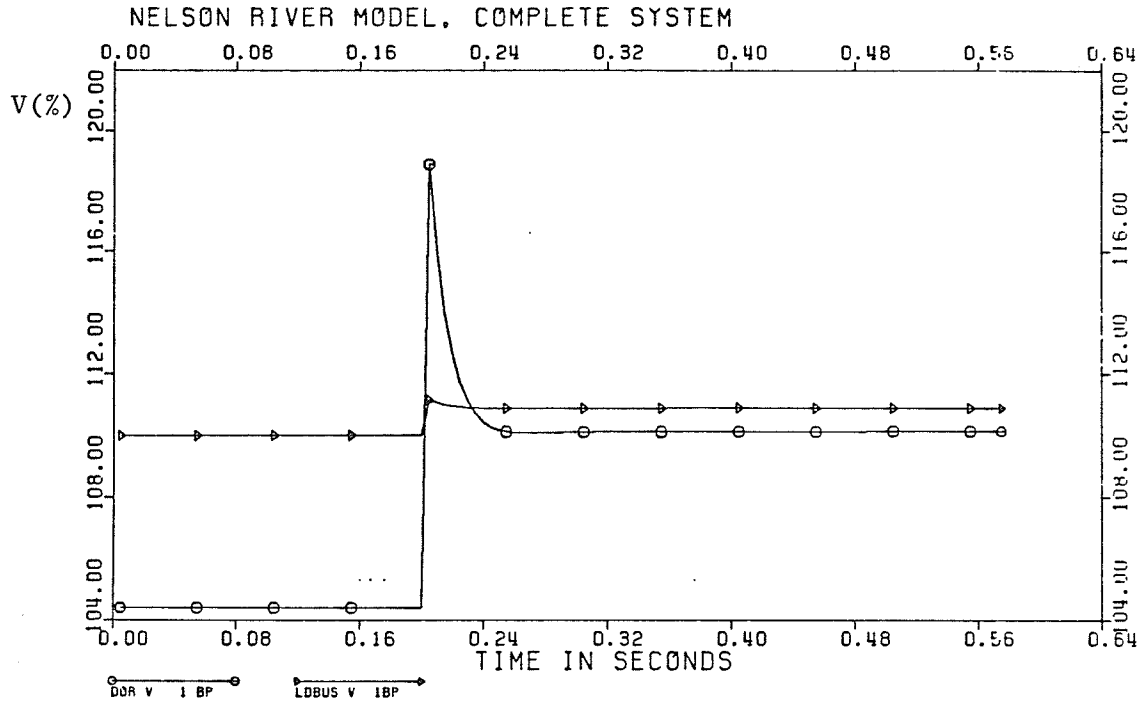


FIG.5.11:SR ON COMPLETE SYSTEM, BIPOLE 1 BLOCKED,DROOP=3%

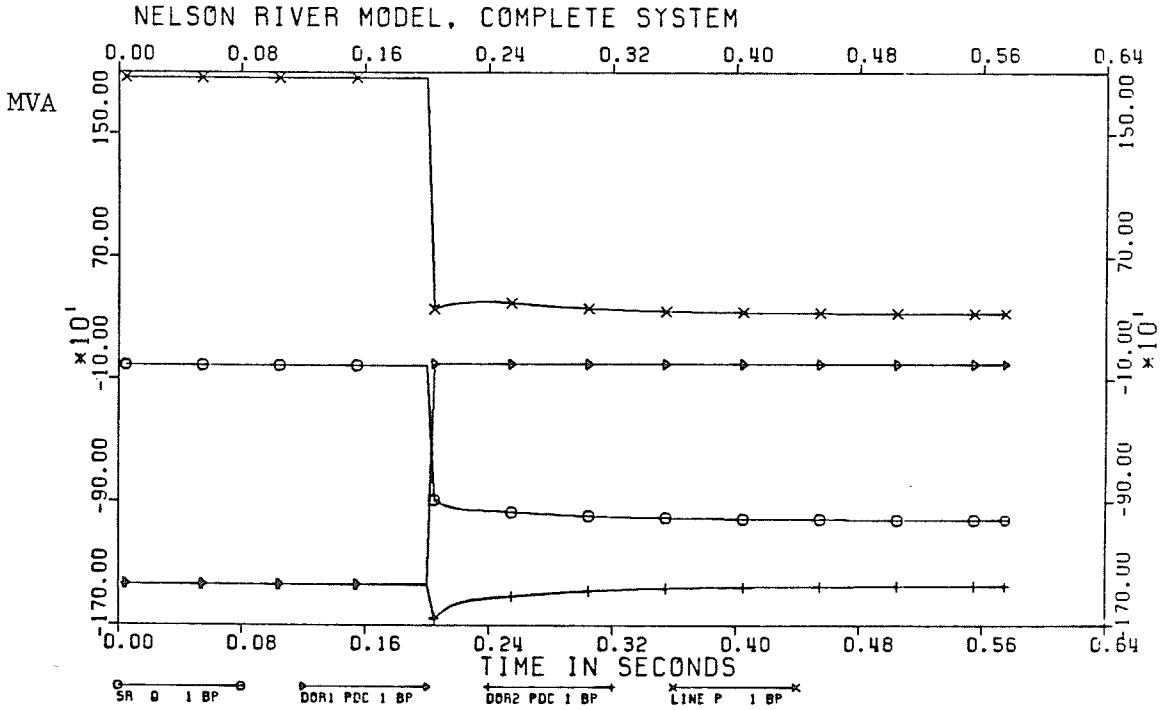


FIG.5.12:SR ON COMPLETE SYSTEM, BIPOLE 1 BLOCKED

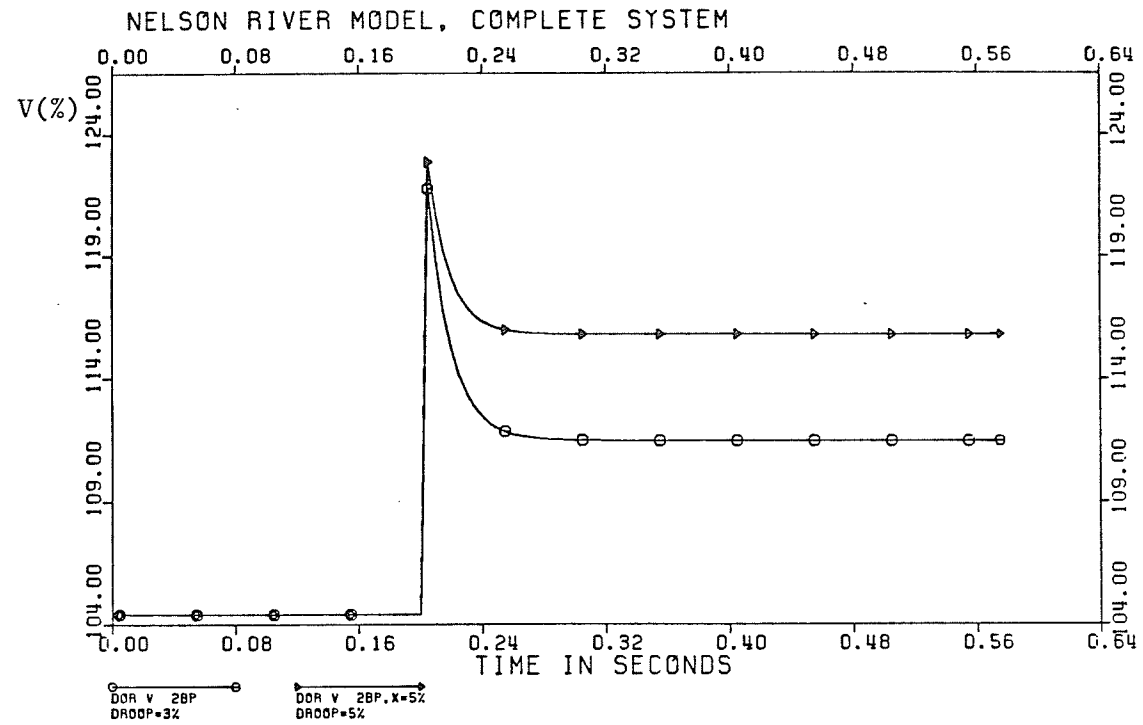


FIG.5.13: SR ON COMPLETE SYSTEM, 2 BIPOLES BLOCKED

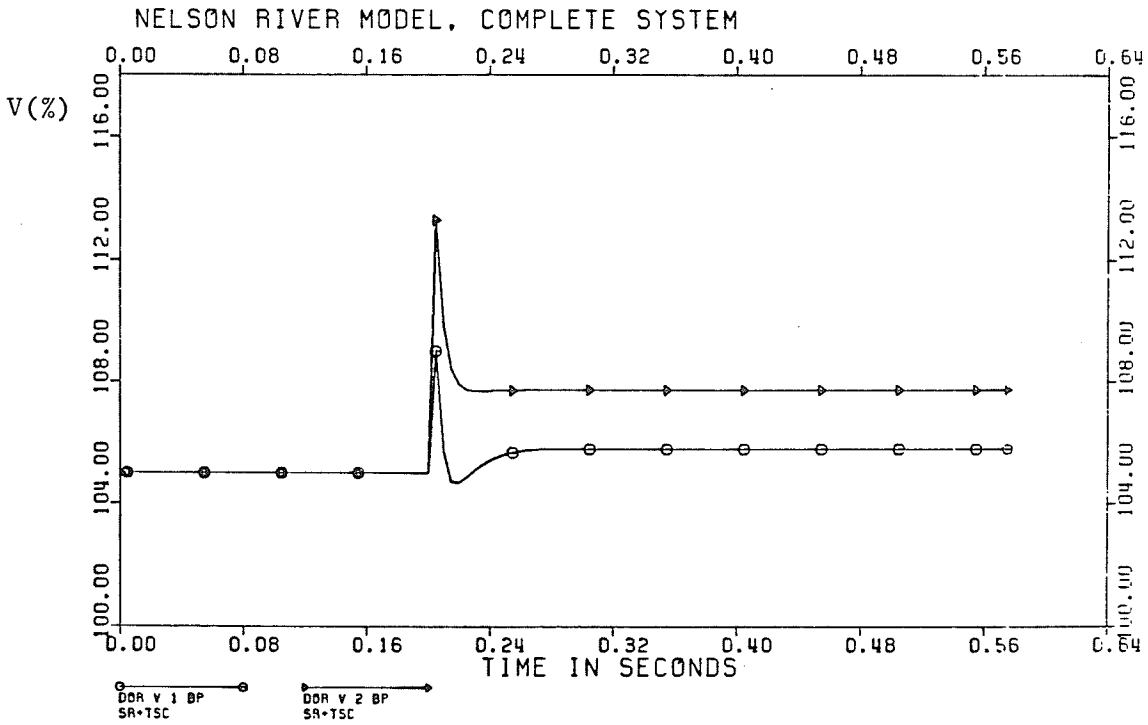


FIG.5.14: SR WITH TSC ON COMPLETE SYSTEM

the SC, occur now. The SR absorbs in a very short time more than 950 MVar and remains near this value for the rest of the run (Fig. 5.12). In Table 5.4 again the energy integral W is listed.

$t-t_F$	5	10	25	50	150	ms
$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt$	$2.36 * 10^{-3}$	$4.30 * 10^{-3}$	$7.26 * 10^{-3}$	$10.7 * 10^{-3}$	$22.9 * 10^{-3}$	pu

Table 5.4: One Bipole Blocked with SR.

Similar results are obtained when two bipoles are blocked, the maximum overvoltage in this case is around 1.22 pu (Fig. 5.13, curve 1). Curve 2 in Fig. 5.13 is also with both bipoles blocked but the droop of the SR is 5%. The transient peak is practically not affected while the final postfault voltage is substantially higher.

A last test with SR has been done together with thyristor switched capacitors instead of fixed capacitor banks. As soon as the bus voltage passes 1.1 pu, the TSC are switched off with a very short delay (Fig. 5.14). The first peak is again smaller than before (now ≈ 1.09 pu with 1 blocked bipole) because almost 50% of all the capacitors are turned off after a few milliseconds. The steady-state postfault value is smaller too since less MVars have to be absorbed by the SR.

5.5 Tests with SVS on Complete System

This series of tests has been done after substituting all 6 SC by static compensators with TCR/TSC. This means that one SVS with the operating range from -480 to 960 MVar was connected to DOR. The installed filter capacity remained the same. Fig. 5.15 shows the response of the Dorsey voltage with two different regulator settings. In curve 1 the regulator gain is at the lower limit while curve 2 shows the response set to its optimum value for obtaining a fast response. Due to the delays in the electronic filter circuits and in the TCR/TSC-transfer function (see Chapter 3) the SVS has no influence in the initial moments of the DC-blocking. Therefore the peak in the bus voltage is very high and almost at the value of the uncompensated system (which is bigger than 1.5 pu). But then the SVS reacts very fast and pulls the voltage within 30 ms below 1.07 pu. The third curve in Fig. 5.15 represents the bus voltage when both bipoles were blocked. The corresponding curves of the regulator output (HSVS which is approximately proportional to the SVS power output) are compared in Fig. 5.16. In all three cases the SVS is able to compensate completely in its active range and hence the bus voltage can be kept at a value near the prefault value with only a difference caused by the droop (set to 3% over the full compensator range).

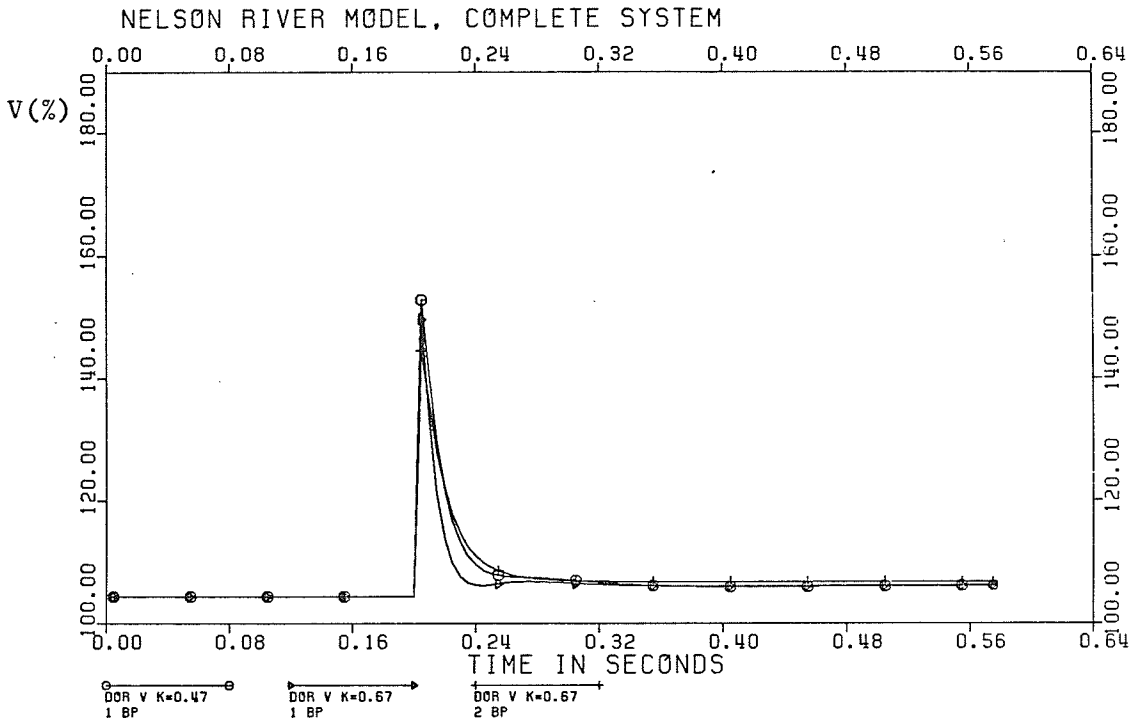


FIG.5.15:SVS ON COMPLETE SYSTEM, BUS VOLTAGE

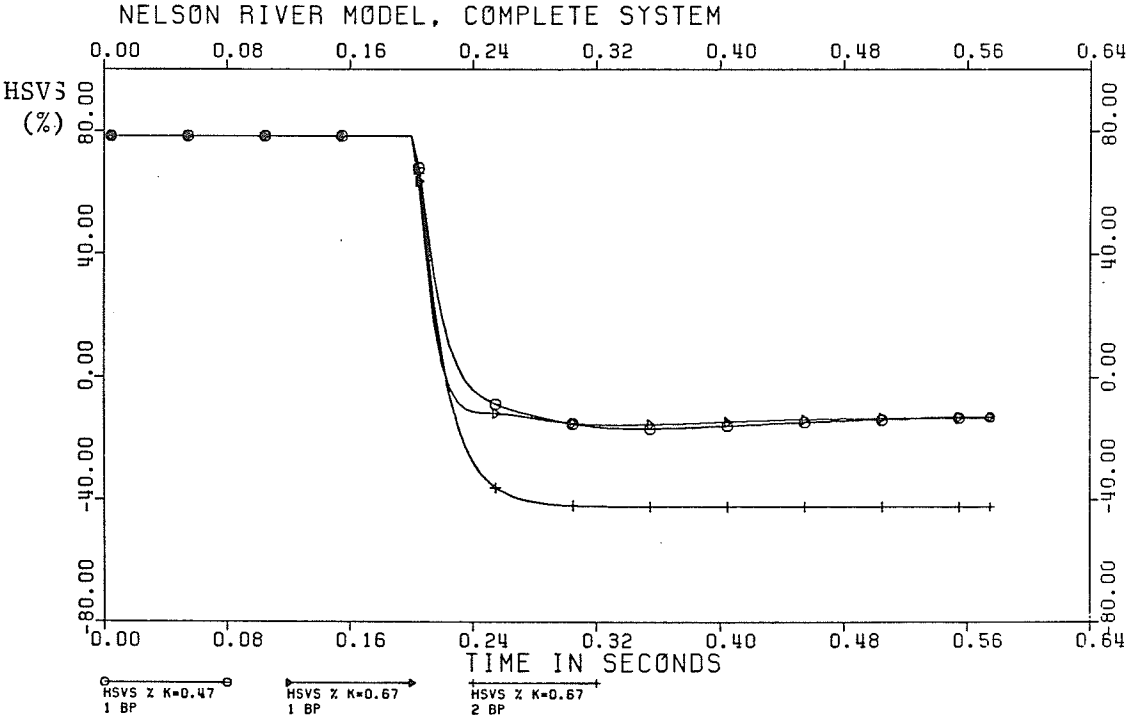


FIG.5.16:SVS ON COMPLETE SYSTEM, REGULATOR OUTPUT

$t-t_F$	5	10	25
$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt$	$6.85 * 10^{-3}$	$11.70 * 10^{-3}$	$16.75 * 10^{-3}$

50	150	ms
$18.10 * 10^{-3}$	$22.6 * 10^{-3}$	pu

Table 5.5: One Bipole Blocked with SVS.

For the test in Fig. 5.17 the SVS regulator was overridden as soon as the voltage reached 1.1 pu and the compensator was forced to its full reactive limit. The purpose of this test was mainly to show a principle of fast control of the SVS. In our special case the voltage is brought down very fast but the bus is then overcompensated. This test series also points out that the SVS could operate with a smaller inductive range, especially in the case of the much more likely blocking of only one bipole.

5.6 Tests with SC and SR Combined

In this and the next section several combinations of synchronous and static compensators are studied. This is of special interest since there are already SC installed in the Nelson River system.

For the following tests groupings of four and two SC have been considered. The balance to the required capacitive power for the inverter terminals have been supplied by fixed capacitor banks while the

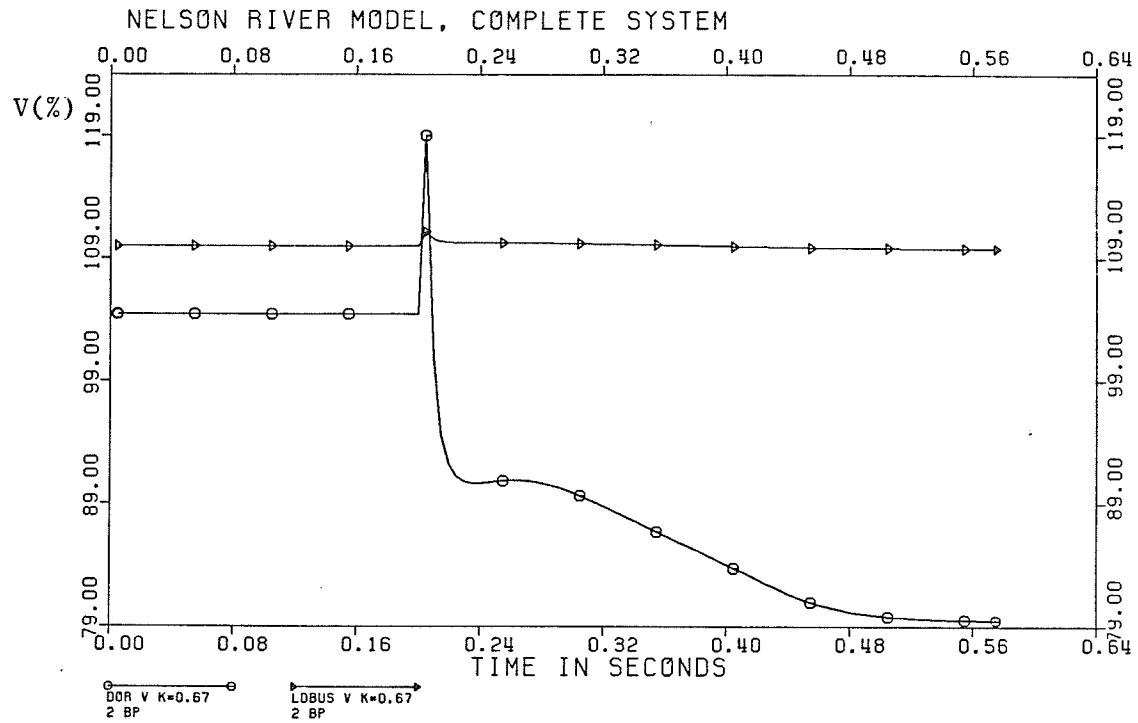


FIG.5.17:SVS ON COMPLETE SYSTEM WITH OVERRIDE

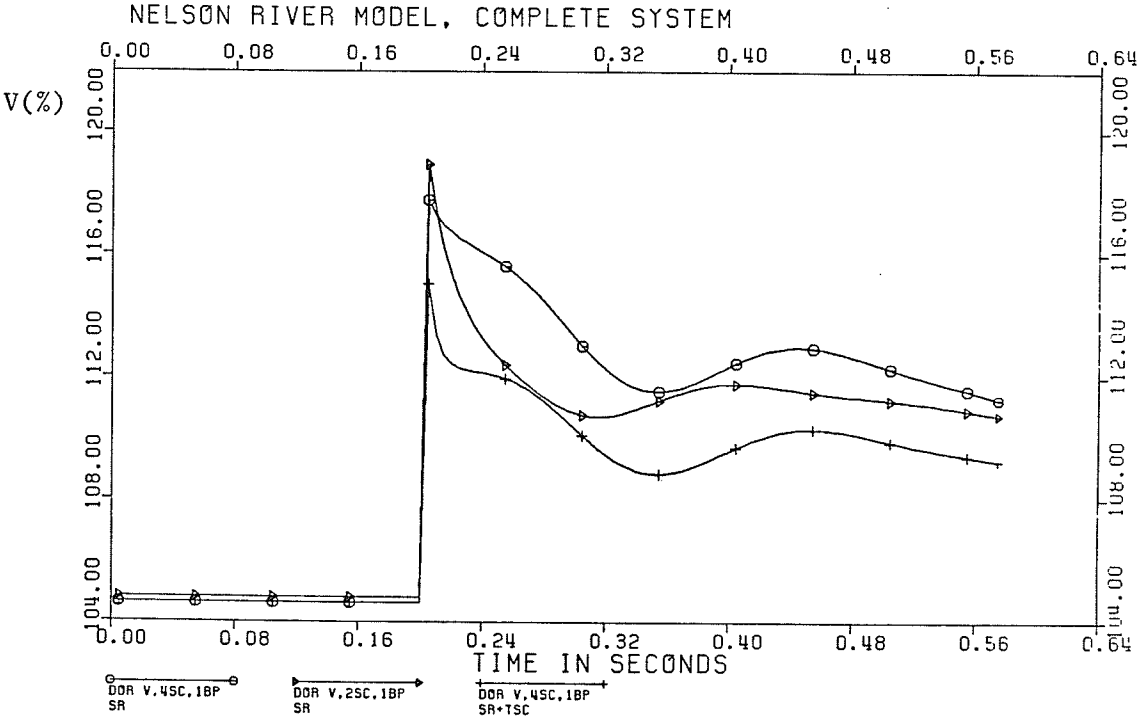


FIG.5.18:SC AND SR ON COMPLETE SYSTEM,BIPOLE 1 BLOCKED

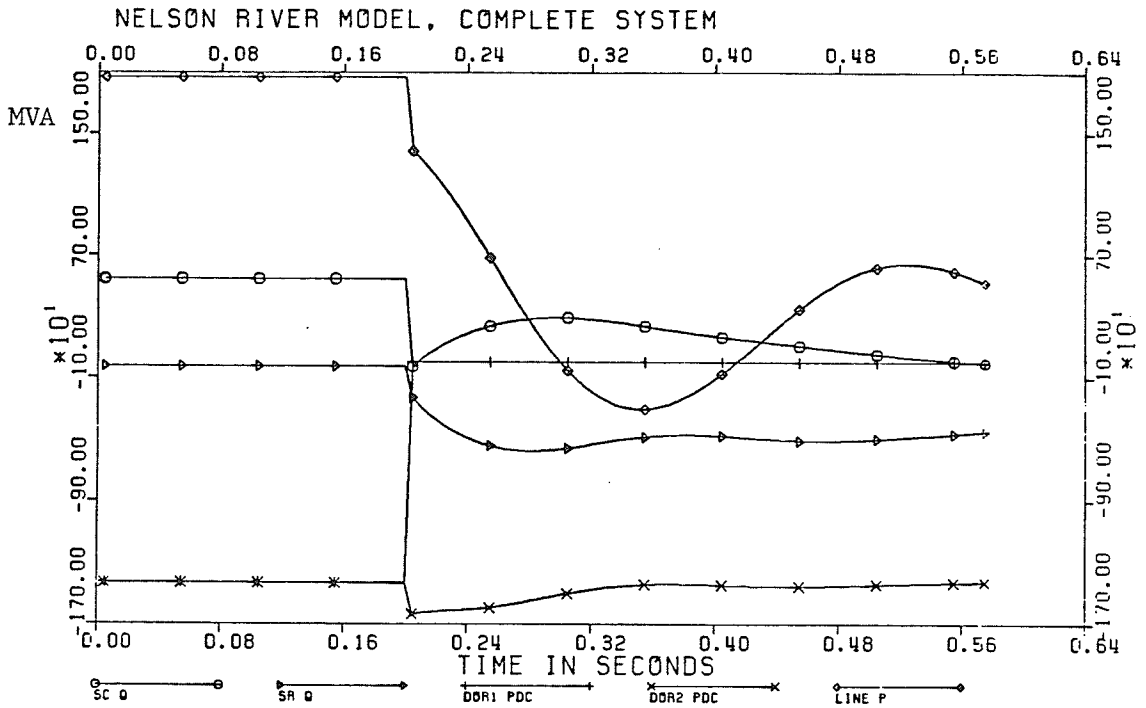


FIG.5.19:4 SC AND SR ON COMPLETE SYSTEM,BIPOLE 1 BLOCKED

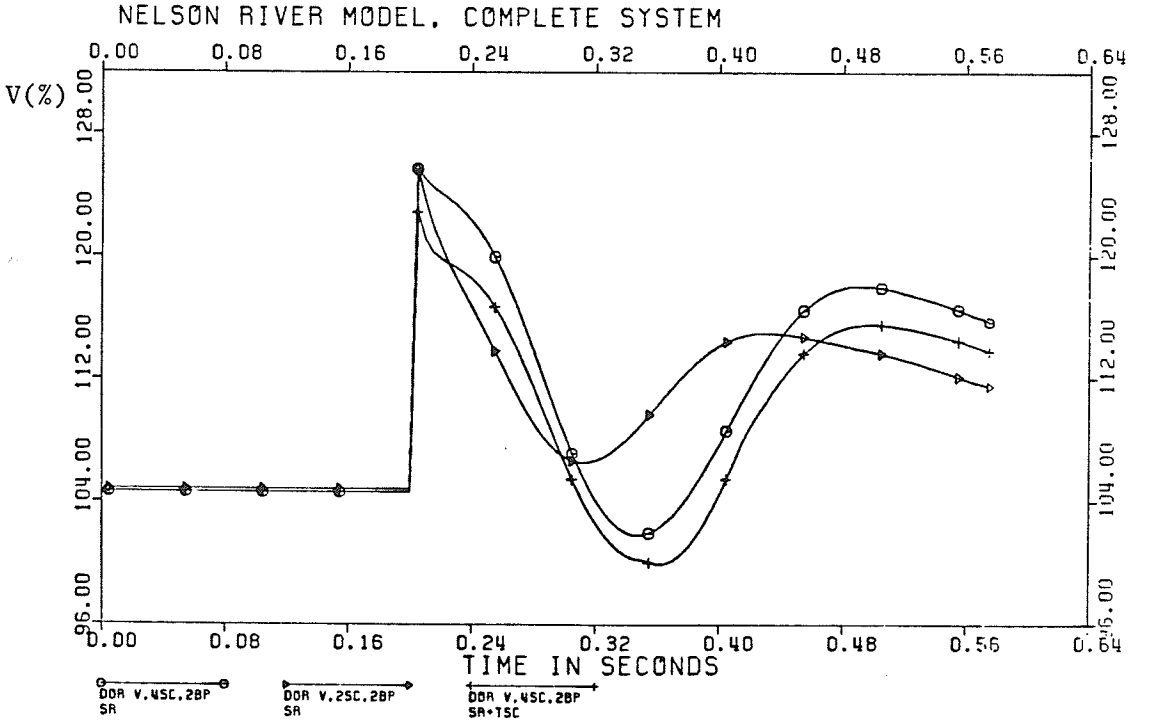


FIG.5.20:SC AND SR ON COMPLETE SYSTEM,2 BIPOLES BLOCKED

SR operated near its neutral point. A summary of the filter and compensator parameters is given in Table 5.6.

Number of SC	Nominal Power of SR (MVar)	Droop of SR based on nom. power	Additional Capacitors (MVar)	Steady-State Power of SR (MVar)
0 (see Chap. 5.4)	480	3%	765	-12.55
2	320	3%	530	-24
4	160	3%	280	-24

Table 5.6: Compensator Parameters in Function of Number of SC

Fig. 5.18 illustrates the effect of the variable numbers of SC. For curve 1 four SC were connected and the behaviour of the voltage is very similar to the case without SR at all (Fig. 5.7), except in the first few milliseconds. The first peak reaches about 1.2 pu but then the voltage can be pulled down by the SR (for SC and SR Q see Fig. 5.19). This effect can be seen even better in the case of 2 SC (curve 2), where the first peak is higher.

In the third curve of Fig. 5.18 with 4 SC again, the additional fixed capacitor banks have been replaced by TSC which results in a lower overall voltage profile. For the case with 4 SC some characteristic power curves (SC, SR and DC systems) are displayed in Fig. 5.19. In Fig. 5.20 finally the same three combinations are shown with both bipoles blocking. The data of the integral W for the case with 4SC and one blocked bipole are given in Table 5.7.

$t-t_F$		5	10	25	50	150	ms
$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt$	4 SC + SR	$1.63 * 10^{-3}$	$3.05 * 10^{-3}$	$7.13 * 10^{-3}$	$13.35 * 10^{-3}$	$32.7 * 10^{-3}$	
	4 SC + SR + TSC	$1.43 * 10^{-3}$	$2.55 * 10^{-3}$	$5.12 * 10^{-3}$	$9.24 * 10^{-3}$	$21.53 * 10^{-3}$	pu

Table 5.7: One Bipole Blocked with 4 SC and SR

5.7 Tests with SC and SVS Combined

The same series of tests as for SR have been performed with SVS combined with synchronous compensators. The results of the various combinations are plotted in Fig. 5.21:

Curve 1 with 4 SC and SVS range from - 160 to 320 MVar

Curve 2 with 4 SC and SVS range from - 320 to 320 MVar

Curve 3 with 2 SC and SVS range from - 320 to 640 MVar

Curve 4 with 4 SC and SVS range from - 160 to 320 MVar with override.

In case 1, 2 and 4 the SVS goes very fast to its reactive limit but with the override in curve 4 the response can even be improved to a certain extent. The first peaks in curve 1 and 2 are of the same magnitude, but with the larger inductive range of the compensator in curve 2 the voltage comes down faster. The effect of both compensators can be seen very nicely in these tests. The fast control of the SVS decreases the over-voltage immediately until the SVS reaches its reactive limit. Then the slow control of the synchronous compensator takes over and the resulting

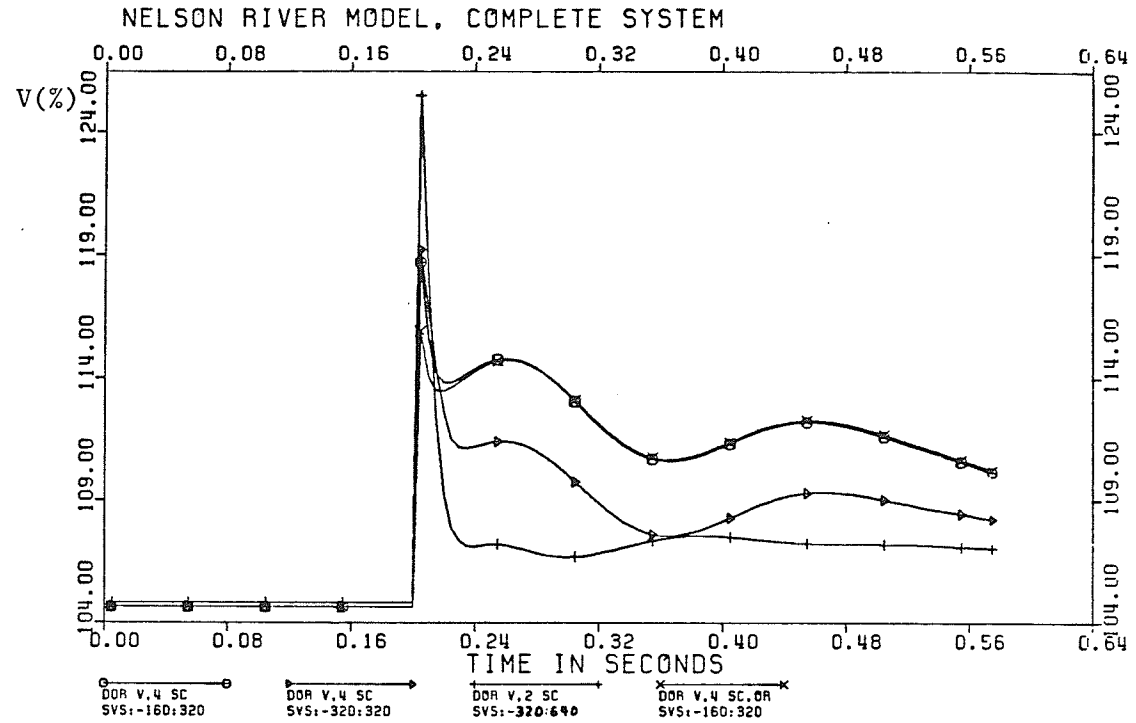


FIG.5.21:SVS WITH SC ON COMPLETE SYSTEM,BIPOLE 1 BLOCKED

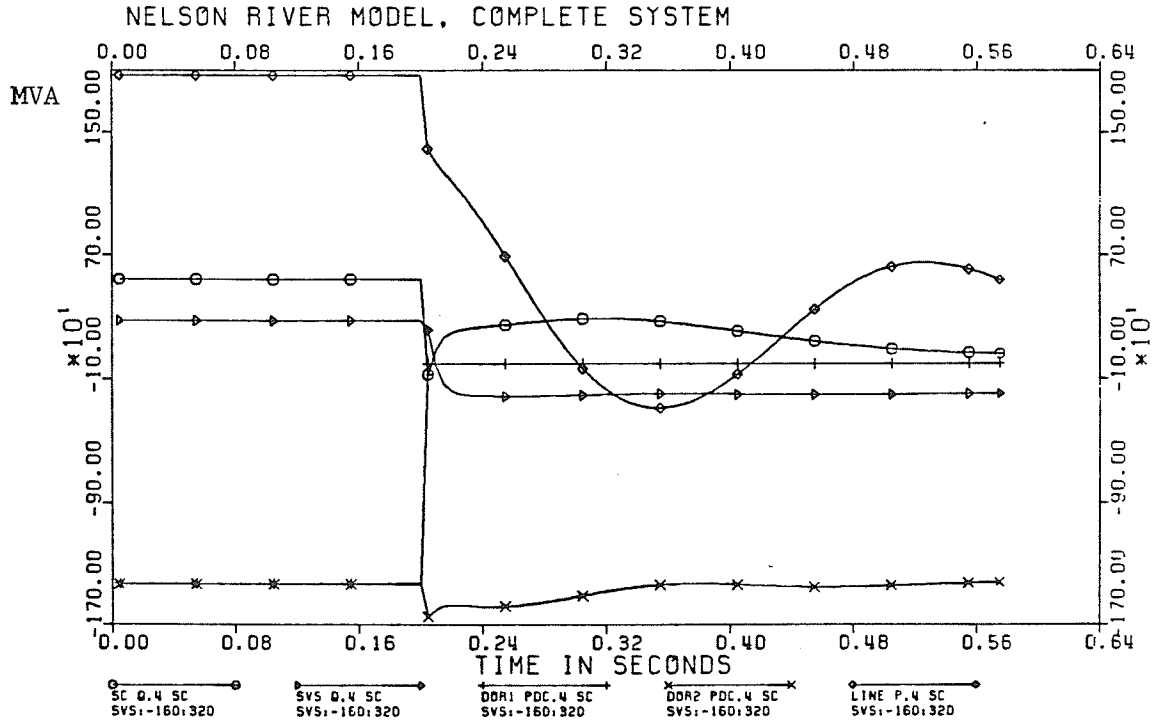


FIG.5.22:SVS WITH SC ON COMPLETE SYSTEM,BIPOLE 1 BLOCKED

shape of the voltage is very similar to the results seen in chapter 5.3 with SC only.

Fig. 5.22 displays the SC an SVS powers of case 1. In Table 5.8 the W integrals for cases 1 and 2 are compared.

$t-t_F$	SVS / $t-t_F$ Range (MVar)	5	10
$W = \int_{t_F}^{t} (V^2 - V_o^2)\, dt$	-160 to 320	$1.72 * 10^{-3}$	$3.15 * 10^{-3}$
	-320 to 320	$1.72 * 10^{-3}$	$3.25 * 10^{-3}$

25	50	150	ms
$6.32 * 10^{-3}$	$11.55 * 10^{-3}$	$30.16 * 10^{-3}$	pu
$6.23 * 10^{-3}$	$9.85 * 10^{-3}$	$21.1 * 10^{-3}$	

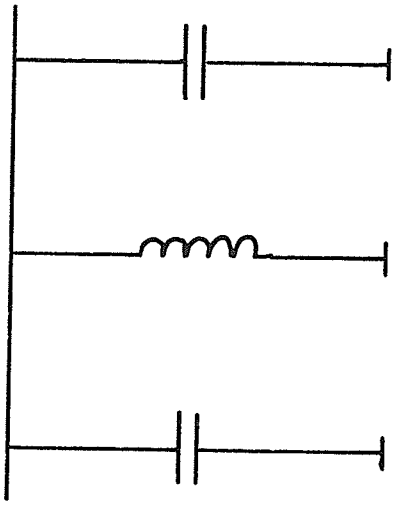
Table 5.8: One Bipole Blocked with 4 SC and SVS

5.8 Small Disturbance Tests

In order to observe the regulator performance of the static compensators, when operated together with synchronous compensators, some tests with small pertubations in the bus voltage at Dorsey have been done. The test series have been held very short because the stability program turned out to be not very suitable for regulator investigations with fast controlled devices.

One possible source of errors is the iteration speed in the program. As already mentioned in Chapter 3 the choice of the load-flow balance interval can affect the response of the compensator.

Another reason is the occurence of low system resonance frequencies above power frequency. For example in the Nelson River model with only static compensation, the receiving system together with the filters and the SVS form a parallel resonance circuit with a resonance around 90 Hz (with SVS 50% capacitive, which is a normal operating point). This is illustrated in Fig. 5.23.



f_{res} = 91 Hz

Fig. 5.23: Resonance Circuit Formed by System and Compensators

Those resonances can affect very heavily the compensator response but they do not show up in the stability program. Because of those problems some results could come out wrong, especially for small disturbances where the regulator action is essential.

In the previous chapter, where only large disturbances have been investigated, the influence is not that big and the results are still representative. Comparative tests with different iteration speed (1 ms

and 0.2 ms) have been done and differences are found to be very small. But the following tests with small disturbances can be used only to illustrate the principal behaviour of the system.

The fault applied in the following tests was a small change in the reactive load at DOR. 200 MVar were rejected and reconnected after 200 ms in order to obtain a voltage change in each direction.

Fig. 5.24 to 5.26 illustrate the compensator reaction to a small fault with only static compensation at DOR, which corresponds to a SVS of the range -480 to +960 MVar. Three different regulator settings are compared and it can be seen that with a value of 0.53 the voltage can be stabilized quite fast (Fig. 5.24), while the response is much slower with a gain of 0.33.

With higher gains the system becomes unstable. The Var output in Fig. 5.25 of the SVS shows some slow drift after the voltage is settled. This could be caused by the action of the HVDC - power controller (see α at Henday in Fig. 5.26). In contrast to this fast action the bus voltage at DOR with only synchronous compensation can be seen in curve 1 of Fig. 5.27. The SC is not able to control the bus voltage, only a reduction of the voltage due to the subtransient effect can be noticed. The case with 4 SC and a SVS of the range -160 to 320 MVar is shown in curve 2 and 3 of the same Figure with one slow and one optimum regulator setting. Even with only a small SVS the voltage at DOR can be controlled very easily.

Fig. 5.28 shows the reactive power supplied by both SC and SVS for curve 3 in the previous Figure, compared with the SC output for synchronous compensation only. It can be seen again, that the SC can not follow the Var-demand of the system.

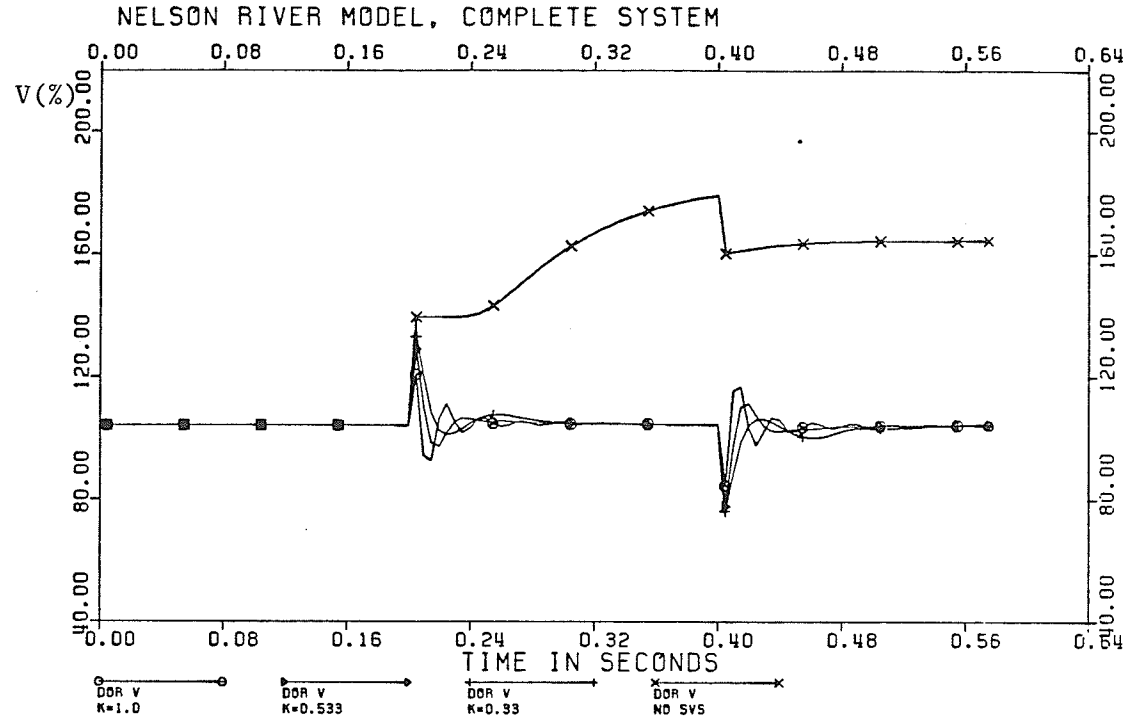


FIG.5.24: SMALL DISTURBANCE AT DOR, SVS ONLY

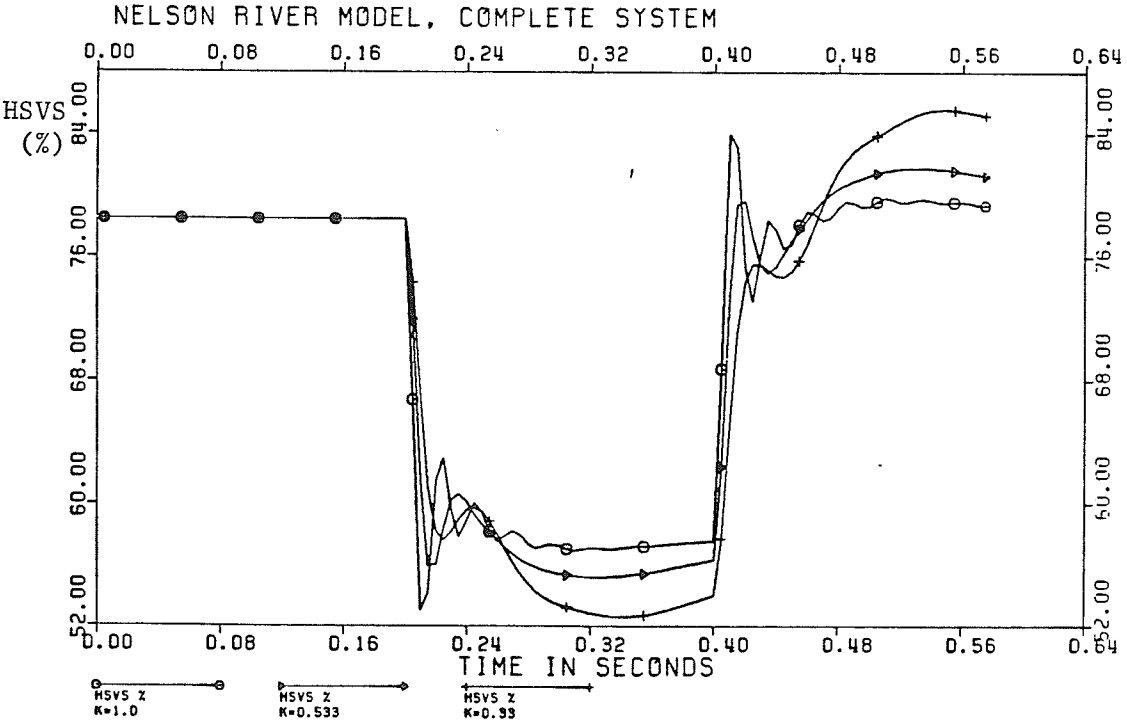


FIG.5.25: SMALL DISTURBANCE AT DOR, SVS ONLY

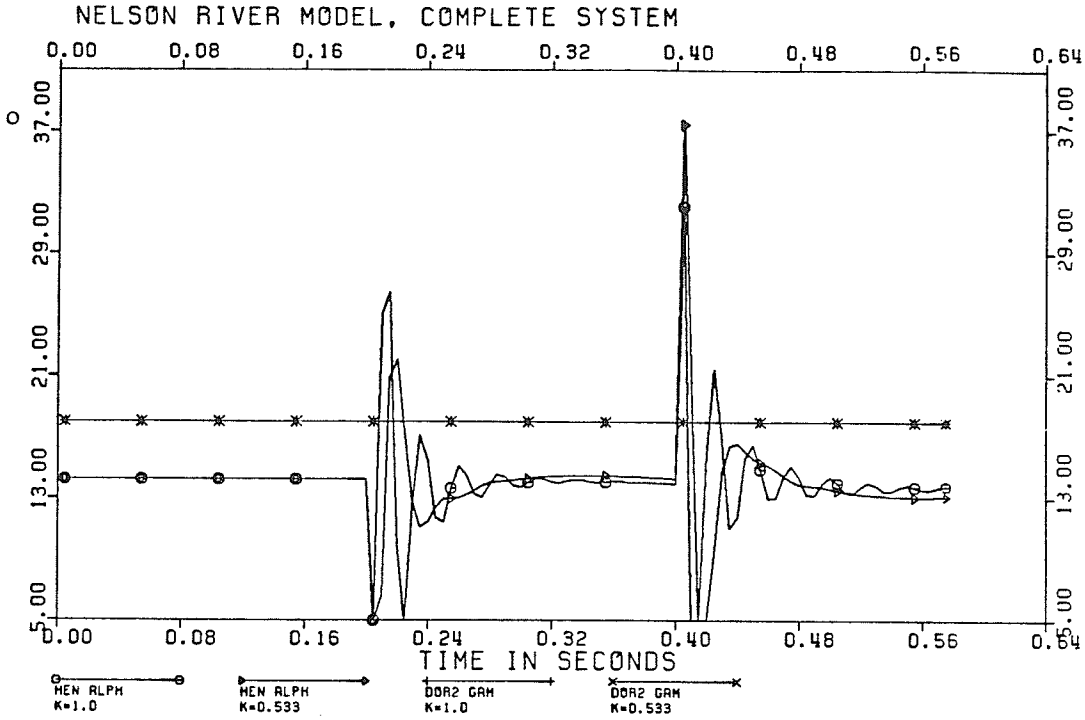


FIG.5.26: SMALL DISTURBANCE AT DOR, SVS ONLY

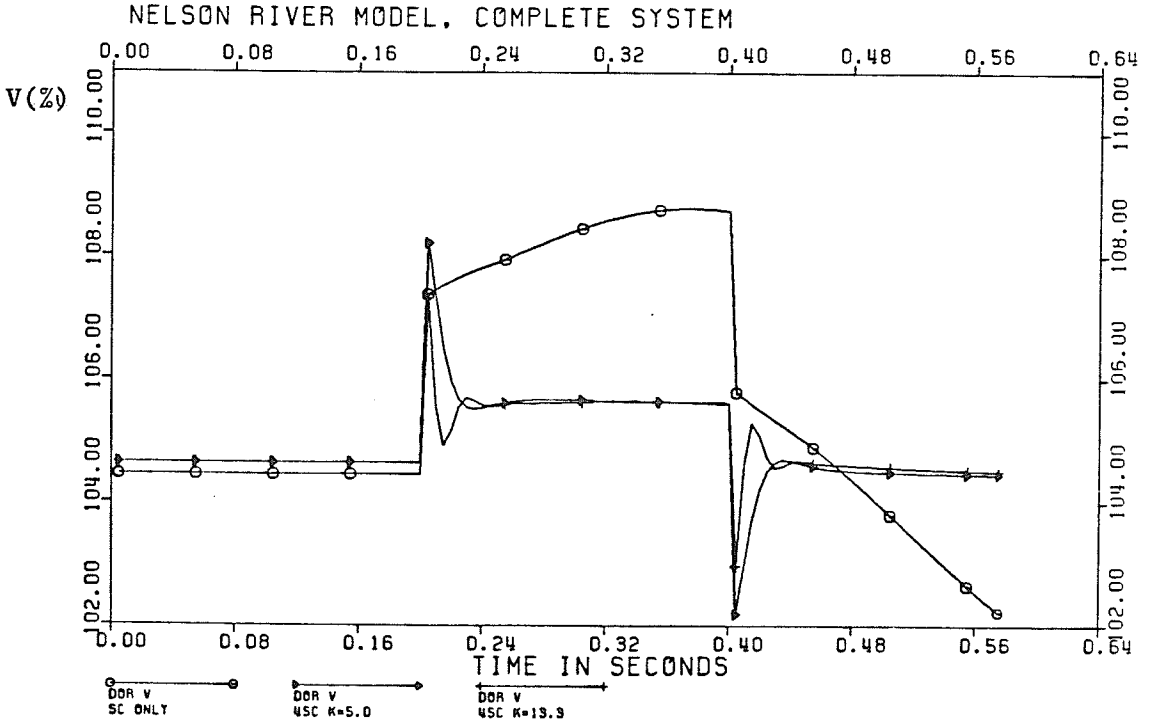


FIG.5.27: SMALL DISTURBANCE AT DOR, SVS AND SC

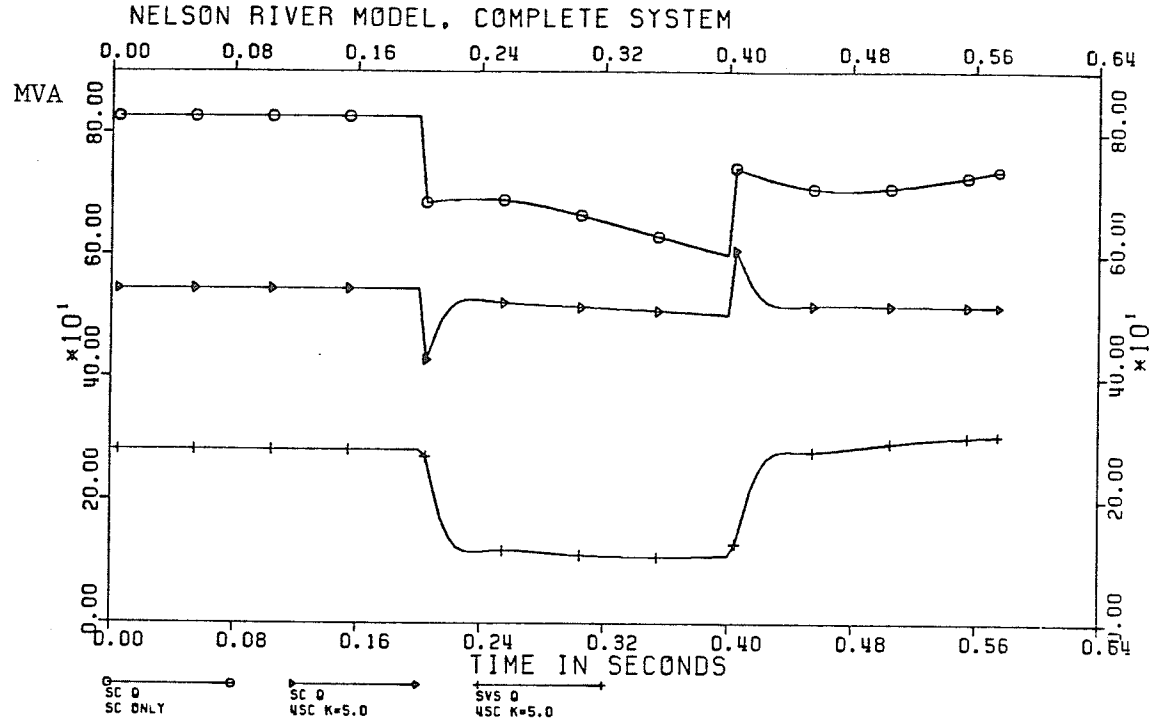


FIG.5.28: SMALL DISTURBANCE AT DOR, SVS AND SC

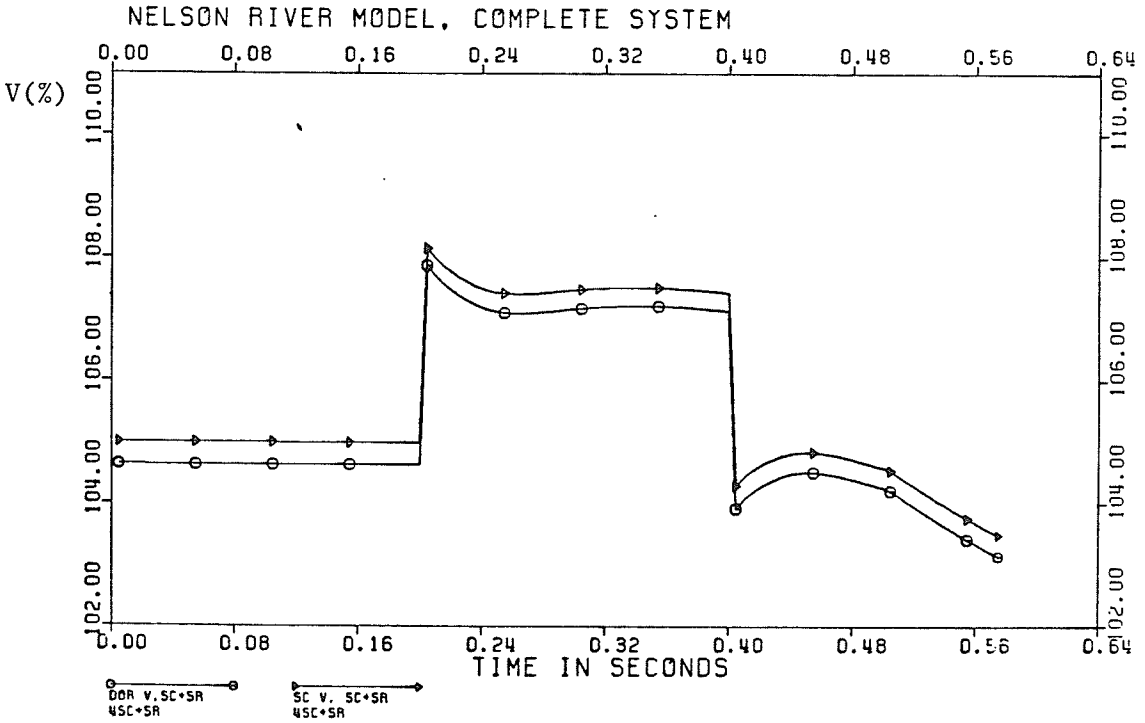


FIG.5.29: SMALL DISTURBANCE AT DOR, SR AND SC

The last case which was investigated was the combination of 4 SC and a saturated reactor with -160 MVar nominal power. The results of this test are shown in Fig. 5.29. Similar to the SVS, the SR shows a good response. The bigger difference between pre- and post-fault value of the voltage at Dorsey (≈2.7% compared to 1% with SC and SVS) is due to the different droop specification of the two static compensators:

SR: Operating range: 0... -160 MVar with 3% Droop

SVS: Operating range: 320... -160 MVar with 3% Droop

→ Droop for SVS on same base is three times smaller. For both compensators the lowest commonly used droops were specified.

Even with this very crude investigation it can be seen easily, that a big improvement in the bus response to small perturbations can be achieved by adding static compensators to the system.

6. DISCUSSION OF THE RESULTS

6.1 Summary

In this chapter the test results which were described in the previous chapter are compared and discussed. A list of the tests to be discussed is given below:

Group 1: Tests with SC on the reduced systems. These are not discussed further, their purpose was to verify the system model and to check the program.

Group 2: Tests with SC on complete system, one and two bipoles blocked.

Group 3: Tests with SR on complete system, combined with fixed capacitors or TSC, one and two bipoles blocked.

Group 4: Tests with SVS on complete system, one and two bipoles blocked. One run was done with regulator override.

Group 5: Tests with SR and SC combined, the main emphasis in the discussion will be laid on the combination with 4 SC. Some runs have been done with TSC.

Group 6: Tests with SVS and SC combined, also here mainly the combination with 4 SC will be discussed further.

Group 7: Tests with various combinations of compensators and small disturbances. These tests are already discussed to a large extent in the previous chapter.

As already mentioned in the previous chapter, the base for our comparison is the interpretation of the dynamic overvoltages caused by the blocking of the DC-system. The criteria used for the comparison are

- maximum voltage at compensator bus (Dorsey)
- voltage shape in the first 150 to 200 ms after fault application

- stress integral W for the first 10 ms and for the first 150 ms after fault.

In the following section the collected results are examined from these three viewpoints.

6.2 Comparison of the Results

6.2.1 Peak Voltage

The peak value of the bus voltage supplies information about the insulation level which is necessary for a certain combination of compensators. In Table 6.1 the maximum overvoltages obtained for each test group are listed.

It should be noted that the values from tests with static compensators are only estimates since the first peaks occur right after the fault application in these cases. Nevertheless they are useful for our comparison as long as they are considered only as reference values.

Test	Chapter	Bipoles Blocked	Maximum Overvoltage in pu	At Time(ms) (Fault-t=0)	Maximum Amount of Absorbed Mvars in first 150ms
SC only (Group 2)	5.3	1 2	1.20 1.28	75 50	106(Min cap.) 700
SR only (Group 3)	5.4	1 2	1.18 1.22	<5 <5	1000 1260
SR and TSC (Group 3)	5.4	1 2	<1.18 <1.22	<5 <5	480 (SR) 685 (SR)
SVS only (Group 4)	5.5	1 2	>1.40 >1.40	<5 <5	170 460
SR and SC (Group 5)	5.6	1 2	1.19 1.26	<5 <5	530(SR) 850(SR)
SR and SC with TSC (Group 5)	5.6	1 2	<1.19 <1.26	<5 <5	280(SR) 620(SR)
SVS and SC (Group 6)	5.7	1 2	1.21 1.30	<5 <5	210(SVS) 250(SVS)

Table 6.1.: Maximum Overvoltages for Each Test Group

The highest peak was obtained with only SVS connected to the Dorsey bus. This is so, because the SVS does not react in the first moment, its effect can be seen only after a few milliseconds due to the time constants in the control system.

The lowest overvoltages could be seen with saturated reactors since they are very fast in reaction, the overvoltage is cut off by the saturation slope of the reactor which is 15% in the first few milliseconds. All combinations of synchronous and static compensators result in more or less the same magnitude in voltage.

With only synchronous compensation the peak voltage is reached at 50 to 75 msec after the fault, while the peak occurs immediately after fault if there is any static compensator in service in parallel to the SC.

A look at the maximum reactive power absorption after the fault shows that the SR can absorb much more MVars than the SVS. But the value of 250 MVars for an SVS designed for 160 MVar at 1 pu voltage does not raise much problems for its design.

6.2.2 Waveform of the Bus Voltage

The waveform is discussed to obtain some general statements about the system and compensator behaviour. Also some qualitative ideas about the stresses in equipment can be found.

In Fig. 6.1 the resulting bus voltages of four cases are compared. In each case only one bipole was blocked and only one type of compensator has been used.

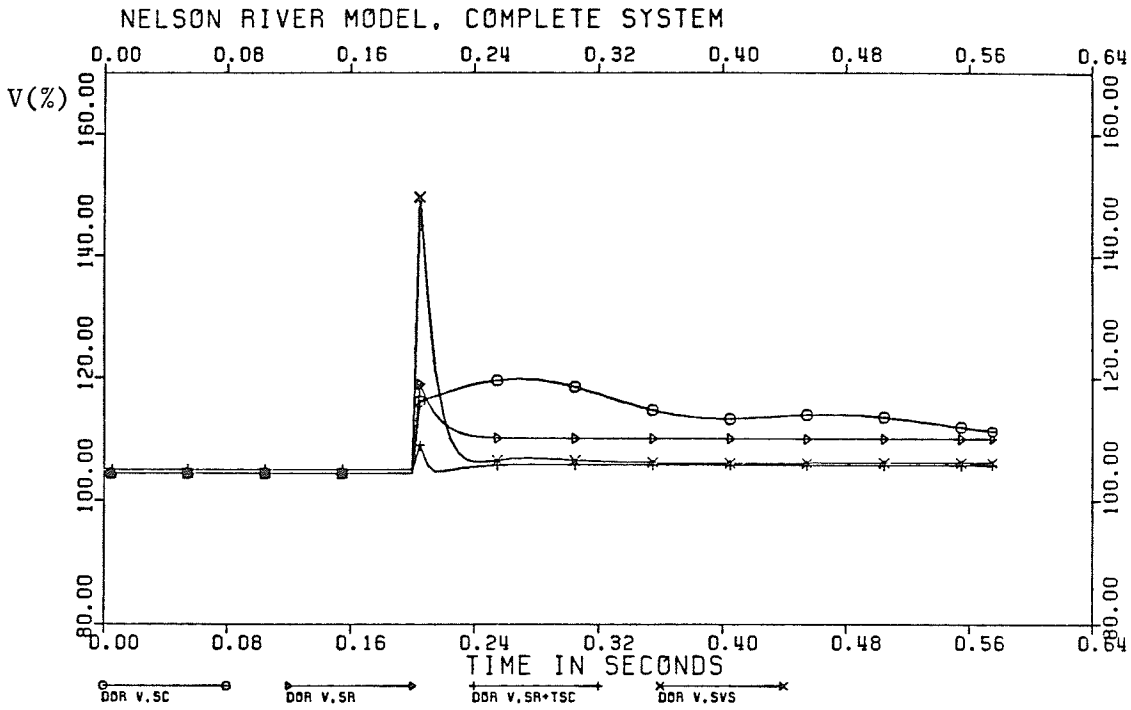


FIG.6.1:COMPARISON OF COMPENSATOR RESPONSE,1BIPOLE BLOCKED

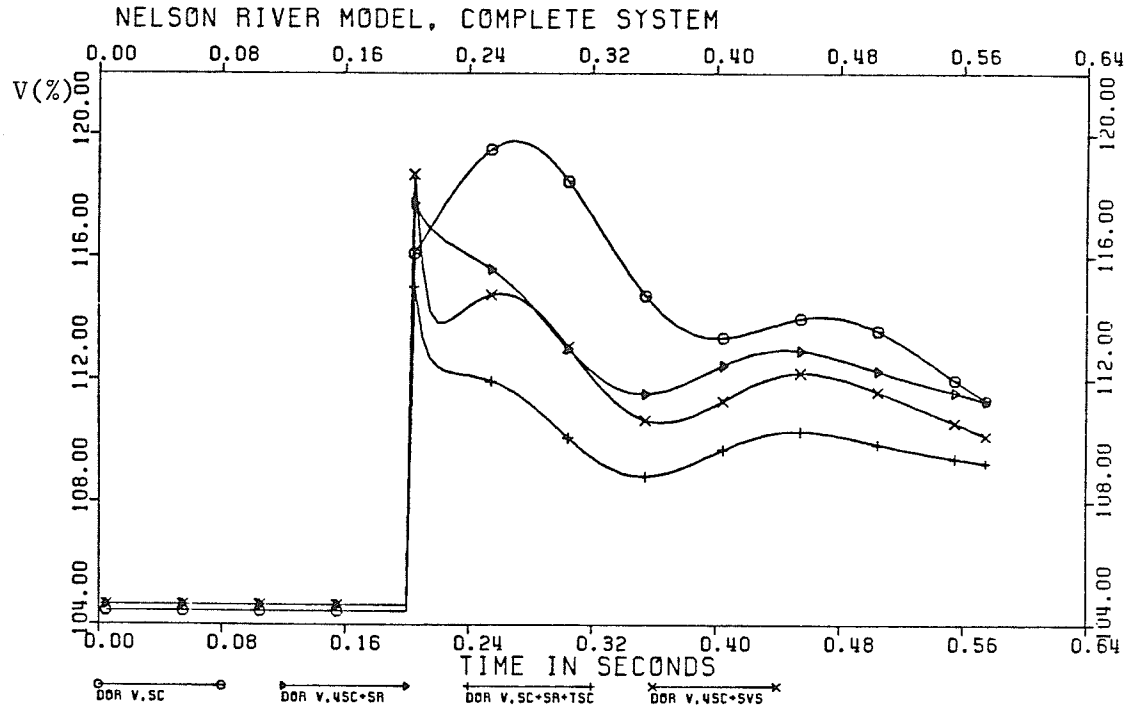


FIG.6.2:COMPARISON OF COMPENSATOR RESPONSE,1 BIPOLE BLOCKED

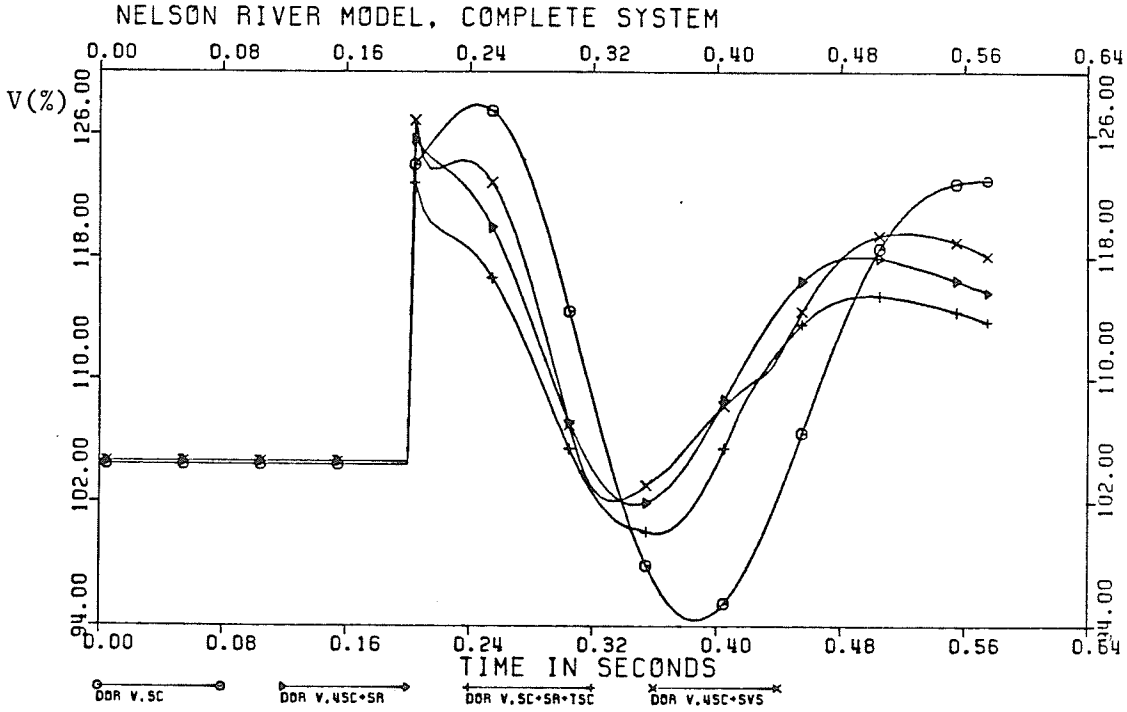


FIG.6.3:COMPARISON OF COMPENSATOR RESPONSE,2 BIPOLES BLOCKED

Curve 1 shows the case with 6 SC at Dorsey. As already mentioned in the last chapter, the voltage rises immediately to 1.16 pu while the maximum overvoltage is then built up with a much slower speed. The reason for this is a low frequency oscillation of the machines and the slow exciter control. In opposition to this, all types of static compensators (Curve 2: SR, Curve 3: SR with TSC, Curve 4: SVS) produce the highest voltage peak in the beginning. Then they reduce the voltage very rapidly (within 20 to 30 ms) to a stable value. This type of overvoltage is much less dangerous for the system. It can be handled easily by surge arresters (see also next section).

Moreover, the fast action of the static compensators can stabilize the system after the fault, something which is not possible with the synchronous compensators. Fig. 6.2 and Fig. 6.3 show the bus voltage at Dorsey with the various combinations of SC and SR or SVS. In Fig. 6.2 only bipole 1 was blocked while Fig. 6.3 displays the same combinations with two blocked bipoles. The best results were obtained in both cases with the combination of SC, SR and TSC, closely followed by the other configurations with static compensators.

It can be seen from both figures, that with the combination of synchronous and static compensators both the high peaks of the SR and SVS and the sustained overvoltage of the SC can be reduced. Also the contribution of each compensator type is illustrated nicely in these graphs. For the two last figures the arrangement of compensators was chosen as 4 SC plus static compensator. This configuration represents most closely a possible future situation at the Dorsey terminals.

In the next section a more quantitative comparison of the various waveshapes is given.

6.2.3 Energy Content in Overvoltage

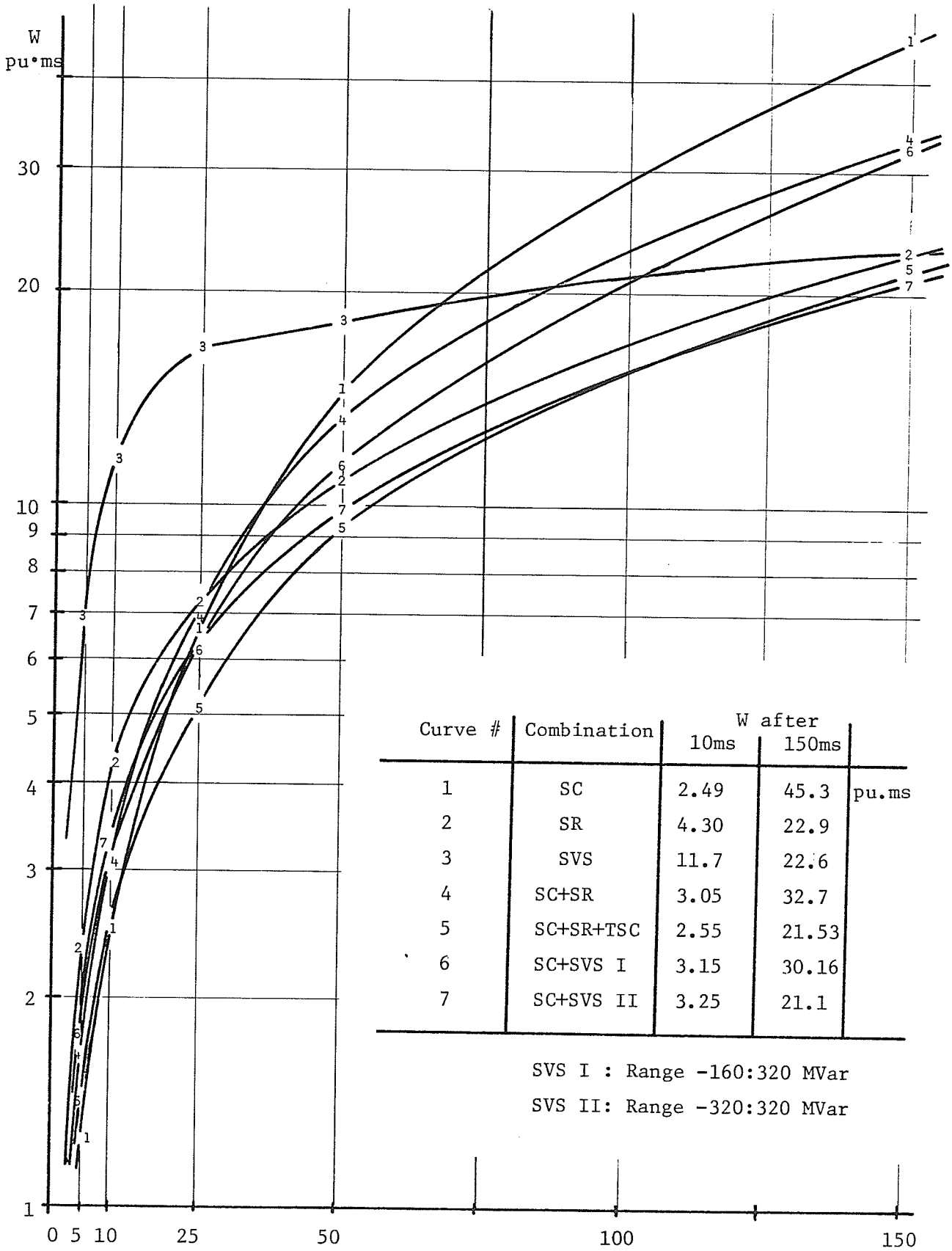
In Chapter 5 the stress integral

$$W = \int_{t_F}^{t} \left(V^2 - V_o^2\right) dt$$

was introduced to determine a numerical value which is related to the energy a surge arrester would have to absorb at the compensator bus. According to the different waveshapes discussed in the previous section it seemed reasonable to compare the values of W on the one hand very shortly after the fault (10 to 25 ms), on the other hand the value after 100 to 150 ms should be characteristic for the overvoltages of longer duration.

In Fig. 6.4 the values of W for various configurations are recorded. The values are taken from Chapter 5. For all cases only one bipole was blocked.

The curves illustrate well that in spite of the very high voltage peak at the beginning, the SR (curve (2)) or the SVS (3) can handle the overvoltage better than the synchronous compensator (1). The SC with its long lasting voltage swing creates much more difficulties if surge arresters should be used for absorbing the surplus of energy. A good compromise for the Nelson River system seems to be the combination of SC and static compensators. For example curves (4a) with SC, SR and TSC or (5a) with SC and SVS (range -320 to 320 MVar) seem to be reasonable not only for low peaks at the beginning but also for reduced overvoltages some time after the disturbance.



Curve #	Combination	W after 10ms	W after 150ms	
1	SC	2.49	45.3	pu.ms
2	SR	4.30	22.9	
3	SVS	11.7	22.6	
4	SC+SR	3.05	32.7	
5	SC+SR+TSC	2.55	21.53	
6	SC+SVS I	3.15	30.16	
7	SC+SVS II	3.25	21.1	

SVS I : Range -160:320 MVar

SVS II: Range -320:320 MVar

Fig. 6.4: Integral W for Various Compensator Combinations

6.3 Conclusions

Summarizing the results from this chapter it can be said that from the point of view of dynamic overvoltages the application of only synchronous compensators at an HVDC terminal is not the optimum choice. Although the use of static compensators decreases the short circuit ratio of the system, the grade of stability with saturated reactors as well as with SVS is much higher than with SC. SC are slow during transients and even with their ability to increase the SCR of a system they can not reduce overvoltages as well as static compensators do. This impression is even enhanced with the consideration of the handling of small disturbances by compensators as already discussed in Chapter 5.8. During small disturbances SC show practically no regulating effect, on the contrary they start oscillating with low frequency and have to be damped.

Even for a system like the Nelson River scheme, where additional compensators have to be combined with existing SC, static compensators can bring strong improvements in the system behaviour. It seems that a combination of 2/3 synchronous compensators and 1/3 static is a very effective way to handle overvoltages, although there still remains the need of damping the SC's.

7. CONCLUSIONS

7.1 Test Results

The study described in this thesis covered one aspect of implementing static Var sources into an HVDC-system. Dynamic overvoltages caused by blocking partially or completely the transmitted DC power were investigated with different reactive power compenstors at the inverter terminal as parameter. The obtained results appeared to be in favour of static compensators or of combinations between synchronous and static Var sources.

With reference to the Nelson River HVDC-system the most effective way to increase the reactive power capacity at Dorsey in the near future is to add static compensators of the SR or the SVS type to the existing synchronous compensators. Both SR and SVS create much lower operation and maintenance costs as compared to SC, and both can improve the DOV profile at the inverter bus.

The static compensator with TCR and TSC is more flexible in operation than the SR. Although the SR can be highly overloaded during system transients, the maximum overvoltages occurring in the Nelson River system can easily be handled by SVS. The best results were obtained by combining SR with TSC. Although this configuration seemed to be the most effective, it is much more complex than a corresponding SVS arrangement and could be therefore more expensive.

It was mentioned several times in this report that some uncertainties in the obtained results remained due to limitations from the side of the stability program.

Fast transients could not be studied with this program and therefore the response times obtained with the fast acting static compensators

might not be used as reference, yet the principal behaviour of the tested devices is certainly close to reality and the results are considered reliable.

7.2 Suggestions for Further Investigations

The study described above was limited to dynamic overvoltages caused by blocking of the HVDC-system. This is only one aspect of the problem in a complex combination of HVDC-terminal and static compensation.

Possible further investigations which are of importance for the evaluation of Var compensators can be split into three areas, although they are closely related to each other:

1) New criteria for evaluation

Besides dynamic overvoltages the optimum compensator response and the fast system stabilization after fault as well as transients and valve stresses are possible criteria. But specially the latter group of tests can not be done with this stability program.

2) New disturbances and changing system parameters

In our study various compensator configurations were compared under the same system and fault conditions. A further extension of the work is the observation of the performance of some optimized compensator arrangement under all possible system configurations and fault cases. This is of great importance since the regulator performance of a compensator is highly dependent on parameters like short circuit ratio or resonances in the connected system.

3) New test tools

Since the present load-flow and stability program is used to its limits from the point of view time scale, further investigations should be done with other programs like EMTDC or EMTP or on a physical real-time simulator. This is necessary mainly because the program used works with phasors and no statements can be made about waveforms of voltages and currents or about fast transients in the moment of a fault. Besides that power frequency is assumed during all disturbances and the influence of system resonances or frequency or phase changes can not be considered. Furthermore it is not possible to study a system under unbalanced conditions with this program.

APPENDIX A: REFERENCE LIST

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1.4 G.W. Stagg, A.H. El-Abiad — Computer Methods in Power System Analysis, McGraw-Hill 1968.

1.5 G.W. Swift — Power Systems Control, Lecture Notes, University of Manitoba, 1981.

2. Nelson River HVDC-System

2.1 C.V. Thio — Nelson River HVDC Bipole-Two, Part 1 - System Aspects, IEEE PAS-98, No. 1, 1979.

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2.3 D.A. Woodford — The Application of Controlled Reactive Compensation for Single Pole Switching on long EHV Line Sections, IREC/EPRI Symposium, Montreal 1979.

3. Var Compensation in AC-DC Systems

3.1 M. Sakai, et al. — Overvoltage and Var Compensation Studies on Hokkaido-Honshu HVDC Linkage, Overvoltage Conference, Winnipeg 1980.

3.2 C.A.O. Pexioto, et al. — Simulator and Digital Studies on Var Compensation for the Itaipu HVDC Transmission System, Overvoltage Conference, Winnipeg, 1980.

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3.4	Cigré Study Committee 14, Working Group 03	Use of Static or Synchronous Compensators in HVDC-Systems (preliminary report 1981).
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4. Simulation

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5. HVDC Systems in General, AC-DC Interactions

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5.2	J.P. Bowles	Alternative Techniques and Optimization of Voltage and Reactive Power Control at Converter Stations, Overvoltage Conference, Winnipeg 1980.
5.3	J.P. Bowles	Overvoltages in HVDC Transmission Systems Caused by Transformer Magnetizing Inrush Currents, IEEE PAS-93, 1974, pp. 487-493.

6. Static Var Compensators

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6.2	G. Romegialli H. Beeler	Problems and Concepts of Static Compensator Control, IEE-Proceedings, Volume 128, Part C, No. 6, 1981.

6.3	H.L. Thanawala et al.	Static Compensators Using Thyristor Control with Saturated Reactors and with Low Reactance Linear Reactors, IEE Conference Publication 205, England, 1981.
6.4	Ch. Tuttas	Thyristor Controlled Saturated Reactor - A New Design of Static Var-Systems, IEE Conference Publication 205, England, 1981.
6.5	Cigré Working Group 31.01	Modelling of Static Shunt Var Systems (SVS's) for System Analysis (Draft, 1976).

APPENDIX B: SYSTEM DATA

A collection of the data used for the modelling of the Nelson River System is given in this paragraph. For a description of the generator and of the HVDC controller models please refer to the user manual for the stability program (Reference [4.3].

The following data are put together below:

.Nelson River System configuration

.230 KV Collector System with Kettle, Longspruce and Limestone generation stations.

.Machine, Exciter and Governor data for generators.

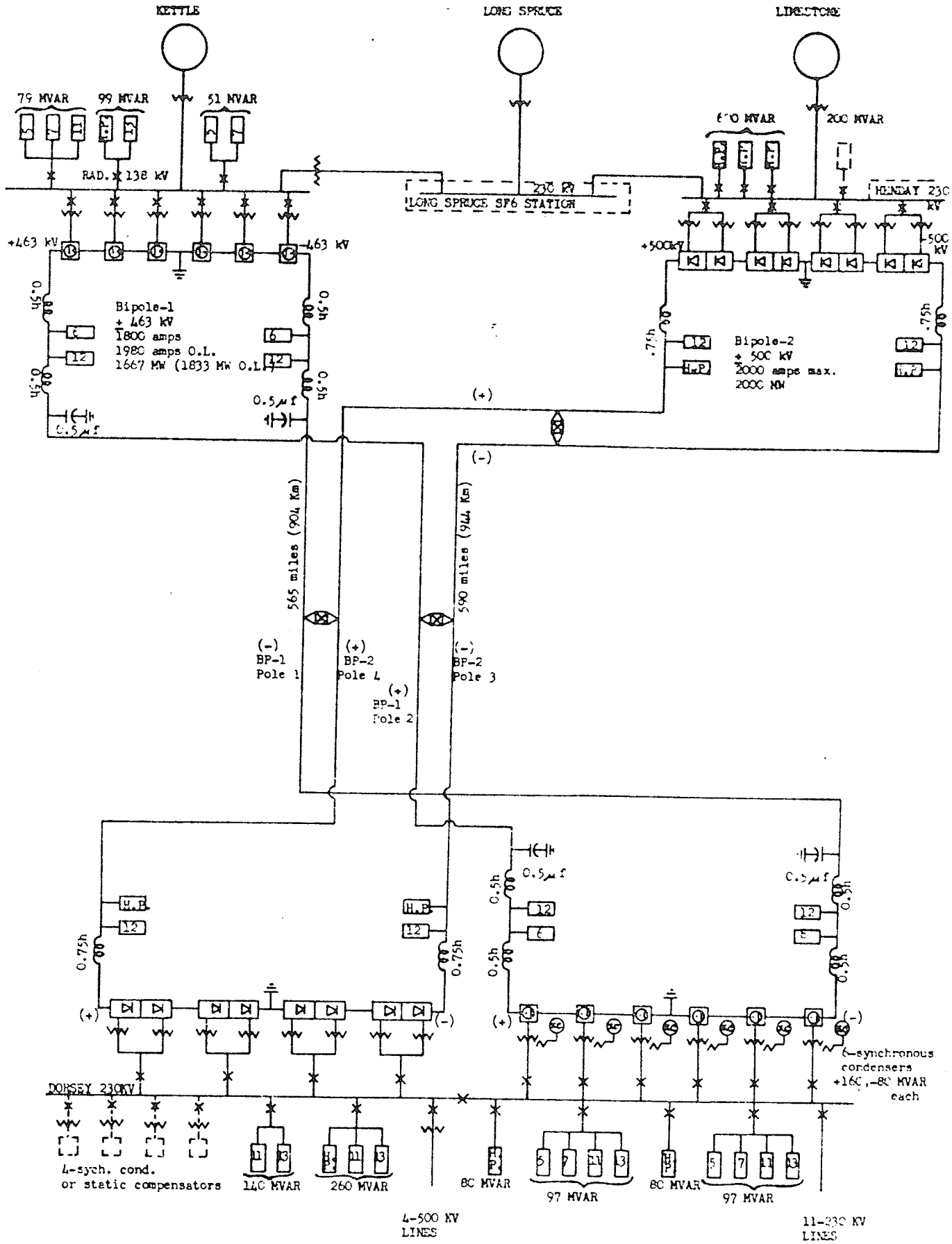
.Machine parameters for synchronous compensators at Dorsey.

.DC-system data:

- Converter yransformers
- DC-Terminals
- DC-Lines

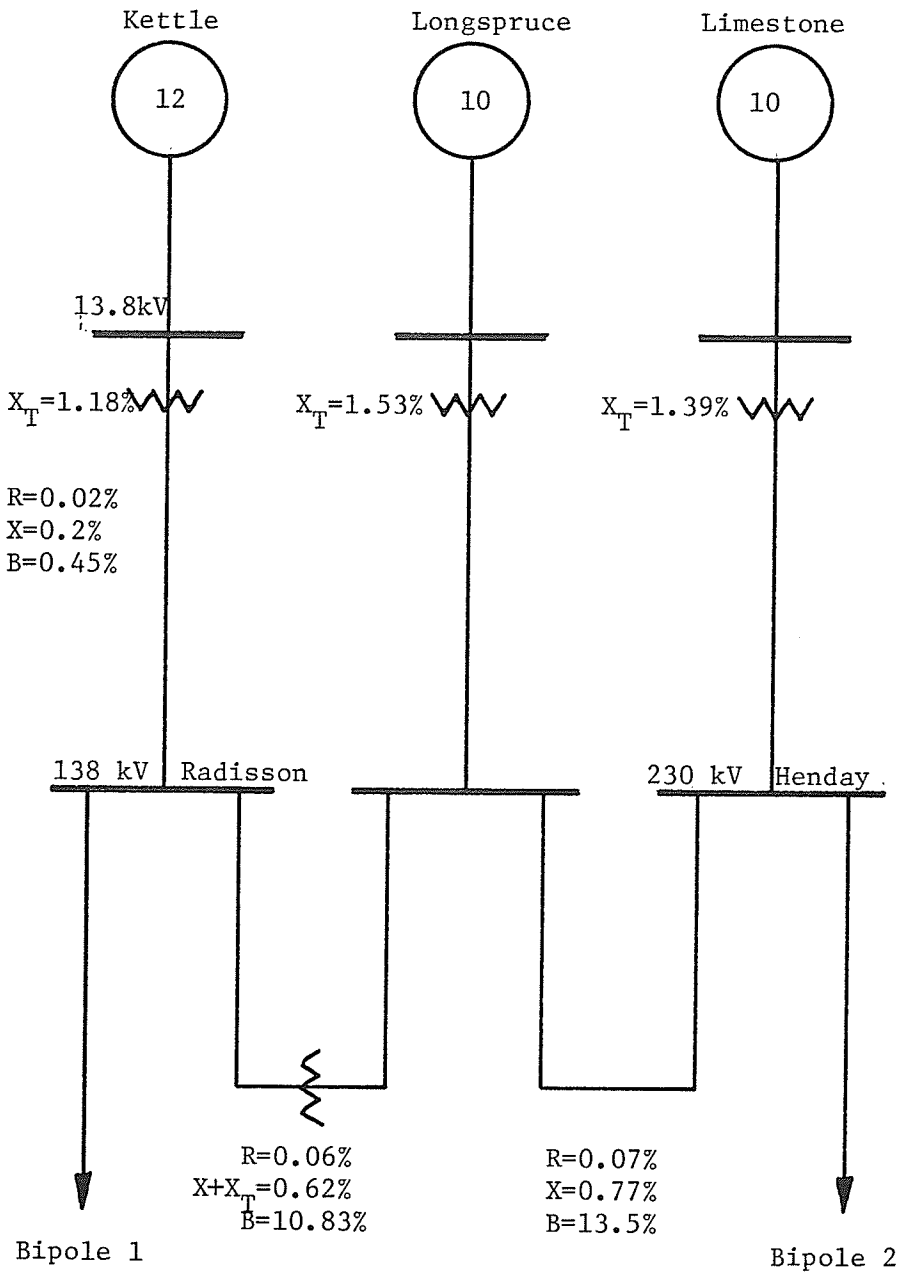
.DC-controller data.

.Sample of input data (for case with SC only)



1. Nelson River System Configuration

   (From Reference [2.1])



Assumption for Transformer Impedances: 15% on own Base
All Values Based on 100 MVA

2. Collector System with Kettle,Longspruce and Limestone Generating Stations

3. Machine Data for Generators

All data given below are the equivalent for the total number of machines at each bus. The values are based on 100 MVA.

Parameter	Kettle	Longspruce	Limestone	
Number of Machines	12	10	10	
X_d	7.68	6.2	6.2	%
X_q	4.47	4.3	4.3	%
X'_d	2.08	2.35	2.35	%
X''_d	1.62	1.56	1.56	%
X''_q	1.68	1.56	1.56	%
H	49.25	39.57	39.57	$\frac{\text{MWs}}{\text{100MVA}}$
X_L	1.18	1.2	1.2	%
T'_{do}	4.1	6.6	6.6	s
T''_{do}	0.019	0.03	0.03	s
T''_{qo}	0.048	0.03	0.03	s
A_g	0.0243	0.0231	0.0231	
B_g	7.57	6.79	6.79	

4. Exciter Data

Parameters	Kettle	Longspruce	Limestone
K_A	289	169	169
T_A	0.099 s	0.05 s	0.05 s
K_E	1.0	1.0	1.0
T_E	0	1.0 s	1.0 s
μ_s	0.0134	0	0
T_{SE}	1.43 s	0	0
$V_{A\ Max}$	5.0 pu	5.0 pu	5.0 pu
$V_{A\ Min}$	-3.5 pu	-3.5 pu	-3.5 pu

5. Governor and Turbine Model

	Kettle	Longspruce/ Limestone
1/FR	0.461	0.75
T_{max}	1224.0 MW	977.5 MW
T_3	0	999
T_4	0.394 s	0.753 s
D	4.08	14.0
T_s	8.16 s	1.0 s
T_c	0	999.0 s
T_5	-0.9 s	-0.48 s
C_1	4.55	4.5
C_2	0.266	1.0
C_3	0.04	0.04
C_4	0.39	0.2
C_6	0.4	0.32

6. Synchronous Compensators at Dorsey

Machine Data

All reactances in %, based on 100 MVA. Time constants in seconds. Calculation based on assumption of 50% ASEA and 50% English Electric machines.

Parameters		Number of Units				
		1	2	4	6	8
X_d	%	99.31	49.66	24.83	16.46	12.41
X_q	%	65.53	32.77	16.38	10.9	8.19
X'_d	%	19.72	9.86	4.93	3.28	2.47
X''_d	%	10.91	5.46	2.73	1.8	1.36
X''_q	%	14.72	7.36	3.68	2.45	1.84
H	%	2.72	5.44	10.88	16.33	21.76
X_o	%	7.66	3.83	1.92	1.27	0.96
T'_{do}	%	10.25	10.25	10.25	10.25	10.25
T''_{do}	%	0.11	0.11	0.11	0.11	0.11
T''_{qo}	%	0.32	0.32	0.32	0.32	0.32

Exciter Data

$K_A = 150$ $K_E = 1.0$ $\mu_s = 0.006$ $V_{R\ max} = 6.0$ pu

$T_A = 0.08$ s $T_E = 0$ $T_{SE} = 0.5$ s $V_{R\ min} = 6.0$ pu

7. DC-System Data

a) Converter Transformer Data: Commutating Reactances

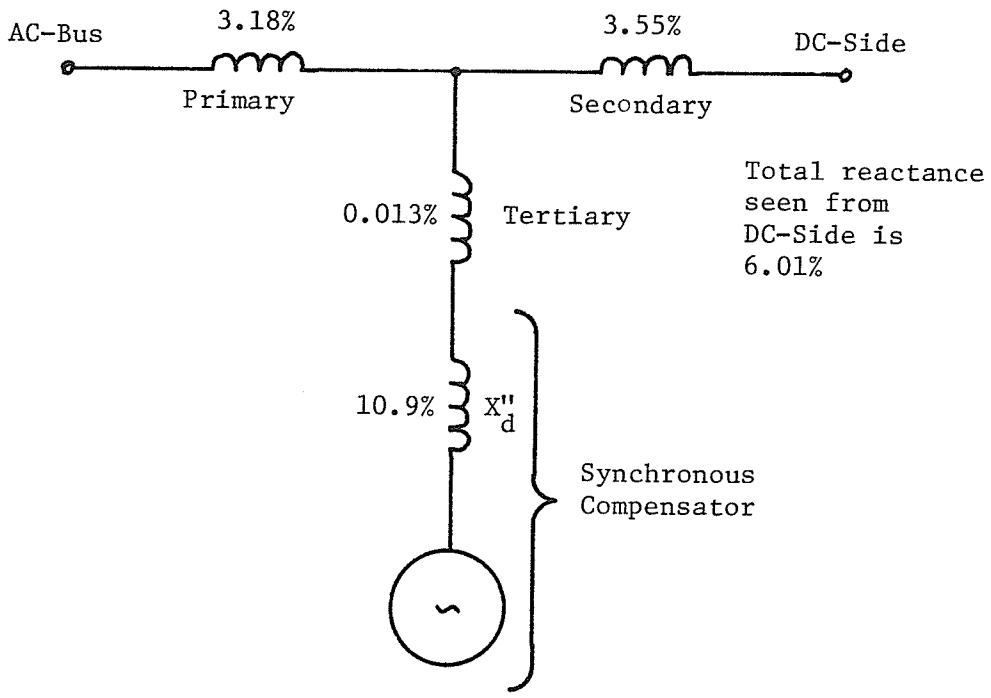
(All Reactances on 100 MVA Base)

Bipole 1 (2 x 3 Bridges)

Radisson: 6.24% per Bridge ≙ 2.08% for 2 Bridge Model

Dorsey: 6.05% per Bridge ≙ 2.02% for 2 Bridge Model

Three winding transformer at Dorsey:



Bipole 2 (2 x 4 Bridges)

Henday: 8.00% per Bridge ≙ 2.00% for 2 Bridge Model

Dorsey: 8.39% per Bridge ≙ 2.10% for 2 Bridge Model

b) AC Secondary Base Voltages of Converter Transformers

	Bipole 1		Bipole 2	
	Rad.	Dor.	Hen.	Dor.
V_B(kV)	402.0	381.0	448.0	424.0
Tap changer ranges				
Min	93%	93%	95.3%	95.3%
Max	120%	128%	131.6%	131.6%
Steps	19	19	27	27

c) DC Voltages and Firing Angles at Converter Terminals

Base Voltage on DC-side: 463kV

Terminal	DC-Voltage	α range under normal conditions
Radisson	463 kV	12°...14°
Henday	500 kV	16°...19°

At inverter terminals $\gamma = \gamma$ min = 18°

d) DC-Lines

Bipole 1: R = 26.78 Ω per pole

Bipole 2: R = 29.06 Ω per pole

8. DC Controller Data

Filter:	$T_F = 0.1$ s
Telecom delay:	$T_t = 25$ s
Frequency damping:	$k_F = 0.32$
	$T_{Fn} = 10$ s
Angle damping:	$k_d = (4...10)*0.17$
	$T_{id} = 1$ s
	$T_{2d} = 0.17$ s
DC-power order:	$T_P = 8$ ms
Marginal current:	$I_{marg} = 10\%$

```
 1.  NELSON RIVER MODEL, COMPLETE SYSTEM, DATA 11.23, TEST R1.1
 2. 2
 3.    000.20   000.5      000.5        0.001
 4.     25 25  0  1
 5.      1KETLO   21.05                 1270.        -750. 750.    0.
 6.      2KETHI   01.0        0.    0.    0.    0.     0.   0.    0.
 7.      3LOSLO   11.05                  980.        -750. 750.    0.
 8.      4LOSHI   01.0        0.    0.    0.    0.     0.   0.    0.
 9.      5LIMLO   11.05                 1080.        -750. 750.    0.
10.      6RAD     01.0    0.  0.    0.    0.    0.     0.   0.  229.
11.      7HEN     01.0        0.    0.    0.    0.     0.   0.  300.
12.      8BIPTRA1 11.05       0.    0.    0.        -480. 960.    0.
13.      9DOR     01.0      1000.  200.   0.    0.     0.   0.  864.
14.     10LINEBUS 01.0        0.    0.    0.    0.     0.   0.    0.
15.     11LOADBUS 21.10  0.5000. 2500.
16.    999
17.      1    2 1  0.   1.18     0.       .980          0.0
18.      2    6 2  .02  .20   450.
19.      3    4 3 0.    1.53     0.       .980          0.0
20.      4    6 4  .06  .62 10830.
21.      4    7 5  .07  .77 13500.
22.      5    7 6 0.    1.39     0.       .980          0.0
23.      8    9 7 0.     .07     0.
24.      9   10 8 0.42 1.58
25.     10   11 9 0.42 1.58
26.    999
27.    6  51RAREC1  1      2402.0 1500.       1  1500.     580 2.081.0 .93 1.2
28.    9  52DOINV1  2      2381.0 .      1500.2   890.    1880 2.021.0 .93 1.28
29.
30.    7  53HEREC1  1      2448.0 1500.       1  1500.     580 2.001.0 .95 1.32
31.    9  54DOINV2  2      2424.0        1500.2   960.    1880 2.101.0 .95 1.32
32.     9999
33.      51   52  26.78
34.      53   54  29.06
35.   9999
36. 00010 5
37.  DOV-STUDY WITH ONLY SYNCHRONOUS CONDENSERS  82-01-29
38. 11  1   2.08    4.47    7.68    1.18   49.250 100. 0 100.          4.1 1
39.         1.62    0.019   0.048   0.024   7.57
40.           289.      0.099   5.0    -3.5    1.0        0.     1.43    0.0
41. 10         0.013    0.0
42.           0.461  1224.0    0.0      0.394             8.16     0.0    -0.9
43.           4.55    0.266   0.04     0.39             0.4
44. 11  3   2.35    4.3     6.2     1.2    39.570 100. 0 100.          6.6 1
45.         1.56    0.03    0.03    0.023   6.79
46.           169.      0.05    5.0    -3.5     1.0       1.0    0.0     0.0
47. 10         0.0      0.0
48.           0.75   977.5   999.0    0.753             1.0    999.0   -0.48
49.           4.5      1.0     0.04     0.2              0.32
50. 11  5   2.35    4.3     6.2     1.2    39.570 100. 0 100.          6.6 1
51.         1.56    0.03    0.03    0.023   6.79
52.           169.      0.05    5.0    -3.5     1.0       1.0    0.0     0.0
53. 10         0.0      0.0
54.           0.75   977.5   999.0    0.753             1.0    999.0   -0.48
55.           4.5      1.0     0.04     0.2              0.32
56. 11  8   3.28   10.90   16.46    1.27   16.335 100. 0 100.        10.25 1
57.         1.80    0.11    0.32    0.023   6.79
58.           150.      0.08    6.0    -6.0     1.0       0.0    0.5     0.0
59.  0         0.006    0.0
60. 11 11   0.1     0.1     0.1             0.0 0 100. 0 100.
61.   999
62. 999
63.   5100.0310.01  10.  1.0 0.17  0.32   1.7  0.  0. 1500.       0.5
YYY
64.   5210.0310.01  10.  1.0 0.17  0.32   1.7  0.  0. 1500. 150. 0.7 0.3  51
65.   5300.0310.01  10.  1.0 0.17  0.32   1.7  0.  0. 1500.       0.5
66.   5410.0310.01  10.  1.0 0.17  0.32   1.7  0.  0. 1500. 150. 0.7 0.3  53
67. 9999
68.  9   8   9   9   8   9  10  10   9  10  11  11  10   2   6   4   6
69.      4   7
70.  4  52  54  51  53
71.  2  51  52  53  54
72.      19   14   43*  24   53/  31   83.
73.      ++   DOR V     LDBUS V   SC V
74.      02   11   86*  21   85/  35   15.  45   25-  54   35"
75.      ++   SC Q      SC P      DOR1 PDC  DOR2 PDC  LINE P
76.      05   11   82*  24   44/  35   11.  45   21-  55   41"
77.      ++   SC DELT   DOR DELT  DOR1 GAM  DOR2 GAM  HEN ALPH
78.      15   15   13*  25   23/  35   12.  45   22-
79.      ++   DOR1 VDC  DOR2 VDC  DOR1 IDC  DOR2 IDC
80.      09   14   73*  24   93/  21   13.  31   33-
81.      ++   RAD V     HEN V     KETLO V   LOSLO V
82.  0.6 99
83.    999
84.    999
85.     0.01  .050
86. 9999
87.     0.2   .005
88. 23 2
89.   52
90.   54
91. 98   1   9
92. 9999
93.     0.25  .100
94. 9999
95. 1  0.575
```

9. Sample of Input Data

APPENDIX C: NEW MANUAL FOR STATIC COMPENSATORS

Comment: This manual for the static compensator is adapted to the corresponding paragraph in the user manual for the HAMMAD/1 power system digital simulation program, written by Manitoba Hydro, 1978. Therefore some parts of the following text, which needed not to be changed, are directly copied from this user manual. The numbers of chapters and figures refer to the user manual, not to the thesis text.

6.3 Static Var Systems

Two models for static compensators are available. These are: a saturated reactor model and a general model for compensators with thyristor controlled reactors (TCR) and thyristor switched capacitors (TSC) or fixed capacitors (FC).

6.3.1 Saturated Reactor

This compensator can be modelled with its slope correcting capacitor. The inherent delay time for slope correction (usually 1/2 to 1 cycle of time duration) is specified if slope connecting capacitors are needed. To ensure the proper operation of the model with very low values for the slope, a first order lag function has been added to the model whose time constant should be chosen as 2 ms. This additional lag does practically not affct the response of the compensator and can be set to zero if not needed (i.e. values for slope reactance above 10%). Also the load balance interval should be chosen as 0.001 s (see Section 5.3.9).

6.32 Static Compensation with TCR, TSC or FC

This compensator model is illustrated in Fig. 5a. The control part consists of a PI-Regulator with current feedback which is equivalent to a lead-lag-function. The upper and lower Var limits can be chosen freely and therefore a compensator consisting only of TCR or only TSC can be simulated easily. This model replaces the two former representations of TCR and TSC compensators. Since the program operates only with fundamental frequency phasors, there is no need to distinguish in the model between TCR, TSC and FC types of compensators.

The user has the possibility to add various filters and regulator-bypass functions to the program. This can be done in the subroutine STATIC which is a part of the program. For further details refer to the listing of subroutine STATIC.

7.3 Assembling Data for Static VAR System

Data for static Var systems must immediately follow the 999 card which terminates machine, exciter and governor data. The data for static Var systems is terminated by a card having 999 punched in columns 1-3. If no static Var system is to be included with the data, just insert the 999 card after the 999 card terminating the machine, exciter and governor data.

Static Var systems are described in Section 6.3 and Figures 4 and 5. The input data for saturated reactors (SR) and compensators with thyristor controlled reactors and thyristor switched capacitors (SVS) do not have to follow in this order. The compensator type is recognized by the system code in column 7 and the SVS card has to be followed by a second card specifying Var limits and filters data. Hence the compensator types can be specified randomly.

7.3.1 Saturated Reactors

Column 1-3	The bus number from the load-flow to which the compensator is to be connected to, is entered. Format I3.
Columns 4-6	Leave blank
Column 7	System code, for SR = 2. Format I1.
Columns 8-13	Slope reactance in % on 100MVA base is entered (usually 12% to 15% on base of compensator rating). This is converted to 100 MVA base as follows: Slope reactance % = $\frac{\text{slope reactance \% on rating}}{\text{Rating in MVAR}} \times 100$ Format F6.2
Columns 14-17	The per unit knee voltage in % is entered. If left blank, the reactive power being absorbed in predisturbance steady state (0 or 1 in column 18) and slope reactance (columns 8-13) must be entered. (Format F4.1).
Column 18	Integer code defining reactive power being absorbed is entered: = 0, Reactive power is derived from load flow generated MVars at the bus. = 1, Reactive power is specified in MVars in columns 19-25 = 2, Reactive power is calculated. This occurs when knee voltage and slope reactance are known. Format I1.

Columns 19-25	Predisturbance reative power is entered in % of generated MVars at bus from load flow if integer in column 18 is 0. If integer code is 1, reactive power is specified in MVars at 1 pu voltage and then subtracted from MVars to ground in load-flow. MVars should be entered negative for SR, % value is always positive. Format F7.1.
Columns 26-30	Enter lag time constant (Fig. 4). Value usually 2 ms, but can be zero. Format F5.4.
Comumns 31-38	Leave blank
Columns 39-43	Enter delay time for slope correction (default value = 10 ms) Format F5.4.
Columns 44-48	Enter slope correcting capacitance in per unit on 100 MVA (positive if capacitive). Format F5.3.
Columns 49-53	Insert the voltage across the slope correcting capacitance in per unit at which the capacitor is bypassed. Format F5.4.

7.3.2 SVS

The SVS model is a universal representation of compensators with TCR and/or TSC. The distinction is simply made by selection of the Var limits in the inductive or capacitive range. The input data for the SVS consists always of two cards.

First Card

Columns 1-3	Bus number as for SR
Columns 4-6	The bus number which is to be regulated throughout the stability simulation is to be entered. This may or may not be the connection bus. Format I3.
Column 7	System code, for SVS = 3, Format I1
Columns 8-13	The droop in % on compensator range base is always entered. For example for a SVS with range - 100 to 200 MVar, the droop is entered on 300 MVar base. Format F6.2.
Columns 14-17	The reference voltage (voltage at which power output is zero, see Fig. 5b) is entered in %. If blank, the reference voltage is calculated

	from initial MVar and droop which must both be specified then. Format F4.1.
Column 18	Integer code defining reactive power being absorbed or generated, same as for SR.
Columns 19-25	Pre disturbance reactive power, same as for SR. It can be positive or negative for SVS, but % value is always positive.
Columns 26-30	Enter lag time constant T_Y, which can be zero. Recommended value for 60 Hz system: 5, 6, ms for 50 Hz system: 6.7 ms Format F5.4
Columns 31-35	Enter regulator gain K (see Fig. 5a) Format F5.2.
Columns 36-38	Leave blank
Columns 39-43	Regulator time constant T_R is specified in s. Format F5.4
Columns 44-53	Leave blank

Second Card

Columns 1-7	Reactive limit of the compensator is entered in MVars. Negative or zero. This can be entered at any voltage. Format F7.2
Columns 8-11	Voltage in pu for which reactive limit is specified. Format F4.3
Columns 12-18	Capacitive limit of the compensator is entered in MVars. Can be positive or zero (if TCR only). Format F7.2
Columns 19-22	Voltage in pu for which capacitive limit is specified. Format F4.3
Column 23	Regulator control code. Can be specified by user if gadget subroutine is inserted into program (see instructions in Chapter 6.3) Format I1.
Column 24-27	Threshold voltage at which regulator action is bypassed (in pu). Format F4.3.
Column 28	Filter control code is entered. With this control code the user written filter subroutines can be selected. For code = 1, a

first order low pass filter is connected. Time constant T_F has then to be entered in columns 34-38. Format I1

Columns 29-48

Four input parameters for free disposition of the user. All data specified here are only stored in a data array and are then available in all compensator subroutines. Format 4(F5.2).

Static compensator data is terminated by a card with 999 punched in Columns 1-3, whether or not any data is submitted.

Output for static compensators is automatically printed.

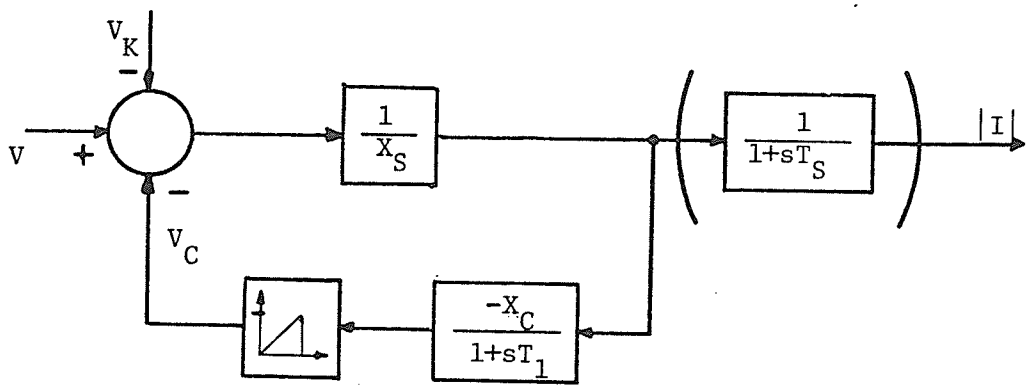


Fig. 4: Model of Saturated Reactor

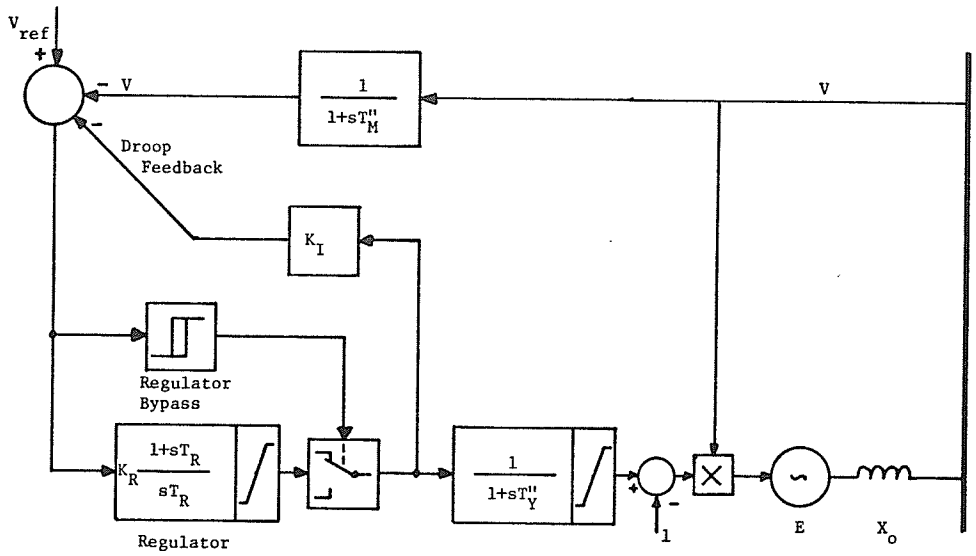


Fig. 5a: Static Compensator Model

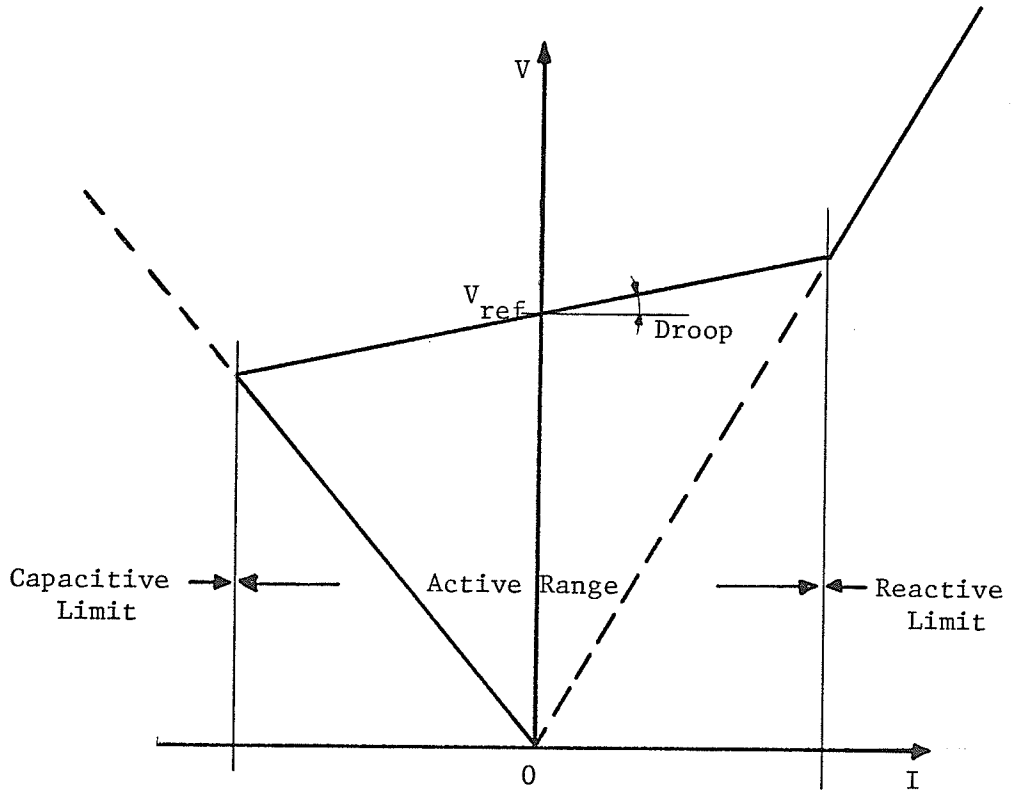


Fig. 5b: Regulator Characteristic of Static Compensator