AN AUTOMATED TESTING TECHNIQUE FOR MHO RELAYS USING A MINICOMPUTER

A Thesis

Submitted to

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JAMALUDIN BIN MOHD JARJIS

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"AN AUTOMATED TESTING TECHNIQUE FOR MHO RELAYS USING A MINICOMPUTER"

by

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ABSTRACT

A distance relay as with other protective equipment is normally tested during its factory and initial commissioning period manually, using the conventional test bench method [1]. With the advent of low-power-requirement solid state relays and minicomputers, there arises a possibility of automating the relay testing technique.

Such a test program has been written to assess the static and dynamic characteristic of a distance relay. An experimental Mho distance relay was used in the development of the test technique.

The test method is highly automated with all data handling and processing automatically performed. The test results in the forms of the relay characteristic locus and operating time are finally displayed on the graphic display terminal of the minicomputer.

The proposed automated test technique can lead to valuable savings in time and expense and as well as increased flexibility over the conventional method.

ACKNOWLEDGMENTS

The author gratefully acknowledges the help and supervision he has received from Professor G.W. Swift during the course of this study without whose guidance and encouragement this work would not have been possible. The author also wishes to express his sincere appreciation to the Dean, Professor L.M. Wedepohl, for the numerous invaluable advice and suggestions. Last, but not least, the author wishes to acknowledge his gratitude to Professor Lehn, Mr. N.J. Morphy, and Mr. A.W. De Groot of the Electrical Engineering Department and Mr. Jim Roik from the Manitoba Hydro for many helpful discussions.

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LIST OF SYMBOLS

C(I)	The magnitude of current at the I^{th} sampling instants.
C.T	Current transformer.
C_{max}	Maximum number of cycles of simulated test waveform.
d/dt	First differentiation with respect to time.
E	Source voltage.
I	Integer number between 1 and 20 for number of sample.
I_C	Magnitude of the exponential component of fault current at time equal zero.
I_F	Fault current.
I_M	The amplitude of the steady state fault current.
I_T	Transient component of the fault current.
K	The constant of the polarizing voltage.
L_2	The inductance of the fault impedance.
m	Number of samples per cycle.
N	Number of cycles.
N_T	The number of cycle at which the relay trips.
P.T.	Potential transformer.
R_1	Resistance of source impedance.
R_2	Resistance of fault impedance.
R_3	Fault resistance.
S	Input to relay.

t	Time variable.
T_I	Sampling time.
T	Time constant of the system.
$V(I)$	Magnitude of voltage at the sampling instant.
$V(N)$	Amplitude of the voltage at the N^{th} cycle.
V_o	Initial value voltage at N = 0.
V	Input relay voltage.
V_P	Polarizing voltage.
W	Frequency in radians/sec.
X	Trip signal of relay.
X_1	Reactance of the source impedance.
X_2	Reactance of the fault impedance.
$Z(N_T)$	Impedance seen by the relay.
Z_F	Impedance from the relay position to fault not including the fault resistance.
Z_L	Line impedance.
Z_N	Replica impedance of the relay.
Z_S	Source impedance.
Z_T	Total system impedance.
α	System phase angle.
β	$\theta - \alpha$
γ	Multiplication factor for voltage in the static test.
θ	Phase angle of the source voltage.
ϕ	Phase angle between the inputs of the comparator.

CHAPTER 1

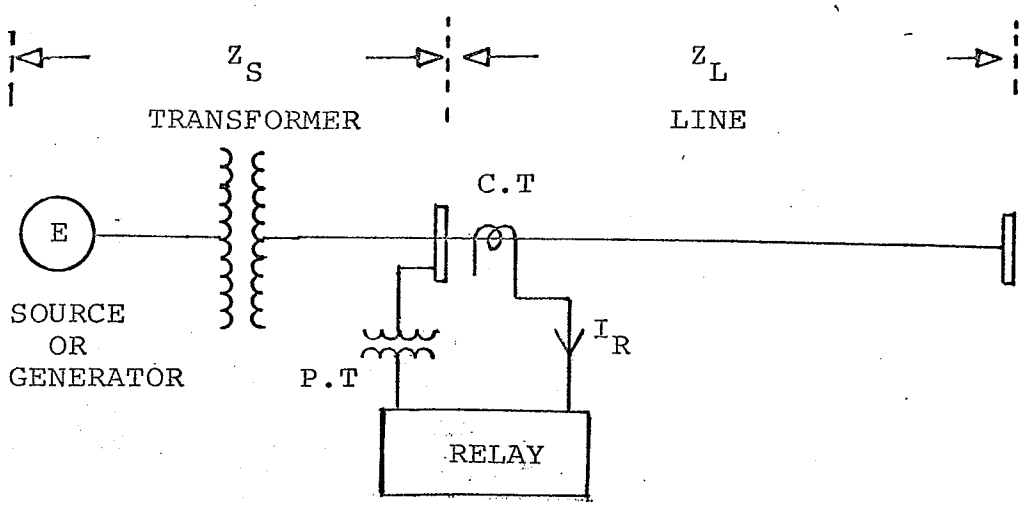
INTRODUCTION

Distance relays such as the Mho relays are used to protect a section of a power system transmission line. The Mho relay measures the distance of the inception of a fault from the terminal point by monitoring the impedance of the line and comparing it with a preset value in the relay. The preset value of the replica impedance of the relay corresponds to the impedance of the section of the line under protection. The relay recognises the occurrence of a fault on the line when the impedance it monitors falls to a value less than the preset value. Subsequently, the relay initiates a trip signal to the circuit breaker which opens the faulty line. In this way, the faulty line is prevented from possible destruction due to the high fault current. The removal of the faulty line may also prevent the system from swinging to instability. A typical protection scheme using a Mho relay is shown in Figure 1.1 (a) and (b).

1.1 Principle and Characteristic of a Static Mho Relay

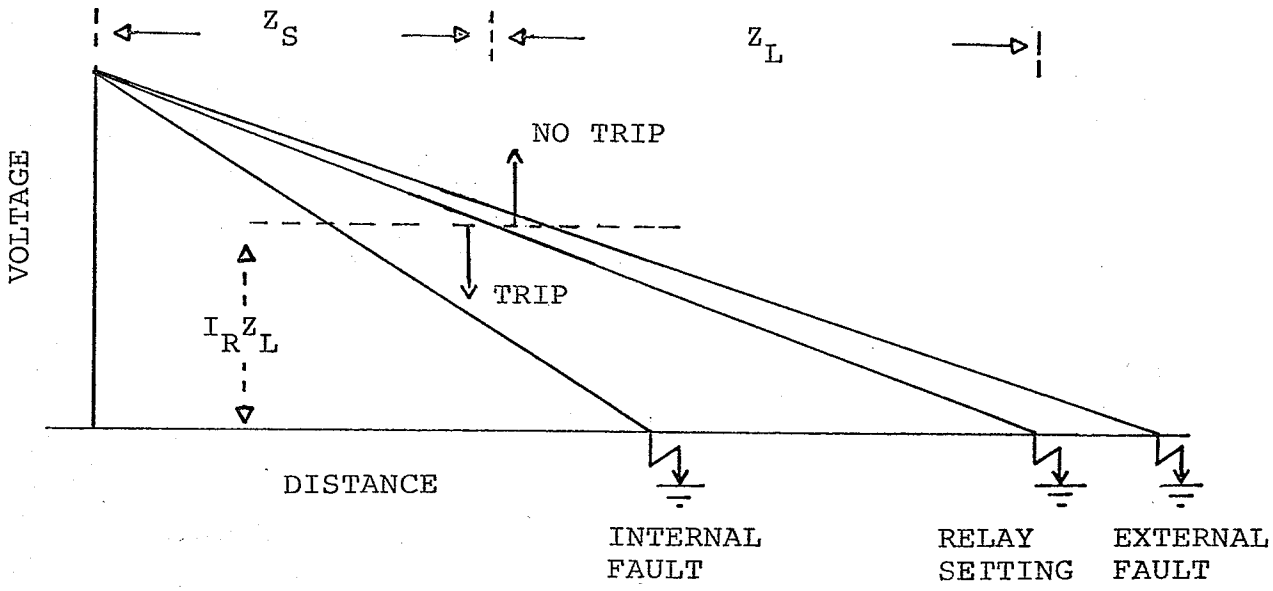
1.1.1 Unpolarised Mho Relay

The characteristic of a Mho relay was first introduced by A.R. Van C. Warrington [2]. On an impedance diagram, the Mho



An example of transmission line protection scheme using a Mho distance relay

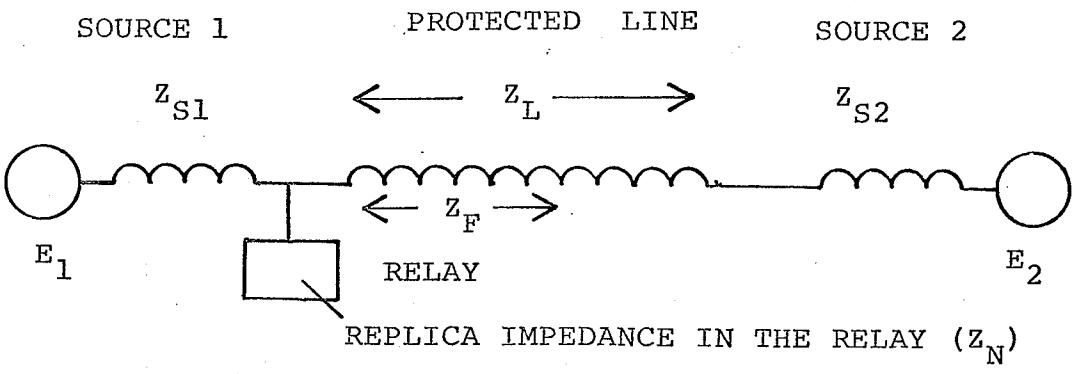
(a)

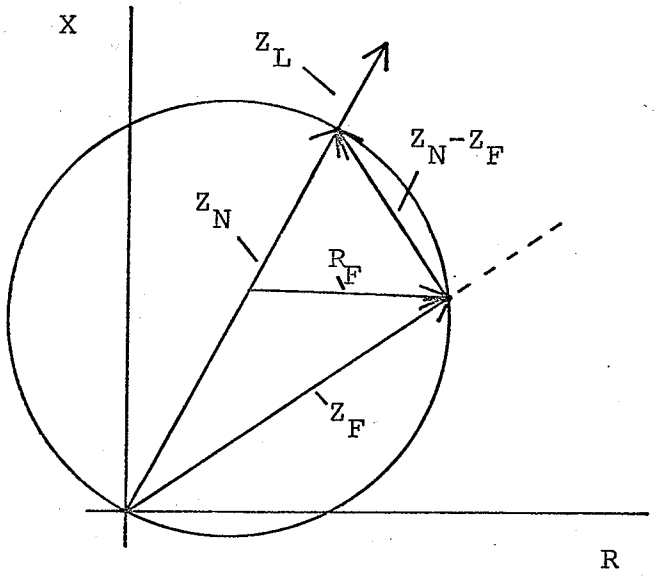


Principle of impedance distance measurement (voltage profile from source to fault)

(b)

Fig. 1.1





The theoretical characteristic of an unpolarized relay

Fig. 1.2

characteristic is a circle passing through the origin as shown in Fig. 1.2. The area which is inside the circle represents the trip zone and outside the no trip zone.

The Mho characteristic can be realised by either using a phase or an amplitude comparator. In a typical Mho relay using a phase comparator, the two inputs to the relay are

$$S_1 = V \tag{1.1}$$

$$S_2 = I_R Z_N - V \tag{1.2}$$

where

S_1 and S_2 are inputs to the comparator;

V is the voltage at the relay;

I_R is the input current to the relay;

Z_N is the replica impedance, a resistance-plus-inductance built into the relay and through which I_R is passed, (e.g., Z_N = 80% of Z_L); and

Z_F is the impedance from the relay to a fault location including the arc resistance.

The phase comparator measures the phase between the two inputs to the relay and initiates relay operation when the phase angle falls to less than ninety degrees (90^o). Thus, the criterion of operation of the relay is

where $$\overline{\Pi}/2 \leqslant \phi \leqslant \overline{\Pi}/2$$

ϕ is the phase angle between the inputs of the comparator. Such a criterion of operation as illustrated in Fig. 1.2 gives the familiar circular characteristic of a Mho relay.

1.1.2 Polarized Mho Relay

The principal aspect of a polarized Mho relay is that it has an extra memory element incorporated into the device.* The memory element holds the voltage phase information for a few cycles after an inception of a fault on the line.

Without a memory element, a relay may fail to operate properly for a close-in or terminal fault since the characteristic of an unpolarized Mho relay near the origin is a point of an uncertainty. The point of uncertainty is removed from the origin when the Mho relay is polarized. The inputs to the phase comparator of a polarized Mho relay are

$$S_1 = V + V_p \tag{1.3}$$

$$S_2 = I_R Z_N - V \tag{1.4}$$

where

V_p is the polarizing voltage from the memory element.

The polarizing voltage (V_p) ensures that the phase information of the relay voltage prior to the fault is maintained for several cycles after the inception. The voltage feeding the relay which is obtained through the voltage transformer, may be reduced to zero for close-in fault but the memory element provides the necessary phase information in a polarized Mho relay.

---

* "Sound phase polarizing" where the polarizing voltage is derived from the healthy phases of the line is another commonly used technique.

Suppose the polarizing voltage is given by the following equation [3]

$$V_p = KE$$

where

K may be complex and E is the source voltage.

The inputs to the phase comparator of the polarized Mho relay become

$$S_1 = V + KE$$

$$= I_R(Z_F + KZ_S + KZ_F) \qquad (1.5)$$

$$S_2 = I_R Z_N - V \qquad (1.6)$$

where

Z_F is the line impedance from relay to fault and

Z_S is the source impedance.

Dividing equations (1.5) and (1.6) by current (I_R) results in the following equations:

$$S_1' = KZ_S + (1 + K)Z_F \qquad (1.7)$$

$$S_2' = Z_N - Z_F \qquad (1.8)$$

Assuming (1 + K) is real, it is apparent that the characteristic of the polarized Mho relay [3] is a circle whose diameter is defined by points

$$Z_F = Z_N$$

and

$$Z_F = -(K/(1 + K)Z_S)$$

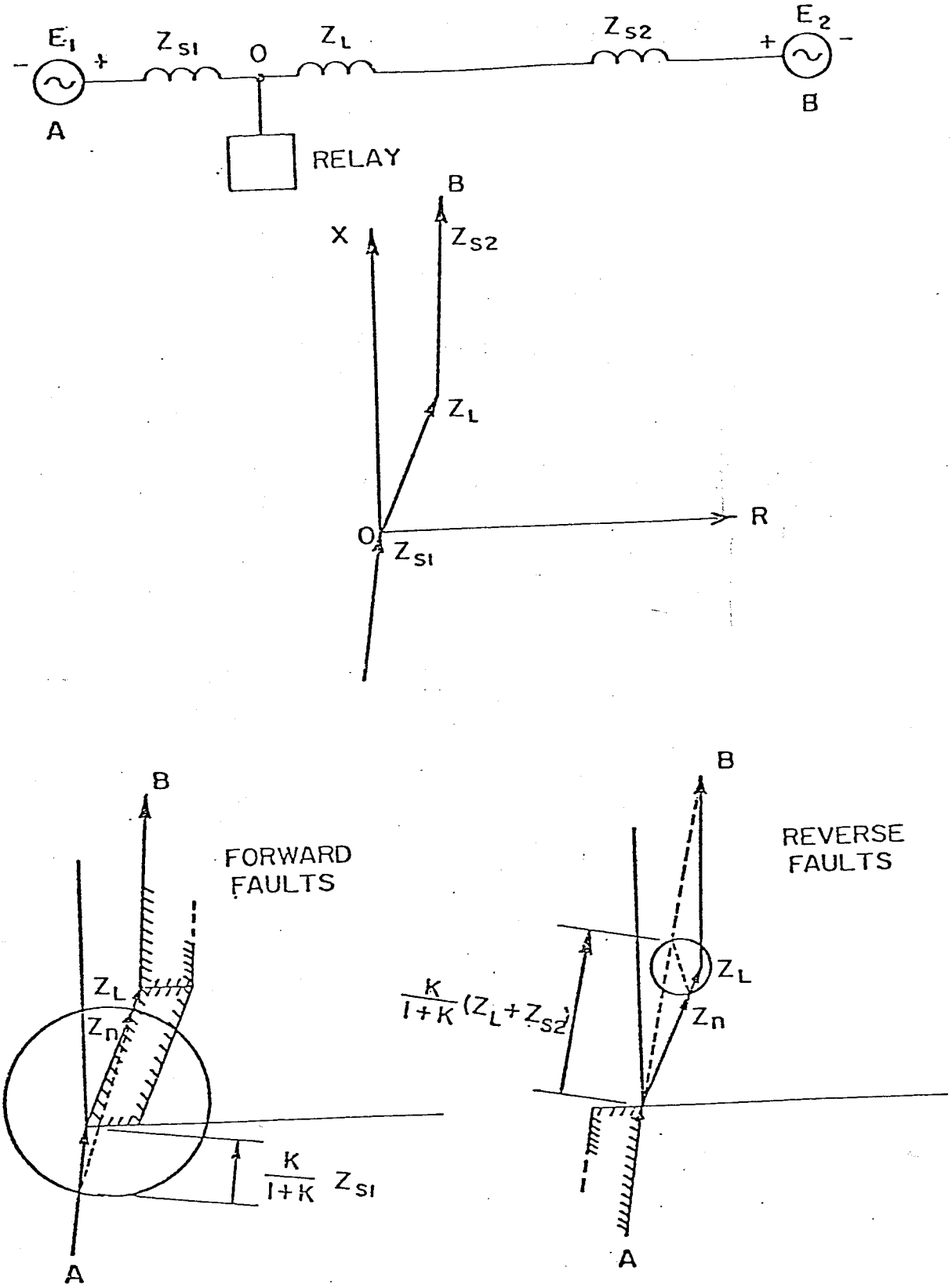


Illustration of the characteristics of a polarized Mho relay for the forward and reverse faults.

Fig. 1.3

In his work, Wedepohl [3] has also shown that for a reverse fault, the circle has diameter defined by points

$$Z_F = -Z_N$$

and

$$Z_F = -(K/(1 + K)Z_S$$

The circular characteristics of the polarized Mho relay for the forward and reverse faults are shown in Fig. 1.3.

1.2 Performance Criteria of a Static Mho Relay

In general, the performance of a static relay is expressed in terms of [3]

a) its immunity to surges

b) its static and dynamic characteristics .

The surge test attempts to establish the relay's immunity to power system surges such as those caused by switching and lightning.

The static performance test examines the characteristic of the relay for different values of current levels. This test would assess the tendency of the relay characteristic to be deformed at low current levels. The relay's accuracy and operating time under transient fault conditions are investigated too. This is normally pursued using the so-called dynamic test.

1.3 Conventional Testing Method

The conventional testing technique [1] which is used for a relay performance test was first introduced by Hamilton and Ellis [12]. The test procedure has to be done manually on a test bench. All test

parameters such as voltage, current, phase angles and trip conditions have to be recorded and processed manually. Such a task can indeed be laborious, time consuming and expensive too.

In the static test, the current is simply kept constant, but the voltage is decreased manually until the relay trips. The procedure is repeated for different phase angles so that the circular characteristic can be obtained.

In the dynamic test, the test waveforms representative of typical fault conditions have to be generated under a variety of conditions such as line length, line angle, fault resistance, source impedance and d.c. offset conditions. This could be an added cost factor to the test expenses. The measurement of test parameters is more complicated since the operating time of the relay needs also to be measured and recorded too.

Hence present testing techniques are tedious, time consuming and expensive and as well may not accurately assess the performance of a modern Mho relay.

1.4 Computer-aided Methods

Paul, Wright and Cavero [11] introduced a programmable testing technique to test a power system protective equipment. The technique stores simulated fault waveforms on an analogue system analyser and later the waveforms are reproduced to test distance relays or any other protective equipment.

The programmable testing equipment is not capable of automatic data handling and processing. All measurements and processing of parameters have to be done manually. It should be noted that the

whole sequence of the testing procedure is not integrated. Input test waveforms in the form of fault current and voltage have to be generated and stored in one locality and reproduced for testing somewhere else.

The proposed automated method in this thesis attempts to alleviate the shortcomings of the conventional method and that proposed by Paul, Wright and Cavero. The new automated testing technique originates from the realisation that the new modern electronic and solid state relay need only to be provided with information. The operating power requirement is provided separately and at much reduced level. The idea leads to the possible application of the minicomputer to relay testing techniques.

The fault condition is simulated in the computer. Through the computer interface system, the test waveforms are applied to the relay on line and the trip signal is fed back to the computer. All test data are handled and processed automatically. Hence the characteristic of the relay can be plotted automatically on the computer graphic terminal, permitting the performance of the device under test (D.U.T.) to be assessed.

CHAPTER 2

STATIC PERFORMANCE TEST

2.1 Brief Description

The test voltage and current waveforms of the static or the quasi-steady stage are assumed to be sinusoidal in nature. This assumption is consistent with the conventional test-bench method. The test waveforms are simulated in the computer and are applied to the relay via the 'Digital to Analogue Converter' (D/A) of the computer.

In order that the impedance change slowly from a no-trip value, the test current waveform is kept constant at a specified value while the voltage is decreased exponentially. The voltage has the following expression

$$V(N) = V_0(1 - \gamma)^N \qquad (2.1)$$

where

$V(N)$ is the amplitude of the voltage at N^{th} cycle,

γ is a small constant, e.g., 0.02, and

V_0 is the initial value of voltage at N = 0.

It can be easily shown that equation (2.1) has also the following recursive form

$$V_{(N+1)} = V_{(N)} * (1 - \gamma) \qquad (2.2)$$

where

$V_{(N+1)}$ is the voltage amplitude at the $(N+1)^{th}$ cycle, and

$V_{(N)}$ is the voltage amplitude at the $(N)^{th}$ cycle.

The expression in equation (2.2) is used in the test program to simulate the exponentially decreasing voltage waveforms.

The trip signal emanating from the relay is fed back to the computer through the 'Analogue to Digital Device' of the computer. If the relay trips, the computer is programmed to calculate the apparent impedance seen by the relay according to the following equation

$$Z(N_T) = \frac{\text{Magnitude of voltage at } N_T^{th} \text{ cycle}}{\text{Magnitude of current at } N_T^{th} \text{ cycle}}$$

$$= \frac{V_0(1-\epsilon\gamma)^{N_T}}{V_0(1C_0\quad)^{N_T}}$$

where

N_T is the cycle number at which the relay trips;

C_0 is the specified level of current; and

$Z(N_T)$ is the impedance seen by the relay at tripping.

The impedance seen by the relay is assumed to be negligible if the relay does not trip.

Subsequently, the computer transfers the impedance information on the graphic display terminal. The procedures is repeated automatically for different phase angles between current and voltage waveforms until the whole circular locus characteristic of the relay is displayed.

2.2 Description of System Architecture and Software

2.2.1 System Architecture

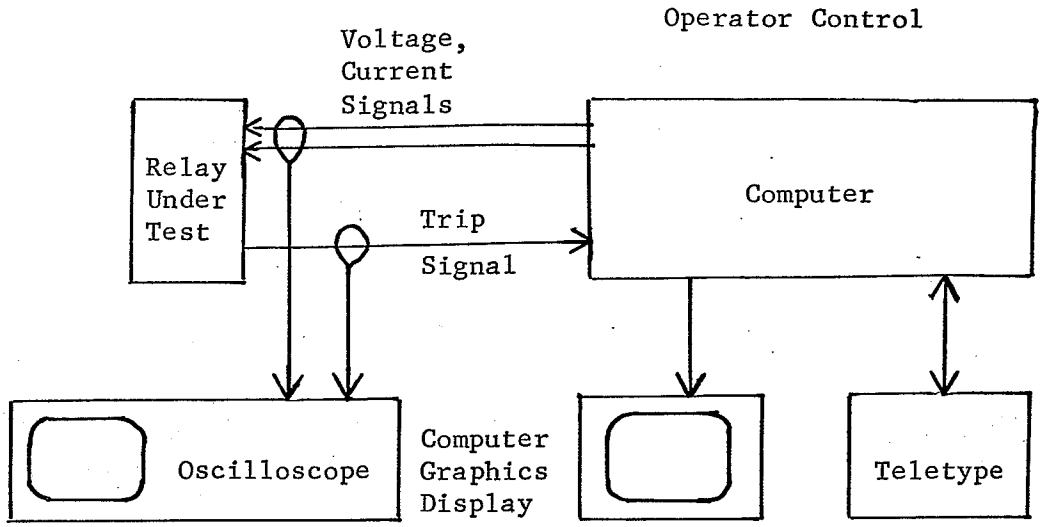
The computer is a Digital Equipment Corporation PDP-11/40 [4,5,6]. The simplified system block diagram is shown in Fig. 2.1. The PDP 11/40 minicomputer which is available at the University of Manitoba's Electrical Engineering Department, has a Central Processing Unit (CPU), Core Memory, a Unibus, a Disc storage, a LA 30 Decwriter, a CRT screen GT 40, and a Laboratory peripheral system. Further illustrations of test system are shown in Fig. 2.2.

The Unibus is the principal communication medium of the computer system peripherals. Communication between any two devices is in the form of a 'Master-Slave' relationship. All device peripherals can control the Unibus and hence can communicate with each other without the intervention of the CPU. When the Unibus is relieved of its control, the Central Processor performs other internal routines such as mathematical and logical operations.

The minicomputer has a 16K core memory. Of this, the operating system uses 6K of memory locations. The remaining 10K is available for the user.

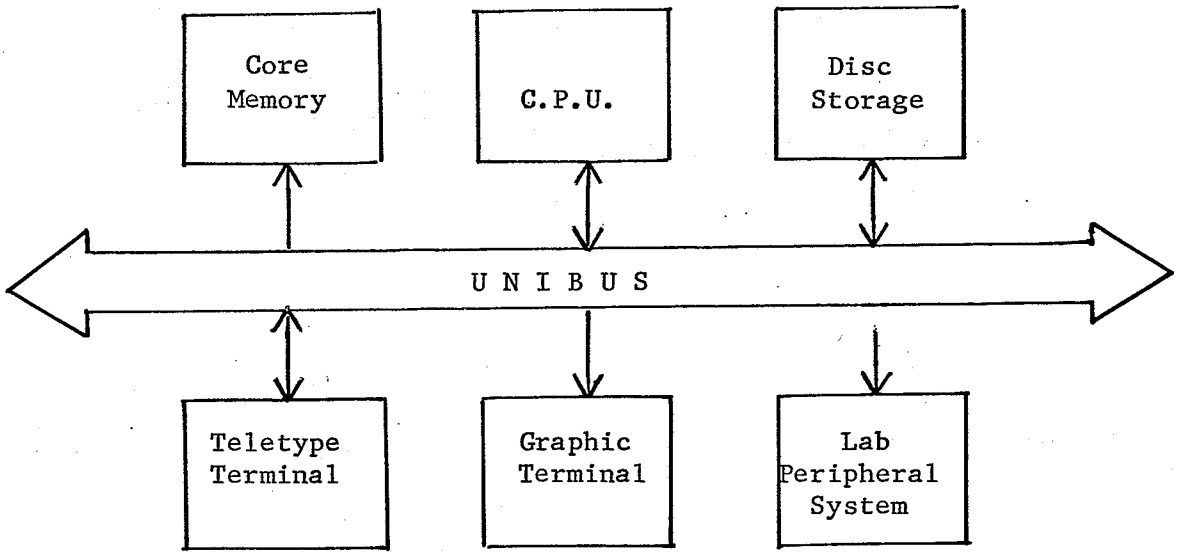
The logical and mathematical operations are performed in the Central Processor. It has eight 16 bit general purpose registers. The sixth and seventh registers are known as the stack pointer (SP) and the program counter (PC) respectively. The other six registers are available for normal programming usage. In addition, there are over four hundred hardwired instructions available.

Many devices in the computer can be programmed to control the Unibus. This procedure is done through the device-interrupt routine.



Testing system configuration

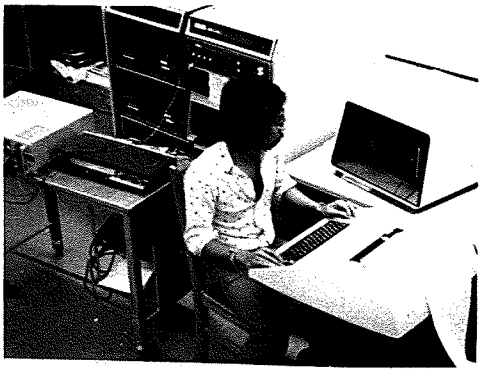
(a)



PDP 11/40 system simplified block diagram

(b)

Fig. 2.1



Photograph of test equip. ment.The relay under test is beside the oscilloscope.

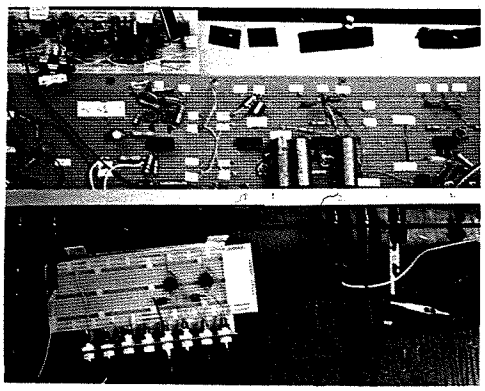
(a)

Graphic and teletype terminal.

(b)

Manual key input.

(c)



Experimental electronic relay under test.

(d)

Fig. 2.2

The clock-interrupt in particular, has been found to be very useful in this work. The former is used to realise the sampling time required to simulate the test waveforms.

The programs and instructions are normally input to the computer through the terminal called the LA 30 Decwriter. Another form of input/output peripheral is the CRT screen or what is also sometimes called the Graphics terminal. The latter is used in this work to plot the R-X diagram, and the operating-time characteristic.

One of the useful aspects of the minicomputer is that it has a Laboratory Peripheral system. The D/A channels of the LPS support are used to apply the simulated test waveforms to the device under test (D.U.T.). The Lab support also has a set of A/D channels, light emitting diodes display, a clock, and a set of relays. The A/D device is used to receive the trip response from the relay device under test.

2.2.2 System Software Support

The operating system on the Declab 11/40 is the RT 11 [7,8]. It performs all the standard users requests such as start and stop routines, and writes new programs onto a disc.

It has been mentioned that only 10K of memory locations are available in the core at a time. Such limited amount of memory may not be sufficient for large programs as in this work. Some kind of a storage economy may thus be desired. The large program which requires more than the available space is divided into several sections. Only the active sections of the program are allowed to reside in the core. The rest of the sections of the program are stored in the mass storage device, the so-called Disc Storage. Hence, a fairly large program such as the size of this test program can be conveniently run.

BASIC [6,7] is the only high level language that is available on the computer. BASIC has a syntax which is similar to the familiar FORTRAN Language. One of the differences between the two languages is that BASIC is an interactive language.

BASIC can be easily interfaced with an Assembly language routine. It can perform a routine of which BASIC is not capable and thus enhance the overall program capability. This may include the users' own written programs.

The operating system has an Assembler which enables the users to write their own routines in Assembly Language. The Assembler which is called the MACRO, produces object modules in Assembly language from the user input ASCII format. The Linkagee Editor (LINK) program takes a group of BASIC object modules and the users' own object modules, if available, and links them together to produce a main machine language program. Another program that is available in the operating system is the Text Editor (EDIT). It is used to write and input all assembly language programs into the computer and can also be used to write BASIC programs.

2.3 Device under Test (D.U.T.) - a Solid State Mho Relay

The experimental electronic mho relay which is used to test the technique developed was constructed by A.W. Degroot. The design of the relay was assisted and advised by Professor L.M. Wedepohl. The additional memory element was incorporated by Professor G.W. Swift and A.W. Degroot.

The block diagram of the static Mho relay is shown in Fig. 2.3 (a). The block average comparator was preferred over the block instan-

taneous comparator and the pulse comparison type in the design of the relay. The block average comparator [3,14] is well-known to have good immunity against transient offsets and surges. Also, the minimum operating time [14] of the comparator can be designed to be one-half of the power frequency period without incurring transient overreach and without requiring special filtering circuits in the input signals.

The mixing circuit used an operational amplifier as the analog signal processor. The circuit configuration is shown in Fig. 2.3 (b). The replica or the mimic impedance is realised by setting the impedances Z1, Z2, Z3, Z4 and Z5 to some specified values. The detailed derivation of the necessary conditions is given in the Appendix A. The outputs of the mixing circuit are the following Signals:

$$S_1 = IZ_L - V$$

$$S_2 = V + V_P$$

where

S_1 and S_2 are the outputs of mixing circuit unit;

I and V are fault current and voltage respectively; and

V_P is the polarizing voltage.

The coincidence circuit produces standard output pulses which are positive when the input signals (S_1 and S_2) are of the same polarity and are negative when they are of the opposite polarity. A typical output is shown in Fig. 2.4 (b).

The output of the coincidence circuit is fed to the integrating circuit. The integrating circuit produces an output which increases linearly when the input pulse is positive and falls at the same rate when the polarity reverses as shown in Fig. 2.4 (c).