THE UNIVERSITY OF MANITOBA

THE SIMULATION OF VARIABLE TIME DELAY USING A PROCESS COMPUTER (IBM SYSTEM/7)

BY

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ABSTRACT

A program is written in assembler language which converts the process computer, IBM System/7, into a variable delay unit (VDU). The System/7, under the program control, stores the present information and delivers the delayed information. The delay can be either time varying or constant. Some examples are taken, first solved analytically and then verified experimentally using the analog computer and the VDU. The excellent agreement between the predicted and the test results indicate that a versatile VDU has been developed. Restrictions in the use of this VDU are also discussed.

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ACKNOWLEDGMENTS

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CHAPTER I

INTRODUCTION

Systems with time delay describe processes with after effect. They are found particularly in the field of automatic control, economic studies and biological processes. The time delay encountered in a process could be either variable or constant. The analog simulation of a control system is a simple and quick method of investigating the system performance. It gives a clear insight of the system behavior. Since the simulation of the variable time delay presents a problem, many papers have been devoted on this subject [2-3].

The basic principle of this simulation is to sample a signal $x(t)$, store it in a core memory in digital form, then sample another signal $\tau(t)$ and compute from it the delayed signal address, and thus generate $x(t-\tau(t))$ by digital/analog conversion.

The above principle can be used to simulate a continuous system, provided the rate of sampling is twice the highest frequency of the signal spectrum [6].

Carson's [3] variable delay simulator although satisfactory, has the drawback that it cannot be used on repetitive operation mode for oscilloscope display. Moreover, the unit cannot be modified easily due to hard-wired construction.

To have a versatile variable time delay simulator it was decided at the very outset that a programmable system be developed using a small sensor-based digital computer (IBM System/7) as a variable time delay unit. A program is written in assembler language for the simulation of variable time delay from analog input to analog output. The repetitive

operation is possible because of the 50 microsecond sampling cycle available in the System/7 hardware.

In Chapter II, a brief description of the System/7 and its hardware limitations are outlined. The problem of matching the System/7 with the analog computer (EAI 580 Analog/Hybrid Computing System) is considered. The programming structure which converts the System/7 into a variable time delay unit is described. Chapter III deals with the accuracy of the variable delay unit. Two examples of constant time delay are taken, solved analytically and then verified experimentally. In Chapter IV, processes with the variable time delay are investigated. Chapter V concludes with a general evaluation.

CHAPTER II

VARIABLE DELAY UNIT

2.1 IBM SYSTEM/7

The System/7 is a sensor based digital computer. The storage area ranges from 2K to 16K words depending on the model of the processor module. Each word is made up of 16 bits. The processor provides 4 levels of priority interrupt processing, each of which has 7 index registers and an accumulator. The System/7 can read digital and analog inputs, and generate both digital and analog outputs. The digital input group is equipped with the process interrupt feature. The sampling of the analog input can be made dependent on the external synchronisation pulse. The maximum scanning speed of the analog input multiplexor is 20,000 samples per second. The System/7 can be programmed either as a stand alone system or by using the host computer (System/360 or System/370). The communication with the host computer is supported through the telecommunication access method. The detailed information about the System/7 can be found in IBM publications [7-10].

2.1.1 Hardware Limitations

Analog input: The analog input voltage ranges from -5.12V to 5.12V.

Analog output: The analog output is unipolar with a range of 0 to 10.24V.

2.2 MATCHING PROBLEM

The operating voltage range of the analog computer (EAI 580 Analog/Hybrid Computing System) is [-10, +10]. Due to hardware limitations of

the System/7, a scheme is required to mate it with the analog computer. The matching scheme shown in Fig.(2.1) is described below:

The signal $x(t)$ generated by the analog computer is halved and then fed to the System/7. After sampling and A/D conversion, the digital equivalent of 5V is added and then stored. The stored digital signal, $[\frac{1}{2}x(t)+5V]$ occupies the equivalent of the voltage range [0, 10] thus ensuring that, on conversion, the output will be positive. The actual output of the System/7 after D/A conversion, will be $[\frac{1}{2}x(t-\tau(t) + 5V]$, from which 5V is subtracted and the result doubled, producing the required delayed signal $x(t-\tau(t))$.

Since, a real process is considered, the variable time delay $\tau(t)$ is nonnegative. The analog signal representing $\tau(t)$ can have a voltage range, [0, 10.23].

The 'operate' logic of the analog computer is fed to the digital input group with the process interrupt feature. The external synchronisation pulse is provided by the analog computer which is capable of generating 5 volt, 1 microsecond pulses at a variety of repetition rates [11].

2.3 PROGRAM STRUCTURE

The System/7 digital computer is programmed to simulate a variable time delay from analog input to analog output. For each 'channel', the program requires the computer to sample the signal $\frac{1}{2}x(t)$, add 5V, store it, sample another signal $\frac{1}{2}\tau(t)$ and compute from it the required address for the output, retrieve it (the output) and generate the output $[\frac{1}{2}x(t-\tau(t))+ 5V]$. On loading this program, the System/7 behaves as a Variable Delay Unit (VDU) as shown in Fig.(2.2). The system as programmed is capable of simulating two independent delay channels.

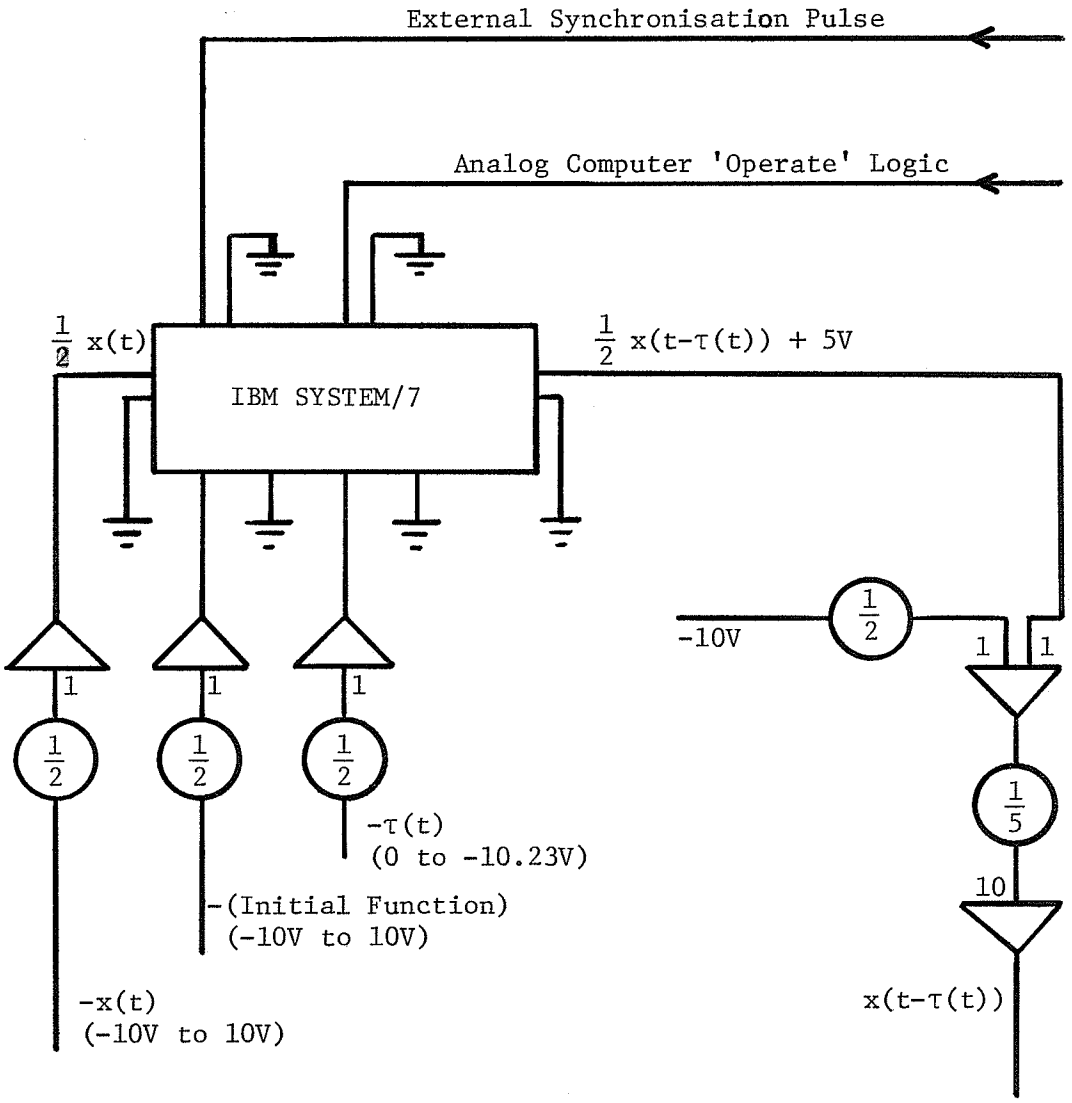


Fig.(2.1) Matching Scheme

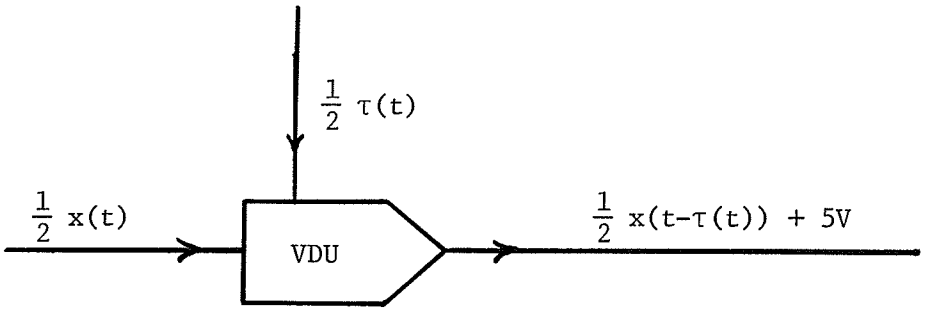


Fig.(2.2) System/7 as a Variable Delay Unit

2.3.1 Processing Period

The processing period of the VDU consists of the time required for (i) the A/D conversion, (ii) the computation and (iii) the D/A conversion. This period should be less than 50 microsecond for the successful operation of the VDU at the maximum sampling rate of 20,000 Hz. This restriction dominates the program evolution.

2.3.2 Storage Detail

For each channel, the storage area consists of two consecutive sections of 1024 addresses each, the first section is used for the initial function table and the second section for the x(t) table. This is shown in Fig.(2.3).

An initial function of sufficient length in time [1] is stored in the initial function table. When the problem solution is initiated, the current values of x(t) are stored in the x(t) table sequentially until the whole 1024 addresses are filled. The storage position then reverts to the first address of x(t) table. Since, through programming

Fig.(2.3) The storage area

it can be arranged that τ_{max} never exceeds 1023 addresses, there is no need to use the memory that has been over written.

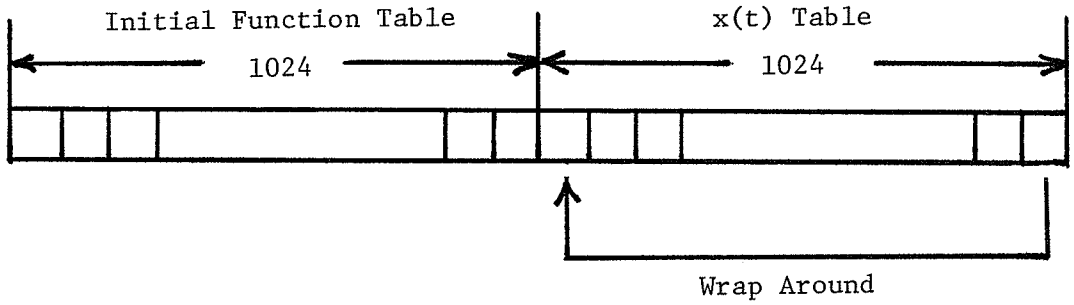


Fig.(2.3) The Storage Area

2.3.3 The Delay

The variable time delay is given by the relation

$$\tau(t) = \frac{n}{N} \text{ sec} \qquad (2.1)$$

where where n = address increment number

and N = number of samples/sec

After sampling and digital conversion of the signal $\frac{1}{2}\tau(t)$, the data are shifted logically to the right by 5 bits, which produces the desired address increment number. Shifting the data logically to the right by 5 bits is equivalent to dividing the data by 32. A divide sub-routine of the System/7 requires larger execution time than that of logical shifting. Hence, logical shifting is chosen. The following example illustrates the technique.

$\tau(t)$ (secs)	$\tau(t)$ (volts)	$\frac{1}{2}\tau(t)$ (volts)	after A/D conversion (Hexadecimal)	after shift operation (Hexadecimal)	n (Decimal)
0.0	0.0	0.0	/0000	/0000	0
5.12	5.12	2.560	/4000	/0200	512
10.23	10.23	5.115	/7FE0	/03FF	1023

(0.3125 mV = 1 least significant bit, 5.12V = /8000)

Thus for example, τ_{max} = 10.23 secs may be accommodated by setting the sampling rate to 100 Hz.

The voltage signal that represents the time delay is then given by

$$\tau(\text{volts}) \equiv \frac{N}{100}\,\tau(\text{secs}) \qquad (2.2)$$

2.3.4 Execution Indicators

The indicator W is used to set the table pointer at the beginning of the x(t) for every fresh run of the problem and to wrap around the x(t) table. Initially, it is set to zero. W = 0, places the table pointer at the first address of x(t) table and then sets itself (W) to 1. When the table pointer reaches the end address of x(t) table, W is again set to zero.

The indicator C is used in computing the delayed output address. Initially, it is set to zero. When the table pointer reaches the end address of the x(t) table, C is equated to unity.

2.3.5 Program Outline

The System/7 program is prepared on a host computer (the IBM System/360), using the host program preparation facilities [9]. The host computer produces storage load modules that can be loaded into the System/7

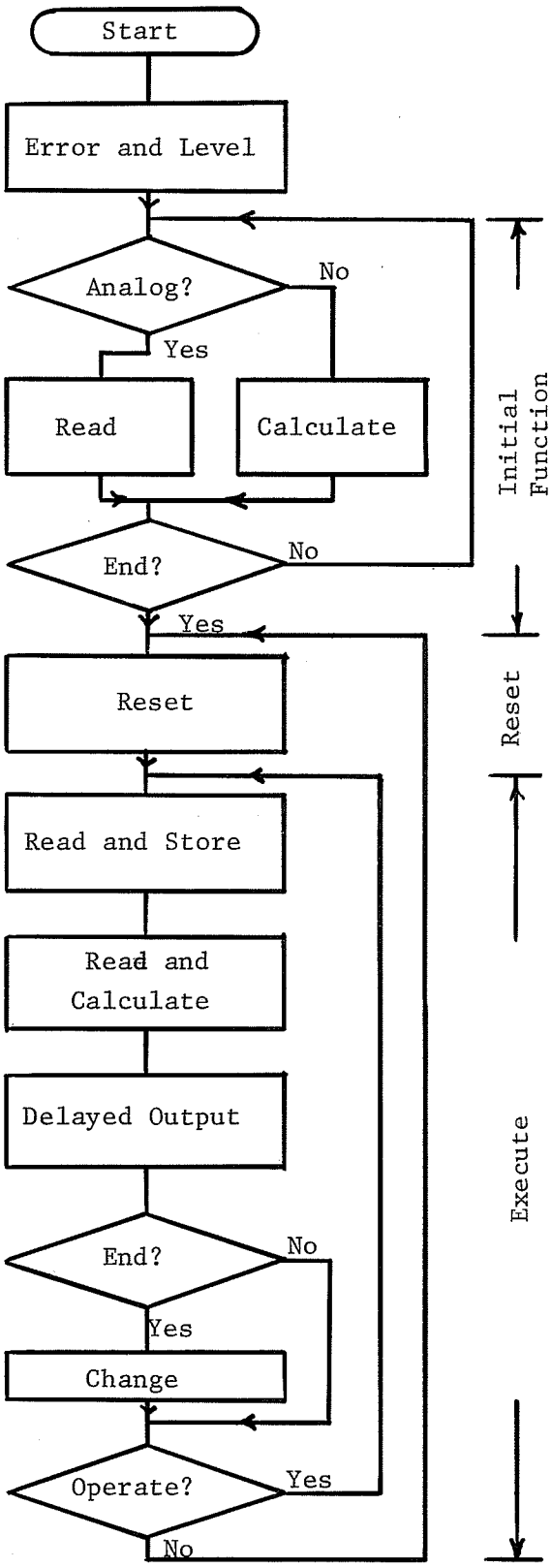
via teleprocessing. For the initial program load (IPL), the host attachment switch on the System/7 console should be in the enable and IPL position. At the end of IPL, the System/7 starts executing the program. The program flow chart diagram, shown in Fig.(2.4), is described below:

The error routine and the address pointers to level tables are stored in the reserved storage locations of the System/7 [8]. The level 0 is used to service the 'reset' subroutine. The level 1 is used to service the 'initial function' subroutine. The levels 2 and 3 are used to service the 'execute' subroutine.

The 'initial function' subroutine checks the type of initial function. For an analog type initial function, the System/7 samples the analog signal, converts it into the digital form, adds 5V and then stores it in the initial function table. For the functional type initial function, it calculates the initial function from the given equation. If both channels are in operation, two initial functions are stored. When the initial function table is full, the processor goes to service the 'reset' subroutine.

In the 'reset' subroutine, the execution indicators are reset for a fresh run of the problem. The digital input group with the process interrupt feature is prepared, which keeps track of the analog computer operating mode. If the analog computer is in the 'initial condition' mode, the processor goes to the 'wait' state. The processor exits the 'wait' state and goes to service the 'execute' subroutine when the analog computer is put into the 'operate' mode.

In the 'execute' subroutine, the signal $\frac{1}{2}x(t)$ is sampled, 5V added and then stored in the $x(t)$ table. The signal $\frac{1}{2}\tau(t)$ is sampled, from which the address of the delayed output is calculated. The delayed



Store the error routine and level tables in the reserved storage locations.

Is it an analog type initial function?

Read or calculate the initial function, add 5V, and then store in the initial function table.

Is it the end of the initial function table?

Reset the execution indicators and wait until the analog computer operates.

Read $\frac{1}{2}$ x(t), add 5V, and then store in the x(t) table.

Read $\frac{1}{2}\tau(t)$ and then calculate the address of the delayed output.

Generate the signal $\frac{1}{2}x(t-\tau(t))+5V$

Is it the end of the x(t) table?

Change the Execution Indicators.

Is the Analog Computer in 'operate' mode?

Fig.(2.4) Program Flow Chart

analog output, $[\frac{1}{2}x(t-\tau(t) + 5V]$, is generated after D/A conversion. If both channels are in operation, the level 3 services the channel 1 operation and the level 2 services the channel 2. Next, the analog computer operating mode is checked. The processor goes to loop the 'execute' subroutine if the analog computer is operating, otherwise, it goes to service the 'reset' subroutine.

2.4 QUANTIZATION ERRORS

The A/D converter has an accuracy of 0.05% of full scale. The output voltage established by the D/A converter has an accuracy of 0.1% of full scale. Therefore, the D/A converter introduces a small error in producing the delayed output.

The variable time delay is also quantized and has a resolution of 1 part in 1023.

CHAPTER III

VDU PERFORMANCE

Two tests were devised to determine the static accuracy of the variable delay unit (VDU). These problems, contributed by Prof. R.A. Johnson, have fixed time delays. They were originally formulated to determine the sensitivity of solution to a change in the number of samples used to represent the delay - in particular - the stability limit dependence on this number. Here they are used to evaluate the simulation accuracy since the analytical results are exact.

3.1 EXAMPLE 1

The system shown in Fig.(311a) is described by the differential-difference equation

$$\dot{x}(t) = -\alpha x(t-\tau) \tag{3.1}$$

The identically zero solution is stable provided $\alpha\tau < \frac{\pi}{2}$ [1].

3.1.1 Analysis

Let the delay τ be represented by N samples of time increment Δ so that

$$\tau = N\Delta \tag{3.2}*$$

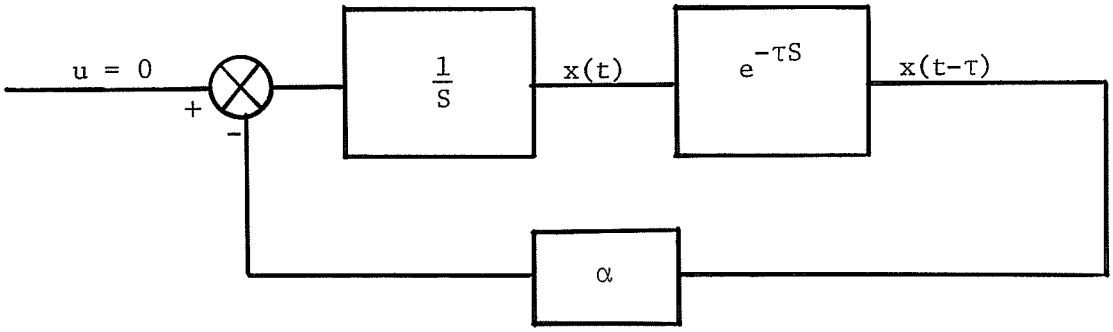
In the $(n\Delta, \overline{n+1}\Delta)$ interval, Eq.(3.1) becomes

$$\dot{x}(t) = -\alpha x(\overline{n-N}\Delta) \tag{3.3}$$

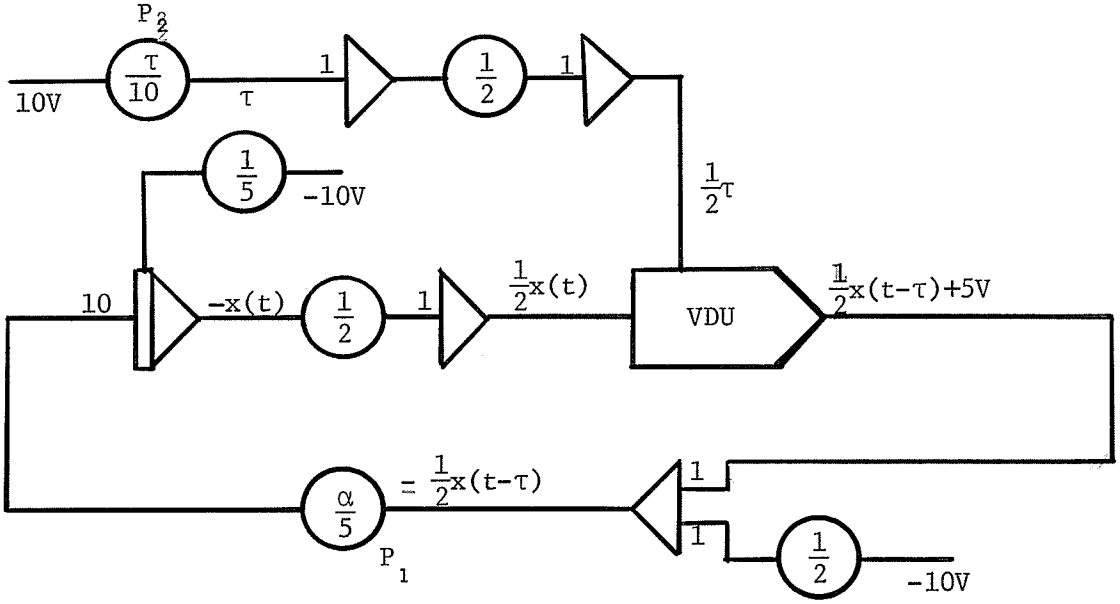
Therefore, in this interval,

$$x(t) = x(n\Delta) - \alpha x(\overline{n-N}\Delta)(t-n\Delta)$$

* Note that N is the number of samples in the time delay.



(a) System Block Diagram



(b) Simulation Diagram

Fig.(3.1) Example 1

and so

$$x(\overline{n+1}\Delta) = x(n\Delta) - \alpha\Delta x(\overline{n-N}\Delta) \tag{3.4}$$

Define $$x(j\Delta) = x_j \tag{3.5}$$

Then (3.4) becomes

$$x_{n+1} = x_n - \alpha\Delta x_{n-N} \tag{3.6}$$

In order to determine the limit of α for the stability of the null solution of this discrete approximation ($x_j \equiv 0$), suppose that

$$x_n = A\gamma^n \tag{3.7}$$

substitution of (3.7) in (3.6) produces

$$\gamma^{N+1} = \gamma^N - \alpha\Delta$$

Since, $\Delta = \tau/N$, the above equation becomes

$$\gamma^{N+1} - \gamma^N + \alpha\tau/N = 0 \tag{3.8}$$

The limit of stability will occur when the amplitude of successive x_j's are identical; that is, when

$$\gamma = e^{j\phi/N} \tag{3.9}$$

where ϕ is the phase shift during the time delay τ.

If $\gamma = e^{j\phi/N}$ is a root of the Eq.(3.8), then $\alpha\tau$ can be found for different values of N. Furthermore, as N tends to infinity, $\alpha\tau$ should approach $\frac{\pi}{2}$, which is the stability boundary of the differential-difference equation.

Substitution of $\gamma = e^{j\phi/N}$ in Eq.(3.8) produces

$$e^{j(1+\frac{1}{N})\phi} - e^{j\phi} + \alpha\frac{\tau}{N} = 0 \tag{3.10}$$

Equating of real and imaginary parts produces

$$\cos(1 + \frac{1}{N})\phi - \cos\phi + \alpha\frac{\tau}{N} = 0 \tag{3.11}$$

$$\sin(1 + \frac{1}{N})\phi - \sin\phi = 0 \tag{3.12}$$

From Eq.(3.12)

$$\sin\phi = \sin(1 + \frac{1}{N})\phi$$

Possible solutions are

$$\phi = (1 + \frac{1}{N})\phi = 0 \qquad \text{or}$$

$$\pi - \phi = (1 + \frac{1}{N})\phi$$

limiting ϕ to the range $(-\pi, \pi]$.

The first of these contradicts Eq. (3.11) and is therefore discarded. The second leads to

$$\phi = \frac{N\pi}{2N+1} \tag{3.13}$$

Substitution of the value of ϕ in Eq.(3.11), and simplification produces

$$\alpha\tau = 2N \sin\frac{\pi}{4N+2} \tag{3.14}$$

For the limiting case,

$$\lim_{N \to \infty} \alpha\tau = \frac{\pi}{2}$$

which is in agreement with the continuous case [1].

Let T_N be the time period of the sinusoidal solution, then,

$$\frac{\phi}{\tau} T_N = 2\pi \tag{3.15}$$

Substituting the value of ϕ produces

$$T_N = (4 + \frac{2}{N})\tau \tag{3.16}$$

As $N \to \infty$, the limiting period

$$T_\ell = 4\tau \tag{3.17}$$

The time period in the limiting case can also be derived in the following manner [1].

The equation

$$\dot{x}(t) = -\frac{\pi}{2\tau} x(t-\tau) \tag{3.18}$$

supports a solution of the form $e^{j\omega t}$, provided

$$j\omega + \frac{\pi}{2\tau} e^{-j\omega\tau} = 0 \tag{3.19}$$

Equating real and imaginary parts,

$$\frac{\pi}{2\tau} \cos \omega\tau = 0$$

$$\omega - \frac{\pi}{2\tau} \sin \omega\tau = 0$$

The value of ω which satisfies these two equations simultaneously is

$$\omega = \frac{\pi}{2\tau}$$

with the corresponding time period

$$T = 4\tau$$

This result verifies that of Eq.(3.17).

3.1.2 Simulation

This system is simulated using the analog computer and the System/7 as a VDU as shown in Fig.(3.1b). In this experiment, τ is assumed to be 1 second, and the voltage signal representing this time delay is calculated from the Eq.(2.2). The potentiometer P_2 is used in setting τ. The potentiometer P_1 represents the value $\frac{1}{5}\alpha$. For a certain sampling rate N, P_1 was set at a value such that the system is stable. Then P_1 was increased and the response was observed in an oscilloscope. In this way, α_c (the critical value of α) was determined. A change of $\pm$ 0.0010 (1%) in the P_1 setting from the critical setting makes the

system either unstable or stable.

3.1.3 Experimental Results

N (no. of samples/sec)	α_c (Analytically)	α_c (Experimentally)
2	1.23607	1.230
5	1.42315	1.420
10	1.49460	1.490
20	1.53411	1.530
100	1.56152	1.555
10000	1.57002	1.565

The experimental values of α_c are quite close to the analytical calculations. For N = 100 Hz, the problem solution x(t) is almost sinusoidal (as observed in the oscilloscope) and the period of oscillation is 4 secs. which is 0.5% lower than the predicted value. The period of oscillation does not change for N > 100 Hz.

The possible sources of error are the quantization error of the System/7 and the potentiometer settings of the analog computer.

3.2 EXAMPLE 2

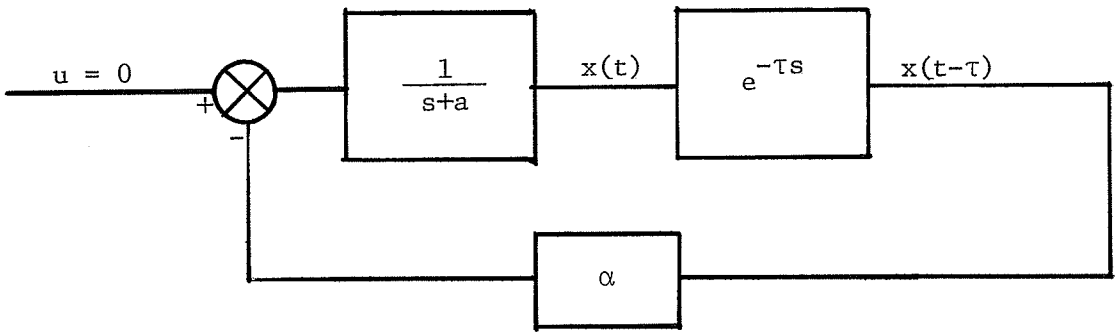
The system shown in Fig.(3.2a) is described by the differential-difference equation

$$\dot{x}(t) + ax(t) = -\alpha x(t-\tau) \qquad (3.20)$$

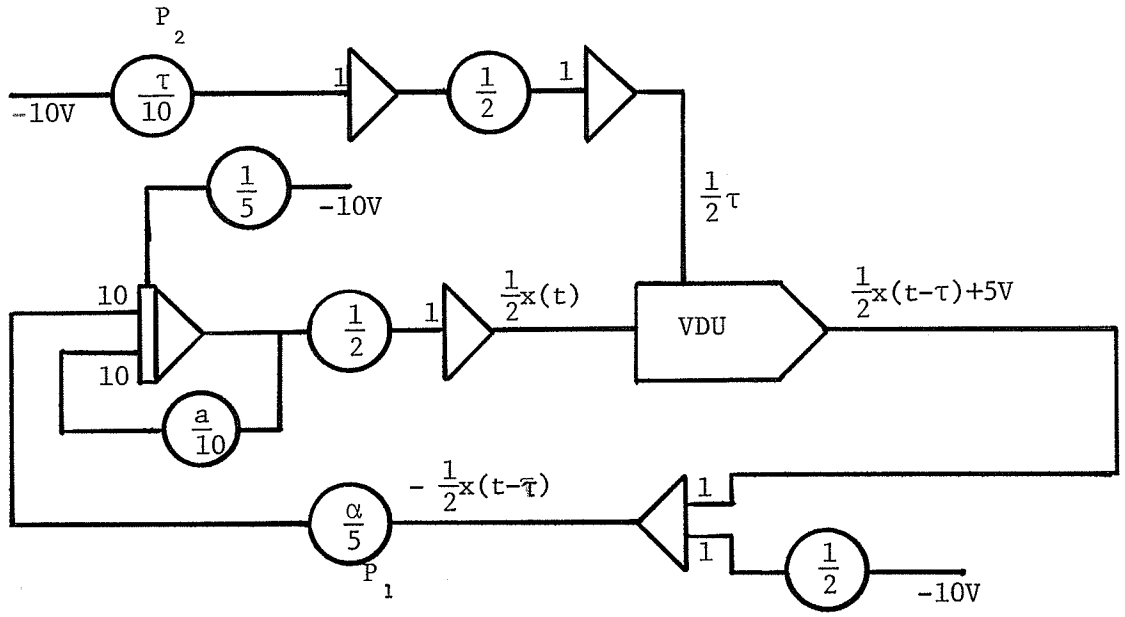
The stability region of this system [1] is shown in Fig.(3.3)

3.2.1 Analysis

Following the previous procedure, the stability limit solution of

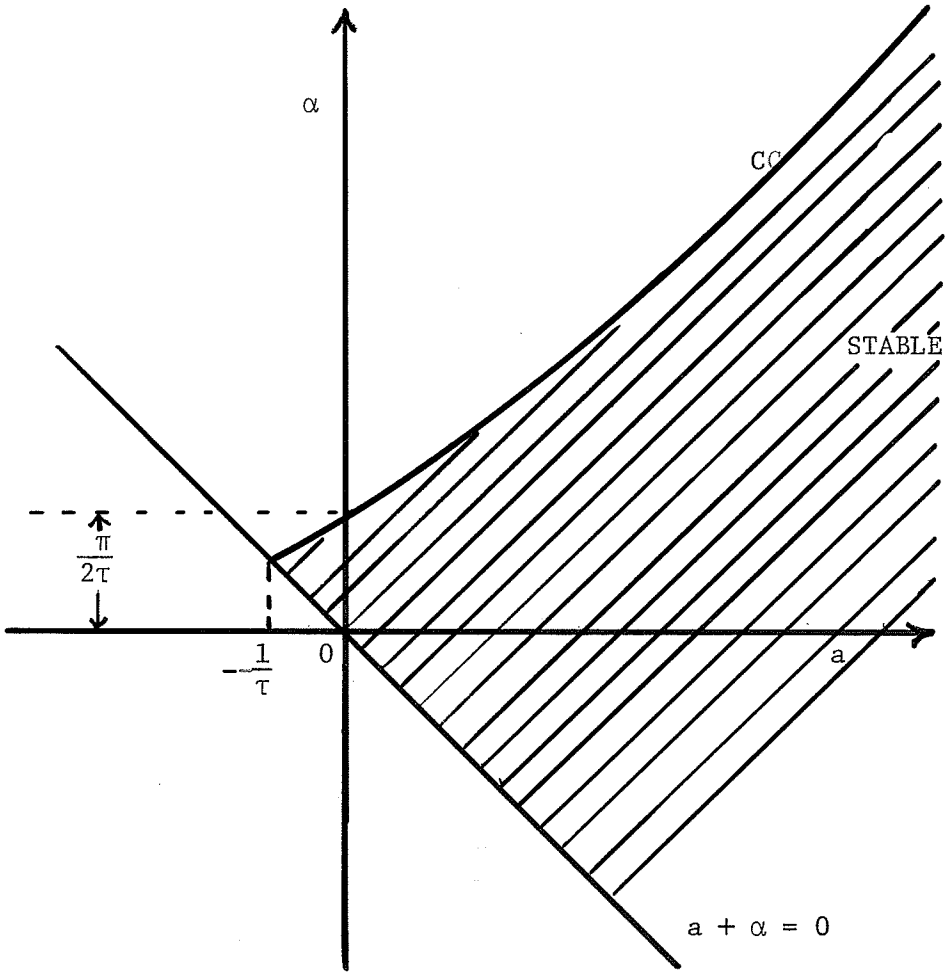


(a) System Block Diagram



(b) Simulation Diagram

Fig.(3.2) Example 2



The parametric equations for the curve C are

$$a = -\frac{\omega\cos\omega\tau}{\sin\omega\tau}$$

$$\alpha = \frac{\omega}{\sin\omega\tau}$$

for $0 < \omega\tau < \pi$

Fig.(3.3) Stability Region

the Eq.(3.20) may be written as

$$e^{\frac{a\tau}{N}} e^{j(1+\frac{1}{N})\phi} - e^{j\phi} + \frac{\alpha}{a}(e^{\frac{a\tau}{N}} - 1) = 0 \tag{3.21}$$

Equating real and imaginary parts

$$e^{\frac{a\tau}{N}} \cos(1+\frac{1}{N})\phi - \cos\phi + \frac{\alpha}{a}(e^{\frac{a\tau}{N}} - 1) = 0 \tag{3.22}$$

$$e^{\frac{a\tau}{N}} \sin(1+\frac{1}{N})\phi - \sin\phi = 0 \tag{3.23}$$

From Eq.(3.23)

$$e^{\frac{a\tau}{N}} = \frac{\sin\phi}{\sin(1+\frac{1}{N})\phi} \tag{3.24}$$

Substituting the value of $e^{\frac{a\tau}{N}}$ in Eq. (3.22) and simplifying, gives

$$\frac{\alpha}{a} = -\frac{\cos\frac{1}{2N}\phi}{\cos(1+\frac{1}{2N})\phi} \tag{3.25}$$

For a given value of a, τ and N, Eq.(3.24) can be solved for ϕ, and the corresponding value of α can be obtained from the Eq.(3.25).

Since for all N, $\phi = 0$ is also a solution of the Eq.(3.23), substitution of this value in the Eq.(3.25), produces

$$\frac{\alpha}{a} = -1 \tag{3.26}$$

The physical interpretation is that for the positive feedback, α_c is independent of the sampling rate.

The Eq.(3.24) can be converted into the form,

$$\tan\phi = \frac{\sin\frac{1}{N}\phi}{e^{\frac{-a\tau}{N}} - \cos\frac{1}{N}\phi} \tag{3.27}$$

from which for large N,

$$\tan\phi \simeq -\frac{1}{a\tau}\phi \tag{3.28}$$

Also, for $N \to \infty$,

$$\frac{\alpha}{a} = -\frac{1}{\cos \phi} \tag{3.29}$$

The limiting values of ϕ and α [Eq.(3.28-3.29)] check with the continuous case [1].

3.2.2 Simulation

The simulation diagram is shown in Fig.(3.2b). The fixed time delay is assumed to be 1 sec. The voltage signal representing this delay is calculated from the Eq.(2.2) and set using the potentiometer P_2. P_1 is used to vary α . The experimental procedure is similar to the previous example. The system response is sensitive to a 1% change in the P_1 setting.

3.2.3 Experimental Results

With negative feedback

N	α_c (Analytically)	α_c (Experimentally)
2	1.88508	1.880
5	2.10728	2.100
10	2.18493	2.180
100	2.25425	2.250
1000	2.26104	2.255

With positive feedback

N	α_c (Analytically)	α_c (Experimentally)
10	-1.000	-1.000
100	-1.000	-1.000
1000	-1.000	-1.000

3.2.4 Comments

For positive feedback (negative α), the problem solution is exponential (as observed in the oscilloscope) which decays or grows depending on the value of α . The critical value of α does not depend on the number of samples which confirms the physical interpretation of Eq.(3.26).

For negative feedback (positive α), the experimental values of α_c are in good agreement with the analytical calculations. The possible sources of error are the quantization errors of the System/7 and the potentiometer settings of the analog computer.

CHAPTER IV

VARIABLE DELAY SYSTEMS

4.1 DOPPLER EFFECT

The changing pitch of sound, e.g. that of a fire engine siren passing at a high speed, is familiar to all. This happens due to the relative motion between the sound source and the receiver or observer.

4.11 Analysis

A simple situation is illustrated in Fig. (4.1) in which the observer R moves along a straight line towards the source at 0 (origin), with a constant velocity v smaller than the velocity of sound c.

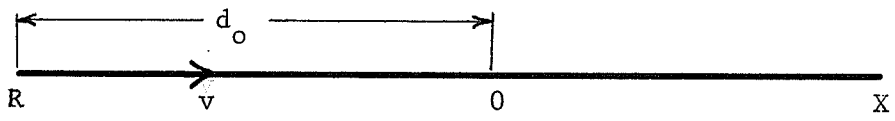


Fig. (4.1) Doppler Shift

Let $v = mc$, where $m < 1$. Since the source is at rest in the medium, the source frequency f_s is related to the wavelength of sound in the medium, λ by

$$f_s = \frac{c}{\lambda} \tag{4.1}$$

and the observed frequency is, therefore, given by

$$f_o = \frac{c + v}{\lambda}$$

or

$$f_o = (1 + m) f_s \tag{4.2}$$

This frequency shift is known as the Doppler Shift. The above derivation will be found in most physics textbooks.

4.1.2 Variable Delay approach

The Doppler Shift can be treated as a system with a variable time delay.

Let $x_s(t)$ be the source signal and d_o be the distance of the observer from the origin 0 at time t = 0.

The observed signal,

$$x_o(t) = x_s(t - \tau(t)) \tag{4.3}$$

where the variable time delay,

$$\tau(t) = \frac{d_o}{c} - \frac{v}{c} t$$

or $$\tau(t) = \tau_o - mt \tag{4.4}$$

If $$x_s(t) = A \sin 2\pi f_s t$$

then $$x_o(t) = A \sin 2\pi f_s [(1+m)t - \tau_0]$$

which verifies the fact that the observed frequency,

$$f_o = (1 + m) f_s \tag{4.5}$$

To speak of 'the observed frequency' is meaningful in this case because the observed signal $x_o(t)$ is sinusoidal.

When the sound source moves past the observer, the Eq.(4.4) takes the form

$$\tau(t) = mt \tag{4.6}$$

and the observed frequency,

$$f_o = (1 - m) f_s \tag{4.7}$$

4.1.3 Simulation

The analog simulation diagram is shown in Fig.(4.2). The Eq.(4.4) is used in simulating the variable time delay. When the sound source passes the observer and continues to move towards X, the variable delay is simulated by the Eq.(4.6)

4.1.4 Experimental Results

Observation no.	Source frequency f_s	Ratio of source to sound velocity m	Source moving towards the observer		Source moving away from the observer	
			Predicted f_o	Observed f_o	Predicted f_o	Observed f_o
1	0.50	0.50	0.75	0.72	0.25	0.25
2	2.00	0.50	3.00	2.90	1.00	0.96
3	2.00	0.25	2.50	2.50	1.50	1.47

The strip chart recording for the observation no. 1 has been shown in Fig.(4.3).

4.1.5 Comments

The excellent agreement between the predicted and the experimental results justifies the use of this VDU in solving problems containing the variable time delay.

Possible sources of error are (i) strip chart recorder calibration error (ii) analog computer error and (iii) the quantization error of the System/7.

4.1.6 An Extension

In this example, the position of the source will be altered and

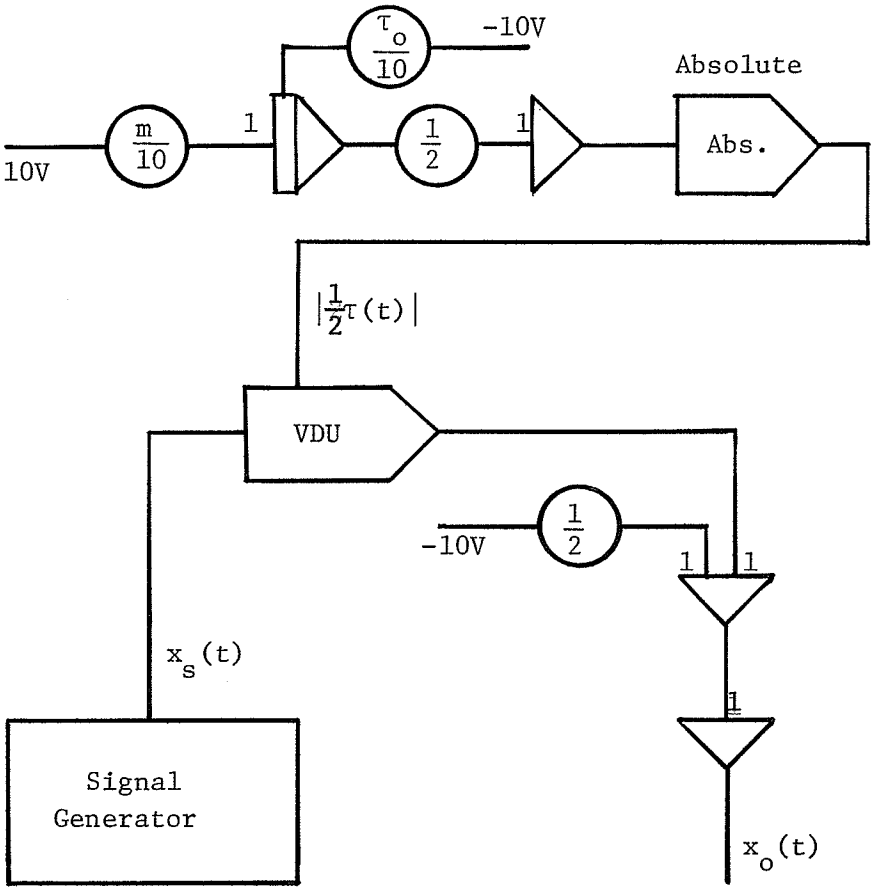


Fig.(4.2) Doppler Shift Simulation

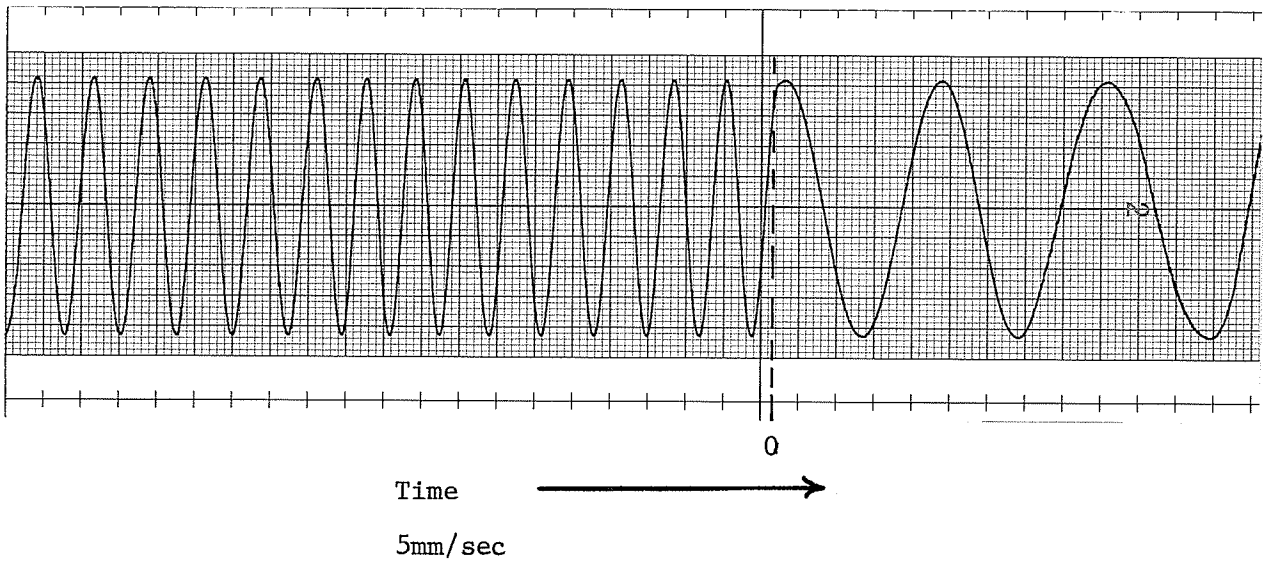


Fig.(4.3) Observed Signal

the effect on observed frequency and waveform will be investigated. Let the source be placed on the Y axis, at a distance d_1 from the origin 0, as shown in Fig. (4.4a) The variable time delay is given by

$$\tau(t) = \frac{1}{c}\sqrt{(d_o - vt)^2 + d_1^2}$$

$$= \sqrt{(\tau_o - mt)^2 + \tau_1^2} \qquad (4.8)$$

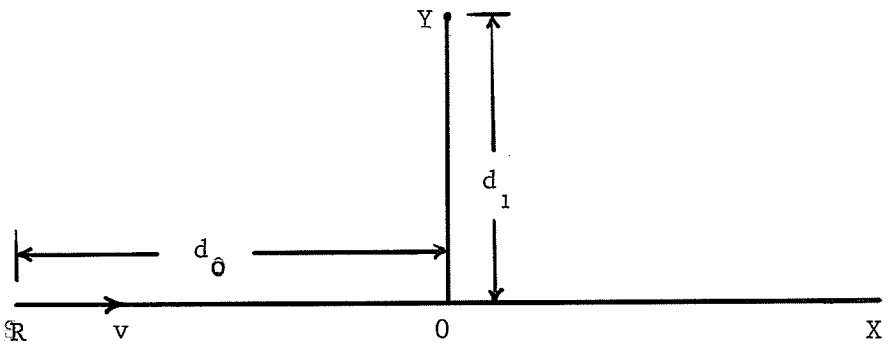
The Fig.(4.4b) represents the simulation diagram for the variable time delay, expressed by the Eq.(4.8). Assuming, $m = 0.5$, $\tau_o = 9$ sec., $\tau_1 = 4$ sec. and $f_s = 2$Hz, the experiment was performed and the observed signal was recorded using a strip chart recorder. The observed signal is found to have a sinusoidal waveshape with continously varying time period. It is as if the observed frequency is shifting continously. This frequency is plotted in Fig. (4.5).

4.2 FLOW RATE OF SOLIDS

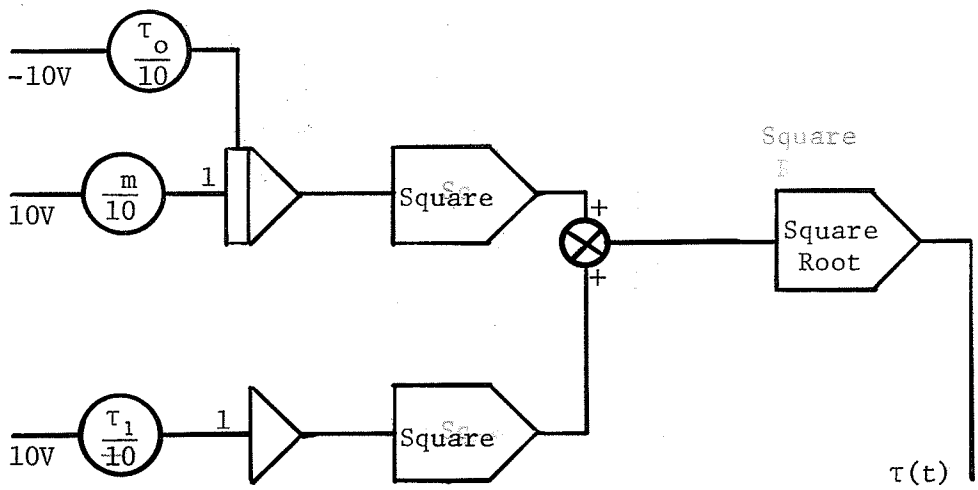
A recently proposed system for controlling the flow rate of dry solids [5] involves a controlled (variable) delay. In the proposed system, shown in Fig.(4.6), speed is controlled to maintain the desired flow rate. The authors have assumed a constant delay, but the following analysis shows that the assumption of a variable delay is significantly more accurate.

4.2.1 Weighbelt Analysis

The weighbelt consists of three sections: The front section d_1, the weighing section d_2 and the tail section d_3. The extent of the weighing section is generally determined by the two idlers closest to



(a) Observer Position



(b) Simulation of $\tau(t)$

Fig.(4.4) An Extension

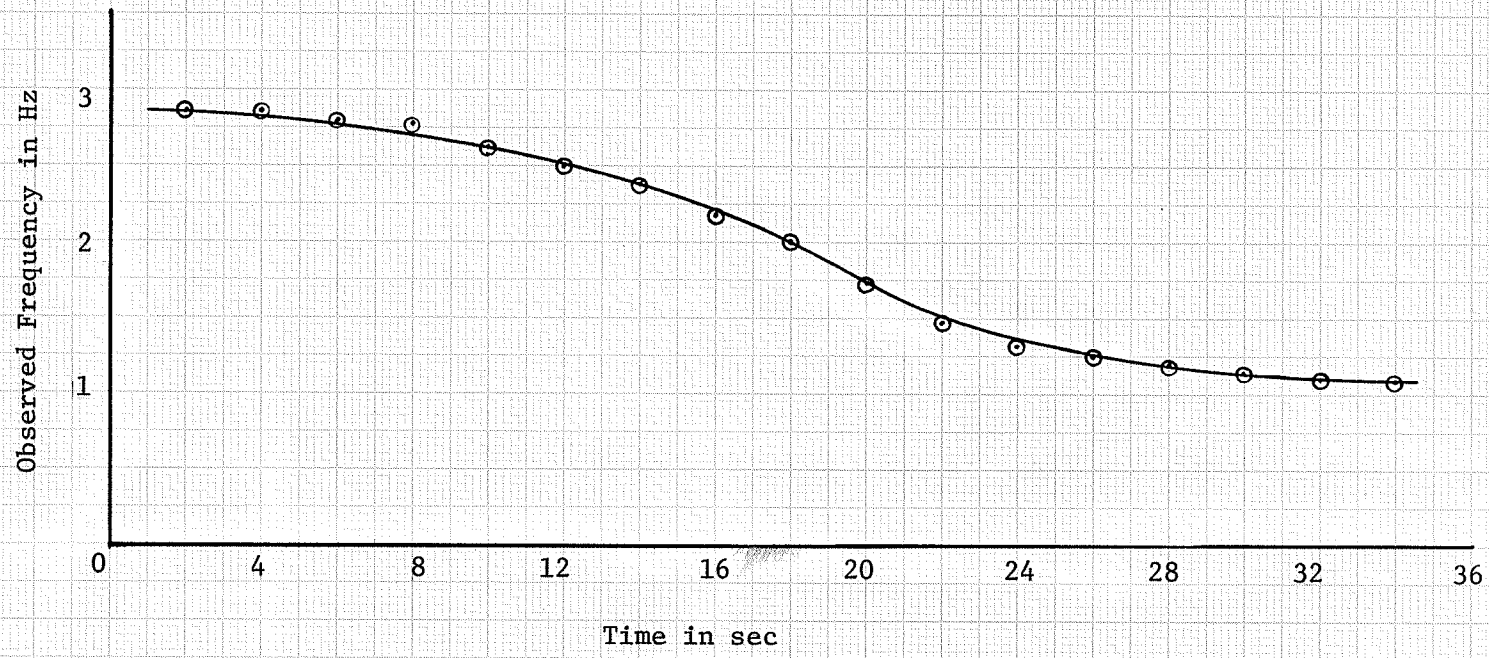


Fig.(4.5) Frequency Plot

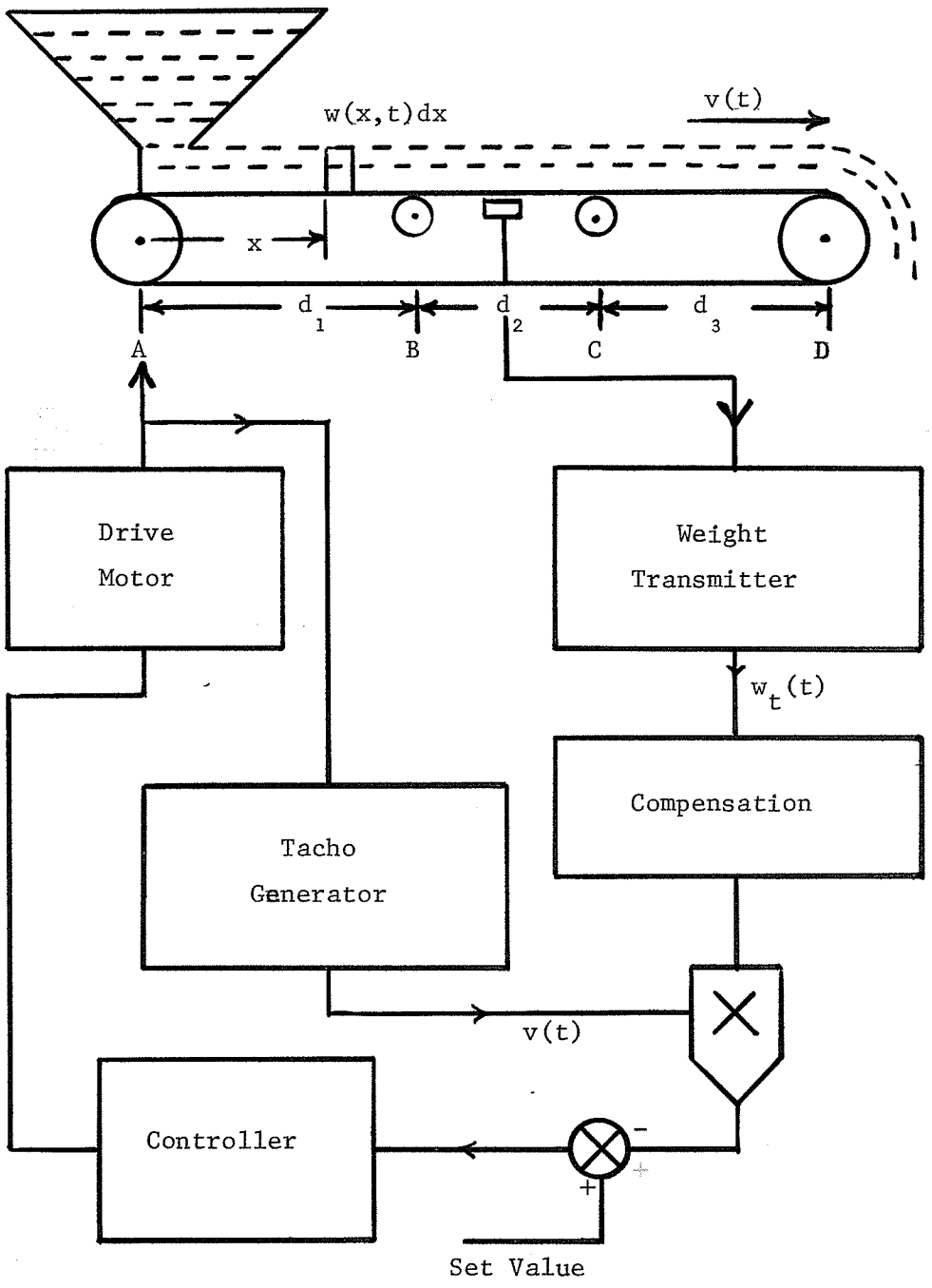


Fig.(4.6) Belt Speed Controlled Feeder

the weight-sensor. Let $w(x,t)$ be the belt loading in lbs/ft evaluated at a distance x from A and at time t, and $v(t)$ be the belt speed. Therefore, the flow rate

$$c(t) = w(x,t)\, v(t) \tag{4.9}$$

Generally the required steady state is specified by

$$w(x,t) = w_s \text{ , a constant and}$$

$$v(t) = v_s \text{ , a constant and}$$

$$c_s(t) = w_s v_s \tag{4.10}$$

When a disturbance is introduced by the belt loading, the controller alters the belt speed to maintain the desired $c_s(t)$.

Since there is no control action on the belt loading, B may be taken as the origin. Assuming $d_1 = 0$, the input flow rate

$$c_i(t) = w(0,t)\, v(t) \tag{4.11}$$

The output flow rate is given by

$$c_o(t) = w(x_d,t)\, v(t) \tag{4.12}$$

or

$$c_o(t) = w(0, t-\tau(t))\, v(t) \tag{4.12}$$

where $\tau(t)$ is the variable time delay, given implicitly by the relation

$$d_2 + d_3 = \int_{t-\tau(t)}^{t} v(\xi)\, d\xi \tag{4.13}$$

Since the left hand side of this equation is a constant, differentiation of both sides produces

$$\dot{\tau}(t) = -\frac{v(t) - v(t-\tau(t))}{v(t-\tau(t))}$$

or

$$\dot{\tau}(t) = 1 - \frac{v(t)}{v(t-\tau(t))} \tag{4.14}$$

4.2.2 Weighing Device

Generally, the system performance is investigated by applying a step input disturbance. The weighing device can be modelled by analysing its response due to a step input disturbance w_d in the belt loading. A platform type scale will be considered as the weighing device. For this type, the weight transmitter signal is proportional to the total load on the weighing section [4]. The total load on the weighing section [Fig.(4.7)] is given by

$$W(x) = w_d x \qquad \text{for} \qquad o < x \leq d_2 \tag{4.15}$$

and

$$W(x) = w_d d_2 \qquad \text{for} \qquad x > d_2 \tag{4.16}$$

where x is related to t by the relation

$$x = \int_0^t v(\xi)\, d\xi \tag{4.17}$$

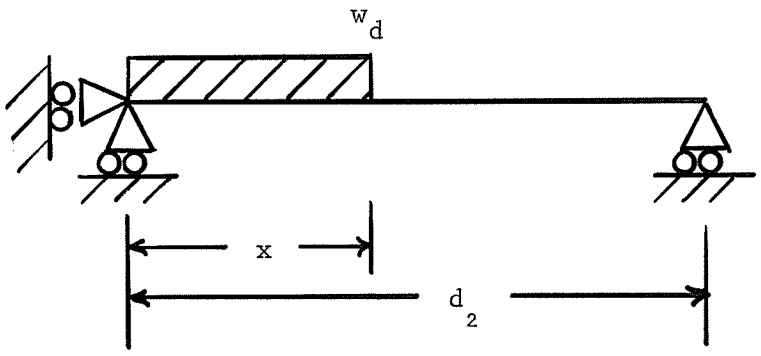
Therefore, the weight transmitter signal,

$$w_t(t) = \frac{W(x)}{d_2} + w \tag{4.18}$$

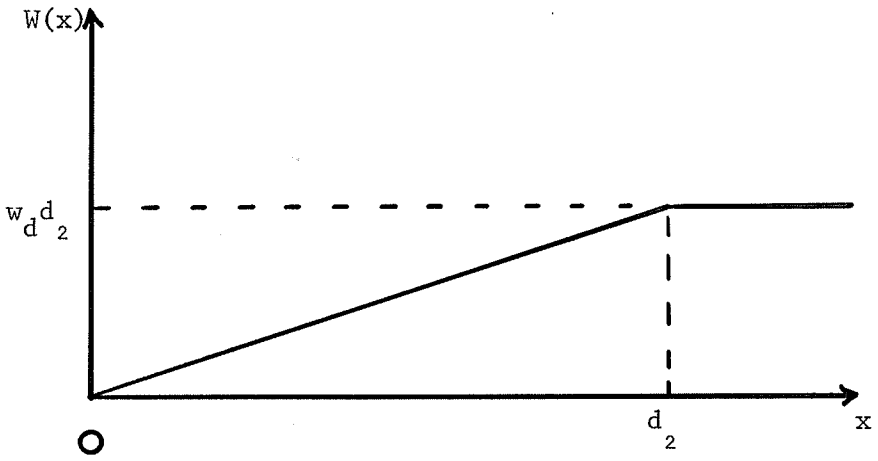
4.2.3 Simulation

The belt feeder system contains a variable time delay as indicated in the Eq.(4.12). The feeder block diagram is shown in Fig.(4.8). The weight transmitter is simulated by using equations (4.15-4.18), and is shown in Fig.(4.9). Eq.(4.14) is used in computing the $\dot{\tau}(t)$ which upon integration yields $\tau(t)$. Fig.(4.10) illustrates the variable time delay simulation technique. In this example, both channels of the System/7 must be used: channel 1 for simulating the delayed belt loading, $w(t-\tau(t))$, and channel 2 for the delayed belt speed, $v(t-\tau(t))$.

The feeder parameters chosen for this experiment are given in tabulated form as follows:



(a) Platform Type Scale



(b) Total Load Response

Fig.(4.7) Weighing Device

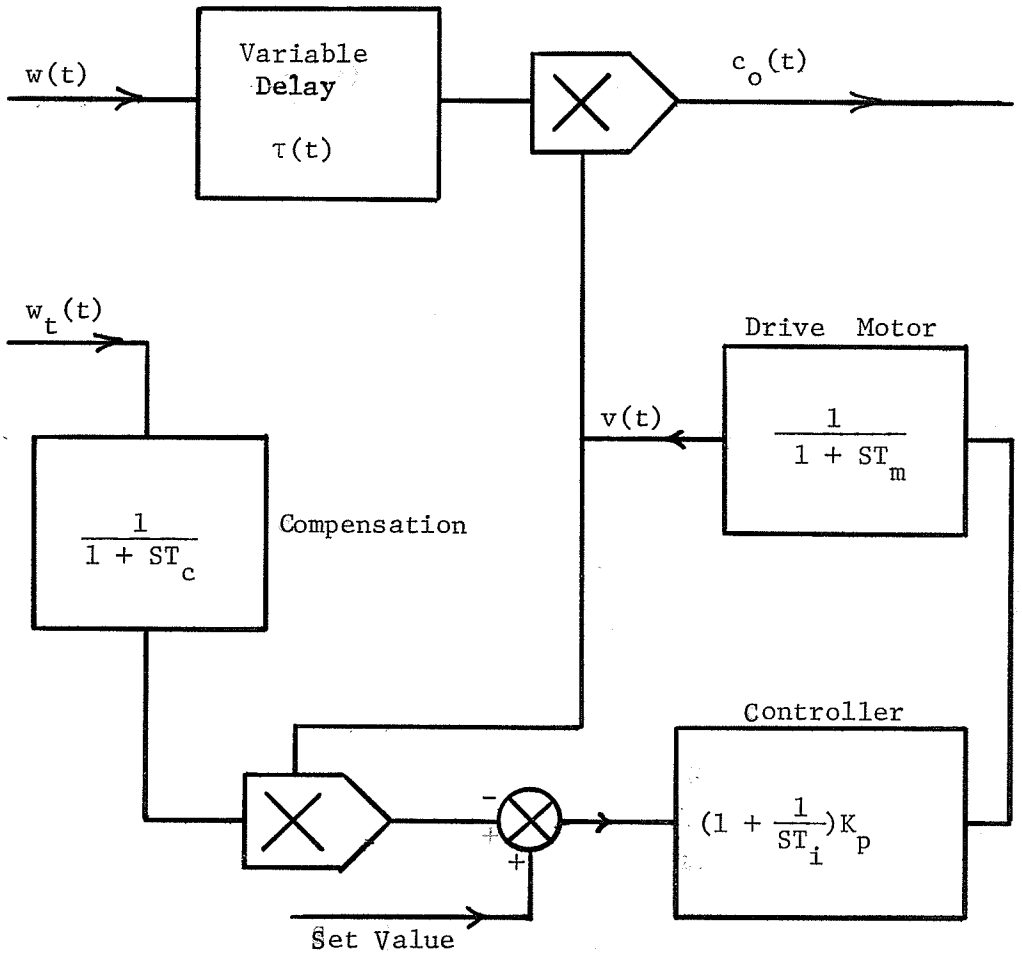
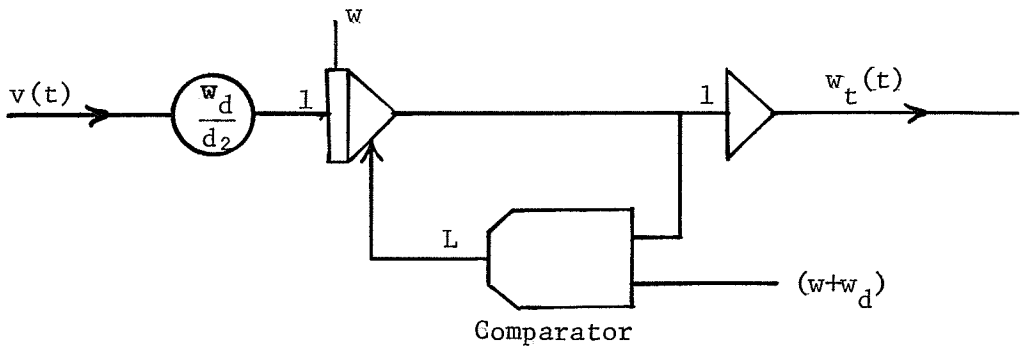


Fig.(4.8) Feeder Block Diagram



Integrator with mode control

Operate when L = 1
Hold when L = 0

Fig.(4.9) Weight Transmitter Simulation

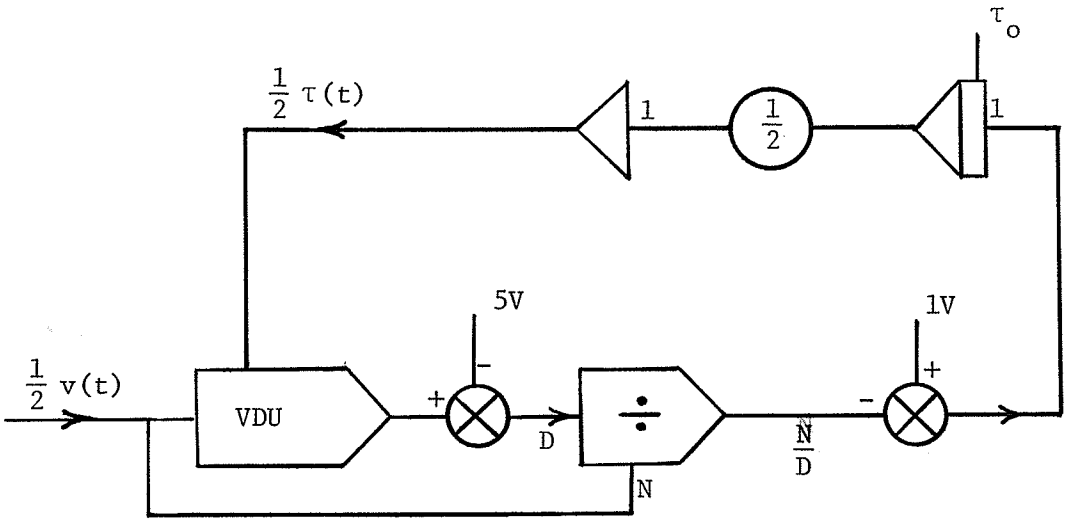


Fig.(4.10) Variable Time Delay Simulation

	Belt feeder parameters	values
K_p	Proportional gain	0.20
T_i	Integral time, sec	0.25
T_c	Compensation time constant	
T_m	Drive motor time constant, sec	0.10
d_2	Length of weighing section, ft	3.00
d_3	Length of tail section, ft	15.00
w	Belt loading, lb/ft	2.00
v	Belt speed, ft/sec	3.00
c	Feed rate, lb/sec	6.00
T_o	Dead time from weigh platform to end of belt, sec	6.00

The performance criteria for the belt feeder system chosen are (i) the recovery time t_r and (ii) the net error I . The recovery time is taken as the time required by the output flow rate $c_o(t)$ to return to within ± 1% of the steady state flow rate. Defining,

$$e(t) = c_o(t) - c_s(t) \tag{4.19}$$

the integral

$$I = \int_0^{t_r} e(t)\, dt \tag{4.20}$$

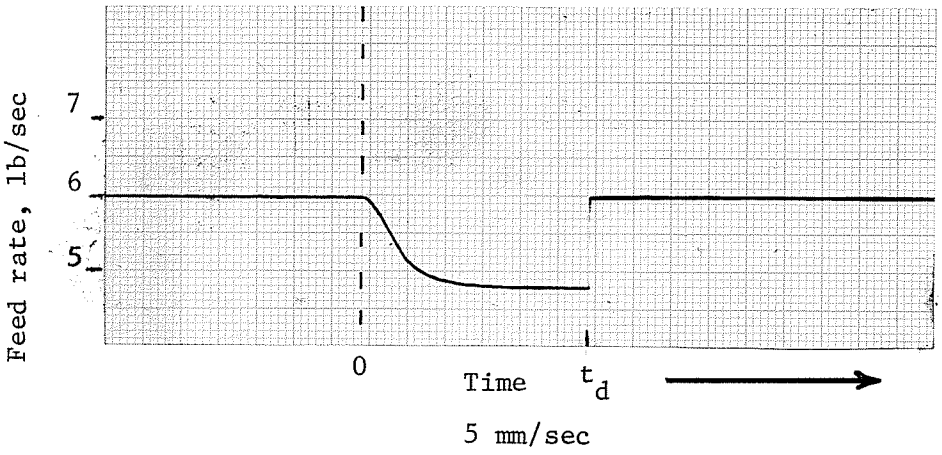
gives the net error in pounds.

The system performance was investigated by applying ± 25% disturbance in belt loading $w(t)$. The effect of introducing a compensation network was also considered.

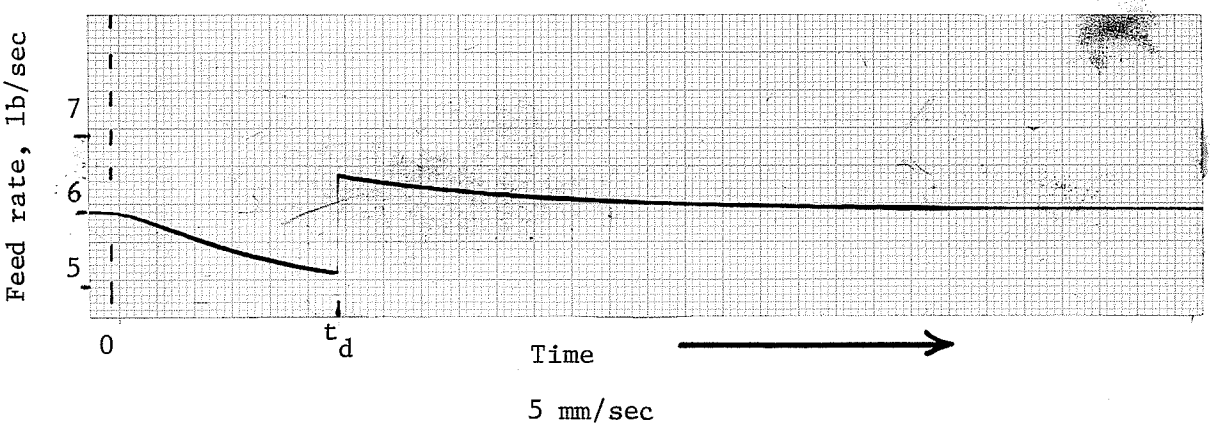
4.2.4 Experimental Results

Observation no.	Belt loading disturbance, percent	Compensation time constant T_c, sec	Net error, lbs	Recovery time, sec
1	25	None	-7.68	7.2
2	-25	None	6.90	4.7
3	25	5.56	0.13	13.0
4	-25	5.56	1.95	13.8

The strip chart recordings of $c_o(t)$ for the observation no.1 and 3 are shown in Fig.(4.11). With no compensation the recovery time is minimum although the net error is large. The net error decreases and the recovery time increases when a compensation network is introduced. The compensation considered is a single lag network with time constant T_c. When T_c = 5.56 seconds, the minimum net error is obtained with positive disturbance. Another compensation scheme consisting of two lag networks was also considered and the net error was minimized. The recovery time in this case was found greater than the previous one (single lag network).



Observation number 1



Observation number 3

The jump at the time, t_d, corresponds to the time at which the step disturbance reaches the end of the conveyor belt, D [Fig. (4.6)].

Fig.(4.11) Response Curves

CHAPTER V

CONCLUSIONS

When the analog signal is digitized some error is involved. The digital output of the A/D converter represents the input analog voltage at some instant during the conversion time. The rapidly changing signal may degrade the accuracy of conversion. This places a bandwidth limitation on the input signal. If the input is a sine wave ($E_m \sin 2\pi ft$), a maximum allowable error of q volts is reached at

$$f = \frac{q}{2\pi E_m \Delta T}$$

where ΔT is the conversion time [12]. For example, if q is 0.1% of E_m and ΔT = 20 microsecond, f is equal to 8 Hz.

For full 14 bit A/D conversion the System/7 limits the spectrum of the analog input to 30 Hz. Since, however, the analog accuracy need not exceed approximately 0.1% only 10 bits are necessary. If this degradation is allowed then the spectrum may be extended significantly so that normal repetitive operation of analog computer plus VDU (variable Delay Unit) is satisfactory.

Thus the limitation on input signal spectrum is due to the sampling "window" length rather than the sampling frequency which may be as high as 20,000 samples per second.

Processes containing time delays have been investigated in Chapter III and IV. The close agreement between the analytical and the experimental results indicates very satisfactory performance of the VDU. In conclusion, a process containing a variable delay

can now be simulated easily using this VDU and its behavior can be investigated. Full details on the program and operation of the simulator may be found in reference 13.

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