A
HIGH VOLTAGE DIRECT CURRENT TRANSMISSION SYSTEM WAVEFORM SIMULATOR

A THESIS PRESENTED TO
THE FACULTY OF GRADUATE STUDIES
AND RESEARCH
THE UNIVERSITY OF MANITOBA

In partial fulfillment
of the requirements for the
degree of Master of Science
in
Electrical Engineering

by
F.T. Shinyei
May 1969

c1969

ACKNOWLEDGEMENT

The author wishes to express his thanks to Professor M.Z. Tarnawecky, the technical staff of the University of Manitoba, and the National Research Council of Canada for their practical and financial assistance during the preparation of this thesis.

Table of Contents

List of Figures and Plates

ABSTRACT

For the purpose of illustrating the conversion principles involved in the transmission of high voltage direct current a model composed entirely of electronic solid state devices has been constructed. The four major subsystems comprising the complete model are:

1. The pulse circuits which fire the thyristor bridges
2. The rectifier bridge
3. The inverter bridge
4. The transmission line

An attempt has been made to simulate the voltage and current waveforms occurring in the actual system as closely as possible.

INTRODUCTION

The growing acceptance of high voltage direct current (hvdc) transmission for power transfer has made imperative the basic understanding of the conversion principles involved. In the field of alternating current (ac) power systems operational models such as network analyzers have proven their usefulness. Although schemes have been developed whereby the ac models can be adapted for hvdc simulation, the true hvdc simulator is not as readily available.

The purpose of this project is to present a model employing solid state electronic devices which performs the conversion operations vital to the hvdc transmission scheme, namely rectification and inversion. A description of some aspects of rectification and inversion has been included with the chapters dealing with the rectifier and inverter bridges. Appendix A will also be useful in understanding hvdc valves.

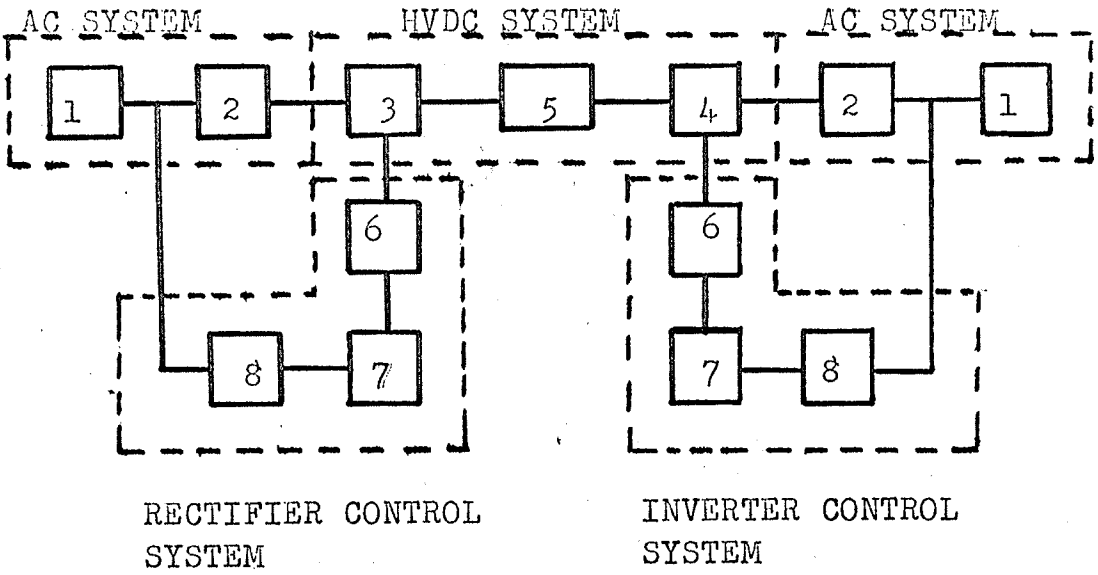
Both rectification (the conversion from alternating current to direct current) and inversion (the conversion from direct current to alternating current) rely heavily upon the adequacy of the pulse circuit which fires the valves in the bridges. Experience in the full scale power system has shown that pulses of 120^{o} duration are the most desirable because they have proven their reliability and efficiency. This statement will be explained in Chapter 3.

The model has been patterned with this fact in mind.

The transmission line is that subsystem which conveys the direct current from the rectifier to the inverter.

The block diagram shown in Figure I.1 illustrates the general layout of the model system.

Appendices have been included to aid in the understanding of hvdc transmission and the model.



1. 3ϕ variacs, associated transformers, and loads
2. current limiting resistors and additional winding reactance
3. rectifier bridge
4. inverter bridge
5. transmission line
6. pulse circuits
7. isolating transformers
8. phase shifters

Figure I.1 Block diagram of model system

CHAPTER 1

The Rectifier Bridge

Rectification, the conversion of alternating current to direct current, will be analyzed briefly. The assembled model will then be presented.

Since the model employs thyristors all drawings of bridges will indicate these. Rectifier operation is discussed and extended to inverter performance in Chapter 2.

Consider the standard full wave three phase bridge configuration having six controlled legs and supplied from an ac source. Refer to Figure 1.1.

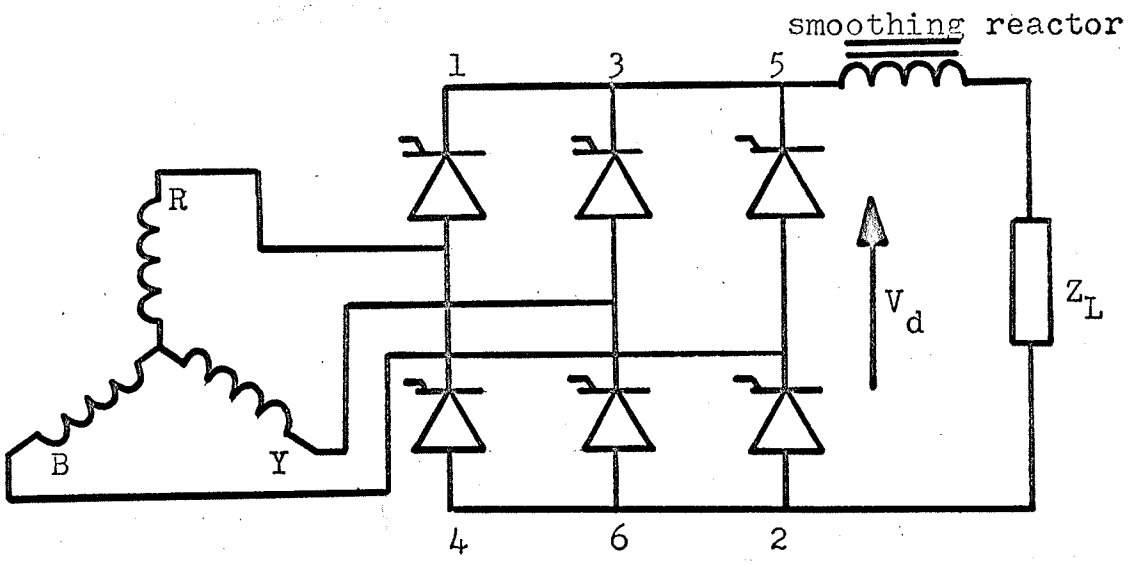


Figure 1.1 Rectifier Bridge

The load may be either passive or a variable voltage source as would be the case when an inverter is connected

to the output of the rectifier. The need for the smoothing reactor is explained later.

It is assumed that a suitable circuit exists which generates properly sequenced pulses which can be phase shifted from 0^{o} to 180^{o}. The amount of phase shift is referred to as the delay angle since it is the angle by which the firing of the valve is delayed. The following remarks will clarify this. It is instructive to examine the three phase voltage waveforms. See Figure 1.2 which is drawn for a delay angle (a) of zero degrees.

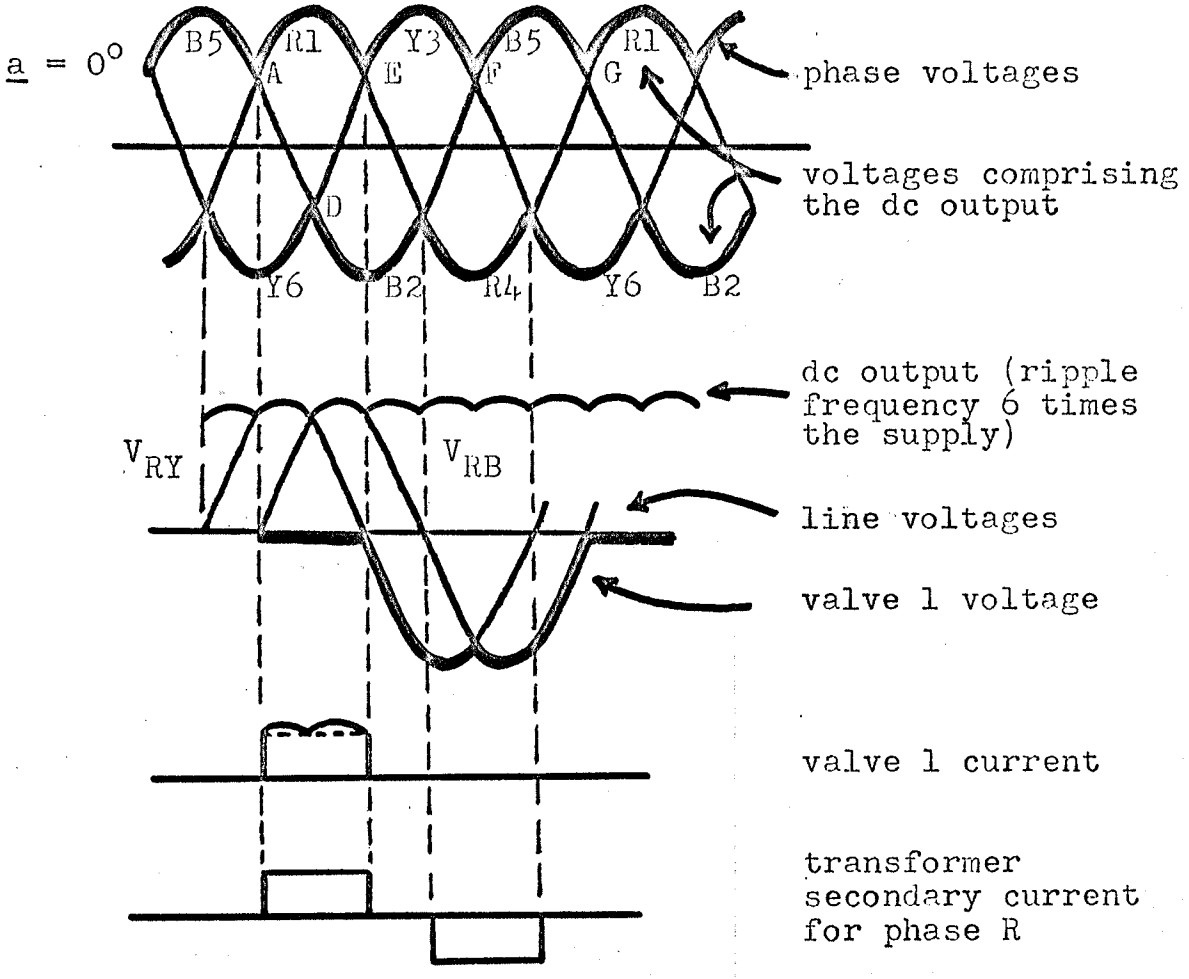


Figure 1.2 Rectifier waveforms for a = 0^{o}

Any one valve will conduct for the intervals indicated. Also one valve will conduct with two valves during its 120^{o} conduction period. Consider point A when valve 1 is conducting with valve 6. Since the valve voltages are practically zero the load voltage becomes a portion of the positive half cycle of the line voltage V_{RY}. At point D the load voltage becomes V_{RB} since valve 2 begins conduction. For the situation stated here a valve will cease conduction if its anode to cathode voltage is made negative. Consider valve 1. When it conducts, its voltage is virtually zero. At point E a positive line voltage V_{YB} exists between the anode and cathode of valve 3 since valve 2 is still conducting. When the firing pulse is received valve 3 begins conduction thereby placing the cathode of valve 1 at the voltage of phase Y. Hence the anode (phase R) is at a lower potential than the cathode (phase Y) and valve 1 turns off. This corresponds to the negative half cycle of the line voltage V_{RY}. The valve voltage follows V_{RY} up to point F whereat valve 5 fires and the cathode potential of of valve 1 becomes that of phase B. Since the anode to cathode voltage is still negative valve 1 remains in the off state. Hence the valve voltage transfers to the line voltage V_{RB}. At point G valve 1 fires and the cycle repeats.

It is obvious from Figure 1.2 that the dc ripple will be six times the frequency of the 3ϕ input voltage. A further observation is that the duration of conduction through one valve is 120^{o}.

Now consider the case when delay is added. See Figure 1.3 drawn for $\underline{a} > 60^{\circ}$. It is apparent that the dc output

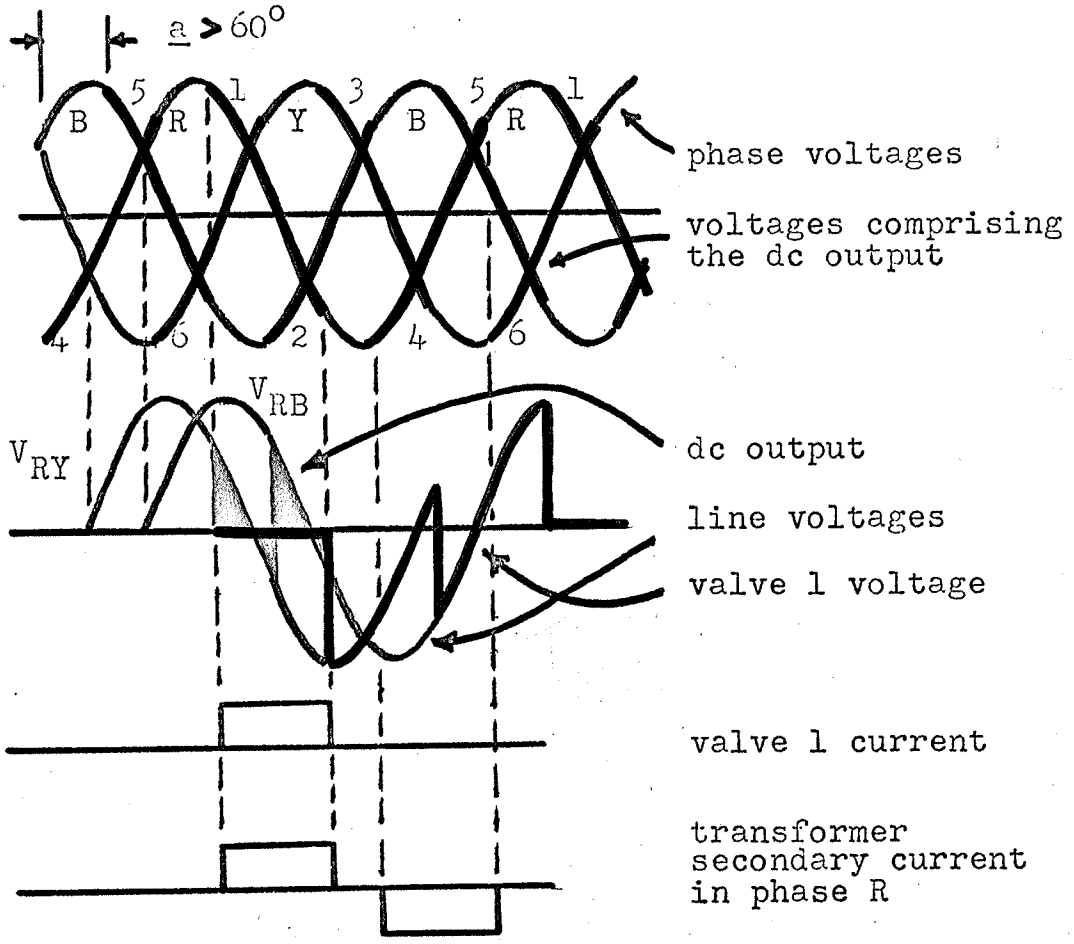


Figure 1.3 Rectifier waveforms for $\underline{a} > 60^{\circ}$

voltage will be much less than that at zero delay angle. Furthermore a portion of the voltage is negative when the anode voltage of valve 1 falls below that of the cathode of valve 6. This occurs when $\underline{a}$ exceeds 60°. If the load were purely resistive the negative portion of the dc output would not appear since conduction would not be pos-

sible due to the negative anode to cathode voltage. However, if the reactor shown in Figure 1.1 is included it has the effect of maintaining current flow against the negative voltage due to its stored energy. If it is of sufficient size it will permit continuity of operation. This condition will be achievable up to $\underline{a} = 90^{o}$ whereat the net output will be zero. This may be evidenced from Figure 1.3 by observing that when $\underline{a} = 90^{o}$ the volt-degree areas above and below the zero line are equal.

The bridge arrangement used in the model is shown in Appendix B. Line to line voltage is impressed across any two valves which conduct simultaneously. Thus the pulses can be applied between 0^{o} and 180^{o} of line voltage. For rectifier operation the range is 0^{o} to 90^{o} since at the upper limit the dc output voltage is zero.

To guard against excessive currents through the thyristors in the event of failure of the bridge, resistances were placed in series with the variac windings. The thyristors employed were low voltage (25 v) and low current (1.6 amp rms) types with a very high gate sensitivity. The maximum gate current required to fire them is 200 microamps. The necessity for these is explained in Chapter 3. Additional winding reactance in the variac was required since the commutation voltage dents were not of sufficient width to be readily observable. Commutation voltage dents are explained in Appendix D. A value of 60 mh. was found adequate.

Because of the high gate sensitivity of the thyristors, a negative gate bias of 1.5 volts was incorporated to prevent spurious firing when the valves were not conducting. See Figure 1.4. The negative portion of the pulse transformer output was not utilized as a bias since it decayed in less than 240^{o}, the required blocking duration, and since its peak amplitude might have damaged the sensitive gates. This is further explained in Chapter 3.

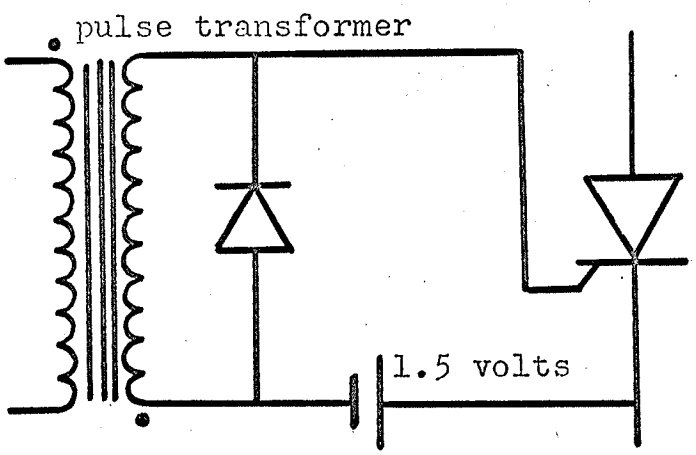
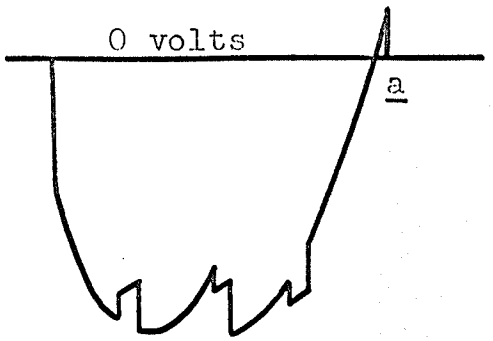
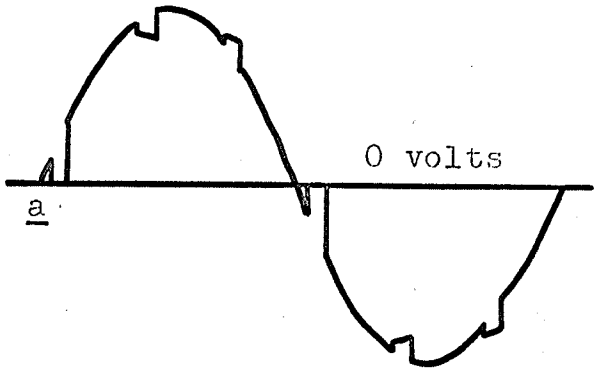


Figure 1.4 Thyristor gate bias arrangement

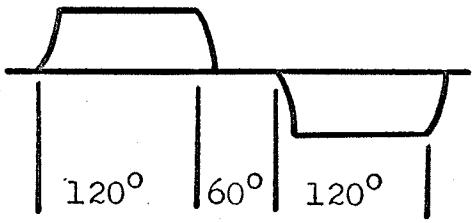
The various theoretical waveforms which arise from rectifier operation are illustrated in Figure 1.5. Photographs of the waveforms obtained from the model are shown in Plate 1.



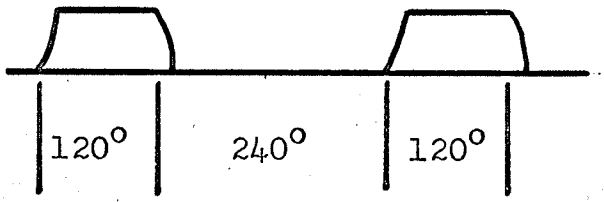
valve voltage with delay



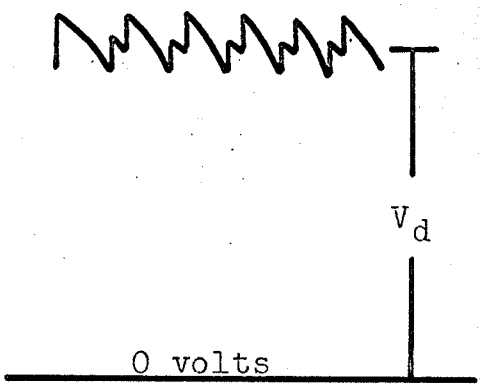
transformer secondary line voltage with delay



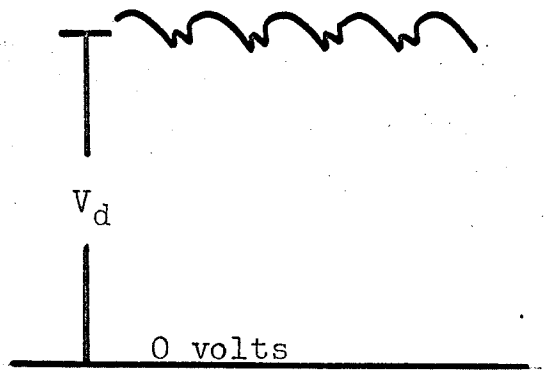
transformer secondary current



valve current

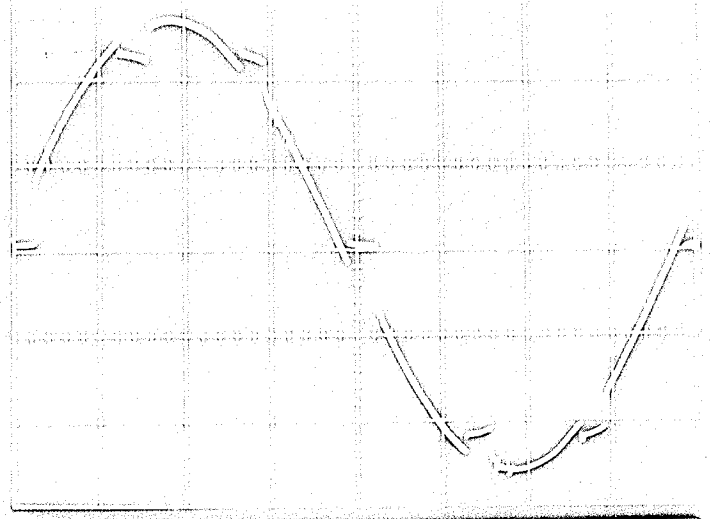


dc voltage with 30° delay

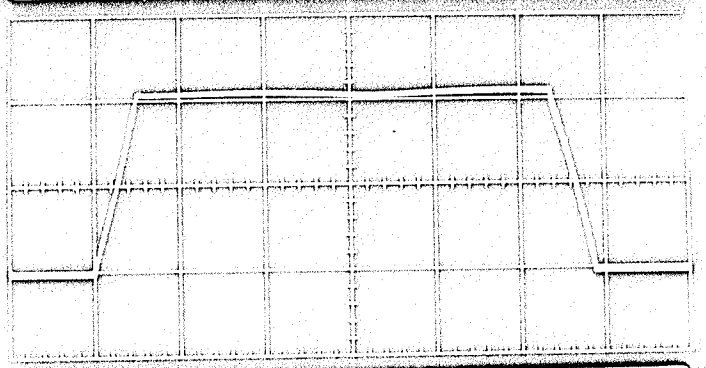


dc voltage with a delay

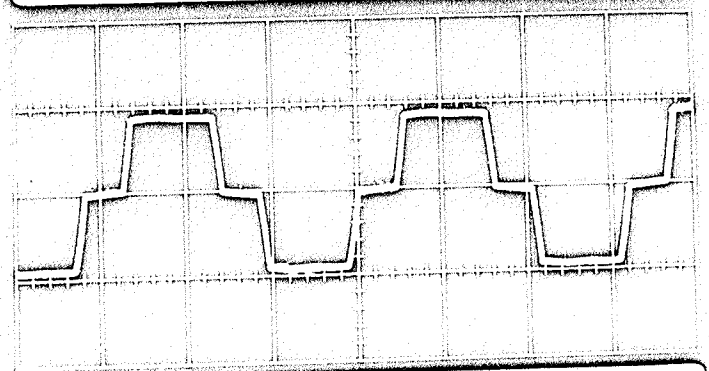
Figure 1.5 Theoretical rectifier waveforms



transformer secondary line voltage with delay



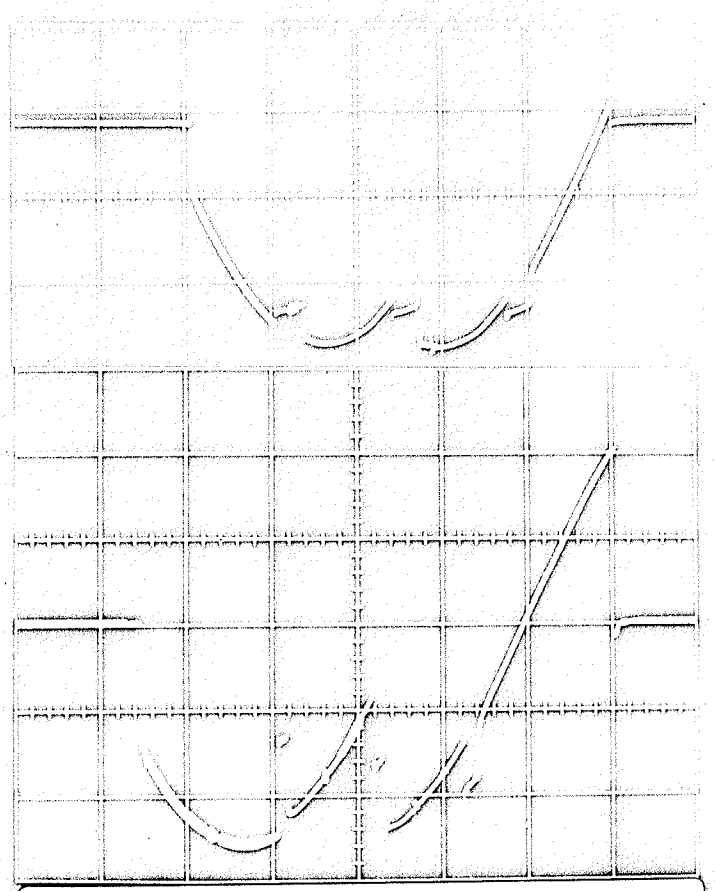
valve current



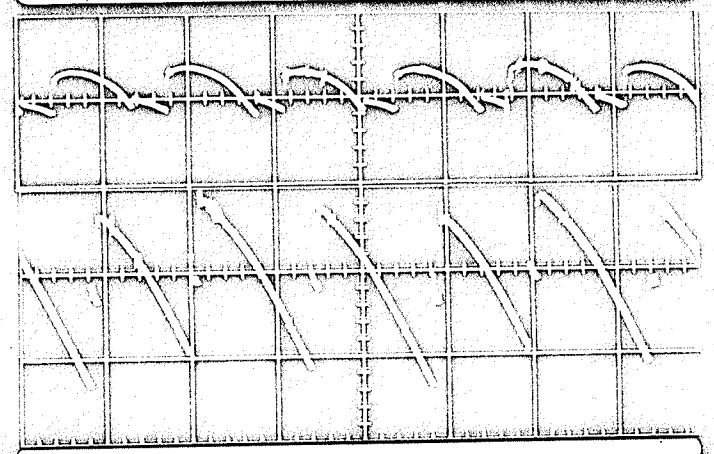
transformer secondary current

PLATE 1

rectifier waveforms



valve voltage - small delay
valve voltage - 30° delay



dc voltage - small delay
dc voltage - 30° delay

PLATE 1

(con't)

CHAPTER 2

The Inverter Bridge

Inversion as an extension of rectifier operation is explained and the constructed model presented. Commutation failure, the major fault in inverters, is also examined.

As mentioned in Chapter 1, the rectifier functions up to 90° delay angle. Past this point a voltage negative with respect to the previously defined rectifier output voltage will exist only if a dc source of sufficient magnitude is connected as a "load" which can force current through the valves against the negative voltage which prevails for $\underline{a} > 90^{\circ}$. See Figure 2.1 and Figure 2.2 which is drawn for $\underline{a} \approx 170^{\circ}$.

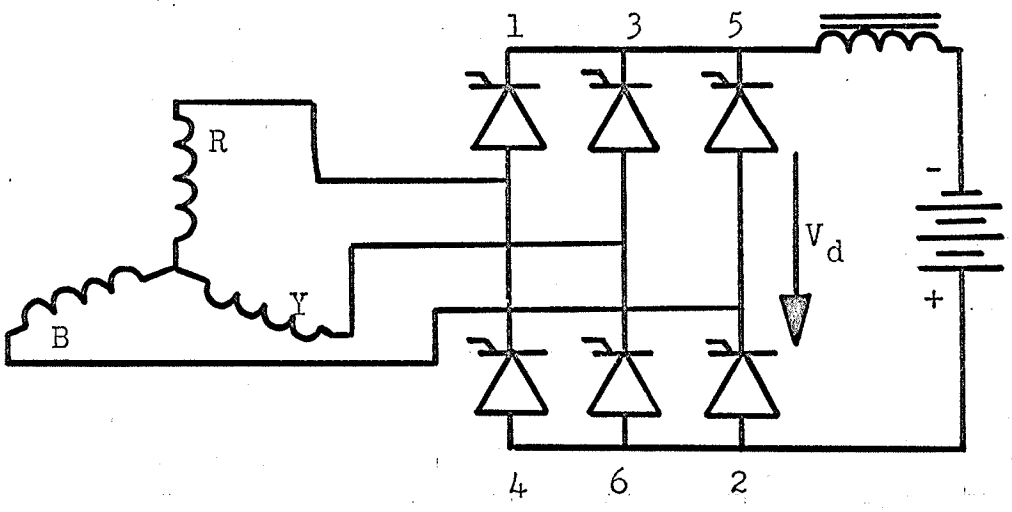


Figure 2.1 Inverter operation

This operation is exactly that of an inverter. The small

angle of negative voltage in the valve voltage waveform must be present to return the valve to the blocking state and thereby regain control. This angle is called the de-ionization angle (d). Obviously gate control is imperative for inverter operation since the voltage on a valve is positive for 240° and conduction must be prevented in most of this region.

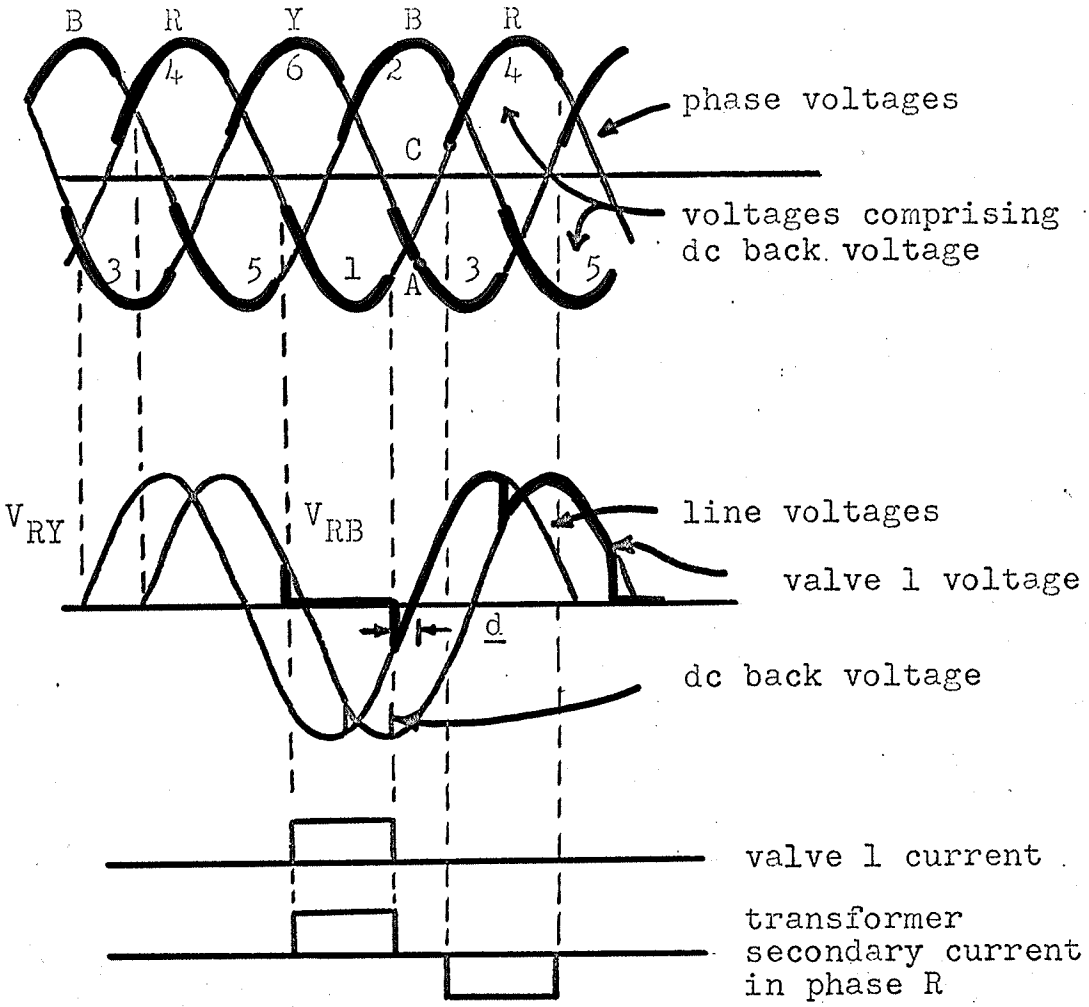


Figure 2.2 Inverter waveforms for $\underline{a} \approx 170^{\circ}$

It should be noted that the valve fires when its anode to cathode voltage is positive and that the source forces current when this voltage becomes negative. A thyristor could never fire when its anode to cathode voltage was negative.

The firing pulses must be timed accurately otherwise commutation (the transfer of conduction from valve to valve in the proper sequence) will not occur correctly. Commutation failure is the most severe and most common type of inverter fault. It occurs primarily due to failure of the pulse circuit which fires the valves or to a decrease in one of the phase voltages supplying the inverter. The effect of the latter is to reduce the available deionization angle to a point where the reduced voltage is insufficient to clear the charge carriers from the conducting zones of the thyristor. It continues conduction with the same valve until a commutation occurs which short circuits the transformer windings. Hence no current is supplied to the ac load.

As a more detailed explanation consider the former cause in which the pulse to valve 3 is not received until point A in Figure 2.2. As a result valve 1 continues because its anode to cathode voltage is now positive. Valve 3 turns off since its anode (phase Y) is more negative than its cathode (phase R). This situation is maintained up to point C when valve 4 fires. Conduction through valves 1 and 4 constitutes a short circuit. A failure of

this type is known as a commutation failure. It rarely occurs in rectifiers because of the large angle of negative voltage on the valve.

The line reactors tend to average or smooth the current from the rectifier. Thus the current through the valves is a reasonably flat-topped pulse of 120^{o} duration. At any instant of time the current is obviously flowing into one transformer winding and out of another. Thus each winding sustains current flow in either direction depending upon which valve connected to it is conducting. The current waveforms are shown in the preceding illustrations. For the examples shown the winding current is due to conduction in valves 1 and 4 which are connected to phase R.

To further emphasize that inversion is simply an extension of rectifier operation the following derivation of the inverter equivalent circuit from that of the rectifier will be presented.

The foregoing analysis has been performed under the assumption that the transformer winding impedance is zero. This gives rise to an output before the smoothing reactor of

$$V_d = V_o \cos \underline{a}$$

where from a complete analysis V_o = 1.35 x the rms value of the line voltage.[1] Although the winding resistance is generally negligible, the voltage drop across the winding leakage reactance is of considerable magnitude. Figure 2.3

shows the general case with delay. Notice the volt-degree area shown shaded which represents the voltage drop due to winding reactance.

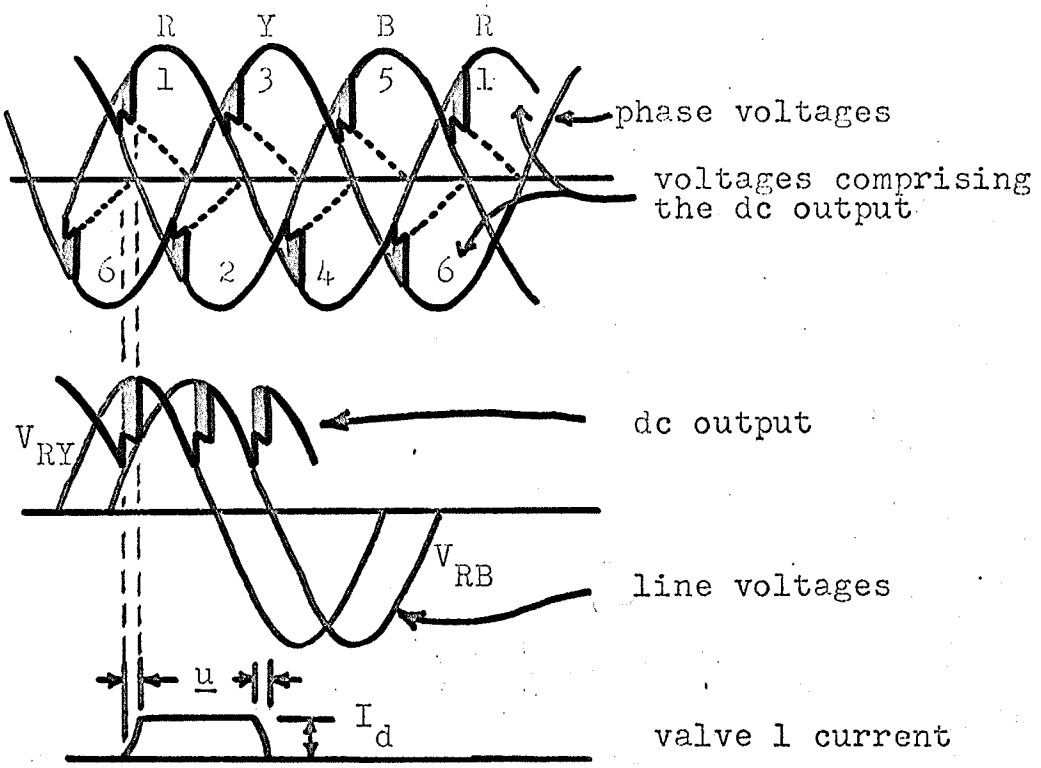


Figure 2.3 Effect of winding reactance

The conduction does not pass instantaneously from valve to valve because the winding inductance tends to maintain whatever current was flowing through it. Hence the valve current takes a finite number of degrees (u) to decay to zero or to build up to its final value, I_d. Since the next valve in the sequence fires during this interval a short circuit results between the two phases. The output voltage

follows the average value of the two phase voltages (shown by the dotted lines in Figure 2.3). This results in a drop in the output voltage determined from the volt-degree areas and the angle u. An equivalent non-dissipative resistance can be derived to account for this drop. A more rigorous analysis shows that the magnitude of this resistance is 3wL/3.14 where w is the supply frequency and wL is the sum of the transformer leakage reactance and the ac system reactance referred to the transformer secondary.[1*] When this is accounted for the output voltage before the smoothing reactor is

$$V_d = V_o \cos a - (3wL/3.14) I_d$$

A more detailed explanation of the effects of winding reactance can be found in Appendix D. This gives rise to the equivalent circuit shown in Figure 2.4.

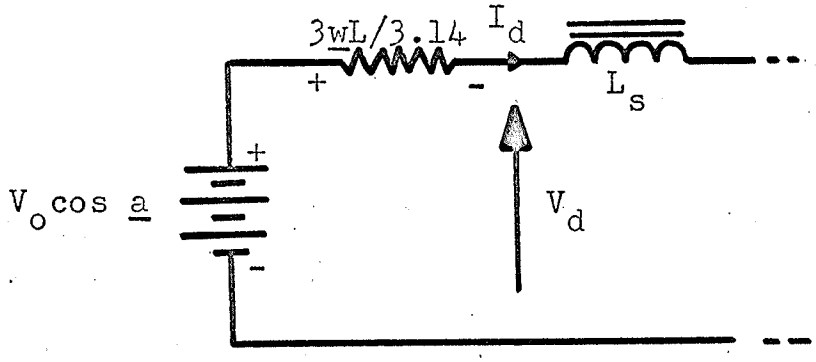


Figure 2.4 Rectifier Equivalent Circuit

* Note: Superscripts refer to references in the bibliography.

For $\underline{a}$ greater than 90° it is convenient to introduce the equivalence $\underline{a} = 180^{\circ} - \underline{B}$, where $\underline{B} = \underline{d} + \underline{u}$ as shown in Figure 2.5.

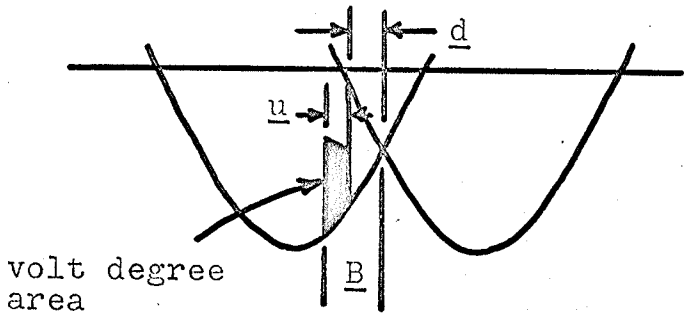


Figure 2.5 Angle $\underline{B}$

This results in the equation

$$V_d = V_o\cos(180^{\circ} - \underline{B}) - (3\underline{w}L/3.14)I_d$$

$$= V_o(\cos 180^{\circ}\cos\underline{B} + \sin 180^{\circ}\sin\underline{B}) - 3\underline{w}LI_d/3.14$$

$$= -(V_o\cos\underline{B} + 3\underline{w}LI_d/3.14)$$

An equivalent circuit for this equation is presented in Figure 2.6. A dc source has been included to drive current against the negative output voltage called the back voltage. If V_d is to be represented as a positive variable back voltage the bridge configuration is usually inverted which leads to the conventional equivalent circuit shown in Figure 2.7 where $V_d = V_o\cos\underline{B} + 3\underline{w}LI_d/3.14$.
A thorough analysis of rectifier and inverter operation is presented in references 1 and 7.

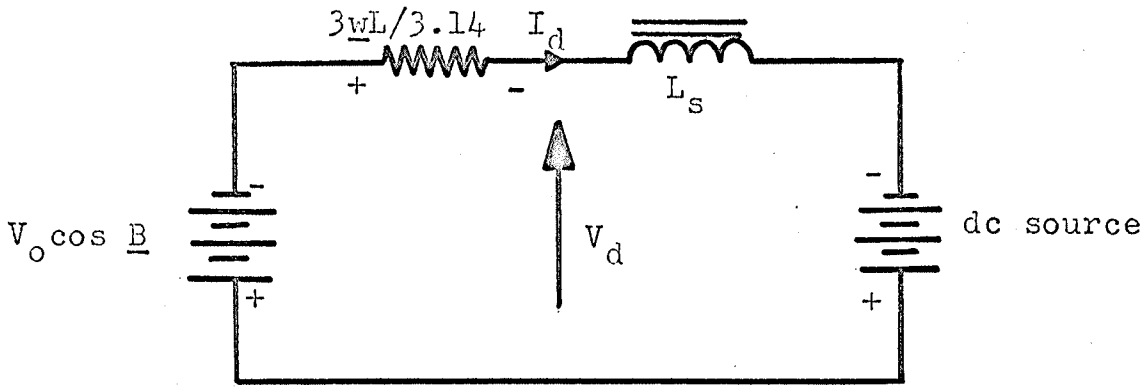


Figure 2.6 Inverter Equivalent Circuit

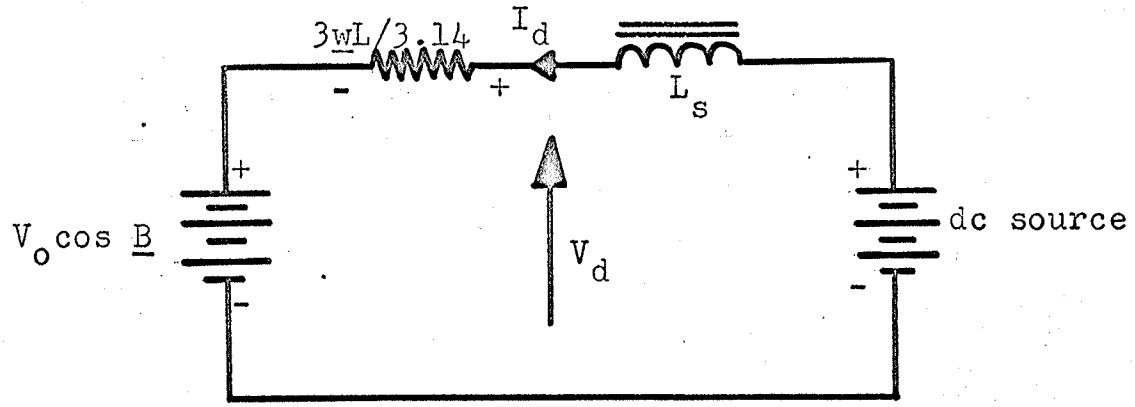


Figure 2.7 Conventional equivalent circuit

In summation several essential points should be noted.

1. Rectifier operation occurs for delay angles between 0^o and 90^o.
2. Inverter operation is an extension of rectifier operation for delay angles between 90^o and 180^o.
3. Smoothing inductors are necessary for rectifier oper-

ation to maintain current flow despite negative anode to cathode voltage (ie. to extend the valve conduction period into the region of negative voltage on the valve).

4. Similarly a dc source, the rectifier in this case, must be employed to force current against the inverter back voltage despite the negative anode to cathode voltage on the inverter valves for most of the conduction period.
5. Gate control is essential to inverter operation since during one cycle of 3ϕ voltage the valve must block for close to 240^{o} of positive anode to cathode voltage.
6. The inverter 3ϕ supply must be as reliable as possible and the control pulses to the valve gates must be timed accurately otherwise commutation failure will result.
7. For a fixed rectifier voltage the current I_d can be varied by altering the inverter back voltage. Similarly for a constant inverter back voltage I_d can be varied by changing the rectifier output voltage. This is the more conventional operating scheme. Most important is the fact that the rectifier dc voltage must never be allowed to fall below the combined inverter back voltage and transmission line voltage drop otherwise the the system will run down. This occurs since the current will not flow into the inverter under this situation.

9. Commutation in the inverter must be complete prior to the minimum deionization angle required to return the thyristor to its controllable state. If this does not happen commutation failure will result.
10. B can easily be thought of as the angle by which the transformer current at the inverter end leads the voltage. a can similarly be thought of as the angle by which the rectifier transformer current lags the voltage. This points out the fact that reactive power plays an important part in convertor operation.

Appendix B shows that the bridge configuration used is that illustrated in Figure 2.7. The rectifier replaces the dc source. From tests performed on the model system it was found that if the inverter were supplied through a transformer with a load placed on the primary the system functioned satisfactorily. See Figure 2.8.

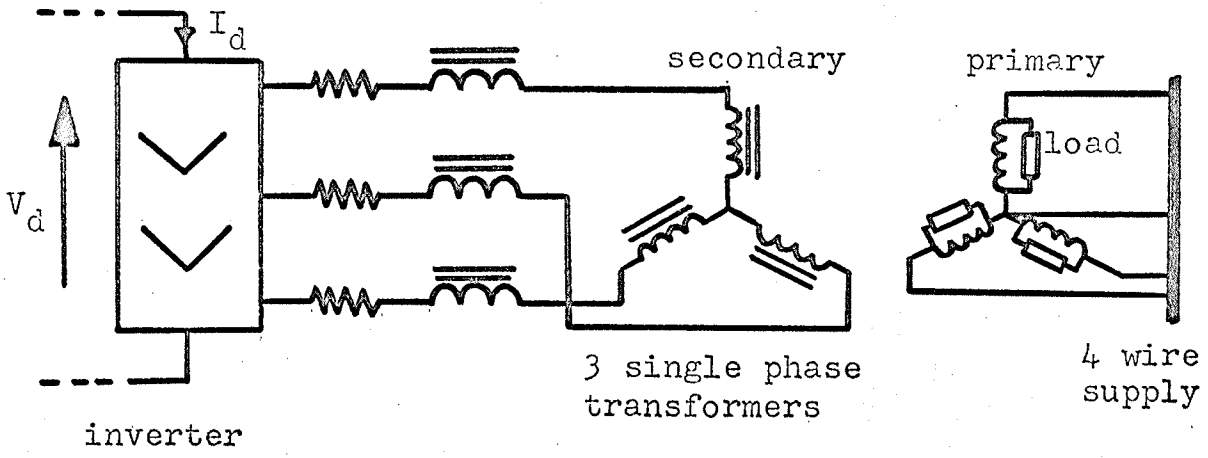


Figure 2.8 Inverter 3ϕ Supply

In this case the reactive power is supplied by the ac system. Various 4 wire supplies were examined. Their effects on system performance are discussed in detail in Chapter 5.

As mentioned previously the deionization angle is critical. However, the maximum phase shift attainable from the model left a large enough angle and the problem was eliminated. The components used in the inverter are the same as those of the rectifier and are mentioned in Chapter 1.

Theoretical waveforms are included in Figure 2.9. For the actual waveforms see Plate 2.

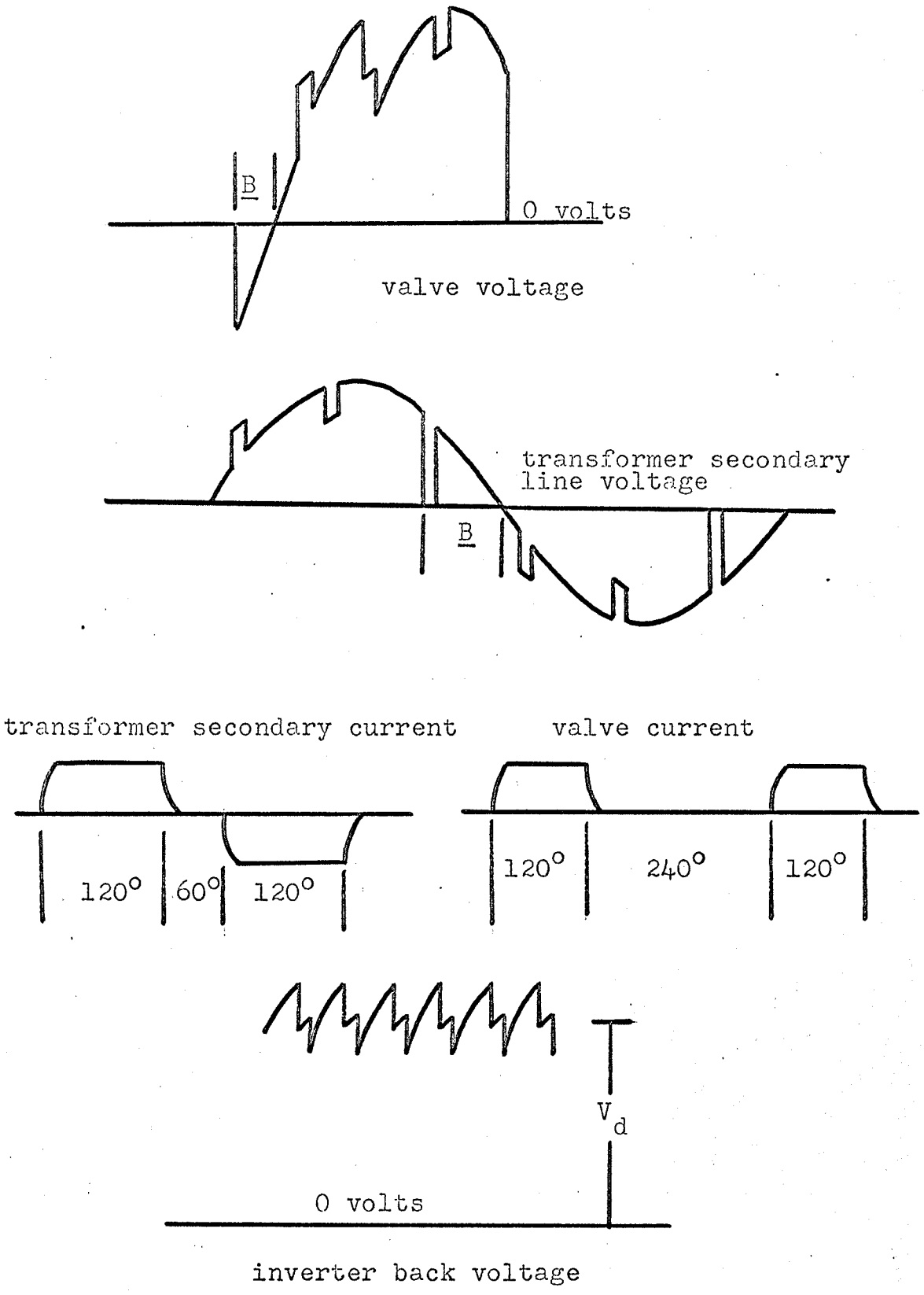
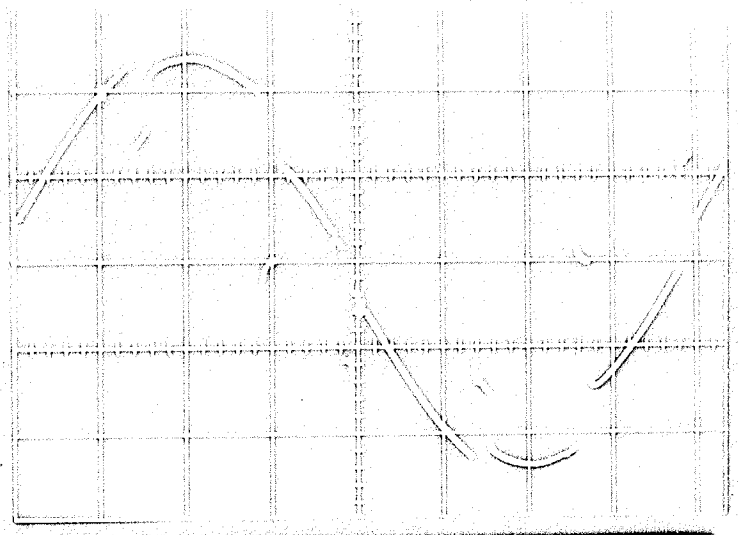
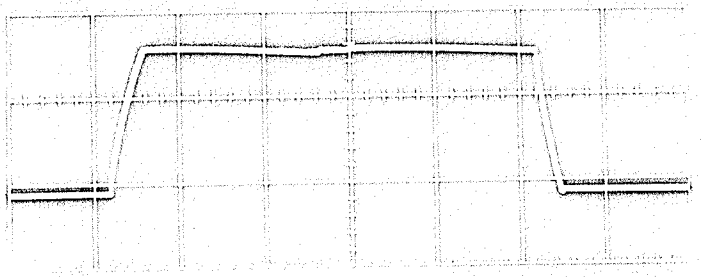


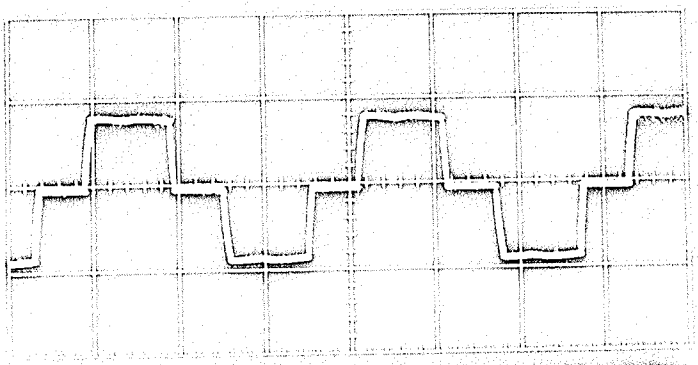
Figure 2.9 Theoretical inverter waveforms



transformer secondary line voltage



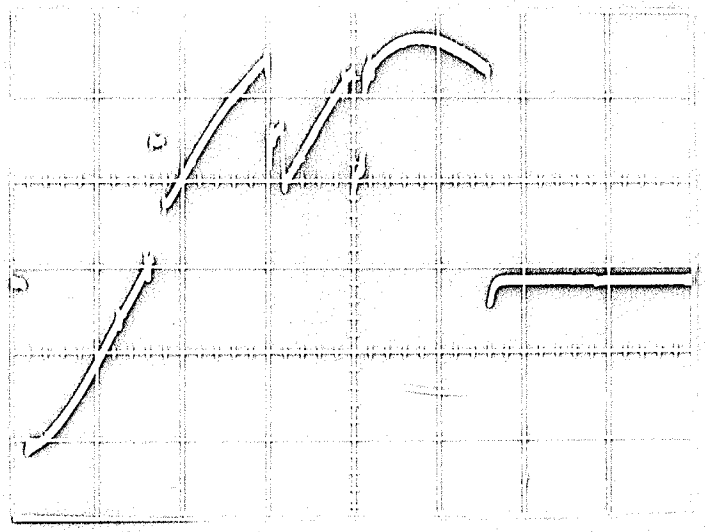
valve current



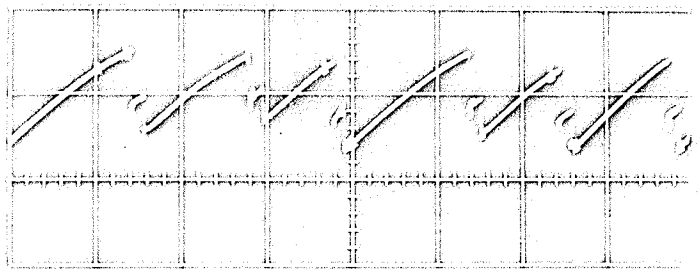
transformer secondary current

PLATE 2

inverter waveforms



valve voltage



inverter back voltage

PLATE 2

(con't)

CHAPTER 3

The Pulse Circuit

Control of the firing angle of the valves in the bridge-connected rectifier or inverter is a major requirement of the conversion of power in the high voltage direct current transmission system. A transistorized pulse circuit is developed which meets the demands placed upon a circuit of this type. Because of its importance to the system, the overall firing arrangement including the pulse circuit, phase shifter, and power supply is discussed fully.

The manner in which power is controlled in the hvdc transmission system is through the medium of grid or gate control of the electronic valves which are either mercury arc rectifiers or thyristors. The latter are solid state devices that are composed of modules of smaller units connected in series and parallel to obtain the desired operating voltage and current. Appendix A explains the basic characteristics of these devices.

Control pulses of 120^{o} duration are the most desirable for two primary reasons. Since the pulses last for the entire conduction period of a valve, if conduction should cease for any reason, the pulse will still be available to refire the valve. See Appendix D. The second and most important reason is that for the system to become energized two valves in each bridge must fire simultaneously. If the

pulses are less than 120° a probability exists that one of the two valves necessary to effect conduction will not fire concurrently with the other. Hence 120° duration pulses eliminate complex synchronization schemes. The firing arrangement is that subsystem which converts an ac 3ϕ voltage into a series of pulses of 120° duration which are spaced at 60° intervals, properly sequenced, and phase shiftable from 0° to 180°. In addition the following restrictions are placed upon the pulses.

1. The rise and fall times should be small so that the starting and stopping of two pulses in sequence are simultaneous.
2. The pulse for any one valve completing conduction should be switched off coincidentally with the initiation of the next pulse in the sequence. This guards against commutation failures which were explained in Chapter 2.
3. There should be provision for blocking which should be arranged to block all valves simultaneously for protection purposes or for disconnection of a bridge.[1]

These pulses trigger the valves in full wave bridges which are connected either for rectification or inversion.

Consider Appendix B, the complete schematic for the system. The pulse circuit is very nearly a transistorized version of that shown in Adamson and Hingorani.[1] This is a

very common type of circuit in control schemes for hvdc transmission which converts sinusoidal waves into rectangular pulses.

Examine a segment of the circuit which fires one valve. See Figure 3.1.

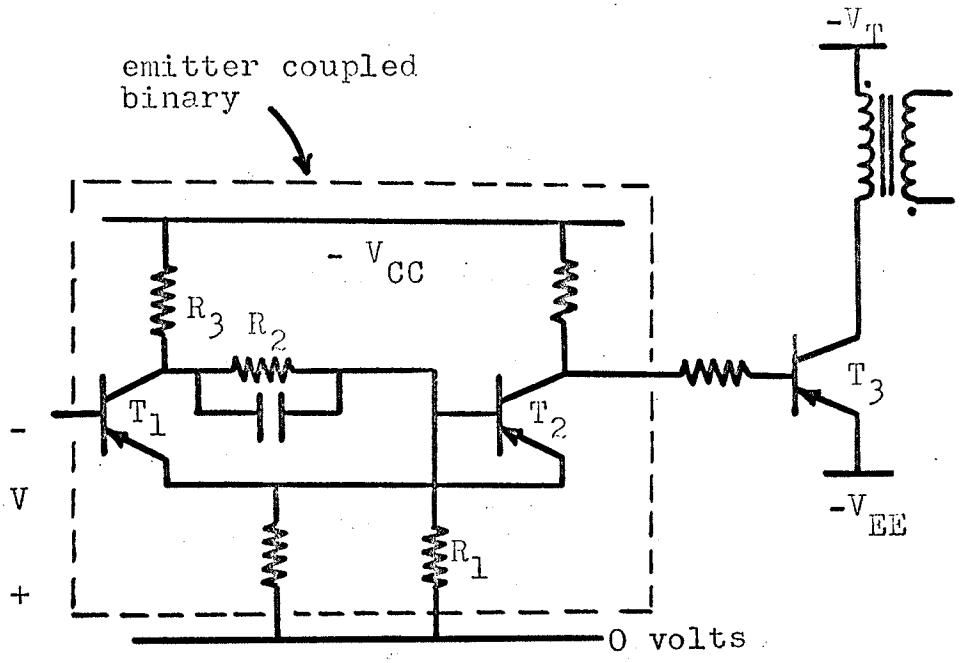


Figure 3.1 Schmitt Trigger

The heart of the circuit is an emitter coupled binary (a type of bistable switching circuit) commonly known as a Schmitt trigger. A thorough analysis of this type of bistable may be found in Millman and Taub,[2] however, the following concepts will be sufficient to understand its usefulness to the pulse circuit.

Suppose that T_1 is cutoff (non-conducting) which means that T_2 is on (conducting). Transistor T_1 can be made to

turn on at a voltage V' called the critical turn on voltage.

$$V' = R_1 V_{cc}/R_1 + R_2 + R_3$$

T_1 will remain on until the input voltage V reaches the critical turn off voltage V". Generally V" is different from V' depending upon the circuit components used. Consider the following illustration, Figure 3.2.

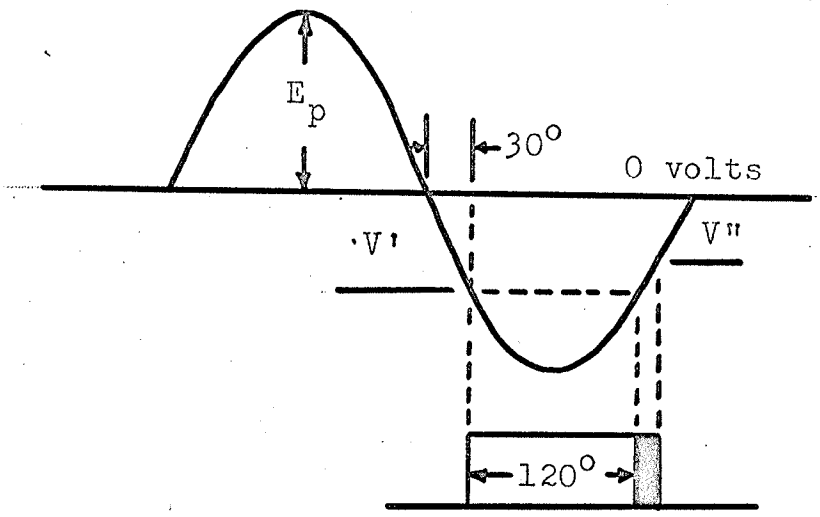
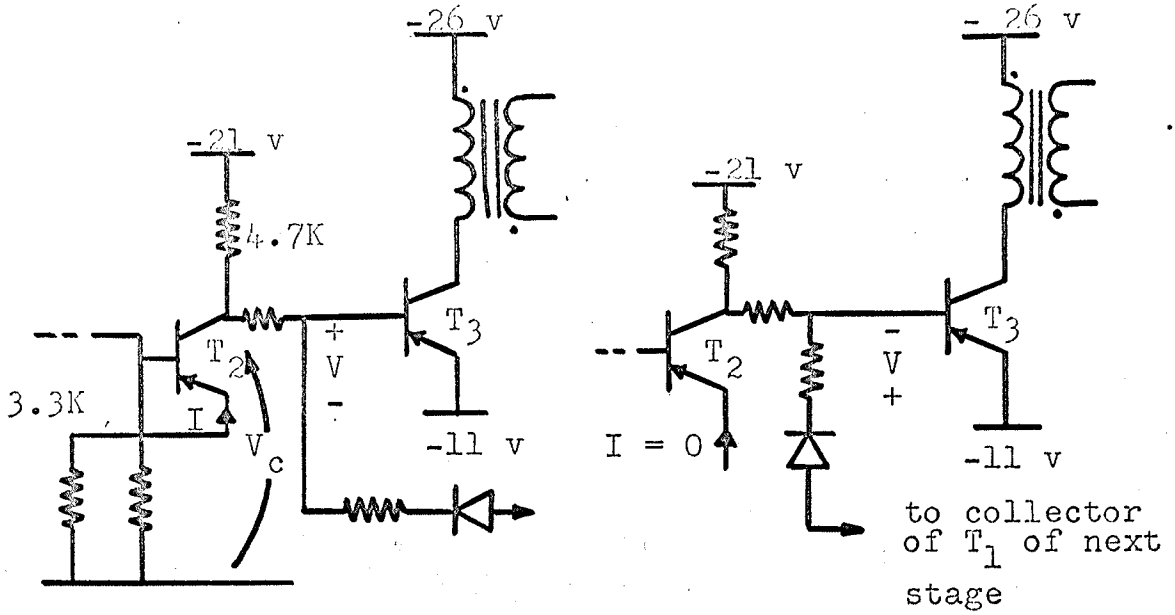


Figure 3.2 Critical input voltages

Suppose that $V' = E_p/2$. If $V' = V"$ then the pulse produced when T_1 is on will be exactly 120°. If $|V"| < |V'|$ the pulse will be greater than 120°. As will be seen later the latter condition provides no difficulty.

In Figure 3.3a suppose that T_2 is conducting and that T_1 is cut off.



T_2 on
T_3 off
T_1 off

(a)

T_2 off
T_1 on
T_3 on

(b)

Figure 3.3 Bias voltages on T_3

The magnitude of the voltage V_c is less than 11 volts which means that the base to emitter voltage of T_3 is positive. Thus T_3 is not conducting. When T_2 is off its collector voltage is -21 volts. Hence the base emitter voltage of T_3 is negative and the base current is enough to saturate T_3. As a result it conducts and a pulse is produced across the transformer. This occurs whenever T_1 is conducting. ie. T_1 and T_3 are on when T_2 is off and block simultaneously when T_2 is on. The former condition is met

if the input to the base of T_1 exceeds the critical turn on voltage. Refer to Figures 3.4 and 3.5.

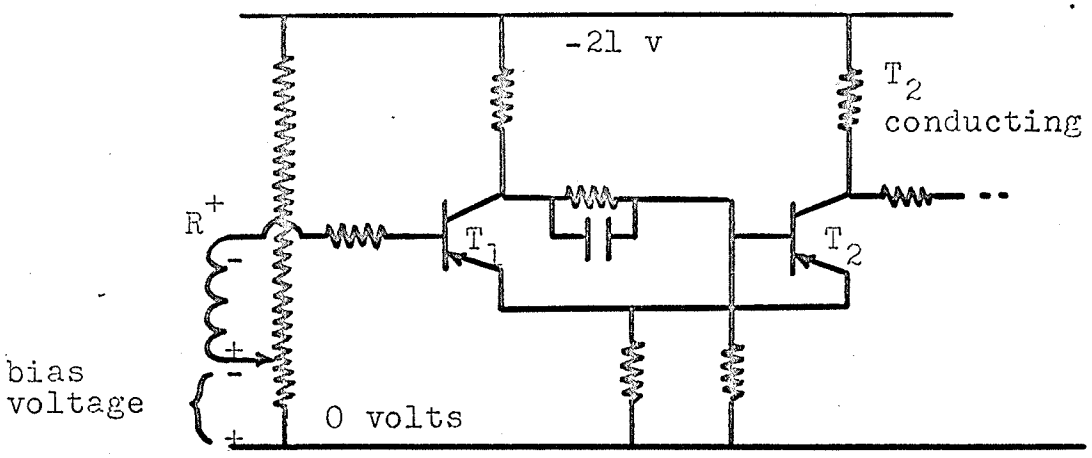


Figure 3.4 Bias voltages on T_1

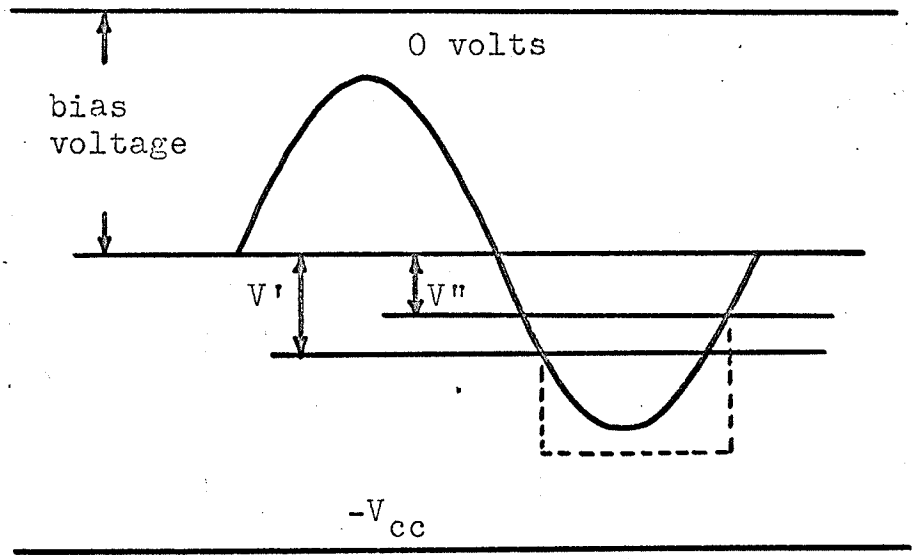


Figure 3.5 Conditions for pulse production

The bias voltage line is adjustable by means of the potentiometer intermediate to the cathode supply and ground. This allows a pulse of desired duration to be obtained.

The transition from one stable state to another occurs rapidly in this type of circuit thereby satisfying the first condition stated. The commutating capacitors assist this function by minimizing the switching time.[2] In order that the turning on of the next pulse in the sequence be coincident with the extinction of the preceding pulse, the collector of T_1 of the circuit initiating the pulse is connected through a diode and a resistor to the base of T_3 of the circuit extinguishing the pulse. See Figure 3.3. Thus when T_1 begins conduction its collector voltage becomes less negative than the emitter voltage of T_3. Hence the resulting positive voltage across the base emitter junction of T_3 turns the pulse off. Consequently the circuit parameters do not have to be chosen such that T_1 turns off after 120° of conduction, ie., the critical turn on voltage does not have to equal the critical turn off voltage. What is required is that the conduction period be somewhat greater than 120° (a condition more easily satisfied). The turn off feature assures that the pulses will be of 120° duration, hence eliminating critical biasing of the pulse circuit. See Figure 3.6.

Note that the turn off feature excludes the portion of the preceding pulse subsequent to the turning on of the following pulse.

The pulse circuit must be able to produce pulses for both the positive and negative half cycles of input phase voltage. As seen previously, only one half of the cycle

can be exploited for this function. Consequently the phase voltage from the phase shift circuit is fed into a transformer with a center-tapped secondary. The resulting 180° displacement between the two voltages allows the required two pulses to be formed for any phase voltage. Refer to Figure 3.7 drawn with reference to Appendix B.

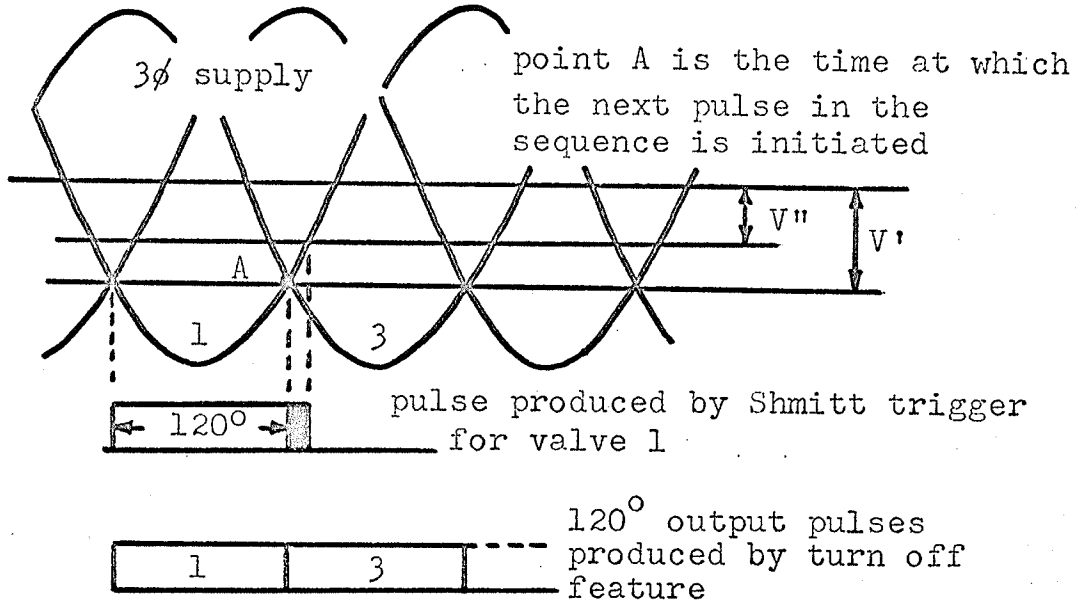


Figure 3.6 Turn off feature

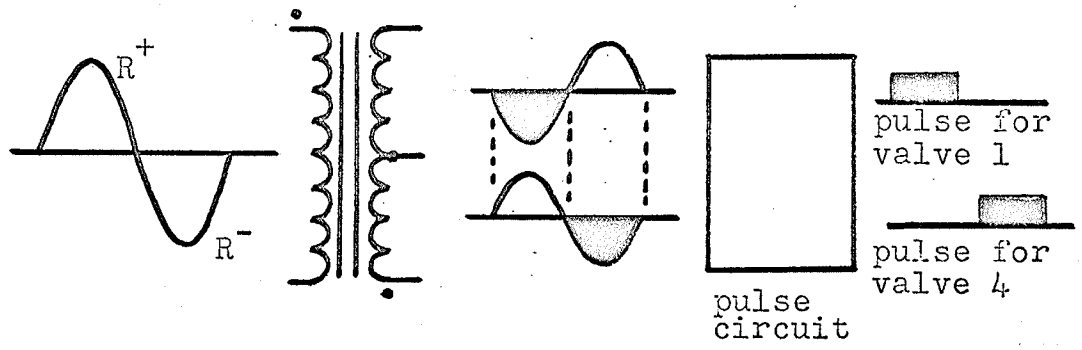


Figure 3.7 Pulse production on the positive and negative half cycles

Three of the six binary circuits produce pulses on pos- half cycles. These are tied together by the turn off circuitry and form a closed system. Identical closed systems are required for each set of three circuits generating pulses for the positive and negative portions of the input phase voltages. Note in Figure 3.7 that the dot placement for the transformer has been selected for 180° phase reversal between the voltage to the bridge and the voltage to the pulse circuit. This is necessary since the PNP transistors of the pulse circuit create pulses on negative half cycles whereas the thyristors in the bridge utilize positive half cycles. Ideally the outputs to the bridges appear as in Figure 3.8.

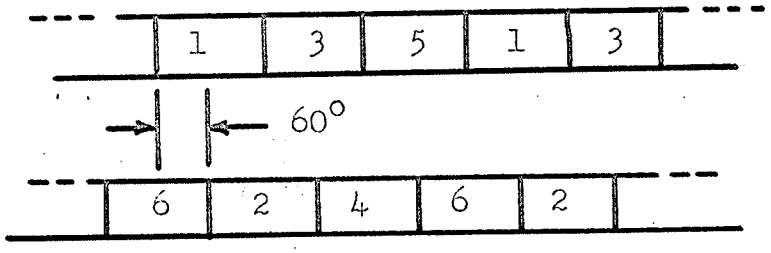


Figure 3.8 Ideal Pulses

Provision for blocking all valves simultaneously would be obtained by simply connecting all transistors T_2 through resistors from their collectors to ground. This would result in a positive voltage across the base emitter junctions of transistors T_3 which would cut them off. This feature has not been included since by-pass valves were

not incorporated.[1]

The collectors of transistors T_3 are connected in series with audio transformers as shown in Figure 3.3. Pulse transformers would have been more desirable, however, the waveshape is not distorted excessively. Testing of the circuit indicated that thyristors rated at 200 volts and 7 amps demanded triggering gate currents in excess of what the pulse circuit could produce since the audio transformers did not closely approximate an ideal voltage supply. As mentioned in Chapter 1 gate sensitive thyristors were employed. These incorporated 10,000 ohm resistors in series with their gates to obtain high input impedance and thereby reduce loading of the transformers. A transformer no load secondary voltage of 5 volts maximum was found to be satisfactory. In addition the excessive negative voltage present in the output was eliminated by the use of diodes shunted across the secondaries of the transformers. See Figure 3.9.

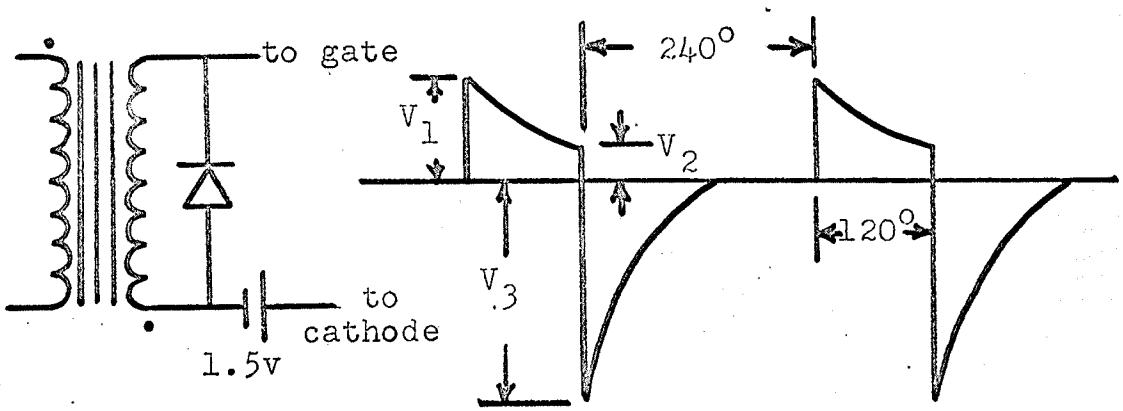


Figure 3.9 "Pulse transformer" output

The negative portion arises through transformer action. Since only changes are transformed, voltages are produced on the leading and trailing edges of the input pulse. The initial voltage peaks, V_1 and V_3, decay according to time constants determined by the magnetizing inductance of the transformer divided by the resistance in the conducting paths. Because of the high input impedance the peak of the positive voltage is maintained near 5 volts. The decay results in V_2 having a magnitude of about 2 volts. This combined with the negative bias of 1.5 volts still yields a voltage of sufficient magnitude to refire the valves if necessary. The energy stored in the transformer during the positive half cycle is released in the negative half cycle and is manifest as a large spike which decays in less than 240° since the resistance seen by the negative voltage is larger. This voltage spike is undesirable since it could damage the sensitive gates of the thyristors.

The phase shifting device is one found in many electronics books.[3] Its function is to shift the phase voltages from the ac 4 wire supply. Refer to Appendix B and Figure 3.10.

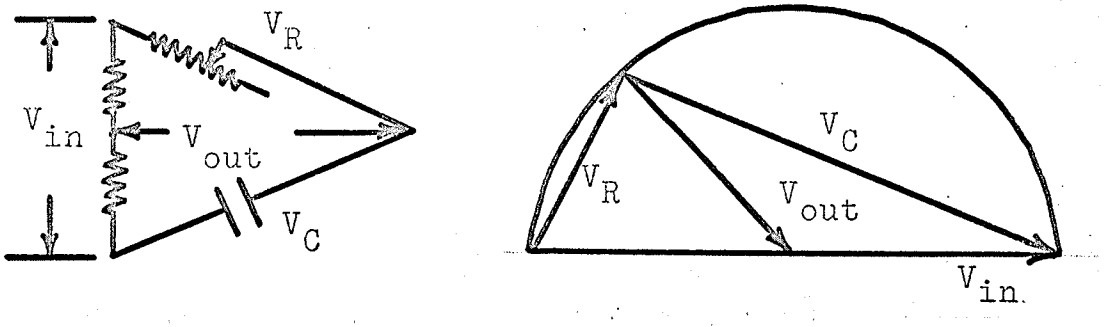


Figure 3.10 Phase Shifter

In this circuit the output voltage is a constant magnitude equal to one half the input voltage per phase. Phase displacement between input and output is theoretically variable from 0° to 180°. The alterable device is a ganged three element variable resistor. When the phase shift is zero V_R must be zero. This is easily obtained from the resistors. However, when the phase shift is near maximum the capacitor impedance must be small compared to that of the resistance elements. Furthermore the output impedance of the phase shifter must be small since the input impedance of the pulse circuit is low. The output impedance is of the form shown in Figure 3.11.

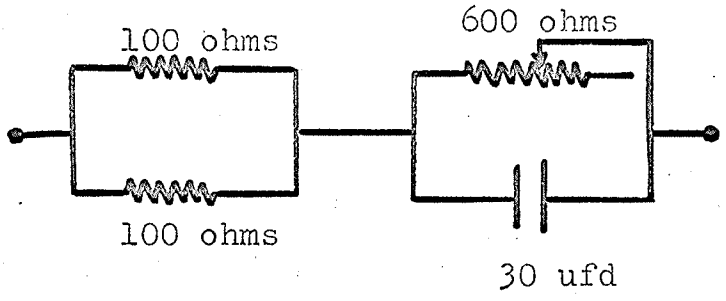


Figure 3.11 Output impedance of the phase shifter

Hence the component impedances must be kept low and in accordance with the previous restriction. The values shown produce very nearly 180° of phase shift continuously from 0°.

Since the input and output of the phase shifter did not share a common point, three single phase transformers with

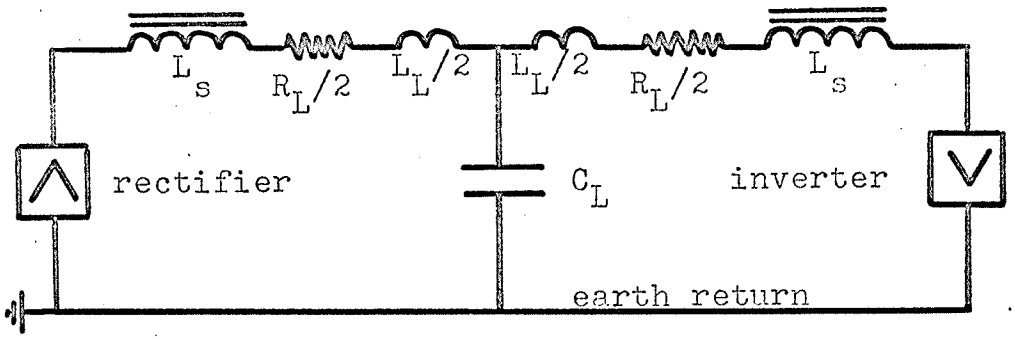
turns ratios of 1 : 2ct were connected to the three independent outputs thereby providing isolation and hence eliminating short circuiting of components in the phase shift circuit. The center taps on the secondaries of these transformers were joined thus providing the required six outputs and a floating neutral point. The input voltages to the pulse circuit and phase shift circuit were identical in magnitude because the attenuation of the latter and the transformer turns ratio combined to produce an overall 1 : 1 ratio. This allows the proper phase voltages to be set at the ac system terminals. A maximum phase voltage of 15 volts peak proved to be compatible with the bias conditions shown in Appendix B.

Three power supply voltage levels were necessitated by the pulse circuit. Two regulated dc supplies were built to independently provide these voltages to the rectifier and inverter pulse circuits. Appendix C discusses the more salient details of these.

CHAPTER 4

The Transmission Line

The line to be simulated is a monopolar arrangement which is the simplest form of hvdc transmission line. It consists of a high voltage conductor and an earth return. Its equivalent circuit is shown in Figure 4.1.



L_s smoothing inductor

R_L line resistance

L_L line inductance

C_L line capacitance

Figure 4.1 Equivalent circuit of a monopolar hvdc transmission line

The purpose of the line inductors, L_s, as explained in Chapters 1 and 2 is to smooth the ripple in the dc as it leaves the rectifier. A satisfactory value of the smoothing inductance was found to be 9 henries. Line resistances $R_L/2$ of 2.5 ohms were also inserted. The capacitance and

transmission line inductance were neglected since L_L was much less than L_s and under steady state conditions C_L has little effect. The earth return was represented by a zero resistance conductor. Figure 4.2 illustrates the theoretical dc line voltage past the smoothing inductor. The actual waveform obtained from the model is shown in Plate 3.

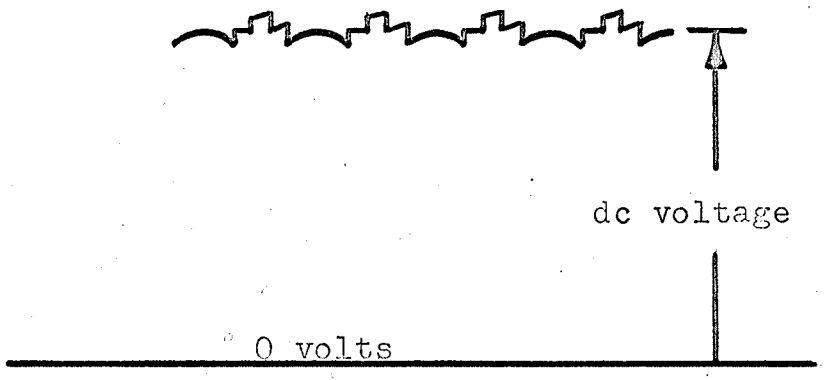
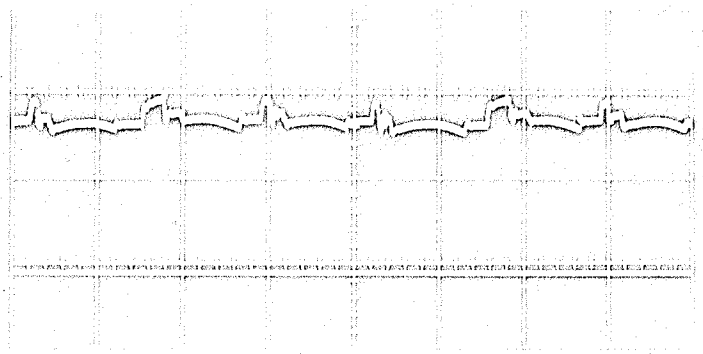
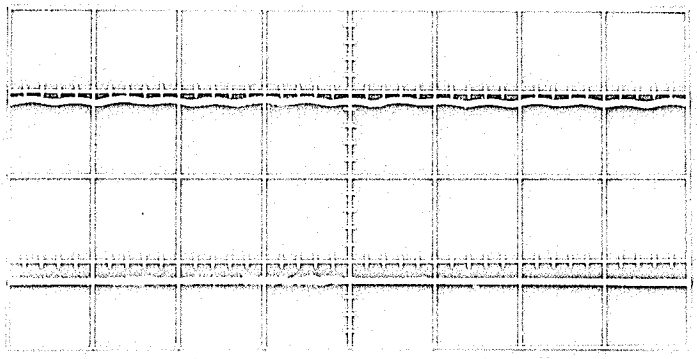


Figure 4.2 Transmission line voltage

Because the smoothing inductors have finite inductance the dc line current contained a small amount of ripple as seen in Plate 3.



dc line voltage



dc line current

PLATE 3

dc line waveforms

CHAPTER 5

Assessment of the Operation of the Model

The purpose of this project was to construct a model that would adequately simulate the voltage and current waveforms arising in a hvdc transmission system. The emphasis has not been on large amounts of power but rather on faithfully reproducing the waveshapes inherent in the conversion processes. The ability of the model to simulate modes of operation has also been a design objective. The degree to which these criteria have been met is indicated from the results presented in this chapter.

The photographs shown in Plates 1,2, and 3 illustrate that the model functioned in basically the correct manner. The two most obvious deviations from the theoretical are the high frequency oscillations which appear on the voltage waveforms and the improperly spaced firing points of the valves. The high frequency oscillations or "ringing" arise in circuits in which there are capacitive and inductive energy storing devices and switching operations. In the conversion section of the model system large amounts of inductance are present, ie. the 60 mh. winding inductances. The firing of the valves in the bridges provides the fast voltage changes. Because the changes are of greater magnitude at the inverter ($\underline{B} > \underline{a}$) it seems likely that the ringing will be originated there. No capacitance has been

placed in this part of the circuit so that its origin must be parasitic capacitances in the thyristors, stray capacitance in the connecting wires, and winding capacitances in the transformers and inductors. The frequency of these oscillations is very high indicating that the capacitances are small. The decay of the ringing is rapid since there is much resistance in the circuit. Because of the high frequency of oscillation and the damping the ringing appears as a small spike. The oscillations do not affect the performance of the model and have not been eliminated. They could be suppressed by properly selected R-C damping circuits placed across the valves. The propagation of the ringing along the line could be prevented by high frequency filters at the dc terminals of the convertors.

The second major deviation from theoretical is the non-uniform spacing of the firing pulses. As mentioned in Chapter 3 the pulses should appear at 60^{o} intervals. However, as can be observed from photographs of the rectifier and inverter line voltages (see Plates 1,2) the voltage dents do not appear to be separated according to this criterion. The reason for this is that the ganged three element variable resistors used in the phase shift circuits were not adequately balanced. The resistors were non-linearly tapered and not matched. Two of the elements were 600 ohms while the other was much larger. To partially correct this 560 ohm resistors were placed in parallel with the odd resistor. In so doing the compensated resis-

tor did not possess the same non-linearity as the other two. Hence the phase shift was unequal and caused the spacing of the pulses to deviate from 60^{o}. The problem could be corrected by inserting precision ganged, 600 ohm, linear taper resistors with possibly 1% tolerance on their linearity. This unbalanced phase shift detracts from the value of the model for illustrating theoretical principles but does not seriously affect the functioning of the system.

With the exception of the above two difficulties the model produced waveforms comparable to theoretical expectations. The additional winding reactance created wide readily observable voltage dents on the valve and transformer secondary voltages. The current waveforms were especially good. See Plates 1,2, and 3. The ripple on the dc line current was almost completely removed by the 9 h. chokes. The nature of the rise and decay of the valve currents were preserved at the rectifier and inverter bridges. As mentioned previously power transfer capability was secondary to faithful representation of the waveforms. Because the dc current expected was low, the 60 mh. chokes were added to the transformer windings. Also a considerable amount of voltage at the rectifier (approximately 50%) is dropped across the smoothing chokes. Hence this was the greatest factor in determining the amount of current which could be transferred. The problem is one of sacrificing the ripple improvement by decreasing the size

of the smoothing chokes for a greater current magnitude. The choice in this case tended toward smooth dc since this would produce a more accurate waveshape. In the present model an increase in current to 50 milliamps from 20 milliamps can be achieved if desired by shorting one of the smoothing inductors. Provision for this has been included by means of a switch. Chokes with less dc resistance could have been utilized to obtain some improvement. Smoothing inductors of 1.5 h. each were tried but it was found that they placed more stringent restrictions on the ac line voltages at the bridges.

The pulse circuits at both ends were flexible enough to allow the ac system voltage to vary within several percent of the 15 volt limit required to operate them. This was due in large part to the neutral point of the isolating transformer secondaries being connected to the potentiometer as explained in Chapter 3. Hence tap changing can be simulated to alter both the rectifier and inverter voltages.

Several tests were conducted to demonstrate the usefulness of the model. The tests were as follows.

1. Comparison of measured quantities with theoretical calculations.
2. Simulation of the interconnection by a dc link of two ac systems with capacities large compared to the dc system.

3. Simulation of the interconnection by a dc link of two ac systems having different frequencies to illustrate the asynchronous nature of the tie.
4. Power flow reversal to simulate a dc interconnection between two ac systems for the interchange of power.

Test 1

In performing the test the following point was observed. The line voltages were measured at the rectifier and inverter bridges. This means that the limiting resistance and the additional winding reactance were included with the transformer secondary. The test set up was as shown in Figure 5.1.

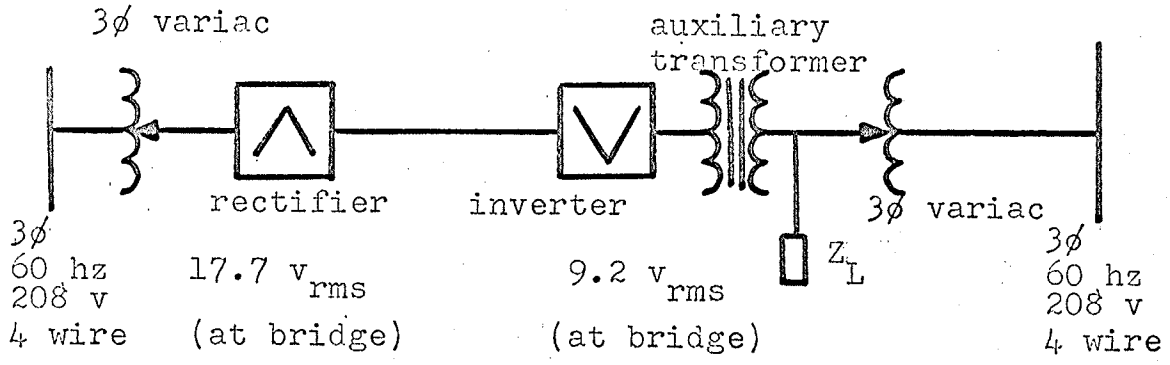


Figure 5.1 Arrangement for Test 1

The auxiliary transformer was utilized to more closely simulate the inverter end in that a two winding transformer would generally be used. The load was represented by

resistances boxes wye connected having 1.61 ohms per phase. The following were measured on the model with the use of an oscilloscope having a differential input and dc voltmeters. The currents were measured by determining voltage drops across known resistors.

Rectifier

ac line voltage, E_R, 17.7 v_{rms}
rectifier output voltage, V_{dr}, 22.0 v
dc line current, I_d, 20 ma
rectifier delay angle, a, 10°
commutation angle, u, 12°
transformer winding resistance, R_R, 20 ohms/phase
transformer winding inductance, L, 60 mh
supply frequency 60 hz

Inverter

ac line voltage, E_I, 9.2 v_{rms}
inverter back voltage, V_{di}, 10.5 v
dc line current, I_d, 20 ma
inverter advance angle, B, 30°
commutation angle*, u, 9°
transformer winding resistance, R_I, 4 ohms/phase
transformer winding inductance, L, 60 mh
supply frequency 60 hz

*Note: The commutation angle is slightly less at the inverter because of the reactive current in the transformer windings.

Theoretically the dc voltage at the rectifier before the smoothing inductor is given by

$$V_{dr} = V_d - 2V_{arc} - 2I_dR_R$$

where: V_d is given in Chapter 1 as $V_d = V_o \cos \underline{a} - 3\underline{w}LI_d/3.14$

V_{arc} is the voltage drop in the thyristor and is considered negligible

R_R is the resistance in the transformer secondary windings

Substitution of the values yields $\underline{V_{dr} = 21.6}$ volts. This compares favourably with the 22.0 volts measured on the model system.

The theoretical inverter back voltage is given by

$$V_{di} = V_d + 2V_{arc} + 2I_dR_I$$

where: V_d is given in Chapter 2 as $V_d = V_o \cos \underline{B} + 3\underline{w}LI_d/3.14$

R_I is the resistance in the transformer secondary windings

Substituting the values yields $\underline{V_{di} = 11.3}$ volts.
The measured value was 10.5 volts.

The discrepancy at the rectifier is only 0.4 volts which means that within limitations the system functions in close agreement with theory. The major restriction is in the ability to set the angle of delay at precisely 10^{o} by means of the calibrations on the scope. Also the unequal phase shift might account for the larger than expected value. In the low resistance range of the phase shift resistors the two identical elements will have approximately the same ohmage. The third will have a value which is less than that of the resistor alone since an additional resistance has been placed in parallel with it. Hence if the resulting resistance is less than the other two then part of the output voltage will be due to a smaller delay angle. Consequently the voltage will be slightly increased.

The unbalance of the variable resistors can also be used to explain the larger deviation in the inverter back voltage. For the delay angle required for inverter operation the resistance on the variable resistors is close to maximum. The element which has been compensated by the parallel resistor will reach its maximum value prior to the other two because its uncompensated value is very large. Hence one pair of thyristors will be delayed more. The resulting larger angles of advance for the other pairs

of valves will introduce a lower net back voltage. Thus the voltage V_{di} as measured from the model will be lower than expected. The difficulty in setting B accurately is another source of error. Neglect of the actual transformer winding resistances and reactances might have a small effect but generally their values should be small compared to the added quantities.

If the type of variable resistors mentioned previously were installed, the discrepancies at both the rectifier and inverter would be reduced considerably.

The rms current in the transformer secondary windings was measured with an ac instrument and found to be 14.0 ma. From theoretical considerations[1] the rms current in the transformer is given by

$$I_{rms} = (2/3 - u/3 \cdot 3.14)^{\frac{1}{2}} I_d$$

where u is given in radians

Substitution of the values yields $I_{rms} = 16.3$ amps.

The lack of closer agreement is due in large measure to the fact that the ac meter employed was designed to measure sinusoidal waves. If it is assumed that the meter responds to the fundamental (60 hz) and that the 5th, 7th, 11th, etc. harmonics in the current are excluded then the value indicated on the meter would be to a close approximation[1]

$$.78I_d = .78(20) = 15.6 \text{ ma}$$

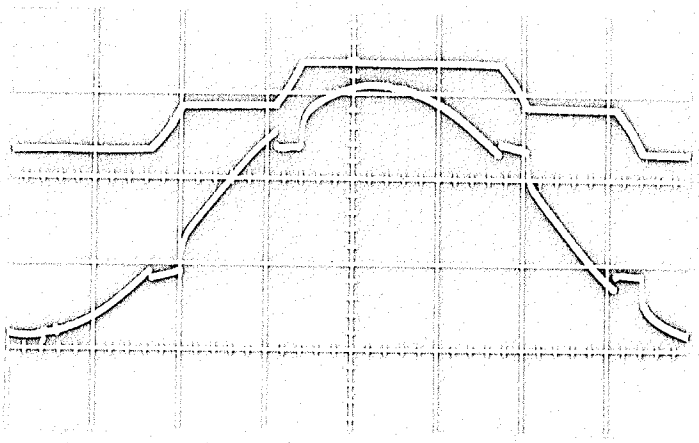
If in addition the triplen harmonics introduced by the unbalanced firing of the valves are excluded by the meter, the fundamental content would be reduced even further. The value of I_d as determined from the peak of the transformer current and in the dc line was identical to the latter and equal to 20 ma. as required.

Power measurements were not undertaken because of the small currents involved. From the measured quantities the theoretical power could be calculated. Plate 4 shows the transformer secondary voltage and current for one phase at the rectifier and inverter. The characteristic phase angle relationships are clearly visible. ie. At the rectifier the current lags the voltage whereas at the inverter the current leads the voltage.

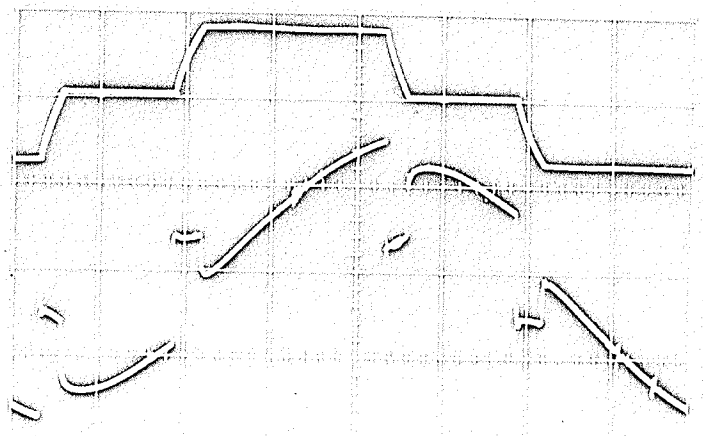
Test 2

The arrangement for this test is the same as shown in Figure 5.1. The purpose of this test was to observe how the model system reacted under certain operating conditions.

The current in the dc line is controlled by the inverter back voltage if the rectifier voltage is invariate. By adjusting B at the inverter the current observed on an oscilloscope was seen to rise and fall with increasing and decreasing B. Also by increasing I_d the voltage dents were



rectifier transformer phase voltage and current



inverter transformer phase voltage and current

PLATE 4
transformer voltage and current waveforms

made wider. Similarly, if the inverter voltage is fixed and the rectifier delay angle, a, is increased, the current decreases. If the rectifier voltage is dropped to below the inverter back voltage the system will run down. However, by returning the angle to zero the system will recover. Tap changing on both the rectifier and inverter transformers can be simulated by varying the output voltage on the 3ø variacs. The amount of allowable change is about 10%. The simplest manner in which to energize the system was found to be to operate the inverter slightly into the rectifier region ($B > 90^{\circ}$) and then to decrease the angle to the desired value.

Test 2 illustrated that the model adequately represented a dc link between two large capacity ac systems.

Test 3

The arrangement for this test is shown in Figure 5.2.

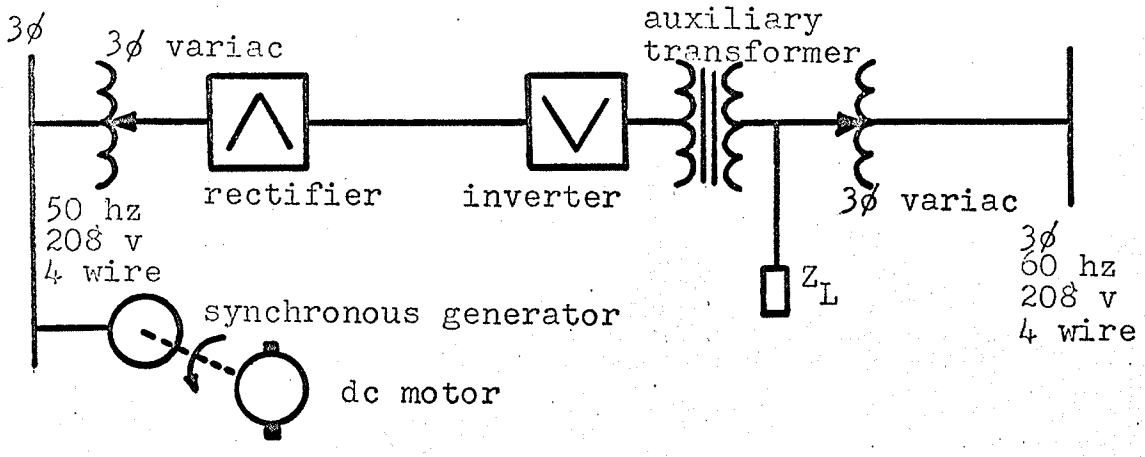


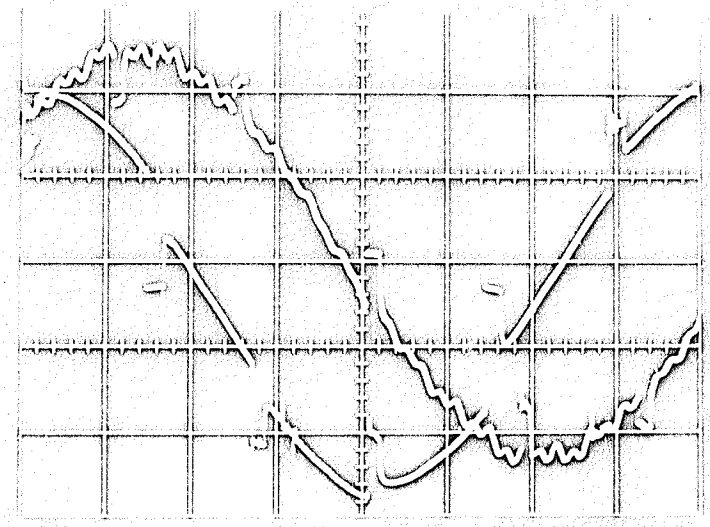
Figure 5.2 Arrangement for Test 3

In this test the 3ϕ ac mains at the rectifier were replaced by a synchronous generator driven to produce an output frequency of 50 hz. The line voltages at the convertor bridges were set as in Test 1. The system operated according to theory even at frequencies less than 50 hz. However, it should be noted that at these lower frequencies the total phase shift is not attainable since the circuits which perform this function were designed around 60 hz. This is not a serious problem in this case since the rectifier operates at small delay angles. Plate 5 illustrates the transformer secondary line voltages and currents at both the rectifier and inverter. The lower frequency of the rectifier waveforms is clearly in evidence.

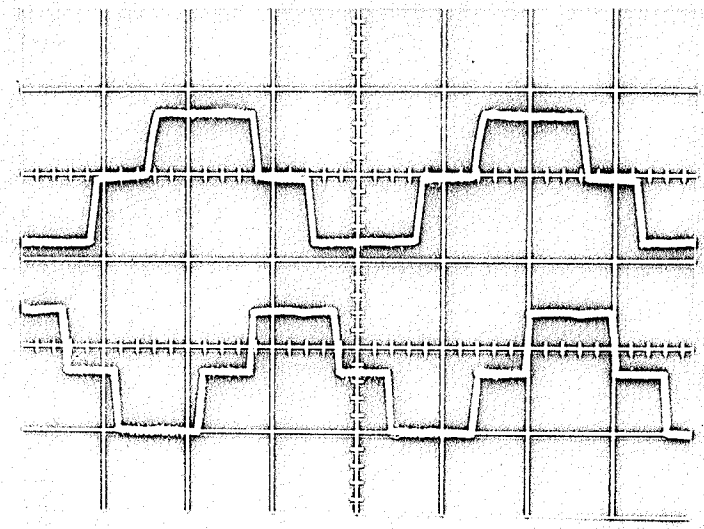
This test indicates the asynchronous nature of the dc link.

Test 4

For this test the arrangement shown in Figure 5.1 was modified so that the auxiliary transformer and the load were placed at the rectifier end and the inverter was supplied from a 3ϕ variac directly. The line voltages mentioned in Test 1 were interchanged and $\underline{a}$ was set at 150^{o} and $\underline{B}$ at 10^{o}. From observations of the voltage and current waveforms it was obvious that the power flow reversed. When the inverter functions as a rectifier its dc voltage becomes negative. The rectifier voltage also changes sign under these conditions and becomes a variable negative



transformer line voltages
rectifier - 50 hz
inverter - 60 hz



transformer secondary currents
top rectifier - 50 hz
bottom inverter - 60 hz

PLATE 5
operation at different
frequencies

back voltage. Since the current still flows in the same direction the power flow has reversed. See Figure 5.3.

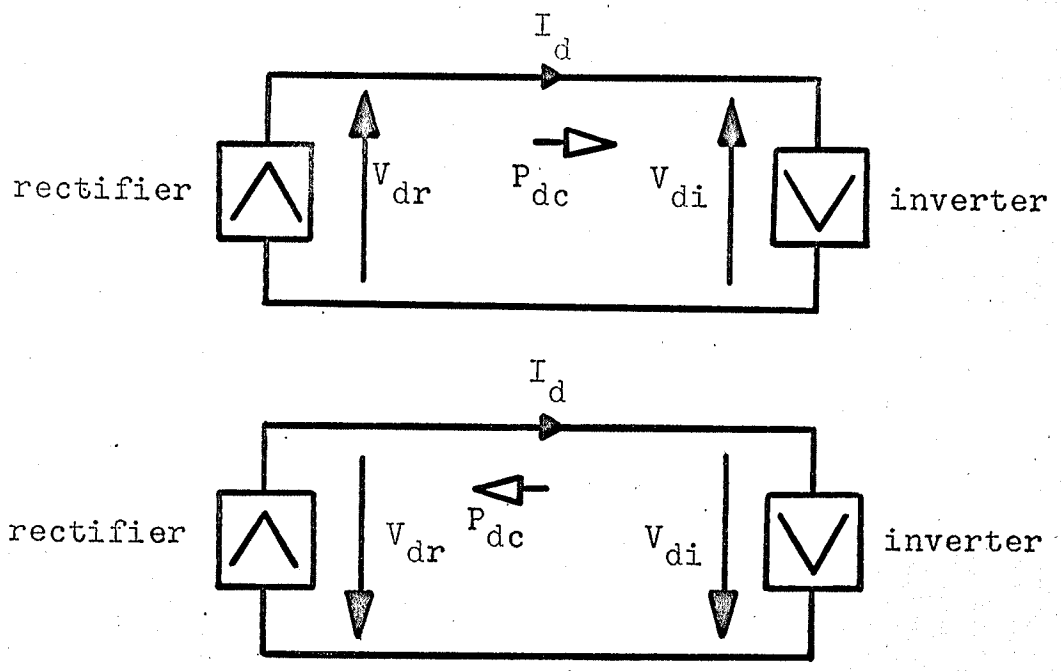


Figure 5.3 Power flow reversal.

Hence both convertors function as either rectifiers or inverters. This simulates power flow reversal.

From the above tests it can be concluded that the model hvdc system performs well enough to illustrate the conversion and operating principles involved in hvdc transmission. The model is deficient in several areas and could be greatly improved if the following modifications were made.

1. Replacement of the present ganged variable resistors in

the phase shift circuits with linear taper, 600 ohm variable resistors having 1% tolerance on their linearity. This would greatly enhance the use of the model for accurate measurements.

2. Removal of the dependence of the pulse circuitry and the bridge on the same 3ø ac supply voltage. A scheme such as shown in Figure 5.4 would allow more power to be transferred.

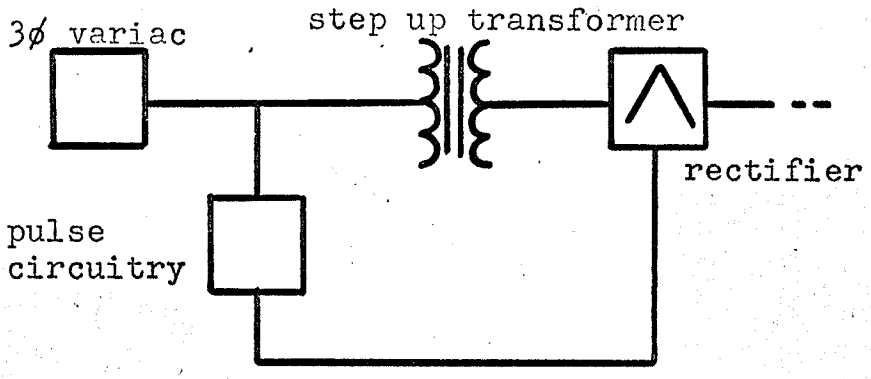


Figure 5.4 Alternate bridge supply

This system employs a step up transformer which would allow the voltage at the bridge to be increased without affecting the bias arrangement of the pulse circuit. In the present set up the ac voltage to the pulse circuitry lags the voltage to the bridge because of the isolating transformer. See Figure I.1. Thus with the addition of the step up transformers the lag introduced in the voltage to the bridge would compensate the lag

of the voltage to the pulse circuits and hence would improve the system performance.

3. Use of the existing thyristors to trigger ones of higher voltage and current rating. A scheme of this type entitled "Thyratron Replacement" is given in Reference 4 in the bibliography. This method would have to be used in conjunction with the above modification for full benefit. By so doing the power transferred could be appreciable and measurable.
4. Addition of damping circuits to minimize the high frequency oscillations appearing on the voltage waveforms. These damping circuits, series R-C arrangements, would be placed in shunt with the anode and cathode of the thyristors.
5. Addition of harmonic filters on both the ac and dc system sides of the convertor. The ac side filters would remove the harmonics from the current resulting in essentially a sinusoidal current waveform. The filters on the dc side would be utilized to suppress voltage harmonics on the dc line. Hence the ringing from one convertor would not propagate to the other.
6. Addition of miscellaneous equipment such as by-pass valves, valve blocking circuitry, and anode reactors.

Cory[7] has outlined several design objectives for realization of a hvdc simulator. Among these which could be incorporated into the present model are variable ac system impedance, variable smoothing inductance in the dc

transmission line (partially realized in the model), and filter circuits to remove the current harmonics. This would add to the usefulness of the model as an accurate representation of the hvdc transmission scheme.

In its current state the model performs several of the required functions. The waveforms attainable from it possess sufficient clarity such that measurements of voltages, currents and angles are precise enough to allow calculated values to compare favourably with measured ones. With regard to the representation of operating conditions the system worked well. Some of the simulations were:

1. system operation at two different frequencies
2. power flow reversal
3. running down of the rectifier
4. tap changing of the convertor transformers

Because the model was designed with small currents in mind (very much less than the thyristor rating) the danger of ruining the circuitry is minimal. Operation of both convertors fully as rectifiers inflicts no damage on the system whatsoever. The following voltage limits should be born in mind for adequate functioning of the model system.

RECTIFIER LINE VOLTAGE (measured at the bridge)

18 volts $\pm$ 10% (rms)

INVERTER LINE VOLTAGE (measured at the bridge)

9 volts $\pm$ 10% (rms)

PULSE CIRCUIT POWER SUPPLY VOLTAGE

110 volts (rms)

A number of hvdc simulators are currently in existence. They for the most part belong to research laboratories such as the one owned by Manchester College of Science and Technology or are scale replicas of actual working systems such as the Stalingrad Hydro-electric Station to Donbass D.C. Power Transmission System.[8] The latter model is an elaborate system consisting of various groups of bridges which can be selected for study from a control panel. Several transformer banks connected in wye or delta supply bridges that have pairs of valves in series. Filter circuits, damping circuits, and by-pass valves with suitable control have also been included. Tests performed on this large model give accurate representations of conditions which might appear on the full scale system. This model is one of the most important of the hvdc simulators.

Other models owned by English Electric, C.E.G.B. Laboratories, General Electric, et al. are of the same degree of complexity. References in the bibliography illuminate some of the more salient features and construction details of these systems. References 7,9, and 10 consider some of the design criteria for hvdc system simulators. Characteristics of the dc simulators owned by Manchester College and Imperial College are presented in Reference 7. For purposes of comparison a similar table has been pre-

pared for the model system constructed.

Type of rectifier and group arrangement	thyristors connected in 3ø 6 pulse bridge group without by-pass
Number of groups, rating and methods of connection	two groups to form 2 - 6 pulse convertors each rated at 25 v, 20 or 50 ma
Number, rating and connection of group transformers	one wye-wye at the inverter, no tertiary
D.C. reactors	switchable from 18 h to 9 h
D.C. line simulation	5 ohm resistance
A.C. system simulation	external circuits and machines as required
Harmonic filters and var compensation	not provided
Voltage control	ac voltage varied by 3ø variacs
Grid control methods	manual phase shift control

Grid control methods (con't)	through bistable circuits providing 120° pulses. Each group controlled from one phase shifter
Measuring facilities	external sockets in the valve connections for observation with a differential input CRO, similar sockets on dc connections, external meters plugged into sockets as required

The constructed model cannot be classed as a system simulator but rather as a waveform simulator. Nevertheless it fulfills the requirement of illustrating conversion principles and as such is a working tool for understanding high voltage direct current transmission.

** Bibliography **

1. C. Adamson, N.G. Hingorani; High Voltage D.C. Power Transmission, Garraway Ltd., London 1960
2. J. Millman, H. Taub; Digital and Switching Waveforms, McGraw Hill Book Co.,Inc., New York 1965
3. J.D. Ryder; Engineering Electronics, McGraw Hill Book Co., Inc., New York 1957
4. F.W. Gutewiller; General Electric SCR Manual, 4th Ed., Semiconductor Products Dept., General Electric, Syracuse 1967
5. J.F. Cleary; General Electric Transistor Manual, 7th Ed., Semiconductor Products Dept., General Electric Syracuse 1964
6. C.L. Alley, K.W. Atwood; Electronic Engineering, 2nd Ed., John Wiley & Sons, Inc., New York 1967
7. B.J. Cory; High Voltage Direct Current Convertors and Systems, Macdonald and Co. (Publishers) Ltd., London 1965
8. V.V. Voskresenskii, Kh. F. Barakaev, L.V. Travin; "A Scale Model of the Stalingrad Hydro-electric Station to Donbass D.C. Power Transmission System", Direct Current, Vol.6, No.1, April 1961
9. C. Adamson, N.G. Hingorani; "Semiconductor Circuitry and Arrangements for the Protection and Control of Bridge-connected Current Convertors", Direct Current, Vol.5, No.2, September 1960

10. R. Feinberg, N.G. Hingorani, M. Brown, R.K. Pearson; "The Construction of an HVDC Power Transmission System Model", Direct Current, Vol.7, No.7, July 1962

11. J.P. Bowles, B.J. Cory; "The Model HVDC Transmission System at Imperial College , London", Direct Current, Vol.8, No.9, September 1963

12. C. Adamson; "A High Voltage Direct Current Laboratory at Manchester College of Science and Technology", Direct Current, Vol.3, No.2, September 1956

13. N.G. Hingorani; "The Scope of Semiconductor Devices in the Control and Protection of HVDC Systems", Direct Current, Vol.6, No.6, September 1961

14. C.G. Dewey, F.J. Ellert, T.H. Lee, T.H. Titus; "Development of Experimental 20KV, 36MW Solid State Convertors for HVDC Systems", IEEE Transactions on Power Apparatus and Systems, Vol.PAS 87, No.4, April 1968

APPENDIX A

HVDC Valve Operation

Consider the generalized valve shown in Figure A.1.

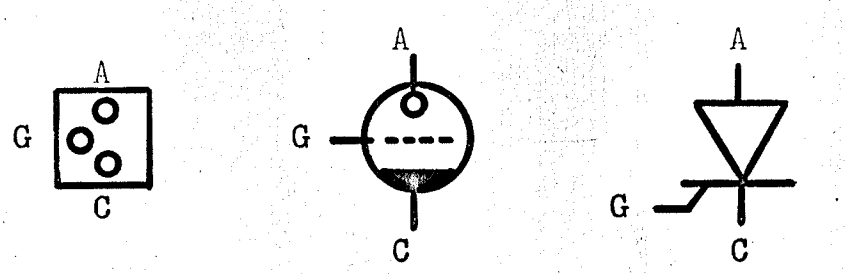


Figure A.1 HVDC Valves

Both the mercury arc rectifier and thyristor valves have anode and cathode elements. The G element in the former is called a grid; that in the latter is called a gate. Conduction in the former is via an arc of mercury vapor. The thyristor conducts through the medium of electron current which avalanches across the junctions of solid state material when certain conditions exist in the device.

Suppose the generalized device is driven by a sinusoidal voltage as shown in Figure A.2. A load is also placed in series with the anode of the device. The valve will block (prevent current flow through it) up to a certain critical voltage called the forward breakdown voltage. Hence when this voltage is not exceeded no current will flow through the load. If during the positive half cycle a positive

voltage, E_{GC}, of sufficient magnitude is applied, current will flow for the duration of the half cycle susequent to the application of the voltage. See Figure A.3.

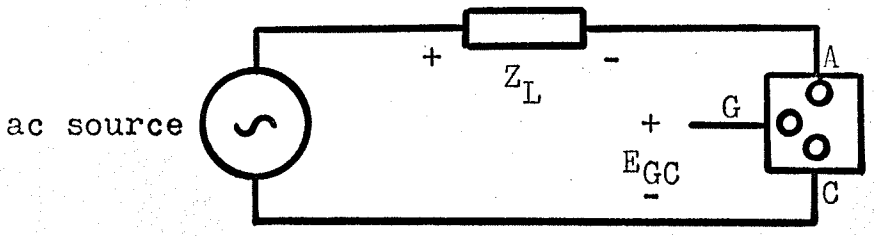


Figure A.2 Typical rectifier circuit

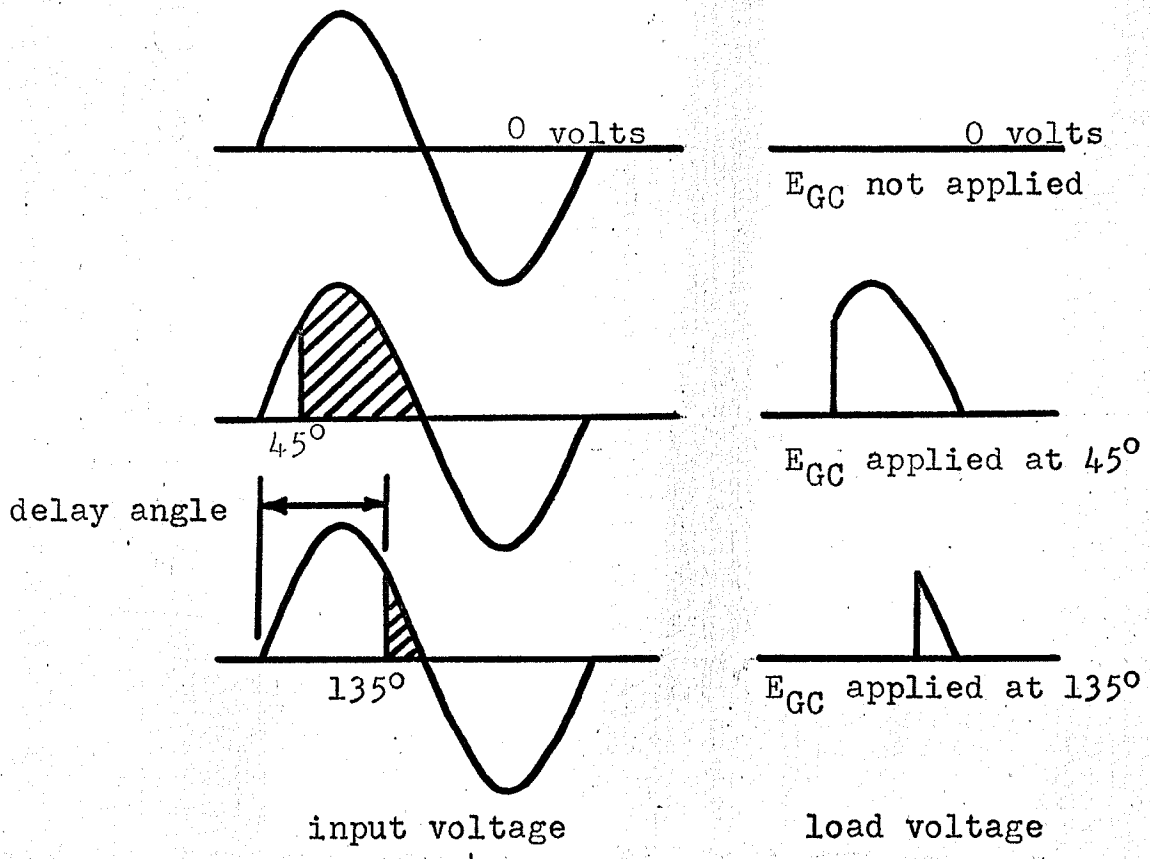


Figure A.3 Effect of E_{GC}

The magnitude of E_{GC} varies with the anode to cathode hence it should be chosen so that the device will fire

(begin conduction) at the lowest anode to cathode voltage expected. The angle measured from the zero of the voltage wave at which E_{GC} is applied is commonly referred to as the delay angle. E_{GC} may be a high energy impulse or pulse of predetermined width.

Since the device is a rectifier a negative anode to cathode voltage will arrest conduction unless the current can be maintained as would be the case if the load were largely inductive. In this case the conduction period would extend into the negative half cycle. At the completion of the conducting period the negative voltage returns the device to the off state by clearing charge carriers from the conducting zones.

Hence the device operates as a controlled switch either on or off. The on period is variable depending upon when the voltage E_{GC} is applied relative to the driving sine wave. In the on state the voltage drop across the valve is very small and the device can be considered to be a short circuit.

In duality contrast to the mercury arc rectifier the thyristor has a current sensitive firing characteristic. Thus it must be triggered from a low impedance voltage source due to its low input impedance.

The controlled load voltage variation by means of a delay angle is referred to as grid or gate control of the mercury arc rectifier or thyristor.

APPENDIX B

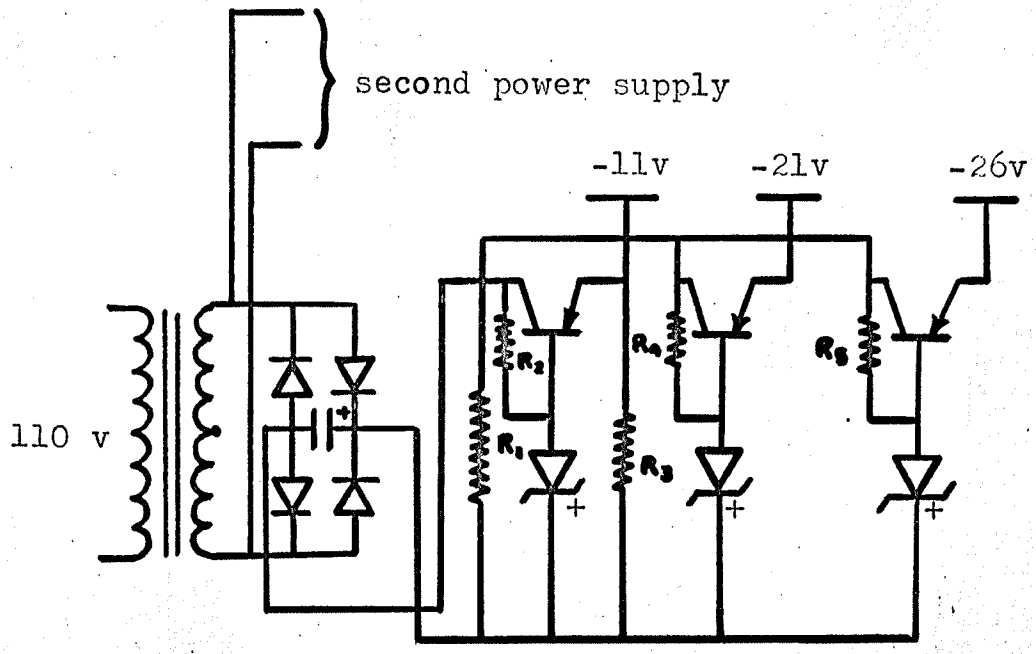
Schematic Diagram

Figure B.1 is a schematic diagram of the complete model system. It has been drawn in accordance with the block diagram contained in the introduction. The drawing is included in a pocket in the back of the thesis.

APPENDIX C

Pulse Circuit Power Supplies

The circuit for the power supply employs a full wave rectifier bridge. The bridge is fed from a 110 : 40 volt transformer. The rectified voltage is impressed across a resistor capacitor combination. The 1000 ufd. electrolytic capacitor maintains the peak rectified voltage of approximately 50 volts. This voltage is regulated to obtain three independent levels. The bias resistors for the transistors were selected in accordance with the expected current demand on each of the three stages. PNP transistors were used since the desired voltages were negative. The reference zener diodes were connected to obtain the proper polarity. A resistor was connected from the -11 volt bus to ground since conventional current could not pass from from ground through the PNP transistor. The -11 volt bus is joined to the emitters of transitors T_3 and hence must supply current when these fire. Figure C.1 is a schematic of the regulated power supply. An identical unit not shown is connected to the secondary of the transformer as indicated.



R_1 4.7K
R_2 1.5K
R_3 820 ohms
R_4,R_5 680 ohms
capacitor 1000 ufd electrolytic

Figure C.1 Regulated power supply

APPENDIX D

Commutation Voltage Dents

To understand the mechanism by which commutation voltage dents are produced consider Figure D.1.

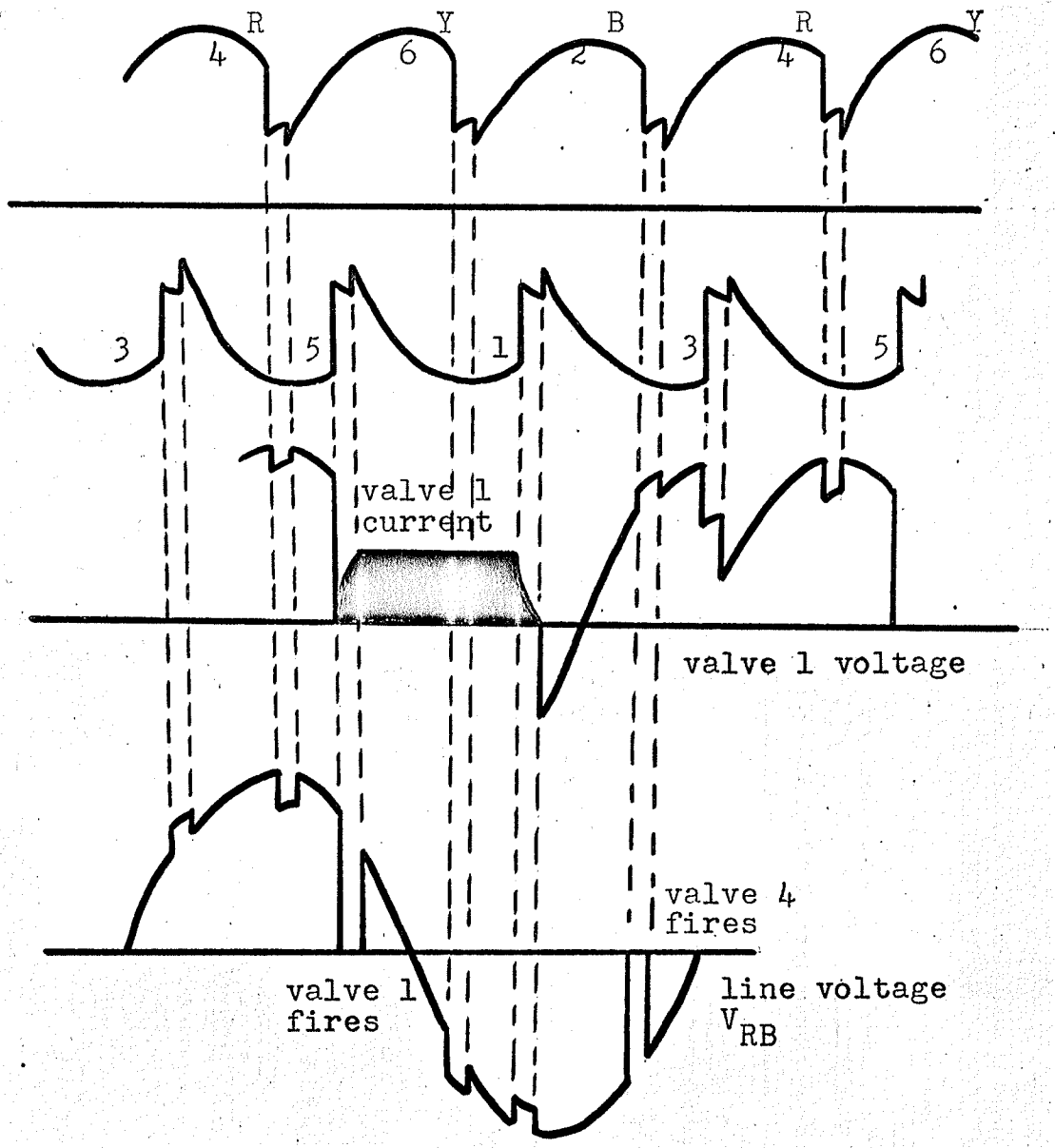


Figure D.1 Effects of voltage dents

As mentioned in Chapter 2 the interval for which commutation occurs (angle u) results in virtually a short circuit between two phases. The voltages between which the dc output is measured follow the median of the phase voltages comprising the shorted line voltage since the remaining two line voltages must adjust so that no component exists in the direction of the shorted voltage. ie. The original magnitudes must be multiplied by the sine of 30^{o}. The voltages must adjust since the transformer secondary neutral is not utilized. The median lines are indicated in Figure D.1. As a result both the valve and line to line voltages must be modified to account for these changes when they occur. Note that the line voltage drops to zero when the valves connected to any one phase fire and commutation is effected. Six dents appear for one cycle of line voltage since there are six valves firing during this interval.

The analysis has been shown for inverter operation but the same can be applied to that of the rectifier.

An important observation should be made concerning the current through any valve when winding reactance is considered. Refer to Figures D.1 and D.2. It can be seen that a valve conducts for an angle u past 120^{o}. This is the angle during which the valve current falls to zero. However, as the current in the valve ceasing conduction decays the current in the valve initiating conduction rises. The sum of these currents during the interval u is I_d. Hence

even though a valve conducts for more than 120^{o} it is convenient to refer to this period as being 120^{o} because the area under the valve current waveform is equal to that under a rectangular pulse of height I_d and width 120^{o}.

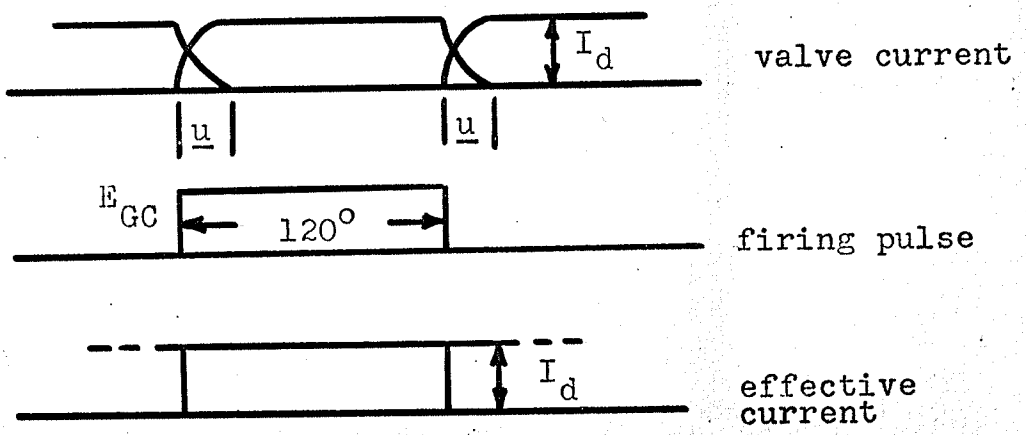


Figure D.2 Valve conduction

APPENDIX E

Parts List

Note: Model numbers were not available for all parts listed below.

Phase Shift Circuits

12 - 100 ohm, 10W resistors
2 - ganged 3 element, 2W variable resistors
6 - 30 ufd. capacitors

Isolating Transformers

6 - 120/240ct power supply transformers

Pulse Circuits

2 - 500K, linear taper, 2W potentiometers
24 - 4.7K, ½W resistors
12 - 3.3K, " "
36 - 1K , " "
12 - 2.2K, " "
12 - 6.8K, " "
12 - 10K , " "
12 - Hammond driver transformers, No. 145G
36 - Motorola 6518 PNP transistors
24 - silicon diodes
12 - 1.5 volt "C" size batteries
6 - 470 pfd capacitors

Limiting Resistors and Additional Winding Reactance

3 - 20 ohm, 10W resistors
3 - 4 ohm, 10W resistors
6 - Hammond 60 mh. chokes, No. 159zc

Rectifier and Inverter Bridges

12 - 25 volt, 1.6 amp(rms), General Electric No. C5A (Jedec No. 2N2324)
2 - 1 ohm, ½W resistors

Transmission Line

2 - 2.5 ohm, ½W resistors
2 - 9 h. chokes

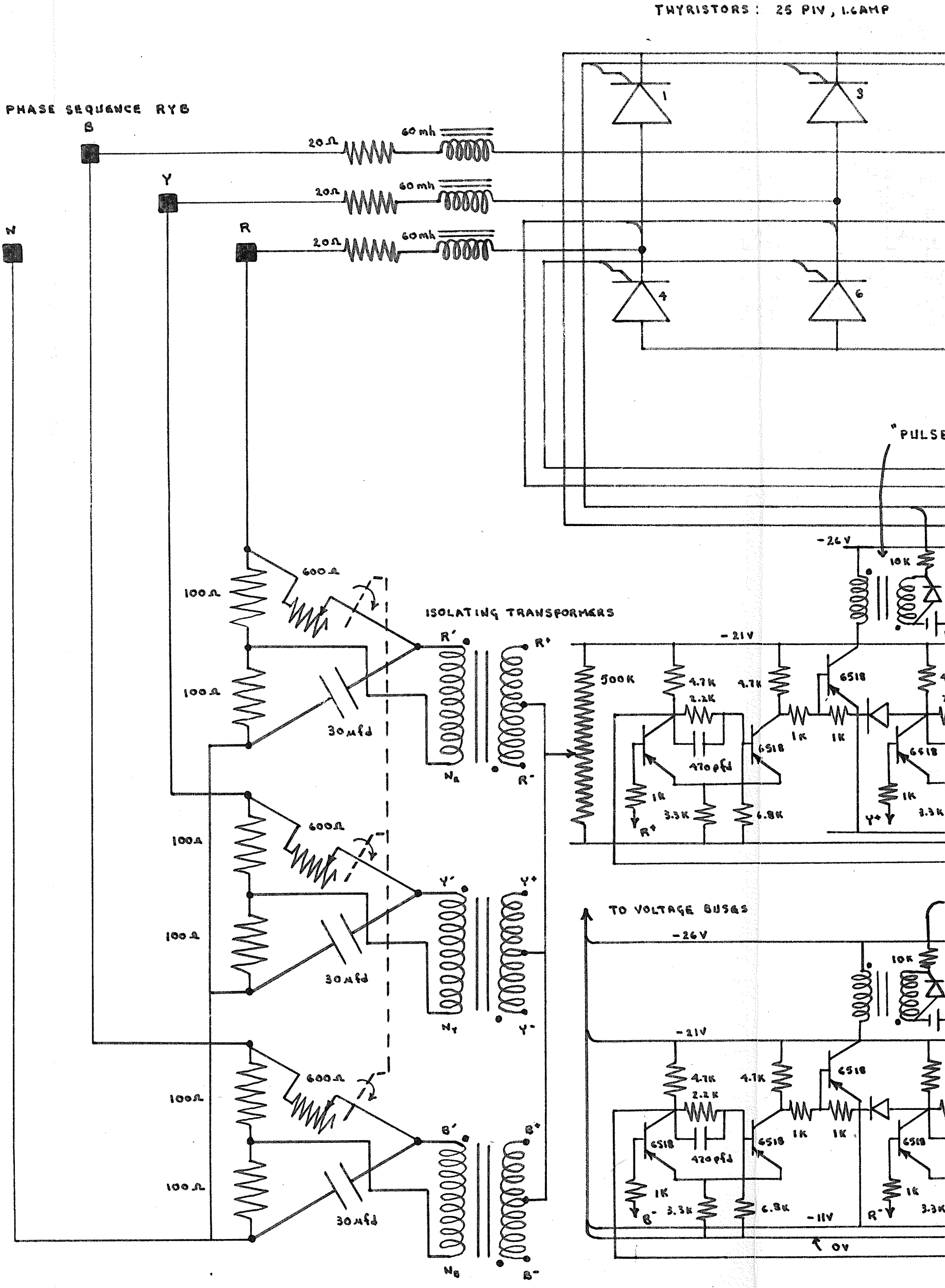
Power Supplies

2 - 4.7K, ½W resistors
2 - 1.5K, ½W resistors
2 - 820 ohm, 2W resistors
4 - 680 " " "
2 - 26 volt, 1 amp zener diodes
2 - 22 " " " " "
2 - 12 " " " " "
2 - 1000 ufd., 50WV electrolytic capacitors
8 - 5 amp power diodes
1 - 110/20ct power supply tfr., Hammond No. 167J25

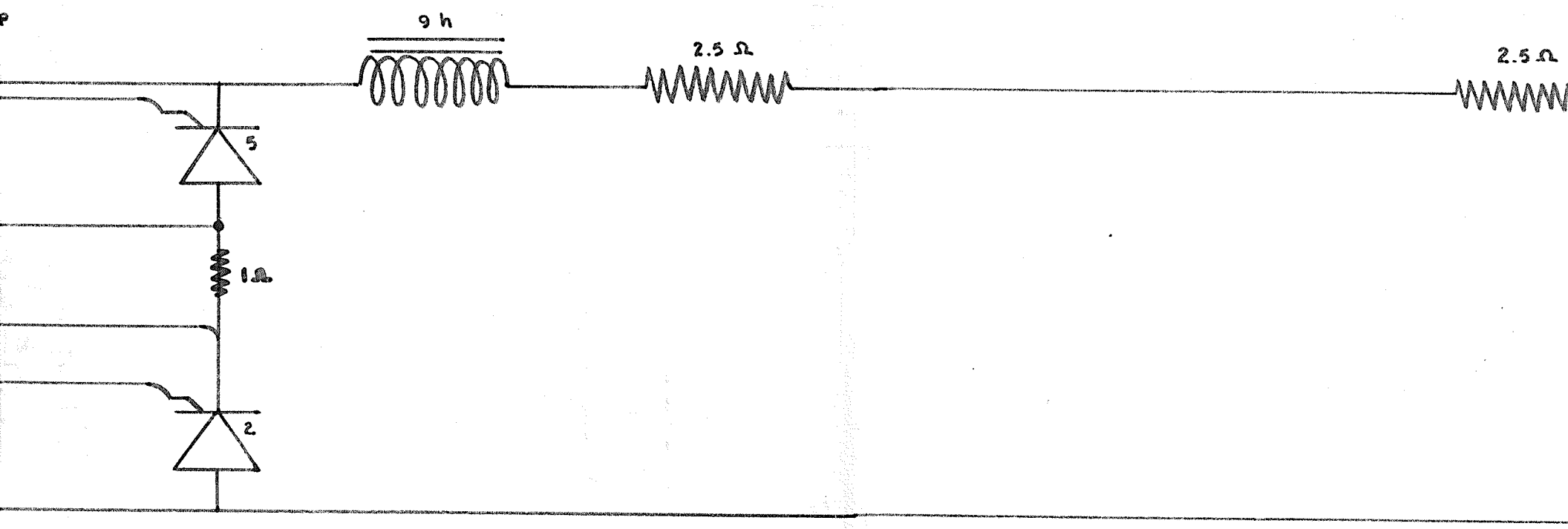
Miscellaneous

metal cabinet, aluminum panel engraved to represent the system, toggle switches, input jacks, miscellaneous hardware for mounting the components

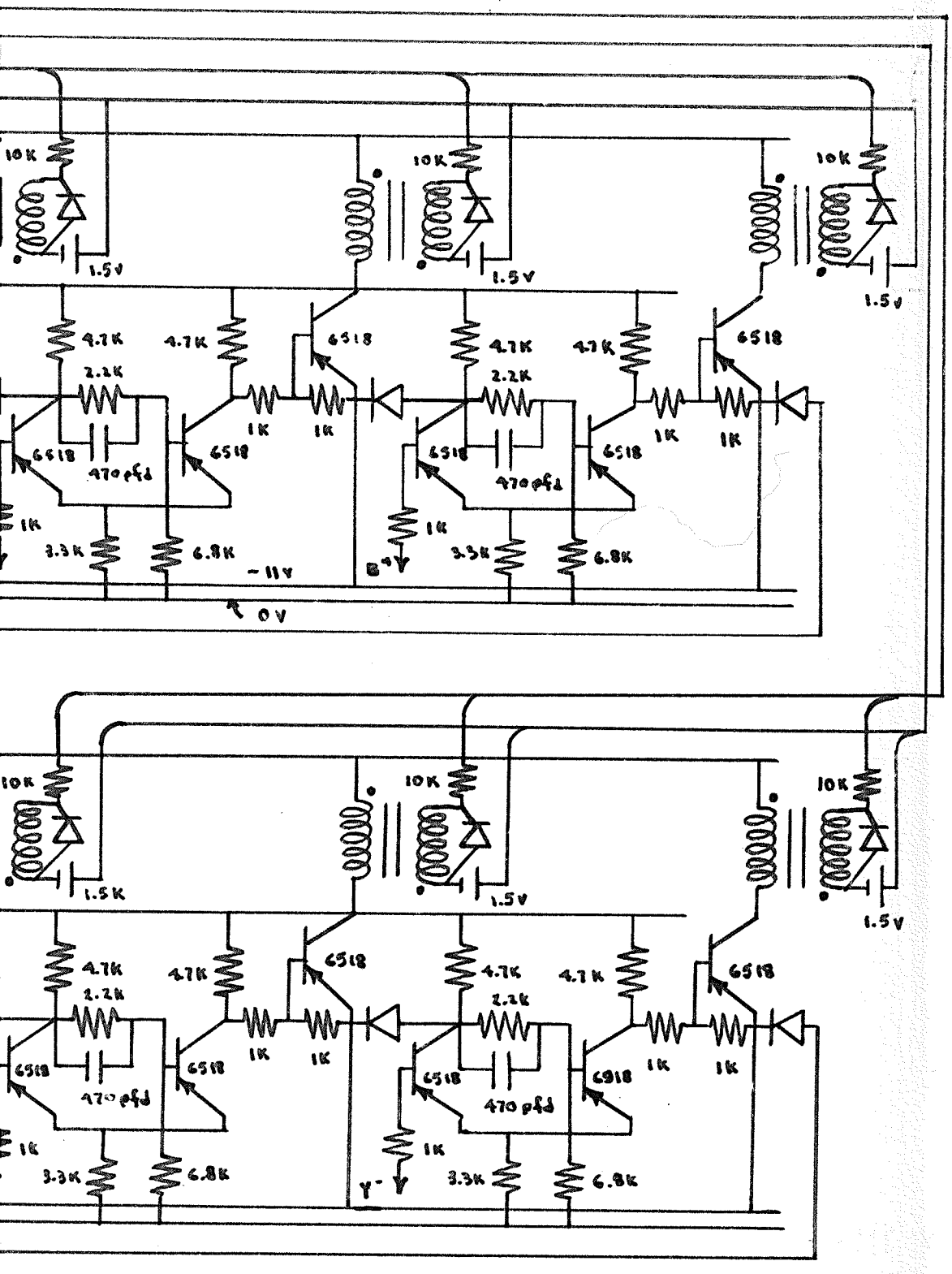
NOTE: PULSE CIRCUITS ARE SUPPLIED FROM INDIVIDUAL POWER SUPPLIES. SEE APPENDIX C.



APPENDIX B SCHEMATIC DIAGRAM

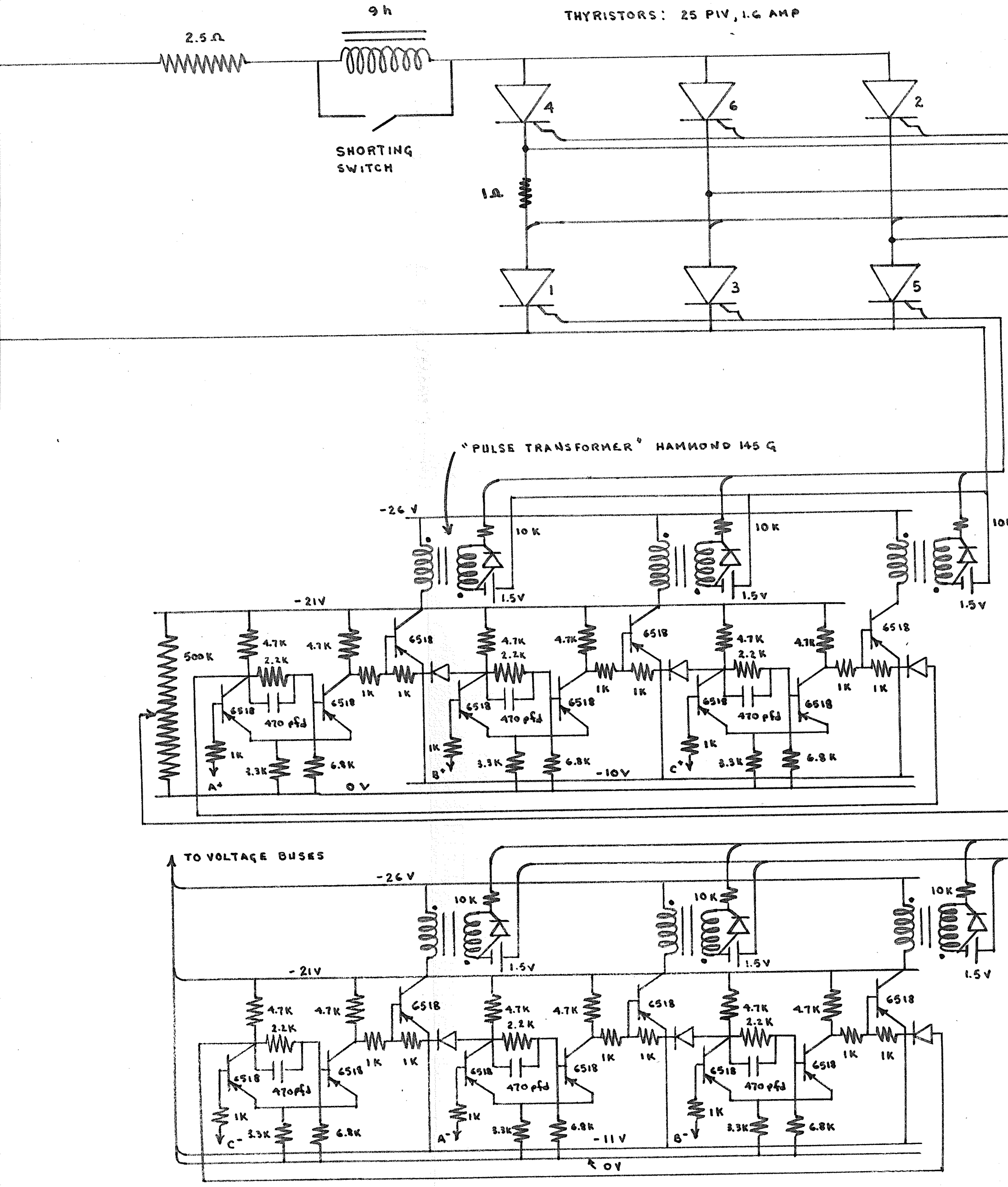


"PULSE TRANSFORMER" HAMMOND 145 G



AGRAM

NOTE : FOR COMPONENT DETAILS REFER TO APPENDIX E



S REFER TO APPENDIX E

CORS: 25 PIV, 1.6 AMP