DISCRETE ANALOG SIMULATOR FOR CONTROLLABLE VARIABLE TIME DELAY

A Thesis

Presented to

The Faculty of Graduate Studies

The University of Manitoba

In Partial Fulfillment

of the Requirements to the Degree

Master of Science in Electrical Engineering

by

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January [illegible], 1969

ABSTRACT

Discrete Analog Simulator For
Controllable Variable Time Delay

An electronic simulator is designed and built that is capable of delaying a signal (which might be a function of "state"). Intended for ± 10 volt analog computer applications, the device utilizes a magnetic core memory, presenting at its output terminals a quantized, discrete-time representation of the delayed input. Owing to its electronic speed, the device imposes little restriction on bandwidth, while high accuracy is maintained with a resolution of 1 part in 1023. Also, within bandwidth limitations, no restriction is placed on the rate-of-change of delay (i.e. a monotonic increasing delayed argument is not required).

Information is "written" into the memory (1024 10-bit words) at fixed intervals of time in a count-down sequence, each "write address" being interrogated once every 1024 counts. At each interval, a word (corresponding to the delayed input) is "read" non-destructively from memory at an address differing from the present write address by a number proportional to the required delay. (Analog-to-digital and digital-to-analog convertors perform the required interfacing with the memory.) Four ranges of delay are provided by selecting the appropriate sampling frequency.

The Variable Delay Simulator (VDS) is tested for constant delay and for a sinusoidally varying delay. It is concluded from the excellent results that useful information will be obtained with the VDS, once the performance limits of the device are established. Possible sources of limitations are discussed and recommendations for improving system versatility made.

ACKNOWLEDGMENT

I wish to thank my wife, Marlene, for her assistance in typing this thesis. I am also grateful for the advise of my thesis advisor, Professor R.A. Johnson, who originated the basic simulation technique and assisted me in every phase of the project. The assistance provided in the earlier stages by Glen Marston, of Digital Equipment of Canada is also appreciated. Also, financial support of this project provided by the Defence Research Board of Canada is greatly appreciated.

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Chapter 1: INTRODUCTION

The Problem

The occurrence of pure time delays in various physical processes (e.g. in: control systems, biological processes, economic studies) is well known. Systems of this type have received considerable attention of late, particularly where delay varies with time or, in a control sense, as a function of the "state" of the system. Although a great deal of material has been accumulated on the mathematical side, little has been done to illustrate the qualitative behaviour of time-variable delay systems. It is for this reason that the need for an accurate, versatile simulator for variable time delay arose.

Possible Types of Simulators

Prior to the classification of variable delay by Seddon[1] most simulators were of the "Pipe" variety, variable delay being achieved by controlling the velocity (v_m) of an incompressible medium carrying the input signal from a fixed "write" position over a fixed distance to the output at the "read" position.[1] (The simulator used by Seddon utilized a constant medium velocity, a fixed "read" position, and a variable "write" position.) The storage media used include paper chart, magnetic tape, capacitor store, or magnetic core. However accurate these systems could be made, they all were incapable of reproducing state-variable delay.

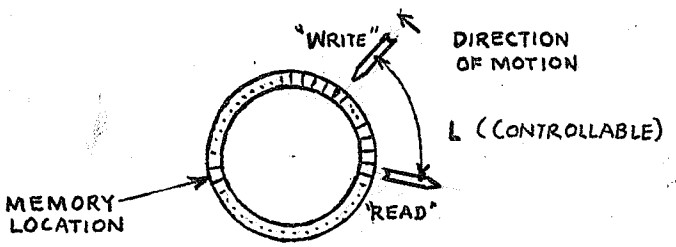
[1] No. in brackets( ) refers to Bibliography, p. 30.

Fortunately, the problem of what form the simulator should take was resolved.[1], [2] Only with a variable "read" position (other velocities constant) would the delay be proportional to the read position (relative to the write position) at that time.

Basic Design Philosophy

Since the bandwidth limitations normally associated with mechanical devices were considered too severe, an electronic simulator using a magnetic core memory was decided upon. Because of the organization of the memory stacks available, the following technique was decided upon (with the core memory represented as a ring for illustration purposes):

Figure 1-1 Simulation Technique



The write head advances at a constant rate (f), one location at a time. A word is read out at a read position, L positions "behind" the write head, thus obtaining the delayed input. If L is controlled in some way, the delay function will be given by:

$$\tau(t) = \frac{L(t)}{f}$$

A system composed of modules purchased from Digital Equipment Corp. (hereafter referred to as DEC) was selected for the following reasons:

(1) Design problems and hence design time were reduced

(2) Fast Analog - to Digital Convertors (required to maximize the bandwidth of the simulator) as well as a complete magnetic core storage system were available as standard plug-in units.

(3) Complete system modularity resulted in better organization as well as more efficient maintenance.

(4) Interconnection became a simple matter of wire-wrapping, facilitating future modifications.

In general, the proposed system seemed to afford simplicity of design without sacrificing speed and accuracy. In addition we could expect to have a workable system in a reasonable period of time.

Chapter 2: THE SIMULATOR

Physical Description

The VDS consists of suitably interconnected DEC modules housed in a cabinet 21 in. wide, 29 in. high and 13 in. deep. Rear access to the modules is provided by a hinged door, while removable panels in front permit inspection of the wire-wrapped connections.

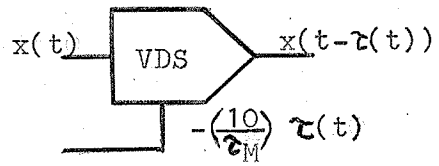
The unit is designed to mate with ± 10 volt analog computers, although it is to be used principally with the EAI 580 Hybrid Computer. Although at the time of this writing the control panel details are unfinished, it is anticipated that analog input connections will be made via coaxial connectors.

Simulation Technique

The signal to be delayed, $x(t)$, is sampled at regular intervals (determined by a clock), converted into digital form and stored in a core memory, each new sample being "written" into a location whose address (represented by a 10-bit binary number) is one less than that of the previous sample. Immediately following the writing process, a sample is read out of memory at an address obtained by adding to the current write address a number "proportional" to the delay signal τ. The sample is loaded into a digital-to-analog convertor to obtain the delayed analog signal at the convertor's output terminals.[1]

[1] The reader will note that, while $x(t)$ and $\tau(t)$ are "continuous functions of time, the output signal is a quantized, discrete function of time. However, it will be referred to as $x(t-\tau(t))$ for simplification. The proposed simulation diagram symbol for the VDS appears in Fig. 2-1.

Figure 2-1 Computer Symbol



(τ_M - maximum delay for a particular clock - rate setting.)

Specifications

1. Memory: 1024 10-bit words, non-destructive read.

2. Delay: - maximum delay using 1024 words : 100 sec.

- minimum delay using 1024 words : 0.1 sec.

The delay range is fixed by the Clock - Rate Selector Switch which divides the basic clock rate of 10,230 Hz.[2] in 3 decades to 10.23 Hz., thus providing 4 delay ranges.

The rate of change of delay is restricted only by the limitations of the simulator itself.

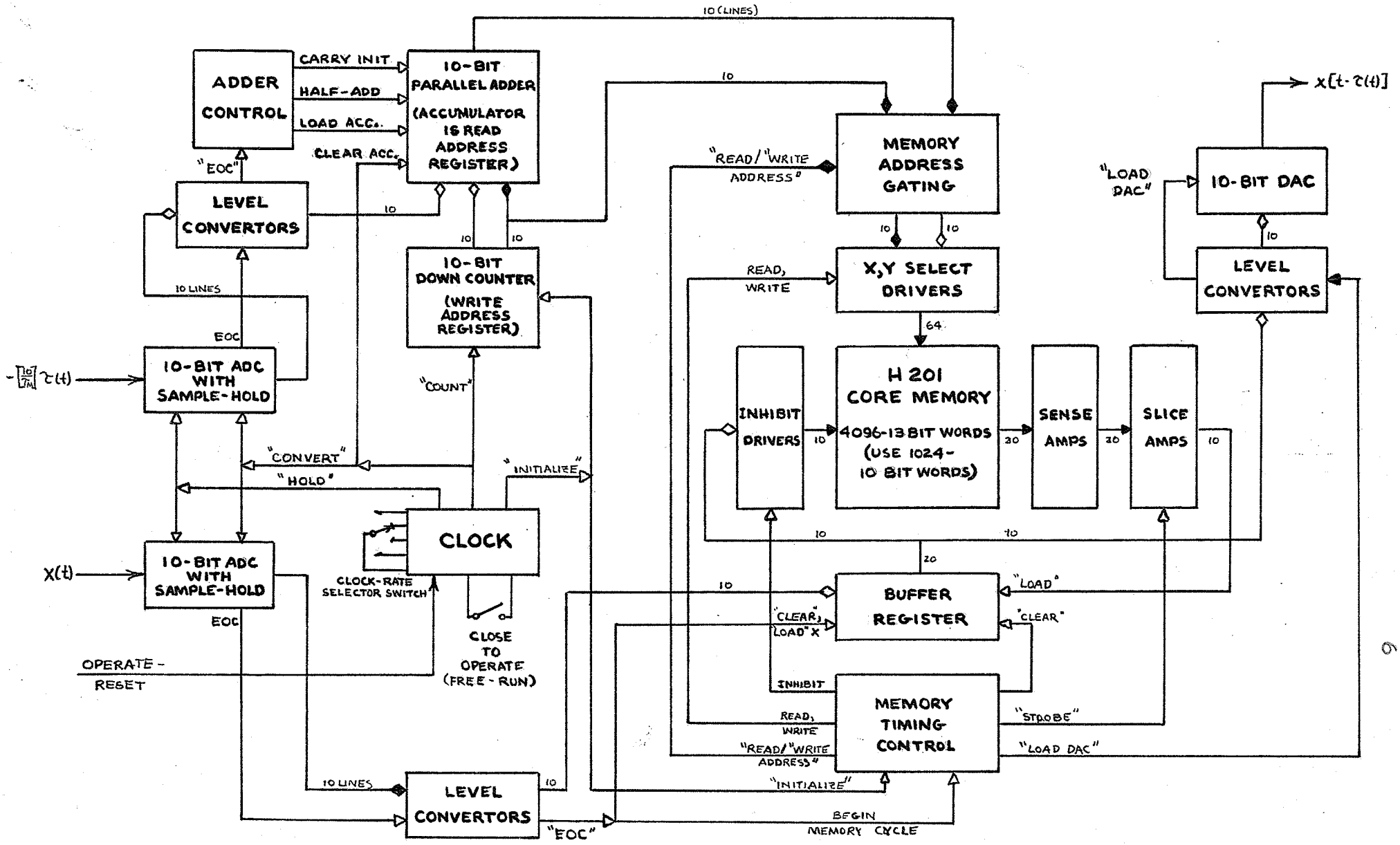
3. Control: The clock is started (Operate) and stopped (Reset) by manual control (single throw switch) and an external analog signal between +10 and -10 volts. When placed in the Operate mode manually, theVDS is insensitive to the analog control.

4. Inputs: The signal to be delayed, x(t), is in the range $(-10^V,+10^V)$, while the delay signal is in the range $(-10^V, 0^V)$. Both signals must be supplied from a source whose output impedance is less than 10 ohms.

[2] If a constant delay of .1 sec. utilizes the entire memory the sampling frequency, f, must be such that:

$$f = \frac{\text{no. of sampling intervals betw. read and write addresses}}{0.1} = \frac{1023}{.1} = 10230\text{Hz.}$$

FIGURE 2-2 : SYSTEM BLOCK DIAGRAM



5. Output: Quantized representation of $x(t-\tau(t))$ in the range $(-10^V, +10^V)$. The resolution (quantization) of the signal is 10 MV.

Organization

1. System Block Diagram (Figure 2-2)

The basic structure is broken down into a number of subsystems whose functions can be detailed independently. The diagram illustrates the major signal flows as well as the type of function performed.

Figure 2-3 Signal Classification

Pulse, positive going

Pulse, negative going

Level, positive for assertion

Level, negative for assertion

2. Subsystems

To make the Sequence of Operations section more concise, the operation of each subsystem is outlined below:

2(a) Analog to Digital Convertor (ADC)

A 10-bit binary number proportional[3] to the analog input signal is available within 10 μsec. after a "Convert" pulse is received.[4] In order to improve the accuracy of the convertor, it is preceded by a sample-hold unit which holds the input constant over the entire conversion period.[5]

(b) Clock

The clock emits a uniform pulse train at a frequency determined by the position of the Clock-Rate Selector switch (to give the desired range of delay), the first pulse coinciding with the Operate command. (In reset no pulses are generated). It also governs the initial state of the system.

(c) Down Counter

The counter consists of 10 flip flops representing a ten-bit binary number. Each "Count" pulse decreases this number by one, in a cyclic manner (i.e...,3,2,1,0, 1023,1022,..., etc.)

[3] For input voltage E ϵ (0^V, 10^V), 0^V - 000.....0 = 0
$+10^V$ - 111.....1 =1023

[4] The method of conversion is "successive approximation", outlined on pp. 362-363 of (7).

[5] The improvement afforded by the sample-hold will be discussed in Chapter 4.

(d) Parallel Adder

At the conclusion of the following sequence of commands issued by the Adder-Control, the adder Accumulator contains the sum of the two digital inputs:

(i) Load Accumulator (Acc.)

(ii) Half-Add

(iii)Carry initiate

The maximum size of the 10-bit sum is 1023. The next greatest sum is 0 to 1,2,.... .

(e) Memory : Storage and Retrieval

(i) Core Memory: Address selection is on a co-incident current basis. A Read current clears all cores (each core representing one bit of a 10-bit number) in the address selected to zero while a write current sets all selected cores to one except where an inhibit current acts to oppose it.

(ii) Read/Write Drivers (x,y selection) - decode the memory address to select one x and one y line intersecting at the address to be interrogated.

(iii) Inhibit Drivers - decode the digital input, providing the current necessary to prevent the writing of one's and thus store the correct bit pattern.

(iv) Memory Output: The signal induced on a sense winding during a Read process (through those cores which were in the "one" state) is amplified (Sense Amps) and sliced (Slice Amps) to produce a

standard pulse, provided the "Strobe" input is "true". There are ten sense windings, one for each bit of the stored word.

(f) Memory Control Functions

(i) Memory Address Gating - a set of logical gates which present either of two digital inputs on command ("Read Address" or"Write Address").

(ii) Buffer Register - stores the contents of either binary input depending upon the load command received. By converting the pulsed information from the memory to constant voltage levels, it permits the number just read to be re-written (non-destructive read).

(iii) Memory Timing Control - governs the operation of the memory by issuing the sequence of commands necessary to write in or read out a word. It determines which address is to be interrogated (i.e. either "Read Address or "Write Address").

(g) Level Convertors

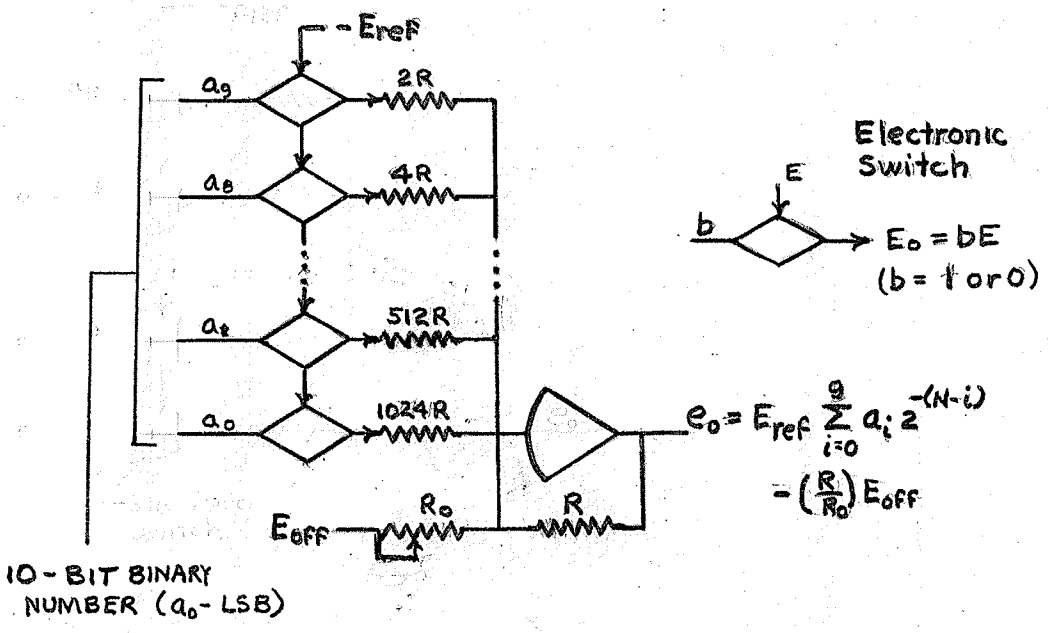
Since the system as a whole incorporates devices which operate under different logic levels (i.e. those levels which represent either "1" or "0"), it is necessary to convert from one scheme to another for proper interconnection. This service is performed by level convertors.

(h) Digital to Analog Convertor (DAC)

As the name implies, this device produces an analog output proportional to the digital number at its input. The output voltage changes each time the DAC receives a "load" signal.

In contrast to an ADC, the DAC reproduces its input without error, (other than the normal error one associates with analog devices). The basic decoding scheme (assuming a 10-bit system) is as follows:

Figure 2-4 Digital-to-Analog Convertor



Sequence of Operations [6]

Assume that the system is initially at rest (Reset mode). When the clock is switched to the Operate mode, the following sequence of events takes place:

(a) An "Initialize" pulse is immediately issued by the clock to set the write address register and memory timing control to the proper initial state.

(b) Each clock timing pulse increments the "Write Address Register" (down counter) and "clears" the adder accumulator for proper control.

(c) Each timing pulse switches the Sample - Hold (S/H) units to the "hold" mode.[7] Once "hold" is assured, conversion is initiated ("Convert"). At the end of the conversion process, each ADC issues an "EOC" pulse which triggers the respective S/H unit to the "track" mode.

(d) The "EOC" pulse produced by the A/D convertor for $(-10/\tau_M)\tau$ initiates the addition operation that produces the "Read Address" by adding the digitized delay function to the write address.

(e) The "EOC" pulse produced by the convertor for x(t) loads the digitized x into the "Memory Buffer Register" and initiates one cycle

[6] The reader is referred to the System Block Diagram, Figure 2-2.

[7] In "Reset", the S/H units are held in the "track" mode in order to record the initial values of the variables to be converted.

of the "Memory Timing Control" which:

(i) clears the contents of the memory location specified by the write address register to zero by performing a "read" operation without an accompanying "strobe" (thus nothing is actually read out);

(ii) writes the contents of the buffer register into the memory location which has just been cleared;

(iii) reads the contents of the memory location specified by the Read Address Register into the buffer register and into the D/A Convertor;

(iv) writes the contents of the buffer register back into the memory location which has just been read.

Notes:

1. Consider the problem of converting a bipolar signal, namely x(t), into an unsigned digital number [illegible] here.

Since the A/D convertor accepts only positive inputs (see Specifications), we include an offset voltage with the S/H for x(t) as well as a gain of $-\frac{1}{2}$ (S/H units invert) in order to present the following function to the convertor:

$$z(t) = -\tfrac{1}{2}(x(t) - 10) \qquad \text{where} \quad -10 \leq x \leq 10 \Rightarrow 10 \geq z \geq 0$$

A logical inversion of z (every bit is complemented) produces:

$$\overline{z}(t) = I - z(t) \quad \text{where } I = z_{MAX}$$

Converting to analog form (via the DAC), we have the delayed output:

$$\begin{aligned} \overline{z}(t-\tau) &= 10 - z(t-\tau) \\ &= 10 + \tfrac{1}{2} (x(t-\tau) - 10) \\ &= \tfrac{1}{2} (x(t-\tau) + 10) \end{aligned}$$

Thus if we incorporate a gain of 2 and a suitable offset voltage in the DAC, we get $x(t - \tau(t))$.

2. The need for a non-destructive read capability is not immediately obvious, since suitable restrictions on $\tau'(t)$ [8] should eliminate the possibility of reading a piece of history twice:

For $t - \tau(t)$ monotonic increasing,

$$\tau'(t) < 1$$

However, even for constant delay, the possibility is still present. Consider, for example, a constant τ which lies midway between two quantization levels. Assume that, due to noise first the lower state and then (on the next count) the higher state is selected by the ADC. Since the write address has decreased by one in the process, the write address stored in the adder will not change, resulting in the reading of a false zero (the location having been cleared by previous "read").

When the effect is compounded over a period of time, the degradation of the output signal becomes intolerable, necessitating a non-destructive read.

[8] ' denotes differentation, i.e. $\tau'(t) \equiv (d/dt)\,\tau(t)$

Chapter 3 : EXPERIMENTAL EVIDENCE OF SYSTEM PERFORMANCE

Two tests were devised to give some quantitative indication that the simulator was functioning properly. One was an example of fixed delay[1] to check the static accuracy of the system. The second example incorporated a sinusoidally varying delay.

Example 1 : Constant Delay

Examine the following nonlinear differential - difference equation (dde):

$$f'(t) = - \alpha f(t-1)(1 - f^2(t)) \quad \ldots\ldots\ldots\ldots\ldots \quad 3\text{-}1$$

Consider sn (u,k) (Jacobian Elliptic Function)

$$\frac{d}{du}sn(u,k) = cn(u,k)dn(u,k)$$
$$= cd(u,k)dn^2(u,k)$$
$$= - sn(u-K,k)\ (1- k^2sn^2(u,k))$$

Now if we set

$$f(t) = k\ sn(u,k) \quad \text{with } ct = u$$
$$f'(t) = - c\ f(t-\tau)\ (1 - f^2(t))$$

wherein $\tau = K/c$.

Since $\tau = 1$ and $c = \alpha$ for identification with 3-1 the solution is

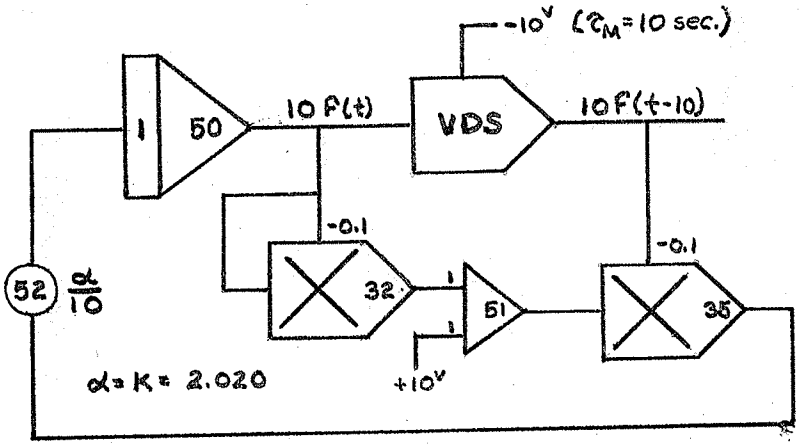
$$f(t) = k\ sn(Kt,k) \quad \text{with } K = \alpha$$

[1] Contributed by Prof. R.A. Johnson (University of Manitoba)

Analog Simulation

A value for K was chosen such that comparison with tabulated results [3] could easily be made. The system equations were time-scaled (slowed) by a factor of 10 in order to minimize tracking errors by the plotter. An EAI 580 hybrid computer was used in conjunction with the VDS and a Houston Model HR-101 X-Y plotter.

Fig 3-1 : Simulation Diagram [2]



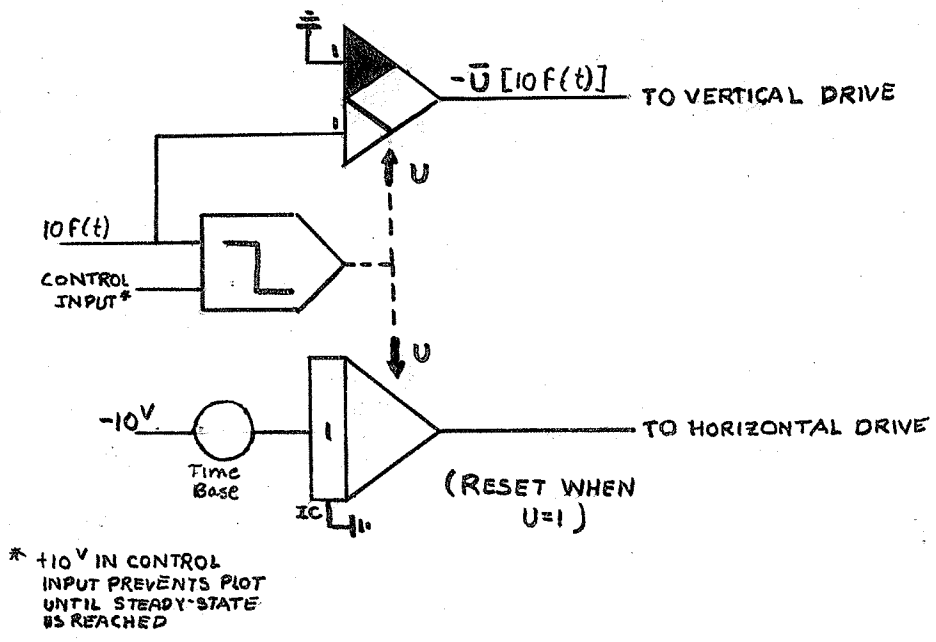
Scaled Computer Equations

$$f'(\lambda) = -\alpha f(\lambda-1)(1 - f^2(\lambda)) \qquad \lambda = t/10 = \text{computer time}$$

$$-10f'(t) = \frac{\alpha}{10}\left\{-\frac{1}{10}[10f(t-10)]\left[-10 + \frac{1}{10}(10f(t))^2\right]\right\}.$$

[2] See Appendix 2. for explanation of symbols.

Fig. 3-2: Plotting Technique



A plot of f(t) vs. time was obtained (Graph I) and a series of calculated values (f(t) = ksn(Kt,k)) superimposed as follows:

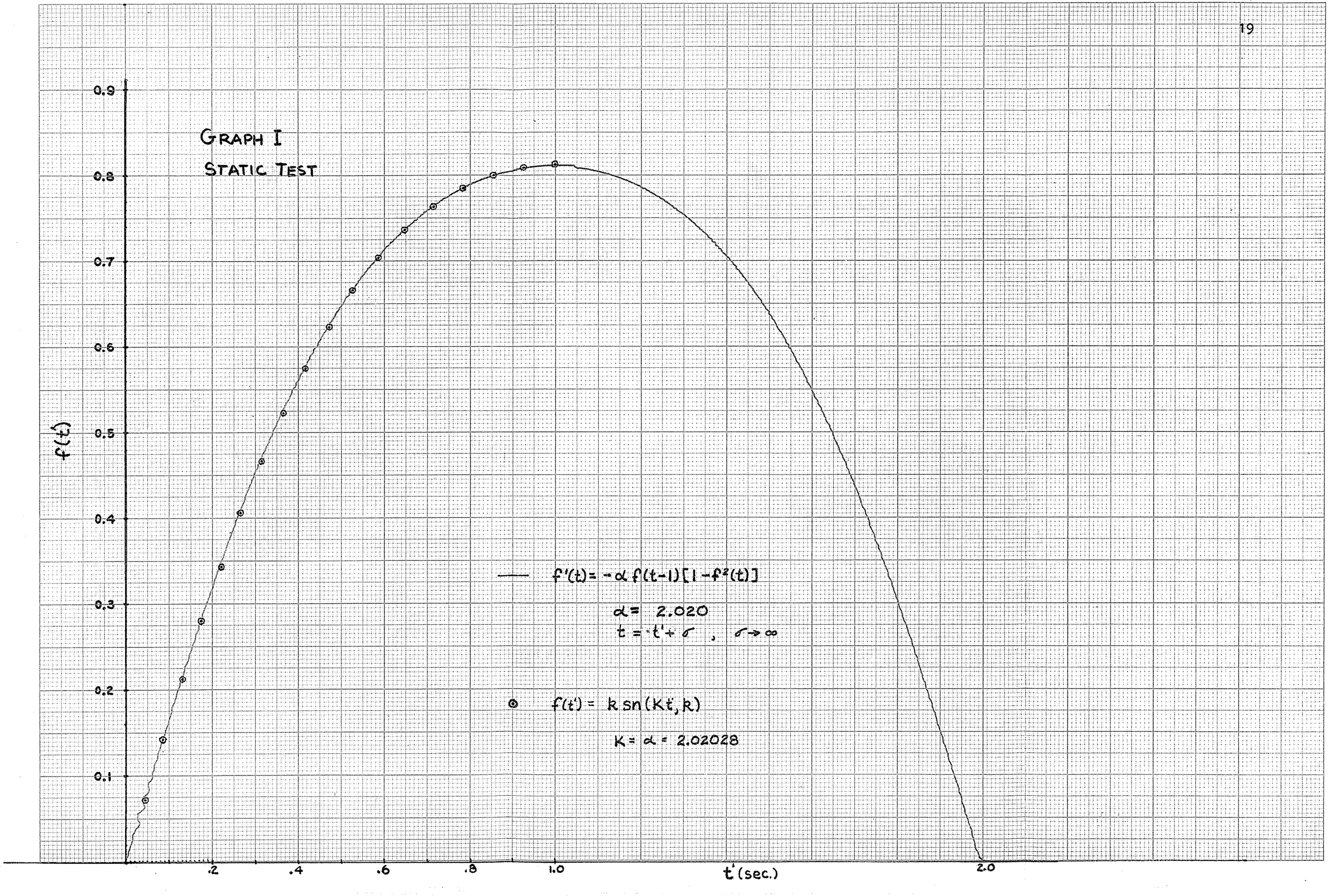
For $K = 2.02028$, $\quad k = \sqrt{.66} = .8124$

$$u = \int_0^{\phi} (1-k^2\sin^2\theta)^{-\frac{1}{2}}\, d\theta \; ; \quad K = \int_0^{\frac{\pi}{2}} (1-k^2\sin^2\theta)^{-\frac{1}{2}}\, d\theta$$

The procedure is to select values of ϕ at 5° intervals, find the corresponding u in tables [3] ($k^2 = .66$) and the value of $\mathrm{sn}\,u = \sin\phi$. Since sn u is symmetric (as is $\sin\phi$), the range of ϕ need only be $(0, \pi/2)$.

Properties of the delay system are illustrated in Graph I(a), page 19 a., for the constant delay case considered.

GRAPH I
STATIC TEST



—— $f'(t) = -\alpha f(t-1)[1-f^2(t)]$

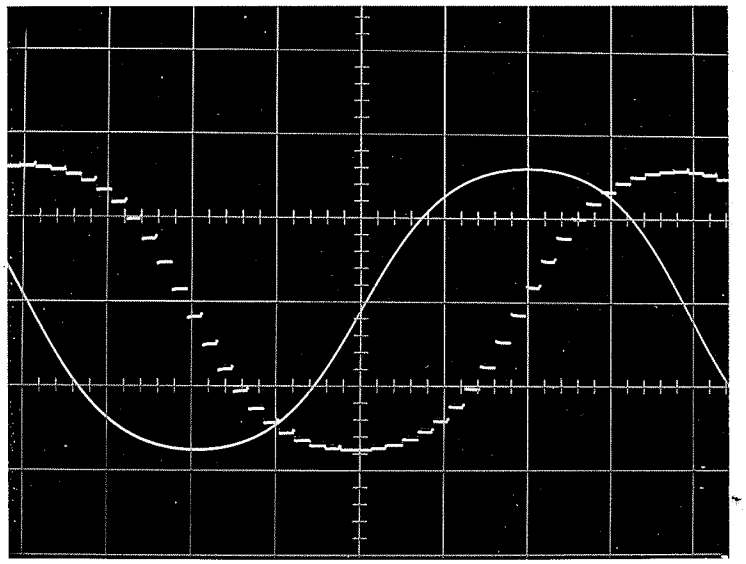
$\alpha = 2.020$

$t = t' + \sigma$, $\sigma \to \infty$

⊙ $f(t') = k\,sn(Kt', k)$

$K = \alpha = 2.02028$

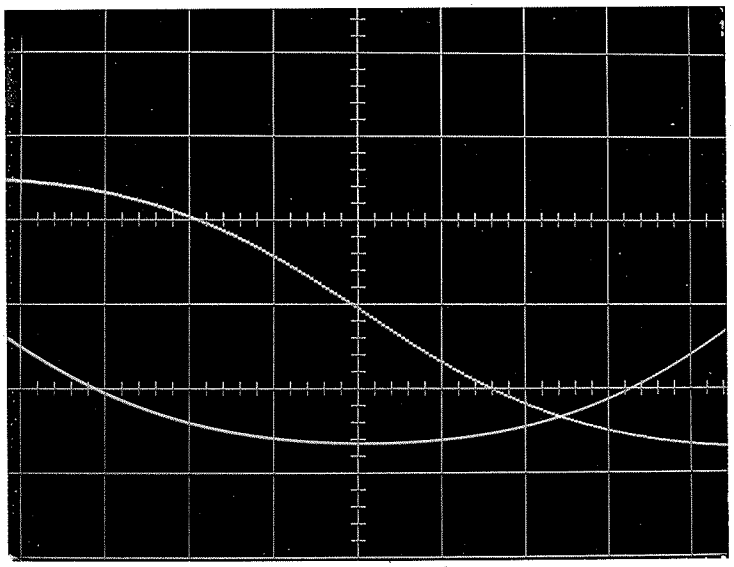
GRAPH I(a): VDS OPERATION



Horizontal:
.5 ms./cm.

Vertical:
2 volts/cm.

$\tau(t)$ = .001 sec., τ_M = .1 sec.



Horizontal:
2 ms./cm.

Vertical:
2 volts/cm.

$\tau(t)$ = .01 sec., τ_M = .1 sec.

Table 3-1 : Calculation of k sn u

ϕ°	u	t=u/K	k sn u
5	0.08734	0.0432	0.0708
10	0.17512	0.0867	0.1410
15	0.26379	0.1306	0.2103
20	0.35380	0.1752	0.2779
25	0.44564	0.2206	0.3433
30	0.53980	0.2672	0.4062
35	0.63682	0.3152	0.4660
40	0.73725	0.3649	0.5222
45	0.84167	0.4166	0.5745
50	0.95067	0.4706	0.6223
55	1.06483	0.5259	0.6655
60	1.18465	0.5864	0.7036
65	1.31052	0.6487	0.7363
70	1.44258	0.7141	0.7634
75	1.58058	0.7824	0.7847
80	1.72382	0.8533	0.8001
85	1.87098	0.9261	0.8093
90	2.02028	1.0000	0.8124

Results:

It is apparent from Graph I that agreement between experimental and theoretical results is excellent. A slight error in the period of f(t) (≈5%) is apparently due to a plotter malfunction in the x-drive at t ~ 1.05.

Possible sources of error (other than sampling error) include plotter calibration, quarter-square multipliers, and slight errors in pot setting and delay setting.

Example 2: Sinusoidally Varying Delay

A search of the literature revealed an example of variable time delay for which numerical results were available.[4] It concerns finding the mean value of the periodic solution to the following dde. as a function of the parameter k.

$$\dot{u}(t) = -u(t-1-k\sin\omega t) + \sin at \qquad \left(\dot{} = \frac{d}{dt} \right)$$

with $w = a = 2\pi$; $k \in (0,1)$

The reader will note that we expect a non - zero mean value for u(t) even though the input, $\sin 2\pi t$, has a zero mean value. Without actually calculating the mean values vs. k as Bellman did, in this preliminary study we will compare experimental results with the graph presented by Bellman.

Analog Simulation

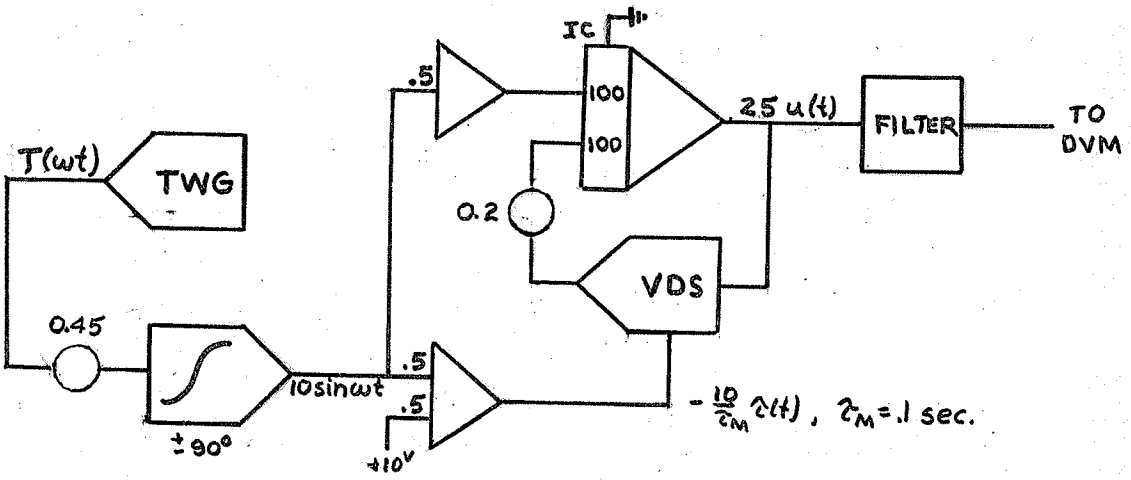
First, the system equation was time scaled by a factor of 2 to extend the operating range of $\tau(t)$ and thus minimize quantization errors in the digitized τ over the entire range of k. For the same reason, u(t) was amplitude scaled, within the limits of saturation.

Unscaled Equation:

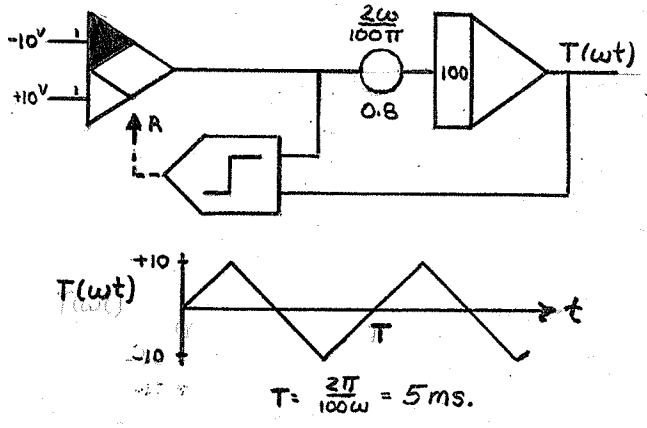
$$u'(\lambda) = -u(\lambda - 1 - k\sin 2\pi\lambda) + \sin 2\pi\lambda$$

λ = computer time.

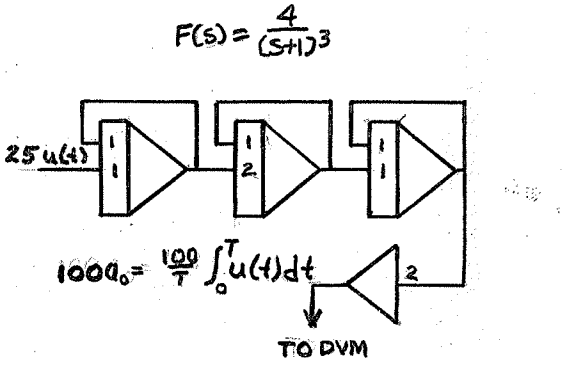
Figure 3-3 Simulation Diagram



(a) Complete Set-up



(b) Triangle Wave Generator (TWG)



(c) Measuring Circuit (Low-Pass Filter)

Scaled Equation:

$$-[25\dot{u}(t)] = 2[25u(t - .5(1+k\sin 4\pi t))] - 50\sin 4\pi t$$

wherein: t = real time $= \lambda/2$; $\text{Max}_K \tau(t) = \tau_M = 1$

The source of the sinusoid was an EAI sin/cos diode function generator driven by a triangle - wave generator as shown in Figure 3-3(b). Since $T(\omega t)$ was a computer-generated function, accurate frequency setting as well as easy system time scaling (in factors of 10, both on the 580 and the VDS) was achieved. (A simple sine wave produced by simulation of $\ddot{x} = -\omega^2 x$ suffers amplitude degeneration with time, due to leakage of integrator capacitors.)

A final time scaling by a factor of 10 was introduced in order to obtain an oscilloscope display of suitable persistence[3] (Tektronix - 453 dual-trace 'scope), to reduce the setting time of the mean value of $u(t)$, and to simplify the measurement scheme.[4]

A plot of a_o was made (Graph II) for suitable values of k (tabulated in Table 3-2). Bellman's results were transferred onto the same grid,[5] assuming that the following scales had originally been used:

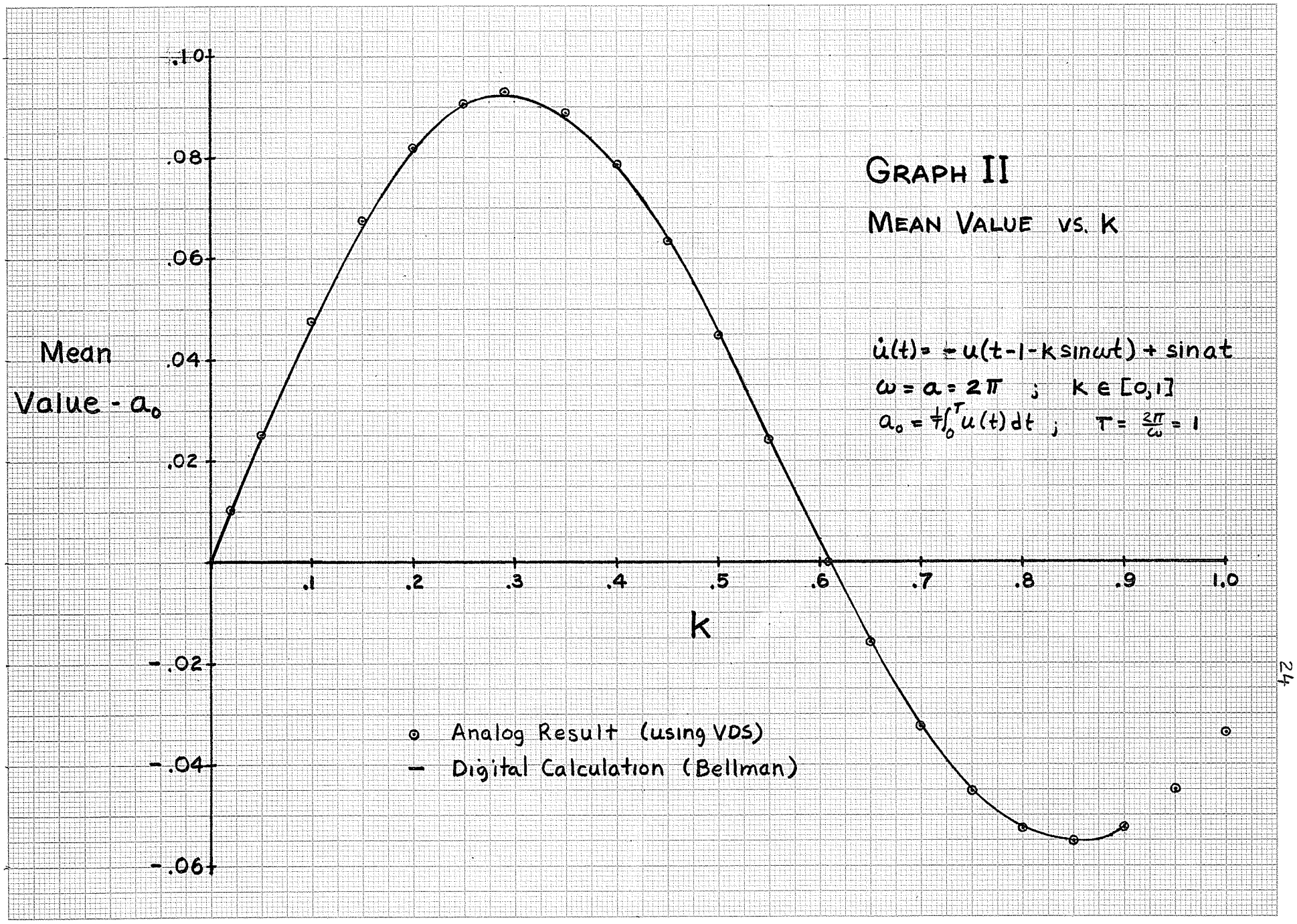
a_o : .02/cm.

k : .05/cm.

3. For the interested reader, sketches of the oscilloscope display of $u(t-\tau(t))$ were made (See Appendix) to demonstrate the distortion produced by a varying delay (since $u(t)$ was distorted very little, even at k=1, it was not reproduced.)

4. The increased frequency scale enabled the use of a primitive low pass filter (fig. 3(c)), easily simulated on the 580, to practically eliminate the higher harmonics so that a stable value of a_o could be read from the DVM.

5. Since the results were graphical, they were first transferred point-by-point, then expanded to the scale used for experimental values.



Results:

Table 3-2 : Variation in Mean Value with k

k	a_o	k	a_o
0.0000	0.0000	0.5000	0.4482
0.0200	0.1020	0.5500	0.2414
0.0500	0.2503	0.6087	0.0000
0.1000	0.4755	0.6500	- 0.1587
0.1500	0.6728	0.7000	- 0.3251
0.2000	0.8187	0.7500	- 0.4512
0.2500	0.9066	0.8000	- 0.5270
0.2900	0.9300	0.8500	- 0.5515
0.3500	0.8874	0.9000	- 0.5250
0.4000	0.7861	0.9500	- 0.4500
0.4500	0.6344	1.0000	- 0.3375

The results agreed quite acceptably with those of Bellman, although a precise comparison of the two could not be made owing to the lack of numerical data through Bellman's numerical technique.

General Remarks - Significance of Experimental Results

The results obtained in the static case demonstrated the remarkable accuracy of the device, although time prevented a study of the effects of reducing the sampling rate relative to snKt. It is anticipated that in most cases, time scaling the system equations (as was done for Ex. 1) will minimize this problem.

The close agreement between the two independent results obtained for the sinusoidal case, even taking into account graphical errors, is a good indication that varying delay is well simulated by the VDS (Note that Bellman's results, obtained via "digital integration", are also subject to error).

In conclusion, while it has been shown that the VDS provides a suitable approximation to variable delay, the results are by no means conclusive. A more rigorous evaluation of the capabilities of the simulator is certainly warranted.

Chapter 4: COMMENTS AND RECOMMENDATIONS

Tightening Bounds on System Performance

The next logical phase in the development of the simulator into a useful computer unit is to obtain some quantitative operating limits (e.g.: bandwidth, maximum quantization level (q) relative to maximum voltage swing of the input). Since calculations are necessarily crude, this data must be measured in the laboratory.

Recognition of the limitations of a device is a mandatory first step in the measurement of performance limits. An outline of limitations of the VDS is presented below as a guideline for future research:

1. Errors due to Sampling: A bandwidth limitation is placed on the input signal which, if exceeded, results in unsatisfactory signal reproduction. (presence of false frequency components) at the output.

2. Errors due to Quantizing: A statistical analysis[1]

[1] A.K. Susskind "ed." Notes on Analog - Digital Conversion Techniques. (New York: The Technology Press of M.I.T. and John Wiley & Sons Inc., 1957), pp. 2-40 to 2-49.

reveals that a quantized signal may be "recovered" if a sufficiently fine quantization level (q) is used. While this effect can always be minimized by amplitude scaling, a knowledge of the greatest admissible degree of "coarseness" would be useful.

3. Errors in Quamtizing: While the A/D convertors are sufficiently accurate, conversion of rapidly varying waveforms may result in a significant error in the quantized output, if the input voltage changes too much during the conversion interval (Δt).

For a sinusoidal input ($E_f \sin 2\pi ft$) a maximum allowable error of q volts places the following restriction on f:

$$f E_f < \frac{q}{2\pi\Delta t}$$

For a more general waveform, application of the above restriction (on $f E_f$) is extremely difficult. However, the addition of a S/H unit effectively reduces Δt to the switching time of the S/H (since the input to the ADC is held constant over Δt). Thus, it is expected that the problem will be minor.

Improvement of System Performance and Versatility

1. Coaxial input connections grounded at the VDS are unconditionally recommended to reduce quantization errors due to pickup.

2. A ventilation system should be installed to shorten the warm-up period, preferably in the bottom section, to minimize noise effects of the fan motor on the analog units.

3. Filtering of the output or the installation of a first-order hold is indicated to eliminate switching spikes when the DAC changes state and to improve signal reconstruction in general.

4. The storage of an initial function in an unused quarter of the memory to be used in the Repetitive - Operation mode (for 'scope displays, is entirely feasible. The stored function could be loaded sequentially into the "operate" portion of the memory at the end of each operate period.

In Retrospect

The results of this investigation are extremely satisfying. A versatile simulator has been built, satisfying the needs of the interested researcher. Though the overall cost of the VDS was high, its versatility and accuracy will reap large rewards in the investigation of time - variable delay systems.

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(3) Belyakov, V.M., P.I. Kravtsova, and M.G. Rappaport, Tables of Elliptic Integrals Part I, trans. B. Prasenjit, New York: The Macmillan Co., 1965.

(4) Bellman, R.E., J.D. Buell, and R.E. Kalaba, Mathematical Experimentation in Time - Lag Modulation, The RAND Corp., RM - 4432 - NIH, February 1965.

(5) Susskind, A.K., ed., Notes on Analog - Digital Conversion Techniques, New York: The Technology Press of M.I.T. and John Wiley & Sons Inc., 1957.

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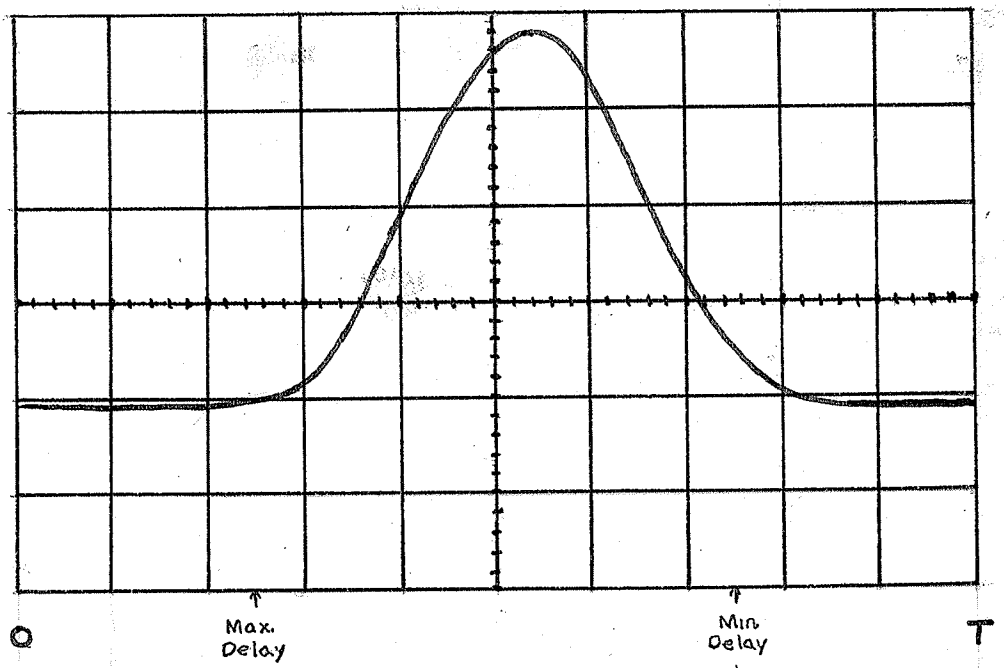
(7) Digital Equipment Corporation, Digital Logic Handbook, 1968.

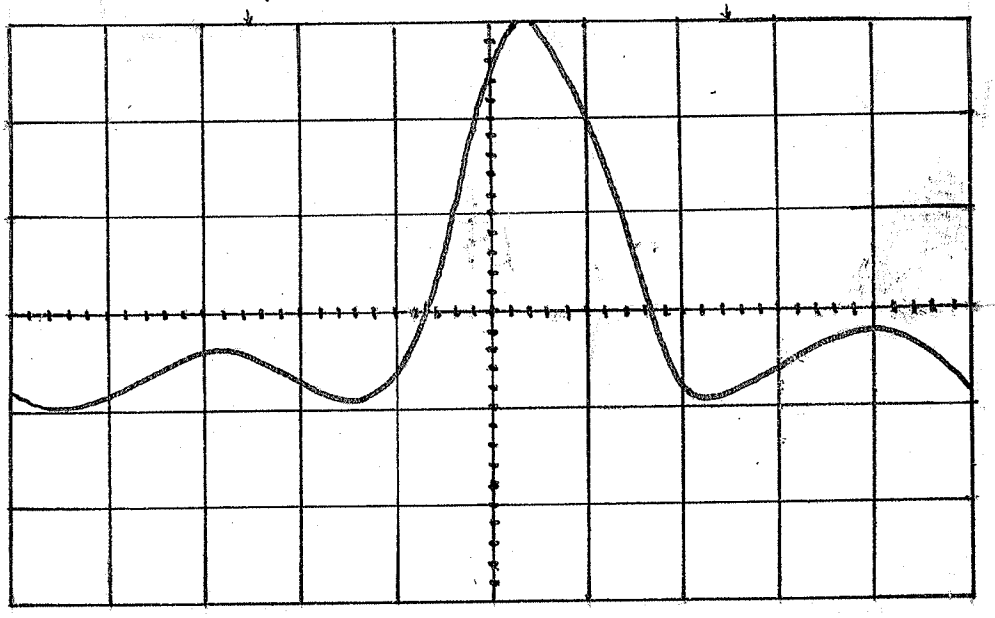
APPENDIX 1

WAVEFORMS - Variable Delay

Presented below are representative waveforms, sketched from the 'scope ("453") display of the output of the VDS ($u(t-\tau(t))$) for the sinusoidal case tested. Notice the increasing distortion of the wave-shape as k increases.

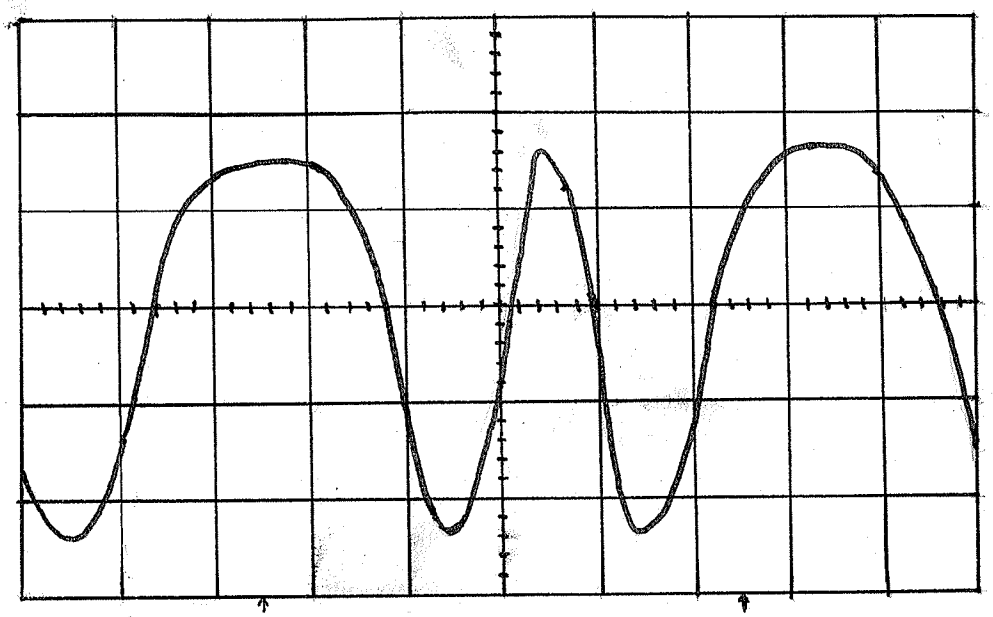


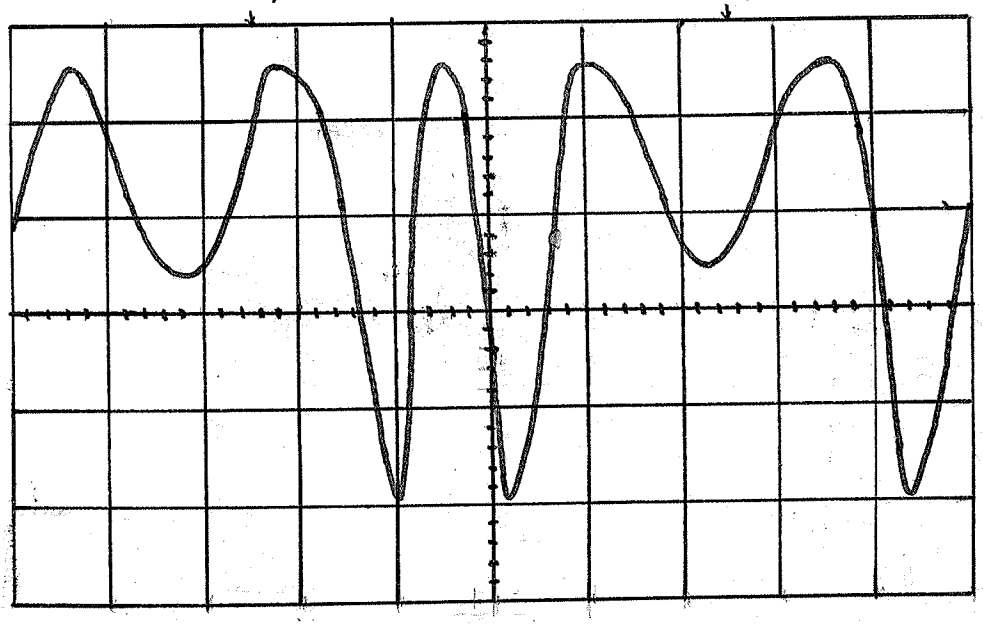
K = 0.1750



K = 0.3500

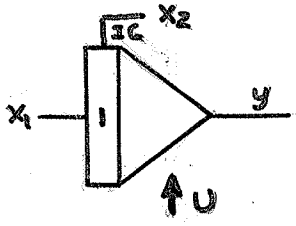
APPENDIX 1 (Cont.)





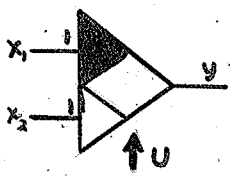
APPENDIX 2

Outlined below for the edification of the reader are some of the less familiar simulation diagram symbols. [1]



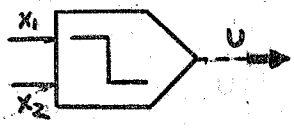
Mode-Controlled Integrator

$U=0 : y=-\int x_1\,dt$
$U=1 : y \cong -x_2$



Electronically Switched Amplifier (S.P.D.T. Switch)

$y=-Ux_1-\bar{U}x_2$



Comparator

$x_1+x_2>0 \Rightarrow U=1$
$x_1+x_2<0 \Rightarrow U=0$

[1] Due to: G.A. Korn and T.M. Korn, Electronic Analog and Hybrid Computers, McGraw - Hill, 1965, page 391.