LOGARITHMIC AND ANTILOGARITHMIC AMPLIFIER CIRCUITS

A Thesis Presented to The Faculty of Graduate Studies and Research,

University of Manitoba

In Partial Fulfillment of the Requirements for the Degree of

Master of Science

BY

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September 1959

ABSTRACT

This thesis discusses an investigation of some logarithmic and antilogarithmic computing circuits which may be used in the design of a special type of analog computer being developed at the University of Manitoba. This computer is to be used in solving network synthesis problems. It simulates complex numbers by sinusoidal voltages, and multiplies these numbers by first taking the logarithm of each factor and adding the terms. The output of the computer is a voltage proportional to the logarithm of the magnitude of the complex function, and to determine the magnitude of the function, it becomes necessary to compute the antilogarithm of the output.

The antilogarithmic networks are discussed first, since they find immediate use with the computer. The logarithmic networks and the design of a new channel for the computer are then presented with the view that they may be used to improve the performance of the present computer. Only the determination of the magnitude of a complex function is of concern here, the phase determination being reserved for another project.

PREFACE

Under further development in the Department of Electrical Engineering at the University of Manitoba, is an analog computer called the Complex-Plane Scanner, and discussed by E. P. Valstyn in his M. Sc. Thesis (See Bibliography). This computer simulates and computes the logarithm of the magnitude of a complex variable function, and in order to determine the magnitude of the function, the antilogarithm of the computer's output must be found.

This thesis discusses the antilogarithmic network which was developed to be used in conjunction with the computer, and also an investigation of some logarithmic and antilogarithmic circuits. The investigation of these circuits found its incentive from the fact that the present computer is subject to many errors, and it was hoped that the entire computer may be improved from the results of these investigations.

There are four chapters in this thesis. Chapter 1 deals with the theory and construction of the antilogarithmic circuit which was designed to be used with the present computer, while Chapter 2 deals with the theory and design of another probable antilogarithmic network. Chapter 3 discusses some logarithmic circuits, and presents a successful unit which may be used to improve the logarithmic network used in the present computer. Chapter 4 discusses an alternative channel for the computer, utilizing the logarithmic network described in Chapter 3.

This project was sponsored by the National Research Council of Canada with a grant to the Department of Electrical Engineering.

The author wishes to express his gratitude to Professor R. A. Johnson for his advice and assistance, and to thank Mr. H. Wagerer for his suggestions on the logarithmic circuits. He also wishes to express his appreciation of the help received from the entire Department of Electrical Engineering, especially that of Mr. T. J. White and Mr. R. D. Woods.

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CHAPTER 1

AN ANTILOGARITHMIC CIRCUIT

(1) THEORY OF THE LOGARITHMIC FEEDBACK CIRCUIT

The antilogarithmic circuit to be discussed first consists of a high gain d-c amplifier with a logarithmic network in the feedback loop. The logarithmic network considered in the feedback loop is the C.E.S. Logaten 511E, a logarithmic attenuator produced commercially by Custom Electronic Services. The output voltage of the Logaten is a linear function of the logarithm of the input voltage for inputs between 0.1 and 100 volts peak.

Referring to the block diagram of Fig. (1), and neglecting grid current,

$$(-E_1 - E_g)/R_i = (E_g - E_f)/R_f = (E_g - B \log E_o - C)/R_f \quad (1)$$

where $E_f = B \log E_o + C$, B and C being constants of the logarithmic attenuator. Substituting for E_g in Equation (1) and solving for E_1 gives,

$$E_1 = E_o(1 + R_i/R_f)/A + (R_i/R_f)(B \log E_o + C). \quad (2)$$

If the amplifier gain A is very large, the first term on the right-hand side of Equation (2) becomes negligible, and we get,

$$E_1 = (R_i/R_f)(B \log E_o + C) \quad (3)$$

Re-arranging the terms of Equation (3) gives,

$$\log E_o = E_1 (R_f/R_i B) - C/B$$

or,

$$E_o = 10^{K_1 E_1} 10^{-K_2} \quad (4)$$

where $K_1 = R_f/R_i B$ and $K_2 = C/B$.

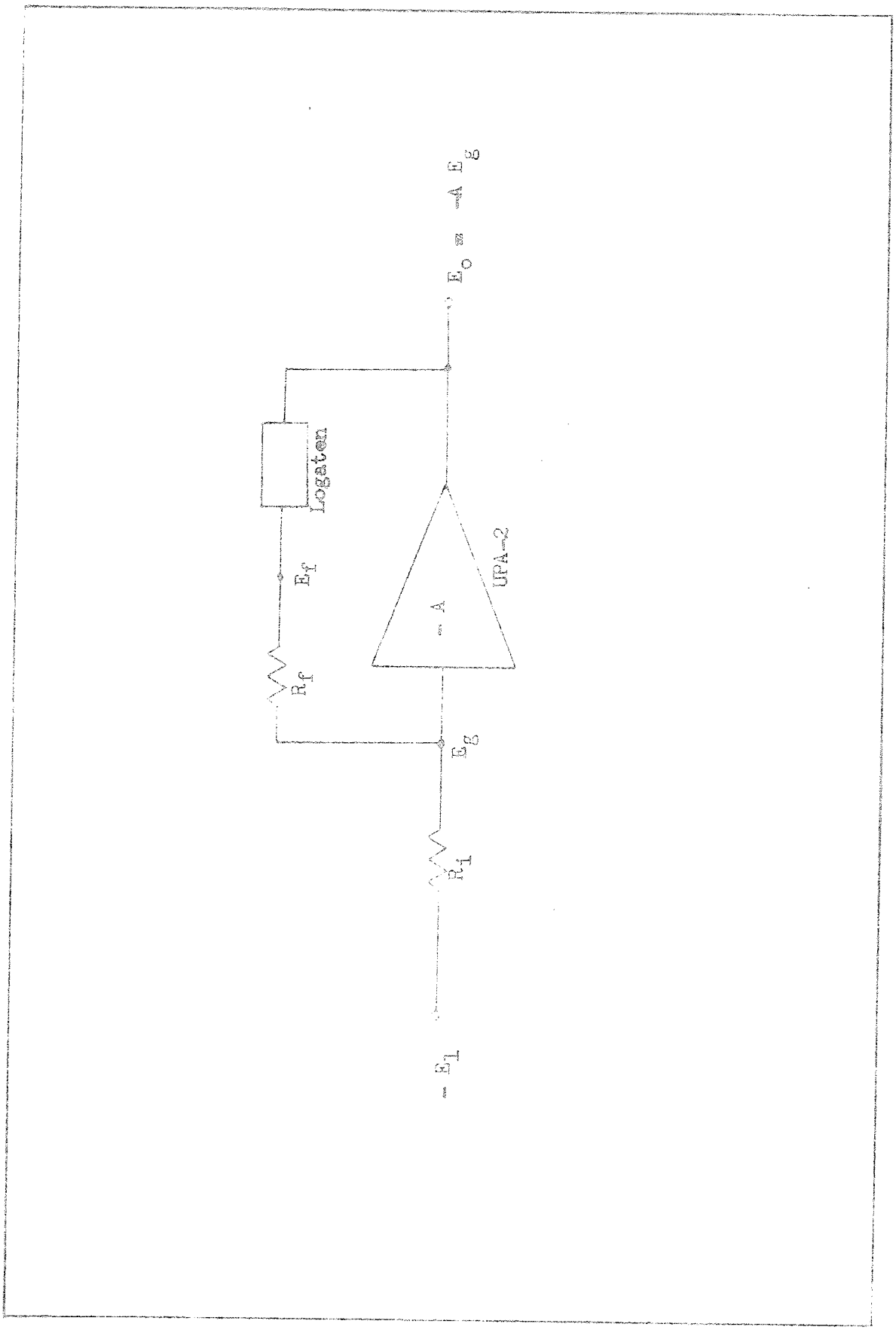


FIG. 1. BLOCK DIAGRAM OF ANTILOGARITHMIC CIRCUIT

The Logaten should be loaded with at least 100 K, thus the value of R_f is limited to a minimum of 100 K. Typical values of the constants B and C are,

$$B = 0.024 \quad \text{and} \quad C = 0.033$$

If R_f is chosen as 100 K, and R_i as 2.2 M, then we get,

$$K_1 = 1.89 \quad \text{and} \quad K_2 = 1.375$$

Equation (4) then becomes,

$$E_o = 0.0422 \times 10^{1.89E_1} . \qquad (5)$$

This is the basic antilogarithmic system. The values of R_i and R_f were so chosen to make the ratio R_i/R_f as high as possible without introducing appreciable errors due to noise voltages.

(2) THE D-C AMPLIFIER

The performance of the antilogarithmic system discussed above depends critically on the d-c amplifier used. The Logaten 511E has an input impedance of approximately 10 K, and an input range of 0.1 to 100 volts peak. The d-c amplifier must, in addition to having an extremely high gain, be capable of delivering 100 volts to a 10 K load. It should be very stable so that errors due to noise and drift can be made negligible. It was also desirable that the amplifier should operate only with two power supplies of plus and minus 300 volts. In the search for a suitable amplifier, it was found that the Model UPA-2 D-C Amplifier produced by Philbrick Researches was almost ideal. This amplifier has an internal gain design centre of 5×10^7, with a guaranteed minimum value of 10^7. With a 42 K, 10 watt load current balancing resistor connected from the output to minus 300 vdc., the

amplifier is capable of delivering plus or minus 100 volts to a 12 K load. This output was not quite sufficient to utilize the full range of the Logaten. However, this is no disadvantage. The Logaten is capable of handling sinusoidal signals and positively and negatively varying signals. According to specifications, the output of the Logaten is a linear function of the logarithm of the input within plus or minus 1.0 db for inputs between 0.1 and 100 volts peak for all types of signals. Tests on several Logatens showed that they were quite accurate for either positively or negatively varying inputs, but inaccurate for sinusoidal inputs. This is the main reason for the investigation of other logarithmic circuits. For the specific application, the input of the antilogarithmic circuit will be a slowly varying signal. If, therefore, the input is restricted to only negatively varying signals, the amplifier output will always be positive, and only the positive characteristics of the Logaten will be utilized. Without the 42 K current balancing resistor, the UPA-2 amplifier is capable of delivering plus 220 volts and minus 80 volts to a 10 K load. Since only the positive signal is of importance now, the output of the amplifier is more than sufficient to utilize the full range of the Logaten. Also, the characteristics of the Logaten under these conditions are accurate within the specifications, and the errors due to sinusoidal voltages are avoided. The UPA-2 amplifier is also chopper stabilized, so that errors due to drift and noise are negligible. Full specifications of this amplifier are given in the appendix.

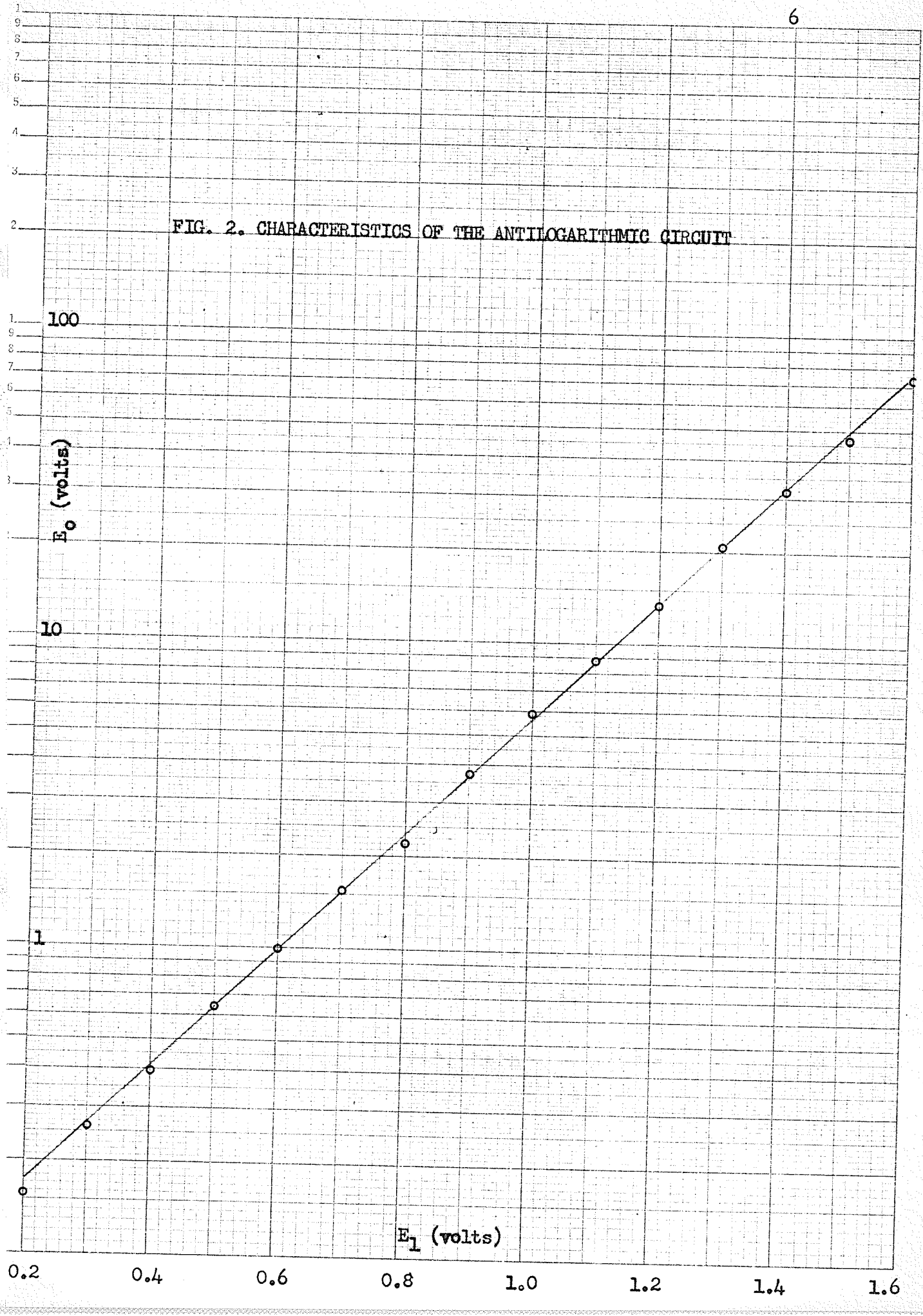
(3) CHARACTERISTICS OF THE ANTILOGARITHMIC CIRCUIT

From Equation (5), it can be calculated that for outputs in the range 0.1 to 100 volts, the input range is approximately 0.2 to 1.78 volts. Results of the characteristics of the circuit are given below, and the plot of the curve is shown in Fig. (2).

E_1 (volts)	E_o (volts)
0.1	0.08
0.2	0.158
0.3	0.26
0.4	0.398
0.5	0.64
0.6	0.99
0.7	1.55
0.8	2.40
0.9	3.75
1.0	5.85
1.1	8.80
1.2	13.50
1.3	20.8
1.4	31.8
1.5	46.5
1.6	73.0
1.7	110.0

From the curve of Fig. (2) it is found that $K_1 = 1.89$ and $K_2 = 1.144$, and the curve is linear over nearly three decades. It was found however, that for different tests, the value of K_2 varied, and the output drifts slowly if high output voltages are sustained. This

FIG. 2. CHARACTERISTICS OF THE ANTILOGARITHMIC CIRCUIT



is due to the effects of temperature on the Logaten.

(4) THE PRE-AMPLIFIER

From Equation (4) we have,

$$E_o = 10^{K_1 E_1} 10^{-K_2}$$

that is, $$\log E_o = K_1 E_1 - K_2$$

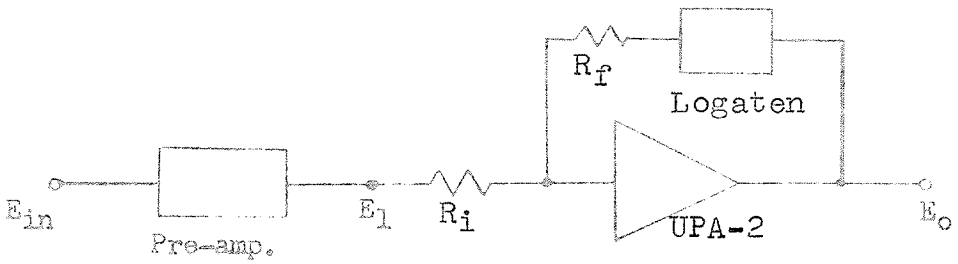
Consider the circuit of Fig. (3a). Let E_{in} be the input to the pre-amplifier and E_1 the input to the antilogarithmic circuit. If it is desired that the output be the true numerical antilogarithm of the input, then we have,

$$\log E_o = K_1 E_1 - K_2 = E_{in}$$

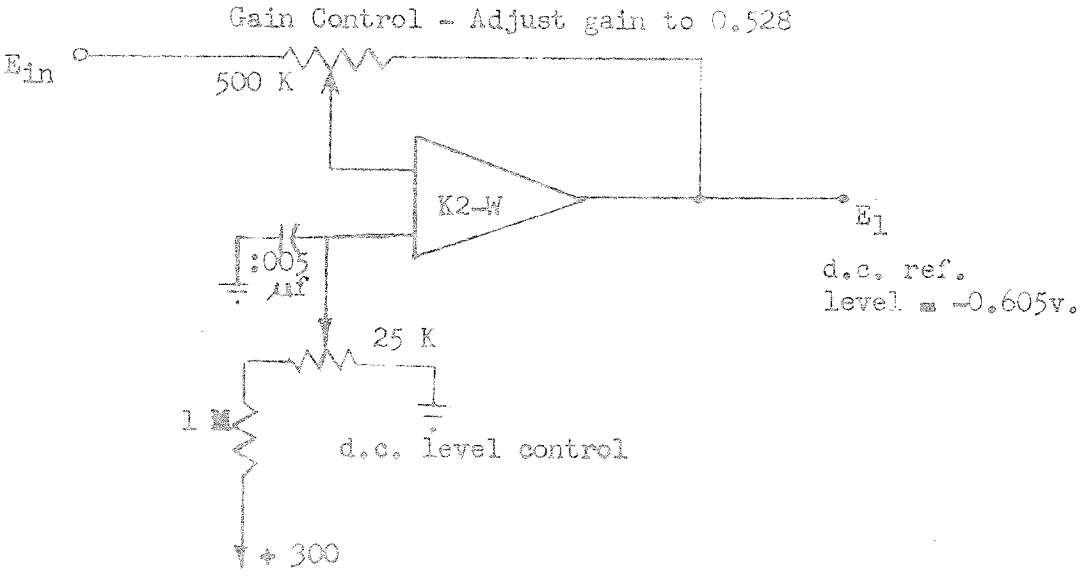
from which,

$$E_1 = E_{in}/K_1 + K_2/K_1 \qquad (6)$$

The pre-amplifier must therefore multiply the input by a constant and add another constant. This can be done easily with a high gain d-c amplifier having a differential input. The amplifier chosen for this was the Philbrick K2-W plug-in unit. This amplifier has an internal gain of 15,000 and a differential input, by means of which a constant voltage may be added or subtracted from the output. The circuit diagram of this amplifier is given in the appendix. The schematic diagram of the pre-amplifier is shown in Fig. (3b). The amplifier also causes an inversion of the signal so that E_{in} will be positive for E_o positive, and E_1 will be negative, which is necessary for the operation of the system.



(a)



(b)

FIG.3. THE PRE-AMPLIFIER CIRCUIT

Assuming $K_1 = 1.89$ and $K_2 = 1.144$, then from Equation (5)

$$-E_1 = -0.528\, E_{in} - 0.605$$

That is, the overall gain of the pre-amplifier should be adjusted to 0.528 with a zero reference level of -0.605 volts. In this manner the input range of E_{in} will be -1 to +2 volts for an output range of E_o between 0.1 to 100 volts. The output is therefore the numerical antilogarithm of the input in volts. The input E_1 of the antilogarithmic system will vary between -.077 volts to -1.661 volts. In this system it is not necessary that the constants K_1 and K_2 be known accurately. The gain and level controls on the pre-amplifier can always be adjusted so that the output is the antilogarithm of the input. A method for adjustment of the total circuit is as follows.

(a) Adjust the gain potentiometer of the pre-amplifier to approximately 0.528. (This can best be done by utilizing a sinusoidal a-c input signal and adjusting the gain, since the measured a-c output is independent of the d-c level).

(b) Connect the pre-amplifier to the antilogarithmic network. With the input grounded, adjust the d-c level potentiometer so that the output is 1 volt. Apply an input of 1 volt d-c and adjust the gain control until the output is 10 volts.

(c) Ground the input again and the output should be 1 volt. If not, adjust the d-c level again. Apply a 1 volt d-c signal again and readjust for 10 volts output. Repeat until the outputs of 1 volt and 10 volts correspond to inputs of zero and

1 volt d-c. This is the difficult part of the adjustment, since the d-c level adjustment depends on the gain setting, although the gain is independent of the d-c level.

It will be necessary to adjust both settings until the desired results are obtained, but actual tests show that the practical procedure is not difficult and not as time-consuming as indicated.

(5) CONSTRUCTION OF THE ANTILOGARITHMIC UNIT

Available as an accessory to the UPA-2 Amplifier is a plug-in shielded component box. With such a unit available, the Logaten and the K2-W Amplifier were mounted on the box and all other components were placed within the box so that complete shielding was possible. The circuit diagram of the plug-in unit is shown in Fig. (4) and the total antilogarithmic network assembly is shown in Figs. (5), (6) and (7).

(6) THE RANGE-EXTENDING CIRCUIT

For the antilogarithmic network described above, the input range extends from -1 to +2 volts. It is very desirable that this range be extended, and since the output range is limited from 0.1 to 100 volts, it is therefore convenient to introduce a scale factor. If the output is to represent one-tenth of the actual value, then this corresponds to the subtraction of one volt from the input. In general, subtraction of e volts from the input yields an output that is 10^{-e} times the correct value. The true value must therefore be obtained by multiplying the actual output by the scale factor 10^{e}. The range-extending circuit is thus one whereby arbitrary or fixed

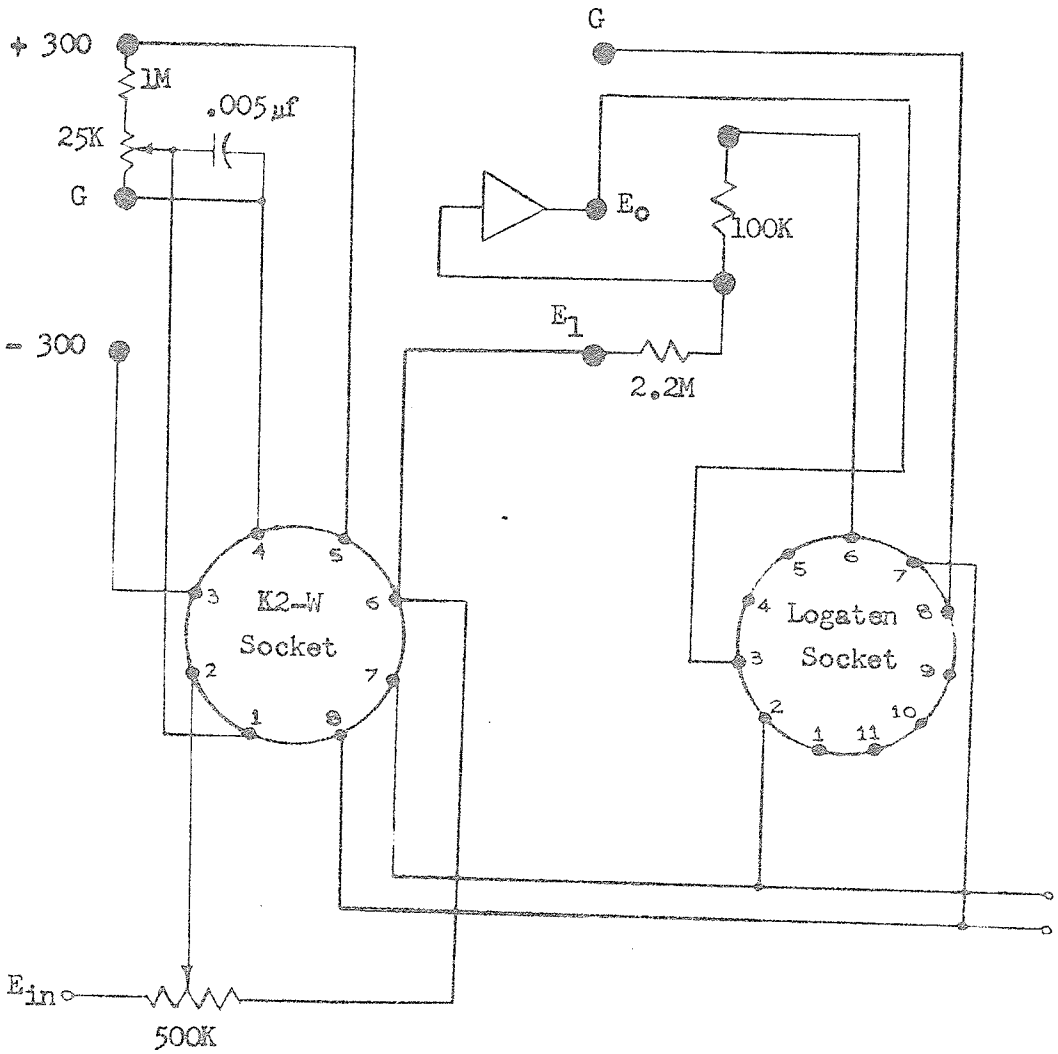


FIG. 4. PLUG-IN UNIT OF THE ANTILOGARITHMIC CIRCUIT

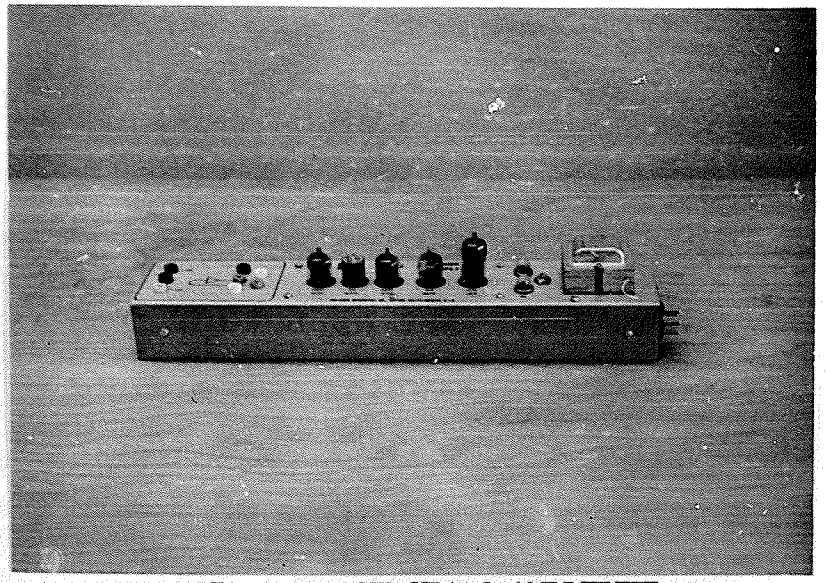


FIG. 5. THE UPA-2 AMPLIFIER

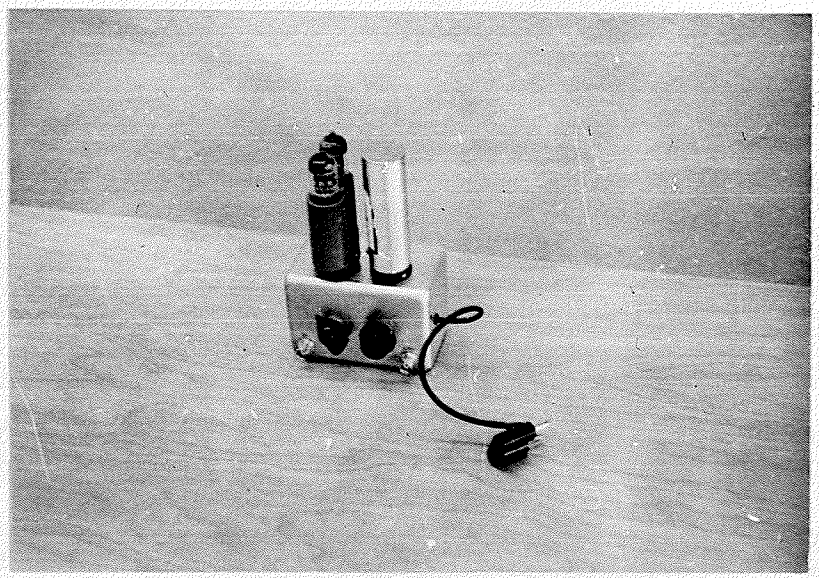


FIG. 6. THE PLUG-IN UNIT

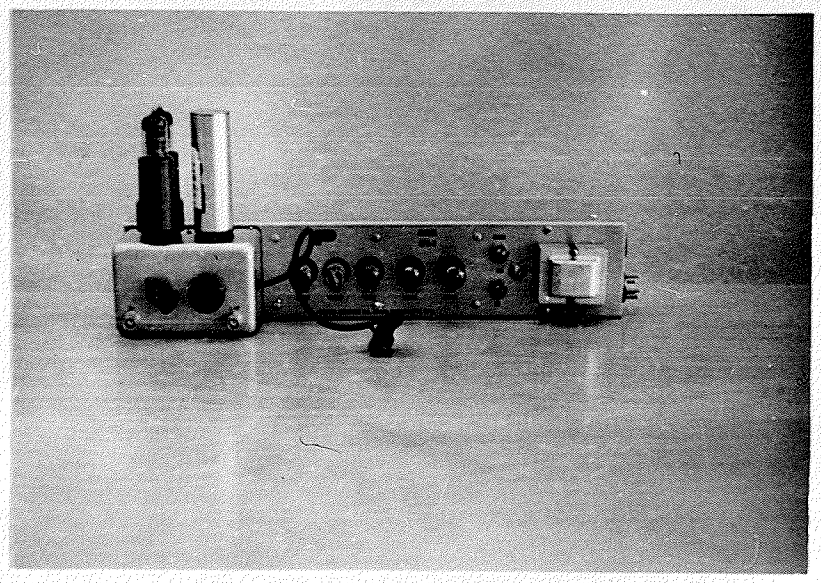


FIG. 7. THE ANTILOGARITHMIC UNIT

voltages may be subtracted or added to the input signal. This can be done easily by means of a d-c amplifier with a differential input. Here again the K2-W amplifier was utilized. In the actual circuit, shown in Fig. (8), two such amplifiers were used - one as a voltage adder and the other as a gain and level control. The adder circuit consists of a chain of precision resistors connected to the positive input. By convention, the positive input is that which gives an output in phase with the input signal, and the negative input yields an inverted output. The chain of resistors is connected between plus and minus 300 volts, and the adding or subtracting switch is connected across three 1 K precision resistors of the chain. A 500 K potentiometer is used as the gain control in the feedback loop between the output and the negative input grid. The gain control is adjusted so that switching across one of the 1 K resistors at the positive input corresponds to exactly 1.0 volt change at the output. The gain control is fixed at this point. This set-up however, has no means by which any desired d-c reference may be set, and the gain is fixed. The other K2-W amplifier provides the means by which these controls may be added. It is connected as a variable gain amplifier in the usual manner, with an adjustable d-c level control at the positive input. These controls affect the total system since the gain and d-c level of the adder amplifier alone are fixed, and also, the output is in phase with the input of the overall system. The gain of the total range-extending circuit may therefore by adjusted to exactly unity with a zero d-c reference level, and with the arrangement as shown in Fig. (8), one volt may

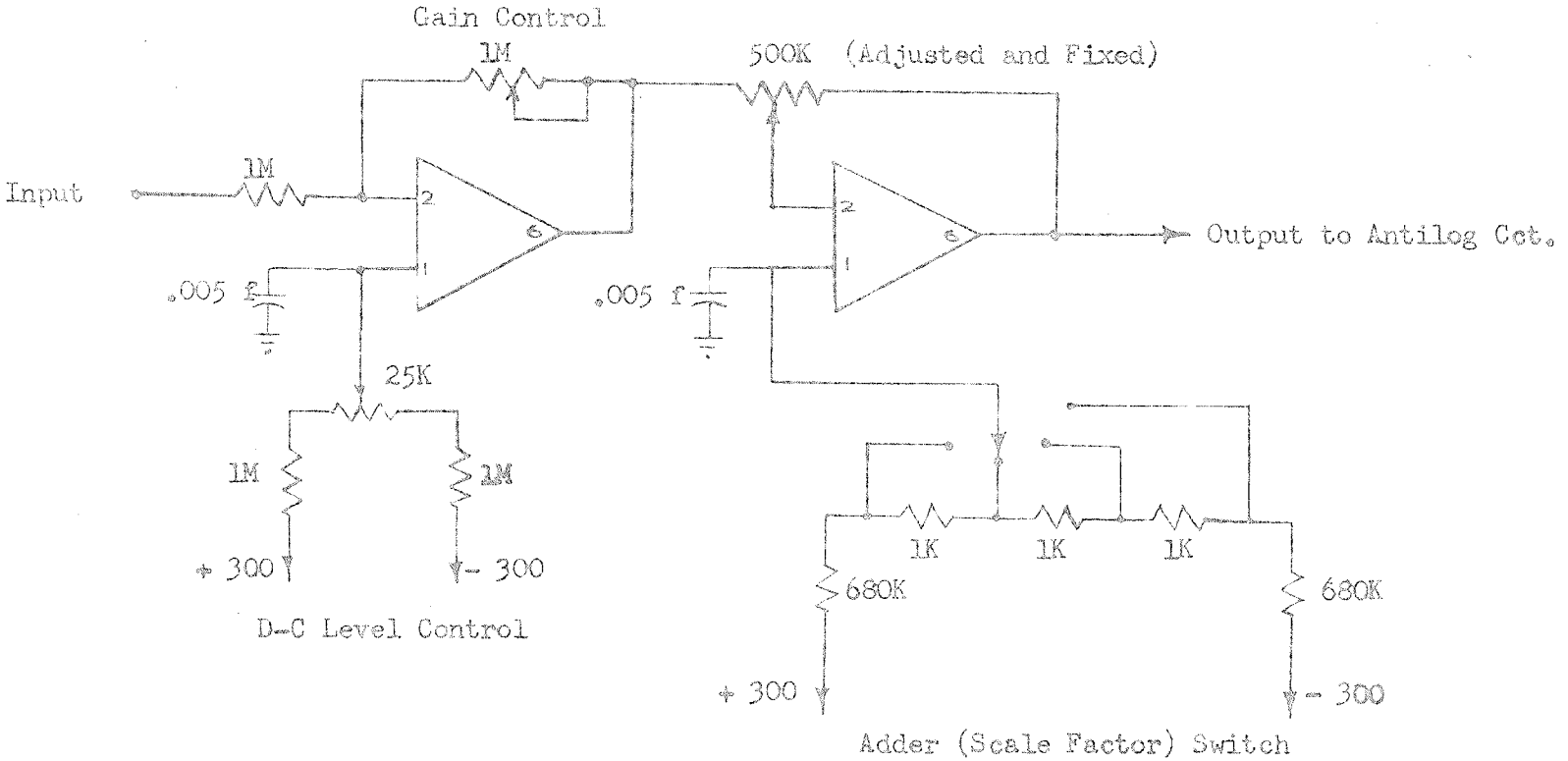


FIG. 8. RANGE-EXTENDING CIRCUIT

be added to the output and either one or two volts may be subtracted from the output. When connected to the antilogarithmic circuit previously described, this circuit has the effect of multiplying the final output by scale factors of 0.1, 1.0, 10, and 100. It will be noted that the gain and level controls of the range-extending circuit accomplish the same function as the controls of the preamplifier of the antilogarithmic unit. Consequently, once the range-extending circuit is connected to the antilogarithmic unit, the final adjustments of the overall system may be made by the gain and level controls of the range-extending circuit alone. The very same procedure for the adjustments previously outlined also apply in this case.

(7) THE SUMMER-ATTENUATOR AND COMPLETE ANTILOGARITHMIC SYSTEM

The Complex-Plane Scanner (Va)[1] contains twelve channels, each of which has an output voltage that is the simulation of a factor of the form $\log (s - s_k)$, where s is the complex frequency variable and s_k is a pole or zero position of the complex function F(s) being investigated. The outputs from each channel must be summed, so that the output from the summer will represent the function $\log F(s) + K$. K represents an arbitrary constant, the value of which is not important in this application. When this output is fed into the antilogarithmic unit, the final output will be $K_o F(s)$, where $K_o = 10^K$. The summing amplifier circuit used, is the conventional one, with a K2-W as the d-c amplifier, and twelve 1 M precision resistors for the input summing resistors, A 1 M precision resistor is also used in the feedback loop

[1] The abbreviations in parentheses refer to the Bibliography.

for unity gain, and a zero d-c level adjustment is connected in the same manner as shown in Fig. (3b) to the positive input of the K2-W.

In order to measure the phase of the function, it is necessary that the output of the summing amplifier be also fed to the phase measuring system. Since the total output from the summer is usually high, it is necessary to attenuate the output before applying it to the phase measuring system. For this reason the summing amplifier was connected with a number of conveniently chosen feedback resistors so arranged that any desired attenuation factor may be used by means of a switching arrangement. In this way, the outputs from the channels are both summed and attenuated at the same time. Since the output of the summer must also be applied to the antilogarithmic system, and since adjustment of the antilogarithmic system makes it necessary to ground the input of the range-extending circuit, the attenuator switch is ganged to another switch so that on the first position the summer is connected as a unity gain amplifier with the output disconnected, while the input of the range-extender is grounded. On any other position, the output of the summer-attenuator is directly connected to the input of the range-extender. The values of attenuation factors chosen for the system are 1, 2, 5, 10, 20, 50, 100, 200, 500, and 1000. Measurement of these factors shows that the attenuator is accurate except on the 500 and 1000 ranges.

The input range of the antilogarithmic unit is limited to the range between -1 and +2 volts. The range-extender increases the range to -2 and +4 volts. As mentioned before, the output of the summer is usually high and may be well outside the input range of the range-extender circuit. Attenuation of the summer output

results in an output from the antilogarithmic unit that involves roots of the magnitude of the original function. That is to say, if the output of the summer is attenuated by a factor of two, the output now represents $\frac{1}{2}$ log F(s) + K, and the final output from the antilogarithmic unit will be K_o $F(s)^{\frac{1}{2}}$, which is the square root of the function of interest. Generally, attenuation by a factor n results in the n^{th} root of the required function. Because of this difficulty, it was decided to modify the range-extender so that larger voltages may be added or subtracted. The adder switch of the range-extender was modified so that the chain of 1 K precision resistors is connected across another set of resistors by means of a ganged switch, and so arranged that the total resistance of the whole chain between plus and minus 300 volts is constant. By using 3 K precision resistors in the secondary chain, addition or subtraction of 3 volts at a time can be accomplished by means of a secondary range-extending switch, and in the circuit used, the total input range of -5 to +13 volts is made possible. The circuit diagram of the summer-attenuator, range-extending unit, and the antilogarithmic unit, representing the complete antilogarithmic system is shown in Fig. (9).

(8) ACCURACY OF THE ANTILOGARITHMIC SYSTEM

It was desirable that the output of the system be a linear function of the antilogarithm of the input over three decades. To check the accuracy of the antilogarithmic unit, the input to the pre-amplifier in the range -1 to +2 volts was plotted against the

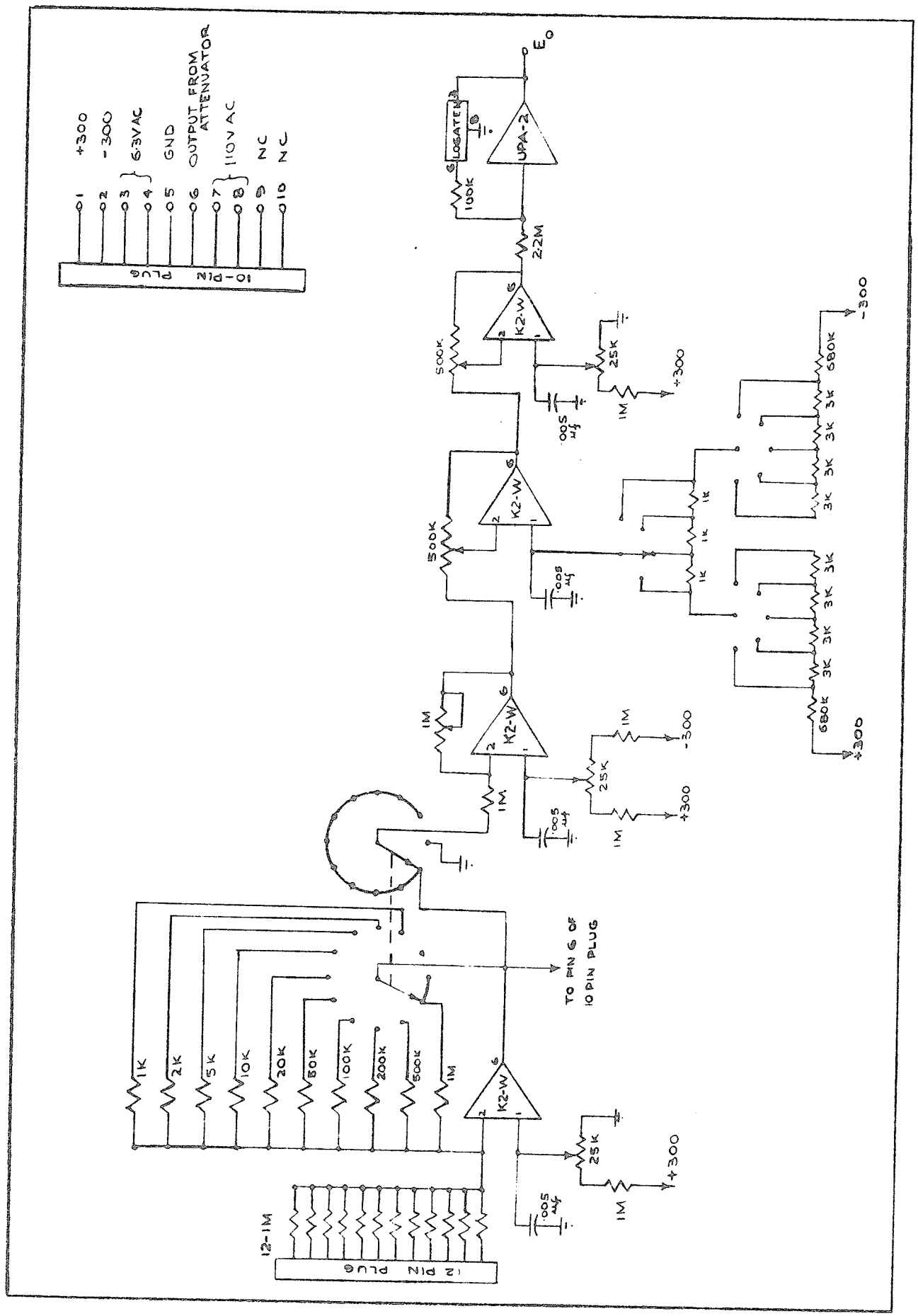


FIG. 9. THE COMPLETE ANTILOGARITHMIC SYSTEM

logarithm of the output. The results are given below and the curve is shown in Fig. (10).

E_{in} (volts)	E_o (volts)
-1.0	0.08
-0.9	0.11
-0.8	0.15
-0.7	0.20
-0.6	0.26
-0.5	0.32
-0.4	0.42
-0.3	0.50
-0.2	0.63
-0.1	0.72
0	1.00
0.1	1.25
0.2	1.58
0.3	2.00
0.4	2.60
0.5	3.20
0.6	3.80
0.7	4.95
0.8	6.20
0.9	7.90
1.0	10.05
1.1	13.0
1.2	16.5
1.3	20.5

E_{in} (volts)	E_o (volts)
1.4	26.5
1.5	33.5
1.6	41.5
1.7	56.0
1.8	68.0
1.9	78.0
2.0	94.0

From the plot of Fig. (10), the characteristics of the antilogarithmic unit were linear over nearly three decades, with slight deviations at both the low and the high ends. It was calculated that over the three decades the output reading for any given input will be correct to within plus or minus 0.8 db. Investigation and tests on the individual components showed that the error is due primarily to the characteristics of the Logaten, in fact, the total accuracy of the unit depends primarily on the accuracy of the Logaten used. The K2-W amplifiers in all of their applications in the system were found to be quite stable, and because of the high feedback ratios and comparatively high voltage inputs, errors due to noise were negligible. The use of precision resistors, and the method of adjustment, makes the system as accurate as the degree of manual precision, and because of this method of manual adjustment, the system can always be easily checked for accuracy.

The complete antilogarithmic network is shown in Figs. (11), (12), (13), and (14).

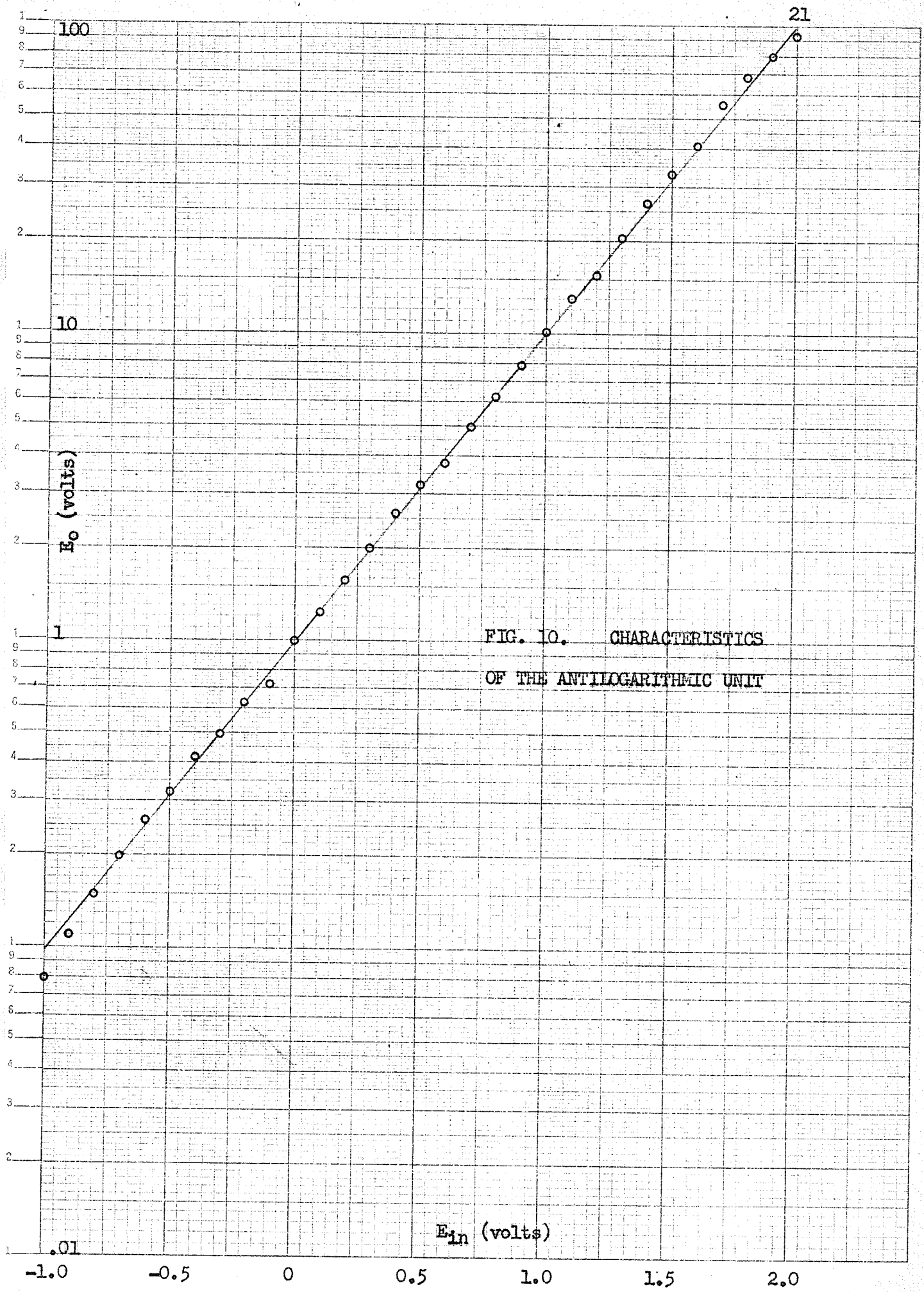


FIG. 10. CHARACTERISTICS OF THE ANTILOGARITHMIC UNIT

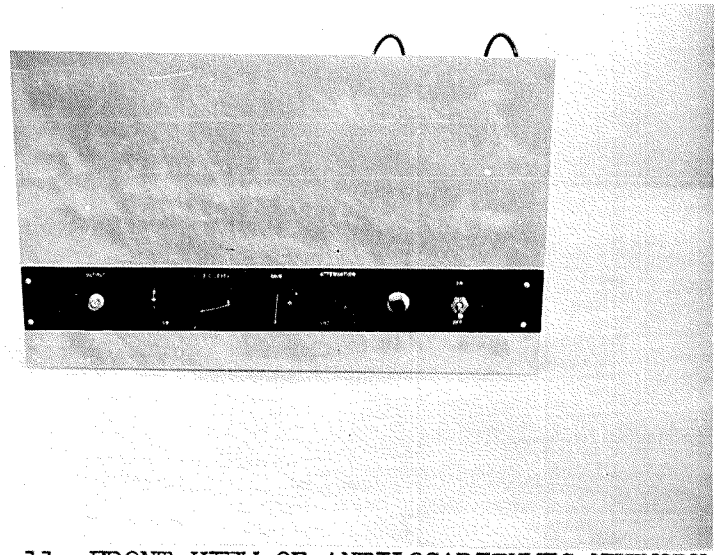


FIG. 11. FRONT VIEW OF ANTILOGARITHMIC NETWORK

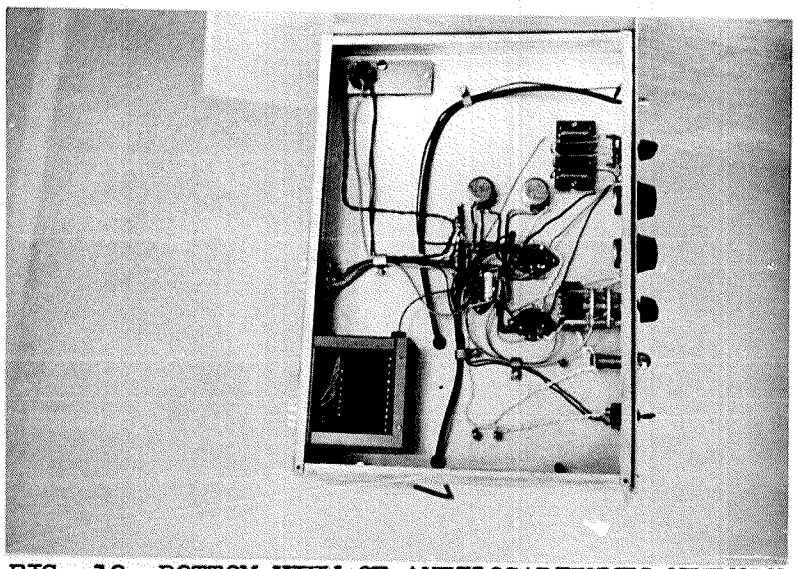


FIG. 12. BOTTOM VIEW OF ANTILOGARITHMIC NETWORK

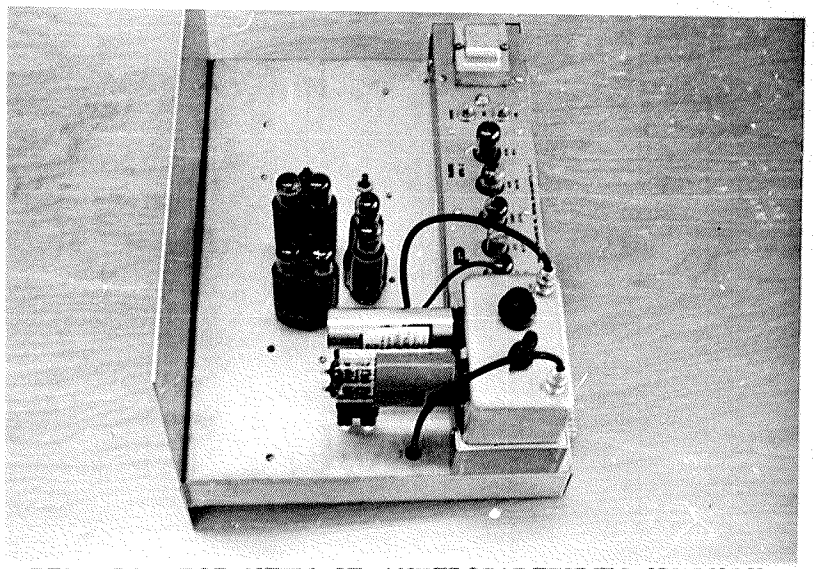


FIG. 13. TOP VIEW OF ANTILOGARITHMIC NETWORK

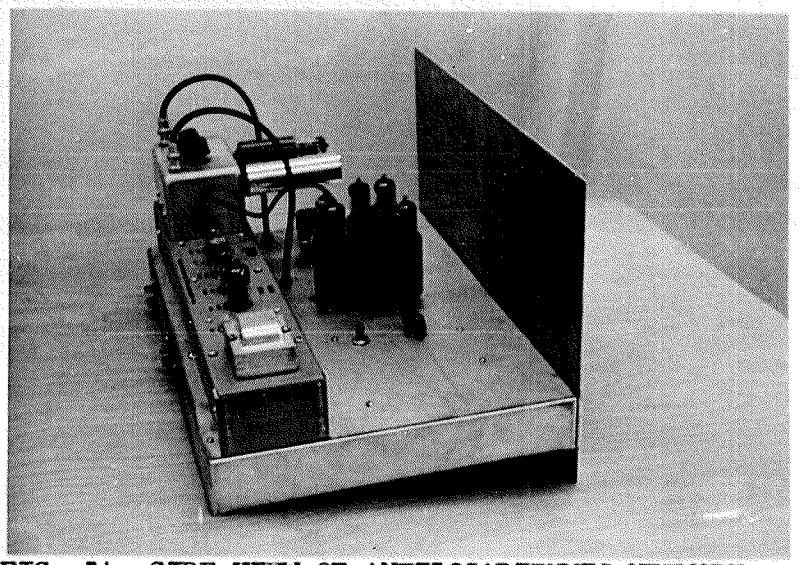


FIG. 14. SIDE VIEW OF ANTILOGARITHMIC NETWORK

CHAPTER 2

THE DIODE ANTILOGARITHMIC CIRCUIT

The core of this circuit is a silicon junction diode, Type 604C, produced by Texas Instruments Inc. The characteristics of this diode are such that the current I through the diode varies as the antilogarithm of the voltage E across its terminals.

(1) TYPICAL CHARACTERISTICS OF THE 604C JUNCTION DIODE

In order to determine the linearity, constants, and the typical operating voltages and currents of the diode, the current-voltage characteristics were plotted on semi-logarithmic paper. A typical curve is shown in Fig. (15). From the curve, it can be seen that the characteristics are linear over three decades, with a current range from 10 microamperes to 10 milliamperes, and a corresponding voltage range from 0.6 to 0.8 volts. For the linear part of the curve, the current is related to the voltage by the equation,

$$I = K_1 10^{K_2 E} \qquad (7)$$

From the curve shown, it can be calculated that the values of the constants are,

$$K_1 = 10^{-12} \text{ ma. and } K_2 = 16.3 \text{ volts}^{-1}.$$

(2) THEORY OF THE ANTILOGARITHMIC CIRCUIT

Consider the circuit of Fig. (16). The 6J6 tube acts as a current source capable of delivering over 10 ma. to the diode. Feedback is used so that the voltage input will be proportional to the voltage across the diode.

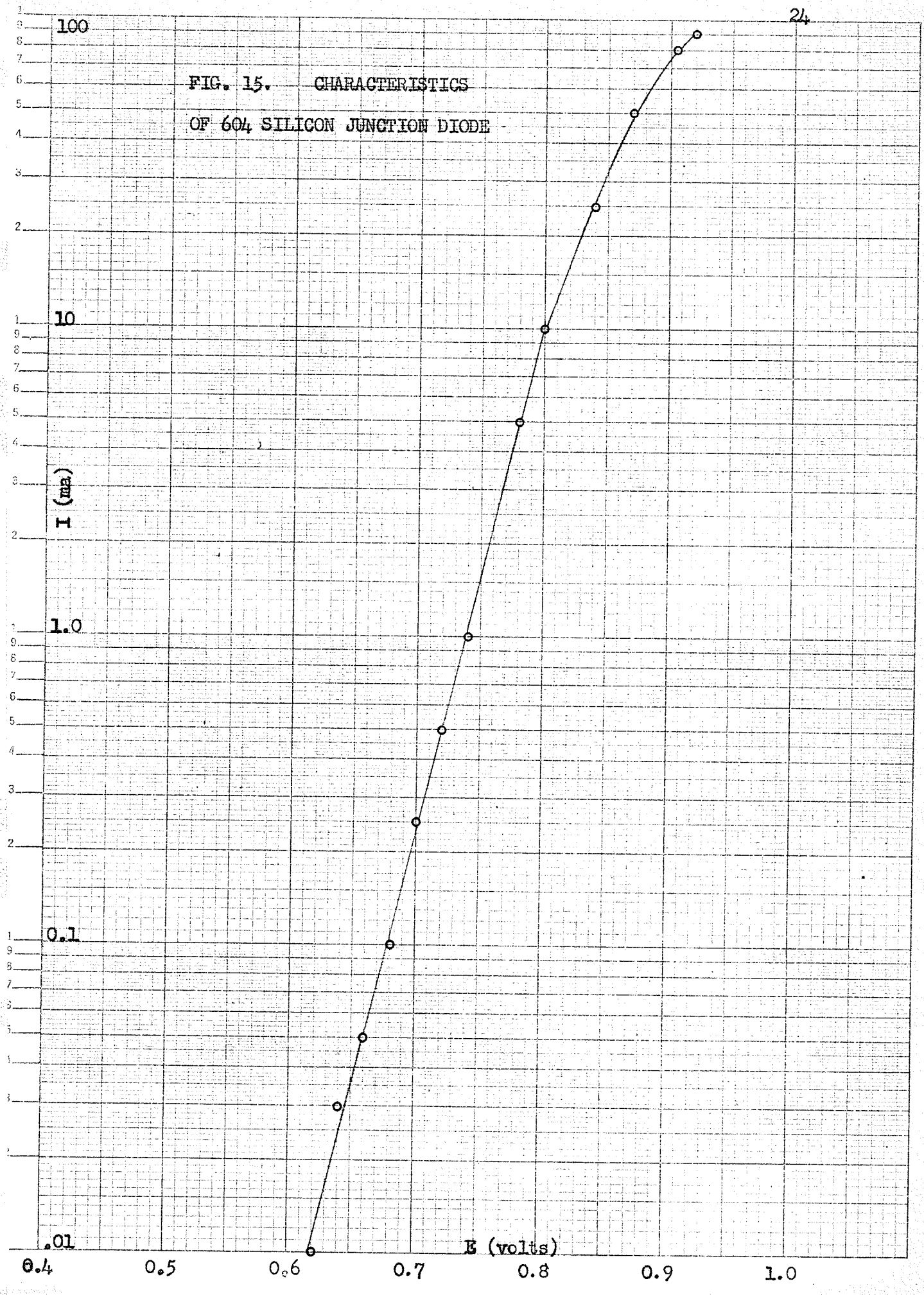


FIG. 15. CHARACTERISTICS OF 604 SILICON JUNCTION DIODE -

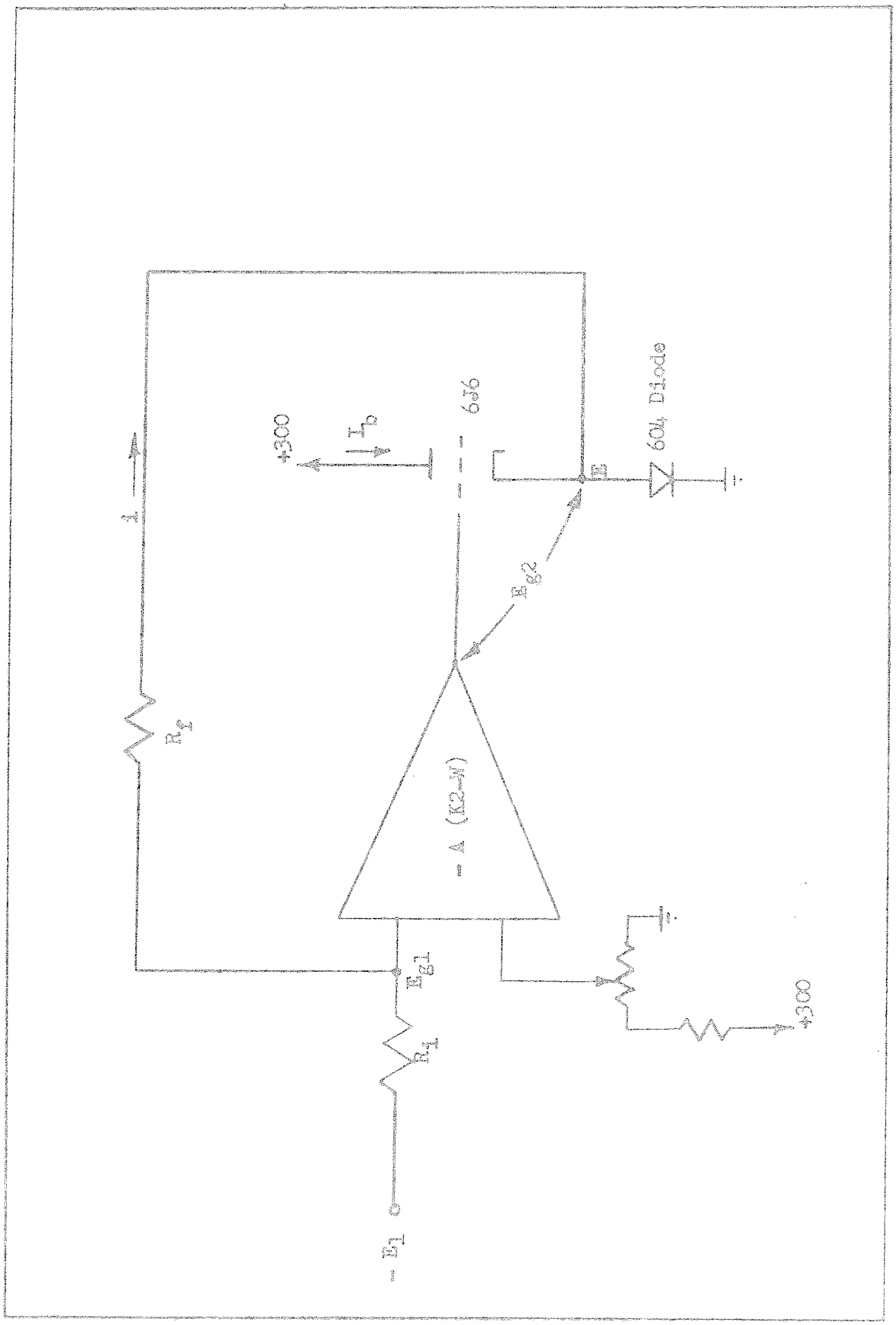


FIG. 16. THE DIODE ANTILOGARITHMIC CIRCUIT

From the diagram we have;

$$(-E_1 - E_{g1})/R_i = (E_{g1} - E)/R_f = i = K_1 10^{K_2 E} - I_b \qquad (8)$$

$$I_b = KE_{g2} \qquad (9)$$

$$E_{g2} = -AE_{g1} - E \qquad (10)$$

Solving these equations for E_1 and I_b we get,

$$K_1 10^{K_2(E_1/K_4 + K_3 I_b/K_4)} = (E_1/R_i)(1 + 1/AK_4) + I_b(1 + 1/AKR_i + K_3/K_4 AR_i) \qquad (11)$$

where $K_4 = (R_i/R_f)(1 + 1/A) - 1/A$ and $K_3 = (1 + R_i/R_f)/AK$, and and the value of K will be approximately equal to that of the transconductance (g_m) of the tube. From Equation (10), it is seen that for the current I_b to be approximately proportional to the antilogarithm of the voltage input, it is necessary that the gain of the amplifier and the value of the input resistor R_i be large. If a K2-W amplifier is used, the value of A is about 15,000. If R_i is chosen as 2 megohms, and R_f as 0.2 megohms, then the value of K_3 is approximately $10^{-2}/15K$ ohms, and that of K_4 approximately 10. Assuming K_1 has a value of 10^{-15} amps. and K_2 has a value of 16.3 volts^{-1}, then Equation (10) becomes, approximately,

$$10^{-15}\ 10^{(1.63E_1 + .001I_b/K)} = I_b \qquad (12)$$

since the large values of A and R_i make the co-efficient of I_b almost unity, and the term comtaining E_1 negligible, on the right-hand side of the equation.

From Equation (12), the linearity of the equation depends on the term $10^{.001\ I_b/K}$. But I_b/K is equal to E_{g2}, which varies from zero to about -13 volts. The greatest error will then occur when E_{g2} has a value of -13, and the value of the term becomes 0.9705 . This therefore indicates a 3% error at low current operation. This effect is due to the fact that the 6J6 has a logarithmic transfer function, and the value of K, and consequently the value of the tube transconductance, decreases for low current operation. Neglecting this slight variation, we can write Equation (11) as,

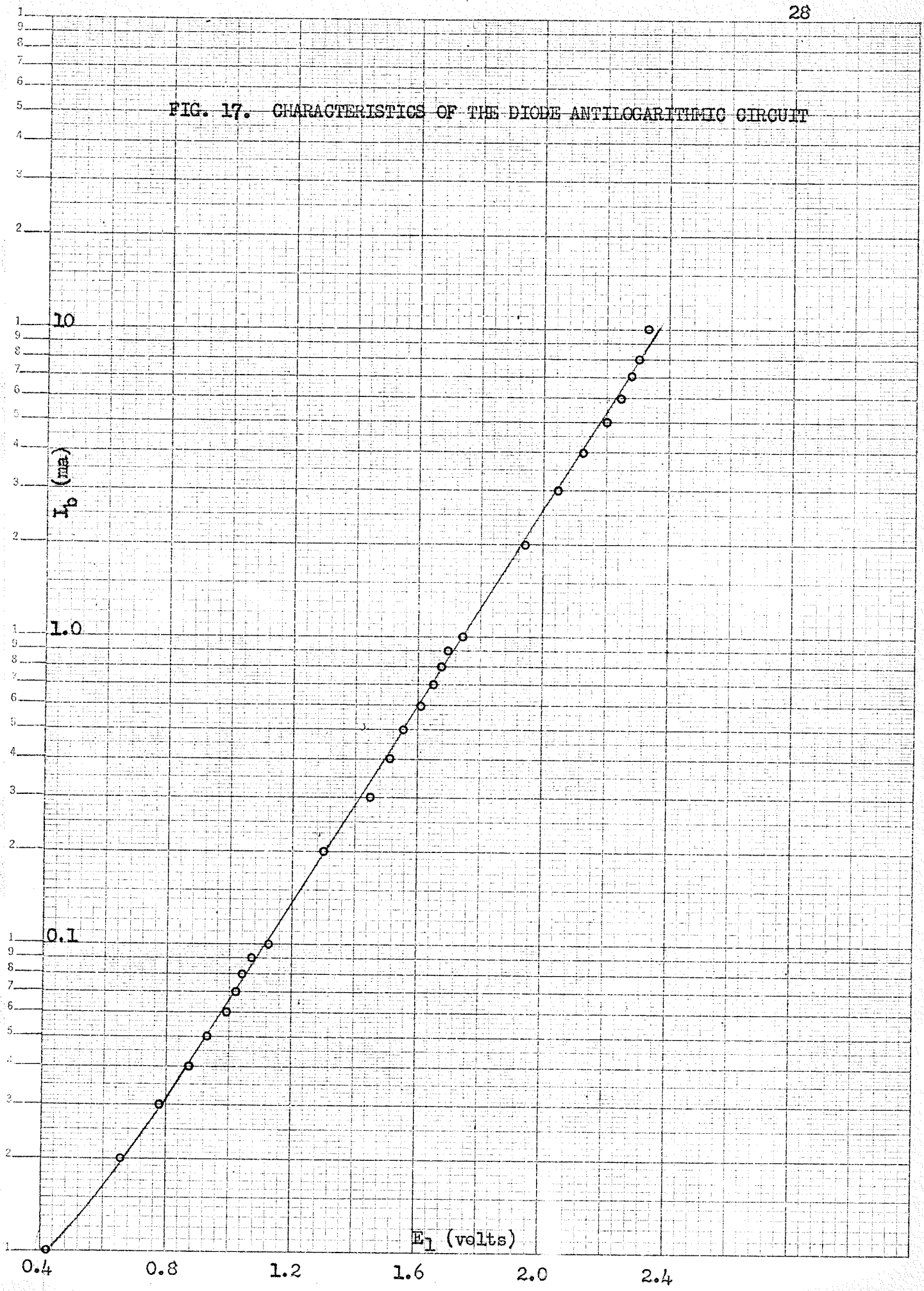
$$I_b = K_5 \quad 10^{K_6 E_1} \tag{13}$$

(3) CHARACTERISTICS OF THE ANTILOGARITHMIC CIRCUIT

From the above theory, if all the assumptions are correct, the plot of the current I_b against the input voltage E_1 on semi-logarithmic paper should be linear over nearly three decades with a slight deviation at the low end. The results of the circuit characteristics are given below, and the curve is shown in Fig. (17).

E_1 (volts)	I_b (ma.)
0.42	0.01
0.66	0.02
0.78	0.03
0.87	0.04
0.93	0.05
0.97	0.06
1.02	0.07
1.04	0.08

FIG. 17. CHARACTERISTICS OF THE DIODE ANTILOGARITHMIC CIRCUIT



E_1 (volts)	I_b (ma.)
1.07	0.09
1.13	0.10
1.30	0.20
1.45	0.30
1.51	0.40
1.55	0.50
1.61	0.60
1.65	0.70
1.67	0.80
1.69	0.90
1.75	1.0
1.95	2.0
2.05	3.0
2.13	4.0
2.20	5.0
2.25	6.0
2.28	7.0
2.30	8.0
2.35	10.0

From the plot of Fig. (17), the curve is linear over nearly three decades, with a slight deviation at the low end. This is due to the behavior of the 6J6 tube at very low currents. The results show that the assumptions and approximations are quite valid, and the current varies as the antilogarithm of the input voltage to within plus or minus 1 db.

(4) CURRENT DETECTION OF THE ANTILOGARITHMIC CIRCUIT

It is desirable that the output of the antilogarithmic circuit be a voltage output so that it may be used to drive any recording device. The current variation can be detected as a voltage variation by means of a load resistor in the plate circuit of the 6J6 tube. The circuit is then directly coupled to another d-c amplifier through a resistive chain so as to obtain a low d-c reference level, and to compensate for the attenuation caused by the resistive chain. A K2-W amplifier was used for this purpose, and the circuit is shown in Fig. (18). It was also desirable that the output voltage cover a three-decade range, and since the output of the K2-W is limited to 50 volts, the range would have to be between 0.05 and 50 volts. Experimental results showed that it was impossible to cover this range with a K2-W amplifier, since this involves very low currents and the amplification of a very low voltage variation, and the rejection ratio (VW) of the amplifier was too low to permit the amplification of such a small variation accurately. However, to test the feasability of such a circuit, it was decided to operate the circuit for a two-decade output. By means of the d-c level control of the first amplifier, the circuit may be biased so that the diode may operate on the two upper decades or two lower decades of its characteristic. Operation on the two upper decades involves a current range from 0.1 ma. to 10 ma., and with a 15 K plate load resistor this results in a plate voltage change of 298.5 volts to 150 volts. The second K2-W amplifier is capable of amplifying or following such a change even though there is an attenuation factor of about two caused by the resistive chain.

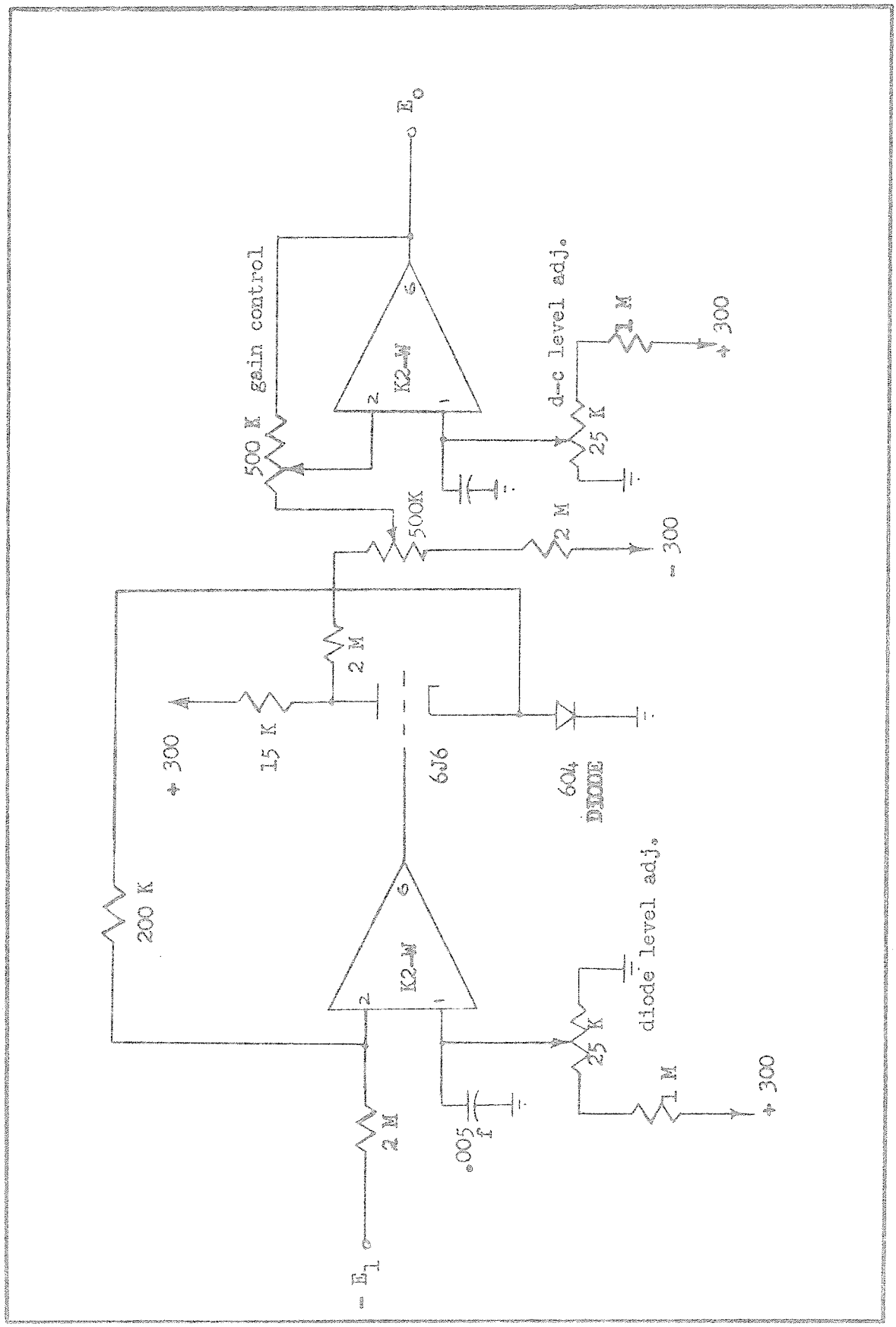


FIG. 18. THE EXTENDED DIODE ANTILOGARITHMIC CIRCUIT

The results of one such test are given below, and the plot of the curve is shown in Fig. (19).

E_1 (volts)	E_o (volts)
0.36	0.1
0.52	0.2
0.62	0.3
0.69	0.4
0.76	0.5
0.80	0.6
0.87	0.8
0.92	1.0
1.11	2.0
1.22	3.0
1.30	4.0
1.38	5.0
1.48	8.0
1.55	10.0
1.75	20.0
1.95	30.0

The curve of Fig. (19) shows that the behavior of the circuit is quite linear over two decades.

Operation on the two lower decades of the diode characteristics involves a current range from 0.01 ma. to 1.0 ma., and consequently a plate voltage change from almost 300 volts to 285 volts. The first of these two decades must cover a voltage change from 300 volts to 298.5 volts, a total change of almost 1.5 volts, and with the added

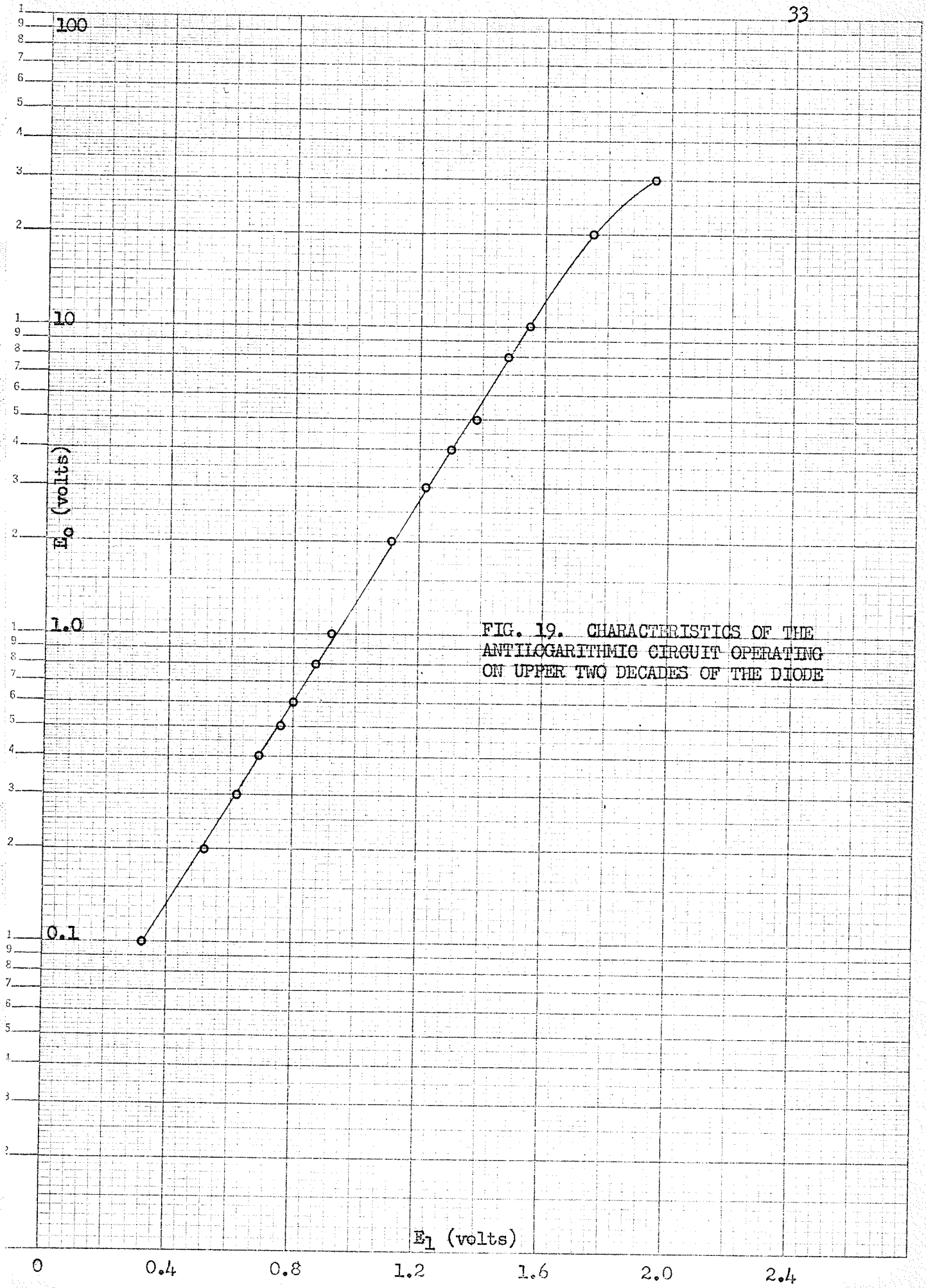


FIG. 19. CHARACTERISTICS OF THE ANTILOGARITHMIC CIRCUIT OPERATING ON UPPER TWO DECADES OF THE DIODE

attenuation factor of the resistive chain, this involves the amplification of a very small voltage variation. Results of this test condition are given below, and the plot of the curve is shown in Fig. (20).

E_1 (volts)	E_o (volts)
0.62	0.1
0.66	0.2
0.70	0.3
0.73	0.4
0.76	0.5
0.78	0.6
0.83	0.8
0.86	1.0
0.99	2.0
1.08	3.0
1.16	4.0
1.20	5.0
1.25	6.0
1.30	8.0
1.35	10.0
1.54	20.0
1.70	30.0

The curve of Fig. (20) shows a reasonable linearity in the upper decade of the output covering the range from 1.0 volt to 10 volts, but a marked curvature in the lower decade. This is due to the poor rejection ratio of the K2-W amplifier and the added inaccuracy of the basic circuit itself at low current operation.

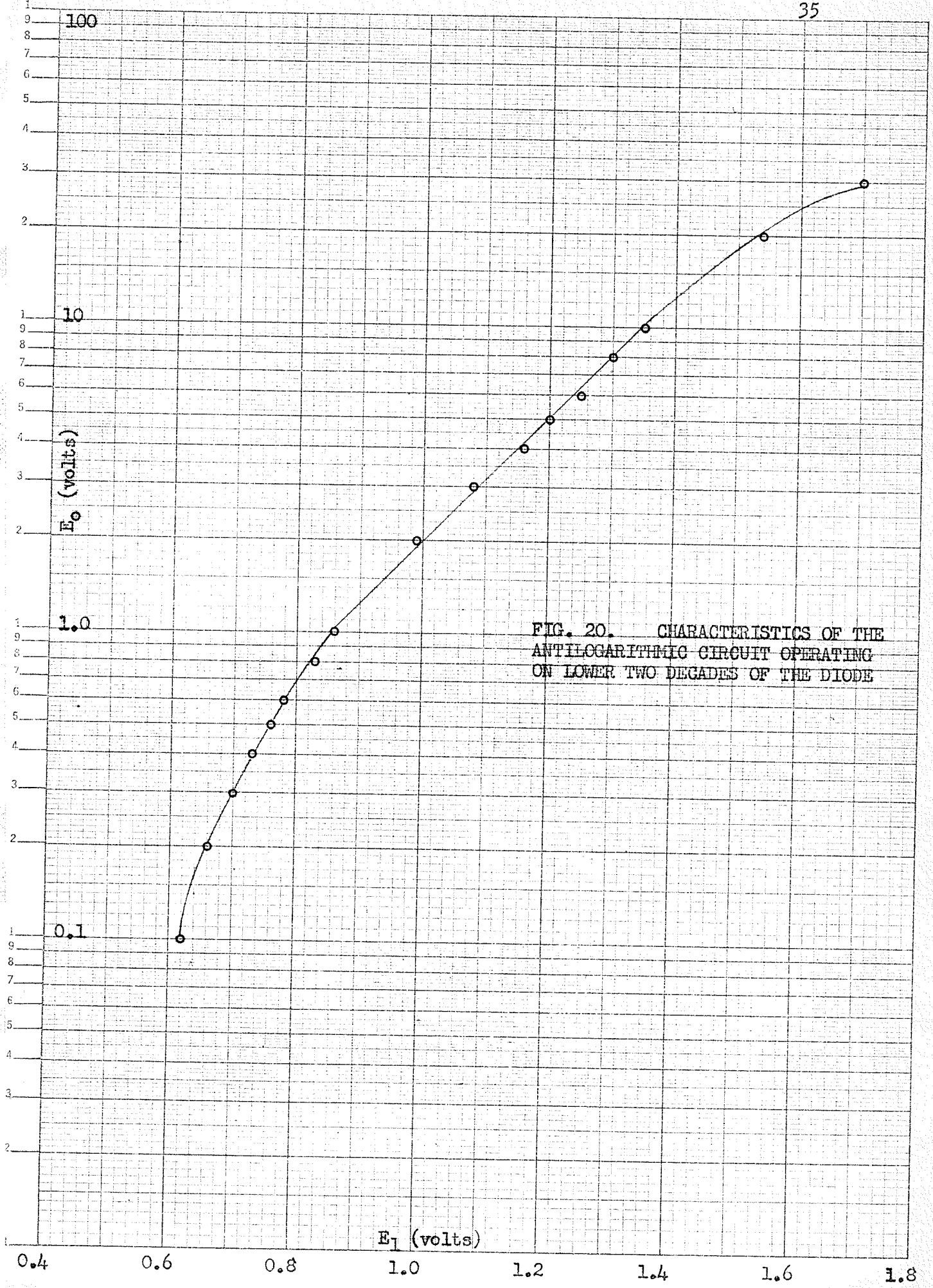


FIG. 20. CHARACTERISTICS OF THE ANTILOGARITHMIC CIRCUIT OPERATING ON LOWER TWO DECADES OF THE DIODE

In order to utilize the full three-decade range of the diode, it is therefore necessary to have a differential input amplifier with a very high rejection ratio. It is best to operate the network in an output voltage range of 0.1 to 100 volts, so that the amplifier must also be capable of delivering a large output. If such an amplifier can be found, then it is quite possible that this circuit will operate in a satisfactory manner, and together with the range-extending circuit described in the previous chapter, another complete antilogarithmic network may be designed.

Note: Temperature effects on the silicon diode were not investigated because it was thought that under normal operation of the circuit, the ambient temperature would not change sufficiently to warrant such an investigation.

CHAPTER 3

LOGARITHMIC CIRCUITS

The Complex-Plane Scanner contains twelve channels which are capable of computing the logarithm of the magnitude of a complex variable. The principal computing component of each channel is a Logaten 511E, which, as mentioned in the first chapter, was found to be inaccurate when used with alternating sinusoidal input voltages. Because of this discrepancy, it was desirable to investigate the possibility of other logarithmic circuits which may be more stable and accurate. The availability and characteristics of the 604C silicon diode suggested a starting point for such an investigation, and the results of this investigation are presented in this chapter.

(1) THE SERIES RESISTOR CIRCUIT

The characteristics of the 604C silicon diode show that the voltage across its terminals is proportional to the logarithm of the current through the diode. If then we can find a circuit such that the input signal is proportional to the current through the diode, then the output voltage taken across the diode terminals will be proportional to the logarithm of the input voltage. This condition can be approximated by using a high resistor in series with the diode. Since the voltage drop across the diode is small, varying from 0.6 to 0.8 volts, the total drop across the resistance and diode will be approximately equal to the drop across the resistance alone. Thus the voltage drop across the circuit will be proportional to the current through the circuit, except at very low current values.

Since the initial voltage drop across the diode is 0.6 volts, the initial drop across the total circuit should be at least 1.0 volt. For a corresponding current of 0.01 ma., the series resistor should then be about 40 K. For an upper limit of 10 ma., the input voltage will then have to be about 400 volts. For practical purposes, it was decided that the upper limit of the input signal be 100 volts, so that the maximum current for a 40 K series resistor will be 2.5 ma. If the maximum current of 10 ma. at 100 volts is desired, then the series resistor must be 10 K. With this value, the minimum value of the current must be 0.04 ma. In either case, it is seen that the full three-decade range of the diode from 0.01 ma. to 10 ma. can never be utilized. However, to test the feasability of such a circuit, a K2-W amplifier was connected as a voltage follower to provide a signal source of low output impedance. Because the output current of the K2-W is limited to about 1.0 ma., a 30 K resistor was used in series with the diode. The voltage output across the diode was further amplified by means of another K2-W connected in the conventional manner as a voltage amplifier. The circuit is shown in Fig. (21). The initial drop of 1.0 volt across the resistor and diode can be adjusted by means of the level control on the K2-W follower, and any arbitrary reference level on the output can be fixed by the level control of the K2-W amplifier. The results of the circuit characteristics are given below and the plot of the curve is shown in Fig. (22).

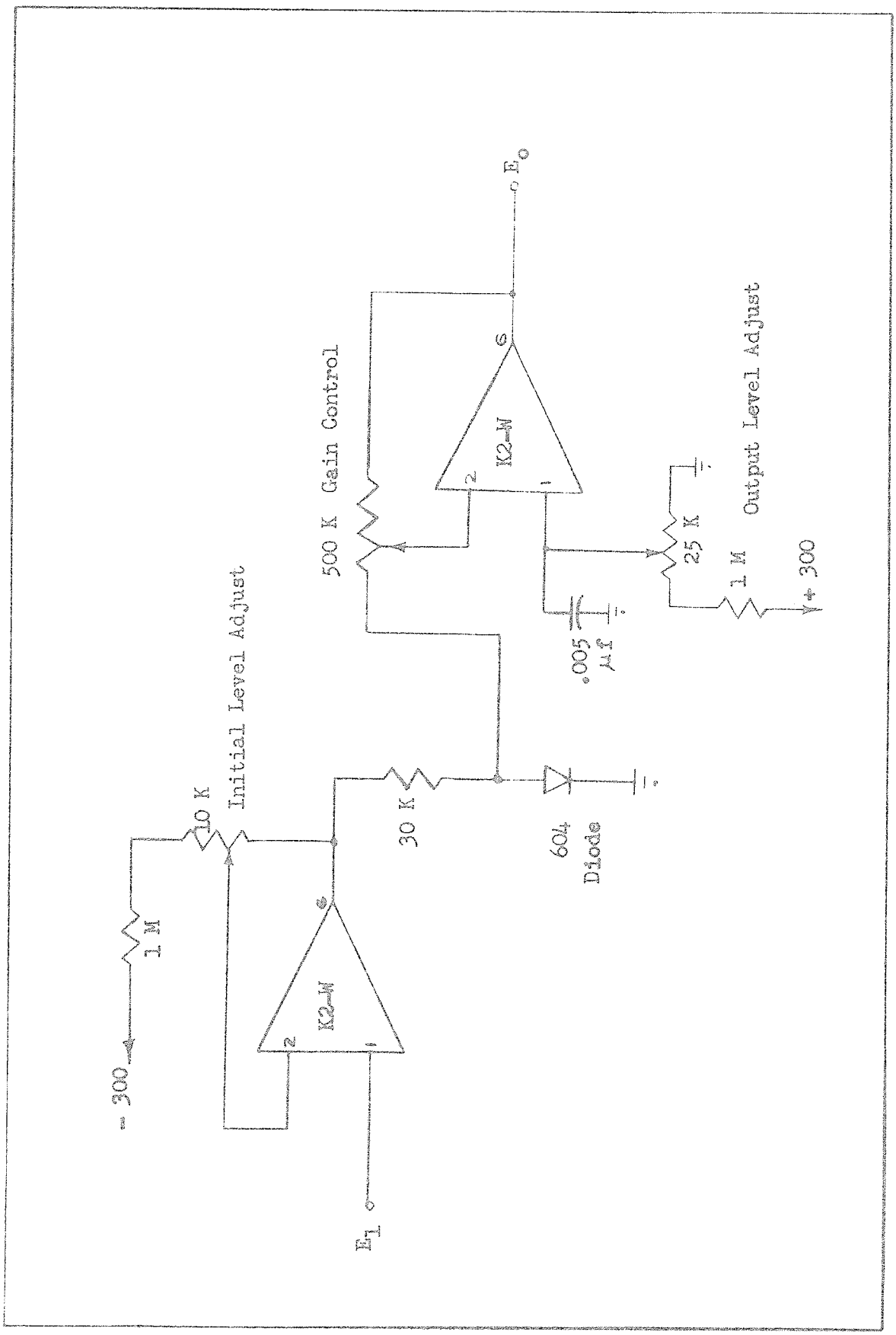


FIG. 21. THE SERIES RESISTOR LOGARITHMIC CIRCUIT

E_1 (volts)	E_o (volts)
0.05	1.06
0.1	1.12
0.2	1.26
0.3	1.38
0.4	1.50
0.5	1.58
0.6	1.63
0.7	1.70
0.8	1.75
0.9	1.82
1.0	1.85
2.0	2.22
3.0	2.45
4.0	2.61
5.0	2.72
6.0	2.82
7.0	2.92
8.0	2.98
9.0	3.05
10.0	3.10
20.0	3.50
30.0	3.75
40.0	3.90

From the curve of Fig. (22), it is seen that the logarithmic circuit is linear for almost two decades, the curve at the low end

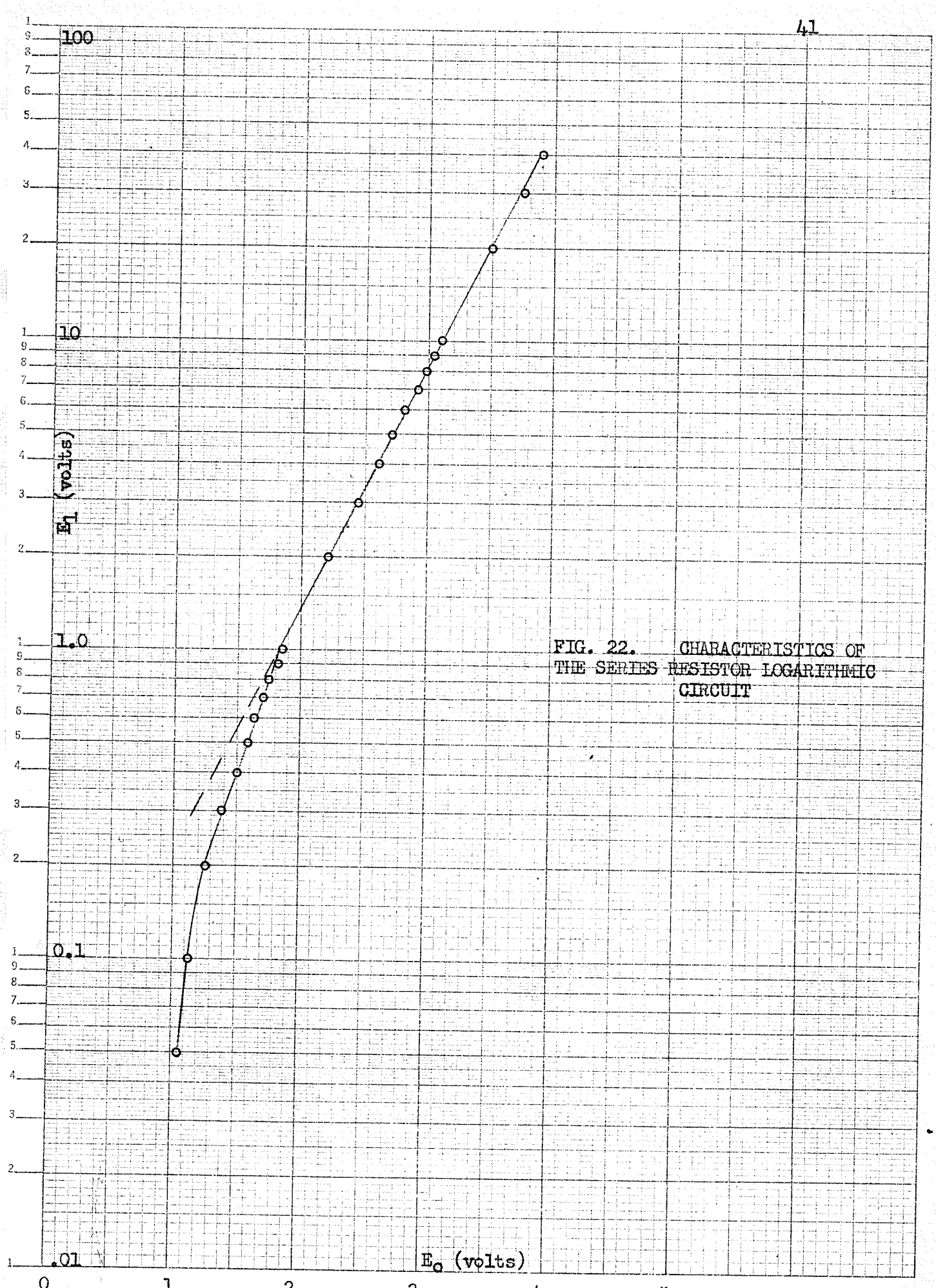


FIG. 22. CHARACTERISTICS OF THE SERIES RESISTOR LOGARITHMIC CIRCUIT

being due to the fact that the approximation that the voltage across the resistor is proportional to the current through the diode is not valid at low voltage inputs. Since the circuit is reasonably accurate at high voltage inputs, then if a follower amplifier capable of delivering an output of 100 volts is used in place of the K2-W follower, then a logarithmic circuit accurate to within plus or minus 1.0 db over a two and a half decade range may be easily constructed.

(2) THE CURRENT SOURCE CIRCUIT

The basic and most straight-forward logarithmic circuit using the properties of the 604C silicon diode is simply a current source applied to the terminals of the diode. A current source can be approximated by using a vacuum tube, and the logarithm of the current in the plate circuit of the network will be proportional to the voltage across the diode. However, the problem of making the input signal proportional to the tube current arises. Using a 6J6 tube as shown in Fig. (23), the following characteristics were obtained.

E_1 (volts)	I_b (ma.)	E_o (volts)
0	6.10	0.785
1	5.80	0.780
2	5.10	0.775
3	4.65	0.770
4	3.95	0.765
5	3.10	0.760
6	2.35	0.758
7	1.60	0.740

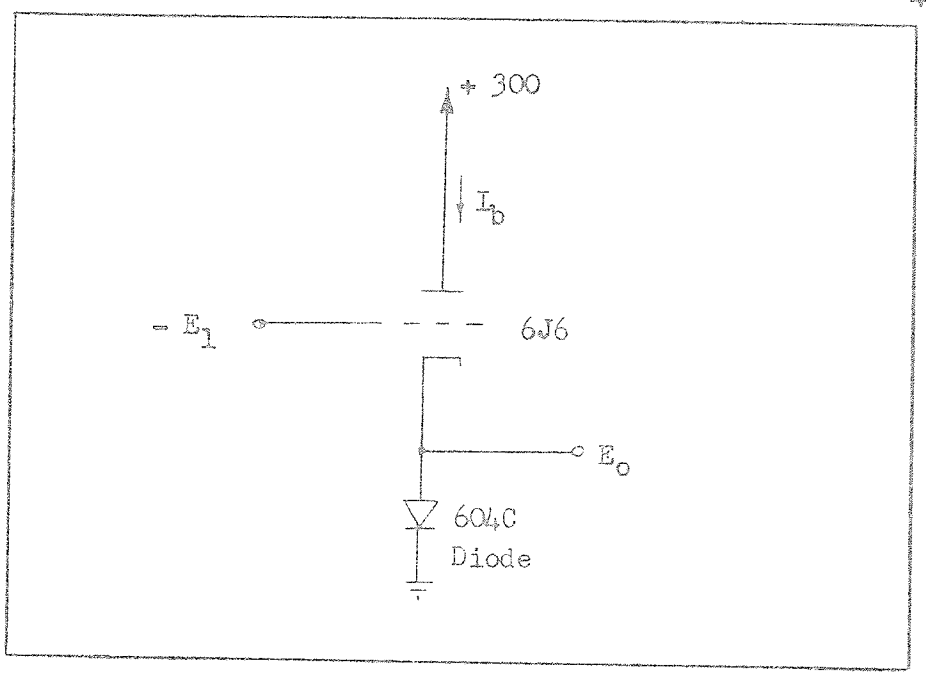


FIG. 23. THE CURRENT SOURCE CIRCUIT

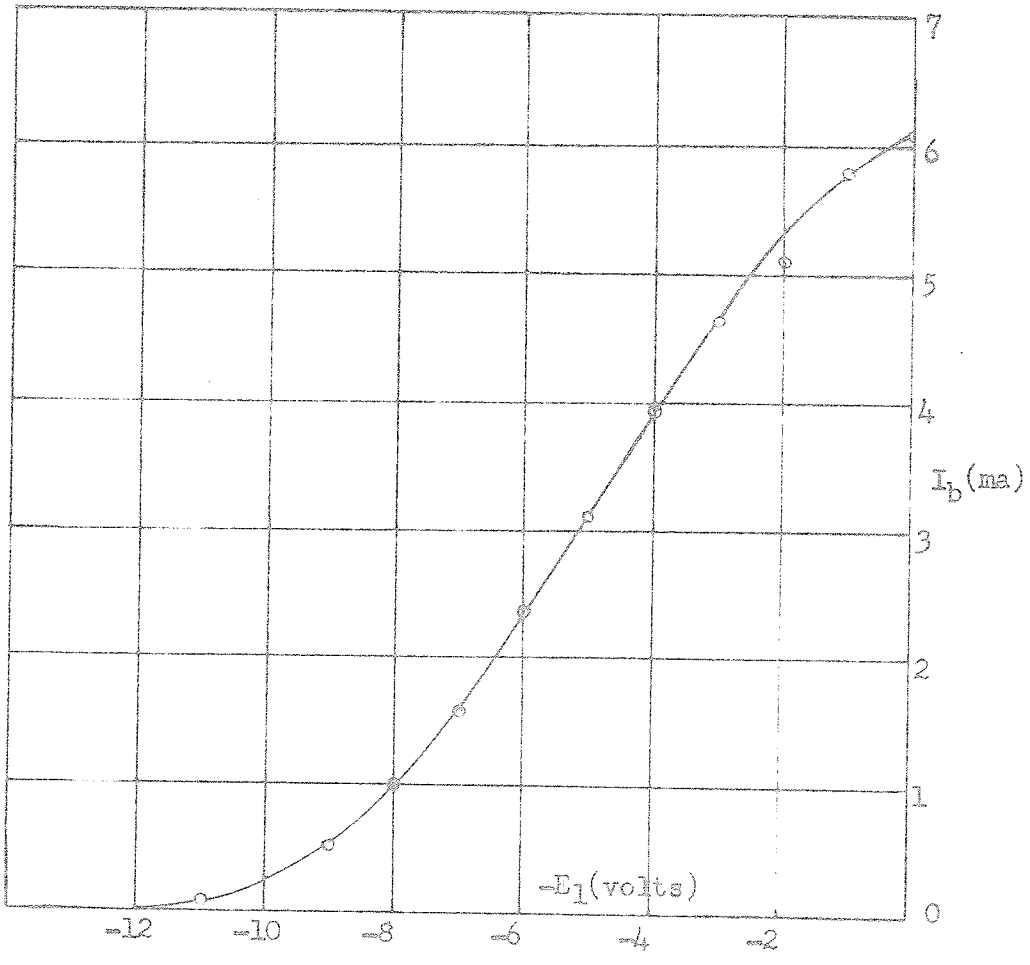


FIG. 24. TRANSFER CHARACTERISTIC OF THE 6J6 TUBE

E_1 (volts)	I_b (ma.)	E_o (volts)
8	1.00	0.730
9	0.53	0.715
10	0.27	0.695
11	0.115	0.670
12	0.0375	0.645
12.2	0.0285	0.630
13	0.0079	0.595

A plot of the current against the output voltage results in a curve similar to that of Fig. (15), and linear over three decades. However, a plot of current against the input voltage shows that the curve can be considered approximately linear over a small range. The curve is shown in Fig. (24), and the linear portion of the curve covers a current range from 1 ma. to 5 ma. approximately. This means that only half of a decade of the uppermost portion of the diode characteristic can be utilized to obtain a logarithmic circuit.

The input signal may be made proportional to the tube current by using a d-c amplifier with a differential input, and a feedback loop to compensate for the transfer characteristics of the tube. Such a circuit is shown in Fig. (25). The input signal is applied to the positive input of a K2-W amplifier, and its output is applied to the grid of the 6J6 tube. A small resistor is placed in the cathode circuit of the tube so that a voltage proportional to the tube current may be fed back to the negative input of the K2-W.

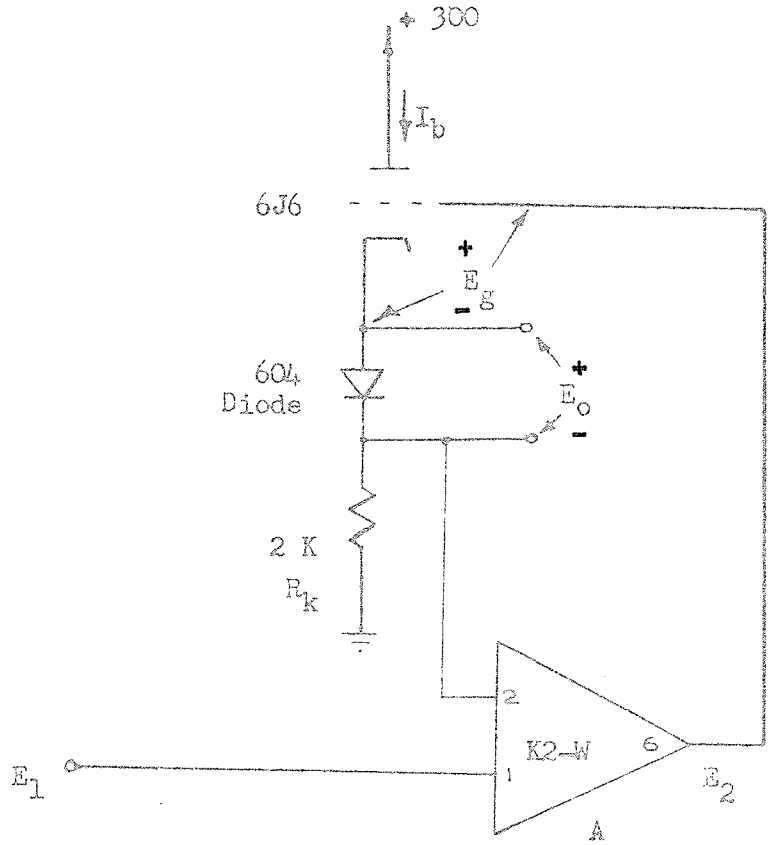


FIG. 25. THE COMPENSATED CURRENT SOURCE CIRCUIT

From the circuit diagram we have;

$$E_2 = A(E_1 - I_bR_k) + (A/r)(E_1 + I_bR_k)$$

where r is the common mode rejection ratio, and,

$$E_g = E_2 - E_o - I_bR_k .$$

Solving these equations, we get,

$$E_1 = (I_bR_k)(1 + A - A/r)/A(1 + 1/r) + (E_o + E_g)/A(1 + 1/r)$$

and if A is large, the second term on the right-hand side of the equation can be neglected, so that the input signal will be proportional to the tube current. However, from the practical aspects of the circuit, it was found that the initial input level must be at least 8 volts for the circuit to operate, and the output across the diode had a varying reference level. This reference level reaches a comparatively high value, so that in order to measure and amplify the voltage change across the diode, an amplifier with a differential input of extremely high rejection ratio is needed. Such an amplifier was not readily available, but it is possible to design a suitable one (MT). Such a project was not undertaken, and since the circuit was very susceptable to drift, together with the problem of proper d-c levels, the circuit was abandoned in favour of the circuit to be described in the following section.

(3) THE DIODE FEEDBACK CIRCUIT

Consider the circuit of Fig. (26). The 604C diode is placed in the feedback loop between the output and the input grid of the d-c amplifier. The current through the diode is proportional to the antilogarithm of the voltage across its terminals, so that, neglecting grid current, and writing the nodal equation at the grid of the amplifier, we have,

$$(-E_1 - E_g)/R_1 = -I = -K_1 10^{K_2(E_o - E_g)}$$

and since $E_o = -AE_g$, then,

$$E_1 - E_o/A = R_1K_1 10^{K_2E_o}(1 + 1/A)$$

If the gain of the amplifier, A, is very large, we get,

$$E_1 = R_1K_1 10^{K_2E_o};$$

from which,

$$\log E_1 = K_2E_o + K_3 \qquad (14)$$

where $K_3 = \log R_1K_1$.

Equation (14) may be re-written as,

$$K_2E_o = \log E_1 - K_3$$

or,

$$E_o = 1/K_2 \log E_1 - K_3/K_2. \qquad (15)$$

The value of K_1 is 10^{-12} ma., and that of K_2 is 16.3 volts^{-1}, so that if R_1 is chosen as 15 K, the value of K_3 becomes -10.824 .

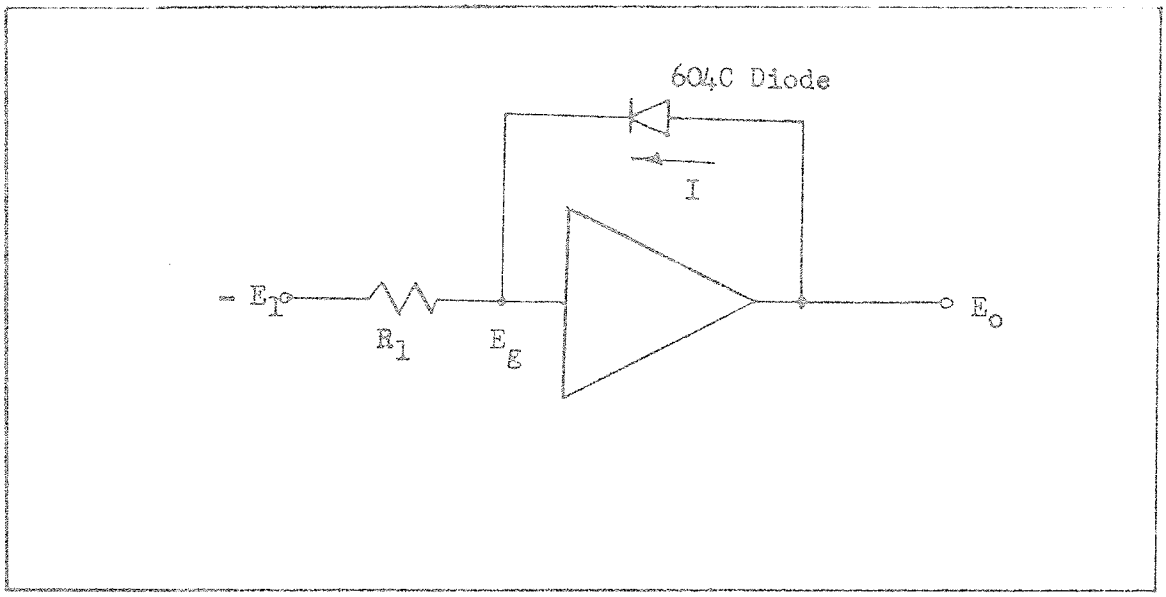


FIG. 26. THE DIODE FEEDBACK CIRCUIT

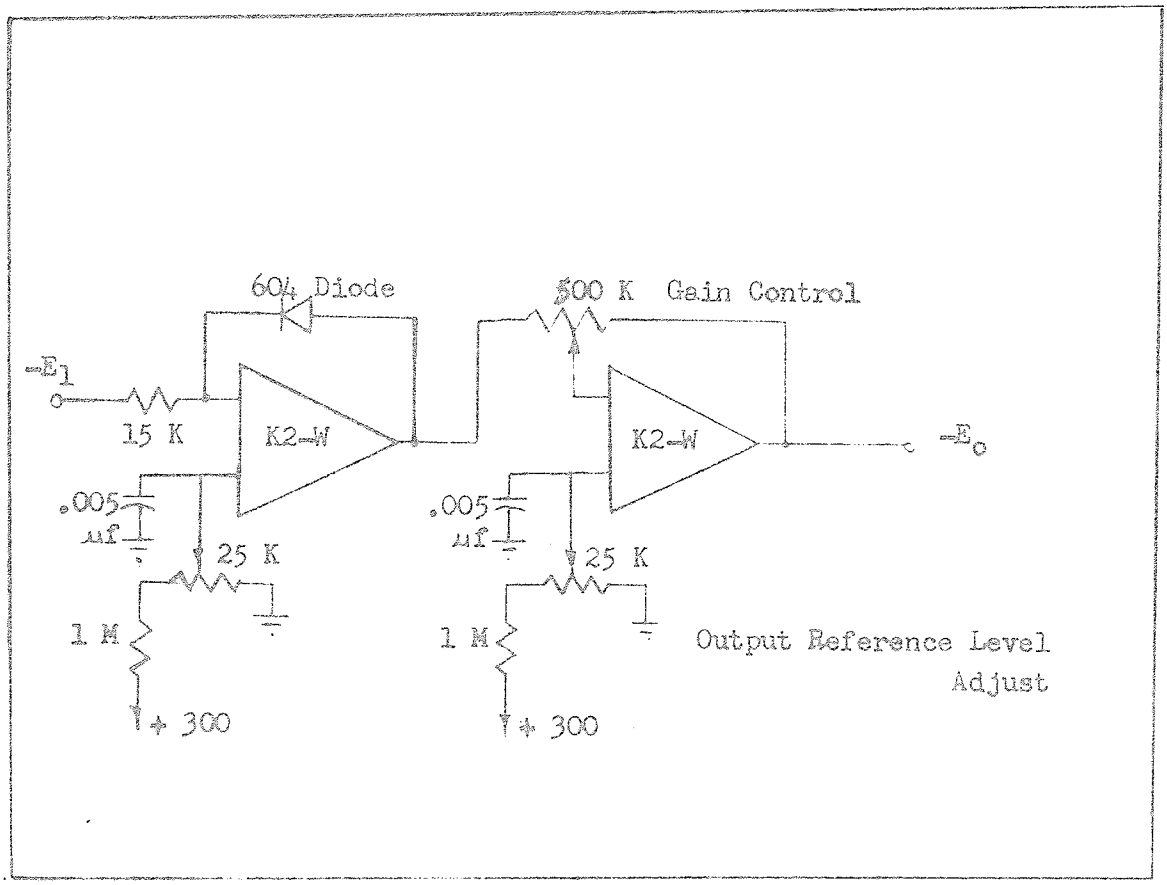


FIG. 27. THE K2-W DIODE FEEDBACK CIRCUIT

With these values, then for an output range between 0.6 and 0.8 volts, the input range is between 0.09 and 160 volts. This is very desirable since the practical range needed for the input was for design purposes set at the three decades from 0.1 to 100 volts. To test the characteristics of this circuit, a K2-W amplifier was used in the basic circuit, and another K2-W used to amplify the logarithmic output. The circuit is shown in Fig. (27). Results of the characteristics of the circuit are given below, and a plot of the curve is shown in Fig. (28).

E_1 (volts)	E_o (volts)
0.1	1.00
0.2	1.20
0.3	1.31
0.4	1.44
0.5	1.55
0.6	1.65
0.7	1.72
0.8	1.80
0.9	1.86
1.0	1.92
2.0	2.37
3.0	2.58
4.0	2.74
5.0	2.86
6.0	2.96
7.0	3.06

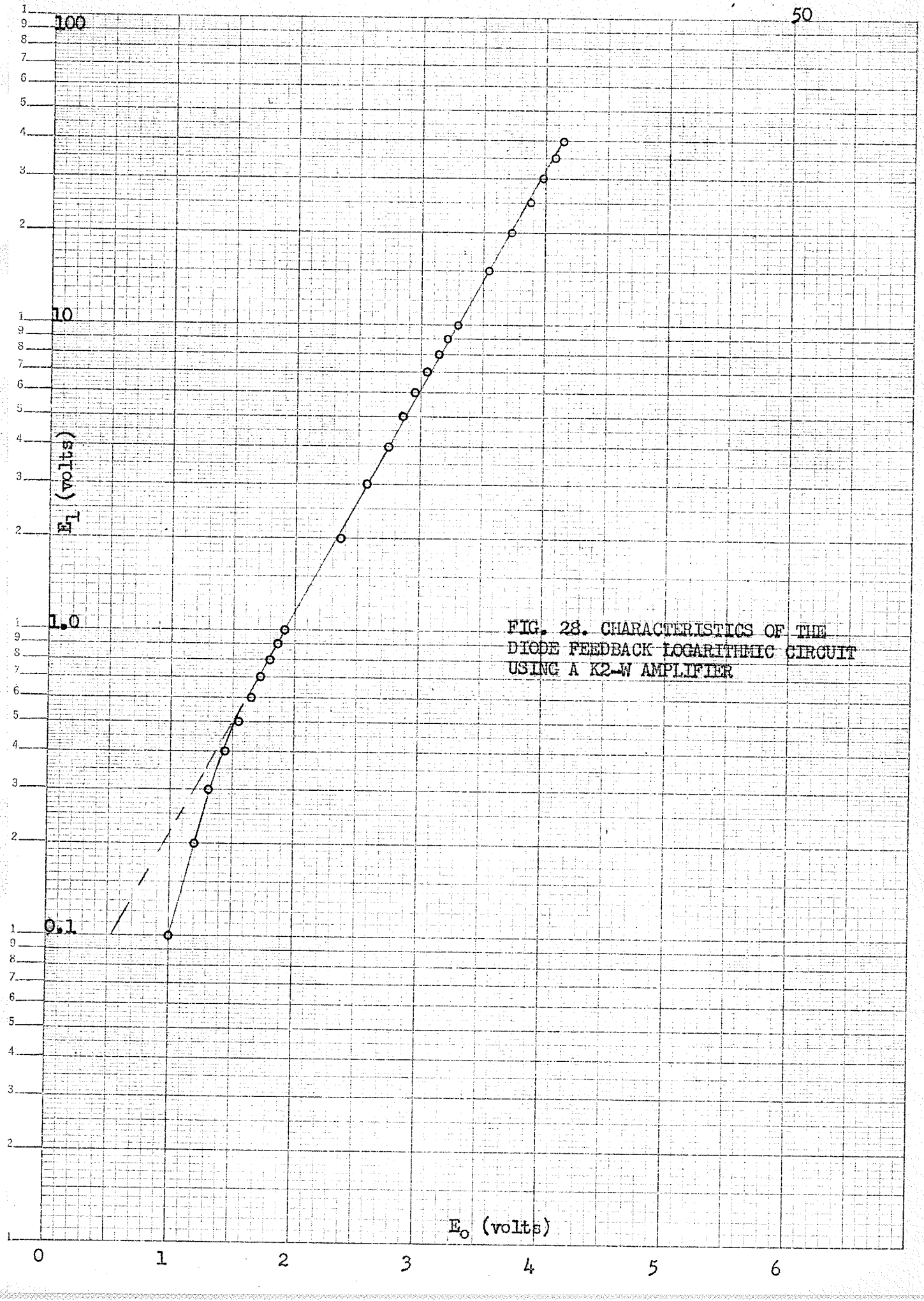


FIG. 28. CHARACTERISTICS OF THE DIODE FEEDBACK LOGARITHMIC CIRCUIT USING A K2-W AMPLIFIER

E_1(volts)	E_o(volts)
8.0	3.15
9.0	3.22
10.0	3.30
15.0	3.56
20.0	3.73
25.0	3.87
30.0	3.98
35.0	4.08
40.0	4.14

From the curve of Fig. (28), it is seen that the circuit is quite reasonably accurate for two decades. The upper limit of the input voltage for this circuit is determined by the output current limitations of the main K2-W amplifier, and the deviation of the curve at the low input end is mainly due to amplifier drift. If, therefore, a stabilized d-c amplifier capable of output currents in excess of 10 ma. were used in the circuit, the three decade input range should be attainable. For this condition, it was decided to use the UPA-2 amplifier (See Appendix) which was previously used in the antilogarithmic circuit described in the first chapter. Replacing the K2-W by the UPA-2 amplifier in the basic circuit of Fig. (27), the following results were obtained.

E_1(volts)	E_o(volts)
0.1	0.40
0.2	0.89
0.3	1.37

E_1(volts)	E_o(volts)
0.4	1.73
0.5	1.95
0.6	2.17
0.7	2.34
0.8	2.48
0.9	2.62
1.0	2.78
2.0	3.52
3.0	4.01
4.0	4.32
5.0	4.57
6.0	4.78
7.0	4.92
8.0	5.10
9.0	5.20
10.0	5.30
20.0	6.10
30.0	6.55
40.0	6.90
50.0	7.10
60.0	7.38
70.0	7.50
80.0	7.70
90.0	7.85
100.0	7.95
110.0	8.10

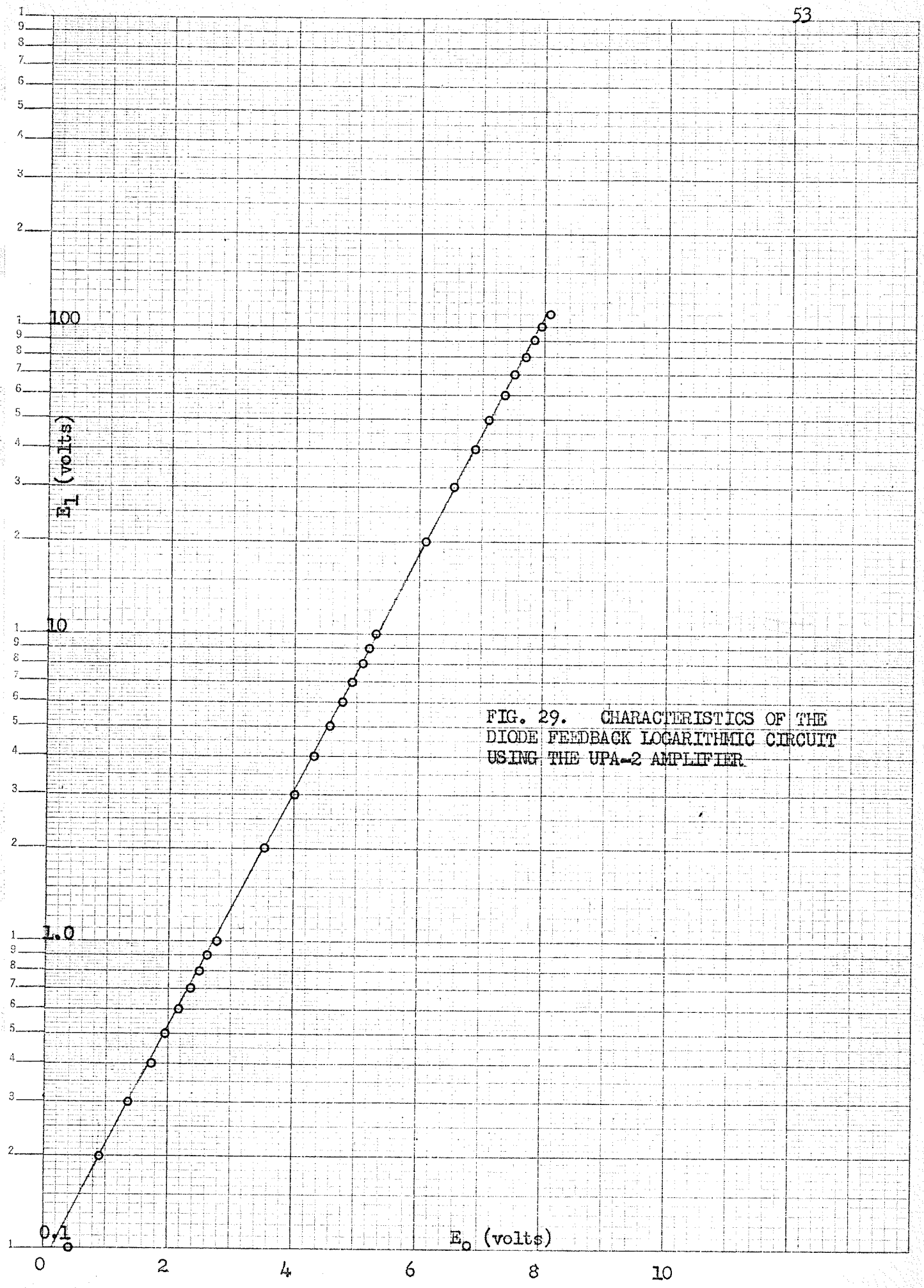


FIG. 29. CHARACTERISTICS OF THE DIODE FEEDBACK LOGARITHMIC CIRCUIT USING THE UPA-2 AMPLIFIER

The plot of the characteristics is shown in Fig. (29), and the curve shows that the desired linearity over three decades was obtained. This circuit is theoretically and practically accurate, and because of the utilization of the chopper stabilized UPA-2 amplifier, errors due to noise and drift are negligible.

Of all the logarithmic circuits discussed in this chapter, this final circuit is the best, and although the cost of the UPA-2 amplifier is comparatively high, the total cost of this circuit is comparable to that of the Logaten 511E. However, the basic circuit operates only on negatively varying signals, so that its application with positively varying and sinusoidal alternating signals will involve the use of inverting amplifiers and detectors.

CHAPTER 4

DESIGN OF A NEW CHANNEL FOR THE COMPLEX-PLANE SCANNER

With the success of finding a stable and reliable logarithmic circuit, and the availability of the convenient K2-W plug-in d-c amplifiers which were found to be very reliable within their specifications, it was decided to design a new channel for the Complex-Plane Scanner using the above components wherever possible. In this way it was hoped to eliminate many of the errors of the old channel, especially those due to the inaccuracy of the Logaten 5llE, and thus improve the performance of the Complex-Plane Scanner.

(1) THE OLD CHANNEL

The function of each channel is to compute the logarithm of the magnitude of a complex variable factor of the form $(s - s_k)$, where s is the complex frequency variable, and s_k represents a pole or zero position of the complex function, and is called a critical frequency of the function. The critical frequency s_k is composed of a real and imaginary components represented by σ_k and jw_k.

The components s, σ_k, and jw_k are simulated by sinusoidal voltages (Va), their magnitudes being proportional to the magnitudes of the corresponding voltages. Signals representing -s, σ_k, and jw_k are summed and amplified in the channel by an amplifier called the Logaten Driver Amplifier. Because of the inversion caused by the amplifier, the output voltage now represents the factor $(s - s_k)$. This output - a sinusoidal voltage varying in magnitude - is then

fed to the Logaten. This is where the main source of error lies. The output of the Logaten, which now represents the factor $A \log (s - s_k) + B$, is amplified by the Detector Driver Amplifier, and peak detected. The constants A and B are due to the characteristics of the Logaten. The Peak Detector can detect either negatively or positively, depending on whether the component s_k represents a pole or a zero, and its output represents the term $C \log (s - s_k) + D$. This output is then fed to the summing amplifier of the antilogarithmic network. The constants C and D include the constants A and B, and although the value of D is not of much importance in this application, the value of C must be known accurately, since this constant introduces a power index in the value of the magnitude computed by the antilogarithmic circuit. The block diagram of this channel is shown in Fig. (30).

(2) DESIGN CONSIDERATIONS OF THE NEW CHANNEL

Since the logarithmic component of the new channel can operate only on negatively varying inputs, it is therefore necessary that the detector unit must be placed ahead of the logarithmic unit and operated for negative detection only.

Also, in order to utilize the full input range of the logarithmic unit, the output from the detector, and consequently the output of the summimg amplifier which precedes the detector, must have a maximum peak value of at least 100 volts. Since a K2-W amplifier is incapable of such an output, it was therefore necessary to design a booster amplifier to be used with the K2-W as a summing amplifier. For reasons of stability, the booster amplifier should

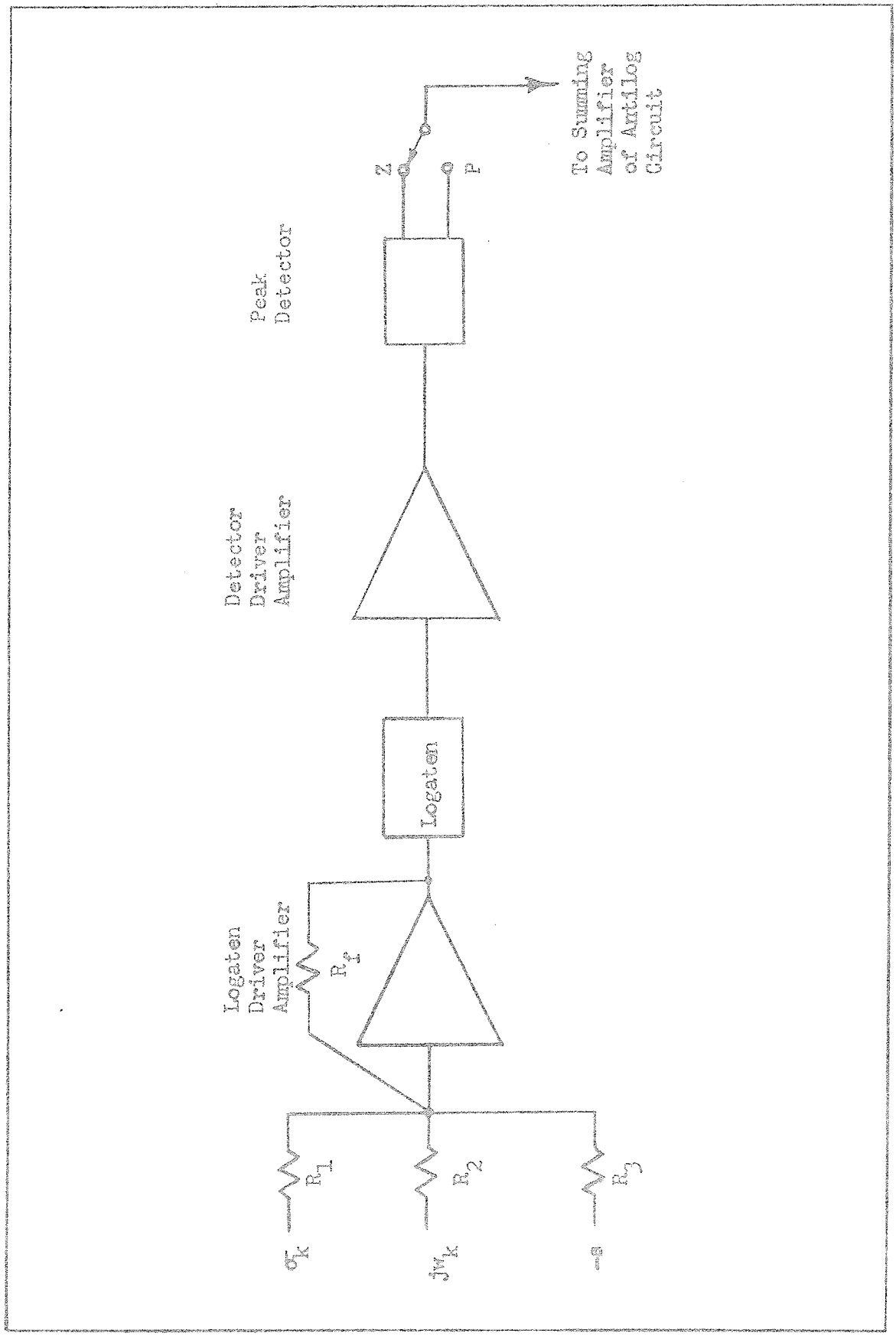


FIG. 30. BLOCK DIAGRAM OF THE OLD CHANNEL

operate within the overall feedback loop of the summing system.

It is also desirable that the constants introduced by the channel be eliminated in the final output, and at the same time the channel must be able to represent the factor due to either a pole or a zero. These functions can be accomplished by means of a single K2-W amplifier placed behind the logarithmic unit. The summing amplifier, detector circuit, and final output amplifier are discussed in the following sections.

(3) THE BOOSTER AMPLIFIER AND SUMMING AMPLIFIER

In order to obtain an output swing of plus or minus 100 volts from the booster amplifier, a 5687 tube was used in the output stage. One section of the tube was used as an amplifier to give the required output, and the other section was used as a cathode follower. Since the object of the booster made it desirable that the output should be in phase with the booster input, another stage of amplification was necessary. For this, a 6AN8 tube was used as the input stage, the pentode section being used as an amplifier stage, and the triode section as a cathode follower stage. Internal feedback loops were used around each stage of amplification so as to stabilize the whole network. The circuit diagram is shown in Fig. (31). The gain of the booster by itself was found to be approximately 9, and it may be used as a separate unit. The circuit of Fig. (32) shows how the booster may be used together with a K2-W amplifier to give an increased output. However, to increase the stability of the summing amplifier, it is highly desirable that the

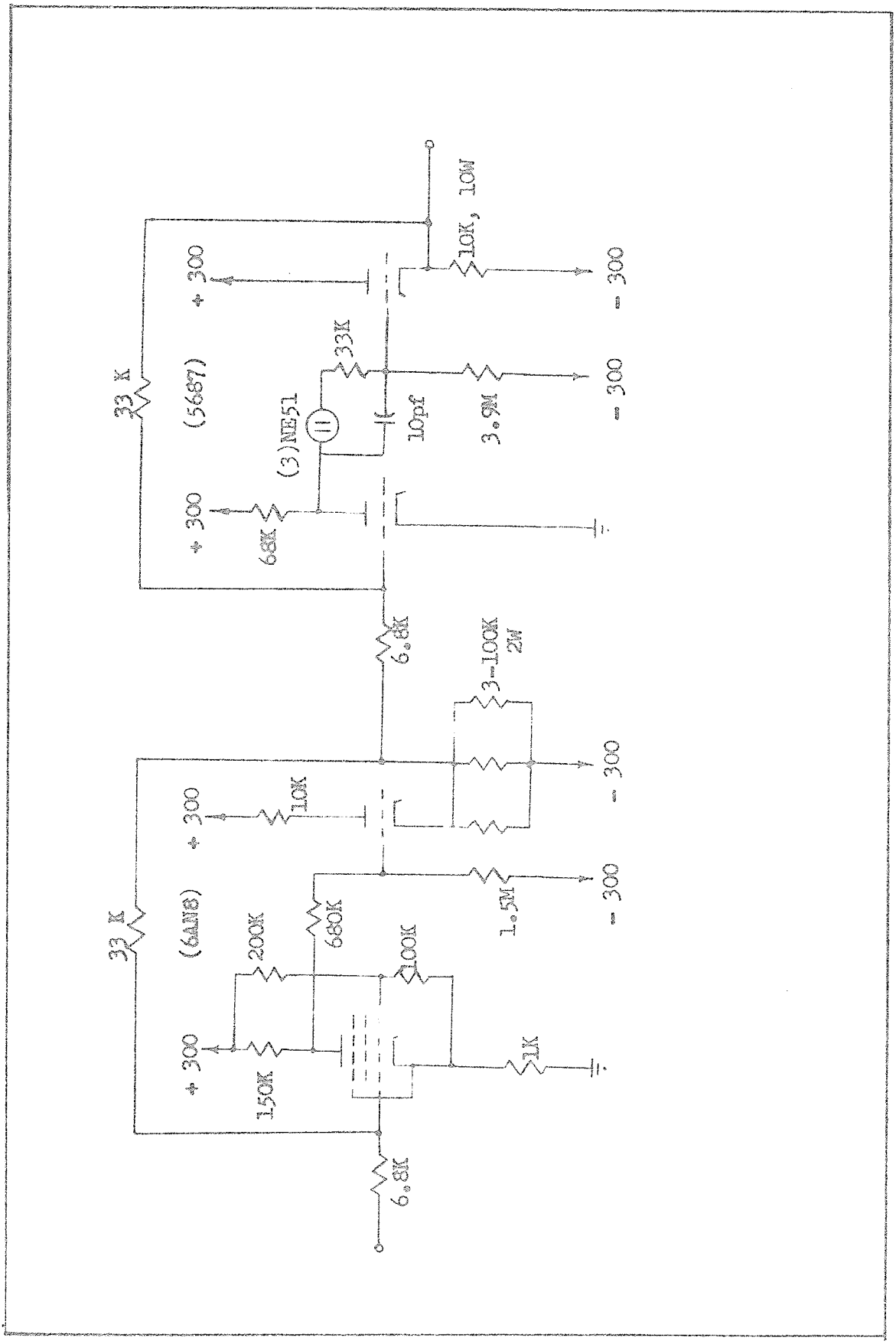


FIG. 31. BOOSTER AMPLIFIER CIRCUIT DIAGRAM

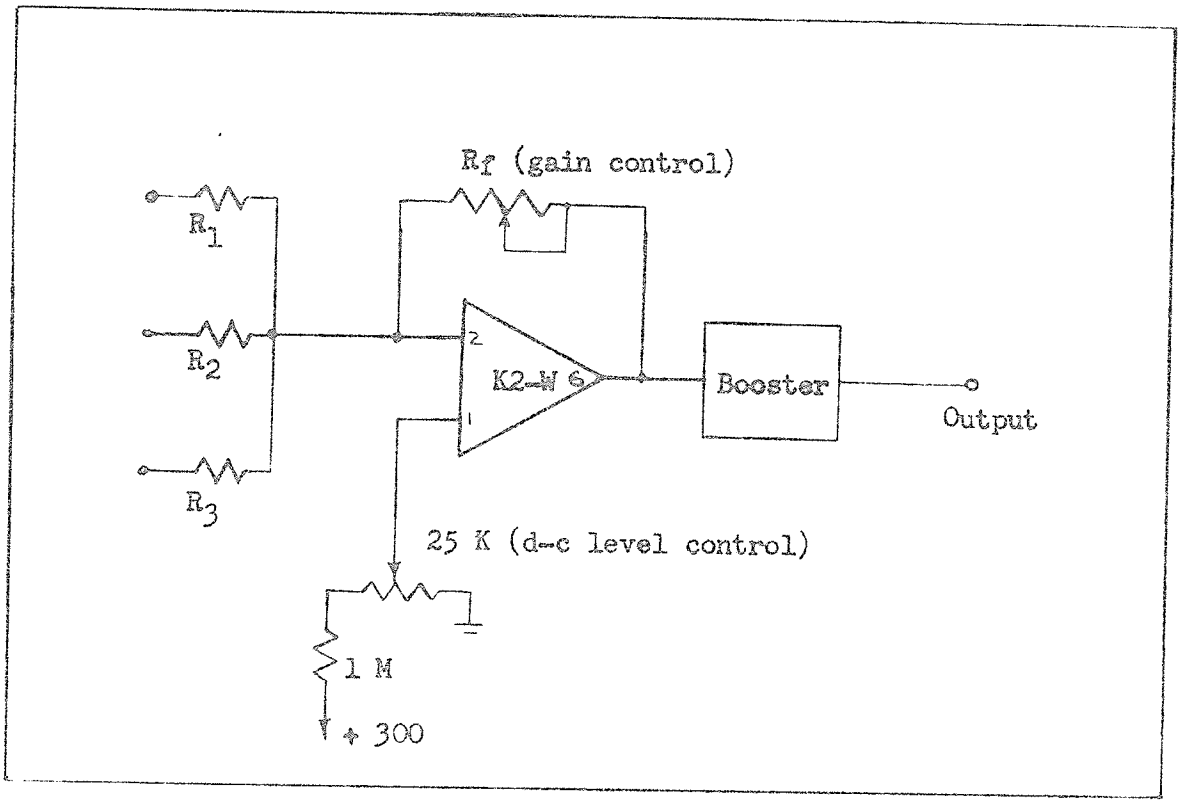


FIG. 32. SUMMING AMPLIFIER WITH EXTERNAL BOOSTER

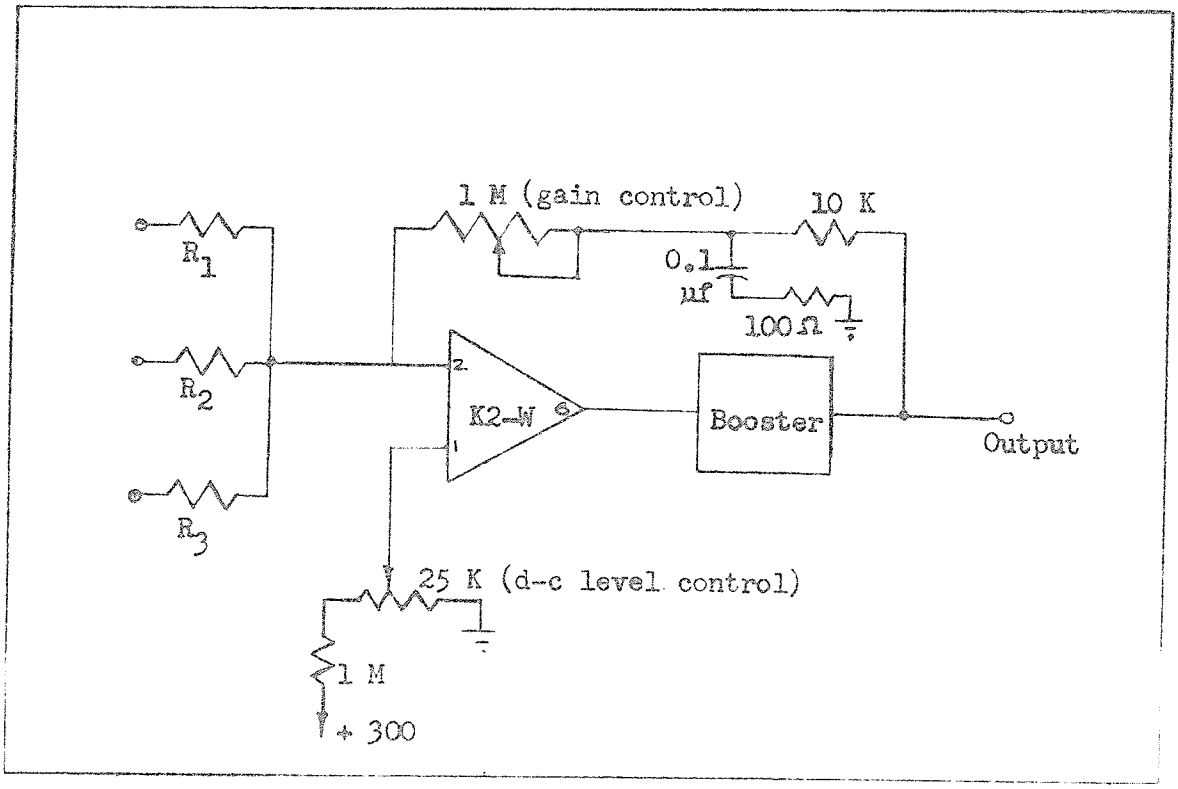


FIG. 33. SUMMING AMPLIFIER (BOOSTER WITHIN FEEDBACK LOOP)

booster be within the feedback loop of the network. With the normal, purely resistive, feedback loop, it was found that the system was unstable, giving rise to oscillations, if the overall gain were less than two hundred. For the purpose of the system, this gain was too high, and it was necessary that the gain should be adjustable for all values, especially in the vicinity of unity. To do this, the feedback loop had to be modified, and it was found that a lag network placed in the feedback loop completely stabilized the system. The final circuit of the summing amplifier with booster is shown in Fig. (33).

(4) THE DETECTOR CIRCUIT

The detector unit which follows the summing amplifier must be able to follow the negative peaks of the amplifier output, since the detector output, which becomes the input of the logarithmic unit, must be a negatively varying signal. For the sake of simplicity, a single diode and capacitor were considered for the detector circuit. A Type 1N1084 diode and a 0.02 μf capacitor were used, the cathode of the diode being connected to the amplifier output terminal for negative detection. It was found that in this system the d-c output of the detector was very close to the peak value of the amplifier output, except for small outputs, and that the detector output had a negligible ripple if there were no load, or a very high impedance load, on the system. It was found, also, that the diode itself operated with approximately a two volt drop across

its terminals, so that for small signals the system was inoperative. To overcome this difficulty, the diode must be negatively biased initially at two volts, so that very small peak values may be detected. This can be done very easily by means of the d-c level control of the summing amplifier. If the detector is to detect a peak signal of 0.1 volt, this bias must be set quite accurately, and remain fixed at that point. This is also not difficult, but if there is any drift in the amplifier, the change in bias level will cause the sensitivity of the detector to decrease.

It was also found that if the logarithmic unit were connected to the detector so far discussed, the loading effect caused the ripple voltage to increase tremendously. Since the output impedance of the detector should be low, and its load impedance high, the idea of a cathode follower between the basic detector unit and the logarithmic unit appeared to be a reasonable and simple solution. Using one section of a 5687 tube for the follower stage, since a high current output was essential, the complete detector system was found to be very satisfactory, the output from the cathode follower containing a negligible amount of ripple. In order to obtain the right output level, the output from the cathode follower was taken across a large portion of the cathode resistor. It was found that this circuit was capable of over 100 volts output with a 10 K load resistor. The complete detector circuit is shown in Fig. (34).

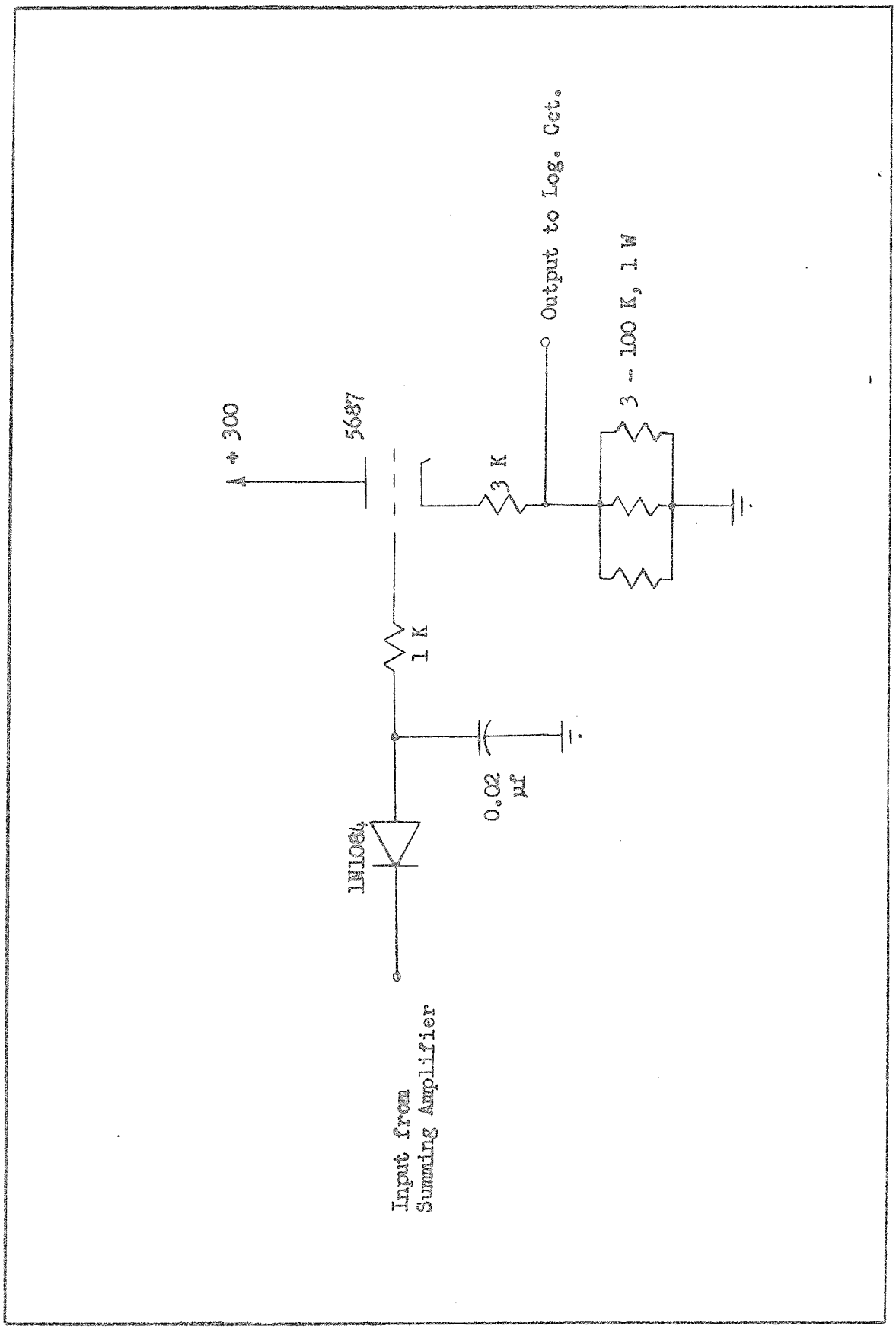


FIG. 34. THE DETECTOR CIRCUIT

(5) OUTPUT STAGE OF THE NEW CHANNEL

The output from the detector circuit will simulate the magnitude of the complex variable factor $(s - s_k)$, and the output of the logarithmic unit which follows the detector unit in the channel will represent the quantity C log $(s - s_k)$ + D. (cf: Eqn. 15. P.47). As mentioned previously, it is necessary that the constant C be known accurately, or eliminated completely. Also, if the term $(s - s_k)$ is due to a pole of the complex function, the channel output should represent - log $(s - s_k)$, and if the term is due to a zero of the function, the output must represent log $(s - s_k)$. These two functions can be accomplished by a single K2-W amplifier. The gain of the amplifier can be adjusted to the value 1/C, and the negative or positive sign of the output can be obtained simply by using the negative or positive input terminal of the amplifier. A single switching arrangement is all that is necessary to accomplish this function. The value of D is of not much importance, but this too can be eliminated by means of the d-c level control of the amplifier. The circuit arrangement of the output stage is shown in Fig. (35).

(6) PERFORMANCE AND CHARACTERISTICS OF THE NEW CHANNEL

To sum up, the new channel consists of a summing amplifier, a detector unit, the logarithmic unit, and finally the output amplifier. The block diagram of this channel is shown in Fig. (36).

In order to test the performance of this channel, certain preliminary adjustments were first made on the summing amplifier and the detector. A single sinusoidal signal was applied to the

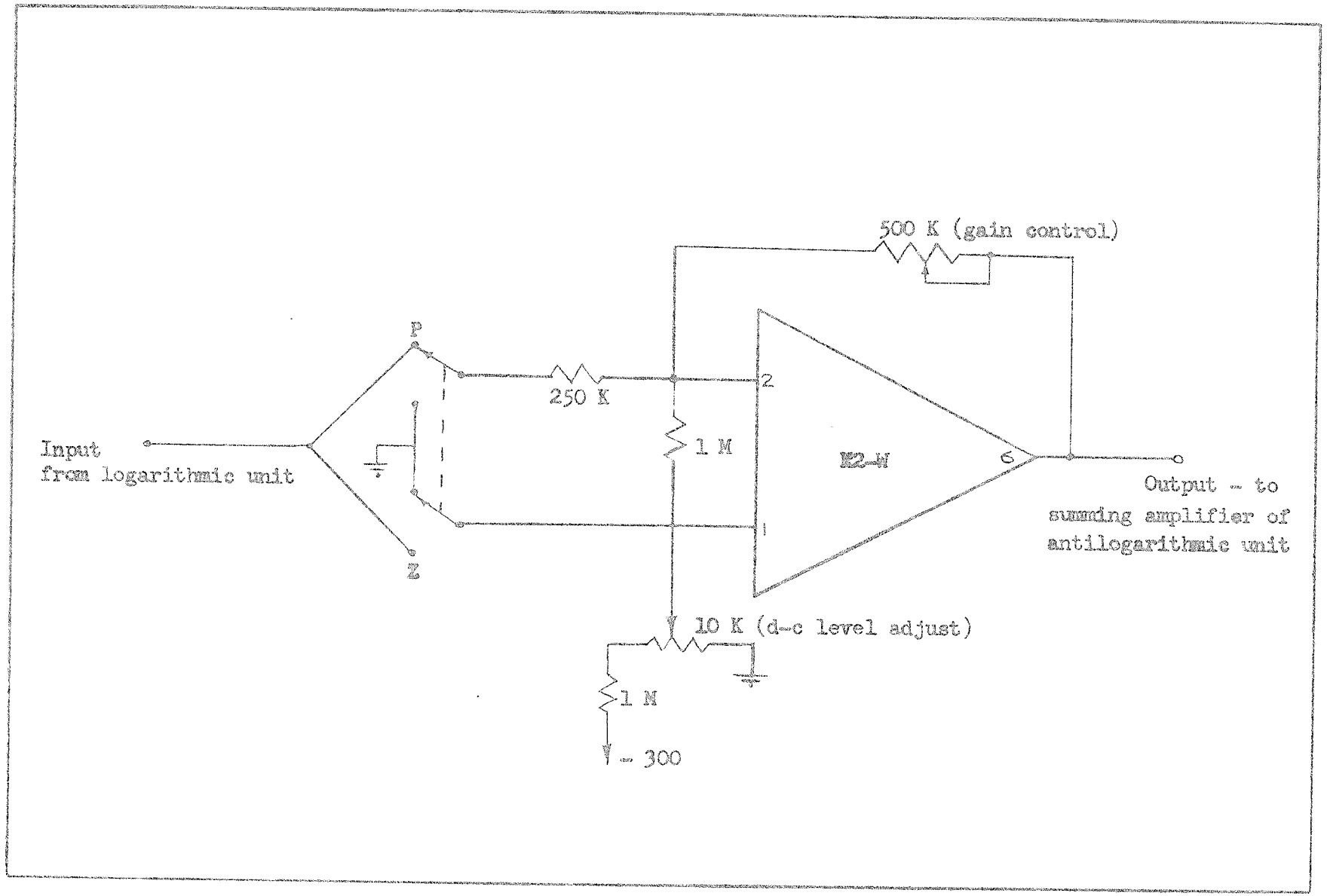


FIG. 35. OUTPUT STAGE OF NEW CHANNEL

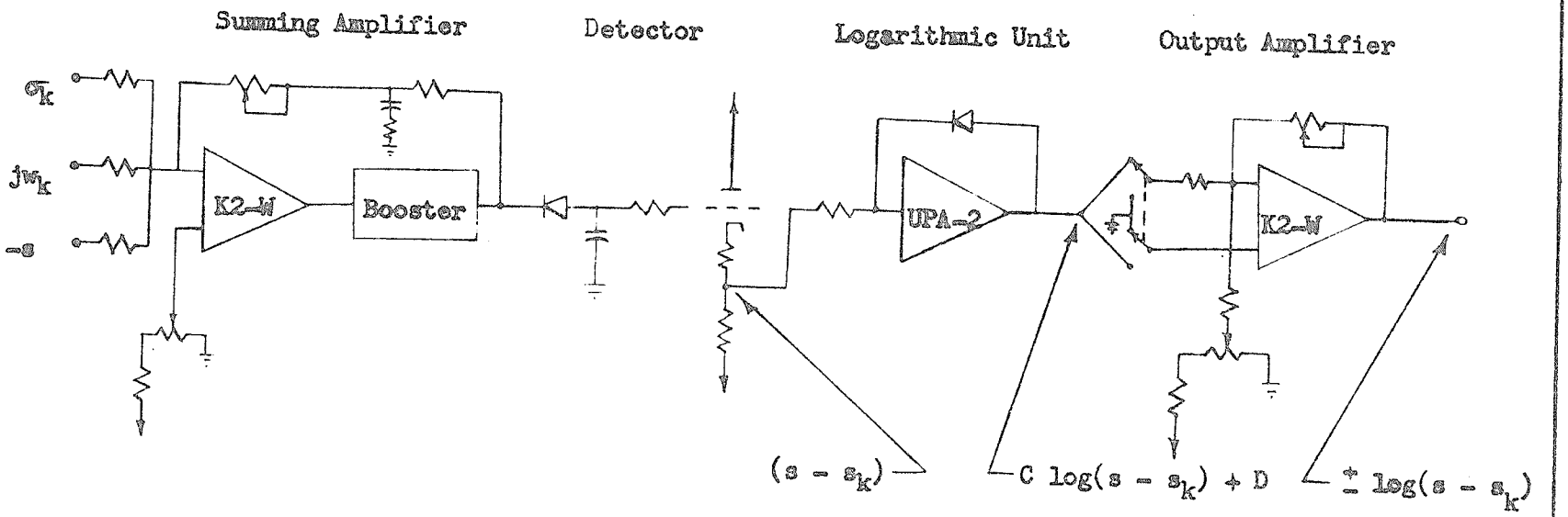


FIG. 36. BLOCK DIAGRAM OF NEW CHANNEL

summing amplifier, and the gain control was adjusted for unity gain. The input signal was then made a value of 0.07 volts rms. and the d-c level control adjusted until the d-c output of the detector was -0.1 volts. This adjustment was to ensure the proper bias on the detector diode. The signal strength was increased, and the detector output was checked to make sure that the detector output was proportional, if not equal, to the peak value of the input signal. The logarithmic unit, and then the output amplifier were connected to the detector. The gain and level controls of the final amplifier were not adjusted to compensate for the channel constants, but adjusted to amplify the output from the logarithmic unit so that point by point readings of the input and output could be made with the best possible accuracy. The results of one such test on the channel characteristics are given below.

E_{in} (rms. volts)	E_o (d-c volts)
0.07	0.30
0.1	0.52
0.2	0.75
0.3	0.89
0.4	1.00
0.5	1.08
0.6	1.14
0.7	1.30
0.8	1.38
0.9	1.50
1.0	1.55

E_{in}(rms. volts)	E_o (d-c volts)
2.0	2.05
3.0	2.42
4.0	2.50
5.0	2.55
6.0	2.70
7.0	2.72
8.0	2.85
9.0	2.90
10.0	2.95
20.0	3.50
30.0	3.78
40.0	3.90
50.0	4.15
60.0	4.20
70.0	4.32

The plot of this curve is shown in Fig. (37).

The test circuit of this new channel was made up of bench models of each separate component, and consequently the readings were subject to much 60 cycle pick-up noise. The readings are therefore not as accurate as they might be. Nevertheless, they are good enough to give a fair picture of the performance of the channel. From the curve of Fig. (37), it is seen that the mean curve through the points is linear over nearly two and a half decades, with a downward deviation in the lowermost half decade. This deviation

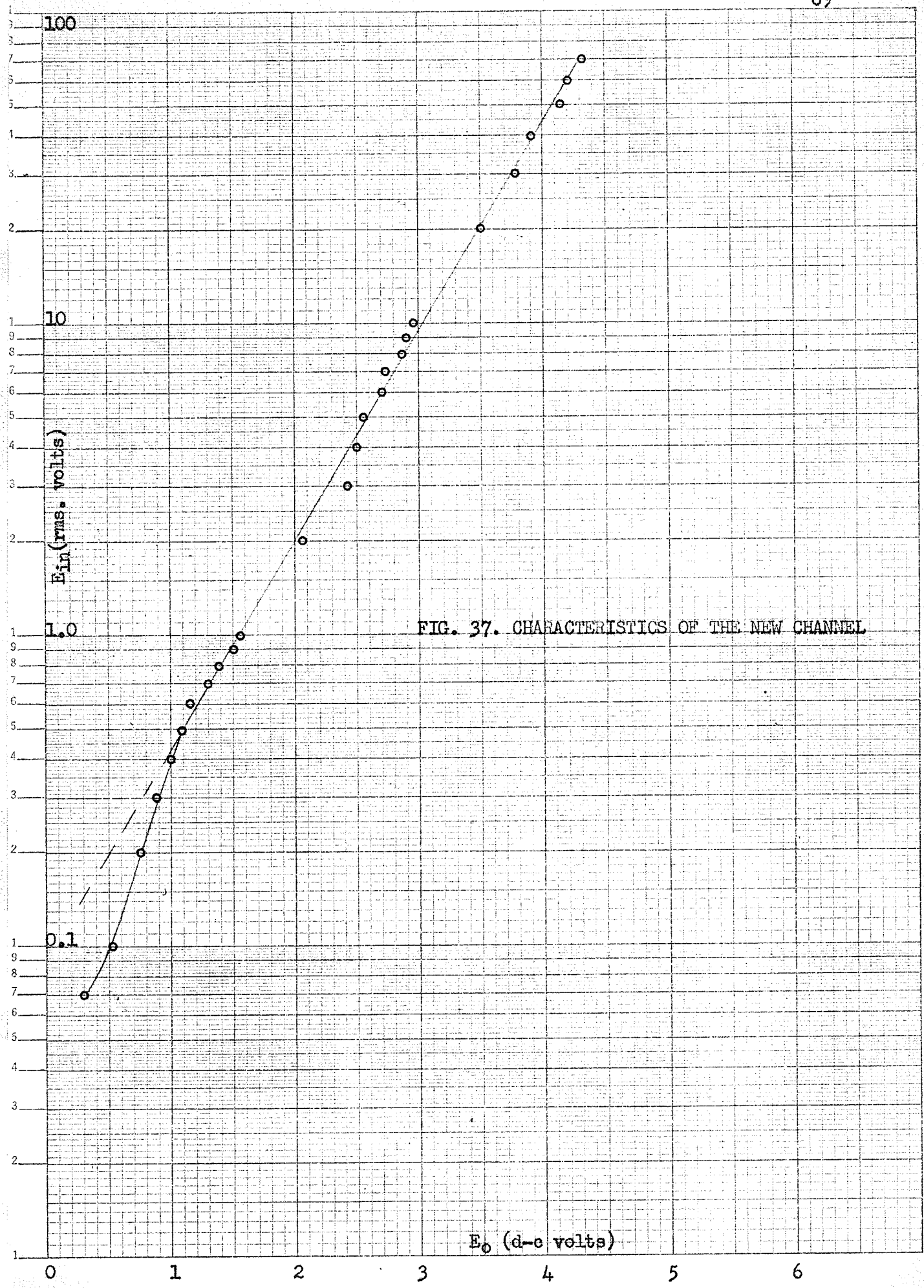


FIG. 37. CHARACTERISTICS OF THE NEW CHANNEL

was found to be due mainly to drift in the summing amplifier, which caused a shift in the bias on the detector diode. This is the critical problem of this new channel. It is absolutely necessary that the bias on the detector diode be fixed accurately and be completely stable, as any change in this bias will cause an error at low input values. This in turn necessitates the complete stabilization of the summing amplifier. This can be done by using a chopper stabilizer unit for each amplifier, but since there are twelve channels, the cost of such stabilization is extremely high. As a project for future development and improvement of the channel, the idea of using a single chopper unit to stabilize all the channels (KK) may be considered. The basic scheme of this system is to connect the single chopper unit in periodic succession to each amplifier by means of a motor-driven commutator-type switch. Complete shielding of all components and the use of shielded leads should eliminate the errors due to 60 cycle noise.

APPENDIX

THE K2-W OPERATIONAL AMPLIFIER

GENERAL SPECIFICATIONS

Gain:
15,000 d-c open loop

Power Requirements:
4.5 ma at + 300vdc
4.5 ma at - 300vdc
0.6 amp at 6.3 vac (or dc)

Tubes:
2 12AX7

Impedances:
Either Input:
Above 100 megohm
(Open Grid)
Output:
Open loop - below 1 K
Fully fed back - below 1 Ω

Drift Rate:
± 5 mv per day,
referred to the input

Voltage Range:
Both Inputs:
- 50 vdc to + 50 vdc
Output: - 50 vdc to + 50 vdc

Input Current:
Either input: Less than 0.1 μa

Output Current:
- 1 ma to + 1 ma,
driving 50K load from
- 50 vdc to + 50 vdc

Input Bias:
For balance, a bias adjustable from 0 to 2.6 vdc is used in series with either input(Pin 1 positive with respect to Pin 2)

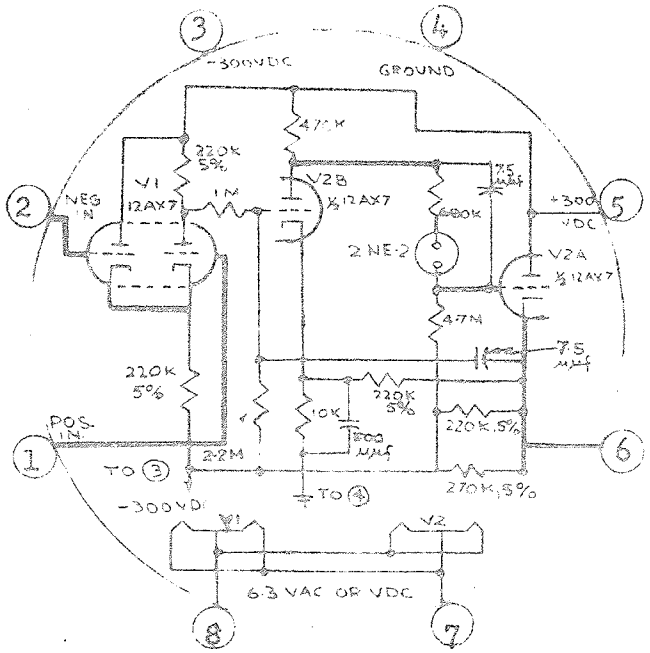
Response:
2 μsec rise time with bandwidth over 100 kc when used as an inverter

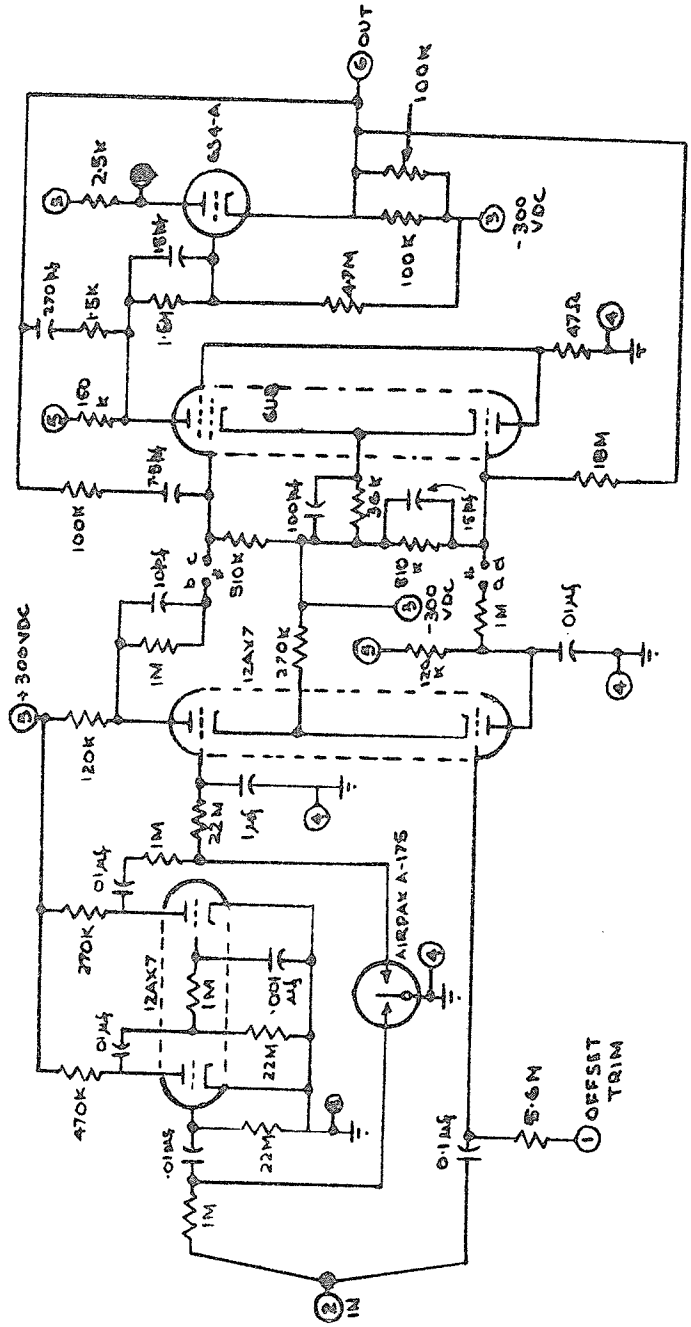
Casing:
Molded plastic, sealed unit

Base:
Octal plug

Height:
4½ in. overall

Weight:
Installed: 3 oz.





CIRCUIT DIAGRAM OF THE UPA-2 AMPLIFIER

UPA-2 CHARACTERISTICS

ITEM	MIN.	DESIGN CENTRE	MAX.
INTERNAL PERFORMANCE			
Overall d-c gain of amplifier before feedback	10^7	5×10^7	Infinite
Effective output resistance before feedback	350 ohms	1000 ohms	1400 ohms
As a gain-of-100 amplifier, d-c effective output resistance		0.01 ohm	
Effective capacitance from summing point to ground		9 uuf	
Effective resistance from summing point to ground		1 M	
Input d-c current (balanced normal operation)		10^{-11} amp.	
Approximate frequency at which open-loop gain drops to unity		1 Mc	
"Break frequency" (-3 db point) when connected as a gain-of-100 amplifier	7½Kc	10Kc	12Kc
Noise (appears from two separate sources):			
A. Due to apparent noise voltage in series with input grid, peak to peak.	100uv	200uv	350uv
B. Due to apparent noise current fed into summing point, peak to peak.	0.002ua*	0.004ua*	0.006ua*
Drift (long term) referred to input after allowing time for temperatures to stabilize	20uv	50uv	100uv

*With terminal 7 (heater) grounded. However, this can usually be improved by afactor of 20 or better by connecting a 500 ohm potentiometer across the heaters, grounding its wiper arm, and adjusting for minimum noise, instead of grounding terminal 7.

UPA-2 CHARACTERISTICS

	MIN.	DESIGN CENTRE	MAX.
OUTPUT CURRENT (MAX. AVAILABLE)			
At +100v output:			
Steady state positive	+18 ma	+22 ma	+27 ma
Steady state negative	-7.5	-8	-8.4
At zero output:			
Transient positive	+38	+42	+46
Steady state positive	+14	+14	+14
Steady state negative	-5.5	-6	-6.3
At -100v output:			
Transient positive	+58	+63	+68
Steady state positive	+10	+10	+10
Steady state negative	-3.5	-3.8	-4.0
POWER REQUIRED			
6.3v ± 10% at 50-70 cps			2.0 amp

	DESIGN CENTRE	
	Quiescent	Fully loaded with output at +100v
+ 300 vdc supply	12 ma	35 ma
- 300 vdc supply	17 ma	29 ma

TUBE COMPLEMENT

2 - 12AX7 1 - 6U8 1 - 6S4A

Chopper: 1 - Airpax A-175, or 172, or equal.

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