Controller Implementation and Performance Evaluation of a High Power Three-Phase Active Power Filter using Controller Hardware-in-the-Loop Simulation

by

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Abstract

This thesis presents a demonstration of Real-Time High-Speed controller hardware-in-the-loop (CHIL) testing for a digital signal processor (DSP) -based controller of a shunt active power filter (APF) for medium voltage (MV) grid power quality improvements. A recently developed Real-Time and high-speed simulator (RT Box) and a DSP are used for the CHIL simulation to validate the control algorithms which are implemented in a commercial low-cost DSP. The filter reference current is extracted based on synchronous reference frame theory. Hysteresis current control is employed to generate PWM switching signals for controlling the APF to inject compensating currents into the grid. The direct current (DC) side capacitor voltage level of the APF is maintained by a PI controller. The results show the APF associated with the implemented controller can mitigate variety power quality problems, such as harmonic elimination, power factor correction, and load balancing. The whole CHIL simulation system work stable with high switching frequency.

Acknowledgments

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Thank my parents for your unconditional and endless support, inspiration and encouragement with my study and work. I am honoured to have you as my parents. I would love to say thank you to my wife for her understanding and countless sacrifices to support me to achieve this point.

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Nomenclature

Symbol	Description
$\boldsymbol{\theta}$	Phase Angle
PQ	Power Quality
PCC	Point of Common Coupling
THD	Total Harmonic Distortion
TDD	Total Demand Distortion
APF	Active Power Filter
IGBT	Insulated-Gate Bipolar Transistor
HV	High Voltage
HP	High Power
LP	Low Power
HF	High Frequency
EMI	Electromagnetic Interference
RCP	Rapid Control Prototyping
HIL	Hardware-in-the-Loop
DSP	Digital Signal Processor
CHIL	Controller Hardware-in-the-Loop
I/O	Input/Output
PWM	Pulse Width Modulation
DFT	Discrete Fourier Transform
FFT	Fast Fourier Transform
RDFT	Recursive Discrete Fourier Transform
SRF	Synchronous Reference Frame
PLL	Phase-Locked-Loop
HPF	High Pass Filter
LPF	Low Pass Filter
HCC	Hysteresis Current Control

HB	Hysteresis Band
SPWM	Sinusoidal Pulse Width Modulation
RTDS	Real-Time Digital Simulation
PHIL	Power Hardware-in-the-Loop
ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
DUT	Device-Under-Test
PI	Proportional-Integral
VCO	Voltage Controlled Oscillator
CCS	Code Composer Studio
CMPSS	Analog Comparator Subsystem
EPWM	Enhanced Pulse Width Modulator
PFC	Power Factor Correction
FFT	Fast Fourier Transform
GM	Gain Margin
PM	Phase Margin

Dedication

To my parents and my wife …

Chapter 1: Introduction

1.1 Power Quality

With the fast development of power electronics technology, power-electronic-based power apparatuses and other non-linear loads are widely employed in modern electrical systems [1]. Since their non-linearity characteristics, power quality (PQ) issues are usually generated to the power system by injecting high volume of reactive power, harmonics and unbalanced currents into the electric grid. The reactive power, harmonics and unbalanced currents will cause low system efficiency and poor power factor [2]. Moreover, poor grid PQ can lead to some further negative effects, including power failure, malfunctions of equipment, overheating of machines, electronic communication interference and increased system losses [3].

Harmonics and their sources can be summarised into two categorizes [1, 4, 6-7]:

- Identified harmonic sources: High-Power (HP) diode or thyristor rectifiers, cycloconverters, and arc furnaces. The High Frequency (HF) harmonics can cause electromagnetic interference (EMI) for the communication networks and malfunctions of microprocessors.
- Unidentified harmonic sources: TV sets, personal computer, lighting, and adjustable speed heat pumps.

The identified harmonic sources are HP non-linear power equipment that installed on distribution systems and producing a significant amount of harmonic current. The unidentified harmonic sources are normally coming from Low-Power (LP) consumers. Individually, the LP

non-linear load produces negligible amounts of harmonics. However, as the use of LP non-linear loads increases, multiple of LP non-linear load can create a large amount of harmonic currents that flow into the power distribution system.

Fig. 1.1 illustrates the distortion problem caused by a three-phase non-linear loads. The non-linear load draws harmonic currents and distorts voltage at the point of common coupling (PCC).

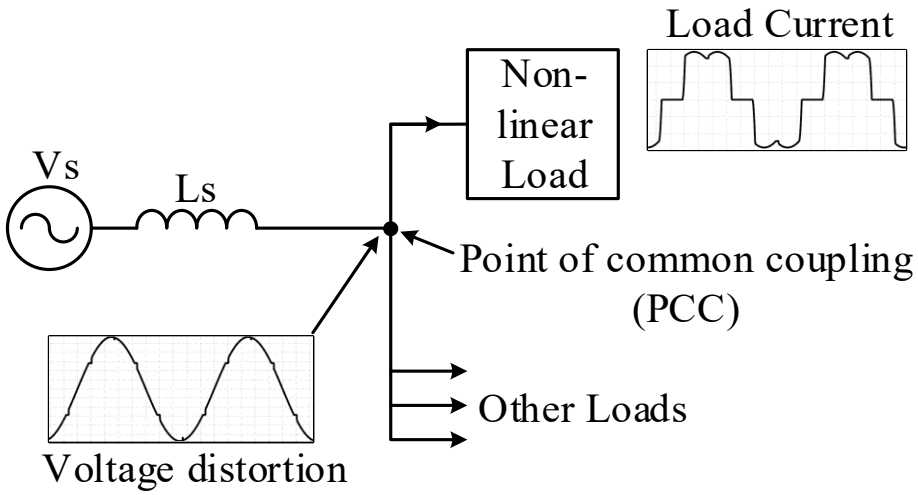

Figure 1.1: Harmonic distortion at PCC.

1.2 Harmonic Standards

In order to provide guidelines for dealing with current and voltage harmonics generated by power-electronic-based equipment and other non-linear loads, IEEE Std 519 was introduced in 1981 [8]. The Std 519 established voltage and current distortion limits at PCC for individual order of harmonics and Total Harmonic Distortion (THD) on various voltage ranges. Table 1.1 gives an example of current distortion limits for a general distribution system rated 120 V through 69 kV [9]. If any of disturbance exists above the prescribed levels, it is considered as a power quality

problem. The standard provides a detailed guideline for designing a grid-commuted power apparatus or a harmonic compensator.

Table 1.1: Current distortion limits for systems rated 120 V through 69 kV.

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)						
I_{SC}/I_L	3<h<11	11≤h<17	17≤h<23	23≤h<35	35≤h≤50	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Note: I_{SC}: the maximum short-circuit current at PCC.
I_L: the maximum fundamental frequency load current at PCC.
TDD: Total demand distortion, harmonic current distortion in % of maximum demand load current.
*All power generation equipment is limited to these values of current distortion, regardless of actual I_{SC}/I_L.

Table 1.2: Voltage distortion limits.

Bus voltage V at PCC	**Individual harmonic (%)**	**Total harmonic distortion THD**
V≤1.0kV	5.0	8.0
1kV<V≤69kV	3.0	5.0
69kV<V≤161k	1.5	2.5
161kV≤V	1.0	1.5

1.3 Harmonic Compensation Techniques

1.3.1 Passive Filters

Conventionally passive harmonic filters are used to connected in parallel with non-linear loads. It has been widely installed in distribution systems because of its robustness, reliability, low cost, and control-less characteristics [11]. The passive filter consists L-C components that are tuned to eliminate certain order of harmonics and provide reactive power [4]. However, passive filters have the drawbacks of large size, fixed compensation, instability and resonance with load and impedances of the utility [5]. Power distribution system frequency variation and components tolerances may affect the performance of passive filter [10].

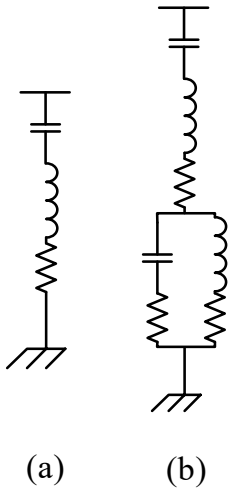

Figure 1.2: Passive tuned filters, (a) Single tuned, and (b) Double tuned.

Figure 1.2 and 1.3 show various configurations of passive tuned filters and high-pass filters on a per-phase base. They are shunt connected with non-linear loads. For instant, four single tuned filters can be designed to eliminate 5^{th}, 7^{th}, 11^{th} and 13^{th} order of harmonics and a second order

high pass filter can be tuned around the 17th harmonic frequency to deal with the harmonics for a thyristor-based rectifier [4].

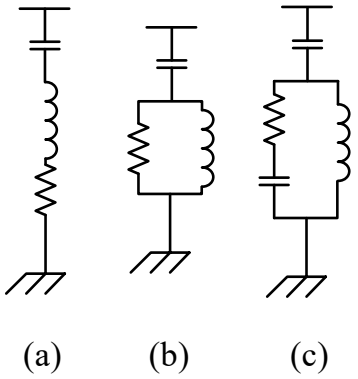

Figure 1.3: Passive high-pass filters, (a) First order, (b) Second order, (c) Third order.

1.3.2 Active Power Filters

APF has been recognized as the most effective and mature method to solve poor PQ problems [2]. Research related to APF began in the 1970s and has been focusing on diverse configurations, control strategies and so on. The concept of active filtering is based on the principle of injecting the harmonic component of the load current into the ac power grid with the same amplitude but in opposite phase [6]. According to Prof. Akagi [4], APF has the ability of filtering harmonics, compensating reactive power for power factor correction, voltage regulation, current balancing and regulating voltage-flicker, depending on the type of control methodology.

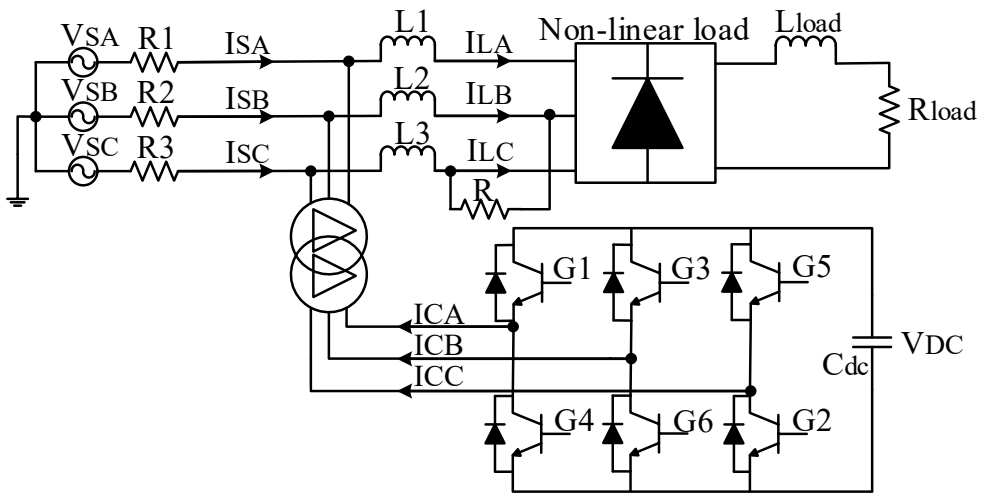

Figure 1.4: Example of a shunt-connected active power filter.

An example of shunt-connected APF is shown in Fig. 1.4, a voltage-source converter equipped with a DC capacitor. Six insulated-gate bipolar transistor (IGBT) switches are connected in anti-parallel with free-wheeling diodes, which provides bi-directional power flow.

1.4 Problem Statement

APF is widely employed in mitigating harmonics in utility power lines because of the advantages, and many researches related to APF has been done to investigate its new topology and control methodology [3, 10, 14, 16-38]. In the process of design and testing a control system or a new topology, it is very common to use an off-line simulation tool (e.g. PSCAD/EMTDC). This is because high voltage (HV) and high power (HP) systems are difficult, expensive, and dangerous to be prototyped. Also, an off-line simulation software gives the user a simple access to modify the system parameters, which can shorten the design duration in the early stage of implementation.

However, it is apparent that there is a technical gap between controllers in simulations and practical due to a lot of assumptions and ideal components in the controller design. For example,

most commercial off-line simulators need an Automatic Code Generator to transit the controller model to an implementation. In real-time simulation, there is no need to use the Automatic Code Generator, which takes less effort [12]. Besides, a real-time simulator is ideal for Rapid Control Prototyping (RCP) where a controller model is implemented inside the real-time simulator, and then the controller can be tested with a physical plant. The real-time simulator makes it very convenient to modify controller parameters and speed up the RCP process. Figure 1.5 shows an example connection for the RCP testing using a real-time simulator.

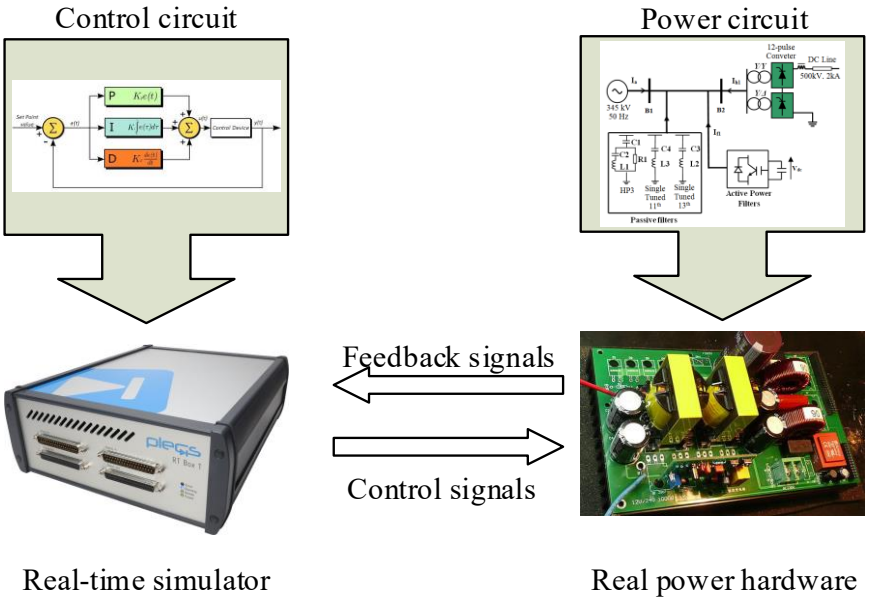

Figure 1.5: Rapid control prototyping (RCP) block diagram.

On the other hand, the real-time simulator is essential for hardware-in-the-loop (HIL) testing as well. For HIL applications, a physical controller is connected to a power circuit that executed in the real-time simulator. The HIL allows user to test controllers before connecting to real power hardware. A layout of a controller HIL simulation is illustrated in Fig. 1.6, the control system is implemented in a DSP where receive and process feedback signals from the real-time simulator and send the control signal back to the simulator.

Thus, controller hardware-in-the-loop (CHIL) is an ideal platform to evaluate a control system. In the platform, the real-time digital simulator has been designed to run power circuits with real-time response. Since the simulator has extremely low input/output (I/O) latency, the controller runs like controlling a real power circuit. In conclusion, CHIL simulation provides easy, cost-effective and safe platforms to evaluate controllers, especially in the early stage of power electronics system design.

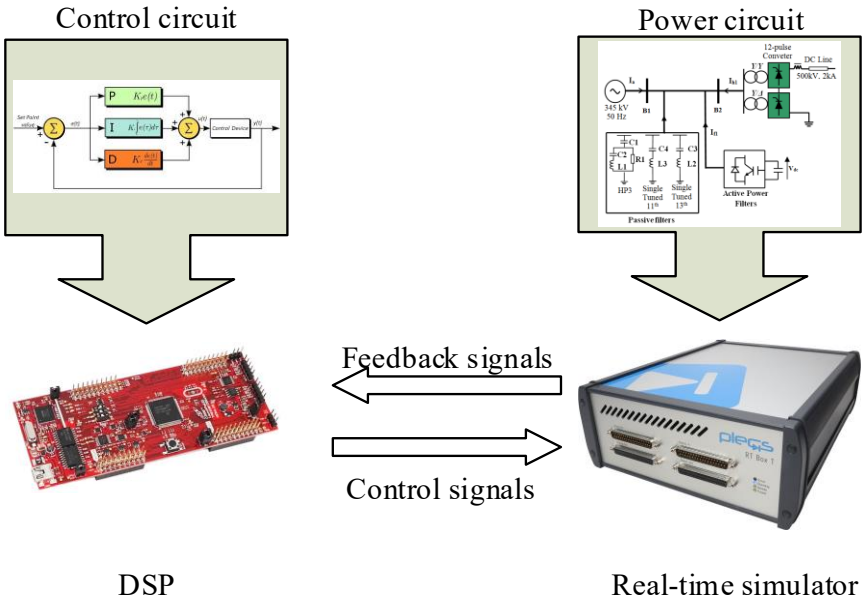

Figure 1.6: Controller Hardware-in-the-Loop simulator block diagram.

Conventional real-time simulators in power system simulations, such as RTDS, are limited by the switching frequency (e.g. 4kHz) and high-cost [12]. However, thank the technology development of power semiconductors, switching frequency of HV and HP power electronic apparatuses increases in order to increase power density by reducing the size of passive devices. Therefore, it is essential to use a cost-effective way to practically verify control algorithms in real-time running environment for HV, HP, and high switching frequency (e.g. 10 kHz and higher) applications.

This thesis uses the latest developed real-time simulator “RT-Box”, which is designed for power electronics applications. A low-cost commercial DSP-based controller for a three-phase APF is implemented. The power circuit is executed in the RT-Box. The developed controller is tested in a CHIL simulation platform, where the controller receives analog signals from the RT-Box simulator and processes them to generate gating signals, then signals are sent back to the simulator for proper switching actions in the simulated power circuit. The RT-Box can capture digital signals with a resolution of less than 10 ns. The switching frequency of the APF is around 10 kHz. The results are observed for performance evaluation.

1.5 Motivation

The motivation for the thesis stems from the fact that there is a need to evaluate the performance of the new real-time simulation platform (RT-Box) in RCP and CHIL for HV and high switching frequency power electronics applications. This thesis conducted a real-time CHIL simulation for a three-phase APF using a real-time simulator (RT-Box) from Plexim and a DSP microcontroller from Texas Instruments. In addition, to study the behavior of the control loop, CHIL is an effective platform in university laboratory conditions to minimize the risk, cost, and duration. Since the control of an APF requires high switching frequency to eliminate current harmonics, which make it a good application to evaluate the performance of the RT-Box as well. It is necessary to determine the minimum step size of the simulator through this project. The complete controller was tested without the real power stage.

1.6 Outline of the Thesis

The structure of the thesis is described as follow:

- Chapter 2 presents a literature review on APF, including circuit configurations, reference current calculation algorithms, gating signal generation methods, and a summary of researches done on the HIL simulation regarding to the APFs.
- Chapter 3 covers control system implementation and analysis. The controller has four major components: A phase-locked loop, a synchronous reference frame-based reference filter current calculation, a hysteresis band current control to generate gating signals, and a proportional-integral controller for DC-link capacitor voltage control.
- Chapter 4 validates the theoretical concepts by off-line and real-time simulation. Performance of the APF is evaluated under a non-linear load and unbalanced load combined situation.
- Chapter 5 concludes the thesis and identifies some future research work to optimize the project.

Chapter 2: Literature Review

In this chapter, a literature review on the three-phase APF is presented. This review will firstly present a summary on classification of the APFs through reading literatures that contributed in the last three decades based on their converter type and topology. Then the next section reviews different control strategies of the APF. The control strategy of APF normally can be split into two stages: compensating signal derivation and gating signal generation. Finally, a review on HIL simulation related in APF application will be presented.

2.1 Classification of APF

2.1.1 Converter-based Classification

An APF can be classified based on its converter type. Two types of converters are generally used in APF applications, current-sourced and voltage-sourced. User can choose the filter configuration in consideration of cost and size of energy storage element or complexity and reliability of a power system [13].

Fig. 2.1 shows a current-sourced pulse width modulation (PWM) inverter-based APF. There is a DC reactor that supplies a constant DC current in the current-sourced-type APF. The APF continuously injects current to compensate harmonic currents generated from the non-linear load. Six IGBTs in series with a diode to block the reverse voltage. This type of APF is considered highly reliable due to the absence of electrolytic capacitor, but limits to its higher loss and smaller filter capacity [14].

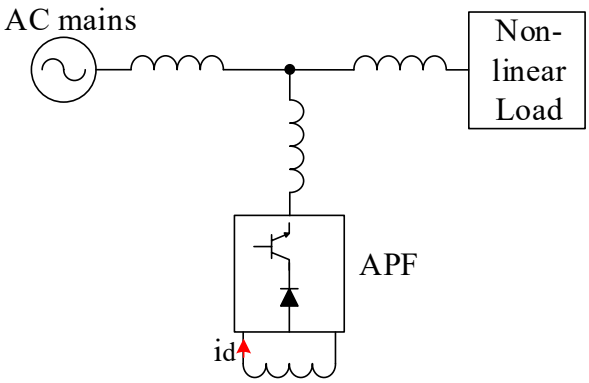

Figure 2.1: Current-sourced inverter-based APF.

Another converter type of APF is shown in Fig. 2.2, which is based on voltage-sourced inverter. The energy storage element is a capacitor. This type of configuration is more popular in APF applications because of it is less expensive, able to construct multilevel converter [2]. Moreover, according to [15], a voltage-sourced inverter has a faster speed of response of 0.1 ms compare to the response time of a current-sourced inverter which is around 1 ms.

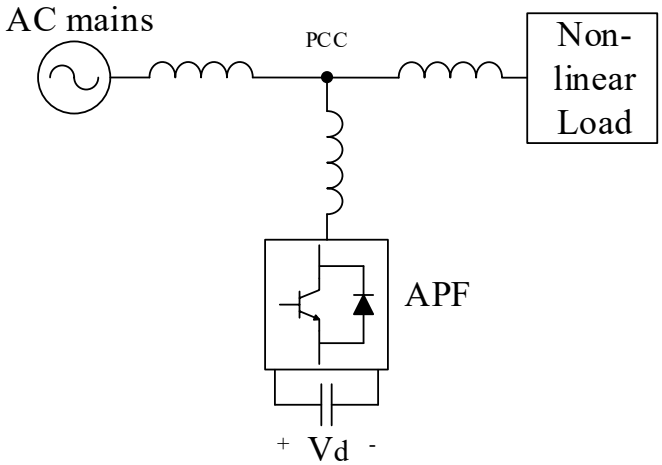

Figure 2.2: Voltage-sourced inverter-based APF.

2.1.2 Topology-based Classification

The APF can also be classified into three major types: shunt, series and hybrid. Shunt APF is the most widely used for harmonic elimination. Many researches [16-27] have conducted to introduce the design and implementation of a shunt APF. An example of shunt APF is illustrated in Fig. 2.2. The shunt APF is connected in parallel with the load, at the load end, as a current-source to inject compensation current to eliminate the harmonic current and reactive components of non-linear load at the PCC. A shunt APF is suitable to deal with the current harmonics produced by a diode or thyristor rectifier with inductive loads. Shunt connection allows one to connect multiple APFs together for high power rating harmonic compensations [37].

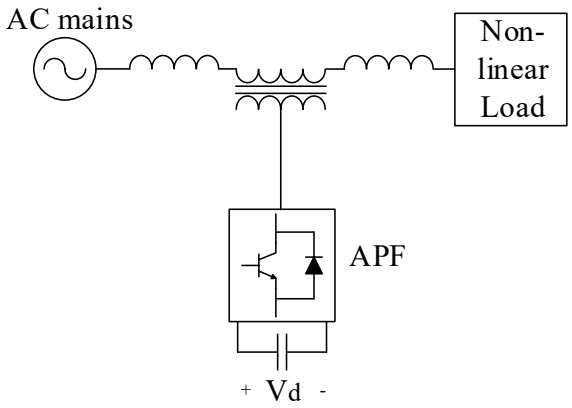

Figure 2.3: An example of series-connected APF.

Fig. 2.3 shows a series APF, which is connected in series with the load and the utility through a matching transformer. Series APF applications are described in literatures [28-35]. Unlike shunt APF, a series-connected APF acts as a voltage source and is used for AC voltage regulation and suitable for large capacity diode rectifiers with capacitive loads [1]. The series APF applies a compensating voltage to the primary side of the transformer, and the voltage is added to the load

voltage, which results a sinusoidal voltage at the PCC [4]. Therefore, the series APF is designed to deal with voltage type harmonic-producing load.

As a combination of the APF and passive filter, Fig. 2.4 gives an idea of the structure of a hybrid APF. Scholars introduce design and implementation of series hybrid APF in these papers [36-41]. The series hybrid APF is capable of compensating current as well as voltage harmonics [36]. The combination can improve filter performance and provide a cost-effective topology in harmonic compensation.

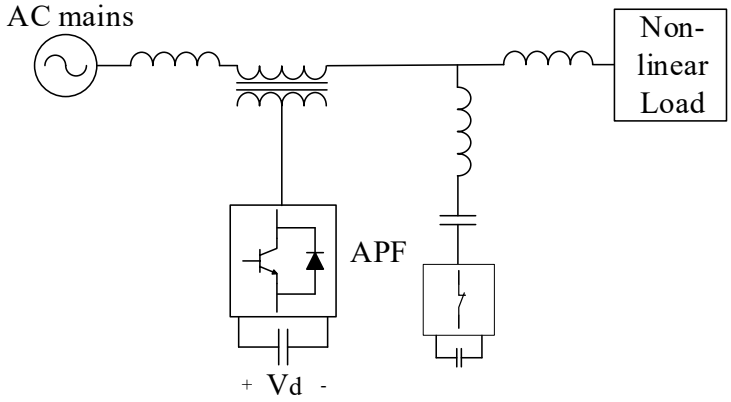

Figure 2.4: An example of series-hybrid APF.

2.2 Control Strategy for APF

The control strategy plays an important role in APF. Generally, the control of an APF includes a compensating signal derivation process which detects harmonic component produced by the non-linear load, and then followed by an inner control loop where gating signal are generated. At the compensating signal derivation stage, either current or voltage reference signals are derived based on control method and topology. Gating signals for the solid-state devices of the APF are

generated at the gating signal generation stage. In following sections, variety of control strategies are reviewed and summarized.

2.2.1 Compensating Signal Derivation Schemes

At the compensating signal derivation stage, the controller has the responsibility of detecting the harmonic current or voltage component that needs to be compensated by the APF. The detected harmonic component is then considered as the reference signals to the inner controller. The compensating signal detection techniques can be concluded into two categories: frequency-domain-based and time-domain-based. Table 2.1 summarises common-used harmonic detection methods for the APF applications [42, 44, 47-52, 56-61].

Table 2.1: Classification of harmonic detection method for APF.

Domain	Harmonic Detect Method
Frequency Domain	• Discrete Fourier Transform [42]. • Fast Fourier Transform [44]. • Recursive Discrete Fourier Transform [47-52].
Time Domain	• Instantaneous Power (p-q) Theory [56]. • Synchronous Reference Frame (d-q) Theory [57, 58]. • Synchronous Detection Method [59,60]. • Direct Detection Method [61].

2.2.1.1 Frequency Domain-based Harmonic Detection Methods

The frequency domain-based harmonic detection method is to use Fourier analysis to extract the harmonic component from the distorted voltage and current signals. A basic frequency domain-based method is called Discrete Fourier Transform (DFT). The DFT is a transformation that uses the sampled voltage or current signal as input to calculate the amplitude and phase of the harmonic component [42]. The phase and amplitude information of the harmonic component can be derived by Eqn. 2.1. The equations mathematically transform discrete signals to frequency domain. Once harmonic component is detected, it will be transformed back to time domain as the reference signal for inner control loop. The DFT method has the advantages of simplicity, excellent selectivity and steady state accuracy. However, this method suffers from slow operation time and sensitivity to frequency changes [43].

$$\bar{X}_b = \sum_{n=0}^{N-1} x(n) \cdot \cos\left(\frac{2\pi \cdot b \cdot n}{N}\right) - j \cdot \sum_{n=0}^{N-1} x(n) \cdot \sin(\frac{2\pi \cdot b \cdot n}{N})$$

$$\bar{X}_b = X_{b(real)} + j \cdot X_{b(imag)}$$

$$|\bar{X}_b| = \sqrt{X_{b(real)}^2 + X_{b(imag)}^2}$$

$$\varphi_b = \arctan(\frac{X_{b(imag)}}{X_{b(real)}}) \tag{2.1}$$

Another enhanced frequency domain-based harmonic detect method is Fast Fourier Transform (FFT). The FFT uses a different form from DFT to reduce computational operations therefore increase reaction time [44]. The working concept of FFT is that it converts the voltage or current signal into frequency domain. Then each individual frequency component is compared

with the reference signal. The error signal is calculated as the compensating reference signal. According to literature [45], the FFT method has faster reaction time because it uses a 2-point transforms of N/2 instead of using N point transform, where N is the sample number. This leads a reduce in the time of computation from N^2 to $N \cdot log_2(N)$. Three major drawbacks of FFT method are picket-fence effect, aliasing, and leakage [46].

As an improvement based on DFT method, the Recursive Discrete Fourier Transform (RDFT) is introduced by authors in [47-52]. The RDFT method has the same principle as the DFT method but the calculation is based on a sample-by-sample basis with a fixed shifting window. The window usually shifts in every sampling cycle by one sample. The new result can be calculated from the previous result by adding the latest sample and subtracting the first sample. Thus, the RDFT saves a plenty of sampling and calculation time.

The methods described above are the most common frequency domain-based harmonic detect method that are found in literature review. Modified methods are presented in literatures [43, 53-54] to further improve their performance over the conventional methods. Some drawbacks of Fourier analysis-based harmonic detect methods can be conclude as: necessary to pay attention to synchronize the fundamental frequency with the sampling frequency, need large memory storage space, require high performance digital controller, poor transient response due to delay in calculation [45,55].

2.2.1.2 Time Domain-based Harmonic Detection Methods

The time domain-based harmonic detection method is another way to extract harmonic components from the voltage or current signals. The control method of APF in time domain is

built on instantaneous calculation of compensating signals from the polluted voltage or current signals.

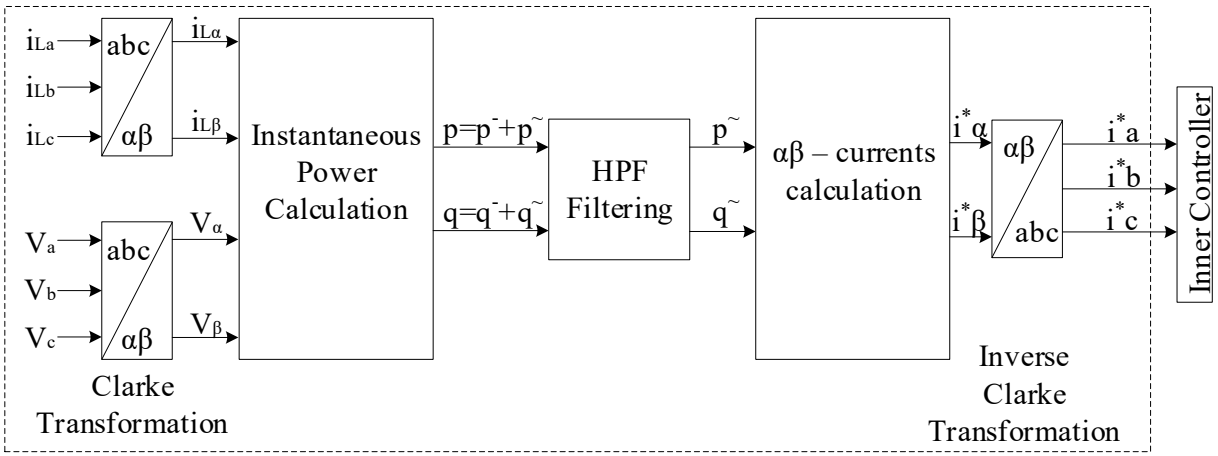

Figure 2.5: Block diagram of instantaneous (p-q) theory.

One common time-domain technique is instantaneous power theory or p-q theory. The instantaneous power theory extracts the harmonic distortion by calculating the instantaneous power for the three-phase power system (shown in Figure 2.5). The theory and its applications are written by professor H. Akagi and other authors in the book [56]. The method uses Clarke transformation to convert a three-phase signal from a-b-c coordinates to α-β coordinates. As shown in Figure 2.5, load current and source voltage signals are transformed into α-β coordinates, which followed by the instantaneous power calculation. Then instantaneous power p and q (real and reactive power) can be calculated from instantaneous values of currents and voltages using Eqn. 2.2. Then, the real power p is separated to its average (p^{-}) and oscillating ($p^{\sim}$) parts. Likely, the reactive power q is separated into (q^{-}) and ($q^{\sim}$). This step is done by a high pass filter. After obtaining the oscillating real and reactive power. The compensating current signal can then be calculated in Eqn. 2.3. Finally, an inverse Clarke transformation is applied to calculate the compensating currents in a-b-c coordinates, which will be used in the inner control loop.

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \tag{2.2}$$

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = -\frac{1}{V_\alpha^2 + V_\beta^2} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \cdot \begin{bmatrix} \tilde{p} \\ \tilde{q} \end{bmatrix}. \tag{2.3}$$

Another popular time-domain method is Synchronous Reference Frame (SRF) theory or also called as d-q theory, which is shown in Fig. 2.6. It is based on Park's Transformation (Eqn. 2.4), where three-phase load current signals are transformed from a-b-c coordinates (stationary reference frame) into d-q coordinates (rotating reference frame).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \cdot \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{2.4}$$

where θ is the transformation angle determined by Phase-Locked-Loop (PLL).

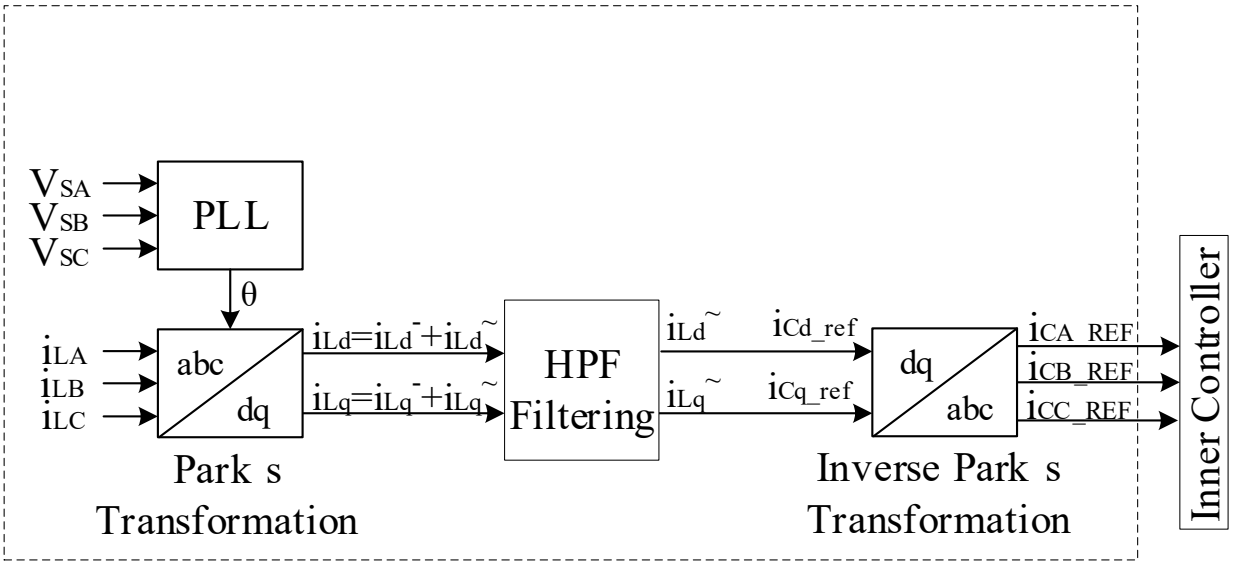

Figure 2.6: Block diagram of the synchronous reference frame theory or (d-q) theory.

The obtained current signals i_{Ld} and i_{Lq} in d-q coordinates consist of a fundamental dc component ($\bar{i_{Ld}}$ and $\bar{i_{Lq}}$) and harmonic ac component ($\tilde{i_{Ld}}$ and $\tilde{i_{Lq}}$). The extraction of harmonic components from i_{Ld} and i_{Lq} is done through a High Pass Filter (HPF). Since the injection current from the APF is equal to the ac harmonic component of the load current, the HPF outputs $\tilde{i_{Ld}}$and $\tilde{i_{Lq}}$are treated as the APF's filter current references. Finally, an inverse Park's Transformation is applied to the converter filter current references to transform them from d-q coordinates to a-b-c coordinates, which are then sent to the inner control loop for current controlling.

One thing can be noticed is that this method requires a PLL to calculate the transformation angle or reference angle from three-phase source voltage signals. The design of PLL needs extra care when dealing with non-ideal cases, such as line voltage unbalances and non-sinusoidal waveforms [57]. The paper [58] proposed a modified SRF method that does not require PLL in compensating signal calculation.

Synchronous detection method is also capable of harmonic signal detection for APF applications. This harmonic detection technique is introduced in papers [59, 60], and is suited to work under unbalanced voltage supply and unbalanced load situation. The synchronous detection method is proposed based on three assumptions: (a) each phase carries equal magnitude of current, (b) each phase shares equal real power, and (c) that each phase has equal load resistance. Under these assumptions, the total average power is obtained from source line currents and phase voltages. Then, the total average power is used to calculate reference active source currents. Finally, the compensating current can be extracted by subtracting the reference active source current from the actual load current. Fig. 2.7 shows the example of synchronous detection method for phase A, P_{av3} is the total average power which is the summation of the three-phase power. V_{am} is the peak value

of phase voltage $v_{an}(t)$. V_T is the summation of V_{am}, V_{bm} and V_{cm}. $I_{acc}(t)$ is the reference active source current, and $I_{an}(t)$ is the load current of phase A. Finally, the reference compensating current $I^*_{can}(t)$ is calculated and sent to current control loop to generate switching signals.

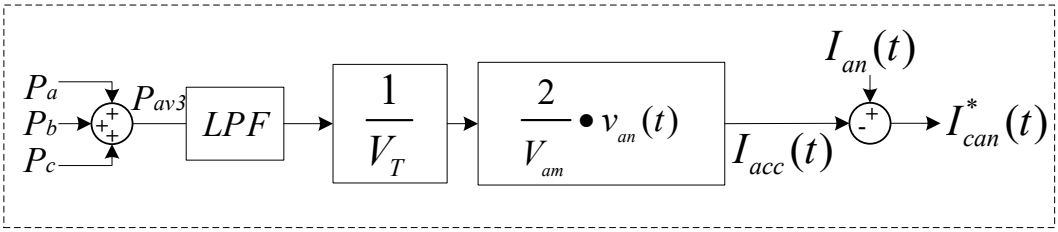

Figure 2.7: Block diagram of synchronous detection method.

The direct detection method is designed to separate the harmonic component from the load current. However, it is different than above techniques, because it does not require transformation of signals into any reference frame. This method uses the a-b-c phase source voltage, load current and voltage error of the APF's DC-link capacitor to calculate the reference compensating signal directly.

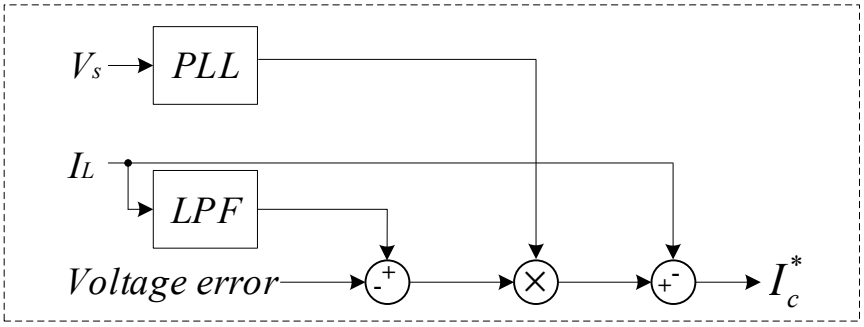

Figure 2.8: Block diagram of the direct detection method.

Fig. 2.8 shows an example block diagram of the direct detection method. In this example, the load current is assumed to be distorted with harmonics. It passes through a low pass filter (LPF) to extract its fundamental component. On the other hand, a PLL calculates the phase angle of the

source voltage. The load current signal is multiplied with the phase angle to achieve the goal of reactive power compensating. Then the signal subtracts the actual load current to get the reference compensating current signal. The DC capacitor voltage error of the APF is added to the current signal to have proper control over the capacitor voltage. This kind of direct harmonic detection method is not widely used. A disadvantage is that it causes low frequency oscillation problem on the APF's DC bus voltage [61].

2.2.2 Generation of Gating Signal

2.2.2.1 Hysteresis Current Control

The Hysteresis Current Control (HCC) technique is employed to control the active filter currents. It is recognized as the most popular switching technique in the APF applications [62]. Advantages of the HCC are easy implementation and fast dynamic response [63]. Many papers [63-69] used the HCC as switching control technique. This technique uses the filter reference current that is calculated from harmonic current extraction stage and the Hysteresis Band (HB) is set by the user. The hysteresis upper band equals to $I_c^* + HB$ and the hysteresis lower band is $I_c^* - HB$. The HCC continuously compares the actual filter current I_c with the upper and lower bands to make switching decisions that whether turn on or off the power electronic switches. Fig. 2.9 illustrates the control law of the HCC. When the actual filter current I_c reaches the lower band, the switch S_1 will be turned on. Oppositely, the switch S_1 will be turned off when I_c reaches the upper band. The state of the switch will remain unchanged if I_c is anywhere in between the upper and lower band. The HCC is demonstrated to be a robust control technique that has advantages of dynamic response, good stability and easy implementation [61]. On the other hand, the HCC also has a drawback, that is it produces a variable switching frequency for the APF. One fixed-

switching frequency HCC approach has been proposed in paper [70] by changing the width of the hysteresis band.

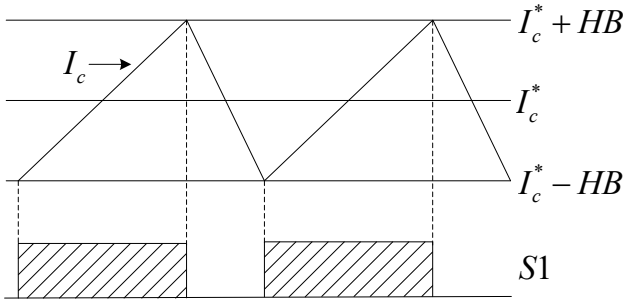

Figure 2.9: Block diagram of the hysteresis current control.

2.2.2.2 Sinusoidal Pulse Width Modulation

The sinusoidal pulse width modulation (SPWM) technique is a carrier-based PWM switching technique has been introduced in papers [71-73]. This technique is based on a comparison on the actual filter current and the reference filter current. The difference between the two currents is the error signal ($e = I_C^* - I_C$) that is amplified and compared with a triangular carrier wave. When the e is higher than the triangular carrier wave, the comparator will generator pulses to turn on the lower inverter switches and turn off the upper inverter switches. On the other hand, when the e is lower than the triangular carrier wave, the comparator will turn on the upper inverter switches and turn off the lower switches to increase the filter currents.

2.3 A Review on Real-Time Simulation for the APF Application

Real-time digital simulation (RTDS) is commonly used in electric power system applications, which can be designed to represent the behavior of the real power system. In RTDS, a real-time digital simulator is defined as a simulator that can solve the model equations in a time (execution

time: T_e) that is shorter or equal to the selected time-step [74]. The simulator solver works at discrete time intervals, the time interval can be set by user in the simulator setting as a fixed time-step, and different kind of real-time simulators have their own limits of time-step. If T_e of one simulator is greater than one time-step, the simulator is considered running in off-line.

HV and HP systems are changeling, expensive, and dangerous to be prototyped to evaluate controller hardware or power hardware performance under laboratory conditions. Off-line computer simulators (e.g. PSCAD) are generally used in most cases, but it is apparent that there is a technical gap between simulations and practical for controller and power hardware due to a lot of assumptions have been made and ideal components are used in the simulator. Thus, a real-time simulator is an ideal selection for both rapid controller prototyping and power hardware-in-the-loop (PHIL) simulation. The real-time digital simulator has been designed to run power circuits with real-time response. An real-time hardware-in-the-loop simulation helps reduce risk caused by HV and HP, minimize development efforts, and speed up controller prototyping. Additionally, the real-time simulator has extremely low I/O latency, so the simulator runs like a real power circuit. Thus, it provides convenient, cost-effective, and a safe platform to evaluate controller and power circuit performance, especially in the early stage of power system design.

The RTDS for power system applications can be classified into two categories: 1) A pure digital real-time simulation, and 2) HIL real-time simulation [74]. A pure digital real-time simulation requires all components in the system to be modelled in the simulator without external interfacing. However, a HIL real-time simulation involves actual physical hardware to be interfaced with the simulator through analog-to-digital converter (ADC) or digital-to-analog converter (DAC). The physical hardware is normally called the device-under-test (DUT), which can be a controller or a power hardware. If the DUT is a controller hardware, this kind of HIL

simulation is called CHIL simulation, and it is used for RCP. There is no real power transfer between the real-time simulator and the controller hardware. The power circuit is modelled in the simulator and communicate with the controller through ADC or DAC. The real-time simulator acts as the power circuit and sends signals to the controller, the controller processes the signals and sends controller command back to the simulator. One can test and modify the controller using CHIL without connecting the controller to the real power circuit but with high accuracy. On the other hand, if the HIL simulation requires real power transfer and the DUT is a real power apparatus, the HIL is considered a PHIL simulation. There is real power transfer between devices through power amplifier. The simulator sends signals to the power amplifier that produces voltages or currents to the DUT, and sensors take measurements from the DUT and send feedback signals to the simulator. Fig. 2.10 illustrates the concept of CHIL and PHIL.

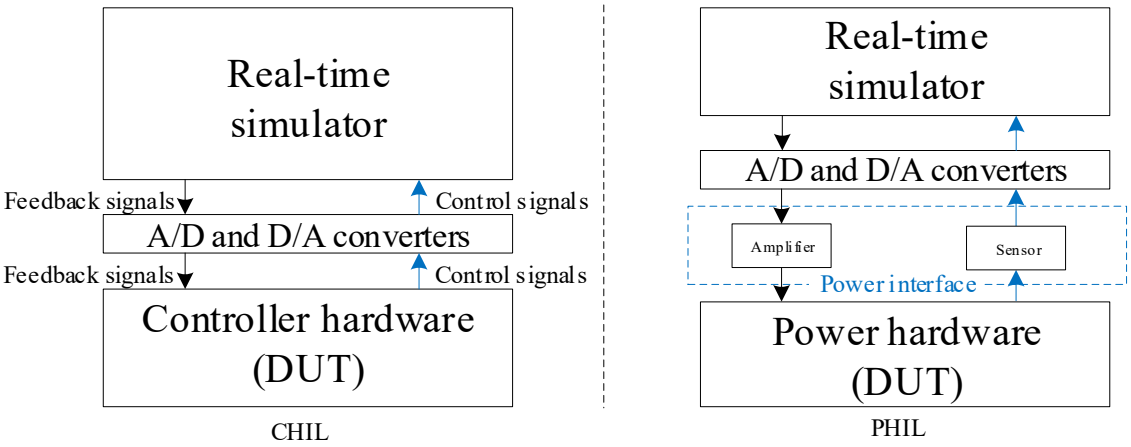

Figure 2.10: HIL simulation arrangement for CHIL and PHIL.

A real-time simulator must be able to solve a grid-scale model in approximately at least 50 μs time-step to successfully replicate transients for 50/60 Hz power systems [74]. The first commercial real-time digital (RTDS) simulator was took place by RTDS Technologies Inc. in 1993. It has been used in wide range of power system application, such as microgrid, distribution

automation, PHIL, CHIL, HVDC and FACTS, smart grid and distribution generation, and power electronics over the last two decades [75]. Later, ARENE was introduced as a fully digital real-time power system simulator developed by Electricity of France in 1996, which is capable to simulate high frequency applications using parallel computer [76]. Another PC-based real-time simulator was developed by Siemens and the Technical University of Berlin, its name NETOMAC stands for Network Torsion Machine Control [77]. The NETOMAC has the capability of HIL testing for protective relays. Since 1997, OPAL-RT Technologies Inc. was established and developed a real-time simulator called OPAL-RT, which has been demonstrated the excellent ability of running real-time simulation and HIL testing for electrical, electro-mechanical and power electronics systems [78-80]. Conventional power system real-time simulators such as RTDS and OPAL-RT, are limited by the switching frequency and high-cost. However, thank the technology development of power semiconductors, switching frequency of HV and HP power electronic apparatuses increases in order to increase power density by reducing the size of passive devices [4]. So, it is essential to find a cost-effective way to practically perform real-time HIL simulation for HV, HP, and high switching frequency applications. Therefore, a recently developed real-time simulator, RT-Box, for power electronics is released by Plexim Inc. The RT-Box has 32 analog channels and 64 digital I/O channels along with its powerful 1 GHz dual-core CPU, which makes it becomes an ideal simulator for both real-time CHIL and PHIL testing [81].

Researches that are related to the topic of HIL simulation for APF applications have been discussed in many papers [82-86]. RTDS and OPAL-RT are still the most common platforms for APF real-time HIL simulation. In some papers, the power source, the non-linear load, and the APF are modelled inside the simulator, and controller are developed in the DSP. The interface between the simulator and the controller is achieved through ADC and DAC converters. This type of

configuration is CHIL simulation. Otherwise, the power circuit can be built physically, and controller can be developed inside the simulator to construct a PHIL simulation.

Chapter 3: Controller Implementation and Analysis

3.1 Introduction

A shunt APF consists of two components: a voltage-fed converter for power processing and a controller for signal compensating. The converter is controlled to synthesize compensating current signals to cancel the harmonic component in the load current. The controller is responsible for signal processing in real-time to generate gating signals to the converter. The APF controller continuously senses the source voltage, the load current, the filter current, and the APF DC-link capacitor voltage to calculate the filter reference current. Then the controller compares the filter reference current with the actual filter current using selected current control technique to generate PWM signals for proper switching of the converter.

In this chapter, the topic will focus on the "brain" of the APF, control system. The layout of the control system for the APF is given in Fig. 3.1. The control of the APF includes two parts: the reference current extraction part and the current control part. The reference current extraction is used to calculate the reference filter current in direct-quadrature (d-q) coordinates. A PLL is taken place to determine the phase angle θ, and load current I_L are transformed from a-b-c to d-q coordinates using Park's Transformation. Afterwards, the APF extracts the harmonic components $i_{Ld}^{\sim}$ and $i_{Lq}^{\sim}$. The reference filter current is then transformed back to a-b-c coordinates and compared with the actual filter current using the hysteresis band current controller. Other than controlling the filter current, the filter DC-link capacitor voltage also need to be maintained at a certain level. This

is done through a Proportional-Integral (PI) controller. The output of the PI controller is combined with $i_{Ld}^{\sim}$ to close the control loop.

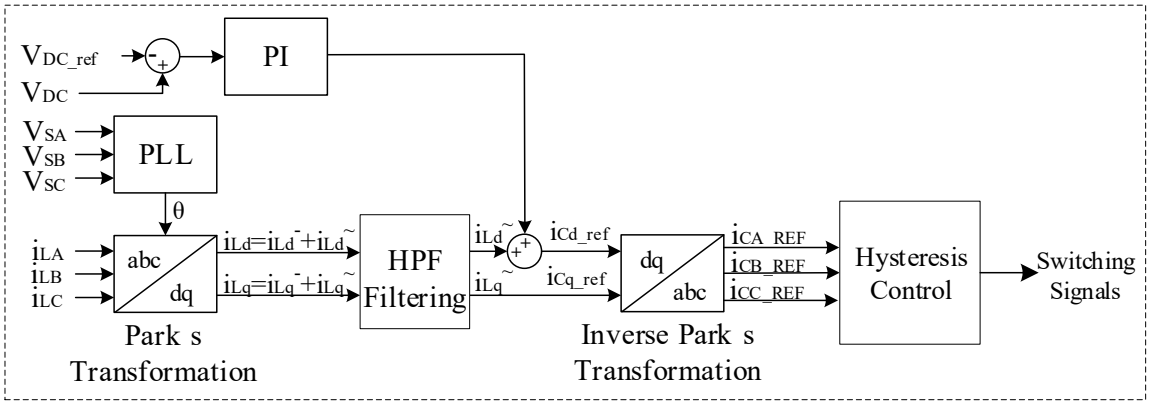

Figure 3.1: The control system layout for the APF.

The construction of this chapter will cover the design and implementation of the PLL, the reference filter current extraction technique, which is based on the SRF theory, the HCC and the DC-link capacitor voltage control.

3.2 Phase-Locked-Loop

It is necessary to keep a grid-connected converter currents synchronized with the power grid voltages [64], [87]. Thus, a PLL is developed to detect system frequency and phase angle of the three-phase voltage at PCC. Phase angle (θ) can be extracted in this step and used in next stage, which is direct-quadrature (*d-q*) transformation.

Fig. 3.2 shows the designed PLL block diagram. V_{SA}, V_{SB} and V_{SC} are three-phase AC voltage that input to PLL. The error signal is processed by a PI regulator with proportional gain $K_p$and integral gain K_i. Then the output of the PI controller is fed to voltage-controlled oscillator (VCO) to derive phase angle θ for the $sin\theta$ generator. The nominal frequency ω is controlled by a

reference frequency ω_{ref}. The output of VCO is limited in the range of 0 to 2π. This type PLL is described as *Transvektor* type or *d-q-0* type in [88], [89].

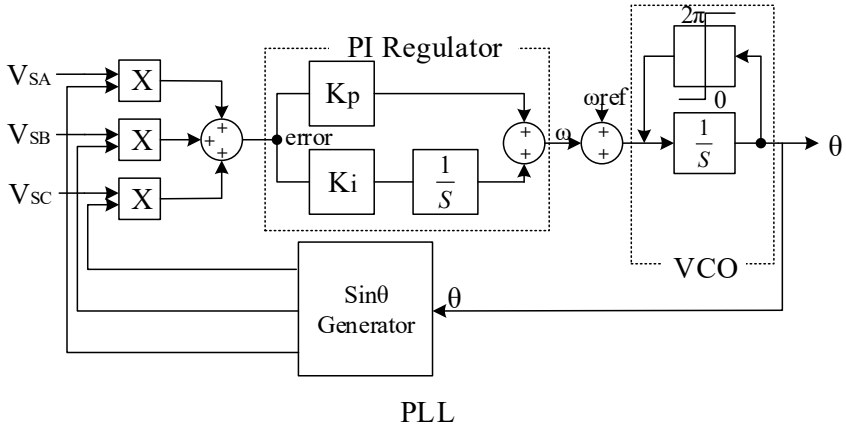

Figure 3.2: The block diagram of PLL.

The PLL is implemented in a DSP from Texas Instrument using the code composer studio (CCS) software. Firstly, the PLL is programed in the DSP alone, which makes easier to do test and modification. In the test, the real-time simulator RT Box is used to generate real-time three-phase signals to imitate the three-phase source voltage signals. The DSP reads the signals and processes them to calculate the phase angle θ. In order to compare the results are as expected, the waveforms of $cos\theta, \cos(\theta - 120°), \cos(\theta + 120°)$ are observed in oscilloscope.

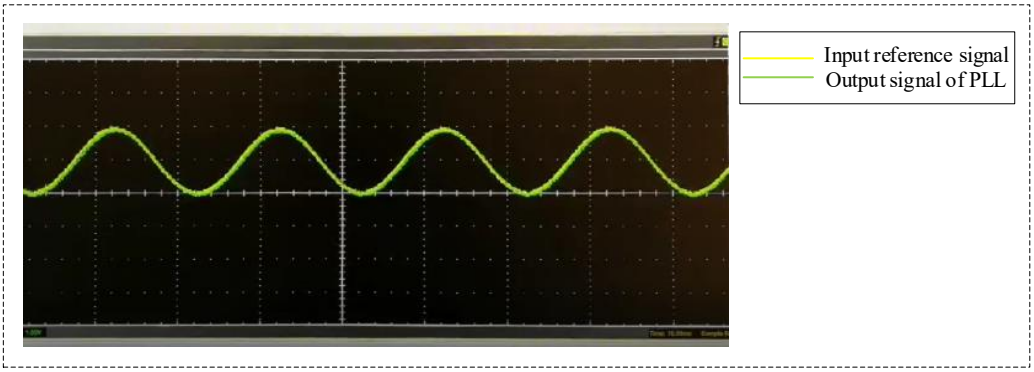

Figure 3.3: PLL test result.

The result of one phase is shown in Fig. 3.3, the green line is the output of the DSP and the yellow line is the input signal in per phase. the result can conclude that the PLL is functional and stable, it is able to lock on the reference signal waveform. Therefore, the PLL output, phase angle θ is accurate. The detailed code of implementation and specification of controller will provide in the appendix.

3.3 Synchronous Reference Frame Transformation

The technique used to generate reference current is based on SRF theory or *d-q-0* theory, which can be found in literatures [61, 85, 90-91]. SRF theory is built on Park's Transformation, where three-phase signals are transformed to synchronously rotating reference frame. The APF works in a three-phase three-wire system, so zero-sequence component can be neglected. The three-phase load currents i_{LA} , i_{LB} and i_{LC} are transformed to direct (or active) and quadrature (or reactive) components i_{Ld} and i_{Lq} using Park's Transformation.

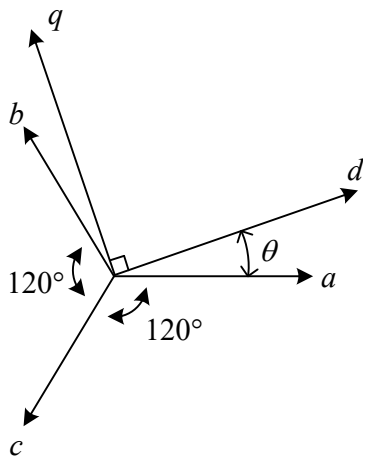

Figure 3.4: Vector representation of the three-phase electrical variable in stationary (a-b-c) and synchronous reference (d-q) frame.

Fig. 3.4 shows the vector representation of the three-phase electrical variables in the stationary and synchronous reference frames. The transformation can be done using Eqn. 3.1.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{LA} \\ i_{LB} \\ i_{LC} \end{bmatrix} \quad (3.1)$$

where, i_{Ld} and i_{Lq} are the load current component of space vector along d-axes and q-axes respectively. Phase angle θ is from the output of the PLL. i_{LA}, i_{LB} and i_{LC} are the load current in a-b-c coordinates.

To verify the results, the code of d-q transformation is programmed in the DSP and added to the PLL code. The three-phase sinusoidal signals are coming from the RT Box. The PLL calculates the phase angle θ, and then passes to the d-q transformation block. The output i_{Ld} and i_{Lq} are observed on oscilloscope software and compared with the waveforms in an off-line simulator. In Figure. 3.5, it shows the resulting waveform from oscilloscope, the yellow waveform is the sinusoidal signal of phase A current, and the green waveform is the d-axes component i_{Ld}. Similarly, in Figure. 3.6, the yellow waveform is the sinusoidal signal of phase A current, and the green waveform is the q-axes component i_{Lq}.

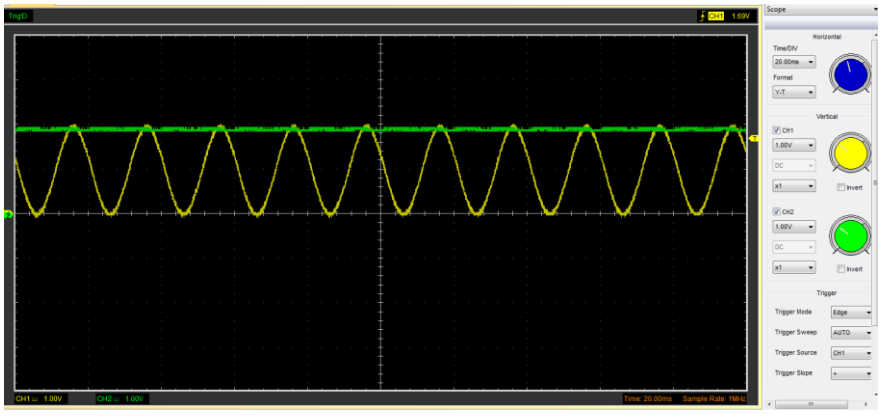

Figure 3.5: The d-axes component of the three-phase sinusoidal signal.

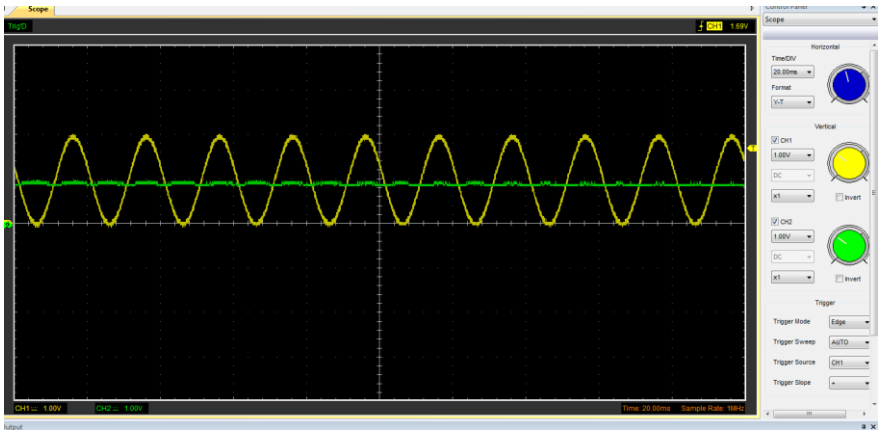

Figure 3.6: The q-axes component of the three-phase sinusoidal signal.

After comparing the results with the waveforms from the off-line simulator, there is a good agreement. Therefore, the PLL and d-q transformation code are considered as implemented correctly.

After successfully calculate the d-q component of the load current, the next step is to extract the harmonic component from i_{Ld} and i_{Lq}. The currents i_{Ld} and i_{Lq} consist of both fundamental and harmonic components, which can be separated by a HPF or a moving average block. In this application, a moving average block is implemented in the DSP to continuously calculate the average value of the load current. The currents i_{Ld} and i_{Lq} are fed to the moving average, and the outputs are their average values $\bar{i_{Ld}}$ and $\bar{i_{Lq}}$. Then the harmonic components $\tilde{i_{Ld}}$ and $\tilde{i_{Lq}}$ can be extracted by Eqn. 3.2.

$$\tilde{i_{Ld}} = i_{Ld} - \bar{i_{Ld}}$$
$$\tilde{i_{Lq}} = i_{Lq} - \bar{i_{Lq}} \tag{3.2}$$

The results of moving average are captured in the oscilloscope and shown in Fig. 3.7 and 3.8. The green waveforms are the current signals i_{Ld} and i_{Lq}, correspondingly. The yellow waveforms in Fig. 3.7 and 3.8 are the average values calculated by DSP, which are $\bar{i_{Ld}}$ and $\bar{i_{Lq}}$.

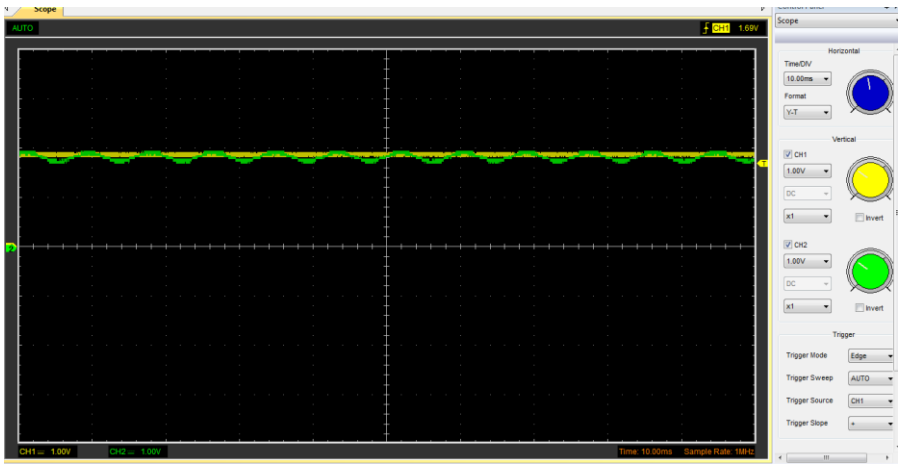

Figure 3.7: The moving average of current I_{Ld}.

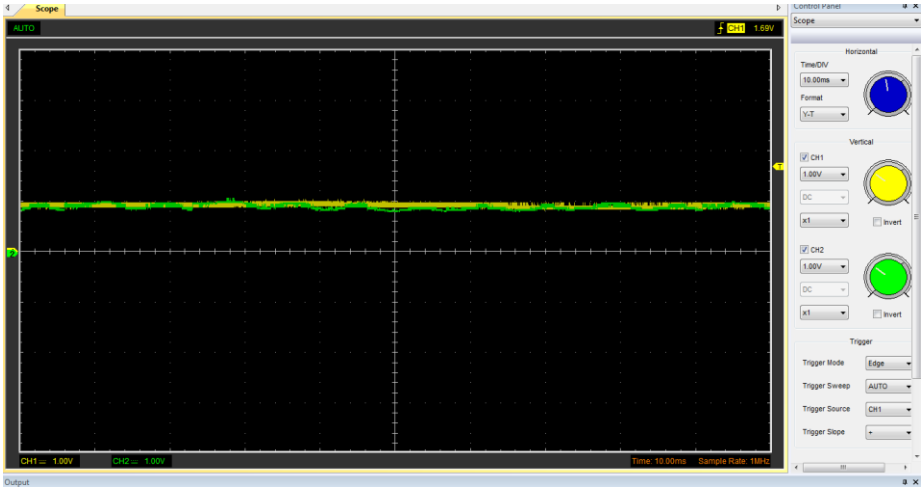

Figure 3.8: The moving average of current I_{Lq}.

Since the currents are injected into the grid by the APF must equal to the harmonic component of the load currents, the reference filter currents in d-q axes are now determined as $\tilde{i_{Ld}}$ and $\tilde{i_{Lq}}$. Before the reference filter current signals are transformed back to a-b-c axes, the output of the PI

controller for maintaining the DC-link capacitor voltage is combined with the $i_{Ld}^{\sim}$ signal. The PI controller implementation is discussed on the next section.

Additionally, an inverse Park's Transformation or d-q transformation is performed to bring the reference filter currents back to a-b-c coordinates. The inverse Park's Transformation is given in Eqn. 3.3.

$$\begin{bmatrix} i_{CA\_REF} \\ i_{CB\_REF} \\ i_{CC\_REF} \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{Cd\_REF} \\ i_{Cq\_REF} \end{bmatrix} \quad (3.3)$$

where, i_{Cd_REF} and i_{Cq_REF} are the reference filter current in d-q axes, i_{CA_REF}, i_{CB_REF}, and i_{CC_REF} are the reference filter current in a-b-c axes.

3.4 DC-Link Capacitor Voltage Control

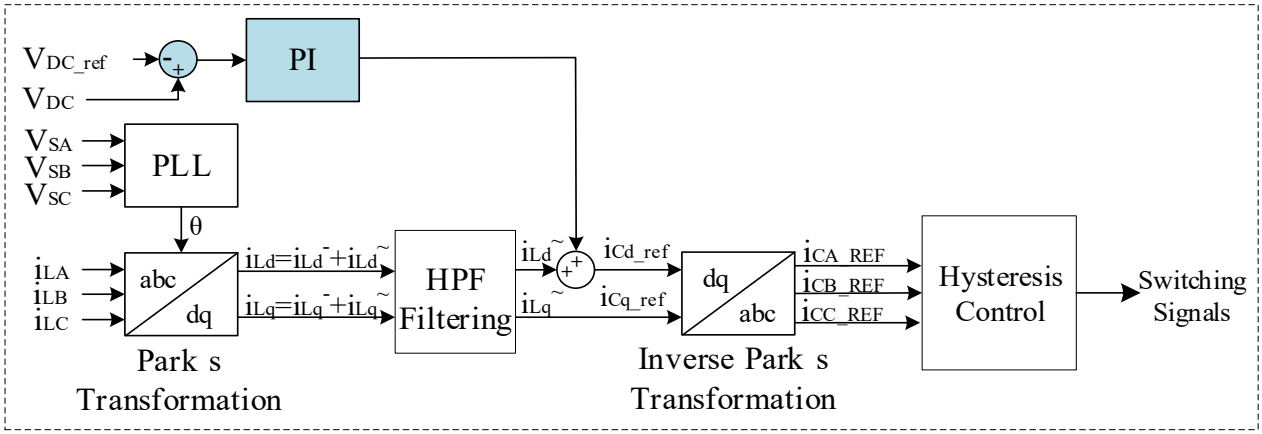

Figure 3.9: PI controller in the control loop.

The purpose of using PI control here is to keep the voltage of the DC-link capacitor of the APF at a desired level. The DC-link capacitor voltage is maintained by regulating the direct component

of the load current, I_{Ld}. The PI controller algorithm is described by Eqn. 3.4. and the discrete approximation of the integral is presented by Eqn. 3.5.

$$u(t) = K_p \times e(t) + K_i \times \int_a^b e(t)dx \tag{3.4}$$

$$Integral = PreviousIntergral + Error \times dt \tag{3.5}$$

where, $u(t)$ is the output of the PI controller, K_p and K_i are the proportional and integral gain of the PI controller, respectively. The $Error$ is the difference between the reference and actual DC voltage signals. The dt is the time step that programmed in the DSP.

3.5 Hysteresis Band Current Control

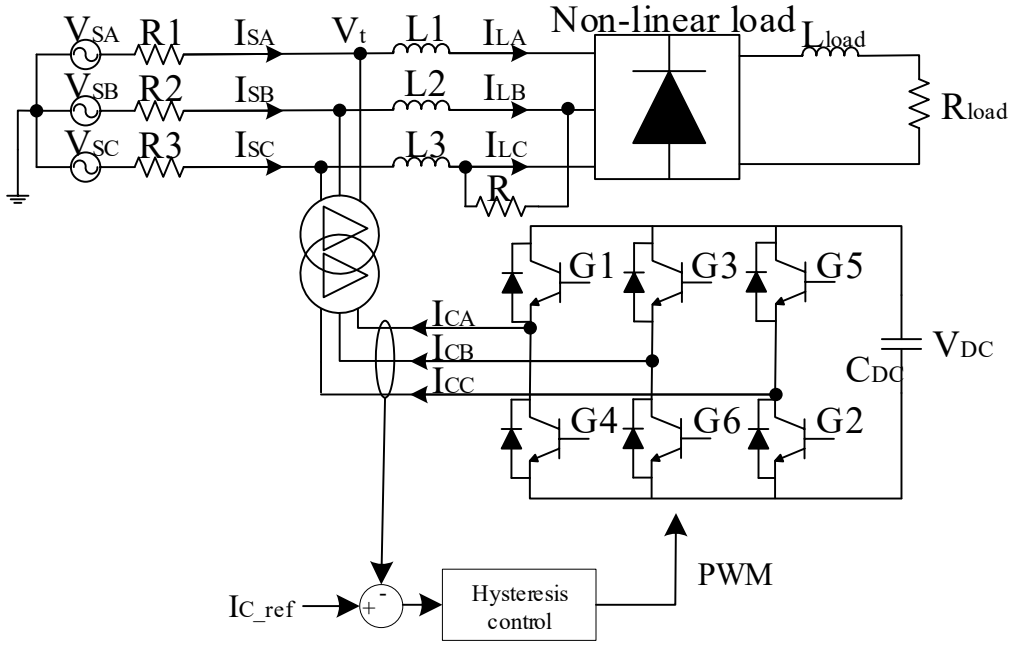

Figure 3.10: Hysteresis current controller in APF.

The HCC is selected as the current control technique to control the filter current because of its dynamic response time. Especially for the APF application, which requires high speed switching.

The detailed theoretical background was introduced in literature review chapter. The inputs of HCC are the actual filter current and reference filter current. The block diagram of an HCC in the APF is shown in Fig. 3.10.

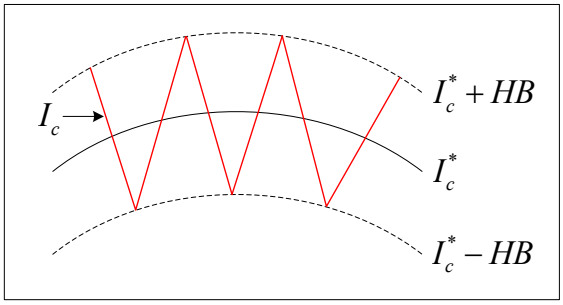

Figure 3.11: Hysteresis band current control.

The HB is set up by the designer. The basic idea of the HCC is shown in Fig. 3.11, that the actual filter current I_c is controlled in between an upper band and a lower band, where the upper band is equal to the reference filter current I_c^* plus the HB and the lower band is the subtraction of reference filter current I_c^* and HB. When the actual filter current I_c reaches the upper band, the IGBT will be turned off by the HCC so that the filter current drops. On the other hand, when the actual filter current I_c drops to the lower band, the HCC will turn on the IGBT to increase the filter current.

The HCC is implemented in the DSP using the built-in analog comparator subsystem (CMPSS). The analog comparators give user fast reaction time and dynamic control of the filter current. The inputs of HCC are the actual filter current and the reference filter current. The actual filter currents are fed to the HCC from the RT Box through analog signals. The filter reference currents are calculated in DSP at reference current extraction stage and then transformed to an analog signal by the internal DAC. The CMPSS compares actual current with the upper band and the lower band. The output of CMPSS triggers the enhanced pulse width modulator (EPWM) module, where

produces PWM signals to switch IGBTs on and off. Here are the ON-OFF criteria of the hysteresis control for phase A:

$$I_{CA} < I_{CA\_REF} - HB \tag{3.6}$$

$$I_{CA} > I_{CA\_REF} + HB \tag{3.7}$$

where I_{CA} is the phase A actual filter current, I_{CA_REF} is the phase A reference filter current, HB is the hysteresis band that is determined based on the desired switching frequency of the APF. When actual current is lower than the lower boundary as shown in Eq. (3.6), G1 is ON and G4 is OFF are shown on Fig. 3.10; when actual current is higher than the upper boundary as shown in Eq. (3.7), G1 is OFF and G4 is ON. In any other situation, the state of the switch remains unchanged. Similarly, phase B and C follow the same switching rule. The HCC block diagram of the software simulation is shown in Fig. 3.12.

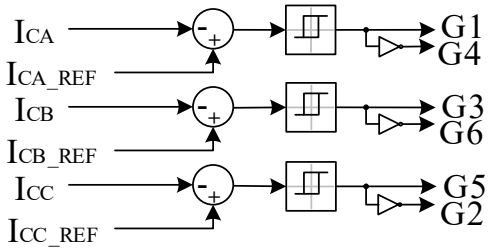

Figure 3.12: Block diagram of the HCC in software simulation.

3.5.1 Hysteresis Current Band Calculation

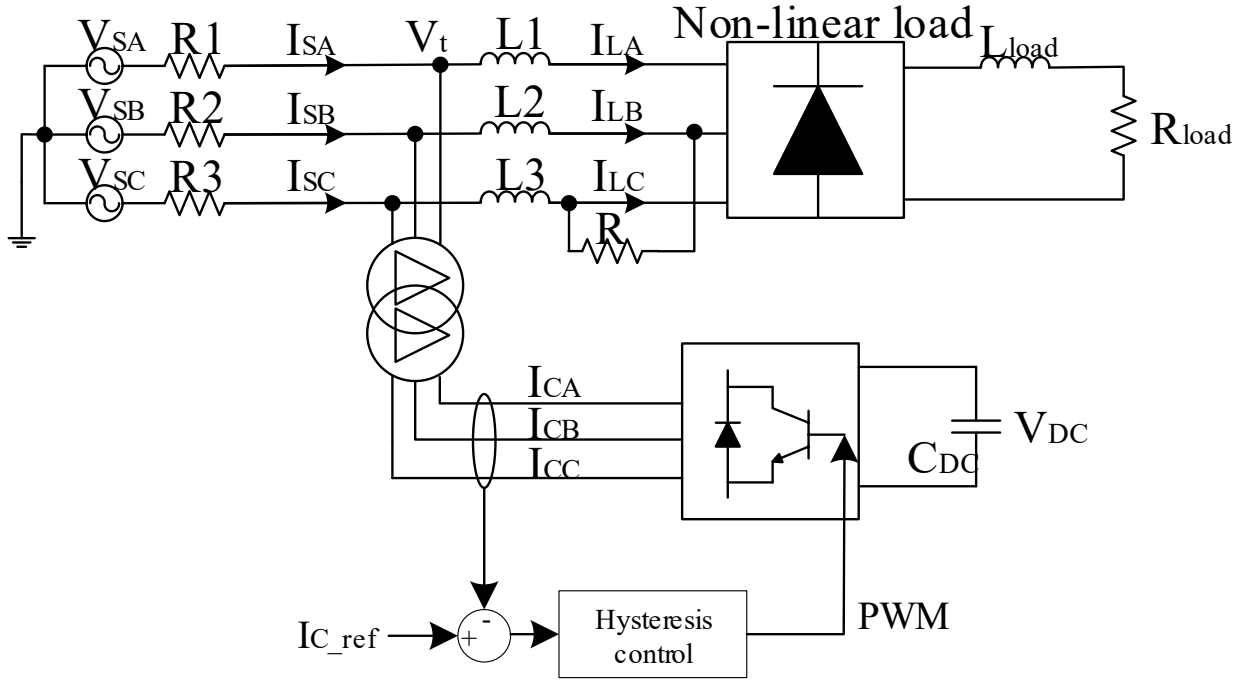

Figure 3.13: Hysteresis current control for APF.

Fig. 3.13 shows an overall system diagram for HCC model. One important parameter when setting up HCC is the HB. The HB defines an acceptable error in the filter current based around a reference filter current. By applying a positive and negative DC offset to the reference current, the actual filter current will vibrate up and down within the upper and lower limits. Fig. 3.14 shows HCC's operating modes.

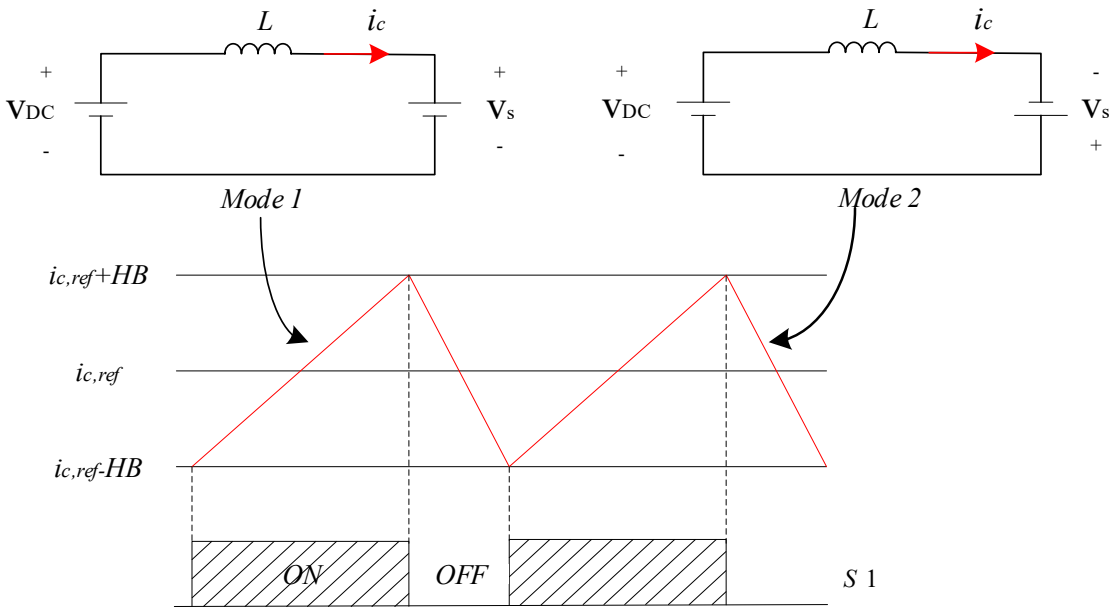

Figure. 3.14: Operating mode of the VSI.

Steady − State Characteristics:

There are two operating modes for the VSI. If switch 1 (G1) is selected as an example, the steady-state characteristics for the VSI can be calculated in mode 1 and mode 2 shown in Fig. 3.14.

Mode 1:

The inductor voltage: $$v_L = L\frac{di_c}{dt} \quad (3.8)$$

the inductor is the coupling transformer's secondary side leakage inductance.

$$v_L = v_{DC} - v_s(t)$$

$$L\frac{di_c}{dt} = v_{DC} - v_s(t)$$

$$L\frac{\Delta i_c}{T_{ON}} = v_{DC} - v_s(t)T_{ON} = \frac{L \cdot \Delta i_c}{v_{DC} - v_s(t)} \tag{3.9}$$

$Mode\ 2$:

$$v_L = v_{DC} + v_s(t) \tag{3.10}$$

$$T_{OFF} = \frac{L \cdot \Delta i_c}{v_{DC} + v_s(t)} \tag{3.11}$$

$Combined$:

$$T = T_{ON} + T_{OFF} = \frac{L \cdot \Delta i_c}{v_{DC} - v_s(t)} + \frac{L \cdot \Delta i_c}{v_{DC} + v_s(t)} = \frac{L \cdot \Delta i_c\big(v_{DC} + v_s(t)\big) + L \cdot \Delta i_c(v_{DC} - v_s(t))}{(v_{DC} - v_s(t))(v_{DC} + v_s(t))}$$

$$T = \frac{2 \cdot L \cdot \Delta i_c \cdot v_{DC}}{v_{DC}^2 - v_s^2(t)} \tag{3.12}$$

$The\ switching\ frequency$:

$$f_{sw}(t) = \frac{1}{T} = \frac{v_{DC}^2 - v_s^2(t)}{2 \cdot L \cdot \Delta i_c \cdot v_{DC}} \tag{3.13}$$

$where\ \Delta i_c = 2HB, the\ relationship\ between\ f_{sw}(t)\ and\ HB$:

$$f_{sw}(t) = \frac{1}{T} = \frac{v_{DC}^2 - v_s^2(t)}{4 \cdot L \cdot HB \cdot v_{DC}} \tag{3.14}$$

$$or\ HB = \frac{v_{DC}^2 - v_s^2(t)}{4 \cdot L \cdot f_{sw}(t) \cdot v_{DC}} \tag{3.15}$$

$where\ v_s(t) = V_s \cdot \sin(\omega_0 \cdot t),$

It is obvious that the switching frequency is varying along with the value of $v_s(t)$. However, the maximum and minimum value of the switching frequency $f_{sw}(t)$ can be found through following equations:

$$f_{sw}(t) = \begin{cases} Max\text{:}\ \dfrac{v_{DC}^2}{4 \cdot L \cdot HB \cdot v_{DC}} \\ Min\text{:}\ \dfrac{v_{DC}^2 - V_s}{4 \cdot L \cdot HB \cdot v_{DC}} \end{cases} \tag{3.16}$$

If HB is selected as 200A, which is around 10% of the magnitude of the reference current, then

Practical values:

$v_{DC} = 7kV,$

$L = 470\mu H,$

$V_s = 4.95kV$

V_S is the RMS value of the voltage on secondary side of the coupling transformer.

$$f_{sw}(t) = \begin{cases} Max: \dfrac{v_{DC}^2}{4 \cdot L \cdot HB \cdot v_{DC}} = 18.617\ kHz \\ Min: \dfrac{v_{DC}^2 - V_s}{4 \cdot L \cdot HB \cdot v_{DC}} = 9.307\ kHz \end{cases} \quad (3.17)$$

Therefore, based on the selected HB = 200A, the switching frequency of the APF should in the range between 9.3 ~ 18.6 kHz. From the steady-state characteristic analysis, the desired switching frequency range is calculated as theoretical value. In chapter 4, this value will be verified by comparing it with the switching frequency from the real-time HIL simulation.

3.6 Control Analysis

3.6.1 Power Circuit Configuration

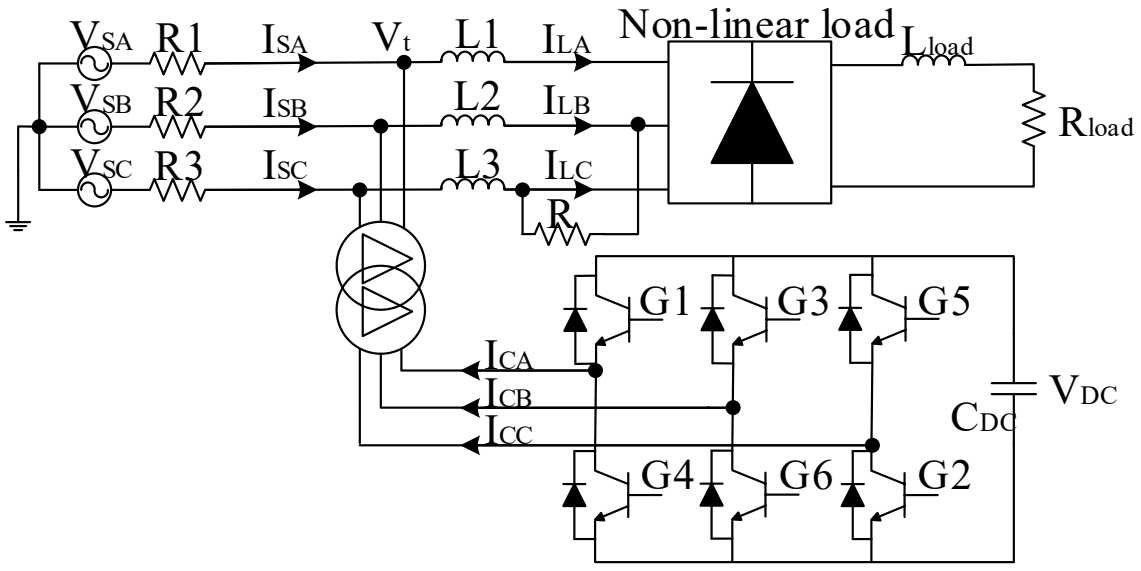

Figure 3.15: 3-phase diagram of the APF.

An APF is connected to the transmission line through a coupling transformer. The connection point is usually at the middle of the transmission line to provide voltage support. The VSI employs six IGBT semiconductor switches with anti-parallel diode which provides bi-directional power flow.

A detailed 3-phase system diagram of the APF using typical three-phase VSI is given in Fig. 3.15, where

V_{SA}, V_{SB}, V_{SC}: source voltage of phase a, b and c.

I_{SA}, I_{SB}, I_{SC}: source currents of phase a, b and c.

R_1, R_2, R_3: transmission line resistance.

V_t: voltage at the PCC.

L_t: leakage inductance of the coupling transformer on secondary side.

I_{CA}, I_{CB}, I_{CC}: APF current injected into the transmission line.

V_{DC}: the voltage across the DC-link capacitor of VSI.

3.6.2 System Simplification

In real electrical power systems, the transmission line and non-linear loads to which the APF is connected is under constantly changing status. It is difficult to take into consideration the complex system when analyzing the system model of the APF. Therefore, the system is simplified with some assumptions being made.

To simplify the circuit, the assumptions are made as follows:

(1) All semiconductor switches and diodes in the VSI are ideal,

(2) The coupling transformer is represented using its leakage inductor L_t,

(3) the converter is lossless.

The simplified three-phase APF circuit is shown in Fig. 3.16.

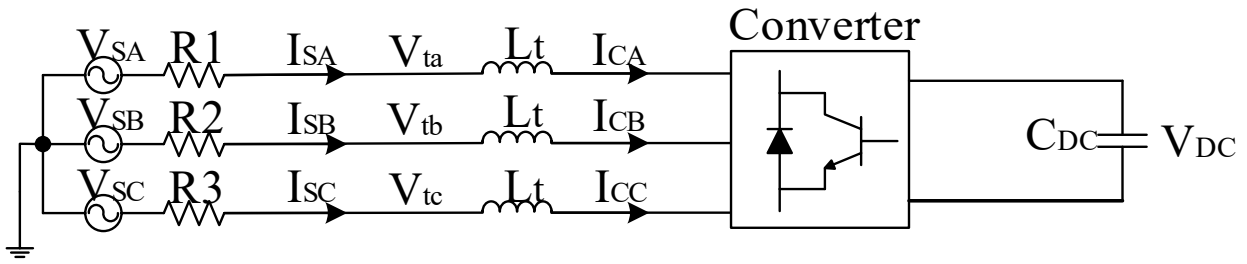

Figure 3.16: Simplified three-phase APF circuit.

The AC side output currents of APF are denoted by $[i_C] = [i_{CA}, i_{CB}, i_{CC}]^T$, the AC bus voltages at the PCC are denoted by $[v_t] = [v_{ta}, v_{tb}, v_{tc}]^T$, the source voltages are denoted by $[v_s] = [v_{SA}, v_{SB}, v_{SC}]^T$.

The power balance equation for the DC and AC side of the VSI can be written as:

$$P_{ac} = P_{dc} \tag{3.18}$$

3.6.3 Control System Small Signal Modelling

Since the control algorithm is based on synchronous rotating reference frame, the analysis of the system in Fig. 3.13 under done using d-q coordinates. The AC bus voltage at PCC is denoted by Eqn. 3.19:

$$[v_t] = \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} = V_t \begin{bmatrix} sin\theta \\ \sin(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \tag{3.19}$$

$$K = \frac{2}{3} \begin{bmatrix} cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.20}$$

The d-q-0 transformation equation is given in Eqn. 3.20, the inverse d-q-0 transformation is given in Eqn. 3.21.

$$K^{-1} = \frac{2}{3} \begin{bmatrix} cos\theta & -sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{3.21}$$

where $\theta = \omega t$ is the rotating phase angle of v_t.

The voltage and current variables can be then decomposed into d and q components by the transformation matrix **K**:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \\ 0 \end{bmatrix} = K \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}, \begin{bmatrix} v_{td} \\ v_{tq} \\ 0 \end{bmatrix} = K \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix}, \begin{bmatrix} i_{cd} \\ i_{cq} \\ 0 \end{bmatrix} = K \begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} \tag{3.22}$$

v_{td} and v_{tq} can be derived using Eqn. 3.19, 3.20, and 3.21 as follow:

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ 0 \end{bmatrix} = K \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot V_t \begin{bmatrix} sin\theta \\ \sin(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) \end{bmatrix}$$

$$v_{td} = \frac{2}{3} V_t \left[sin\theta cos\theta + \sin\left(\theta - \frac{2\pi}{3}\right) \cos\left(\theta - \frac{2\pi}{3}\right) + \sin(\theta + \frac{2\pi}{3}) \cos(\theta + \frac{2\pi}{3}) \right]$$

$$v_{tq} = -\frac{2}{3} V_t \left[sin\theta sin\theta + \sin\left(\theta - \frac{2\pi}{3}\right) \sin(\theta - \frac{2\pi}{3}) + \sin(\theta + \frac{2\pi}{3}) \sin(\theta + \frac{2\pi}{3}) \right]$$

Then, according to [93], both equations can be simplified as following:

$$v_{td} = \frac{2}{3} \cdot \frac{3}{2} \cdot V_T \cdot \sin(\theta - \theta) = V_T \tag{3.23}$$

$$v_{tq} = -\frac{2}{3} \cdot \frac{3}{2} \cdot V_T \cdot \cos(\theta - \theta) = 0 \tag{3.24}$$

The instantaneous three-phase active power on the AC-side of the APF is:

$$P_{ac} = v_{ta} i_{ca} + v_{tb} i_{cb} + v_{tc} i_{cc} \tag{3.25}$$

The instantaneous three-phase active power can also be written in d-q-0 components [93]:

$$P_{ac} = \frac{3}{2} (v_{td} i_{cd} + v_{tq} i_{cq} + 2 v_{t0} i_{c0}) \tag{3.26}$$

If under balanced operation, $v_{to} = i_{co} = 0$, the expression for power is given by:

$$P_{ac} = \frac{3}{2}(v_{td}i_{cd} + v_{tq}i_{cq}) \tag{3.27}$$

Substitute the variables with Eqn. 3.23 and 3.24:

$$P_{ac} = \frac{3}{2}V_t i_{cd} \tag{3.28}$$

The power balance equation Eqn. 3.18 gives the relationship between the active power delivered by the AC source and absorbed by the DC side of the APF. In order to simplify the analysis complexity, assuming the converter has 100% efficiency, the input and output powers are the same.

The active power of the APF on the DC side is:

$$P_{dc} = v_{DC}(t) \cdot C \cdot \frac{dv_{DC}(t)}{dt} \tag{3.29}$$

Combining Eqn. 3.18, 3.28, and 3.29:

$$\frac{3}{2}V_t i_{cd}(t) = v_{DC}(t) \cdot C \cdot \frac{dv_{DC}(t)}{dt} \tag{3.30}$$

To analyze the small signal disturbance response, V_t is assumed stable. The small disturbances of signals $i_{cd}(t)$ and $v_{DC}(t)$ are represented by $\Delta i_{cd}(t)$ and $\Delta v_{DC}(t)$, Eqn. 3.30 can be rewritten as:

$$\frac{3}{2}V_t\left(I_{cd} + \Delta i_{cd}(t)\right) = (V_{DC} + \Delta v_{DC}(t)) \cdot C \cdot \frac{d(V_{DC} + \Delta v_{DC}(t))}{dt} \tag{3.31}$$

Ignoring the DC steady state variables and second order signals,

$$\frac{3}{2}V_t\Delta i_{cd}(t) = V_{DC} \cdot C \cdot \frac{d\Delta v_{DC}(t)}{dt} \tag{3.32}$$

Laplace transform of Eqn. 3.32:

$$\frac{3}{2}V_t\Delta i_{cd}(s) = V_{DC} \cdot C \cdot s \cdot \Delta v_{DC}(s) \tag{3.33}$$

Eqn. 3.33 can be rewritten as:

$$T_p(s) = \frac{\Delta v_{DC}(s)}{\Delta i_{cd}(s)} = \frac{\frac{3}{2}V_t}{V_{DC} \cdot C \cdot s} \tag{3.34}$$

Hence, Eqn. 3.34 represents the small signal response of DC-side voltage v_{DC} to the d-component of the APF output current i_{cd}. $T_p(s)$ represents the transfer function of the power stage.

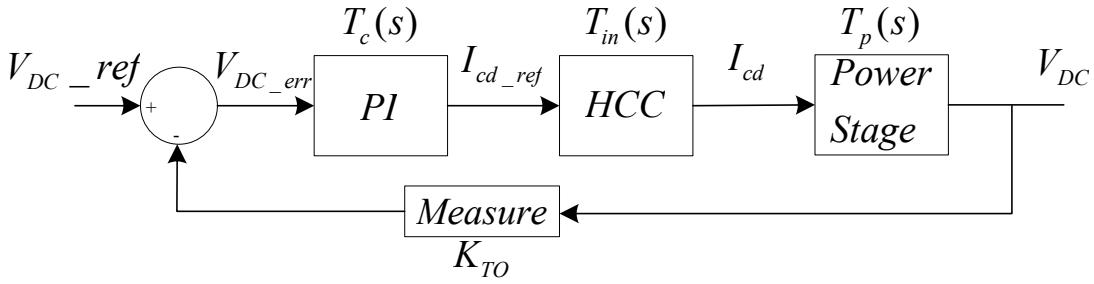

Figure 3.17: Control loop block diagram.

The control loop block diagram is developed in Fig. 3.17 which is based on the control algorithm introduced and illustrated in Fig. 3.1 in the beginning of this chapter. The transfer function of the converter is $T_p(s)$, which has already been derived in Eqn. 3.34. The parameter K_{TO} is the gain for scaling down the V_{DC} signal. The transfer function of the PI regulator is $T_c(s)$ and the transfer function of the HCC is $T_{in}(s)$. The control strategy of HCC is to force the APF output current i_c

to track the reference current i_{c_ref}. Since the fundamental component for both i_c and i_{c_ref} are in phase and have same magnitude, despite harmonics present in i_c, the overall HCC control block can be treated as a unit gain factor. The PI controller transfer function can be written as:

$$T_c(s) = -K_{TO}(K_p + \frac{K_i}{s}) \tag{3.35}$$

Practical values:

$V_T = 11.390\ kV$, the magnitude of the voltage at the PCC.

$V_{DC} = 7\ kV$, the APF DC-side voltage.

$C = 0.5\ F$, the APF DC-side capacitance.

K_p, the PI controller proportional gain.

K_i, the PI controller integral gain.

The power stage transfer function:

$$T_p(s) = \frac{\Delta v_{DC}(s)}{\Delta i_{cd}(s)} = \frac{\frac{3}{2}V_t}{V_{DC} \cdot C \cdot s} = \frac{\frac{3}{2} \times 11390}{7000 \times 0.5 \times s} = \frac{17085}{3500s} \tag{3.36}$$

PI controller transfer function:

$$T_c(s) = \left(K_p + \frac{K_i}{s}\right) = K_i(\frac{\frac{K_p}{K_i}s + 1}{s}) \tag{3.37}$$

The transfer function of the process is shown as follow:

$$T_1(s) = T_{in}(s)T_p(s) = \frac{17085}{3500s} \times 1 = \frac{17085}{3500s} \tag{3.38}$$

Design Criteria for PI controller:

The bode plot of power stage transfer function $T_1(s)$ is shown in Fig. 3.18. Since the switching frequency of the APF is 11kHz ~ 17kHz, the averaging switching frequency is around 14kHz. The crossover frequency for tuning the controller parameter can be chosen as 10% of the switching frequency, which is 1.4kHz or 8796.45 rad/s. In Fig. 3.18, at chosen crossover frequency the process stage has a Gain Margin (GM) of -65.1dB.

In order to achieve a fast setting time and keep the entire system stable, the design criteria for the controller is to keep the Phase Margin (PM) of the entire system higher that 45°. In other words, the phase angle of the entire system needs to be higher than $-135°$. The phase angle is at $-90°$ which is $45°$ higher than $-135°$.

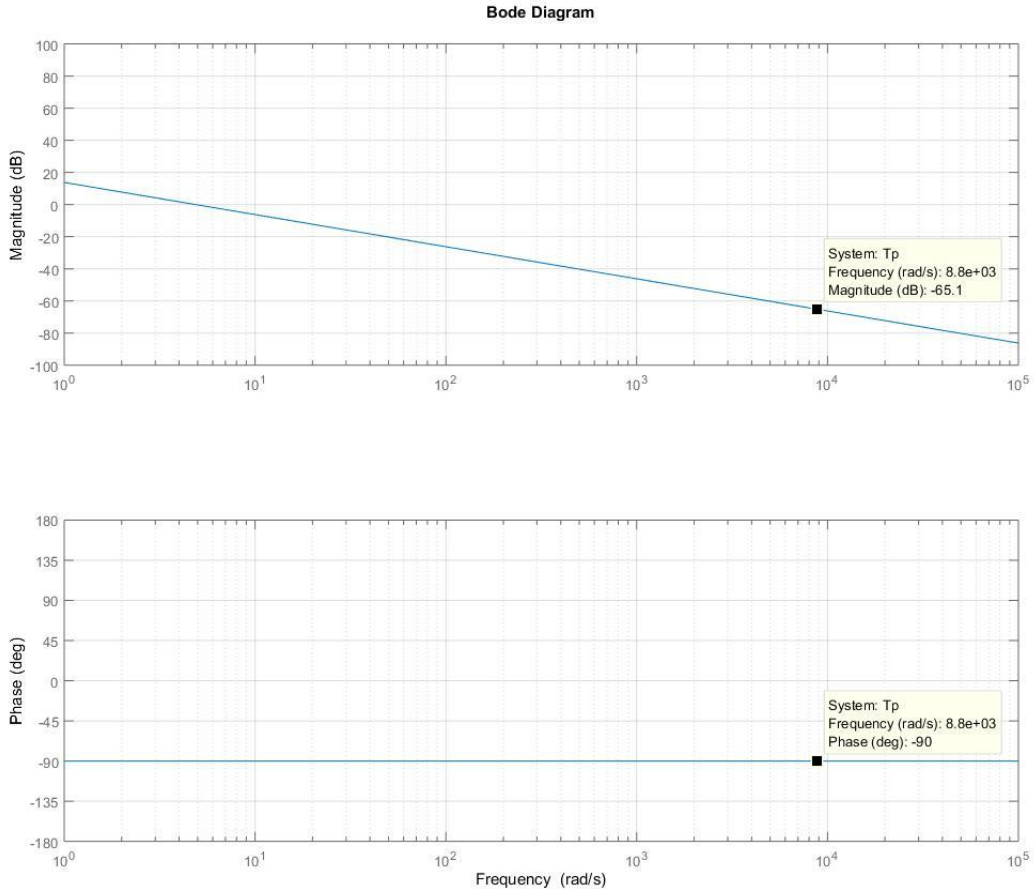

Figure 3.18: Bode plot of power stage transfer function $T_1(s)$.

$$20\log(K_p) \geq 65.1 \tag{3.39}$$

$$K_p \geq 1798.87 \tag{3.40}$$

$$\frac{K_i}{\omega_c K_p} \leq tan45° \tag{3.41}$$

$$K_i \leq 1 \times 8796.45 \times 1798.87 = 1.582 \times 10^7 \tag{3.42}$$

Choose $K_p = 1800, K_i = 18000$:

$$T_c(s) = \left(K_p + \frac{K_i}{s}\right) = \left(K_p + \frac{K_i}{s}\right) = (1800 + \frac{18000}{s}) \tag{3.43}$$

The overall system transfer function:

$$\begin{aligned} T_{OL}(s) = T_c(s)T_1(s) &= \left(1800 + \frac{18000}{s}\right) \times \frac{17085}{3500s} \\ &= \frac{30753s + 307530}{3.5s^2} \end{aligned} \tag{3.44}$$

The Bode plot of the overall system transfer function is shown in Fig.3.19.

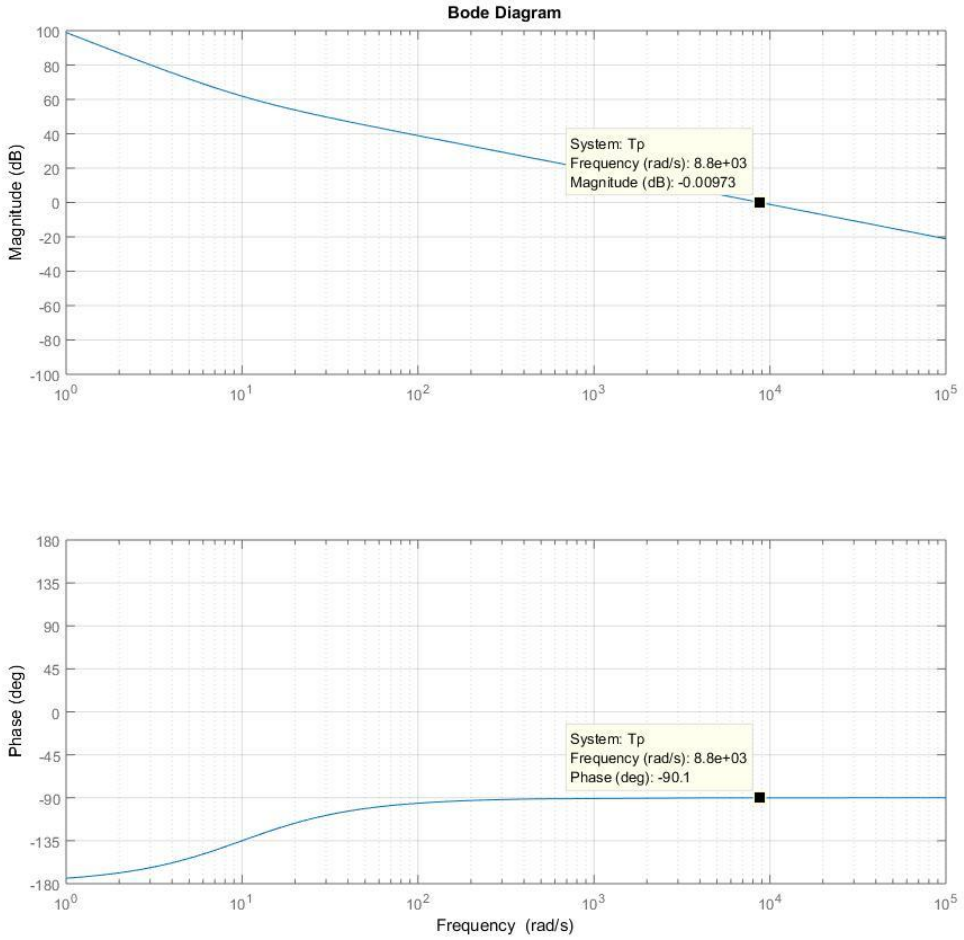

Figure. 3.19: Bode plot of the overall system transfer function.

As a conclusion, the selected PI controller parameters can keep the entire system stable with a PM of 45 degrees. This optimization is done at one operation point, which is under the worst scenario. Also, sub-optimization may be performed for other operation points. For a robust controller, it should maintain a good performance for all operating points. This is left for future work.

3.7 Conclusion

The implementation of the control system is worked on a step-by-step basis. The first stage is the software simulation, where most of the parameters of the controller are determined and ready to use as a reference. Then second stage is to split the control system into several blocks, then program and test each of the blocks individually. In this stage, the real-time simulator RT Box is utilized. After ensuring each block is working properly, they can be combined one at a time to test the results. So, if the result is incorrect, it makes the designer much easier to troubleshoot. The band of the hysteresis controller is calculated in steady-state analysis. Also, in this chapter, the small-signal analysis is performed to investigate the controller stability. The flow chart of the whole control system will be given in the appendix.

Chapter 4: Real-time Controller Hardware-in-the-Loop Simulation

4.1 Introduction

Based on the literature review and controller implementation presented in Chapter 2 and 3, a real-time CHIL simulation has been designed and implemented on a RT Box real-time simulator and a DSP microprocessor. The power circuit including the electric grid with a non-ideal load and the APF is modelled inside the RT Box. The control system described in Chapter 3 is implemented in a DSP.

Prior to performing the real-time simulation, the power circuit and controller have been simulated in PLECS software to demonstrate the feasibility and provide a reference that can guide real-time simulation effectively.

The real-time simulation is performed using the RT Box and a DSP (TMS320F28377S). The power circuit is implemented in the RT Box through the simulation software PLECS. On the other hand, the implementation of the controller is done by programming in the CCS. Results are shown and discussed in this section. The simulation parameters are listed in Table 4.1. And the CHIL testing platform is shown in Fig. 4.1.

Table 4.1: Real-Time Controller Hardware-in-the-Loop Simulation Parameters.

Components	**Parameter description**	**Value**
Power Grid	Source Voltage (V_S) $_{peak\text{-}peak}$	11.43 kV
	Line Resistance (Rs)	0.01 Ω
	Line Inductance (L1, L2 and L3)	0.1 mH
	Fundamental Frequency (f)	50 Hz
Load	Load Inductance (L_{load})	0.1 mH
	Load Resistance (R_{load})	7 Ω
	Resistor (R)	7 Ω
APF	DC Capacitor	0.5 F
	DC-Link Reference Voltage	7 kV
	Switching Frquency	10.93-17.98 kHz
Transformer	Winding Ratio	80:15 kV/kV
	Primary Leakage Inductance	1 mH
	Secondary Leakage Inductance	470 μH
Controller	DSP Sampling Rate	20μs
	PLL Proportional Gain	1000

Components	Parameter description	Value
	PLL Integral Gain	1000
	DC-link PI Proportional Gain	1800
	DC-link PI Integral Gain	18000
	Hysteresis Band (HB)	200 A
	RT Box Analog Output Scale Factor	0.0001
	RT Box Analog Output Offset	1.5V

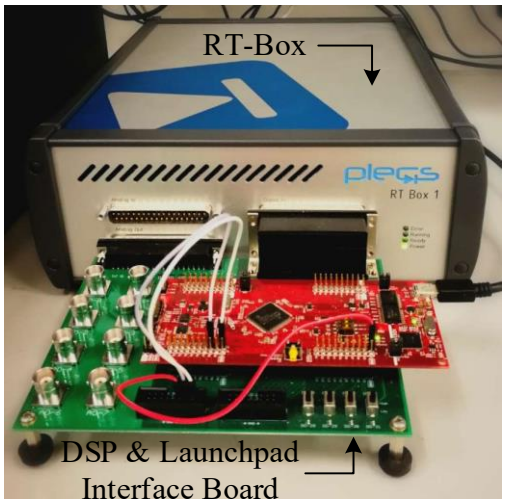

Figure 4.1: A general view of the RT Box simulator, the DSP microcontroller and the Launchpad interface board.

The RT Box and the DSP communicate through the analog I/Os. A Launchpad Interface board facilitates a convenient connection between the RT Box and the controller. It helps users to test control algorithms without building own interface hardware. Also, the board gives access to 8

analog outputs of the RT Box through BNC connectors, 8 digital input pins and 8 digital output pins.

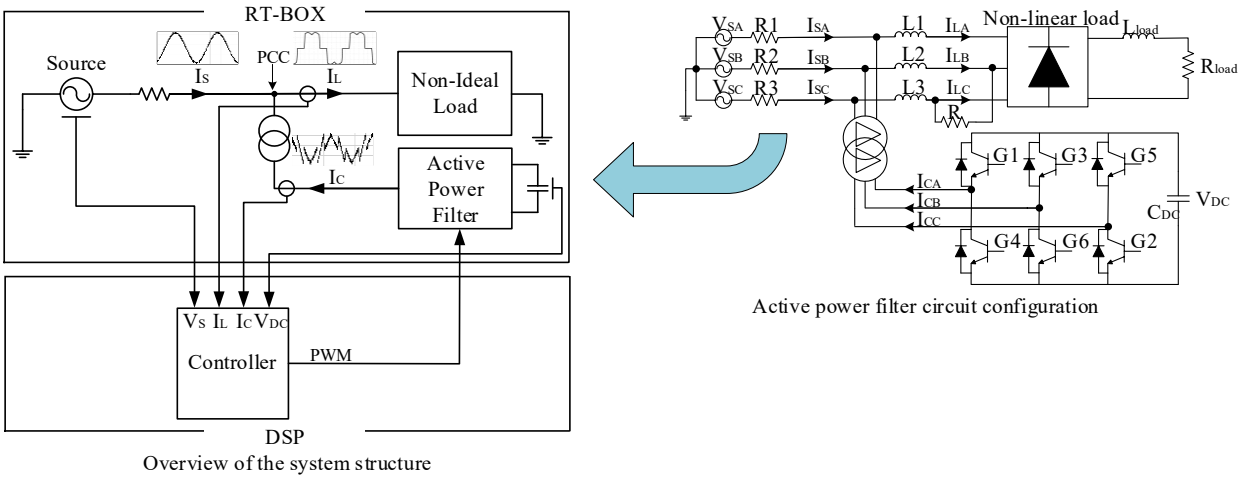

Figure 4.2: Overview of the HIL system structure.

The overall structure of the implemented CHIL demonstrator is shown in Fig. 4.2, a non-ideal load is fed by a three-phase source. The load is described as non-ideal because it represents not only non-linear load but unbalanced load. The implemented controller is developed to improve poor PQ issues that include current harmonics, current unbalances and low power factor.

As illustrated in Fig. 4.2, the power circuit including the three-phase source, the non-ideal load and an APF are implemented in the RT Box. The RT Box is a latest developed real-time simulator, which provides a platform for real-time HIL testing with 1 GHz CPU. The simulator is running at a step-size of 6 μs under this circuit complexity. The controller is implemented in a Single-Core Delfino Microcontroller (TMS320F28377S) from Texas Instruments. A PLL and an SRF-based filter reference current extraction method are programmed to continuously calculate filter reference current, then the HCC compares both actual and reference filter currents to generate gating signals.

Meanwhile, the DC-link capacitor voltage is maintained by a PI controller. The DSP sampling rate is programmed as 48.82 kHz.

Fig. 4.2 shows the power circuit of APF. A voltage-source converter equipped with a DC capacitor is used. A rectifier with an RL load is connected to the gird as the harmonics source. To create unbalance load currents, a resistor R is placed between phase B and phase C. The shunt connected APF injects compensation currents into the grid to eliminate current harmonics, compensate reactive power and balance currents. The APF is connected to an 11.3 kV system through an 80kV:15kV delta-delta transformer. Table 4.1 shows the parameters of the APF system and power grid. A voltage-sourced converter is chosen because of its high efficiency, lower cost and smaller compare to a current-sourced converter [4]. Six IGBT switches are connected in anti-parallel with free-wheeling diodes, which provides bi-directional power flow.

For real-time interfacing between the RT Box and the DSP, parameters in the RT Box need to be scaled down to fit the analog output range. Scaling factors are also listed in Table 4.1. Once the scaled analog signal is sent to the DSP, it is scaled back to original value for simple implementation.

The objective of this project is to implement a DSP-based controller and evaluate the controller performance utilizing the CHIL simulation. The RT Box can capture digital signals with a time resolution of less than 10 ns. The reason for using CHIL simulation is that the APF is working at a high voltage level in 11.3 kV and high switching frequency around 10 kHz. To study the behavior of the control loop, CHIL is an effective platform in university laboratory conditions to minimize the risk, cost and duration. The complete controller can be tested without the real power stage.

4.2 Real-Time Simulation Results

As mentioned in last section, the non-ideal load consists of a rectifier with an RL load and a resistance between phase B and C. The non-ideal load produces current harmonics as well as unbalanced current simultaneously. The performance of the proposed controller is evaluated and discussed in following circumstances. The waveforms are captured in real-time simulation using an oscilloscope.

4.2.1 Current Harmonic Elimination and Load Balancing

Since the RT Box's analog output is ranged from 0 to 5 V, all analog signals coming out of RT Box have been scaled down by a factor of 0.0001 and added an offset of 1.5 V. For instants, the amplitude of source current phase A is 4408 A. In this case, it will be scaled to 1.94 V at the analog output channel.

In Fig. 4.3, the three-phase source currents without APF compensation is shown. In this case, the source currents are exactly same as the load currents. These currents are polluted by harmonic and unbalance currents. It is obvious that the amplitude of I_{SA} is lower than the other phases, which is caused by the resistor R between phase B and C.

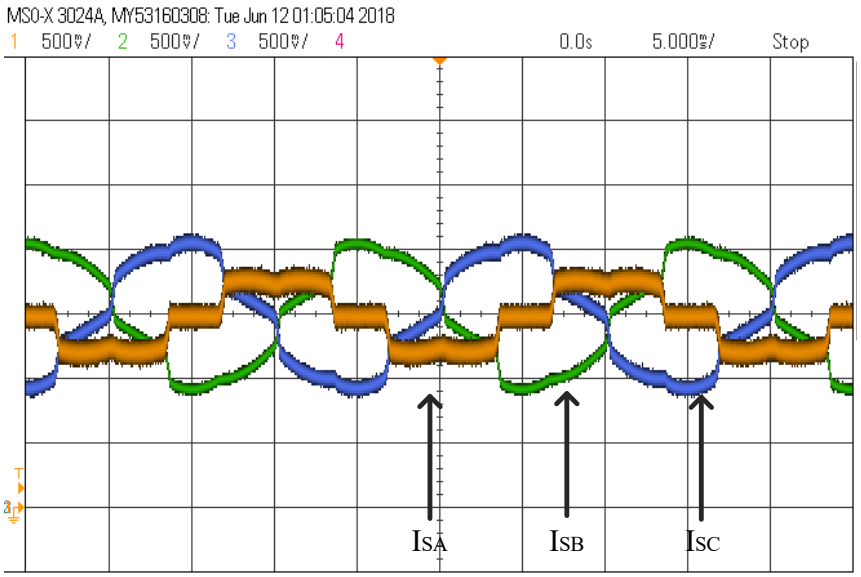

Figure 4.3: Three-phase source currents without APF.

Then, the APF is connected to the grid. The three-phase source current at the PCC is observed in oscilloscope. It is obvious that the currents now are balanced and compensated as in Fig. 4.4.

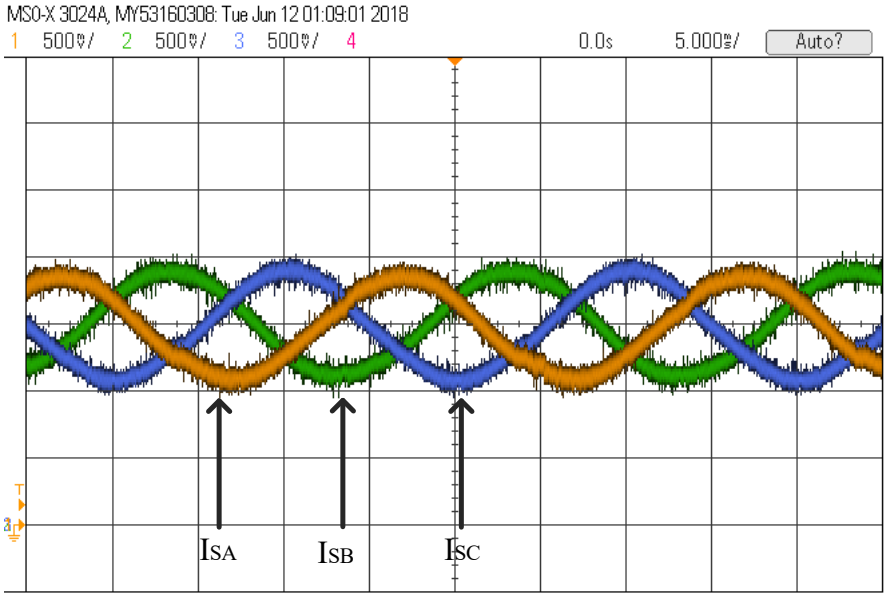

Figure 4.4: Three-phase source currents with APF.

The APF injects compensation current into the grid that compensates the harmonics and unbalances. The three-phase filter currents are shown in Fig. 4.5.

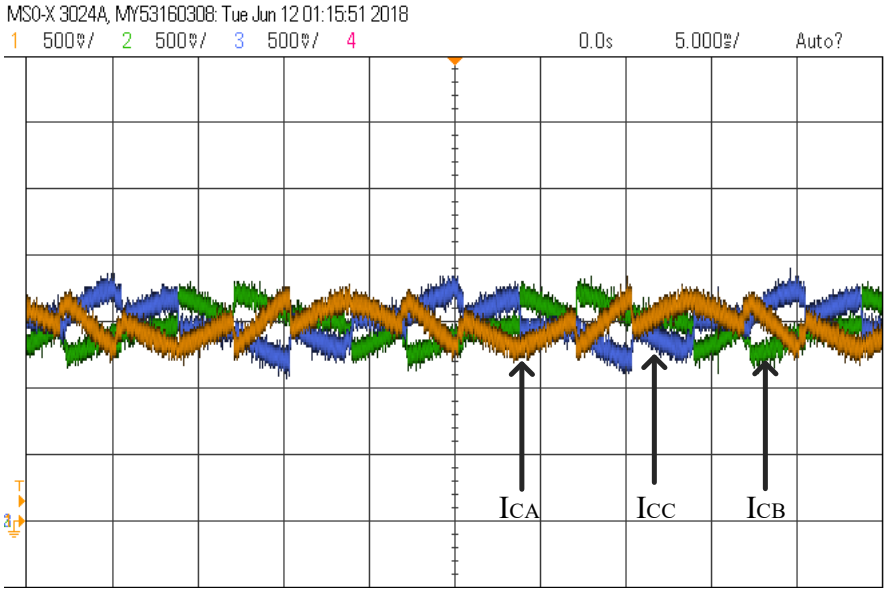

Figure 4.5: Three-phase filter currents injected into the grid.

A factor is normally used to evaluate APF is THD. The standard of harmonic control in electric power systems is explained in the IEEE Std 519 [9]. The current THD can be calculated as the ratio of the root-sum-square value of the harmonic content of the current to the root-mean-square value of the fundamental voltage [9].

$$I_{THD} = \frac{\sqrt{I_2^2+I_3^2+I_4^2+I_5^2+\cdots}}{I_1} \times 100\% \tag{4.1}$$

where I_{THD} is the THD percentage of a signal, I_1 is the fundamental frequency component, I_n $(n = 2, 3, 4, \ldots, \infty)$ are the harmonic component of the signal.

The THD of the source current phase A, B, and C are calculated using Eqn. 4.1. A comparison of THD with and without active filtering is listed in Table 4.2. The THD of source current phase A,

B and C without APF are calculated using Eqn. 4.1, which are equal to 27.96%, 14.74% and 14.87%, respectively. After compensation, the current THD of each phase then decreased to 4.62%, 4.66% and 5.31%.

Table 4.2: Comparison of source current THD with and without the APF.

	Source Current Phase A	Source Current Phase B	Source Current Phase C
THD without APF	27.96%	14.74%	14.87%
THD with APF	4.62%	4.66%	5.31%

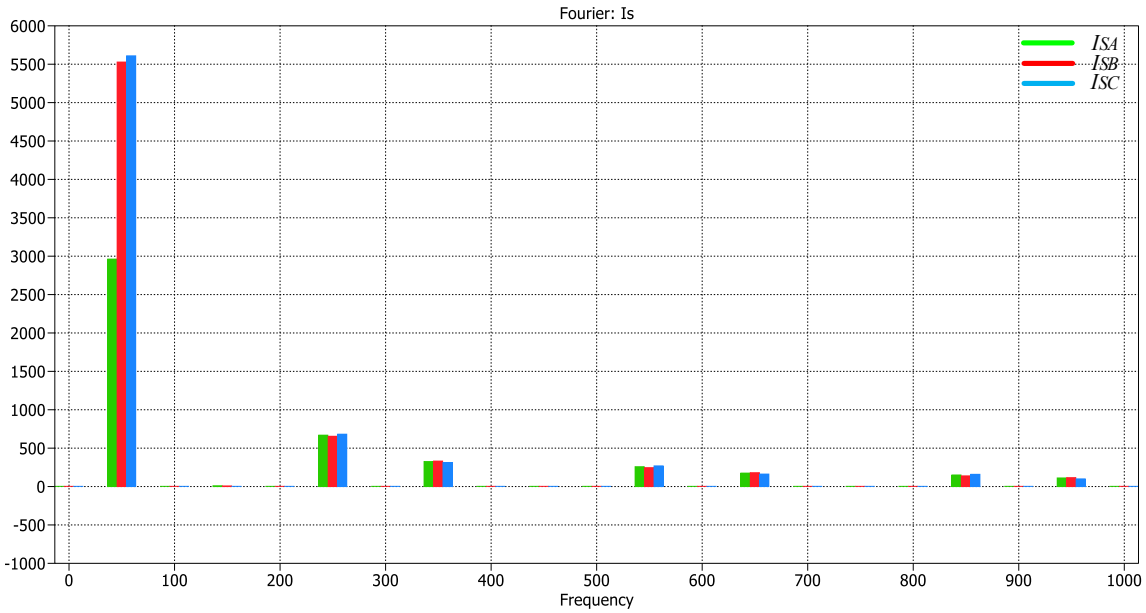

Figure 4.6: Fourier spectrum of the three-phase source current without APF.

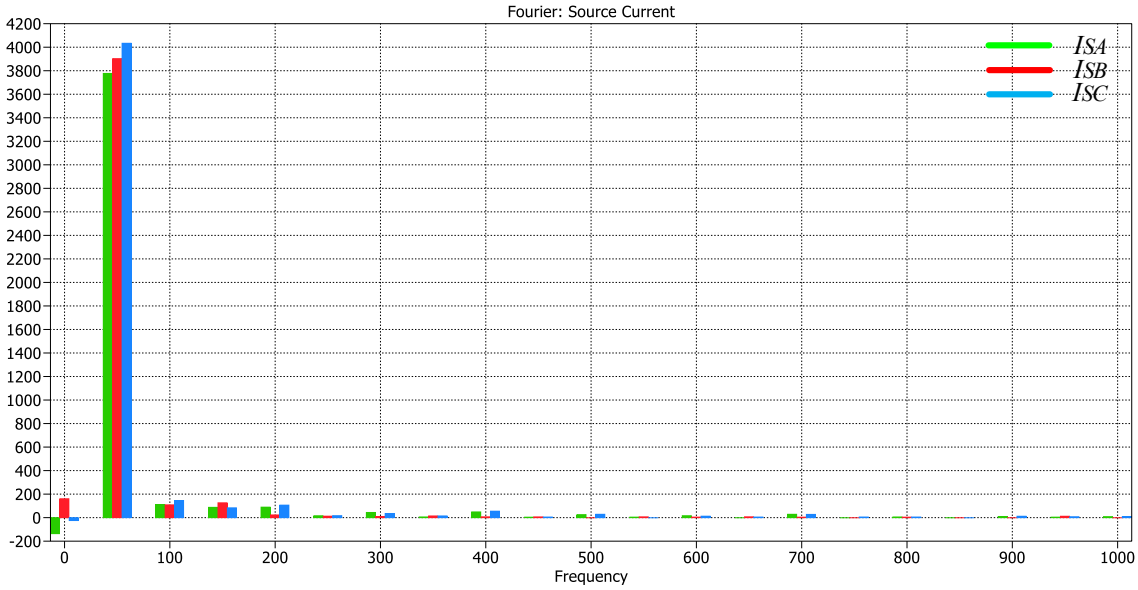

Figure 4.7: Fourier spectrum of the three-phase source current with APF.

Fig. 4.6 illustrates the Fourier spectrum of three-phase source currents without APF and Fig. 4.7 is the Fourier spectrum of three-phase source currents after connecting APF. The Fourier spectrum is obtained directly from the PLECS software. When the CHIL simulation is running in real-time, the PLECS provides an "External Mode" so the user can observe and analyze real-time data easily. Fig. 4.6 shows the unbalance in source current phase A along with strong signs of harmonics at 5^{th}, 7^{th}, 11^{th}, 13^{th}. The Fourier spectrum in Fig. 4.7 shows significant harmonic component reduction in source current after compensating.

As a conclusion, the three-phase source current waveform shows the implemented controller has the ability of harmonic elimination and load balancing. From the THD, it is obvious that the THD percentage for three-phase source current reduced from 27.96%, 14.74%, 14.87% to 4.62%, 4.66%, 5.31%. The recommended maximum THD in the IEEE Std 519 is 5%. Therefore, the THD of phase A and B satisfy the requirement. However, THD of phase C is 6% greater than the requirements. This can be attributed to the delay in the interface between the control hardware and the simulator.

The delay implies that the hysteresis controller is therefore not able to increase or decrease load current when it first exceeds the switching threshold, a result of which is an artificially higher harmonic content. So, it can be said with some degree of confidence, that the actual controller would work within 5% threshold. According to researches related to simulation delay in real-time HIL of hysteresis current control [92], propagation delay can cause significant THD increment. For example, a 30 μs delay will lead to a THD incensement from 20% to 50%. The simulation delay of the HIL HCC will be discussed and calculated in Chapter 4.

4.2.2 Power Factor Correction and DC-Link Voltage Control

Besides the harmonic current elimination and load current balancing, another important function of the APF is to perform the Power Factor Correction (PFC). As described in literature review chapter, low power factor is a negative effect that caused by non-linear loads. The lower the power factor, the higher the current is drawn from the source, which will incur more energy losses. The APF brings the power factor back to unity by compensating reactive power.

Fig. 4.8 shows the waveform of phase A source current I_{SA} and source voltage V_{SA}. It is clear they are in-phase which means a high-power factor is achieved. The purple line shows the DC-link capacitor voltage V_{DC} that is controlled by the PI controller. The reference DC voltage V_{DC}^{*} is set as 7kV. The waveform of V_{DC} on the oscilloscope indicates the voltage level is at 7kV.

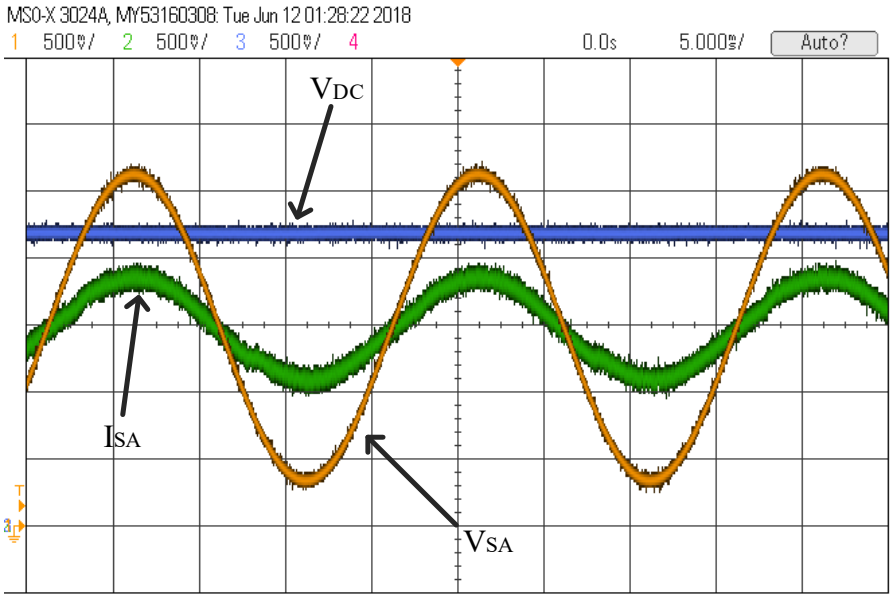

Figure 4.8: Phase A source voltage and current, DC-link voltage.

4.2.3 Switching Frequency of the APF

In Fig. 4.9, the waveforms of the source current phase A and gating signal of G1 are captured. The FFT function is used in the oscilloscope to analysis gating signal of G1. The variable switching frequency is in the range from 10.93 kHz to 17.98 kHz.

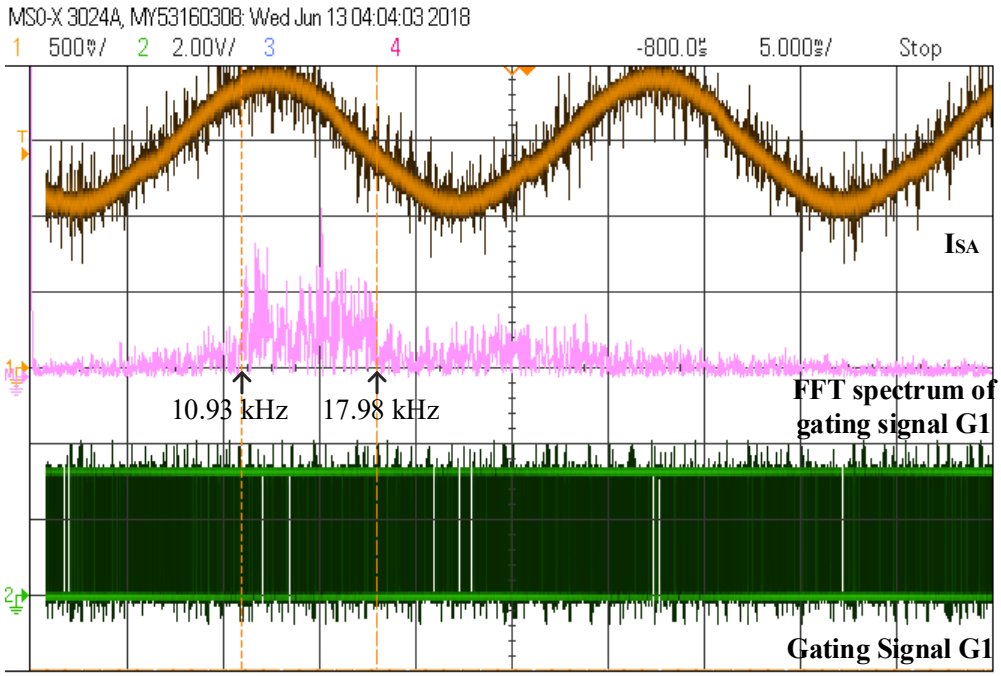

Figure 4.9: Source current phase A, FFT spectrum of G1 and gating signal G1.

In Section 3.5.1, the theoretical value of the switching frequency is calculated in the range of 9.3 kHz ~ 18.6 kHz. The real-time simulation results are within the theoretical values, which successfully verified the results in both steady-state analysis and real-time simulation.

Another important point in this section is to find out what is the maximum switching frequency the system can response. Recalling the equation used in Chapter 3:

$$f_{sw}(t) = \begin{cases} Max: \dfrac{v_{DC}^2}{4 \cdot L \cdot HB \cdot v_{DC}} \\ Min: \dfrac{v_{DC}^2 - V_s}{4 \cdot L \cdot HB \cdot v_{DC}} \end{cases} \tag{4.2}$$

.

The value of switching frequency $f_{sw}(t)$ is inverse proportional to HB. Theoretically, $f_{sw}(t)$ will increase when HB decreases.

However, during the real-time HIL simulation with RT Box, the switching frequency stops increasing once it reaches about 18 kHz, which is shown in Fig. 4.9. In order to figure out the problem, waveforms of filter current phase A, i_{CA} and the gating signal of IGBT, G1 are observed in oscilloscope and shown in Fig. 4.10 and Fig. 4.11. It is obvious that there is a significant simulation delay between the gating signal and the filter current. Simulation delay in real-time HIL of hysteresis current control has been introduced in Section 4.2.1 and mentioned in paper [92]. The simulation delay causes poor performance in harmonic elimination in terms of THD. Also, the switching frequency is constrained by the simulation delay. Several waveforms are captured to calculate the average simulation delay time. After analyzing the signals using oscilloscope in real-time HIL simulation, the average simulation delay time can be calculated as around 12 μs.

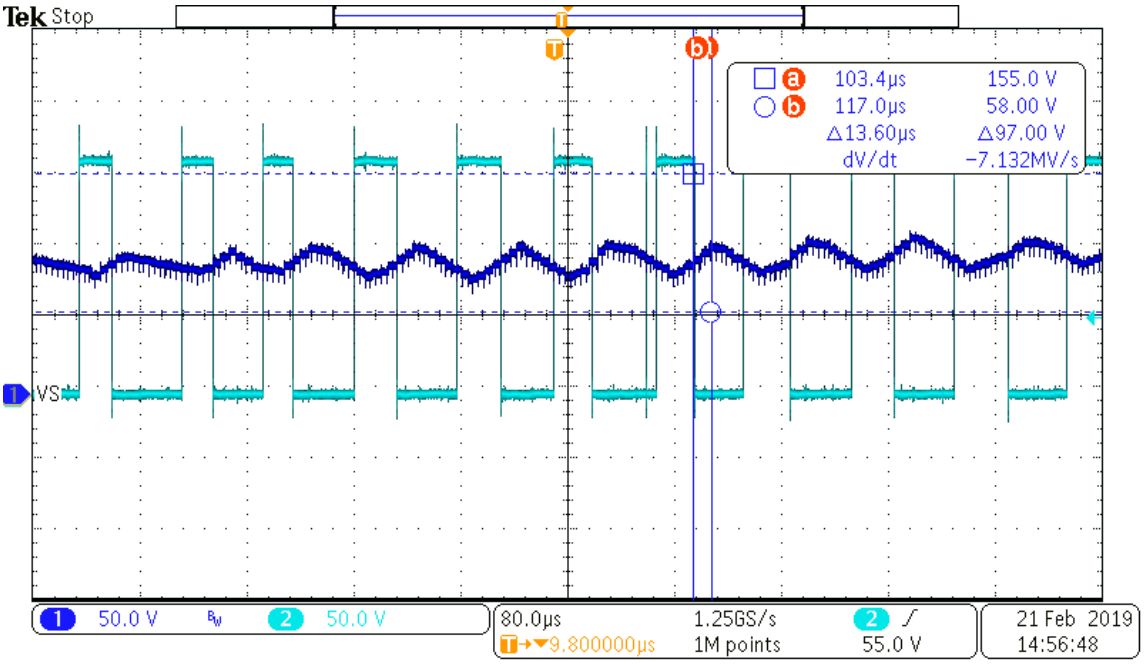

Figure. 4.10: Filter current phase A and gating signal G1 analysis 1.

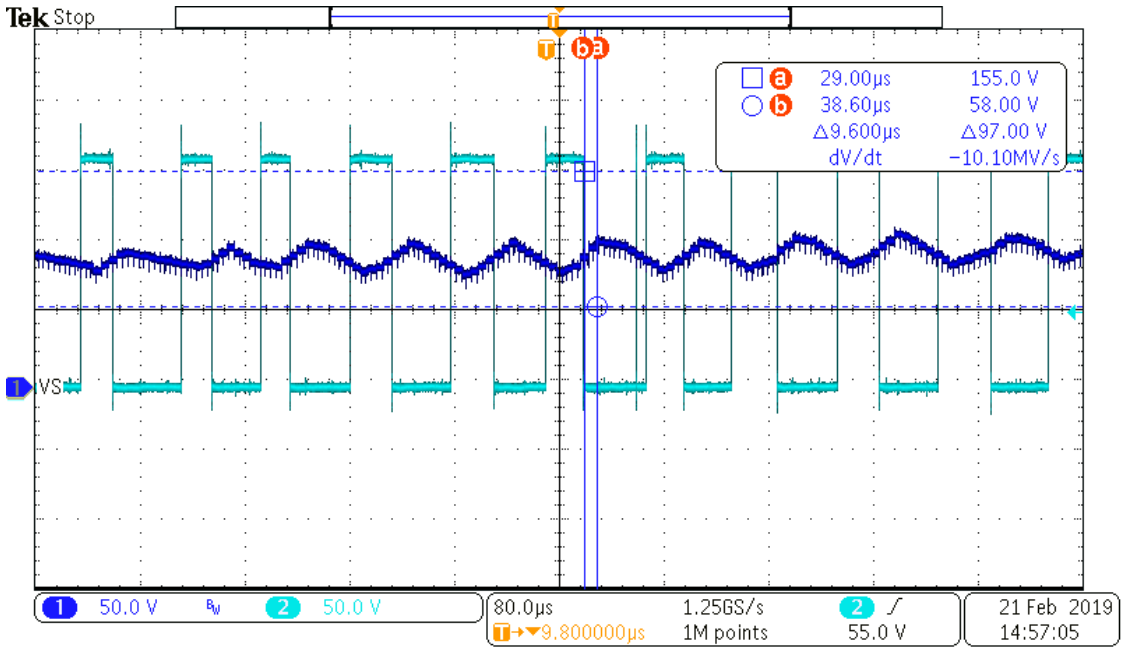

Figure. 4.11: Filter current phase A and gating signal G1 analysis 2.

Chapter 5: Conclusion and Future Work

In this M.Sc. thesis, we have addressed the purpose and procedure of using CHIL simulation in controller implementation and performance evaluation for a high power three-phase APF. One of the main purposes is to explore whether the RT-Box is an effective platform for designing controller hardware under university laboratory condition. Compared with off-line simulation software, the CHIL offers more realistic results and characteristics, which is close to real power hardware in the power system. The use of CHIL also avoids building hardware prototype which saves time and money. For high voltage applications, CHIL is an ideal method to prevent electrical hazard. In this project, the CHIL simulation use two major tools: DSP micro-controller and RT Box real-time simulator. The complete controller was tested without the real power stage. The control system of the APF was implemented in the DSP using CCS. The power circuit was modelled in the RT Box using PLECS simulation tool. The results were observed to evaluate performance of the APF in improving power quality problems such as harmonics, unbalanced currents, and power factor correction. The development of CHIL simulation for the three-phase APF can be divided into three parts: (i) off-line simulation of the system (determine components parameters for both power and control circuit), (ii) controller implementation in DSP micro-controller, and (iii) real-time CHIL testing with RT Box.

Firstly, the entire system was modelled in PLECS under off-line mode includes power circuit and controller. The power circuit consists of a three-phase ac source, a non-linear load, and the APF. The control circuit was built using control modules. In this stage, the parameters for both power and control circuit were determined and tested. The controller parameters were tuned to

achieve optimal performance for the APF. The resultant waveforms and data were collected using scope module to provide a reference for the real-time simulation.

Next, the control system was programmed using C programming software for code verification. Then, the code was compiled to the DSP using CCS. The control of APF includes two parts: filter reference current extraction and current control. Filter reference current extraction uses SRF based technique which has a PLL block to calculated the phase angle θ, a Park's transformation block to transform load currents from a-b-c to d-q coordinates, a moving average filter block that extracts the harmonic component from the load currents, a PI controller block for DC-link capacitor voltage control, and an inverse Park's transformation block brings the load currents back to a-b-c coordinates. On the other hand, the hysteresis current control is employed to generate gating signals, so that force the APF to produce a filter current that equals to the reference filter current calculated from the previous stage. The HCC has the character of fast dynamic control which is suitable for APF application. The reference current extraction part was implemented digitally. Since the HCC is traditionally an analog type control, it was implemented in the analog comparator subsystem module inside the DSP. The analog comparator provides fast and stable control over the filter current. The mathematical relationship between HB and switching frequency was introduced as well. The maximum and minimum switching frequencies were calculated under selected HB. A small-signal analysis was performed to calculate the transfer function of the APF. The parameters of the PI controller for DC-side voltage control were estimated using Bode diagram in MATLAB. The Bode diagram of entire system was plotted. The control system is stable under the selected controller parameters.

Finally, the power circuit was modelled in the real-time simulator RT Box using PLECS under coder mode (allow user to activate real-time simulation). The implemented controller

communicated with the RT Box through a launch-pad interface board. The real-time simulation workspace is well organized without extra wiring. An oscilloscope was connected directly to the analog outputs of the RT Box to observe result waveforms, including source currents before and after compensation, filter currents, source currents Fourier spectrum, DC-link capacitor voltage. The THD of source current was calculated. The switching frequency of the APF was calculated using the Fast Fourier Transform function in the oscilloscope. The real-time simulation switching frequency matches with the theoretical value calculated in Chapter 3. The maximum switching frequency that the system can response was observed through oscilloscope. The maximum frequency reaches 18 kHz, which is limited by the simulation delay of the HCC in real-time HIL. The simulation delay was calculated as $12\mu s$.

Therefore, based on the real-time simulation results, the controller is capable of eliminating current harmonics, compensating unbalanced currents, and improving power factor. The RT Box is running at a step-size of 6 μs. The active power filter controller is able to meet all the design specifications as shown in Chapter 4 using the fully digital simulations on PLECS. Although the CHIL results indicate a slight violation (by 6%), this can be attributed to the delay in the interface between the control hardware and the simulator which averages to about 12 μs as shown in Chapter 4. The delay implies that the hysteresis controller is therefore not able to increase or decrease load current when it first exceeds the switching threshold, a result of which is an artificially higher harmonic content. Nevertheless, the CHIL simulation has the important purpose of demonstrating that the physical control hardware will be able to function in actual applications.

Thus, the research shows that the CHIL simulation is ideal for controller hardware implementation. The RT Box has been evaluated that it is an excellent platform for providing a fast and safe controller develop environment.

There are many future research avenues that can be taken from this thesis. First, after evaluating the performance of the recently developed real-time simulator RT Box, it is interesting to interface the RT Box with the other power system real-time simulator RTDS. For example, the RT Box is designed for high speed switching applications, so high switching frequency devices can be simulated inside the RT Box and low switching frequency power components can be simulated inside the RTDS. The interfacing between the two rea-time simulators will provide a new option for power system real-time simulations. Secondly, it is better to perform the small-signal analysis for all operation point to build a robust controller.

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Appendix A

Controller Implementation Code

```
// Included Files
//
#include "F28x_Project.h"
//
// Function Prototypes
//
#define MPI 3.1415926

void ConfigureADC(void);
void ConfigureDAC(void);
void ConfigureEPWM(void);
void ConfigureEPWM2(void);
void ConfigureEPWM6(void);
void ConfigureEPWM7(void);

void SetupADCEpwm(void);
void InitCMPSS(void);

interrupt void adca1_isr(void);
//
// Variables
//
int Va_sample, Vb_sample, Vc_sample;
int ICA_COMP_HI, ICA_COMP_LOW, ICB_COMP_HI, ICB_COMP_LOW, ICC_COMP_HI, ICC_COMP_LOW;
double Va, Vb, Vc;
double ICA_HI, ICA_LOW, ICB_HI, ICB_LOW, ICC_HI, ICC_LOW;

double h = 0.0001;
double sin120 = 0.8660254;
double cos120 = -0.5;
double theta;
double thetapre = 0.0;
double sinA, sinB, sinC;
int sinA_sample, sinB_sample, sinC_sample;
double cosA, cosB, cosC;
int cosA_sample, cosB_sample, cosC_sample;

double xpre = 0.0;
double ypre = 1.0;
double xcurr, ycurr;              //xpre = sin(theta), ypre = cos(theta)
double w0 = 2.0 * MPI * 50.0;
double w;

double kp_pll = 1000.0;              //kp and ki for pi controller inside of PLL
double ki_pll = 1000.0;
```

```
double PIoutput_pre;
double PIstate_pre = 0.0;
double PIstate_curr;
double epre; //error, input to pi controller
//initializing parameter for DQ transformation
double ILD, ILQ;     //output of DQ transformation
//Variable for Moving Average Filter
double input_ILD_old[100] = { 0 }, input_ILQ_old[100] = { 0 },
       input_ILD_new[100] = { 0 }, input_ILQ_new[100] = { 0 };
double sum_ILD, sum_ILQ;
double MA_ILD_old, MA_ILD_new, MA_ILQ_old, MA_ILQ_new;
int array_size = 0;
double N = 100.0;
int count = 0;
int ind;

//parameters for stage.6
double ILD_AV, ILQ_AV, ICLD, ICQ_REF, ICD_REF, idref_dc;

//parameter of stage 7, PI controller
double Vdc;
double Vdc_REF = 7.0;
int Vdc_sample;
double Kp = 1.0;
double Ki = 10.0;
double ERROR_PI;
double PISTATE_CURR;
double PISTATE_PRE = 0.0;
double PIOUTPUT_PRE;

//parameters for stage 8 Reverse DQ
double ICA_REF, ICB_REF, ICC_REF;
//int ICA_sample, ICB_sample, ICC_sample;
//parameter stage 9
int ILA_sample, ILB_sample, ILC_sample;
double ILA, ILB, ILC;

void main(void) {
    InitSysCtrl();
    InitGpio(); // Skipped for this example

    InitEPwm2Gpio();
    InitEPwm6Gpio();
    InitEPwm7Gpio();
    DINT;

    InitPieCtrl();

    IER = 0x0000;
    IFR = 0x0000;
    InitPieVectTable();
    ConfigureADC();
    ConfigureDAC();
    ConfigureEPWM();
```

```
    ConfigureEPWM2();
    ConfigureEPWM6();
    ConfigureEPWM7();
    SetupADCEpwm();
    InitCMPSS();
    EALLOW;
    PieVectTable.ADCA1_INT = &adca1_isr; //function for ADCA interrupt 1
    EDIS;
    IER |= M_INT1; //Enable group 1 interrupts
    EINT;
    // Enable Global interrupt INTM
    ERTM;
    PieCtrlRegs.PIEIER1.bit.INTx1 = 1;
    EALLOW;
    CpuSysRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    EPwm1Regs.ETSEL.bit.SOCAEN = 1;  //enable SOCA
    EPwm1Regs.TBCTL.bit.CTRMODE = 0; //unfreeze, and enter up count mode
    while (1)
        ;
}
void ConfigureADC(void) {
    EALLOW;
    AdcaRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4
    AdcSetMode(ADC_ADCA, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);

    AdcbRegs.ADCCTL2.bit.PRESCALE = 6; //set ADCCLK divider to /4
    AdcSetMode(ADC_ADCB, ADC_RESOLUTION_12BIT, ADC_SIGNALMODE_SINGLE);
    AdcaRegs.ADCCTL1.bit.INTPULSEPOS = 1;
    AdcbRegs.ADCCTL1.bit.INTPULSEPOS = 1;
    AdcaRegs.ADCCTL1.bit.ADCPWDNZ = 1;
    AdcbRegs.ADCCTL1.bit.ADCPWDNZ = 1;
    DELAY_US(1000);

    EDIS;
}

void ConfigureDAC(void) { // Configure the DAC:
// Initialize the dac
    EALLOW;

    CpuSysRegs.PCLKCR16.bit.DAC_A=1;
    DacaRegs.DACCTL.bit.LOADMODE=0;//load DACVALA from DACVALS on next SYSCLK
    DacaRegs.DACCTL.bit.DACREFSEL=1;//DAC reference slect ADC VREFHI/VREFLO are the
references voltages
    DacaRegs.DACOUTEN.bit.DACOUTEN=1;
    DacaRegs.DACVALS.all=0;

    CpuSysRegs.PCLKCR16.bit.DAC_B = 1;
    DacbRegs.DACCTL.bit.LOADMODE = 0;
    DacbRegs.DACCTL.bit.DACREFSEL = 1;
    DacbRegs.DACOUTEN.bit.DACOUTEN = 1;
    DacbRegs.DACVALS.all = 0;

    CpuSysRegs.PCLKCR16.bit.DAC_C = 1;
```

```
    DaccRegs.DACCTL.bit.LOADMODE = 0;
    DaccRegs.DACCTL.bit.DACREFSEL = 1;
    DaccRegs.DACOUTEN.bit.DACOUTEN = 1;
    DaccRegs.DACVALS.all = 0;
    DELAY_US(2);

    EDIS;
}
void ConfigureEPWM(void) {
    EALLOW;
    EPwm1Regs.ETSEL.bit.SOCAEN = 0;    // Disable SOC on A group
    EPwm1Regs.ETSEL.bit.SOCASEL = 4;   // Select SOC on up-count
    EPwm1Regs.ETPS.bit.SOCAPRD = 1;       // Generate pulse on 1st event
    EPwm1Regs.CMPA.bit.CMPA = 0x0800;     // Set compare A value to 2048 counts
    EPwm1Regs.TBPRD = 0x1000;             // Set period to 4096 counts
    EPwm1Regs.TBCTL.bit.CTRMODE = 3;      // freeze counter
    EDIS;
}
void ConfigureEPWM2(void) {
    EALLOW;
    // Enable PWM
    EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
    //Configure EPWM to run at SYSCLK
    EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV2;// Clock ratio to SYSCLKOUT, EPWMCLK =
SYSCLKOUT/2
    EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;//TBCLK =EPWMCLK/(HSPCLKDIV * CLKDIV)
    EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;// Disable phase loading
    EPwm2Regs.TBPHS.bit.TBPHS = 0x0000;// Phase is 0
    EPwm2Regs.TBCTR = 0x0000;// Clear counter
    EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;//use shadow mode to load compare
register
    EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
    EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

    // Set actions
    EPwm2Regs.AQTSRCSEL.bit.T1SEL = 0x1;// select DCAEVT2 as T1 event source
    EPwm2Regs.AQTSRCSEL.bit.T2SEL = 0x3;// select DCBEVT2 as T2 event source
    EPwm2Regs.AQCTLA2.bit.T1U = AQ_CLEAR;// clear PWM2A upon T1 event
    EPwm2Regs.AQCTLA2.bit.T2U = AQ_SET;// set PWM2A upon T2 event

    // Set digital compare and trip zone
    // determine the input-ouptput logic of the Digital Comparator
    EPwm2Regs.TZDCSEL.bit.DCAEVT2 = TZ_DCAL_HI_DCAH_LOW;//generate DCAEVT2 (current
signal hit upper limit)
    //when DCA low input (trip 4) is high, high input (trip 5) is low
    // be careful how to connect trip input to DC later
    EPwm2Regs.TZDCSEL.bit.DCBEVT2 = TZ_DCBL_HI_DCBH_LOW;//generate DCBEVT2 when DCB
low input is high, high input is low

    //Configure DCA input
    EPwm2Regs.DCTRIPSEL.bit.DCALCOMPSEL = 0x3;// DCAL input is trip 4
    EPwm2Regs.DCTRIPSEL.bit.DCAHCOMPSEL = 0x4;// DCAH input is trip 5
    //Configure DCB input
```

```
    EPwm2Regs.DCTRIPSEL.bit.DCBLCOMPSEL = 0x4;// DCBL input is trip 5
    EPwm2Regs.DCTRIPSEL.bit.DCBHCOMPSEL = 0x3;// DCBH input is trip 4

    //Configure DCA path to be unfiltered & async
    EPwm2Regs.DCACTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm2Regs.DCACTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;
    //Configure DCB path to be unfiltered & async
    EPwm2Regs.DCBCTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm2Regs.DCBCTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;

    // make sure the DC event does no directly change the EPWMxA/B through trip zone
    EPwm2Regs.TZCTL.bit.DCAEVT2 = TZ_NO_CHANGE;//do nothing on DCAEVT2
    EPwm2Regs.TZCTL.bit.DCBEVT2 = TZ_NO_CHANGE;//do nothing on DCABVT2
    EPwm2Regs.TZCTL.bit.TZA = TZ_NO_CHANGE;//do nothing
    EPwm2Regs.TZCTL.bit.TZB = TZ_NO_CHANGE;//do nothing

    // Configure CTRIPH output to ePWM X-BAR logic
    //Configure TRIP4 to be CMPSS1 CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP4MUX0TO15CFG.bit.MUX0 = 0;//select .1 input
    //Configure TRIP5 to be CMPSS1 CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP5MUX0TO15CFG.bit.MUX1 = 0;//select .1
    //Enable TRIP4 Mux for Output
    EPwmXbarRegs.TRIP4MUXENABLE.bit.MUX0 = 1;
    //Enable TRIP5 Mux for Output
    EPwmXbarRegs.TRIP5MUXENABLE.bit.MUX1 = 1;

    EDIS;
}

void ConfigureEPWM6(void) {
    EALLOW;
    // Enable PWM
    EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
    //Configure EPWM to run at SYSCLK
    EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV2;// Clock ratio to SYSCLKOUT, EPWMCLK =
SYSCLKOUT/2
    EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;//TBCLK =EPWMCLK/(HSPCLKDIV * CLKDIV)
    EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE;// Disable phase loading
    EPwm6Regs.TBPHS.bit.TBPHS = 0x0000;// Phase is 0
    EPwm6Regs.TBCTR = 0x0000;// Clear counter
    EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;//use shadow mode to load compare
register
    EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
    EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;

    // Set actions
    EPwm6Regs.AQTSRCSEL.bit.T1SEL = 0x1;// select DCAEVT2 as T1 event source
    EPwm6Regs.AQTSRCSEL.bit.T2SEL = 0x3;// select DCBEVT2 as T2 event source
    EPwm6Regs.AQCTLA2.bit.T1U = AQ_CLEAR;// clear PWM2A upon T1 event
    EPwm6Regs.AQCTLA2.bit.T2U = AQ_SET;// set PWM2A upon T2 event
    EPwm6Regs.TZDCSEL.bit.DCAEVT2 = TZ_DCAL_HI_DCAH_LOW;//generate DCAEVT2 (current
```

```
    EPwm6Regs.TZDCSEL.bit.DCBEVT2 = TZ_DCBL_HI_DCBH_LOW;//generate DCBEVT2 when DCB
low input is high, high input is low

    //Configure DCA input
    EPwm6Regs.DCTRIPSEL.bit.DCALCOMPSEL = 0x6;// DCAL input is trip 7
    EPwm6Regs.DCTRIPSEL.bit.DCAHCOMPSEL = 0x7;// DCAH input is trip 8
    //Configure DCB input
    EPwm6Regs.DCTRIPSEL.bit.DCBLCOMPSEL = 0x7;// DCBL input is trip 8
    EPwm6Regs.DCTRIPSEL.bit.DCBHCOMPSEL = 0x6;// DCBH input is trip 7

    //Configure DCA path to be unfiltered & async
    EPwm6Regs.DCACTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm6Regs.DCACTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;
    //Configure DCB path to be unfiltered & async
    EPwm6Regs.DCBCTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm6Regs.DCBCTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;

    // make sure the DC event does no directly change the EPWMxA/B through trip zone
    EPwm6Regs.TZCTL.bit.DCAEVT2 = TZ_NO_CHANGE;//do nothing on DCAEVT2
    EPwm6Regs.TZCTL.bit.DCBEVT2 = TZ_NO_CHANGE;//do nothing on DCABVT2
    EPwm6Regs.TZCTL.bit.TZA = TZ_NO_CHANGE;//do nothing
    EPwm6Regs.TZCTL.bit.TZB = TZ_NO_CHANGE;//do nothing
    // Configure CTRIPH output to ePWM X-BAR logic
    //Configure TRIP4 to be CMPSS1 CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP7MUX0TO15CFG.bit.MUX2 = 0;//select .1 input
    //Configure TRIP5 to be CMPSS1 CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP8MUX0TO15CFG.bit.MUX3 = 0;//select .1
    //Enable TRIP4 Mux for Output
    EPwmXbarRegs.TRIP7MUXENABLE.bit.MUX2 = 1;
    //Enable TRIP5 Mux for Output
    EPwmXbarRegs.TRIP8MUXENABLE.bit.MUX3 = 1;

    EDIS;
}

void ConfigureEPWM7(void) {
    EALLOW;
    // Enable PWM
    EPwm7Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
    //Configure EPWM to run at SYSCLK
    EPwm7Regs.TBCTL.bit.HSPCLKDIV = TB_DIV2;// Clock ratio to SYSCLKOUT, EPWMCLK =
SYSCLKOUT/2
    EPwm7Regs.TBCTL.bit.CLKDIV = TB_DIV1;//TBCLK =EPWMCLK/(HSPCLKDIV * CLKDIV)
    EPwm7Regs.TBCTL.bit.PHSEN = TB_ENABLE;// Disable phase loading
    EPwm7Regs.TBPHS.bit.TBPHS = 0x0000;// Phase is 0
    EPwm7Regs.TBCTR = 0x0000;// Clear counter
    EPwm7Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;//use shadow mode to load compare
register
    EPwm7Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
    EPwm7Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm7Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
    // Set actions
    EPwm7Regs.AQTSRCSEL.bit.T1SEL = 0x1;// select DCAEVT2 as T1 event source
    EPwm7Regs.AQTSRCSEL.bit.T2SEL = 0x3;// select DCBEVT2 as T2 event source
```

```
    EPwm7Regs.AQCTLA2.bit.T1U = AQ_CLEAR;// clear PWM2A upon T1 event
    EPwm7Regs.AQCTLA2.bit.T2U = AQ_SET;// set PWM2A upon T2 event
    // Set digital compare and trip zone
    // determine the input-ouptput logic of the Digital Comparator
    EPwm7Regs.TZDCSEL.bit.DCAEVT2 = TZ_DCAL_HI_DCAH_LOW;//generate DCAEVT2 (current
signal hit upper limit)
    //when DCA low input (trip 4) is high, high input (trip 5) is low
    // be careful how to connect trip input to DC later
    EPwm7Regs.TZDCSEL.bit.DCBEVT2 = TZ_DCBL_HI_DCBH_LOW;//generate DCBEVT2 when DCB
low input is high, high input is low

    //Configure DCA input
    EPwm7Regs.DCTRIPSEL.bit.DCALCOMPSEL = 0x8;// DCAL input is trip 9
    EPwm7Regs.DCTRIPSEL.bit.DCAHCOMPSEL = 0x9;// DCAH input is trip 10
    //Configure DCB input
    EPwm7Regs.DCTRIPSEL.bit.DCBLCOMPSEL = 0x9;// DCBL input is trip 10
    EPwm7Regs.DCTRIPSEL.bit.DCBHCOMPSEL = 0x8;// DCBH input is trip 9

    //Configure DCA path to be unfiltered & async
    EPwm7Regs.DCACTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm7Regs.DCACTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;
    //Configure DCB path to be unfiltered & async
    EPwm7Regs.DCBCTL.bit.EVT2SRCSEL = DC_EVT2;
    EPwm7Regs.DCBCTL.bit.EVT2FRCSYNCSEL = DC_EVT_ASYNC;

    // make sure the DC event does no directly change the EPWMxA/B through trip zone
    EPwm7Regs.TZCTL.bit.DCAEVT2 = TZ_NO_CHANGE;//do nothing on DCAEVT2
    EPwm7Regs.TZCTL.bit.DCBEVT2 = TZ_NO_CHANGE;//do nothing on DCABVT2
    EPwm7Regs.TZCTL.bit.TZA = TZ_NO_CHANGE;//do nothing
    EPwm7Regs.TZCTL.bit.TZB = TZ_NO_CHANGE;//do nothing

    // Configure CTRIPH output to ePWM X-BAR logic
    //Configure TRIP4 to be CMPSS3 CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP9MUX0TO15CFG.bit.MUX4 = 0;//select .1 input
    //Configure TRIP5 to be CMPSS3 CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP10MUX0TO15CFG.bit.MUX5 = 0;//select .1
    //Enable TRIP4 Mux for Output
    EPwmXbarRegs.TRIP9MUXENABLE.bit.MUX4 = 1;
    //Enable TRIP5 Mux for Output
    EPwmXbarRegs.TRIP10MUXENABLE.bit.MUX5 = 1;

    EDIS;
}
void SetupADCEpwm(void) {
    Uint16 adc_acqps;

    adc_acqps = 14; //

    EALLOW;
//  //*****Va on ADCIN14
    AdcaRegs.ADCSOC0CTL.bit.CHSEL = 0x0E; //SOC0 will convert internal//connection 14
    AdcaRegs.ADCSOC0CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcaRegs.ADCSOC0CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
```

```
//  //*****Vb on ADCIN15
    AdcaRegs.ADCSOC1CTL.bit.CHSEL = 0x0F; //SOC0 will convert internal//connection 15
    AdcaRegs.ADCSOC1CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcaRegs.ADCSOC1CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
//  //*****Vc on ADCINB0
    AdcbRegs.ADCSOC0CTL.bit.CHSEL = 0; //adcbSOC0 will convert internal//connection B0
    AdcbRegs.ADCSOC0CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcbRegs.ADCSOC0CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA
//  //ILA******on ADCINB5
    AdcbRegs.ADCSOC1CTL.bit.CHSEL = 5; //ADCBSOC1 will convert internal//connection B5
    AdcbRegs.ADCSOC1CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcbRegs.ADCSOC1CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA
//  //ILB******on ADCINB4
    AdcbRegs.ADCSOC2CTL.bit.CHSEL = 4; //ADCBSOC2 will convert internal//connection B4
    AdcbRegs.ADCSOC2CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcbRegs.ADCSOC2CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA
    //ICC******on ADCINB2=COMPIN3P
    AdcbRegs.ADCSOC3CTL.bit.CHSEL = 2; //ADCBSOC3 will convert internal//connection B2
    AdcbRegs.ADCSOC3CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcbRegs.ADCSOC3CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA
    //ILC******on ADCINA3
    AdcaRegs.ADCSOC2CTL.bit.CHSEL = 3; //SOC2 will convert internal//connection A3
    AdcaRegs.ADCSOC2CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcaRegs.ADCSOC2CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
    //ICA******on ADCINA2=COMPIN1P
    AdcaRegs.ADCSOC3CTL.bit.CHSEL = 2; //SOC3 will convert internal//connection A2
    AdcaRegs.ADCSOC3CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcaRegs.ADCSOC3CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
    //ICB******on ADCINA4 = COMPIN2P
    AdcaRegs.ADCSOC4CTL.bit.CHSEL = 4; //SOC4 will convert internal//connection A4
    AdcaRegs.ADCSOC4CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcaRegs.ADCSOC4CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
    //VDC******on ADCINB3
    AdcbRegs.ADCSOC5CTL.bit.CHSEL = 3; //SOC5 will convert internal//connection B3
    AdcbRegs.ADCSOC5CTL.bit.ACQPS = adc_acqps; //sample window is 100//SYSCLK cycles
    AdcbRegs.ADCSOC5CTL.bit.TRIGSEL = 5; //trigger on ePWM1 SOCA/C
    AdcaRegs.ADCINTSEL1N2.bit.INT1SEL = 1; //end of SOC0 will set INT1 flag
    AdcaRegs.ADCINTSEL1N2.bit.INT1E = 1;   //enable INT1 flag
    AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //make sure INT1 flag is cleared
    AdcbRegs.ADCINTSEL1N2.bit.INT1SEL = 1; //end of SOC0 will set INT1 flag
    AdcbRegs.ADCINTSEL1N2.bit.INT1E = 1;   //enable INT1 flag
    AdcbRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //make sure INT1 flag is cleared
    EDIS;
}
interrupt void adca1_isr(void) {
    Va_sample = AdcaResultRegs.ADCRESULT0;
    Vb_sample = AdcaResultRegs.ADCRESULT1;
    Vc_sample = AdcbResultRegs.ADCRESULT0;

    ILA_sample = AdcbResultRegs.ADCRESULT1;
    ILB_sample = AdcbResultRegs.ADCRESULT2;
    ILC_sample = AdcaResultRegs.ADCRESULT2;

    Vdc_sample = AdcbResultRegs.ADCRESULT5;
```

```
    Va = ((Va_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 / 11430.95;
    Vb = ((Vb_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 / 11430.95;
    Vc = ((Vc_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 / 11430.95; // * BY 0.0001,
Because PLL won't work if a large number as input
    ILA = ((ILA_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 * 0.001;
    ILB = ((ILB_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 * 0.001;
    ILC = ((ILC_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 * 0.001; //same as PLECS
    Vdc = ((Vdc_sample) * 3.0 / 4096.0 - 1.5) * 10000.0 * 0.001;// same as PLECS model,
IC * 0.001 at PLECS AO end and directly input to CMPSS
    // 3. PLL code
        //initializing the output parameters
        sinA = xpre;
        sinB = xpre*cos120 - ypre*sin120;//sin(theta-120)
        sinC = xpre*cos120 + ypre*sin120;//sin(theta+120)

        cosA = ypre;
        cosB = ypre*cos120 + xpre*sin120;//cos(theta-120)
        cosC = ypre*cos120 - xpre*sin120;//cos(theta+120)

        epre = -(Va*sinA + Vb*sinB + Vc*sinC);
        PIstate_curr = PIstate_pre + h*epre;
        PIoutput_pre = kp_pll*epre + ki_pll*PIstate_pre;

        w = w0 + PIoutput_pre;

        xcurr = xpre + w*h*ypre; //output to test with Va
        ycurr = ypre - w*h*xcurr;
        theta = thetapre + w*h;
        if(theta >= 2.0*MPI){
            theta = 0.0;
            xcurr = 0.0;
            ycurr = 1.0;
        }

        xpre = xcurr;
        ypre = ycurr;
        PIstate_pre = PIstate_curr;
        thetapre = theta;
        // 4. DQ transformation
        ILD = 2.0/3.0*(cosA*ILA + cosB*ILB + cosC*ILC);
        ILQ = -2.0/3.0*(sinA*ILA + sinB*ILB + sinC*ILC);

        // 5. Moving Average Calculation, this MA should calculate the average of
every 100 samples from the ADC.

        if(count<100){

            input_ILD_old[array_size] = ILD;//save the first 100 data to first array
            input_ILQ_old[array_size] = ILQ;

            sum_ILD = sum_ILD + ILD;//take sum of iLd for each cycle
            sum_ILQ = sum_ILQ + ILQ;
```

```
            MA_ILD_old = sum_ILD/array_size;//calculate MA for each cycle
            MA_ILQ_old = sum_ILQ/array_size;

            array_size++;
            count++;
        }

        if(count>=100){//MA calculation when count is higher than 100
            array_size = 0;//reset array size for new array

            while(array_size < 99){
                input_ILD_new[array_size] = input_ILD_old[array_size + 1];
                input_ILQ_new[array_size] = input_ILQ_old[array_size + 1];//Move the
old array to new array,example: old "1" to new "0".
                array_size++;
                }

                input_ILD_new[99] = ILD;
                input_ILQ_new[99] = ILQ;

            MA_ILD_new = MA_ILD_old + ILD/N - (input_ILD_old[0])/N;
            MA_ILQ_new = MA_ILQ_old + ILQ/N - (input_ILQ_old[0])/N;

            MA_ILD_old = MA_ILD_new;
            MA_ILQ_old = MA_ILQ_new;

            ind=0;
            while (ind<100) {//replace the old array with new array
                input_ILD_old[ind] = input_ILD_new[ind];
                input_ILQ_old[ind] = input_ILQ_new[ind];
                ind++;
            }
        }

        //6.1 and 6.2 Calculation of ICLD and ILQ References
        ILD_AV = MA_ILD_new;
        ILQ_AV = MA_ILQ_new;

        ICLD = ILD - ILD_AV;
        ICQ_REF = ILQ - ILQ_AV;

        //7. PI DC voltage control
        ERROR_PI = Vdc - Vdc_REF;
        PISTATE_CURR = PISTATE_PRE + h*ERROR_PI;
        PIOUTPUT_PRE = Kp*ERROR_PI + Ki*PISTATE_PRE;
        idref_dc = PIOUTPUT_PRE;

        //6.3 Calculation of ICD_REF
        ICD_REF = ICLD + idref_dc;

        PISTATE_PRE = PISTATE_CURR; //////////////ADDED ON APRIL 19.2018

        //8. Reverse DQ Transformation
        ICA_REF = ICD_REF*cosA - ICQ_REF*sinA;
```

```
        ICB_REF = ICD_REF*cosB - ICQ_REF*sinB;
        ICC_REF = ICD_REF*cosC - ICQ_REF*sinC;

        ICA_HI = ICA_REF + 0.0002;
        ICA_LOW = ICA_REF - 0.0002;
        ICB_HI = ICB_REF + 0.0002;
        ICB_LOW = ICB_REF - 0.0002;
        ICC_HI = ICC_REF + 0.0002;
        ICC_LOW = ICC_REF - 0.0002;

        ICA_COMP_HI = (ICA_HI * 0.1 + 1.5) * 4096.0 / 3.3;
        ICA_COMP_LOW = (ICA_LOW * 0.1 + 1.5) * 4096.0 / 3.3;
        ICB_COMP_HI = (ICB_HI * 0.1 + 1.5) * 4096.0 / 3.3;
        ICB_COMP_LOW = (ICB_LOW * 0.1 + 1.5) * 4096.0 / 3.3;
        ICC_COMP_HI = (ICC_HI * 0.1 + 1.5) * 4096.0 / 3.3;
        ICC_COMP_LOW   =   (ICC_LOW   *   0.1   +   1.5)   *   4096.0   /   3.3;//VDAC   =
DACxVALA*DACREF/4096, where the DACREF = 3.3v


        //Update of CMPSS DACH and DCAL value
        //High comparator get upper limit, so its output is normally low
        Cmpss1Regs.DACHVALS.bit.DACVAL = ICA_COMP_HI;
        //Low comparator get lower limit, so its output is normally high
        Cmpss1Regs.DACLVALS.bit.DACVAL = ICA_COMP_LOW;

        //High comparator get upper limit, so its output is normally low
        Cmpss2Regs.DACHVALS.bit.DACVAL = ICB_COMP_HI;
        //Low comparator get lower limit, so its output is normally high
        Cmpss2Regs.DACLVALS.bit.DACVAL = ICB_COMP_LOW;

        //High comparator get upper limit, so its output is normally low
        Cmpss3Regs.DACHVALS.bit.DACVAL = ICC_COMP_HI;
        //Low comparator get lower limit, so its output is normally high
        Cmpss3Regs.DACLVALS.bit.DACVAL = ICC_COMP_LOW;

        //DAC OUTPUT
        cosA_sample = ((ICB_REF*0.01+1.5)*4095.0/3.0);
        //cosB_sample = ((*0.1 + 1.5)*4095.0/3.0);
        //cosC_sample = ((IC*0.1+1.5)*4095.0/3.0);
        DacaRegs.DACVALS.all = cosA_sample;
        DacbRegs.DACVALS.all = ICB_REF;
        DaccRegs.DACVALS.all = ICC_COMP_HI;
        DELAY_US(2);

    AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 flag
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}

void InitCMPSS(void) {
    EALLOW;
    //Enable CMPSS
    Cmpss1Regs.COMPCTL.bit.COMPDACE = 0x1;
    //NEG signal of High comparator comes from DAC
    Cmpss1Regs.COMPCTL.bit.COMPHSOURCE = 0x0;
```

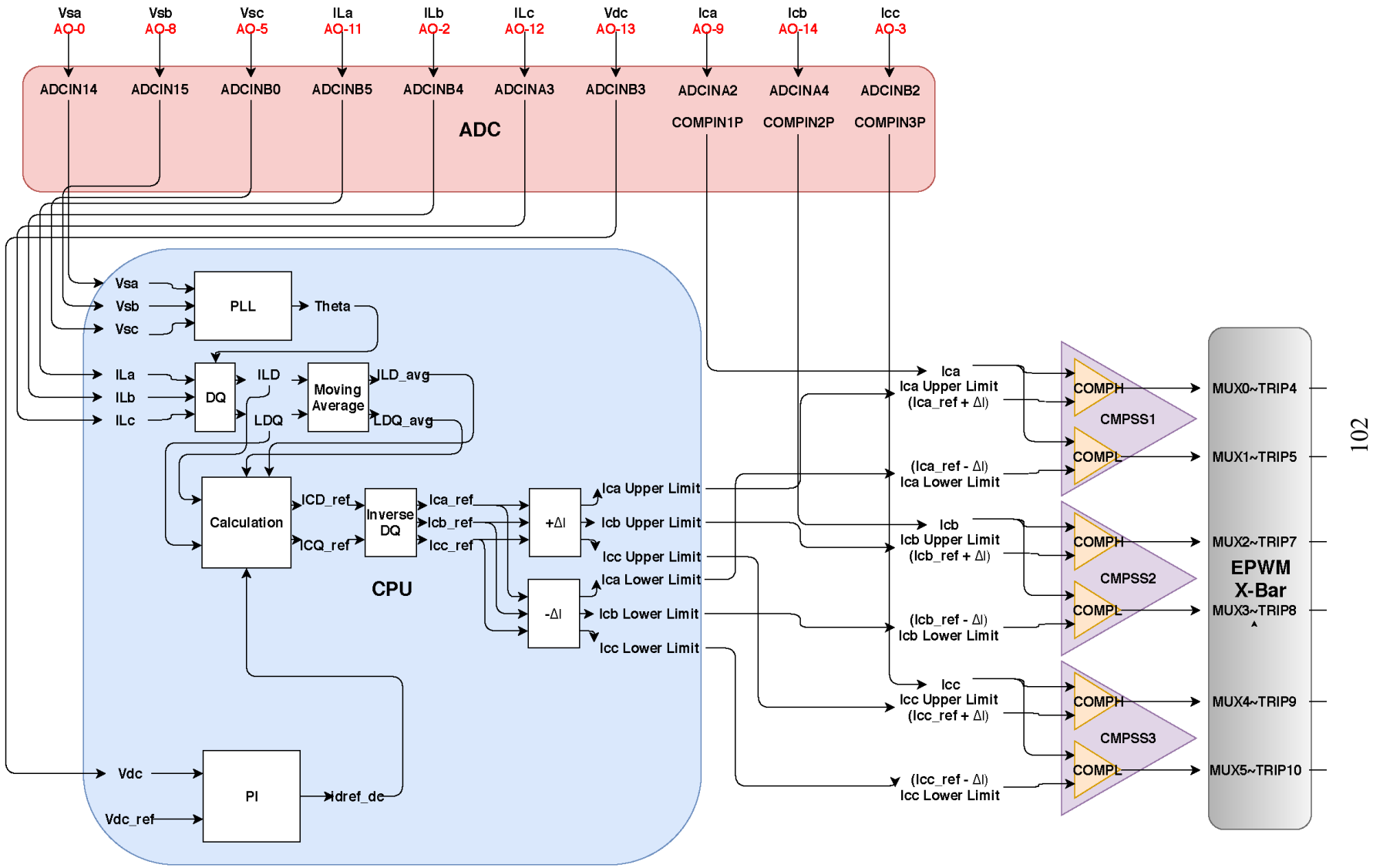
```
    //NEG signal of Low comparator comes from DAC
    Cmpss1Regs.COMPCTL.bit.COMPLSOURCE = 0x0;
    //Use VDDA as the reference for DAC
    Cmpss1Regs.COMPDACCTL.bit.SELREF = 0x0;
    // Load DACxVALA from its shadow registor (not the ramp generator)
    Cmpss1Regs.COMPDACCTL.bit.DACSOURCE = 0x0;
    // Load DACxVALA immediately after loading its shadow registor
    Cmpss1Regs.COMPDACCTL.bit.SWLOADSEL = 0x0;
    //Set DAC voltage level
    //High comparator get upper limit, so its output is normally low
    Cmpss1Regs.DACHVALS.bit.DACVAL = ICA_COMP_HI;
    //Low comparator get lower limit, so its output is normally high
    Cmpss1Regs.DACLVALS.bit.DACVAL = ICA_COMP_LOW;
    // invert Low comparator
    Cmpss1Regs.COMPCTL.bit.COMPLINV = 0x1;
    //do not invert High comparator signal
    Cmpss1Regs.COMPCTL.bit.COMPHINV = 0x0;
    // Configure Digital Filter

// Configure compare result output path
    //Asynch output feeds CTRIPH and CTRIPL
    Cmpss1Regs.COMPCTL.bit.CTRIPHSEL = 0x0;
    Cmpss1Regs.COMPCTL.bit.CTRIPLSEL = 0x0;
    //Asynch output feeds CTRIPOUTH and CTRIPOUTL

// Configure CTRIPH output to ePWM X-BAR logic
    //Configure TRIP4 to be CMPSS1 CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP4MUX0TO15CFG.bit.MUX0 = 0; //select .1 input
    //Configure TRIP5 to be CMPSS1 CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP5MUX0TO15CFG.bit.MUX1 = 0; //select .1
    //Enable TRIP4 Mux for Output
    EPwmXbarRegs.TRIP4MUXENABLE.bit.MUX0 = 1;
    //Enable TRIP5 Mux for Output
    EPwmXbarRegs.TRIP5MUXENABLE.bit.MUX1 = 1;

    //************CMPSS2************************

    Cmpss2Regs.COMPCTL.bit.COMPDACE = 0x1;
    //NEG signal of High comparator comes from DAC
    Cmpss2Regs.COMPCTL.bit.COMPHSOURCE = 0x0;
    //NEG signal of Low comparator comes from DAC
    Cmpss2Regs.COMPCTL.bit.COMPLSOURCE = 0x0;
    //Use VDDA as the reference for DAC
    Cmpss2Regs.COMPDACCTL.bit.SELREF = 0x0;
    // Load DACxVALA from its shadow registor (not the ramp generator)
    Cmpss2Regs.COMPDACCTL.bit.DACSOURCE = 0x0;
    // Load DACxVALA immediately after loading its shadow registor
    Cmpss2Regs.COMPDACCTL.bit.SWLOADSEL = 0x0;
    //Set DAC voltage level
    //High comparator get upper limit, so its output is normally low
    Cmpss2Regs.DACHVALS.bit.DACVAL = ICB_COMP_HI;
    //Low comparator get lower limit, so its output is normally high
    Cmpss2Regs.DACLVALS.bit.DACVAL = ICB_COMP_LOW;
```

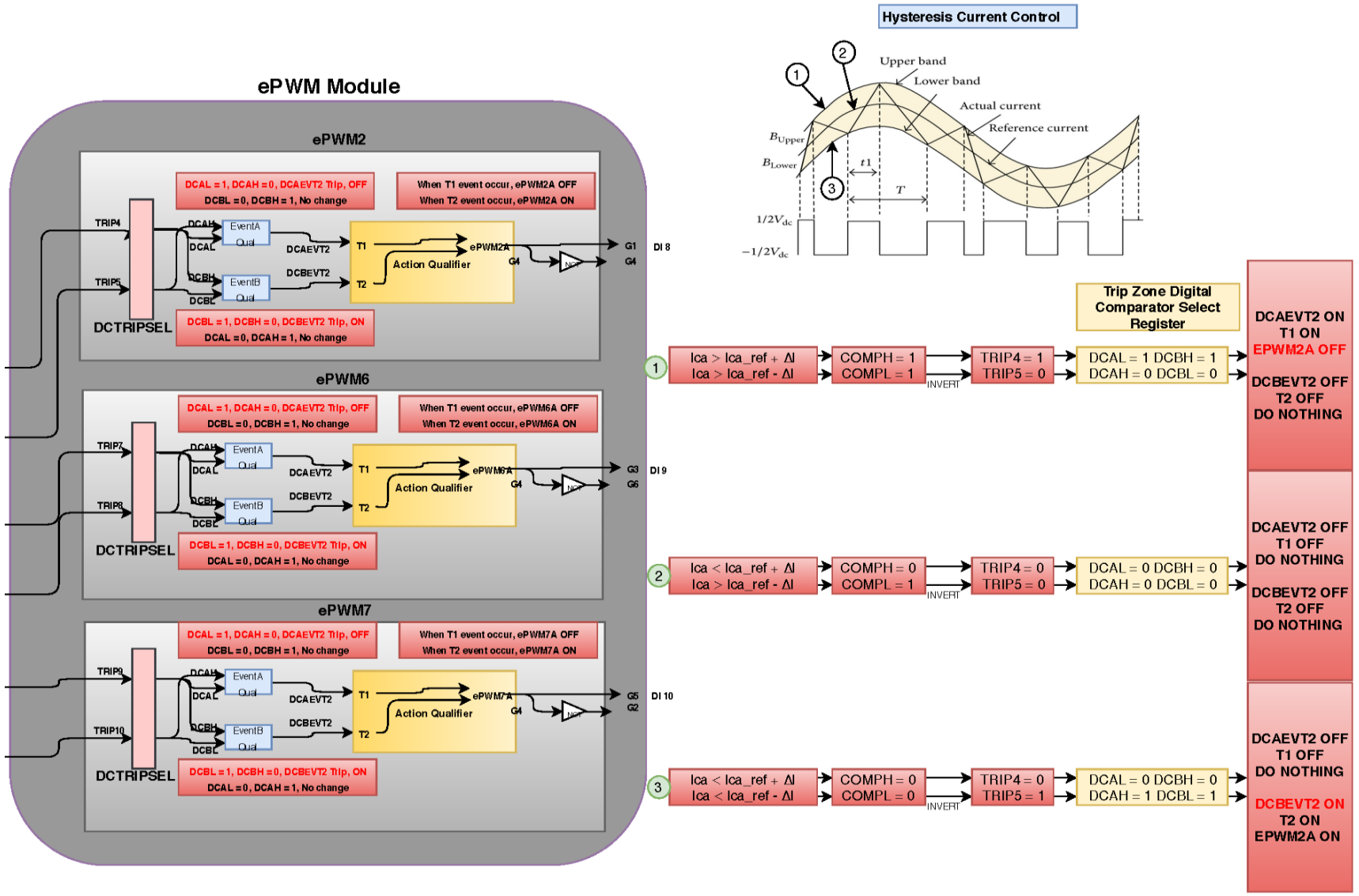
```
    //comment: invert Low comparator OUTPUT signal since we use high to trigger PWM
event
    //Do invert Low comparator
    Cmpss2Regs.COMPCTL.bit.COMPLINV = 0x1;
    //do not invert High comparator signal
    Cmpss2Regs.COMPCTL.bit.COMPHINV = 0x0;
    // Configure Digital Filter

    // Configure compare result output path
    //Asynch output feeds CTRIPH and CTRIPL
    Cmpss2Regs.COMPCTL.bit.CTRIPHSEL = 0x0;
    Cmpss2Regs.COMPCTL.bit.CTRIPLSEL = 0x0;

    // Configure CTRIPH output to ePWM X-BAR logic
    //Configure TRIP7 to be CMPSS2.CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP7MUX0TO15CFG.bit.MUX2 = 0; //select .1 input
    //Configure TRIP8 to be CMPSS2.CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP8MUX0TO15CFG.bit.MUX3 = 0; //select .1
    //Enable TRIP7 Mux for Output
    EPwmXbarRegs.TRIP7MUXENABLE.bit.MUX2 = 1;
    //Enable TRIP8 Mux for Output
    EPwmXbarRegs.TRIP8MUXENABLE.bit.MUX3 = 1;

    //***********CMPSS3**********************

    Cmpss3Regs.COMPCTL.bit.COMPDACE = 0x1;
    //NEG signal of High comparator comes from DAC
    Cmpss3Regs.COMPCTL.bit.COMPHSOURCE = 0x0;
    //NEG signal of Low comparator comes from DAC
    Cmpss3Regs.COMPCTL.bit.COMPLSOURCE = 0x0;
    //Use VDDA as the reference for DAC
    Cmpss3Regs.COMPDACCTL.bit.SELREF = 0x0;
    // Load DACxVALA from its shadow registor (not the ramp generator)
    Cmpss3Regs.COMPDACCTL.bit.DACSOURCE = 0x0;
    // Load DACxVALA immediately after loading its shadow registor
    Cmpss3Regs.COMPDACCTL.bit.SWLOADSEL = 0x0;
    //Set DAC voltage level
    //High comparator get upper limit, so its output is normally low
    Cmpss3Regs.DACHVALS.bit.DACVAL = ICC_COMP_HI;
    //Low comparator get lower limit, so its output is normally high
    Cmpss3Regs.DACLVALS.bit.DACVAL = ICC_COMP_LOW;
    //Do invert Low comparator
    Cmpss3Regs.COMPCTL.bit.COMPLINV = 0x1;
    //do not invert High comparator signal
    Cmpss3Regs.COMPCTL.bit.COMPHINV = 0x0;
    // Configure Digital Filter


    // Configure compare result output path
    //Asynch output feeds CTRIPH and CTRIPL
    Cmpss3Regs.COMPCTL.bit.CTRIPHSEL = 0x0;
    Cmpss3Regs.COMPCTL.bit.CTRIPLSEL = 0x0;
```

```
    // Configure CTRIPH output to ePWM X-BAR logic Table 7-2. ePWM X-BAR ,ux
Configuration Table
    //Configure TRIP9 to be CMPSS3.CTRIPH (select MUX0.1)
    EPwmXbarRegs.TRIP9MUX0TO15CFG.bit.MUX4 = 0; //select .1 input
    //Configure TRIP10 to be CMPSS3.CTRIPL (select MUX1.1)
    EPwmXbarRegs.TRIP10MUX0TO15CFG.bit.MUX5 = 0; //select .1
    //Enable TRIP9 Mux for Output
    EPwmXbarRegs.TRIP9MUXENABLE.bit.MUX4 = 1;
    //Enable TRIP10 Mux for Output
    EPwmXbarRegs.TRIP10MUXENABLE.bit.MUX5 = 1;

    EDIS;
}
```

Appendix B

Control System Implementation Flowchart


Vsa
AO-0
Vsb
AO-8
Vsc
AO-5
ILa
AO-11
ILb
AO-2
ILc
AO-12
Vdc
AO-13
Ica
AO-9
Icb
AO-14
Icc
AO-3
ADCIN14
ADCIN15
ADCINB0
ADCINB5
ADCINB4
ADCINA3
ADCINB3
ADCINA2
ADCINA4
ADCINB2
COMPIN1P
COMPIN2P
COMPIN3P
ADC
Vsa
Vsb
Vsc
PLL
Theta
ILa
ILb
ILc
DQ
ILD
LDQ
Moving Average
ILD_avg
LDQ_avg
Calculation
ICD_ref
ICQ_ref
Inverse DQ
Ica_ref
Icb_ref
Icc_ref
+ΔI
-ΔI
Ica Upper Limit
Icb Upper Limit
Icc Upper Limit
Ica Lower Limit
Icb Lower Limit
Icc Lower Limit
CPU
Vdc
Vdc_ref
PI
idref_dc
Ica
Ica Upper Limit
(Ica_ref + ΔI)
(Ica_ref - ΔI)
Ica Lower Limit
Icb
Icb Upper Limit
(Icb_ref + ΔI)
(Icb_ref - ΔI)
Icb Lower Limit
Icc
Icc Upper Limit
(Icc_ref + ΔI)
(Icc_ref - ΔI)
Icc Lower Limit
COMPH
COMPL
CMPSS1
CMPSS2
CMPSS3
MUX0~TRIP4
MUX1~TRIP5
MUX2~TRIP7
MUX3~TRIP8
MUX4~TRIP9
MUX5~TRIP10
EPWM
X-Bar


ePWM Module
ePWM2
DCAL = 1, DCAH = 0, DCAEVT2 Trip, OFF
DCBL = 0, DCBH = 1, No change
When T1 event occur, ePWM2A OFF
When T2 event occur, ePWM2A ON
TRIP4
TRIP5
DCTRIPSEL
EventA Qual
EventB Qual
DCAEVT2
DCBEVT2
Action Qualifier
ePWM2A
G1
G4
DCBL = 1, DCBH = 0, DCBEVT2 Trip, ON
DCAL = 0, DCAH = 1, No change
ePWM6
DCAL = 1, DCAH = 0, DCAEVT2 Trip, OFF
DCBL = 0, DCBH = 1, No change
When T1 event occur, ePWM6A OFF
When T2 event occur, ePWM6A ON
TRIP7
TRIP8
ePWM6A
G3
G6
DCBL = 1, DCBH = 0, DCBEVT2 Trip, ON
DCAL = 0, DCAH = 1, No change
ePWM7
DCAL = 1, DCAH = 0, DCAEVT2 Trip, OFF
DCBL = 0, DCBH = 1, No change
When T1 event occur, ePWM7A OFF
When T2 event occur, ePWM7A ON
TRIP9
TRIP10
ePWM7A
G5
G2
DCBL = 1, DCBH = 0, DCBEVT2 Trip, ON
DCAL = 0, DCAH = 1, No change
DI 8
DI 9
DI 10
Hysteresis Current Control
Upper band
Lower band
Actual current
Reference current
B_{Upper}
B_{Lower}
t1
T
$1/2V_{dc}$
$-1/2V_{dc}$
Trip Zone Digital Comparator Select Register
1
Ica > Ica_ref + ΔI
Ica > Ica_ref - ΔI
COMPH = 1
COMPL = 1
INVERT
TRIP4 = 1
TRIP5 = 0
DCAL = 1 DCBH = 1
DCAH = 0 DCBL = 0
DCAEVT2 ON
T1 ON
EPWM2A OFF
DCBEVT2 OFF
T2 OFF
DO NOTHING
2
Ica < Ica_ref + ΔI
Ica > Ica_ref - ΔI
COMPH = 0
COMPL = 1
INVERT
TRIP4 = 0
TRIP5 = 0
DCAL = 0 DCBH = 0
DCAH = 0 DCBL = 0
DCAEVT2 OFF
T1 OFF
DO NOTHING
DCBEVT2 OFF
T2 OFF
DO NOTHING
3
Ica < Ica_ref + ΔI
Ica < Ica_ref - ΔI
COMPH = 0
COMPL = 0
INVERT
TRIP4 = 0
TRIP5 = 1
DCAL = 0 DCBH = 0
DCAH = 1 DCBL = 1
DCAEVT2 OFF
T1 OFF
DO NOTHING
DCBEVT2 ON
T2 ON
EPWM2A ON