

DESIGN OF A NEW THYRISTOR ASSISTED ON LOAD
TAP CHANGER FOR TRANSFORMERS

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presented to the University of Manitoba
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by

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TO MY MOTHER . . .

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ABSTRACT

This report describes design modifications in a reactive type on load tap changer for transformers. Frequent operation of these tap-changers causes pitting of diverter contacts and contamination of oil due to sparking at the contacts. Sparking is caused, essentially, due to current chopping. In the new design, a pair of thyristors, connected in anti-parallel, is included with each diverter contact. These thyristors take over the duty of current making and breaking. Current making and breaking is carried out selectively at current zero thus the root cause for sparking is eliminated. The thyristors are triggered by deriving a signal from the movement of the tap-gear which is motor operated.

The new system is analysed by using a lumped parameter equivalent circuit model. Calculations are made for the worst transient conditions. Results of these calculations are used to dimension the thyristors and design their snubber circuits. Complete firing, monitoring and protection circuits are developed for a prototype. The prototype was successfully tested in the Federal Pioneer Electric plant in Winnipeg.

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CHAPTER 1

INTRODUCTION

1.1 Problem

In a power transmission and distribution system the voltage level at a given bus gets changed due to variation in load conditions. Changes are caused due to reactances of the transmission and distribution lines. The power utility and consumers would, in fact, like the power system to behave ideally, that is - no fluctuations in the voltages should results from the load variations. Theoretically such a system can exist if at each terminal of the lines, infinite sources and sinks of controllable reactive power were to exist. Clearly this suggestion is neither practical nor economical to warrent serious consideration. In practical systems, selected consumers can be assured a nearly constant voltage if the supply transformers are equipped with on load tap changers (OLTC). The function of an OLTC is to effectively change the turns ratio of the connecting transformer. OLTC equipped transformers are widely used by electric utilities in their own transmission system and in a large number of distribution systems.

An OLTC responds to minimise the deviation of the terminal voltage from the desired value. In its operation, in effect, a moving contact connects and electrical terminal to an appropriate tapping on the transformer winding. Each move therefore breaks contact from its original tap and makes to the next. In order to maintain an overall continuity of current, ingenious methods are employed which short the windings between two taps momentarily, through external impedance, until the full current is established from the new contact.

The process of making and breaking currents invariably leads

to sparking. In order to protect and enhance the life of the main contacts, the current making and breaking duty is relegated to auxiliary contacts. Due to repeated operations even the auxiliary contacts get pitted and wear out and, in the process, contaminate the oil.

Federal Pioneer employs a reactor type OLTC. This tap changer is also subject to the arcing conditions and hence requires regular field maintenance.

This project was inspired by a desire to make the OLTC maintenance free. The scope of the project was limited to seek simple design modifications which can be carried out on the existing design and therefore make retrofitting a distinct possibility.

The requirements are set forth very clearly by identifying the following important tasks:

1. Devise methods to eliminate arcing of the OLTC contacts.
2. Suggest design changes which can be incorporated in the existing gear and therefore make retrofitting, of equipment in service, possible.
3. The new design should be such that in the event of failure of the added system the working of OLTC will revert to its original state.
4. Design suitable monitoring, protection and alarm systems to continually supervise the new OLTC.
5. Incorporate an emergency freezing of the tap-changer movement, in the event of a catastrophic failure develops in the OLTC, so that the transformer would continue to supply, albeit degraded, service.

In the new design an anti-parallel pair of thyristors is

incorporated in series with the arcing contacts. The thyristors provide current breaking and making service while the arcing contact merely isolates and makes the circuit.

Chapter 2 describes in detail the working of the existing line of reactor type on load tap changer (OLTC) marketed by Federal Pioneer Electric.

In chapter 3 the proposed new concept is described. It also deals with the preliminary investigations which were carried out in the laboratory to test the feasibility.

Chapter 4 deals with the analytical aspects of the proposed design. It describes the electrical circuit model of the new design and presents the results of theoretical investigations.

Chapter 5 establishes general design criteria and procedure for the new design.

Chapter 6 shows the results of the tests carried out for the prototype development.

Chapter 7 presents conclusions and recommendations.

1.2 Background

The purpose of an on load tap changer is to control the ac line volage within specified limits (normally 5/8th of one percent) under varying load conditions while the transformer or step voltage regulator is in service. This is achieved by changing taps on one of the windings to permit adjustment of the turns ratio of the transformer. A tap changer carries out disconnection and reconnection from one tap to the next without actually interrupting the line current at any instant, or directly short circuiting any part of the winding.

On load tap changers were first manufactured around 1910. These were used on furnace transformers. They consisted of a tap selector and a current limiting resistor. The resistor was introduced in circuit during the instant of transfer. In this arrangement the current was interrupted by the selector switch contacts. These tap-changers could be used only for relatively light duty because interruption of large currents caused strong arcing and led to rapid destruction of the contacts. Soon it became necessary, therefore, to provide the tap changers with diverter switches which carried out the current interruptions.

The modern on load tap changer had its beginning in 1925. Since that time, on load tap changing equipment is applied to power transformers to regulate the secondary voltage and thus to control the flow of the reactive power.

There are various types of tap changers on the market. They are built with their regulation range divided into 8, 16, or 32 steps. The usual range of regulation is ± 10 per cent of the rated line voltage.

1.3 On Load Tap Changer Operation

Although a variety of switching equipments and transformer connections have been used for the purpose of tap changing under load, however, their underlying operating principle remains unchanged. It is described below:

In one type, tap change is made without opening the circuit by using a mid-tapped auto-transformer generally called the preventive auto-transformer. The Block Schematic of such a tap changer is shown in Fig. 1.1(a). The load voltage is the sum of main winding and tapped winding voltage. This load voltage can be varied by varying the tap position illustrated in Fig. 1.1(b). The tap position 3 is altered to position 4 in four steps. Notice during step 2 there is a circulating current flowing through the reactor, and that the load current is never interrupted. Further details are given in the next section.

To move from transformer tap from A to B, as shown in Fig. 1.2 (a), one arm of the reactor makes contact with tap B. During this interval when both A and B are closed on adjacent taps, a circulating current flows through the reactor limited by the impedance in the loop, composed of the tap winding B and auto transformer C. The load current divides equally between the two halves of the transformer. Since currents flow in the opposite directions, a negligible amount of reactance is introduced into the main circuit. Additional internal voltage drop is therefore, primarily resistive due to 50% load current in each half of the auto-transformer winding. With A closed and B open, entire load current flows through one half of the auto-transformer, magnetizing the autotransformer and thereby introducing into the circuit additional reactive voltage drop, this situation however occurs only transiently. It is important that the magnetizing reactance be kept as low as pos-

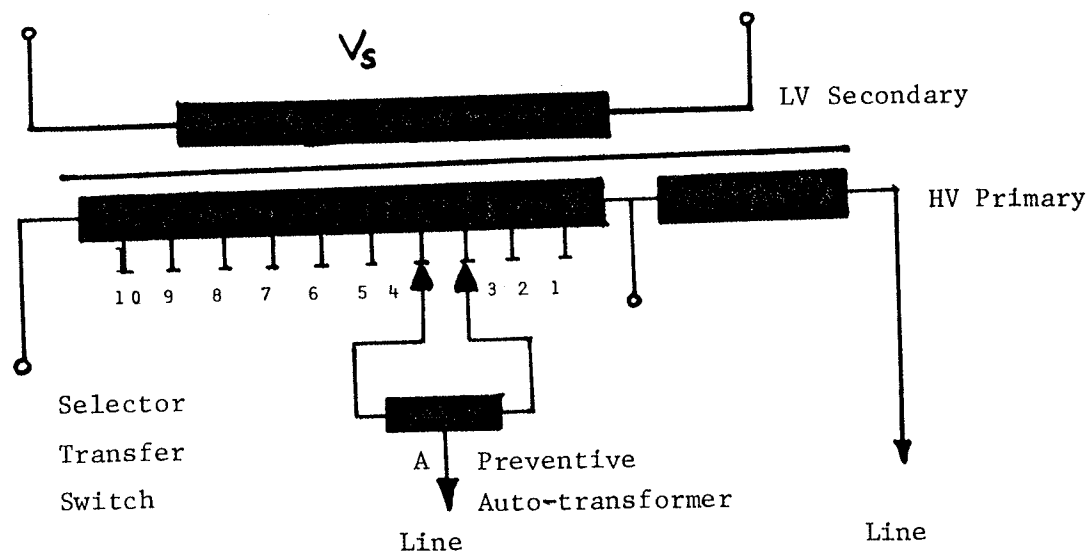


Fig.1.1 a) Schematic Diagram of an On Load Tap Changer

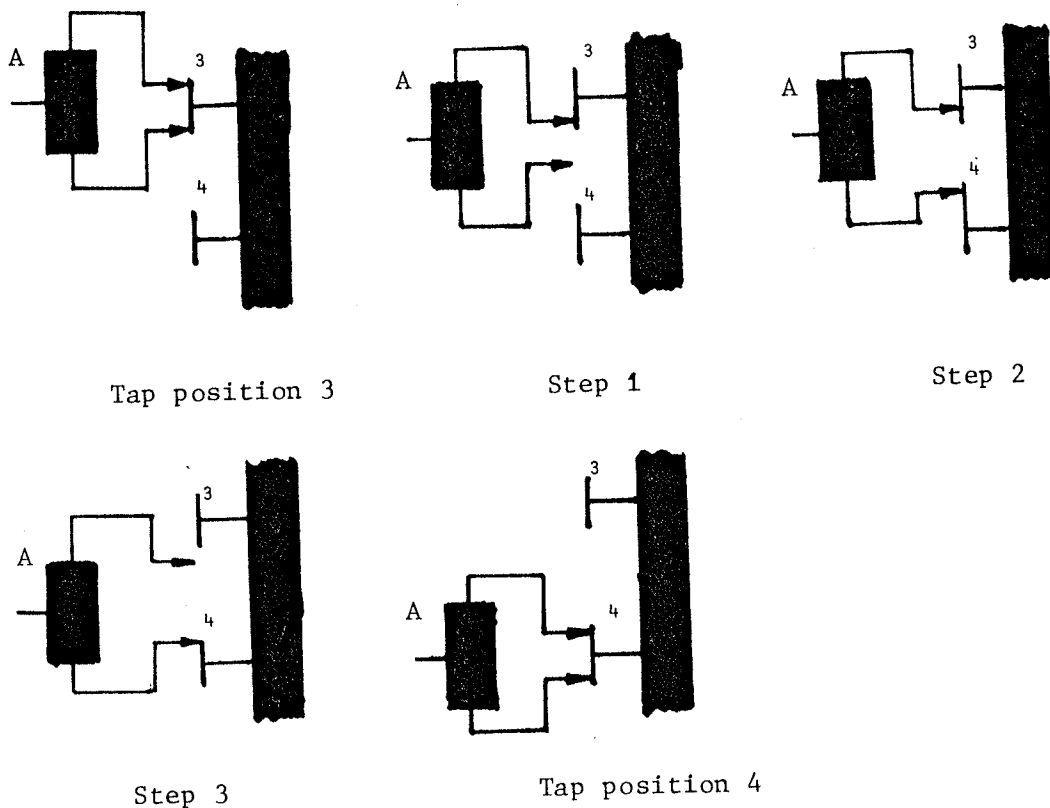


Fig. 1.1 b) Sequence of Steps for tap change from position 3 to 4

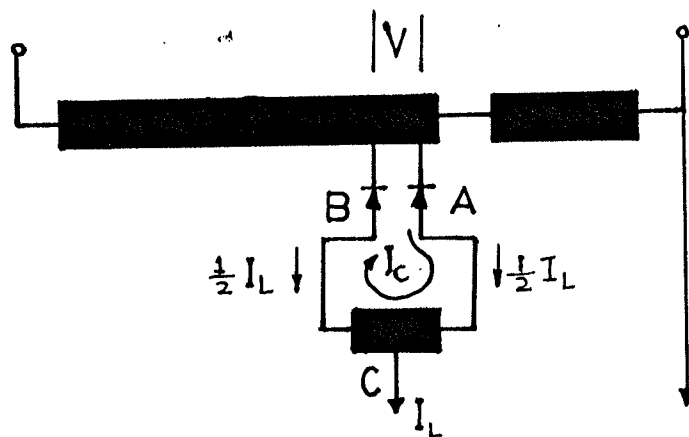
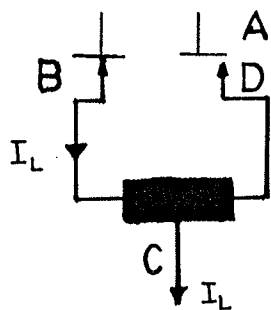


Fig. 1.2 a) Schematic Diagram of OLTC in Bridging Position



Tap change from lower to upper tap

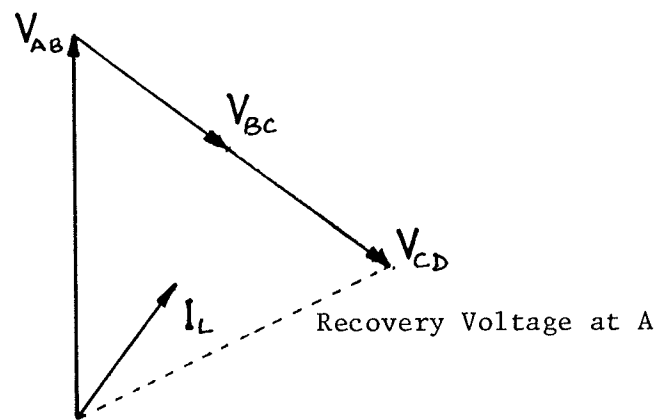


Fig. 1.2 b) Phasor Diagram for Recovery Voltage across switch A at lower Tap Change

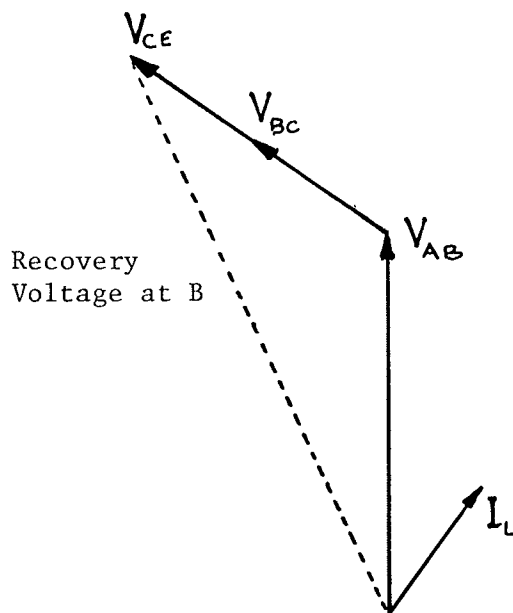
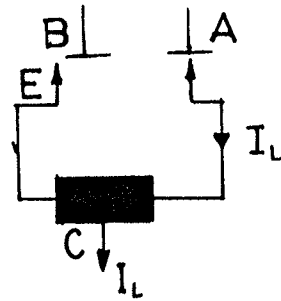


Fig. 1.2 c) Phasor diagram for Recovery Voltage across Switch B at Upper Tap Change

sible to limit the voltage drop and, further, to avoid excessive arcing at the contacts - which are used to break the current during a tap-change. Arcing takes place, because the energy stored ($\frac{1}{2} L i^2$) in the half reactor has to be dissipated when breaking the contact.

To avoid an excessive voltage drop through the autotransformer when one side is open and at the same time to keep the circulating current at a low level when in the bridging position, the auto-transformer is usually designed with an air gap in the magnetic circuit to get a magnetizing current of about 50-60% of the normal full-load current.

Fig. 1.2 shows a phasor diagram depicting various voltage phasors during a tap change, for 50% circulating current and load power factor of 0.8 lagging. Study of these figures shows that when magnetizing reactance of the autotransformer is increased, to reduce the circulating current, then

- 1) The voltage across the full autotransformer winding during tap change increases,
- 2) Recovery voltage increases,
- 3) Voltage fluctuation at the load end increases, and
- 4) Arcing increases.

CHAPTER II

FEDERAL PIONEER ON LOAD TAP CHANGER (FPE OLTC)

2.1 Introduction

Federal Pioneer's on load tap changer is of reactor type and is normally applied to transformers requiring either 16 or 32 tap steps. The tapped winding of the transformer has 9 tap sections with 10 tap leads connected to the tap changer. The tap terminals 2-9 are connected as shown in Fig. 2.1. The end of the tap winding terminals 1 and 10 are connected via a reversing switch to the selector switch contact K. The transformer winding can therefore be connected through the contact K and the reversing switch to either end of the tapping winding. The two possible positions of the tap winding can be described as either a buck position, effectively reducing turns in the transformer winding or boost position which adds turns to the transformer winding.

The selector switch allows a double circuit connection CRI and CR3 to the stationary selector contacts 2-9 and K. The two pairs of moving selector contacts are spaced such that they can be positioned to either fit on a single contact, or bridge two contacts. These positions are called the nonbridging and bridging positions respectively. The tap changer switches from nonbridging to a bridging position or vice versa in a single step. This allows a tap changer to have 16 buck positions and 16 boost positions or in effect 32 tap positions.

The reversing switch is actuated by the movements of the selector switch from the K position to either 2 or 9. Movement from K to 9 puts the reversing switch in position 10, and moving from K to 2 puts the reversing switch in position 1.

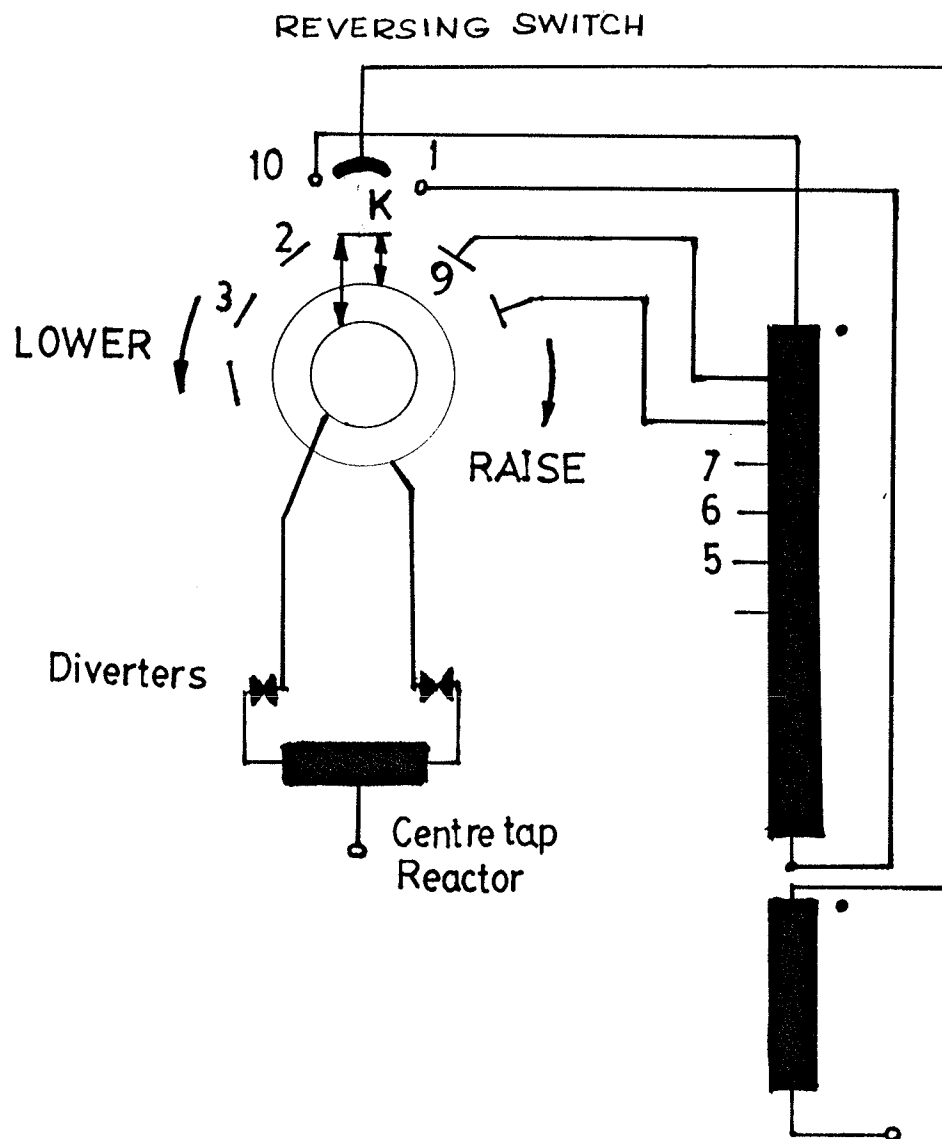


Fig. 2.1 Federal Pioneer On Load Tap Changer Schematic Diagram

In switching from one selector position to another, one of the moving selector contact pairs must be moved between two stationary contacts. Before this contact breaks, or makes, on a fixed contact the appropriate circuit CR1 or CR3 must be interrupted. This is accomplished via a diverter arcing switch which is equipped with a special arcing contact capable of interrupting the main current.

2.2 FPE OLTC Description

The divertors consist of the main contact in parallel with the arcing contact as shown in Fig. 2.2. They are mechanically constructed in such a manner that when contacts are opened the main contact opens first and then the arcing contact. Similarly when closing, the arcing contact closes first and then the main contact. The resistance of the arcing switch is made more than the main switch so that under normal condition the main switch carries the tap current. When diverter is opened during tap change the current is commutated from the main to the arcing contact without any appreciable arcing at the main contact. Then the current is interrupted by arcing contact which causes current chopping resulting in severe arcing and erosion of the arcing contact. The deenergized selector switch then moves to the next tap position. Selector switch is shown in Fig. 2.3 along with diverter and reversing switches in the tap head assembly. When closing, the arcing contact closes first with some pre-arcing and makes the new tap current. The main contact then closes after some delay without any arcing. Arcing contact is made of a tungsten alloy to reduce the erosion to a minimum, however, its life is limited still to 10,000 to 20,000 operations. The sequence of operation for this tap-changer is illustrated in Fig. 2.4(a). An actual recording with existing FPE OLTC in a simulated test is presented in Fig. 2.4(b). It shows the amount

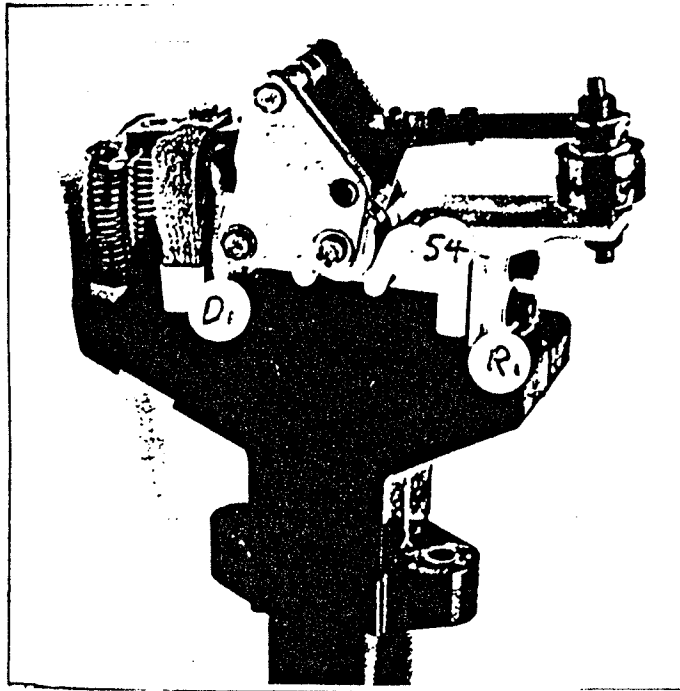


Fig. 2.2 a) Photograph of FPE Diverter Switch in Closed Position

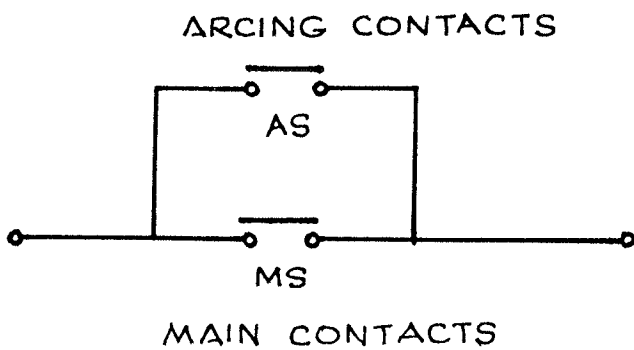
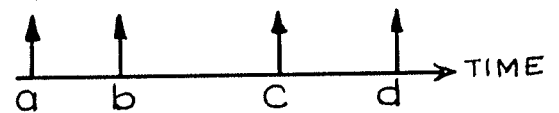


Fig. 2.2 b) Schematic Diagram of FPE Diverter showing the main and arcing contact



- a) Main Contact opens
- b) Arcing Contact opens
- c) Arcing Contact closes
- d) Main Contact closes

Fig. 2.2 c) FPE Diverter - Sequential Functional Diagram

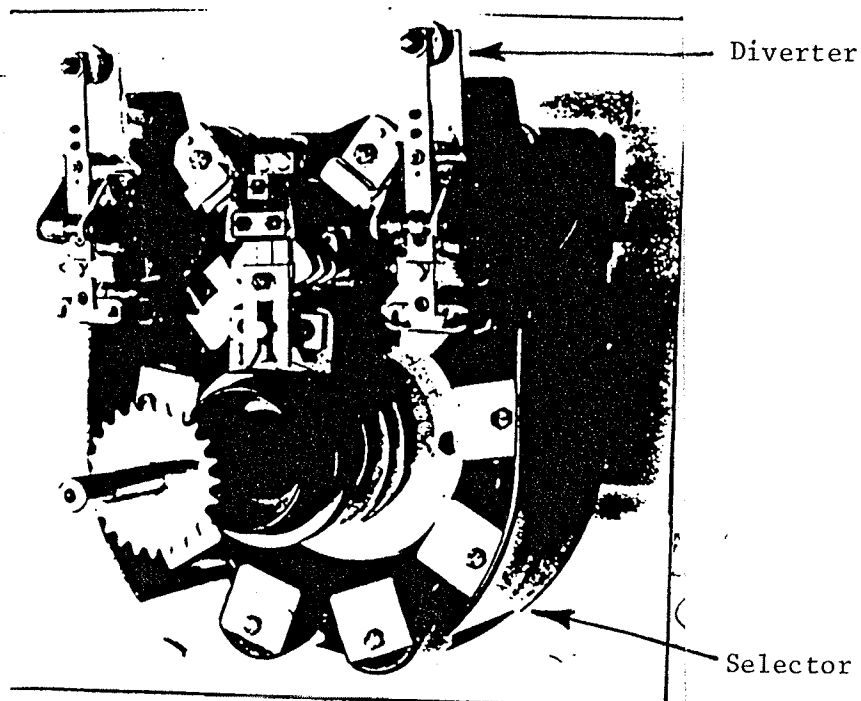
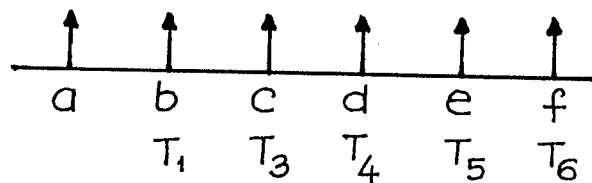


Fig. 2.3 FPE Tap head



- a) Main Contact opens
- b) Arcing Contact opens, T_1 (current is interrupted at T_2)
- c) Selector Switch opens with Existing Tap, T_3
- d) Selector Switch closes with Next Tap, T_4
- e) Arcing Contact closes, T_5
- f) Main Contact closes, T_6

Fig. 2.4 a) Sequence of Operation of FPE Tap Changer

of arcing and pre-arcing at the arcing contact.

Figure 2.4(b) illustrates different time sequence during tap change for arcing contact, voltage across divertors, load voltage and diverter current. At $t = T_1$ the arcing contact opens after the main contact is already open. Observe the voltage across the diverter. Before $t = T_1$, it is zero, because the arcing contact was closed but when it opens an arc is produced and recovery voltage follows. The arc is extinguished at $t = T_2$ and diverter current goes to zero,. In Fig. 2.4(b) observe when the diverter current starts conducting at $t = T_5$ the arcing contact is still open and approaches its closing position at $t = T_6$. This conduction of current is due to 'pre-arc' at the arcing contact and its pre-arc voltage is very low.

The main tank houses three contact head assemblies, six diverter contact assemblies and the main drive mechanism. The driving motor is housed in the control panel along with the relay circuit. Each contact head assembly consists of circular selector switch for 9 taps, reversing switch and two diverter switch assemblies. The main mechanism assembly, which drives the diverter switches consists of a spring in a cylinder, geneva gears and diverter driving cam as shown in Fig. 2.5. The mechanical power is transmitted to the tap shaft by chains.

The selector head and tap shaft are cast accurately in epoxy resin of high dielectric and mechanical strength. The tap head forms a permanent oil-seal between the transformer and tap gear compartments. The selector contacts are capable of 2 million mechanical operations without replacement. This type of connection can withstand 20 times rated current for four seconds on short circuit.

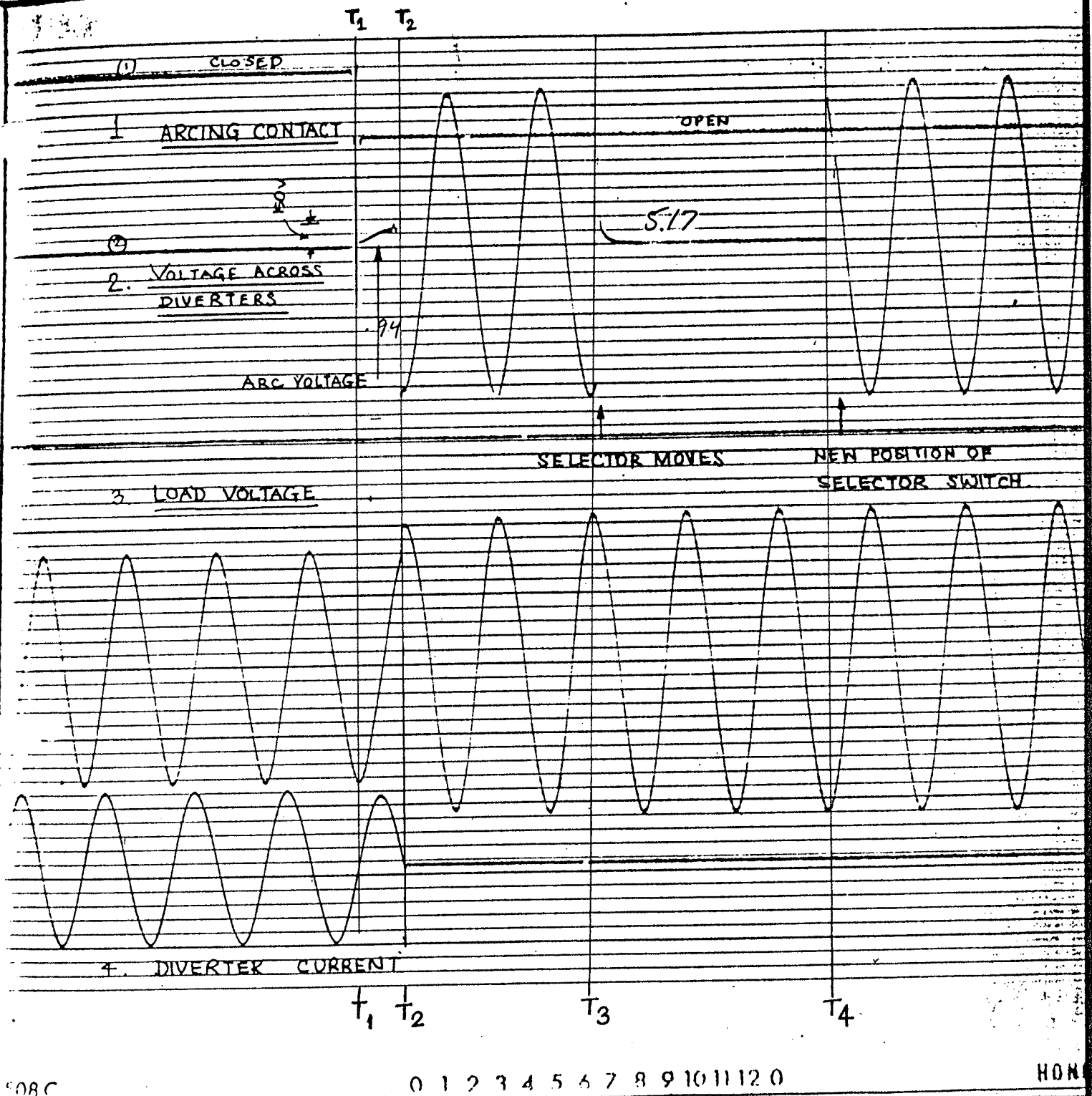


Fig. 2.4 b) Simulated test recordings of FPE Tap Changer

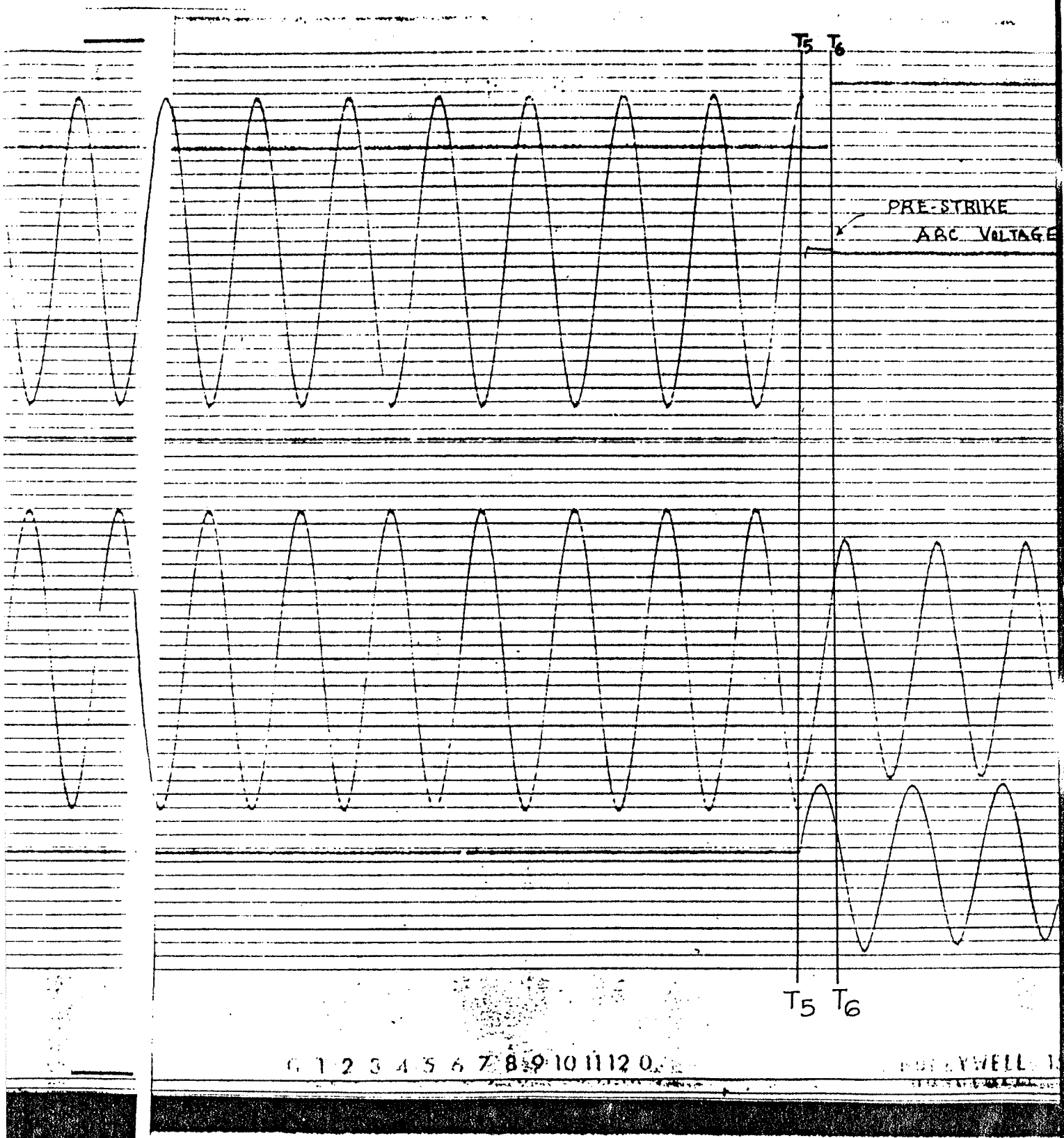


Fig. 2.4 b) Simulated test recording of FPE Tap Changer

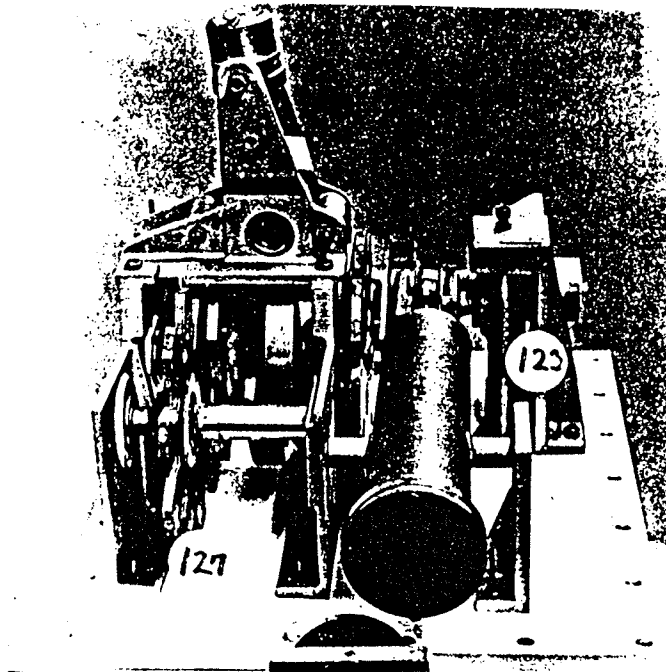


Fig. 2.5 a) FPE Tap Changer mechanism showing springs, gears, cams, etc.

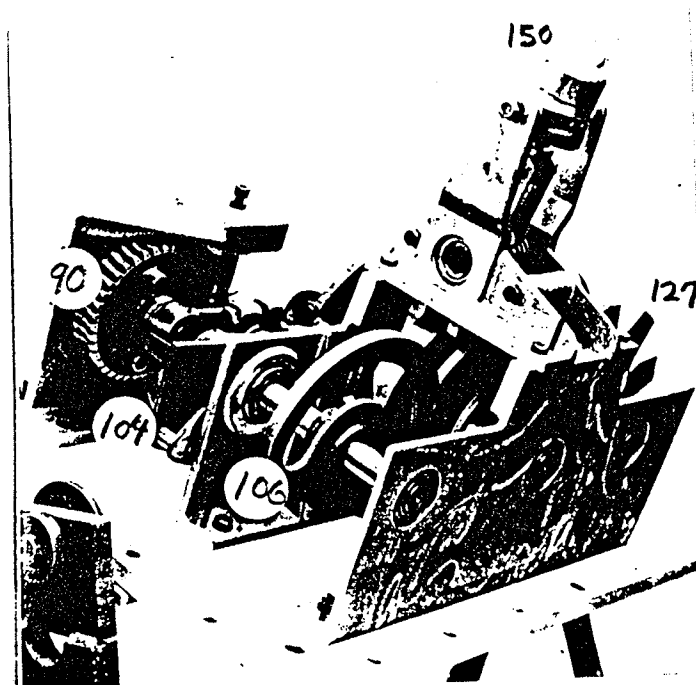


Fig. 2.5 b) Another view of FPE OLTC

2.3 Rating of FPE OLTC

The ratings of Federal Pioneer tap changers are as follows:

1. TC15: 5KV to 15kV for heavy current
2. TC25: 5kV to 25kV
3. TC34: 5kV to 34.5kV with external divertors
4. TC46: 5kV to 46kV with external divertors
5. TCA 15: 5kV to 15kV dry type with vacuum switches.

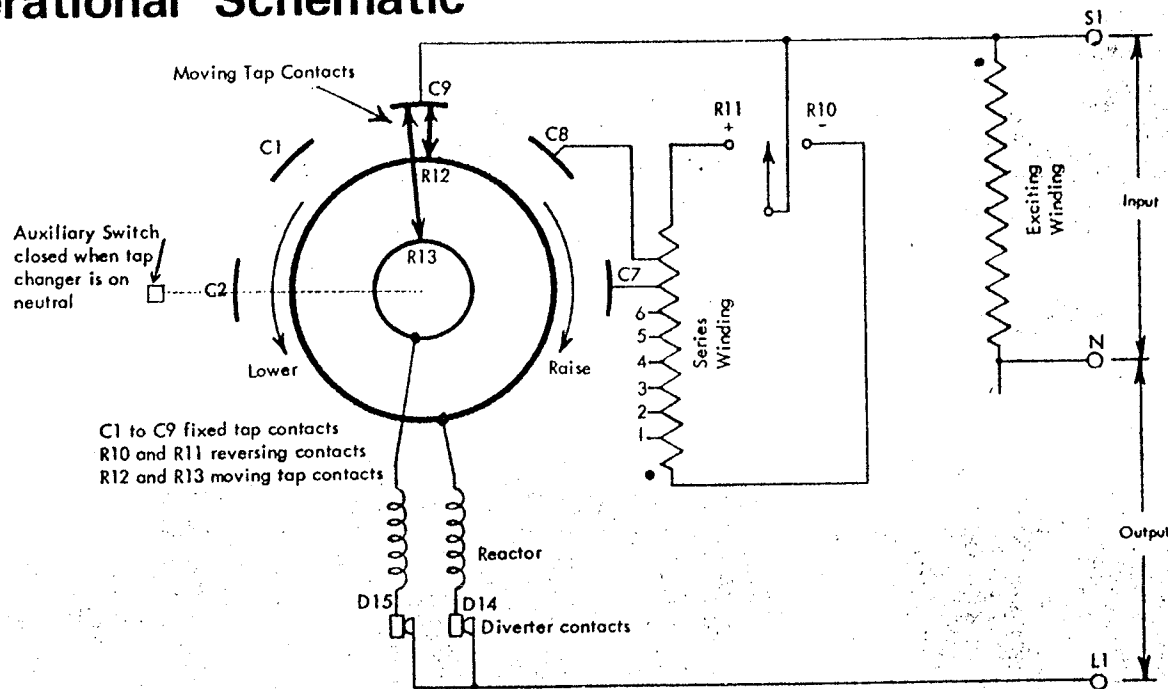
2.4 Operational Schematic of FPE OLTC

Figure 2.6 shows the sequence of steps for a rise or lower operation on the tap changer. The series winding can be either connected for bucking or boosting the exciting winding voltage by a two way reversing switch (R11, R10 in Fig. 2.6). This reduces the number of taps required to half the number without the reversing switch. This tap changer further allows an additional tap position in the bridging position. The voltage under bridging position is average of the connected taps. This reduces the number of actual taps from transformer winding from one-half to one-fourth, making this tap changer economically attractive.

2.5 Control Circuit of FPE OLTC

Figure 2.7 shows the control diagram for the on load tap changer. The control circuit is mounted below the switching compartment. It consists of a drive motor, synchronous timers, solid state relay and other control equipment. The tap changer can operate in two modes: 'auto' and 'manual'. In the 'auto' mode the PT and CT sense the line voltage and current respectively. It then compensates the voltage for the line drop voltage and compares it with a reference voltage. Depending on the error signal between these two voltages the voltage sensing device gives a signal to a timer. The timer prevents tap

Operational Schematic



TYPICAL ARRANGEMENT
Tap changer on neutral, one phase shown

	RAISE	LOWER
NEUTRAL to STEP 1	(a) Diverter D14 opens (b) Reversing switch moves to R11 (+) (c) Moving contacts move to bridge C8-R12 and C9-R13. (d) Diverter D14 closes (e) L1 load is supplied through tap head contacts C8 and C9, which are bridged by the reactors	(a) Diverter D15 opens (b) Reversing switch moves to R10 (-) (c) Moving contacts move to bridge C1-R13 and C9-R12 (d) Diverter D15 closes (e) L1 load is supplied through tap head contacts C1 and C9, which are bridged by the reactors
STEP 1 to STEP 2	(a) Diverter D15 opens (c) Moving contacts move to bridge C8-R12 and C8-R13 (d) Diverter D15 closes (e) L1 load is supplied through tap head contact C8 and paralleled reactors	(a) Diverter D14 opens (c) Moving contacts move to bridge C1-R13 and C1-R12 (d) Diverter D14 closes (e) L1 load is supplied through tap head contact C1 and paralleled reactors

STEPS 2 to 15 SIMILAR

STEP 15 to STEP 16	(a) Diverter D15 opens (c) Moving contacts move to bridge C1-R12 and C1-R13 (d) Diverter D15 closes (e) L1 load is supplied through tap head contact C1 and paralleled reactors (f) Further raise movement is prevented by limit switch (g) Limit Sw. is backed up by mechanical lock and control power "cut-off" contact	(a) Diverter D14 opens (c) Moving contacts move to bridge C8-R13 and C8-R12 (d) Diverter D14 closes (e) L1 load is supplied through tap head contact C8 and paralleled reactors (f) Further lower movement is prevented by limit switch (g) Limit Sw. is backed up by mechanical lock and control power "cut-off" contact
NOTE	If (g) above has not operated, an impulse opposite to that shown above will move tap changer in the opposite direction from any step	

Fig. 2.6 FPE Operational Schematic

changer from hunting by introducing a time delay for the transients in the system to settle down. If signal still persists during this time delay it gives signal to a solid state relay which operates one of the contactors L or R. These contactors L or R provide supply voltage to a single phase induction motor which can rotate in reverse or forward direction respectively. When the motor compresses the main spring completely a limit switch cuts off the motor supply. The energy stored in the main spring moves the whole mechanism through one tap-change i.e., opening of diverters, selector switch moving to new position and the diverter switch closing on a new tap.

2.6 Timing Charts

Experiments were carried out to get the timing charts for the tap sequence illustrated in Fig. 2.7. Two of the six diverters were adjusted to operate simultaneously. The main contact of one of the diverters and arcing contact of the other diverter were insulated. They were connected as shown in Fig. 2.8 to get a plot of full sequence of the tap-changer as shown in Fig. 2.9.

Control Diagram On Load Tap Changing Equipment

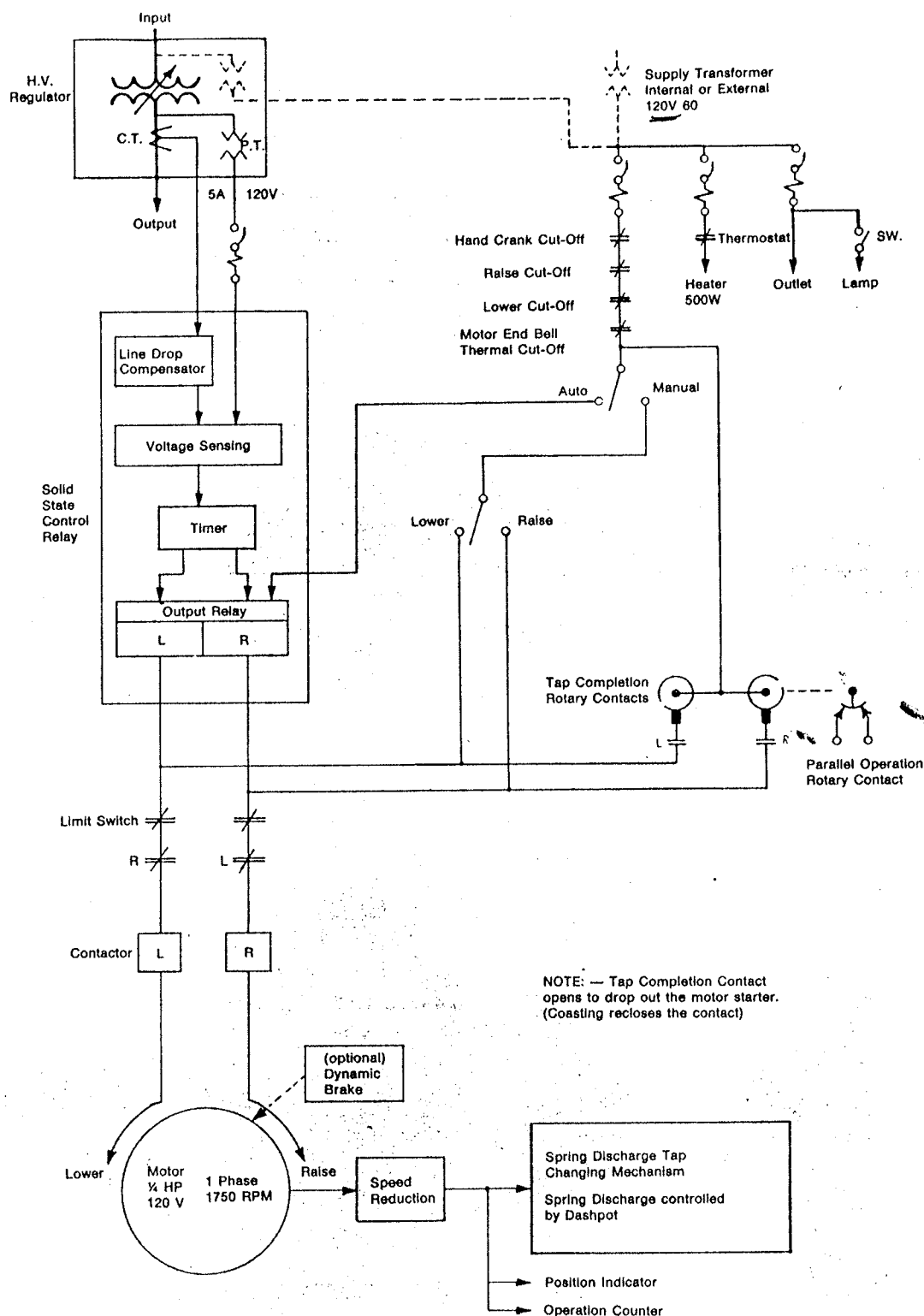


Fig. 2.7 FPE Tap Changer control circuit

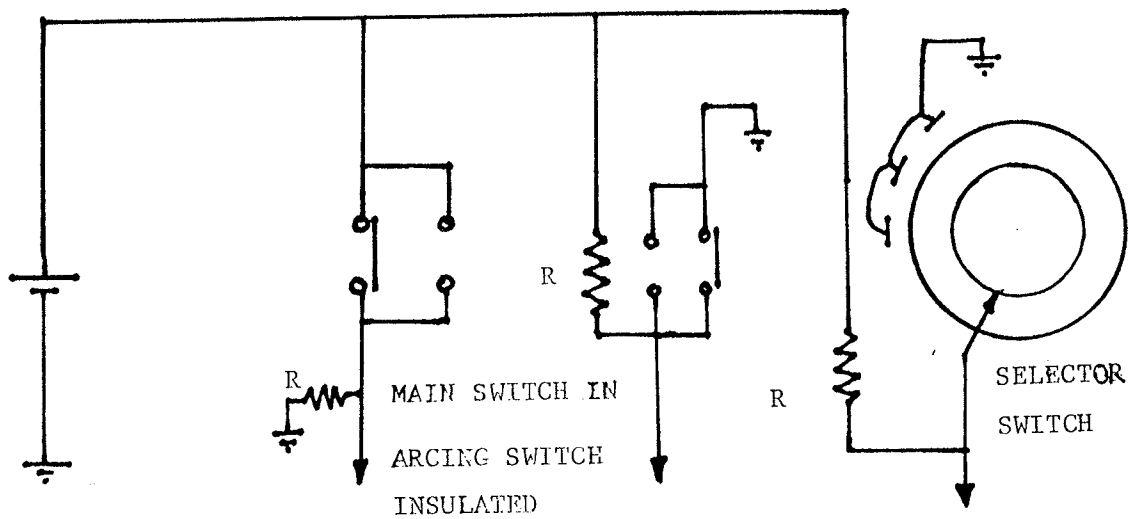


Fig. 2.8 Circuit Diagram for recording main, arcing and selector contact timing sequences

CLOSED

MAIN CONTACT

OPEN

ARCING CONTACT

OPEN

CLOSED

8ms
b

SELECTOR SWITCH

TAP N

TAP N-1

c

d

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

SCALE:- 1 DIV. = 10 ms.

NORMAL SETTING
(LOWER)

Fig. 2.9 Timing charts showing the main,
arcing and selector control sequence

0 1 2 3 4 5 6 7 8 9 10

0 1 2 3 4 5 6 7 8 9 10

OPEN

CLOSED.

e

- 25 -

55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80

Fig. 2.9 Timing charts showing the main, arcing and selector control sequence

Lower Normal setting

0 1 2 3 4 5 6 7 8 9 10 11 12

CHAPTER III

NEW THYRISTOR ASSISTED ON LOAD TAP CHANGER

3.1 Proposed Scheme

The existing Federal Pioneer on load tap changer breaks the tap current in the diverter switches. These diverter switches consist of an arcing switch (SA) in parallel with a main switch (SM). The tap current is normally carried by SM by virtue of its lower resistance path than through SA, but when a tap change is taking place SM opens first and diverts the tap current through SA. Then, SA opens and causes the chopping of the tap current resulting in severe arcing at its contacts. Thus the arcing switch (SA), made of tungsten-copper alloy, protects the main switch from breaking any current. The arc produced, due to energy stored in the reactor, damages the SA contacts and contaminates the oil. This arcing can be eliminated by integrating thyristors in the diverter switches in such a manner that the thyristors perform the current making and breaking duty while mechanical switches carry normal and fault currents. The current conduction in the thyristors can be controlled by gate trigger [1],[2].

The proposed scheme uses a pair of antiparallel thyristors in series with each arcing contact (Fig. 3.1). Under normal condition the main switch carries the tap current and thyristors remain non-conducting. Before the main switch opens the thyristors are supplied with gate current. The current through the main switch, SM, then commutates through the thyristor branch allowing SM contacts to open with negligible arcing. The current through the thyristors stops at its next natural zero when their gate signals are suppressed. This eliminates the arcing at the arcing switch which now acts as a back up switch.

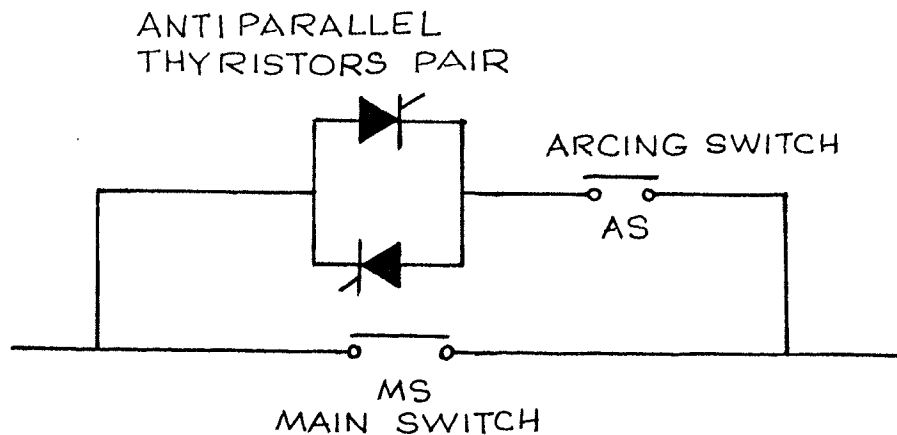
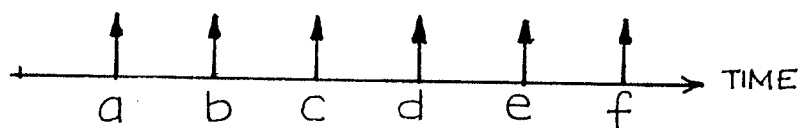


Fig. 3.1 Proposed Scheme for the new thyristor assisted on load tap changer



- a) Main Switch (SM) opens
- b) Thyristors gate signals blocked
- c) Arcing Contact opens
- d) Arcing Contact closes
- e) Thyristor gate signals started
- f) Main Switch (SM) closes

Fig. 3.2 Sequence of operation of the proposed scheme

Similarly when making current at a new tap the reverse sequence is repeated, that is SA closes first without initiating any current. The thyristors, after some time delay, are triggered by gate current to conduct the tap current. This prevents any pre-arc condition on the arcing contact. The main switch then closes to carry the tap current, relieving the thyristors. This full sequence is arc free and is illustrated in Fig. 3.2.

3.2 Advantages of the Proposed Scheme

1. The tap change is arc-less and thus it increases contact life and minimizes oil contamination.
2. Since thyristors carry current only for a few cycles they can be used for higher currents than their rated value.
3. Thyristors have been proven to be very reliable devices and would therefore not affect the reliability of the tap changer.
4. In the event the thyristor(s) fail in short the tap changer acts like the original tap changer.
5. In the rare event of thyristor failure in open, the condition is sensed and tap change is disabled.

3.3 Preliminary Investigations

To gain confidence in the proposed scheme, at first, a preliminary investigation by using a diode in place of the thyristors in the auxiliary circuit was made. The Federal Pioneer tap changer was simulated in the laboratory as shown in Fig. 3.3(a). The center-tap air gap reactor was adjusted to get 50% circulating current. A pure inductive load was connected for the worst expected transients. An electrically operated switch acted as the main switch (SM). This switch was shunted by a diode. The switch was operated several times

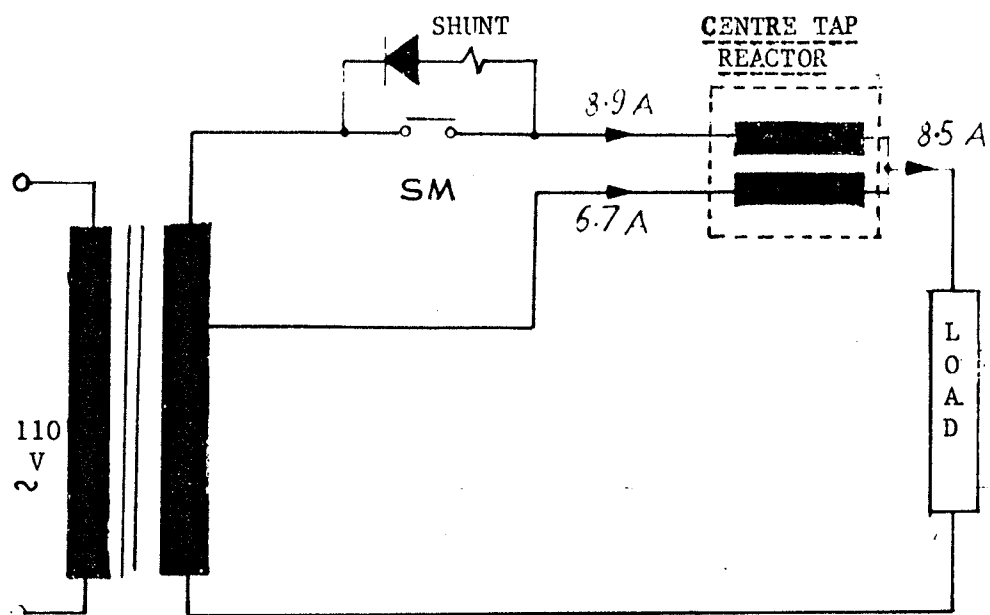


Fig. 3.3 a) Experimental set-up with a diode

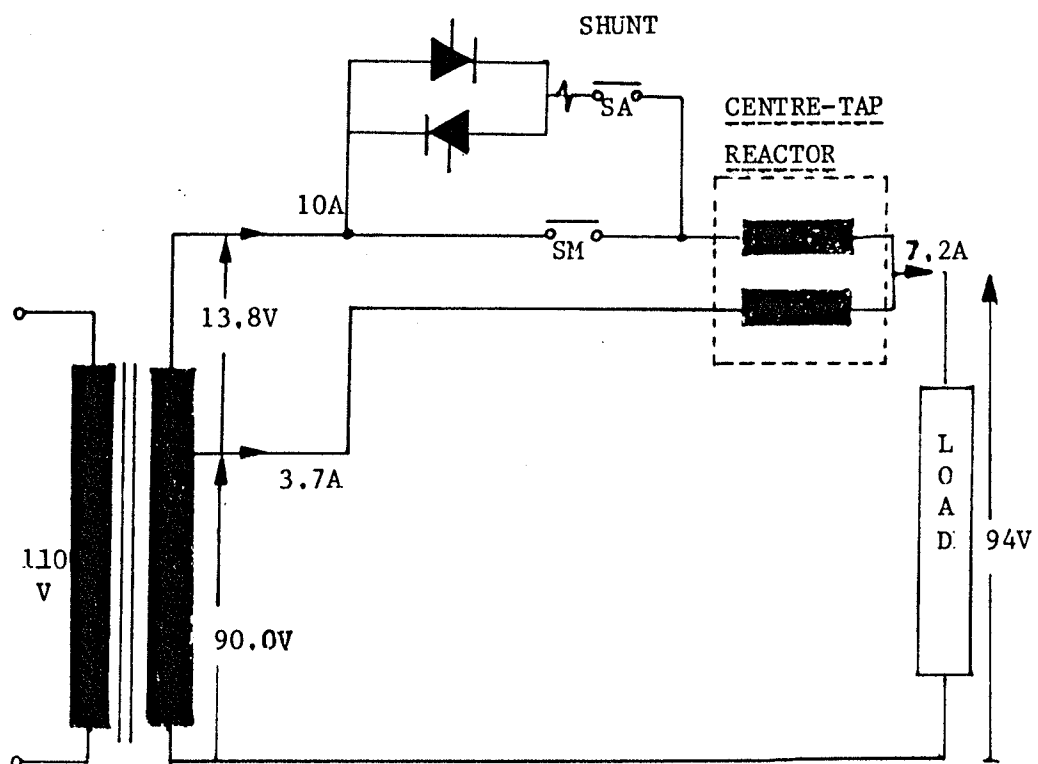


Fig. 3.3 b) Experimental set-up with anti-parallel thyristors

and the transient voltage and current were observed for the diode. Sample results are presented in this section.

- 1) When the switch is opened in positive half cycle the diode is reverse biased. This situation corresponds to the opening of the arcing contacts (SA) of the existing tap changer. The oscillogram in Fig. 3.4(a) shows large voltage (due to large di/dt) which is responsible for causing the arcing at the contacts.
- 2) When the switch is opened in the negative half cycle, the diode is forward biased and this corresponds to the situation of main contact opening, commutating the current through the arcing contact and interrupting it at current zero. Fig. 3.4(b) shows the absence of the voltage spike which otherwise causes arcing.

The above experiment was repeated after replacing the diode with thyristors as shown in Fig. 3.3(b). The block diagram of the control circuit used for firing the thyristors is shown in Fig. 3.5. The transformer T1 steps down the voltage. A voltage comparator produces a pulse when this voltage goes positive. This triggers a monostable to give a pulse of half cycle. The logic AND gates divert the clock signals to the forward biased thyristor. To stop these signals at current breaking the current cycles through the thyristors are counted in a counter by using a voltage comparator sensing the wave shaped current signal. The pulses from the clock are disabled at the end of the desired count. For making current, the switch S1 is set high and thyristors are continuously gated.

Current Making Sequence:

- a) Firing pulses are applied to the thyristors while the arcing contact (SA) is closed and main contact (SM) is open.
- b) Main contact is closed, thereby commutating the thyristor current to the main contact

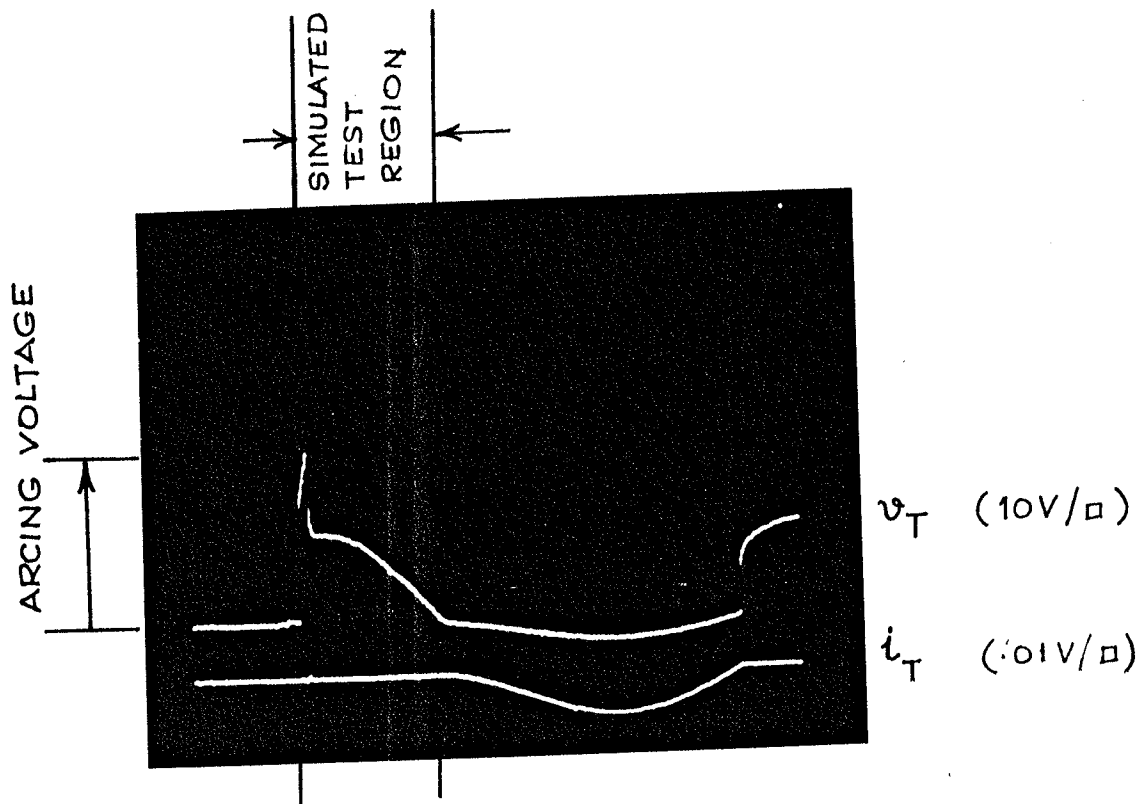


Fig. 3.4 (a) Voltage transient, which causes arcing on SA contacts

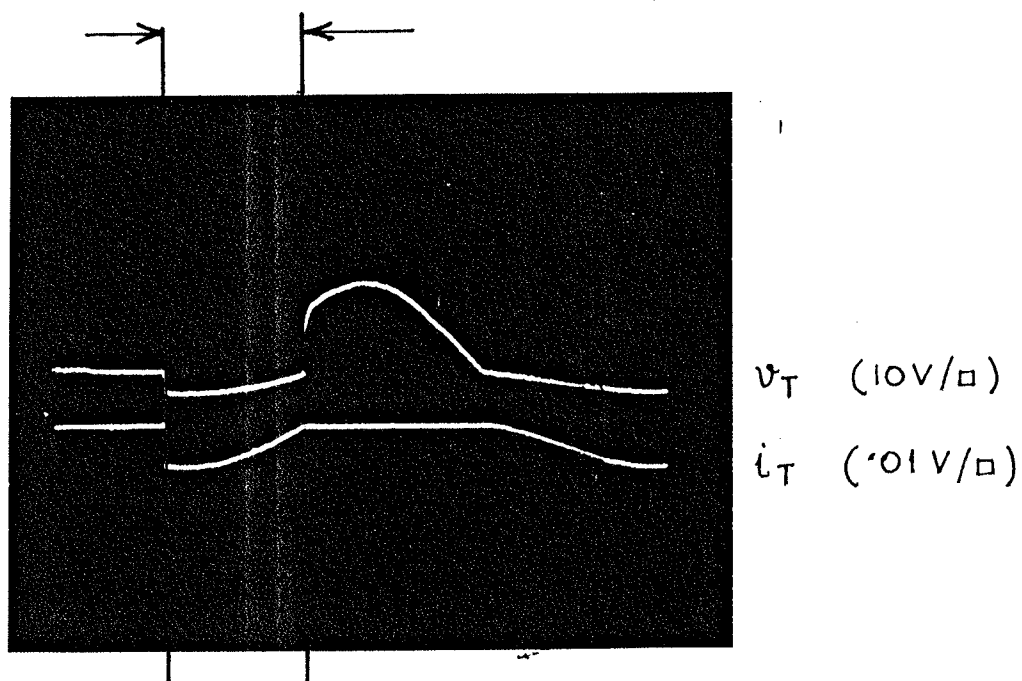


Fig. 3.4 (b) Elimination of the voltage spike which causes arcing

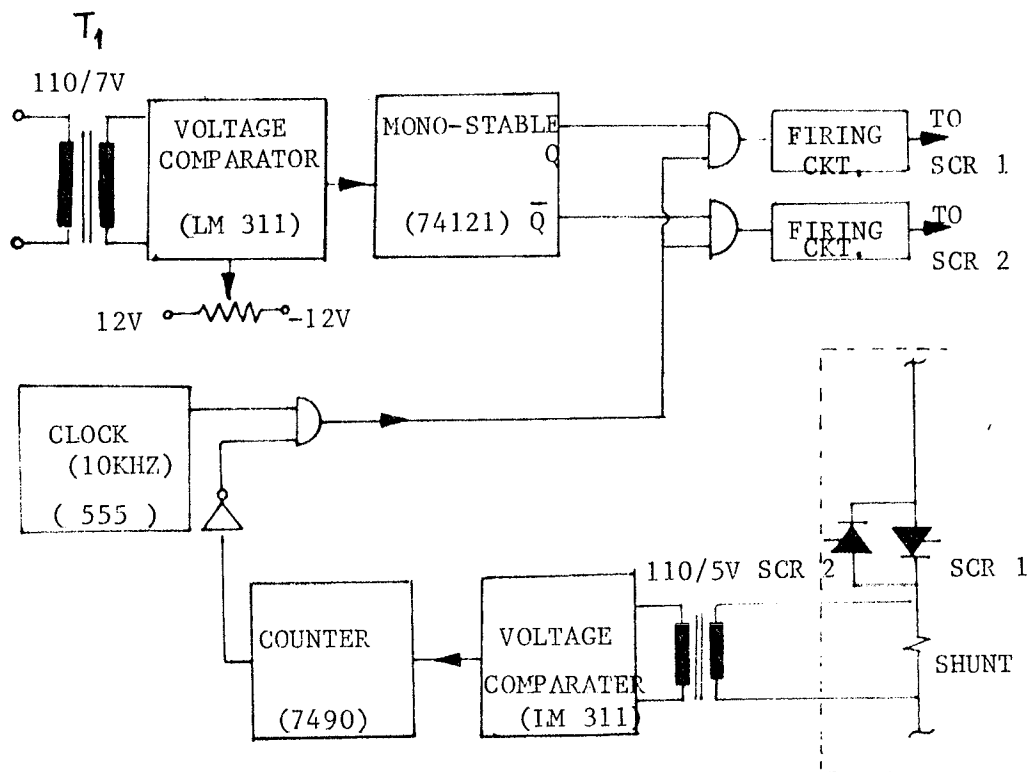


Fig. 3.5 a) Block schematic of the control scheme for experimental set-up

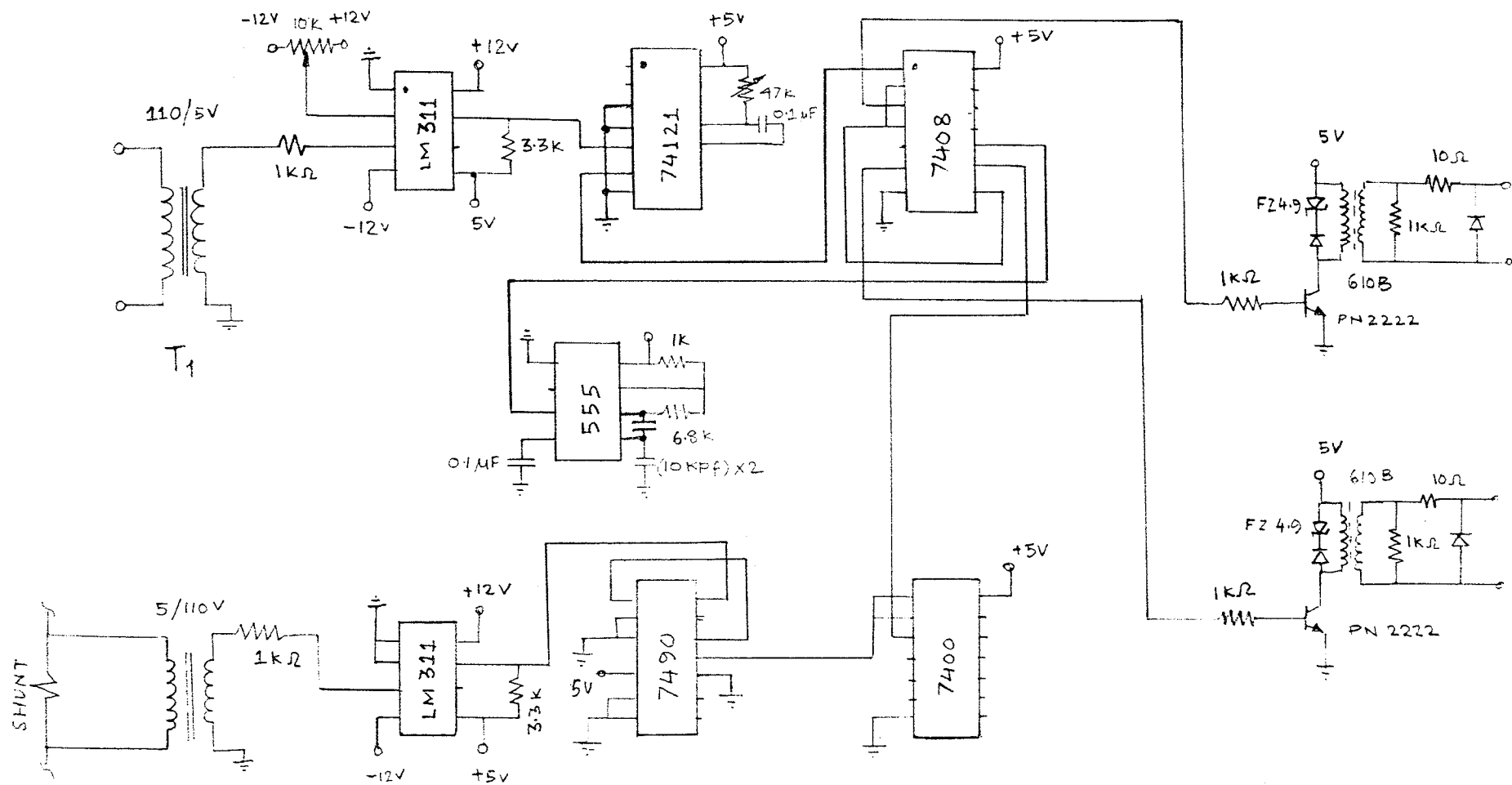


Fig. 3.5 b) Circuit diagram of control circuit

Current Breaking Sequence

- 1) Firing pulses are applied when both the arcing and the main switches are closed.
- 2) Main switch is opened, this makes the thyristors and the arcing contact to carry the current.
- 3) Firing pulses to the thyristors are blocked. This in turn causes the thyristor to go to the blocking state on the next current zero.
- 4) Arcing contacts (SA) are opened.
- 5) The mechanism is ready for tap change.

The results obtained are shown in Figs. 3.6 (a), (b), (c) & (d).

3.4 Literature Search

A literature search in computer data base was carried out from the University of Manitoba Engineering Library. The data base in this search is maintained at Canada Institute for Scientific and Technical Information, Ottawa, Canada which scrutinizes records over the last ten to eleven years. The paper keyword search with keywords Transformer and Tap Changer resulted in a list of thirty five papers and patents. A later search for patents from U.S.A., Canada, Japan, Germany, U.K. and other European countries over a period of last ten years resulted in only one patent [35]. Another search carried out through NRC - Technical Advisory Committee resulted in six patents [36 to 41].

The papers [1] and [2] are among the most useful. They describe thyristor application for resistive type tap changers. The test results for 200 to 400 A have been presented.

Two papers, [3] and [4] deal with thyristor application to tap

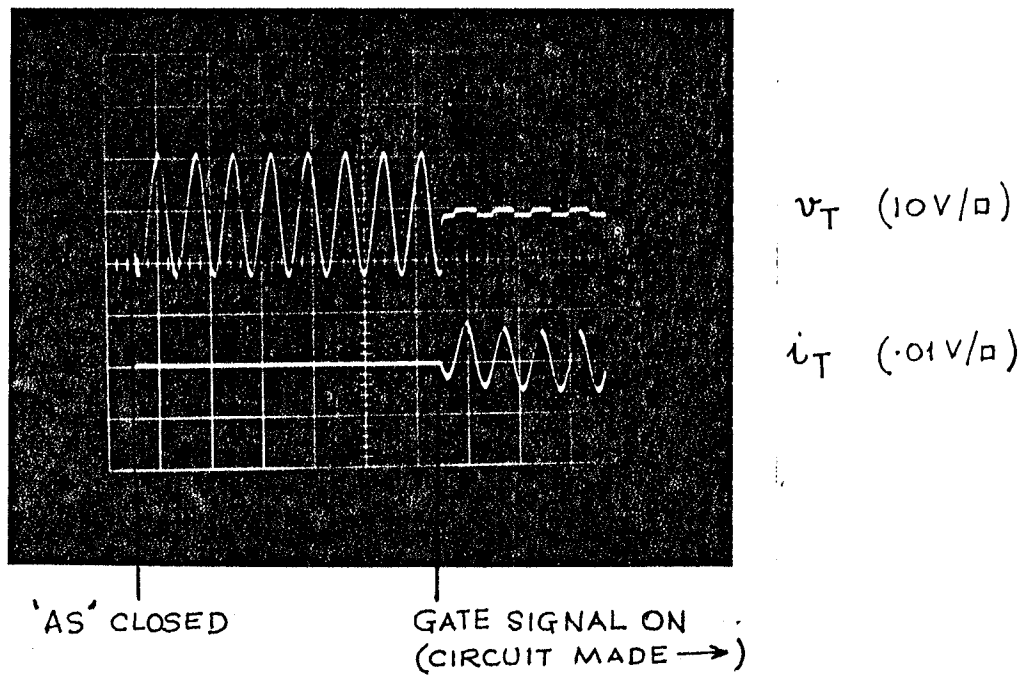


Fig. 3.6 a) Current making in tap changer arm
(gating signals removed after 8 cycles)

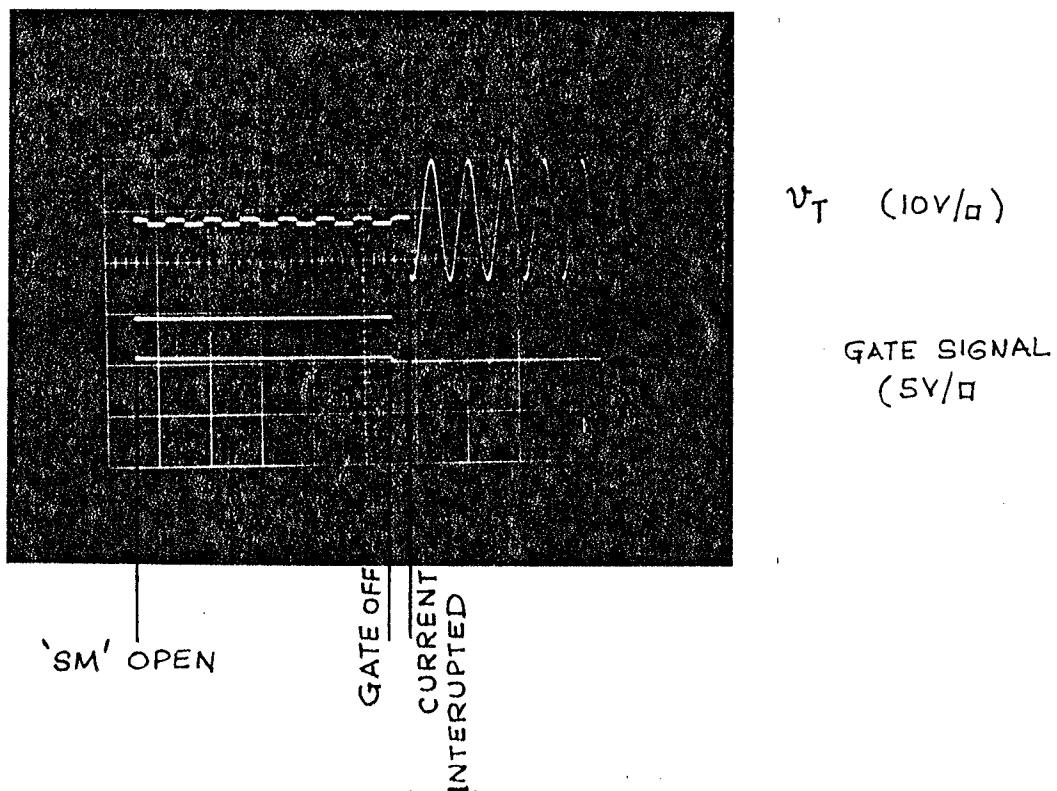


Fig. 3.6 b) Current breaking in tap changer arm

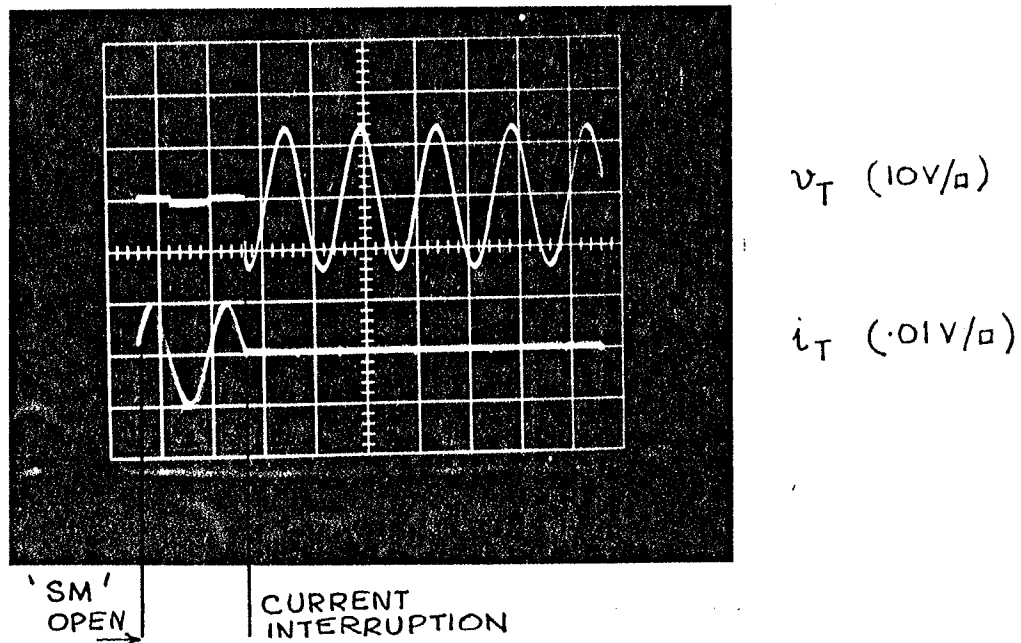


Fig. 3.6 c) Current breaking in tap changer arm after removing gate signals (3 half cycles)

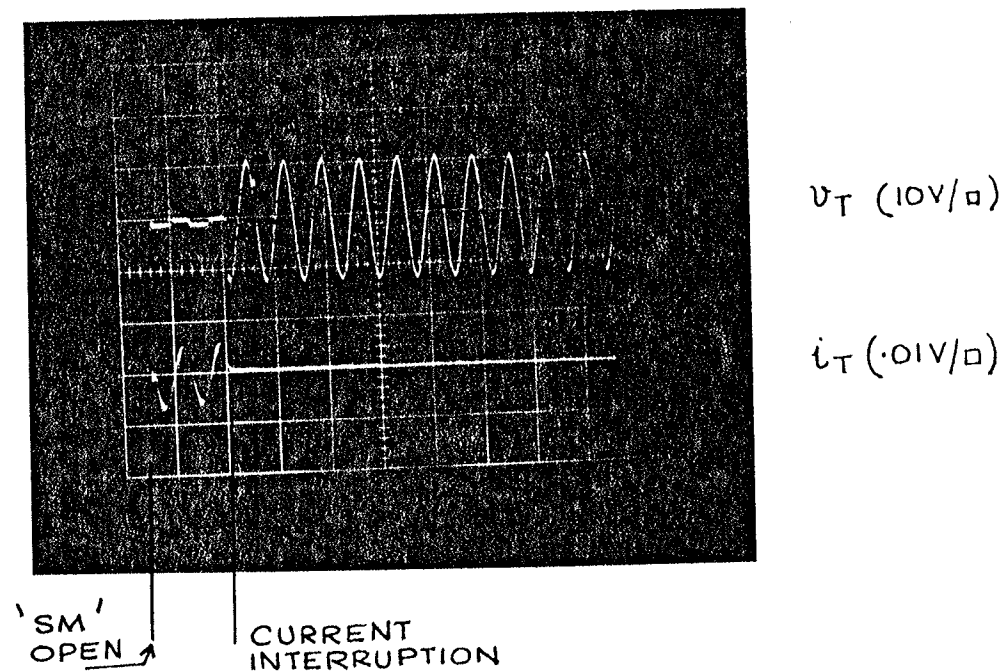


Fig. 3.6 d) Current breaking in tap changer arm after removing gate signals (4 half cycles)

changers in which continuous duty cycle of the thyristors is required. These papers are of marginal interest only. Papers [5] and [6] deal with vacuum bottle application to tap changers. These papers are of some interest because they address to the same problem. Papers and patents [9] to [14] deal with various commercial products and, some of them, especially [14] are valuable. Remaining references [15] to [35] are of general interest. Useful references for the design of the proposed tap changer are listed.

CHAPTER IV

ANALYSIS OF THE PROPOSED TAP-CHANGER

4.1 Introduction

The proposed scheme uses a thyristor to switch the current on and off through the reactor. It is important to study the transient behavior of current and recovery voltages for thyristor valve sizing for the tap changer. This chapter describes the analysis, computer simulation of the tap changer and some of the results obtained using the simulation programs. The tap changer has been modelled by a single phase equivalent circuit shown in Fig. 4.1. The transformer secondary side has been modelled as a voltage source in series with resistance and inductance. The reactor has been modelled as two equal, non-ideal mutually coupled coils ($k < 1$) with winding resistances. The load has been represented as an inductive load. The model variables are summarized in Table 4.1. The circuit in general consists of two coupled current loop equations of the first order. These equations have then been solved to get uncoupled equations in currents. The resulting differential equations have been simulated on computer using CONTINUOUS SIMULATION MODELLING PROGRAM (CSMP). A set of three simulation programs have been developed namely: (1) TCTA-OFF (2) TCTA-ON and (3) TCTA-SNUB. Figure 4.2 describes the general algorithm of the programs.

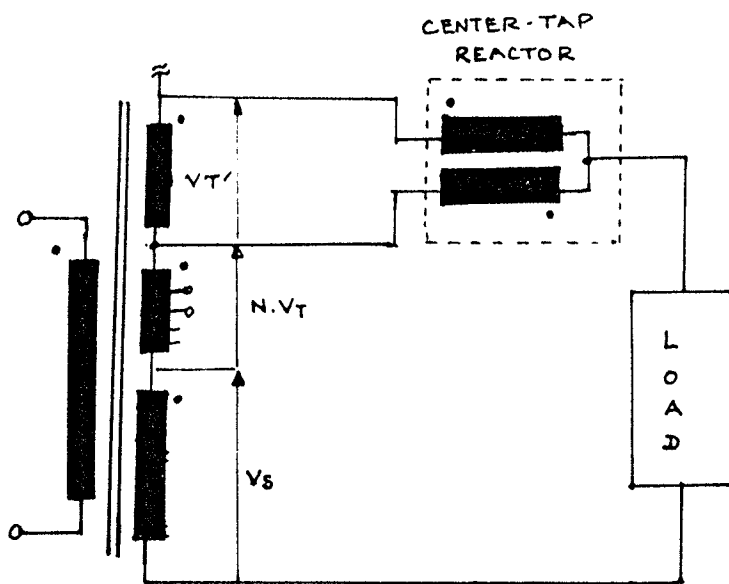


Fig. 4.1 a) Schematic representation of FPE Tap Changer

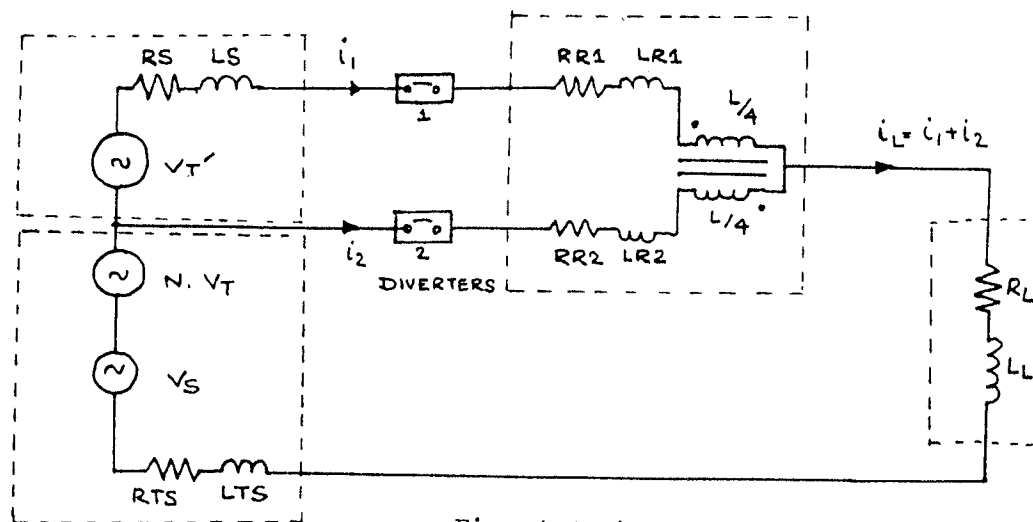


Fig. 4.1 b) Equivalent circuit model

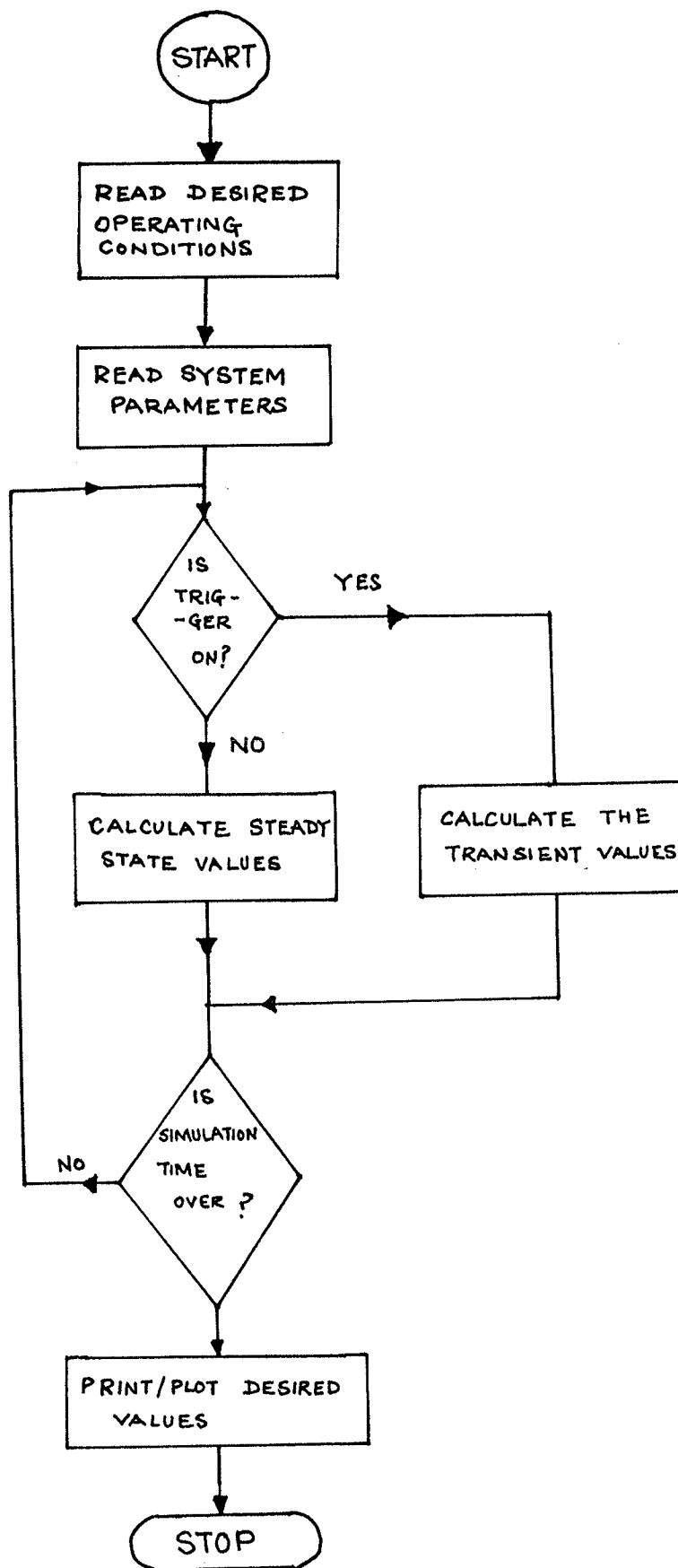


Fig. 4.2 General flowchart of simulation program

Table 4.1

List of Variables

VOLTAGE

- | | | |
|----|----------------|--|
| 1. | V _s | Equivalent main-secondary winding voltage source as seen from secondary. |
| 2. | V _t | Equivalent tap winding voltage source as seen from secondary. |
| 3. | V _t | 0 for nonbridging position
V _T for bridging position |

INDUCTANCES

- | | | |
|----|----------------------------------|--|
| 4. | L _S | Equivalent leakage inductance reflected on tap winding side (bridging position)
0 (nonbridge in position) |
| 5. | L _{R1} /L _{R2} | Upper/lower half leakage inductances of the reactor. |
| 6. | L | Total end to end inductance of the reactor. |
| 7. | M | Mutual inductance of the two halves of the reactor winding. |
| 8. | L _L | Equivalent load inductance |
| 9. | L _{TS} | Equivalent leakage inductance reflected on secondary S1S3. |

RESISTANCES

- | | | |
|-----|----------------------------------|---|
| 10. | R _S | Equivalent resistance reflected on tap winding secondary (bridging position)
0 (nonbridging) |
| 11. | R _{R1} /R _{R2} | Upper/lower half reactor winding resistances. |
| 12. | R _L | Equivalent load resistance. |

MISCELLANEOUS

- | | | |
|-----|----------|---|
| 13. | k | Co-efficient of mutual coupling. |
| 14. | N | Number of tap at which lower arm of reactor is sitting. |
| 15. | ω | Angular frequency ($=2\pi f$) |
| 16. | f | Power frequency (60 Hz). |
| 17. | j | $\sqrt{-1}$ |

The programs have a feature analogous to pretrigger in an oscilloscope. It gives the steady state values of current and voltages just before the desired change is occurring in the tap changer. The simulation programs solve for both bridging and nonbridging positions of the reactor. Results of the desired voltage and currents are plotted on the Versatec plotter using a plotting program.

4.2 Analysis

4.2.1 TCTA OFF

When the tap-changer is in bridging position, from the Kirchhoff's law, equations can be written in the following form:

$$\begin{aligned} v_s + N.v_t &= (R_{TS} + R_L).i_1 + (L_{TS} + L_L - k.L/4).di_1/dt \\ &+ (R_{TS} + R_L + R_{R2}).i_2 + (L_{TS} + L_L + L_{R2} + L/4).di_2/dt \end{aligned} \quad (4.1)$$

$$\begin{aligned} v_t' &= (R_S + R_{R1}).i_1 + (L_S + L_{R1} + L/4 + k.L/4).di_1/dt \\ &- R_{R2}.i_2 - (L_{R2} + L/4 + k.L/4).di_2/dt \end{aligned} \quad (4.2)$$

These simultaneous equations are solved for tap currents in the frequency domain. The expressions for individual currents in phasor representation are given in Table 4.2.

When the switching occurs in upper or lower arm in the proposed scheme the corresponding current stops at its next current zero. After this instant of time the circuit consists of a single loop. The loop equations for the resulting transient current, in instantaneous



TABLE 4.2 Formulations for TCTA-OFF

Steady-State currents:

$$\bar{I}_1 = \sqrt{\left(\frac{N1REAL^2 + N2IMAG^2}{DREAL^2 + DIMAG^2}\right)} \angle \left(\tan^{-1} \frac{N1IMAG}{N1REAL} - \tan^{-1} \frac{DIMAG}{DREAL}\right)$$

$$\bar{I}_2 = \sqrt{\left(\frac{N2REAL^2 + N2IMAG^2}{DREAL^2 + DIMAG^2}\right)} \angle \left(\tan^{-1} \frac{N2IMAG}{N2REAL} - \tan^{-1} \frac{DIMAG}{DREAL}\right)$$

where

$$N1REAL = vt'A4 - (vs+N.vt) A2$$

$$N1IMAG = vt'B4 - (vs+N.vt) B2$$

$$DREAL = A1*A4 - B1*B4 - A2*A3 + B2*B3$$

$$DIMAG = B1*A4 + B4*A1 - A2*B3 - A3*B2$$

$$N2REAL = A1*(vs+N.vt) - vt'*A3$$

$$N2IMAG = -B3*vt' + B1*(vs+N.vt)$$

$$A1 = RS+RR1$$

$$A2 = RR2$$

$$A3 = RTS + RL$$

$$A4 = RTS + RR2 + RL$$

$$B1 = \omega*(LS-LR1+L*(k+1.0)/4.0)$$

$$B2 = \omega*(LR2-L*(k+1)/4.0)$$

$$B3 = \omega*(LL-k*L/4.0+LTS)$$

$$B4 = \omega*(LR2+L/4.0+LL+LTS)$$

Transient currents

1. Upper arm switching

$$vs+N.vt = (RR2+RTS+RL) i_2 + (LR2+LL+L/4 + LTS) \frac{di_2}{dt}$$

$$i_1=0$$

$$\text{Recovery voltage, } RV = vt' + RR2i_2 + (LR2+L/4(k+1)) \frac{di_2}{dt}$$

2. Lower arm switching

$$vs+N.vt+vt' = (RS+RR2+RL+RTS) i_1 + (LS+LR2+L/4+LL) \frac{di_1}{dt}$$

$$\text{Recovery voltage, } RV = vt' - (RS+RR2) i_2 - (LR2+L/4(k+1)) \frac{di_1}{dt}$$

values are as follows:

for upper arm switching

$$v_s + N.v_t = (R_{R2} + R_{TS} + R_L).i_2 + (L_{R2} + L_L + L/4 + L_{TS}).di_2/dt \quad (4.3)$$

$$i_2(t_0) = \sqrt{2} . I_2 . \sin (\theta_2 - \theta_1) \quad (4.4)$$

where t_0 = switching time instant

or for lower arm switching

$$v_s + N.v_t + v_t' = (R_S + R_{R2} + R_L + R_{TS}).i_1 + (L_S + L_{R2} + L/4 + L_L).di_1/dt \quad (4.5)$$

$$i_1(t_0) = \sqrt{2} . I_1 . \sin (\theta_1 - \theta_2) \quad (4.6)$$

The first order differential equations are solved with initial current equal to respective initial conditions. The recovery voltage across the thyristors is calculated by the equations given in Table 4.2.

For nonbridging position the switching equations remain same as above but $v_t' = R_S = L_S = 0$.

4.2.2 TCTA-ON

Before the current conducts on a new tap the circuit consists of a single loop. The steady state value of other tap current (lower or upper) is given by the following:

$$v_s + N.v_t = (R_{R2} + R_L + R_{TS}).i_2 + (L_{R2} + L/4 + L_L + L_{TS}).di_2/dt \quad (4.7)$$

or

$$v_s + N.v_t + v_t' = (R_S + R_{R1} + R_{TS} + R_L).i_1 + (L_S + L_{R1} + L/4 + L_L + L_{TS}).di_1/dt \quad (4.8)$$

The resulting expressions are summarized in Table 4.3.

Table 4.3 Formulations for TCTA-ON

Lower or upper arm switching

$$\frac{1}{\omega^2} (B_1 B_4 - B_2 B_3) \frac{d^2 i_1}{dt^2} + \frac{1}{\omega} (B_1 A_4 + B_4 A_1 - A_2 B_3 - A_3 B_2) \frac{di_1}{dt} + (A_1 A_4 - A_2 A_3) i_1$$

$$= (A_4 vt - vst A_2) + \frac{1}{\omega} (B_4 \frac{d}{dt} vt - B_2 \frac{d}{dt} vst)$$

where $vst = vs + N \cdot vt$

$$\frac{1}{\omega^2} (B_1 B_4 - B_2 B_3) \frac{d^2 i_2}{dt^2} + \frac{1}{\omega} (B_1 A_4 + B_4 A_1 - A_2 B_3 - A_3 B_2) \frac{di_2}{dt} + (A_1 A_4 - A_2 A_3) i_2$$

$$= A_1 vst + \frac{B_1}{\omega} \frac{d}{dt} vst - A_3 vt - \frac{B_3}{\omega} \frac{d}{dt} vt$$

Initial conditions

Lower arm switching

$$i_2^{(0)} = 0$$

Upper arm switching

$$i_1^{(0)} = 0$$

For both conditions

$$i_1^{(0)} = \frac{d}{dt} i_1 \Big|_{t=0} = [(vt - \frac{B_2}{B_4} vst) - (A_2 \frac{B_2}{B_4} \cdot A_4) i_2$$

$$- (A_1 - \frac{B_2}{B_4} \cdot A_3) i_1] \frac{\omega}{B_1 - B_3 \cdot \frac{B_2}{B_4}}$$

$$i_2^{(0)} = [(vt - \frac{B_1}{B_3} vst) - (A_1 - \frac{B_1}{B_3} A_3) i_1 - (A_2 - \frac{B_1}{B_3} A_4) i_2] \frac{\omega}{B_2 \frac{B_1 B_4}{B_3}}$$

The transient current equations for both cases are given by the equations 4.1 and 4.2. These two coupled equations when solved can be expressed as two independent equations given in Table 4.3.

4.2.3 TCTA-SNUB

The circuit, when a snubber circuit (series combinations of R and C) is used to limit the dv/dt across the thyristors, is represented by two loop equations (at current interruption) as follows:

$$\begin{aligned} v_s + N.v_t = & (R_{TS} + R_L)i_1 + (L_{TS} + L_L - k.L/4) di_1/dt \\ & + (R_{TS} + R_L + R_{R2})i_2 + (L_{TS} + L_L + L/4 + L_{R2})di_2/dt \end{aligned} \quad (4.9)$$

$$\begin{aligned} v_t' = & (R_S + R_{R1} + R)i_1 + (L_R + L_{R1} + (k+1)L/4)di_1/dt + \frac{1}{C} \int i_1 dt \\ & - R_{R2}.i_2 - (L_{R2} + (k+1)L/4)di_2/dt \end{aligned} \quad (4.10)$$

the solution to these equation is given by a third order equation given in table 4.4. From the solution of these equations we calculate the voltage and dv/dt across the thyristors at turn off.

4.3 Simulation Programs

Tables 4.2, 4.3 and 4.4 give equations for both steady state and transient conditions. These sets of equations have been used to simulate the system in CSMP. The three programs have been developed for the three conditions, i.e., (1) TCTA-OFF, (2) TCTA-ON, (3) TCTA-SNUB. The flowchart of these programs is given in Fig. 4.2. The programs calculate the steady state values until the trigger (TRIG) is set. Then, they calculate the transient values by the CSMP program. The operating condition of the tap changer can be specified by vari-

ables in the program like 'BRIG', 'LOWON', 'UPON'. The number of pretrigger cycles is specified by variable 'PRE' and its sensitivity by 'EPS'. The parameters like vt,vt',vs,LRI, etc. can be specified for a given transformer. The desired output variables are specified in 'PRTPLT' statement.

Table 4.4 Formulations for TCTA-SNUB

With R-C (Resistance and capacitor combination) across the
divertor at turn off.

$$v_t = F_{33} \ddot{q} + F_{22} \ddot{q} + F_{11} \ddot{q} + F_{oo} \ddot{q} + C_{oo}$$

$$F_{33} = \frac{LE2.F_2}{F_3}$$

$$F_{22} = LE1 + \frac{RE2.F_2}{F_3} + \frac{LE2.F_1}{F_3}$$

$$F_{11} = RE1 + \frac{RE2}{F_3} \cdot F_1 + \frac{LE2}{F_3 \cdot C}$$

$$F_{oo} = \frac{RE2}{F_3 \cdot C}$$

$$C_{oo} = -\frac{RE2}{F_3} \cdot (v_t + \frac{LE2}{LE4} \cdot v_{st}) - \frac{LE2}{F_3} \cdot (v_t + \frac{LE2}{LE4} \cdot v_{st})$$

Initial conditions

$$q(0) = 0$$

$$\dot{q}(0) = 0$$

$$\ddot{q}(0) = (v_t - F_1 \cdot i_1(0) - F_3 i_2(0) + \frac{LE2}{LE4} \cdot v_{st}(0)) / F_2$$

$$F_1 = RE1 + \frac{LE2.RE3}{LE4}$$

$$F_2 = LE1 + \frac{LE2.LE3}{LE4}$$

$$F_3 = -RE2 + \frac{LE2.RE4}{LE4}$$

$$RE1 = RS + RR1 + R$$

$$RE2 = RR2$$

$$RE3 = RTS + RL$$

$$RE4 = RTS + RR2 + RL$$

$$LE1 = LS + LR1 + L/4 (k+1)$$

$$LE2 = LR2 + L/4 (k+1)$$

$$LE3 = LL - k \cdot L/4 + LTS$$

$$LE4 = LR2 + L/4 + LL + LTS$$

4.4 Simulation Results

The simulation programs were run for various operating conditions. A typical set of results is shown in Fig. 4.3 to 4.6. These results are for the following data:

- 1) Load Current 1000 A, 0.8 pf
- 2) Circulating current 500 A,
- 3) Tap voltage 150 V

When the tap changer is in bridging position and a tap change is desired to lower the load voltage then the resulting current and voltage waveforms are shown in Fig. 4.3(a) to (c). Figure 4.3(a) shows the current in the upper tap thyristors when the main contact opens at tap voltage $v_t=0$ at $t=0$. This current is the steady state current and is sum of half the load current and the circulating current till $t=T_2$. The gate signals to the thyristors are blocked between T_1 and T_2 by virtue of which the circuit is turned off after the current zero at $t=T_2$. Figure 4.3b shows the current in the lower tap. It may be noted that this current is leading the tap voltage while the upper tap current was lagging the tap voltage and that it is smaller in magnitude. At time $t=T_2$ the current changes from its initial steady state value of sum of half the load current and the circulating current to the load current.

Figure 4.3c shows the voltage across the thyristors in the upper arm. When the thyristors are conducting as shown in Fig. 4.3(a) the voltage across the thyristors remain nearly zero but when they stop conducting a voltage, which is the sum of tap and induced voltage in the center tap reactor, appears across them. This voltage, as can be observed from Fig. 4.3(c) reaches almost the peak value at the instant

Fig. 4.3 a) Current in the upper arm thyristors when it is required to move to a new setting from bridging position

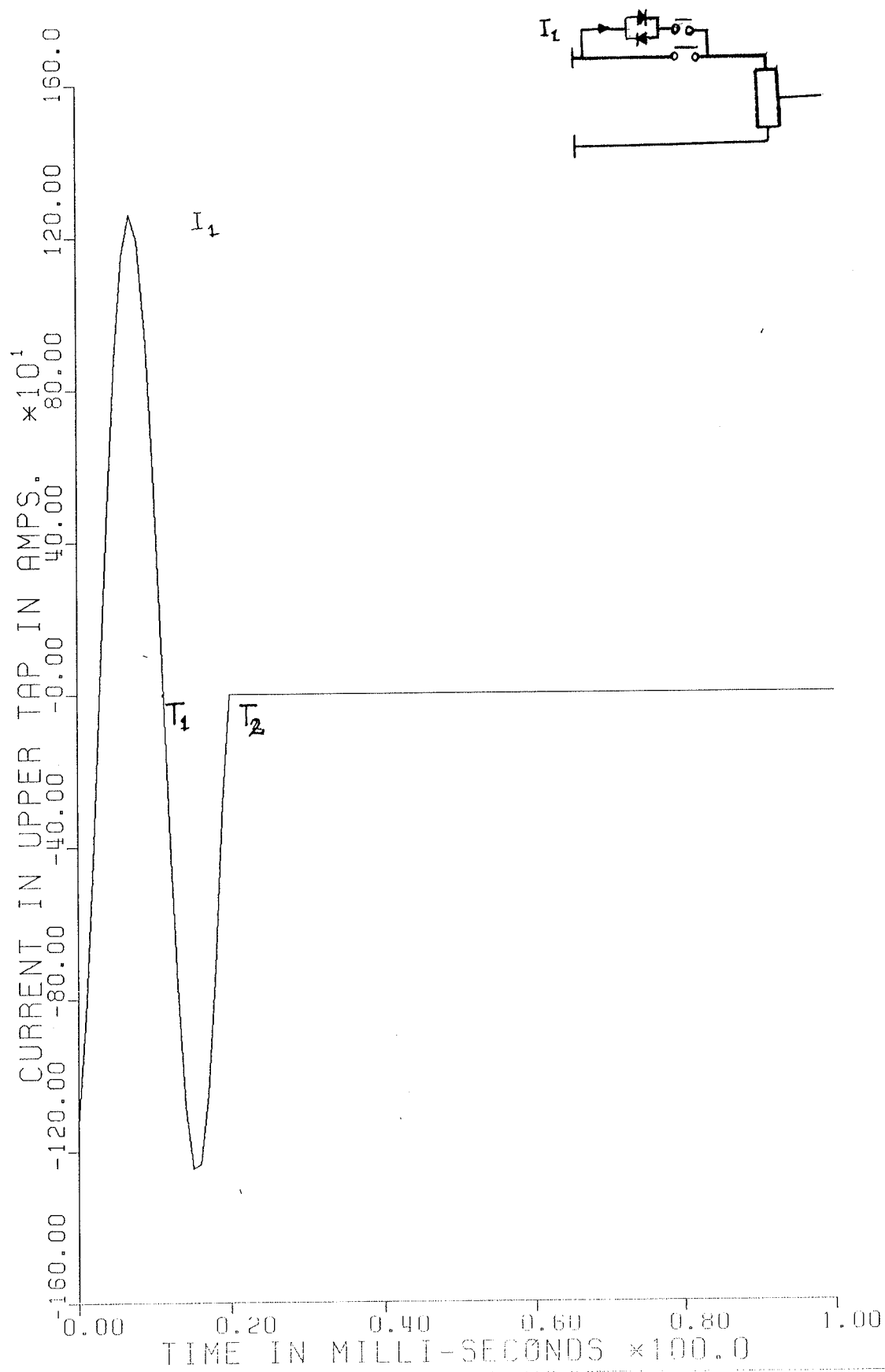
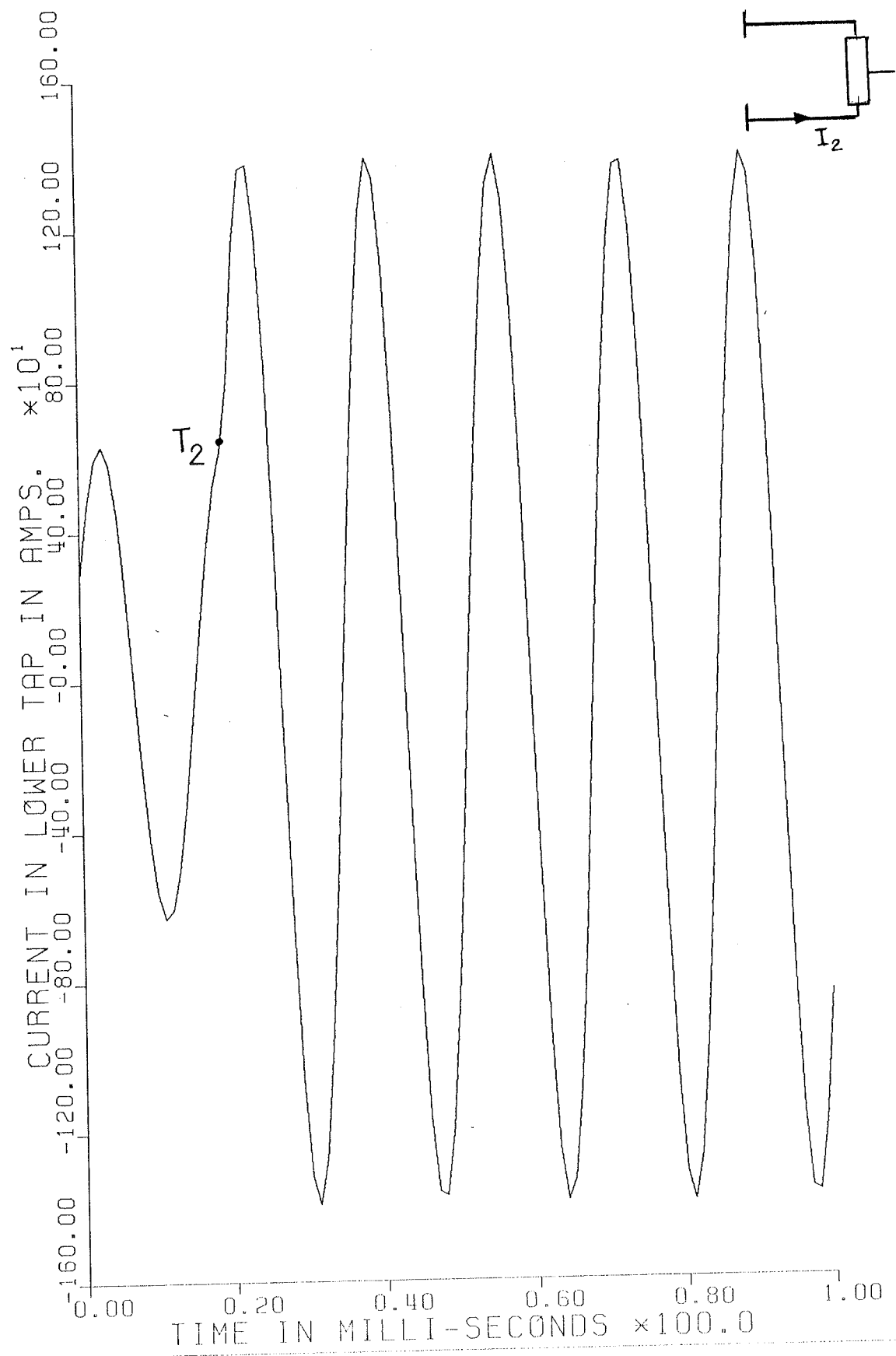


Fig. 4.3 b) Current in the lower arm when the upper arm is disconnected from the bridging position



- 54 -

Fig. 4.3 c) Voltage across the thyristors in the upper arm which is required to move to a new setting from the bridging position

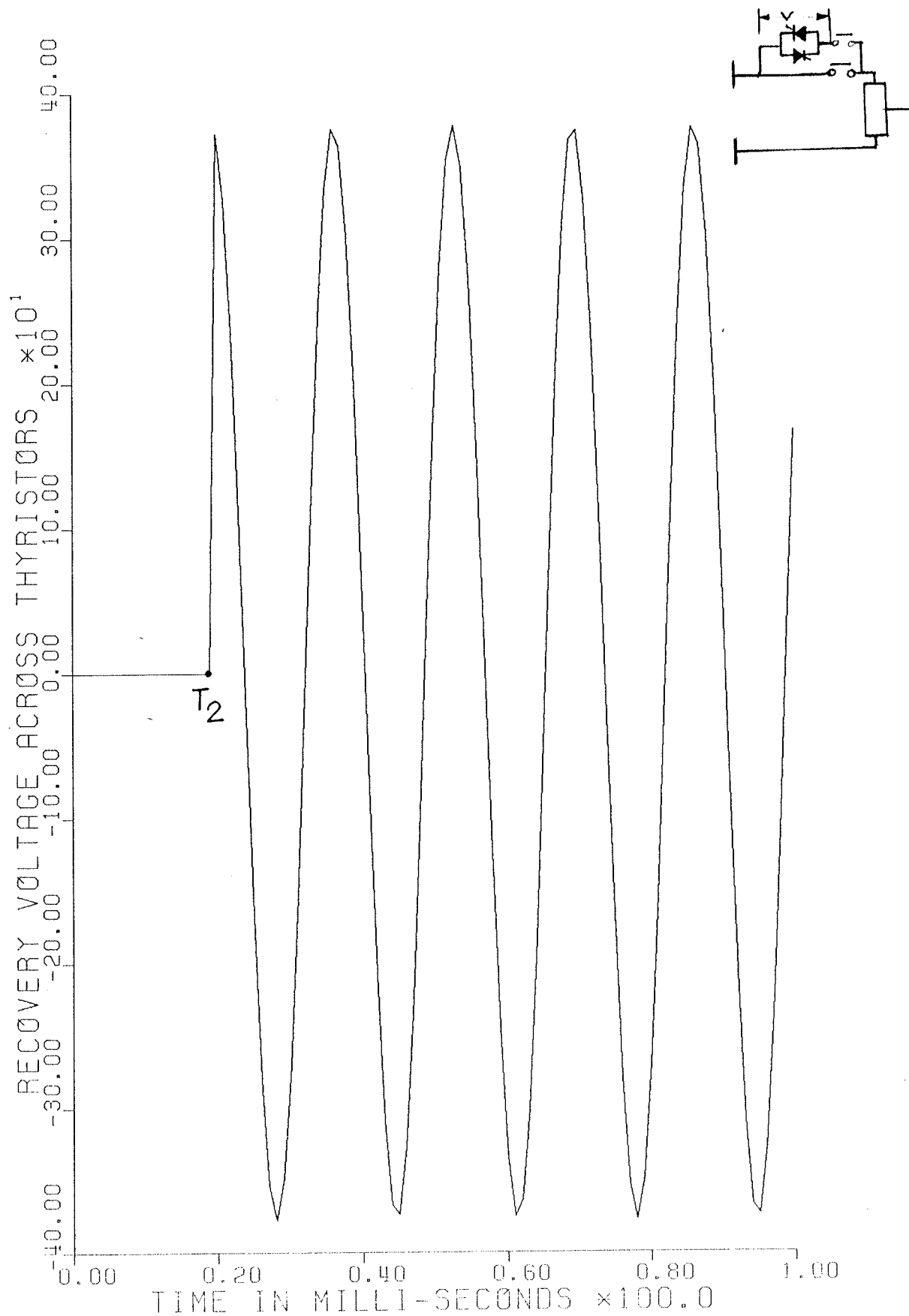


Fig. 4.4 a) Current in the upper arm when the lower arm is brought into nonbridging position. Thyristors in lower arm start conducting at $t=T_1$ (case 1)

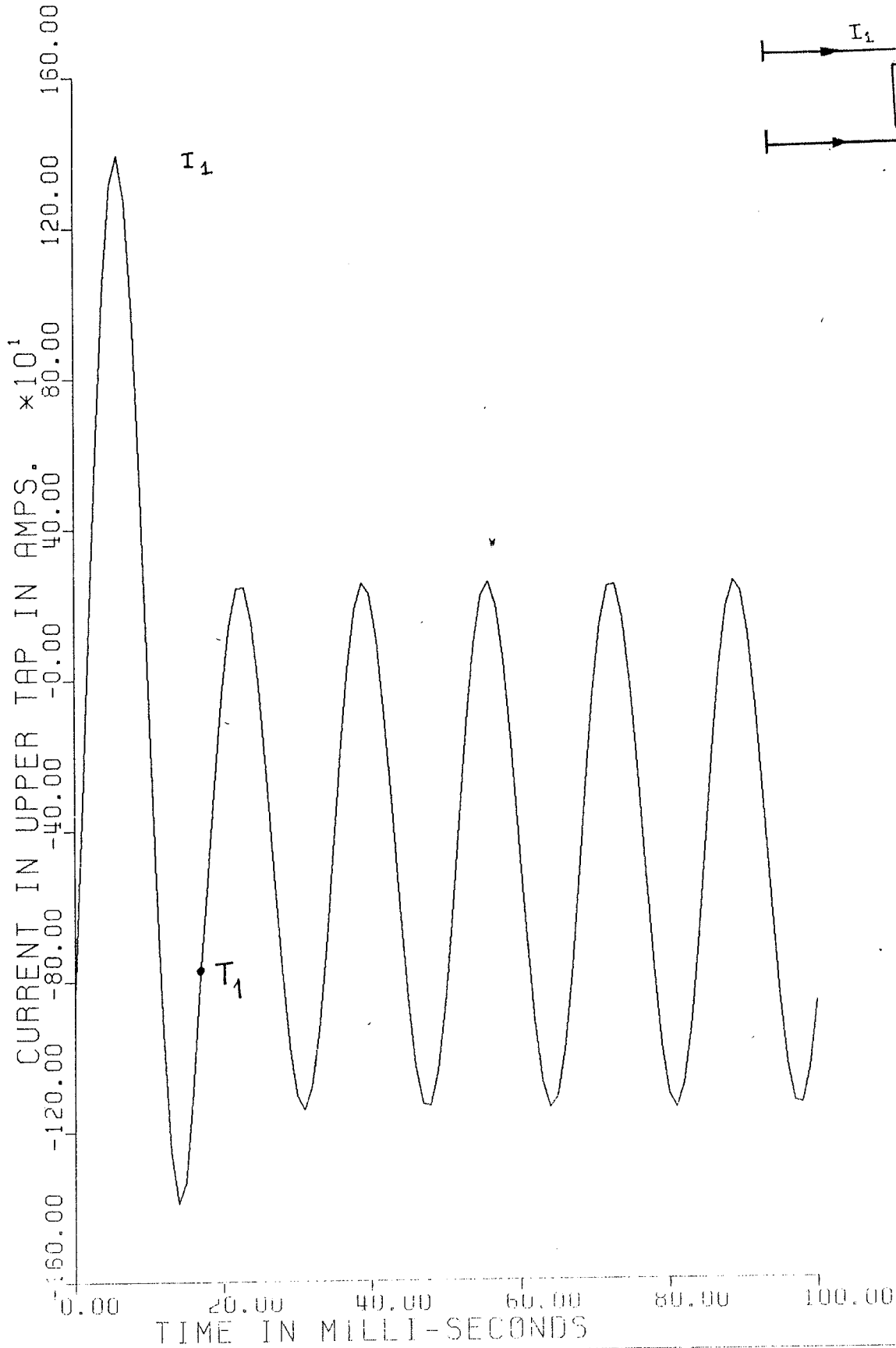
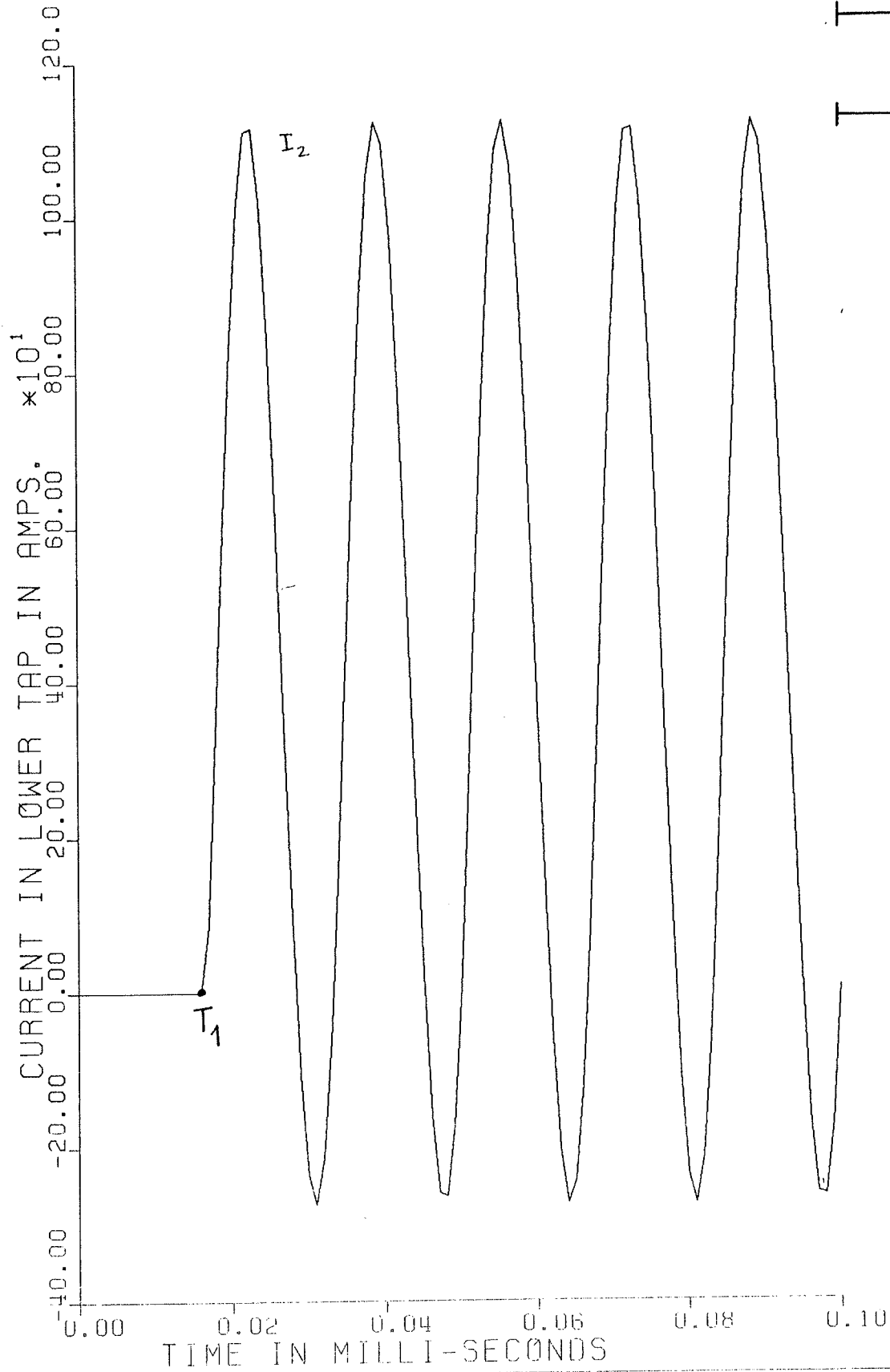


Fig. 4.4 b) Current in lower arm thyristors ,
fired at $t = T_1$ (case 1)



(T_2) of current interruption. This shows a large dv/dt stress on the thyristors and hence some protection against large dv/dt is required. Figures 4.4 and 4.5 show the output for the situation when one of the tap position changes from nonbridging to lower position at different instants of time. The currents in Figures 4.4(a) and 4.5(a) show the steady state load current until $t=T_1$ when the lower tap thyristor start conducting. The lower tap thyristor current as shown in figures 4.4(b) and 4.5(b) show that the transient current through them is dc offset and hence larger than the steady state value. This dc offset current normally decays to zero due to resistive elements in the circulating loop. However for the above cases resistance was set to zero. Figure 4.5(b) represents the worst transient current through the thyristor.

Figure 4.6 shows the voltage waveforms when a snubber circuit consisting of a simple series resistor and capacitor circuit is connected across the thyristors. A typical value of $R=200\ \Omega$ and $C=0.1\ \mu F$ was tried for the tap changer. The programme TCTA-SNUB was used to get the voltage and dv/dt across the thyristors. Figure 4.6(a) shows the dv/dt stress in $\mu V/s$ across the thyristor. It can be noted that it is maximum at the instant of current interruption. This value has to be limited within the thyristor specification by proper selection of R and C .

Figure 4.6(b) shows the voltage across the snubber circuit. This voltage rises quite rapidly to a maximum value of 280 V within 20 μs . Figure 4.7 shows the transient as well as steady state voltage across the thyristors. It may be noted that the first peak voltage is larger than subsequent voltages. Thus this value determines the thyristor voltage specifications.

Fig. 4.5 a) Current in the upper arm when the lower arm is brought into nonbridging position. Thyristors in the lower arm start conducting at $t = T_1$ (case 2: worst case)

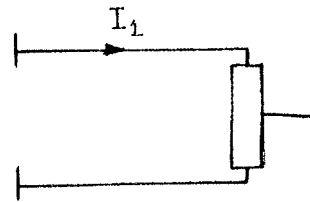
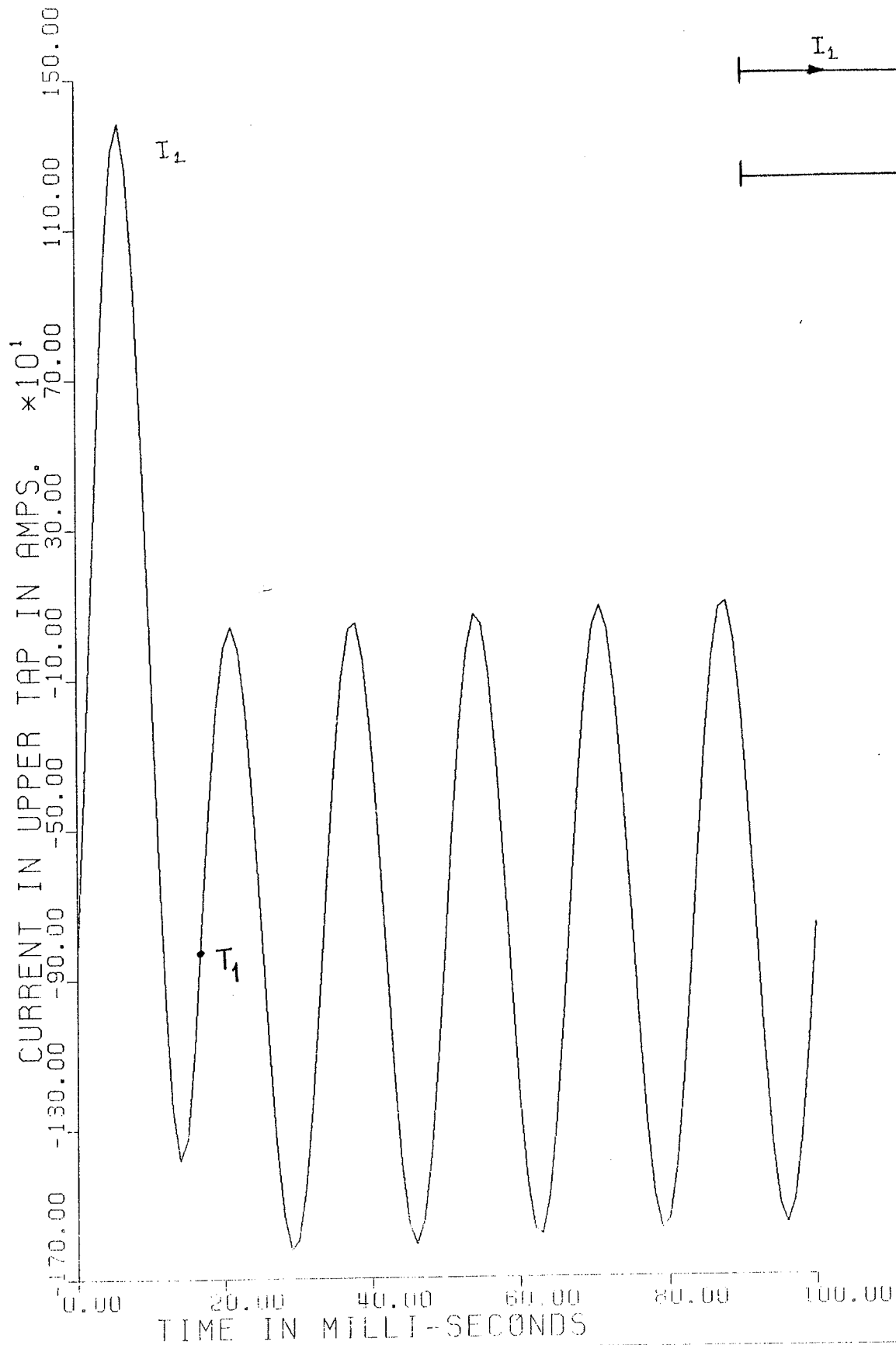


Fig. 4.5 b) Current in lower arm thyristors, fired at $t = T_1$
(case 2: worst case)

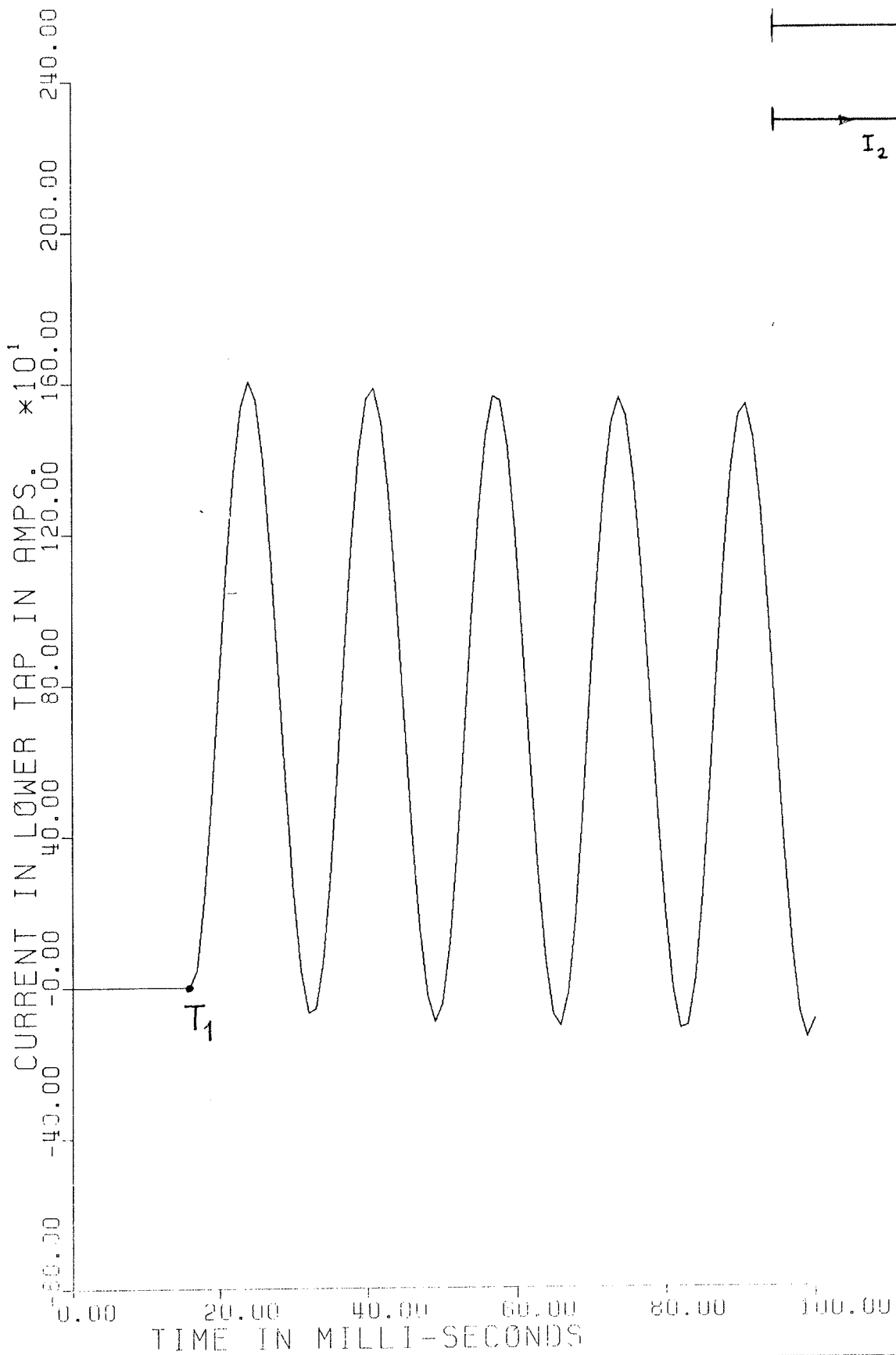


Fig. 4.6 a) $\frac{dv}{dt}$ across thyristors when the current is interrupted (with snubber circuit)

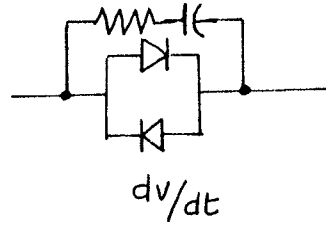
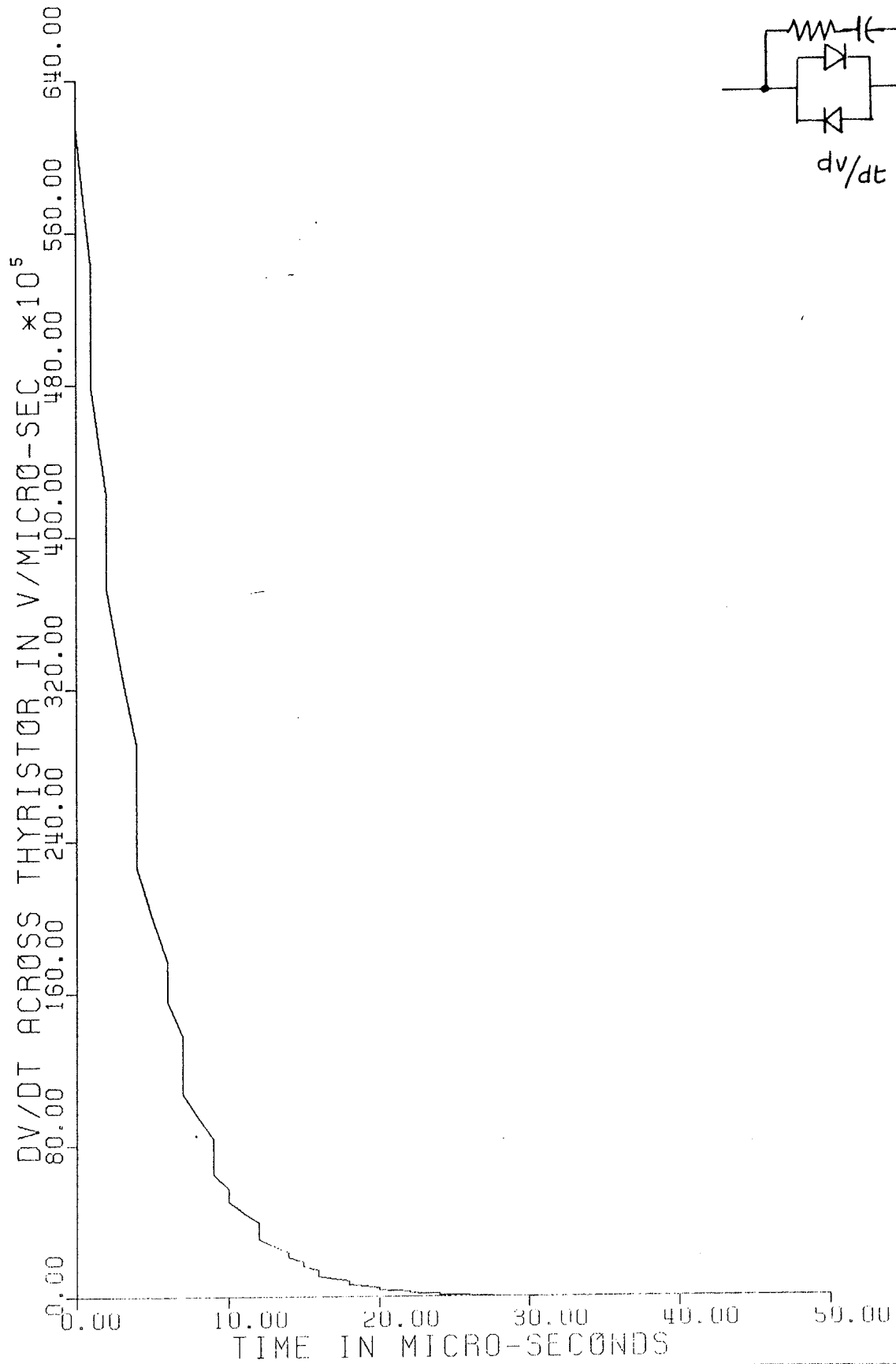


Fig. 4.6 b) Voltage rise across snubber circuit
(thyristors) following current inter-
ruption at $t = 0$

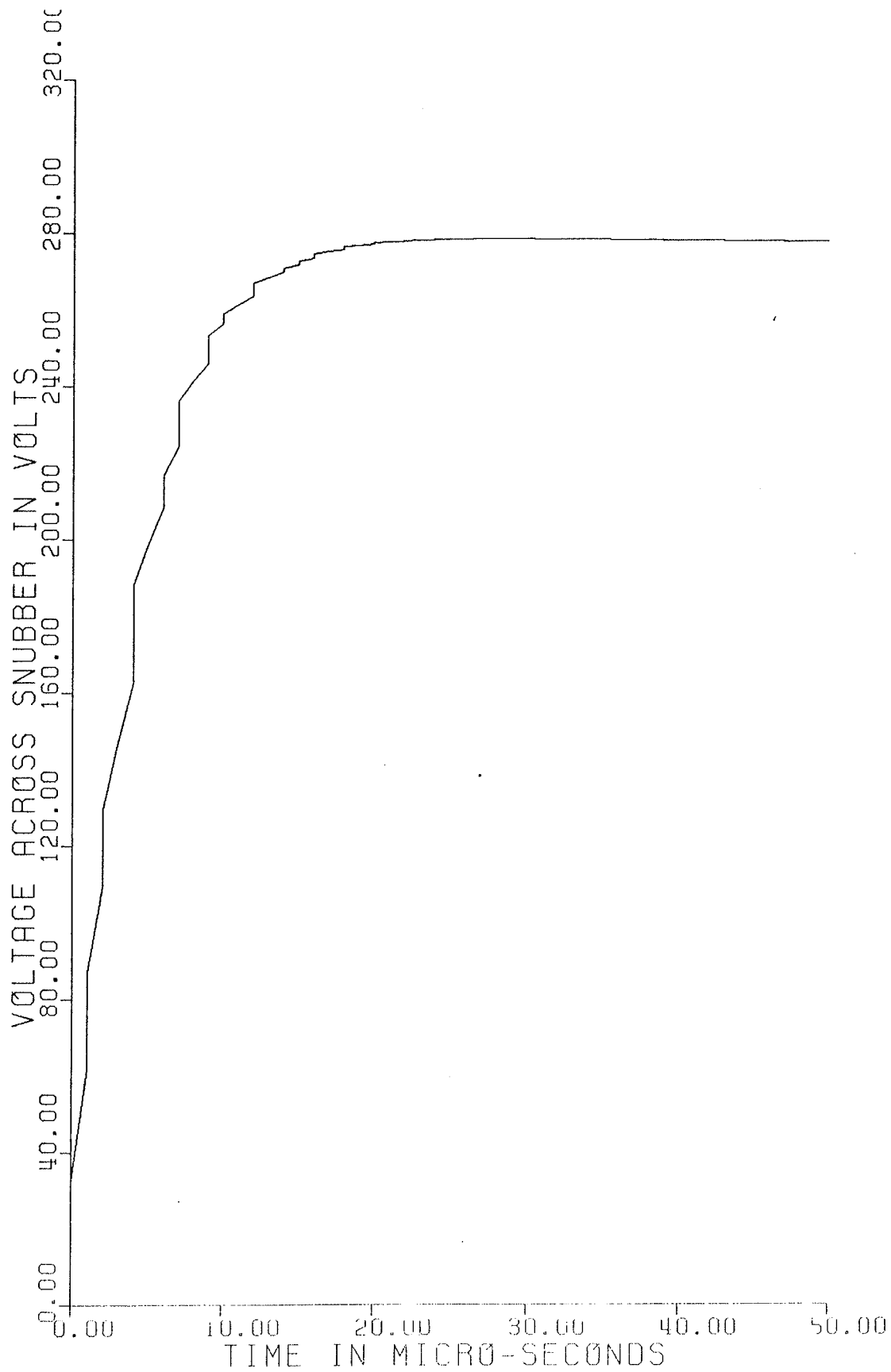
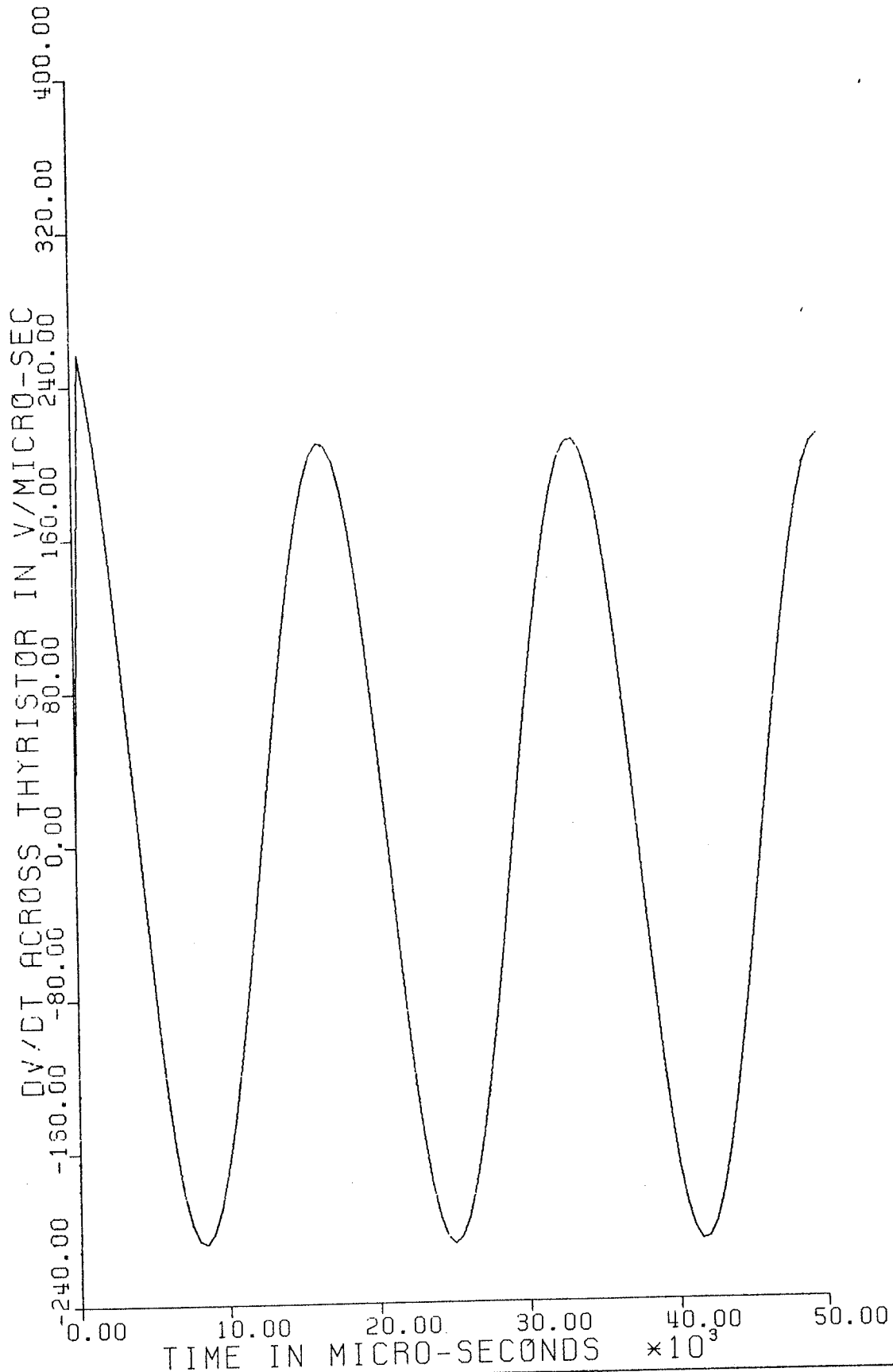


Fig. 4.7 Voltage across thyristors at turn off
(with snubber circuit)



4.5 Observations and Conclusions

TCTA-OFF

The results from the program TCTA-OFF which simulates the conditions when the current in the thyristor is switched off at natural zero during the first stage of the tap-change, shows that the recovery voltage across the thyristor reaches almost the peak steady state value instantaneously, causing a very large dv/dt across the thyristor.

1. The recovery voltage increases as the power factor changes to lower values and is observed to be maximum for zero power factor condition (Fig. 4.8(a)).
2. The recovery voltage is observed to increase as the coupling of the reactor increases to ideal coupling ($k=1$) as shown in Fig. 4.8(b).
3. The recovery voltage is higher when the tap changer is in bridging position.
4. The recovery voltage is higher when upper arm is in bridging position and is making a transition to step down.

TCTA-ON

TCTA-ON programme simulates the conditions when the selector-switch in the tap changer has moved to a new position and the arcing switch (SA) is closed and the thyristors are supplied with the gate signal. The firing angle can be controlled by the variable 'FIANG' in the program. Some of the results are shown in Figs. 4.4 and 4.5

1. The transient current in thyristors is lower when the tap arms are in nonbridging condition.
2. The transient current is higher when the upper arm thyristor is switched on in bridging position.

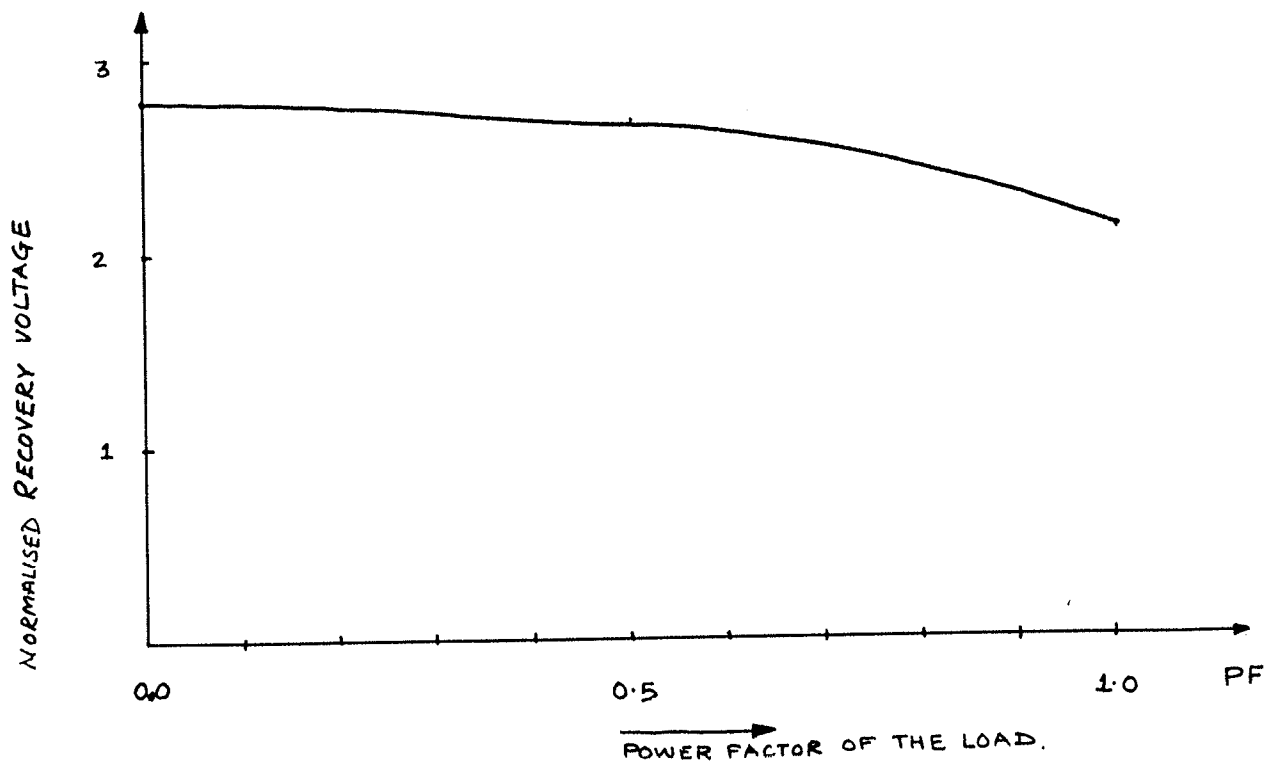


Fig. 4.8 a) Normalised recovery voltage across thyristors (with respect to tap voltage) as a function of load p.f.

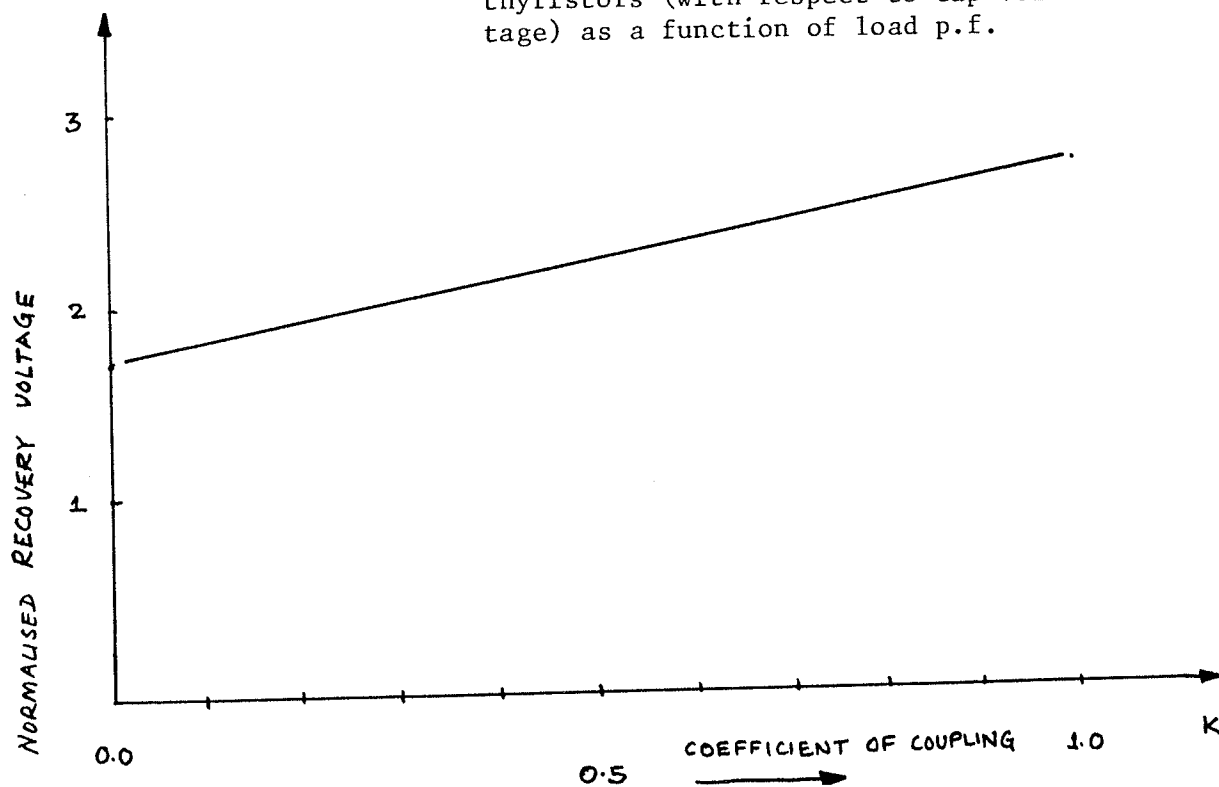


Fig. 4.8 b) Normalized recovery voltage across thyristors (with respect to tap voltage) as a function of k.

3. The transient current contains a dc bias which decays gradually to zero. The time constant for the dc component decay is dependent on RR_1 and RR_2 .
4. The current transient is sensitive to the firing angle of the thyristors. The exact nature of this behavior is rather complex as it is dependent on almost all parameters of the model.

TCTA-SNUB

As from the results of TCTA-SNUB, it was observed that the dv/dt is high across the thyristors at the instant of thyristor current switching off at natural current zero which necessitates the use of a snubber circuit for dv/dt protection. This snubber circuit is a series resistor-capacitor combination connected across the thyristors. Proper values for this snubber circuit can be selected for limiting the dv/dt across the thyristors within safe limits.

The results of Fig. 4.6 show the dv/dt and voltage across the thyristors for a typical values of $R = 200\Omega$ and $C = 1F$. The initial peak voltage is slightly higher than the steady state value.

CHAPTER V

DESIGN OF THE PROPOSED THYRISTOR ASSISTED ON LOAD TAP CHANGER

5.1 Introduction

The thyristors in the proposed scheme have to carry the tap current when the main switch opens and also before it closes again on a new selected tap. This requires the thyristors to be capable of withstanding the system voltage and thermal stresses due to current conduction. One of the main specification of concern for the thyristors is the thermal rating. Thyristor junction temperature should not exceed 125°C . This can be checked by a computer program developed for this purpose. The program calculates the junction temperature from Superposition Integral and uses thermal impedance characteristics of the thyristor. This technique of calculation is less conservative in estimating the junction temperature than other known methods [42].

The thyristors are also required to withstand high dv/dt at turn-off and are protected by snubber circuits made up of a series combination of resistor-capacitor (R-C) connected across the thyristors. The value of C limits the dv/dt and the value of R determines the damping of the circuit. The values of R and C are chosen to reduce the dv/dt below the specified limits without excessive voltage overshoot.

The firing circuit for applying firing signals to the thyristors uses a circuit to deliver gate current to the thyristors. The signal source is electrically isolated from the power thyristor by using a pulse transformer or an opto-coupler. A signal from auxiliary switch controls the start of gate current to the thyristor from the

firing circuit. The operation of these signals and the state of these thyristors is monitored by a logic integrated circuit (IC) which detects the loss of gate signals and thyristor failure in open or short condition. In the event, there is a breakdown of firing circuit a protection circuit is required to provide an emergency firing of thyristors. In the case of malfunction of any of the above an annunciation is required from monitoring circuit to stop tap changer movement.

5.2 Design Procedure

5.2.1 Selection of Thyristors:

Important factors for the selection of thyristors for the tap changer are:

Power dissipation and temperature rise

dv/dt limit

Voltage blocking

di/dt limit

Power Dissipation:

From the analysis of chapter IV we see that the maximum power dissipation in a thyristor occurs when the tap position moves from the common tap to higher bridging position. Under the worst condition the ac current passing through the thyristor could be unidirectional due to dc offset. This current condition is taken to be the maximum duty on the conducting thyristor for calculating the junction temperature.

The junction temperature is given by [42]

$$T_j(t) = P(0) \cdot r_t(t) + \int_0^t \{r_t(t-T) \cdot \frac{d}{dt} P(T)\} dT \quad (5.1)$$

$$= r_t(0) \cdot P(t) + \int_0^t \{P(t-T) \cdot \frac{d}{dt} r_t(T)\} dT \quad (5.2)$$

Where $P(0)$ is applied power at $t=0$

r_t is transient thermal impedance in $^{\circ}\text{C}/\text{W}$

Equation 5.1 has been used to simulate the convolution integral to calculate the junction temperature. The program listing is shown in Fig. 5.1(a). Junction temperatures can be calculated with different number of conduction cycles to see if the junction temperature exceeds the limit of 125°C. A sample plot for 750 A thyristor is shown in Fig. 5.1(b). The initial temperature of 25°C rises rapidly when 1600 A asymmetrical current flows through it. It reaches 58°C after 1 cycle of conduction, 60°C after 2 cycles and 76°C after 5 cycles.

dv/dt limit

When the tap current commutates from the main switch to the thyristor and the gate signals are removed then a sudden voltage appears across the thyristors at the current zero, resulting in very high dv/dt. This can be avoided by proper selection of resistance and capacitance values in the snubber circuit. The proper values are selected using TCTA-SNUB program which calculates the dv/dt and voltage overshoot.

Voltage Blocking

Another criterion to be met, for reliable operation, is that the reverse blocking voltage of the thyristor should be more than the recovery voltage due to stored charge in the thyristor. This is illustrated in Fig. 5.2.

di/dt limit

When the main switch opens the current through it must commute to the thyristors. Since conduction in a thyristor is not instantaneous there is a transient turn-on voltage across the thyristor. The thyristor, therefore, should be capable of withstanding high di/dt and should possess low transient turn-on voltage characteristic.

****CONTINUOUS SYSTEM MODELING PROGRAM****

*** VERSION 1.3 ***

```

/      DIMENSION RD(1000)
      FIXED I,J,K
INITIAL
      COUNT=0.0
      IM=SQRT(2.0)*1600.0
      W=120*3.141619
      V=3.0
DYNAMIC
      JT=25.0
      TAU=0.0
      FUNCTION R=(0.0,0.0),(0.001,0.004),(0.007,0.005),(0.008,0.009)...
      , (0.01,0.009),(0.03,0.01),(0.07,0.014),(0.09,0.016)...
      , (0.1,0.02)
      I=TIME/0.0001+1.0
NOSORT
      RO=AFGEN(R,TIME)
NOSORT
      ICHECK=IM*(1.0-COS(W*TIME))
      V=3.0
      IM=SQRT(2.0)*1600.0
      W=120.0*3.14169
      C=IM*W
      IF (TIME.GT.0.1000) C=0.0
      RD(I)=RO
      IF (COUNT.NE.10.0) GO TO 10
20  J=(TIME-TAU)/0.0001+1.0
      RR=RD(J)
      W=120*3.14169
      TOT=TAU*W
      S=SIN(TOT)
      IF (ICHECK.LE.1000) V=1.5
      IF (ICHECK.GT.1000.AND.ICHECK.LE.4000) V=2.5
      INT=C*RR*S*.0001*V
      JT=JT+INT
      IF (J.EQ.1.0) GO TO 10
      IF (KEEP.EQ.1) TAU=TAU+0.0001
      GO TO 20
10  IF (KEEP.EQ.1) COUNT=COUNT+1.0
      IF (COUNT.EQ.11) COUNT=1.0
88  FORMAT(1H,2F16.6)
      TERMINAL
      TIMER DELT=0.0001,FINTIM=0.10,OUTDEL=0.0010
      PRTPLOT JT
END
STOP

```

Fig. 5.1 a) Function temperature program listing

	MINIMUM	JT	VERSUS TIME	MAXIMUM
	2.5000E+01			1.4840E+
TIME	JT	I		I
.0	2.5000E+01	+		
.0000E-03	2.5402E+01	+		
.0000E-03	2.7475E+01	-+		
.0000E-03	3.5295E+01	-----+		
.0000E-03	4.3447E+01	-----++		
.0000E-03	5.2642E+01	-----++++		
.0000E-03	6.1632E+01	-----+++++		
.0000E-03	7.8210E+01	-----++++++		
.0000E-03	8.5341E+01	-----++++++		
.0000E-03	9.1962E+01	-----++++++		
.0000E-02	9.7982E+01	-----++++++		
.1000E-02	8.9388E+01	-----++++++		
.2000E-02	9.1611E+01	-----++++++		
.3000E-02	9.1137E+01	-----++++++		
.4000E-02	8.8656E+01	-----++++++		
.5000E-02	6.0720E+01	-----++++		
.6000E-02	5.7642E+01	-----++++		
.7000E-02	5.4417E+01	-----++++	1 Cycle	
.8000E-02	5.1512E+01	-----++++		
.9000E-02	4.9370E+01	-----++++		
.0000E-02	6.3840E+01	-----++++		
.1000E-02	6.4166E+01	-----++++		
.2000E-02	6.6568E+01	-----++++		
.3000E-02	7.0762E+01	-----++++		
.4000E-02	8.6436E+01	-----++++		
.5000E-02	9.3575E+01	-----++++		
.6000E-02	1.0038E+02	-----++++		
.7000E-02	9.2446E+01	-----++++		
.8000E-02	9.5434E+01	-----++++		
.9000E-02	9.6387E+01	-----++++		
.0000E-02	9.5221E+01	-----++++		
.1000E-02	6.5286E+01	-----++++		
.2000E-02	6.2595E+01	-----++++		
.3000E-02	5.9487E+01	-----++++	2	
.4000E-02	5.6443E+01	-----++++		
.5000E-02	5.3948E+01	-----++++		
.6000E-02	7.0653E+01	-----++++		
.7000E-02	7.0064E+01	-----++++		
.8000E-02	7.1651E+01	-----++++		
.9000E-02	7.5261E+01	-----++++		
.0000E-02	9.1571E+01	-----++++		
.1000E-02	9.8960E+01	-----++++		
.2000E-02	1.0655E+02	-----++++		
.3000E-02	1.1335E+02	-----++++		
.4000E-02	1.0294E+02	-----++++		
.5000E-02	1.0536E+02	-----++++		
.6000E-02	1.0563E+02	-----++++		
.7000E-02	1.0379E+02	-----++++		
.8000E-02	7.0103E+01	-----++++		
.9000E-02	6.7227E+01	-----++++		
.0000E-02	6.4089E+01	-----++++		

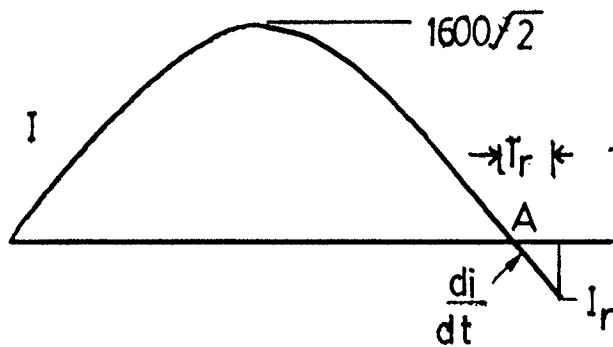
1 Cycle

2

Fig. 5.1 b) Junction temperature output

	MINIMUM	JT	VERSUS TIME	MAXIMUM
	2.5000E+01			1.4840E+01
TIME	JT	I		T
1000E-02	6.1182E+01	-----+		
2000E-02	5.8961E+01	-----+		
3000E-02	7.9641E+01	-----+		
4000E-02	7.9778E+01	-----+		
5000E-02	8.2067E+01	-----+		
6000E-02	8.6276E+01	-----+		
7000E-02	1.0526E+02	-----+		
8000E-02	1.1282E+02	-----+		
9000E-02	1.2026E+02	-----+		
0000E-02	1.2660E+02	-----+		
1000E-02	1.1340E+02	-----+		
2000E-02	1.1511E+02	-----+		
3000E-02	1.1463E+02	-----+		
4000E-02	1.1214E+02	-----+		
5000E-02	7.4827E+01	-----+		
6000E-02	7.1832E+01	-----+		
7000E-02	6.8707E+01	-----+		
8000E-02	6.5970E+01	-----+		
9000E-02	6.4052E+01	-----+		
0000E-02	8.8815E+01	-----+		
1000E-02	8.9663E+01	-----+		
2000E-02	9.2624E+01	-----+		
3000E-02	9.7363E+01	-----+		
4000E-02	1.1895E+02	-----+		
5000E-02	1.2662E+02	-----+		
6000E-02	1.3379E+02	-----+		
7000E-02	1.2050E+02	-----+		
8000E-02	1.2360E+02	-----+		
9000E-02	1.2461E+02	-----+		
0000E-02	1.2348E+02	-----+		
1000E-02	8.2234E+01	-----+		
2000E-02	7.9543E+01	-----+		
3000E-02	7.6434E+01	-----+		
4000E-02	7.3404E+01	-----+		
5000E-02	7.0892E+01	-----+		
6000E-02	9.8869E+01	-----+		
7000E-02	9.8260E+01	-----+		
8000E-02	9.9825E+01	-----+		
9000E-02	1.0345E+02	-----+		
0000E-02	1.2538E+02	-----+		
1000E-02	1.3281E+02	-----+		
2000E-02	1.4073E+02	-----+		
3000E-02	1.4840E+02	-----+		
4000E-02	1.3346E+02	-----+		
5000E-02	1.3781E+02	-----+		
6000E-02	1.4061E+02	-----+		
7000E-02	1.4178E+02	-----+		
8000E-02	9.4949E+01	-----+		
9000E-02	9.4077E+01	-----+		
0000E-01	9.2834E+01	-----+		

Fig. 5.1 b) Junction temperature output



$$i = 1600 \sqrt{2} \sin(\omega t)$$

$$\left. \frac{di}{dt} \right|_{\text{at A}} = 1600 \sqrt{2} \times 377 = 0.853 \times 10^6 \text{ A/S}$$

$$T_r = I_r / \frac{di}{dt}, \quad q_r = \frac{T_r}{2} \cdot I_r = \frac{1}{2} \frac{I_r^2}{\frac{di}{dt}}$$

$$I_r = \sqrt{2 \times 50 \times 10^{-6} \times 0.853 \times 10^6}$$

$$= 9.23 \text{ A}$$

Recover voltage should be less than device rated reverse blocking

$$R < \frac{V_s}{I_r}$$

$$R < \frac{1500}{9.23} = 162.5$$

Fig. 5.2 SCR recovery characteristic

5.3 Voltage Blocking

The voltage blocking requirement is studied by analysing the bridging position in TCTA-OFF and TCTA-SNUB program. This gives us the worst forward and reverse voltages on the thyristor during the tap change. The thyristor voltage blocking rating should be significantly higher than that which occurs under the worst condition.

5.4 Firing Circuit

The firing circuit schematic is shown in Fig. 5.3 it consists of an IC clock generator (555) at 10 kHz the output of which is amplified by transistors to drive the gate. These signals are controlled by an auxiliary switch. When the tap changer is in idle situation the gate signals are provided to the thyristors. During the tap change when the main switch opens, the thyristors keep on getting the gate signals. After the opening of main switch and allowing sufficient time for the commutation to take place from the main switch to the thyristors the auxiliary switch opens to block the gate current. This is illustrated in Fig. 5.3. The output of clock is ANDed with auxiliary signal. The auxiliary switch controls the signal c to the gates of the thyristors.

5.5 Power Supply

Low voltage power supply (5Vdc., 2A) is required for firing, monitoring and annunciation circuits. This is derived from 120 V ac available in the control panel. Another power supply of 24 V is made for gating 70 A thyristors. A regulating transistor is used to regulate the voltage. In the final design of tap changer this supply can be derived from one of the taps in the selector head.

5.6 Design Changes

In the existing tap changer the arcing switch opens within

about 0.4 cycle which is too fast to turn off current in the thyristor. This timing therefore has to be slowed down to greater than 0.6 cycle. Changes were, therefore, made to achieve this.

5.7 Monitoring Devices

For constantly monitoring the satisfactory operation of the tap changer we need to monitor the gate signals and thyristor failure conditions. As shown in Figs. 5.4, 5.5 and 5.6 the monitoring circuit detects.

Loss of gate current

Thyristor failure in short

Thyristor failure in open

5.7.1 Loss of Gate Current

This can be detected by voltage sensing devices when the auxiliary switch is closed. A loss in voltage at the pulse transformer when the auxiliary switch is closed would give a signal for fault condition. A schematic of this circuit is shown in Fig. 5.4.

Two monostables are connected across collector of output transistors for firing circuit. The firing pulses of 10 kHz produce pulses of duration greater than 0.1 ms. Under normal condition of operation when firing pulses in both the transistors are present the monostable output Q is low. The signal c is therefore high and since d is low signal e remains low. But in case the firing pulses of channel 1 fail due to some reason. The output a goes high, signal c goes low and signal e goes high to give indication that the firing pulses have failed and thus the tap change should be avoided. In the event both the channels fail the logic still works.

5.7.2 Thyristor Failure in Short

When a thyristor in the tap changer is destroyed in short the

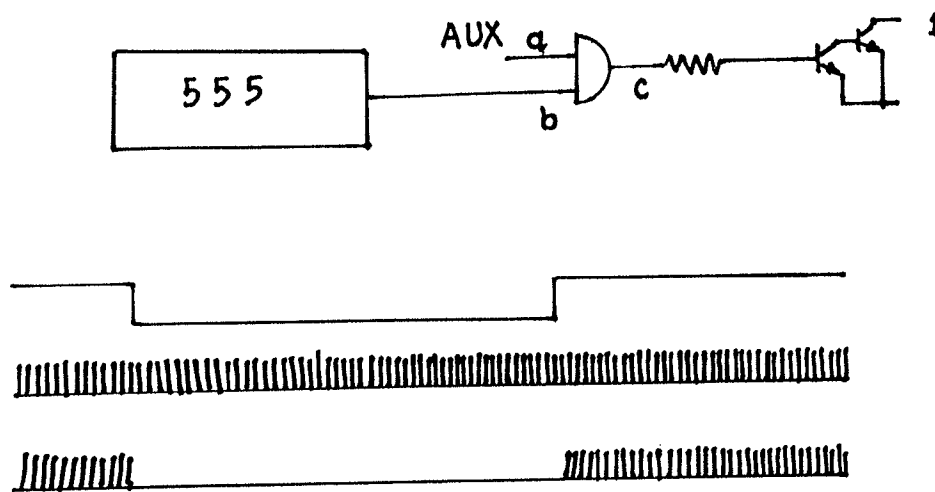


Fig. 5.3 Firing circuit schematic

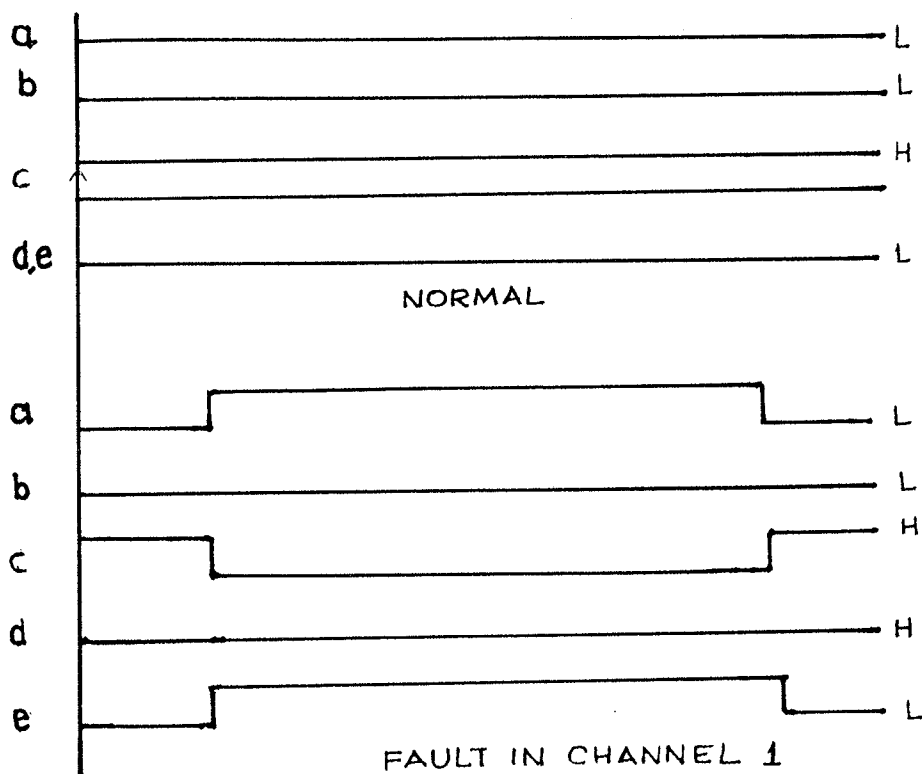
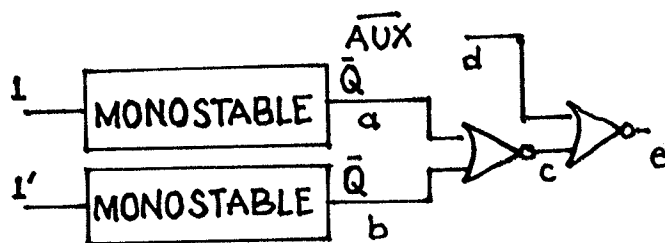


Fig. 5.4 Monitoring logic for gate current

tap changer acts like the existing tap changer and the arcing contact breaks the tapcurrent. This condition can easily be detected by the loss of voltage across thyristor during the tapchange by a logic circuit. A schematic of this logic circuit is shown in Fig. 5.5. The auxiliary switch signal sets a flip flop (7476) and produces a monostable (74123) pulse when it opens during the opening of the diverters. The monostable pulse (≈ 15 ms) acts like a blanking pulse, because during this interval, for normal operation, the thyristor stops conducting and voltage appears across the thyristors. This voltage resets the flip-flop output c through an opto coupler. The signal d, e remains low indicating healthy condition. The signal d is ANDed with inverted auxiliary signal to eliminate erroneous signal at the closing of the auxiliary contact due to contact bounce. Under thyristor short condition there is no voltage across the thyristors to reset the flip flop. The signals d and e go high at the end of blanking pulse b to indicate thyristor short condition.

5.7.3 Thyristor Failure in Open

If the thyristor is not conducting when it is supposed to, it could be either due to the loss of gate current or due to the thyristor failure in open. The first condition can be overcome by having another circuit to supply the gate current when this happens. The second condition is highly undesirable because it leads to severe arcing at the main contact. The logic circuit must, therefore, be able to differentiate between these two conditions. This can be achieved by sensing the voltage across the main contact, which under normal conditions should always be negligible. The output signal from the logic circuit should give a trip signal to the circuit breaker to switch off the tap changer drive to protect the main contacts. Such a happening is

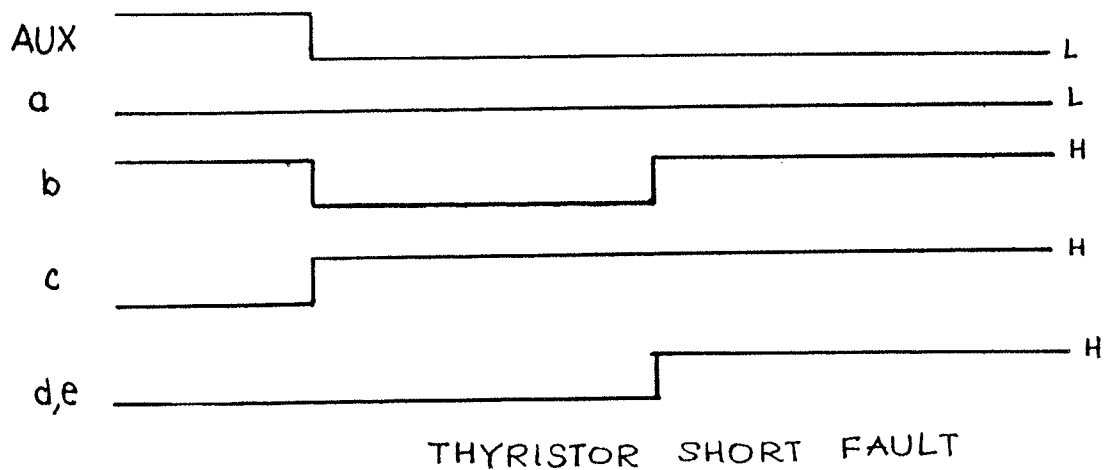
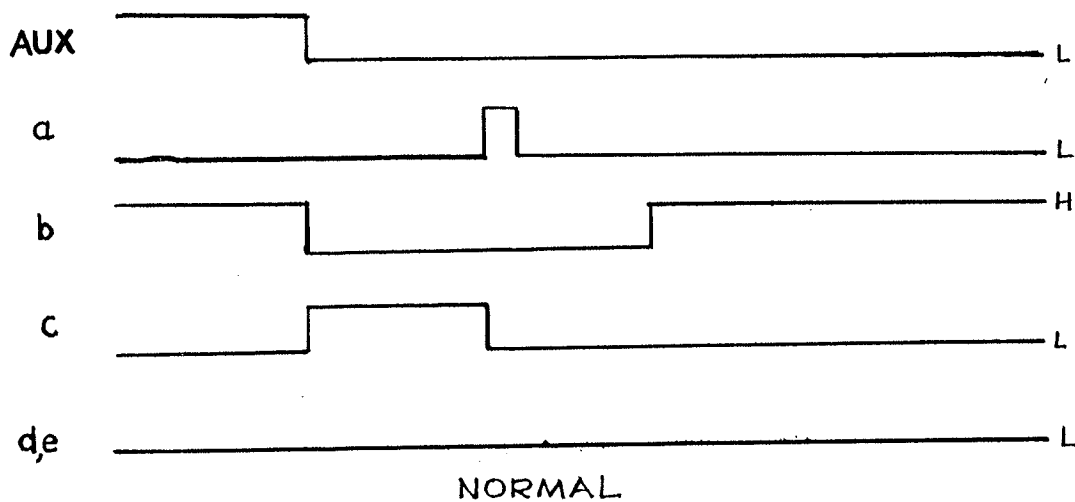
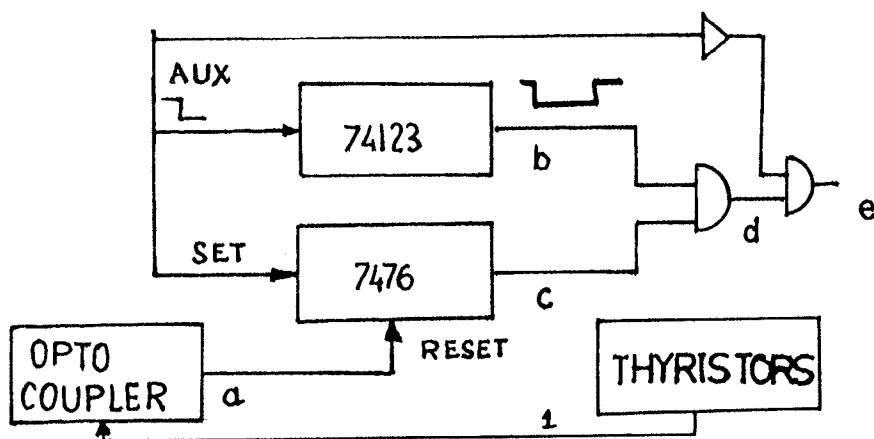


Fig. 5.5 Monitoring circuit logic for thyristors (short condition)

expected to be very rare. A schematic of this circuit is shown in Fig. 5.6. The main voltage is monitored by an opto coupler. Under normal operation the main switch opens when auxiliary signal is high and there is no voltage developed across the main switch as the current commutates to the thyristor branch. When the thyristors have failed in open, as the main switch opens, the tap current is interrupted causing arcing followed by system voltage appearing across the main switch making signal b high. The signal d goes high to indicate the thyristor open condition and to disable the tap change.

5.7.4 Temperature Control

The thyristors used on the proposed scheme are overrated for the current, since the current carried by the thyristors is only for very few cycles. If the ambient temperature in the tap changer oil rises in excess of 70-80°C the junction temperature of 125°C may be exceeded and the thyristors may be damaged. Therefore, a temperature detecting circuit using a temperature sensitive element is included to disable the tap changer should the temperature exceed beyond 80°C.

5.7.5 Auxiliary Switch Failure

A microswitch or ordinary contacts can be used for auxiliary switch for the control circuit. The reliability of this auxiliary switch is essential. It can be increased by paralleling a few of them as their failure in open condition is more likely.

5.8 Redundancy

It is seen that redundancy in the circuit and the power supply will increase the reliability of the tap changer. Care has to be taken in the design stage of make the tap changer as reliable as possible by having an alternate power supply to take over in the event the irregular power supply fails.

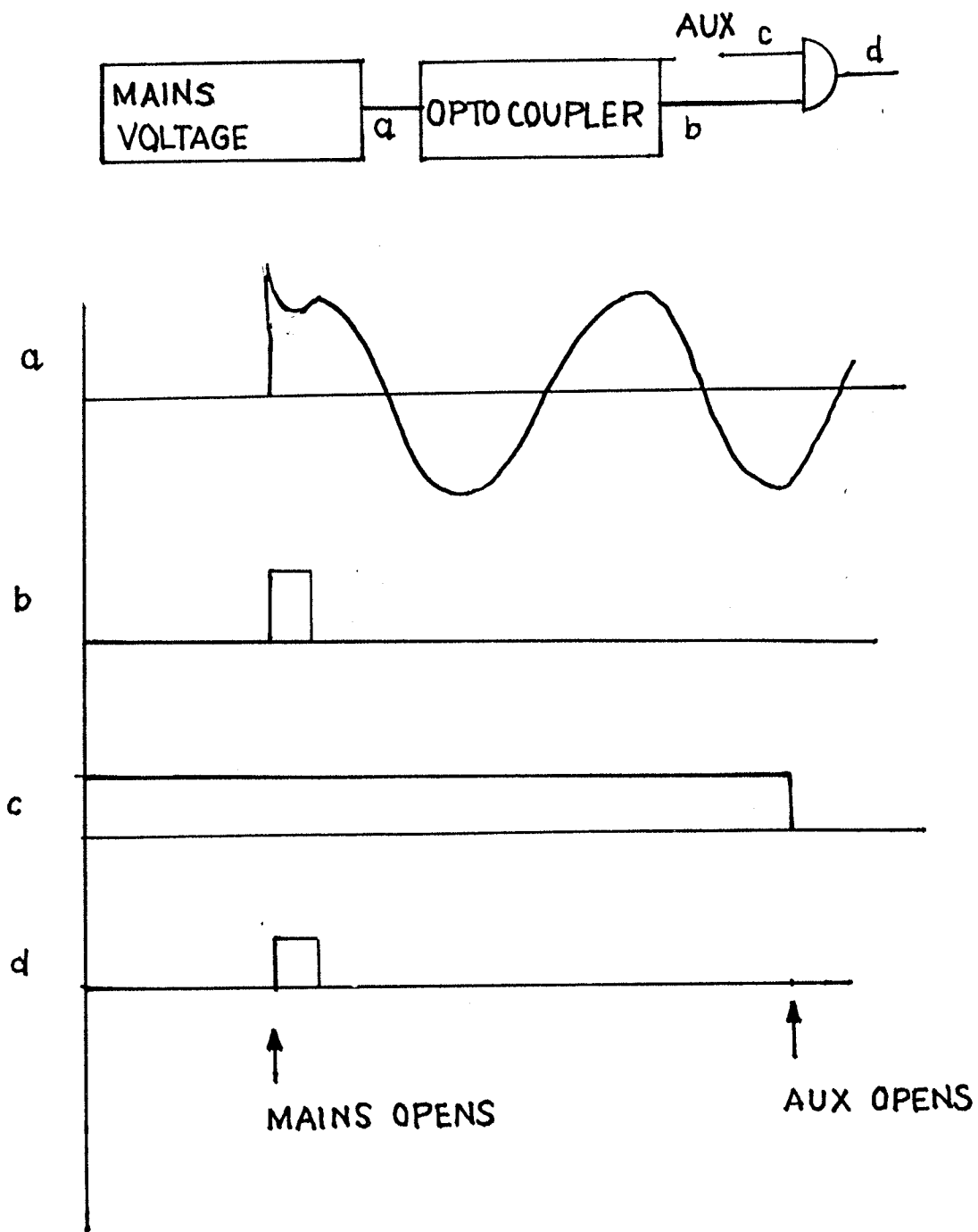


Fig. 5.6 Monitoring circuit logic for thyristors (open condition)

CHAPTER VI

PROTOTYPE FABRICATION AND TESTS

6.1 Fabrication of the prototype

Chapter V gives the general design requirements for the proposed scheme. For making a prototype first attempt was made for 40 A and then for 170 A load current. Figure 6.1 shows the top view of the control circuit for 40 A prototype. The figure shows integrated circuit chips and transistors mounted on a breadboard. The circuit uses light emitting diodes to indicate fault condition by the monitoring circuit. Figure 6.2 shows the wired prototype of an actual Federal Pioneer tap-changer for 40 A testing. The firing circuit signals were wired through a shielded wire to the thyristors which were located on top of the tap changer chamber. The voltage signals from the main switch and the thyristors are brought down by using shielded wire to the breadboard. In this arrangement the circuit was prone to stray pick ups but was found to work satisfactory.

Figure 6.3 gives the complete circuit diagram of control circuit for the 170 A prototype. It is based on the design discussed earlier in Chapter V. The clock signal generated by 555 is ANDed with auxiliary signal and AND gate (7408) to drive darlington pair (MJE 100) transistors. For logic circuit the NOR (9402), J.K. flip flop (7476) and monostables (74123) have been used to monitor proper operation of the tap changer. The opto couplers (2N29A) are used to provide TTL compatible signal to the logic gates. The annunciation signals provided by the logic circuits discussed earlier set SCR's to conduct to provide a permanent signal to light the light emitting diode. Figure 6.4 shows the printed circuit layout of the control circuit. The IC's

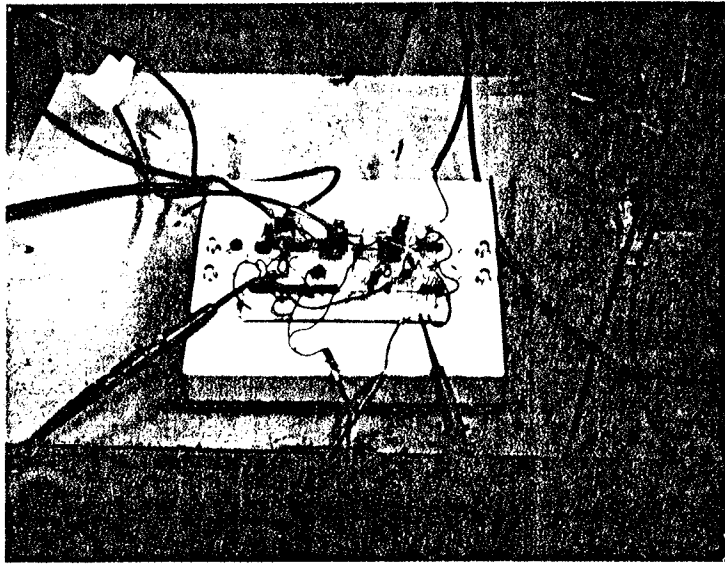


Fig. 6.1 Top view of breadboarded control circuit for 40 A load

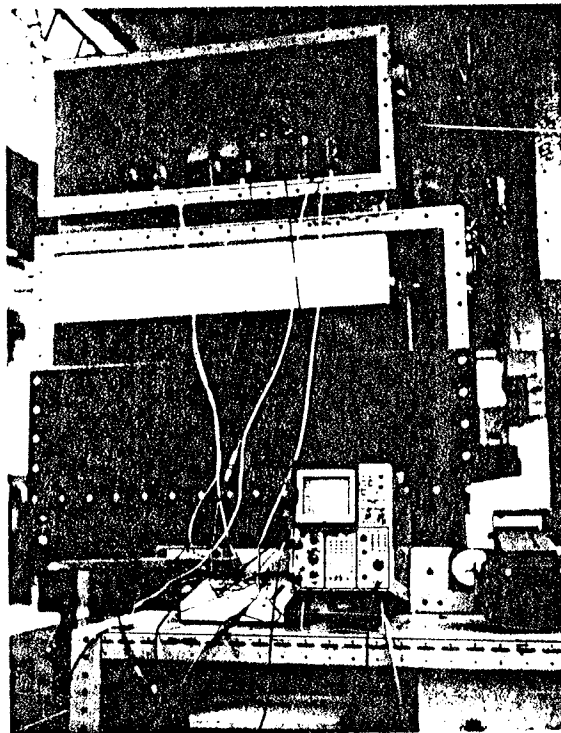


Fig. 6.2 Factory set up to test prototype for 40 A load

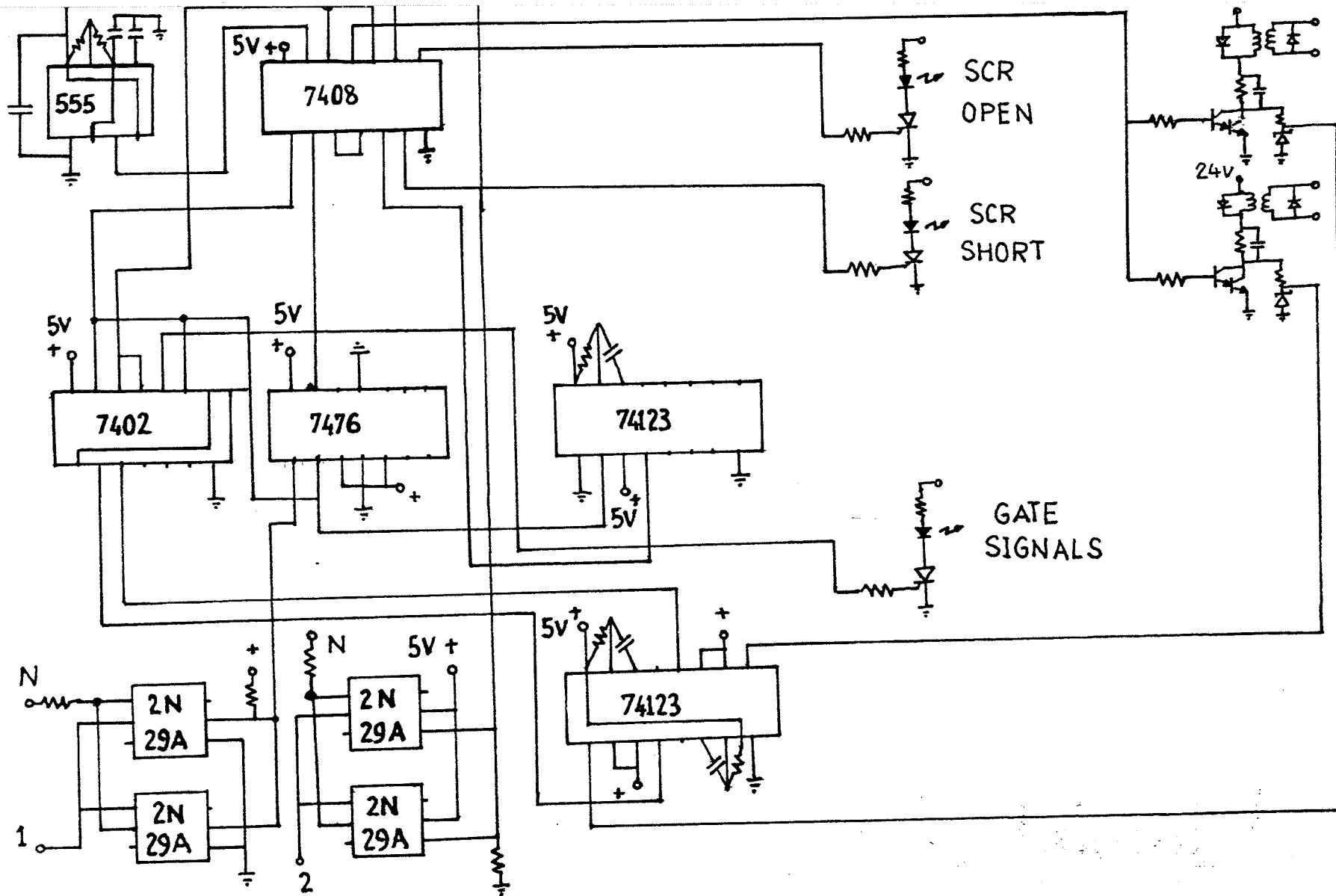


Fig. 6.3 Circuit diagram for 170 A prototype

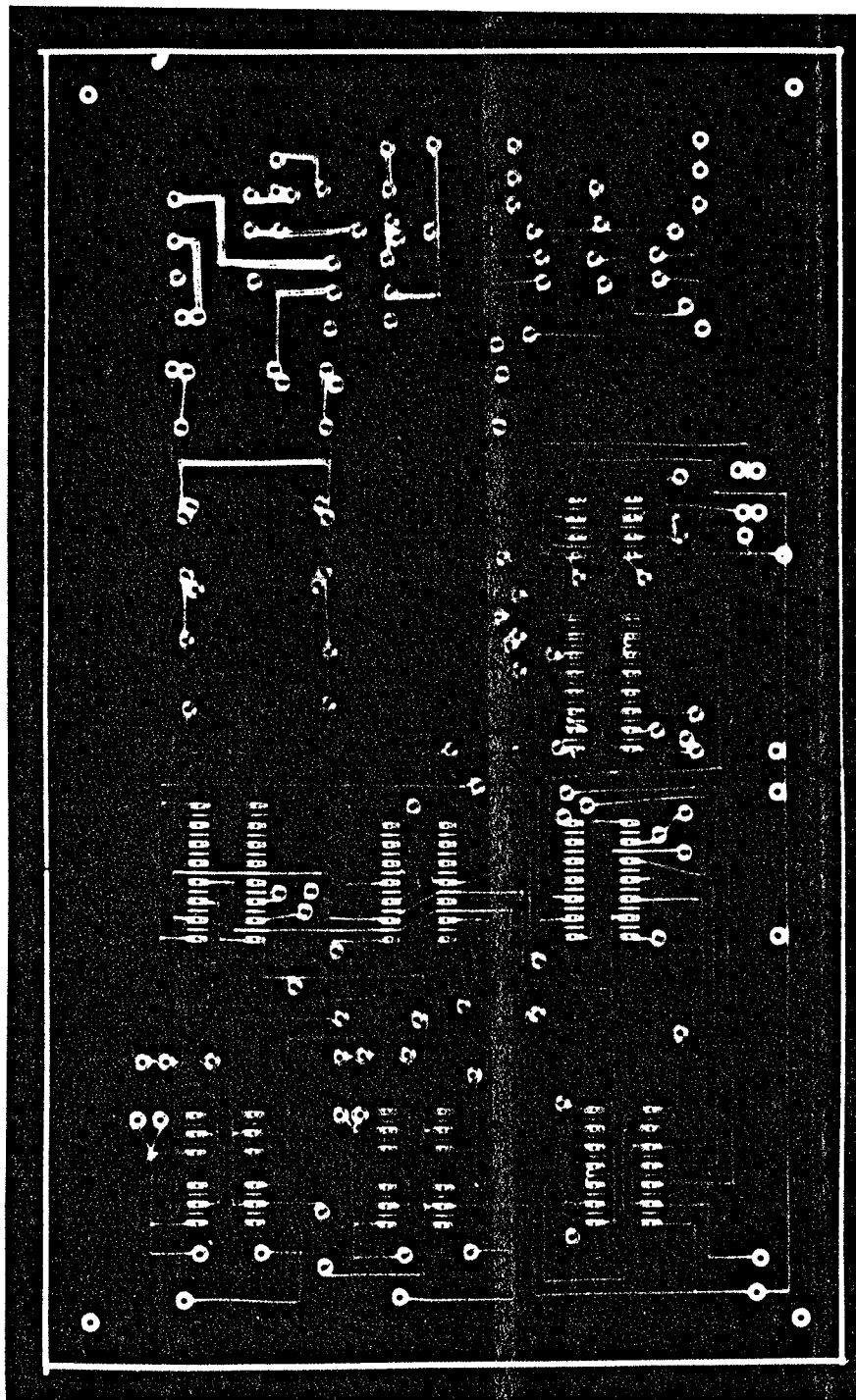


Fig. 6.4 Printed circuit board for control circuit

are mounted on IC sockets for easy maintenance.

Figure 6.5 shows the front, back and top view of the thyristor assisted tap-changer control circuit box. The front panel has three LEDs for annunciation - the thyristor short condition, thyristor open condition and the no gate signals condition. There is a switch which resets this indicator LED by cutting its power supply. The front panel also includes the power supply switch and its indicator lamp. The circuit should always be switched on during tap changer operation. The back panel has a fuse (2A) for the power supply circuit. It has terminals for:

1. gate signals for both antiparallel thyristors,
2. Auxiliary switch,
3. Main voltage, and
4. Thyristor voltage.

The darlington pair power transistor are also mounted on the back panel. The top view of thyristor assisted tap changer control circuit shows the power transformer and power supply circuit mounted on the left hand side. The printed circuit is mounted on the right hand side.

6.2 Simulated Test Set Up

Figure 6.6 shows the circuit arrangement for the simulated test set-up. One of the arcing tip is insulated and an antiparallel thyristor is inserted as shown in the figure. A series resistor capacitor ($R=10\ \Omega$, $C=0.1\ \mu F$) is connected across the thyristor as a snubber circuit to suppress the dv/dt stress on the thyristor. A power supply 60 V for 40 A testing or 440 volts for 170 A testing is connected in series with the modified diverter and a shorted transformer. The thyristor rating was 70 A. Figures 6.7(a),(b) show the unmodified and

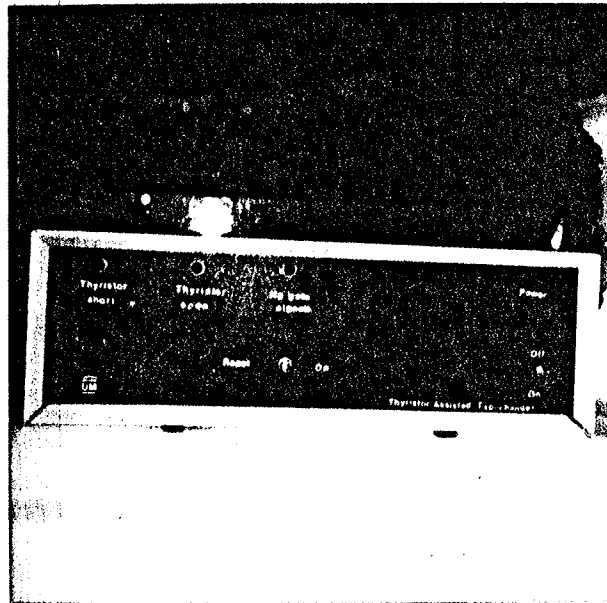


Fig. 6.5 a) Front view of thyristor assisted tap changer control circuit box

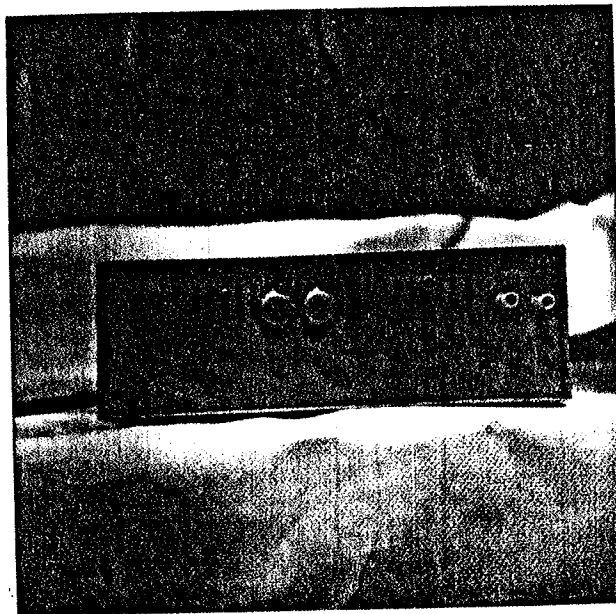


Fig. 6.5 b) Back view of thyristor assisted tap changer control circuit box

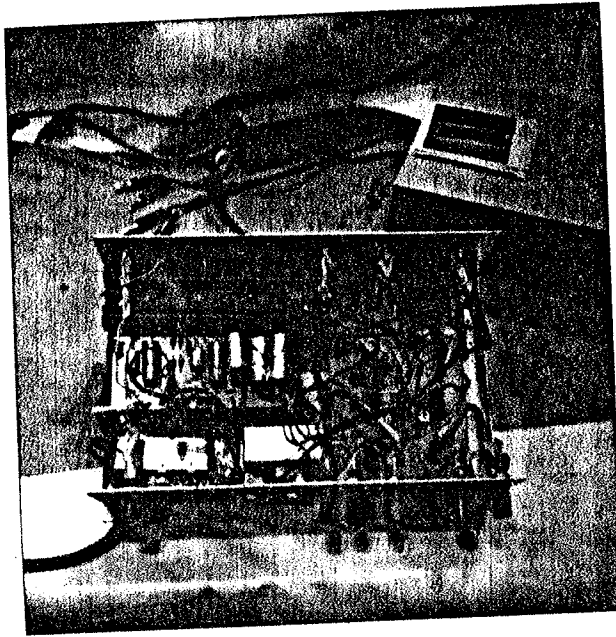


Fig. 6.5 c) Top view of thyristor assisted
tap changer control circuit box

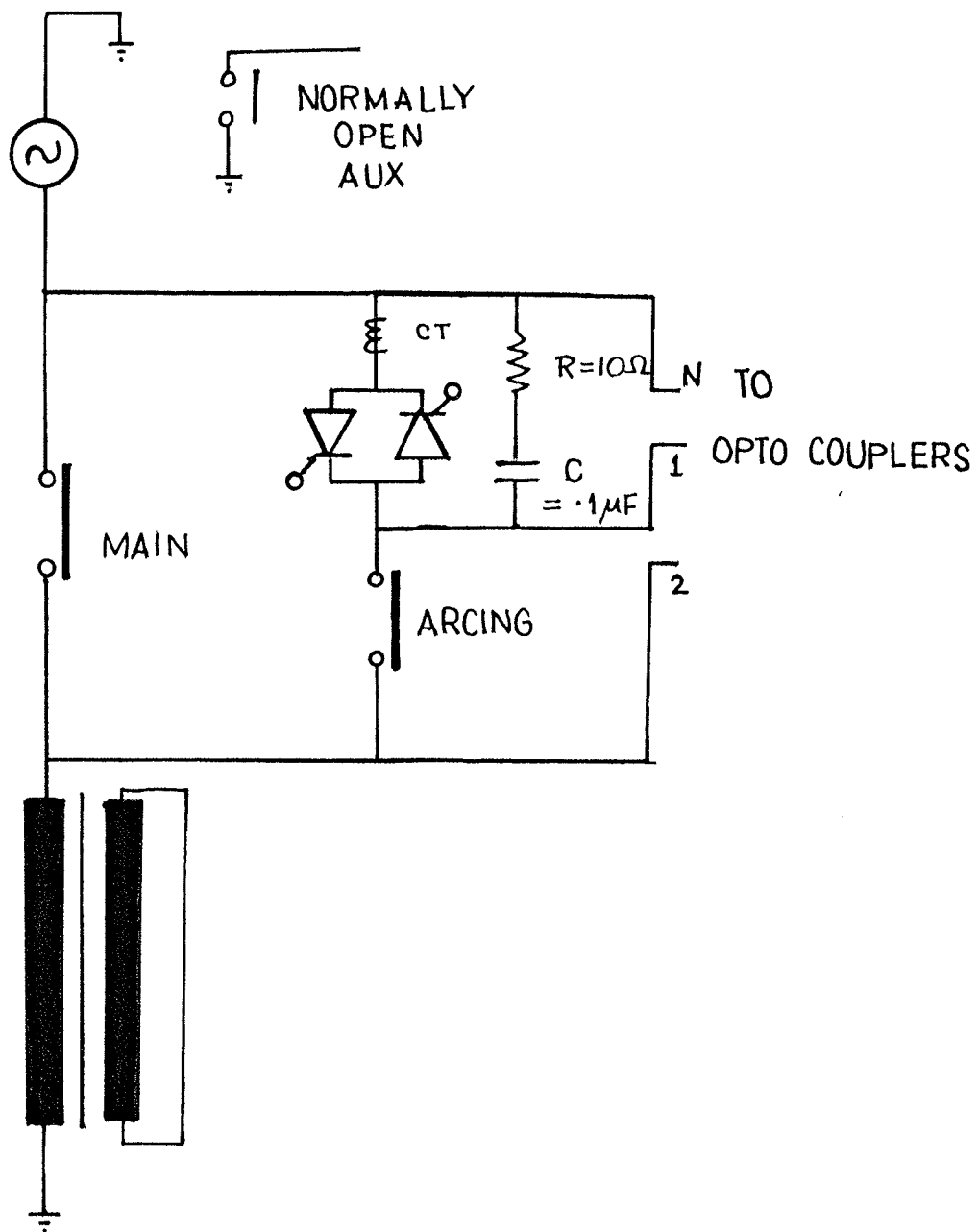


Fig. 6.6 Simulation test set up

modified diverter. The modified diverter has an auxiliary switch in the form of a microswitch attached to the main contact as shown in Fig. 6.7b which is open when the diverters are in normal idle condition. Thus the open auxiliary switch corresponds to logic 1. The wires connected to the main switch and thyristors go to opto-couplers for monitoring circuit.

A storage oscilloscope was used to record the waveforms. For triggering, the oscilloscope signals from auxiliary switch and other phase diverters were used.

6.3 Simulated Test results

The prototype developed in the laboratory was tested in Federal Pioneer premises on an actual tap changer for 40 A and 170 A current interruption. Figure 6.7 shows the thyristor voltage and current waveforms for 10 A and 40 A at current interruption. As the main switch opens the current is commutated to the thyristors. The thyristor current ceases at next current zero and then a voltage appears across the thyristors. The selector switch next moves and disconnects the supply voltage and the voltage across the thyristors remain floating. The circuit behaved as expected.

Figure 6.9 shows the current and voltage waveforms through the thyristors for 40 A and 10 A respectively at the current making. This current signal is sensed by a shunt in series with thyristors. The waveform shows that the current signal is zero and the voltage across the thyristors appear when the arcing switch closes. The current starts flowing through the thyristor when the auxiliary switch closes and allows the gate signals from the control circuit to the thyristors. Observe that the voltage across thyristors collapses as soon as they conduct. The current is commutated to the main switch

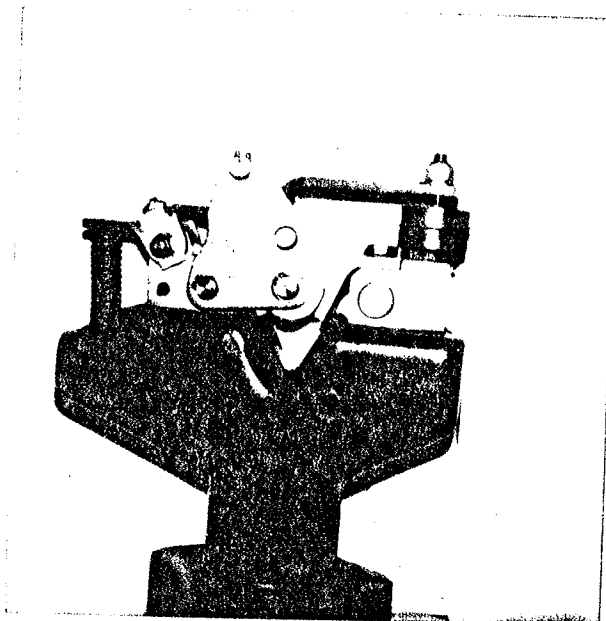


Fig. 6.7 a) Unmodified diverter

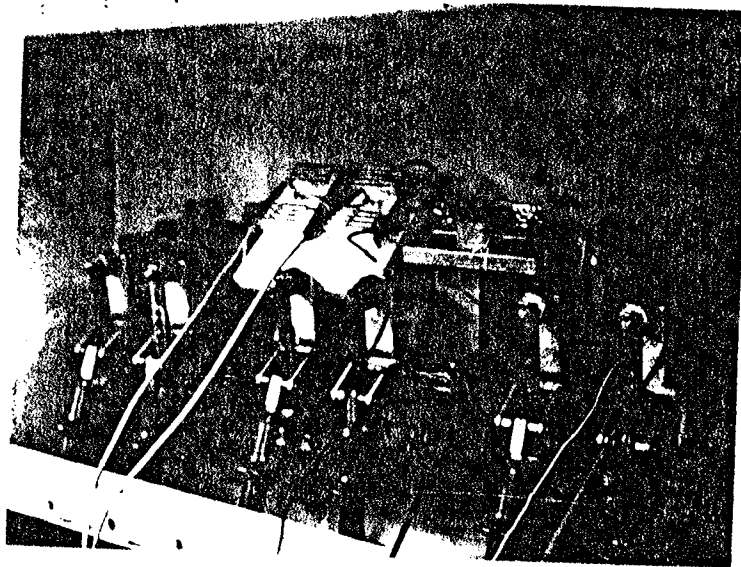
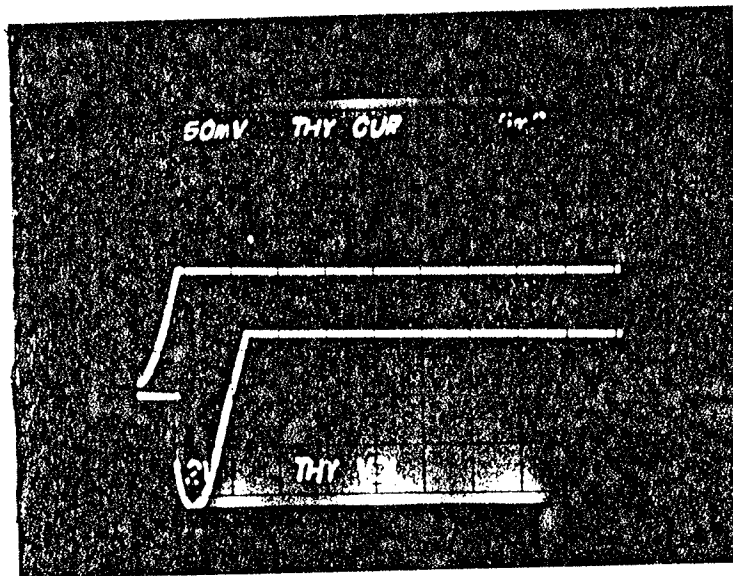


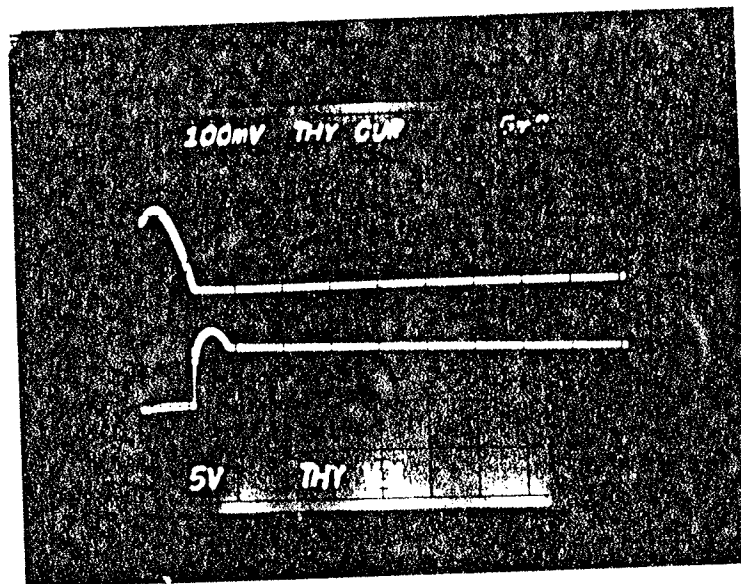
Fig. 6.7 b) Modified diverters with auxiliary switch and thyristors



i_T

v_T

Fig. 6.8 a) Thyristor current and voltage at current breaking operation for 30 A



i_T

v_T

Fig. 6.8 b) Thyristor current and voltage at current breaking operation for 40 A

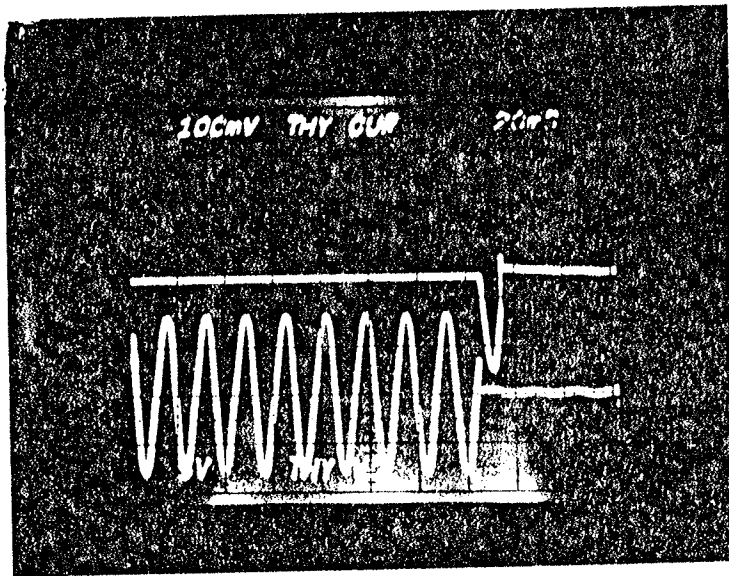


Fig. 6.9 a) Thyristor current and voltage at current making operation for 40 A

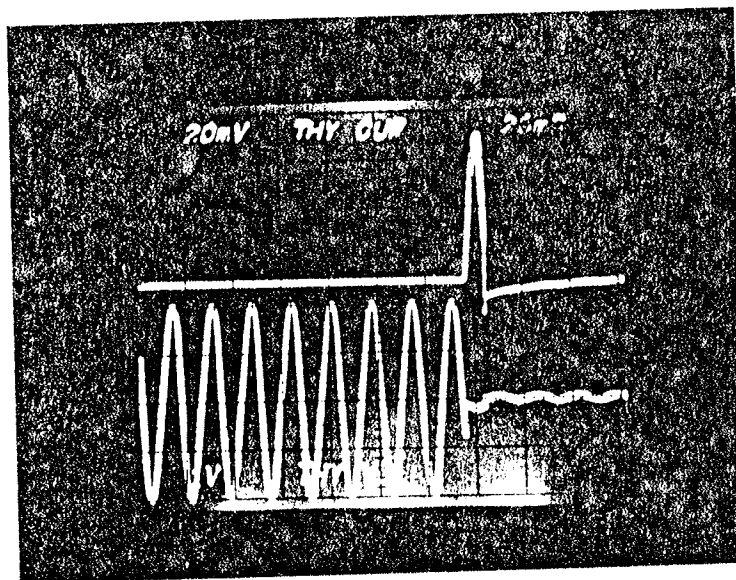


Fig. 6.9 b) Thyristor current and voltage at current making operation for 10 A

from the thyristor when the main switch closes.

Figures 6.10(a),(b), show the current making and breaking condition waveforms for 20 A. Notice that the current through the thyristors is less than one cycle and thus exerts light duty on the thyristors. Figures 6.11(a),(b) show the current breaking waveforms for 10 A and 20 A respectively.

Figure 6.12(a) shows current through thyristors at current break at 170 A. At this current break it is to be observed that no arcing occurs in the proposed scheme whereas considerable arcing occurs in the original tap changer. The current waveforms are monitored by a CT placed in the thyristor branch.

Figures 6.13(a),(b) show again current through thyristors at current making for 50 A and 170 A respectively.

Figures 14(a),(b) show the uppertrace of auxiliary switch changeover at the current breaking when a thyristor has failed in open condition. The lower trace of the main switch voltage shows the arcing voltage switch appears when the main switch voltage shows the arcing voltage which appears when the main switch opens the current of 170 A. The supply voltage appears across main switch after the arcing ceases.

Figures 6.15(a),(b) show the uppertrace of auxiliary switch changeover at current break at main switch and arcing switch respectively. In Fig. 6.15(a) the lower trace show the LED signal when arcing voltage appears across the main contact. This signal triggers a SCR ON to give fault annunciation. Similarly in Fig. 6.15(b) a signal is provided when thyristors are shorted and arcing switch breaks the current. Figures 6.16(a),(b) show the logic states for the above case. Figure 6.16(a) shows the blanking pulse (Refer to b of Fig. 5.5) provided by a monostable. Figure 6.16(b) shows that the flip-flop remains

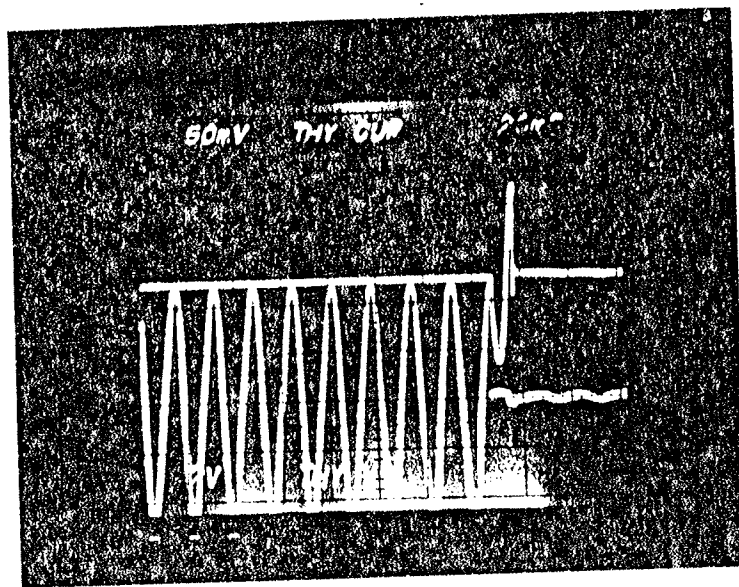


Fig. 6.10 a) Thyristor current and voltage at current making operation for 25 A

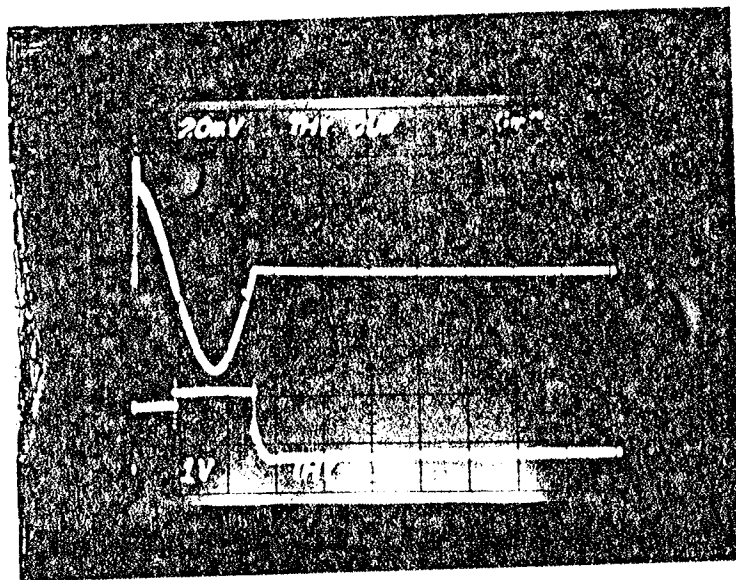


Fig. 6.10 b) Thyristor current and voltage at current breaking operation for 25 A

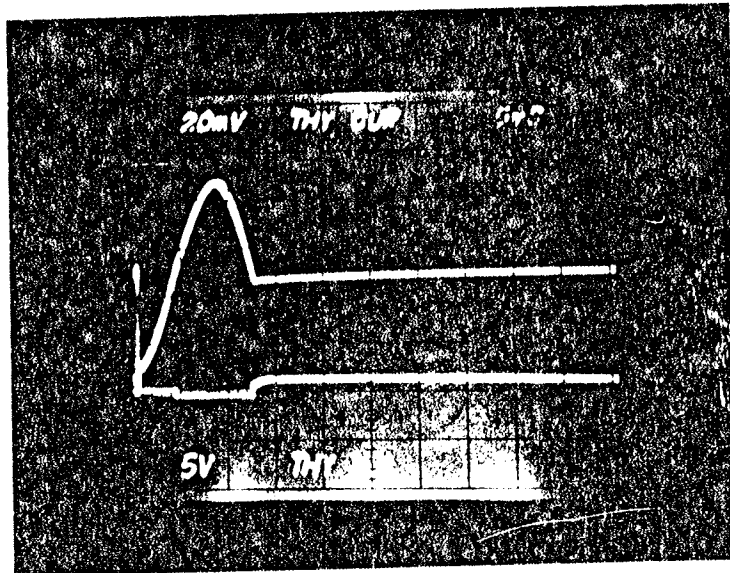


Fig. 6.11 a) Thyristor voltage and current at current breaking operation for 15 A

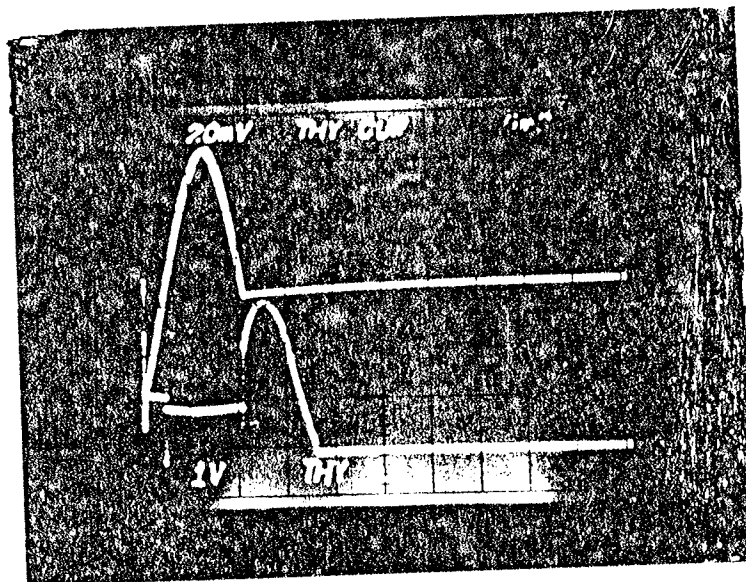


Fig. 6.11 b) Thyristor voltage and current at current breaking operation for 25 A

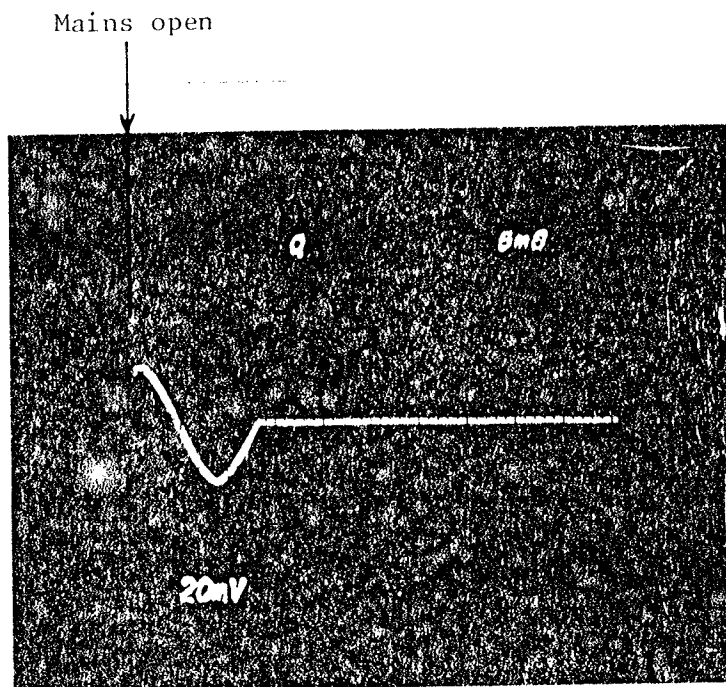


Fig. 6.12 a) Current through thyristors at
current break 170 A (20 mv/dv)

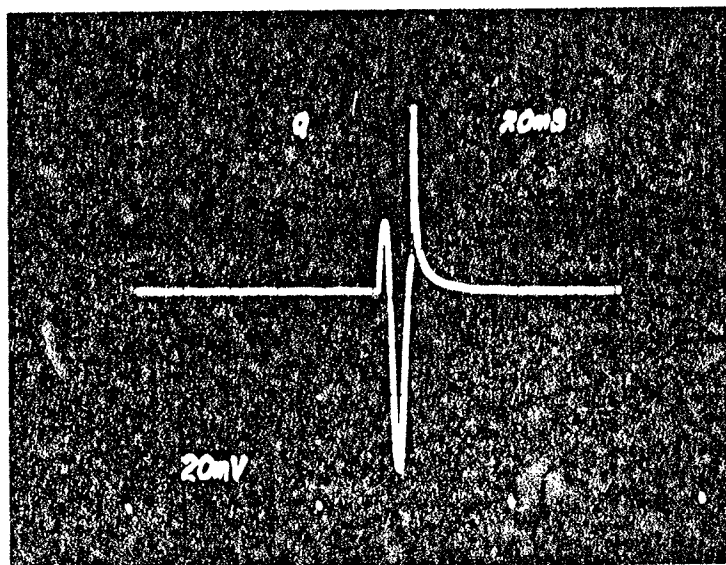


Fig. 6.13 a) Current through thyristors at current make at 50 A

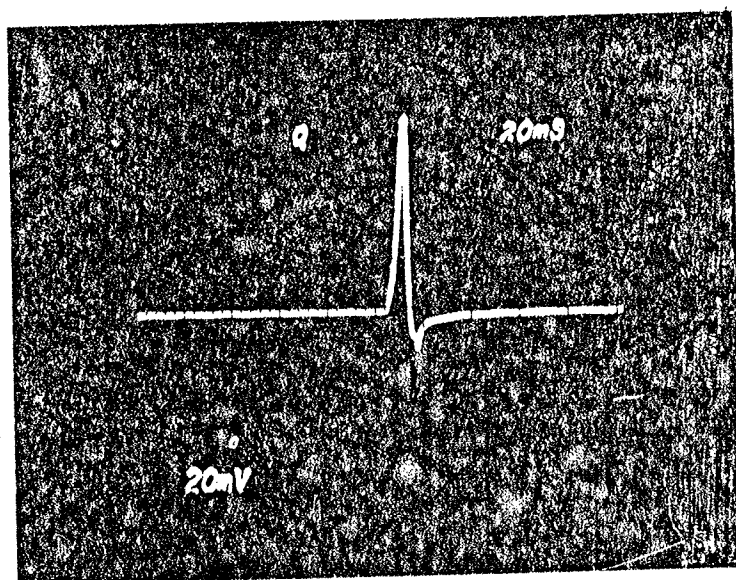


Fig. 6.13 b) Current through thyristors at current make at 170 A

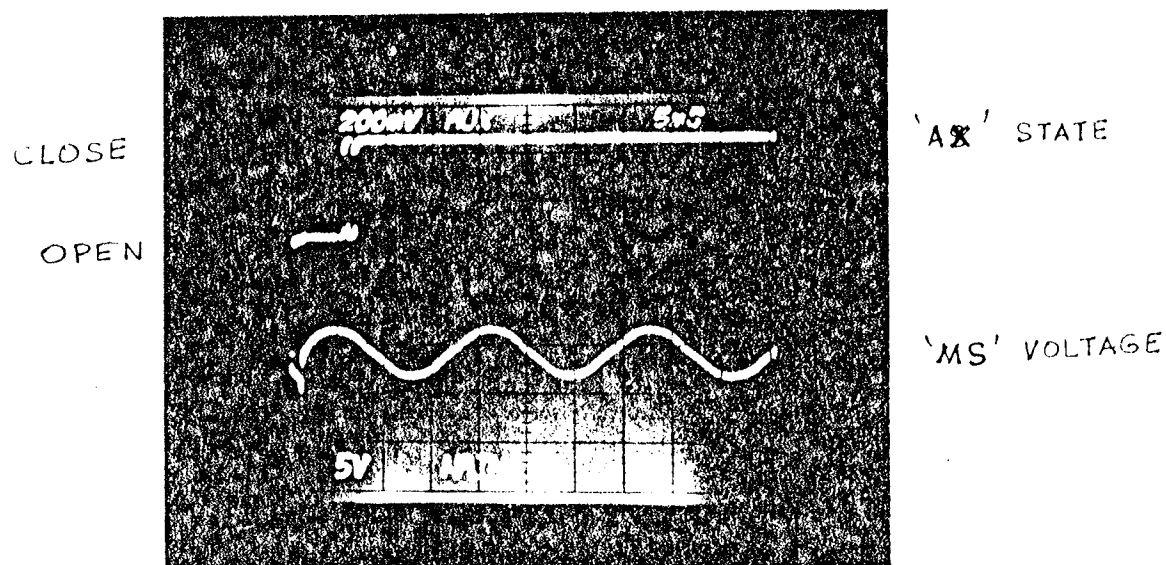


Fig. 6.14 a) Auxiliary position (AX) and mains voltage for open thyristor condition

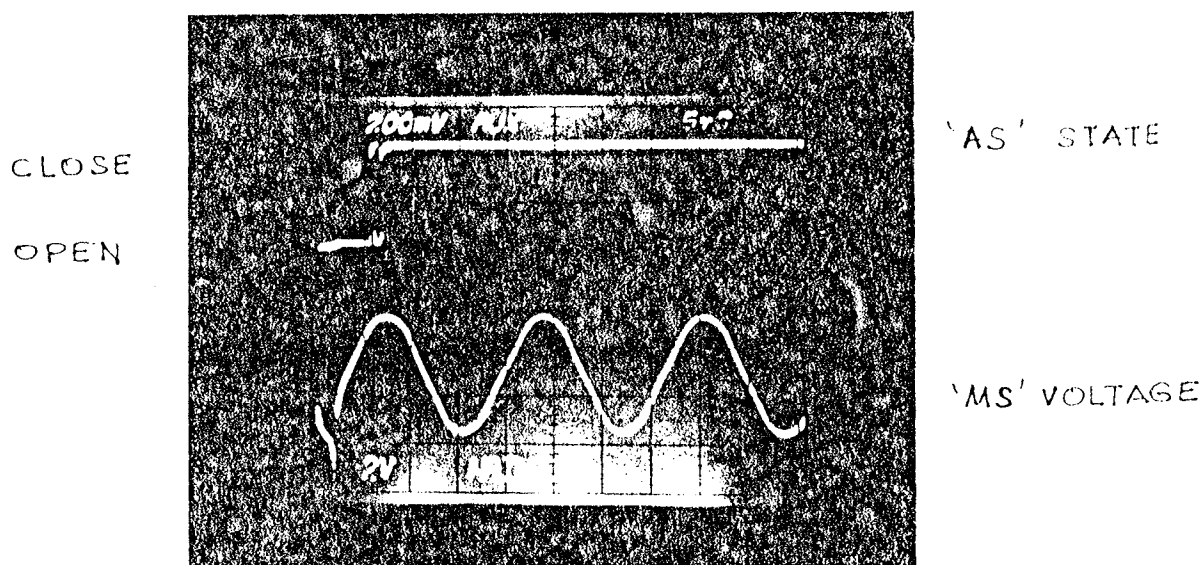


Fig. 6.14 b) Auxiliary position (AX) and mains voltage for open thyristor condition

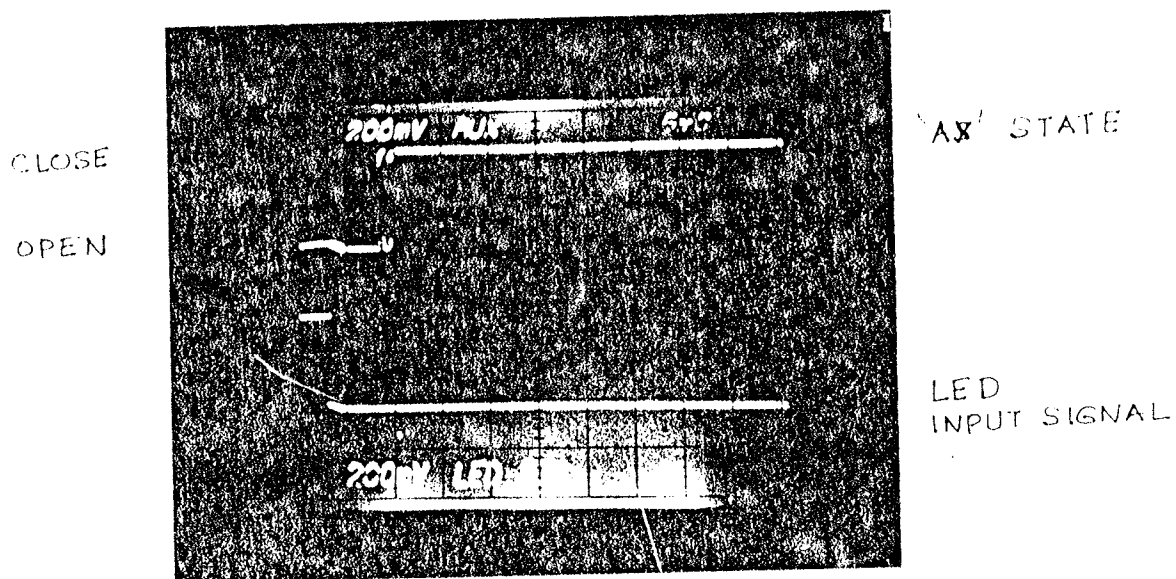


Fig. 6.15 a) Auxiliary position (AX) and signal input to SCR latched LED for thyristor open condition (Ref. b of Fig. 5.6)

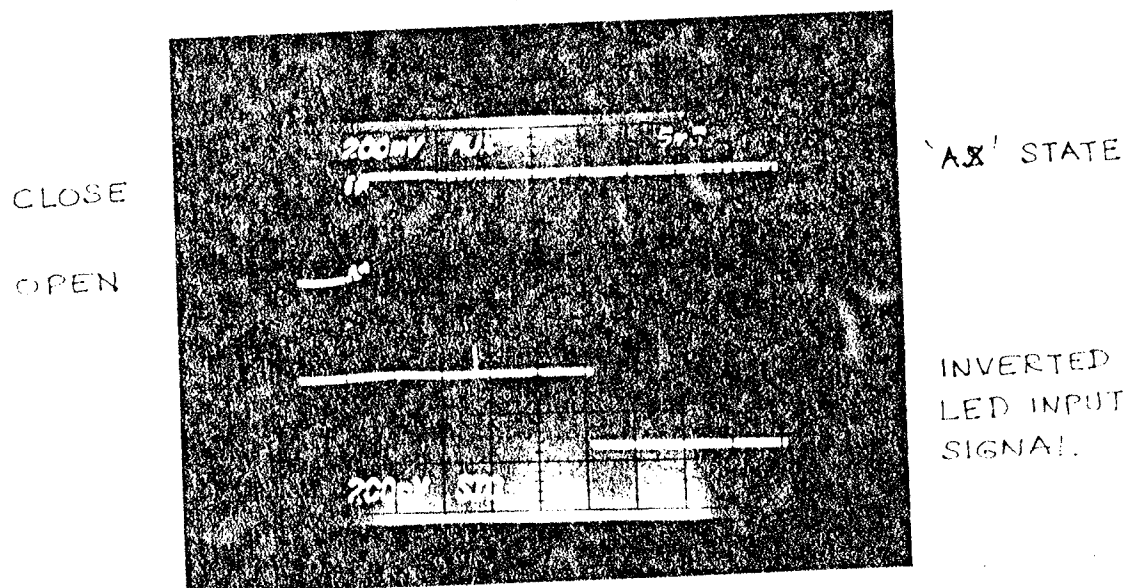


Fig. 6.15 b) Auxiliary position (AX) and inverted input to SCR latched LED for thyristor short condition (Ref. d, e of Fig. 5.5)

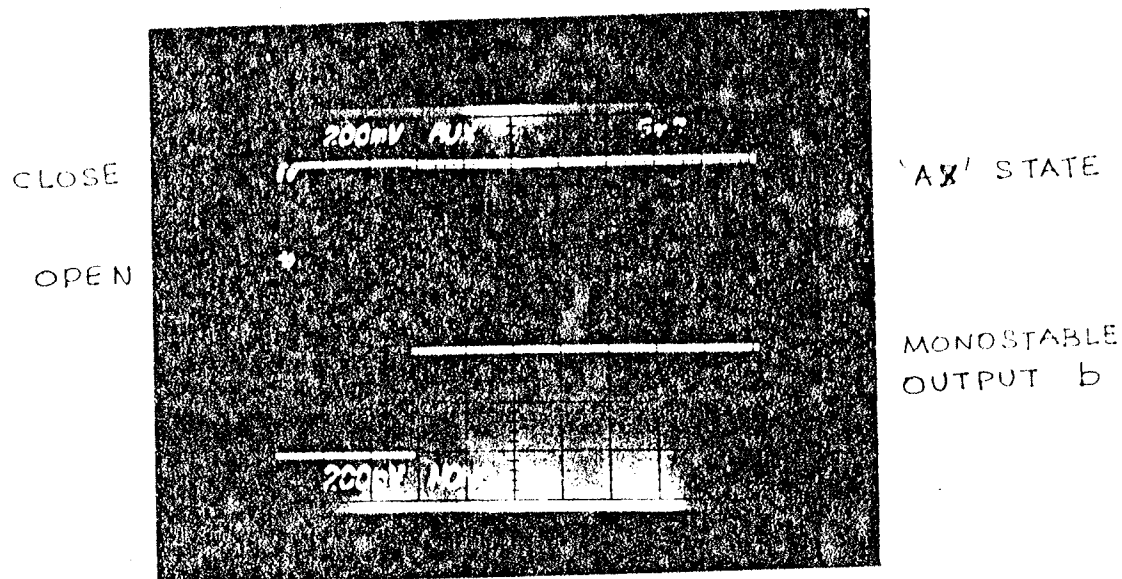


Fig. 6.16 a) Auxiliary position (AX) and monostable output (Ref. b of Fig. 5.5) for thyristor short condition

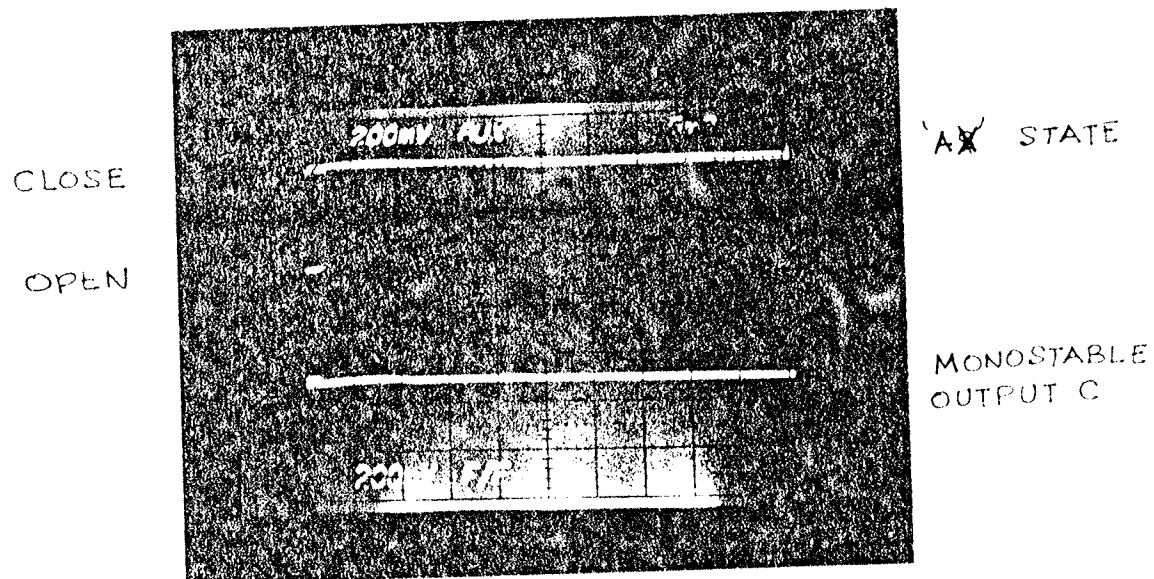


Fig. 6.16 b) Auxiliary position (AX) and flip flop output (c of Fig. 5.5) for thyristor short condition

set to logic high since the voltage does not appear across the thyristors to reset it.

Figures 6.17(a),(b) and 6.18(a),(b) show the logic states for normal tap changer. Figure 6.17(a) shows the voltage which appears across the thyristors at current zero. This voltage disappears when the arcing switch opens. Figure 6.17(b) shows the inverted signal a of Fig. 5.5, the auxiliary changeover sets the signal but thyristor voltage resets it but this happens during the blanking pulse by the monostable shown in Fig. 6.18(a). Therefore the flip-flop resets during this blanking pulse shown in Fig. 6.18(b) and provides no annunciation.

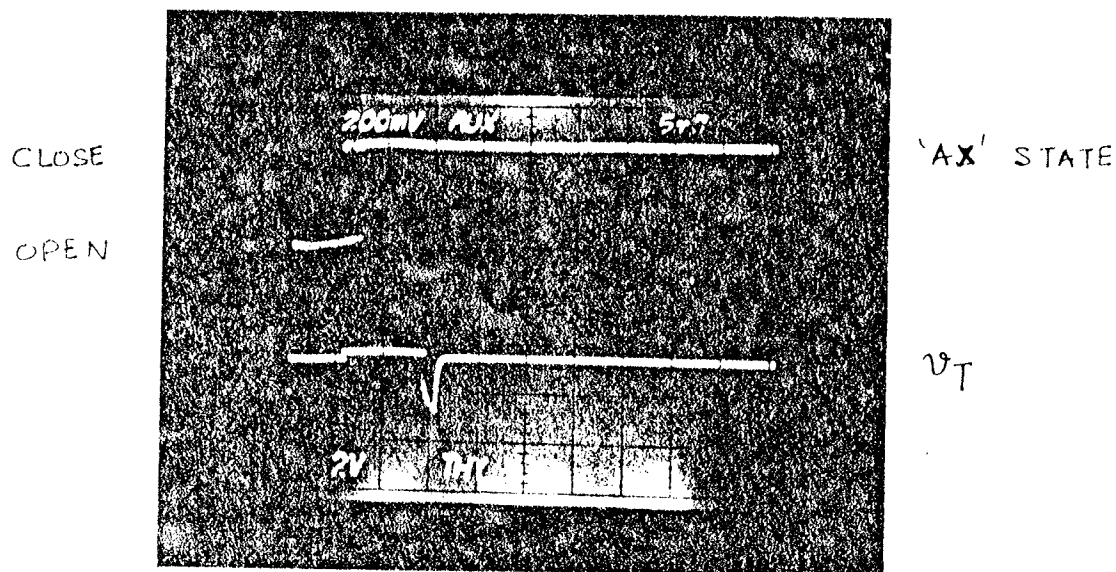


Fig. 6.17 a) Auxiliary position (AX) and thyristor voltage (Ref. 1 of Fig. 5.5) for normal tap changer

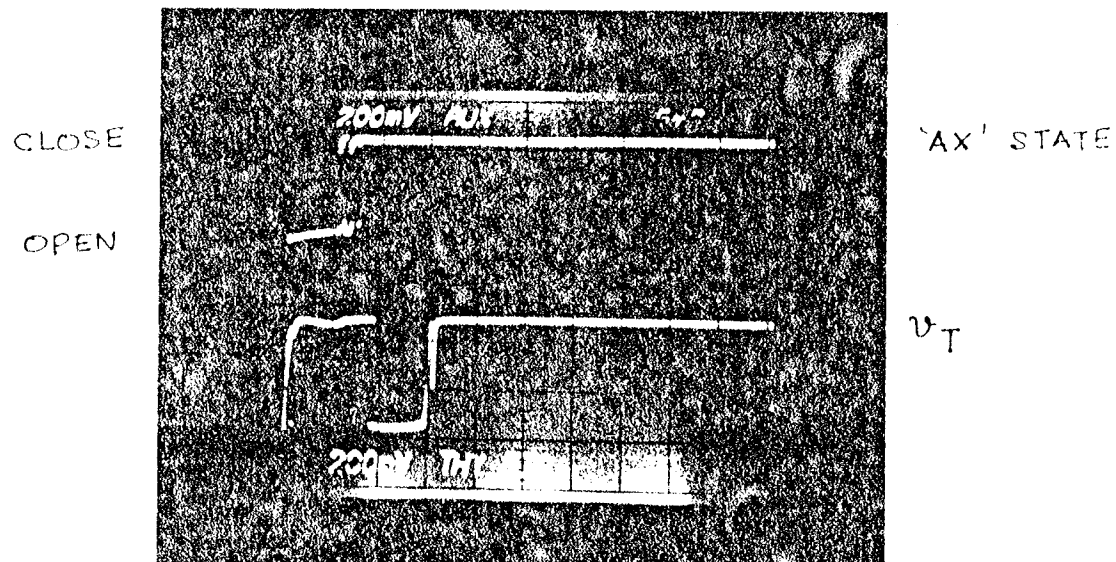


Fig. 6.17 b) Auxiliary position (AX) and opto coupler output (Inverted a of Fig. 5.5) for normal tap changer

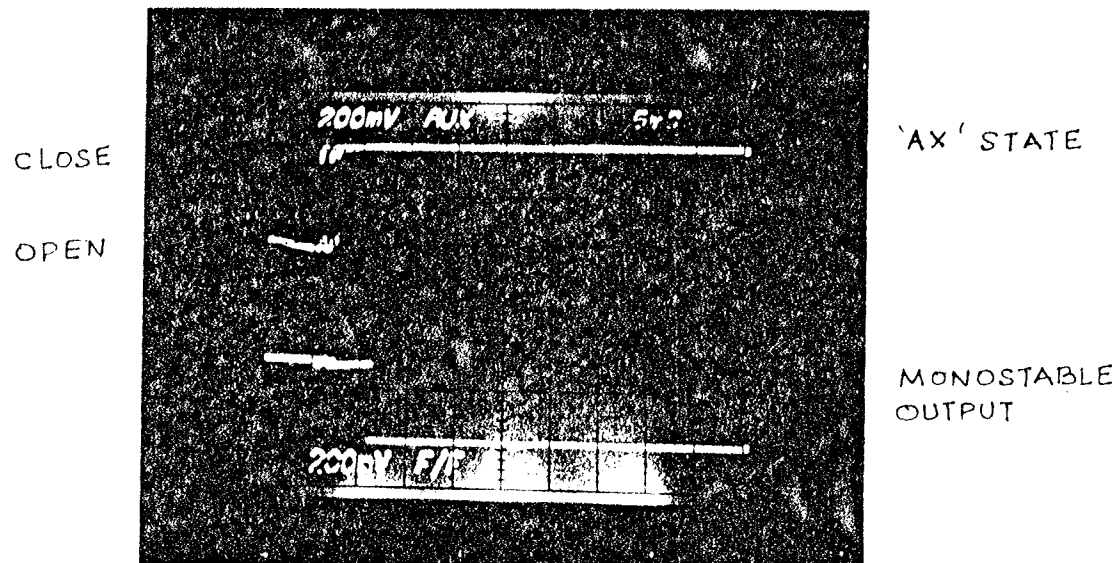


Fig. 6.18 a) Auxiliary position (AX) and monostable output (b of Fig. 5.5) for normal tap changer

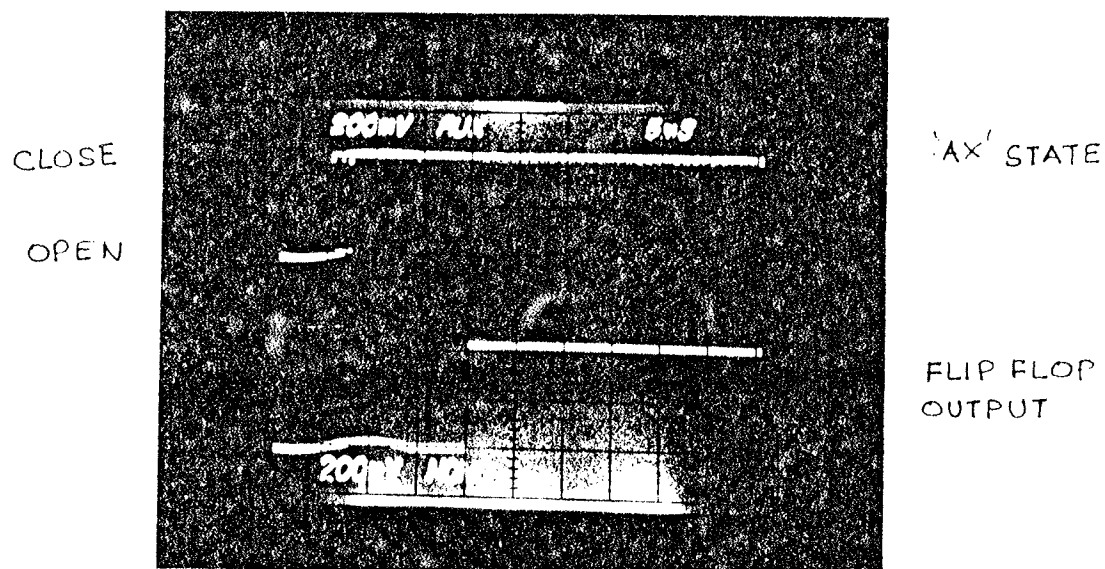


Fig. 6.18 b) Auxiliary position (AX) and flip flop output (c of Fig. 5.5) for normal tap changer

CHAPTER VII

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

The following conclusions are drawn on the basis of the theoretical and experimental results obtained in this thesis.

1. A new scheme is proposed to eliminate arcing in the existing reactor type on load tap changers of FPE. The proposed scheme can be retrofitted in the units in use to eliminate the maintenance of arcing contacts and the oil.
2. The proposed scheme adds a small additional cost which is likely offset by the maintenance free operation.
3. The proposed scheme is safe. It has a monitoring circuit to guard against possible failures in the thyristors. The tap changer reverts to the existing tap changer operation if the thyristors fail in short. If the thyristors fail in open further tap change is blocked and therefore no catastrophe takes place. Another circuit monitors the continuity of gate signals and in the event that the gate signals fail then the tap changer is also blocked from operation.
4. A proto-type for 40A and 170A was constructed on the actual system and tested satisfactory. The monitoring circuit was tested repeatedly by deliberately introducing short and open thyristor failures.

7.2 Alternate design

Figure 7.1 shows an alternate scheme to reduce the arcing in the arcing contacts of the diverter. A voltage triggered nonlinear resistance is introduced across each leg of the center tap reactor.

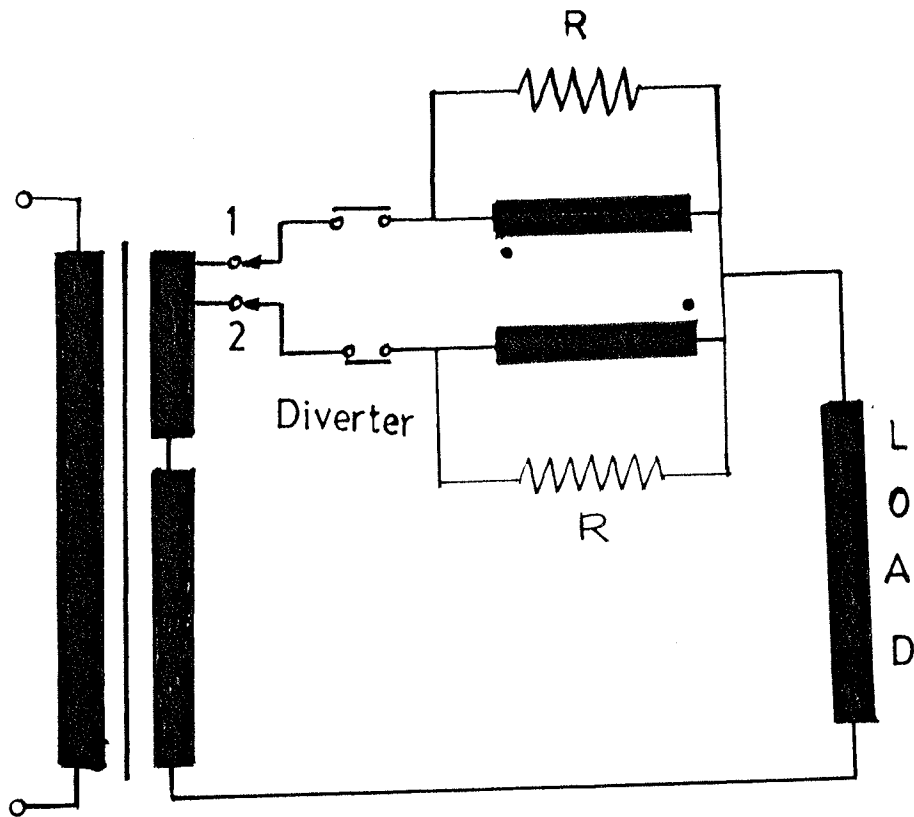


Fig. 7.1 Alternative tap changer with external resistor

When the diverter switch interrupts the current a large voltage is developed across the reactor discharging current through this resistance. Hence the arcing is reduced in the arcing switch.

7.3 Recommendations

A prototype for higher rating up to 1600A should be made and tested for reliability.

A temperature sensor which disables the tap changer if the temperature in the transformer goes beyond 80°C should be included in the circuit.

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30. "General Report of Study Committee No. 12", Electra (France), Dec. 1976.
31. "Loading Transformer by Temperature", Proc. 50th Annual Conf. of Electricity supply Engineers Assoc. of New South Wales, Aug. 1975.
32. "Transient Processes in the Synthetic Testing of Load Diverter Switches in On Load Transformer Tap Changers", Elin-z (Austria), 1975; 27 (1-2).
33. "Automatic Voltage Regulation of Transformers with Tap Changers", Osterr. Z. Elektwirtsche. (OZE) (Austria), Aug. 1969.
34. "The Scheme Securing Interaction of the Voltage Regulator with the Driving Mechanisms of the Tap Changers', Energetick (USSR), 1969.

35. Western Electric Co "Tap Changer for Electrical Inductive Apparatus", Patent by GB 2063572 a (810603) Appl. No. 79 7938379a.
36. "De-Energised Tap Changer for Transformers", Patent No. 96752 on May 6, 1975.
37. "Multi Tap Plug", Patent No. 774, 746 on Dec. 26, 1971.
38. "Multitap Device for Transformers", Patent No. 868045 on April 6, 1971.
39. "Electrical Inductive Apparatus Having Sheet and Strapwound Windings", Patent No. 1012218.
40. "Tap Changing Series-Multiple Transformer System", U.S.A. Patent No, 3, 818, 402 on June 18, 1974.
41. "Multiple Tap Device for Transformer", U.S.A. Patent No. 3, 497, 848 on Feb. 24, 1970.
42. E.W. Gutzwiller and T.P. Sylvan, "Power Semiconductor Rating Under Transient and Intermittent Loads", Proceedings of A.I.E.E., Jan. 1961, p. 699-705.

DATA SHEETS



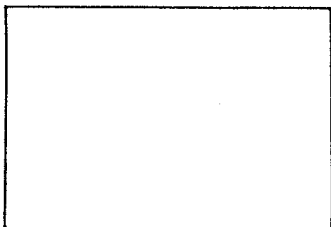
PHASE CONTROL SCR APPLICATION CHECKLIST

(Make copy for each use)

1. APPLICATION: _____

2. CIRCUIT:

Sketch circuit (showing all component values including inductances) or attach drawing



3. CIRCUIT VOLTAGE:

- Maximum peak forward and/or reverse voltage across SCR _____ V
- Maximum expected transient voltage _____ V
- Desired voltage safety factor _____
- Preferred SCR voltage rating _____ V
- Other _____

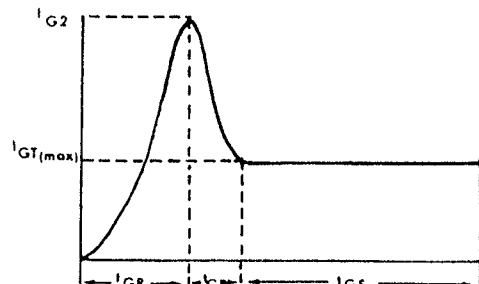
4. CIRCUIT CURRENT: (sketch waveform(s) on back of page)

- Maximum continuous SCR current* -
☐ DC, ☐ AVERAGE, or ☐ RMS _____ A
- Phase - ☐ 1 ϕ , ☐ 3 ϕ , ☐ 6 ϕ , or ☐ OTHER _____
- Conduction angle - ☐ Sine or ☐ Square, degrees _____
- Current waveform, frequency, and duty cycle _____
- Overload peak current (waveform) _____
 - Duty Cycle _____ %
 - Pulse Width _____
 - Resume Operation Following Overload ☐ YES ☐ NO
- Peak surge current (waveform) _____ A
 - Pulse Width _____
 - Number of Cycles _____
 - Assymetry (L/R ratio) _____
- Other _____

*If paralleling is required, state method of current sharing: _____

5. GATE DRIVE AVAILABLE:

- I_{G2} _____ A
- t_{GR} _____ μs
- $I_{GT(max)}$ 25°C _____ A
- t_{GP} _____ μs
- t_{GS} _____ ms
- Forward gate source voltage _____ V



6. THERMAL:

- Cooling Medium (check one) -
☐ AIR - ☐ Natural Convection, altitude _____ feet or
☐ Forced _____ LFM _____ CFM **
- ** Duct cross-sectional area _____
- Water - _____ GPM flow rate
- OIL (immersed) - Type _____ Manufacturer _____
- OTHER - _____
- Cooling medium maximum temperature, °C _____
- If heat sink is known, specify $R_{\theta SA}$ _____ °C/W.
- Other thermal considerations _____

7. MECHANICAL:

- Desired package type (check one) -
☐ STUD MOUNT
☐ DISC MOUNT
☐ INTEGRAL HEAT SINK
☐ FLAT BASE
☐ OTHER _____
☐ NO PREFERENCE
- Special size, weight, or other restrictions _____

8. PROJECT REQUIREMENTS: Quotation Due Date _____

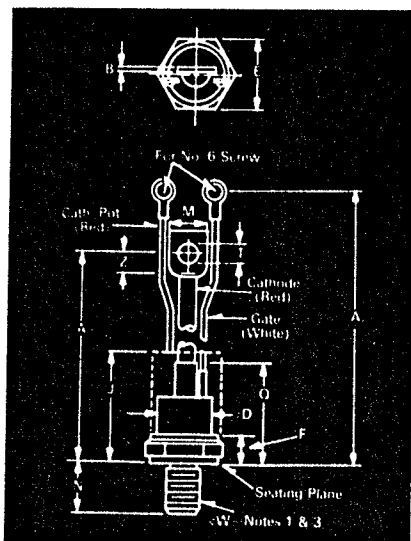
- Quantity Required _____ Person Requesting Information _____
- Timetable _____ Name _____
- Long-range Potential _____ Phone _____ X _____
- Other Remarks _____ Job Function _____
- _____ Company _____
- _____ Address _____
- _____ City _____ State _____
- _____ Bldg. _____ Zip _____
- ☐ Special screening and/or high reliability test requirements are attached.
- ☐ Also quote on this application using assemblies.

Please complete a copy of this form for each different application. Forward this form to Westinghouse Electric Corporation, Semiconductor Division, Attention: Sales Department, Youngwood, Pa. 15697 for complete quotation. If you need faster service, please call (412) 925-7272 for a quote.



Phase Control SCR 2N1909/2N1792 Series

70 A Avg.
Up to 600 Volts



Conforms to TO-94 Outline

Features:

- Center fired, di/namic gate
- All diffused design
- Low gate current
- Compression Bonded Encapsulation
- Low V_{TM}
- Lifetime Guarantee

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	5.775	6.265	146.69	159.13
A ₁	6.850	7.500	173.99	190.50
B	.055	.075	1.40	1.91
φD	.860	1.000	21.84	25.40
E	1.031	1.063	26.19	27.00
F	.255	.400	6.48	10.16
J	2.50		63.50	
M	.437	.650	11.10	16.51
N	.796	.827	20.24	21.01
Q		1.675		42.55
φT	.260	.291	6.60	7.39
Z	.250		6.35	

φW ½-20 UNF-2A

Creep & Strike Distance.

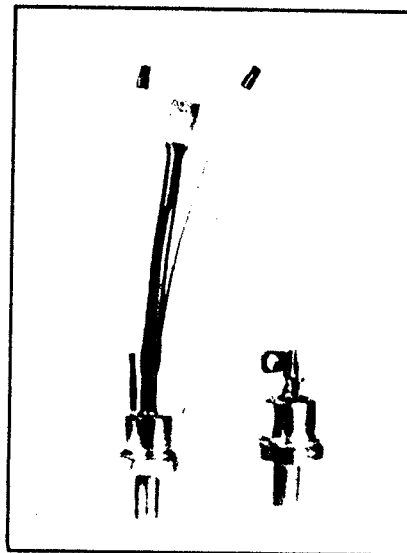
.10 in. min. (2.54 mm).

(In accordance with NEMA standards.)

Finish—Nickel Plate.

Approx. Weight—5 oz. (142 g).

1. Complete threads to extend to within 2½ threads of seating plane.
2. Angular orientation of terminals is undefined.
3. Pitch diameter of ½-20 UNF-2A (coated) threads (ASA B1.1-1960).
4. Dimension "J" denotes seated height with leads bent at right angles.



For TO-83 Outline, see page S23.

Applications:

- Phase control
- Power supplies
- Motor control
- Light dimmers

Voltage

Blocking State Maximums ($T_J = 125^\circ\text{C}$)

Symbol	2N1909	2N1910 2N1792	2N1911 2N1793	2N1912 2N1794	2N1913 2N1795	2N1914 2N1796	2N1915 2N1797	2N1916 2N1798	2N1805 2N1799	2N1806 2N1800
Repetitive peak forward blocking voltage, V	V_{DRM}	25	50	100	150	200	250	300	400	600
Repetitive peak reverse voltage, V	V_{RRM}	25	50	100	150	200	250	300	400	600
Non-repetitive transient peak reverse voltage, V	V_{RSM}	35	75	150	225	300	350	400	500	700
$t \leq 5.0$ msec, V	I_{DRM}	20	20	20	20	18	16	14	12	10
Forward leakage current, mA peak	I_{RRM}	20	20	20	20	18	16	14	12	10
Reverse leakage current, mA peak										

Note: For better ratings & higher voltages, see T500 series.

Current

Conducting State Maximums ($T_J = 125^\circ\text{C}$)

Symbol	Value
RMS forward current, A	$I_T(rms)$ 110
Ave. forward current, A	$I_T(av)$ 70
One-half cycle surge current ^① , A	I_{TSM} 1000
I^2t for fusing (for times ≥ 8.3 ms) A ² sec.	I^2t 4000
Forward voltage drop at $I_{TM}=500$ A and $T_J = 25^\circ\text{C}$, V	V_{TM} 2.3

Switching

Symbol	Value
Typical turn-off time, $t_T = 50$ A	
$T_J = 125^\circ\text{C}$, $di/dt = 5$ A/ μsec , reapplied $dv/dt = 20$ V/ μsec linear to $0.8 V_{DRM}$, μsec	t_q 100
Typ. turn-on time, $t_T = 100$ A	
$V_D = 100$ V ^② , μsec	t_{on} 4
Min. critical dv/dt , exponential to V_{DRM}	
$T_J = 125^\circ\text{C}$, V/ μsec ^{③④}	dv/dt 300
Min. di/dt ^① non-repetitive, JEDEC ₁	
A/ μsec	di/dt 800

Gate

Maximum Parameters

Symbol	Value
Gate current to trigger at $V_D = 12$ V, mA	I_{GT} 70
Gate voltage to trigger at $V_D = 12$ V, V	V_{GT} 3
Non-triggering gate voltage, $T_J = 125^\circ\text{C}$, and rated V_{DRM} , V	V_{GDM} 25
Peak forward gate current, A	I_{GTM} 4
Peak reverse gate voltage, V	V_{GRM} 5
Peak gate power, Watts	P_{GM} 16
Average gate power, Watts	$P_{G(av)}$ 3

Thermal and Mechanical

Symbol	Value
Min., Max. oper. junction temp., $^\circ\text{C}$	T_J -40 to +125
Min., Max. storage temp., $^\circ\text{C}$	T_{stg} -40 to +150
Max. mounting torque, in lb. ^①	130
Max. Thermal resistance ^②	
Junction to case, $^\circ\text{C}/\text{Watt}$	$R_{\theta JC}$.40
Case to sink, lubricated $^\circ\text{C}/\text{Watt}$	$R_{\theta CS}$.12

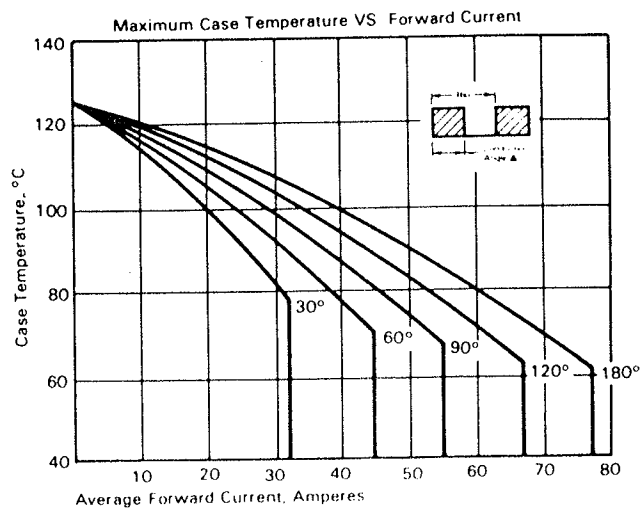
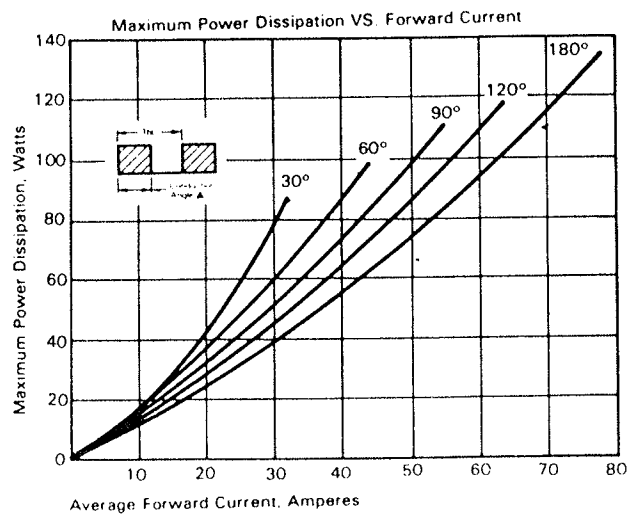
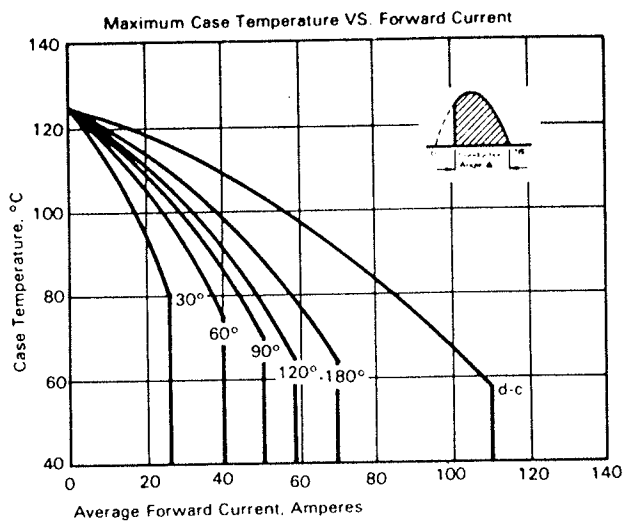
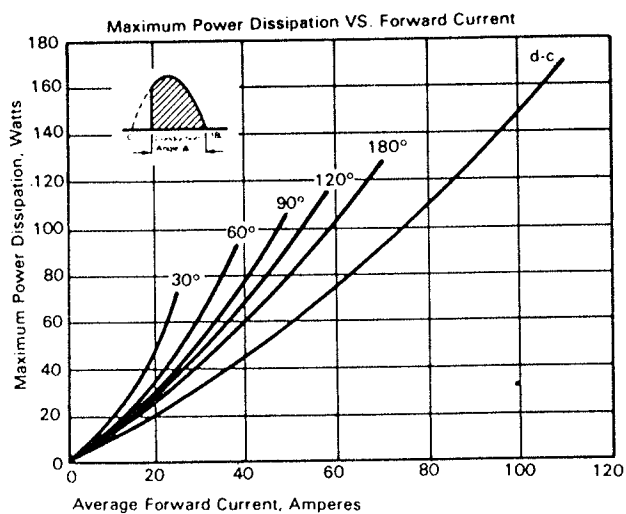
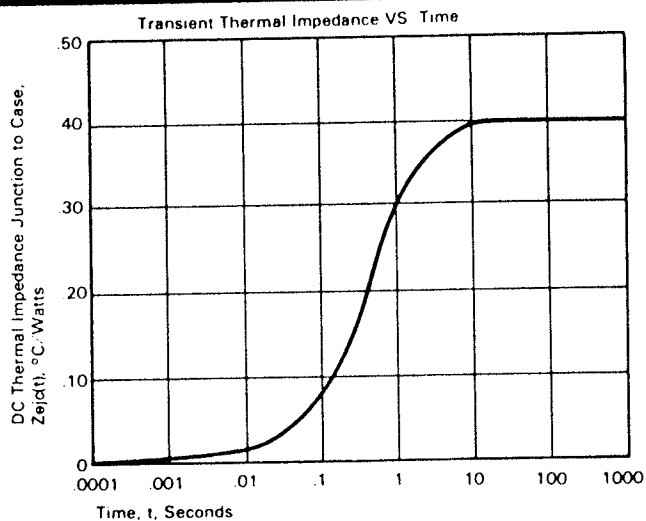
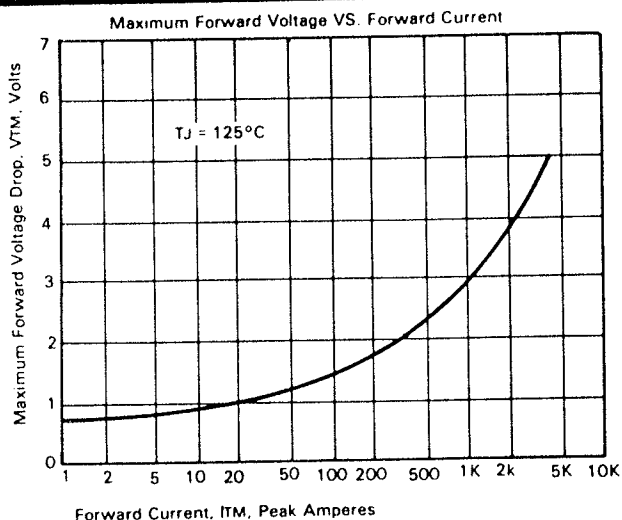
- ① Consult recommended mounting procedures.
- ② Applies for zero or negative gate bias.
- ③ Per JEDEC RS-397, 5.2.2.1.
- ④ With recommended gate drive.
- ⑤ Higher dv/dt ratings available, consult factory.
- ⑥ Per JEDEC standard RS-397, 5.2.2.6.

*2N1909 Series in TO-94 PKG
2N1792 Series in TO-83 PKG

THYRISTOR

**70 A Avg.
Up to 600 Volts**

Phase Control SCR 2N1909/2N1792 Series

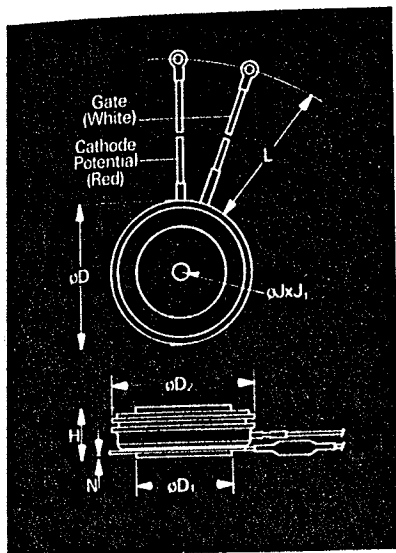


THYRISTOR



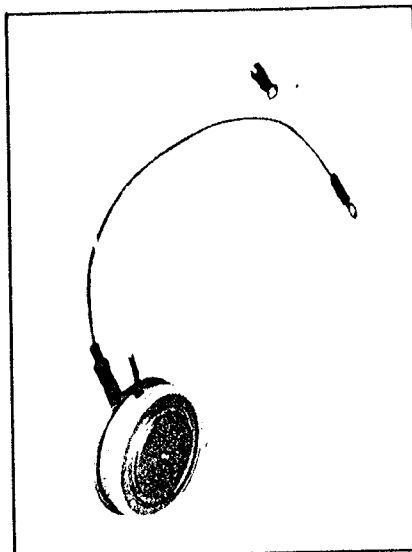
Phase Control SCR T7S0

550-750A / Avg
Up to 2200 Volts



Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
ϕD	1.850	1.900	45.72	48.26
ϕD_1	1.140	1.180	28.96	29.97
ϕD_2	1.760	1.850	44.70	46.99
H	.545	.605	13.84	15.37
ϕJ	.135	.145	3.43	3.68
J ₁	.072	.082	1.83	2.08
L	7.75	8.50	196.85	215.90
N	.025		.64	

Creep Distance—.408 in Min. (10.36mm)
Strike Distance—.203 in Min. (5.16mm)
Finish-Nickel Plate.
Approx. Weight—4 oz. (113 g.)
1. Dimension "H" is a clamped dimension.



Package I²t (case rupture)
rating: 30 x 10⁶ A² sec.

T7S Outline

Features:

- Center fired di/namic gate
- All diffused design
- Low gate current
- Low V_{TM}
- Low Thermal Impedance
- High surge current capability
- Low profile package
- Lifetime guarantee

Applications:

- Phase Control
- Motor Control
- Power Supplies
- Welding

Ordering Information

Type	Voltage		Current		Turn-off		Gate Current		Leads	
Code	V _{DRM} and V _{RRM} (V)	Code	I _{T(av)} (A)	Code	t _q (μsec)	Code	I _{GT} (ma)	Code	Case	Code
T7S0	100	01	550	55	150 (typical)	0	150	4	T7S	DN
	200	02								
	400	04	650	65						
	600	06								
	800	08	750	75						
	1000	10								
	1200	12								
	1300	13								
	1400	14								
	1500	15								
	1600	16								
	1700	17								
	1800	18								
	2000	20								
	2200	22								

Example

Obtain optimum device performance for your application by selecting proper order code.

Type T7S0 rated at 750A average with V_{DRM} = 1000V,
I_{GT} = 150ma, and standard flexible lead—order as:

Type	Voltage	Current	Turn Off	Gate Current	Leads
T 7 S 0	1 0	7 5	0	4	D N

THYRISTOR

**550-750A / Avg
Up to 2200 Volts**

Phase Control SCR T7S0



Voltage

Blocking State Maximums² (T_J = 125°C)

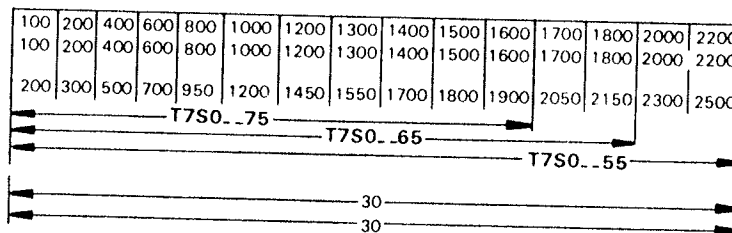
Repetitive peak forward blocking voltage, V_{DRM}
Repetitive peak reverse voltage, V_{VRRM}
Non-repetitive transient peak reverse voltage,
t ≤ 50 msec, V_{VRRM}

Symbol

V_{DRM}

V_{VRRM}

V_{VRRM}



Forward leakage current, mA peak
Reverse leakage current, mA peak

I_{DRM}

I_{VRRM}

Current

Conducting State Maximums
(T_J = 125°C)

RMS forward current, A
Ave. forward current, A
One-half cycle surge current¹, A
3 cycle surge current¹, A
10 cycle surge current¹, A
I_{PT} for fusing (for times ≥ 8.3 ms)
A²sec
Forward voltage drop at I_{FM} = 3000 A
and T_J = 25°C, V

Symbol

I_{TRMS}

I_{TA}

I_{TSM}

I_{TSM}

I_{TSM}

I_{PT}

I_{PT}

V_{FM}

T7S0-.55

T7S0-.65

T7S0-.75

860

1020

1180

550

650

750

7500

9000

10500

5400

6490

7570

4670

5600

6530

234,000

338,000

460,000

3.30

2.55

2.15

Switching

(T_J = 25°C)

Typical turn-off time, I_T = 250 A,
T_J = 125°C, di/dt = 25
A/μsec, reappplied dv/dt =
20V/μsec linear to 0.8 V_{DRM}, μsec
Typ. turn-on time, I_T = 100 A
V_D = 100 V, μsec
Min. critical dv/dt, exponential to V_{DRM}
T_J = 125°C, V/μsec
Min. di/dt non-repetitive,
A/μsec

Symbol

t_q

t_{on}

dv/dt

di/dt

150

7

300

600

Gate

Maximum Parameters
(T_J = 25°C)

Gate current to trigger at V_D = 12V, mA
Gate voltage to trigger at V_D = 12V, V
Non-triggering gate voltage, T_J = 125°C,
and rated V_{DRM}, V
Peak forward gate current, A
Peak reverse gate voltage, V
Peak gate power, Watts
Average gate power, Watts

Symbol

I_{GT}

V_{GT}

V_{GDM}

I_{GTM}

V_{GRM}

P_{GM}

P_{GAV}

150

3

0.15

4

5

16

3

Thermal and Mechanical

Min., Max. oper. junction temp., °C
Min., Max. storage temp., °C
Min., Max. mounting force, lb.
Max. Thermal resistance
With double sided cooling
Junction to case, °C/Watt
Case to sink, lubricated, °C/Watt

Symbol

T_J

T_{stg}

F_{max}

R_{θJC}

R_{θCS}

-40 to +125

-40 to +150

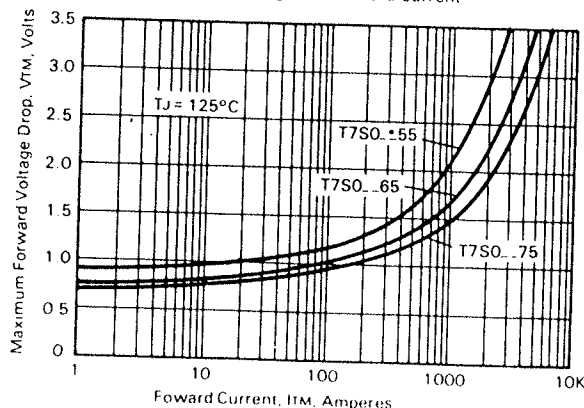
2000 to 2400

.035

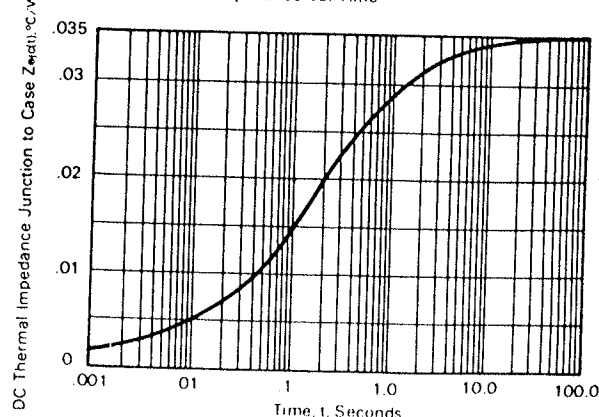
.02

- ① Consult recommended mounting procedures
- ② Applies for zero or negative gate bias.
- ③ Per JEDEC RS-397, 5.2.2.1.
- ④ With recommended gate drive.
- ⑤ Higher dv/dt ratings available, consult factory.
- ⑥ Per JEDEC standard RS-397, 5.2.2.6.

Maximum Forward Voltage VS. Forward Current



Transient Thermal Impedance Vs. Time

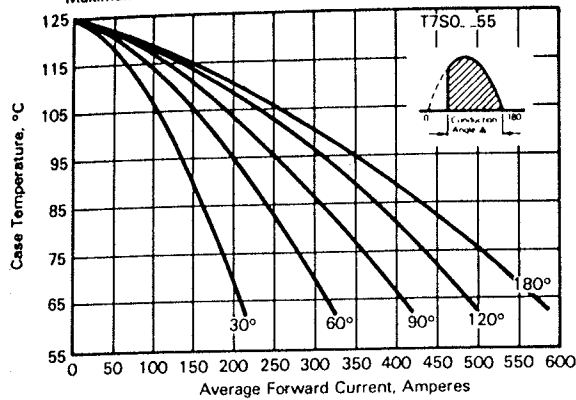




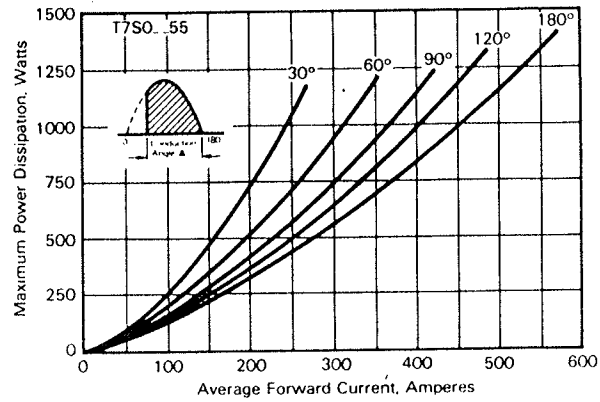
Phase Control SCR T7S0

550-750A Avg.
Up to 2200 Volts

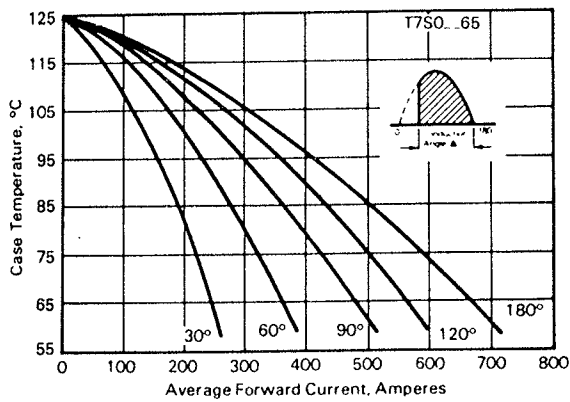
Maximum Case Temperature Vs. Forward Current



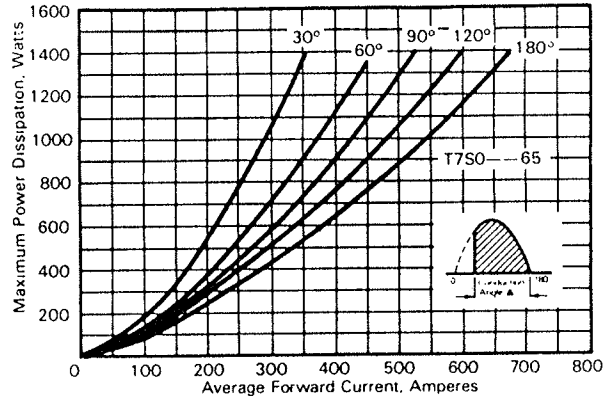
Maximum Power Dissipation Vs. Forward Current



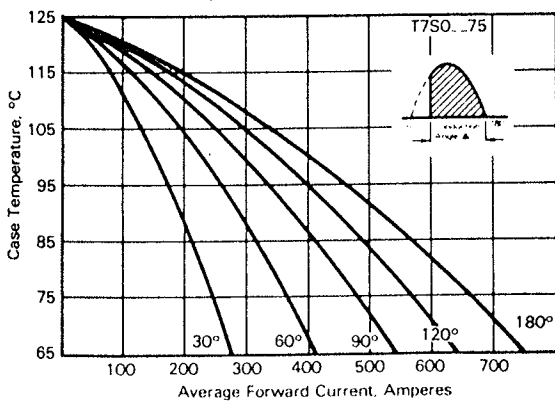
Maximum Case Temperature Vs. Forward Current



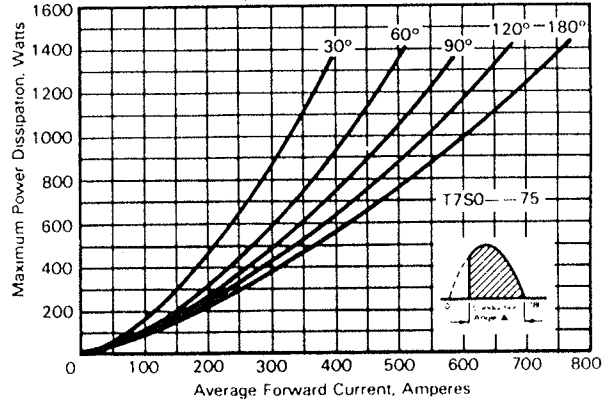
Maximum Power Dissipation Vs. Forward Current



Maximum Case Temperature Vs. Forward Current



Maximum Power Dissipation Vs. Forward Current



THYRISTOR

550-750A Avg.
Up to 2200 Volts

Phase Control SCR T7S0

