Investigation of a Cascade Multi-Level Inverter as an Advanced Static Compensator

by

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A Thesis

submitted to the Faculty of Graduate Studies

in partial fulfillment of the requirements for the Degree of

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Department of Electrical and Computer Engineering

University of Manitoba

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INVESTIGATION OF A CASCADE MULTI-LEVEL INVERTER AS AN ADVANCED STATIC COMPENSATOR

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HUSAM K. AL-HADIDI

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree of

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Finally, I express my deep appreciation to my beloved wife, Mona, for her continuous support, understanding and encouragement in all ways.

Abstract

An advanced static var compensator or STATCOM is a reactive power source applied for the dynamic compensation in power systems to provide voltage support, increase transient stability margin and improve damping of power systems. The thesis investigates the possibility of using a cascade M-level inverter consists of (M-1)/2 H-bridges in which each bridge has its own separate dc source as an advanced static compensation or STATCOM, in which the design of the seven level inverters as well as corresponding switching methods, harmonic spectrum and control strategies are carefully developed. The basic operation features of a STATCOM is simulated in a simple ac system.

The merit of the cascade converter configuration over the other two multilevel converter configurations, diode-clamped converter configuration, and flying-capacitor converter configuration, is that the cascading configuration uses a small number of diode and capacitors. Moreover, packaging and physical layout is very easy due to its modular structure. An efficient control strategy based on the control of the phase angle of switching pattern is developed in this thesis. A switching scheme of rotated fundamental pattern is applied to control the dc voltage balancing. The simulation results indicate that the proposed design of the cascade M-STATCOM and corresponding control strategies are successful, cost efficient and easy to implement, which make it emerge as an practical alternative approach.

Contents

List of Figures

List of Tables

List of Symbols

Some of the most frequently occurring abbreviation and symbols used in the Thesis are tabulated below. Others are explained where they are used.

Table A.2

Ac	Peak-to-peak amplitude of the carriers
ac	Alternating current
A_m	Amplitude of the modulating signal
A_c	Amplitude of the carrier wave
dc	Direct current
EMTDC	Electromagnetic Transient Program for dc system
FC	Fixed capacitor
f_c	Frequency of the carriers
FFS	Fundamental frequency switching
f_m	Frequency of the modulating signal
GTO	Gate Turn Off thyristor
HVDC	High Voltage Direct Current
k	Frequency ratio
kA	Kiloampere
kV	Kilovolt
MI	Modulation index
M-STATCOM	Multilevel GTO thyristor inverter type of STATCOM
Mvar	Mega-var
PI	Proportional integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation

Table A.2(continued)

SC	Synchronous condenser
SFO-PWM	Switching frequency optimal PWM
SH-PWM	Sub harmonic PWM
STATCOM	Voltage source inverter type of the var compensator
SVC	Static var compensator
TCR	Thyristor controlled reactor
THD	Total Harmonic Distortion
TSC	Thyristor switched capacitor
var	Volt-ampere reactive
VSI	Voltage Source Inverter
ω	System frequency

CHAPTER 1

CHAPTER 1 Introduction

1.1 BACKGROUND

In an ac power system the transmittable electric power is related to the transmission line voltage profile under steady state and dynamic conditions over a wide range of network contingencies. It is known that the voltage profile along the transmission line can be controlled in a more effective way by controlling the reactive power flow in the line.

The application of the reactive power conditioner is a well established practice and it is termed as 'reactive power compensation'. The methods that have long been employed to increase the steady state power of the line are fixed or mechanically switched capacitors and reactors. The reactors are installed in shunt at intervals along the line and large capacitors are connected in series or in parallel. With the development of high power solid state devices such as the thyristor along with electronic controls, new devices have emerged which offer smooth continuous control of reactive power. Thyristor controlled series compensators (TCSC) can control the amount of series compensation of the transmission line and static var compensators (SVC) can control the amount of the reactive power injected into or absorbed from the transmission system. During the last decade it has been convincingly demonstrated that both the transient and dynamic stability of the power system can be improved, and voltage collapse can be prevented [1] with rapid continuously variable control accomplished by such solid state technology. A few years ago the integrated gate commutated thyristor (IGCT) was developed which has power ratings comparable to that of the conventional thyristor. This has led to the development of self commutated converters for reactive power sources. This new technology has resulted in equipment that is fundamentally different from the conventional thyristor-controlled static var compensator (SVC). The new equipment is called the Advanced Static Var Compensator or STATCOM. It has many technical advantages over the conventional SVC.

1.2 CONVENTIONAL STATIC VAR COMPENSATOR (SVC)

The traditional static var compensators use either banks of shunt connected capacitors or thyristor-switched capacitors with thyristor controlled reactors to provide the needed

controlled shunt reactive power compensation. A simplified diagram of a fixed capacitor / thyristor control reactor (FC/TCR) type of compensator is shown in Figure 1.1 and its elements are:

I) The fixed capacitor (FC), provides a permanently connected generation of reactive power, designed also to act as suitable harmonic filter.

II) The thyristor controlled reactor (TCR) consisting of anti-parallel thyristors connected in series with shunt reactors usually in a delta configuration. These controlled reactors are used to absorb reactive power. The thyristor may be switched at any point over the half wave (90 to 180 electrical degrees behind the voltage sine wave) to provide a fully adjustable control from 100 percent to zero of rated reactive power absorption.

III) Power transformer to connect to the high voltage busbar.

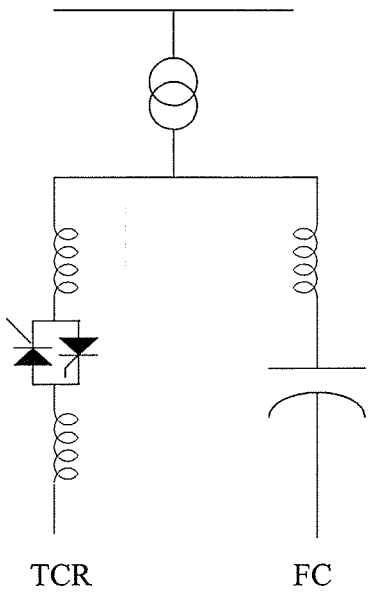


Figure 1.1 A Simplified Diagram of FC/TCR SVC

The disadvantages of the SVC here are [2]:

a) The ac capacitor banks consist of capacitor units in parallel. Therefore, particular care must be exercised to ensure proper separation between capacitor groups in the event of an external flashover.

b) Due to their physical size and other considerations, the reactor and the capacitor banks are mounted outdoors, in the switchyard. Their insulation system must withstand harsh environmental conditions.

c) The FC tends to lower system resonant frequency.

For these reasons, the traditional static var compensators form quite a large system, requiring considerable equipment at significant cost. This may limit their application in densely populated areas where severe environmental and space restrictions are imposed.

1.3 Principles of the STATCOM

The shunt static compensator or STATCOM (for Static Compensator) is an electronic equivalent of the synchronous condenser, synchronous machine not driven by a prime mover connected to the power system. The equivalent circuit and Phasor diagram of the synchronous condenser are shown in Figure 1.2. By varying the magnitude of the excitation, or field current, both the amount and the direction of the reactive power produced by

the synchronous condenser can be changed. That is, if the excitation current is increased up to such level that the amplitude of the internal voltage of the synchronous condenser is higher than the voltage of the equivalent ac system ($E > U$), then the current flows through the synchronous reactance and winding resistance from the synchronous condenser to the ac system, and the synchronous condenser generates reactive power for the ac system (capacitive). If

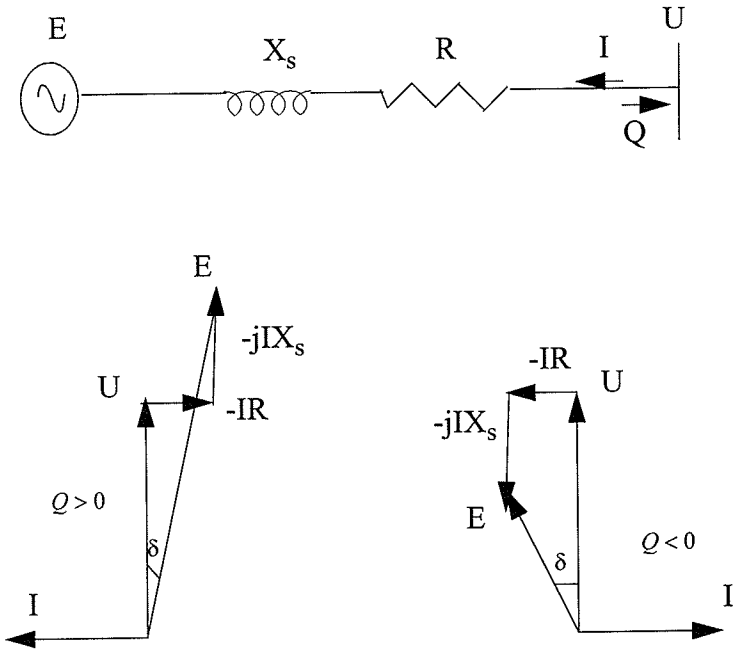


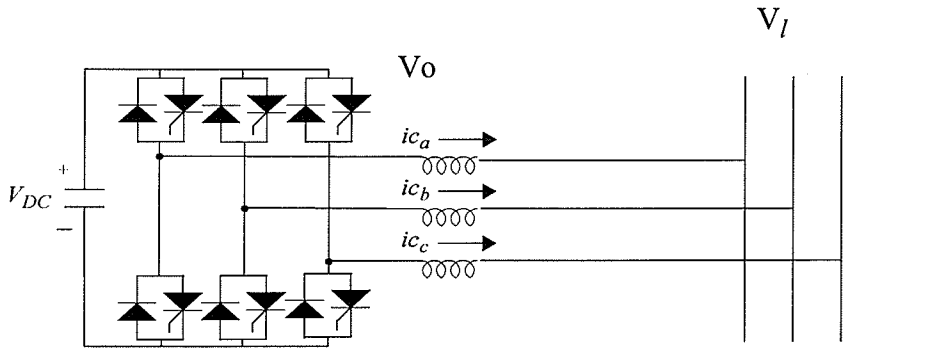
Figure 1. 2 A Equivalent Circuit and Phasor Diagram of the Synchronous condenser

the excitation current is decreased to a level such that the internal voltage is less than the voltage of the equivalent ac system ($E < U$), then the current flows through the reactance and resistance from the ac system to the synchronous condenser, and the synchronous condenser absorbs reactive power from the ac system (inductive). If the amplitude of the

internal voltage of the synchronous condenser is equal to the voltage of the equivalent ac system ($E = U$), the reactive power exchange is zero. As the stator resistance, R, is much less than the synchronous reactance, X_S, the angle δ is very small and E and U are essentially in phase. The only power flow into the synchronous machine is to overcome the losses of the machine.

1.4 The Basic STATCOM.

The STATCOM is based on a simple concept. A GTO based power converter is used to produce an alternating voltage source in phase with the transmission line voltage, and is connected to the line through a series inductance (usually the transformer leakage). When the voltage source is greater than the line voltage, leading reactive current is drawn from the line and the equipment acts as a capacitor. When the voltage source is smaller than the line voltage, lagging reactive current is drawn from the line and the equipment acts as inductor. In practice a small amount of real power is also drawn from the line to supply the losses of the converter. The basic electronic building block for a STATCOM is a voltage-sourced inverter that converts the dc voltage at its input terminals into a three-phase set of output voltages. A six-pulse inverter, the simplest implementation of such an inverter, is illustrated in Figure 1.3, together with a typical line-to-line output voltage waveform. In practice, a quasi-square waveform such as this would produce unacceptable current harmonics when connected to a line. Consequently a practical STATCOM must use some technique to control the harmonics. The approaches have been to use many such inverters, appropriately phase shifted, with their outputs combined magnetically to produce a nearly sinusoidal resultant waveform [3], to use some kind of PWM switching technique, and/or to use the multilevel inverter to improve the harmonics.

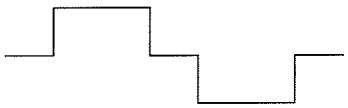


GTO Voltage Source Inverter Transmission Line

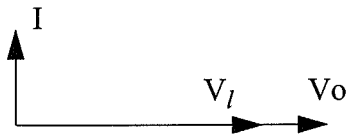
If V_l = Vo, I = 0

If $V_l < Vo$, I is capacitive

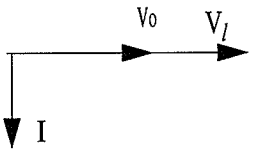
If $V_l > Vo$, I is inductive



Inverter output line-to-line voltage



Capacitive current



Inductive current

Phasor Diagram of the STATCOM

Figure 1. 3 Basic STATCOM with Elementary Six-pulse Inverter.

1.5 ADVANTAGES OF STATOM OVER SVC

The advantages of the STATCOM design over the traditional fixed capacitor/ thyristor controlled reactor (FC/TCR) or thyristor switched capacitor/thyristor controlled reactor (TSC/TCR) type design are:

a. The voltage source converter is more compact and requires only a small coupling reactance, usually the ac system transformer leakage and a single dc capacitor about one-eighth of the size of the capacitor in a SVC of the same rating [4]. This leads to a significant reduction in equipment size and installation cost.

b. The design offers a fast continuous variation of reactive output power from capacitive to inductive, and more effective reactive power generation during undervoltages. The improvement in var output of the STATCOM during under voltage conditions is illustrated in Figure 1.4.

c. Better control stability [5] which translates to superior performance during major transients and, ultimately, increased system transient stability and improved damping.

However, many design considerations lie in the path of the development of the STATCOM, such as system configuration, control of the switching losses and harmonic distortion, the balancing of the dc voltage of STATCOM and the system response to the step change of reactive power.

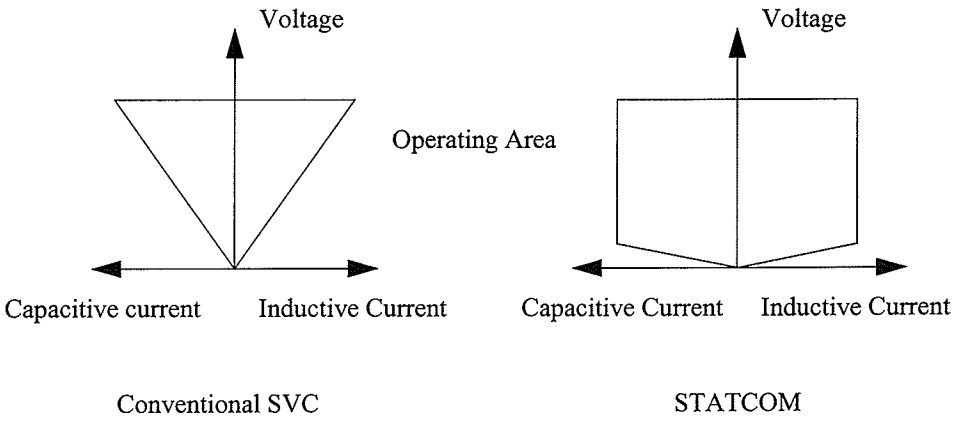


Figure 1. 4 Comparison of VAR output between Conventional SVC and STATCOM

For these reasons, the multilevel-STATCOM(M-STATCOM) using cascaded multilevel inverters is studied in this thesis, which will offer an interesting alternative to other circuit topologies being considered for the STATCOM.

1.6 The Scope Of The Thesis

1.6.1 Review of different topologies of multilevel inverters.

There are mainly three different system configurations of multilevel voltage source inverters suitable for STATCOM application. They are:

1- Diode-clamped converter configuration

2-Flying-capacitor converter configuration.

3- Cascade converter configuration.

The first and third configuration will be discussed in Chapter 2. A 7-level cascade GTO inverter was chosen as the candidate design of the M-STATCOM in Chapter 4.

1.6.2 Investigation of the switching methods

For a 7-level cascade inverter, both the fundamental frequency switching (FFS) and pulse width modulation (PWM) technique will be studied to determine which switching method is best.

1.6.3 Control Strategy Study

Development of suitable control strategies which will be aimed at:

1- Maintaining individual dc capacitor voltages at desired levels.

2- Realizing the reactive current output control.

3- Obtaining excellent dynamic performance with high control stability.

1.6.4 Digital Simulation

A 7 level cascade multilevel inverter based STATCOM will be simulated using the electromagnetic transient simulation program called PSCAD/EMTDC^{TM} which is the product of Manitoba HVDC Research Centre, Canada.

1.6.5 In Chapter 5, some of the results and conclusions from the above studies will be listed .

CHAPTER 2 Analysis of a Multilevel GTO Thyristor Inverter

2.1 Introduction

MULTILEVEL power conversion has been receiving increased attention in the past few years for high-power applications [6]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature [7]. These converters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. In this multilevel voltage source inverter (VSI) based on STATCOM category, there are mainly three different system configurations. They are 1) diode-clamped converter configuration [8], 2) cascade converter configuration [9] and 3) flying-capacitor converter configuration. In this chapter the first configuration will be analyzed in brief and focus will be given to the second configuration to develop STATCOM system in this thesis.

2.2 Diode-Clamped Multilevel Inverter

The diode-clamped multilevel inverter uses one dc bus subdivided into a number of voltage levels by a series string of capacitors [10]. A generalized structure of one phase of an 5-level GTO inverter is shown in Figure 2.1 where the level number $N = 5$. The dc capacitors are shared by the other phases, and possibly by the other bridges in higher pulse number designs. In a three-phase bridge configuration the number of level in the line-to-line voltage will be 2N+1. The advantages of such a structure is that the thyristor needs only block the voltage of its own level and not the full dc voltage. Furthermore, each GTO thyristor is well protected against overvoltage by the clamping action of the dc capacitors. The lower group of GTO thyristors requires the complementary gating pulses of the upper group of the same number. That is if $\mathbf{T_2}$ is on, then $\mathbf{T'_2}$ must be off. It should be mentioned that for each voltage step only one GTO thyristor must turn on and one GTO thyristor must turn off. For example, if $\mathbf{T_1}$ is off, then $\mathbf{T_2}$, $\mathbf{T_3}$,.....$\mathbf{T_{N-1}}$ and $\mathbf{T'_1}$ are on, and the terminal V1 is connected to the output terminal through $\mathbf{DP_1}$, $\mathbf{T_2}$, $\mathbf{T_3}$,....$\mathbf{T_{N-1}}$ for positive current, or through $\mathbf{T'_1}$ and $\mathbf{DN_1}$ for negative currents. As described above, taking one single phase into account, the five voltage levels could be achieved at the output terminal if the gate logic in Table 2.1 is followed, a stepped output voltage of the five level inverter shown in Figure 2.2, which is a simple sum of the two rectangular waveforms. It should be noted that the clamping diodes are required to block different voltages, e.g. $\mathbf{DP_1}$ must block the voltage of a single dc level, V, while $\mathbf{DP_{N-2}}$ must block (N-2)Vc, assuming that all the capacitor voltage are equal to Vc.

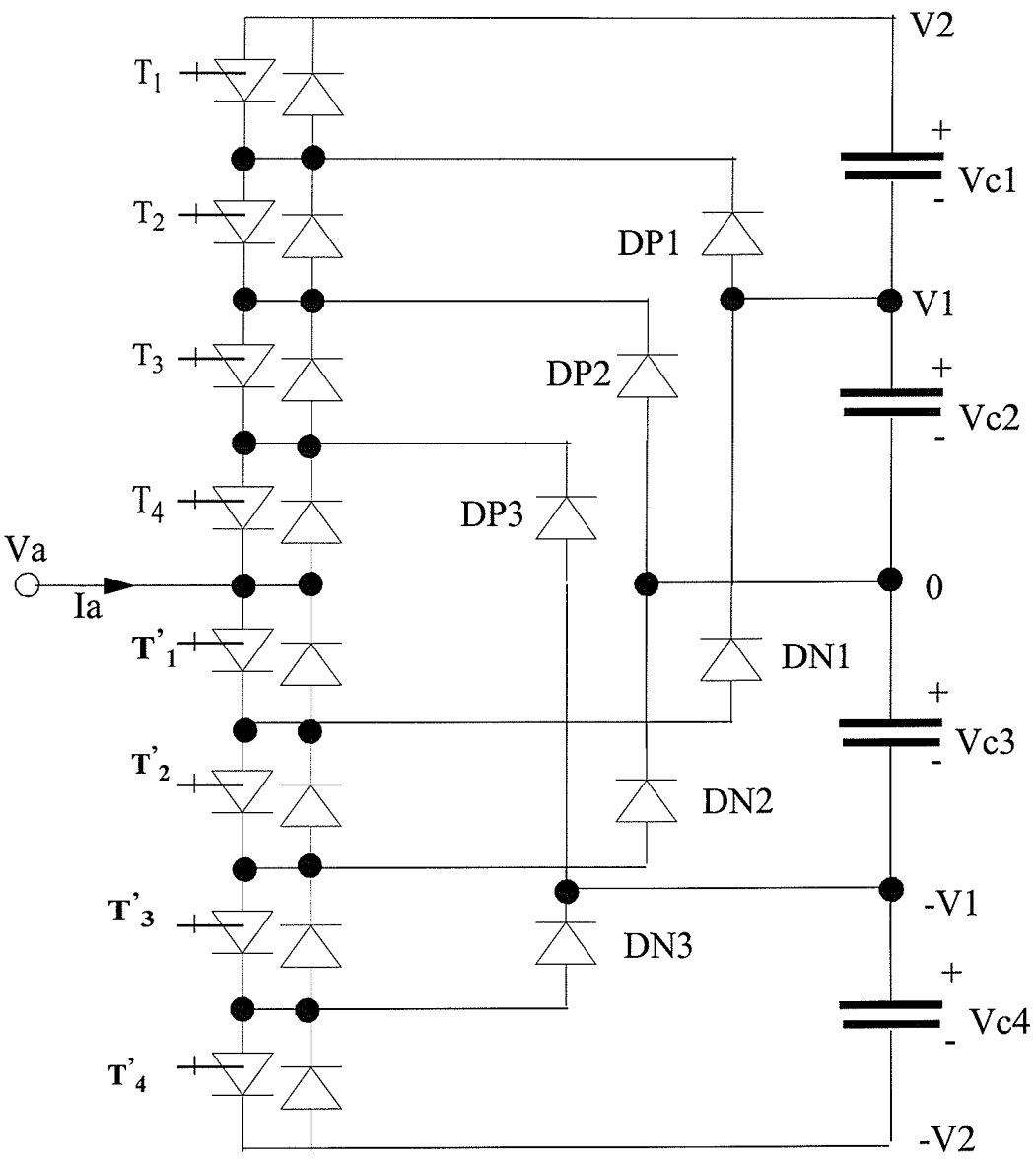


Figure 2.1: One Phase of Diode-clamped 5-level Inverter

Table 2.1 The Gate Logic for Five-level Diode-clamped Inverter

output	**The state of GTO thyristors**							
(E_a)	**T_1**	**T_2**	**T_3**	**T_4**	**T'_1**	**T'_2**	**T'_3**	**T'_4**
$+2V_c$	1	1	1	1	0	0	0	0
$+V_c$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_c$	0	0	0	1	1	1	1	0
$-2V_c$	0	0	0	0	1	1	1	1

In the above Table we asumed that $V_{c1} = V_{c2} = V_{c3} = V_{c4} = V_c$.

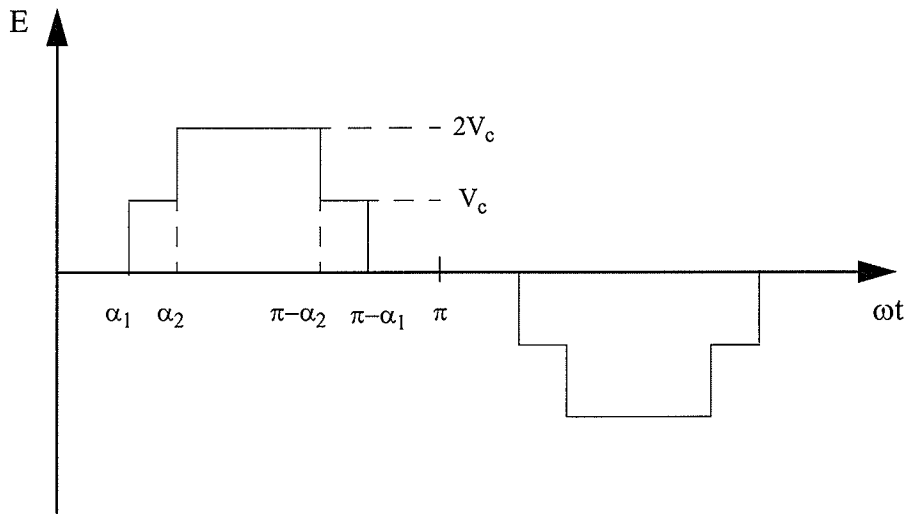


Figure 2.2: Five level Diode-clamped Inverter Waveform Voltage

2.3 Cascade Multilevel Inverters

2.3.1 Circuit and Working Principle

The cascade inverter is made up from series connected single phase full bridge inverters, each with their own isolated dc bus [11]. Figure 2.3 illustrates the connection di

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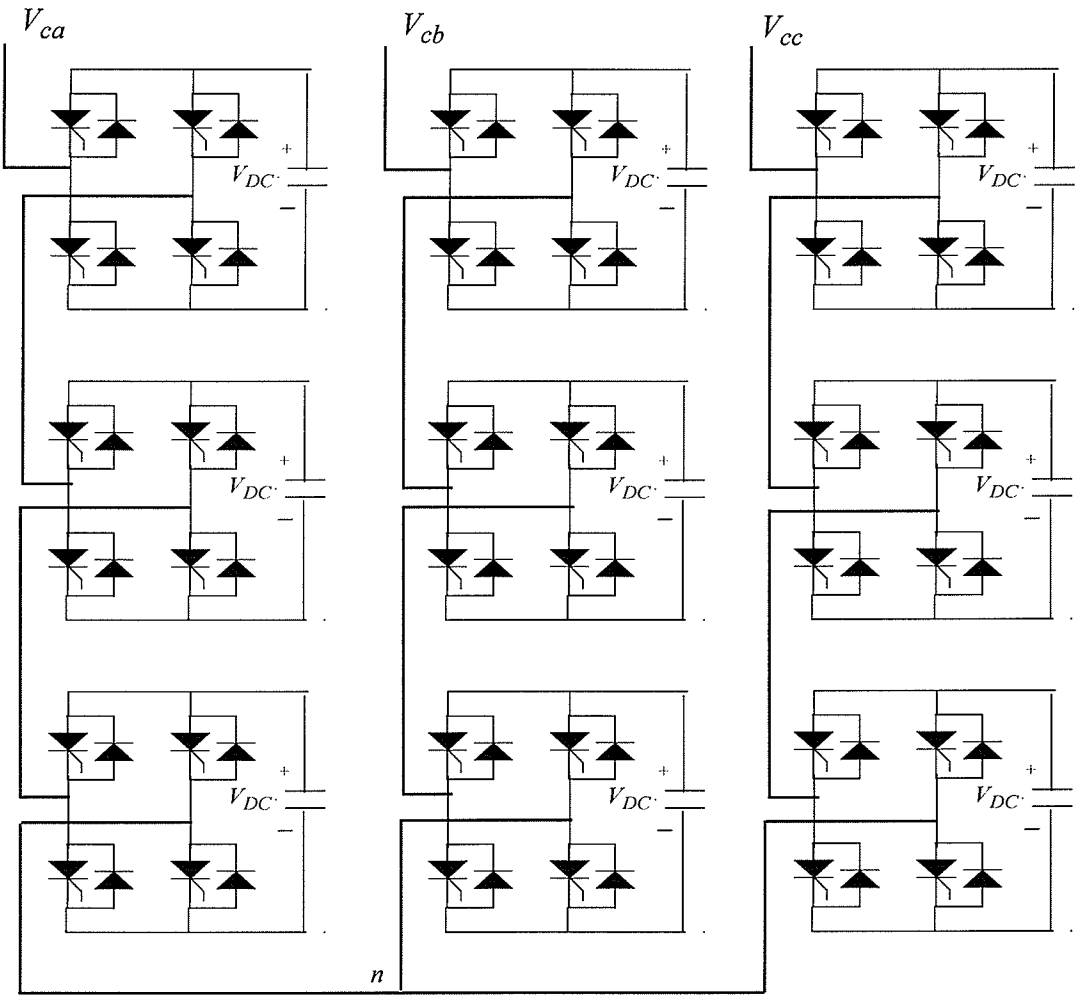


Figure 2.3 The Three Phase Y-structure 7-level Cascade Inverter

It is clear from Figure 2.3 that to have M-level cascade multilevel inverters we need $\left(\frac{M-1}{2}\right)$ H-bridge units in each phase. Each H-bridge inverter can generate three level outputs, V_{dc}, 0, and $-V_{dc}$. Figure 2.4 shows the structure of one unit of H-bridge inverter and its three level output voltage waveform. And the output voltage of M-level inverter is a simple sum of the M-rectangular waveform from each H-bridge inverter for each phase. There are many switching techniques to control the output voltage of the H-bridge inverter. We will discuss two of them the Fundamental Frequency Switching (FFS) method and the Pulse Width Modulation (PWM) technique in a later section.

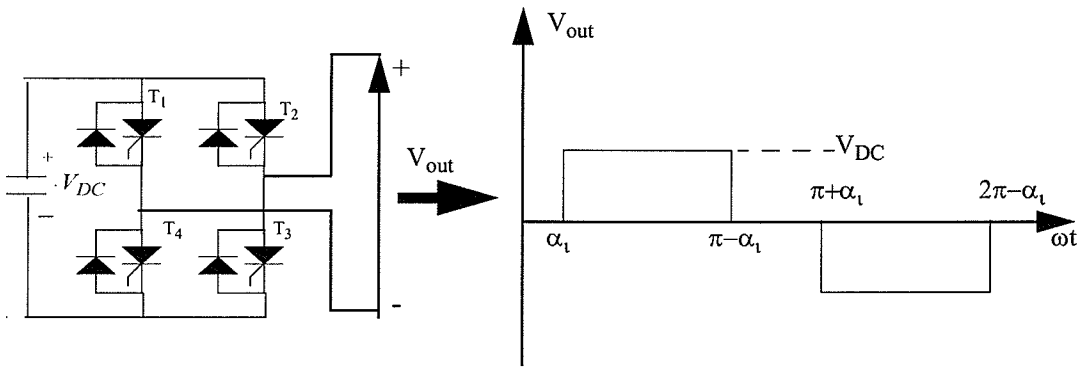


Figure 2.4. The H-bridge Inverter and its Three Level Output Voltage Waveform

2.3.2 The Advantages and Disadvantages of Cascade Multilevel Inverter

There are three types of multilevel inverters as stated before, the most common two of them are the cascade type and the diode-clamped type. The following are some of the advantages of the cascade type compared to diode-clamped type.

1- The diode-clamped configuration requires a very large number of clamping diodes where the cascade configuration does not require clamping diodes.

2- In the case of the cascade configuration, the packaging and physical layout is very simple in comparison with diode-clamped configuration due to its modular structure. It is constructed by cascading several voltage source H-bridge inverters.

3-The problem of dc voltage unbalancing between the capacitors is more severe in the case of the diode-clamped configuration than in case of the cascade configuration, as in case of cascade type each H-bridge can be controlled independently.

The cascade converter has the following disadvantages:

1) The dc voltage unbalancing between the capacitors of each inverter makes it difficult to regulate the output voltage of the STATCOM with cascade multilevel inverter.

2) The dc voltage unbalancing makes system design, maintenance and stocking of spare parts complicated.

Different methods and control strategies have been investigated in resent years to overcome the dc voltage unbalancing between the capacitors of each H-bridge inverter. An installation with one of these methods is in service where an SVC, rated 0 to +225 Mvar at 400 kV is operating in East Claydon substation in Buckinghamshire, England [20]. The SVC comprises a fixed filter of 23 Mvar, a conventional TSC of 127 Mvar and GTO-based 33-level cascade inverter STATCOM rated at +/- 75 Mvar. The dc capacitor voltage

charging and balancing is accomplished by using a dual IGBT rectifier/inverter at each H-bridge, which are connected to an auxiliary power transfer bus at earth potential via a fully insulated auxiliary power isolating transformer (APIT). The rating of the inverter/APIT combination is 5 kVA at 7.5 kHz. Although the test study on the system showed good results, these results were accomplished at the expense of adding more devices and complicating the control system. On other hand, in this thesis an alternative approach illustrated in Chapter 3 based on the rotated switching scheme [19] of fundamental frequency is studied, which is more cost efficient and easier to implement.

2.3.3 The Output Voltage Control of the Cascade Multilevel Inverter

It is clear by examining the cascade inverter structure as described in Section 2.3.1 that the H-bridge inverter forms the building block of the cascade multilevel inverter, therefore by controlling of the individual H-bridge voltages, we can control the total output voltage of the cascade inverter. By referring to Figure 2.4 we can see that there are mainly three methods to control the output voltage of the H-bridge inverter. These method are as follows:

1- By controlling the output voltage pulse width by Fundamental Frequency Switching (FFS) method or PWM technique while keeping the dc voltage fixed. This can be done by controlling the firing angle value of the GTO.

2- By controlling the dc voltage value while keeping the output voltage pulse width fixed or by controlling the modulation index in case of PWM.

3- By controlling the both values of dc voltage and the output voltage pulse width.

The basis of selecting the method of controlling the inverter output voltage is dependent on the ability to control the total harmonic distortion. The second method will be adopted in this thesis to control the inverter output voltage as it makes it easier to implement the Selected Harmonic Elimination method (SHE), illustrated in the coming section, which keeps the total harmonic distortion low in the output voltage of the inverter. The dc voltage magnitude of the inverter will be controlled by controlling the phase angle difference between the fundamental of the converter output voltage (V_o) and the ac system voltage, which leads to control, of the magnitude of V_o and the reactive current produced by the STATCOM. There are mainly two switching methods to achieve the above objective, the Fundamental Frequency Switching (FFS) and the Pulse Width Modulation (PWM) Switching Techniques.

2.4 **Fundamental Frequency Switching (FFS) of GTO's**

Using the fundamental frequency switching (FFS) method [12], each GTO thyristor is switched on and off once during a power frequency (60 Hz) cycle.

As mentioned earlier, the H-bridge inverter forms the building block of the cascade multilevel inverters. For simplification let us consider one phase of a 7-level cascaded multilevel inverter as shown in Figure 2.5, it is clear from the figure that it consists of three H-bridge inverters per-phase, called HBI-1, HBI-2 and HBI-3.

To generate 7-level voltage waveform at the output terminal of the 7-level, single phase cascaded inverter shown in Figure 2.5, by applying FFS technique to each H-bridge inverter, let us start by examine the first H-bridge inverter (HBI-1). We can see that the main switching devices T_1, T_2, T_3 and T_4 can be any self-commutated devices such as a IGCT or an IGBT transistor (for lower rating). In one cycle period each switch must be turned on for π period and turn off for the remaining π period. If the H-bridge inverter switching devices turned on for π period, each switch as follow: T_1 at $-\alpha$ angle, T_4 at $(\pi-\alpha_1)$, T_3 at α_1 angle and T_2 at $(\pi+\alpha_1)$ angle and turn them off at $(\pi-\alpha_1)$, $2\pi-\alpha_1)$, $(\pi+\alpha_1)$ and $2\pi+\alpha_1$ angle, respectively. The inverter output voltage will be as follow: between the period zero to α_1, T_1 and T_2 are on then the load terminal will be connected to zero voltage, between the period α_1 to $(\pi-\alpha_1)$, T_1 and T_3 are on then the load terminal will be connected to the positive dc supply, between the period $(\pi-\alpha_1)$ to $(\pi+\alpha_1)$, T_4 and T_3 are on then the load terminal will be connected to zero voltage, between the period $(\pi+\alpha_1)$ to $2\pi-\alpha_1)$, T_2 and T_4 are on at this period the load terminal will be connected to negative dc supply voltage and between the period $2\pi-\alpha_1)$ to (2π), T_1 and T_2 are on then the load terminal will be connected to zero voltage. By this way three level outputs + V_{dc}, 0, - V_{dc} can be generated, as shown in figure 2.6 (a). If the same role is applied to other two H-bridge inverter HBI-2 and HBI-3 but with different firing angles α_2 and α_3. Where

$$\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$$

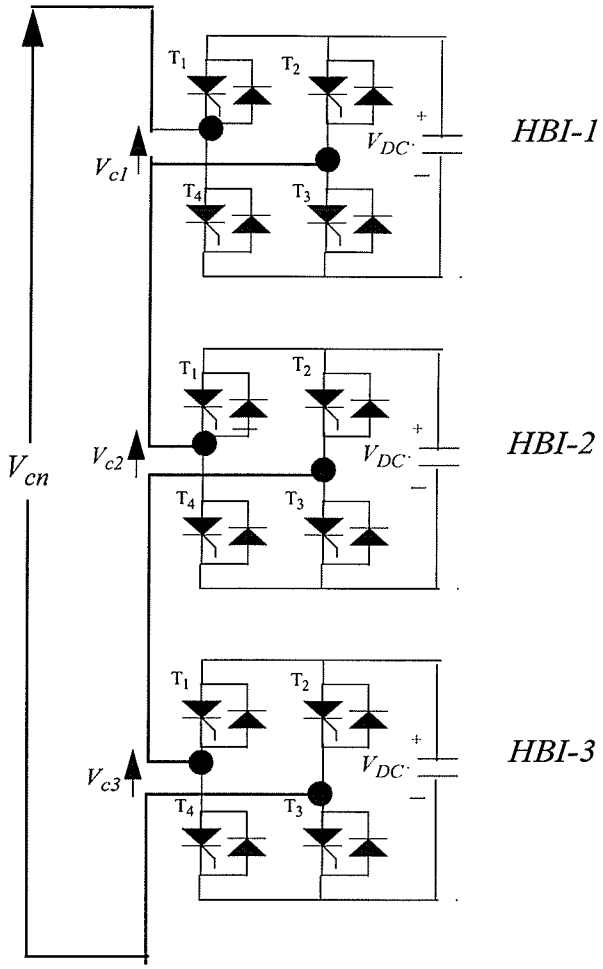
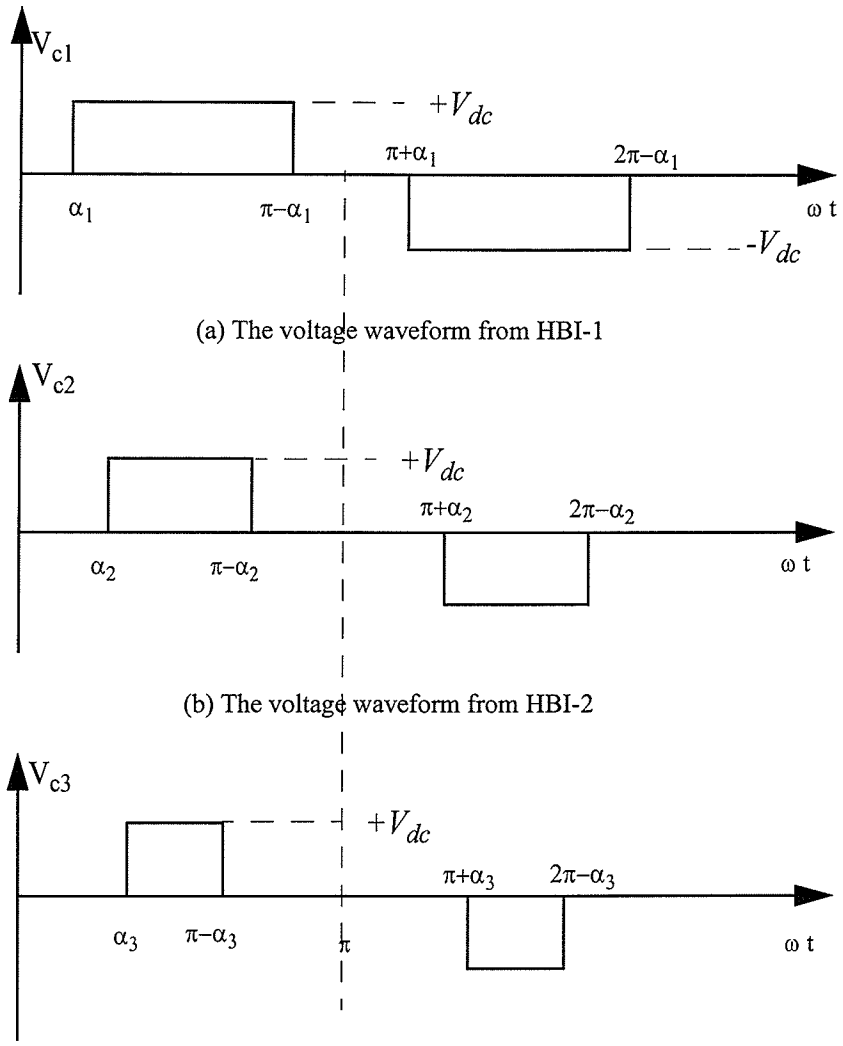


Figure 2.5: One Phase of a 7-Level Cascaded Multi-Level Inverters

we generate an output voltage from each H-bridge as shown in Figure 2.7 (b & c). Then by simple sum of the three rectangular waveforms generated from HBI-1, HBI-2 and HBI-3 we can achieved our 7-level voltage waveform as shown in Figure 2.7.

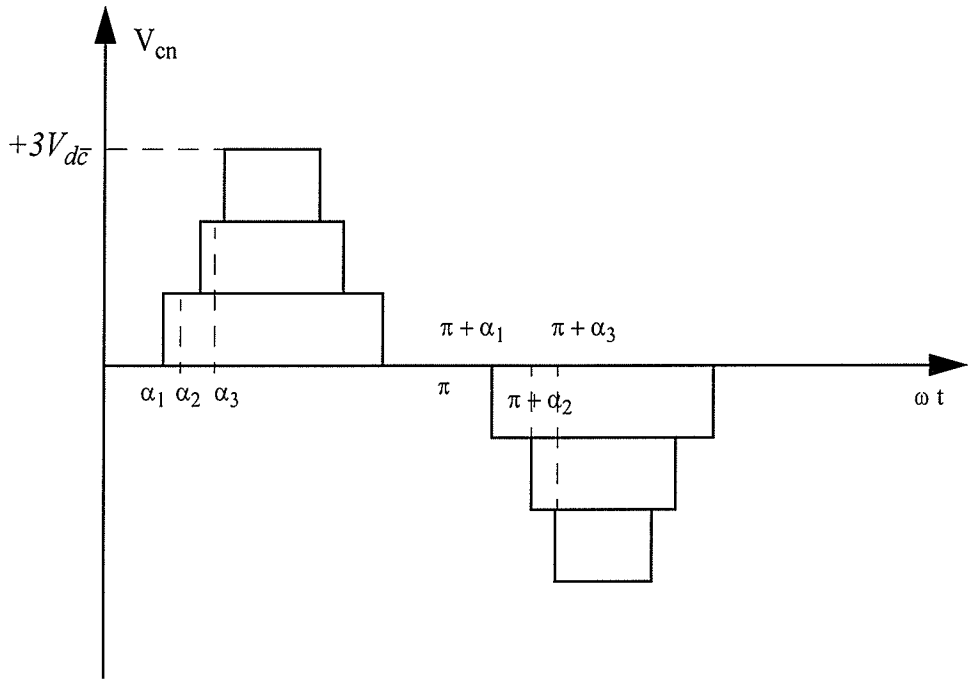


(a) The voltage waveform from HBI-1

(b) The voltage waveform from HBI-2

(c) The voltage waveform from HBI-3

Figure 2.6 The Output Voltage Waveform for Each H-Bridge


V_{cn}
$+3V_{d\bar{c}}$
α_1 α_2 α_3
$\pi + \alpha_1$
$\pi + \alpha_3$
π
$\pi + \alpha_2$
ω t

Performing the Fourier Transform for this waveform, the total output voltage can be obtained as:

$$E(\omega t) = V_c(\alpha_1, \omega t) + V_c(\alpha_2, \omega t) + V_c(\alpha_3, \omega t)$$

Where

$$V_c(\alpha_x, \omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_x\right)\sin(n\omega t)$$

Where $x = 1,2$ or 3
$n = 1, 3, 5, 7,.....$

$$E(\omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_1\right)\sin(n\omega t) + \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_2\right)\sin(n\omega t)$$

$$\frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_3\right)\sin(n\omega t)$$

$$E(\omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)]\sin(n\omega t)$$

Where n = 1, 3, 5, 7,.....

From the formula (2.1), the magnitude of the Fourier coefficients can be obtained, which is equal to the magnitude of the n^{th} harmonic normalized to V_c as follows:

$$H(n) = \frac{4}{\pi n}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] \qquad \text{Eq.....2.2}$$

Where $n = 1, 3, 5, 7,.....$

As we mentioned before that the α_1, α_2, and α_3 can be chosen at any angle within the range of $\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$, on the basis of getting a lower harmonic content or a larger fundamental voltage. The degree of freedom, in choosing the switching angles is equal to (M-1)/2, where M is the level of the multilevel inverter. In the present case with M = 7, the system has three degrees of freedom. Therefore α_1, α_2, and α_3 can be selected at such values to control the magnitude of any three harmonics, if any one of them needs to be eliminated, then equation (2.2) is set to zero for that particular value of n. For example, if the 5^{th}, 7^{th} and 11^{th} harmonics, are to be cancelled, the write three equations, by substituting n=5, 7, and 11 in Equation 2.2, are as follow:

$$\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) = 0$$

$$\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) = 0 \qquad \text{Eq..... 2.3}$$

$$\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) = 0$$

The set of Equations (2.3) are nonlinear transcendental equations which can be solved by an iterative method. By using Newton-Raphson method to solve these equation different sets of solutions can be obtained where each set of solution has a different modulation index (MI). The MI is defined as:

$$MI = \frac{V_{c(out)}}{3V_{dc}} \qquad \text{Eq....2.4}$$

It is obvious that the magnitude of the fundamental component and the harmonic content in the inverter output voltage will change with these switching angles which are listed in Table 2.2. In other words, the inverter waveform can be optimized to achieve the larger modulation index (MI) and/or the best Total Harmonic Distortion factor which was defined as the ratio of the root-mean-square of the harmonic content to the root-mean-square of the fundamental quantity [13], which is expressed as a percent of the fundamental, that is:

$$THD = 100\sqrt{\sum_{n\neq 1,3n}\left(\frac{V_n}{V_1}\right)^2}$$

Table 2.2 Calculated Switching Angles for Different MI

H(1)	α_1 (degree)	α_2 (degree)	α_3 (degree)	THD
1.0	11.68	31.18	58.58	7.6%
0.9	7.09	15.68	36.17	5.9%
0.85	22.77	49.38	64.57	9%

Figure 2.8 shows the line to neutral output voltage waveform of 7-level cascaded inverter using the FFS method with $\alpha_1 = 7.09$ degrees, $\alpha_2 = 15.68$ degrees, and $\alpha_3 = 36.17$ degrees. Figure 2.9 illustrates the Fourier analysis of the obtained waveform, from the Figure 2.8, it can be seen that 5, 7, and 11 harmonic orders can be eliminated . Although triplen order harmonics, such as third, and ninth, in the line to neutral output voltage waveform exist, the line to line voltage will not have any triplen harmonics. The result verify this method and the obtained switching angle values. The same set of switching angles will be used for the simulation studies in Chapter 4.

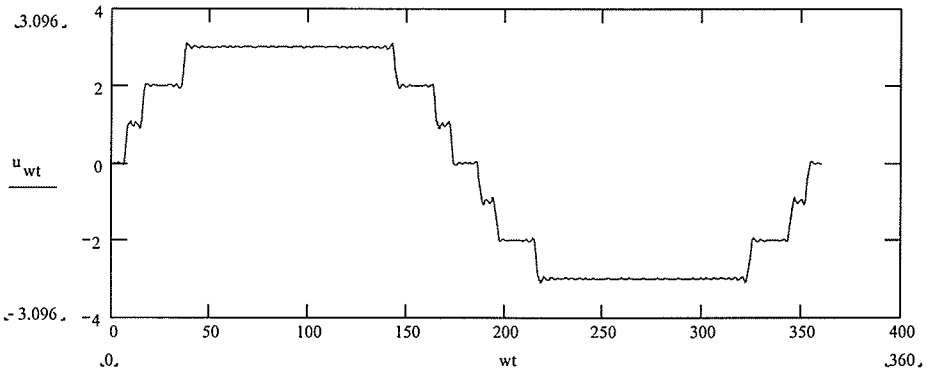


Figure 2.8: The Output 7-Level Voltage Waveform Using FFS Method.

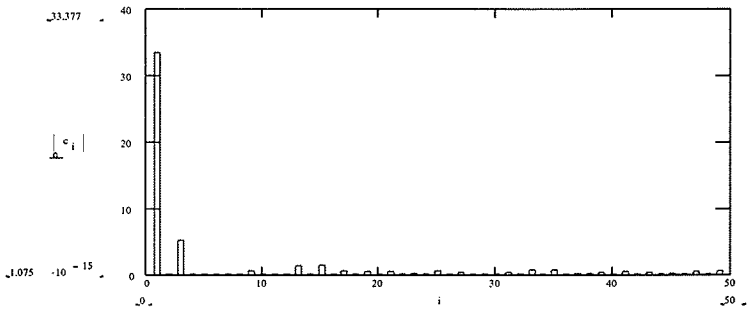


Figure 2.9: Harmonic Spectra For Line to Neutral 7-Level Voltage Output Waveform Using FFS Method

2.5 Pulse Width Modulation (PWM) Switching Techniques

Various PWM techniques applied to the multilevel converter have been studied during the past two decades. Generally, the PWM techniques can be classified into the two categories: the triangle intersection techniques and the direct digital techniques (space voltage vector). Both are extensions of traditional two-level PWM strategies to multilevel. Recently, with the development of digital technology, the space voltage vector PWM is widely used, due to not only its relatively easily hardware implementation, but also its features of good dc-link voltage utilization and low current ripple. But this method has a very significant drawback that if the voltage level is more than five, the control algorithm becomes too complex to implement. So it is reasonable to adapt the triangle intersection techniques in high level applications. In this section the principles and the features of three kinds of triangle intersection PWM techniques applied to the cascade multilevel inverter will be described.

2.5.1 Subharmonic Pulse Width Modulation (SHPWM)

The control principle of the SHPWM [13] method is to use several triangular carrier signals with only one modulation wave per phase. For an n-level inverter, n-1 triangular carrier of the same frequency f_c and the same peak-to-peak amplitude A_c, are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulation wave is a sinusoidal of frequency f_m and amplitude A_m. At

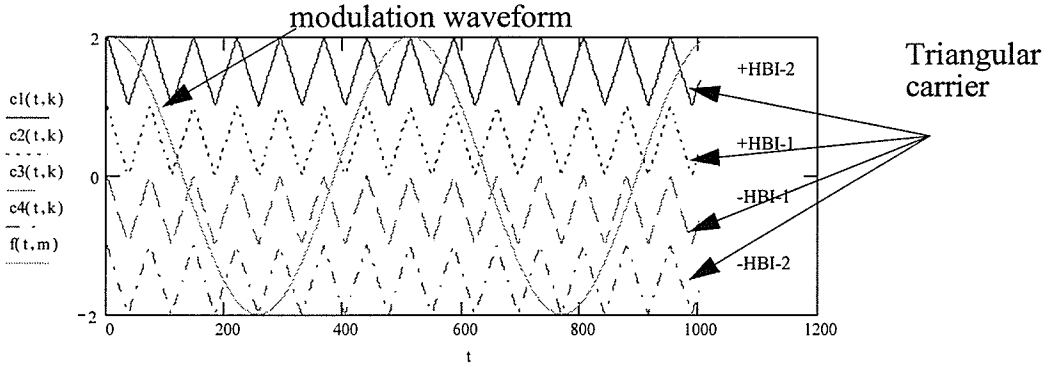
every instant each carrier is compared with the modulation waveform. Each comparison switches the device on if the reference signal is greater than the triangular carrier assigned to that device level; otherwise, the device switches off. In an n-level inverter, the amplitude modulation index (MI) and the frequency index (K) are defined as:

$$MI = \frac{A_m}{(n-1)A_c}$$

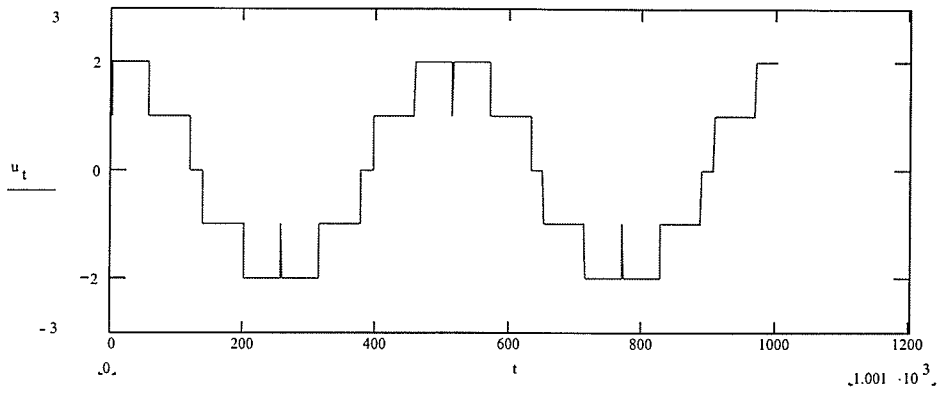
$$K = \frac{f_c}{f_m}$$

Where A_m: The amplitude of the modulation wave
A_c: The amplitude of the carrier wave
f_m: The frequency of the modulation wave
f_c: The frequency of the carrier wave

Figure 2.10(a) shows the principle of SH PWM for n=5, k=7 and MI=1.0 from the figure. it can be seen that we have 4 carrier waveforms, the two carrier which are above the zero reference controlling the switching of the HBI-1 and HBI-2 during the positive period of the fundamental cycle, while hand the other two carriers which are below the zero reference take care of the negative periode as shown in Figure 2.10(a).



(a)



(b)

Figure 2.10: The Principle of The SHPWM for n = 5, k = 7, and MI = 1.0

2.5.2 Triangular Carrier Phase Shifting PWM Technique (PS PWM)

The triangular carrier phase-shifting PWM techniques is a PWM technique [14] specially suitable for cascaded multilevel inverters. The control principle of the PS PWM method is the switching logic controller, in which each H-bridge module receives its unique triangular carrier, which is phase shifted with respect to its neighbors. As illustrated in Figure 2.11, this method uses multiple converter modules, the device's of which are switched in staggered intervals to create the effect of a high sampling rate, its effective triangular carrier number is equal to n*k, where n is the number of converter modules. The triangular carrier phase shift for n modules is $\theta_{sh} = \frac{2\pi}{nk}$

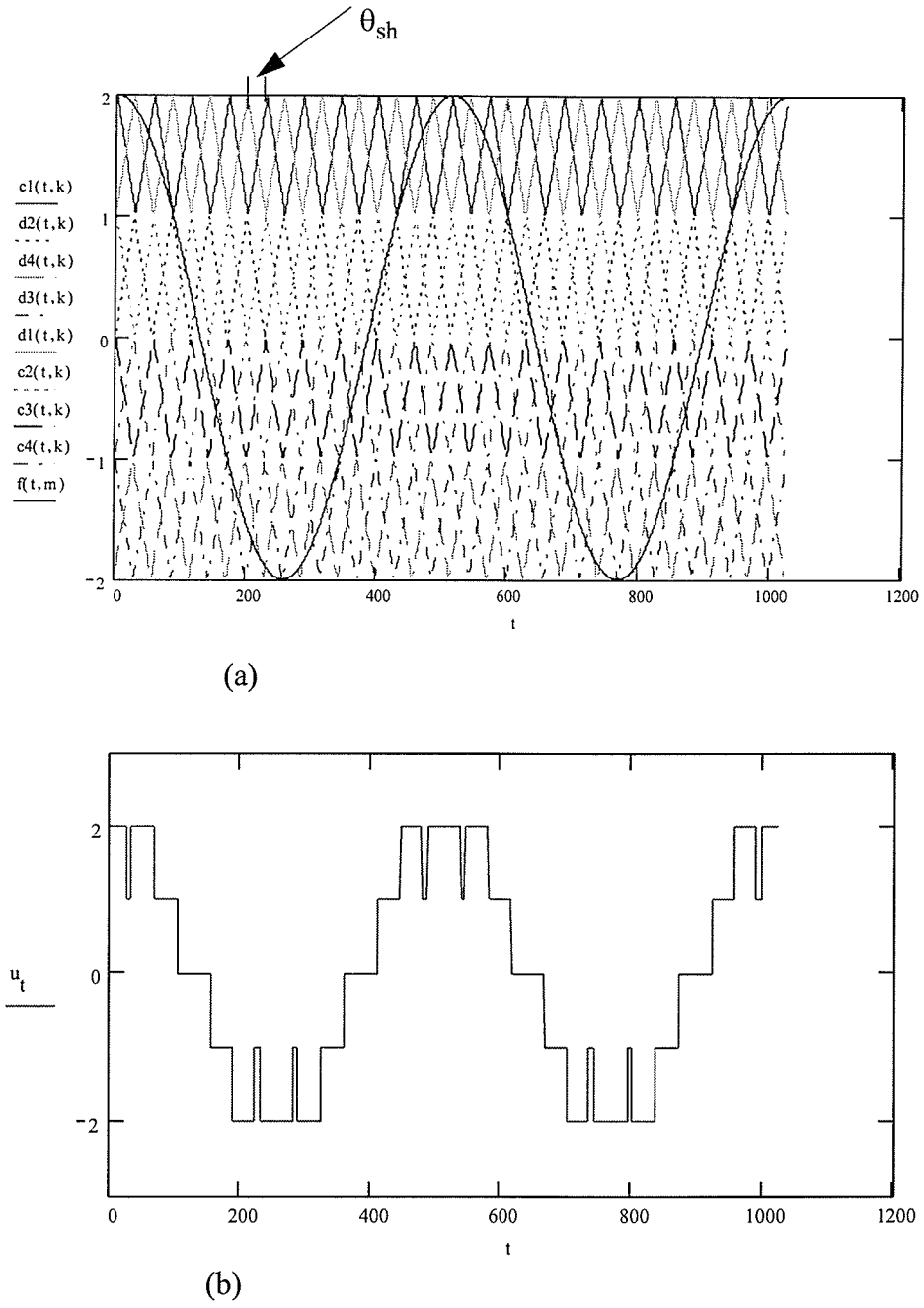


Figure 2.11(a & b): The Principle of The PS-PWM for n = 5, k = 9, and MI = 1.0

2.5.3 Switch Frequency Optimal PWM

Switch Frequency Optimal PWM (SFO PWM) as proposed by Steinke [15], is another triangle carrier based PWM technique, which is something like the SHPWM, except that a zero sequence voltage is added to each of the carrier waveforms. It means the instantaneous average of the maximum and minimum of the three reference voltages (V_a, V_b, V_c) are subtracted from each of the individual reference to obtain the modulation waveform, in other words:

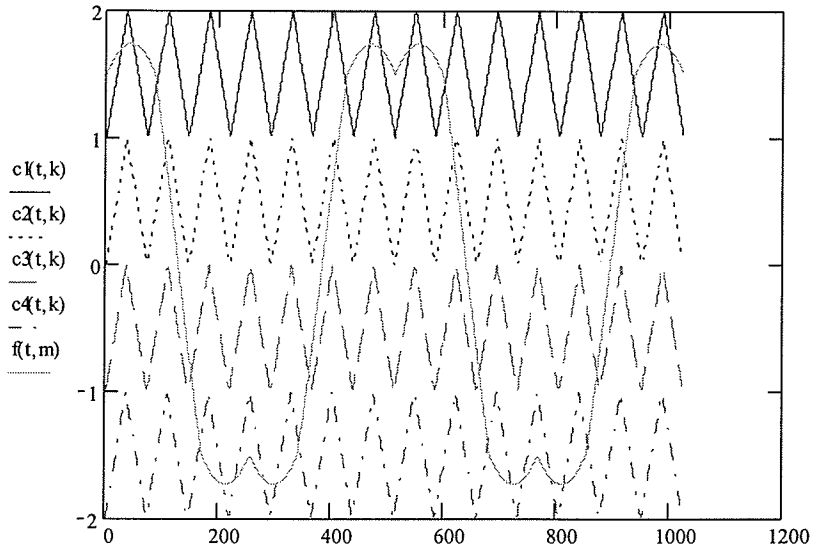
$$V_{zero} = \frac{max(V_a, V_b, V_c) + min(V_a, V_b, V_c)}{2}$$

$$V_a'' = V_a - V_{zero}$$

$$V_b'' = V_b - V_{zero}$$

$$V_c'' = V_c - V_{zero}$$

The algorithm above is convenient for microprocessor implementation and also analog implementation. The principle of SFO PWM is illustrated in Fig. 2.12.



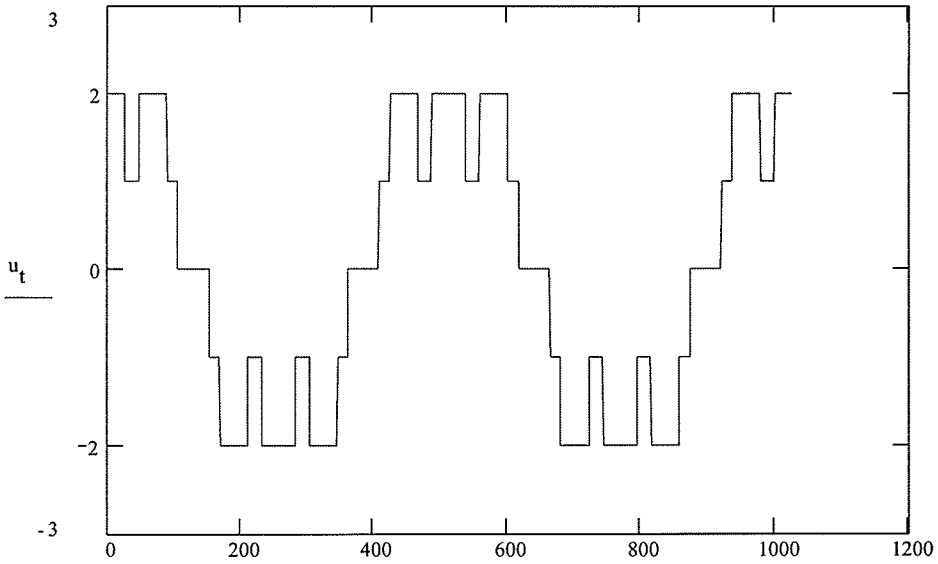


Figure 2.12: The Principle of SFO PWM For n = 5, k = 7, and MI = 1.0

2.6 Comment on Different Techniques of PWM

1- In multilevel converter application, if the number of voltage levels is more than five, then in terms of control simplicity, it is clear from comparing the control principle of different techniques of PWM that the triangular carrier PWM technique has the simplest control.

2- For a single-phase system, PS PWM has better control effect

3- For a three-phase system, SFO-PWM which only works with three phase system has a better control effect as we are able to achieve lower harmonic content and a higher modulation index.

4- In general it can be concluded [16] that in multilevel triangular carrier PWM strategies, there are at least three control degrees of freedom in triangular carrier: frequency, phase and amplitude and also at least three control degrees of freedom in modulation waveform: amplitude, frequency and zero sequence. Composite of some of these control freedom degree can generate a good number of PWM strategies.

2.7 Comparison Between FFS Method And PWM Techniques

In this section FFS method will be compared with other two types of PWM methods the SHPWM method and SFO PWM method as the PS PWM is special case of the SHPWM, our comparison are based on reducing Total Harmonic Distortion (THD), power losses, and transient response. Off course, the best control strategies is the one

which has the lowest harmonic distortion, lowest power losses, and the faster transient response.

2.7.1 Total Harmonic Distortion

To show the performance of the various techniques FFS method, the SH-PWM and SFO-PWM techniques with respect to the (THD) of the output line voltage, the sample Mathcad programs are listed in Appendix A. By running the above mentioned Mathcad programs for 5-level inverters and 7-level inverters, the THD was calculated with different modulation index for each switching technique. The results are summrized as: Table 2.3 for FFS method, Table 2.4 for SH-PWM technique, and Table 2.5 for SFO-PWM technique.

Table 2.4: Typical Calculation Results Using SH-PWM

Waveform level	Frequency ratio (k)	Modulation Index (MI)	THD
5	9	1	12.1%
		0.9	14%
		0.85	15.2%
		0.8	15.7%
		0.7	19.6%
		0.6	20.3%
		0.5	33.0%
		0.4	37.6%

Waveform level	Frequency ratio (k)	Modulation Index (MI)	THD
7	9	1	6.8%
		0.9	10.1%
		0.85	11.6%
		0.8	9.5%
		0.7	14.5%
		0.6	14%
		0.5	11.6%
		0.4	16.6%

Table 2.5: Typical Calculation Results Using SFO-PWM

Waveform level	Frequency ratio (k)	Modulation Index (MI)	THD
5	9	1	13.1%
		0.9	13.4%
		0.85	16%
		0.8	18.4%
		0.7	19.2%
		0.6	27%
		0.5	35.6%
		0.4	39.2%
7	9	1	12.4%
		0.9	12.8%
		0.85	12.9%
		0.8	11%
		0.7	12.8%
		0.6	13.4%
		0.5	19.6%
		0.4	21.3%

Table 2.3: Typical Calculation Results Using FFS.

Waveform level	THD
5	10.9%
7	7.6%

From the above Tables it can be concluded that:

1- As for higher level order of inverters the total harmonic distortion goes down for all types of switching techniques.

2- For SH-PWM technique, the modulation index MI=1 will give the best THD as shown in Table 2.4 which is equal to 6.8% for 7-level waveform.

3- For SFO-PWM technique, the modulation index MI = 1 will not always give the best THD as shown in Table 2.5 that the best THD value is at MI = 0.8 for 7-level waveform.

4- For 5-level waveform the FFS method has the best THD which equal to 10.9%, on the other hand, for 7-level waveform SFO-PWM technique has the best THD at MI=1 which is equal to 6.8%. In general the THD value depends on the MI and the level order.

2.7.2 Power Losses

The main element in determining the power losses is that the power losses due to switching of the power electronics switch on and off, therefore to compare the power losses for the different switching methods the number of GTO thyristor switched per fundamental cycle should be calculated. By referring to Section 2.3 where the principle of each switching techniques was discuss it can be concluded:

1- The FFS method has the minimum number of GTO thyristors switched per fundamental cycle, which is equal to 12 in case of 7-level waveform.

2- In case of different techniques of PWM, the number of switches is dependent on the modulation index as well as on the frequency ratio (K) but in general under the same condition the SH PWM has the minimum switching number in comparison with other PWM techniques.

2.7.3 Transient Response

The comparison between FFS method and PWM techniques will be studied in detail in Chapter 4 where we compare the transient response of the STATCOM when applying FFS method and SH-PWM technique to maintain the line voltage under transient load.

CHAPTER 3 System Modeling and Control Strategies

3.1 Introduction

In the first part of this chapter, a general mathematical model for the converter based STATCOM suitable for optimal power flow study will be developed. There are several solution methods for optimal power flow available. In this chapter the OPF problem is solved by Nonlinear Interior Point Methods [17].

In the second part of this chapter, the detailed control system analysis to determine the response of a STATCOM using either the fundamental frequency switching or PWM techniques is given which also includes the analysis of negative sequence and harmonic voltage components in the transmission system.

3.2 STATCOM Operation

The STATCOM like its conventional counterpart, the SVC (Static Var Compensator), is used to control transmission voltage by reactive power shunt compensation.

Typically, a STATCOM consists of a coupling transformer, an inverter and a dc capacitor, which is shown in Figure 3.1. For such an arrangement, in ideal steady state analysis, it can be assumed that active power exchange between ac system and the STATCOM can be neglected, and only reactive power can be exchanged between them. However, if a storage device is connected with the STATCOM, it can then exchange active power with the ac system.

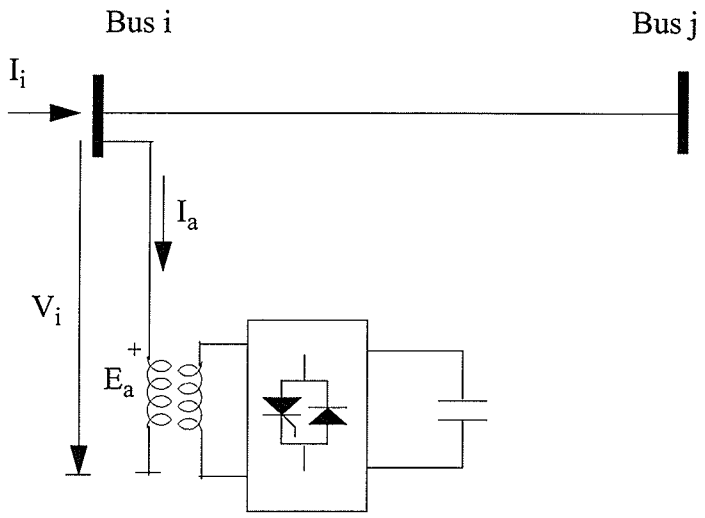


Figure 3.1: STATCOM Operation Principle

Based on the operating principle shown in Figure 3.1, the equivalent circuit of the STATCOM can be derived, which is given in Figure 3.2. In principle, the STATCOM output voltage can be regulated so that the reactive power of the STATCOM can be changed.

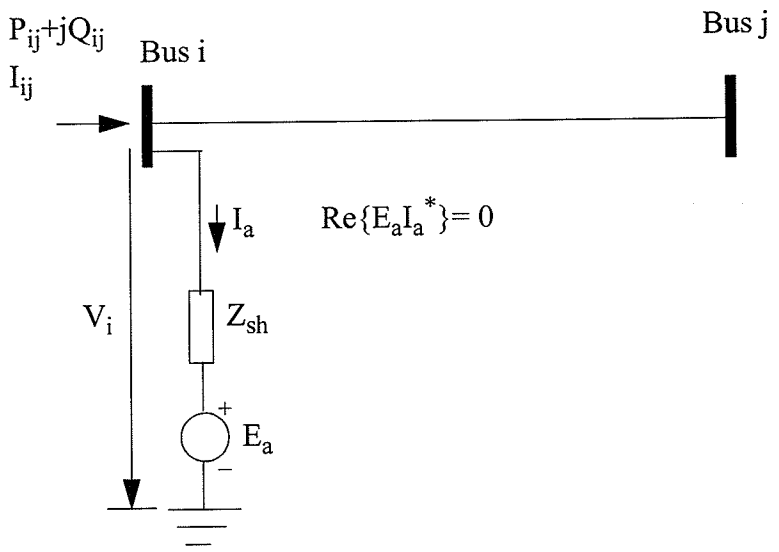


Figure 3.2: STATCOM Equivalent Circuit

According to the equivalent circuit of the STATCOM shown in Figure 3.2, suppose $\mathbf{E_a} = \mathbf{E_a}\angle\theta_a$ the voltage on the inverter side, $\mathbf{V_i} = \mathbf{V_i}\angle\theta_i$ the i bus bar voltage, then the power flow constraints of the STATCOM are:

$$\mathbf{P_{ij}} = \mathbf{V_i^2 g_{sh}} - \mathbf{V_i E_a}(\mathbf{g_{sh}}\cos(\theta_i - \theta_a) + \mathbf{b_{sh}}\sin(\theta_i - \theta_a)) \qquad \text{Eq. 3.1}$$

$$\mathbf{Q_{ij}} = -\mathbf{V_i^2 b_{sh}} - \mathbf{V_i E_a}(\mathbf{g_{sh}}\sin(\theta_i - \theta_a) - \mathbf{b_{sh}}\cos(\theta_i - \theta_a)) \qquad \text{Eq. 3.2}$$

Where

$$g_{sh} + jb_{sh} = \frac{1}{Z_{sh}} \qquad \text{Eq. 3.3}$$

Operating constraint of the STATCOM (active power exchange via the dc link) is:

$$P_{exchange} = Re(E_a I_a') = 0$$

Or

Eq. 3.4

$$E_a^2 g_{sh} - V_i E_a (g_{sh} \cos(\theta_i - \theta_a) + b_{sh} \sin(\theta_i - \theta_a)) = 0$$

The bus voltage control, and active and reactive power flow control constraints are as follows:

$$V_i - V_i^{Specified} = 0 \qquad \text{Eq. 3.5}$$

Where $V_i^{Specified}$ is the specified bus voltage.

3.3 Control Strategies

There are two control strategies adopted in this investigation, the first one is based on the fundamental frequency switching (FFM). As described in the second chapter, the reac-

tive output of the advanced static var compensator considered can be controlled by a single parameter: the phase angle between the output voltage of the inverter and the ac system voltage. This is because by controlling the phase angle between the inverter voltage and the ac system voltage the real power absorbed from, or supplied to, the dc storage capacitor can be controlled, and the voltage of this capacitor determines the amplitude of the voltage produced by the inverter and thereby the reactive power generated for, or absorbed from the ac system. Furthermore studies will be presented in this chapter to overcome the problem of unbalanced dc voltage of the storage capacitance which occurs when applying this control strategy.

The second strategy adopted in this investigation is based on the Pulse Width Modulation (PWM) switching techniques, as described in Chapter 2. In this strategy the modulation index is fixed and the phase angle between the two voltages is vaired to control the dc voltage, and hence the reactive power.

3.4 **Main Control Loops**

There are two main tasks that the control scheme has to achieve. One is to establish and maintain synchronism between the output voltage of the converter and the ac system voltage. The other is to control the phase angle between them to control the flow of real power into and out of the capacitor, therefore controlling the inverter's output voltage and the reactive power flow.

To achieve the above mention tasks, two main control loops are needed. The first one is a phase locked loop (PLL), to establish and maintain synchronism between the output voltage of the inverter and system voltage. The second loop aims to adjust the phase angle between the inverter voltage and system voltage to control the reactive power flow. This is done by inputting to the proportional integral (PI) controller an error signal resulting from the difference between the rms value of the measured ac system voltage and the reference voltage. The output of the PI controller, representing the var demand of the ac system, is added together with the output of the phase locked loop to adjust the angular reference signal fed to the Gate Drive Logic. The main function of the Gate Drive Logic is to produce the desired firing pulse order. In Figure 3.3 it can be seen clearly how these two loops are integrated to control the STATCOM.

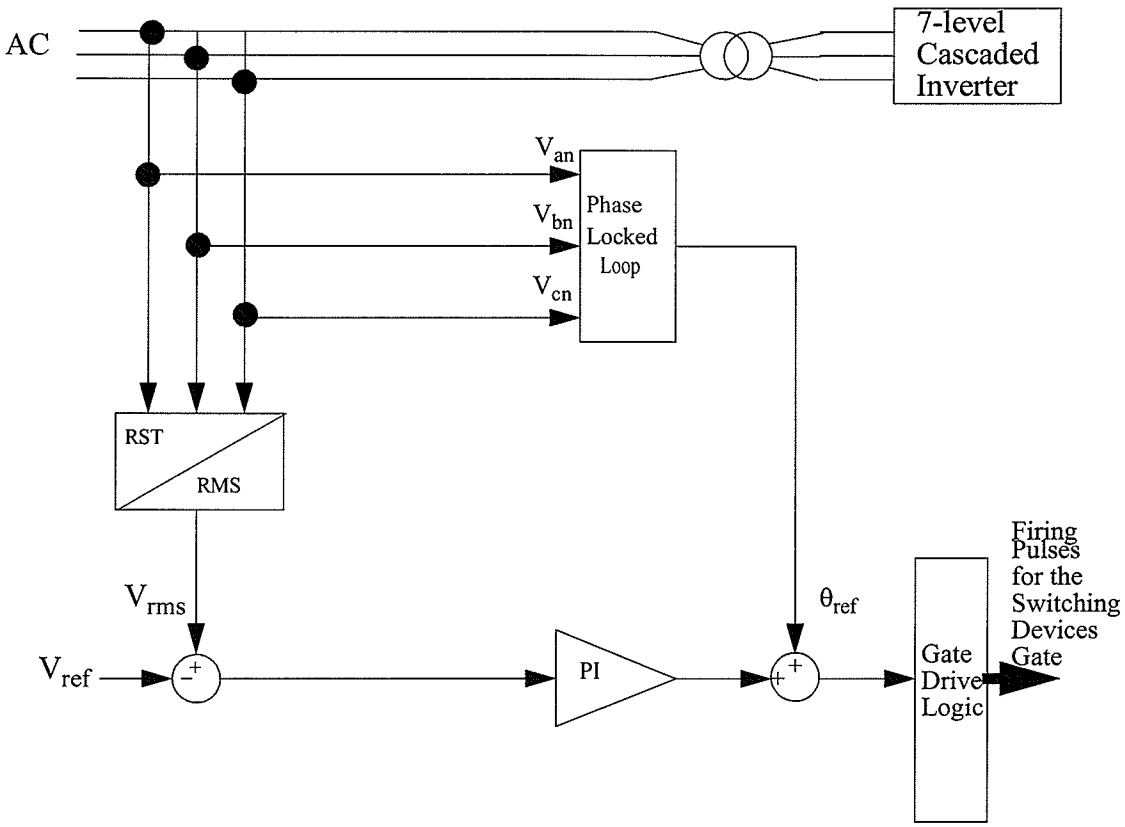


Figure 3.3: Basic Control Loop For The M-STATCOM

3.4.1 Phase-Locked-Loop

The output of the compensator must be able to stay synchronized with the source voltage and quickly keep up with external phase-shifts or frequency variations. A phase-locked-loop is used [18] to feed the angular displacements (θ_a, θ_b, θ_c) of the source voltage to the control system. Figure 3.4 shows the outputs of this phase-locked-loop.

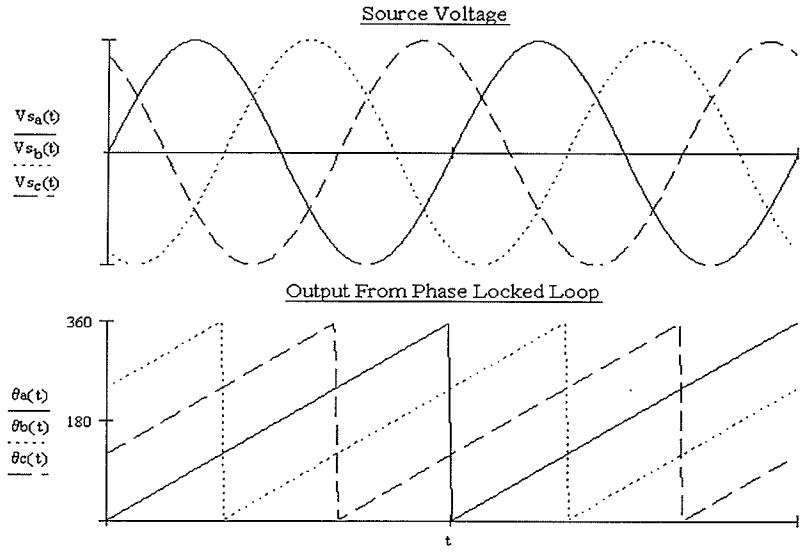


Figure: 3.4: Output Signals from Phase Locked Loop

3.5 A Rotated Switching Scheme of Fundamental Frequency

When applying FFS control strategy to control the phase angle difference between the inverter side and ac system voltages, it will be demonstrated in the following chapter that it has the following disadvantages:

a) Each H-bridge faces unequal stress.

b) Unbalancing dc voltage between the capacitors of each inverter makes it difficult to regulate the output voltage of STATCOM with cascade multilevel inverter.

To overcome the above problems a novel control scheme [19] of cascade multilevel inverter type STATCOM is used in this thesis. Figure 3.5 shows the synthesized phase voltage waveform of a 7-level cascaded inverter with three H-bridge inverters as it was explained in detail in Section 2.3. For a stepped waveform such as the one depicted in Figure 3.5 with 7-steps, the Fourier Transform for this waveform is as follows

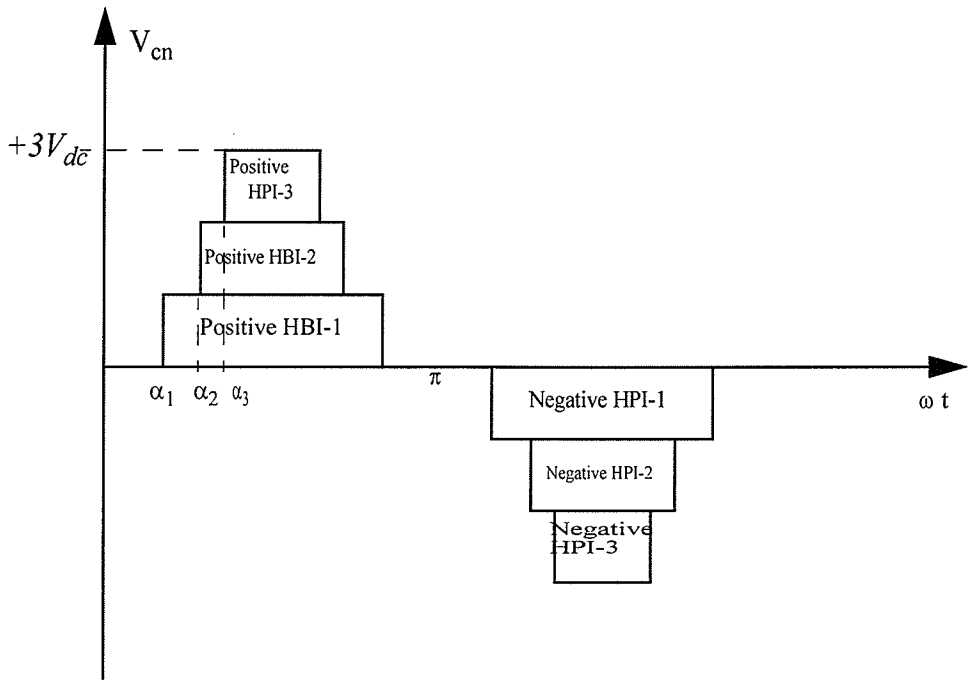


Figure 3.5 Waveforms of the 7-level Cascade Inverter

$$\mathbf{H(n)} = \frac{4}{\pi \mathbf{n}}[\mathbf{cos}(\mathbf{n}\alpha_1) + \mathbf{cos}(\mathbf{n}\alpha_2) + \mathbf{cos}(\mathbf{n}\alpha_3)] \qquad \text{Equation 3.7}$$

Where $n = 1, 3, 5, 7, \ldots\ldots$

As it was mentioned before that the α_1, α_2, and α_3 can be chosen at any angle within the range of $0 < \alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$, on the basis of getting a lower harmonic content or a larger fundamental. In this thesis the 5^{th}, 7^{th} and the 11^{th} harmonics are going to be eliminated, therefore Equation 3.7 can be written as the following three equations by substtution for n=5, 7, and 11:

$$\begin{aligned} \mathbf{cos}(5\alpha_1) + \mathbf{cos}(5\alpha_2) + \mathbf{cos}(5\alpha_3) &= 0 \\ \mathbf{cos}(7\alpha_1) + \mathbf{cos}(7\alpha_2) + \mathbf{cos}(7\alpha_3) &= 0 \\ \mathbf{cos}(11\alpha_1) + \mathbf{cos}(11\alpha_2) + \mathbf{cos}(11\alpha_3) &= 0 \end{aligned} \qquad \text{Equation 3.8}$$

equation 3.8 can be solved by an iterative method to find the value of α_1, α_2, and α_3.

In order to overcome the dc voltage unbalance and to have an equal stress on switching devices in each H-bridge inverter, the switching patterns are rotated every half cycle,

as shown in Figure 3.6, where HBI-1, HBI-2 and HBI-3 are the switching pattern of each H-bridge.

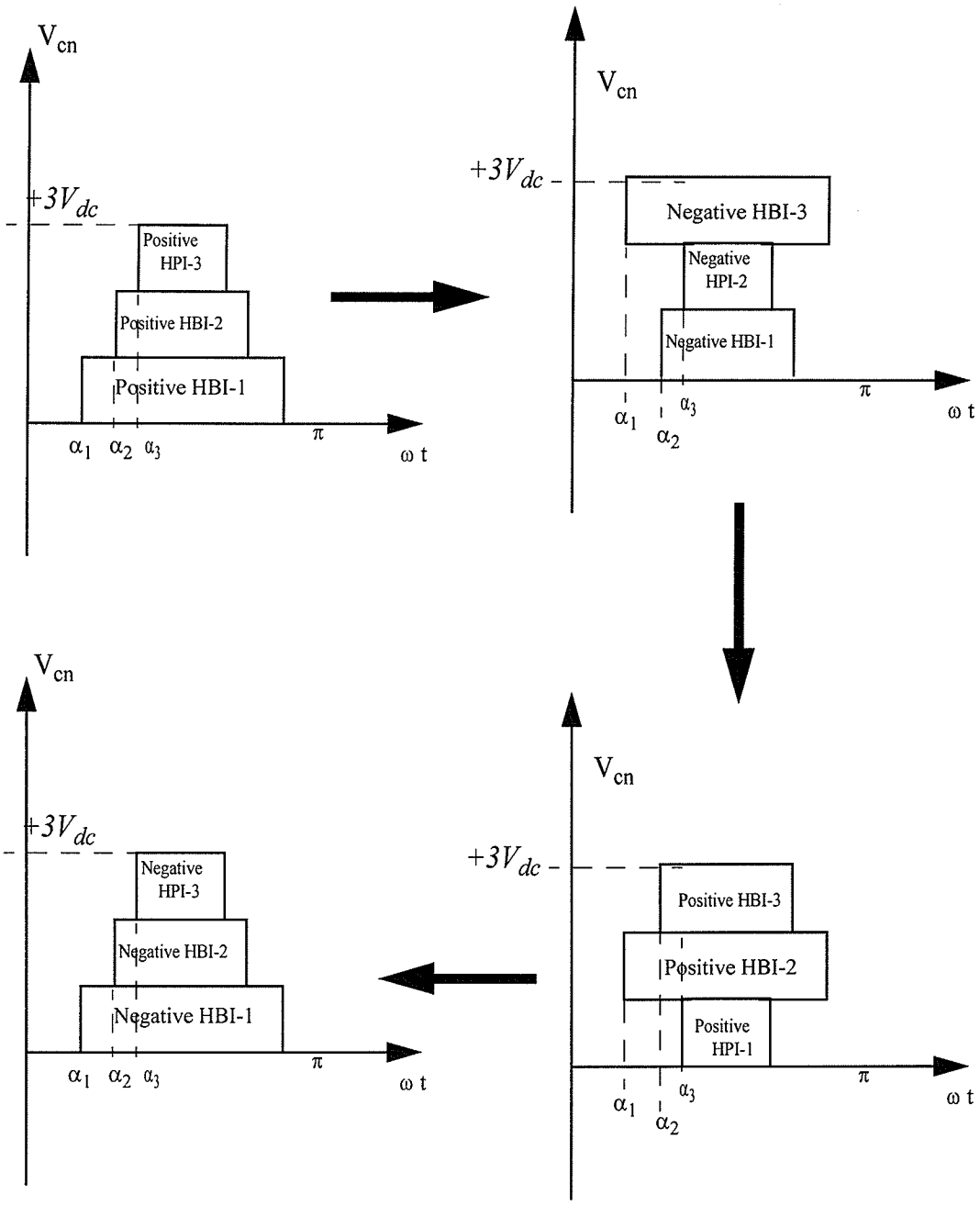


Figure 3.6: Method of Single Pulse Rotation Every Half Cycle

Figure 3.7 shows the control logic scheme of rotated switching pattern.

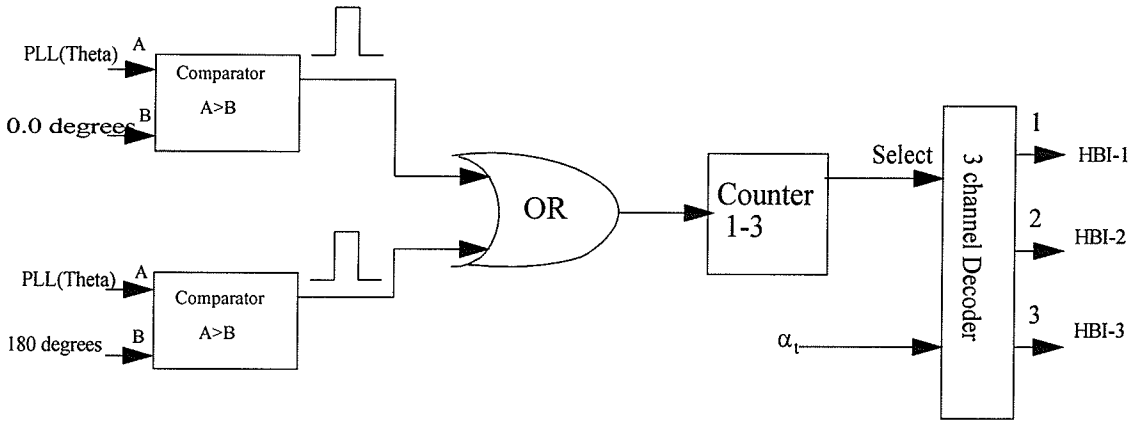


Figure 3.7: Control Logic Scheme of Rotated Switching Pattern.

As a result of the above rotation switching method, all dc capacitors are equally charged and discharged each half cycle. This means that each switching device in HBI modules is turned on and off equally. So, the dc voltage of capacitor is balanced in each HBI modules. Each bridge has equal charge / discharge on each capacitor.

3.6 Method of Pre-Charging The Inverter

An economic and convenient approach is to use the ac system to start-up the system directly because the reverse- conducting diodes of the GTO thyristors in the H-bridge inverter, form an ideal single phase full wave rectifier. If the inverter is connected to the ac system while the GTO thyristors are blocked, the dc capacitor of the inverter will be charged by the ac system voltage through the reverse-conducting diodes of the GTO thyristors, thereby the constant dc capacitor voltage can be established. However, there may

be overcurrent problems caused by the charging current of the dc capacitor or overcharging of the capacitors because of the leakage reactance of the transformer.

To avoid these problems, a pre-insertion resistor is used in the pre-charging circuit.

CHAPTER 4 Test Studies

Based on the previous analysis and discussion, a 7-level cascaded H-bridge inverter was chosen as candidate design for M-STATCOM. The investigation will study the operation of the M-STATCOM in areas such as: start-up of the inverter to charge the dc capacitors, steady state performance of the device, dynamic behavior of the M-STATCOM and controlling and balancing the capacitor voltage. The above study is done by using two switching methods, the first one is the FFS method with pulse rotation and the second method is PWM switching techniques. The system is digitally modelled to obtain the study result. Simulation activities are carried out using the PSCAD/EMTDC program. PSCAD/EMTDC is an electromagnetic transient simulation program, with a graphical interface, for simulation of complex electrical power networks and the associated control [20].

4.1 EMTDC System Model

To demonstrate the results of the above mentioned studies, and to show the effects of the two control strategies as mentioned above, a single phase equivalent circuit of the test system used in this study is shown in Figure 4.1, comprising of an infinite power source, a transformer with leakage inductance, an inductance and resistance representing the transmission line and a resistive / inductive load.

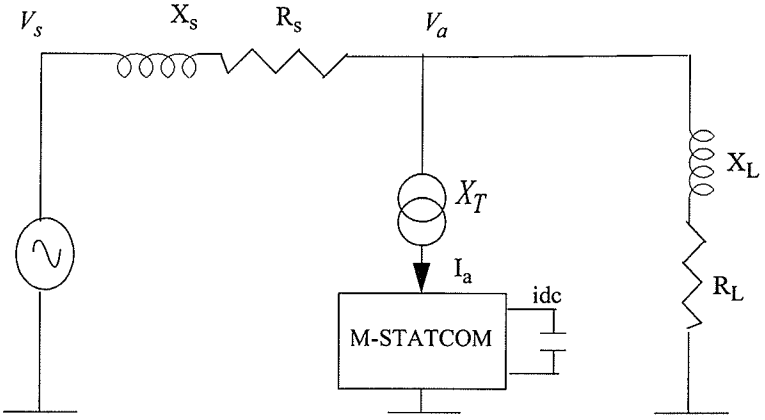


Figure 4.1: A Schematic Diagram of the Simulation Test System

The rating of the system and the parameters values of the system is given in Appendix B. The control system is designed to control the reactive power of the STATCOM to maintain the system voltage at the desired level, when load is changed.

4.2 Operational Characteristics

4.2.1 Start-up of The STATCOM

As mentioned in Chapter 3 that the most economic and convenient approach is to use the ac system to start-up the system directly utilizing the reverse-conducting diodes of the

GTO thyristors in the H-bridge inverters. Figure 4.2 shows dc capacitance voltage and charging current during the start-up of the STATCOM without including a pre-insertion resistor,in which the STATCOM is turned on at 0.035 s thereby the invertervoltage is established.

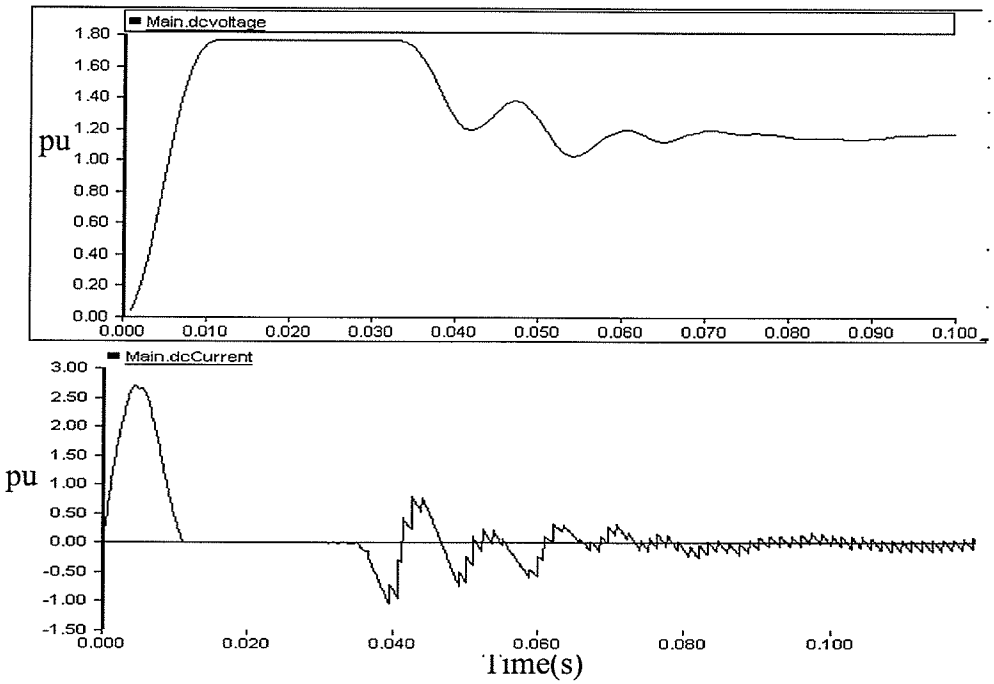


Figure 4.2: The Capacitance Current and Voltage During the Start-up Without a Pre-insertion Resistor.

As expected, the pre-charging current of the inverter is high, which gives a peak current of 2.6 pu. It is well known that the value of the charging current depends on the capacitor size of the inverter, therefore for large capacitance on the dc side of the inverter to have less ripple on dc voltage across the capacitance will result in increased the peak value of the pre-charging current.

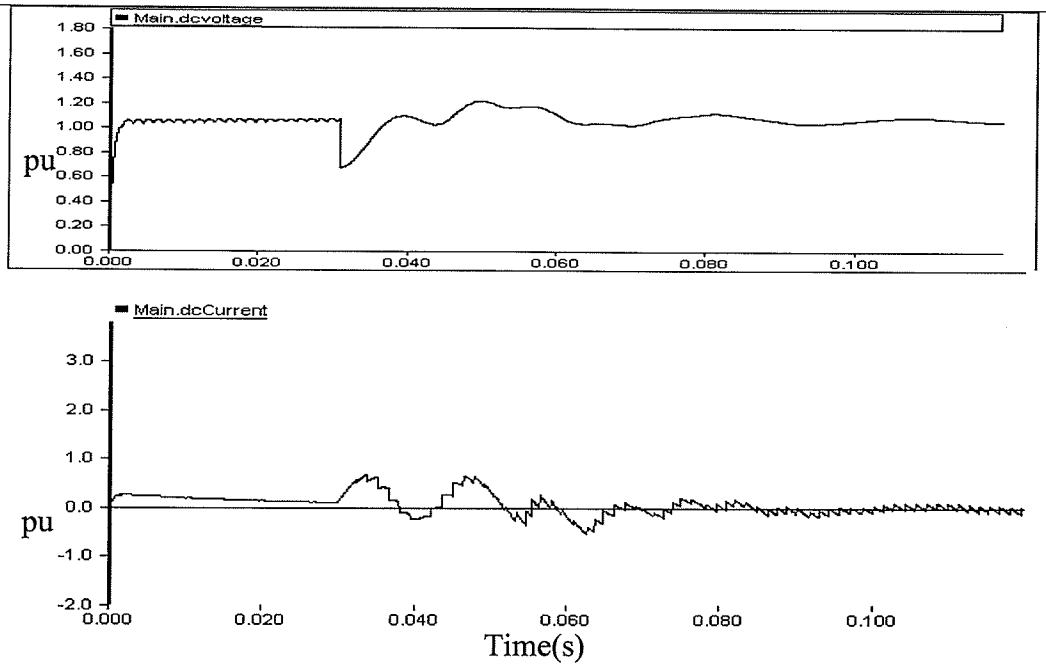


Figure 4.3: The Capacitance Current and Voltage During the Start-up With a Pre-insertion Resistor

On the other hand, as shown in Figure 4.3 the capacitance dc pre-charging current of the inverter is reduced significantly when a pre-insertion resistor is used. The pre-insertion resistor is first connected between the ac system and the STATCOM at zero second, then at 0.03 s, the STATCOM is started while the resistor circuit is shorted at 0.032 s. It is clear that the start-up of the STATCOM from the ac system side is very successful when the pre-insertion resistor is used and by controlling the value of the resistor we can control the charging current of the inverter.

4.2.2 Steady State Operation

Figure 4.4(a) shows the inverter voltage and current of the compensator at the fully inductive operating point during the steady state operation. As expected, 7-level staircase type of the inverter voltage is clearly shown when using the application of the fundamen-

tal frequency switching method. From the figure it can also be seen that the lagging reactive current. The result also shows that the current was very sinusoidal without filters or a high pulse number connection. Figure 4.4(c) show the Fourier analysis of the compensator current the analysis is done by using livewire software. The analysis tells us that the highest noticeable harmonic order is the 5th.

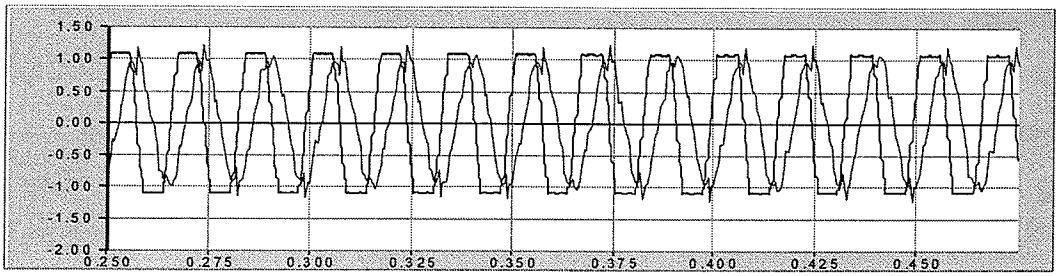


Fig 4.4(a):The Inverter Output Voltage and Current at the ac side

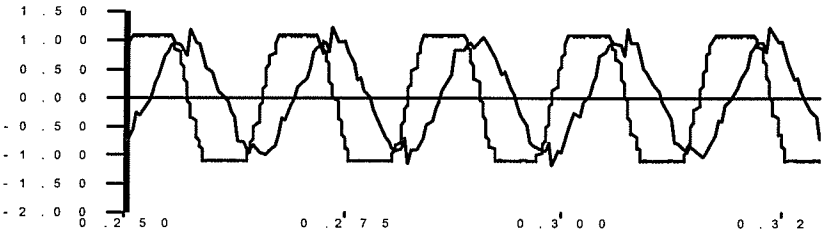


Fig 4.4(b) :Zoom out of Fig 4.4 (a).

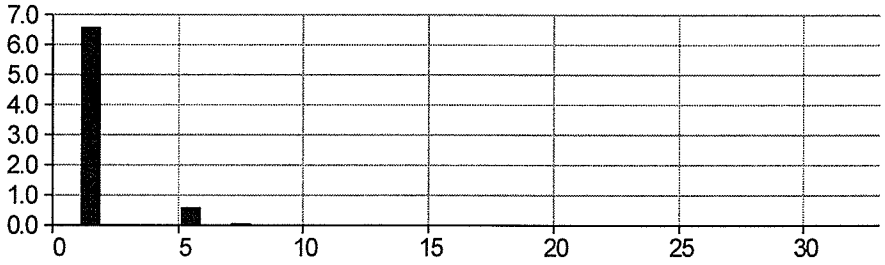


Figure 4.4(c): The Fourier Analysis of The Compensator Current

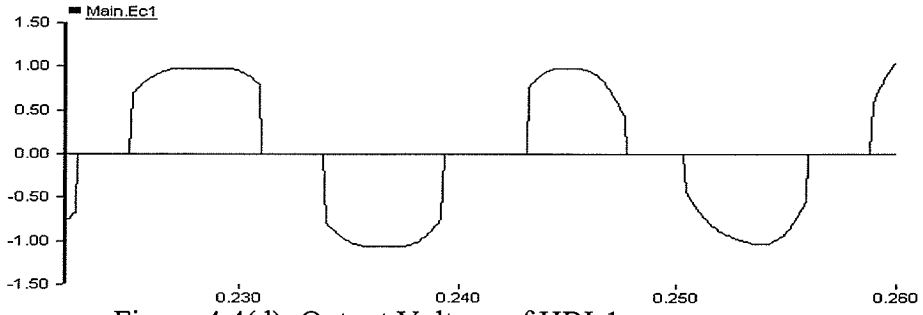


Figure 4.4(d): Output Voltage of HBI-1

The triplen harmonics can not flow through the three wire connection of the STATCOM to the system. Although the 5th, 7th, and 11th harmonics are eliminated by FFS method as mentioned in Chapter 3, the 5th, and the 7th, harmonics are reintroduced because of the switching angles used in the SHE scheme are predetermined from the switching function, assuming a constant capacitor voltage on the dc side. When the capacitor voltage contains ripple due to the current as shown in Figure 4.4(d), the actual ac side voltage of the STAT-COM will have a different wave shape than the ideal waveform used in the calculation of the switching angles.

4.2.3 Transient Operation

To illustrate the transient response of the compensator by using the FFS switching method, Figure 4.5(a) shows waveforms of the terminal voltage on the system side, V_a, and the compensator current, I_a, during the sudden change imposed by changing the line voltage as result of a sudden drop in the reference voltage. The figure shows that the reactive current of the compensator is quickly adjusted from the leading to the lagging state so that the load voltage is dropped to the new desired voltage as it is clear in Figure 4.5(c) which shows how fast compensator adjust the line voltage to the new value. The simulation results show that the phase locked loop and the simple proportional- integral controller can respond rapidly to any change in the line voltage as a result of changing the desired voltage level or change in the load as showlater in section 4.4.

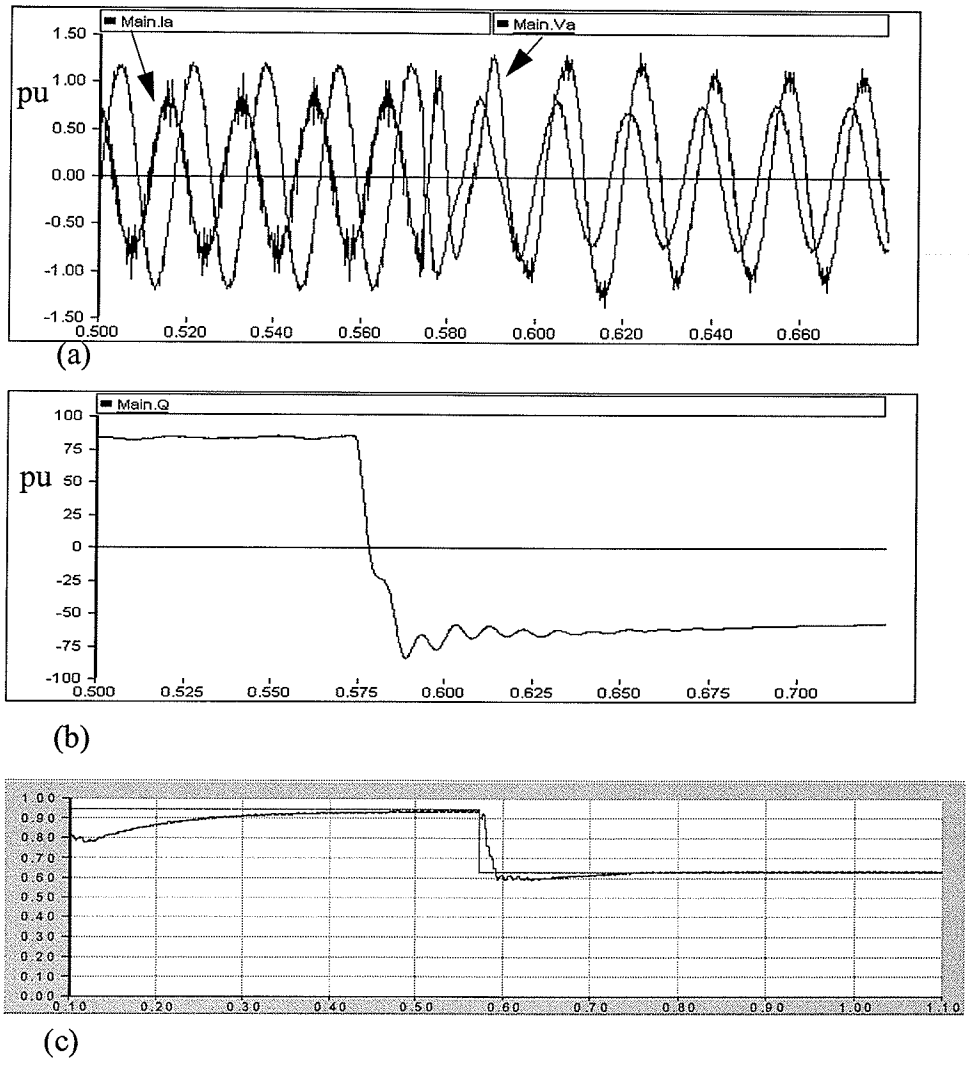


Figure 4.5: Transient Response of The M-STATCOM

4.2.4 Capacitors Voltage Balance

Figure 4.6 shows simulation of the dc capacitors voltage across HBI-1, HBI-2,

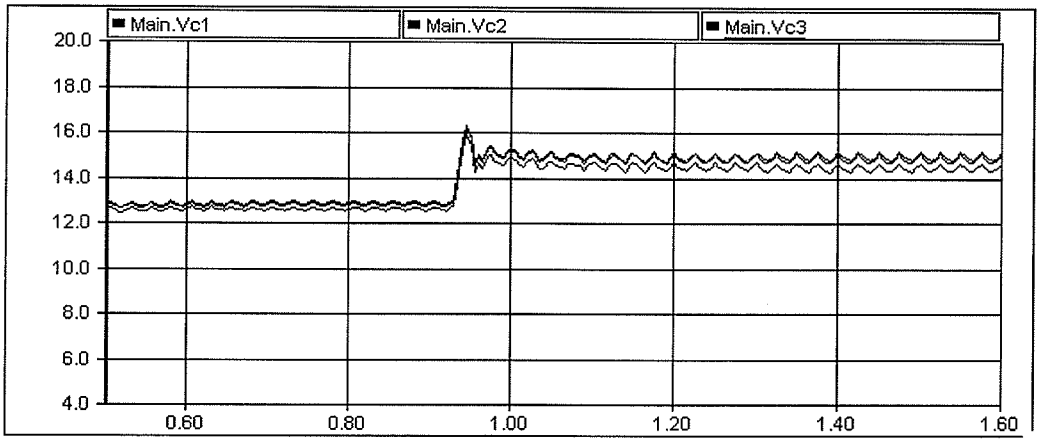


Figure 4.6: The Capacitive Voltage with Non-Rotated Switching Pattern

and HBI-3, in the non-rotated switching pattern. It is clear from the simulated result that in case of the non-rotated switching pattern control we have unbalanced dc voltages across the capacitors.

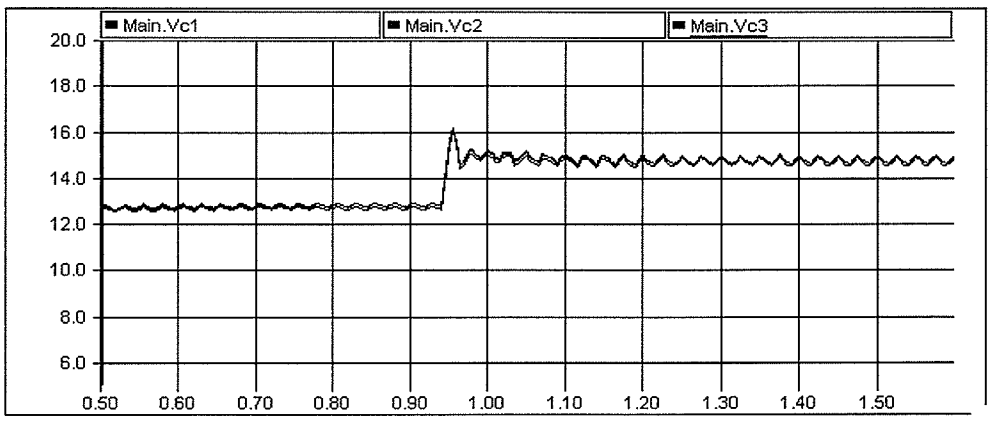


Figure 4.7: The Capacitive Voltage with Rotated Switching Pattern

On the other hand, at the same condition, Figure 4.7 shows the simulation results of the dc capacitor voltage across HBI-1, HBI-2, and HBI-3, in the rotated switching pattern. It is clear from the simulated result that in case of the rotated switching pattern control we have balanced dc voltage across the capacitors. The simulation result agrees with the theory that with the use of FFS with rotated switching pattern a balanced dc capacitors voltage can be achieved .

4.3 System Performance With PWM Switching Technique

The PWM switching technique is used to obtain the following simulation results. Figure 4.8 show the multi carrier PWM technique for F_c= 33, and modulation index (MI) = 1, also we can see that M-type carrier waveform is used where all the carriers above the zero reference are in phase, but in opposition with those below the zero reference.

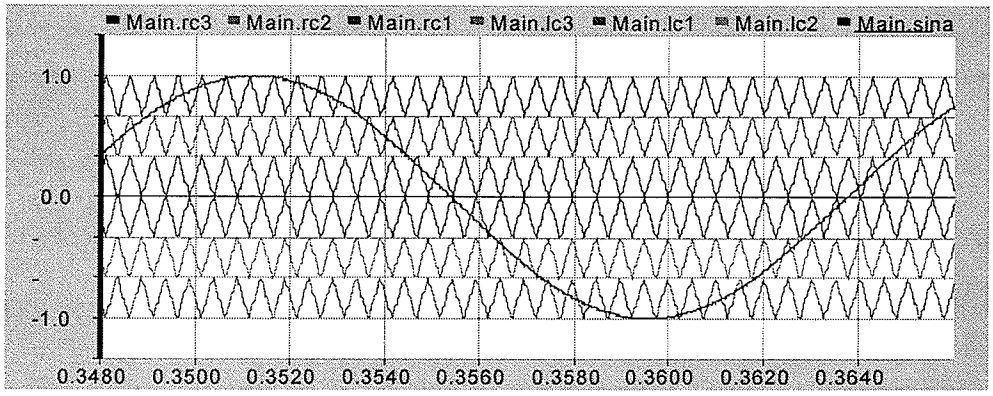
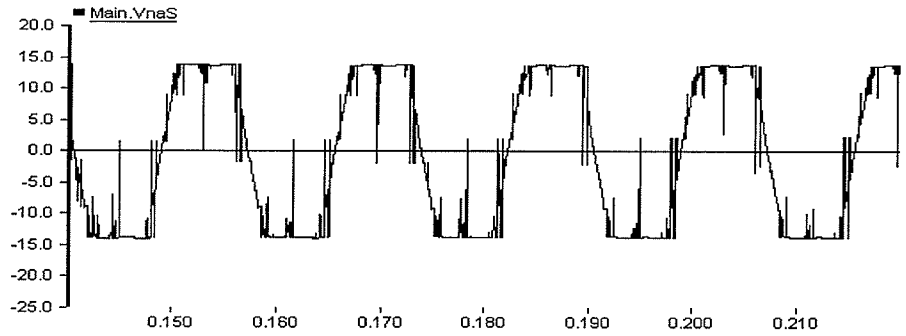


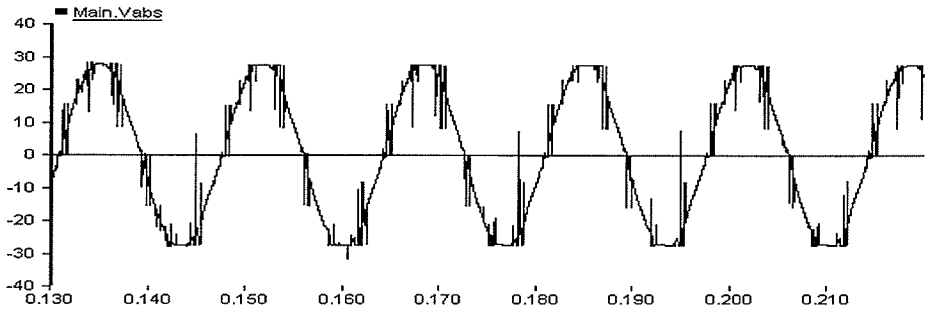
Figure 4.8: Multi-Carrier Waveform Technique

4.3.1 Steady State Operation

Figure 4.9(a) shows the inverter output line-neutral voltage, where Figure 4.9(b) shows the line to line inverter voltage. As expected, the high pulse number type of the inverter voltage is clearly seen because of the application of the PWM switching method. The Fourier analysis of the l-l inverter voltage tells us that the highest noticeable harmonics are the 5th, the 7th and then the 27th as shown in Figure 4.10.



(a)



(b)

Figure 4.9: Inverter Output Voltage When PWM is Applied. (a) Phase Voltage, and (b) Line Voltage

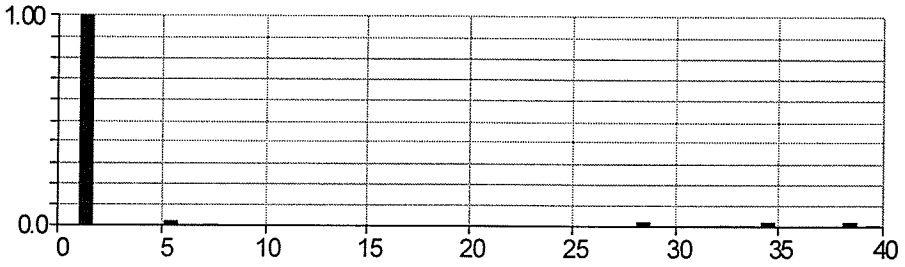


Figure 4.10: Line Voltage Spectrum.

4.4 Comparison between PWM and FFS Response During Dynamic Operation

Figure 4.11 and Figure 4.112 illustrate the dynamic response of the STATCOM to maintaine the desired line voltage (1 pu) during switching of the R/L load to the system as shown in Figure 4.13. The switch is turned on at t = 1.5 s for 0.75 s. By comparing simulation results of Figure 4.11 which represent the STATCOM response when the PWM switching technique is used, with Figure 4.12 which represents the STATCOM response when the FFS switching method is used we can see that both of them response to the step change of the reactive power demand, we can also see that the advantage of applying the FFS in improving the response speed.

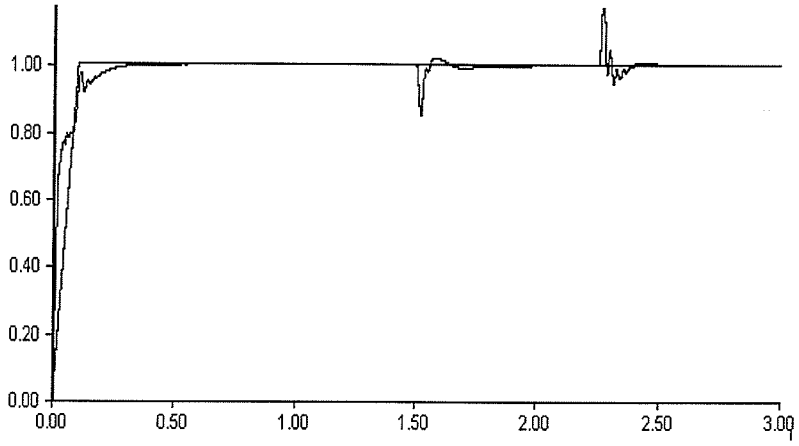


Figure 4.11: The Dynamic Response Of The STATCOM With PWM.

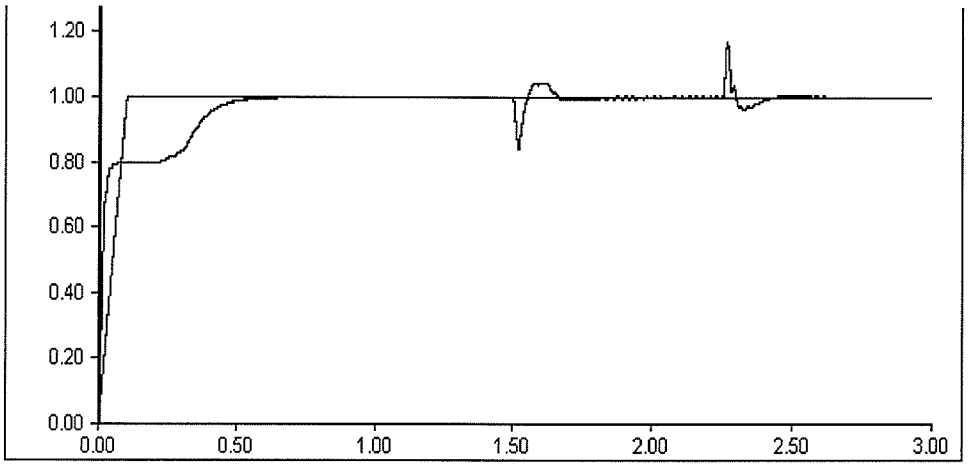


Figure 4.12: The Dynamic Response Of The STATCOM With FFS.

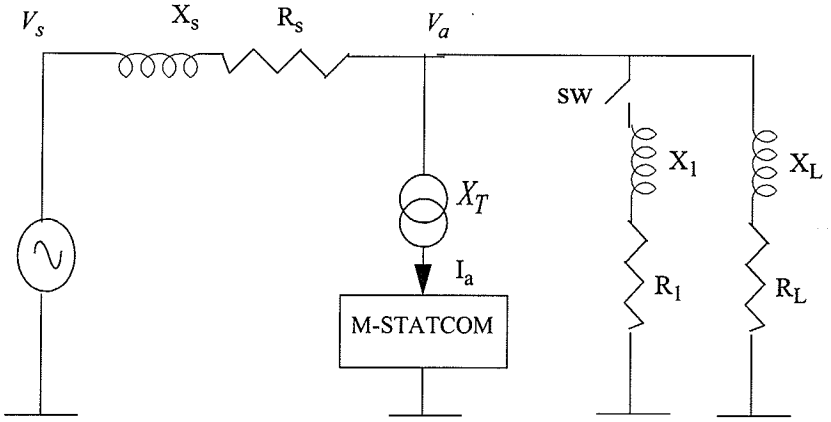


Figure 4.13: A Schematic Diagram of the Simulation Test System for Dynamic studies.

CHAPTER 5 Conclusions and Future Work

5.1 Conclusions

There are mainly three different circuit configurations for the multilevel thyristor inverter for STATCOM applications. The studies presented in this thesis especially revealed the aspect of the design, control and performance of the cascaded inverter type STATCOM, which has offered an interesting alternative to other circuit configurations being considered for the M-STATCOM.

The major conclusions are as follows:

1- The main advantage of the M-STATCOM is that the voltage level can be increased without series connection of GTO thyristors and the necessity of simultaneous switching, which means this type of design is more practical for power transmission systems as higher reactive power output can be achieved by increasing the number of levels of the inverter.

2- The studies show that the cascade type multilevel inverter has many dominant advantages:

a) The structure is based on conventional three level full bridge inverter units (H-bridge), so the topology is very simple.

b) Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.

3- To control the output voltage of the cascade multilevel inverter output, both the FFS method and PWM techniques were investigated. By analyzing the calculated result and the simulated result it can be concluded that FFS method has lower total harmonic distortion, reduced switching losses, and better dynamic response, which makes it the preferable method to control the output voltage of the cascade multilevel inverter.

4- In case of FFS method, a switching scheme of rotated fundamental pattern is successfully applied to control the dc voltage balancing. The selective harmonic elimination method is employed to reduce the low order harmonics in this switching scheme.

5- The simulation studies confirm that the cascaded multilevel inverter STATCOM can provide fast continuous variation of leading or lagging reactive power system, and is very effective as a dynamic compensator for supporting the system voltage.

6- In comparison with other methods to overcome the dc voltage unbalancing problem which use some physical devices to balance the dc voltage. The rotated switching scheme emerged as an practical alternative due to its cost efficient and easier implementation.

5.2 Recommendations For Future Work

For a true evaluation, the following points should be given consideration:

1- More work should be done in studying the system response to different types of PWM techniques with different control strategies.

2- The establishment and test of an experimental model of a Cascade type inverter STATCOM should be undertaken.

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APPENDIX A

Mathcad Programs for the Analysis of 7-Level Inverter

1. FFS Method

2. SH-PWM Technique

3. SFO-PWM Technique

4. PS-PWM Technique

FFS Method for 7-Level Inverter

$$deg := \frac{\pi}{180}$$

$wt := 0 .. 360$ $n := 1, 3 .. 100$

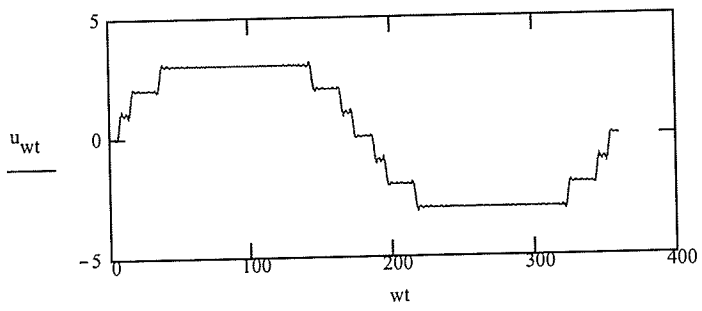
$\alpha 1 := 7.09$ $\alpha 2 := 15.68$ $\alpha 3 := 36.17$

$$ud1_{wt} := \frac{4}{\pi} \cdot \sum_n \frac{1}{n} \cdot \left(\cos\left(n \cdot \alpha 1 \cdot deg\right)\right) \cdot \sin(n \cdot wt \cdot deg)$$

$$ud2_{wt} := \frac{4}{\pi} \cdot \sum_n \frac{1}{n} \cdot \left(\cos\left(n \cdot \alpha 2 \cdot deg\right)\right) \cdot \sin(n \cdot wt \cdot deg)$$

$$ud3_{wt} := \frac{4}{\pi} \cdot \sum_n \frac{1}{n} \cdot \left(\cos\left(n \cdot \alpha 3 \cdot deg\right)\right) \cdot \sin(n \cdot wt \cdot deg)$$

$$u_{wt} := ud1_{wt} + ud2_{wt} + ud3_{wt}$$



Total Harmonic Distortion

$p := 5, 11 .. 50$ $q := 7, 13 .. 50$

$$THD1(p) := \left(\frac{1}{p}\cdot\cos(p\cdot\alpha1\cdot deg)\right) + \frac{1}{p}\cdot\cos(p\cdot\alpha2\cdot deg) + \frac{1}{p}\cdot\cos(p\cdot\alpha3\cdot deg)$$

$$THD2(q) := \left(\frac{1}{q}\cdot\cos(q\cdot\alpha1\cdot deg)\right) + \frac{1}{q}\cdot\cos(q\cdot\alpha2\cdot deg) + \frac{1}{q}\cdot\cos(q\cdot\alpha3\cdot deg)$$

$$THD := \frac{\sqrt{\sum_p (THD1(p))^2 + \sum_q (THD2(q))^2}}{\cos(\alpha1\cdot deg) + \cos(\alpha2\cdot deg) + \cos(\alpha3\cdot deg)}$$

$THD = 0.059$

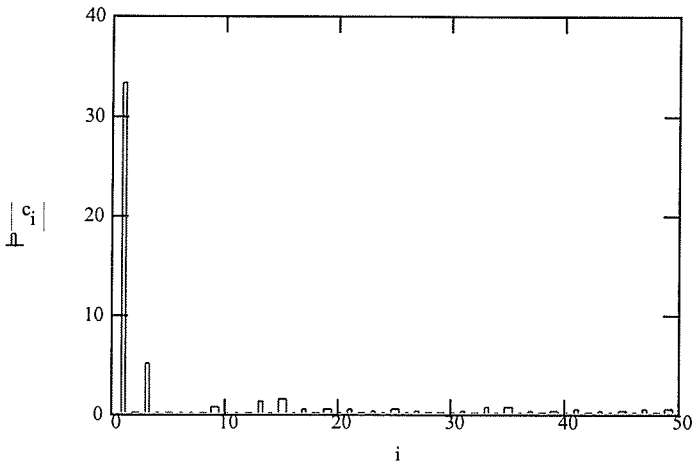
$i := 0 .. 50$

$$F(u) := \frac{2j}{\sqrt{512}}\cdot(fft(u) - 2j\cdot Im(fft(u)))$$

$$H1(p) := \frac{4}{\pi}\cdot|\,THD1(p)\,|$$

Harmonic Spectra

$c := cfft(u)$



SH-PWM Technique for 7-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 511$ $m := 1$ $k := 9$

$$c(t,k) := \frac{-1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

$c1(t,k) := 1.5 + c(k,t)$

$c5(t,k) := 2.5 + c(k,t)$

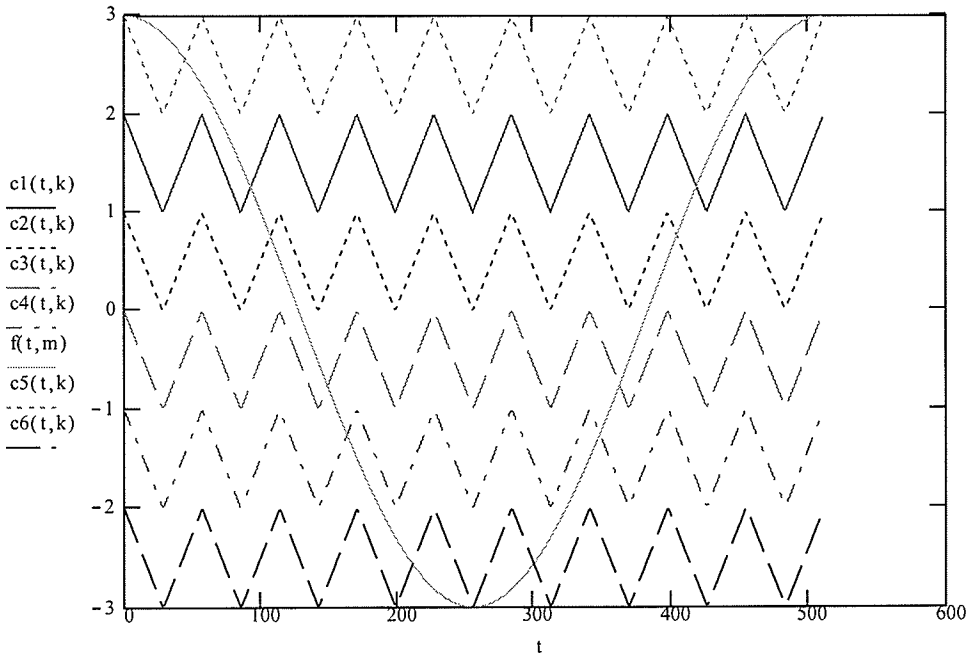
$c2(t,k) := .5 + c(k,t)$

$c3(t,k) := -0.5 + c(k,t)$

$c4(t,k) := -1.5 + c(k,t)$

$c6(t,k) := -2.5 + c(k,t)$

$f(t,m) := 3 \cdot m \cdot \cos(\omega \cdot t)$



$$u1(t,k,m) := -\left(\Phi(c1(t,k) - f(t,m)) - 1\right)$$

$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

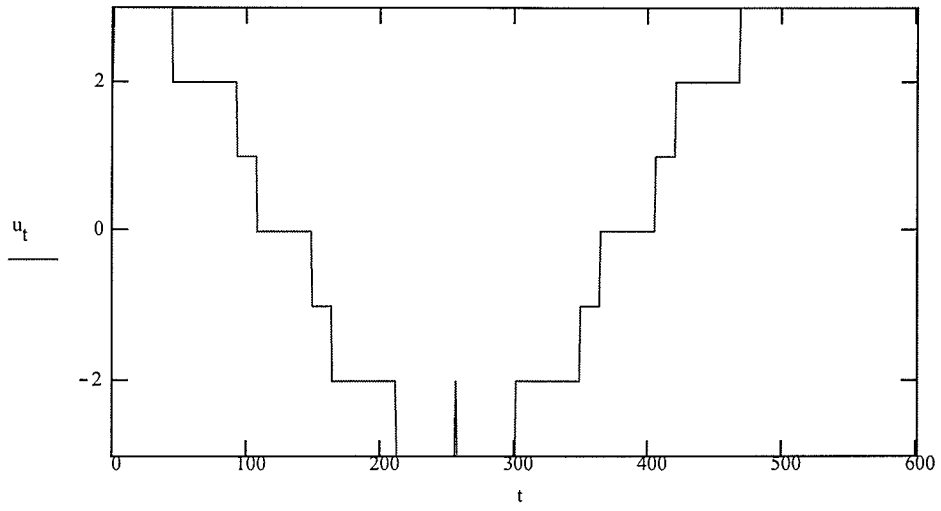
$$u5(t,k,m) := -\left(\Phi(c5(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \left(\Phi(f(t,m) - c4(t,k))\right) - 1$$

$$u6(t,k,m) := \left(\Phi(f(t,m) - c6(t,k))\right) -$$

$$u_t := ((((u1(t,k,m) + u2(t,k,m)) + u5(t,k,m)) + u6(t,k,m) + u4(t,k,m)) + u3(t,k,m))$$



Total Harmonic Distortion

$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (fft(u) - 2 \cdot i \cdot Im(fft(u)))$$

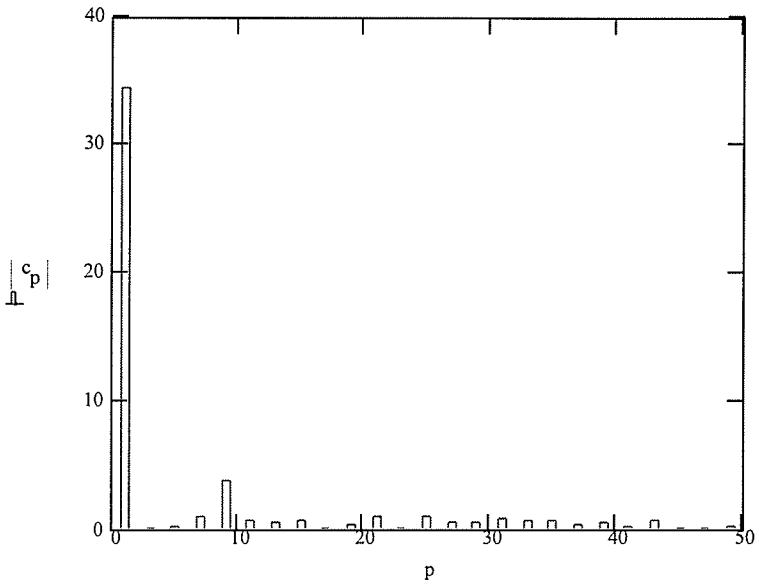
$j := 5, 11 .. 50$ $q := 7, 13 .. 50$

$$DF := \frac{\sqrt{\sum_j \left[\left(\left(\left| F(u)_j \right| \right) \right)^2 \right] + \sum_q \left[\left(\left| F(u)_q \right| \right)^2 \right]}}{\left| F(u)_1 \right|}$$

DF = 0.068

Harmonic Spectra

$c := cfft(u)$



SFO-PWM Technique for 7-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 511$ $m := 1$ $k := 9$ $\beta := 2 \cdot \frac{\pi}{3}$

$$c(t,k) := \frac{1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

$$c1(t,k) := 1.5 + c(k,t)$$

$$c2(t,k) := .5 + c(k,t)$$

$$c3(t,k) := -0.5 + c(k,t)$$

$$c4(t,k) := -1.5 + c(k,t)$$

$$c5(t,k) := 2.5 + c(k,t)$$

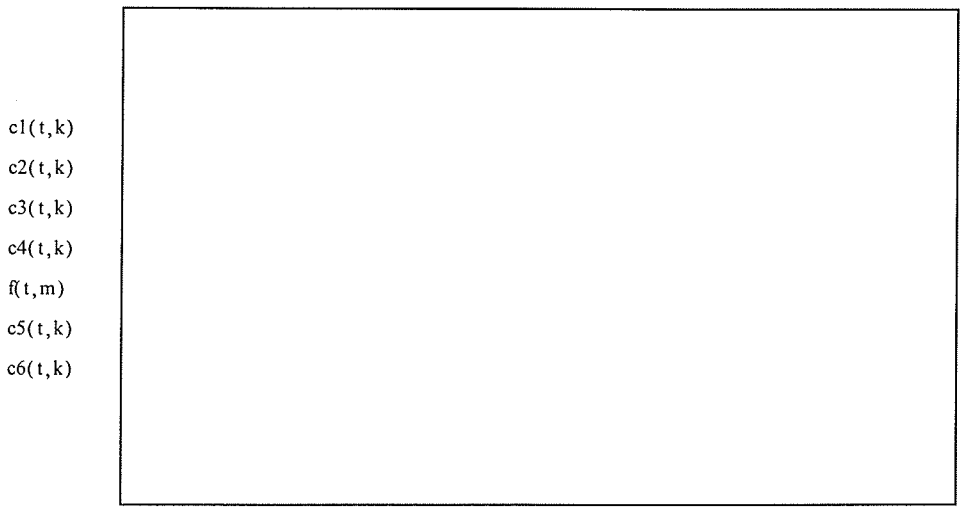
$$c6(t,k) := -2.5 + c(k,t)$$

$$f1(t,m) := 3 \cdot m \cdot \cos(\omega \cdot t)$$

$$f3(t,m) := \begin{bmatrix} 3 \cdot m \cdot \cos(\omega \cdot t) \\ 3 \cdot m \cdot \cos(\omega \cdot t - \beta) \\ 3 \cdot m \cdot \cos(\omega \cdot t + \beta) \end{bmatrix}$$

$$f0(t,m) := \frac{\max(f3(t,m)) + \min(f3(t,m))}{2}$$

$$f(t,m) := f1(t,m) - f0(t,m)$$



$$u1(t,k,m) := -\left(\Phi(c1(t,k) - f(t,m)) - 1\right)$$

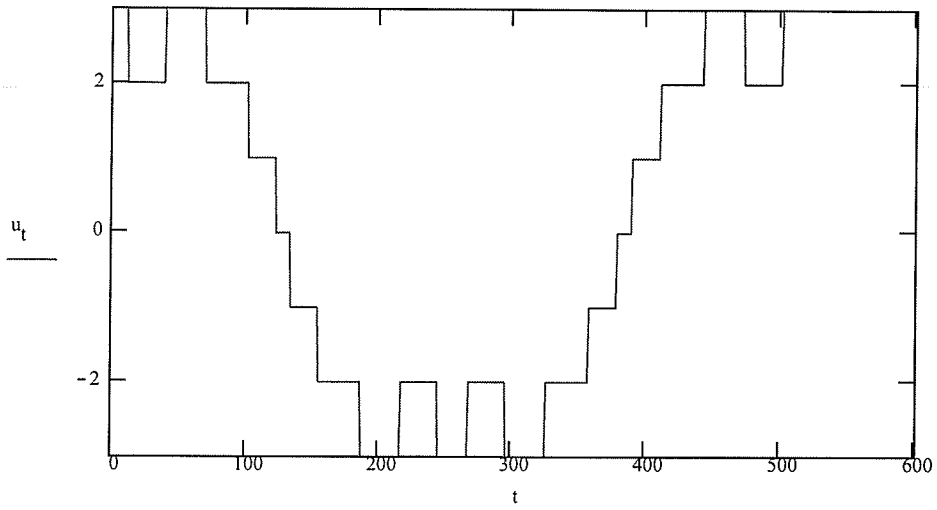
$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

$$u5(t,k,m) := -\left(\Phi(c5(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \left(\Phi(f(t,m) - c4(t,k))\right) - 1 \qquad u6(t,k,m) := \left(\Phi(f(t,m) - c6(t,k))\right) - 1$$

$$u_t := ((((u1(t,k,m) + u2(t,k,m)) + u5(t,k,m)) + u6(t,k,m) + u4(t,k,m)) + u3(t,k,m))$$



$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (fft(u) - 2 \cdot i \cdot Im(fft(u)))$$

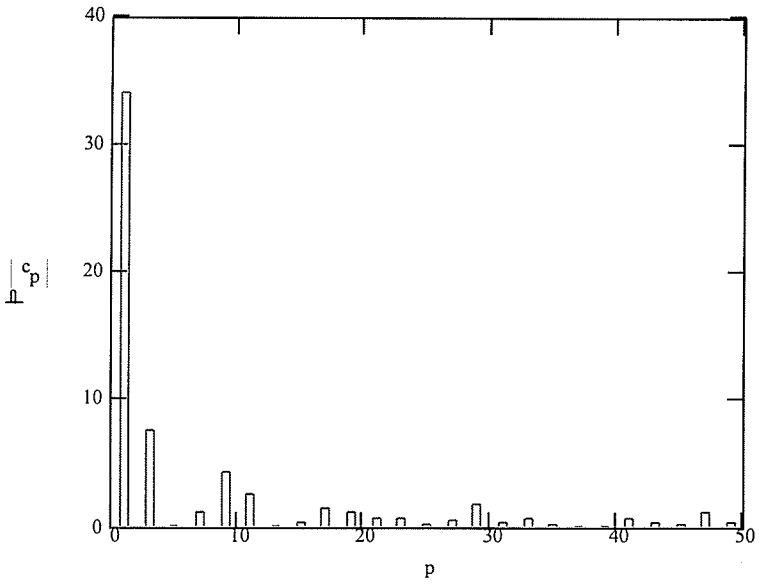
$j := 5, 11 .. 50$ $\qquad$ $q := 7, 13 .. 50$

$$DF := \frac{\sqrt{\sum_j \left[\left(\left| F(u)_j \right| \right)^2 \right] + \sum_q \left[\left| F(u)_q \right|^2 \right]}}{\left| F(u)_1 \right|}$$

$DF = 0.124$

Harmonic Spectra

$c := cfft(u)$



PS-PWM Technique for 5-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 1022$ $m := 1$ $k := 9$

$$c(t,k) := \frac{-1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

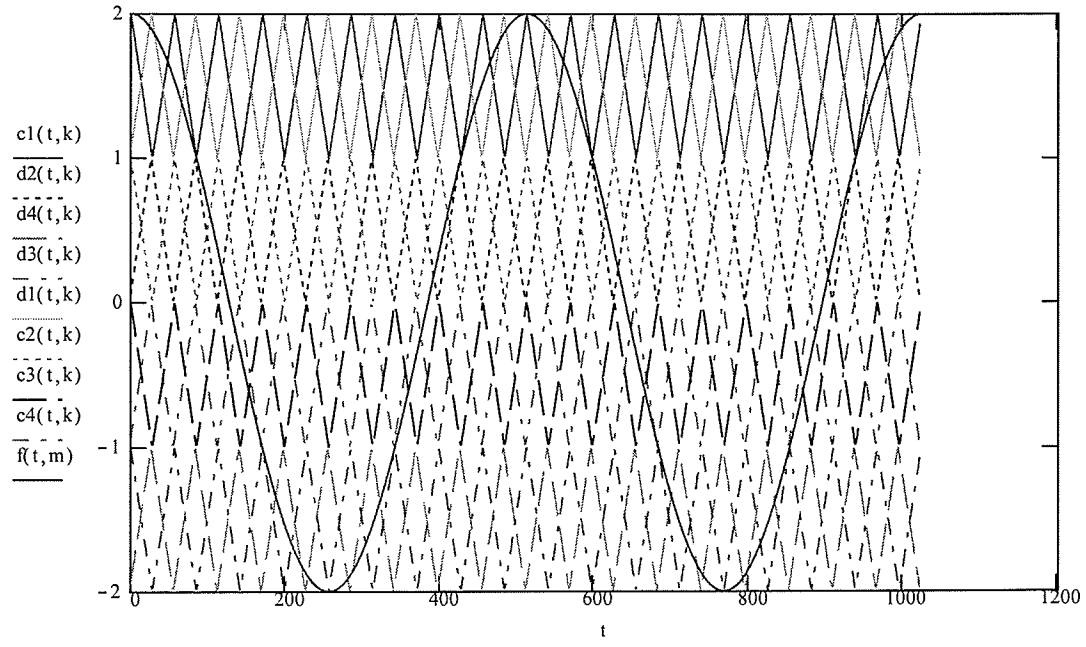
$c1(t,k) := 1.5 + c(k,t)$ $d1(t,k) := c1(k,(t+30))$

$c2(t,k) := .5 + c(k,t)$ $d2(t,k) := c2(k,(t+30))$

$f(t,m) := 2 \cdot m \cdot \cos(\omega \cdot t)$

$c3(t,k) := -0.5 + c(k,t)$ $d3(t,k) := c3(k,(t+30))$

$c4(t,k) := -1.5 + c(k,t)$ $d4(t,k) := c4(k,(t+30))$



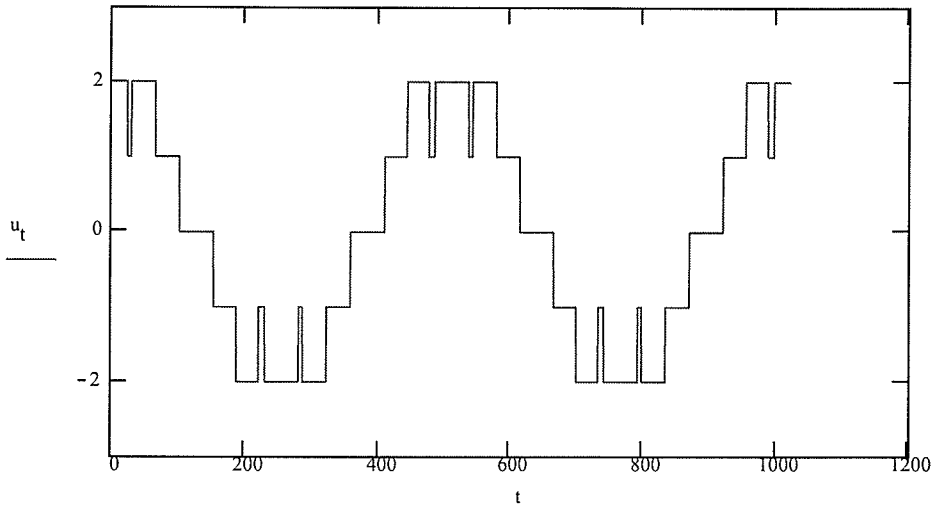
$$u1(t,k,m) := -\left(\Phi(d1(t,k) - f(t,m)) - 1\right) + 1$$

$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \Phi(f(t,m) - d4(t,k)) - 2$$

$$u_t := (u1(t,k,m) \cdot u2(t,k,m)) - u3(t,k,m) \cdot u4(t,k,m)$$

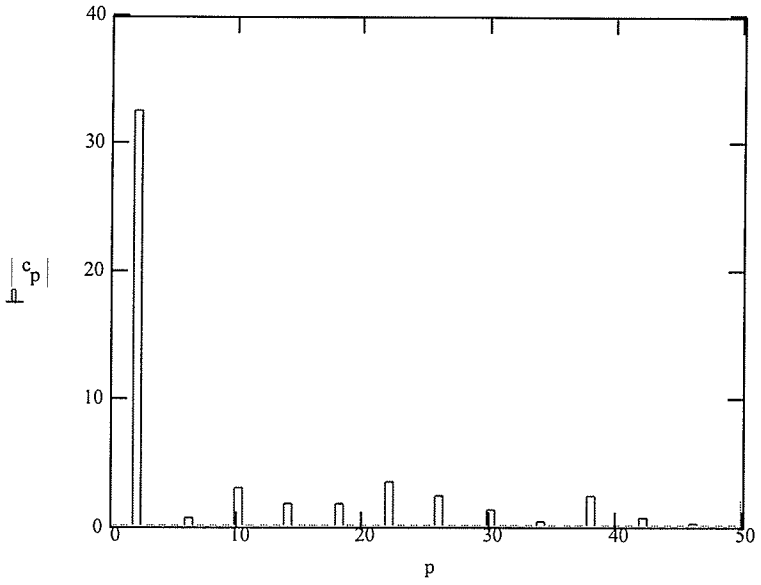


Harmonic Spectra

$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (\mathrm{fft}(u) - 2 \cdot i \cdot \mathrm{Im}(\mathrm{fft}(u)))$$

$c := \mathrm{cfft}(u)$



APPENDIX B

The Parameters of the Test System

$V = 1.000$ pu.

$V_s = 1.100$ pu.

$X_s = 0.060$ pu.

$X_T = 0.200$ pu.

$R_L = 0.251$ pu.

$R_1 = 0.15$ pu.

$X_L = 0.092$ pu.

$X_1 = 0.067$ pu.

The Parameters of Controls

PI Regulator	**Proportional Gain**	**Integral Gain**
Phase Locked Loop	50	2000.0
Ac Terminal Voltage Control	2.0	0.01
Reactive Power Output Control	1.8	0.01