DSP-Based Control Strategies for An Inverter-Based Compensator

by

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A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree of MASTER OF SCIENCE

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Abstract

The focus of this thesis is on the study and experimental implementation of a voltage source inverter-based reactive power compensator. A general mathematical model of the system has been developed, from which a approximate linearized model is derived. The approximate model introduces a simple means of characterizing the fundamental frequency behaviour of the compensator. This permits the characterization of the stationary and dynamic behaviour of the compensator in terms of the system parameters and the switching scheme used. The experimental results have verified that this approximate model represents very well the fundamental frequency behaviour of the system over the operating range of interest.

Feedforward and feedback control on the dc bus voltage are also investigated. Piecewise linearization of the compensator's stationary response proved to be a good solution in overcoming the deviation from the desired values in feedforward control. Feedback control not only reduced the steady-state errors, but also improved the dynamic performance of the compensation system. It is demonstrated that the laboratory prototype behaves satisfactorily under stationary and dynamic conditions.

Furthermore, details of the system hardware and software are described. Theoretical and experimental results concerning the solvability of harmonic elimination schemes are also presented.

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List of Symbols

Some of the most frequently occurring abbreviators and symbols used in the thesis are tabulated below.

ac . . . . . alternating current
A/D . . . . . Analog to Digital
ADC . . . . . Analog-to-Digital Converter
ALU . . . . . Arithmetical Logic Unit
ARAU . . . . .Auxiliary Register Arithmetic Units
BSS . . . . . Basic Switching Scheme
dc . . . . . direct current
DSP . . . . . Digital Signal Processor
DMA . . . . . Dynamic Memory Access
FFT . . . . . Fast Fourier Transform
GTO . . . . . Gate-Turn-Off Thyristor
Hz . . . . . .hertz
IGBT . . . . . Insulated Gate Bipolar Transistor
I/O . . . . . Input and Output
KCL . . . . . Kirchhoff's Current Law
kVAr . . . . . kiloVAr
KVL . . . . . Kirchhoff's Voltage Law
l-l . . . . . line-to-line
l-n . . . . . line-to-neutral
MFLOPS . . . .Million FLOating-point instructions Per Second
MIPS . . . . . Million Instructions Per Second
PC . . . . . Personal Computer
PLL . . . . . Phase-Lock-Loop
PU . . . . . Per Unit

PWM . . . . . .Pulse-Width-Modulation

rms . . . . . root mean square

SC . . . . . Synchronous Condenser

SHE . . . . . .Selective Harmonic Elimination

STATCOM . . .STATic COMpensator

STATCON . . . STATic CONdenser

SVC . . . . . Static VAR Compensator

TCR . . . . . Thyristor-Controlled Reactor

TI . . . . . Texas Instruments

TSC . . . . . .Thyristor-Switched Capacitor

VSI . . . . . Voltage Source Inverter

Chapter 1.

Introduction

1.1 General

The main objective of this investigation is the implementation of a Voltage Source Inverter (VSI)-based reactive power compensator with satisfactory stationary and dynamic behaviour given the constraint that the power electronic inverter should have minimal complexity.

At low to medium power levels such simple methods are desirable to limit complexity and cost of the compensator. Dynamic response at these power levels is also of great concern. In addition, in spite of the low power level of the prototype compensator, the inverter should switch at minimal frequency in order to reduce system complexity. Furthermore, by constraining the switching frequency we do not preclude the application of the methods developed in this investigation to compensators of higher power ratings employing power electronic components that are limited in the rate at which they can be switched on and off.

Conventional compensation technologies such as synchronous condensers, thyristor-controlled

inductor and thyristor-switched capacitor can not meet the requirements of fast dynamic response demanded by applications like voltage flicker control. Power switches like Gate-Turn-Off thyristors (GTOs) can only be switched at low frequencies (typically several hundred hertz) [1], which implies that only a few switching actions may take place within each fundamental period at a working frequency of 60 Hz. Although we are using Insulated Gate Bipolar Transistors (IGBTs), we do not want to preclude the use of GTOs which are available at much higher current/voltage ratings but limited in switching frequency. That is why we constrain the switching frequency.

The focus of this thesis is on the study and experimental implementation of an inverter-based reactive power compensator switching and control strategies. A general mathematical model of the system is developed to reflect the behaviour of the system under stationary and dynamic conditions. Furthermore, a linearized modelling approach is derived from the general model. It will be shown that the simplified model represents very well the fundamental frequency behaviour of the system over the operating range of interest.

The control strategies for various switching schemes are discussed and implemented on the laboratory prototype. Experimental results demonstrate the stationary performance of each switching scheme at different operation modes.

Feedforward and feedback control on the dc voltage are also studied. The piecewise linearization is shown to be a good solution in overcoming the deviation from the desired values. The feedback control implemented not only reduces the steady-state errors, but also improves the dynamic performance of the compensation system. The optimized gain is achieved through root locus analysis and in turn is compared with experimental results.

The critical timing requirements associated with the switching schemes necessitate a high per-

formance microprocessor. The TMS320C30 Digital Signal Processor (DSP) is therefore employed as the controller of the prototype.

1.2 The Need For Dynamic Reactive Power Compensation

Applications like voltage flicker compensation due to loads such as arc furnaces and single-phase railway traction demand fast dynamic response which cannot be met by conventional static VAR compensators (SVCs). Conventional SVCs which consist of thyristor-switched capacitors (TSC) and thyristor controlled reactors (TCR) (shown in Figure 1.1), suffer from large size and slow dynamic response.

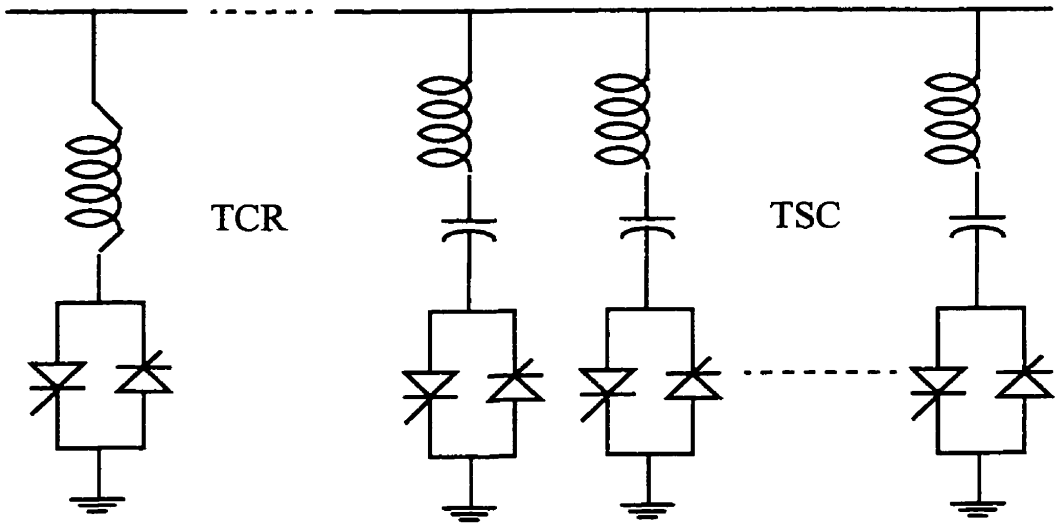


Figure 1.1 Conventional static var compensators

The inverter-based compensators consist of a three-phase voltage-source inverter (VSI) and a coupling inductor or transformer to connect it to the distribution or sub-distribution level voltage

(shown in Figure 1.2). For this voltage type inverter, there is a dc capacitor across the inverter input and a free-wheeling diode connected in anti-parallel with each GTO thyristor or IGBT valve. The advantages of the inverter-based compensator over the conventional compensators are as follows:

- The inverter-based compensator design is more compact and requires a small coupling reactance, or may just utilize the transformer's leakage reactance without requiring extra inductors.
- The inverter-based compensator offers fast and continuous variation of reactive output power.
- The inverter-based compensator offers superior performance over other reactive power control devices, in areas such as fault response time, voltage support ability and dc recovery, while operating with very weak ac systems [2].

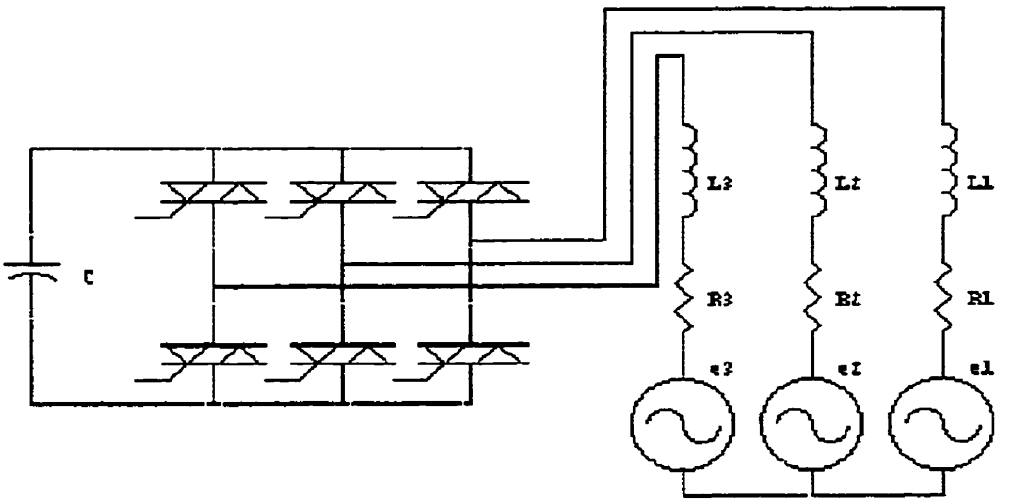


Figure1.2 Three-phase inverter-based compensator

1.3 Introduction to Selective Harmonic Elimination (SHE)

The inverter-based compensator is superior over the conventional compensators by virtue of not only its fast dynamic response, but also that SHE can selectively eliminate certain of the low-order harmonics, which are considered to be more harmful than high-order ones [3]-[6].

The objective of SHE is to eliminate a set of low-order harmonics by pushing the harmonic energy into high-frequency regions such that the low-frequency harmonics are well attenuated [7]. The advantage of applying this technique is that low-order harmonics are eliminated through the designed switching strategies, only high-order harmonics will appear at the output and need to be attenuated by the filter. The cut-off frequency of the filter can thus be increased, leading to a significant reduction of the filter size.

1.4 Control Strategies

The studies propose a new approximate linearized control modelling scheme to improve both the steady-state and transient responses of the compensation system. Piecewise linearization is applied in feedforward control to overcome the deviation from desired values. Feedback control can not only improve the transient response, but also reduce the steady-state errors [8]. The proposed control has been realized by using a single-chip digital signal processor. A ±3 -kVA SHE inverter has been constructed to verify the proposed control strategies. Simulation and experimental results show that the DSP-controlled compensator can achieve both good dynamic response and low harmonic distortion using appropriate control and switching strategies.

1.5 Outline of the Thesis

The objective of the thesis is to study and develop a VSI-based compensator, including device selection, switching valve construction, functional circuits design, DSP interface configuration and programming, control plant modelling and feedforward and feedback control implementation.

In Chapter 2, the working-principle of the inverter-based compensator is presented. Construction details of the three-phase IGBT-based inverter is introduced, including the main electrical parameters of the prototype compensator. In this chapter, Texas Instruments TMS320C30 digital signal processor is also introduced including the features of its architecture, various functional registers, memory maps, addressing, timer and serial-port configuration and expansion bus interface. The phase-locked-loop (PLL) which synchronizes the DSP to the network, and the two timers of the DSP that control the switching of the inverter are also considered. Functional circuits associated with data acquisition are presented. Issues associated with control implementations in both hardware and software conclude the chapter.

In Chapter 3, several switching schemes are investigated including Basic Switching Scheme (BSS) and Selective Harmonic Elimination (SHE). SHE includes 5th harmonic elimination (SHE-5) and 5th & 7th harmonics elimination (SHE-5-7). Two algorithms associated with 5th & 7th harmonic elimination are presented and compared. Implementation details for each switching scheme are also presented.

Chapter 4 develops a general mathematical model of the compensation system, for the sake of comprehending the dynamic behaviour of the system. This model is simplified by neglecting harmonic components. Two modelling approaches are discussed and compared. First, exact modelling which accounts for all harmonics and dc voltage ripple is presented, then an approximate modelling which only considers the fundamental components in voltage and current is presented.

In Chapter 5, a simple means of characterizing the fundamental frequency behaviour of the compensator is introduced. This approach permits the characterization of stationary and dynamic behaviour of the three-phase inverter-based compensator in terms of the system parameters, the switching scheme used and the input phase angle. The approximate approach formulates the equilibrium problem in terms of a fundamental frequency power balance.

In Chapter 6, the stationary performance of the prototype in different compensation modes with different switching schemes is compared. Feedforward control of the dc voltage is introduced, along with piecewise linearization to approximate the nonlinear relations of the phase angle and the dc voltage for various switching schemes. The experimental results of dynamic performance of the compensating system in both open-loop and closed-loop control are compared. Lastly, stability of the system is analysed and control parameters are optimized by root locus.

Chapter 7 concludes the thesis and future work is proposed.

Chapter 2

Inverter-Based Compensation

2.1 Overview

This chapter will introduce the basic mechanism of variable reactive power compensation as well as practical realization based on a three-phase, two-level voltage source inverter. A brief overview of the prototype inverter-based compensator is also presented. This includes the DSP configuration, IGBT gate driver circuits, PLL-based synchronization circuit, data acquisition as well as the software implementation of the switching and control strategies.

2.2 Working Principle of Three-Phase Inverter-Based Compensator

The inverter-based compensator is an electronic equivalent of the synchronous condenser (SC),

that is to say, the basic principle of the compensator is almost identical to that of SC. The synchronous condenser is an unloaded synchronous machine connected to the power system. Consider the equivalent circuit of the SC depicted in Figure 2.1, Assume that the machine is lossless (i.e. R = 0), then the load angle is zero and the induced voltage of the machine (denoted U_s) is in phase with system voltage (denoted U_n). From the equivalent circuit of SC, the phase current which flows into the SC is given as $I_s = \frac{U_n - U_s}{jX}$, where X is the reactance of synchronous condenser. U_s will vary linearly with the field current I_f, governed by the constant K_f, then the compensating current can be regulated by the field current $I_s = \frac{U_n - K_f I_f}{jX}$.

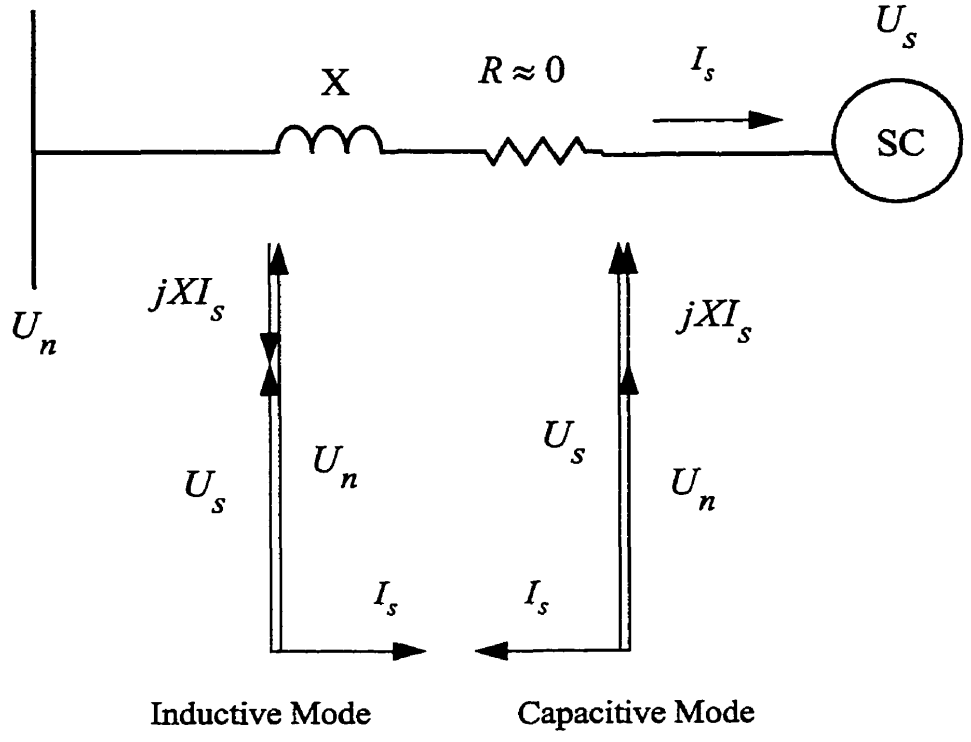


Figure 2.1 Equivalent circuit and vector diagram of synchronous condenser

When the system voltage U_n is too high, U_s is reduced by decreasing field current I_f, which leads to an inductive compensation current (lagging system voltage by 90 degrees) to lower system voltage. When the system voltage is too low, then U_s is increased by increasing I_f, which leads to a capacitive current (leading system voltage by 90 degrees) to support system voltage. When $U_n = U_s$, $I_s = 0$, there is no reactive power exchange between machine and system. In practice, there will always be a small in-phase current flowing into the machine to overcome the losses.

The inverter-based compensator is based on the same principle. Figure 2.2 shows a simplified equivalent circuit of the inverter-based compensator, whereby U_s represents the output voltage of the inverter; X is the inductive reactance between the inverter and the network, possibly the leakage reactance associated with the coupling transformer.

Similarly, we have the equation $I_s = \frac{U_n - U_s}{jX}$. When the inverter's output voltage is higher than the system, a capacitive current will flow into the compensator while an inductive current will flow into the compensator in the case of a lower inverter voltage.

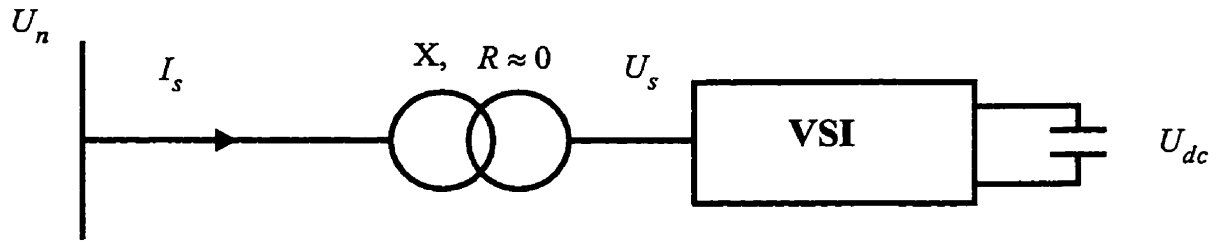


Figure 2.2 Equivalent circuit of VSI-based compensator

The voltage-source-inverter, a particular class of dc to ac power switching device, is presently considered an efficient and practical topology due to the availability of power electronic components suitable for its implementation. Like the synchronous condenser, the inverter voltage should be in phase with the system voltage. This can be controlled by a phase-locked-loop synchronization circuit, consequently, analogous to the SC, only reactive power is exchanged between the system and inverter. Under these conditions, there is no need for an external dc source of power for the inverter, and a capacitor across the dc bus is all that is required [9]. As mentioned before, the voltage difference between the inverter and the system determines the direction of reactive power flow. Thereby we may control the reactive power flow into or out of the system by controlling the magnitude of inverter ac-side voltage U_s.

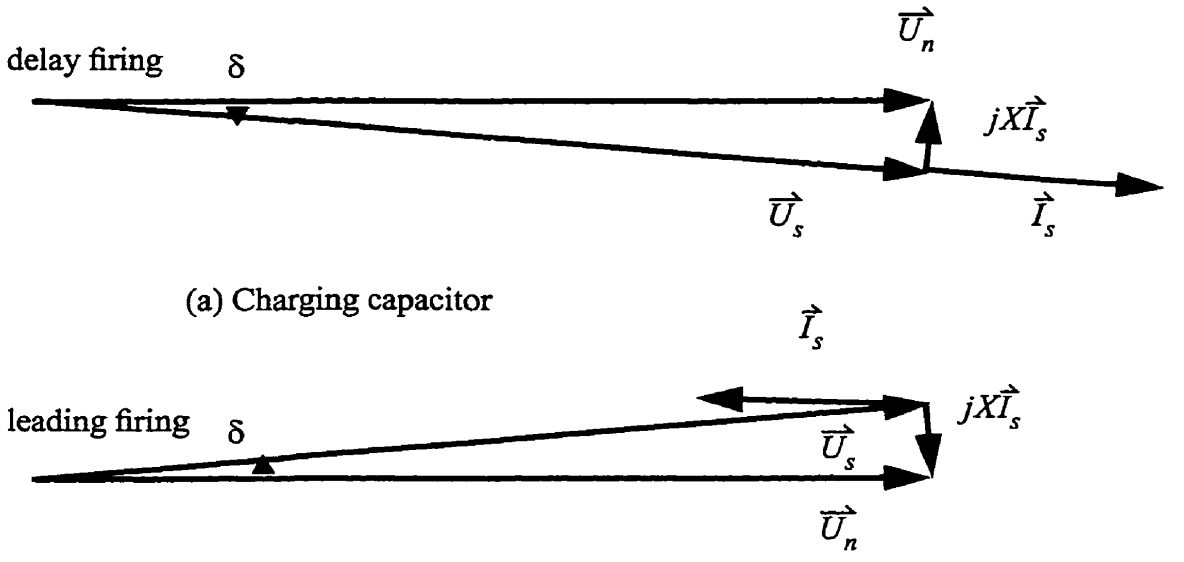


Figure 2.3 Vector diagram when charge / discharge capacitor of inverter

There are two alternatives available for controlling the magnitude of U_s:

1. Maintain a constant dc-link voltage and employ pulse-width-modulation (PWM) carrier-based techniques to control the fundamental voltage as well as limit some of the harmonics produced.

2. Produce a fixed switching pattern using fundamental frequency switching or SHE and control the magnitude of the ac voltage by controlling the dc voltage U_{dc}. As shown in Figure 2.3, a slight phase shift in the phase of U_s with respect to U_n will cause energy flow into or out of the dc bus, thereby charging or discharging the capacitor. SHE is a waveshaping technique used to eliminate or reduce certain harmonics by additional switching. The details of this technique, its implementation and experimental results are deferred to Chapter 3 and Chapter 6.

The current thinking is that the first control strategy employing PWM is necessary to obtain satisfactory harmonic and dynamic performance. However this precludes the use of high power rating switching devices such as GTOs due to limitations in switching frequency [9]. This work will concentrate on the second option of the above control strategies which due to the lower switching frequency involved do not preclude the use of devices like the GTOs.

The voltage-current characteristic of the VSI-based compensator in comparison with that of conventional SVCs is shown in Figure 2.4. The operation principle of VSI based compensator determines that they can maintain maximum compensation current under both over-voltage and under-voltage conditions as long as the difference between the system and the inverter voltage is kept constant. The current is limited only by the device ratings. This ability to compensate the system is much better than that obtained with a conventional SVC where the compensation cur-

rent falls proportionally with the drop of the system voltage. This is precisely when the compensation current is needed most.

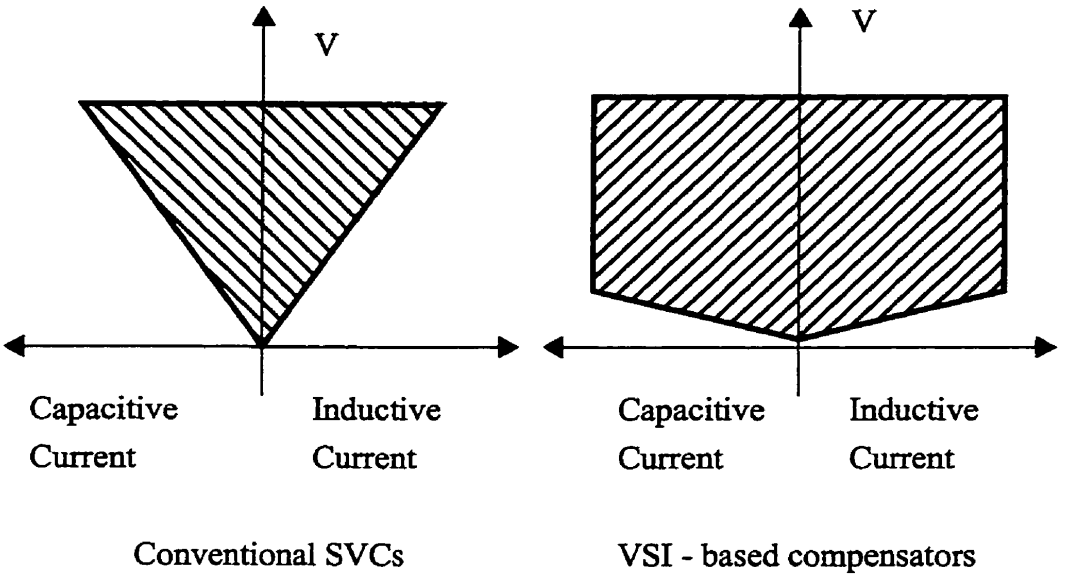


Figure 2.4 Comparison of voltage-current characteristic between conventional SVCs and VSI -based compensators

2.3 Overview of The Hardware System

2.3.1 Construction and Main Parameters

The inverter-based compensator is constructed with a three-phase voltage-source-inverter which is made of three dual IGBT modules (half-bridge configuration), a dc-link capacitor, three single-phase reactors coupling each half-bridge of the inverter to the network, and two busbars

connecting the inverter dc side with the capacitor. The capacitor provides sufficient energy storage to stabilize the dc link voltage for supplying the inverter. Furthermore, as the dc link capacitor feeds the inverter through busbars of minimal inductance, it also serves as a snubber, thereby reducing number of components in the system. The IGBT modules are mounted on aluminium heatsinks for thermal management. A fan for forced-air cooling can also be readily mounted on the inverter heat-sinker depending on the devices' load. The ratings of components of the prototype are as follows:

- IGBTs: 50 A, 600 V (POWREX CM50DY - 12E)
- Capacitor: 2400 μF, 450 V
- Reactor: 3.5 mH, 50 A rms
- Quality factor (ratio of inductance to resistance) of the inductors: 5.6 (based on basic switching scheme).

2.3.2 DSP Controlled System

Referring to Figure 2.5, the operating principle of the prototype is as follows: The host computer is a Powerland 486 PC, which is used to edit and compile C and/or Assembly codes, and serves as a man-machine interface as well. The TMS320C30 is synchronized with the network, reads once in each sampling period the feedback dc voltage, and then outputs a sequence of switching pulses to the gate drive circuit of the inverter (Refer to Appendix A for details).

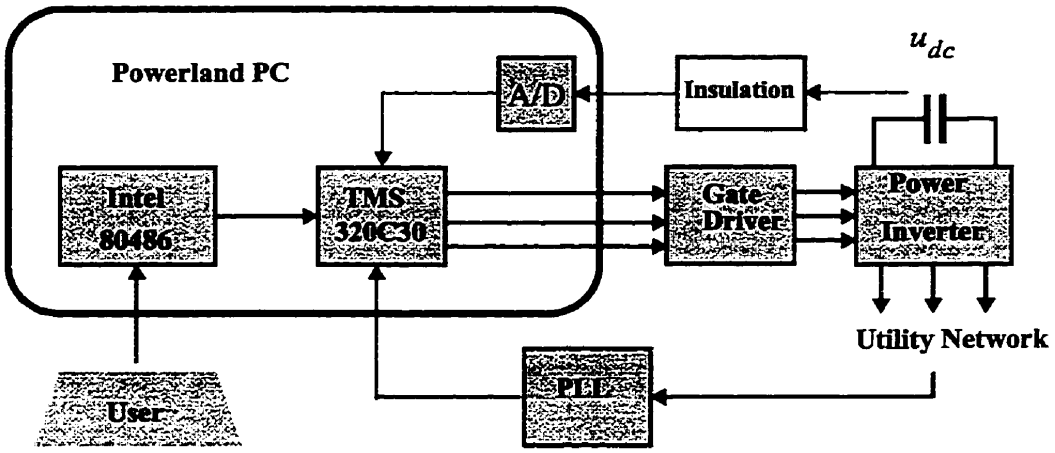


Figure 2.5 Hardware set up of DSP controlled inverter

2.3.3 The TMS320C30

In a DSP-based control system, the control algorithm is implemented in software. No component aging or temperature drift is associated with digital control systems. Additionally, sophisticated algorithms can be implemented and easily modified to upgrade system performance.

The Texas Instruments (TI)'s TMS320C30 DSP facilitates the development of high-speed digital control for power electronic applications. Dynamic requirements demand that compensators should response very fast, thus the controller must compute and analyse various signals acquired from the compensator and the system and respond very quickly.

The TMS320C30 digital signal processor is a high-performance CMOS 32-bit floating-point

device in the TMS320 family of single-chip digital signal processors. The processor operates with a 33 MHz clock speed (33.3 MFLOPS, 16.7 MIPS) in a single cycle.

Power electronic applications are greatly enhanced by the large address space, the two serial ports, the two-timers, and the multiple interrupt structure. More details regarding the TMS320C30 DSP are presented in Appendix A.

2.4 Control Implementations

The TMS320C30 has two general-purpose, 32-bit timer modules. The Timer 0 is used to time the interval between IGBT gating signals associated with the various of switching strategies. The Timer 1 is used time data acquisition. The global-control register for both timers are configured as internal clock mode. The count-down timers generate an interrupt at zero count.

The two serial ports of DSP are identical and independent with a complementary set of control registers for each one. Serial Port 0 is employed to control the lower switches of the three-phase inverter, while Serial Port 1 controls the upper switches. The serial ports are configured as general-purpose outputs.

Two external hardware interrupts and two timer internal interrupts are used in the control implementation. One external interrupt $\overline{INT0}$ is generated by the phase-locked-loop which synchronize the control algorithm to the network voltage. The other $\overline{INT1}$ is generated by the A/D converter to signal that a conversion is complete. The two internal interrupts TINT0 and TINT1 are associated with Timer 0 and Timer 1 respectively.

The control implementation is programmed to guarantee a switching dead-time, which is a small interval of alternative switching between upper and lower switches of each leg in IGBT module, to ensure that both switches in the same leg of the inverter does not conduct at the same time, thereby only after one switch switches off, can the other one in the same leg switches on. The dead-time is a configurable parameter set to 10 μs in the implementation. Furthermore, the software developed can meet the control requirements of the compensator while eliminating some selected harmonics. The program associated with the real-time control is coded in a mixture of C and Assembly language. The flow-chart of the control program is depicted in Figure 2.6.

In addition, the software provides certain protection to associated with dc over-voltage and mis-setting of input parameters.

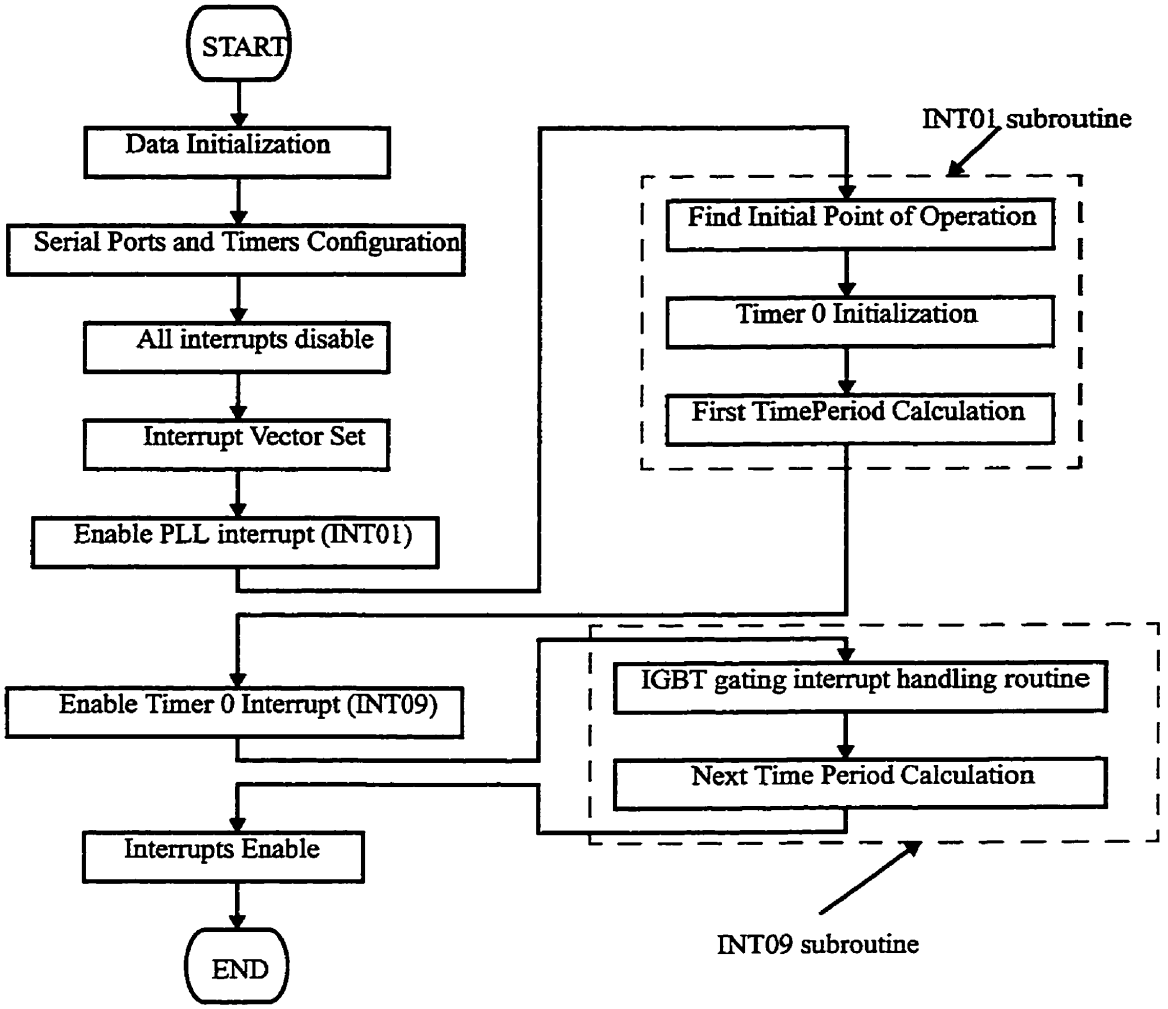


Figure 2.6 Flowchart of DSP control routine (Open-loop)

Chapter 3

Inverter Switching Strategies

3.1 Overview

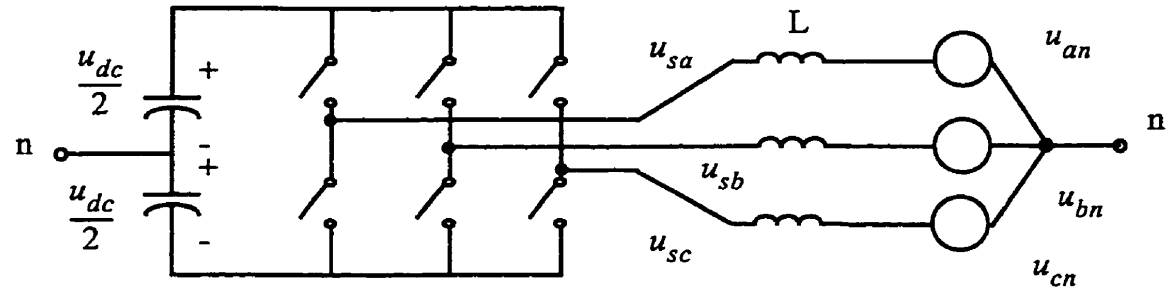
This chapter begins with the most basic switching strategy for synthesizing an ac voltage from a dc voltage. It will be shown that although the magnitude of the synthesized ac voltage is determined by the dc voltage, the switching scheme permits regulation of the phase of the ac voltage.

In addition, means of improving the harmonic profile of the synthesized ac voltage waveform by Selective Harmonics Elimination (SHE) are presented. The trade-off between dc voltage utilization and harmonic performance will be highlighted.

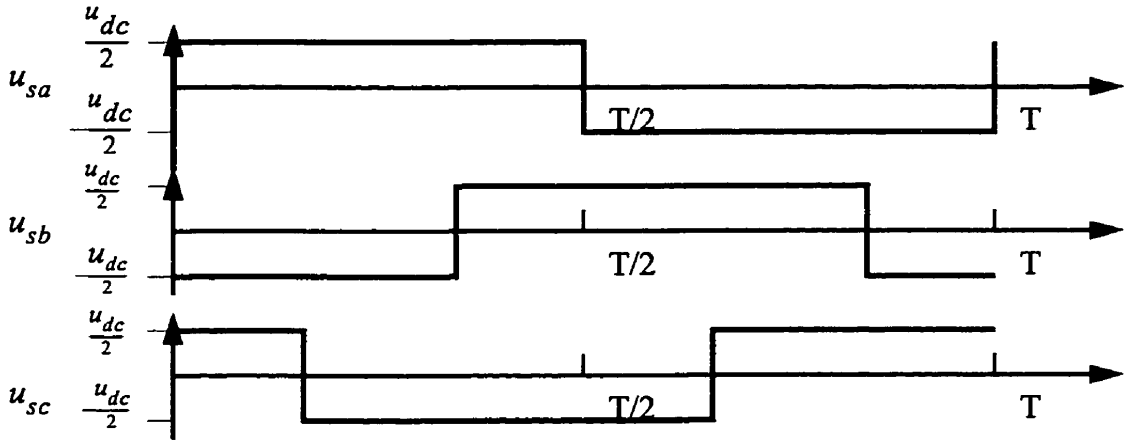
3.2 Basic Switching Scheme

The three-phase inverter circuit depicted in Figure 3.1 (a) is used to illustrate the operating prin-

ciple of the Basic Switching Scheme. The power electronic switches are represented by their functional equivalent. A fictitious neutral point is introduced to facilitate describing system operation. The operation of the inverter is described in terms of the line-to-neutral voltages where the



(a) Three phase inverter coupled to network with fictitious neutral



state	1	2	3	4	5	6
a	+	+	+	-	-	-
b	-	-	+	+	+	-
c	+	-	-	-	+	+

Note: ⬭ shows that states changed

(b) Waveforms and switch states associated with BSS

Figure 3.1 Inverter waveforms associated with BSS

neutral represents a fictitious mid-point of capacitor. The resulting two-level waveforms associated with BSS are depicted in Figure 3.1(b). Note that these waveforms cannot be measured directly in the real circuit, however they are directly related to the gating signals that are used to drive each leg of the inverter.

The table in Figure 3.1(b) represents the six switch states of the inverter as it progresses through one cycle of operation.

An inverter leg is marked in the '+' state when the upper switch is on and the lower one is off, while the '-' state indicates that the lower switch is on and upper one is off. For example, the '+-+' state describes the mode in which the upper switches of phase a and c, and the lower switch of phase b are on, while the other switches are off.

Under balanced conditions, it is sufficient to consider a single-phase of the inverter. The synthesized inverter ac voltage u_{sa}, its fundamental component $\langle u_{sa} \rangle_1$, and the network voltage u_{an} (all associated with phase a) are shown in Figure 3.2. The angle δ represents the phase difference between the network voltage and the inverter voltage. This permits control of the power flowing into or out of the compensator. When $\delta = 0$, the voltages of network and compensator are in phase, hence no energy is exchanged between them; When $\delta > 0$, the inverter voltage lags the network voltage, and energy flows into the compensator. Consequently the dc capacitor will be charged, and the dc voltage will rise. Similarly when $\delta < 0$, the inverter voltage leads the network voltage, resulting in energy flow out of the compensator and consequently the dc capacitor is discharged and dc voltage drops; Assume that the reference network voltage is

$$u_{an} = U_{an} \sin(\omega t)$$

Then with respect to the above, the fundamental component of the inverter ac voltage is given by

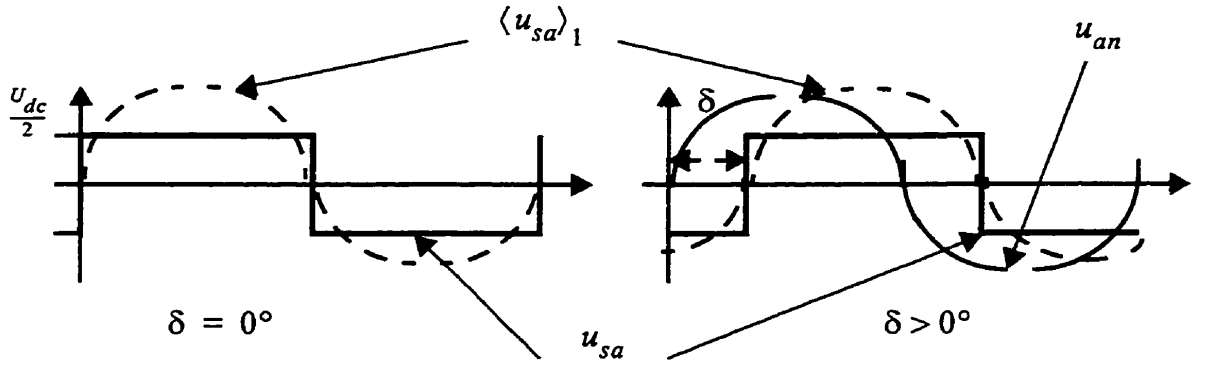


Figure 3.2 Fundamental component of ac voltage of inverter

$$\langle u_{sa} \rangle_1 = \frac{4}{\pi}\frac{U_{dc}}{2}\sin(\omega t - \delta) \tag{3.2.1}$$

for the BSS. Experimental results associated with capacitive and inductive modes will be compared and analysed in Chapter 6.

Besides the fundamental component, the ac voltage of the inverter contains 5th, 7th and higher-order harmonics. For balance, three-phase operation we need not consider triple-n harmonics. The magnitude of the n-th harmonic is given by

$$\left\| \langle u_{sa} \rangle_n \right\| = \frac{2U_{dc}}{n\pi} \tag{3.2.2}$$

for BSS.

The magnitude of the inverter voltage harmonics are inversely proportional to the order of the harmonic component. Therefore, we will focus on switching schemes aimed at eliminating the lower order harmonics.

3.3 Selective Harmonic Elimination

The principle drawback of BSS is the harmonic content of the resulting inverter voltage waveform. SHE offers the prospect of reducing the harmonic content while maintaining the functionality of BSS. SHE is attractive because of ease of implementation and relatively low switching frequency in comparison with pulse width modulation (PWM) techniques. Several schemes are investigated in this chapter, including 5th harmonic elimination (denoted SHE-5), and 5th and 7th harmonics elimination simultaneously (denoted SHE-5-7). Two algorithms (denoted SHE-5-7A and SHE-5-7B) associated with SHE-5-7 will be described and compared.

3.3.1 SHE-5

An important potential benefit of controlling the firing instants of the inverter switches is that the amplitude of certain harmonics may be controlled. In order to control the amplitude of the 5th harmonic, two notches at both ends of the former square wave are introduced as illustrated in Figure 3.3. For notches of width of α, the 5th harmonic amplitude of u_{sa} is

$$\left\| \langle u_{sa} \rangle_5 \right\| = \frac{2U_{dc}}{5\pi}(2\cos 5\alpha - 1) \tag{3.3.1}$$

Therefore the 5th harmonic and all other harmonics of order 5n are eliminated if we control the switches so that $\left\| \langle u_{sa} \rangle_5 \right\| = \frac{2U_{dc}}{5\pi}(2\cos 5\alpha - 1) = 0$, then $\alpha = \frac{\pi}{3 \bullet 5} radians = 12°$. However, the magnitude of the fundamental component will also decrease to

$$\left\| \langle u_{sa} \rangle_1 \right\| = \frac{2U_{dc}}{\pi}(2\cos\alpha - 1) = \frac{4}{\pi}\frac{U_{dc}}{2}(2\cos 12° - 1) = 0.9563\left(\frac{4}{\pi}\frac{U_{dc}}{2}\right) \tag{3.3.2}$$

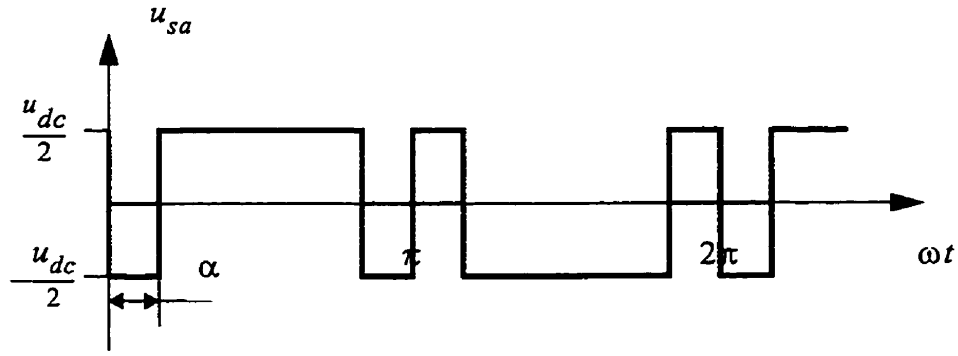


Figure 3.3 Switching scheme in elimination of 5th harmonic

The three phase switching strategy for 5th harmonic elimination is shown in Figure 3.4. There are eighteen switch states per cycle, which increases the complexity in comparison with BSS.

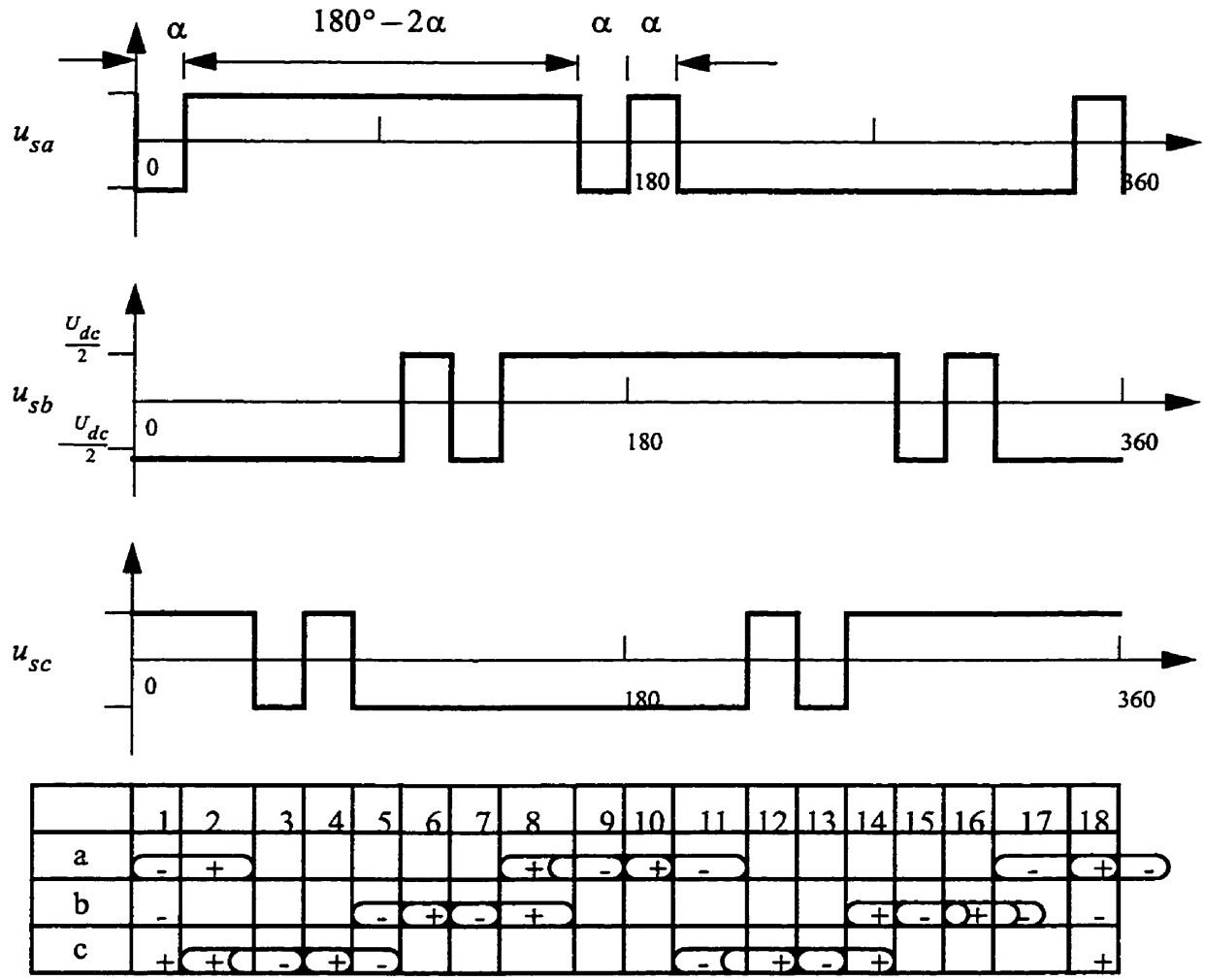


Figure 3.4 Three-phase switching scheme for 5th harmonic elimination

3.3.2 SHE-5-7

In this section, two algorithms for the simultaneous elimination of the 5th and 7th harmonics

will be introduced. The performance and implementation of both algorithms will be compared, and the superior one will be selected for further experiment which will be introduced in Chapter 6.

3.3.2.1 SHE-5-7A

Now we set out to eliminate 5th and 7th harmonics simultaneously. As mentioned above, the 5th harmonics can be eliminated by choosing of appropriate $\alpha = 12°$. In order to eliminate 7th harmonic while maintaining the cancellation of the 5th harmonic, additional notches of width 2β are needed and should be located at zero-crossing points of 5th harmonic waveform so as to cut equal amounts of positive and negative areas (Refer to Figure 3.5). Notches are placed symmetrically about $\phi = 36°$ and $144°$. Now we can eliminate 7th harmonic by controlling the width of notches. The magnitude of 7th harmonic is given by

$$\left\| \langle u_{sa} \rangle_7 \right\| = \frac{-2U_{dc}}{\pi} \int_0^{\frac{\pi}{15}} \sin(7\omega t)\, d\omega t + \frac{2U_{dc}}{\pi} \int_{\frac{\pi}{15}}^{\frac{\pi}{5}-\beta} \sin(7\omega t)\, d\omega t$$

which simplifies to

$$\left\| \langle u_{sa} \rangle_7 \right\| = \frac{2U_{dc}}{7\pi} \left(4\cos\frac{\pi}{10} \left(\sin 7\beta - \sin\frac{\pi}{15} \right) \right) \tag{3.3.3}$$

Therefore, to eliminate the 7th harmonic, we need set $\beta = \frac{\pi}{15 \bullet 7} radians$ so that Equation (3.3.3) equals to zero.

Eliminating the 5th and 7th harmonics comes at the expense of a smaller fundamental component. The magnitude of fundamental component decreases correspondingly to

$$\left\|\langle u_{sa}\rangle_1\right\| = \frac{2U_{dc}}{\pi}\left(-1+2\cos\frac{\pi}{15}-4\sin\frac{\pi}{5}\sin\beta\right) = 0.8860\left(\frac{4}{\pi}\frac{U_{dc}}{2}\right) \qquad (3.3.4)$$

Generally, we can extend this result to any chosen two harmonics to be eliminated by controlling the corresponding width and position of the notches. For instance, to eliminate the 11th and 13th harmonics, we can set $\alpha = \frac{\pi}{3 \bullet 11} radians$ and $\beta = \frac{\pi}{3 \bullet 11 \bullet 13} radians$, placing the two notches symmetrically about $\frac{\pi}{11}$ and $\pi - \frac{\pi}{11}$.

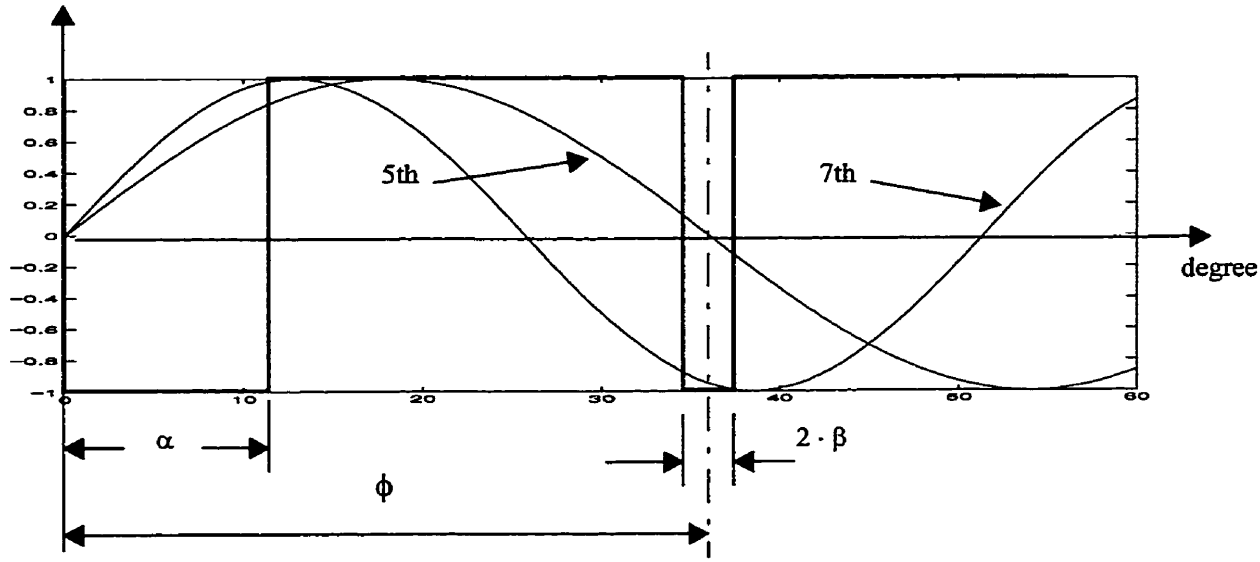
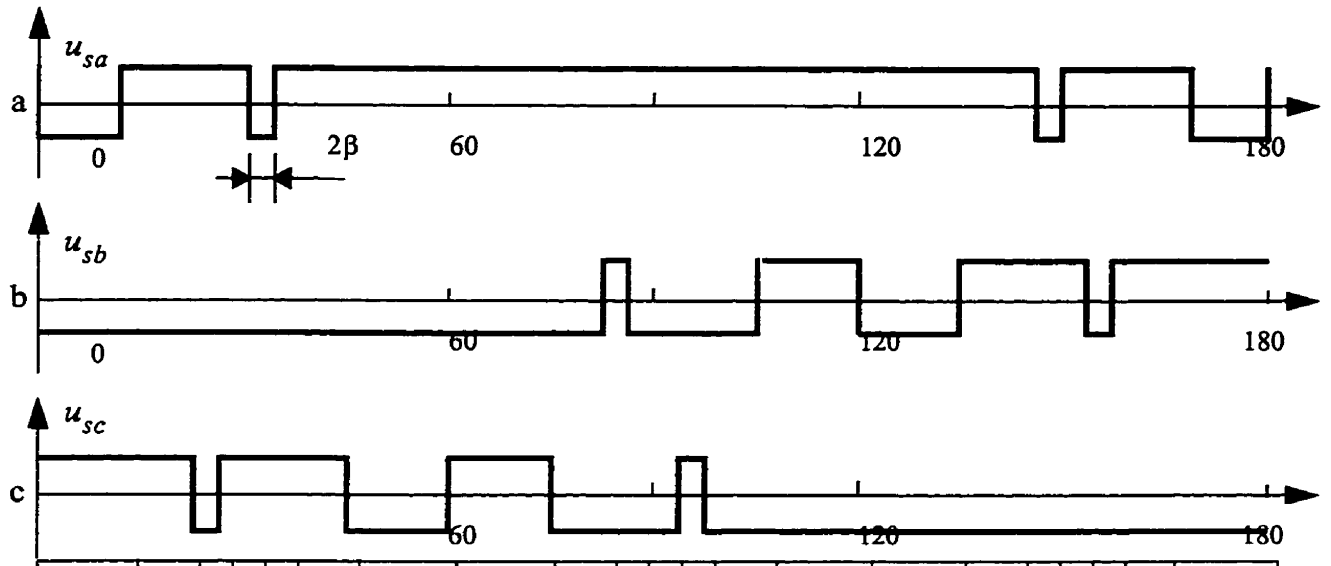


Figure 3.5 SHE-5-7A algorithm analysis in elimination of 5th and 7th harmonics



0	1	2	3	4	5	6	7	8	9	0	1	2	13	14	5	6	7	8	9	20
-	+	+	+	-	+	+	+	+	+	+	+	+	+	+	+	-	+	+	+	-
-	-	-	-	-	-	+	-	-	+	-	-	-	+	-	+	+	+	-	+	+
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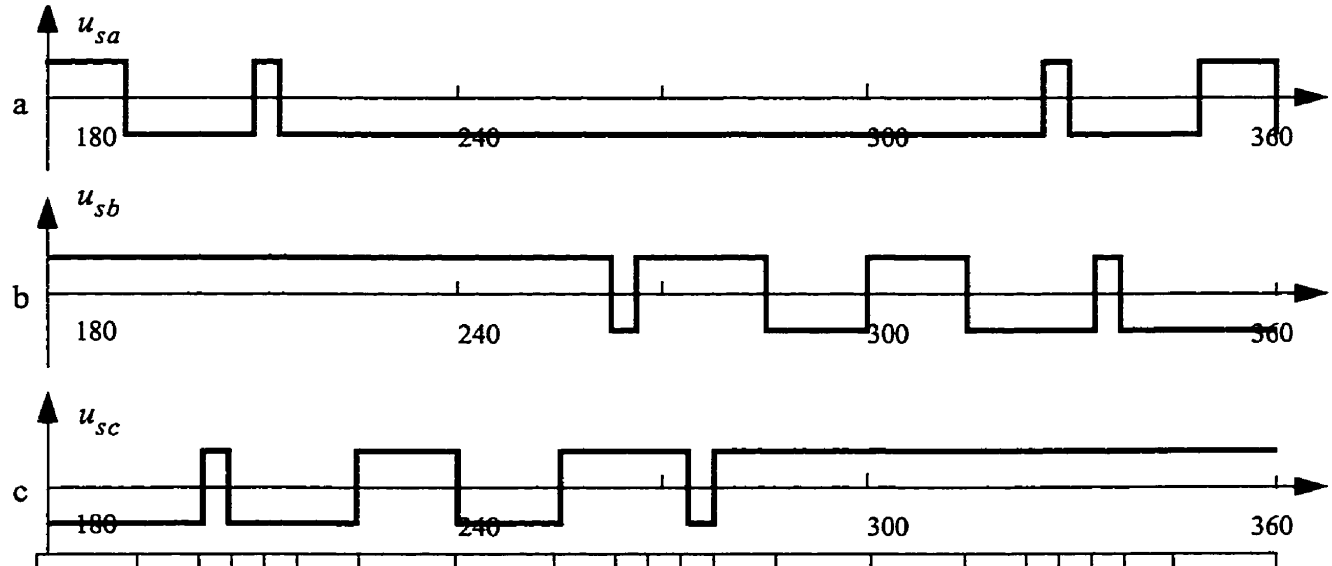


21	2	3	4	5	6	27	28	9	0	1	2	3	34	35	6	7	8	9	0	41
+	-	-	-	+	-	-	-	-	-	-	-	-	-	-	-	+	-	-	-	+
-	-	-	-	-	-	-	-	-	-	+	+	+	-	+	-	-	-	+	-	-
-	-	+	-	-	-	+	-	+	+	+	-	+	+	+	+	+	+	+	+	+

Figure 3.6 Three-phase switching scheme for 5th and 7th harmonics elimination (variant A)

3.3.2.2 SHE-5-7B

The switching scheme associated with SHE-5-7B is illustrated in Figure 3.7. Here we only use one notch placed in each quarter waveform of BSS. The objective is to adjust the position and width of this notch to eliminate 5th and 7th harmonics simultaneously. Assuming the notch begins at angle ϕ_1 and ends at angle ϕ_2 as illustrated below

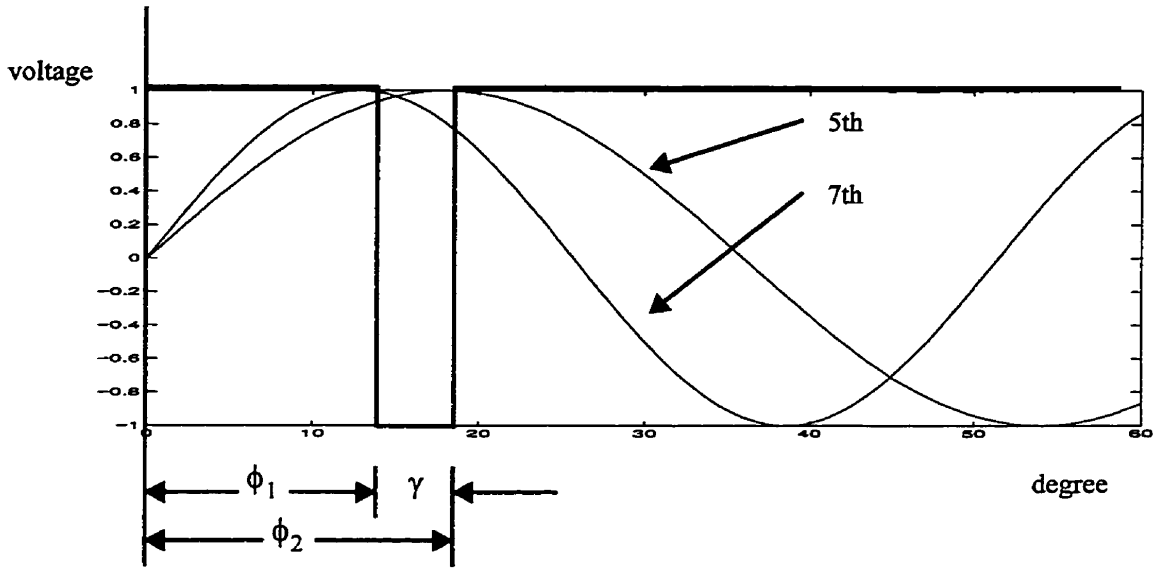


Figure 3.7 SHE-5-7B algorithm analysis in elimination of 5th and 7th harmonics

Then, the magnitude of k-th harmonic component is given by

$$\left\| \langle u \rangle_k \right\| = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} u(\omega t) \sin(k\omega t)\, d(\omega t)$$

$$= \frac{4}{\pi}\int_0^{\phi_1} \sin(k\omega t)\, d(\omega t) - \frac{4}{\pi}\int_{\phi_1}^{\phi_2} \sin(k\omega t)\, d(\omega t) + \frac{4}{\pi}\int_{\phi_1}^{\frac{\pi}{2}} \sin(k\omega t)\, d(\omega t) \quad (3.3.5)$$

$$\left\| \langle u \rangle_k \right\| = \frac{4}{k\pi}(1 - 2\cos(k\phi_1) + 2\cos(k\phi_2)) \quad (3.3.6)$$

To eliminate the 5th and 7th harmonics, we only need set $\left\| \langle u \rangle_5 \right\| = \left\| \langle u \rangle_7 \right\| = 0$. Solving two equations in two unknowns yields $\phi_1 = 16.2472°$ and $\phi_2 = 22.0685°$. The associated magnitude of the fundamental component is

$$\left\| \langle u \rangle_1 \right\| = \frac{4}{\pi}(1 - 2\cos\phi_1 + 2\cos\phi_2) = 0.9333\left(\frac{4}{\pi}\frac{U_{dc}}{2}\right) \quad (3.3.7)$$

Equation (3.3.7) indicates that the variant B can obtain 93.33% of the fundamental component (obtained with BSS), while variant A can only obtain 88.60% of the fundamental component. This illustrates that variant B has superior dc voltage utilization in comparison with variant A. Furthermore, because of the reduction in the number of notches, variant B will be easier to implement. The three phase switching scheme is described in terms of the effective line-to-neutral voltages with two state depicted in Figure 3.8, which is related to the gating signals that drive each leg of the inverter.

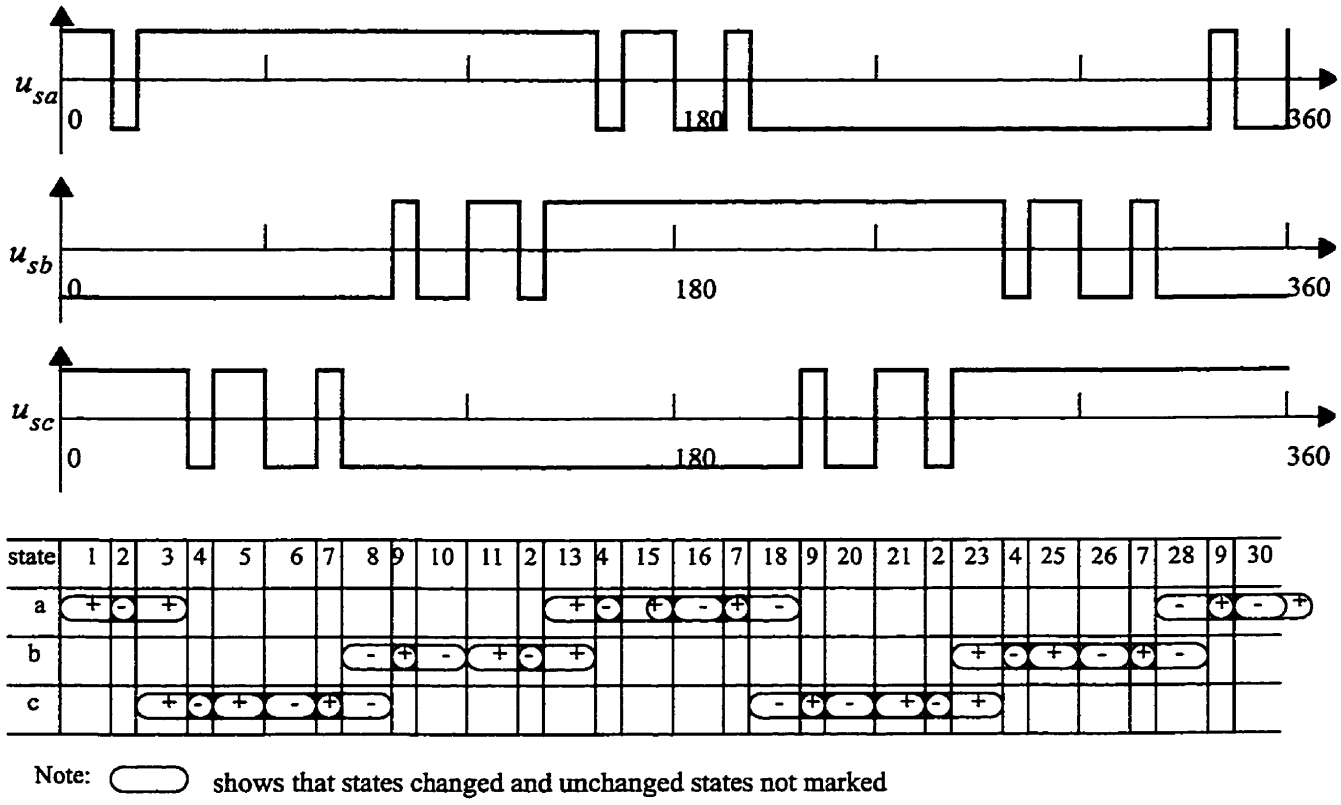


Figure 3.8 Three-phase switching scheme for 5th and 7th harmonics elimination (variant B)

3.4 Comparison of the Switching Strategies

In this chapter, we have introduced four switching schemes: BSS, SHE-5, SHE-5-7A and SHE-5-7B. Among them, BSS is the easiest to implement, but contains low-order harmonics. The other two schemes are used to eliminate 5th, or 5th and 7th harmonics which are the lowest-order characteristic harmonics. The magnitude of the fundamental component in SHE is decreased with the elimination of harmonics. The more harmonics eliminated, the smaller the magnitude of the fundamental component for a constant dc voltage. Therefore, the SHE requires an increase of the dc

voltage to reach the same compensation level as BSS. The four switching schemes are compared in Table 3.1. Please note the elimination of some low order harmonics may greatly increase the proportion of higher order harmonics. In comparison with SHE-5-7B, SHE-5-7A not only has completely eliminated the 5th and 7th harmonics, but also has reduce the proportion of the 11th and 13th harmonics. However, it has much less fundamental component than the variant B, moreover, it is relatively difficult to implement.

.

PU value of voltage components	$\frac{\langle u_a \rangle_1}{\left(\frac{U_{dc}}{2}\right)}$	$\frac{\langle u_a \rangle_5}{\left(\frac{U_{dc}}{2}\right)}$	$\frac{\langle u_a \rangle_7}{\left(\frac{U_{dc}}{2}\right)}$	$\frac{\langle u_a \rangle_{11}}{\left(\frac{U_{dc}}{2}\right)}$	$\frac{\langle u_a \rangle_{13}}{\left(\frac{U_{dc}}{2}\right)}$
BSS	$\frac{4}{\pi}$	$0.2000\left(\frac{4}{\pi}\right)$	$0.1429\left(\frac{4}{\pi}\right)$	$0.0909\left(\frac{4}{\pi}\right)$	$0.0769\left(\frac{4}{\pi}\right)$
SHE-5	$0.9563\left(\frac{4}{\pi}\right)$	0	$0.1130\left(\frac{4}{\pi}\right)$	$0.2126\left(\frac{4}{\pi}\right)$	$0.2570\left(\frac{4}{\pi}\right)$
SHE-5-7A	$0.8860\left(\frac{4}{\pi}\right)$	0	0	$0.0399\left(\frac{4}{\pi}\right)$	$0.0501\left(\frac{4}{\pi}\right)$
SHE-5-7B	$0.9333\left(\frac{4}{\pi}\right)$	0	0	$0.1894\left(\frac{4}{\pi}\right)$	$0.2532\left(\frac{4}{\pi}\right)$

Table 3.1 Comparison of the four switching schemes

Chapter 4

General Mathematical Modelling of The System

4.1 General Modelling and Analysis

The three-phase inverter-based compensator is depicted in Figure 4.1, with associated parameters C, L, R and u_{nk} (k = {1, 2, 3}) representing the dc capacitance, the inverter coupling inductance, its associated resistance and the network line to neutral voltages. The model assumes generic switching elements that can carry bidirectional currents, in this case an IGBT with an anti-parallel diode. Note that R is not a design parameter like C and L, rather it models the power loss inherent in any practical inductor. R is typically parameterized by the X/R or quality factor of the inductor.

A three phase mathematical model for the VSI-based compensator can be derived by applying Kirchhoff's voltage and current laws (KVL and KCL) to the circuit. Neglecting the resistance of the power switches, the compensator can be modelled by the following equations

$$C\frac{du_{dc}}{dt} = i_{dc} = \sum_{k=1}^{3} i_k d_k \tag{4.1.1}$$

$$L\frac{di_k}{dt} = -Ri_k - u_{sk} + u_{nk} = -Ri_k - u_{dc}d_k + u_{nk} \tag{4.1.2}$$

where

$\sum_{k=1}^{3} i_k = 0$ to satisfy KCL,

and

k index for the three-phase = {1, 2, 3}, corresponds to phases {a, b, c};

u_{nk} network k-th phase (l-n) voltage at point of coupling;

u_{sk} inverter k-th phase (l-n) voltage;

i_k line current;

u_{dc} dc capacitor voltage;

i_{dc} capacitor charging current

d_k switching function associated with phase k;

The above described parameters along with three-phase based inverter is depicted in Figure 4.1. The switching function d_k is associated with different switching schemes. For BSS the switching function is

$$d_k = \frac{1}{2}(-1)^{n(k)}$$

where $$n(k) = int\left(\frac{\omega t - (k-1)\frac{2\pi}{3}}{\pi} - 1\right) \qquad (4.1.3)$$

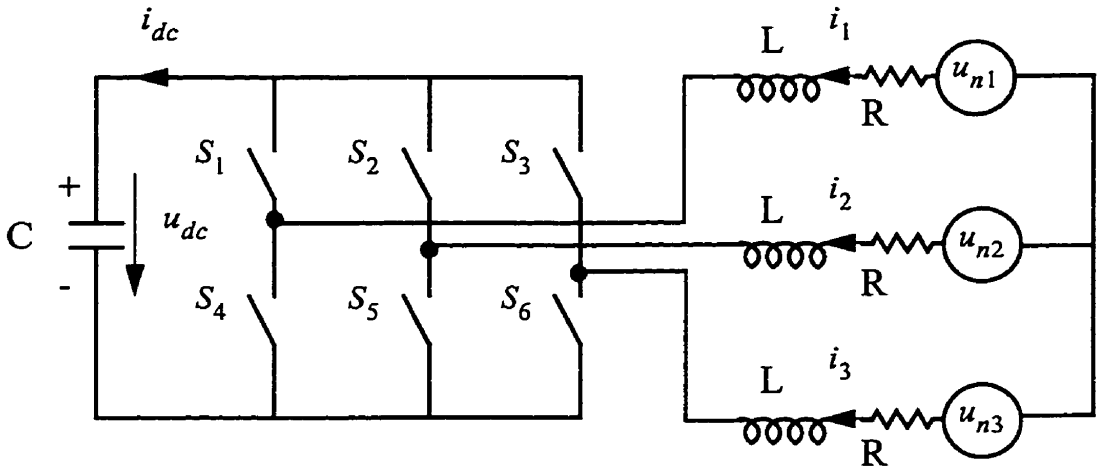


Figure 4.1 Basic circuits of three-phase voltage source inverter-based compensator

where $\omega = 2\pi f$ and f represents the working frequency of network, and int() is the function that return the integer part of the argument. Other switching schemes are more difficult to express and are not discussed here.

Consider now a nonzero phase angle as δ (radians). The switching function then becomes

$$d_k = \frac{1}{2}(-1)^{n(k)}$$

where $$n(k) = int\left(\frac{\omega t-\left((k-1)\frac{2\pi}{3}+\delta\right)}{\pi}-1\right) \qquad (4.1.4)$$

The three-phase network line to neutral (l-n) voltage at point of coupling can be expressed as

$$u_{nk} = U_{nk}\sin\left(\omega t-(k-1)\frac{2\pi}{3}\right) \qquad (k=\{1,2,3\}) \qquad (4.1.5)$$

where U_{nk} is the magnitude of network voltage (l-n).

We can verify Equation (4.1.1) by applying the Energy Conservation Law assuming a lossless inverter. Then the power at both dc and ac sides of inverter are equal at any instance, i.e. $p_{dc} = p_{ac}$, and

$$p_{ac} = \sum_{k=1}^{3} i_k u_k = \sum_{k=1}^{3} i_k u_{dc} d_k \qquad (4.1.6)$$

then,

$$C\frac{du_{dc}}{dt} = i_{dc} = \frac{p_{dc}}{u_{dc}} = \frac{p_{ac}}{u_{dc}} = \sum_{k=1}^{3} i_k d_k \qquad (4.1.7)$$

It is obvious that the (4.1.7) is identical with (4.1.1). This model can be expressed in the state-space form

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{du_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & \frac{d_1}{L} \\ 0 & -\frac{R}{L} & 0 & \frac{d_2}{L} \\ 0 & 0 & -\frac{R}{L} & \frac{d_3}{L} \\ \frac{d_1}{C} & \frac{d_2}{C} & \frac{d_3}{C} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ u_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} u_{n1} \\ u_{n2} \\ u_{n3} \end{bmatrix} \tag{4.1.8}$$

where d_1, d_2, d_3 are calculated by equation (4.1.4).

The above model is generally applicable, and can account for different switching schemes, various harmonics existing in the system and unbalanced conditions. However, the model is seldom used directly due to its complexity. Therefore, we'll set out to simplify the above model in the following section.

Now we use the computer to simulate the above model built. The PSCAD is used as graphic interface of this simulation, and the algorithm is expressed in the flowchart as shown in Figure 4.2. The simulation results of a transient when compensator operates from inductive (capacitive) to capacitive (inductive) modes are shown in Figure 4.3 and Figure 4.4 respectively. The single-phase system simulation is for comparison. We can notice that the dc bus voltage of three-phase system only has small 6th and higher order harmonic component without the largely undulated third harmonic which exists in the single phase system, and the ac output currents no longer have third harmonic, because the three phase connection configuration precludes the third harmonics in the line currents and voltages.

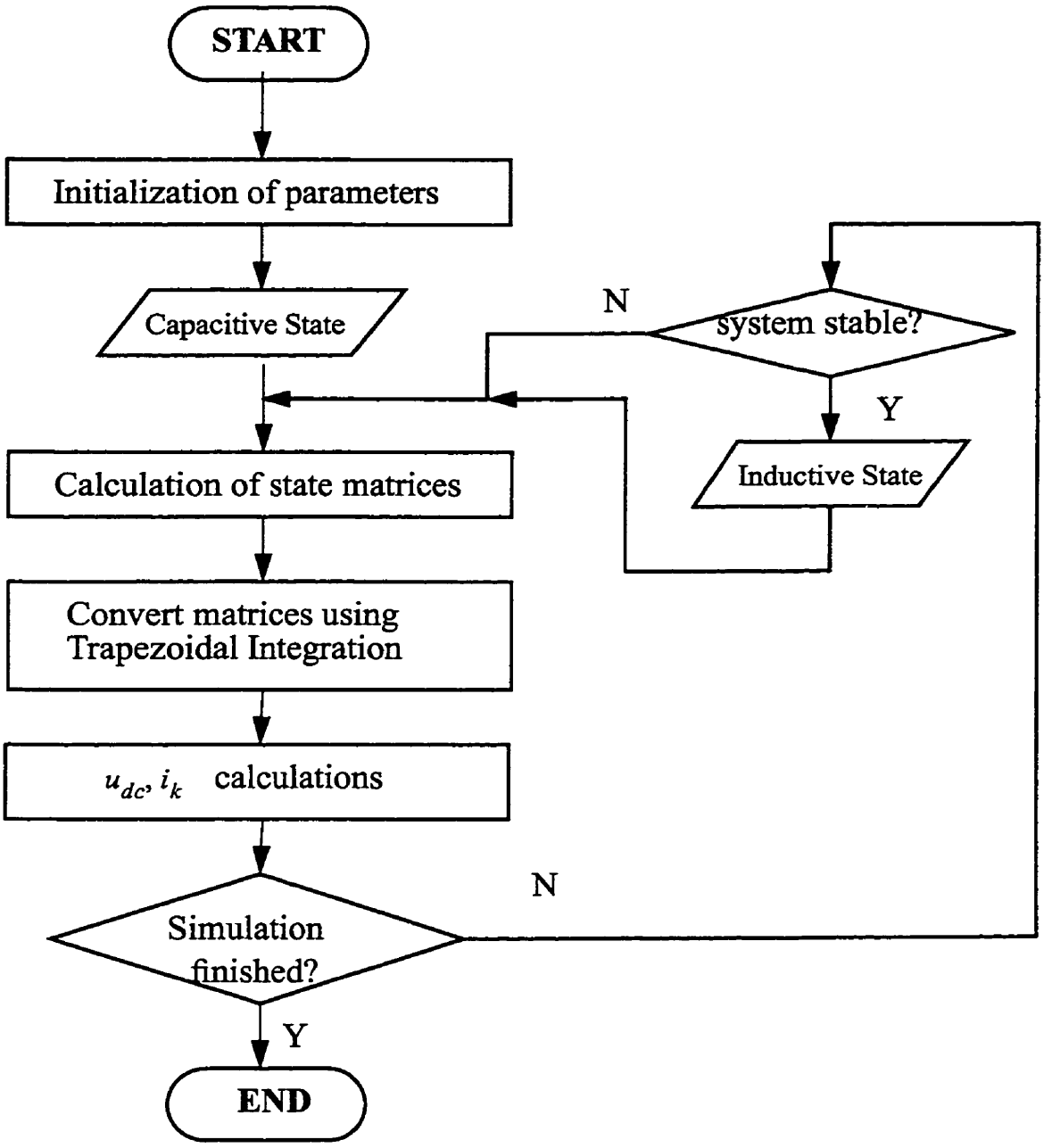


Figure 4.2 Simulation program chart based on general mathematical modelling

4.2 Modelling of Simplified System

From above simulation, we find that in the three phase system, the dc -link only embody small percent harmonic components, and the line current/voltage at the ac-side of inverter have been filtered out of third harmonic component. Therefore, we may use the fundamental component to approximately represent output voltages and currents. We can verify it using following example:

The fundamental components of u_{sk} and i_k are symbolized as $\langle u_{sk}\rangle_1$, $\langle i_k\rangle_1$ respectively. For the kth phase, it is easy to obtain

$$\langle u_{sk}\rangle_1 = \frac{2}{\pi}u_{dc}\sin\left(\omega t-\delta-(k-1)\frac{2\pi}{3}\right) \tag{4.2.1}$$

It means that

$$d_k = \frac{2}{\pi}\sin\left(\omega t-\delta-(k-1)\frac{2\pi}{3}\right) \tag{4.2.2}$$

It is obvious that the above switching function d_k is simpler than that obtain from Equation (4.1.4). Calculating d_1, d_2, d_3 based on above switching function, this new model is expressed as

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{du_{dc}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & \frac{\frac{2}{\pi}\sin(\omega t-\delta)}{L} \\ 0 & -\frac{R}{L} & 0 & \frac{\frac{2}{\pi}\sin\left(\omega t-\delta-\frac{2\pi}{3}\right)}{L} \\ 0 & 0 & -\frac{R}{L} & \frac{\frac{2}{\pi}\sin\left(\omega t-\delta+\frac{2\pi}{3}\right)}{L} \\ \frac{\frac{2}{\pi}\sin(\omega t-\delta)}{C} & \frac{\frac{2}{\pi}\sin\left(\omega t-\delta-\frac{2\pi}{3}\right)}{C} & \frac{\frac{2}{\pi}\sin\left(\omega t-\delta+\frac{2\pi}{3}\right)}{C} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ u_{dc} \end{bmatrix}.$$

$$+\begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} u_{n1} \\ u_{n2} \\ u_{n3} \end{bmatrix} \qquad (4.2.3)$$

The simulation using this approximate model has the similar algorithm in programming, and the simulation results of transient when the compensator operates from inductive (capacitive) to capacitive (inductive) mode are shown in Figure 4.5 and Figure 4.6 respectively, while its counterpart of single-phase system only for comparison.

4.4 Summary

This chapter proceeds from a general mathematical modelling of the system, for the sake of comprehending of the dynamic behaviour of system operating between capacitive mode and inductive mode. This model is simplified by neglecting harmonic components. Two modelling approaches - exact modelling which accounts all harmonics and dc link voltage ripple, and approximate modelling which only considering fundamental component are discussed and compared. The simulation results suggest that approximate analysis of a relatively simple lumped element switching model is sufficient to characterize the equilibrium behaviour of the system.

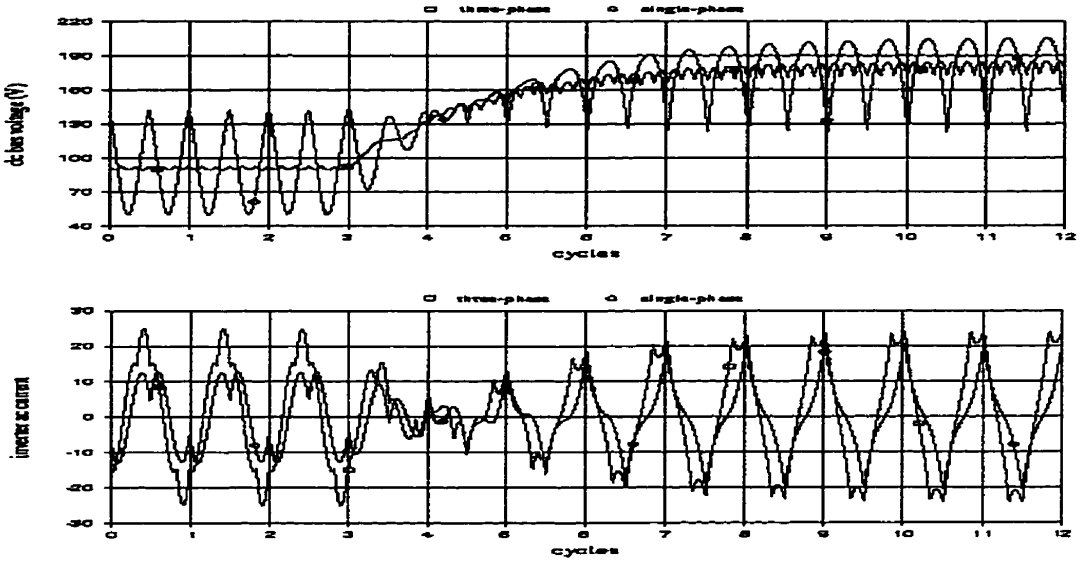


Figure 4.3 Inverter-based compensator operation from inductive state to capacitive state considering all harmonics

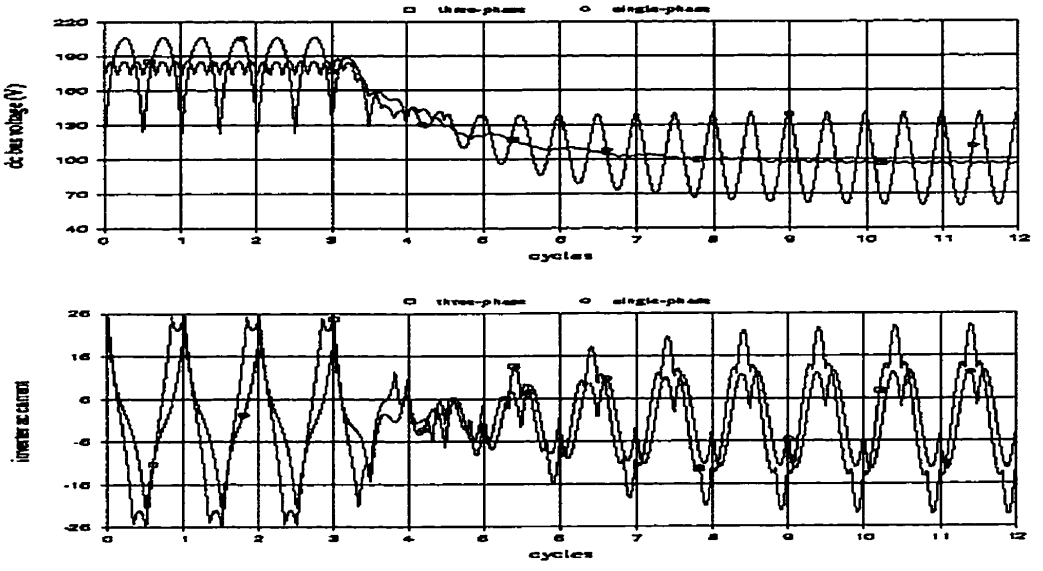


Figure 4.4 Inverter-based compensator operation from capacitive state to inductive state considering all harmonics

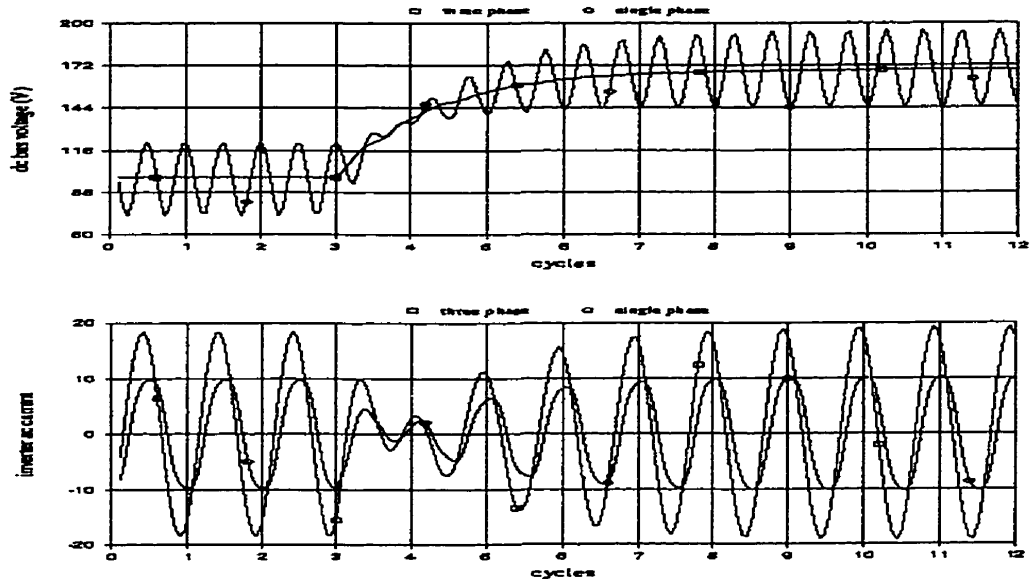


Figure 4.5 Inverter-based compensator operation from inductive mode to capacitive mode based on approximate modelling

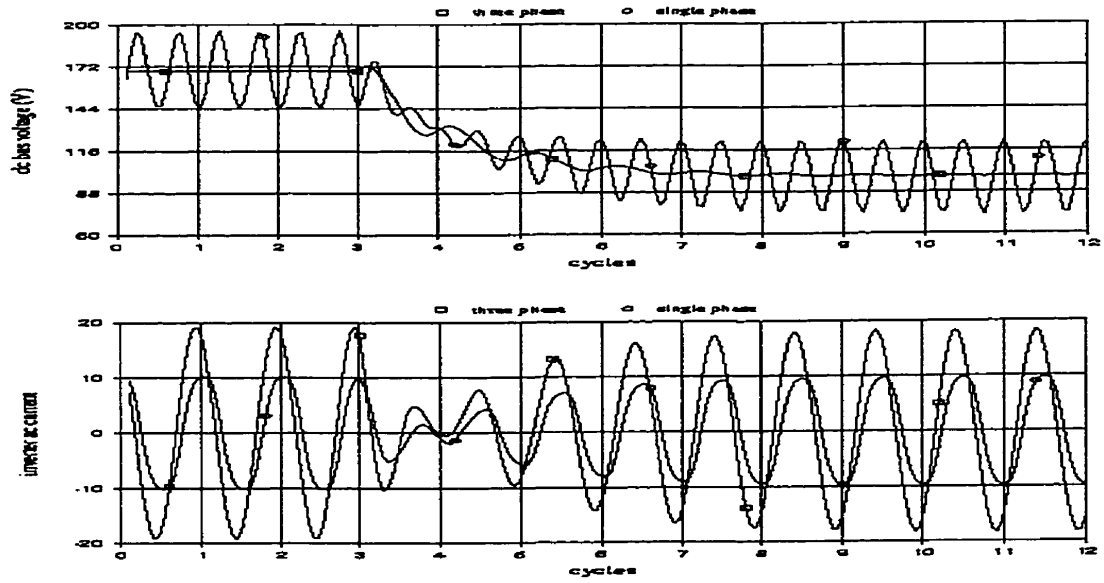


Figure 4.6 Inverter-based compensator operation from capacitive mode to inductive mode based on approximative modelling

Chapter 5

Approximate Modelling of The System

5.1 Overview

The compensator consists of a three-phase inverter shunt-connected at a point of coupling to the network. No external source of energy is used so the inverter must draw active power from the network in order to overcome compensator losses and maintain the dc voltage in associated with the compensation task. The phase angle δ is used to regulate the reactive power generated or absorbed by the compensator. Modelling of the system under stationary and dynamic conditions will be discussed.

5.2 Stationary Analysis

5.2.1 Introduction

In this section, our concern is with characterizing the periodic steady-state of the compensator as a function of the input phase angle δ.

5.2.2 Approximate Analysis

In the last chapter, we introduced a general approach to the modelling of the system. Although the method is generally applicable, it lacks physical insight and is difficult to solve [10]. Here an approximate method is developed for the analysis of the compensator under stationary behaviour. The approach approximates certain aspects of the circuit behaviour to formulate a system of equations describing the fundamental frequency behaviour of the circuit. Stationary conditions are subsequently described in closed-form and admit a ready physical explanation based on the fundamental frequency power balance. Consider the differential equations introduced in the last chapter:

$$L\frac{di_k}{dt} = -Ri_k - u_{sk} + u_{nk} = -Ri_k - u_{dc}d_k + u_{nk} \tag{5.1.1}$$

$$C\frac{du_{dc}}{dt} = i_{dc} = \sum_{k=1}^{3} i_k d_k \tag{5.1.2}$$

where the circuit variable are as before.

In the last chapter these equations were solved in detail with no approximation. In this chapter, we consider approximating certain aspects of circuit behaviour which yields a simpler model of

the compensator. The following approximations are made:

1. Only the fundamental components of d_k and i_k are accounted for

2. Only the dc component of u_{dc} is accounted for

3. Balanced conditions are assumed.

The fundamental component of i_k d_k are denoted as $\langle i_k \rangle_1$ and $\langle d_k \rangle_1$ respectively which substituted into (5.1.1) yield

$$L\frac{d\langle i_k \rangle_1}{dt} = -R\langle i_k \rangle_1 - u_{dc}\langle d_k \rangle_1 + u_{nk} \tag{5.2.3}$$

$$C\frac{du_{dc}}{dt} = \sum_{k=1}^{3} \langle i_k \rangle_1 \langle d_k \rangle_1 \tag{5.2.4}$$

The fundamental component of the switching functions associated with BSS is given by

$$\langle d_k \rangle_1 = \frac{2}{\pi}\sin\left(\omega t - \delta - (k-1)\frac{2\pi}{3}\right) \tag{5.2.5}$$

Other switching functions differ from (5.2.5) only by a scalar factor. Substitute (5.2.5) to (5.2.3) and (5.2.4),

$$L\frac{d\langle i_k \rangle_1}{dt} = -R\langle i_k \rangle_1 - u_{dc}\frac{2}{\pi}\sin\left(\omega t - \delta - (k-1)\frac{2\pi}{3}\right) + U_{nk}\sin\left(\omega t - (k-1)\frac{2\pi}{3}\right) \tag{5.2.6}$$

where U_{nk} represents the magnitude of k-th phase voltage (l-n) of network.

$$C\frac{du_{dc}}{dt} = \sum_{k=1}^{3} \langle i_k \rangle_1 \frac{2}{\pi} \sin\left(\omega t - \delta - (k-1)\frac{2\pi}{3}\right) \tag{5.2.7}$$

It is convenient to express $\langle i_k \rangle_1$ as follows

$$\langle i_k \rangle_1 = i_{II} \sin\left(\omega t - (k-1)\frac{2\pi}{3}\right) + i_{\perp} \cos\left(\omega t - (k-1)\frac{2\pi}{3}\right) \tag{5.2.8}$$

where i_{II}, $i_{\perp}$ is the parallel and quadrature components of fundamental inverter current respectively. Then the derivative of $\langle i_k \rangle_1$ is given by

$$\frac{d\langle i_k \rangle_1}{dt} = \left(\frac{di_{II}}{dt} - \omega i_{\perp}\right) \sin\left(\omega t - (k-1)\frac{2\pi}{3}\right) + \left(\frac{di_{\perp}}{dt} + \omega i_{II}\right) \cos\left(\omega t - (k-1)\frac{2\pi}{3}\right) \tag{5.2.9}$$

Substituting above equation into (5.2.3) and (5.2.4) and collecting terms in $\sin\left(\omega t - (k-1)\frac{2\pi}{3}\right)$ and $\cos\left(\omega t - (k-1)\frac{2\pi}{3}\right)$ respectively, we obtain the following differential equations with some simplification

$$\frac{di_{II}}{dt} = -\frac{R}{L} i_{II} + \omega i_{\perp} - \frac{2}{\pi}\frac{\cos\delta}{L} u_{dc} + \frac{U_{n1}}{L} \tag{5.2.10}$$

$$\frac{di_{\perp}}{dt} = -\omega i_{II} - \frac{R}{L} i_{\perp} + \frac{2}{\pi}\frac{\sin\delta}{L} u_{dc} \tag{5.2.11}$$

$$C\frac{du_{dc}}{dt} = \frac{3}{\pi}(i_{II}\cos\delta - i_{\perp}\sin\delta) \tag{5.2.12}$$

where U_{n1} represents the magnitude of line to neutral network voltage

Equations (5.2.10), (5.2.11) and (5.2.12) form a system of nonlinear differential equations in the averaged variables i_{II}, $i_{\perp}$ and u_{dc}. The equations yield a closed-form solution for the stationary conditions as follows. Let I_{II}, $I_{\perp}$ and U_{dc} denote the circuit variables under stationary conditions, then

$$\frac{dI_{II}}{dt} = \frac{dI_{\perp}}{dt} = \frac{dU_{dc}}{dt} = 0 \tag{5.2.13}$$

Under stationary conditions, the three nonlinear equations describing the system simplify to

$$RI_{II} - \omega LI_{\perp} + \frac{2}{\pi}U_{dc}\cos\delta = U_{n1} \tag{5.2.14}$$

$$\omega LI_{II} + RI_{\perp} - \frac{2}{\pi}U_{dc}\sin\delta = 0 \tag{5.2.15}$$

$$I_{II}\cos\delta - I_{\perp}\sin\delta = 0 \tag{5.2.16}$$

with closed-form solution

$$I_{II} = \frac{U_{n1}}{R}(1 - \cos 2\delta) \tag{5.2.17}$$

$$I_{\perp} = \frac{U_{n1}}{R}\frac{\sin 2\delta}{2} \tag{5.2.18}$$

$$U_{dc} = \frac{\pi}{2}U_{n1}\frac{\cos(\phi-\delta)}{\cos\phi} \tag{5.2.19}$$

where $\phi = \text{atan}\left(\frac{\omega L}{R}\right)$ represents the impedance angle associated with the coupling inductors.

The solution describes the stationary conditions as a function of the circuit parameters and the control parameter δ. Note that I_{II} and $I_{\perp}$ are not directly measurable quantities, however, we can express the magnitude of the fundamental component of the inverter current

$$|I_k| = \sqrt{I_{II}^2 + I_{\perp}^2} = \frac{1}{\sqrt{2}}\frac{U_{n1}}{R}\sqrt{1-\cos 2\delta} = \frac{U_{n1}}{R}|\sin\delta| \tag{5.2.20}$$

The operation of the compensator can be easily explained in terms of the fundamental frequency power flow

$$S_n = P_n + jQ_n = \frac{3}{2}U_{n1}I_k^* = \frac{3}{2}U_{n1}(I_{11} - jI_{\perp}) \tag{5.2.21}$$

where I_k^* is the conjugation of I_k, then

$$P_n = \frac{3}{2}U_{n1}I_{II} = \frac{3}{2}\frac{U_{n1}^2}{R}(1-\cos 2\delta) = \frac{1}{2}\frac{U_n^2}{R}(1-\cos 2\delta) \tag{5.2.22}$$

$$Q_n = -\frac{3}{2}U_n I_{\perp} = -\frac{3}{4}\frac{U_{n1}^2}{R}\sin 2\delta = -\frac{1}{4}\frac{U_n^2}{R}\sin 2\delta \tag{5.2.23}$$

where U_n represents the peak magnitude of network line to line voltage.

The above equations illustrate that the compensator always absorbs nominal real power in order to maintain equilibrium however generates or absorbs reactive power depending on the sign of δ.

5.3 Dynamic Modelling

5.3.1 Introduction

Now we need to deal with the consequences of the inevitable disturbances or errors that cause circuit operation to deviate from the nominal. These disturbances include variations and uncertainties in source, load, and circuit parameters or perturbation in switching times [11]. We refer to the resulting evolution of the deviations from nominal behaviour as the dynamic behaviour.

Most often, departures from nominal conditions have to be counteracted through properly designed controls. A controller or "compensator" must first provide the user with simple and convenient means of selecting the desired nominal operation condition. Second, it must automatically regulate the circuit at this operating condition by delaying or advancing the times at which switches are turned on and off. Hence, the focus of this section will be on analysis and control design by means of appropriate dynamic models. This approach allows us to anticipate the behaviour of the circuit under diverse operating conditions, generate candidate controller structures and parameters, plan simulation studies, understand experimental results, recognize which regimes of operation call for further investigation, and so on.

In this section, an approach is described and based on an averaging in time and leads to a sys-

tem of continuous-time differential equations [10] [12]. This approach involves linearization of the continuous-time differential equations about a nominal operating point.

5.3.2 Linearized Average Model

Consider the differential equations developed in the previous section

$$\begin{cases} \dfrac{di_{II}}{dt} = -\dfrac{R}{L}i_{II} + \omega i_{\perp} - \dfrac{2}{\pi}\dfrac{\cos\delta}{L}u_{dc} + \dfrac{U_{n1}}{L} & (5.3.1) \\ \dfrac{di_{\perp}}{dt} = -\omega i_{II} - \dfrac{R}{L}i_{\perp} + \dfrac{2}{\pi}\dfrac{\sin\delta}{L}u_{dc} & (5.3.2) \\ C\dfrac{du_{dc}}{dt} = \dfrac{3}{\pi}(i_{II}\cos\delta - i_{\perp}\sin\delta) & (5.3.3) \end{cases}$$

Equations (5.3.1), (5.3.2) and (5.3.3) form a system of non-linear differential equations in the averaged variables. It is desirable to obtain a set of linearized equations describing the dynamics of the system at a given operating point. Suppose that the system is operating at the steady-state operating point associated with δ_0, then

$$I_{II} = \frac{U_{n1}}{R}(1 - \cos 2\delta_0) \qquad (5.3.4)$$

$$I_{\perp} = \frac{U_{n1}}{R}\frac{\sin 2\delta_0}{2} \qquad (5.3.5)$$

$$U_{dc} = \frac{\pi}{2} U_{n1} \frac{\cos(\phi - \delta_0)}{\cos\phi} \tag{5.3.6}$$

Now consider the following perturbations to the above operating point expressed as follows

$$\begin{cases} i_{II} = I_{II} + \tilde{i}_{II} \\ i_{\perp} = I_{\perp} + \tilde{i}_{\perp} \\ \delta = \delta_0 + \tilde{\delta} \end{cases}$$

where the tided quantities represent deviations from the steady-state operation point.

Substituting into (5.3.1), (5.3.2) and (5.3.3) and neglecting second-order terms yields the following set of linear differential equations in the perturbed quantities:

$$\frac{d}{dt}\tilde{i}_{II} = -\frac{R}{L}\tilde{i}_{II} + \omega\tilde{i}_{\perp} - \frac{2}{\pi}\frac{\cos\delta_0}{L}\tilde{u}_{dc} + \frac{2}{\pi}\frac{\sin\delta_0}{L}U_0\tilde{\delta} \tag{5.3.7}$$

$$\frac{d}{dt}\tilde{i}_{\perp} = -\omega\tilde{i}_{II} - \frac{R}{L}\tilde{i}_{\perp} + \frac{2}{\pi}\frac{\sin\delta_0}{L}\tilde{u}_{dc} + \frac{2}{\pi}\frac{\cos\delta_0}{L}U_0\tilde{\delta} \tag{5.3.8}$$

$$\frac{d}{dt}\tilde{u}_{dc} = \frac{3}{\pi C}\cos\delta_0\tilde{i}_{II} - \frac{3}{\pi C}\sin\delta_0\tilde{i}_{\perp} - \frac{3}{\pi C}(I_{II}\sin\delta_0 + I_{\perp}\cos\delta_0)\tilde{\delta} \tag{5.3.9}$$

Note that the above equations admit the state-space form

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + B\tilde{\delta} \tag{5.3.10}$$

where $\tilde{x} = \begin{bmatrix} \tilde{i}_{II} \\ \tilde{i}_{\perp} \\ \tilde{u}_{dc} \end{bmatrix}$

$$A = \begin{bmatrix} -\frac{R}{L} & \omega & -\frac{2}{\pi}\frac{\cos\delta_0}{L} \\ -\omega & -\frac{R}{L} & \frac{2}{\pi}\frac{\sin\delta_0}{L} \\ \frac{3}{\pi C}\cos\delta_0 & -\frac{3}{\pi C}\sin\delta_0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{2}{\pi}\frac{\sin\delta_0}{L}U_0 \\ \frac{2}{\pi}\frac{\cos\delta_0}{L}U_0 \\ \frac{3}{\pi C}(I_{II}\sin\delta_0 + I_{\perp}\cos\delta_0) \end{bmatrix}$$

Substituting the element parameters of the three-phase inverter-based compensator laboratory prototype to above matrices A and B, and when compensator operates in inductive mode associated with $\delta_0 = -2.7°$ and in capacitive mode associated with $\delta_0 = 2.85°$, then we obtain

i) for $\delta_0 = -2.7°$,

$$A = \begin{bmatrix} -0.1786 & 1.0000 & -0.4819 \\ -1.0000 & -0.1786 & 0.0227 \\ 1.0543 & 0.0497 & 0 \end{bmatrix}\omega \qquad B = \begin{bmatrix} -2.2268 \\ 47.2200 \\ 17.9442 \end{bmatrix}\omega$$

or in transfer function form

$$\tilde{u}_{dc}(s) = \frac{17.0615\,[s-(-0.1786+1.9443i)]\,[s-(-0.1786-1.9443i)]}{(s-0.0812)\,[s-(-0.1085+0.8240i)]\,[s-(-0.01085-0.8240i)]}\tilde{\delta}(s)$$

ii) for $\delta_0 = 2.85°$,

$$A = \begin{bmatrix} -0.1786 & 1.0000 & -0.4819 \\ -1.0000 & -0.1786 & 0.0240 \\ 1.0541 & -0.0525 & 0 \end{bmatrix}\omega \qquad B = \begin{bmatrix} 4.0839 \\ 82.0330 \\ -18.9451 \end{bmatrix}\omega$$

or in transfer function form

$$\tilde{u}_{dc}(s) = \frac{-22.4657\,(s+2.0695)\,(s-1.7124)}{(s+0.0355)\,[s-(-0.0616+0.6270i)]\,[s-(-0.0616-0.6270i)]}\tilde{\delta}(s)$$

where $\omega = 377$ rad/sec associated with the 60 Hz working frequency. The above will be used in the coming chapter.

5.4 Summary

This chapter has introduced a simple means of characterizing the fundamental frequency behaviour of the compensator. This approach permits the characterization of stationary and dynamic behaviour of the compensator in terms of the system parameters, the switching scheme used and the input phase angle. Furthermore, the above characterization motivates a simple approach to the control of the three-phase inverter-based compensator developed in the following chapter.

Chapter 6

Comparison With Laboratory Prototype

6.1 Overview

The model of the inverter-based compensator under stationary and dynamic behaviour developed in the last chapter is compared with results obtained on a laboratory prototype. Feedforward control, stability analysis and feedback control are also discussed and supported with experimental results. It is demonstrated that the laboratory prototype behaves satisfactorily under stationary and dynamic conditions.

6.2 Comparison of Stationary Behaviour

The stationary analysis of the last chapter approximates certain aspects of the circuit behaviour to formulate a system of equations describing the dynamics of the fundamental frequency components of the circuit variables. The stationary conditions are subsequently described in closed form and admit a ready physical explanation based on the fundamental frequency power balance.

In the following, the stationary behaviour of the three switching schemes described in Chapter 3 are compared with experimental results. The network voltage in the experiment is set to 60 V rms (l-n).

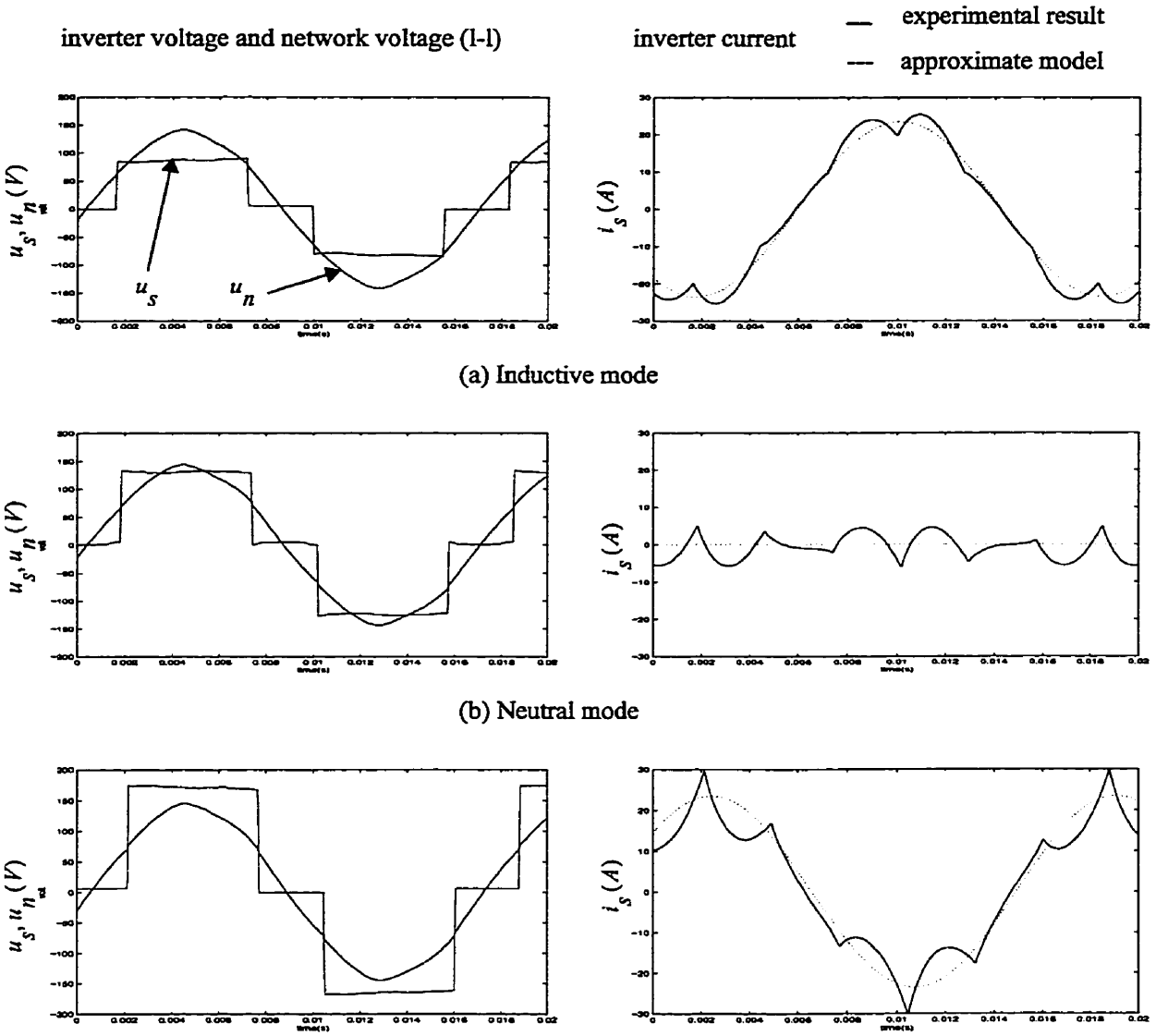
6.2.1 BSS

The software associated with the basic switching scheme (BSS) was implemented on the DSP. Figure 6.1 depicts operating points associated with inductive ($\delta = -5°$), neutral ($\delta = 0°$) and capacitive ($\delta = 5°$) compensation modes respectively. The compensator is said to be operating in capacitive (inductive) mode when it is generating (absorbing) fundamental frequency reactive power. Note the harmonic distortion in the compensator current associated with BSS. Also note that the inverter and network voltages u_s, u_n are line to line voltages.

6.2.2 SHE-5

The software associated with SHE-5 was implemented on the DSP enabling the compensator to operate in capacitive or inductive mode as required while eliminating the 5th harmonic. Figure 6.2 depicts the tested waveforms of the compensator voltage and current in different operating modes associated with SHE-5.

It is obvious that the harmonic distortion in the compensator current associated with SHE-5 is somewhat reduced in comparison with that of BSS.



(a) Inductive mode

(b) Neutral mode

(c) Capacitive mode

Figure 6.1 Comparison of inverter ac current and voltage waveforms at different operation modes

6.2.3 SHE-5-7

The software associated with SHE-5-7B was implemented in favour of SHE-5-7A for reasons

discussed in Chapter 3. This enables the compensator to operate in inductive ($\delta = -5°$), neutral ($\delta = 0°$) and capacitive ($\delta = 5°$) compensation modes as required while eliminating the 5th and 7th harmonics. Consequently the harmonic distortion in the inverter compensator current is further reduced as depicted in Figure 6.3.

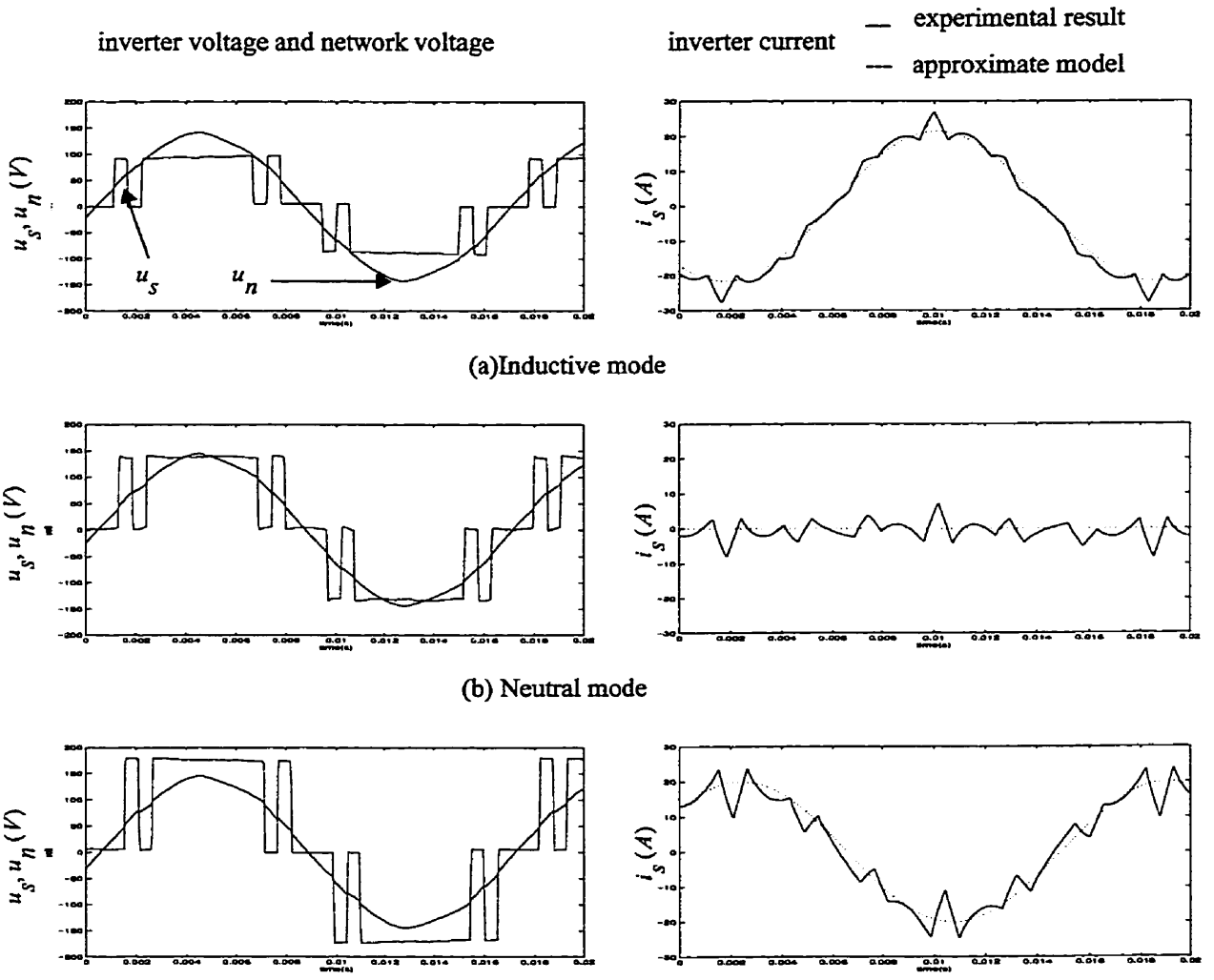


Figure 6.2 Comparison of inverter ac current and voltage waveforms based on SHE-5 at different mode

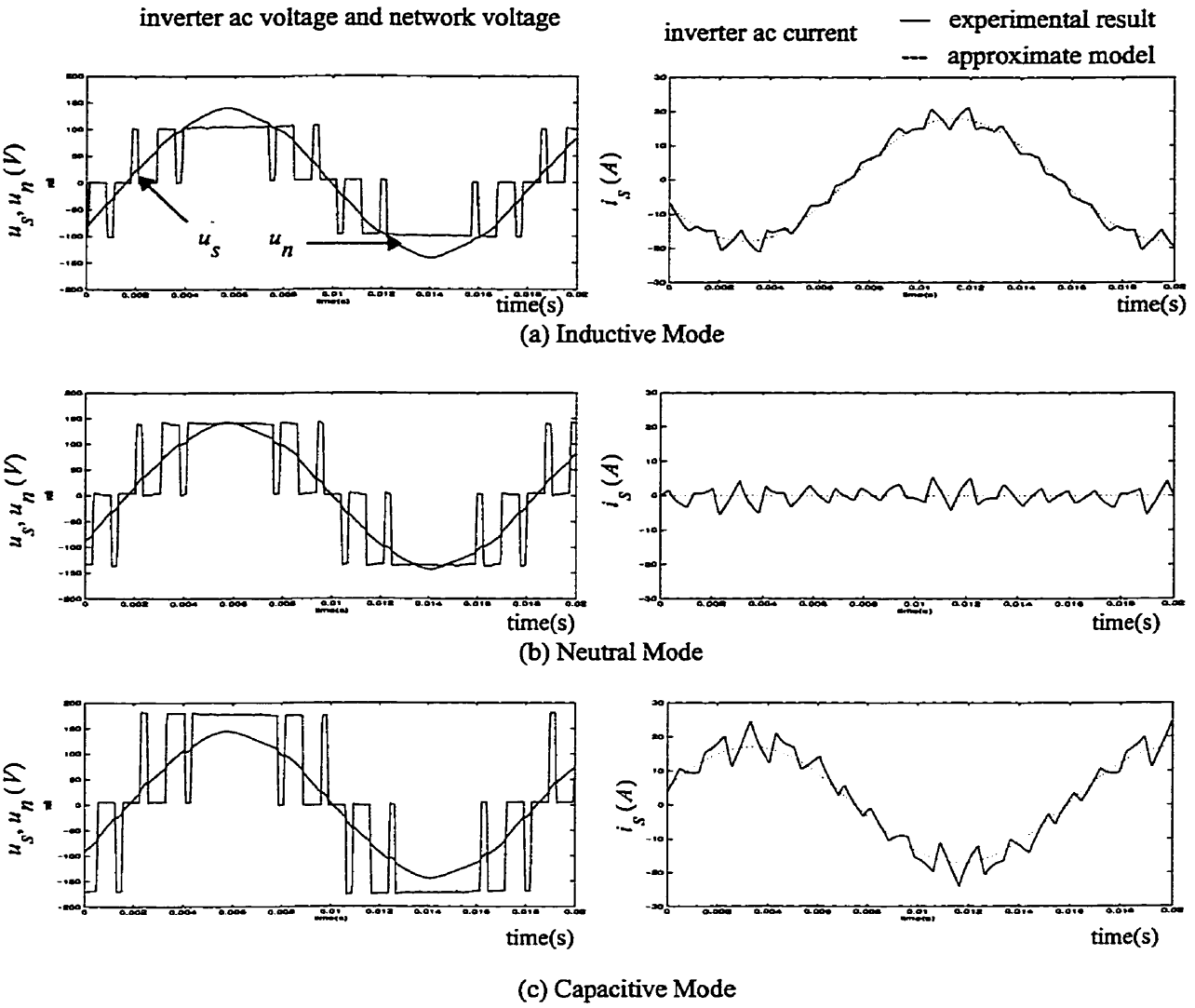


Figure 6.3 Inverter ac current/voltage waveform at different operation modes

6.2.4 Comparison of Results

Note that the compensator current associated with SHE-5-7 more closely approximates a sinesoid than either SHE-5 or BSS. However, the elimination of selective harmonics with SHE requires an increased dc voltage for the same level of the compensation. Figure 6.4 illustrates the

effectiveness of the SHE schemes in eliminating selected low order harmonics. The figure depicts the harmonics decomposition of the currents associated with the inductive compensation mode.

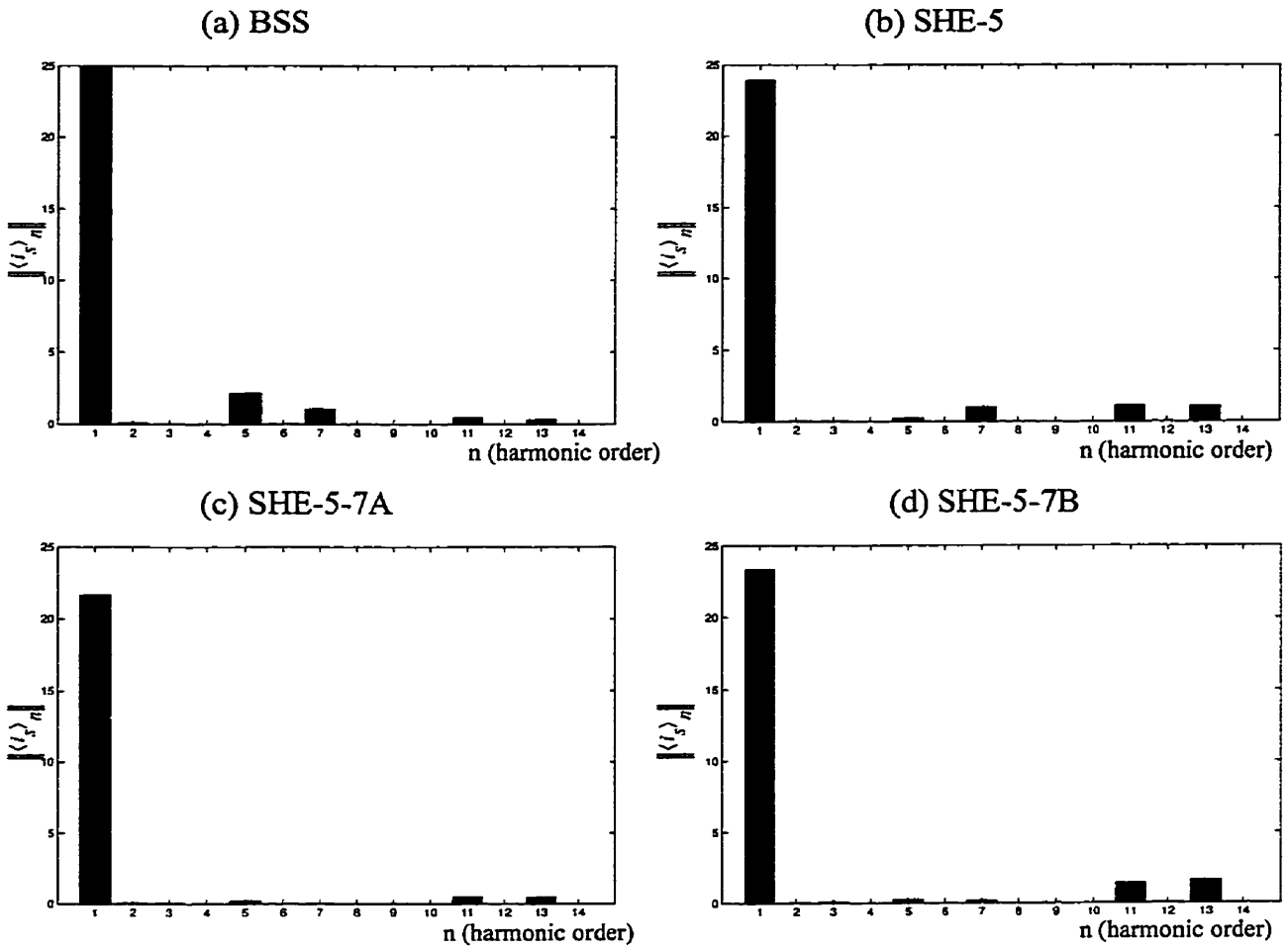


Figure 6.4 Harmonic components of compensation currents for different switching schemes

6.3 Feedforward Control

The analysis outlined in chapter 5 describes a relationship between the input δ and the steady-

state operating point of the compensator. For a given switching scheme, the operating point of the compensator can be completely characterized by the dc voltage on the assumption of a fixed network voltage. This suggests a feedforward control scheme in which the desired steady-state operating point is obtained by means of realizing an appropriate δ. Such a scheme precludes the need to sense any circuit variable.

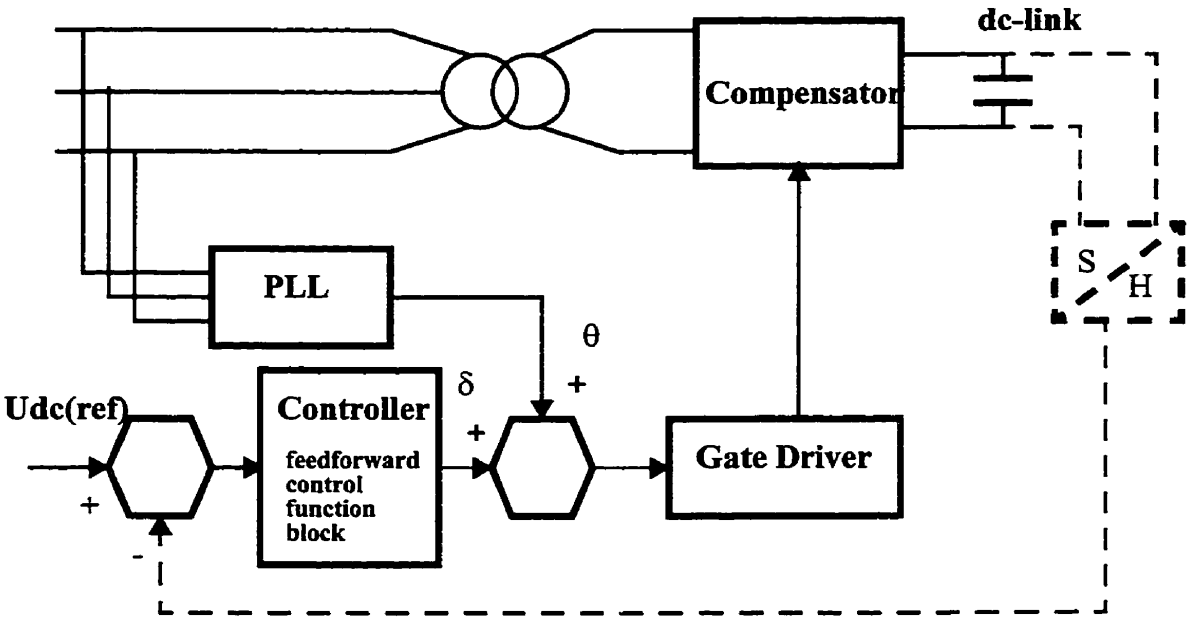


Figure 6.6 Feedforward control of dc-link voltage of compensator

The idea of feedforward control is embedding δ as a function of u_{dc} (which characterizes the operating point) in the controller based on the knowledge of the parameters of the system. Consequently we can obtain the desired dc voltage (operating point) by feedforward control of the input δ.

In the following sections, we will compare the analysis of chapter 5 with the experimental

results obtained from the laboratory prototype for the three switching schemes. A means of overcoming the discrepancy between the experimental and analytical results will also be presented.

6.3.1 Feedforward Control with BSS

From (5.2.19), the dc voltage of the compensator under stationary conditions is given by

$$U_{dc} = \frac{\pi}{2} U_{n1} \frac{\cos(\phi - \delta)}{\cos\phi} \tag{6.3.1}$$

In neutral mode, there is essentially no fundamental frequency current flow in the compensator and network (except for a small current for overcoming losses). The equation (6.3.1) provides a simple relation between δ and U_{dc} in steady state. In neutral mode when $\delta = 0°$, $U_{dc} = \frac{\pi}{2} U_{n1} = 133V$. For small δ and assuming ϕ is fixed, then U_{dc} as a function of δ is approximately a straight line. However, the parameter $\phi = \text{atan}\left(\frac{\omega L}{R}\right)$ cannot be calculated out directly, because the R which represents the compensator losses is not directly measurable. Therefore, the parameter $\phi = \text{atan}\left(\frac{\omega L}{R}\right)$ must be experimentally obtained.

The experimental set up for the first measurement is based on the Basic Switch Scheme which was introduced in Chapter 3. Figure 6.7 plots the experimental curve (E) for u_{dc} as a function of δ for BSS. The latency of the system has been compensated in the experimental data.

From the experimental results, it is obvious that the relation between δ and U_{dc} is nonlinear but symmetrical about the point (0°, 133V). A central symmetrical axis of the experimental

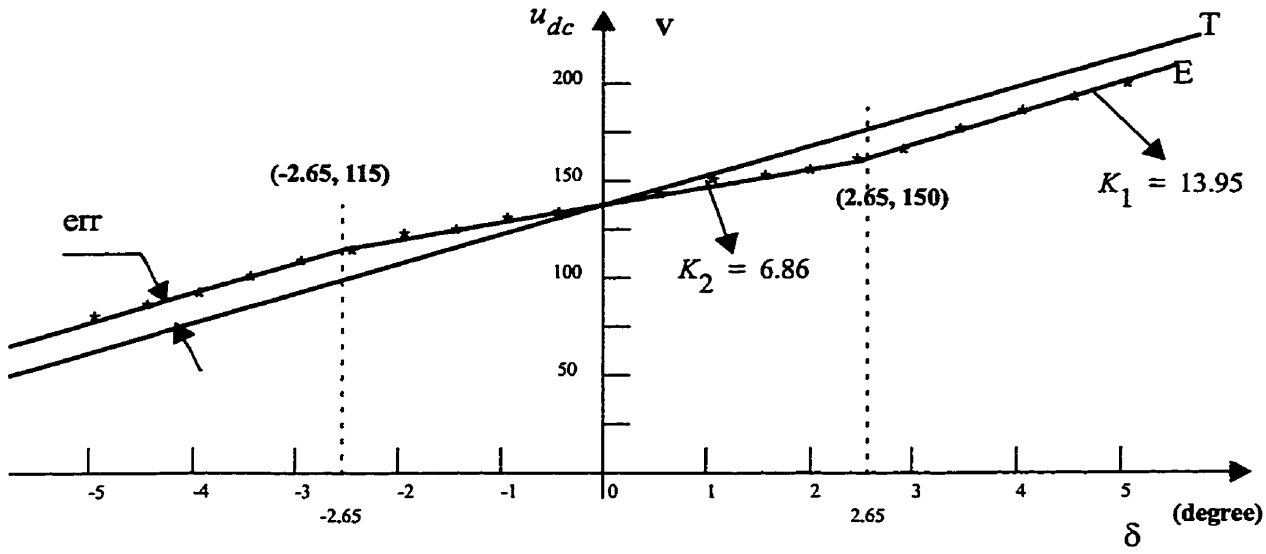


Figure 6.7 Experimental and theoretical curve of δ and u_{dc} based on BSS

curve is denoted as T, which approximately represents the relation of δ and U_{dc} . In this case, we obtain $\tan\phi = 5.6 = \frac{\omega L}{R}$.

Note, however, from Equation (6.3.2) that the approximation is worse as δ increases in magnitude. A piecewise linearization is used to approximate the nonlinear experimental curve for the feedforward control implementation. The piecewise line can be expressed as

$$\begin{cases} U_{dc} = 13.95\delta + 151.85, & \delta \le -2.65^\circ; \\ U_{dc} = 6.86\delta + 133.00, & -2.65^\circ < \delta < 2.65^\circ; \\ U_{dc} = 13.95\delta + 251.75, & \delta \ge 2.65^\circ \end{cases} \qquad (6.3.2)$$

or δ as a function of U_{dc}:

$$\begin{cases} \delta = \dfrac{U_{dc}}{13.95} - 10.89 , & U_{dc} \le 115V; \\ \delta = \dfrac{U_{dc}}{6.86} - 19.39 , & 115V < U_{dc} < 150V ; \\ \delta = \dfrac{U_{dc}}{13.95} - 18.05 , & U_{dc} \ge 150V \end{cases} \tag{6.3.3}$$

The above equations can be directly implemented for feedforward control.

6.3.2 Feedforward Control with SHE-5

The experimental results associated with SHE-5 are depicted in Figure 6.8, along with its centre-symmetrical axis T representing an approximate relation between δ and U_{dc}, from which we obtain $\tan\phi = 4.5 = \dfrac{\omega L}{R}$ by using (6.3.1).

The piecewise representation of SHE-5 is expressed as

$$\begin{cases} \delta = \dfrac{U_{dc}}{11.55} - 13.56 , & U_{dc} \le 127V; \\ \delta = \dfrac{U_{dc}}{5.36} - 26.59, & 127V < U_{dc} < 154V ; \\ \delta = \dfrac{U_{dc}}{11.55} - 10.72 , & U_{dc} \ge 154V \end{cases} \tag{6.3.4}$$

The above functions are implemented by controller and experimental results demonstrate the effective of the feedforward control.

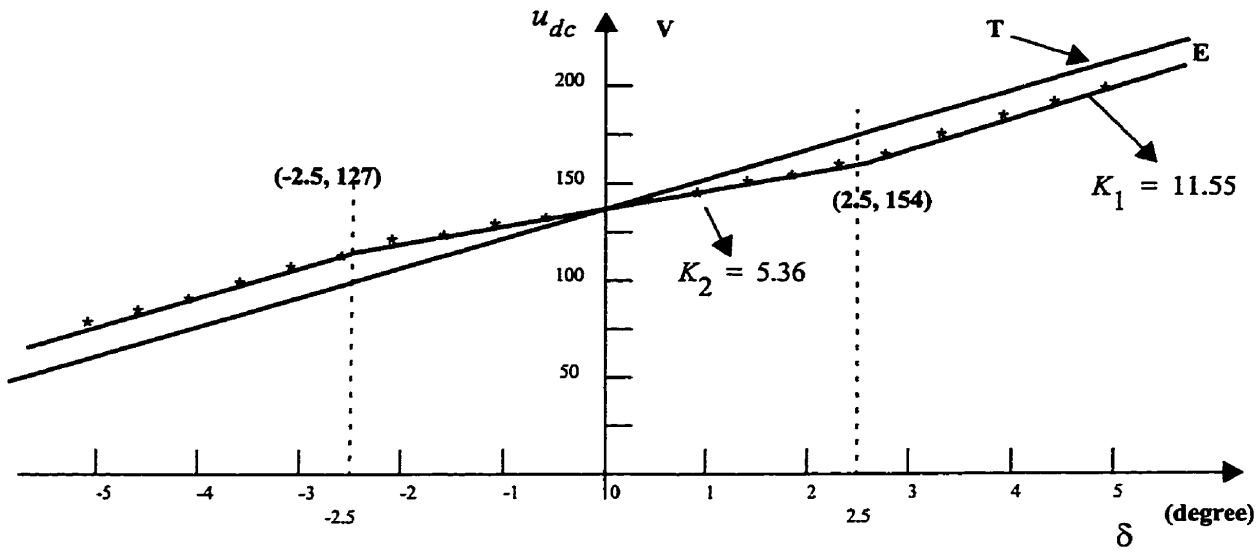


Figure 6.8 Experimental and theoretical curve of δ and u_{dc} based on SHE-5

6.3.3 Feedforward Control with SHE-5-7

In this experiment, we only consider using SHE-5-7B, which has been proved to be superior in performance and easier in implementation in comparison with SHE-5-7a. The details of the switching scheme refer to Chapter 3. Figure 6.9 depicts the experimentally obtained relation between δ and U_{dc}, along with its centre-symmetrical axis T - which roughly approximates the relation δ and U_{dc}, from which we obtain $\tan\phi = 4.02 = \frac{\omega L}{R}$ by using (6.3.1).

The piece-wise approximation of the relation between U_{dc} and δ for SHE-5-7B is expressed as

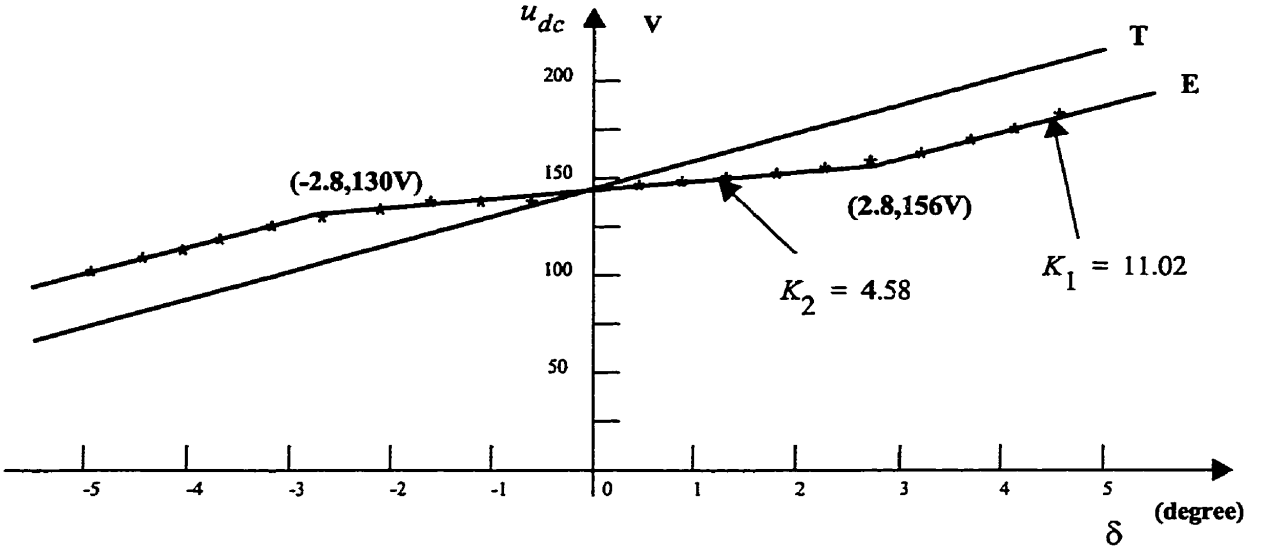


Figure 6.9 Experimental and theoretical curve of δ and u_{dc} based on SHE-5-7B

$$\begin{cases} \delta = \dfrac{U_{dc}}{11.02} - 14.38 , & U_{dc} \le 132V; \\ \delta = \dfrac{U_{dc}}{4.58} - 31.00 , & 132V < U_{dc} < 154V \quad ; \\ \delta = \dfrac{U_{dc}}{11.02} - 11.57 , & U_{dc} \ge 154V \end{cases} \qquad (6.3.5)$$

The above functions are embedded in the controller and experimental results demonstrate the effective of the feedforward control.

The deviations from the desired value can be further minimized by feedback of the dc voltage which is the subject of section 6.5.

6.4 Open-Loop Dynamic Performance

In order to compare the linearized dynamic model with the laboratory prototype, the compensator is controlled with a step change in the dc voltage order. Figure 6.10 corresponds to a change from inductive to capacitive operation of the compensator. Note that the compensator requires

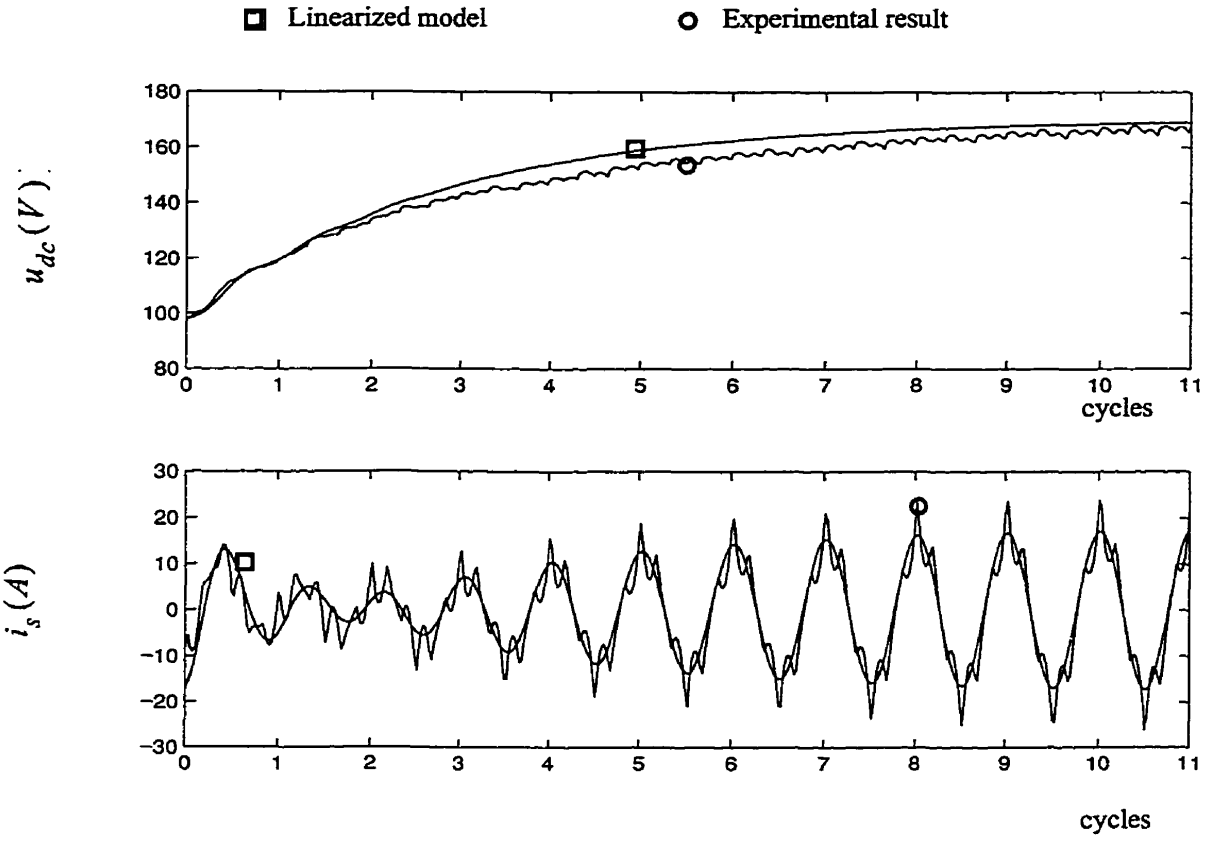


Figure 6.10 Dynamic behaviour (from inductive to capacitive operation) of inverter at open-loop

about nine cycles to effect this change in open-loop. This would not be sufficient to compensate rapidly changing load conditions. Also note that the linearized dynamic model represents the fundamental frequency response of the prototype.

Figure 6.11 corresponds to a change from capacitive to inductive operation of the compensator. Note again the relatively slow dynamic response. The response of linearized dynamic model is also shown for comparison.

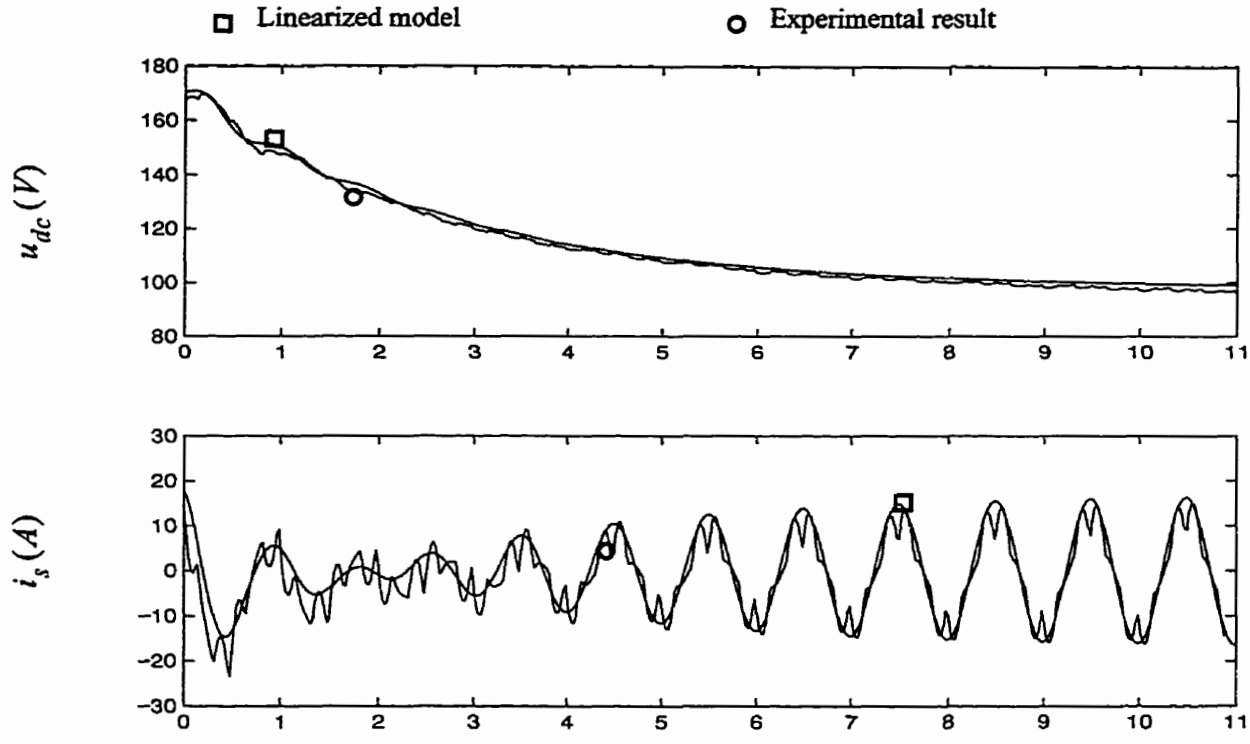


Figure 6.11 Dynamic behaviour (from capacitive to inductive operation mode) at open-loop

6.5 Closed - Loop Dynamic Performance

In order to minimize steady-state error and impose dynamic performance, a feedback of the dc voltage is in order as depicted in Figure 6.12. The feedback is implemented with a resistive voltage divider, isolation amplifier and analog-to-digital converter (ADC). In order to facilitate implementation the dc voltage is sampled once per cycle.

The feedforward control is augmented with a proportional control based in the dc voltage error. The following section investigates the stability of such a scheme

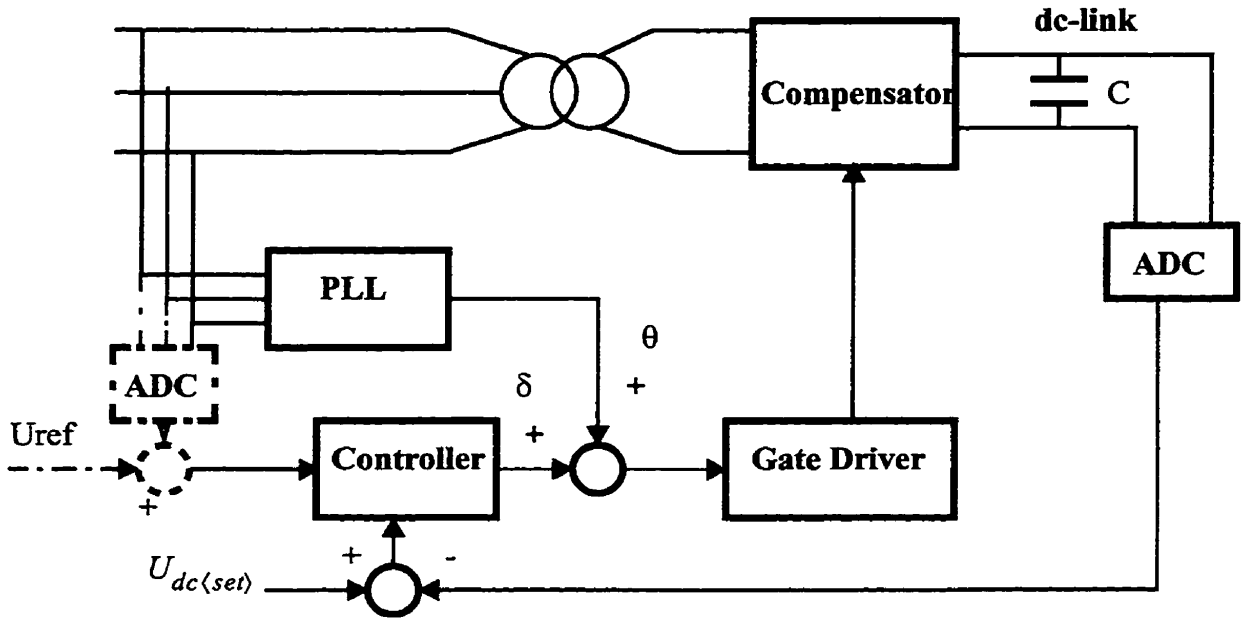


Figure 6.12 Feedback control of dc-link voltage of compensator

6.5.1 Root Locus Stability Analysis

Closed-loop stability is the primary concern in control design [11]. The secondary concern is typically dynamic response of the closed-loop system.

Larger controller gains mean greater amplification of the error signal, resulting in smaller steady-state errors and improved dynamic response. Stability considerations usually impose an upper limit on the gain, and hence a limit in dynamic performance.

A root locus plot associated with the linearized dynamic model is used to determine the range of permissible controller gains, where the controller has the feedforward / feedback structure

$$\delta = \delta_0 + (-K)\ (u_{dc} - u_{dc}^*)$$

where δ_0 represents the initial value of the firing angle; u_{dc}* represents the dc voltage set point, u_{dc} represents the dc voltage feedback, K represents the controller gain ('-' indicates this is a negative feedback) and δ represents the calculated value of the phase angle to be effected by the switching scheme.

When the dc voltage u_{dc} is different from the desired u_{dc}*, for example $u_{dc} > u_{dc}$*, then $(-K)\ (u_{dc} - u_{dc}^*) < 0$, so that $\delta < \delta_0$, which means that the controller is reducing the δ to try to decrease the dc voltage to reach the desired set point (u_{dc}*). Clearly, the larger the gain K, then the larger the δ change, and hence the faster the dc voltage reach the value set. However, all of these are subject to the stability limit imposed on the gain K.

Root locus is used to determine system stability in operating modes. The root locus plots associated with the linearized dynamic model obtained in the last chapter are depicted in Figures 6.13a and 6.13b respectively. From Figure 6.13a, the maximum permissible gain to maintain system stability is 0.0040 rad/volt or 0.23 deg/volt. The optimal value of the gain is about 0.001 to 0.0017 rad/volt or 0.057 to 0.100 deg/volt.

From Figure 6.13b, the maximum permissible gain to maintain stability in inductive mode is 0.0114 rad/volt or 0.653 deg/volt. The optimum value of the gain at this operating state is 0.0014 to 0.0020 rad/volt, or 0.080 to 0.115 deg/volt.

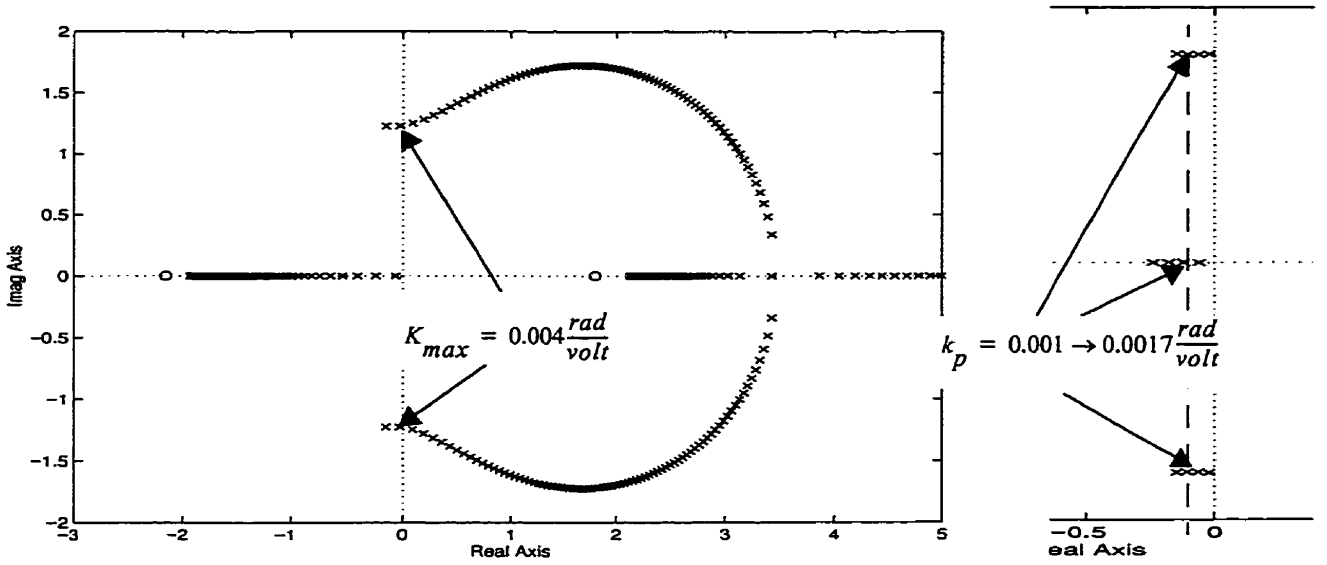


Figure 6.13a Root locus associated with dc voltage when compensating system operates in capacitive mode

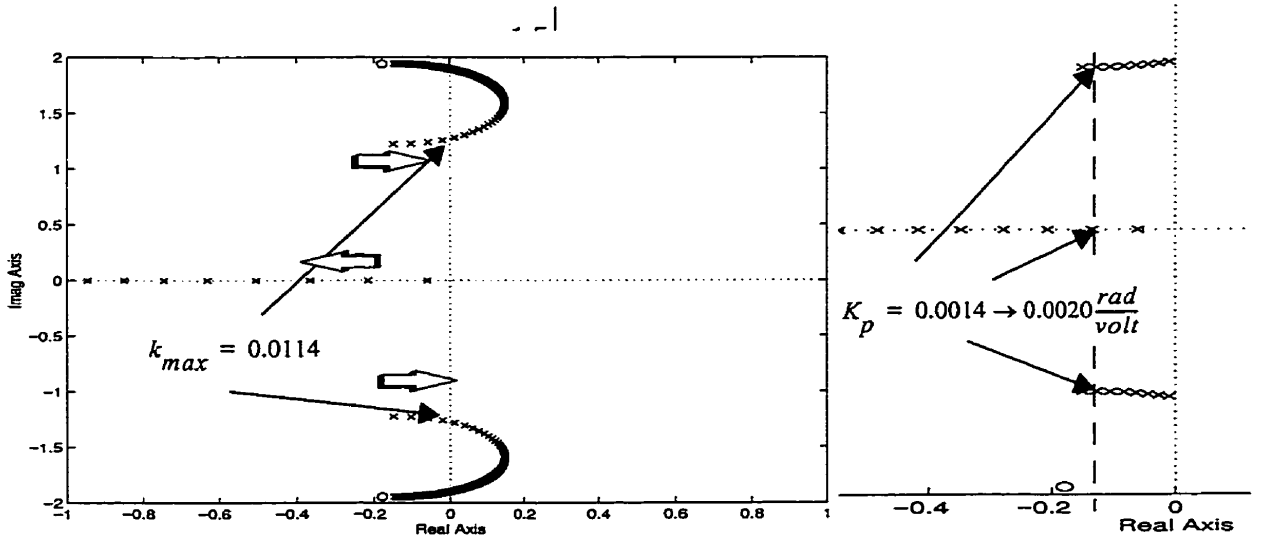


Figure 4.12 Root locus associated with dc voltage when compensating system operates at inductive mode

6.5.2 Experimental and Analytical Results

The closed-loop dynamic behaviour of the inverter-based compensator are depicted in Figure 6.14, 6.15 and 6.16, for different values of the feedback gain. The figures illustrate the response of the compensator to a step change from inductive to capacitive mode as well as from capacitive mode to inductive mode. Both the response associated with the linearized dynamic model and the experimental prototype depicted.

Clearly the dynamic response is better than in the open-loop case. With the increased feedback gain, the compensating system responds more quickly in the order of a few cycles when the gain is increased to 0.15 deg/volt. However, when the gain is increased beyond a certain value (such as 0.15 deg/volt), the response time cannot be reduced. This is consistent with the root locus analysis.

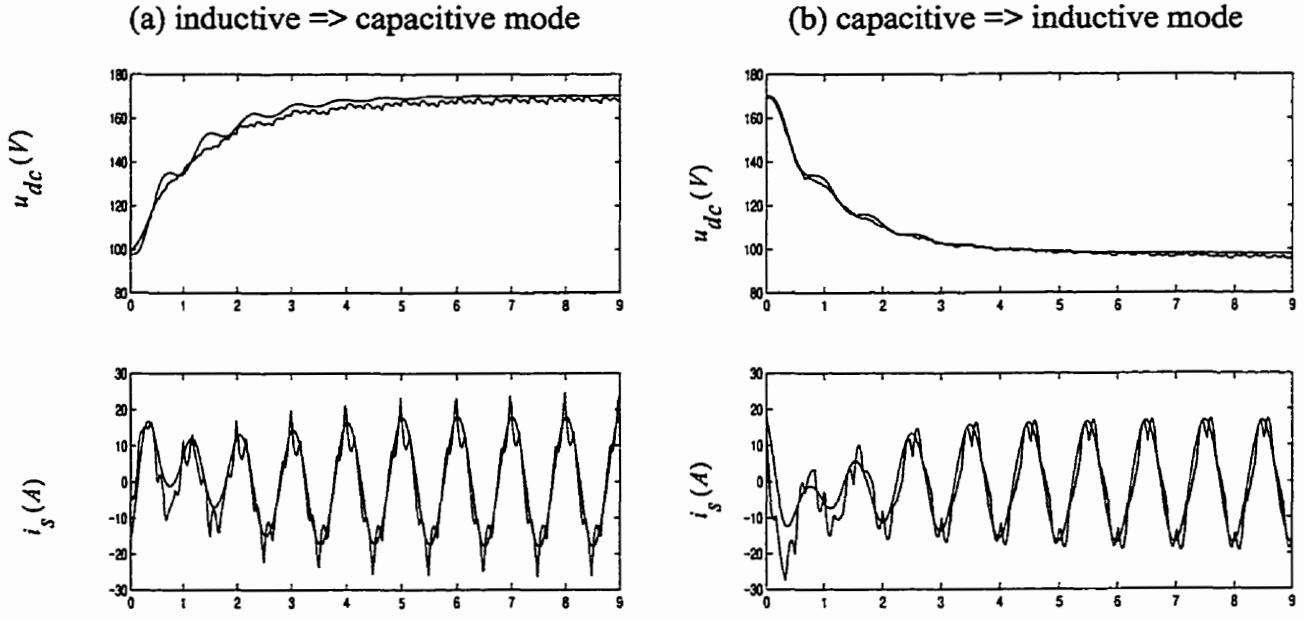


Figure 6.14 Closed-loop dynamic of compensator (feedback gain K = 0.10 deg/volt)

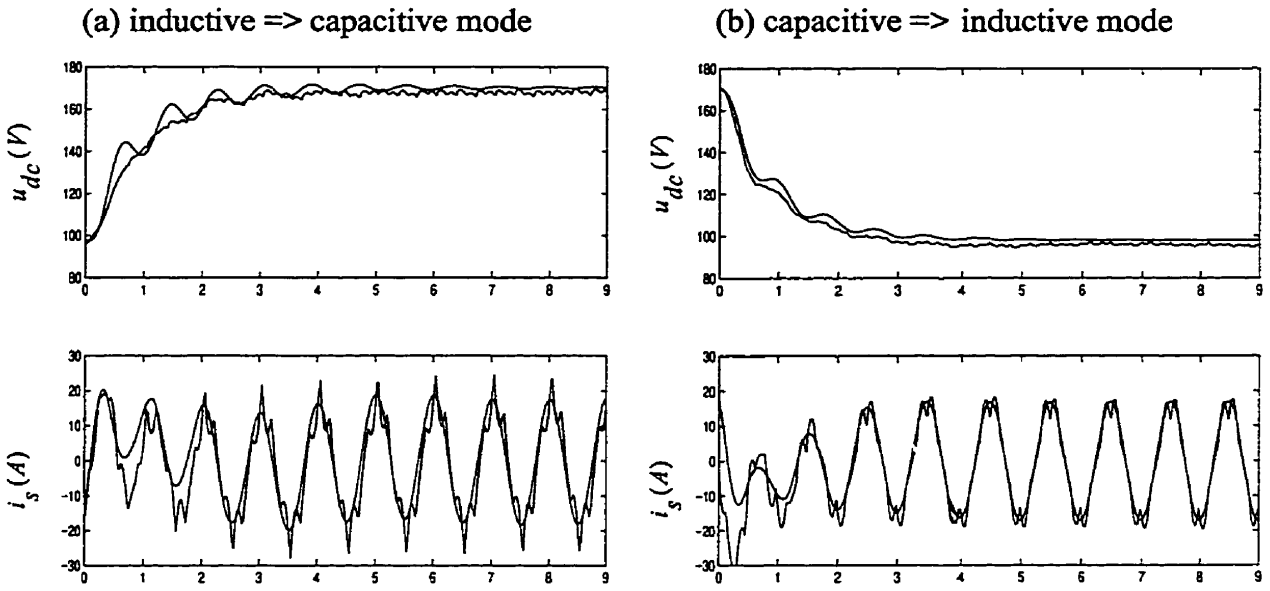


Figure 6.15 Closed-loop dynamic of compensator (feedback gain K = 0.15 deg/volt)

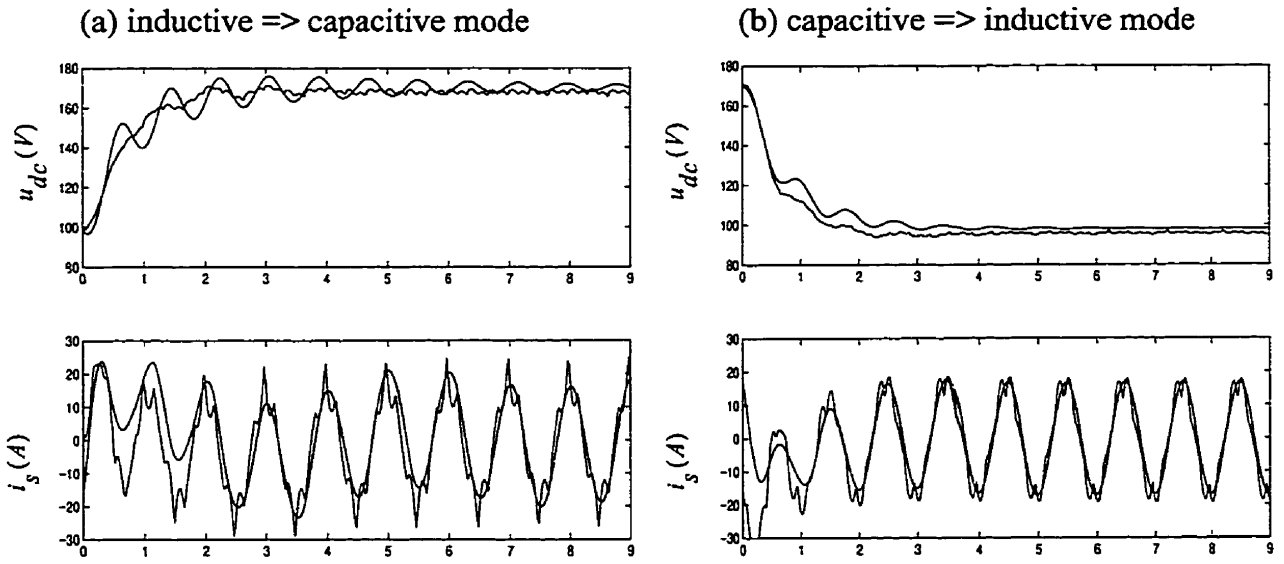


Figure 6.16 Closed-loop dynamic of compensator (feedback gain K = 0.20 deg/volt)

Chapter 7.

Conclusion and Future Work

7.1 Conclusion

Inverter-based compensation holds the promise of effective compensation of dynamically varying loads. This thesis presents some aspects of the modelling, analysis and implementations of DSP-based switching and control strategies for a prototype compensator.

The stationary and dynamic behaviour of the inverter-based compensator operating with block firing has been characterized in this study. The approximate model of system represents very well the fundamental frequency behaviour over the operating range of interest. The experimental results suggest that the loss component of the inductive coupling along with the switching losses, can be approximately represented by an equivalent resistance.

Various switching strategies have been studied for the elimination of selected low-order harmonics. The performance and implementation of these switching schemes are compared. Feedforward control based on the approximate model is also discussed. Piecewise linearization has been

proved to be an easy and effective measure to realize a feedforward control of the compensator dc voltage. Feedback control, can further reduce steady-state error. Furthermore, the experimental results show that the feedback control can improve the response of the system, and hence improve the dynamic behaviour of the compensator.

The stability analysis is concerned with achieving a satisfactory compromise between stability and performance. The gain is optimized by using root locus to improve the system response time to within a few cycles.

In addition, the studies verify through experimental implementations that software controlled switching strategies can effectively eliminate selected low-order harmonics. SHE is an attractive solution in comparison to the complicated PWM technique, demonstrating that SHE is a solution for harmonic control in the compensation of low-voltage loads.

7.2 Future Work

Future work for this project is recommended as follows:

1. Construct an external feedback control on the voltage or current of network. For the control of low-voltage load compensation, the system current feedback signal is preferred. We might build function blocks in DSP controller to handle the on-line real-time with the analysis of the data to make decisions regarding gating of the inverter, at the objective of both compensating the system and eliminating harmonics.

2. To improve the harmonic profile of the compensator current, switching schemes with additional elimination of harmonics are to be studied and implemented. A low-pass filter is suggested to be used in the prototype to suppress the higher-order harmonics.

3. Investigation of a multi-level IGBT inverter-based compensator to obtain higher compensating ratings, and improved harmonic performance. The studies will focus on the control of the neutral point voltage.

References

[1] J. Sun, S. Beineke, and H. Grotollen, "Optimal PWM Based on Real-Time Solution of Harmonic Elimination Equations", IEEE Transaction on Power Electronics, Vol. 11, No. 4, July 1996

[2] Y. Zhuang, R. W. Menzies, O. B. Nayak and H. M. Turanli, "Dynamic Performance of a Statcon at an HVDC Inverter Feeding a Very Weak AC System", IEEE / PES Summer Meeting, July 23 -27, 1995.

[3] H. Patel and R. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I -- Harmonic elimination," IEEE Trans. Industry Application, Vol. IA-9, No. 3, pp. 310 - 317, May/June 1973

[4] P. Enjeti and J. Lindsay, "Solving nonlinear equations of harmonic elimination PWM in power control," Electron. Lett., Vol. 23, No. 12, pp.656 -657, June 4 1987.

[5] Q. Jiang, D. Holmes, and D. Giesner, "A method for linearising optimal PWM switching strategies to enable their computation on-line in real-time," in Conf. Proc. 1991 IEEE Indus try Applications Society Ann. Meet, Oct. 1991, pp.819 - 825.

[6] R. Chance and J. Taufig, "A TMS320c10 based near optimized pulse width modulated wave form generator," in Conf. Proc. 1988 IEEE Industry Applications Society Ann. Meeting, Oct. 1993, pp. 903 - 908.

[7] IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters, Approved by IEEE standards Board on December 20, 1979

[8] G. Franklin, J. Powell and A. Emami-Naeini, Feedback Control of Dynamic Systems (Reading, Massachusetts: Addison-Wesley, 1986).

[9] R. W. Menzies and Y. Zhuang, "Advanced Static Compensation Using GTO Thyristor Inverter", IEEE Transaction on Power Delivery, 1995

[10] Brian K. Perkins, "Dynamic Modelling of an Inverter-Based Compensator", to be presented at IEEE / PES Conference, June 1999

[11] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, "Principles of Power Electronics", ISBN 0-201-09689-7, 1991

[12] S. Sanders, J. Noworolski, X. Liu and G. Verghese, "Generalized Averaging Method for Power Conversion Circuits", in IEEE Power Electronics Specialists Conference (PESC), San Antonio, June 1990, pp. 333-340.

[13] TMS320C3x User's Guide, Texas Instruments, Houston, TX, July 1991.

[14] Matlab Version 5 User's Guide

[15] PSCAD User's Manual, Manitoba HVDC Research Centre, Winnipeg, MB,

[16] IGBT Module Applications and Technical Data Book, Powerex, Youngwood, Pennsylvania

Appendix A Inverter-Based Compensator Construction Description

A1. Overview

The compensator is constructed with a three-phase voltage-source-inverter (VSI) comprising three dual IGBT modules (half-bridge configuration), a dc capacitor, three single-phase reactors coupling each half-bridge of the inverter connected to the network, and two busbars connecting the inverter dc side with the capacitor. The dc capacitor provides sufficient energy storage to stabilize the dc voltage for supplying the inverter. Furthermore, as the dc capacitor feeds the inverter through busbars of minimal inductance, it also serves as a snubber, and thereby reduces the amount of components in the system. The IGBT modules are mounted on aluminium heatsinks for thermal management. A fan for forced-air cooling can also be readily mounted on the inverter module.

A2. The Insulated Gated Bipolar Transistor

With increasing voltage ratings, insulated gate bipolar transistors (IGBTs) are being used in high-power applications. The IGBT is simple to turn on and off from the gate and does not require any inductive turn-on or capacitive turn-off snubbers within the usual application power and frequency ranges.

Each IGBT module consists of two IGBT transistors in a half-bridge configuration with a reverse-connected super-fast recovery free-wheel diode for each transistor. All components and interconnects are isolated from the heat sinking baseplate, offering simplified system assembly and thermal management.

A3. Gate Driver Circuit

IGBTs require gate voltage signal in order to establish collector to emitter conduction or non-conduction. We choose Powerex M57959L IGBT driver modules with TTL compatible input interface. M57959L is a hybrid integrated circuit designed for driving n-channel IGBT modules in any gate-amplifier application. This device operates as an isolation amplifier for these modules and provides the required electrical isolation between the input and output with an opto-coupler. Short circuit protection is provided by a built in desaturation detector. A fault signal is provided if the short circuit protection is activated.

The gate driver circuit associated with a single IGBT module is depicted in Figure A1. The $\pm 15\,V$ power source is provided by an isolated DC/DC step-up converter (Calex 5D15.033SIP) which is sourced by TTL voltage level. There are filtering capacitors connected between the positive and negative outputs and the isolated ground. The input TTL switching levels are coupled to the isolated side of the gate driver which generates gating signals to drive the IGBTs.

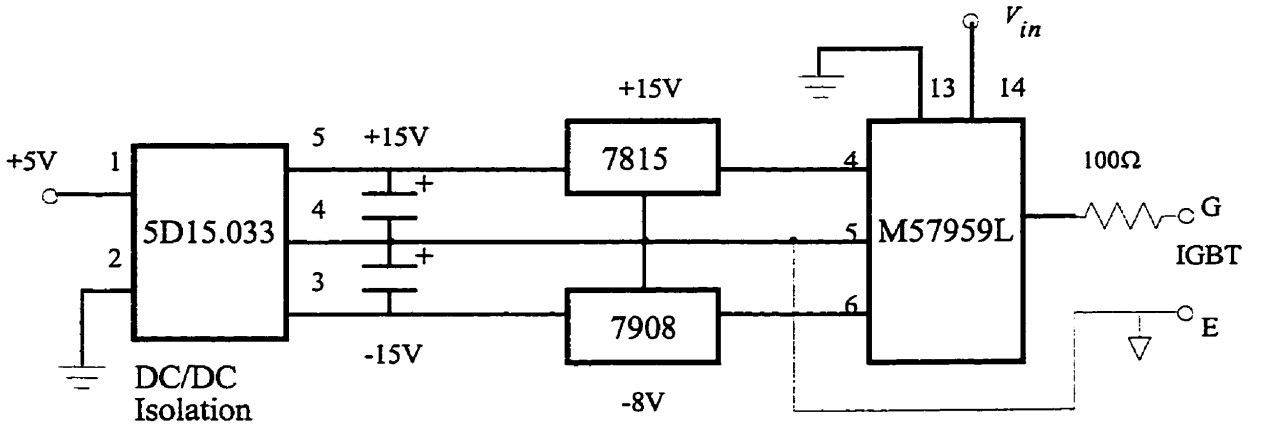


Figure A1 IGBT gate driving circuits

A4. Phase-Locked-Loop and Interrupt Generator

The solution to the reference phasor problem is to make use of the phase-locked-loop (PLL)

synchronization circuit. A PLL essentially locks on to the fundamental frequency component of the system voltage producing reference pulses with respect to zero crossings of this reference voltage. This technique will provide the reference phasor for the controls which is locked onto fundamental frequency component of the system voltage.

The synchronization circuit is made up of the following components

- CMOS components:

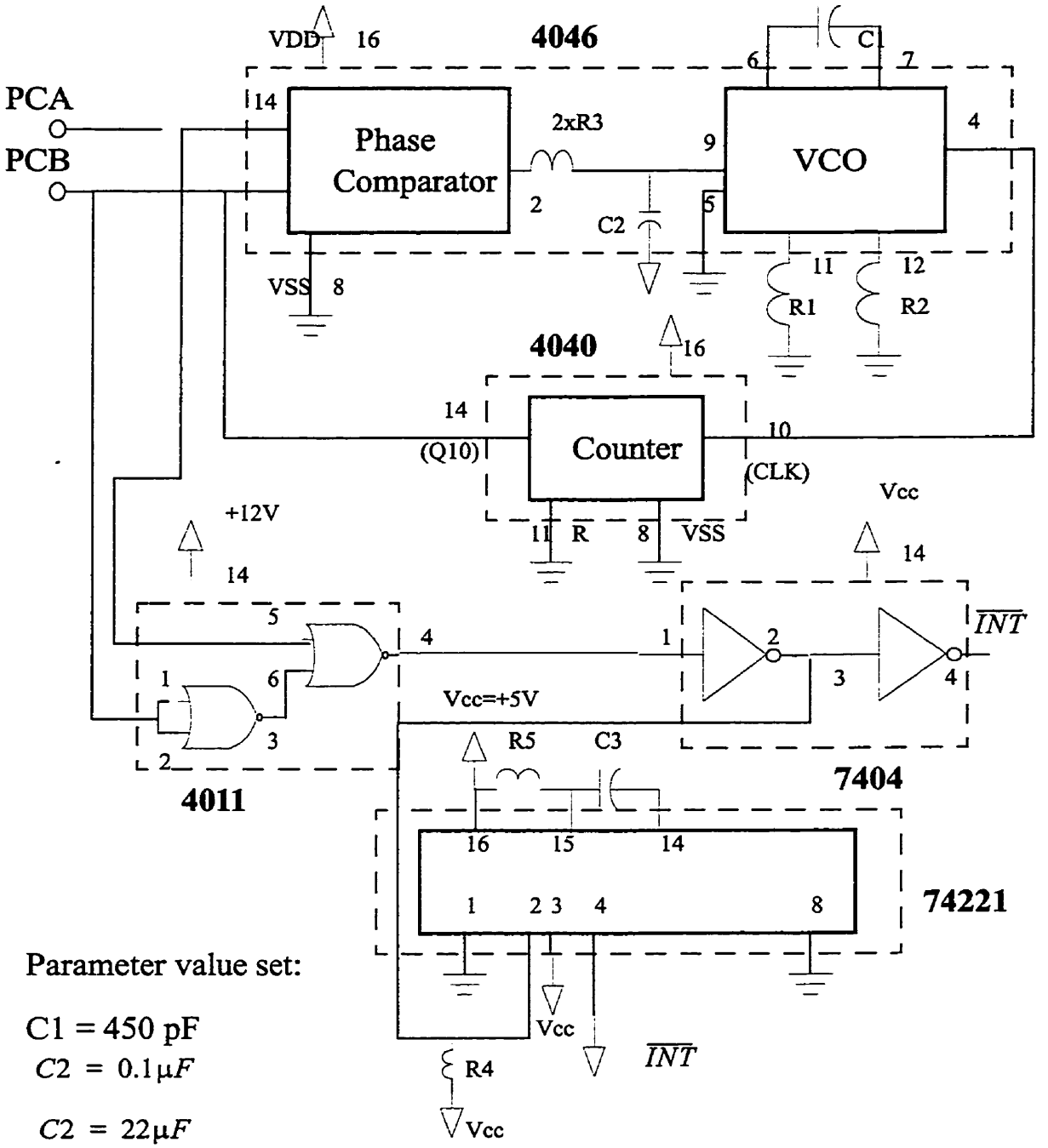
Motorola MC14046B (PLL), MC14040B (12-bit binary counter), MC14011B (quad 2-input NAND gate),

- TTL components:

Texas Instruments SN74LS04 (hex inverter), SN74221(dual monostable multivibrators with Schmitt-trigger inputs)

- Other passive components

The main function chip MC14046 phase-locked-loop contains two phase comparators and a voltage-controlled oscillator (VCO). The SN74221 has its outputs independent of further transitions of inputs once triggered, which is used to generate a stable interrupt. The synchronization circuit schematic is shown in Figure A2.



Parameter value set:

C1 = 450 pF

$C2 = 0.1\mu F$

$C2 = 22\mu F$

$R_1 = 44k\Omega$ $R_2 = 680k\Omega$ $R_3 = 512k\Omega$ $R_4 = 1.5k\Omega$ $R_5 = R_4 /2$

Figure A2 Schematic of synchronization circuit

A5. Digital Signal Processor Control

In the past, control systems for power electronics used only analog circuitry or simple micro-controller/microprocessor implementations. However, the growth of digital signal processing (DSP) technology has made digital control theory a reality. Figure A3 depicts a block diagram of a generic digital control system using a DSP, along with an analog-to-digital converter (ADC) and a digital-to-analog converter (DAC).

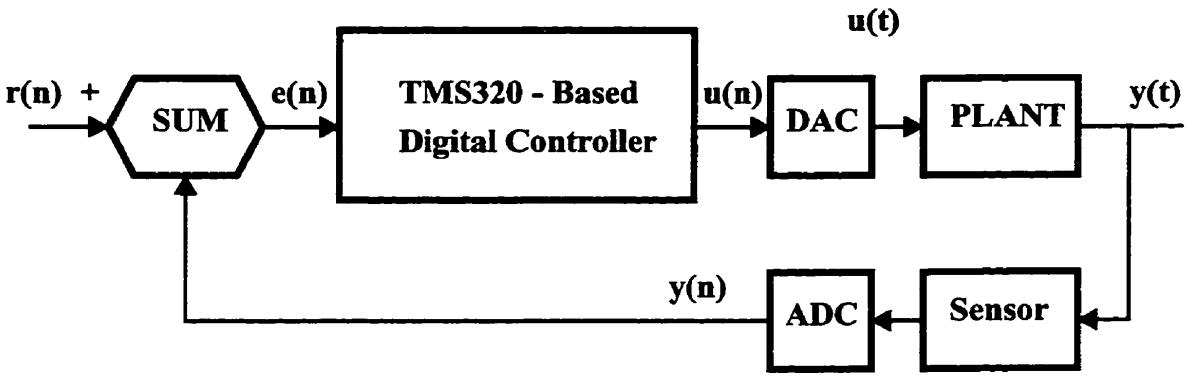


Figure A3 Block diagram of a generic digital control system using a DSP

In a DSP-based control system, the control algorithm is implemented via software. No component aging or temperature drift is associated with digital control systems. Additionally, sophisticated algorithms can be implemented and easily modified to upgrade system performance.

Texas Instruments (TI)'s TMS320c30 DSP have facilitated the development of high-speed digital control in power electronic applications. Dynamically changing network conditions demand that compensators should response very fast, thus the controller must analyse various signals acquired from the system and make decisions very quickly. We will introduce the DSP details below.

A5.1. Introduction of TMS320C30

The TMS320C30 digital signal processor (DSP) is a high-performance CMOS 32-bit floating-point device in the TMS320 family of single-chip digital signal processors (refer to Figure A4). The TMS320c30 can perform parallel multiply and arithmetic logic unit (ALU) operations on integer of floating-point data in a single cycle. The processor also processes a general -purpose register file, a program cache (64x32), dedicated auxiliary register arithmetic units (ARAU), internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time (60 ns).

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, two external interface ports, two timers, two serial ports, and multiple interrupt structure.

A5.2 DSP Interface Configuration

TMS320C30 peripherals are controlled through memory-mapped registers on a dedicated peripheral bus. This peripheral bus is composed of a 32-bit data bus and a 24-bit address bus. This peripheral bus permits straightforward communication to the peripherals. The peripherals include two timers and two serial ports.

A5.2.1 Timers

The two timers are general-purpose, 32-bit, timer/event counters, with two signalling modes and internal or external clocking. We use an internal clock to control the waveform of the inverter output while the other is used to time data acquisition.

A5.2.2 Serial Port

The TMS320C30 has two totally independent bidirectional serial ports. Both serial ports are identical, and there is a complementary sets of control registers in each one. Each serial port can

be configured to transfer 8, 16, 24, or 32 bits of data per word simultaneously in both directions. The clock for each serial port can originate either internally, via the serial port timer and period registers, or externally, via a supplied clock. A continuous transfer mode is available, which allows the serial port to transmit and receive any number of words without new synchronization pulses.

Eight memory-mapped registers are provided for each serial port:

- Global-control register
- Two control register for six serial I/O pins
- Three receive/transmit timer registers
- Data-transmit register
- Data-receive register

The global-control register controls the global functions of the serial port and determines the serial-port operating mode. Two port control registers control the functions of the six serial port pins. The transmit buffer contains the next complete word to be transmitted. The receive buffer contains the last complete word to be transmitted. Three additional registers are associated with the transmit/receive sections of the serial-port timer. A serial port has the following interrupt sources: transmit / receive timer interrupt, transmitter / receiver interrupt.

A5.2.3 Expansion Bus Interface

The TMS320C30's expansion bus interface provides a second complete parallel bus, which can be used to implement data transfers concurrently with (and independently of) operations on the primary bus. The expansion bus comprises two mutually exclusive interface controlled by the $\overline{MSTRB}$ and $\overline{IOSTRB}$ signals, respectively.

A5.2.4 A/D Converter Interface

A/D and D/A converters are commonly required in DSP systems and interface efficiently to the I/O expansion bus. These devices are available in many speed ranges and with a variety of features. While some might require one or more wait states on the I/O bus, others can be used at full speed.

Figure A4 illustrates a TMS320C30 interface to an Analog Devices AD1678 analog-to-digital converter. The AD1678 is a 12-bit, 5-μs converter that allows sample rates up to 200 kHz and has an input voltage range of 10 volts, bipolar or unipolar.

In this application, the converter's chip select is driven by XA12, which maps this device at 804000h in I/O address space. Conversions are initiated by writing any data value to the device, and the conversion results are obtained by reading from the device after the conversion is completed. The buffers used here are 74LS244s that can isolate the converter outputs from the DSP. When a conversion cycle is completed, the AD1678's EOC output is used to generate an interrupt on the TMS320C30 to indicate that the converted data can be read.

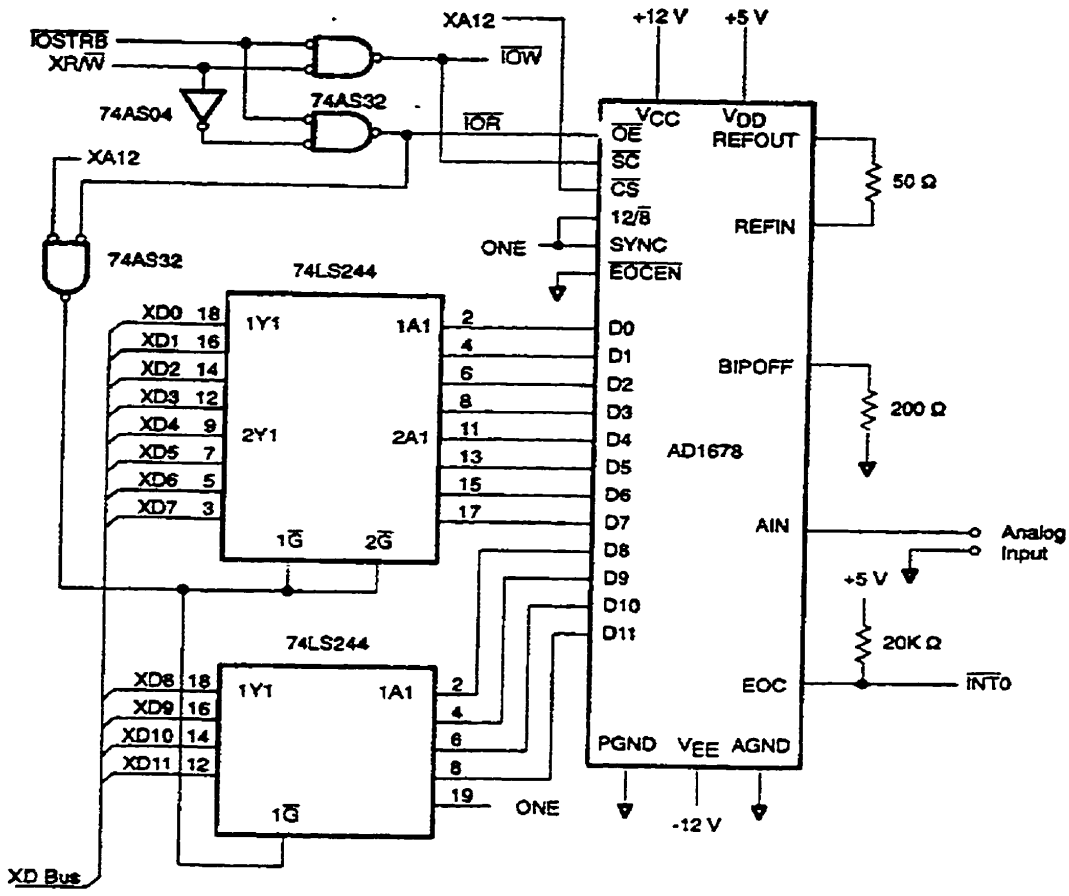


Figure A5 DSP interface to AD 1678 Analog - to -Digital Converter

Appendix B Measurement Data for Feedforward Control

δ	U_{dc}	δ	U_{dc}	δ	U_{dc}
-5	84	-1.5	123	2	147
-4.5	89	-1	127	2.5	151
-4	97	-0.5	130	3	158
-3.5	105	0	133	3.5	163
-3	110	0.5	137	4	170
-2.5	117	1.0	141	4.5	176
-2	120	1.5	144	5	183

Table B1 Measurement of δ ~ U_{dc} for BSS

δ	U_{dc}	δ	U_{dc}	δ	U_{dc}
-5	98	-1.5	133	2	153
-4.5	105	-1	135	2.5	156
-4	110	-0.5	138	3	160
-3.5	116	0	140	3.5	165
-3	122	0.5	143	4	170
-2.5	127	1.0	145	4.5	176
-2	130	1.5	148	5	182

Table B2 Measurement of δ ~ U_{dc} for SHE-5

δ	U_{dc}	δ	U_{dc}	δ	U_{dc}
-5	105	-1.5	136	2	153
-4.5	112	-1	138	2.5	156
-4	117	-0.5	140	3	161
-3.5	123	0	142	3.5	165
-3	128	0.5	144	4	170
-2.5	133	1.0	147	4.5	179
-2	134	1.5	150	5	188

Table B3 Measurement of δ ~ U_{dc} for SHE-5-7B