Active Gate Drive Based Hybrid MVDC Circuit Breaker with a Modular Architecture for Flexible Voltage and Current Ratings

by

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Abstract

MVDC networks present an effective means for integrating renewable-based Distributed Generators into the power network. Protection of Medium Voltage Direct Current (MVDC) networks presents significant challenges, including the absence of natural zero crossings, rapid fault current rise, and a lack of MVDC-compatible protection devices, standards, guidelines, and practical experience.

Solid-state DC Circuit Breakers (DCCBs) have emerged as an attractive protection solution for DC networks, offering fast and reliable fault isolation. Seamless integration of DCCBs into MVDC networks is challenging due to the diverse voltage and power levels and varying network architectures. Furthermore, the limited current and voltage capability of semiconductor devices limits the full integration of solid-state DCCBs for MVDC applications. Series and parallel-connected IGBT arrays can be employed to match the required current and voltage levels. However, with passive gate drives, devices may fail due to non-homogeneous current and voltage distribution across IGBTs. Closed-loop Active Gate Drives (AGDs) offer a solution to overcome these challenges.

This research aims to develop an AGD scheme that drives IGBTs with status feedback, allowing them to follow a set current/voltage trajectory during IGBT switching. Hybrid Circuit Breaker (HCB) architecture, based on standardized Active Switch Modules (ASMs), is proposed as a flexible protection solution for MVDC networks.

Steady-state current imbalances in parallel-connected IGBTs can lead to thermal runaway conditions and degrade the IGBTs. Conventional steady-state current balancing methods rely on device matching and passive gate drive concepts, which are inadequate for modern MVDC applications. The proposed Active Current Balancing (ACB) scheme actively regulates the gate-

drive voltage of each device based on measured current deviations, enabling precise control of the static operating point.

The integrated operation of ACB-AGD schemes within a unified framework provides a practical and scalable solution for voltage and current management in MVDC-DCCB applications. Experimental validation on a unidirectional DCCB prototype confirms that the integrated ACB-AGD system maintains stable switching behavior while effectively correcting steady-state current imbalance.

Collectively, the proposed ACB, AGD, and modular HCB architecture establish a scalable protection framework capable of delivering enhanced dynamic switching performance, steady-state current sharing, and secure fault-interruption capability for next generation MVDC networks.

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I am profoundly grateful to my parents, whose unwavering support, sacrifices, and belief in my work have guided me through every step of this journey. Their strength and encouragement have been the foundation on which this achievement stands.

Dedications

To my loving wife and parents

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List of Abbreviations

ACB	Active Current Balancing
ADC	Analog to Digital Converter
AGC	Active Gate Clamping
AGD	Active Gate Drive
ASM	Active Switch Module
CCS	Current Commutation Switch
DAC	Digital to Analog Converter
DCCBs	DC Circuit Breakers
DPT	Double Pulse Test
DSP	Digital Signal Processor
ESS	Energy Storage System
EV	Electric Vehicle
HCB	Hybrid Circuit Breaker
HVDC	High Voltage DC
IGBT	Insulated Gate Bipolar Transistor
LDO	Low Dropout
LVDC	Low Voltage DC
MVDC	Medium Voltage DC
MB	Main Breaker
MS	Mechanical Switch
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
PCB	Printed Circuit Board
PI	Proportional-Integral
PTC	Positive Thermal Coefficient
PV	Photovoltaic
RES	Renewable Energy Sources
SOA	Safe Operating Area
SSCB	Solid State Circuit Breaker
TIV	Transient Interrupt Voltage

Chapter 1: Introduction

1.1 Background and Research Motivation

The efficient integration of Renewable Energy Sources (RESs) is a key focus in modern power system research. Due to problems stemming from increasing energy demand and reliance on conventional fossil fuel-based energy sources, considerable resources and effort have been devoted to integrating cleaner energy sources, such as solar Photovoltaic (PV), into the energy mix. Significant advancements in power electronics have led to the widespread adoption of DC loads and power electronic converters, which are prevalent in various applications at different levels [1], [2]. In this context, DC distribution systems are emerging as an attractive power system solution for efficiently integrating RESs. Furthermore, DC distribution networks facilitate flexible power flow and increase network reliability [2], [3].

The commercial unavailability of DC fault-interrupting devices that can meet the safe operating time and current limits of DC systems poses a significant challenge [1], [4], [5], [6]. Fast-acting DC Circuit Breaker (DCCB) designs have gained popularity recently for protecting DC networks. These DCCBs offer promising DC fault interruption solutions with high-speed fault current breaking capability [7], [8], [9], [10]. Smart DCCBs with self-fault detection and active current limitation capabilities reduce the additional sensory and communication requirements while minimizing network outages [11]. However, the lack of flexibility to serve across different power levels, low technology readiness levels, and high costs associated with these breaker designs preclude the widespread use of these technologies [1], [4], [7].

Modern DCCB implementations increasingly rely on power semiconductor devices, such asIGBTs) and Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), due to their

arcless interruption and fast switching. Semiconductor device-based DCCBs interrupt the current faster than mechanical circuit breakers [1], [3], [12]. However, due to the limitations of semiconductor devices current and voltage capabilities, the application of DCCBs in medium-voltage applications remains challenging. For medium-voltage operation, DCCBs are required to handle currents of up to several kiloamperes and voltages of several tens of kilovolts, which exceed the ratings of single IGBTs available [13], [14]. Furthermore, IGBTs employed in Hybrid Circuit Breakers (HCBs) are subjected to high fault currents and Transient Interrupt Voltage (TIV) [3], [11], [15], [16], [17]. Hence, multiple IGBT units must be arranged in series and parallel to accommodate the required current and voltage rating [12], [18], [19]. However, this necessitates voltage and current balancing between devices, as well as increased control complexity [15], [19], [20]. An Active Gate Drive (AGD) scheme, which controls di/dt and dv/dt during device turn-on and turn-off, allows the balance of voltage and current stress in the devices during dynamic switching [21], [22], [23]. With a controllable rate of change of collector current and voltage, an additional degree of freedom during IGBT switching can be achieved, allowing for dynamic voltage and current balance.

MVDC networks exhibit complex dynamic and transient responses to faults [24], [25]. The lack of a fast, reliable, and low-cost protection solution for DC networks is a significant barrier to their widespread adoption. A scalable breaker architecture that matches the network's current and voltage levels will provide a suitable solution to address this problem.

While current studies primarily focus on the dynamic performance of DCCBs during a fault event, the steady-state operation of semiconductor-based protective devices is also an important aspect [16], [26]. Design methodologies applicable to thermal design and steady-state current sharing haven’t been adequately explored in the literature. Evaluating the steady-state and

transient thermal characteristics of the DC circuit breaker is critical, as these thermal behaviours directly influence device stress, allowable current levels, and the overall reliability of the breaker during continuous operation and fast interruption events [26], [27].

Due to the limitations in the nominal current and thermal limits of semiconductor devices, ensuring steady-state current sharing and thermal integrity in parallel IGBTs is vital for the reliable operation of DCCBs. This motivates the need for a control approach to achieve steady-state current sharing, preventing device overstress and degradation while maintaining device thermal stability [1], [16].

The ability of the proposed schemes to operate in an integrated manner and enable a unified DC protection solution is a central consideration, as effective coordination among these mechanisms determines the overall responsiveness, reliability, and robustness of the proposed DCCB architectures.

1.2 Problem Statement

Due to their inherent advantages, MVDC networks are increasingly used across various applications, such as shipboard networks, MVDC collector grids, traction power networks, Electric Vehicle (EV) charging stations, and data center networks. Despite the advantages of DC networks, protection challenges stemming from the lack of reliable interruption equipment have hindered their widespread adoption.

The MVDC voltages range from 1.5 to 100 kV DC and tens of megawatts across various applications [28], [29]. This enables the use of varying technologies across both low- and high-voltage ranges, providing flexibility in selecting the required topology. Although several DC

breaker topologies have been proposed in the literature, they lack the scalability and flexibility needed to serve various applications involving different voltage and power levels [26], [30].

DC networks exhibit a rapid rise in fault current during converter capacitor discharge, necessitating equipment capable of detecting and interrupting faults quickly to prevent severe damage [3]. While semiconductor-based DCCBs offer a good solution for fast fault interruption, the limitations of semiconductor voltage and current ratings require series and parallel connections of semiconductor devices to match network fault levels. Conventionally, the problem of dynamic current and voltage balancing is achieved using snubbers and other passive balancing techniques [27], [31]. The snubber's performance can deteriorate over time, resulting in poor voltage sharing and device failure [15], [32]. Furthermore, significant IGBT derating increases the costs associated with DCCBs. Hence, there is a necessity for a reliable, low-cost solution to achieve dynamic current and voltage balance among semiconductor devices.

Achieving a stable, steady-state current sharing among parallel-connected IGBTs remains challenging due to inherent device mismatches and varying thermal conditions that change during continuous operation. These could lead to localized overheating and accelerated aging, compromising the reliability of the DCCB in steady-state operation [16], [33]. The conventional approach to addressing this challenge is to heavily derate the IGBTs, a measure that significantly increases the device count and the cost of breaker assemblies. This drives the need for a dedicated control approach to ensure reliable steady-state current sharing and thermal stability.

1.3 Research Objectives

The primary objective of the proposed research is to design and develop a gate-drive technology for DC circuit breaker applications that enables higher-voltage, higher-current switching through cascaded and parallel arrangements of semiconductor devices. The gate-drive technology can be employed to develop a flexible MVDC circuit breaker architecture with reliable fault protection capability for MVDC network protection.

The following objectives are to be achieved under this:

1) To develop AGD technologies for dynamic voltage and current balancing in IGBTs during switching.
2) To develop an Active Current Balancing (ACB) scheme that enables steady-state current sharing between parallel-connected IGBTs, which can work in coordination with the proposed AGD scheme.
3) To develop a scalable, standardized DCCB architecture with unified gate drive technology to achieve both steady state and dynamic voltage and current balancing, while ensuring thermal stability.
4) To evaluate the thermal performance of the proposed DCCB architecture under steady-state and transient operating conditions.

1.4 List of Publications

- S. Jayamaha, C. N. M. Ho and A. Rajapakse, "Parallel/Series Connected Standardized Active Switching Modules for High Power DCCBs in MVDC Networks", *in IEEE Transactions on Power Electronics, vol. 39, no. 8, pp. 9602-9613, Aug. 2024.*

- S. Jayamaha, C. N. M. Ho and A. Rajapakse, "Active Gate Control Scheme for Current Balancing in Parallel Connected IGBTs for DCCB Applications", *manuscript in preparation for submission to IEEE Transactions on Industrial Electronics.*
- S. Jayamaha, C. Ho and A. Rajapakse, "Active Current Balancing Scheme for Steady-State Operation of Parallel IGBTs in Hybrid Circuit Breakers", IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024, pp. 1-6.
- S. Jayamaha, C. N. Man Ho and A. Rajapakse, "Electro-Thermal Design: Standardized Hybrid DC Breaker Architecture for Scalable Operation in MVDC Networks", 2024 IEEE Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 2024, pp. 707-713.
- D. K. J. S. Jayamaha, K. K. M. Siu, C. N. M. Ho and A. D. Rajapakse, "Design and Development of Modular Hybrid DC Breaker Scheme for DC Distribution Systems", 2021 IEEE Energy Conversion Congress and Exposition (ECCE), Vancouver, BC, Canada, 2021, pp. 5920-5926.

1.5 Thesis Outline

This thesis is organized into six chapters, each presenting a distinct contribution of the research. The overall structure of the thesis is outlined below.

Chapter 1 presents the background necessary to understand the core concepts of the thesis. It defines the research problem, reviews conventional approaches to the identified challenges, and outlines the objectives and key contributions of this work.

Chapter 2 presents an extensive review of the existing literature on topics central to this research. It examines MVDC applications, DC circuit-breaker technologies, conventional voltage and current balancing techniques, and active gate-drive methods used in power semiconductor devices. This chapter establishes the theoretical foundation for developing the AGD-based DCCB solution proposed for MVDC networks.

Chapter 3 details the development of the AGD technology, including its experimental validation and the characterization of the proposed AGD scheme. This chapter also presents the small-signal modeling formulation for assessing the stability of the proposed controller and introduces the Active Switch Module (ASM) concept.

Chapter 4 presents the ASM-based HCB architecture as a scalable protection solution for a wide range of MVDC applications. ASM-based HCB prototype development and experimental validation are discussed in this section. Furthermore, steady-state and transient thermal characterization of HCBs is evaluated in this chapter.

Chapter 5 examines the necessity for steady-state current balancing and the impact of Positive Thermal Coefficient (PTC) on the natural balancing of current. This study presents a detailed analysis of the Active Current Balancing (ACB) scheme for steady-state current sharing among parallel IGBTs. Characteristic equations governing the ACB control approach are derived, and the theoretical framework for assessing the stability of the control loops is presented. A combined ACB-AGD scheme featuring time-scale separation of the two control loops to develop a unified control scheme for series-parallel-connected IGBTs in MVDC circuit breaker applications is further examined in this chapter. Experimental studies to validate the combined operation of the two controllers are presented.

Chapter 6 summarizes the key conclusions drawn from the research and its findings. It highlights the main contributions of this research. This chapter also discusses potential future work that could extend and build upon the findings of this thesis.

Chapter 2: Literature Review

2.1 MVDC Applications and Governing Standards

MVDC networks support a diverse range of applications in modern power systems, and a growing body of technical standards and regulatory frameworks guides their development. Figure 2. 1 shows the typical voltage levels used in DC transmission and distribution systems, ranging from High Voltage DC (HVDC) to Low Voltage DC (LVDC), along with their corresponding applications. MVDC is typically deployed in the 1.5 kV – 100 kV range for power transfer levels ranging from a few MW to several hundred MW, primarily for DC distribution networks and large-scale industrial or renewable energy interconnections.

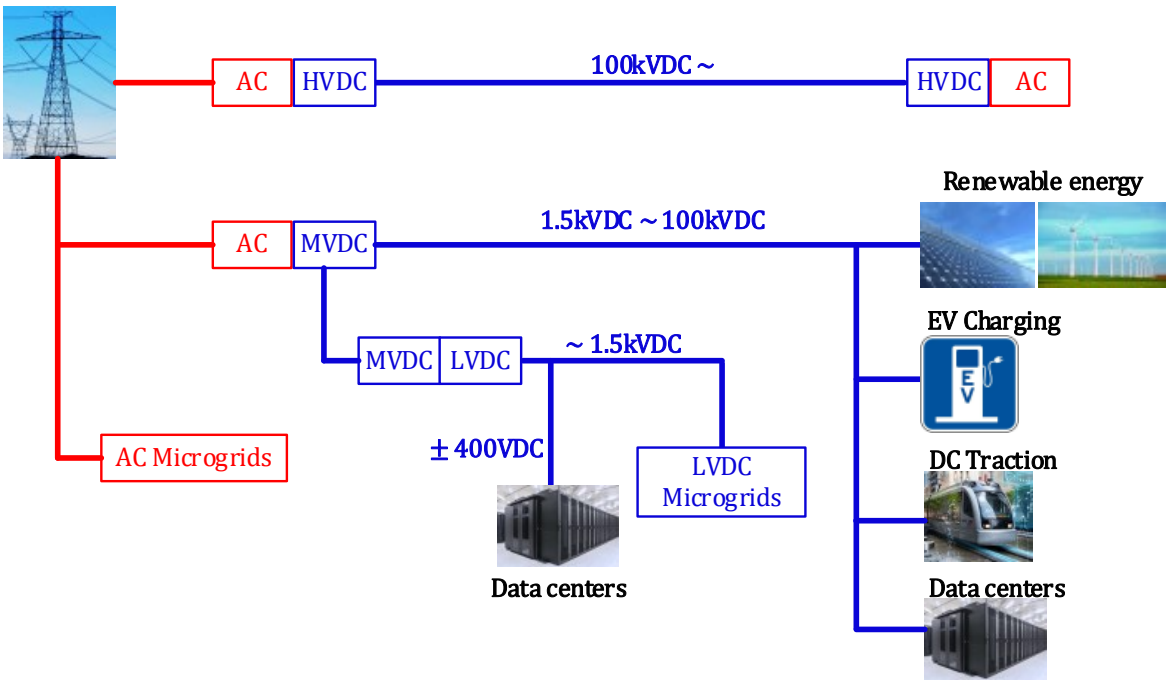


Figure 2. 1: An illustration of various DC voltage levels of applications [28].

2.1.1 MVDC Applications

MVDC networks are increasingly employed across various applications due to their inherent advantages. The main benefits include fewer power conversion stages, reduced cable sizing requirements, enhanced controllability, and simplified integration of RES and energy storage systems. This section examines various applications for which MVDC networks are being utilized, as well as future trends.

2.1.1.1 Shipboard Power Systems

Shipboard electrical networks are transitioning from conventional AC power systems to DC power systems. The main reason is the easier integration of variable frequency drives and ESSs, which eliminates a conversion stage and reduces the weight and space required for the equipment. Zonal DC Networks are the preferred architecture for shipboard networks, and in case of a fault, the faulted zone is isolated from the network [1], [34], [35].

2.1.1.2 MVDC Collector Grids

Due to the increasing penetration of RESs into the energy mix, collector grids interconnecting several distributed energy sources, such as wind turbines and solar PVs, have gained prominence. MVDC collector grids offer several advantages, including reduced conversion stages, lower costs, and a smaller size. Furthermore, reducing the number of conversion stages increases power efficiency [35].

2.1.1.3 Traction Power Networks

MVDC has been widely employed in traction networks such as trams and railways, mainly due to the speed control capability of DC motors. Voltages up to 3kV are used in these networks. Active rectifier units are integrated into these networks, allowing seamless power transfer between these MVDC networks and the AC grid [35], [36].

2.1.1.4 MVDC Interface for Interconnecting AC Networks

Interconnection of several AC networks or distributed energy sources is challenging due to frequency differences, harmonics, phase differences, and protection limitations, such as short-circuit currents. However, DC networks decouple the AC interfaces and offer a solution for interfacing sections of AC networks [35].

2.1.1.5 MVDC in EV Charging Stations and Data Center Networks.

While MVDC networks serve as a platform for interconnecting renewable energy sources, high-power loads such as EV charging stations and Data centers can be powered through MVDC. By eliminating the AC-DC conversion stage, network efficiency is increased. Even though these networks are required to connect to the AC utility grid, they operate as standalone systems in most situations [35], [37].

2.1.2 MVDC Networks: Relevant Standards

Table 2.1 provides a summary of relevant standards for MVDC networks across various applications.

Table 2.1. Summary of relevant standards for MVDC networks

Standard	Description	Highlights
IEEE Std 1709-2018 [38]	IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships.	• Standard ratings of MVDC power networks, operating devices, and auxiliary equipment. • Recommendations for rated continuous and short circuit currents and grounding considerations. • MVDC testing should be in accordance with the approved test program based on IEEE Std 1662-2006, IEC 600092-350, and IEEE std 45-2002 • It is recommended that MVDC networks be based on Power Electronic Building Blocks (PEBBs), with each PEBB having its own control and protection capability.
IEC 61660 [39]	IEC standard- Short circuit currents in DC auxiliary	• *Part I* - Calculation of short circuit currents

	installations in power plants and substations	• *Part II* - Calculation of effects of short circuit current on equipment • *Part III* - Additional considerations in short circuit current calculations
IEEE C37.14-2015 [40]	IEEE Standard for DC (3200V and below) Power circuit breakers used in enclosures.	• Covers preferred ratings and testing requirements of enclosed DC circuit breakers having a rated maximum voltage up to 3.2 kV.
IEC TS 61936-2 [29]	IEC standard- Power installations exceeding 1.5 kV DC	• Standard rules for designing and developing electrical power installations in systems with nominal voltages above 1.5kV DC to provide safety and proper functioning.

2.2 DC Breaker Technologies and Challenges

2.2.1 DC Breaker Technologies

DC circuit-breaker technologies can be broadly classified into mechanical, solid-state, and hybrid designs, each offering distinct operating principles, interruption capabilities, and application constraints.

2.2.1.1 Mechanical DC Circuit Breakers

Due to the absence of natural zero crossings, like in an AC system, arc extinguishing does not occur naturally in mechanical DCCBs. Resonance circuits are used to create a current zero crossing in mechanical DCCBs. Mechanical DCCBs can be categorized based on the passive and active resonance circuits they utilize. Figure 2.2 (a) and (b) show mechanical DCCBs using passive and active resonance circuits, respectively [1].

The main advantages of mechanical DCCBs include high efficiency and low cost. However, compared with other DCCB technologies, mechanical DCCBs have slower response times and limited current-interruption capability [7], [8].

2.2.1.2 Solid State Circuit Breaker

Solid-state CBs can be used to protect DC networks, overcoming their slow response times. Si-based semiconductor switches such as IGBTs, IGCTs, GTOs, and MOSFETs are commonly used in Solid-state CBs (Figure 2.2 (c)) [7], [8], [19], [41]. The main drawbacks of solid-state CBs include high conduction losses, high implementation costs, cooling requirements, and the lack of galvanic isolation [13], [20].

2.2.1.3 Hybrid DC Breaker

While Mechanical DCCBs and SSCBs have inherent disadvantages, HCBs combine the two to achieve fast current breaking, high efficiency, low cost, arc-free current interruption, and galvanic isolation [11], [13], [41]. The HCB structure is illustrated in Figure 2.2 (d). While this structure has several variants, the basic operating principle remains unchanged. As shown in Figure 2.2 (d), HCB consists of 3 main parts: Mechanical Switch (MS), Current Commutation Switch (CCS), and Main Breaker (MB) unit [1], [14]. Under normal conditions, current passes through the MS and CCS. During the current interruption, the MB unit is turned on, and CCS is turned off to commutate the current from the main path to the MB path. MB continues to conduct current until MS is fully open and can withstand full voltage. When the MB is turned off, Metal Oxide Varistor (MOV) clamps TIV, providing a current path [15], [41].

Selecting a low conduction loss switch for the CCS is a key design criterion in HCB design. CCS only needs to generate a reverse voltage higher than the MB unit's on-state voltage drop. Hence, a low-voltage-rated switch can be selected. The speed of the HCB is mainly dependent on the speed of MS. Hence, fast-acting MS is required for HCB [1].

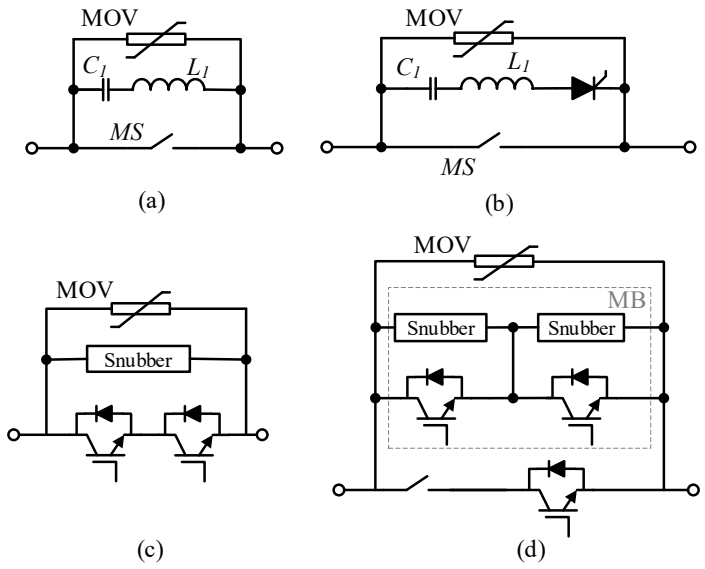


Figure 2.2: (a) Mechanical DCCB with passive resonance circuit, (b) Mechanical DCCB with active resonance circuit, (c) Solid-state CB (SSCB), (d) Hybrid CB (HCB) [1], [7], [8], [41].

2.2.2 DC Breaker Testing

Testing of DCCBs over the full range of operating conditions, both under normal and fault conditions, requires a source capable of sourcing short-circuit fault current at the rated voltage. Utilizing a power source capable of sourcing the test current and voltage is impractical. Several test apparatuses have been proposed in the literature for testing DCCBs under normal and fault conditions.

Utilizing a capacitor bank and a short-circuit switch for DCCB testing, as shown in Figure 2.3, is widely employed because it can produce high-current pulses for breaker testing [8]. However, this approach has limitations, including the inability to source current for a complete current-breaking cycle, to test the breaker's ability to transfer from normal operating conditions to fault conditions, and to assess the breaker's thermal characteristics under normal operating conditions.

A test circuit proposed in [42] to test the DCCBs at rated current and dynamically switch the pulse capacitor circuit to generate a high short-circuit current, thereby testing the DCCB's

fault-interruption capability, is shown in Figure 2.4. This circuit enables the insertion of a high-voltage pulse into the circuit while the DCCB is under nominal operating conditions, thereby emulating a short-circuit fault. Furthermore, this approach allows steady-state thermal testing of the DCCB.

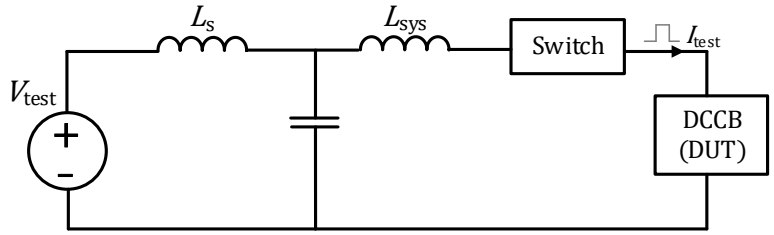


Figure 2.3: Circuit for short circuit testing of the DCCB [8].

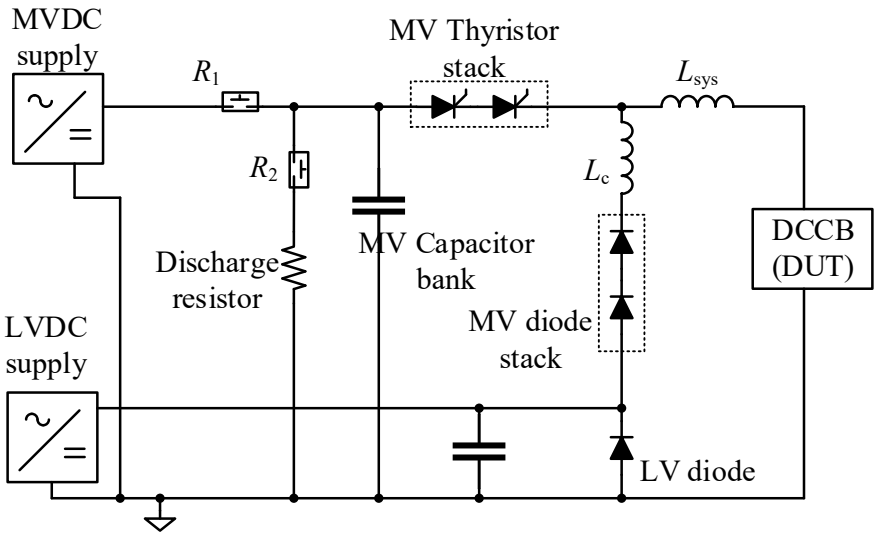


Figure 2.4: Modified short circuit test setup for both high voltage and current testing of the DCCB [42].

The inability to generate TIV for an extended period due to insufficient test capacity was a significant drawback of the previous test configuration. To provide sufficient stress for DCCB, a synthetic test method is proposed in [43] and illustrated in Figure 2.5. The parallel connection of two-level voltage sources ensures that the TIV amplitude and duration are more consistent with actual DC breaking.

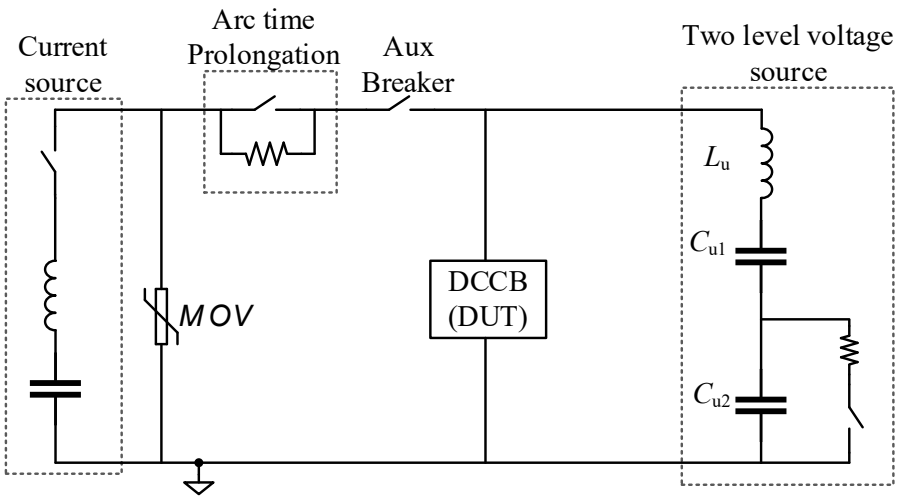


Figure 2.5: Modified short circuit test setup to generate TIV for DCCB testing [43].

2.2.3 DC Circuit Breaker Practical Challenges

While DC networks are gaining popularity due to their advantages over AC counterparts, DCCB technologies still face several challenges. The main challenge is the limitations of the current and voltage ratings of power semiconductor switches, such as IGBTs, MOSFETs, and SiC devices. This requires connecting and matching series and parallel devices to meet the current and voltage requirements of the MVDC networks [1], [9], [34].

Semiconductor devices incur significant conduction losses during steady-state operation of the DCCBs. Specialized cooling systems are required to dissipate the heat produced, which significantly increases the size and cost of the DCCBs [1], [2], [44].

Breaking high DC fault currents results in very high transient interrupt voltages, requiring large MOVs to absorb the energy. These MOVs are increasing the size and cost associated with DCCBs; furthermore, repeated current interrupting operations age the MOVs [1], [2].

Most DCCB designs are still at the prototype, pilot, or limited release stages, making them unviable for commercial applications. Furthermore, DC switchgear lacks universally accepted test standards, which slows the adoption of DCCBs as a common protection solution [7], [8].

There is a wide range of DC applications, including EV charging, Data centers, DC traction, DC shipboard, and offshore platforms. Each presents distinct power handling requirements and a distinct fault spectrum. Hence, requires the custom tailoring of DCCBs for individual applications, which presents a significant challenge [3], [7].

2.3 Voltage and Current Balancing Techniques for IGBTs

With the increasing use of MVDC and HVDC applications, DCCBs are required to handle currents of up to several kiloamperes and voltages of several hundred kilovolts, which exceed the ratings of available IGBT switches [1], [7], [15]. Hence, multiple IGBT units must be arranged in series and parallel to accommodate the required current and voltage rating. Several techniques are suggested in the literature to ensure voltage and current balancing between series and parallel-connected IGBTs [15], [32], [45], [46], [47], [48], [49].

2.3.1 Series Connected IGBTs

Passive snubber devices are primarily employed to achieve voltage sharing between series IGBT arrays. Snubbers compensate for IGBT parameter mismatches and gate-drive delays by limiting the voltage slope during IGBT turn-off [45], [47], [50]. IGBTs in DCCBs are expected to handle high short-circuit currents, and such high currents give rise to very large TIVs. The snubber capacity required is proportional to the square of the device current; Hence, the required capacitor must be several times larger than during normal operating conditions [15], [32], [51]. These high-voltage, high-capacity snubbing capacitors are large and expensive. Additionally, snubber performance tends to deteriorate over time, potentially leading to poor voltage sharing between IGBTs [46], [52]. Hence, snubber-connected IGBT stacks require significant derating.

Active Gate Clamping (AGC) circuits are proposed to suppress overvoltage and achieve voltage balance between series-connected IGBTs [47], [53]. AGC uses Zener diodes to provide

direct feedback of the collector voltage to the IGBT gate. When the voltage across the IGBT exceeds a defined limit, the gate clamping circuit activates and injects a current into the IGBT's gate, which limits the rate of change of collector-emitter voltage, dv_{CE}/dt [47].

Due to the direct feedback of the collector voltage to the gate, bypassing the gate control circuitry, gate clamping may lead to high voltage overshoots and device failures. To overcome the poor voltage sharing, combining the AGC with passive snubber voltage balancing is discussed in Figure 2.6 (a) [54], [55].

Advanced gate clamping schemes with status feedback to achieve controllability over the clamping are proposed in [53], [56]. The sensing circuit can detect both the activation of the clamp circuit and the magnitude of the injected current (Figure 2.6 (b)). The gate drive control circuit can calculate the compensation factor accordingly.

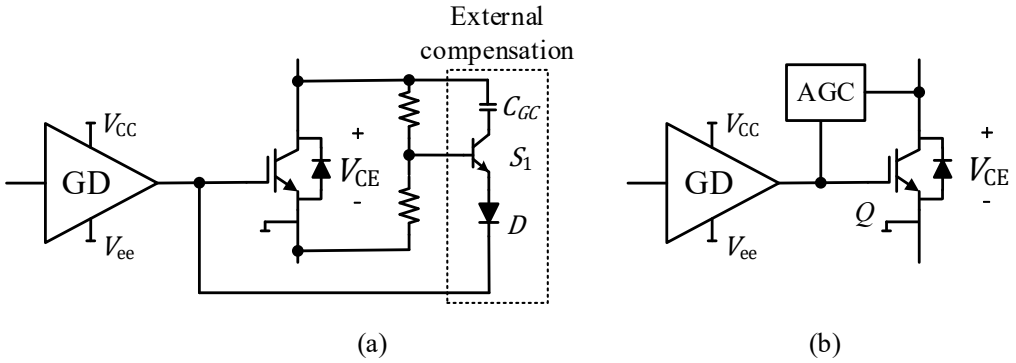


Figure 2.6: (a) Combined active gate clamping with passive snubber device to improve voltage sharing, (b) Active gate clamping with status feedback [55], [56].

The literature discusses the use of Active Gate Drive (AGD) schemes for voltage balancing between series IGBTs. An active gate current control method is proposed to achieve dynamic voltage sharing between series IGBTs [57]. The balance is achieved by measuring the time it takes for each IGBT to reach its desaturation point. Accordingly, the gate current (i_G) is adjusted so that all IGBTs start increasing their collector-to-emitter voltage (v_{CE}) simultaneously. The

main drawback of this scheme is that it relies on multiple measurements and sensor circuits for individual IGBT measurements and requires gate-current calibration based on the IGBT desaturation period.

An active gate voltage control scheme has been proposed in [58]. This approach applies a predefined voltage slope signal to the gate drive as the reference voltage. The slope of the reference voltage can be adjusted independently and depends on the response of the slowest IGBT. A global controller signals individual gate controllers to maintain or reduce the voltage slope to achieve voltage balance.

Similarly, a cascaded voltage control loop for IGBT switching is proposed in [59]. Three cascaded feedback loops, v_{CE}, v_{GE}, and dv_{CE}/dt, are used. IGBTs in a series string can follow a predefined voltage reference ramp to achieve dynamic voltage balance during switching. AGD schemes will be further discussed in Section 2.4.

2.3.2 Parallel Connected IGBTs

Dynamic and static imbalances in the collector current of parallel-connected IGBTs can result in device failures. Static unbalances related to parametric variations in IGBTs and different parasitic resistances of the wires connecting the IGBTs. Dynamic imbalances are mainly due to delays in the gate drive circuits and differences in the inductances of the connecting circuit between IGBTs [21], [60], [61]. Thus, ensuring both dynamic and steady-state current balance in parallel-connected IGBT modules requires careful control and compensation strategies.

The loop inductance of the circuit is crucial to ensure dynamic and steady-state current sharing among IGBTs in parallel. An unbalanced gate drive impedance can cause dynamic current imbalance during switching [62]. Furthermore, switching delay skew among individual

gate drives can result in asymmetric switching. Gate drive delay skews must be minimized to connect IGBTs in parallel. Thermal coupling between IGBTs connected in parallel is crucial, as a similar thermal profile can prevent thermal runaway [49], [62].

Using a return gate resistor (R_E) (Figure 2.7 (a)) to dampen parasitic oscillations induced by cross-coupling between IGBT gates is discussed in [49] and [63]. In this approach, each IGBT in a parallel combination is driven in a common-emitter configuration to compensate for differences in module transfer characteristics. Thermal coupling is achieved by mounting the IGBTs in the same heat sink.

The current that is flowing in the common emitter connection can cause gate oscillations. To overcome this, the use of common-mode chokes with a common gate driver for parallel IGBTs (Figure 2.7 (b)) is discussed in the literature [63]. Common-mode chokes present a low impedance to the gate current but a high impedance to the current flowing in the gate emitter loop.

A double-stage gate drive circuit is proposed in [21] to achieve equal dynamic current sharing. The gate driver features two low and high-resistance modes, splitting the IGBT switching operation into two stages. Dynamic current balance is achieved by detecting the current edge times of the IGBTs in parallel and adjusting the turn-on and turn-off times of the individual IGBTs accordingly.

An active gate drive scheme is proposed in [64], in which the static current through the IGBTs connected in parallel is balanced by controlling the gate-to-emitter voltage (v_{GE}). The collector current through each IGBT is estimated using the internal voltage across the stray inductance (L_{bond}), which is proportional to di_C/dt. The controller calculates the correction factor

for each current, increasing or decreasing the v_{GE} accordingly. AGD schemes will be further discussed in the next Section.

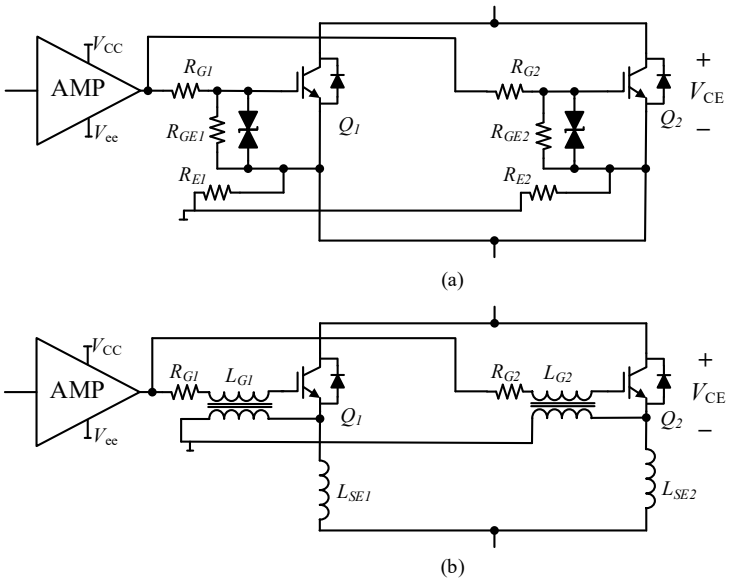


Figure 2.7: (a) Using a return gate resistor to dampen the parasitic oscillations due to cross-coupling of parallel IGBT gates, (b) Using a common-mode choke to dampen parasitic oscillations [49], [63].

2.4 Active Gate Drive Technology

2.4.1 Open-loop Active Gate Drives

AGD concepts where the gate current is controlled by employing adjustable gate resistors (Figure 2.8 (a)) [64], gate current sources (Figure 2.8 (b) and (c)) [65], and gate voltage sources (Figure 2.8 (d)) [66] in a feedforward manner are presented.

The underlying idea is to divide the switching transient into distinct periods, such as gate current delay, voltage slope, and current slope. A specific gate resistor, current source, or gate voltage is applied in each interval to obtain the desired switching characteristics.

Without feedback, IGBT non-linearities and temperature dependencies cannot be compensated, a significant drawback of these schemes. Thus, achieving the defined current and voltage switching trajectories is impossible.

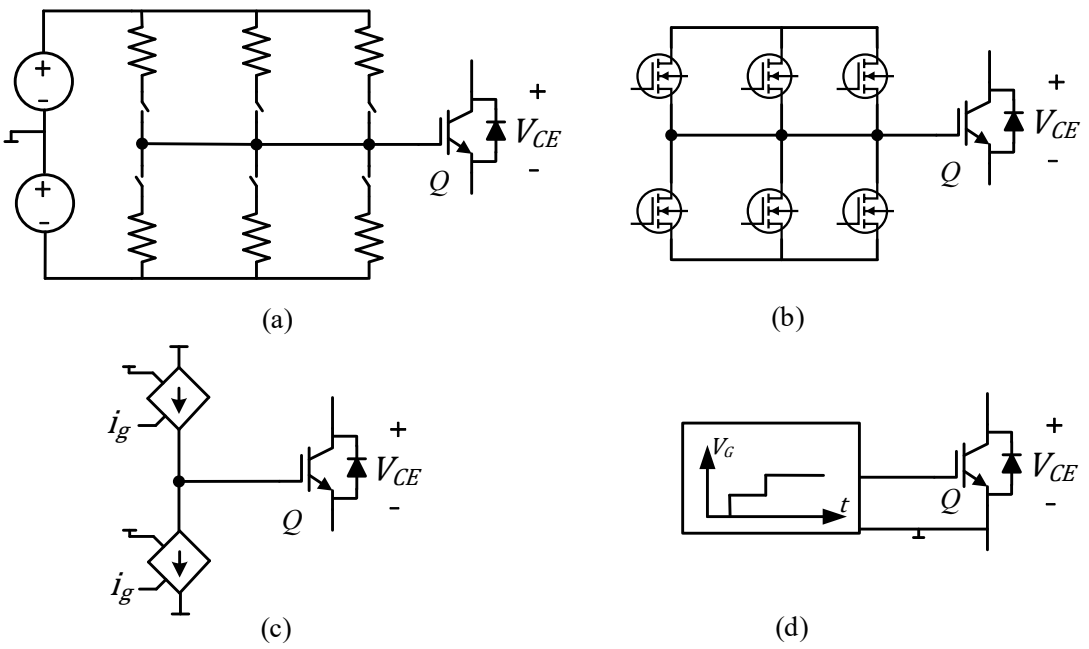


Figure 2.8: Open-loop AGD implemented by (a) Switchable gate resistors, (b) Adjustable gate current by operating the MOSFETs in the saturation region, (c) Adjustable gate current by current source, (d) Adjustable gate voltage source [64], [65], [66].

2.4.2 Closed-loop Active Gate Drives

Closed-loop AGDs can compensate for IGBT non-linearities and temperature dependencies to achieve desired switching characteristics. Different implementations of closed-loop AGD are shown in Figure 2.9.

Direct control of v_{CE} with a feedback loop is illustrated in Figure 2.9 (a). The reference input defines the IGBT's voltage trajectory during dynamic switching [32]. A similar approach to voltage feedback, where a cascaded dv_{CE}/dt and v_{GE} feedback loop serves as the inner feedback loop, is discussed in [50].

The AGD scheme with di_C/dt and dv_{CE}/dt feedback loop control is illustrated in Figure 2.9 (b). The proposed technique requires active selection of a control loop using a multiplexer or other circuitry at the transition of the current slope to the voltage slope and vice versa. This requires a complex circuit to accurately detect IGBT status [67].

A digital implementation of AGD is illustrated in Figure 2.9 (c) [68]. The v_{CE} and i_C values are sampled by the Analog to Digital Converters (ADCs), and accordingly, the digital controller calculates the gate voltage profile. The proposed scheme has the drawback of delays in ADC and Digital to Analog Converter (DAC) conversions, resulting in inaccurate control. Iterative and adaptive control methodologies are utilized to compensate for the delays [67], [68].

The AGD scheme, which utilizes complementary current sources to inject additional drive current into the IGBT gate, is illustrated in Figure 2.9 (d) [69]. Specific transient switching stages are accelerated by injecting via the complementary current source. The proposed digital control scheme requires complex circuitry for practical realization, which is a drawback.

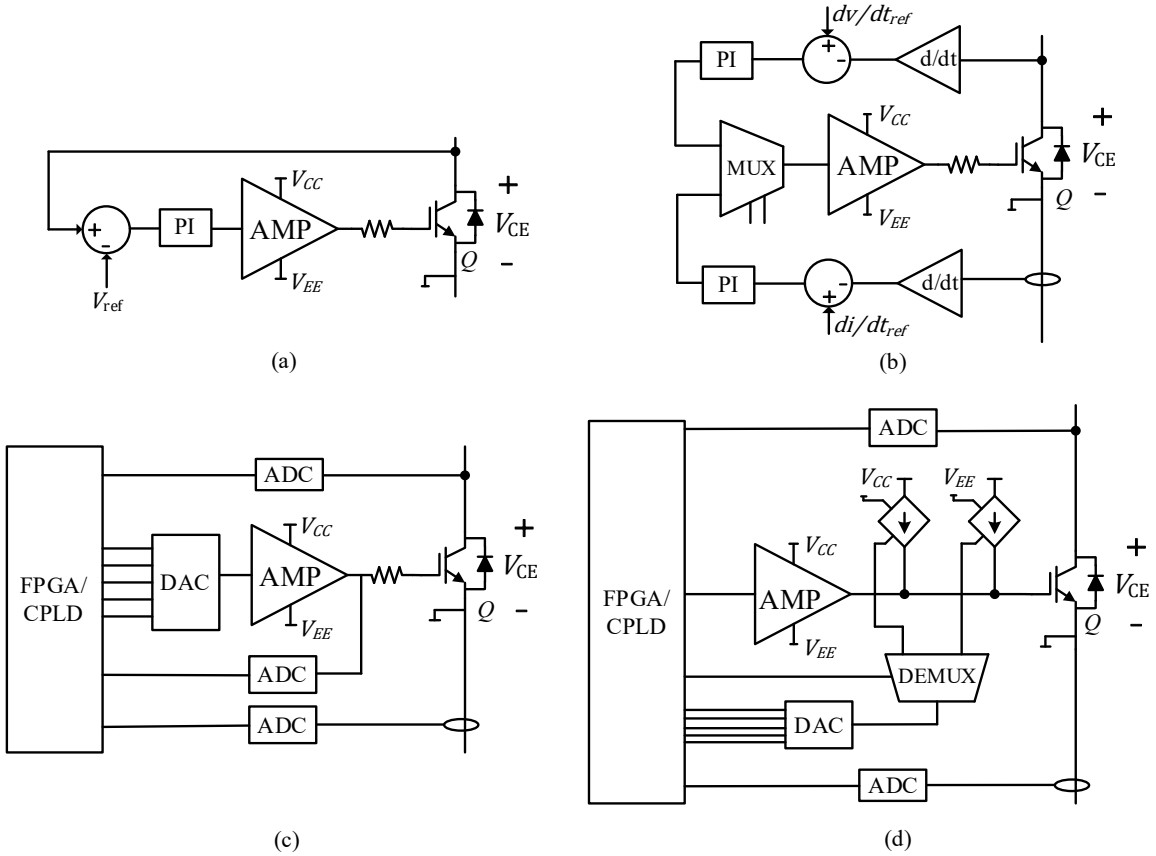


Figure 2.9: (a) AGD with direct v_{CE} feedback, (b) di_C/dt and dv_{CE}/dt feedback loops with active selection, (c) Digital implementation of AGD with v_{CE}, $i_{C,}$ and v_{GE} feedback, (d) AGD with complementary current sources [32], [67], [68], [69].

DC Circuit Breaker (DCCB) technologies can provide reliable protection for MVDC networks. However, the challenges associated with DCCBs stemming from the limited current and voltage capabilities of discrete semiconductor devices need to be addressed. AGD technologies could provide a reliable solution to overcome these challenges and will be explored in the next chapter.

Chapter 3: Active Gate Drive for Dynamic Voltage and Current Balancing

This chapter discusses the development methodology for the AGD scheme for voltage and current slope control, aiming to achieve dynamic voltage and current balancing in IGBT arrays, as well as the development of a standardized Active Switching Module (ASM). The fundamental theory underlying the proposed concept of AGD is discussed in detail, along with experimental studies validating the di_C/dt and dv_{CE}/dt control capabilities.

3.1 Development of an Active Gate Drive Scheme for Voltage and Current Balancing Operation.

3.1.1 Active Gate Drive Concept

In principle, AGD controls the gate current (i_G) through the IGBT gate to achieve the desired dynamic switching characteristics [22], [60], [69]. By controlling the gate-to-emitter voltage (v_{GE}), i_G can be controlled, which determines the operating behavior of the IGBT during both turn-on and turn-off operations [46], [61].

Typically, the IGBT switching time ranges from 50 ns to 1 μs, depending on the size and construction of the IGBTs. Control of the i_G to actively adjust the di_C/dt and dv_{CE}/dt during IGBT switching requires high-speed control action by the AGD. Furthermore, high bandwidth di_C/dt and dv_{CE}/dt measurements are imperative for implementing closed-loop AGD [46], [65].

The proposed closed-loop AGD technique can enable individual control of current and voltage slopes independent of non-linearities, temperature dependencies, and varying operating points of the IGBTs [67]. IGBTs incur high switching losses in the active region and undergo

high stress. It may easily lead to hot-spotting and current hogging within the die, ultimately resulting in linear-mode failure of the IGBT due to localized thermal overstress [64], [70]. Hence, the Safe Operating Area (SOA) limits provided by the manufacturers must be adhered to. Power IGBTs can operate in the active region from several hundred microseconds to a few milliseconds below their rated current and voltage. Operating the IGBTs safely for an extended period in the active region is an important design consideration for AGDs [70]. Furthermore, the developed AGD should be immune to common mode dv/dt transients at the IGBT terminals [71].

3.1.2 Proposed Active Gate Drive for di_C/dt and dv_{CE}/dt Control.

The schematic diagram of the proposed AGD is shown in Figure 3.1. The dynamic switching period must be extended to allow the current and voltage slopes to synchronize, compensating for non-linearities and delay skews during IGBT switching. IGBT parasitic miller capacitance ($C_{GC,int}$) and gate-to-emitter capacitance ($C_{GE,int}$) are non-linear and voltage-dependent. In the proposed AGD scheme, an external gate-emitter capacitor ($C_{GE,ext}$) and an external Miller capacitor ($C_{GC,ext}$) are connected across each IGBT. A small damping resistor (R_D) is added to avoid oscillations between $C_{GE,ext,}$ and $C_{GE,int}$. $C_{GE,ext}$ adds to the $C_{GE,int}$ and increases the gate charge during the current slope interval. Hence it slows di_C/dt without significantly affecting dv_{CE}/dt period. Similarly, $C_{GC,ext}$ adds to the $C_{GC,int}$ and increase the gate charge during the voltage slope period. Thereby slowing down the dv_{CE}/dt without affecting di_C/dt period.

External capacitances behave linearly over the voltage range and assist in more accurate di_C/dt and dv_{CE}/dt control. This increases the dynamic control capability of di_C/dt and dv_{CE}/dt, resulting in more homogeneous current and voltage profiles across the IGBTs. The downside of adding $C_{GC,ext}$, and $C_{GE,int}$ is the increase in total gate charge and switching losses [67].

Nonetheless, this is not a drawback concerning the DCCB application for which the AGD is designed. In DCCBs, the primary role of IGBTs is to operate during breaker switching, where they absorb the transient inrush current and TIV. IGBTs are not expected to be continuously switched as in switching power applications [71], [72].

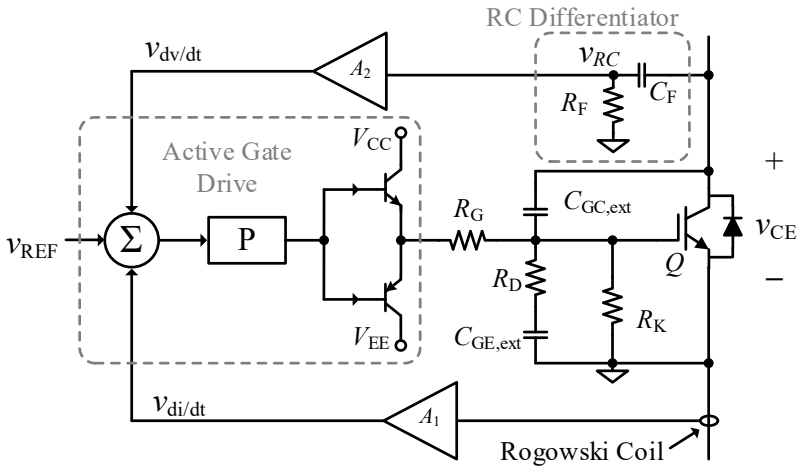


Figure 3.1: Schematic diagram of the proposed Active Gate Drive (AGD).

3.1.3 di_C/dt and dv_{CE}/dt Sensing Circuitry.

The proposed AGD requires high bandwidth di_C/dt and dv_{CE}/dt measurements. As shown in Figure 3.1, an RC differentiator measures the dv_{CE}/dt across the IGBT during switching. The output of the RC differentiator is proportional to the derivative of the input voltage within its operating bandwidth, thereby providing a scaled representation of dv/dt. This approach eliminates the need for dedicated high-speed voltage sensors and explicit differentiator circuits, which are often sensitive to noise and bandwidth limitations. Filter resistance (R_F) and capacitance (C_F) can be selected to achieve the required measurement bandwidth.

When the measured signal satisfies $\omega \ll 1/R_F C_F$, the output voltage of the RC differentiator can be written as;

$$v_{RC}(t) \approx R_F C_F \frac{dv_{CE}(t)}{dt} \tag{3.1}$$

High bandwidth Op-Amp Gain of A_1 amplifies the induced voltage.

$$v_{dv/dt} = -A_1 R_F C_F \frac{dv_{CE}(t)}{dt} \tag{3.2}$$

Printed Circuit Board (PCB) Rogowski coil measures the di_C/dt through the IGBT. The Rogowski coil is a low-cost alternative to a high-bandwidth Hall sensor for current measurement and for deriving di_C/dt. Previous studies on AGDs suggest using bond wire inductance (L_{bond}) to measure di_C/dt. However, it may lead to measurement and calibration errors, as the L_{bond} depends on the IGBT construction.

The induced voltage in the coil terminal v_{ROG} is;

$$v_{ROG} = -M \frac{di_C(t)}{dt} \tag{3.3}$$

Here, M is the mutual inductance of the coil. Apart from mutual inductance, each coil turn has parasitic capacitance between its turns, resulting in multiple resonance points [73]. In regular operation, the Rogowski coil is used only at frequencies below its first resonance frequency. The high-bandwidth OpAmp amplifier, with gain A_2, amplifies the induced voltage.

$$v_{di/dt} = A_2 M \frac{di_C(t)}{dt} \tag{3.4}$$

3.1.4 Voltage and Current Slope Control

The proposed AGD utilizes a single Proportional (P) controller that automatically transitions between di_C/dt and dv_{CE}/dt. During IGBT switching, voltage and current slope periods appear in sequence without overlap. This allows us to use a single controller for di_C/dt and dv_{CE}/dt control, as di_C/dt feedback is zero during the voltage slope period, and dv_{CE}/dt is zero during the current slope period. Hence, an automatic transition between the di_C/dt and

dv_{CE}/dt control loops occurs, eliminating the need for complex circuitry for IGBT switching-phase detection and feedback signal multiplexing.

As shown in Figure 3.1, the reference voltage V_{REF} defines the di_C/dt and dv_{CE}/dt during turning on/off switching cycles. Reference values for di_C/dt and dv_{CE}/dt are defined in equations (3.5) and (3.6).

$$\left(\frac{di}{dt}\right)_{REF} = -\frac{V_{REF}}{A_2.M} \tag{3.5}$$

$$\left(\frac{dv}{dt}\right)_{REF} = \frac{V_{REF}}{A_1.R_F.C_F} \tag{3.6}$$

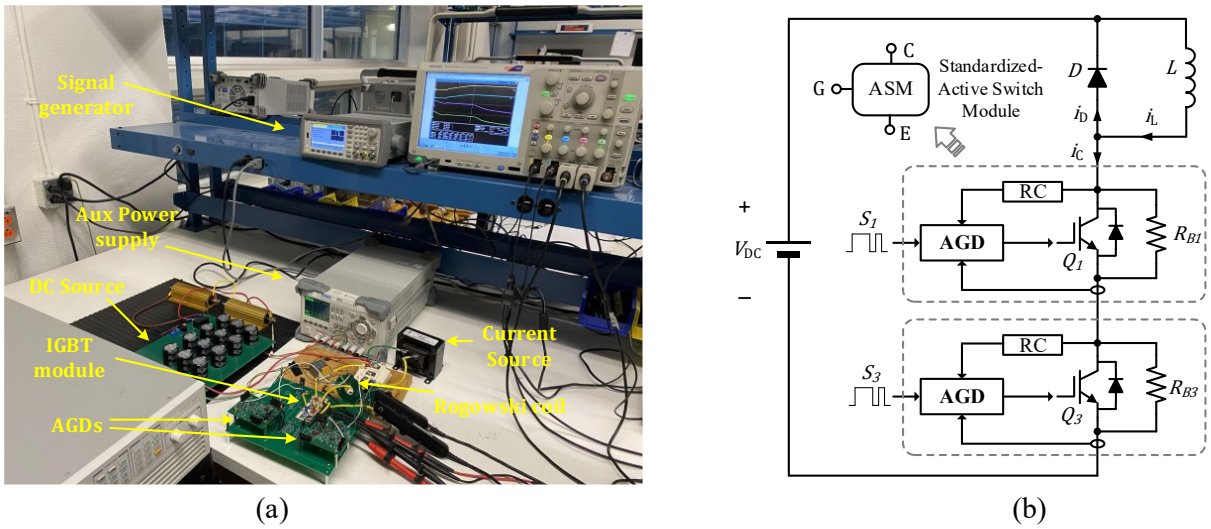
According to Equations (3.5) and (3.6), a negative V_{REF} initiates the IGBT turning on (i.e., positive current slope and negative voltage slope), and a positive V_{REF} initiates the IGBT turning off (i.e. negative current slope and positive voltage slope). The sign inversion is used to compensate for the controller output inversion in the inverting amplifier configuration.

The proposed AGD controller is only active during the dynamic voltage and current slope period, as there is no feedback with di_C/dt and dv_{CE}/dt zero during the steady state. Therefore, without di_C/dt and dv_{CE}/dt feedback, the AGD functions as a resistive gate drive.

3.1.5 Hardware Prototype of the AGD and Test Setup.

Figure 3.2 (a) shows the experimental Double Pulse Test (DPT) setup to verify the proposed AGD for di_C/dt and dv_{CE}/dt control. The AGD prototype is implemented using high-bandwidth Op-Amps to achieve high control bandwidth. The schematic block diagram of the test setup is shown in Figure 3.2 (b). The AGD unit is referenced to the IGBT emitter. IGBT, measurement circuits, and the AGD collectively constitute an Active Switch Module (ASM). The ASM is isolated from the control unit using an isolated gate drive, and each ASM requires an isolated DC power supply for the AGD control circuit. V_{REF} is set at the start of the switching cycle.

Switching pulses are generated by the central controller. The DPT setup (560V and 60A) with an inductive load of 2.5 mH is used.



(a) (b)

Figure 3.2: Evaluating platform for the proposed AGD (a) Experimental Setup, (b) Schematic block diagram.

The first series of experiments examines the independent control capability of di_C/dt and dv_{CE}/dt in the IGBT for different V_{REF} values. Secondly, to assess the independent voltage and current balancing capability using AGD, tests are conducted with ASMs connected in parallel and in series arrays.

3.1.6 Switching Behavior of ASMs

The switching behavior of the ASM is examined in this Section. Different stages of IGBT switching are identified during the IGBT's turn-on and turn-off processes for this analysis. Figure 3.3 (a) and (b) show the voltage and current waveform trends at IGBT turning on and off, respectively. An equivalent circuit of an IGBT operating in the active region during IGBT turning on and off is shown in Figure 3.4. During the ASM turning on and off, the progress of the IGBT operating point along the IGBT output characteristics and transfer characteristics is shown in Figure 3.5 (a) and (b), respectively.

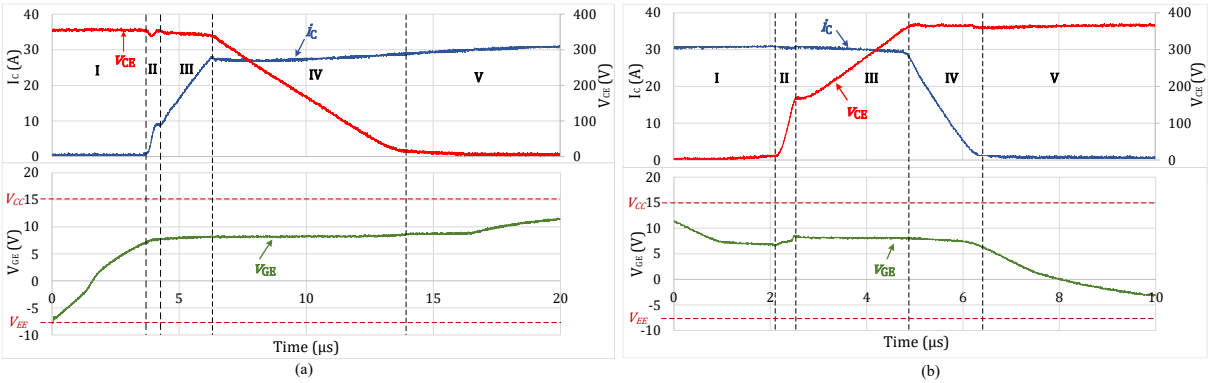


Figure 3.3: Transient voltage and current waveforms during (a) ASM turning on, (b) ASM turning off.

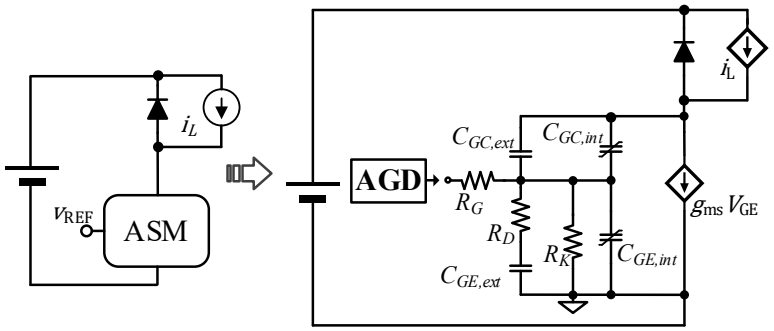


Figure 3.4: Equivalent circuit of the IGBT operating in the active region during ASM switching.

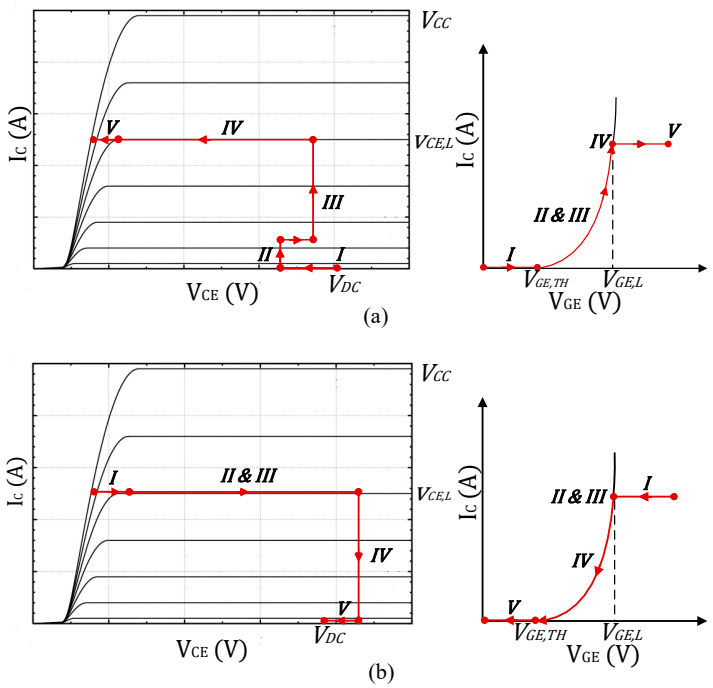


Figure 3.5: Progress of operating point in IGBT output and transfer characteristics during (a) ASM turning-on, (b) ASM turning-off.

As shown in Figure 3.3 (a), ASM turning on can be characterized into five stages for analysis. *Stages III* and *IV* are the periods during which the IGBT's active current and voltage slope are controlled. Similarly, ASM turning off can be identified into five stages, as shown in Figure 3.3 (b). During *stages III* and *IV,* voltage and current slopes are controlled by AGD, set by voltage slope reference $(dv/dt)_{REF,}$ and current slope reference $(di/dt)_{REF}$, respectively.

A detailed behavioral analysis of ASM turning on and off, along with the ASM switching equations, is provided in *Appendix A*.

The first series of experiments examined the capability of the AGD to independently control the di_C/dt and dv_{CE}/dt with different $(di/dt)_{REF}$ and $(dv/dt)_{REF}$. Figure 3.6 (a) and (b) show the measurements of ASM turning on and off with different $(di/dt)_{REF}$ and $(dv/dt)_{REF}$.

The measured results demonstrate the AGD's capability to control the di_C/dt and dv_{CE}/dt during both IGBT turn-on and turn-off. During IGBT turn-on, a rapid current rise occurs before the controller achieves the desired di_C/dt. Similarly, when the IGBT is turned off, a rapid voltage rise can be observed before the AGD achieves the desired dv_{CE}/dt.

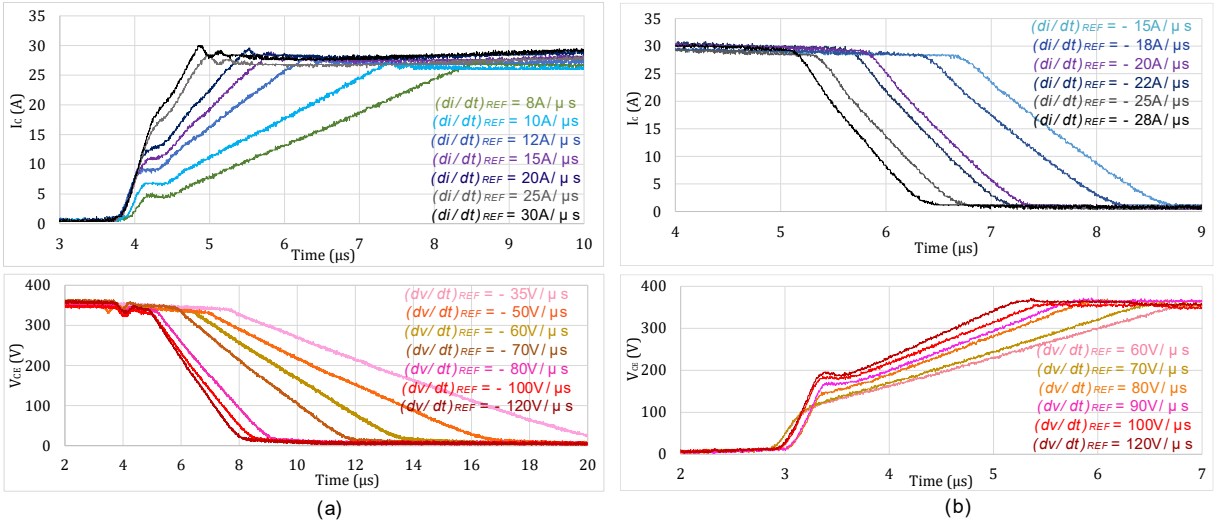


Figure 3.6: Collector current (i_C) and collector-emitter voltage (v_{CE}) with different V_{REF} during (a) IGBT turning-on, (b) IGBT turning-off.

3.2 Current and Voltage Balancing Operation of Standardized-ASMs: Testing and Verification

In this section, the voltage and current balancing proficiency of the ASMs when interconnected in series and parallel arrangements is assessed. The AGD regulates the di_C/dt and dv_{CE}/dt during IGBT switching, facilitating dynamic voltage and current balance between ASMs. This eliminates dependence on non-linearities and differences in operating point between IGBTs, allowing compensation for gate-drive delays between ASM modules.

Voltage balancing in steady state can be achieved using static voltage balancing resistors (R_B), as shown in Figure 3.7. Differences in internal parameters such as C_{GE}, C_{GC}, C_{CE}, and R_G cause a dynamic voltage imbalance between IGBTs connected in series. Other factors that affect uneven dynamic voltage sharing include delay skew between gate drives and differences in stray inductance and capacitance in the circuit.

In a series-connected ASM array (Figure 3.7), dynamic voltage sharing can be achieved by increasing the dynamic voltage rise/fall time interval using the AGD to accommodate gate drive delays. Figure 3.8 (a) and (b) show the voltage sharing between two series ASMs during turning off and on, respectively, with different V_{REF} for dynamic voltage slope control. The different V_{REF} values result in different dv_{CE}/dt, demonstrating the capability of the proposed AGD to regulate the switching transient over a wide operating range.

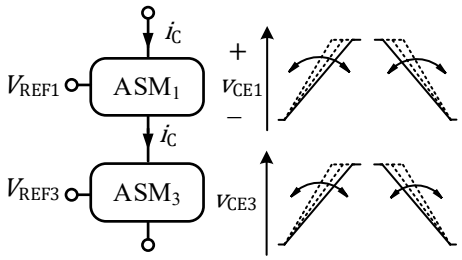


Figure 3.7: Series connection of IGBTs for voltage sharing operation.

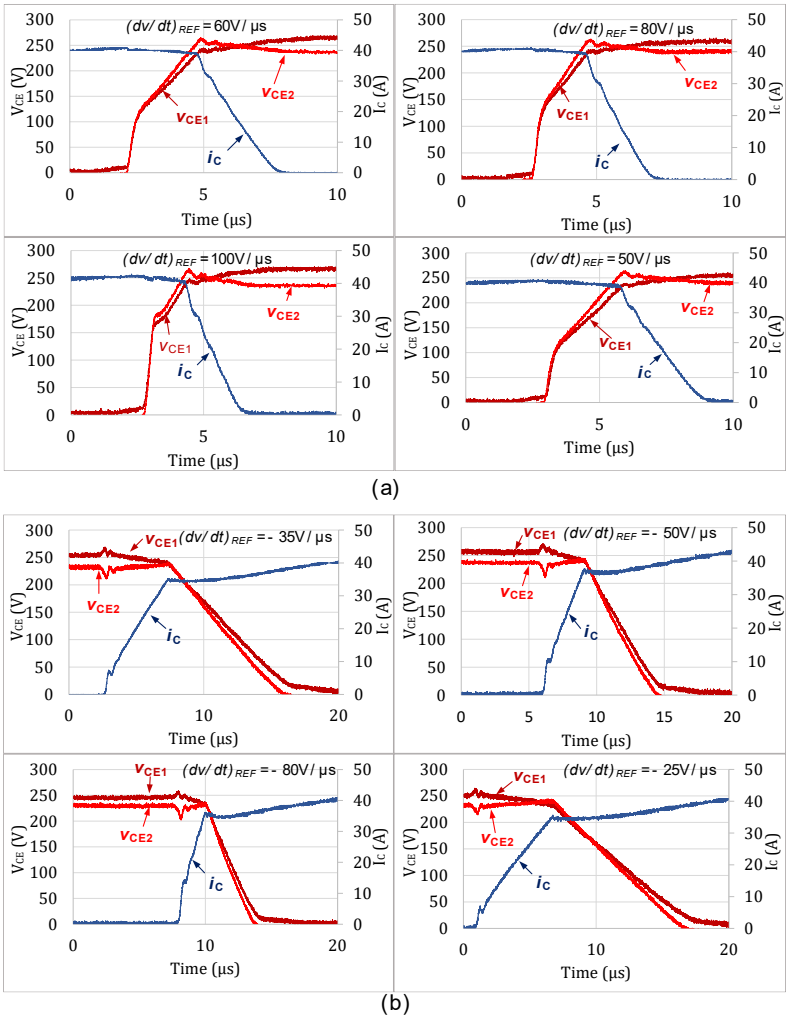


Figure 3.8: Voltage sharing between two series-connected ASMs, with different $(dv/dt)_{REF}$, during (a) turning off, (b) turning on.

Dynamic current unbalance during IGBT switching is primarily caused by differences in delay times between gate drives and optical isolators, as well as variations in IGBT parameters. Current sharing between parallel-connected IGBTs is tested with two parallel ASMs (Figure 3.9) in the DPT setup. Figure 3.10 (a) and (b) show the current sharing between two parallel ASMs during IGBT turning-on and turning-off, respectively. ASM_1 and ASM_2 share current with minimal current imbalance during switching. This demonstrates the ability of the proposed ASM scheme to achieve dynamic current balance while maintaining predefined $(di/dt)_{REF}$.

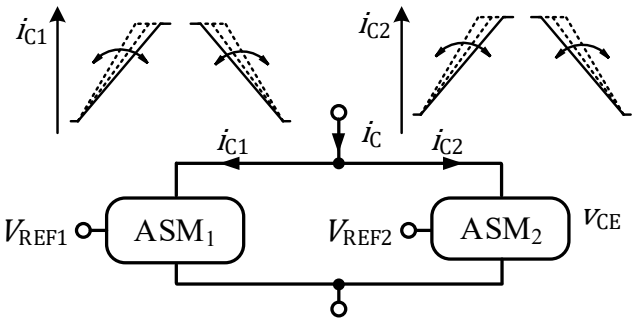
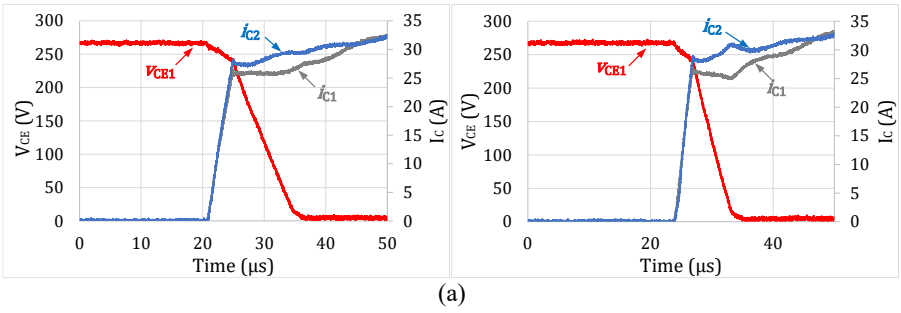
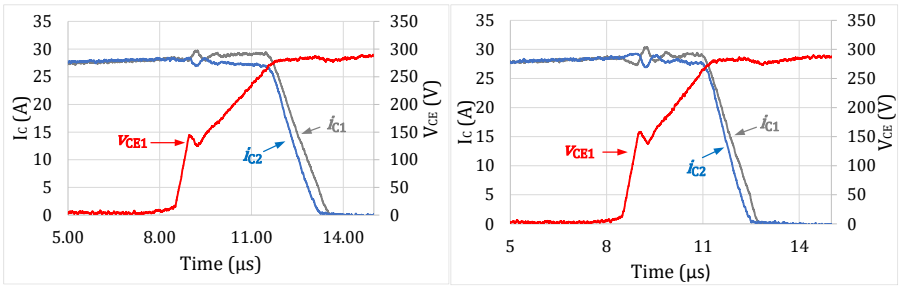


Figure 3.9: Parallel connection of ASMs for current sharing operation



(a)



(b)

Figure 3.10: Current sharing between two parallel connected ASMs with different $(di/dt)_{REF}$ during (a) turning on and (b) turning off.

3.3 Small Signal Modeling and Stability Analysis

A central requirement in the closed-loop design is ensuring adequate loop stability. This section presents the small-signal modeling of the di_C/dt and dv_{CE}/dt control loops, followed by a corresponding stability assessment. The analysis is developed for the IGBT turn-on interval. The governing equations for turn-off have an analogous structure; therefore, the modeling framework and resulting stability conclusions remain valid for the turn-off transition as well.

3.3.1 Plant Transfer Function Modeling for di_C/dt Control

During the current slope control period, v_{CE} is clamped by the diode to the DC link voltage. Hence, it can be assumed to be constant. The characteristic equation for the dynamic di_C/dt control stage can be written as (See *Appendix A* for derivation);

$$\frac{di_C(t)}{dt} = g_{ms}\left[\frac{i_G(t)}{C_{GE,int}+C_{GE,ext}}\right] = \frac{v_{AGD}(t)-v_{GE}(t)}{R_G+R_D} \times \frac{g_{ms}}{C_{GE,int}+C_{GE,ext}} \qquad (3.7)$$

Using the simplifying assumptions; $R_G = R_G+R_D$ and $C_{GE} = C_{GE,int}+ C_{GE,ext}$

$$\frac{di_C(t)}{dt} = \frac{v_{AGD}(t)-v_{GE}(t)}{R_G} \times \frac{g_{ms}}{C_{GE}}$$

During the period of di_C/dt

$$v_{GE}(t) = V_{GE,th} + \frac{i_C(t)}{g_{ms}}$$

Define $\tau = R_G C_{GE}$

$$\frac{di_C(t)}{dt} = \frac{g_{ms}}{\tau}\left(v_{AGD}(t) - V_{GE,th}\right) - \frac{i_C(t)}{\tau} \qquad (3.8)$$

Equation (3.8) is the core dynamic relation for di_C/dt control. Consider a small perturbation around the operating point I_{C0} and V_{AGD0}.

$$i_C(t) = I_{C0} + \Delta i_C(t)$$

$$v_{AGD}(t) = V_{AGD0} + \Delta v_{AGD}(t)$$

Writing Equation (3.8) in small signal form

$$\frac{d\,(I_{C0}+\Delta i_C(t))}{dt} = \frac{g_{ms}}{\tau}\left(V_{AGD0} + \Delta v_{AGD}(t) - V_{GE,th}\right) - \frac{(I_{C0}+\Delta i_C(t))}{\tau} \qquad (3.9)$$

The derivative of the I_{C0} is zero.

$$\frac{dI_{C0}}{dt} = 0$$

Obtaining the DC operating point relationship from Equation (3.9)

$$\frac{d\,(I_{C0})}{dt} = \frac{g_{ms}}{\tau}\left(V_{AGD0} - V_{GE,th}\right) - \frac{I_{C0}}{\tau}$$

$$0 = \frac{g_{ms}}{\tau}\left(V_{AGD0} - V_{GE,th}\right) - \frac{I_{C0}}{\tau}$$

We can rewrite the small signal relationship of Equation (3.9)

$$\frac{d\Delta i_C(t)}{dt} = \frac{g_{ms}}{\tau}\left(\Delta v_{AGD}(t)\right) - \frac{\Delta i_C(t)}{\tau}$$

Obtaining the Laplace transform of the above equation

$$s\Delta I_C(s) + \frac{1}{\tau}\Delta I_C(s) = \frac{g_{ms}}{\tau}\Delta V_{AGD}(s)$$

Transfer function for current slope di_C/dt

$$L\left(\frac{d\,\Delta i_C(t)}{dt}\right) = s\Delta I_C(s)$$

The transfer function for current slope control can be written as

$$G_{di}(s) = \frac{s\Delta I_C(s)}{\Delta V_{AGD}(s)} = \frac{s(g_{ms}/\tau)}{s+{}^{1}/_{\tau}} = \frac{sg_{ms}}{sC_{GE}R_G+1} \qquad (3.10)$$

g_{ms} is the small-signal transconductance (slope of i_C vs. v_{GE}) in the linear region of the IGBT. It is not a constant over the whole waveform. For small signal equations, g_{ms} should be linearized around the operating point. Refer to *Appendix B* for the calculation of g_{ms} around (I_{C0}, T_{J0}) from the transfer characteristics.

3.3.2 Plant Transfer Function Modeling of dv_{CE}/dt Control

After the collector current reaches the load current I_L, it remains constant. Hence, the gate voltage stays clamped to $V_{GE,th} + {}^{I_L}/_{g_{ms}}$. The gate current only discharges C_{GC} and leads to the decay of v_{CE}.

The characteristic equation for the dynamic dv_{CE}/dt control stage can be written as (Refer to *Appendix A*);

$$\frac{dv_{CE}(t)}{dt} = -\left[\frac{dv_{GC}(t)}{dt}\right] = -\left[\frac{i_G(t)}{C_{GC}}\right] = -\left[\frac{v_{AGD}-(V_{GE,th}+{I_L}/{g_{ms}})}{R_G}\right]\frac{1}{C_{GC}} \quad (3.11)$$

Consider a small perturbation around the operating point (I_{C0}, V_{AGD0})

$$v_{CE}(t) = V_{CE0} + \Delta v_{CE}(t)$$

$$v_{AGD}(t) = V_{AGD0} + \Delta v_{AGD}(t)$$

The term $v_{\mathrm{GE,th}} + {I_L}/{g_{ms}}$ is constant

Writing Equation (3.11) in small signal form

$$\frac{d(V_{CE0}+\Delta v_{CE}(t))}{dt} = -\left[\frac{(V_{AGD0}+\Delta v_{AGD}(t))-(V_{GE,th}+{I_L}/{g_{\mathrm{ms}}})}{R_{\mathrm{G}}}\right]\frac{1}{C_{GC}} \quad (3.12)$$

The derivative of the V_{CE0} is zero.

$$\frac{dV_{CE0}}{dt} = 0$$

Obtaining the DC operating point relationship from (3.12)

$$\frac{dV_{CE0}}{dt} = -\left[\frac{(V_{AGD0})-(V_{GE,th}+{I_L}/{g_{\mathrm{ms}}})}{R_{\mathrm{G}}}\right]\frac{1}{C_{\mathrm{GC}}}$$

$$0 = -\left[\frac{V_{AGD0}-(V_{GE,th}+{I_L}/{g_{\mathrm{ms}}})}{R_{\mathrm{G}}}\right]\frac{1}{C_{\mathrm{GC}}}$$

We can rewrite the small signal relationship Equation (3.12)

$$\frac{d\Delta v_{CE}(t)}{dt} = -\left[\frac{\Delta v_{AGD}(t)}{R_{\mathrm{G}}}\right]\frac{1}{C_{\mathrm{GC}}}$$

Obtaining the Laplace transform of the above equation

$$s\Delta V_{CE}(s) = -\frac{\Delta V_{AGD}(s)}{R_G C_{GC}}$$

Transfer function for current slope

$$L\left(\frac{d\,\Delta v_{CE}(t)}{dt}\right) = s\Delta V_{CE}(s)$$

The transfer function for voltage slope control can be written as

$$G_{dv}(s) = \frac{s\Delta V_{CE}(s)}{\Delta V_{AGD}(s)} = -\frac{1}{R_G C_{GC}} \qquad (3.13)$$

The negative sign in the transfer function is due to the negative voltage slope during IGBT turn on. But will be disregarded in the open loop transfer function derivation as the closed loop transfer function of the dv_{CE}/dt is modelled as negative feedback model.

3.3.3 Controller and Feedback Transfer Function Modeling for di_C/dt and dv_{CE}/dt Control

The controller is implemented using high-bandwidth OpAmps. The transfer function of the OpAmp is given by.

$$G_{Op}(s) = \frac{A_{DC,Op}}{s\frac{A_{DC,Op}}{2\pi \times GBW}+1} = \frac{A_{DC,Op}}{1+\frac{s}{\omega p}} \qquad (3.14)$$

$A_{DC,Op}$ → DC gain of the OpAmp

GBW → OpAmp Gain Bandwidth (Transit frequency)

ω_p → dominant pole rad/s

The OpAmp is used in an inverting amplifier configuration. A parallel capacitor path is added to stabilize the OpAmp output. Hence, the transfer function of the controller becomes

$$G_C(s) = -\frac{K_p}{1+\frac{1+K_p}{G_{Op}(s)}} \cdot \frac{1}{1+sR_P C_P} \qquad (3.15)$$

Here, R_P and C_P represent the feedback resistor and capacitor, respectively. The purpose of C_P is to limit the high-frequency loop gain by adding an intentional pole. *Kp* is the proportional gain of the controller.

The driver output stage, which is used as the current buffer for the IGBT, can be modeled as a low-pass filter with a cutoff frequency $f_{C,AMP}$.

$$G_{AMP}(s) = \frac{1}{s\frac{1}{2\pi f_{C,AMP}}+1} \tag{3.16}$$

The output stage of the Active Gate Driver (AGD) was characterized using small-signal AC analysis in LTspice, utilizing behavioral models of the BJT transistors used in the amplifier. The measured -3 dB bandwidth is $f_{C,AMP}$ = 7.65 MHz.

An RC differentiator circuit is used for dv_{CE}/dt measurement. It can be modeled as a constant gain.

$$H_{dv}(s) = \frac{V_{RC}(s)}{sV_{CE}(s)} = A_1 R_F C_F \tag{3.17}$$

A Rogowski coil is used to generate a feedback signal proportional to di_C/dt.

$$H_{di}(s) = \frac{V_{ROG}(s)}{sI_C(s)} = A_2 M \tag{3.18}$$

3.3.4 Closed-loop Transfer Functions for di_C/dt and dv_{CE}/dt Control

A key consideration for the proposed closed-loop gate driver is system stability. This section evaluates the stability and gain metrics of the proposed di_C/dt and dv_{CE}/dt control.

Small signal control block diagram representing the voltage and current slope depicted in Figure 3. 11 (a) and (b), respectively. The polarity inversion introduced by the inverting amplifier stage is compensated through the configuration of the reference and feedback paths.

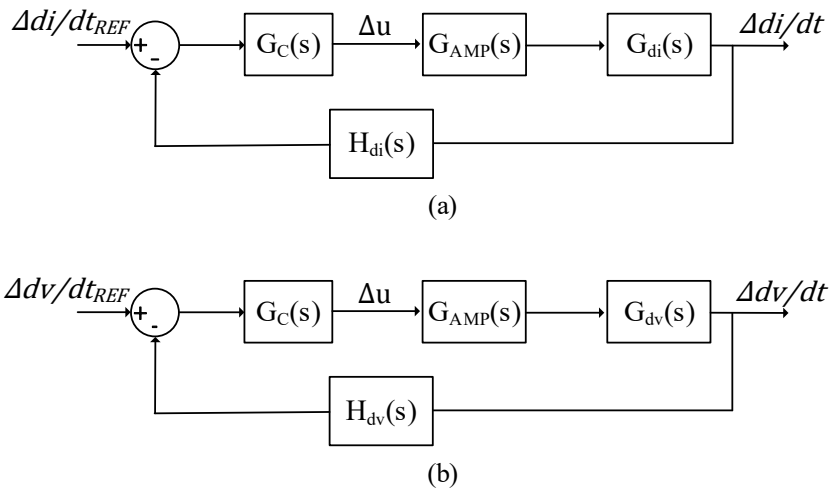


Figure 3. 11: Small signal control block diagram (a) di_C/dt control, (b) dv_{CE}/dt control

Accordingly, the open-loop transfer function from the reference signal $V_{REF,di/dt}$ to the current is given by

$$G_{di,OL}(s) = \frac{di/dt(s)}{V_{REF,di/dt}(s)} = G_C(s).G_{AMP}(s).G_{di}(s).H_{di}(s) \quad (3.19)$$

The open-loop transfer function from the reference signal $V_{REF,dv./dt}$ to the dv_{CE}/dt is given by

$$G_{dv,OL}(s) = \frac{dv/dt(s)}{V_{REF,dv/dt}(s)} = G_C(s).G_{AMP}(s).G_{dv}(s).H_{dv}(s) \quad (3.20)$$

Measured loop transfer function ($G_{meas(s)}$) indicates how well the output follows the reference.

$$G_{di,meas}(s) = \frac{G_{di,OL}(s)}{1+G_{di,OL}(s)} = \frac{G_C(s).G_{AMP}(s).G_{di}(s).H_{di}(s)}{1+G_C(s).G_{AMP}(s).G_{di}(s).H_{di}(s)} \quad (3.21)$$

$$G_{dv,meas}(s) = \frac{G_{dv,OL}(s)}{1+G_{dv,OL}(s)} = \frac{G_C(s).G_{AMP}(s).G_{dv}(s).H_{dv}(s)}{1+G_C(s).G_{AMP}(s).G_{dv}(s).H_{dv}(s)} \quad (3.22)$$

The parameters used for calculating control transfer functions are tabulated in *Appendix B*.

3.3.4.1 *Frequency Response of the Closed-loop Transfer Function $G_{di,meas}(s)$, and Open-loop Transfer Function $G_{di,OL}(s)$*

The closed-loop frequency response of $G_{di,meas}(s)$, and open-loop frequency response $G_{di,OL}(s)$, for the di_C/dt control loop are shown in Figure 3.12 and Figure 3.13, respectively. At low-mid frequencies of usable bandwidth (i.e. 100kHz - 1MHz), $|G_{di,meas}(s)|$ = 0dB, indicating accurate tracking of the reference voltage. There is a slight peaking around 1.5 MHz due to the pole positioning. -3dB closed-loop bandwidth is 1.9 MHz, which indicates a desirable bandwidth range. Loop gain and stability margins extracted from Figure 3.12 and Figure 3.13 are summarized in Table 3.1.

From the open loop frequency response $G_{di,OL}(s)$, a good phase margin of 56° at 0dB crossover point can be observed, which indicates good stability margin. Also, the gain at the phase crossover is positive indicating stability of the control loop.

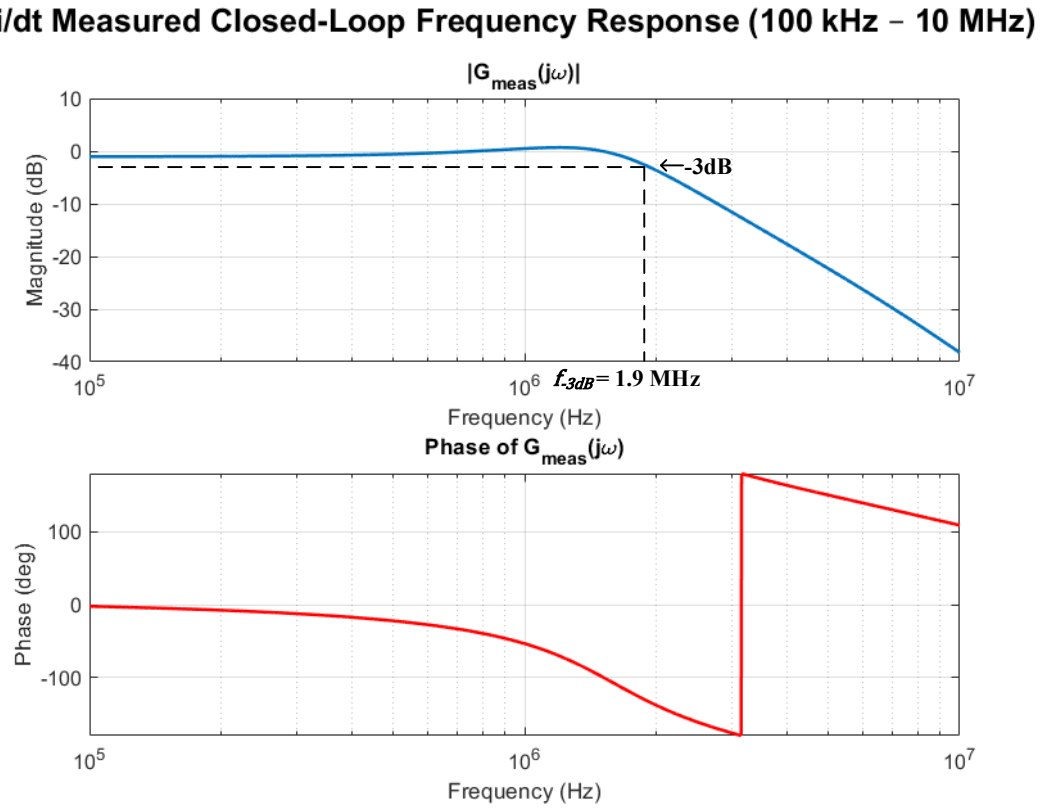


Figure 3.12: Frequency response of measured closed-loop transfer function $G_{di,meas}(s)$.

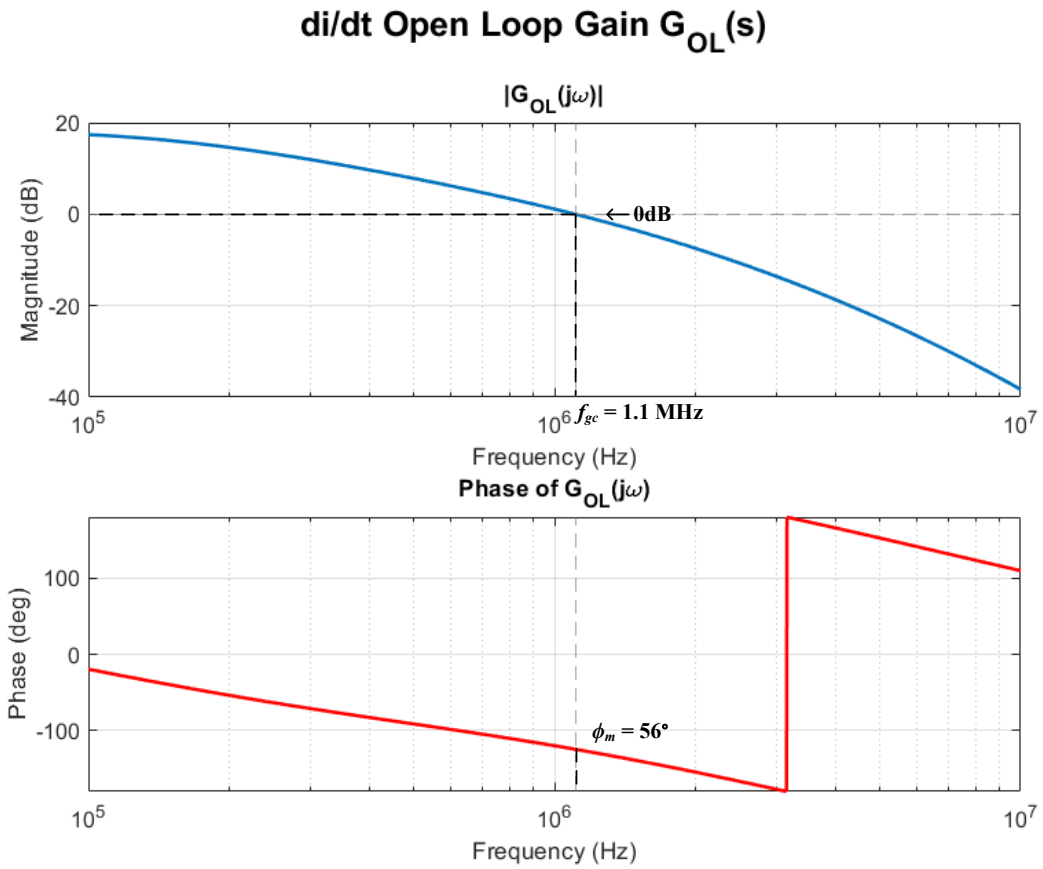


Figure 3.13: Frequency response of open-loop transfer function $G_{di,OL}(s)$.

Table 3.1: Loop gain and stability metrics for di_C/dt control

Parameter	**Value**
-3dB closed-loop bandwidth	1.9 MHz
$G_{di,\ OL}(s)$ Gain Crossover frequency	1.1 MHz
Phase margin (ϕ_m)	56°
Gain margin (G_m)	17 dB

3.3.4.2 Frequency Response of the Closed-loop Transfer Function $G_{dv,meas}(s)$, and Open-loop Transfer Function $G_{dv,OL}(s)$

Figure 3.14 and Figure 3.15 show the closed-loop and open-loop frequency responses of the dv_{CE}/dt control loop. At the low to mid-frequency range of usable bandwidth, the closed-

loop gain is close to -2dB. This indicates the control loop follows the reference with approximately 82% accuracy. This is due to the absence of integral action in the controller, resulting in a finite DC gain. However, as the controller is designed to ensure stable, fast, and monotonic operation, achieving unity gain is not essential. The closed-loop gain can be further improved by adjusting k_p. The -3dB measured loop bandwidth point is at 3.65 MHz. The gain and stability metrics from Figure 3.14 and Figure 3.15 are summarized in Table 3.2. From the frequency response of $G_{dv,OL}(s)$, at the unity gain crossover point $|G_{dv,OL}(s)| = 0$ dB, the phase margin is close to 70°, indicating good stability. Also, the $G_{dv,OL}(s)$ frequency response indicates 15 dB positive gain margin which indicates stable control loop.

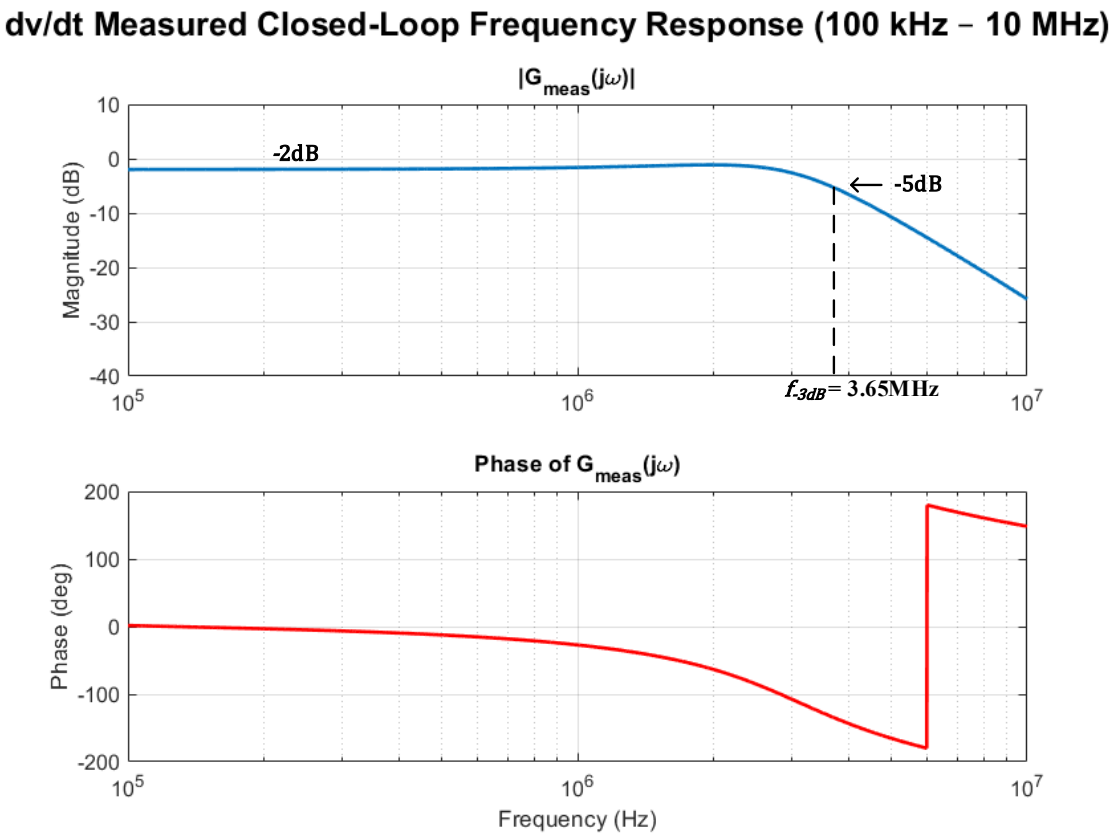


Figure 3.14: Frequency response of measured closed-loop transfer function $G_{dv,meas}(s)$.

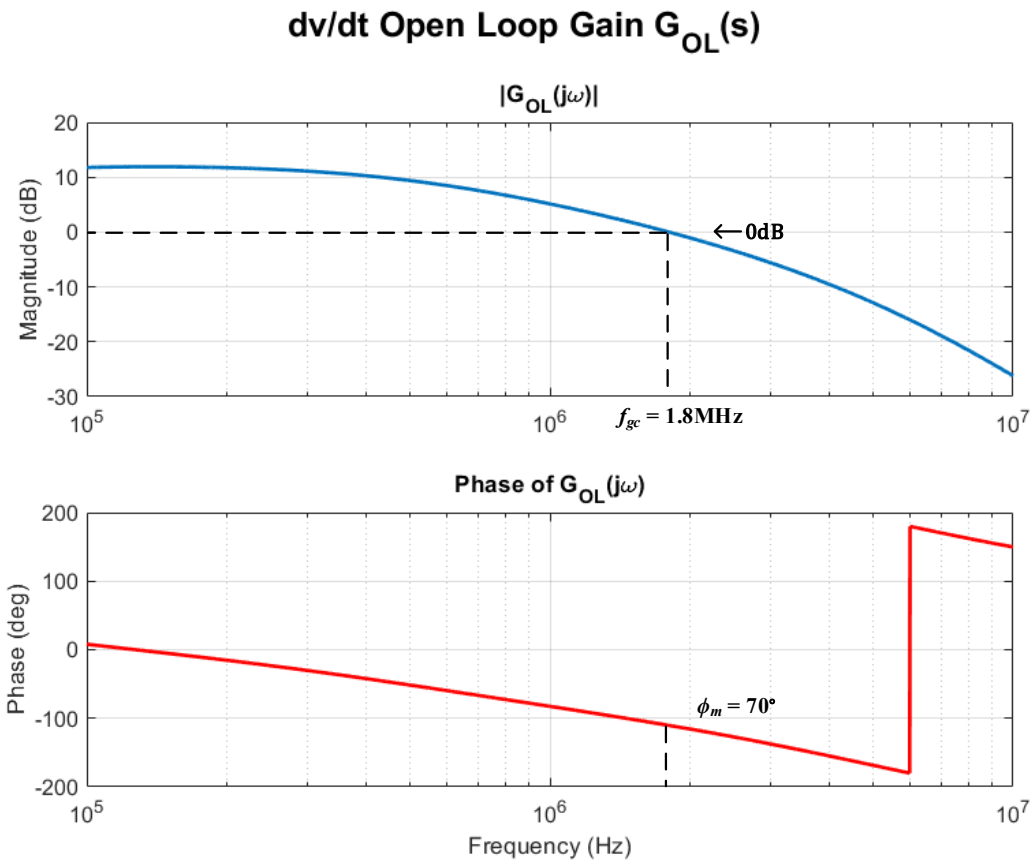


Figure 3.15: Frequency response of open-loop transfer function $G_{dv,OL}(s)$.

Table 3.2: Loop gain and stability metrics for dv_{CE}/dt control

Parameter	Value
-3dB closed-loop bandwidth	3.65 MHz
$G_{dv,\,OL}(s)$ Gain crossover frequency	1.8 MHz
Phase margin (ϕ_m)	70°
Gain margin (G_m)	15 dB

In principle the experimental verification of the developed small signal model has to be done using the frequency response measurements of the developed dv/dt and di/dt control loop. However this requires the biasing of the IGBT in active region of operation and injecting a

perturbation signal to measure the response. Operating the IGBT in the active region results in significant power dissipation. Hence, direct frequency measurements are challenging in practice.

The experimental results also serve to indirectly validate the small signal models developed in this study. The measured dynamic responses, including dv/dt and di/dt characteristics, show good agreement with the predictions from the small-signal model. In particular, the observed bandwidth and damping trends are consistent with the frequency-domain analysis, confirming that the proposed small-signal representations accurately capture the dominant dynamics of the system within the operating range.

3.4 Summary of Contributions

- **Development of Active Gate Drive (AGD) scheme**: A systematic methodology for designing an AGD scheme for controlling di_C/dt and dv_{CE}/dt in series parallel connected IGBTs during switching.
- **Theoretical foundation for AGD**: A comprehensive study of the principles governing AGD is presented.
- **Standardized Active Switching Module (ASM)**: Introduce a modular, scalable ASM architecture that enables flexible deployment across various MVDC applications.
- **Experimental validation of AGD**: Conducted experimental studies demonstrating the di_C/dt and dv_{CE}/dt control capability using AGD.
- **Small-signal modeling of the AGD control:** Developed linearized dynamic models that characterize the AGD behaviour during di_C/dt and dv_{CE}/dt control, enabling analytical evaluation of the device-controller interaction.
- **Stability and gain-limit assessment:** Analyzed the frequency response of the derived transfer functions to determine the stability margins, bandwidth constraints, and performance limits of the proposed AGD scheme.

Chapter 4: ASM-HCB Architecture and Testing

This Chapter discusses the proposed ASM-HCB architecture and its operating principle. A unidirectional HCB prototype was developed and tested at rated voltage and current to evaluate the performance of ASMs in the proposed HCB architecture. The steady-state and transient thermal characteristics of the proposed ASM-HCB architecture are evaluated using thermal design procedures. Furthermore, this chapter presents thermal design guidelines for ASM-based HCB systems.

4.1 Standardized ASM Based HCB Architecture

A Hybrid Circuit Breaker (HCB) configuration, featuring a Mechanical Switch (MS) and a Current Commutation Switch (CCS), is utilized within the primary conduction branch in this study. The Main Breaker (MB) unit is the current-making/breaking unit during HCB turning on and off. CCS assists the current breaking operations by commutating the current to and from the MB unit during turning off and on operations of the HCB. This allows the MS to close with minimal arc voltage and to close its contacts at zero current.

Figure 4.1 (a) illustrates the schematic of a hybrid type DCCB. The turn-on and turn-off sequences of the hybrid DCCB are presented in Figure 4.1 (b) and (c), respectively. The current-making and current-breaking actions of the hybrid DC circuit breaker represent the periods during which the device is subjected to its highest electrical stresses, both in terms of network current and voltage. Hence, these transition intervals are the primary focus of the AGD scheme, in which the di_C/dt and dv_{CE}/dt control loops are actively engaged to regulate the IGBT dynamic behavior [71].

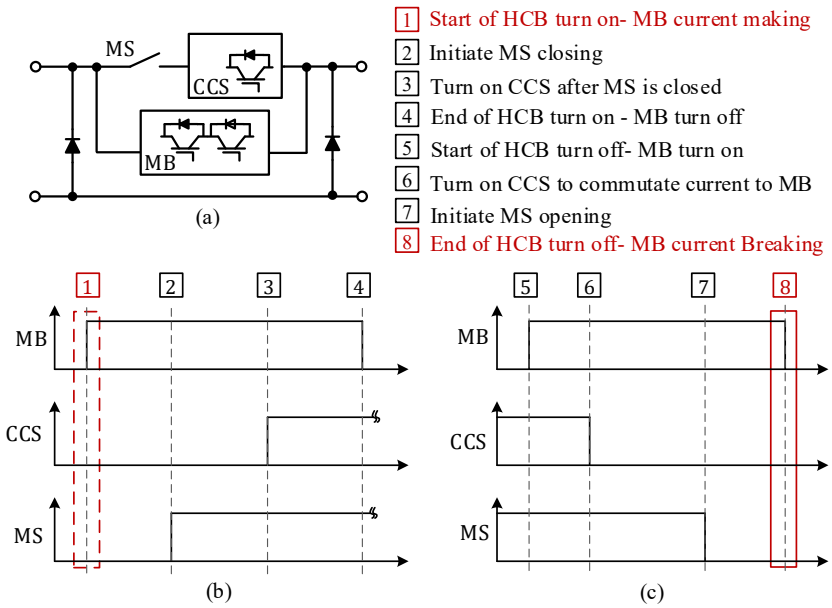


Figure 4.1: (a) Hybrid CB, (b) HCB turn-on sequence, (c) HCB turn-off sequence.

The proposed HCB architecture enables scalability by allowing the addition of standardized ASM units in series and parallel and is shown in Figure 4.2. This scalability can be tailored to meet the application's specific voltage and power level demands. With a wide range of MVDC applications requiring varying voltage and power levels, the scalable DCCB architecture, utilizing standardized ASMs, provides a flexible DC protection solution. The freewheeling diode provides a continuous current path during the energy dissipation process after current interruption.

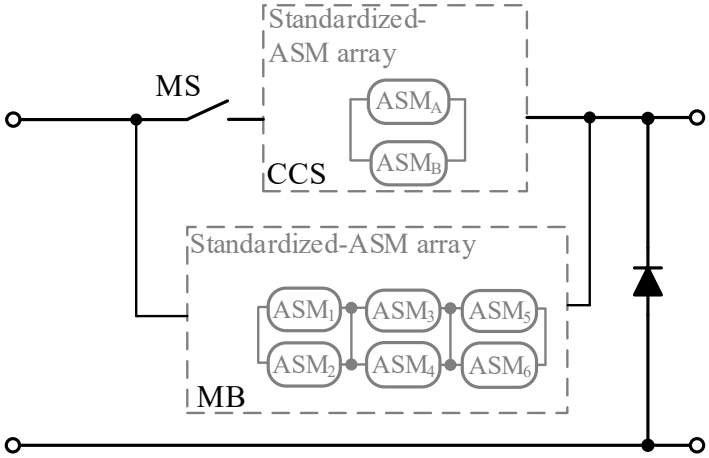


Figure 4.2: Standardized ASM-based DCCB architecture.

4.1.1 2kV/100A Hybrid DC breaker: Test Prototype

The schematic of the 2kV/100A ASM-based HCB developed for testing is shown in Figure 4.3. The current commutation switch consists of two parallel ASMs (ASM_A and ASM_B) to achieve equal current sharing. The MB unit consists of six series and parallel-connected ASMs, as shown in Figure 4.2. ASMs connected in series share voltage during current interruption operations and when HCBs are turned off. Similarly, parallel-connected ASMs in the MB unit share current when the current path is commutated through the MB unit until the current interruption occurs.

At current interruption the network energy stored up should be dissipated. The diode freewheeling path facilitates current to decay naturally through freewheeling path and resistive elements of the circuit. This approach is effective for the scale of test setup employed in this study, and freewheeling current decays in a short duration dissipating the stored energy in the cables. However, for high energy MVDC networks, supplementary energy absorption methods such as MOVs and active dissipation methods are required for faster current decay. Furthermore, the developed HCB protype is placed close to the source and the source side network inductance is considered negligible in this study.

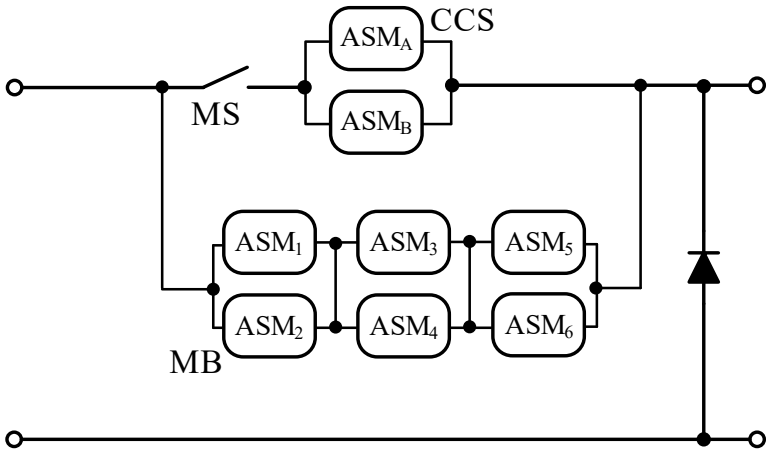


Figure 4.3: Schematic diagram of the 2kV/100A MVDC HCB prototype.

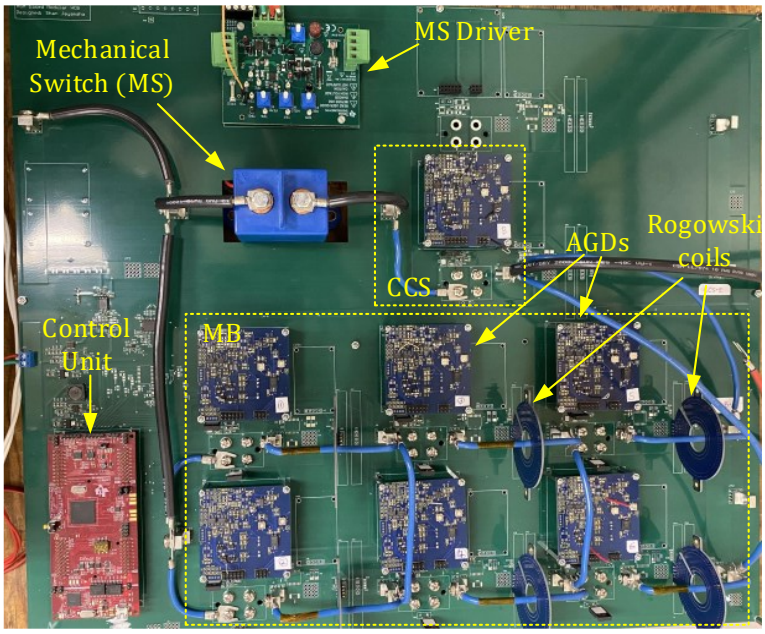


Figure 4.4: 2kV/100A HCB prototype based on ASM-HCB architecture.

The 2kV/100A unidirectional HCB prototype developed based on the proposed HCB architecture is shown in Figure 4.4. The test procedure for dynamic switching of the HCB and the test setups is discussed in the following section.

4.2 Test Procedure and Setup for Testing the 2kV-100A Hybrid DC Breaker Prototype

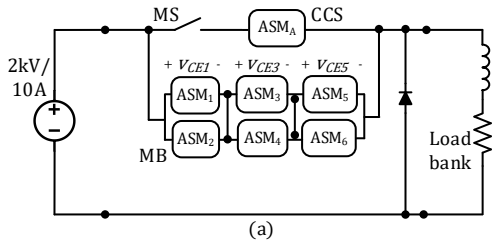
Testing the developed HCB prototype over its complete operating range of voltage and short-circuit current is impractical due to the high cost of DC sources and loads capable of the rated voltage and short-circuit current. The test procedures discussed in this section were developed based on the DC breaker test setups discussed in Section 2.2.2.

4.2.1 High Voltage Low Current Testing (2kV/10A)

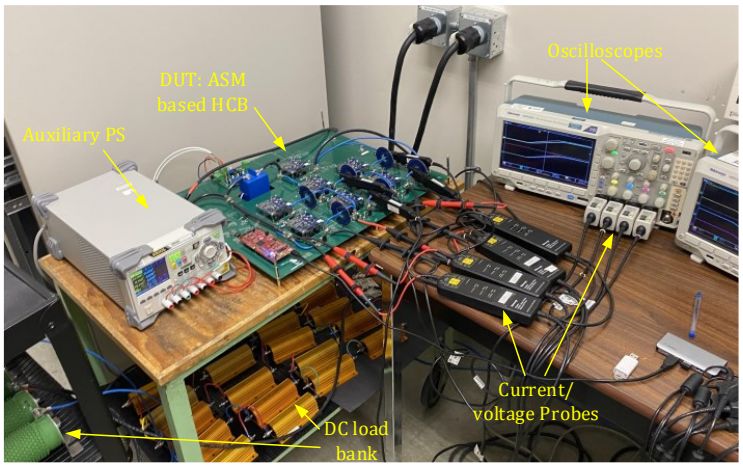
This experiment aims to evaluate the voltage-sharing capability of the ASMs in the HCB architecture. The schematic and the experimental setup for 2kV/10A testing of the HCB are shown in Figure 4.5 (a) and (b). Figure 4.6 (a) illustrates the voltage sharing between series-

connected ASMs and the current sharing between each parallel ASM pair during MB turn-off, specifically, during HCB turn-off with inductive loads. The inclusion of freewheeling diodes provides an energy dissipation path during the HCB turn-off. Figure 4.6 (b) shows the voltage and current sharing between ASM units in the MB during turn-on. A non-inductive load is used in this test to assess the current-sharing capability during a rapid current rise through the MB unit.

The test results shown in Figure 4.6 demonstrate a homogeneous current and voltage distribution across the ASMs in the proposed HCB architecture, with minimal deviations, indicating robust current and voltage sharing capabilities. The 2kV test voltage (V_{TEST}) is equally shared between the series-connected IGBTs of the MB during both turn-on and turn-off. Similarly, the network current is shared between parallel-connected IGBT pairs, demonstrating the dynamic voltage and current-sharing capabilities of ASMs in the HCB.



(a)



(b)

Figure 4.5: (a) Schematic of MV test setup for HCB testing, (b) Experimental setup.

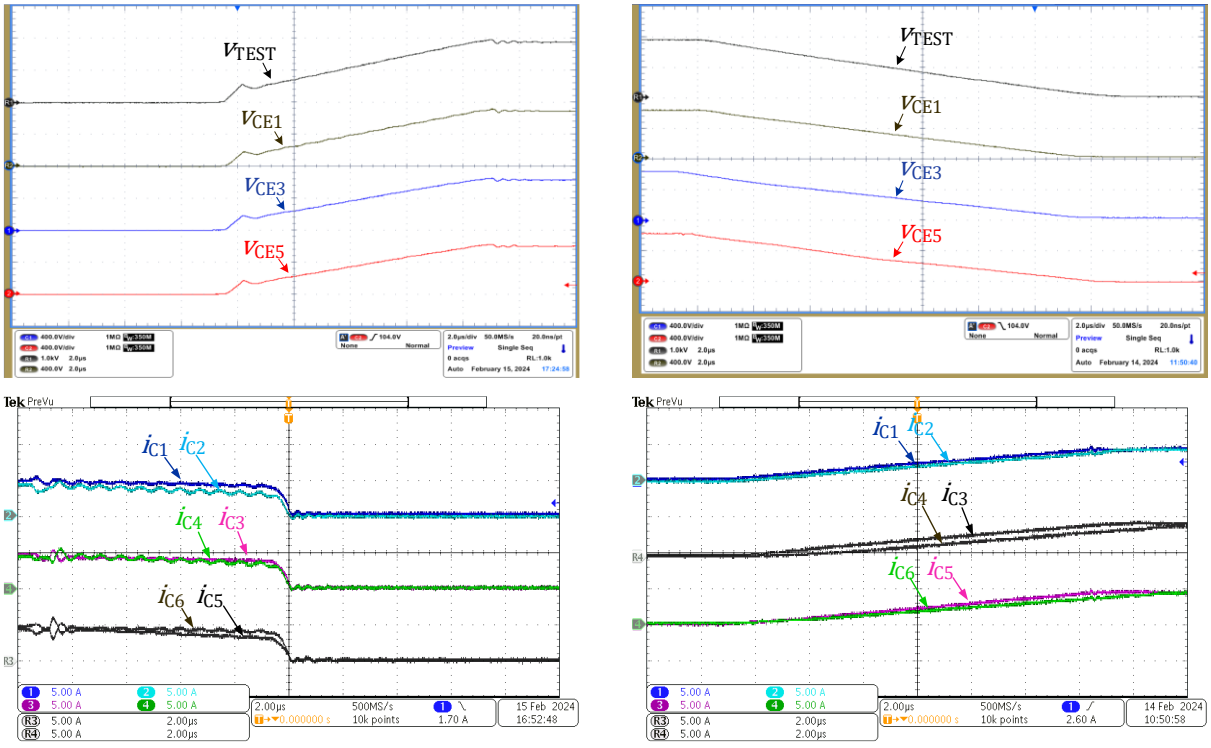


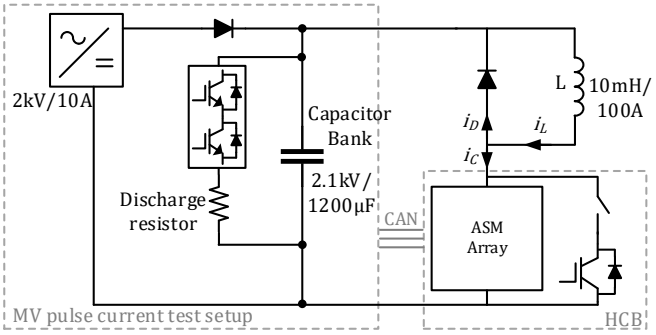
Figure 4.6: Voltage and current sharing between ASMs during (a) MB turn-off (in the course of HCB turn-off), (b) MB turn-on (in the course of HCB turn-on).

4.2.2 High Voltage Pulse Current Testing (2kV/100A)

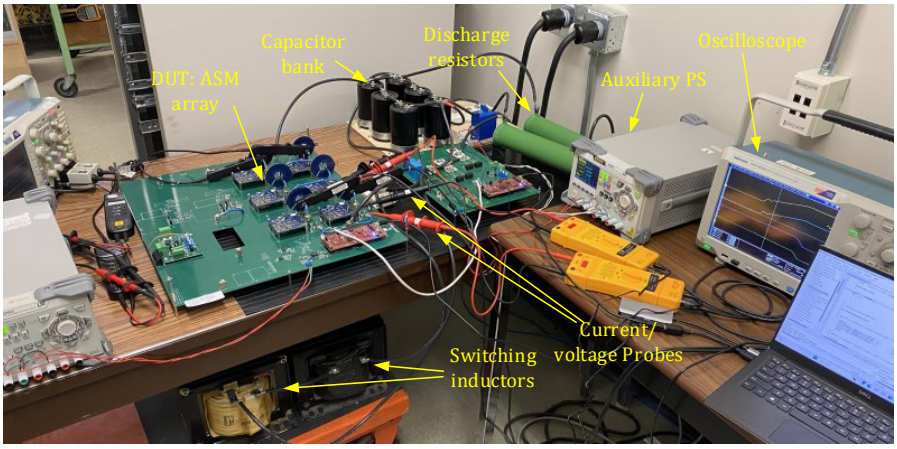
Figure 4.7 (a) and (b) show the schematic and experimental setup for high voltage pulse current testing. A high voltage capacitor bank is used to supply a pulse current at the rated HCB voltage. A high voltage, low current power supply charges the capacitor bank. A high voltage IGBT array discharges the capacitor bank after the pulse test. The capacitor bank can source a pulse current for several hundred microseconds without a significant voltage drop. The current-breaking operation of the MB unit under rated voltage and current, and the commutation from the main conduction branch to the MB unit, are evaluated.

Considering the time it takes the MS to close and open its contacts, to fully test the on-off operation of the HCB, the capacitor bank should be able to source a current pulse for a few tens of milliseconds. This requires a larger capacitor bank and a capacitor charging power supply.

Figure 4.8 (a) and (b) show the experimental results during MB turn-off and turn-on, respectively. During both turn-on and turn-off dynamics, the test voltage (V_{TEST}) of 2kV is shared equally among three series-connected IGBTs. Similarly, during the dynamic current rise and fall stages, the test current of 100A is shared equally among all three pairs of ASMs, as shown in Figure 4.8. The experiment results illustrate the capability of the proposed ASM modules to share the voltage and current stress within the proposed HCB architecture. The di_C/dt and dv_{CE}/dt control periods are approximately 12 µs and are well within the SOA requirements of each IGBT.



(a)



(b)

Figure 4.7: (a) Schematic of the MV pulse current test setup for ASM array testing, (b) Experimental setup.

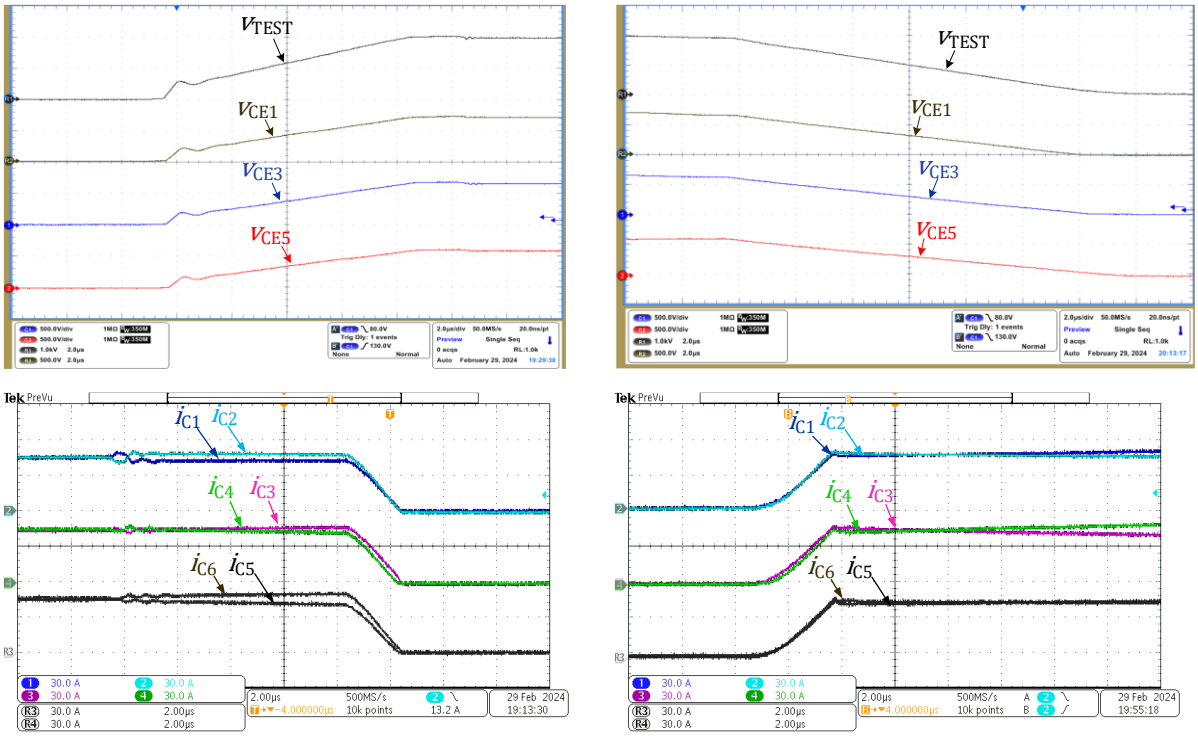


Figure 4.8: Voltage and current sharing between ASMs during (a) MB turn-off (in double pulse switching), (b) MB turn-on (in double pulse switching).

4.3 Electrothermal Design and Steady State Characteristics of HCBs

4.3.1 HCB Steady State Current Balance and Thermal Design

When the HCB is fully on, the current flows continuously through the CCS. The heat dissipated by the IGBTs in the CCS is the IGBT conduction power loss. Due to the Positive Temperature Coefficient (PTC) of IGBTs, their on-state resistance increases with increasing junction temperature. Thus, an efficient cooling system design capable of dissipating the produced heat is necessary [63], [67], [74].

The proposed HCB architecture utilizes a parallel connection of IGBTs to accommodate the steady-state current. Steady-state current sharing among parallel-connected IGBTs is a crucial requirement. The imbalance in current sharing among parallel IGBTs is caused by mismatches in IGBT device characteristics. Even IGBTs manufactured within the same production batch exhibit variations in output characteristics due to manufacturing tolerances inherent in semiconductor fabrication processes. These differences can lead to unequal turn-on resistances ($R_{CE,on}$), affecting current sharing in parallel configurations. For two IGBTs that exhibit differing $R_{CE,on}$ values, their on-state collector-to-emitter voltages ($V_{CE,on}$) will vary for a given current level. When these IGBTs are connected in parallel, the $V_{CE,on}$ is forced to be the same for both IGBTs. Thus, one IGBT will carry more current than the other, resulting in a higher junction temperature that may exceed the rated junction temperature [49], [63], [64].

The positive temperature dependence of the IGBTs helps stabilize the current imbalance. IGBTs operating in the PTC region increase $V_{CE,on}$ with increasing junction temperature, whereas those with a negative temperature coefficient decrease $V_{CE,on}$ with increasing junction temperature. Therefore, it is considered good practice to operate the IGBT within its positive temperature coefficient region, as this facilitates natural steady-state current balancing among parallel devices and mitigates the risk of thermal runaway [74], [75], [76].

4.3.2 Thermal Network Model for Current Commutation Switch of HCB

Electrothermal models can be used to predict the heat flux and the temperature distribution of power electronic devices. One such electrothermal modeling approach is the use of an equivalent thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) model. Figure 4.9 shows the equivalent thermal model for the CCS.

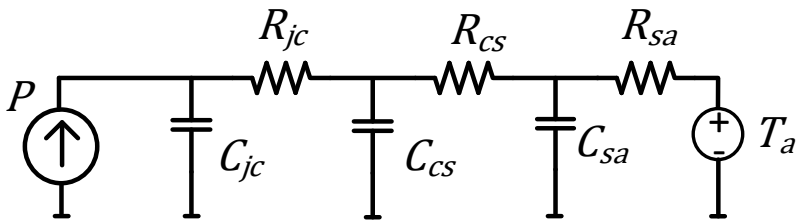


Figure 4.9: Equivalent thermal network for representing the heat flow from IGBT junction to the ambient.

The physical parameters of the heat sink, such as size, shape, and material, affect the IGBT's steady-state current limit. The maximum heat loss ($P_{dissip,\ max}$) and the maximum steady-state collector current ($I_{C,max}$) as a function of the heat sink's thermal resistance can be approximated by the following equation.

$$P_{dissip,max} = \frac{T_j - T_a}{R_{TH,j-a}} \tag{4.1}$$

Here, T_j is the maximum rated junction temperature, T_a is the operating ambient temperature, and $R_{TH,j\text{-}a}$ is the cumulative thermal resistance from junction to ambient. The main parameter that determines the physical current limit of the IGBT is the $R_{TH,j\text{-}a}$.

The $I_{C,max}$ for selected $R_{TH,j\text{-}a}$

$$I_{C,max} = \sqrt{\frac{T_j - T_a}{R_{TH,j-a} \times \frac{\Delta V_{CE,on}}{\Delta I_C}}} \tag{4.2}$$

Here, $\Delta V_{CE,on}/\Delta I_C$ is the gradient of IGBT output characteristics in the linear region of operation for a given V_{GE}.

For multiple IGBTs connected in parallel to carry current;

$$I_{C,max} = \sqrt{\frac{n^2 \times T_j - T_a}{R_{TH,j-a} \times \frac{\Delta V_{CE,on}}{\Delta I_C}}} \tag{4.3}$$

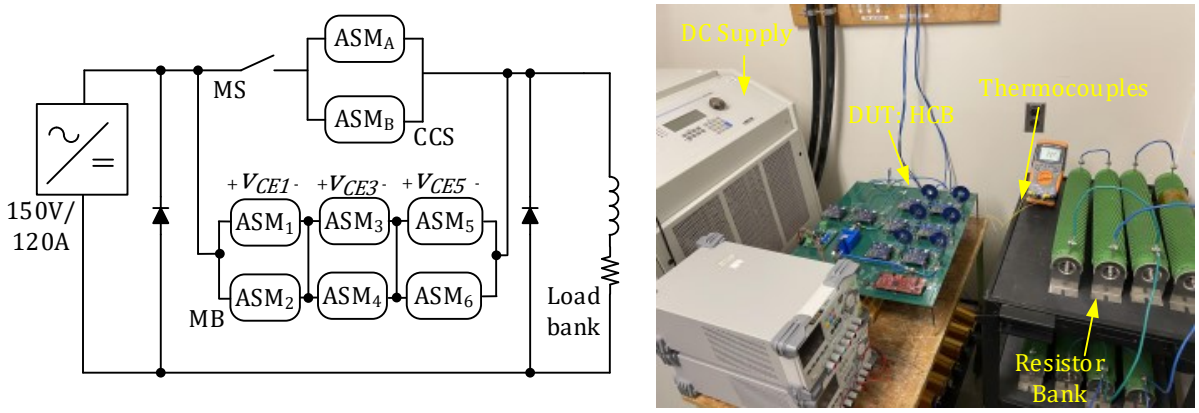
Here, n is the number of parallel-connected IGBTs. It is assumed that T_j, T_a, $R_{TH,j\text{-}a}$, $\Delta V_{CE,on}$, ΔI_C values of all parallel-connected IGBTs are equal.

4.3.3 Steady State Thermal Characterization of HCB: Experimental Verification

The schematic and the experimental test setup used for steady-state thermal characterization are shown in Figure 4.10 (a) and (b). Heat sinks with cooling fans are used to cool the CCS IGBTs, as shown in Figure 4.11. The cooling system parameters are listed in Table 4. 1. K-type thermocouples are used to measure the IGBT case temperature at the thermal equilibrium point.

Table 4. 1: CCS Cooling System Parameters.

Parameter	Symbol	Value
Heat sink to ambient thermal resistance (With forced airflow)	$R_{c\text{-}s}$	0.6˚C/W
Air flow speed	-	550 ft/min
IGBT junction to case thermal resistance	$R_{j\text{-}c}$	0.15 ˚C/W
Ambient temperature	T_a	22˚C
IGBT junction temperature thermal limit	$T_{j,max}$	150 ˚C



(a) (b)

Figure 4.10: (a) Schematic diagram, and (b) Experimental setup for steady-state thermal characterization of the proposed HCB.

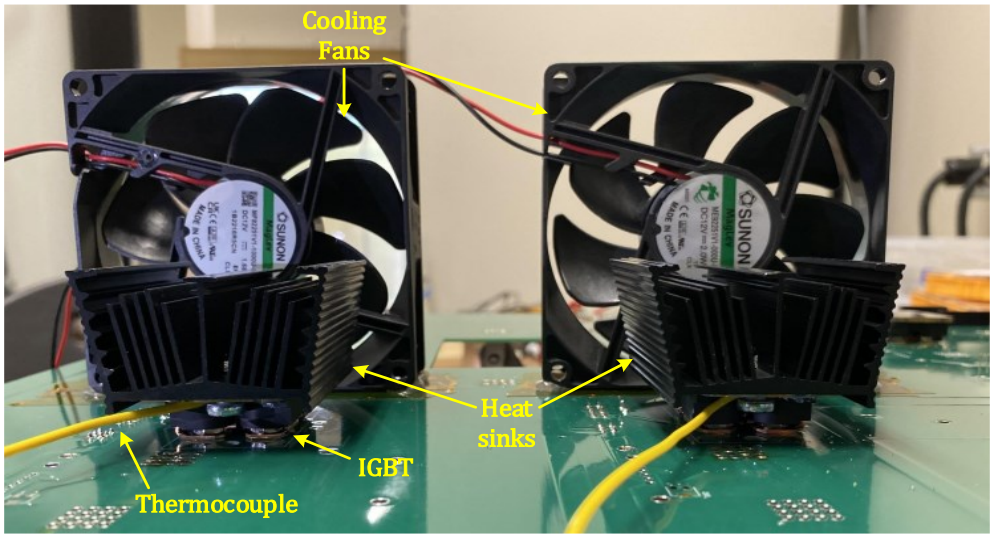
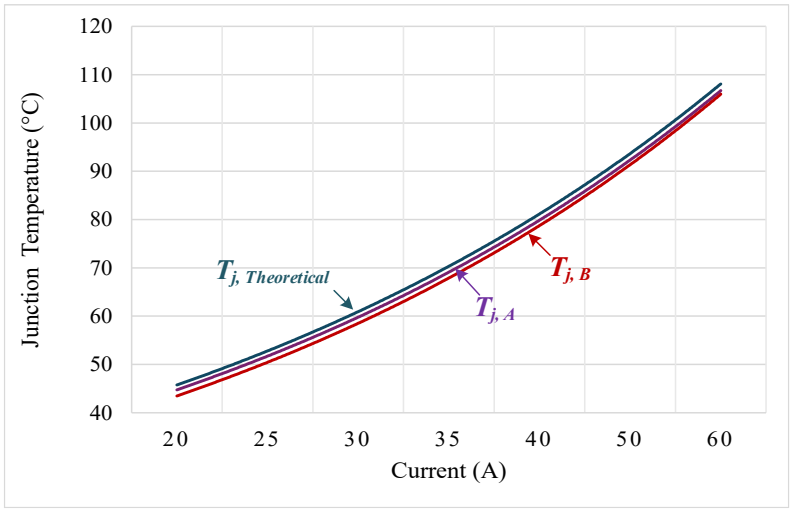


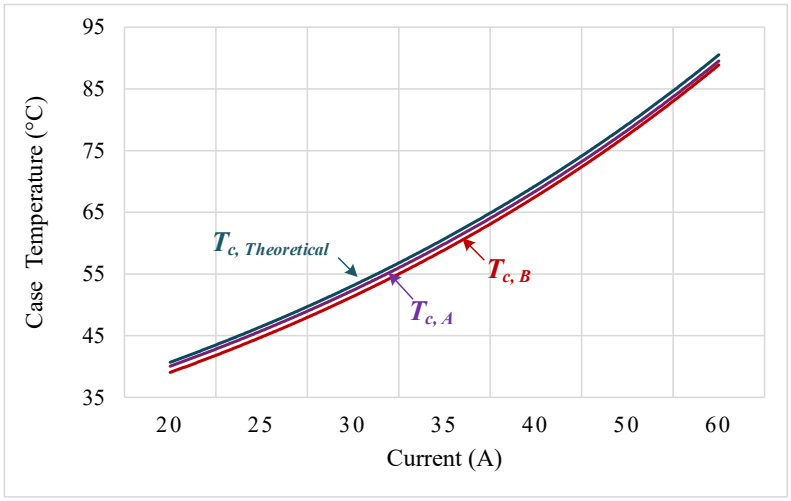
Figure 4.11: Cooling arrangement used for the IGBTs in CCS.

The variation of steady-state conduction losses and junction temperature under varying steady-state breaker currents is evaluated using the experimental setup shown in Figure 4.10. The steady-state case temperature (T_c) is measured at the thermal equilibrium point after the HCB is turned on. Thermal equivalent circuit calculations are used to determine the junction temperature (T_j) from measured case temperatures.

The comparison of theoretical and measured junction and case temperatures at varying loading levels is shown in Figure 4.12. It can be seen that the measured junction and case temperatures closely follow the theoretical junction and case temperatures ($T_{j,Theoretical}$ and $T_{c,Theoretical}$). Furthermore, the junction temperatures are within the safe thermal limits, supplying the nominal current of the HCB. This confirms the accuracy of the proposed thermal design procedure and its suitability for reliable long term operation under rated conditions.



(a)



(b)

Figure 4.12: Comparison of theoretical and measured (a) junction and (b) case temperatures, under different load levels.

4.3.4 Transient Thermal Impedance of IGBTs

In a fault condition, the current through the HCB can be several times the nominal current. During this period, the device's junction temperature may exceed its maximum limit, potentially damaging it. The IGBT junction-to-case transient thermal impedance ($Z_{TH,j\text{-}c}$) determines the transient increase in junction temperature during a short pulse current [77], [78].

Typically, the $Z_{TH,j\text{-}c}$ curve as a function of pulse duration and duty cycle shows that $Z_{TH,jc}$ converges to $R_{TH,j\text{-}a}$ with increasing pulse duration. Hence, by replacing $R_{TH,j\text{-}c}$ in Equation (4.3)

with $Z_{TH,j\text{-}c,}$ the maximum transient current with n number of parallel IGBTs can be calculated. The minimum transient current with n number of parallel IGBTs is;

$$I_{f\,(\max)} = \sqrt{\frac{n^2 \times (T_j - T_c)}{Z_{TH,j-c} \times \frac{\Delta V_{CE,on}}{\Delta I_C}}} \tag{4.4}$$

Here $\frac{\Delta V_{CE,on}}{\Delta I_C}$ is the on-state resistance of the IGBT under the anticipated fault current and junction temperature conditions and can be approximated from the IGBT output characteristic curve.

For transient fault conditions the junction temperature rise was evaluated using $Z_{TH,j\text{-}c}$. This approach is justified as the fault duration is typically very short (in the ms range), and the generated heat is largely confined within the semiconductor chip and module package. Only negligible amount of heat is transferred to the heatsink, and heatsink temperature remains unchanged. However, an efficient heat sink design lowers the junction and case temperatures, thereby increasing the thermal margin available for surviving transient fault currents.

An accurate fault simulation with an equivalent thermal model is used to obtain a precise estimate of the transient thermal requirements of the HCBs pertaining to MVDC network faults [78].

The number of required IGBTs for the CCS is calculated considering both steady-state and transient fault currents. The higher value n obtained from the steady-state and transient current evaluations is adopted to ensure thermal stability across all operating conditions.

4.3.5 Transient Thermal Performance of CCS Under Faults

DC network fault rises fast, limited only by the line inductances and resistance. During the fault duration, the conduction losses of the CCS IGBTs will be excessively high. The IGBTs

employed should withstand the transient increase in junction temperature. Hence, CCS IGBTs operating in steady state should have sufficient thermal margin to undergo thermal transients without exceeding their safe thermal limits.

Heat transfer from the IGBT junction to the heatsink usually takes a few milliseconds [77]. Hence, IGBTs have a limited capability to handle fault currents. Furthermore, the thermal equilibrium point of the CCS IGBT plays a crucial role in the short-circuit withstand capability of the IGBTs. In addition, the fault detection and interruption times are determining factors for the fault current-handling capability of the CCS IGBTs.

PLECS simulation is used to evaluate the transient thermal performance of the CCS IGBTs of the developed HCB prototype. The thermal model of the IGBT, *VS-GT90SA120V*, is imported into PLECS, and a transient fault simulation is carried out to determine the thermal limits for handling fault currents.

The PLECS simulation model used to evaluate the transient thermal performance of the CCS is shown in Figure 4.13. The fault is applied once the CCS IGBTs reach the thermal equilibrium. A fault detection time of 10ms and a maximum fault current level ($I_{f,max}$) of 3.5 times the nominal current is considered for the thermal simulation.

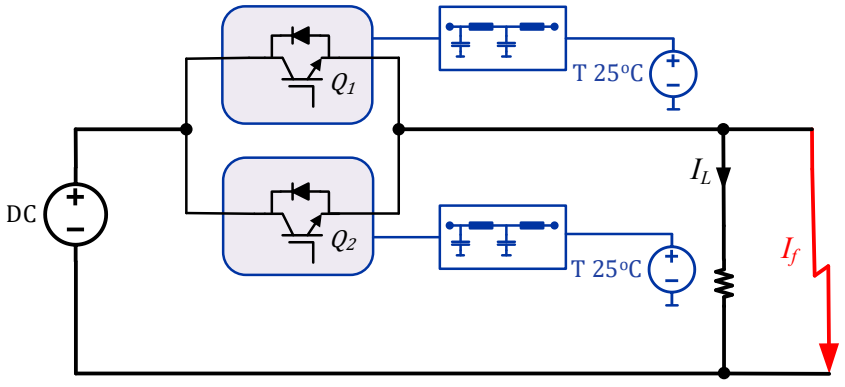


Figure 4.13: PLECS simulation model for evaluating the transient thermal performance of the CCS.

The simulated transient thermal behavior is shown in Figure 4.14. Since the current commutation from CCS to the MB unit takes only a few microseconds, the fault detection time is considered equivalent to the fault current duration in this study. It can be seen that during transient fault current, the IGBT junction temperature does not exceed the thermal limit of 150° C. To withstand higher fault currents or accommodate longer fault durations before detection, the number of parallel IGBTs needs to be increased according to Equation (4.4).

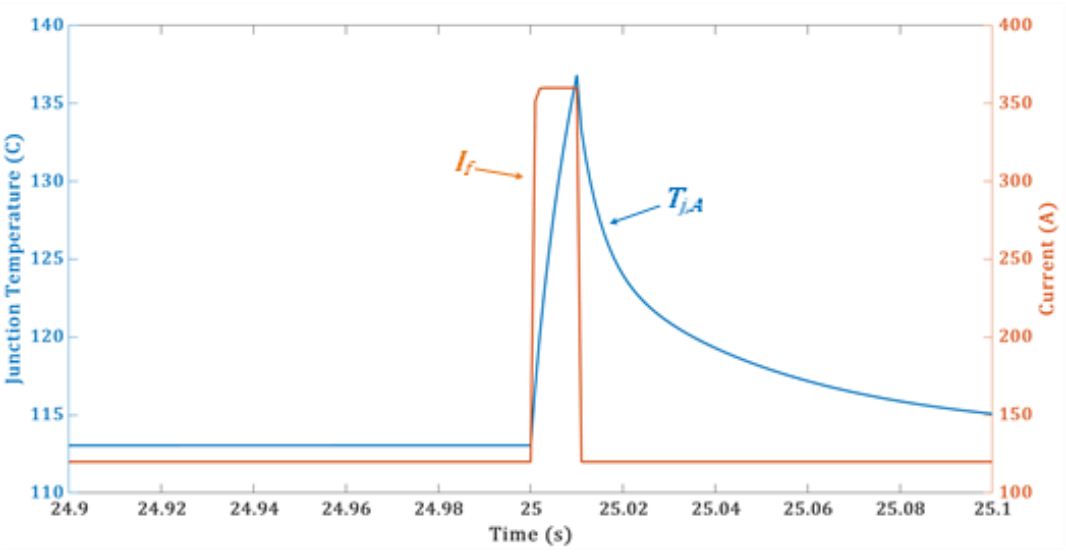


Figure 4.14: Transient thermal behavior of CCS IGBTs under network fault current.

4.3.6 Steady State Current Imbalance

Even though the positive temperature coefficient of IGBTs helps stabilize the current imbalance, it does not guarantee complete thermal stability. Additional measures are required to compensate for the current imbalance among parallel IGBTs resulting from device mismatches. Chapter 5 presents the Active Current Balancing (ACB) technique, proposed to eliminate steady-state current imbalance among parallel IGBTs.

4.4 Summary of Contributions

- **Proposed ASM-HCB architecture**: Introduction of a modular HCB architecture based on ASMs, enabling a scalable and flexible protection solution of MVDC networks.
- **HCB prototype development and validation**: Development of a scalable HCB prototype to experimentally validate the proposed ASM-based HCB architecture.
- **Steady state and transient thermal analysis**: Evaluation of steady state and transient thermal characteristics of HCBs using experimental studies.
- **Guidelines for thermal design**: Development of thermal management design guidelines for ASM-HCBs, and experimental validation.

Chapter 5: Active Current Balancing for Parallel Connected IGBTs under Steady State Operation.

Due to the unmatched impedance of each IGBT connection and variations in IGBT parameters, $V_{CE,on}$ varies among parallel IGBTs. Hence, current sharing between parallel IGBTs is not achieved naturally. Various approaches have been proposed to achieve steady-state current balance in parallel-connected IGBTs. Most of these approaches focus on derating the IGBTs used and selecting the semiconductor devices to facilitate natural current sharing between parallel IGBTs [49], [62], [63], [67], [79]. Hence, there is a necessity for an Active Current Balancing (ACB) scheme to ensure equal current sharing in the steady state. This chapter presents the development and validation of an innovative architecture for steady-state current balancing in MVDC circuit breaker applications.

5.1 Active Current Balancing (ACB) Concept

The proposed AGD controller in Chapter 3 is effective only during the dynamic voltage and current slope period, since the rates of change of collector current (di_C/dt) and collector-to-emitter voltage (dv_{CE}/dt) are zero in steady state. Therefore, without di_C/dt and dv_{CE}/dt feedback, the AGD functions as a resistive gate drive [71], [72].

Steady state current balancing between parallel-connected IGBTs in the CCS is an essential requirement for the reliable operation of HCBs [1], [67], [71], [79]. This cannot be achieved by the dynamic di_C/dt and dv_{CE}/dt control action of the proposed AGD. Hence, requires a separate control scheme, which is proposed in this chapter.

5.1.1 ACB Controller

Typical output characteristics of two distinct IGBTs are shown in Figure 5. 1. The on-state collector to emitter voltage ($V_{CE,on}$) can be actively regulated by adjusting the gate to emitter voltage (V_{GE}). The proposed ACB scheme leverages this property to achieve a steady-state current balance among parallel-connected IGBTs. Monitoring the current imbalance enables us to dynamically adjust the V_{GE} to mitigate it.

If the V_{GE} of $IGBT_2$ is reduced, the resulting on-state resistance increases, thus reducing the current through $IGBT_2$. This will increase the current through $IGBT_1$. Alternatively, an increase in V_{GE} of $IGBT_1$ will decrease the IGBT's on-state resistance. Considering the voltage drop across the two IGBTs is identical, the current through $IGBT_1$ will increase, resulting in a decrease in the current through $IGBT_2$. The variation in IGBT operating points is shown in Figure 5. 1. By using this principle, V_{GE} can be dynamically adjusted to mitigate current imbalances.

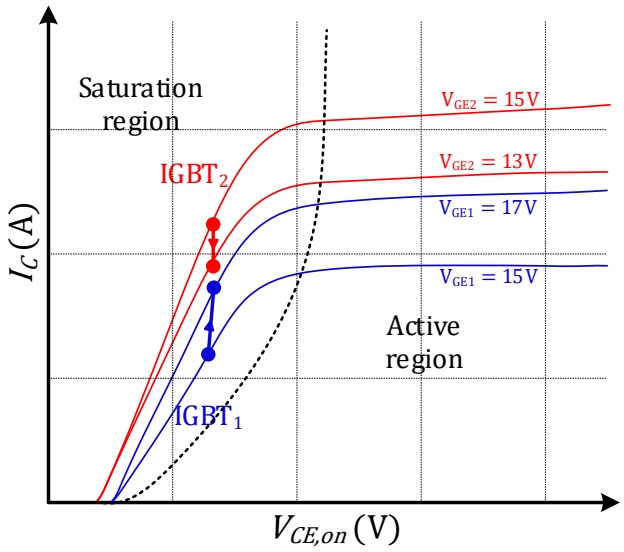


Figure 5. 1: IGBT output characteristics, and variation of IGBT operating point in response to a change in gate-emitter voltage (V_{GE}).

The proposed ACB scheme is based on the following key conditions for safe operation.

- The V_{GE} of the IGBT should be within the specified limits [67], [76].
- To prevent the IGBT from moving into the active region in steady state operation, V_{GE} should not be reduced below a limit determined by the IGBT output characteristics [63], [67].
- The PTC of the IGBT helps stabilize the current imbalance. Operating the IGBT within the PTC region inherently self-balances the current among parallel IGBTs [23], [74].

The proposed scheme does not necessitate high-speed control action, as it primarily targets steady-state current sharing among parallel IGBTs. The schematic shown in Figure 5.2 illustrates the digital implementation of the ACB controller. This architecture enables closed-loop regulation of the gate-emitter voltage (V_{GE}) for each IGBT, thereby facilitating precise control of current sharing among devices connected in parallel. While the ACB controller adjusts the on-state gate voltage ($V_{GE,on}$), the AGD controls the current flowing into the gate during IGBT turn-on and turn-off operations [71]. Hence, by design, ACB and AGD have independent control action on the IGBTs.

As shown in Figure 5.2, the ACB is implemented using a Digital Signal Processor (DSP), which executes the core control algorithm. The DSP processes real-time current measurements from a Hall-effect current sensor to calculate the current imbalance between parallel IGBTs. The proposed ACB requires an active communication link between DSPs of the parallel IGBTs to transmit and receive measured current values. A Proportional-Integral (PI) controller is used in the ACB scheme. The digital control signal is converted to an analog voltage reference using a biasing Digital-to-Analog Converter (DAC) to control the Low-Dropout (LDO) regulator's

output voltage (V_{CC}). A high-precision, adjustable-voltage LDO is used to control V_{CC} with fine resolution.

The control block diagram for ACB in *n* parallel-connected IGBTs is shown in Figure 5.3. The control objective is to eliminate the steady-state current imbalance between IGBTs by adjusting the IGBT on-state V_{GE} by changing the V_{CC}, as shown in Figure 5.3.

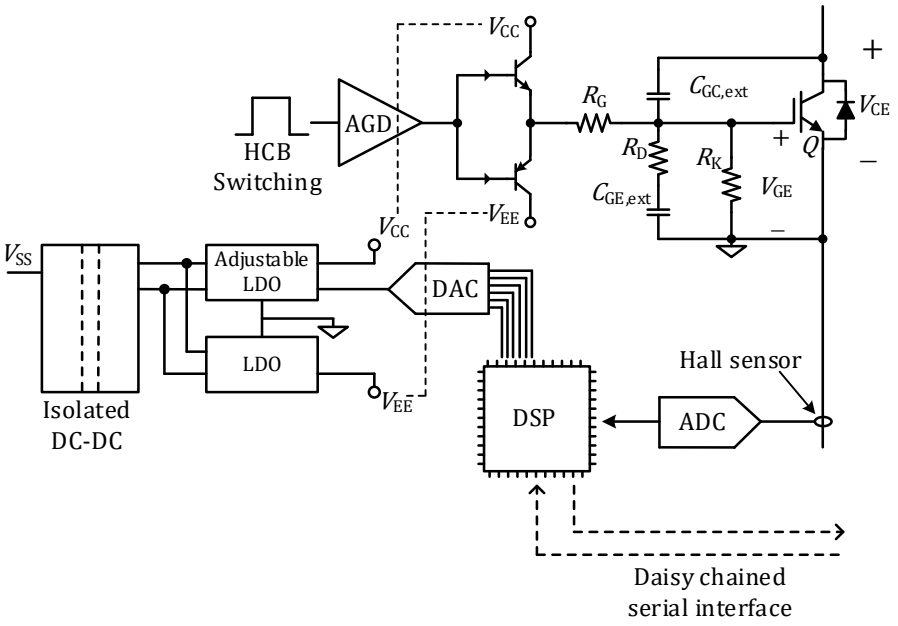


Figure 5.2: Schematic of the proposed ACB controller for current balancing in parallel IGBTs.

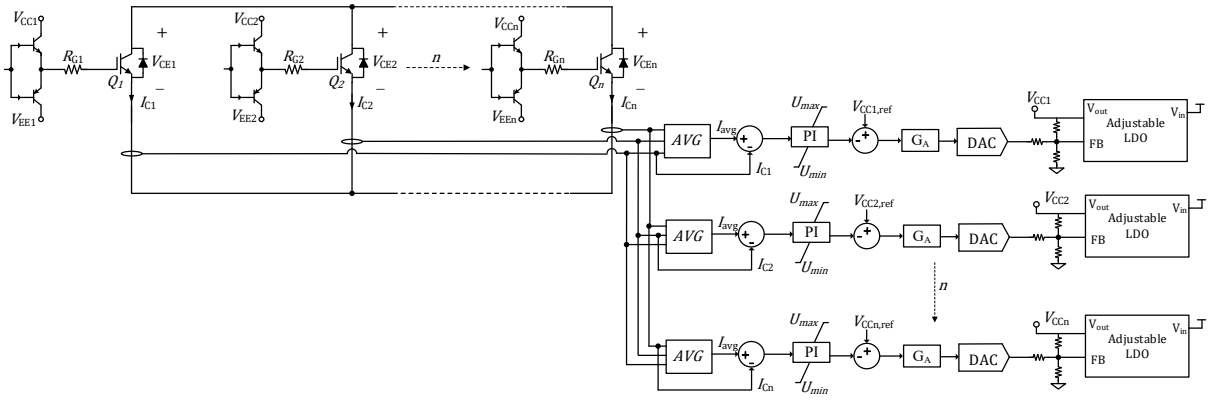


Figure 5.3: Control block diagram for current balancing between *n* parallel IGBTs.

To avoid control interactions with AGD, the control speed of the PI controller is set significantly slower than AGD. The separation of control timescales between ACB and AGD enables stable operation, allowing ACB to perform fine-tuned steady-state current equalization without affecting the fast-switching actions governed by AGD. This independent control strategy eliminates the need to switch between controllers during different phases of IGBT operation, thereby simplifying the overall control architecture, and will be further discussed in Section 5.5.

Even though Figure 5.3 illustrates PI controller for each *n* parallel IBGTs, only *n-1* current sharing states are independent because the sum of all IGBT currents are constrained by network current. Hence, the control structure contains one redundant current balancing loop. However, the ACB speed is intentionally very slow and is only active during imbalance correction. As a result, no integrator interaction associated with redundant control loop is observed experimentally.

Alternatively, equivalent reduced order formulation with *n-1* controller can be employed in the proposed ACB control structure. However, it would require additional coordination logic to reconstruct the remaining gate-voltage command from the other controller outputs.

5.1.2 Effect of Temperature Feedback on the Proposed ACB

The output characteristics of an IGBT depend on the junction temperature. Changes in junction temperature of an IGBT result in gradual changes in collector current. These temperature feedback phenomena are slow and insufficient for correcting the current imbalance [23], [79].

The output characteristics of the IGBTs with varying junction temperatures are shown in Figure 5.4. The on-state voltage $V_{CE,on}$, increases with increasing junction temperature, as the

IGBT has a positive temperature coefficient. A high positive temperature coefficient will facilitate better current sharing, but will also increase power dissipation at higher power levels.

In the proposed ACB control, adjusting the gate drive voltage to control the collector current essentially increases $V_{CE,on}$ leading to higher losses in the IGBTs. This increases the junction temperature of the IGBT, which in turn further increases $V_{CE,on}$. This thermal feedback needs to be considered when devising the proposed ACB controller [71].

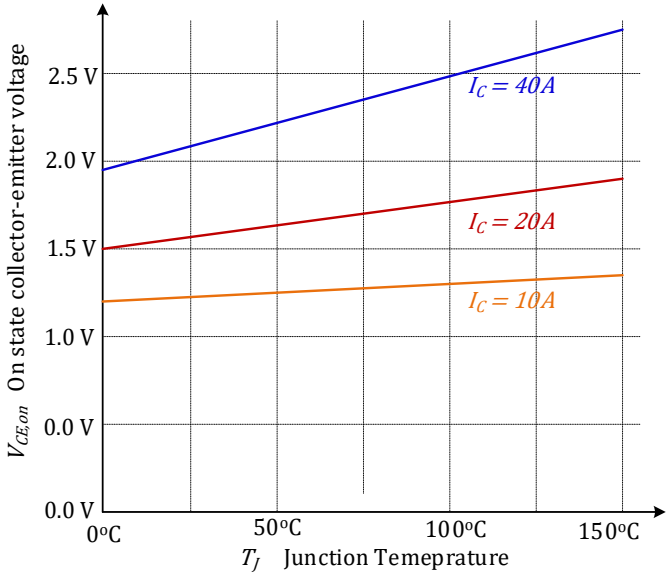


Figure 5.4: IGBT characteristics, $V_{CE,on}$ as a function of the junction temperature.

5.2 System Modeling and Stability Assessment of ACB

The on-state characteristics of the IGBT around an operating point can be approximated by a linear function, as shown in Figure 5.5 [74], [76].

$$v_{CE} = V_{CE,th}[v_{GE}, T_J] + R_{CE,on}[v_{GE}, T_J] i_C \qquad (5.1)$$

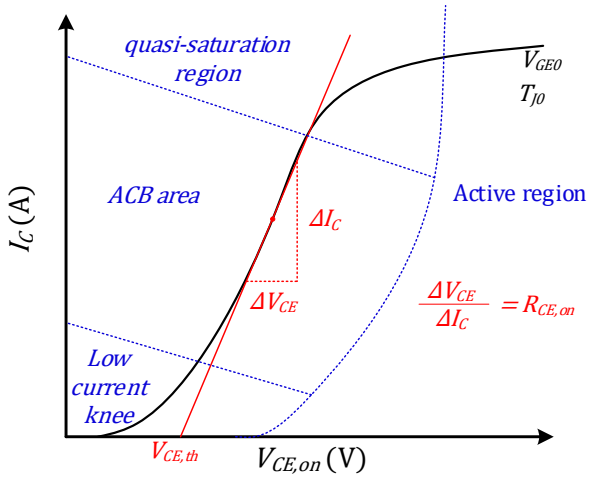


Figure 5.5: Approximation of IGBT on-state characteristics using a linear function.

$V_{CE,th}$ and $R_{CE,on}$ are the collector-emitter threshold voltage and on-state resistance, respectively. $V_{CE,th}$, and $R_{CE,on}$ are functions of v_{GE} and T_J. The low-current knee and quasi-saturation regions of the IGBT cannot be used for this approximation and are valid only for the ACB area (see Figure 5.5), where the IGBTs V-I characteristics are nearly linear [74], [76]. Figure 5. 6 shows how $V_{CE,th}$, and $R_{CE,on}$ vary as functions of v_{GE} and T_J in the saturation region of the IGBT [76].

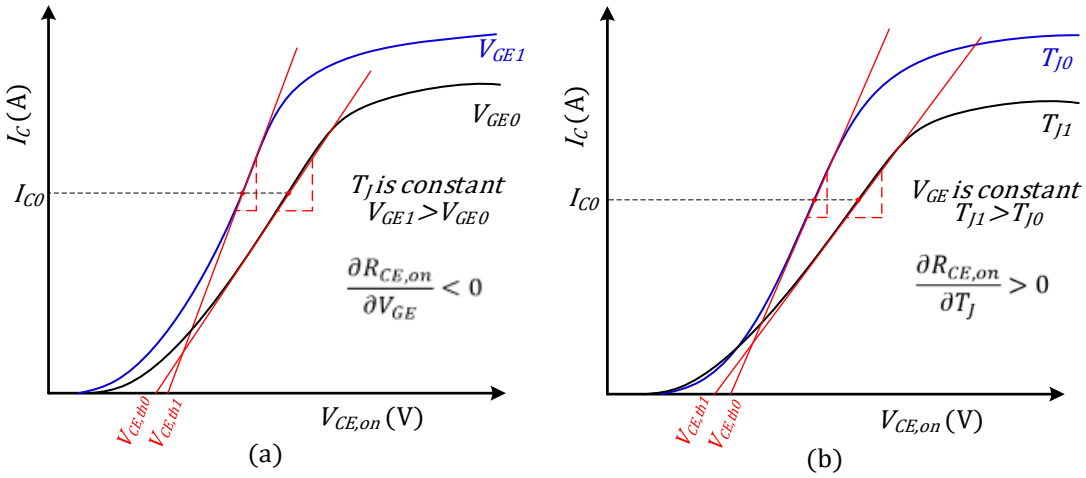


Figure 5. 6: Variation of $V_{CE,th}$, and $R_{CE,on}$ as functions of V_{GE} and T_J

5.2.1 Small Signal Model of ACB Control

The small signal V-I relationship can be derived by linearizing Equation (5.1) around the initial operating point (V_{GE0}, I_{C0}).

$$\Delta I_C(s) = K_{ACB}\Delta V_{GE}(s) \tag{5.2}$$

Where

$$K_{ACB} = -\frac{1}{R_{CE,on0}}\left(\frac{\partial V_{CE,th}}{\partial V_{GE}} + I_{C0}\frac{\partial R_{CE,on}}{\partial V_{GE}}\right)$$

The small signal Equation (5.2) considers only electrical variables, ΔV_{GE} and ΔI_C. T_J is considered constant. K_{ACB} is the current control sensitivity of the IGBT.

Gate dynamics during IGBT on-state can be modeled as a first-order RC network. Deriving the small signal transfer function

$$G_{Gate}(s) = \frac{\Delta V_{GE}(s)}{V_D(s)} = \frac{1}{(1+sR_GC_{GE})} \tag{5.3}$$

Detailed derivations of Equations (5.2) and (5.3) are given in Appendix C. The ACB controller simplifies to the Laplace equation of a PI controller.

$$G_C(s) = K_p + \frac{K_i}{s} \tag{5.4}$$

Since the DAC bandwidth is significantly higher than the ACB control bandwidth, its dynamics can be neglected, allowing it to be modeled as a static gain.

$$G_{DAC}(s) = K_{DAC} \tag{5.5}$$

The LDO regulator's time constant is negligibly small, allowing its model to be simplified to a static gain.

$$G_{LDO} = K_{LDO} \tag{5.6}$$

Delay time T = 10μs is introduced to account for communication and sampling delays of the controller. The current sensor gain of K_H is considered.

$$H(s) = K_H \tag{5.7}$$

The small signal control block diagram for ACB control is shown in Figure 5.7. The open-loop transfer function of the ACB control *L(s)* can be derived using Equations (5.1) to (5.7).

$$\begin{aligned} L(s) = {} & G_{control}(s)G_{DAC}(s)G_{LDO}(s)G_{Gate}(s)G_{ACB}(s)H(s)e^{-sT} \\ = {} & (K_p + \frac{K_i}{s})K_{DAC}K_{LDO}\frac{1}{(1+sR_GC_{GE})}K_{ACB}K_He^{-sT} \end{aligned} \tag{5.8}$$

Steps for the calculation of K_{ACB} using the data provided in the datasheet are shown in *Appendix D*. The device and control Parameters for calculating the ACB transfer function are summarized in Table 5. 1. Based on the parameters listed in Table 5. 1, *L(s)* given in Equation (5.9) is derived. Frequency plots for the *L(s)* are shown in Figure 5.8.

$$L(s) = \frac{0.0136(0.15s+1000)(1-5\times10^{-6}s)}{s(1+2.4\times10^{-6}s)(1+5\times10^{-6}s)} \tag{5.9}$$

Open-loop stability margins obtained from the frequency plot are summarized in Table 5. 2. The loop bandwidth is 2.1 Hz, which is very low and suitable for steady-state ACB control. The phase margin of 90.1° indicates the control system is well-damped and stable. Phase crossover occurs at 71.1 kHz and has a gain margin of 56 dB, indicating a large stability margin that can tolerate a significant increase in ,gain or phase lag before becoming unstable.

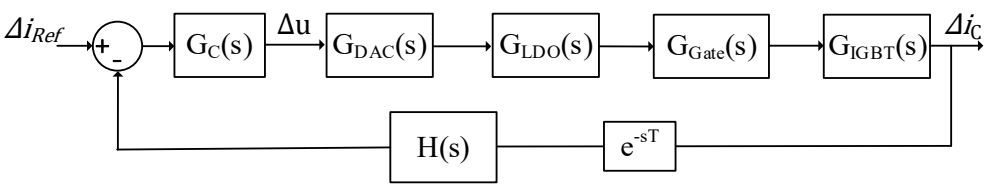


Figure 5.7: Small signal closed-loop control block diagram for the ACB control.

Table 5. 1: ACB model parameters for calculation of *L(s)*.

Parameter	Value	Unit
K_{DAC}	8.06×10^{-4}	V/count
K_{LDO}	5.626	V/V
$R_G C_{GE}$	2.4×10^{-6}	s
K_{ACB}	3	A/V
K_H	1	V/A
T_{Delay}	10×10^{-6}	s
K_P	0.15	-
K_i	1000	-

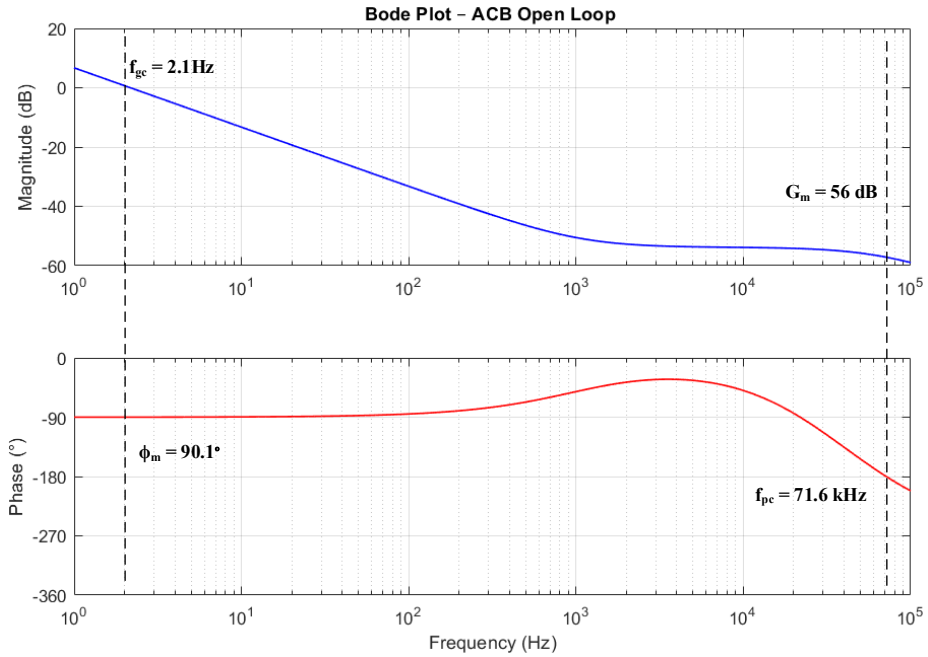


Figure 5.8: Frequency plots for open-loop transfer function *L(s)*.

A high gain margin at high frequencies also shows that the ACB controller is well separated from the AGD bandwidth region, a critical design requirement for ACB. For standalone applications that do not require the AGD function, the loop gain can be increased substantially to broaden the bandwidth and achieve a faster response to current imbalance.

Table 5. 2: Open-loop stability margins

Parameter	Value
Gain Crossover frequency (f_{gc})	2.1 Hz
Phase margin (ϕ_m)	90.1°
Phase Crossover frequency (f_{pc})	71.6 kHz
Gain margin (G_m)	56 dB

The validity of the developed small-signal model for the ACB scheme is further supported by the experimental results presented in Section 5.4, where the measured current-sharing dynamics show good agreement with the analytical predictions.

5.2.2 Modeling the Positive Temperature Feedback and Stability Analysis

The small-signal model Equation (5.2) considers only electrical variables ΔV_{GE} and ΔI_C. To account for variations in junction temperature and its effect on $V_{CE,on}$, we must consider the junction temperature T_J as a state variable [49], [62], [63], [74].

Linearizing the on-state Equation (5.1) around the operating point (V_{GE0}, I_{C0}, T_{J0}), considering v_{GE}, i_C, and T_J as state variables.

$$\Delta I_C(s) = K_{ACB}\Delta V_{GE}(s) + K_{TH}\Delta T_J(s) \tag{5.10}$$

Where,

$$K_{TH} = -\frac{1}{R_{CE,on0}}\left(\frac{\partial V_{CE,th}}{\partial T_J} + I_{C0}\frac{\partial R_{CE,on}}{\partial T_J}\right)$$

K_{TH} is the thermal sensitivity of the IGBT in the steady state. Detailed derivation of (5.10) is given in *Appendix E*.

Since

$$\left(\frac{\partial V_{CE,th}}{\partial T_J} + I_{C0}\frac{\partial R_{CE,on}}{\partial T_J}\right) > 0 \text{ and } R_{CE,on0} > 0,$$

It follows that;

$$K_{TH} < 0.$$

Physically, this implies that an increase in junction temperature ($\Delta T_J > 0$) results in a decrease in collector current ($\Delta I_C < 0$) with gate voltage constant ($\Delta V_{GE} = 0$). This represents the current self-balancing effect inherent to the IGBTs with PTC [62], [76].

The ACB controller is designed with a bandwidth that provides adequate separation from the junction-to-case thermal dynamics. Using the concept of time-scale separation (singular perturbations), we can consider these two subsystems as independent, thereby simplifying the control problem. Because PTC thermal feedback is inherently slow, it does not destabilize the ACB controller. The stability criterion for the IGBT thermal feedback is given in Equation (5.11) (Refer to *Appendix E* for the derivation).

$$|K_{TH}|V_{CE0}R_{TH,j-c} < 1 \qquad (5.11)$$

If $|K_{TH}|V_{CE0}.R_{TH,\,j\text{-}c}$ is too high; the system's thermal feedback is too strong. The IGBT can exhibit thermal runaway despite its PTC property. Unstable thermal runaway heating and continuous I_C change will overwhelm the balancing effect.

However, if $|K_{TH}|V_{CE0}R_{TH,j\text{-}c}$ is too small (close to 0), the system is stable and has an overdamped PTC response. Hence, slow thermal current balancing. The following design practices ensure stable thermal feedback.

- Selection of devices with appropriate PTC strength.
- Operate in moderate V_{CE}

5.3 Daisy Chain Hardware Architecture for Active Current Balancing

The proposed daisy chained architecture for implementing the ACB with multiple parallel-connected IGBTs is illustrated in Figure 5.9. Each gate driver unit is equipped with a local DSP, which is interconnected via a communication link. This decentralized control approach eliminates the need for centralized controllers, thereby simplifying the overall system architecture and enhancing modularity.

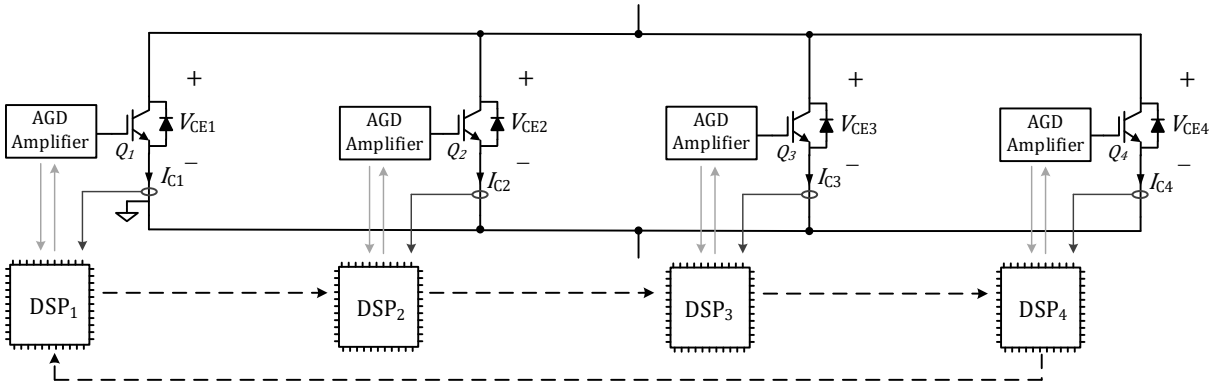


Figure 5.9: Daisy chain hardware architecture for IGBT parallel connection.

Each gate driver independently monitors and regulates the current through the IGBT while exchanging current information with other units in parallel. This architecture facilitates seamless integration of additional parallel IGBT modules, enabling straightforward scalability of the HCB.

The schematic and the experimental setup used for testing the proposed ACB scheme are shown in Figure 5.10 (a) and (b). As illustrated in the figure, four IGBTs are connected in parallel, and the local DSP of each IGBT is linked through a fast serial communication link in a daisy chain. The test setup uses a 60V/40A DC power supply with a resistive load to evaluate the proposed ACB. This paper employs the Fast Serial Interface (FSI) communication protocol

for Texas Instruments DSPs [80]. Serial communication protocols such as EtherCAT, CAN-FD, and LVDS are inherently well-suited for daisy chaining due to their low latency and network expandability. I_C and V_{GE} waveforms are recorded under each test case. *K*-type thermocouples are used to measure the case temperature.

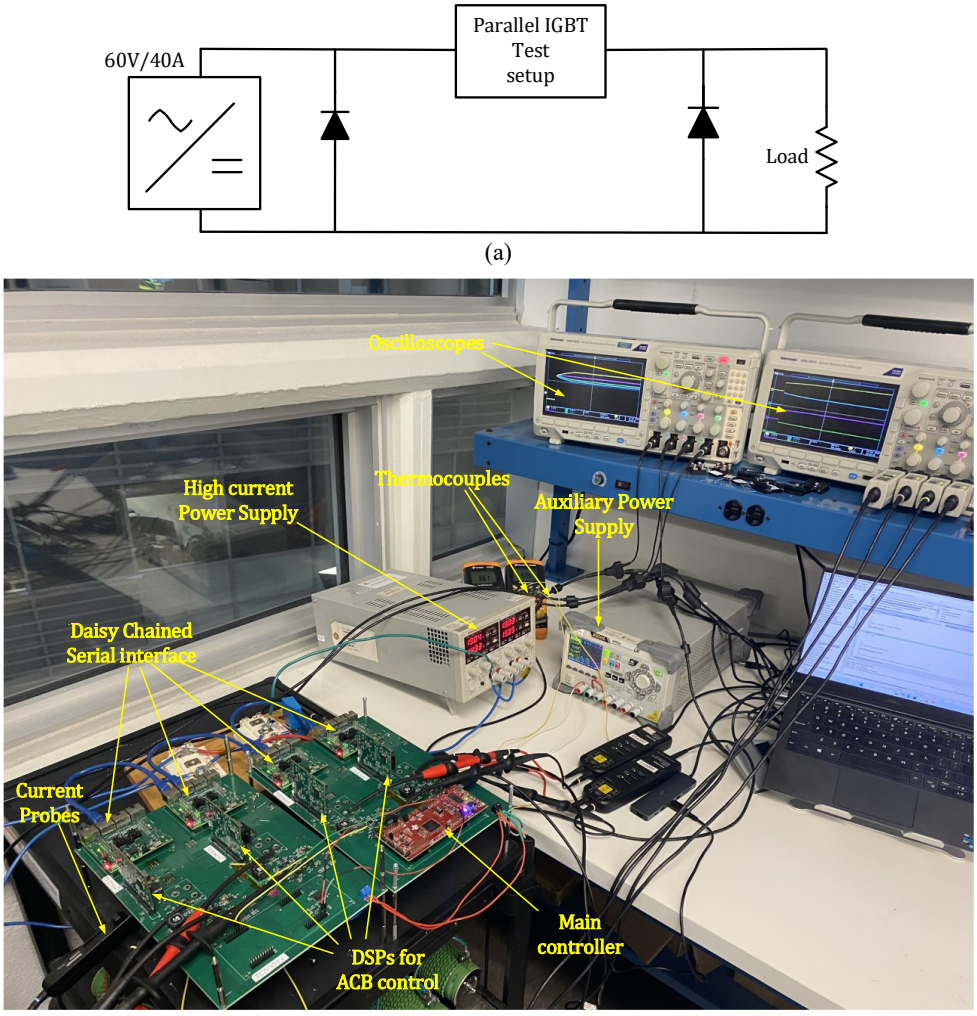


Figure 5.10: (a) Schematic and (b) Experimental setup for evaluating the proposed Active Current Balancing (ACB) scheme.

5.4 Active Current Balancing: Experimental Study

The proposed ACB scheme is evaluated under different test scenarios to assess the capability to achieve current balance among parallel IGBTs. Three distinct test cases with

different IGBT parallel path resistance, IGBT models, and gate voltages (V_{GE}) are considered to evaluate the ACB scheme. Case 4 assesses the thermal response of the IGBTs to test the PTC thermal feedback and stability of the ACB scheme with thermal feedback.

Figure 5.11 shows the schematic of the test setup used for four parallel IGBTs under different conditions. Test conditions for each case are summarized in Table 5. 3. The proposed ACB scheme is validated for parallel-connected IGBTs in a unidirectional HCB configuration.

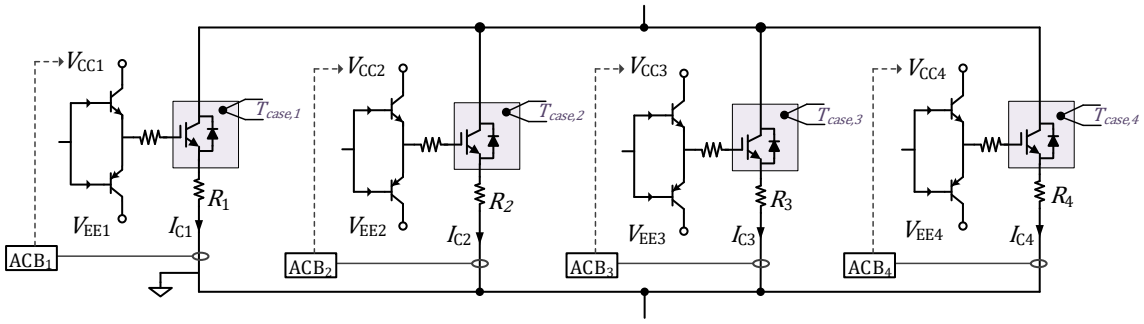


Figure 5.11: Schematic of four parallel IGBTs for ACB testing.

Table 5. 3: Summary table for different conditions used for testing the ACB

Case	R	V_{CC}	IGBT Models	T_{Case}
Case 1	R_1= 0.02 Ω R_2 = 0.01 Ω R_3 = 0 Ω R_4 = 0.03 Ω	$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4}$ = 15 V	*STGW10M65DF2*	-
Case 2	-	$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4}$ = 15 V	Q_1= *STGW30H65FB* Q_2= *STGW30H65FB* Q_3= *IGW30N60T* Q_4= *IKW20N60T*	-
Case 3	-	V_{CC1} = 10 V V_{CC2} = 17 V V_{CC3} = 15 V V_{CC4} = 15 V	*STGW19NC60HD*	-
Case 4	R_1= 0.05 Ω R_2 = 0 Ω R_3 =0.02 Ω R_4 = 0.01 Ω	$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4}$ = 15 V	*STGW10M65DF2* (with no heatsinks)	Measured

5.4.1 Case 1: ACB Action with Four Parallel IGBTs with Different Resistance Paths

The objective of this experiment is to verify the desired performance of the ACB for IGTBs of the same model, but with variations in output characteristics that result in different $V_{CE,on}$ for the same I_C and V_{GE}. Four parallel IGBTs with different parallel resistance paths are used to create a current imbalance (see Figure 5.11). The resistance values used are listed in Table 5. 3.

From the experimental results in Figure 5.12, the proposed gate drive can achieve current balancing in approximately 4-5 seconds. Here, the PI control parameters are set to ensure the control action is very slow compared to AGD. This approach avoids any control interaction during turning on and off, where the AGD current and voltage slope control is done. However, as discussed in Section 5.2.1, the ACB loop gain may be increased to achieve faster current balancing action after evaluation of the AGD bandwidth to ensure adequate separation between the two control loops.

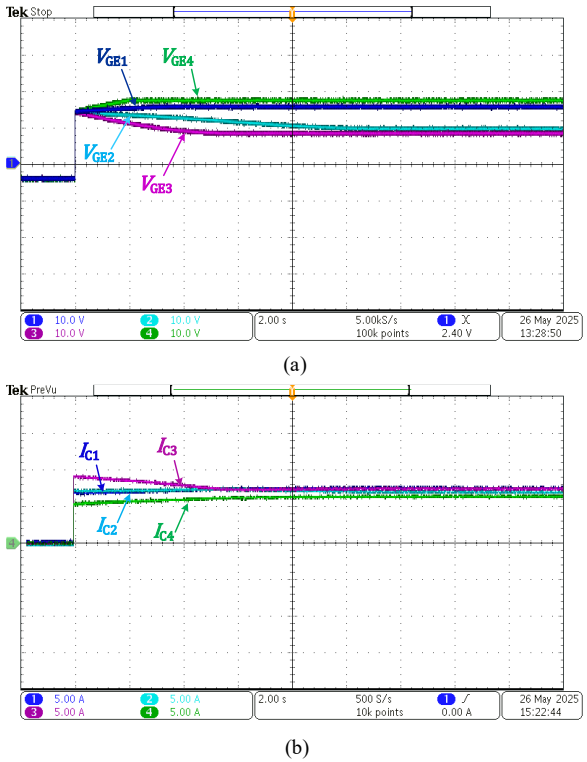
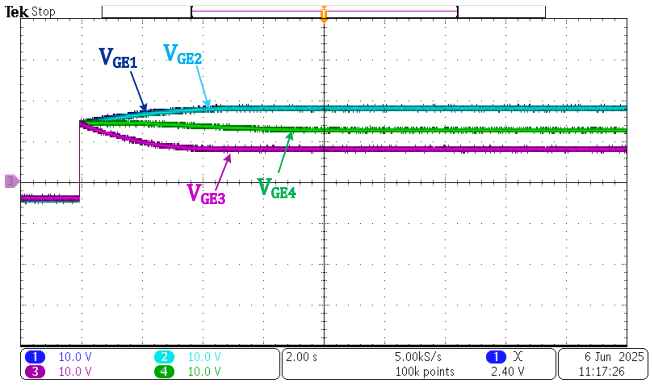


Figure 5.12: ACB control action for parallel IGBTs with different resistance paths (a) Gate-emitter voltage (V_{GE}), (b) Collector current (I_C).

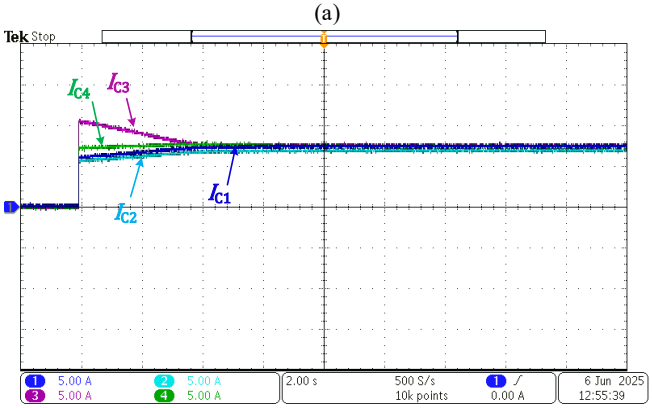
5.4.2 Case 2: ACB Action with Four Parallel IGBTs with Different Output Characteristics.

To evaluate the robustness and adaptability of the proposed ACB controller, experimental validation was carried out using four IGBTs with dissimilar output characteristics. The devices were intentionally selected to exhibit a mismatch in conduction and switching behavior, thereby replicating real world variability often encountered in parallel-connected modules. Table 5. 3 lists the IGBT models used for this test.

From the experimental results in Figure 5.13, it can be seen that the proposed ACB controller achieves current balance within a few seconds, demonstrating its ability to balance current across parallel IGBTs of different makes and models.



(a)



(b)

Figure 5.13: ACB control action for parallel IGBTs with different output characteristics (a) Gate – emitter voltage (V_{GE}), (b) Collector current (I_C).

5.4.3 *Case 3: ACB Action with Four Parallel IGBTs with Different Gate Voltages*

To evaluate the capability of the proposed ACB scheme to compensate for current unbalances caused by V_{GE} differences, four parallel IGBTs are tested with different initial V_{CC} values.

Device and circuit level asymmetries can result in differences in V_{GE} across parallel-connected IGBTs [62], [63]. The objective of this experiment is to assess the sensitivity of the ACB to mismatches caused by differences in V_{GE}. Since no other parameter can independently change the V_{GE} in the experimental setup, the initial V_{CC} at IGBT turn-on is set differently to emulate a difference in V_{GE} for this experiment. This approach provides an equivalent means of introducing different V_{GE} conditions.

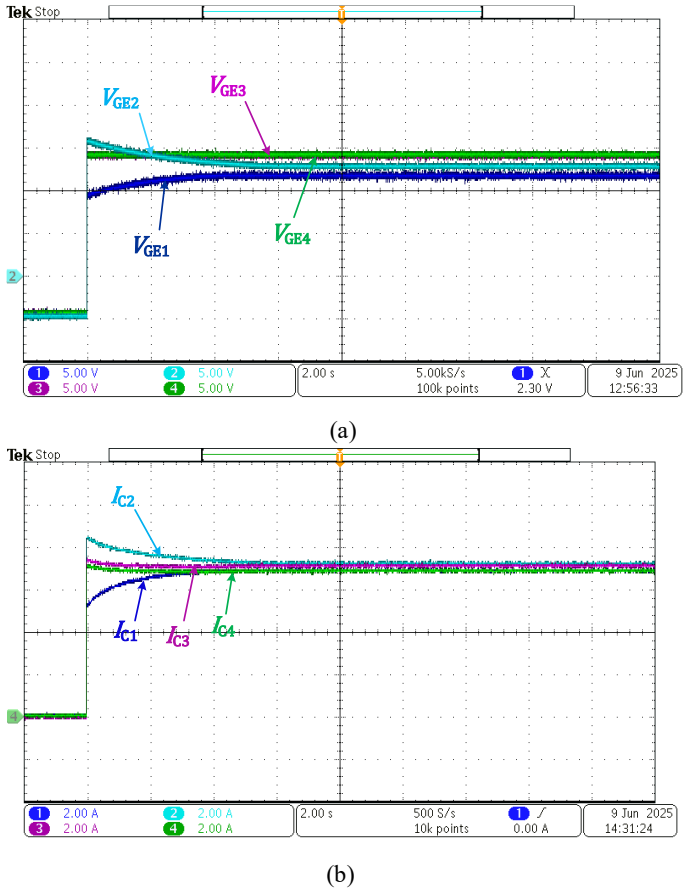


Figure 5.14: ACB control action for parallel IGBTs with different turn-on gate voltages (V_{CC}) (a) Gate-emitter voltage (V_{GE}), (b) Collector current (I_C).

The test case conditions are presented in Table 5. 3. Different initial V_{CC} values are set to turn on the IGBTs, resulting in varying collector currents (I_C), which are governed by the output characteristics. The experimental results in Figure 5.14 demonstrate that the proposed ACB eliminates current imbalances by correcting the V_{CC} differences.

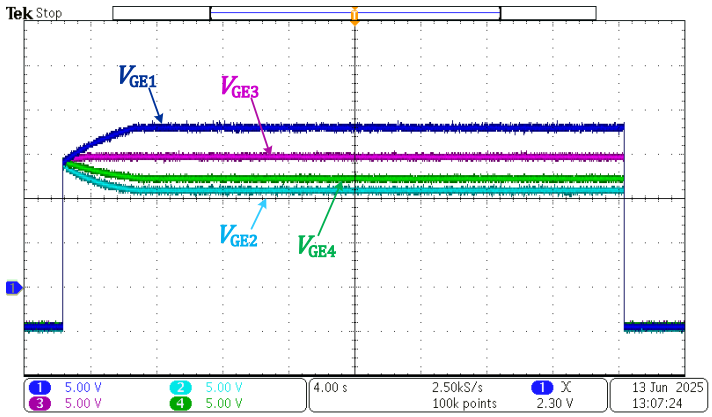
5.4.4 Case 4: Effect of Positive Temperature Coefficient with ACB Action

The objective of this experiment is to evaluate the effects of positive temperature feedback on the ACB control action. For this experiment, a low current-rated IGBT with a high $V_{CE,on}$ is selected to allow the IGBTs to heat up quickly. Heat sinks are not utilized for the same purpose. The experiment was carried out with different parallel resistance paths to force unbalanced current sharing, which in turn activates the ACB (See Table 5. 3).

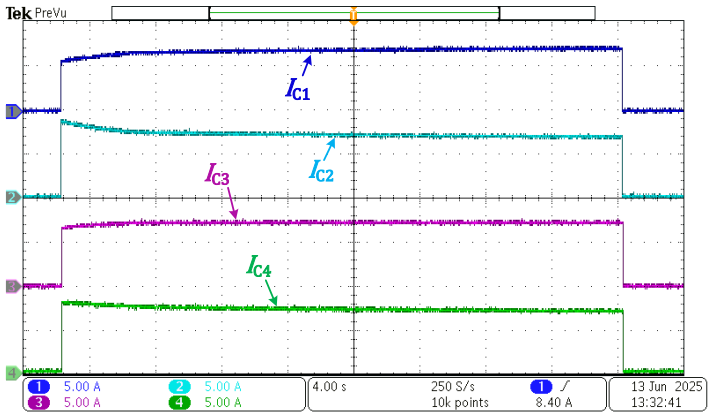
Steady-state current sharing is achieved by dynamically adjusting the V_{GE} of the individual IGBTs. Specifically, V_{GE2} and V_{GE4} were reduced to 10.5V and 11.5V, respectively, while V_{GE1} was increased to 18V. As a result, $IGBT_2$ and $IGBT_4$ experienced higher conduction losses compared to $IGBT_1$ and $IGBT_3$. Consequently, $IGBT_2$ and $IGBT_4$ heat up more rapidly, and due to the PTC, the current gradually decreases. This thermal feedback mechanism is inherently slow, as shown in the experimental results in Figure 5.15. This thermally induced change in current may slowly lead to a current imbalance between IGBTs, triggering the ACB to counteract it.

The experimental studies confirm that the proposed ACB scheme reliably achieves steady-state current balancing and maintains stable operation across varying electrical and thermal conditions. These findings establish a strong foundation for integrating the ACB with the AGD to achieve coordinated control across the entire switching cycle. The next Section evaluates the

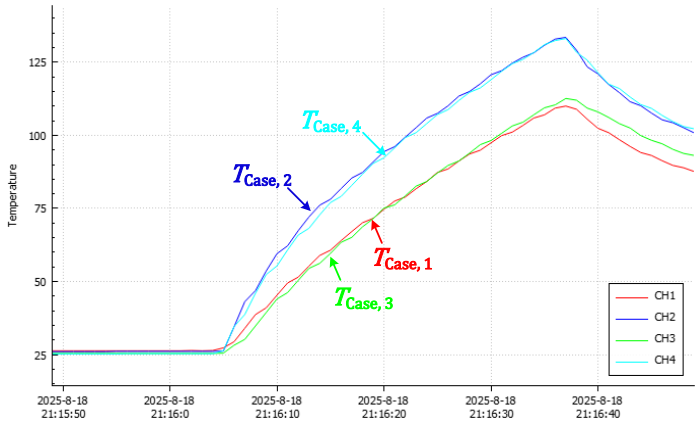
combined ACB and AGD control scheme to demonstrate coordinated dynamic and steady-state current balancing in both series and parallel connected IGBTs.



(a)



(b)



(c)

Figure 5.15: Positive thermal feedback with ACB control action for parallel IGBTs with different parallel resistance paths (a) gate-emitter voltage (V_{GE}), (b) collector current (I_C), (c) IGBT case temperature (T_{Case}).

5.5 Combined Active Gate Drive and Active Current Balancing Scheme

The Active Gate Drive (AGD) scheme presented in Chapter 3 ensures dynamic voltage and current sharing between series and parallel-connected IGBTs. However, it cannot address the steady state current imbalance among parallel IGBTs. Hence, combining the AGD scheme with ACB is crucial for safe and reliable operation.

In high power HCB applications, both dynamic switching performance and reliable steady-state operation are critical. Hence, integrating the ACB functionality into the AGD is essential. While this combined approach simultaneously controls dynamic voltage/current slopes and ensures steady state current sharing, the control loops must be independent to avoid controller interactions. Tight coupling between AGD and ACB can lead to complex interactions, such as:

- Unnecessary modulation of gate voltages by current balancing logic during IGBT switching.
- Fast current balancing actions can lead to current transients, leading to high di_C/dt triggering the AGD action to slow down the di_C/dt, thereby causing controller interactions.

Figure 5. 16 shows the AGD and ACB control areas, which clearly indicate that the IGBT operates in two distinct regions of the IGBT characteristics curves.

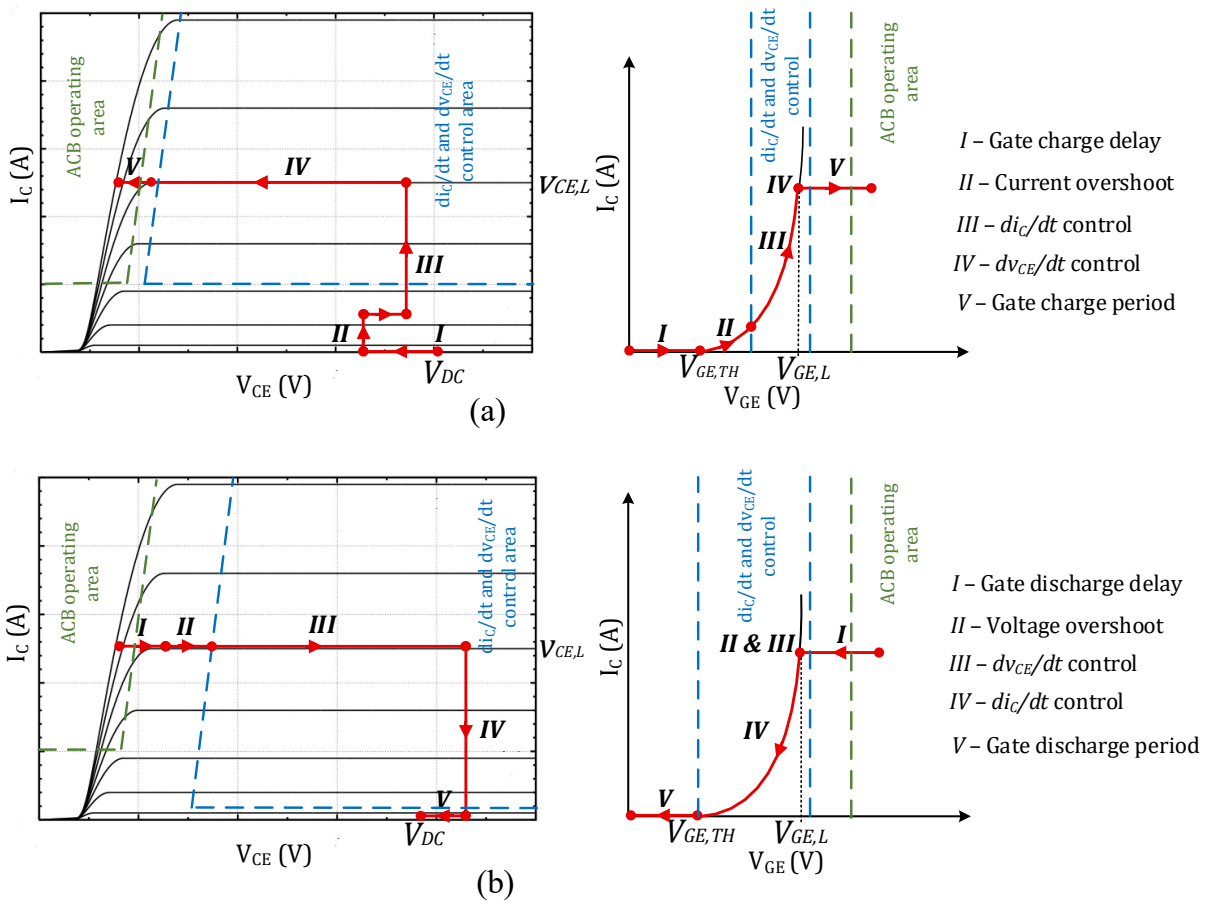


Figure 5. 16: Visual illustration of the IGBT operating areas during IGBT (a) turn-on and (b) turn-off (AGD operation) and steady state (ACB operation).

In the proposed independent control strategy, the control of dynamic current and voltage slope, and steady-state current balancing operate on different time scales. Figure 5. 17 shows the schematic block diagram integrating AGD and ACB.

The AGD focuses on high-bandwidth control of switching transients by directly controlling dv_{CE}/dt and di_C/dt on a ns-µs time scale. In contrast, the proposed ACB scheme has a lower control bandwidth and operates on a ms-s time scale. Thus, it prevents interference between the dynamic switching control and the steady-state current balancing control.

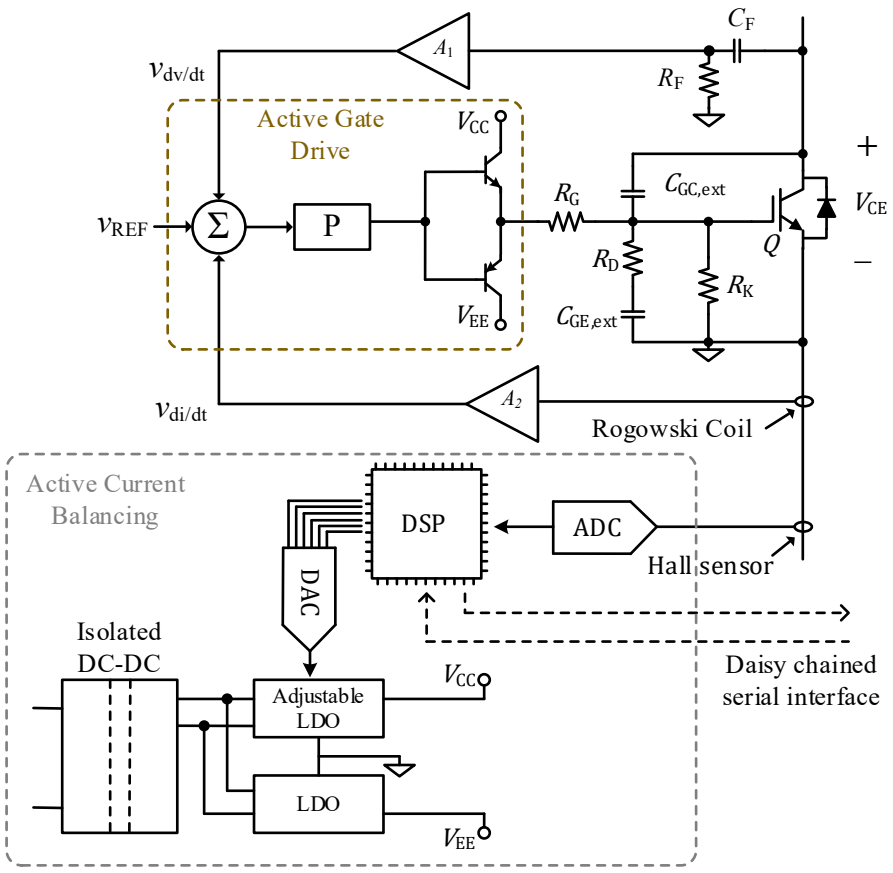
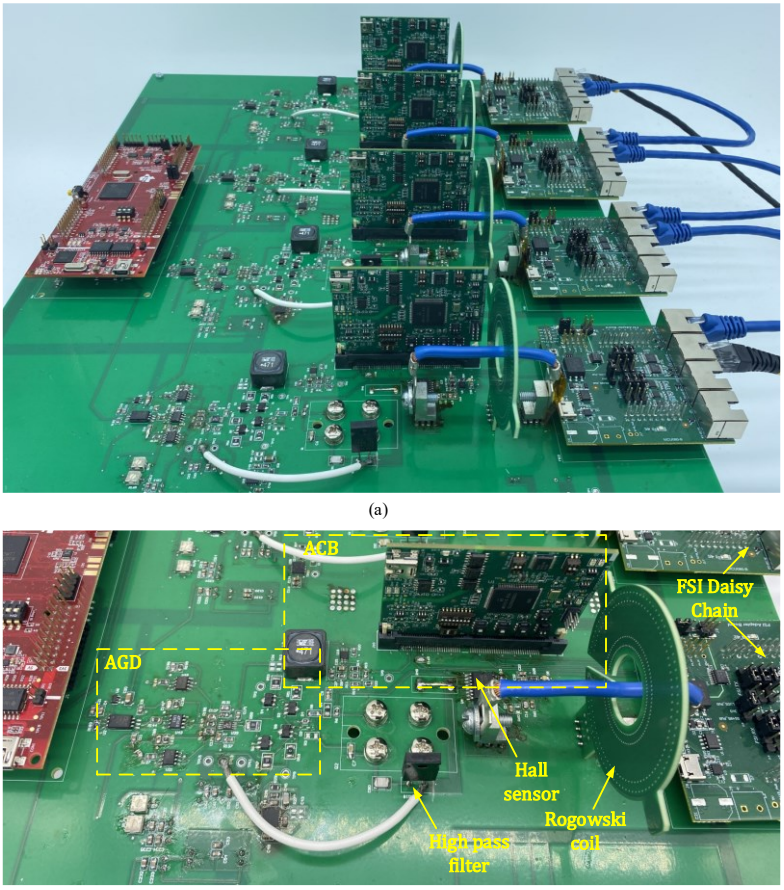


Figure 5. 17: Schematic representation of the ACB scheme combined with AGD technology

An experimental study is conducted to investigate the combined control capability of the AGD and ACB and to determine if the two control actions interfere with each other. Figure 5. 18 shows the prototype board with combined AGD and ACB control capability for four parallel-connected IGBTs. The experimental studies are conducted under two test scenarios to evaluate the independent control between ACB and AGD.

- Both ACB and AGD enabled - Shows the dynamic voltage and current slope control capability during IGBT switching and the steady-state current balancing performance.
- ACB only (with AGD disabled) - Demonstrates the dynamic current imbalance between IGBTs during IGBT switching with AGD disabled.

Figure 5. 19 shows the schematic of the test setup used to assess the combined AGD and ACB scheme under different conditions. Test conditions for each case are summarized in Table 5. 4. The Testing was done using a 150V/100A high-power test setup.



(a)

(b)

Figure 5. 18: (a) Prototype board developed to validate the integrated operation of the Active Gate Drive (AGD) and Active Current Balancing (ACB) schemes across four parallel-connected IGBTs. (b) Zoomed-in view highlighting the component-level layout and interconnection of the AGD and ACB control circuitry.

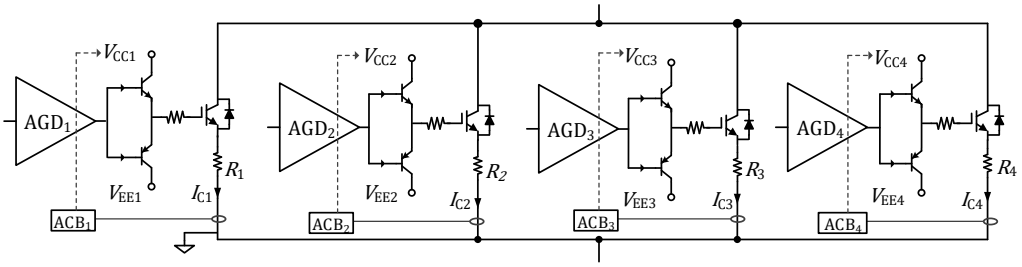


Figure 5. 19: Testing combined ACB and AGD action: four parallel IGBTs with different resistance paths.

Table 5. 4: Summary table for different conditions used for testing the combined ACB and AGD scheme

Case	R	V_{CC}	IGBT Model	AGD
Case 1	R_1= 0.015 Ω R_2 = 0 Ω R_3 =0.005 Ω R_4 = 0.02 Ω	$V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4}$ = 15 V	*VS-GT80DA120U*	Enabled
Case 2	R_1= 0.005 Ω R_2 = 0 Ω R_3 = 0 Ω R_4= 0.005 Ω	V_{CC1} = 15 V V_{CC2} = 15 V V_{CC3} = 12 V V_{CC4} = 12 V	*VS-GT80DA120U*	Enabled

5.5.1 Case 1: Combined ACB and AGD Action with Four Parallel IGBTs with Different Resistance Paths.

This experiment aims to assess the performance of AGD in conjunction with ACB, using parallel IGBTs of different resistance paths. Table 5. 4 summarizes conditions for the experiment. It is anticipated that the ACB will effectively mitigate steady-state current imbalances, while the AGD will be responsible for regulating di_C/dt and dv_{CE}/dt during dynamic switching events.

Figure 5. 20 shows the experimental results demonstrating the combined operation of ACB and AGD, including steady-state current sharing and the dynamic current balancing during IGBT turn-off. ACB action eliminates the steady-state current imbalance within a few seconds by reducing the gate drive voltage (V_D) of the $IGBT_1$, $IGBT_2$, and $IGBT_3$ to 11.2V, 8.8V, and 10.5V, respectively. However, when IGBTs turn off, the parallel-connected IGBTs with different V_D values may turn off at different rates. This causes severe switching current imbalances. The AGD scheme compensates for this by controlling the di_C/dt and dv_{CE}/dt during the IGBT turn-off. For comparison, the dynamic current and voltage profiles of the four parallel IGBTs with AGD action disabled are shown in Figure 5. 21.

With AGD disabled, the current through the $IGBT_2$ and $IGBT_3$ commutates quickly to the other IGBTs. This results in significant imbalances in the switching current between the 4 IGBTs. Furthermore, the IGBTs turn off at rates determined by device characteristics and the applied gate drive voltages before turn-off. In high current applications, this could result in significant dynamic current imbalances that surpass the critical current limits of the discrete IGBTs. In addition, IGBT turn-off voltage overshoot is significantly reduced when AGD is enabled to control the di_C/dt and dv_{CE}/dt. With AGD enabled, the switching current slope follows the di_C/dt reference. This curtails the transient interrupt voltage to a lesser value as shown in Figure 5. 21 (a) and (b).

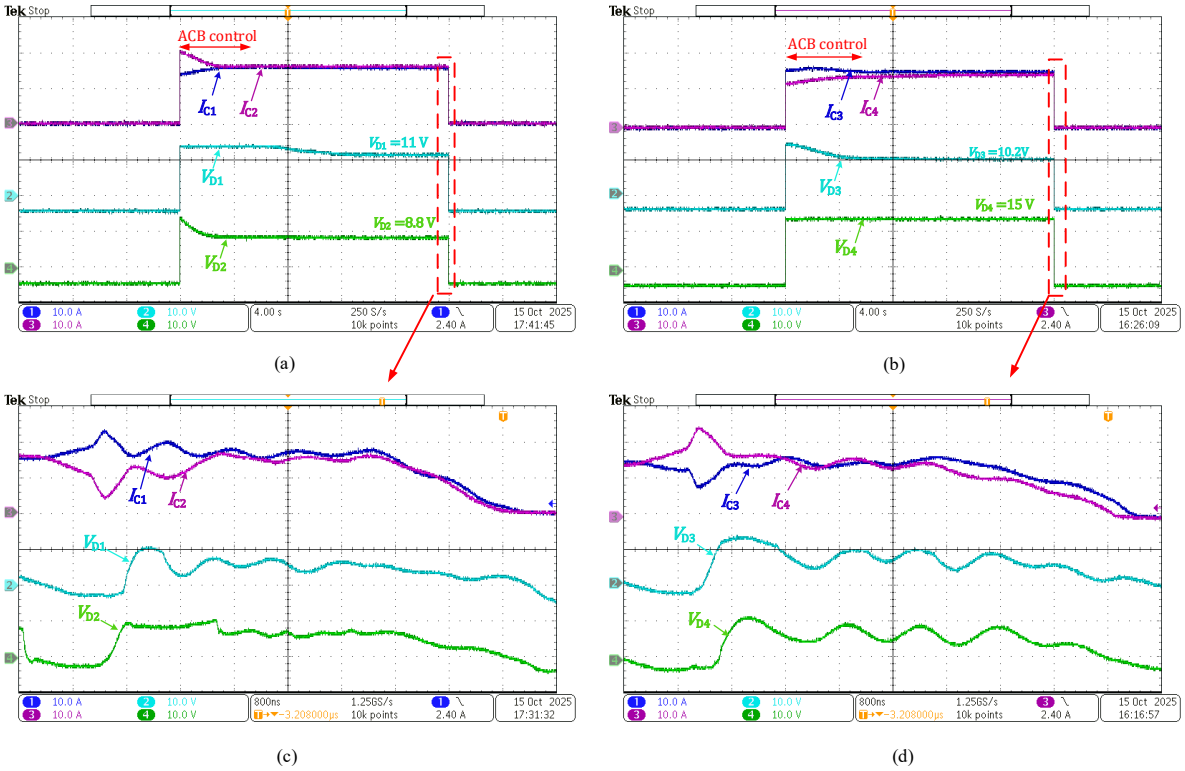


Figure 5. 20: Collector current (I_C) and Gate drive voltage (V_D) showcasing ACB control action for parallel IGBTs with different resistance paths (a) $IGBT_1$ and $IGBT_2$, (b) $IGBT_3$ and $IGBT_4$, AGD control action during IGBT turn-off (c) $IGBT_1$ and $IGBT_2$, (d) $IGBT_3$ and $IGBT_4$.

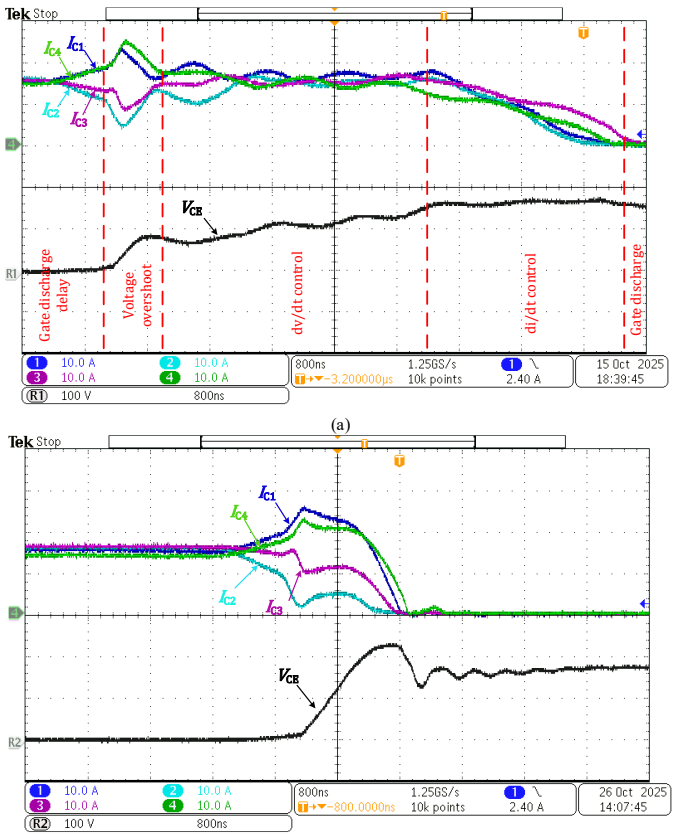


Figure 5. 21: Collector current (I_C) and collector-emitter (V_{CE}) voltage during IGBT turn off with different parallel path resistance (a) With combined AGD-ACB scheme, (b) with AGD disabled.

Transition of operating point of the $IGBT_1$ and $IGBT_3$ during distinct operating stages of AGD-IGBT turn-off is shown in Figure 5. 22. Due to the ACB control action, $IGBT_1$ and $IGBT_3$ have different gate drive voltages. Hence, during the initial gate discharge stage (*stage I*), they follow different trends as shown in Figure 5. 22. However, during the voltage overshoot stage (*stage II*), they converge to the same operating point of the IGBT transfer characteristics. From there onwards, they follow the same trend during the dv_{CE}/dt and di_C/dt control stages (*stage III* and *IV*).

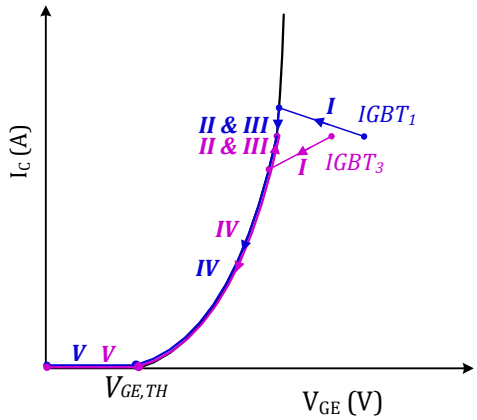


Figure 5. 22: Transition of $IGBT_1$ and $IGBT_2$ operating point during turn-off in the transfer characteristics.

5.5.2 *Case 2: Combined ACB and AGD Action with Four Parallel IGBTs with Different V_{GE} and Resistance Paths.*

To assess the performance of the combined AGD and ACB scheme under varying conditions, four parallel IGBT setups with different initial V_{CC} (to emulate different V_{GE}) and parallel path resistances are used. Test parameters are summarized in Table 5. 4.

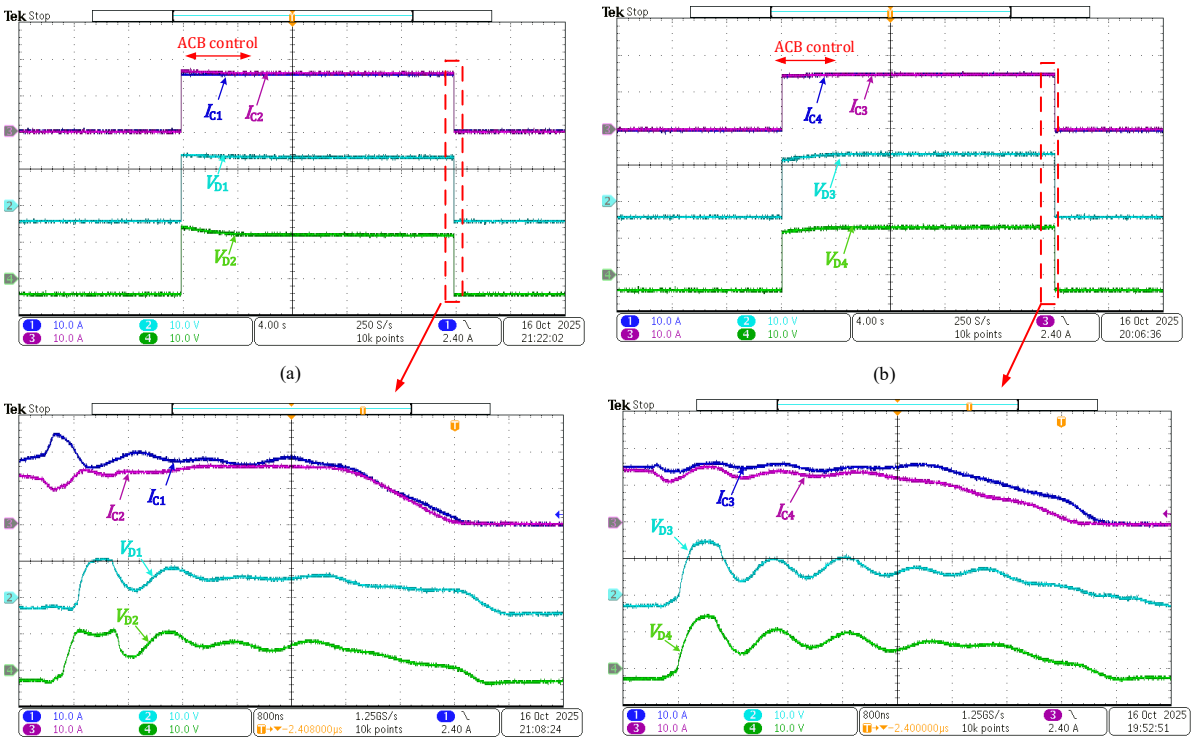


Figure 5. 23: Collector current (I_C) and Gate drive voltage (V_D) showcasing ACB control action for parallel IGBTs with different V_{CC} and resistance paths (a) $IGBT_1$ and $IGBT_2$ (b) $IGBT_3$ and $IGBT_4$, AGD control action during IGBT turn off (c) $IGBT_1$ and $IGBT_2$, (d) $IGBT_3$ and $IGBT_4$.

The experimental results are shown in Figure 5. 23. The results show that when the IGBTs are turned on, ACB adjusts the V_{CC} to compensate for current imbalances caused by different initial V_{CC} and parallel path resistance. Due to differences in V_{CC}, during turn-off $IGBT_2$, $IGBT_3$, and $IGBT_4$ turn off faster than $IGBT_1$. However, during the voltage overshoot stage, the dynamic current imbalance is rectified, and the IGBT operating points converge to the same point of the IGBT transfer characteristics. The experimental results demonstrate that with AGD control, the four IGBTs share the dynamic switching current equally.

The comparison of I_C and V_{CE} profiles with and without AGD action, shown in Figure 5. 24 demonstrates the effectiveness of the AGD scheme for controlled turn-off operation of the parallel-connected IGBTs. With di_C/dt control, transient voltage overshoot is reduced across device and circuit inductances. This controlled switching action minimizes transient energy coupling and suppresses overvoltage stress, enhancing the safe operating margin of the IGBTs.

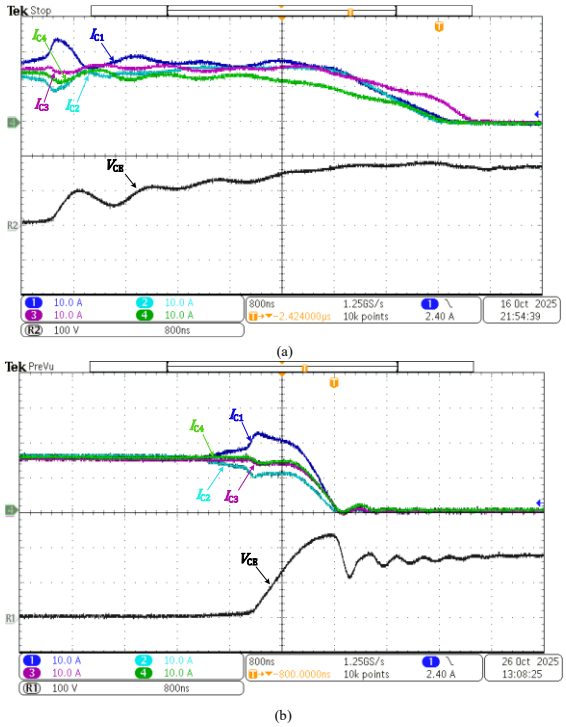


Figure 5. 24: Collector current (I_C) and collector-emitter (V_{CE}) voltage during IGBT turn-off with different V_{CC} and parallel path resistance (a) With combined AGD-ACB scheme, (b) with AGD disabled.

5.6 Summary of Contributions

- **Proposed ACB Concept**: Introduction of the ACB Scheme capable of mitigating steady state current imbalance in parallel-connected IGBTs.
- **Modeling and Stability Assessment** of the proposed ACB scheme, to identify key parameters governing its dynamic behavior and the loop stability.
- **Daisy-Chained Hardware Architecture**: Development of a scalable, daisy-chained hardware architecture for the implementation of the ACB scheme while enabling modularity for multiple IGBTs connected in parallel.
- **Experimental Validation**: Evaluation of the proposed ACB scheme using experimental studies under multiple operating scenarios, demonstrating the effectiveness of the ACB scheme.
- **Combined ACB and AGD Scheme**: Introduction of the combined ACB and AGD scheme as a solution to both steady state and dynamic switching operation of the IGBTs.
- **Time Scale Decoupling Strategy and Experimental Validation:** Introduction of a time scale separation strategy for AGD and ACB for unified operation without control interference. Evaluation of the combined operation and its ability to function without any control interference, using different experimental studies.
- **Applicability to MVDC DCCBs**: Formulation of a practical current sharing solution for next-generation MVDC Circuit breakers.

Chapter 6: Conclusions, Contributions and Future Work

This Chapter outlines the conclusions and main contributions of this study, including further research areas for the proposed concept.

6.1 Conclusions

- The main challenge for MVDC networks is the lack of a reliable DC Circuit Breaker (DCCB) solution for network protection. DCCBs require an effective method to facilitate current and voltage sharing among discrete IGBT devices.
- Active Gate Drive (AGD) technologies proposed in this research demonstrated their ability to achieve dynamic current and voltage balance among series-parallel IGBTs by controlling di_C/dt and dv_{CE}/dt during IGBT switching.
- The Active Switch Module (ASM) concept demonstrates strong potential as a flexible and scalable foundation for future DCCB solutions, supporting a wide range of MVDC network applications.
- The proposed ASM-HCB Architecture is evaluated through extensive experimental studies. It demonstrates its current-interrupt capability with minimal IGBT derating by efficiently sharing current and voltage during switching. Furthermore, the AGD eliminates the need for passive components, such as snubber devices and large MOVs, thereby significantly reducing the size and cost of DCCBs.
- The steady-state and transient thermal behavior of the DCCB is a crucial aspect for ensuring reliable operation. DCCB Thermal design guidelines are presented and validated through an experimental study.

- This research identifies the need for a steady-state current balancing scheme. An Active Current Balancing (ACB) scheme is presented, featuring a daisy chain hardware architecture for its practical implementation. Experimental studies under various test cases confirm the validity of the proposed ACB scheme and demonstrate the effectiveness of the proposed hardware architecture.
- A time scale separated control strategy integrating AGD and ACB schemes into a unified dynamic and steady-state current-voltage balancing scheme for series-parallel IGBTs is presented and validated through experimental studies.

6.2 Main Contributions

- Development and demonstration of an Active Gate Drive (AGD) strategy capable of regulating both di_C/dt and dv_{CE}/dt during IGBT switching, enabling dynamic current and voltage balancing among series–parallel IGBTs.
- Introduction of the Active Switch Module (ASM) concept as a flexible and scalable building block for next generation DCCB solutions suitable for a wide range of MVDC applications.
- Development of the ASM-HCB architecture for scalable and reliable operation in MVDC networks. The proposed architecture eliminates the need for costly passive snubbers and MOV components while significantly reducing the IGBT derating requirements.
- Development of an Active Current Balancing (ACB) scheme to achieve steady state current balancing between parallel-connected IGBTs for DCCB applications.

- Development of an integrated ACB-AGD control scheme for DCCBs that enables coordinated dynamic and steady-state current and voltage balancing among parallel-connected IGBTs.

6.3 Future Research

- Developing higher voltage and higher current prototypes for practical MVDC networks and performing long-term field testing to evaluate reliability, aging effects, and maintenance requirements under real operating conditions.
- Investigation of direct experimental validation of the developed small signal model for di_C/dt and dv_{CE}/dt control through frequency response measurements. Such a validation requires operating the IGBT in the active region within the SOA to measure the frequency response, or alternative frequency response identification techniques.
- Integrating real-time IGBT case temperature monitoring into the ACB scheme provides direct thermal management feedback, enabling device temperature to be actively regulated rather than relying solely on thermal feedback.
- Incorporating on-state voltage measurement into the ACB scheme can further refine the scheme by ensuring IGBTs operate in the saturation region, thereby enhancing overall device reliability.
- The Application of the proposed AGD and ACB schemes to bidirectional DCCBs should be investigated. With back-to-back IGBTs employed to achieve bidirectional capability, the additional diode conduction path introduces additional dynamic and steady state effects that may influence dynamic and steady state voltage and current balancing.

- Study the application of the proposed AGD and ACB scheme for Solid-State Circuit Breakers (SSCBs). Steady-state current and thermal balancing demands are significantly higher in SSCB applications, underscoring the need for detailed studies of the stability of the associated thermal feedback mechanisms.

Appendix

A. ASM Turn On-Off Behavioral Analysis and Switching Equations

I. ASM Turn On Behavior.

Stage I: Gate charge delay period – Initiates the charging of the IGBT input capacitance, C_{ies}. i.e., C_{GE} is charged while C_{GC} is discharged. The IGBT is blocked while v_{GE} stays below the threshold voltage, $V_{GE,th}$. When the v_{GE} reaches $V_{GE,th}$ the IGBT starts to conduct current according to its transfer characteristics. Until this point, AGD behaves as a resistive GD; hence, the equations that govern IGBT behavior with a resistive GD are valid.

For the charging of an RC circuit using a resistive gate drive,

$$v_{GE}(t) = V_{CC}\left[1 - e^{-t/\tau_G}\right] \quad \text{(A1)}$$

$$i_G(t) = \frac{V_{CC} - v_{GE}(t)}{R_G + R_D} \quad \text{(A2)}$$

Here, τ_G is the time constant of the equivalent circuit. $i_G(t)$ is the instantaneous gate current. $C_{GE,int}$, R_D, and $C_{GE,ext}$ make up a second-order low-pass filter with two different time constants τ_1 and τ_2. When we take the output across $C_{GE,int}$ we have a system with two poles and a zero. By using the open-circuit time constant method.

$$\tau_1 = R_G C_{GE,int} \quad \text{(A3)}$$

$$\tau_2 = [R_G + R_D]C_{GE,ext} \quad \text{(A4)}$$

Considering $C_{GE,ext}$ is several times larger than $C_{GE,int}$, for simplicity of analysis, we can consider the circuit time constant.

$$\tau_g = \tau_2 = [R_G + R_D]C_{GE,ext} \quad \text{(A5)}$$

Stage II: Current overshoot period – Due to the absence of di/dt feedback, the AGD behaves as a resistive GD. As a result, the IGBT experiences a steep rise in collector current. However, AGD receives di/dt feedback and gains control of the current slope.

The collector current is defined using the static transfer characteristics of the IGBT. g_{ms} is the IGBT transconductance.

$$ic(t) = g_{ms}\left[v_{GE}(t) - V_{GE,th}\right] \tag{A6}$$

$$\frac{di_C(t)}{dt} = g_{ms}\left[\frac{dv_{GE}(t)}{dt}\right] = g_{ms}\left[\frac{i_G(t)}{C_{ies}}\right]$$

$$\approx g_{ms}\left[\frac{i_G(t)}{C_{GE,int}+C_{GE,ext}}\right] \tag{A7}$$

Stage III: Active current slope control period – AGD controls the collector current rise as set by the $(di/dt)_{REF}$. Since the IGBT is still in the active region, Equation (A7) governing the $di_C(t)/dt$ in the previous stage remains valid.

$(di/dt)_{REF}$ determines the $i_G(t)$ during this stage. The drive voltage of the AGD, $v_{AGD}(t)$, replaces the V_{CC} in Equation (A2) for calculating $i_G(t)$.

$$i_G(t) = \frac{v_{AGD}(t)-v_{GE}(t)}{R_G+R_D} \tag{A8}$$

The gate voltage is a threshold voltage, $V_{GE,th}$, and the instantaneous collector current, $i_C(t)$, function during this period.

$$v_{GE}(t) = V_{GE,th} + \frac{i_C(t)}{g_{ms}} \tag{A9}$$

Stage IV: *Active voltage slope control period* – After the collector current reaches load current I_L, the collector current is constant. Hence, the gate voltage stays clamped to $v_{GE,th} + I_L/g_{ms}$. The gate current only discharges C_{GC} and leads to the decay of V_{CE}.

$$\frac{dv_{CE}(t)}{dt} = -\left[\frac{dv_{GC}(t)}{dt}\right] = -\left[\frac{i_G(t)}{C_{GC}}\right]$$

$$= -\left[\frac{v_{AGD}(t)-(V_{GE,th}+\frac{I_L}{g_{ms}})}{R_G}\right]\frac{1}{C_{GC}} \qquad \text{(A10)}$$

AGD automatically adjusts $v_{AGD}(t)$ to attain the set voltage slope. Here, C_{GC} is the sum of internal and external Miller capacitors.

$$C_{GC} = C_{GC,int} + C_{GC,ext} \qquad \text{(A11)}$$

Stage V: *Gate charge period* – When the v_{GE} reaches zero, the IGBT moves to the saturation region of operation, and the gate voltage continues to increase to V_{CC}.

II. ASM Turn Off Behavior

Stage I: *Gate discharge delay* – When a negative V_{REF} is applied to the ASM it initiates the IGBT turn-off. v_{GE} starts decaying, and the IGBT enters the active region. AGD does not receive dv/dt feedback; therefore, ASM operates as an IGBT with a resistive gate drive during this period.

The mathematical equations governing the turning off process are similar to those of the turning on process. The IGBT input capacitor C_{ies} is discharged, and the gate voltage v_{GE} can be calculated from

$$v_{GE}(t) = V_{EE}\left[1 - e^{-t/\tau_G}\right] \qquad \text{(A12)}$$

Gate current can be calculated from

$$i_G(t) = \frac{V_{EE} - v_{GE}(t)}{R_G + R_d} \tag{A13}$$

Stage II: *Voltage overshoot period* – Initially, due to the absence of the dv/dt feedback, the voltage rise is rapid until AGD gains control over the dv/dt rate of the IGBT. The IGBT switching equations with resistive GD are valid in this region.

When the gate voltage reaches the minimum value to carry the load current, which is $V_{GE,th} + {I_L}/{g_{ms}}$, IGBT enters the active region

Gate current only charges C_{GC} and leads to the rise in $v_{CE}(t)$.

$$\frac{dv_{CE}(t)}{dt} = -\left[\frac{dv_{GC}(t)}{dt}\right] = -\left[\frac{i_G(t)}{C_{GC}}\right]$$

$$= -\left[\frac{V_{EE} - V_{GE,th} - \frac{I_L}{g_{ms}}}{R_G}\right]\left[\frac{1}{C_{GC,int} + C_{GC,ext}}\right] \tag{A14}$$

Stage III: *Active voltage slope control stage* – AGD controls the voltage rise as set by $(dv/dt)_{REF}$. Since the IGBT is still in the active region, the mathematical equations describing $dv_{CE}(t)/dt$ from the previous stage remain valid. However, $i_G(t)$ is determined by the $(dv/dt)_{REF}$. Hence, drive voltage $v_{AGD}(t)$ replaces V_{EE} in Equation (A13) for calculating $i_G(t)$.

$$\frac{dv_{CE}(t)}{dt} = -\left[\frac{v_{AGD}(t) - V_{GE,th} - \frac{I_L}{g_{ms}}}{R_G}\right] \times \left[\frac{1}{C_{GC,int} + C_{GC,ext}}\right] \tag{A15}$$

Stage IV: *Active current slope control stage* – AGD controls the collector current rise set by the $(di/dt)_{REF}$. The IGBTs static transfer characteristics define the IGBT collector current as in (A6). The rate of change of collector current can be calculated from (A7). Similar to when the IGBT turning on, $i_G(t)$ can be calculated from (A8). The gate voltage is a function of threshold voltage and collector current and can be calculated from (A9).

Stage V: *Tail current and gate discharge* – The collector current reaches the level of tail current. Therefore, it cannot be actively reduced further by AGD and relies solely on the IGBT characteristics and other external passive components. The tail current decays, and after v_{GE} decreases until it reaches V_{EE}.

B. Calculation of g_{ms} from transfer characteristics, and the control parameters di_C/dt and dv_{CE}/dt control.

IGBT transconductance (g_{ms}) is not constant and depends on I_C, $V_{GE,}$ and T_J. AGD small signal models are linearized around an operating point, and g_{ms} is calculated around the same operating point (I_{C0}, V_{GE0}, T_{J0}). g_{ms} should be calculated in the linear region of the IGBT transfer characteristics. In the low-current knee region, calculating g_{ms} will result in unusually low values.

From the transfer characteristics in the IGBT datasheet, the g_{ms} value at the selected operating point (I_{C0} = 40A and T_{J0} = 125°C) can be calculated using the equation below.

$$g_{ms} = \frac{\Delta I_C}{\Delta V_{GE}} \qquad \text{(B1)}$$

Transfer characteristics for the IGBT *VS-GT80DA120U* are shown in Figure B.1. The g_{ms} at the operating point can be calculated to be 40A/V.

$$g_{ms} = \frac{50-30\ (A)}{8.5-8\ (V)} = 40A/V$$

The IGBT control parameters for the di_C/dt and dv_{CE}/dt control loops are given in .

Table B. 1

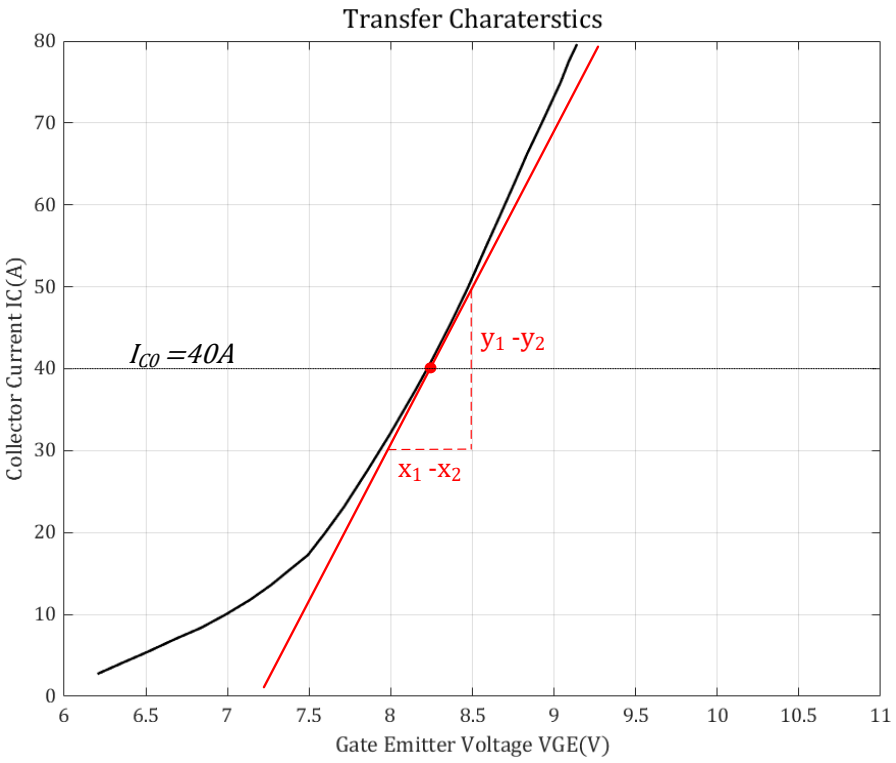


Figure B.1: *VS-GT80DA120U* IGBT transfer characteristics, and the calculation of g_{ms} [81].

Table B. 1: IGBT control parameters for the di_C/dt and dv_{CE}/dt control loops

Parameter	Value	Unit
Kp	40	-
A_{DC}	90	dB
GBW	40	MHz
$f_{c,Amp}$	7.65	MHz
R_P	400k	Ω
C_P	10	pF
R_G	30	Ω
C_{GC} $(= C_{GC,int}+C_{GC,ext})$	1.2	nF
A_1	16/3	-
R_F	50	Ω

C_F	100	pF
C_{GE} (= $C_{GE,int}$+$C_{GE,ext}$)	40	nF
A_2	2	-
M	5×10^{-8}	H
g_{ms}	40	A/V

C. Small Signal V-I Relationship of an IGBT for ACB

A linear function can approximate the on-state characteristics of the IGBT.

$$v_{CE} = V_{CE,th}[v_{GE}, T_J] + R_{CE,on}[v_{GE}, T_J] i_C \quad \text{(C1)}$$

Linearization of Equation (C1) for small signal analysis, around a steady state operating point (I_{C0}, V_{GE0}, T_{J0}). We can treat slowly varying T_J as a constant when analyzing a fast electrical dynamic system and its small signal AC behavior.

$$f = v_{CE} = V_{CE,th}[v_{GE}] + R_{CE,on}[v_{GE}] i_C \quad \text{(C2)}$$

Applying the total differential with respect to i_C and v_{GE}

$$dv_{CE} = \frac{\partial f}{\partial v_{GE}} dv_{GE} + \frac{\partial f}{\partial i_C} di_C \quad \text{(C3)}$$

Differentiating with respect to i_C, $V_{CE,th}$, and $R_{CE,on}$ is considered a constant. Also differentiating with respect to v_{GE}, i_C is considered constant.

$$\frac{\partial f}{\partial i_C} = R_{CE,on0} \quad \text{(C4)}$$

$$\frac{\partial f}{\partial v_{GE}} = \frac{\partial V_{CE,th}}{\partial v_{GE}} + I_{C0} \frac{\partial R_{CE,on}}{\partial v_{GE}} \quad \text{(C5)}$$

Substituting (C4) and (C5) in Equation (C3)

$$\Delta v_{CE} = (\frac{\partial V_{CE,th}}{\partial v_{GE}} + I_{C0}\frac{\partial R_{CE,on}}{\partial v_{GE}})\Delta v_{GE} + R_{CE,on0}\Delta i_C \quad \text{(C6)}$$

$$\Delta v_{CE} = A\Delta v_{GE} + B\Delta i_C$$

For multiple IGBTs operating in parallel, v_{CE} of all devices is dictated by the shared external circuit node. All parallel IGBTs experience the same v_{CE}, and the only variable that can redistribute current is v_{GE}.

Therefore, we can use the simplifying assumption $\Delta v_{CE} = 0$ for a small-signal model of the IGBT within a parallel group.

$$0 = A\Delta v_{GE} + B\Delta i_C$$

$$\Delta i_C = -\frac{A}{B}\Delta v_{GE} = K_{ACB}\Delta v_{GE} \quad \text{(C7)}$$

Where;

$$K_{ACB} = -\frac{1}{R_{CE,on0}}\left(\frac{\partial V_{CE,th}}{\partial v_{GE}} + I_{C0}\frac{\partial R_{CE,on}}{\partial v_{GE}}\right)$$

D. Calculation of K_{ACB} for an Operating Condition from the Datasheet

The V-I Characteristics curves provided in the datasheet can be used to obtain an approximate value of K_{ACB} for a given operating condition (V_{GE0}, I_{C0}, T_{J0}). Output characteristics curves obtained from the *VS-GT80DA120U* datasheet for T_J = 125 °C is shown in Figure D.1.

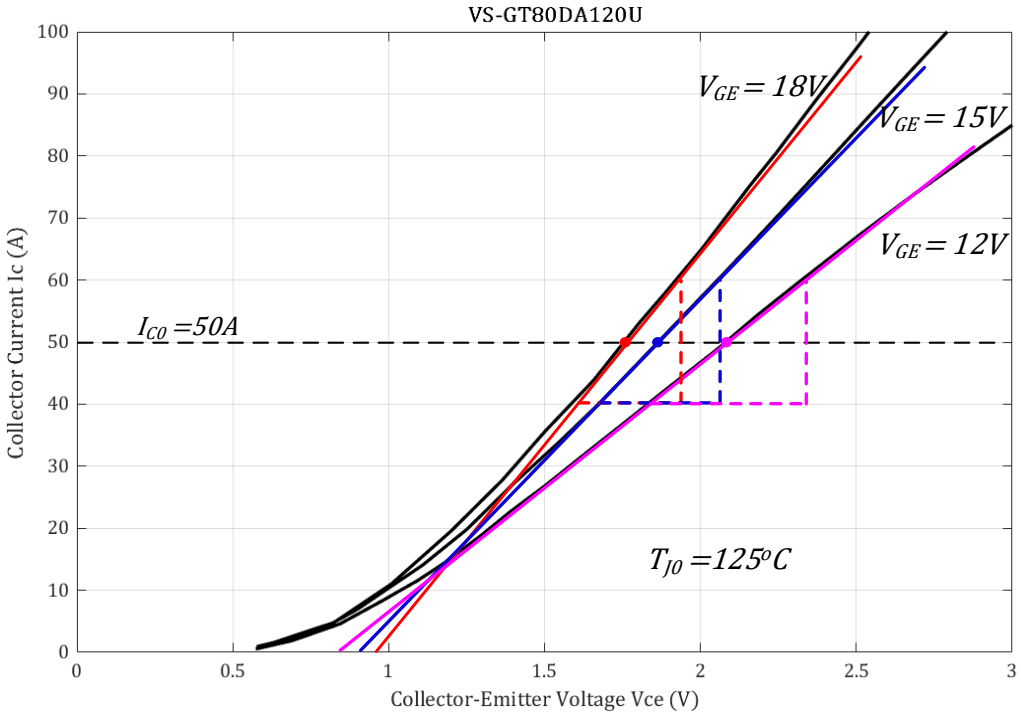


Figure D.1: Output characteristics curves extracted from the *VS-GT80DA120U* datasheet

The steps followed for calculating the K_{ACB} are given below.

Step 1: Calculate $R_{CE,on0}$ at an operating point (V_{GE0}, I_{C0}, T_{J0}) by fitting a line

$$R_{CE,on0} = \frac{\Delta V_{CE}}{\Delta I_C} = 0.01923$$

Step 2: Repeat the line fit for two gate voltages bracketing V_{GE0} ($V_{GE0} \pm \Delta V$). Calculate the $V_{CE,th}$ and $R_{CE,on}$ at each line fit.

For $V_{GE0} + \Delta V$:

$$V_{CE,th}\,[V_{GE0} + \Delta V] = 0.9230\,V$$

$$R_{CE,on}[V_{GE0} + \Delta V] = \frac{\Delta V_{CE}}{\Delta I_C} = 0.01538$$

For $V_{GE0} - \Delta V$:

$$V_{CE,th}\,[V_{GE0} - \Delta V] = 0.7884\,V$$

$$R_{CE,on}[V_{GE0} - \Delta V] = \frac{\Delta V_{CE}}{\Delta I_C} = 0.025$$

Step 3: Compute the gate sensitivities

$$\frac{\partial V_{CE,th}}{\partial V_{GE}} \approx \frac{V_{CE,th}\,[V_{GE0} + \Delta V] - V_{CE,th}\,[V_{GE0} - \Delta V]}{2\Delta V} = 0.02243$$

$$\frac{\partial R_{CE,on}}{\partial V_{GE}} \approx \frac{R_{CE,on}\,[V_{GE0} + \Delta V] - R_{CE,on}\,[V_{GE0} - \Delta V]}{2\Delta V} = -0.001603$$

Step 4: Calculate K_{ACB}

$$K_{ACB} = -\frac{1}{R_{CE,on0}}\left(\frac{\partial V_{CE,th}}{\partial V_{GE}} + I_{C0}\frac{\partial R_{CE,on}}{\partial V_{GE}}\right) = 3.0015$$

The K_{ACB} calculated using this approach is an approximate value because the datasheet output curves are not provided for small variations of V_{GE}. When selecting two gate voltage curves bracketing V_{GE0}, choose curves as close as possible for greater accuracy.

E. Small Signal V-I Relationship of an IGBT with Variable Junction Temperature, and the Stability Criterion

I. Small Signal V-I Characteristics of an IGBT with PTC

Linearizing the IGBT on state Equation (C1), around the operating point (V_{GE0}, I_{C0}, T_{J0}) with respect to the variables v_{GE}, i_C, and T_J.

The resulting modified linearized small signal equation becomes

$$\Delta v_{CE} = A\Delta v_{GE} + B\Delta i_C + C\Delta T_J \qquad \text{(E1)}$$

Where;

$$C = \frac{\partial V_{CE,th}}{\partial T_J} + I_{C0}\frac{\partial R_{CE,on}}{\partial T_J}$$

Now applying the assumption of $\Delta v_{CE} = 0$ for parallel IGBTs

$$\Delta i_C = -\frac{A}{B}\Delta v_{GE} - \frac{C}{B}\Delta T_J$$

In the Laplace domain

$$\Delta I_C(s) = K_{ACB}\Delta V_{GE}(s) + K_{TH}\Delta T_J(s) \quad \text{(E2)}$$

Where

$$K_{TH} = -\frac{1}{R_{CE,on0}}\left(\frac{\partial V_{CE,th}}{\partial T_J} + I_{C0}\frac{\partial R_{CE,on}}{\partial T_J}\right)$$

II. Stability Criterion for PTC Thermal Feedback

Using the principle of time scale separation, we can assume $\Delta v_{GE}(t) = 0$,

A change in current for a small increase in T_J can be obtained using Equation (E2).

$$\mathrm{G_{TH}}(\mathrm{s}) = \frac{\Delta I_C(s)}{\Delta T_J(s)} = K_{TH} \quad \text{(E3)}$$

Modeling of the IGBT heating in the on-state, the power dissipation of the IGBT is

$$p_{dis} = v_{CE} \times i_C$$

Linearizing around the operating point (V_{GE0}, I_{C0}, T_{J0})

$$\Delta p_{dis} = \frac{\partial p_{dis}}{\partial i_C}\Delta i_C + \frac{\partial p_{dis}}{\partial v_{CE}}\Delta v_{CE}$$

Since we assume $\Delta v_{CE} = 0$, and in the Laplace domain

$$G_{dis}(s) = \frac{\Delta P_{dis}(s)}{\Delta I_C(s)} = V_{CE0} \quad \text{(E4)}$$

The temperature increase in the junction can be calculated by (T_C is considered as a constant)

$$C_{TH}\frac{d\Delta T_j}{dt} = p_{dis} - \frac{\Delta T_j}{R_{TH,J-C}}$$

With $\tau_{TH} = R_{TH,J\text{-}C} \times C_{TH}$

$$\tau_{\mathrm{TH}}\frac{d\Delta T_j}{dt} + \Delta T_j = R_{TH,J-C}\Delta P_{dis}$$

We can obtain the relationship in the Laplace domain.

$$(\tau_{TH,J-C}s + 1)\Delta T_J(s) = R_{TH,J-C} \times \Delta P_{dis}(s)$$

$$Z_{TH,J-C}(s) = \frac{\Delta T_J(s)}{\Delta P_{dis}(s)} = \frac{R_{TH,J-C}}{\tau_{TH,J-C}s+1} \qquad \text{(E5)}$$

$R_{TH,J\text{-}C}$, C_{TH}, $\tau_{TH,J\text{-}C}$ are junction to case thermal resistance, junction thermal capacitance, and junction to case thermal time constant, respectively.

The closed-loop block diagram for thermal feedback is shown in Figure E.1.

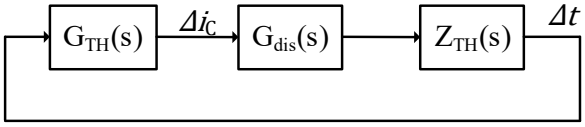


Figure E.1: Closed-loop block diagram for PTC thermal feedback phenomenon.

The stability of the thermal feedback can be analyzed using the closed-loop transfer function.

$$T(s) = \frac{K_{TH}V_{CE0}R_{TH,J-C}}{\tau_{TH,J-C}s+(1+K_{TH}V_{CE0}R_{TH,J-C})} \qquad \text{(E6)}$$

The stability criterion is that the pole must be in the left half-plane.

Since $\tau_{TH,J\text{-}C} > 0$ and $K_{TH} < 0$ we can write

$$|K_{TH}|V_{CE0}R_{TH,J-C} < 1 \qquad \text{(E7)}$$

References

[1] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC Microgrid Protection: A Comprehensive Review," *IEEE J. Emerg. Sel. Top. Power Electron.*, pp. 1–1, Mar. 2019.

[2] M. E. Baran and N. R. Mahajan, "DC distribution for industrial systems: Opportunities and challenges," *IEEE Trans. Ind. Appl.*, vol. 39, no. 6, pp. 1596–1601, Nov. 2003.

[3] D. K. J. S. Jayamaha, N. W. A. Lidula, and A. D. Rajapakse, "Protection and grounding methods in DC microgrids: Comprehensive review and analysis," *Renewable and Sustainable Energy Reviews*, vol. 120, Mar. 2020.

[4] M. Farhadi and O. A. Mohammed, "Protection of multi-terminal and distributed DC systems: Design challenges and techniques," *Electric Power Systems Research*, vol. 143, pp. 715–727, Feb. 2017.

[5] Y. Chen, S. Chakraborty, A. Zamzam, and J. Wang, "End-to-end microgrid protection using distributed data-driven methods," *Appl. Energy*, vol. 391, Aug. 2025.

[6] G. Emmers, T. Van Acker, S. Ravyts, and J. Driesen, "The impact of protection devices on the availability of low-voltage direct current microgrids," *Reliab. Eng. Syst. Saf.*, vol. 262, Oct. 2025.

[7] R. Schmerda, R. Cuzner, R. Clark, D. Nowak, and S. Bunzel, "Shipboard Solid-State Protection: Overview and Applications," *IEEE Electrification Magazine*, vol. 1, no. 1, pp. 32–39, Nov. 2013, doi: 10.1109/mele.2013.2273395.

[8] L. Qi *et al.*, "Solid-State Circuit Breaker Protection for DC Shipboard Power Systems: Breaker Design, Protection Scheme, Validation Testing," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 952–960, Mar. 2020.

[9] H. Pugliese and M. Von Kannewurff, "Discovering DC: A primer on dc circuit breakers, their advantages, and design," *IEEE Ind. Appl. Mag.*, vol. 19, no. 5, pp. 22–28, 2013.

[10] P. Dworakowski, J. D. Páez, W. Grieshaber, A. Bertinato, and E. Lamard, “Protection of radial MVDC electric network based on DC circuit breaker and DC fuses,” *International Journal of Electrical Power and Energy Systems*, vol. 153, Nov. 2023.

[11] A. Jaafari, S. Mohsenzade, and A. A. Razi-Kazemi, “An adaptive current commutation for hybrid DC circuit breaker,” *Electric Power Systems Research*, vol. 247, Oct. 2025.

[12] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, “Assembly HVDC breaker for HVDC grids with modular multilevel converters,” *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 931–941, Feb. 2017.

[13] M. Bhaskar and B. Chowdhury, “Comparative Analysis of Hybrid DC Breaker and Assembly HVDC Breaker,” in *2017 North American Power Symposium (NAPS)*, Morgantown, WV, USA, 2017, pp. 1–6.

[14] K. K. M. Siu, C. N. M. Ho, and D. Li, “Design and Analysis of a Bidirectional Hybrid DC Circuit Breaker Using AC Relays with Long Life Time,” *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2889–2900, Mar. 2021.

[15] Q. Yi *et al.*, “Snubber and Metal Oxide Varistor Optimization Design of Modular IGCT Switch for Overvoltage Suppression in Hybrid DC Circuit Breaker,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 4, pp. 4126–4136, Aug. 2021.

[16] Z. Chen *et al.*, “Analysis and Experiments for IGBT, IEGT, and IGCT in Hybrid DC Circuit Breaker,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 4, pp. 2883–2892, Apr. 2018.

[17] W. Lv, T. Zheng, Y. Yang, R. Li, and S. Sun, “Novel fault isolation scheme under protection failure in MVDC distribution networks without DC circuit breakers,” *International Journal of Electrical Power and Energy Systems*, vol. 148, Jun. 2023.

[18] X. Zhang *et al.*, “A State-of-the-Art 500-kV Hybrid Circuit Breaker for a dc Grid: The World’s Largest Capacity High-Voltage dc Circuit Breaker,” *IEEE Industrial Electronics Magazine*, vol. 14, no. 2, pp. 15–27, Jun. 2020.

[19] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, “A Review of Solid-State Circuit Breakers,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[20] S. Johan and K. Berg, “Solid State Circuit Breakers In Medium Voltage Direct Current Systems Designing, improving and optimizing solid state circuit breakers for MVDC applications,” Norwegian University of Science and Technology, 2018.

[21] D. Bortis, P. Steiner, J. Biela, and J. Kolar, “Double-stage gate drive circuit for parallel connected IGBT modules,” in *IEEE Transactions on Dielectrics and Electrical Insulation*, Aug. 2009, pp. 1020–1027.

[22] H. Ghorbani, V. Sala, A. P. Camacho, and J. L. R. Martinez, “A simple closed-loop active gate voltage driver for controlling di C /dt and dv CE /dt in IGBTs,” *Electronics (Switzerland)*, vol. 8, no. 2, Feb. 2019.

[23] L. Yanick, K. Johann, and L. Matti, “ Active gate drive circuit ,” US20140375362A1, 2014

[24] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, P. Crolla, and G. M. Burt, “Optimizing the roles of unit and non-unit protection methods within DC microgrids,” *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 2079–2087, 2012.

[25] J. Yang, J. E. Fletcher, and J. O’Reilly, “Short-circuit and ground fault analyses and location in VSC-based DC network cables,” *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827–3837, 2012.

[26] M. F. Roslan *et al.*, “State-of-the-art on advanced technologies of solid-state circuit breaker for reliable and sustainable power supply: A bibliometric analysis and future guidelines,” *Alexandria Engineering Journal*, vol. 104, pp. 636–664, Oct. 2024.

[27] M. Moradian, T. T. Lie, and K. Gunawardane, “DC Circuit Breaker Evolution, Design, and Analysis,” Sep. 01, 2023, *Multidisciplinary Digital Publishing Institute (MDPI)*.

[28] IEC, “Medium voltage DC (MVDC) grids for an all-electric society,” 2025. [Online]. Available: https://www.iec.ch/basecamp/medium-voltage-dc-mvdc-grids-all-electric-society

[29] IEC 61936-2, *Power installations exceeding 1 kV AC and 1,5 kV DC-Part 2: DC*. 2021.

[30] C. M. Franck, “HVDC circuit breakers: A review identifying future research needs,” *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, Apr. 2011.

[31] X. Yan *et al.*, “Snubber Branch Design and Development of Solid-State DC Circuit Breaker,” *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 13042–13051, Oct. 2023.

[32] M. Bruckmann, R. Sommer, M. Fasching, and J. Sigg, “Series connection of high voltage IGBT modules,” in *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, IEEE, 1998, pp. 1067–1072.

[33] E. Taherzadeh, H. Radmanesh, S. Javadi, and G. B. Gharehpetian, “Circuit breakers in HVDC systems: state-of-the-art review and future trends,” *Protection and Control of Modern Power Systems*, vol. 8, no. 1, Dec. 2023.

[34] N. Bayati and M. Savaghebi, “Protection systems for dc shipboard microgrids,” *Energies (Basel).*, vol. 14, no. 17, Sep. 2021.

[35] Jurgen K Steinke, P. Maibach, G. Ortiz, F. Canales, and P. Steimer, “MVDC Applications and Techology,” in *PCIM Europe* , G Ortiz, Ed., 2019.

[36] P. Simiyu and I. E. Davidson, “MVDC railway traction power systems; state-of-the art, opportunities, and challenges,” *Energies (Basel).*, vol. 14, no. 14, Jul. 2021.

[37] L. de Oliveira-Assis *et al.*, “Optimal energy management system using biogeography based optimization for grid-connected MVDC microgrid with photovoltaic, hydrogen system, electric vehicles and Z-source converters,” *Energy Convers. Manag.*, vol. 248, Nov. 2021.

[38] IEEE Std 1709, *IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships*. IEEE, 2018.

[39] IEC, *IEC 61660:Short circuit currents in DC auxiliary installations in power plants and substations - Part 1: Calculation of short-circuit currents*. 1997.

[40] IEEE std C37.14, *IEEE Standard for DC (3200 V and below) Power Circuit Breakers Used in Enclosures*. 2015.

[41] C. Gu, P. Wheeler, A. Castellazzi, A. J. Watson, and F. Effah, “Semiconductor devices in solid-state/hybrid circuit breakers: Current status and future trends,” *Energies (Basel).*, vol. 10, no. 4, Apr. 2017.

[42] A. Schroedermeier and A. Rockhill, “Design and Operation of a Medium Voltage Pulse Test Apparatus for Short-Circuit Testing of DC Solid State Circuit Breakers,” in *2021 ECCE - Proceedings*, IEEE, 2021, pp. 5716–5722.

[43] S. Xiu *et al.*, “Synthetic test circuit with two-level voltage source for HVDC circuit breakers,” *IET Generation, Transmission and Distribution*, vol. 17, no. 8, pp. 1857–1869, Apr. 2023.

[44] M. Monadi, M. A. Zamani, J. I. Candela, A. Luna, and P. Rodriguez, “Protection of AC and DC distribution systems Embedding distributed energy resources: A comparative review and analysis,” *Renew. Sustain. Energy Rev.*, vol. 51, pp. 1578–1593, Aug. 2015.

[45] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, “Series-connected IGBTs using active voltage control technique,” *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4083–4103, 2013.

[46] P. R. Palmer and H. S. Rajamani, “Active voltage control of IGBTs for high power applications,” *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 894–901, 2004.

[47] B. Masoomeh, W. R. Tonny, and Z. E.-K. Walid, “Clamping system for series connected IGBTs to avoid transient break down voltages,” in *24th Nordic Insulation Symposium on Materials, Components and Diagnostics*, Sep. 2017.

[48] “IGBT Gate Driver Reference Design for Parallel IGBTs With Short-Circuit Protection and External BJT Buffer,” Dec. 2016. [Online]. Available: www.ti.com

[49] S. Bontemps, “Parallel Connection of IGBT and MOSFET Power Modules,” 33700 Merignac, France, Nov. 2004. [Online]. Available: www.advancedpower.com

[50] Y. Wang, A. T. Bryant, P. R. Palmer, S. J. Finney, M. Abu-Khaizaran, and G. Li, “An analysis of high power IGBT switching under cascade active voltage control,” in *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, 2005, pp. 806–812.

[51] Y. Zhang, S. Sobhani, and R. Chokhawala, “Snubber Considerations for IGBT Applications,” 233 Kansas St., El Segundo, CA, 90245 USA. [Online]. Available: www.irf.com

[52] L. Yue, I. Lee, and X. Yao, “A Review of Voltage Sharing Control Methods for Series-connected IGBTs for Applications in Pulsed Power Generation,” in *Proceedings 2018 IPMHVC - IEEE*, Jackson, WY, USA, 2018, pp. 397–402.

[53] Y. Jiang, T. Lu, L. Yuan, Z. Zhao, and F. He, “Simulation analysis of active clamping circuit with status feedback for HV-IGBTs,” in *Proceedings - 2014 International Power Electronics and Application Conference and Exposition, IEEE PEAC 2014*, Feb. 2014, pp. 1172–1176.

[54] B. Kim, Heung-Jin ju, Kwang-Cheol KO, and E. Hotta, “Active Clamping Circuit to Suppress Switching Stress on a MOS-Gate-Structure-Based Power Semiconductor for Pulsed-Power Applications,” *IEEE Transactions on Plasma Science*, vol. 38, no. 8, 2011.

[55] R. Withanage, N. Shammas, and S. Tennakoon, “Series connection of Insulated Gate Bipolar Transistors(IGBTs),” EPE Association, 2005.

[56] M. Chen, Z. Xiong, Y. Zhang, E. Zhu, Y. Zhao, and Z. Ma, “IGBT Overvoltage Protection Based on Dynamic Voltage Feedback and Active Clamping,” *Applied Sciences (Switzerland)*, vol. 13, no. 2, Jan. 2023.

[57] I. Baraia, J. A. Barrena, G. Abad, J. M. C. Segade, and U. Iraola, “An experimentally verified active gate control method for the series connection of IGBT/diodes,” *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 1025–1038, 2012.

[58] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, “Series-connected IGBTs using active voltage control technique,” *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4083–4103, 2013.

[59] Y. Wang, A. T. Bryant, P. R. Palmer, S. J. Finney, M. Abu-Khaizaran, and G. Li, “An analysis of high power IGBT switching under cascade active voltage control,” in *Conference Record - IEEE IAS Annual Meeting*, 2005, pp. 806–812.

[60] I. Lizama, “New gate drive unit concepts for IGBTS and reverse conducting IGBTS,” Ph.D. dissertation, Dresden University of Technology, 2017.

[61] Y. Lobsiger and J. W. Kolar, “Closed-loop di/dt and dv/dt IGBT gate driver,” *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3402–3417, Jun. 2015.

[62] Renesas, “Usage Notes for Paralleled IGBT,” Dec. 2018.

[63] Hitachi Energy, “Paralleling of IGBT modules.” Accessed: Dec. 19, 2024. [Online]. Available: www.hitachienergy.com/semiconductors

[64] V. Andreas and H. Michael, *IGBT Modules Technologies, Driver and Application*, 3rd ed. Munich: Infineon Technologies AG, 2017.

[65] N. Oborny, “Understanding Smart Gate Drive,” 2015. [Online]. Available: www.ti.com

[66] N. Idir, R. Bausière, and J. J. Franchaud, “Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors,” *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 849–855, Jul. 2006.

[67] Lobsiger and Yanick, “Closed-Loop IGBT Gate Drive and Current Balancing Concepts,” ETH Zurich, 2014. [Online]. Available: https://doi.org/10.3929/ethz-a-010432443

[68] M. Blank, T. Glück, A. Kugi, and H. P. Kreuter, “Slew rate control strategies for smart power ICs based on iterative learning control,” in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, IEEE, 2014, pp. 2860–2866. doi: 10.1109/APEC.2014.6803710.

[69] F. Zhang, X. Yang, Y. Ren, L. Feng, W. Chen, and Y. Pei, “Advanced active gate drive for switching performance improvement and overvoltage protection of high-power IGBTs,” *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3802–3815, May 2018.

[70] J. Dodge, “How to Make Linear Mode Work.” Accessed: May 23, 2024. [Online]. Available: https://forums.futura-sciences.com/attachments/electronique/438614d1620122990-mosfet-lineaire-microsemi-power-an-make-linear-mode-work.pdf

[71] S. Jayamaha, C. N. M. Ho, and A. Rajapakse, “Parallel/Series Connected Standardized Active Switching Modules for High Power DCCBs in MVDC Networks,” *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 9602–9613, Aug. 2024.

[72] S. Jayamaha, C. N. M. Ho, and A. Rajapakse, “Electro-Thermal Design: Standardized Hybrid DC Breaker Architecture for Scalable Operation in MVDC Networks,” in *IEEE - ECCE*, Phoenix, AZ, USA, 2024, pp. 707–713.

[73] “High Accuracy AC Current Measurement Reference Design Using PCB Rogowski Coil Sensor TI Designs High Accuracy AC Current Measurement Reference Design Using PCB Rogowski Coil Sensor,” Jun. 2016. [Online]. Available: www.ti.com

[74] onsemi, “AND9100/D Paralleling of IGBTs,” 2014. [Online]. Available: www.onsemi.com

[75] D. Bortis, P. Steiner, J. Biela, and J. Kolar, “Double-stage gate drive circuit for parallel connected IGBT modules,” in *IEEE Trans Dielectr Electr Insul*, Aug. 2009, pp. 1020–1027.

[76] STMicroelectronics, “IGBT Datasheet Tutorial, AN4544 Application note,” 2014. Accessed: Aug. 03, 2024. [Online]. Available: https://www.st.com/resource/en/application_note/an4544-igbt-datasheet-tutorial-stmicroelectronics.pdf

[77] W. Ali, A. Bissal, and M. März, “Experimental Verification of a Hybrid DC Breaker’s Solid-State Branch, Utilizing Discrete IGBTs, for LVDC Systems,” in *IEEE- ECCE*, Nashville, TN, USA, 2023, pp. 1410–1416.

[78] R. Wu, H. Wang, K. Ma, P. Ghimire, F. Iannuzzo, and F. Blaabjerg, “A temperature-dependent thermal model of IGBT modules suitable for circuit-level simulations,” in *IEEE- ECCE* , Nov. 2014, pp. 2901–2908.

[79] I. Lizama, R. Alvarez, S. Bernet, and M. Wagner, “Static Balancing of the Collector Current of IGBTs Connected in Parallel,” in *IECON 2014 - 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Dallas, TX, USA, 2014, pp. 1827–1833.

[80] A. Li, K. Allen, A. Dholakia, and N. Kothuri, “Using the Fast Serial Interface (FSI) With Multiple Devices in an Application,” 2023. [Online]. Available: www.ti.com

[81] Vishay Semiconductors, “vs-gt80da120u.” Accessed: Jul. 03, 2023. [Online]. Available: www.vishay.com