RELAY PERFORMANCE ON THE 500 KV SERIES–COMPENSATED DORSEY–FORBES–CHISAGO TRANSMISSION LINE

A thesis submitted to

The Faculty of Graduate Studies

in Partial Fulfillment of the Requirements for the Degree

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SUMMARY

Over the decades, methods have been sought to maximize the power transfer capability of existing transmission line systems. Series compensation, using capacitors to compensate the inductive reactance of a long transmission line, has been widely used for upgrading existing power line systems. Besides increasing the power transfer capability of the existing transmission line system, series compensation can also maximize the usage of a transmission system by optimizing the sharing of active power between alternative paths connecting the busbars. Since the reactive power generation in a series capacitor increases as the transmitted current increases, series compensation can improve voltage control and reactive power balance in a transmission line system.

Although series compensation is very effective in raising the transient stability limit and optimizing the sharing of active power between parallel paths of a transmission system, it also gives rise to some problems such as self–excitation, negative–damping, subsynchronous resonance and voltage inversion [1]. This thesis mainly deals with the problems introduced by the varied degree of involvement of the MOV on different kind of faults at different locations. The series capacitors used in this thesis are protected from overvoltage under heavy fault conditions by the inclusion of an MOV (Metal Oxide Varistor). The operating relationship between the series–capacitor and the MOV was studied.

Fault simulations were done on the Manitoba Hydro Dorsey–Forbes–Chisago 500 kV transmission line system by using the Manitoba HVDC centre's EMTDC [2] program. The feasibility of modifying the existing GE relaying system which mainly consists of a positive sequence directional comparison scheme, a negative sequence directional comparison scheme and a direct tripping scheme was studied. In addition, the performance of a GEC Micromho protection scheme on the series–compensated transmission line system was studied to see the possibility of using it on the future compensated system. A comparison of performance between the two relaying schemes on the planned series–compensated line was done.

Moreover, a study on an adaptive protection scheme using a DFT (Discrete Fourier Transform) was included.

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Finally, I wish to thank my parents for their patience and understanding during the preparation of this thesis.

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CHAPTER 1

INTRODUCTION

1.1 Role of protection:

In order to generate electric power and transmit it to customers a vast amount of money must be spent on equipment, so that it is important to run it at peak efficiency and protect it from accidents. Unfortunately, a certain number of accidents are inevitable as insulation deteriorates or unforeseen things occur, such as strokes of lightning or the entry of birds into the equipment.

Insulation breakdowns are called 'faults' by relay engineers. When one occurs it is liable to be very expensive because of the damage that can be done by the tremendous amount of electrical energy in modern power systems. Protective relays minimize this damage and expense by locating the fault immediately and opening the correct breakers to isolate the faulted circuit. Therefore it is obvious that reliability, speed and selectivity are the most desirable qualities of a protective relay.

1.1.1 Nature of the relay:

A protective relay is a device which responds to abnormal conditions on an electrical power system to control a circuit breaker, so as to isolate the faulty section of the system with the minimum interruption to service. To achieve this function, relays must be able to decide promptly which circuit breakers are to trip in order to isolate only the faulted section.

Relays recognize and locate faults by constantly measuring electrical quantities from the system. These quantities will all change between normal and abnormal conditions. The basic electrical quantities which may change when a fault occurs are current, voltage, phase–angle and frequency. It is generally necessary to provide relays responding to more than one of these conditions because, for instance, the current during a fault with minimum generation may be less than load current during maximum generation and power–factor may be as low

during a power swing as during a fault. Fig. 1.1 [3] shows how the relays are arranged to trip only the breakers which isolate the faulted circuit and yet to overlap their zones of operation so as to leave no unprotected spots.

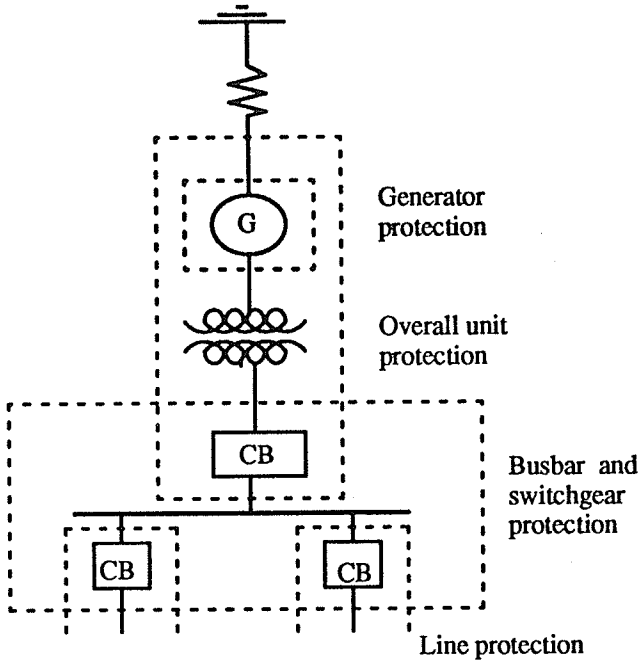


Figure 1.1 Zones of protection

In order to keep the size and cost of relays to reasonable values, the enormous currents and voltages of the actual primary circuit are reduced to relatively small values by current transformers (ct' s) and potential transformers (pt' s). The relays measure these secondary electrical quantities and operate when the magnitude of one of them is abnormal or when the ratio between two of them is abnormal.

All protective relays have two positions, the normal position, usually with their contact circuit open, and the fault position usually with their contact circuit closed. A relay is changed to the fault position when a fault occurs by the preponderance of abnormal operating quantities (such as overcurrent) over normal restraining quantities (such as voltage or through–fault current).

Fig. 1.2 [4] shows schematically the basic connections of a relay to the trip coil of the circuit breaker which controls the power supply to the protected circuit. When the relay contacts close, the high L/R ratio of the trip coil delays the build–up of current so that a fast breaker is tripped before the current reaches its steady value. For this reason, and because the duration of the trip coil current is only a few cycles, the relay contacts need to have a continuous rating of only 5 amperes and yet operate a 30 ampere trip coil 50 times without needing maintenance .

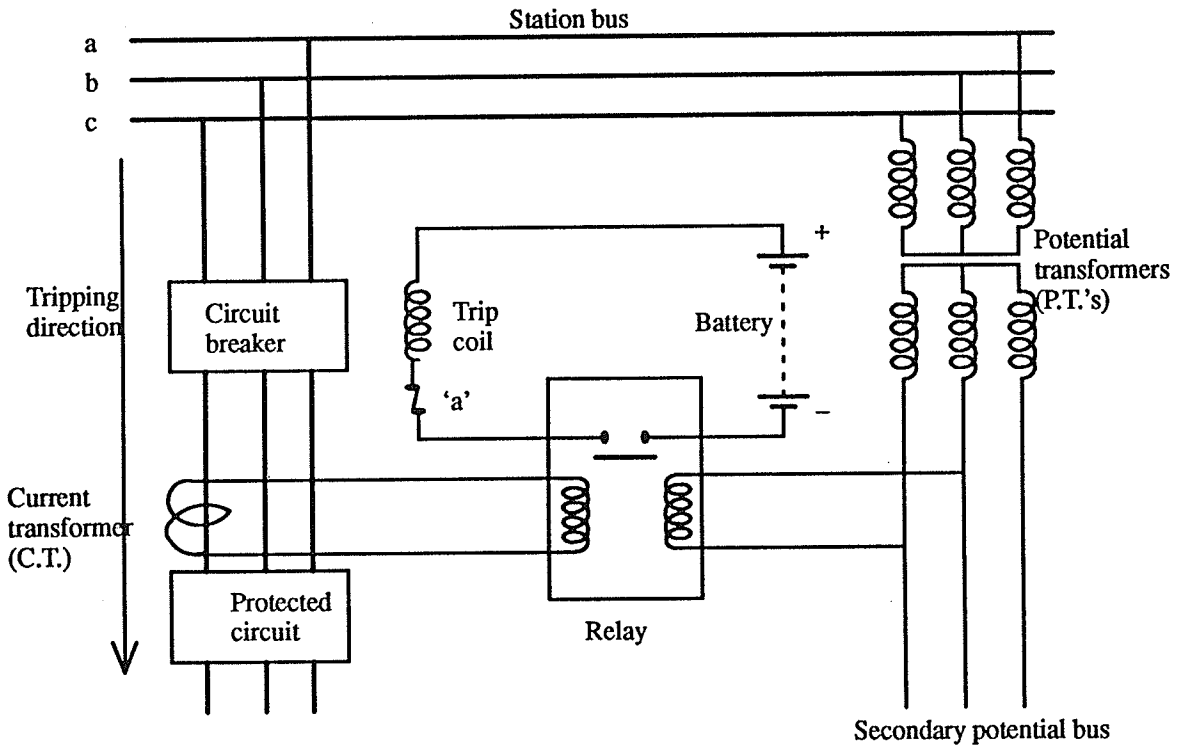


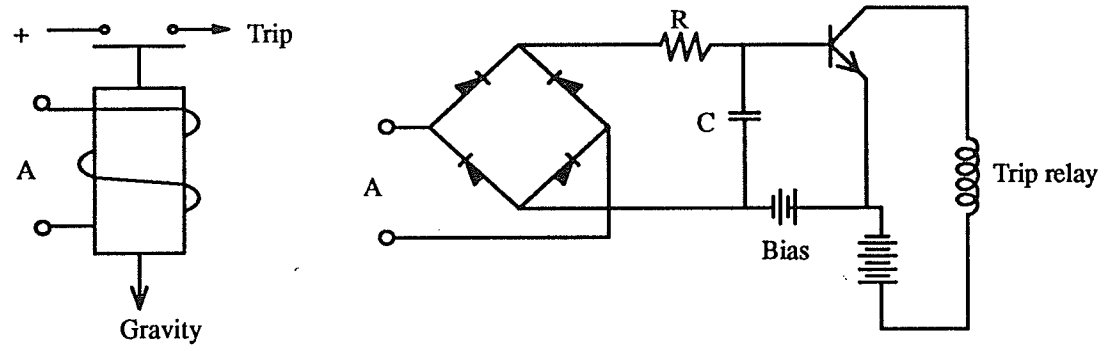
Figure 1.2 Basic connections of a protective relay

After the breaker has tripped, its auxiliary switch (marked 'a' in Fig. 1.2) opens the highly inductive trip coil circuit and the relay can reset when de–energized by the opening of the breaker. It is important however that the relay contacts do not chatter while trip current is flowing, otherwise they will be badly burned. This is ensured either by non–bounce design or by the use of a magnetic hold–in coil on the relay.

1.1.2 Level detectors and comparators:

A relay operates when the measured quantity changes, either from its normal value or in relation to another quantity. The operating quantity in most protective relays is the current entering the protected circuit. The relay may operate on current level against a standard bias or restraint, or it may compare the current with another quantity of the circuit such as the bus voltage or the current leaving the protected circuit.

In a simple electromagnetic relay, used as a level detector, gravity or a spring can provide the fixed bias or reference quantity, opposing the force produced by the operating current in an electromagnet. The spring is thus a means of calibration of the relay pick–up. In static relays the equivalent is a d.c. voltage bias, as shown in Fig. 1.3b [3].



(a) Electromagnetic (b) Semiconductor

Figure 1.3 Inherent level detectors

Since the fault level changes with generating conditions, it is seldom possible to obtain selectivity on the basis of current magnitude alone. Usually a time function is added so that the relay nearest the fault, which see the most current, will trip before relays in the unfaulted circuits.

It is difficult to obtain selectivity by measuring one quantity such as current, potential, phase–angle, etc., without using time delay. Hence most high–speed relays measure a desired quantity which is a combination of several simple quantities; for example, imped-

ance, current–ratio, etc., in which two simple quantities are compared in magnitude and/or phase relation.

1.1.3 Operating characteristic:

The most important operating characteristic of a single–input relay (level detector) is the relation between the input magnitude and the operating time [3], e.g. the time–current curve of a time–current relay.

Modern amplitude and phase comparator relays are virtually instantaneous but a curve of time versus the ratio of the inputs is of interest even though the time scale is in milli-seconds; for example, a time–impedance curve of a distance relay. In such relays, the most important characteristic is the ratio of the two input quantities at the threshold of operation for varying phase between them.

This operating characteristic is plotted on a polar graph whose ordinates are the real and imaginary components of A/B or B/A where A and B are the two quantities compared. The ordinates of the graph are $|A/B|\cos\varnothing$ and $j|A/B|\sin\varnothing$, where $\varnothing$ is the angle by which A leads B; this can be abbreviated as $|A/B|p$ and $|A/B|q$.

An example is the distance relay, where A is voltage and B is current, so that the ordinates of its operating characteristics are $|V/I|\cos\varnothing=R$ and $|V/I|\sin\varnothing=X$. This is generally referred to as the R–X diagram or the impedance diagram as shown in Fig. 1.4 [3]. Similarly, the components of I/V gives an admittance (G versus jB) diagram.

1.1.4 Main and backup protections:

In order to isolate any of the electrical equipment in case of trouble, each item must be separated from the others on each side of it by a circuit breaker. The relays themselves must be connected to trip only the breakers next to the protected unit, and the zone of protection of each relay must overlap the zones of the adjacent relays to ensure that there are no dead spots.

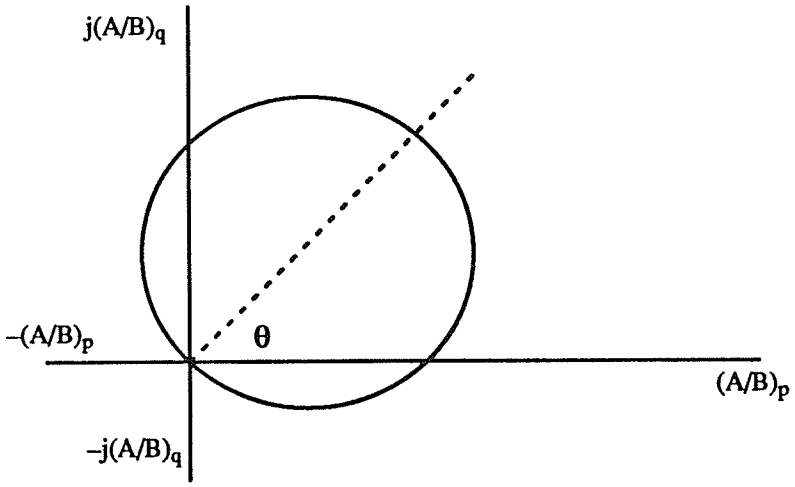


Figure 1.4 Typical relay characteristic plotted on α–plane

These relays are the main relays. In addition to this first line of defence there must be a second line of defence provided by back–up relays, which will clear the fault if the primary relays for some reason fail to operate. There are three kinds of back–up relays [4]:

(a) those which trip the same breaker if the main relay fails (Relay Back–up);

(b) those which open the next nearest breakers on the same bus in case one of the local breakers fails to open (Breaker Back–up), or in case there is a failure of the local secondary current or potential supplies or the a.c. wiring;

(c) those which operate from a neighboring station so as to back–up both relays and breakers and their supplies (Remote Back–up) in case of the failure of any local supply including the battery, or in case a circuit breaker or relay fails to function.

Relay back–up means literally the duplication of the main relays and their c.t's and p.t's, etc., but usually a compromise is employed resulting in the addition of a simple relay such as a time–overcurrent relay. The best relay back–up is a device using an entirely different principle, such as the gas detector relay in a transformer.

Breaker back–up is necessary when a feeder breaker fails to trip on a fault because the feeder fault then becomes virtually a busbar fault. It usually consists of a time–delay relay operated by the main relays and connected to trip all the other breakers on the bus if the proper breaker has not tripped within a half second after its trip coil was energized.

Remote back–up is provided by a relay at the next station in the direction towards the source which trips in a delayed time if the breaker in the faulted section is not tripped. It usually consists of an inverse time–current relay or by the second and third zones of a distance relay. This is the most widely used form of back–up protection.

1.1.5 Reclosing:

In cases where continuity of service cannot be maintained by quickly isolating the faulted circuit from the system, automatic reclosing relays are used to reconnect the circuit so that, if the fault is a transient one, the system is returned to normal operation.

Automatic reclosing is used mostly on overhead transmission and distribution lines because there is statistical evidence that 90% of the faults on such lines are caused by lightning or by objects passing near or through the lines (birds, tree branches, etc.) [4]. These conditions result in arcing faults which can be extinguished by opening the circuit breakers to de–energize the line. Reclosing immediately after the fault arc has been interrupted is hence a practical means of minimizing the interruption to service, especially at unattended stations.

Where there is only one transmission line between an important load and its power source, single pole switching is used , i.e. interrupting and reclosing only the faulted phase so that power is never completely cut off.

The combination of high–speed tripping and high–speed reclosing is nearly equivalent (as far as disturbance to the rest of the power system is concerned) to the ideal condition of eliminating faults.

1.2 Types of protection:

There are hundred of types of protection relays but the most important ones can be grouped under the headings, directional, overcurrent, differential, distance and pilot.

1.2.1 Overcurrent relays:

On less important circuits, such as distribution systems, only the cheapest relaying is justified, so that the local current is merely checked for magnitude only and the relay is simple and cheap [3].

This method is possible in distribution systems because the short–circuit is large compared with the load current and because the faulted section has the most current since it is fed from all the neighboring unfaulted circuits. Its selectivity is improved by adding a delaying means so that the operating time is inversely proportional to the current; with this arrangement the relay in the faulted section tends to trip first and clear the fault before the others can trip. Such relays are also used for back–up protection on transmission lines in case the more sophisticated primary relays should fail.

The time–current curve of an inverse–time relay of the electromagnetic type used to be a direct function of the B–H magnetization curve of the iron core of an electromagnet. This made it very difficult to obtain consistency between the characteristics of individual relays and to obtain a time–current characteristic which had a simple mathematical equation. In the static relay the time–current relationship is based on an R–C circuit which can be precisely controlled and can be arranged to give any desired relationship between current and operating time.

The desirable form of equation is [3]

$$\text{time } t = [\ A / (m^n - 1)\ ] + B$$

where A and B are adjustable constants and m is the multiple of pick–up current. The integer n is 0 for a definite time relay, 1 for an inverse time relay and 2 for an extremely inverse time relay. These three relay characteristics are shown in Fig. 1.5 [3].

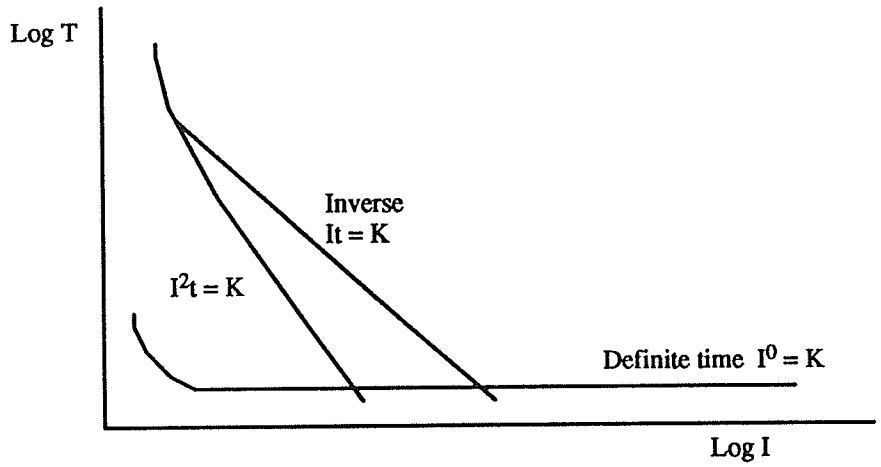


Figure 1.5 Inverse, extremely inverse and definite time–current relay characteristics

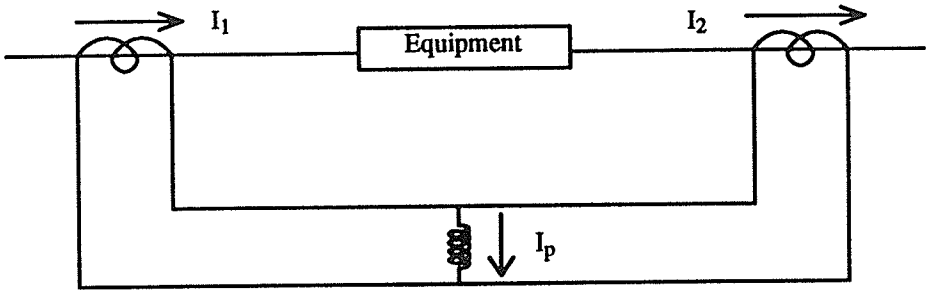
1.2.2 Differential relays:

The basic principle on which a differential relay operates is the circulating current principle. It involves a direct comparison of the magnitude and phase of the currents entering and leaving the protected equipment/section. To accomplish this, current transformers having suitable ratios of transformation are interposed in the circuit at both ends of the protected equipment. These C.T.'s have their secondaries connected as shown in Fig. 1.6 [5].

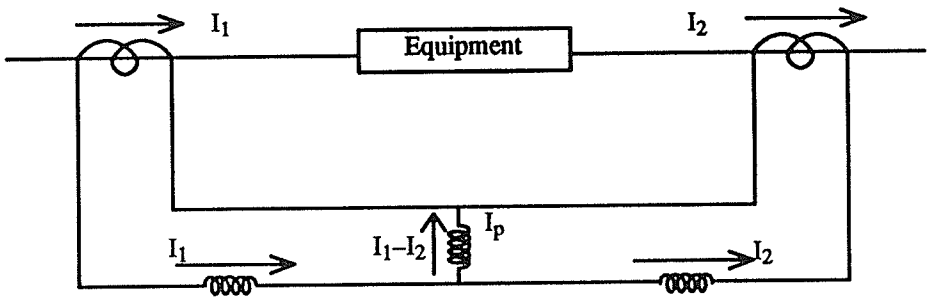
Ideally, with the direction of normal power flow shown, the current through the operating relay (I_1–I_2) should be zero. However, due to various factors such as unequal C.T. saturation, magnetizing inrush current, etc. such an ideal condition may not be obtainable specially in the case of transformer protection. Thus a differential relay is characterized by its ability to distinguish between internal faults requiring isolation of the faulty section and an external fault (or normal condition of power flow) requiring non–operation of the relay.

1.2.3 Distance relays:

Distance relays compare the local current with the local voltage. Since V/I=Z the relay is known as an impedance relay and, since the impedance of the line is proportional to its length, it is called a distance relay.



(a) Merz Price



(b) Percent differential

Figure 1.6 Differential relays

Fig. 1.7 [3] shows how a relay, set for impedance Z_L, will trip if the fault is within that setting because $V<IZ_L$, whereas faults beyond that setting will not cause tripping because $V>IZ_L$. Since this relay ignores the phase angle between A and I, the characteristic is the circle in Fig. 1.8 [3]. It will be seen that the effect of fault resistance is to shorten the reach of the relay.

Here again there are refinements. Instead of comparing I with V it is sometimes necessary to compare I with a component of V, or a component of I with V. For example, one type of distance relay operates when $I > V\sin\varnothing$, where $\varnothing$ is the angle between V and I. The ratio $(V\sin\varnothing)/I=X$, so that the relay measures the reactance of the line instead of its impedance and hence its distance measurement is not affected by fault resistance. Such a relay is used for very short lines and for ground faults where the resistance of the fault path through the earth may be appreciable.

On the other hand, comparing V with a component of I makes the relay more suitable for longer lines where the impedance of the line is close to that of a heavy load (shown in

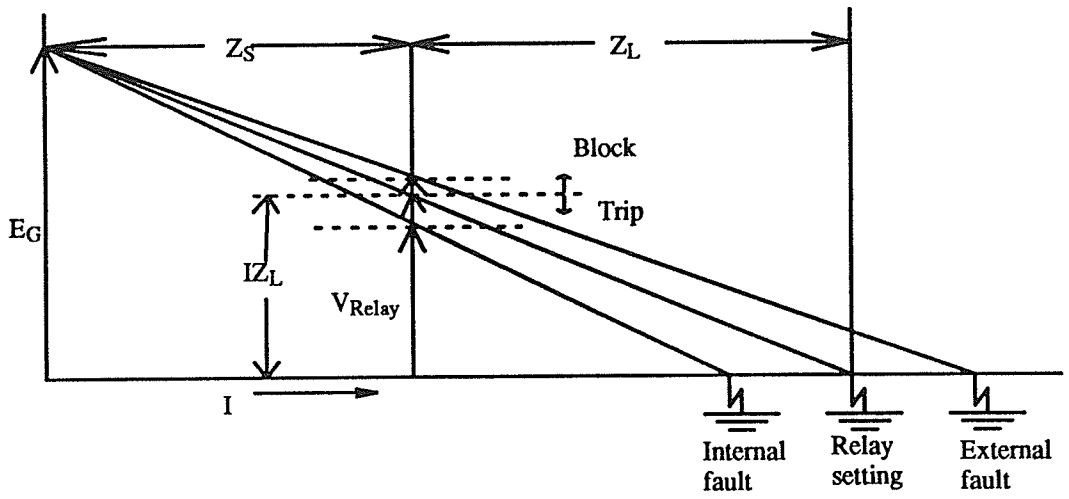


Figure 1.7 Operating principle of distance relay

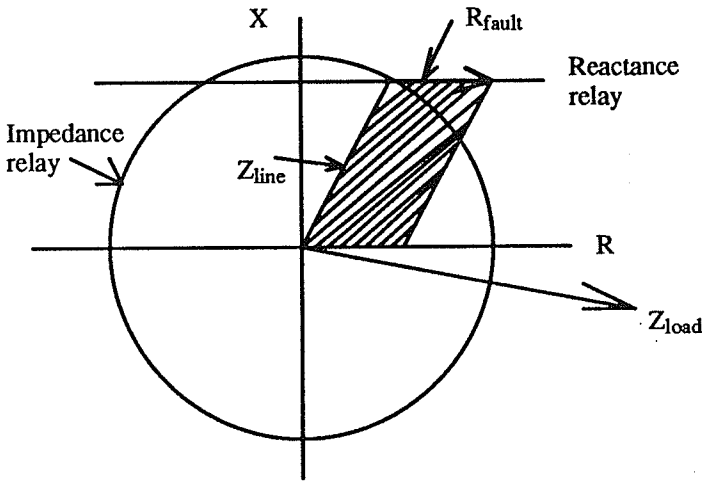


Figure 1.8 Impedance and reactance characteristics

Fig. 1.9) [3] or a power swing, except for the phase angle. In this instance the relay measures the ratio V/[Icos(∅–θ)] or Zsec(∅–θ), where θ is the value of ∅ for maximum sensitivity and hence it is the angle of the impedance circle relative to the R axis. This is called a mho relay (shown in Fig. 1.10) [3] because it operates on a constant value of admittance, viz. Ycos(∅–θ), which is the angle–admittance Y∠θ. It will be noticed that the mho circle fits snugly round the fault area and hence is very selective between internal faults and any other conditions.

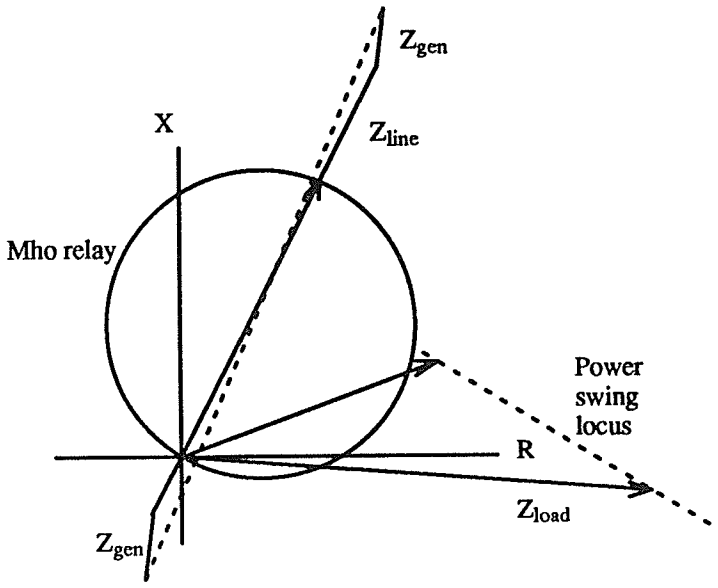


Figure 1.9 Effect of power swing on mho relay

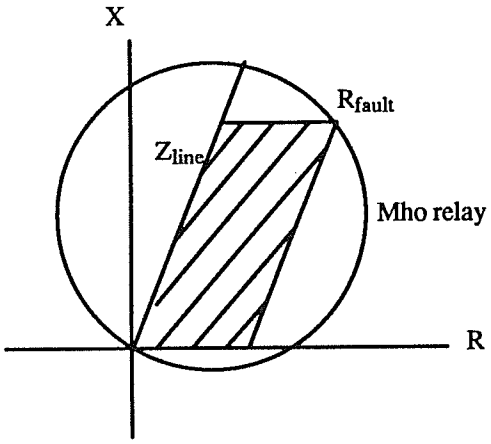


Figure 1.10 Mho relay characteristic snugly fits fault area

The conventional distance relaying uses three distance measuring units (physically separate units or one unit for first and second zones with a timing unit to increase the reach of the former and a second unit for the third zone). The first zone unit which is set to cover usually between 80 and 90% of the first section, is an instantaneous high speed relay while the second zone unit which is set to cover about 25% of the second section and the third zone unit which is set to cover up to the end of the second section are time–delayed relays. Fig. 1.11 shows the respective line sections protected by the three separate zone units. The time delays T2 and T3 for the second and third zones, respectively, are provided by a separate tim-

er relay. Setting in the first zone for less than 100% of the length is made to avoid overreach of the relay into the adjacent section. The overreach would occur because of the following:

(i) Transient overreach of the relay

(ii) Errors in the relay

(iii) Errors in the C.T'.s and V.T'.s

(iv) Errors in the data on which the impedance settings are made.

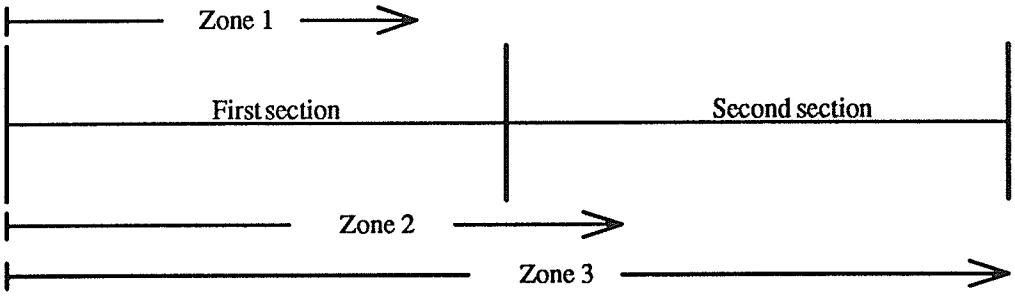


Figure 1.11 Three zone protection

The main object of the second zone unit is to provide protection to the end zone of the first section and also to give remote back–up to the next section up to about 25% of its length. It should be adjusted such that it will be able to operate even for arcing faults at the end of the first section. Also the tendency to underreach by the relay due to the effect of intermediate current sources and the other errors as mentioned above, should be taken into account.

The third zone unit provides back–up protection (remote) for faults in the adjoining line sections. As far as possible its reach should extend beyond the end of the largest adjoining line section under conditions that cause the maximum amount of underreach, namely arcs and intermediate current sources.

The prime purpose of zone one and two protection is to preserve stability, and the zone–three unit protects the apparatus. In many cases, where the consecutive line sections

differ very much in length, alterations in the above scheme, in the number of steps or time delays, may be necessary to give optimum selectivity and protection.

1.2.4 Directional relays:

Directional relays are used to obtain directional sensitivity to relays of the types like overcurrent, impedance distance, etc. They are not used by themselves for protection, but can only augment the performance of other relays as above.

The main problem of directional units is to preserve their discrimination at a very low voltage such as would occur with a fault close to the bus. In static directional relays, the problem is less serious because static comparators are inherently very sensitive and can be designed to be reliable down to 1% of the system voltage, which is well below the minimum fault voltage [5].

For phase faults the directional relay usually compares the phase relation of the current in one phase with the voltage between the two other phases because they will be less affected by a fault involving the first phase; this is called the quadrature connection.

For ground faults the residual current ($3I_0$) of the c.t's is compared in phase angle with the residual voltage ($3V_0$) because it is known that V is a maximum at the fault and the current flows from the fault to the nearest grounded neutral. Alternatively, the residual current may be compared with the neutral current of a grounding transformer.

1.2.5 Pilot relaying scheme:

Pilot relaying schemes employ a communication channel of one type or another in conjunction with protective relays to ascertain in the minimum time possible whether a fault is within the protected section or external to it. High speed determinations of the fault location permits simultaneous high speed tripping of all terminals feeding the faulted line. This minimizes damage at the point of fault and usually permits successful high speed automatic reclosing of the tripped circuit breakers to restore the line to service within a period of about one third of a second from the inception of a fault. High speed auto reclosing with high speed

fault clearing improves the overall stability of the system and, in addition, permits economies in system design that would not be possible otherwise.

There are several basic types in general use for protective relaying. Although they are completely different from one another, their functions are similar, i.e. they either provide a relaying signal or they do not – this fact is utilized in determining the location of the fault. If the presence of a pilot signal blocks tripping, it is called pilot blocking scheme. If the presence of a pilot signal is required in order to trip, it is called pilot permissive scheme.

1.2.6 Block average phase comparator:

With two inputs, it is possible to obtain a wide range of relaying characteristics using different operating principles. The function is generally defined by the relationship between the inputs, which governs the boundary condition of operation. The two basic forms are as follows:

(i)Amplitude comparison—One input is a restraining quantity and the other is an operating quantity so that an output is obtained when the ratio of these quantities is less than a critical value. Ideally the comparison of the amplitudes of the two inputs is independent of the level and phase relationship, of the inputs. The function is represented by a circle in the complex plane with its centre at the origin—defining the boundary of marginal operation. Examples of this are biased relays and impedance type distance relays.

(ii)Phase comparison—Output appears when the inputs have a phase relationship lying with specified limits. Both inputs must exist for an output to occur—ideally the output is independent of their magnitudes, but dependent only on their phase relationship. The function as defined by the boundary of marginal operation is represented by two straight lines from the origin of the complex plane. Examples of

these are directional relays, distance relays excluding the impedance type and other phase comparison relays.

In this thesis, a commonly used phase comparator namely the block average phase comparator is used. In such a comparator V_1 amd V_2, the input voltages to the comparator, are designed from the system voltage (V_L) and current (I_L). The comparator produces output pulses which are positive when V_1 and V_2 have the same polarity and negative when they are of opposite polarities. These are applied to an integrating circuit whose output increases linearly during the time when the pulse is positive and falls at the same rate when the pulse reverses as shown in Fig. 1.12. The level detector operates on the basis of the increase of the integrator output beyond a pre–set value. In this figure V_S is the setting of the level detector which will be reached in time T/2 under continuous energization where T is the period for one cycle. On the other hand, by using different up and down count rates, different protection characteristics other than a circle can be achieved.

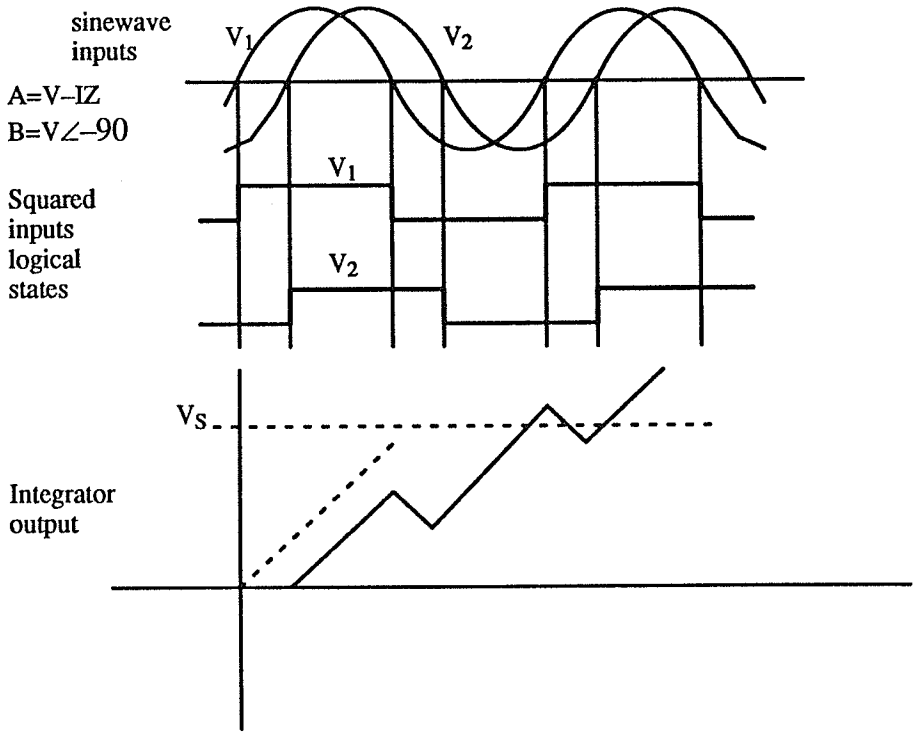


Figure 1.12 Input waveforms and integrator outputs for block average phase comparator

1.3 Background:

Transmission line protection plays a vital role in power system protection. Since a transmission line is built to connect the power plant and the substations through a long distance, the possibility of getting a fault caused by nature is obviously high. Over the decades, impedance relays such as the Mho relay have been widely used over Extra High Voltage(EHV) transmission line systems. It basically responds to the impedance between the relay location and the fault position. The Mho relay is inherently directional, and can provide a versatile protection system for high–voltage transmission line systems with a three–zone distance relaying scheme.

The Manitoba Hydro Dorsey–Forbes–Chisago 500kV transmission line system consists of two major transmission line sections which serve Manitoba Hydro, Northern States Power (NSP), and Minnesota Power. The southern section of the system is 220km long which connect NSP's Chisago County Substation to Minnesota Power's Forbes Substation. The northern section of the system is a 528km long line which connects Manitoba Hydro's Dorsey HVDC Converter Station to the Forbes Substation, and it was the longest single–phase switched section of transmission line in the world at one time [6].

Due to the growing economic and environmental pressures from different sources, it is difficult to construct new transmission and substation facilities to meet the increasing need. As a result, methods have to be looked for to maximize the utility out of existing transmission line systems. In recent decades, series compensation, using capacitors to compensate the inductive reactance of a long transmission line, has been widely used for upgrading existing power line systems. Besides increasing the power transfer capability of the existing transmission line system, series compensation can also maximize the usage of a transmission system by optimizing the sharing of active power between alternative paths connecting the busbars. Since the reactive power generation in a series capacitor increases as the transmitted

power increase, series compensation can improve voltage control and reactive power balance in a transmission line system.

1.4 Problem:

Although series compensation is very effective in raising the transient stability limit and optimizing the sharing of active power between parallel lines of a transmission system, it also gives rise to some problems on power system protection. A simple single–line diagram of the Dorsey–Forbes–Chisago line with series compensation is shown in Fig. 1.13. The series capacitors used in such a case are protected from overvoltage under heavy fault conditions by the inclusion of an MOV (Metal Oxide Varistor). A detailed description on the MOV and the transmission line system will be provided in Chapter 2 and 3 respectively.

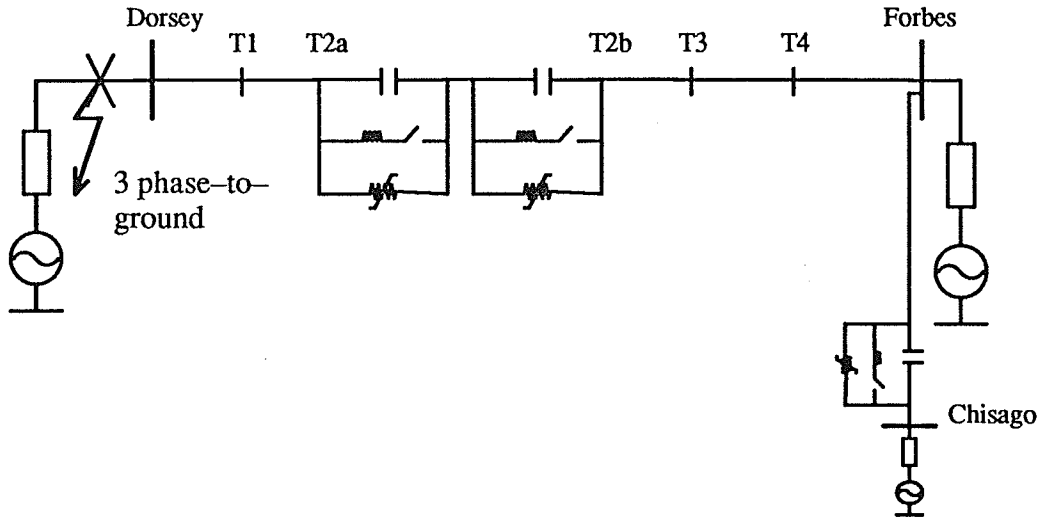


Figure 1.13 Single line diagram of the planned series–compensated Dorsey–Forbes–Chisago line

For the relay at the Dorsey busbar, the measured impedance for a three–phase–ground fault at T3 is smaller than that for a similar fault occurring at T2a for at least 4 cycles after fault. This is because the capacitor compensates a certain amount of inductive reactance of the line, so the relay at Dorsey measures a smaller impedance than it would if the series–capacitor were not there. After four cycles, the bypass switch closes, and the series–capacitor

is taken out of the system. As a result, the measured impedance for a fault at each point corresponds to the distance between the relay and the fault location.

Furthermore, transmission line systems that already have series compensated capacitors installed have experienced problems such as self–excitation, negative–damping and subsynchronous resonance [1]. These effects are not the main concern in this thesis.

1.5 Scope:

The original transient study was on the Ontario Hydro Lakehead–WaWa line. Due to incomplete information on the transmission line system by Ontario Hydro, all studies on that line had to be suspended. As a result, this thesis only considers problems on the Manitoba Hydro Dorsey–Forbes–Chisago 500kV line.

This thesis studies the feasibility of modifying the existing GE relaying system which mainly consists of a positive sequence directional comparison scheme, a negative sequence directional comparison scheme and a direct tripping scheme. The problem caused by inductive–reactance compensation of the transmission line is the main concern. Studies on the problems such as self–excitation, negative damping and subsynchronous resonance are excluded.

A GEC Micromho protection scheme on the series compensated transmission line system is studied to see the possibility of using it on the future compensated system. Moreover, a study on an adaptive protection scheme using a DFT (Discrete Fourier Transform) is also included.

All transient studies were done using the Manitoba HVDC Centre's EMTDC [2] program at the University of Manitoba.

1.6 Purpose:

The purpose of this thesis is to document the results of an investigation aimed at finding a feasible protection scheme for the proposed series–compensated Manitoba Hydro Dorsey–Forbes–Chisago 500kV transmission line system.

A background on series compensation is introduced in Chapter 2. Also the MOV (Metal Oxide Varistor) is illustrated briefly. Furthermore, protection problems on series compensated systems will be discussed.

Chapter 3 gives some detailed information on the Manitoba Hydro Dorsey–Forbes–Chisago line. In order to validate the simulation, staged fault tests data of the existing non–compensated transmission line system are studied. A comparison between these data and that generated by the EMTDC program is done.

In Chapter 4 and 5, descriptions and performance of the existing GE relay and a newly introduced Micromho scheme relay are shown. Furthermore, a comparison on performance between the two relays on the planned series compensated line is given in Chapter 6.

CHAPTER 2

SERIES COMPENSATION

2.1 Background:

In recent decades, series compensation, using capacitors to compensate the inductive reactance of a long transmission line, has been widely used on power line systems. It has two main advantages on a long transmission line system. By raising the transient stability limit, it can increase the power transfer capability. On the other hand, it can maximize the usage of a transmission line system by optimizing the sharing of active power between parallel paths linking the same busbars.

Series–capacitors are usually placed either at the end or middle of the transmission lines. The degree of compensation ranges from 20 to 70 percent, as referred to the inductive reactance of the transmission line. For EHV systems, series–capacitors are typically in the range 100Mvar to 1000Mvar in size [7]. The technology on series compensation has been improved in recent years. Besides improvement to capacitors, auxiliary equipments such as protective devices and signalling linkage have been developed. The latest technology on protecting series–capacitors involves Metal Oxide Varistors (MOV) which largely improves the reliability and also shortens the time needed for reinsertion of the capacitor into the system after fault clearing. Series compensation also lowers the financial burden of utility company by not having to build a costly additional transmission line.

2.2 Theory:

Series–capacitors can increase the power transfer capability and optimize the sharing of active power between parallel paths. The series–capacitors compensate the line inductance to allow maximum power transmitted in a transmission line system.

Fig. 2.1 gives a simple single line diagram of a section of transmission line with series compensation.

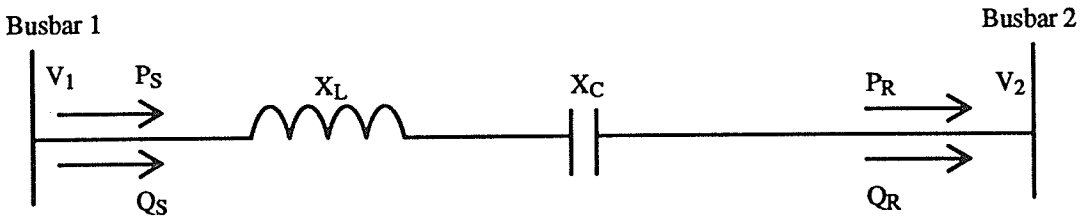


Figure 2.1 Transmission line with series compensation

The active power flowing towards busbar2 (using short line approximation) is [7]

$P_R = (V_1 . V_2 / X_L) . \sin\theta$ .....(2.1) without series compensation,

and

$P_R = [V_1 . V_2 / (X_L - X_C)] . \sin\theta$ .....(2.2) with series compensation,

where θ is the phase difference between the two busbar voltages. It is obvious that the active power delivered can be increased by compensating the inductive reactance of the line. On the other hand, the phase difference between the two busbar voltages can be dropped while keeping the active power delivered fixed. This will increase the transient stability of the transmission line system.

In parallel line systems, the power flow is divided according to the impedances of different sections of the line system. This means the sharing of power flow in the transmission line system is set by the length (impedance) of each line section but not by the economic point of view. When the particular line section with the lowest power transfer capability reaches its limit, the power flow on other unsaturated lines cannot be increased anymore. This leads to a waste of natural resource and money. Series–capacitors can maximize the power transfer capability by rearranging the distribution of line impedances of the whole system. Fig. 2.2 shows a simple single line diagram of a parallel line system with one line being series–compensated.

With line AB_2 being longer then line AB_1, the length difference between line AB_1 and line AB_2 have already determined the power flow situation . If a series–capacitor is in-

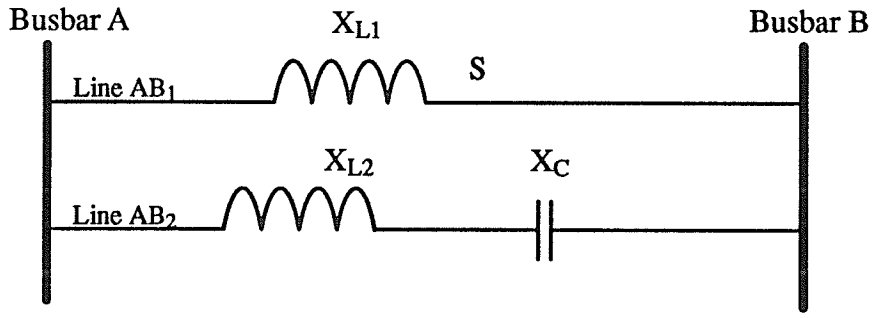


Figure 2.2 Single line diagram of a parallel line system

stalled on line AB_2, the power flow strategy can be set by the economic point of view. Moreover, an appropriate sharing of current between the parallel lines can minimize the system losses.

2.3 Protection schemes for the series–capacitor:

Since series capacitors are installed out on the transmission line, they have to work in harmony with other parts of the system. In order to achieve this task, proper protective devices are needed to make sure the capacitors are bypassed effectively during fault situations that may damage the capacitors. On the other hand, this protective scheme has to reinsert the capacitors into the system quickly after the fault is cleared. Since series compensation was introduced, protective schemes such as single–gap, dual–gap and ZnO schemes have been developed. The single–gap scheme take 0.2–0.4 second to reinsert the capacitors into the system after the fault is cleared. Following up is the dual–gap scheme, which takes only 60 milliseconds approximately [7]. The newest ZnO scheme reinserts the capacitor almost instantaneously after fault clearing.

Fig. 2.3 [7] shows a model of a single–gap scheme device. During a fault, the current into the capacitor will charge up the capacitor. When the voltage reaches a certain level, the spark gap G1 will ignite. This will also close the bypass breaker S1 (which operates a lot slower than the spark gap), and extinguish the spark gap consequently. When the voltage across the capacitor drops to a preset safety level, the bypass breaker will be opened and the capacitor will operate at the prefault voltage level.

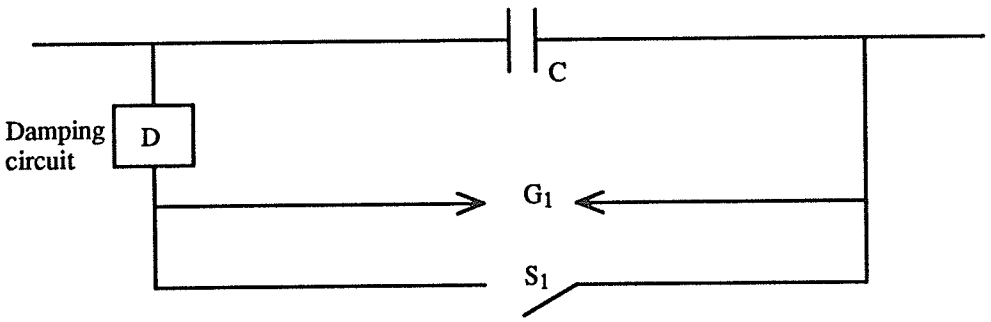


Figure 2.3 Single–gap scheme device

For the single–gap scheme, the spark gap has to cool down before the reinsertion of the capacitor. This may delay the whole process of reinsertion. A double–gap scheme shown in Fig. 2.4 [7] provides an additional lower settings spark gap (G2) which can be cut off by opening a series bypass breaker (S2). The series bypass breaker (S2) is closed during normal operation. When a fault occurs, the voltage across the capacitor will induce an ignition of the lower–setting spark gap (G2), then the bypass breaker (S1) will close before the bypass breaker (S2) opens. After the fault is cleared, the bypass breaker will open, and more importantly, the spark gap (G2) has considerable amount of time to cool down. The higher–setting spark gap (G1) works as a back–up protection unit in the period right after the reinsertion. Since the cooling of spark gap (G2) does not affect the operation, the reinsertion time can be considerably decreased.

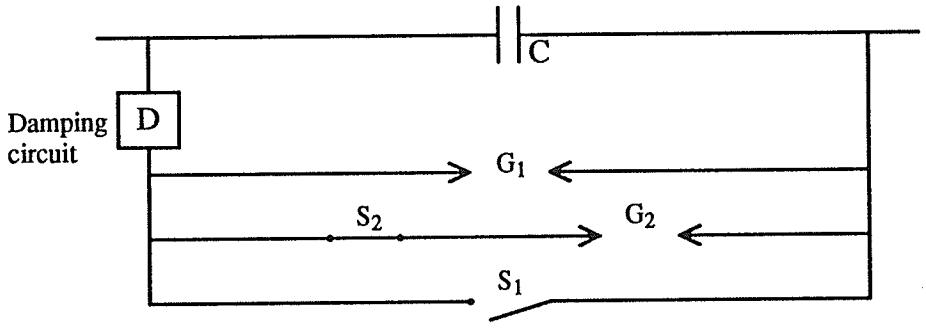


Figure 2.4 Double–gap scheme device

Fig. 2.5 shows a model of a ZnO scheme which is known as the Metal Oxide Varistors (MOV). A typical MOV voltage–ampere characteristic is shown in Fig. 2.6, and it is the es-

sential property behind the MOV scheme. The relation between voltage across the capacitor and the current through the MOV can be explained by Equation 2.3. The MOV does not carry any current during normal operating conditions. During a fault, the MOV is diverting some of the current from the capacitor to lower the voltage across the capacitor and the MOV. As a result, the capacitor will not be damaged by high voltage and is still working as a part of the system. In a heavy fault situation, if the energy absorbed by the MOV exceeds a certain limit, the spark gap will be ignited and all the current will go through the bypass route. This prevents the MOV from being damaged by exceeding its energy capacity. The advantage of the MOV is that the capacitor stays within the system for most kind of fault conditions and the reinsertion time of the capacitor is almost zero.

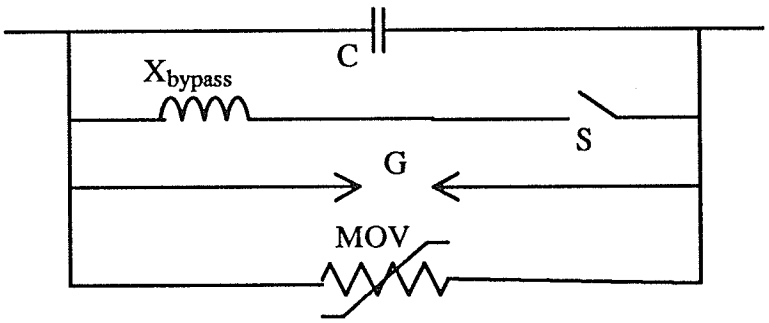


Figure 2.5 ZnO scheme device

$$i = [\, v / V_N \,]^n \qquad \text{.....(2.3)}$$

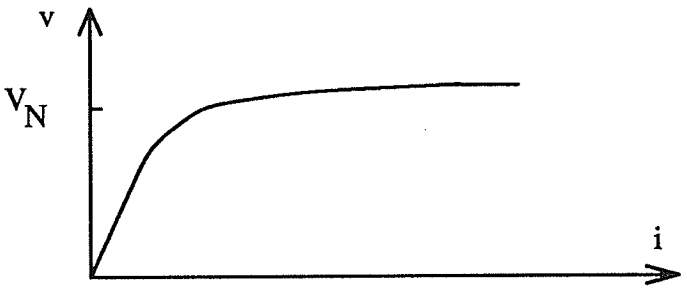


Figure 2.6 Typical MOV voltage–ampere characteristic

2.4 Operating relationship between the MOV, capacitor and transmission line:

The Metal Oxide Varistor protects the capacitor from being damaged by overcharging, and leaves the capacitor as a working component of the system for non–heavy fault situ-

ations. The MOV usually conducts within the first half–cycle after fault. For a heavy fault, the bypass switch usually closes within 4 cycles after fault, depending on the energy capacity of the MOV and the size of the capacitor. If the fault is not severe, the MOV usually stays in operation until the circuit breakers trip at both ends of the faulted line.

The nominal voltage V_N in Equation 2.3 is normally set to be 0.75 times the limiting voltage across the capacitor (and the MOV). The MOV index n is usually in the range of 30 to 50, and it is set at 32 in this thesis. The limiting voltage is normally 2.5 times the rated voltage for the capacitor. Fig. 2.6 shows that normal current flowing through the capacitor yields a very low value of i which is the current through the MOV [8]. Under severe fault conditions, the current through the capacitor increases; and it brings up the voltage across the capacitor. When this voltage exceeds V_N a large increase of current through the MOV results. The current can reach up to several kA and it may increase the energy absorbed by the MOV to a dangerous level. At this moment, the spark gap triggers and the bypass activates to isolate the MOV and the capacitor from the rest of the system.

A power system shown in Fig. 2.7 is set up to study the current and voltage waveforms of the MOV, capacitor and the bypass switch during fault conditions. The triggered gap is not shown separately.

The data selected for the system in Fig2.7 is as follows:

System Voltage = 500 $kV_{rms\ line–line}$

Series Capacitance = 63.9 μF per phase

Energy Limit = 25 MJ for MOV

$V_N = 216.5\ kV_{peak–value}$

Arrestor Characteristic $i = (v / 216.5 \times 10^3)^{32}$

A three phase fault is applied at point A which gives the most severe fault condition. Fig. 2.8 shows the line current at the sending end busbar, the voltage across the capacitor, the capacitor current, the MOV/bypass current and the MOV energy level. The MOV/bypass

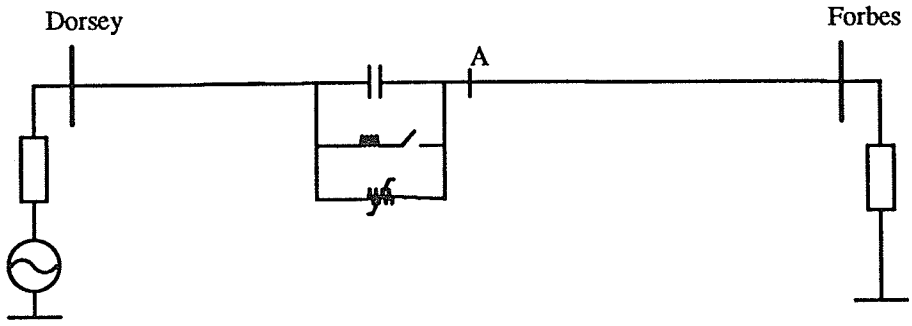


Figure 2.7 A 500 kV transmission line with series compensation

current is the sum of the currents flowing through the MOV and the bypass switch. Before the bypass switch is closed, the MOV/bypass current is basically the MOV current alone, and it becomes the bypass current after the bypass switch has closed.

When the fault occurs, the current flowing through the capacitor (Fig. 2.8c) increases and this increases the voltage across the capacitor (Fig. 2.8b). When the voltage across the capacitor (Fig. 2.8b) reaches V_N (216.5 kV), the MOV will conduct and it induces a sudden rise of current (Fig. 2.8d). At the moment that the MOV starts to conduct, the current through the capacitor (Fig. 2.8c) will drop to a low value. Then the capacitor and the MOV take turns to conduct currents until the bypass switch closes. Notice that the MOV operates only when the instantaneous capacitor voltage (Fig. 2.8b) is above a certain level. When the MOV operates, the energy level shown in Fig. 2.8e increases. It will reach a certain limit and cause the triggered gap and the bypass switch to close. At this particular moment, a spike of current (Fig. 2.8d) goes through the bypass route due to the discharging of the capacitor. After the bypass switch closes, the bypass route will conduct all of the line current (Fig. 2.8a) and the MOV energy (Fig. 2.8e) will stop increasing. As a result, the voltage across the capacitor (Fig. 2.8b) is kept under the limiting voltage, and the MOV is not damaged by exceeding the energy capacity. Under non–extreme fault conditions, the energy level of the MOV does not reach the limit for at least 15 cycles after the fault. In these cases, the faults would have been

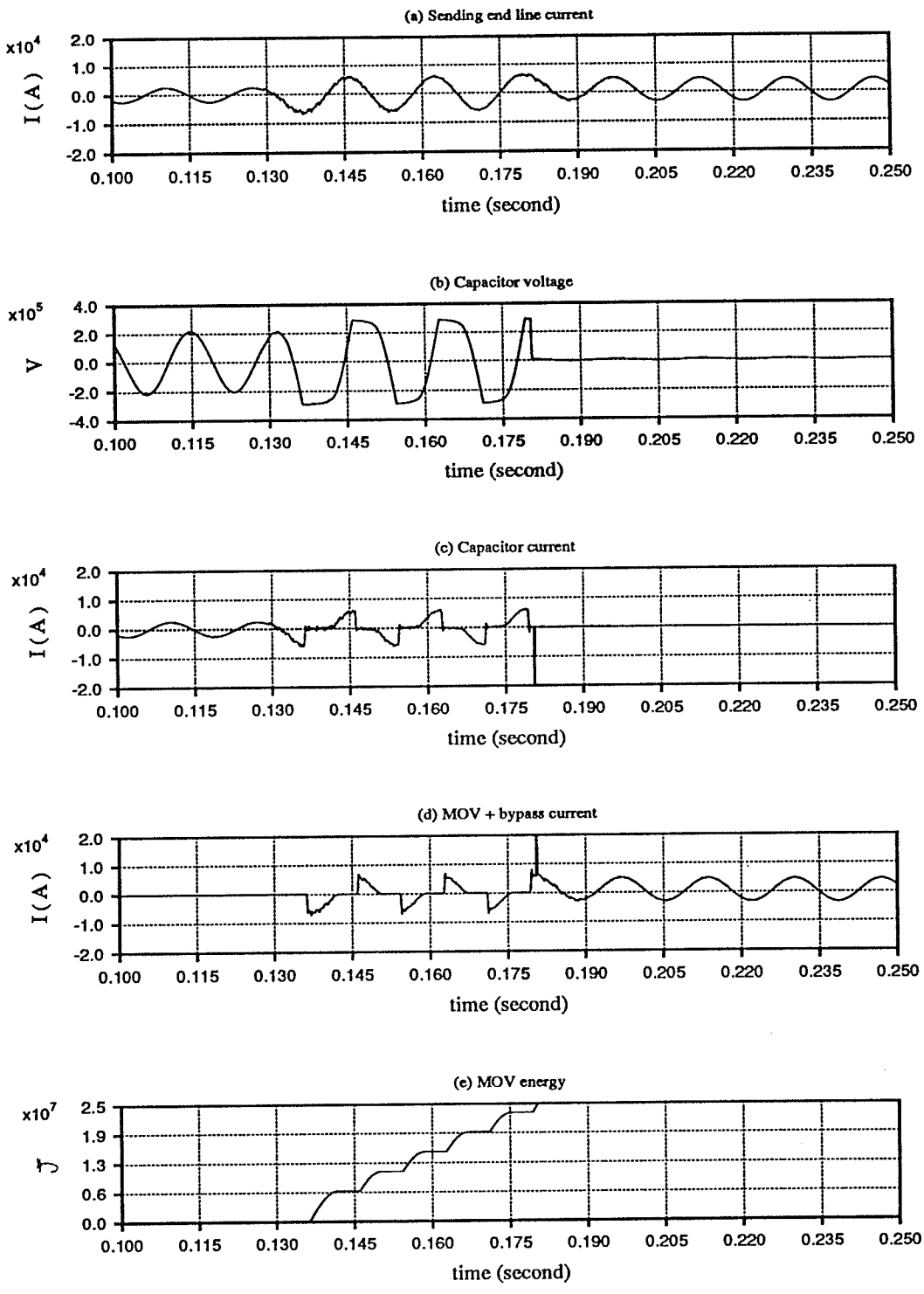


Fig 2.8 Series compensated line waveforms

detected and cleared earlier, and the bypass switch will not close at all during the whole operation.

The Metal Oxide Varistor not only protects the capacitor from being damaged, it also simplifies the protection of a series compensated transmission line. Since the relay on a centre–compensated series compensated line takes information from the source side of the capacitor, the operation of the MOV will affect the measured impedance. The power line system shown in Fig. 2.9 was chosen to illustrate the changes in measured impedance caused by the MOV on a series compensated line. A 1–cycle Fourier algorithm was used to extract the fundamental components of the voltages and currents measured at the relay location which is at the Dorsey busbar.

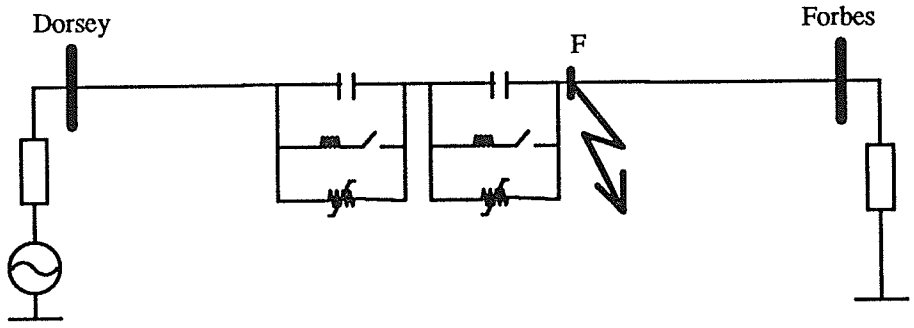


Figure 2.9 System used for MOV studies

Without series compensation, the impedance trajectory of a 3 phase–ground fault at point F seen by the relay at Dorsey is shown in Fig. 2.10(Δ). After the fault, it goes straight into the mho circle. With series compensation but no MOV, the impedance trajectory in Fig. 2.10(×) misses the mho circle since the series–capacitor compensates about half of the line inductance. Unless the mho characteristic is altered, the relay will not detect the fault in this situation. The MOV raises the reactive component of the measured impedance and the impedance trajectory in Fig. 2.10(∇) will cut the mho circle. Notice that when the bypass switch closes, the impedance trajectory suddenly climbs up to the corresponding un–compensated line impedance.As a result , the MOV makes it possible to use the original mho characteristic to protect this series–compensated line.

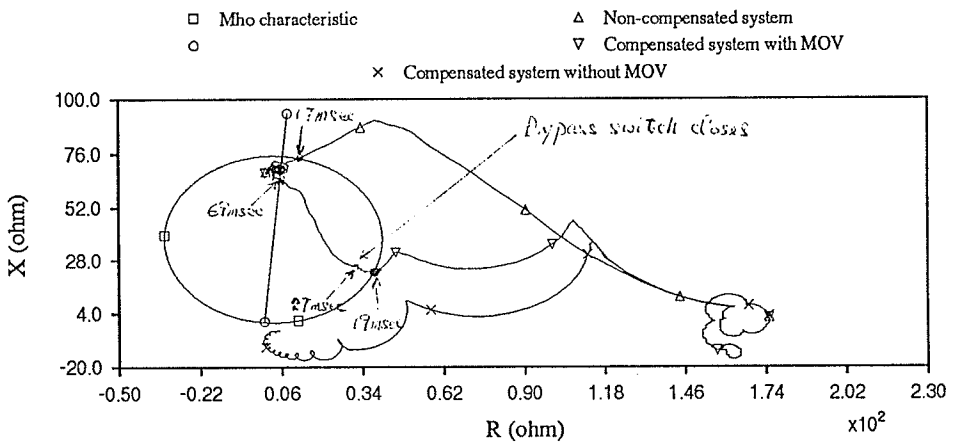


Figure 2.10 Impedance Trajectories

2.5 Protection problems on the series-compensated transmission line:

Since series compensation was introduced, various protection problems on series compensated transmission lines have arisen. These include self-excitation, negative-damping, subsynchronous resonance, capacitor overvoltage, voltage inversion and current inversion [1]. Among all of these problems, voltage inversion has been recognized by protection engineers as one of the major problems for distance protection. It is the result of inductive current flowing through a capacitive impedance. From a relaying point of view, the maximum magnitude of voltage inversion is expected to occur at a measuring location directly adjacent to a capacitor installation. This is why more complex relaying is required for an end compensated line than a mid compensated line.

The term 'voltage inversion' was derived by neglecting the smallest line parameter, the circuit resistance. This leads to only two types of impedance, inductive and capacitive reactance. The overall impedance, being the sum of a positive and negative reactance, then can only be one of the two types, depending upon which has the larger magnitude. The resultant voltage lies along the line of the EMF, and is therefore either in-phase or in anti-phase with it. The latter possibility led to the term 'voltage inversion' [9].

2.5.1 End–compensated line:

For an end compensated transmission line such as shown in Fig. 2.11, the choice of the location of voltage and current signals taken for impedance measurement has to be seriously considered. The measurement can be done either on the source side or the line side of the series capacitor.

For the case where the measurement is taken from the source end of the capacitor, the measured impedance is capacitive if X_F is less than X_C and inductive if X_F is greater than X_C. If F is the point where $X_F=X_C$ then for a fault to the left of point F (net reactance is negative), the relay sees the fault in a reverse direction.

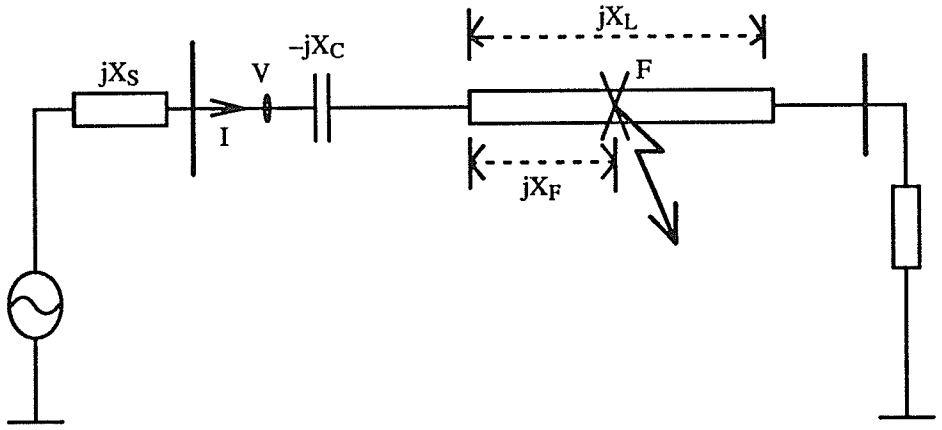


Figure 2.11 Series compensated line with meaurement on source side

For the case where the measurement is taken from the line side of the series capacitor, the impedance measurement for a forward fault on the line does not cause a problem. But for a reverse fault just beyond the busbar which is shown in Fig. 2.12, the impedance measured by the relay is inductive. This means that the reverse fault will appear as in a forward direction to the relay.

Although the capacitor will be bypassed for a fault directly adjacent to itself, it may take more than four cycles for the bypass switch to close. This is too late since the relay has already tripped for the reverse fault.

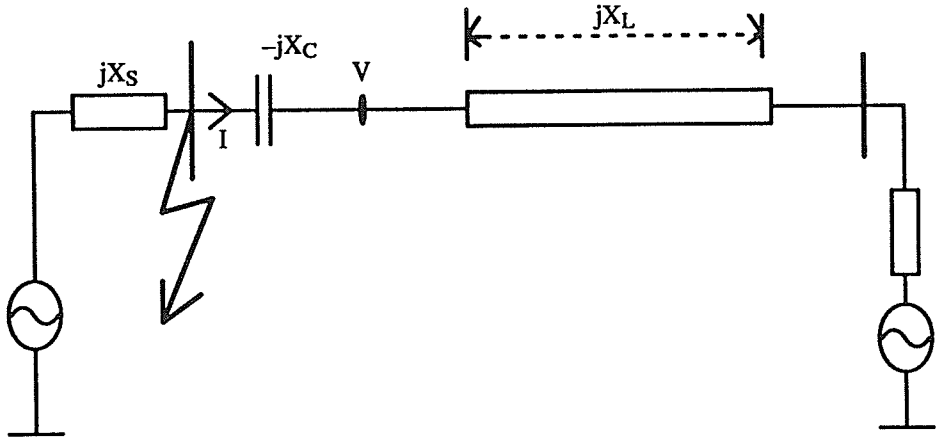


Figure 2.12 Series compensated line with measurement on line side

2.5.2 Mid–compensated line:

For a mid compensated transmission line as shown in Fig 2.13, there is no choice for the location of impedance measurement but at the busbar. An inductive impedance will only be measured for a fault at point F where $X_F+X_{L1} > X_C$, otherwise the relay will see it as a reverse fault. So, it is important to make sure $X_{L1} > X_C$ and $X_{L2} > X_C$ ($X_C \leq (X_{L1}+X_{L2})/2$) if a complex protection scheme is not available.

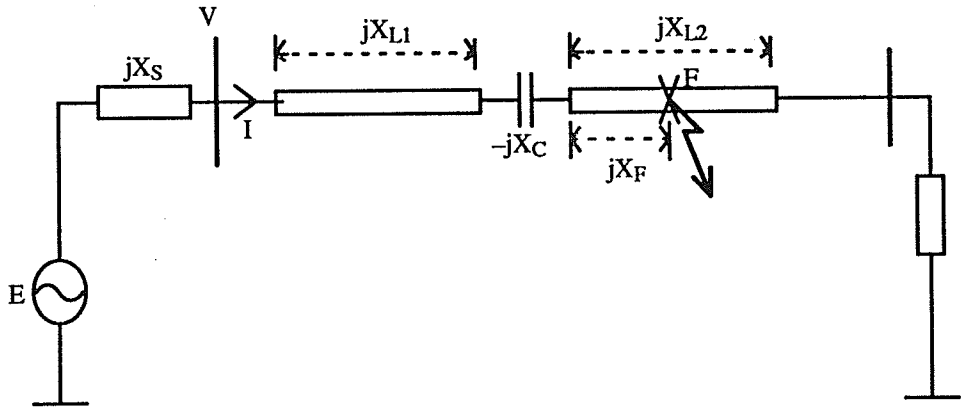


Figure 2.13 Mid compensated line with fault location

2.5.3 Effect of the MOV:

For a fault directly adjacent to the capacitor, since the bypass switch will not usually close until approximately four cycles after fault, the effect of the series capacitor still exists

for the end compensated line. For the mid compensated line with condition $X_{L1} \geq X_{L2} > X_C$, the relay at the end of the longer line section may not be able to protect all the line section between the capacitor and itself. Especially for the case when X_{L2} approximately equals X_C, an impedance reach setting for the relay that covers up to the capacitor will also trip for a fault beyond the remote end busbar. So careful relay setting planning has to be done.

CHAPTER 3

INFORMATION ON DORSEY–FORBES–CHISAGO LINE

3.1 Background:

The two parts of the Dorsey–Forbes–Chisago 500kV transmission line system were placed in commercial operation in September, 1979 and May, 1980. It was jointly constructed by Manitoba Hydro, Northern States Power, and Minnesota Power. The transmission line system connects the three companies. The southern section of the system is 220km long and connects Northern States Power's Chisago County Substation to Minnesota Power's Forbes Substation. The northern section of the system is 528km long and connects Manitoba Hydro's Dorsey HVDC Converter Station to the Forbes Substation. This was the longest single–phase switched section of 500kV transmission line in the world at one time [6]. During the summer, the excess generation in Manitoba can compensate the summer peak situation for Northern States Power. In the winter, Northern States Power does the opposite, since the lakes are frozen in Manitoba.

Three–phase shunt reactors with sizes 225MVARs, 300MVARs, and 150MVARs are installed respectively in the Dorsey, Forbes, and Chisago substations. These shunt reactors provide both lines with a total of 73% shunt compensation. On the other hand, neutral reactors with sizes 425 ohms, 325 ohms, and 1250 ohms are located respectively in Dorsey, Forbes, and Chisago. These neutral reactors limit the secondary arc currents under ground fault conditions. The Dorsey–Forbes–Chisago line is transposed along the route in order to yield more equal phase–to–phase capacitive coupling [6].

3.2 Comparison between the EMTDC simulated data and staged fault test results:

A model of the Dorsey–Forbes–Chisago 500kV transmission line system is simulated by using the EMTDC program. In order to ensure its accuracy, an official staged–fault–tests document prepared by Manitoba Hydro is used. The staged fault tests on the 500kV line

were done in 1980, and line–to–ground fault tests were done on the 528km Dorsey–Forbes 500kV line. Different fault locations and line loading conditions were used in nine different fault tests, and the measurements include primary and secondary arc currents and the arc recovery voltage. In this thesis, two selected fault test conditions are simulated with the EMTDC program. A comparison between the simulated fault data and the staged fault test result is done. Fig. 3.1 shows the locations of the two selected fault tests on the one–line diagram of the system [6].

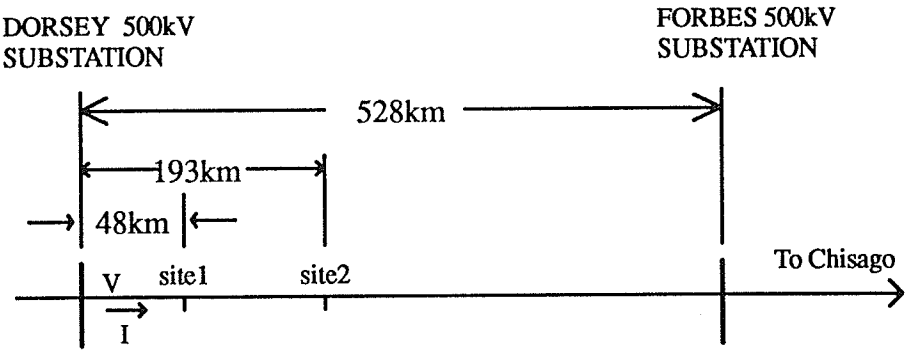


Figure 3.1 Fault test sites & one line diagram

The first fault test condition and test results are summarized as follows [6]:

Test Site : Site1

Load Flow : 320 MW

Prefault L–G voltage $_{(kV-rms)}$: 300

Fault Phase : C

Voltage Angle Degrees : 255° (at instant of fault initiation)

Primary Fault Current : 7640 A (peak of first cycle including D.C. offset, hardwired recording system)

The line currents at Dorsey for this particular fault test are shown in Fig. 3.2. A similar fault condition is simulated by using the EMTDC program, and the results are shown in Fig. 3.3. Table 3.1 compares the two faulted line currents.

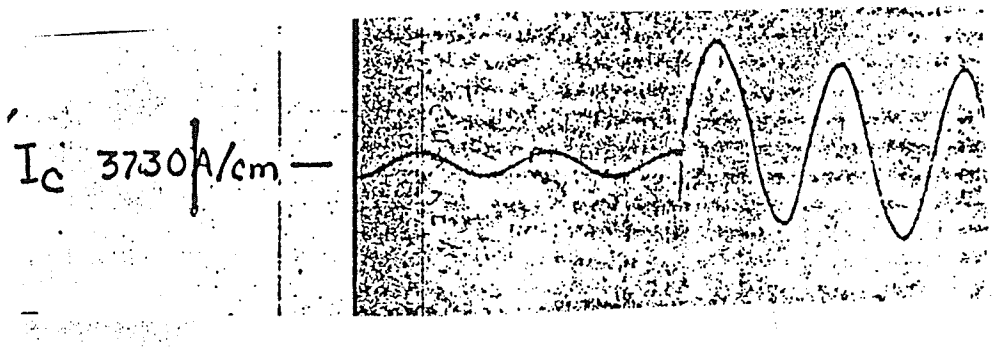


Figure 3.2 Line current measured at Dorsey in fault test #1

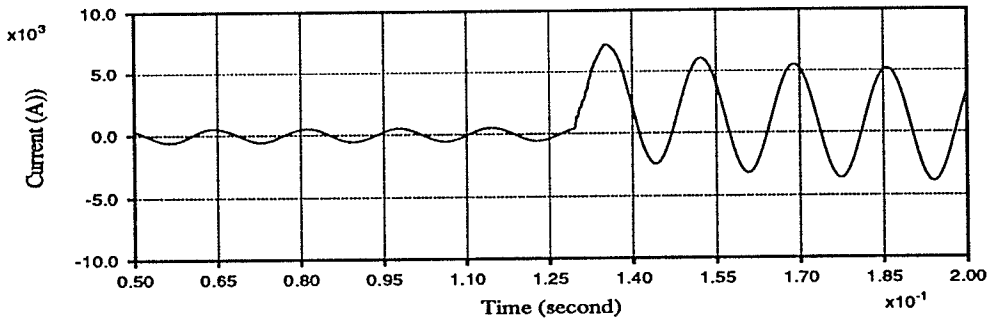


Figure 3.3 Line current measured at Dorsey in setup model using EMTDC

Table 3.1 Comparison on waveforms between the staged fault test and EMTDC model

	Stage fault test	EMTDC model
Prefault line current (A_{peak})	560 ± 5%	540 (3.6% difference)
Peak–peak of fault current (A)	8200 ± 5%	8800 (7.3% difference)

In this case, the prefault line current generated by EMTDC program agrees with the staged–fault–test result to a large degree. There is a difference of 600 A (7.3 % difference) in the peak–to–peak value of the fault current between the two current waveforms. Since the

voltage waveforms on the stage fault test were not provided, only currents are compared. However, in the next fault test, voltage and current waveforms will be shown.

The second fault test condition and results are summarized as follows [6]:

Test Site : Site2

Load Flow : 510 MW

Prefault L–G voltage $_{(kV-rms)}$: 296

Fault Phase : A

Voltage Angle Degrees : 84° (at instant of fault initiation)

Primary Fault Current : 3770 A (peak of first cycle including D.C. offset, hardwired recording system)

The line currents and voltages at Dorsey for this particular fault test are shown in Fig. 3.4. Again, a similar fault condition is simulated by using the EMTDC program, and the results are shown in Fig. 3.5. Table 3.2 compares the two voltages and line currents.

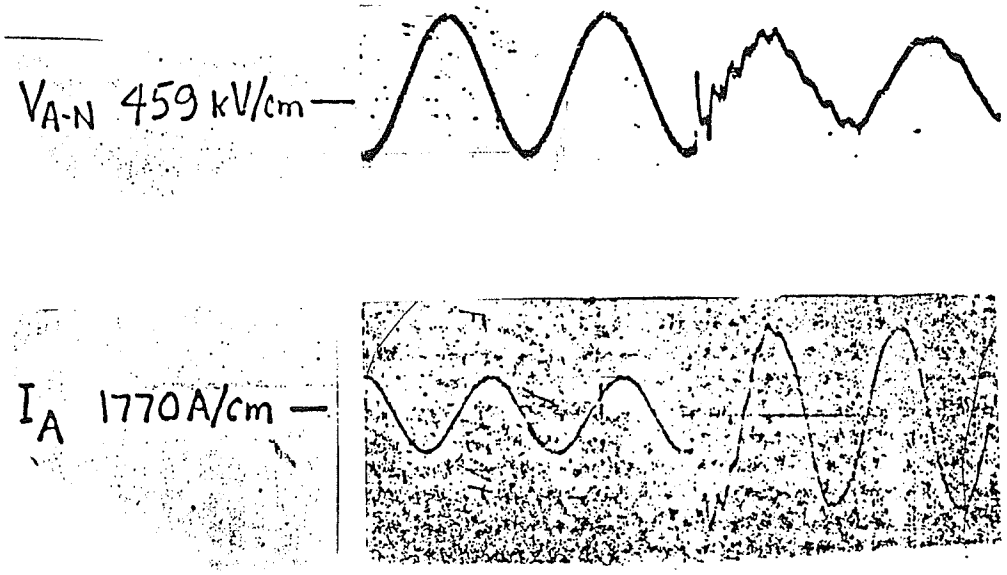


Fig 3.4 Waveforms measured at Dorsey in staged fault test #2

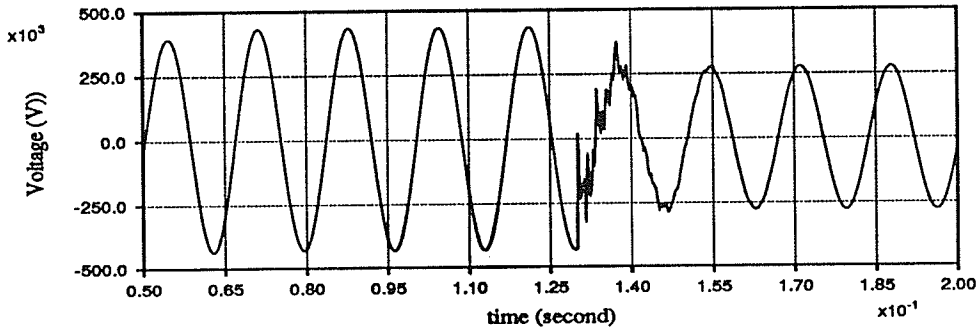


Figure 3.5a

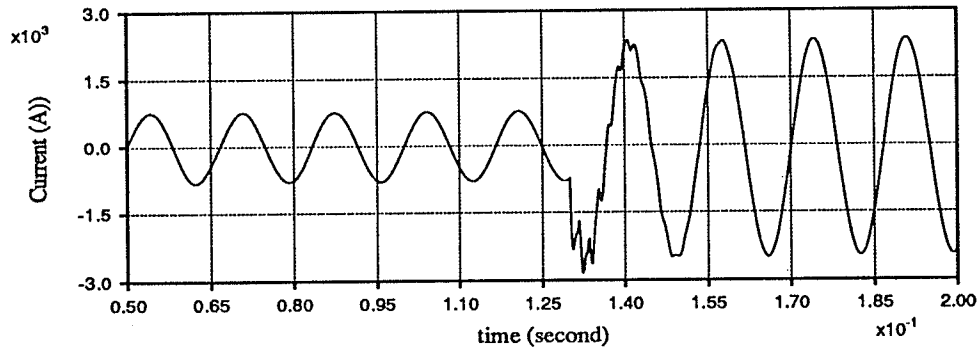


Figure 3.5b

Figure 3.5 Waveforms measured at Dorsey in set–up line model

Table 3.2 Comparison on waveforms between the staged fault test and EMTDC model

	Stage fault test	EMTDC model
Prefault line current (A_{peak})	860 ± 5%	800 (7.5% difference)
Peak–peak of fault current (A)	4400 ± 5%	4800 (9.1% difference)

Prefault voltage (V_{peak})	410 ± 5%	430 (4.9% difference)
Peak–peak of fault voltage (V)	520 ± 5%	550 (5.8% difference)

In this case, the two sets of results show a large degree of agreement except for the peak–to–peak value of the fault current which shows a 9.1% difference. As a result, it gives assurance for using the present model to do further studies.

3.3 Location of the series–capacitors:

Since the idea of installing series capacitors on the Dorsey–Forbes–Chisago line arose, the sizes and the locations of the capacitors have been rigorously considered. Series capacitors installed on the power system can be located at one end or the middle of the line, and both installations have advantages and disadvantages. As a result, three 63.92μF capacitors with individual MOV and bypass switches will be installed on the Dorsey–Forbes–Chisago 500kV line, which is shown in Fig. 3.6. Two of the capacitor banks will be put in series at 225km from Dorsey on the Dorsey–Forbes line section. The other capacitor bank will be put at the Chisago substation on the Forbes–Chisago line. All three capacitor banks have identical parameters such as capacitor size, MOV energy dissipation limit, and nominal voltage of MOV. Characteristics of one of the capacitor banks are listed as below:

System Voltage = $500kV_{rms}$

Series Capacitance = 63.9 μF per phase (41.5ohm at 60 Hz)

Energy Limit = 12.5 MJ for MOV

Arrestor characteristic $i = (v/(108.25x10^3))^{32}$

The planned Dorsey source–impedance short–circuit level is 1860 MVA, and 1500 MW of real power will be delivered from the Dorsey substation. Also, synchronous condensors will be installed in Dorsey, and shunt capacitors will be installed in the Forbes substation. Furthermore, there will be two transformers instead of one in all three substations, and tertiary capacitors will be installed in the Dorsey and Chisago substations.

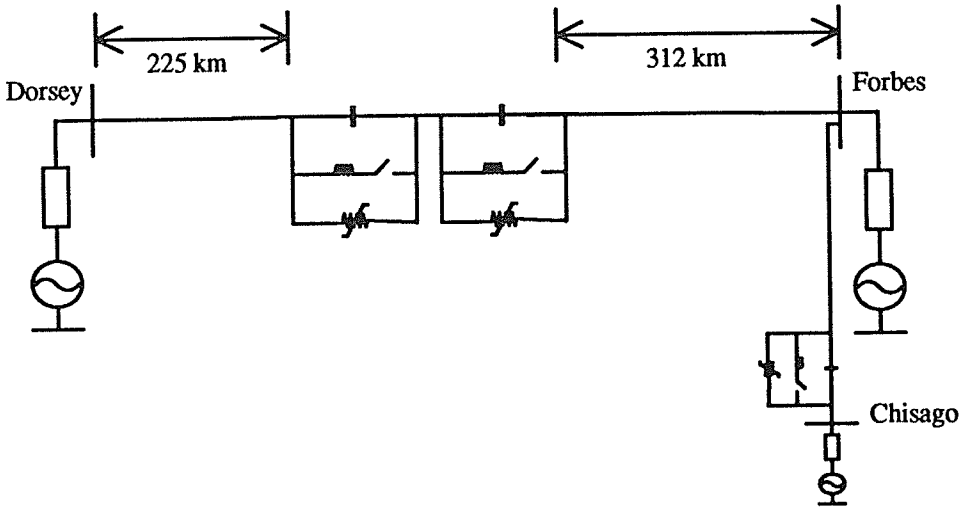


Figure 3.6 Planned series–compensated transmission line system

CHAPTER 4

GE RELAY ON DORSEY–FORBES–CHISAGO LINE

4.1 Mechanism of the GE relay:

The GE relay [12] described in this thesis consists of three major parts: a positive sequence directional comparison scheme, a negative sequence directional comparison scheme and a direct tripping scheme. The positive sequence directional comparison scheme measures distance on three phase faults, and will underreach on unbalanced faults. The negative sequence directional comparison scheme includes forward and reverse blocking negative sequence directional functions designed to respond to all types of unbalanced faults. The direct tripping scheme provides supplemental protection for faster operation on heavy internal faults or to cover special operating conditions. The actual GE relay has other features such as weak infeed and phase selection for single–pole tripping but they are not covered in this thesis.

In this thesis, the positive sequence, negative sequence and zero sequence quantities are extracted from the three phase–voltages and currents using the DFT (Discrete Fourier Transform). Firstly, the phasors V_A, V_B, V_C, I_A, I_B and I_C are produced from the DFT. Then V_0, V_1 and V_2 are produced by

$$V_0 = (V_a + V_b + V_c) / 3$$

$$V_1 = (V_a + a\, V_b + a^2\, V_c) / 3$$

$$V_2 = (V_a + a^2\, V_b + a\, V_c) / 3$$

where $a = 1 \angle 120$

and I_0, I_1 and I_2 are produced by

$$I_0 = (I_a + I_b + I_c) / 3$$

$$I_1 = (I_a + a\, I_b + a^2\, I_c) / 3$$

$$I_2 = (I_a + a^2\, I_b + a\, I_c) / 3$$

The DFT provides a filtering effect that is different from that provided by the actual GE relay. This will lead to a difference on the tripping time between the real and simulated relays. Fig 4.1 shows the input phase voltage and the corresponding positive sequence voltage waveforms of the DFT for a three–phase–ground fault.

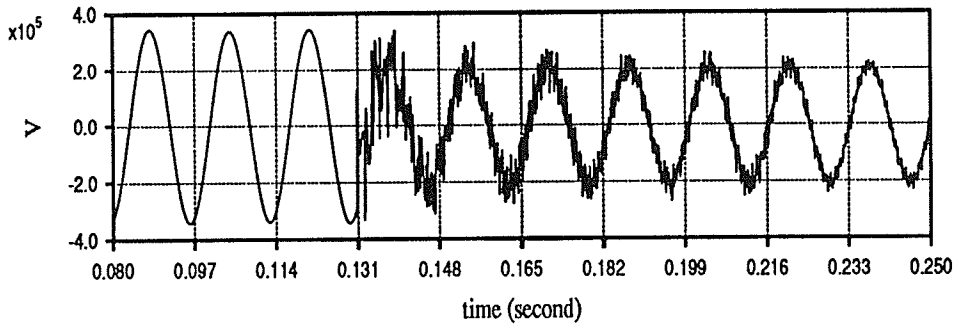


Fig 4.1 a Waveform before the DFT

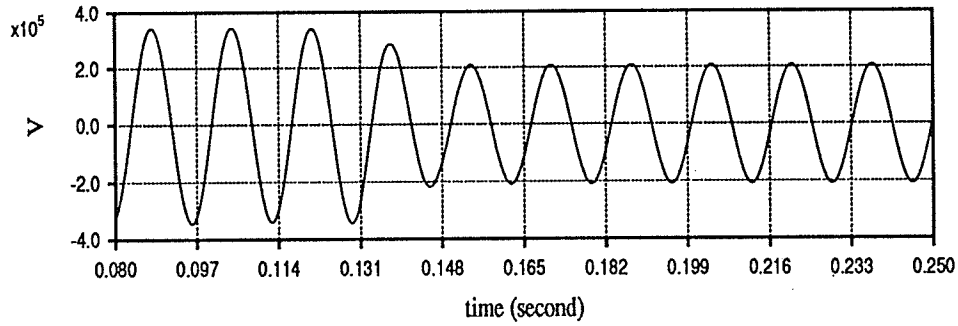


Fig 4.1 b Waveform after the DFT

4.1.1 Positive sequence directional comparison scheme:

The positive sequence directional comparison scheme utilizes positive sequence current and voltage quantities to detect three–phase faults on transmission line systems either with or without series capacitors. Fig. 4.2a illustrates the principle used to derive the mho characteristics.

The I_1Z quantity is a voltage proportional to the positive sequence current in the line, and is obtained from the positive sequence current filter. The V_1 quantity is proportional to positive sequence voltage at the relay location and is obtained from the positive sequence voltage network. The quantity $(I_1Z–V_1)$ is the phasor difference between these two quantities. I_1Z' is the reverse reach of the relay. The phase difference between $(I_1Z–V_1)$ and $(I_1Z'+V_1)$ is less than 90 degrees for an impedance point internal to the relay characteristic,

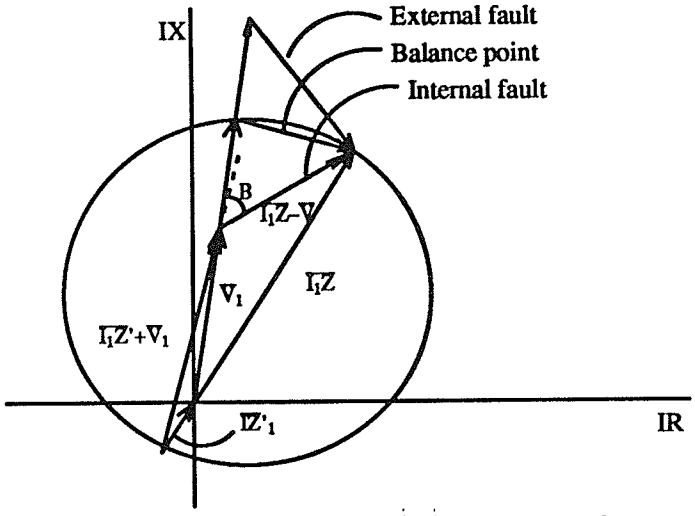


Figure 4.2a Offset mho characteristic by phase angle measurement

equal to 90 degrees at the balance point, and greater than 90 degrees for an external impedance point for which the relay should not operate.

The instantaneous quantities V_1 and I_1Z are combined in operational amplifiers and converted into digital waveforms of voltage representing the sign of the quantities ($I_1Z–V_1$) and ($I_1Z'+V_1$) . The coincidence of these blocks is then measured. Blocks which are exactly 90 degrees out of phase are coincident for 4.17msec (1/4 cycle). Blocks which are less than 90 degrees out of phase are coincident for more than 4.17msec. The mho function consists of a filter card, a coincidence card, and a timer card which measures the coincidence of ($I_1Z–V_1$) and ($I_1Z'+V_1$) [12]. If the characteristic has no reverse reach the operating principle remains the same as just described except I_1Z' is zero.

The positive sequence directional comparison scheme consists of an overreaching tripping distance function, M_1T, an underreaching tripping distance function, $(M_1)_1$, and a blocking distance function, M_1B. The mho characteristics of the three functions are shown in Fig. 4.2b and they are obtained by using block average phase comparators with different ascending and descending integrating rates (non–circular characteristics are obtained by using different ascending and descending integrating rates) [12].

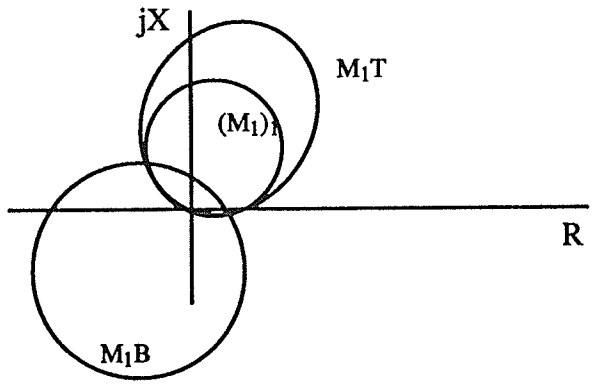


Figure 4.2b Mho characteristic of three positive mho tripping functions

The operate and reset times of each mho function are basically determined by the characteristic timer, the type of fault and the incidence angle. There is no significant time delay in the circuitry ahead of the timer in the simulated relay. Besides the described mho functions, the positive sequence directional comparison scheme also utilizes positive sequence overcurrent functions $I_1(T)$ and $I_1(B)$ for current supervision of the positive sequence tripping and blocking functions. This overcurrent supervision is primarily intended to prevent outputs of the positive sequence distance functions during the deenergizing transients of lines with shunt reactors. The $I_1(T)$ may also provide security for a condition of a blown potential transformer fuse if the application permits the use of pickup settings above load current. Furthermore, a pilot protection scheme is used to provide communication between the relays at both ends of the protected line.

Fig. 4.3 shows a detailed logic diagram of the positive sequence directional comparison scheme. For an internal three phase fault, either the underreaching $(M_1)_1$ or the overreaching M_1T will produce a TRIPBUS signal under supervision by the positive sequence overcurrent fault detector. When the $(M_1)_1$ function detects a fault, the procedure of producing a TRIPBUS signal is through AND2, OR8, OR10, OR11, AND32 to OR31. If only the M_1T function detects a fault, this means that the fault location is out of the underreaching $(M_1)_1$ protected zone, but it could still be near the remote end of the protected line. In this situation, a TRIPBUS signal can only be produced if AND16 receives a RCVR PILOT signal

from the relay at the remote end of the line looking into the same protected line. At the same time, the M_1T function will inhibit the blocking M_1B function through OR1, OR17 and NOT1.

For a three phase fault behind the relay, the blocking function M_1B will block the operation of AND16 and AND17. Since $(M_1)_1$ and M_1T do not detect the fault, even though AND16 may receive a RCVR PILOT signal generated by the M_1T function of the relay at the remote end, no TRIPBUS will be produced.

For a three phase fault further down and beyond the protected line, again no TRIP-BUS signal will be produced since AND16 will be inhibited by the absence of the RCVR PILOT from the relay at the remote end of the protected line.

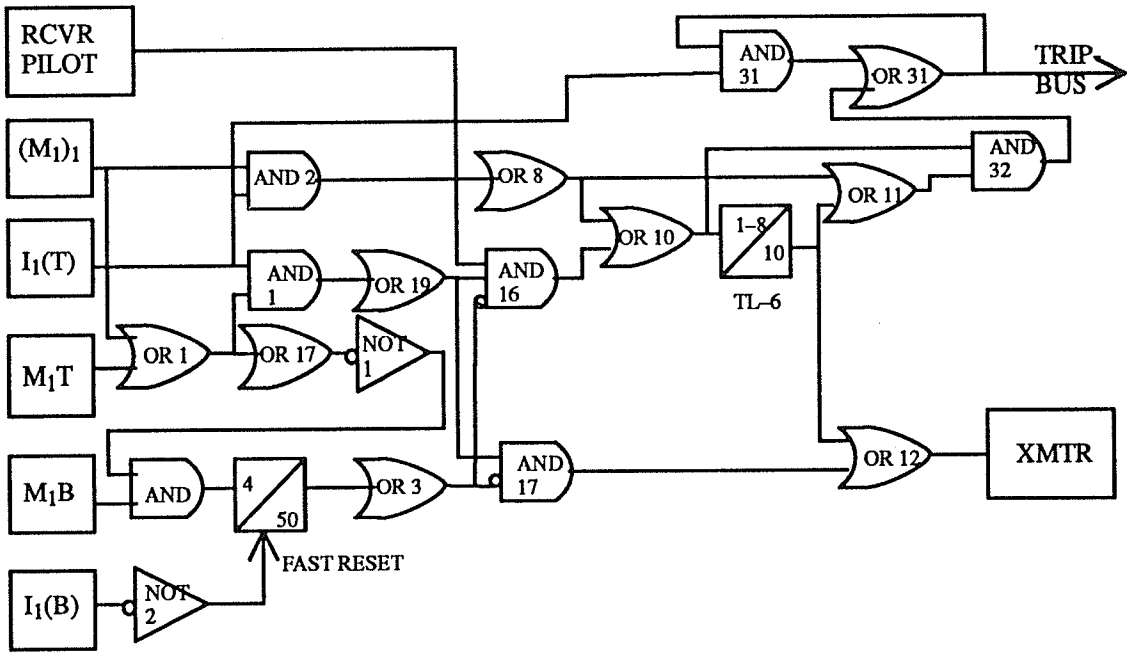


Figure 4.3 Positive sequence directional comparison

The $I_1(T)$ function is utilized to seal–in the trip circuit on internal three phase faults. This is necessary because the mho functions may reset and deenergize the TRIPBUS signal on a continuing close–in zero voltage fault due to a local stuck breaker condition. The $I_1(T)$ utilizes AND31 and OR31 to seal–in the TRIPBUS once a trip signal output is produced. The $I_1(B)$ positive sequence overcurrent function supervises the M_1B positive sequence mho

blocking function at the 4/50 M_1B characteristic timer to prevent spurious blocking outputs during the deenergizing transients in the line prior to automatic reclosing.

The TL6 timer provides a 10 msec prolonging of the trip permission channel after the local terminal has cleared to accommodate slower operation at the remote end of the line. The prolonging of the trip permission channel provides additional channel security and effective channel–relay coordination without any significant delay in pilot trip time.

4.1.2 Negative sequence directional comparison scheme:

The negative–sequence directional–comparison scheme utilizes negative–sequence current and voltage quantities to detect all types of unbalanced faults on the transmission line either with or without series capacitors. The scheme mainly includes forward $D_2(T)$ and reverse $D_2(B)$ blocking negative–sequence directional functions which respond to the fault locations. Also, a number of negative– and positive–sequence overcurrent functions are also included for fault detection and supervision of other functions utilized in the directional–comparison pilot–production schemes.

The forward $D_2(T)$ and reverse $D_2(B)$ blocking negative–sequence directional functions utilize negative sequence voltages V_2, and I_2Z which are proportional to the negative sequence current in the line. The coincidence between the quantities $V_2–I_2Z'$ and $–I_2Z$ is measured by the $D_2(T)$ and $D_2(B)$ timers. The $D_2(T)$ function will produce an output for a fault in the tripping direction if negative sequence quantities are generated. On the other hand, the $D_2(B)$ function will produce an output for an external fault behind the relay. For $V_2–I_2Z'$, the addition of the voltage component I_2Z' (which is proportional to the negative sequence current) to the negative–sequence polarizing voltage provides a reliable polarizing quantity for remote faults where the negative sequence voltage drop in the source may be very small.

Fig. 4.4 shows a detailed logic diagram of the negative–sequence directional–comparison scheme. For an internal unbalanced fault, the forward negative–sequence directional

tripping function $D_2(T)$ combines the negative–sequence overcurrent fault–detector $I_2(B)$ and the $(I_2–KI_1)(T)$ negative–sequence overcurrent fault–detector with positive sequence restraint to produce a TRIPBUS signal through AND3, OR19, AND16, AND32 and OR31. This is allowed by receiving a RCVR PILOT signal from the remote end of the protected line by AND16. The reverse–blocking negative–sequence directional function $D_2(B)$ will be inhibited by NOT3, and will not play a role in the protection scheme in this situation. During the operation, a tripping transmitter signal XMTR will be transmitted to the relay at the remote end of the line through AND17 and OR12.

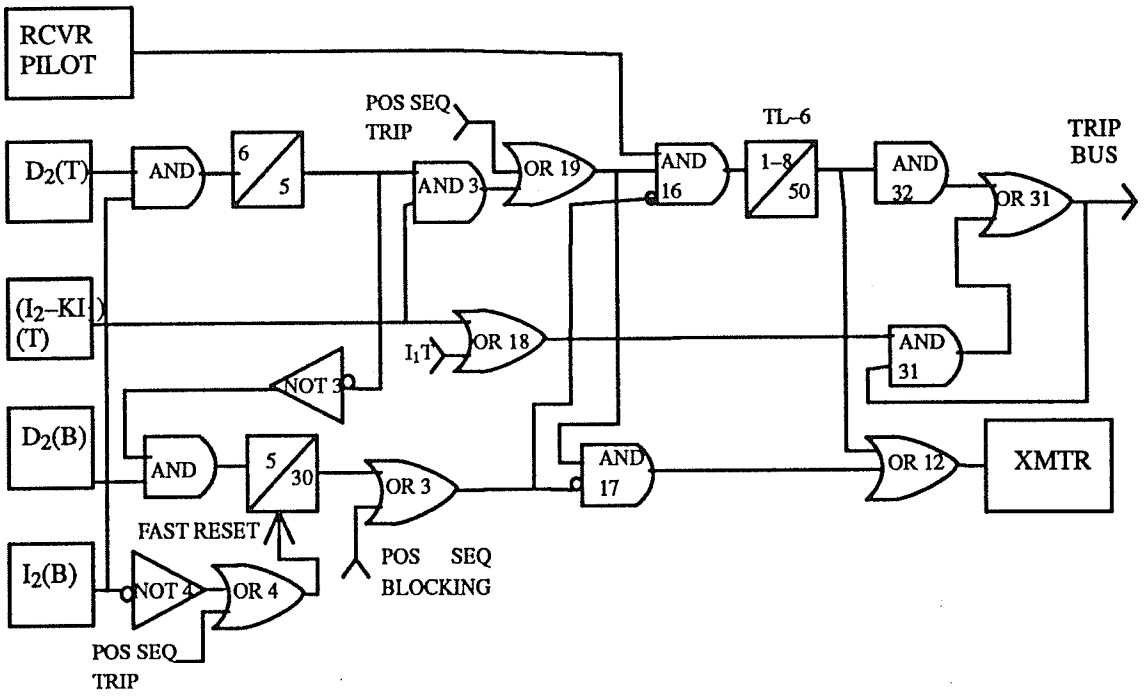


Figure 4.4 Negative sequence directional comparison

For an external unbalanced fault behind the relay, only $D_2(B)$ detects the fault. This factor, combined with the output of NOT3, will inhibit AND16 and AND17. In this situation, even though a tripping RCVR PILOT signal may be received from the remote end relay, no local TRIPBUS signal will be produced.

For an external unbalanced fault beyond the remote end relay, $D_2(T)$ will produce a tripping transmitter signal XMTR to the remote end relay. Since a tripping RCVR PILOT

signal will be received by an inhibited AND16 at the remote end relay, a local TRIPBUS signal will not be produced at the remote end. At the same time, no RCVR PILOT signal will be received at the local relay to further any operation.

The addition of a small positive sequence component KI_1 in the $(I_2–KI_1)(T)$ negative–sequence overcurrent function inhibits operation on unsymmetrical system impedance or current, or potential source errors under load conditions. $(I_2–KI_1)(T)$ is utilized to seal–in the trip circuit on internal unbalanced faults through OR18 and AND31. I_1T is also used because it provides more reliability on very large fault currents for near–end three–phase faults which require maximum relaying speed.

4.1.3 Direct tripping scheme:

The direct tripping scheme provides supplemental protection for faster operation on heavy internal faults or to cover special operating conditions. Fig. 4.5 shows a detailed logic diagram of the direct tripping scheme with various independent direct tripping functions. The underreaching positive sequence mho tripping function $(M_1)_1$ provides high speed direct tripping for internal balanced faults, close–in phase–phase and phase–phase–ground faults under the supervision of the overcurrent fault detector $I_1(T)$. This overcurrent supervision is primarily intended to prevent outputs of the positive sequence distance functions during the deenergizing transients of lines with shunt reactors. The $I_1(T)$ may also provide security against a condition of potential failure if the application permits the use of pickup settings above load current.

The high–set positive–sequence overcurrent direct–tripping function I_1T also provides high speed tripping for close–in three–phase faults. The zero–sequence direct–tripping function $(3I_0–KI_1)T$ provides high speed tripping on heavy phase–to–ground and interphase–to–ground faults. The positive sequence restraint KI_1 provides a larger difference between the $3I_0–KI_1$ quantity on internal and external faults. The $(I_2–KI_1)(T)$ negative–sequence overcurrent fault–detector with positive sequence restraint is used to seal–in the trip

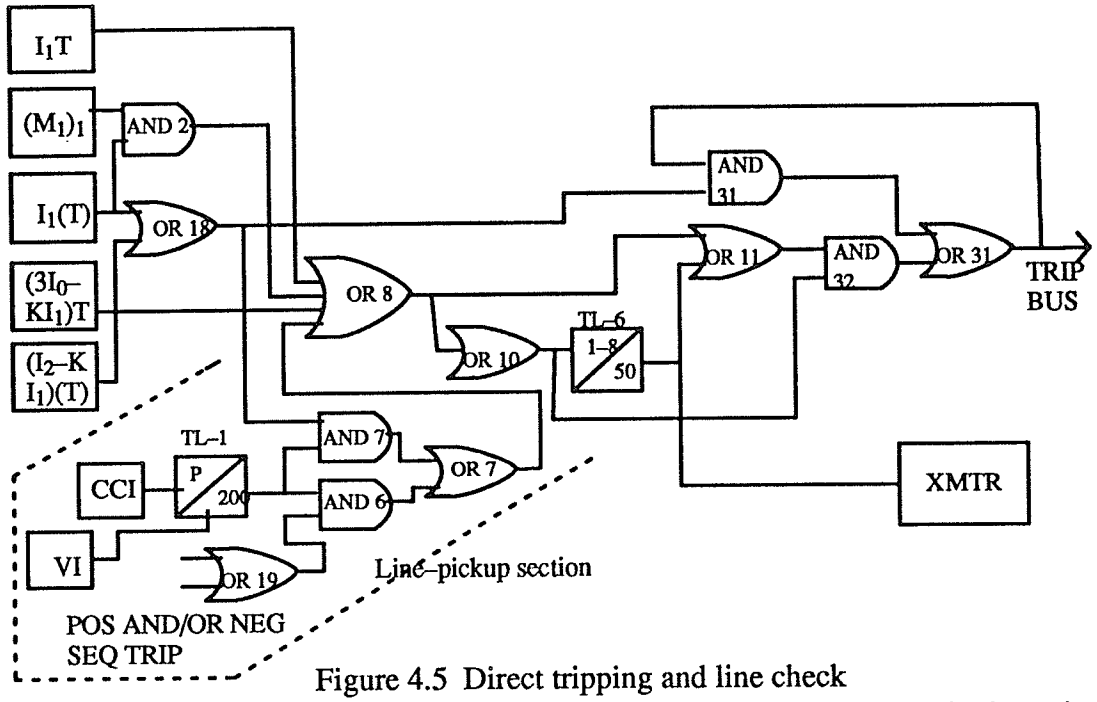


Figure 4.5 Direct tripping and line check

circuit on unbalanced internal faults. The 'line pickup' section in the direct tripping scheme is not set up in this thesis.

4.2 Performance of the GE relay on the Dorsey–Forbes–Chisago line:

The positive sequence directional comparison scheme, negative sequence directional comparison scheme, and the direct tripping scheme are simulated in FORTRAN to study the performance of the three schemes on protecting the Dorsey–Forbes–Chisago line. A Dorsey–Forbes–Chisago 500kV line model is set up by using the EMTDC program, and its accuracy was proven by comparing stage fault test waveforms to the fault simulation results run on the setup model in the previous chapter. Although the GE relay algorithm in this research is not exactly translated from the electronic components of the relay, the main idea of the mechanism is preserved. In this section, the performance of the three protection schemes on the existing uncompensated Dorsey–Forbes–Chisago 500kV line and the future series compensated transmission line system will be studied.

4.2.1 Existing system with old relay–settings:

The existing uncompensated Dorsey–Forbes–Chisago 500kV line model with load flow conditions similar to that in the staged fault test 4a is set up by using the EMTDC program. A GE Relay with existing relay settings is simulated to run on different fault situations to show the mechanism and performance of the relay on the existing system.

When a three–phase–ground fault occurs approximately 200 km form Dorsey on the 528 km Dorsey–Forbes line, the positive sequence directional comparison scheme and the direct tripping scheme relays are expected to produce a tripbus. Since it is a balanced fault the negative sequence directional comparison scheme is expected not to produce a trip signal.

4.2.1.1 *Positive sequence directional comparison scheme:*

A single line diagram of the faulted transmission line system is shown in Fig. 4.6. The three–phase–ground fault is applied at T2 on the Dorsey–Forbes line section with a very small resistance. The busbar voltage and line current measured at the Dorsey end are shown in Fig. 4.7a, and the three–phase voltages and currents are shown in Fig. 4.7b.

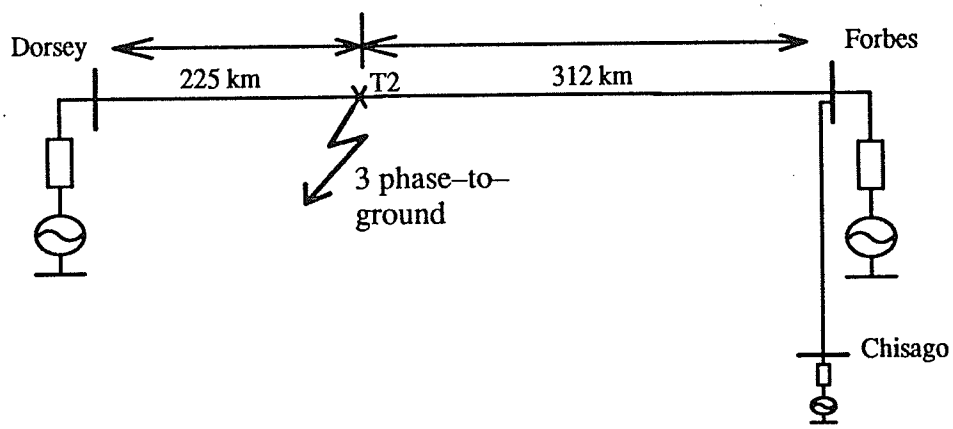


Figure 4.6 Existing transmission system with the fault location

Fig. 4.8 shows the inputs and outputs in the positive–sequence directional–comparison scheme logic diagram with voltages and currents measured at the Dorsey busbar. The fault occurs when time=0, and the fault simulation is run for a total time period of 0.24 sec-

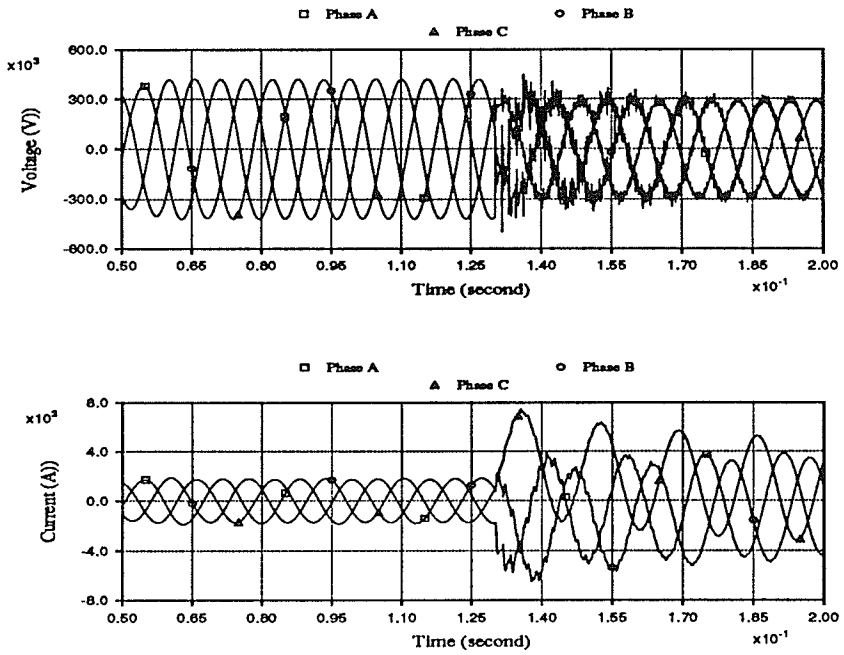


Figure 4.7a Voltage and Current waveforms measured at the Dorsey busbar

onds. The $I_1(T)$ positive–sequence overcurrent fault–detector for trip supervision stays at '1' during the whole simulation. This is due to the original low setting of the overcurrent detector. The $(M_1)_1$ underreaching positive–sequence mho tripping–function and M_1T overreaching positive–sequence mho tripping–function both detect the fault (output reaches '1') at approximately 1 cycle after fault. These will automatically inhibit the output of the positive–sequence reversed–mho blocking–function M_1B which produces a '0' output in this case. On the other hand, the relay at the remote end of the line transmits a tripping RCVR PILOT signal to the Dorsey end, and the combination of the RCVR PILOT signal, $(M_1)_1$, M_1T, $I_1(T)$ and the inhibited M_1B produce a local TRIPBUS signal and a tripping XMTR signal to the remote–end positive–sequence relay.

Fig. 4.9 shows the inputs and outputs in the positive–sequence directional–comparison–scheme logic diagram with voltages and curents measured at the Forbes busbar. The overall operation at this end is similar to that of the remote Dorsey end. Again the $I_1(T)$ positi-

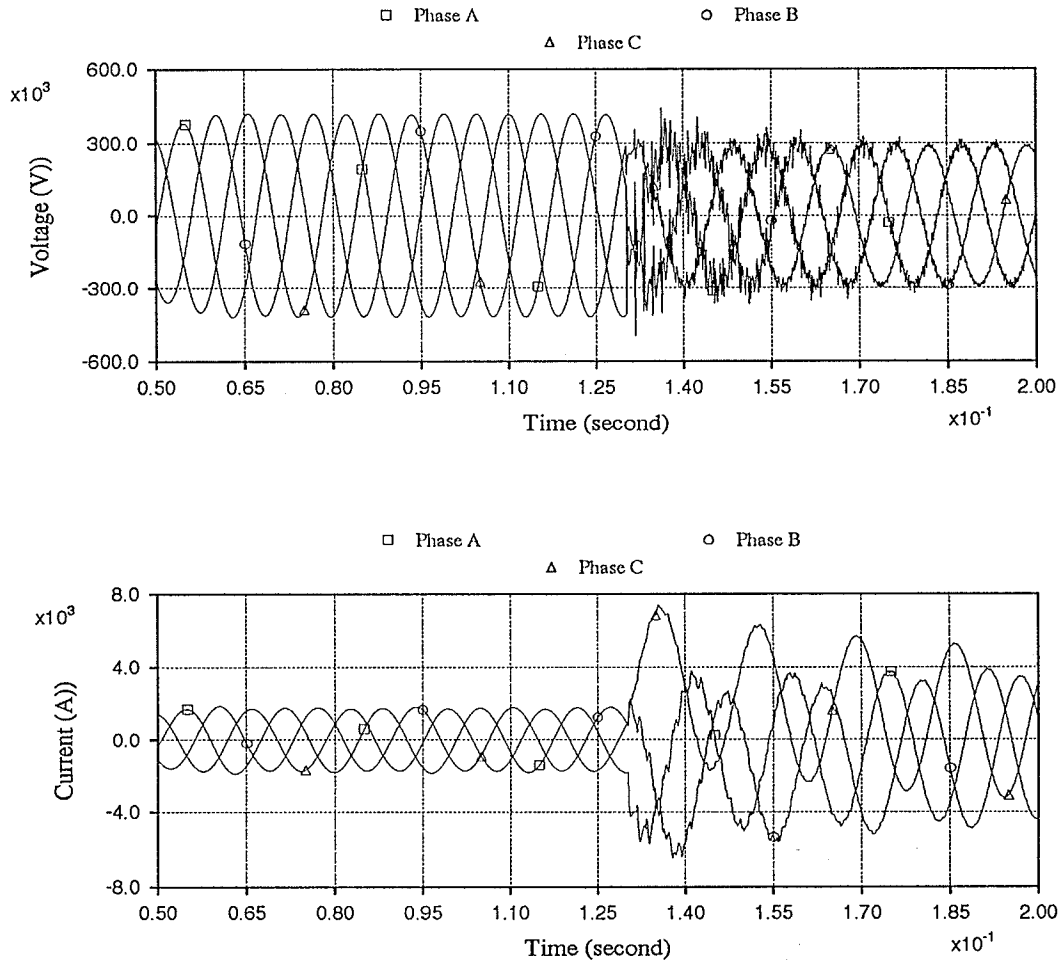


Figure 4.7b Three-phase voltages and currents measured at the Dorsey busbar

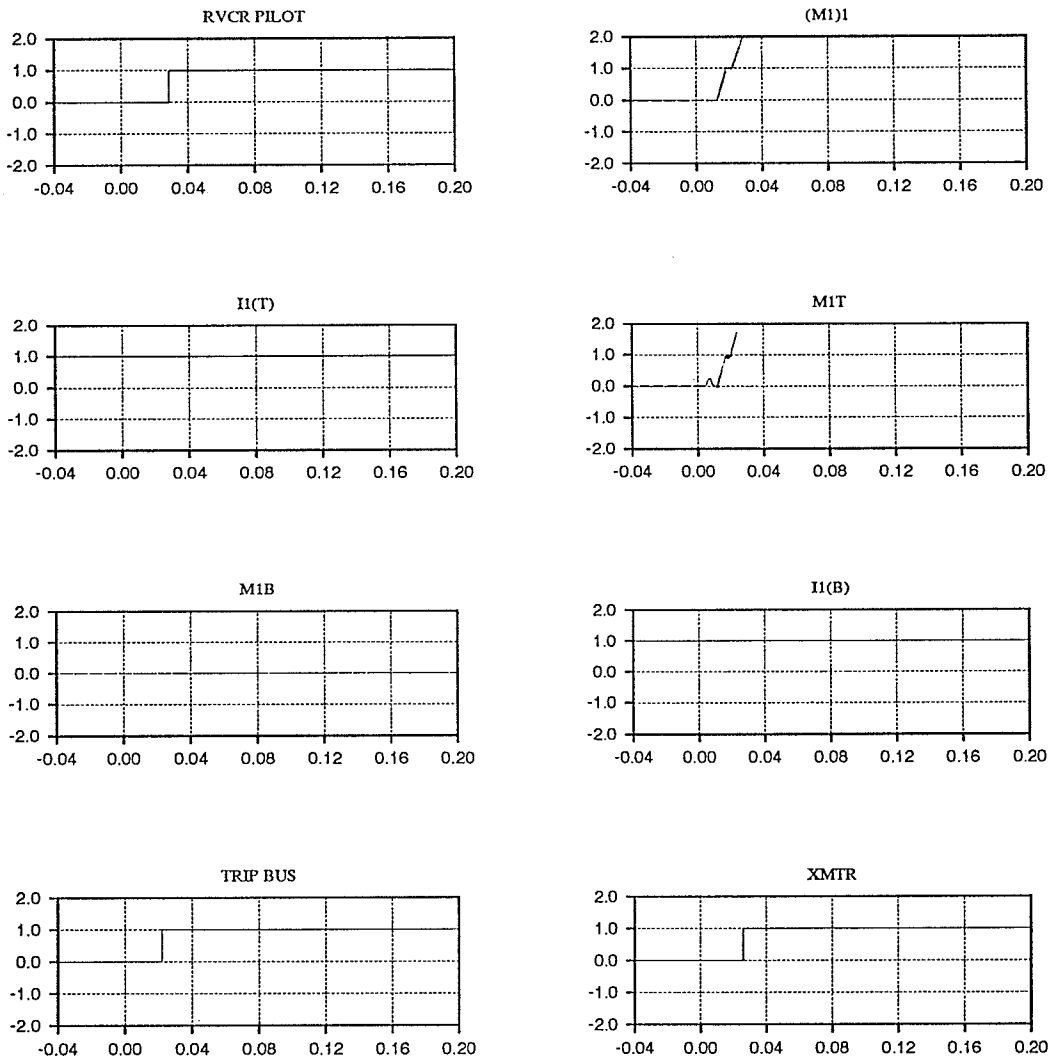


Figure 4.8 Positive sequence directional comparison inputs and outputs for the Dorsey relay

ve-sequence overcurrent fault-detector stays at "1" all the time. Both the $(M_1)_1$ and M_1T detect the fault approximately one cycle after fault and inhibit M_1B from affecting the operation. A tripping RCVR PILOT signal is received from the relay at the remote Dorsey end and the combination of $I_1(T)$, $(M_1)_1$, M_1B and tripping RCVR PILOT signal cause a local TRIPBUS signal. A tripping XMTR signal is also transmitted to the Dorsey end relay to allow a local trip at Dorsey.

4.2.1.2 *Direct tripping scheme:*

The Direct Tripping Scheme provides supplemental protection for faster operation on heavy internal faults. Fig. 4.10 shows the inputs and outputs in the direct tripping scheme

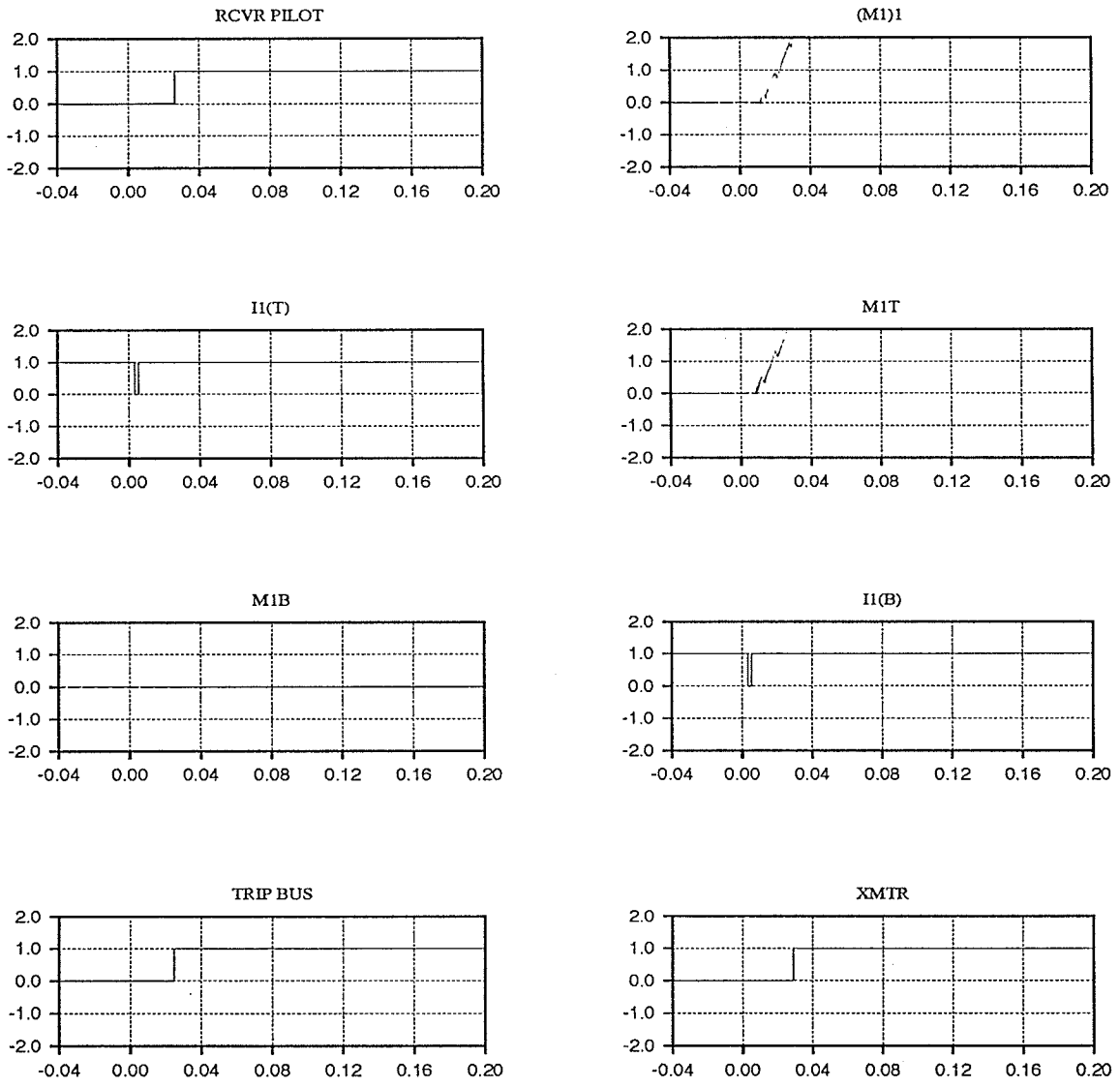


Figure 4.9 Positive sequence directional comparison inputs and outputs for the Forbes relay

logic diagram with voltages and currents measured at the Dorsey busbar for a three-phase-ground fault at T2 in Fig. 4.6. The positive-sequence overcurrent direct-tripping function I_1T reaches "1" within 1 cycle after fault. This is the overcurrent detector that responds to the internal heavy balanced fault in the direct tripping scheme, and it directly generates a TRIPBUS signal.

On the other hand, the underreaching positive-sequence mho tripping-function $(M_1)_1$ picks up the fault about 1 cycle after fault, the $(M_1)_1$ combines with the positive-sequence overcur-

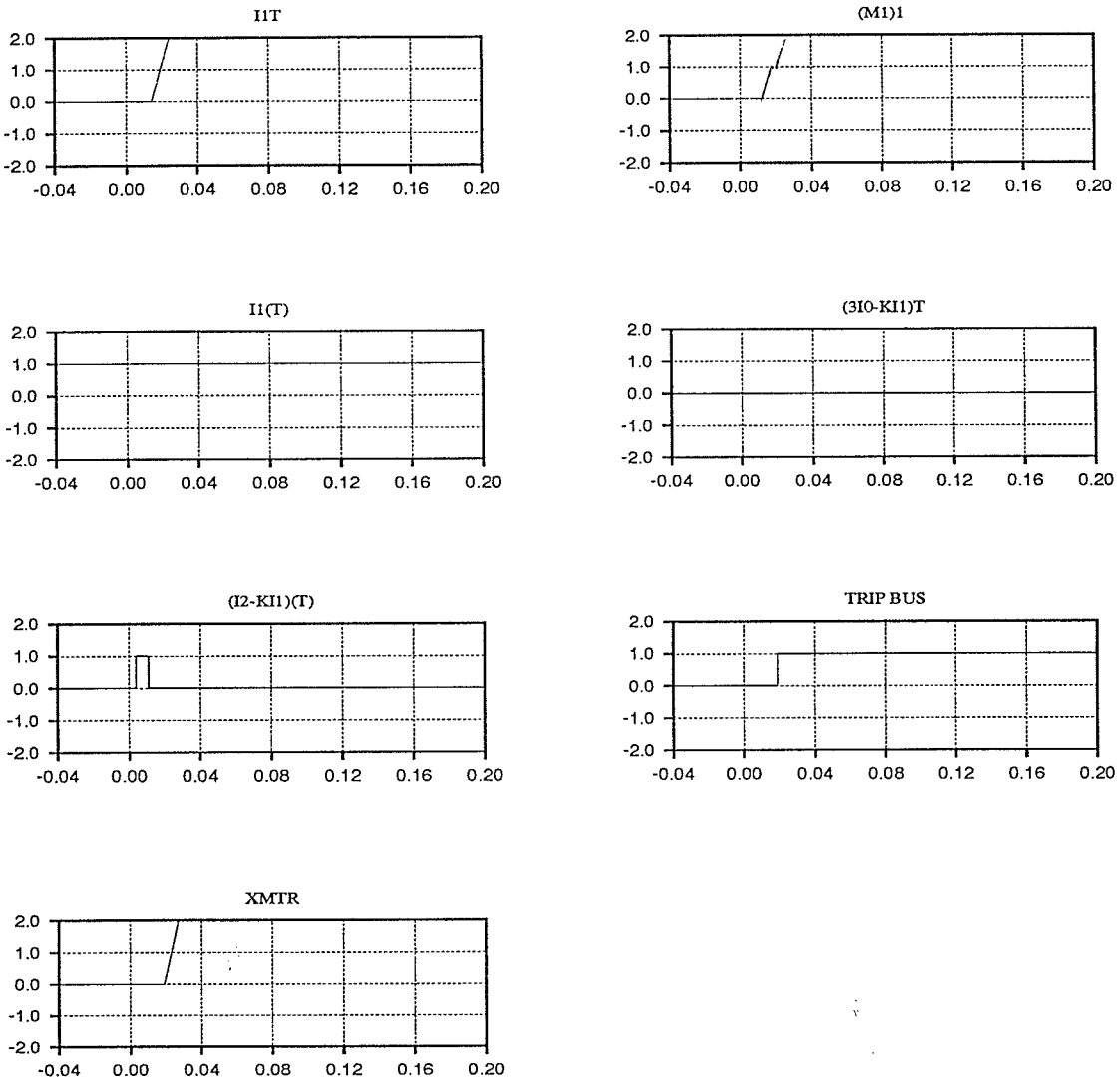


Figure 4.10 Direct tripping scheme inputs and outputs for the Dorsey relay

rent fault-detector-for-trip-supervision $I_1(T)$ to directly generate a TRIPBUS signal. The direct tripping relay sends a tripping XMTR signal to the remote end breaker to isolate the faulted line from other healthy lines. Notice that the time it takes to signal a TRIPBUS in the direct tripping scheme is a little bit faster than that of the positive sequence directional comparison scheme in this case.

Fig. 4.11 shows the inputs and outputs in the direct-tripping scheme logic-diagram with voltages and currents measured at the Forbes busbar. Since T2 is 155km closer to Dorsey than to the Forbes busbar, the positive-sequence overcurrent direct-tripping function I_1T at Forbes does not detect the fault. However, the underreaching positive-sequence

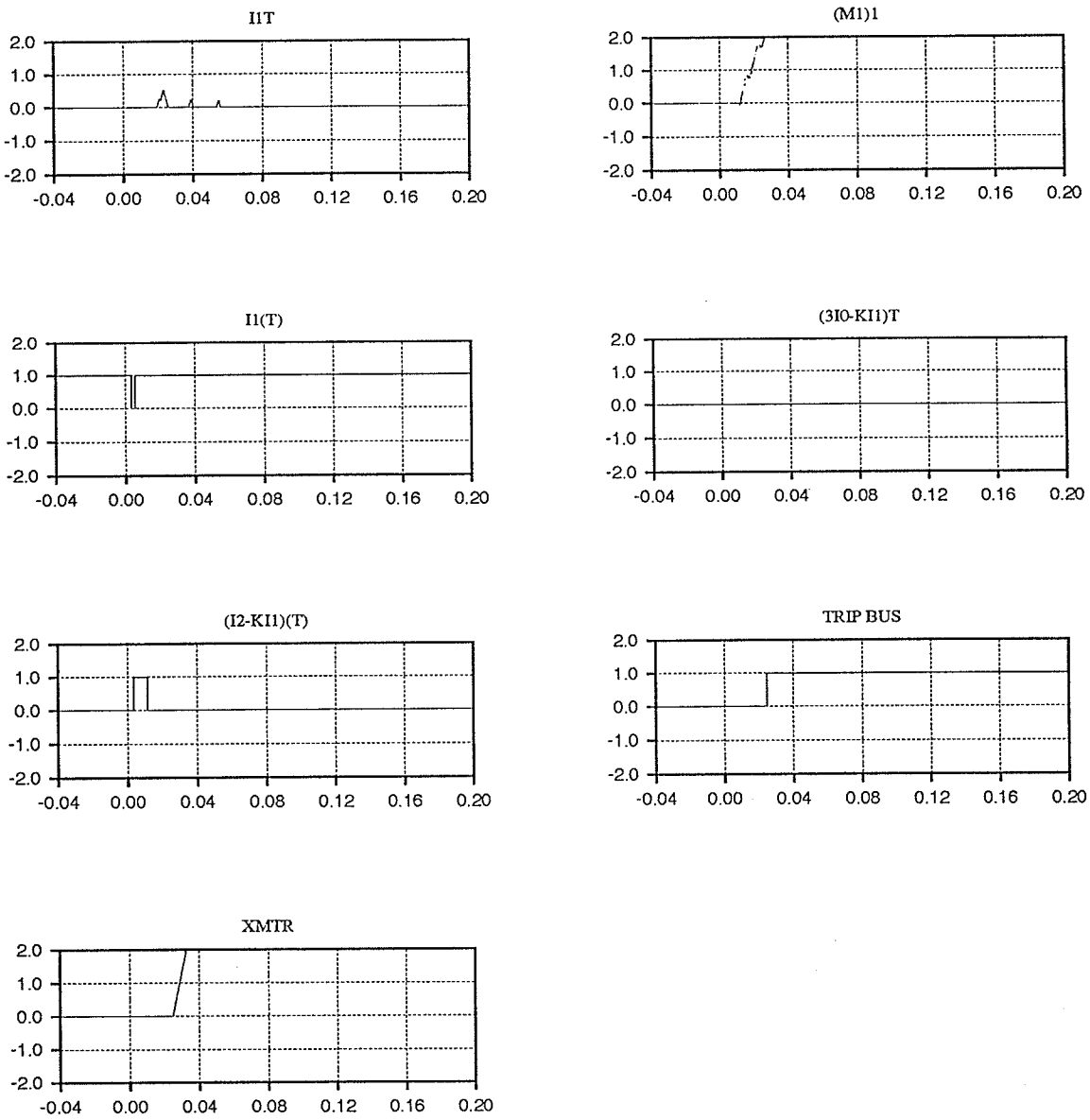


Figure 4.11 Direct tripping scheme inputs and outputs for the Forbes relay

mho tripping–function $(M_1)_1$ does detect the fault after 1 cycle following fault occurrence. These combined with $I_1(T)$ will generate a tripping signal. Notice that the time of producing a TRIPBUS signal is slightly longer for the Forbes end relay than the Dorsey end relay.

4.2.1.3 *Negative sequence directional comparison scheme:*

For an unbalanced single–line–ground fault at T2 on the Dorsey–Forbes line section, the negative–sequence directional–comparison scheme is expected to detect the fault. The

direct tripping scheme operates according to the overcurrent detector setting of the zero-sequence direct-trip overcurrent-function with positive sequence restraint $(3I_0-KI_1)T$. In this case, the direct tripping scheme will not produce a tripping signal since the level of the $(3I_0-KI_1)T$ overcurrent detector function is set too high. As a result, only the negative-sequence directional-comparison scheme logical input/output are shown here. The $(3I_0-KI_1)T$ overcurrent detector also responds to heavy phase-phase-ground faults on the line.

Fig. 4.12 shows a single line diagram of the faulted transmission line system. The single-line-ground fault is applied at T2 on the Dorsey-Forbes line with a very small resistance.

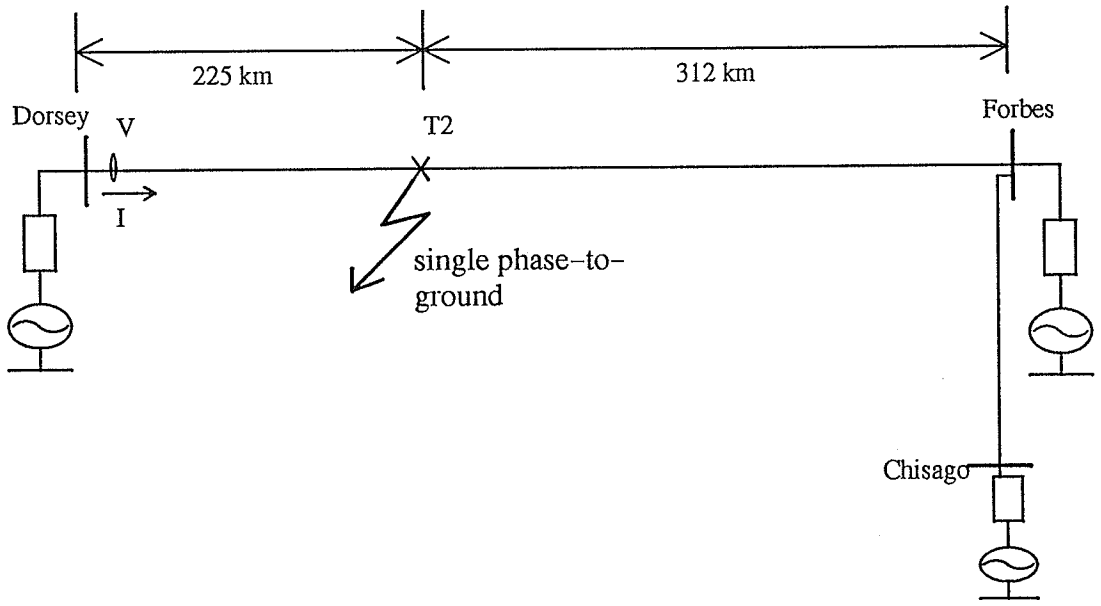


Figure 4.12 Existing transmission line with the fault location

The busbar voltages and line currents at the Dorsey end are ahown in Fig4.13.

Fig. 4.14 shows the inputs and outputs in the negative-sequence directional-comparison scheme logic-diagram with voltages and currents measured at the Dorsey busbar. The negative-sequence forward directional-function $D_2(T)$ stays above '1', this indicates that

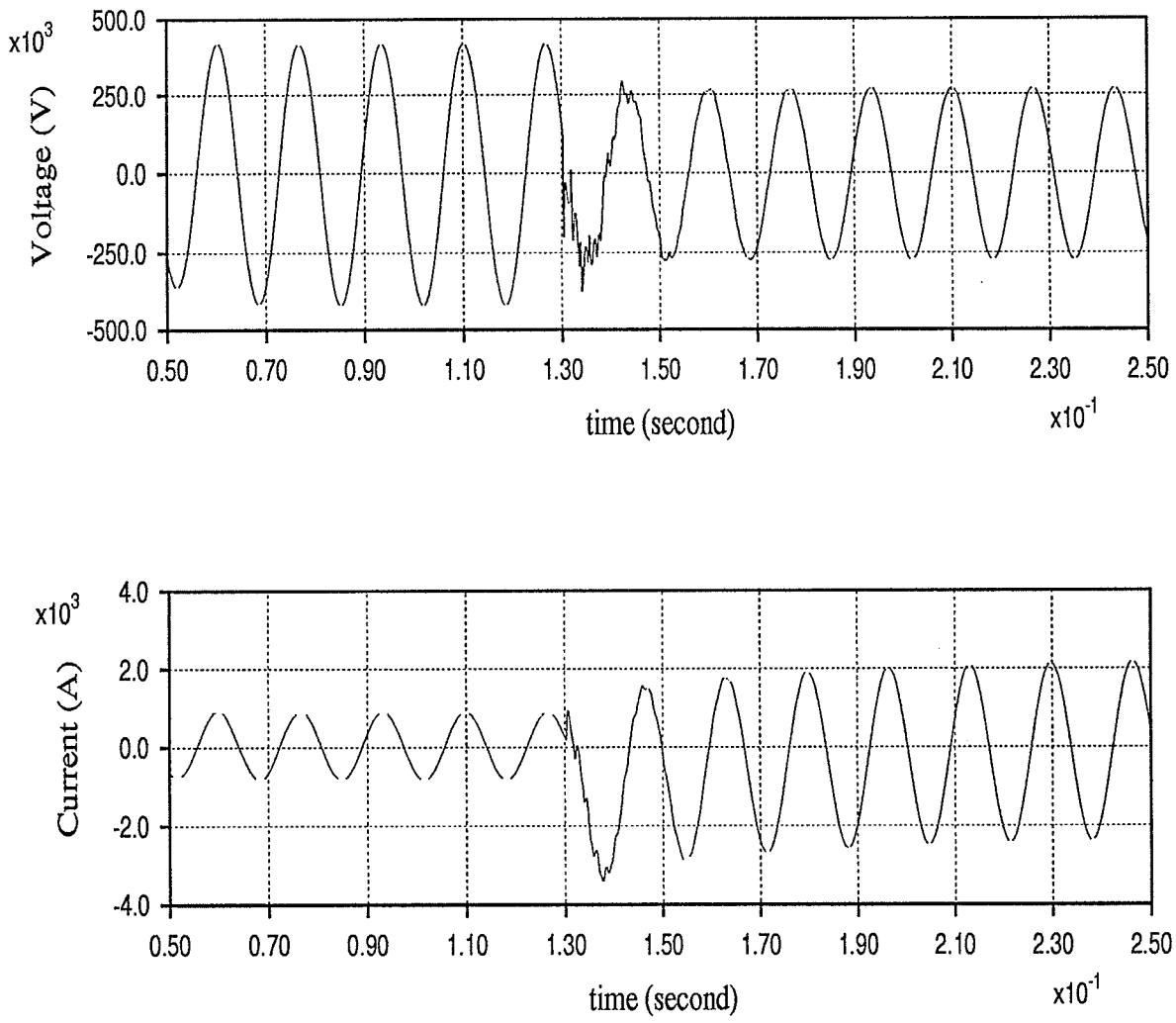


Figure 4.13 Waveforms at Dorsey

the unbalanced fault is in front of the Dorsey relay. Then $D_2(T)$ combines with the negative-sequence overcurrent fault-detector $I_2(B)$ to inhibit the negative-sequence reverse directional-function $D_2(B)$ which has detected no unbalanced fault behind the Dorsey relay. The combination of the remote end tripping RCVR PILOT signal, $D_2(T)$ and $I_2(B)$ produce a local TRIPBUS signal and a tripping XMTR signal to the remote end relay. The negative-sequence overcurrent fault-detector with positive sequence restraint $(I_2-KI_1)(T)$ will keep the local TRIPBUS signal at '1' even when $D_2(T)$ stops picking up the fault.

The inputs and outputs in the logic diagram for the negative-sequence directional-comparison scheme at the Forbes end are similar to that of the Dorsey end. For the relays

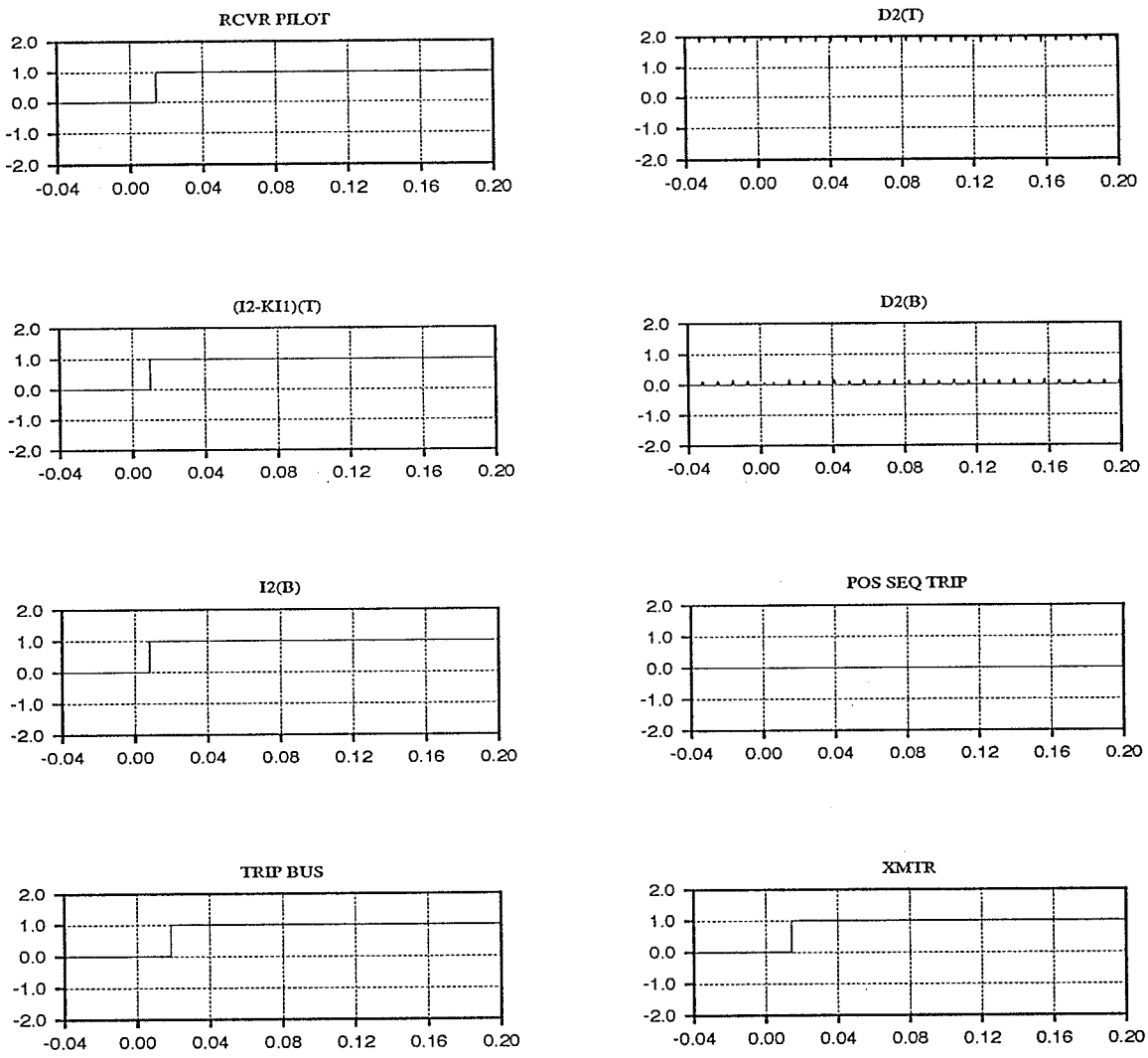


Figure 4.14 Negative sequence directional comparison inputs and outputs for the Dorsey relay

at both ends, the time of producing a tripbus in this fault situation is within 1 cycle after fault if communication delays are not included.

The negative sequence directional comparison scheme also responds to phase-phase-ground fault and phase-phase fault in a similar way.

4.2.2 New system with old relay-settings:

The future series-compensated line will run on a regular load flow condition that involves maximum line currents. With addition of the compensated capacitor banks, the parameters of the transmission line are changed. The changes in measured line impedance can

lead to the maloperation of the GE relay with existing settings which include impedance reaches and overcurrent detector levels.

For a three-phase-ground balanced fault behind the Dorsey busbar, shown in Fig. 4.15, the compensating capacitor will stay in the system as an operating component since the fault location is too far away from the capacitor banks to activate the MOV's. The compensation on the line impedance will drive the measured fault impedance into the mho characteristic of the underreaching positive sequence relay at the Forbes busbar giving a direct trip condition.

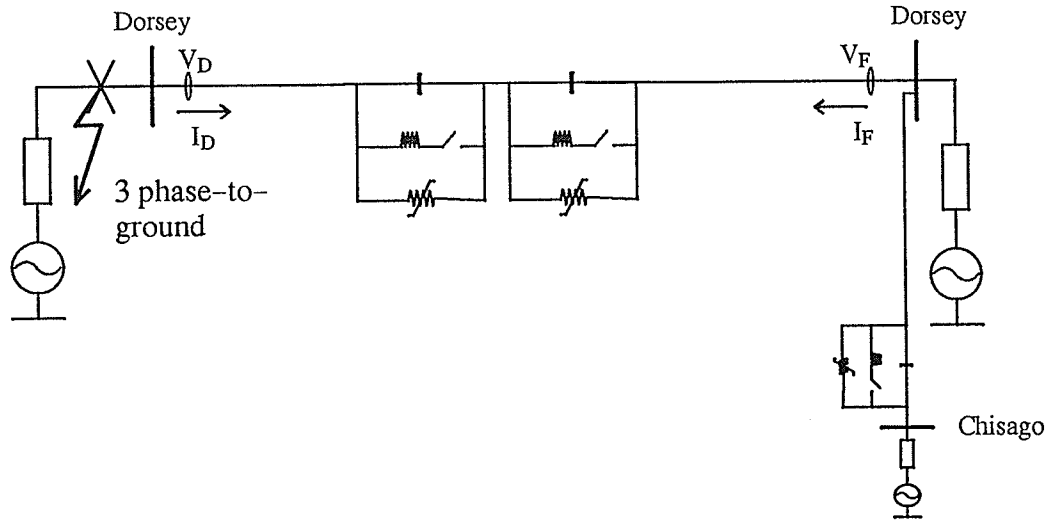


Figure 4.15 Future series-compensated system

Fig. 4.16 shows the inputs and outputs of the positive-sequence directional-comparison scheme logic-diagram with voltages and currents measured at the Forbes busbar. The underreaching positive-sequence mho tripping-function $(M_1)_1$ reaches "1" shortly after the fault has lasted for 1 cycle. The overreaching positive-sequence mho tripping-function M_1T has no effect on the local TRIPBUS signal since no tripping RCVR PILOT signal is received from the remote end relay at Dorsey.

For the direct tripping scheme, the positive-sequence overcurrent direct-tripping function I_1T and the underreaching positive-sequence mho tripping-function $(M_1)_1$ are the essential elements that contribute to the detection of the three-phase balanced fault. Fig. 4.17

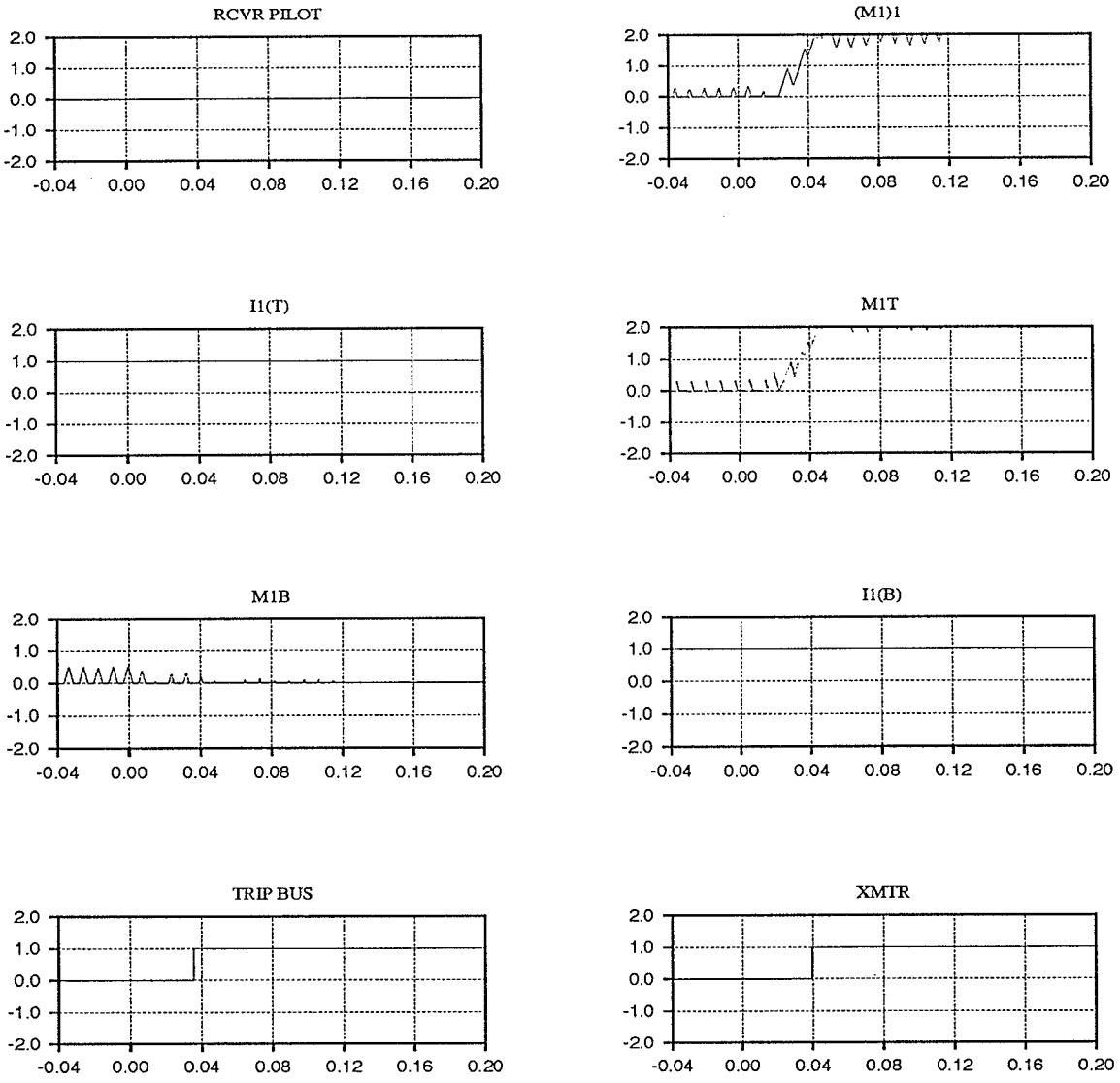


Figure 4.16 Positive sequence directional comparison inputs and outputs for the Forbes relay

shows the inputs and outputs of the direct tripping scheme with voltages and currents measured at Dorsey. The I_1T overcurrent detector will detect the sudden increase of positive sequence curent when the three-phase-ground fault is behind the Dorsey busbar, with currents provided from the power source at the Forbes end. In this case, the $(M_1)_1$ will not detect the fault since it is behind the relay. However, I_1T exceeds "1" one cycle after fault, and $I_1(T)$ keeps the local TRIPBUS signal at "1". A tripping XMTR signal is sent to the remote end busbar shortly after the local direct TRIPBUS signal is produced.

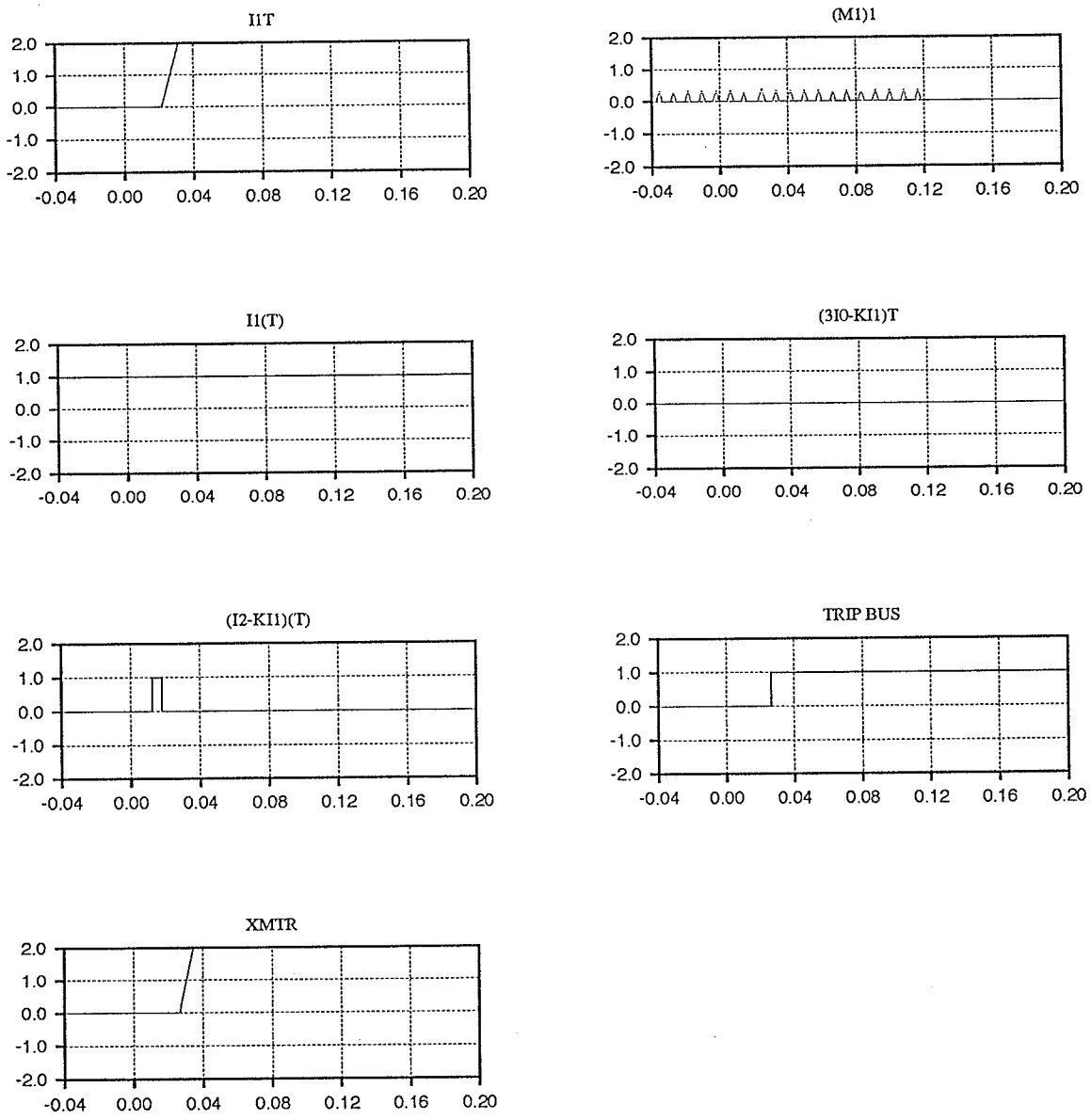


Figure 4.17 Direct tripping scheme inputs and outputs for the Dorsey relay

For the direct tripping scheme relay at the Forbes busbar, since $(M_1)_1$ has already detected the fault due to the compensation of the line impedance by the series capacitors, a direct TRIPBUS signal is generated accordingly. However, the I_1T also signals a trip due to the large amount of positive sequence current.

Up to this point, the only load flow condition that has been considered is the future everyday operating condition. In order to ensure the reliability of the relay model, another load flow condition involving minimum line currents has been set up. In the case that the

future system faces an extreme load flow condition that involves minimum line current, $(3I_0-KI_1)T$ zero-sequence direct-trip overcurrent function with positive sequence restraint responds to both unbalanced single-line-ground and phase-phase-ground faults in the direct tripping scheme. The existing current level setting of $(3I_0-KI_1)T$ is too high . This means the direct tripping scheme only covers a very small region of fault location on the line. For example, even a phase-phase-ground fault at T4 will not trigger the $(3I_0-KI_1)T$ detector at the Forbes end, and that is only 93 km away from the Forbes busbar.

4.3 Settings-modification and performance of the GE relay on the series-compensated Dorsey-Forbes-Chisago line:

The problems of the GE Relay with existing settings on the compensated Dorsey-Forbes-Chisago line are:

1. $(M_1)_1$ impedance settings are too high. This leads to the production of a TRIPBUS signal for balanced three phase faults outside the protected line in the direct tripping scheme and the positive sequence directional comparison scheme.

2. I_1T overcurrent detector settings are too low. This leads to maloperation for three-phase-ground faults outside the protected line for the direct tripping scheme.

For the $(M_1)_1$ function at the Dorsey end, it is very important to know that if the range is shortened to a certain amount, it may not cover a fault near T3. Since a fault occurring between T2b and T3 may cause the bypass switch to close, the compensation effect of the capacitor will disappear. This makes the measured line impedance larger than that for situations with the capacitor in. The goal is to set the $(M_1)_1$ function at both ends to cover as much line section as possible, and not overreach for faults occurring outside the protected line section.

The $(M_1)_1$ function settings have to survive not only in a typical load flow situation, but in extreme low current conditions as well. In this thesis, two cases of load flow conditions are considered. The first one is the future everyday operating system load flow condition which involves maximum line current and the second involves very low power flow which involves minimum line current. The first case involves series compensation while the second case does not. Both situations will be possible in the future.

4.3.1 Case 1 - Series-compensated system involving maximum line current:

Fig. 4.18 shows a single line diagram of the series compensated Dorsey–Forbes–Chisago line .

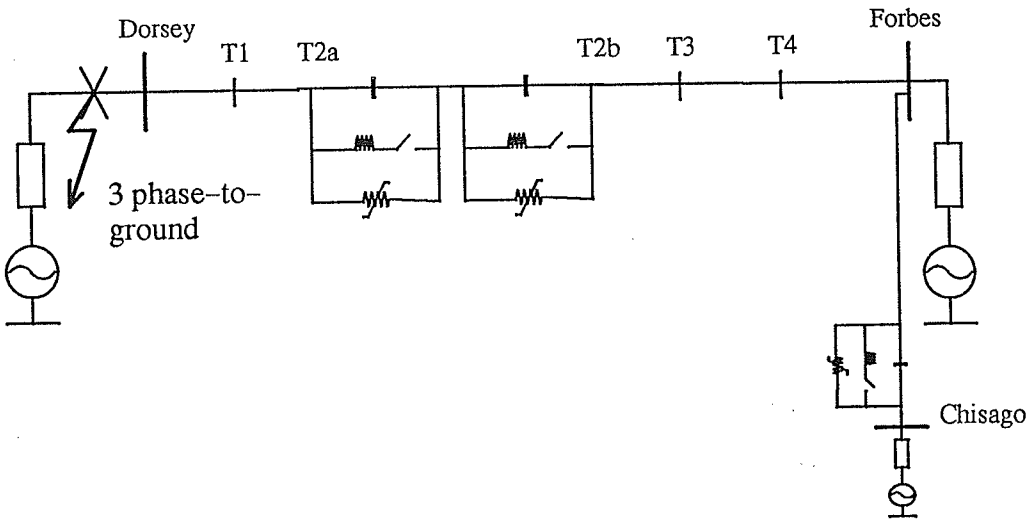


Figure 4.18 Series–compensated line involving maximum line currents

The approximate impedance of each line section is listed as follows:

Dorsey–T1	31.3 ohms	88km
T1–T2a	48.7 ohms	137km
T2b–T3	31.7 ohms	99km
T3–T4	38.5 ohms	120km
T4–Forbes	29.8 ohms	93km

and the reactance of the capacitors is 83 ohms.

The reach of the underreaching positive-sequence mho tripping-function $(M_1)_1$ has to be set as far as possible, and at the same time must not operate for faults at or beyond the remote end busbar. Furthermore, a safety margin of 5-10 % should be left for error. The reach of the existing settings for $(M_1)_1$ for both ends of the line is 129.8 ohms. This will cause over-reach since the impedance of the line with series compensation drops to approximately 100 ohms.

Balanced three-phase-ground fault simulations have been done at different locations on the series-compensated line. Studies show that an impedance reach of 85 ohms and 75 ohms for the $(M_1)_1$ mho tripping function respectively at the Dorsey and Forbes ends, should be used. With the new relay settings, the Dorsey $(M_1)_1$ mho tripping function will cover from the Dorsey busbar up to T4, and the $(M_1)_1$ function at the Forbes end will cover from the Forbes busbar to T4 and the small line section just beyond the capacitor banks. The $(M_1)_1$ mho tripping functions at both ends have an intersection around T4. In this thesis, we feel that there is no significant need to alter the reach settings of the M_1T overreaching positive-sequence mho tripping-function since the excess protection on zone2 will not affect the protection scheme in zone1 in any way.

The performance of the positive-sequence directional-comparison scheme with the new reach setting on $(M_1)_1$ for three-phase-ground faults on different locations is shown in Table 4.1. From this point on, a 20 msec of nominal communication delay will be considered into the time of producing a TRIPBUS.

Table 4.1 New $(M_1)_1$ relay setting on three-phase-ground faults

	Dorsey end $(M_1)_1$ (msec)	Forbes end $(M_1)_1$ (msec)	Dorsey end TRIPBUS (msec)	Forbes end TRIPBUS (msec)
Dorsey busbar	9.85	-----	10.18	39.61
T1	9.85	-----	10.18	38.42
T2a	17.85	44.84	18.19	45.1
T2b	33.2	-----	33.46	67.19

T3	32.27	-----	32.87	61.04
T4	40.87	18.19	41.47	18.78
Forbes busbar	-----	14.15	43.58	14.48

In the direct tripping scheme, the positive-sequence overcurrent function I_1T is designed for fast operation on heavy internal three-phase-ground faults. The existing I_1T overcurrent detector at both the Dorsey and Forbes ends produce TRIPBUS signals for three-phase-ground faults behind the busbars. The existing setting for I_1T at both ends is 1920 A_{rms} (2715.3 A_{peak}). Table 4.2 shows the positive sequence currents measured at both ends of the Dorsey-Forbes line section for three-phase-ground faults at different locations.

Table 4.2 Positive sequence current for three-phase-ground faults

	I_1 measured at Dorsey (A_{peak})	I_1 measured at Forbes (A_{peak})
Behind Dorsey busbar	3679	3033
Dorsey busbar	12880	3033
T1	7515	3496
T2a	4336	4637
T2b	6205	2661
T3	5092	3661
T4	4147	5618
Forbes busbar	3588	8961
Beyond Forbes busbar	3588	3783

Table 4.2 shows that I_1T will signal a direct tripbus for three-phase-ground fault just behind either busbar. As a result, the level of I_1T has to be raised to avoid such a maloperation. Since the positive sequence current for three-phase-ground fault in different load flow conditions vary, those conditions that produce minimum positive sequence fault currents have to be studied before a final I_1T setting is set. At this moment, a I_1T setting of over 3800 A_{peak} should be adequate.

4.3.2 Case 2 - Non-compensated system involving minimum line current:

In this case, series compensation is not used. Moreover, in all three substations, the source impedances are doubled and one transformer is used instead of two. Power flow from Dorsey is limited to below 20MW. The performance of the positive-sequence directional-comparison scheme with new reach settings on $(M_1)_1$ on three-phase-ground fault on different locations are shown in Table4.3.

Table 4.3 New $(M_1)_1$ setting on three-phase-ground faults

	Dorsey $(M_1)_1$ (msec)	Forbes $(M_1)_1$ (msec)	Dorsey TRIP-BUS (msec)	Forbes TRIP-BUS (msec)
Dorsey busbar	13.89	-----	14.15	42.66
T1	16.33	-----	16.6	44.84
T2	22.15	-----	22.48	50.66
T3	-----	24.6	53.11	24.93
T4	-----	18.19	46.96	18.45
Forbes	-----	16.0	44.51	16.33

The $(M_1)_1$ mho tripping functions at both the Dorsey and Forbes ends may not cover the line section between T2 and T3. However, this particular line section will be covered by the pilot tripping function. Table 4.4 shows the positive sequence currents measured at both ends of the Dorsey-Forbes line for three-phase-ground faults at different locations.

Table 4.4 Positive sequence current for three-phase-ground faults

	Dorsey I_1 (A_{peak})	Forbes I_1 (A_{peak})
Behind Dorsey	1739	1688
Dorsey busbar	6041	1921
T1	4467	2144
T2	3071	2300
T3	2514	2732

T4	2027	3539
Forbes busbar	1752	4740
Beyond Forbes	1752	1903

With I_1T set at 3800 A_{peak}, the direct trip relays at both ends of the line do not respond to faults occurring behind them. The direct trip relay at Dorsey will trigger for three-phase-ground faults occurring at T1, but the one at the Forbes busbar does not operate for faults occurring at T4.

A summary of the performance of the settings-modified GE relay on the future series-compensated Dorsey-Forbes-Chisago line will be shown in Chapter 6.

CHAPTER 5

MICROMHO SCHEME RELAY ON DORSEY-FORBES-CHISAGO LINE

5.1 Mechanism of the Micromho scheme relay:

The micromho distance-protection scheme is designed for high speed protection on high-voltage transmission systems over a very wide range of system parameters with a three zone protection scheme. It provides good security on power line protection by using a memory register and cross-polarizing scheme [10].

High speed and high security are the goals of relay design. Unfortunately, the faster the operating speed, the greater the possibility of false operation due to noisy relay input signals. The noisy input could be caused by lightning impulses, switching surges, travelling waves, harmonic components, or exponential decays [11].

The micromho scheme employs a comparator that automatically tests the purity of the input signals. If the power system frequency waveform dominates the comparator input, high speed operation will be achieved. Otherwise, more data are required by the comparator to prevent maloperation. In this scheme, a sequence of filtering and pre-conditioning processes are employed to enable the full-speed operation of the relay.

5.1.1 The Comparator:

The micromho scheme employs a comparator which uses a different tripping and counting logic scheme from the conventional block average phase comparator. In order to emphasize only the tripping scheme, conventional block average phase comparator inputs will be used for explanation before cross-polarizing is introduced in a later section.

The block average phase comparator inputs V-IZ and V$\angle$-90 are shown in Fig. 5.1. The condition for operation in the micromho scheme is that the V-IZ vector lags V$\angle$-90 vector by 0 to 180 degrees [10].

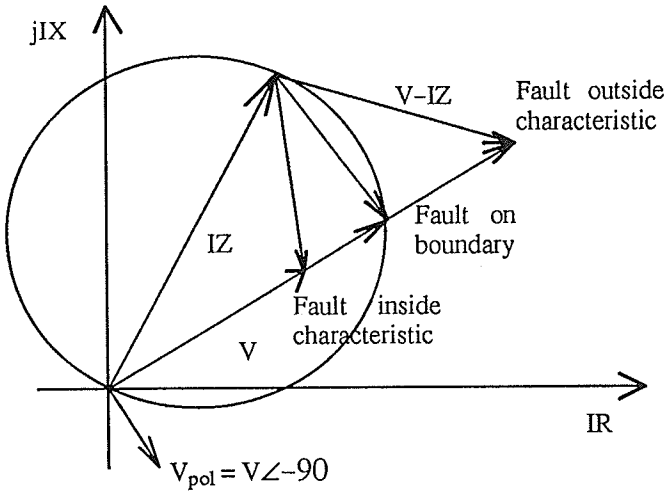
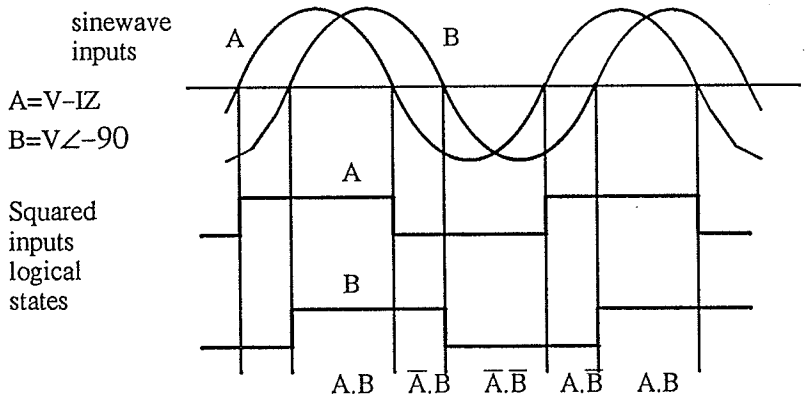


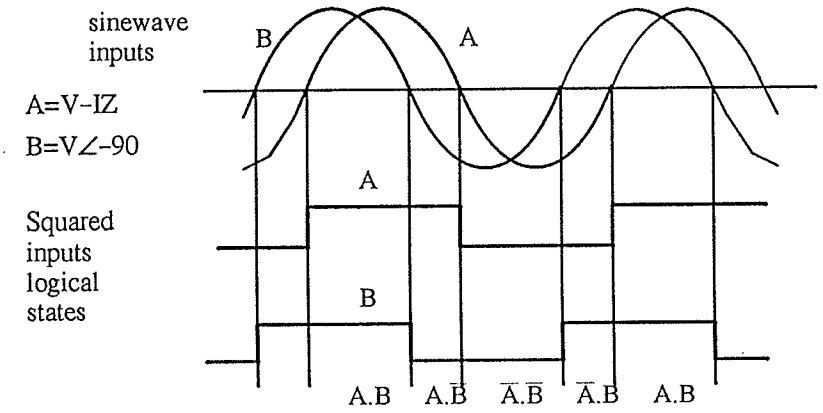
Figure 5.1 Sequence comparator voltages for mho characteristics

The quantities V–IZ and V∠–90 are first changed to square waves which only carry phase information. They are then fed into the micromho scheme comparator. The comparator utilizes a logic state scheme that assigns a high or low state for the square input waveforms. In this section, signal A represents V–IZ, and signal B represents V∠–90. In the comparator, signal A exists as high state A or low state $\overline{A}$, the same rule is applied for signal B. Fig. 5.2 illustrates the comparator logic variables in restraint and operate situations [11].



a) restrain condition

In normal operating situations, a sequence of input logic variables such as A.B, $\overline{A}$.B, $\overline{A}.\overline{B}$, A.$\overline{B}$, A.B appears. This means signal A leads signal B by 0 to 180 degrees. When signal A changes its state, a signal B of the opposite state will appear. On the other hand, when signal B changes its state, a signal A of the same state will appear.



b) operate condition

Figure 5.2 Comparator logic variables: a) restrain condition; b) operate condition.

In a faulted situation, if a sequence of input logic variables such as $A.B, A.\overline{B}, \overline{A}.\overline{B}, \overline{A}.B, A.B$ appears, this means signal A lags signal B by 0 to 180 degrees. This can also be interpreted as when signal A changes its state, signal B will appear with the same state. On the other hand, when signal B changes its state, it will experience the state opposite of signal A.

The comparator uses the above algorithm to determine whether it is in a restrain or operate state. Since noise can be carried by the input signals, the comparator uses a security scheme to detect whether the logic state of each signal carries high frequency components in a certain period of time. That means a second tripping state will not be invoked if the time between two operate states is within a certain value.

5.1.2 Counter action:

The micromho scheme comparator uses a counter that can only count up to four. A valid change that indicates an operate condition will increment the counter, while any change that indicates a restrain condition will decrement the counter which has a lowest level of zero. For clean input signals, the comparator will signal a trip to the circuit breaker when the counter reaches 2. When noise is detected, the trip count will automatically be set to 3 or 4 for secu-

rity of the system. The operation of the counter for a typical fault condition is shown in Fig. 5.3 where there is no noise component in the input waveforms [10].

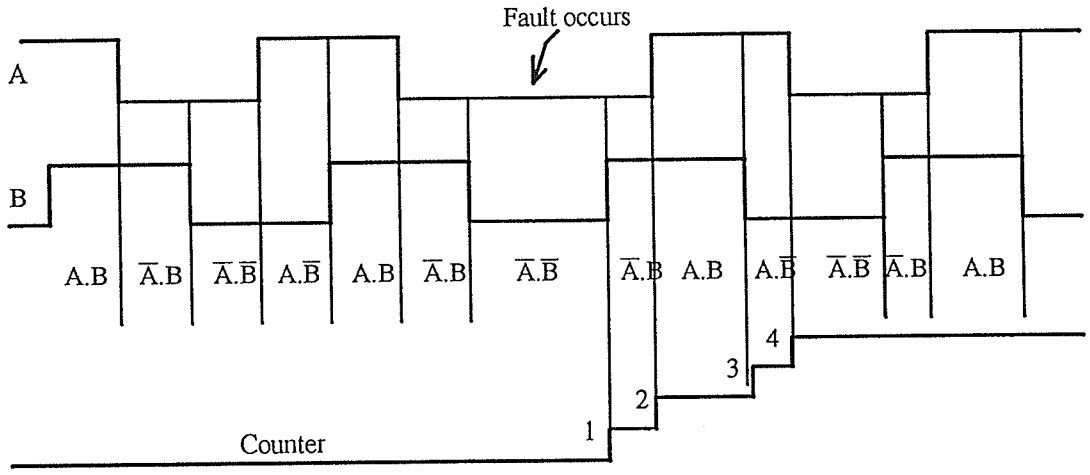


Figure 5.3 Comparator counter

A timing circuit is used to restrict the rate of counting-up in case of noisy input signals. When a tripping signal is received, the timer will start to run for 4 ms [10]. If a second tripping occurs while the timer is running, the timer is restarted and the counter will not increment. Within this period, each change of state that matches the restraint sequence decrements the counter and terminates the running of the timer, and there is no timing restriction on counting down. A restrain sequence occurring after the counter has been incremented to one (or more) implies that there is noise in the signals. In order to provide security against maltripping, the criterion for tripping is changed from a count of two to a count of three. The count-of-three criterion will be retained for 120 ms [10], an arbitrary time selected to enable any high-frequency transients to decay before restoring the normal count-of-two criterion.

5.1.3 Synchronous polarization circuit:

Up to now, the relay described has employed self polarized inputs. The actual micromho scheme uses partial synchronous polarizing and partial cross-polarizing components. The polarizing components are used because a correct polarizing (or directional reference) signal can still be obtained under all types of close-up faults. Also, fast operation can

be achieved under close-up faults. Moreover, under ground faults, where the resistance in the faulted path may be large, an expansion of the resistive coverage of the mho characteristic can be obtained [10].

The polarizing components are square wave signals of amplitude 16% of the peak prefault sinusoidal voltage supply [10]. This proportion can overcome the effect of normal CVT transients under unbalanced fault conditions. It can also work against the CVT errors in a similar way under balanced faults. The result of synchronous polarization on waveforms is shown in Fig. 5.4 [11].

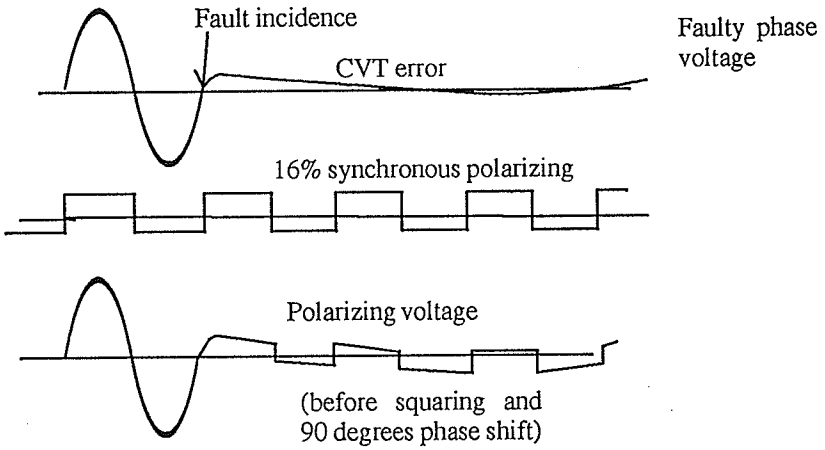


Figure 5.4 Action of synchronous polarizing

The synchronous polarizing circuit consists of a shift register with a time delay of 16 cycles for a three-phase fault. The register is operated by a clock-pulse generator, so that the system can operate correctly, irrespective of changing power system frequency in faulted situations. A single shift register is used to obtain synchronous polarization signals for all phases of the comparator by using tapping points V_{MA}, V_{MB}, V_{MC} at different locations as shown in Fig. 5.5 [11].

The input voltages V_A, V_B, V_C are filtered, squared, and then processed to obtain three nominally co-phasal signals under healthy live-line conditions. V_B is inverted and phase-retarded by 60 degrees, and V_C is phase retarded by 120 degrees [10]. A special logic

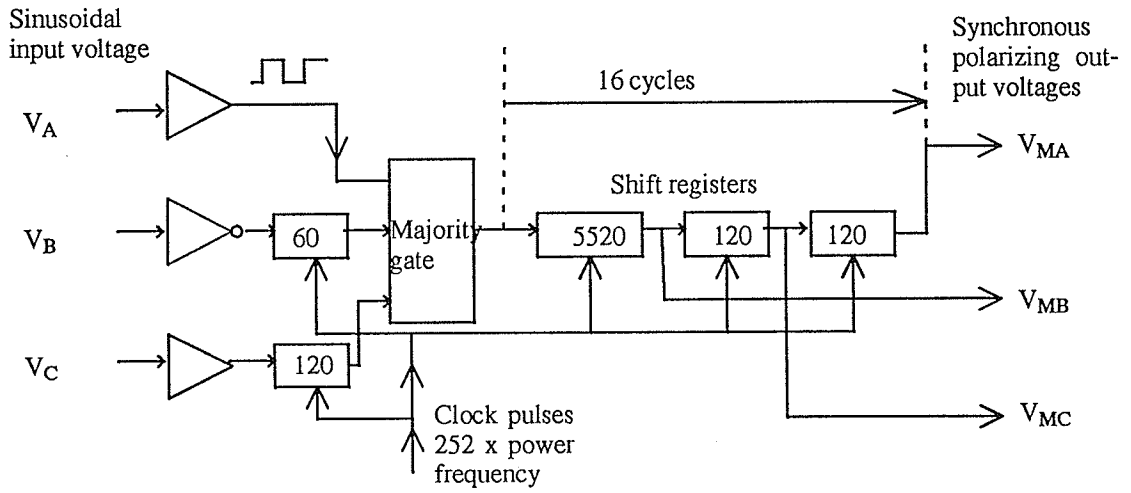


Figure 5.5 Synchronous polarizing

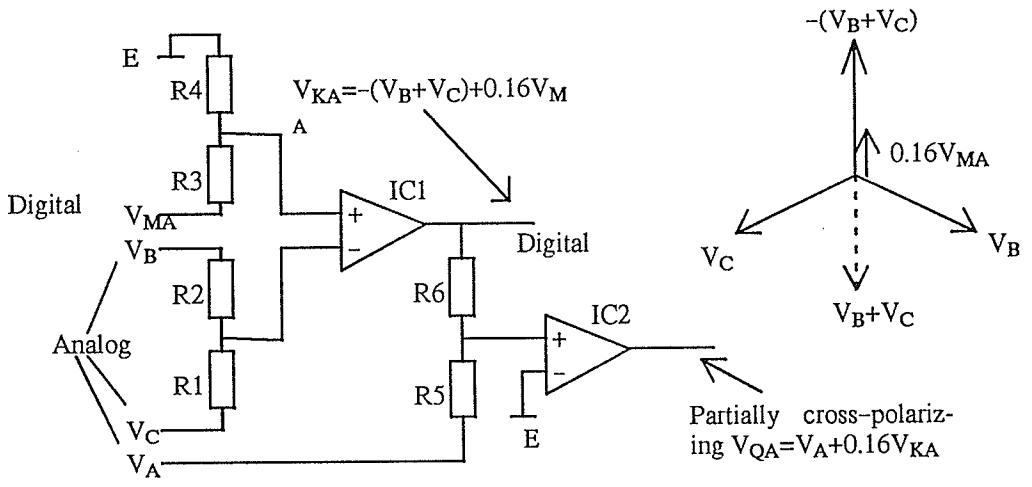
gate continuously makes a majority decision on the instantaneous logic states of the three nominal co-phasal signals, and supplies the result to the input of the main register.

The memory length of 16 cycles for three-phase close-up faults is long enough for other protection to clear a fault behind the relaying point. It also allows the relay to trip on a close-up fault in the forward direction of the relay.

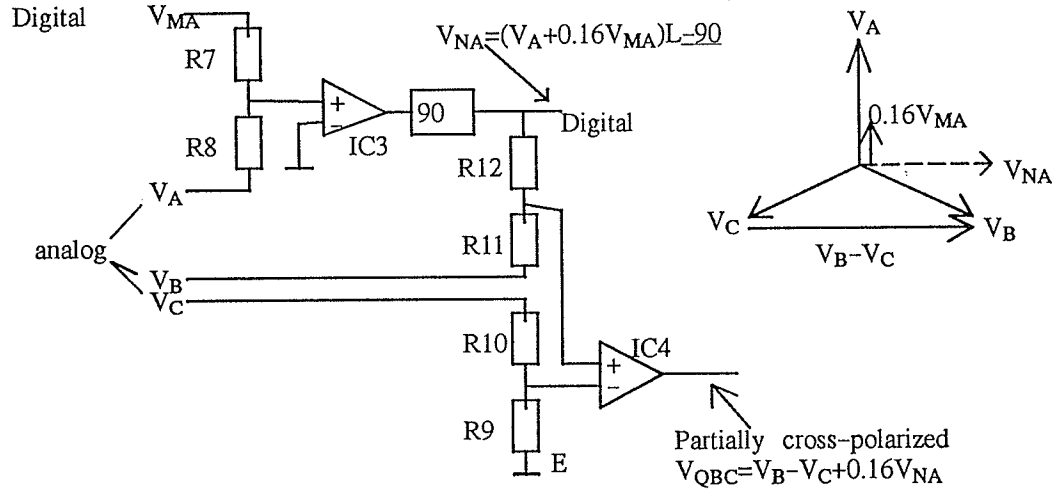
5.1.4 Polarizing mixing circuits:

The polarizing mixing circuits are specially designed for conditions where the phase-ground voltages are reduced when a close-in three-phase fault occurs. Fig. 5.6 shows a single-line-to-ground polarizing mixing circuit and a phase-to-phase polarizing mixing circuit [10].

The polarizing quantity is formed by squaring and summing circuits supplied with up to three phase-ground voltages and the relevant synchronous polarizing signal. In the single-line-to-ground polarizing mixing circuit, the square-wave synchronous polarizing voltage V_{MA} is mixed with sine-waves V_B and V_C on resistors R3, R4, R2 and R1. The values of these resistors are selected so that, under healthy voltage supplies, the peak value of V_{MA} has 16% of the effect of the peak value of $-(V_B+V_C)$ at the input of IC1 [11]. A pair of resistors R6 and R5 are used to proportionally mix V_{KA} and V_A so that the peak value of



a) A–E circuit



b) B–C circuit

Figure 5.6 Polarizing mixing circuits: a) A–E circuit; b) B–C circuit

V_{KA} corresponds to 16% [11] of the peak value of V_A at the input of squaring amplifier IC2. Then the squared output V_{QA} is phase shifted 90 degrees by a shift register (not shown in diagram), and the resultant signal is supplied to the comparator. The phase of V_{QA} is dominated by input V_A over all types of faults except earth fault conditions involving phase A, and three-phase faults which cause the voltage to collapse. For these described conditions, V_{KA} which mainly consists of -(V_B+V_C) will dominate the V_{QA}. If V_A collapses to less than 16% [11] of rated voltage, it will no longer dominate V_{QA}. In this case, the comparator effectively becomes fully cross-polarized. The resistive expansion of the characteristic for low-

voltage ground faults is therefore much stronger than for a conventional partially cross-polarized mho relay [11].

In the phase-to-phase polarizing mixing circuit, the square-wave synchronous polarizing voltage V_{MA} is mixed with the sine-wave V_A on resistors R7 and R8. The values of these resistors are selected so that, under a state of healthy supply voltage, the peak value of V_{MA} has 16% of the effect of the peak value of V_A at the input of the amplifier IC3. The resultant square-wave at the output of IC3 is phase-retarded by 90 degrees using a shift register to produce a square wave V_{NA}. A set of resistors R9, R10, R11, R12 are used to proportionally mix V_{NA}, V_B and V_C so that the peak value of V_{NA} corresponds to 16% of the peak value of V_B–V_C at the input of squaring amplifier IC4. The output V_{QBC} of IC4 is phase-shifted through a lagging angle of 90 degrees by a shift register (not shown in the diagram) and is then supplied to the comparator. The phase of V_{QBC} is determined largely by the zero crossings of V_B–V_C under all types of fault conditions except B-C, B-C-ground and three-phase faults which cause the B-C voltage to collapse when the V_{NA} signal takes control. If V_B–V_C falls below 16% of normal, V_{NA} alone dictates the phase of the polarizing signal, V_{NA} in turn being controlled by V_A if this fault involves the B-C or B-C-ground phase only, or by V_{MA} if the fault involves all three phases. Therefore, if V_B–V_C collapses below 16%, the B-C unit is effectively fully cross-polarized, and consequently the resistive expansion of the impedance characteristic is greater than for a conventional partially cross-polarized relay. Furthermore, the resistive expansion also applies to three-phase faults [11].

5.1.5 Level detectors:

In situations where a transmission line is deenergized, the voltage transformers can supply one input terminal of the comparators with low frequency transient voltage waveforms, especially if electromagnetic transformers are connected to the isolated line. A line current level detector is provided to avoid the risk of false operation of the relay comparators caused by the continuing presence of the synchronous polarizing on the other input of the

comparators. These line current level detectors have a very fast response and are connected as in Fig. 5.7 to block the comparator operation when the line is de-energized [10].

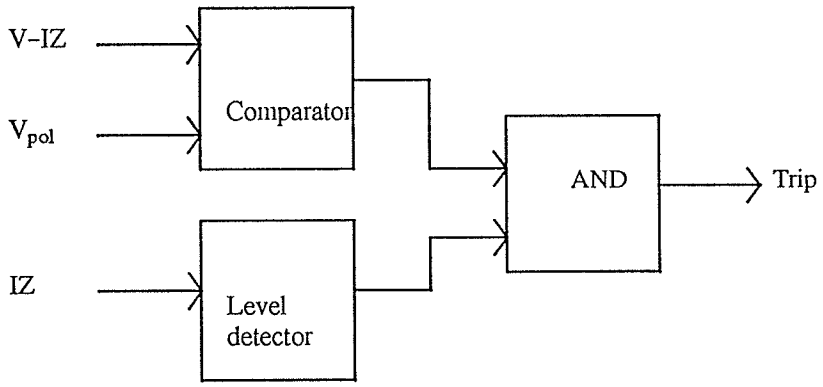


Figure 5.7 Control of level detector on comparator

Fig. 5.8 [10] explains the operating principle of a current level detector. If the instantaneous amplitude of the input voltage exceeds a threshold setting V, either on a positive half-cycle or on an inverted negative half-cycle, a timer t_1 is started. If t_1 finishes before the non-inverted input signal has dropped below V, the input sine wave is known to be greater than the level-detector setting, and the output bistable is set. At the moment the output is set, a second timer t_2 is started. This timer connects the operation between the positive and negative half-cycles. When t_2 is running, the output cannot reset. If the input voltage exceeds the threshold voltage V in the next half-cycle before t_2 finishes running, t_1 will start running to keep the output bistable set. If the voltage fails to exceed V even after t_2 finishes, the output bistable will be reset. The level detector also detect the DC offset of the input voltage. A large DC offset component will reset the bistable after t_1 and t_2 timers finish running. Furthermore, positive feedback gives a reset/operate ratio of 0.95, to prevent chatter when the input signal is at the pick-up level [10].

The current level detectors have a low setting of 8.7% [10] of rated current at the relay reference setting which restricts the operating range of the relay to a reasonable value, and the operating time of the level detector circuit is fast enough to block the fastest trip operation of the relay.

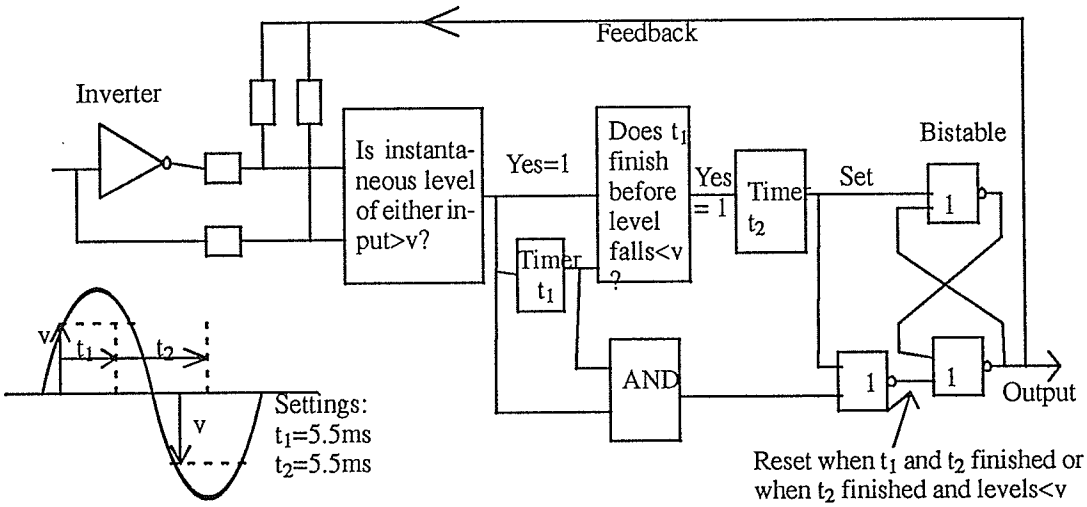


Figure 5.8 Level detector logic state diagram

Voltage level detectors are also used with 70% [10] of rated voltage setting to combine with the current level detectors on a similar operating principle. When the transmission line is deenergized, the voltage and current level detector of the deenergized poles reset to produce a 'pole-dead' signal to the 'inhibit' terminals of the relevant comparators, as shown in Fig. 5.9 [10]. In this situation, this terminal causes the counter of the comparator to decrement for any change in the state of input A or B.

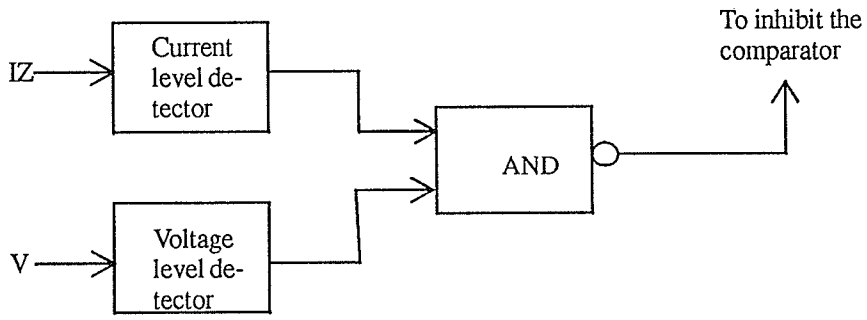


Figure 5.9 Pole dead inhibition on comparator

5.2 Performance of the Micromho relay on the new system:

5.2.1 Circular operating characteristic:

A pilot tripping scheme will be used on the micromho relay to protect zone1 of the series compensated transmission line system. The pilot tripping scheme consists of two micromho relays, a zone1 micromho relay and a zone2 micromho relay at Dorsey, and the other two at Forbes. Each micromho relay consists of six comparators. Three comparators detect single-line-ground faults on three separate phases, the other three comparators detect phase A-B, B-C, C-A phase-phase faults. The two zone1 relays can initiate a local trip, and the two zone2 relays are connected by a communication link to provide pilot tripping. Since three-pole-tripping is assumed in this thesis, any one of six Dorsey zone2 comparators can transmit a pilot tripping signal to the remote Forbes end zone2 relay with a nominal communication delay of 20ms. In the case when any one of the six remote end zone2 comparators operates, a signal will be sent to open the circuit breaker. This pilot tripping scheme is shown in Fig. 5.10.

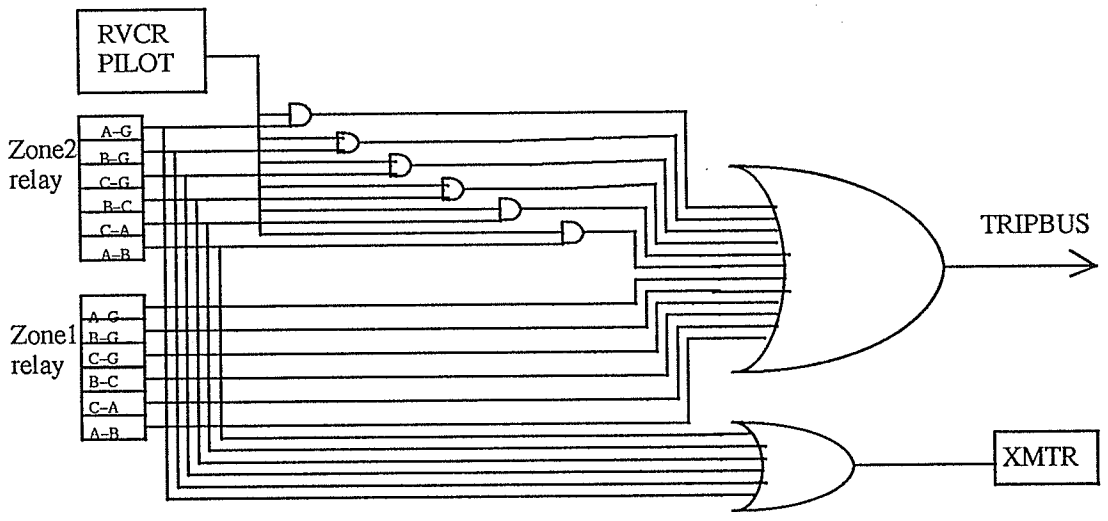


Figure 5.10 Micromho pilot tripping scheme

The micromho pilot tripping scheme is tested on the Dorsey-Forbes-Chisago 500kV line with two distinctive load flow conditions states as below:

1. Regular operating set with series compensation, maximum line current, shunt capacitor at Forbes, 1500MW delivered from Dorsey sources, 1860 MVA

2. Minimum line current operating set without series compensation, approximately 20MW delivered from Dorsey sources, 930 MVA

The first system is shown in Fig. 5.11. This will be the everyday operating set of the future series compensated line, and it delivers maximum line current in order to transfer maximum power available.

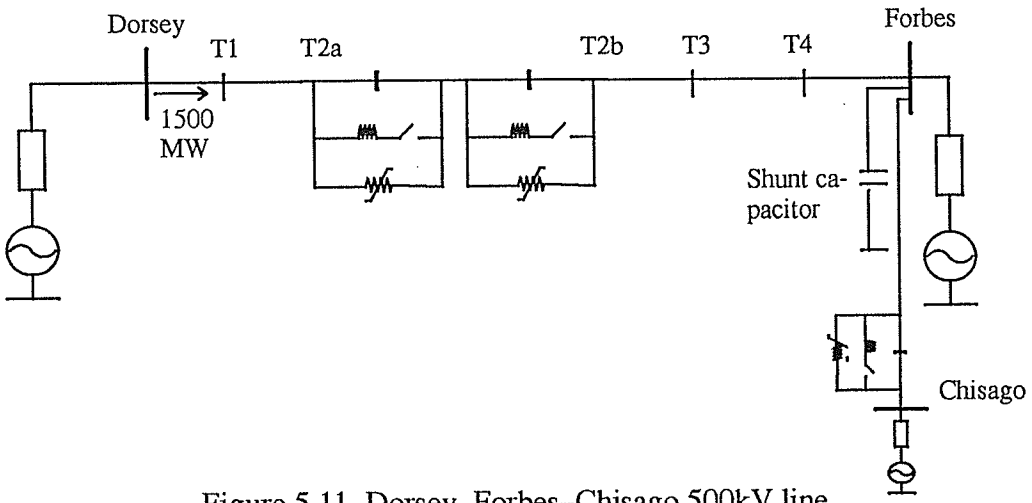


Figure 5.11 Dorsey–Forbes–Chisago 500kV line

The zone1 relays are set in such a way that they should not operate on any faults occurring on the remote end busbar and beyond. This can be achieved easily on an uncompensated transmission line. With series capacitor banks on the line, the capacitor brings a fault location much closer than it should be on a distance basis. This can be understood by looking at the impedance trajectories for the 1–cycle Fourier based relay at Dorsey for three–phase–ground faults at T3 and Forbes busbar which are shown in Fig. 5.12.

It is obvious that no mho circle can be found to cover only the final settling point of the impedance trajectory for the fault at T3 and also exclude the final settling point for the fault at Forbes since they are so close to each other. As a result, the mho circle can only cover

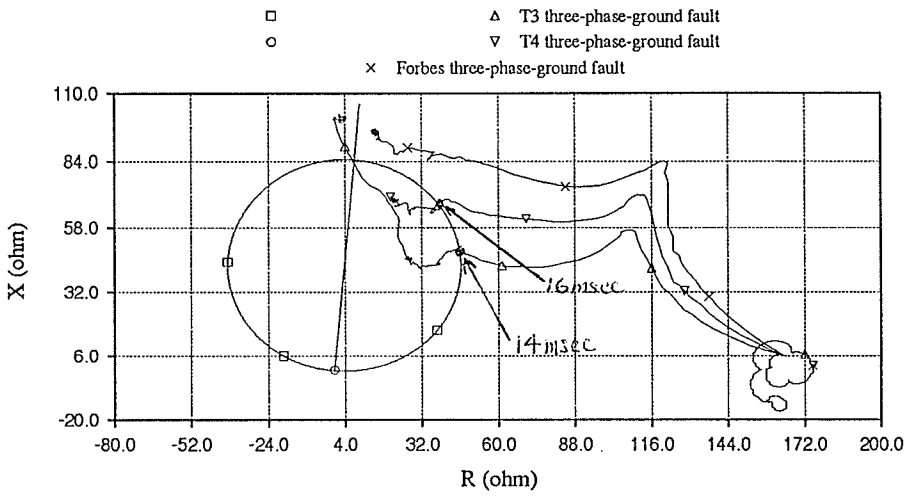


Figure 5.12 Impedance trajectories

part of the impedance trajectory for a three–phase–ground fault at T3. The impedance trajectory for the T3 three–phase–ground fault shows a low reactance before it goes into the mho circle, then an increase of line reactance is induced by the action of the MOV and the eventual closure of the bypass switch. Finally, it settles above the mho circle with reactance corresponding to the line reactance between Dorsey and T3. This means that the relay reach setting for a zone1 relay has to be restricted to a certain level to avoid maloperation over zone2 fault conditions.

The micromho pilot tripping scheme is similar to the directional comparison scheme used by the GE Relay, except it does not have the direct tripping overcurrent scheme. The zone1 relay at Forbes is set in such a way that it will mainly cover regions T4–Forbes and 100 km beyond T2a, any excess reach expansion will lead to maloperation on faults behind the Dorsey busbar. The zone1 relay at Dorsey is set to cover regions Dorsey–T2a and T2b–T4. The zone2 pilot tripping scheme provides fast and reliable protection to the system, especially for the second load flow situation where there is no series compensation.

In the past, single–pole–tripping has never occurred on the Dorsey–Forbes–Chisago line, and three–pole–tripping is assumed in the micromho pilot tripping scheme. The per-

formance of this tripping scheme on three-phase-ground, single-line-ground, phase-phase, phase-phase-ground faults at different locations on the line are shown in Tables 5.1, 5.2, 5.3 and 5.4.

Table 5.1 Three-phase-ground faults

	Dorsey local trip (msec)	Forbes local trip (msec)	Pilot trip (msec)
Dorsey busbar	8.73	-----	25.29
T1	11.77	-----	30.45
T2a	20.37	25.86	33.43
T2b	25.60	-----	35.28
T3	26.85	58.47	33.56
T4	32.28	14.49	31.38
Forbes busbar	-----	14.15	34.22

Table 5.2 Single-line-ground faults

	Dorsey local trip (msec)	Forbes local trip (msec)	Pilot trip (msec)
Dorsey busbar	8.73		28.73
T1	8.80	-----	28.80
T2a	22.69	32.67	33.29
T2b	31.15	-----	42.75
T3	39.42	-----	32.96
T4	-----	13.10	29.00
Forbes busbar	-----	14.02	34.09

Table 5.3 Phase-to-phase faults

	Dorsey local trip (msec)	Forbes local trip (msec)	Pilot trip (msec)
Dorsey busbar	10.52	-----	27.21
T1	10.25	-----	30.52
T2a	24.87	28.11	36.73
T2b	28.24	-----	37.59
T3	29.70	-----	38.59
T4	35.12	15.74	33.16
Forbes busbar	-----	21.23	33.56

Table 5.4 Phase-phase-ground faults

	Dorsey local trip (msec)	Forbes local trip (msec)	Pilot trip (msec)
Dorsey busbar	10.52	-----	27.21
T1	10.25	-----	28.80
T2a	22.69	38.16	33.49
T2b	28.24	-----	34.09
T3	28.18	32.67	33.23
T4	33.73	15.74	30.25
Forbes busbar	-----	15.74	30.25

5.2.2 Quadrilateral operating characteristic:

In single-line-ground faults involving large resistance, the normal zone1 mho circle usually takes more time to detect the fault, or it can even miss the fault completely. The quadrilateral protection characteristic provides a larger adjustable resistance reach which provides more reliability and faster operation. Unfortunately, there are some constraints to the usage of the quadrilateral protection characteristic for relaying on the compensated Dorsey-

Forbes–Chisago line. Fig. 5.13 shows the impedance trajectories for three-phase-ground fault at T2a and Forbes respectively.

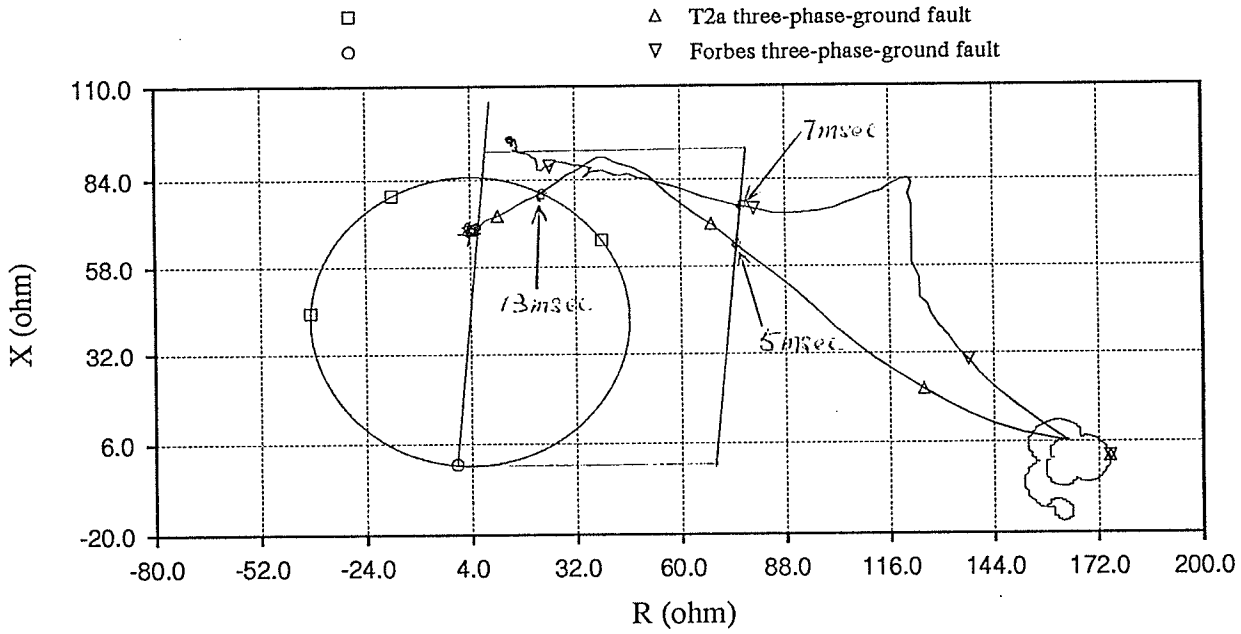


Figure 5.13 Impedance Trajectories

A quadrilateral protection characteristic that covers the whole impedance trajectory for a fault at T2a also covers the impedance trajectory for a fault at Forbes. As a result, this will force a reduction of inductance reach in order to avoid maloperation on the fault at Forbes. However, the quadrilateral characteristic will miss the T2a fault if a reduction of inductance reach is imposed. As a result, the zone1 relay will not cover up to T2a, and the task is taken by the Forbes zone1 relay and pilot tripping elements which take more time to operate. Thus, quadrilateral protection characteristic will not be seriously considered for protection of the Dorsey–Forbes–Chisago line.

5.2.3 Adaptive protection scheme:

The term 'adaptive protection' refers to the ability of the protection system to automatically alter its operating parameters in response to changing network conditions to maintain optimal performance. The criterion uses a large mho circle if the MOV conducts heavy current, otherwise the original, smaller, mho circle stays in operation. Fig. 5.14 illustrates such a scheme. For a fault that involves very limited MOV action, an original mho circle is

employed since the impedance trajectory comes straight into the mho tripping region soon after the fault.

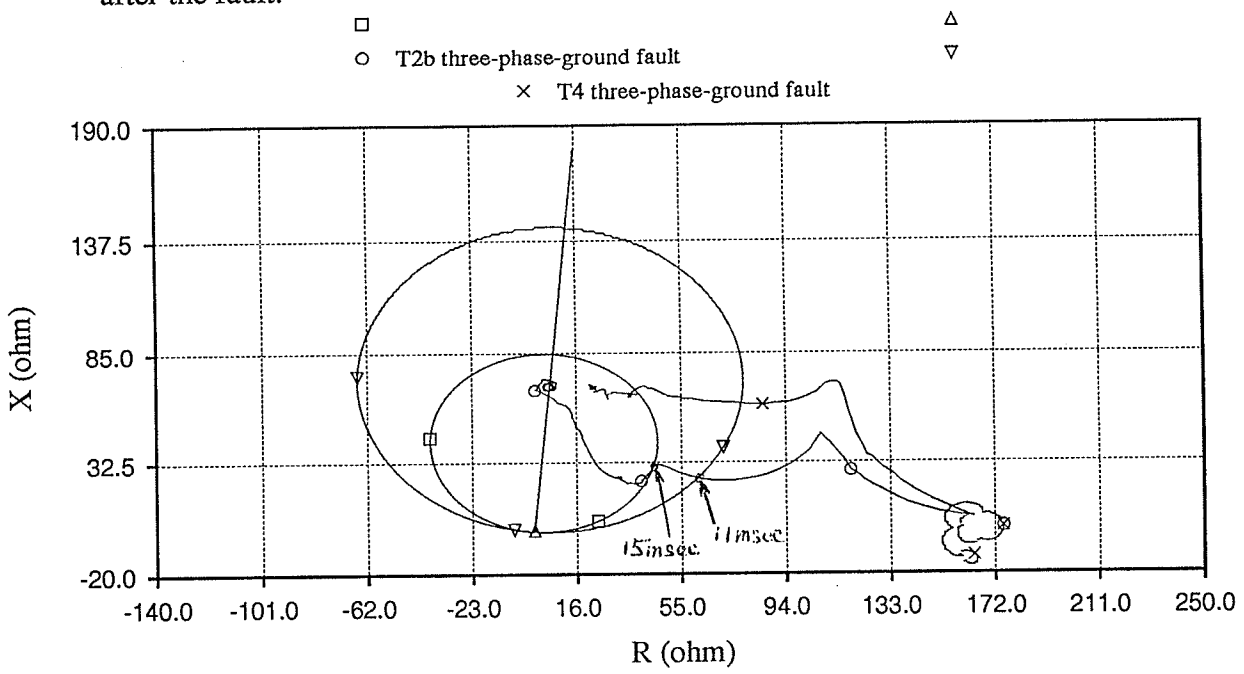


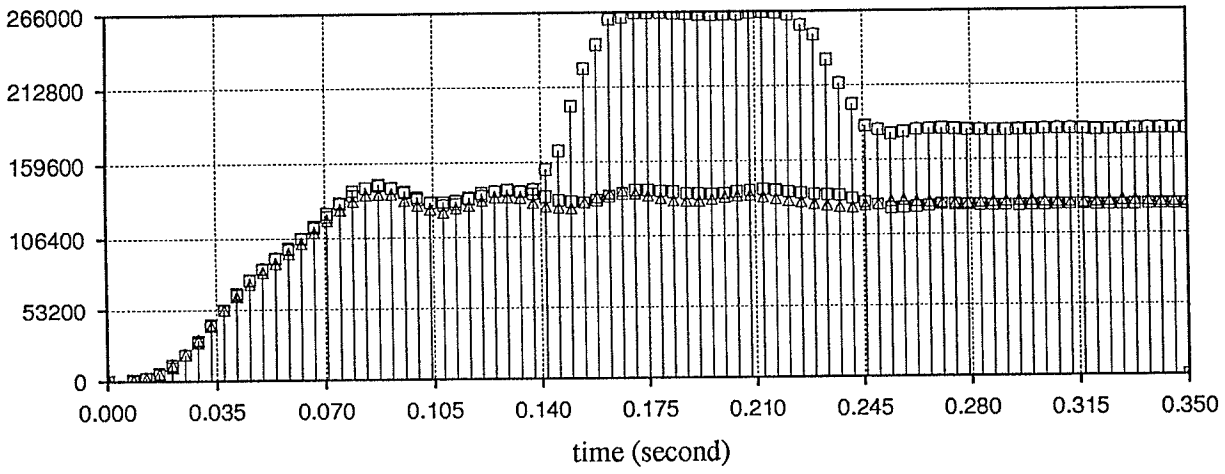
Figure 5.14 Impedance Trajectories

On the other hand, for a fault involving the MOV, the impedance trajectory hesitates around the boundary before it reaches the tripping circle. This means a slower tripping time. In this case, a larger mho circle is used to provide faster operation for the relay.

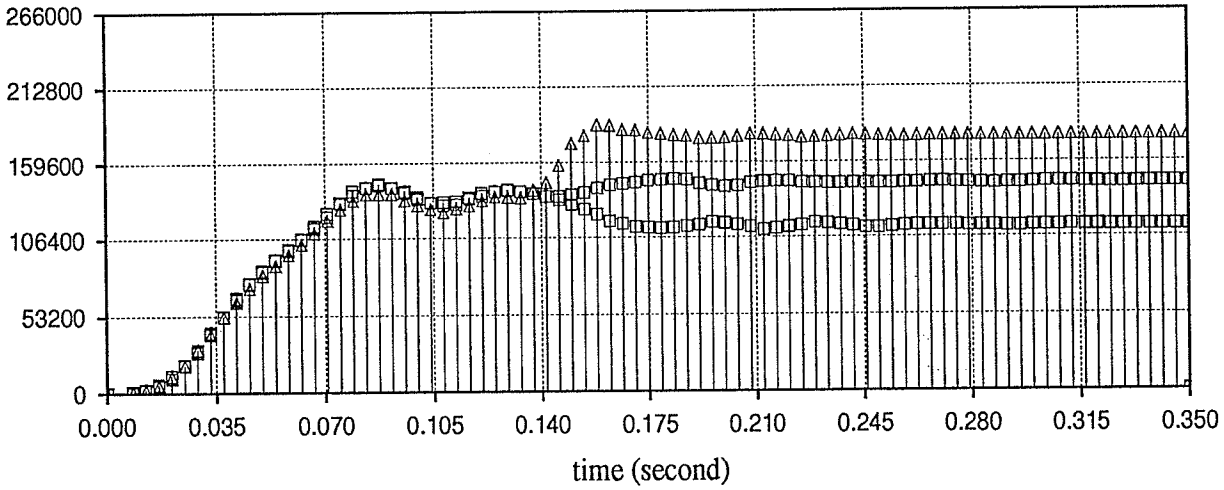
In order to determine whether the MOV is conducting heavy current, a DFT is performed to extract the magnitude of the fundamental of the line current measured at the Dorsey end busbar. Then analyses are done to find out if there are any distinct characteristics between fundamental currents in situations with and without heavy MOV operation at different locations for different types of faults.

Fig. 5.15 shows the magnitude of the fundamental of the Dorsey end line current for single-line ground faults occurring (at t=0.1295 second) respectively at T2b and T4. For a single-line-ground at T2b, the fundamental of the line current of the faulted phase increases to a certain level (>200 kunits where 1 unit = 130 A) after the fault while the fundamental of the line current of the faulted phase for a single-line-ground at T4 never passes 200 kunits.

This is one of the criteria used to form the adaptive protection scheme.



a) T2b



b) T4

Figure 5.15 Amplitudes of the fundamentals of line currents

A set of adaptive protection schemes is produced and simulated. Simulation shows that adaptive protection only improves the tripping time by less than half a cycle for most cases. This is due to the time delay caused by the DFT which leads to a 20ms time period before the characteristic of the fundamental of the line current can be distinguished. This can be seen in Fig. 5.15. The fundamental of line current for a fault at T2b does not pass 200 ku-nits until 20ms after the fault. Also, the adaptive protection scheme is produced by analyzing

the fundamentals of the line currents at one prefault load flow condition. The scheme is so sensitive that any changes on the source impedances will lead to maloperation. Actually this can be avoided if the measurement of the source impedances are included in the adaptive protection scheme.

CHAPTER 6

COMPARISON BETWEEN THE MICROMHO AND SETTINGS-MODIFIED GE RELAY ON THE FUTURE TRANSMISSION LINE SYSTEM

In previous chapters, the mechanism and performance of the GE relay and the micromho relay have been introduced. In this chapter, a comparison between the performance of the GE relay and the micromho relay on the future transmission line section will be given. The final settings of the GE relay and the micromho relay are shown in Table 6.1 and 6.2.

Table 6.1 GE relay settings

	Dorsey	Forbes
$(M_1)_1$ impedance reach	85 ohms	75 ohms
M_1T impedance reach	194.74 ohms	194.74 ohms
M_1B impedance reach	194.74 ohms (reverse) and 40.56 ohms (forward)	194.74 ohms (reserve) and 40.56 ohms (forward)
I_1T overcurrent detector	3750 A_{peak}	3850 A_{peak}
$(3I_0-KI_1)T$ overcurrent detector	2263 A_{peak}	800 A_{peak}

Table 6.2 Micromho relay settings

	Dorsey	Forbes
Zone1 L-G imped. reach	85 ohms	75 ohms
Zone1 L-L imped. reach	85 ohms	75 ohms
Zone2 L-G imped. reach	194.74 ohms	194.74 ohms
Zone2 L-L imped. reach	194.74 ohms	194.74 ohms

The performance of the GE relay and the micromho relay on the future everyday operating system, which involves maximum line currents, are compared. The DFT in the simulated GE relay provides a filtering effect that is different from that provided by the actual GE

relay. In fact, the trip time for the simulated relay is at least 10 msec faster than the actual GE relay. In this section, emphasis is put on the earliest tripbus produced at either end of the Dorsey–Forbes line section. Table 6.3 shows the performance of the two relaying systems on three-phase-ground faults at different locations on the Dorsey–Forbes line section.

Table 6.3 Trip time for relays on three-phase-ground faults

	GE relay	Micromho relay
Dorsey busbar	8.33 msec	8.73 msec
T1	9.85 msec	11.77msec
T2a	13.89 msec	20.37 msec
T2b	13.29 msec	25.60 msec
T3	15.74 msec	26.85 msec
T4	18.78 msec	14.49 msec
Forbes busbar	14.48 msec	14.15 msec

For three-phase-ground faults, the times taken for producing a tripbus for the GE relay and the micromho relay are very close, except at fault locations T2a, T2b and T3 at which the GE relay is approximately 0.5 cycle quicker than the micromho relay. At most fault locations, except T4 and Forbes, the I_1T high set overcurrent level detector in the GE relay signals the TRIPBUS. For faults at T4 and Forbes, the TRIPBUS generation time for the positive sequence directional comparison scheme is coincident with that for the direct tripping scheme.

Table 6.4 shows the performance of the two relaying systems on single-line-ground faults at different locations on the Dorsey–Forbes line section.

Table 6.4 Trip time for relays on single-line-ground faults

	GE relay	Micromho relay
Dorsey busbar	12.37 msec	8.73 msec
T1	20.90 msec	8.80 msec
T2a	20.63 msec	22.69 msec

T2b	19.97 msec	31.15 msec
T3	20.30 msec	39.42 msec
T4	15.41 msec	13.10 msec
Forbes busbar	7.74 msec	14.02 msec

For single-line-ground faults, the times taken for producing a tripbus for the GE relay and the micromho relay are very close, except at fault locations T2b, T3 and Forbes at which the GE relay is approximately 1-0.5 cycle quicker than the micromho relay. On the other hand, the micromho relay is approximately 0.75 cycle quicker than the GE relay for a fault at T1. The TRIPBUS signals for the GE relay are totally generated by the direct tripping scheme.

Table 6.5 shows the performance of the two relaying systems on phase-phase-ground faults at different locations on the Dorsey-Forbes line section.

Table 6.5 Trip time for relays on phase-phase-ground faults

	GE relay	Micromho relay
Dorsey busbar	8.66 msec	10.52 msec
T1	15.08 msec	10.25 msec
T2a	20.90 msec	22.69 msec
T2b	19.11 msec	28.24 msec
T3	21.82 msec	28.18 msec
T4	19.71 msec	15.74 msec
Forbes busbar	8.99 msec	15.74 msec

For phase-phase-ground faults, the times taken for producing a tripbus for the GE relay and the micromho relay are very close, except at fault locations T2b, T3 and Forbes at which the GE relay is approximately 1-0.5 cycle quicker than the micromho relay. The TRIPBUS signals for the GE relay are totally generated by the direct tripping scheme.

Table 6.6 shows the performance of the two relaying systems on phase–phase faults at different locations on the Dorsey–Forbes line section.

Table 6.6 Trip time for relays on phase–phase faults

	GE relay	Micromho relay
Dorsey busbar	13.89 msec	10.52 msec
T1	16.33 msec	10.25 msec
T2a	35.91 msec	24.87 msec
T2b	19.71 msec	28.24 msec
T3	35.65 msec	29.70 msec
T4	34.72 msec	15.74 msec
Forbes busbar	19.38 msec	21.23 msec

For phase–phase faults, the times taken for producing a tripbus for the GE relay and the micromho relay are very close, except at fault locations T2a, T3 and T4 at which the GE relay is approximately 1 cycle slower than the micromho relay. This is because the overcurrent level detector $(3I_0–KI_1)T$ was only designed for single–line–ground and interphase–ground faults. The negative sequence directional comparison scheme which involves a nominal communication delay of 20ms is responsible for the long tripping time of the GE relay. On the other hand, the GE relay is approximately 0.5 cycle quicker than the micromho relay for the fault at T2b.

In conclusion, the settings–modified GE relay is generally better than the micromho relay on three–phase–ground, single–line–ground, and phase–phase–ground faults if the difference on filtering effect between the simulated and actual GE relay is not considered. In phase–phase faults, since the negative sequence directional comparison in the GE relay involves a pilot signal transmission delay which prolongs the operation by 20 milliseconds, the micromho relay is considerably more desirable under these circumstances.

CHAPTER 7

CONCLUSION

After studies, it is found that the existing GE relay is able to protect the future series-compensated 500 kV Dorsey-Forbes line section by adjusting the relay-settings. The GEC Micromho relaying scheme is also able to achieve the same goal. The tripping time between the real and simulated GE relays are different since the filtering effect of the DFT is different from that provided by the actual GE relay. The performance of the two relays are comparable for three-phase-ground, single-phase-ground and phase-phase-ground faults if the time delay of the unsimulated filtering system in the actual GE relay is taken into account. Otherwise, the GE relay is faster than the Micromho relay in all three cases. In the phase-phase faults, due to the pilot transmission delay in the negative sequence directional comparison scheme, the GE relay is inferior to the Micromho relay. Also, the possibility of using a quadrilateral protection zone instead of the conventional circular protection zone was looked at. Moreover, a study on an adaptive protection scheme using a DFT (Discrete Fourier Transform) was conducted. After studies, the use of the quadrilateral protection zone and the DFT adaptive protection scheme cannot be easily done efficiently.

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