Cross-sectional Imaging of Semiconductor Devices using Nanometer Scale Point Contacts

A Thesis report

written by

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submitted to the Department of Electrical and Computer Engineering

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FACULTY OF GRADUATE STUDIES

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CROSS-SECTIONAL IMAGING OF SEMICONDUCTOR DEVICES USING NANOMETER SCALE POINT CONTACTS

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JOCHONIA NORMAN NXUMALO

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree

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DOCTOR OF PHILOSOPHY

ABSTRACT

In order to study semiconductor dopant profiles a novel technique based on localized contact resistance measurements has been designed and implemented. Scanning Resistance Microscopy (SRM) is a nanometer scale technique for performing two-dimensional p-n junction delineation and carrier profiling on semiconductor surfaces. It utilizes a sharp conducting probe tip that is biased and raster scanned in contact with the sample surface while an ohmic back contact provides the circuit return path. By monitoring the current flowing across the tip-surface interface while scanning the sample beneath the probe this technique performs localized resistance measurements over a semiconductor surface. These measurements are used to delineate between regions of different doping type and magnitude with spatial high resolution (20 nm). SPM technology is used to regulate the contact force between the tip and the surface during a scan in order to attain high spatial resolution consistently.

Simulations of the junction formed between SRM tips and silicon substrates suggest that when the tip loading pressure is kept low enough ($\leq$ 5 GPa) the resistance across the junction is dominated by the **contact** resistance rather than series **spreading** resistance. Furthermore, I-V spectra taken over uniformly doped silicon substrates in contact with conducting diamond tips demonstrate that these junctions are rectifying. These results show stronger rectification when the diamond tip makes contact to p-silicon compared to n-silicon. Capacitance derivative measurements performed on the same samples also indicate a similar asymmetry. By studying the I-V spectrum and comparing with band models for a similar heterojunction used by other researchers we have proposed an energy band model that explains SRM data quite well.

In this thesis we present experimental results obtained from imaging cross-sections of a wide variety of semiconductor devices. These results demonstrate the capability of SRM to perform two-dimensional imaging on device cross-sections providing simultaneously surface topographic and resistance profiles. We also demonstrate that by using conducting diamond (instead of metal) tips the SRM spatial resolution is improved significantly and resistance profiles of MOSFET cross-sections reveal source drain extensions that are a result of the presence of lightly doped drains.

A technique for characterizing semiconductor devices in their normal operation mode has been investigated. Normal operation of a sectioned device is verified by comparing its I-V characteristics before and after sectioning. Imaging is done with a conductive tip that is attached to a high input impedance voltage sensing circuit and used to probe local surface potentials on the device cross-section. This is perhaps the most direct method of evaluating the impact of semiconductor process variation because the potential profiles reflect the activity inside the device during normal operation. Preliminary results demonstrate the ability for this technique to perform 2D surface potential mapping and hence the capability to study the behavior of MOSFET channel formation under different bias condition.

ACKNOWLEDGMENTS

Firstly, I would like to thank my advisor Professor D. J. Thomson for giving me the opportunity to do this work in the SPM laboratory. The privilege to attend conferences and presenting our research findings gave me the opportunity to establish dialog with world class researchers in the area of semiconductor dopant profiling, thanks to my advisor who made all this possible.

I thank the Canadian International Development Agency (CIDA) and my supervisor for financial support without which doing this work would have been even more challenging. I particularly thank Professor D. J. Thomson and Professor G.E. Bridges for the profound encouragement, enthusiastic assistance and infectious optimism that made my research possible and enjoyable. I also thank the technical staff, Bill Bourbonnais, Allan Mckay and Allan Symmons for their assistance in different ways during instrument design and construction. The discussions that I have had with my colleagues in the SPM group were educational and are very much appreciated.

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I want to thank my wife Yoliswa for her patience and encouragement while I was engaged to my academic work. I would also like to thank my father and mother, Mr. and Mrs. A. M. Nxumalo, as well as my brothers and sisters for their encouragement whenever necessary and the patience in awaiting my return home with my degree.

I would like to dedicate this thesis to my two girls Welile and Phesheya Nxumalo as well as my late grandmother.

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SEMICONDUCTOR IMPURITY MEASUREMENTS

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1.1 INTRODUCTION

Future development of faster semiconductor devices and their high density fabrication on integrated circuits has resulted in device dimension reduction into the deep sub-micron level. This rapid dimension reduction has prompted researchers to develop diagnostic tools that are capable of characterizing these devices with nanometer-scale lateral and depth resolution. High resolution two-dimensional (2D) dopant profiling and p-n junction delineation has been identified by SEMATECH as one of the critical diagnostic technologies that needs to be developed in order to meet the challenges presented by rapid shrinkage of IC devices **[1].** In order to calibrate process and device simulation tools the Semiconductor Industry Association (SIA) requires, as input data, sub-ten nanometer spatial resolution 2D dopant profiles from profiling instruments.

In the past semiconductor dopant profiles have been studied using several different techniques. These techniques range from those that are based on chemical reactions taking place on specimen-surfaces combined with electron microscopes, a variety of scanned probe methods that measure localized electrical properties on specimen surfaces, secondary ion mass spectroscopy (SIMS), to scanning tunneling microscopy (STM) based methods. Although active research is going on in this area, none of the techniques developed to date can provide **all** the answers to questions regarding semiconductor dopant profile measurements.

The basic requirements for diagnostic tools include wide measurement dynamic range ($10^{15} \rightarrow 10^{20}$ cm^{-3}), high accuracy (10%), none-destructive testing of specimen surfaces, non-complex sample preparation, and the ability to provide quantitative two dimensional dopant information on semiconductor surfaces. Most of the reported diagnostic tools can provide some but not all the above mentioned requirements. There are fundamental limits to each technique that are based on the type of measurement.

1.2 NATIONAL ROAD MAP TECHNOLOGY PROJECTIONS

Dynamic random access memory (DRAM) chips have been the leading edge products in semiconductor technology for a long time. Flash memory has recently emerged as a potential contender with DRAM technology and is projected to remain so for the next 10-15 years. In the last few years development of new technologies used to manufacture microprocessors has accelerated. Microprocessor products have now closed the technology gap with DRAM. Nowadays it is recognized that microprocessors and DRAM products share the technology leadership role. Technology working groups have studied the technological advancements of DRAM product manufacturing and have used DRAM production as a milestone calculation criterion for minimum feature size generation of semiconductor devices. Table 1.1 shows some projections on technological advancements based on Moore's Law and the aforementioned criterion. This table was extracted from "The Nantional Roadmap for Semiconductors, 1994" published by SEMATECH.

Year of First Product Shipment	1995	1998	2001	2004	2007	2010
minimum feature size (μm)	0.35	0.25	0.18	0.13	0.10	0.07
X_j (@ channel) nm	70-150	50-120	30-80	20-60	15-45	10-30

Table 1.1 Doping Technology Requirements. (source: The National Technology Roadmap for Semiconductors, 1994).

The end of feature size reduction will be based on technological, physical and fundamental limits[2(a)].

Although Table 1.1 shows future predictions beyond the year 2000, the pace at which technology generations are being introduced has been accelerated from the 3-year cycle to an approximate two-year cycle since the publication of the 1994 Roadmap. As a result the Semiconductor Industry Association has come up with revised predictions of the time-frame for introduction of new technology generations into the market. Table 1.2, extracted from the National Technology Roadmap for Semiconductors 1997, shows some of the projections.

Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Minimum feature size (μm)	0.25	0.18	0.15	0.13	0.10	0.07	0.05
S/D Extension Junction Depth (norminal) (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20

Table 1.2 Doping Technology Requirements. (source: The National Technology Roadmap for Semiconductors, 1997).

Here, a new 0.15 μm generation has been introduced and the first year of its shipment to the market place is forecast to be 2001[2(b)]. The overall schedule for introduction of a new technology has been accelerated by one year.

Feature size reduction to a sub-micron level has made device fabrication a very delicate process because device parameters have now become critical to device performance. Ultra-shallow device junctions mandate the use of low energy dopant ion beams (<5KeV) and a careful monitoring of defects and radiation damage within these regions. SEMATECH and SIA project a minimum device feature size of 0.10 μm by the year 2006 and source/drain extension junction depth of 20 nm. This feature size reduction rate demonstrates the urgency for the need of device characterization techniques with nanometer scale spatial resolution. The current state-of-the-art in semiconductor dopant profiling and p-n junction delineation techniques will be reviewed in the following sections.

1.3 SCANNING PROBE MICROSCOPY

The advent of the Scanning Tunneling Microscope, invented by Binnig and Rohrer [3], has spawned a large variety of SPM derivatives that are being utilized in many different scientific disciplines today. The essential elements of the STM include a conducting tip that is placed in close proximity with a conductive or semiconductive sample surface. A bias voltage applied to the tip with respect to the sample causes a current to flow between the two when their separation is small enough. This current is due to quantum mechanical tunneling of carriers across the gap when mechanical point contact is not reached. Since the tunneling current varies exponentially with the separation, a 2D scan of the tip on the sample while monitoring the current produces a 2D profile of the sample surface topography. Atomic scale spatial resolution with the STM was demonstrated about 10 years ago [4].

The type of interaction force between the tip and surface depends on their separation. At large separations (>10 nm) the interaction is dominated by van der Waals forces. For separation of a few tenths of a nanometer the overlap of the wavefunctions of the tip and the sample surface is significant and short-range quantum mechanical exchange-correlation forces become dominant. For metallic tip and sample these forces appear strongly attractive. This is the STM operation regime. If the tip and sample are brought even closer, the quantum mechanical forces become repulsive as a result of the Pauli exclusion principle. The forces in the last regime have been exploited to develop another type of scanning probe microscope, the Scanning Force Microscope (originally named the Atomic Force Microscope or AFM) [5].

The AFM tip is attached to one end of a flexible cantilever while the other end is fixed to a rigid mount. The AFM tip is not necessarily conductive and is placed in contact with the sample surface. As the sample is raster scanned beneath the tip, the cantilever deflects vertically under the influence of the repulsive interaction force between the tip and the surface. A deflection sensor is utilized to monitor the vertical deflection of the cantilever thus producing a topographic profile of the surface.

A number of scanned probe techniques have been derived from the basic idea of the AFM. These derivatives utilize tips with a variety of electrical and magnetic properties. SPM tips in these techniques are used to probe local properties of the sample surface. In microelectronics, electronic properties of SPM tip-sample interaction under various bias conditions are being used to study carrier density profiles on semiconductor surfaces.

Conventional semiconductor dopant characterization methods such as SIMS [6] and Spreading Resistance Probe (SRP) [7] provide one dimensional but not two dimensional information with high spatial resolution. Other techniques such as Selective-Doping Etching and

Chemical Staining are being investigated **[8-9]**. Newer scanned probe electrical approaches such as the STM **[10]**, Scanning Capacitance Microscopy **[11]**, Nano-SRP **[12]** and Scanning Resistance Microscopy **[13]** possess the required two dimensional imaging capability as well as high spatial resolution for device characterization. However, these techniques are all still in the development stage and none have emerged as a dominant method for two dimensional dopant diagnostics.

Development of techniques for performing two-dimensional dopant profile delineation entails meeting requirements such as sensitivity and spatial resolution, complexity of the method of delineation and sample preparation prior to performing the measurement. Furthermore, it is necessary to determine whether the method is sensitive to chemical (atomic) or electrically active dopants. Methods should also be evaluated on the basis of whether they are applicable to structures commonly encountered in microelectronics, or they require special test structures.

The Semiconductor Industry Association has recognized that research is required for SPM based profiling techniques and projects that, by the year 1999, their development into commercial off-line doping characterization tools will be underway. It is hoped that by 2001 the qualification and pre-production of commercial tools based on SPM technology will occur**[2(b)]**.

1.3.1 Secondary Ion Mass Spectroscopy

In this technique the material to be analyzed is bombarded with a beam of primary ions of energy 1-10keV, resulting in the sputtering of atoms and molecules from the upper atomic layers of the sample (0.5 -5 nm in depth). Some of the sputtered particles are ejected as ions while most of them are ionized outside of the solid within a few angstroms away from its surface **[14]**. The

primary beam can be focused to achieve a lateral resolution of 1μm and trace elements can be detected to a sensitivity of 1 ppm. Secondary ions are subsequently analyzed by a mass spectrometer and the mass spectrum provides a quantitative measurement of the chemical composition of the sputtered material. Conventionally, SIMS provide a one dimensional depth profile of the dopant distribution. However, Goodwin-Johansson *et al.* **[15]** proposed a 2D SIMS technique in which primary ion beams at various angles are used to profile the unknown dopant distribution, yielding several angular projections of the dopant profile. From this data they claim that a complete 2D reconstruction of the surface dopant distribution is achieved rather than isoconcentration contours. One of the limitations of SIMS is that it is a **destructive** technique, therefore many **identical** samples are required to provide a 2D profile, a time consuming exercise. A complete 2D distribution of an implanted boron profile was measured with a sensitivity of $\approx 1\times10^{17} cm^{-3}$ and spatial resolution of 10nm **[16]**. Another 2D technique was demonstrated by Dowsett *et al.* **[17]** in which a resolution of 50nm and sensitivity of $\approx 1\times10^{14} cm^{-3}$ was obtained. SIMS methods are of great importance in dopant profiling because they are among the few known techniques for measuring chemical profiles. More work is still being done to improve the sensitivity and resolution of SIMS to meet the challenge of ultra-shallow junctions.

The Semiconductor Industry Association has recognized that development is underway for recently improved SIMS and projects that, by the year 1999, qualification and pre-production of SIMS as an off-line doping characterization tool will occur**[2(b)]**.

1.3.2 Scanning Capacitance Microscopy (SCM)

The SCM has shown great potential in direct measurement of doping profiles with nanometer scale lateral resolution. This approach is based upon the general concepts used in 1D capacitance-voltage measurements performed on semiconductor surfaces **[18]**. A small probe electrode is placed in close proximity with the surface to be studied. By assuming a parallel plate geometry of the electrode tip-surface capacitor (a first order approximation) this capacitance is inversely proportional to the spacing between the probe and surface. This dependence of the capacitance on the separation may be exploited to control the height of the probe above the surface, providing a means for non-contact imaging of conducting and non-conducting surfaces. However, in general, the capacitance depends in a complicated way on the geometry of the probe and the sample properties such as dielectric constants of the probe, the sample and the medium between them.

A number of research groups have taken the C-V measurement approach a step further in order to perform doping profiling on semiconductor surfaces. In one approach, a doped semiconductor surface is coated with a thin oxide layer and a biased metal probe tip is placed in contact with the oxide surface. This arrangement forms an MOS structure. A localized depletion region is created in the silicon beneath the tip contact point. The width of the depletion region depends on the probe bias polarity and magnitude as well as the local dopant concentration. The depletion capacitance formed by the tip-oxide-silicon structure is measured and the data is analyzed to extract dopant profiles **[12]**. The tip is then raster scanned to obtain a 2D dopant profile of the surface. A lock-in technique is employed so that the derivative of the capacitance with respect to voltage is extracted at a frequency that is high enough to avoid shot noise effects.

Uniformly and moderately doped surfaces are suitable for the SCM as described above. When applied to shallow implanted (or diffused) junctions with non-homogeneous dopant profiles the lateral resolution of the SCM changes with dopant density. To get around this problem C.C. Williams *et al* [19] have developed a closed loop technique where the tip-sample capacitance derivative is measured and compared with a reference signal. The magnitude of the bias signal is adjusted using control circuitry in order to maintain a constant capacitance derivative as the tip is scanned. A model to extract 1D profiles from the data using this scanning mechanism of the SCM has been developed.

The SCM measures carrier concentration rather than dopant concentration. The carrier density profile in heavily doped samples does not directly follow the chemical dopant profile. Therefore, the SCM is well suited for moderately doped samples. However, the presence of the oxide layer separating the tip and the sample limits the spatial resolution of the technique.

1.3.3 Selective Doping Etching and Chemical Staining

Chemical staining of doped silicon layers for the delineation of p-n junctions has been known since the early days of the semiconductor industry [20]. Generally, staining solutions plate the N-type region more than the P-type and are thus mainly useful for junction delineation. On the other hand, selective etching removes material from the sample surface at a rate that depends on the solution concentration, etching conditions as well as the dopant concentration of the surface. With all other variables maintained constant, etching non-uniformly doped surfaces leaves the surface topography with a profile that represents the surface dopant profile. Using techniques such as transmission electron microscopy (TEM), scanning electron microscopy

(SEM) or atomic force microscopy (AFM) the treated (stained or etched) surface topography is imaged and the doping profile is extracted.

Samples are beveled at a shallow angle in order to magnify the p-n junction depth. A drop of the staining solution is placed on a sample that is illuminated with high intensity ultraviolet light and left for a period less than a minute for plating to occur. The staining solution is then cleaned and the sample examined to measure the length of the stained section and then determine the P-N junction depth. Staining has also been used to perform 2D junction delineation **[16]**.

Selective-etching solutions exhibit greater dependence on surface dopant density compared to staining solutions. The former can be controlled to etch up to either the P-N junction or to selected concentration levels by changing the etching conditions. This technique has been applied to polished sample cross-sections to map out contours of dopant concentration **[21]**.

Literature reports that vertical resolution of 20 nm is routinely obtainable by both staining and etching methods using careful experimental techniques **[22]**. However, selective etching and staining are destructive techniques and labor intensive.

1.3.4 Kelvin Probe Force Microscopy

If a conductive probe tip is held close to a sample surface, the force acting on the tip consists of van der Waals force and the electrostatic force caused by the potential difference between the tip and the sample. The Contact potential difference between two materials depends on a variety of parameters such as the work function difference, adsorption layers, oxide layers, dopant concentration in semiconductors, or temperature changes on the sample. In principle, the measurement of the contact potential difference can be used to obtain information concerning

these parameters. A common method used to measure contact potential is the vibrating capacitor or Kelvin method [23].

A simplified model of the tip-sample system is a parallel plate capacitor with a small separation. In this simplified model the contact potential difference between the two materials is $V_{cp} = e^{-1}(\Phi_t - \Phi_s)$, where Φ_t and Φ_s are the effective work functions of the tip and sample respectively. The force between the capacitor plates resulting from the potential difference caused by their work function difference can be nulled by applying an equivalent potential on the tip such that V_{cp} is zero. This nulling technique forms the basis of the Scanning Kelvin Probe Microscope's ability to measure local surface potentials.

A measurement of the capacitance derivative in the z direction has been demonstrated by utilizing a heterodyne interferometer to detect a vibrating cantilever deflection with lockin amplifiers to extract topographic and surface potential profiles simultaneously **[24].** Henning *et al* **[25]** have applied the SKPM technique to the problem of profiling dopant concentrations in 2D in silicon microstructures. By measuring the electrochemical potential difference which minimizes the electrostatic force between the probe tip and sample surface, Henning *et al* were able to estimate the work function difference between the tip and the sample and doping profiles were inferred from the measurement. For these measurements, a lateral spatial resolution of less than 100 nm (at best 25 nm). This group claimed a voltage sensitivity better than 5 mV/$\sqrt{\text{Hz}}$.

Tanimoto *et al* **[26]** have also applied the Kelvin Probe technique to characterize AlGaAs/GaAs multilayer structures with thickness ranging from 40 nm to 180 nm separated by 370 nm of undoped GaAs, as well as silicon p-n junction structures. This group was able to just resolve the 40 nm AlGaAs layer with a potential of 15mV while the 180 nm layer was measured

at 60 mV. P-N junction delineation was performed successfully with contrasts between p and n regions enhanced by illuminating the surface with white light. Furthermore, Tanimoto *et al.* claimed that they were able to measure depletion layer thickness.

The Kelvin method has high sensitivity for potential measurement but integrates over a large portion of the tip area including some of the side walls. Dependence on the tip geometry of the measurement degrades the spatial resolution capability of the technique. Henning *et al.*. [25] claim that the technique is sensitive to changes in dopant concentration from 10^{15} to 10^{20} cm^{-3} of less than 10%.

1.3.5 Spreading Resistance Profiling (SRP)

Spreading Resistance Profiling is one of the longest-lived dopant density profiling techniques [28] to date and is still used in the semiconductor industry. Fundamentally, in the SRP technique two closely spaced sharp probes are placed in contact with a sample surface (see Fig. 1.1), a potential difference is applied on the probes, and the current flowing between the two probes is measured.

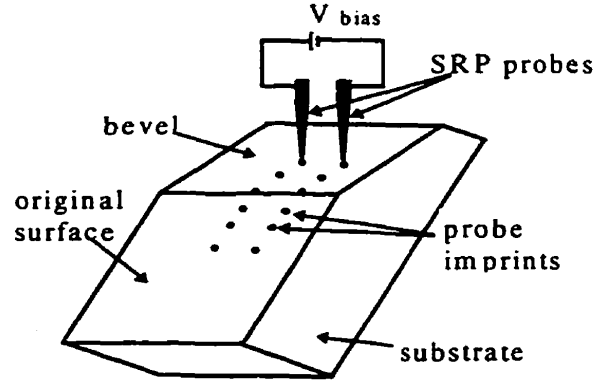


Figure 1.1 Two-probe spreading resistance measurement.

The measured current is then used to calculate the sample local **spreading resistance.** The two probes are then lifted and moved in small steps on the surface in the direction perpendicular to a line joining them (shown as probe imprints) and the current is measured at each step. The sample line dopant profile is then calculated from the expression

$$R_{sp} = \frac{\rho}{2\pi r} \qquad (1.1)$$

where ρ is the resistivity of the sample and **r** is the contact radius. Tip loads on the sample surface of 0.1 N with a contact radius of 1-10 μm have been used and the tip was found to leave imprints on the surface. About 80% of the total potential drop due to spreading resistance occurs within 5**r** **[29]**. To enhance the spatial resolution of the technique, samples are beveled at a shallow angle and spreading resistance (SR) measurements are taken on the bevel. Therefore, SRP measurements provide one-dimensional doping profiles. This technique is also destructive. Recently, there has been advancements in the SRP technique by modifying the current-voltage (I-V) characteristics (referred to as probe conditioning) of point contacts. It has been demonstrated that probe conditioning improves the SRP spatial resolution on ultra-shallow (less than 100 nm) layers **[30]**. Studies show that excessive tip pressure (above 8 GPa) on a silicon surface causes a phase transitions to a metallic state locally. In this state the contact is dominated by spreading resistance over contact resistance **[31].**

The Semiconductor Industry Association has recognized that improvement is underway for SRP probing and projects that, by the year 1999, qualification and pre-production of SRP as a off-line doping characterization tool will occur**[2(b)]**.

1.3.6 Nano-SRP

Nano-SRP is a single probe spreading resistance profiling technique that uses a biased conducting tip positioned in contact with the sample surface with a large grounded back contact to complete the circuit. Here the sample is not beveled and the tip load is reduced to the range 70μN→260μN which reduces the contact area [12].

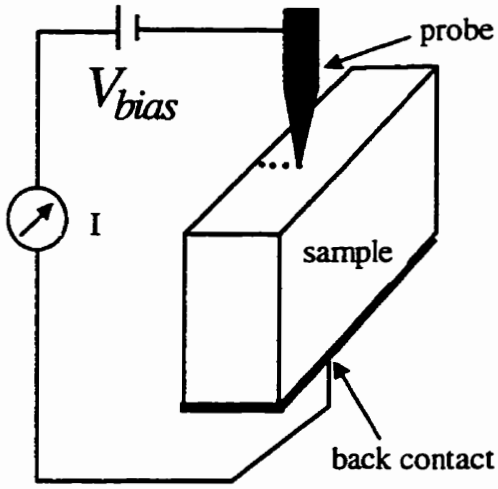


Figure 1.2 Schematic drawing for Nano-Spreading Resistance Probing System

Utilizing a single probe allows smaller tip step sizes when taking data and hence higher spatial resolution is achieved. The tip load applied in nano-SRP measurements is set high enough so that the tip breaks through the native oxide layer and establishes a good electrical contact with the silicon. The imprints that remain after removal of the tip have been studied on polished uniformly doped samples. The pressure from these micro-contacts causes silicon to undergo a phase transition from silicon to a metallic β-tin phase [31]. In [31], it has been shown that the

interface between β-tin phase and normal silicon behaves as an ohmic contact. Although this is a good contact for performing spreading resistance measurements, it is not possible to perform these measurements at identical tip locations more than once. While this technique is gaining popularity in the SRP community because of its high sensitivity and dynamic range and the ease by which doping profiles are extracted from resistance measurements, the technique still suffers from its destructive nature. Nano-SRP can provide 2D doping profiles.

1.3.7 Metal-Semiconductor C-V Measurements

Recently, we have developed a technique based on the measurement of the Schottky contact capacitance for performing p-n junction delineation and carrier profiling. This technique is based on the measurement of the Schottky contact capacitance that is formed at the interface of a metal-semiconductor junction **[32]**. Literature shows that in the past extensive research has been done on Schottky contact capacitance**[33]**. Williams *et al.*. **[11]** and other semiconductor research groups are actively using capacitance measurement techniques to study carrier profiles in semiconductors using metal-oxide-semiconductor (MOS) structures.

Schottky capacitance-voltage measurements are performed with a sharp conductive tip that is held in contact with a sample surface, an ac bias potential applied to the sample, and using a capacitance sensor and lockin amplifier the voltage derivative of the contact capacitance is measured. A theoretical relationship between the capacitance derivative and the local dopant concentration in the sample is given by equation (1.2). Experimental results show that this technique is sensitive to dopant densities ranging from 10^{14} to 10^{18} cm^{-3}. The sign of $\partial C/\partial V$ depends on the local dopant type thus making this technique ideal for p-n junction delineation with nanometer spatial resolution. Its magnitude depends on the local carrier density. When the

tip-surface contact area is small enough the junction capacitor between the tip and the semiconductor surface may be approximated with a parallel plate capacitor and the capacitance per unit area is given by $C = \varepsilon_s / W$, where ε_s is the dielectric constant of the semiconductor and W is the width of the space charge region. Under the assumption that all the dopant atoms in the depletion region are singly ionized, the space charge density is equal to the density of dopant atoms in the region. By applying a small a.c signal to the probe and using a lockin amplifier $\partial C/\partial V$ can be measured from which the surface dopant density may be determined from the relationship

$$\partial C / \partial V = \sqrt{\frac{q \varepsilon_s N_D}{2(V_{bi} - V)}} \qquad (1.2)$$

where V is the externally applied voltage, V_{bi} is the built in potential at thermal equilibrium and N_D is the semiconductor dopant density. $\partial C/\partial V$ measurements are relatively insensitive to surface conditions. It is still important to clean the surface of native oxide to maintain the integrity of the contact as Schottky rather than MOS.

1.3.8 Scanning Resistance Microscopy (SRM)

Delineation of p-n junctions in semiconductors with nanometer scale spatial resolution has been demonstrated with the SRM using conducting tips [2,33]. This technique measures the ***contact*** resistance that results from the potential barrier formed at the interface of a biased tip when it is held in direct contact with a semiconductor surface.

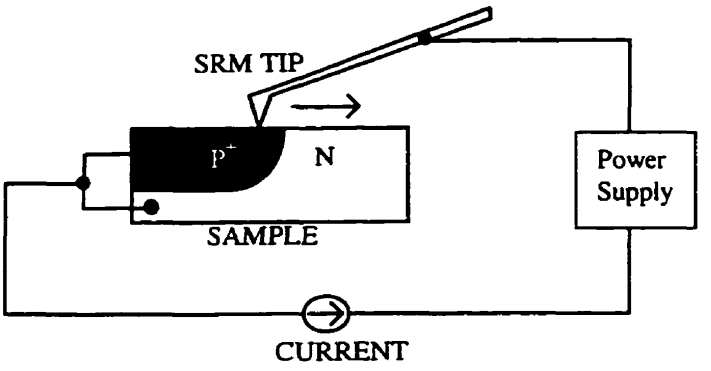


Figure 1.3 A simplified schematic diagram of the SRM instrument.

As shown in Fig.1.3, a potential is applied to the tip and the current flowing in the circuit is monitored. Spatial resolution of 20 nm has been achieved with this technique when imaging device cross sections using boron doped diamond tips. A discussion of the theoretical considerations and calibration of the SRM technique will be presented in chapter 3.

Most of the work in this thesis centers around the use of the SRM for semiconductor device analysis. The initial work in this technique was done by Shafai *et al.*. **[13].** Significant improvements of the SRM instrumentation and modifications of the technique have since been made **[34].** The SRM has been utilized to perform cross-sectional characterization of a wide variety of state-of-the-art devices. In most of the contract work done for four microelectronic companies in Canada the SRM results have provided good insight towards solving device performance problems associated with dopant diffusion that occur during device processing. Solutions to these problems lead to variations of the fabrication process of the devices and improvement of their performance. A more detailed discussion of SRM is presented in the following chapters.

CHAPTER 2

INSTRUMENT DEVELOPMENT AND TESTING

2.1 INTRODUCTION

This chapter provides a discussion of SRM instrument design, implementation and testing. Figure 2.1 shows a photograph of the SRM experimental setup used currently. The head of the SRM stage and part of the x-y-z stage are shown in (a), and the close up view of the sample, tip and SRM cantilever are shown in (b). The schematic diagram shown in Fig. 2.2 will be used to explain the basic components of the instrument. Some of the components discussed in this chapter have been replaced with better performance equipment during on going development of the instrument.

At the beginning of a measurement the deflection sensor is setup to monitor the SRM cantilever deflection. In previous SRM setups a capacitance probe was positioned approximately 100 nm above the SRM cantilever. In the current setup a laser beam is aligned so that it is reflected by a mirror on the cantilever and focused on a photodetector (Fig 2.1 b). After the sample is mounted on the piezoelectric tube scanner the x-y-z stage is used for sample coarse positioning to within a few millimeters of the tip with the aid of an optical microscope. An electronic picomotor (Model 8701) is then used for the final fine approach to the tip until mechanical contact is made.

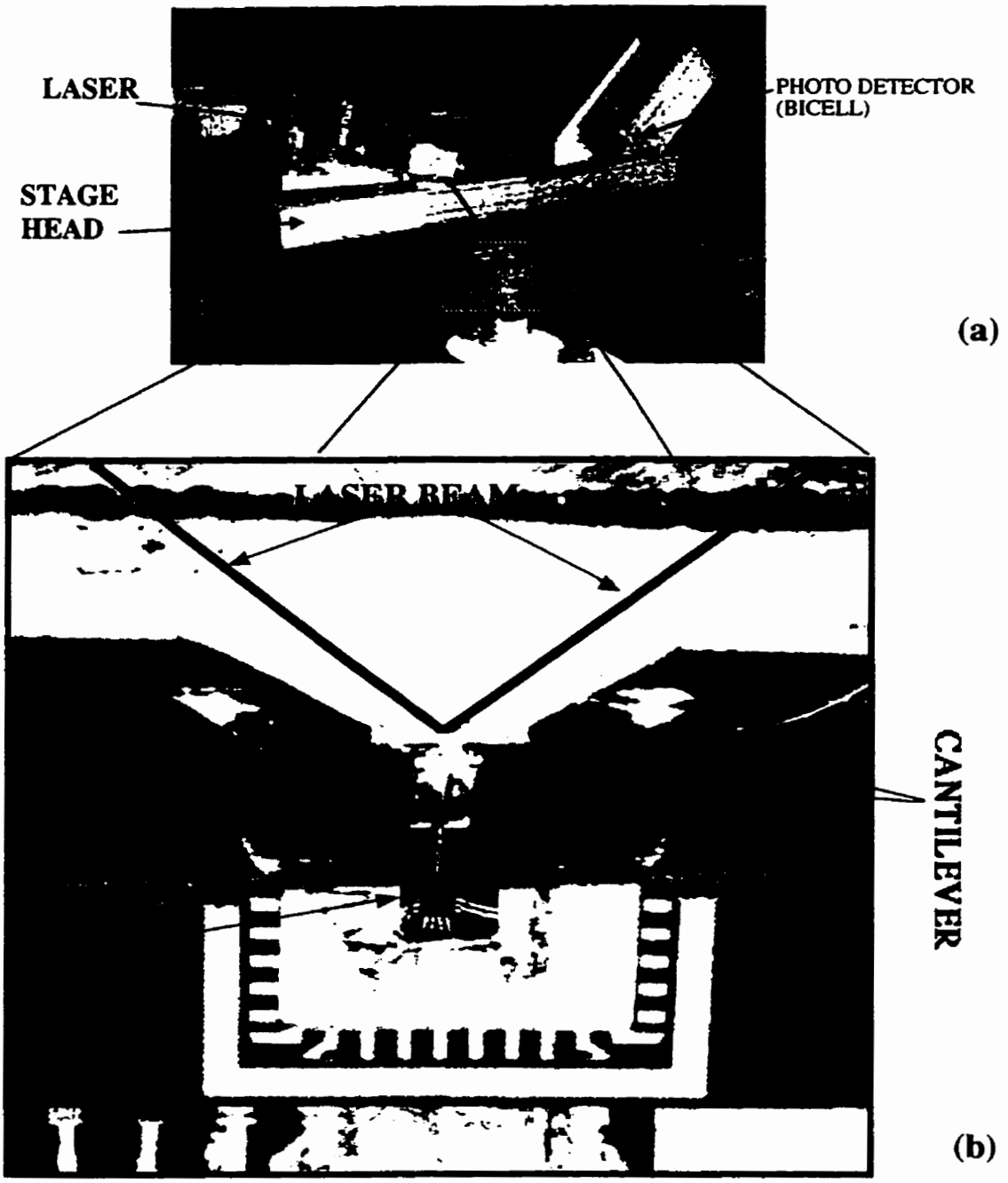


Figure 2.1 A photograph showing (a) the SRM stage and (b) a close up view of the sample mount for active device samples.

2.2 SRM EXPERIMENTAL SETUP

Figure 2.2 shows a schematic circuit of the SRM. Two independent control loops are turned on during data acquisition. One loop is used to measure the resistance profiles and the other is used to measure the topographic profile of the surface simultaneously. The overall operation principle and that of individual components of the SRM will be discussed in more detail in later sections of this chapter.

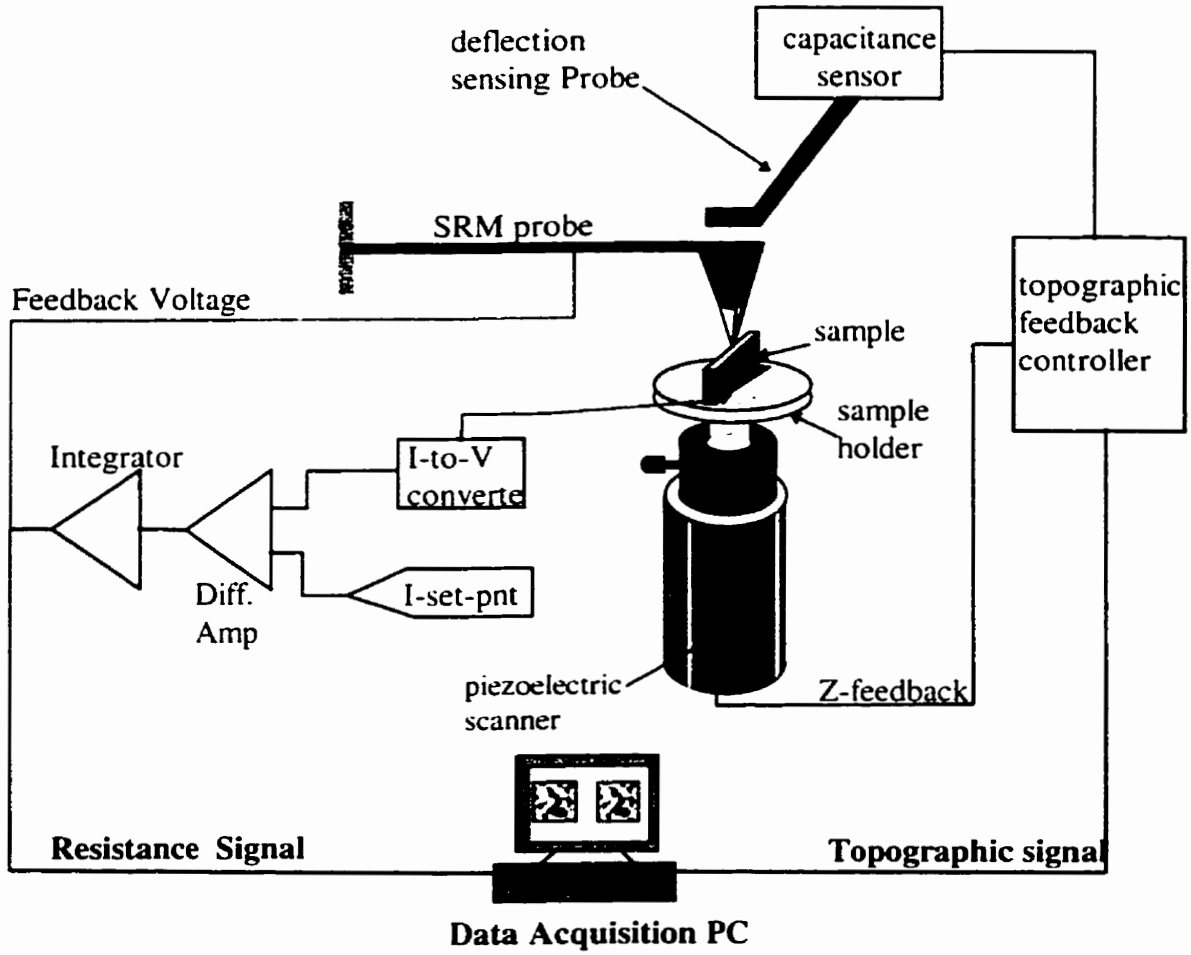


Figure 2.2. A Block Diagram of SRM experimental set-up; showing force control (right hand circuit) and current control circuit (left hand circuit).

All the SRM circuitry were developed and constructed in this laboratory. SRM measurements are performed at ambient conditions in a dark environment (aluminum box) to reduce 60 Hz noise coupling into the measurements from the laboratory lights. In order to reduce acoustic noise the walls of the SRM box are lined internally with acoustic absorbing foam material. Experiments are performed with the instrument setup on a mechanical vibration isolation table. All power supplies and equipment that uses vibrating elements, such as transformers, are kept away from the vibration isolation table.

Starting with the resistance profiling system (left hand circuit in Fig. 2.2), the SRM probe is placed in contact with the sample surface. Here the sample is mounted in a cross-section orientation. By modulating the tip voltage so that a constant current flow across the tip-surface interface is maintained it is shown (in section 3.3.8) that the SRM measurement dynamic range is enhanced significantly. This is in comparison with applying a constant voltage to the tip and measuring the current. The left hand circuit (in Fig.2.2) shows the implementation of constant current SRM.

The junction current is converted to a voltage and then compared with a set point voltage using a differential amplifier. The difference between the two signals is integrated and applied to the probe. The purpose of the feedback voltage is to minimize the difference between the set point and the measured signal. In essence this circuit maintains the tip-sample current at a value that is selected using the set-point adjuster. The local feedback voltage is then representative of the local ***contact*** resistance on the sample surface when the tip is scanned in a raster fashion.

In this measurement, the spatial resolution depends very strongly on the tip-to-surface contact area which in turn depends on the force between the tip and the sample surface. During a scan, the contact force may change as a result of sample slope with respect to the relative motion

of the tip and the sample. The contact force may also change if the surface topographic profile is not flat enough within the imaging area. In order to achieve a constant spatial resolution throughout a scan the tip loading force must be regulated such that the contact area is constant. The deflection of the SRM cantilever is monitored using a capacitance sensor through the sensing probe. If the separation between the SRM and the deflection sensing probe changes, a corresponding change in capacitance between the probes is detected and this signal is used to adjust the height of the sample in such a way as to compensate for the SRM probe deflection.

The deflection sensor shown in Fig. 2.2 is a capacitance sensor whose output is inversely proportional to the separation between the two probes. The principle of operation and calibration of the capacitance sensor is outlined in section 2.7.1. Sensitivity as high as 3 mV/nm was achieved routinely with this deflection sensor. However, whenever a new sample is mounted on the SRM stage the sensitivity of the sensor changes. Also, during a scan, the operating point on the sensor resonance curve shifts as a result of stray capacitance in the room. In order to achieved consistent and repeatable results it became necessary to calibrate the capacitance sensor quite frequently. This exercise was time consuming.

Recently the capacitance sensor has been replaced with a laser beam bounce system to monitor the deflection of the SRM cantilever. Significant improvement in the consistency and spatial resolution of the resistance and topographic results is achieved.

2.3 SRM PROBE

The SRM probe is fabricated from a 100 μm thick stainless steel foil in a typical AFM probe geometry, Fig. 2.3, with each arm 10 mm in length. A sharp conducting tip, 250 μm diameter, is bent and spring loaded in a stainless steel tube which is spot-welded at the free end of the cantilever.

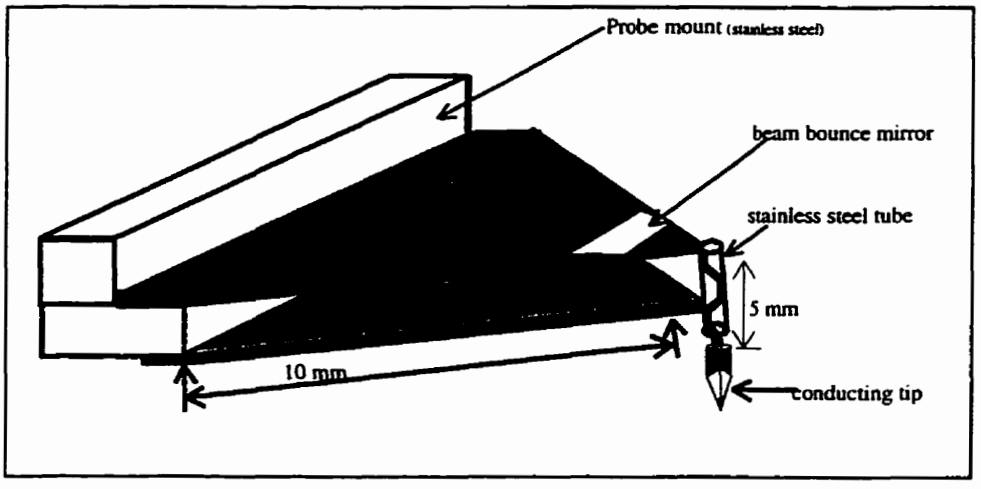


Figure 2.3 The SRM cantilever in a typical AFM cantilever geometry.

The spring constant of a single rectangular beam of length l and area moment of inertia I is given by

$$k = 3\frac{EI}{l^3} \tag{2.1}$$

where E is Young's Modulus of the beam material. The area moment of inertia of a uniform beam with a width "w" and thickness "t" is $I = \frac{wt^3}{12}$. The spring constant of this type of beam is then given by

$$k = \frac{Ewt^3}{4l^3} \tag{2.2}$$

Two identical beams mounted in parallel have an effective spring constant of $2k$. The resonance frequency of a solid rectangular lever with a concentrated load m_c at one end is given by

$$w_r = \sqrt{\frac{Ewt^3}{4l^3(m_c + 0.24wtl\rho)}} \tag{2.3}$$

The effective resonance frequency of two parallel beams is given by $\sqrt{2} \cdot w_r$. The properties of the SRM cantilever shown in Fig.2.3 can be approximated using the above formalism. In this case we have n beams of width "dw". The calculation of the spring constant and resonance frequency for this cantilever geometry is quite involved. However, a rough estimate of the spring constant was achieved by hanging known weights at the tip end of the cantilever and using a traveling microscope to measure the vertical deflection of the free end of the cantilever. The estimated spring constant here was 150 N/m with a free vibration resonance frequency of 500 Hz.

While the SRM is being developed the cantilever properties and geometry are also being modified. The instrument cantilever geometry has evolved from simple 125 μm radius tungsten and molybdenum wires of a wide variety of geometries and lengths, to triangular geometry cantilevers, much like the commercially available microfabricated AFM with two arms, all homemade. For some of the SRM cantilevers the above equations were used to predict the cantilever properties. The resonance frequency is measured by exciting the beam mechanically and measuring its frequency response.

Since SRM measurements are performed with the tip held in contact with the specimen surface the measured free vibration resonance frequency and spring constant give a lower limit

measurement (worst case). A more realistic calculation or measurement should be done with the beam fixed at both ends.

2.4 SRM TIPS

Previous SRMs have utilized metal tips fabricated from 250 μm diameter Molybdenum or Tungsten wires and conducting diamond tips. To form a sharp metal tip, a Mo or W wire is electrochemically etched by passing ac current between the wire and a platinum or graphite electrode through 1.27M KOH or 4M NaOH solution. Typical tip radii of 300 nm were obtained with this method. Sharper metal tips were obtained by using a "waxed end etch and catch" technique. Here one end of a wire is coated with wax (bees' or candle wax) and then submerged in 4M NaOH until the wax is just below the solution level. A +10V potential is applied to the wire and a graphite or platinum electrode is used for a cathode. Tips with radii down to 30nm were obtained with this method. Tip wear and contamination problems were encountered when metal tips were used to image device cross sections[13]. Most recently we have replaced metal tips with commercially available B-doped diamond tips to solve the tip wear problems and improve the lateral resolution. An SEM image of a B-doped diamond tip is shown in Fig.2.4. This tip has an apex angle of 60°. To fabricate these tips diamond was brazed into a titanium shrank and then ground to a tripyramidal shaped tip. Boron ions were then implanted into the diamond to form a conducting tip. This tip is conductive enough to perform STM measurements [35]. It has also been used to perform nano-SRP measurements [12].

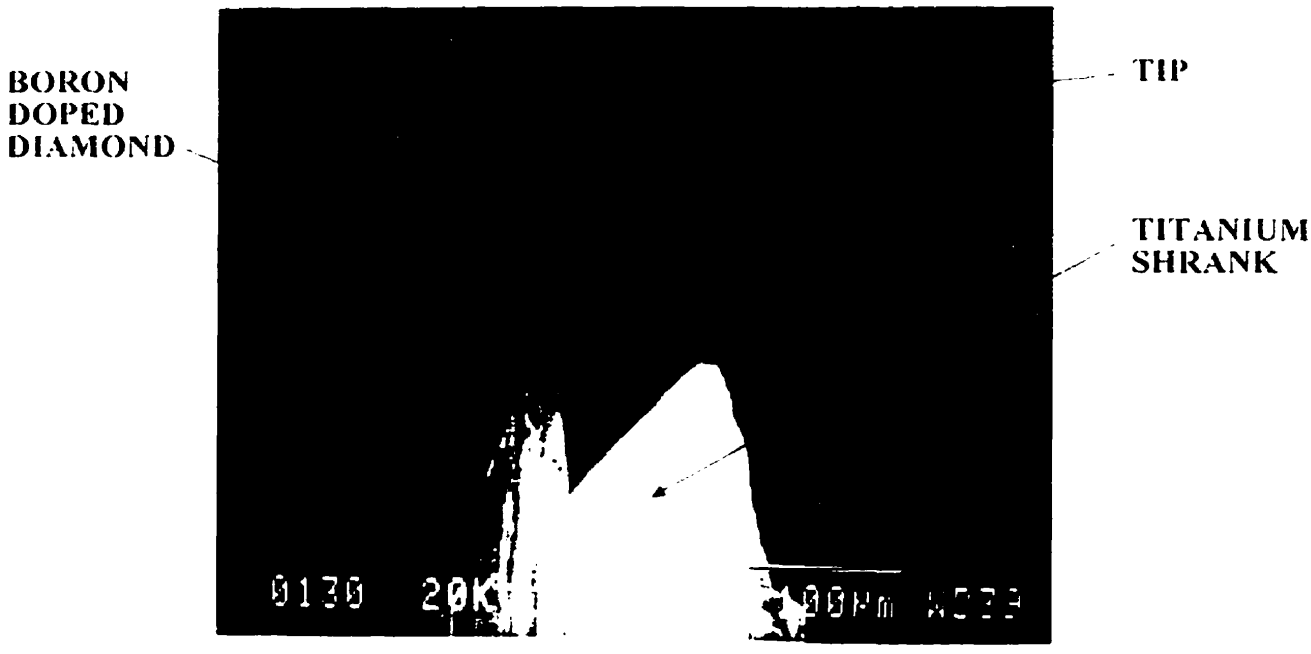


Figure 2.4 A SEM image of a diamond tip with a 60 apex angle.

2.5 PERFORMING SRM MEASUREMENTS

Previous SRM imaging was performed using constant tip voltage imaging mode. A modification was made in favor of a constant current imaging mode. The latter possesses better dynamic range in dopant measurement. The two modes are discussed in the following sections.

2.5.1 Constant Voltage SRM

A simplified SRM circuit operating in **constant voltage** mode is shown in Fig.2.5. Here a constant potential is applied to the tip and the current flowing across the tip-sample interface is measured. Using this circuit together with metal tips, it has been shown that the SRM can localize p-n junctions with a lateral spatial resolution of 35 nm [34]. As discussed in section 3.3.6, the current-voltage relationship of such a junction is exponential. For a tip voltage of 1V

and semiconductor doping density change from 10^{15} cm^{-3} to 10^{20} cm^{-3} the current changes by 8 orders of magnitude. This measurement may be carried out with the use of a logarithmic current to voltage converter.

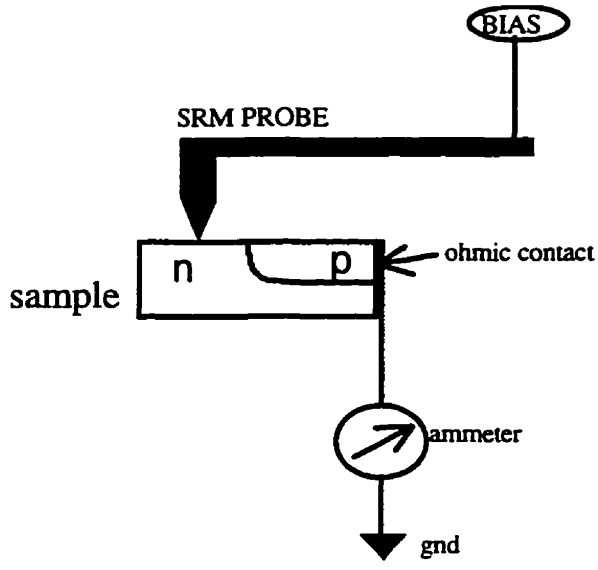


Figure 2.5 Constant voltage SRM imaging mechanism. The tip voltage is maintained constant and the current is measured and used to delineate p-n junctions.

2.5.2 Constant Current SRM

A new technique in which the probe voltage is modulated in order to maintain a **constant current** across the tip-surface contact has been implemented. A current control loop circuit, shown in Fig. 2.6, maintains several nano-amps of current flowing across the tip-sample junction. The analysis given in section 3.3.6 shows that this imaging mode has a four orders of magnitude advantage over constant voltage imaging for dopant measurements. The modulated voltage as a scan progresses is used to delineate between regions of different contact resistance.

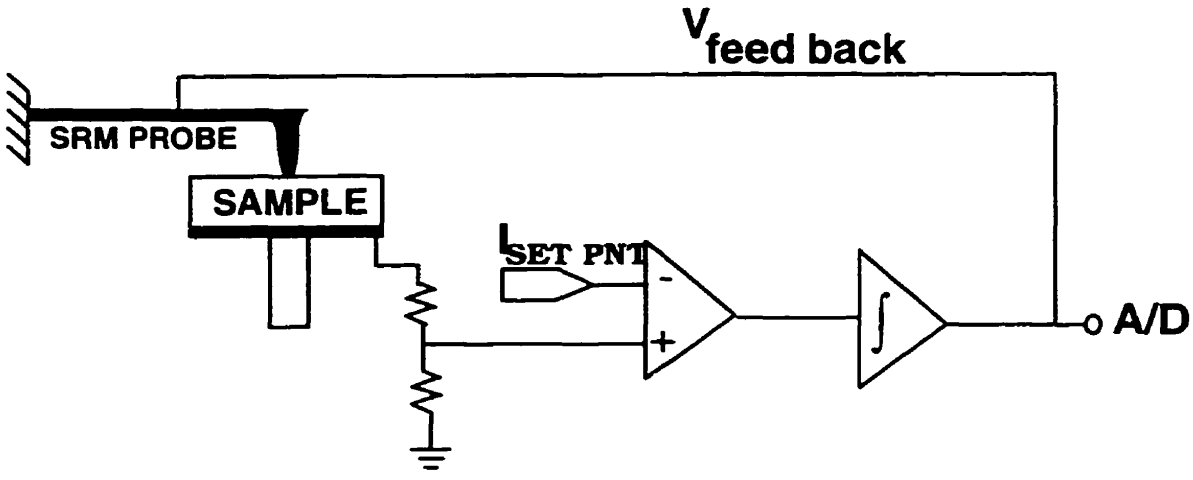


Figure 2.6 Constant current SRM imaging mechanism. The tip voltage is modulated so that the junction current is maintained constant.

2.6 IMAGING A SIMPLE TEST STRUCTURE

Constant current SRM imaging mode was used to image a simple p-n junction test structure. The results obtained from this structure were compared against "SCM" results obtained from the same structure.

Figure 2.7 below shows a schematic diagram of the test structure used to test SRM and SCM imaging techniques.

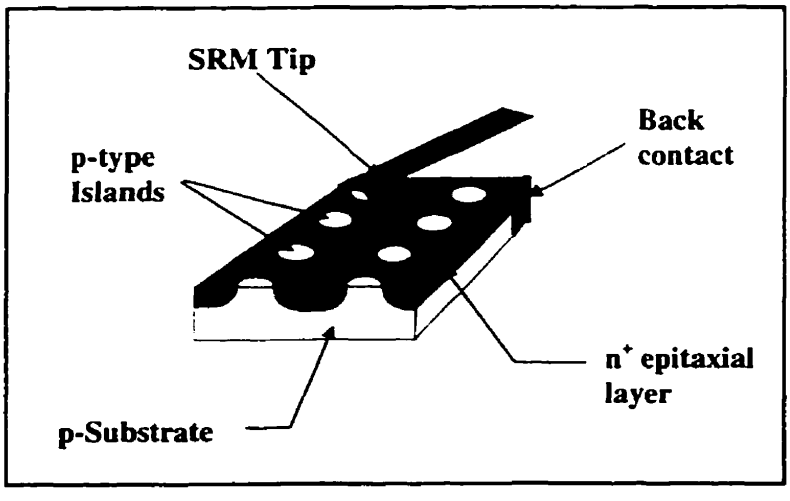
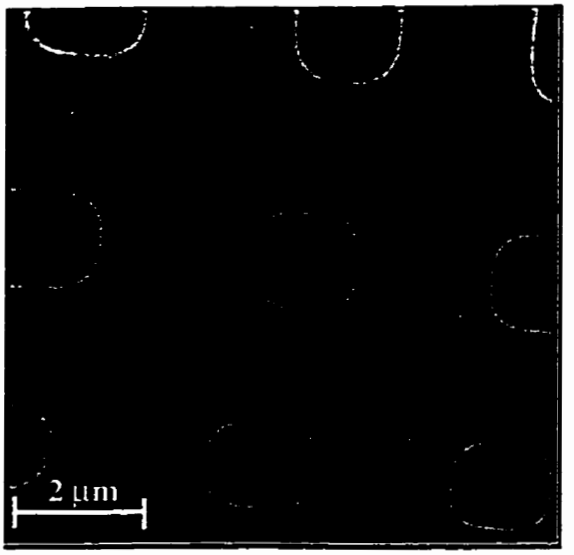


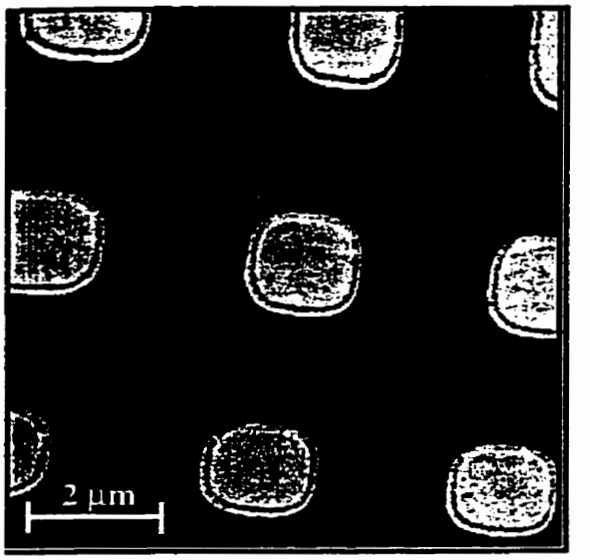
Figure 2.7 A schematic diagram of SRM test sample made up of p-type dots surrounded by n-type silicon.

To fabricate this sample islands on a p-type substrate were masked and n-type dopant (arsenic) was implanted into unmasked regions. The mask material was removed and the structure was annealed in order to activate the dopants. Topographic images of the surface show a "donut" shaped ring of height ≈10 nm surrounding the p-type regions. This ring is attributed to remains of mask material that has probably formed chemical bonds with silicon and/or arsenic during implantation or the anneal step or both. Resistance profiles show that the resistance of the ring is lower than the surrounding regions.

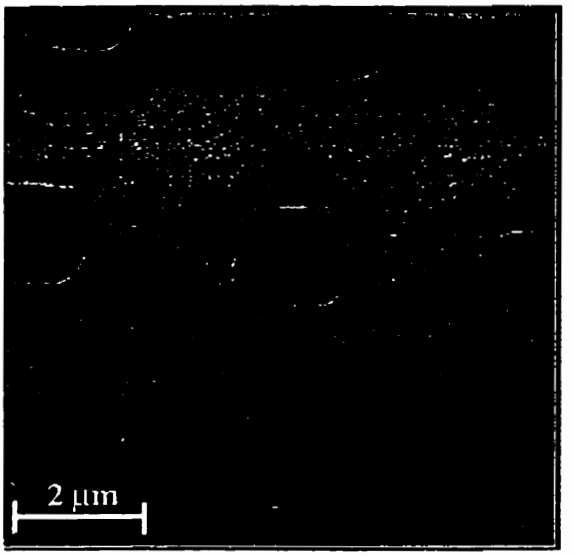
Prior to imaging with SRM or "SCM" the sample is dipped in a bath of 2.5 % HF solution for 3 seconds in order to etch off native oxide from the surface. In this etchant the residue ring does not etch as fast as either p or n type silicon. Therefore, after etching the sample a few times with HF, "donut" rings remained on the surface 15-20 nm higher than the surrounding regions. Figure 2.8 (a) and (b) show topographic and resistance profiles respectively. For this resistance profile, negative probe polarity with respect to the substrate is applied. (c) is a resistance profile image with positive probe polarity. The topographic profiles associated with Fig. 2.8 (c) and (d) are not shown here. Figures (b) and (c) demonstrate clearly the capability for SRM to perform p-n junction delineation. Figure 2.8 (d) shows a typical Schottky capacitance derivative profile.



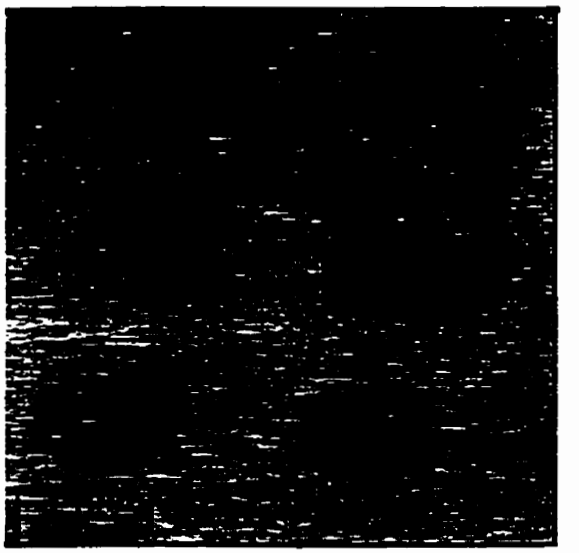
(a) Topography



(b) SRM with negative probe



(c) SRM with a positive probe



(d) "Schottky capacitance derivative"

Figure 2.8 (a) a topographic profile taken simultaneously with the resistance profile(b) where the probe is negatively polarized, (c) a resistance profile of the same area with a positively polarized probe, and (d) a "SCM" profile of the area.

2.7 ACHIEVING HIGH SPATIAL RESOLUTION

The lateral resolution of the SRM technique depends mainly on the contact force/area between the tip and the surface. The contact radius between a spherical tip and a semiconductor surface can be approximated by the cubic relation $r_c \propto F^{1/3}$ [28]. High lateral resolution is obtained by minimizing the contact radius (low contact force). The SRM is equipped with a deflection sensor (a capacitance sensor, or laser-beam-bounce system), shown in Fig.2.9, whose output signal is proportional to the SRM cantilever deflection. The capacitance sensor is used to monitor the deflection of the cantilever as the tip scans the surface. The output signal is then used to adjust the sample height through a piezoelectric scanner to maintain a constant force between the tip and the surface. Two dimensional imaging of the surface is achieved by displacing the sample in a raster pattern beneath the tip. Using this technique both resistance and topographic profiles of the surface are obtained simultaneously as shown in Fig.2.2

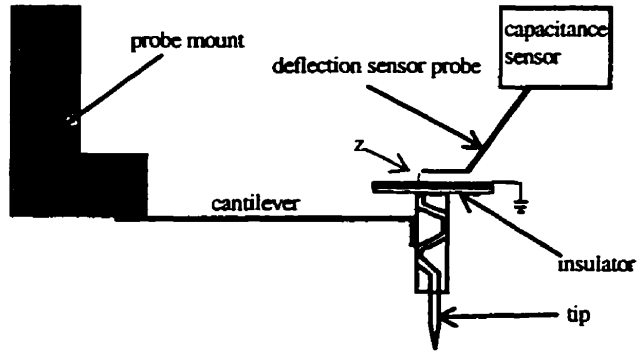


Figure 2.9. Capacitance sensor detects the deflection of the cantilever by sensing the capacitance change between the sensor probe and the grounded plate.

2.7.1 The Capacitance Sensor

The capacitance sensor is described in detail elsewhere [36]. It is constructed using a transmission line resonator from a RCA Video Disc capacitance pickup circuit operating at 915 MHz. The circuit response to this driving frequency is the capacitance sensor output signal. A probe wire is connected to the resonating transmission line with the tip positioned near the SRM probe (see Fig.2.6). The sensor-SRM probe capacitor forms part of the resonant circuit of the capacitance sensor. Any deflection of the SRM cantilever due to topographic variations on the sample surface changes the spacing between the two probes and hence the capacitance between them. This change is coupled through the sensor probe and results in a change in the resonant frequency of the resonator. Since the output signal of the sensor is the circuit response to the driving frequency, variations in the sensor-SRM probe capacitance shifts the center frequency and in effect the output signal moves up and down the flank of the bell shaped tuning curve. The center frequency can also be changed by adjusting a dc bias of a voltage variable capacitance varactor diode which also forms part of the resonance circuit. The operating point of the sensor is set by adjusting the varactor diode bias voltage so that the circuit response to the driving frequency is located at the steepest slope section of the tuning curve.

If the deflection of the cantilever changes the probes' separation by δz, the sensor gives a corresponding output voltage δV. The sensitivity of the deflection sensor is then given by $S_{cs} = \delta V / \delta z$. The slope of the tuning curve at the operating point depends on the maximum circuit response when the circuit is tuned so that its center frequency is equal to the driving frequency (the maximum height of the curve). Typically, the height of the bell shaped resonance curve is 3.0V and the operating point is positioned ≈0.4 V below the peak. By modulating the

position of the SRM probe using a calibrated piezoelectric tube (with z-parameter of 13.3 nm/V) an amplitude of δz (=1339nm) with the smallest initial probes' separation, obtained by first bringing the probes to touch and then backing them off until the contact is just broken (verified by observing the sensor output), the sensitivity of the capacitance was measured to be 0.6 mV/nm. This calibration was done for a flattened Tungsten wire and a grounded metal plate thus approximating a parallel plate capacitor.

2.8 PIEZOELECTRIC SCANNER

A piezoelectric is a material that deforms in response to an electric field. Generally SPMs use different geometry piezoelectric materials to control the position of the sample relative to the tip very accurately. By controlling the voltage applied to the piezo electrodes, sub-nanometer displacements can be achieved.

The SRM utilizes a cylindrical shape piezoelectric scanner that is capable of making three dimensional motion. Voltage is applied to electrodes that are attached to the outside surface of the piezo tube and referenced to an electrode attached to the inside surface. The outside electrodes are symmetrically divided into four quadrants. The potentials applied to opposite quadrants are equal in magnitude and 180° out of phase. These potentials represent the ±x or ±y axis. Figure 2.10 shows a drawing of the piezoelectric ceramic tube used to actuate SRM samples.

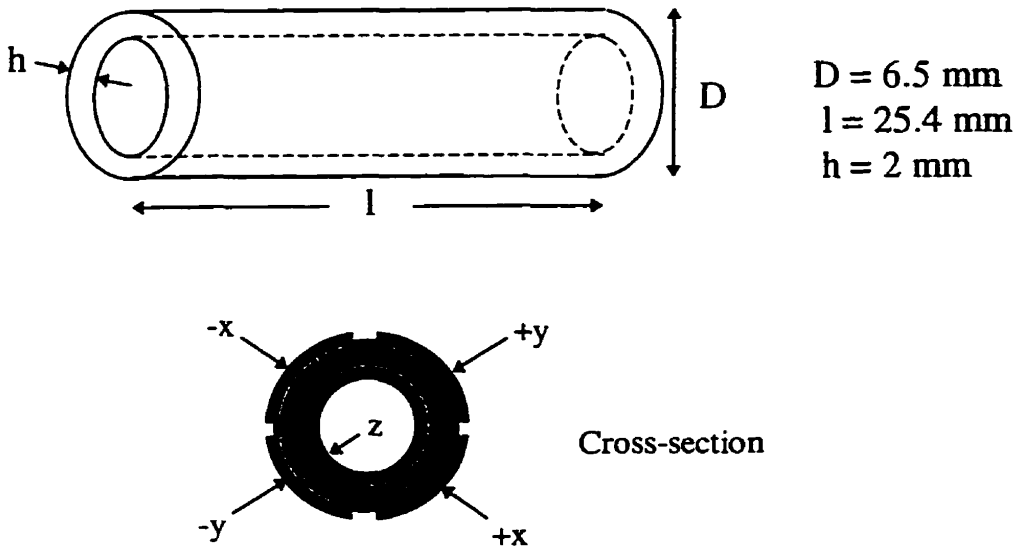


Figure 2.10 A drawing of a piezoelectric tube scanner. The cross-section view shows the arrangement of four quadrants (±x, ±y) and the inside z-electrode.

2.8.1 Calibration of the Piezoelectric Scanner

In order to calibrate the x, y, and z motions of the piezoelectric tube two techniques were used, (i) an optical fiber interferometer and (ii) imaging the topography of a 1μm diffraction grating and comparing with SEM images.

Optical fiber interferometry is a more accurate method for calibrating displacements in the nano-scale range. Here, a piece of printed circuit board was mounted on a regular Al sample stub and then mounted on the piezo tube. One end of an optical fiber was then held close to the printed circuit board with its cross section perpendicular to the axis to be calibrated. A triangular wave signal 10 Vp-p was applied to the axis of interest in order to activate the piezo. Interference of the light signal that is reflected at the glass air interface at the tip of the optical fiber with that reflected from the surface of the printed circuit board is detected by the interferometer and

displayed by an oscilloscope. Using the wavelength of the fiber light with the voltage driving the piezo and the interferometer output signal, the piezo parameters for all three axes were evaluated. The results are shown in the Table 2.1.

Axis	**Piezo constant** (nm/V)	**Motion Range** (μm)
x *and* y	120	36
z	13.3	4

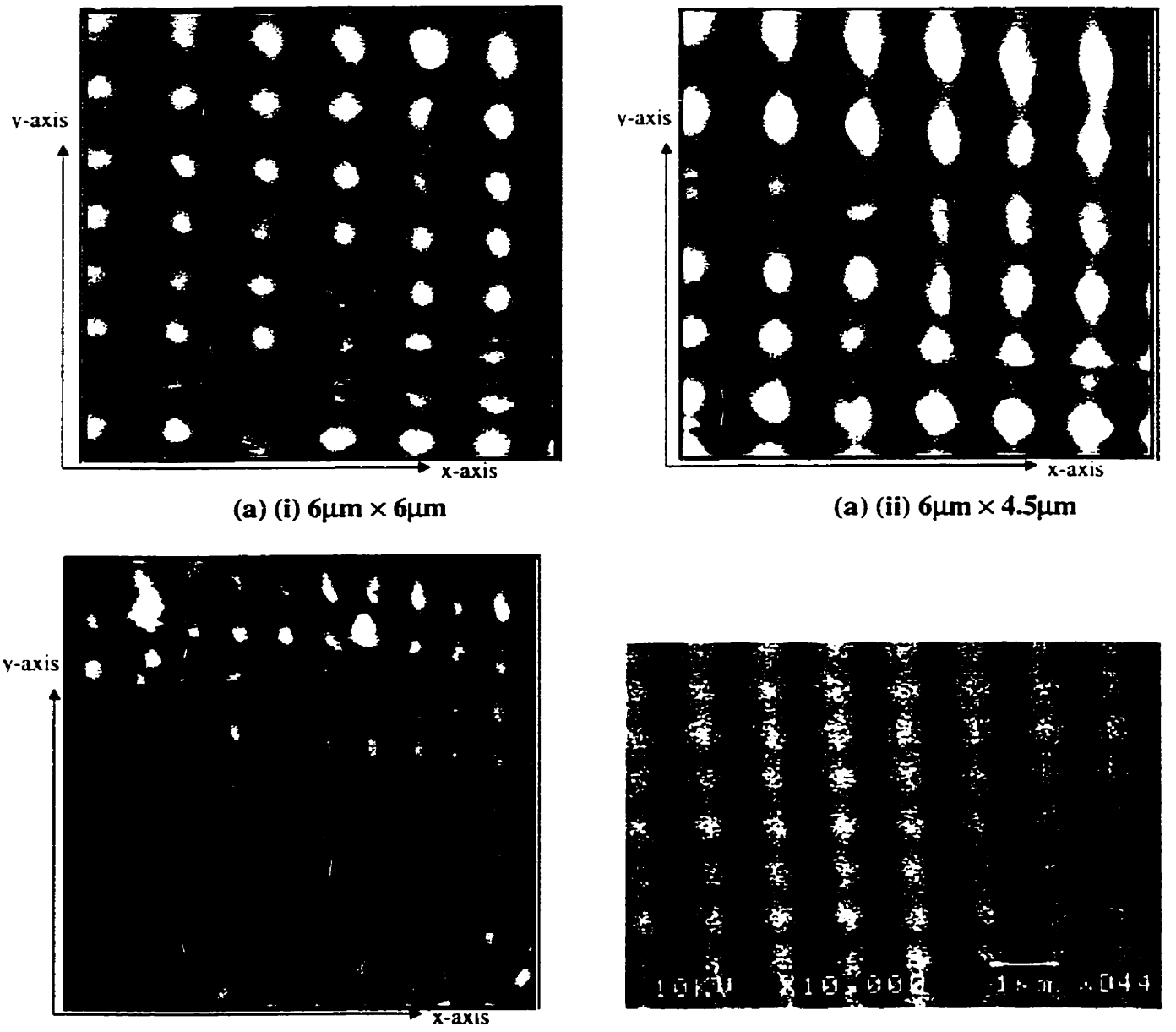
Table 2.1. Piezoelectric tube scanner parameters

The piezo **x** and **y** parameters were verified by imaging a diffraction grating sample of known periodicity. The grating is made of a square lattice of bumps of 1μm separation in both x and y directions. The results obtained from this sample were compared with SEM micrographs of the same sample. Figure 2.11 (a) (i),(ii),(iii) shows the topographic micrographs of the grating obtained using the SRM in contact AFM mode. An SEM image of the same structure is shown in Fig.2.11 (b).

Figure 2.11 (a) (i) was taken with the piezo x and y-axis scan sizes set identical (**6μm** × **6μm**). This image shows that although the piezo covers a range of 6 μm in the x direction, as expected, the y scan is **8μm,** a 25% discrepancy between the x and y axis dimensions. The same result was obtained when the fast and slow axis were reversed. Reversing the axis and getting the same result eliminates the possibility that the asymmetry is a result of the piezo being asymmetrical. The other possibility is that the scan range is a function of the scan frequency. Here the x scan rate was 2 Hz and the y scan rate was a factor of 256 slower. The asymmetry here may be corrected in two ways; first by using a slower x-scan rate, or secondly by making a 25%

adjustment on the y scan size. Figure 2.11 (ii) and (iii) show the results when the latter is chosen. A fairly good agreement is observed between x-axis and y scan sizes.

In order to verify its size, the grating was imaged with a SEM. Figure 2.11 (b) shows that the diffraction grating has 1μm periodicity.



(a) (i) 6μm × 6μm **(a) (ii) 6μm × 4.5μm**

(a) (iii) 10μm × 7.5μm **(b) SEM image**

Figure 2.11 Topographic micrographs of 1μm diffraction grating (a) (i→iii) SRM and (b) SEM.

2.9 SAMPLE PREPARATION

Much of the early work in this area was accomplished using cleaving to prepare cross sectional samples. Unfortunately this technique did not routinely yield surfaces that were consistently flat over large areas. Much better reproducibility and resolution consistency were achieved using cross-sectional polishing techniques.

Surface polishing has worked well for several other scanning probe groups [37]. Sample preparation starts by taking two samples and holding the sides of interest against each other (see Fig.2.12 (b)). Mounting the samples face-to-face avoids chipping of the edge of interest during polishing. These samples are held together by cold mount resin (see photograph in Fig.2.12 (a)). A sample is polished starting with a SiC 400 grit paper, followed by 600 grit. Then a cloth polish with 6 μm diamond grit is done, followed by 1 μm. The final polishing step was done with a 0.05 μm colloidal silica. After every polishing step the samples are ultrasonic cleaned and rinsed with methanol.

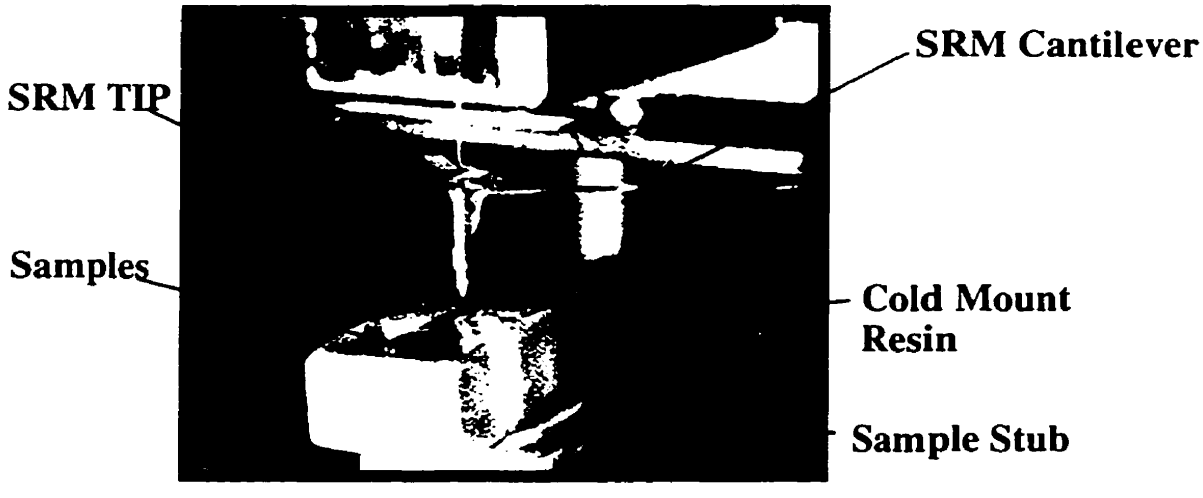


Figure 2.12 (a) A photograph of the samples mounted in cold mount resin

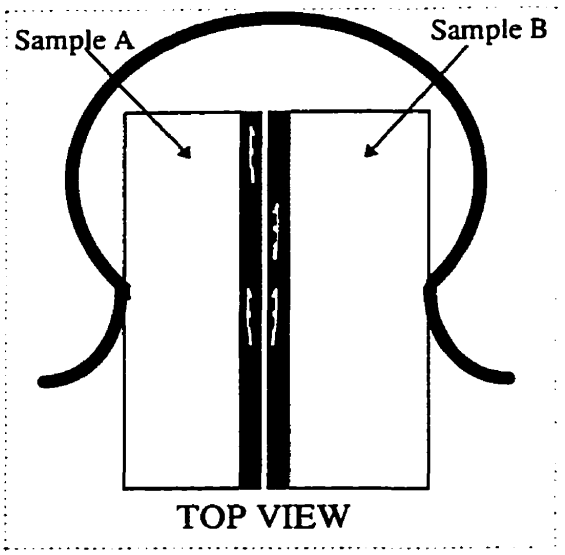


Figure 2.12 (b) A drawing of the samples' top view showing sample in face-to-face orientation. Samples are held against each other to minimize the gap between them.

2.10 SAMPLE MOUNTING FOR SRM IMAGING

Samples are cleaved and mounted either in a cross section orientation (as shown in Fig.2.12) or flat on the sample stub. The bottom of the sample is scratched with a diamond pen in order to make an ohmic contact for the return path. Conductive silver epoxy is deposited on a plastic disc which is placed on the sample stub and the sample is placed on the epoxy. A signal wire is then attached to the epoxy. Silver epoxy is left to cure in a heated oven (120°C) for at least 15 minutes. Silver epoxy becomes hard thus bonding the sample to the disc which is held to the stub quite firmly. The stub is then inserted into the piezoelectric tube and the arrangement is positioned close to the tip.

2.11 SRM ARTIFACTS

2.11.1 Piezoelectric Scanning Arc

When performing x and y scans the piezoelectric scanner traces an arc and hence introduces curvature to the images. Figure 2.13 illustrates how the x (or y) scan does not follow the assumed linear base line but a curved one. The curvature of the base line couples into the image in such a way that a flat sample would result in an image superimposed on the piezo scanning arc. This artifact is more significant when the scan size is big.

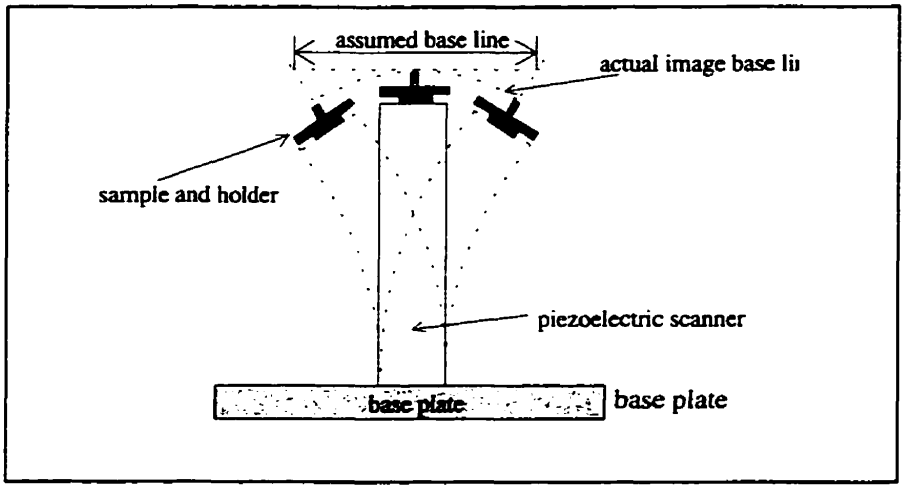


Figure 2.13 Schematic diagram of a scanning piezoelectric tube illustrating a curved base line on an image introduced by bending of the piezo as it scans in the x or y direction.

Figure 2.14 shows the topographic profile of the SRM test sample described in section 2.6. A line cross section taken along the x scan direction (after plane subtraction) is shown below.

The line cross section (Fig.2.14) demonstrates that the image is superimposed on a curved background. This curvature is attributed to the arc that the piezo traces when performing lateral scans. The radius of curvature of the profile is expected to be smaller than the sum of the length of the piezo and the height of the sample and stub because the piezo bends (see Fig.2.13) in a

complicated manner in response to bias. If large areas are imaged this artifact is expected to be more severe in topographic than resistance profiles.

A possible solution to this artifact is to build into the analysis software a **piezo-scan-arc** compensating feature that can be obtained through calibration measurements. This feature would be specific to the piezoelectric tube scanner being used.

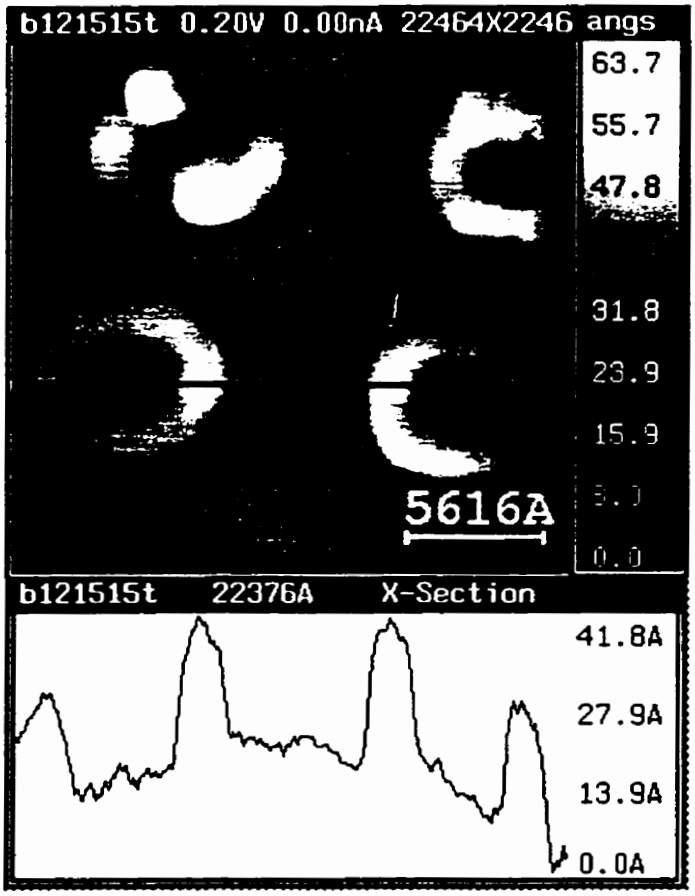


Figure 2.14. A topographic profile of "donut" ring of the SRM test sample. The line profile shown at the bottom demonstrates an artificial curvature introduced by piezo scanning arc.

2.11.2 Tip Artifacts

In the past the SRM has used metal tips fabricated from electrochemically etched tungsten wires. Since tungsten is very brittle, cutting the wire sometimes resulted in a crack that runs along the length of the wire. After etching to a sharp tip, a wire with a crack will result in a tip that is split into two. Depending on the orientation of the two tips and their relative heights, the image features will repeat. The **double-tip** artifact will be manifest in both the resistance and the topographic profiles. Figure 2.15 is a topographic profile of a "donut" showing a classic example of double tip effect. This artifact has been eliminated by using the commercial B-doped diamond tips.

Low aspect ratio and larger radius tips may result in artificially broadening SRM profiles especially when imaging a surface with radically changing topography. This artifact will be discussed in section 4.2.

2.11.3 Cross Talk

There is an artifact that couples the topographic signal to the resistance profiles. This artifact is one of the explanations for the presence of a high resistance region at the interface of the gate and substrate in Fig.4.4(a). This artifact is caused by coupling of the signal that drives the z-electrode of the piezoelectric tube to the resistance signal. Although the aluminium sample stub is electrically isolated from the z-electrode, the insulation does not shield the stub from electromagnetic coupling of this electrode signal to the resistance feedback circuit of which the sample stub is an integral part. Another possible explanation of cross talk is that the topographic control loop does not respond fast enough to step changes of the surface topographic profile. As a

result drastic change in tip-surface contact force/area and hence a drastic change in the feedback voltage occurs.

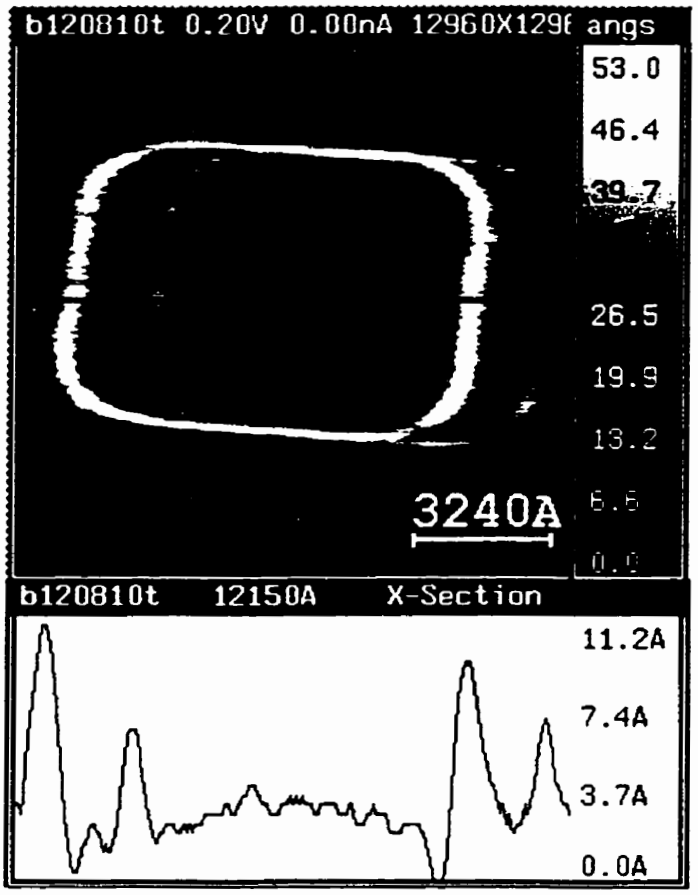


Figure 2.15: A topographic profile of a "donut" showing a classic example of double tip effect.

CHAPTER 3

TIP-SILICON JUNCTION MODELS

3.1 INTRODUCTION

Carrier profiles measured with SRM on semiconductor surfaces are based on the rectifying properties of the junction formed between conducting SRM probe tips and the semiconductor surfaces. Therefore, it is important to develop an energy band model for the junction that can be used to interpret SRM data. This chapter provides an analysis of the electrical properties of the tip-silicon junction for both metal and conducting diamond tips. In the case of metal tips the analysis is based on the known theory of metal-semiconductor (MS) junctions and their I-V characteristics. Various electrical properties of metal-semiconductor contacts have been studied extensively in the past [38,39].

The contact area between SRM tips and specimen surfaces are much smaller than most of the well studied MS junctions. Furthermore, these nanometer scale contacts possess a spherical geometry as a result of the hemispherical geometry of the tip. While the tip is in contact with the surface, it is also scanned along the surface. Friction between the tip and surface may result in excessive heat generated at the junction, which may affect its I-V characteristics of in an unpredictable manner compared to stationary MS junction. Potentially, the junction may be far enough from thermal equilibrium so that the theory of well behaved MS junctions may be invalid.

Superior mechanical and chemical properties of diamond tips generated more interest in studying the electrical properties for the junction it forms with silicon surfaces compared to metal tips. Studies have shown that, unlike most semiconductors, diamond has a negative electron

affinity and hence is a good candidate material for low energy electron emission experiments **[40]**. Its electron affinity depends on the crystal plane of interest. In this study, an I-V characteristic model for the diamond tip-to-silicon junction is developed. This model is based on I-V spectra obtained from measurements performed on uniformly doped silicon substrates of well known dopant densities.

The high pressures present in these contacts can actually change the electronic character of the semiconductor. This interaction must always be kept in mind when studying electrical properties of semiconductors using contact mode SPMs. A systematic survey of literature for the study of mechanical and electrical aspects of high pressure microcontacts was reported by T. Claryse **[31]**. This report shows that three successive regimes are observed as the pressure between a tip and a silicon surface is increased. Initially an elastic regime, followed by the elasto-plastic regime where essentially a plastically deformed region is surrounded by an elastically deformed region, and finally the fully plastic regime are observed. This analysis concluded that if the pressure is increased beyond 8 GPa in the presence of shear stresses silicon and germanium undergo a localized transformation from the cubic structure to a denser β-tin state. The forbidden energy band (E_g = 1.1 eV for silicon) between the conduction and valence band narrows by about 50% at pressures of 5 Gpa. After the transformation, current-voltage characteristics for this junction show that the contact is approximately ohmic. Tip imprints that remain on the surface after the probe has been removed provide evidence of the surface deformation under the tip stress. Under these conditions the current flowing across this junction is limited mainly by the bulk spreading resistance of the sample. The direct relationship between sample spreading resistance and local sample resistivity when using metal tips has been exploited in order to extract semiconductor dopant profiles **[12, 31]**. Nano-SRP measurements taken with conducting

diamond tips have been used to extract dopant profiles [12]. The SRM probe tip exerts much lower forces (typically < 20 μN or pressure ≡ 3.5GPa or less) on the sample surface compared to SRP. It will be shown in section 3.3.4 that when the tip-substrate force is low enough (pressure < 8Gpa) the tip-surface **contact** resistance dominates the series sample **spreading** resistance.

3.2 SRM : CONTACT RESISTANCE MEASUREMENTS

Initially, the SRM utilized metal tips. More recently conducting diamond tips have been utilized because of the superior mechanical properties of diamond as well as its chemical inertness. A schematic circuit diagram of the SRM is shown below (Figure 3.1).

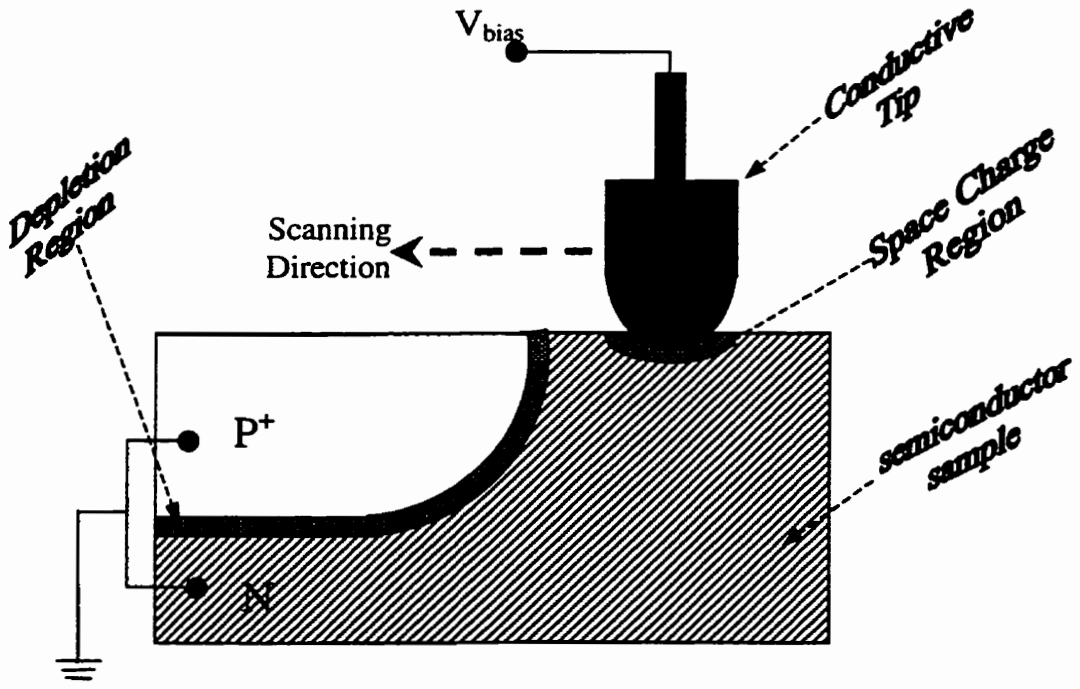


Figure 3.1 A schematic circuit of SRM showing space charge regions at the interface of the tip and sample as well as a P^+-N junction.

Figure 3.1 shows the essential elements of the SRM. As discussed in section 2.5.2, a conductive tip is biased and positioned in contact with the semiconductor surface. While

scanning the tip across the surface in a raster pattern, the current flowing across the tip-surface interface is also monitored. A scan rate of 2 Hz on the fast axis is used in SRM imaging. For purposes of modeling the interface between SRM tips and sample surfaces it has been assumed that the tip is stationary relative to the surface while a measurement is being taken at each point. This approximation assumes that the effect of friction between the tip and surface on the I-V behavior of the junction is insignificant. In this analysis, attention is paid to the electrical properties of the nano-contact between the tip and the sample surface. An equivalent electrical circuit of this system is shown in Fig.3.2.

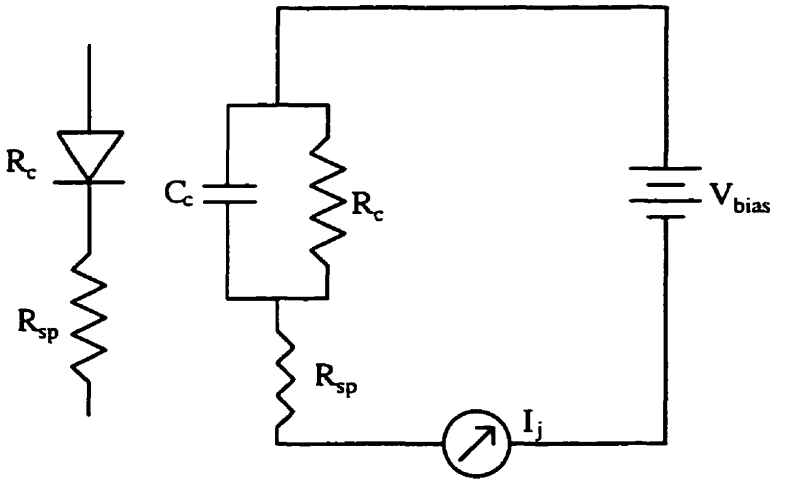


Figure 3.2 An Equivalent Circuit for SRM

The tip-surface junction is modeled as a parallel combination of a capacitor (depletion capacitor) and a resistor (due to junction barrier) connected in series with the bulk spreading resistance of the sample. The SRM is based on measurements of a d.c. current flowing across the junction. Since SRM is a d.c measurement technique, the capacitor is bypassed through the contact resistance.

All other elements of the SRM circuit (except R_c) have been verified to possess either negligibly small impedances or impedances that do not change as the tip scans the surface or both. R_c is the contact resistance experienced by carriers when they cross the junction interface. This resistance is a consequence of the potential barrier that exists at the interface after the semiconductor and tip are brought into contact at thermal equilibrium. The Fermi energy level of the two materials equalize and remain flat throughout the sample and tip in the absence of any externally applied voltage. A potential barrier can also exist at the surface of a material if there is a high density of surface states. The presence of the potential barrier implies that the region is depleted of majority charge carriers. The space charge region (depletion region) located at the interface results in the formation of a junction capacitor, C_c. R_{sp} is the series resistance experienced by charge flowing within the body of the sample in the vicinity of the tip.

A relatively large area on the back of the substrate is scratched with a diamond pen in order to create defects and conductive silver epoxy is deposited and heat treated at 120 °C for 20 minutes. Silver epoxy is used to bond the ground electrode that completes the circuit to the substrate. Although this contact is a metal-semiconductor contact, the technique used to bond the ground electrode results in a contact that has approximately linear I-V characteristics. The resistance between two such contacts is of the order of 200 → 300 Ω. The contact area is also substantially larger than the probe tip-surface contact thus making the back contact resistance much smaller than R_{sp} and R_c. If the SRM diamond tip is held in contact with a p-type silicon sample (F ≡ 1 μN) of dopant density 1.2×10^{17} cm^{-3}, the contact resistance varies between 0.2 GΩ and 2 GΩ for tip bias voltages varying between -4V and -0.2V respectively. If the tip is positively polarized the contact resistance varies between 1 GΩ and 20 GΩ for tip bias voltages

varying between +4V and +0.2V respectively. This analysis was done using the I-V data shown in Appendix A. As expected, the contact resistance depends on the magnitude and polarity of the bias voltage applied to the tip.

Section 3.3 below provides a discussion of simulations of a metal tip contacting a silicon surface. Here, it is demonstrated that when the tip-surface contact pressure is low enough (< 8 GPa) the contact resistance (R_c) is dominant over spreading resistance (R_{sp}).

3.3 METAL TIPS ON SILICON

Metal SRM tips were fabricated from molybdenum and tungsten wires. These 125μm radius wires were electrochemically etched in 1.27M KOH or 4M NaOH solutions as described in chapter 2. Tip radii as small as 100 nm were obtained. When the contact force is carefully monitored and kept at a minimum, contact radii as small as 30 nm can be achieved resulting in spatial resolution as high as 35 nm.

3.3.1 Contact Resistance (R_c)

Here contact between metal tips and silicon surfaces is assumed to be an ideal metal-semiconductor contact. Spherical geometry is assumed for this junction because the shape of the very end of the tip is estimated to approximate a hemisphere. It is also assumed that there is no junction interfacial layer and no interface states. The energy band structure for such an ideal M-S contact possesses flat band at the two surfaces prior to making contact. This metal-semiconductor contact is illustrated by the figure below.

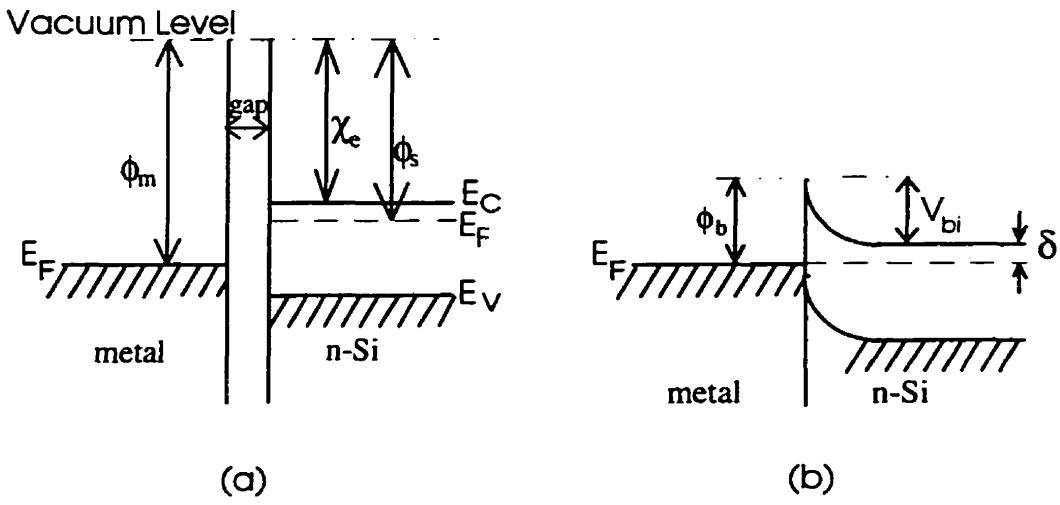


Figure 3.3 Energy Band Diagram for a metal↔n-type semiconductor contact at thermal Equilibrium (a) before contact and (b) after contact. Here $\phi_m > \phi_s$ and the contact is rectifying.

Figure 3.3 shows an energy band diagram for a metal-n-type semiconductor system (a) before intimate contact is made and (b) after intimate contact has been made and the system is allowed to reach thermal equilibrium. The metal work function (ϕ_m) is larger than the semiconductor work function (ϕ_s) and hence the junction is rectifying. For the condition $\phi_m < \phi_s$, the above junction would **not** rectify. This point will be developed further later. Figure 3.3 (b) shows that the metal and semiconductor Fermi energy levels are aligned in order to satisfy the thermodynamic equlibrium requirement. This is achieved through diffusion of electrons from the semiconductor to the metal thus leaving uncompensated dopants near the interface on the semiconductor side. In this way a potential barrier is formed at the interface as shown in Figure 3.3 (b). For this idealized contact the absence of surface states has been assumed. However, for non-ideal contacts the junction barrier height is dominated by the presence of interface states [41]. Here the built in potential is given by

$$V_{bi} = \phi_{bn} - \delta \qquad (3.1)$$

where δ is the defined to be (E_c - E_F) and ϕ_{bn} is the height of the potential barrier. Using the abrupt-junction approximation (P^+-N) for a planar junction geometry the width of the potential barrier is given by

$$W_{pl} = \sqrt{\frac{2\varepsilon_s}{qN_D}(V_{bi} - V)} \qquad (3.2)$$

where N_D is the semiconductor doping concentration, ε_s is permittivity of the semiconductor and V is external voltage applied across the junction [33].

The discussion presented here is based on the assumption that thermionic and field emission, acting in parallel, are the only mechanisms by which electrons are transported across the junction. Previous work on simulation of the metal tip-silicon contact was performed by C. Shafai.[29]. The **contact** resistance was calculated for thermionic emission as a function of bias voltages for different contact areas. Thermionic emission current exhibits no dependence on the dopant density of the semiconductor. The results demonstrated that the contact resistance ranges from about 1 kΩ to 100 MΩ as the voltage is decreased from 600mV to 100mV for 50nm contact radius. A combined thermionic and field emission current calculation showed that the contact resistance is also sensitive to the substrate dopant density. For a 50nm contact radius the contact resistance varies from about 30MΩ to 50GΩ on a p-Si substrate with dopant density of 10^{19} cm^{-3}.

In this work, a comparison is made between the spreading resistance (R_{sp}) and contact resistance (R_c) as a function of the semiconductor dopant concentration. An ideal metal-semiconductor contact with spherical geometry is assumed and the calculation is performed for different contact areas. Tip-to-surface contact area depends on the force between the two.

A hemispherical tip of radius R exerting a force F on an elastic surface makes contact on a circular area of radius r_c given by [42]

$$r_c = \left(\frac{3RF}{4E^*}\right)^{1/3} \tag{3.3}$$

where $E^* = [(1-\nu_1^2)/E_1 + (1-\nu_2^2)/E_2]^{-1}$ and E_1, ν_1 and E_2, ν_2 are Young's Modulus and Poisson's ratio of the tip and sample, respectively. Obviosly, in order to achieve high spatial resolution SRM imaging it is essential to maintain as small a contact area as possible. Equation 3.3 shows that spatial resolution may be enhanced by keeping the tip radius and the applied force at a minimum. This is achieved by utilizing very sharp SRM probe tips (radius of curvature of sub 100 nm) and good force control system while scanning.

3.3.2 Thermionic Emission

Thermionic emission is a term used to describe the emission of electrons (and/or ions) from a solid when heated in a vacuum. Thermionic emission can be viewed as an evaporation process, the temperature dependence of which is accurately described by the Richardson equation for the current density of emitted electrons

$$j_R = A(1-r)T^2 \cdot \exp(-e\phi / kT) \tag{3.4}$$

where **A** is the Richardson constant, $1-r$ is the transmission coefficient of the surface barrier for electrons, T is the temperature, and $e\phi$ is the work function. Applying an electric field to the surface of a metal increases the thermionic current density (Schottky effect) because the field lowers the surface potential barrier.

The Schottky barrier in a metal-semiconductor contact inhibits the flow of electrons from the semiconductor to the metal or vice versa. However, by thermal excitation or absorbing incident photons electrons can attain enough energy to surmount the energy barrier by the process of thermionic emission. Marginally excited electrons can cross above the barrier if the built in potential is reduced by forward biasing the junction. In principle, the bias voltage can be controlled to allow a certain thermionic current to flow across the barrier. The bias voltage dependence of the thermionic current density is given by

$$J_{TE} = A^* T^2 \cdot \exp(-q\phi_b / kT)\{\exp(qV / kT) - 1\} \qquad (3.5)$$

where $A^* = 4\pi m^* qk^2 / h^3$ is the effective Richardson constant and m^* is the effective mass of electrons in the semiconductor, and V is the applied bias voltage.

3.3.3 Field Emission

Electrons can be extracted from cold conductors or semiconductors by applying a strong electric field in the reverse bias condition of the junction. This phenomenon (**field emission**) occurs at fields of the order of $10^9 \rightarrow 10^{10}$ V/m. Application of a high field to the metal produces a triangular potential-energy barrier and electrons arriving at the metal surface may quantum mechanically tunnel through the potential barrier. The field emission current density depends on the width of the barrier and the external field.

Similarly electrons that have energies below the height of the Schottky barrier may penetrate the barrier by quantum mechanical tunneling. Since the width of the Schottky barrier gets narrow with increasing energy the tunneling current increases very rapidly with electron

energy. The bias voltage dependence of field emission current density (J_{FE}) at low temperatures is given by:

$$J_{FE} = J_{SF}[\exp(\frac{qV}{kT}) - 1] \tag{3.6}$$

where

$$J_{SF} = A^* T^2 (\frac{E_{00}}{kT})^2 (\frac{\phi_b + V}{\phi_b}) \exp[\frac{-2\phi_b^{3/2}}{3E_{00}\sqrt{\phi_b + V}}] . \tag{3.7}$$

Here A^* is the effective Richardson constant, ϕ_b is the barrier height, $E_{00} = \frac{2q}{\alpha}\sqrt{\frac{N_d}{2\varepsilon_s}}$, $\alpha = \frac{4\pi\sqrt{2m_e}}{h}$, and N_d is the semiconductor dopant concentration. It is interesting to note that the field emission current is also sensitive to the semiconductor dopant concentration. This implies that, if all else remains constant (e.g. applied voltage, contact area), the surface contact resistance profile of a semiconductor represents the dopant profile on the surface.

3.3.4 Junction Current Versus Substrate Dopant Concentration

The curves shown in Figure 3.4 represent the dependence of the junction current on substrate dopant density for an ideal contact between a metal tip and the surface of a P and N-type silicon. This calculation is done for a tip-surface contact area of $10^{-10} cm^2$ for constant probe bias voltages. The negative signs on the left half of the horizontal axis was used only for the purpose of separating the P from N type regions.

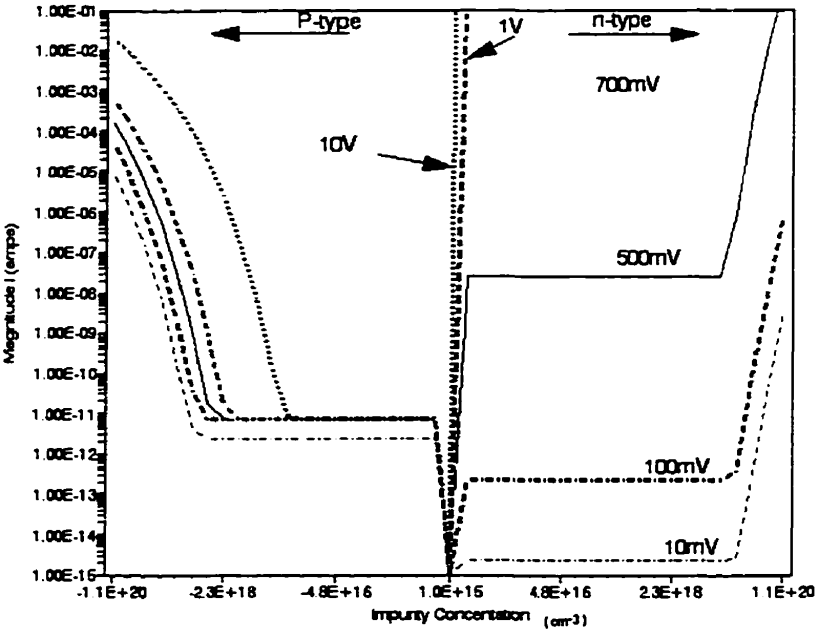


Fig 3.4. Calculated junction current versus impurity concentration at four different bias voltages for a dopant density range of $10^{15} \rightarrow 10^{20} cm^{-3}$ on both p and n type semiconductor.

These curves show that the current is constant for dopant densities below $\approx 3\times10^{18} cm^{-3}$ on both regions at low bias voltage. The increase in current above this concentration indicates that field emission current is the dominant means of current flow. However, the graphs show that at bias voltages higher than 0.5V the junction current is much higher on N-type substrates. This shows that, as expected, positive bias on the metal relative to the N-type semiconductor forward biases the junction. However, the graphs show that the current is constant for low dopant densities (thermionic emission is dominant) and show dependence on substrate doping at higher densities (dominated by field emission). The characteristic curves have the same shape on the P-type region. These curves represent an SRM operating in constant voltage mode. Although Fig.3.4 shows curves for positive probe bias, the same shape curves are obtained for negative bias. Furthermore, this family of curves demonstrate how the SRM performs P-N junctions delineation. For instance, at 100 mV bias and $4.8\times10^{16} cm^{-3}$ doping concentration the current flowing across the junction is $\approx 0.3 pA$ on an N-type region and $\approx 10 pA$ on a P-type region.

3.3.5 R_c / R_{sp} Vs Dopant Concentration

The contact resistance for an ideal metal-semiconductor contact (as described above) is given by

$$R_c = \left(\frac{\partial I}{\partial V}\right)^{-1} \tag{3.8}$$

where $I = J_{TE} + J_{FE}$.

For the same contact conditions spreading resistance is calculated from the expression

$$R_{sp} = \frac{\rho}{2\pi r} \tag{3.9}$$

The resistivity ρ is proportional to the inverse of the dopant concentration.

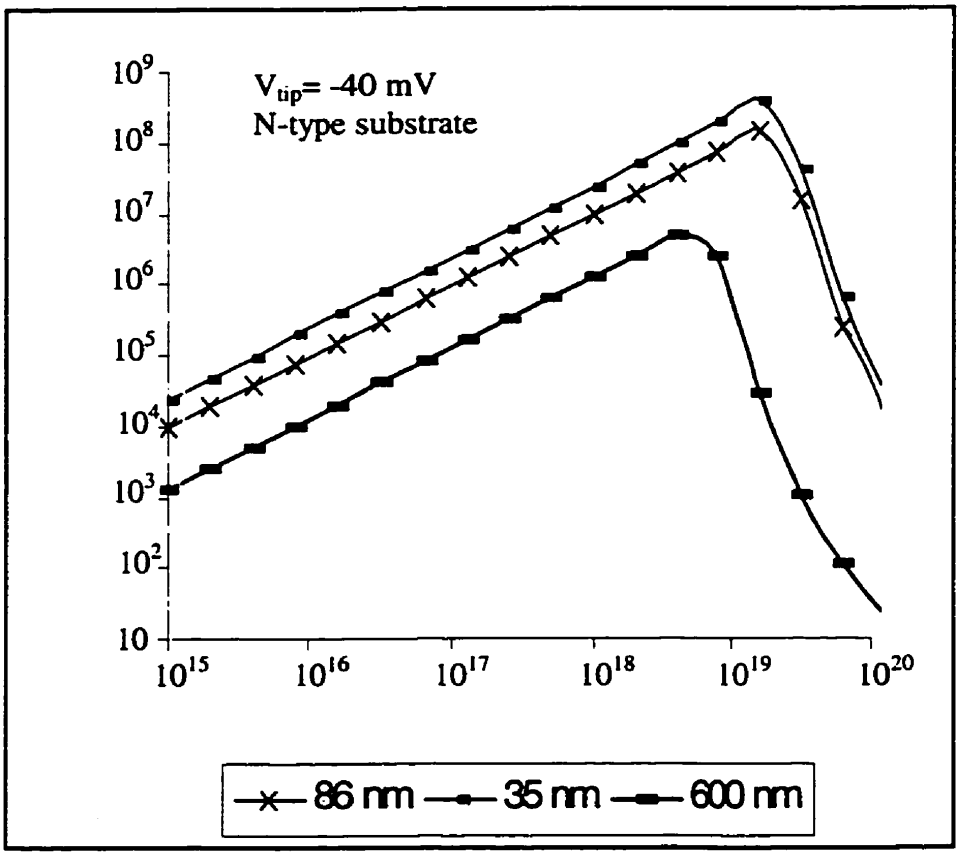


Figure 3.5 Contact-to-Spreading resistance ratio as a function of dopant concentration for contact radii 35nm, 86nm and 600nm. Tip voltage is set at -40mV in contact with n-Si.

Figure 3.5 shows that for low contact area (low contact force) the contact resistance becomes dominant over spreading resistance. At high dopant concentration ($\approx 3\times10^{18} cm^{-3}$) field emission becomes a dominant current transport mechanism across the barrier and the contact resistance decreases. Spreading resistance does not decrease as rapidly with dopant concentration. However, if the contact area is kept below 86 nm the contact resistance is still four orders of magnitude higher than spreading resistance at high dopant concentration.

3.3.6 Enhancing Dynamic Range Using Constant Current Measurement

Constant voltage mode SRM imaging, as discussed in section 2.4, was utilized previously by Shafai et al. A new technique in which the probe voltage is modulated in order to maintain a constant current across the tip-surface contact has been implemented as discussed in chapter 2. The modulated voltage as a scan progresses is then used to delineate between regions of different contact resistance. The use of constant current imaging significantly improved the dynamic range of this technique as demonstrated by Fig.3.6.

The curves shown here were obtained from a simulation of a micro-contact between a metal tip and a P-type silicon surface. This simulation is based on the assumption that thermionic and field emission, acting in parallel, are the only mechanisms by which carriers are transported across the junction. The open-squares line graph shows the contact current variation with doping levels for a tip-surface contact area of $10^{-10} cm^2$ at a **constant voltage** (1V) applied to the probe. Whereas current remains constant at doping levels below $\approx 3\times10^{18} cm^{-3}$, the increase in current above this concentration indicates that field emission, which depends on dopant concentration, is the dominant mechanism of current flow across the junction. The characteristic

curves have the same shape on an N-type region with negative polarity. Over this range of dopant concentration the current changes by eight orders of magnitude.

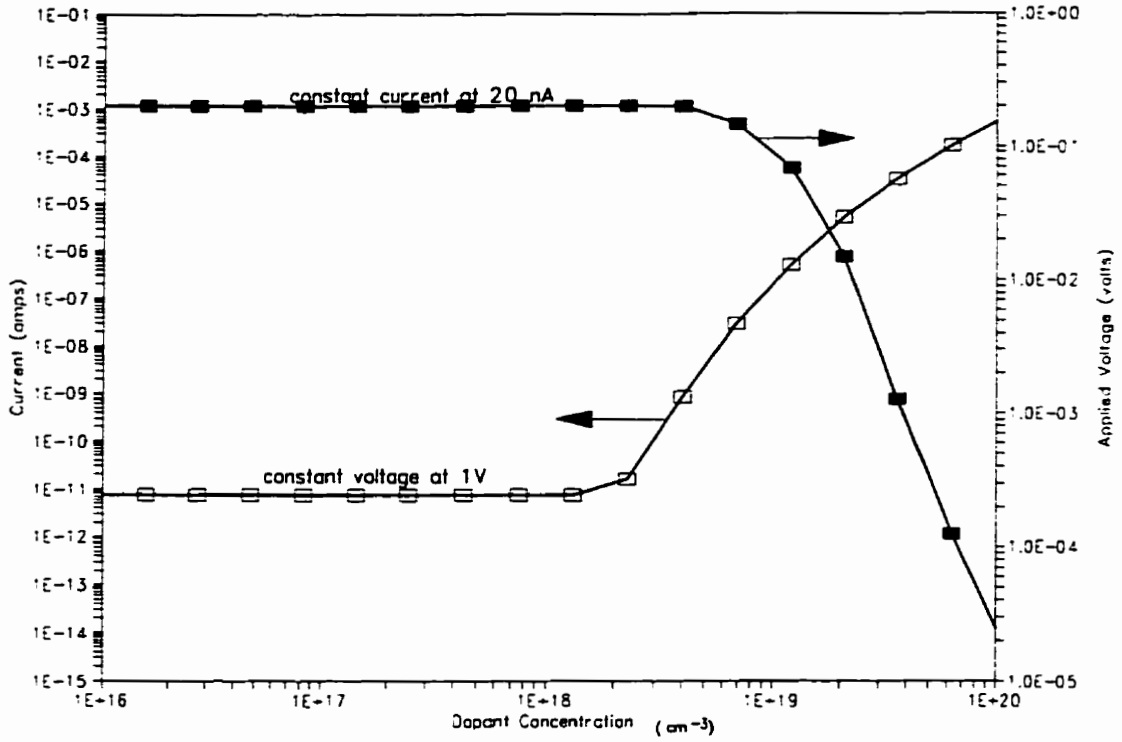


Figure 3.6 Junction current (open squares) and applied voltage (filled squares) versus dopant concentration on a P-type silicon substrate.

Constant current (20 nA) SRM imaging is represented by the filled-squares line graph. This current is maintained constant while the voltage (right hand side Y-axis) is modulated. Again, the voltage remains constant at low dopant levels and a decrease in voltage is observed after $\approx 3\times10^{18} cm^{-3}$ dopant concentration. This decrease is attributed to field emission becoming a dominant mechanism of current transport across the junction. Over the range of dopant concentration used in this calculation the voltage changes by four orders of magnitude. Therefore, over this range of dopant concentration constant current signal covers four orders of magnitude fewer than constant voltage signal. Although Fig.3.6 shows curves for positive probe

bias and P-type silicon surface, the same shape curves and dynamic range argument holds for negative bias and N-type silicon surface. This new technique offers increased dynamic range for SRM imaging.

3.4 INTERFACE BETWEEN DOPED DIAMOND TIPS AND SILICON

The use of metal tips to perform SRM imaging experiments presented difficulties in achieving a consistently high spatial resolution especially when imaging real cross sections. Metal tips picked up debris and became blunt quite quickly especially after scanning over metals and thus degraded the spatial resolution quite significantly. Commercially available conducting diamond tips have replaced metal tips. There are two main advantages of using diamond tips; 1) chemical inertness of diamond to common semiconductors, and 2) the physical hardness of diamond improves the life time of the tip and gives good repeatability. The experimental results presented in chapter 4 show that the use of the heavily doped diamond tips improved the SRM spatial resolution significantly. Diamond has a wider band gap (5.5 eV) compared to silicon (1.1 eV). This means that the junction formed between the tip and a silicon surface is a heterojunction. This is in contrast to a homojunction where only one semiconductor is involved. The results obtained with this tip provided the motivation for a careful analysis of the junction formed between the boron doped diamond tip and silicon surface. Such an analysis will provide a way of calibrating the system in order to interpret the results.

3.4.1 Energy-Band Profile of Heterojunctions

A heterojunction is defined as a junction formed between two dissimilar semiconductor materials. When the two semiconductors have the same type of doping, the junction is called isotype and when they differ, the junction is called anisotype. Heterojunctions have been studied for more than 30 years and have been utilized in many applications. A basic device model for heterojunctions was proposed by Anderson in 1962 [43]. This is an energy-band model of an ideal abrupt heterojunction without interface traps. Anderson's model is based on the discussion of a Ge-GaAs heterojunction. This model is favored because it can explain most transport processes, and only a slight modification of the model is needed to account for non-ideal cases such as the presence of interface traps [37].

Consider the energy-band diagram shown in Fig. 3.7 below.

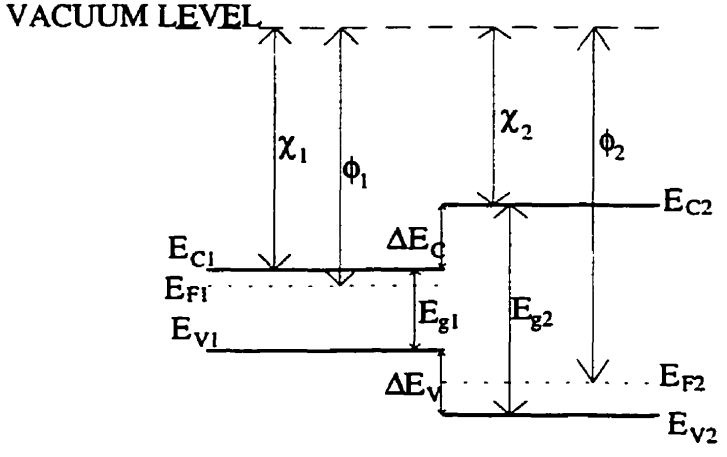


Figure 3.7 Energy-Band Diagram for two isolated dissimilar semiconductors with no surface states.

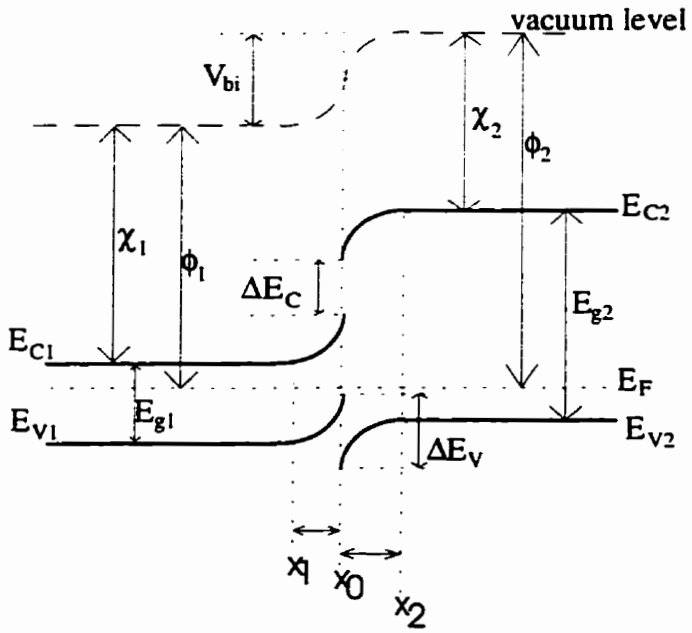


Figure 3.8 Energy-Band Diagram of n-p heterojunction at equilibrium.

This system satisfies the requirement that the Fermi levels must line up at thermal equilibrium. Because of the discontinuities in the band edges at the interface, the barriers to the two types of carriers have different magnitudes. This means that current flowing across a heterojunction will, in most cases, consist almost entirely of electrons or holes [43]. Figure 3.8 shows that the barrier to electrons is considerably higher than that to holes, and so hole current will predominate. The conduction band discontinuity, ΔE_c, equals the difference in electron affinities of the two materials. The transition widths on either side of the interface for an abrupt junction are obtained from solution of Poisson's equation and are given by

$$X_1 = \left[\frac{2}{q}\frac{\varepsilon_1\varepsilon_2 N_A(V_{bi}-V)}{N_D(\varepsilon_2 N_D+\varepsilon_1 N_A)}\right]^{1/2} \tag{3.10}$$

$$X_2 = \left[\frac{2}{q}\frac{\varepsilon_1\varepsilon_2 N_D(V_{bi}-V)}{N_A(\varepsilon_2 N_D+\varepsilon_1 N_A)}\right]^{1/2} \tag{3.11}$$

where ε_1 and ε_2 are the relative dielectric constants of the two materials[41].

3.4.2 Energy-Band Profile of Diamond-Silicon Heterojunction

The electronic properties of diamond and silicon are shown in the table below.

Property	Silicon	Diamond
E_g	1.1 eV	5.5 eV
χ_e	4.01 eV	-2→1 eV

Table 3.1 Electronic properties of silicon and diamond [31]

Diamond is a negative electron affinity semiconductor with the magnitude on χ_e dependent on the crystal plane [40]. The geometry of the SRM diamond tip is such that the contacting surface is not associated with any one crystal plane. This poses the difficulty of approximating the electron affinity of these tips. The fabrication laboratory that produces these diamond tips provided very little information on the properties of these tips. We know that the diamond is heavily doped with boron and annealed to activate the dopants, as well as how the tri-pyramidal shape of the diamond was achieved. We have no information regarding the dopant concentration other than the fact that these tips were used to perform STM experiments. The energy-band diagram shown below describes an isolated p-type diamond and a silicon substrate.

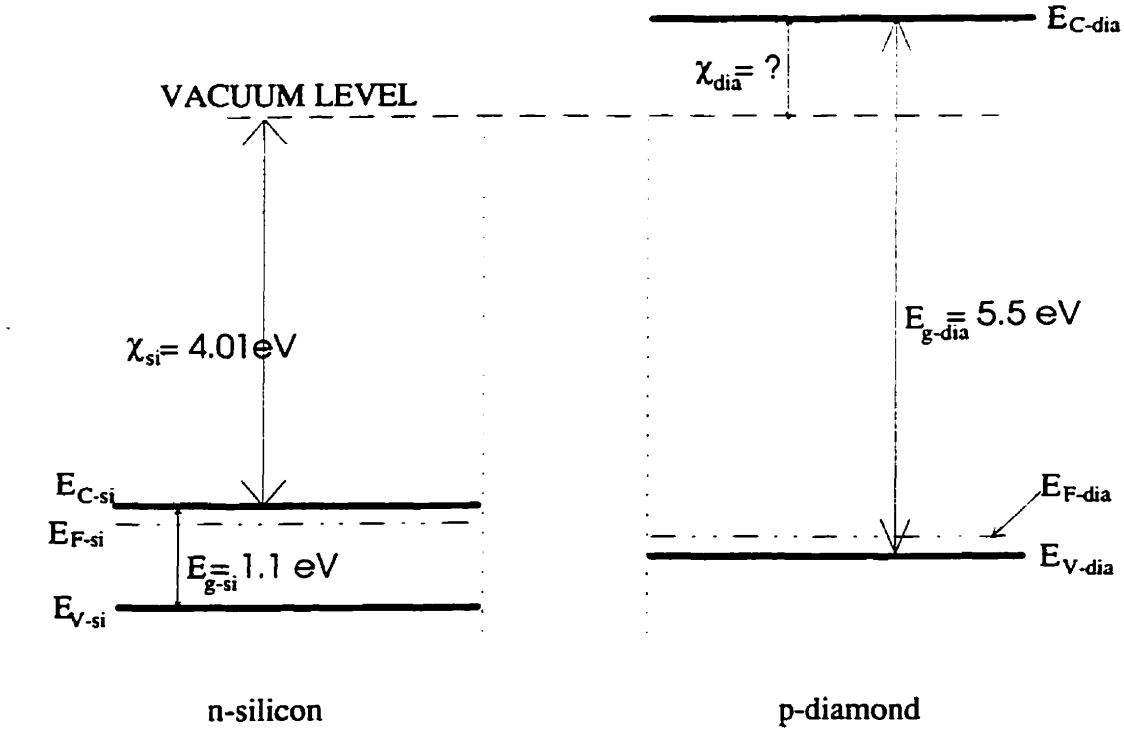


Figure 3.9 Energy-Band Profile for isolated n-Si and p-Diamond. Electron affinity of diamond tip is unknown.

In order to derive a current-voltage relationship that fits observed calibration I-V data for the diamond-silicon contact it is important to develop an energy-band profile that qualitatively explains the observed results. Since this is a heterojunction, it is essential to evaluate the location of each material energy-band profile relative to vacuum level and hence the relationship between the materials' energy levels before and after an electrical contact has been made between them. For a more realistic junction, it is also very important to make an estimate of surface states density effect, interfacial layer and surface termination condition. Ideally, the only parameter that relates semiconductor material energy bands to vacuum is the electron affinity (χ_e). The electron affinity is defined as the minimum energy required to remove an electron from the bottom of the conduction band of the semiconductor to the vacuum level. Figure 3.8 shows that the electron affinity for the diamond is unknown. The literature emphasizes the important *negative* electron

affinity property of diamond which makes the material attractive for photoelectric emission. Since χ_e for the SRM diamond tip is unknown, the energy-band structure of the system will be developed from the calibration I-V spectrum.

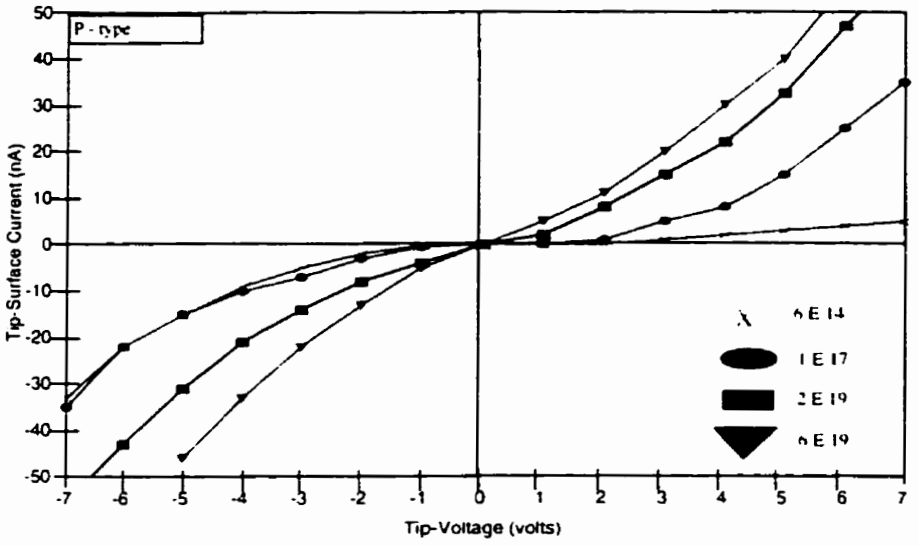
3.4.3 I-V Characteristics of B-doped Diamond-Silicon nanoscale Junctions

Current-Voltage spectra for a diamond tip on a series of uniformly doped silicon substrates of well known dopant concentrations were measured. The dopant density of these standard samples range from 10^{14} cm^{-3} to 10^{19} cm^{-3}, both n and p type. These measurements were performed on Si <100> plane. The surfaces were first polished with colloidal silica solution, then rinsed with de-ionized water, ultrasonically cleaned and rinsed with de-ionized water again. This preparation procedure was followed in order to ensure that the surface preparation on the calibration samples matched that of the research samples that are imaged with the SRM. A few minutes prior to I-V measurements the sample is dipped into a hydrofluoric acid (HF) bath for a several seconds to ensure removal of any native oxide. The tip was rinsed with ethanol.

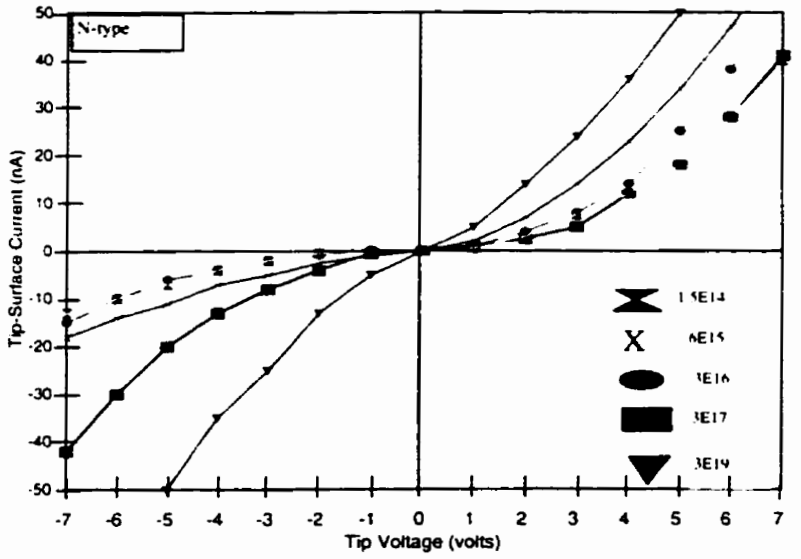
A calibration sample was mounted on the SRM stage in the usual manner, and the force regulation system was activated. A HP 4145A Semiconductor Parameter Analyzer was used to ramp the tip voltage while measuring the junction current in a dark environment. After the tip was brought into contact with the surface, initially the force was adjusted until a repeatable I-V spectrum was obtained. The force was then reduced to the lowest value that still gave a stable contact. Each measurement was repeated three times at the same point on the substrate. The tip was then lifted and the force was verified to check for any drift that could have taken place

during the measurement. This procedure was repeated on at least three different locations on the same surface. The I-V spectra were measured with the force regulated at 1μN.

Initially, the voltage was ramped from -7V to +7V and the data presented on a linear-linear plot. Figure 3.10 (a) and (b) show the I-V spectra for p and n-type substrates respectively. Although these results show that the diamond-silicon heterojunction possesses rectifying properties, the plots do not show enough details at low voltages and low currents. The current at low voltage (below 3V) can be observed if the current axis is a log scale. Furthermore, SRM measurements are performed at voltages below ±3V. This is mainly because the SRM tip tends to modify the surface if the magnitude of the tip voltage is higher than 3V [44]. The modifications are due to field enhanced oxidation of the surface when the tip voltage is below -3V [44]. Figure 3.11 shows sample I-V curves in log-linear plot for the tip on n- and p-type substrates. The rest of the data is presented in appendix A.

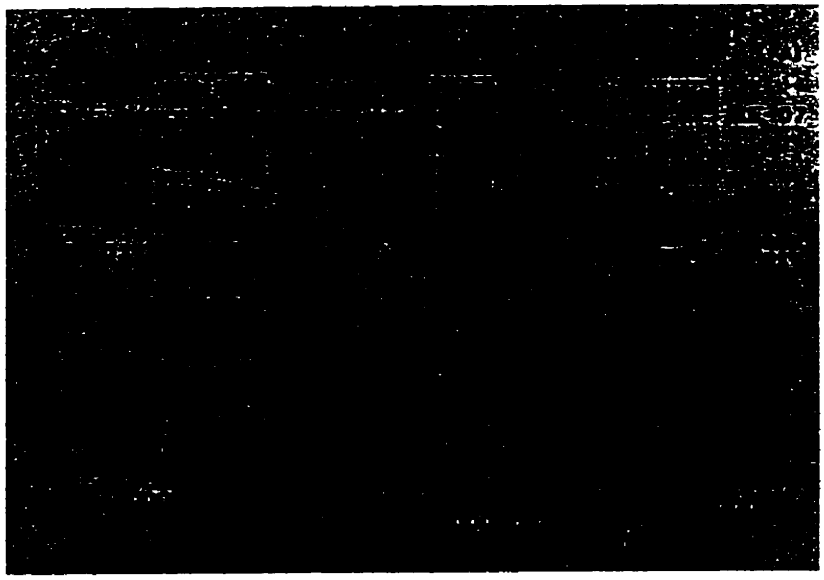


(a)

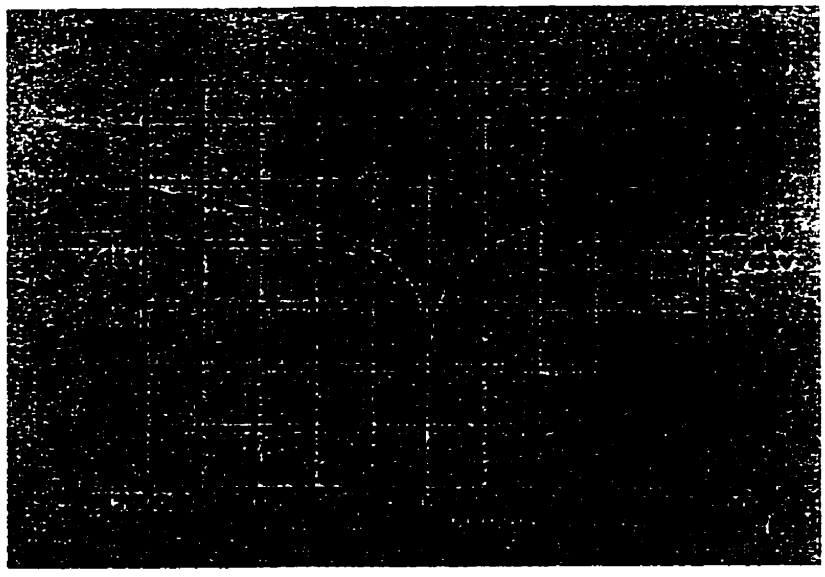


(b)

Figure 3.10 I-V characteristics for p-diamond on (a) p-type (page 63) and (b) n-type silicon substrates (linear plots) showing rectifying property of the heterojunction.



(a) (P: 1.2×10^{17} cm^{-3})



(b) (N: 3×10^{17} cm^{-3})

Figure 3.11 Typical I-V characteristic curves for the diamond tip on (a) P and (b) N type silicon substrates with similar doping concentrations.

Figure 3.11 (a) and (b) show typical I-V characteristic curves for the diamond tip on p and n type silicon substrates with similar doping concentrations. The contact force was set at 1μN for both measurements. Each curve represents the I-V profile at one spot on each surface and measurement taken three times to ensure repeatability. Fig. 3.11 (a) shows lower current when the tip is positively polarized with respect to the p-type substrate than the junction current when the tip is negatively polarized. This asymmetry is indicative of a rectifying junction where a positive voltage on the probe tip reverse biases the junction while negative voltage forward biases the junction. An order of magnitude difference in current at two corresponding tip voltages and opposite polarity is observed here. Conversely, Fig. 3.11(b) shows that a negatively polarized tip on an n-type substrate results in less junction current compared to a corresponding positive tip junction current. This implies that a negative tip reverse biases the junction while a positive tip forward biases it. However, the asymmetry in this latter case is not as obvious as that in the former case. A total of 18 I-V curves for each doping type were taken on six different doping concentrations. The results are summarized in Fig. 3.12. From each I-V curve three current levels ±1, ±5, and ±10 nA were chosen and the corresponding voltage values read. An average of the voltage values read from the three I-V curves obtained for each doping concentration was taken to make up one data point and the results plotted below.

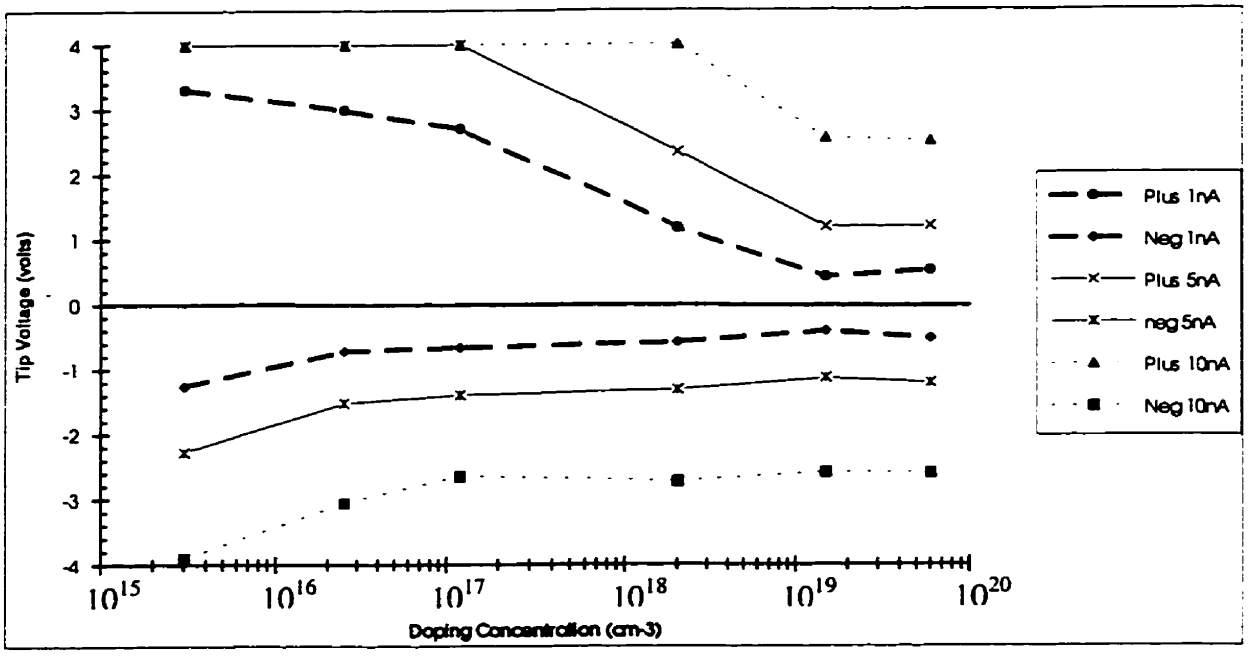


Figure 3.12 (a) SRM diamond tip-Silicon substrate **I-V** calibration curves on P-type substrate. These curves show the tip voltage required to cause ±1, ±5, and ±10 nA junction current to flow as a function of substrate doping.

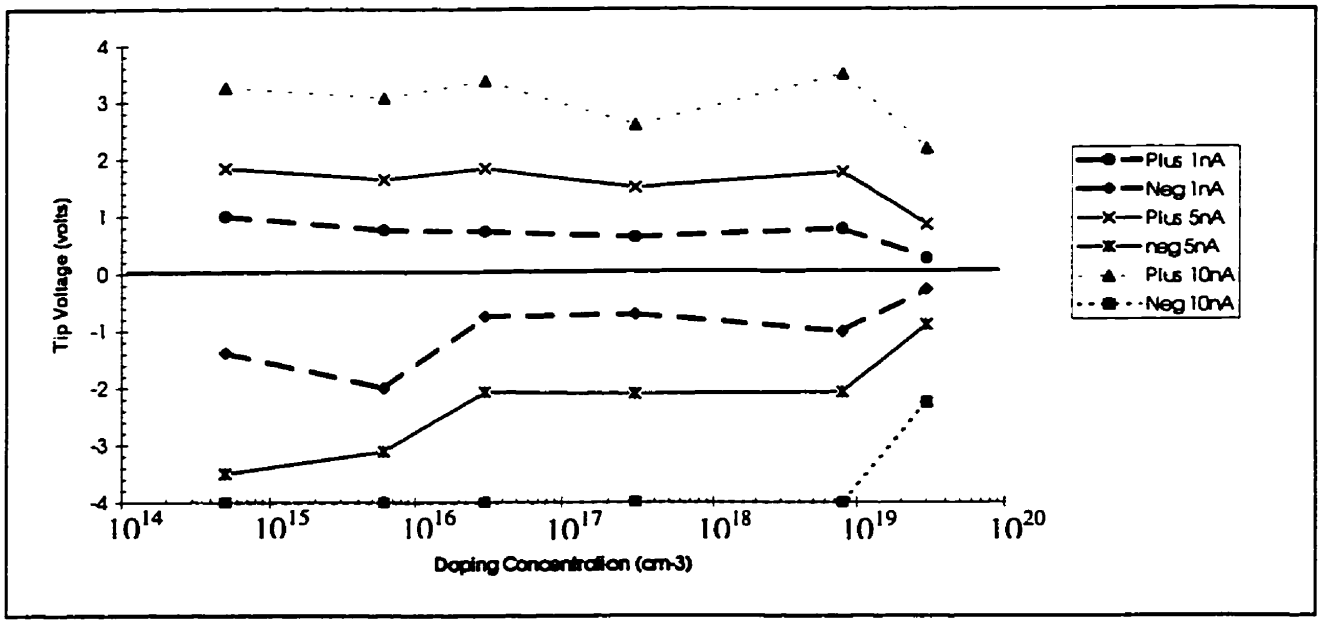


Figure 3.12 (b) SRM diamond tip-Silicon substrate **I-V** calibration curves on N-type substrate. These curves show the tip voltage required to cause ±1, ±5, and ±10 nA junction current to flow as a function of substrate doping.

Figure 3.12 (a) demonstrates two properties of the diamond-P-type silicon heterojunction: Firstly, more junction rectification occurs at lower doping compared to higher doping. This is demonstrated by the asymmetry between each pair of curves. Secondly, I-V curves for negative probe polarity are not very sensitive to substrate doping whereas positive probe polarity I-V curves discriminate between different substrate doping concentrations. However, at very low doping levels, negative probe I-V curves show a small degree of sensitivity to substrate dopant density.

Figure 3.12 (b) shows two characteristic features of the junction: Firstly, very little rectification of the diamond-N-type silicon heterojunction is observed. The asymmetry between corresponding curves is not very obvious at mid and high substrate doping levels. Secondly, although negative probe bias does not give as much junction current as positive bias, both polarities are not very sensitive to substrate doping levels. Negative probe polarity starts to discriminate between substrate doping at levels below 1×10^{16} cm^{-3}. However both polarities show a dramatic drop in voltage at all three currents when the substrate doping level is greater than 1×10^{19} cm^{-3}.

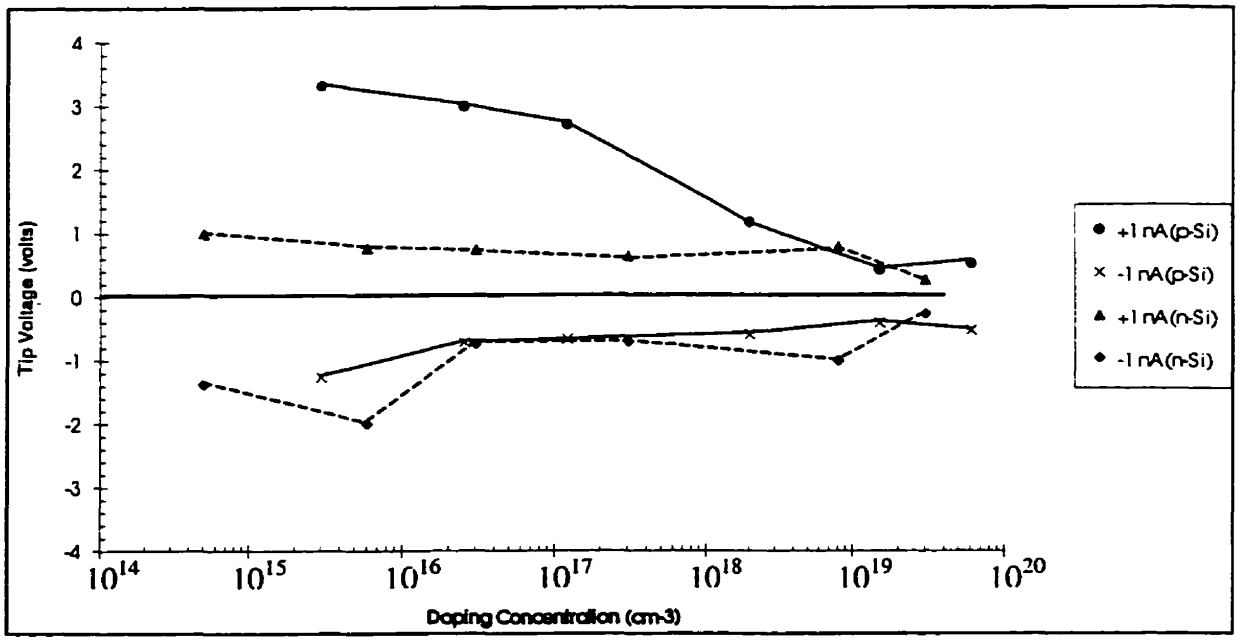


Figure 3.13 A comparison between N and P-type heterojunction calibration curves illustrating how voltage contrast are obtained during SRM constant current (1 nA) imaging across P-N junctions and dopant profiling.

Figure 3.13 is an illustration of tip voltage modulation in order to maintain a constant junction current of 1nA. This figure also demonstrates that positive tip voltage offers better SRM performance when performing p-n junction delineation than negative tip voltage. Although the curves overlap at high doping, p-n junctions are located at the lower doping concentration end where the curves show better discrimination between N and P type. As shown by Figure 3.12 (a) and (b), at a higher set point current (5 nA) the SRM performance is better. However, since the SRM dynamic range is limited to ±3V, higher set point current results in saturation.

The results shown above suggest that while the SRM diamond tip is sensitive to p-type doping, it is not very sensitive to N-type substrates. This is an indication that there is a depletion region on P-type substrates. Furthermore, this suggests that the bottom of the valence band of the diamond tip is located near or above the middle of the silicon band gap.

3.4.4 Capacitance Derivative ($\partial C/\partial V$)

The properties of the heterojunction were further investigated by measuring the differential capacitance of the space charge region at the junction. As shown in Appendix B, $\partial C/\partial V$ is proportional to the relative dopant densities of the tip and substrate. Therefore measurements of $\partial C/\partial V$ as a function of the substrate doping concentration for both N and P-type provides further insight regarding the junction barrier. Specifically, this measurement provides more information about the side in which the depletion width is larger for N and P type substrates. Although other aspects of the results presented in Appendix B are consistent, such as the sign of $\partial C/\partial V$ on n and p-type substrates, with regards to depletion width investigation these results are inconclusive. It is suspected that the problem may have been lack of good back contact to the substrate for lower dopant density substrates. Perhaps a self contained sample could solve the problem.

3.5 A PROPOSED BAND MODEL FOR p-Dia-Si HETEROJUNCTION

In order to explain current transport mechanisms across the heterojunction formed between boron doped single crystal diamond tips and silicon surfaces (both N and P type), it has been necessary to determine the energy band model on the basis of experimental data. Current-voltage characteristics and capacitance derivative data have been used in estimating unknown electronic parameters such as the electron affinity for the diamond tip.

Previously, there have been proposed band models for polycrystalline diamond and N and P type silicon [45]. Toempong Phetchakul et al. studied the rectification characteristics of p-type

diamond on N-type silicon heterojunctions. Their analysis of I-V curves obtained at different ambient temperatures led to the conclusion that forward and reverse currents for their system were diffusion and tunneling currents, respectively. With their analysis, Toempong Phetchakul et. al. proposed an energy band model that could suitably explain their experimental results qualitatively. This model uses diamond electron affinity of +0.5eV.

The doping concentration for the diamond tip used for the present work will be approximated at 10^{19} cm^{-3}. This approximation is based on the work done by a research group [12] using similar tips. Figure 3.14 shows a proposed energy band diagram for the present p-diamond and silicon heterojunction.

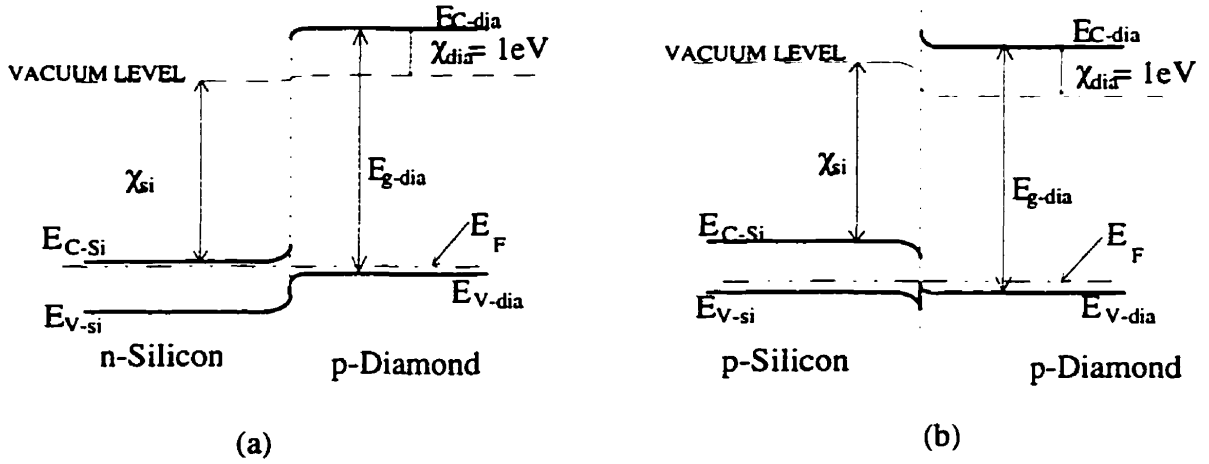


Figure 3.14 A proposed energy band diagram for P-type diamond tip on (a) N-type and (b) P-type silicon heterojunction at thermal equilibrium.

3.5.1 Current transport across the heterojunction

Current-Voltage characteristics show that for p-diamond on P-type silicon a higher current flow across the junction is observed at a negative probe bias voltage compared to that observed at a positive probe voltage of the same magnitude. This behavior implies that negative probe bias forward biases the junction, whereas positive probe bias reverse biases it. This

phenomenon can be explained with the aid of the proposed energy band model shown in Fig. 3.14 (b). This Figure shows a space charge layer on the p-Si side. Figure 3.15 shows the band structure when the tip is positively biased with respect to the substrate. This bias condition enhances the depletion width from W_o to W_1. The reverse current is due to recombination-generation of electrons and holes from traps within the depletion region. If the polarity is reversed the junction is forward biased. In this case the dotted E_{c1} and E_{v1} will be below E_{co} and E_{vo} respectively. This will reduce the height of the hole barrier and the depletion width.

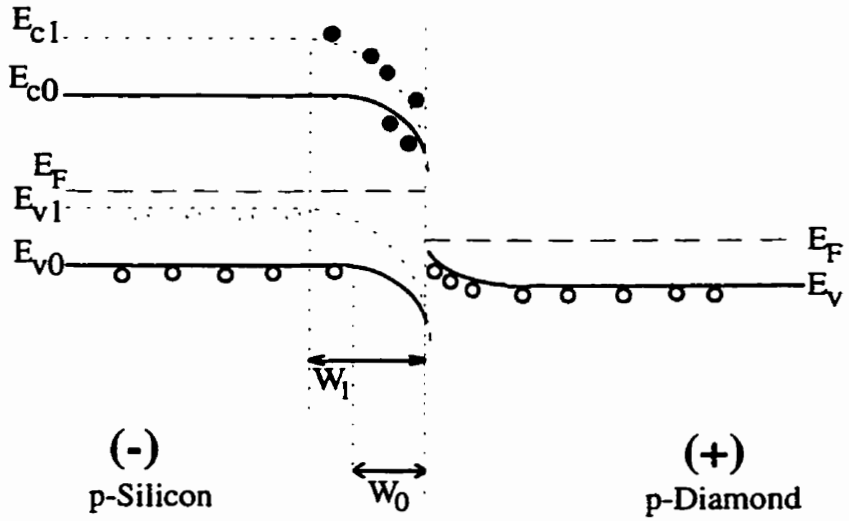


Figure 3.15 An energy band diagram for a reverse biased p-diamond on p-type silicon. Solid lines show the band structure before bias and dotted lines after reverse voltage is applied.

Figure 3.14 (a) is used to explain I-V data obtained from p-diamond tip on n-type substrates. This will be illustrated by Figure 3.16 for a reverse biased heterojunction.

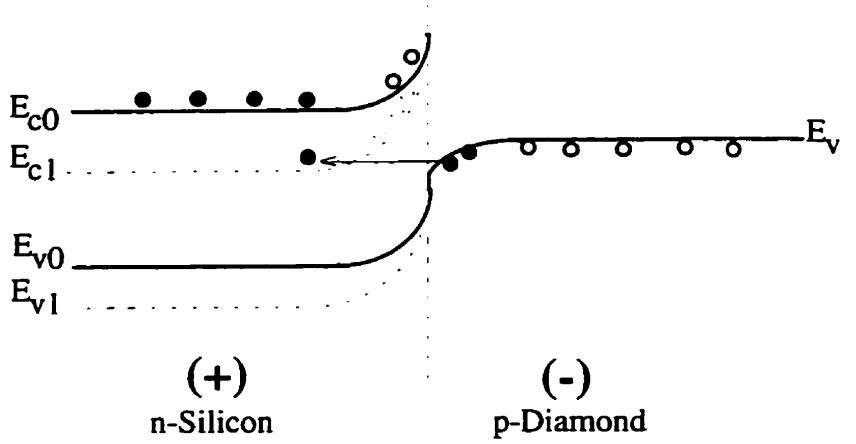


Figure 3.16 An energy band diagram for a reverse biased p-diamond on n-type silicon. Solid lines show the band structure before bias and dotted lines after reverse bias is applied.

Figure 3.16 shows the band structure for the tip negatively biased with respect to the substrate. Under this bias condition, the bottom of the conduction band in n-Si overlaps with the top of the valence band in diamond. It appears that reverse current under such a bias condition may result from electrons tunneling from the valence band in diamond into the conduction band in silicon. However, this process should only occur for very heavily doped silicon. The symmetry observed between positive and negative probe bias voltages suggests that there may be another mechanism limiting the flow of current across this junction. A good candidate would be "space–charge–limited" (SCL) currents. However, calculations using using fairly conservative estimates of parameters for the junction show that, at best, the resistance resulting from SCL is of the order of 10^6 Ω. This resistance is insignificant compared to the junction **contact** resistance (10^9 Ω).

3.6 CONCLUSION

A heavily doped diamond tip was used to measure I-V characteristics of the heterojunction formed between single crystal diamond and n and p-type silicon substrates. The results obtained

in this study show a non-linear relationship between the current and voltage for the diamond-Si heterojunction. When the tip is placed on p-type silicon and a positive voltage applied to the tip with respect to the substrate the junction appears to be reverse biased. Negative tip voltage appears to forward bias the junction. The opposite is true when the tip is positioned in contact with n-type substrates. It is concluded therefore that the heterojunction is rectifying. Furthermore, reverse current flowing across the p-diamond/p-Si interface is sensitive to silicon dopant concentration while the forward current is not as sensitive. However, the rectification of p-diamond/n-Si heterojunction is not very obvious. The results suggest that there may be another current limiting mechanism present at this junction. Although simple calculations show that "space-charge-limited" current is unlikely, lack of further information to carry out a thorough analysis leaves SCL as a possibility. While the diamond/p-Si junction shows an order of magnitude difference between forward and reverse currents at a doping concentration of 10^{17} cm^{-3}, the diamond/n-Si junction only shows half an order of magnitude difference at the same doping level. Analysis of the I-V data leads to the proposed energy band model shown in Fig. 3.15. This band model can explain most but not all the features of the observed data.

The current-voltage results show that when a positive bias is applied to the diamond tip, the SRM operating in constant current mode is capable of performing P-N junction delineation as demonstrated by the calibration curves in Fig.3.12 and 3.13. These results also show that the measurement dynamic range for SRM carrier profiling on P-type silicon is 10^{15} cm^{-3} to 10^{19} cm^{-3}. It should be noted that the calibration performed in this study was done using **one** diamond tip due to scarcity of these tips. In order to confirm the validity of the band model proposed here it is necessary to use a large enough sample of tips that were fabricated using the same technique.

CHAPTER 4
IMAGING OF SEMICONDUCTOR DEVICE CROSS-SECTIONS

4.1 INTRODUCTION

This chapter presents several examples of device cross-sectional imaging by constant current mode SRM. The results presented here were taken from cross-sections of the following semiconductor devices and test structures; MOSFETs, Bipolar junction transistors, Silicon-On-Insulator structures, MBE grown SiGe multilayer structures, MOSFETs with asymmetric source/drain for EEPROM cells. In chapter 5 I will present SRM results obtained from 0.4 μm gate MOSFET. This test structure is part of an international round-robin project that is organized by SEMATECH for evaluating dopant profiling instruments.

These examples demonstrate the instrument ability to

1. perform true **two dimensional** imaging on sample surfaces
2. image and show clear resistance contrasts between **insulating**, **semiconducting** and **metallic** regions on device cross-sections
3. **delineate** between regions of different dopant type thus locating **p-n junctions**
4. **delineate** between **heavily** doped and **lightly** doped regions of a semiconductor
5. image with **nanometer scale spatial resolution** on device cross-sections
6. image real **state-of-the art** CMOS and BIPOLAR devices

The results obtained from imaging polished device cross-sections have been found to be very repeatable and consistent between experiments. If a sample is suitably fabricated for SRM imaging, that is, all regions of the devices of interest are electrically shorted to a common contact, mounting of sample on stubs and polishing may take up to six hours (representing more

than half of the turn-around time). It may take up to an hour to locate the SRM tip on a required device. Once the SRM tip is located at the desired location it takes about two minutes to acquire two complete images each of size 256×256 pixels. Data analysis is done on a SUN workstation using an image processing program that was developed by our group.

4.2 TYPICAL SEMICONDUCTOR DEVICES AND THEIR FABRICATION

Fabrication of semiconductor devices is a process that involves many steps of mask material deposition on a surface and depositing impurity atoms in unmasked regions. The processes that are used in fabrication of devices and integrated circuits can be categorized into **oxidation, diffusion, ion implantation, photolithography, epitaxy, metalization and interconnections.** Introduction of impurity atoms into selected regions of a wafer is performed either by high energy ion implantation or diffusion of impurity atoms.

In the case of diffusion, most of the solid-state diffusion processes occur in two steps namely *predeposition* and then *drive-in* diffusion. In the predeposition step, a high concentration of dopant atoms are introduced at the semiconductor surface by a vapor that contains the dopant atoms at a high temperature (about 1000 °C). The impurity atoms, which are incident on the surface, diffuses into the semiconductor because of their concentration gradient into vacant lattice sites. This results in a shallow but heavily doped layer. The second step of diffusion, drive-in, is used to drive the impurity atoms at a higher temperature (about 1100 °C) deeper into the surface. This step does not introduce any more dopants, and hence reduces the surface concentration of the dopants. The diffusion depth is controlled by the *time* and *temperature (to*

within 0.25 °C) of the drive-in process to obtain accurate junction depth (to within a fraction of a micron).

Ion implantation is a process of introducing dopants into selected areas of a semiconductor surface by bombarding the surface with high-energy ions of the particular dopant. The dopants are ionized in a gaseous state and accelerated to about 20 keV. Mass spectrometry techniques are used to separate the dopant atoms from unwanted ionic species that may have been ionized and accelerated with the dopant ions. The dopant ion beam is further accelerated so that their energy reaches several hundred keV, whereupon they are focussed on and strike a semiconductor surface. Upon entering the wafer, the ions loose their energy through collisions with electrons and nuclei of the semiconductor. Several advantages of ion implantation include precise control of doping level, easy regulation of dopant depth (capable of very shallow penetration), extreme purity of the dopant ion current, very accurate junction depth and limited diffusion of dopants as this is a low temperature process. Major disadvantages include crystal damage to the semiconductor (the crystalline structure may be restored by furnace annealing) and financial implication of the process because of its complexity. A brief high temperature (600→1000 °C) annealing process activates the impurity atoms. The anneal process results in diffusion of dopants.

SRM is used to map out profiles of carrier density and type that result from implanted and/or diffused dopants. The MOSFET cross sections studied in this work were fabricated by the Nortel (Ottawa) 0.8 μm BiCMOS process[46].

Typically, the starting substrate for the Nortel BiCMOS process is lightly doped (15 ohm-cm) p-type silicon with <100> crystal orientation. With the appropriate pattern of masks, a buried n^+ layer is then formed by ion implantation (antimony implant) followed by a high

temperature anneal to activate the impurities. During the anneal step surface oxidation is performed to introduce an alignment mark for the next masking level. The masked regions are subsequently exposed to another ion implantation step (boron implant) to form a buried p^+ layer. A weakly doped thin epitaxial silicon layer is grown on top of the buried layers to form n and p wells: Isolation structures such as Poly Buffered Local Oxidation of Silicon (PB LOCOS) are then formed followed by formation of device wells. A thick field oxide is grown and a n^+ sinker is formed from high dose phosphorus implant. The purpose of the n^+ sinker is to provide low resistance link to the buried layer in order to minimize collector resistance in bipolar devices. A high quality thin gate oxide (17.5 nm) is grown followed by gate poly for the MOSFETs. A photoresist mask is used during a moderate phosphorus doping to form lightly doped drain regions. The purpose of the LDD is to reduce the peak electric field and hence the generation rate of hot carriers near the drain end of the channel. A drive in step allows the LDD region to extend toward the gate controlled region. Moving the junction under the gate, and moving the point of peak electric field away from the surface are known to be the key in improving device reliability. Deep graded junctions are not suitable for sub-micron MOSFETs hence device performance design would ideally involve no LDDs at all. In order to reduce short channel effects, side wall spacer oxides are formed that space the heavily doped n^+ region away from the channel region.

Figure 4.1 shows a schematic drawing of a typical CMOS device structure with source/drain extensions.

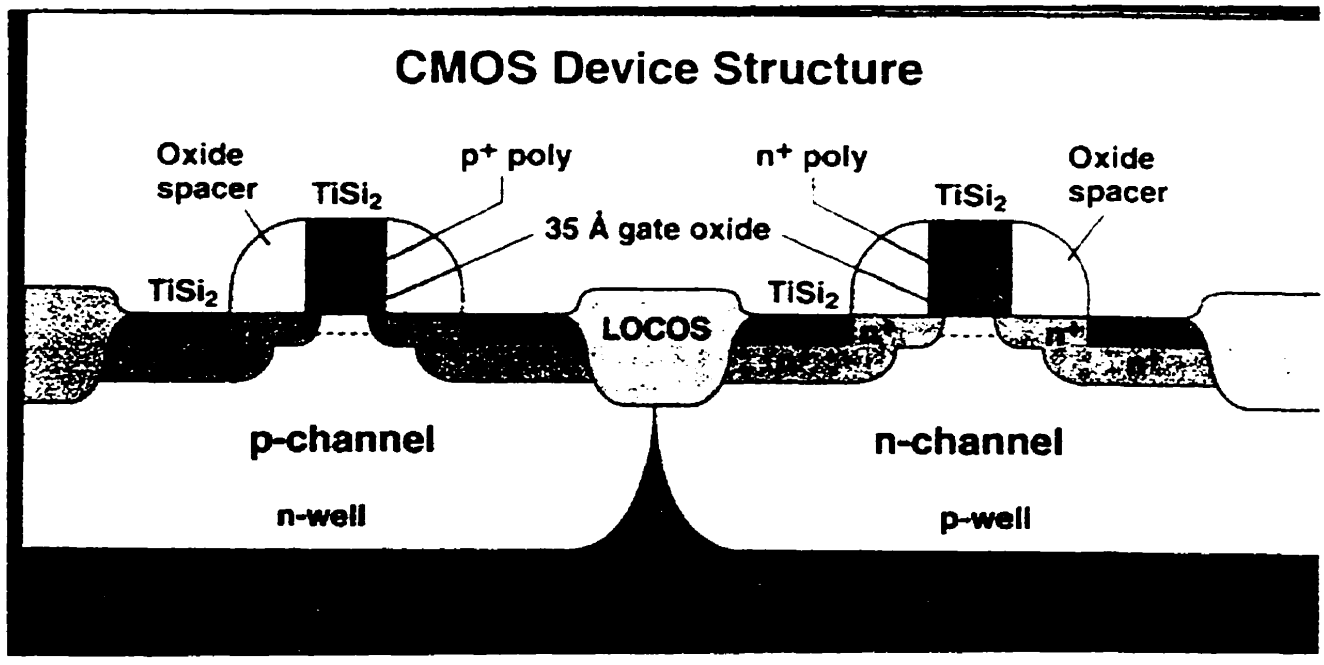


Figure 4.1 Schematic of a CMOS device structure cross-section with source/drain extensions.

4.3 IMAGING MOSFET CROSS SECTIONS

The sample used in this study was prepared at Nortel (Ottawa) and is a standard sample for Scanning Electron Microscopy (SEM) cross-section analysis. In this section, results from SRM imaging of MOSFETs using boron-doped diamond tips will be presented. The resolution obtained in these results will be compared with that obtained with metal tips (Tungsten). When contrasted with SEM images of the MOSFETs, provided by Nortel, the SRM profiles reveal tip artifacts that are associated with dimensions and aspect ratio of the diamond tip.

Figure 4.2 shows an SRM profile of a MOSFET obtained with a Tungsten tip. This image shows the different regions of the device as well as some doped layers in the region below the device. However, there is no clear definition of the boundaries between source/drain and substrate or even the gate. The resolution in this image is not good enough to make quantitative

spatial resolution measurements. While Fig.4.2 shows the MOSFET structure with all regions identifiable, the image is quite patchy. This is a good demonstration of resolution degradation by imaging with a tip that has either been contaminated by picking up debris and/or become blunt through losing pieces of the tip during the scan.

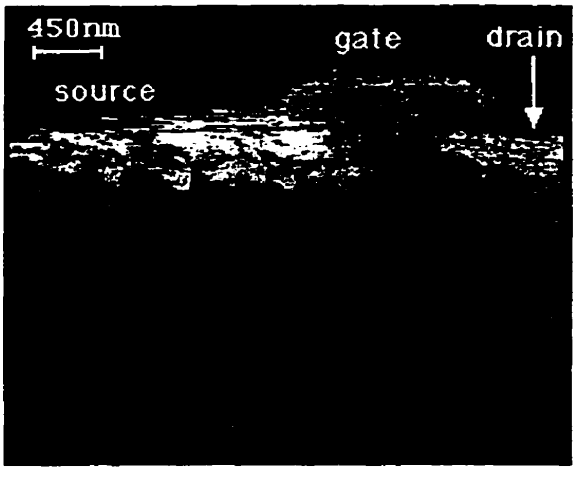


Figure 4.2. An SRM image of a MOSFET obtained with a tungsten tip. This image shows a close view of the source, gate and drain regions. The threshold current was set at 200nA.

Figure 4.3 (a) and (b) shows an SRM profile and the corresponding topographical profile of a n-channel MOSFET with a Lightly Doped Drain (LDD) respectively. These two images were taken simultaneously. In the SRM profile brighter regions on the gray scale represent lower contact resistance while darker regions represent higher contact resistance. Clearly the source/drain regions can be identified on either side of the gate in Fig. 4.3(a). Most of the bright region on the source/drain is attributed to a silicide that is grown in these regions for purposes of making an ohmic contact. A higher resolution view of these regions, shown in Fig. 4.4 (a), shows the silicide grown on the polysilicon gate. Below the device in Fig. 4.3(a) is the silicon substrate shown by a darker shade. The very dark region above the source/drain and gate level is the inter-metal dielectric in which the metal layer can be observed above the source/drain region. In the

topographical profile, Fig. 4.3(b), the field oxide is elevated compared to the inter-metal dielectric. We attribute this to preferential removal of the lower quality inter-metal oxide by polishing and the final cleaning step (5 seconds hydrofluoric acid dip) prior to imaging the sample. The substrate and the gate are also elevated relative to the inter-metal dielectric.

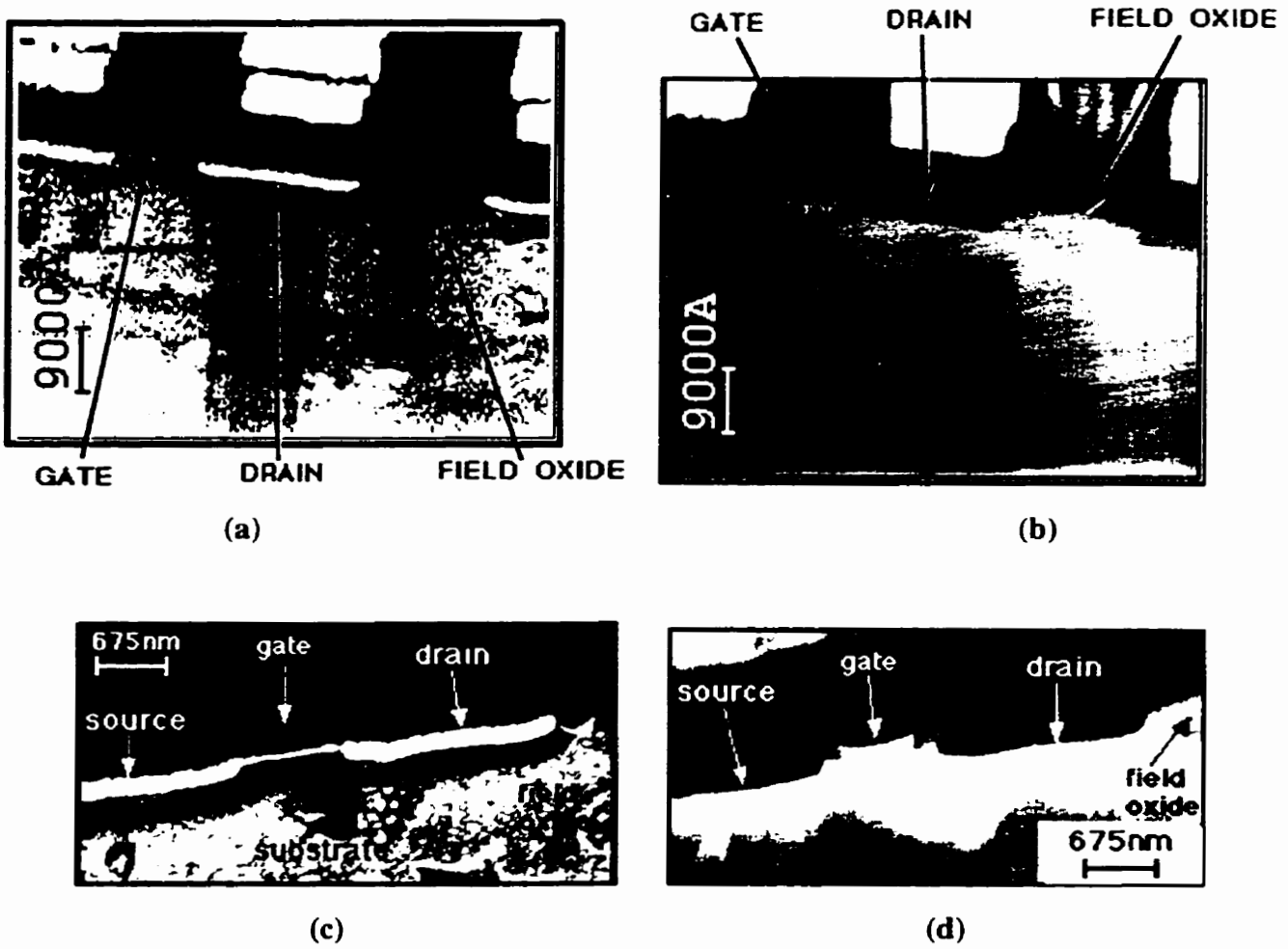
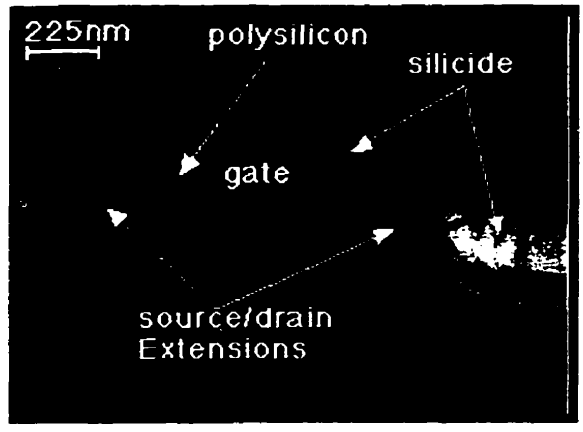
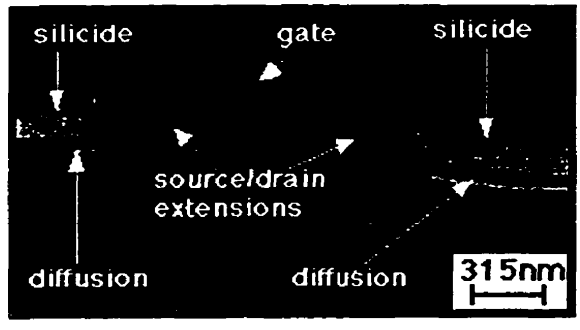


Figure 4.3 SRM images of an n-channel MOSFET showing; (a) and (c) SRM profiles and (b) and (d) the corresponding topographic profiles. The metal inter-connect is shown in (a) and (b) as large bright regions above the source/drain.



(a)



(b)

Figure 4.4 Higher resolution images of a MOSFET showing (a) the resistance profile of the gate (polysilicon and silicide delineation), source/drain (diffusion and silicide delineation), and (b) lightly doped drain extensions into the region underneath the gate.

4.3.1 Interpretation of Results

This section provides a description and discussion of the several features observed in Fig.4.4(a). This image shows details of the MOSFET such as the silicide-polysilicon delineation in the gate and silicide-diffusion delineation in the source/drain regions. The source/drain diffusion extends about 0.12 μm beyond the silicide. This image also shows the lightly doped drain extensions into the region underneath the gate. The very dark region above the device is the inter-metal dielectric (an insulator), and the region below is the silicon substrate. Between the gate region and the substrate there is a thin high resistance (dark) region. There are at least two possible reasons for this dark region: (1) there may be a depletion of carriers under the gate. (2) there is an artifact that couples topographic features into the resistance image and since the gate is at a different height compared to the substrate we expect to see this artifact in this region. Under the gate we expect reason (2) to be the dominant one. In future work we will be conducting experiments where the gate potential can be independently controlled to check the magnitude of (1). With control of the gate potential we may also be able to observe the inversion layer in this structure. Underneath the source/drain regions there is also a dark region that is the result of carrier compensation or the topographic coupling artifacts. Figure 4.4 (b) shows an SRM profile of the same MOSFET demonstrating the presence of the lightly doped drain structures on both sides as well as the shape of the LDD in comparison with Fig.4.1.

The SRM profiles are contrasted with an SEM image in Fig.4.5. The SEM image was taken from a cleaved cross-section of the n-channel MOSFET (courtesy of M. Simard-Normadin, Nortel (Ottawa)). This image shows the polysilicon gate, the silicides on the source/drain and on the gate, the gate oxide and the less obvious oxide-spacers on either side of the gate. The gate length is measured to be ≈560 nm, silicide thickness on the gate and source/drain is ≈46 nm,

and the thickness of the polysilicon gate is ≈230 nm. Figure 4.4(a) shows a thicker silicide in all regions than that shown by the SEM image. The explanations for this are related to the finite radius of the tip. Since the gate is topographically higher than the inter-metal dielectric (as shown in Fig.4.3 b), the side of the tip makes contact with the silicide before its bottom reaches the edge of the silicide. This shifts the actual edge of the silicide towards the inter-metal dielectric. Figure 4.6 shows that the thickness of the polysilicon is consistent with that obtained from the SEM image. The SRM image gives a channel length of ≈800 nm. We believe that the discrepancy with the SEM image channel length is due to uncertainties in calibration and non-linearity of the SRM piezoelectric scanner.

Figure 4.6 shows conductance level profiles taken across the drain (open circles) and the gate (filled circles) of Fig.4.4(a) starting from the dielectric. The drain profile shows higher conductance level in both the silicide and the diffused region compared to the gate profile. A rapid drop in the conductance level is observed just below the gate and drain. The substrate conductance level is approximately the same in both profiles as expected. We obtain a conservative estimate of the spatial resolution to be ≈ 20 nm from Fig.4.4. We believe that the coupling artifact and the tip size are the most significant limiting factors to the resolution.

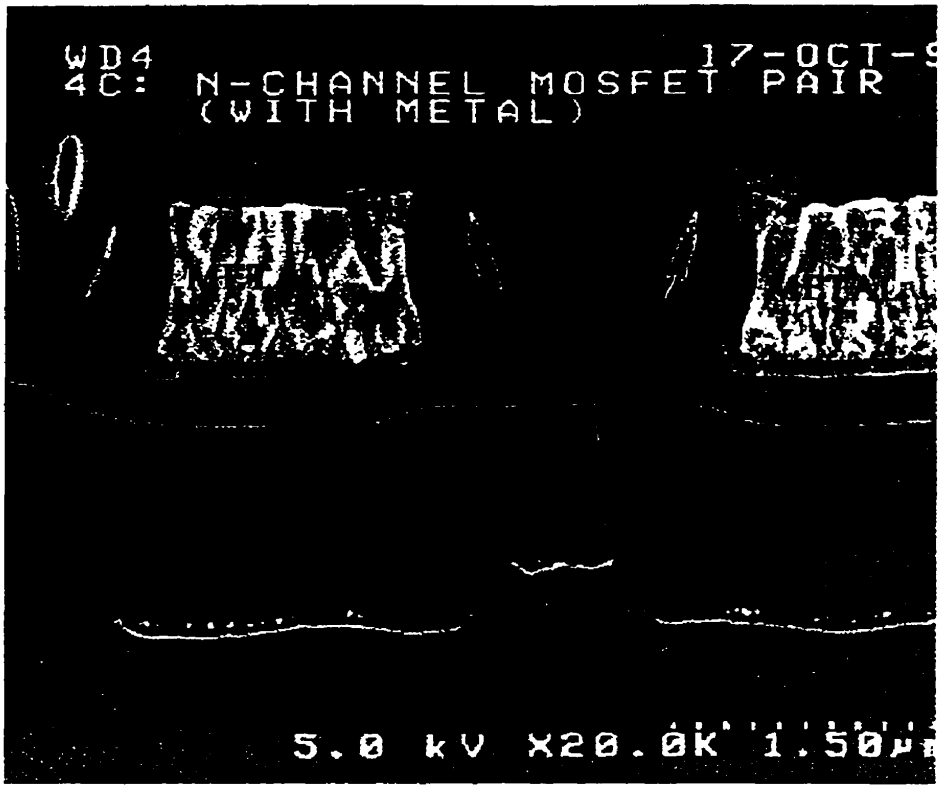


Figure 4.5 An SEM image of a MOSFET cross-section showing the silicides, polysilicon gate, gate oxide, substrate and inter-metal dielectric. This image was provided by Nortel (Ottawa).

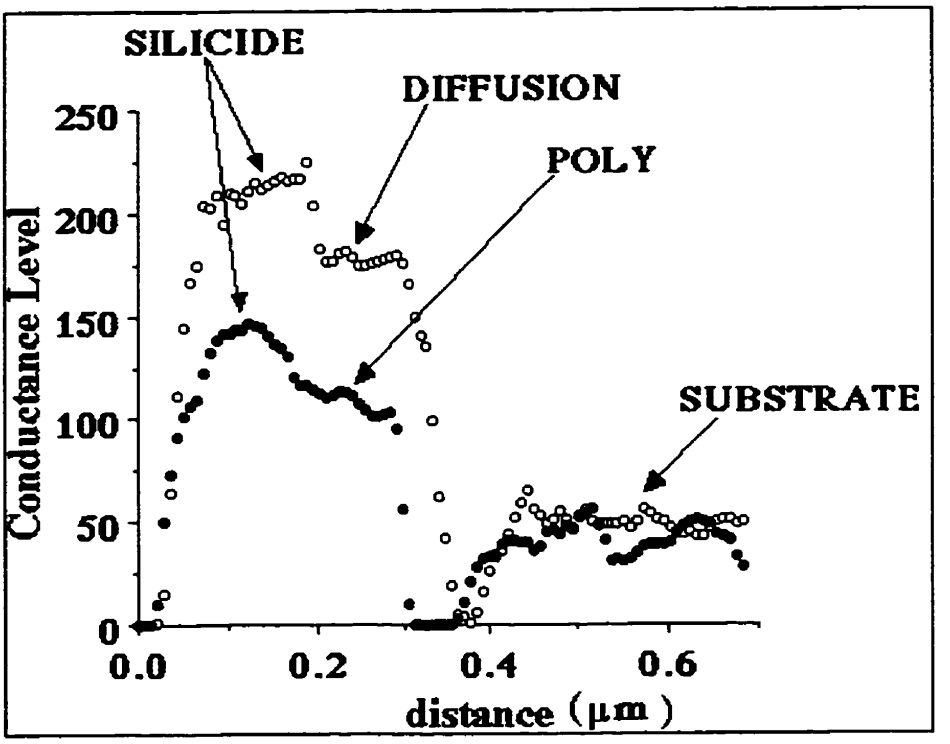


Figure 4.6 Conductance level cross-sections starting from the inter-metal dielectric extending across the gate (filled circles) or across the drain (open circles) of Fig.4.3(a) into the substrate.

4.4 SILICON ON INSULATOR (SOI)

Figure 4.7 shows a diagram of a beveled (11°) SOI structure with a large back contact. The ultimate goal of this experiment is to image a cleaved cross section of this structure and use it to measure the resolution of the SRM versus applied force, probe material, etc. Beveling the structure enhances the lateral resolution by a factor of 5.24 This structure has been imaged on the bevel to show the contrast of imaging an insulator versus p-type silicon.

The SOI structure, prepared by Silicon On Insulator Technologies (SOITEC), consists of a 0.4 μm oxide layer buried approximately 0.2μm below the silicon surface. Preparation involved implanting an extremely high oxygen dose into a p-type substrate at high current followed by a high temperature anneal to allow a segregation of the implanted oxygen into a buried oxide layer.

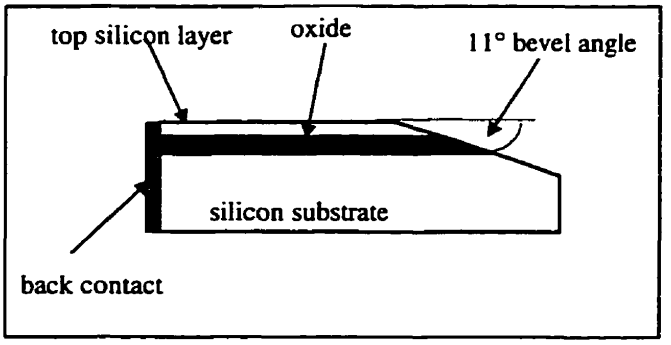


Figure 4.7 Schematic diagram of silicon on insulator structure with the top p-type silicon layer being 0.2μm, the oxide layer is 0.4 μm on the cross section.

In order to perform SRM imaging all the three layers were electrically connected to the back contact at one end as shown in Fig.4.7. Figure 4.8 shows an image of the beveled region of the SOI structure at one edge of the sample. This figure shows the three layers, the bright region is the silicon top layer, the dark region is the buried oxide layer, and the substrate is at the top

right corner of the image. For this SRM image brighter regions represent lower resistance than darker regions. The oxide layer indicates higher resistance than the top layer and the bulk. Since the sample was beveled, the SRM can easily resolve the different layers.

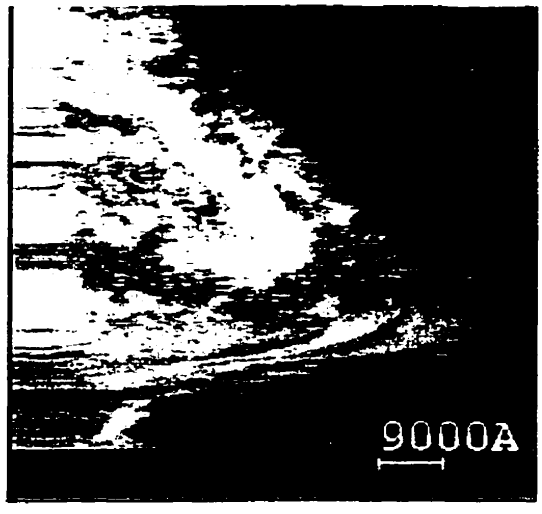


Figure 4.8. SRM image of a beveled SOI structure showing the oxide layer as a dark region "V" shaped at the bottom right hand corner, the top silicon film as the bright region on the left and the bulk silicon as the bright region at the top right hand corner. The threshold current was set at 90nA.

On the SRM image we measured $\approx 1.8\ \mu m$ as the width of the buried oxide (shown in dark on the greyscale). The SRM measurement is quite close to the expected 2 μm width of the buried oxide on the bevel. The discrepancy is attributed to the physical dimensions of the tip, inaccuracy in the bevel angle, and sample cleaning (hydrofluoric acid (HF) dip) before imaging. Notice at the bottom right hand corner of the figure the "V" shaped region. This part of the image corresponds to the edge of the beveled region and clearly demonstrates the two dimensional capability of this technique. However, the bottom edge of this oxide layer is quite rough as a result of sample preparation.

4.5 IMAGING BIPOLAR DEVICE CROSS SECTIONS

In this section a discussion of two bipolar junction transistor cross-sections is provided. One is a research structure provided by Nortel (Ottawa) referred to as the "front end SEM stripe"(FE SEM) and the other is a real device structure from a contract project that I did.

4.5.1 BJT from FE SEM stripe structure (Nortel)

MOSFETs and BJTs fabricated by Nortel 1 μm process have been imaged with the SRM. This is a standard test structure that has been used by Nortel for cross-sectional SEM analysis. These devices are fabricated in such a way that they extend along their width far enough to allow multiple cross-section polishing without losing them. Metal 1 layer is fabricated so that all regions of each device are electrically shorted together, making the structure suitable for SRM imaging. A SEM image of a polished BJT cross-section of the FE SEM stripe is shown in Fig. 4.9.

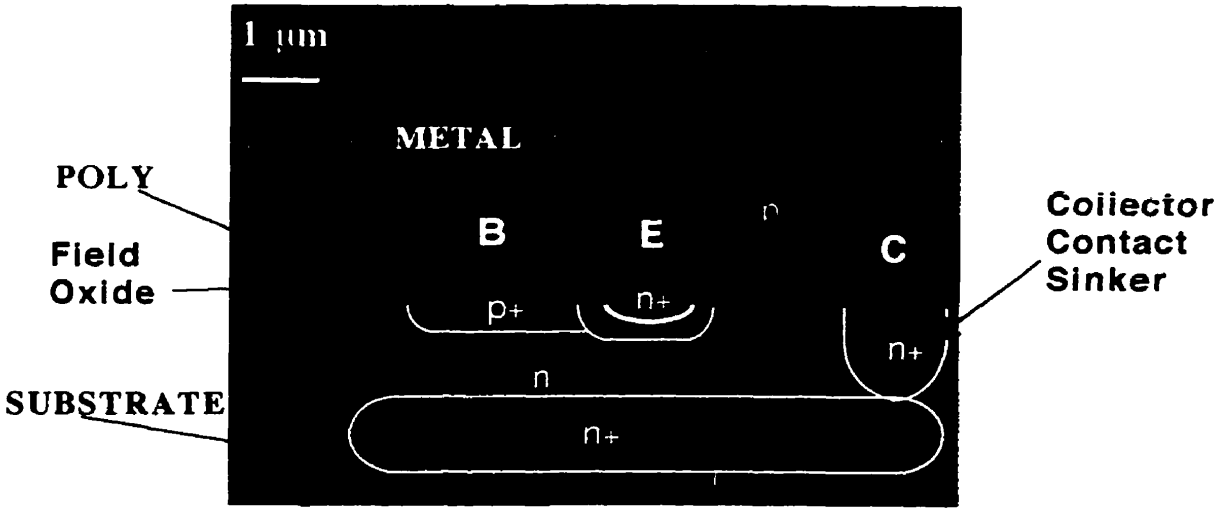


Figure 4.9 A SEM image of a FE SEM stripe bipolar transistor cross-section. The white lines mark expected boundaries of the different device regions.

This SEM image shows contrasts on the greyscale that are associated with topographic profile. It does not show contrasts that are associated with dopant profiles within the device. White lines have been drawn on the image to indicate the expected positions and shapes of doped regions of the BJT such as the P^+ base, P^- base, emitter and collector. Since these are test structures, there may be some slight differences between these devices and real state-of-the-art BJTs.

The dimension of the emitter region is expected to be of the order of $0.1 \rightarrow 0.2$ μm. This dimension is large enough for the SRM lateral resolution. However resistance results obtained from imaging this region suggest that the metal may extend too far into the silicon. This caused some difficulties in identifying the end of the metal contact and the beginning of the emitter region. Topographic profiles of the area taken after polishing show that the metal is slightly elevated compared to the silicon and surrounding dielectric materials. This is attributed to faster polishing rates for other materials compared to the metal interconnect. As a SRM tip scans across the metal-to-silicon interface at the emitter (say from the metal towards substrate), its side walls make contact with the edge of the metal even after the actual tip has passed the metal edge. Conceivably the side wall contact area may be larger than the usual contact area of the tip when imaging on flat areas. This may result in larger current flow across the junction. Since the emitter region is heavily doped, a large current is also expected when the SRM tip is located here. This metal-emitter difficulty was partially resolved by polishing the structure up to a height between vias. However, the silicides that are grown on this region could not be avoided using this polishing strategy.

Figure 4.10 (a) and (b) shows SRM images of a NPN bipolar junction device in real cross-section. The image in (a) shows all regions of the device including the collector contact sinker at the left hand side, the collector, base and base contact to a polysilicon layer.

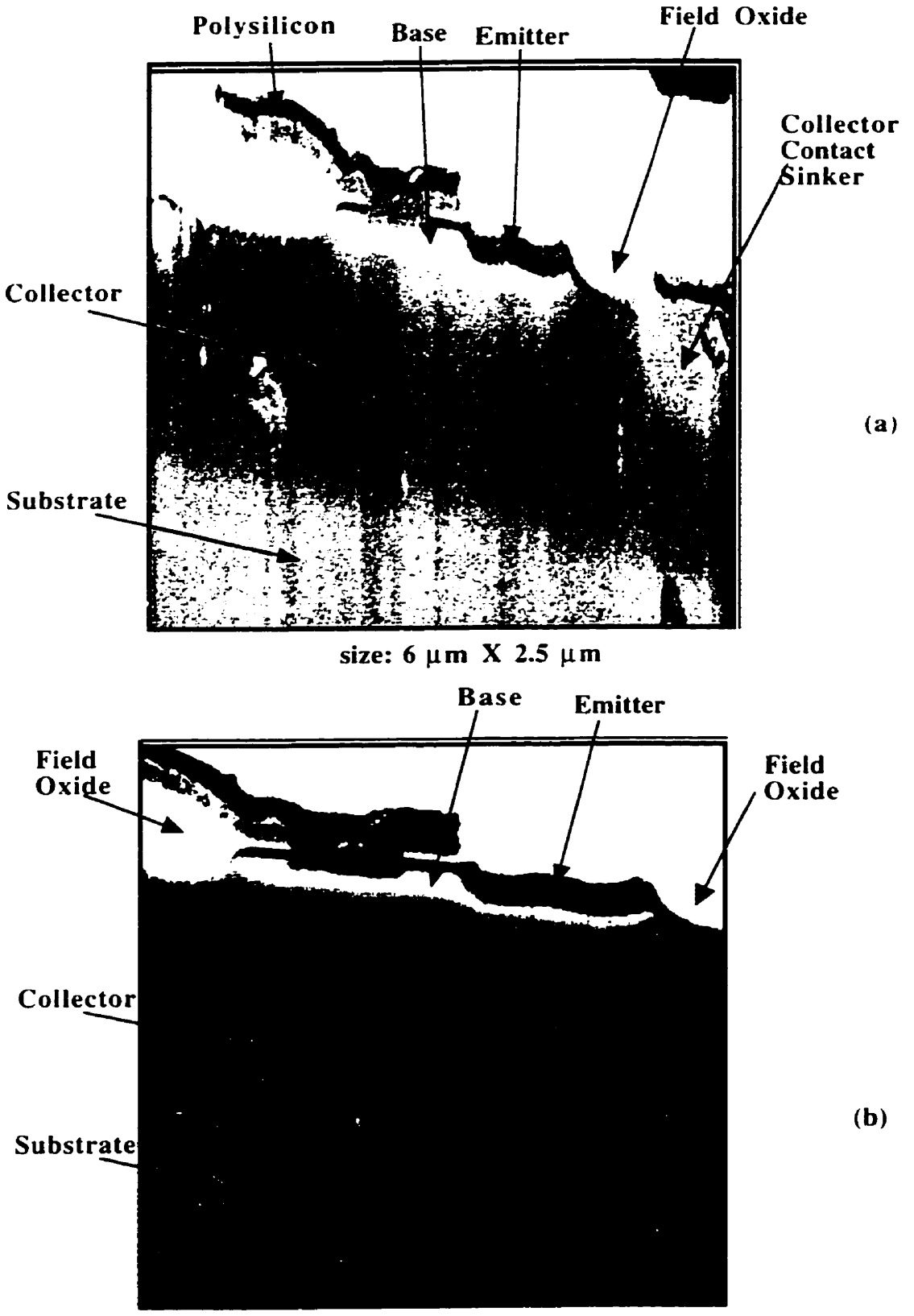


Figure 4.10 Resistance profiles of FE SEM stipe BJT (npn) cross section showing (a) a wider view and (b) a closer view in the active region.

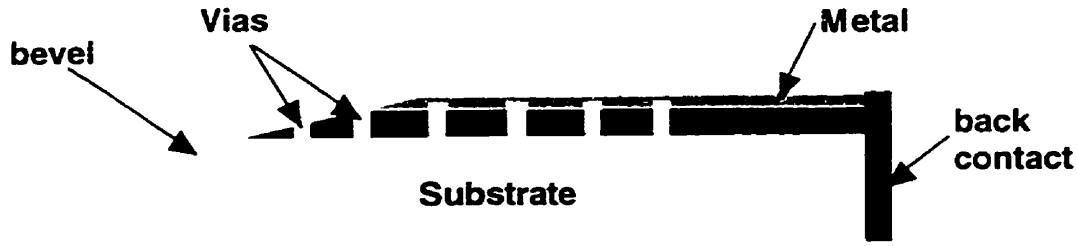
In Fig. 4.10 (a), three spots are observed, one at the left edge of the image within the sinker, another located within the collector and the third at the bottom (right). These are attributed to diamond tip landing marks. A close-up image of the emitter-base region shows, in Fig. 4.10 (b) the dark region labeled Emitter. We believe that the signal in this low resistance region (dark) is composed of three components; (i) the heavily doped emitter, (ii) the silicide present here and used for making a good contact to metal 1, and (iii) a topographic coupling that results from the side walls of the tip making contact to the silicide when the tip is close to but not on the elevated region. The dark region is observed to extend further from the emitter into the region above the base, break at the base contact, and then proceed to the end of the base. Topographic images of this area show that there is a topographic step everywhere along this dark region. This suggests that topographic coupling contribution to the emitter region may be the most significant one. However, the region at the emitter is wider than everywhere else, suggesting that the other two contributions (emitter and silicide) are quite significant. However, it is difficult to delineate the contribution of the emitter alone. The base is observed as a brighter region. The epitaxial layer of the sample (forming the collector) is clearly delineated from the substrate.

Another method that was undertaken to resolve the emitter from the metal contact and silicide was to bevel the structure at a 11° angle. Figure 4.11 (a) shows an illustration of the sample bevel. Since this sample structure is a long stripe and metal one layer makes contact to all device regions multiple times along its length, beveling exposes some of the vias on the beveled cross-section. Figure 4.11 (b) shows a resistance profile of a beveled BJT. This figure can be compared against the SEM image shown in Fig. 4.9 (rotated clockwise by 90°). Figure 4.11 (b) shows clearly a contrast between the insulating dielectric material (dark region), the silicon substrate on the left side on the image (brighter region), and the top metal layer and vias

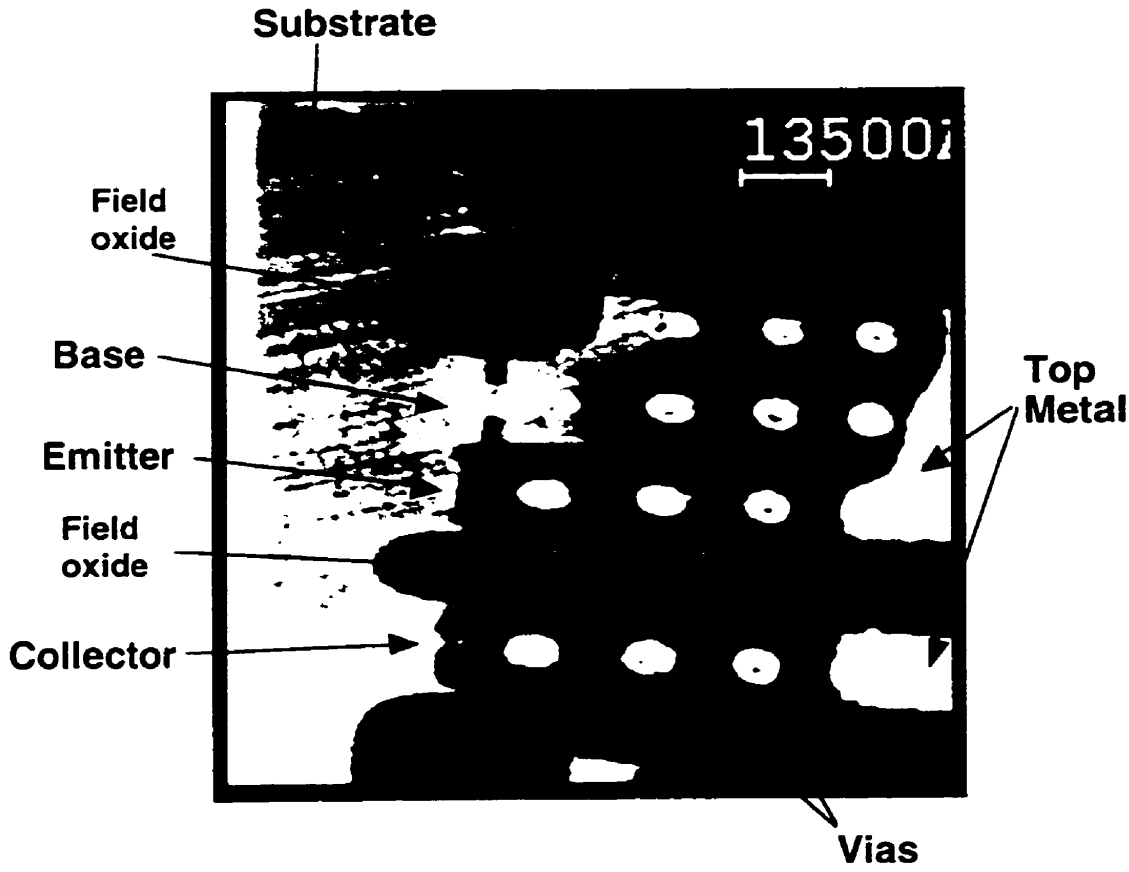
(brightest dots and regions). This image also shows straight streaks on the substrate running about 15° with respect to the top or bottom edge of the image. These features are attributed to topographic coupling of polishing marks into the resistance image.

Figure 4.11 (b) does not show contrasts that are associated with doped regions marked on Fig. 4.9. This can be explained by the presence of native oxide as this surface was not dipped into an HF solution. Beveling was done by an organization outside our laboratory and we did not know how the polished surface was terminated. An HF dip was not administered here in order to preserve the integrity of the topography of the beveled surface after polishing. The surface was then dipped in 2.5% HF solution for 5 seconds a few times before a signal was observed on this cross-section. The results are shown in Figure 4.12.

Clearly this image shows the whole base region. The P^+ base region appears as the brightest contrast in the greyscale, adjoining with the P^- base appearing in less bright contrast. The contrast between P^+ and P^- regions of the base here demonstrate the ability for the SRM to delineate between regions of high and low dopant density. The darkest region at the top end of the image corresponds to the location of insulating inter-metal dielectric material. The bottom end of the image corresponds to the collector region and substrate. The emitter region appears dark (high resistance). This contrast was not expected for this region because the emitter is heavily doped. One possible explanation for the dark contrast is that the tip does not make contact with the emitter at all. The topographic image of this region shows a deep depression at the emitter location. This may have resulted from HF preferentially etching the heavily doped n^+ emitter during while we were removing native oxide.



(a)



(b)

Figure 4.11 (a) An illustration of the bevel on the BJT structure. **(b)** A SRM resistance profile of a beveled BJT cross-section.

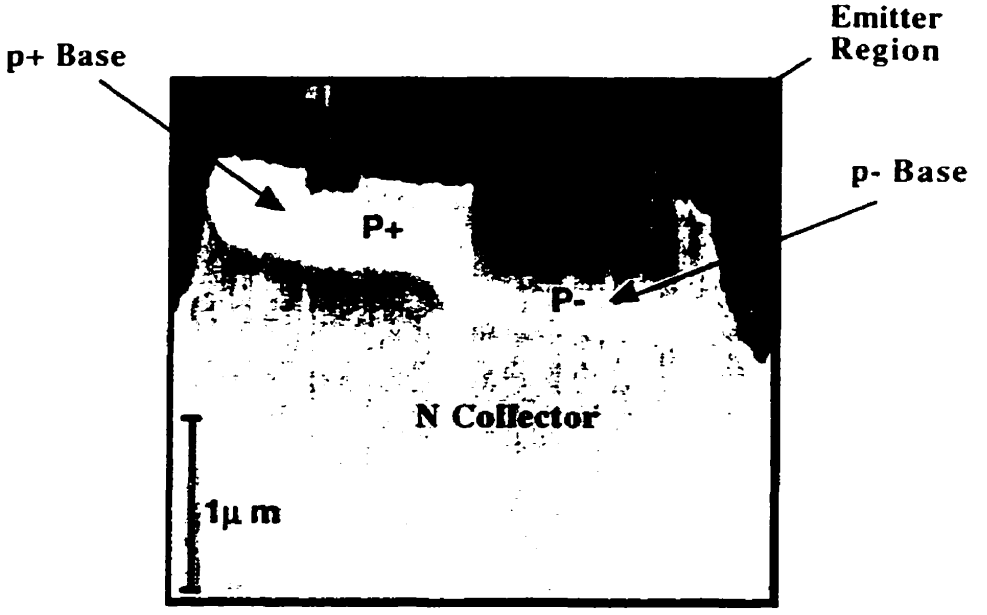


Figure 4.12 SRM resistance profile of a beveled BJT (p-n-p) cross-section showing contrast between P+ and P- base. The shape of the base is consistent with Fig.4.9

Figure 4.12 is compared with a SCM image of the base region for this BJT in Fig 4.13 (b). The topographic profile shown in Fig. 4.13 (a) shows that the substrate is elevated compared to the field oxide and the rest of the inter-metal dielectric materials. Furthermore, a depression is observed at the emitter region below the via. This region is topographically lower than the rest of the substrate as well as the metal via. Figure 4.13 (a) shows quite clearly the P+ base (very bright), the P- base adjoining towards the right (less bright), the collector region below the base (darkest contrast), polysilicon layer and dielectric material above the base region (less dark contrast). For the capacitance image bright regions on the greyscale represent a positive $^{dC}/_{dV}$ which in this image corresponds to p-type regions, while dark regions represent negative $^{dC}/_{dV}$ or n-type regions. On insulating regions, metals and heavily doped regions we expect the capacitance derivative to vanish (zero) when using metal tips. The SCM image shows the emitter in a contrast that is the same as the polysilicon layer.

Figure 4.12 and 4.13 (b) both show contrast between the heavily doped base and the lightly doped base. SRM and SCM results are complementary.

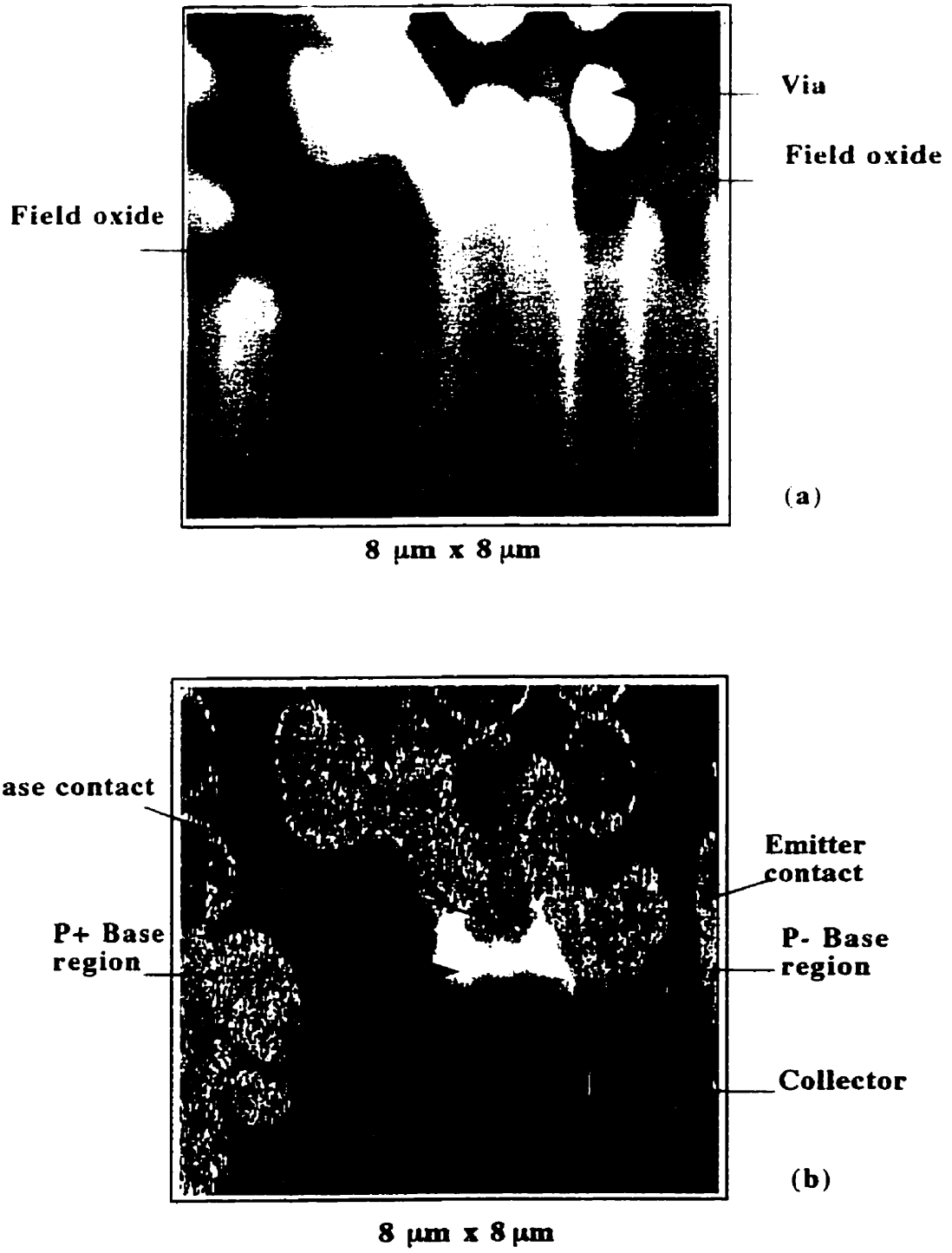


Figure 4.13 (a) A topographic and (b) capacitance profile of a beveled BJT cross-section.

4.5.2 Imaging Real BJT Devices

The results presented in this section was part of the contract work that we did for a microelectronic company. Figure 4.14 shows a schematic diagram of the structure of a BJT cross-section illustrating the expected profile of the diffused emitter, base, and collector regions including an n+ polysilicon emitter finger overlaid on the active region.

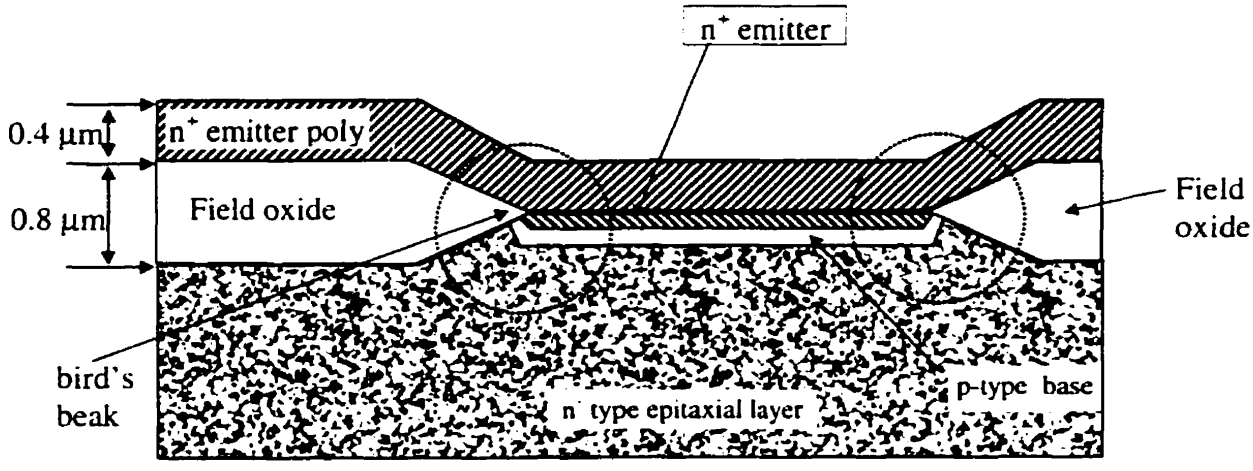
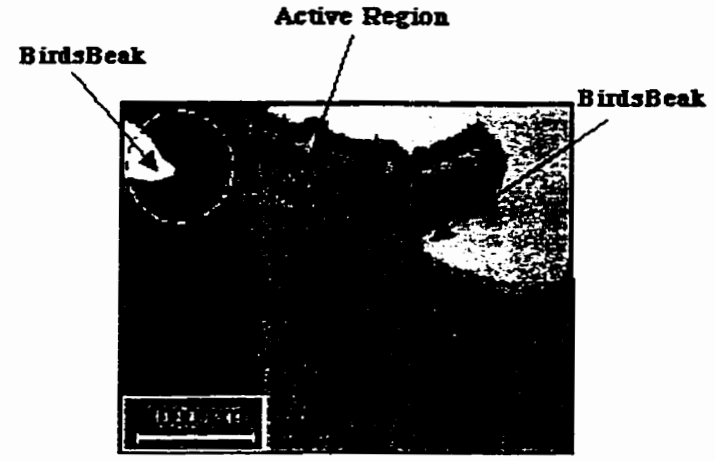


Figure 4.14. A schematic diagram of a BJT structure illustrating the base, emitter and collector regions overlaid with a poly emitter finger. Dotted circles mark the regions to be imaged with the SRM probe.

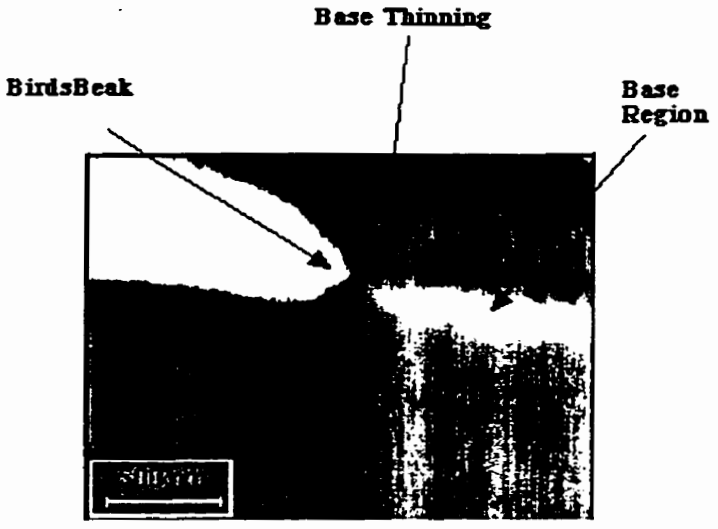
The emitter finger shown as "n^+ emitter poly" runs over the field oxide, above the active region and on to another field oxide. The active region is made up of an emitter, a base and a n^- collector. We are interested in the resistance/doping profile in the active regions close to the "bird's beaks" marked with dotted circles and, in particular, in the shape of the base region close to the "bird's beak".

To prepare the devices for SRM imaging, the wafer was processed up to and including Metal 1 patterning. A 200 nm thick layer of AlCuSi was then deposited to short out everything. Finally 1.5 μm of CVD oxide was deposited for passivation.

SRM results of this structure are shown in Fig. 4.15 (a) and (b). On the greyscale, brighter regions in these images represent lower resistance regions while darker regions represent higher resistance regions.



(a)



(b)

Figure 4.15 Resistance Profiles of a NPN bipolar device cross-sections. (a) A wide view of the active region up to the bird's beaks. (b) A close up of the active region near one "Bird's Beak".

Figure 4.15 (a) is a resistance profile of a polished cross-section showing the active region of another BJT structure. The two bird's beaks, the active region and one end of the emitter finger are shown in this image. At this scale the image shows some contrast in the active region that is indicative of the resistance variation. This is the region where the base layer is expected. Fig. 4.15 (b) shows a close-up view of the active region near the "bird's beak". Clearly the delineation between the p- base, n+ emitter and n- collector is observed. The thickness of the base region reduces dramatically near the "bird's beak". The same base region narrowing was observed at its other end. This base narrowing is an undesirable phenomenon which may require modification of the fabrication process of this device. The following table shows a comparison of the expected dimensions of the emitter and base region with those from SRM results.

	Base (nm)	emitter (nm)
expected (fab)	110	50
SRM values (FWHM)	144	67

Table 4.1. A comparison between expected and measured dimensions of the base and emitter regions.

A good agreement is observed between these values. The differences are mainly due to finite tip size. At both ends the base region almost seems to disappear. This may result in increased emitter-collector leakage currents that would affect the device characteristics.

SRM was also used to image a PNP bipolar device. The structure of this device is shown in Fig. 4.16. Metal contacts to the emitter, base and collector regions are identified by the letters "E", "B" and "C" respectively. Of course all device regions are shorted out for the purposes of SRM imaging. This device was built in a n-type device well. The collector contact "C" makes contact to the lowly doped n-type collector region through a low resistance path provided by the "**SINKER**" and the n+ buried layer as illustrated by the schematic drawing. The device is also

electrically isolated from adjacent devices using p+ doped isolation structures "**ISO**" in order to reduce parasitic effects.

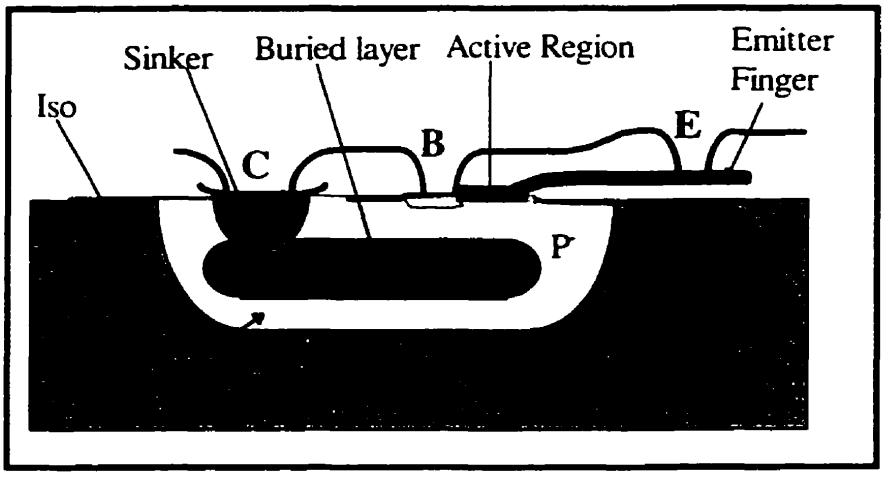
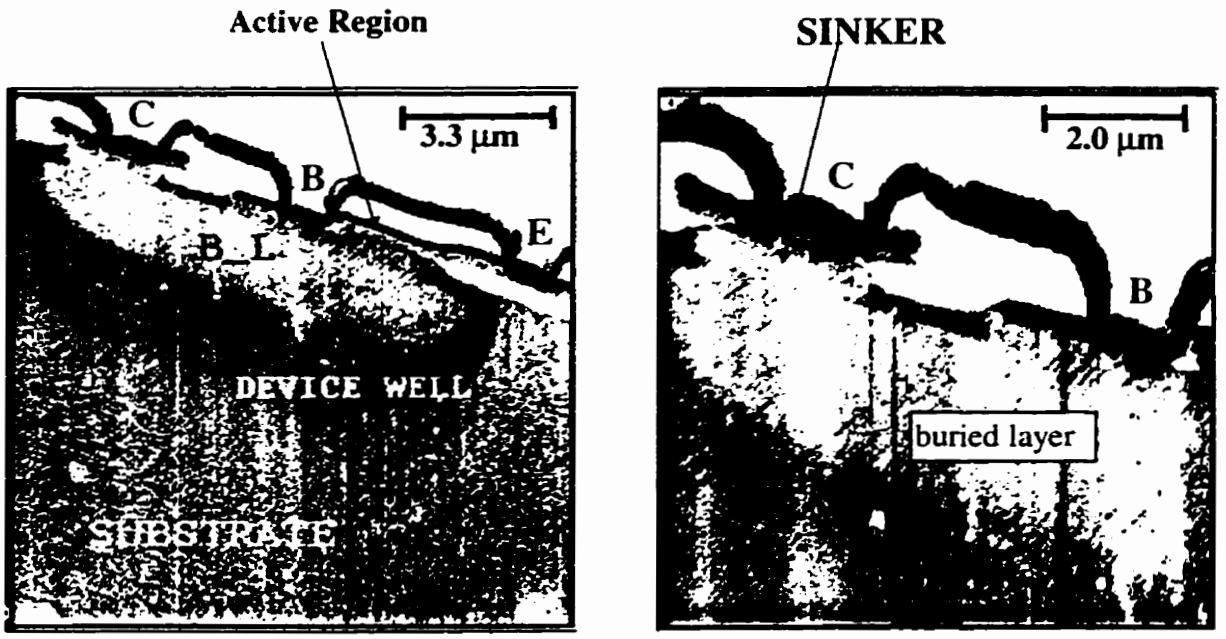


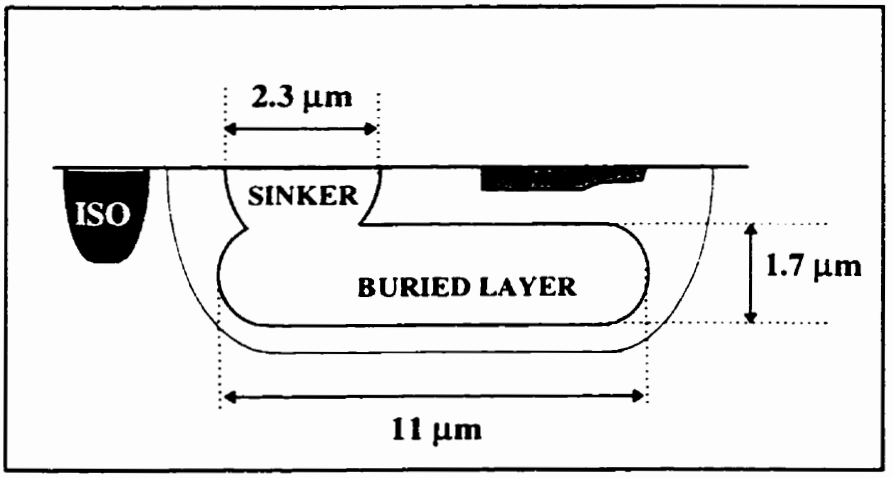
Figure 4.16 A Schematic drawing (not drawn to scale) for a PNP bipolar transistor.

The purpose of this experiment was to measure the dimensions of the sinker and the isolation structures. This experiment was done using SCM and SRM. SRM results are shown in Fig. 4.17. In these SRM images **brighter** regions on the greyscale represent **higher** contact resistance regions while **darker** regions represent **lower** contact resistance regions.

The bright region at the top in Fig. 4.17 (a) is the inter-metal dielectric from where the metal interconnects make contact to the collector, base and emitter. The "SINKER" is shown as a brighter region below the collector contact. The sinker is attached to the buried layer "**B_L**" having the greyscale contrast. The device well appears as a darker region surrounding the buried layer. Notice that the right hand side edge of the device well does not curve back with the edge of the buried layer. The substrate shows a "hazy" contrast with a high density of dark spots. The origin of this haze is not well understood. However, this it is a very repeatable character on this surface when imaged with SRM.

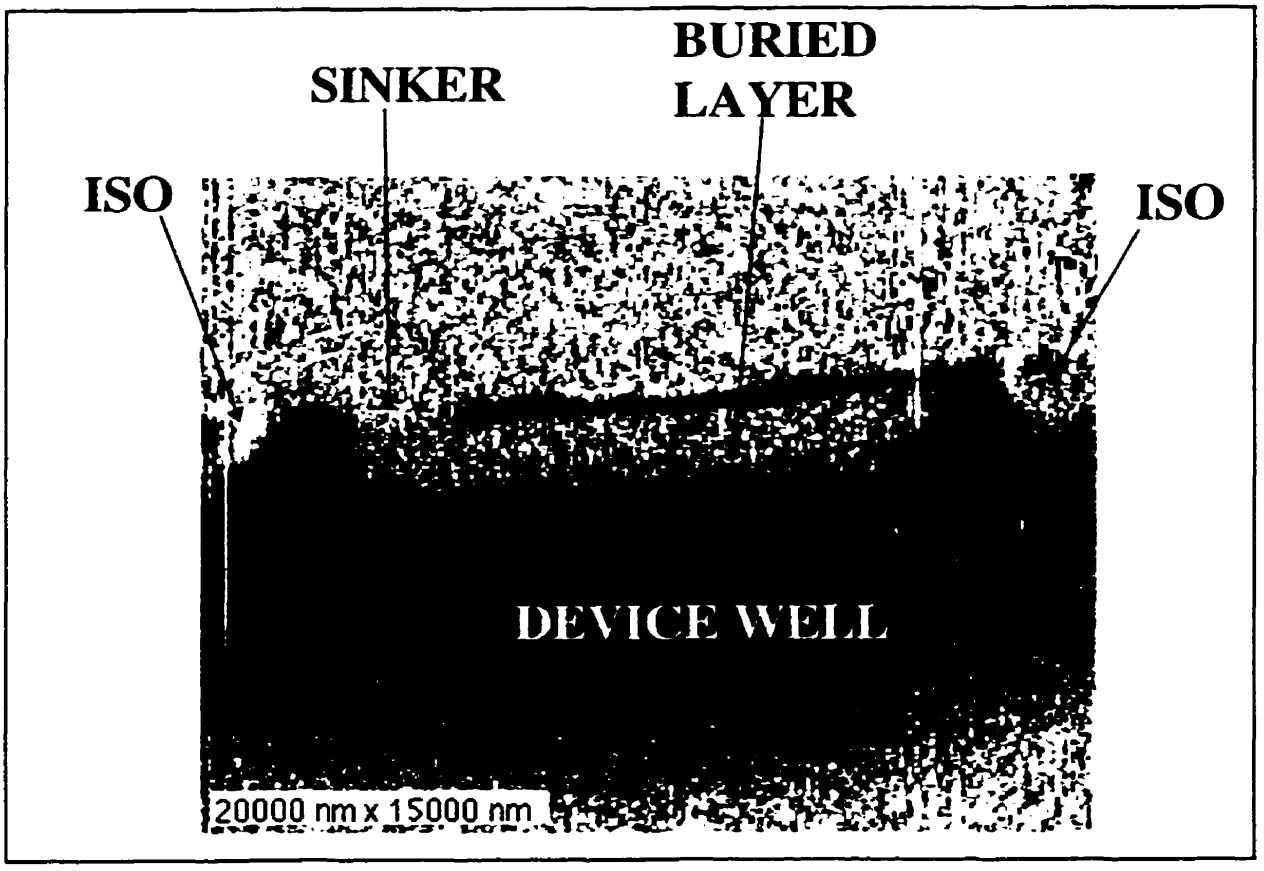


(a) (b)



(c)

Figure 4.17 Resistance Profiles of a PNP bipolar device: **(a)** An overall image showing the device well, buried layer "B_L", metal contacts to all three regions of the device. **(b)** A close up view of the "SINKER" and part of the active region. **(c)** A sketch diagram showing measured dimensions.



(d)

Figure 4.17 (d) A SCM of a PNP bipolar transistor showing isolation structures, SINKER, and a heavily doped p-type buried layer.

In Fig. 4.17 (b) the shape of the "SINKER" is observed to resemble that shown in the schematic drawing. A sketch diagram illustrating the dimensions that were measured from SRM images is shown in Fig. 4.17 (c). Visual examination of SRM images for this structure do not show enough contrast to clearly locate the device isolation structures. A possible explanation for the small signal in this region is that the isolation structures do not make direct electrical contact to the common ground contact. SRM is a d.c. technique and therefore it is essential that every layer of interest make direct contact to ground. Lack of such a contact may result in the current being limited by a reverse biased p-n junction that is located between the tip-surface junction and

ground or even an insulating layer. This is one of the major limitations of the SRM technique. SCM results reveal the isolation structure quite clearly. For the SCM, (1) it is an a.c. measurement technique and (2) it measures very small capacitances under the tip. Since the isolation structure connects to the common contact through other layers via a larger area compared to the tip contact, a larger series capacitor is formed. If this capacitor is much larger than the depletion capacitor, the equivalent capacitance is of the order of the tip-sample depletion capacitance. Therefore, ideally SCM does not necessarily require shorting of all layers directly to a common ground. The only requirement is that a potential must be applied to the sample to complete the circuit. For this reason SCM results reveal the isolation structure quite clearly. A SCM image of the PNP bipolar structure is shown in Fig. 4.17 (d).

4.6 DIFFUSION PROFILE OF BORON IN HEAT TREATED SIGE LAYERS

SiGe has been used as a base material to fabricate Si-SiGe-Si HBTs in order to reduce the emitter capacitance for high frequency operation. This structure has been used in the study of anomalous boron diffusion in the base of Si-SiGe-Si HBTs [47]. SRM has been used to image the cross-section of six MBE grown p+ SiGe layers of 20 nm thickness separated by 70 nm of intrinsic silicon. A schematic drawing of the structure is shown in Fig.4.18. The heavily doped layers are sandwiched between two 100 nm thick intrinsic layers. At the surface there is a shallow arsenic implant layer. Furthermore, there are platinum electrodes on the surface of the sample as shown on the schematic drawing. This structure was then subjected to a high temperature treatment, a usual step for implant activation in semiconductors. As a result there was diffusion of dopants from the SiGe layers towards the neighboring intrinsic silicon layers. The National Research Council of Canada provided these samples. The purpose of this

experiment is to study the diffusion pattern of boron in the region near the platinum electrodes. Both a straight cross-section and a beveled cross-section of the structure were examined with SRM. The results from this experiment should give an insight into the effect of a surface electrode on dopant diffusion under heat treatment.

Figure 4.19(a) shows a resistance profile taken on a straight cross-section of the SiGe multilayer structure. In this SRM image, the bright vertical lines correspond to intrinsic silicon layers separated by dark lines that correspond to the SiGe layers. The left hand side of the image corresponds to the substrate and on the right hand side is the edge of the sample (dark). This dark end of the image, indicating low resistance, is attributed to the shallow asernic implant at the surface. This region appears much wider than expected. There are two reasons for increased junction current in this region and they are based on the fact that as the tip scans past the edge of the sample, a topographic step, its side wall remains in contact with the edge. They are; (1) the contact area between the side-wall of the tip and the edge is larger than that between the actual tip and the flat surface, (2) the side wall of the tip is in contact with a heavily doped surface layer (low resistance arsenic layer). A line cross-section taken along A-A′ of Fig.4.19(a) is shown in Fig.4.19(b). Here, troughs correspond to the location of intrinsic silicon regions while peaks correspond to doped silicon regions. The line cross-section shows wider intrinsic regions (marked with arrows) at both ends of the layer structure. This is consistent with the specifications of the sample. The line cross section shows six peaks between the arrows that correspond to the six MBE grown SiGe layers with a spatial resolution of 40nm. SRM spatial resolution is limited by the contact radius of the tip (~30 nm), and surface roughness. These layers appear to be wider than the nominal dimensions because of boron diffusion due to the anneal step as well as the finite tip size and sample surface roughness. Low SRM signal intensity is observed when

scanning over the layers close to the surface. Low signal intensity in this region may be attributed to faster diffusion of dopants during annealing.

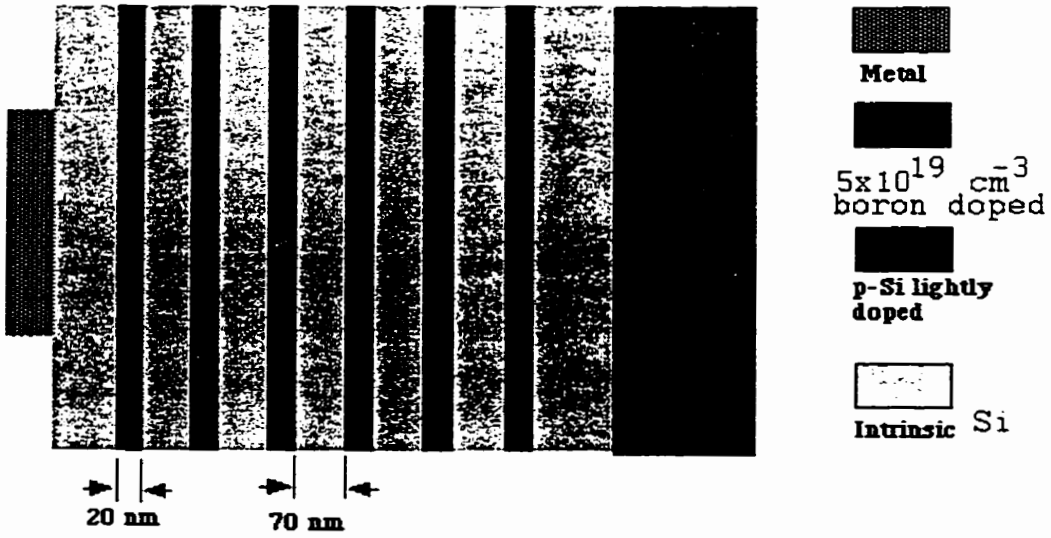


Figure 4.18 A schematic drawing of the MBE grown SiGe layers.

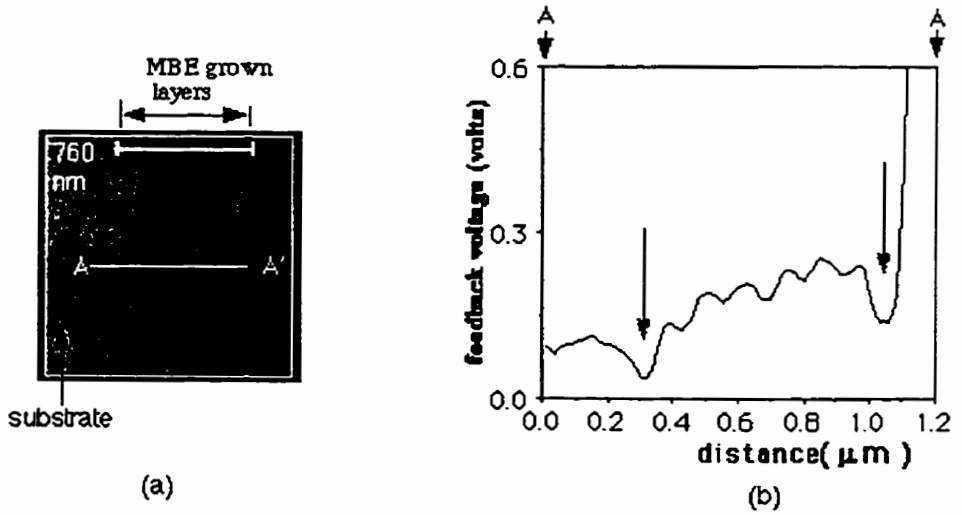
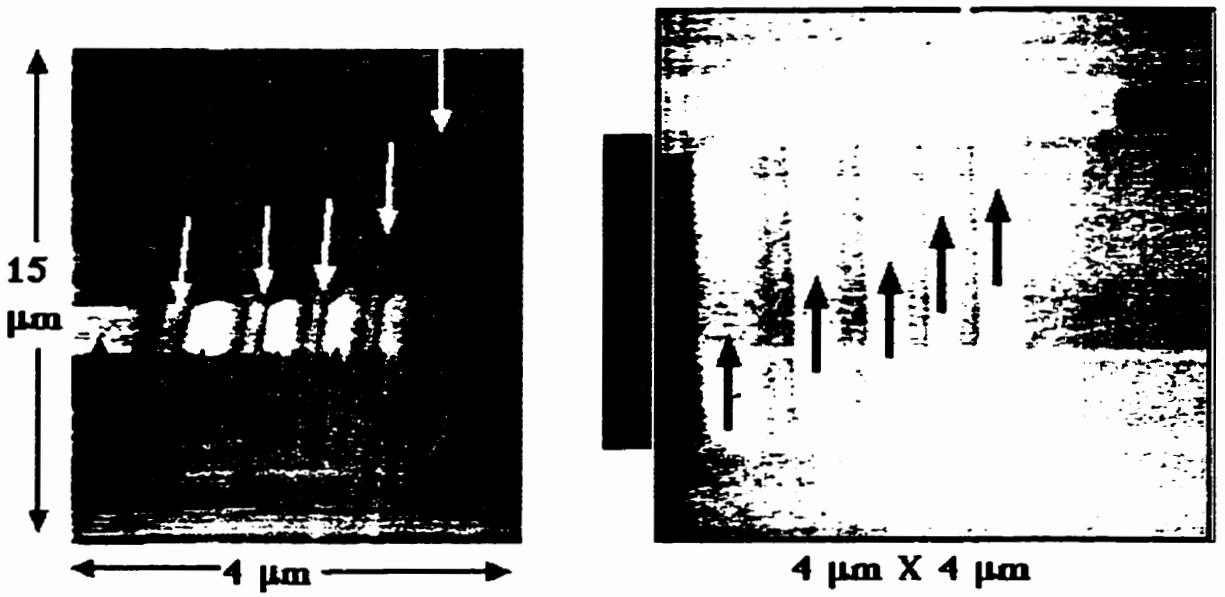


Figure 4.19 (a) A SRM profile of the layer structure cross section. (b) shows a line cross section across A-A'.

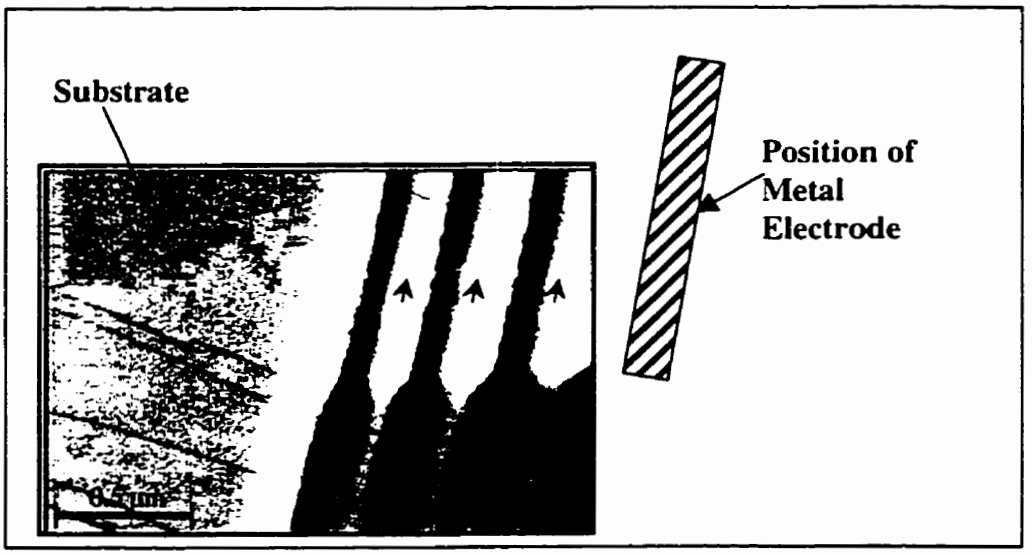
The same structure was beveled at 11° and then imaged with the SRM. Figure 4.20 (a) shows a large scale view resistance image of the bevel in the region close to the metal. A close up and symmetrical scan of the same region is shown in Fig.4.20 (b). In these images dark regions represent low resistance regions and brighter regions represent higher resistance regions. The SRM images show vertical dark lines (highlighted with white arrows) separated by brighter lines (highlighted with black arrow). The bright lines correspond to the intrinsic layers and dark lines represent the doped layers (low resistance).

The SRM images show that in the region below the electrode, boron doped layers do not diffuse as much as they do in regions outside of the electrode. The doped layers seem to merge in the region away from the electrode (Fig. 4.20a), However, in the region nearest to the electrode the dark lines are quite clearly defined. It seems that the presence of the electrode inhibits boron diffusion during heat treatment. When imaging this structure the metal electrode was avoided because it did not polish very well and tends to catch the tip causing instability. The black rectangle on the left hand side of the image represents the position of the metal.

The multilayer structure was re-polished at about the same bevel angle and then the cross-section was cleaned with 2.5 % HF and imaged a few minutes later with SRM. Figure 4.20c shows a resistance profile taken on the beveled surface the first time. This image illustrates that when the SRM probe scans a surface the first time around, very clean contrast can be obtained. When the probe scans over the same area again the intensity of the signal gets degraded. The biased tip seems to modify the surface by field enhanced oxidation. Figure 4.20c demonstrates more clearly the diffusion pattern of boron in the region under the platinum electrode. Under the electrode the doped layers are much narrower than outside the electrode. This image was taken at one end of 22 μm wide electrode.



(a) (b)



(c)

Figure 4.20 SRM profiles of a MBE grown multilayer structure. Profile (a) shows the diffusion pattern of boron both near and far from the surface electrode. From profile (b) it is observed that boron diffusion is slower at higher depth. Profile (c) shows a close-up view of one end of a 22 μm wide electrode and the deepest three doped layers. Green arrows show the location of i-Si interleaved with layers of non-uniform boron doped layers (red arrows).

4.7 IMAGING OF MOSFETS FROM EEPROM CELLS

Another example of SRM imaging of state-of-the-art devices is the cross-sections of MOSFETs from an Electrically Erasable Programmable Read Only Memory (EEPROM) cell. This device is made of a control gate, floating gate, and asymmetrical source/drain regions. The source was realized by an initial deep phosphorus diffusion followed by a shallow arsenic diffusion.

Figure 4.21 shows a SRM image of the EEPROM CMOS device. In this image brighter regions on the greyscale represent higher resistance regions while darker regions represent lower resistance regions. Clearly the asymmetry in the S/D regions is observed in this image. The source region clearly overlaps with the gate while the drain does not show much overlap with the gate. This figure also shows two layers in the gate region. The thinner layer located closest to the channel represent the floating gate while the wider layer located immediately above is the control gate. The curved line that runs from the source towards the drain in the substrate is attributed to a topographic coupling from a scratch mark that remained after polishing. Metal 1 appears as the dark curved region at the top end of the image. The source p-n junction depth is approximately 0.5 μm where as the drain p-n junction depth is 0.2 μm. The SRM signal from the floating gate is weak because of lack of a direct electrical contact with common ground.

Analysis of SRM results do not show the presence of a lightly doped drain in these devices.

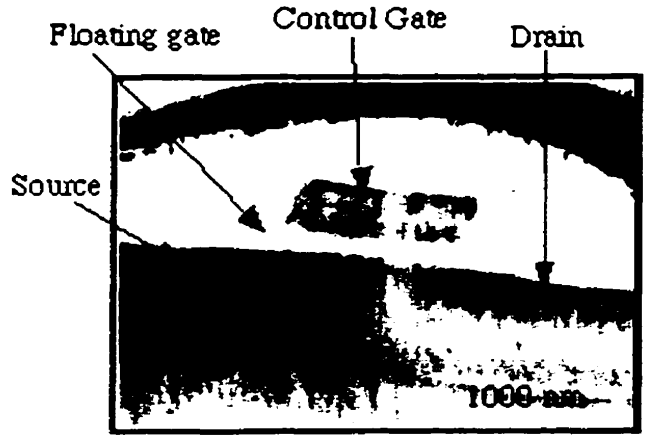


Figure 4.21 A SRM image of an EEPROM cell with asymmetrical source/drain regions.

4.8 CONCLUSION

The SRM technique has been demonstrated as a method of 2D imaging of semiconductor cross sections by imaging a wide variety of devices. The results presented here form a fraction of the number of semiconductor structures imaged with the instrument. So far SRM results have provided qualitative analysis of semiconductor device cross-sections. Quantitative SRM results will be achieved by using the calibration technique outlined in chapter 3. The biggest limitation to calibration presently is unavailability of a reliable source of boron-doped diamond tips as well as a self contained calibration sample made up of regions that are doped from 10^{15} cm^{-3} to 10^{20} cm^{-3}. Such a sample would eliminate systematic errors that are associated with differences in sample surface condition in the calibration. In order to produce reliable I-V calibration curves, for the SRM tip-semiconductor junctions, calibration must be done with a large enough number of tips to cover statistical fluctuations in tip quality on a calibration sample. All surfaces that are imaged with SRM must undergo the standard polishing procedure that is performed on calibration samples in order to maintain consistency in the interpretation of SRM results.

High spatial resolution (20 nm so far) was achieved by using boron doped diamond tips to scan on state-of-the-art device cross-sections. The biggest limitation to resolution is the physical dimensions of the tip.

CHAPTER 5
IMAGING OF ROUND-ROBIN STRUCTURES

5.1 INTRODUCTION

In order to evaluate the characteristics of profiling techniques, SEMATECH has provided dopant profiling research groups world-wide with semiconductor structures of known impurity profiles. Typical fabrication processes used in normal semiconductor technology, such as ion implantation and epitaxial growth of layers, were used to fabricate these test structures. The round-robin samples used in this study were specially designed to test various aspects of dopant metrology including [46]:

- spatial resolution as a function of dopant concentration
- the ability for a profiling technique to correctly profile linear impurity concentration gradients
- the ability for a technique to profile both n- and p-type regions, and junction delineation

After the analysis is completed, research groups then send their results to SEMATECH so that a comparison of the results from different groups may be done.

We have taken part in these international round-robin projects. We started off by imaging two samples (sample #1, and sample #2) with the SRM. In this chapter, SRM profiles are compared with SIMS profiles from IBM Analytical Services[48]. We have also imaged state-of-the-art (0.4 μm) MOSFET structure cross-sections fabricated by SEMATECH.

Constant current SRM imaging mode was used with the current regulated between 1 and 10 nA and the tip-surface contact force was regulated between 1 and 20 μN. The calibration

measurements discussed in chapter 3 show that, when a diamond tip is utilized, a good sensitivity in SRM measurements is obtained at set point currents below 10nA.

5.2 ROUND-ROBIN STRUCTURE #1

This structure was fabricated using low temperature epitaxial growth starting with a <100> p-type silicon substrate doped with boron at 11-25 Ω-cm. Figure 5.1 shows the impurity profile of structure #1 as specified [46]. Also shown in this figure are electron and hole profiles calculated from solution of Poisson's equation using the specified impurity concentrations. The carrier profiles were included here because carrier concentrations are the basic quantities to which electrical profiling measurements, such as SRM and SCM, are sensitive.

Basically, structure #1 is composed of two heavily doped peaks as shown. Abrupt doping steps between 10^{20} , 10^{19} and 10^{18} cm^{-3} are shown on one side of the first peak. The purpose of these steps is to determine the spatial resolution of a profiling technique as a function of doping level. Of course the carrier densities are not as abrupt as the specified impurity concentrations because no discontinuities are allowed in carrier profiles. The second peak is formed by a linear gradient of impurity concentrations (appears curved on the log plot) starting from $10^{18} \rightarrow 10^{20}$ cm^{-3} and back to 10^{18} cm^{-3}.

The following definition of spatial resolution was proposed by SEMATECH [46];

> *" ..the maximum of the rise or fall distance between 16% and 84% concentration levels of a measurement on an abrupt concentration step".*

The two steps in the first peak provide convenient locations for determining spatial resolution for a measurement technique.

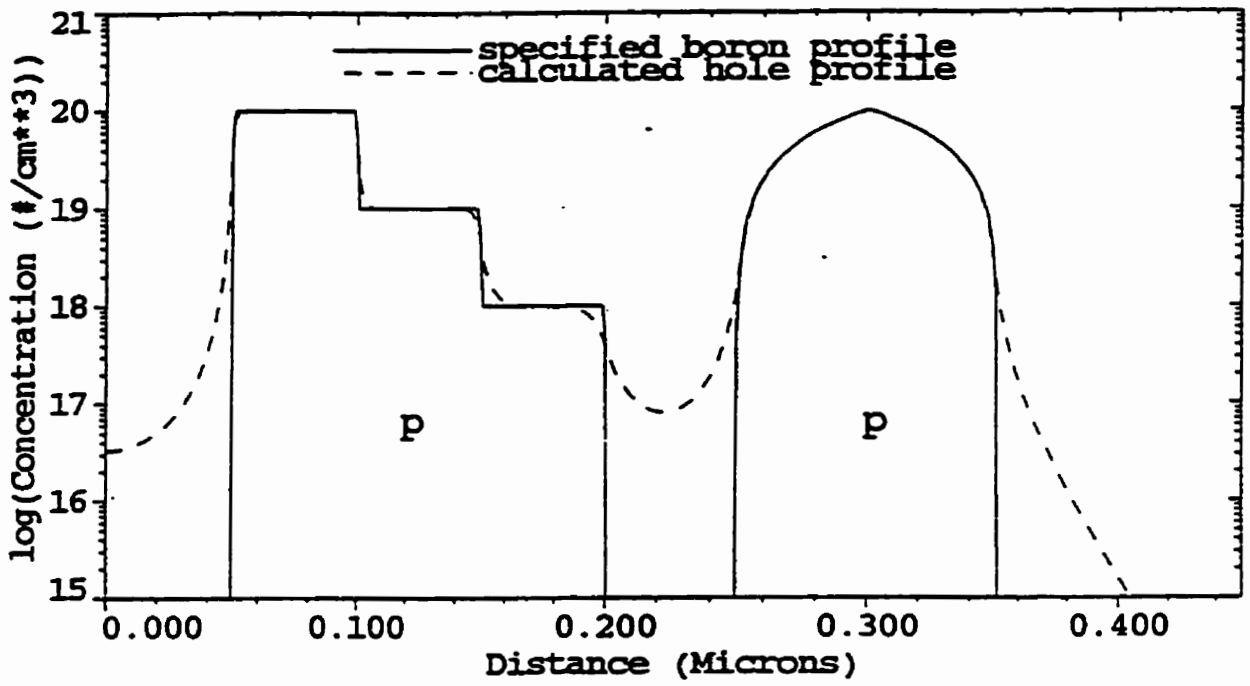


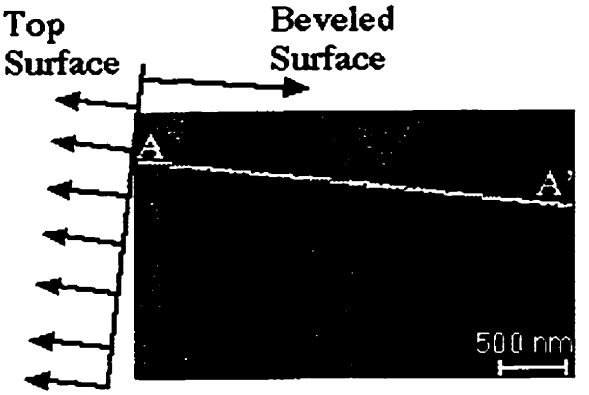
Figure 5.1 Specified dopant profile and calculated carrier densities for SEMATECH Round-Robin sample #1. (source: Ref. [48])

5.2.1 A Comparison Of Resistance With SIMS Profiles (#1)

Prior to performing SRM imaging, the sample was prepared in the usual manner (section 2.7) including a 11° bevel in order to enhance spatial resolution. Figure 5.2(a) and (b) show a 2D SRM resistance profile and a line cross-section taken along A→A′, respectively. Figure 5.2(c) shows a SIMS profile from IBM Analytical Services.

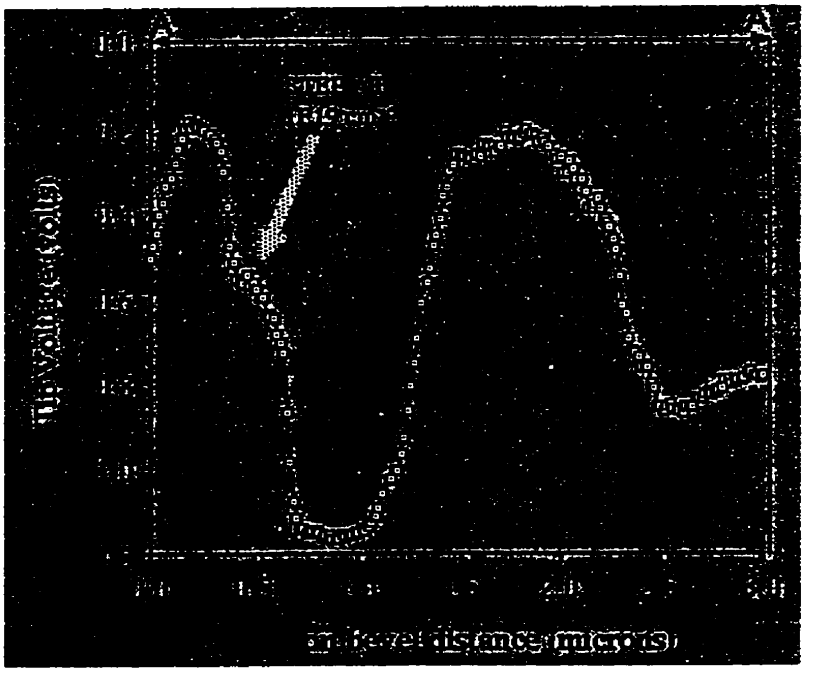
The SRM line cross-section shows quite clearly the two peaks. The "shoulder" on the right hand side of the first peak corresponds to one of the 50 nm wide steps shown in Fig.5.1. This shoulder is attributed to the doping step located at 10^{19} cm^{-3}. Calibration curves show that the SRM is sensitive to doping concentration levels above 10^{18} cm^{-3}. This implies that the second step (at 10^{18} cm^{-3}) is at the same greyscale level as the next region that is doped below 10^{18} cm^{-3}.

A resolution of 30 nm is measured at 10^{20}→10^{19} cm^{-3} abrupt concentration step. This resolution is consistent with spatial resolution obtained on imaging real device cross sections. Unfortunately the bevel here introduces broadening of the abrupt doping concentration steps which makes the resolution measurement less meaningful. However, this measurement provides a measure of the sensitivity for the SRM.



2D SRM PROFILE

(a)



(b)

Figure 5.2 A comparison of SRM profiles with SIMS profiles for structure #1. (a) shows a 2D SRM image of a beveled structure, (b) a line cross section across A→A′

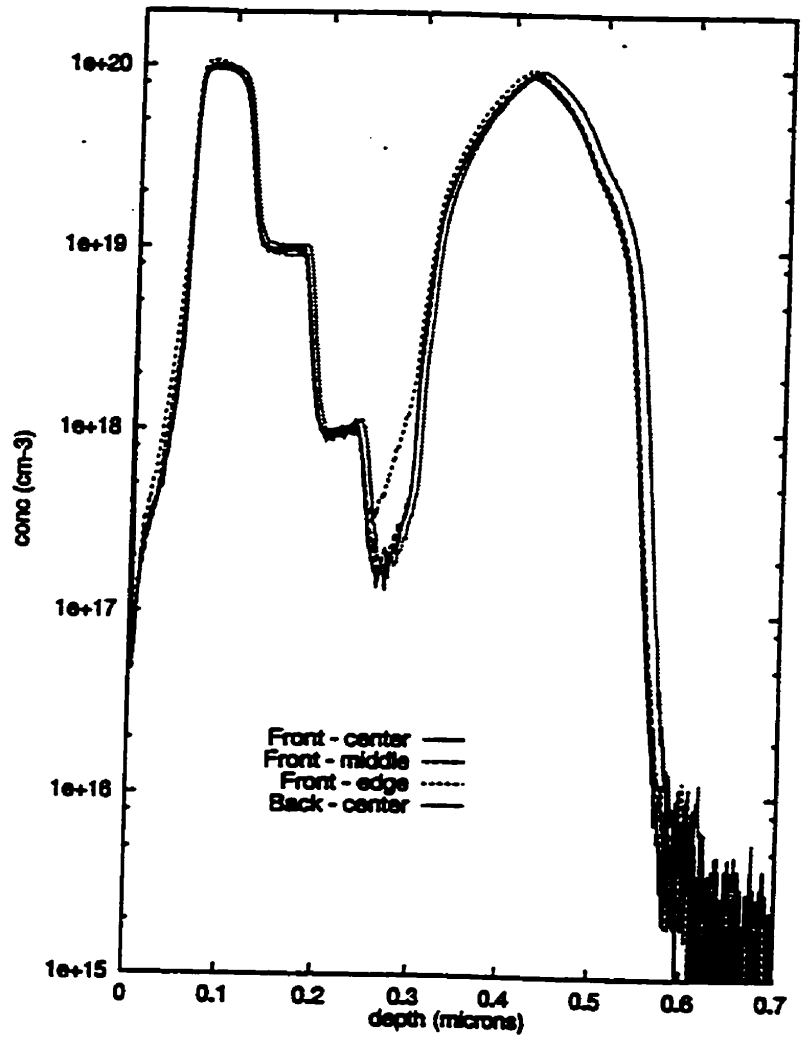


Figure 5.2 (c) SIMS profiles for round-robin sample #1 at the center, middle and edge of the wafer frontside and the center on the backside (source: Ref. [48]).

5.3 ROUND-ROBIN STRUCTURE #2

The fabrication process of this structure and starting material was the same as that of structure #1. The specified impurity profiles and calculated carrier concentration profiles are shown in Fig. 5.3. This structure is composed of abrupt p-n junctions formed by 10^{18} cm^{-3} doped regions of boron and phosphorus doping. This region is meant to test the ability for a profiling technique to deal with p- and n-type as well as depletion regions. Also included in this structure are narrow boron doped plateaus that are meant to test the spatial resolution of small features. As shown in Fig.5.3, there are 10 nm, 40 nm and 100 nm wide (10^{20} cm^{-3}) regions separated by 50nm wide regions of 10^{18} cm^{-3} boron doping.

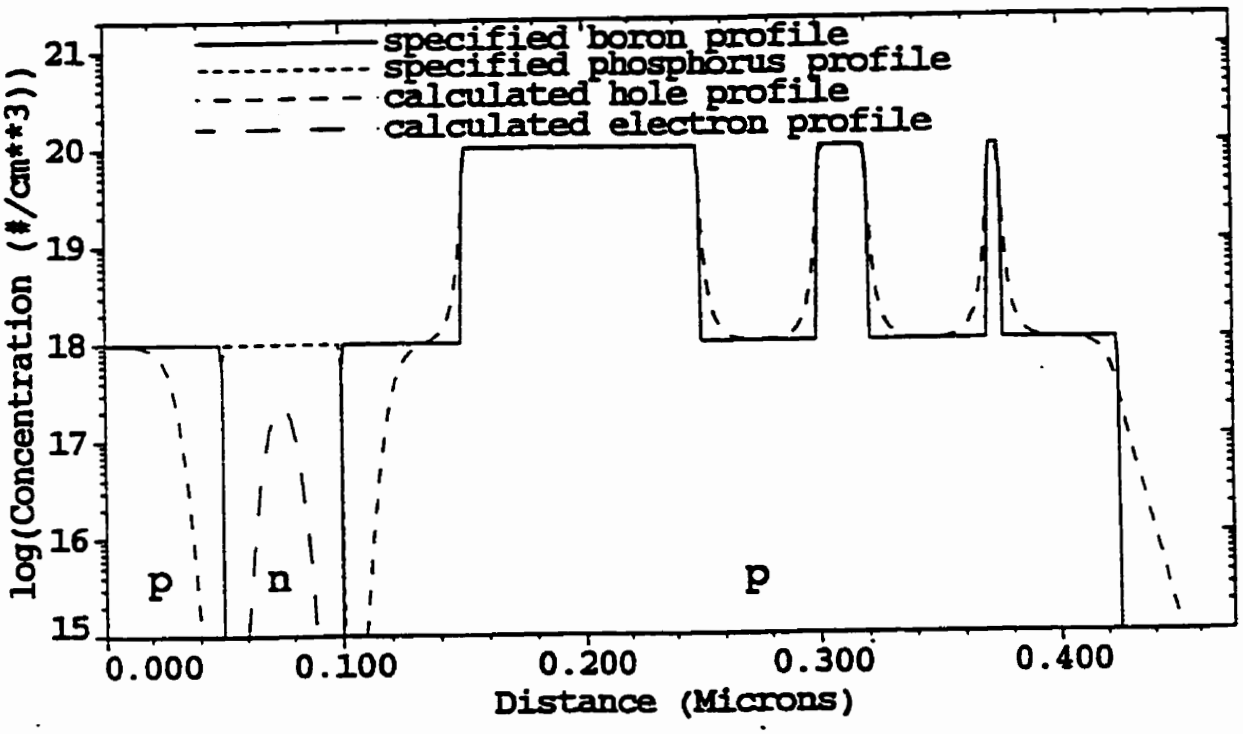


Figure 5.3 Specified dopant profile and calculated carrier densities for SEMATECH Round-Robin sample #2. (source: Ref. [48])

5.3.1 *A Comparison of resistance with SIMS profiles* (#2)

SRM imaging was performed on a polished cross section of the structure #2. The sample was mounted on a SRM stage in the usual (chapter 2). Figure 5.4 (a) and (b) shows SRM images of the structure cross section. Here, brighter regions on the greyscale (higher feedback voltages) represent higher resistance regions while darker regions (lower feedback voltages) represent lower resistance regions.

Figure 5.4(a) shows a large scale view (1.5 μm × 1.5 μm) of the layer structure including the top edge of the sample. A close up view is shown in Fig. 5.4(b) (1 μm × 1 μm). The sample orientation is such that the right hand side of the image is the substrate and the left hand side is the top edge. Starting from the substrate end toward the top of Fig. 5.4(a), the images shows quite clearly a thin vertical dark line labeled P_a. This line corresponds to the smallest boron doped (10^{20} cm^{-3}) plateau of shown as P_1 on Fig. 5.3. The image shows even more clearly the second and third boron plateaus P_b and P_c in succession corresponding to P_2 and P_3 in Fig.5.3 respectively. Beyond P_c, the images do not show much contrast on the greyscale. The p-n junctions are located in this region as shown by Fig.5.3.

Figure 5.5(a) and (b) show line cross section profiles of the structure taken with SRM and SIMS respectively. The SRM profile shows feedback voltage required to attain 1nA current across the tip-surface junction. This profile is an average of 37 line profiles taken at regular intervals from the top to the bottom of Fig. 5.4(a). This was done in order to enhance the signal to noise ratio on the line cross sections. The peaks shown in this profile correspond to the lower boron doped regions (10^{18} cm^{-3}) and the higher boron doped regions are shown as depressions with labels corresponding to those in Fig.5.4(a). However, the line profile also shows two peaks between which there is a depression near the top of the sample. The peaks represent 10^{18} cm^{-3}

boron regions and the depression in between them represents the 10^{18} cm^{-3} phosphorus doping region. Although these three regions have equal dopant densities, the n-type region shows lower feedback voltage (lower resistance) compared to the neighboring p-type regions. This is consistent with the results of the I-V calibration measurements given in chapter 3. This demonstrates the ability of the SRM to delineate p-n junctions with equal dopant densities on both sides of the junction.

Since SRM data is not converted to dopant density data here, the profile doesn't look like the SIMS profile. However, the interpretation of the SRM profile given above matches the SIMS profiles quite well.

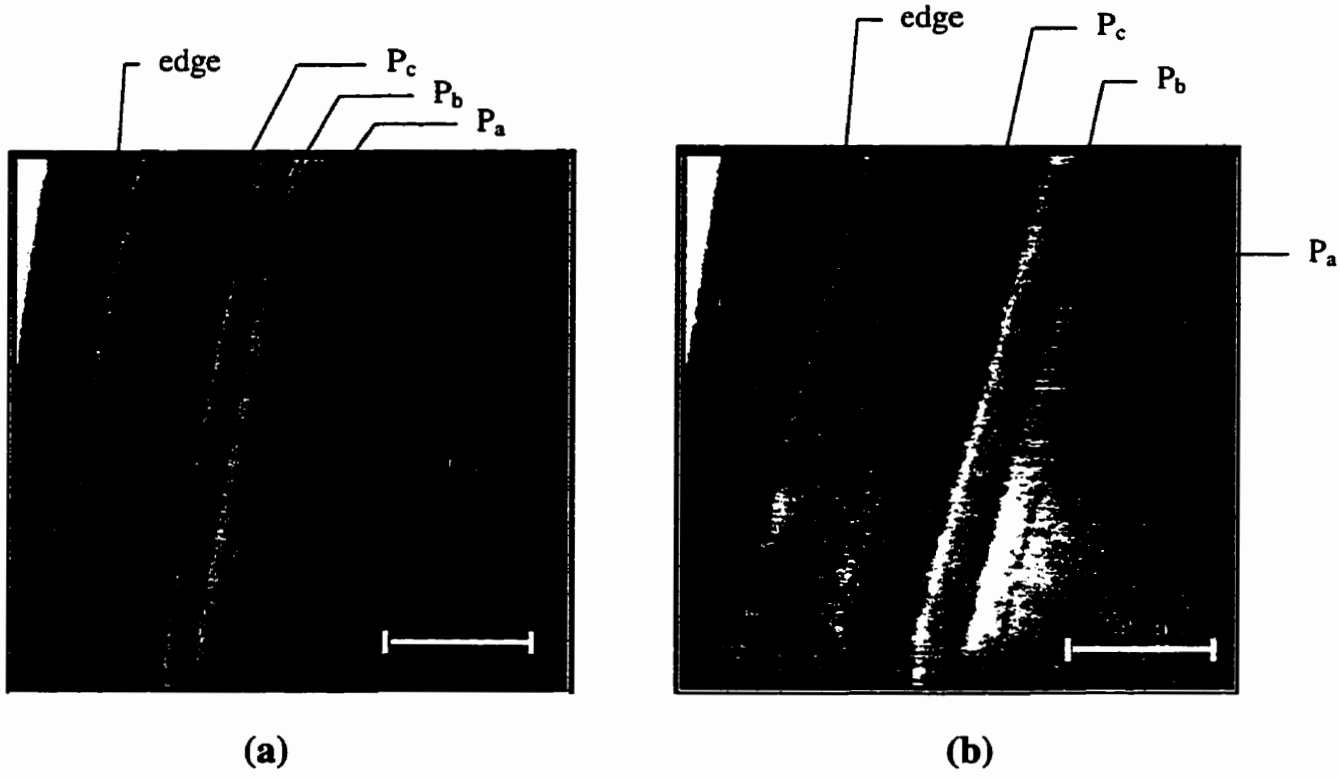
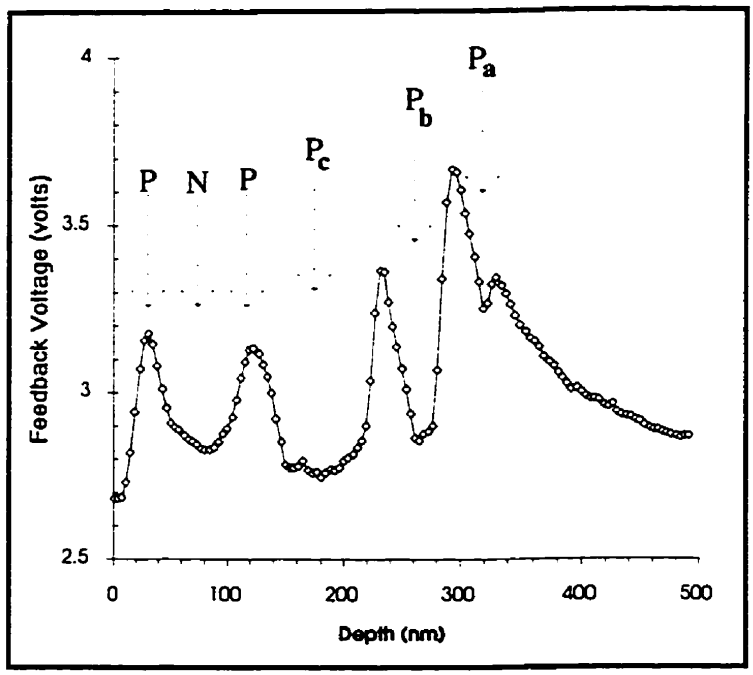
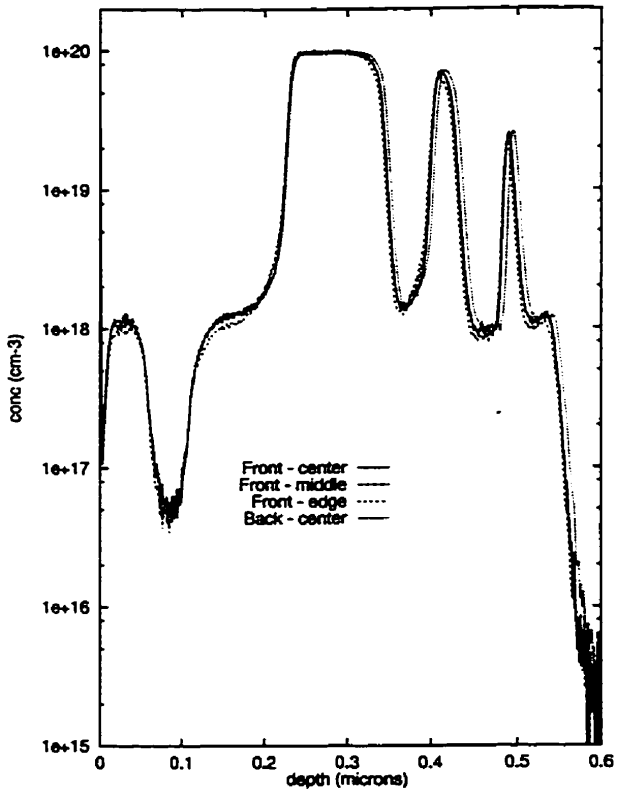


Figure 5.4 2D SRM images of round-robin sample #2 showing resistance contrasts in the region on the right hand side of the sample edge for a wider view (a) and a close up view (b). In both images the vertical dark lines (P_a, P_b, P_c) correspond to heavily doped p-Si plataues.



(a)



(b)

Figure 5.5 (a) shows line cross section profiles taken from the SRM image in Fig5.4(a), and (b) shows SIMS profiles of this structure cross section (source: Ref. [48])

5.4 IMAGING ROUND-ROBIN MOSFETs (0.4 μm)

In this section we present SRM results from imaging of p-channel MOSFET cross-sections with a nominal gate length of 400 nm. These devices were provided by SEMATECH as part of a round-robin project aimed at evaluating profiling techniques. The results from different groups are compiled by SEMATECH and a comparison of the data is published. These devices were fabricated in cascade with a pitch of 1400 nm as shown in the illustration below.

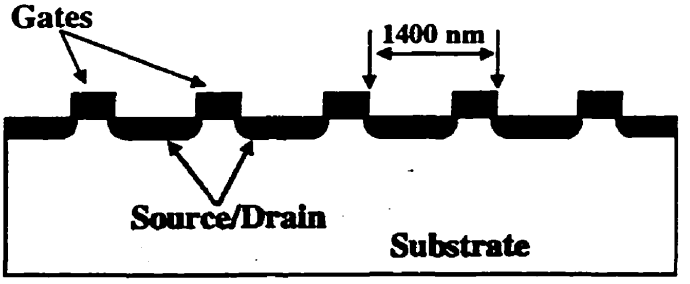


Figure 5.6 A schematic diagram of round-robin sample containing 0.4 μm MOSFETs.

The desired measurements from these devices are:

(i) channel length

(ii) gate length

(iii) Source/Drain junction depth

(iv) Dopant density profiles at the following locations;

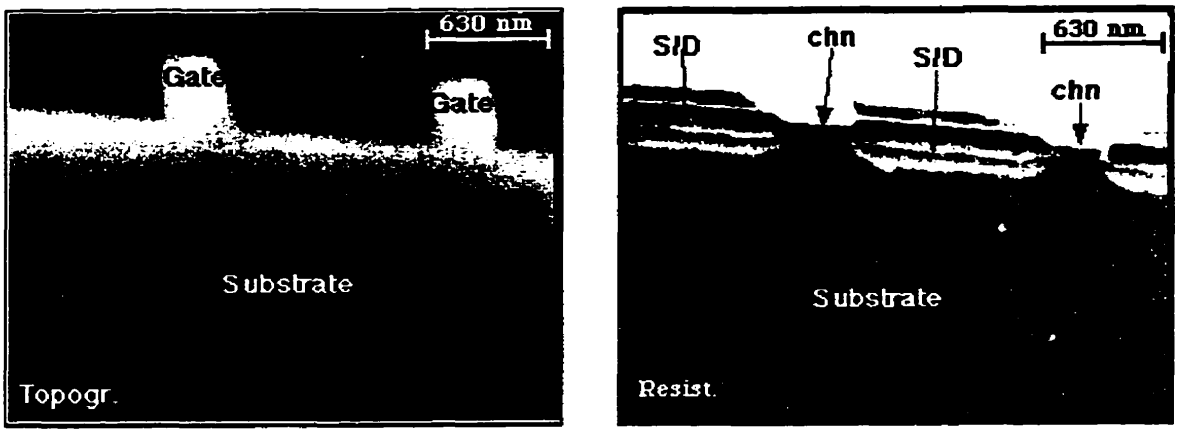
> horizontally along the channel

> vertically across the channel

> vertically across the source/drain region

> isoconcentration contours within the Source/drain at half-decade intervals

The sample was polished and mounted in cross-section orientation such that all the layers of interest are shorted to a common ground contact. However, the resistance of the gates as observed from the SRM results is very high suggesting that there is no direct contact between the gates and common ground contact. In this case topographic images are used to determine the position of the gate.



(a) (b)

Figure 5.7 Topographic (a) and resistance (b) profiles of two p-channel MOSFETs side-by-side.

The greyscale in all images in this section is interpreted as follows:

Profile / Greyscale	Bright Regions	Dark Regions
Resistance	High	Low
Topographic	Elevation	depression

Table 5.1 Interpretation of the grescale contrasts in for images in this section

Figure 5.7 shows the relative location of the MOSFETs in this round-robin sample. From these images one is able to measure the pitch of the devices in order to verify the calibration of

the x/y dimensions of the SRM piezoelectric scanner. The topographic image here shows that the gates are not symmetric. This is attributable to polishing. In Fig 5.7 (b) the source/drain regions labeled S/D is observed and the corresponding topographic image may be used to locate the position of the gate and hence the channel (chn). The substrate appears in dark shade of grey at the bottom of the image. Within the substrate region, there is a curved thin darker region. This region is attributed to a topographic coupling from a scratch mark created during polishing. The topographic image shows the scratch mark quite clearly. Notice that the S/D regions appear in dark shade at the surface and brighter towards the junction. This phenomenon will be explained latter in this section.

Figure 5.8 (a) shows a close up view of the channel region in the vicinity of a gate. The corresponding topographic profile is not provided for this image. In order to measure the channel and gate lengths line profiles were taken along the channel (A→A') on the resistance image and across the gate at half height from the topographic image (not shown here). Because of polishing the edges of the gate may be rounded and may therefore give a shorter gate length. The two profiles are plotted on the same x-axis (Figure 5.8 (b). From this graph the overlap of the source/drain regions with the gate is determine. The results are given in Table 5.3.

Figure 5.9, (a) and (b) show a resistance and topographic profile of the S/D region respectively. By taking a line cross-section vertically across the S/D the junction depth can be measured. Because of a topographic coupling artifact the resistance image shows that the top edge extends further than the actual edge of the silicon. This is because the side wall of the tip makes contact with the top edge even after the actual tip is past the edge. In order to determine the location of this top edge, the topographic profile across both the gate and the S/D are

superimposed. The two line cross-sections taken from each image at identical locations and plotted in the same axis (see Fig. 5.10) will be discussed in more details.

Both topographic line profiles (black dotted and solid curves) show a none-zero slope at displacements below 480 nm. This slope is a result of sample surface orientation. The topographic profile across the gate shows a small depression starting at 542 nm on the displacement axis which is attributed to the beginning of the gate. By correlating this profile with the resistance line profile taken across the gate and showing a transition from low to saturation resistance at 517 nm (red solid curve) it can be concluded that the bottom of the gate oxide is located at 517 nm. The thickness of the gate oxide is then determined to be 25 nm which is in good agreement with the expected value 20 nm [50]. The topographic line profile across the drain shows a monotonic drop beginning from 470 nm towards the right. The point of departure between the two topographic profiles doesn't coincide with the silicon top edge as shown by the resistance profile across the gate. This suggests that the top edge of silicon (most heavily doped end of the drain) is topographically dropping. The topographic drop in this region is attributed to preferential etching of the heavily doped drain by hydrofluoric acid (HF) during pre-SRM imaging cleaning step to remove native oxide.

Preferential etching by 2.5 % HF solution was observed on beveled cross-sections of MBE grown multilayer structures containing boron doped silicon (10^{19} cm^{-3}) and intrinsic silicon. AFM images showed that boron doped layers were topographically lower than intrinsic silicon layers.

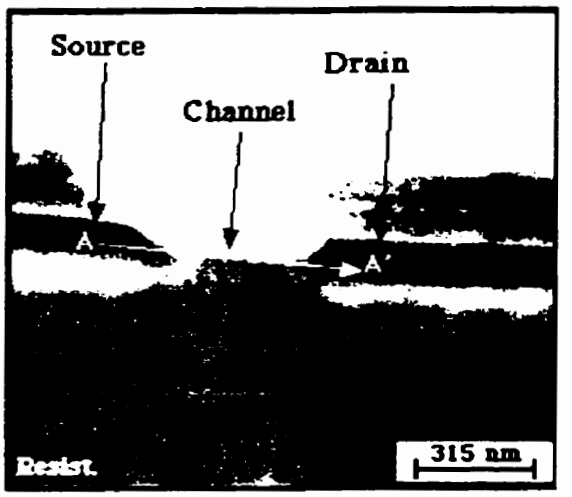
The p-n junction depth is determined from the resistance profiles across the drain (red dashed curve). The SRM tip is biased with positive polarity for all the data described in this section. Therefore, when scanning on the substrate (n-type silicon) the junction formed between

the tip and the surface is forward biased (Fig.3.13 of chapter 3). In these experiments the junction current was set at 2.5 nA. The resistance line profile across the drain in Fig.5.10 (red dashed curve) shows that the substrate resistance is constant at 1.5 GΩ from the beginning of the cross-section at "A" for 270 nm on the displacement axis. At this point the resistance starts increasing gradually up to 2.4 GΩ. This region corresponds to the transition from the n-type silicon substrate into the p-type drain. There are two reasons for the resistance to increase in this region: (1) There is a depletion region at the junction in which there no carriers, and the number of n-type and p-type dopants is roughly the same thus making this region behave like intrinsic silicon, and hence large contact resistance. (2) The positively polarized tip forms a reverse biased heterojunction (see Figure 3.13 of chapter 3) with p-type silicon resulting in higher resistance than the substrate. At the deep end of the drain the dopant density is still low enough to observe the inversion of the resistance at a p-n junction based on the dopant type change. However, as the tip scans towards the shallow end of the drain (heavily doped end) current transport across the tip-Si junction becomes dominated by tunneling current because the barrier becomes thinner. The contact resistance then drops drastically. The resistance curve shows a drop from 2.4 GΩ to 0.2 GΩ. Similar to the line profile across the gate, the resistance is expect to increase after 517 nm on the displacement axis. The "delay" is attributed to topographic coupling artifact resulting from a larger contact area between the edge of silicon and the side walls of the tip. The low resistance region at the top (beyond 567 nm) is attributed to some conducting layer that may have been deposited on the source/drain regions for ohmic contact purposes.

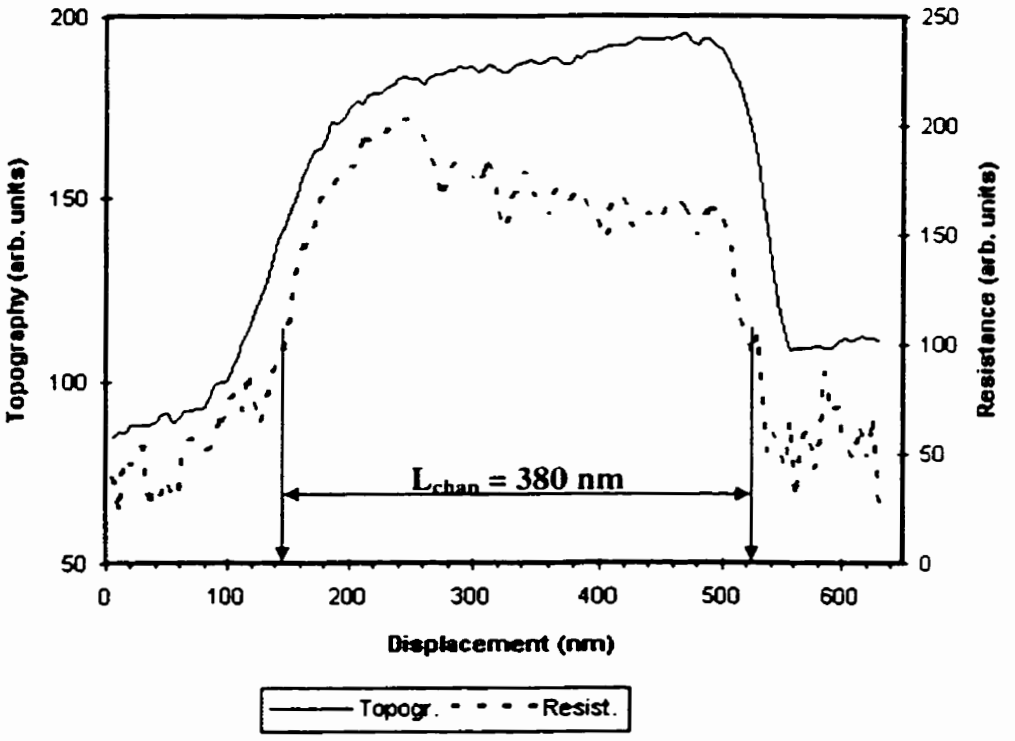
It is concluded that the drain region begins from 302 nm to 517 nm making the junction depth (X_j) 215 nm. The table below shows a summary of the results.

Parameter	Dimension (nm)
Junction Depth (X_j)	215
Gate Length (L_{gate})	403
Channel Length (L_{chan})	380
S/D/G overlap	11

Table 5.2 SRM measurements of parameters from Round-Robin (0.4 μm) MOSFETs

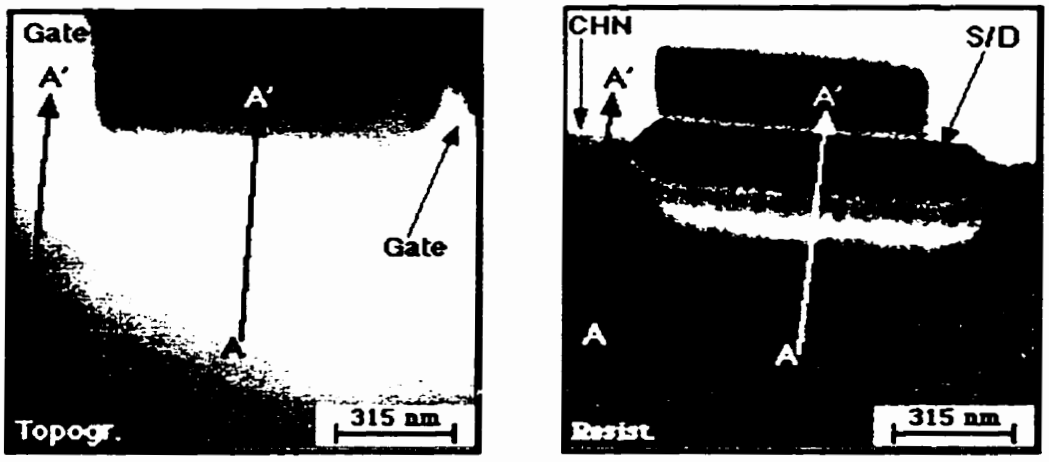


(a)



(b)

Figure 5.8 (a) Resistance profile showing a close up view of channel region. (b) Resistance and (simultaneous) topographic line cross-sections superimposed.



(a) (b)

Figure 5.9 Topographic (a) and resistance (b) profiles taken simultaneously in the S/D region.

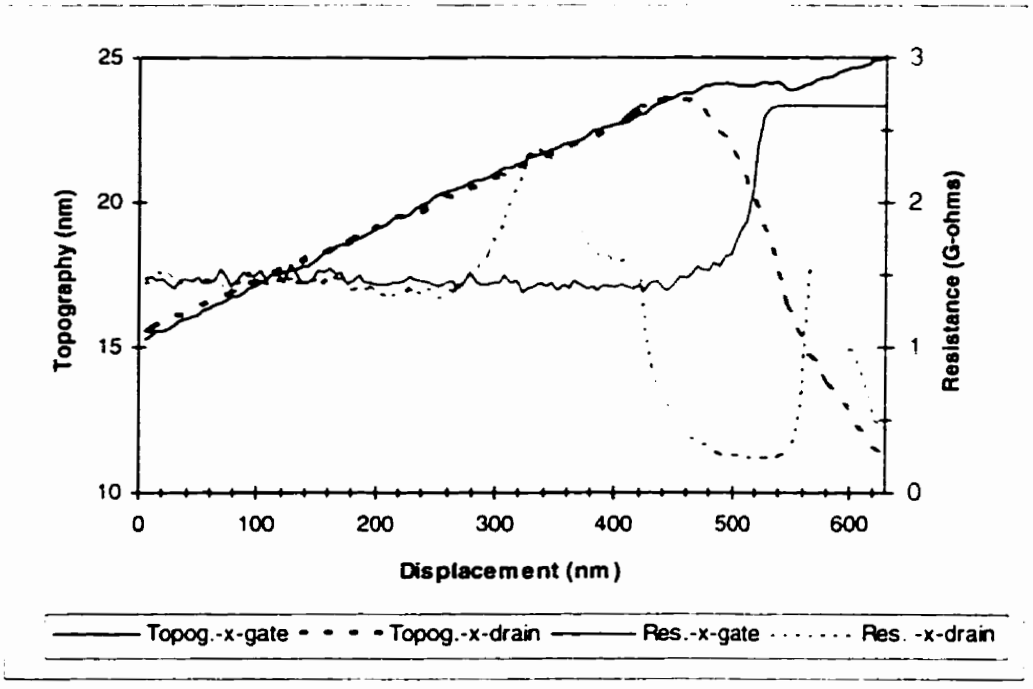


Figure 5.10 Line profiles of the taken from Fig.5.9 above at identical locations.

5.5 CONCLUSION

By performing SRM measurements on the SEMATCH round-robin samples and comparing with SIMS profiles some of the capabilities of the technique have been demonstrated.

Although SRM data has not been converted into quantitative dopant densities, the resistance measurements performed on structure #1 show that SRM is capable of delineating between regions of high and low carrier/dopant densities. Figure 5.2 shows a good demonstration of this capability where the resistance profile shows two peaks separated by a trough, a consequence of the dopant density variation between these regions. The dimensions of the separation between the peaks is within 20% of the specified values for this structure (Fig. 5.1) and SIMS profiles (Fig.5.2 c). It should be noted that the lateral dimensions shown on the resistance profile were measured on a 11° beveled cross-section. In order to make a direct comparison a factor of 5.24 should be used to re-scale the SRM data. The lateral resolution measured from the first step change in carrier density has been approximated at 30 nm.

The SRM measurements obtained from structure #2 demonstrate the following capabilities of the SRM: (1) can delineate shallow p-n junctions with a spatial resolution of 15 nm, (2) can resolve small p-type structures of nominal sizes 20 and 10 nm, fabricated with abrupt carrier density changes between 10^{18} cm^{-3} and 10^{20} cm^{-3}, giving a measurement of 33 and 13 nm respectively. It is interesting to note that the intensity of the peaks decreases monotonically with decreasing lateral size of the peaks. The same trend is observed with the SIMS profiles.

The SRM has been used to image p-MOSFET structures also provided by SEMATECH as part of a round-robin project. The results obtained here are quite comparable to those obtained by other groups.

CHAPTER 6
NANOPOTENTIAL MAPPING ON ACTIVE DEVICE CROSS-SECTIONS

6.1 INTRODUCTION

In order to characterize semiconductor devices several techniques that measure a variety of parameters on the device have been designed. For instance, SIMS provides direct information regarding the chemical composition in certain regions of the device, while SPM based techniques such as SCM, SRP, nano-SRP and SRM measure 2D carrier density profiles. Calibration procedures are then used to convert carrier density data into dopant profiles. The data obtained from these techniques is then used as input for process and device simulation tools. Simulation tools then provide information that is used to evaluate the device performance under normal operation. A common attribute to all these techniques is that measurements are performed on devices that are not in their normal operation mode.

In order to evaluate the impact of process variation the semiconductor industry depends on measurements of the I-V characteristics of active devices, and by extracting relevant parameters from the I-V data, the process is adjusted accordingly. Recently, T. Trenkler et al reported a technique for carrying out local surface potential measurements on the cross-section of active CMOS transistors using a contact mode AFM equipped with a conductive tip (Nanopotentiometry) [51]. In order to carry out a potential measurement in this technique, Trenkler et al sectioned a device in such a way that its cross-section was exposed. The device was then biased so that it assumes its normal operation. A conductive AFM tip attached to a high impedance voltmeter was scanned on the device cross-section and a 2D potential profile was measured.

Performing local potential measurements on active devices using SPM technology is perhaps a more direct method for evaluating the impact of process variation. This technique is capable of providing an good insight into the physical parameters of a device because the potential profile reflects the activity inside the device during its normal operation.

We have taken the nanopotentiometry approach to study the behavior of CMOS devices in their normal operation. The aim is to perform a 2D surface potential map of a device cross-section with high enough spatial resolution and sensitivity to observe the formation of the channel as the device bias conditions are changed. In this chapter surface potential measurements performed with a probe tip on cross-sections of a functionally operational devices (even after sectioning) are presented. This technique is basically similar to that reported by Trenkler et al [51]. The basic structure of a MOSFET is shown schematically in Fig. 6.1.

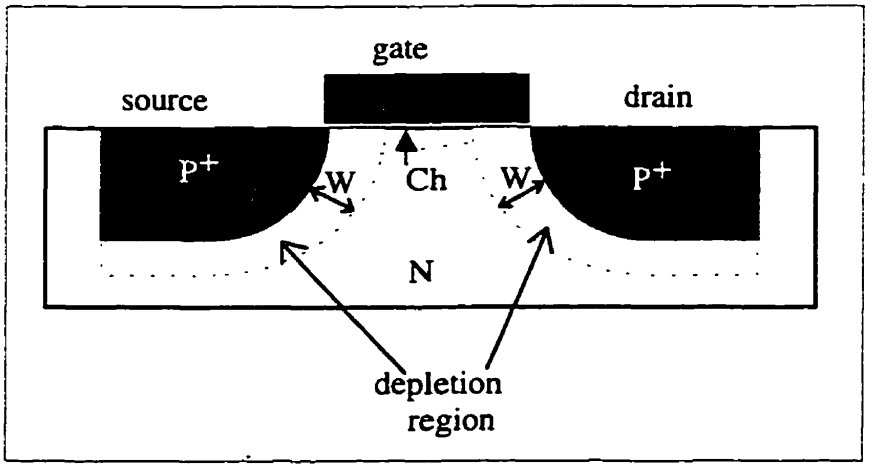


Figure 6.1 Basic structure of a p-channel MOSFET showing depletion regions of width "W" and the channel region indicated by "Ch".

With device dimension shrinkage the dopant density in the region "Ch" is being increased (now $\approx 10^{17}$ cm^{-3}) in order to reduce the extent of the depletion width in this region. This minimizes

the chances of short channel effects and punch through. Nanopotentiometry will be used to map out 2D potential profiles in the region "Ch" while the device is in its normal operation. The data obtained here may provide information regarding depletion width and an insight into the effect of increasing the dopant density in this region. This technique is a more direct way of evaluating device fabrication processes compared to the dopant profiling techniques discussed in chapter 1 because this data is obtained while the device is in operation.

6.2 POTENTIAL MEASUREMENT USING A CONDUCTIVE PROBE TIP

Localized potential measurements were performed using a conductive probe tip (boron doped diamond tip) attached to the closed loop potential sensing circuit shown in Fig. 6.2.

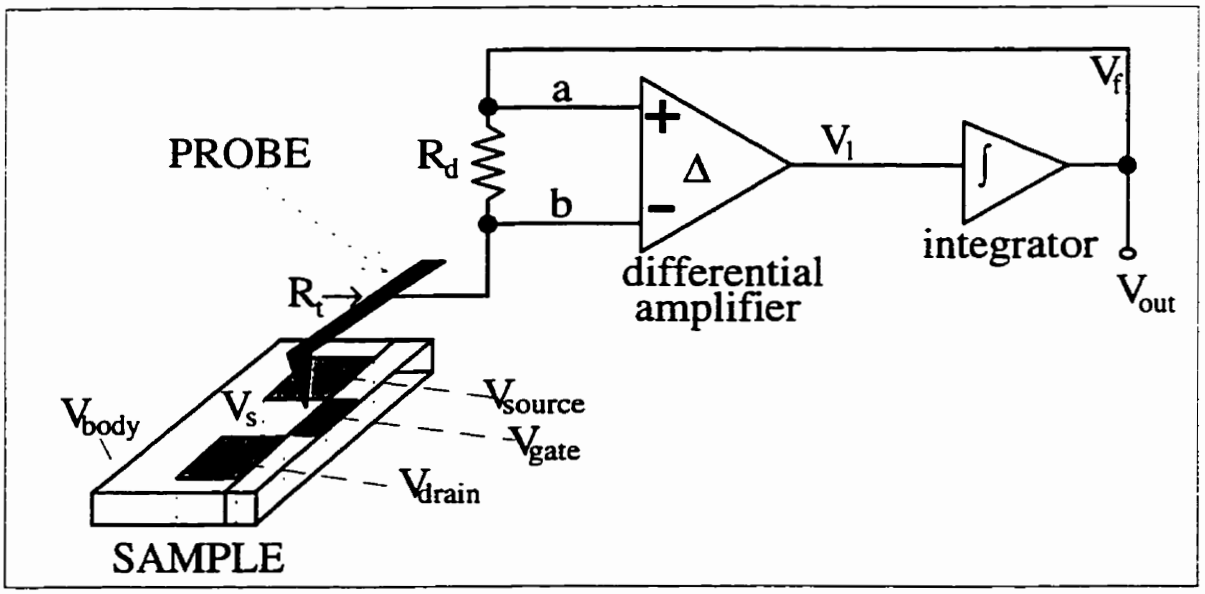


Figure 6.2 A schematic diagram of local potential measurement circuit. Here R_t and V_s represent the tip resistance and local surface potential respectively.

A MOSFET input stage operational amplifiers with input impedance of 10^{12} Ω have been used to build a standard three op amp differential amplifier. A balance potentiometer is utilized at

the input stage of the differential amplifier in order to reduce offset current. The noise level at the balance point was measured to be 5 mV_{p-p}.

Ideally, potential measurements on an active device should be performed without loading the circuit through which the device-under-test is biased. This implies that the presence of the tip in contact with the surface of the active device should not draw current from the device circuit during surface potential mapping. In Fig.6.2, this means that the condition $V_f - V_s = 0$ must be satisfied. Analysis of this circuit in closed loop mode shows that the feedback voltage (or output voltage) is given by

$$V_f = -\frac{gK}{RC}\int (V_f - V_s)dt \qquad (6.1)$$

where g is the gain of the differential amplifier, $K = \frac{R_d}{R_d + R_t}$, and R and C are the input resistor and feedback capacitor of the integrator stage. In order to maintain the sensitivity of the circuit high R_d must kept high, but lower than the input impedance of the first stage of the differential amplifier. R_d was set at 10MΩ.

The circuit in Fig.6.2 was tested by using a square wave signal to simulate the surface potential V_s and a 20MΩ resistor to simulate the tip resistance. A time constant of 5ms was measured for this value of R_t whereas for $R_t = 0\Omega$ a time constant of 25 μs was obtained. This implies that the recovery time for the closed loop system is degraded by large tip resistance.

6.3 CONTACT FORCE CALIBRATION

This section provides a discussion of calibration of the contact force necessary to make a stable and reproducible potential measurement on the surface of a semiconductor.

A uniformly doped p-type silicon substrate (1.2×10^{17} cm^{-3}) was biased with 2V d.c., and the tip was loaded on this surface. The force control loop was engaged and starting at 0 N the output voltage was monitored as the force was gradually increased. Figure 6.3 shows measured surface potential as a function of the force between the tip and the sample.

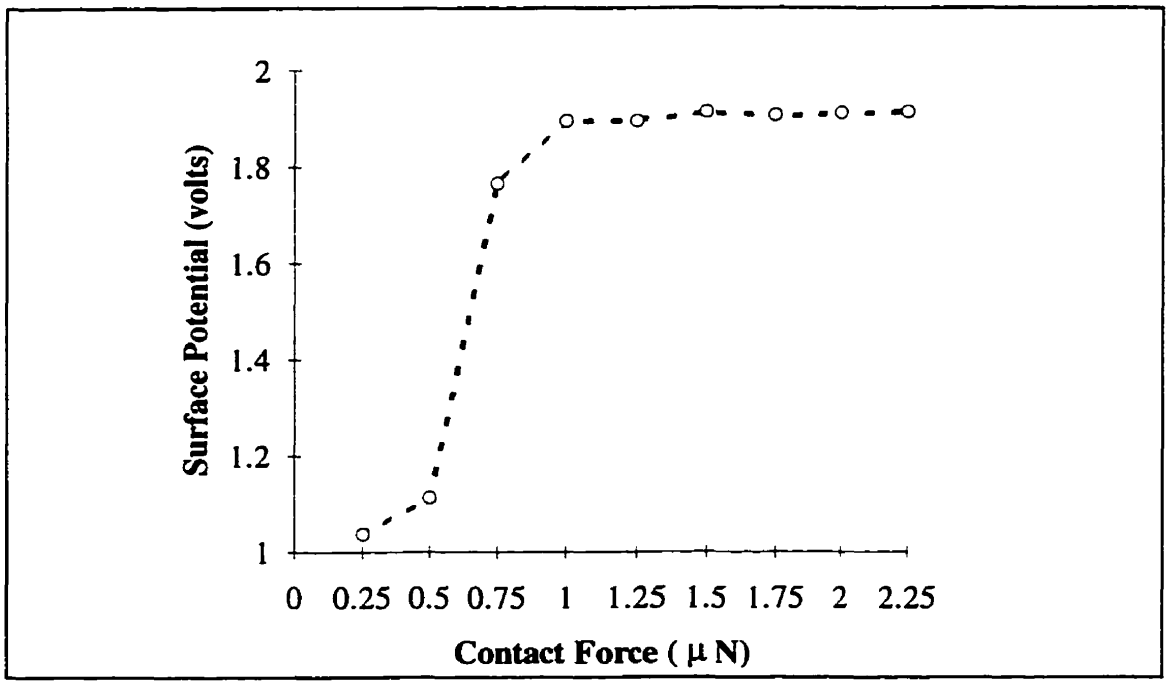


Figure 6.3 Measured surface potential as a function of tip-surface contact force when 2V is applied to the substrate.

This graph shows that the force necessary to measure 95% of the applied substrate potential on a silicon surface with the diamond tip is 1μN. At this force the circuit measures 1.91V while 2V is applied to substrate. Increasing the contact force beyond 1μN did not bring the measured voltage

any closer to 2V. This experiment was done only on a silicon surface. The discrepancy between the measured and applied voltage is attributed to voltage drop across the sample from the back contact to the measurement point. This means that approximately 0.1V drops across the sum of spreading, contact and the tip resistance.

6.4 TWO-DIMENSIONAL POTENTIAL PROFILES ON ACTIVE MOSFETS

6.4.1 Sample Structure And Preparation

Surface potential measurements were performed on polished sample cross-sections. The sample preparation and polishing procedure described in chapter 2 was followed to prepare these cross-sections. Since the samples are not passivated and bonding wires were exposed, no backup substrate was attached to the top surface here. However there is a 1.5 μm thick oxide layer above the substrate in which the first metal layer is fabricated. The oxide layer prevents the tip from falling over the edge of the sample during a scan.

The sample used for this experiment is a special structure consisting of an array of three p-channel and three n-channel MOSFETs. Each set of transistors (p-channel or n-channel) is connected in parallel. This means that the gate, source and drain of each transistor in each set are connected to a common pad. The nominal gate lengths for these MOSFETs is 3 μm. Standard bonding wires were attached to the bonding pads so that the transistor set could be biased appropriately. The sample also consists of three inverters, which are also connected, in parallel. The inverters are made of transistors with a channel length of 1 μm. All transistors in this structure extend approximately 1mm along the direction perpendicular to the gate length. The length of these structures allows for polishing the cross-section of the structure without affecting

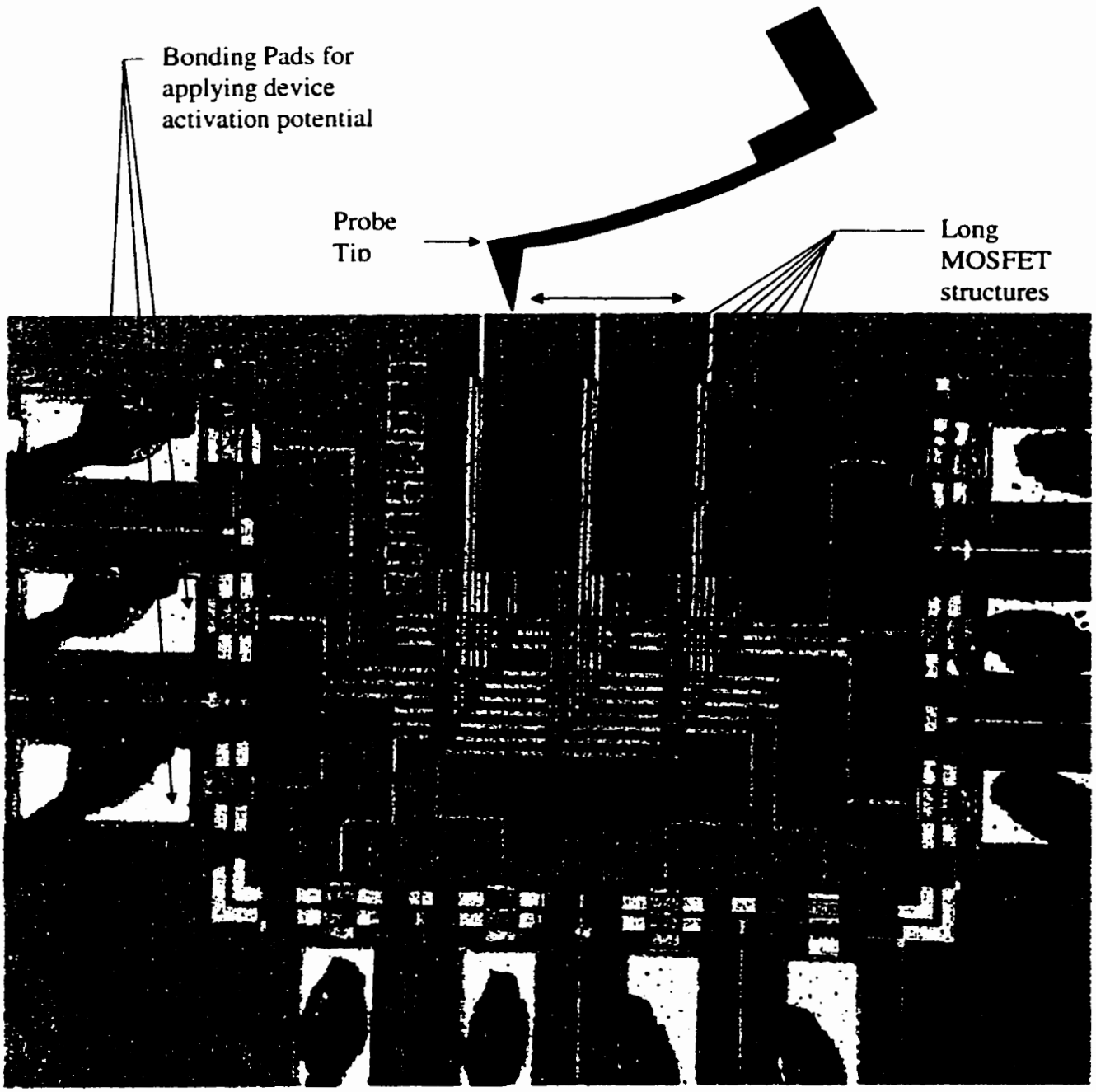


Figure 6.4 A photographic image of the surface layout showing six long transistor structures and three inverters as well as wire bonding pads. The drawing of a probe tip at the top illustrates the polished and imaged cross section of the structure. (Fabricated by Nortel through CMC)

6.4.2 I-V Characteristics After Sectioning

Current-voltage measurements were carried out using a 4145A HP Semiconductor Parameter Analyzer. These measurements were done after the devices were sectioned in order to verify that they were still functionally operational. Figure 6.5 (a) and (b) shows I-V characteristic curves for the p- and n-channel transistors respectively. Also shown are the corresponding I_{ds}-V_{gs} curves demonstrating the threshold voltages for each set of transistors.

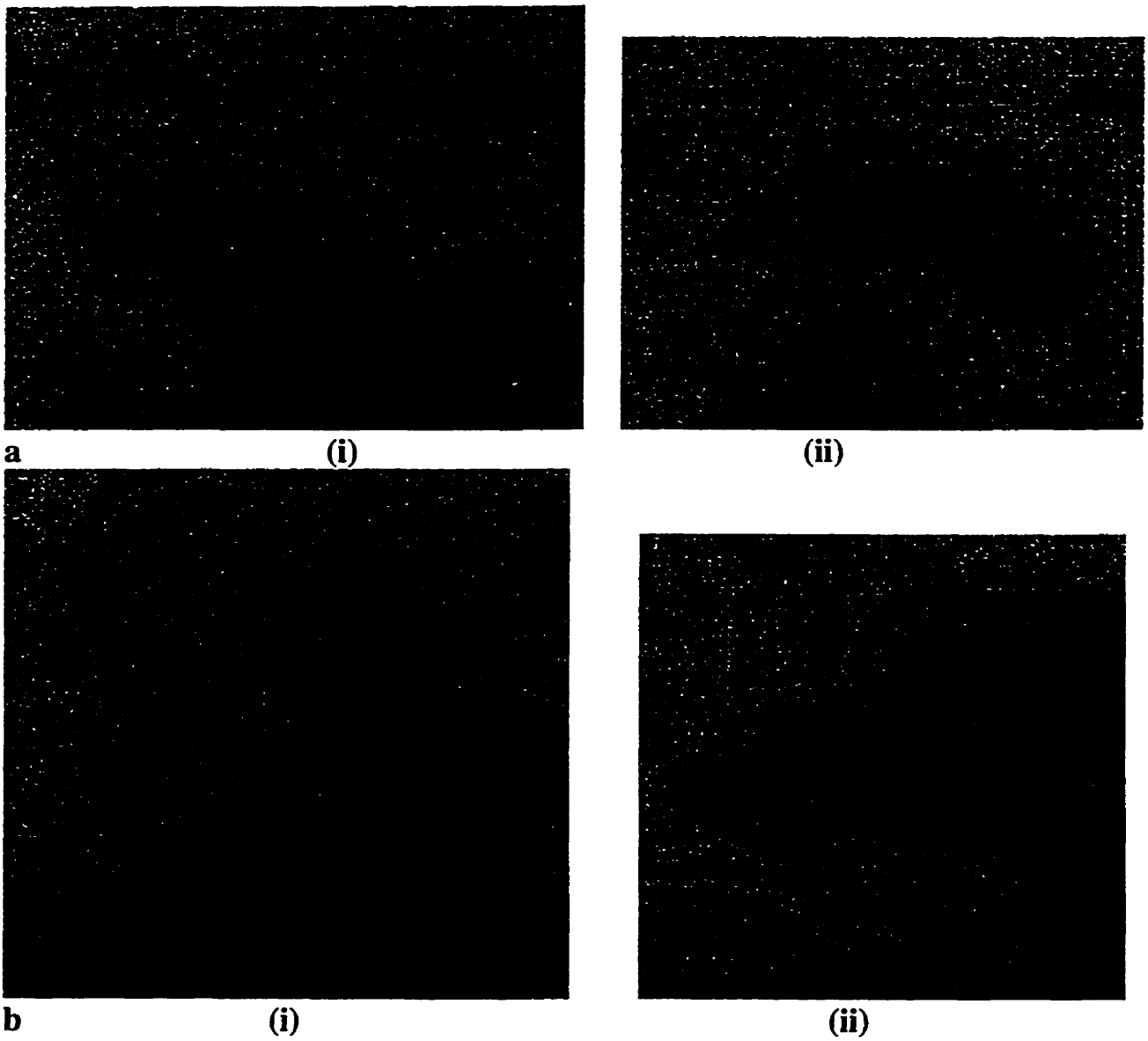


Figure 6.5 I-V characteristic curves for (a) a p-channel and (b) a n-channel MOSFET with corresponding I_{ds} Vs V_{gs} curves (ii) showing threshold voltages for the sectioned devices.

6.5 EXPERIMENTAL RESULTS

Although the results shown here are preliminary, they do demonstrate the ability for the technique to map out 2D potential distribution on active MOSFET cross-sections. The results shown here were obtained from imaging 3 μm p-MOSFETs. Figure 6.6 shows the bias conditions of the p-MOSFET during this measurement. The gate voltage was varied from 0V to -2.5V as shown in Fig.6.7.

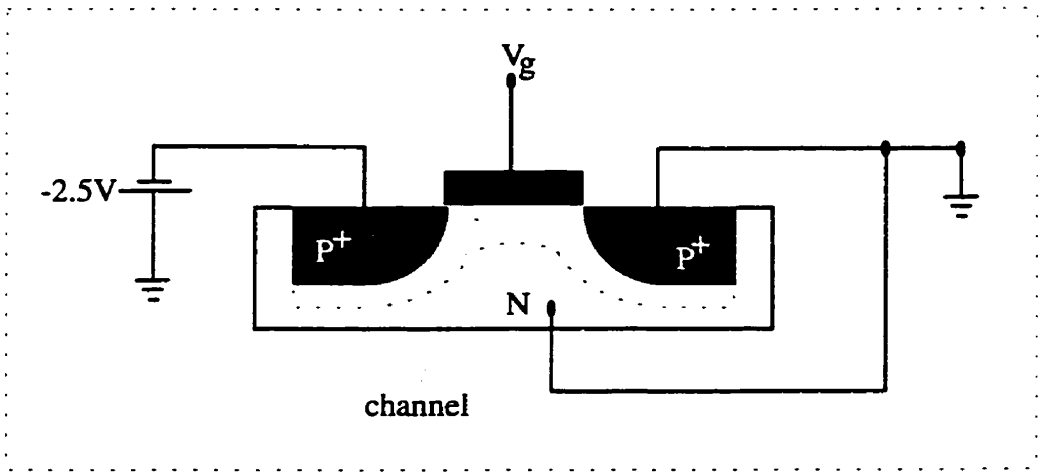
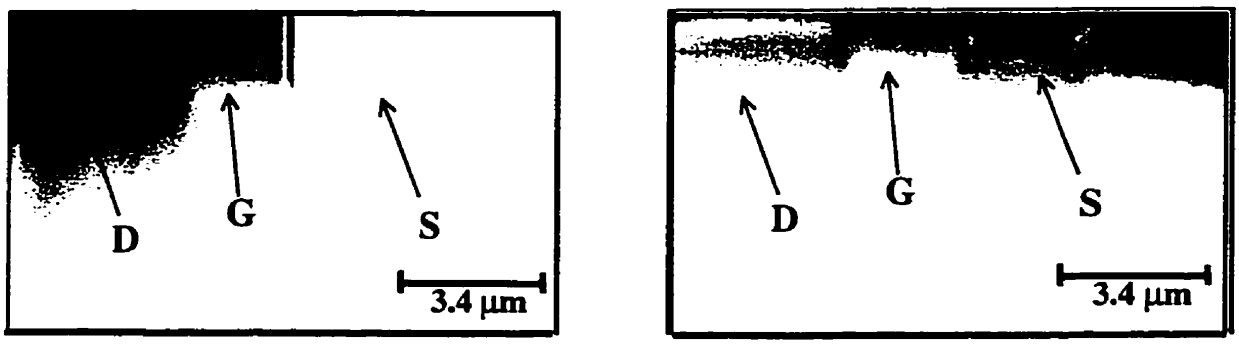


Figure 6.6 A schematic diagram showing the bias conditions for a p-channel MOSFET during nanopotential imaging.



(a) (b)

Figure 6.7 Cross-sectional images showing surface (a) potential and (b) topographic profiles on a p-channel MOSFET. Topographic profile is used to locate the gate "G", source "S" and drain "D".

6.5.1 Discussion of Results

Figure 6.7 (a) and (b) show a surface potential map and a topographic image of a p-channel MOSFET respectively. The topographic image (b), taken simultaneously with the surface potential profile, is used to identify the features observed in the surface potential image (a). The former shows clearly the location of the gate at the top of the image. This position corresponds to the region labeled "G" on the potential image. The drain is biased with a -2.5 V d.c. potential with respect to the source. The drain is identified as the very dark region located at the top left corner on the surface potential image while the source shows the same bright contrast as the rest of the substrate. The gate is biased at -0.9V and hence on the grayscale, it is not as dark as the drain. The contrasts observed in this potential profile is consistent with the expected results.

However, spatial resolution (top-to-bottom) on the potential profile is quite poor. While the image clearly shows contrast between the drain and gate potentials, each potential level extends further than the expected edge of the gate or drain. This is a result of an artifact caused by the resistance of the tip (R_t). The time constant of the closed loop measurement circuit is much higher than the measured value (5ms) when the tip resistance is simulated with a 20MΩ resistor. This implies that the actual tip resistance is much higher than the test value.

For these measurements a boron doped diamond tip was utilized. Upon testing the conductivity of the tip by performing SRM measurements on "donut" samples, it was observed that the conductivity of the tip had decreased significantly compared to earlier results obtained with the same tip on this same "donut" sample. Unfortunately this was the last doped diamond

tip available (production has been discontinued). We have observed the same conductivity degradation of these tips with time while performing other experiments (SCM and SRM).

As an alternative, usage of metal tips was undertaken. For this experiment, metal tips have the advantage of lower contact resistance. This means that the time constant of the closed loop measurement circuitry is improved. However, metal tips wear out quite easily as described in section 2.3. Furthermore attaching bonding wires to the devices, as shown in Fig. 6.4, makes it very difficult to mount the sample with a backup wafer as shown in Fig. 2.6. This means that the tip falls off the edge of the sample occasionally thus increasing the chances of metal tip bending and getting damaged as the tip recovers to the surface of interest. The artifact introduced by diamond tip resistance was confirmed by imaging the same structure with a tungsten tip and obtaining Fig. 6.9.

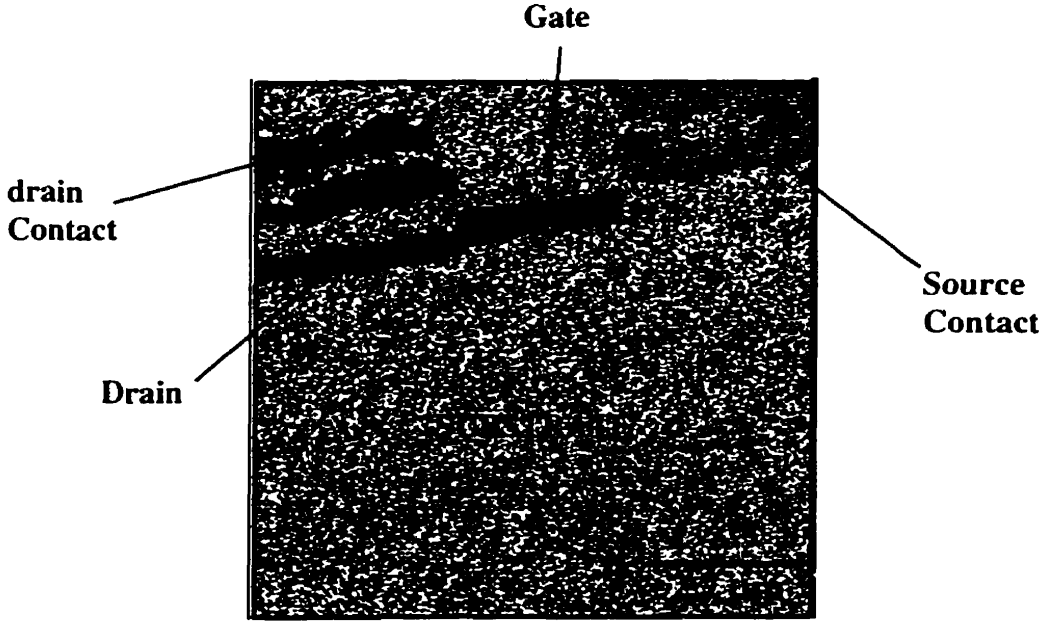
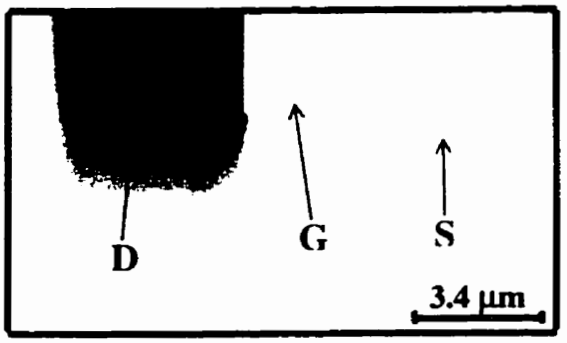


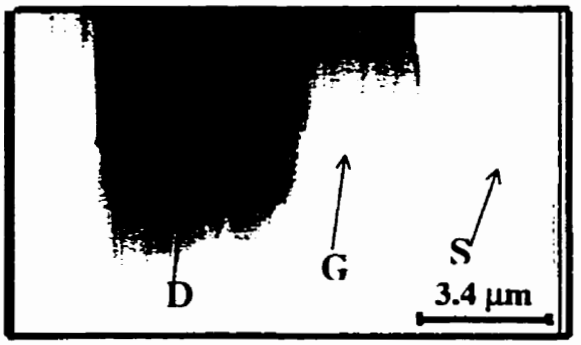
Figure 6.8 A surface potential profile on the cross-section of an active p-channel MOSFET obtained using a tungsten tip. The bias conditions are as shown in Fig. 6.7 with $V_g = -1.5V$.

Figure 6.9 shows the source, drain and gate of an active p-channel MOSFET. As a result of the short lifetime of the tip, scanning could only be done once and the surface and/or tip changes very significantly by the second scan. To do this experiment, at least three scans are required to measure the surface potential for least three different gate voltages. Therefore, usage of metal tips proved to be very difficult in doing this experiment.

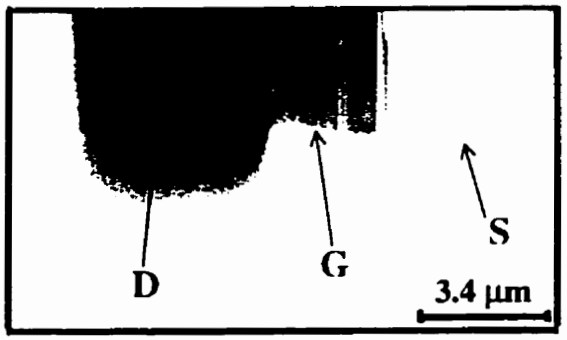
The images shown in Fig. 6.10 are surface potential profiles taken over the p-channel MOSFET structures with the diamond tip. The location of the gate is the same as that shown in Fig. 6.8. Different gate voltages starting from 0.2V decreasing in discrete steps down to -2.0V were applied as shown. Figure 6.10 (i) and (ii) do not show any contrast between the gate and the source in the greyscale levels. This implies that since the gate potential is very close to the source voltage and the transistor is still in the linear mode of operation. However, Fig.6.10 (iii) up to 6.10 (v) show that the magnitude of the gate potential is gradually increasing. According to Fig.6.6 (ii), the channel should be turned on at a threshold voltage of -0.75V. This means that the channel is gradually forming as the gate potential is decreased from -0.9V to -2.0V. Qualitatively, these results are consistent with Fig.6.6 (ii). Using a more conductive diamond tip will improve the sensitivity and spatial resolution, and hence channel formation can be observed on the images.



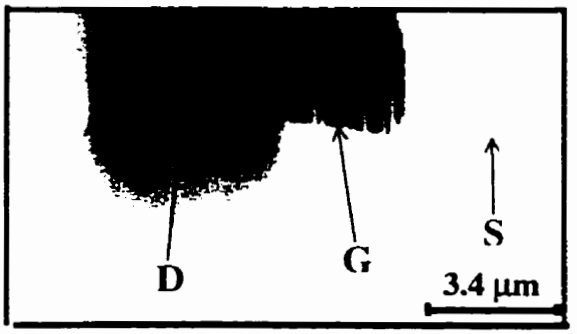
(i) Vg = 0.2 V



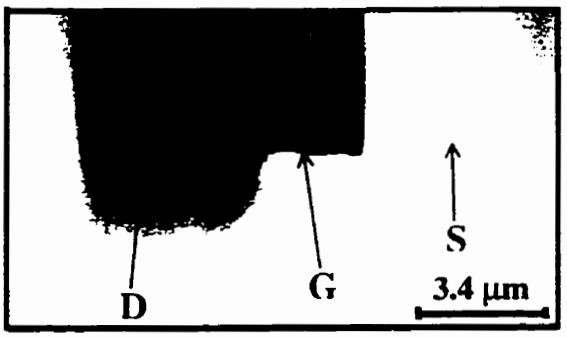
(ii) Vg = -0.3 V



(iii) Vg = -0.9 V



(iv) Vg = -1.5 V



(v) Vg = -2.0 V

Figure 6.9 Potential profiles on the cross-section of an active p-channel MOSFET as the magnitude of the gate potential increases. The location of the gate is approximately the same position as shown in Fig. 6.8.

6.6 CONCLUSION

Mapping the potential profile on the cross-section of a device in its normal operation is a more direct technique of characterizing semiconductor devices. One of the key requirements for this technique's success is performing the measurement without loading the device. The probe must be attached to a high input impedance voltmeter and draw as small a current as possible.

The results presented in this chapter demonstrate the feasibility of the technique. A polished cross-section of a p-channel MOSFET structure was biased and the gate potential was changed in steps of about 0.5V from off state until the channel was turned on. At each step a 2D potential profile was taken on the cross-section. The results show voltage contrasts that indicate differences in grayscale levels on the gate implying different gate voltage. The intensity of the signal at the gate increases with decreasing gate voltage. The resolution obtained in these results is quite poor. No activity is observed in the channel. To enhance the signal level so that the channel can be observed, a highly conductive and very sharp tip is required. For this experiment a doped diamond tip was utilized. Diamond tips have very good mechanical properties (hard and none-reactive) but are not conductive enough.

A draw back of nanopotential mapping is the fact that it requires sectioning of the device and maintaining its operational I-V characteristics. Sectioning a real device and still retaining its good operation when it is biased may be quite challenging in view of the ever-decreasing device sizes.

SUMMARY

Scanning probe microscopy is, so far, the key technology that is capable of meeting the challenges posed by rapid advances in semiconductor technology with regards to development of faster and very large scale integration (VLSI) of devices. These devices are now produced with ultra-shallow p-n junctions. This is according to the projections of SIA [2a, 2b], stating that the next generation CMOS devices will require a source/drain depth of 70 nm for 0.18 μm gate length, 50 nm for 0.13 μm gate length, and so on, at a substrate doping level of 1×10^{17} cm^{-3}. Accordingly, SEMATECH has recognized SPM technology as the key towards solving the critical problem of characterizing these devices with nanometer scale spatial resolution.

A SPM based technique for mapping out carrier profiles in 2D with nanometer scale spatial resolution, Scanning Resistance Microscopy, has been demonstrated in this thesis. The initial work in scanning resistance microscopy was done by Dr. C. Shafai [29]. In his work, Shafai used electrochemically etched metal tips, mounted on an AFM stage, to perform one and two dimensional resistance profiles on p-n junction test structures. Shafai operated SRM in constant voltage mode. Using the metal tips to perform 1D imaging across a p-n junction formed by a shallow boron implant on a n-type substrate, Shafai was able to delineate a p-n junction with a spatial resolution of 35 nm [34].

In this thesis, I have presented the first prototype SRM instrument as well as drastic modifications to the technique. This recently developed version of the instrument has been used to image a wide variety of semiconductor devices and test structures. The SRM has proved to be a reliable tool for performing p-n junction delineation with as high as 20 nm spatial resolution on state-of-the-art devices. Metal imaging probe tips have been replaced with conductive diamond tips because of the superior mechanical properties of diamond and its chemical inertness to most

semiconductors. A calibration procedure has been established which should provide a way to obtain quantitative information from SRM data. To date, we have not found a reliable source of well-characterized conductive diamond or diamond coated microfabricated silicon tips.

The prototype of the SRM was designed, constructed and systematically tested in the laboratory. This technique measures localized **contact** resistance, in 2D, at the interface of a sharp conductive probe tip and a semiconductor surface. It has been demonstrated that this **contact** resistance is a function of the tip bias potential (with respect to the sample under test), tip-surface contact area, and the local substrate dopant density and type. Simulations of the tip-surface junction show that by controlling the interface current and measuring the tip voltage necessary to cause the set current (constant current mode SRM), a higher measurement dynamic range is achieved compared to applying a constant voltage to the probe and measuring the current (constant voltage mode SRM). By imaging devices on polished cross-sections I have demonstrated that the SRM is capable of delineating p-n junctions with a 20 nm spatial resolution.

Metal probe tips wear out very quickly when imaging real cross-sections thus degrading the resolution. Boron doped diamond tips have replaced the metal tips because the latter is mechanically harder therefore exhibits longer life times. The use of diamond tips significantly improved the spatial resolution of SRM.

SRM results obtained from imaging 0.8μm MOSFET structures reveal source/drain extensions that are a result of the presence of lightly doped drains. SRM images of MBE grown SiGe multilayer structures clearly demonstrate the diffusion pattern of boron that results from heat treating the sample in the presence of a metal electrode at the surface. Imaging round-robin test structures (#2) demonstrated that SRM is capable of delineating between high (10^{20} cm^{-3})

and medium (10^{18} cm^{-3}) dopant density. I imaged 0.4 μm MOSFETs (a round-robin project) and the results obtained are comparable with those obtained by other research groups using different techniques. SRM has also been used to perform contract work for some major microelectronic companies (Nortel, Gennum Corporation, and Semiconductor Insights) in addressing device performance problems. The SRM results are mainly qualitative.

Calibrating the instrument has presented some problems because the technique is sensitive to surface conditions. This implies that calibration must always be done prior to imaging. Prior to imaging, a surface must be cleaned with hydrofluoric acid (HF) solution to remove native oxide. Low contact force (< 20 μN) and positive probe bias is preferred in order to avoid surface modification by the tip. Such surface modification may be a result of field enhanced oxidation of the sample surface. Keeping the scanning environment dry also helps to minimize field enhanced oxidation.

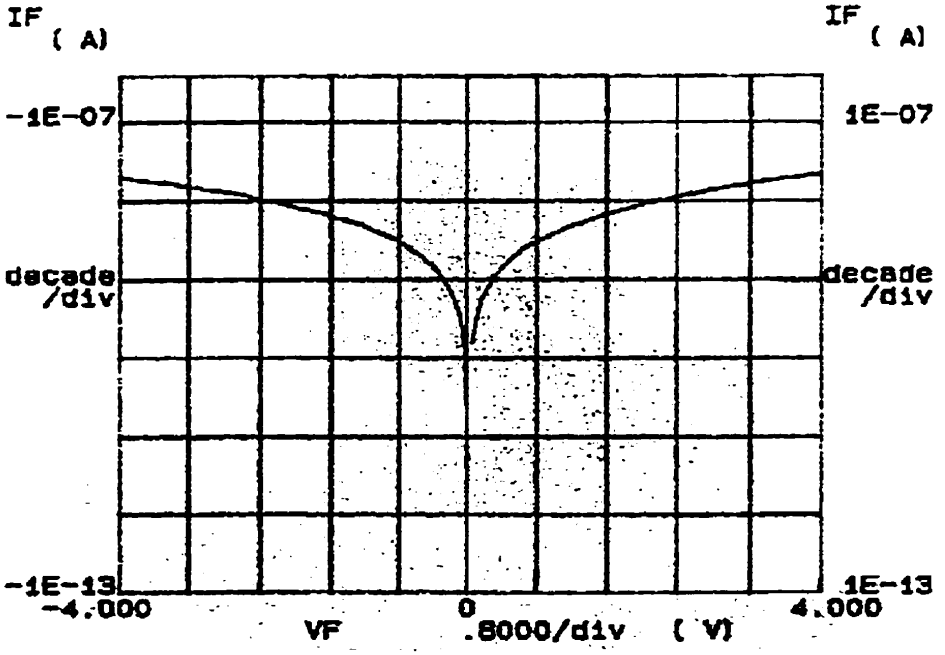
A surface potential mapping technique for characterizing semiconductor devices in their normal operation mode has been demonstrated. This technique offers a more direct way of evaluating the impact of process variation because the measured potential directly reflects the activity inside the device. A disadvantage of this technique is that one requires that the sectioned device under test be functionally operational even after sectioning to expose the cross-section. This may be a challenge especially in light of device dimension shrinkage. Furthermore, the potential measuring system must have minimal loading to the device circuit.

APPENDIX A

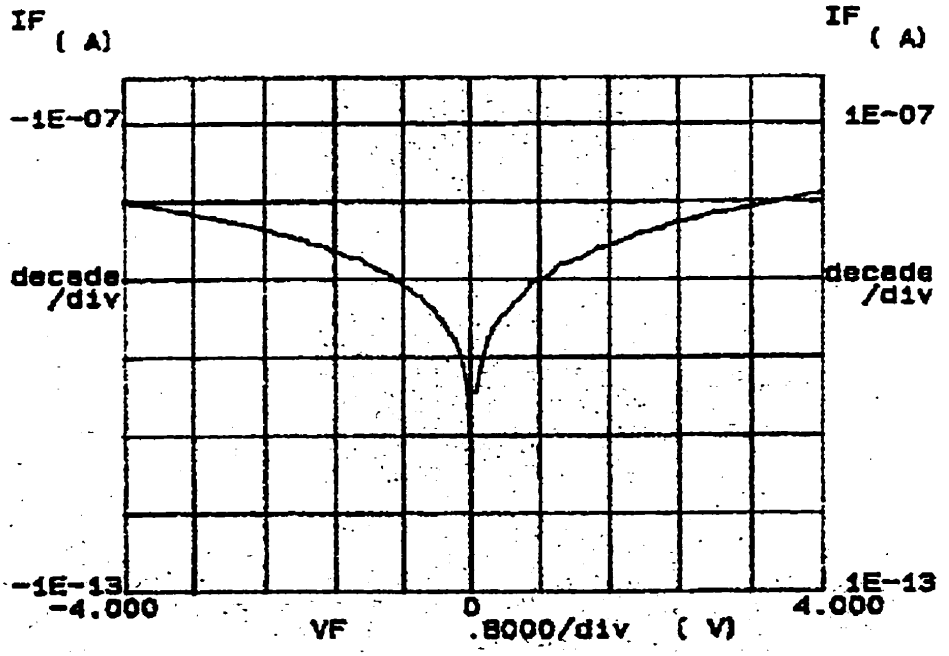
A boron doped diamond tip was placed in contact with silicon surfaces with the contact force maintained at 1μN. Current-voltage characteristcs of the heterojunction formed at the contacting point were measured using a HP 4145A Semiconductor Parameter Analyzer by ramping the tip potential relative to the substrate between -4V and +4V and monitoring the current.

I-V measurements were carried out on silicon substrates with dopant densities varying from 5×10^{14} cm^{-3} to 3×10^{19} cm^{-3} for n-type and from 3×10^{15} cm^{-3} to 6×10^{19} cm^{-3} for p-type. Figures (A-i) through (A-vi) (on following pages) show I-V characteristic curves for n-type silicon and Figs. (A-vii) through (A-xii) show I-V curves for p-type substrates. A summary and discussion of these results is given in Fig.3.11.

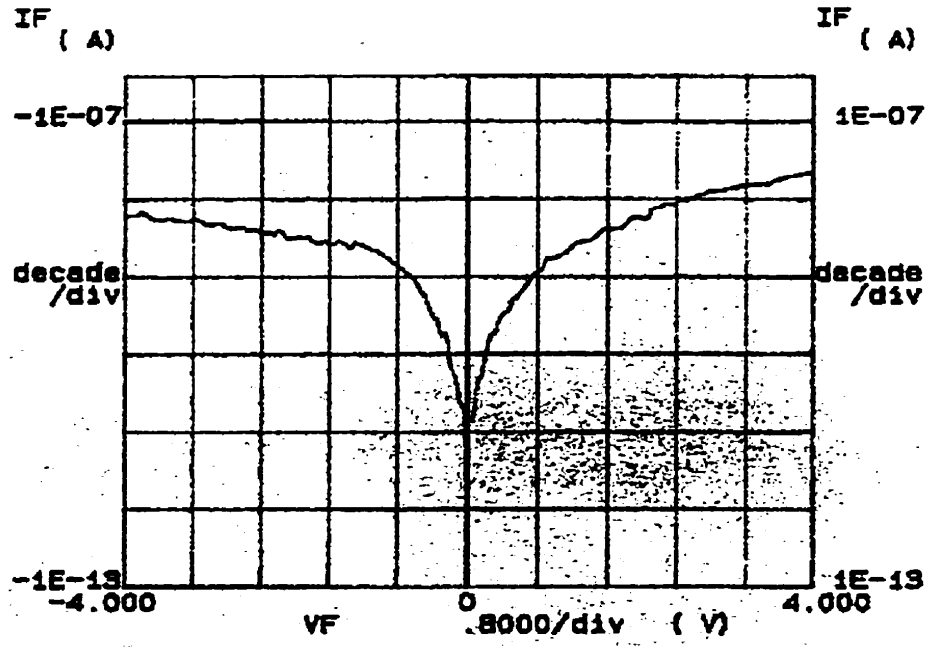
Figure (A-xiii) shows a comparison between n-Si (3×10^{17} cm^{-3}) and p-Si (1.2×10^{17} cm^{-3}) I-V curves. This figure demonstrates that at positive tip bias, at this doping level, the current flowing across the junction is approximately one order of magnitude higher on n-Si than p-Si. For negative tip polarization this figure shows that the current is approximately the same magnitude for both types of silicon doping. However, at higher substrate doping there isn't as much difference in positive current.



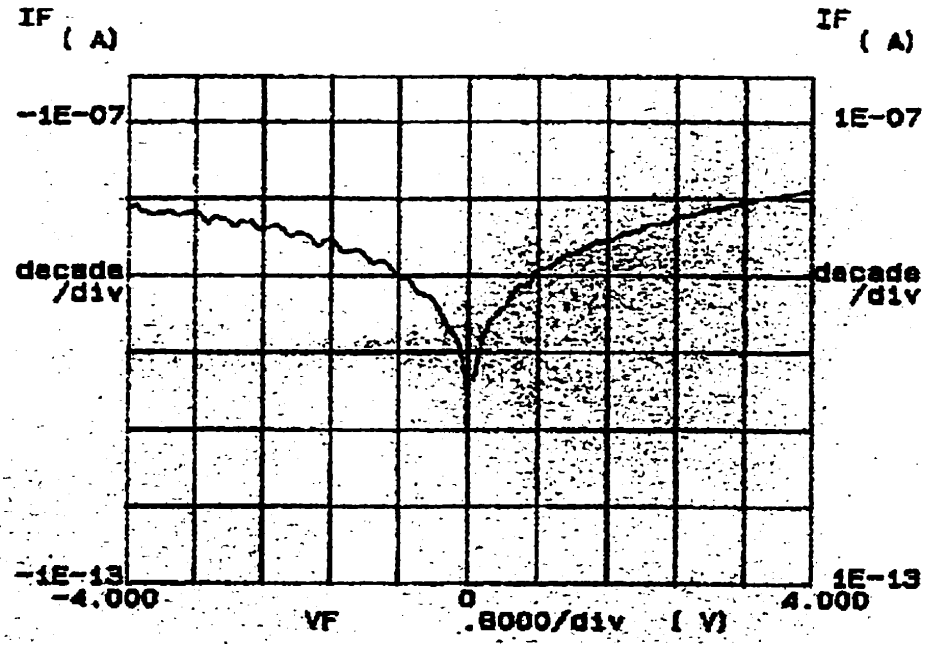
(i) n-type Si 3×10^{19} cm^{-3}



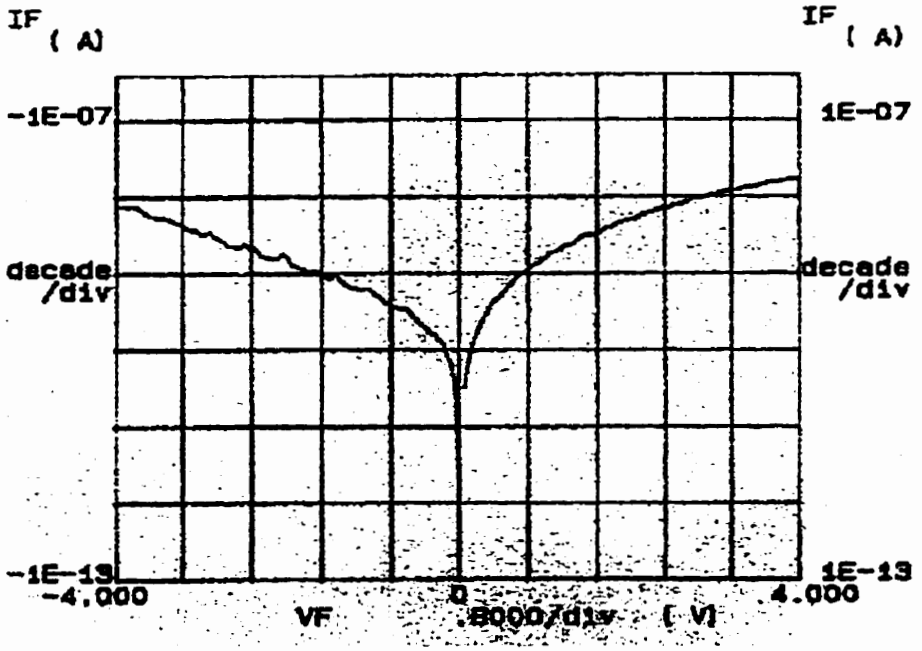
(ii) n-type Si 8×10^{18} cm^{-3}



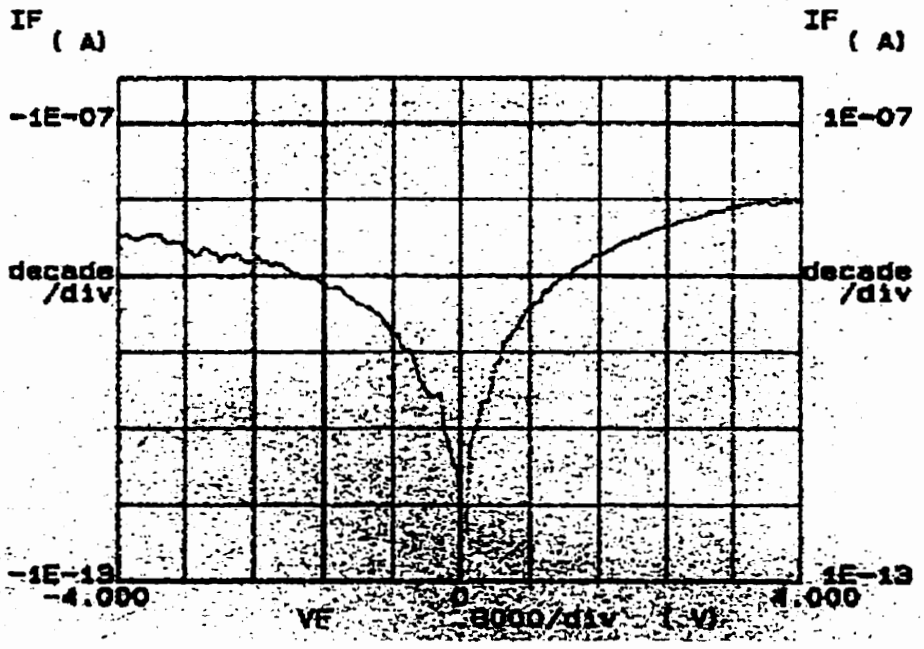
(iii) n-type Si 3×10^{17} cm^{-3}



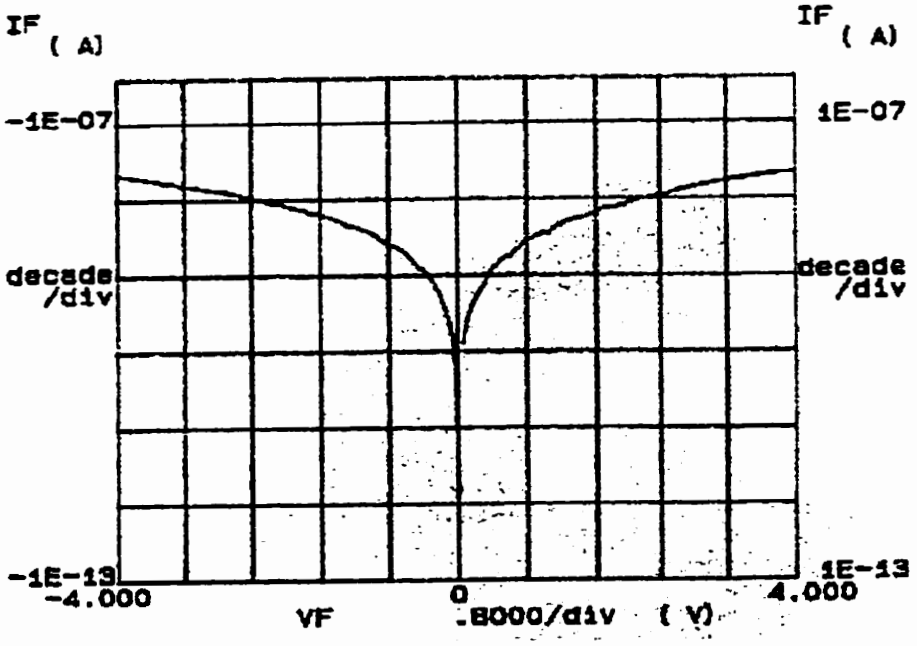
(iv) n-type Si 3×10^{16} cm^{-3}



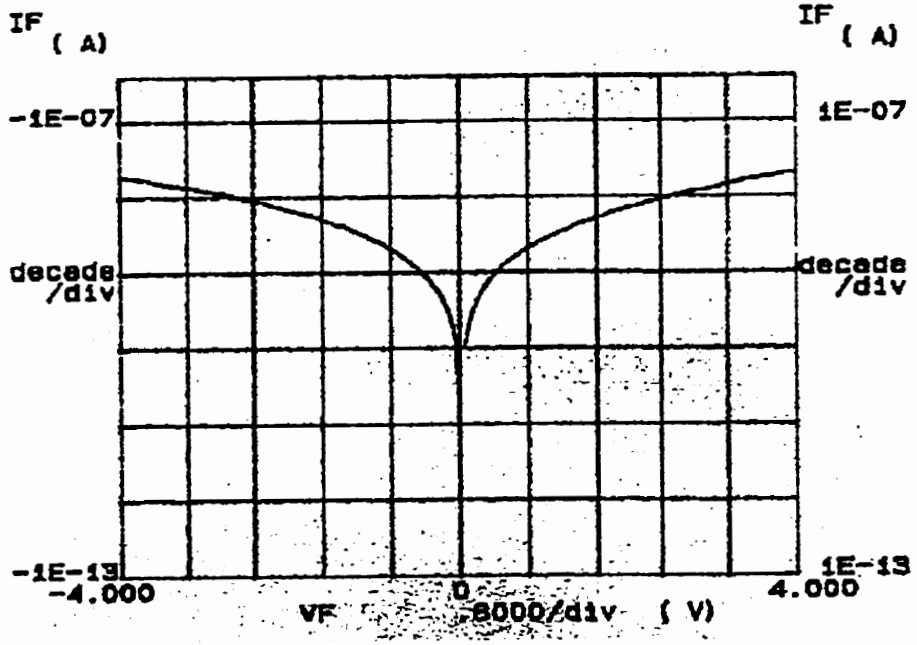
(v) n-type Si 6×10^{15} cm^{-3}



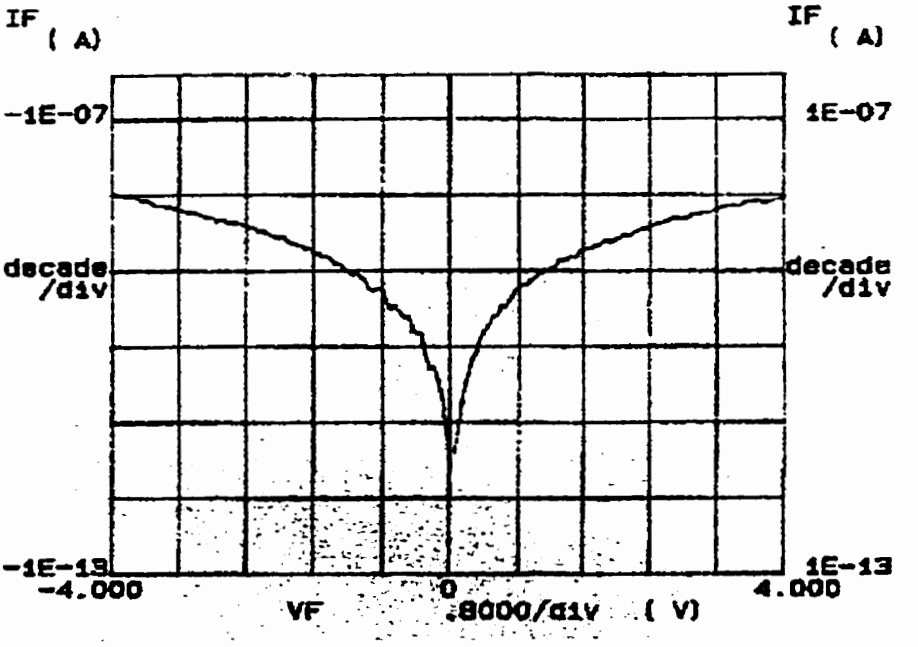
(vi) n-type Si 5×10^{14} cm^{-3}



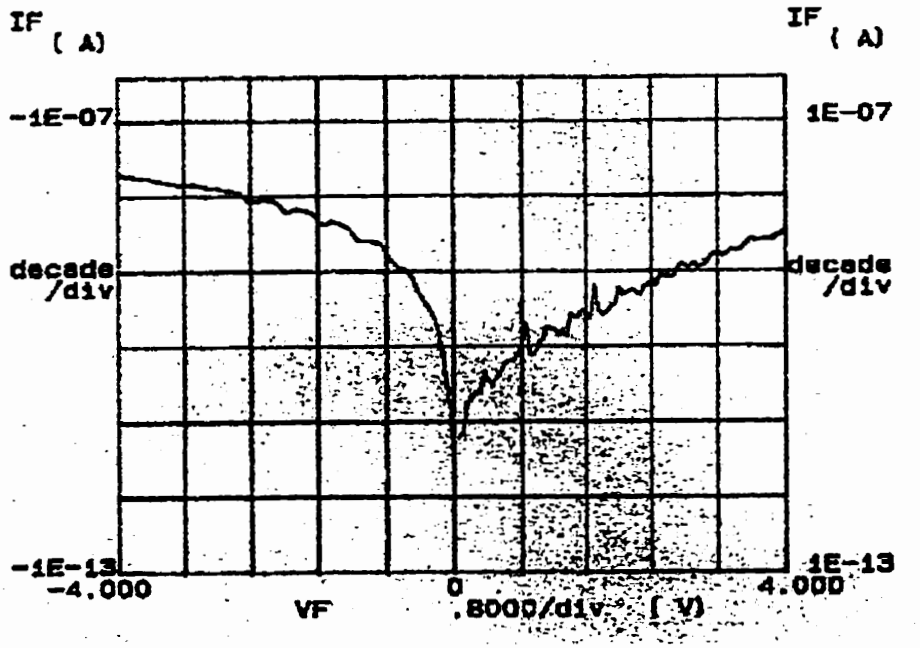
(vii) p-type Si 6×10^{19} cm^{-3}



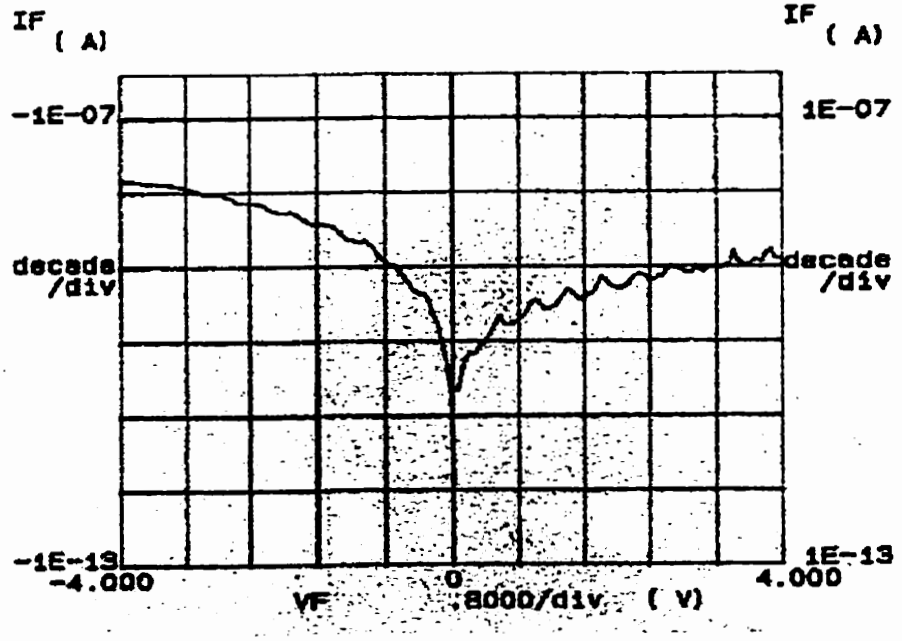
(viii) p-type Si 1.5×10^{19} cm^{-3}



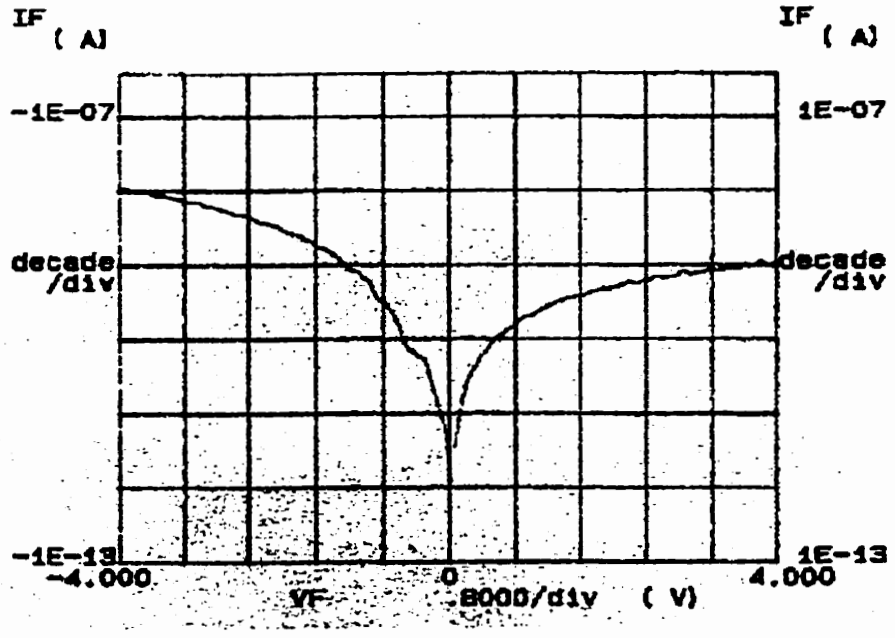
(ix) p-type Si 2×10^{18} cm^{-3}



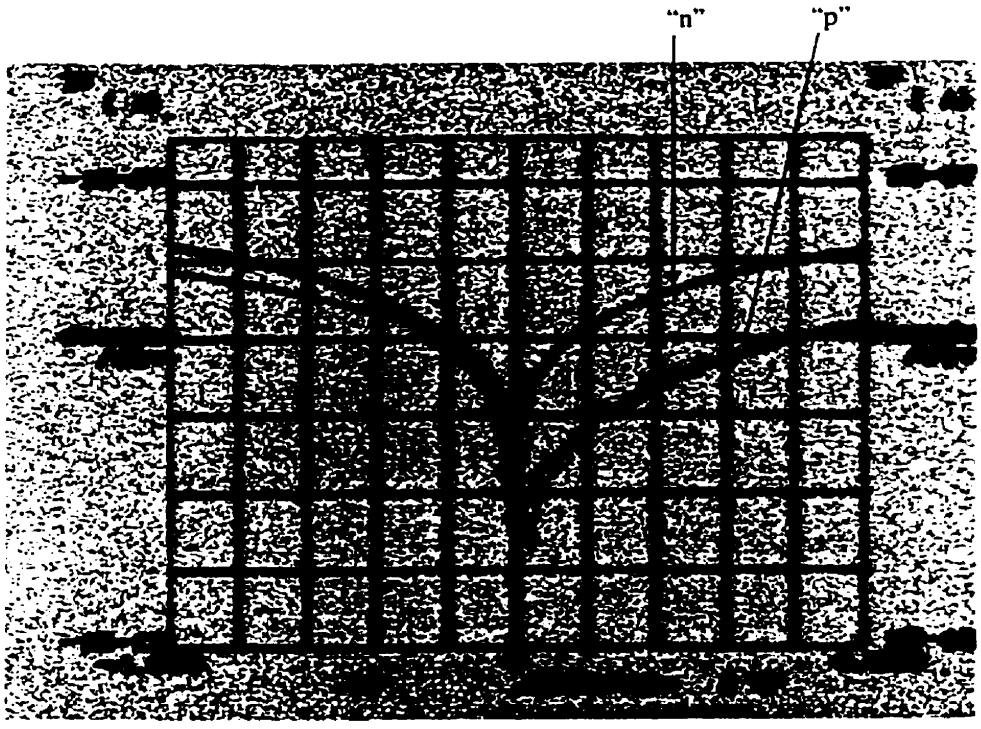
(x) p-type Si 1.2×10^{17} cm^{-3}



(xi) p-type Si 2.5×10^{16} cm^{-3}



(xii) p-type Si 3×10^{15} cm^{-3}



(xiii) "p" p-type Si 1.2×10^{17} cm^{-3}
"n" n-type Si 3×10^{17} cm^{-3}

APPENDIX B

CAPACITANCE DERIVATIVE FOR p-Dia/Si JUNCTION

The space charged region at the tip-Si junction forms a capacitor whose magnitude is magnitude is of the order of 1 fF. Such capacitances cannot be measured directly with a capacitance meter because of the presence of stray capacitance of the same order of magnitude. However, the capacitance derivative can be measured at a much higher frequency (10 Khz) to eliminate low frequency stray capacitance.

Similar to p-n homojunctions, energy band bending occurs at the interface of a heterojunction as a result of carrier diffusion across for the system to reach equilibrium. A space charged region, and therefore a depletion capacitance is formed at the interface. Solutions of Poisson's equation for the step junction on either side of the interface can be used to obtain the depletion width [41]. The depletion width is given by

$$W_d = x_1 + x_2$$

$$= \left[\frac{2\varepsilon_1\varepsilon_2(V_{bi} - V)(N_A + N_D)^2}{q(\varepsilon_1 N_D + \varepsilon_2 N_A)N_D N_A} \right]^{1/2} \qquad \text{(B-1)}$$

where ε_1 and ε_2 are the relative dielectric material of the two semiconductors, V_{bi} is the built in potential, V is externally applied voltage, and N_A and N_D are the donor and acceptor dopant densities respectively. A generalization of the result for homojunctions gives the transition capacitance

$$C = \left[\frac{q\varepsilon_1\varepsilon_2 N_A N_D}{2(V_{bi} - V)(\varepsilon_2 N_A + \varepsilon_1 N_D)} \right]^{1/2} \qquad \text{(B-2)}$$

and the differential capacitance is given by

$$\partial C/\partial V = \left[\frac{q\varepsilon_1\varepsilon_2 N_A N_D}{8(V_{bi}-V)^3(\varepsilon_2 N_A + \varepsilon_1 N_D)}\right]^{1/2} \quad \text{(B-3)}$$

The differential capacitance is proportional to the relative doping concentration of both tip and substrate. This means that by measuring $\partial C/\partial V$ as a function of the substrate doping concentration for both N and P-type one can get a further insight regarding the junction barrier. Specifically, this measurement would give more information about the side in which the depletion width is larger for N and P type substrates. So far, I-V measurements suggest that for P-type substrates, the depletion layer is mainly on the substrate side whereas for N-type the depletion is predominantly on the diamond side.

The capacitance derivative was measured using the technique described in chapter 1 for performing Schottky contact capacitance profiling. In this case, the contact is a heterojunction. The sample preparation procedure followed prior to measuring I-V characteristics was adopted here. The purpose being that the distribution of surface states must be similar to that of SRM research sample surfaces as well as removal of any interfacial layers such as native oxide. I-V curves were measured again within a few minutes after the capacitance derivative measurements. The latter was measured at least five different locations on a sample surface and the average was calculated. The contact force was regulated at 1μN. The same procedure as before was followed to measure corresponding I-V spectra. It was physically not possible to ensure that I-V measurements were performed at the same spots as $\partial C/\partial V$, because the tip had to be lifted before I-V measurement instruments were setup. The analysis procedure was the same as before (Fig. 3.12).

Figure B-1 below shows a graphical representation of variation of the capacitance derivative with substrate doping concentration.

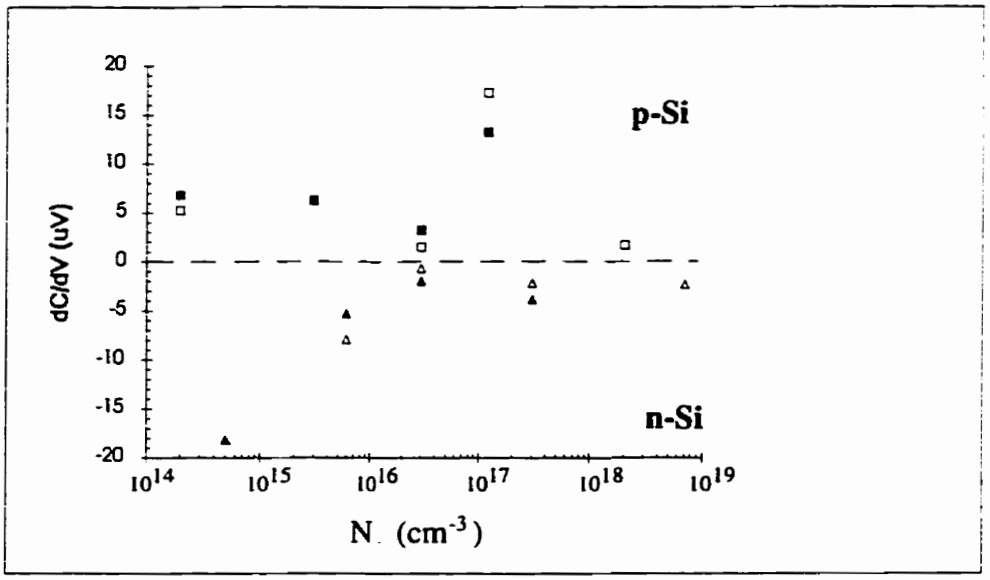


Figure B-1 $\partial C/\partial V$ Vs substrate doping concentration for the calibration samples.

Three characteristics of the capacitance derivative can be observed on Fig.B-1: Firstly, $\partial C/\partial V$ for P-type substrates is consistently positive while that for N-type substrates is negative. Secondly, above doping level of 10^{16} cm^{-3} $\partial C/\partial V$ values increases with doping except at very high doping level (10^{19} cm^{-3}) where $\partial C/\partial V$ becomes smaller. For N-type at this high doping level, $\partial C/\partial V$ value was fluctuating from 0.5 to 3.8 μV. However, below 10^{16} cm^{-3} doping level $\partial C/\partial V$ is observed to increase again for both N and P-type substrates. This feature posses some difficulty explaining using basic theory of well-behaved heterojunction. Thirdly, for each doping level, $\partial C/\partial V$ values for P-type are consistently higher that those for N-type substrates except at the two extremes (very high and low doping levels). Furthermore, a considerably steeper increase

in the $\partial C/\partial V$ values for P-type compared to N-type is observed here. This is consistent with I-V data summarized in Fig. 3.12 (a) and (b). The reason for $\partial C/\partial V$ to suddenly increase at low doping levels is not very well understood. It may be that the back contact to the substrate for lowly doped substrates is not as easy to make into an ohmic contact as it is for higher level doped substrates. This would mean that the back contact is a rectifying metal-semiconductor contact with a larger contact area and therefore the resulting $\partial C/\partial V$ is higher and dominant over that at the tip-surface heterojunction. However, $\partial C/\partial V$ has been observed to reduce drastically for more heavily doped substrates in metal-semiconductor contacts using this technique[30]. The reason is that at high doping levels the depletion width becomes very small so that the change in capacitance when $\partial C/\partial V$ is measured is much smaller and sometimes collapses under forward bias. When the junction is forward biased, the tip is essentially short-circuited to ground and the Q-value for the capacitance sensor resonant curve reduces dramatically.

From the analysis of capacitance derivative data it can be concluded that for the diamond-silicon heterojunction, a relatively larger depletion is present in the P-type substrate compared to that on a N-type substrate when the same diamond tip is placed on these surfaces for dopant density larger than 10^{16} cm^{-3}. For doping concentration change from 10^{16} cm^{-3} to 10^{17} cm^{-3} an order of magnitude change in $\partial C/\partial V$ is observed when the tip is on P-type surface while a factor of two increase is observed when the surface is N-type. The level of sensitivity of $\partial C/\partial V$ to doping density variation on a P-type compared to that obtained on a corresponding change in doping concentration on a N-type substrate does suggest that not much depletion is present in the N-type silicon. The trend followed by the capacitance derivative is not consistent with theoretical predictions. Therefore the results are not conclusive in this regard.

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IMAGE EVALUATION
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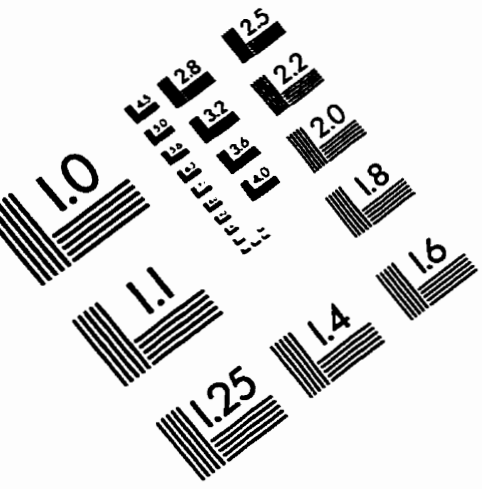

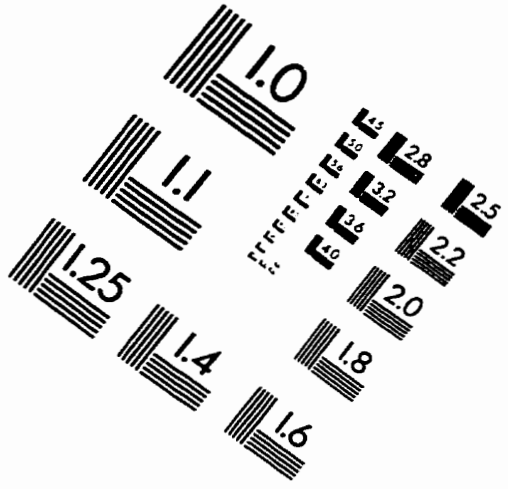

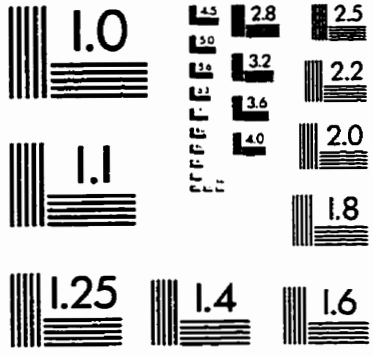

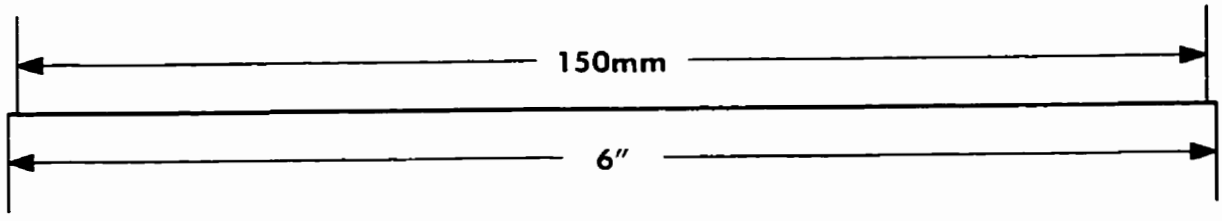

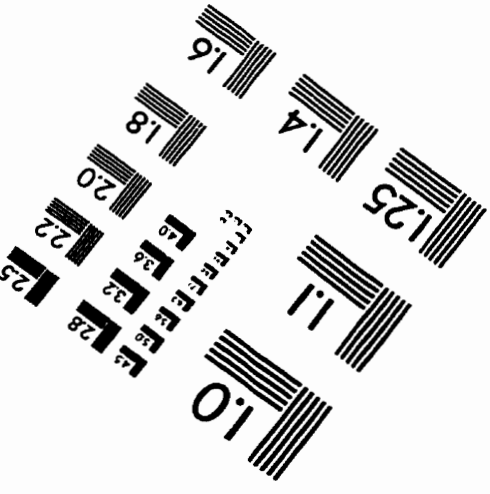

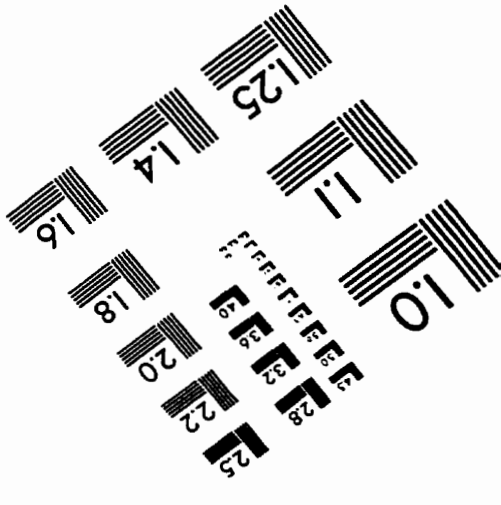

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