RESEARCH ON STABILITY ISSUES OF A GRID-CONNECTED PV INVERTER IN POWER HARDWARE IN THE LOOP (PHIL) ARCHITECTURE

by

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Abstract

This thesis presents an in-detail stability analysis of a Power Hardware in the Loop (PHIL) network formed through an Ideal Transformer Method (ITM) interface. The ever-growing demand of PHIL testing necessitates a thorough research in the area. The ITM interface devices are crucial in determining the accurate and stable PHIL. Therefore, this thesis considers the parameters of these individual devices to develop analytical equations with which the stability can be determined quantitatively. This helps in choosing the interface devices as well as the system parameters before forming the PHIL setup. The PHIL testing is something that requires an experimental result to validate its operation besides the theoretical and mathematical formulations. The work in this thesis follows the methodology of mathematical analysis followed by experimental results.

The PHIL setup used in this thesis for its analysis considers a simple resistor divider network to formulate its hypothesis and finally extends the study to evaluate a Grid Connected PV Inverter (GCPI) in a PHIL architecture. The delay present in the PHIL network as a result of non-ideal interface devices creates a major discrepancy between the results in the actual system with the PHIL system. In order to eliminate the effect of this delay, this thesis considers an application of a Smith Predictor (SP) compensator. This SP compensator consists of a model of the interface and the estimation of the delay in the PHIL network of choice. This thesis

works towards developing the model of the interface device in the ITM interface. To validate the model, an experimental gain and phase measurements are made and compared with the gain and phase of the model. This ensures that an accurate model of the interface is obtained to model the SP compensator. Also, the round-trip delay of the PHIL network under study is estimated through various combinations of I/O devices. Once the SP compensator model is developed, it is implemented in Real Time Digital Simulator (RTDS) to verify the stability predictions made from the theory. The SP employed PHIL network with resistor divider and a GCPI is used as an actual hardware for the experimental validations.

Besides the stability analysis of a PHIL network, this thesis also presents a fundamental work that could benefit the dynamic response of a switched-mode amplifier. The switched-mode amplifier with a conventional linear controller would have a bandwidth limited by the converter parameters. This thesis explores the area of non-linear control by implementing a Second Order Switching Surface (SSS) based Boundary Controller (BC) to a Full Bridge (FB) Voltage Source Inverter (VSI) operating with unipolar switching. The experiments are performed in a 550 VA, VSI prototype which showed a transient response in the range or 150-320 μs. This can easily be extended to push the dynamic response of such setup with use of advanced digital control card complemented by a higher switching semiconductor device.

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I would like to confirm the approval from all the authors and hereby acknowledge the use of following publications during the preparation of this thesis. Only the contents of the publications where I am the first author are included in this thesis.

Publications in IEEE Journal

- **M. Pokharel**, and C. N. M. Ho, "Development of Interface Model and Design of Compensator to Overcome Delay Response in a PHIL Setup for Evaluating a Grid-Connected Power Electronic DUT," IEEE Transactions on Power Electronics (Submitted).
- ©2020 IEEE. Reprinted, with permission, from **M. Pokharel**, and C. N. M. Ho, "Stability Analysis of Power Hardware in the Loop (PHIL) Architecture with Solar Inverter," IEEE Transactions on Industrial Electronics (Early Access), 2020.
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Publications in IEEE Conference

- ©2020 IEEE. Reprinted, with permission, from **M. Pokharel**, and C. N. M. Ho, "Modelling and Experimental Evaluation of Ideal Transformer Algorithm Interface for Power Hardware in the Loop Architecture," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, pp. 1404-1410, March 2020.
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Dedication

To my dear parents, my beloved wife and my supportive sister!

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Nomenclature

List of Symbols

i_{pv}	Photovoltaic current
v_{pv}	Photovoltaic voltage
I_{mpp}	Current at maximum power point of a photovoltaic source
V_{mpp}	Voltage at maximum power point of a photovoltaic source
R_{mpp}	Resistance at maximum power point of a photovoltaic source
I_o	Saturation current of a photovoltaic source
V_t	Thermal voltage of a photovoltaic array
N_s	Number of cells in series of a photovoltaic array
R_S	Equivalent series resistance in a single diode model
R_p	Equivalent parallel resistance in a single diode model
a	Diode ideality constant
L	Inductance of a converter
C	Capacitance of a converter
R	Load resistance of a converter
r_L	Parasitic resistance of an inductor
r_C	Parasitic resistance of a capacitor

v_{dc}	DC link voltage representing the DC bus
v_C	Voltage across a capacitor
i_L	Current through an inductor
i_{LB}	Boundary current between CCM and DCM mode
f_{sw}	Switching frequency of a converter
D	Duty cycle of a converter
V_s	Input voltage at the software end
R_s	Resistance at the software end
R_h	Resistance at the hardware end
R_C	Resistance in parallel to a current source
K_1	Software gain
K_2, A	Amplifier gain
T_2	Amplifier input output delay
T_a, T_{amp}	Amplifier bandwidth
T_f, T_{aaf}	Anti-aliasing filter cut-off
T_s, T_d	Time step delay
T_{lpf}	Low pass filter cut-off of an analogue input card
T_{comp}	Time constant of a compensator
G_{aaf}	Gain of an anti-aliasing filter
v_{ref}	Reference voltage to a controller
D	Hysteresis voltage band

List of Abbreviations

PHIL	Power Hardware in the Loop
PE	Power Electronic
PV	Photovoltaic
FC	Fuel Cell
DUT	Device Under Test
CHIL	Controller Hardware in the Loop
PCS	Power Conversion Stage
RTS	Real Time Simulator
AI	Analogue Input
AO	Analogue Output
GCPI	Grid Connected Photovoltaic Inverter
RTDS	Real Time Digital Simulator
INC	Incremental Conductance
MPPT	Maximum Power Point Tracking
ITM	Ideal Transformer Method
SP	Smith Predictor
VSI	Voltage Source Inverter
HIL	Hardware in the Loop
ABS	Automatic Braking System
TCS	Traction Control System
V2G	Vehicle to Grid
DSP	Digital Signal Processors

IA	Interface Algorithms
PCD	Partial Circuit Duplication
DIM	Damping Impedance Method
DAC	Digital to Analogue Converter
ADC	Analogue to Digital Converter
PA	Power Amplifier
TF	Transfer Function
PD	Padé Approximations
PCC	Point of Common Coupling
GPA	Gain Phase Analyzer
MPP	Maximum Power Point
PI	Proportional Integral
SD	Single Diode
CCM	Continuous Conduction Mode
PWM	Pulse Width Modulator
CC	Constant Current
CV	Constant Voltage
DCM	Discontinuous Conduction Mode
GTAO	Giga-Transceiver Analogue Output
GTDI	Giga-Transceiver Digital Input
ISR	Interrupt Service Routine
AQ	Action Qualifier
RH	Routh-Hurwitz

SE	Simulation Environment
ISE	Integral Square Error
LHS	Left Hand Side
SCR	Short Circuit Ratio
WG	Weak Grid
SG	Strong Grid
PLL	Phase Locked Loop
GTAI	Giga-Transceiver Analogue Input
AAF	Antialiasing Filter
ZOH	Zero Order Hold
FB	Full Bridge
BC	Boundary Controller
SSS	Second order Switching Surface
BSS	Bipolar Switching Scheme
USS	Unipolar Switching Scheme
FSM	Finite State Machine
PR	Proportional Resonant
THD	Total Harmonic Distortion
FPGA	Field Programmable Gate Arrays

Chapter 1

Introduction

1.1. Background

The technology of Power Hardware in the Loop (PHIL) is gaining interest in the recent years in industries as well as in academic research settings. The PHIL arrangement offers a variety of advantages in terms of flexibility, space requirement and time. This semi-physical simulation setup can emulate an actual-like environment to evaluate real power apparatuses. This type of testing platform provides a great degree of freedom while evaluating Power Electronic (PE) converters with renewable energy sources, such as solar or wind energy. One of the applications is, testing a Photovoltaic (PV) inverter connected to the grid under changing environmental conditions and performing various other grid interaction studies. This is just one application and PHIL platforms have been widely adopted to evaluate systems with real energy sources and energy storage elements to study the interactions between them [1], [2].

In industries, PHIL-based burn-in systems are used to evaluate the efficiency and stability of a power converter instead of using a real resistive load to dissipate the power supplied by the converter. Typically, these burn-in tests last for a couple of minutes to even several years. The PHIL-based approach can minimize the energy wasted in these tests by

power cycling the energy to air-conditioning systems needed to cool the testing setup. In order to enhance power process efficiency and enable full manual control of element characteristics, full power electronics PHIL platforms have been proposed. These platforms are common to use a PE based emulators instead of real energy sources and storage elements. One example is a Fuel Cell (FC) energy source. This requires a PE converter and a controller to emulate the electrical behaviors of the FC to have reactions with the connecting system [3], [4]. This benefits in significantly reducing the size of testing platform as well as providing a relatively safe testing environment. For the PHIL applications described above, it is a common practice to usually evaluate a single element, e.g. FC, single Device-Under-Test (DUT), or electronic ballasts, in the power loop.

1.2. Motivation

PHIL may be described as a system consisting of a real-time software model interacting with a physical device through an interface for exchange of power between them. With this feature, PHIL stands out among real-time simulations for running a wide variety of tests ranging from evaluating power converters, performing various grid interaction studies, integration of renewables in microgrid to various source emulation applications. Unlike the existing real-time simulation where the entire system with controllers and power-networks are simulated in real-time, PHIL is an extension to these real-time simulations and existing Controller-Hardware-in-the-Loop (CHIL) simulations.

The increasing trend towards renewable based energy sources demand more system level investigations. The impact of integrating these sources at different power coupling point becomes important for system engineer to ensure stability as well as to aid in system planning.

Microgrids that integrate renewable energy sources are new approach for overcoming high operating costs for delivering power to remote communities and providing improved energy efficiency of electrical networks in modern buildings [5], [6]. However, most of research in this topic is at the computer simulation level or individually testing of a power apparatus in microgrid. These studies entail a wide technology gap between the reported research results and the realities of practical performance [7]-[9]. In order to achieve results more accurate to the practical system, it has been proposed to use a PHIL platform to evaluate microgrids with actual power flowing into the electrical networks and devices [10]-[16].

It is therefore not wrong to foresee the applications of PHIL in testing and evaluating renewable sourced devices growing. Also, when it comes to renewable based sources, it is imperative to use PE converters as the Power Conversion Stage (PCS) before the power can be delivered to the grid or in any other usable form. This is another high-potential application area of PHIL where a non-linear PE converter is involved. The use of these real PE hardware in testing is due to the complexities in accurately modelling all the non-linear dynamics of PE devices. The PHIL testing would particularly flourish in such environments as there is no more reliance on computer models rather an actual PE hardware.

1.3. Statement of the Problem

The PHIL forms an attractive way for testing various linear devices as well as non-linear PE converters in laboratory scale and yet get a result that resembles an actual like scenario. This approach, however promising, suffers from various stability problems arising due to the interface between the hardware and software environment required to create a PHIL. The PHIL architecture comprises of a power apparatus (source or load) as a part of the system interfaced

with a Real Time Simulator (RTS) accompanying remainder of the sub-system. The intermediary medium to create the interaction between these two sub-systems are vital in achieving an actual like response.

The interface medium in PHIL basically consists of devices like, amplifier, Analogue Input (AI) card, Analogue Output (AO) card and sensor. This interface, therefore, naturally consists of an unavoidable delay from the fiber cables, input /output (I/O) cards, sensors, conditioning circuits, filters and amplifiers. While, ideally, it is desirable to have an infinite bandwidth interface with no delays but practically this cannot be achieved as the conversion time within the I/O cards, computation time required by the RTS and the response of the amplifier contributes to this delay and bandwidth restrictions. With this, it is therefore required that a comprehensive analysis of the stability of a PHIL system be performed. Also, from the standpoint of system performance, these interface devices in PHIL play a significant role in quantifying the stability as well as the accuracy. Moreover, the stability problems of PHIL have been intriguing to many researchers and the challenge remains to completely demystify the stability issues. The solution to this would demand a trade-off between robustness and accuracy.

To unravel the problem; the first major concern is the time delay of the loop and its effect on stability and the second challenge is to obtain an actual-like results with acceptable errors. As to consider the issue independently, the improvement areas are;

- Changing the amplifier platform from linear to PE based (also termed as switched-mode amplifier). This allows performing PHIL test for high power applications as the size and cost of PE amplifiers reduces significantly with increasing power level compared to

linear amplifiers. However, the limitation of PE based power amplifier in terms of achieving a fast-dynamic response for PHIL application should first be addressed.

- The I/O cards require a considerable amount of time to perform analogue to digital conversion and digital to analogue conversion. The solution to this is more restricted towards the RTS manufacturer rather than on the user end.
- To deal with the stability problems in algorithm level. This requires the need for detailed investigation of the interface and accordingly design compensators that can eliminate the instability due to delays as well as improve accuracies.

1.4. Thesis Statement

While the application of PHIL for evaluating power electronic DUTs is gaining popularity, the stability concerns associated with the delay in the interface is lacking a thorough investigation. The studies currently present cannot provide answers to all the factors affecting instability and therefore requires an in-depth study. The effect of delay in the closed loop response of PHIL can be eliminated by integrating a Smith Predictor compensator with the PHIL loop which consequently aids in stability as well.

1.5. Thesis Objectives and Research Contributions

The objective of this thesis is to investigate the stability issues in PHIL and develop a mathematical and analytical framework along with future recommendations for interface amplifier. Since PHIL is an application-oriented architecture, all the theoretical formulations and analysis in this thesis are verified experimentally. A Grid-Connected PV Inverter (GCPI)

is chosen as the non-linear power electronic DUT to demonstrate the operation of a stable PHIL. The arrangement of GCPI in a PHIL is shown in Figure 1.1. The outcomes from this work can directly benefit any industrial / academic research or test application in the field of PHIL.

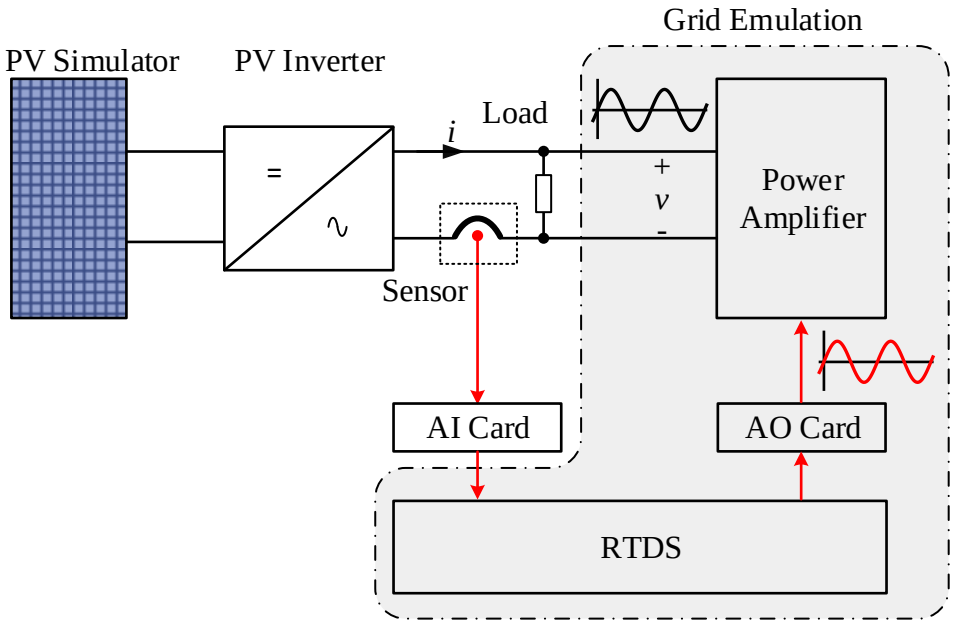


Figure 1.1 A PHIL test setup for a grid-connected PV inverter.

To explicitly detail the research objective, each component in Figure 1.1 needs to be studied individually to understand the research questions and the analysis follows accordingly. The main contribution and research objectives of this work is divided into following themes;

- To familiarize with the RTS device (Real Time Digital Simulator (RTDS)) and its interface: - a CHIL approach is used to study the performance of a PV module with its corresponding controllers. This includes the development of small-signal model of PV module and Incremental Conductance (INC) based Maximum Power Point Tracking

(MPPT) algorithm. The developed mathematical model is verified with experimental results obtained from RTDS by the means of frequency response plots. The contribution of this work includes the comprehensive model development and experimental verification with CHIL approach.

- Stability evaluation of PHIL loop: - This study includes the development of a set of mathematical inequalities that defines the boundary of stability in a PHIL, considering the existing model of interface. The contribution in this work is quantifying the stability criteria in terms of interface device parameters, DUT and delay time.
- PHIL interface device characterization and interface model development: - The characterization includes development of each interface device model and experimentally verifying it using frequency response approach. The potential research contribution in this work is the experimental validation of developed model which has not been reported in existing literatures.
- Designing a compensator to overcome delay response in a PHIL: - this work includes designing a compensation block which eliminates the effect of time delay in the closed response to achieve a robust PHIL operation. The contribution from this work is the application of Smith Predictor compensator in a PHIL setup.
- Design, implementation and demonstration of an interface switched-mode amplifier: - The interface amplifier which is a critical component of a PHIL architecture needs to be designed to have a fast-dynamic response, especially for a switched-mode amplifier which is an obvious choice for applications requiring high power testing. This work includes the application of boundary controller to design and experimentally verify a fast-dynamic switched-mode power amplifier even while operating at low switching

frequency. This work could contribute in establishing a benchmark for future PE amplifier for PHIL applications.

1.6. Thesis Organization

The content of this thesis comprises of material published/under-review in IEEE conferences and journals organized to form majority of the chapters within this thesis. In total, this thesis contains seven chapters structured in following ways;

Chapter 1 introduced various applications of PHIL in industries as well as in academic research environment along with the motivation behind this work. The problems with PHIL setup are also discussed in great lengths along with research objectives to address few of these problems.

Chapter 2 reviews the integral components comprising the PHIL architecture. This includes, interface algorithms, amplifiers, delay models, delay compensation methods and a brief section of existing studies in PHIL. Also, existing literatures on a PV source connected to the grid is summarized in the same chapter.

Chapter 3 presents the development of a linear model of PV along with its related controller. The CHIL approach is applied to verify the developed model. The details on small-signal modelling and experimental validations are also discussed in this chapter.

Chapter 4 works to develop a mathematical framework to describe the stability of a PHIL loop. The evaluation of a PV inverter in a stable PHIL loop is also demonstrated in this chapter with adequate experimental results.

Chapter 5 presents the characterization of the Ideal Transformer Method (ITM) interface in a PHIL and develops the individual model of interface devices. The experimental validation

of the model also forms the part of Chapter 5. Additionally, Chapter 5 discusses the design methodology of a Smith Predictor (SP) compensator followed by the application of SP compensator in PHIL along with the experimental results which also makes the content of this chapter.

Chapter 6 includes the design and implementation of a single-phase Voltage Source Inverter (VSI) with a second order switching surface-based controller. This VSI forms the basis of a switched-mode amplifier in a PHIL. This chapter shows the experimental validations of the VSI-based switched amplifier at various operating conditions.

Chapter 7 concludes this thesis by discussing briefly the research objectives achieved and presenting the possibility of extending this research work.

Finally, the references followed during the course of this research is listed with numbers representing the cross-referencing location pointing the corresponding text in this thesis.

Chapter 2

Literature Review on Components of a PHIL

2.1. A Brief History

The history of Hardware-in-the-Loop (HIL) simulations dates back to as early as 1930s, where it was used in the aircraft industry for flight simulators [17]. Over the years, with the growing computational power of the microprocessors the real-time simulations opened its way. With this, the application of HIL simulations progressed rapidly. The major application included testing missile guiding system by NASA [18]. Later, the automobile industry adopted the HIL simulations to design Automatic Braking System (ABS) and Traction Control System (TCS) to name a few [17]. The electric power and robotic sector also could not remain untouched by it [18]. A brief description of various applications and extensions of HIL in electric power research areas and industries are discussed in [19]. This include, CHIL for designing and testing a control hardware (including the controller) without the need to operate an actual power stage hardware (simulated in real-time), PHIL for testing the part of real hardware along with its controller in actual simulated environment, and other variants being PHIL with thermal HIL for designing an air conditioning system for buildings.

Recently with the increasing penetration of renewable sources in the grid, the PCS with non-linear PE converter poses a new challenge for this integration. This requires a thorough analysis of the renewable hardware in an actual-like setting to be able to test the engineering elements as well as to foresee the risks involved during implementations. This has been one of the major areas where PHIL applications have been mainly applied, typically, in micro-grids with distributed generations. Besides, the upward trend in electric vehicle market also demands a detailed investigation in the technologies like Vehicle to Grid (V2G) where the energy stored in the batteries are utilized by the grid in smoothing the load profile during peak periods [20]. The evaluation of V2G technology with PHIL is also an active research area [21]-[23]. From this, it can only be predicted the evolution of HIL in every aspect starting from engineering design to ensuring the system operation in a projected manner.

Given the flexibility and demand of PHIL testing in industry and academia, it is important to understand the existing state-of-the-art in the field. The subsequent sections present a brief overview of the key elements that forms a PHIL study platform.

2.2. Real Time Simulators

Real-time simulations have been in use for many years now. Down the time, many different types of RTS have been developed. One of the pioneers in the field of simulator development include RTDS Technologies Inc, who started their commercial RTS in 1991 with Digital Signal Processors (DSP). Following this, by 1996 other companies like Électricité de France, SIEMENS and OPAL-RT developed their simulators too [24]. Currently, the number of RTS are growing, notable mentions being; RTDS, OPAL-RT, dSPACE, Typhoon and RTBOX. These RTS are grouped under variety of functionality, hardware architecture,

modelling and solution algorithm to name a few. The detailed comparison of various RTS including the characteristics of hardware and software is presented in [24]. Further, Lauss et al. [25] presents the potential applications of currently existing digital RTS for PHIL studies. It is important to quantify the time-step whenever real-time simulation is discussed. It has been suggested that "50µs" would provide a good enough resolution to study the transients of a 50/60 Hz power system network [24], [25]. However, when it comes to studying high frequency PEs devices the time step must be lowered considerably [24], [25]. Also, multi-rate simulation is a feasible alternative to represent interfacing of PE devices with 50/60 Hz power system network. With the development of such high computational capability RTS, the simulation studies have been revolutionized. The conventional non-real-time simulation are easily replaceable to perform real-time simulation studies and can also be extended to perform CHIL and PHIL simulations.

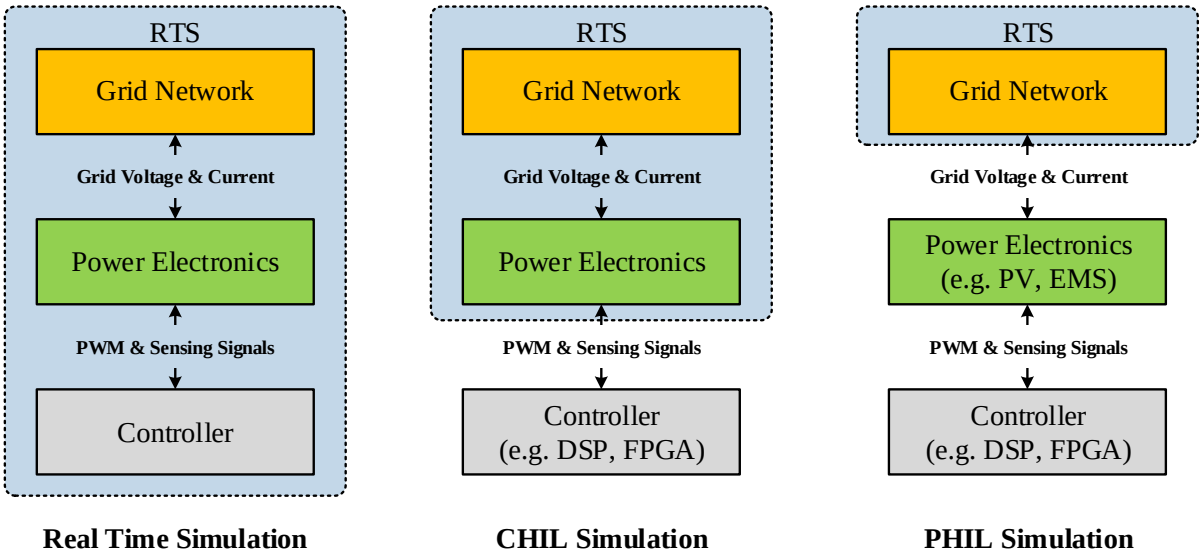


Figure 2.1 A comparison of various simulation platforms.

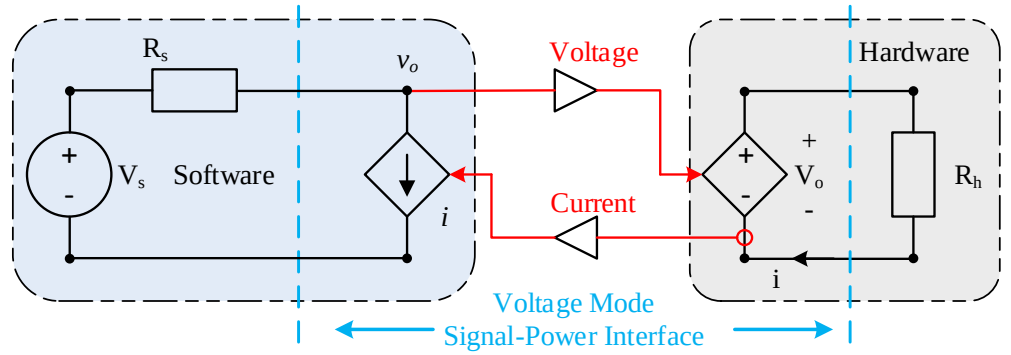
The functional difference between three simulation platforms for the case of PE converter exchanging power with the grid is shown in Figure 2.1. As mentioned in Faruque et al. [24], CHIL simulation consists of a physical controller generating switching signals for controlling PE converter simulated inside the RTS. The entire system including the controller is run in RTS for a real-time simulation of the similar system. Moreover, if a part of power exchange point is decoupled between RTS and physical hardware (Grid and PE Converter in Figure 2.1.) to have a virtual exchange of power, such type of simulation technique has been termed as PHIL by the literatures [24]-[27]. To achieve virtual power exchange between RTS and physical system, design of proper interface is imperative.

2.3. Interface Algorithms

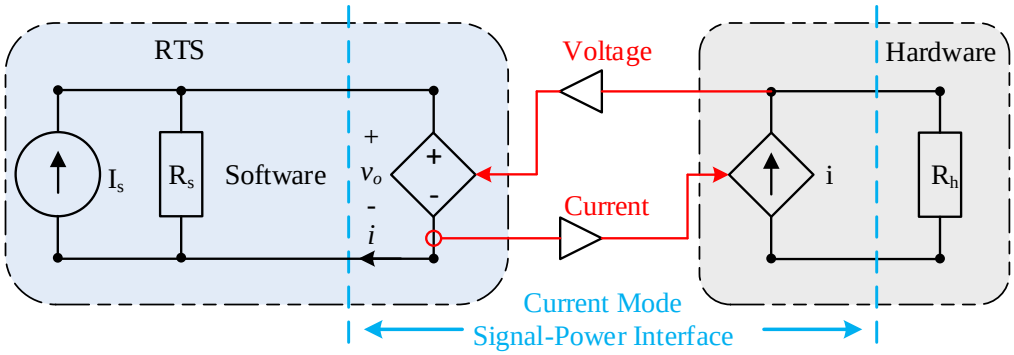
The interface in PHIL is the one that differentiates it from its actual counterpart. Therefore, the arrangement of devices in interface for exchange of power affects the performance of the PHIL-based system. Based on applications and performance requirements, interface devices can be arranged to create a PHIL. These arrangements of devices to form interface is termed what is called an Interface Algorithms (IA). There are several IA proposed in the literatures based on their performance parameters like, implementation ease, stability margin and accuracy [26], [28], [29].

It is well reported that IA like Ideal Transformer Method (ITM) offers advantages in ease of implementation and accuracy but often suffers from stability problems [26], [29]. Another IA called Partial Circuit Duplication (PCD) that requires a linking impedance duplicated in software and hardware has an improved stability than ITM but at the expense of lower accuracy [25], [26], [29], [30]. Besides, this inclusion of hardware impedance is not desirable for high

power applications. The IA which offers considerable balance between accuracy and stability is Damping Impedance Method (DIM) but the implementation complexities with DIM is relatively higher [25]. DIM is created as a result of combining the advantages of both ITM and PCD. Other notable mentions of IA include time variant first order approximation and transmission line model [26]. These IAs due to their higher limitations in implementations are not widely used for PHIL applications.



(a)



(b)

Figure 2.2 ITM interface (a) Voltage mode (b) Current mode.

The IAs, in general, are classified into two types; voltage and current, based on the type of signal interfaced [25], [30]. Figure 2.2 shows such arrangements of an ITM interface with

voltage mode and current mode signal exchanges. In voltage mode interface, Figure 2.2 (a), voltage from RTS is sent out through output Digital to Analogue Converter (DAC) card in signal level which is then amplified using voltage amplifier before its connected to DUT. The current drawn by DUT is sensed and fed back to RTS through its input Analogue to Digital Converter (ADC) card. With similar arrangement, by sending out the current and feeding back the voltage in the interface, current mode interface shown in Figure 2.2 (b) can be configured. Due to the advantages of ITM, it has become a common method to conduct PHIL studies. Similarly, this research work considers ITM interface for evaluating the stability of PHIL.

2.4. Power Amplifier

Power Amplifier (PA) is one of the crucial devices in the interface of a PHIL architecture. For a real system represented by PHIL, interface devices are mandatory but ideally are expected to have a unity gain with infinite bandwidth. Same applies for PA whose performance characteristics are based on factors like bandwidth, rise time, power level, slew rate and operating regions. Given these parameter dependencies, it is practically not possible to achieve unity gain and infinite bandwidth PA. A comprehensive analysis on the application of three types of PA, viz., switched-mode, generator type and linear amplifier used for PHIL simulations is presented in [31]. Each of these types of PA have their own advantages and applications in a PHIL interface and therefore there is no one clear winner. As described in Lauss et al. [25], Ren et al. [31] and Lehfuss et al. [32], switched-mode PA are flexible in terms of their use as a voltage or current amplifier and are easy to design and implement even for megawatts power range. However, switched-mode PA suffers from a drawback of low bandwidth and slower response time compared to linear amplifiers [25], [31]. Linear amplifiers

are ideal for low power applications, but their size, weight, and cost go up considerably for high power applications [25]. Similarly, generator type amplifier is ideal for system requiring three-phase balanced supplies such as testing a microgrid [13], [25], [31].

2.5. Time Delay

The time delay in PHIL is the result of interface devices cascaded to form the power exchange medium. Additionally, the time-step required to solve a simulation by digital RTS also contributes to this time delay. Ideally, it is desirable to have a system without any delays. Moreover, with the digital RTS running at a certain time-step, even if the interface is designed to have no delays the unavoidable time-step delay is inherently present within. This calls for characterizing the delays in each interface devices before incorporating it in any studies related to PHIL simulation. It also becomes essential to be able to represent the delays with their corresponding mathematical expression to enable better understanding of its effect on system performance.

A time dependent function $f(t)$ with a time delay T_d when exposed to a unit step input can be represented as $f(t - T_d)$. Taking Laplace transform, it can be expressed in frequency domain by $s = j\omega$ where ω represents the angular frequency.

$$f(t - T_d) \xrightarrow{\mathcal{L}} F(s) \cdot e^{-sT_d} \tag{2.1}$$

The exponential function in (2.1) if plotted in frequency domain using bode plot would represent a constant magnitude with infinitely growing phase. This infinite phase lag in time delay results in non-rational Transfer Function (TF) and mathematically be seen as a system with infinite dimension state vector which makes it difficult to control and analyze [33]. In order to avoid such situation, it is a general practice to rationalize the exponential TF of time

delay using Taylor, and Padé approximations (PD) [34], [35]. The comparison of Taylor series with PD for delay is presented in [35]. It is seen that Taylor series has a larger error compared to PD when approximating a pure time delay. Also, Hanta and Prochazka [35] proposes that accuracy of PD increases if the order of numerator is made less than the denominator. The comparison between different degrees of PD have been further presented in [34]. It is seen that, rational approximation of delay using Padé has the highest accuracy when the order of numerator is one less than the denominator.

Rational approximation of time delay using PD results in a polynomial equation in numerator and denominator. If $R_{m,n}(sT_d)$ is the rational approximation of e^{-sT_d} of order (m, n) where m and n are positive integers then PD can be expressed by (2.2) [34];

$$e^{-sT_d} \xrightarrow{Pade} R_{m,n}(sT_d) = \frac{P_m(sT_d)}{Q_n(sT_d)} \tag{2.2}$$

Where,

$$P_m(T_d) = \sum_{k=0}^{m} \frac{(m+n-k)!\,m!}{(m+n)!\,k!\,(m-k)!}(-sT_d)^k$$

and,

$$Q_n(T_d) = \sum_{k=0}^{n} \frac{(m+n-k)!\,n!}{(m+n)!\,k!\,(n-k)!}(-\mathrm{s}T_d)^k$$

With (2.2), delay can be represented by rational function which is more comfortable to handle than the exponential function. However, this approximation remains valid only for a certain frequency range. This is because the phase lag from a rational function is bounded unlike the infinite phase of pure delay and the error in phase increases beyond the frequency band [33].

2.6. Delay Compensation Techniques

The delay in the interface directly affects the performance of the PHIL. Studies have suggested that the stability margin reduces with the increasing delay of the PHIL interface [36], [37]. Similarly, it is also obvious that the accuracy of the PHIL is greatly reduced with the delays [37]. Therefore, it is apparent that the effect of these delays be eliminated or compensated if an accurate and a stable PHIL is desired. One of the feasible solutions to eliminate the effect of delay in PHIL is to compensate for this delay in the result. A compensation method that takes care of the phase delay introduced by the time delay is proposed in [36]. This compensation method used high pass filter to provide the additional phase. Another method to compensate for the effect of time delay is to add a phase advance to the fundamental and harmonic component obtained after Fourier analysis of original signal in RTS [28]. The original signal is then recreated from the phase advanced signal and amplified to take care of time delay in the PHIL loop. However, this method suffers from a lot of limitation like number of harmonics order, time to solve the Fourier by RTS, and power angle of DUT and software node. Another work by Marks, Kong and Birt [37] considers the entire PHIL loop like a classical control block and introduces a pole-zero compensator that deals with any inaccuracies within certain frequency range. This also improves the stability of a PHIL loop; specially for DIM interface.

Time delay compensation has been popular in process control systems where the time delay originates from the sluggish nature of plant. This delay in system to respond to any control actions has led system to run towards instability. This has been a trivial problem for researchers for decades and numerous solutions to overcome the effect of time delay have been proposed. One among many solutions was proposed by Smith [38] which eliminates the delay

effect in the closed loop response by inserting a feedback loop in the original system termed as Smith Predictor (SP) [39], [40]. Another advantage of SP is that it can be incorporated with the system with existing controllers [41], [42]. This makes SP an ideal application for PHIL to eliminate delay in its closed loop response and incorporating compensators as in [37] to improve the stability. However, such application of SP in PHIL has not been reported in the literature so far and therefore makes the study of this research work.

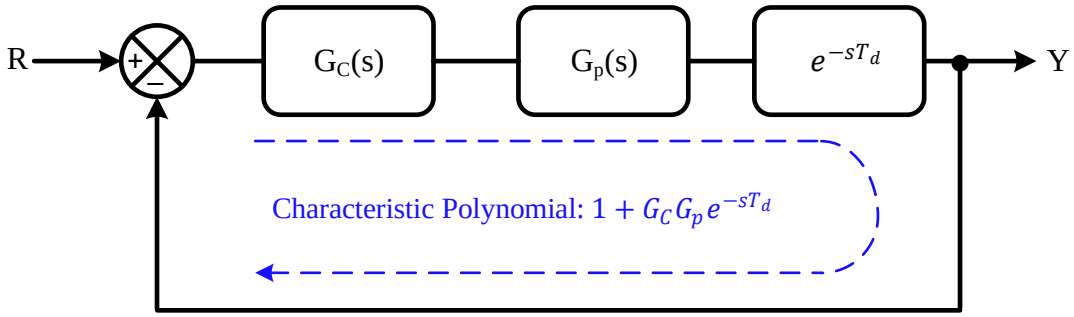


Figure 2.3 Control of a plant with delay.

A standard block representing a delay inherited plant G_p controlled by a controller G_C is shown in Figure 2.3. The closed loop response of such delayed plant with a standard controller would contain the delay term with infinitely growing phase. This makes the system difficult to achieve the set design criteria and controller design becomes extremely difficult. However, if the delay term in the forward path is pushed after the feedback node, the closed loop response of the resulting system would no longer contain the delay term. To achieve this objective, a SP based compensator can be designed.

Following up with the control block in Figure 2.3, the SP employed block with compensator $C(s)$ and the expected equivalent block is presented in Figure 2.4. The input to

output closed loop TF from Figure 2.4 (a) and Figure 2.4 (b) can be derived and equated to obtain the compensator TF $C(s)$.

From Figure 2.4 (a),

$$\frac{Y(s)}{R(s)} = \frac{G_p(s)C(s)^* e^{-sT_d}}{1+G_p(s)C(s)^* e^{-sT_d}} \tag{2.3}$$

Where, $C(s)^*$ is the combined controller and compensator TF. Similarly, from Figure 2.4 (b), the equivalent closed loop response that is expected by employing a SP can be obtained and is given by (2.4).

$$\frac{Y(s)}{R(s)} = \frac{G_p(s)G_c(s)}{1+G_p(s)G_c(s)} e^{-sT_d} \tag{2.4}$$

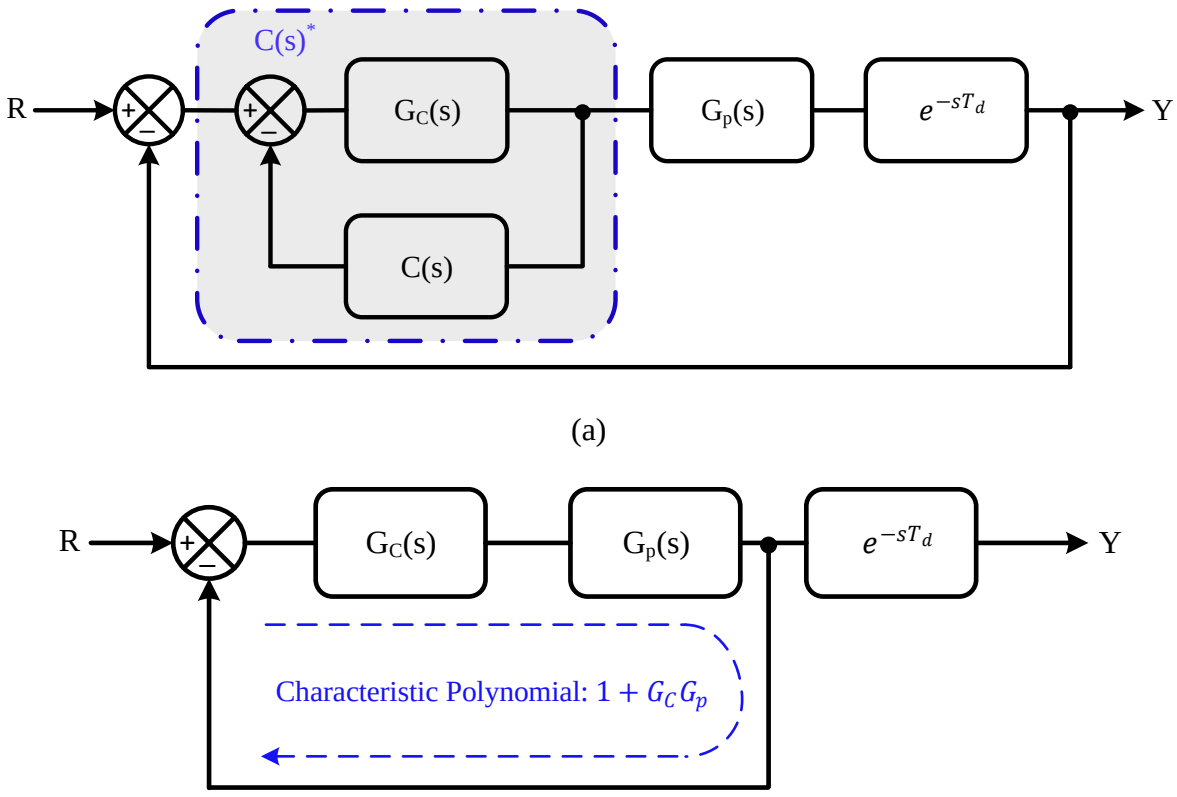


Figure 2.4 Control of a plant with delay (a) SP employed block (b) equivalent block [40].

Equating the closed loop TF of (2.3) and (2.4), the TF of $C(s)^*$ can be obtained;

$$C(s)^* = \frac{G_c(s)}{1+G_c(s)G_p(s)(1-e^{-sT_d})} \tag{2.5}$$

Also, referring to block in Figure 2.4 (a), $C(s)^*$ can be derived;

$$C(s)^* = \frac{G_c(s)}{1+G_c(s)C(s)} \tag{2.6}$$

The expression for SP compensator shown as $C(s)$ in Figure 2.4 (a) can be obtained by comparing (2.5) and (2.6);

$$C(s) = G_p(s)(1 - e^{-sT_d}) \tag{2.7}$$

Equation (2.7) gives the model of compensator to be employed in the forward path along with existing controller to achieve a delay free response. Moreover, an important observation from (2.7) is that it requires the model of plant and delay. When such compensator is realized for a system consisting of delays like the PHIL, it becomes critical that each device in the PHIL loop is modelled accurately.

2.7. A Grid Connected PV Source

The use of PV source as a backup supply for supporting the main power units as well as in emergency facilities has been popular over the years [43]. In addition, PV systems being renewable source are preferred in standalone and grid-connected configurations. Each PV application demands different implementation schemes. Grid connected PV systems require either a centralized inverter or multiple inverters for power transfer. This can be achieved through single or two stages. Each of these schemes have their own pros and cons [44]. The single stage topology in which a centralized inverter is responsible for MPPT, grid current control and voltage amplification is simple and cost effective but has potential drawbacks [45].

The reduced tracking efficiency during partial shading due to centralized MPPT, losses due to module mismatch, and derating result in low power output. There are other schemes where a string of PV modules interfaced with a string inverter has higher tracking efficiency as compared with the centralized inverter configuration due to localized MPPT in individual strings. Few other single stage topologies require the PV voltage to be higher or equal to the peak of grid voltage and hence offer lesser flexibility [44]. Considering the limitations of single stage topologies, dual stage PV energy conversion techniques were introduced to obtain better flexibility in terms of mass production and higher efficiency in the energy conversion process [46]. In these topologies, each PV module or string is connected with a DC-DC converter stage that is interfaced with a DC link of a common inverter stage. While each DC-DC converter is responsible for MPPT, the DC-AC inverter takes care of the grid current and DC bus voltage control [47]. A better control is achieved on individual PV strings by implementation of distributed level energy converters, which sometimes are also referred as DC power optimizers. This approach overcomes the shortcomings of the central inverters in terms of energy harvesting efficiency, reliability as well as flexibility in operation and future enlargements.

Integrating PV power to AC or DC grid requires a converter in between. The advantages of these converters are MPPT and power factor correction to name a few. However, the interaction of these converters with the grid raises a concern for stability issues. The PHIL study with the PV inverter to estimate the grid impedance is presented in [48]. This estimation technique allows to study the effect of connecting the converter to an emulated grid with time varying grid impedance, especially in a PHIL setup. Similar other studies have been carried out with PV source to evaluate the performance in PHIL. A PV emulation including the electric

thermal model with PHIL is presented in [49], while [50] uses PHIL to evaluate PV micro-inverter. A case study for testing a 500 kW PV inverter connected to a PV source using PHIL is presented in [51]. A DC loop PHIL is used to emulate the PV characteristic and an AC loop PHIL is used to emulate the connection of inverter to a distribution grid to study the reactive power control of an inverter as well as its effect on the distribution grid. There are no limitations in the type of system evaluation with PHIL, but PV application remains a popular choice to carry out such investigations.

2.8. PHIL Case Studies

The majority of PHIL studies in literatures have focused towards improving the stability and accuracy of the PHIL loop. Work proposed in Ren, Steurer and Baldwin [26], and Ren, Steurer and Baldwin [52] serves as a basic framework for choosing IA based on accuracy and stability for various applications. Similarly, the interfacing issues of RTS along with inclusion of compensation for improving the accuracy of ITM is discussed in [30] and [36]. Another work focuses on accuracy improvement through online-parametric estimation using wide-band system identification technique for a DIM interface [53].

The application of PHIL studies is broad yet relatively new and the existing works are analyzed case-based rather than generic. The range of PHIL application varies from source emulation like solar and wind farm [49], [54], [55], switch-mode amplifier [32], [56], grid connected systems evaluation [57], [58] to cases where it requires grid impedance measurement [48].

2.9. Summary of Chapter 2

This chapter presented a general overview of the crucial components comprising the PHIL architecture. The chapter started with a short historical background behind the development of RTS and finally ended with the mentions of some notable case studies relating to PHIL. In between, the rational representation of delay model along with the SP compensator development is described with some mathematical formulations.

Chapter 3

Small-Signal Model of a Physical PV-Controller with CHIL Validation

- *This chapter is the result of original work published under* ***M. Pokharel****, A. Ghosh and C. N. M. Ho,* ***"Small-Signal Modelling and Design Validation of PV-Controllers With INC-MPPT Using CHIL," IEEE Transactions on Energy Conversion****, vol. 34, no. 1, pp. 361-371, March 2019.*

The purpose of this work is to analyze the PV source to be able to apply it as a renewable source for PHIL testing. Also, to understand and get familiar with RTS device and its interface, PV model in RTDS is configured with a PCS with an actual controller connected using a CHIL approach. With CHIL, the MPPT controller implemented in DSP control-card can directly be used to track the maximum power from the PV panel. The CHIL approach enables to practically validate the PV model and its associated controller for power conversion which may aid in control design process. The details about this work is discussed in sections following.

3.1. Introduction

The maximum energy that can be harvested from a PV system at any instant depends on the effectiveness and response time of the MPPT algorithm used and related controllers. To facilitate proper controller design, a precise mathematical model of the system is required. Besides the controller, it is also important to know the architecture in which the PV source is connected to extract its power. It is common to have PV systems connected to the grid through inverters to transfer power to the grid. But as the number of PV source starts to grow, concerns for reliability and efficiency becomes critical. As a result, a lot of researches have reported various structures with single and two stages of power processing for connecting PV source to the grid [44]- [47]. One of such prominent schemes for extracting power from PV source is a two-staged GCPI which consists of a DC-DC converter responsible for MPPT and a DC-AC inverter for feeding power to the grid. A typical layout for power extraction with such scheme is shown in Figure 3.1.

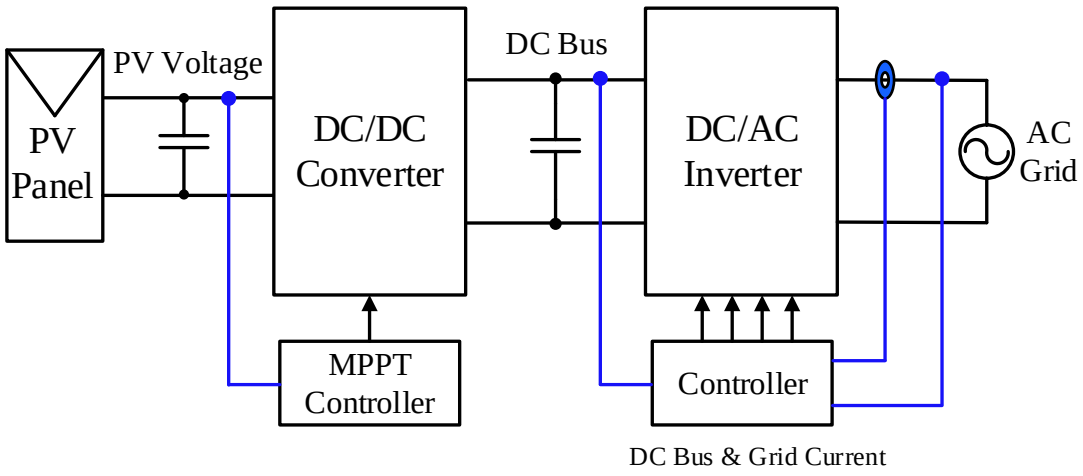


Figure 3.1 A typical two-stage grid connected PV inverter scheme.

One of many variants of schematic in Figure 3.1 is its application as a DC power optimizer where the DC PCS (PV panel and DC-DC converter) is paralleled with multiple such stages followed by a single central inverter [44], [47], [59]. The DC-DC converter in the DC PCS is particularly responsible for MPPT which may be achieved with topologies like boost converter, buck-boost converter, SEPIC converter or various boost derived converters [60]-[62]. There are no such limitations in the topology itself and are also application dependent, but the choice of boost-based converter is supported by the fact that such converters provide a stable DC output voltage along with input voltage step-up function for PV [62]. The limitations are rather with the controller or the control algorithm as the same topology may exhibit improved power conversion and MPPT efficiency with the use of more advanced algorithms [63], [64].

For a GCPI shown in Figure 3.1, the performance of each PCS as well as their controllers is important in determining the overall performance of such system. Therefore, it is essential that each of these components are evaluated to decide the architecture and algorithm that can guarantee an efficient system. With the increasing penetration of PV energy into the grid, the effect of adding these switching converters at the Point of Common Coupling (PCC) also becomes an important grid integration study. Besides, the performance of inverter during various grid transients is another prospect that needs to be covered to understand the operation challenges of connecting such switching converters to the grid. Further, to simplify the study, the system in Figure 3.1 can be broken down into two parts; first the DC PCS which consists of a PV panel, a DC-DC converter and a MPPT controller, and second the AC PCS which consists of an inverter connected to the grid with its controller which controls the power delivered to the grid by controlling the grid current and at the same time maintaining the DC

bus voltage to the desired set point. The DC and AC PCS can be analyzed individually to understand their performance parameters. The sections in this chapter would focus on analyzing the DC PCS while the AC PCS is covered in the section of upcoming chapters, Chapter 4 and Chapter 5.

3.2. System Description

In this chapter, a simplified approach to obtain the comprehensive small-signal model of a DC PCS is proposed. This model enables robust and accurate control system design and evaluation of system performance. The small-signal model consists of a linearized model of PV, an outer loop responsible for MPPT and an inner voltage control loop. The small-signal model of a controller implemented in a DSP is verified with an RTS-based testing environment. The power stage consisting of a PV source and a boost converter is simulated in RSCAD, which is the software interface for RTDS real time simulator. The controller is implemented in a F28M35 Texas Instrument DSP, which is commonly used in the industry. This method of implementation is widely known as CHIL. In addition to the development of small-signal model, this work also proposes a unique approach of frequency response measurement using a Gain Phase Analyzer (GPA) by further extending the CHIL implementation.

In control system design and optimization studies, the system model and controller are conventionally validated in simulations followed by a laboratory-scale hardware setup [65]. However, the proposed system-evaluation approach allows a control system designer to test and ensure the robustness of the controller in an environment that closely emulates its real-world application. This technique offers great flexibility in design process and scalability, as it allows easy change of design parameters to study the system response.

3.3. System Architecture

The system schematic shown in Figure 3.1 consists of a PV panel connected to a DC-DC converter controlled through a digital controller at Maximum Power Point (MPP). The DC bus voltage at the output is controlled by a second stage inverter and can simply be replaced by a DC voltage source. Similarly, among other DC-DC converters, boost is considered efficient as well as flexible in terms of stepping up the panel voltage by significant amount [66]. Therefore, for evaluating the DC PCS, boost converter is selected for this study. For this, firstly a small-signal model of the converter and their controllers is developed followed by their validations. The system is further analyzed in the entire range of I-V curve to demonstrate its performance along various operating points.

3.3.1 Topology of Power Conversion Stage

A boost converter coupled to a PV source constitutes the PCS whereas a MPPT and voltage controller forms the controller stage. The schematic of the DC PCS under investigation is shown in Figure 3.2. The power exchange occurs between the DC grid and the PV source. A constant DC voltage source v_{dc} is connected at the output terminal of the boost converter to represent the DC bus of the system shown in Figure 3.1 [67]. Although the topology is same as a simple boost converter, the principle of operation is different. The output voltage is fixed by the central inverter as shown in Figure 3.1. The boost converter in this application is used to control the input voltage in contrast to the output voltage control of a conventional boost converter. This difference makes the state space model of the power circuit different from that of a boost converter.

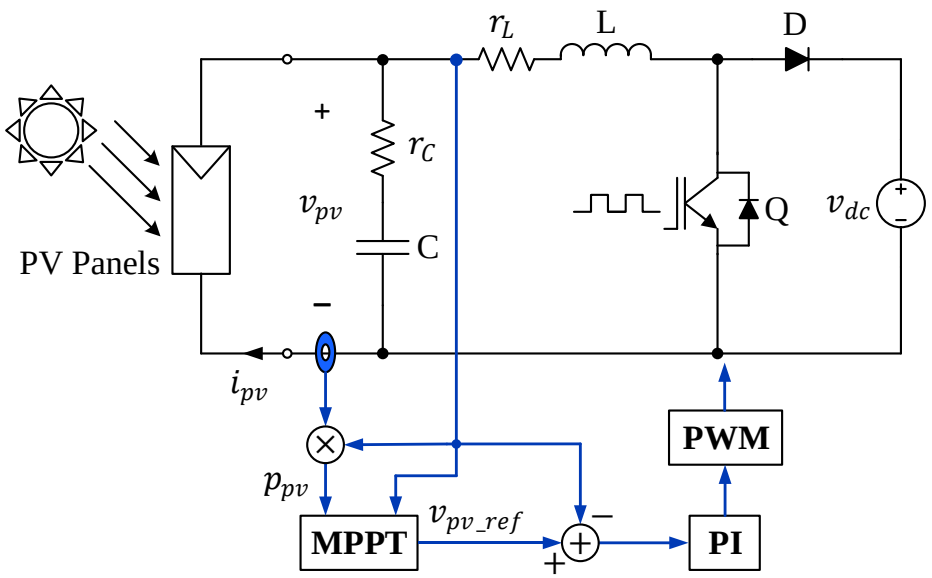


Figure 3.2 Architecture of a DC power conversion stage.

3.3.2 Control Strategy

There are two control loops associated with the system in Figure 3.2. In the first loop of MPPT, the INC algorithm is used to track the PV panel voltage at MPP under different operating conditions. The measurement of PV panel voltage v_{pv} and current i_{pv} is required to track the instantaneous power p_{pv}. Based on the INC algorithm, any deviation from the MPP would result in the change in conductance estimated through the computation of derivative of instantaneous power with respect to voltage i.e. dp_{pv}/dv_{pv}. The point at which this ratio becomes zero is the point of MPP and the corresponding voltage at this point is considered by the MPPT controller as the reference voltage $v_{pv_{ref}}$. This reference voltage is fed to the inner control loop in which the Proportional Integral (PI) controller tries to maintain the input voltage at $v_{pv_{ref}}$. To reiterate, even though the topology of power circuit is a boost converter, its

principle of operation is similar to that of a typical buck converter hence it is often referred as inverse buck converter [68].

3.4. Mathematical Modelling

The mathematical modelling includes the development of linear model of PV source along with state space model of an inverse buck converter as a PCS model and consequently modelling individual controllers. The developed small-signal model presents a comprehensive model capable of describing the dynamics of the power stage and controllers that can aid in robust controller design.

3.4.1 Linearized Model of a PV source

The PV source can be linearized around the MPP by a tangent passing through the MPP. The typical I-V characteristics of a PV panel is shown in Figure 3.3 and a point (V_{mpp}, I_{mpp}) is marked in the curve to indicate the MPP. A tangent drawn at this point with a slope $-1/R_{mpp}$ represents the conductance of the system (R_{mpp} being the resistance of the system at MPP). Henceforth the linear model of PV operating at its MPP is represented with a negative resistive source [69].

Mathematically, it can be expressed as a linear equation having a certain slope.

$$i_{pv} - I_{mpp} = -\frac{1}{R_{mpp}} \cdot \left(v_{pv} - V_{mpp}\right) \tag{3.1}$$

The above equation (3.1) can be readily used to represent the linear model of a PV source operating around the point of MPP. This equation is valid as long as the system operates around the MPP and is therefore helpful to develop the small-signal model of PV source with MPPT.

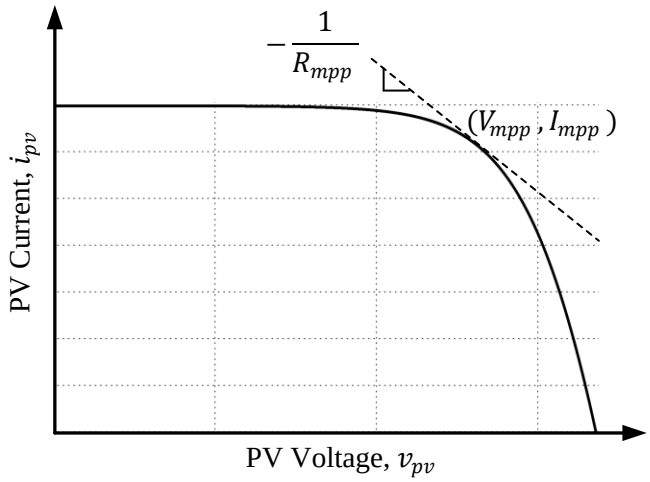


Figure 3.3 Linear model of a PV source

If the linear model of PV is to be operated at points other than MPP, expression (3.1) cannot guarantee the accuracy. Therefore, one of the approaches to develop the linear PV model is to linearize the PV equation about the operating points. The Single-Diode (SD) model can be considered to validate the PV model at points other than MPP. Other improved models which considers the accuracy in developing the PV model is described in literatures [70], [71]. Similarly, the dynamic model of the PV considering both the forward and reverse bias characteristics of diode, parallel capacitances and series inductances is presented in [72]. All these models have their own advantages in terms of accuracy or completeness. Moreover, the SD model in [73] and [74] offers a fair balance between accuracy and simplicity and hence the model has been chosen in this work for analysis. The SD model presented in Villalva, Siqueira and Ruppert [74] can be represented by the mathematical expression in (3.2). Linearizing (3.2) about an operating point gives the conductance at that particular point.

$$i_{pv} = I_{pv} - I_o \left[\mathrm{e}^{\left(\frac{v_{pv}+R_S \cdot i_{pv}}{V_t \cdot N_S \cdot a}\right)} - 1 \right] - \frac{v_{pv}+R_S \cdot i_{pv}}{R_p} \tag{3.2}$$

Differentiating (3.2) about any operating point (V, I) the conductance may be estimated [74]. The equation governing the conductance can be expressed as;

$$g(V,I) = \frac{-I_o \cdot e^{\left(\frac{V+I\cdot R_S}{N_S \cdot V_t \cdot a}\right)} - \frac{1}{R_p}}{1+\frac{R_S}{R_p}+I_o \cdot e^{\left(\frac{V+I\cdot R_S}{N_S \cdot V_t \cdot a}\right)} \cdot \frac{R_S}{N_S \cdot V_t \cdot a}} \tag{3.3}$$

Where, I_{pv} and I_o are the photovoltaic and saturation currents of the array and V_t is the thermal voltage of the array with N_s cells connected in series. R_s and R_p are the equivalent series and parallel resistance of the array, and a is the diode ideality constant.

3.4.2 Modelling a Converter

For the completeness of modelling, boost converter is modelled with parasitic resistances of both inductor and capacitor. The inclusion of parasitics in the power stage simplifies the controller design, as the damping introduced by these parasitic elements eliminates the need for an additional differential component and just a standard PI controller can maintain the PV array voltage at the reference [75].

The schematic in Figure 3.4 consists of a linear model of PV represented with a resistance R_{mpp} and a boost converter including the parasitic resistances r_L and r_C associated with the inductor L and capacitor C respectively. The state space averaging technique is used to represent the converter in terms of its low frequency small-signal TF.

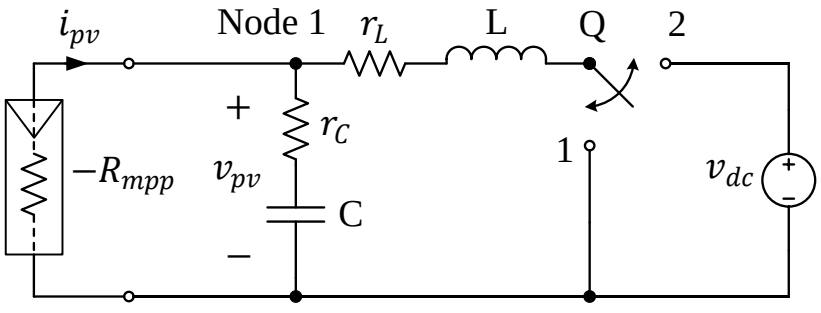


Figure 3.4 Schematic of a power conversion stage

There are two operating modes due to the switching of main semiconductor switch Q in Figure 3.4; Q=ON represented by Mode-I when switch position is in "1" and Q=OFF represented by Mode-II when switch position is in "2". State equations for each operating mode are averaged to combine them using the duty cycle information. The converter is assumed to be operating in Continuous Conduction Mode (CCM) and the natural frequency of the converter is much lower than the switching frequency [76], [77].

Using the following definitions to operating circuit in Figure 3.4,

- State variables $x(t)$ as inductor current and capacitor voltage; $x(t) = \{i_L(t), v_c(t)\}$.
- Input variable $u(t)$ as the DC link voltage v_{dc}.
- Output variable $y(t)$ as the PV voltage $v_{pv}(t)$.

For Mode-I operation with Q=ON, the state equations are,

$$\frac{dv_C}{dt} = -\frac{R_{mpp}}{C(R_{mpp}+r_C)} \cdot i_L - \frac{1}{C(R_{mpp}+r_C)} \cdot v_c \tag{3.4}$$

$$\frac{di_L}{dt} = -\frac{R_{mpp}(r_C+r_L)+r_L \cdot r_C}{L(R_{mpp}+r_C)} \cdot i_L + \frac{R_{mpp}}{L(R_{mpp}+r_C)} \cdot v_C \tag{3.5}$$

An expression for the output in terms of state variables can be derived as,

$$v_{pv} = -\frac{r_C \cdot R_{mpp}}{(R_{mpp}+r_C)} \cdot i_L + \frac{R_{mpp}}{(R_{mpp}+r_C)} \cdot v_C \tag{3.6}$$

For Mode-II operation with Q=OFF, the state equation of (3.4) remains valid for this mode as well. The state equation with respect to $i_L(t)$ however changes.

$$\frac{di_L}{dt} = -\frac{R_{mpp}(r_C+r_L)+r_L \cdot r_C}{L(R_{mpp}+r_C)} \cdot i_L + \frac{R_{mpp}}{L(R_{mpp}+r_C)} \cdot v_C - \frac{v_{dc}}{L} \tag{3.7}$$

A detailed derivation of (3.4) – (3.7) is presented in the Appendix A.1.

Comparing the state and output equations with the standard averaged state equation, the respective state, input and output matrices can be easily extracted. The averaged state equations are given by:

$$\left.\begin{matrix}\dot{x} = [A]x + [B]u \\ y = [C]x\end{matrix}\right\} \tag{3.8}$$

where, $A = A_1\, d + A_2\,(1-d)$, $B = B_1\, d + B_2\,(1-d)$, $C = C_1\, d + C_2\,(1-d)$ and d the duty cycle. The ON time is defined by dT_s and OFF time by $(1-d)T_s$, where T_s is the time period for one switching cycle.

Comparing (3.4), (3.5), (3.6) and (3.7) with the standard averaged state equations (3.8),

$$A = A_1 = A_2 = \begin{bmatrix} -\dfrac{R_{mpp}(r_C + r_L) + r_L r_C}{L\left(R_{mpp} + r_C\right)} & \dfrac{R_{mpp}}{L\left(R_{mpp} + r_C\right)} \\ -\dfrac{R_{mpp}}{C\left(R_{mpp} + r_C\right)} & -\dfrac{1}{C(R_{mpp} + r_C)} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}; B_2 = \begin{bmatrix} -\dfrac{1}{L} \\ 0 \end{bmatrix}; C = C_1 = C_2 = \begin{bmatrix} -\dfrac{r_C R_{mpp}}{R_{mpp} + r_C} & \dfrac{R_{mpp}}{R_{mpp} + r_C} \end{bmatrix}$$

Introducing small-signal perturbation in state variables and duty cycle, and taking Laplace transform, the power-stage TF can be determined as:

$$T_p(s) = \frac{\tilde{v}_{pv}}{\tilde{d}} = C \cdot [sI - A]^{-1} \cdot [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot V_{dc}] + (C_1 - C_2) \cdot X \tag{3.9}$$

By substituting the values of A_1, A_2, B_1, B_2, C_1 and C_2 into (3.9):

$$T_p(s) = \frac{-V_{dc}}{L} \cdot \left\{ \frac{{R_{mpp}}^2}{C \cdot {R_{C\_mpp}}^2} + \frac{r_c \cdot R_{mpp}\left(s + \frac{1}{C \cdot R_{C\_mpp}}\right)}{R_{C\_mpp}} \right\} \cdot \frac{1}{p(s)} \tag{3.10}$$

where,

$R_{C_{mpp}} = r_C + R_{mpp}$ and $p(s) = \frac{{R_{mpp}}^2}{L \cdot C \cdot {R_{C\_mpp}}^2} + \left(s + \frac{1}{C \cdot R_{C\_mpp}}\right)\left(s + \frac{r_c \cdot R_{mpp} + r_L \cdot R_{C\_mpp}}{R_{C\_mpp}}\right)$

With the small-signal TF of power stage developed, the mathematical models of MPPT and voltage controller is required to complete the small-signal model of the overall system shown in Figure 3.2.

3.4.3 Modelling a MPPT Controller

The input to MPPT controller is PV voltage and current, which is used to generate the reference voltage at which the instantaneous power from the PV array is maximum. The operating point can be easily estimated based on the incremental conductance computed by calculating $\Delta p_{pv}/\Delta v_{pv}$. Mathematically, INC may be expressed as:

$$\frac{dp_{pv}}{dv_{pv}} = \frac{d(v_{pv} \times i_{pv})}{dv_{pv}} = i_{pv} + v_{pv} \cdot \frac{di_{pv}}{dv_{pv}} \Longrightarrow \frac{1}{v_{pv}} \cdot \frac{dp_{pv}}{dv_{pv}} = \frac{i_{pv}}{v_{pv}} + \frac{di_{pv}}{dv_{pv}}$$

$$\Longrightarrow e = \frac{i_{pv}}{v_{pv}} + \frac{di_{pv}}{dv_{pv}} \tag{3.11}$$

In (3.11), the error e is expressed as a sum of the actual conductance i_{pv}/v_{pv} and the incremental conductance di_{pv}/dv_{pv}. The maximum power can be harvested from the PV array at the point where the measure of incremental conductance and actual conductance are equal. If this ratio is greater than zero, the operating point lies to the left of MPP and it lies to the right if this ratio is less than zero, as shown in Figure 3.5.

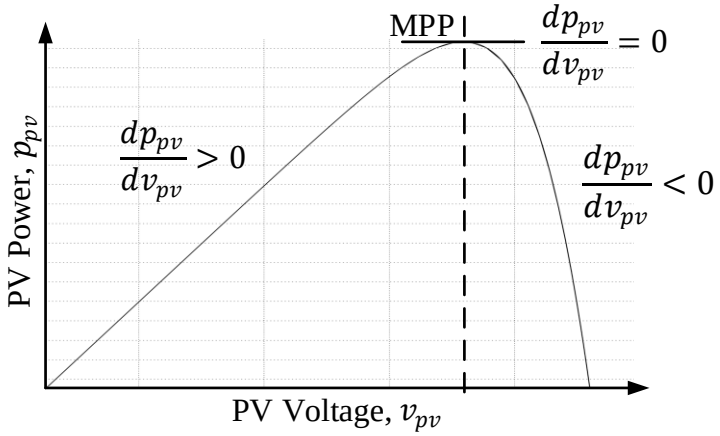


Figure 3.5 Graphical representation of an INC algorithm.

Linearizing (3.11) around MPP (V_{mpp}, I_{mpp}) as shown in Figure 3.3 and Figure 3.5. The small-signal model is,

$$\tilde{e} = K_m \cdot \tilde{v}_{pv} \tag{3.12}$$

where, $K_m = -\frac{2}{R_{mpp} \cdot V_{mpp}}$

The detailed derivation of (3.12) is included in the Appendix A.2.

The above equation gives the small-signal relation between error variable $\tilde{e}$ and PV voltage $\tilde{v}_{pv}$ with a factor K_m that describes the MPPT action. This error when fed through an integrator generates the required voltage reference. Mathematically, this may be shown by,

$$V_{pv\_ref}[k] = V_{pv\_ref}[k-1] + K_i \cdot \frac{T_s}{2}(E[k] + E[k-1]) \tag{3.13}$$

The detailed derivation of (3.13) is shown in the Appendix A.3.

Since the implementation is carried out digitally, discrete integrator is considered for the entirety of the modelling. Equation (3.13) gives the expression for digital implementation of an integrator. This discrete integrator of trapezoidal form is then converted to its s-domain continuous time counterpart using the bilinear Tustin's transformation for modelling purpose. This would simply result in K_i/s.

3.4.4 Modelling a Voltage Controller

A PI controller may be used to control the process consisting of power stage and Pulse Width Modulator (PWM). The TF of a typical PI controller is given below in (3.14). Since the overall open loop gain of the voltage control loop is negative, the PI controller is designed with a negative gain such that a positive gain is finally introduced in the system.

$$T_c(s) = -\left(\frac{K_p s + K_i}{s}\right) \tag{3.14}$$

The PI controller above is digitally implemented in DSP to regulate the PV voltage at its reference MPP value. The digital implementation of PI controller requires the z-transform of the continuous-time function of PI controller.

$$v_i[k] = v_i[k-1] + r[k] \cdot \left[K_p + \frac{K_i \cdot T_s}{2}\right] + r[k-1] \cdot \left[\frac{K_i \cdot T_s}{2} - K_p\right] \tag{3.15}$$

A detailed derivation of (3.15) is presented in the Appendix A.4.

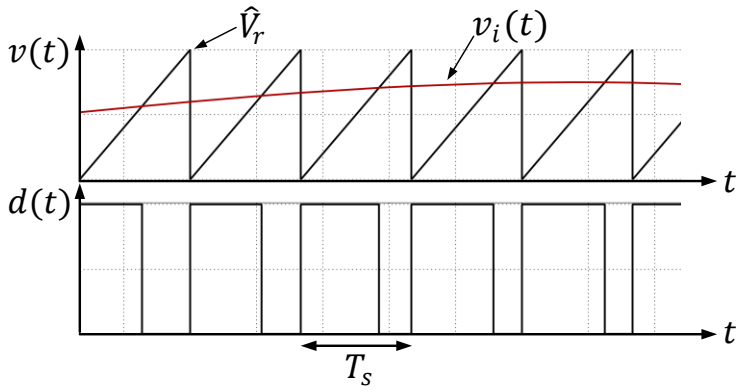


Figure 3.6 Generation of PWM.

With the mathematical model of controllers developed in discrete domain, the discrete model of the PWM can then be developed. From Figure 3.6, the small-signal TF of the modulator can be expressed as:

$$T_m(s) = \frac{\tilde{d}(s)}{\tilde{v}_i(s)} = \frac{1}{\hat{V}_r} \tag{3.16}$$

where, $v_i(t)$ is the input signal of the modulator and $\hat{V}_r$ is the peak value of the carrier. A detailed derivation of (3.16) is included in the Appendix A.5. From (3.16) it is seen that the TF of the modulator is a gain expressed as the reciprocal of the carrier peak.

With the mathematical models for power stage, MPPT controller, voltage controller and modulator, the small-signal relationship between these key elements can be represented with a block diagram in Figure 3.7.

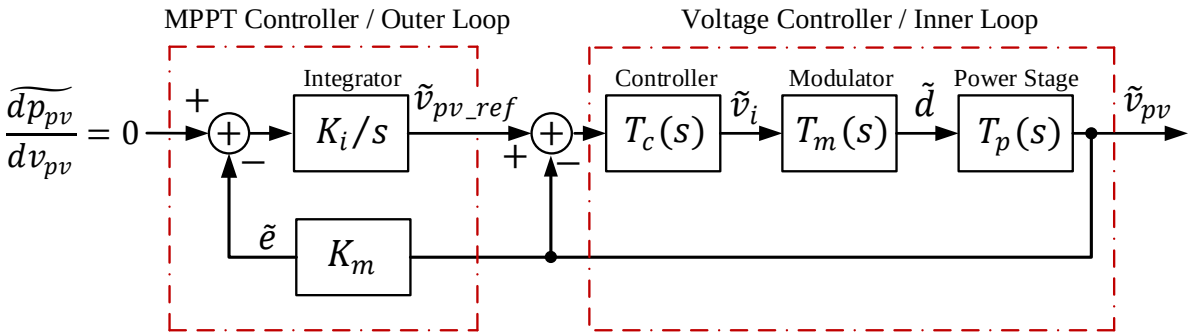


Figure 3.7 A comprehensive small-signal model of PV source with its controller.

3.5. Model Validation and Controller Design

The mathematical model of power conversion stage developed in Section 3.4 needs to be validated for its accuracy before it can be used to design the controller. The subsequent sections present the details about the model validation and controller designs.

3.5.1 Power Stage Model Validation

To validate the mathematical model of DC PCS in the entire operating region of the I-V curve a single BP-365 PV-module is considered. The specification of the module is presented in Table 3.1.

The model presented in Section 3.4 is validated in the Constant Current (CC) region, MPP and Constant Voltage (CV) region of the I-V curve. In this model, the PV source is modelled as a negative resistance. It may be noted that the value of this resistance changes for every operating point. The linearized PV model given by equation (3.3) is used to calculate the equivalent PV resistance for that point. The key parameters for this model are determined in a similar way shown in [74] and is tabulated in Table 3.2.

Table 3.1 Parameter of BP-365 PV module at Standard Test Conditions (STC).

PV Module Parameter	**Value**
Open circuit Voltage (V_{OC})	22.1 V
Short circuit current (I_{SC})	3.99 A
Voltage at MPP (V_{mpp})	17.6 V
Current at MPP (I_{mpp})	3.69 A
Power at MPP (P_{max})	65 W
Temperature coefficient of I_{SC}	0.065 %/°C
Temperature coefficient of V_{OC}	-0.08 V/°C

Table 3.2 Equivalent SD model data for BP-365.

PV Module Parameter	**Value**
Saturation Current (I_O)	7.4198e-10 A
Series Resistance (R_S)	0.444 Ω
Parallel Resistance (R_P)	204.027 Ω
Ideality Factor (a)	1.067

In Figure 3.4, R_{mpp} is replaced with the corresponding resistances at each operating point while performing the analysis. The AC sweep results from PLECS (simulation), are superimposed with the developed mathematical model frequency response, labelled as “Sim”, and “Math” respectively, for each of these operating points and is presented in Figure 3.8.

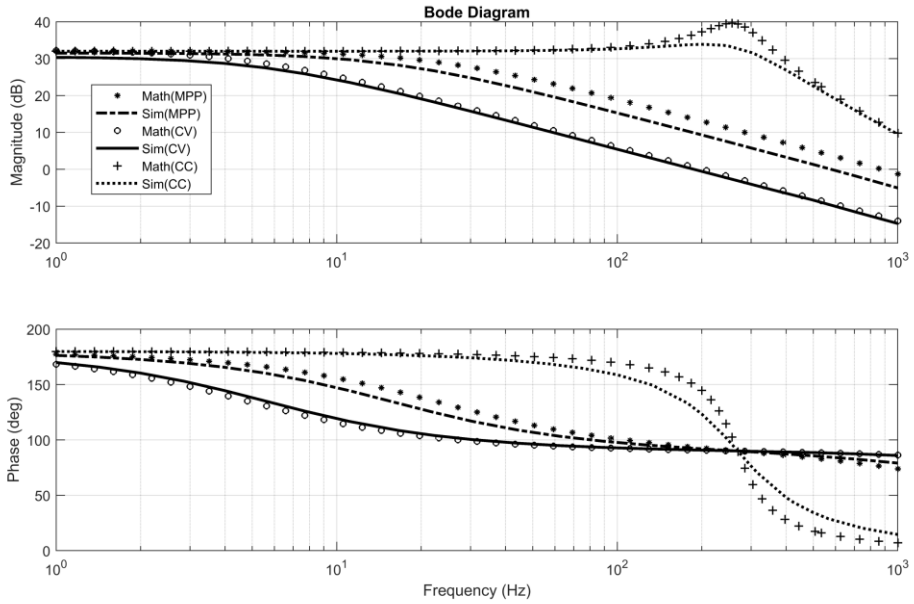


Figure 3.8 Power stage frequency responses at various operating points in I-V curve.

The results from both simulation and developed mathematical model exhibit a close match thus validating the small-signal model derived for the power stage. Once the model is validated with single PV module, it is scaled up to 10 × 4 array system with specifications shown in Table 3.3 for implementation purpose.

Table 3.3 System specifications.

PV Source Parameter	**Value**	**Converter Parameter**	**Value**
Rated power	2.6 kW	Output Voltage (v_{dc})	400 V
Open Circuit Voltage (V_{OC})	221 V	Input Capacitance (C)	10 µF
Voltage at MPP (V_{mpp})	176 V	Capacitive resistance (r_C)	0.05 Ω
Short Circuit current (I_{SC})	15.96 A	Inductor (L)	35 mH
Current at MPP (I_{mpp})	14.76 A	Inductive resistance (r_L)	0.2 Ω
Array Size	10 × 4	Switching Frequency (f_{sw})	2 kHz

Further, the model accuracy is investigated through frequency response for variation in input capacitance considering the stray capacitance contributed by the PV string. The model showed a very little to no variation in gain and phase from original specified capacitance as shown in Figure 3.9. The label C=1, C=0.9 and C=1.1 in Figure 3.9 represents the nominal value in Table 3.3, 90 % of the nominal value and 110 % of the nominal value respectively.

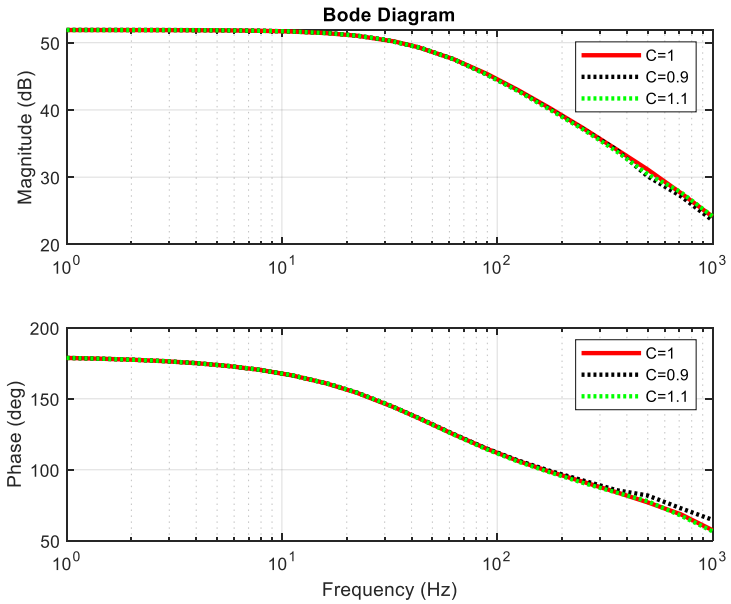


Figure 3.9 Frequency response of power stage due input capacitance variations.

3.5.2 Controller Design

The inner control loop constitutes the process to be controlled i.e. boost converter power stage coupled with PV source (modelled as impedance) and modulator, whereas the MPPT controller represents the outer loop which generates a voltage reference for the inner loop. With the TFs derived in the previous section and system specification shown in Table 3.3, the frequency responses of the overall open loop TF, $T_{OL}(s)$, is studied to design a suitable error

amp for the inner loop. The selection of controller parameters and appropriate bandwidth is done by studying the frequency response of the inner loop shown in Figure 3.10.

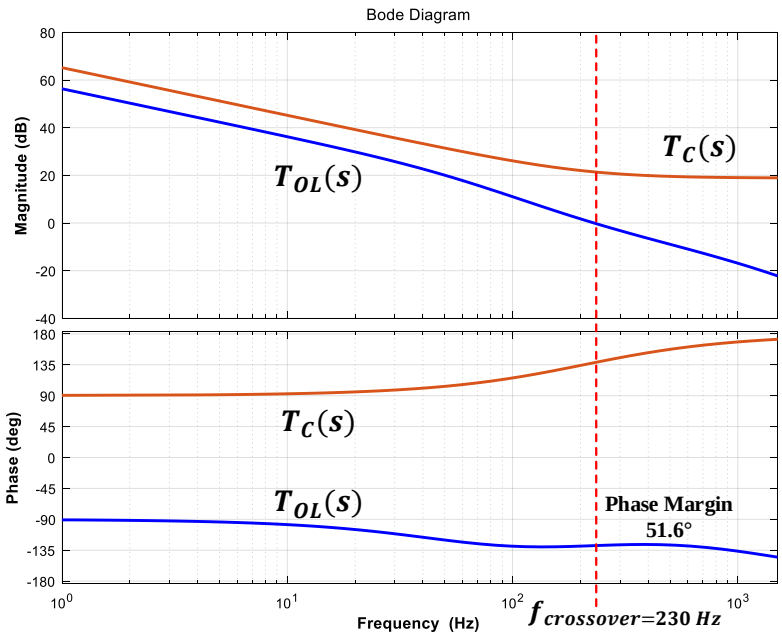


Figure 3.10 Frequency response of inner loop $T_{OL}(s)$ and controller $T_C(s)$.

The overall open loop TF of the voltage control loop is given by:

$$T_{OL}(s) = T_C(s) \cdot T_m(s) \cdot T_p(s) \tag{3.17}$$

The frequency response of $T_{OL}(s)$ is plotted using TFs of $T_p(s)$, $T_C(s)$ and $T_m(s)$ from (3.10), (3.14) and (3.16) respectively.

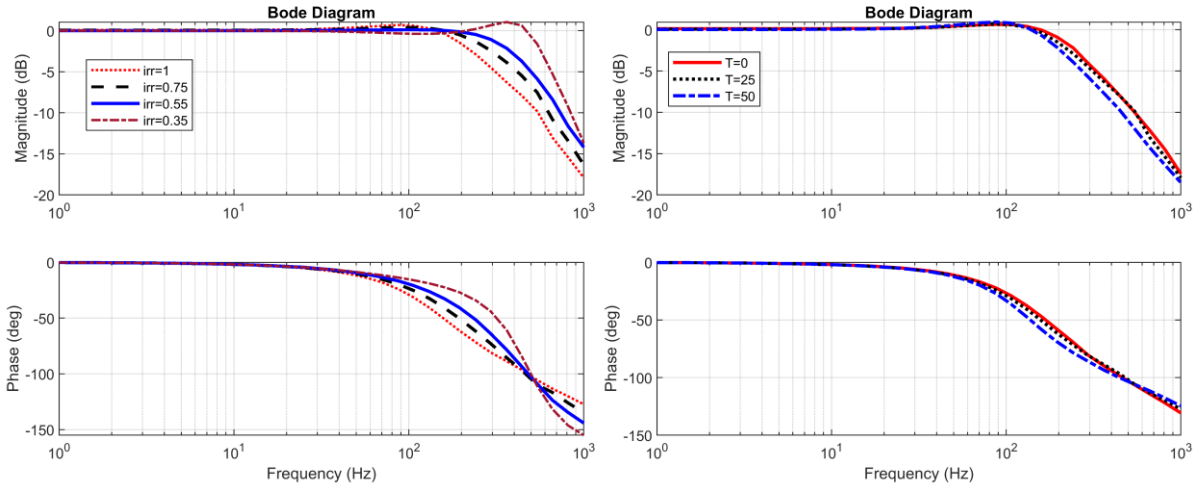
As a rule of thumb, the bandwidth of the inner loop is designed at approximately one-tenth of the switching frequency [78] i.e. at 230 Hz as seen from Figure 3.10. A phase margin of 51.6° at the crossover ensures control system stability and high gain of $T_{OL}(s)$ at low frequency minimizes the steady-state error.

The MPPT and voltage control loops are designed with different bandwidths and the controller parameters are carefully chosen to avoid any possible interference between the two loops.

3.5.3 Controller Performance Evaluation

The response of the designed controller with the chosen MPPT algorithm is assessed for variation of operating conditions such as change in irradiance and temperature. The simulation results for the dynamically changing environmental conditions is presented in Figure 3.11.

The variation observed in the magnitude and phase plots of Figure 3.11 is due to the change of the impedances between MPP points. The system response however remains similar for all operating points with respect to STC response.



(a) (b)

Figure 3.11 Frequency response of inner loop with varying (a) Irradiance at Temp=25 °C and (b) Temperature at Irradiance=1 Sun.

Further to verify the robustness of the controller, the system is simulated with dynamic transition in irradiance causing the inductor current to switch from continuous to Discontinuous Conduction Mode (DCM). The controller can accurately track the correct operating point even during transients, which proves its robust operation. Figure 3.12 demonstrates the controller performance during the transient. The boundary current I_{LB} between CCM and DCM for boost converter can be expressed with (3.18), which serves as a mathematical tool for selection of current and irradiance [79].

$$I_{LB} = \frac{V_{dc}}{2 \cdot L \cdot f_{sw}} \cdot D \cdot (1 - D) \tag{3.18}$$

The duty cycle (D) can be calculated using steady-state equations of boost converter while v_{dc}, L and f_{sw} are known from the converter specifications in Table 3.3.

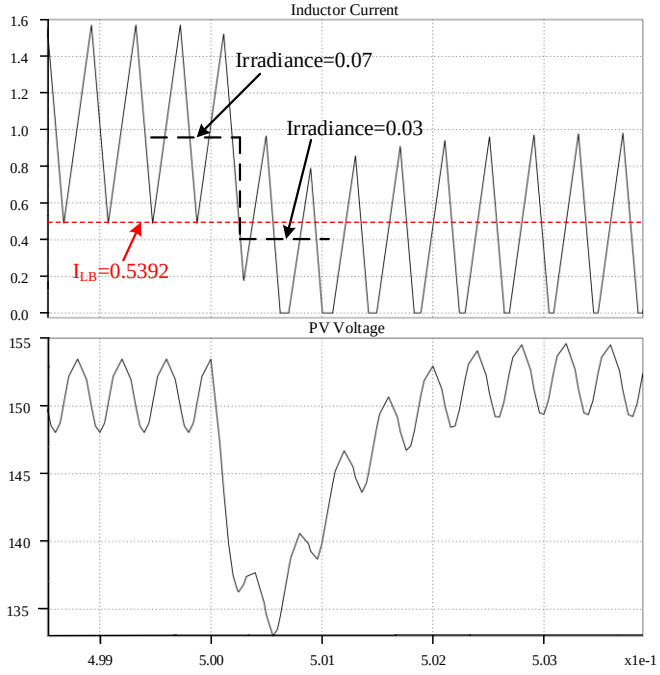


Figure 3.12 Dynamic transition in irradiance for switching from CCM to DCM.

Further extending the analysis, the loci of MPP operating points are plotted for different values of irradiances and temperatures in Figure 3.13. At 25°C, the system moves from CCM to DCM as the inductor current falls below the boundary current with irradiance dropping below 40 W/m^2. This phenomenon is also seen in the simulation result of Figure 3.12. Similar behavior is noticed for other operating points in Figure 3.13.

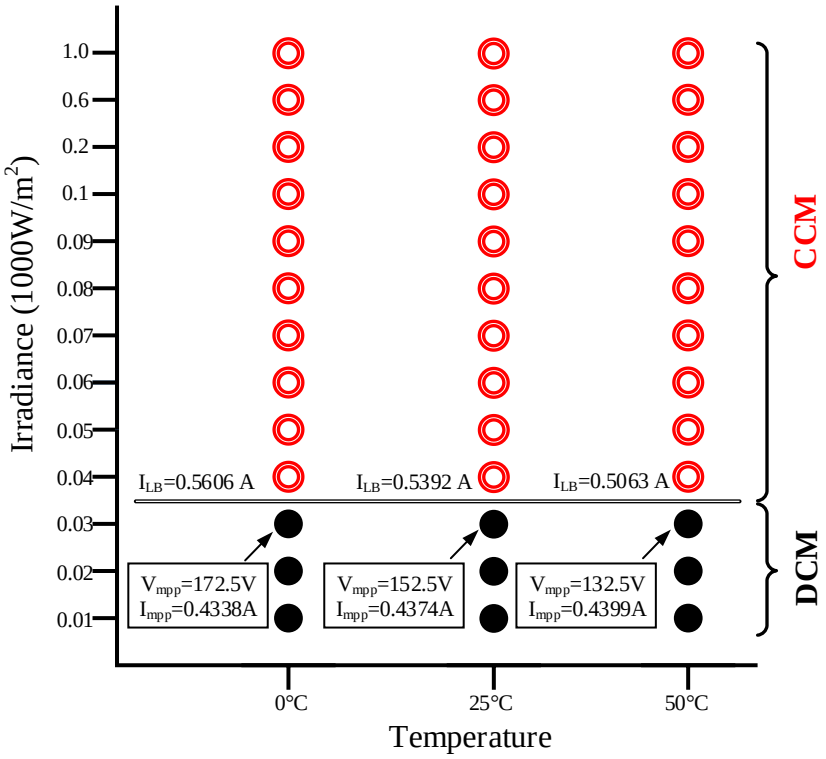


Figure 3.13 Loci of operating points with variation in temperature and irradiance.

3.6. System Implementation and Experimental Results

In order to study the dynamic behavior and bandwidth of the control loops in a practical control hardware as well as to verify the developed small-signal models, CHIL testing methodology is used. The power stage is implemented in the RTDS simulator using RSCAD.

The control loops are implemented in Texas Instrument (TI) F28M35x which is a 150 MHz clock, 12-bit ADC resolution DSP with 300 kHz sampled data. The PV voltage and current are sensed using an analogue interface between the DSP controller and RSCAD power stage. The analogue interface consists of the Giga-Transceiver Analogue Output (GTAO) card and ADC of the DSP. A digital interface provides the gate pulses to the converter from the controller using Giga-Transceiver Digital Input (GTDI) card. The setup used for the experiment is shown in Figure 3.14.

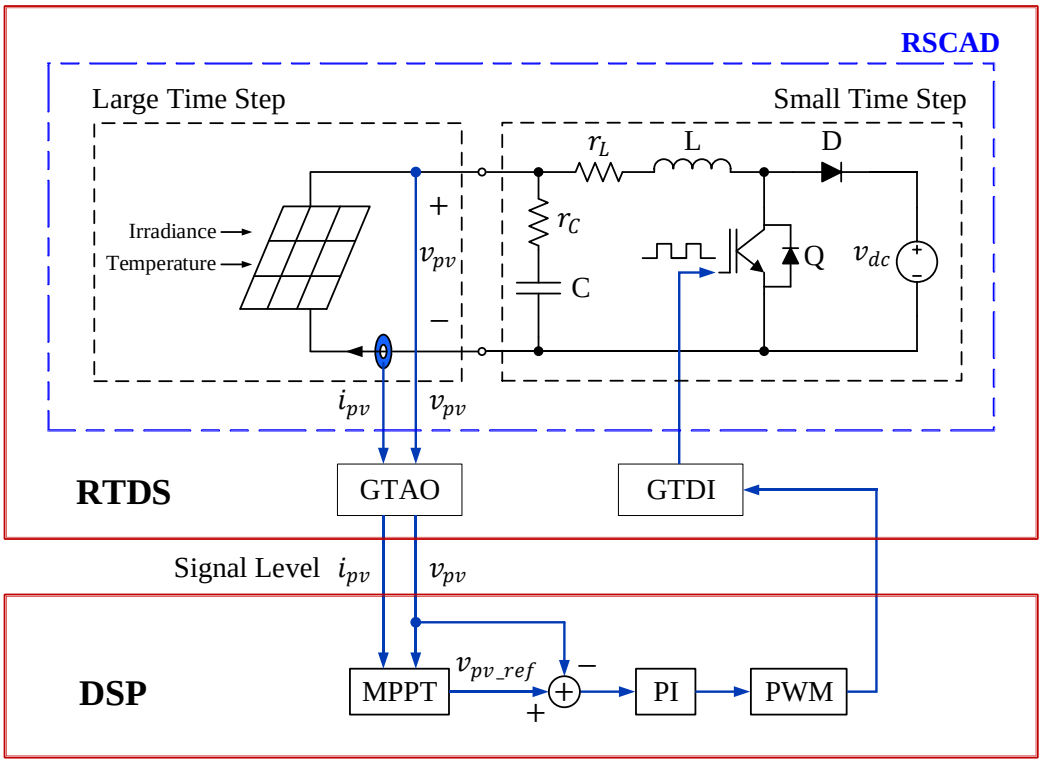


Figure 3.14 System implementation setup for CHIL testing of controller.

In the RSCAD environment, the PV source with specifications shown in Table 3.3 is simulated in the large-time step at 30 µs and the converter inside the small-time step block at 1.4 µs. The small-time step block is configured to receive the switching pulses from the GTDI

card to the converter switches. The up-down counter in the DSP used as the carrier wave is set at 2 kHz, i.e. the switching frequency of the designed system. Two enhanced-PWMs (EPWM) running at different Interrupt Service Routine (ISR) are configured, one to perform MPPT (at 12 kHz) and second to generate modulating signal (at 25 kHz). The MPPT controller with low bandwidth filters out the aliasing noises seen due to down sampling in this kind of multi-rate sampled system [80]. Compare (CMP) registers are configured to store modulation signal and Action Qualifier (AQ) is used to set and reset the pulses based on values in CMP registers.

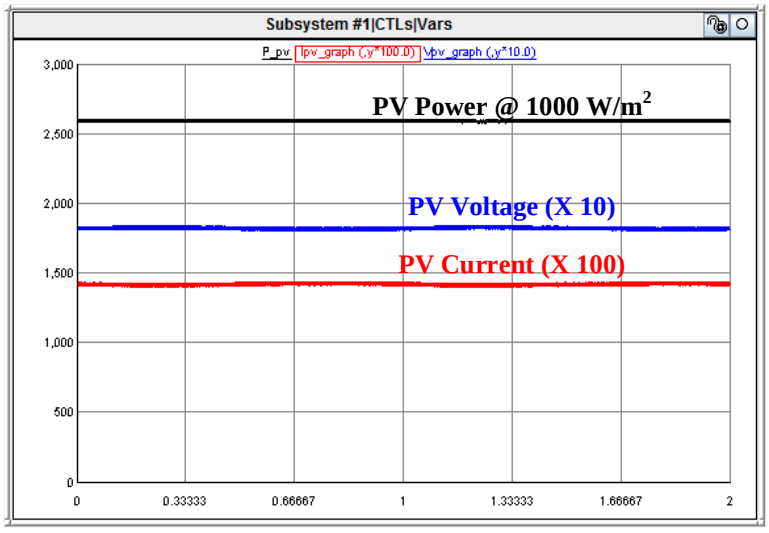
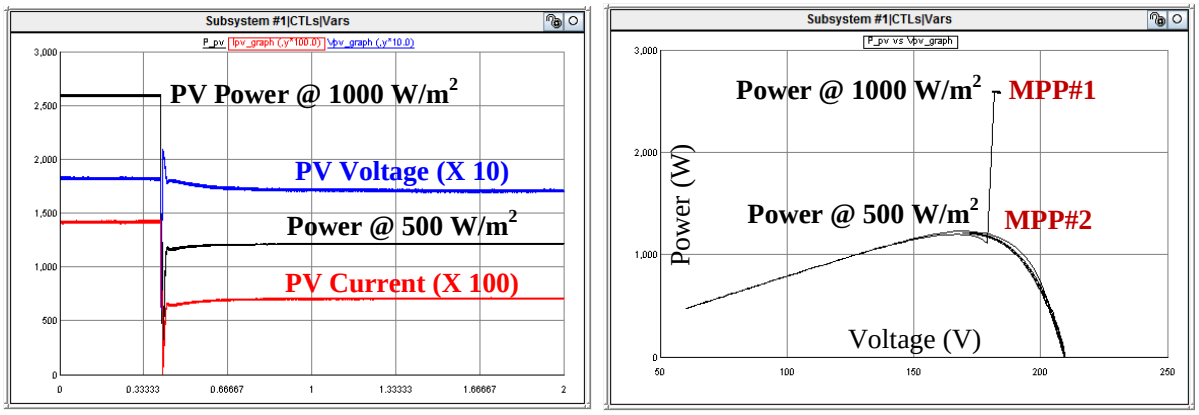


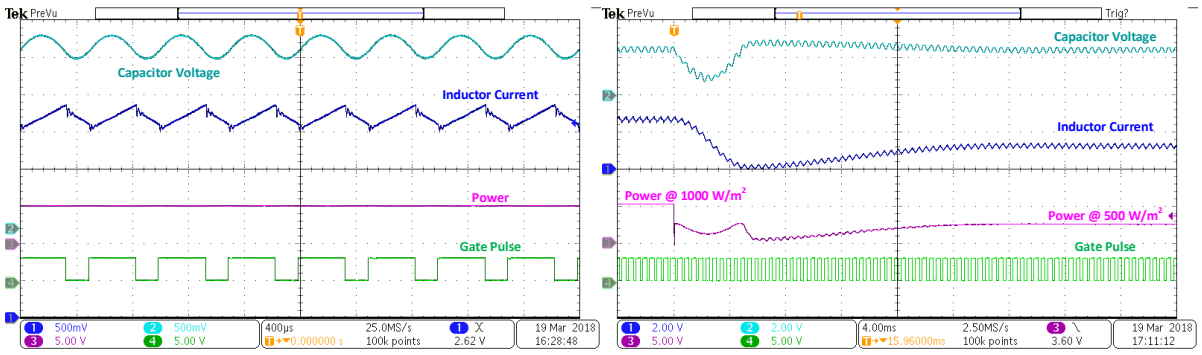
Figure 3.15 Steady-state response captured in RSCAD-runtime at irradiance 1000 W/m^2

The controller parameters derived in Section 3.5.2 are used to experimentally verify the steady-state and transient performance of the system. Figure 3.15 shows the plots for PV power, voltage and current in RSCAD runtime window. These plots are also monitored in oscilloscope and presented in Figure 3.17. A stable steady-state performance of the system can be observed from Figure 3.15 and Figure 3.17 (a). Similarly, stable performance of the system after transients are recorded in Figure 3.16 and Figure 3.17 (b).



(a) (b)

Figure 3.16 (a) Transient response of the system for irradiance change from 1000 W/m^2 to 500 W/m^2 (b) Change of operating point in P-V curve due to transient.



(a) (b)

Figure 3.17 Experimental results (a) Steady-state and (b) Transient, Ch. 1 (5 V corresponds to 26.6 A), Ch. 2 (5 V corresponds to 368.33 V), Ch. 3 (5 V corresponds to 2.597 kW)

To validate the small-signal model of the power stage and voltage controller loop, a small-signal perturbation is introduced externally in the voltage reference (MPP voltage) using a GPA (Bode100) and the PV input voltage is monitored. Figure 3.18 shows the connection scheme along with indication of key variables measured. Since the MPPT controller block generates the reference inside the DSP, it is disabled to perform this test.

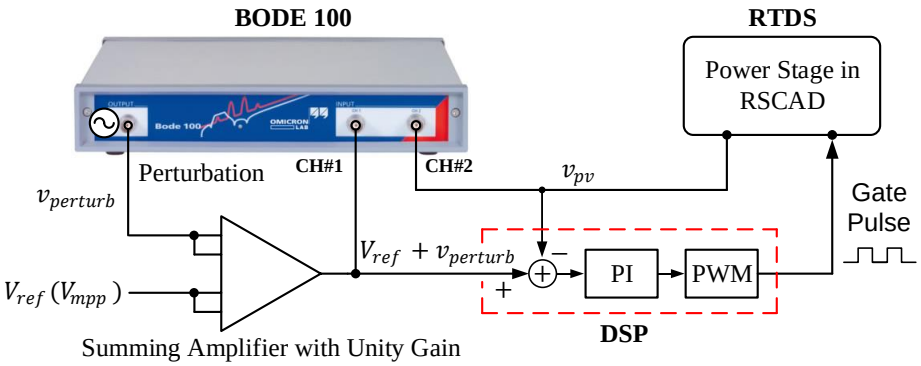


Figure 3.18 Connection scheme of Bode100 for frequency response evaluation.

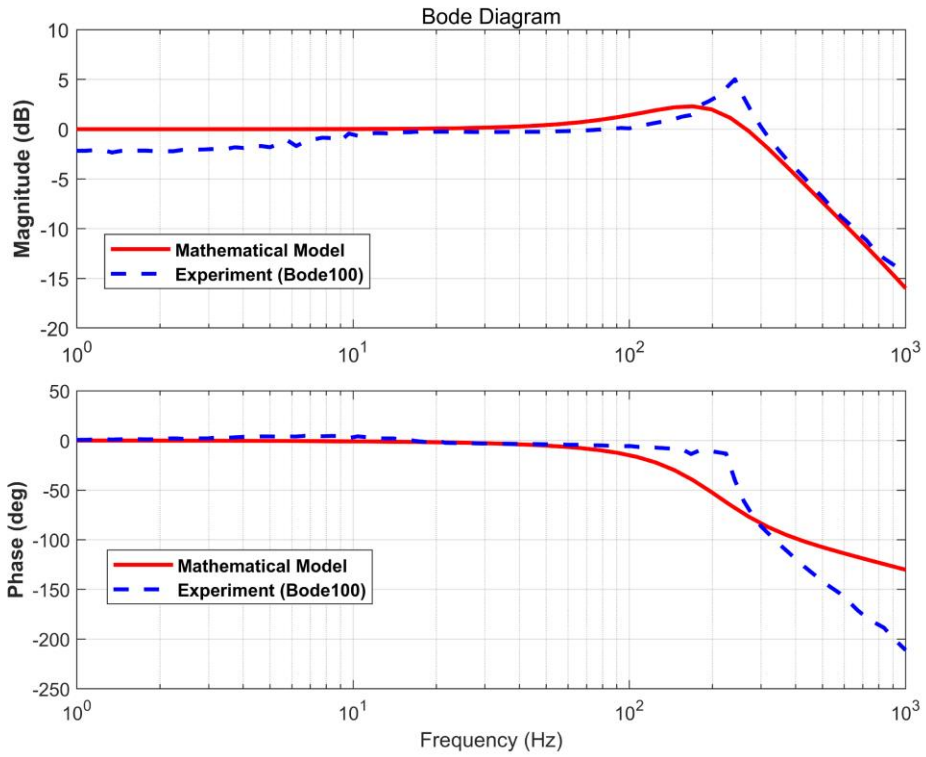


Figure 3.19 Comparison of closed loop frequency response of voltage controller from mathematical model, simulation and experiment.

The frequency response result obtained from GPA is superimposed with the frequency response of the developed mathematical model and is presented in Figure 3.19. It can be

observed that the experimental results closely follow the response of the mathematical model, especially in the low frequency region. It may be noted that the semiconductor switches in RSCAD are modelled as simple turn-on and turn-off resistances [81]. It is observed that the values of these resistances affect the frequency response of the system. Also, the fact that the developed model doesn't take into account the delays resulting from the time step, the phase plot of the experiment is deviated further from the model. This is a possible reason for the slight variations of the experimental results with that of the developed model. Therefore it is safe to report that this validates the modelling of all the key elements of the inner loop from Section 3.4 as well as the controller design.

3.7. Summary of Chapter 3

This chapter presented a comprehensive small-signal model describing the dynamic relationship between a PV source, boost converter, INC MPPT and a voltage controller. The frequency response of the system, determined using the developed small-signal TFs, is used to compute the controller parameters. A detailed analysis showing the performance of the system during various parameter changes are studied. The models are verified and validated through simulation, mathematical analysis as well as experimental results. The experiment is conducted with power stage in RTDS and control operations in DSP with CHIL. A GPA is used to measure the frequency response experimentally. This approach to verify the small signal model for DC PCS can provide a safe and practical testing environment to evaluate the dynamic response of a control system in actual control hardware. The mathematical model and controller design are supported by a good agreement of simulation with experimental results.

The work presented in this chapter detailed the performance of a PV panel along with the MPPT controller. To extend this analysis to evaluate a GCPI in a PHIL system, it is essential to understand the effect of DC PCS in the PHIL operation. In general, the dynamics of the PHIL system remains unaffected from the dynamics of the PV panel and its controller. This is because the voltage controller that controls DC bus in Figure 3.1 is designed to eliminate the double line frequency which limits the bandwidth of the controller around 10-20 Hz. [82], [83]. Due to the presence of this DC bus capacitor, most of the dynamics of the PV will be filtered out and therefore can be assumed to have nearly no effect on the PHIL evaluation of the PV inverter. Therefore the chapters following, Chapter 4 and Chapter 5, neglects the dynamic of PV panel to conduct PHIL studies.

Chapter 4

Stability of a PHIL System: A Quantitative Analysis

- *A Part of the work presented in this chapter is the result of original work published under* ***M. Pokharel*** *and C. N. M. Ho,* ***"Stability study of power hardware in the loop (PHIL)simulations with a real solar inverter," IECON 2017****, pp. 2701-2706, Beijing, 2017.*
- *A Part of the work in this chapter is also the result of original work accepted to be published under* ***M. Pokharel*** *and C. N. M. Ho,* ***"Stability Analysis of Power Hardware in the Loop (PHIL) Architecture with Solar Inverter," IEEE Transactions on Industrial Electronics (Early Access), 2020.***

The purpose of this work is to understand the stability problems of a PHIL system. In this chapter, the factors that affect the stability in a PHIL setup is analyzed along with the recommendations for interface device parameters. The quantitative analysis of the stability is performed with a Routh-Hurwitz (RH) table which forms the basis for mathematical formulations. Besides, in this chapter, the system stability is tested and verified experimentally by evaluating a grid-connected PV micro-inverter. The details of the work can be followed in the subsequent sections.

4.1. Introduction

The stability problem of PHIL simulations is discussed extensively in literatures [26] and [57]. There have been many other studies that focus on accuracy and stability improvement of HIL simulations [10], [30], [84]. However, PHIL being an emerging technology, research focused on generalizing the stability theory has been minimal and more investigation in this area is needed before the techniques with HIL can directly be employed. Similarly, the methods proposed by Ren, Steurer and Baldwin [26], Ren et al. [30], and Hong et al. [84] for stability analysis and accuracy improvements in PHIL are mostly case specific and provide the basis for analysis for a particular interfacing method. Another important factor in PHIL implementation is choosing the proper IA, as implementation with different IAs poses a unique challenge of stability and accuracy. The performance evaluation of various IAs is analyzed and well documented in [25]-[27], [29], [30], [85]-[87]. Among these studies made for stability analysis, it is common to define the stability criteria in terms of the impedance ratio of the simulation and hardware [25], [26], [57], [87]. Therefore, an estimate of output impedance is required to carry out these stability studies. As the measurement of actual impedance of the system under study is not always accurately obtained, this will have a significant impact on stability studies. Additionally, it is essential that other parameters that impact the PHIL be analyzed in detail to understand the stability issues. As illustrated in [30], the open loop TF of the PHIL can be one of the ways to analyze the system to understand the measure of the stability and parametric effects on stability.

The stability studies in the existing literatures have focused more on the graphical way of analyzing the PHIL system. If, instead a quantification of the stability could be done, the parameters of the interface that could result in a stable PHIL could be known. This would allow

the user to select the interface devices with a known specification. This opens an entirely new way of looking at the stability problem of a PHIL system.

4.2. System Modelling and Analysis

The advantages of PHIL approach for system evaluation and testing is discussed in Chapter 2 along with the review of literatures with significant contribution in the area. As suggested by these existing research articles, the IAs in PHIL play an important role in the stability and accuracy. Based on these studies it has been shown that ITM offers a good balance between accuracy and stability, and at the same time is simple for implementation. Therefore, this work follows the similar trend and models the PHIL with an ITM interface to further its analysis.

4.2.1 PHIL Architecture

A general test setup of a PHIL arrangement with an ITM interface for a resistor divider circuit is shown in Figure 4.1.

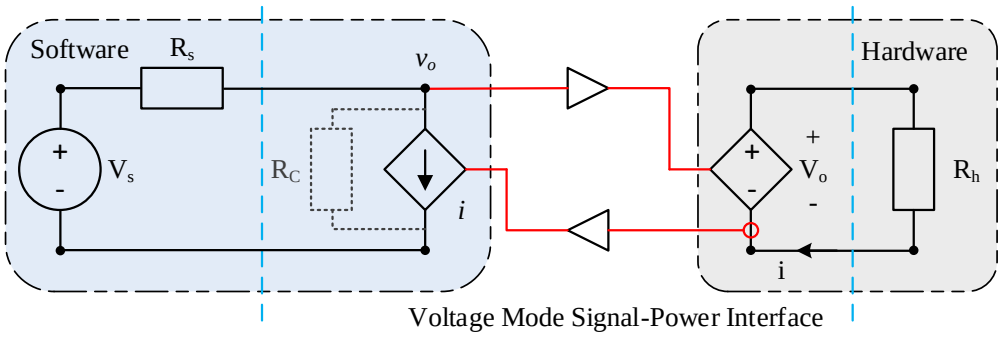


Figure 4.1 Resistor divider network in PHIL with ITM interface.

The ITM setup for a resistor divider consists of a resistor (R_s) sourced through a voltage-source (V_s) inside a Simulation Environment (SE) followed by an interface that connects it to the DUT (R_h). The interface includes a DAC card, a linear amplifier, current sensor and ADC card. The voltage from SE is fed out by DAC card in signal level which is then amplified to corresponding power level voltage. The current from the hardware is sensed and fed-back into SE through ADC card.

An additional resistor R_C has been integrated with the controlled current source and the interface is modified accordingly, Figure 4.1. This resistor is needed for the entirety of the interface modelling as an actual PHIL system includes this parallel resistor, and it is vital that it is incorporated in the system model to understand its effect on system performance. This work considers this current source resistor and accordingly presents the mathematical basis for analysis. The implementation diagram for a modified ITA used in this chapter is shown in Figure 4.1.

4.2.2 Interface Modelling

Each interface devices for PHIL in ITM can be modelled with their respective TF and delays [26], [36], [57], [84]-[87]. Since the interface bridges the SE with the real system, delay within the digital computation and time for ADC and DAC is of utmost importance in determining system performance. Additionally, the amplifier and sensor response cannot be overlooked if the overall system stability is to be studied. Taking these considerations, the system in Figure 4.1 can be represented in terms of control block consisting of TFs of each component. Figure 4.2 shows the control block equivalent of system in Figure 4.1 with important components and nodes labelled.

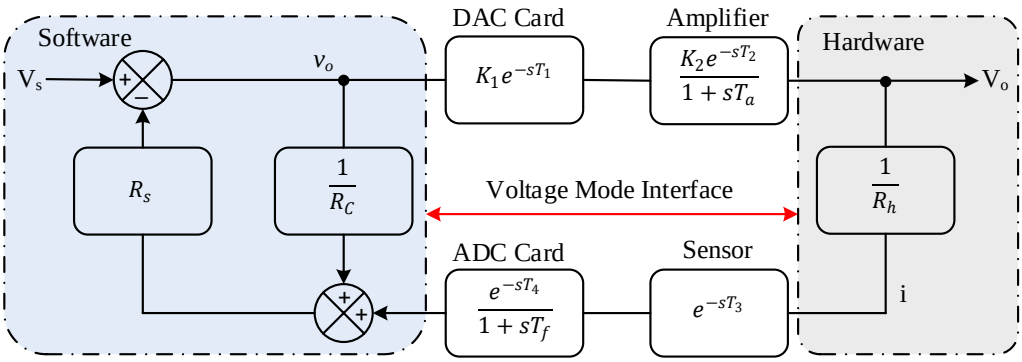


Figure 4.2 Control block representation of a resistor divider network in PHIL.

The open loop TF of the system with resistor divider can be derived using the control block in Figure 4.2 and is given by (4.1).

$$G_{OL}(s) = \frac{V_o(s)}{V_s(s)} = \frac{R_s}{R_C} + G(s) \cdot H(s) \cdot \frac{R_s}{R_h} \tag{4.1}$$

where, R_s, R_C and R_h are the software, current source and hardware resistances respectively and, $G(s)$ and $H(s)$ are the TFs of forward path and feedback path respectively. $G(s)$ contains the TF for AO card and amplifier. Similarly, $H(s)$ contains the TF for AI card and sensor delay. Expression for $G(s)$ and $H(s)$ is given by (4.2) and (4.3) respectively.

$$G(s) = K_1 \cdot K_2 \cdot \frac{e^{-s(T_1+T_2)}}{1+sT_a} \tag{4.2}$$

$$H(s) = \frac{e^{-s(T_3+T_4)}}{1+sT_f} \tag{4.3}$$

where, K_1 is the software gain, K_2 is the amplifier gain, T_1 and T_4 are the time-step delay, T_2 is amplifier response time, T_3 is the sensor delay, T_a is the cut-off of amplifier and T_f the anti-aliasing filter cut-off of AI card.

The open loop TF of the system can be used to analyze the effect of current source resistance on the accuracy. It is also important to note that, delay exponentials in (4.2) and (4.3) are not always easy to deal using a standard bode-based frequency response approach.

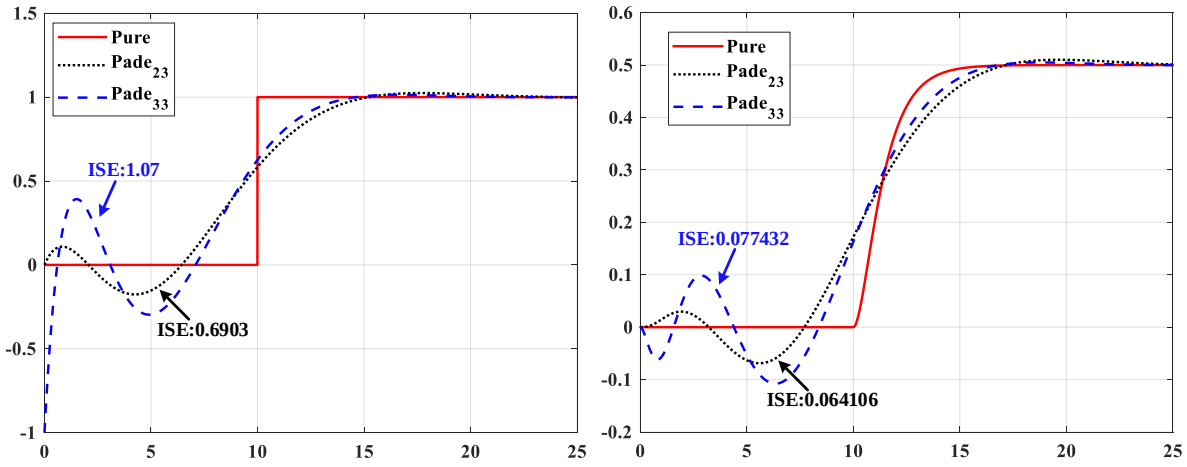
To overcome this problem, the subsequent section presents the approximation of delay using polynomial along with its accuracy quantified.

4.2.3 Approximate Delay Model

There are various graphical and mathematical tools to analyze delays. However, the challenge remains for representing the system with delays using TF by suitable rational function. Considering this, Taylor series and PD are widely accepted as the mathematical tool to approximate pure delays by their respective numerator and denominator polynomials. This allows the use of classical control techniques to analyze the system. Moreover, the approximation is governed by the accuracy of the model.

The comparison between Taylor and PD model for delays presented in [35] shows that Taylor approximations for delays has several disadvantages in terms of physical realizability, unstable zeros and unstable for higher order polynomials. Conversely PD offers a considerable flexibility in terms of the degree of polynomials in numerator and denominator and are accurate if the order of numerator is less than that of denominator. Also as discussed in Chapter 2, an improved accuracy for PD is obtained when the order of numerator is one less than the denominator [34]. To validate this, a comparison is made in this paper based on the measure of Integral Square Error (ISE) of PD for equal numerator and denominator order, and PD with one less order in numerator than denominator. A comparison of step responses of Third Order Denominator-Third Order Numerator (TDTN) PD and Third Order Denominator-Second Order Numerator (TDSN) PD with its pure delay counterpart is shown in Figure 4.3 (a). Similarly, Figure 4.3 (b) presents the step response comparison of second order system with pure delay with TDTN PD and TDSN PD. In Figure 4.3, a TDTN, TDSN and a pure delay

system is denoted as *Pade*$_{33}$, *Pade*$_{23}$ and *Pure* respectively. In both the cases ISE for TDSN is lower than TDTN. This is due to the fact that TDTN system experiences a negative jump at the start, otherwise is fairly accurate.



(a) (b)

Figure 4.3 Step response of PD for (a) Pure delay & (b) Second order TF with Pure delay.

Based on the observation from Figure 4.3, delays can be modelled with PD having one less order in numerator than denominator. For the case of this analysis, a TDSN PD represented by (4.4) is considered, as there is relatively low improvement in the accuracy by going higher orders.

$$PD_{23}(e^{-sT_d}) \approx \frac{60-24\cdot sT_d+3\cdot(sT_d)^2}{60+36\cdot sT_d+9\cdot(sT_d)^2+(sT_d)^3} \tag{4.4}$$

After approximating the exponential delay function by polynomials, the accuracy of interface with respect to current source resistance can be estimated using (4.1), (4.2), (4.3) and (4.4) for the system parameters presented in Table 4.1. The parameter T_d represents the lumped delay of the overall loop in Figure 4.2.

Table 4.1 Interface parameters.

Parameter	K_1	K_2	T_d	T_a	T_f
Value	1/20	20	100 µs	0.4 µs	15.75 µs

For the purpose of accuracy evaluation, frequency response of (4.1) when $R_C \to \infty$ is compared with finite values of R_C. This is done to achieve an ideal like characteristic as setting value of R_C much higher than R_s would result in the term R_s/R_C to be negligible and (4.1) would yield to an ideal current source model. Additionally, this approach allows to choose the value of R_C based on R_s. To be able to compute the accuracy of this approach, ISE is used to quantify and judge the accuracy limit for varying values of R_s dependent R_C.

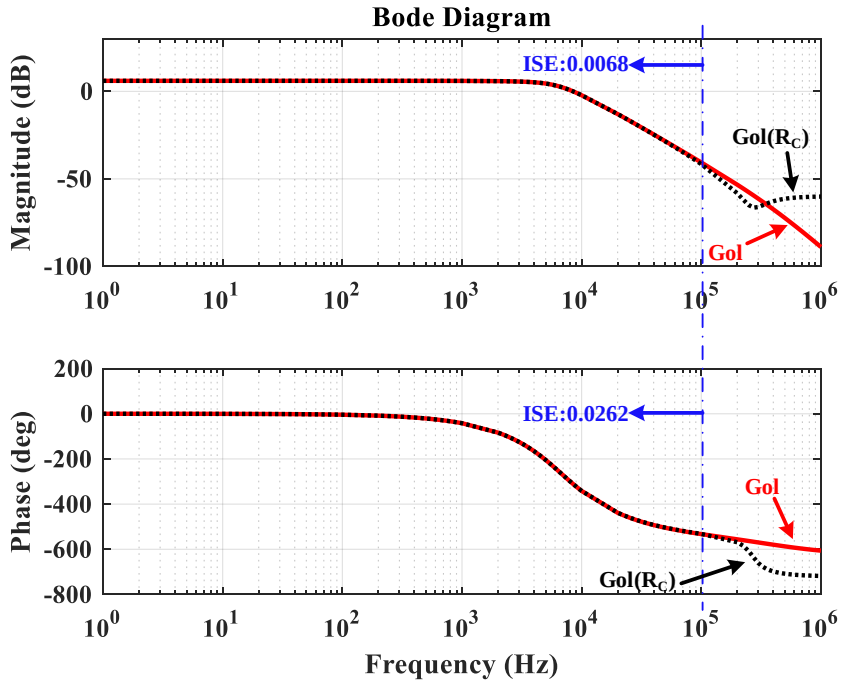


Figure 4.4 Accuracy evaluation of interface with current source resistor.

The frequency response presented in Figure 4.4 compares a plot of $Gol(R_C)$ when $R_C = 1000 \cdot R_s$ with $R_C \to \infty$. The ISE of the frequency response of the plot for finite R_C is recorded to check the accuracy until a frequency range of 100 kHz. For the purpose of this study, it is a reasonable frequency range to estimate the accuracy considering the fact that cut-off frequency of anti-aliasing filter in AI card is limited to 84.2 kHz. The effect of current source resistor can basically be neglected for the choice of current source resistor, $R_C = 1000 \cdot R_s$, for the frequency range of interest. To further show the variation in accuracy with changing R_C, ISE for various values of R_C is recorded and presented in Table 4.2. One important conclusion that can be drawn from Table 4.2 is, the value of R_C lower than 100 times R_s results in a very high error and therefore should be avoided, while choosing values higher than 1000 times is merely the accuracy requirement of the user.

Table 4.2 ISE comparisons for varying value of R_C.

Value of R_C	**Accuracy Index**	
	ISE (Mag.)	**ISE (Phase)**
$R_C = R_s$	31.872	715.3529
$R_C = 10 \cdot R_s$	4.1016	572.098
$R_C = 100 \cdot R_s$	1.7087	34.8617
$R_C = 1000 \cdot R_s$	0.0068	0.0262
$R_C = 10000 \cdot R_s$	6.3599e-5	2.3862e-4

4.3. Development of Stability Equations

Rightly choosing the interface method for PHIL does not entirely guarantee the stability of the system. The interface consists of an unavoidable delay from the fiber cables, I/O cards, sensors, conditioning circuits, filters and the amplifiers. In-detail investigation of this interface delay along with other parameters in the interface is therefore required if the stability of the system is to be understood. To study the stability of PHIL with resistor divider network, interface device models described in Section 4.2.2 and Section 4.2.3 serves a basis for further mathematical formulation. Considering the selection of current source resistor so as to have a minimal effect in accuracy within the frequency range of interest, (4.1) can be represented as;

$$G_{OL}(s) = G(s) \cdot H(s) \cdot \frac{R_s}{R_h} \tag{4.5}$$

Once the open loop transfer function of the system in Figure 4.2 is known, stability can be easily studied by treating it as a standard control block. Equation (4.6) describing the characteristics equation can therefore be used to quantify the stability.

$$1 + G_{OL}(\mathrm{s}) = 0 \tag{4.6}$$

$$(1 + sT_a) \cdot \left(1 + sT_f\right) + K_1 \cdot K_2 \cdot \mathrm{e}^{-\mathrm{s}T_d} \cdot \frac{R_s}{R_h} = 0 \tag{4.7}$$

Substituting (4.4) in (4.7) and considering parameters described in Table 4.1, K_1 and K_2 would cancel out each other and the overall equation would resolve to a 5th order polynomial of the form (4.8).

$$\mathcal{F}(s) = a \cdot s^5 + b \cdot s^4 + c \cdot s^3 + d \cdot s^2 + e \cdot s + f = 0 \tag{4.8}$$

Where,

$$a = T_a \cdot {T_d}^3 \cdot T_f$$

$$b = (T_a + T_f) \cdot {T_d}^3 + 9 \cdot T_a \cdot T_f \cdot {T_d}^2$$

$$c = \left(9 \cdot T_a + 9 \cdot T_f + T_d\right) \cdot {T_d}^2 + 36 \cdot T_a \cdot T_d \cdot T_f$$

$$d = 36 \cdot \left(T_a + T_f\right) \cdot T_d + 3 \cdot \left(3 + \frac{R_s}{R_h}\right) \cdot {T_d}^2 + 60 \cdot T_a \cdot T_f$$

$$e = 60 \cdot \left(T_a + T_f\right) + 12 \cdot \left(3 - 2 \cdot \frac{R_s}{R_h}\right) \cdot T_d$$

$$f = 60 \cdot \left(1 + \frac{R_s}{R_h}\right)$$

4.3.1 Necessary but Not Sufficient Condition

From the characteristic equation described by (4.8), it is evident that system would be unstable if following two conditions are met;

i) If there is any missing term in the characteristic's equation; Equation (4.8) shows all the coefficients finite, hence not unstable.

ii) If there is any sign change in the coefficients; All the coefficients are positive except for e, which might turn up negative with changing ratios of R_s/R_h. This needs to be ensured positive before investigating stability.

Therefore, necessary condition for stability is governed by the positive value of coefficient e which yields (4.9).

$$\frac{R_s}{R_h} < \frac{60 \cdot \left(T_a + T_f\right) + 36 \cdot T_d}{24 \cdot T_d} \tag{4.9}$$

Equation (4.9) describes the necessary condition for stability in terms of amplifier bandwidth and interface delays but most importantly the boundary of instability for a chosen software-hardware resistor. To have the quantitative measure of stability, RH criteria serves the sufficient condition.

4.3.2 Formulation of Stability Criteria

If, in characteristics equation, there are no missing terms and all the coefficient have the same sign does not guarantee the stable system. For stability, RH table is constructed, and any sign change in the first column is looked for. The first column of RH table for (4.8) is tabulated in Table 4.3. With the criteria from Table 4.3, the stability of the system under test can be ensured beforehand.

Table 4.3 Stability criteria with RH table.

For $a > 0$	$X = bc - ad > 0$	$Y = be - af > 0$	$Z = (dX - bY)Y - X^2 f > 0$	f

Considering the system in Table 4.1, for a linear amplifier, T_a is much smaller than T_f and T_d, and therefore would have a minimal contribution in coefficient b,c,d and e. With this modification, the updated coefficients of (4.8) may be rewritten and expressed as in (4.10).

$$\left.\begin{aligned} b &= T_f \cdot {T_d}^3 \\ c &= {T_d}^2 \cdot (9 \cdot T_f + T_d) \\ d &= 36 \cdot T_f \cdot T_d + 3 \cdot \left(3 + \frac{R_s}{h}\right) \cdot {T_d}^2 \\ e &= 60 \cdot T_f + 12 \cdot \left(3 - 2 \cdot \frac{R_s}{R_h}\right) \cdot T_d \end{aligned}\right\} \tag{4.10}$$

The stability criteria in Table 4.3 can be analyzed with updated coefficients to observe the effect of time delay to determine the stable range of R_s/R_h. But first, (4.9) can be revisited with above assumptions and can be revised as;

$$\frac{R_s}{R_h} < \frac{5 \cdot T_f + 3 \cdot T_d}{2 \cdot T_d} \tag{4.11}$$

The criteria stated in Table 4.3 along with updated coefficients form the mathematical basis to analyze the stability. By subsequently plugging (4.10) in criteria of Table 4.3, stability

equations can be simplified to analyze the effects of interface parameters in stability. With this, the following inequalities can be tested to find the stability boundary.

Ineq.1: Cond.1: $\boldsymbol{X > 0; X = bc - ad}$

$$\text{Cond. } 1 \rightarrow \frac{T_d + 9 \cdot T_f}{3 \cdot T_a} - \frac{3 \cdot (T_d + 4 \cdot T_f)}{T_d} > \frac{R_s}{R_h} \tag{4.12}$$

Ineq.2: Cond.2: $\boldsymbol{Y > 0; Y = be - af}$

$$\text{Cond. } 2 \rightarrow \frac{5 \cdot T_f + 3 \cdot T_d}{2 \cdot T_d} > \frac{R_s}{R_h} \tag{4.13}$$

Ineq.3: Cond.3: $\boldsymbol{Z > 0; Z = (dX - bY)Y - X^2 f}$

$$\text{Cond. } 3 \rightarrow \textit{Graphical determination}$$

4.3.3 Investigating Stability

The analytical equations governing the stability is a set of three multivariate inequalities given by *Cond.1*, *Cond.2* and *Cond.3*. These multivariate inequalities would yield infinite number of solutions without imposing any constraints in the variables. Hence it becomes computationally cumbersome to determine the solution analytically. Rather a better approach would be to compare each condition graphically to determine the operating boundary for a specified constraint in variables. The methodology of sequence follows as; first, an operating range of T_d is chosen for a given T_f, and with varying T_a the Left-Hand Side (LHS) of the inequality (4.12) is determined and compared with the ratio R_s/R_h to conform the criteria described by *Cond.1*. After identifying the operating region governed by *Cond.1*, LHS of inequality (4.13) is checked for *Cond.2* in a similar manner followed by which inequality in *Cond.3* is also evaluated. To be able to properly understand the effect of each parameters

describing stability criteria, each condition is individually represented in a graphical plane showing their operating boundary.

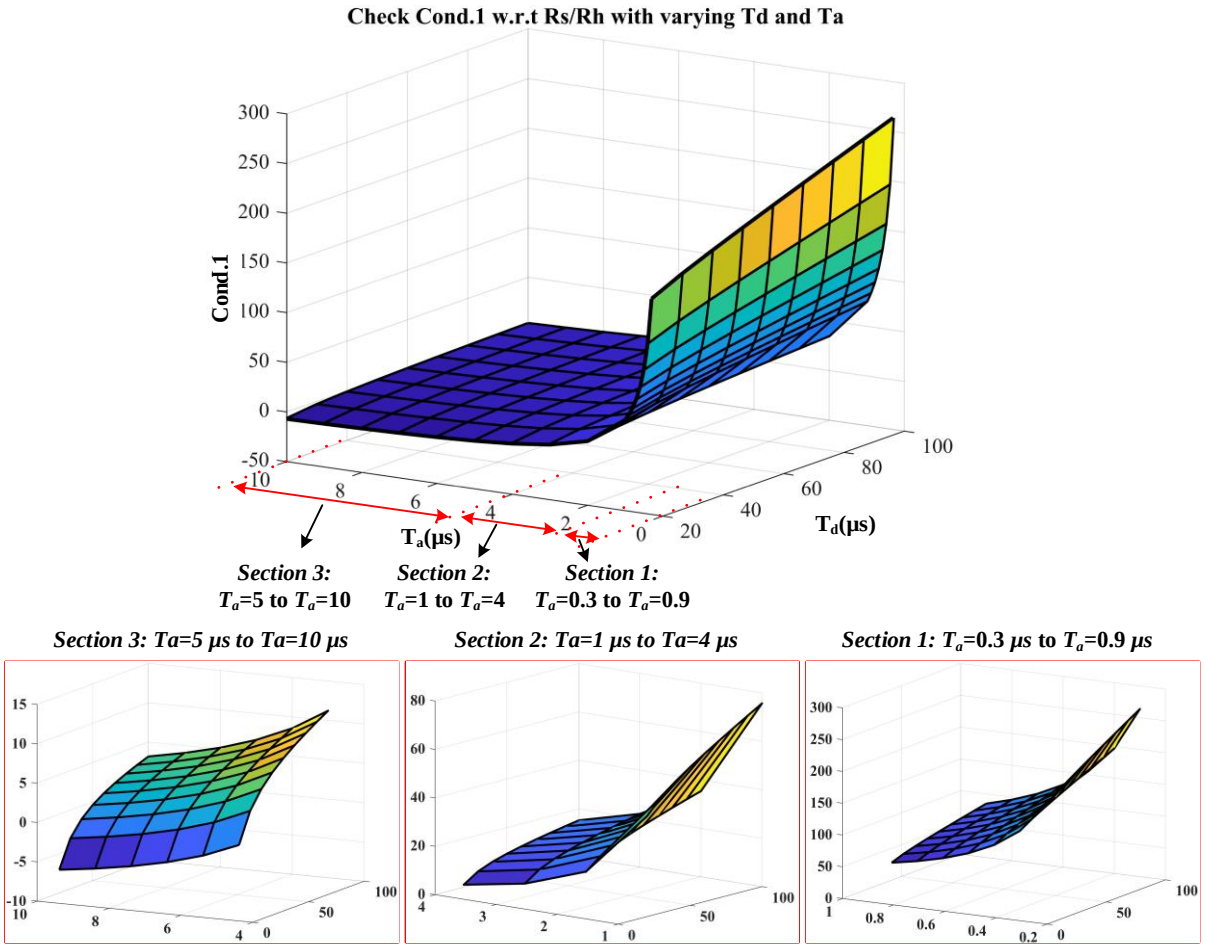


Figure 4.5 Graphical representation of *Cond.1* for varying T_d and T_a.

The plot of *Cond.1* is generated for a T_f specified in Table 4.1 by varying T_d and T_a. The 3-dimensional variation of LHS of inequality in (4.12) is shown in Figure 4.5. This serves as a graphical tool to choose the ratio R_s/R_h such that it is always less than the value of *Cond.1* (Z-axis) in Figure 4.5 so as to satisfy the inequality (4.12). Basically, the plot in Figure 4.5 sets a boundary above which the system would be unstable for a defined range of parameters. This

sets a tone for going forward and evaluating remaining two conditions to be able to judge the stable operating region.

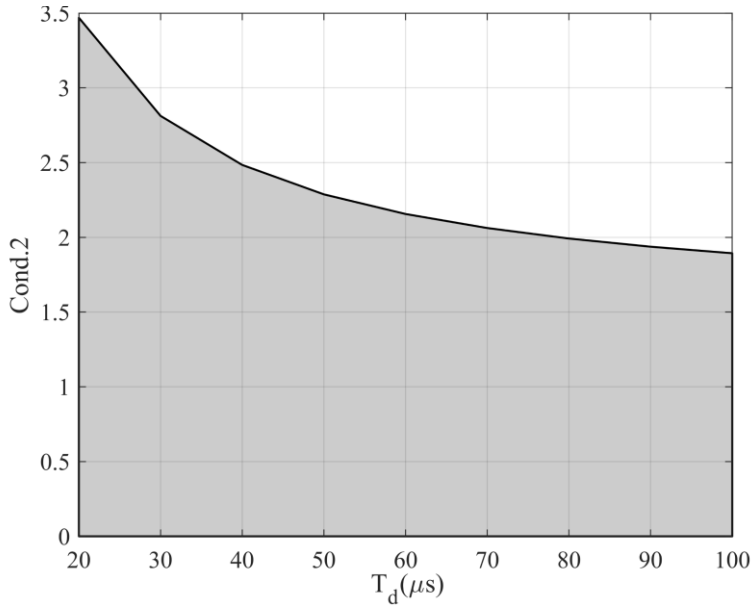


Figure 4.6 Area under the plot showing region satisfying *Cond.2*.

The inequality in *Cond.2* can be represented graphically in a manner similar to *Cond.1* for a given T_f. This leads the LHS of inequality in (4.13) dependent only on the delay time T_d. A plot of the LHS of (4.13) for varying T_d is shown in Figure 4.6 for a T_f specified in Table 4.1. The shaded region in the plot shows the region under which the ratio R_s/R_h must remain in order to satisfy the stability inequality stated by *Cond.2*. With *Cond.1* and *Cond.2* both satisfied to find the operating boundary of resistances ratio, it is further necessary to proceed with examining *Cond.3* to completely show the stable operating boundary of the system under study.

The inequality stated to check *Cond.3*, unlike other two conditions, is a high order polynomial; at least a square of sixth order on initial examination resulting due to the term X^2.

Further simplification to independently collect the ratio R_s/R_h becomes intensive and instead the expression Z can be directly evaluated as it is, for the specified range of parameters and stability check can be made with respect to the positive value of Z. To evaluate the inequality relating *Cond.3*, a series of operating conditions for varying T_d for a given T_a and T_f is chosen. Consequently, for a chosen range of resistance ratio bounded by *Cond.1* and *Cond.2* the variation in Z value is studied. The plot of Z against varying T_d and R_s/R_h ratio is shown in Figure 4.7 and the resultant plot is compared with $Z = 0$ plane to check for the inequality governing *Cond.3*. Once all three conditions for a given operating point is satisfied, the system under test should ensure stable operation.

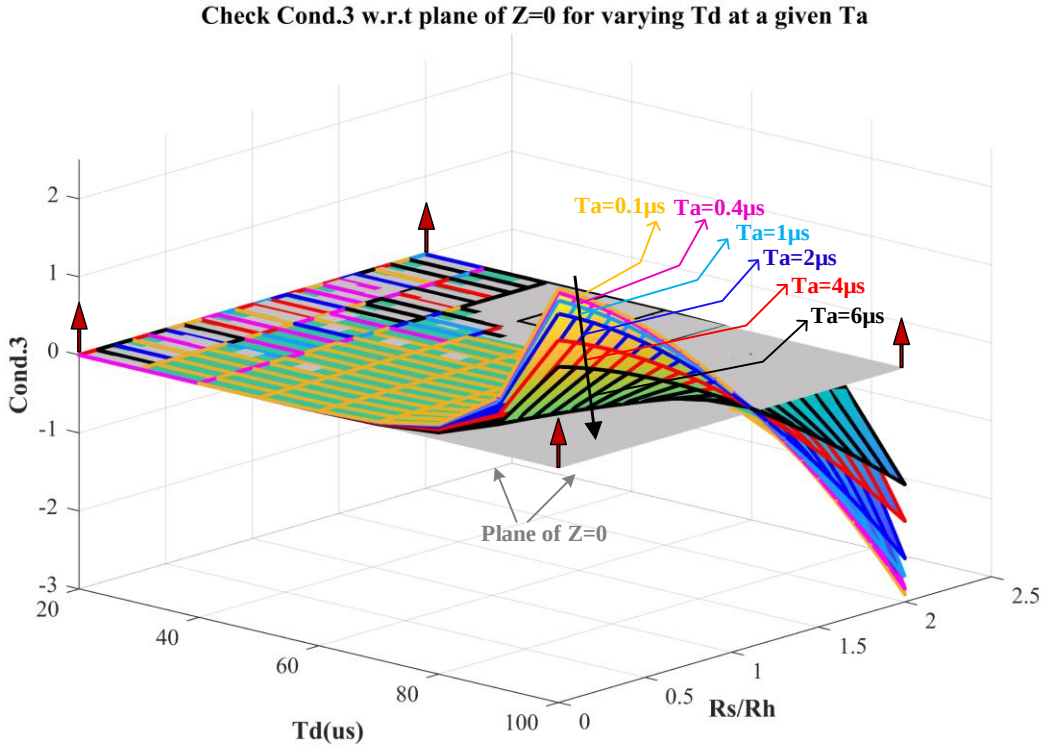


Figure 4.7 Plot showing the plane of stable operating region for varying T_d and resistance ratio.

4.4. Verifying the Stability

There are variety of tools widely employed to design a control system as well as to examine its stability. Among these tools, the graphical methods like Bode and Nyquist plot are preferred to evaluate the controller of a practical system as these methods can be directly applied to experimentally obtained frequency response of an actual hardware. Additionally, for a non-minimum phase system like the system consisting of delays and right half plane zeros, the usual controller design approach with bode using gain and phase margins becomes insufficient as these systems introduce extra phase lag for the same attenuation. However, Nyquist plot overcomes this shortcoming and comes in handy to completely evaluate the performance parameters of a non-minimum phase system as well. Therefore, in this work Nyquist plot is used to make initial verification of the stability criteria derived in Section 4.3. Further, additional experimental results to support this verification is presented considering a resistor divider network as well as a grid connected PV inverter.

4.4.1 A Resistor Divider Network

A system of resistor divider network with two combinations of R_s and R_h is chosen to verify the stability test. Nyquist plot is used to test stability graphically for $R_s > R_h$ and $R_s = R_h$, and is shown in Figure 4.8. The plot is based on the open loop transfer function in (4.5) and the rest of parameters are chosen from Table 4.1. The system with $R_s > R_h$ shows an unstable characteristic as compared with $R_s = R_h$ which shows a stable characteristic. With this method it is difficult to quantify the stability margins and therefore we settle for absolute stability for verifications.

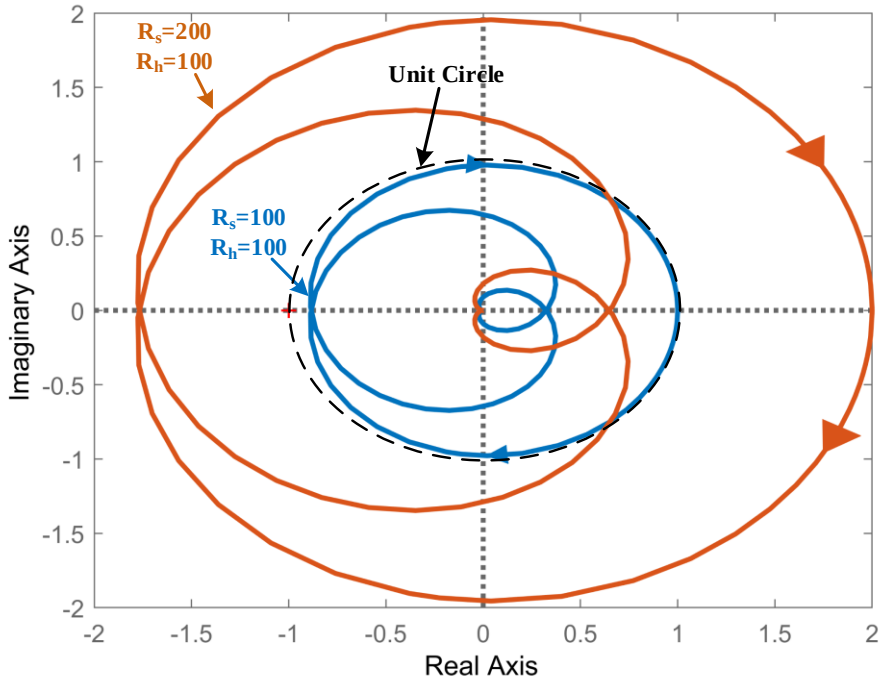


Figure 4.8 Nyquist stability test for a system of resistor divider.

To put the stability equations derived in Section 4.3 to test, similar parameters to that of Nyquist plot is required. Each condition is checked methodically in the graphs Figure 4.5 through Figure 4.7.With the parameter from Table 4.1, *Cond.1* lies in section-1 of the plot in Figure 4.5 with corresponding value approximated to 200 (196.6 being the actual value). From (4.12) it is obvious that the ratio R_s/R_h must be lower than this value to ensure stability. However, *Cond.2* overrides *Cond.1* by setting $R_s/R_h < 1.894$ (obtained from Figure 4.6). Moreover, to completely guarantee stability, *Cond.3* needs to be satisfied as well. From Figure 4.7, for specified parameters, $R_s/R_h < 1.1$ guarantees the stability. Similar observations are also seen from Figure 4.8 when $R_s/R_h = 1$ and $R_s/R_h = 2$.

4.4.2 A Grid Connected PV Inverter

The stability investigation methodology developed in the previous sections is further used to evaluate the stability of a grid connected PV inverter in PHIL configuration. To be able to directly apply the criteria developed in Section 4.3, the output impedance of a PV inverter needs to be estimated. For this, an impedance analyzer is configured as shown in Figure 4.9 (a) which measures the response in inverter current as the grid voltage changes. With these two measurements of grid voltage and inverter current the output impedance of the inverter in Figure 4.9 (b) can be determined experimentally. The labels ($\widetilde{V_p}$) and ($\widetilde{i_r}$) in Figure 4.9 represents the grid voltage perturbation and corresponding inverter current response respectively.

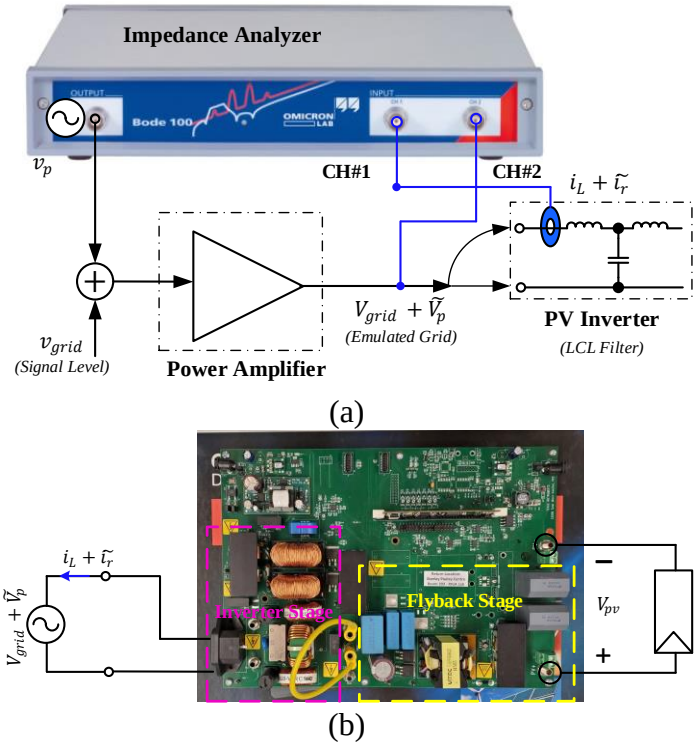


Figure 4.9 Output impedance measurement of a micro inverter (a) testing setup (b) inverter connection scheme.

The impedance characteristic of an inverter can be examined to determine the output impedance at the frequency of interest, in this case being the line frequency. The experimental result obtained from the impedance analyzer is presented in Figure 4.10 which records the impedance of 124.4 Ω at 60 Hz with a phase of 1.7 deg. Once the output impedance of the PV inverter is known, similar analysis to that for the resistor divider case can be made to predict the stable operating conditions for a micro inverter connected to the grid.

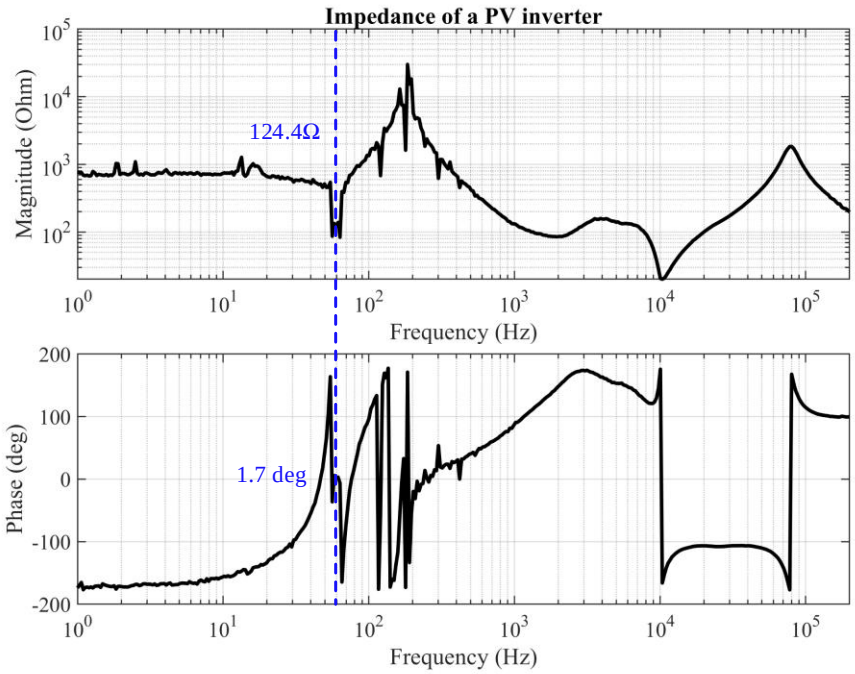


Figure 4.10 Experimental determination of output impedance of an inverter.

4.5. Experimental Evaluation with PHIL

The major challenge while implementing the PHIL, be it a simple network with resistors or with interconnected switching regulators, is to make the loop stable. Therefore, it is important to understand the performance of a PHIL with a network of resistor divider first.

4.5.1 A Resistor Divider Network

The PHIL implementation equivalent of a resistor divider network is shown in Figure 4.11. Resistances R_s and R_h form the voltage divider with the source voltage V_s in the software environment. The power amplifier is required to reflect the voltage drop across the hardware resistor. The combination of current sensor (current feedback) and voltage amplifier completes the PHIL arrangement with ITM interface.

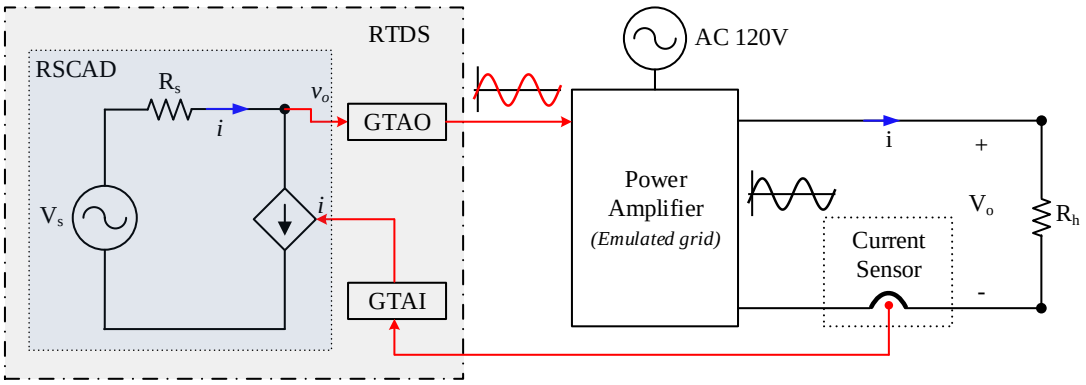


Figure 4.11 PHIL Implementation with resistor divider network.

The implementation of a resistor divider network with PHIL requires a digital low pass filter in RTDS to eliminate the noise associated with analogue to digital conversion. However, this comes at an expense of additional lag to the already present time step lag into the fed current signal. At the same time, it is also evident that a low pass filter would increase the stability margin due to the presence of a left half plane pole. Therefore, to take full advantage of the integrated current filter, a compensator can be designed such that any lag associated with the filter can be compensated. Figure 4.12 shows the bode plot of a low pass filter with crossover at 1 kHz and the required characteristics of the compensator superimposed along with the response of their combinations.

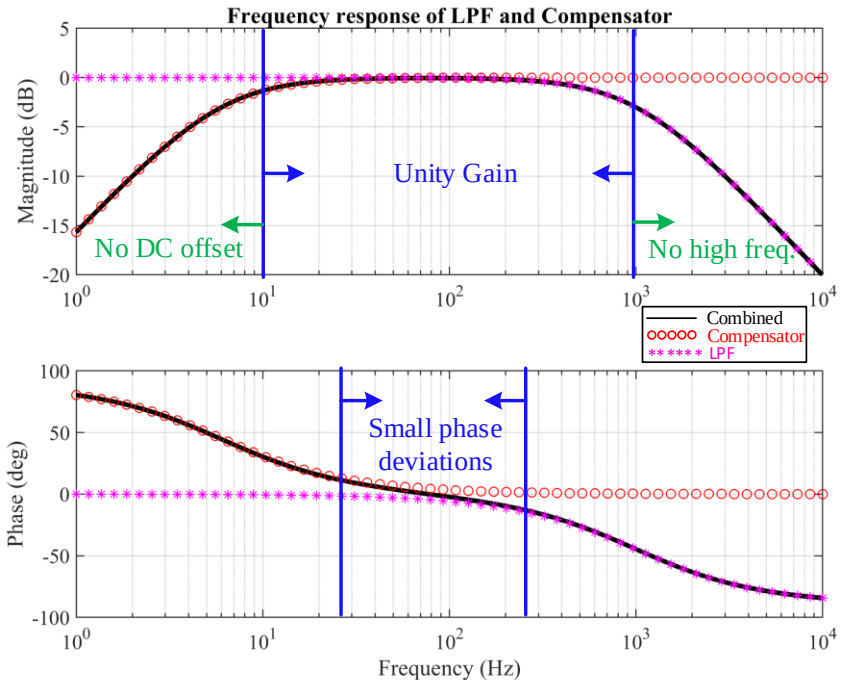


Figure 4.12 Compensator design to eliminate the delay due to filter.

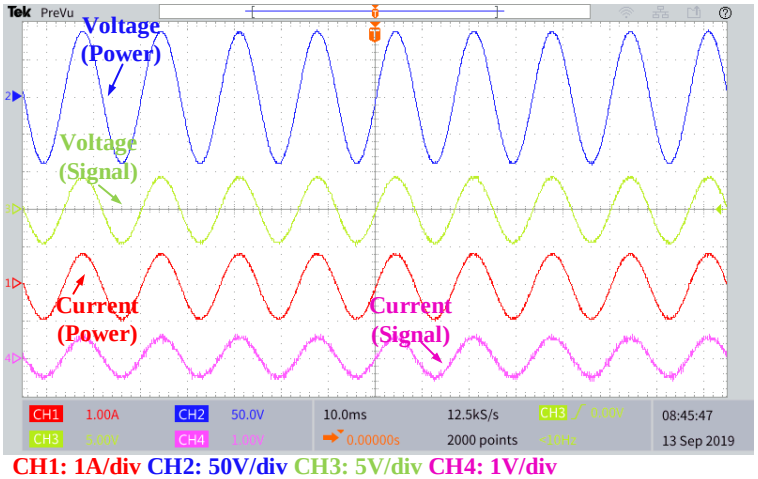
From Figure 4.12 the advantage of employing a compensator can be clearly understood. At low frequency, the gain of the filter-compensator combination is low such that it helps eliminate any unwanted DC gain in the loop and at the same time it preserves the low pass nature at frequency above 1 kHz. Another advantage of such compensator is, it can be designed to improve the phase lag due to low pass filter at a frequency of interest. With this knowledge the compensator and filter transfer functions can be expressed as;

$$G_{LPF} = \frac{1}{1+s \cdot T_{lpf}} \tag{4.14}$$

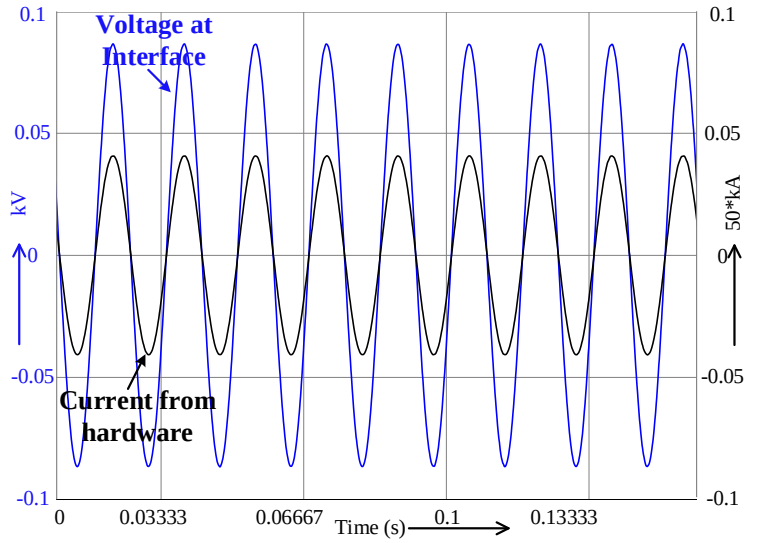
$$G_{Comp} = \frac{s \cdot T_{comp}}{1+s \cdot T_{comp}} \tag{4.15}$$

Employing the compensator and filter given by (4.14) and (4.15) in RTDS to the PHIL implementation for $R_s = R_h = 100\,\Omega$, a stable operation of resistor divider network is obtained as predicted by the stability criteria. The experimental result for stable operation of

resistor divider network is shown in Figure 4.13. The result presented in Figure 4.13 (a) is the measurement made at the physical hardware and Figure 4.13 (b) shows the corresponding voltage and current measurements inside the software environment.



(a)



(b)

Figure 4.13 Resistor divider measurement (R_s/R_h=1) at (a) hardware node (b) software node.

With only the filter present, the current in Figure 4.13 (b) would have a small DC offset as well as a lagging phase with respective to the voltage. To prove the operation of the

compensator as described in Figure 4.12, an experiment is run and the measurements of voltage at interface as well as currents with and without the compensator are made. From the result presented in Figure 4.14, it is clearly seen that the current without the compensator has a phase lag with respective to the voltage while the compensator employed current and voltage are in phase with an insignificant error. This error can be quantified using the reactive power measurements at both hardware and software end. This is because for a system with resistors, ideally, there should be zero reactive power exchange. Due to the phase shift between voltages and currents as a result of PHIL delays, a reactive power exchange may be seen which can be measured to estimate the errors. For a compensator employed system with $R_s = R_h = 100\ \Omega$, a Yokogawa power analyzer is used to measure the reactive power physically and also reactive power measurement is made at the software end. The combined hardware and software reactive power measurements directly correspond to the error in PHIL. The measurement showed a total error of 2.243% out of which hardware and software error is recorded at 0.214% and 2.028% respectively. With this, it is valid to say that the errors will be much larger for system without the compensator.

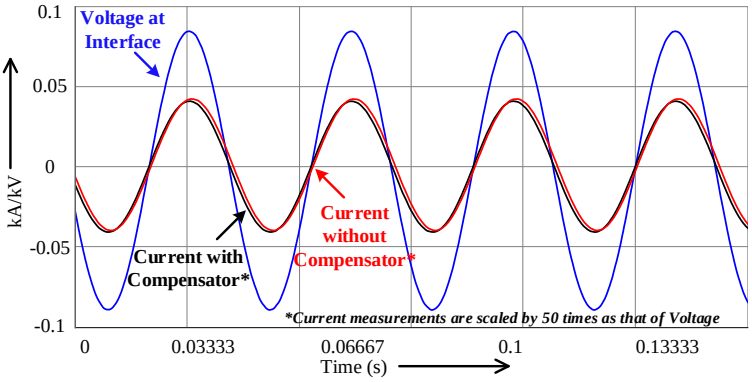


Figure 4.14 Comparison of results with and without employing the compensator.

Further to examine the stability margin, the ratio R_s/R_h is increased until the oscillation in the system is observed. This should be enough to give an idea about the operation boundary. As analyzed in Section 4.4.1, the system should show unstable operation when the ratio R_s/R_h increases beyond 1.1. Various experiments were performed by changing the software resistance. The system showed stable operation until $R_s/R_h < 1.48$ which is higher than the theoretical prediction. This is expected due to the fact that theoretical analysis considers the stability margin for a system without additional pole from low pass filter. However, it still gives a fair estimate of the stability operation which can be employed during system specification before performing the PHIL evaluation. The experimental result showing the operation of a resistor divider network when resistances ratio changes from 1.45 to 1.49 is presented in Figure 4.15. The oscillation recorded shows the system operating in a margin of instability and hence no further increment in source resistance was made.

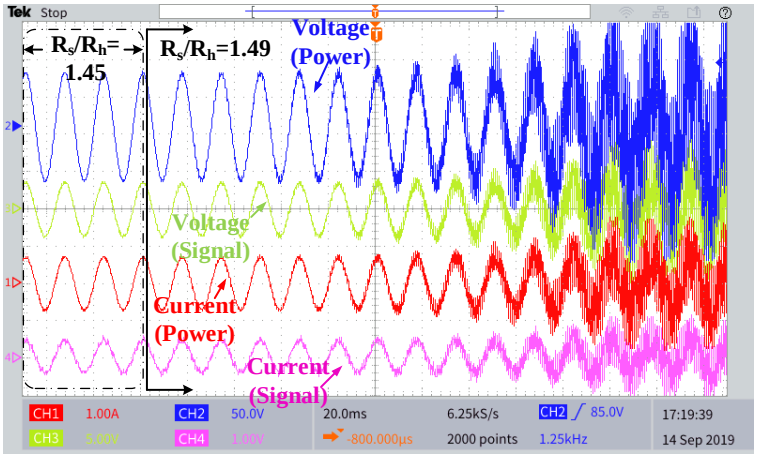


Figure 4.15 Measurements for varying R_s/R_h.

4.5.2 PHIL with a Grid Connected PV Inverter

Once the system of PHIL with resistor divider is analyzed and implemented, it can be directly extended to evaluate a grid connected PV inverter. The schematic for a grid connected PV inverter under PHIL arrangement is shown in Figure 4.16 with all measurement points marked. The measurements are made at the hardware as well as at the software runtime environment simultaneously.

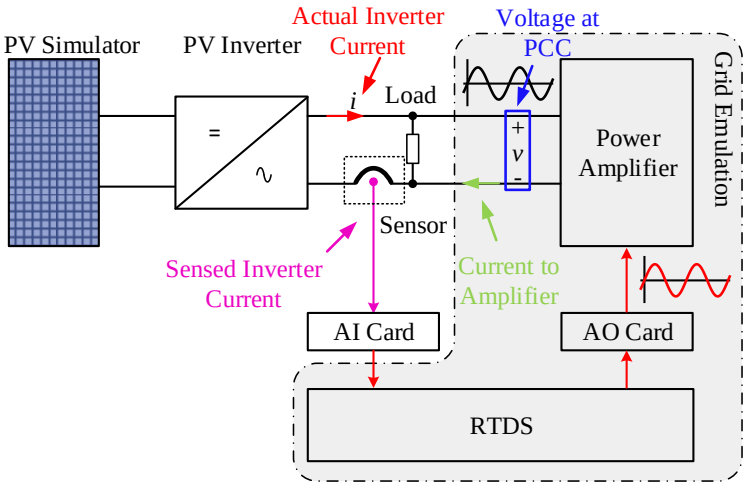


Figure 4.16 PHIL arrangement for evaluating a grid connected PV inverter.

In Figure 4.16, an ITM arrangement is formed through the combination of current sensor and voltage amplifier. The amplifier emulates the grid inside RTDS. A load is connected between the emulated grid and inverter to have a circulating power as well as to protect the amplifier against any potential large current flowing into it. Besides, it is also a common practice to connect a load in between the grid and PV inverter for cases where a distributed generation unintentional islanding operation is to be evaluated [88]. A PV simulator is

configured to match the ratings of the inverter. With this setup, the PV inverter evaluation can be performed with PHIL.

The measured impedance of PV inverter will guide in the initial setup of the system as in the resistor divider case. However, careful attention is needed if a very large source resistance in series to the grid is used. Moreover, the stability criteria with resistance ratio remains valid for PV inverter as well, but the value of source resistance in this case is dictated by the strength of the grid. It is common to define the stiffness of the grid in terms of Short Circuit Ratio (SCR); low SCR corresponding to Weak Grid (WG) and high SCR relating to Strong Grid (SG) [48]. For grid connected power electronic applications, a large inductor connected to the grid is generally used to emulate a WG [48].

Table 4.4 System specifications.

	PV Simulator			**Power Amplifier**		
Parameter	V_{oc}	I_{SC}	P_{max}	P_o	Gain	Type
Value	38.8 V	4.24 A	118.5 W	1 KVA	20	4Q-Linear
	PV Inverter					
	Output Filter (L_1-C-L_2)			**Switching Frequency**		
Parameter	L_1	C	L_2	DC-DC Stage	Inverter Stage	
Value	7.2 mH	0.22 µF	0.47 mH	50 kHz	100 kHz	

In this work, the performance of PV inverter is examined under both SG and WG. A PHIL test setup shown in Figure 4.17 is configured based on Figure 4.16 arrangement. The system specification for this arrangement is given in Table 4.4. The PV micro-inverter is a 140

W two-stage setup with a Flyback DC-DC converter followed by a dual buck in three-level modulation with a 120 V rms output. A Lab-Volt simulator is used to configure it as a PV simulator which is the input to the micro-inverter. Similarly, an AE TECHRON power amplifier is used to emulate the grid. The following section describes the experimental results under different operating conditions.

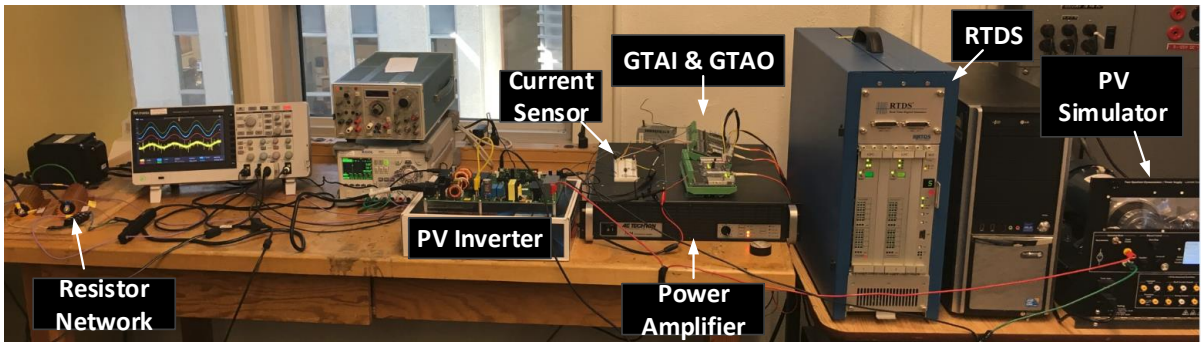


Figure 4.17 PHIL test bed for PV inverter evaluation.

4.5.2.1 Steady-State Operations

The steady-state performance of PV inverter is evaluated under SG and WG conditions. As discussed earlier, SG is configured considering high SCRs (greater than 20). Similarly, for WG emulation, selection of proper inductor in series with grid is vital. From the output impedance characteristic of inverter in Figure 4.10, it is clear that the inverter offers a high impedance path to the high frequency components injected into the grid. Also, at the same time, the third harmonic component in the inverter current cannot be neglected [89]. Therefore, the inductor required to emulate WG can be chosen based on third harmonic component of the line frequency.

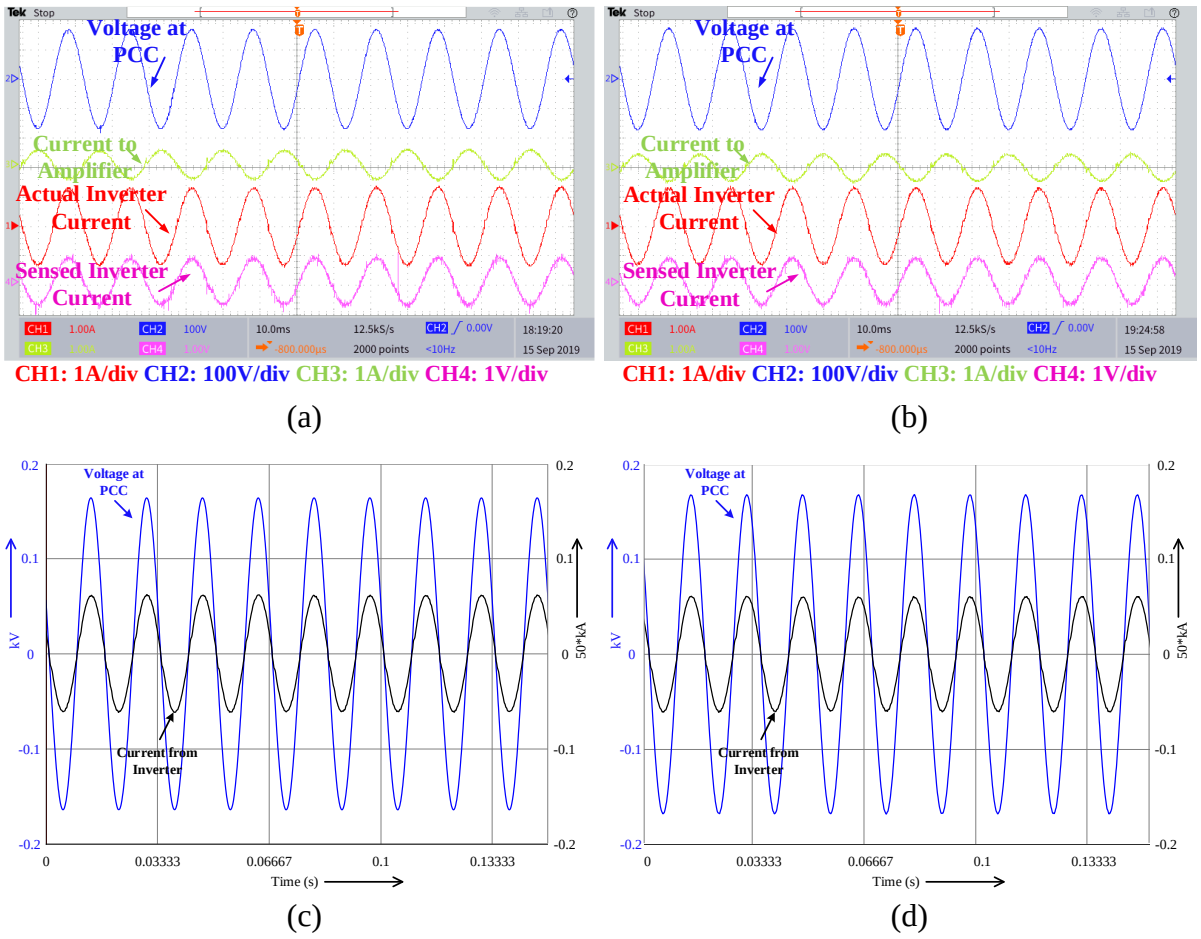


Figure 4.18 Steady-state results of PV inverter with (a) SG-hardware measurements (b) WG-hardware measurements (c) SG-software measurements and (d) WG-software measurements.

The steady-state performance of the inverter under SG shows 110.58 W delivered to the grid. At the same instant, the PV source showed delivering 116.6 W with maximum power point in action. Also, an additional power dissipation of 2.7 W is seen by the source resistance in series to the grid. The difference of 3.32 W (efficiency of 97.15%) accounts for losses within inverter and PHIL inaccuracies. Figure 4.18 (a) demonstrates the key waveforms during steady-state operation with SG. Since the power delivered by PV panel is more than the circulating power dissipated in the resistor at the PCC of inverter and grid, the remaining power

is sunk in by the amplifier. This can be clearly seen in Figure 4.18 (a) as the current to the amplifier is out of phase with the grid voltage. This is the reason behind selecting a four-quadrant amplifier for PHIL implementation. The equivalent inverter voltage and current reflected at the software side is shown in Figure 4.18 (c) which shows the in-phase waveform of voltage and current as in the hardware. Similar operation of PV inverter is observed also with the WG configuration where the power exchange with the grid is recorded at 110.66 W with PV source delivering about 115.2 W power (efficiency of 96.8%). The steady-state operation of PV inverter during this case is shown in Figure 4.18 (b) which records the measurement at hardware and the equivalent in-phase voltage-current waveform at software environment is shown in Figure 4.18 (d).

4.5.2.2 Transient Operations

The PHIL system with PV inverter is further tested for its performance during grid voltage transients viz., sag and swell. The grid voltage transient is made at the peak of the sinewave after each 40 cycles for both SG and WG conditions. From the experimental results presented in Figure 4.19 (a)-(d), it can be observed that, in response to any increase in grid voltage the inverter decreases the current it supplies to by equal proportion, thereby maintaining the power flow. Similarly, decrease in grid voltage causes the inverter to boost up more current, while remaining within its limit, to maintain the power supplied. It is to be noted that, the system remains stable even during grid transients. Therefore, it can be verified that, the stability analysis in Section 4.3 provides enough information to work with a stable PHIL. These observations are crucial in understanding the performance of PV inverter connected to the grid.

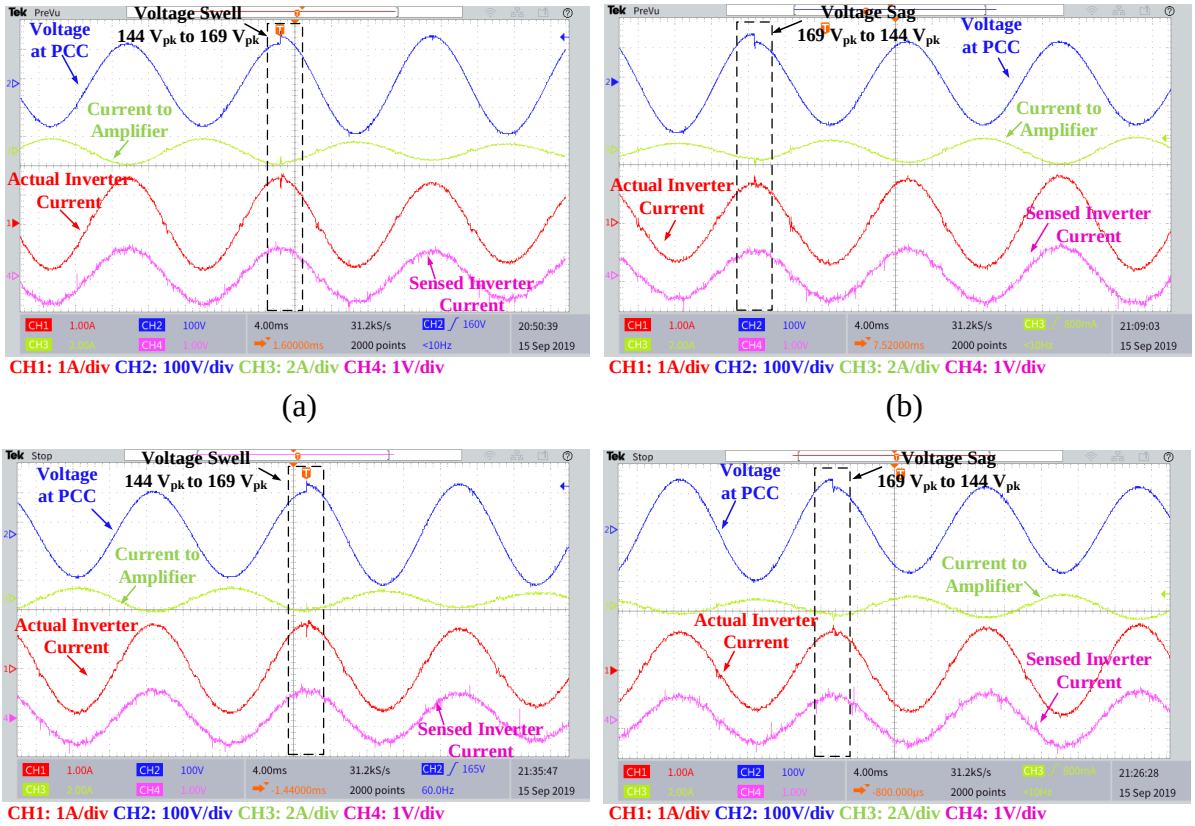


Figure 4.19 Transient performance of PV inverter with PHIL under (a) SG-voltage swell (b) SG-voltage sag (c) WG-voltage swell (d) WG-voltage sag.

4.5.2.3 Accuracy Estimation

The accuracy of a PHIL system with PV inverter can be estimated in a way similar to that described in Section 4.5.1. Since the PV inverter under study does not support reactive power exchange, any reactive power seen at the PCC of hardware end and software end corresponds to the error due to PHIL. These measurements are taken at different loading conditions of the power amplifier and are tabulated below in Table 4.5.

Table 4.5 Error measurements.

Amplifier Loading	Error %		
	Hardware	Software	Total
~No-Load	2.902	0.658	3.56
~Half-Load	2.621	0.394	3.015

In Table 4.5, the error measurements at hardware does not take into considerations the error in the Phase Locked Loop (PLL). This could be the possible reason for higher error at the hardware end compared to the software. Basically, it can be said that use of compensator aids in stability with a reasonable accuracy margin.

4.6. Discussion on Future Applications

The methodology described in this work to perform PHIL experiments with PV micro-inverter can be easily extended to perform similar type of other PHIL experiments with hardware consisting of renewable sources. The reason being, the stability criteria developed in this work is based on resistance and therefore as long as the hardware resistance is known, the analysis methodology can be employed to guarantee a stable PHIL. Considering this, instead of modelling PV by a negative resistance as in [90], [91] and state space averaging to model inverter, this work directly uses an impedance measured from the network analyzer to perform the stability analysis. Another important factor that can be considered for the completeness of the analysis is replacing the hardware resistance in the mathematical formulations with a frequency dependent impedance. This allows to include the effect of hardware in the overall

stability of the PHIL. Additionally, this would also help to analyze the effect of harmonic resonances from the hardware impedance. However, the resistance criteria proposed in this thesis forms the basis for further formulations. Moreover, the resistance-based criteria still serve as an important tool to understand the overall system behavior with PHIL architecture. The experiments performed are in good standing to validate the proposed method. Further advantages of such approach could be an evaluation of a converter connected to a renewable source with unknown topology and controller with PHIL, in other words, the DUT could be a black box.

4.7. Summary of Chapter 4

This chapter presented a mathematical framework for considering stability analysis of PHIL. The expression considers all the parameters in the interface to predict the stability and therefore may serve as a tool in determining the proper interface devices beforehand. Besides, the effect of adding a current filter along with compensation design technique to eliminate the effect of filter delays has been extensively analyzed. The quantitative stability analysis has been proposed in this paper considering a resistor divider network. This analysis has been further extended to experimentally evaluate a grid connected PV inverter with PHIL. The PV inverter with PHIL configuration showed a stable and accurate operation at steady-state and during various grid transients. The experimental results of PHIL system showed a good agreement with the theoretical predictions.

Chapter 5

ITM Interface Characterization and Compensator Design for a Delay Free PHIL Response

- *A Part of the work presented in this chapter is the result of original work accepted to be published under* ***M. Pokharel****, and C. N. M. Ho,* ***"Modelling and Experimental Evaluation of Ideal Transformer Algorithm Interface for Power Hardware in the Loop Architecture," IEEE Applied Power Electronics Conference (APEC),*** *March 15-19, N.O., LA, USA..*
- *A Part of the work in this chapter is also the result of original work submitted under* ***M. Pokharel*** *and C. N. M. Ho,* ***"Development of Interface Model and Design of Compensator to Overcome Delay Response in a PHIL Setup for Evaluating a Grid-Connected Power Electronic DUT," IEEE Transactions on Power Electronics.***

The purpose of this work is to develop an accurate model of interface devices arranged to form an ITM interface. The experimental arrangement consisting a GPA for extracting the individual interface devices frequency response is presented in this work. The comparison between experimentally obtained frequency response and developed model frequency

response is also presented in this chapter. The accurate model of interface devices aids in any stability and accuracy studies of a PHIL. The experimentally verified model is used to design a SP-based compensator that works to eliminate the effect of delay in the closed loop response of a PHIL system. The details of the work are presented in the subsequent sections.

5.1. Introduction

Interface devices are crucial to achieving PHIL configuration. It is the interface that separates PHIL implementation with its real counterpart. This inclusion of interface at power decoupling point has raised the concern of stability and accuracy among researchers. It is therefore essential to study the effect of interface if the PHIL system is to be entirely understood. The overview on various interfacing methods and their performance parameters is discussed in Section 2.3. Also, it is well reported that ITM is one of the widely accepted interfacing algorithms to form a PHIL testing. In this regard, the analysis and testing that forms the part of this chapter uses ITM to further its studies.

The graphical approach for stability analysis with Nyquist has been in frequent use in the literatures [57], [92]. Besides, RH stability table is another tool that is been in use to perform the stability studies of PHIL [92], [93]. While both these tools offer advantages in stability assessments, there is no clear mention on the accuracy of the models used which are relied on theoretical formulations only. Besides, it is vital that any stability or accuracy analysis made henceforth with the existing interface models be handled with extra caution. Instead, a better approach would be to first ensure that the interface model is accurately reflecting the actual interface hardware in action. Taking this into consideration, this work proposes an operational-sequence-based model of interface devices and validates this model

experimentally using frequency sweep approach. The frequency sweep is carried out using a GPA to the interface consisting of analogue cards and a linear amplifier with RTS in the loop. In this work, RTDS with its GTAO and Giga-Transceiver Analogue Input (GTAI) cards is used for validation of the model experimentally.

The stability analysis of PHIL has made the part of many research literatures [26], [37], [57], [93]. This is due to the fact that if a system is decoupled at a certain power exchange point and an interface is introduced to complete this power flow loop, it comes at an expense of delay and limited bandwidth within the interface that raises the concern of stability. This has also been discussed in Section 1.3 in details. To reiterate, limitations like bandwidth and delay of the interface calls for a detailed investigation of the stability of a PHIL system. The work presented in this chapter focuses on the effect of delay on PHIL instability and proposes a compensator that acts to overcome the response due to delay while aiding the stable operation of PHIL system. The proposed model of interface devices in ITM extracted from experiments is utilized to design this compensator.

5.2. Mathematical Model of ITM Interface

The general arrangement of a PHIL in ITM interface used to evaluate a PE based DUT is shown in Figure 5.1. As seen in Figure 5.1, the combination of GTAO, PA, sensors and GTAI forms the interface device in an ITM. Considering this, the sections following studies each of this interface devices and develops a working model that can be used in performing stability and accuracy studies. The analyses made throughout this chapter considers the sensor's response to be fast enough to model it as a device with unity gain.

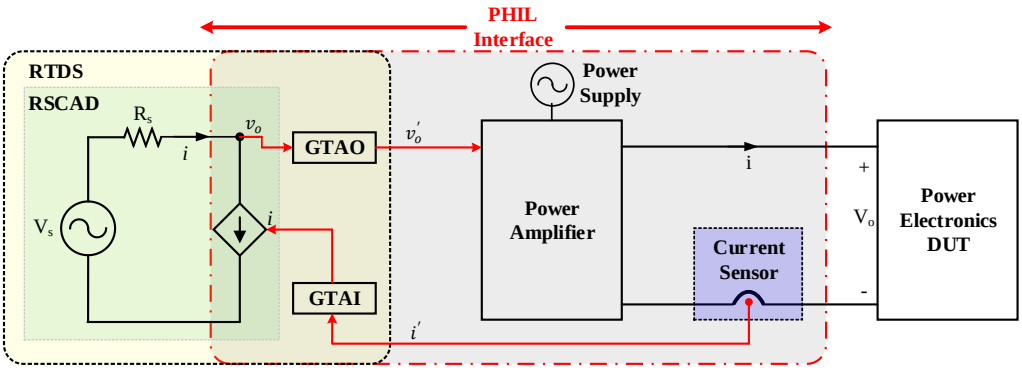


Figure 5.1 An ITM configuration for evaluating a PE DUT.

5.2.1 Model of an Analogue Input Card

The AI, labelled as GTAI in arrangement of Figure 5.1, takes signals from the physical system into simulation environment for further processing. This requires that the physical analogue signal be first converted to digital before it can be used in the simulation system.

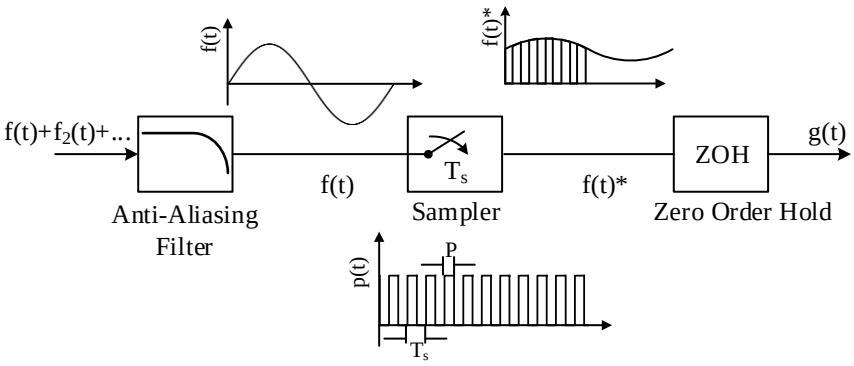


Figure 5.2 Functional block of an AI card.

The operational sequence of an AI card can be represented by a functional block in Figure 5.2. The AI card consists of 12 channels, 16-bit resolution ADC with an Anti-Aliasing Filter

(AAF) at each input before the ADC to remove the aliasing due to sampling. The TF representing the AAF model can be expressed as a first order low pass filter given as;

$$G_{aaf}(s) = \frac{G_{aaf}}{1+sT_{aaf}} \tag{5.1}$$

where, G_{aaf}=gain of the filter, and $T_{aaf} = 1/(2\pi f_{aaf})$ is the cut-off of the AAF. The AAF cut-off is to be selected based on the sampling or the time-step used in the RTS model.

Further, the ADC process can be represented in two steps; first, by a sampler which samples the continuous time signal $f(t)$ by a series of pulse train with width *P* and period T_s, and followed by a Zero Order Hold (ZOH). If the width of the pulse *P* is very small, the sampling operation can be simplified using an impulse sampler. Mathematically, the impulse sampling operation of a continuous time signal is described by (5.2).

$$f^*(t) = f(t)\sum_{k=-\infty}^{k=+\infty}\delta(t - kT_s) \tag{5.2}$$

where, $f(t)$ is the original continuous time signal and $f^*(t)$ is the sampled signal by an infinite impulse train represented by $p(t)$.

In frequency domain, (5.2) can be expressed by the convolution of original signal with a pulse train.

$$F^*(\omega) = \frac{1}{2\pi}\, F(\omega) * P(\omega) \tag{5.3}$$

where, $P(\omega) = 2\pi\sum_{k=-\infty}^{k=+\infty} P_k\delta(\omega - k\omega_s)$ and using Fourier Transform P_k can be derived with ω_s being the radial sampled frequency given by $\omega_s = T_s/2\pi$.

$$P_k = \frac{1}{T_s}\int_{-\frac{T_s}{2}}^{\frac{T_s}{2}}\delta(t)e^{-jk\omega_s t}dt = \frac{1}{T_s}$$

Therefore, it can be said that P_k is a just a number $1/T_s$ for all Fourier series coefficient which yields the frequency domain representation of an impulse sampling train.

$$P(\omega) = \frac{2\pi}{T_s}\sum_{k=-\infty}^{k=+\infty}\delta(\omega - k\omega_s) \tag{5.4}$$

Substituting (5.4) in (5.3) and using convolution property for impulse we arrive at the final expression of sampled signal.

$$F^*(\omega) = \frac{1}{T_s}\sum_{k=-\infty}^{k=+\infty}F(\omega - k\omega_s) \tag{5.5}$$

Equation (5.5) shows that a sampled signal contains an infinite collection of the shifted version of the original signal frequency spectrum $F(\omega)$ scaled by a factor $1/T_s$. The above deductions are directly interchangeable with the Laplace domain. Therefore expressing (5.5) in s-domain results in;

$$F^*(s) = \frac{1}{T_s}\sum_{k=-\infty}^{k=+\infty}F(s - \mathrm{j}k\omega_s) \tag{5.6}$$

Unlike an impulse sampler which cannot be physically realized, more practical way to sample is ZOH which can be understood more like an impulse sampled signal fed to a low pass filter.

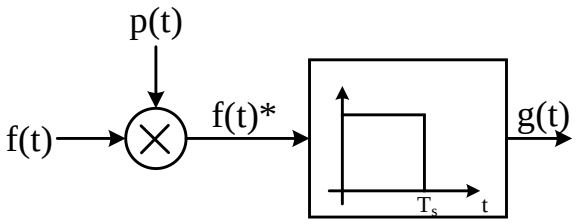


Figure 5.3 Mathematical representation of a ZOH.

The mathematical formulation of ZOH is shown in Figure 5.3 where $f(t)$, $p(t)$ and $f(t)^*$ are the continuous time signal, sampler signal and sampled signal respectively. The ZOH operation in Figure 5.3 can be explained as; for every impulse sample that comes in, a

rectangular pulse comes out. The time domain representation of a ZOH operation is a rectangular function expressed by (5.7).

$$h_{zoh}(t) = rect\left(\frac{t-\frac{T_s}{2}}{T_s}\right) \tag{5.7}$$

The frequency domain representation of (5.7) can be obtained by performing a Laplace transformation as;

$$H_{zoh}(s) = \mathcal{L}\{h_{zoh}(t)\} \rightarrow \int_{-\infty}^{+\infty} h_{zoh}(t)e^{-st}dt$$

Which yields;

$$H_{zoh}(s) = \frac{1-e^{-sT_s}}{s} \tag{5.8}$$

From (5.6) and (5.8) the overall transfer function that models the ADC process in general can be obtained.

$$G(s) = H_{zoh}(s)F^*(s)$$

$$G(s) = \frac{1-e^{-sT_s}}{sT_s}\sum_{k=-\infty}^{k=+\infty} F(s - jk\omega_s) \tag{5.9}$$

In (5.9), it is valid to assume that the high frequency components due to sampling will have minimal to no effect due to the low pass nature of ZOH. Hence, only considering the low frequencies (5.9) yields to;

$$G(s) = \frac{1-e^{-sT_s}}{sT_s}F(s) \tag{5.10}$$

From (5.1) and (5.10) the complete model of AI card can be obtained as;

$$G_{AI}(s) = \frac{G_{aaf}\left(1-e^{-sT_s}\right)}{sT_s\left(1+sT_{aaf}\right)} \tag{5.11}$$

5.2.2 Model of an Analogue Output Card

The AO card labelled as GTAO in Figure 5.1 functions to feed out the signal specified in the simulation environment to signal that can be directly processed for real world applications. This includes use of this signal as control signal when working with CHIL applications or as a power signals after amplifying for PHIL applications. Irrespective of the application, the conversion in the AO card is carried out by a high precision DAC and therefore can simply be represented by the conversions delay specified in the hardware manual.

$$G_{AO}(s) = e^{-sT_1} \tag{5.12}$$

Where, T_1 is the conversion time it takes for the digital value to be converted to its corresponding analogue value.

5.2.3 Model of a Linear Amplifier

For a PHIL application with linear amplifier, the transfer function model can be estimated with a first order low pass characteristic. The model contains a gain to represent the amplification and a low pass cut-off frequency that represents the bandwidth of the amplifier. Additionally, a delay function is needed to incorporate the delay between input and output of the amplifier. The complete model of amplifier is given by (5.13).

$$G_{AMP}(s) = \frac{A}{1+sT_{amp}} e^{-sT_2} \tag{5.13}$$

Where, A= amplifier gain, T_{amp}=amplifier bandwidth=$1/2\pi f$, and T_2=delay between input and output.

5.3. System Implementation

The individual model of interface devices developed in Section 5.2 needs to be verified to check for their accuracy. For this, the combination of AO and AI cards are configured in real hardware setup to extract their frequency responses. The frequency response obtained from the experimental measurements can then be compared with the frequency response from the developed model for their accuracy.

For the purpose of this work, the models are developed considering RTDS along with its accessories cards as the RTS. A four-quadrant linear amplifier from AE TECHRON 7224 is used as the amplification device for PHIL application. To extract the experimental frequency response of these devices, a GPA from Bode-100 is employed. A GPA is used to inject various frequencies into the system and measure the sweep response back from the GPA. This approach allows to generate the gain and phases at various frequencies experimentally for the DUT.

5.3.1 AO-AI Card Frequency Response Measurement Setup

The experimental determination of frequency response of individual AO and AI cards is not possible as either of input or output points are inaccessible in the physical hardware. The way around this is to set up a GPA such that it feeds multi frequency sinusoid as an input to the AI card and measures the response at the AO card. With this, the sinusoid fed through AI card from GPA experiences AAF, ADC, a time step delay at the simulation environment through its path before it is fed out of high precision DAC by AO card back into the GPA. This allows to extract the frequency response of both the AO and AI cards combined at once. The system implementation setup to achieve the experimental determination of frequency response

of AO-AI card combination is shown in Figure 5.4. As explained in Figure 5.4, GPA labelled as Bode 100 feeds the multi frequency sinusoid into AI card which is monitored at Channel-1 and the response out from AO card monitored at Channel-2. The resulting frequency response from GPA is extracted through the interfacing software.

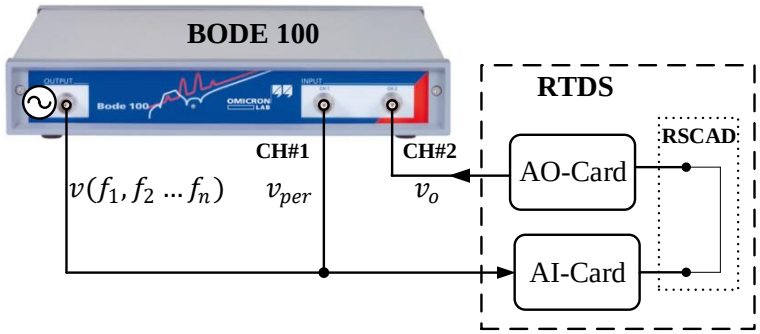


Figure 5.4 Hardware setup for frequency response extraction of AO-AI card.

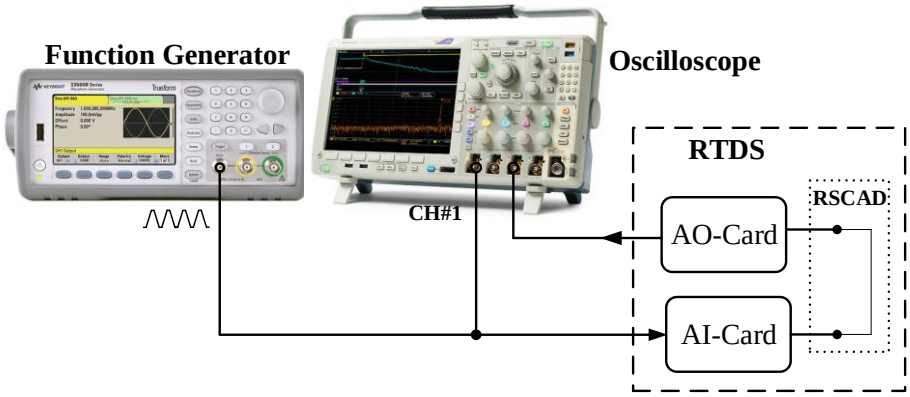


Figure 5.5 Hardware Setup for delay estimation of AO-AI card.

Additionally, it is also important to know the round-trip delay for the signal fed into AI to be seen back at AO. For this, a ramp signal with flat top and bottom is manually generated using a Keysight function generator and fed into AI. The input to AI and output from AO is overlaid together to measure the delay between input and output. The fact that RTDS has a

projection advance factor at AI input interface to compensate for the time step, for a waveform with a sharp slope it would distort the signal at the point of change. Therefore, a flattened ramp would give a good estimate of the round-trip delay. The experimental arrangement for estimating the time delay from input to AI to output from AO is shown in Figure 5.5.

5.3.2 Linear Amplifier Frequency Response Measurement Setup

The frequency response measurement for a linear amplifier, AE TECHRON 7224, is made in a way similar to the method mentioned for AO-AI card. The GPA is used to inject a multi frequency sinusoid at the input of amplifier and the gain of the amplifier is set to its maximum, a value of 20. It is important that extra care is given when the amplified output is fed back to the GPA so that it doesn't exceed its rated limit. For this purpose, a probe with suitable attenuation is selected such that amplified voltage can be lowered to the range suitable for GPA. Also, at the same time, the attenuation can be recovered back into the software or the calibrations can be run beforehand with the probes.

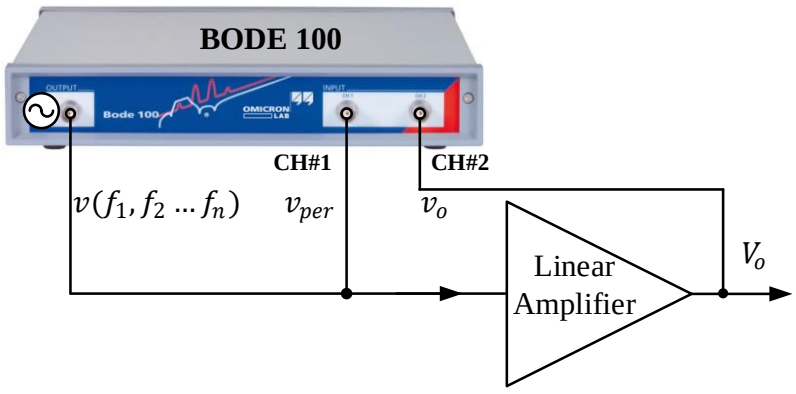


Figure 5.6 Hardware setup for frequency response extraction of linear amplifier.

The experimental setup for frequency response measurement of a linear amplifier is presented in Figure 5.6. Similar to that of AO-AI card, the response generated from GPA is fed to the input of amplifier and monitored by GPA in Channel-1 and the output of the amplifier is fed back to Channel-2 of GPA through a Testec differential probe with attenuation factor of 1:1/10.

The delay between input and output of the amplifier is also required to understand the performance of the amplifier. For this, the setup shown in Figure 5.7 can be arranged where a square pulse from function generator is fed to the input of amplifier and the amplified output is overlaid with the input to measure the delay in the oscilloscope.

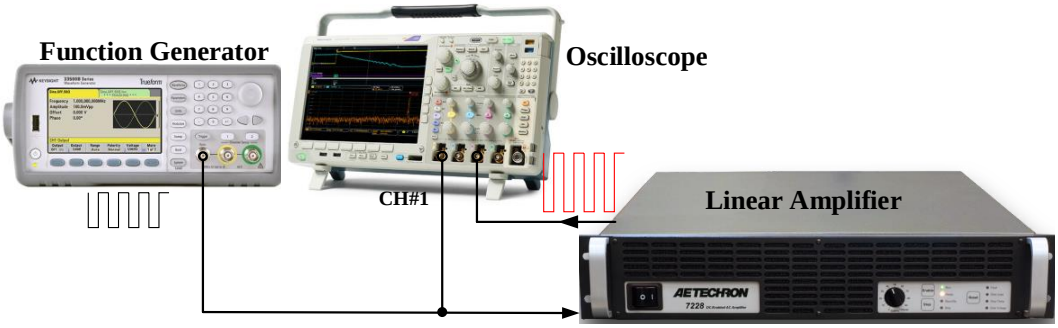


Figure 5.7 Hardware Setup for delay estimation of linear amplifier.

5.3.3 AO-AI-Linear Amplifier Frequency Response Measurement Setup

The measurement setup of a combination of linear amplifier with AO-AI card follows the similar setup as that of AO-AI except the amplifier comes after the output of AO before it is fed back to the GPA, shown in Figure 5.8. Careful consideration as that of linear amplifier frequency response measurement is to be taken, specially when the output of amplifier is fed back to the GPA. Probe compensations are to be made beforehand.

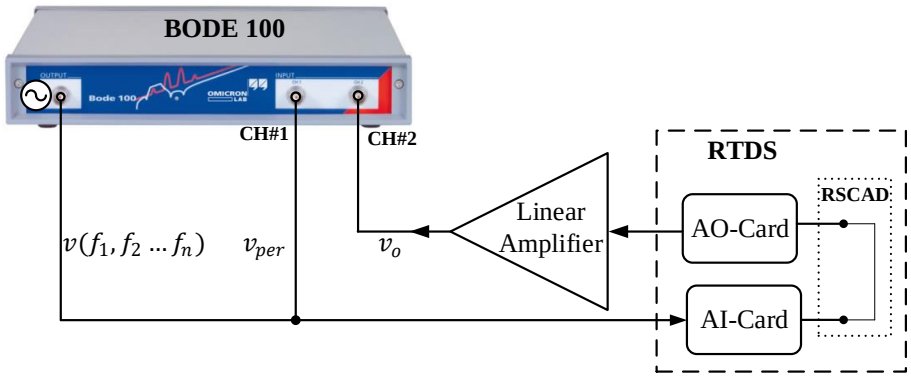


Figure 5.8 Hardware setup for frequency response extraction of linear amplifier-AO-AI card.

5.4. Experimental Results and Model Validation

In Section 5.3, various arrangements for validating the model of individual interface devices that form the ITM interface in PHIL studies are presented. The frequency response obtained experimentally helps to understand how the actual system behaves for various system parameters. By plugging in parameter similar to obtain the experimental gain-phase measurements in the model developed in Section 5.2, the theoretical frequency response can be obtained. For comparison between theoretical and experimental frequency responses, results can be overlaid for varying time-steps.

5.4.1 AO-AI Card Model Validation

The model of AO-AI card combined can be derived from their respective transfer functions (5.11) and (5.12). For the system setup as shown in Figure 5.4 which forms the part of the arrangement of ITM in PHIL, following can be written.

$$G_{AOAI}(s) = \frac{G_{aaf}\left(1-e^{-sT_s}\right)}{sT_s\left(1+sT_{aaf}\right)} e^{-sT_1} \tag{5.14}$$

Though (5.14) gives the model of AO-AI combined, it does not however replicate the experimental setup of Figure 5.4. This is due to the fact that, for every input that is fed through AI card it experiences a time step delay before it is fed out of AO. In order to validate this, a setup as shown in Figure 5.5 is arranged. The delay between input ramp and output ramp is measured in the oscilloscope which gives the round-trip delay that a signal experiences as it goes from AI to AO.

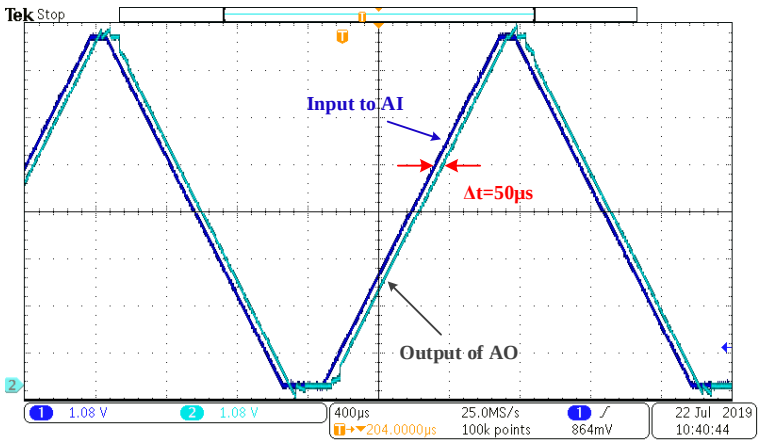


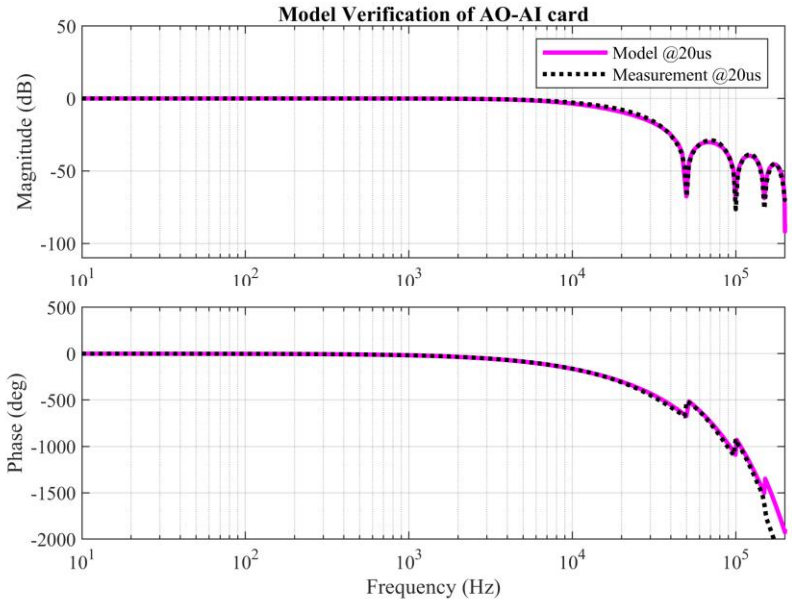
Figure 5.9 Delay measurement from AI to AO for a time step of 50 μs.

The measurement in Figure 5.9 shows the oscilloscope reading for a time step of 50 μs in the RTS. As expected, the oscilloscope reading also shows this delay between the two measurements. Therefore, for the completeness of the model the transfer function in (5.14) needs to incorporate a time-step delay.

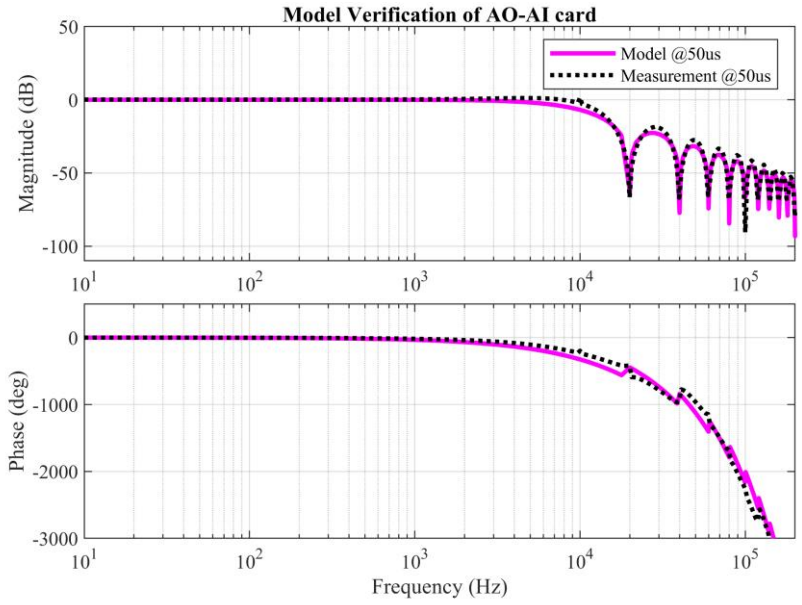
$$G_{AOAI}(s) = \frac{G_{aaf}\left(1-e^{-sT_s}\right)}{sT_s\left(1+sT_{aaf}\right)} e^{-s(T_1+T_d)} \tag{5.15}$$

The transfer function in (5.15) contains T_1 which is the conversion time of DAC and T_d the time step delay. Usually the effect of T_1 is very minimal as compared to that of time step

and hence can be excluded from the analysis. Also, the sampling time T_s is again the time step of the simulation and the antialiasing filter parameters are known as well. With this, there is enough information to plot the frequency response of the AO-AI model. The parameter used for gain phase plot for AO-AI model is tabulated in Table 5.1.



(a)



(b)

Figure 5.10 AO-AI frequency response for a time step of (a) 20 µs (b) 50 µs.

Table 5.1 AO-AI card model parameter.

Parameter	G_{aaf}	T_{aaf}	T_1	$T_d = T_s$
Value	1	$1/2\pi f_{aaf}$; $f_{aaf} = 10.1\ kHz$	1.8 µs	50/20 µs

The gain and phase plot of AO-AI model with the parameters described in Table 5.1 for a time step of 20 µs and 50 µs is compared with the experimentally obtained data with the setup shown in Figure 5.4. The plots of gain and phase are overlaid and presented in Figure 5.10. The results show a good agreement between the experiment and theoretical model in a certain frequency range. Also, the fact that Nyquist criteria would be violated after a certain frequency the measured signal cannot entirely follow the modelled response. Again, it is irrelevant to consider the model after the Nyquist frequency. Therefore, considering linearity, the proposed model gives an accurate response as that of the actual system.

5.4.2 Linear Amplifier Model Validation

The linear amplifier model is expressed by it transfer function in (5.13). The parameters like the gain and bandwidth required to plot the frequency response for (5.13) is taken from its datasheet. The delay however is measured using the experimental setup shown in Figure 5.7. The measurement recorded from the setup is shown in Figure 5.11. Multiple runs are made, and they are all averaged to estimate the delay. The parameters used to plot the frequency response of linear amplifier are tabulated in Table 5.2.

The experimental determination of frequency response of linear amplifier is made using the approach mentioned in Section 5.3. The system implementation setup is given in Figure

5.8 and the results from experiment and developed model are overlaid and presented in Figure 5.12.

Table 5.2 Amplifier parameter.

Parameter	**Gain(A)**	**Bandwidth (T_{amp})**	**Avg. Delay (T_2)**
Value	1	$1/2\pi f_{aaf}; f_{aaf} = 400\ kHz$	687 ns

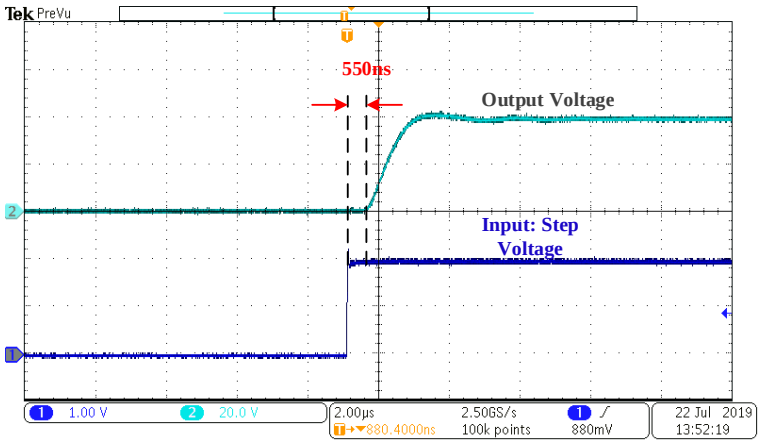


Figure 5.11 Delay measurement of a Linear amplifier.

The frequency response of the developed model and the one obtained from the experiment is in close match until 100 kHz after which the gain and phase deviates widely. This is due to the fact that amplifier is modelled with a first order response while the one obtained from experiment is attenuating at more than 20dB/decade indicating it has more than a first order response. However, for the application of PHIL with AI card having antialiasing filter with a maximum cut-off of 84.3 kHz, the 100 kHz margin seems to be a fair enough margin to consider the accuracy of the developed model.

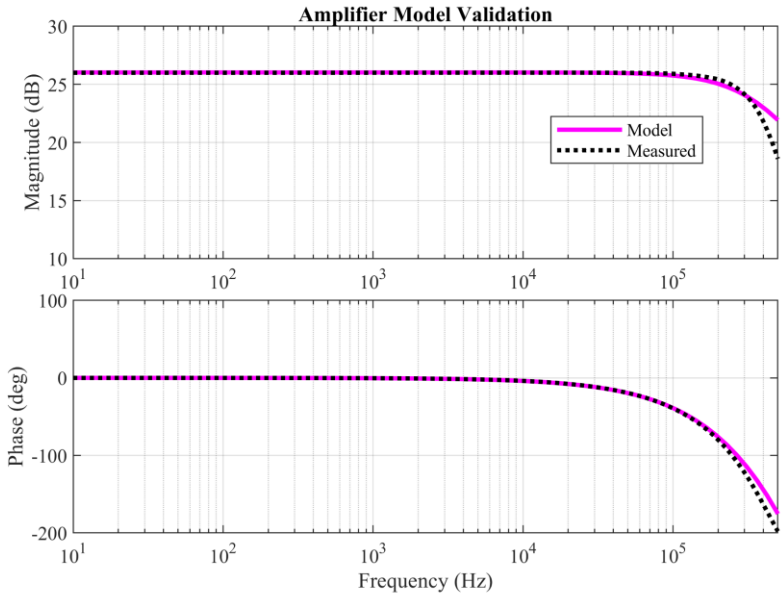


Figure 5.12 Frequency response of a linear amplifier for developed model and experiment.

5.4.3 Linear Amplifier with AO-AI Model Validation

The model developed for AO, AI and linear amplifier forms the basis for further verification for similar other architectures. Considering the linearity of the system, using superposition, the system of transfer functions can be lumped to obtain the overall system model consisting of AI-AO-amplifier combination. The setup shown in Figure 5.8 can be used to export the frequency response experimentally of such combination. The result from the experiment and model are overlaid in Figure 5.13. The theoretical frequency response is in close agreement with experimental responses. In addition, the linearity of the system is also verified by adding the individual experimental responses of AO-AI and amplifier and compared with combined experimental and theoretical responses. As seen from Figure 5.13, all three responses overlap each other until a frequency close to 100 kHz. This therefore validates the developed model that can be used to further the studies in PHIL.

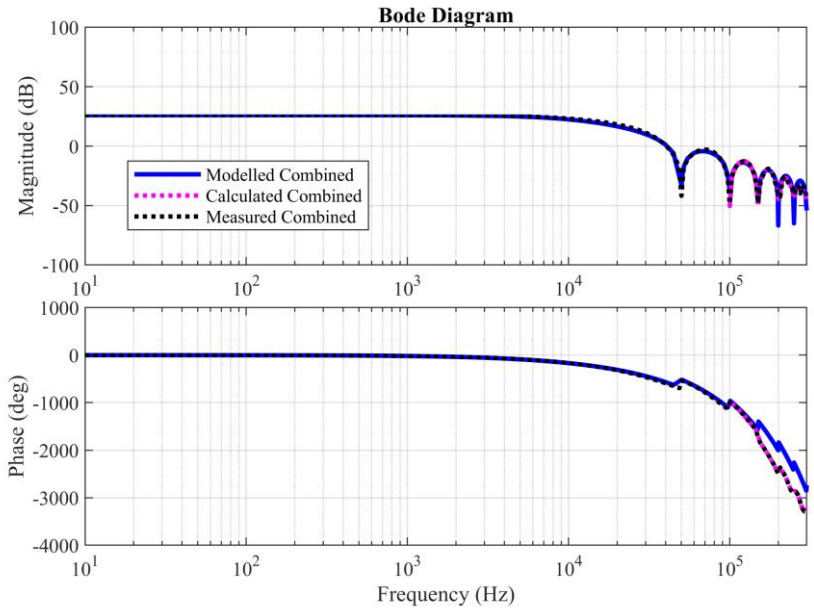


Figure 5.13 Frequency responses of modelled, calculated and measured AO-AI-amplifier combination.

5.5. Stability of a PHIL with an ITM Interface

The stability studies in PHIL has made the focus of many research works. Moreover, before investigating the stability, it is important to understand the PHIL operation. As the interface in the PHIL is the bottleneck to achieving a stable and accurate actual-like performance, it is evident that an in-depth examination of the interface is required to gain clarity on the PHIL performance.

An actual hardware setup in a PHIL arrangement suffers from a delay as a result of the interface devices and the RTS computation. It is obvious that this delay needs to be eliminated to be able to guarantee an accurate and stable PHIL. A system of PHIL network when analyzed by treating it as a control block as in Section 4.2.2 can be directly compared with a standard delay inherited system represented by Figure 2.3. In this respect, the effect of delay is seen in

the closed loop response of the PHIL system. There are various compensation techniques to overcome the delay for a conventional delay inherited system. One of those methods that eliminates the effect of delay seen in the closed loop response is a Smith predictor compensator. The design methodology and details of designing such compensator is presented in Section 2.6.

The mathematical expression of a SP compensator when employed to a system consisting of delay is given by (2.7). Equation (2.7) gives the model of compensator to be employed in the forward path along with existing controller to achieve a delay free response. Moreover, an important observation from (2.7) is that it requires the model of plant and delay. When such compensator is realized for a system consisting of delays like the PHIL, it becomes critical that each device in the PHIL loop is modelled accurately. And, this is where the experimentally verified model in Section 5.2 and Section 5.4 comes particularly handy. So is the case with delay model, whose accuracy with PD is well discussed in Section 4.2.3. With the interface and delay model, it is apparent that there is enough information to go forward with the compensator design for a PHIL system.

5.6. Delay Compensation of a PHIL System

To demonstrate the delay compensation in a PHIL system, a standard case of a resistor divider network arranged in PHIL configuration shown in Figure 5.14 is considered. The input is a controlled voltage source which could be a DC, or an AC connected to an input resistor R_s. The network is decoupled by an ITM interface at the node between two resistors R_s and R_h.

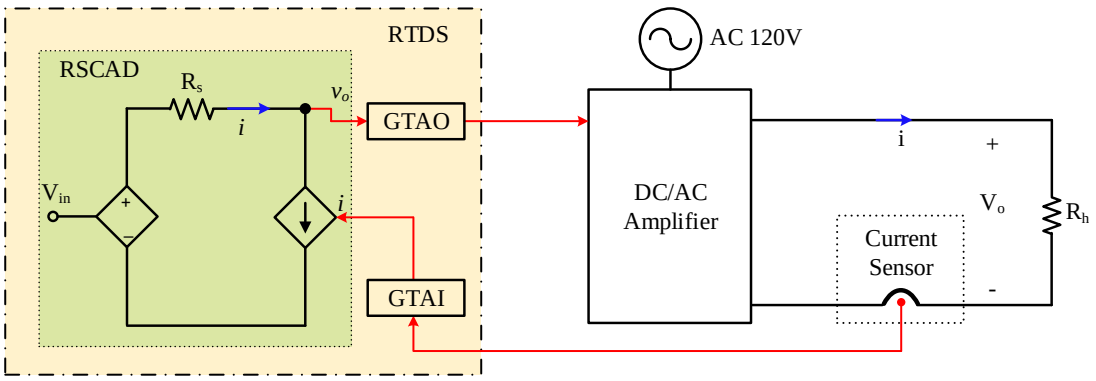


Figure 5.14 PHIL arrangement of a resistor divider network.

The system in Figure 5.14 can be developed to form a standard control block like structure by expressing individual interface devices by their respective TFs developed in Section 5.2. The architecture of the PHIL for resistor divider replicates the combination of AO-AI-amplifier as in the model validation section. This can also be seen from the control block in Figure 5.15. A delay due to time step is included in the forward path to accurately model the arrangement in Figure 5.14.

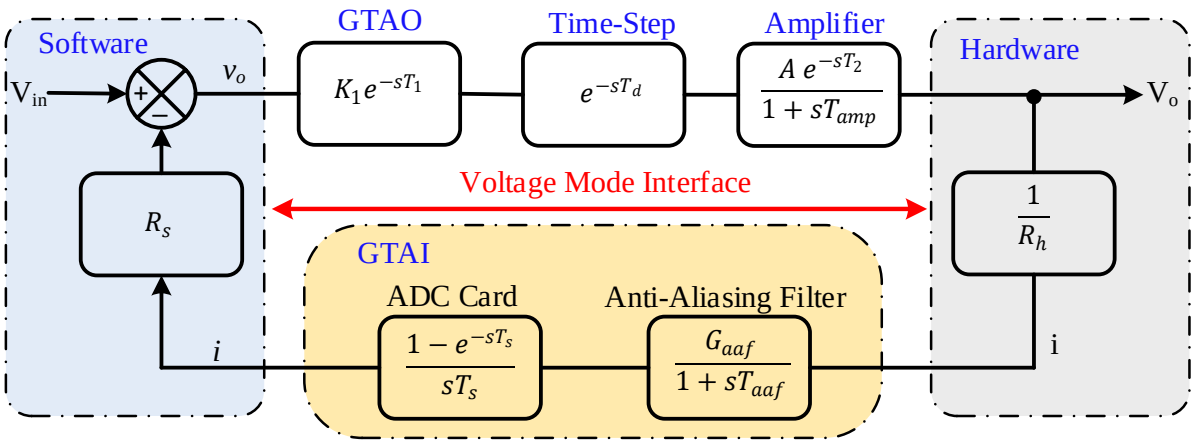


Figure 5.15 Control block representation of a PHIL resistor divider network.

The system in Figure 5.15 closely resembles the standard control of Figure 2.3, except the controller $G_c(s)$ and an additional transfer function in the feedback path. Similar sequence of mathematical formulations can be made to design the compensator that eliminates the effect of delay in forward path in the closed loop response. However, before that, it is essential to study the system response without the compensator. For this, Nyquist plot and step response of the system are analyzed for the parameters of the interface specified in Table 5.1 and Table 5.2 for resistances ratio $R_s/R_h = 1.4$ with a time step of 50 µs.

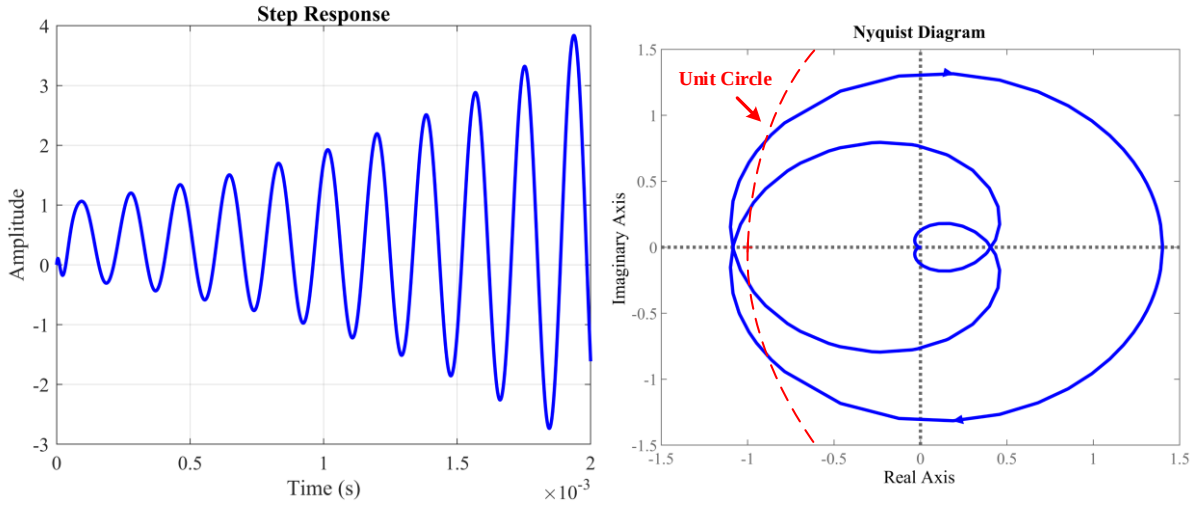


Figure 5.16 A response of an uncompensated PHIL network.

As can be seen from the plot of Figure 5.16, the time response of the uncompensated PHIL shows an increasing oscillatory response and the Nyquist plot shows an unstable closed loop response as the unit circle is encircled in clockwise direction. Further, it is observed that the system response degrades as the time delay increases. This proves the need for improvement of the uncompensated PHIL system.

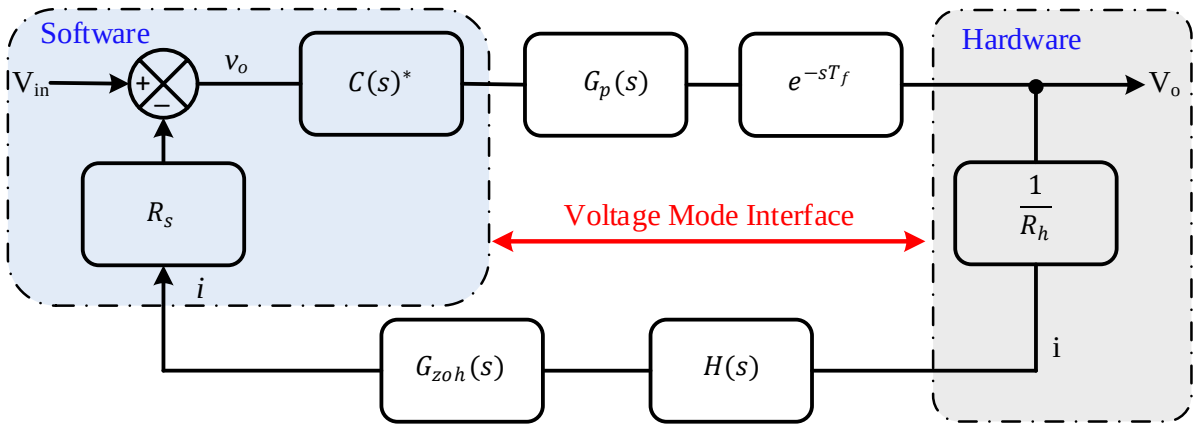


Figure 5.17 Architecture of a compensated PHIL network.

Once the response of an uncompensated system is studied, it becomes evident the need to overcome the effect of delay. To achieve this, a SP based compensator can be designed and placed in the software environment. Other advantage of having the compensator in software environment is the flexibility with which it can be redesigned to match the design specifications. The redesigned control block of Figure 5.15 with compensator inserted is shown in Figure 5.17. All the delays in the forward path are lumped into T_f, the gain K_1 and A are configured to cancel out each other and other notations in Figure 5.17 follows as;

$$\left.\begin{aligned} G_p(s) &= \frac{1}{1+sT_{amp}} \\ G_{zoh}(s) &= \frac{1-e^{-sT_s}}{sT_s} \\ H(s) &= \frac{1}{1+sT_{aaf}} \end{aligned}\right\} \tag{5.16}$$

From Figure 5.17 and by comparing with the equivalent delay free system, the compensator structure can be derived as;

$$C(s)^* = \frac{1}{1+G_p(s)H(s)G_{zoh}(s)\left(\frac{R_s}{R_h}\right)\left(1-e^{-sT_f}\right)} \tag{5.17}$$

Comparing (5.17) with a standard SP controller structure in (2.6), the SP compensator model can be obtained.

$$C(s) = G_p(s)H(s)G_{zoh}(s)\left(\frac{R_s}{R_h}\right)(1 - e^{-sT_f}) \tag{5.18}$$

In (5.18), the presence of exponent representing delays and ZOH makes it difficult to realize it practically. Therefore, (5.18) needs to be studied further to transform it into a physically realizable form. Looking carefully at (5.18), ZOH can be understood as the discretization term that converts continuous TF to discrete domain. This term can be eliminated for implementation purposes but is essential during design for checking the Nyquist frequency limit. Further, the exponential delay term can simply be expressed in rational form with PD. With this, the compensator becomes practically implementable and can be tested for the unstable system of Figure 5.16.

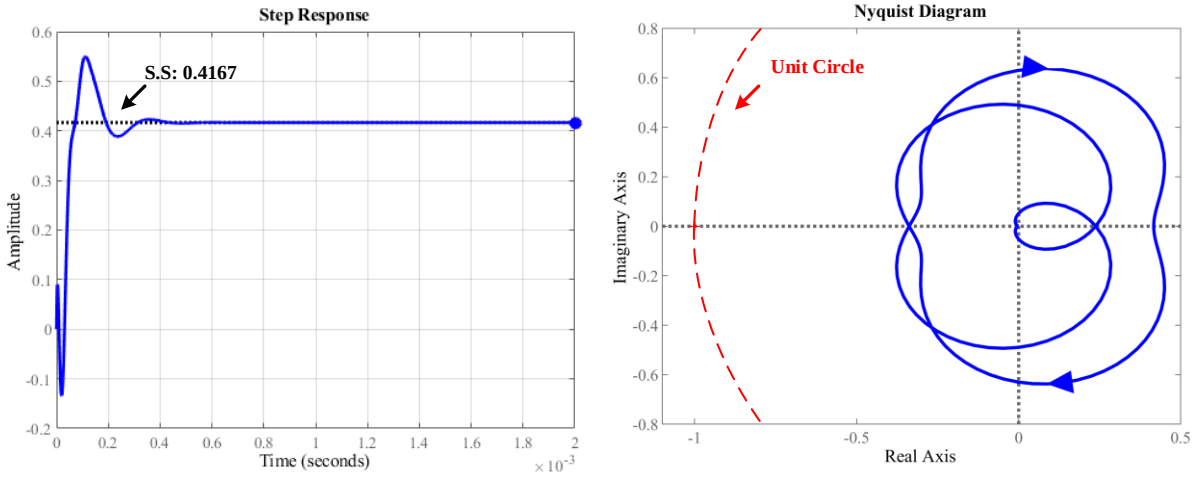


Figure 5.18 Response of a PHIL network with compensator.

The response in Figure 5.18 shows a stable Nyquist plot for a compensator employed resistor divider PHIL system of Figure 5.15. Also, the time response of this compensator

employed network shows a steady-state value of 0.4167 (for $R_s = 1.4\ R_h$). This theoretically verifies the use of SP compensator for PHIL application. Further, the compensator will be tested in an actual PHIL application to validate its operation in real time.

5.7. Experimental Verification of a Compensator Employed PHIL

In Section 5.6, a detailed procedure for designing a SP compensator to overcome the delay response in a PHIL system was presented. The compensator was tested for an unstable PHIL network to check for any improvement in the stability. Even though the system shows a stable operation in design, it is important to check its operation when employed in a real time system with an actual DUT. Since the application of PHIL in evaluating PE converters is common, this work follows the trend and presents the experimental validation of compensator to evaluate a PV micro-inverter. Also, a case study of a resistor divider network is presented to compare with the theoretical predictions.

5.7.1 A Case Study of Resistor Divider Network in PHIL

The system of resistor divider network in PHIL is shown in Figure 5.14. The compensator is designed based on (5.18) and implemented in RSCAD using a TF block. With the compensator, the layout of implementation is similar to that of Figure 5.17. To test the PHIL of resistor divider network, an AC voltage of 120 V (RMS), 60 Hz is applied at the input resistor in the software end which is transferred to the physical resistor through interfaces in between. The hardware resistor of 100 Ω is used and the resistance from the software end is varied to check the stability limit for a time step of 50 μs. This is done for both compensated and uncompensated system to highlight the advantage of the SP compensator.

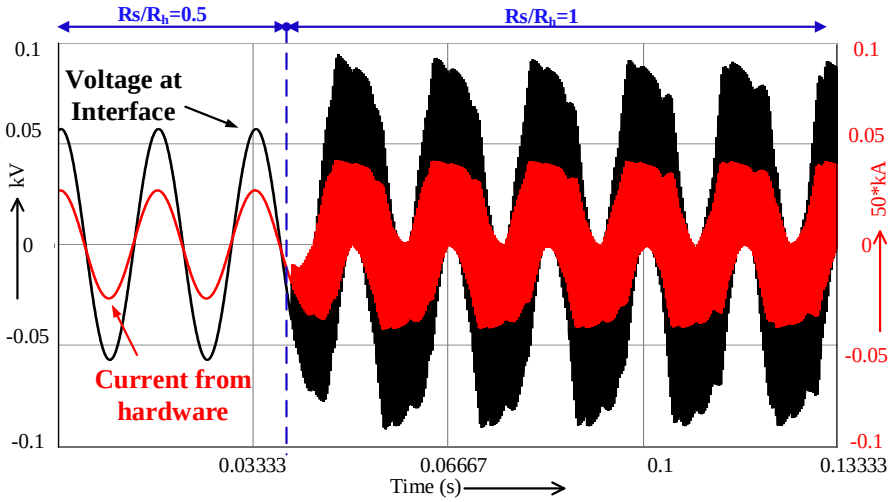
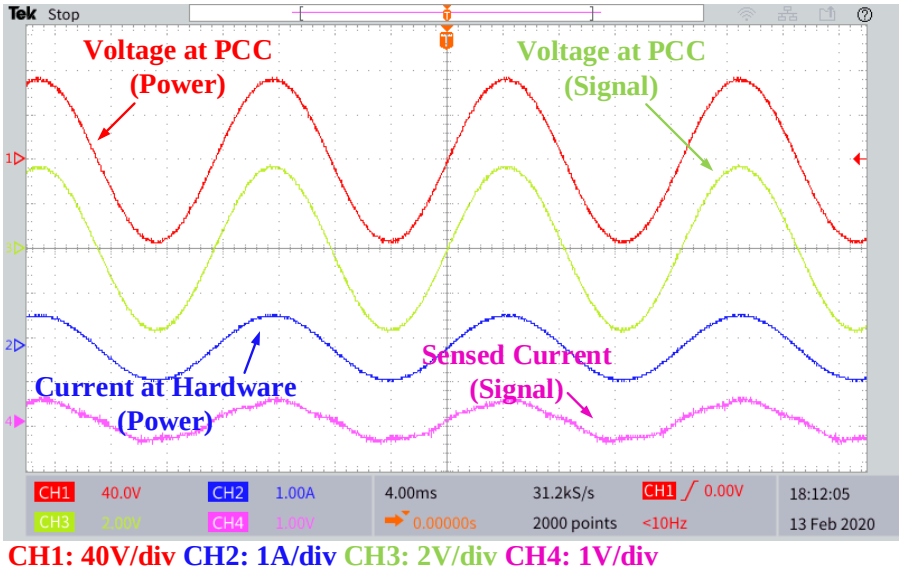


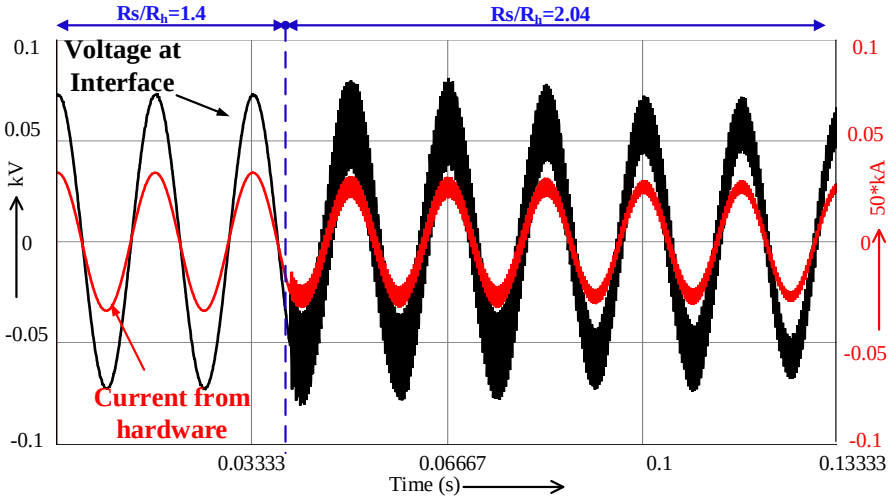
Figure 5.19 Uncompensated PHIL result for varying resistances ratio.

The waveforms in Figure 5.19 shows the result of a resistor divider network for resistor ratios of 0.5 and 1 for an uncompensated PHIL resistor divider. The input resistance is varied in real time and the system starts to show oscillation when the source and hardware resistances are equal. No further increase in the source resistance is made to avoid any potential damage to the system. Now, a similar set of experiment is repeated with the compensator in the PHIL network. To validate the theoretical response of Figure 5.18, the resistor ratio is set to 1.4 and the compensator is implemented with the TF block in RSCAD. As predicted, a stable PHIL is achieved in the real implementation as well. The results are shown in Figure 5.20. The experimental result from the hardware side for $R_s/R_h = 1.4$ is presented in Figure 5.20 (a) which shows a steady-state value of ~0.426. The error compared to the theoretical value is 2.4%. This is acceptable given the fact that actual hardware resistance used has a tolerance of ±5% and the voltage source in software has a small resistance of 1 Ω. With this, it is valid to claim an accurate performance of compensated PHIL. Further, to check the robustness of the system, the resistance ratio is increased until an oscillation is observed. As recorded in Figure

5.20 (b), system starts to exhibit an oscillatory response after $R_s/R_h = 2.04$. This proves a robust operation of the compensator as it operates stably to almost 1.5 times its designed value.



(a)



(b)

Figure 5.20 Compensated PHIL result (a) for R_s/R_h=1.4 (b) for increasing R_s/R_h.

5.7.2 A Case Study of Evaluating a PV Inverter in PHIL

The evaluation of a GCPI requires performing a steady state as well as transient performance during grid voltage change. Additionally, the performance of a PV inverter with weak grid is of particular interest as it comes with problems like, harmonic resonances and control loop interaction as mentioned in [94] and [95].

The PHIL scheme for evaluating a PV inverter is shown in Figure 4.16. A PV simulator from LabVolt is configured with 4 series and 45 parallel modules (total of 134.5 W maximum power) as an input to the PV micro-inverter (TI evaluation board) with L-C-L filter at the output. The grid is emulated inside the RTDS and the amplifier. The PHIL loop is completed with ITM interface. A resistor bank is connected at PCC of inverter and the grid to create a circulating power as well as to protect the amplifier from any potential unwanted situations similar to as discussed in Section 4.5.2. The experimental test set up for the system in Figure 4.16 is shown in Figure 5.21.

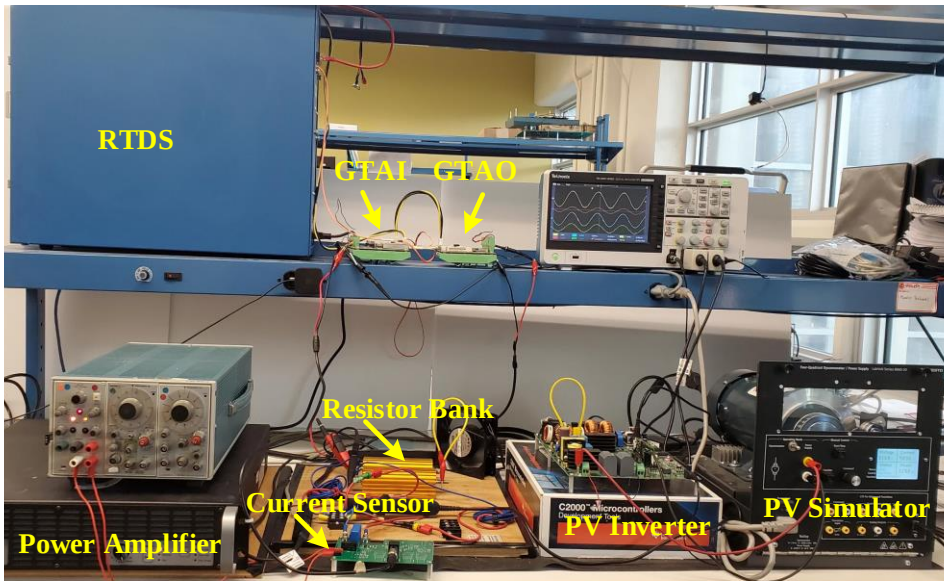
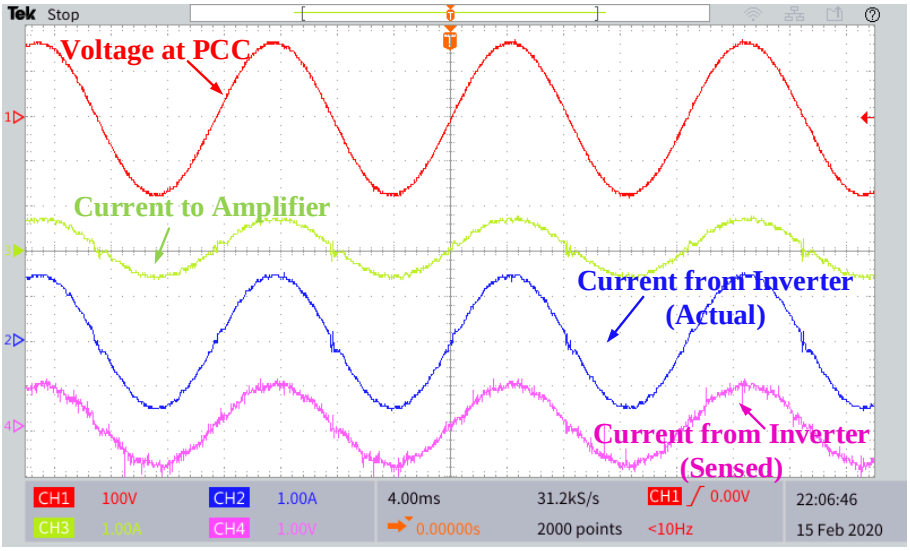
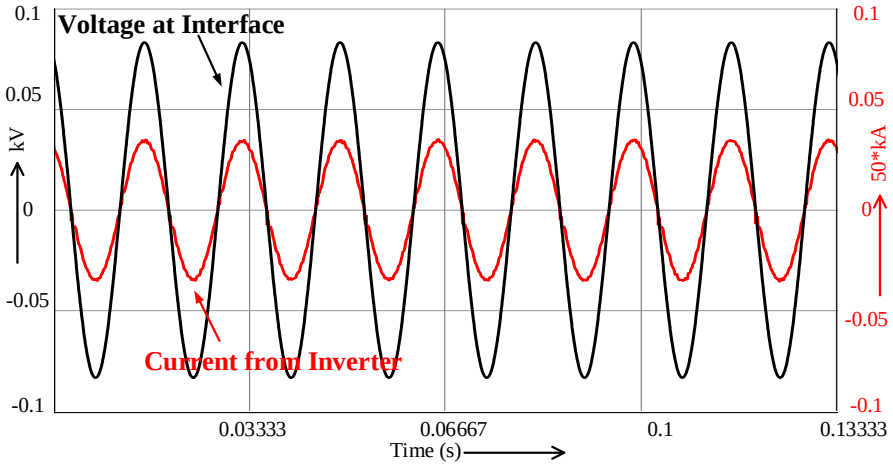


Figure 5.21 Experimental setup for PV inverter evaluation in PHIL.

Similar to the case study of resistor divider, first a compensator is designed considering the worst-case scenario with $R_s = R_h$. Once the compensator is designed, PV inverter can now be tested with strong and weak grid conditions. The SG is emulated in the RSCAD with a voltage source in series to a small resistance while the WG is emulated with inductor in series to a voltage source similar to what was done in Section 4.5.2.



(a)



(b)

Figure 5.22 PV inverter steady-state results with SG (a) measurement at actual inverter PCC (b) measurement at software node.

The steady-state performance of PV inverter in PHIL with SG is presented in Figure 5.22. The measurements are made at the inverter end as well as at the corresponding node in the software. During steady state, the PV with MPPT enabled, showed delivering 134.5 W. At the inverter end, it showed 125.69 W delivered to the grid out of which 75 W is consumed by the resistor bank and remaining is sunk-in by the amplifier. It is due to this reason, for PHIL applications, selection of amplifier is crucial and therefore a 4-quadrant amplifier is necessary. The steady-state performance of PV inverter in PHIL showed an efficiency of 95.15% which accounts for losses in the converter as well as in the voltage source resistors.

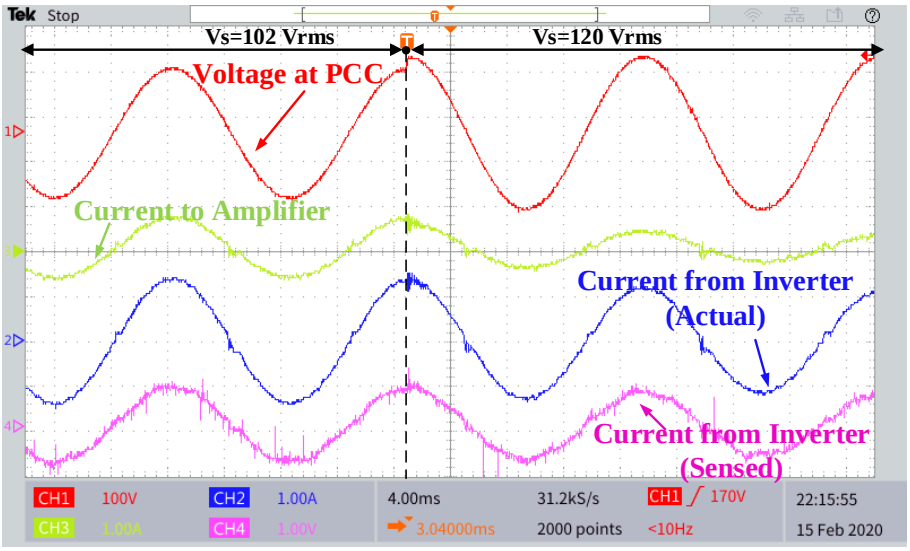
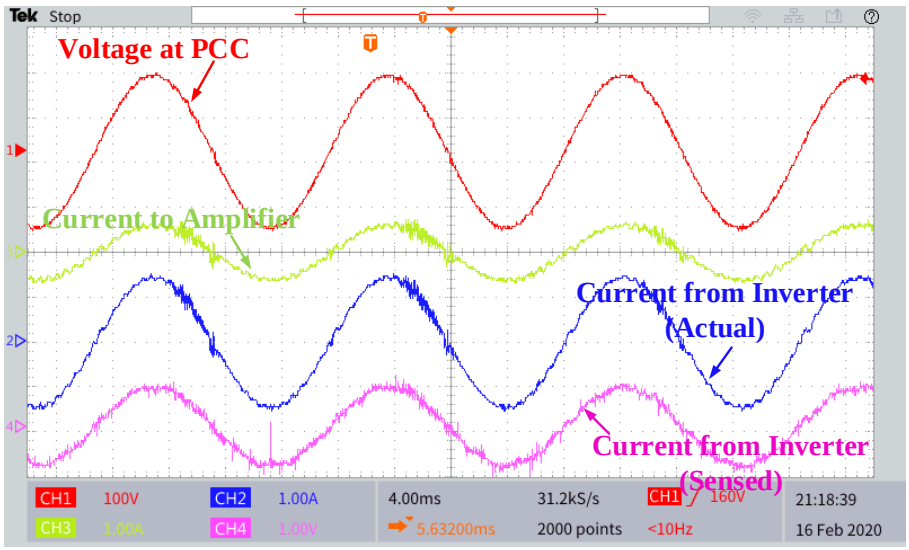


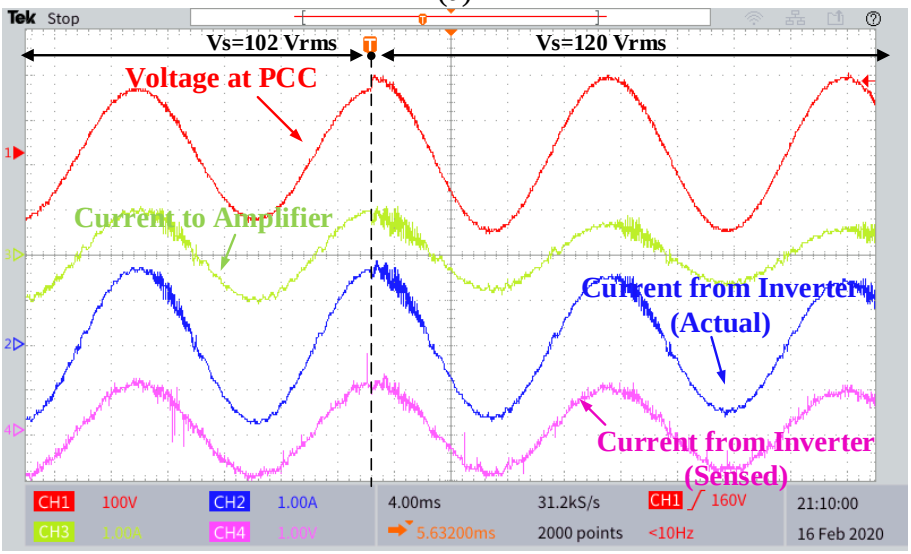
Figure 5.23 PV inverter during voltage swell with SG.

Similarly, PV inverter is tested during grid transient of 15% voltage swell (102 V_{rms} to 120 V_{rms}). The result is presented in Figure 5.23. As expected, the PV inverter responds to voltage swell by lowering the current to the grid to maintain the power.



CH1: 100V/div CH2: 1A/div CH3: 1A/div CH4: 1V/div

(a)



CH1: 100V/div CH2: 1A/div CH3: 1A/div CH4: 1V/div

(b)

Figure 5.24 PV inverter with WG (a) steady-state (b) transient.

Further, the PV inverter is tested with WG to evaluate its performance during steady-state and transients. The steady-state performance of PV inverter showed 123.45 W delivered to the grid against an input power of 134 W from the PV. The loss of 10.55 W (efficiency of 92.1%) accounts for converter losses, PHIL inaccuracies and the effect of additional grid

inductance in the current controller of the inverter. As also mentioned in [95], the current control of the PV inverter needs to incorporate the active damping scheme to damp out the harmonic resonances to achieve a superior current control scheme. The PV inverter under study lacks the active damping on its current controller and therefore it is expected to have a detrimental effect on the current waveform as the strength of the grid reduces. This can also be observed in the experimental results of Figure 5.24.

In Figure 5.24 (b), the PV inverter is operating in a weak grid during grid voltage transients and it shows a stable PHIL. This scheme with PHIL allows a systems engineer to design and test an actual PE renewable converter in a laboratory set up and the result obtained would reflect an actual like phenomena.

5.8. Summary of Chapter 5

This chapter presented a comprehensive model of ITM interface along with their experimental verifications. The developed model was further utilized to propose a smith predictor-based compensator for PHIL applications. The detailed design procedure along with the stability improvement of PHIL network with the proposed compensator was presented. The theoretical as well as the experimental verifications were made to highlight the performance of the proposed compensator. To validate the superior performance of the compensator, a PHIL setup was used to evaluate a linear as well as a non-linear DUT. A resistor divider network in PHIL was used as the case study to validate the operation of compensator with linear load. Similarly, a GCPI was evaluated with a compensator employed PHIL. Finally, the experimental results were presented which showed a good agreement with the theoretical predictions.

Moreover, it is also important to understand the effectiveness and limitations of such implementations. Theoretically, as long as the round-trip delay and the plant model of the overall PHIL system under investigation is accurately known, the compensator is able to eliminate the effect of the delay in the closed loop response. However, from the implementation point, for a measurement containing harmonic components (from the DUT in PHIL) fed into the real time model, it is essential that the time step of the simulator is well within the Nyquist limit to capture these dynamics. As the time step of the sub-circuit in real time increases, though the stability can be guaranteed with the compensator, the accuracy on the other hand is sacrificed. This is because of the fact that compensator employed closed loop PHIL system would still have a delay component present but pushed out of the feedback loop similar to what is shown in Figure 2.4 (b). Additionally, the investigation on the accuracy of the real time system model with different time step is an entirely different research area.

Chapter 6

A Fast Dynamic Switched-Mode Amplifier with 3-Level Switching

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The previous chapters in this thesis considered a linear amplifier for analyzing and evaluating a PHIL application. Also, it has been shown that the delay has a detrimental effect in the accuracy and stability of a PHIL. Moreover, the delay effect limitations so far reported is not due to the amplifier but the I/O cards. Having said that, the response time and bandwidth of amplifier are critical parameters to decide the choice of power amplification stage in a PHIL. Additionally, if a PHIL is conducted for high-power applications, the linear amplifier becomes unfeasible given its size and cost. The switched-mode amplifier finds its place in the PHIL loop for conducting high power PHIL tests. However, it is crucial that such switching amplifiers have a faster response to reflect the dynamics of an actual system. Considering this,

the purpose of the work in this chapter is to achieve a fast-dynamic response of a switched-mode amplifier with a Full Bridge (FB) inverter. The recommended solution and details of the work can be followed in the subsequent sections of the chapter.

6.1. Introduction

VSI is a well-known PE unit which has been widely employed to serve a variety of applications. The most common use of VSIs in industries are for devices such as Uninterrupted Power Supplies (UPS), Dynamic Voltage Restorers (DVR) and Active Voltage Conditioners (AVC) [96]-[100]. In a DC microgrid, VSIs basically acts as an interface between the DC grid and typical AC loads, such as household appliances [100]. To sum up the applications of VSI, it is mainly used to emulate an AC grid. It is therefore of utmost importance that output AC voltage be of highest quality. One of the other applications of VSI that is gaining popularity in recent times is its use as a switched-mode amplifier or a grid emulator for a PHIL testing [101], [102]. Applications as such requires a fast-dynamic performance of VSI. A typical FB VSI topology is shown in Figure 6.1.

The performance of VSI is largely dependent on the controller used to control its output voltage. One of the effects of control dynamics of a VSI is its impact in the Power Quality (PQ) of the emulated grid. Therefore, various fast-dynamic control schemes for VSIs have been proposed to shorten the transient period to get rid of any distortions seen in the output voltage. One of many ways to improve dynamic performance of the system is to go with a multiloop control system. Taking this into consideration Tzou and Jung [103] proposed a digital implementation of linear controller (PI) with current and voltage loop in a FB VSI. The performance comparison of existing multiloop linear controllers with other advanced control

like sliding mode, quasi-sliding and deadbeat controlling a VSI is tabulated in [104]. The sliding mode controller with fixed frequency proposed by Abrishamifar, Ahmad and Mohamadian [104] showed the shortest transient response time of *0.5 ms* in the comparison.

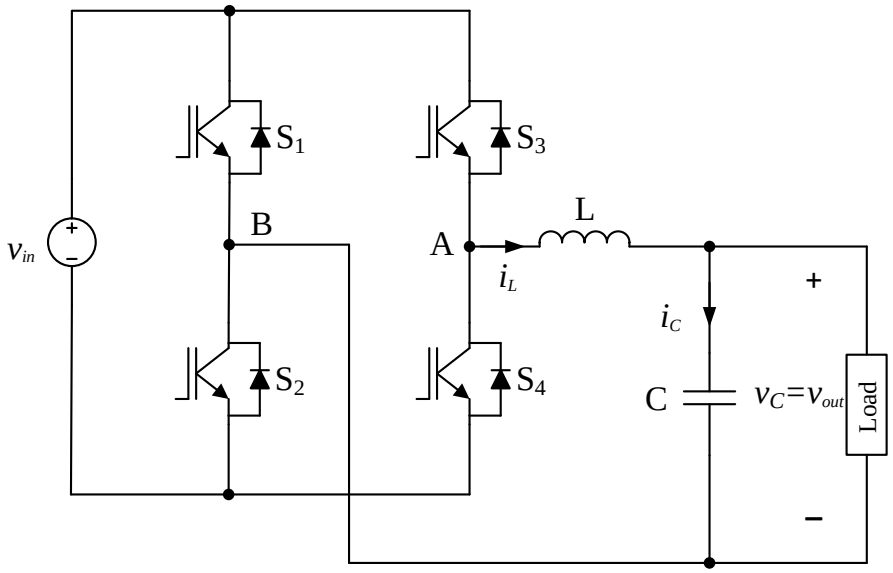


Figure 6.1 A typical full-bridge VSI.

Among various existing linear and non-linear controllers, the Boundary Control (BC) with Second order Switching Surface (SSS) offers a promising solution. The control scheme gives nearly the shortest transient time as it can predict the move of system switching trajectories [105]-[110]. Also, the implementation of such controller is relatively simple; it can be implemented using analog discrete devices [98] or digitally with a DSP [105]. Digital implementation of BC with SSS for a half-bridge VSI has been proposed by Au et al [105]. Similarly, a geometric approach to BC for implementing the control law for inverters is proposed in [106]. Basically, BC with SSS estimates the inherent state-trajectory of the converter with a second order polynomial. The state-trajectory estimation with BC can be made

with higher order switching surfaces too which is termed as “N-order” [107]. Different values of “N” result in different controllers and the estimation of the inherent state-trajectory is lowered with the lower orders. With N=0 and N=1, the N-order Switching Surface with BC (NSBC) reduces to well known Hysteresis control and Sliding Mode control respectively [107]. The NSBC requires the measurement of load impedance and hence an extra current sensor is required. It is also reported that NSBC has an improved transient response compared with SSS with BC [107]. Moreover, during the development of SSS control law, since the output current is assumed constant over a switching period, the load information is not required in the control law [111]. Therefore, this gives SSS with BC an extra edge due to implementation simplicity and also it gives a good approximation of inherent state-trajectory over the operating point.

The importance of power amplifier in the PHIL study is well demonstrated in Chapter 4 and Chapter 5. While the users can choose between a linear and a switched mode amplifier when conducting PHIL experiments but the choice in general depends on a lot of factors like power ratings, size, cost and performance. The major differences between these amplifiers are well documented in [112] and [113]. The linear amplifiers have a major disadvantage for high power applications due to its high costs and also high losses [112]. Similarly, switched-mode amplifiers are reported to have a slower response lower than 50 μs and also reduced bandwidths [112]. This is due to the limitations in the switching frequency of the semiconductor devices before the development of Silicon Carbide (SiC) and Gallium Nitride (GaN) devices as well as the restrictions on PWM based linear controllers. The bandwidth and response time may be pushed to higher levels with the use of SiC and GaN semiconductor switches, but this comes

at an expense of high switching frequencies. The work presented in this chapter addresses this research gap by applying a BC for a FB VSI operating with 3-level switching scheme.

6.2. Principle of Operation

The conventional sinusoidal based PWM switching control scheme of a FB VSI can be configured to operate either in a Bipolar (2-level) Switching Scheme (BSS) or Unipolar (3-level) Switching Scheme (USS) [114]. Due to the presence of two-switch pairs in each leg, as seen in Figure 6.1, the combination of these switches can result in the node A and B connected to either positive or negative terminals of the input. If voltage across node AB switches between positive and negative input, a BSS is achieved. Similarly, for USS, in addition to bipolar scheme like switching, both the nodes A and B can be connected to the same input node such that the voltage across AB is zero. This results in the voltage at AB switching between positive to zero in positive half cycle of the output and negative to zero in the negative half cycle of the output. The arrangement of Inductor (L) and Capacitor (C) achieves a low pass second order filter to get a clean sinusoidal output.

In contrary to a PWM based control scheme, control law like BC are based on the instantaneous values of the measurement at converter and the switching occurs whenever the system trajectory hits the set boundary. Hence, careful attention is required in the formulation of control law for a FB VSI to achieve switching schemes like bipolar or unipolar. Basically, SSS based BC is derived considering the steady-state characteristics of the converter. In order to simplify the control law, a BSS with a half bridge VSI is chosen and the results are presented in [105]. It is well known that using BSS in a FB inverter leads to a higher current ripple and consequently a larger inductor size and higher losses compared to a USS [115]-[118]. Although

multi-level switching scheme of BC with SSS has been proposed by Chan, Chung and Hui [119], it is for a general three-level topologies, for example Neutral Point Clamped (NPC), T-NPC and flying-caps topologies. If this is applied to a FB VSI, two semiconductor switches would work at higher switching frequency and other two semiconductor switches would work at line frequency thereby, causing the losses to concentrate on the high frequency switching devices. This leads to higher thermal stress on the devices thus requiring a larger cooling system. Thermal management is one of the critical design criteria in designing PE converter, for example, an AC grid emulator for DC microgrid applications as it requires higher power density to fit into a very small outlet box to convert a DC voltage to an AC voltage powered loads [120], [121]. This is also one of the desired characteristics of a switched-mode amplifier for high power applications.

This work presents the application of BC with SSS to achieve a USS for a FB VSI using a Finite state machine (FSM) method. The application of FSM allows to take the advantage of a fast-dynamic response of BC while keeping all the switches within their thermal limits. This is as a result of uniformly distributed switching signal given by the controller. The theory, concept and the implementation of a BC employed FB VSI with USS switching scheme is demonstrated in this chapter through a physical laboratory prototype.

6.2.1 Switching Pattern of a USS

The individual switches in VSI in Figure 6.1 can be controlled to operate it in a USS. However, it is to be ensured at all times that the switches in the same leg are complementary to avoid potential shorting of the input DC voltage. Another criterion that is to be satisfied during switching is to achieve uniform switching of all the semiconductor devices. With these

design criteria, the switching scheme of system in Figure 6.1 can be represented by a series of switching states shown in Figure 6.2. It is to be noted that the switching states are shown using an ideal switch for representative purposes only.

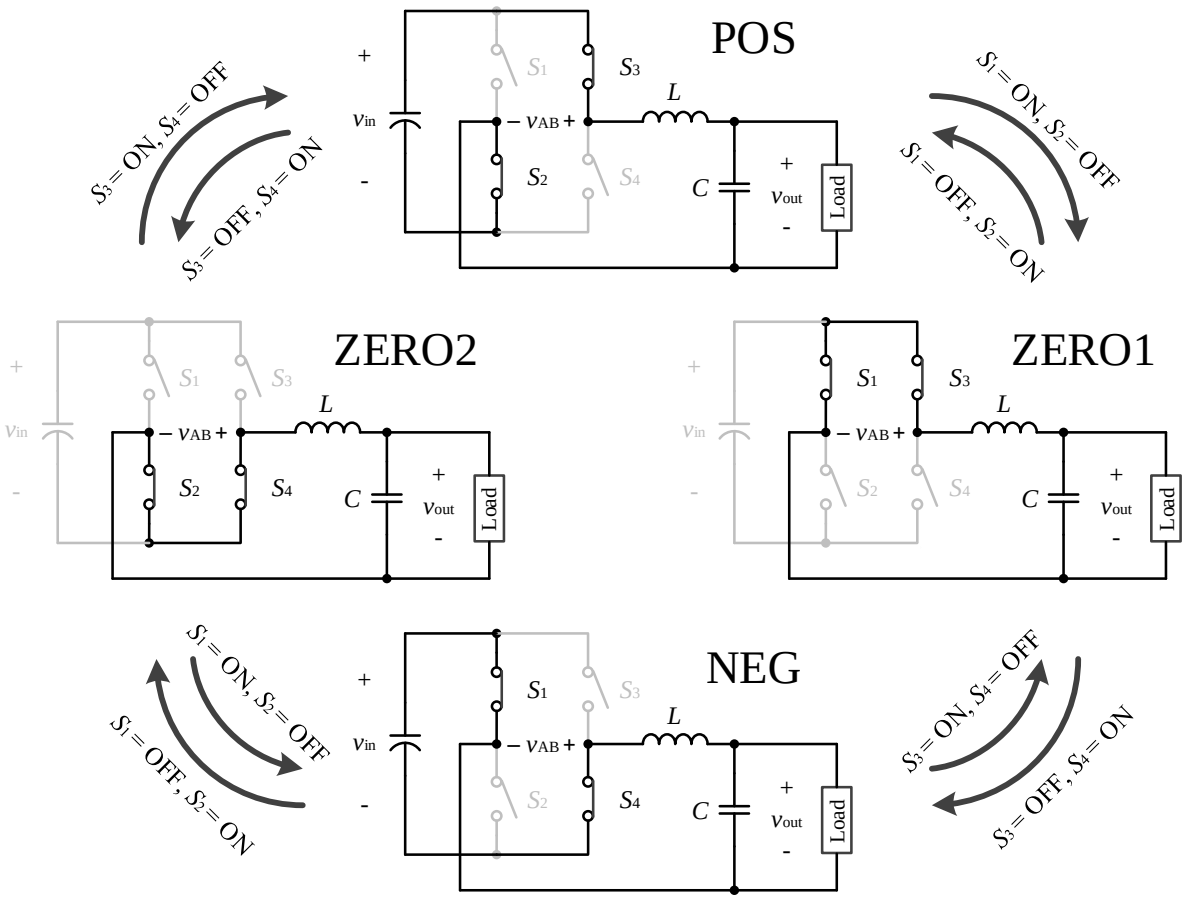


Figure 6.2 Unipolar switching scheme pattern with uniform switching.

The switching combinations shown in Figure 6.2 can be grouped under three states; (i) *positive*, where the positive input voltage is connected to the damped LC network, (ii) *zero*, where the damped LC network is connected to shorted input and (iii) *negative*, where the negative input voltage is connected to the damped LC network. The detailed analysis of the damped LC networks is in presented in [111]. To summarize, solution to these LC networks

would require solving a second-order ordinary differential equations which would eventually result in a set of three inherent state-trajectories of the FB VSI. The general equation combining these three states can be represented using state-space form and is given by (6.1).

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} v_{in} \tag{6.1}$$

The second term of (6.1) changes for each of the three states; for positive, zero and negative, v_{in} is $+v_{in}$, 0 and $-v_{in}$ respectively.

Once the switching pattern and the corresponding inherent trajectory of the switched state is determined to achieve a USS, it becomes evident to formulate the control law to estimate these trajectories for switching.

6.2.2 BC Law for Output Voltage Control with USS

The BC law with SSS has been employed to control the output voltage of a numerous converter topologies. The works presented in [122]-[124] forms the foundation of the development of BC law. Later, the work was picked by Leung and Chung [109] and a thorough analysis along with the development of control law and implementation of a buck converter was presented. The promising result with the buck converter attracted attention towards the use of BC law for other DC-DC converters [125]. Similarly, the control law has also been extended to use it with the inverters having output LC filters [98], [105]-[107]. Following the concept proposed in these papers, Hildebrandt [111] developed a boundary control law suitable for USS. In addition, the use of FSM in BC to allow uniform switching for VSI opens up a completely different area of research. The application of FSM with BC for USS has been demonstrated through theory and simulations in [111] but it fails to demonstrate the implementation of this combination in an actual prototype. Therefore, this chapter picks up the

work of [111] and implements the BC law with SSS integrated with an FSM to achieve a USS for a VSI. This VSI can be configured to work as a switched-mode amplifier whose architecture would look like what is show in Figure 6.3. The input in this case would be a v_{ref} as a signal and the amplified output as the v_{out}. The gain of amplifier depends on factors like LC filter parameters and ADC precisions.

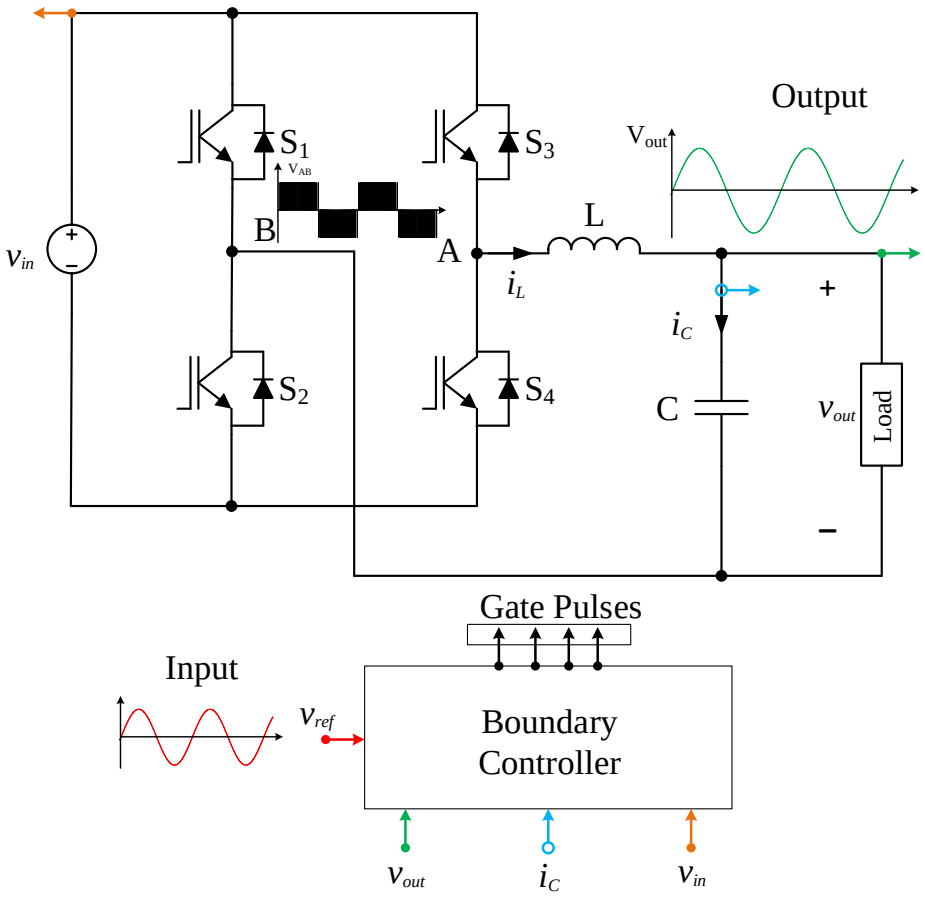


Figure 6.3 Architecture of a BC employed VSI.

This work focuses on demonstrating the fast-dynamic performance of the BC employed VSI with a 3-level switching. As the control law is formulated from steady-state characteristics of VSI, the steady-state waveforms can be drawn considering the switching states of Figure

6.2. The steady state switching cycle waveforms in Figure 6.4 shows the operation of a BC employed FB VSI working with USS.

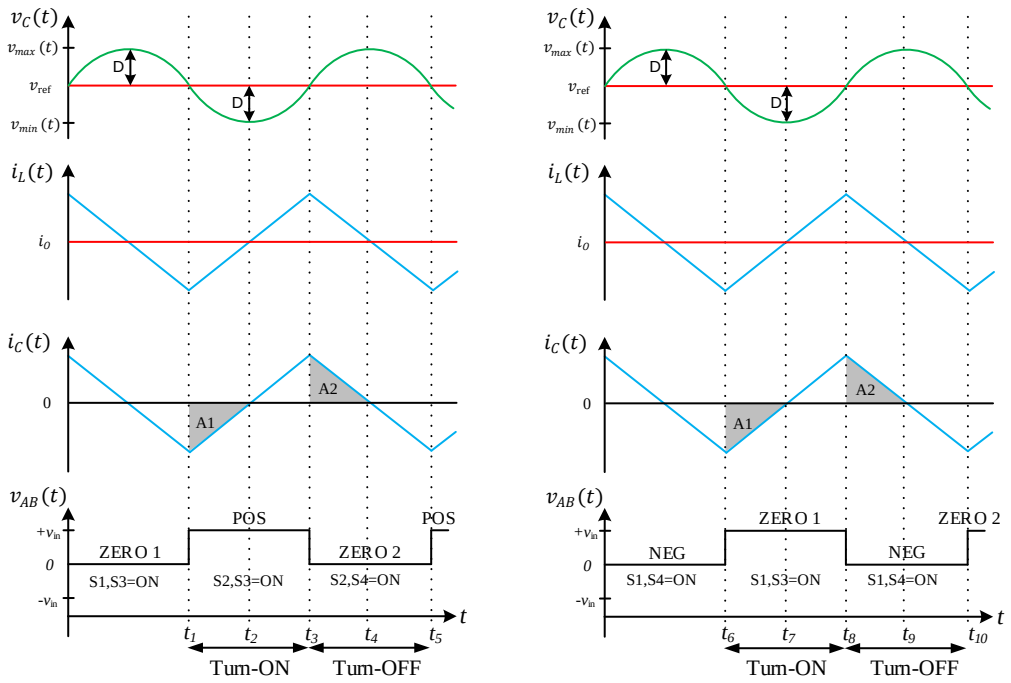


Figure 6.4 Steady state waveforms for (a) Mode I: $V_{ref}>0$ (b) Mode II: $V_{ref}<0$

From Figure 6.4 (a) for $v_{ref} > 0$ i.e., during the positive half cycle of the sinewave, if the controller gives Turn-ON action exactly at hypothesized time t_1, the output voltage ripple would not go below the set limit of v_{min} at time t_2 and similarly, the output voltage would not go beyond v_{max} at time t_4 if the controller actions to Turn-OFF the switch combinations at hypothesized time t_3. This cycle repeats to achieve a controlled output voltage while switching between positive and zero voltage across node AB. In a similar way, for negative half cycle of sinewave ($v_{ref} < 0$), the switching actions can be predicted to switch between negative voltage and zero across AB while achieving a controlled voltage as shown in Figure 6.4 (b).

With this, the BC law now can be derived for USS which follows similar principle of operation as that of a buck-converter and therefore similar approach can be used to derive the control law. Four different switching criteria can be determined based on switching instants dictated by the BC law using similar approach as in [98], [99], [105], [107]-[110]. The detailed derivation of the control law is shown in [111], and it has been reviewed and summarized below.

Control law for Mode I: when $v_{ref} > 0$; states switching between POS and ZERO (1 & 2) with reference to Figure 6.2 and steady-state waveforms of Figure 6.4 (a).

The Turn-ON equation at time t_1 such that a positive-state trajectory is estimated can be derived as;

$$v_C(t) \leq v_{\min}(t) + k_1(v_{\text{in}}, v_{\text{ref}}) \cdot {i_C}^2(t) \;\&\; i_C(t) < 0 \tag{6.2}$$

During this instant, the positive input voltage is connected across the LC terminal.

The Turn-OFF equation at time t_3 such that a zero-state trajectory is estimated can be derived as;

$$v_C(t) \geq v_{\max}(t) - k_2(v_{\text{ref}}) \cdot {i_C}^2(t) \;\&\; i_C(t) > 0 \tag{6.3}$$

During this instant, the LC terminal is connected across same point at the input such that $v_{AB} = 0\,V$. Important point here to be noted is that control law doesn't differentiate between two zero states, this feature is later integrated with FSM to achieve uniform switching.

Control law for Mode II: when $v_{ref} < 0$; states switching between NEG and ZERO (1 & 2) with reference to Figure 6.2 and steady-state waveforms of Figure 6.4 (b).

The Turn-ON equation at time t_6 such that a zero-state trajectory is estimated can be derived as;

$$v_C(t) \leq v_{\min}(t) - k_2(v_{\text{ref}}) \cdot {i_C}^2(t) \;\&\; i_C(t) < 0 \tag{6.4}$$

Similar to the Turn-OFF condition of Mode I, the control law is not able differentiate between two zero-states. The Turn-OFF equation at time t_8 such that a negative-state trajectory is estimated can be derived as;

$$v_C(t) \geq v_{\max}(t) - k_3(v_{\text{in}}, v_{\text{ref}}) \cdot {i_C}^2(t) \;\&\; i_C(t) > 0 \tag{6.5}$$

During this instant, the negative input voltage is connected across the LC terminal.

The definition of key parameters from (6.2) through (6.5) is;

$v_c = v_{out}$ = Output voltage,

$v_{max} = v_{ref} + \Delta$; where v_{ref} is the reference voltage and Δ the voltage hysteresis band,

$v_{min} = v_{ref} - \Delta$, i_C = Capacitor Current,

$k_1(v_{in}, v_{ref}) = \frac{L}{2C}\frac{1}{v_{\text{in}}(t) - v_{\text{ref}}(t)}$, $k_2(v_{ref}) = \frac{L}{2C}\frac{1}{v_{\text{ref}}(t)}$, $k_3(v_{in}, v_{ref}) = \frac{L}{2C}\frac{1}{v_{\text{in}}(t) + v_{\text{ref}}(t)}$.

Equation (6.2) through (6.5) is a second order polynomial which defines the switching surface in the state-plane of the VSI, hence the name SSS. The SSS has been defined by σ^2 in the literatures [107]-[110]. Figure 6.5 shows the plot of inherent trajectories in the state-plane obtained by solving (6.1) for three different inputs which represents the USS. Also, the σ^2 representing the BC law for USS is overlaid in the same state-plane. The upper boundary ($\sigma^2 + \Delta$) and lower boundary ($\sigma^2 - \Delta$) of the switching surface is shown for a know reference voltage. Families of similar switching surface boundaries can be obtained for a given reference voltage. This switching surface boundaries decides the switching action of the converter which would eventually glide the system operating point to settle at the intersection of the load line and system trajectory. The hysteresis voltage band allows the system to operate in the vicinity of the targeted operating point while eliminating the effects of chattering due to very high switching frequency. The parameters used to generate the plot of Figure 6.5 is tabulated below in Table 6.1.

Table 6.1 System parameter for the state-plane plot.

	VSI (Inherent Trajectories)				BC Law (σ^2)	
Parameter	Capacitor (C)	Inductor (L)	Load (R)	Input Voltage (v_{in})	Ref. Voltage (v_{ref})	Voltage Band (D)
Value	4.7 µF	7 mH	100 Ω	200 V	±120 V	5 V

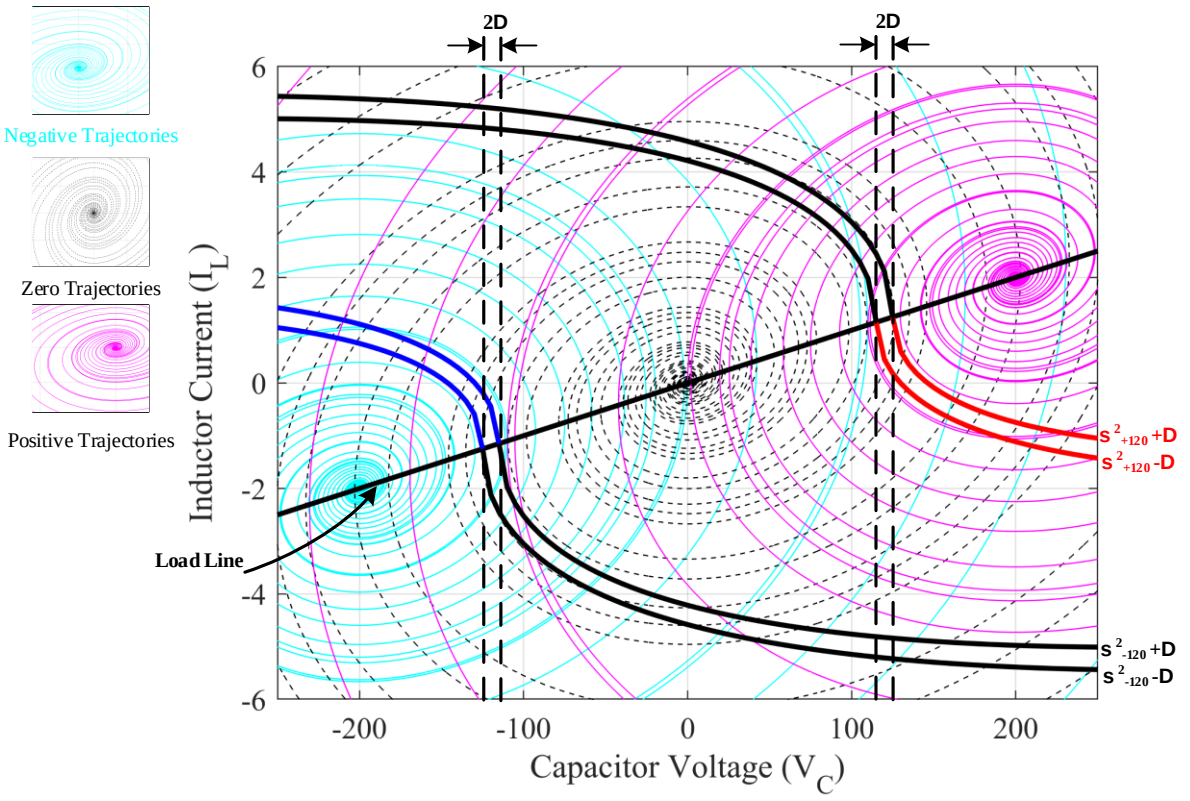


Figure 6.5 State-Plane representation of inherent trajectories along with switching surface.

6.3. Steady-State Characteristics

The steady-state characteristics of a BC employed VSI with USS defines the key operating parameters. Even though in the switching cycle, the FB VSI operation resembles that of a buck-converter, but the presence of time-varying output voltage creates a changing

operating condition. This can be represented by expressing the operating parameters mathematically in the following sections.

6.3.1 Duty Ratio

It is obvious that the duty ratio of an inverter would be a time varying quantity dependent on the position of the output voltage magnitude which is a varying sinusoidal quantity. At the same time, the operating principle of an inverter may be compared to that of a buck converter and the relation of duty cycle can be easily derived.

The output voltage of the inverter can be expressed taking into assumption the steady state output voltage equal to the reference voltage.

$$v_C(t) = v_{ref}(t) = V_m \sin \omega t$$

where, V_m is the peak value of the output sinusoidal voltage which is always less than or equal to the input DC voltage v_{in}.

As the voltage across node AB switches between $+v_{in}$ and $zero$, the output voltage after the LC filter is a positive half cycle of the sinusoid. Similarly, during the negative half cycle of the output the inverter is switching between $-v_{in}$ and $zero$. With this, the time varying duty cycle relation can be expressed by (6.6).

$$D(t) = \frac{V_m \sin \omega t}{v_{in}} \tag{6.6}$$

6.3.2 Inductor Current Ripple

The steady state inductor current ripple would vary with the duty cycle and output voltage. Basically, the slope of the rising or falling current of the inductor can be calculated to

have the estimate of inductor current ripple. Considering the positive half cycle of the output when the voltage through node AB is v_{in}, the rate of rise of inductor current can be known.

$$\frac{dI_L}{dt} = \frac{v_{in} - V_m \sin \omega t}{L} \Rightarrow \Delta I_L(t) = \left(\frac{v_{in} - V_m \sin \omega t}{L}\right) \frac{D(t)}{f_{sw}} \tag{6.7}$$

Now, considering a constant switching frequency (f_{sw}) and CCM of the inductor current as well as substituting (6.6) in (6.7).

$$\Delta I_L(t) = \frac{(v_{in} - V_m \sin \omega t) V_m \sin \omega t}{L\, f_{sw}\, v_{in}} \tag{6.8}$$

One important observation from (6.8) is that during the negative half cycle and when the node AB is connected to $-v_{in}$, the ripple from (6.8) gives a negative value indicating that the inductor current slope is decreasing while the magnitude would remain same for both the half cycles as long as the quantities like inductance, output voltage, duty cycle, switching frequency and input voltage remains unchanged.

6.3.3 Capacitor Voltage Ripple

The capacitor voltage ripple is controlled by BC defined by the hysteresis band, Δ. Therefore, for a voltage band defined by BC the steady state voltage ripple would be equal to 2Δ. Moreover, the steady-state characteristic of the converter would remain unchanged. Hence, the capacitor voltage ripple is the result of the contribution of the inductor current ripple. Also, the average capacitor current is equal to zero. With this, the capacitor voltage ripple can be calculated by finding the area under the capacitor current curve corresponding to where the voltage would change between maximum to minimum or vice versa. From Figure 6.4 (a) between time t_2 to t_4 the capacitor voltage ripple can be expressed as;

$$\Delta V_c(t) = \frac{1}{\mathrm{C}} \int_{t_2}^{t_4} i_c(t)\, dt \tag{6.9}$$

The capacitor current ripple is the inductor current ripple without the average load current. With this, the area under the capacitor current between time instants t_2 to t_4 can be computed.

$$A = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2} \tag{6.10}$$

Substituting (6.8) and (6.10) into (6.9) the voltage ripple equation can be derived.

$$\Delta V_c(t) = \frac{(v_{in} - V_m \sin \omega t)\, V_m \sin \omega t}{8\, L\, C\, {f_{sw}}^2\, v_{in}} \tag{6.11}$$

The equation (6.11) is valid as long as the parameters like v_{in}, v_c, L, C and f_{sw} is unchanged. From this expression, an important observation can be made by comparing the desired hysteresis band with the steady state voltage ripple given by (6.11).

$$\Delta = \frac{(v_{in} - V_m \sin \omega t)\, V_m \sin \omega t}{16\, L\, C\, {f_{sw}}^2\, v_{in}} \tag{6.12}$$

From (6.12) the steady-state hysteresis voltage band can be estimated. However, since the voltage band is fixed by BC law, it is desired that the voltage band is maintained at all times. To achieve this, the switching frequency of the system would vary to maintain this voltage band.

6.3.4 Switching Frequency

The equations for inductor current ripple (6.8) and capacitor voltage ripple (6.11) have reciprocate relation with the switching frequency. Therefore, if one is fixed the other varies with time. This way it is difficult to have the measure of switching frequency if the control objective is to maintain the voltage or current ripple.

A relation between the voltage band and switching frequency has been described by Yan et al. [108]. For Mode-I when $v_{ref} \geq 0$ the operation of VSI switching between positive and

zero trajectory is similar to that of a buck converter, except the time varying quantities. With this, the same relation is valid as derived in [108] with key parameters defined for VSI.

$$f_{sw}(t) = HK\Delta^{-0.5} \tag{6.13}$$

Where,

$$H = \frac{\left(v_{in} - v_{ref}\right) v_{ref}}{L\, v_{in}}$$

and,

$$K = \frac{\sqrt{k_1 k_2}}{\sqrt{2Dk_2} + \sqrt{2(1-D)k_1}}$$

The parameters in H and K are known from the steady state characteristics and BC law.

The above expression is valid only in the positive half cycle of the inverter because the control law is defined separately during negative half cycle. Similar equations can be derived for the negative half cycle when the node voltage across AB is switching between negative v_{in} and 0. The only change would be the variables H and K which can be expressed as below;

$$\left.\begin{aligned} H &= \frac{-\left(v_{in}+v_{ref}\right) v_{ref}}{L\, v_{in}} \\ K &= \frac{\sqrt{k_2 k_3}}{\sqrt{-2Dk_3}+\sqrt{2(1-D)k_2}} \end{aligned}\right\} \tag{6.14}$$

Detailed derivation of (6.14) is given in Appendix B.1.

Hence, the measure of average switching frequency can be estimated even if the voltage band is fixed.

6.4. Controller Design and Implementation

The control law has been implemented using TI F28M35H52C DSP. Figure 6.6 shows the block diagram of the designed controller. Three functional blocks are included; ADC,

digital control algorithm and FSM. Source voltage (v_{in}), filter capacitor current (i_C), reference voltage (v_{ref}) and capacitor voltage (v_C) are sampled at 300 kHz. An internally programmed voltage reference is used to generate a simple sinusoidal waveform for the purpose of verifying the control and topology operations. For the switched-mode amplifier operation, the reference voltage has to be fed in externally through the ADC. Subsequently, the digital values are evaluated in the digital control algorithm. The algorithm determines the switching criteria which decides the upcoming switching action based on the instantaneous values of the sensed signals. The algorithm comprises of two switching criteria each for Mode I and Mode II. Every ISR call is followed by the evaluation of one switching criteria. The output of the control algorithm is finally the decision based on trajectory to be taken; positive (coded "+1"), negative (coded "-1") or zero (coded "0").

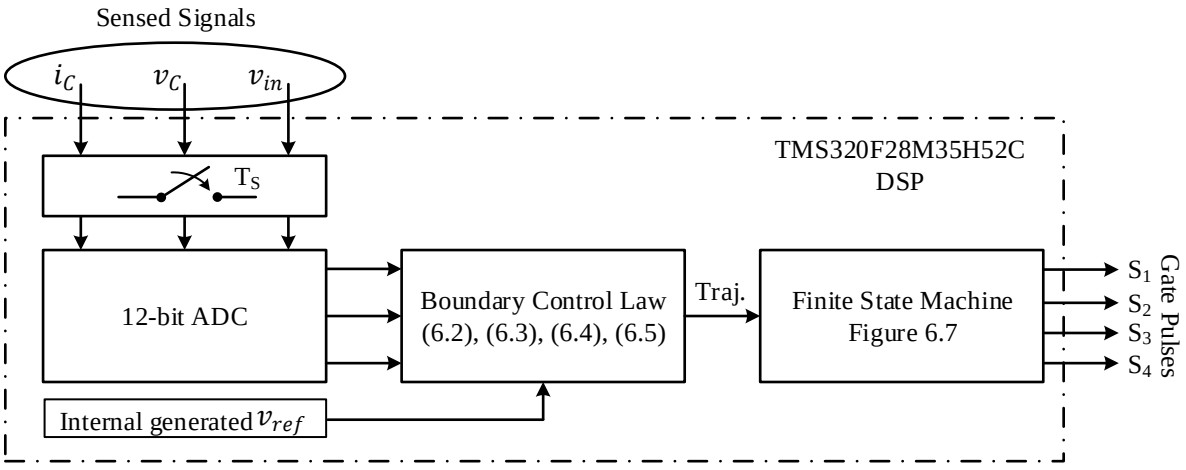


Figure 6.6 Controller operational sequence.

BC laws like SSS have no memory as their actions are based on instantaneous values only [108]. This allows easy implementation of such controllers either analog or digital. To

have uniform distribution of switching losses among all switches, the controller should keep track of previously used switch combination of the freewheeling state. Based on previous freewheeling switching state a decision is made by the controller to take alternative switch combination in the current state. This work implements the FSM method proposed in [111] to add this memory function without losing the inherent dynamics of SSS control law.

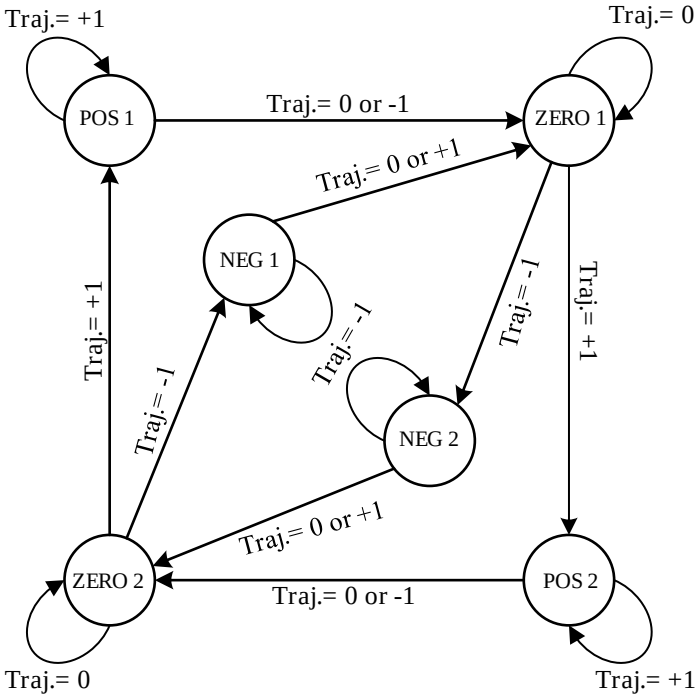


Figure 6.7 Finite State Machine for trajectory movements [111].

Figure 6.7 shows the state diagram in the FSM which handles the trajectory decision of the controller to generate necessary gate signals. The switching combinations of each states is shown in Figure 6.2. The output of ZERO1 state is complementary to the output of the state ZERO2 whereas the output of both POS states is identical, evenly the output of both NEG states is identical. As long as the output from control algorithm does not change, the state in

the FSM remain unchanged, so is the gate control signal generated by FSM. When a new criterion is satisfied, FSM changes both its state and output according to the trajectory decision. For instance, during Mode I, i.e. positive half of the reference voltage, the inverter switches between positive and zero state trajectory. This is dictated by the FSM incorporated BC law which ensures that the two zero states ZERO1 and ZERO2 always alternate between the POS1 and POS2 states. Similarly, the pattern is also followed during the negative half cycle of the reference where the zero states alternate between the NEG1 and NEG2 states. By doing this, FSM is forcing all the states to change uniformly thereby achieving uniform switching in both the branches.

6.5. Simulation and Experimental Results

Once the operation of VSI controlled by an SSS based BC is understood and the corresponding control law is developed, it is important to verify the theoretical formulations through a series of simulations and experiments. The subsequent section presents the various tests made to verify the controller operation which makes it suitable for applications requiring a fast-dynamic performance, for instance, an AC source or a switched-mode amplifier. The VSI parameter as tabulated in Table 6.1 is used for the verification.

6.5.1 Simulation Results with Boundary Controller

The performance and switching patterns of the BC employed FB VSI is verified through various simulations. Figure 6.8 (a) shows a simulation waveform of an inverter with BC operating under a sudden load change. The load change is made from 57 Ω to 97 Ω and back to 57 Ω again. This load change is made at the peak of the voltage waveform and can been

seen through the change in load current (I_{load}). The output voltage remains a pure sinusoid before and after the load transients. Also, the output capacitor voltage (v_C) is following the reference voltage (v_{ref}) at all times which demonstrates the superior tracking performance of the controller. The system is throughout operating with USS as shown by the node voltage across v_{AB}.

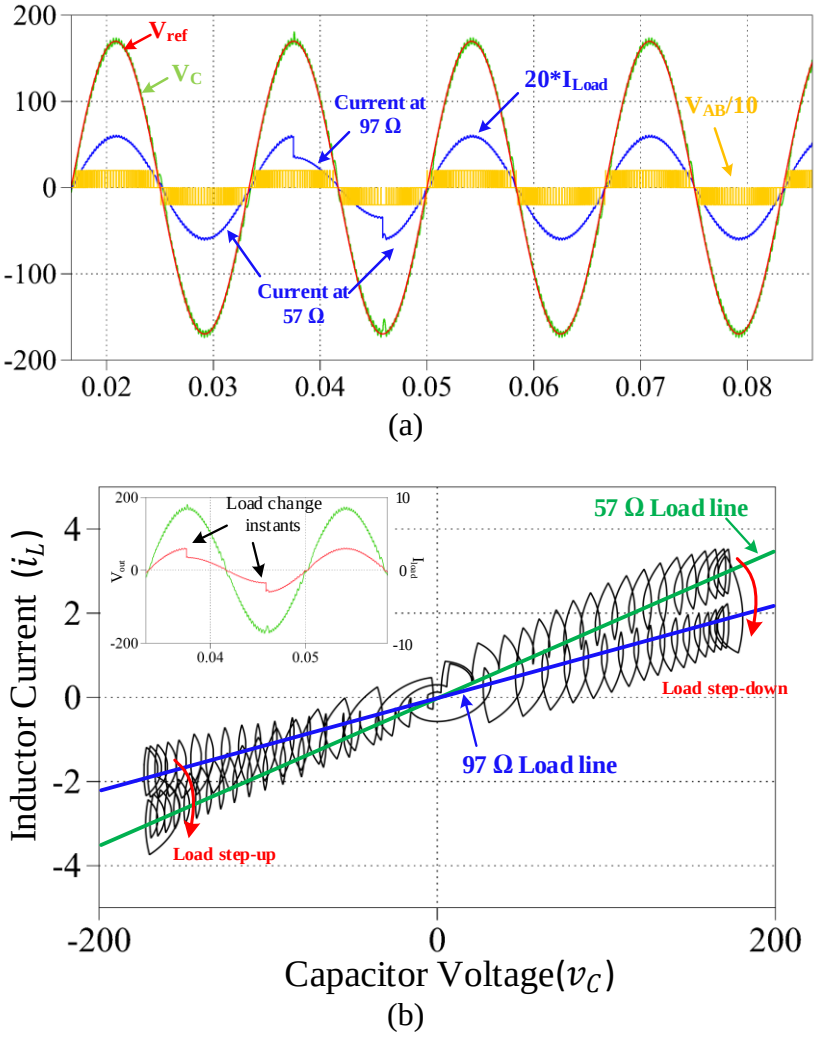


Figure 6.8 Simulation showing performance during load transients (a) time-domain plot (b) state-plane plot.

Figure 6.8 (b) shows the corresponding state-plane plot obtained by plotting a X-Y chart between inductor current and capacitor voltage. It illustrates that the inverter is initially operating in Mode I and is therefore operating with positive trajectory around a 57 Ω load line where at the peak of the reference voltage it encounters a load transient to 97 Ω. The system immediately follows this new load line and the system trajectory runs through a zero state to a negative trajectory (Mode II) where again at the peak of the negative voltage it experiences another large load transient to 57Ω. The controller immediately responds to this transient and starts following a new load line. The new steady state operating point is reached within two switching actions; read from the state-plane plot as each circle representing one switching cycle. Similar action is seen when the load transient (57 Ω to 97 Ω) occurs at the peak of positive half cycle. This shows a promising result of a BC based VSI as a strong prospect for an AC voltage source to achieve fast dynamic response.

Similarly, the tracking performance of the system can be validated by analyzing the reference changes. The reference voltage change is made at the peak of the sinusoid both at the positive and negative cycle. The load remains unchanged at 97 Ω and the reference is varied from 120 V_{rms} to 60 V_{rms} and back to 120 V_{rms} again. The results are presented in Figure 6.9. As seen from the time-domain plot in Figure 6.9 (a), the change in reference voltage is immediately followed by the measured output voltage. During the entire performance, the voltage at node v_{AB} shows the unipolar switching operation of the VSI. The state-plane plot during this reference transient operation is shown by Figure 6.9 (b). While the system is operating in Mode I with a positive reference voltage, it experiences a sudden reference change from 170 V peak to 85 V peak. The controller immediately responds by estimating the shortest trajectory to the new operating point. As seen in Figure 6.9 (b), the immediate action of the

controller is to lower the inductor current until it glides to the targeted voltage where it increases the inductor current again to follow the load line. This entire operation is achieved within a switching cycle. Similar operation can be seen when the reference change occurs again during the negative half cycle of the inverter. This shows a promising application of the BC employed VSI to be used as a switched-mode amplifier where the dynamics of the reference is required to be reflected by the hardware circuit within a shortest time span possible.

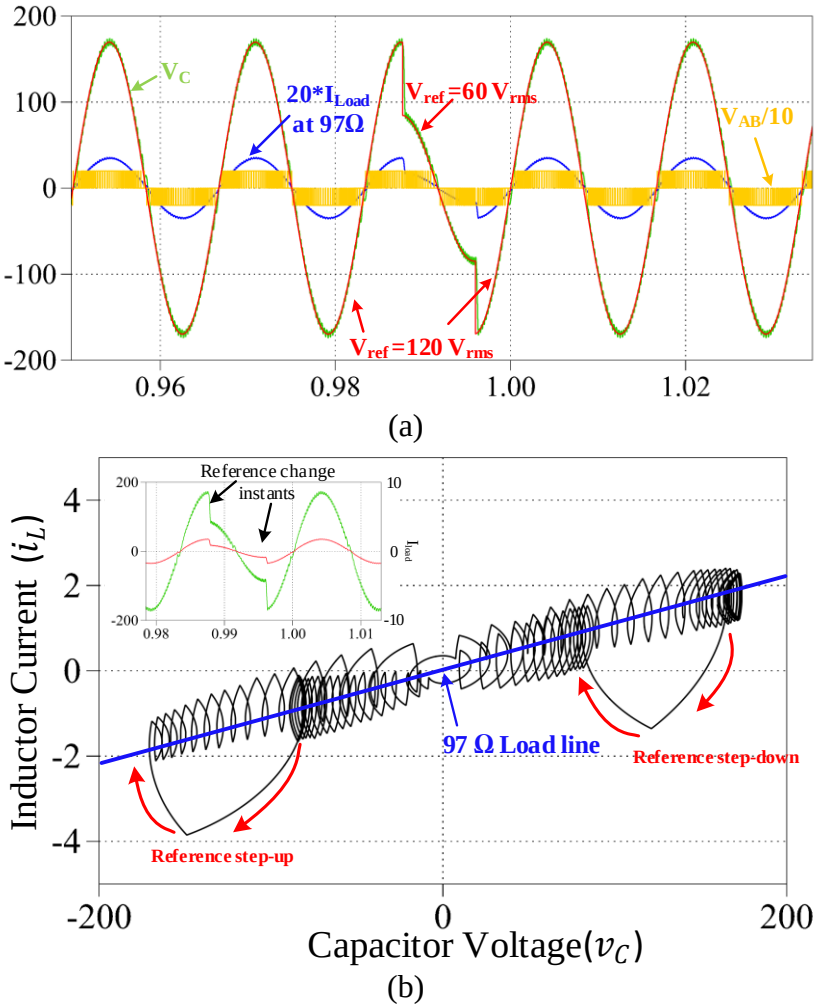


Figure 6.9 Simulation showing performance during reference transients (a) time-domain plot (b) state-plane plot.

6.5.2 Simulation Results with Conventional Controllers

To have a reference to validate the fast-dynamic performance of a BC based VSI, three simulation cases are made; one with a direct PI controller, second with a reference frame PI and final one with a Proportional Resonant (PR) controller. The key parameters along with the dynamic performance of these individual controllers are compared with the BC to evaluate the case.

6.5.2.1 Directly Implemented PI Controller

The simplified block diagram of a directly implemented PI controller is shown below in Figure 6.10. The inverter power stage is modelled using state space averaging technique and the controller parameters are chosen using frequency response accordingly. Using the designed parameters, the steady state and transient performance of the controller is recorded.

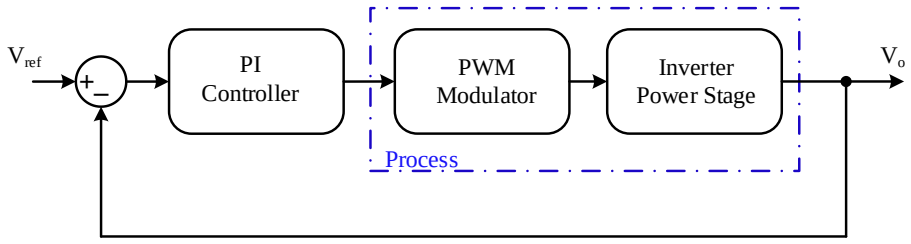


Figure 6.10 Output voltage control with a directly implemented PI.

6.5.2.2 PI Controller with Reference Frame Transformation

The PI controller in Figure 6.10 can be transformed into d-q reference frame by creating two orthogonal sinewaves. A transport delay of one quarter is used to create an orthogonal vector of the reference sinewave which is then converted to d-q axis frame using α-β to d-q

transformation. Similar approach is followed for the output measured sinewave. The reference d-axis, q-axis voltages and measured d-axis, q-axis voltages are fed to individual PI controllers. Since d and q axes are DC values, the use of PI controller on individual voltages would result in zero steady state error [126]. The simulation case of decoupled PI controller is made to study the steady state and transient performance of the controller. The block diagram of the implementation is shown in Figure 6.11.

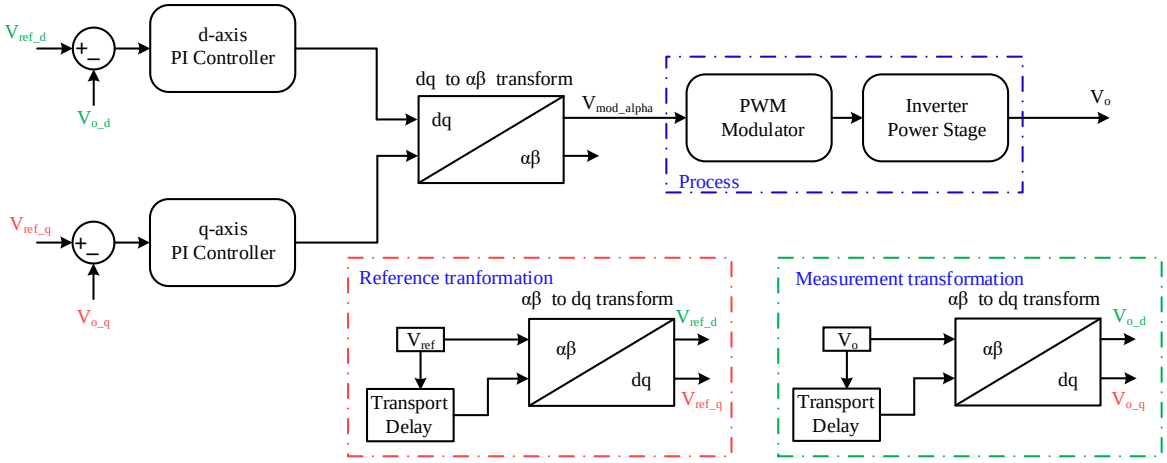


Figure 6.11 Output voltage control with a reference frame transform PI.

6.5.2.3 PR Controller

In terms of achieving zero steady state error PR controller acts the same way as a decoupled PI controller. A non-ideal PR controller is chosen for comparison due to its less sensitivity variation to resonance frequency drift. The transfer function of non-ideal PR controller is represented by equation (6.15) below;

$$G_{pr}(s) = K_p + \frac{2K_i\omega_c s}{s^2+2\omega_c s+\omega_o} \tag{6.15}$$

Where, K_p is the proportional gain, K_i is the integral gain, ω_o is the resonant frequency and ω_c is the cut-off frequency [127]. A simulation was made to study the performance of this controller with inverter. The system implementation setup is similar to that of a directly implemented PI controller.

Table 6.2 System performance with various controllers.

Parameters	**Controller Type**			
	PI	**Decoupled PI**	**PR**	**Boundary**
Steady State Error (%)	0.58	0.0431	0.071	Within the boundary specified
% Peak Overshoot	88.03	72.89	91.67	
Settling Time (2%)	2.82 ms	2.2 ms	2.06 ms	296 µs

Table 6.2 summarizes the performance of various controllers to control the output voltage of a FB VSI in unipolar operation. It is clearly seen that application of BC for a single-phase FB VSI with unipolar switching can result in a better transient tracking performance and at the same time have flexibility over other controller parameters.

6.5.3 Experimental Results

The experimental results present the steady-state and transient performance of a 550 VA FB VSI prototype equipped with TI F28M35x control card to program the control algorithm. The system is tested with various linear and non-linear loads to investigate its operation. The BC algorithm implemented in DSP follows the design and implementation methodology

explained in Section 6.4. In addition, a direct PI is also implemented to compare the system dynamics of an actual prototype. The specification of the prototype is given in Table 6.3.

Table 6.3 Specification of the VSI prototype.

Parameter	**Value**	**Parameter**	**Value**
Input Voltage (v_{in})	185 V	Output Filter Inductor (L)	7 mH
Output Voltage (v_{out})	120 V_{rms}	Output Filter Capacitor (C)	4.7 µF
Rated Power (P_O)	550 VA	Avg. Switching Frequency (f_{sw})	4 kHz

6.5.3.1 Steady State Operation with BC

Figure 6.12 shows the steady-state waveforms of the prototyped VSI working under different loadings. In Figure 6.12, Ch1 represents the capacitor voltage; Ch2 represents the voltage across the mid-points of two arms (v_{AB}); Ch3 represents the switching instant of the lower arm switch of branch A; and Ch4 represents the output load current.

The no-load operation of the VSI is presented in Figure 6.12 (a). The output voltage shows a purely sinusoidal voltage. The voltage across two arms (v_{AB}) shows that the system is in unipolar operating mode and the switching instant of the lower arm switch shows that it is switching in high frequency at all times. Figure 6.12 (b) shows waveforms when the system is running with a load resistance of 57 Ω (250 W). The output voltage is sinusoidal while the VSI is still in unipolar switching mode. Similarly, the result with an inductive load is shown in Figure 6.12 (c). The load is formed by an inductor and a resistor bank. It draws 550 VA with the measured Power Factor (P.f.) of 0.78. The output voltage is a purely sinusoidal wave maintaining unipolar switching operation.

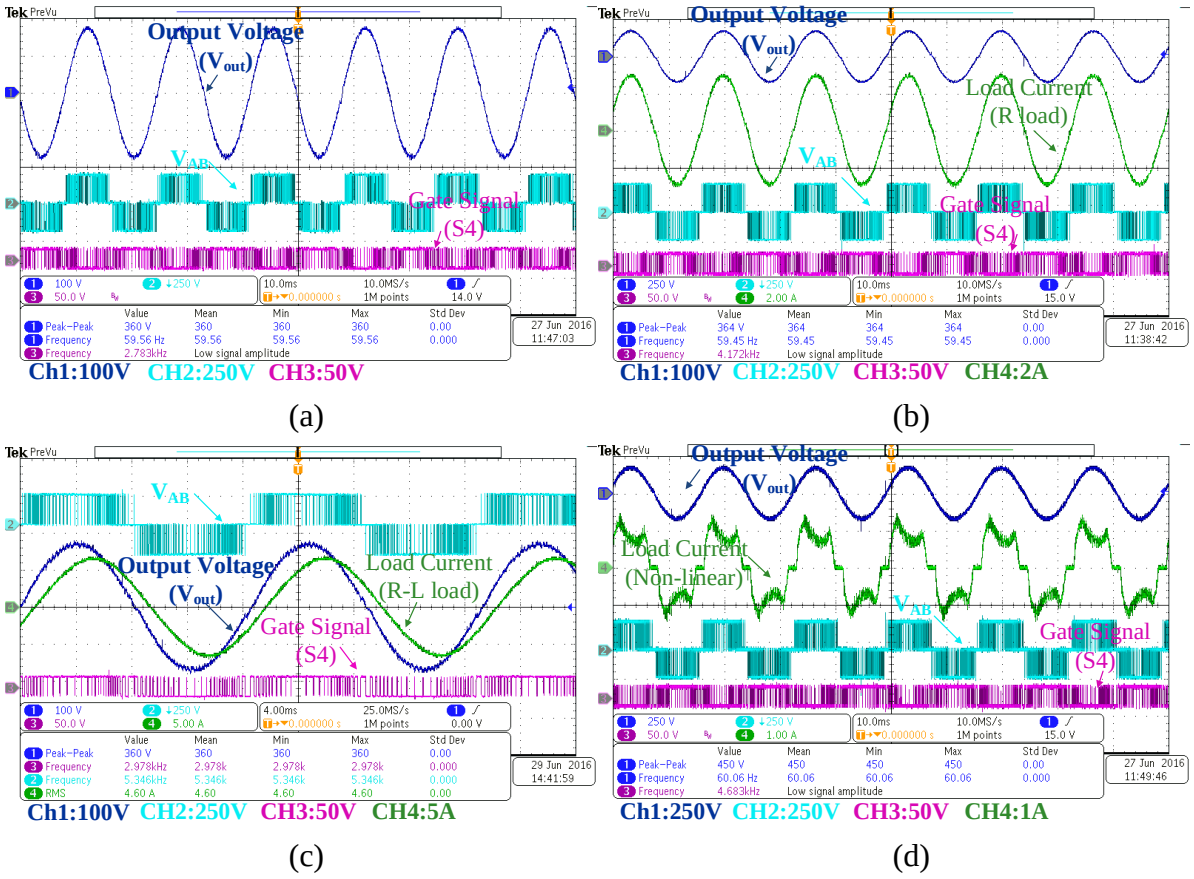


Figure 6.12 Steady-state operation of BC based VSI for (a) No-Load, (b) 250 W linear load, (c) 550 VA inductive load, and (d) 100 W non-linear load.

In order to verify the VSI application in a DC microgrid setup, 9 commercial 12 W LED light bulbs are connected at the output of the VSI. This is to replicate a conventional lighting network connected in a DC microgrid. Moreover, the front stage of the LED light bulbs is a diode bridge, and this is used to test the controller performance under non-linear loading characteristics. The waveforms are shown in Figure 6.12 (d). It shows that the output voltage is kept sinusoidal and without distortion.

The measured voltage Total Harmonic Distortion (THD) during all the steady-state operations are in the range of 1.27% to 1.5%. This signifies VSI providing a high-quality output

voltage under all loading conditions, at the same time remaining well below the limit specified by the international standard IEEE 519 [128]. The experimental results verified that the VSI with BC can operate to provide a high-quality sinusoidal voltage independent of the loading conditions. The sustained voltage output avoids any interference with the loads which would generate harmonic and subsequently contribute to higher losses in the loads.

6.5.3.2 Performance of BC During Load Transients

The controller operation for the load step is demonstrated through experimental results presented in Figure 6.13 which shows a step change of load from 97 Ω to 57 Ω (150 W to 250 W) and back to 97 Ω. The experimental result shows proper agreement with the theoretical predictions and simulations. The change in load step seeks for a new operating point which has to be determined by the controller. The experimental results show a fast-dynamic performance of the controller to reach a new stable operating point for a load step change. The results show that transients have no effect on the quality of output voltage waveform. The gate signals in Figure 6.13 show that the system works with unipolar switching. The time for controller to find a new operating point after the transient is recorded at 150-200µs.

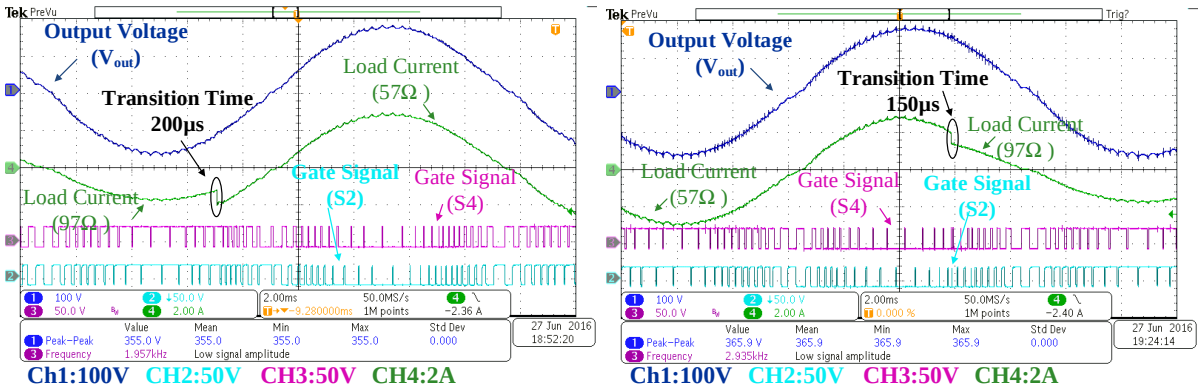


Figure 6.13 System performance during load transients: (a) 97Ω to 57Ω, and (b) 57Ω to 97Ω.

6.5.3.3 Performance of BC During Reference Transients

To have better understanding on operation and performance of the controller, controller response to a change in reference voltage can further be analyzed. Figure 6.14 shows waveforms when the output voltage reference changes from 120 V to 24 V with a 97 Ω linear load. Although it may not happen in an AC grid emulator for DC microgrids, but this is typically important in applications like switched-mode amplifier where the dynamic performance is of importance during reference transients.

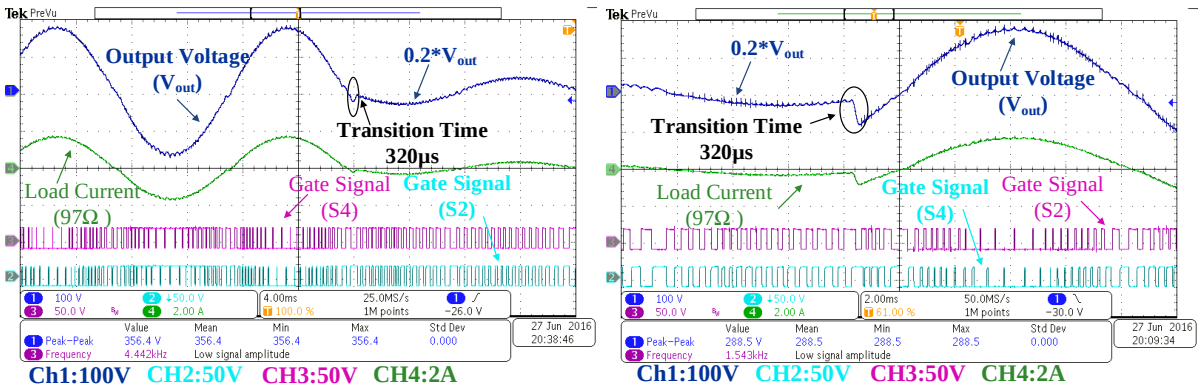


Figure 6.14 System performance during reference transients: (a) 120 V_{rms} to 24 V_{rms}, and (b) 24 V_{rms} to 120 V_{rms}.

The waveform of output voltage (Ch1) in Figure 6.14 follows the reference voltage change. It is to be noted that as the reference is generated through DSP, this change in reference is made internally. The load current (Ch 4) exactly follows the load voltage. The important thing here to be noticed is the performance of the controller even with a huge reference step of 80%. The controller finds the stable operating point within two switching actions and forcing the output voltage to reach to the desired value. This has been studied for both the case of

increasing and decreasing reference steps. The output voltage keeps sinusoidal without distortion and is stable before and after the transients.

The time taken by the system from the instant of reference change to finding a next steady state operating point is recorded at 320 μs. This is the time taken by the controller to find a new stable operating point. This is almost 10 times smaller compared to results from the conventional PI based controller scheme shown in Section 6.5.3.5 which has its transition time in range of few milliseconds. This can be a good standing point for stating the tight performance of the controller even under severe reference transient. This has also been verified through simulation results in Section 6.5.2 where the various controller parameters are analyzed under reference transients.

6.5.3.4 Performance of BC During Transients with Non-linear Load

To further demonstrate the performance of the controller, various tests are carried out even under non-linear loading conditions. For the sake of realization of non-linear load, nine 12 W LED lamps are connected in parallel with the provision of switching a group of 3 lamps each with one respective switch.

To study the transient performance of the controller due to non-linear loading step, one switch is turned on and off during different times and the results are recorded. Similarly, the controller performance is also recorded for change in reference steps. Figure 6.15 shows the response of the controller for a step change in load and reference voltage. For the step change in load, Figure 6.15 (b), the output is changed to the next corresponding stable operating point in a very short time. Similarly, for the case of change in reference voltage in Figure 6.15 (b), the output voltage tracks the reference voltage immediately. Two switching actions is enough

for the controller to reach to the next steady state operating point. Figure 6.15 (b) shows that the output voltage has a sudden change from 60V to 120V. The VSI reacts instantly without affecting the quality of output voltage before and after the transient.

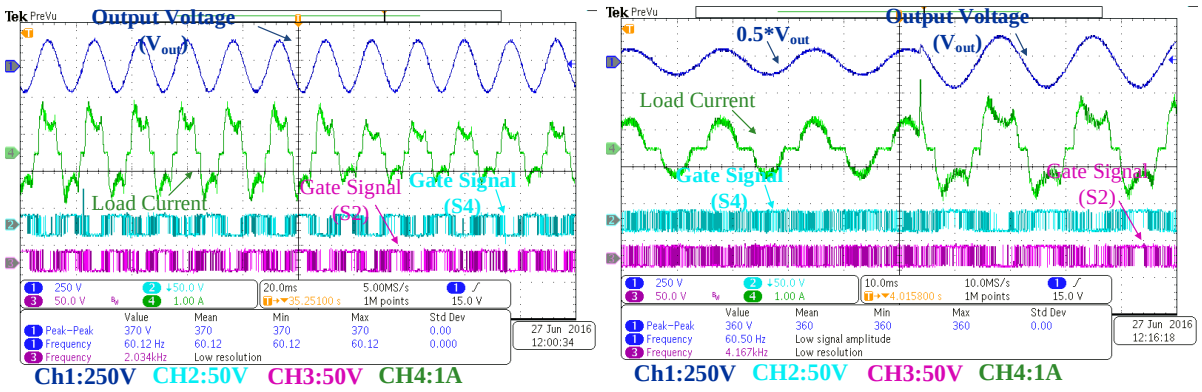
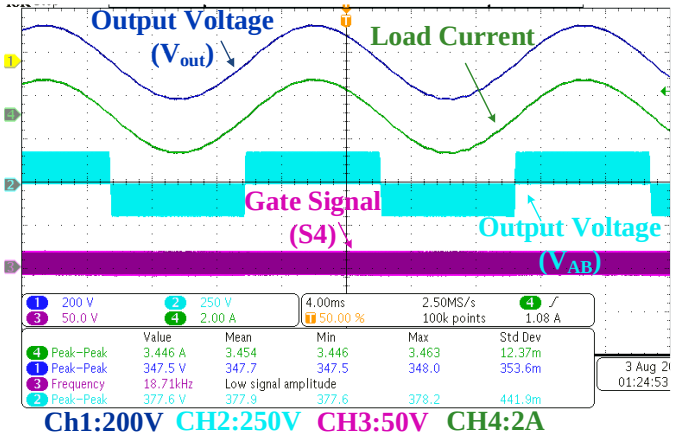


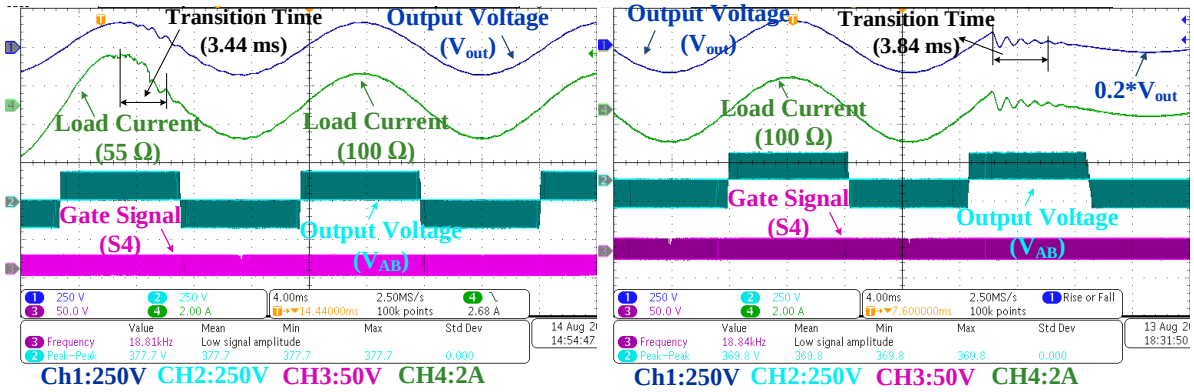
Figure 6.15 System performance with non-linear load: (a) load transient, and (b) reference transient.

6.5.3.5 Performance with a Conventional PI Controller

Unipolar FB VSI with a conventional PI based controller is simulated and accordingly implemented through a DSP as a benchmark case. Steady-state and transient performance of the controller is investigated under various operating scenarios. The steady-state operation of the system shows output voltage in track with the reference voltage. The stable performance of the system under both steady and transient conditions are shown in Figure 6.16. The dynamic performance of the system during load and reference change shows a transition time of 3.44ms (Figure 6.16 (b)) and 3.84ms (Figure 6.16 (c)) respectively. This is almost 10 times higher than what is achieved through a BC employed VSI despite the fact that PI based VSI is configured to run at almost four times the average switching frequency with which BC based VSI is operating.



(a)



(b) (c)

Figure 6.16 System performance with PI controller: (a) steady state, (b) load change and (c) reference change.

6.5.3.6 Performance Evaluation of BC based FB VSI

The dynamic performance of the BC based FB VSI operating in USS is demonstrated from sections 6.5.3.1 through 6.5.3.4. Further to analyze the performance of the system, THD and efficiency of the system is recorded under various loading conditions.

The efficiency of the system under leading, lagging and unity power factor conditions shows measurements above 95%, Table 6.4. Similarly, THD measurements under leading, lagging and unity power factor are recorded and shown in Table 6.4. The THD measurements are well

under 5% under all loading conditions. These measurements show the high-quality performance of BC when employed with a FB VSI operating with USS.

Table 6.4 Table of measurements.

Calculated	**Measured**			
P.f.	**P.f.**		**THD (%)**	**Efficiency (%)**
0.9727	0.9739	Leading	1.8830	95.95
0.9025	0.9072		1.8505	95.84
0.7234	0.7288		1.6371	95.36
0.5727	0.5829		1.4405	95.04
1	1	Unity	1.7025	97.75
1	1		1.9550	95.78
0.9651	0.9442	Lagging	1.6368	96.07
0.9888	0.9809		1.4750	97.58
0.8671	0.882		1.2407	98.98
0.6954	0.7373		1.4680	96.59

6.6. Discussions

The superiority of BC compared to the conventional linear controllers when employed to VSI operating with USS is well demonstrated through simulations and experiments in the above sections of this chapter. Also, it is shown that the dynamic response of the system with BC is less than 10 times with lower switching frequencies as compared to PI controller. Even

though this poses an exciting prospect to achieve improved response when the FB VSI with USS is operated as a switched-mode amplifier, the important notion however should be if the response time is comparable enough with its linear counterpart. From the experiments conducted to a 550 VA VSI prototype with DSP control card a response time of around 300 µs is observed with a switching frequency of around 4 kHz. What this suggests is, if the similar concept is implemented on a hardware platform that compliments the controller (BC) as well as the topology, higher switching frequency and hence better dynamic responses may be achieved. To demonstrate this case, a simulation is done which requires advanced hardware platform compared to the one in this work to replicate the simulation. The simulation results are presented to compare the performance of such switched-mode amplifier to the linear amplifier.

6.6.1 Comparison with Linear Amplifier

One of the factors that affects the stability and accuracy of a PHIL simulation is the delay. Therefore, the amplifier should have as minimum delay as possible if it is to be used in PHIL experiments. Besides, the transient response is also of importance as it decides the response time of the overall PHIL simulation. Considering this, a step response of the switched mode amplifier is simulated and the parameters like delay and transient response is recorded.

Table 6.5 Simulation parameters for measuring step response of switched-mode amplifier.

Parameter	**ADC Sampling**	**Inductor (L)**	**Capacitor (C)**	**Avg. Switching Freq.**
Value	1.2 MHz	800 µH	1 µF	18.75 kHz

Figure 6.17 shows the simulation results for the step response of a BC employed FB VSI operating with USS for the parameters tabulated in Table 6.5. Comparing this result with the linear amplifier of section 5.4.2 with delay around 0.7 µs and step response close to 4 µs, the delay of 1.66 µs with transient time of 39.1 µs for switched-mode is a remarkable improvement that allows possibility for further reducing these numbers with the selection of proper hardware. This just shows the conceptual validation that BC employed FB VSI with USS can function to closely match the specifications as that of a linear amplifier. However, there are certain limitations of such scheme when it comes to implementation which is discussed in the section below in detail.

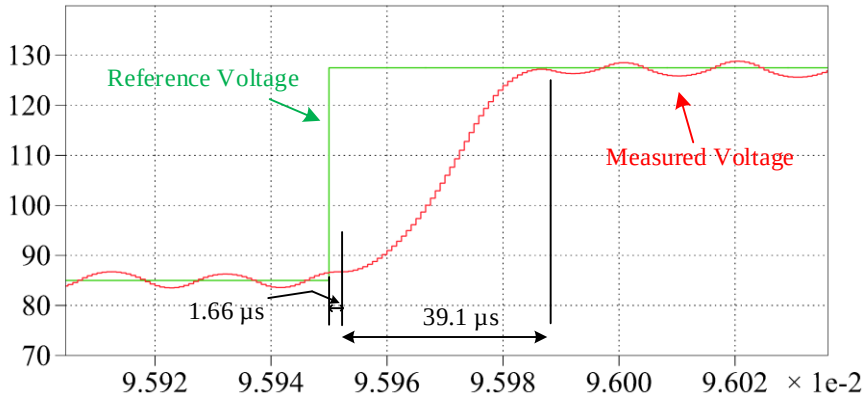


Figure 6.17 Step response of a switched-mode amplifier.

One of the noticeable works in switched amplifier design is presented in [129] which proposes a Class-D amplifier with a VSI as power stage and a PID controller as its control structure as an interface amplifier for PHIL study. However, with this design, the maximum bandwidth of the system is dependent on the maximum frequency that the switches can withstand. Even with a 50 kHz switching frequency the bandwidth of system is reported only about 3.5 kHz (45.7 µs) [129]. Comparing this with the BC employed PHIL amplifier

discussed in this chapter, a shorter transient time is achieved without going ultra high switching frequency. The relatively low switching frequency operation helps reduce the switching losses. Additionally, the FSM guarantees that all the switches are uniformly switching which aids in thermal management. All these advantages help BC as an ideal controller choice for amplifier application.

6.6.2 Limitations

The benefits of BC have been presented in great details in the previous sections which makes it a better choice as a controller for switched-mode amplifier. However, the implementation of BC based FB VSI operating with USS suffers from certain limitations that need to be considered before the prototype can be applied as a switched-mode amplifier for a PHIL setup.

The major consideration for employing a BC law is the sampling time of the measured signal required for the control law as well as the computation time. From the simulation parameters in Table 6.5, it can be justified that the switching frequency of the system can be pushed further with proper choice of parameters like sampling frequency, L and C. Therefore, a high precision ADC with higher sampling is one of the requirements for achieving a faster response time suitable for using such setup as a switched-mode amplifier. Since DSP is used for implementing the controller in this thesis, it does not meet the requirement mentioned above. Moreover, the work presented in this thesis is a conceptual demonstration which opens up a new research area in the field of designing such high performance switched-mode amplifier. With the use of more advanced hardware like a high precision and high sampling rate ADC, a Field Programmable Gate Arrays (FPGA) for implementing control law and use

of SiC/GaN semiconductor switches, the conceptual demonstration in this thesis can be easily extended to a more practical solution that can achieve the specifications as close to the linear amplifiers.

6.7. Summary of Chapter 6

This chapter presented a detailed analysis and performance of a FB VSI which qualifies to work as a switched-mode amplifier. The work presented in this chapter could be a framework for potential future switched-mode amplifier for PHIL applications. The fast-dynamic requirement of switched-mode amplifier is achieved through the application of an SSS based BC to a FB VSI operating with a USS. The controller performance was evaluated with various linear and non-linear loads during steady-state and transient operation. The fast-dynamic performance of the controller was validated through numerous simulations and experiments. The dynamic response of the BC employed VSI was compared with the conventional controllers which showed the superior performance of BC. The theoretical formulations were successfully verified through implementation of controller in a digital platform applied to a 550 VA VSI prototype. Since the stable operating point after transients is achieved within 1-2 switching actions, the dynamic performance of the system can be further improved by increasing the switching frequency. Therefore, the work presented in this chapter can be further extended with advanced hardware to design a high switching frequency system to improve the dynamic response which is ideal for switched-mode amplifiers.

Chapter 7

Conclusion and Possibility of Future Extensions

This thesis presented a thorough analysis of the PHIL instability while evaluating a PE DUT. While the existing research in PHIL is still in its preliminary phase, the application of PHIL for evaluating linear and non-linear devices is growing rapidly. Due to this, work presented in this thesis aims at analyzing various aspects while interfacing an actual hardware with a real time system model. Additionally, as the system size grows, the need for a switched-mode amplifier becomes apparent. Considering this, the work presented in this thesis comprise of a switched-mode amplifier design and implementation that could form the basis of future such amplifiers.

7.1. Conclusion and Major Contribution

The result of the work from this thesis contains a workflow that is broken down into chapters to investigate the issues leading towards stability concerns for a PHIL system. The individual chapter covers a comprehensive analysis of the various research aspects in PHIL setting. These individual chapters consist of a theoretical background followed by a

mathematical model development and finally validating the theoretical predications through a series of experiments to fulfill the research objectives.

To be able to understand how the interfacing of the chosen RTS, in this case RTDS, works as well as to familiarize with the overall system, in Chapter 3 a CHIL setup is configured to validate the controllers of a PV array in a DC optimizer. A comprehensive small-signal model of an MBC is developed, and the model is verified with a CHIL. The results from the model and experiments showed a close agreement.

Once the operation of the RTDS along with its interface is known, in Chapter 4, a PHIL system is formed with an ITM interface for a resistor divider network. The model of individual interface devices is taken to represent the PHIL network by a standard control block. With the control block representation containing parameters of interface devices and the time-step delay of the RTDS, a R-H criterion is used to formulate a set of inequalities to analyze the stability. This allowed to propose a methodical step by step approach to work with a stable PHIL. The quantitative formulation of the stability with R-H criteria could help choose the right interface parameters to ensure a stable PHIL. Additionally, a compensator design methodology is also presented in this chapter which is employed in two actual PHIL network cases, a resistor divider and a GCPI, to verify the theory and mathematics.

In Chapter 4, the in-depth stability analysis of a PHIL network is presented based on the existing interface device models. The accuracy of these interface models is not validated. Therefore, in Chapter 5 a model of individual interface devices is developed and verified experimentally. From Chapter 4 the effect of delay in the stability is well known. Hence, a Smith Predictor compensator is designed that eliminates the effect of delay in the closed loop

response of a PHIL network. This is verified theoretically and experimentally to evaluate a GCPI.

Besides the detailed investigation of stability of a PHIL network, this thesis also presents the work that could form the basis for designing a switched-mode amplifier. The work presented in Chapter 6 utilizes a FB VSI as the power stage of the switched-mode amplifier. Since such amplifiers have a poor dynamic response as compared to the linear ones, a suitable controller is required to boost the dynamic performance. In this work, an SSS based BC is applied to operate the FB VSI in a unipolar operation. The performance of the FB VSI with BC is evaluated under severe load and set-point transients. Various simulations and experimental results are presented to verify the fast-dynamic operation of the FB VSI which sees a big improvement in the dynamic response in the same inverter platform with the same power level, topology, switching frequency and semiconductor switches.

With the contributions listed below arising from the set of chapters compiled to form this thesis, it can be concluded that the objective of this thesis has been achieved.

1. A comprehensive small-signal model of the PV array along with their respective controllers is developed and then experimentally verified with a CHIL testing approach. To the best of author's knowledge, such model development and verification approach has not been reported in the existing literatures.
2. A mathematical formulation to quantitatively analyze the stability of a PHIL network is proposed in this thesis. The mathematical formulation considers various parameters of the interface that could guarantee the stability of a PHIL network. Besides, this thesis also contributes in designing a compensator to improve the stability margin.

3. The interface device models in ITM interface are developed considering an operational sequence and the developed models are verified experimentally. Such experimentally verified models is one of the contributions of this thesis.
4. The delay has an effect of degrading the stability margin of a PHIL system. This thesis contributes to eliminate the effect of delay in the closed loop response of the PHIL network by employing a SP compensator. The use of SP for PHIL systems in this thesis is the first such reported application.
5. This thesis contributes in designing and implementing a switched-mode amplifier with a FB VSI operating with a unipolar switching controlled by an SSS based BC. Such switched-mode amplifier would have a fast-dynamic response which is desired for a switched-mode amplifier in a PHIL setup.

7.2. Possible Future Extensions

The applications like PHIL testing can be foreseen to gain more and more popularity in the industrial settings. With this demand, the research aspect in PHIL is vital towards understanding various uncertainties in the area. The work presented in this thesis could open up a new research direction with following possible extensions;

1. The work in Chapter 3 to validate the PV controllers is limited by the system model inside the RTDS which cannot guarantee its accuracy above 3 kHz switching frequency. With this, the delay between the control signal and actual measurement would have a minimal effect in the control system performance. Moreover, to replicate the actual PE converters operating at high switching frequency, one of the

possible research options would be to find the proper modelling approach which could handle such high switching frequencies.

2. The quantitative stability analysis of a PHIL network as well as the delay elimination with SP is formulated with a linear amplifier having a high bandwidth. Further research can be done to evaluate the system with a switched-mode amplifier. This research could be formulated as; first the interface model can be developed and experimentally verified considering a switched-mode amplifier, and the mathematical formulations can be carried out in a way similar to Chapter 4. Further, the research can be extended to a digital interface instead of an analogue. With this, the delays due to conversion in ADC can be avoided but it requires a digital interface protocol to connect the amplifier (either linear or switched mode).
3. In Chapter 5, the application of SP in a PHIL setup is first introduced. There are many different variants of SP compensator. The comparative analysis of applications of these variants could be another possible extension to the work presented in this thesis.
4. The work in Chapter 6 presents the implementation of an SSS based BC to operate a FB VSI in USS. This work presents an important framework to design a future fast-dynamic switched-mode power amplifier. The controller like BC decides the switching instant of the converter based on the instantaneous value of the measurements. Due to this, the dynamics of the controller is dependent on the sampling of the ADC in the digital control card. With this it is fair to assume that the dynamic response of the FB VSI can be pushed even further with a real time control card like FPGAs equipped to control the semiconductor switches that can handle a higher switching frequency (like GaN devices). This could be the future research area

along with the digital interfacing protocol to connect the amplifier to the RTS directly.

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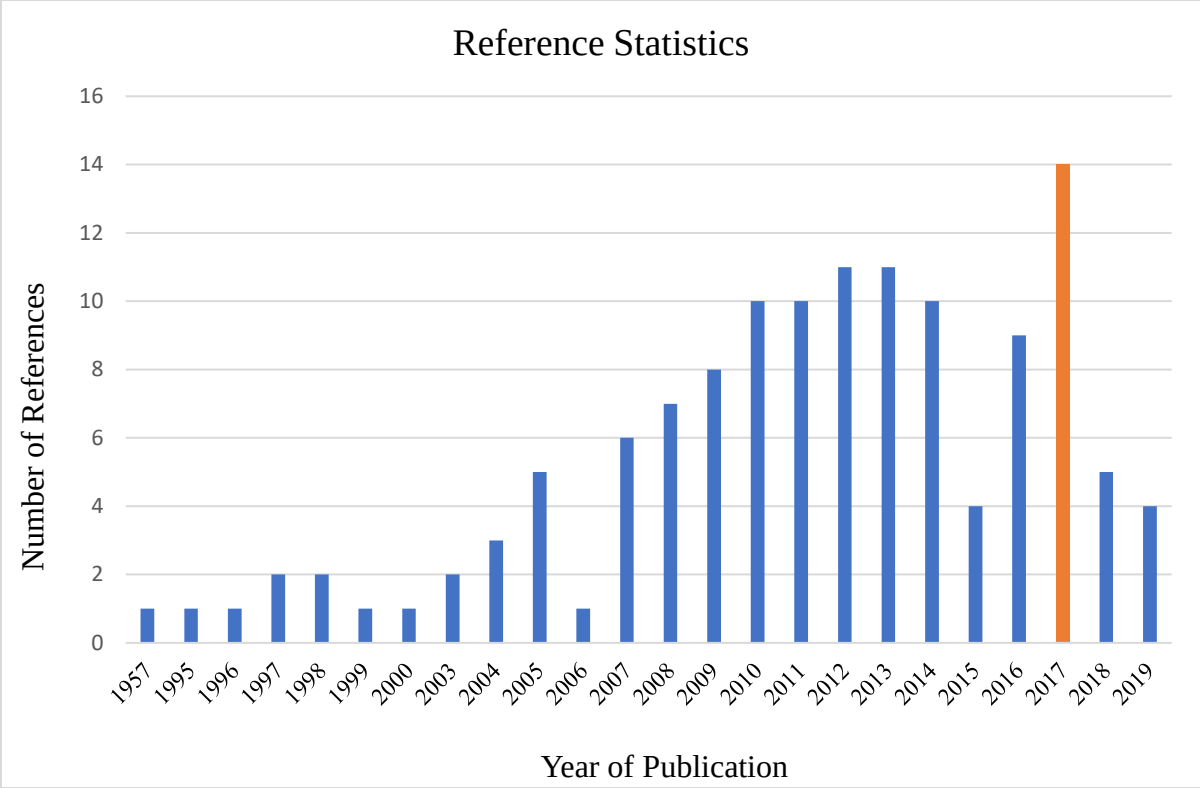

The chart above shows the plot of number of references against the year of publications cited in this thesis. The reported mode of the chart is seen at the year 2017.

Appendix A

In this appendix, the derivations of expressions shown in Chapter 2 is presented.

A.1. Derivation of (3.4) – (3.7)

By using Kirchhoff's Voltage law (KVL) for the circuit in Figure 3.4,

$$v_{pv}(t) = i_C(t) \cdot r_C + v_C(t) \tag{A.1}$$

$$v_{pv}(t) = i_L(t) \cdot r_L + v_L(t) \tag{A.2}$$

Similarly, by using Kirchhoff's Current law (KCL) in Node-1,

$$i_{pv} = i_c(t) + i_L(t) \tag{A.3}$$

Using (A.1), (A.3) & substituting $i_{pv}(t) = \frac{-v_{pv}(t)}{R_{mpp}}$; $i_C(t) = \frac{C \cdot dv_c(t)}{dt}$, (3.4) can be obtained.

Similarly, using (A.1), (A.2), (3.4) and substituting $v_L(t) = \frac{L \cdot di_L(t)}{dt}$, (3.5) can be obtained. Further, to obtain (3.6), (3.4) can be substituted into (A.1).

Using KVL for the circuit in Figure 3.4,

$$v_L(t) = v_{pv}(t) - r_L i_L(t) - v_{dc} \tag{A.4}$$

Finally, (3.7) can be derived by substituting (A.1) and (3.4) into (A.4).

A.2. Derivation of (3.12)

Using Taylor series expansion in (3.11):

$$e(v_{pv}, i_{pv}) = e(V_{mpp}, I_{mpp}) + \left.\frac{\partial e(v_{pv}, i_{pv})}{\partial v_{pv}}\right|_{(V_{mpp}, I_{mpp})} (v_{pv} - V_{mpp})$$

$$+ \left.\frac{\partial e(v_{pv}, i_{pv})}{\partial i_{pv}}\right|_{(V_{mpp}, I_{mpp})} (i_{pv} - I_{mpp})$$

$$e(v_{pv}, i_{pv}) = -\frac{I_{mpp}}{{V_{mpp}}^2}(v_{pv} - V_{mpp}) + \frac{1}{V_{mpp}}(i_{pv} - I_{mpp}) \quad \text{(A.5)}$$

Substituting i_{pv} from (3.1) into (A.5),

$$e = \frac{2}{R_{mpp}} - \frac{2v_{pv}}{R_{mpp}V_{mpp}} \quad \text{(A.6)}$$

Introducing small-signal perturbation, (A.6) is expressed as:

$$\tilde{e} = -\frac{2}{R_{mpp} \cdot V_{mpp}} \cdot \tilde{v}_{pv} \quad \text{(A.7)}$$

Thus, (3.12) can be obtained.

A.3. Derivation of (3.13)

A discrete integrator of trapezoidal form can be expressed as:

$$\frac{V_{pv\_ref}[z]}{E[z]} = K_i \cdot \frac{T_s}{2} \cdot \frac{z+1}{z-1} \quad \text{(A.8)}$$

$$V_{pv\_ref}[z] = V_{pv\_ref}[z] \cdot z^{-1} + \frac{K_i \cdot T_s}{2} \cdot E[z] + \frac{K_i \cdot T_s}{2} \cdot E[z] \cdot z^{-1}$$

Using time shifting property (A.9) on the above expression,

$$z\{x[k-n]\} = z^{-n} \cdot X[z] \text{ where, } z\{x[k]\} = X[z] \quad \text{(A.9)}$$

Equation (3.13) can be derived.

A.4. Derivation of (3.15)

Taking z transform of (3.14):

$$T_c(z) = \frac{v_i(z)}{r(z)} = K_p + K_i \cdot \frac{T_s}{2} \cdot \frac{z+1}{z-1} \tag{A.10}$$

$$v_i[z] = v_i[z] \cdot z^{-1} + K_p \cdot r[z] - K_p \cdot r[z] \cdot z^{-1} + K_i \cdot \frac{T_s}{2} \cdot r[z] + K_i \cdot \frac{T_s}{2} \cdot r[z] \cdot z^{-1} \tag{A.11}$$

Using time shifting property (A.9) on (A.11),

$$v_i[k] = v_i[k-1] + K_p \cdot r[k] - K_p \cdot r[k-1] + K_i \cdot \frac{T_s}{2} \cdot r[k] + K_i \cdot \frac{T_s}{2} \cdot r[k-1] \tag{A.12}$$

Further simplifying (A.12), (3.15) can be obtained.

A.5. Derivation of (3.16)

From Figure 3.6, the duty cycle equation can be expressed as:

$$D(t) = \frac{v_i(t)}{\hat{V}_r} \tag{A.13}$$

Introducing small-signal perturbation in (A.13),

$$D + \tilde{d}(t) = \frac{V_i + \tilde{v}_i(t)}{\hat{V}_r} \tag{A.14}$$

By cancelling the DC terms in (A.14), (3.16) is obtained.

Appendix B

In this appendix, the derivations of expressions shown in Chapter 6 is presented.

B.1. Derivation of 6.14

For Mode II and with reference to the steady state plots in Figure 6.4 (b).

During Turn-ON or when $Zero$ voltage appears across node v_{AB} during time instants t_6 to t_8;

$$\frac{di_L}{dt} \cong \frac{di_C}{dt} = -\frac{v_{ref}}{L} \tag{B.1}$$

In equation (B.1), it is assumed that during steady state the output voltage is equal to the reference voltage and the inductor ripple is equal to the capacitor ripple.

Further, (B.1) can be expressed as;

$$\frac{i_C(t_8) - i_C(t_6)}{t_8 - t_6} = -\frac{v_{ref}}{L}$$

$$\Longrightarrow t_8 - t_6 = \frac{\mathrm{L}}{v_{ref}} \left(i_C(t_6) - i_C(t_8)\right) \tag{B.2}$$

During Turn-OFF or when $-v_{in}$ appears across node v_{AB} at time instants t_8 to t_{10};

$$\frac{di_L}{dt} \cong \frac{di_C}{dt} = -\frac{(v_{in} + v_{ref})}{L}$$

$$\frac{i_C(t_{10}) - i_C(t_8)}{t_{10} - t_8} = -\frac{(v_{in} + v_{ref})}{L}$$

$$\Longrightarrow t_{10} - t_8 = -\frac{\mathrm{L}}{v_i + v_{ref}} \left(i_C(t_6) - i_C(t_8)\right) \tag{B.3}$$

In equation (B.3) from Figure 6.4 (b) the substitution of $i_C(t_6) = i_C(t_{10})$ is made.

Adding (B.2) and (B.3), one switching cycle time period can be obtained.

$$t_{10} - t_6 = \frac{\mathrm{L}v_i}{v_{ref}\,(v_i + v_{ref})} \left(i_C(t_6) - i_C(t_8)\right) \tag{B.4}$$

Now, the capacitor voltage equation can be expressed as;

$$v_C(t) = v_{min} + \frac{1}{C}\int_{t_7}^{t_8} i_C(t)dt$$

$$v_C(t) = v_{ref} - \Delta + \frac{1}{2C}(t_8 - t_7)\Delta i_C \tag{B.5}$$

Substituting, $\Delta i_C = -\frac{v_{ref}}{L}(t_8 - t_7)$ and $t_8 - t_7 = \frac{D}{2f_{sw}}$

$$v_C(t) = v_{ref} - \Delta - \frac{v_{ref}\,D}{8LCf_{sw}^2}D$$

$$v_C(t) = v_{ref} - \Delta + 2\Delta D \tag{B.6}$$

Equation (B.6) can be obtained by substituting the steady state capacitor voltage ripple from (6.11).

To calculate the current $i_C(t_6)$ and $i_C(t_8)$ in (B.3), the BC equation during Turn-ON and Turn-OFF can be used. Also, it is to be noted that (B.6) is valid along the duration t_6 to t_8.

Substituting (B.6) in (6.4) and (6.5);

$$\left.\begin{aligned} i_C(t_6) &= -\sqrt{\frac{2\Delta D}{k_2}} \\ i_C(t_8) &= \sqrt{\frac{2\Delta\,(1+D)}{k_3}} \end{aligned}\right\} \tag{B.7}$$

From (B.3) and (B.7), (6.14) can be obtained.