THE SIMULATION AND ITS VERIFICATION OF HIGH-SPEED PRINTED CIRCUIT BOARDS WITH CAD/CAE TOOLS

by

© Jaroslaw Zarychta

A thesis
presented to the University of Manitoba
in partial fulfillment of the
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MASTER of SCIENCE
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ABSTRACT

This thesis explores ways of achieving good performance in high–speed printed circuit boards (PCBs). Simulations of PCBs and high–speed switching conditions are performed. The results of simulations are verified by measurements.

Literature survey describes: PCB types and technologies; high–speed interconnections, phenomena and parameters; and PCB design and simulation. High–speed measurement and testing techniques are described, for frequencies of several hundred MHz up to the GHz range.

The measurements are performed for two frequency ranges by using a digitizing oscilloscope setup for up to 300 MHz, and a TDR setup for the GHz range. These setups are used to measure time delays, characteristic impedance, crosstalk, and reflections in traces on a specially designed, scaled PCB.

The field simulation is used to create equivalent circuits of PCBs, which are used for time–domain simulations of the measurement setups. Measured results for several configurations and terminations are compared with corresponding simulation results. This comparison is used for verification of simulations. The simulation tools discussed assist one to predict high–speed phenomena very accurately and help to design PCB interconnections.

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LIST OF PRINCIPAL SYMBOLS

Symbols used are:

A	Plate area;
C_m	Mutual line capacitance per unit length;
C_o	Intrinsic line capacitance per unit length;
C_p	Parallel–plate capacitance;
d	Diameter of the wire;
ϵ_r	Dielectric constant;
h	Height between conductor line and plane;
K_f	Forward crosstalk constant;
K_b	Backward crosstalk constant;
L_o	Intrinsic line inductance per unit length;
L_o	Mutual line inductance per unit length;
t_{pd}	Time delay;
t_D	Total one–way line delay equal ($t_{pd}l$);
V_b	Backward crosstalk signal amplitude;
$V_b(x,t)$	Backward crosstalk signal voltage;
V_f	Forward crosstalk signal amplitude;
$V_f(x,t)$	Forward crosstalk signal voltage;
V_s	Input signal voltage amplitude;
$V_s(x,t)$	Input signal voltage;
x	Arbitrary point along line;
w	Width of the conductor line;
Z_o	Characteristic impedance;
ρ_L	Load reflection coefficient;
ρ_S	Source reflection coefficient.

CHAPTER I

INTRODUCTION

The objective of this thesis is to explore ways of achieving good performance in high–speed printed circuit boards (PCBs). This thesis may assist one to understand how to control reflections, ringing and crosstalk. Essentially the PCB design is based on three stages: circuit design; design verification; and final physical design [Clyd86].

The verification stage is particularly important as it enables a design to be simulated and tested as a software model without the expense of building a "bread-board" model. It is possible to produce defect–free boards at the first prototype stage, thereby considerably reducing development times [Clyd86].

For simplicity, the term "Printed Circuit Board", "PCB", and "board" will be used synonymously throughout this thesis. The PCB is an essential part of a total electronic circuit packaging system. This system includes: components required to achieve product functionality; their packages; and the PCB interconnecting the package leads into a total circuit [Clyd86].

A component package provides the connections to the internal component contacts. The technologies of packaging and interconnection have been improved to provide the capability to the smaller, faster, and cheaper integrated circuits available. As more functions are integrated on a chip, more connections off the chip are required, and more circuit traces are needed to interconnect them. The PCB process has to provide electric connection to all of the nodes in a circuit [Clyd86].

Computer–aided design (CAD) is used to design circuits and PCBs. Computer–aided engineering (CAE) enables to simulate circuit and to verify a variety of design alternatives before manufacturing of prototype [WaCr86]. It is necessary to emphasize the importance of accurate device models because any analysis is only as accurate as the models used. The design process with CAD/CAE tools and various types of simulators are described in this thesis.

Modern circuits become faster and faster. High–speed circuits require high performance PCBs with controlled impedance design [DeFa70]. The interconnections are now very important elements in the high speed circuits and adequate CAD/CAE techniques are very useful to ensure the proper operation of these circuits [Royl88]. The result was a concurrent reduction in line (trace) width and increase in the number of conductor layers (multilayer boards) and, therefore, a big increase in capability for circuit density and complexity [GrHi87]. Multilayer PCBs have become very complex. This led to the use of computer programs for design and simulation of PCB.

Modern CAD/CAE systems have large libraries and databases of components and elements, which are very important for efficient designing. Some of CAD/CAE packages have the circuit design, simulation, routing, and layout capabilities [WaCr86]. And some are specialized only in one area (e.g., simulation). The final output can be plotted very accurately by laser plotter or it can be stored in the form of control tapes. The control tapes for a plotting machine and for a numerically–controlled drill can be sent to a manufacturer to manufacture the board. Also many different CAD systems use standard datasets [PaGr86].

This thesis explores ways of achieving good performance in high–speed printed circuit boards (PCBs). Simulations of PCBs and high–speed switching conditions were performed. The results of simulations were verified by measurements.

Literature survey describes: PCB types and technologies; high–speed interconnections, phenomena and parameters; and PCB design and simulation. High–speed measurement and testing techniques are described, for frequencies of several hundred MHz up to the GHz range.

A multilayer PCB was designed, using the PCB–design system called Optimate*. This board was designed for measuring high–speed parameters, crosstalk, reflections, and particularly vias and corners. The influence of vias and corners is very small and very difficult to measure. All necessary data was prepared on a magnetic tape to manufacture this board but it was not manufactured.

An existing example scaled board with microstrips was tested [PoRe86]. The measurements were performed for two frequency ranges by using a digitizing oscilloscope setup for up to 300 MHz, and a TDR setup for the GHz range. These setups were used to measure time delays, characteristic impedance, crosstalk, and reflections in traces on a specially designed, scaled PCB. This scaled PCB has practical cross–section dimensions but the traces are long to enable accurate measurements of transmission line effects and time delays with the equipment of limited bandwidth.

The field simulation was used to create equivalent circuits of PCBs, which were used for time–domain simulations of the measurement setups. The traces on PCB were treated as transmission lines, which parameters such as: time delays; characteristic impedances; and inductance and capacitance matrices were computed using Greenfield**. Also potential distribution, and electrical fields of microstrips and striplines were computed using Greenfield.

The same board was simulated and time–domain analysis was performed using Phyllis*** simulator. Phyllis is part of the Greenfield package and it is an analog simulator used for time domain analysis. Phyllis is particularly efficient for

* $Optimate^{TM}$ is a trademark of Optima Technology Inc., Billerica, MA, USA
** $Greenfield^{TM}$ is a trademark of Quantic Laboratories Inc., Winnipeg, Canada
*** $Phyllis^{TM}$ is a trademark of Quantic Laboratories Inc., Winnipeg, Canada

transmission–line problems [PoWe86]. Experimental results were compared with those obtained from simulation.

The input capacitance of a circuit increases the rise time at the end of the line, thus increasing the effective delay [Bloo82]. The input capacitance of distributed loads (circuits) modifies the line characteristics and should be taken into account when determining line delay. Thus, the whole system including circuits, transmission lines and loads should be simulated because each component of the system changes the characteristics of the system.

The system consisting of signal generator, transmission lines (microstrips) and loads was simulated using Greenfield. The generator was modelled as an equivalent voltage source and impedance. Connector and termination were modelled as resistor and capacitance in parallel. Connector was modelled as capacitance. Reflections, ringing and crosstalk in three parallel microstrip lines were simulated and compared with measured results.

The foregoing discussions are by no means an exhaustive treatment of high–speed PCB problems. Rather, they are intended to focus attention on the general methods used to determine the interactions between high–speed logic circuits and their interconnections. They show how to control reflections, ringing and crosstalk. The simulation tools discussed assist one to predict high–speed phenomena very accurately and help to design PCB interconnections.

CHAPTER II

PRINTED CIRCUIT BOARD TYPES AND TECHNOLOGIES

The basic board technologies and types of printed circuit boards are briefly described in this chapter. The basic function of a printed circuit board is to provide support for circuit components and to interconnect the components electrically. Many printed wiring methods have been developed to achieve these results [Clyd86]. They vary in base dielectric material, conductor type, number of conductor planes, rigidity, etc.

The standard printed circuit board is for simplicity called PCB. The image of the PCB master circuit patterns is formed photographically on a photosensitive material such as glass plate or film. The image is then transferred to the circuit board by screening or photoprinting the artwork generated from the master. The majority of boards are produced in this way.

There are three principal soldering methods, namely wave soldering, vapour phase and infra–red re–flow soldering [Clyd86]. Wave soldering requires that surface mounted components are pre–glued to the underside of the board before it passes across the solder weir. For re–flow soldering, mounds of solder cream are pre–deposited on PCB pad areas prior to component placements and subsequent heating to make the joints. "Pick and place" machines are used for accurate placement. Proper shape and position of each PCB pad area may ensure self–alignment of surface mount components during re–flow soldering [Clyd86].

2.1 Discrete–wire boards

The **discrete–wire board** has wires directly formed onto the wiring board with insulated copper wires. According to Clyde, [Clyd86], the time required for design and production is short in this technology but the process is sequential, and so the productivity is limited. In this section that technology is summarized [PlBS81].

The discrete–wire process was originally developed as a high–density competitor to the multilayer PCB in medium–speed applications, and extensive testing has verified the performance of this discrete–wiring approach in controlled impedance situations (50 to 100 Ω) where rise times approach 1 ns [PlBS81].

The discrete–wire technology relies on No.34 AWG wire [PlBS81]: the wire nominal diameter = 0.005 in (0.152 mm); and the ratio of height to diameter equal about 1.5. Choosing the distance of wire centre to ground equal to h=0.0075 in yields $Z_o = 50\ \Omega$. And h=0.023 in gives $Z_o = 92.8\ \Omega$. By raising the height of the wire above the ground, higher impedances can be obtained.

The initial step in the discrete–wire process is imaging and etching a copper–clad printed circuit board laminate in accordance with a format drawing provided by the customer. The format determines the ground planes for power distribution, as well as for controlled impedance. Copper foil is used for power and ground planes.

Next, the B–stage (partially cured) epoxy–coated fabric is used as an adhesive material applied to the board. Finger regions, card–guide edges, and other areas are left free of adhesion. The discrete wires are fixed to the substrate layer by using adhesive layer. Using computer–driven, numerically–controlled wiring machines, wires are then laid down with the aid of specially designed wiring head on the bed of adhesive in accordance with the wiring instructions and component locations supplied by the customer. While each wire begins and ends at a hole, a wire may intersect any number of holes and wires may cross each other.

The epoxy fibreglass cover sheet is used on the top of the wires for mechanical protection and electrical insulation from the outside environment. After the wires

are processed into the adhesive, usually through ultrasonic means, they are covered by a sheet of epoxy–coated glass cloth (called prepreg) and cured by applying pressure and temperature. This step locks the wires securely in place.

The hole drilling exposes wire ends prior to plating. Plated–through holes create electrical connections between individual wires and are used for mounting of components. Holes are drilled by computer–controlled drilling machines at each plated–through location. Tooling holes for automated insertion and holes for card ejectors or various other purposes are also drilled. After all holes are drilled, the polyimide insulation of the wires is chemically etched back from the wire ends. Then, using an electrodeless additive plating process, copper is deposited in the holes.

Additional steps to complete the fabrication process include applying a cover layer, gold plating of the contact fingers, routing the board perimeter to its final profile, and screening legends in place. Finally, each discrete–wire board is electrically tested to make sure that there is continuity between every hole interconnected by wire. High–potential and insulation–resistance tests are also performed, according to Plonski et al., [PlBS81].

2.2 Single and double–sided boards

The **single–sided board** (SSB) has circuits on one side of the board. It is often referred to as the "print–and–etch" board because the resist protecting the copper during the circuit–forming etching process is usually "printed" by a screen–printing technique. Most etch–resist, solder mask, and legend inks used for the manufacture of SSBs are curable by ultraviolet light which is a quick process and easy to accomplish by using any strong ultraviolet light source. After exposure to ultraviolet light, these inks become hard.

These inks make the print–and–etch line shorter, easier to maintain, and more economical. Its major applications are in packaging consumer electronic products

[Clyd86]. When the production volume is high, SSBs are manufactured by completely automated production lines.

The **double–sided board** (DSB) has circuits formed on both sides of the board. The through holes (TH) are basically used to connect circuitry on both sides. The TH is created by metallizing the walls of a hole (in the substrate) that intersects the circuitry on both sides. The DSBs are very popular because they are easy to design, manufacture, and repair, and they are efficient for designs of medium complexity [Clyd86].

2.3 Multilayer boards

The **multilayer board** (MLB) has three or more circuit layers. Typically there are fewer then 16 layers but there may be many more layers (e.g. 60) [Clyd86]. Typical multilayer board has four layers, or six layers, or eight layers. Four–layer boards are by far the most popular MLBs. Special boards may have between 8 and 16 layers. Boards with more than 16 layers are rather unusual. In this section that technology is summarized [Clyd86].

The most widely practiced method of making MLB is by bonding, or laminating, layers of patterned, pre–etched, undrilled copper–clad laminate together. Interconnections between different layers are made with through holes (THs). After lamination, the subsequent manufacturing processes for MLBs are more or less the same as those used for DSBs made with the TH process.

To increase the interconnection density, *buried via* holes or *blind via* holes may be used in high–level MLBs, but they are used very rarely because they require drilling of additional holes through very thin laminates. To make these kind of vias, inner layer pairs are fabricated exactly like double–sided boards with THs and are then assembled into an MLB, using standard techniques.

The holes going through all layers are called *feed–throughs* or *through–holes*. The cost and reliability of MLB process have improved and its applications are very wide but it is still much more expensive than the DSB process.

Mulilayer board normally consist of two or more layers of separate circuit patterns that have been laminated together under heat and preassure to produce a strong unit. Figure 2.1 illustrates the lay–up details of two multilayer boards, one composed of single–sided boards and the other of double–sided boards.

The typical multilayer printed circuit board is made of [Clyd86], [Kear87]: successive layers of copper; C–stage (fully cured) epoxy–glass dielectric (the same as is used in two–sided boards but much thinner); and B–stage (prepreg) epoxy–glass that has been dried and partially cured, as bonding material (the "glue") to build and hold the board together. The stack of layers is heated under preasure until the prepreg is cured.

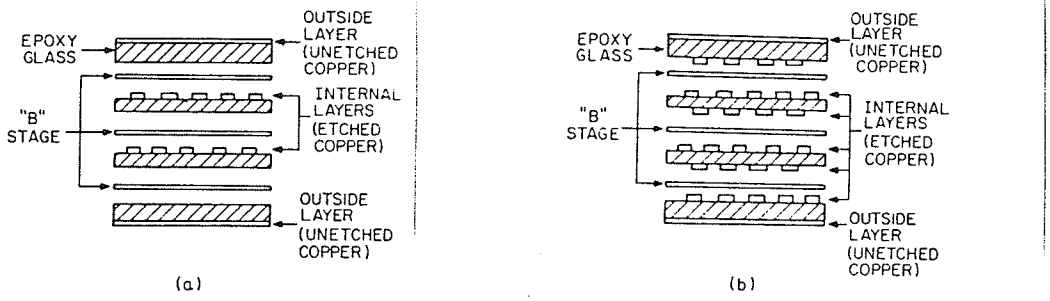


Figure 2.1: The lay–up of multilayer board. (a) Four–layer board; (b) Eight–layer board. From: [Clyd86]

The inner layers are formed by printing and etching circuits and planes on copper–clad dielectric materials (drilled and plated through in the case of buried vias). Dielectric thickness for these inner layers will depend upon the number of layers and overall board thickness specifications.

2.4 Surface mount technology versus through–hole technology

Through–hole technology and surface mount technology are the two basic methods for placing components on the board. There are also mixed surface mount and through–hole assemblies. Typical assembly types may have: surface mount devices on one side; surface mount devices on both sides; through–hole components on one side and surface mount components on the other side; and through–hole and surface mount components on one side, and surfice mount components on the other side. In the conventional through–hole technology the components are mounted to the PCB with leads inserted through the board. This technology is no longer adequate to meet the needs of high–performance electronic assemblies [Clyd86].

Surface mount technology (SMT) is becoming very popular because it offers many benefits over conventional through–hole technology. SMT components are soldered directly to the copper conductors on the surface. For re–flow soldering, mounds of solder cream are pre–deposited on PCB pad areas prior to component placements and subsequent heating to make the joints. "Pick and place" machines are used for accurate placement. Proper shape and position of each PCB pad area may ensure self–alignment of surface mount components during re–flow soldering [Clyd86]. To withstand the rigors of the insertion process, through–hole component leads must be relatively large. Surface components do not require these large leads and can therefore be much smaller than their through–hole equivalents [Clyd86].

Printed circuit technology historically, has been driven by factors relating to the cost, size, and performance of the end product. SMT provides benefits over THT in each area.

Compared to an equivalent through–hole PCB, a typical SMT board can be made 30 to 50 percent smaller [Clyd86]. Main cause of the savings in SMT is the smaller physical size of surface mount components. A smaller number of holes and smaller drilled–hole diameters are used on the PCB. The area required on the PCB for such vias can be reduced by a factor of 3 or more over vias for through–hole

components. Smaller components also permit reduced overall thickness. Boards can be packaged more closely because they have smaller physical size, and components can be placed on both sides to effectively double the available area.

It is possible to design one SMT board which is equivalent to a few through–hole boards because the components are much smaller and there is less holes and holes occupy a substantial part of a PCB. In this way fewer connectors can be used because there is less boards in the system. In other words, fewer system–level interconnects are necessary. This reduces both material costs and assembly labor and gives perhaps the most significant savings.

The shorter leads of SMT components reduce their parasitic inductances and capacitances. For this reason, they are preferred for high–frequency analog applications. Through–hole circuitry is rarely used above 500 MHz, but SMT circuits can be employed successfully in applications benefits from SMT packaging. Propagation delays are not only shorter but more uniform from lead to lead because the parasitic reactances are more uniformly distributed along the leads [Clyd86]. This is especially important for digital circuits with clock rates above 10 MHz.

Because of the small physical size and close spacing of SMT components, assembling production boards manually is impractical. As a result, automation is required and SMT benefits from its higher inherent quality. Surface mouting is a physically simpler process than inserting and crimping component leads. However, because SMT processes are less mature than through–hole processes, additional engineering effort may be necessary to achieve the high quality possible with this technology [Clyd86].

2.5 Impact of new electronic devices on PCB design

The recent progress of the entire electronics industry has been driven by developments in IC technology. Advances in very large scale integration (VLSI) manufacturing have improved yields. The reduction in feature size has made it possible to concentrate within a single chip thousands of transistors. The fast development of VLSI technology is driving active devices toward: higher speeds; more I/O terminals; and increased power.

With the growing popularity of gallium arsenide (GaAs), the board has become just as much an active circuit component as the devices it interconnects. Fast digital devices can operate with signal rise times in the nanosecond range (for Si technology) or even in the picosecond range (for GaAs technology). At these operating speeds conductors interconnecting such devices become active elements of the circuit and their design must be carefully analyzed and executed [DeFa70].

The new generation of electronic systems requires ever–increasing complexity and density of interconnections, and the definite trend toward higher operating frequencies demands extremely careful design of a single conductor. The width, length, location, and relations of conductors, the spacing, and the dielectric material are interrelated and they often exert critical influence on signal propagation, noise ratio, shape of the pulses, and other electrical characteristics of the system.

Therefore, the interest of system design engineers as well as of electrical design engineers in electronic packaging has become much more intensive. When designing system interconnections, the following parameters of transmission lines and signals must be taken into consideration: propagation delay per unit length of line; characteristic impedance Z_o; line attenuation; rising and falling times of the signal; crosstalk; reflections due to mismatched impedance characteristics of the driver, line, connectors, and line terminations; ringing; and signal distortions.

Features which must be specified on the drawing or specification, and which effect these electrical requirements, are as follows [Bloo82],[PoRe86],[Clyd86],[Kear87]:

the dielectric constant of of the laminate and prepreg; conductor line width; spacing between conductors on one layer; dielectric thickness between layers; thickness of the copper conductors; the layering sequence of conductors in the multilayer board; and the sequence in which the signal nets are connected.

Most interconnections on a high–speed PCB behave as transmission lines. The next sections are about PCB transmission lines.

2.6 Transmission lines

The characteristic impedance of a transmission line depends upon the relationship of the conductor width, conductor thickness, dielectric thickness between conductor and ground or power plane, and the dielectric constant of the propagating medium. Formulas used to design controlled impedance are given below. These formulas are quite accurate and they can be used to find an approximation of actual values.

Very accurate results can be obtained using Greenfield CAD/CAE system which produces characteristic impedance, capacitance and inductance matrices for any arbitrary two–dimensional cross–section [PoWe86]. For digital circuits, each connection with a time delay bigger then a half of the signal rise (or fall) time must be considered as transmission line. The following types of transmission lines can be used for interconnecting high–speed logic systems.

2.6.1 Wire over ground

Figure 2.2 shows the cross section of a wire over ground plane. The characteristic impedance of the wire over ground is [Bloo82]:

$$Z_o = \frac{60}{\sqrt{\epsilon_r}} ln(\frac{4h}{d}) \tag{2.1}$$

where: ϵ_r = is the effective dielectric constant surrounding the wire;

h = height of the wire centre above the ground; and

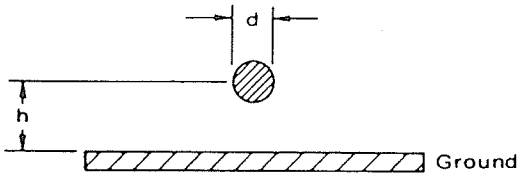


Figure 2.2: Wire over ground. From: [Bloo82].

d = the diameter of the wire.

The characteristic impedance of a wire over a ground plane can vary significantly depending on the distance from the plane, proximity of adjacent wires, and the configuration of the ground. The standard discrete–wire board is composed of a ground plane, an adhesive sheet with the wires embedded in it and a cover layer of epoxy–impregnated glass cloth called a prepreg.

2.6.2 Microstrip line and stripline

Microstrip transmission lines are often used to provide controlled impedance interconnections for high–speed digital circuits. A microstrip line (Fig. 2.3) is a strip conductor (signal line) exposed to air and separated from a ground plane by a dielectric. The characteristic impedance, Z_o Ω, of a microstrip is [Bloo82]:

$$Z_o = \frac{87}{\sqrt{(\epsilon_r + 1.41)}} ln(\frac{5.98h}{0.8w + t}) \tag{2.2}$$

where: ϵ_r = relative dielectric constant of the board material;

h = distance between signal line and reference plane;

w = width of the line; and

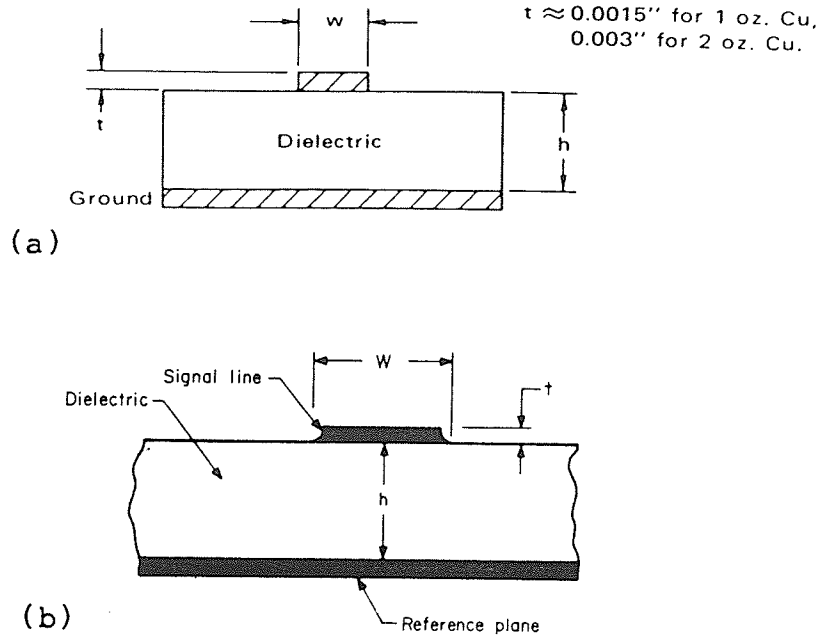


Figure 2.3: Microstrip transmission line. (a) The ideal microstrip, (from: [Bloo82]); (b) The microstrip with undercut, (from: [Clyd86]).

t = thickness of the line.

The signal line is made by etching away the unwanted copper using photo resist techniques. With microstrip, as in Fig. 2.3.b, the width of the line should be measured at its surface closest to the reference plane, because most of the electrical charge is collected on this surface. This line is made by an etching process, and the line width can vary significantly depending upon where it is measured. This will be dependent upon the copper thickness, the etchant used, and the manufacturing process. **Therefore, numerical methods are necessary for calculating the exact value of the characteristic impedance.** The same comment refers to all formulas in this chapter.

This formula is quite useful but only for estimating the value of characteristic impedance. It yields quite accurate results for a typical bare microstrip. For

example:

```
***
For:  w=31 mil      h=31 mil      t=1.4 mil      ( so    w/h=1)
   Characteristic impedance calculated from formula    = 68.8670
   Characteristic impedance calculated by Greeenfield = 68.8745
   The error = (68.8745-68.8670)/68.8745=0.00011=0.011%
Conclusion: in this example the formula is very accurate.
***
For t=0 mil, this formula may be used only in the region:
             0 < w/h < 7.475
In general, this formula may be used only in the region:
             0 < w/h < 7.475-t/(0.8h)
For example, for a typical four layer board with h=20 mil
and t=1.4 mil, we get:
             0 < w/h < 7.475-t/(0.8h)=7.475-0.0875=7.3875
   which is equivalent to:  0 < w < 147.75 mil
For a typical six layer board with h=10 mil and t=1.4 mil,
   we get:   0 < w/h < 7.475-t/(0.8h)=7.475-0.175=7.3
   which is equivalent to:  0 < w < 73 mil
Typical trace widths are: 6 mil; 8 mil; or 12 mil.
The following trace widths are also used: 10 mil; 20 mil; 30 mil.
***
```

In practice, the microstrip is almost always covered with a protective dielectric and it has irregular shape with undercuts. In this case the formula may be still used for a rough estimation but numerical methods are necessary for calculating the exact value of the characteristic impedance.

Boundary element method is an example of a very efficient numerical method suitable for this application. Greenfield is a program which uses boundary element method and calculates exact values not only for characteristic impedances but also time delays, and capacitance and inductance matrices of any complicated system of dielectrics, and conductors with any shape. An example of Greenfield output for three microstrips is included in Chapter VII. These microstrips have w=31 mil h=31 mil and spacing=31 mil.

The characteristic impedance of microstrip lines for various geometries is plotted in Fig. 2.4.a. Figure 2.4.b shows curves for the microstrip capacitance per foot as a function of line width and spacing. These values were calculated from mathematical relation above and closely agree with experimental time domain reflectometer measurements from which it was derived.

The inductance per foot may be calculated using the formula [Bloo82]:

$$L_o = Z_o^2 C_o \tag{2.3}$$

where: Z_o =characteristic impedance in Ω, and C_o =capacitance/ft in F/ft.

The propagation delay may be calculated from the formula [Bloo82]:

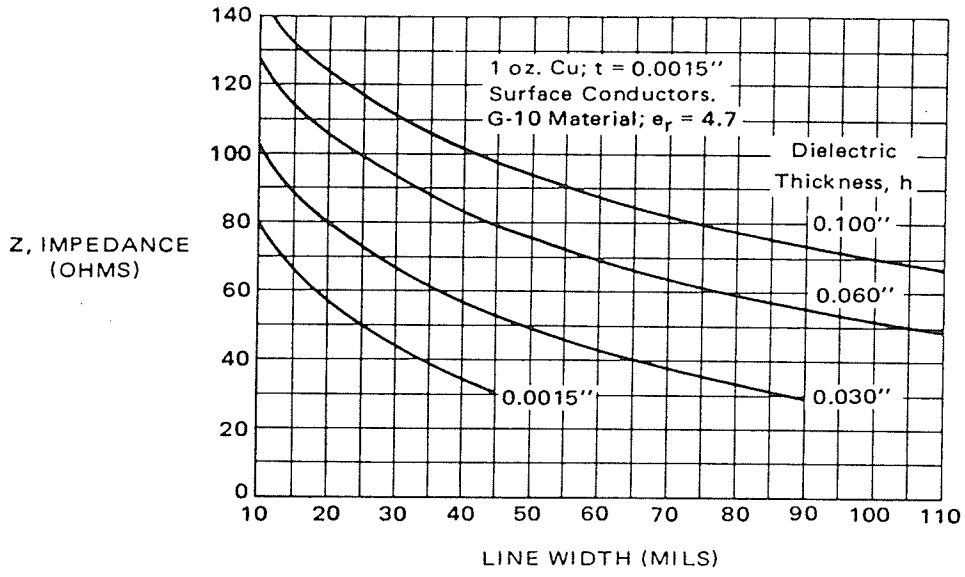
$$t_{pd} = 1.017\sqrt{0.475\epsilon_r + 0.67} \qquad ns/ft \tag{2.4}$$

Note that the propagation delay of the microstrip line is dependent only on the dielectric constant and is not a function of line width, thickness, or spacing. For G–10 fibreglass epoxy boards with $\epsilon_r = 5.0$ the propagation delay of microstrip line is 1.77 ns/ft [Bloo82].

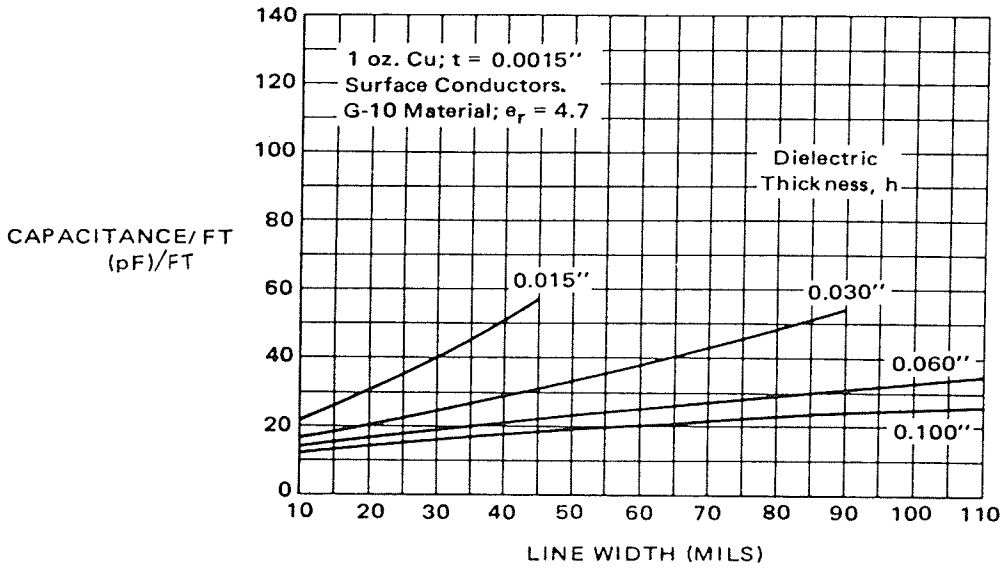
2.6.3 Embedded microstrip

Embedded microstrip is similar to microstrip, but the signal line is covered by a dielectric material — such as solder mask, thin laminate, or conformal coating (Fig. 2.5).

If the line is embedded with a material having the same dielectric constant of the multilayer base material and is at least 0.008 in thick, the surrounding air will have little effect on the effective dielectric constant. Most of the electric field will be confined in the dielectric which will cause the characteristic impedance to be lowered about 20%, and the propagation delay to be increased by approximately



(a)



(b)

Figure 2.4: Characteristic impedance and capacitance of microstrip. (a) Characteristic impedance versus Line width and dielectric thickness; (b) Capacitance per foot. From: [Bloo82]

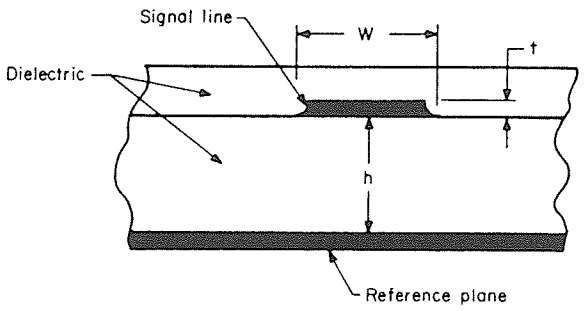


Figure 2.5: Embedded microstrip transmission line, (from: [Clyd86]).

20%. The propagation delay for a fully embedded microstrip can be calculated approximately from the formula [Bloo82]:

$$t_{pd} = 1017\sqrt{\epsilon_r} \quad ns/ft \tag{2.5}$$

Again, the delay is only dependent upon the dielectric constant and not the line geometry.

2.6.4 Stripline

Stripline is a transmission line embedded in a dielectric material and sandwiched between two reference planes, i.e., ground or power. This construction is used widely when the signal lines of the multilayer are not on the surface layers. Figure 2.6.a is an example of a balanced stripline where the line is equally spaced between the two reference planes

This configuration significantly reduces the cross–talk when compared with microstrip lines because most of the electromagnetic field is confined in the small space between the trace and reference planes on both sides of the trace. The equation for calculating the impedance of a single balanced (symmetrical) stripline is

[Bloo82],[F10086],[Clyd86]:

$$Z_o = \frac{60}{\sqrt{\epsilon_r}} ln(\frac{4h}{0.67\pi(0.8w + t)}) \qquad \Omega \tag{2.6}$$

where:

ϵ_r = dielectric constant;

h = distance between reference planes;

w = width of the line; and

t = thickness of the line.

This is a good approximation of what can be expected in an actual board. Test board should be made to prove out the design before it is committed to volume production. Very accurate results may be obtained by using numerical methods. The propagation delay can be calculated from the formula:

$$t_{pd} = 1.017\sqrt{\epsilon_r} \quad ns/ft \tag{2.7}$$

The coefficient 1.017 is the reciprocal of the velocity of light in free space. Note that this is the same equation used for calculating delay for the embedded microstrip, since the signal line is completely surrounded by dielectric material without the influence of air. For G–10 fiber–glass epoxy boards ($\epsilon_r = 5.0$), the propagation delay of the strip lines is 2.26 in/ft [Bloo82].

Figure 2.6.b shows a variation of the stripline — the dual stripline. (Usually, one signal layer is run perpendicular to the other to accommodate routing of the signal lines and reduce cross–talk significantly.) According to Clyde, [Clyd86], close approximation of characteristic impedance of the dual stripline can be made using the following formula :

$$Z_o = \frac{2Z_1Z_2}{Z_1 + Z_2} \tag{2.8}$$

where (see Fig. 2.6.b):

$$Z_1 = \frac{60}{\sqrt{\epsilon_r}} ln(\frac{8A}{0.67\pi(0.8w + t)}) \tag{2.9}$$

$$Z_2 = \frac{60}{\sqrt{\epsilon_r}} ln(\frac{8(A + D)}{0.67\pi(0.8w + t)}) \tag{2.10}$$

$$h = 2A + D \tag{2.11}$$

Note that this equation, with slight modification, can be used for a single stripline not equally centered between two reference planes.

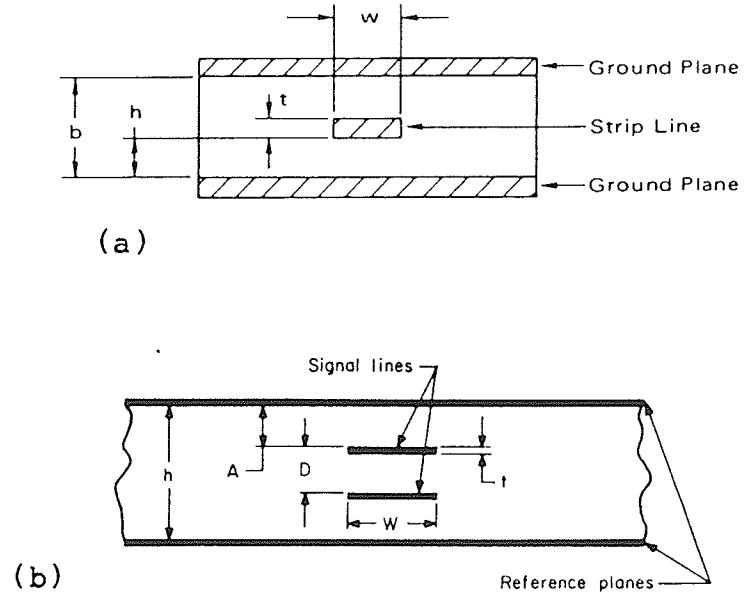


Figure 2.6: Stripline transmission line. (a) Single balanced stripline, (from: [Bloo82]); (b) Dual stripline, (from: [Clyd86]).

The parallel–plate capacitance between two planes can be calculated from this formula:

$$C_p = \frac{0.2249 A \epsilon_r}{h} \tag{2.12}$$

where:

C_p = capacitance, pF;

ϵ_r = dieletric constant;

A = common area betweeen the plates, in^2; and

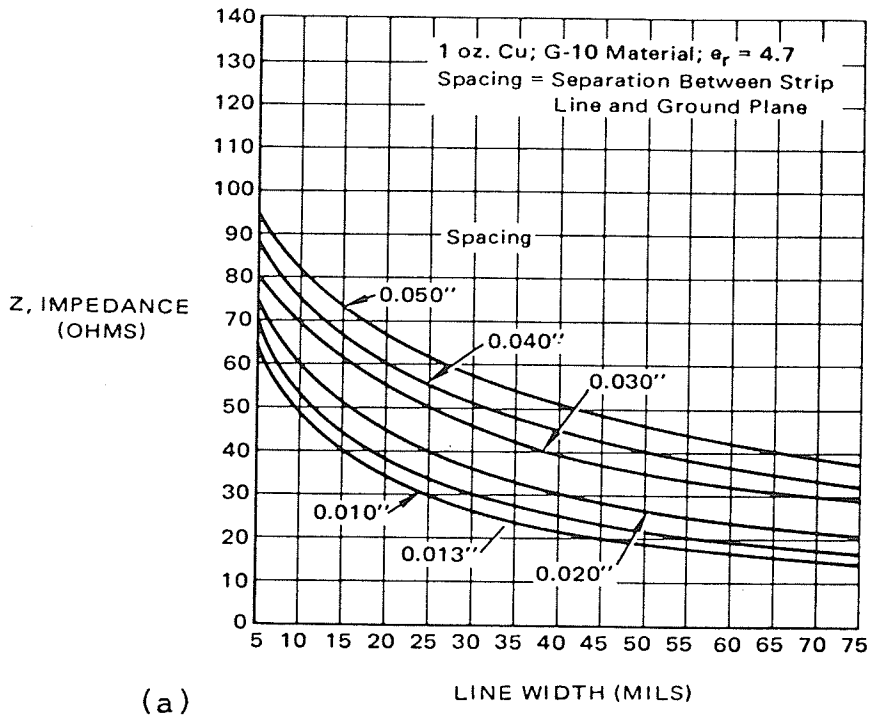
h = distance between the plates, in.

This capacitance minimizes voltage transients between voltage and ground planes in multilayer boards so fewer decoupling capacitors are necessary.

2.6.5 Dielectric constant

Dielectric constant plays a major role in the determination of impedance, propagation delay, and capacitance. As the dielectric constant gets smaller, the delay time gets smaller. In critical high–speed systems in which system performance and speed are of prime concern, lower dielectric constant materials such as teflon–glass ($\epsilon_r = 2.5$) can be used to increase the propagation speed. However, the load capacitances of the line can significantly decrease the propagation speed and performance. The cost of these materials is 2 to 10 times that of epoxy–glass multilayer manufacturing. For these reasons, most multilayer boards are made with epoxy–glass materials.

The epoxy resin has a dielectric constant of approximately 3.45 and glass aproximately 6.2. Depending upon the percentage of each of these materials, the dielectric constant of the laminate will range linearly from 5.3 to 4.2. If the electrical characteristics of the multilayer board are critical, the dielectric constant of the laminate and prepreg can be controlled by the proper selection of resin content of the materials.



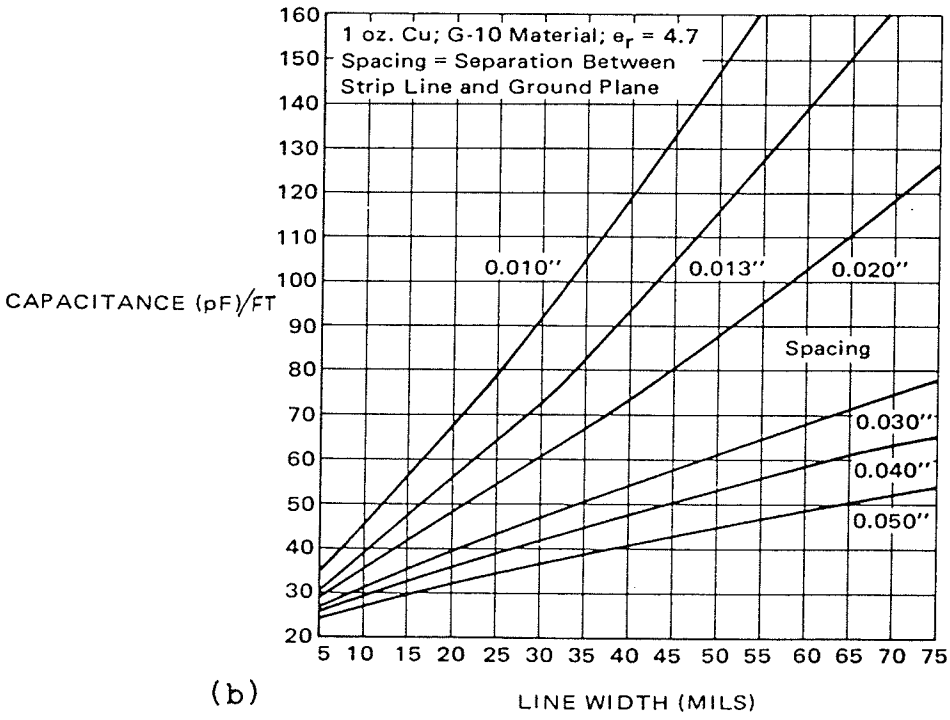


Figure 2.7: Characteristic impedance and capacitance of stripline. (a) characteristic impedance versus line width and dielectric thickness; (b) capacitance per foot versus line width and dielectric thickness. From: [Bloo82].

In this chapter, the most important printed circuit board types and technologies were described. Considering a PCB interconnection in terms of distributed rather than lumped inductance and capacitance leads to the transmission line and line impedance concept. Interconnections play very important role in PCB functionality. Transmission lines used in PCB as interconnections were described and useful formulas were given.

CHAPTER III

REFLECTIONS, CROSSTALK AND TERMINATIONS

This chapter is about PCB interconnection noise. The behaviour of signals on a transmission line is discussed. The high–speeds of today's integrated circuitry have given the interconnections of digital logic circuits characteristics usually associated with transmission lines. The most common method for eliminating reflections that occur in such lines involves a procedure called termination. However, terminating these transmission lines is not always practical because terminations take up space and increase system costs. The most common terminations are resistors which increase power supply requirements.

A possible solution to the problem of reflections is to decrease the length of interconnections by increasing the system density but impedance matching is still needed. However, the trend toward greater density creates another problem — that of crosstalk between the various conductors of the system. This coupling, which often exists between two adjacent transmission lines, may be strong enough for signals to appear on both lines when they are only desired on one. This is what crosstalk is.

The problem of crosstalk is present even if lines are terminated. Since these lines carry digital information, this unwanted coupling introduces false information to the system. The general category of extraneous voltages and currents due to reflections and crosstalk is commonly called interconnection noise [DeFa70].

Signal fidelity and crosstalk noise must be controlled to assure that a high performance system operates as predicted. The signal can become distorted by package electrical design characteristics such as too–high or too–low characteristic impedance, or poor connector design.

In designing a high–speed digital system, both the circuit and the interconnections must be considered or system performance may be impaired.

3.1 Crosstalk

Crosstalk is caused by coupling, which often exists between two adjacent transmission lines, that results in signals to appear on both lines when they are only desired on one. In this section, a simplified analysis of crosstalk is quoted after [Bloo82]. It gives an idea how crosstalk may be approximated. This analysis applies only to two parallel transmission lines. Practical PCBs have many parallel lines which behave as a very complex system. The whole system has to be considered. Numerical methods are necessary for calculating the exact value of crosstalk. Greenfield is capable to do accurate calculations.

Crosstalk amplitude $V(x,t)$ in an arbitrary point along line may be calculated with the following equation [Bloo82]:

$$V(x,t) = V_f(x,t) + V_b(x,t) \tag{3.1}$$

where the forward crosstalk $V_f(x,t)$ in the line is given by:

$$V_f(x,t) = K_f x \frac{d}{dt}(V_s(t - t_D\frac{x}{l})) \tag{3.2}$$

and the backward crosstalk $V_b(x,t)$ is given by:

$$V_b(x,t) = K_b(V_s(t - t_D\frac{x}{l}) - V_s(t - 2t_D + t_D\frac{x}{l})) \tag{3.3}$$

where the mathematical constants K_f and K_b are [Bloo82]:

$$K_f = -\frac{1}{2}(\frac{L_m}{Z_o} - C_m Z_o) \tag{3.4}$$

$$K_b = -\frac{l}{4t_D}(\frac{L_m}{Z_o} + C_m Z_o) \tag{3.5}$$

The symbols used are (Fig. 3.1):

$V_s(x,t)$	Input signal voltage;
x	Arbitrary point along line;
l	Line length;
t	Arbitraty time;
t_D	Total one–way line delay equal $(t_{pd}l)$;
K_f	Forward crosstalk constant;
K_b	Backward crosstalk constant;
Z_o	Characteristic impedance;
C_o	Intrinsic line capacitance per unit length;
L_o	Intrinsic line inductance per unit length;
C_m	Mutual line capacitance per unit length;
L_m	Mutual line inductance per unit length;
	(they describe coupling between traces).

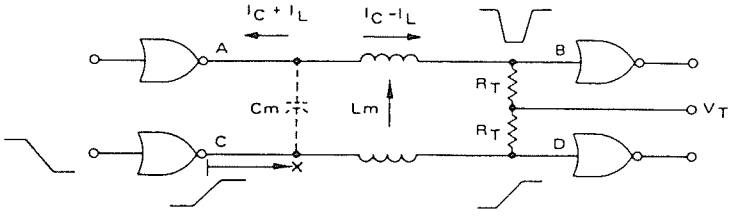


Figure 3.1: Crosstalk coupling in parallel lines. From: [Bloo82].

Also note that:

$$Z_o = \sqrt{\frac{L_o}{C_o}} \tag{3.6}$$

$$t_{pd} = \sqrt{L_o C_o} \tag{3.7}$$

The crosstalk wave travelling toward the load (in the same direction as the signal wave) is called the "forward crosstalk" and that part travelling toward source (in the opposite direction to the signal) is called the "backward crosstalk". Coupling occurs only during the rise and fall times of the signal pulses as it propagates along the line. There is also coupling back to the main line but this can be neglected because of very small value.

Very often it is of interest to the designer to estimate the crosstalk at the ends of the line. For this purpose there are simplified formulas which are derived for the ramp voltage source signal with amplitude V_S and with the rise time t_r and fall time t_f. This gives a forward crosstalk at the load end as a pulse equal in duration to the rise time and starting at time t_D — the amplitude is [Bloo82]:

$$V_f(l, t_D) = \frac{K_f V_S l}{t_r} \tag{3.8}$$

This gives a backward crosstalk at the source end as a pulse starting simultaneously with the driving signal. The leading edge of the backward crosstalk pulse is a ramp until time t_r then the pulse levels off until time $2t_D$ and then slopes to the starting point at time $(2t_D + t_r)$. The amplitude of this pulse is [Bloo82]:

$$V_b(0, t_r) = K_b V_S \tag{3.9}$$

The one factor not included in the calculations is attenuation in the line which damps out the higher frequency components of the signal, slowing the rise time of

the signal as it propagates along the line. The same applies to the fall transition with rise time replaced by fall time.

3.2 Reflections on transmission lines

Signal reflections on transmission lines are a major source of noise in digital systems. They occur whenever a transmission–line signal encounters a discontinuity; i.e., an impedance different from that of the original line. The discontinuity can be another transmission line, a circuit, or a load device.

Let us consider the behaviour of signals on a transmission line. For the purposes of discussion, the line delay t_D will be assumed to be long with respect to the rise time so that reflections will appear at their full amplitude. The line with a characteristic impedance Z_o is driven by a voltage source V_s with a source impedance Z_S in serial, and it is terminated with impedance Z_S. The input voltage swing on the transmission line is a function of the internal source voltage swing, source impedance and line impedance. It may be calculated from the formula [Bloo82]:

$$\triangle V = (\frac{Z_o}{Z_S + Z_o}) \cdot \triangle V_s \tag{3.10}$$

If the Z_S is small compared to line impedance, the input swing is nearly the same as the transition. This signal propagates down the line and is seen at the load line time delay t_D later. The voltage reflection coefficient at the load end of the line ρ_L is a function of the line characteristic impedance and the load impedance Z_L. It may be calculated from the formula [Bloo82]:

$$\rho_L = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{3.11}$$

where

$$\rho_L = \frac{Reflected\ Voltage}{Incident\ Voltage} \tag{3.12}$$

The level of reflection depends on the mismatch between the load and line impedances. Clearly, for the ideal case of $Z_L = Z_o$ there is no reflection. More important, for any value of Z_L close to Z_o the reflection is quite small.

The reflected wave travels back the line until it arrives at the source and encounters the source impedance (at time $2t_D$) and is reflected according to the source mismatch — the sending end reflection coefficient ρ_S:

$$\rho_S = \frac{Z_S - Z_o}{Z_S + Z_o} \tag{3.13}$$

The reflection continues bouncing back and forth between the ends of the line, producing **ringing**, and being successively reduced by the resistance in the line. Serious distortions occur when the reflected signal coincides with a following signal, i.e. when the transmitted frequency equals $f = \frac{1}{2t_D}$.

Calculations of the reflections may be done either graphically or numerically. A typical trace characteristic impedance is designed to be 50 Ω for ECL circuits and 100 Ω for TTL or high–speed CMOS circuit boards. Since the input and output impedances of semiconductor devices are nonlinear, they can not match the trace impedance and, therefore, the resulting line reflections can be minimized only by using proper termination. For instance the input impedance of ECL circuit is about 50 kΩ so we can use parallel termination of 50 Ω, and the equivalent load will be close to 50 Ω, and practically linear.

3.3 Connectors

There are very few high frequency edge connectors that do not cause waveshape distortion when rise times are under 1 ns [Bloo82]. The few that do not are of the "matched impedance" type in which the on–board strip transmission line flows right into and out of the connector, without encountering a mismatch. Unfortunately, this type of connector is usually expensive and it is often difficult to design with.

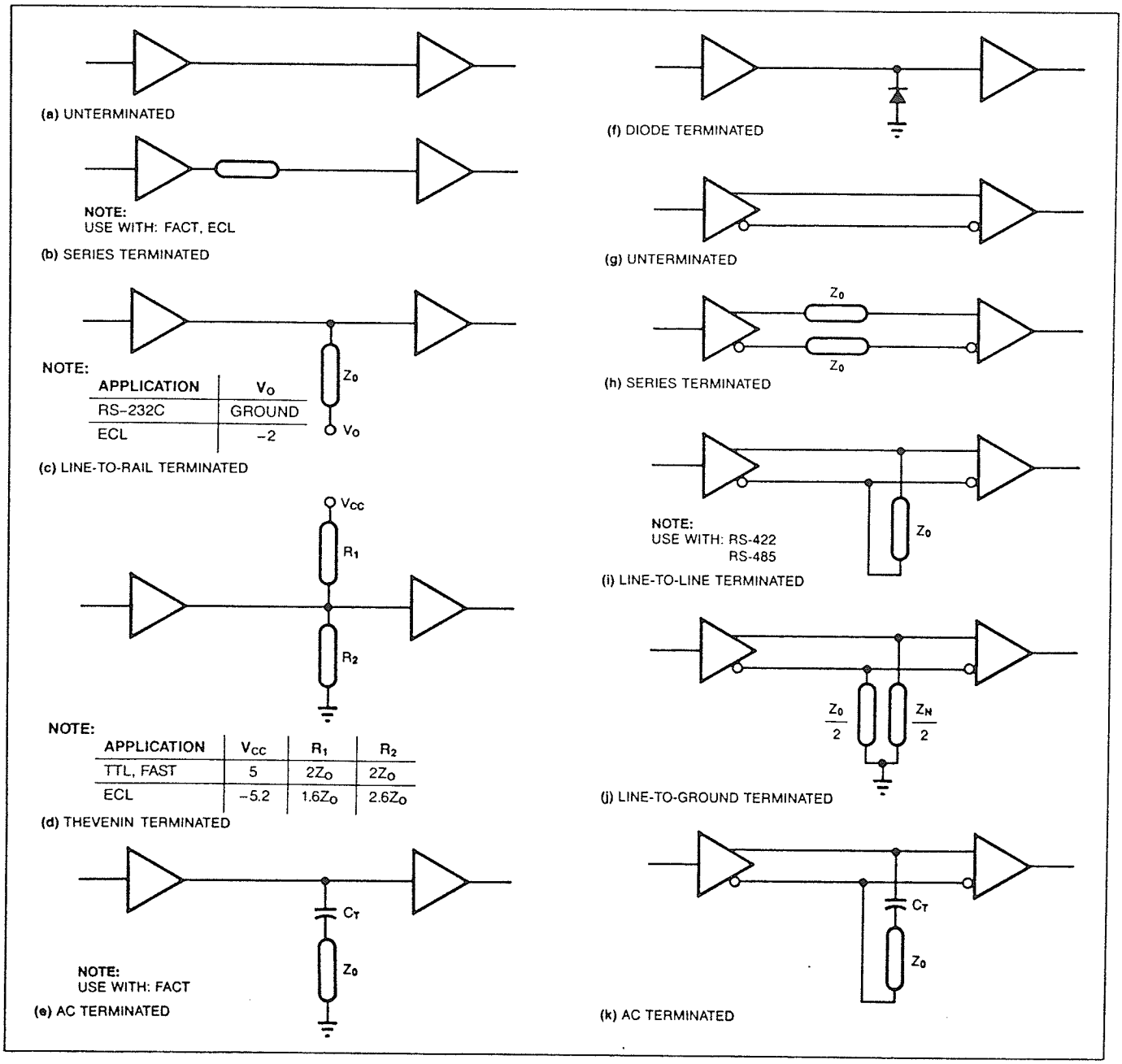
Coaxial cable connectors that have near ideal characteristic over their bandwidths (B) exist in a variety of types. The most popular are BNC connectors. BNC type connector which is not expensive but has a limited bandwidth ($B \leq 2GHz$) and big physical dimensions. Subminature SMA, SMB, or SMC type connectors which offer direct microstrip to coaxial interconnects with low voltage standing ratio (VSWR), i.e. minimum reflection. The bandwidth for SMA type is 8 GHz. The bandwidth for SMB and SMC type is 4 GHz. These connectors are usually expensive. The N type connector which has the best characteristics and the bandwidth (20 GHz) but is rather big. Very often the coaxial cable is directly soldered to the on–board strip transmission line.

3.4 Terminations

It is very important to terminate transmission lines with resistive load equal to the characteristic impedance of the line. The reactive components of the termination can change the terminating impedance, thus causing reflections on the line. In addition, the effective inductance or capacitance would distort the output waveform, causing additional reflection down the line.

Standard carbon resistors display more inductive reactance as the resistor values become smaller, and display more capacitive reactance as the values get larger [Bloo82]. One can choose one of the numerous methods for terminating transmission lines shown in Fig. 3.2.

This chapter was about crosstalk and reflections. Useful formulas were quoted. Connectors and terminations were also described.



You can choose from numerous techniques *for terminating single-ended and balanced transmission lines. Diode termination, shown in (f), usually doesn't require discrete diodes for digital logic. The diodes are within the gates that act as receivers.*

Figure 3.2: Techniques for terminating transmission lines. From: [Royl88].

CHAPTER IV

PCB COMPUTER–AIDED DESIGN AND ENGINEERING

In this chapter, the PCB design process with CAD/CAE tools is described. The design of PCB may be automated by using the CAD/CAE system. The author had an opportunity to work with PCB CAD package Optimate. He also used PCB CAD software called Visula*. They where installed on the Apollo workstation computers. For simulation, Greenfield and Spice simulators were used.

Automation of the engineering, design and electronic manufacturing activities typically leads to: Computer–Aided Engineering; Computer–Aided Design; and Computer–Aided Manufacturing. Computer–Aided Engineering (CAE) is responsible for: design creation; and design analysis. Computer–Aided Design (CAD) is responsible for physical design. Computer–Aided Manufacturing (CAM) is responsible for: process planning; materials management; production scheduling; tool development and generation; fabrication; assembly; and test [Skom87].

One of the more fundamental considerations in an automated design environment is the use of a grid pattern to define the relative positions of component pins, obstacles, connectors, conductors, etc., on the board. Typical grid sizes are 0.100 in, 0.050 in, and 0.025 in, where the value defines the dimension from grid line to grid line. The minimum practical grid size is typically determined by the desired width of printed circuit conductors and the spacing between conductors [Clyd86].

* $Visula^{TM}$ is a trademark of Racal–Redac Inc., Westford, Mass., USA

It is significant that the use of automated design techniques will often permit the use of a smaller grid size than nonautomated practices will permit. This results from the high precision with which the finished artwork can be produced and the hole drilling process controlled.

"Predictable and guaranteed functionality of logic circuits has become increasingly important as advances have been made in integrated circuit fabrication. The density of circuits on a chip and their logic state transition speed have increased to such an extent that the transportation of digital signals is very much dependent on the design of the packaging environment through which they are transmitted. Also, as the system cycle time decreased — a consequence of increased circuit density and speed — the effects of circuit and package delays, matched terminations of signal paths, noise induced in these paths, and overall control of package parameter variations became increasingly critical to overall system peformance" [DeFa70].

The applications of PCB CAD/CAE system are very wide and the system can be used to (the design is done in this sequence) : create a circuit schematic; simulate circuit conditions; provide waveform analysis of simulator outputs; layout and route the corresponding PCB which may be done manually, semimanually, or automatically; check the PCB design; produce reports, plots and artworks; produce the drive files for manufacturing machines such as photoplotter, numerically controlled drilling machine and (or) inserting machines; store designs; update designs; use data from other sources; and communicate with other design systems.

4.1. Preparation for use

The first step is to determine the job parameters, bring the job into the system and set up the system. A database of design data must be created to provide the necessary source of information for the schematic design, layout and postprocessing. For each component used, the appropriate data describing electrical properties and mechanical shape with detailed and accurate dimensions and descriptions must be created and stored in the library of components.

The system usually has a library of standard components. However, there are usually many specific components used in the design for which schematic symbol and mechanical shape have to be created and placed in the components library. This requires a lot of work, but when it is done, the component may be used in other designs. Therefore the size of components library usually determines the usefulness of the CAD system.

4.2. Schematic design

The next stage of PCB design is schematic design. Designs are developed by editing the sheets (pages which contain parts of the circuit schematic) by adding, altering and removing component symbols and annotations. An individual design is referred to by its job name. All the sheets of a circuit design and control information associated with them, are stored in a computer file referred to as a job file, which has a unique job filename.

Having drawn a part or the whole of the PCB design the job can be saved for use at a later date. The design is done by using Circuit Modeller and viewing it on the computer screen. It is very easy to make changes and modifications. The output can be easilly scaled.

The completed schematic design contains all of the electrical components and connections which are used in the circuit. The schematic design is used to:

- interactively design an elctronic circuit;

- produce a finished schematic from an engineer's sketch or drawing;
- produce an output file for the PCB layout;
- produce a circuit description (netlist) file for use by a circuit or logic simulator;
- produce an output drive file for hardcopy generation machine (pen plotter, photoplotter, raster plotter, thermal plotter, etc.).

4.3 PCB layout

The output file from the schematic design part is taken as an input by the layout part of the system. First the board outline is produced with automated routine and the tooling holes are located into the required position. They serve as registration marks and are very important for the mulilayer boards. Next using the placement program the components are placed on the board.

4.3.1 Component placement

The objective of the designer in achieving the proper layout is to position the components for optimum function and minimum cost. This naturally implies that components should be easy to load into the board and that there should be no thermal or electrical problems as a result of their placement. The component placement should be such that it simplifies circuit routing and other features of board design. Also, random orientation of component body axes should be avoided. Component leads of widely differing voltage should be separated as much as possible. Fragile components should be mounted in protected areas [Clyd86].

There are several algorithms for automatic placement [Ohts86]. Automatic placement can be very useful for designing boards with typical circuits and standard components.

Good results may be obtained by using a semiautomatic placement method in which the components are first automtically located on the board and then they are interactively (manually) moved and placed into the optimal position on the board

by the designer, according to his knowledge of the component type, circuit, and the net connection.

The placement is very important and crucial to the success of the design. Many factors must be taken into consideration in the placement process, such as speed of operation, heat generation by the components, sensitivity to noise and radiation, radiation generation, mechanical dimensions, etc. .

Components performing the same function should be grouped into blocks and placed in proximity to each other to reduce the length and number of interconnecting lines. Blocks which generate electromagnetic radiation should be shielded. Blocks which are sensitive to radiation also require shielding.

A special attention must be given to the high–speed circuitry — the interconnection lines should be treated as transmission lines which must be short enough or properly terminated to avoid reflections. The high–speed circuits should be kept close together. High–speed circuits and interconnections require careful crosstalk analysis.

4.3.2 Conductor routing

The next step after placement is routing. The power and ground are usually routed first — they should have very low resistance, and therefore, large widths of the traces should be used. In high–speed boards the power and ground are distributed by separate layers of copper called powerplane and groundplane, which also serve as reference planes (AC ground) for transmission lines design.

There are algorithms for automatic routing [Ohts86]. After finishing of routing the layout should be checked. Checking of electrical connections of layout with the netlist produced from schematic design is usually automated. The checking program produces a list of errors which is helpful to correct the layout [Ohts86].

4.3 Marking, post–design processing and artwork generation

High quality marking inks currently available for use on PCB allow the designer to place almost any marking in the design that is needed. These marking inks are capable of surviving solder flux, solvents and extreme heat. The following types of marking are required [Kear87]: board or assembly part numbers; component designations; polarity designators; plant or vendor codes; revision levels; manufacturing date codes; and pecial markings such as strapping instructions. Some of these can be incorporated into the etching pattern and others will necessarily have to be screened over the conductors (silkscreen).

Post–design processing is the stage in the design process in which drawings for documentation and output files to be used in the manufacturing process are produced from a design. It is possible to produce a check plot at almost any time to monitor the progress of the design. This can be especially usefull for checking component placement, routing, assembly and drill drawings, and master schematics of the circuit [Skom87].

Post–design processing is used to produce: a pen, photo, thermal, or raster plot of a schematic and layout designs, or simulation results; outputs for numerically controled (NC) drilling machine or automatic component insertion (ACI) machine; output for use with automatic test equipment (ATE); and documentation, parts lists and reports [Skom87].

Output for the manufacturing process can include: photoplots for copper etching (Artwork); photoplots for Solder Mask; photoplots markings (Silkscreen); and drive files for NC drills, ACI and ATE machines and similar equipment.

Artwork is basically a manufacturing tool, although it is often prepared by the designer. Highly accurate, properly scaled, original filmwork is the necessary first ingredient for successful high density designs. Hand–taped designs are not longer an option because they introduce so much inaccuracy into the filmwork. But even filmwork which is plotted from CAD output at the customer site or by a third party

introduces inaccuracies. Exposure to changes in temperature and humidity causes changes in the filmwork which may require the PCB vendor to photographically manipulate the filmwork back into tolerance [Skom87].

The most accurate filmwork and drill information are generated directly by the PCB vendor from CAD output sent via mag tape or high–speed modem [GrHi87]. This allows the vendor to generate filmwork using a laser plotter and to maintain all film from its inception in a controlled environment. CAD–generated filmwork which is highly accurate increases the tolerances for fine line manufacturing. Another method of increasing manufacturing tolerances is through planning to maximize line width except in critical areas of the board. Line width is easier to control on innerlayers because the vendor is only etching original copper [GrHi87].

The documentation of PCB should include at least the following drawings [Clyd86]:

1. A *Schematic Diagram* indicates with graphic symbols the electrical connections and functions of a circuit and thereby enables the user to test, evaluate, and troubleshoot;
2. The *Master Drawing* contains all the information for the manufacture of PCB;
3. An *Assembly Drawing* is a pictorial representation of the finished, assembled board and lists all the electromechanical items contained on the assembly;
4. *Artwork* is an accurately scaled configuration of the PCB from which the master pattern is made photographically;
5. *Miscellaneous Drawings* are prepared to support either the master or the assembly drawings.

4.4 Data base for manufacturing process

Managing the product data base from design through production becomes a very complex task. Electronic manufacturers typically have two major organizational groups with product data base responsibility: design and manufacturing. Engineering departments create product designs and are responsible for removing design errors. The manufacturing operation is responsible for producing the product in conformance to the specifications and design data provided by engineering [Skom87].

According to Skomp, [Skom87], one of the major differences in the data supplied by engineering design and that needed by manufacturing is in the area of panelization. Engineering provides design data for single PCBs, but manufacturing works with large panels which may contain several copies of the single PCB. While many CAD/CAE systems supply data for photoplot, drill, profiling, and autoinsertion machinery, most do not concern themselves with the need for generating this data in panelized form for the manufacturing environment.

The computer hardware, software and communication networks used for manufacturing data base management usually will not be the same as that used in engineering and design. RS–232 and Ethernet networks are usually used for data communication. The data must be in the proper format for use by the computer hardware and software. Support of data base standards such as EDIF and IGES eases the task of product data base generation and reduces the development effort when a standard interface exists.

Data must be available from a number of sources (CAE, CAD, CAM) to a variety of tool generation, fabrication, assembly, and test equipment. Each equipment used in manufacturing (such as: photoplotter; NC driller; NC router; autoinsertion; pick–and–place; bare board test; and in–circuit test equipment) needs specific data in its own format. Extracting data for each of these machines is extremely important in the manufacturing environment [Skom87].

Table 4.1: Data requirements of manufacturing equipment [Skom87].

Photoplotter	Complete grafics for traces, pads, vias, silkscreen, solder masks
NC drill	Hole size, coordinates, drill drawing
NC profiler	Commands, path coordinates
Autoinsertion machines	Component type, coordinates
Pick–and–place machines	Component type, coordinates
Bare board tester	Pad and via coordinates, connectivity
In–circuit tester	Component type, pad coordinates
Functional tester	Component type, pad, via, coordinates, netlist

Data, including complete revision information, should be managed for each board which is manufactured. This is very difficult because data must be consolidated and made available not only within engineering, design and manufacturing, but to every functional area concerned with the life of the product, such as production planning, purchasing and accounting [Skom87].

In this chapter, some aspects of automated design and manufacturing were described. The CAD design process and the terminology were explained. CAM manufacturing process and necessary data base were described.

CHAPTER V

COMPUTER–AIDED ELECTRICAL ANALYSIS

This chapter is about computer–aided electrical analysis. Various types of simulators and their applications, and device modelling are briefly described. Today's high level of integration can lead to very large and complex systems with extremely small physical dimensions. An electrical analysis which excludes coupling among the closely spaced components is no longer sufficient. The interconnections are now very important elements in the equivalent circuits [Rueh87].

Thus, the circuit models for integrated circuit systems are extremely complex, with highly coupled components. An electrical analysis of these models without CAD/CAE techniques is not possible, especially for high–performance systems. The type of analysis required for a particular system depends on its performance and purpose. Low speed or low frequency circuits may require a quite simple electrical analysis. In contrast, complex models are required to represent high speed or high performance systems [Rueh86].

The computer aided electrical analysis approach implemented in $Greenfield^{TM}$ CAE package is based on electromagnetic field theory and circuit theory. $Greenfield^{TM}$ is the family name and the package includes — $Greenfield2d^{TM}$ which is 2–dimentional field solver; $Greenfield3d^{TM}$ which is 3–dimentional field solver; and $Phyllis^{TM}$ which stands for Physical Load and Line Simulator — the electrical network analyser. These field solvers produce data which can be accepted by a popular analog simulator, called Spice [PoWe86].

In Phyllis the unknowns are expressed in terms of voltages and currents and this allows the use of well–known circuit theory concepts and models. The interconnection analysis of a system consists of several steps. First, the appropriate models of circuit elements must be determined and the capacitanes, inductances and resistances must be computed. Then an analysis is performed to obtain the signals of interest, namely the voltages and currents, from which we evaluate the electrical operation of the hardware being modelled.

Typical electrical design criteria which must be met by a hardware design can be summarized as follows for the example of a digital system [Rueh79]. All signals in the system must meet the timing requirements. The signal wave shape must be within given tolerances.

Unwanted signal coupling (crosstalk) between wires must be less than an upper bound so that the coupled signals do not cause improper switching of the logic circuits. Voltage transients on voltage and ground distribution wires induced by switching circuits must be limited to small fractions of the supply DC voltages. External electromagnetic disturbances should not cause false switching of the digital circuits. Thus, the purpose of computer aided electrical analysis and simulation is to ensure that the hardware will meet these electrical design criteria [Rueh79].

Capacitance computations are of central importance for the electrical representation of interconnections. The capacitance matrices can be computed very accurately by using Greenfield2d. In most applications, there are problems which can be approximated by two–dimensional computations. Examples are transmission lines with a length much larger than the cross–sectional dimensions and spacings. Greenfield2d can be used in these cases.

5.1 Types of simulators

Analog circuit simulation is the most accurate form of simulation available to electronic designers. If the devices and circuit interconnections between them are accurately modelled, circuit simulation programs can predict circuit characteristics extremely accurately. The most popular circuit analysis program is Spice from the University of California at Berkeley [Nage75]. The most common analysis types performed are : DC; small signal AC; and time–domain transient. Of these, one of the most useful, and the most computationally expensive, is time–domain transient analysis.

Analog, timing, switch–level, logic, register–transfer and behavioural simulation are all based on abstract models of a design. All simulators can simulate circuits in constrained design styles, but may produce incorrect answers when given a problem too difficult for them to solve. Deutsch gives an intersting description of above mentioned simulators in [Deut86], which is summarized below.

Behavioural–level simulation allows verification of the correctness of an algorithm and is commonly used to model computer instruction sets. Behavioural level descriptions of systems do not contain any structural information. Often behavioral–level models of systems are built with standard programming languages.

Register–transfer level simulation is the highest level of simulation to model aspects of the interconnection topology of a system and can be used to verify the functional correctness of a block–level description of a circuit.

Logic simulation models a system as a collection of unidirectional gates, where the signals passed through the network are discrete events which have a logic level and a strength, and can be used to verify that the logic description of a design is correct, and provide first–order delay predictions for combinational networks. Because the elements they model are unidirectional, pure logic simulators can not simulate networks containing pass–transistors and energy charge storage nodes. Many commercial logic simulators contain elements of register–transfer level

and switch level models, and as time goes on, the models used in logic simulators become more complex as more levels and states are added.

Switch–level simulators model a network as a collection of storage nodes and bidirectional transfer gates, connected by ideal wires. Switch level simulators can verify functional correctness of simple MOS networks, but can not provide accurate timing estimates or simulate circuits containing resistors or bipolar transistors.

Timing simulators model a circuit as an electrical network, containing MOS transistors, resistors and capacitors, and use simple models for the transistors. They are simplified models for active devices, combined with fast but approximate and sometimes unstable solution techniques.

Analog circuit simulators model an electronic circuit as a collection of capacitors, resistors, voltage sources, current sources, diodes, transistors, and so on. Each of these components is described by a mathematical model. A large system of equations is then formed, based on the application of Ohm's law, Kirchoff's voltage law and Kirchoff's current law, and the system of equations is solved to produce the behavior of the circuit as a function of time or frequency.

Analog circuit simulation can provide **accurate simulation of any network** that can be constructed out of the elements provided in its model library, independent of any particular design style. In addition, analog circuit simulation can pinpoint logic level and noise margin problems, expose capacitive feed–through, measure static and dynamic power consumption, and show the effect of temperature and manufacturing process variations on the performance of design [Deut86].

5.2 Circuit design with simulator

Simulation makes it easy to try out a variety of design alternatives. Circuit design can be broken down into two phases. The first is choosing the circuit topology, and the second is choosing values of the components to optimize the performance of the design. In most cases, a designer is faced with multiple, possibly conflicting, goals and constraints. Design optimization can be done manually by performing repeated simulations, varying the values of the component parameters each time in an attempt to find the optimal values. Much of this process can be performed automatically by using optimization techniques [Rueh87].

One of the most frequent uses of circuit simulation in digital circuit design is to accurately characterize the speed of a circuit. Usually there are a small number of critical paths in a design that determine the overall speed of a circuit. Often, careful simulation and optimization of these paths, treated as transmission lines, can result in a performance improvement of several times over an unoptimized design. Optimization of designs usually proceeds by a sequence of individual incremental changes, each of which affect circuit performance by a few percent. This requires that the simulation be as accurate as possible [Rueh79].

There are basically five steps to simulate a circuit: describe the circuit; describe the semiconductor devices; define the simulation type; perform the simulation; and interpret the results [Dive88].

Until recently, analog circuit simulation was difficult for the majority of circuit designers to use because the input circuit description was cumbersome, simulators lacked accurate and extensive models, especially of semiconductor devices, and results were difficult to interpret [WaCr86].

To use Spice, one must first construct a description of his circuit, called a Spice deck. The net–list is constructed by first numbering all of the nodes in the circuit and then typing in a file that describes the connectivity of the circuit and the

component values. It is difficult and time–consuming to build the circuit description correctly and find any errors [Rueh79].

Next, the process of describing semiconductor device parameters to Spice can be overwhelming. There are over forty parameters used to describe a bipolar transistor, and only one of these is directly determined from measured data; the others must be derived. Thus a designer can spend more of his time characterizing a transistor than he does designing his circuit [Deut86].

To achieve maximum benefit from circuit simulation, the circuit simulation system should have the following attributes: **simulation accuracy** assuring that the results of simulation are valid; **extensive model library** so that designers need not devote more time to developing models than designing circuits; **schematic capture** to create schematic using on screen technique of editing instead of developing net–lists; **preview of results** showing the output waveforms in the convenient form for comparison to actual circuit measurements; **hardcopy facility** for storing results and producing documentation; and **complete simulation tools** including transmission lines, Monte Carlo, sensitivity, worst case, and "what if" analysis [Deut86].

5.3 Device models

This section is about device models and their types. According to Deutsch, [Deut86], device models are the link between the circuit simulation program and the fabrication process used to manufacture the design. If the models for the devices used in the simulator are not accurate, or if the model parameters used do not reflect the characteristics of the process, the simulation itself will not be accurate.

In addition, it is important to model the effects of voltage on both current and charge. Unless this is done, the numerical errors involved in converting charge to current and back again can seriously impact the accuracy of the simulator. The concept of charge conservation is critical for accurate simulation of circuits such as

switch capacitor filters, high performance amplifiers, and dynamic RAMs. For a circuit simulator to be charge conserving, it is necessary to use charge as a state variable in the equation formulation [Dive88].

Device modelling is an important aspect of circuit simulation — since any analysis is only as accurate as the model used. Semiconductor device models fall into three basic categories [Deut86].

Physics–oriented models, such as Level 2 model in Spice–2, attempt to model the underlying physics of the semiconductor device. Although they can be quite accurate for long–channel devices, such models tend to be less accurate for modern short–channel or narrow–width devices, because of the difficulty in creating accurate analytic expressions for these effects.

Measurement–oriented models, such as CSIM, and BSIM models, are gaining popularity because they can accurately model modern devices, even when the physics is not completely understood. In many cases they are also substantially more computationally efficient than physics–oriented models of similar accuracy.

Table models can provide extremely accurate results because they are based purely on measurements of device characteristics, with minimal reliance on assumptions about the underlying device physics. In addition, they can be even more computationally efficient than measurement–oriented models. Although table models have been used in the past in logic and timing simulators, new high–accuracy table models for circuit simulation are just begining to appear.

Currently available circuit simulation programs, such as Spice–2, have a variety of built–in models. The most important are: PN–junction diode and Schottky diode; bipolar junction transistor (BJT); junction field–effect transistor (JFET); metal semiconductor field–effect transistor (MESFET); and metal oxide semiconductor field–effect transistor (MOSFET) [Nage75]. Usually, significant portions of resources are devoted to model development and a combination of manual and computer–aided techniques are used to derive the necessary parameters.

The new version of Spice called Spice 3 is written in C instead of Fortran and it is more efficient and faster then the previous version Spice 2G.6. For instance, transient analysis runs twice as fast under Spice 3. Spice 3 also has four new device models not included in Spice 2G.6. A BSIM MOSFET model overcomes short–channel deficiencies in MOSFET simulation and there is a model to simulate uniformly distributed RC transmission lines. The last two models are for semiconductor resistors and capacitors [WaCr86].

In this chapter, computer aided electrical analysis and various types of simulators were described. The features of a good simulator were listed. The importance of accurate device models was emphasized and types of device models were described.

CHAPTER VI

MEASUREMENT AND TESTING TECHNIQUES

In this chapter, a digitizing oscilloscope, a novel measurement instrument, and measurements with digitizing oscilloscope are described. The digitizing oscilloscope, model HP 54201D, with the repetitive bandwidth of up to 300 MHz, was used for measurements. Some digitizing oscilloscopes have a bandwidth many times higher than their sampling rate. For example, the HP 54100A/D has a sampling rate of 40 MHz and a bandwidth of 1 GHz.

Typically, the lower price of the oscilloscope the lower is its bandwidth. Digitizing gives an extra convenience and precision of measurements. By using this setup, we measure crosstalk and ringing for signals with rise and fall times corresponding to ECL and high–speed TTL circuits. A high–speed TTL–level signal was used for measurements which are described in Chapter VIII. Results are also included in Appendix A.

The time domain reflectometer (TDR) measurement technique is described. The TDR technique offers GHz range bandwidth which represents the practical limit for the bandwidth used in high–speed PCBs. Above, there are microwave applications. The TDR setup measurements were performed with the signal with 150 ps rise time which corresponds to the GaAs circuits. Results are included in Chapter VIII, and Appendix C.

These two setups cover most of the practical applications. The last part of this chapter is about testing of high–speed boards and devices. All practical active

devices are nonlinear. The problems with testing of high–speed, nonlinear devices and circuits are described.

The measurement and testing of printed circuit boards give very important information and it is the best way to verify if the design is valid. It requires the designing and manufacturing of the prototype which is usually time consuming and expensive. By measuring the basic properties of the PCB it is possible to predict problems and make a good design without too much prototyping.

6.1 Measurements with digitizing oscilloscope

The oscilloscope can make important time–domain measurements. The digitizing–scope provides the same capability of measuring the performance of a circuit as the analog scope. However, it also provides more accurate, more repeatable, and more easily documentable measurement capability than the analog–scope. The microprocessor–based digitizing–scope has some everyday–use features that decrease the time required to learn and operate the scope and increase productivity.

The *Autoscale* feature selects the vertical offset and sensitivity, the time base sensitivity, and the trigger criteria in order to display the input signals on the CRT screen. This is done by the CPU in the digitizing–scope and usually takes less than 3 seconds. The user can access the *Time Base, Channel and Trigger* menus to choose the time base sensitivity, the vertical offset and sensitivity, or the trigger criteria [Digi88].

A *Measure* menu gives access to various measurement tools that allow automatic pulse parameter measurements and recordings. This is an important advantage because the scope's computer can perform measurements faster, more accurately, and more reliably that can be done manually by multiplying the number of divisions read from the screen times the scale [Digi88].

The user can store away the digitized representation of the input waveform in non–volatile memory. This method of waveform saving is superior to the temporary

storage of an analog scope's screen or the permanent storage using a scope camera because it is easier and faster. The CPU keeps all setup factors required to redisplay the memory.

One can use computer as remote controller of digitizing–scope and other compatible measurement instruments through HP–IB interface (IEEE–488 standard). If one is using a controller, (e.g. IBM PC compatible computer with HP–IB interface board), he can program the scope and store waveform memories to a disc drive. Programming the digitizing–scope or any other instrument involves the controller sending a series of commands to its HP–IB port, thus causing the scope to perform tasks that are sent to it. The language of commands sent to the scope is an English based and easy to use. It is possible to extract the digitized data into a controller to perform any required manipulations and calculations [Volt86], [Digi88].

The user can get a hardcopy of the CRT display with all of the scaling factors and scope setup factors, as well as all the measurement results, in 10 to 45 seconds. He can use printer or plotter connected to the HP–IB port.

Bandwidth, along with its time–domain equivalent, rise time, has historically been the principal figure of merit for oscilloscopes. The practical relationship between bandwidth and rise time is:

$$B = \frac{0.35}{t_r} \tag{6.1}$$

With the increasing popularity of digitizing oscilloscopes, sampling rate, or digitizing rate, has attracted almost equal attention as a figure of merit [Band86], [Digi88]. The relationship between bandwidth and sampling rate has given rise to a lot of confusion.

Most oscilloscope measurements are time–interval measurements. When the input voltage changes, the oscilloscope can not exactly reproduce the input signal at every instant of time, due to the transient response of the osciloscope. In general, the

greater the oscilloscope's bandwidth (conversly, the less its rise time), the smaller the errors of measurements.

In a digitizing oscilloscope, the input signal is sampled and the waveform is quantized into discrete time and voltage samples. There are at least three methods of sampling the signal: **real–time sampling; sequential sampling; and random repetitive sampling.**

In **real–time sampling**, the signal is digitized on the fly, in real time. There is a simple 1:1 correspondence between the samples and the times at which they were taken. The advantage of real–time sampling is in single–shot measurements. All the data about the signal is acquired in one acquision cycle [Volt86].

In **sequential sampling**, only one sample of the signal is digitized on each occurance of the trigger. With each succesive trigger, the sampling point is delayed further from the trigger point. After many samples are acquired and digitized , the signal is reconstructed in the oscilloscope's memory. Sequential sampling requires that the signal be repetitive [Volt86].

Random repetitive sampling is similar to sequential sampling , except that the signal is constantly sampled and digitized at a rate determined by the oscilloscope's sampling clock. To determine the time relationship of each sample to the trigger event, the time between the sample clock and the trigger event is detected. The signal is reconstructed after many samples are acquired, so a repetitive signal is required [Volt86].

Some digitizing oscilloscopes have a bandwidth many times higher than their sampling rate. For example, the HP 54100A/D has a sampling rate of 40 MHz and a bandwidth of 1 GHz. This is achieved by using a wideband preamplifier and a narrow–aperture RF sampler ahead of the A/D converter. To view a high–frequency signal, many samples acquired at different times are overlaid in correct time relationship to one another. The time relationship is preserved by the trigger

circuit. The bandwidth for repetitive signals is limited only by the bandwidth of the preamplifier and the aperture width of the sampler [Band86].

The measurement setup (Fig. 6.1) consists of the digitizing oscilloscope HP 54201D with the repetitive bandwidth of 300 MHz, the programmable waveform generator, the scaled PCB with the measured traces and the colour plotter.

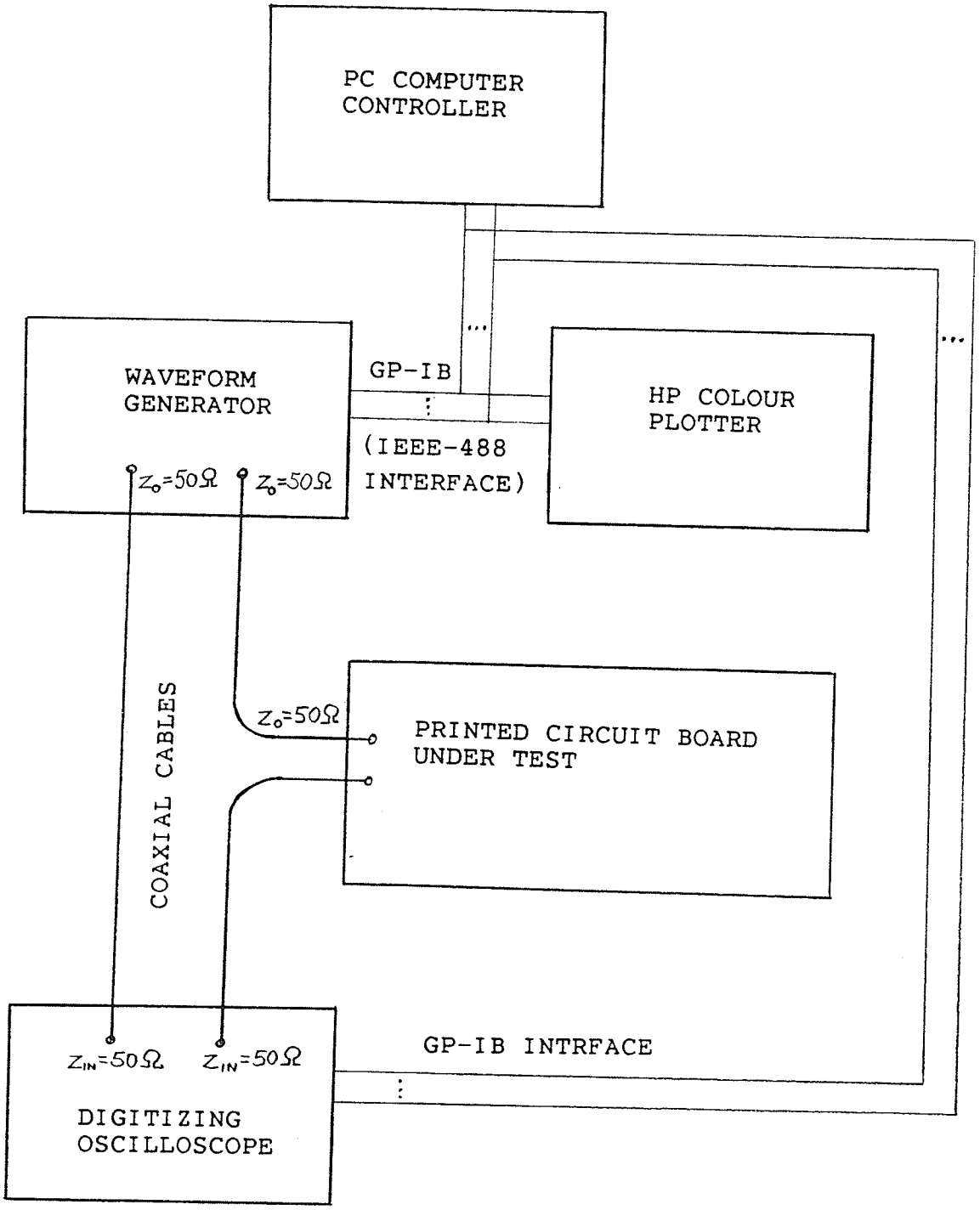


Figure 6.1: Oscilloscope measurement setup.

6.2 Measurements with time domain reflectometer (TDR)

The time domain reflectometer (TDR) can make important time–domain measurements. The TDR provides the capability of measuring the performance of a very high–speed circuit as the microwave range analog scope. However, it also provides other measurement capability than the high–speed analog–scope [Bloo82].

The TDR model HP 1415A, which was used for measurements, has the following main technical specifications: system rise time is less than 150 ps and repetition rate is 200 kHz; oscilloscope signal channel rise time is approximately 110 ps, and input impedance is 50 Ω, feed–through type; and pulse generator rise time is approximately 50 ps, amplitude is approximately 0.25 V into 50 Ω (0.5 V into open circuit), and output impedance is 50 Ω.

It was necessary to use an oscilloscope camera to capture the waveforms. The author found an effective method of illuminating of the oscilloscope's screen to enable taking of pictures of resonable quality.

The pulse generator of the TDR has rise time equal 50 ps. The bandwidth equivalent of 50 ps rise time is 7 GHz. The oscilloscope signal channnel of the TDR has a rise time of approximately 110 ps. The bandwidth equivalent of 110 ps rise time is 3.5 GHz.

The overall TDR system buit from the pulse generator, oscilloscope, connectors and cables has the rise time of approximately 150 ps. The bandwidth equivalent of 150 ps rise time is 2.1 GHz. It was measured from the pictures taken that the rise time of the TDR system was approximately 150 ps. This is well a microwave range of operation, not available for any other standard type of equipment.

The time domain reflectometer (TDR) employs a step generator and an oscilloscope in a system to measure reflections (Fig. 6.2.a). In operation, a voltage step is propagated down the transmission line under investigation. Both the incident and reflected voltage waves are monitored on the oscilloscope at a particular point on the line [Bloo82].

The incident voltage step, E_i, is a positive edge with an amplitude of 0.5 V and a rise time of 50 ps. It is generated by a tunnel diode, which has a source impedance of 50 Ω (Model HP 1415A). Also, the output edge has very litle overshoot (Fig. 6.2.b).

This TDR technique reveals the characteristic impedance of the line under test (Fig. 6.2.c). Figure 6.2.c shows the reflected signal from a microstrip with two corners. The signal is transmitted through a coaxial cable which introduces the time delay equal to 4.08 ns (from point A to B). At point B, the signal enters the microstrip and there is an overshoot due to the impedance mismatch. After one time delay of the microstrip, which is equal to 3.6 ns, there is a small downward peak (point C) caused by the crosstalk coupled from the second, parallel arm of the trace. This point corresponds to the corners' position. After one more time delay of the microstrip, the signal encouters the termination and is reflected. Point D corresponds to termination equal to 50 Ω.

The vertical scale is calibrated both in terms of the voltage and the reflection coefficient, ρ. The characteristic impedance of the line can be determined from the equation [Bloo82]:

$$Z_o = (\frac{1+\rho}{1-\rho}) \cdot Z_{ref} \tag{6.2}$$

where: Z_{ref} = impedance of a known line (input line).

The measured microstrip line reflects a certain voltage (35.7 mV) due to change in the characteristic impedance of the line in camparison with 50 Ω. The calculated characteristic impedance of the measured microstrip is 67 Ω.

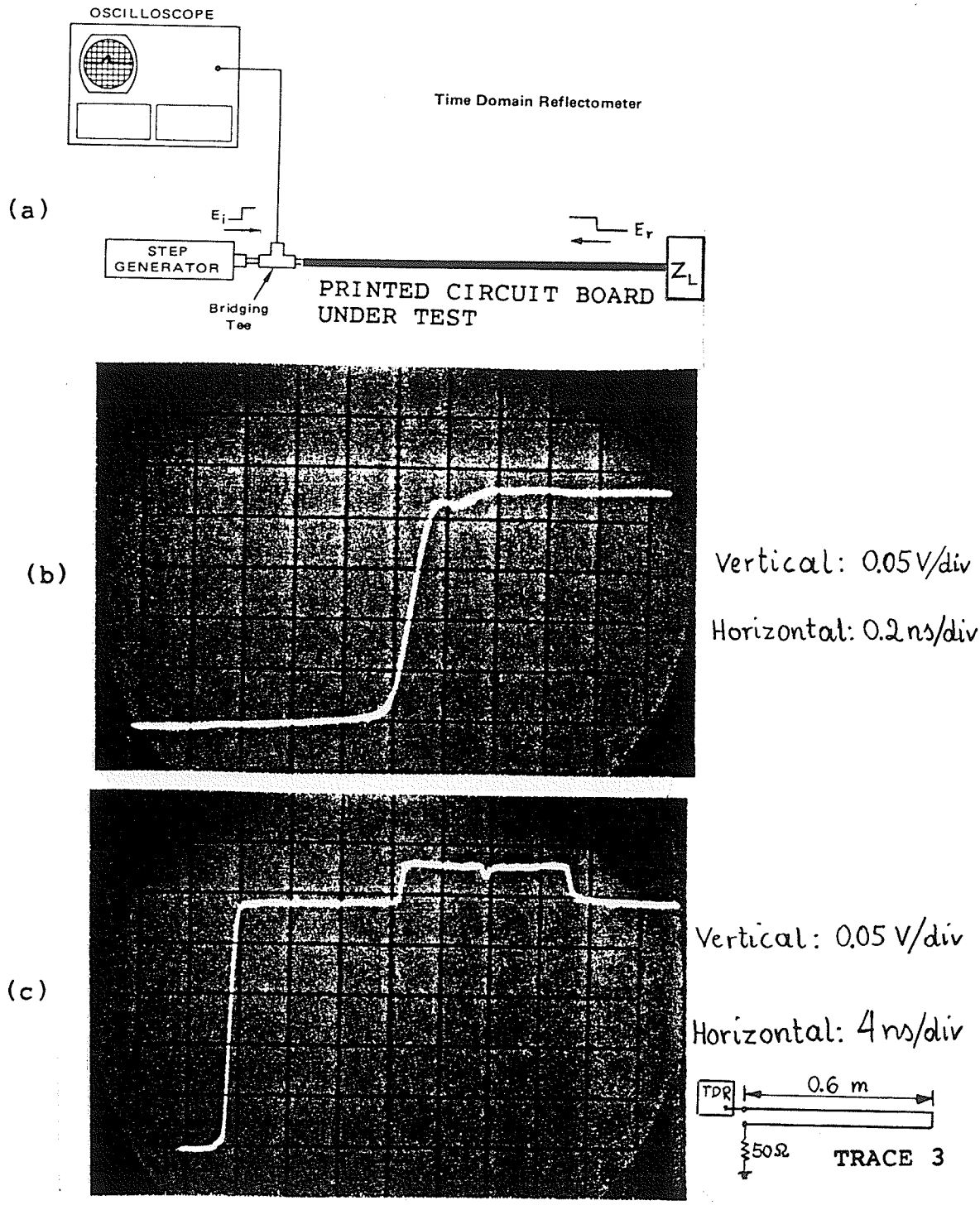


Figure 6.2: TDR measurement technique.
6.2.a TDR measurement setup (from: [Bloo82]);
6.2.b TDR generator output signal into 50 Ω load;
6.2.c TDR incident and reflected waveform from tested microstrip.

6.3 Testing of high–speed boards and devices

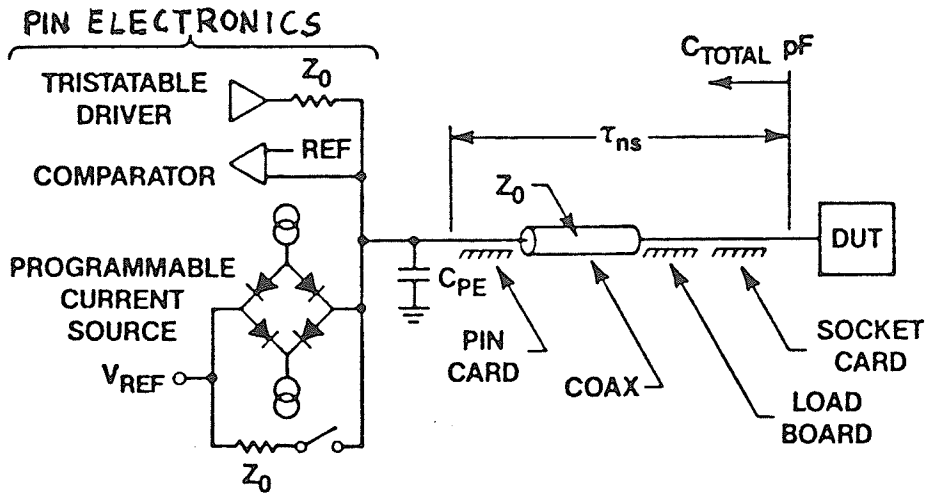
It is very difficult to test boards and devices under high–speed switching conditions. High–speed signals require special care to be measured properly. Special equipment is necessary with an adequate high bandwidth and proper input or output impedances. Special connectors, splitters, terminations and cables with controlled characteristic impedance must be used.

Todays's VLSI testers have 256–pin test heads with transmission lines leading from the device under test (DUT) to driver–comparator circuits that are as far as 50 cm (Fig. 6.3). The ideal system shown here (Fig. 6.3.b) consists of a high–impedance buffer amplifier with a specified load capacitor and programmable current source — all located within a few centimetres of the DUT. The measurement system includes (Fig. 6.3.a) transmission–lines and their properties have to be considered.

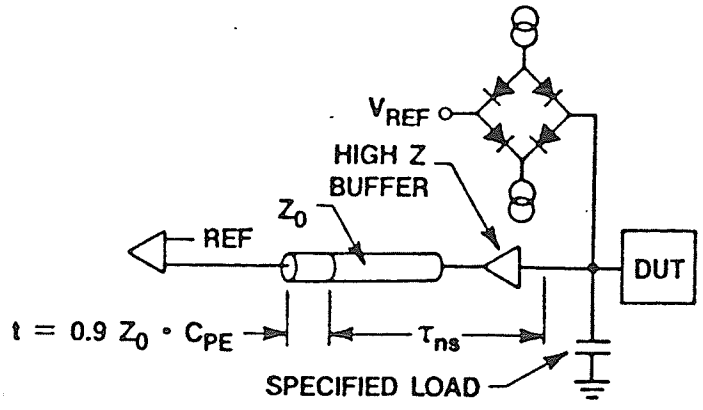
According to Barber, [Barb84], [BaSa87], even though these automatic testers are adjusted to subnanosecond accuracy, reflections within the transmission lines can cause timing measurement errors up to 10 ns for MOS devices whose output impedances are not matched to the transmission lines. Serious test problems occur when accurate timing measurements are required on the outputs of high–speed MOS or GaAs VLSI circuits.

Published results, [Barb84], [BaSa87], [Petr86], show that processing, temperature, and V_{DD} changes can cause the pMOS pull–up transistor impedance to fall from 120 to 30 Ω. During the trailing pulse edges, in nMOS pull–down transistor impedance can fall from 50 to 10 Ω, resulting in the very large damped oscillations. These oscillations, in turn, lead to highly ambiguous or erroneous timing measurements.

It is recommended that very high–speed ICs be designed to drive transmission lines that are terminated with matched resistors at the comparators. Transmission



(a)



(b)

Figure 6.3: Typical tester system. Modelled by (from: [Barb84]):

(a) typical pin electronics circuit;

(b) ideal measurement system, which incorporates timing delays to ensure identical comparator strobe timing.

line reflections could be eliminated by impedance matching at the comparators, but this method results in excessive power dissipation in the DUT.

Impedance matching is used to test ECL circuits, which are designated to drive 50 Ω loads. There is generally no problem in driving an input to a MOS DUT with accurately timed, high–fidelity pulses because voltages reflected from the high–impedance DUT inputs are absorbed in the matched source impedances of the test system drivers. Furthermore, the test system automatically accounts for transmission line delays [BaSa87].

According to Barber, [Barb84], [BaSa87], circuit designers and test engineers should cooperate in using a circuit simulator to study the interaction between the DUT and the test system and to develope an accurate technique for testing CMOS VLSI devices with low–impedance output buffer designed to drive TTL loads, or other high–speed devices. At least, low–temperature, fast process buffers should be simulated to determine whether or not series resistor must be added to the DUT output pins on the load board to prevent voltage ringing.

The simulation of the DUT should be extended beyond the high–current output buffers to include the transmission lines, the pin electronics, and any lumped capacitors or resistors added to the DUT outputs. Test engineer can then study the effect of the waveform reflections and estimate any errors in timing measurements on DUT output waveforms.

Barber further recommends that specified capacitors be added to the load board to reduce the need for pulse–edge timing corrections, which can change with processing variations. If the load capacitors are omitted, pulse–edge timing corrections from 3 to 12 ns must be included in the test program. Timing corrections are determined by comparing the waveforms for the simulated test system with those for a simulated ideal measurement system [BaSa87].

In this chapter, a digitizing oscilloscope and measurements with digitizing oscilloscope were described. Next, the TDR measurement technique was described. Difficulties in testing of high–speed boards and devices were also described.

CHAPTER VII

SIMULATIONS WITH GREENFIELD

In this chapter, first the computer simulation is briefly described. Next, field solver and analog simulators are presented. Results of printed circuit board simulation and computations of transmission line parameters are shown.

Greenfield is a family of integrated CAE software tools with unique capabilities to simulate PCB interconnect media, cables, connectors, hybrid and integrated circuits under high–speed switching conditions. Prior to prototyping, Greenfield can predict cross-talk, ringing, time–delays, parasitics and impedance mismatches [PoWe86].

Circuit simulation requires a lot of memory and a lot of computations. Therefore, workstations are necessary for performing actual computations. The PC–type computers can be used to preprocess data and to create schematic (Schematic Capture). The high–speed interface is necessary (e.g. Ethernet) for communication between PC and workstation to pass commands, data and results.

The results can then be displayed on PC with high–resolution graphics. This is a low cost and efficient solution for many users to do simulations and share computer resources. Usually, most of the time is spent on preparing data and creating schematic and next on interpreting the obtained results. This can be done with PC while heavy computations can be left for workstation and performed on request. The simulation setup is shown in Fig. 7.1.

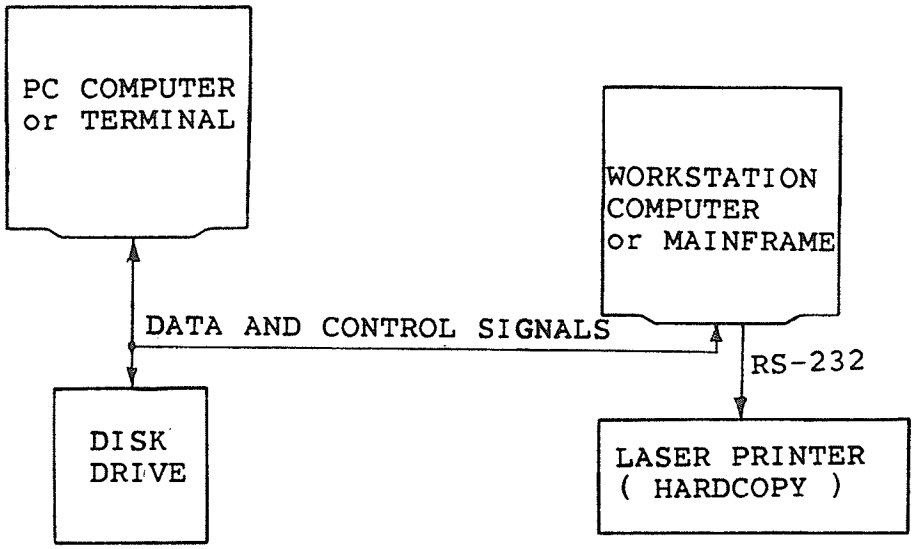


Figure 7.1: Simulation setup.

7.1 Greenfield2d field solver

The Greenfield2d is a field solver which uses the boundary element method as internal algorithm and requires the decription of modelled structure in the form of two–dimensional cross–section [PoWe86]. First the geometrical configuration has to be completed by drawing the cross–section on the computer screen with a number of graphical commands available (Geometric Modeller).

Next, the problem description requires a number of physical constants and mathematical parameters in order to yield the solution. The problem description includes: boundary conditions, material conditions, sources, and boundary elements. For example, to define boundary condition, one of the following must be selected: Dirichlet boundary condition (e.g. voltage specified); Neumann boundary condition (e.g. normal derivative of the voltage at the boundary); or interface boundary condition across boundaries between adjacent dielectric or other permeable media.

With the completion of the problem definition, the equivalent source distributions over all boundaries and interfaces must be found. The process involves setting up a system of simultaneous equations whose solution yields the equivalent source

distribution. The equivalent source distribution is used by a number of output routines to calculate potential distribution, in the form of contour or colour plots, and potential and field values at requested points [PoWe86].

7.1.1 Creating equivalent models of interconnections

Greenfield2d provides an easy method for creating equivalent circuit models. For example, microstrip and stripline transmission lines with multiple conductors and multiple dielectric layers can be easily modelled. Greenfield2d can determine the conductor losses, self–inductances, mutual–inductances, self–capacitances and mutual–capacitances of transmission lines, cables, and PCB interconnections.

With the geometry properly modelled and the problem appropriately defined, the user requests to solve for the equivalent sources on all the interfaces and conductor surfaces. Once the solution process is finished, the user has access to a number of output options. To obtain a capacitance matrix, the user is required to supply information on all the conductors and the ground. The capacitance and inductance matrices, time delays, and characteristic impedances are calculated and printed on the screen and stored in a file.

The cross–section of the simulated and measured two–layer PCB is shown in Fig. 7.2. The calculated transmission–line parameters include: capacitances; inductances; characteristic impedances; time delays; conductor losses; mode loses; and voltage and current eigenvectors [PoWe86]. Results for the simulated PCB which is shown in Fig. 7.2, are included in this section. The simulated characteristic impedance and time delay are in a good accordance with measured values.

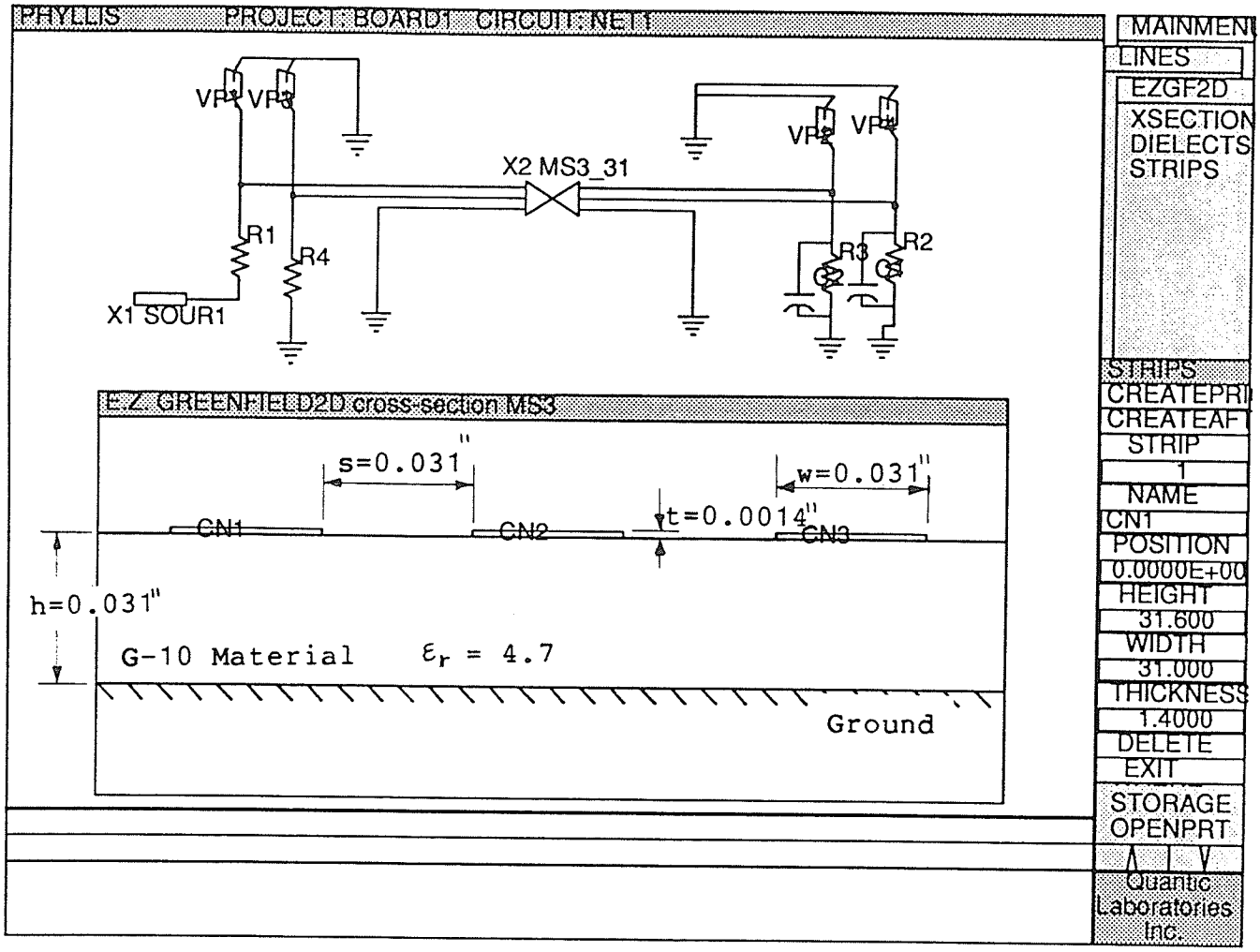
The cross–section of an example of a four–layer PCB (with two layers of microstrips, one stripline layer, one ground–plane) and its field distribution is shown in Fig. 7.3.

TRANSMISSION–LINE PARAMETERS OF SIMULATED MICROSTRIP LINES


```
***
*** File Conductors
*II MS3 3
*** Conductor names
*CN CN1 CN2 CN3
*** Frequency Dimension Material Conductivity
*GI 100.00[Mhz] [mils]  copper  5.800000E+07 [S/m]
***
*** Capacitance matrix [F/m]
***
*CC    8.98484E-11  -9.82947E-12  -1.14088E-12
*CC   -9.83095E-12   9.27593E-11  -9.83127E-12
*CC   -1.14119E-12  -9.82950E-12   8.98479E-11
***
*** Inductance matrix [H/m]
***
*LL    4.22431E-07   8.89272E-08   3.79050E-08
*LL    8.89272E-08   4.12563E-07   8.89271E-08
*LL    3.79050E-08   8.89271E-08   4.22431E-07
***
*** Conductor characteristic impedance [Ohms]
*** All other conductors floating
*** Conductor Impedance Time delay [s/m]
*ZG 1  6.899003e+01 6.123073e-09
*ZG 2  6.748814e+01 6.113117e-09
*ZG 3  6.899023e+01 6.123054e-09
***
*** All other conductors grounded
*** Conductor Impedance Time delay [s/m]
*ZF 1  6.692210e+01 6.012846e-09
*ZF 2  6.385352e+01 5.923011e-09
*ZF 3  6.692228e+01 6.012829e-09
***
*** All other conductors ignored
*** Conductor Impedance Time delay [s/m]
*ZI 1  7.318165e+01 5.772362e-09
*ZI 2  7.512596e+01 5.491615e-09
*ZI 3  7.318195e+01 5.772337e-09
***
```

TRANSMISSION–LINE PARAMETERS
OF SIMULATED MICROSTRIP LINES


```
*** Conductor equivalent resistance [Ohm/m]
***
*RF  1   3.66389E+00
*RF  2   3.61269E+00
*RF  3   3.66400E+00
***
*** Mode Velocity [m/s]:
***
*VV 1 1.519724E+08
*VV 2 1.690605E+08
*VV 3 1.759289E+08
***
*** Potential mode shapes [V]
***
*MV    5.11407E+00  -5.70117E+00   3.19648E+00
*MV    5.78413E+00   1.31508E-04  -5.81821E+00
*MV    5.11390E+00   5.70130E+00   3.19655E+00
***
*** Current mode shapes [A]
***
*MI    6.03022E-02  -8.76998E-02   5.99470E-02
*MI    6.62582E-02   1.67258E-06  -1.06004E-01
*MI    6.02992E-02   8.77008E-02   5.99480E-02
***
*** Mode Equivalent resistance [Ohm/m]
***
*RM  1   9.88474E+00
*RM  2   4.92769E+06
*RM  3   4.83900E+01
***
*** Admittance matrix [S]
***
*YY    1.49212E-02  -2.35925E-03  -4.61463E-04
*YY   -2.35925E-03   1.56270E-02  -2.35926E-03
*YY   -4.61463E-04  -2.35926E-03   1.49212E-02
***
*** Impedance matrix [Ohms]
***
*ZZ    6.88745E+01   1.09819E+01   3.86646E+00
*ZZ    1.09819E+01   6.73078E+01   1.09820E+01
*ZZ    3.86646E+00   1.09820E+01   6.88747E+01
```



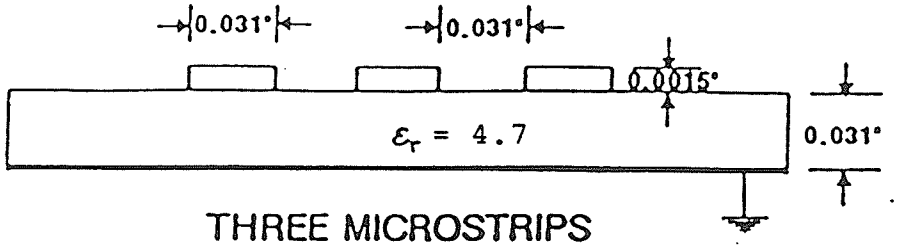


Figure 7.2: Cross–section of simulated and measured PCB.

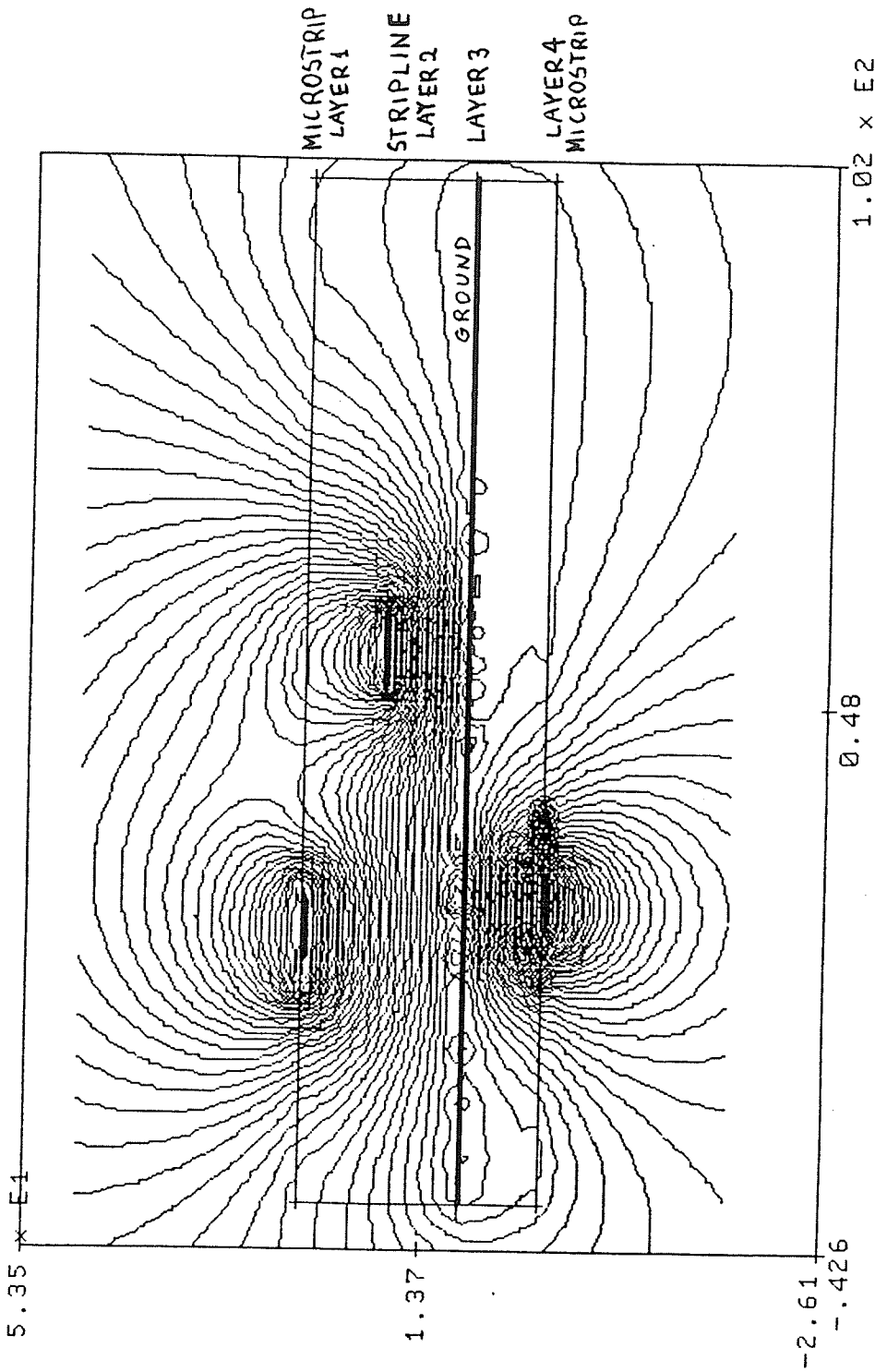


Figure 7.3: Field distribution of four–layer PCB.

7.2 Phyllis circuit simulator

The circuit simulator part of Greenfield, called Phyllis, uses hybrid analysis as the internal method for time–domain circuit simulation. Phyllis operates on a subcircuit–based algorithm. That is, each circuit is built up as a collection of smaller subcircuits. Each unique subcircuit block is reduced to its basic constraining equations one at a time. The only limitation to the number of basic components for any circuit is the amount of time necessary for an analysis to complete.

The user can create circuit by using Circuit Modeller and can use the results of Greenfield2d to describe the transmission lines. The schematic created by Circuit Modeller and the cross–section of analysed PCB is shown in Fig. 7.2. Next, the time–domain analysis can be performed using Phyllis or Spice. At present Phyllis can perform only linear time–domain analysis with such components as: resistors, conductances, capacitors, inductors, independent voltage and current sources, controlled voltage and current sources, and coupled transmission lines [PoWe86].

Spice has capabilities to handle nonlinear components but it is not efficient for circuits with many transmission lines because of the very long time required to find the solution. Phyllis is much faster and it is particularly fast for transmission lines but has no nonlinear analysis.

In this chapter, simulation of printed circuit boards with simulators was described. Field solver and analog simulators were presented. Results of simulation and computations of transmission line parameters were shown.

CHAPTER VIII

RESULTS OF MEASUREMENTS AND SIMULATIONS

In this chapter, results of measurements and simulations are presented, compared and discussed. Measurement results are used for verification of simulations. Directions for future work are suggested.

The board was made by Ponan and Rebizant, [PoRe86]. This two–layer board has one layer of copper foil which is used as ground–plane. On the other layer there are several uncoated microstrip lines. These traces are long enough to be transmission lines for the signals used. The top view of the measured and simulated PCB is shown in Fig. 8.1. The following symbols describe the dimensions of the traces: length (l); width (w); conductor thickness (t); dielectric thickness between trace and reference plane (h); spacing between traces (s); and distance between parts of the same trace (d).

One–ounce copper was used which means that the thickness of the copper was 0.0014 in (i.e. t=1.4 mil). The dimensions of the board were: length (L=24 in); width (W=12 in); and thickness of the board (T=0.032 in). The dielectric constant of the laminate was 4.7. SMA connectors soldered directly to the microstrips on the PCB were used. They were modelled as capacitance in parallel with termination resistors. SMA type termination resistors of value 50 Ω were used. There is no equivalent circuit capacitance nor inductance, included in the technical specifications of the SMA resistors.

Although the trace widths and lengths are large, these board traces are, in other respect, practical for measurement purposes. The characteristic impedance of all these traces is about 67 Ω which is very practical value. Most high–speed designs require the characteristic impedance between 50 Ω and 120 Ω. The lower the characteristic impedance, the faster the transmitted signals are (the transition times are sharper). 60 Ω is very often the best choice and this value is recommended for ECL circuits by Blood, [Bloo82].

The propagation delay depends mainly upon the dielectric constant. This board was made from a standard G–10 laminate (h=31 mil) which has the dielectric constant equal to about 4.7. The ratio of the microstrips' width to the dielectric thickness and to the spacing between traces for this board is: w:h:s = 1:1:1. This ratio determines the characteristic impedance and the capacitance and inductance matrices, and therefore crosstalk and ringing. This ratio is quite practical and often used.

If this ratio is not changed, but the absolute dimensions are changed, crosstalk and ringing will be the same. For instance, one can design a board with microstrips' width equal to 12.5 mil, the dielectric thickness equal to 12.5 mil, and the spacing between microstrips equal to 12.5 mil. These values are quite practical and often used. The crosstalk and ringing will be the same as presented in this work.

The lengths of the traces on this board are quite long because they are used for accurate measurements of the time delays with the oscilloscope setup which has a limited bandwidth (300 MHz). The rise and fall times, for this setup, are between 2 ns and 3.5 ns. The signal is a pulse with amplitude of TTL–levels. These kinds of signals are very often encountered in practical high–speed boards with ECL or high–speed TTL circuits. Even the length of the measured traces is realistic because some traces in practical boards may be very long and going parallel, for instance in back–planes.

The time delay is proportional to the length of the trace so the time delay of trace two times shorter will be two times shorter. There is a practical rule that the trace behaves as transmission line when its time delay is greater than a half of the signal's rise or fall fall time. In this case, the reflection comes after the end of the transition time and may bounce in the line causing reflections. Crosstalk is always present — it is important to predict its amplitude and control it.

The TDR setup signal has very sharp rise which is less than 150 ps. For this signal, any trace longer than 0.013 m is a transmission line (a long line). TDR setup enables to test almost any trace in any practical board.

By using these two setups, we measure crosstalk, reflections and ringing for two representative kinds of signals — the first one corresponds to ECL or TTL circuits, and the other one corresponds to GaAs circuits. That covers the whole spectrum of high–speed circuits. The simulations of both setups are performed. The results of this chapter serve to **validate the simulations.**

The traces were numbered (Fig. 8.1) and each one was designed for a specific purpose. Trace 1 (l=60.5 cm; w=31 mil) was used for measurement of time delay, characteristic impedance, reflections and ringing. There were three microstrips numbered as 2a, 2b, and 2c (l=60.5 cm; w=31 mil; and s=31 mil) — they were used primarily for measurement of crosstalk, but also were used for measurement of reflections and ringing.

Trace 3 (l=121 cm; w=31 mil; d=0.7 cm) was designed for measurement of corners (90 degree angle) and time delay. Trace 4 (l=63.6 cm; w=31 mil; d=0.7 cm) was designed for measurement of corners (90 degree angle). Trace 5 (l=62.8 cm; w=31 mil; d=0.7 cm) was designed for measurement of corners (45 degree angle). Traces 6a, 6b, and 6c (l=65.3 cm; w=31 mil; s=31 mil; d=0.7 cm) were designed primarily for measurement of corners (90 degree angle) and crosstalk. The design of Traces 3, 4, 5, and 6 is incorrect — the spacing between arms of the traces is too small and therefore there is coupling of crosstalk. The forward crosstalk is

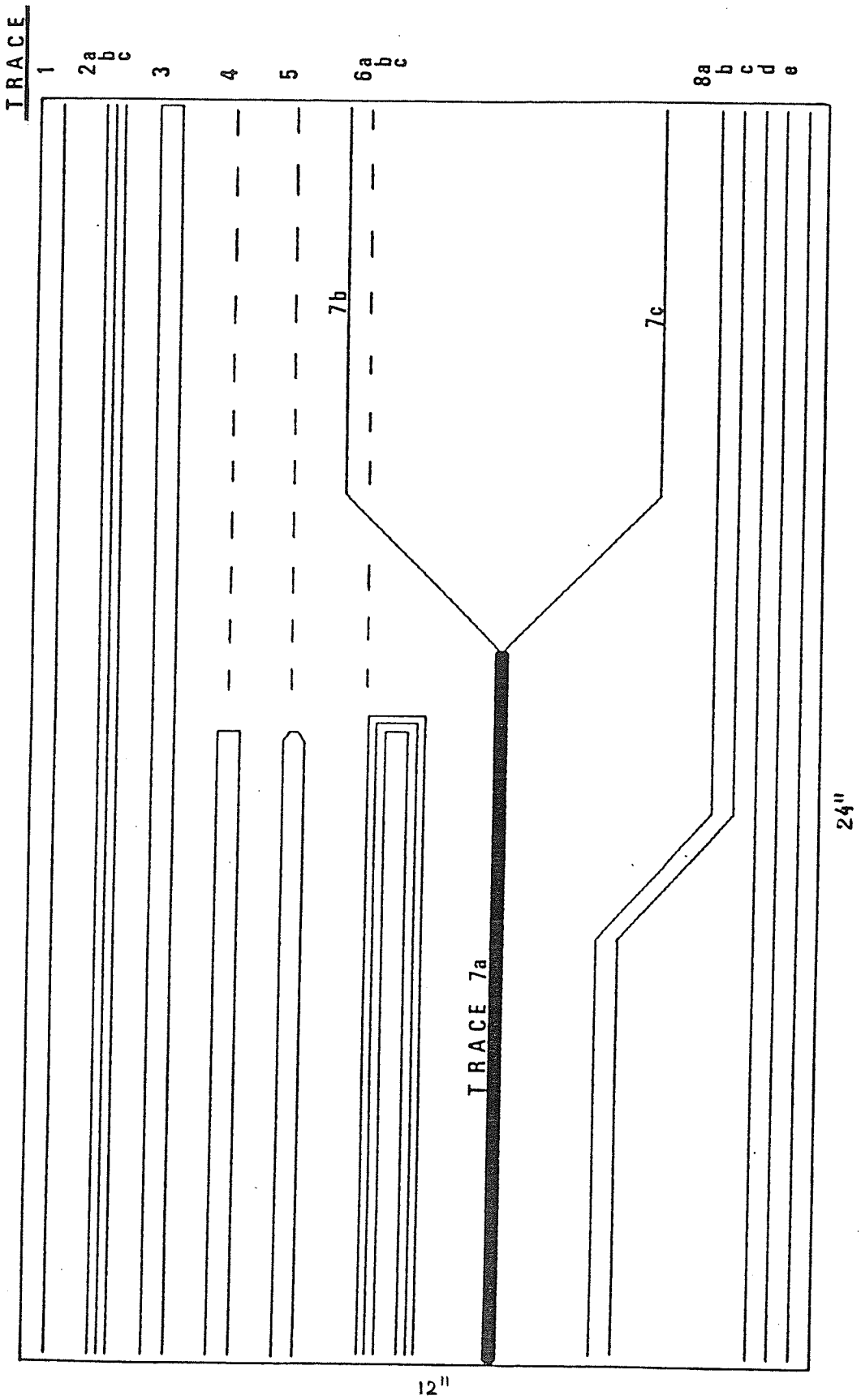


Figure 8.1: Top view of measured and simulated printed circuit board. From: Ponnan et al., [PoRe86].

measured instead of corners. It is very interesting that even with such big spacing the crosstalk is substantial. The influence of corners may be neglected — it is very small even with TDR signal.

Traces 7 and 8 were not used. Each trace could also be used for measurement of time delay, characteristic impedance, reflections and ringing.

The simulations with Greenfield2d (a field solver) and creating equivalent models of interconnections are described in Chapter VII. This board was simulated and transmission line parameters were computed using Greenfield (see results for Traces 2 included in Chapter VII). These simulations give a lot of information and are very accurate.

The input signal used for oscilloscope measurements is shown in Fig. 8.2. The output signal from Trace 2b (Fig. 8.2) and Trace 1 are exactly the same — they are delayed by 3.6 ns in comparison with the input signal (it is measured between cursors), thus the time delay of these two measured microstrips can be taken as 3.6 ns. That gives the propagation delay equal to 5.9504 ns/m.

The measured characteristic impedance of the microstrip lines is 67 Ω and there is a mismatch between the signal source (50 Ω), or coaxial cables (50 Ω) and microstrip lines which can be seen from included graphs. There is a small undershoot present in the output signals (Fig. 8.2) caused by this impedance mismatch between microstrip (67 Ω) and coaxial cable (50 Ω) but it is obscured by relatively large rise and fall time.

As a result of simulation of the middle microstrip line — Trace 2b, we get the propagation delay equal to 6.1131 ns/m for all other conductors floating, and equal to 5.9230 ns/m for all other conductors grounded. It may be concluded that the measured propagation delay should be between 5.9230 ns/m and 6.1131 ns/m, and it is equal to 5.9504 ns/m, therefore we can see that the results of simulation are very accurate.

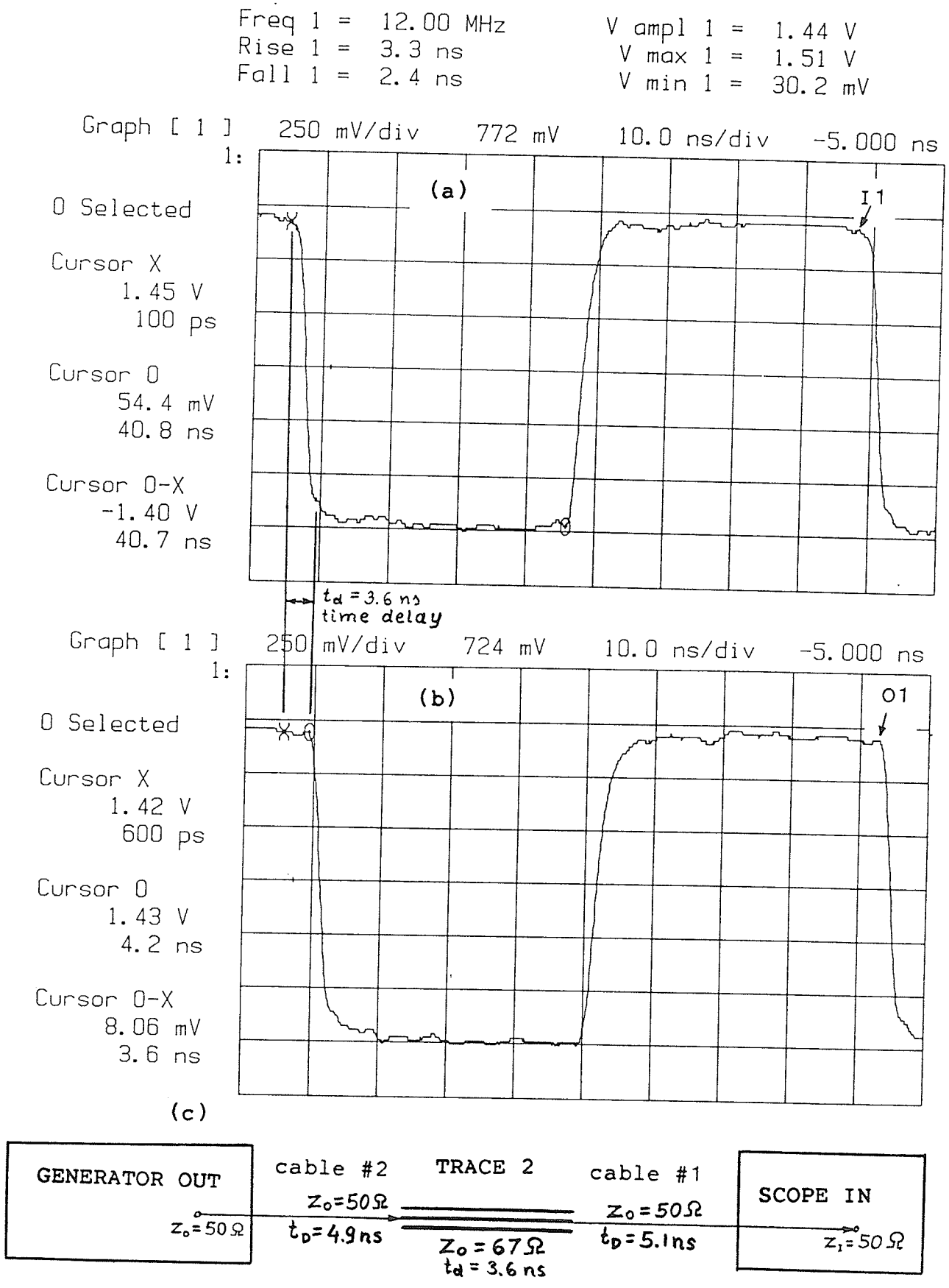


Figure 8.2: Input and output signal used for oscilloscope setup measurements. (a) input signal; (b) output signal; and (c) measurement setup.

The time delays may be easily read from the plots included in this chapter and also in appendices. Both measurements and simulations give similar results. The signals in the line transmitting signal, with reflections added to the signals, are displayed and plotted. The crosstalk signals were both measured and simulated and their shapes are displayed, and plotted. They are included in this chapter or in appendices.

The most useful information may be obtained from Traces 2. The three microstrip lines are spaced close to each other (s=31 mil) so there is substantial crosstalk. Simulations of Traces 2 may be compared with measurements in the next sections. The results of these sections serve to validate the simulations.

8.1 Discussion of results for oscilloscope setup

The results of this section serve to validate simulations for frequencies of several hundred MHz. The input signal (Fig. 8.2) used for measurements was produced by a waveform generator (model Wavetek 178). It was measured by the digitizing oscilloscope (model HP 54201D) and plotted on HP colour plotter (the measurement setup is described in Chapter VI, Fig. 6.1).

Coaxial cables of type RG–58A/U were used, which have the characteristic impedance equal to 50 Ω. These cables were terminated with SMA connectors on one end, and BNC connectors on the other end. The cable SMA connectors were compatible with the SMA connectors soldered onto the PCB traces. Both could be conveniently screwed together. The SMA termination loads could also be screwed into SMA connectors on the PCB. The cable BNC connectors could be screwed to the generator or oscilloscope. Three coaxial cables were used, numbered as 1, 2 and 3 with the lengths 0.933 m, 0.892 m, and 0.981 m, respectively. Their time delays were equal to 5.1 ns, 4.9 ns and 5.4 ns, respectively. The coaxial cable propagation delay was equal to 5.5 ns/m.

The characteristic impedance of the coaxial cables was perfectly matched to the output impedance of the generator and input impedance of the oscilloscope and

there was no reflections at these points. The only effect of the cables was due to their time delays because the cables behaved as transmission lines. This time delay effect was eliminated from the presented graphs. It was achieved by storing corresponding graphs with proper timing in the oscilloscope's memory and then recalling them for comparison and plotting. The result was the same as if the generator was driving the trace directly (without the cable) and the scope was directly connected (without the cable) to the other end of the trace.

For instance, the input signal in Fig. 8.2.a was first measured from the generator output through cable 2 and cable 1 in series to the scope input, and the graph was stored in the memory. Next, the output signal in Fig. 8.2.b was measured from the generator through cable 2 and Trace 2b, and cable 1 in series to the scope input, and the graph was stored. Finally, these two graphs were recalled from the momory to the screen and then plotted together, so the accurate timing was preserved and accurate time delay introduced by Trace 2b was measured and showed in Fig. 8.2. This is a very accurate method of measuring because it eliminates the errors introduced by cables, trigger system and differences between scope channels.

The time delay of Trace 2b is measured between two cursors (Fig. 8.2), which are called x and o, and it is equal to 3.6 ns. It is very easy to read the rise time and fall time from this graph. The graph is not smooth because the signal was measured in a normal mode (not average mode) and some digitizing noise was present.

The input signal from the generator (voltage source) was a pulse signal of frequency equal to 12 MHz (or sometimes different) with the rise time equal to 3.1 ns and fall time equal to 2.2 ns. These are the shortest edge times available from that generator. The voltage delivered by the source to 50 Ω load was 1.4 V for HIGH level and about -45 mV for LOW level. The source was modelled by this

Spice subcircuit and used by Phyllis for simulations:

```
.SUBCKT SO_GEN                1
*
* ------- independent voltage sources
VSO_GEN  1   0  PULSE(-90MV 2.8V 1.0NS 3.1NS 2.2NS 42.0NS 86.0NS)
*
.ENDS SO_GEN
```

Different terminations were used which caused different reflections. It is interesting that the lack of proper terminations caused very big reflections which were bouncing in the line and were producing oscillations with the frequency determined by the length of the line. These oscillations may be very harmful and should be expected particularly in the proximity of lines transmitting repetitive signals with sharp rise or fall times (clock lines) (Fig. A.9 in Appendix A and Fig. B.6 in Appendix B).

8.1.1 Verification of simulations for all Traces 2 terminated with 50 Ω

Let us consider results for the setup with all ends of Traces 3a, 3b, and 3c terminated with 50 Ω. Because the characteristic impedance of each trace is equal to 67 Ω and all terminations (including the coaxial cables) are 50 Ω, there is impedance mismatch and reflections. Reflections cause ringing which can be seen for instance in Fig. 8.5.

The measurements and simulations are compared and discussed with respect to the amplitude, time scale, and general wave shape. Let us describe each designated point by a letter and a number, for instance point B1 will be a corresponding point on the backward crosstalk graph obtained from both simulation and measurement. Point F1 will be a corresponding point on the forward crosstalk graph obtained from both simulation and measurement. Point I1 will be a corresponding point on the input signal graph obtained from both simulation and measurement.

Point O1 will be a corresponding point on the output signal graph obtained from both simulation and measurement.

Each point will be described by two coordinates that is time and amplitude. Let us consider the measured backward crosstalk shown in Fig. 8.3.a. For instance: B1=(41 ns , -7.65 mV) means that at point B5 the time is equal to 41 ns and amplitude is equal to -7.65 mV. And so, point B7 may be described as: B3=(48.5 ns , 75.7 mV). The distance between two points will be described as B3–B1, and for instance it will be equal to: B3–B1=(7.5 ns , 83.4 mV) , which means that the time between these two points is equal to 7.5 ns and the difference in amplitude is equal to 83.4 mV.

The absolute difference will be always calculated in this work as the simulation result value minus the measured result value. The relative difference in % will be always calculated as the simulation result value minus the measured result value and devided by the simulation result value, and multiplied by 100 %.

The simulated amplitude of the input signal at point I1 and output signal at point O1 (Fig. 8.5.a) is equal to 1.4 V, and the measured amplitude is also equal to 1.4 V (Fig. 8.2). The accuracy of the simulation may be checked very accurately by comparing the simulated and measured crosstalk which has rather small amplitude and therefore the difference will be more distinct and the error more probable.

Backward crosstalk starts simultaneously with the input signal which is shown in Fig. 8.3. The measured backward crosstalk is shown in detail in Fig. 8.3 which can be compared with the simulated backward crosstalk in Fig. 8.5.

The signals are periodical and it is enough to show one period, and therefore only one period was plotted. Let us compare measured and simulated backward crosstalk that is Fig. 8.3.a and Fig. 8.5.d. The plotted signals are shifted in time and the first or third impulse in Fig. 8.3.a corresponds to the second impulse in Fig. 8.5.d , and it is caused by the fall time of the input signal. Please notice the appropriate numbering. Let us compare a few points.

1. Measured backward crosstalk (Fig. 8.3.a). The difference between:

   points B3 and B1 : B3–B1=(7.5 ns , 83.4 mV);

   points B7 and B5 : B7–B5=(7.5 ns , 82 mV).

2. Simulated backward crosstalk (Fig. 8.5.d). The difference between:

   points B3 and B1 : B3–B1=(7 ns , 117 mV);

   points B7 and B5 : B7–B5=(7 ns , 110 mV).

3. Simulated backward crosstalk (Fig. 8.6.b). The difference between:

   points B3 and B1 : B3–B1=(7 ns , 114 mV);

   points B7 and B5 : B7–B5=(7 ns , 108 mV).

The amplitude difference between measured and simulated backward crosstalk (between 1. and 3.) is equal to 30.4 mV that is 26.8 % for points B3–B1, and is equal to 26 mV that is 24 % for points B7–B5.

The time difference between measured and simulated backward crosstalk is equal to -0.5 ns that is -7.1 % for points B3–B1 and also for B7–B5.

The terminations were modelled by resistance equal to 50 Ω (Fig. 8.5), or by resistance equal to 50 Ω and capacitance equal to 1 pF in parallel (Fig. 8.6), or by resistance equal to 50 Ω and capacitance equal to 10 pF in parallel (Fig. 8.7). By comparing these figures one may conclude that the closest (to measurements) simulation results were obtained by modelling terminations with resistance equal to 50 Ω and capacitance equal to 1 pF. The equivalent capacitance of the connectors and terminations together should be between 1 pF and 10 pF depending on their type.

The forward crosstalk is always delayed by the time delay of the transmission line which is shown in Fig. 8.4 — the time delay is measured by the two cursors and is equal to 3.6 ns. The forward crosstalk becomes bigger with the increase of the length of the transmission line, and because considered microstrips were quite long, the forward crosstalk is rather big.

The signals are periodical and it is enough to show one period, and therefore only one period was plotted. Let us compare measured and simulated forward crosstalk that is Fig. 8.4.a and Fig. 8.5.e. The plotted signals are shifted in time and the first or third impulse in Fig. 8.4.a corresponds to the second impulse in Fig. 8.5.e , and it is caused by the fall time of the input signal. Please notice the appropriate numbering. Let us compare a few points.

1. Measured forward crosstalk (Fig. 8.4.a). The difference between:

   points F2 and F1 : F2–F1=(2.5 ns , 78 mV);

   points F6 and F5 : F6–F5=(2.5 ns , 92 mV).

2. Simulated forward crosstalk (Fig. 8.5.e). The difference between:

   points F2 and F1 : F2–F1=(2.37 ns , 111 mV);

   points F6 and F5 : F6–F5=(2.37 ns , 143 mV).

3. Simulated forward crosstalk (Fig. 8.6.b). The difference between:

   points F2 and F1 : F2–F1=(2.37 ns , 111 mV);

   points F6 and F5 : F6–F5=(2.37 ns , 141 mV).

The amplitude difference between measured and simulated forward crosstalk (between 1. and 3.) is equal to 33 mV that is 29.7 % for points F2–F1, and 49 mV that is equal to 34.8 % for points F6–F5.

The time difference between measured and simulated forward crosstalk is equal to -0.13 ns that is -5.5 % for points F2–F1 and also for F6–F5.

Extensive simulations were performed for this setup. The simulation results are very similar to those obtained from measurements. The time delays, amplitudes and shapes of signals are correct. The time simulation results are smaller than measured and they are accurate to about -7 %. However, the simulated amplitude of crosstalk is bigger than measured by about 30 % because the sharp impulses of crosstalk were partially attenuated by the measurement system due to a limited bandwidth.

The results (for all traces terminated with 50 Ω) are included in Fig. 8.5 to Fig. 8.7. They may be compared with the measured results included in Fig. 8.2 to Fig. 8.4.

Practically, it was only possible to measure the steady state results for the digitizing scope used had the bandwidth of 300 MHz for repetitive signals and of 50 MHz for one–shot measurements. It is important to notice that Phyllis or Spice should be run for at least several cycles of the source to produce the steady state results which then can be compared with the measured steady state results (see Fig. B.3, Fig. B.4 and Fig. B.5 in Appendix B).

The simulation of the creation of steady state signals is shown in Fig. B.3 in Appendix B. Trace 2a and Trace 2b were terminated with 50 Ω, and Trace 2c was grounded. The input signal was applied to one end of Trace 2a and the output signal was measured from the other end, and the forward and backward crosstalk were measured from Trace 2b. Ten cycles of these signals plotted together are shown in Fig. B.3.a. First, fifth and ninth period of the forward and backward crosstalk are shown in Fig. B.3.b , Fig. B.3.c and Fig. B.3.d , respectively. The difference between the first and fifth cycle shapes are quite significant but they are very small between fifth and ninth cycle shapes. One may conclude that the steady state was reached after several cycles.

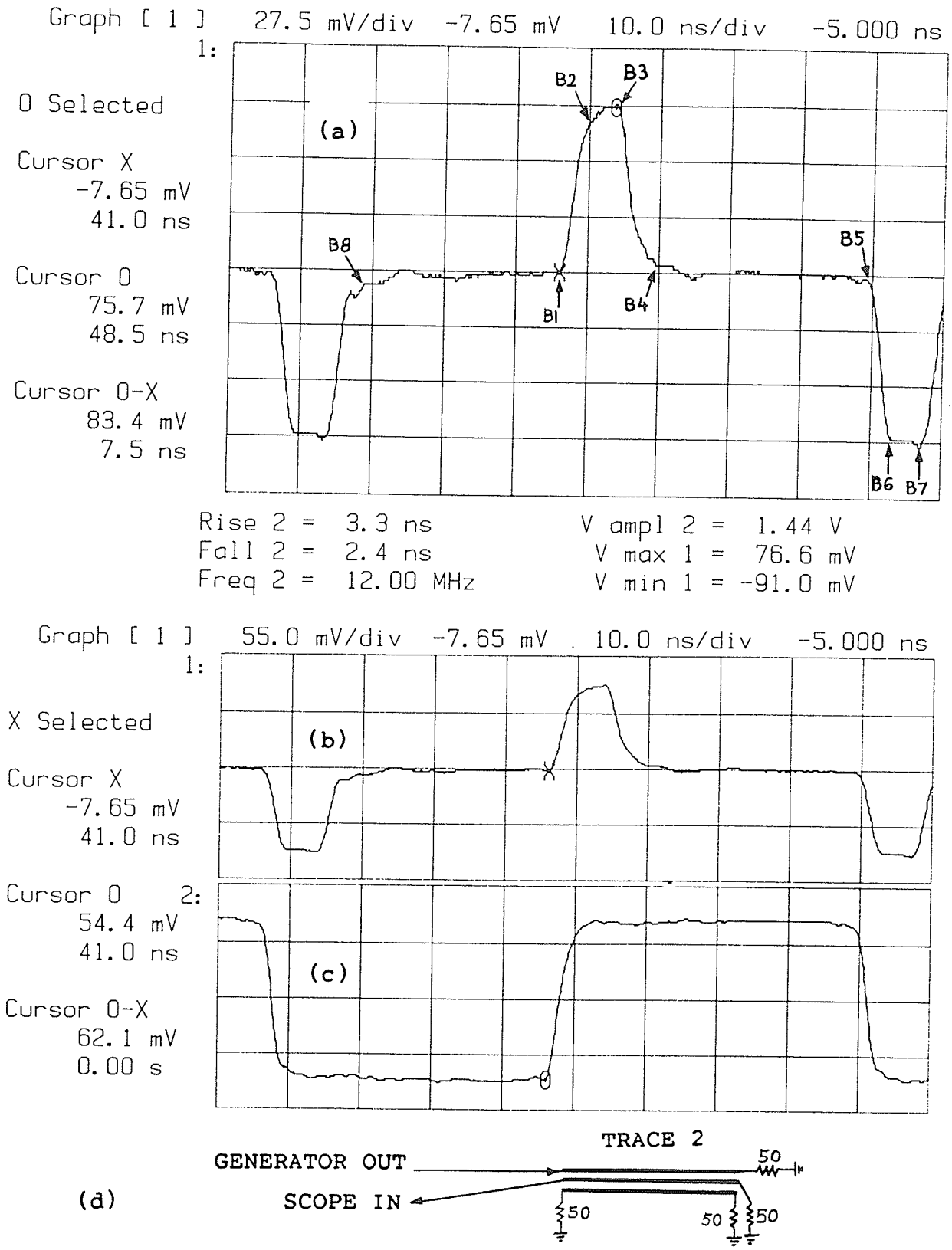


Figure 8.3: Backward crosstalk and input signal for scope setup. All traces terminated with 50 Ω: (a) backward crosstalk from Trace 2b in detail; (b) backward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.

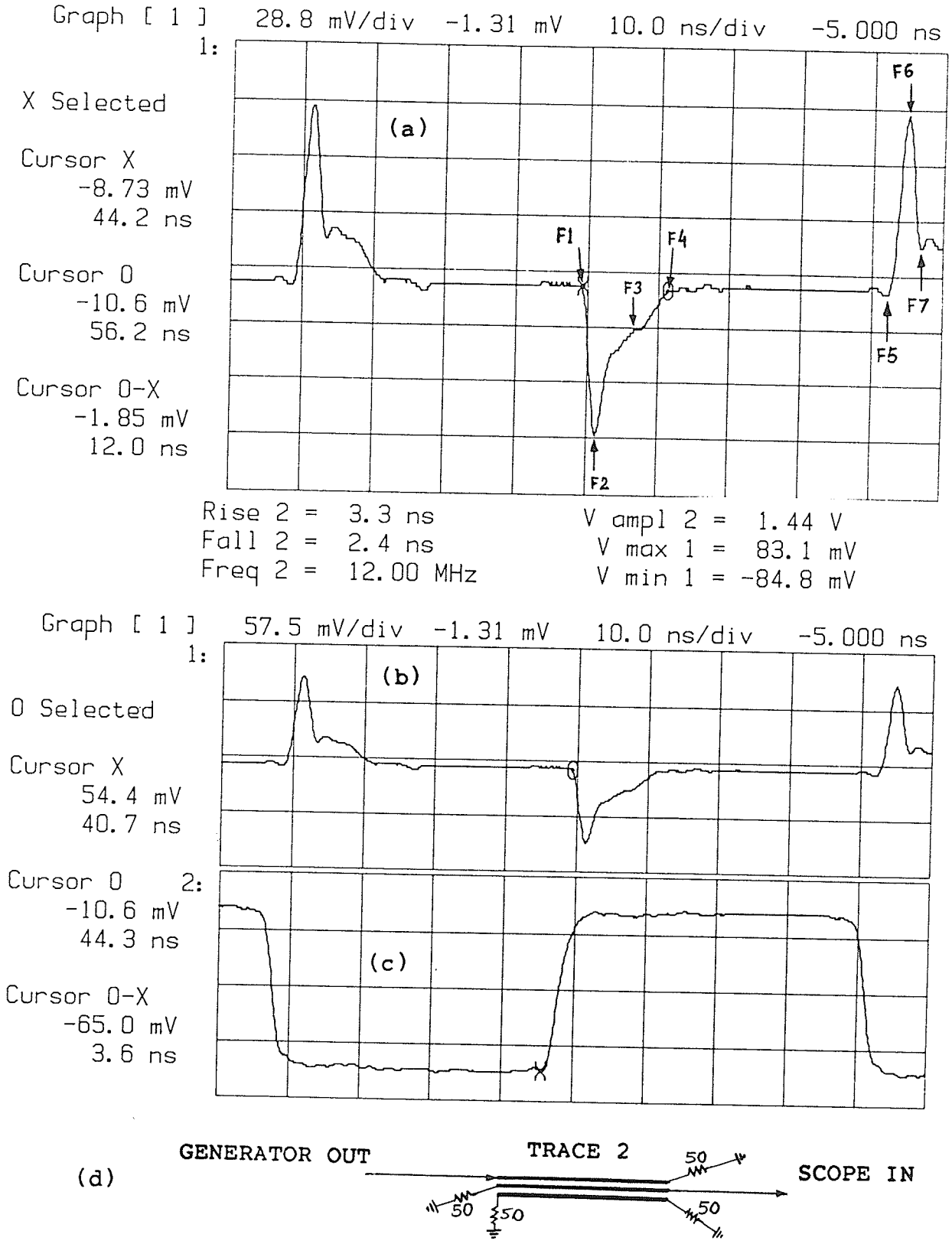


Figure 8.4: Forward crosstalk and input signal for scope setup. All traces terminated with 50 Ω: (a) forward crosstalk from Trace 2b in detail; (b) forward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.

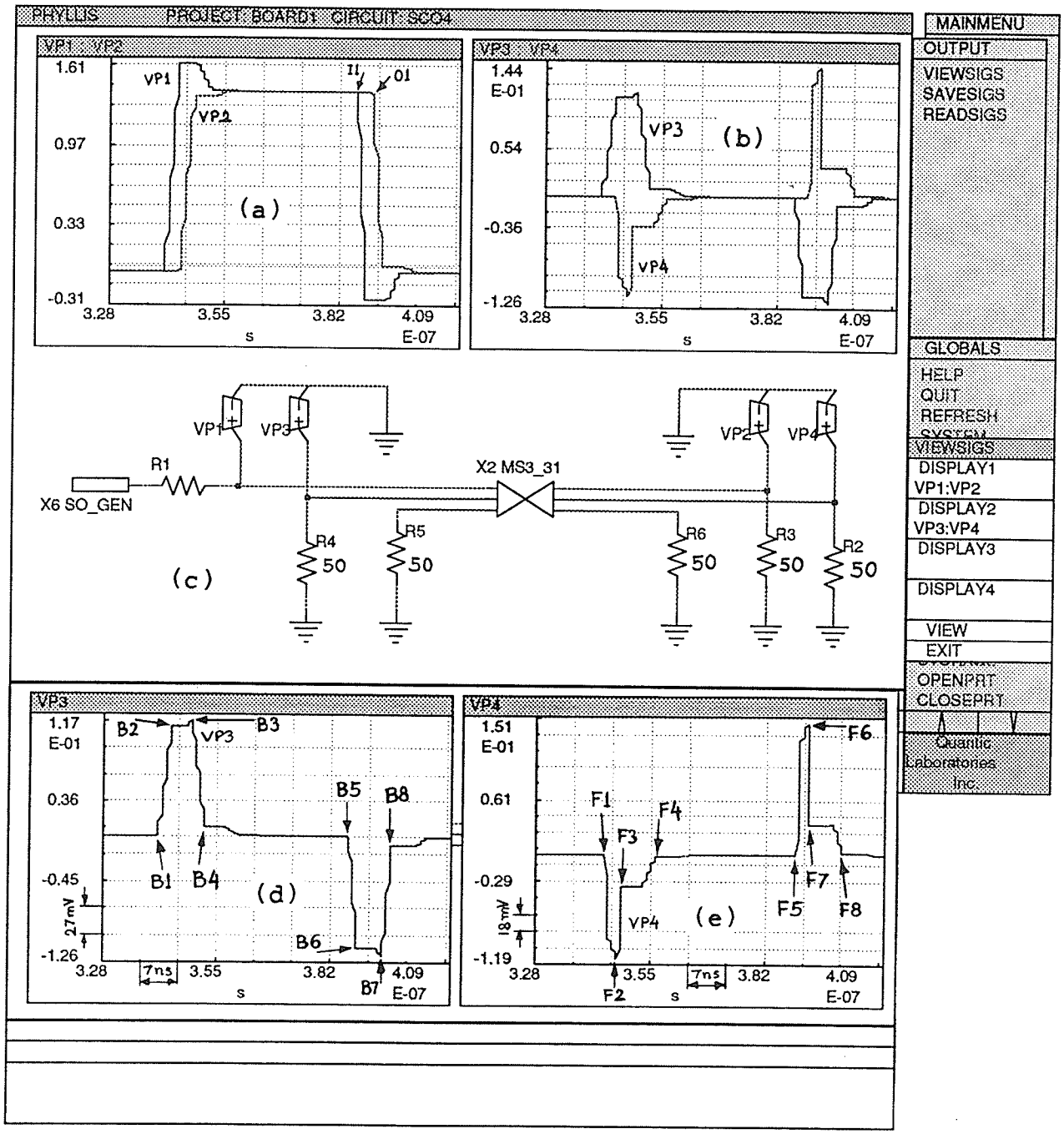


Figure 8.5: Results of simulation of scope setup for three parallel microstrips. For all three traces terminated with 50 Ω: (a) input signal (VP1) and delayed output signal (VP2) in the Trace 2a, both with reflections; (b) backward (VP3) and delayed forward (VP4) crosstalks in the Trace 2b; (c) schematic; (d) backward crosstalk (VP3); and (e) forward crosstalk (VP4).

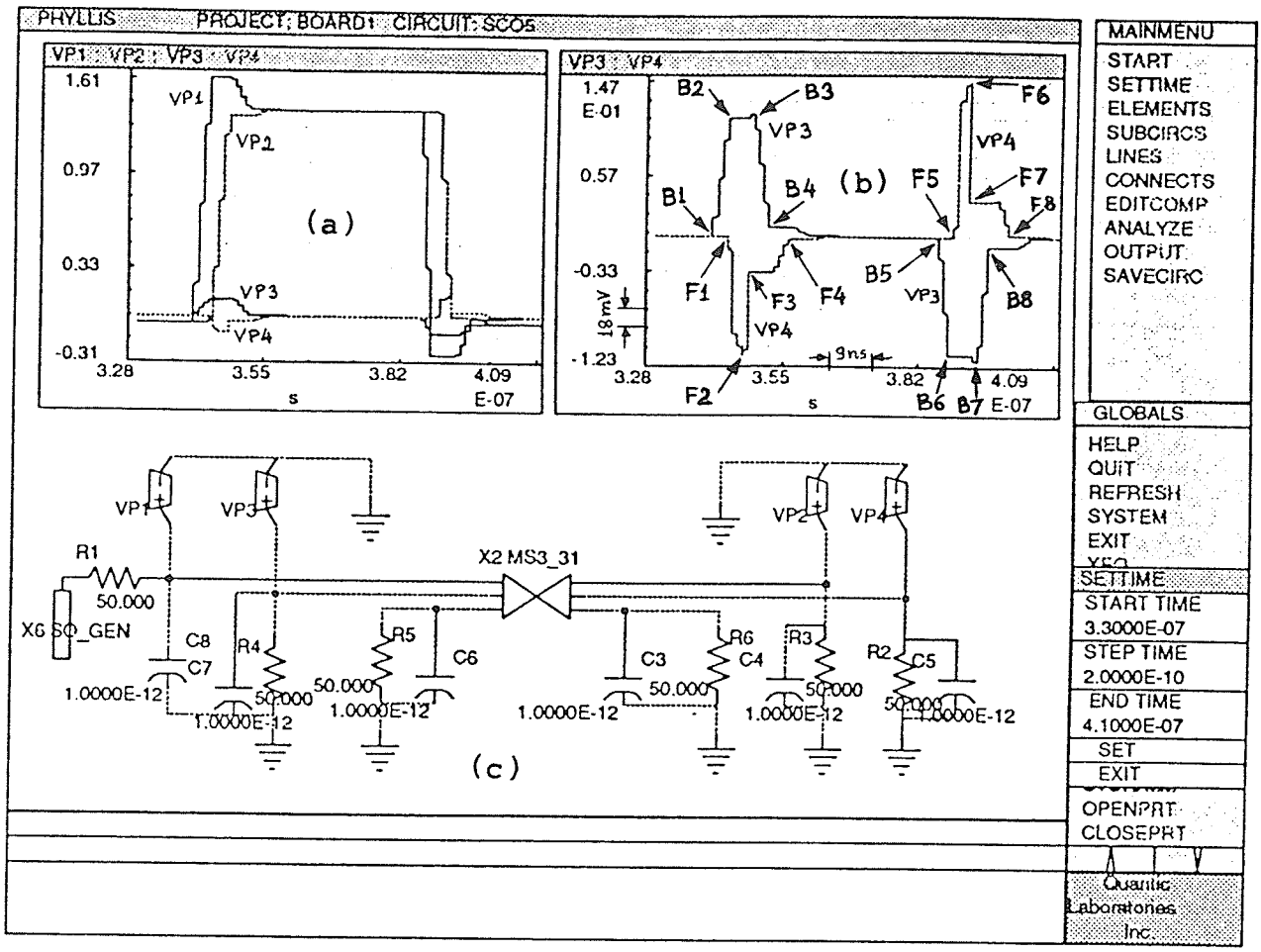


Figure 8.6: Results of resistive and capacitive modelling of terminations. The terminations are modelled by resistor 50 Ω and capacitor **1 pF** in parallel: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a (both with reflections), plotted together with backward and forward crosstalks (VP3 and VP4) in Trace 2b; (b) backward (VP3) and delayed forward (VP4) crosstalks in Trace 2b; and (c) schematic.

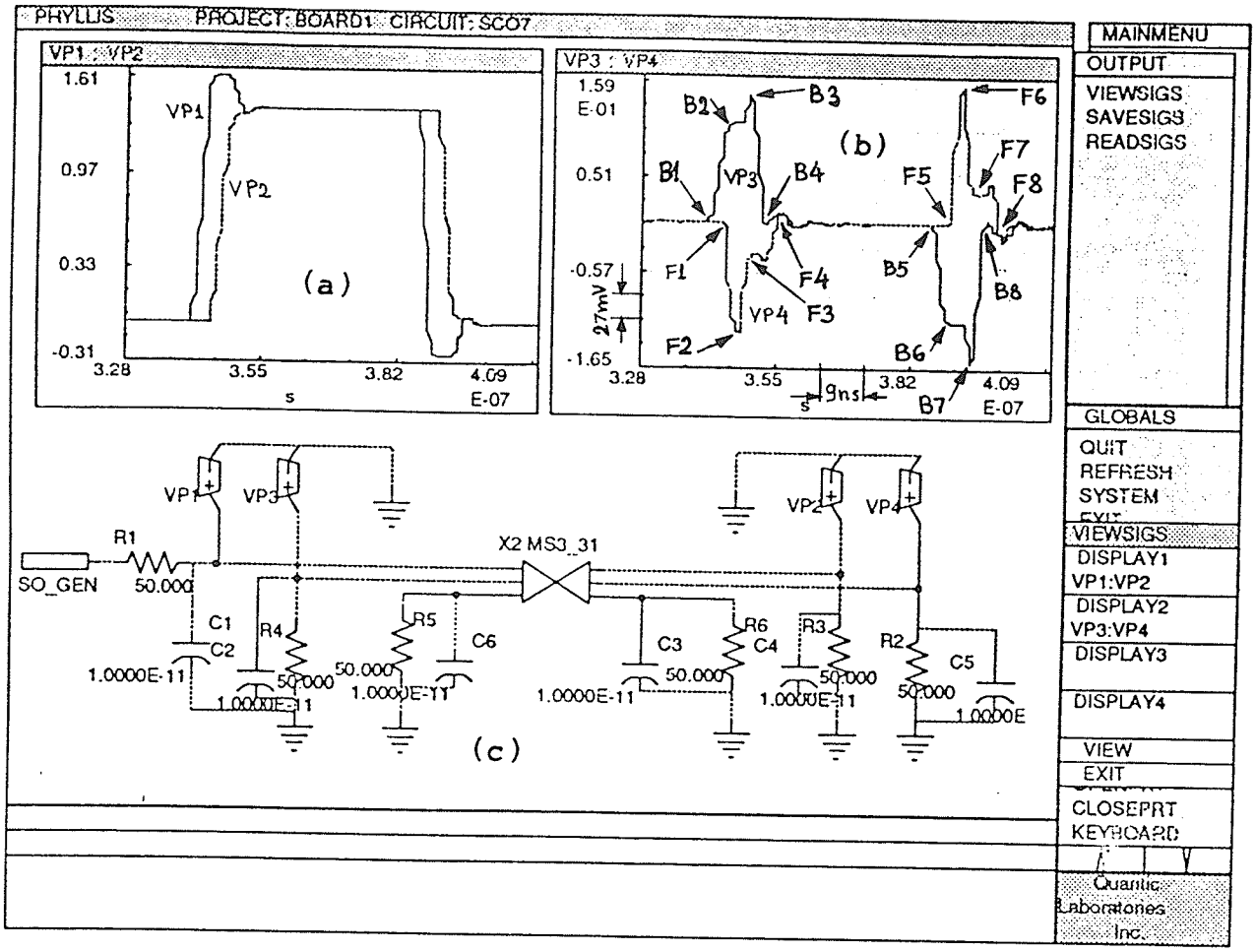


Figure 8.7: Results of resistive and capacitive modelling of terminations. The terminations are modelled by resistor 50 Ω and capacitor **10 pF** in parallel: (a) input signal (VP1) and output signal (VP2) in first trace Trace 2a (both with reflections), and backward and forward crosstalks (VP3 and VP4) in Trace 2b; (b) backward (VP3) and delayed forward (VP4) crosstalks in second trace; and (c) schematic.

8.1.2 Verification of scope setup simulations for Trace 2c floating

The measurements and simulations are compared and discussed with respect to the amplitude, time scale, and general wave shape. Let us describe each designated point by a letter and a number, for instance point B1 will be a corresponding point on the backward crosstalk graph obtained from both simulation and measurement. Point F1 will be a corresponding point on the forward crosstalk graph obtained from both simulation and measurement.

The results of measurements and simulations, for two traces terminated with 50 Ω and third trace floating, are shown in Fig. 8.8 to Fig. 8.10. The backward crosstalk is plotted together with the input signal (Fig. 8.8) and it is shown that they start at the same time. Details of backward crosstalk are shown in Fig. 8.8.

The signals are periodical and it is enough to show one period, and therefore only one period was plotted. Let us compare measured and simulated backward crosstalk that is Fig. 8.8.a and Fig. 8.10.b. Please notice the appropriate numbering. Let us compare a few points.

1. Measured backward crosstalk (Fig. 8.8.a). The difference between:

   points B3 and B1 : B3–B1=(7.5 ns , 85.5 mV);

   points B7 and B5 : B7–B5=(7.5 ns , 85 mV).

2. Simulated backward crosstalk (Fig. 8.10.b). The difference between:

   points B3 and B1 : B3–B1=(7.8 ns , 138 mV);

   points B7 and B5 : B7–B5=(7.8 ns , 141 mV).

The amplitude difference between measured and simulated backward crosstalk (between 1. and 2.) is equal to 52.5 mV that is 38 % for points B3–B1, and is equal to 56 mV that is 39.7 % for points B7–B5.

The time difference between measured and simulated backward crosstalk is equal to 0.3 ns that is 3.9 % for points B3–B1 and also for B7–B5.

Next, forward crosstalk is plotted together with the input signal (Fig. 8.9) — forward crosstalk is defined at the far end from the source so it is delayed by

the time delay of the microstrip which is measured by using two cursors. Forward crosstalk is shown in detail in Fig. 8.9.

These measurements can be compared with simulation results given in Fig. 8.10. The terminations were modelled by resistance equal to 50 Ω. The input and output signals are plotted together on the first graph to show the time delay between them and the overshoot in the input signal, and undershoot in the output signal caused by impedance mismatch (Fig. 8.10.a). On the second graph, backward and forward crosstalks are plotted together to show their shapes and the time delay between them (Fig. 8.10.b). The schematic is included below these two graphs (Fig. 8.10.c).

Let us compare measured and simulated forward crosstalk that is Fig. 8.9.a and Fig. 8.10.b. Please notice the appropriate numbering. Let us compare a few points.

1. Measured forward crosstalk (Fig. 8.9.a). The difference between:

   points F2 and F1 : F2–F1=(2.5 ns , 80.4 mV);

   points F6 and F5 : F6–F5=(2.5 ns , 93.8 mV).

2. Simulated forward crosstalk (Fig. 8.10.b). The difference between:

   points F2 and F1 : F2–F1=(2.65 ns , 117 mV);

   points F6 and F5 : F6–F5=(2.65 ns , 152 mV).

The amplitude difference between measured and simulated forward crosstalk (between 1. and 2.) is equal to 36.6 mV that is 31.3 % for points F2–F1, and 58.2 mV that is 38.3 % for points F6–F5.

The time difference between measured and simulated forward crosstalk is equal to 0.15 ns that is 5.7 % for points F2–F1 and also for F6–F5.

The simulation results are very similar to those obtained from measurements. The time delays, amplitudes and shapes of signals are correct. The time simulation results are bigger than measured time results and they are accurate to about 6 %. However, the simulated amplitude of crosstalk is bigger than measured by about

40 %. The reason of the amplitude difference is not simple. It could be caused by the fact that the sharp impulses of crosstalk were partially attenuated by the measurement system due to a limited bandwidth.

The simulated numbers depend on the model used to represent the actual measurement setup. It is important that the simulations and measurements give very similar results. It is possible to create more complicated schematic and obtain closer approximation but even the most sophisticated one will have very restricted application. The approach implemented here was to obtain the best results while modelling the merit of the system.

8.2 Discussion of results for TDR setup

The results of this section serve to validate the simulations for frequencies up to the GHz range. The used rise time is less than 150 ps which is equivalent to 2.1 GHz. The TDR technique and source are described in Chapter VI. The source has now much faster rise time. It is driving one of the traces. The transmitted signal, reflections and crosstalk are measured. The TDR signal was modelled by the following Spice subcircuit:

```
.SUBCKT SO_TDR
*
* ------- independent voltage source
VSO_TDR  1   0   PULSE(0.0V 0.5V 1.0NS 0.15NS 0.15NS 2.5MS 5.0MS)
*
.ENDS SO_TDR
```

The reflections and crosstalks were measured. The measured results are included in this section and in **Appendix C** together with the results of simulation to enable an easy and quick comparison. It may be concluded that for such fast signals the transmission line effects and crosstalk become very important and that they can be successfully simulated by Greenfield. The time delays, crosstalk and reflections were measured and simulated with different terminations.

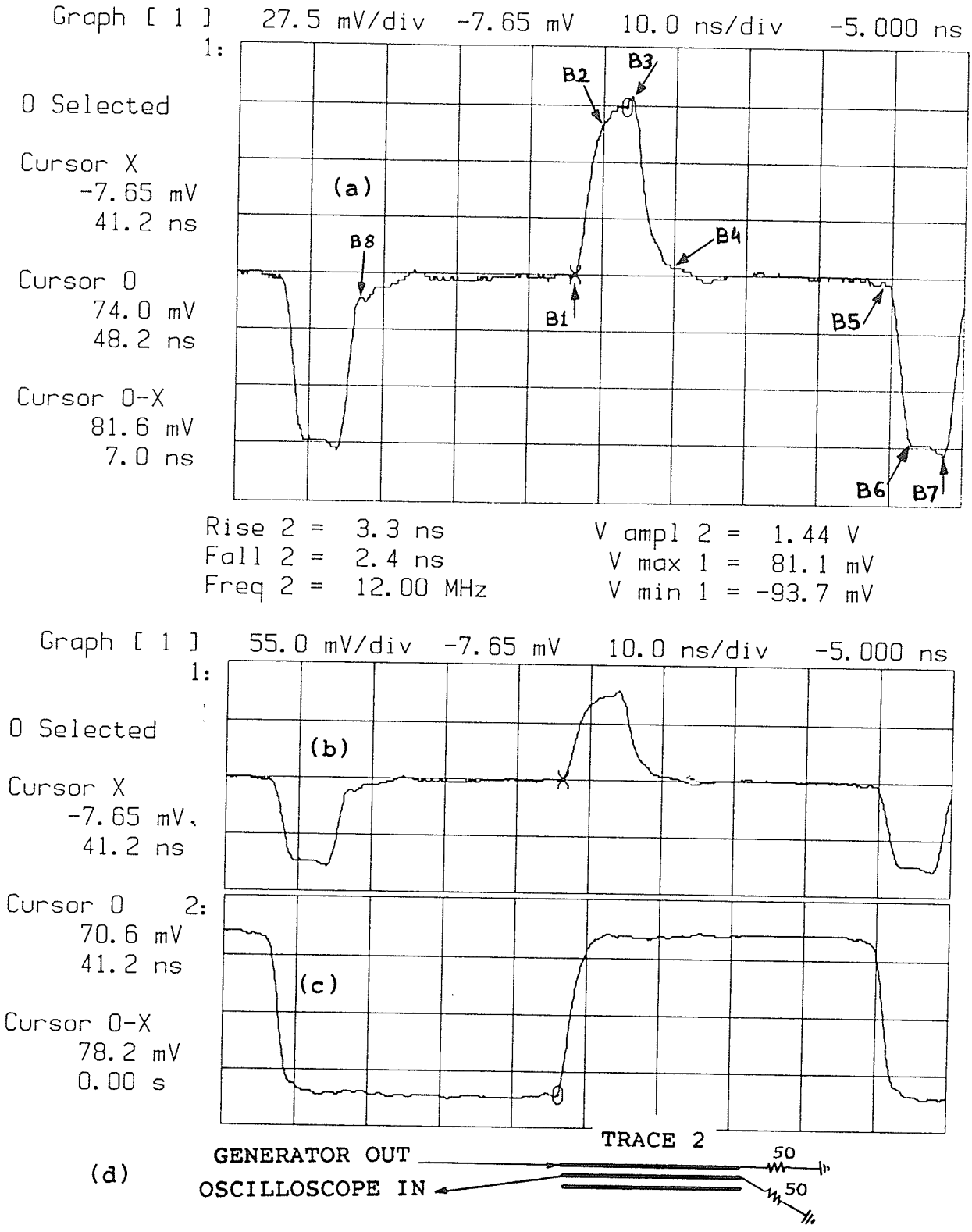
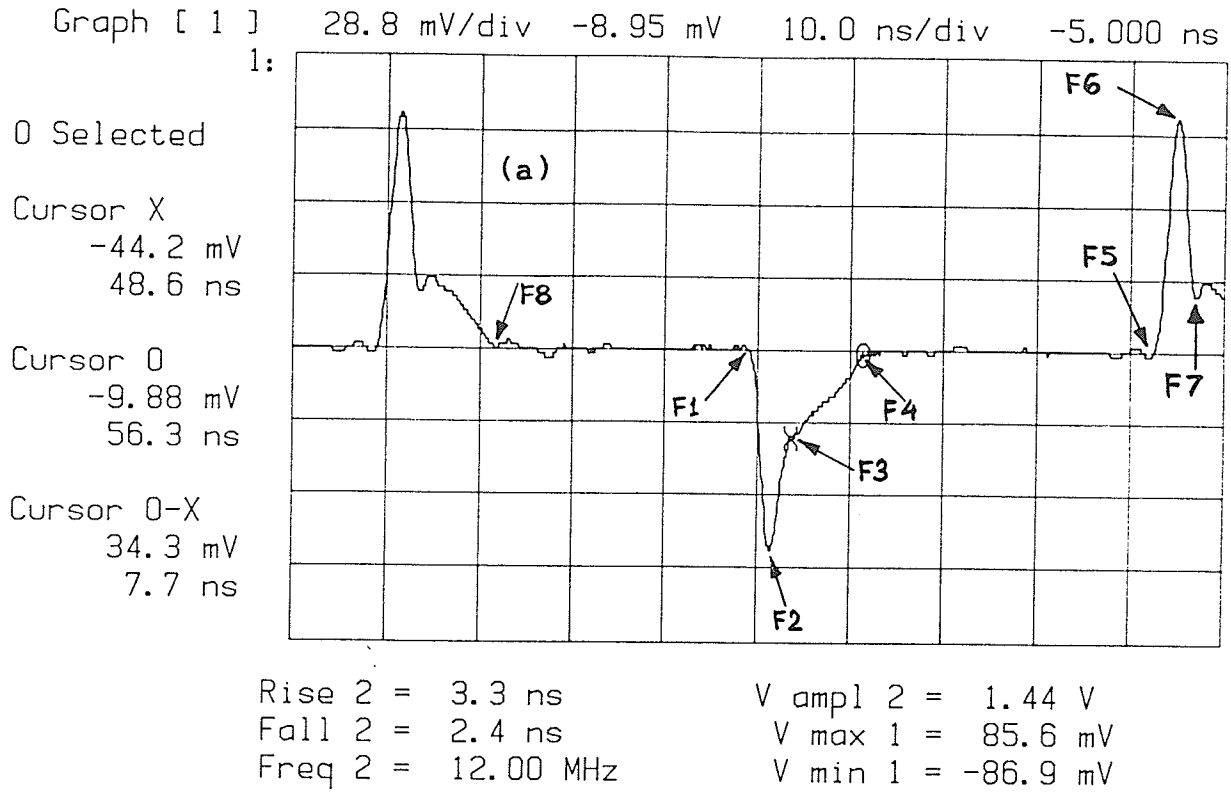
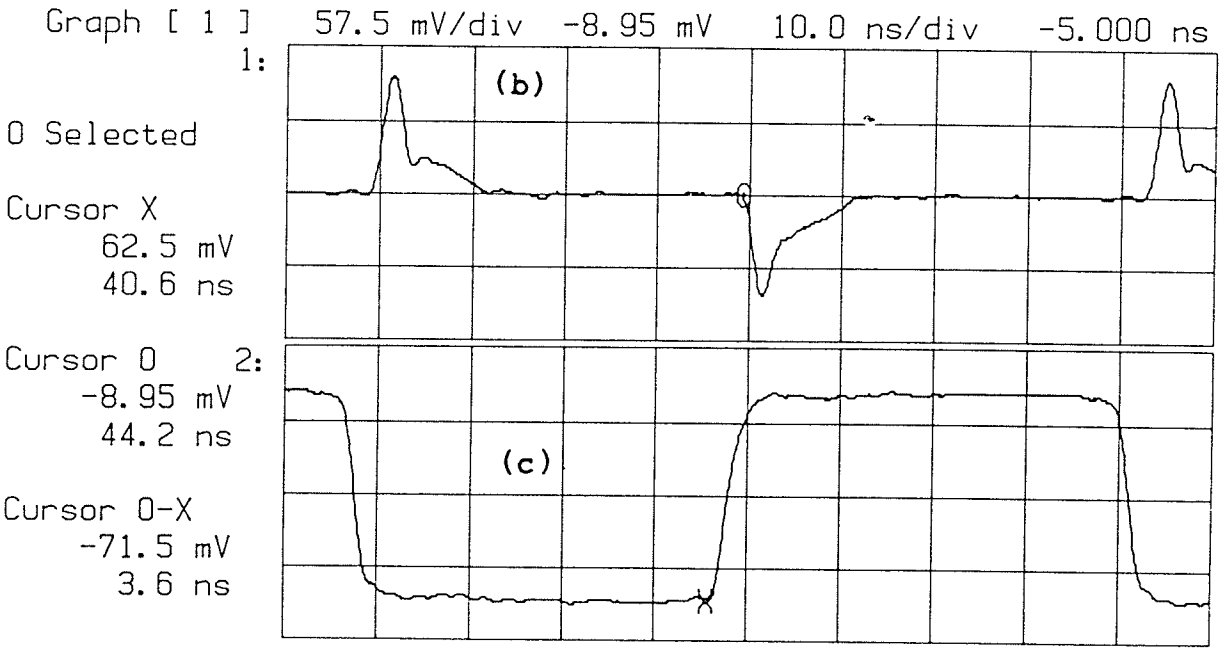


Figure 8.8: Backward crosstalk and input signal for scope setup. Trace 2a and Trace 2b are terminated with 50 Ω, and Trace 2c is floating: (a) backward crosstalk from Trace 2b; (b) backward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.





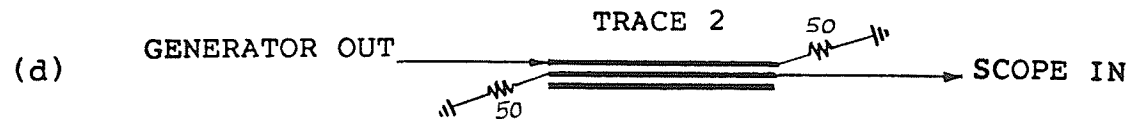


Figure 8.9: Forward crosstalk and input signal for scope setup. Trace 2a and Trace 2b are terminated with 50 Ω, and Trace 2c is floating: (a) forward crosstalk from Trace 2b; (b) forward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.

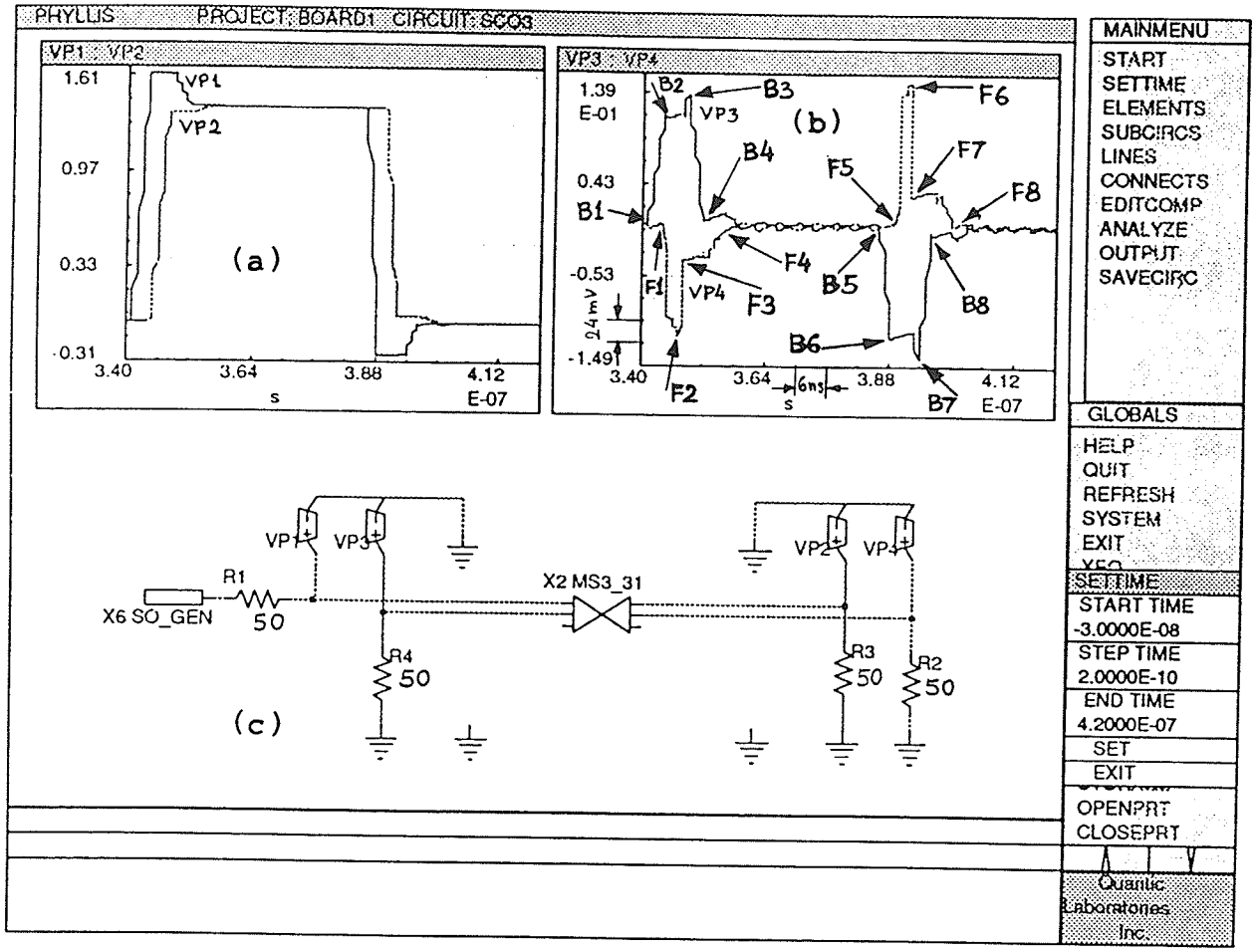


Figure 8.10: Results of simulation for three microstrips. Traces 2a and 2b are terminated with 50 Ω, and Trace 2c is floating: (a) input signal (VP1) and delayed output signal (VP2) in the first trace Trace 2a, both with reflections; (b) backward (VP3) and delayed forward (VP4) crosstalks in the second trace Trace 2b; and (c) schematic.

8.2.1 Verification of simulations for all Traces 2 terminated with 50 Ω

Let us consider the case when all traces are terminated with 50 Ω. In Fig. 8.11 to Fig. 8.13 , the simulation results can be compared with the measured results. The input signal is distorted because there is impedance mismatch between microstrip an coaxial cable — we can compare simulated input signal (Fig. 8.11.a) which is described by VP1 (voltage probe 1) and measured input signal in Fig. 8.11.e. There is overshoot from which the characteristic impedance of the microstrip may be calculated.

In Fig. 8.11.e , the measured input signal from Trace 2a is shown. The signal starts at point I1 — this represents the output of TDR generator. This signal goes through a coaxial cable which has the characteristic impedance equal to 50 Ω therefore it is perfectly matched to the output impedance of the TDR generator and there is no reflection. At point I2 the signal enters into Trace 2a which has the characteristic impedance equal to 67 Ω and there is a mismatch which gives an overshoot.

The time distance from point I1 to I2 is equal to two time delays of the coaxial cable because the signal travelled both ways. It is equal to 4.6 ns. A special high quality coaxial cable was used (type 874–A3). It has double–braid shielding and the inner conductor is a soft–copper wire surrounded by a polyethylene dielectric. The coaxial cable introduces only time delay and does not have any other influence so it was not included in the simulations.

At point I3 the signal was reflected from the termination equal to 50 Ω so there is an undershoot caused by the impedance mismatch. The time distance from point I2 to I3 is equal to two time delays of Trace 2a because the signal travelled one way and the reflected signal travelled back towards TDR scope and was plotted. It is equal to 7.2 ns which gives the time delay of Trace 2a equal to 3.6 ns.

The connectors and terminations were modelled by resistance equal to 50 Ω and capacitance equal to 5 pF in parallel (Fig. 8.11.c). In the simulations, the

signal was driving Trace 2a directly so the point I2 (Fig. 8.11.a) represents the begining of Trace 2a and this is the point where the signal is starting. Point I3 represents the termination which causes undershoot. The time distance from I2 to I3 is exactly the same in the result of simulation and measurement. Please notice the appropriate numbering. Let us compare a few points.

1. Measured input signal (Fig. 8.11.e). The difference between:

   points I3 and I2 : I3–I2=(7.2 ns , 35.7 mV);

   because I2=(1 ns , 285.7 mV) , and I3=(8.2 ns , 250 mV).

2. Simulated input signal (Fig. 8.11.a). The difference between:

   points I3 and I2 : I3–I2=(7.2 ns , 35 mV);

   because I2=(4.6 ns , 285 mV) , and I3=(11.8 ns , 250 mV).

The amplitude difference between measured and simulated input signal is equal to 0.7 mV that is 2 % for points I3–I2.

The time difference between measured and simulated input signal is equal to 0 ns that is 0 % for points I3–I2 (there is no difference).

We can compare the simulated backward crosstalk with the measured one in Fig. 8.13. The connectors and terminations were modelled by resistance equal to 50 Ω and capacitance equal to 10 pF in parallel (Fig. 12.c and Fig. 8.13.c), or by 50 Ω resistance and 5 pF capacitance in parallel (Fig. 8.11.c). Please notice the appropriate numbering. Let us compare a few points.

1. Measured backward crosstalk (Fig. 8.13.e). The difference between:

   points B3 and B1 : B3–B1=(7.2 ns , 28 mV).

2. Simulated backward crosstalk (Fig. 8.11.b). The difference between:

   points B3 and B1 : B3–B1=(7.2 ns , 40.5 mV).

3. Simulated backward crosstalk (Fig. 8.12.b). The difference between:

   points B3 and B1 : B3–B1=(7.2 ns , 43 mV).

4. Simulated backward crosstalk (Fig. 8.13.b). The difference between:

   points B3 and B1 : B3–B1=(7.2 ns , 39.5 mV).

The amplitude difference between measured and simulated backward crosstalk (between 1. and 2.) is equal to 12.5 mV that is 30.9 % for points B3–B1.

The amplitude difference between measured and simulated backward crosstalk (between 1. and 3.) is equal to 15 mV that is 34.9 % for points B3–B1.

The amplitude difference between measured and simulated backward crosstalk (between 1. and 4.) is equal to 11.5 mV that is 29.1 % for points B3–B1.

The time difference between measured and simulated backward crosstalk is equal to 0 ns that is 0 % for points B3–B1 (there is no difference).

We can compare the simulated forward crosstalk with the measured one in Fig. 8.12. The forward crosstalk is always delayed by the time delay of the transmission line which is equal to 3.6 ns. The forward crosstalk becomes bigger with the increase of the length of the transmission line, and because considered microstrips were quite long, the forward crosstalk is rather big. Please notice the appropriate numbering. Let us compare a few points.

1. Measured forward crosstalk (Fig. 8.12.e). The difference between:
   points F2 and F1 : F2–F1=(1.1 ns , 66.4 mV).
2. Simulated forward crosstalk (Fig. 8.11.b). The difference between:
   points F2 and F1 : F2–F1=(1.0 ns , 75 mV).
3. Simulated forward crosstalk (Fig. 8.12.b). The difference between:
   points F2 and F1 : F2–F1=(1.0 ns , 55 mV).
4. Simulated forward crosstalk (Fig. 8.13.b). The difference between:
   points F2 and F1 : F2–F1=(1.0 ns , 48 mV).

The amplitude difference between measured and simulated forward crosstalk (between 1. and 2.) is equal to 8.6 mV that is 11.5 % for points F2–F1.

The amplitude difference between measured and simulated forward crosstalk (between 1. and 3.) is equal to -11.4 mV that is -20.7 % for points F2–F1.

The amplitude difference between measured and simulated forward crosstalk (between 1. and 4.) is equal to -18.4 mV that is -38.3 % for points F2–F1.

The time difference between measured and simulated forward crosstalk is equal to -0.1 ns that is -10 % for points F2–F1.

Extensive simulations were performed for this setup. The simulation results are very similar to those obtained from measurements. The time delays, amplitudes and shapes of signals are correct. The simulated amplitude of the crosstalk is strongly depending on the modelling of the connectors and terminations. The connectors and terminations were modelled by resistance equal to 50 Ω and capacitance equal to 10 pF in parallel (Fig. 8.12.c and Fig. 8.13.c). It looks that the closest approximation was obtained for modelling of connectors with terminations by 50 Ω resistance and 5 pF capacitance in parallel (Fig. 8.11.c). Only the value of capacitance in parallel with resistance was changed.

The time simulation results for the backward crosstalk are exactly the same. The simulated amplitude of the backward crosstalk is bigger than measured by about 30 %. The simulated time results are smaller than measured for the forward crosstalk and they are accurate to about -10 %. The simulated amplitude of the forward crosstalk is bigger than measured by about 11 % for the capacitance equal to 5 pF. The simulated amplitude of the forward crosstalk is smaller than measured by about -20 % for the capacitance equal to 10 pF.

It should be noted that the simulation gives a lot of information at once — all signals may be displayed simultaneously, while each measurement requires a specific setup of cable connections.

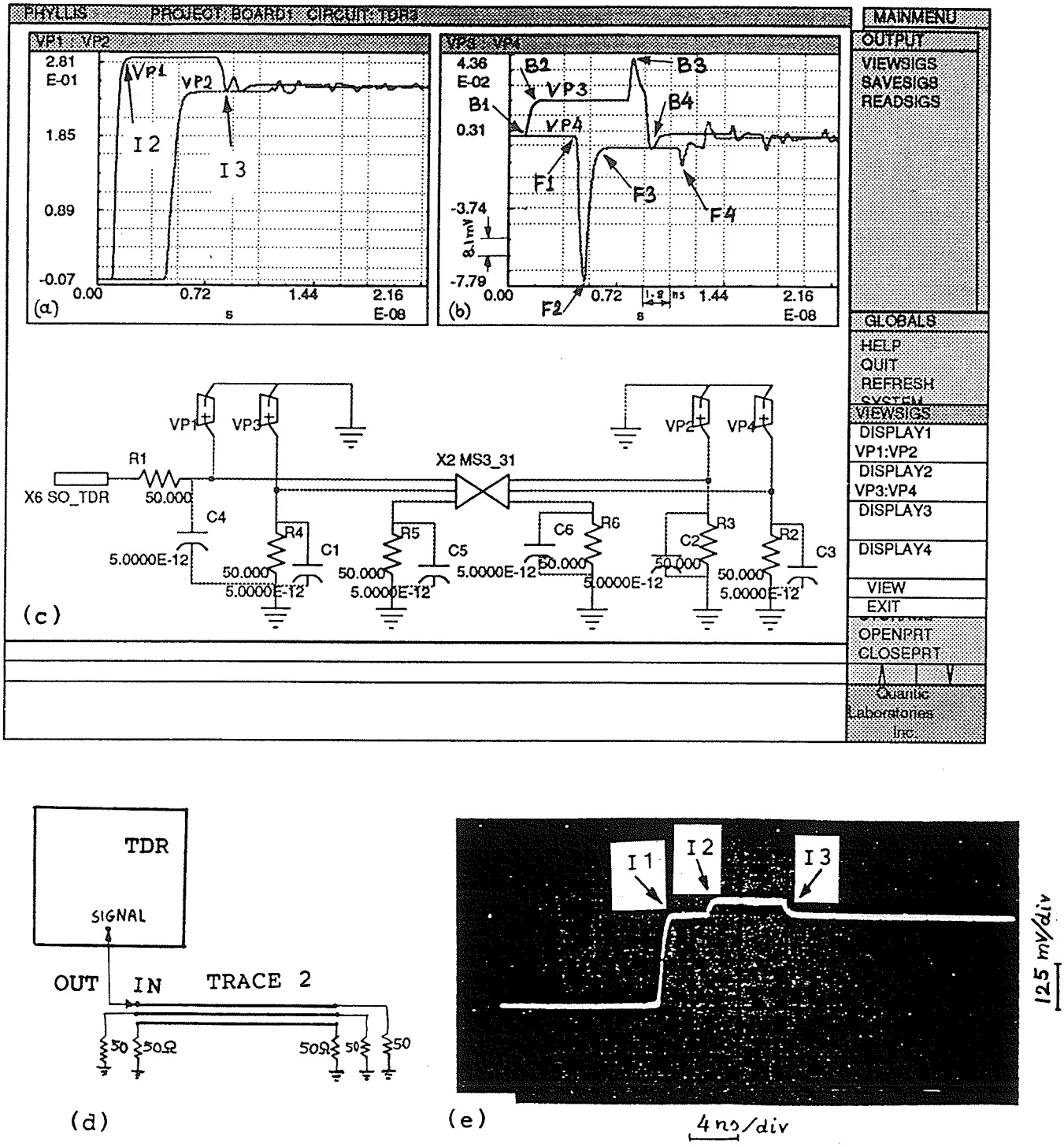


Figure 8.11: Signals from parallel microstrips — all traces terminated with 50 Ω. Terminations modelled as 50 Ω resistance and **5 pF** capacitance, and the input signal connector modelled as **5 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) measurement TDR setup; and (e) measured input signal, reflected from 67 Ω microstrip and delayed by coaxial cable (compare with VP1).

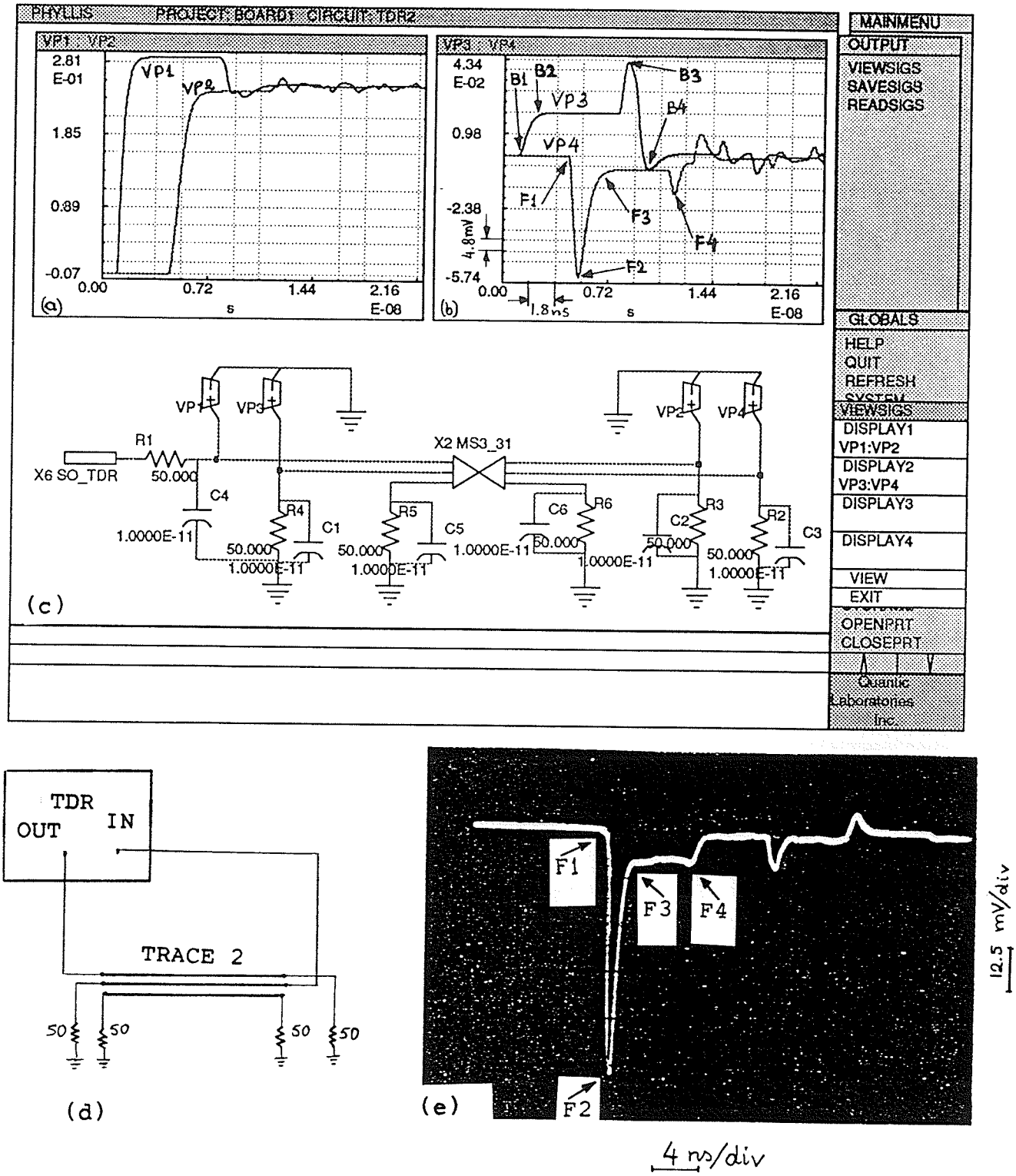


Figure 8.12: Signals from parallel microstrips — all traces terminated with 50 Ω. Terminations modelled as 50 Ω resistance and **10 pF** capacitance, and the input signal connector modelled as **10 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) measurement TDR setup; and (e) measured forward crosstalk in Trace 2b coupled from Trace 2a (compare with VP4).

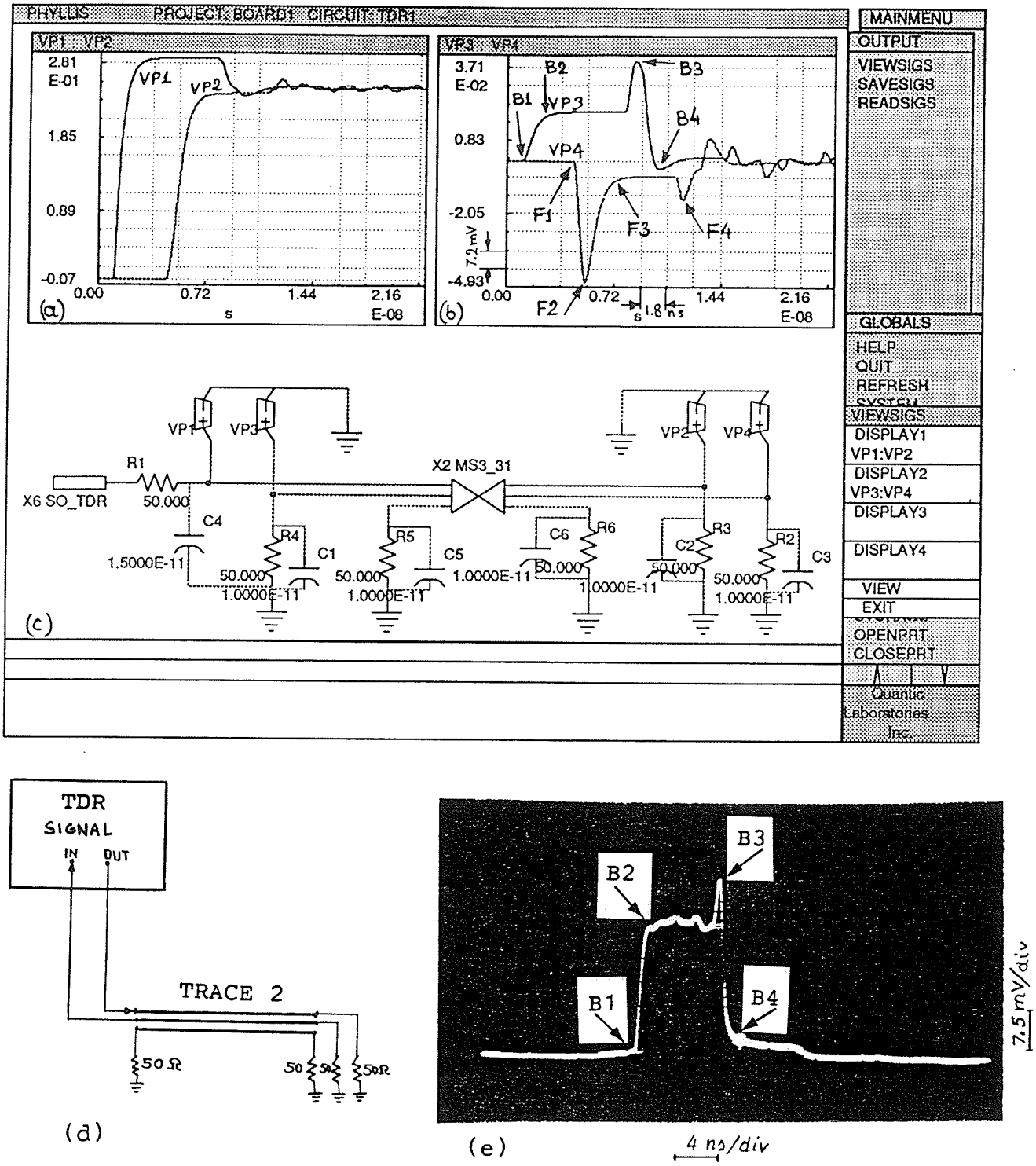


Figure 8.13: Signals from parallel microstrips — all traces terminated with 50 Ω. Terminations modelled as 50 Ω resistance and **10 pF** capacitance, and the input signal connector modelled as **15 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) measurement TDR setup; and (e) measured backward crosstalk in Trace 2b coupled from Trace 2a (compare with VP3).

8.2.2 Verification of TDR setup simulations for Trace 2c floating

Let us consider what happens when the third trace is floating which means that its both ends are terminated with the infinite impedance. Any signal generated in third trace will be reflected at the end of the trace and will be bouncing producing ringing in this trace. That ringing signal will generate crosstalk in the neighbourhood.

Let us keep the first and second trace terminated with 50 Ω. The connectors and terminations were modelled by resistance equal to 50 Ω and capacitance equal to 10 pF in parallel (Fig. 8.15.c). The measured backward and forward crosstalk and the corresponding setup is shown in Fig. 8.14. The results of simulation are shown in Fig. 8.15 together with the measured crosstalks. We can see very good accordance between measured and simulated results. The amplitude of both crosstalks increased by several mV, as expected (compare Fig. 8.12 with Fig. 8.15). Please notice the appropriate numbering. Let us compare a few points.

1. Measured backward crosstalk (Fig. 8.14.b). The difference between:
   points B3 and B1 : B3–B1=(7.2 ns , 39 mV).
2. Measured backward crosstalk (Fig. 8.15.d). The difference between:
   points B3 and B1 : B3–B1=(7.2 ns , 38 mV).
3. Simulated backward crosstalk (Fig. 8.15.b). The difference between:
   points B3 and B1 : B3–B1=(7.2 ns , 59 mV).

The amplitude difference between measured and simulated backward crosstalk (between 1. and 3.) is equal to 20 mV that is 33.9 % for points B3–B1.

The amplitude difference between measured and simulated backward crosstalk (between 2. and 3.) is equal to 21 mV that is 35.6 % for points B3–B1.

The time difference between measured and simulated backward crosstalk is equal to 0 ns that is 0 % for points B3–B1 (there is no difference).

The forward crosstalk becomes bigger with the increase of the length of the transmission line, and because considered microstrips were quite long, the forward

crosstalk is rather big. Please notice the appropriate numbering. Let us compare a few points.

1. Measured forward crosstalk (Fig. 8.15.e). The difference between:
   points F2 and F1 : F2–F1=(1.1 ns , 69 mV).
2. Simulated forward crosstalk (Fig. 8.15.b). The difference between:
   points F2 and F1 : F2–F1=(1.0 ns , 60 mV).

The amplitude difference between measured and simulated forward crosstalk is equal to -9 mV that is -15 % for points F2–F1.

The time difference between measured and simulated forward crosstalk is equal to -0.1 ns that is -10 % for points F2–F1.

The simulation results are quite similar to those obtained from measurements. The time delays, amplitudes and shapes of signals are correct. The time simulation results for the backward crosstalk are exactly the same. The simulated amplitude of the backward crosstalk is bigger than measured by about 35 %. This difference is caused by the fact that the equivalent capacitances of connectors and terminations were modelled by 10 pF. The simulated time results are smaller than measured time results for the forward crosstalk and they are accurate to about -10 %. The simulated amplitude of the forward crosstalk is smaller than measured by about -15 %.

We can also observe the crosstalk coupled from the third trace to second trace which is reflected from the ends thus causing ringing. First there is coupling of crosstalk from first trace to second and third trace. Next the crosstalk on the third trace is coupled to second and first trace — the value of this crosstalk is small because only small part of the signal is coupled as crosstalk at each time.

We can see that the whole system is working together and each signal is depending on the other signals. This shows how important it is what we discuss in this thesis. This example shows that each transmission line in the system should be properly terminated not only the lines which transmit the signals.

At the time of doing simulations it seemed that the best approximation of connectors with terminations could be obtained by modelling them by resistance of 50 Ω and capacitance 10 pF in parallel. Some data books say that the input capacitance of a pin of a semiconductor chip is about 10 pF [FAST82], [Moto86]. Many simulations were done with these values. Though, later by comparison, it was found that the capacitance value should be between 1 pF and 5 pF. For these values, the simulated crosstalk graphs become smooth and very similar to the measured graphs and also the amplitudes become closer. The SMA type connectors and terminations are very good. They have very low equivalent capacitance, which is not even listed in the data books.

The discovered facts about capacitance modelling may have quite practical application to the package modelling. The input capacitance of a ECL circuit is about 3 pF [Bloo82], [ECLU86], [F100K]. The presented results may be easily applied in this case. Test specifications sometimes call for timing measurements to be performed with specified lumped capacitive loads on the order of 25 pF to 100 pF [Barb 84]. Techniques have been documented for testing high–impedance MOS device outputs that drive a lumped pin–electronics capacitive loads of roughly 30 pF [BaSa87], [Barb84].

8.2.3 Discussion of corners

An effort was made to measure the influence of corners. Very interesting results were obtained by comparing measured signals and simulated signals for the microstrip with two corners. The corner may be modelled by an equivalent LC low–pass filter. The values of capacitance and inductance may be calculated from the three dimensional BEM analysis. The value of capacitance obtained from the three dimensional simulation was about 0.02 pF (from: Neil Aitken). This is a very small capacitance.

The approximation value of capacitance of one corner may be calculated from the formula (2.12) included in Chapter II. Let us take a square parallel capacitor

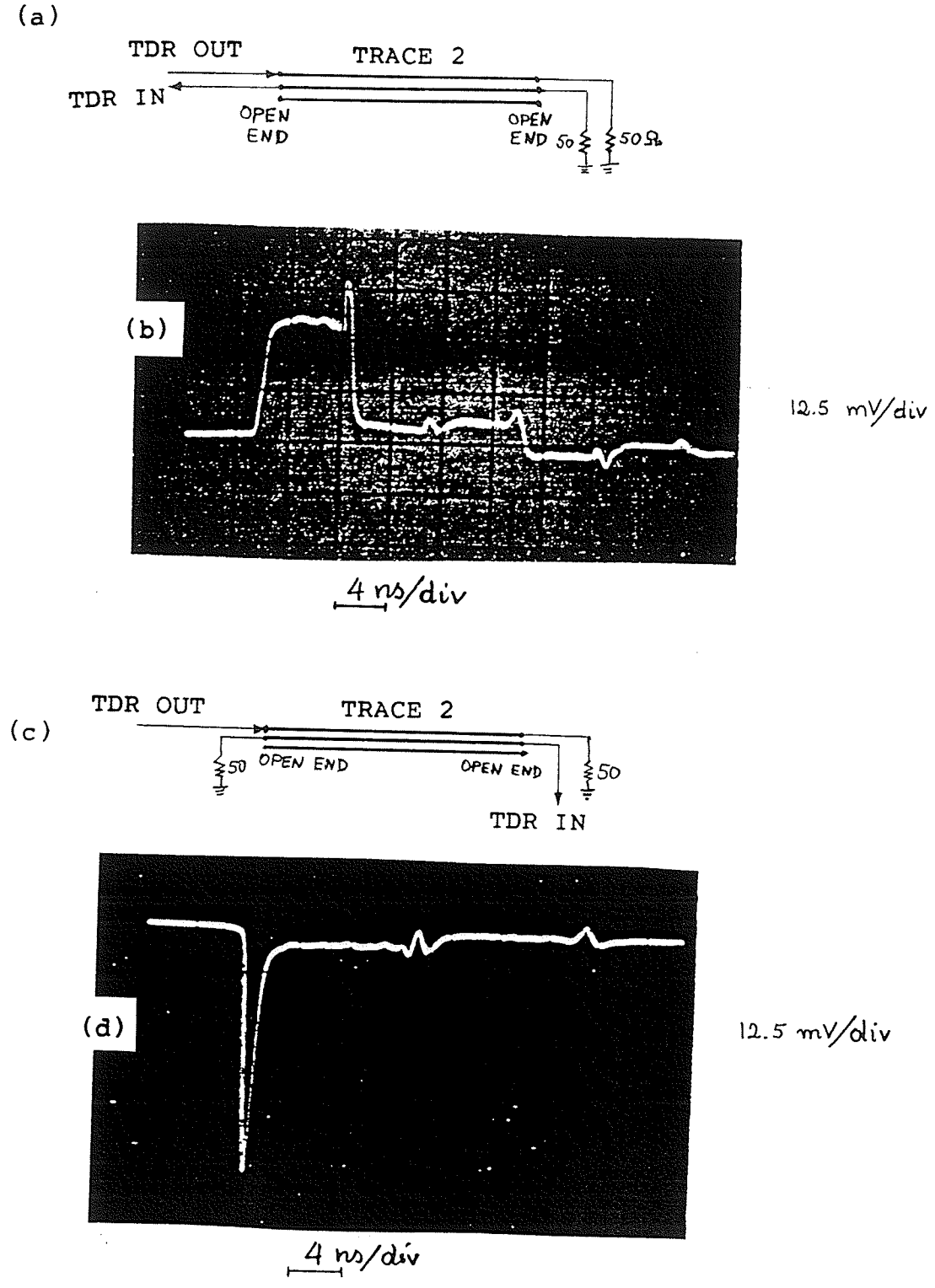


Figure 8.14: Measured backward and forward crosstalk — third trace floating. (a) measurement TDR setup; (b) backward crosstalk in Trace 2b coupled from Trace 2a; (c) measurement TDR setup; and (d) forward crosstalk in Trace 2b coupled from Trace 2a.

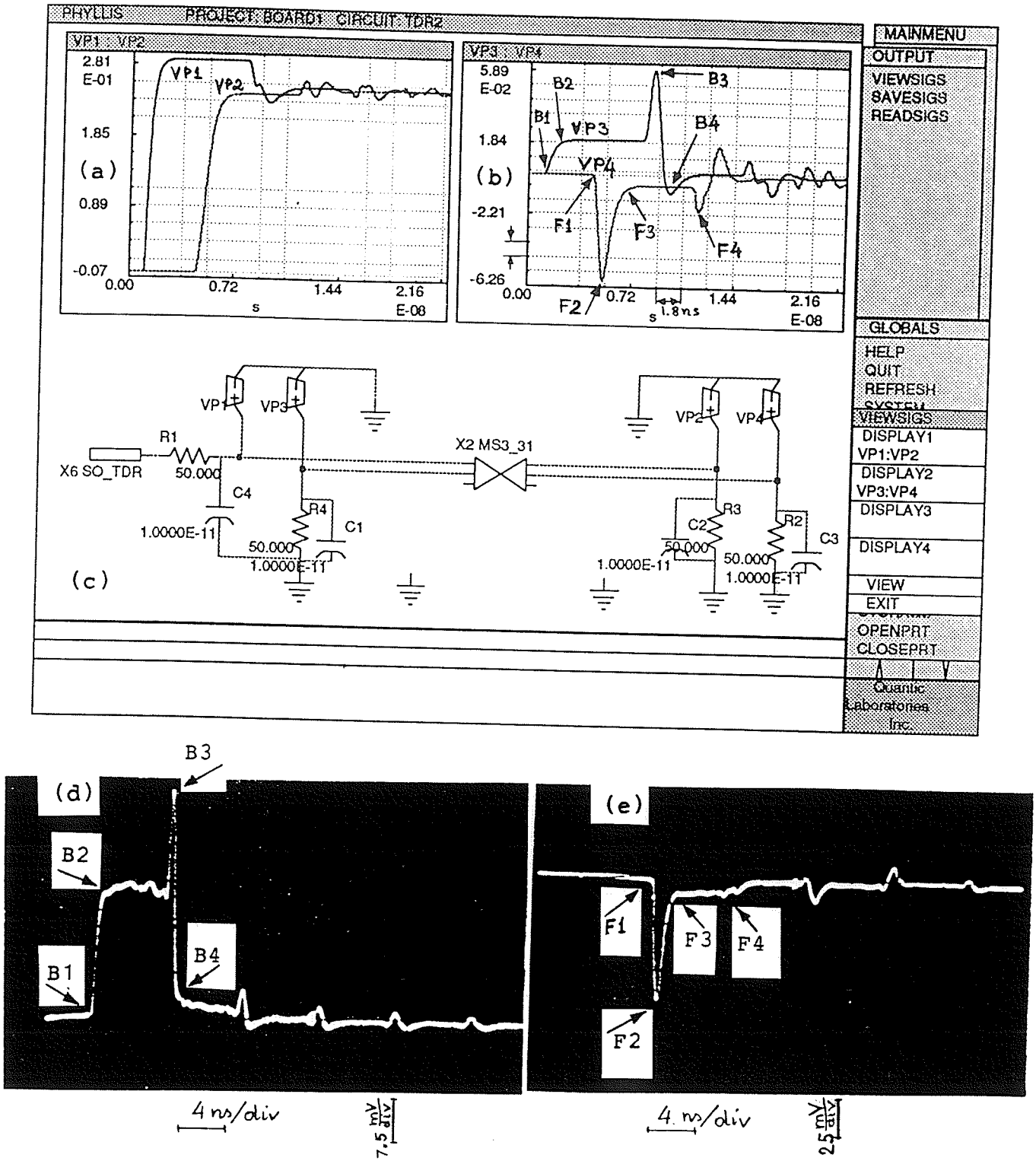


Figure 8.15: Verification of simulations with Trace 2c floating. Terminations modelled as 50 Ω resistance and 10 pF capacitance, and the input signal connector modelled as 10 pF capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a: (b) backward and forward crosstalks in Trace 2b; (c) schematic; (d) measured backward crosstalk in Trace 2b (compare with VP3); and (e) measured forward crosstalk in Trace 2b (compare with VP4).

with the length of one side equal to 31 mil, distance between the plates equal to 31 mil and a dielectric constant equal to 4.7. One may calculate the capacitance from this formula to be equal to 0.033 pF. This is quite close to the three dimensional simulation result.

First the corners in Trace 3, 4, and 5 were carefully measured. It was very intersting what the difference between a corner of 90 degrees and a corner of 45 degrees is. The comparison is shown in Fig. 8.16 where measurement results for Trace 4 and 5 are shown together with the measurement setup. We can see the small peak in the middle of each signal. This is caused by the forward crosstalk from the second part of the trace spaced by 7 mm (275 mil). The signal in one arm of the trace induced a forward crosstalk in the other arm which travelled simultaneously with the signal towards the corners.

They travelled the same distance and met where the corners were so it looked at the begining as the peak was caused by the corners but it was not. The peak was simply the forward crosstalk — it is interesting that the crosstalk was coupled even with such big spacing. The design of these traces was wrong. It is very interesting because it shows that even with such big spacing between traces the coupling of crosstalk is quite significant. The crosstalk should be taken into consideration whenever a high–speed board is designed.

The forward crosstalk travelled towards the source and can be observed as the peak, while the signal continued to travel towards the load. Therefore the peak is not caused by the corners but by this parasitic crosstalk. The infuence of the corners is very small and may be neglected. There is no practical difference between these two types of corners. One corner is practically unmeasurable even with such specialized equipment as TDR which represents the limits in measurements.

The results of simulation and measurements are included in Fig. 8.16 to Fig. 8.20. The measured waveforms can be easily compared with simulated. The

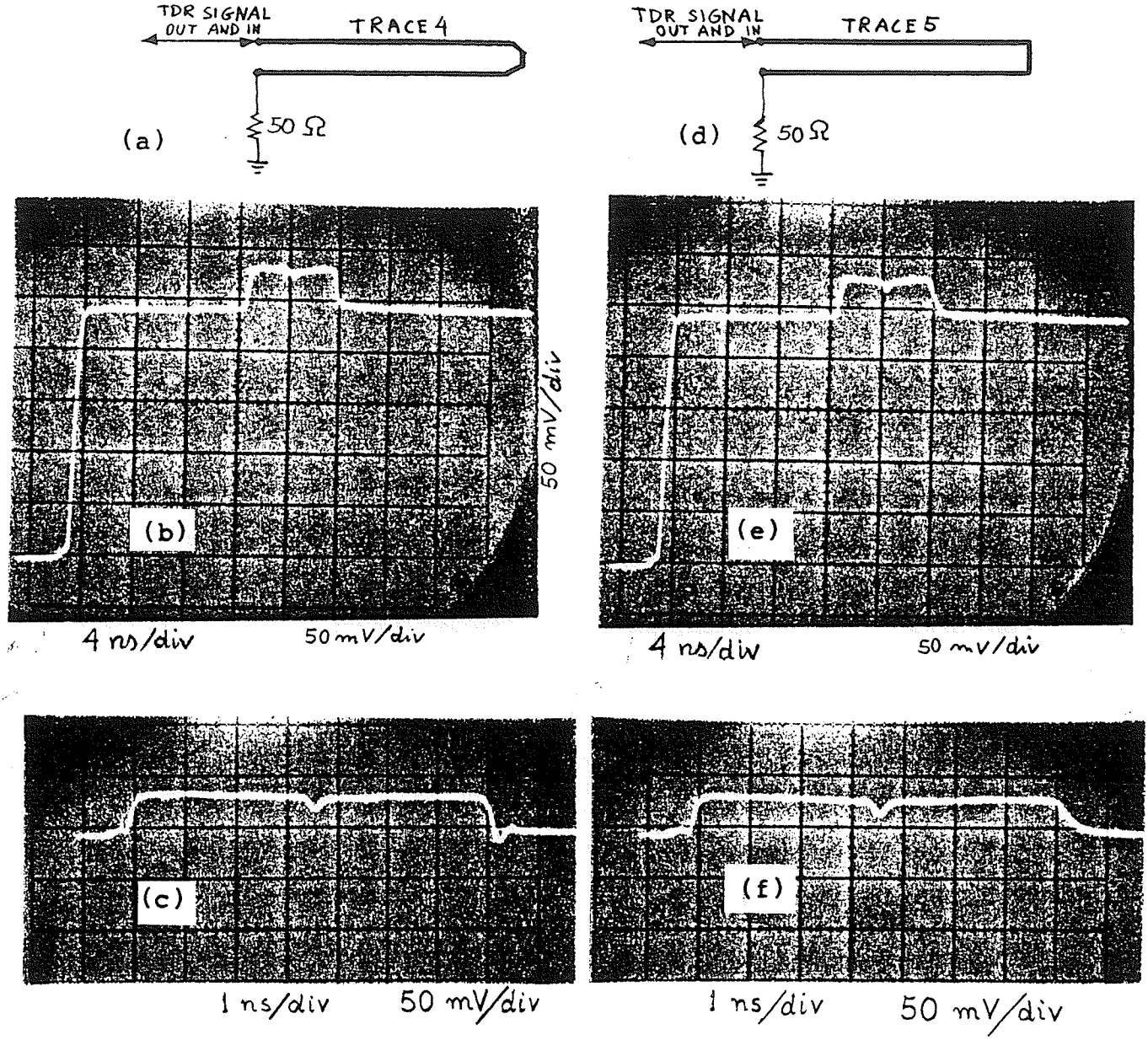


Figure 8.16: Measured results for Trace 4 and Trace 5. (a) TDR setup for Trace 4; (b) result for Trace 4; (c) result for Trace 4 in detail; (d) TDR setup for Trace 5; (e) result for Trace 5; and (f) result for Trace 5 in detail.

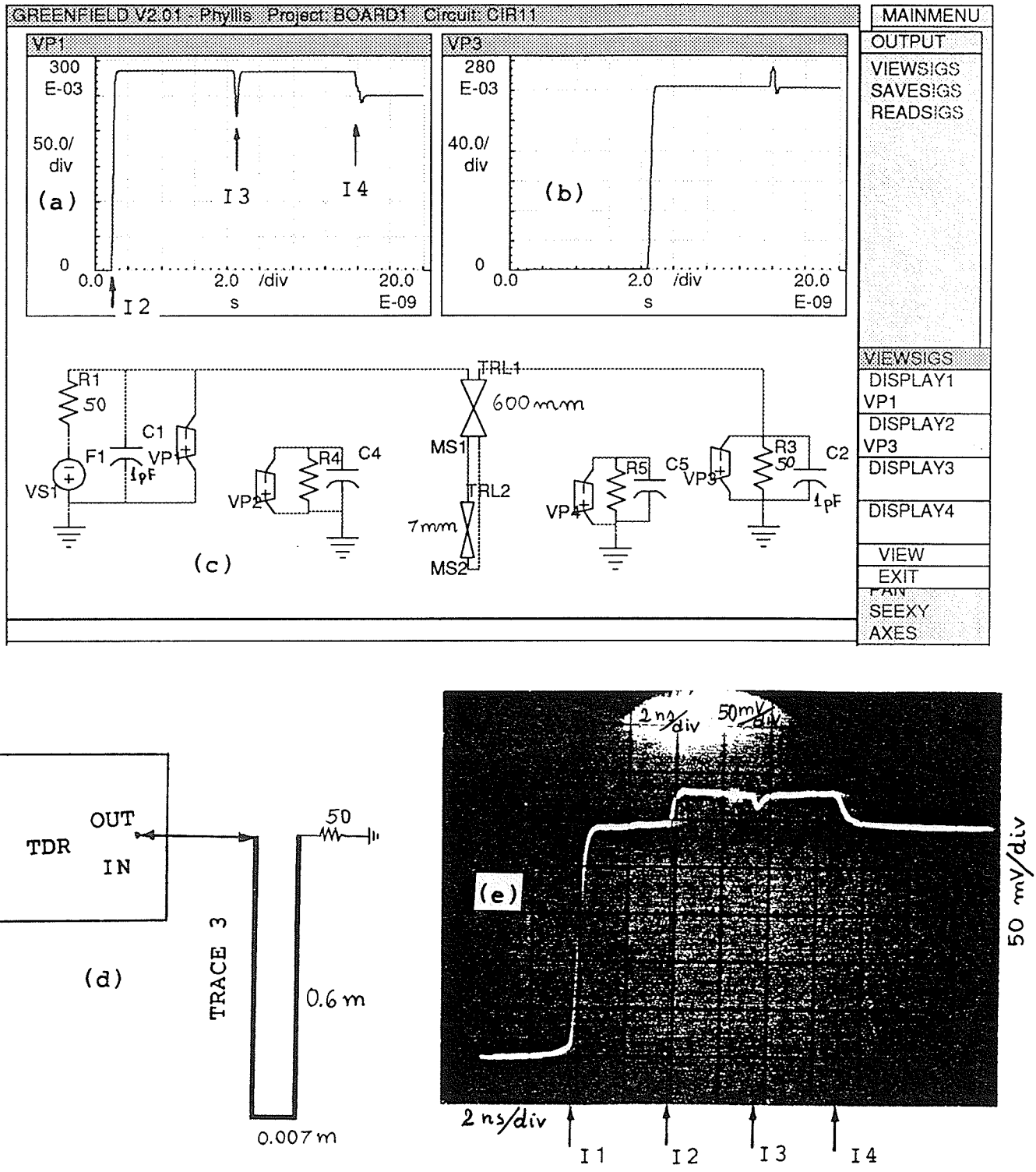


Figure 8.17: Comparison of measured cnd simulated results for Trace 3. The peak is caused by forward crosstalk coupled to the second arm of Trace 3 and transmitted towards source.

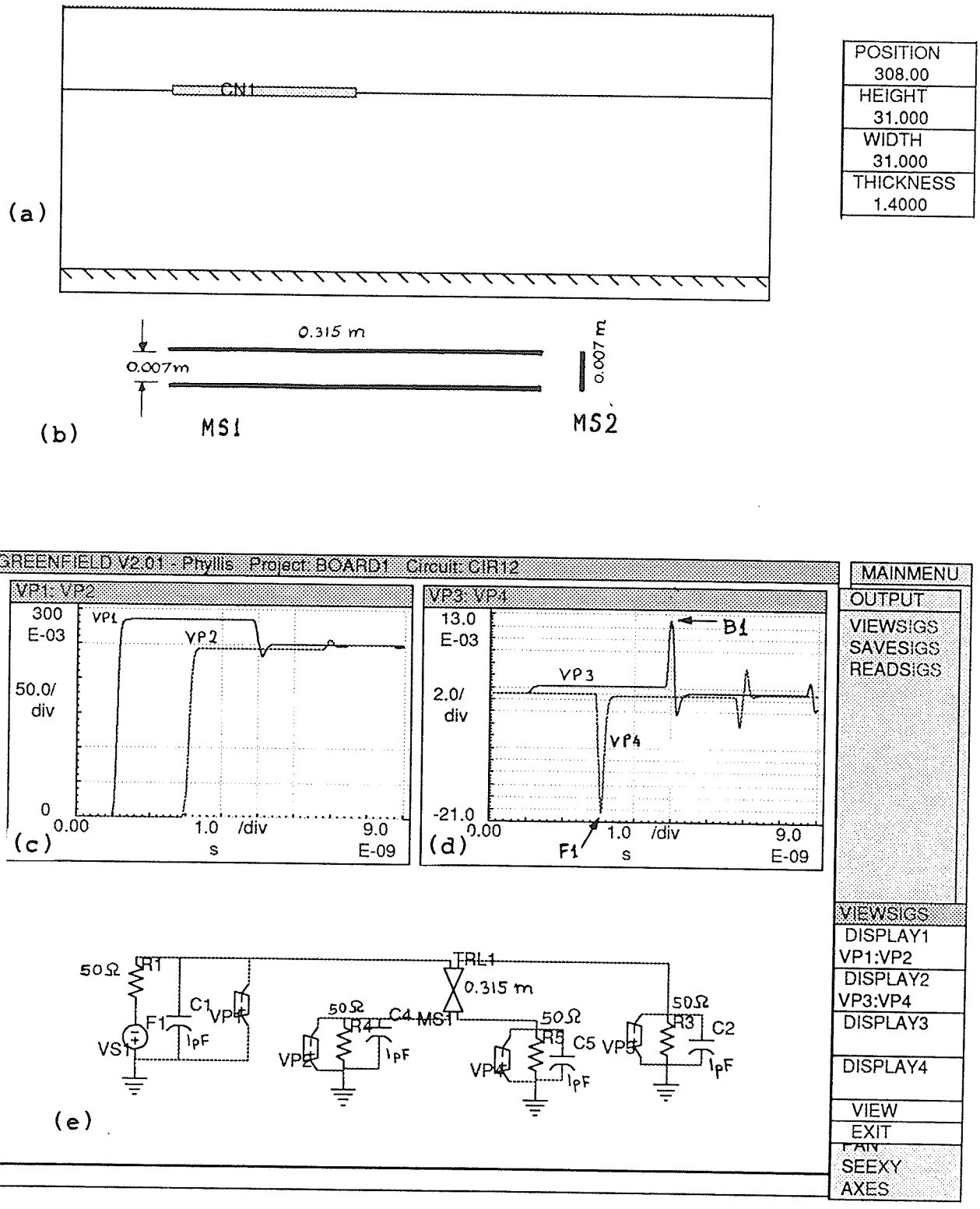


Figure 8.18: Simulation of Trace 4 or Trace 5. Forward crosstalk is quite big (VP4) — it is proportional to the length of the trace.

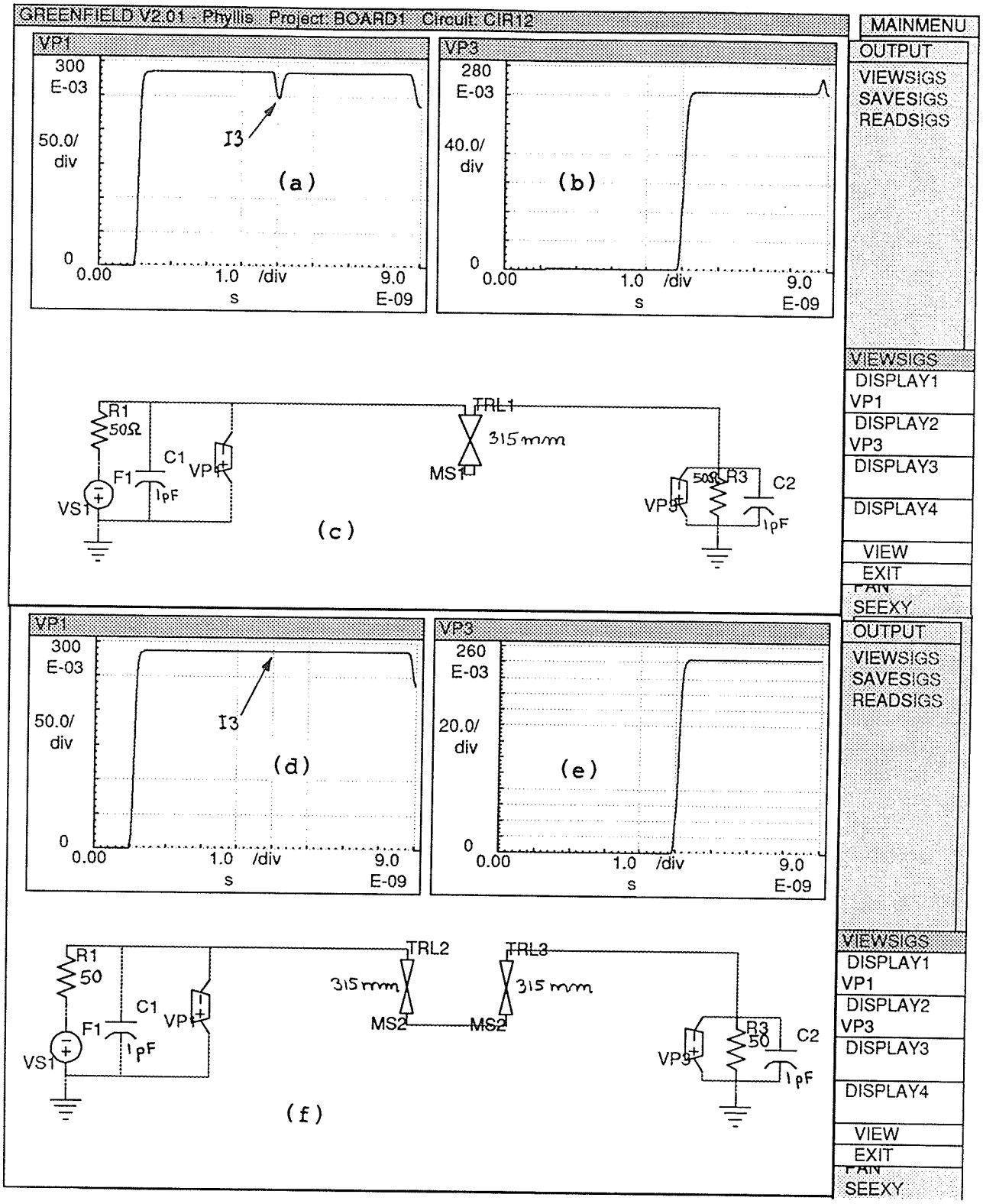


Figure 8.19: Simulation of Trace 4 or Trace 5. Forward crosstalk is causing the peak at point I3 — when the arms of the trace are completely separated, there is no peak.

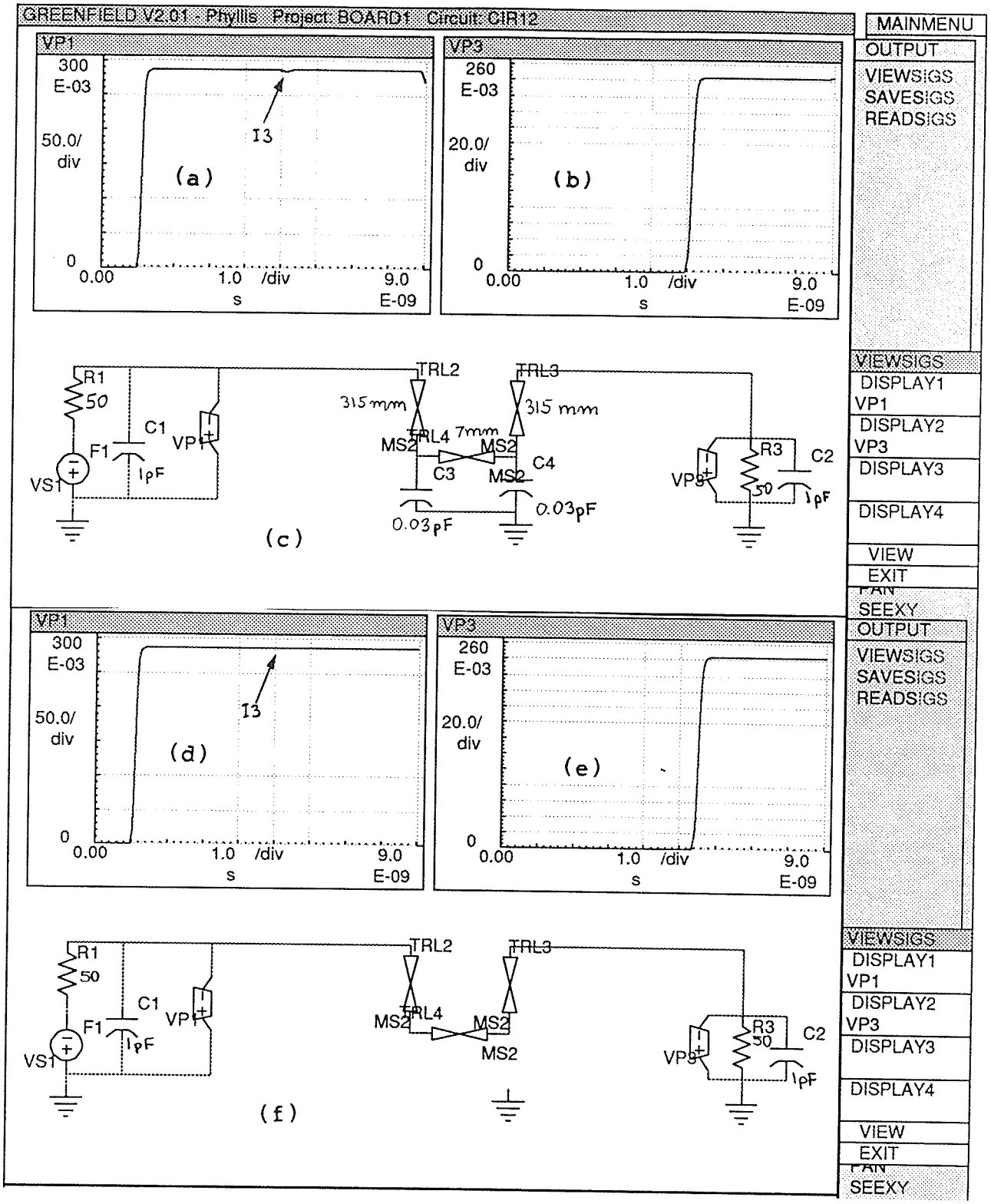


Figure 8.20: Simulation of Trace 4 or Trace 5 and two corners as 0.03 pF each. Two arms are modelled by separate microstrips — corner capacitances cause a small peak downward which disappears when they are removed.

simulations were performed with different methods of representing of the microstrip between the corners.

Figure 8.17 shows the comparison of measured and simulated results for Trace 3 which has two microstrip arms of length equal to 0.6 m and two corners connected by a very short piece of microstrip of length equal to 0.007 m. The spacing between the arms is 0.007 m. The signal was fed through a coaxial cable which can be easily recognized by the time delay between point I1 and I2 on the measured result. The cable produces some attenuation of the signal.

The point I3 represents the position of the 2 corners — the interconnecting short piece of microstrip produces no practical delay and therefore may be neglected. The downward peak at point I3 is caused by the coupled forward crosstalk travelling towards the source. The point I4 represents the termination — the connector and resistor of 50 Ω.

Figure 8.18 shows the cross–section of each of the traces. Trace 3, 4 and 5 may be devided into two parts — one part is built from two long, parallel microstrip lines spaced by 0.007 m, and the second part is built from two corners and a short piece of single microstrip (0.007 m) which connects the two corners, and therefore the two arms. Traces 4 and 5 are shorter than Trace 3 — their length is equal to about 0.315 m.

The results of simulation in Fig. 8.18 show that the forward crosstalk is coupled from one arm to the other. The amplitude of the forward crosstalk at point F1 on the graph of signal VP4 (Fig. 8.18.d) is equal to 20 mV. This crosstalk is moving towards the source and can be observed as the downward peak on Fig. 8.17 and Fig. 8.19. It is not caused by the corners but by the forward crosstalk. The simulated value of the downward peak at point I3 on graph VP1 in Fig. 8.19.a is equal to 37 mV. The corresponding measured value of the downward peak at point I3 on graph VP1 in Fig. 8.16.f is equal to 18 mV. The backward crosstalk (VP3)

(Fig. 8.18.d) is very small and the peak at the point B1 is simply a reflection of the forward crosstalk at the load.

Figure 8.19 shows the comparison of signals obtained from two microstrips of the same length and configuration. First, the Trace 4, or 5 are modelled by the two parallel microstrip arms — the forward crosstalk is coupled from one arm to the other and produces a downward peak at point I3 (Fig. 8.19.a) of signal VP1. Next, the two arms of these traces are modelled by two separated, single microstrips and no crosstalk is observed (Fig. 8.19.d) — and also no peak is observed on the graph of signal VP1.

Figure 8.20 shows what happens when Trace 4 or 5 are modelled by two, separated, single microstrips, and the connection between the corners is modelled by a single, short (0.007 m) piece of microstrip. First, the two corners are modelled by an equivalent 0.03 pF capacitance each. One can observe a very small downward peak in signal VP1 caused by these corner capacitances which practically may be neglected (at point I3 in Fig. 8.20.a).

Next these corner capacitances are removed and the peak in signal VP1 disappears — so they were produced by the corner capacitances. The influence of 0.007 m piece of microstrip is difficult to be noticed therefore it can be neglected.

The general conclusion is that Greenfield is capable of simulating the printed circuit boards and produce results with good accordance with the measured results. It is very important how the connectors and terminations are modelled. They should be modelled as accurate as possible. First, resistances equal to 50 Ω were used. As a result, the shapes and amplitudes of signals were very similar to the measured signals but there were some small differences. Next capacitors were added in parallel with resistors. The value of 1 pF caused desirable change in the shape and amplitudes of the signals. The equivalent capacitance should be between 1 pF and 5 pF. Bigger capacitance, for instance 10 pF, caused bigger differences between simulated and measured results.

8.3 PCB for measurements of vias, corners and crossovers

A scaled printed circuit board was designed for measuring transmission lines such as microstrips or striplines with vias, corners and crossovers. The board was designed to have rather big dimentions (350 mm long and 260 mm wide board) to enable measuring of time delay, ringing, and crosstalk (this is why it is called scaled). The schematic circuit of the designed board is shown in Fig. 8.21. This schematic contains SMA type connectors (high performance miniature microwave connectors) and iterconnecting lines. The purpose of this design was to measure the characteristic impedances and time delays of different traces — transmission lines.

From these measurements it could be possible to calculate the equivalent capacitance and inductance of the line, via, corner and crossover. It is practically impossible to measure the effect of only one via, corner or crossover because it is very small. Instead, a method was proposed to measure these small parameters by measuring not one but many identical vias or corners distributed along the line (trace).

Let us consider vias — the same applies to corners. Many vias, equally spaced and distributed along the trace would equally contibute to the equivalent capacitance and inductance of the trace. First the characteristic impedance Z_o and the propagation delay t_{pd} should be measured for both lines of equal length — one with vias and one without.

Next the capacitance and inductance per length of each line could be calculted from the equations:

$$C = \frac{t_{pd}}{Z_o} \tag{8.1}$$

$$L = CZ_o{}^2 \tag{8.2}$$

The difference between these two capacitances would give the equivalent capacitance of the via. The distance between each two vias should be small and much smaller

then the wavelength of the testing signal so that there would be no reflections and ringing between vias.

The top view (the solder side) of the scaled PCB is shown in Fig. 8.22. The bottom view (the component side) of the scaled PCB is shown in Fig. 8.23. The cross–section of the PCB is shown on Fig. 8.24. For this board, the cross–section, dimensions, spacing and routing of the traces are very important. This is very tedious process to design such a board and CAD software for PCB design does not help in this case. This software may be very efficient to design a typical PCB but it is not convenient to design this special board in which the position of each trace is of most importance.

8.4 Suggestions for future work

The future work should go in the direction of designing two multilayered boards (4–layer and 6–layer boards) for testing the FAST TTL, HC CMOS, and ECL devices driving transmission lines (embedded microstrip and stripline lines). The 4–layer board could have a ground–plane, power–plane and two layers of traces with microstrips and embedded microstrips. It would be easier to design and test this board, and the cost would be lower but there would be no more layers for striplines. The 6–layer board could have a ground–plane, power–plane, two layers of striplines and two layers of traces with microstrips and embedded microstrips. The cross–section of these boards should be symmetrical to enable an easy simulation of vias.

Table 8.1 provides the rise time data for most logic families, including older ones. This data can be very useful to design the testing boards. Transmission–line effects may be ignored, when interconections are short. The table indicates the longest interconnection path that one can treat as lumped. If one can not eliminate transmission line effects, one should apply transmission line theory to ensure the proper operation of those circuits that drive or include transmission lines.

The interconnections on the testing board should be longer then those specified in Table 8.1. Special connectors should be used for measurements — SMA

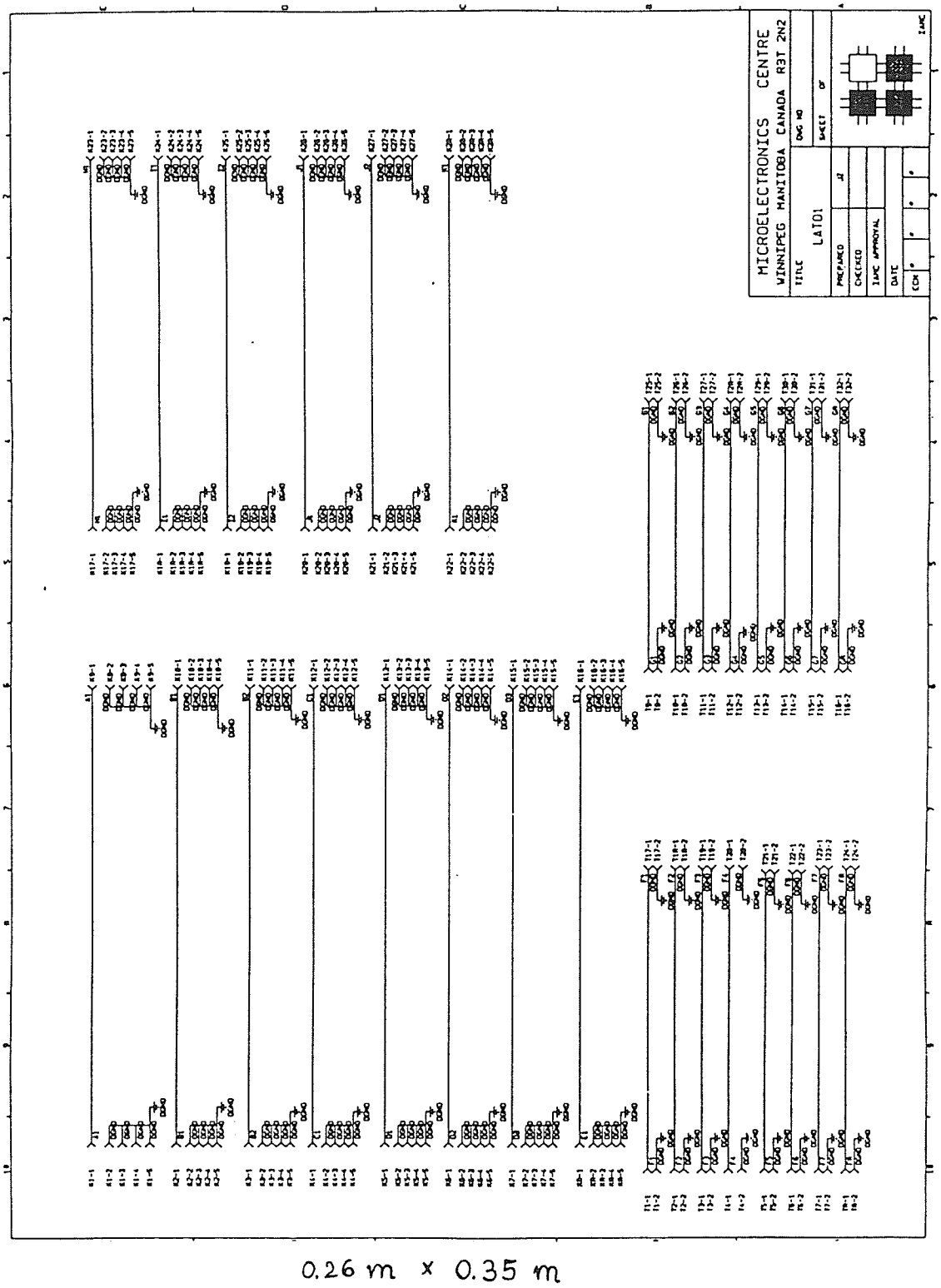


Figure 8.21: Schematic circuit of the designed PCB. The PCB for measurements of vias and corners.

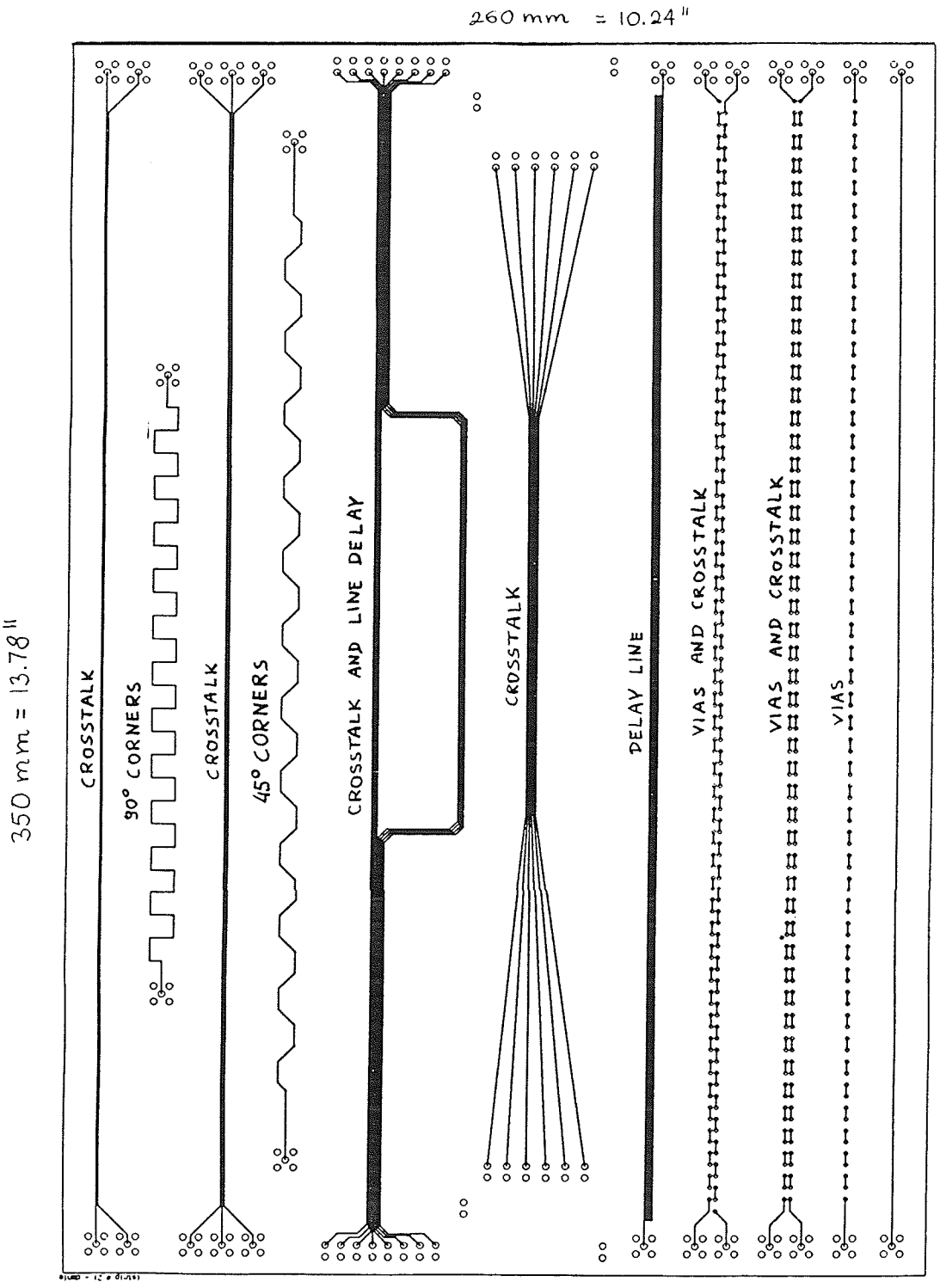


Figure 8.22: Top view of the designed PCB. The solder side of the board for measurements of vias and corners.

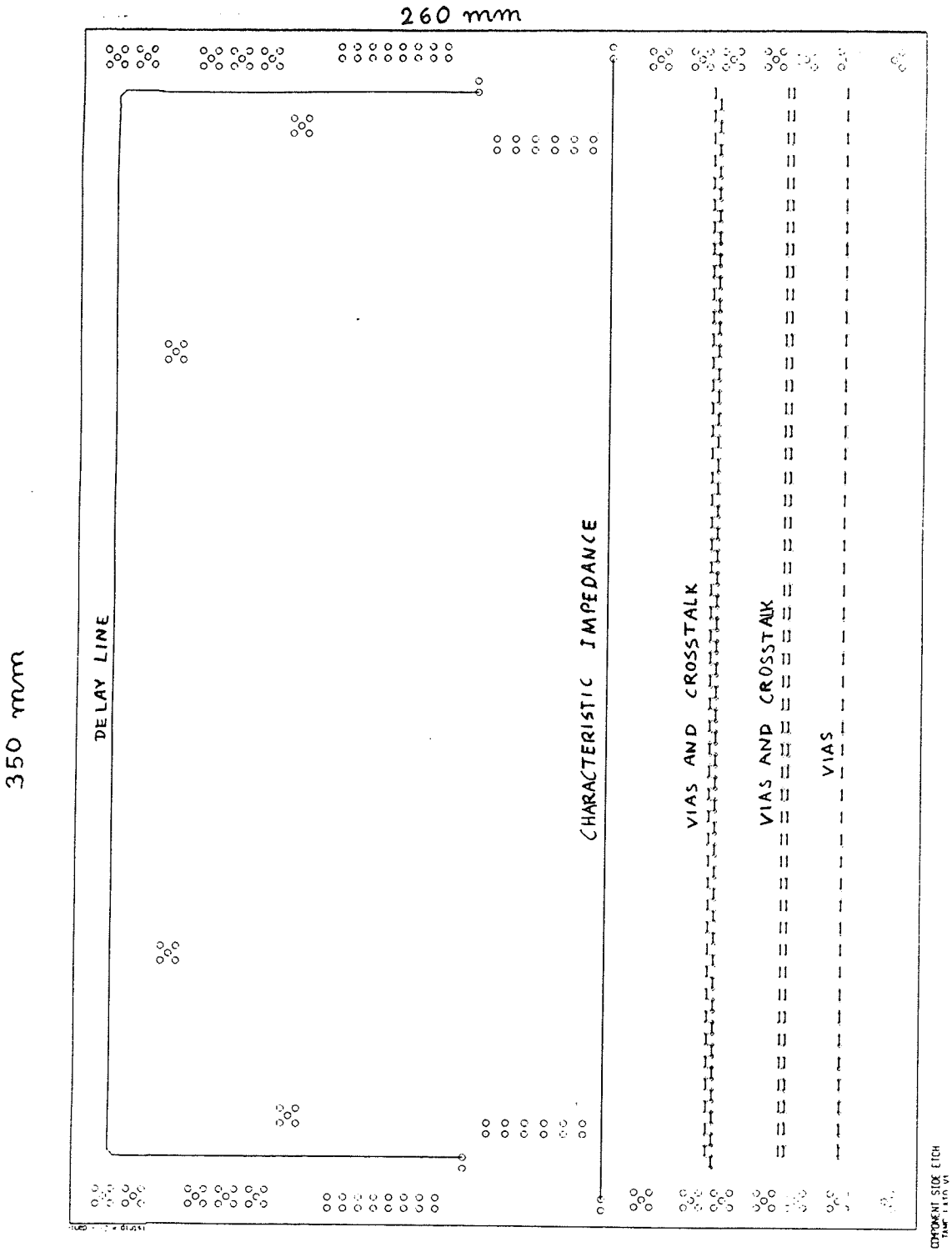


Figure 8.23: Bottom view of the designed PCB. The component side of the board for measurements of vias and corners.

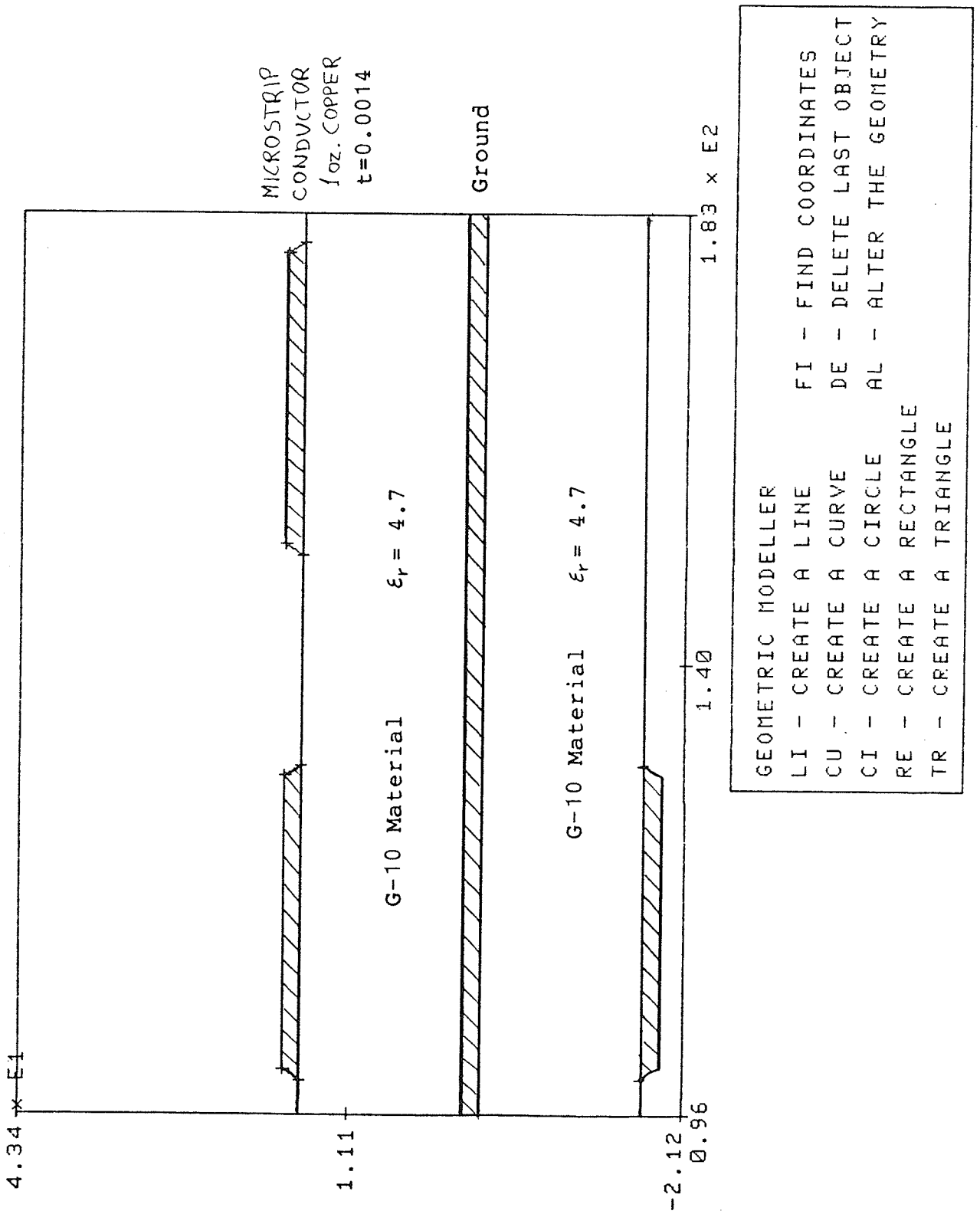


Figure 8.24: Cross-section of the designed PCB. The board for measurements of vias and corners.

Table 8.1: Interconnection lengths for common logic families. From: [Royl88].

TABLE 1—UNTERMINATED INTERCONNECTION LENGTHS FOR COMMON LOGIC FAMILIES

LOGIC FAMILY	PUBLISHED RISE OR FALL TIME (10% TO 100%) (nSEC)	EQUIVALENT t_R MAX (0% TO 100%) (nSEC)	MAX INTERCONNECTION	
			$t_R/\tau=4$	$t_R/\tau=3$
ECL 100K	1	1.25	2.1 IN.	3 IN.
ECL 10K	3.5	4.4	7.5 IN.	10 IN.
ECL 10KH	1.8	2.3	3.9 IN.	5.5 IN.
TTL	4	5	9 IN.	12 IN.
STTL	1.6	2	4 IN.	4.8 IN.
LTTL	4	5	9 IN.	12 IN.
LSTTL	6	8	14 IN.	19 IN.
AS	1	1.3	2.3 IN.	3.1 IN.
ALS	6	7.5	14 IN.	18 IN.
FAST	2	3	5.5 IN.	7.2 IN.
CMOS (5V)	90	113	17 FT	23 FT
CMOS (15V)	50	63	9 FT	13 FT
HIGH SPEED CMOS	10	12.5	23 IN.	30 IN.
FACT	3	3.8	6.5 IN.	9.1 IN.
HC (MOTOROLA)	8	10	17 IN.	24 IN.
AC (TI)	2.4	3	5.1 IN.	7.2 IN.

NOTE:
SEMICONDUCTOR MANUFACTURERS PUBLISH RISE-TIME INFORMATION ON ALL CURRENT LOGIC FAMILIES. THEY NORMALLY SPECIFY THESE RISE TIMES BETWEEN THE 10% AND 90% OR THE 20% AND 80% AMPLITUDE POINTS. YOU MULTIPLY THESE FIGURES BY 1.25 AND 1.67, RESPECTIVELY, TO OBTAIN THE LINEAR-RAMP DURATION FROM 0% TO 100% AMPLITUDE.

type miniature microwave connectors mounted directly on the board under test, and high quality coaxial cables connecting to the measurement instruments. This would prevent before distorsions caused by unmatched connectors and cables. It is recommended that the surface mount components and technology should be applied.

The printed circuit board should have some lines designed for measuring the characteristic impedance and time propagation delay of the lines used. The board should also have some lines designed for measuring the vias and crossovers. The author performed many simulations for different PCBs transmission lines and the use of lines with the characteristic impedance equal 60 Ω is recommended. This is a resonable compromise between different constraints.

The PCB transmission line parameters can be next found by using Greenfield and circuit analysis performed by Phyllis and Spice. A lot of work will be required to model the semiconductor devices which are highly complicated and are strongly depending upon the technology. The device modelling is the most important thing for successful simulation. The Spice program is necessary for any nonlinear devices to be simulated. And all practical semiconductor devices are nonlinear.

The prototype PCB should be designed, manufactured, and tested. The signals produced by high–speed devices driving transmision lines should be measured. The same PCB should be simulated and the same signals obtained. This should verify the accuracy of the simulation software.

8.5 Conclusions

Good performance in high–speed PCBs may be obtained by proper design of PCB interconnections. This issue includes controlled characteristic impedance, time delays, crosstalk, reflections and terminations. The simulation tools discussed assist one to predict high–speed phenomena and to design PCB interconnections.

This thesis describes how the time delays, crosstalk and reflections may be simulated and measured. The crosstalk issue is very important because the crosstalk is always coupled and produces false signals. Its amplitude must be controlled. Reflections may cause signal distortion and false switching and therefore they should be controlled. It may be achieved by simulation to determine when the proper terminations are necessary.

Greenfield is capable of simulating the PCB interconnections and producing accurate results of time–domain circuit analysis. The field simulation is used to create very accurate equivalent models of PCB traces and interconnections. The models are used for simulations of the measurement setups.

Measured results for several configurations and terminations are compared with corresponding simulation results. The results are used for verification of sim-

ulations. Measurements and simulations of time delays, characteristic impedances, crosstalk and reflections give similar results.

The simulated and measured time delays and amplitudes of input and output signals are exactly the same. The accuracy of the simulation may be checked very accurately by comparing the simulated and measured crosstalk which has rather small amplitude and therefore the difference will be more distinct and the error more probable.

The simulation results are very similar to those obtained from measurements. The time delays, amplitudes and shapes of signals are correct. The time simulation results are very accurate and the accuracy is better than 10 % , and typically it is about 5 %. However, the simulated amplitude of crosstalk is bigger than the measured amplitude by about 20 % to 40 %.

One possible explanation is that the sharp impulses of crosstalk were partially attenuated by the measurement system due to a limited bandwidth. It could be also explained by the fact that the simulated amplitudes of crosstalk strongly depend on the model used to represent the actual measurement setup and the model used was not perfect. It is very important how the connectors and terminations are modelled. They should be modelled as accurate as possible.

It is possible to create more complicated equivalent schematic model and obtain closer approximation but even the most sophisticated one will have very restricted application. The approach implemented here was to obtain the best results while modelling the merit of the system. It is important that the simulations and measurements give very similar results.

The closest approximation was obtained for modelling of connectors with terminations by 50 Ω resistance and capacitance between 1 pF and 5 pF in parallel. The equivalent capacitance should be between 1 pF and 5 pF. Bigger capacitance, for instance 10 pF, caused bigger differences between simulated and measured amplitude results.

Measurements and simulations of corners on PCB traces show that the influence of corners is very small and negligible for the range of up to 3 GHz. No difference between corner of 90 degrees and corner of 45 degrees was observed.

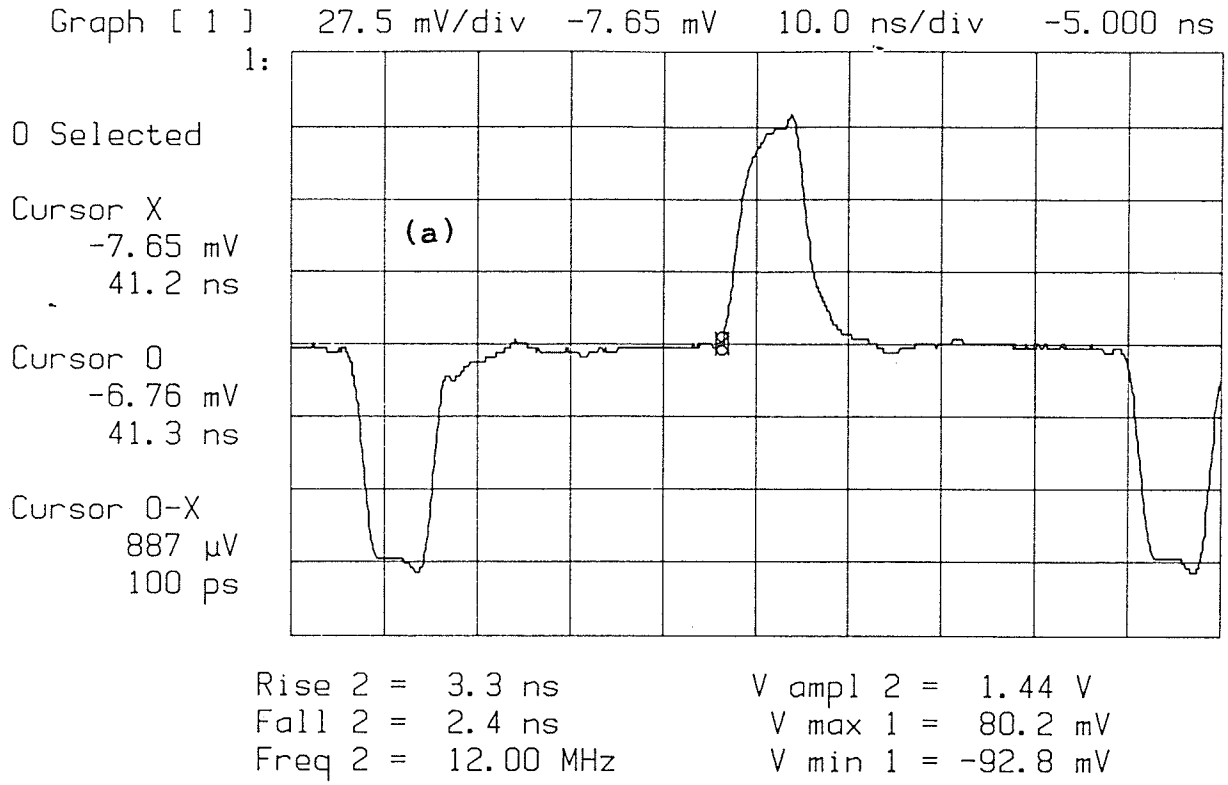
It should be noted that the simulation gives a lot of information at once — all signals may be displayed simultaneously, while each measurement requires a specific setup of cable connections.

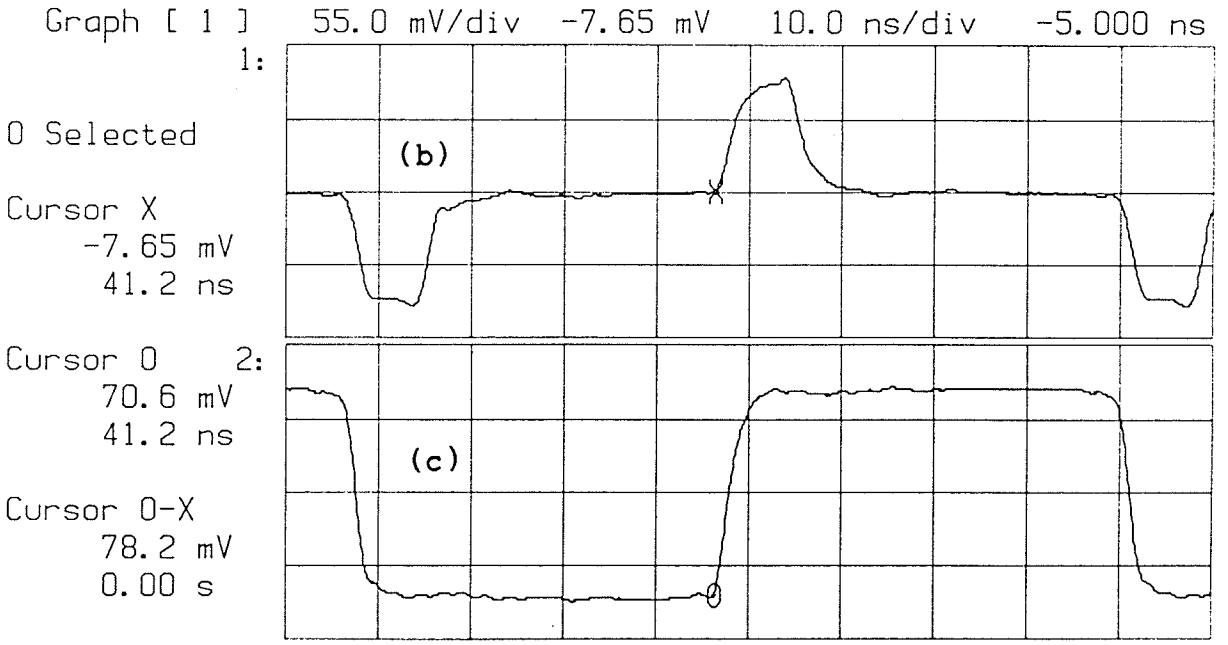
APPENDIX A

DIGITIZING OSCILLOSCOPE MEASUREMENTS

This appendix presents measurement results for oscilloscope setup for several other termination configurations.

Content of Appendix A





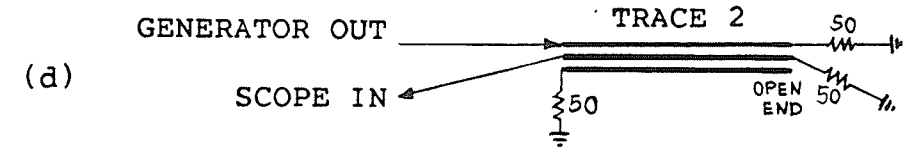


Figure A.1: Backward crosstalk and input signal — one end of Trace 2c floating. All traces are terminated with 50 Ω, except one end of Trace 2c floating: (a) backward crosstalk from Trace 2b in detail; (b) backward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.

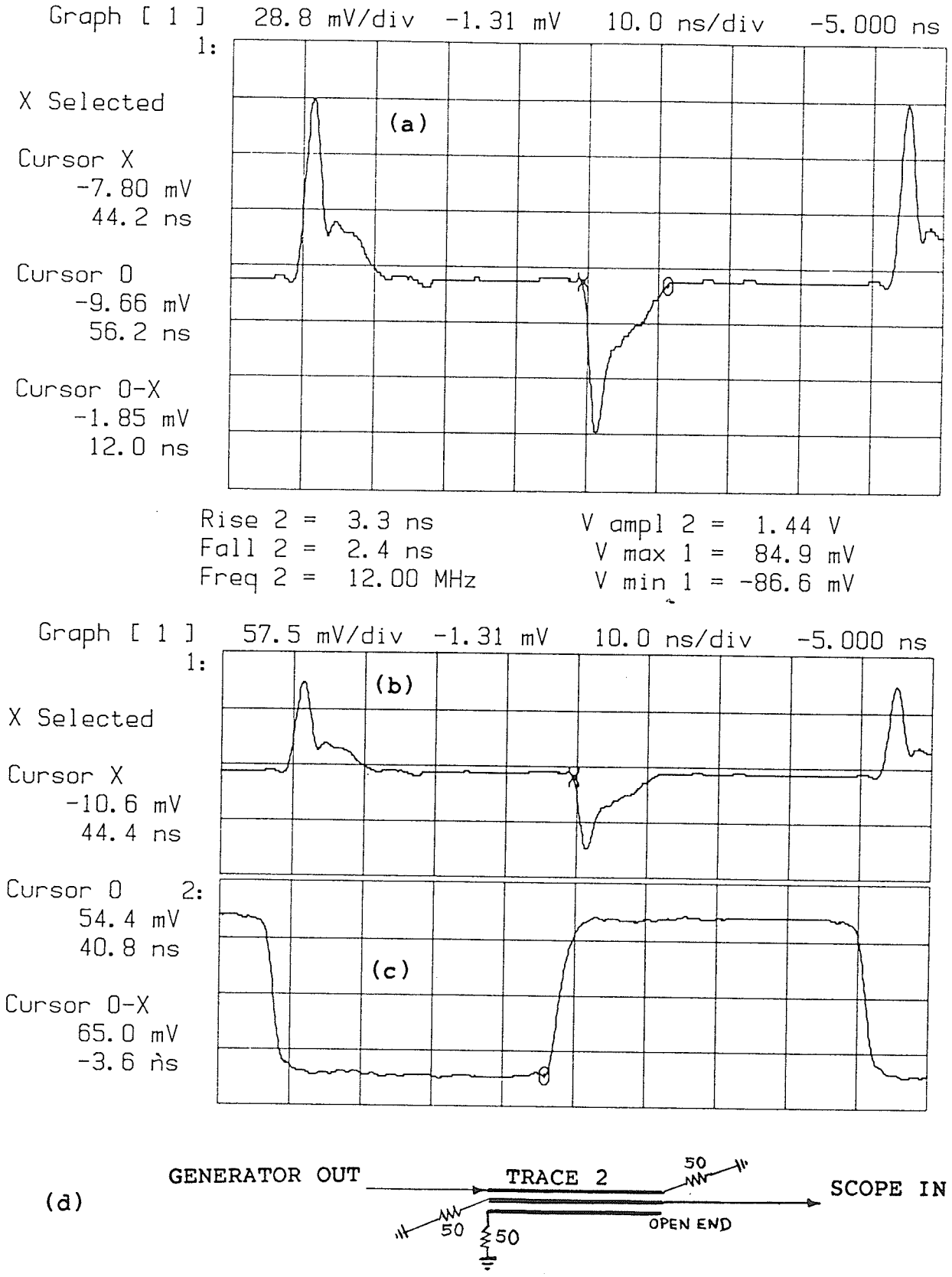
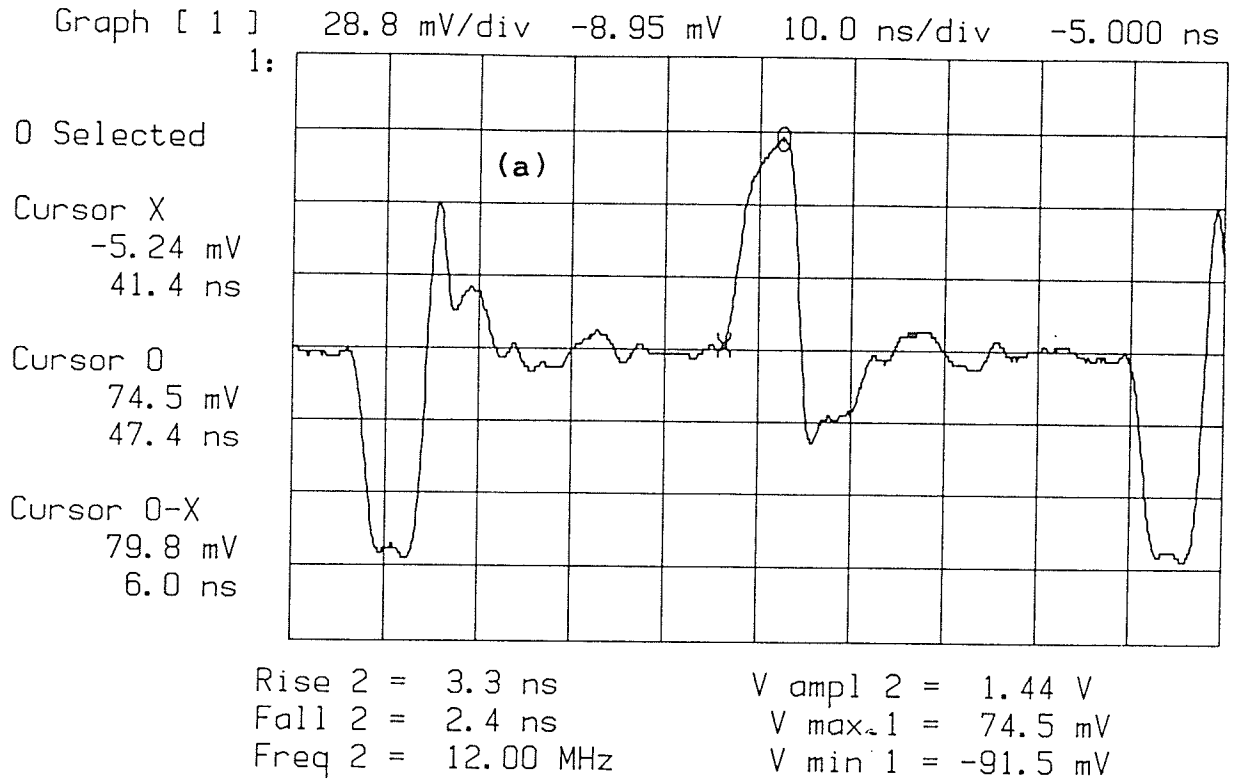


Figure A.2: Forward crosstalk and input signal — one end of Trace 2c floating. All traces are terminated with 50 Ω, except one end of Trace 2c floating: (a) forward crosstalk from Trace 2b in detail; (b) forward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.



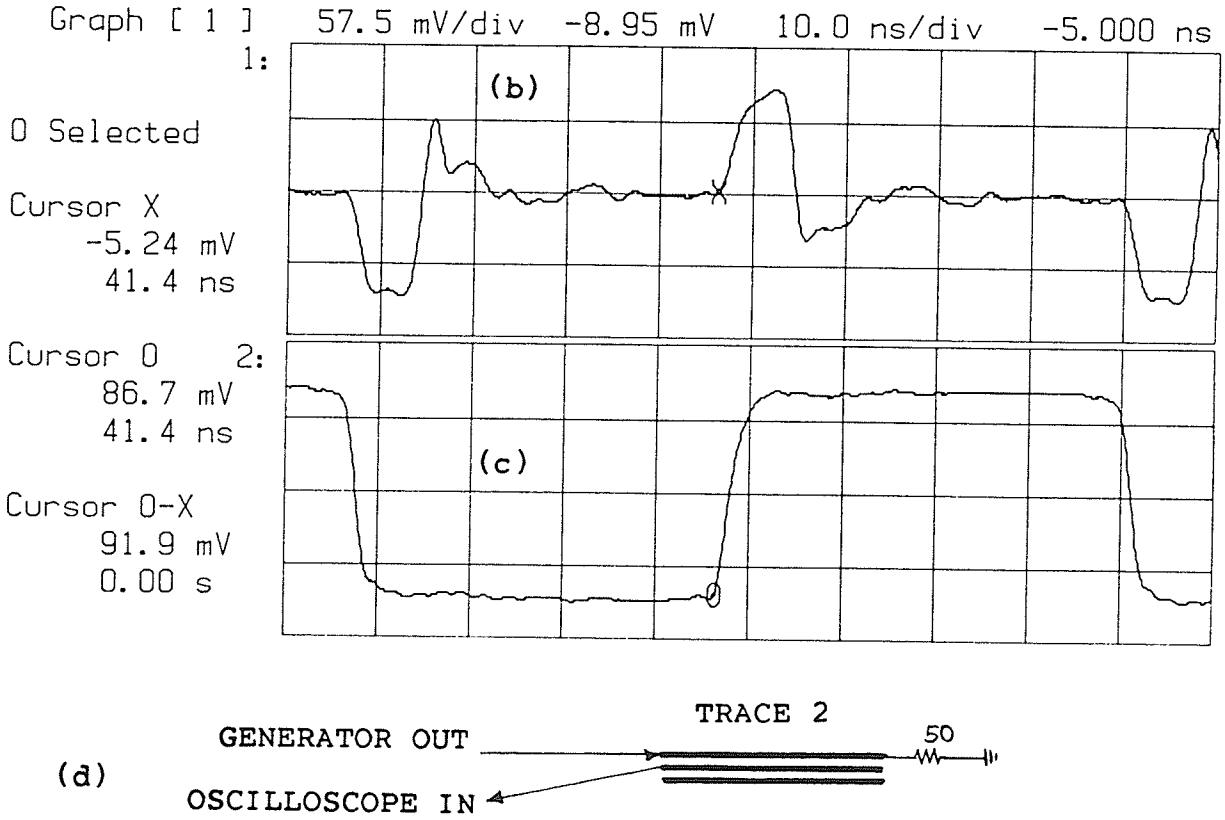
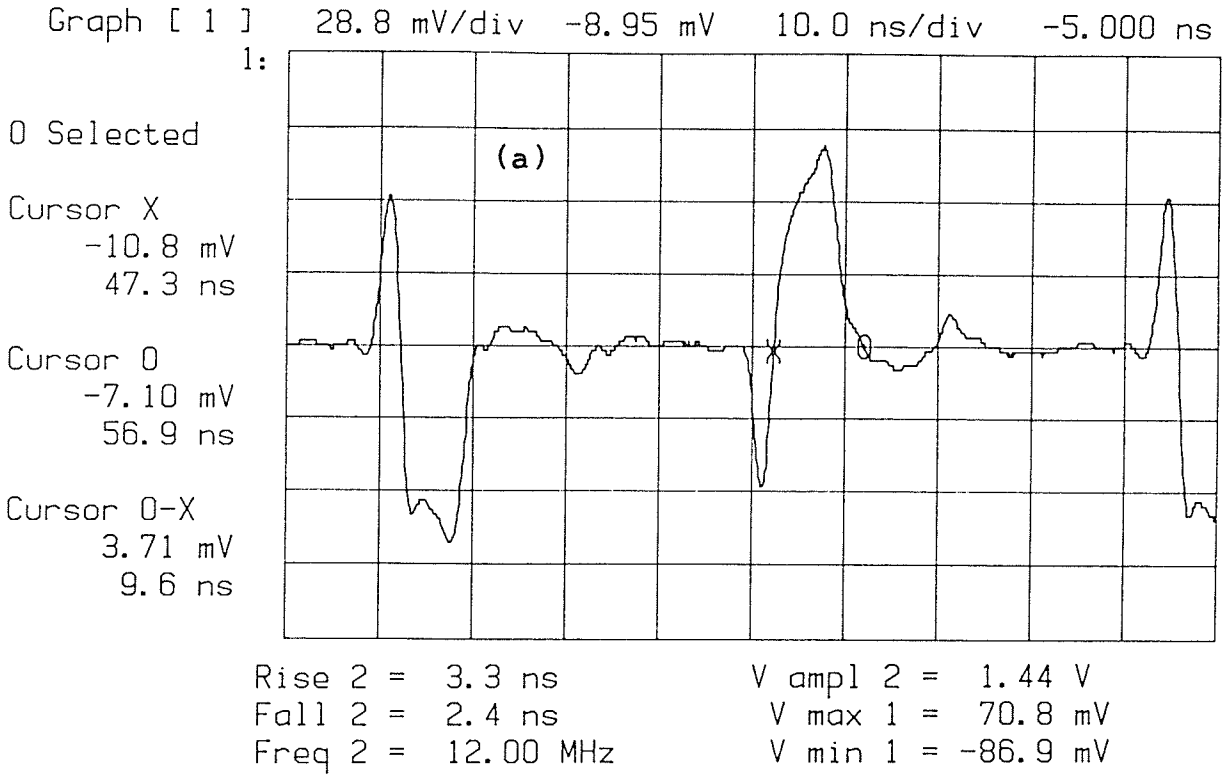
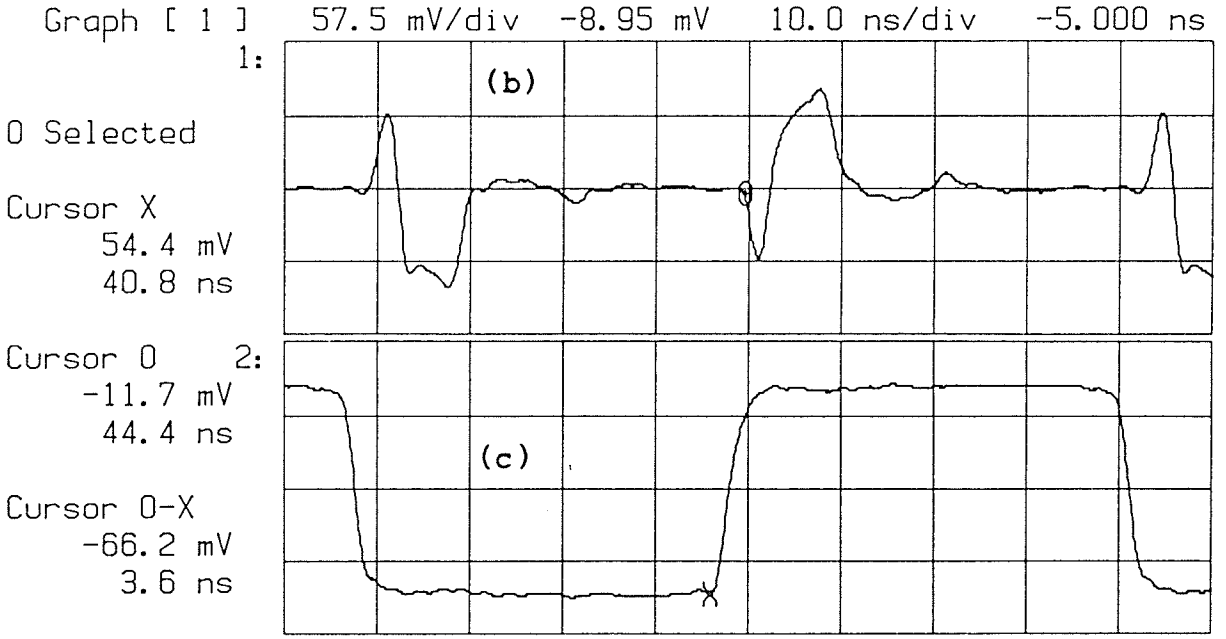


Figure A.3: Backward crosstalk and input signal — three ends are floating. With Trace 2a and one end of Trace 2b terminated with 50 Ω, and other ends floating: (a) backward crosstalk from Trace 2b in detail; (b) backward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.





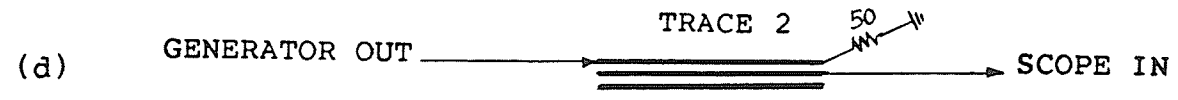


Figure A.4: Forward crosstalk and input signal — three ends are floating. With Trace 2a and one end of Trace 2b terminated with 50 Ω, and other ends floating: (a) backward crosstalk from Trace 2b in detail; (b) backward crosstalk from Trace 2b in time comparison with input signal (c); and (d) measurement setup.

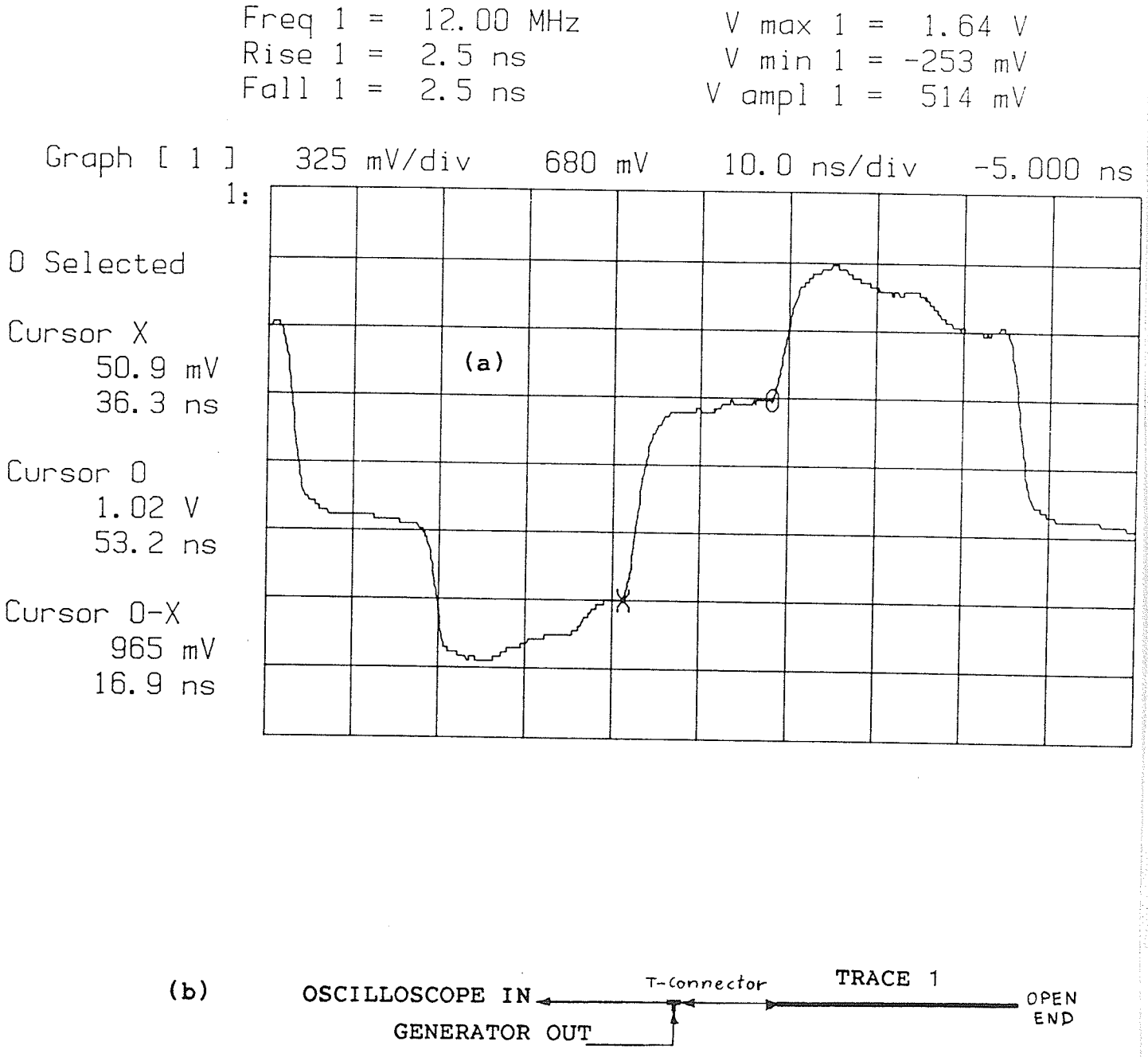


Figure A.5: Input signal in Trace 1 reflected by the other floating end. The signal is delayed by the coaxial cables and the reflections are bouncing causing ringing.

APPENDIX B

RESULTS OF SIMULATIONS FOR OSCILLOSCOPE SETUP

This appendix presents simulation results for oscilloscope setup for several other termination configurations.

Content of Appendix B

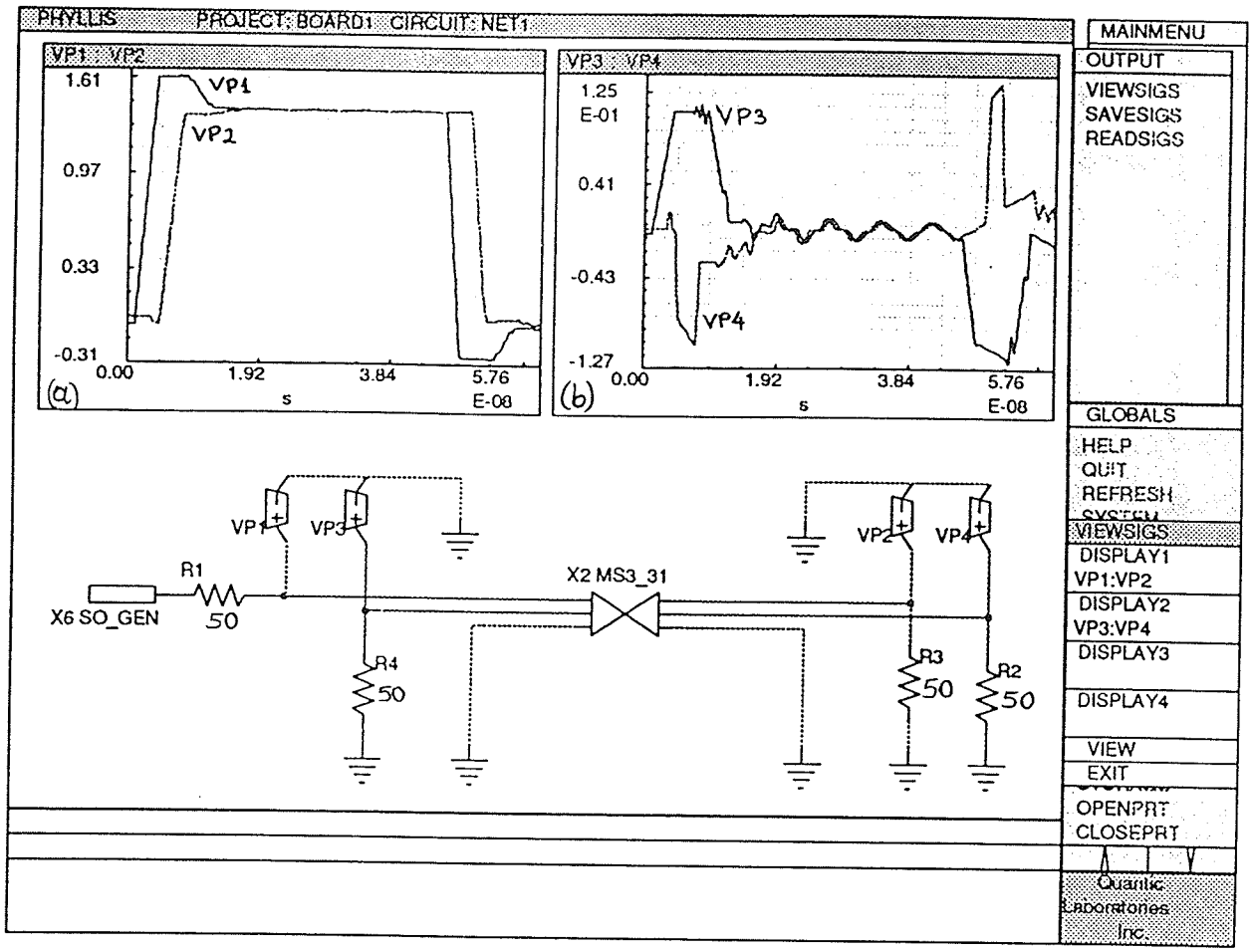


Figure B.1: Simulation of three microstrips — third trace grounded. First and second trace terminated with 50 Ω and third trace grounded: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a — both with reflections; and (b) backward (VP3) and forward (VP4) crostalk in Trace 2b.

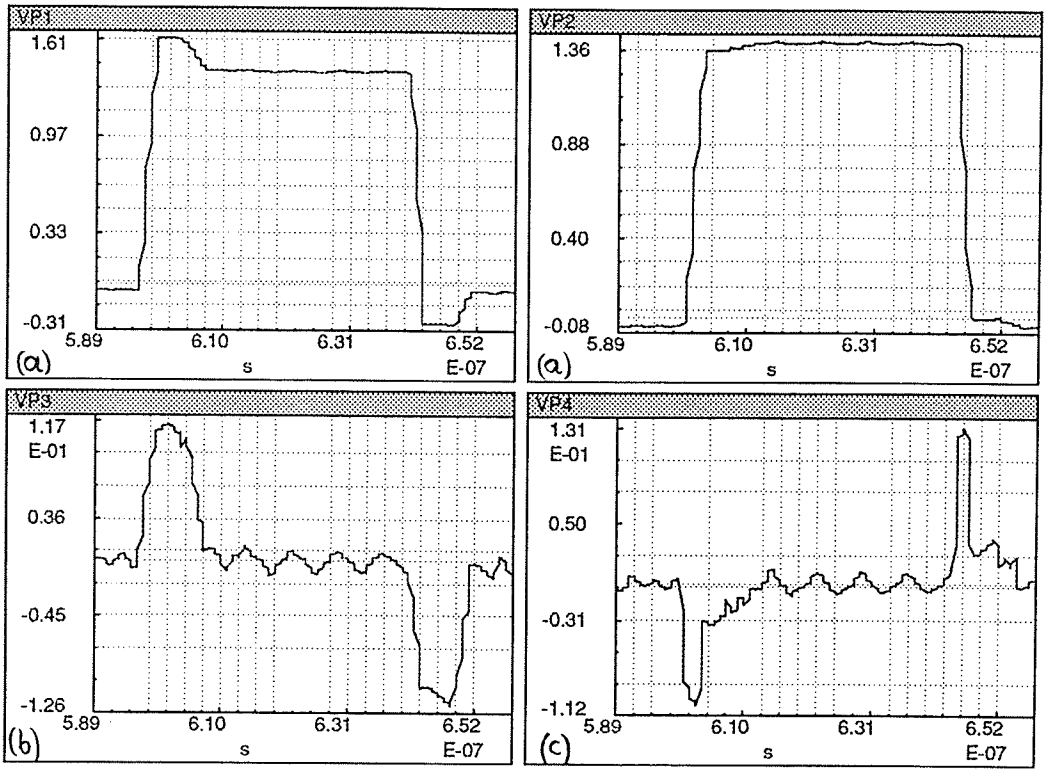


Figure B.2: Simulation of three microstrips — third trace grounded. For first and second trace terminated with 50 Ω, and third trace grounded (schematic is the same as in Fig.B.1): (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a — both with reflections; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) backward (VP3) and forward crosstalk (VP4) in Trace 2b.

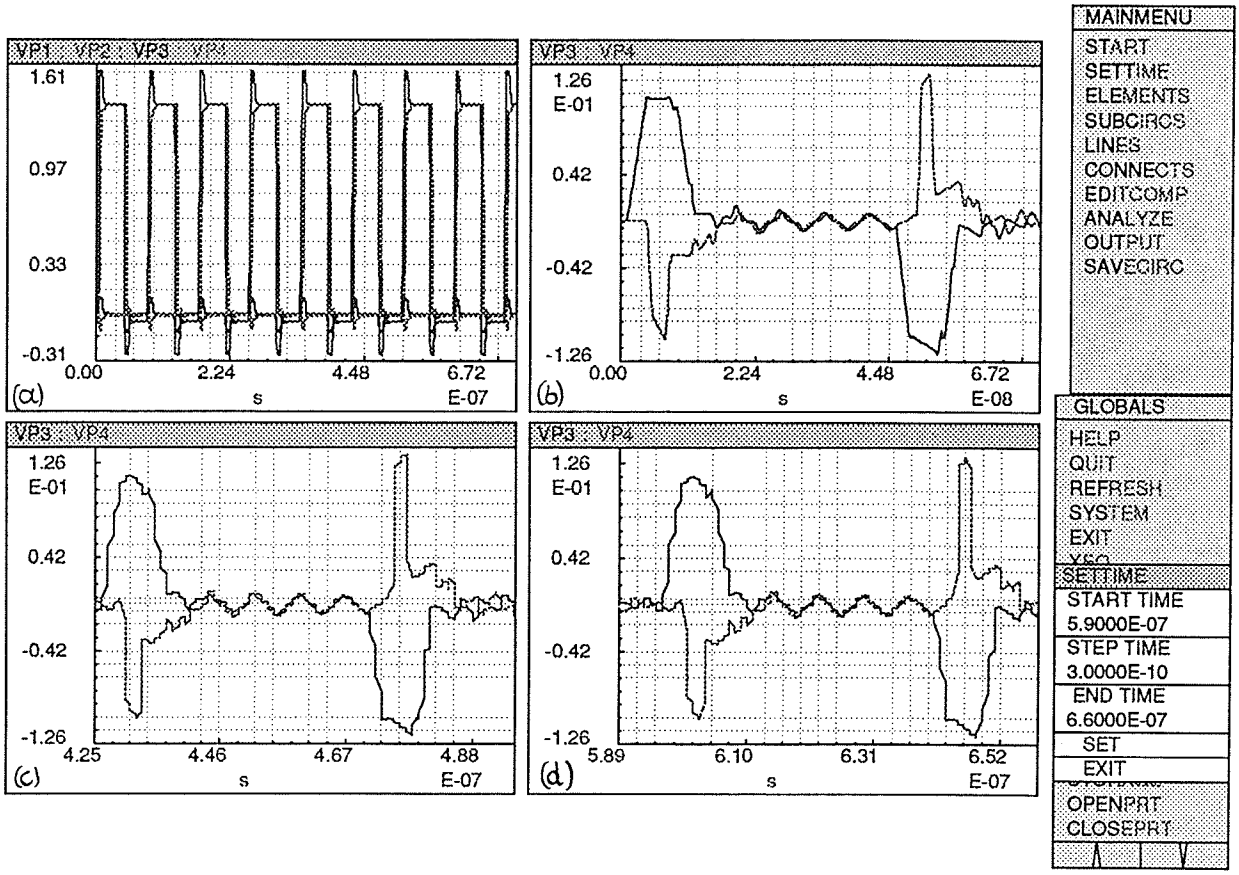


Figure B.3: The creation of steady state signals. Results of simulation with first and second trace terminated with 50 Ω and third trace grounded. The schematic is the same as in Fig.B.1. The shape of signals changes because of reflections bouncing in the transmission–line: (a) ten cycles of input and output signals from the first trace; (b) backward and forward crosstalks (VP3,VP4) from the second trace caused by the first pulse cycle; (c) backward and forward crosstalks (VP3,VP4) after five cycles; and (d) backward and forward crosstalks (VP3,VP4) after nine cycles.

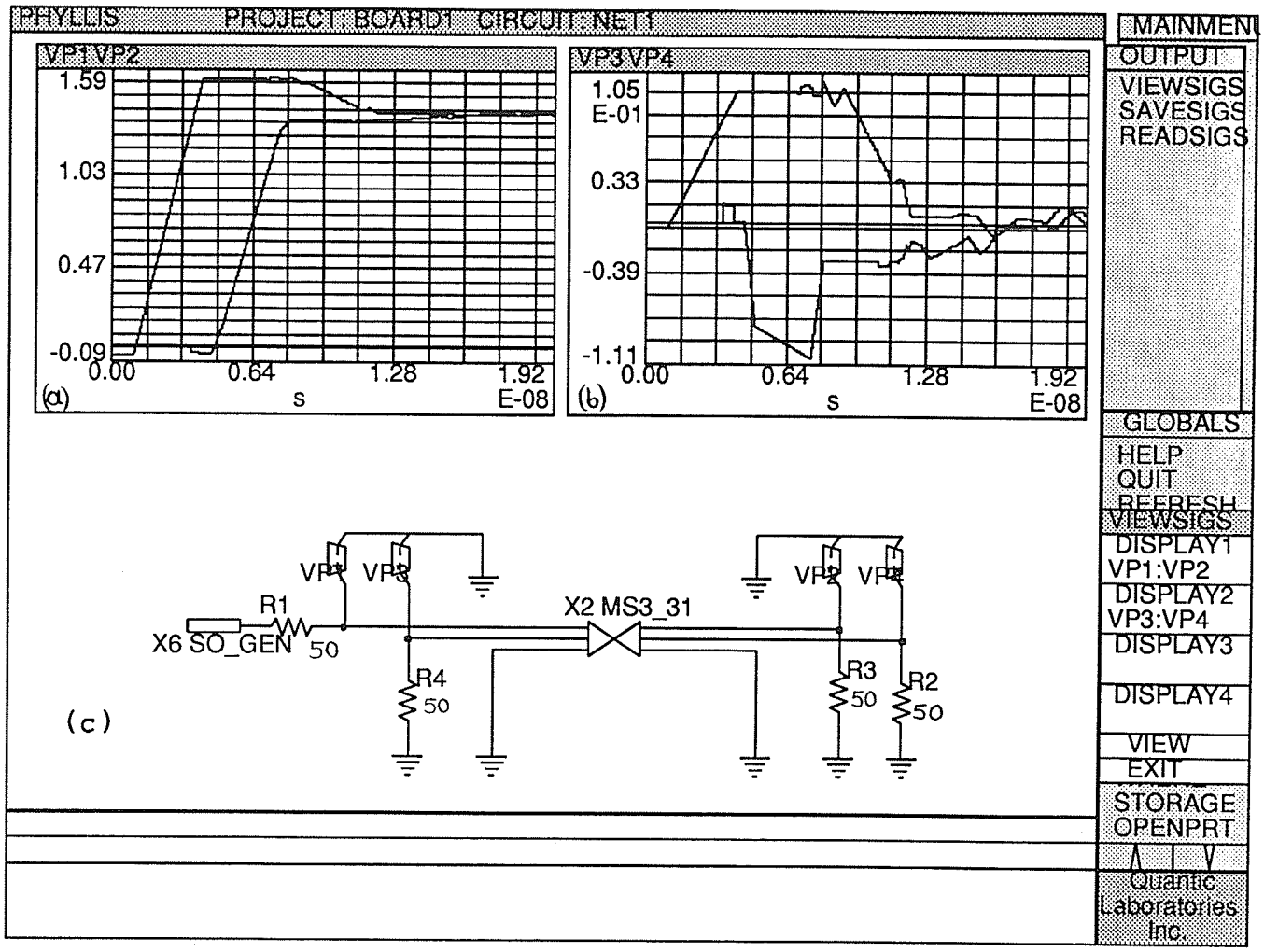


Figure B.4: Signals caused by rise time edge of first pulse of input signal. Results of simulation with first and second trace terminated with 50 Ω and third trace grounded: (a) input (VP1) and output signal (VP2) in Trace 2a; (b) backward crosstalk (VP3) and forward crosstalk (VP4) from Trace 2b; and (c) the schematic with generator, probes, transmission–line and resistors (all equal 50 Ω).

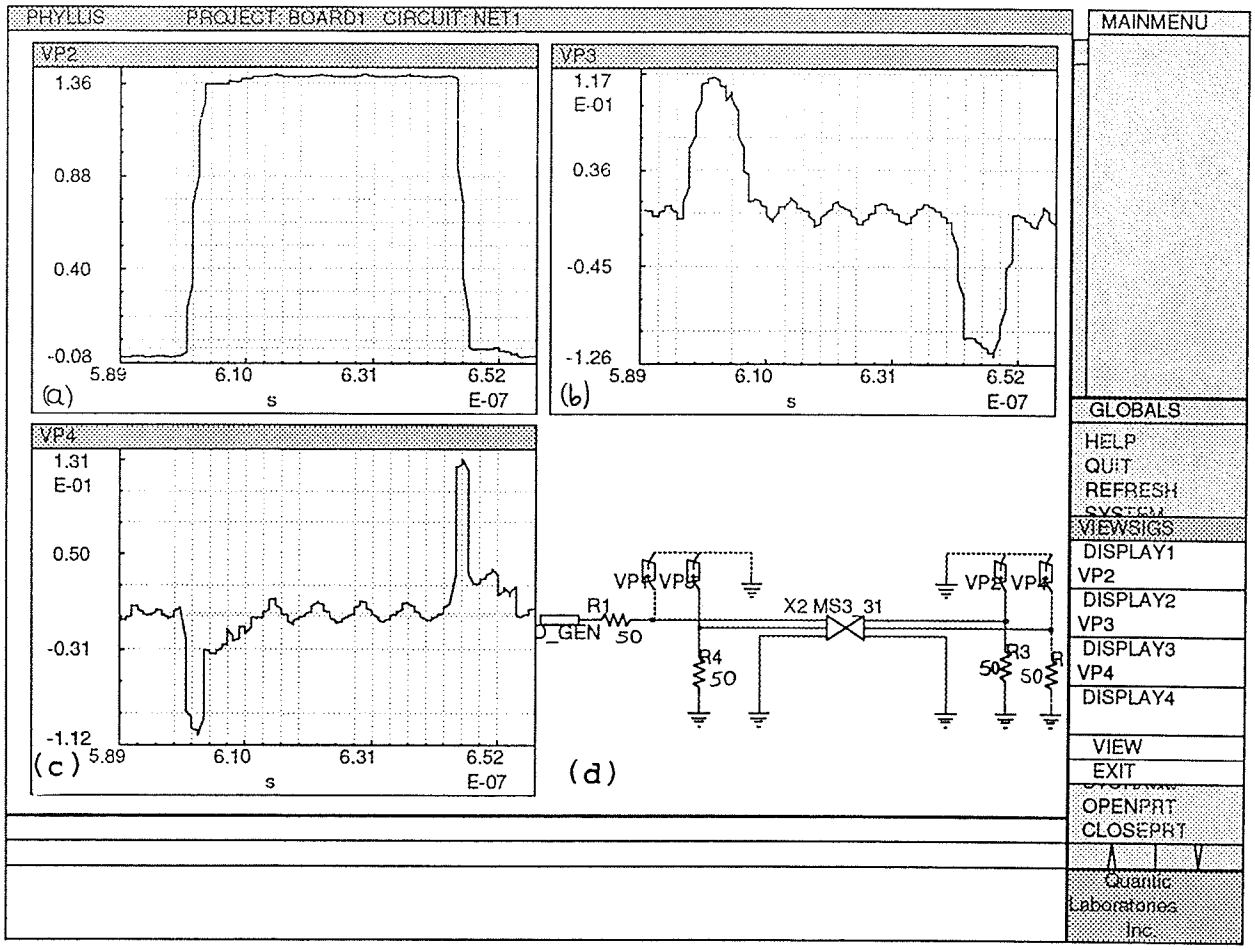


Figure B.5: Steady state signals in three parallel microstrips. Results of simulation with first and second trace terminated with 50 Ω and third trace grounded: (a) input signal in Trace 2a; (b) output signal (VP2) from Trace 2a; (c) backward crosstalk (VP3) from Trace 2b; (c) forward crosstalk (VP4) from Trace 2b; and (d) the schematic with generator, probes, transmission–line and resistors (all equal 50 Ω).

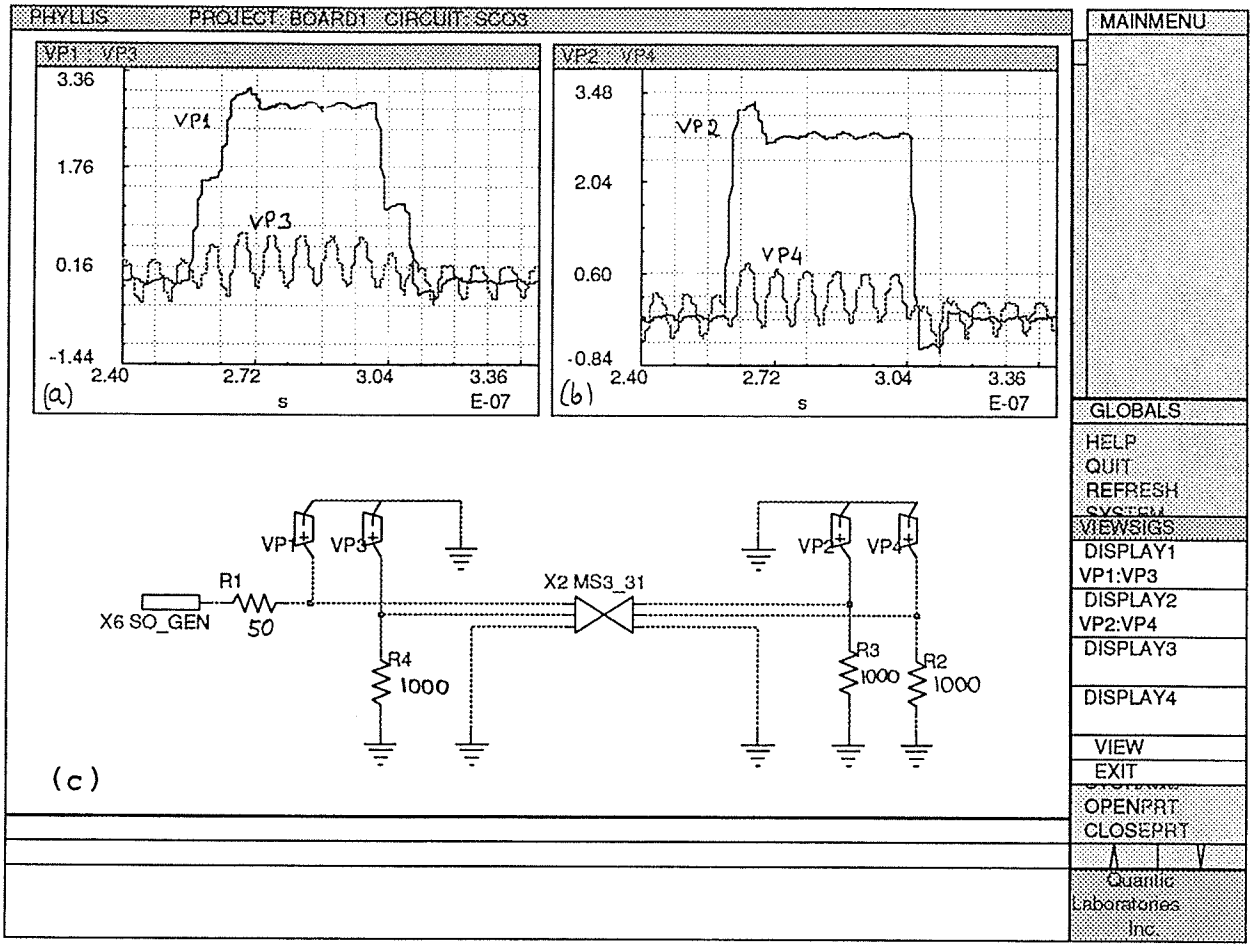


Figure B.6: Results of simulation for 1000 Ω termination. First and second traces terminated with 1000 Ω causing big mismatch and reflections, and third trace grounded: (a) distorted input signal (VP1) by reflections, and backward crosstalk (VP3) with big oscillations; (b) output signal (VP2) with big overshoot, and forward crosstalk (VP4) with big oscillations; (c) schematic.

APPENDIX C

TDR SETUP SIMULATIONS AND MEASUREMENTS

This appendix presents measurement and simulation results for TDR setup for several other termination configurations.

Content of Appendix C

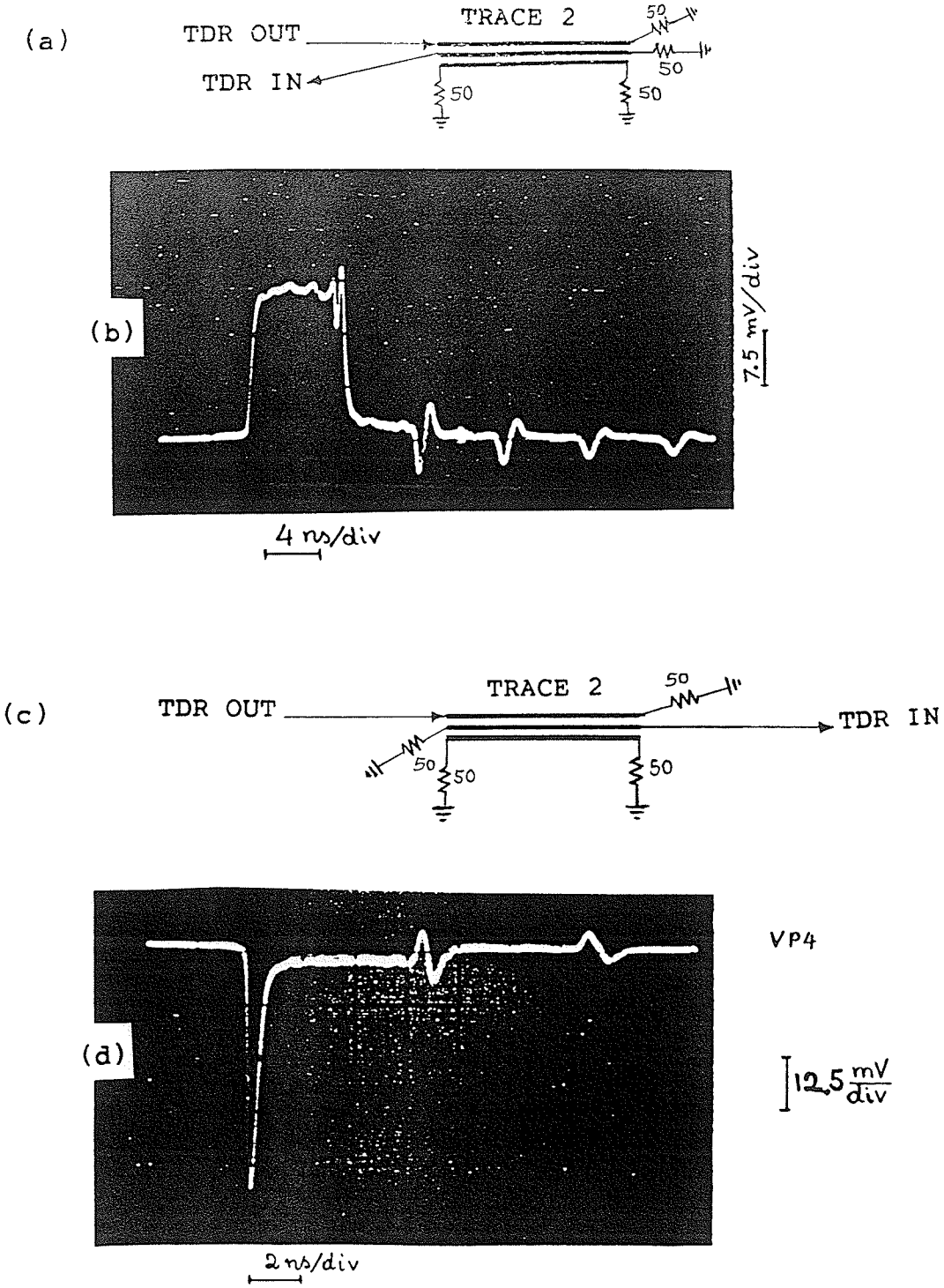


Figure C.1: Measured backward and forward crosstalk — third trace grounded. (a) measurement TDR setup; (b) backward crosstalk in Trace 2b coupled from Trace 2a of three parallel microstrips; (c) measurement TDR setup; and (d) forward crosstalk in Trace 2b coupled from Trace 2a of three parallel microstrips. Source: own.

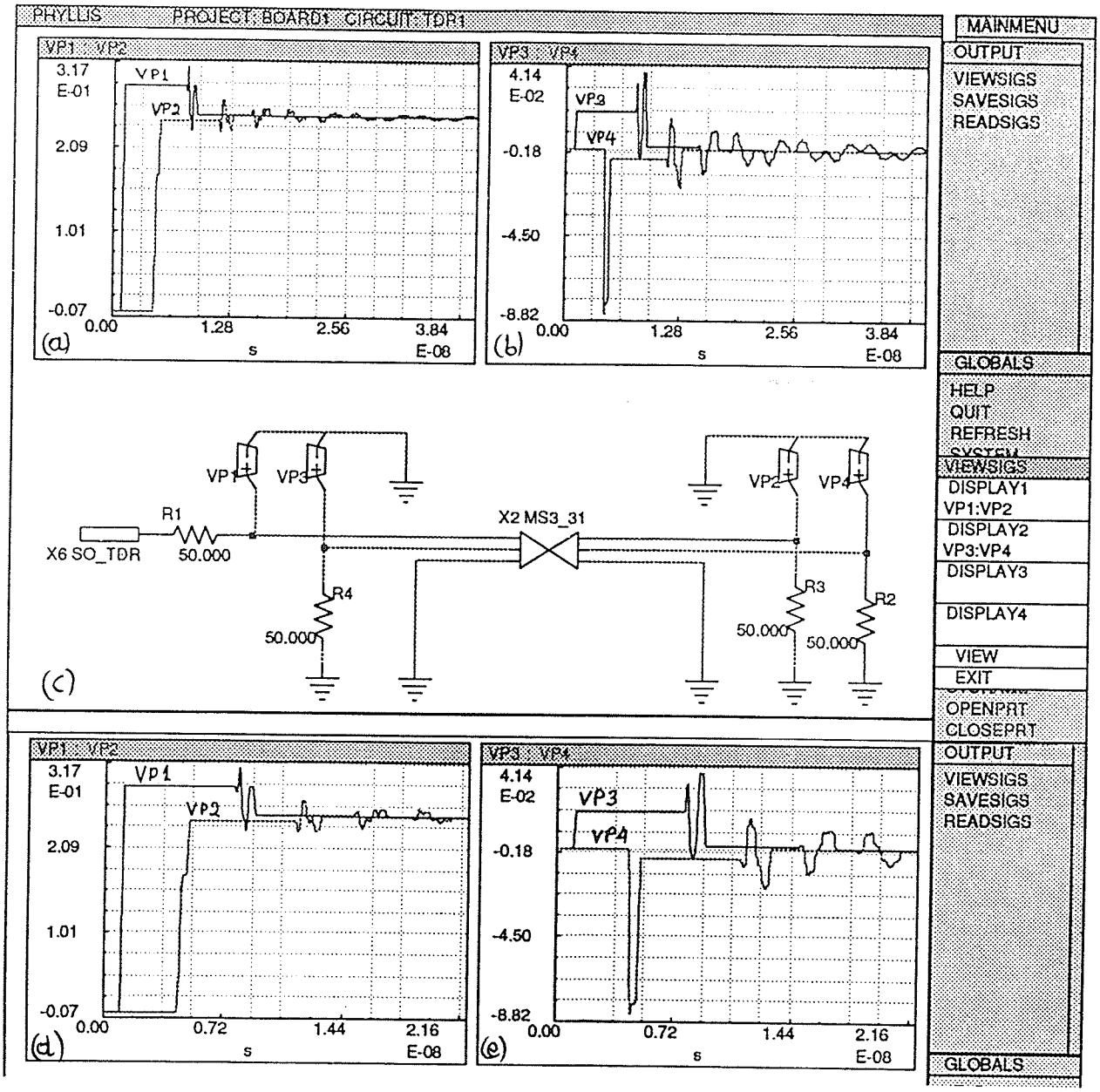


Figure C.2: Simulation with third trace grounded. Trace 2a and Trace 2b terminated with pure resistor 50 Ω and **third trace grounded**: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b: (c) schematic; (d) same as (a) but enhanced; and (e) same as (b) but enhanced.

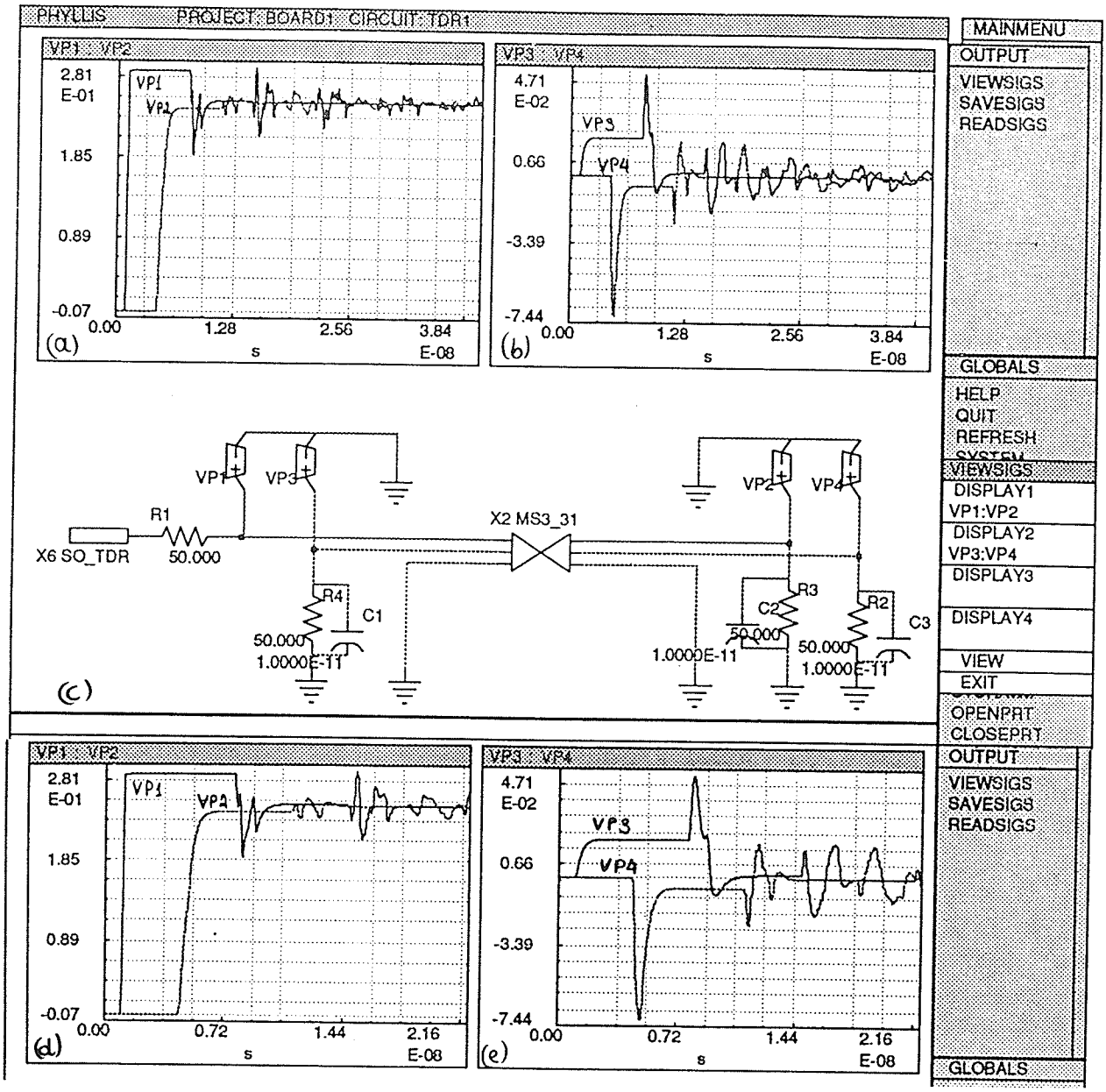


Figure C.3: Simulation with third trace grounded. Terminations modeled as 50 Ω resistance and **10 pF** capacitance in parallel: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) same as (a) but enhanced; and (e) same as (b) but enhanced.

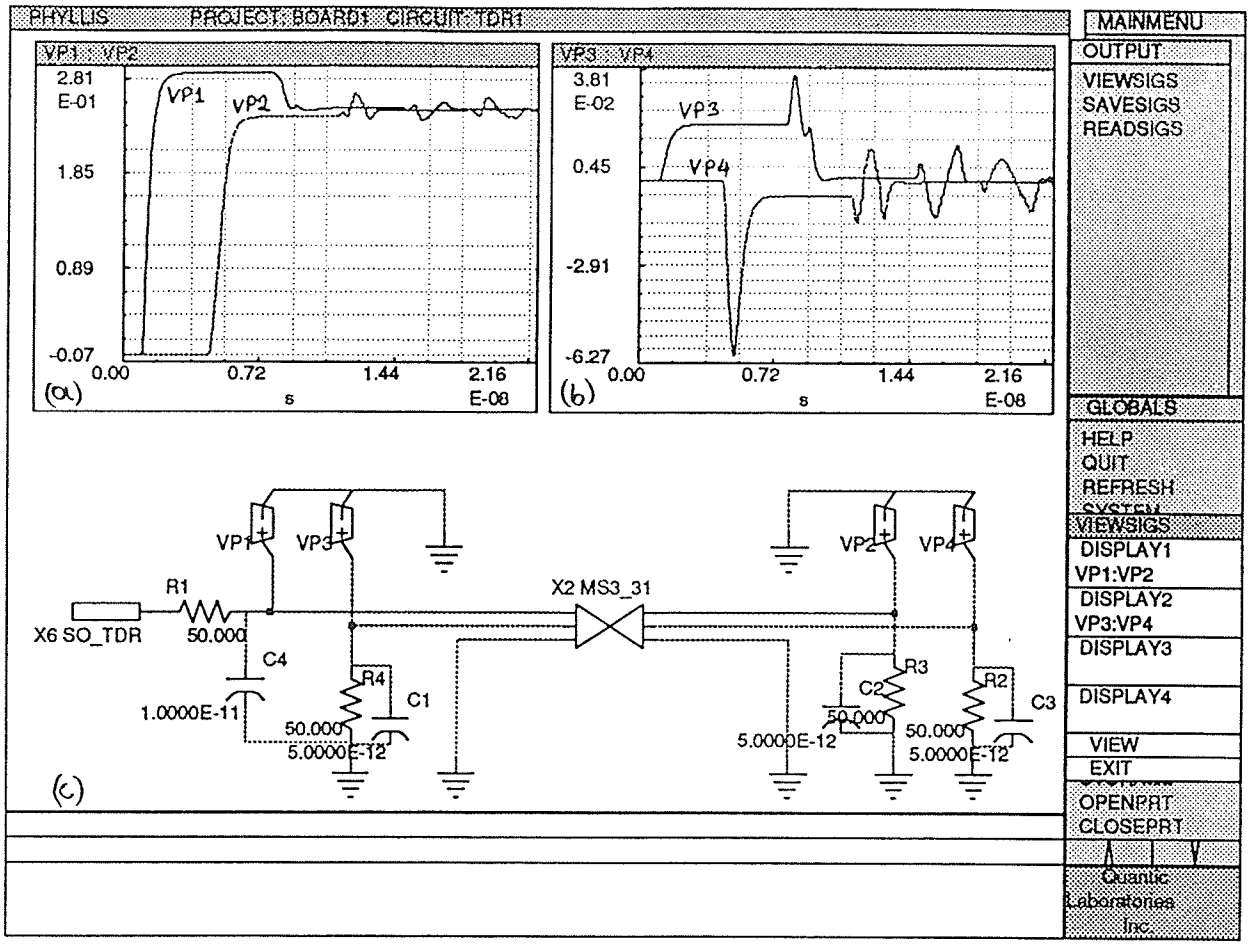


Figure C.4: Simulation results — third trace grounded. Terminations modeled as 50 Ω resistance and **5 pF** capacitance in parallel, and the input connector modeled as **10 pF**: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; and (c) schematic.

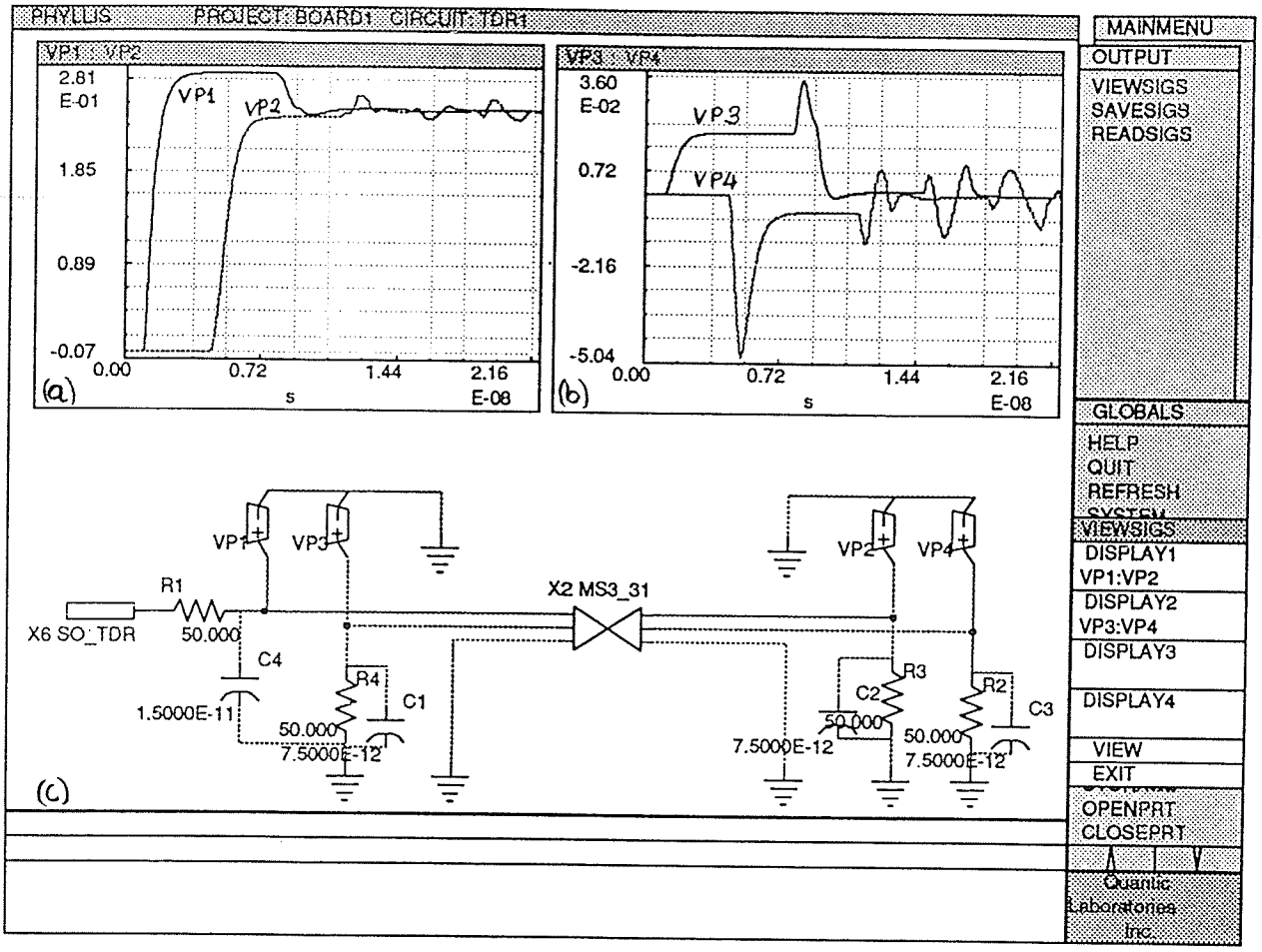


Figure C.5: Simulation results — third trace grounded. The terminating resistors modeled as 50 Ω resistance and **7.5 pF** capacitance, and the input signal connector modeled as **15 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; and (c) schematic.

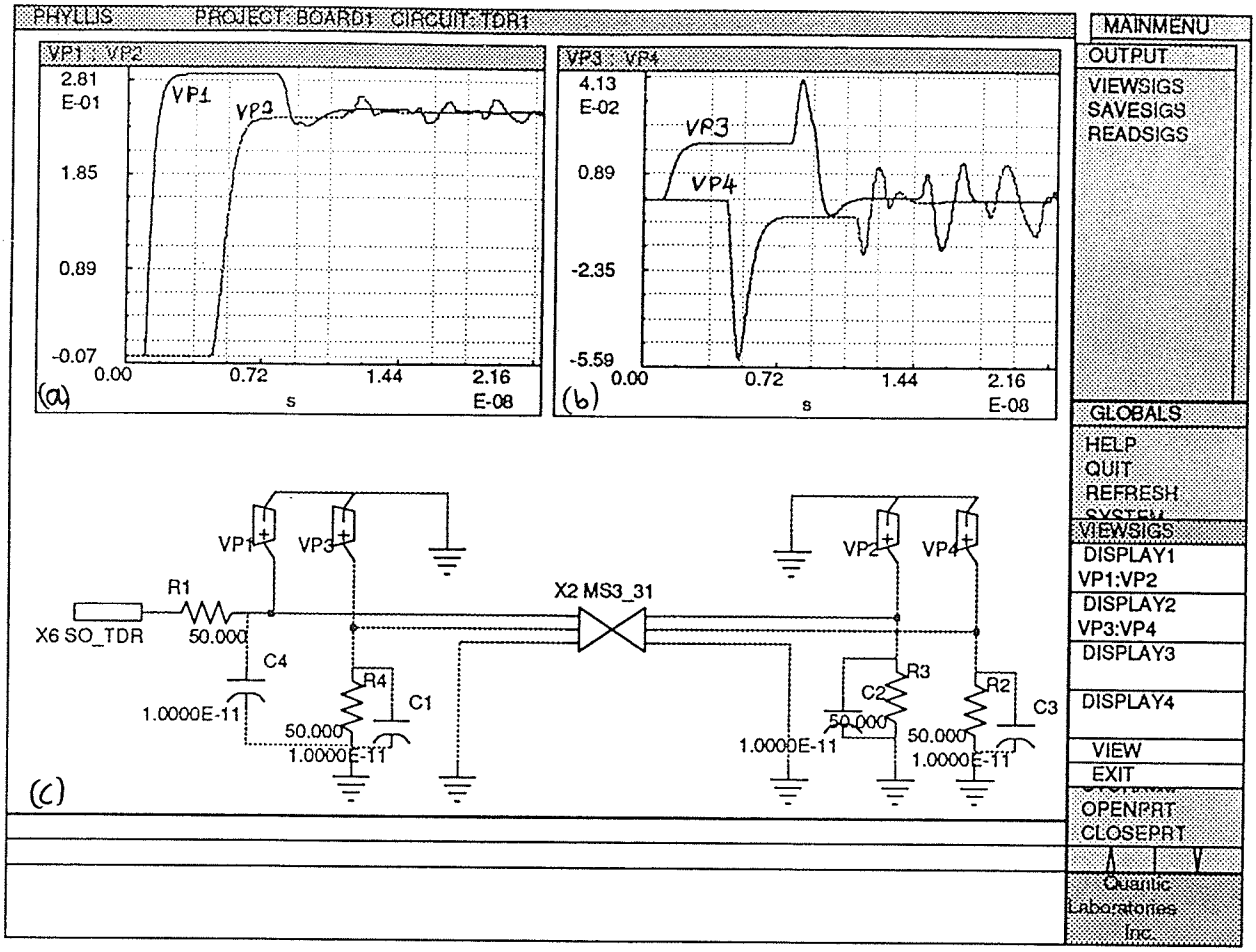
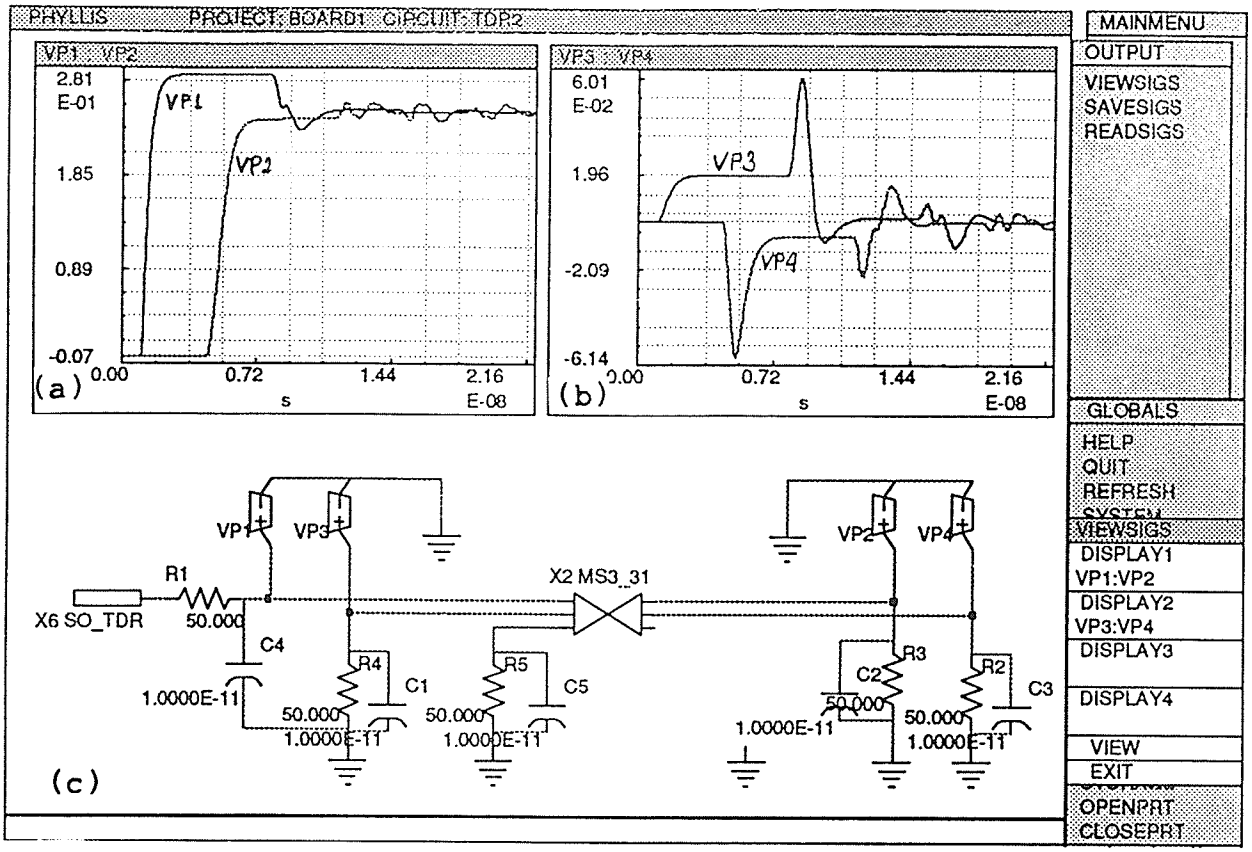


Figure C.6: Simulation of three microstrips — third trace grounded. The terminating resistors modeled as 50 Ω resistance and **10 pF** capacitance, and the input signal connector modeled as **10 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a: (b) backward and forward crosstalks in Trace 2b; and (c) schematic.



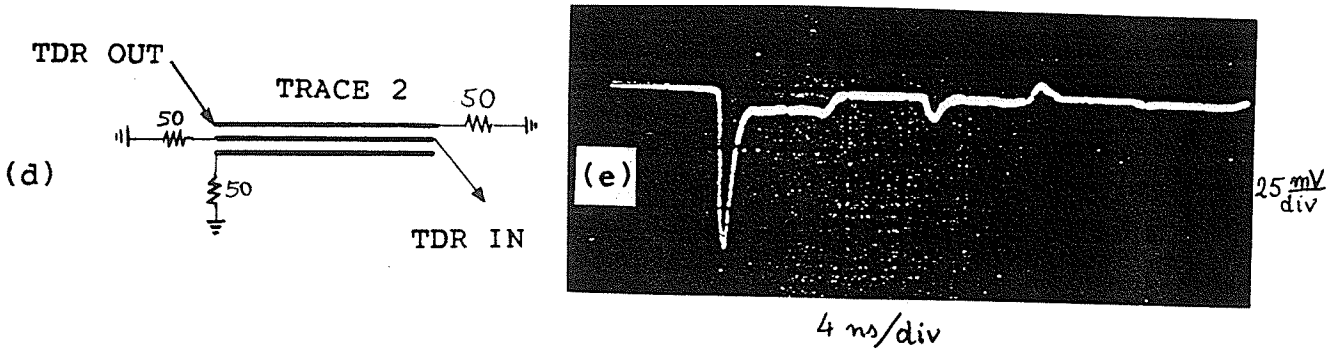


Figure C.7: Comparison of results — one end of third trace floating. The terminating resistors modeled as 50 Ω resistance and **10 pF** capacitance, and the input signal connector modeled as **10 pF** capacitance: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) measurement TDR setup; and (e) measurement of forward crosstalk corresponding to VP4.

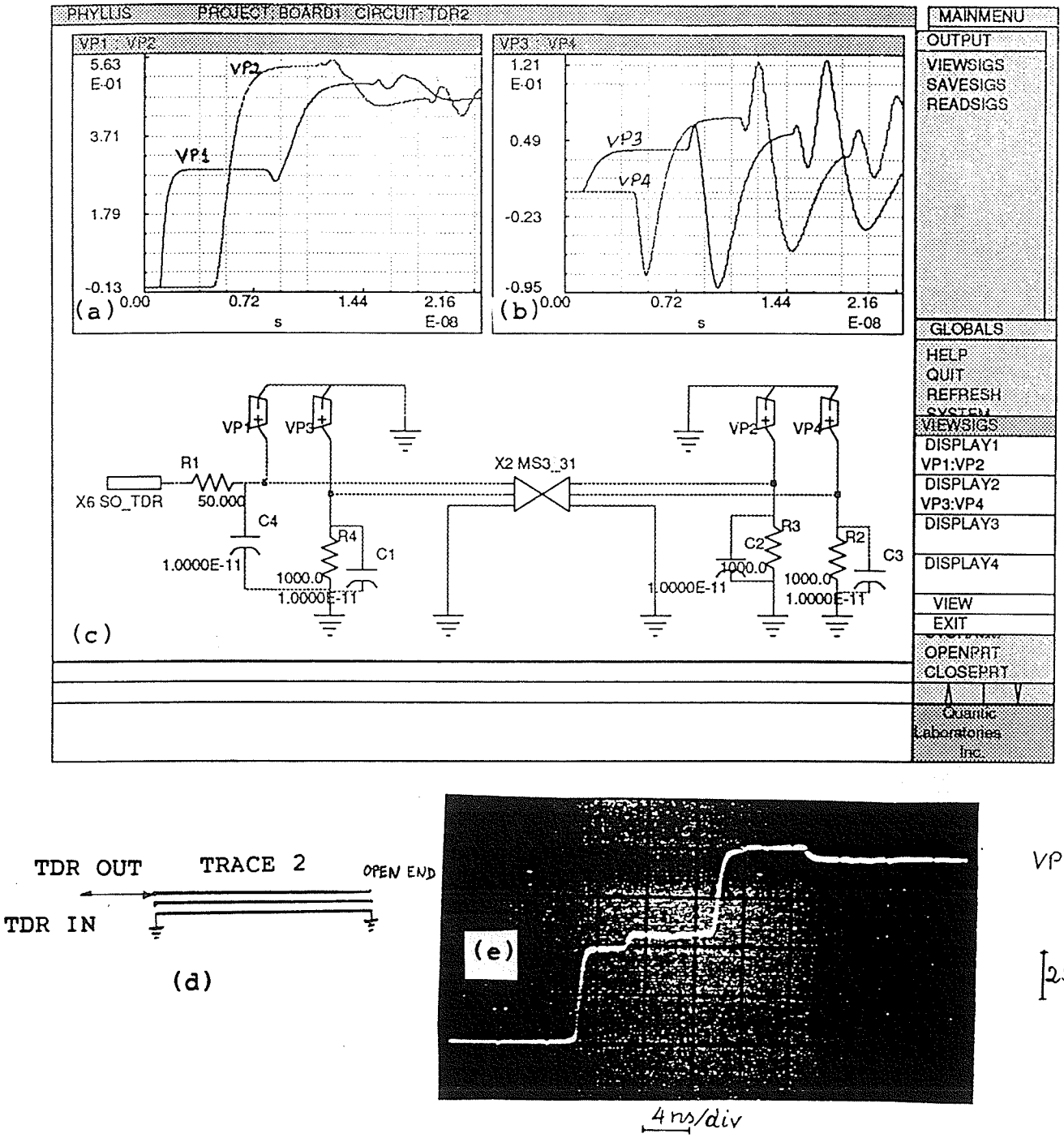


Figure C.8: Results of termination with 1000 Ω. The terminating resistors modeled as 1000 Ω resistance and **10 pF** capacitance, and the input signal connector modeled as **10 pF** capacitance, and third trace grounded: (a) input signal (VP1) and delayed output signal (VP2) in Trace 2a; (b) backward (VP3) and forward (VP4) crosstalks in Trace 2b; (c) schematic; (d) measurement TDR setup; and (e) TDR measurement result corresponding to VP1 — signal is delayed by coaxial cable between TDR and measured trace (4ns).

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