A PRECISION RHYTHM SYNTHESIZER

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George K. Schattschneider

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MASTER OF SCIENCE

ABSTRACT

Rhythm is one of the most important factors that influence the structure of music. However, the precise scientific study of musical rhythm perception thresholds and the hierarchy of rhythm-influencing factors is at present still in its early stages.

One of the reasons for the lack of quantitative knowledge in this field is the fact that until recent years it would have been economically prohibitive to design and build an electronic device with sufficient precision to produce meaningful rhythm experiment results.

This thesis describes an electronic instrument which synthesizes a variable sequence of notes. The frequency, amplitude and duration of these notes can be operator adjusted to produce a wide variety of simple rhythm patterns with great precision. The discussion includes the theory, design and testing of the synthesizing circuitry.

ACKNOWLEDGEMENT

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I INTRODUCTION

1.1 Nature of the Problem

Musical rhythm, an essential element of music, has been with mankind for thousands of years. It is surprising, therefore, to discover that there is very little quantitative knowledge of musical rhythm available.

The following paragraphs are excerpts from a paper entitled "Experiments on the Perception of Rhythm" by C. A. Haenselman of the School of Music of the University of Manitoba. The paper briefly describes the meaning of rhythm, some of the factors which affect rhythm perception, and some of the experimental work which has already been done in an effort to understand rhythm. The excerpts presented below have been edited slightly for direct applicability to the subject matter of this thesis.

> "Experiments done in the area of perception of musical rhythm indicate that there are discrepancies between the objective patterns and the way in which they are perceived. Even where an objective grouping does not occur, the perceiver tends to impose a subjective grouping on a series of regularly recurring pulses. This mode of rhythmic organization and perception is classified as metric rhythm. Metric rhythm is defined as the subjective or objective grouping of regularly recurring events such that an accented event is perceived with one or more unaccented events.
>
> Although it is generally recognized that changes in intensity, duration or pitch can create a perceived metric rhythm, the hierarchy of importance of these factors in perception has not been established. Concerning thresholds at which differences in intensity and duration are perceived, only that of duration has been studied. Another aspect which has not been clarified is the threshold at which sound events are perceived as being separated by silence.

In order to compare the objective sound patterns with the perceived patterns, electronic equipment is being constructed which precisely produces the duration, amplitude and pitch of sound events. With this equipment,a series of experiments can be done which will yield data concerning the perception of rhythmic grouping, the thresholds at which differences in amplitude and duration are detected, and the hierarchial importance of intensity, duration and pitch as determinants in rhythmic grouping."

If it is desired to pursue the subjects of rhythm and rhythm perception to a greater depth than what has been presented here, Appendix A contains a fairly substantial list of pertinent references which were collected by Professor Haenselman.

1.2 Project Description

The purpose of this thesis is to design, construct and test the electronic equipment (rhythm synthesizer) mentioned in section 1.1. The following paragraphs detail the specific requirements of the School of Music with respect to the necessary capabilities of the rhythm synthesizer.

The electronic circuitry which will be used by the School of Music in their rhythm perception experiments is required to generate a series of audible notes. To eliminate as many variables as possible, a "note" is defined as a time-limited block of signal of constant frequency and amplitude. Figure 1.1 illustrates what is meant by a "note".

The circuitry must be designed in such a way that with the appropriate operator manipulation of the frequency, amplitude and duration of the notes, a single stressed beat can be produced on every second, third or fourth note in the sequence. To illustrate this, Figure 1.2 shows three sequences of notes with stressed beats on every

third note. The rhythm influencing factors in the three sequences are, respectively, frequency, amplitude and duration.

All of the variables (frequency, amplitude, duration and notes per minute) should be continuously variable except for the sequency length which should be adjustable to any desired discrete whole number value.

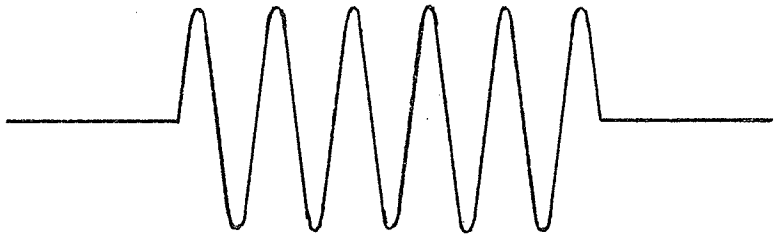
To determine the hierarchy of importance of the rhythm-influencing factors, the circuitry must also be able to generate two simultaneous rhythms. For example, the amplitude of every third note could be different from the preceding two and, at the same time, the duration of every fourth note could be different from the preceding three.

1.3 Basic Design Approach

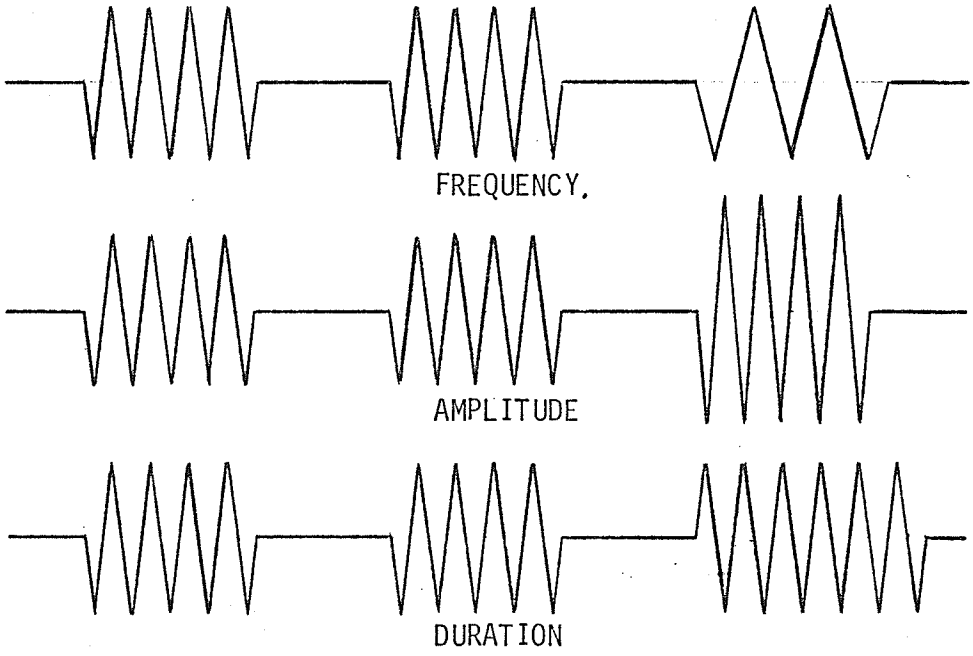
If one examines the basic requirements of the electronic circuit as given in section 1.2, it soon becomes obvious that the only way to achieve these requirements with reasonable precision and for a reasonable cost is to design an analog synthesizing section which is controlled by a digital logic section.

The minimum number of items needed by the synthesizing section which will still satisfy all of the requirements is six: two variable osciallators (frequency), one fixed and one variable amplifier (amplitude), and two variable signal gates (duration).

The minimum requirements for the digital control section are a variable clock (notes per minute control), some means of accurately controlling the starting point and the stopping point of



1.1 A NOTE



1.2 RHYTHMS

the sequence of notes (sequence control), and some means of determining the arrival of every second, third and fourth note in the sequence (rhythm control).

It was decided that the most logical approach to the design of the circuitry would be to have a main synthesizing section consisting of one variable oscillator, a fixed amplifier, and one variable duration producer. When used in conjunction with the clock and the sequence control, the main synthesizing section would produce a predictable and controllable series of identical notes. The rhythm control would switch in the second oscillator, the variable amplifier, or the second duration producer at the appropriate time to complete the desired rhythm synthesis procedure. A block diagram which illustrates the preceeding text is given in Figure 1.3.

It should also be noted at this point that the prime objective in the design of the synthesizer was one of high precision and high accuracy in terms of controllability, observability and repeatability. The absolute purity of the notes in terms of harmonic distortion and signal-to-noise ratio was not considered to be of prime importance because the experiments in which the equipment will be used will be ones which require the perception of small relative differences in the note sequences.

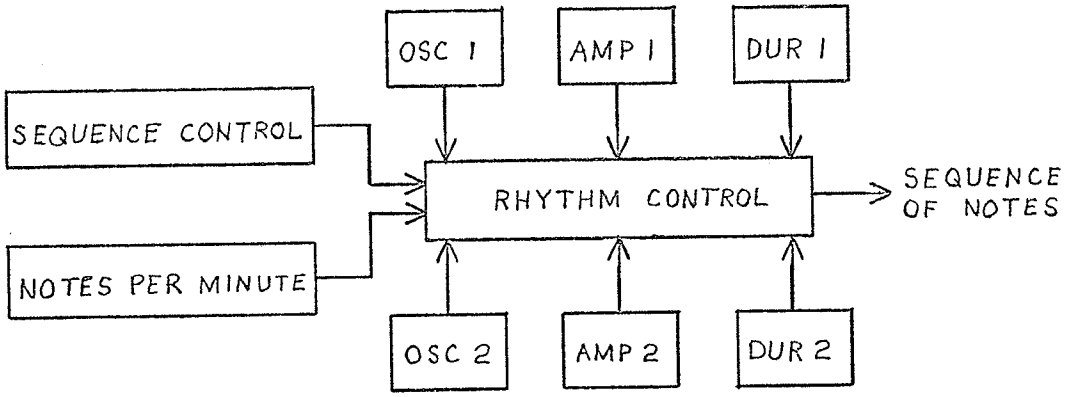
1.4 Schematic Diagram Information

The following four chapters detail the design of the electronic circuitry. The chapters are divided into a number of sections, each of which deals with a specific sub-assembly of the

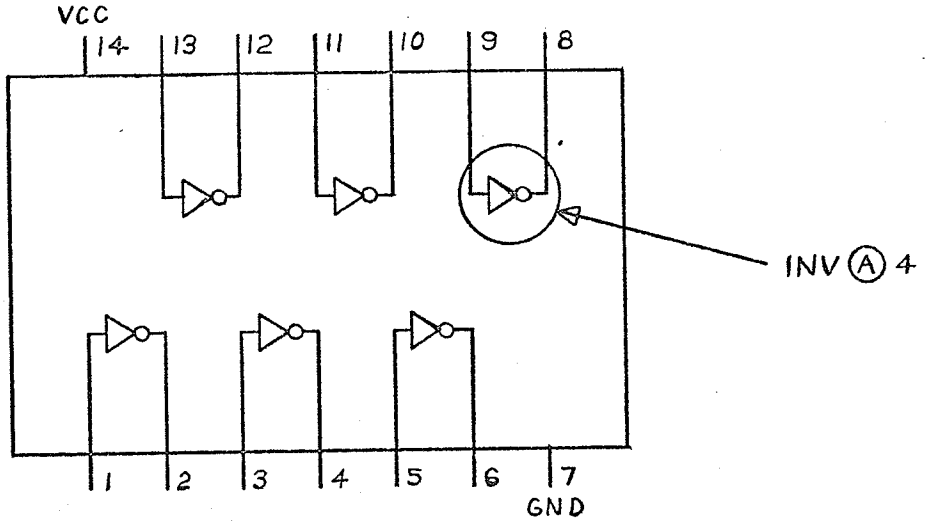
circuitry being examined in that particular chapter. In general, each section contains a schematic diagram which illustrates the material in the corresponding text. The position of the individual schematic diagrams relative to the entire synthesizer circuit is illustrated in Appendix B.

The integrated circuits (IC's) in all of the schematic diagrams are labelled. The labels begin with a two or three letter prefix which indicates the electronic function of the IC. Appendix C gives the corresponding full name and National Semiconductor part number. Following the prefix is a single encircled letter which when correlated to the diagram in Appendix D determines the exact physical location of the IC on the main circuit board.

Finally, if a single IC contains more than one separate circuit component (for example: a CD4081 contains four individual two-input AND gates), the encircled letter in the label will be followed by a number. The number corresponds to the component number defined by National Semiconductor in their data books. If undefined, the number corresponds to the position of the component in the IC data book connection diagram with number one being the component closest to pin one and then proceeding around the IC to the highest pin number. Figure 1.4 illustrates the labelling procedure.



1.3 BLOCK DIAGRAM OF SYNTHESIZER



1.4 IC LABELLING PROCEDURE

II ANALOG SYNTHESIZING CIRCUITRY

The following chapter examines the design of the analog section of the synthesizing circuitry. Specifically, it describes:

(a) the oscillators which produce the synthesizer frequencies,

(b) the amplifiers which are used to control the amplitudes of the signals,

(c) the timers which are the duration producers, and

(d) the output circuitry which provides the final signal processing before the power amplifier.

2.1 Frequency

The oscillators used to synthesize the desired frequencies are two LM566 voltage controlled oscillators (VCO). They are relatively inexpensive, are extremely stable, and have a triangle output which can easily be diode shaped to approximate a sinusoid.

The LM566 is frequency programmable by means of a control voltage, a timing resistor and a timing capacitor. It was decided that for maximum stability and tuning accuracy and a minimum parts count, the voltages and capacitors would be fixed and the resistors would be made variable. The outputs of the oscillators are followed by buffered single-pole high-pass filters which remove the DC components of the triangle waves. Finally, a simple diode shaper, which is shared by both oscillators, is connected between the buffered outputs and ground to convert the triangle signals to waveshapes that more closely approximate sinusoids. One complete oscillator (the other one is identical) is shown in Figure 2.1.

The timing resistor for a 566 is required to be between 2kΩ and 20kΩ for optimum performance of the oscillator. This allows for an output frequency range of approximately 10 to 1.

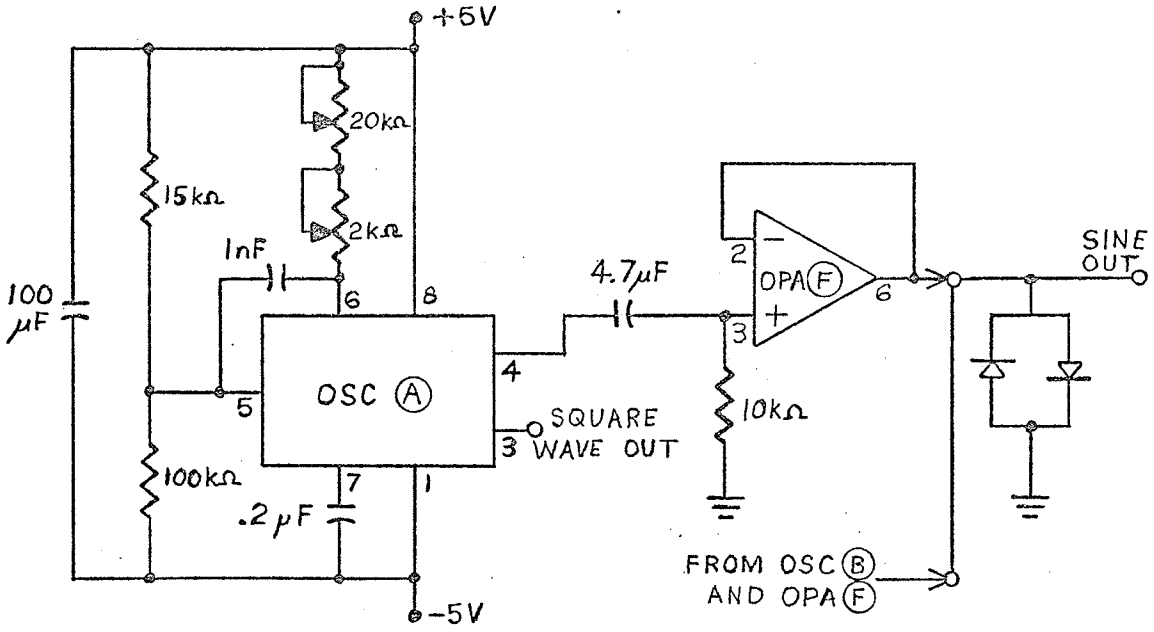
Since most of the musical fundamentals are located between 100Hz and 1kHz, it was decided to choose the timing capacitor and the control voltage so that this particular range would be achieved with resistor values of between 2kΩ and 20kΩ.

2.2 Amplitude

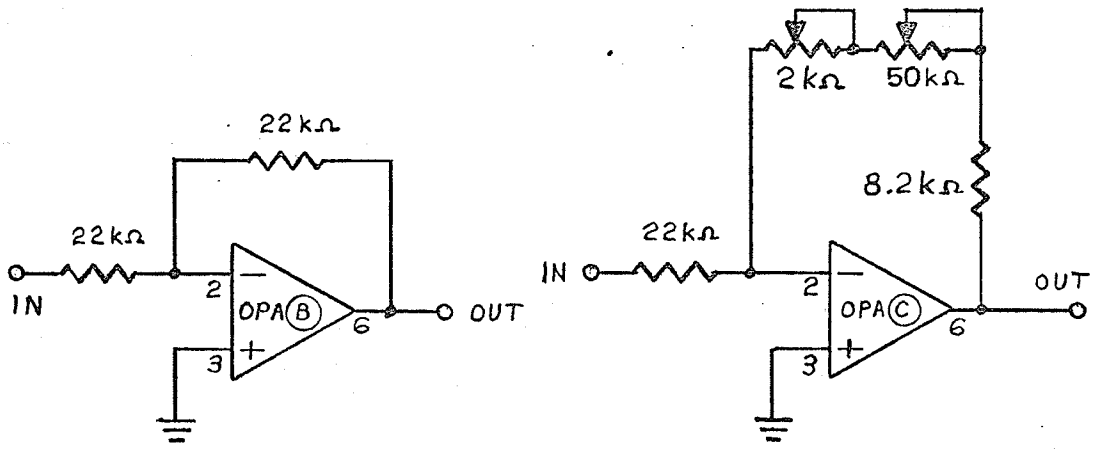
The amplifiers used to control the amplitude of the signal are two 741 op-amps employed in the inverting mode to minimize the component count. The main amplifier has a fixed gain of 1 and the secondary amplifier has an operator controlled variable gain of about .4 to 2.4. Strictly speaking, the gains of the amplifiers are negative values which means that the output is inverted around ground potential with respect to the input. However, since the synthesizer signals are always either at ground potential or are symmetric around ground potential, the minus signs are essentially of no practical consequence and are therefore omitted for the sake of clarity.

The gain of the fixed amplifier was chosen to be 1 because the 1.2 volt (peak-to-peak) outputs of the oscillators are already large enough to ensure a good signal-to-noise ratio and yet small enough to allow the variable amplifier to amplify the signal by at least two times and still be comfortably within the linear operating range of the 741 op-amp. The complete amplifiers are shown in Figure 2.2.

It could be argued that if a minimum parts count is desired, then the main amplifier should be left out completely and the secondary one should be a non-inverting amplifier. One of the reasons for not using this approach goes back to the basic design approach stated in section 1.3. That is, if the amplifiers do add noise or distortion to the signal, then the same amount must be added to the signal for both choices of amplitude. Furthermore, a basic non-inverting amplifier



2.1 OSCILLATOR



2.2 AMPLITUDE AMPLIFIERS

has a minimum gain of 1 and it is desired to produce gains of less than 1. Certainly, a divider network could be placed before the input of the op-amp but then the parts count would be increased to the point where very little or nothing is gained over the chosen method. Finally, the fixed amplifier provides signal buffering which decreases the loading effect that the succeeding stages would otherwise have on the preceding ones.

The variable amplifying ratio limits of .4 and 2.4 enable the operator to produce a secondary signal that is at lease 6 decibels (db) larger or smaller than the main signal. This figure was chosen because it is well accepted that almost anyone can detect an amplitude difference of 3db. Therefore, the amplitude control gives the operator more than twice as much latitude (in terms of decibels) as he is likely to need.

2.3 Duration

The durations of the notes are controlled by two LM3905 precision timers. The timers are entirely self-contained and require only a resistor and a capacitor to set the timing period and a load resistor to limit the current through the output transistor of the IC.

The timing period of the LM3905 is equal to the product of the values of the timing resistor in ohms and the timing capacitor in farads. Furthermore, it was desired to produce durations varying from 0 to 2 seconds. This is to allow the operator to adjust the note durations from 0% (no note) to 100% of even the longest period between notes. The necessity for this will become clear in sections 3.1 and 4.5.

With the afforementioned requirements in mind, the Suggested Timing Components graph for the LM3905 was referred to and it was determined that the optimum timing components were a .22μf capacitor and a 10MΩ variable resistor. One complete duration timer (the other one is identical) is shown in Figure 2.3.

2.4 Output Circuitry

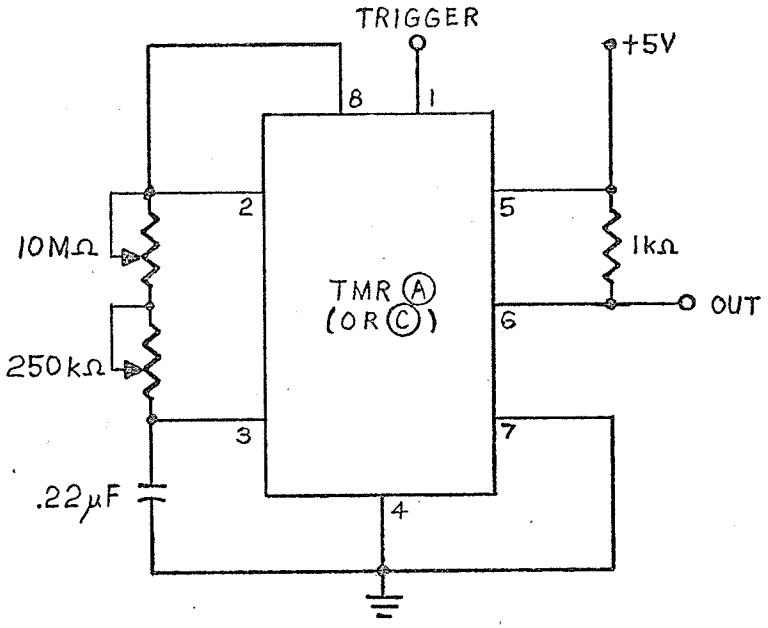
At the output of the synthesizing circuitry, just before the power amplifier, it was necessary to insert an adder and a buffered low-pass filter. The adder is an inverting variable gain amplifier which takes the outputs of the main and secondary synthesizing circuits, adds them together, and allows the operator to control the output amplitude of the synthesizer without affecting the relative amplitudes of the notes in the sequence.

To ensure that the relative amplitudes of the main and secondary signals remain constant, one of the adder input resistors is fixed and the other one is a ten-turn trimpot which is adjusted to exactly equal the value of the fixed resistor. The gain of the amplifier was chosen to be from 0 to .6 which allows the maximum use of the linear range of the power amplifier.

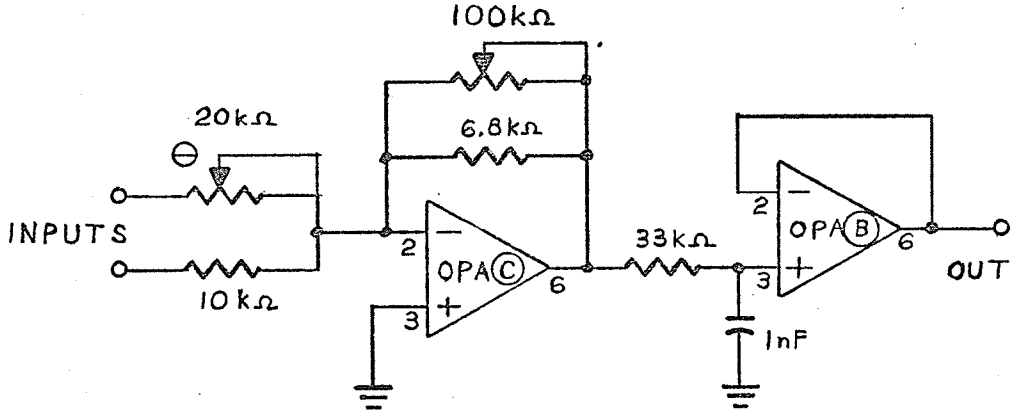
The one-pole low-pass filter removes a great deal of the undesireable high frequency noise that has crept into the signal from the digital control section. The 3db-down point of the filter is approximately 5kHz which passes all the desired fundamental frequencies (up to 1kHz) and at least the next four harmonics. The reason for

allowing some of the harmonics through is that the signals are diode shaped triangle waves and not pure sinusoids. Therefore, to maintain a constant amplitude throughout the entire chosen range of frequencies, it is necessary to allow some of the harmonics to pass through unattenuated.

The output of the buffer amplifier is connected directly to the power amplifier inputs as well as an externally accessible phone jack at the back of the synthesizer case. This is to allow the operator to use a power amplifier and speaker system different from the one provided. The entire output circuit is shown in Figure 2.4.



2.3 TIMER



2.4 MISCELLANEOUS ANALOG CIRCUITRY

III DIGITAL CONTROL CIRCUITRY

The following chapter examines the design of the digital control section of the synthesizer circuitry. Specifically, it describes:

(a) the main system clock which regulates the digital control circuitry,

(b) the sequence control which governs the length of the sequence of notes,

(c) the rhythm control which provides the digital signals which permit the production of rhythms,

(d) the duration control which ensures that spurious noise pulses at the beginnings and ends of the notes are reduced to a minimum, and

(e) the analog switches which interface the digital control circuitry and the analog synthesizing circuitry.

3.1 Clock

The main system clock is generally the heart of any digital circuit. This one is no exception. The clock in this circuit not only regulates every aspect of the digital circuitry but also directly controls the number of notes being produced per minute.

The heart of the clock is the VCO section of an LM565 phase locked loop (PLL). This IC was used instead of the almost identical LM566 VCO because it is less expensive as well as being somewhat more temperature stable. The advantages of the LM566 VCO are a buffered traingle wave output and a maximum frequency of 1MHz as opposed to 500kHz for the LM565. Since neither of these factors are of any benefit in this particular application, the LM566 was not used.

To enable the clock frequency and the duration readout interfacing to track each other accurately (the reason for this is explained in section 4.5), it is necessary to use a fixed timing capacitor, a ten-turn trimpot for the timing resistor, and an operator adjusted voltage to control the clock frequency. The linear range of the VCO is controlled by an input potential of between approximately 2.2 and 4.85 volts which provides a frequency range of approximately 10 to 1.

To provide this control capability, a 741 op-amp is used in non-inverting amplifier form as a voltage controlled voltage source. The non-inverting input of the op-amp is connected to the midpoint of a resistor divider network at approximately 2 volts. A ten-turn trimpot is

connected between the inverting input and ground is adjusted so that the op-amp produces a maximum output of 4.85 volts.

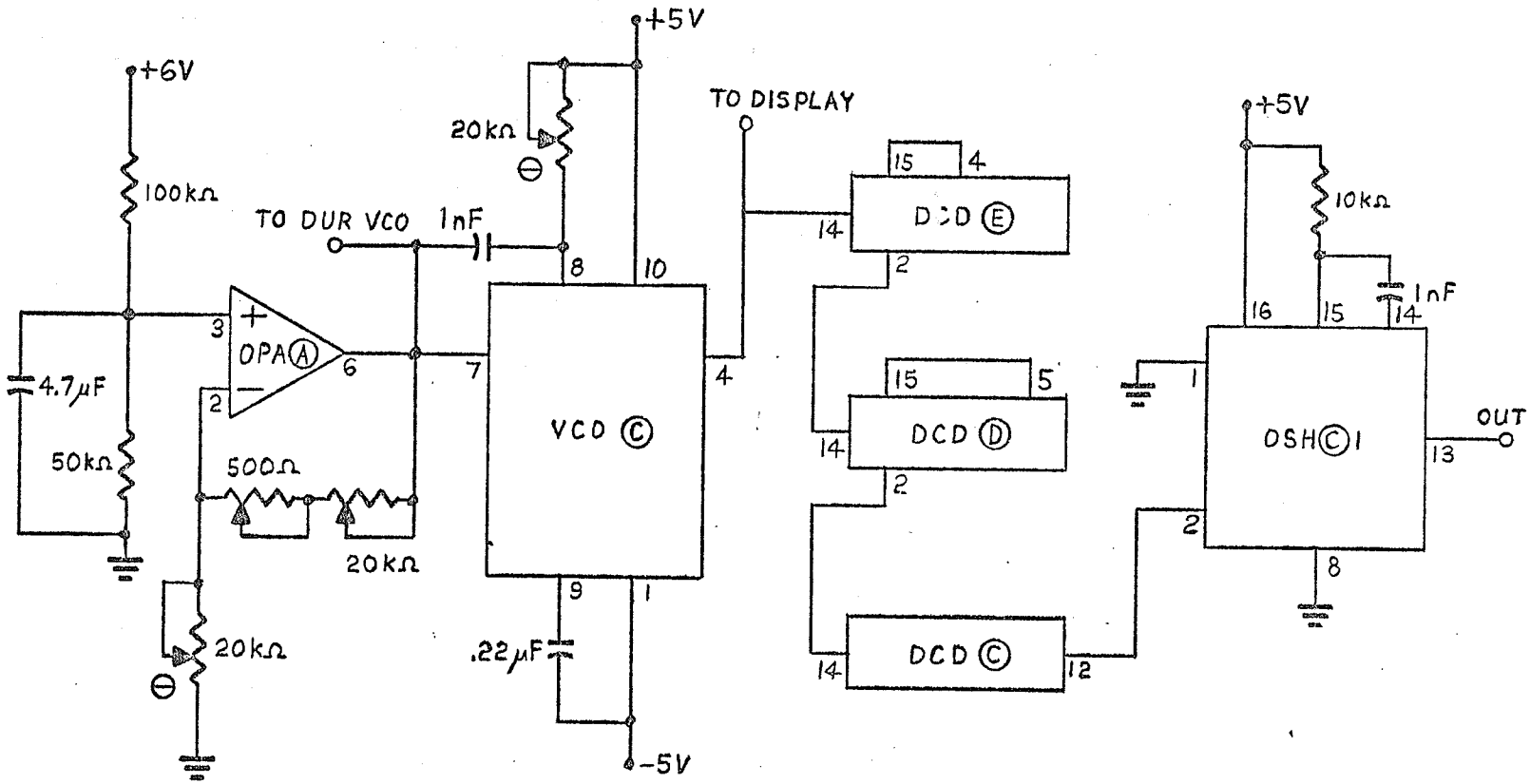
To enable simple and accurate interfacing to the digital readouts for the clock (this is explained in section 4.2) it is necessary to adjust the trimpot on the VCO to produce a frequency output range of 60Hz to 600Hz. The VCO is followed by a digital division section which divides the VCO output by 120. This provides clock frequencies of .5Hz to 5Hz or, equivalently, 30 to 300 beats per minute. This range was decided upon as being more than adequate to cover the rhythm experiment requirements.

Finally, the divider section is followed by a one shot which provides a 10μs pulse at the rising edge of every divider output cycle. The reason for this is explained in section 3.4. Figure 3.1 shows the entire clock circuitry.

3.2 Sequence Control

The sequence control is the section of the digital circuitry which starts the sequence of notes after a command from the operator, stops the notes after a prescribed number of them have been produced, and then resets all of the digital circuitry in preparation for the next note sequence.

When the power switch of the synthesizer is turned on, a .5 second one shot fires which immediately resets all of the digital circuitry and thereby avoids the possibility of a series of notes being produced without intentional operator triggering. When the start button is pushed, the output of a D-type flip-flop (FF), which


+6V
100kΩ
4.7μF
50kΩ
OPA Ⓐ
3
2
6
500Ω
20kΩ
20kΩ
TO DUR VCO
1nF
20kΩ
+5V
8
10
7
VCO Ⓒ
9
1
.22μF
-5V
4
TO DISPLAY
15
4
14
DCD Ⓔ
2
15
5
14
DCD Ⓓ
2
14
DCD Ⓒ
12
+5V
10kΩ
16
15
1nF
14
1
OSH Ⓒ 1
OUT
13
2
8

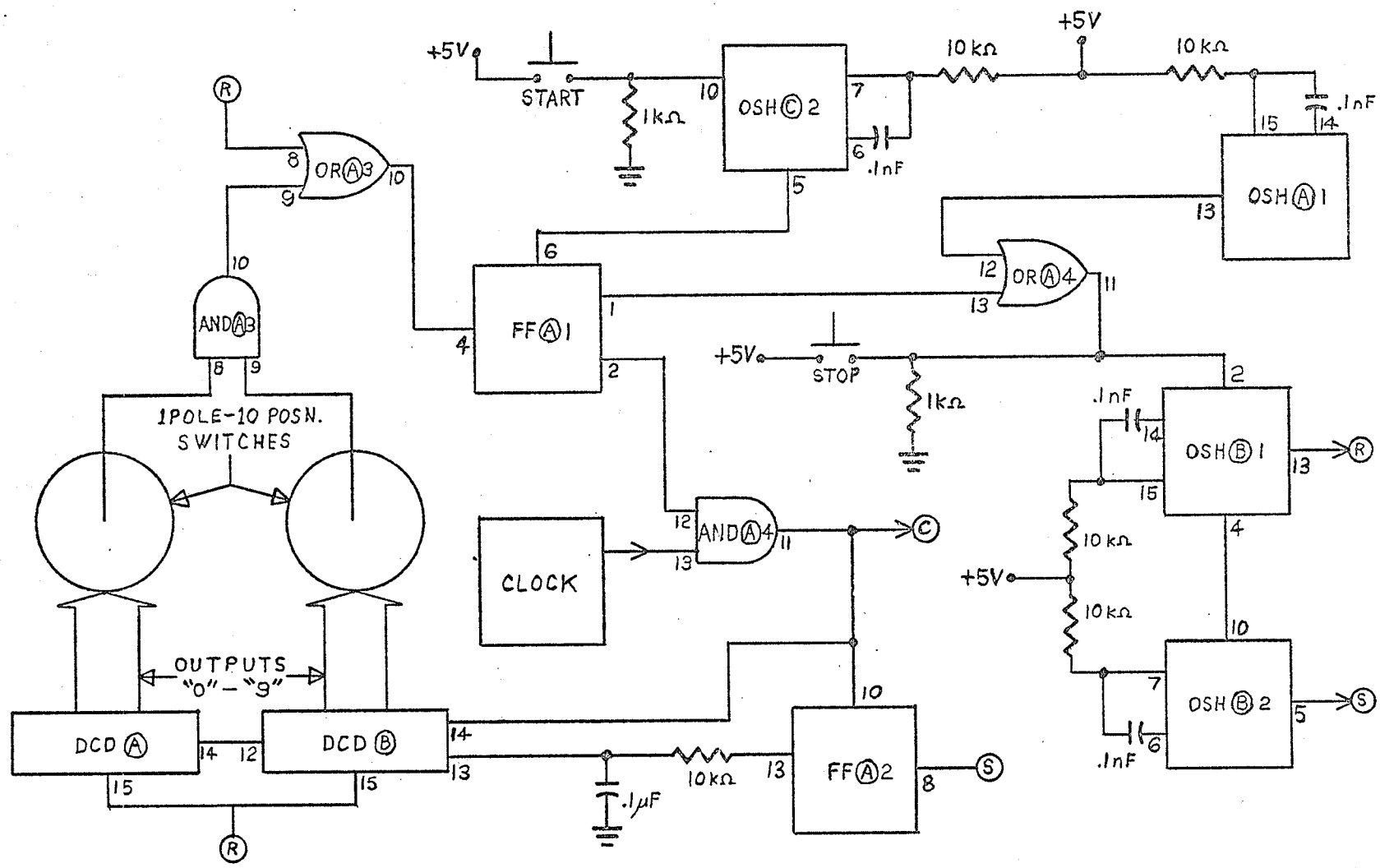
3.1 CLOCK

is being used as a bistable multivibrator, goes high and allows the clock pulses to pass through an AND gate to the rest of the circuitry.

The clock pulses go to the input of the first of two cascaded decade counters which provide a maximum sequence count capability of 99. When the outputs of the decade counters match the sequence length chosen by the operator, an AND gate forces the previously mentioned FF output to zero which removes the clock pulses from the rest of the circuitry. Finally, two oneshots provide consecutive pulses which once again reset and set the control circuitry in preparation for the next note sequence.

Since the decade counters stop the sequence immediately at the rising edge of the nth note, only n-1 notes will be heard. To avoid this, a FF followed by a low-pass network was inserted between the clock output and the clock enable terminal of the first decade counter. In the set position, the FF keeps the clock enable terminal high which disables the clock terminal of the decade counter. The FF output goes low at the arrival of the first operator triggered clock pulse. The lowpass network is chosen with a time constant of approximately 1ms which keeps the clock enable high during the entire first clock pulse but allows it to go low before the second pulse arrives. This timing procedure applies to the entire available range of system clock rates.

An operator controlled stop button which immediately halts the note sequence when depressed is also provided. The entire sequence control is shown in Figure 3.2.



3.2 SEQUENCE CONTROL

3.3 Rhythm Control

The rhythm control provides the capability for the digital control circuitry to switch in the second VCO, the variable amplifier, or the second duration timer at the appropriate position in the note sequence.

Since the School of Music only requires the capability to tailor every second, third, or fourth note, it was decided to solve the rhythm control problem by using groups of shift registers.

The first group of four D-type flip-flops is hooked up in a continuous loop such that the output of each one goes to the input of the next. With the shift registers arranged in this fashion, if the output of only one of them is high at any point in time, then that same one will not go high again until four clock pulses later. In the "ready" position of the synthesizer, the output of one FF is set to high and the other three are reset to low. The control signal for a beat on every fourth note is taken from the output of the FF which was initially set to high.

The second group of shift registers is set up similarly to the first group except that there are only three flip-flops. This group obviously provides the control signal for a beat on every third note. The third group, which provides a beat on every second note is merely a single FF with the output tied back to the input through an inverter.

The various terminals of the flip-flops are hooked up such that at the end of a note sequence, when the reset and set pulses are

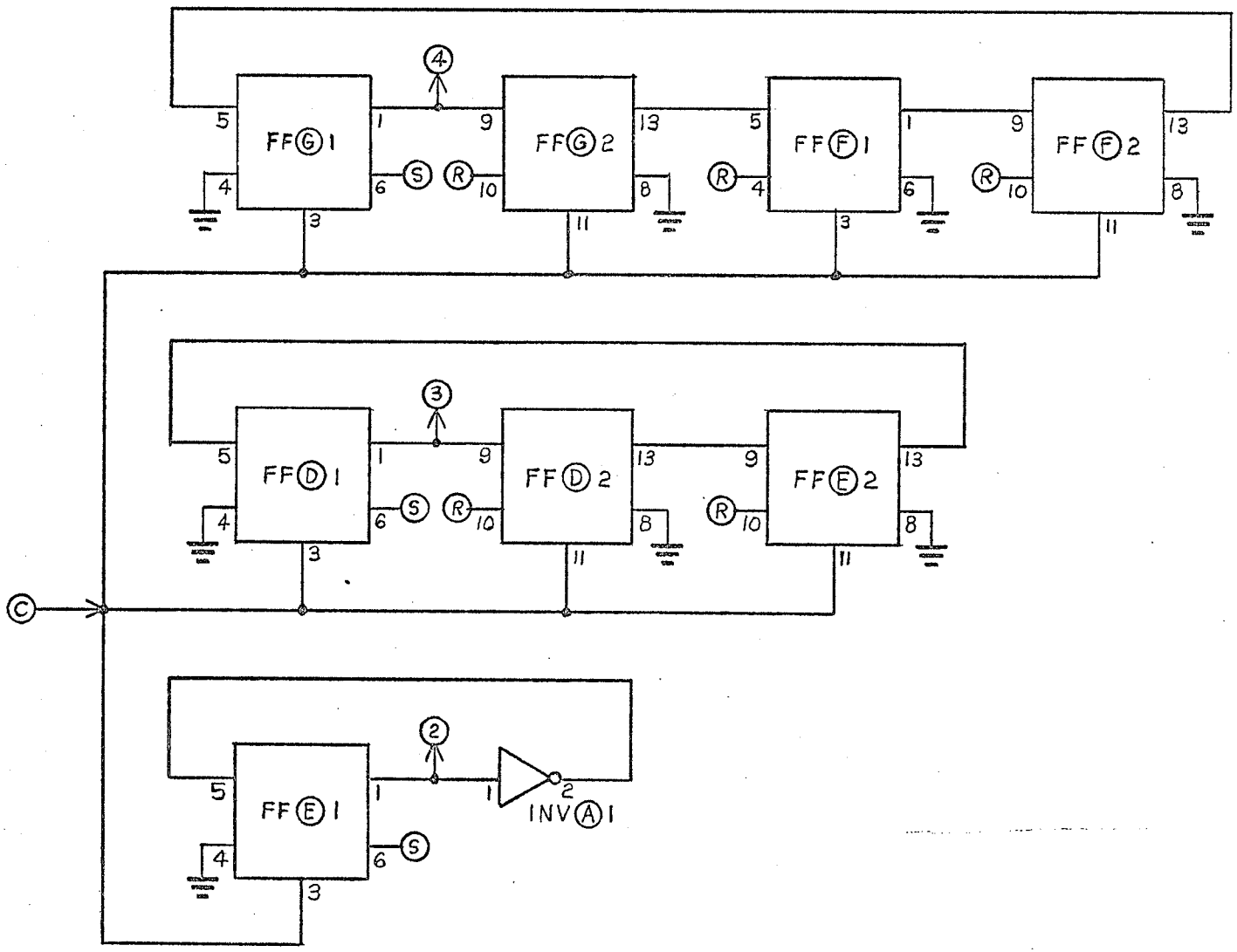
generated, all the flip-flops will be reset to low except for the designated control signal FF in each group which is set to high. The entire rhythm control circuit is shown in Figure 3.3.

3.4 Duration Control

In section 2.3, a timer or "duration producer" was described. Obviously the timer must be triggered by the system clock so that the time between the beginnings of any two consecutive notes in a sequence is the same as the time of one cycle of the desired notes per minute rate.

The problem is that the clock must also perform all of the digital control tasks. If the duration timers are triggered at exactly the same time as the flip-flops in the rhythm control are clocked, the beginnings of the notes are plagued by spurious noise pulses injected into the analog circuitry from the settling digital circuitry. To alleviate this problem it is necessary to delay the beginning of the duration pulses 10μs beyond the start of the notes per minute clock pulse. This explains the need for the one shot in Figure 2.1. The inverting output of the 10μs one shot is tied to the input of a 1μs one shot which in turn triggers the duration timers.

Another problem arises when the timers "open" and "close" and allow a certain portion of the desired oscillator frequency to pass. Looking at Figure 3.4.1 we see how, in general, the timer triggered directly by the clock might pass a certain "block" of signal to produce a note. In the example shown, rather than hearing a single pure tone, one would hear a small "tick" followed immediately by the note which would end in an even louder "tick".

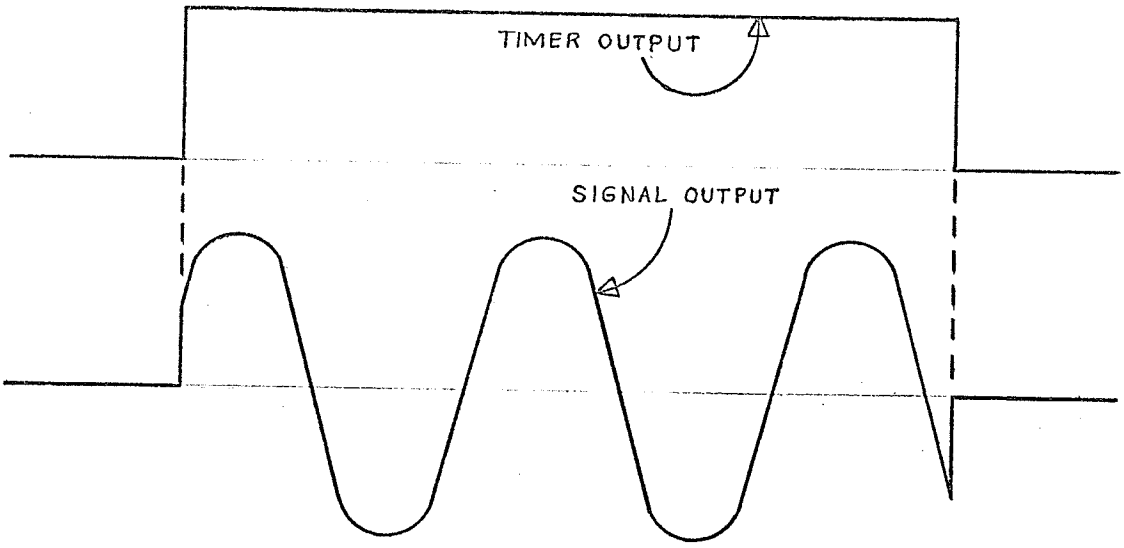


3.3 RHYTHM CONTROL

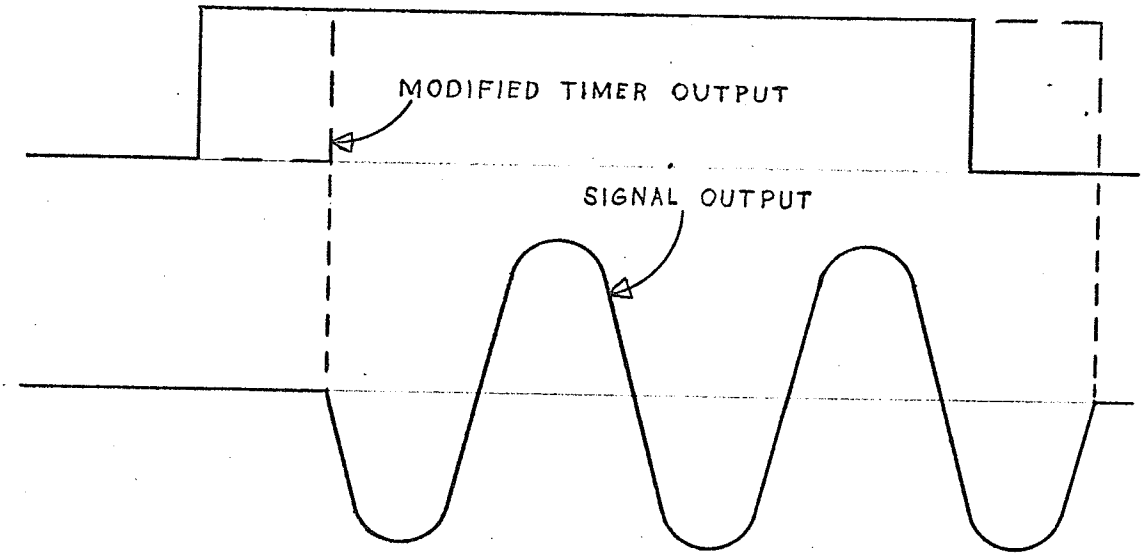
These audible "ticks" or "pops" are caused by the speaker attempting to follow the steep waveforms at both ends of the note. Filtering the signal is a poor solution because any filter that would smooth out the waveform at the maximum frequency of 1kHz would obviously be ineffective at 100Hz. In addition, any filter that would be effective at even a single fixed frequency would have to have a sharp cut-off slope which would introduce severe signal distortion due to phase shift and signal overshoot at the end of the note.

The only acceptable solution to the "tick" problem seemed to be to incorporate a zero-crossing detector into the duration timer output circuit. That is, the timer will go high but no signal will pass until the oscillator signal comes to a zero crossing point (ground potential). Similarly, the signal will not be cut off until both the timer output has gone low and the VCO signal has come to a zero crossing. Using this method, audible "ticks" would be reduced to a minimum. Figure 3.4.2 illustrates the effect.

The circuitry used to implement this concept is shown in Figure 3.4.3. The oscillator signal goes to a comparator which produces a square wave from the sine wave with the vertial portions of the square wave corresponding to the points at which the sine wave crosses zero or ground potential. The square wave triggers two 1μs one shots - one on its rising edge and one on its falling edge. The outputs of the one shots are connected to an EXOR gate. The output of the EXOR gate is therefore a series of 1us pulses at twice the desired oscillator frequency. These pulses go to one input of each



3.4.1 SIGNAL OUTPUT: TIMER TRIGGERED BY CLOCK



3.4.2 Signal Output: Timer Triggered By Clock And Zero Crossing

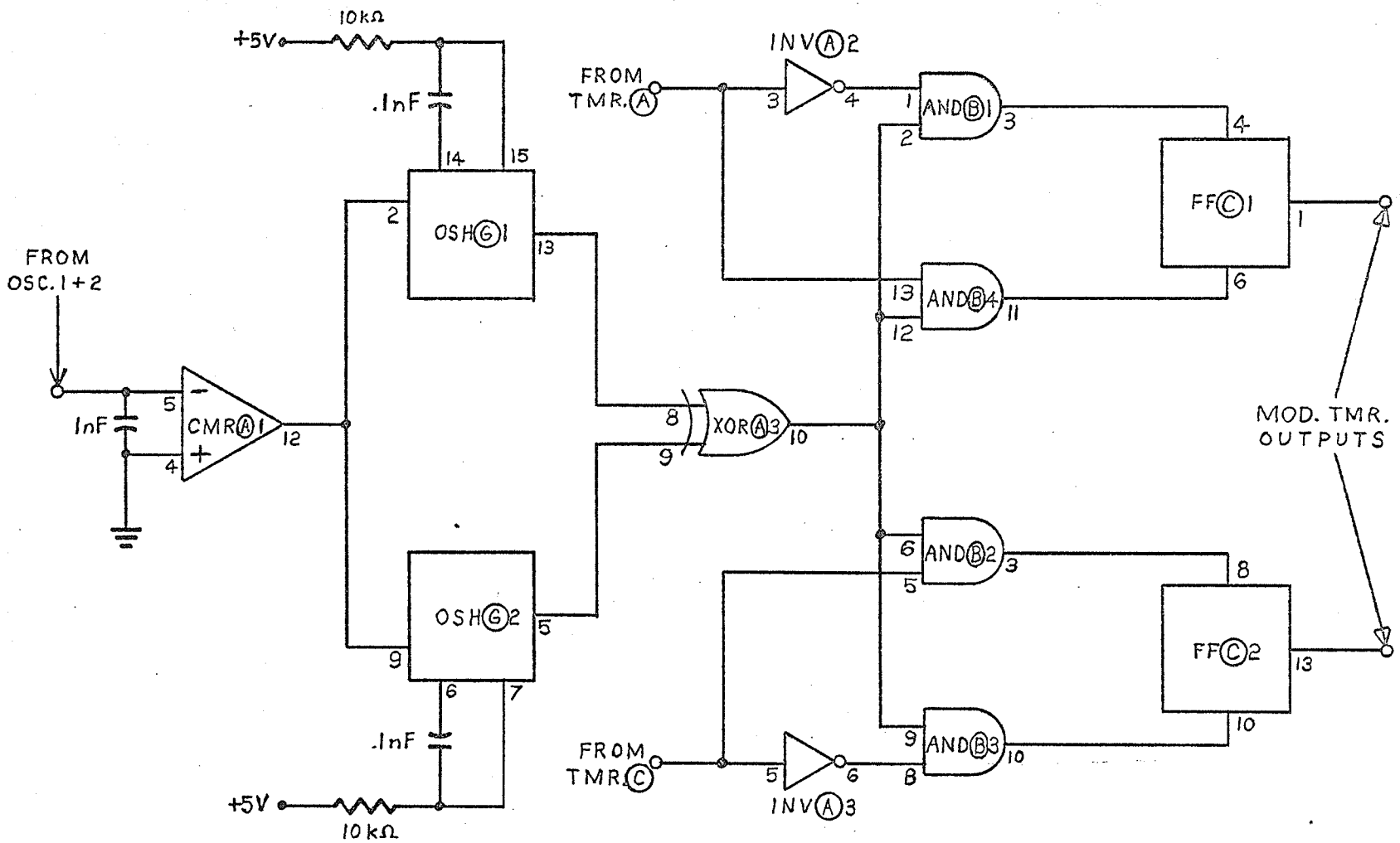
of four two-input AND gates. The other AND gate inputs are controlled by the duration timers as shown. The outputs of the AND gates are connected to the set and reset terminals of flip-flops used as bistable multivibrators. The outputs of the flip-flops are now the modified timer outputs which perform the duration producing function. This modification introduces no duration readout error because the outputs of the flip-flops rather than the timers are used to determine the duration length.

The only negative side effect is that the duration is no longer continuously variable but discretized. In other words, the duration can only be adjusted to values which are integral multiples of twice[1] the oscillator frequency. At the worst possible case of discretization, that is, at a clock rate of 300 beats per minute and an oscillator frequency of 100 Hz, the smallest achievable duration change is 2.5% of the clock rate. At a more typical clock rate of 120 beats per minute and an oscillator frequency of 400 Hz, the smallest duration change is .25%. This restriction is undoubtedly much more tolerable than the annoyance of a sequence of notes filled with "ticks" and "pops" of varying intensities.

3.5 Analog Switches

All of the analog synthesizing circuitry and all of the digital control circuitry mentioned thus far are of no use if they cannot be interfaced in an acceptable manner. The solution to this problem comes in the form of CMOS analog switches. These devices are

1 There are two zero crossings per oscillator cycle.

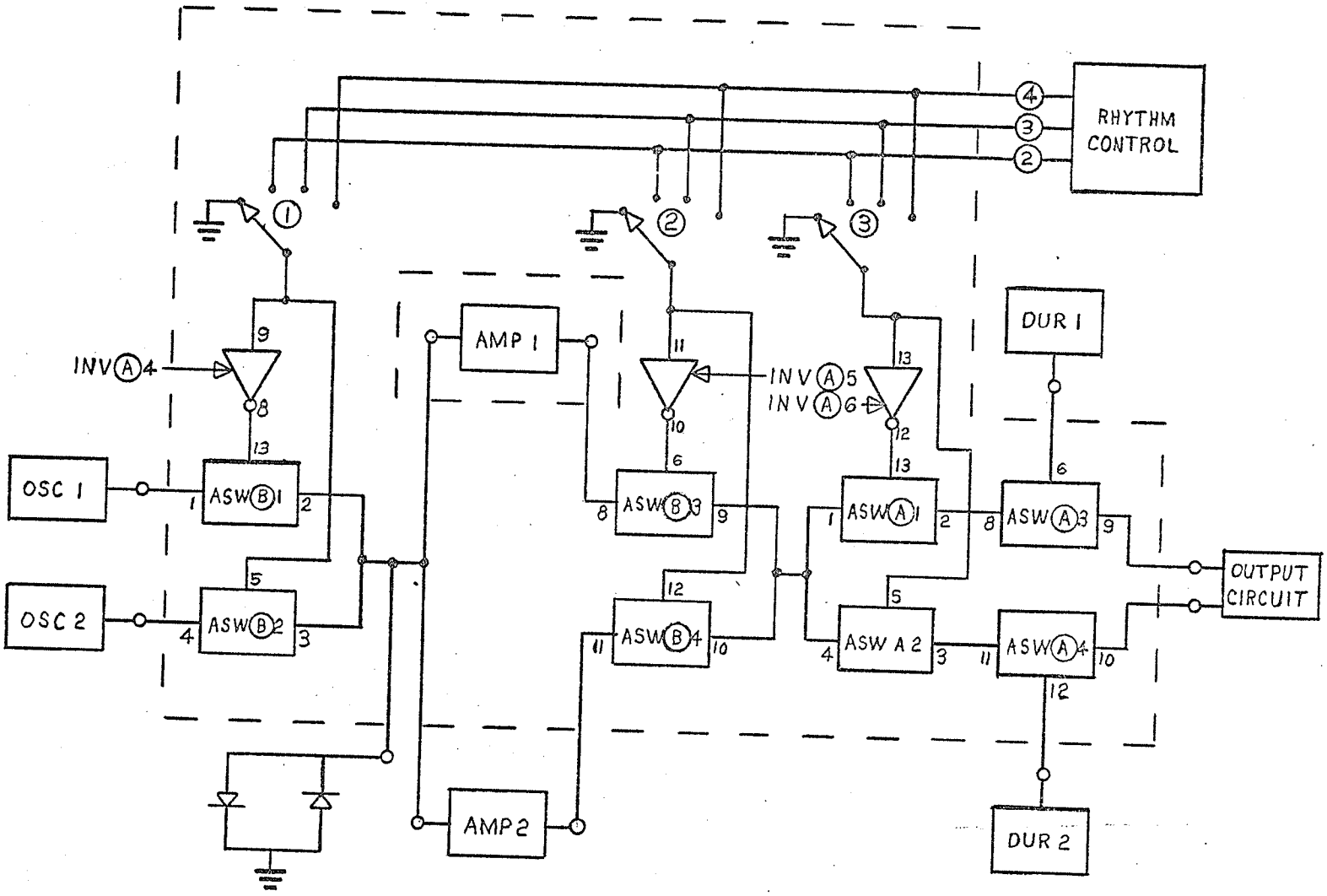


3.4.3 DURATION MODIFICATIONS

used wherever a person requires the ability to electronically switch an analog or digital signal on or off quickly and accurately. Each analog switch has an input, an output, and a control terminal. The switch is closed when the voltage at the control terminal is high and is open when the control voltage is low. So vital are these devices to the operation of the synthesizer that their entire specifications are reprinted in Appendix E.

Figure 3.5 illustrates the position of the analog switches in the synthesizer circuitry. With all three of the manually adjusted four position switches as shown, the main analog synthesizing modules will produce a series of identical notes. Note that though both modified duration producers close their corresponding analog switches at every clock pulse, only one of them will pass a signal because of the pass/block operation of the third pair of analog switches.

To demonstrate the operation of the rhythm control, suppose, for example, that the operator switches manual switch one to position two, manual switch two to position three, and manual switch three to position four. It should be easy to see that every second note would be the frequency of oscillator two instead of oscillator one, that every third note would have an amplitude determined by amplifier two instead of amplifier one, and that every fourth note would have a duration determined by modified duration producer two instead of one.



3.5 ANALOG-DIGITAL INTERFACE

IV DIGITAL READOUT INTERFACING

The following chapter examines the design of the interfacing circuitry between the synthesizer variables and their corresponding digital readouts. Specifically, it describes:

(a) the MM74C926 counter/driver which greatly simplifies the task of readout interface design in this particular application and

(b) the distinctive interface circuitry which is necessary for each of the individually monitored synthesizer variables.

4.1 Introduction

The task of interfacing the various variable functions in the circuitry to seven segment displays was significantly simplified through the use of a very flexible integrated circuit - the MM74C926. This IC is basically a four digit counter with multiplexed seven segment output drivers. The counter section has a clock input and is controlled by a reset terminal and a latch enable terminal. The driver section is entirely self-contained and only requires seven current limiting resistors and four transistors to switch the seven segment displays. A typical display system employing the MM74C926 is shown in Figure 4.1.1. Like the analog switches, the counter/driver is so vital to the operation of the synthesizer that its data sheet has been reprinted in Appendix F.

The digital readouts or displays on the front panel of the synthesizer are all driven directly by MM74C926's. When the reset terminal is pulsed, the counter goes to zero and begins to count the pulses entering the clock terminal. When the latch enable terminal is pulsed, the IC latches onto and displays whatever number is in the counter at the time of the pulse and will continue to display that particular number until the latch enable is pulsed again.

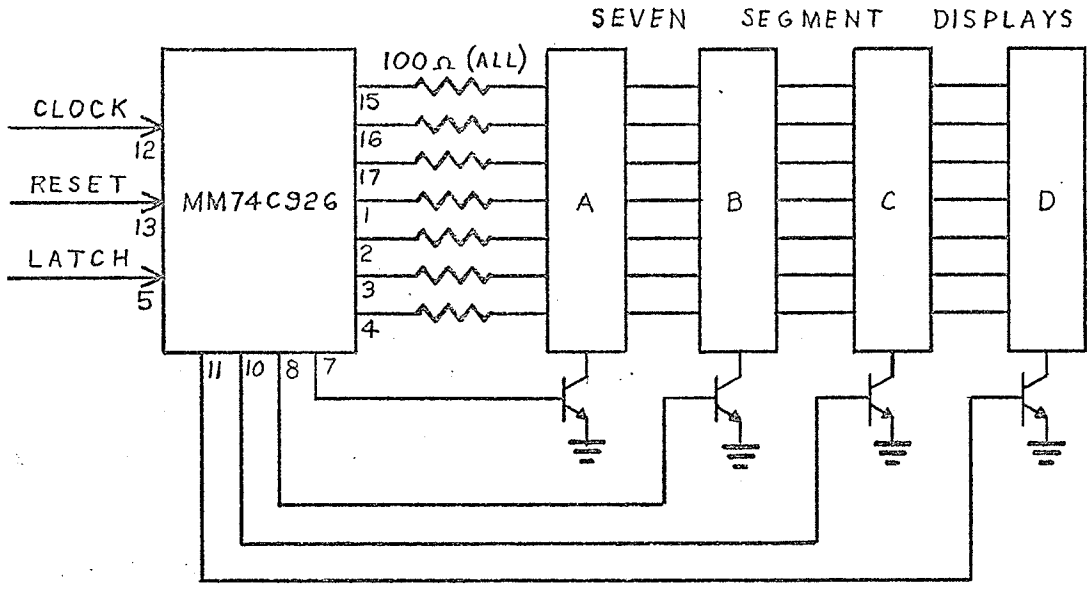
Obviously, with the type of operation just described, the readouts cannot be updated continuously but rather at discrete intervals. In fact, the longer the time between the reset pulse and the latch enable pulse, the greater the ratio between the sample time

and the time of a single counter clock cycle and hence the greater the accuracy of the readout value. It was found that an update sample time of .5 seconds was about optimum for this application. This time period is long enough for good accuracy and yet short enough so that the operator does not become impatient waiting for readout updating while adjusting some variable.

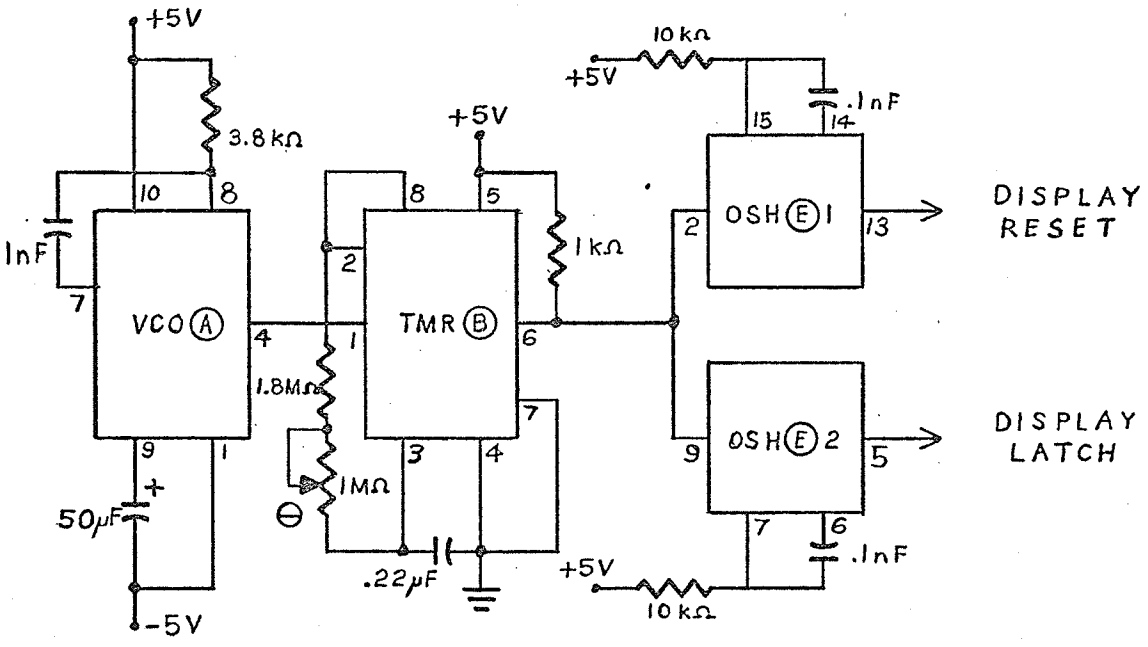
To produce the .5 second sample time, an LM3905 precision timer is used. The timer is triggered by a free-running LM565PLL-VCO operating at about 1.4Hz. The timer itself is fine tuned with a ten-turn trimpot. The output of the timer is connected to two 1μs one shots - one which produces a pulse at the rising edge of the timer output, and one which produces a pulse at the falling edge. These two pulses, appearing .5 seconds apart, are the control signals for the counter/drivers for all the readouts except for those corresponding to the duration values. The sample time control circuit is shown in Figure 4.1.2.

4.2 Clock

In section 3.1 it was stated that the 30 to 300 beats per minute are produced by dividing the output of a 60 to 600Hz VCO by 120. The reason for this is to enable the output of the system clock VCO to be directly connected to the clock terminal of the corresponding counter/driver. Since the sample time is .5 seconds, the display will directly show the number of notes being produced per minute. For example, if the operator wished to have 90 beats per minute he would adjust the appropriate potentiometers until the display read 90. This



4.1.1 MULTIPLEXED DISPLAY SYSTEM



4.1.2 SAMPLE TIME CONTROL

would correspond to a VCO frequency of 180Hz which when divided by 120 would produce a frequency of 1.5Hz or 90 beats per minute.

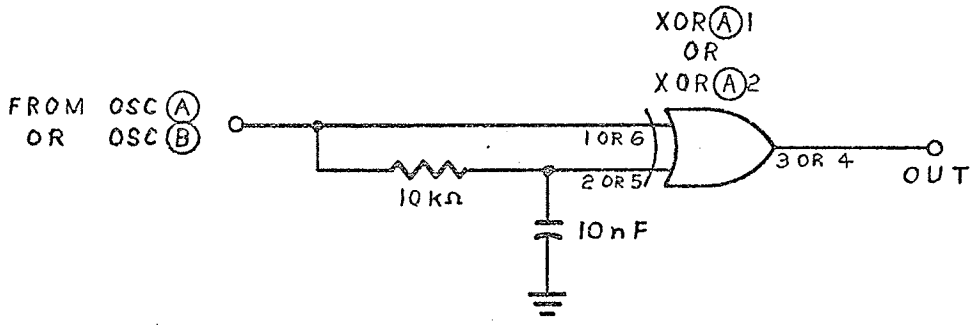
The display section for the clock is similar to Figure 4.1.1 except that only digits B, C and D are used. The reset and latch enable pulses come from the sample time control and, as mentioned previously, the clock terminal of the counter/driver is connected to the VCO output of the system clock.

4.3 Frequency

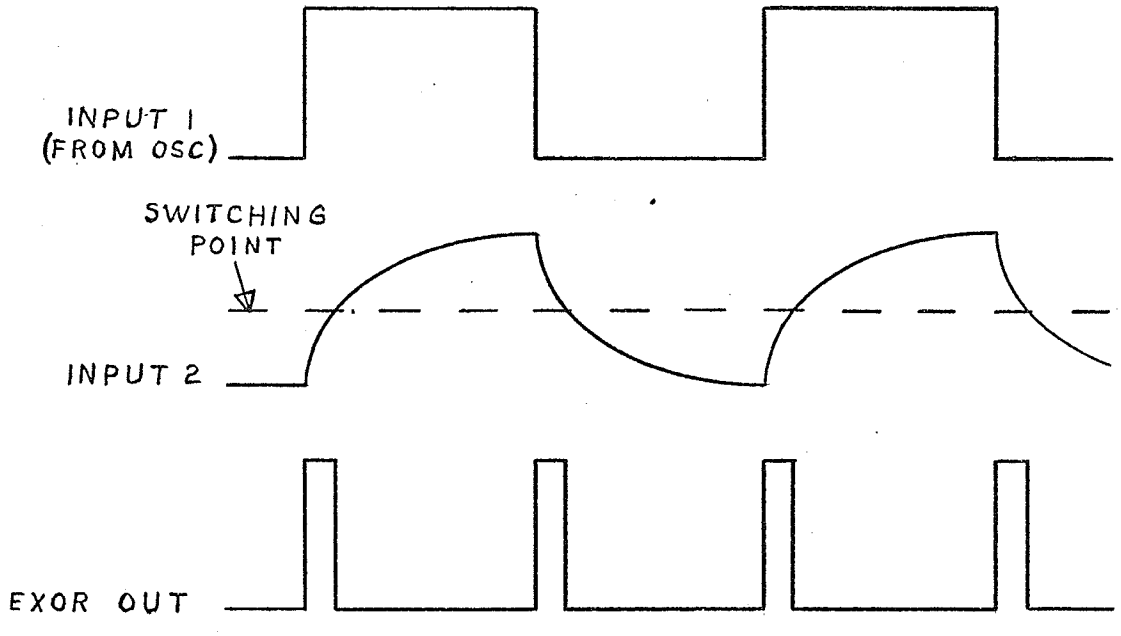
The frequency display sections are exactly as shown in Figure 4.1.1 with the reset and latch enable pulses coming from the sample time control circuitry of Figure 4.1.2. However, production of the appropriate signals for the frequency counter/driver clock inputs proved to be a bit of a problem. Since the sample time is .5 seconds, it is necessary to provide the clock terminals of the frequency counter/drivers with clock rates of exactly twice the oscillator frequencies for accurate frequency display readings.

Since the clock terminal of the MM74C926 can count short duty cycle pulses as easily as square waves, strings of pulses at twice the oscillator frequencies were produced by using a circuit as shown in Figure 4.2.1. The operation of the frequency doubler is described in the following paragraph (refer to Figure 4.2.2).

Just before the beginning of a square wave, inputs 1 and 2 are low causing the EXOR output to be low. When the oscillator goes high, input 1 immediately goes high as does the output of the EXOR gate. Input 2 does not go high until it crosses the "turn-on" point



4.2.1 FREQUENCY DOUBLER



4.2.2 OPERATION OF FREQUENCY DOUBLER

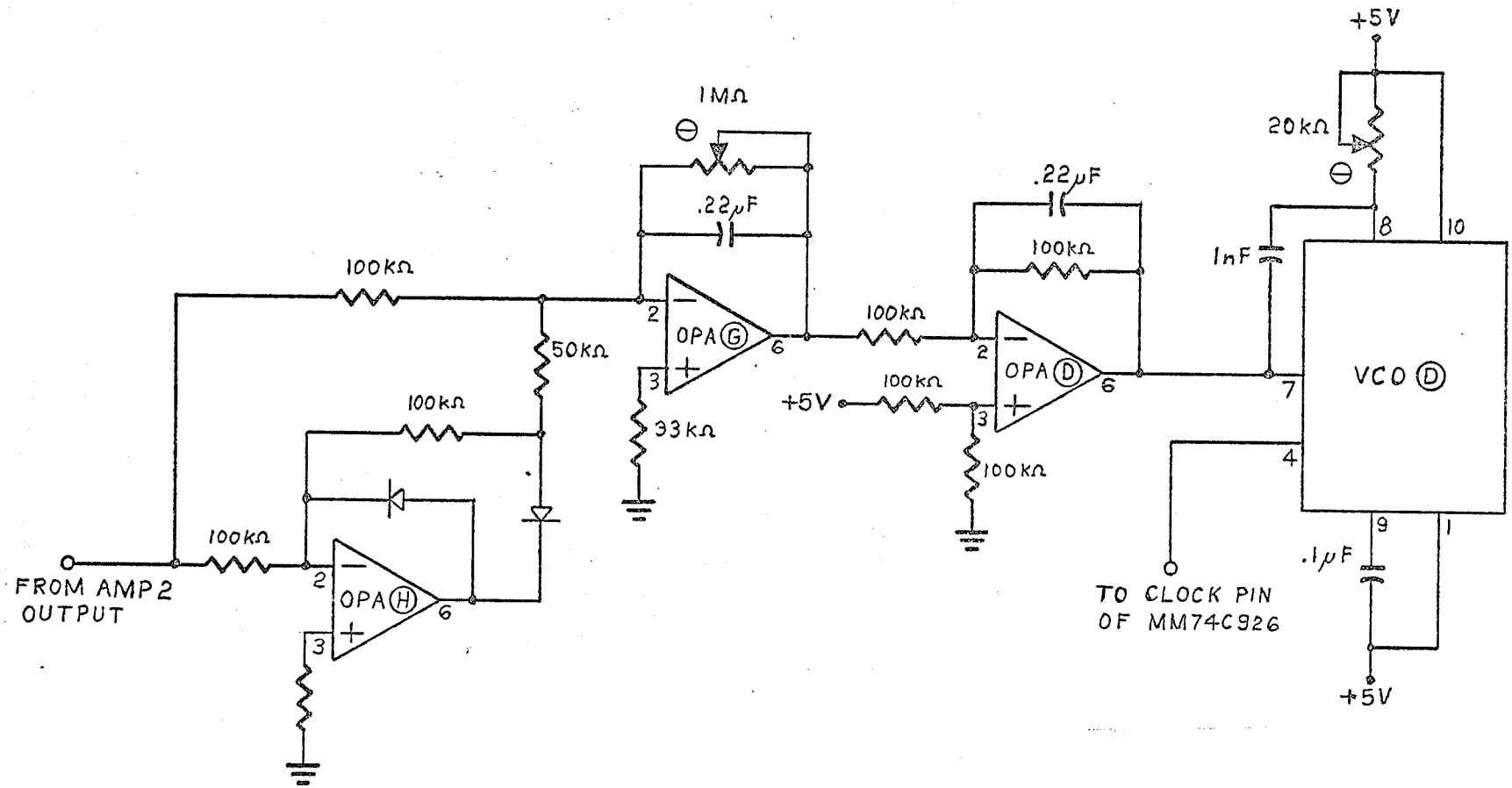
of the EXOR input which takes about .1ms. When this occurs, the output of the gate goes low. When the oscillator goes low, input 1 immediately goes low but input 2 does not. This causes the EXOR output to go high once again. Finally, after about .1ms, the capacitor has discharged sufficiently for input 2 to also go low which the gate output immediately follows. Thus we have two pulses for one oscillator cycle.

It should be noted that with the RC as shown, the circuit will safely double oscillator frequencies up to about 5kHz before the EXOR output pulse widths approach the time duration of one-half oscillator cycle. This means that the frequency doubler will operate satisfactorily for all required oscillator frequencies.

4.4 Amplitude

The circuitry between the variable amplifier and the amplitude readout is the most complex of all the interfacing circuitry. It was decided to take the signal from the output of the variable amplifier and convert it to a DC voltage which is proportional to the amplitude of the signal. After suitable conditioning, the DC voltage is fed to the control terminal of a VCO. When properly adjusted, the VCO frequency increases or decreases in direct proportion to the amplitude increase or decrease of the signal. The amplitude interface circuit is shown in Figure 4.3.

The first two op-amps and related components are the AC to DC converter. This circuit is very common and can be found in practically any book on op-amp applications and will therefore not be analyzed here. Suffice it to say that it produces a DC output from



4.3 AMPLITUDE READOUT INTERFACE

an AC signal input. The choice of the value of the capacitor in the feedback section of the second op-amp requires some care. The larger the capacitance, the purer the DC output. However, the reaction time of the converter is slowed with increasing capacitance. The value finally chosen was the largest capacitance possible which would not cause any noticeable lag in readout update during operator adjustment of the amplitude. The ten-turn trimpot in the feedback path of the second op-amp is adjusted so that the control voltage at the output of the third op-amp is in the centre of the VCO's linear operating region when the variable amplifier is at unity gain.

It is a characteristic of the LM565PLL-VCO that the output frequency increases in direct proportion to control voltage decrease. For this reason the third op-amp, used as a difference amplifier, is inserted to condition the output of the AC to DC converter for suitable interfacing with the VCO. The capacitor in the feedback loop of the third op-amp provides further control signal smoothing.

Finally, the VCO timing capacitor and ten-turn trimpot were chosen and adjusted to provide an output frequency which is twice the value, in percent, of the variable amplifier amplitude relative to the fixed amplifier amplitude. Since the sample time is .5 seconds, the amplitude display, which, like the clock display, uses only digits B, C and D, directly shows the correct value.

4.5 Duration

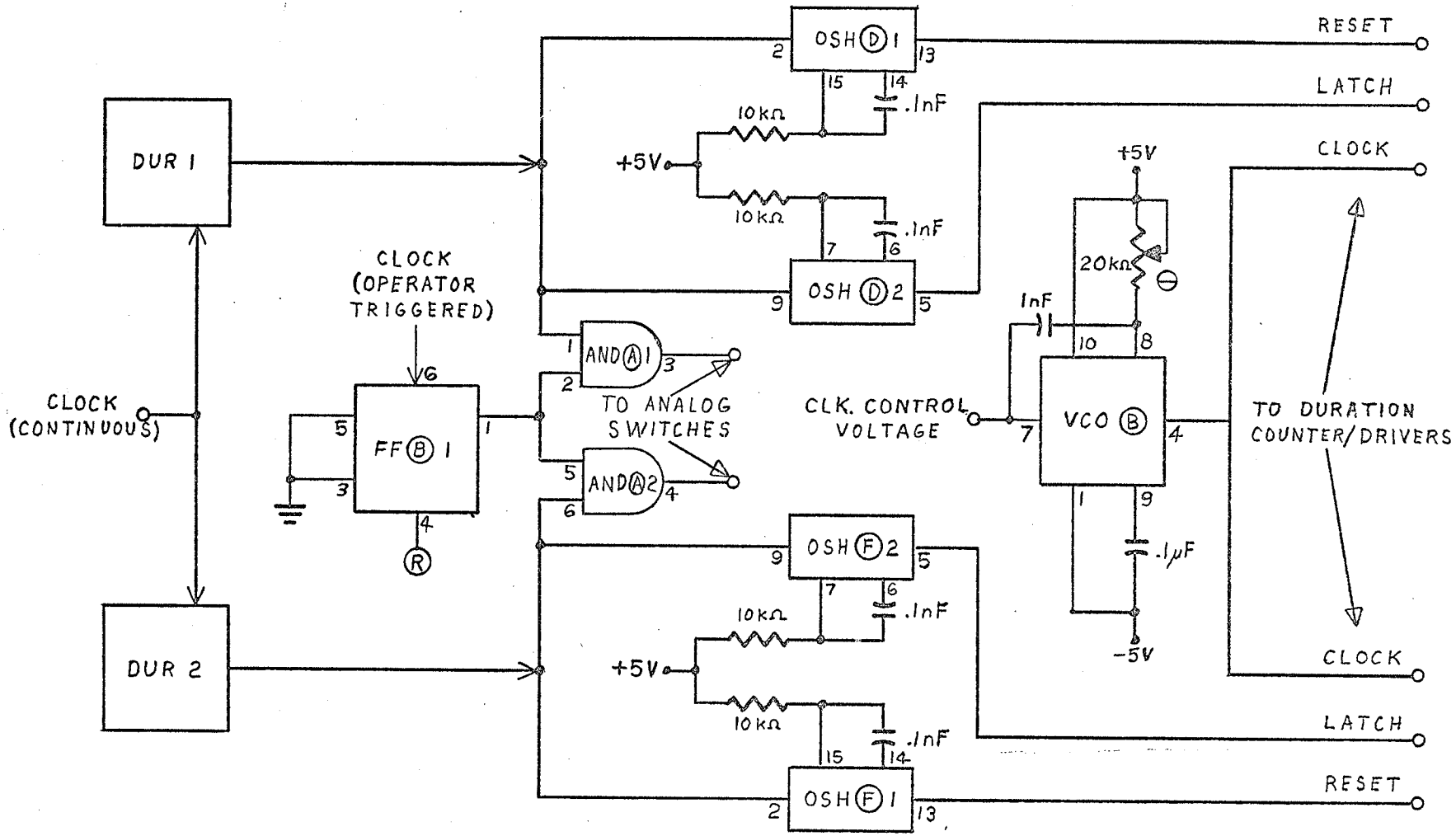
The interfacing for the duration readouts is different from all the other readouts in that the .5 second sample time control is not used. The output of each modified duration producer is connected

to two 1μs one shots - one which is triggered on the rising edge of the duration pulse and one which is triggered on the falling edge. These one shots are connected to the reset and latch enable terminals of the appropriate counter/driver and directly control the sample time of the duration readout circuitry.

The clock inputs of the duration counter/drivers are connected to the output of an LM565PLL-VCO. This VCO has a fixed timing capacitor and a ten-turn trimpot and is controlled by the same operator adjusted voltage which controls the system clock VCO. With the circuitry arranged in this fashion and with the trimpot adjusted suitably, the duration readouts display the duration of the notes in percent of the total time between notes as set by the notes per minute controls. This was decided upon as being the most useful as well as the most easily adjustable method of duration display. Like the clock and amplitude displays, only digits B, C and D are used in the duration readout.

If the duration timers are triggered by the system clock after the sequence control AND gate, then adjustments to the durations will be possible only when the synthesizer is playing. This is clearly undesirable. On the other hand, to be able to adjust the durations at all times, it is necessary to trigger the timers with the system clock before the sequence control AND gate. This would cause the synthesizer to play continuously from the time it is shut on until the time it is shut off. This is clearly even more undesirable.

The entire problem is solved by the addition of a FF and two AND gates as shown in Figure 4.4. In this circuit, the timers are being triggered by every clock pulse and consequently can be adjusted at any time. However, the duration outputs are not allowed to pass to the analog switches until the first operator-triggered clock pulse has passed through to the rest of the circuit. This first pulse forces the FF output to the high state which "turns on" the duration AND gates. When the sequence of notes is over, the sequence control reset pulse causes the FF output to go low which effectively cuts off the duration pulses from the analog switches.



4.4 DURATION READOUT INTERFACE

V MISCELLANEOUS CIRCUITRY

The following chapter examines the design of the necessary synthesizer circuitry which was not covered in the previous three chapters. Specifically, it describes:

(a) the integrated circuit audio power amplifiers,

(b) the synthesizer power supply, and

(c) the power supply protection circuitry.

5.1 Power Amplifiers

The output of the unity gain buffer amplifier shown in Figure 2.4 is tied to both inputs of an LM378. The LM378 is an integrated circuit that contains two independent audio power amplifiers. Each amplifier can deliver up to four watts into a 8Ω load (typical speaker impedance) if adequate heat sinking is provided.

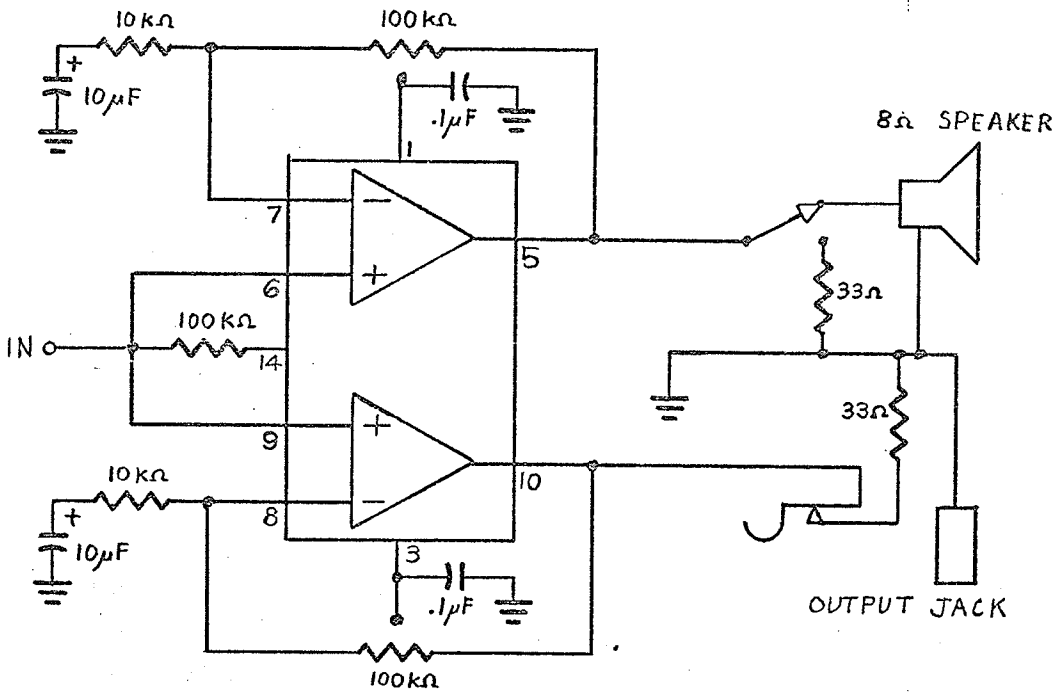
The external components of the amplifiers have been chosen to produce a voltage gain of 10. This value is large enough to ensure that the LM378 operates comfortably within its stable region and yet is small enough to allow the preamplifier circuitry to operate with signals which are of sufficient amplitude to ensure a good overall signal-to-noise ratio.

The output of one of the power amplifiers is used to drive the internal synthesizer speaker. The speaker can be switched on or off as desired. The output of the second amplifier is tied to a standard phone jack at the back of the synthesizer case. This enables the use of an external speaker or headphones.

Figure 5.1 shows the entire power amplifier-speaker circuit.

5.2 Power Supply

There is nothing extremely novel about the power supply design. A 20V-1A transformer is used to step down the standard 120 VAC voltage to an appropriate level. A full wave diode bridge is used to rectify the transformer secondary output signal and a pair of 4700 uF



5.1 POWER AMPLIFIER AND SPEAKER

capacitors are used to provide preliminary filtering. The capacitors are connected in series and the point between them, which is tied to the centre tap of the transformer secondary, is the designated common or ground for the entire electronic circuit.

If the ground point is designated as 0V, then the potentials at the extreme ends of the filter capacitors are approximately +13V and -13V. The transformer was specifically chosen to produce this potential after rectification and filtering. The reason is that some of the voltage regulators used in the circuit require at least 8V to maintain line regulation and some of them are damaged if the input voltage exceeds 25V. The chosen regulator input potential of ±13V is therefore both adequate and safe for all of the regulators used in the circuit.

Since high quality integrated circuit voltage regulators are now extremely inexpensive (approximately $3.50 for the negative and $1.70 for the positive ones chosen), a total of six of them are used in the synthesizer. All of the analog circuitry except for the power amplifiers and two op-amps is supplied by a pair of regulators at +5V and -5V. An additional regulator at +6V provides the positive supply for the previously mentioned op-amps which must be able to deliver up to +4.85V at their output terminals to control some voltage controlled osciallators. Since the internal biasing of the op-amps used requires about .6V, the +5V regulator can obviously not meet their needs.

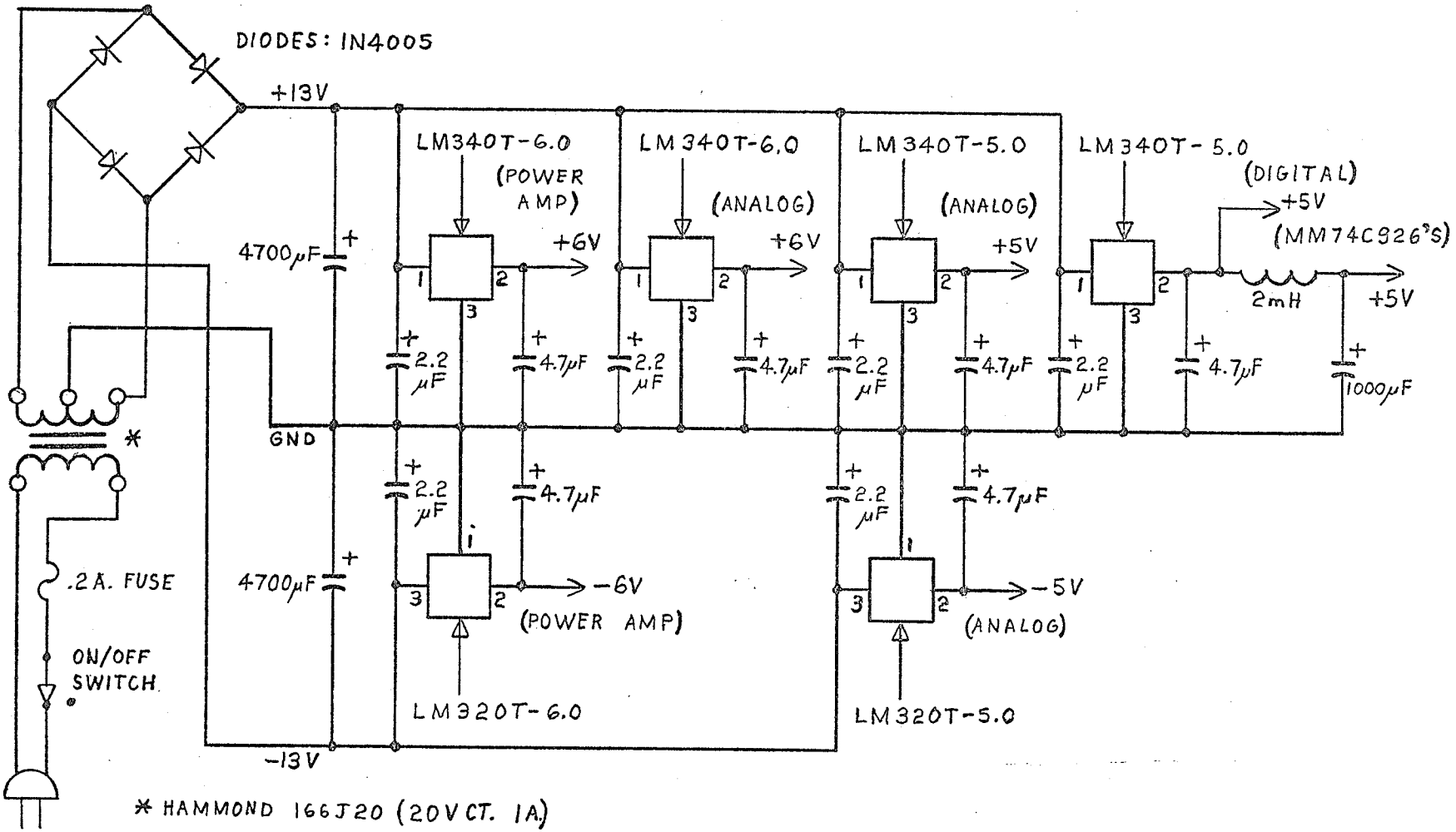
The power amplifier has its own pair of regulators at +6V and -6V. The reason for this is the amplifier draws a considerable amount of current and it draws it in pulses as the notes are played. This sudden loading of the regulator outputs could cause as much as a 250mV change in the IC supply voltage which would unnecessarily disturb the other analog circuitry if the same regulators were to be used for all of the analog integrated circuits.

Finally, the digital circuitry is supplied by its own separate +5V regulator. This is done to decrease the amount of contamination of the analog signals by voltage spikes which are fed into the analog circuitry through the supply lines from the digital integrated circuits. In fact, so great was the effect of the multiplexers in the counter/drivers on the rest of the circuitry that it was necessary to isolate them further by inserting an inductor and a capacitor. Only then was the supply line transmitted noise brought to an acceptably low level.

The entire power supply circuit is shown in Figure 5.2.

5.3 Protection Circuitry

The MM74C926 counter/driver, though very versatile in most respects, has a rather limited supply voltage range when compared to most CMOS integrated circuits. It operates with a supply of 3V to 6V and has an absolute maximum rating of 6.5V beyond which it could be damaged. Since the MM74C926 is also relatively expensive ($15 each) and there are six of them in the synthesizer, it seemed a rather prudent idea to include some circuitry which would protect them should the voltage regulator fail and the output rise to the regulator input potential of +13V.

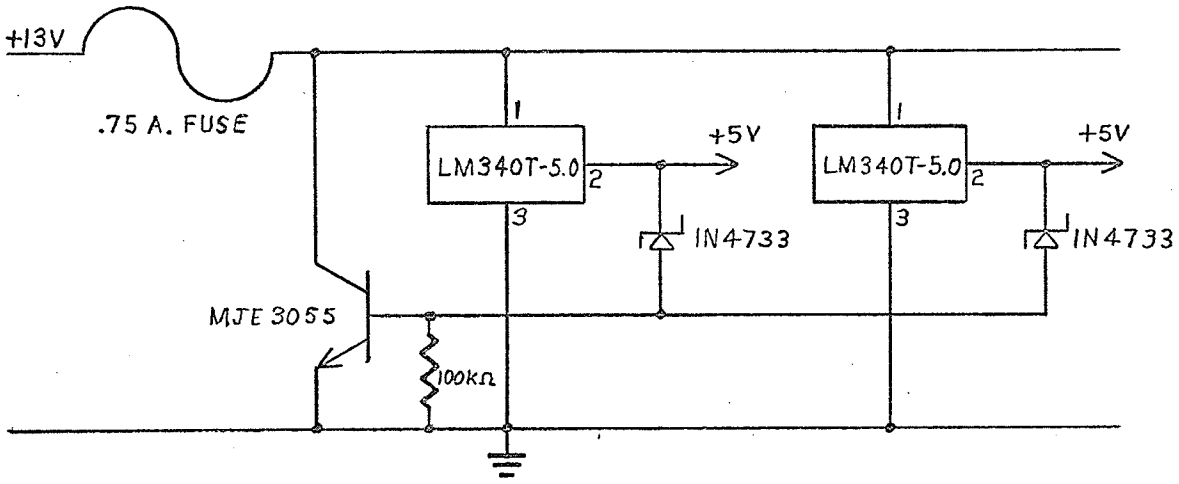


5.2 POWER SUPPLY

The protection circuitry consists of a 3/4A fast-blow fuse inserted into the +13V line, a 10A power transistor, and a 5.1 volt zener diode. The elements are installed in such a way that if the +5V digital regulator output goes higher than 5.1 volts, the zener turns on the power transistor which immediately blows the fuse.

It was then determined that with the addition of one more 5.1V zener diode at the output of the +5V analog regulator, all of the analog circuitry would also be protected since the analog integrated circuits will not be damaged unless both of the +5V and -5V regulators would fail and go to their respective input voltage values of +13V and -13V.

The complete protection circuitry and its position within the power supply is shown in Figure 5.3.



5.3 PROTECTION CIRCUITRY

VI TESTING

The following chapter examines the testing of the completed rhythm synthesizer. Specifically, it describes:

(a) the apparatus used to perform the testing,

(b) the testing procedure that was employed, and

(c) the quantitative results of the testing.

6.1 Apparatus

The following equipment was used in the testing of the completed rhythm synthesizer:

Philips PM3210 Dual Trace Oscilloscope

Advance Instruments TC9A Timer-Counter

(accuracy: ±5ppm after 20 minute warm-up)

HP3476A Digital Multimeter

(accuracy: DC volts - ±.3%

AC volts - ±1.5%

AC amps - ±2%)

It should be noted here that Hewlett-Packard (HP) is one of the most highly respected manufacturers of precision electronic test equipment in the world. Their product specifications are generally very conservative. For example, the DC volts mode of the HP3476A was measured on a standard voltage cell in the University of Manitoba's Standards Laboratory and was found to have an accuracy of better than .1% (limit of the digital readout). This value is at least three times better than the published specification.

6.2 Procedure

The synthesizer was tested using the equipment listed in section 6.1. Frequency measurements were made using the counter mode and duration measurements were made using the timer mode of the TC9A Timer-Counter. AC amplitude measurements were made using the oscilloscope

and the AC volts mode of the HP multimeter. DC voltage levels were measured using the DC volts mode of the HP multimeter. Finally, in order to determine the power consumption, an assumed input voltage value of 120VAC was combined with current readings obtained by using the AC amps mode of the HP multimeter.

6.3 Results

After calibration (as described in Appendix F), the entire synthesizer circuitry was tested a number of times over a period of about a week. The data from all of the tests was compiled, analyzed, and is presented in the following paragraphs.

Since the timer in the sample time control directly affects the accuracy of all of the readouts except for those corresponding to durations, it is undoubtedly the most critical part of the synthesizer in terms of the need for precise calibration. It was found that immediately upon being turned on, the timer value was generally about .25% high or around .50125 seconds rather than .5 seconds. However, after a warm-up period of about ten minutes, it settled to an accuracy of better than ±.05%.

The main system clock was found to produce clock rates of around 26 to 330 beats per minute. The corresponding display reading is taken directly from the output of the clock VCO. Therefore, the accuracy of the notes per minute readout is within ±.05 of the reading plus ±.5 in the least significant digit (LSD). The ±.5 in the LSD is digitization round off error which can be drastically decreased by careful operator adjustment of the controls.

When measured directly, it was found that the oscillators produced frequencies from about 90Hz to 4kHz with the greatest stability and controllability being in the range of 90Hz to 1kHz. The rms values of the oscillator output signals remained constant throughout the desired frequency range dropping only about .3db at 1kHz due to the effect of the output low-pass filter. As was the case in the clock readout, the accuracy of the frequency readout is dependent upon the accuracy of the timer in the sample time control circuit. Taking the warmed up value of ±.05% and keeping the digitization error in mind, we find that the worst inaccuracy is at 1kHz where the readout value is within ±1Hz of the actual frequency. At 100Hz, the accuracy is within ±.55Hz of which ±.5Hz is due to round off error.

The amplitude of the output as modified by the variable amplifier was found to be adjustable from about 38% to 240% of the amplitude of the fixed amplifier. The output of the AC to DC converter was exactly proportional (within the accuracy of the HP multimeter) to the rms value of the signal over the entire range of ±6db. Since the amplitude display circuitry is designed essentially the same as the clock display, the accuracy of the amplitude readout in the range of 50% to 200% is within ±.05% of the reading (if the multimeter readings are taken to be exact) plus ±.5 in the LSD.

The modified duration timers were found to produce pulse widths of 0 to about 2.2 seconds. Since the timers produce their own reset and latch enable pulses there is essentially no sample time error. However, since the duration VCO and the clock VCO are controlled

by the same voltage (section 4.5), there is some error introduced into the duration readout by the mistracking of the two voltage controlled oscillators due to slight differences in their voltage-frequency curves. It was found that from clock rates of 30 to 300 beats per minutes, the duration VCO output frequency inaccuracy was never more than ±1% of the reading. It should be noted that though the absolute error relative to the system clock readout is within ±1%, since both of the duration displays use the same VCO for their counter/driver clock inputs, the relative error between the two duration readouts is zero. In addition, there is also the ±.5 in the LSD inaccuracy.

The maximum rms signal-to-noise ratio of the synthesizer, as measured by the AC volts mode of the HP multimeter and checked on the oscilloscope was found to be about 70 db. This value was determined with the amplifier gain at maximum. With the synthesizer output adjusted to volumes which were comfortably room filling, the rms signal-to-noise ratio was between about 50 and 60 db.

The average power consumption of the synthesizer is about 17 watts.

VII CONCLUSIONS

An electronic rhythm synthesizer has been designed, constructed and tested. The accuracy and precision of all major components of the synthesizer are extremely high - definitely beyond the limits of human detection and, in some cases, beyond the limits of high quality test instruments.

It is sincerely hoped that all of the requirements and expectations of the School of Music of the University of Manitoba have been met or exceeded and that the synthesizer will simplify, as much as possible, the technical aspects of their forthcoming series of rhythm perception experiments.

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APPENDIX A

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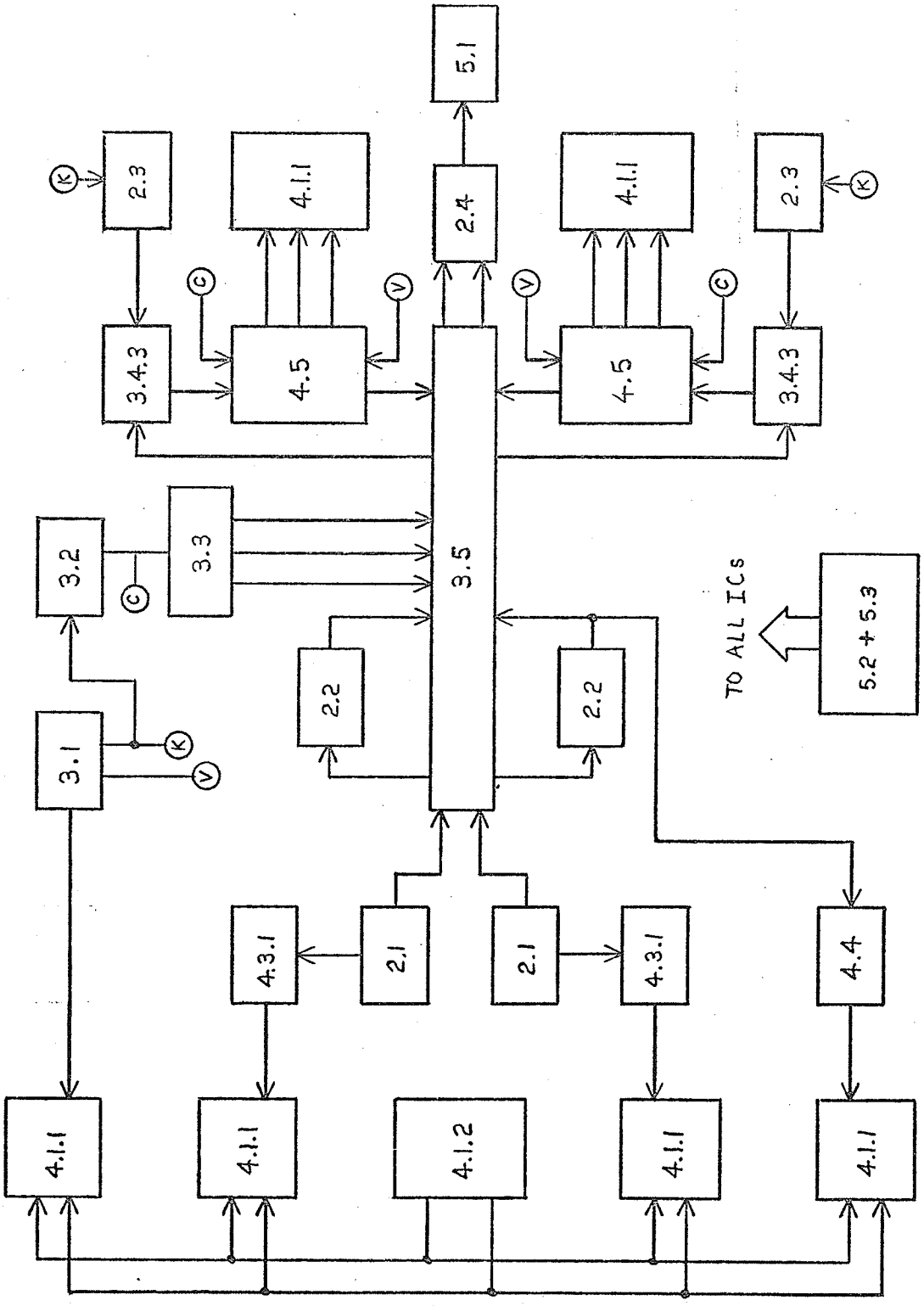
APPENDIX B

SYNTHESIZER BLOCK DIAGRAM



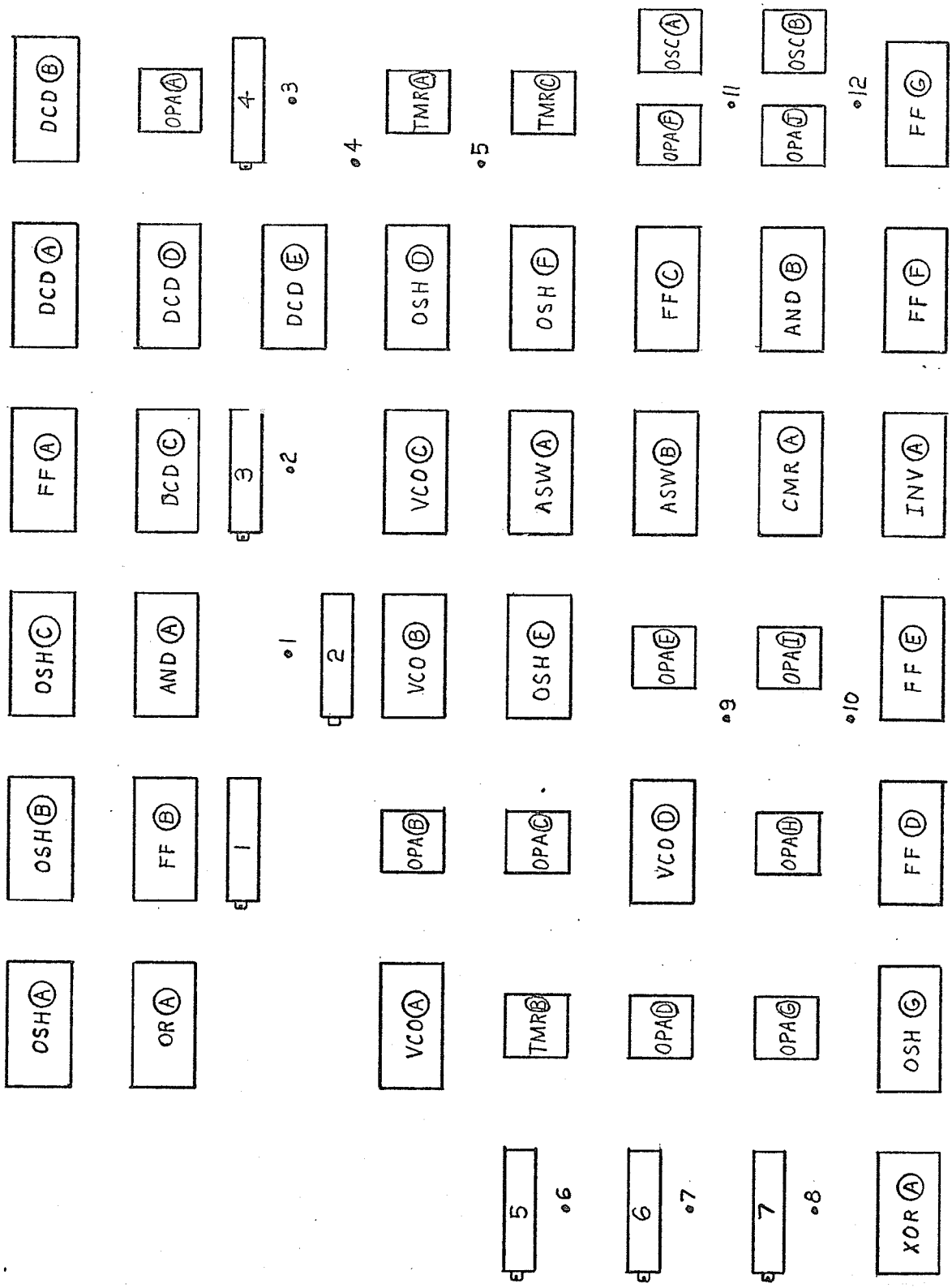
APPENDIX C

LIST OF IC's

LABEL	DESCRIPTION	PART NUMBER
FF	Dual D flip-flop	CD4013
DCD	Decade counter/divider	CD4017
XOR	Quad EXCLUSIVE-OR	CD4030
ASW	Quad bilateral switch	CD4066
INV	Hex inverter	CD4069
AND	Quad 2-input AND	CD4081
OR	Quad 2-input OR	MM74C32
OSH	Dual one-shot	MM74C221
	4 digit counter/driver	MM74C926
CMP	High speed dual comparator	LM319
	-5 volt regulator	LM320T-5.0
	-6 volt regulator	LM320T-6.0
	+5 volt regulator	LM340T-5.0
	+6 volt regulator	LM340T-6.0
	Dual 4 watt audio amplifier	LM378
VCO	Phase locked loop	LM565
OSC	Voltage controlled oscillator	LM566
TMR	Precision timer	LM3905
OPA	Operational amplifier	LM741

APPENDIX D

LAYOUT OF ICS



APPENDIX E

DATA ON THE MM74C926

MM74C925, MM74C926, MM74C927, MM74C928
4-digit counters with multiplexed 7-segment output drivers

general description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

features

- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- High segment sourcing current — 40 mA @ V_{CC} – 1.6V, V_{CC} = 5V
- Internal multiplexing circuitry

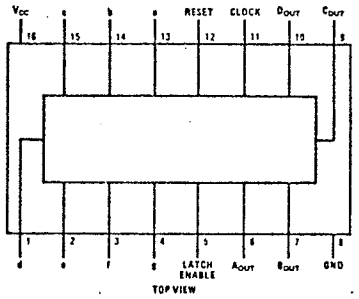
design considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DM75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

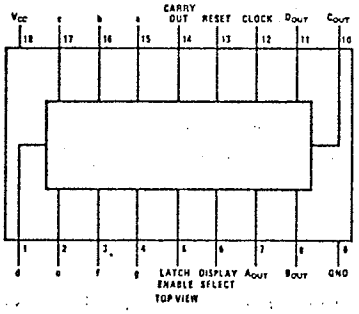
The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

connection diagrams

Dual-In-Line Package
MM74C925



Dual-In-Line Package
MM74C926, MM74C927 and MM74C928



functional description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

Segment Output — Current sourcing with 80 mA @ V_{OUT} = V_{CC} – 1.6V typical. Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @ V_{OUT} = 1.75V. Also, sink capability = 2 LTTL loads

Carry-out — 2 LTTL loads. See carry-out waveforms.

absolute maximum ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V
Voltage at Any Input Pin	Gnd − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply at −40°C ≤ T_j ≤ +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20		Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{JA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

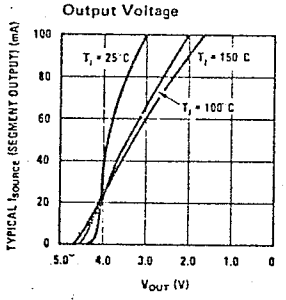
Note 4: θ_{JA} measured in free-air with device soldered into printed circuit board.

ac electrical characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified

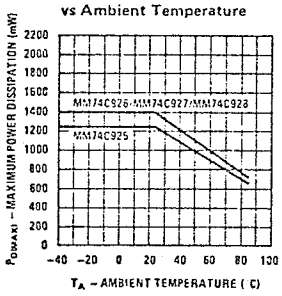
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5.0V,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	V_{CC} = 5.0V				15	μs
t_{WR}	Reset Pulse Width	V_{CC} = 5.0V	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	V_{CC} = 5.0V	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	V_{CC} = 5.0V	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	V_{CC} = 5.0V	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	V_{CC} = 5.0V	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	V_{CC} = 5.0V			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

typical performance characteristics

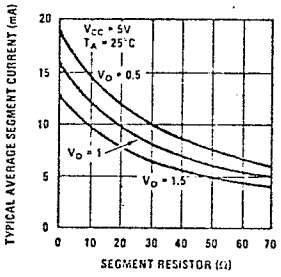
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature



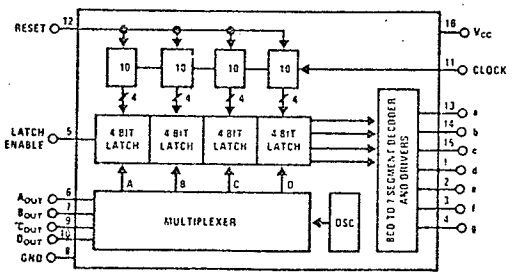
Typical Average Segment Current vs Segment Resistor Value



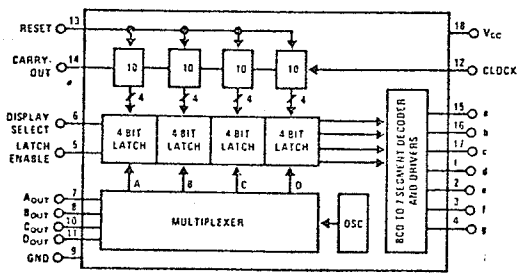
Note. V_D = Voltage across digit driver.

logic and block diagrams

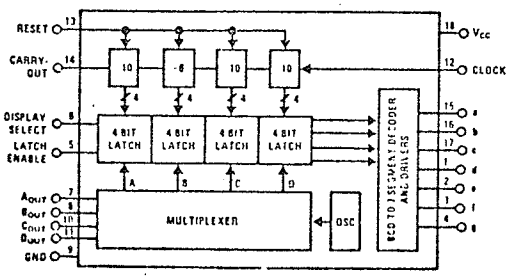
MM74C925



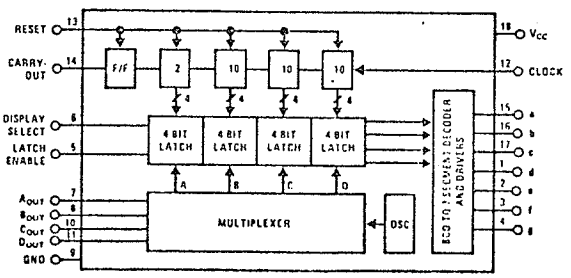
MM74C926



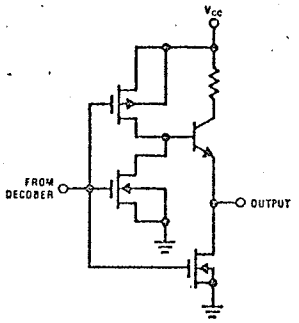
MM74C927



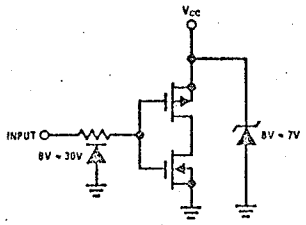
MM74C928



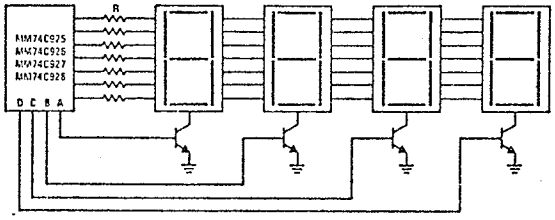
Segment Output Driver



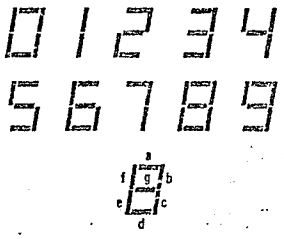
Input Protection



Common Cathode LED Display

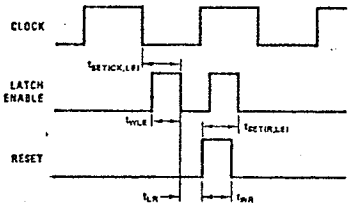


Segment Identification

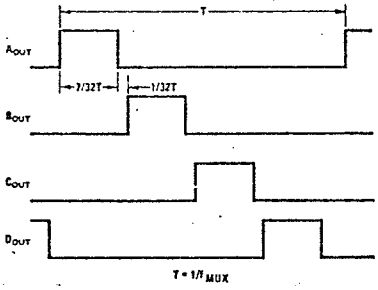


switching time waveforms

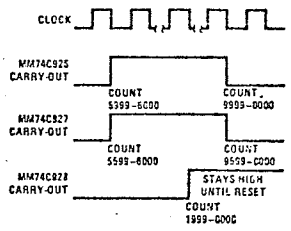
Input Waveforms



Multiplexing Output Waveforms



Carry-Out Waveforms



APPENDIX F

DATA ON THE ANALOG SWITCHES

CD4066BM/CD4066BC quad bilateral switch

general description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

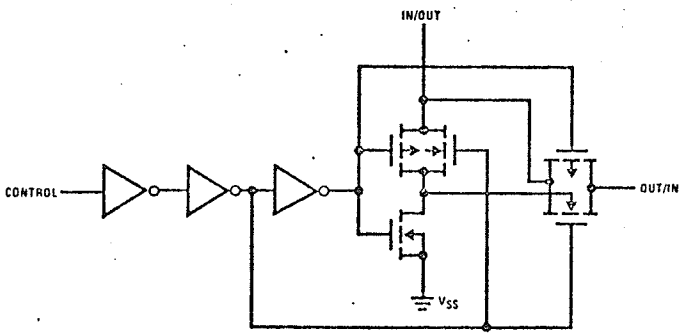
features

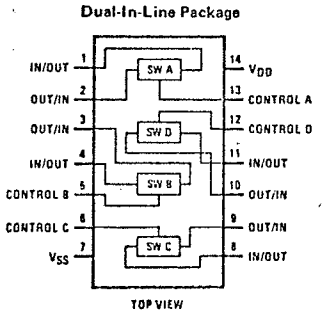
- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω typ
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity — < 0.4% distortion typ @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω typ
- Low crosstalk between switches — −50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz typ

applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

schematic and connection diagrams





absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

dc electrical characteristics CD4066BM (Note 2)

	PARAMETER	CONDITIONS	−55°C MIN	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.01	0.5		15	μA
		V_{DD} = 15V		1.0		0.01	1.0		30	μA
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ								
		V_C = V_{DD} V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V		220		80	280		320	Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V		400		120	500		550	Ω
		10V 0V 0V to 10V								
		2.5V −2.5V −2.5V to +2.5V		3000		270	5000		5500	Ω
		5V 0V 0V to 5V								
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	R_L = 10 kΩ								
		V_C = V_{DD} V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V				5				Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V				10				Ω
		10V 0V 0V to 10V								
I_{OFF}	Input or Output Leakage Switch "OFF"	V_{DD} V_C = V_{SS} V_{is} V_{os}								
		7.5V −7.5V ±7.5V 0V		±50		±0.1	±50		±500	nA
		5V −5V ±5V 0V		±50		±0.1	±50		±500	nA
CONTROL INPUTS										
V_{IL}	Low Level Input Voltage	V_{is} = V_{DD}, V_{os} = V_{SS}, $I_{is} \leq 10\,\mu A$								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V		3.5		2.75	3.5		3.5	V
		V_{DD} = 10V		7.0		5.5	7.0		7.0	V
		V_{DD} = 15V		11.0		8.25	11.0		11.0	V
I_{IN}	Input Current	V_{DD} − V_{SS} = 15V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
		$V_{DD} \geq V_{is} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

dc electrical characteristics CD4066BC (Note 2)

	PARAMETER	CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.01	2.0		15	μA
		V_{DD} = 15V		4.0		0.01	4.0		30	μA

dc electrical characteristics (Continued) CD4066BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	R_L = 10 kΩ								
		$V_C = V_{DD}$ V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V		250		80	280		300	Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V		450		120	500		520	Ω
		10V 0V 0V to 10V								
		2.5V −2.5V −2.5V to +2.5V		3500		270	5000		5200	Ω
		5V 0V 0V to 5V								
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	R_L = 10 kΩ								
		$V_C = V_{DD}$ V_{SS} V_{is}								
		7.5V −7.5V −7.5V to +7.5V				5				Ω
		15V 0V 0V to 15V								
		5V −5V −5V to +5V				10				Ω
		10V 0V 0V to 10V								
I_{OFF}	Input or Output Leakage Switch "OFF"	V_{DD} $V_C = V_{SS}$ V_{is} V_{os}								
		7.5V −7.5V ±7.5V 0V		±50		±0.1	±50		±200	nA
		5V −5V ±5V 0V		±50		±0.1	±50		±200	nA
CONTROL INPUTS										
V_{IL}	Low Level Input Voltage	$V_{is} = V_{DD}$, $V_{os} = V_{SS}$, $I_{is} \leq 10\ \mu A$								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V	3.5			2.75	3.5		3.5	V
		V_{DD} = 10V	7.0			5.5	7.0		7.0	V
		V_{DD} = 15V	11.0			8.25	11.0		11.0	V
I_{IN}	Input Current	$V_{DD} - V_{SS}$ = 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
		$V_{DD} \geq V_{is} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

ac electrical characteristics T_A = 25°C, $t_r = t_f$ = 20 ns and V_{SS} = 0V unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, C_L = 50 pF, *(Figure 1)*				
		V_{DD} = 5V		25	55	ns
		V_{DD} = 10V		15	35	ns
		V_{DD} = 15V		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	R_L = 10 kΩ, C_L = 50 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	60	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	R_L = 10 kΩ, C_L = 5 pF, *(Figures 2 and 3)*				
		V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		55	110	ns
	Sine Wave Distortion	$V_C = V_{DD}$ = 5V, V_{SS} = −5V, R_L = 10 kΩ, V_{is} = 5 Vp-p, f = 1 kHz, *(Figure 4)*		0.4		%
	Frequency Response—Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD}$ = 5V, V_{SS} = −5V, R_L = 1 kΩ, V_{is} = 5 Vp-p, 20 $\text{Log}_{10} V_{OS}/V_{is}$ = −3 dB, *(Figure 4)*		40		MHz

ac electrical characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Feedthrough – Switch "OFF" (Frequency at –50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{is} = 5$ Vp-p, 20 Log_{10} $V_{os}/V_{is} = -50$ dB, *(Figure 4)*		1.25		MHz
	Crosstalk Between Any Two Switch (Frequency at –50 dB)	$V_{DD} = V_{C(1)} = 5V$; $V_{SS} = V_{C(2)} = -5V$, $R_L = 1\ k\Omega$, $V_{is(A)} = 5$ Vp-p, 20 Log_{10} $V_{os(2)}/V_{is(1)} = -50$ dB, *(Figure 5)*		0.9		MHz
	Crosstalk: Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, *(Figure 6)*		400		mVp-p
	Maximum Control Input Frequency (f at V_{os} = 1/2 V_{DD}p-p)	$R_L = 1\ k\Omega$, $C_L = 50$ pF, *(Figure 7)*				
		$V_{DD} = 5V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{is}	Signal Input Capacitance			8		pF
C_{OS}	Signal Output Capacitance			8		pF
C_{ios}	Feedthrough Capacitance			0.5		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

ac test circuits and switching time waveforms

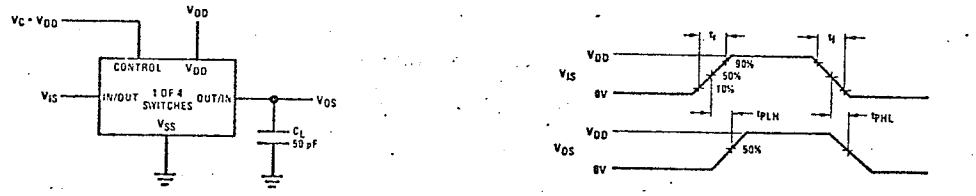


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

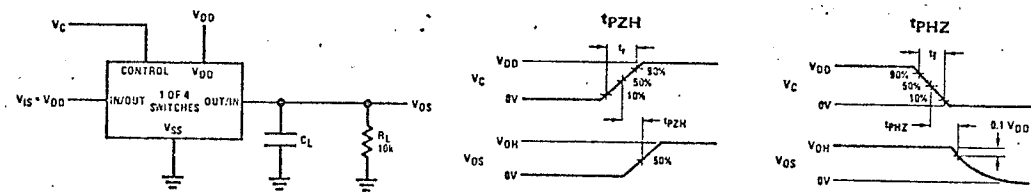


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

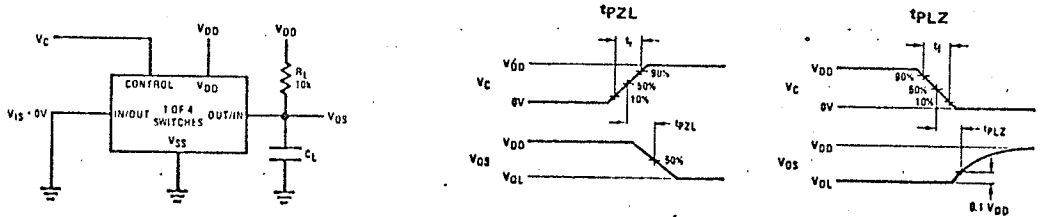
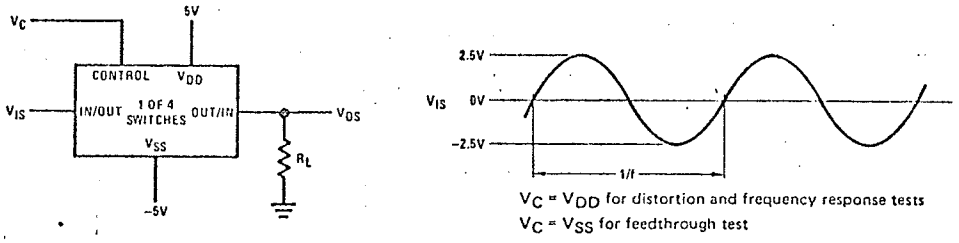


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

ac test circuits and switching time waveforms (Continued)



$V_C = V_{DD}$ for distortion and frequency response tests
$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

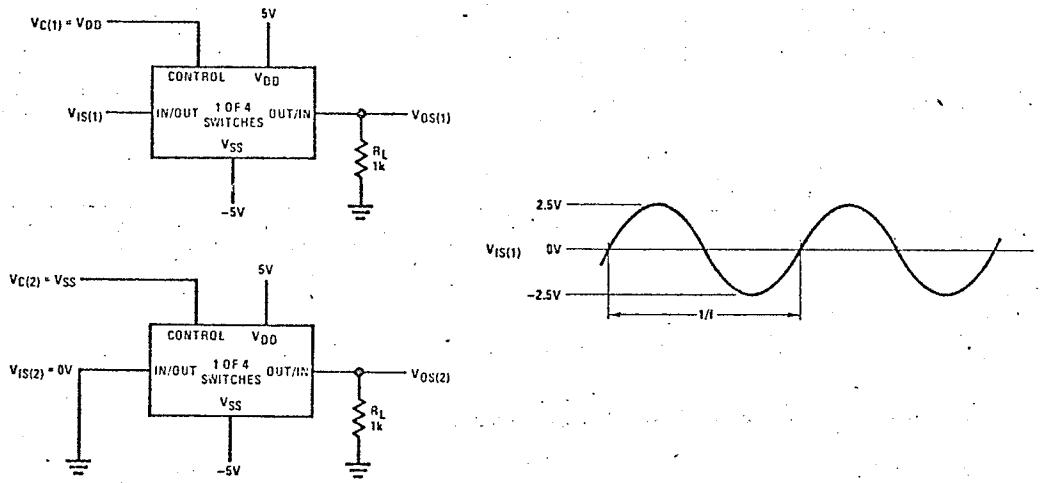


FIGURE 5. Crosstalk Between Any Two Switches

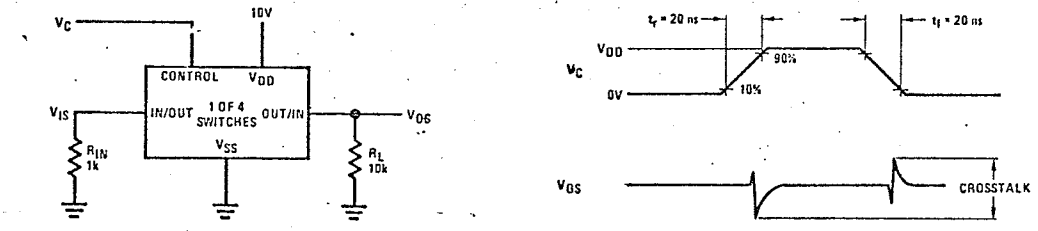


FIGURE 6. Crosstalk: Control Input to Signal Output

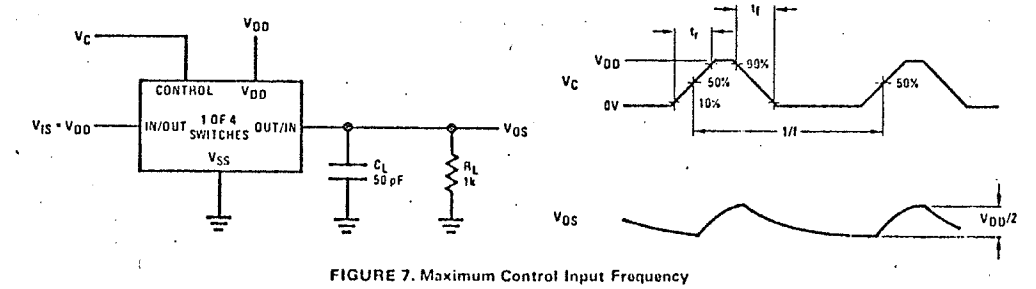
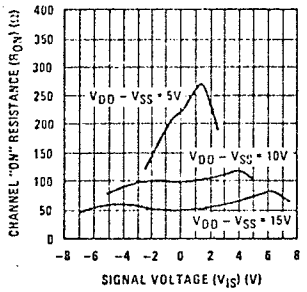


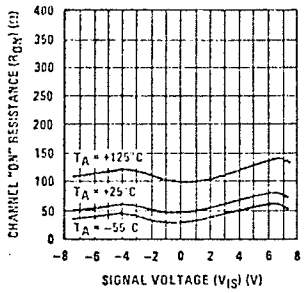
FIGURE 7. Maximum Control Input Frequency

typical performance characteristics

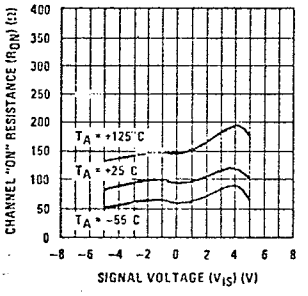
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



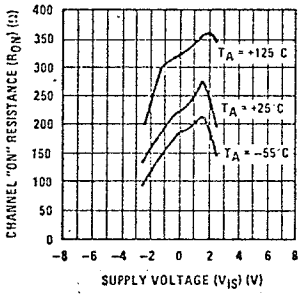
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



special considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

APPENDIX G

CALIBRATION OF THE SYNTHESIZER

Calibration of the circuitry as well as some simple modifications are very easy to perform. If the front panel is unscrewed and lifted off of the base, one will find the main circuit board attached to the front panel with the IC side facing outward. Besides the IC's, there are also a number of ten-turn trimpots and accessible circuit test points (see Appendix D for locations) on this side of the board. Before beginning calibration, one should first turn on the power switch and let the circuit stand for about 10 or 15 minutes to enable all of the components to stabilize at their final operating temperature. It should be noted that actually the only part of the circuit that requires a warm-up time for optimum accuracy is the sample time control. The design of the circuit is such that, in general, if part of the circuit should drift because of temperature, aging or any other cause, this change will be reflected immediately by a change in the corresponding display value and the operator can compensate for the drift by readjusting the appropriate potentiometer on the front panel.

Calibration Procedure

I To test point 6, attach a timing instrument that is adjusted to measure the duration of single positive pulses. Adjust trimpot 5 so that the timer reading is exactly .5 seconds. This calibrates the timer in the sample time control circuit.

II Attach a DC voltmeter to test point 3. Rotate both notes per minute panel pots fully counter-clockwise. Adjust trimpot 4 so that the voltmeter reading is 4.85 volts. This is the upper voltage limit of the linear portion of the clock VCO.

Adjust the panel pots so that the voltage at test point 3 is 4.8 volts. To test point 2, attach a timing instrument that is adjusted to start and stop timing on the rising edge of the signal in order to determine the duration of a single complete cycle. Adjust trimpot 3 so that the timer reading is the time of the lowest notes per minute value desired. For example, at 30 notes per minute the timer would read 2 seconds. The lower limit of the notes per minute control is now set. The upper limit is fixed at approximately 10 times the lower limit.

III With the equipment still connected as in II, adjust the notes per minute panel pots so that the timing instrument reads exactly 1 second. Attach a frequency counter to test point 1 and adjust trimpot 2 so that the frequency is exactly 100Hz. The duration readouts are now calibrated to read in percent of the notes per minute readout.

IV Attach an AC voltmeter to test point 9 and note the reading. Attach the AC voltmeter to test point 10 and adjust the secondary amplitude panel pots so that the voltage reading at test point 10 is the same for test point 9. Attach a DC voltmeter to test point 8. Adjust trimpot 7 for a reading of 4 volts. The amplitude display

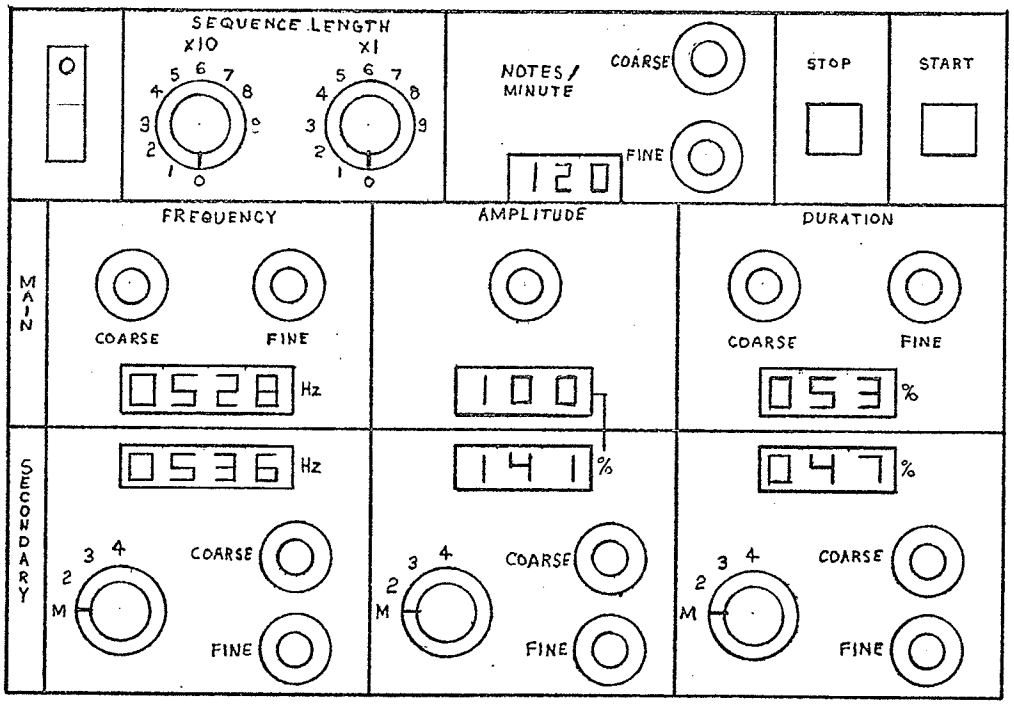
interface VCO control voltage is now set for optimum use of the VCO linear region.

Without readjusting anything, attach a frequency counter to test point 7. Adjust trimpot 6 so that the frequency output is exactly 200 Hz. The amplitude display interface is now calibrated.

V Redo I.

APPENDIX H

CONTROL PANEL OF SYNTHESIZER



1/2 SCALE