INVESTIGATION OF THE PROPERTIES OF PLASMA ENHANCED CVD SILICON DIOXIDE AND ITS APPLICATIONS TO VLSI TECHNOLOGY

by

Yong Qiang Li

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in
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A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

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ABSTRACT

Investigations have been made in this thesis to study various properties of silicon dioxide (SiO_2) films prepared by plasma-enhanced chemical vapor deposition (PECVD) techniques with the deposition temperature in the range of 225–350°C. The properties investigated were oxide charges (mobile ionic charge, interface trap density and oxide fixed charge), dielectric breakdown, electron trapping and negative bias-temperature instability (NBTI). The experimental results showed that the electrical properties of PECVD SiO_2 are approaching those of thermally grown oxide. The densities of mobile ionic charge, oxide fixed charge and interface traps at midgap of the samples deposited at 225°C, 250°C, 275°C, 300°C, 325°C and 350°C were all on the order of 10^{10} cm^{-2} or $cm^{-2}eV^{-1}$ and breakdown field was higher than 5 MV/cm for most of the MOS capacitors tested after a standard postmetallization anneal (PMA) in forming gas ($10\%H_2$-$90\%N_2$ mixture) at 400°C for 30 min. The electron traps were found to be water-related and uniformly distributed in the PECVD SiO_2 and have much larger capture cross section (~$10^{-15}cm^2$) than those in thermally grown oxide (~10^{-20} cm^2). The NBTI in the PECVD SiO_2 were comparable to those in thermally grown oxide, although the NBTI was somewhat dramatic at high temperature if the surface of the samples was not kept clean.

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CHAPTER 1

INTRODUCTION

1.1 Background and Literature Review

VLSI devices with very small dimensions require very shallow junctions and high quality thin oxide film on silicon. High-temperature processing can cause dopant diffusion and growth control problems, which may become very serious as device dimensions shrink. Consequently high temperature processes are being replaced by low-temperature deposition techniques. One of the most widespread low-temperature deposition techniques is plasma-enhanced chemical vapor deposition (PECVD), where the additional energy supplied by a glow discharge promotes the chemical reaction.

For the generation of plasma, an electric discharge is generally used. In the low-temperature plasma, the energy of the electrons is larger than that of the ions or neutral particles and the whole system is thermally in a nonequilibrium state. Although the energy of the ions or neutral particles is relatively low, these particles become excited by colliding with electrons. This excited state is equivalent to a high-temperature state, and the effective reaction can thus proceed at a low temperature.

The enhancement of a chemical reaction by an electrical discharge through gases has been known for over a century. The process has had very few applications because the phenomena are so complex and so difficult to obtain the desired high enough yield to compete with other preparative methods. Only in recent years have requirements in microelectronics research risen that

low-temperature PECVD technology for thin film preparation has no real competition.

The substitution of electron kinetic energy for thermal energy in effecting the reaction can avoid excessive heating and consequent degradation of the substrate structure encountered in conventional chemical vapor deposition techniques which usually require 700–900°C either during deposition or later annealing, and such temperatures would cause intolerable stress, interdiffusion, or outright melting in device structures in the late stages of their fabrication.

The insulating films prepared by PECVD techniques at very low temperature (≤350°C) have many applications in the fabrication of semiconductor devices. They are likely to be widely used as: (1) an electrical insulator between conducting layers; (2) a secondary passivation layer for protection from the environment; (3) a diffusion and ion implantation mask; and possibly (4) a gate insulator for MOS device application.

Although study of plasma-enhanced deposition for microelectronic uses was first reported 25 years ago[1], it took ten more years for the technique to be used in the semiconductor industry with the advent of Reinberg radial-flow reactor[2]. Reactions in the plasma are very complicated. The effect of a variable is usually separable from the effects of many others only over a narrow range. This results in a largely empirical operation and control of plasma processing. Early research has concentrated on the reproducibility of film thickness and composition, which are closely related to many operating parameters[3].

A large number of materials can be deposited by PECVD techniques but only two are widely used in VLSI technology:

PECVD silicon nitride (Si_3N_4) and PECVD silicon dioxide (SiO_2). The former is generally superior to the latter in physical, mechanical and chemical properties such as pinhole density, stress and etch resistance but inferior to the latter in electrical properties and far from ideal for use as a gate insulator. Electronic conduction, even in high quality Si_3N_4, is complex. Both electron and hole injection are important and a high density of bulk traps modulates the conductivity. This leads to an inherent problem in control of threshold voltage and stability. In contrast, electronic quality SiO_2 has much more desirable properties. Conduction is essentially single carrier and interface limited by Fowler-Nordheim (F-N) injection.

The conventional approach to PECVD is based on radial-flow, parallel plate reactor, with a deposition chamber as shown schematically in Figure 1.1. It is a cylinder, usually glass or aluminum, with aluminum plates on the top and bottom. Samples lie on the bottom electrode, which is grounded. A radio frequency voltage is applied to the top electrode to create a glow discharge between the two plates that contains a gas mixture appropriate for the growth of a particular insulating film. Gases flow radially through the discharge. They are usually introduced at the outer edge and flow towards the center. The gases are pumped with a Roots blower backed by a mechanical pump. The grounded electrode is heated to a temperature between 100 and $400^o C$ by resistance heaters or high-intensity lamps[4].

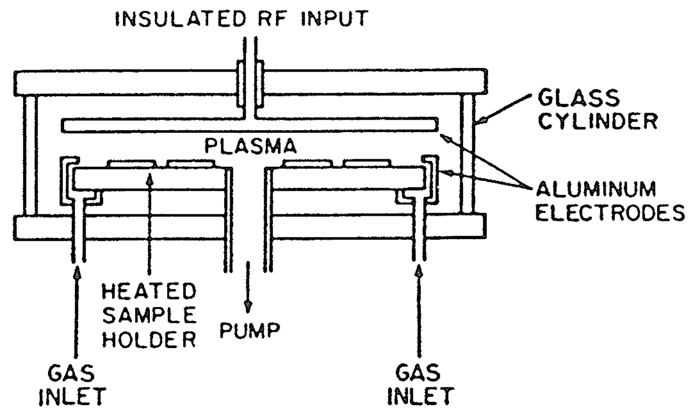

Figure 1.1 Schematic representation of PECVD deposition chamber[4].

Silicon dioxide films are usually deposited from gas mixtures of SiH_4 and either N_2O or O_2. Typically, nitrous oxide (N_2O) has been the oxidant of choice[5-10]. With the exceptions of SiO_2 films deposited from an electron cyclotron resonant microwave plasma[11-13], oxygen (O_2) is generally not used in conventional PECVD due to its high reactivity with silane (SiH_4), which may result in a general reduction in film quality, including nonreproducible deposition, increased particulates and pinhole densities, and nonuniform deposition[5][7].

A large number of researchers have explored the growth of PECVD SiO_2 films. But little has been done in the past to study the electrical stability and $Si-SiO_2$ interface quality because radiation damage from the plasma was expected to degrade these properties and resistivity, interface charge, dielectric strenth, etc. These could strongly depend on deposition variables. Instead, the structure-composition-property correlation in PECVD SiO_2 films has been extensively studied using infrared spectra, index of refraction and chemical etch rate[4-19]. Usually, PECVD films contain large hydrogen concentrations, which depend on the deposition conditions[20-23]. The total hydrogen concentration is often reported as atom percent hydrogen at.% H. Converting concentrations from atom/cm^3 to at.% H requires knowledge of the film density. Reported densities are 2.2 to 2.5 g/cm^3 for SiO_2. Therefore, it is necessary to measure the density for the specific deposition conditions before at.% H is calculated. The hydrogen is bonded to silicon as Si-H and to oxygen as Si-OH and H_2O. The relative concentration of hydrogen in the three bonding sites strongly depends on deposition conditions; however, the total hydrogen only varies between 2 and 9 at.% in PECVD SiO_2

films[4]. The consequences of the hydrogen content are not all clear, but among the properties certainly affected are electrical stability, film stress, and gas evolution upon heating[24]. Chemical etch rate is influenced also[21]. Helium dilution may be used to eliminate hydrogen in radio frequency PECVD SiO_2 films[17]. SiO_2 films prepared from SiH_4/N_2O/He gas mixtures in a radio frequency plasma may contain virtually no ($\leq$1.0 at.%) H[25][26].

An alternative technique to conventional PECVD, which is called remote or downstream PECVD, has been also proposed to avoid direct exposure of the samples to a more energetic gas environment during deposition[27]-[29]. A schematic representation of the deposition system is shown in Figure 1.2. The process is a variation of conventional PECVD process in which only one of the constituent gases, the oxygen or nitrogen containing molecule or a mixture of this gas with a rare gas, is excited by a radio frequency voltage and then mixed with neutral SiH_4. Because of the location of the sample, relative to the discharge zone, the process is expected to be more gentle. In addition to reduction of radiation damage from the plasma, elimination of gas phase plasma reactions that generate precursor species which in turn could introduce unwanted bonding groups in the deposited films is anticipated by not directly plasma exciting the SiH_4.

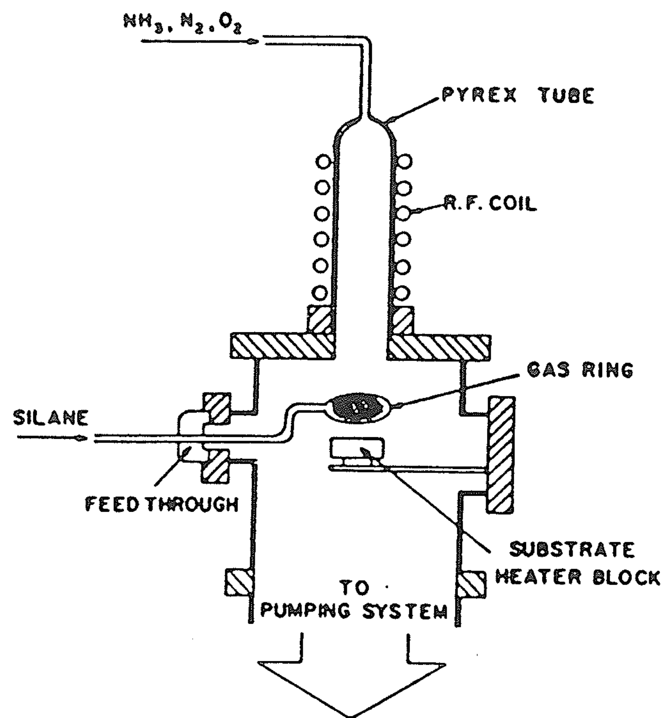

Figure 1.2 Schematic representation of remote PECVD deposition chamber[16].

Only very recently, however, have there been reports of high-electronic-quality SiO_2 films grown by low-temperature PECVD[26][30]. Low-temperature PECVD SiO_2 films are approaching the quality of high-temperature thermally grown oxides when these layers are used as the gate dielectric in metal-oxide-semiconductor field-effect transistor (MOSFET) devices[30]. Therefore, interest has been increased in the study of PECVD SiO_2 as a gate insulator. The research work conducted in this thesis is motivated by this trend.

1.2 Research Scope and Purpose

It is only recently that PECVD SiO_2 has been seriously considered for the application in MOS device technology as a gate insulator, although thermally grown SiO_2 has been used as a perfect gate dielectric for a long time. The application requires control of physical, mechanical and chemical properties as well as electrical properties of PECVD SiO_2. It must be stated that the study of the deposition of electronic quality SiO_2 on silicon by PECVD techniques has just begun. Much work has to be done to clarify the process taking place in the formation of SiO_2 in the plasma and to explain the properties unique to PECVD SiO_2. In this thesis, various properties of PECVD SiO_2 have been studied with compared to those of thermally grown oxide. The mechanisms were briefly investigated. More accurate and fuller study of the mechanisms are left as extension of the work done in this project.

1.3 Organization of the Thesis

The rest of the chapters of this thesis is organized as follows:

Chapter 2 provides the experimental methods to measure the oxide charge (mobile ionic charge, interface trap density and oxide fixed charge) and dielectric breakdown characteristics using metal-oxide-semiconductor (MOS) capacitors. The results from capacitance-vs-voltage (C-V) measurements and ramp current-vs-voltage (I-V) measurements are presented. Mobile ionic charge, interface trap density and oxide fixed charge are calculated and compared to the counterparts of thermally grown oxide.

Chapter 3 presents a study of electron trapping in PECVD SiO_2. Electron trapping parameters such as capture cross section and trapping probability are presented. The centroid of electron trap distribution is obtained using combined ramp current-vs-voltage (I-V) and high-frequency capacitance-vs-voltage (C-V) technique. The effects of deposition temperature and postmetallization anneal (PMA) on the properties of electron traps are also investigated.

Chapter 4 presents the experimental results of negative bias-temperature instability (NBTI) in MOS capacitors incorporating PECVD SiO_2. Two sets of stressing conditions are used in the study, namely, room temperature negative bias stressing and high temperature ($200^o C$) negative bias stressing. The mechanism for the generation of positive charge under stressing is investigated.

Chapter 5 presents the conclusions of the thesis and points out the direction for future research.

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CHAPTER 2

ELECTRICAL PROPERTIES OF PECVD SiO_2

2.1 Introduction

For thin SiO_2 films to be considered for gate insulator purposes, two major properties are of paramount importance: the level of mobile ionized sodium contamination and the dielectric breakdown strength. Also, there are two major electrical properties of the $Si-SiO_2$ interface: oxide fixed charge and interface trap density.

Oxide charges (mobile ionic charge, oxide fixed charge, interface trap charge and oxide trapped charge) adversely affect MOS device performance by changing the threshold voltage, decreasing the drain junction breakdown voltage and reducing the transconductance, etc., if present at high densities. They also pose a stability problem since their densities can change with time during device life. It is very important that these charges be controlled when MOS device are fabricated. Oxide dielectric breakdown strength must be high, or device operation will be adversely affected.

In this chapter, we first give a brief description of charges in metal-oxide-semiconductor (MOS) capacitors and the dielectric breakdown of SiO_2 and then explain the experimental methods to measure them. Finally experimental results are presented and conclusions are drawn.

2.2 Charges in MOS System

There are four types of charges which are of electrical importance to MOS devices. They are mobile ionic charge, oxide fixed charge, interface trap charge and oxide trapped charge. The spatial locations of these charges in MOS system are shown in Figure 2.1.

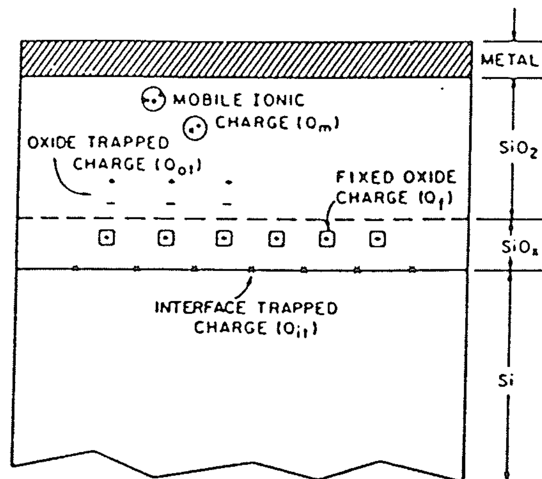

Figure 2.1 Spatial locations of the charges in MOS system[1].

Mobile ionic charge Q_m is most commonly caused by the presence of sodium ions. This type of charge is mobile and located either at the metal-SiO_2 interface, where it originally entered the oxide layer, or at the $Si-SiO_2$ interface, where it drifted under applied field at an elevated temperature.

Oxide fixed charge Q_f is the charge density remaining after interface trap charge is annealed out. It is located at or very near the $Si-SiO_2$ interface. In electrical measurements Q_f can be regarded as a charge sheet located at the $Si-SiO_2$ interface.

Interface trap charge Q_{it} is due to the defects located at the $Si-SiO_2$ interface, each of which has one or more energy levels within the silicon bandgap. These defects can exchange charges

with the silicon. Specifically, they can interact with the silicon conduction band by capturing or emitting electrons and with the valence band by capturing or emitting holes. Capture or emission occurs when interface traps change occupancy.

Oxide trapped charge Q_{ot} can be located not only at the metal-SiO_2 or $Si-SiO_2$ interfaces, but also deep in the oxide. The traps in the oxide, usually uncharged, but become charged when electrons or holes are trapped in them. The important parameters of these bulk traps are energy level (shallow or deep traps), density, capture cross section and distribution centroid. The oxide bulk traps and associated charge will be studied in the following chapter.

The features of the four charges are summarized in Table 2.1.

Table 2.1 Summary of the features of the charges in MOS system[2].

	Q_{it}	Q_{ot}	Q_f	Q_m
Spatial Location	within 10Å of $Si\text{-}SiO_2$ interface	throughout bulk and interfaces	very close to $Si\text{-}SiO_2$ interface	throughout bulk and interfaces
Energy Level	throughout bandgap	relatively shallow in SiO_2 bandgap	outside bandgap	shallowly trapped
Charge Sign	+/—	+/—	+	+
Typical Value	$\sim 10^{10} cm^{-2} eV^{-1}$	$\sim 10^{12} cm^{-2}$	$\sim 10^{11} cm^{-2}$	$\sim 10^{10} cm^{-2}$
Remark	charge density dependent on ψ_s	bulk charge	nature unknown	mobile

2.3 Dielectric Breakdown of SiO_2

The breakdown of an MOS capacitor can be divided into two types: extrinsic or defect-related breakdown and intrinsic breakdown. The defect may have been caused during manufacture by the incorporation of impurities or by the formation of hair-line cracks, asperities or pinholes. Defects may also be introduced when the gate is deposited. Breakdown at a defect will occur at a lower field-strength than intrinsic breakdown, i.e., breakdown for a film with no defects. In general, therefore, the breakdown field-strength of a device will decrease as the number of defects in the film increases.

Defect-related breakdown can be clearly distinguished from intrinsic breakdown in a statistic analysis of the results of tests on a large number of MOS capacitors. The defect density D can be derived from the point where all the capacitors with defect-related breakdown have been detected.

2.4 Device Fabrication

The substrates used in the study were <100> 1-2 Ω•cm n-type single crystal silicon. They were prepared using conventional cleaning procedure before oxide deposition[3]. The SiO_2 films were prepared by a radio frequency (rf) plasma deposition system previously described[4]. In a PECVD process the most important variables are deposition temperature, the total flow of reactive gases, chamber pressure, rf power and reactive gas ratio[4]. The stoichiometry of deposited SiO_2 films is determined by the reactive gas ratio R_o of N_2O to SiH_4: SiO_2 films deposited by APCVD using $R_o \leq 100$ contain excess silicon, whereas those with $R_o \geq 100$ have a Si:O ratio corresponding to that of SiO_2[5]. The

total flow of reactive gases, chamber pressure and rf power must be adjusted to provide suitable deposition rate and uniformity. The rate of deposition is an important factor in determining the electrical quality of the deposited materials. Thin SiO_2 films deposited at high rate usually have poor electrical properties[4]. The following parameters were used to deposit SiO_2 films tested in this study: the flow rates of N_2O and $He-2\%SiH_4$ mixture were 375 sccm and 75 sccm respectively, which gave the ratio R_o=250. The reactive gases were further diluted by ultra-high pure He of 1000 sccm to ensure uniformity and enable a wide range of deposition rates to be achieved simply by varying the reactive gas flow[4]. The chamber pressure and the power level were kept constant to be 1 Torr and 100 W (≈0.25 W/cm^2), respectively. The deposition rates were about 40 A/min for all the samples with deposition temperature ranging from 225°C to 350°C at 25°C intervals. MOS capacitors were fabricated by evaporating a circular aluminum electrode with an area of 0.005 cm^2 through a shadow mask onto the SiO_2 films in a vacuum system at a pressure of 10^{-5} Torr. The samples were given a postmetallization anneal (PMA) treatment in forming gas (10%H_2-90%N_2) at 400°C for 30 min. Finally, Ga-In paste was used to make the back contact. These samples have been used throughout this thesis.

2.5 Experimental Methods

2.5.1 Mobile ionic charge measurement

Mobile ionic charge Q_m is primarily due to the sodium ions in the oxide[6]. When an external bias is applied, these ions drift through the oxide, because of their small size, causing shifts in the flatband voltage of the device. Mobile ionic charge Q_m is measured by stressing a capacitor with a positive voltage on the gate at an elevated temperature for a period of time. At higher temperature a new charge equilibrium is rapidly reached. The amount of mobile charge can be calaulated from the shift between high-frequency C-V curves before and after stress:

$$Q_m = -C_{ox}\Delta V \tag{2.1}$$

where ΔV is the shift in the high-frequency C-V curve before and after stress.

2.5.2 Interface trap charge and oxide fixed charge measurements

The doping concentration of silicon substrate, either donors or acceptors, can be determined by the $C_{\max}$ and $C_{\min}$ from high-frequency C-V curve, by iteratively solving:

$$N = C \ln N - B \tag{2.2}$$

where

$$C = \frac{6.22\times10^5}{A^2}\frac{C_{\max}C_{\min}}{C_{\max}-C_{\min}}$$

$$B = 23.4C$$

and where A is the area of Al electrode in square centimeters and $C_{\max}$ and $C_{\min}$ are in pico-Farads[7]. Then the flatband voltage can be measured from the C-V curve, once the impurity concentration is known. At flatband[6]

$$C_{fb}=\frac{C_{ox}C_s}{C_{ox}+C_s} \tag{2.3}$$

where $C_s=\varepsilon_{si}/L_D$, $L_D=(\varepsilon_{si}KT/q^2N)^{1/2}$ and $\varepsilon_{si}=4.14\times10^{-13}$F/cm. Thus, the flatband voltage is the point on the high-frequency C-V curve at which C = C_{fb} [6].

From combined high-low frequency C-V curves interface trap level density D_{it} is obtained[6]:

$$D_{it}=\frac{C_{ox}}{q}(1-\frac{C_{LF}}{C_{ox}})^{-1}(1-\frac{C_{HF}}{C_{ox}})^{-1} \tag{2.4}$$

where C_{LF} and C_{HF} are quasi-static and high-frequency capacitance,respectively. The experimental setup for low-high frequency C-V measurements is shown in Figure 2.2. The instrument used for high-frequency C-V measurements is Boonton Capacitance Meter (Model 72 AD), which, operating at 1 MHz, measures the direct capacitance of the MOS capacitor from 1 to 2000 pF. A linear voltage ramp generator monitored by a digital multimeter (Keithley 174) is used to apply a time varying gate bias to the MOS capacitor and an x-y recorder to display the resulting C-V characteristics. To measure low-frequency C-V curve the connection to the device is switched to an electrometer (Keithley 610C), which measures the resulting displacement current flowing through the MOS capacitor. This displacement current is directly proportional to the differential capacitance. The relationship between the displacement current I_d and the

differential capacitance C can be easily derived if we choose a linear voltage ramp V = αt, where α is a constant and t is time: I_d = C(dV/dt) or C = I_d/α.

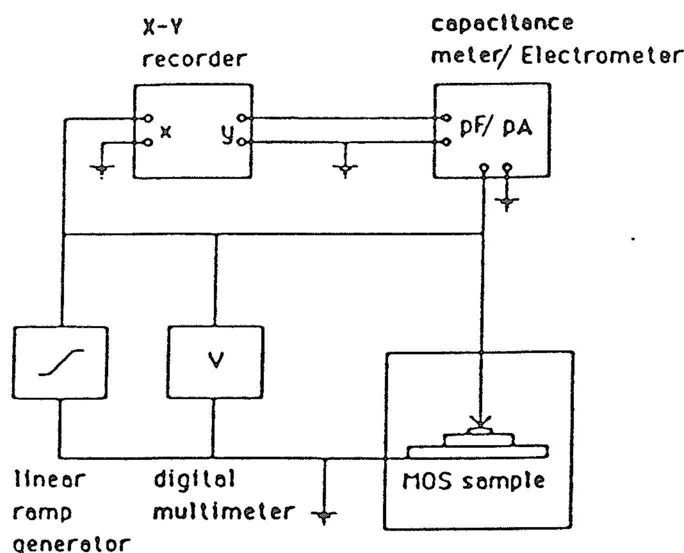

Figure 2.2 The experimental setup for high-low frequency C-V measurements.

Obviously (2.4) yields D_{it} only as a function of gate bias. D_{it} as a function of position in the bandgap can be obtained by using the following equations:

$$\psi_s(V_g)-\psi_s(V_{fb})=\int_{V_{fb}}^{V_g}(1-\frac{C_{LF}}{C_{ox}})dV \qquad (2.5)$$

and

$$\frac{E_c-E}{q}=\frac{E_g}{2q}+\psi_s-\phi_B \qquad (2.6)$$

where V_g is gate voltage, ψ_s silicon surface potential, ϕ_B electrostatic potential in the bulk of the silicon and the flatband voltage, V_{fb}, is defined by $\psi_s(V_{fb})$ = 0[6].

If oxide fixed charge Q_f is assumed to be located at or very near the $Si-SiO_2$ interface as a charge sheet like the case of thermally grown oxide and the metal-semiconductor work function difference is neglected, then it is given by

$$Q_f = -C_{ox} V_{fb} \tag{2.7}$$

where $\varepsilon_{ox}/d = C_{ox}$ is the oxide layer capacitance per unit area, d is the oxide thickness and ε_{ox} is the permittivity of silicon dioxide ($\varepsilon_{ox} = 3.45 \times 10^{-13}$ F/cm)[6].

2.5.3 Dielectric breakdown measurement

In dielectric breakdown measurements, breakdown field-strength for individual capacitors is not really meaningful and usually many capacitors are measured to obtain a statistical distribution.

From the analysis of the results of statistic tests the defect density can be obtained. If the defects are randomly distributed over the surface, a Poisson distribution may be assumed. The probability F_K that one or more defects will be present in an area A is then given by[8]:

$$F_K = \sum_{m=1}^{\infty} \frac{(AD)^m \exp(-AD)}{m!}$$

The probability of finding capacitors without any defects is then:

$$1 - F_K = \frac{(AD)^o \exp(-AD)}{0!} = \exp(-AD) \tag{2.8}$$

where A is the area of Al electrode and D defect density.

2.6 Results and Discussion

2.6.1 Mobile ionic charge

Mobile ionic charges were measured on all the samples deposited at 225°C, 250°C, 275°C, 300°C, 325°C and 350°C using bias-temperature (BT) method. The BT measurements were carried out at 150°C with a biasing voltage of +8V on the gate for 5 min (mobile ions drift from $Al-SiO_2$ interface to $Si-SiO_2$ interface). The high-frequency C-V curves before and after BT aging are shown in Figure 2.3. Using the shifts between the curves, mobile ionic charge densities were calculated and listed in Table 2.2. The mobile ionic charge densities in all the samples deposited at six different temperatures were larger than that in thermal oxide (~$10^{10}cm^{-2}$) shown in Table 2.1. However the PECVD SiO_2 films were deposited under nonclean laboratory conditions. It is expected that with cleaner deposition conditions the mobile ion densities will drop to the level found in thermal oxides.

Table 2.2. Mobile ionic charges of the samples deposited at different temperatures.

T_d(^{o}C)	C_{ox}(pF)	ΔV(V)	Q_m($10^{10}cm^{-2}$)
225	335	0.20	8.4
250	314	0.20	7.9
275	252	0.30	9.5
300	280	0.25	8.8
325	305	0.15	5.7
350	276	0.10	3.5

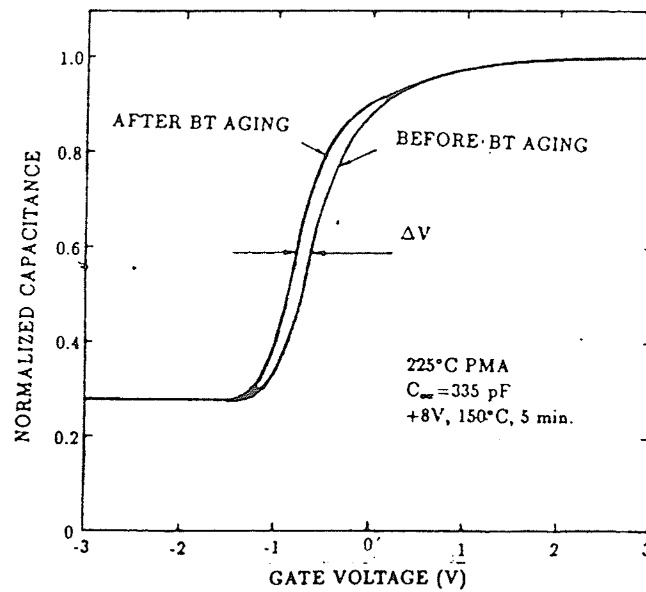

Figure 2.3.(a) The high-frequency C-V curves of the sample deposited at 225°C before and after BT aging.

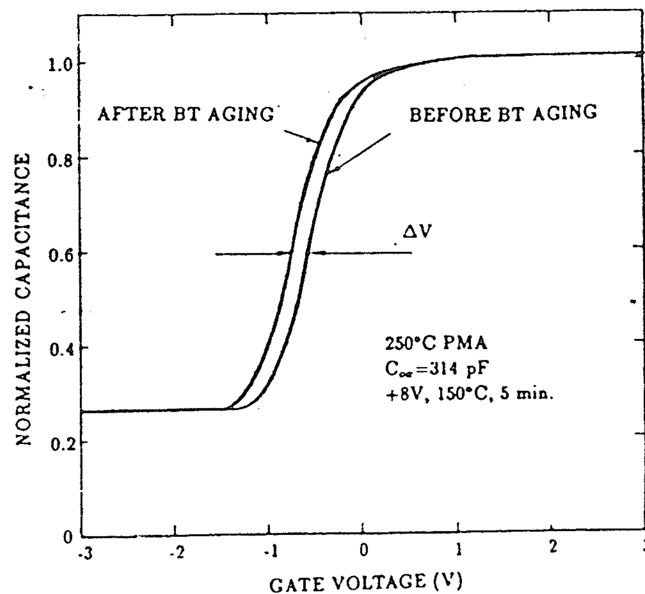

Figure 2.3.(b) The high-frequency C-V curves of the sample deposited at 250°C before and after BT aging.

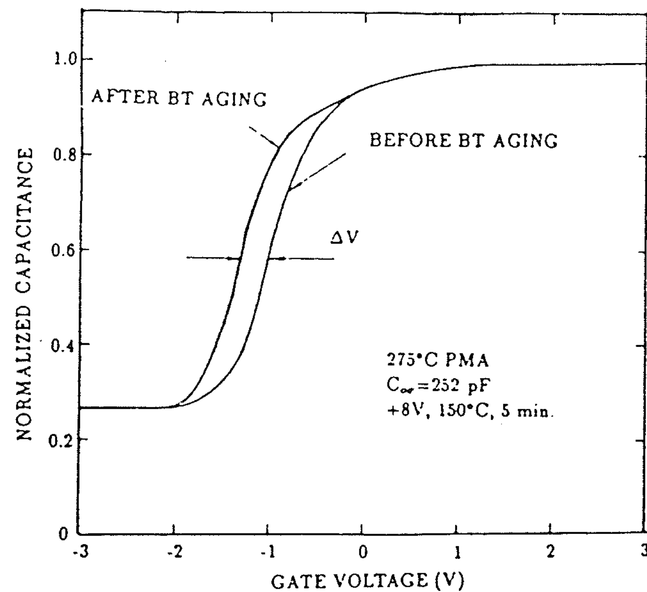

Figure 2.3.(c) The high-frequency C-V curves of the sample deposited at 275° C before and after BT aging.

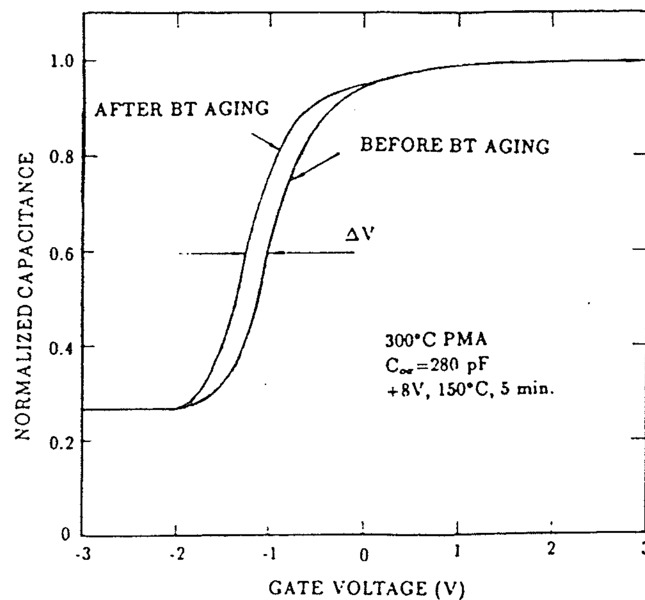

Figure 2.3.(d) The high-frequency C-V curves of the sample deposited at 300° C before and after BT aging.

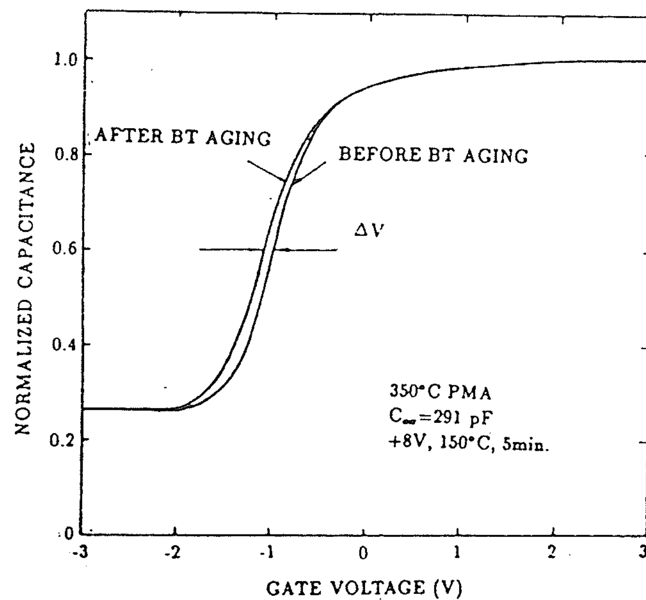

Figure 2.3.(e) The high-frequency C-V curves of the sample deposited at 325° C before and after BT aging.

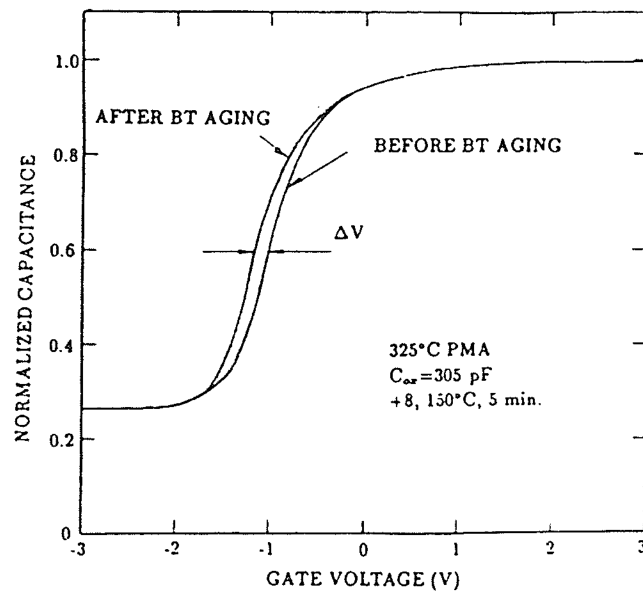

Figure 2.3.(f) The high-frequency C-V curves of the sample deposited at 350° C before and after BT aging.

2.6.2 Interface trap charge and oxide fixed charge

Figure 2.4 shows high-frequency and quasi-static C-V curves of the samples deposited at various temperatures before PMA. The PECVD technique, although low temperature, is still a high-energy process and interfacial damage is to be expected. It was found that the samples deposited at lower temperatures had larger flatband voltage shifts and higher interface trap densities, suggesting that the reaction between the reactive gases and silicon surface might be more complete at higher deposition temperatures. Using Eqs. (2.2) to (2.7) the results of interface trap density and oxide fixed charge density were calculated and listed in Table 2.3. The effect of deposition temperature on flatband voltage shift, which is proportional to oxide fixed charge, is shown in Figure 2.5.

However, after PMA the samples deposited at different temperatures did not show much difference in their interfacial quality, which was close to those of thermally grown oxides. The high-frequency and quasi-static C-V curves of the samples after PMA were shown in Figure 2.6. The interface trap density at midgap and oxide fixed charge density were calculated and listed in Table 2.4.

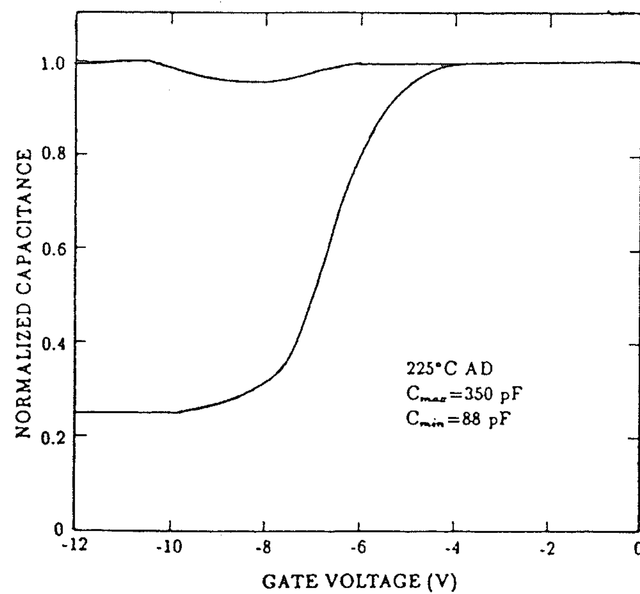

Figure 2.4.(a) The high-frequency and quasi-static C-V curves of the sample deposited at 225°C before PMA.

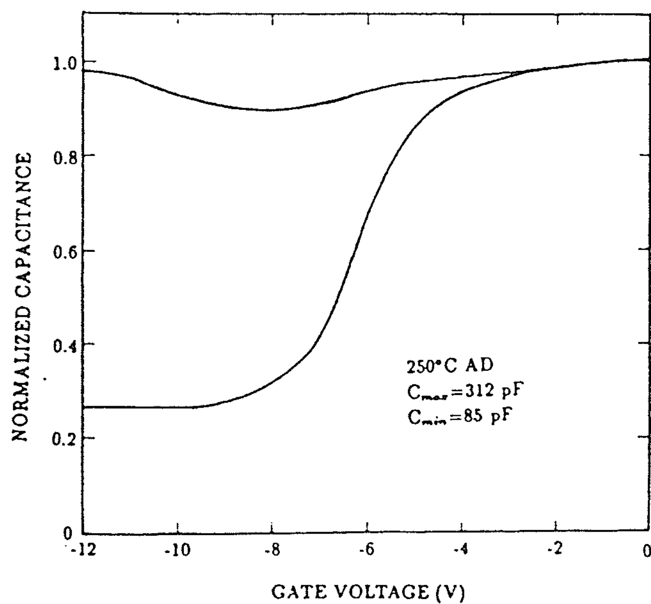

Figure 2.4.(b) The high-frequency and quasi-static C-V curves of the sample deposited at 250°C before PMA.

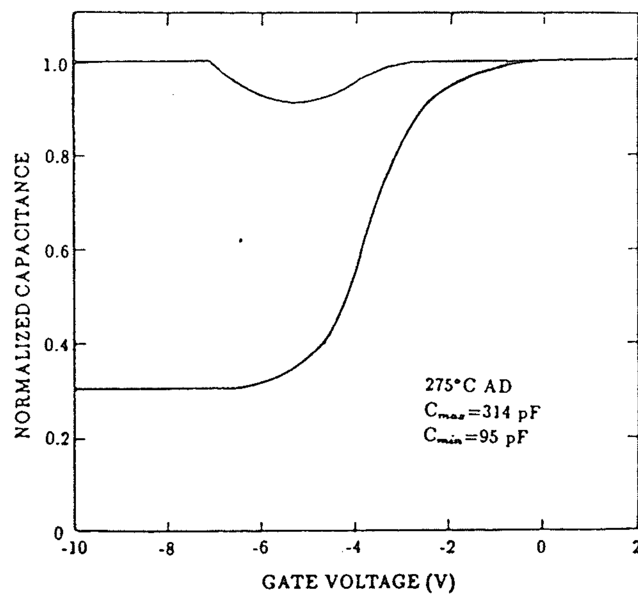

Figure 2.4.(c) The high-frequency and quasi-static C-V curves of the sample deposited at 275°C before PMA.

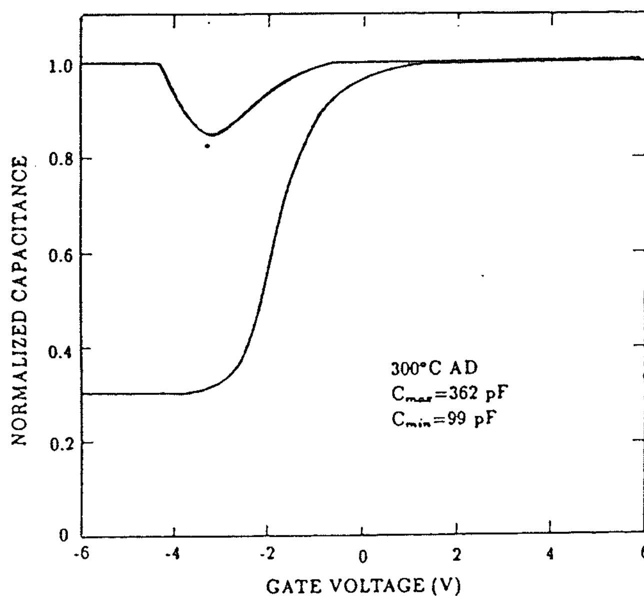

Figure 2.4.(d) The high-frequency and quasi-static C-V curves of the sample deposited at 300°C before PMA.

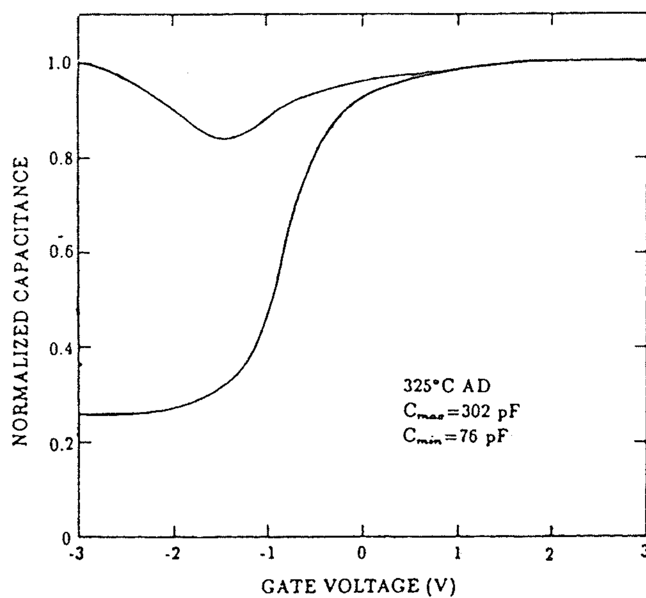

Figure 2.4.(e) The high-frequency and quasi-static C-V curves of the sample deposited at $325^{o}C$ before PMA.

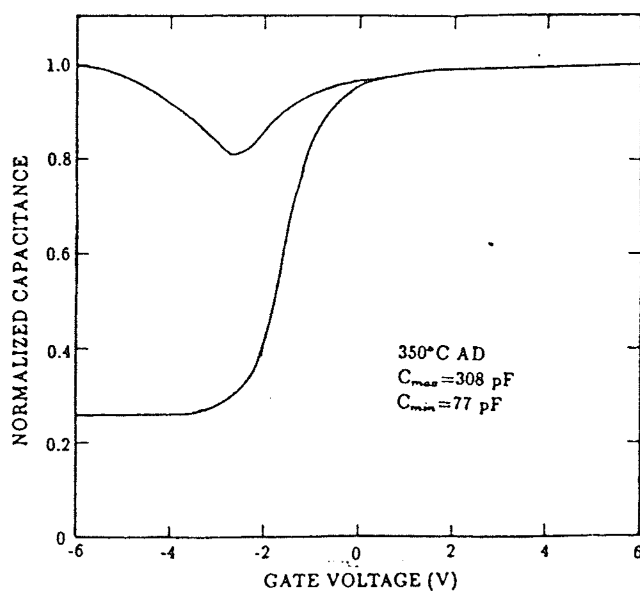

Figure 2.4.(f) The high-frequency and quasi-static C-V curves of the sample deposited at $350^{o}C$ before PMA.

Table 2.3. Interface trap density at midgap and oxide fixed charge density before PMA.

T_d (^oC)	V_{fb}(V)	Q_f ($10^{12}cm^{-2}$)	D_{it} ($10^{12}cm^{-2}eV^{-1}$)
225	-6.3	2.76	4.57
250	-5.2	2.03	3.64
275	-3.4	1.33	1.73
300	-1.6	0.72	1.93
325	-1.4	0.53	1.00
350	-1.4	0.54	1.10

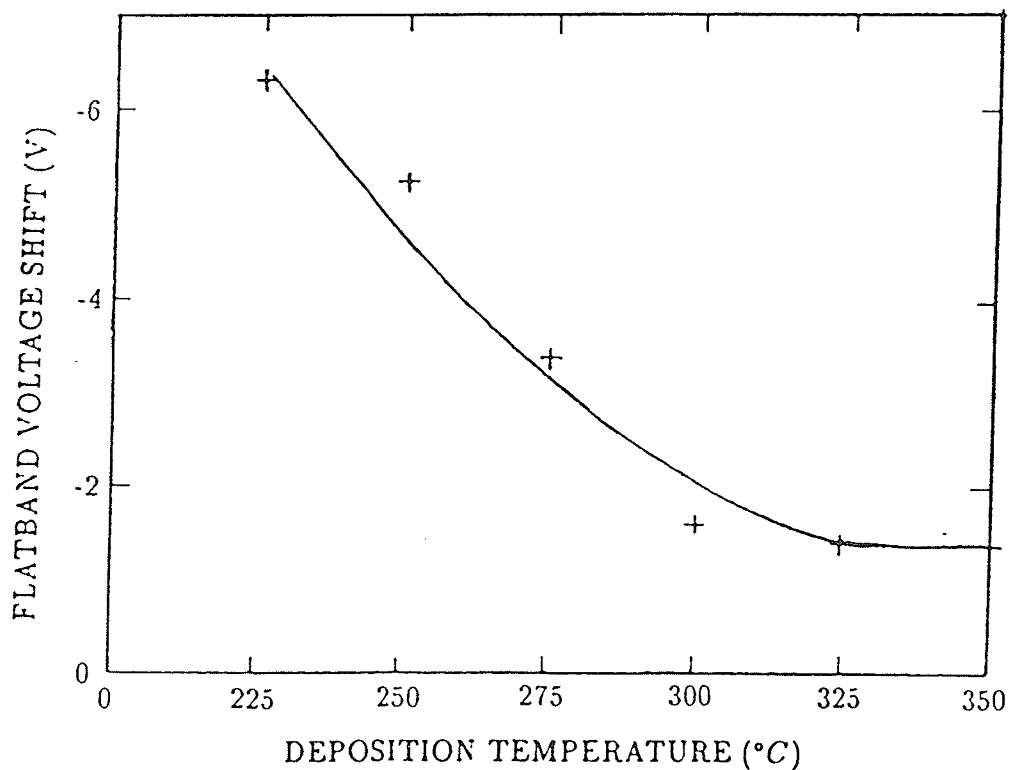

Figure 2.5. The flatband voltage shift as a function of deposition temperature.

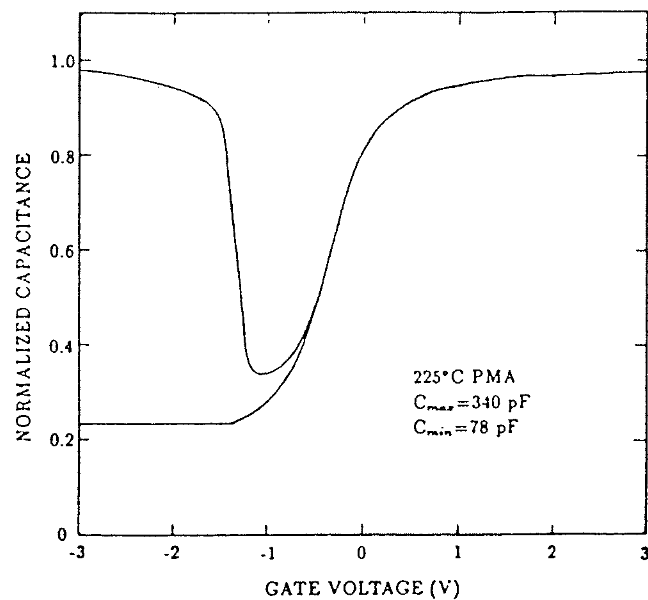

Figure 2.6.(a) The high-frequency and quasi-static C-V curves of the sample deposited at 225°C after PMA.

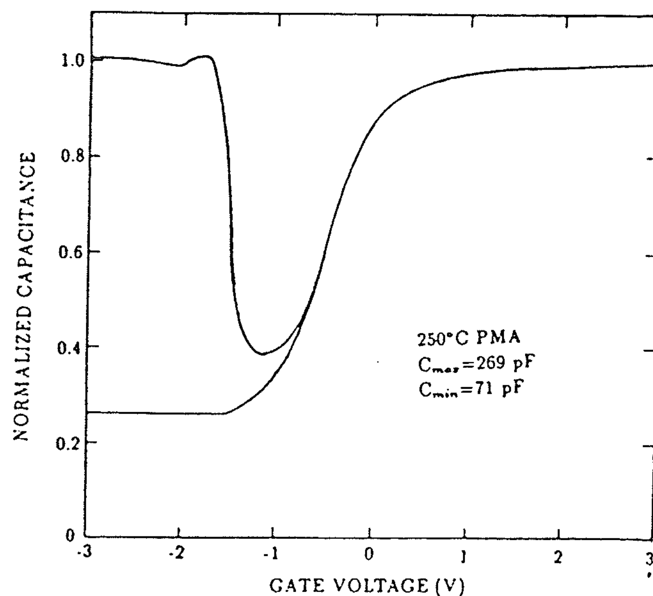

Figure 2.6.(b) The high-frequency and quasi-static C-V curves of the sample deposited at 250°C after PMA.

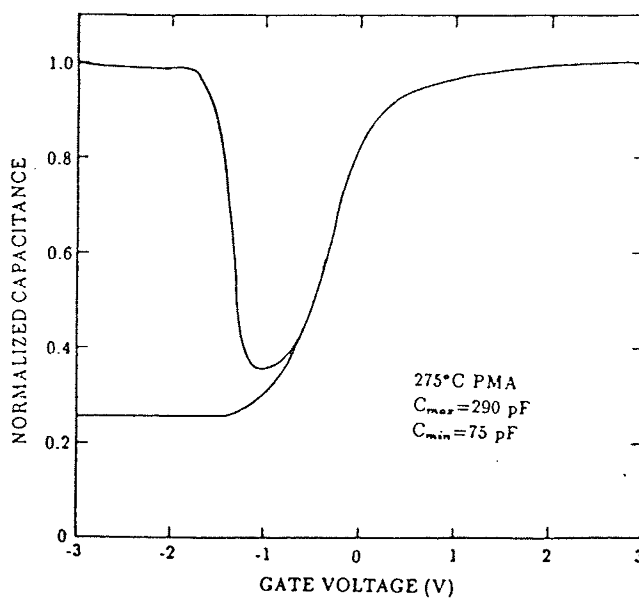

Figure 2.6.(c) The high-frequency and quasi-static C-V curves of the sample deposited at 275°C after PMA.

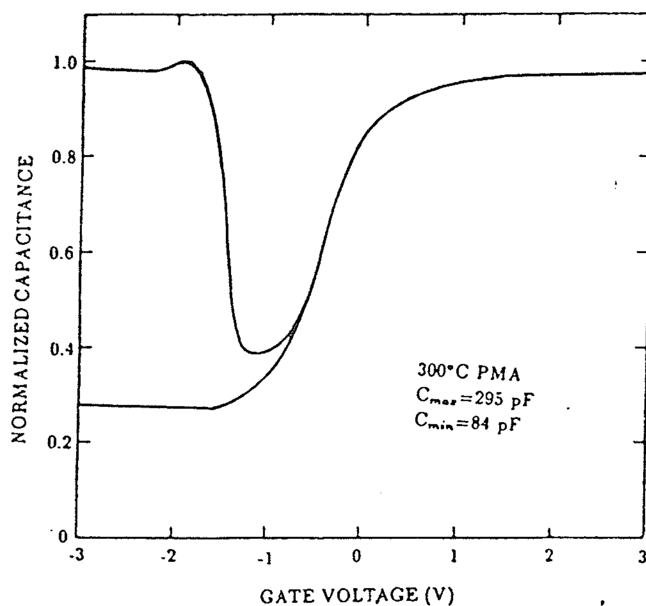

Figure 2.6.(d) The high-frequency and quasi-static C-V curves of the sample deposited at 300°C after PMA.

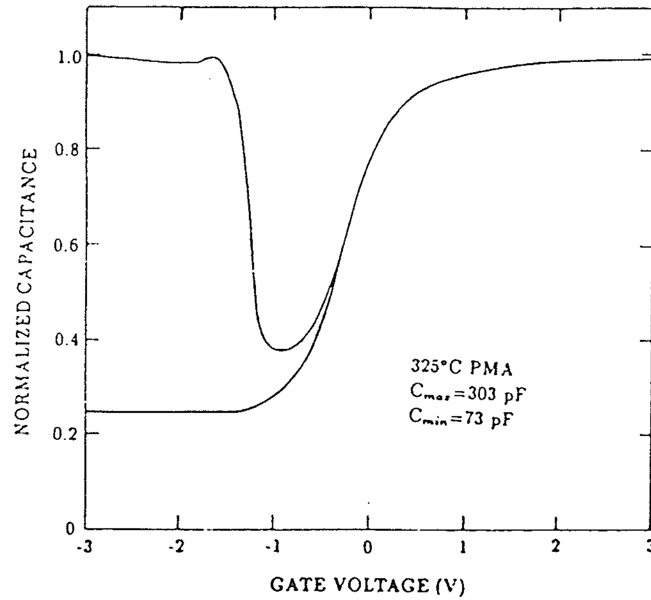

Figure 2.6.(e) The high-frequency and quasi-static C-V curves of the sample deposited at 325°C after PMA.

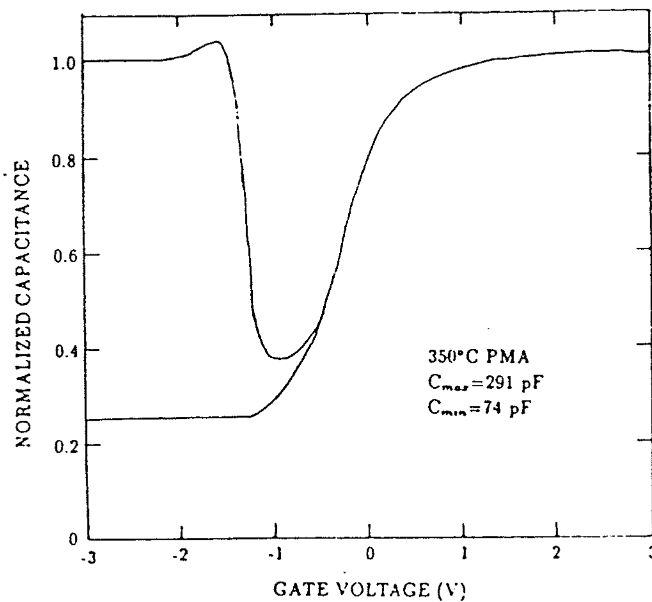

Figure 2.6.(f) The high-frequency and quasi-static C-V curves of the sample deposited at 350°C after PMA.

Table 2.4. Interface trap density at midgap and oxide fixed charge after PMA.

T_d(^oC)	V_{fb}(V)	Q_f ($10^{10}cm^{-2}$)	D_{it}($10^{10}cm^{-2}eV^{-1}$)
225	-0.250	10.6	6.62
250	-0.350	2.94	6.01
275	-0.250	9.06	5.92
300	-0.225	8.30	7.07
325	-0.175	6.63	4.03
350	-0.200	7.28	3.47

2.6.3 Dielectric breakdown

Figure 2.7 shows typical ramp I-V curves for two samples deposited at 275^oC and 350^oC after PMA. At lower field the current is dominated by the displacement current I=CdV/dt. When the fields reach a few MV/cm Fowler-Nordheim (F-N) injection begins. Then the curves go through a trapping ledge onto a new F-N characteristic before breakdown defined in this case as the field when $I=10^{-6}$A.

Figure 2.8 shows the breakdown field distributions of the samples deposited at 275^oC and 350^oC, where 41 and 37 capacitors, each with an area of 0.005 cm^2 were ramped to destructive breakdown. The positive gate voltage was applied on the devices for this test. About 90% of the capacitors tested had a breakdown field higher than 5 MV/cm in both cases. The capacitors having breakdown fields lower than 5 MV/cm were those on the edge of the samples, where they were most likely damaged by the handling during the fabrication. The average field at breakdown was 7 MV/cm and 6 MV/cm for the samples deposited at 275^oC and 350^oC respectively.

The defect densities were calculated using Eq.(2.8) under the assumption that the breakdown which occured at a field lower than 5 MV/cm was due to the oxide defects. The results were shown in Table 2.5.

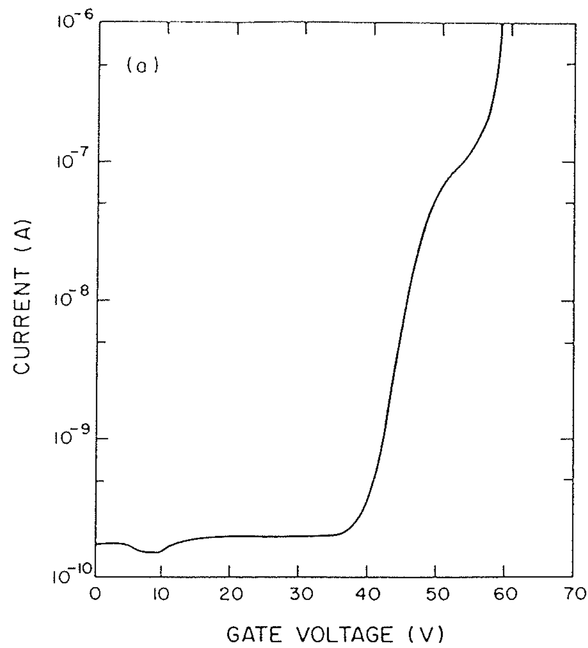

Figure 2.7.(a) The typical ramp I-V curve of the sample deposited at 275°C after PMA.

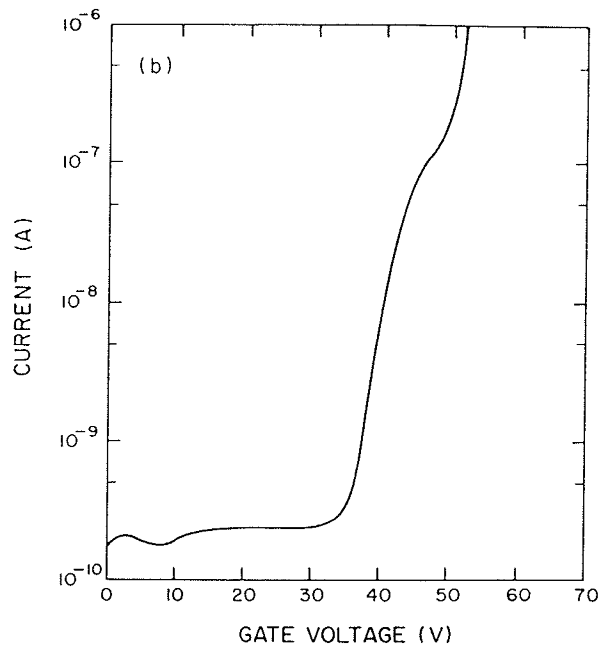

Figure 2.7.(b) The typical ramp I-V curve of the sample deposited at 350°C after PMA.

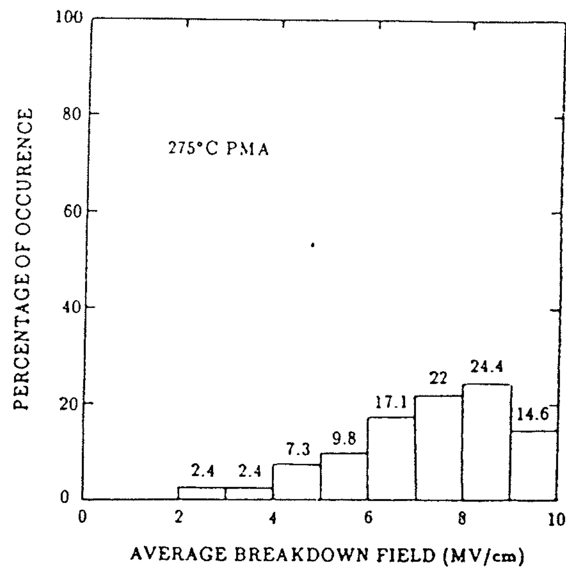

Figure 2.8.(a) The breakdown field distribution of the sample deposited at 275° C after PMA.

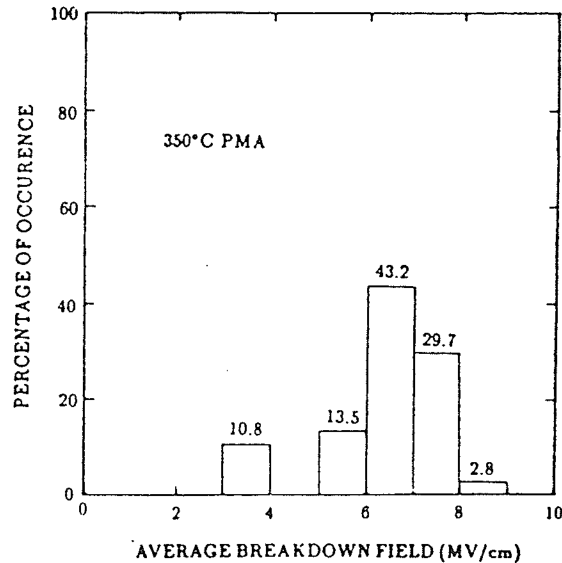

Figure 2.8.(b) The breakdown field distribution of the sample deposited at 350° C after PMA.

Table 2.5. Defect densities of the samples deposited at 275° C and 350° C after PMA.

$T_d(^o C)$	$F_K(\%)$	D(cm^{-2})
275	12	26
350	11	23

2.7 Conclusions

As a low-temperature technique, plasma-enhanced chemical vapor deposition can prepare thin SiO_2 films which have near thermal oxide quality. The bias-temperature (BT) aging measurements (+8V,150°C for 5 min) revealed that the MOS capacitors were stable with mobile inoic charge on the order of $10^{10}cm^{-2}$ in all the samples deposited in the temperature range of 225–350°C, although PECVD SiO_2 films were deposited under nonclean laboratory conditions. High-frequency and quasi-static C-V measurements showed that the as-deposited interface densities were on the order of $10^{12}cm^{-2}eV^{-1}$, which is not much higher than that measured in as-grown 800°C thermal oxide stucture[9], for all the samples deposited at different temperatures and decreased with increasing deposition temperature, although PECVD technique is a high-energy process and radiation damage is expected. A postmetallization anneal reduced interface trap density in all the samples to the values on the order of $10^{10}cm^{-2}eV^{-1}$, which are still higher than those obtained in the thermal oxide structures, but they are good enough for device applications.

The average breakdown fields of PECVD SiO_2 films after postmetallization anneal were around 6-7 MV/cm, which are also high enough for device applications. The percentage of high quality capacitors on the same piece of wafer was high if those damaged on the edge by the handling are excluded.

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CHAPTER 3

ELECTRON TRAPPING IN PECVD SiO_2

3.1 Introduction

Bulk oxide traps are located in the bulk of the SiO_2. They are important to the device stability. Hot carriers generated during device operation can enter the oxide and become trapped, altering device characteristics. Also, either in manufacture or in operation, electron-hole pairs can be created in the SiO_2 by ionizing radiation, with subsequent trapping and deterioration of device characteristics.

These traps are especially crucial to very large scale integration (VLSI), where the channel lengths of MOSFETs are very small and the electric fields in gate oxides are very high. VLSI circuits usually use n-channel MOSFETs, in which hot electrons can be emitted from the silicon into the gate oxide when applied voltages are sufficiently large. Hot electrons can originate from either the surface channel [1] or the silicon substrate [2]. Subsequent trapping of the electrons injected into the oxide can cause instability in the form of transconductance degradation and threshold voltage drift with time[1-6]. These effects also can result from hot hole injection, but hot hole injection occurs only when the drain is in strong avalanche breakdown, which rarely occurs in practice[7].

In this chapter charge trapping in SiO_2 and different methods of studying charge trapping are reviewed. The experimental results of electron trapping in PECVD SiO_2 using Fowler-Nordheim injection are presented and discussed.

3.2 Traps in SiO_2

Bulk oxide traps are associated with defects in the SiO_2 such as impurities and broken bonds. These traps are either connected to the oxide formation or related to processing following oxide formation, often from some form of radiation. Because of continuing scaling-down of device dimensions, the classical high temperature techniques for doping, lithography and etching have to be substituted with low-temperature and more anisotropic physical techniques. These include ion implantation, electron-, x-ray or ion-beam lithography, reactive ion etching , plasma-assisted oxidation or deposition. These techniques either use or generate high-energy electrons, ions or photons which are likely to create electron-hole (e-h) pairs and defect centers in any exposed SiO_2 layer.

3.2.1 Electron traps[7]

There are two different types of electron trapping centers in as-grown SiO_2: (1) Water-related traps. These traps are so called because their density is proportional to the amount of water incorporated in the oxide, but the exact chemical nature of the center is unknown; (2) Sodium-related centers. This electron trap about 2 eV below the conduction band of the SiO_2 appears to be related to sodium in the oxide, because it disappears when sodium levels are reduced. Electron traps can be also produced by tungsten, phosphorus, arsenic, and aluminum that have been delibrately introduced by either diffusion or ion implantation.

3.2.2 Hole traps

There are deep hole traps in as-grown oxide which are located near the interface[7], particularly the $Si-SiO_2$ interface and permanently capture holes at room temperature. They are believed to be caused by impurities introduced into the SiO_2 near the interface such as excess Si near the $Si-SiO_2$ interface and/or caused by strained or broken bonds possibly due to stress or stress relief resulting from viscous shear flow. Energetically, shallow hole traps in SiO_2 are observed to be occupied at low temperatures. Spatially, these traps are thought to be uniformly distributed in the bulk of the SiO_2 film. Captured holes are discharged from these traps at room temperature. Deep stable hole trapping sites at room temperature can be produced by implanting As or P into the bulk of the SiO_2 film.

3.3 Experimental Methods

To study the properties of bulk traps in SiO_2, free carriers must be introduced into the SiO_2 which can then be trapped at impurity sites. Free carrier injection is difficult because there are large energy barriers between the Si and the SiO_2 and between metal electrodes and the SiO_2.

There are various ways of injecting carriers over the electrode energy barriers. These methods are: (1) avalanche injection form the silicon, (2) internal photoemission from either the silicon or the gate electrode, (3) Fowler-Nordheim tunneling from either the silicon or the gate electrode.

3.3.1 Avalanche injection[7]

In avalanche injection, carriers are accelerated by an applied electric field. When the field at the silicon surface reaches the avalanche breakdown field ($\geq 3 \times 10^5$ V/cm, depending on doping density), carriers generated in the surface depletion layer are accelerated to sufficient energy for impact ionization to occur. A plasma of energetic electron-hole pairs is created in the silicon surface depletion layer. Some of the electrons or holes have enough energy to surmount the interfacial energy barrier and enter the SiO_2. Generally, electrons are injected when the substrate is p-type and holes when the substrate is n-type.

A periodic waveform is required to produce avalanche injection in an MOS capacitor. Sinusoidal, square, and sawtooth waveforms can be used. The first step toward injection is to produce an avalanche plasma at the silicon surface of the MOS capacitor. To produce sufficient band bending to make avalanche breakdown occur, the silicon must be driven into deep depletion. Deep depletion is produced by applying a large amplitude periodic ac signal of a frequency too high to for minority carriers to follow. As the ac voltage is increased, band bending at the silicon surface increases until the field at the silicon surface becomes high enough for avalanche breakdown. An avalanche plasma then forms once per cycle. A small fraction of the electrons or holes in this plasma have sufficient energy to surmount the interfacial energy barrier. Once in the oxide, these electrons or holes drift to the gate, driven by the electric field across the oxide. They then flow through the external circuit where they are detected.

Avalanche injection is widely used to introduce free carriers into SiO_2 film and study the charging kinetics because it

provides large current density, requires a simple apparatus and injects only one type of carrier. But avalanche injection has to be combined with the photo I-V method in order to determine the trap distribution in the oxide.

3.3.2 Internal photoemission[8]

Internal photoemission from the metal and the silicon is used in the photo I-V measurement. An electron excited by the absorption of ultraviolet light in either the metal gate or the silicon of an MOS capacitor will be injected into the SiO_2, provided that it can reach and surmount the interfacial energy barrier.

The injection of electrons from either the metal gate or the silicon are affected by: (1) barrier height. Photostimulated electrons must have sufficient energy to surmount the barrier to enter the oxide. (2) barrier position. The further the barrier maximum is from the interface, the greater the probability of carrier scattering before injection. Both the barrier height and the barrier position are affected by the oxide charge and gate bias. Therefore, oxide charge information can be obtained by measuring photo I-V characteristics before and after charging.

The energy-band diagram between the emitter surface and SiO_2 is shown in Figure 3.1. As can be seen, the gate voltage bias and oxide trapped charge will cause the height and position of the barrier to be lower and nearer to the emitter. This makes it easier for the electrons in the emitter surface to reach the energy barrier and surmount it. The trapped charge not very far from the emitter surface can be also detected when applied gate voltage is sufficiently large.

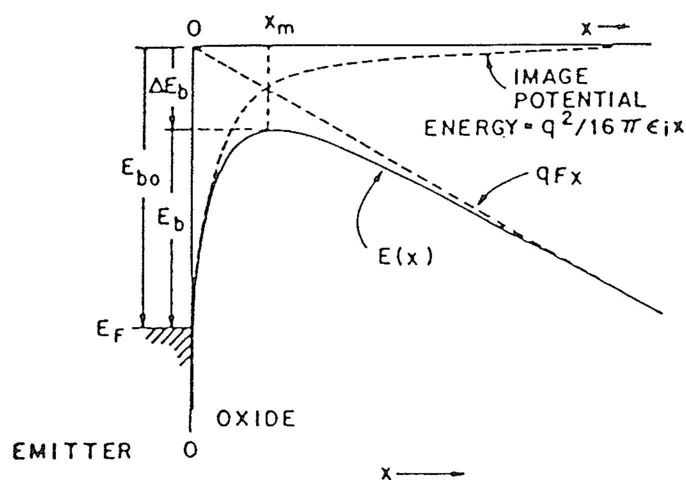


Figure 3.1 Energy-band diagram between the emitter surface and SiO_2. The barrier height at x=0 is E_{bo}. Barrier height is lowered by presence of oxide charge and an applied field, making the effective barrier height E_b. The barrier height lowering ΔE_b is due to the combined effects of the electric field, consisting of the contribution from oxide charge at x>x_m, an applied bias and image force[7].

The potential barrier at a location x_m near the emitter interface can be surmounted by an increasing number of electrons as it is lowered by an increasing applied voltage. The field at the potential maximum at time, t, without the image force contribution, determined from Poisson's equation, is given by

$$E(x_m^+,t)=\frac{V_g^+-\phi_{ms}-\psi_s^+}{d}+\frac{1}{\varepsilon_{ox}}\frac{x_o}{d}Q-\frac{1}{\varepsilon_{ox}}\int_{x_m^+}^{d}n_o(x,t)dx \qquad (3.1)$$

for positive gate voltage, and by

$$E(X_m^-,t)=\frac{V_g^--\phi_{ms}-\psi_s^-}{d}-\frac{1}{\varepsilon_{ox}}(1-\frac{x_o}{d})Q+\frac{1}{\varepsilon_{ox}}\int_0^{x_m^-}n_o(x,t)dx \qquad (3.2)$$

for negative voltage; where Al-SiO_2 interface is the origin of the x coordinates taken positive towards the $Si-SiO_2$ interface, V_g is the applied gate voltage, ϕ_{ms} is the work function difference between the aluminum gate and the silicon, ψ_s is the silicon surface potential, ε_{ox} is the oxide low-frequency permittivity, x_o is the centroid of the trapped charge distribution, Q is the integral of the oxide charge n_o(x, t) over the thickness d, and the superscripts (+ and -) refer to the voltage polarity of the metal gate electrode.

In order to have the same photocurrent before and after charging, the electric field at x_m has to be constant, which requires a change in applied gate voltage $\Delta V_g=V_g^{charged}$ - $V_g^{uncharged}$ given by

$$\Delta V_g^+=-\frac{1}{\varepsilon_{ox}}x_oQ \qquad (3.3)$$

for Si injection, and

$$\Delta V_g^- = \frac{1}{\varepsilon_{ox}}(d - x_o)Q \tag{3.4}$$

for Al injection, provided that the surface potential ψ_s can be considered constant for each polarity over the gate voltage range of interest.

Equations (3.3) and (3.4) are two simultaneous equations in two unknowns that can be solved to obtain

$$Q_{ot} = \frac{\varepsilon_{ox}}{d}(\Delta V_g^- - \Delta V_g^+) \tag{3.5}$$

and

$$x_o = d\left(1 - \frac{\Delta V_g^-}{\Delta V_g^+}\right)^{-1} \tag{3.6}$$

3.3.3 Fowler-Nordheim tunneling injection[9]

In this technique an appropriate polarity gate voltage (positive for n-type silicon substrate and negative for p-type silicon substrate) with constant ramp rate is applied to the gate of MOS capacitors. When the gate voltage reaches a certain value, Fowler-Nordheim tunneling injection begins to dominate and a charge trapping ledge can appear in ramp I-V curve, indicating the injected electrons are filling the traps while drifting across the oxide. The change in energy bands with a positive voltage bias is shown in Figure 3.2.

The trapping parameters can be deduced from the width of the ledge and the current at which it occurs. This technique coupled with the high-frequency C-V technique can determine the centroid of electron trap distribution.

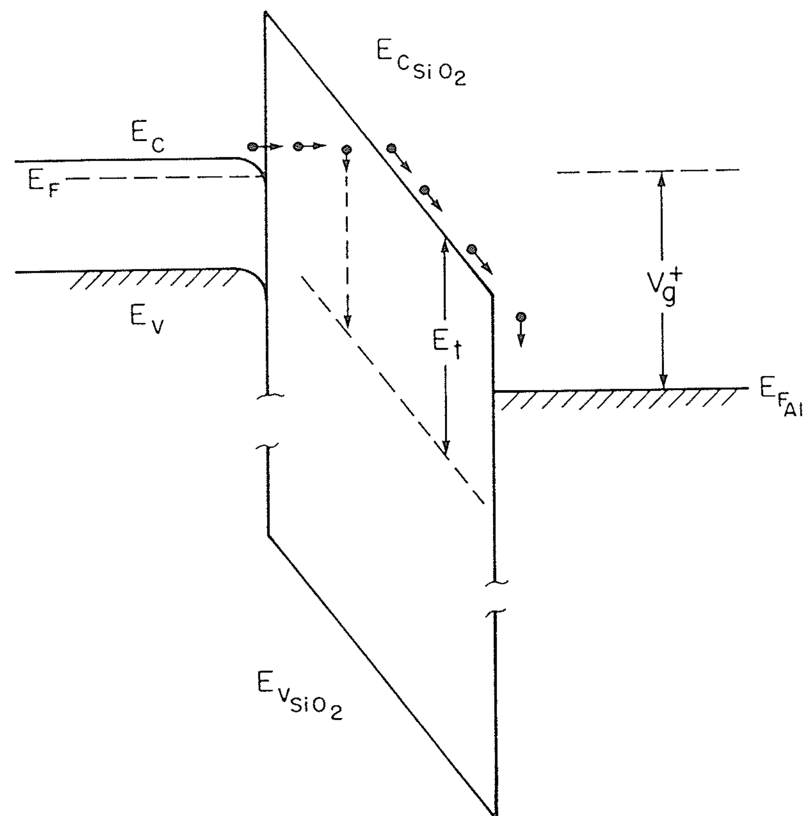


Figure 3.2 Energy band diagrams of MOS structure under positive voltage bias V_g^+ illustrating schematically Fowler-Nordheim tunneling of electrons through the SiO_2 and electron capture by a trapping state located energetically in the SiO_2 bandgap[8].

Fowler-Nordheim tunneling injection has a disadvantage of detrapping due to high fields. The trapping ledge is actually the result of dynamic equilibrium between trapping and high-field detrapping.

The electric field near the injecting interface, at any time t, can be written as[10]

$$E(t)=[(V_g-\phi_{ms}-\psi_s)-Q_{ot}\frac{d-x_o}{\varepsilon_{ox}}]/d \tag{3.7}$$

where V_g is the gate voltage, ϕ_{ms} is metal-silicon work function difference, ψ_s is silicon surface potential, Q_{ot} is the trapped charge per unit area, d (d = A ε_{ox}/C_{ox}) is the thickness of the oxide, x_o is the centroid of trapped charge distribution in the oxide, ε_{ox} is the permittivity of silicon dioxide (ε_{ox} = 3.45 × 10^{-13} F/cm).

The ramp I-V curve starts with a constant displacement current before the injection of electrons into the oxide begins. As the Fowler-Nordheim injection current per unit area J (J=I/A where A is the area of the Al electrode) becomes large enough, a particular trapping center begins to fill and[10]

$$dQ_{ot}(t)/dt=J_i\sigma_n N_o \tag{3.8}$$

here J_i is the current level per unit area (J_i = I_i/A) near the start of the ledge, σ_n is the capture cross section and N_o is the total number of traps per unit area. Assuming dE/dt≈0 when the traps start to fill and during filling

$$dV_g/dt=\frac{d-x_o}{\varepsilon_{ox}}\frac{dQ_{ot}(t)}{dt} , \tag{3.9}$$

Two assumptions have been made to get Eq.(3.9). The first assumption is that the silicon surface potential ψ_s does not

change with time. This is true if we use positive voltage bias for n-type silicon substrate and negative voltage bias for p-type silicon substrate, because the silicon surface is then strongly accumulated during the measurements. The second one is generally satisfied if the initial trapping probability $(N_o \sigma_n) \leq 0.3$[11]. Substituting Eq.(3.8) into Eq.(3.9) yields

$$N_o \sigma_n = \frac{\varepsilon}{(d - x_o) J_i} \frac{dV_g}{dt} \tag{3.10}$$

Integration of Eq.(3.9) over the extent of the current ledge (from traps unfilled to traps filled) yields

$$N_o = \frac{\varepsilon_{ox} \Delta V_{gL}}{q (d - x_o)} \tag{3.11}$$

where q is the charge on an electron ($q = 1.6 \times 10^{-19}$ C) and ΔV_{gL} is the voltage width of the ledge. The oxide trapped charge density Q_{ot} is related to N_o by

$$Q_{ot} = qN_o = \frac{\varepsilon_{ox} \Delta V_{gL}}{d - x_o} \tag{3.12}$$

Substituting Eq.(3.11) into Eq.(3.10) yields

$$\sigma_n = \frac{q}{\Delta V_{gL} J_i} \frac{dV_g}{dt} \tag{3.13}$$

Figure 3.3 shows how I_i and ΔV_{gL} are determined from a ramp I-V curve. The Fowler-Nordheim characteristics before and after electron trapping are extrapolated by dashed lines. The injection current I_i is defined as the intercept of initial Fowler-Nordheim curve and the slope of electron trapping ledge. The voltage width of electron trapping ledge ΔV_{gL} is the voltage shift between two Fowler-Nordheim curves.

The sequential ramp I-V and C-V measurements can be made to determine the centroid of trapped charge distribution and the total number of electrons per unit area in the oxide can be also found. Before and after each ramp I-V cycle, a high-frequency C-V trace is recorded, starting with the virgin sample. The ramp I-V is cycled several times to consecutively higher voltages through the SiO_2 charge trapping ledge until no voltage shift is observed or the destructive breakdown occurs. Then from the flatband voltage shift ΔV_{fb} in the C-V curves and gate voltage shift ΔV_g in the I-V curves, the centroid of trapped charge distribution can be calculated.

The C-V flatband voltage shift ΔV_{fb} and I-V gate voltage shift ΔV_g can be, respectively, written as[7]

$$\Delta V_{fb}=\frac{Q_{ot}x_o}{\varepsilon_{ox}} \tag{3.14}$$

and[9]

$$\Delta V_g=\frac{Q_{ot}(d-x_o)}{\varepsilon_{ox}} \tag{3.15}$$

From Eqs.(3.14) and (3.15) the centroid, as measured from the $Al-SiO_2$ interface, and the total number of trapped electrons per unit area, are given by

$$\frac{x_o}{d}=(1+\frac{\Delta V_g}{\Delta V_{fb}})^{-1} \tag{3.16}$$

where d can be determined from the maximum capacitance in the C-V curve and

$$N_o=\frac{\varepsilon_{ox}}{qd}(\Delta V_g+\Delta V_{fb}) \tag{3.17}$$

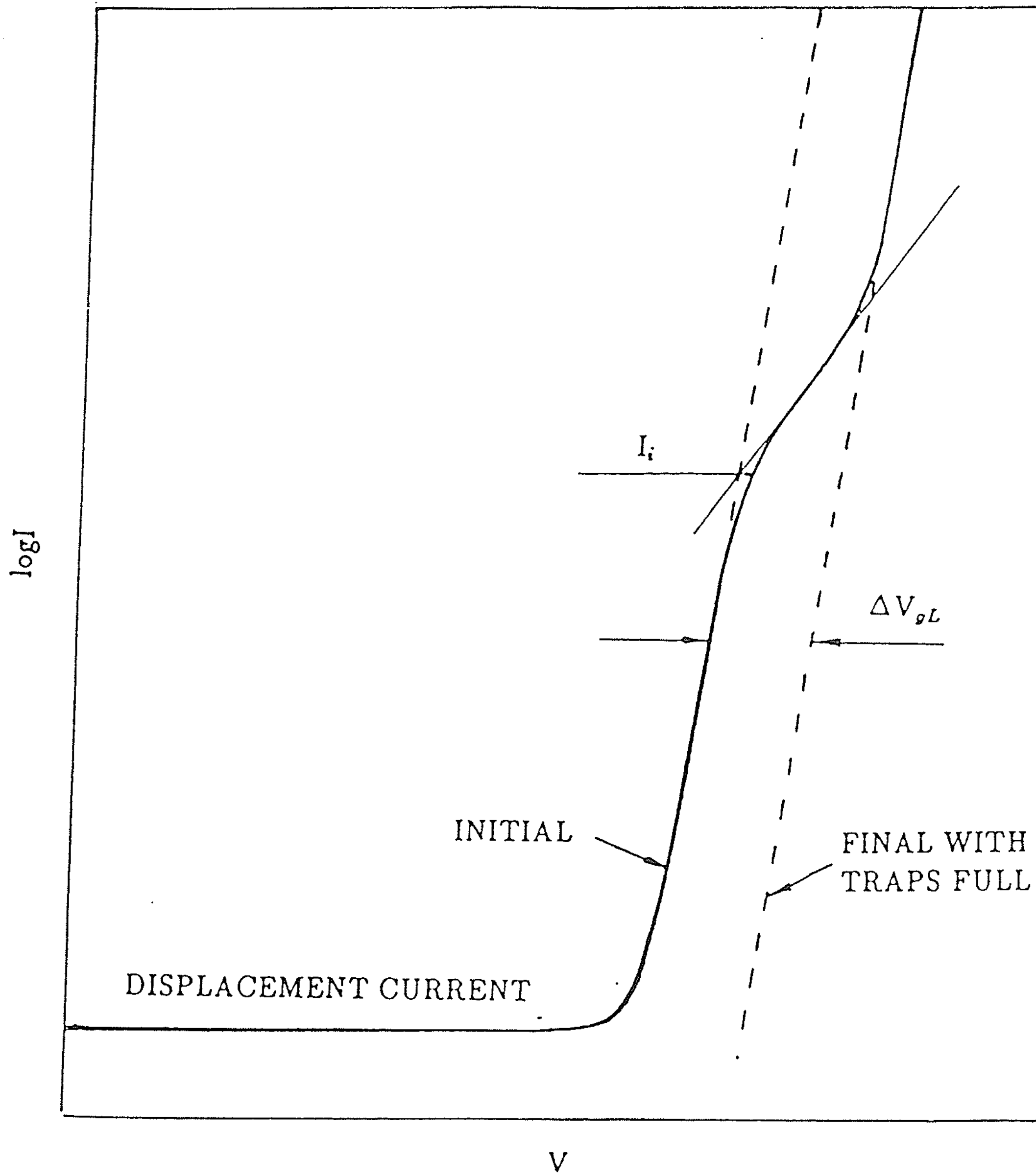


Figure 3.3 Schematic ramp I-V curve illustrating the position of the current near the start of the electron injection I_i and electron trapping ledge width ΔV_{gL}. Dashed curves are the Fowler-Nordheim characteristics before and after trapping.

3.4 Results and Discussion

3.4.1 Parameters obtained from C-V and I-V measurements

From the maximum capacitance in high-frequency C-V and the electron trapping ledge in the ramp I-V measurements made on the samples deposited at 275^oC, 300^oC, 325^oC and 350^oC, the thickness of the oxide and injection current per unit area near the start of electron trapping and width of trapping ledge were found and listed in Table 3.1. In ramp I-V measurements on the samples deposited at 225^oC and 250^oC, catastrophic breakdown occured before reaching the trapping ledge. As can be seen, the higher the deposition temperature, the larger the injection current density and the smaller the width of electron trapping ledge. This indicates that thin films of SiO_2 deposited at higher temperatures have fewer electrically active defects in the films. Significant current injection from silicon substrate for all the samples deposited at the various temperatures required electric field > 6 MV/cm. Although it depends on the ramp rate, the injection current during trapping is much lower in PECVD SiO_2 films than in thermal oxide film at same ramp rate[9], indicating that the trapping probability of electron traps in PECVD SiO_2 films was much higher than that in thermal oxide films.

Table 3.1. Oxide thickness, injection current density and trapping ledge width of the samples deposited at 275° C, 300° C, 325° C and 350° C.

$T_d (^o C)$	d (A)	$J_i (\mu A/cm^2)$	ΔV_{gL} (V)
275	579	10.8	7.0
300	575	10.0	6.0
325	543	12.0	5.0
350	579	14.0	4.0

3.4.2 Centroid of trapped electron distribution

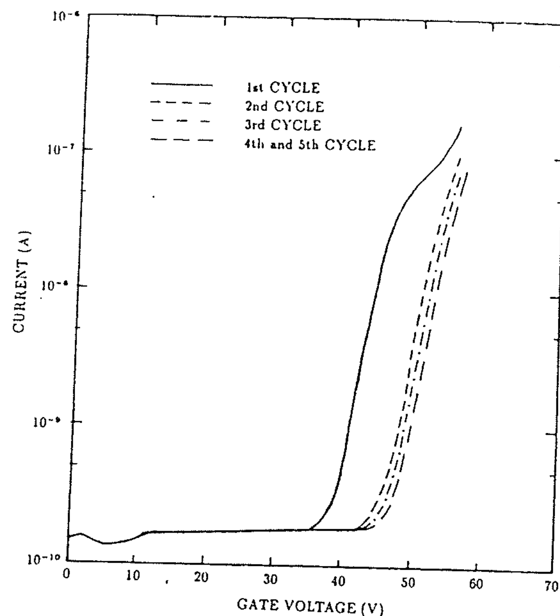
The sequential ramp I-V and high-frequency C-V measurements have been made to obtain flatband voltage shift ΔV_{fb} and gate voltage shift ΔV_g for the samples deposited at $300^o C$ after postmetallization anneal and those deposited at $275^o C$ before postmetallization anneal. The results are shown in Figure 3.4 and Figure 3.5. The centroids of trapped electron distribution and numbers of trapped electrons per unit area calculated from Eqs.(3.16) and (3.17) are listed in Table 3.2 and Table 3.3. It was shown that the postmetallization anneal had little effect on the centroid of trapped electron distribution. The centroids of trapped electron distribution were near the middle of the oxide, indicating that the electron traps were uniformly distributed in the oxide. This was quite different from the thermal oxide, in which the intrinsic electron traps (those related to oxide formation instead of following processing steps such as etching, lithography and ion implantation) were located near the interface, particularly $Al-SiO_2$ interface[7], where they initially entered the oxide. The reason for the uniform distribution of electron traps in PECVD SiO_2 films may be the hydrogen (most rapidly diffusing water related species) in the reactive gases, which introduced electron traps throughout the deposited oxide.

Table 3.2 Distribution centroid and density of electron traps in the sample deposited at 300° C after postmetallization anneal.

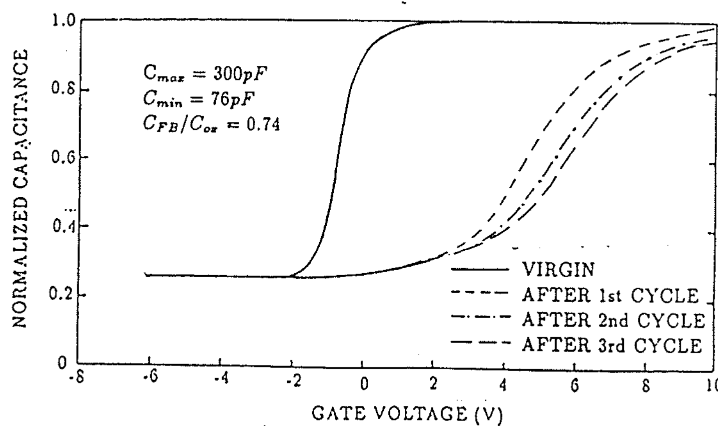
Ramp I-V Cycle	ΔV_g (V)	ΔV_{fb} (V)	x_o (d)	N_o ($10^{12} cm^{-2}$)
2nd-1st	7	5.80	0.45	4.80
3rd-1st	8	6.65	0.45	5.49
3rd-2nd	1	0.85	0.46	0.69
4th-1st	9	7.05	0.44	6.02

Table 3.3 Distribution centroid and density of electron traps in the sample deposited at 275° C before postmetallization anneal.

Ramp I-V Cycle	ΔV_g (V)	ΔV_{fb} (V)	x_o (d)	N_o ($10^{12} cm^{-2}$)
2nd-1st	7.5	6.70	0.47	5.14
3rd-2nd	1.5	1.25	0.45	1.00
3rd-1st	9.0	7.95	0.47	6.14

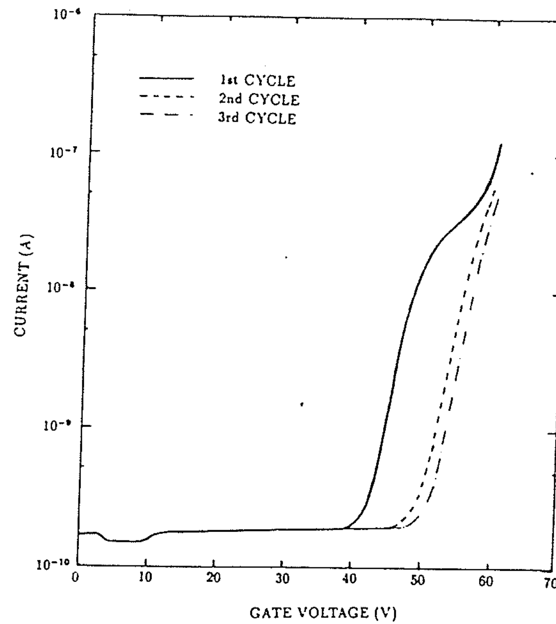


(a)

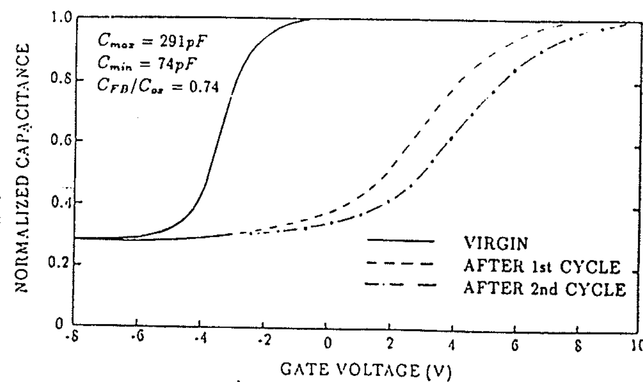


(b)

Figure 3.4 Sequential ramp I-V and C-V measurements on the sample deposited at $300^{o}C$ after postmetallization anneal (a) five cycles of the current as a function of positively ramped (0.65 V/sec) gate voltage (b) high-frequency capacitance as a function of gate voltage before cycling (virgin) and after each cycle.



(a)



(b)

Figure 3.5 Sequential ramp I-V and C-V measurements on the sample deposited at 275^oC before postmetallization anneal (a) three cycles of the current as a function of positively ramped (0.65 V/sec) gate voltage (b) high-frequency capacitance as a function of gate voltage before cycling (virgin) and after each cycle.

3.4.3 Capture cross section and density of electron traps

The ramp I-V curves of the samples deposited at 275^oC, 300^oC, 325^oC and 350^oC are shown in Figure 3.6. The electron trapping ledges and current densities near the start of the ledges were measured from the ramp I-V curves. Using Eqs.(3.10) to (3.13) and previously obtained results of distribution centroid the capture cross section, density of electron traps, trapping probability and density of bulk oxide charge were calculated and listed in Table 3.4. The trapping probability of electron traps in PECVD SiO_2 films with deposition temperatures of 275^oC, 300^oC, 325^oC and 350^oC were all on the order of 10^{-3}, which verified the second assumption $(N_o \sigma_n) \leq 0.3$ made to obtain Eq.(3.9). Although the densities of electron traps in PECVD SiO_2 films with different deposition temperatures were all on the same order $(10^{12} cm^{-2})$ as those in thermal oxide film[9], the electron capture cross section of these bulk traps in all PECVD SiO_2 samples $(\sim 10^{-15} cm^2)$ were much larger than those in thermal oxide film $(\sim 10^{-20} cm^2)$[9], making the trapping probability higher for the injected electrons by Fowler-Nordheim tunneling. This also led to much lower injection currents in PECVD SiO_2 films than in thermal oxide film[9].

Table 3.4 Trapping probability, capture cross section, density of electron traps and charge density of the samples deposited at 275° C, 300° C, 325° C and 350° C.

T_d (^{o}C)	$(\sigma_n N_o)$ (10^{-3})	σ_n $(10^{-15} cm^2)$	N_o $(10^{12} cm^{-2})$	Q_{ot} $(10^{-7} C/cm^2)$
274	8.98	1.73	5.22	8.35
300	7.79	1.73	4.50	7.20
325	6.87	1.73	3.97	6.38
350	6.47	2.17	2.98	4.77

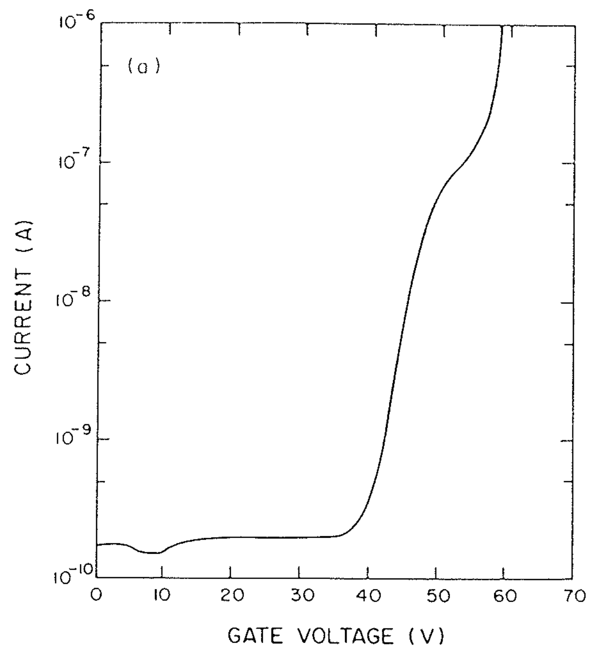


Figure 3.6.(a) The ramp I-V curve of the sample deposited at 275° C.

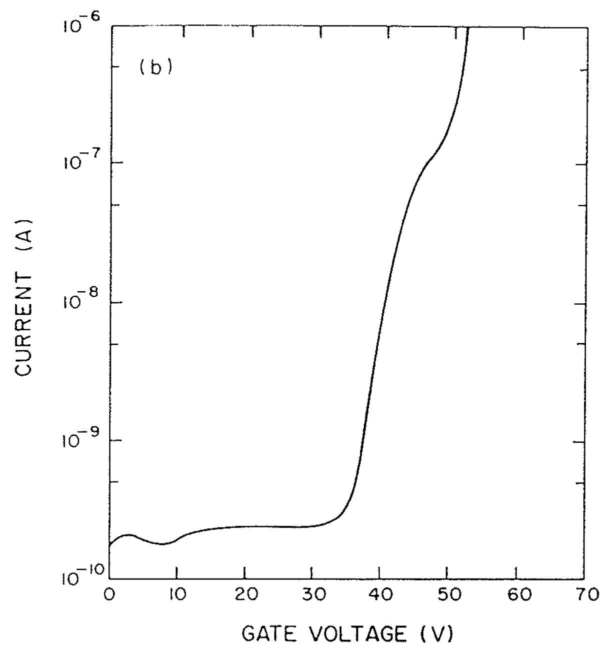


Figure 3.6.(b) The ramp I-V curve of the sample deposited at 300° C.

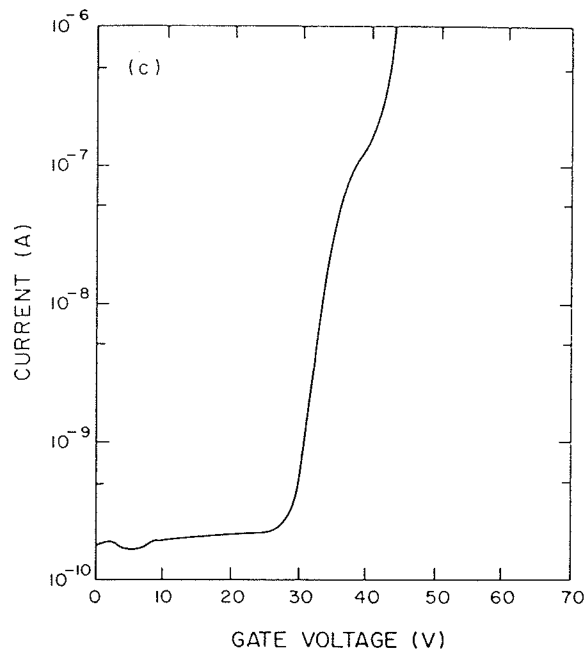


Figure 3.6.(c) The ramp I-V curve of the sample deposited at 325°C.

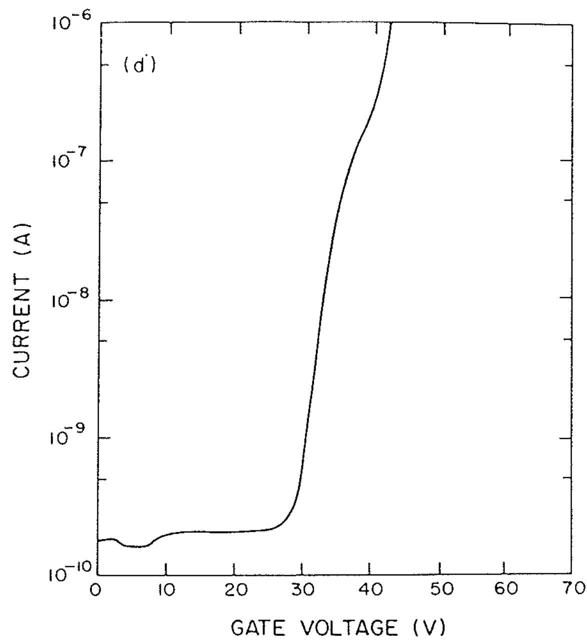


Figure 3.6.(d) The ramp I-V curve of the sample deposited at 350°C.

3.4.4 Effect of deposition temperature on the density of electron traps

The width of electron trapping ledge decreased linearly with increasing deposition temperature and hence so did the density of electron traps, which was, according to Eq.(3.11), proportional to the width of electron trapping ledge. The width of electron trapping ledges were measured from the ramp I-V curves and the densities of electron traps and trapped charge were calculated and listed in Table 3.5. The width of electron trapping ledge as a function of deposition temperature is shown in Figure 3.7. It is believed these were water-related electron traps as determined in [12], fewer traps are present at higher temperatures because less water is incorporated into the oxide. These traps could be removed after heating SiO_2 sample in vacuum at temperatures above 600^oC by driving water out of SiO_2[7]. Electron trapping ledge in PECVD SiO_2 could also be eliminated by a high temperature anneal (1000^oC for 30 min in N_2)[12].

Table 3.5 Effect of deposition temperature on the density of electron traps.

T_d (^{o}C)	ΔV_{gL} (V)	N_o ($10^{12} cm^{-2}$)	Q_{ot} ($10^{-7} C/cm^2$)
275	7.0	5.22	8.35
300	6.0	4.50	7.20
325	5.0	3.97	6.36
350	4.0	2.98	4.77

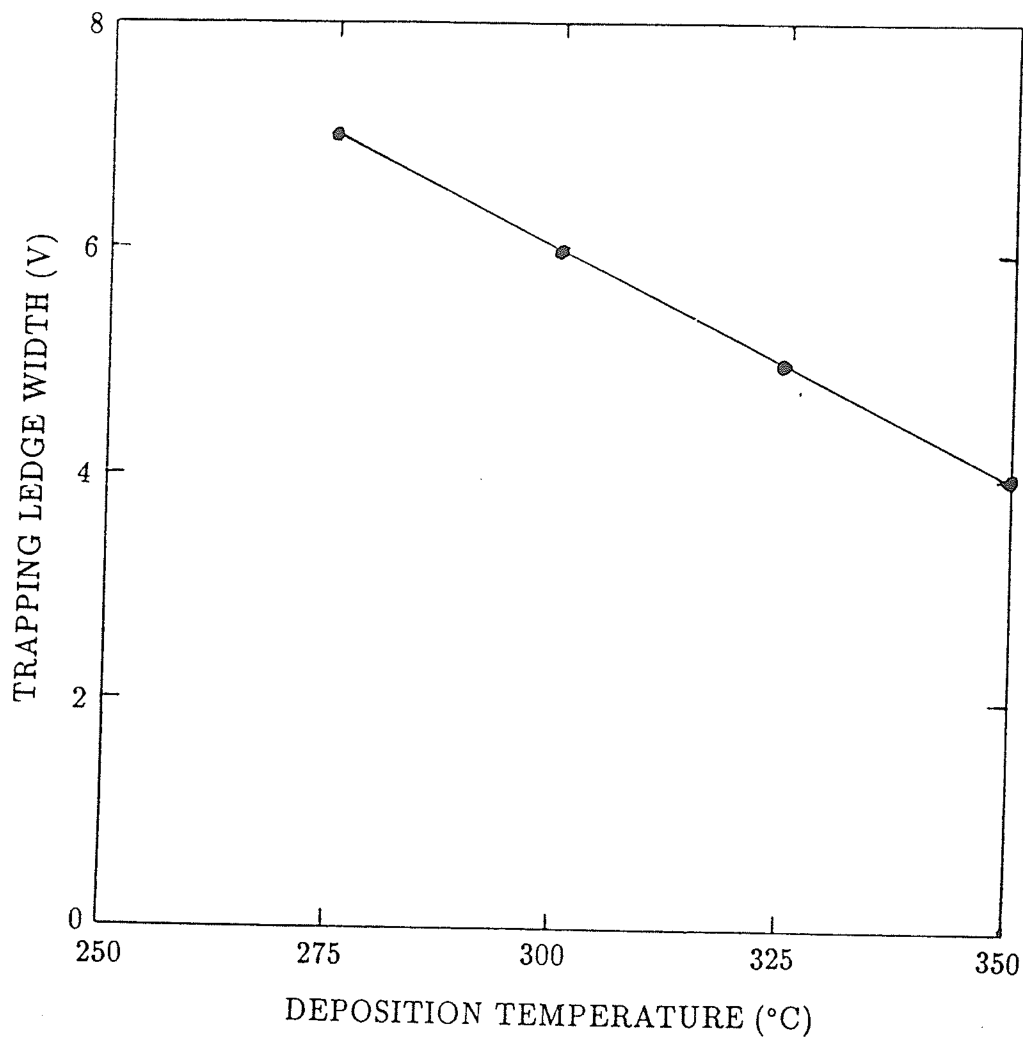


Figure 3.7 Electron trapping ledge width as a function of deposition temperature.

3.4.5 Effect of postmetallization anneal on the properties of electron traps

Figure 3.8 shows the ramp I-V curves made from the samples deposited at $300^{o}C$ before and after postmetallization anneal. Although it could not completely eliminate the electron traps in the bulk of PECVD SiO_2 films, the thermal annealing treatment did improve the properties of the films. This can be seen from the experimental results shown in Table 3.6. The improvement of the properties of the traps in PECVD SiO_2 film through postmetallization anneal was due to the outdiffusion of water in the oxide. This was in agreement with the nature of water-related electron traps, which could only be annealed out at high temperatures[7][12].

Table 3.6 Effect of postmetallization on the properties of electron traps.

Sample type	J_i ($\mu A/cm^2$)	ΔV_{gL} (V)	σ_n ($10^{-15}cm^2$)	N_o ($10^{12}cm^{-2}$)	$(\sigma_n N_o)$ (10^{-3})
300PMA	10.0	6.0	1.7	4.6	7.8
300AD	4.4	7.0	3.4	5.3	17.7

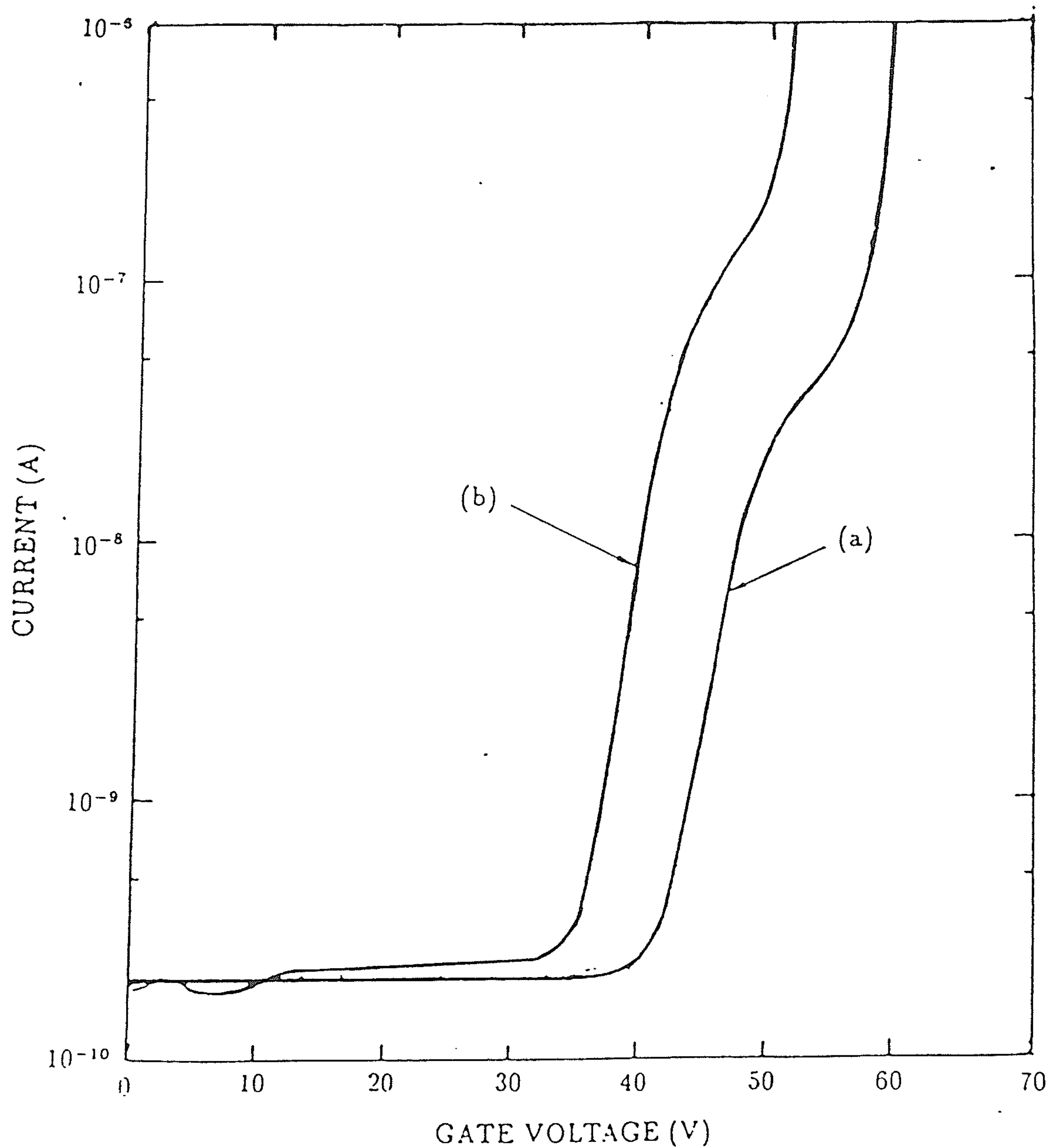


Figure 3.8 The ramp I-V curves of the samples deposited at 300°C (a) before postmetallization anneal (b) after postmetallization anneal.

3.5 Conclusions

Electron trapping in PECVD SiO_2 was studied using Fowler-Nordheim tunneling injection in MOS capacitors. The properties of electron traps in PECVD SiO_2 were quite different from the counterparts in thermal oxide. These traps were uniformly distributed in PECVD SiO_2 films and had much larger capture cross section than that in thermal oxide film, indicating more defects exsited in PECVD SiO_2 films.

The density of electron traps in PECVD SiO_2 was affected by the temperature at which the oxide was deposited. The higher the deposition temperature, the lower the density of electron traps in the oxide. The properties of electron traps in PECVD SiO_2 was also affected by postmetallization anneal. The thermal annealing treatment improved the trapping properties, i.e., lower trapping probability and density of electron traps, although it could not entirely eliminate the traps. Our results are consistent with the source of the electron traps being due to the incorporation of water like complexes in the oxide during deposition.

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CHAPTER 4

NEGATIVE BIAS-TEMPERATURE INSTABILITY IN PECVD SiO_2

4.1 Introduction

The positive charge generated under negative high-field stressing is often referred to as negative bias-temperature instability (NBTI) or slow trapping[1]. This instability can be a major threat to the long-term stability of metal-oxide-semiconductor (MOS) devices. The introduction of traps by this effect would shift the threshold voltage of the MOSFET. The interface traps created at $Si-SiO_2$ interface could also reduce the transconductance and the speed of MOSFET.

In this chapter we will describe our study of the positive charge generated in the bulk of PECVD SiO_2 at room temperature and high temperature (200^oC) under negative high-field stressing using the C-V technique. Experimental results on the samples deposited at 225^oC, 250^oC, 275^oC, 300^oC, 325^oC and 350^oC before and after postmetallization anneal are presented. The NBTI was manifested as a negative shift in the C-V curves due to positive charge creation accompanied by a varying degree of strechout due to generation of interface traps. Positive charge density was calculated from the voltage shift at midgap, which was proved to be a good measure of the increment in fixed charge density[2]. A study is also made to investigate the mechanism of generation of positive charge in PECVD SiO_2 at room temperature before postmetallization anneal.

4.2 Negative Bias-temperature Instability in SiO_2

The negative bias-temperature instability was first reported by Deal et al[3]. Their results measured with an MOS capacitor are shown in Figure 4.1. Curve A is a theoretical high-frequency C-V curve. Curve B is the initial high-frequency C-V curve measured prior to stressing a "sodium free" oxide. Curve C is measured after 2 min at 400^oC under an applied oxide field of -2×10^6V/cm. Curve C has shifted along the voltage axis to more negative voltages, and its shape is distorted compared to curves A and B. The shift of the C-V curve along the voltage axis indicates an increase of positive oxide charge density. The strechout of the C-V curve along the voltage axis or distortion in its shape can be caused by an increase in interface state density D_{it}. Both result from negative bias-temperature stressing.

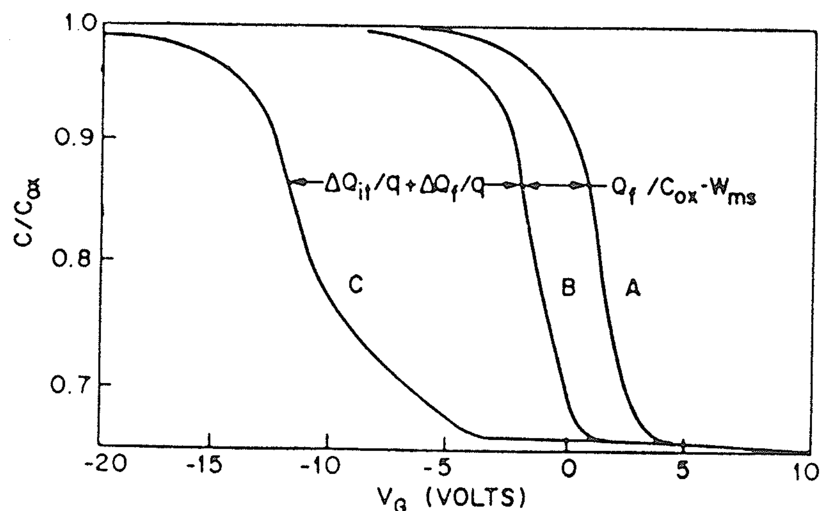

Figure 4.1 High-frequency C-V curves before and after negative bias-temperature stressing, after Deal et al.[3].

Much effort has been made since Deal's work more than twenty years ago to clarify the mechanism of the generation of positive charge in thermally grown oxide. Several possible models have been proposed to explain how positive oxide charge is produced during negative bias stressing. These include: (1) filling of preexistent hole traps in the oxide[4], (2) thermally assisted electron tunneling[5][6], (3) reaction with strained bonds near the $Si-SiO_2$ interface[3][7], (4) formation and migration of oxygen vacancies[8], (5) majority-carrier tunneling via traps[9], and (6) an electrochemical reaction[10]-[12]. Each model is supported by a few experiments, indicating that the mechanism for the effect has not been established.

4.3 Experiments

Two sets of experimental conditions were used in this study. They are: (1) room temperature negative bias-temperature instability (RTNBTI). The samples were stressed at room temperature under a negative gate voltage of -17.45 V (-3 MV/cm) for 0.5 min, 3.5 min, 6.0 min, 20 min, and 30 min consecutively. (2) high temperature negative bias-temperature instability (HTNBTI). The samples were stressed at $200^o C$ under a negative gate voltage of -17.45 V (-3 MV/cm) for 4 min.

4.4 Results and Discussion

4.4.1 RTNBTI in as-deposited PECVD SiO_2

RTNBTI was investigated by the measurements made on the samples deposited at $225^o C$, $250^o C$, $275^o C$, $300^o C$, $325^o C$ and $350^o C$. Five time periods (0.5 min, 3.5 min, 6.0 min, 20 min, and

30 min) were consecutively used to study the cumulative effect of the negative bias stressing on the generation of positive charge. The experimental results from high-frequency C-V measurements are shown in Figure 4.2. Positive charge density was calculated and listed in Table 4.1. Compared to the work of D.Lu et al.[13], RTNBTI in PECVD SiO_2 was higher than that in thermal oxide with the Al deposited via filament evaporation (2-8 $\times 10^{10}$q/cm^2) and lower than that in thermal oxide with the Al deposited via electron beam evaporation (>2.5$\times 10^{12}$q/cm^2), suggesting that the damage induced defects from the plasma during oxide deposition was less than that from soft x-rays during electron beam Al metallization in terms of negative bias-temperature instability[14].

Table 4.1 RTNBTI in the samples deposited at 225°C, 250°C, 275°C, 300°C, 325°C and 350°C before PMA.

T_d (^{o}C)	RTNBTI (10^{10}q/cm^2) 0.5 min	3.5 min	6 min	20 min	30 min
225	19.69	15.31	13.13	17.06	
250	11.70	11.70	7.80	13.65	7.80
275	3.73	7.83	3.73	7.46	3.73
300	4.53	9.06	4.53	9.51	
325	3.78	3.78	3.78	4.35	
350	8.35	7.52	3.76	6.26	2.09

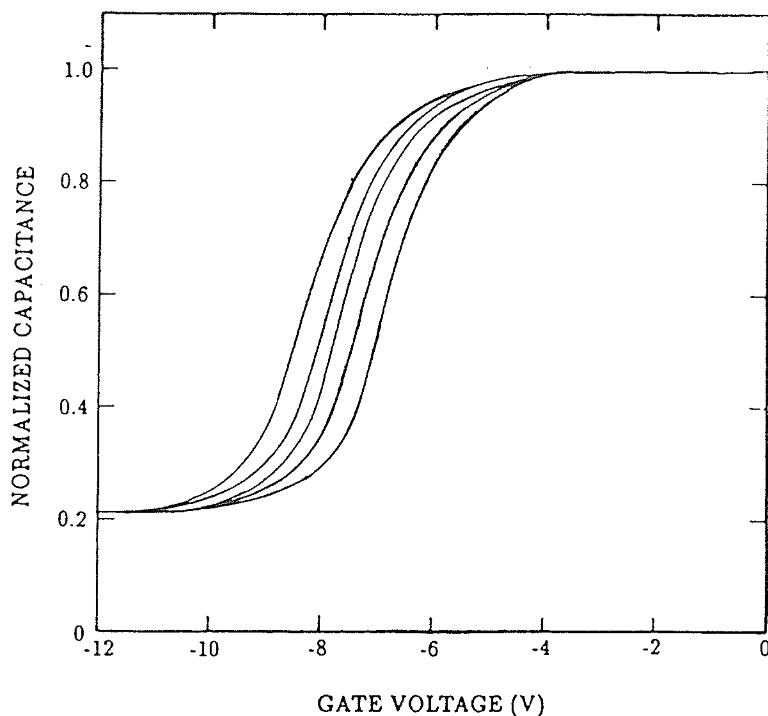

Figure 4.2.(a) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min and 20 min (from right to left) on the sample deposited at 225° C before PMA.

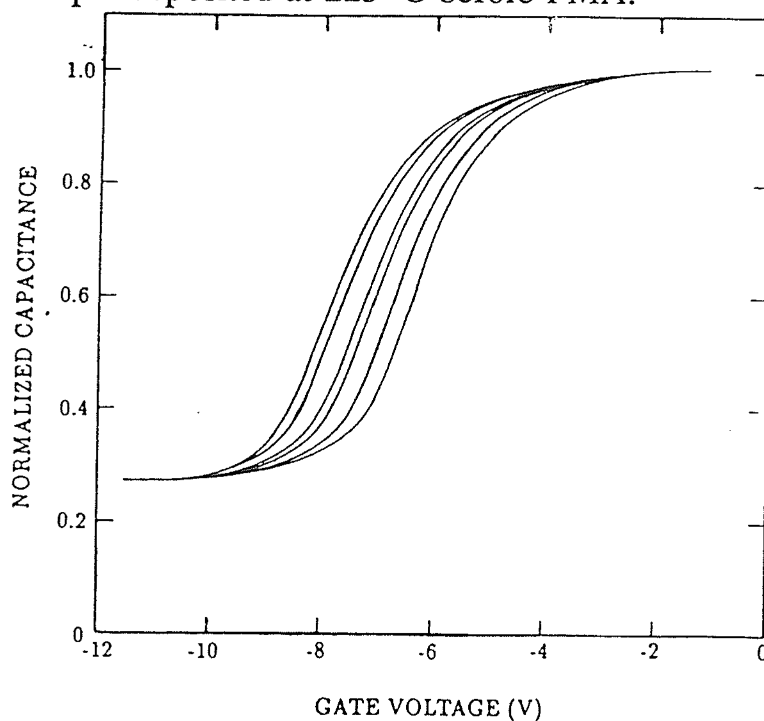

Figure 4.2.(b) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min, 20 min, and 30 min (from right to left) on the sample deposited at 250° C before PMA.

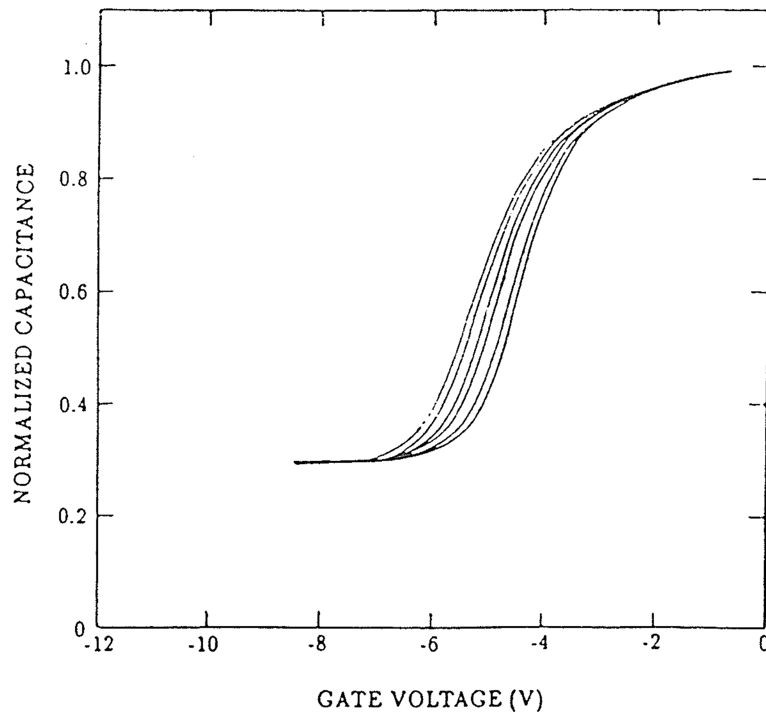

Figure 4.2.(c) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min, 20 min, and 30 min (from right to left) on the sample deposited at 275° C before PMA.

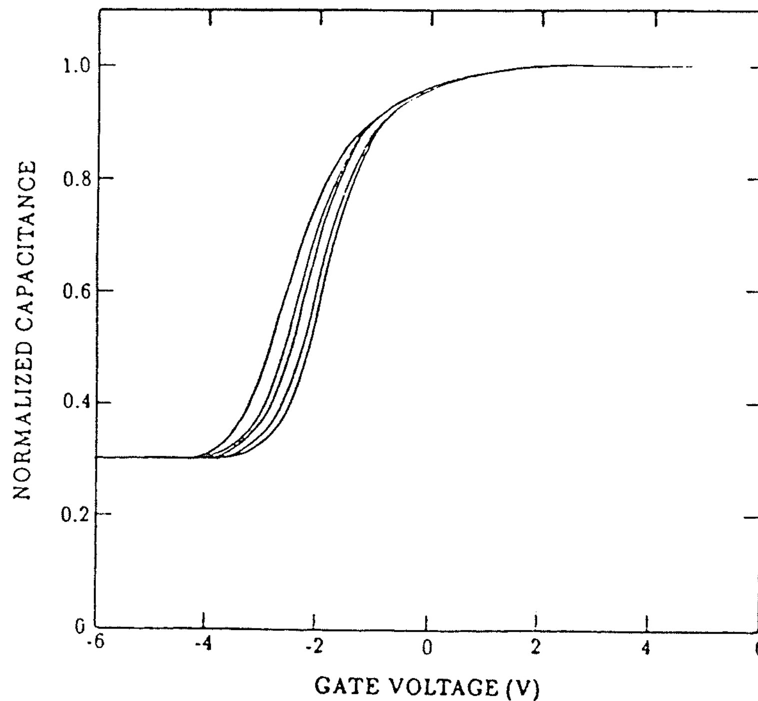

Figure 4.2.(d) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min and 20 min (from right to left) on the sample deposited at 300° C before PMA.

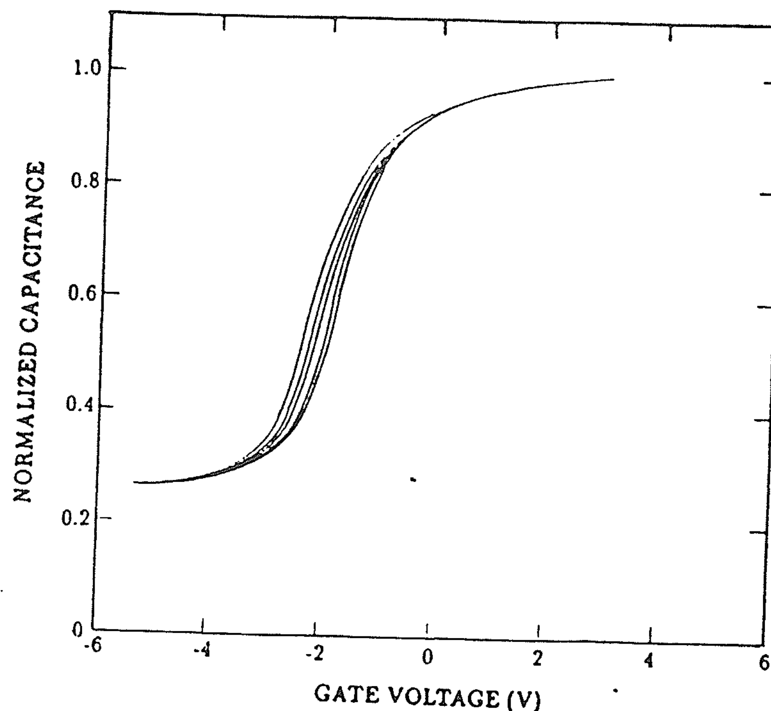

Figure 4.2.(e) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min and 20 min (from right to left) on the sample deposited at 325°C before PMA.

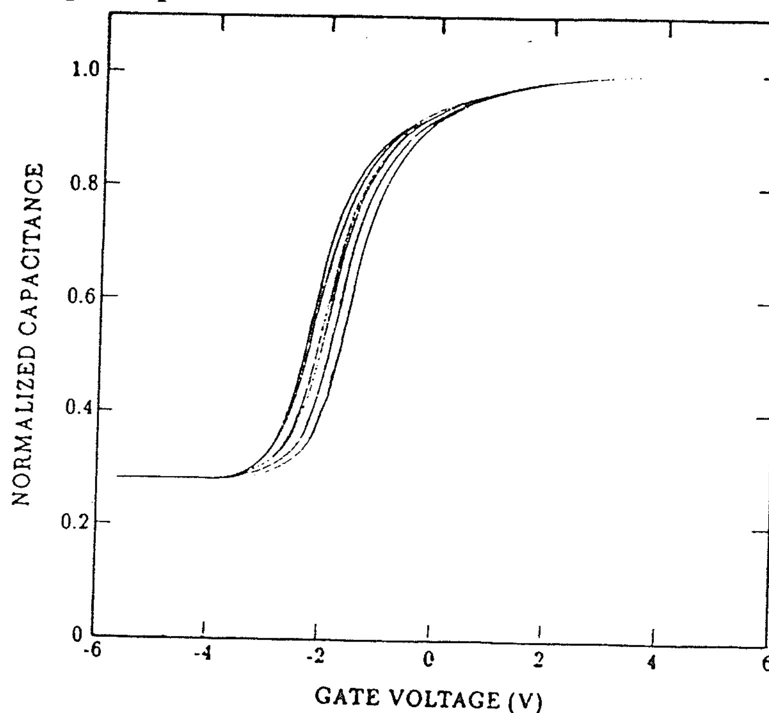

Figure 4.2.(f) H-F C-V curves after RT stressing (-3 MV/cm) for 0 min, 0.5 min, 3.5 min, 6.0 min, 20 min, and 30 min (from right to left) on the sample deposited at 350°C before PMA.

4.4.2 HTNBTI in as-deposited PECVD SiO_2

The as-deposited PECVD SiO_2 samples exhibited dramatic NBTI under negative bias stressing at high temperature (200° C). The severe HTNBTI evident in Figure 4.3 presumably resulted from the radiation damage induced by the plasma during film growth. The positive charge densities generated under negative bias stressing at high temperature in the samples deposited at 250° C, 275° C, 300° C, 325° C and 350° C were calculated and listed in Table 4.2. HTBNTI in PECVD SiO_2 was also higher than that in thermal oxide with the Al deposited via filament evaporation ($2.0\times10^{11} q/cm^2$) by an order of magnitude same as in RTBNTI case[13]. At first sight PECVD SiO_2 films deposited at lower temperatures seemed to have better HTNBTI as they generated less positive charges under stress. Actually there were two processes which took place during HTNBTI experiments. First the samples were thermally annealed when the temperature in the substrates were increased. Then positive charges were generated again when negative bias was applied at high temperature. It was noted that the total shift of the C-V curve along the voltage axis decreased with increasing deposition temperature. This implied that PECVD SiO_2 films deposited at higher temperature had less electrically active centers in the bulk.

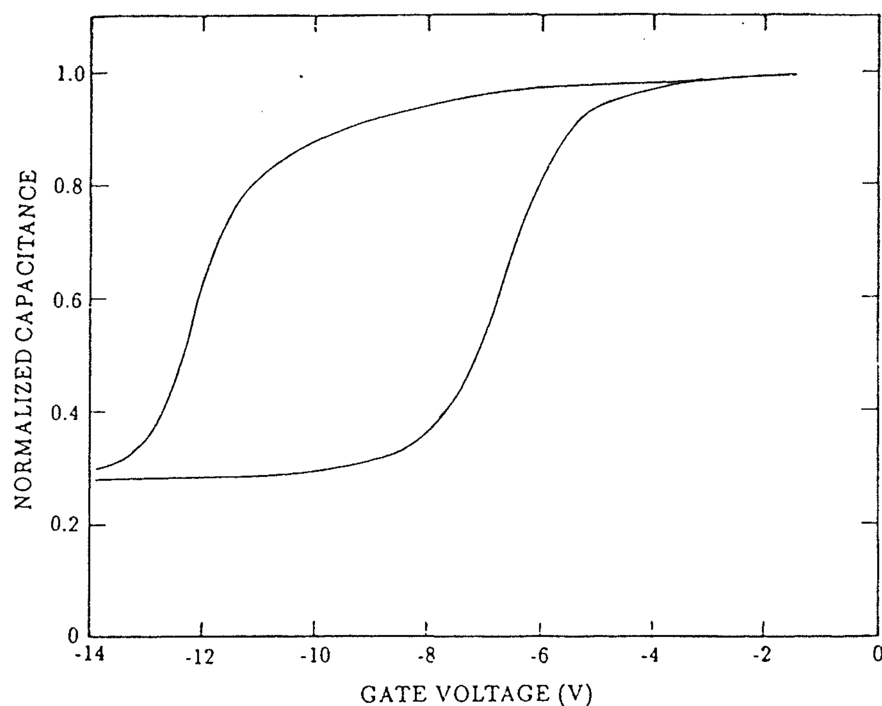

Figure 4.3.(a) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200^oC for 4 min on the sample deposited at 250^oC before PMA.

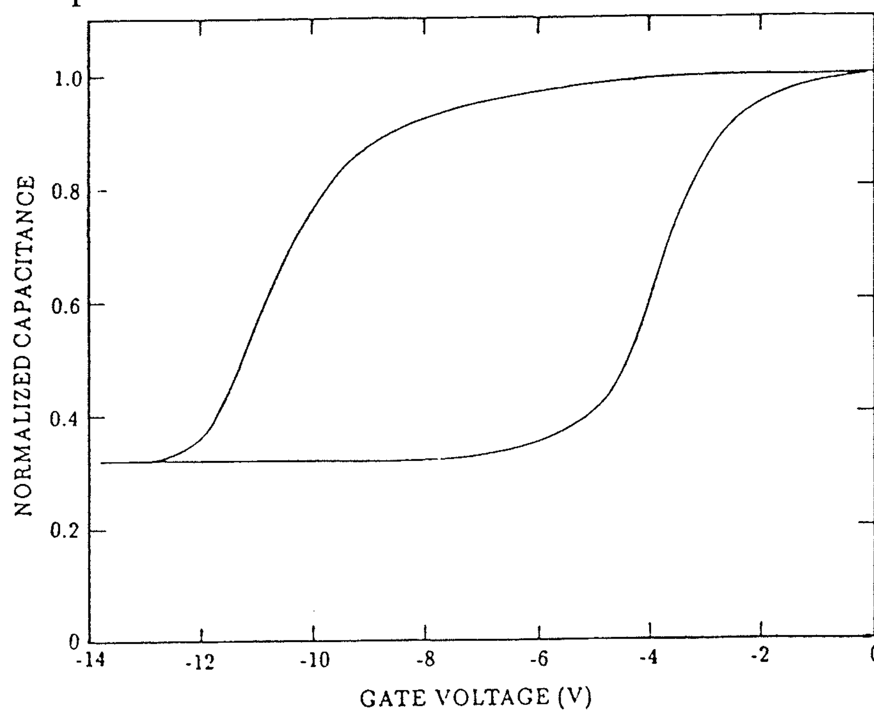

Figure 4.3.(b) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200^oC for 4 min on the sample deposited at 275^oC before PMA.

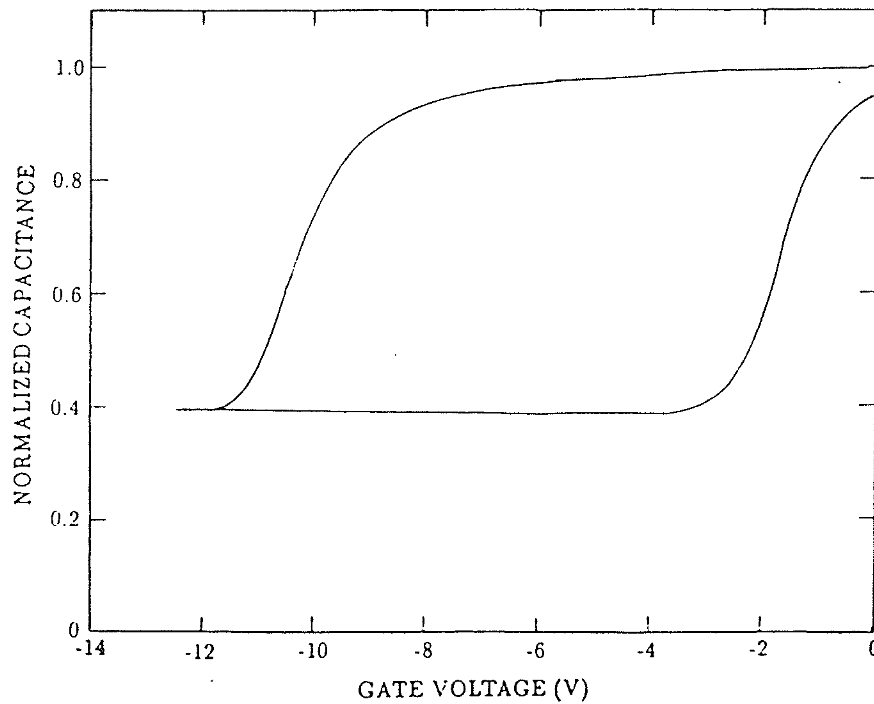

Figure 4.3.(c) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 300°C before PMA.

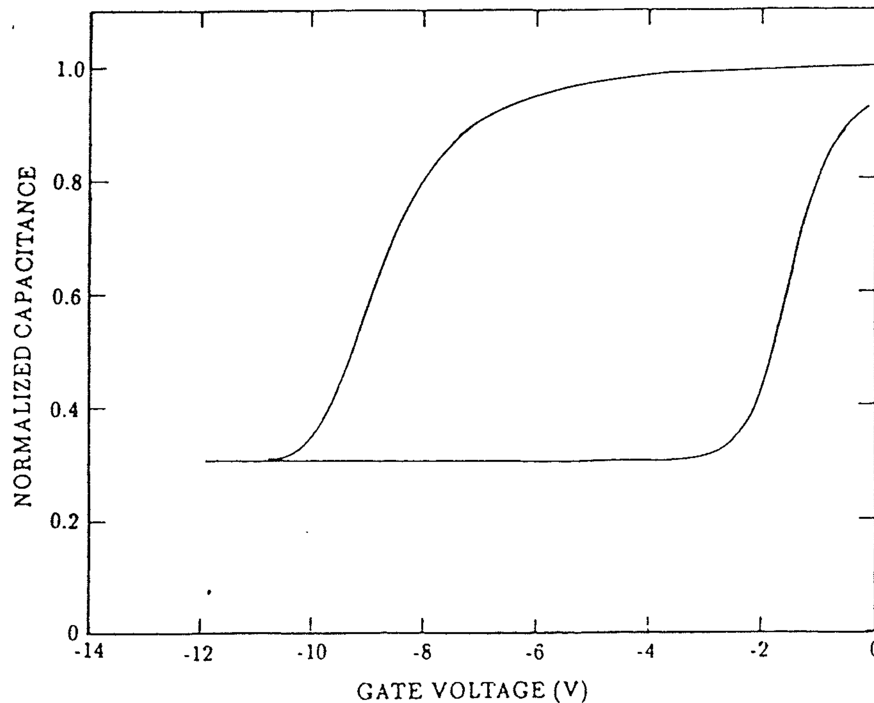

Figure 4.3.(d) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 325°C before PMA.

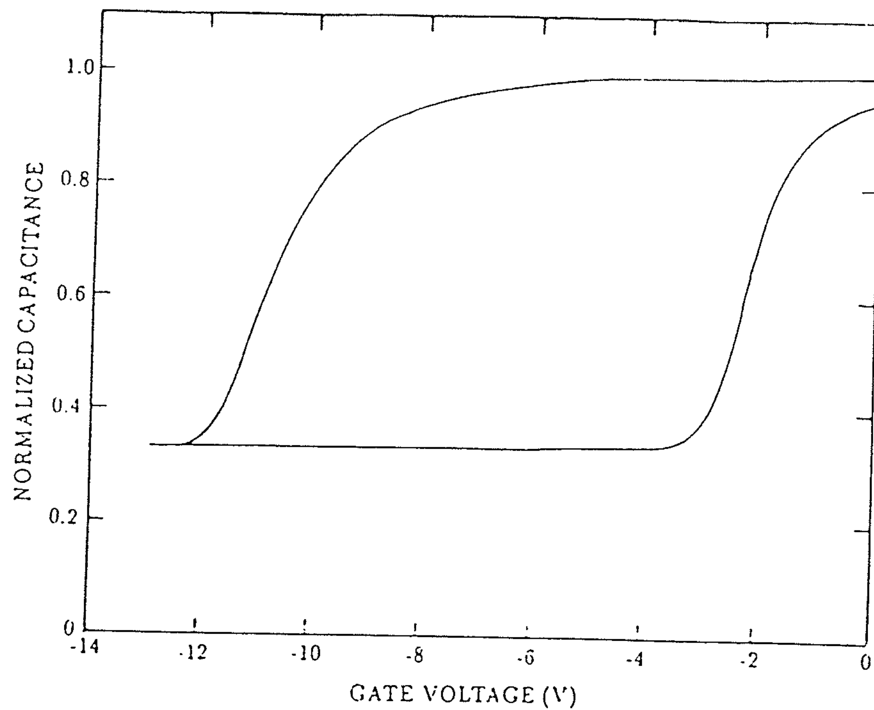

Figure 4.3.(e) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 350°C before PMA.

Table 4.2 Positive charge generated under negative bias stressing (-3 MV/cm) at 200°C for 4 min in the samples deposited at 250°C,275°C, 300°C,325°C and 350°C before PMA.

T_d(^{o}C)	250	275	300	325	350
HTNBTI(10^{12}q/cm^2)	1.70	2.66	2.77	2.38	3.60

4.4.3 NBTI in thermally annealed PECVD SiO_2

Thermal annealing can lead to significant decrease in NBTI. The effect of the plasma damage may not be important in practice because the large room temperature NBTI can be easily removed by a standard postmetallization anneal in forming gas ($10\%H_2$-$90\%N_2$) at 400^oC for 30 min. Room temperature stressing under -3 MV/cm for 60 min revealed no measurable instability for the samples deposited at 225^oC, 250^oC, 275^oC, 300^oC, 325^oC and 350^oC. High temperature NBTI measurements were performed on the samples deposited at 250^oC, 300^oC and 350^oC. The quasi-static C-V measurements were also made on the samples deposited at 250^oC and 350^oC to investigate the change in interface traps. The high-frequency and quasi-static C-V curves are shown in Figure 4.4. The generated positive charge and interface traps were calculated and listed in Table 4.3. The HTNBTI in PECVD SiO_2 was on the same order ($10^{11}q/cm^2$) as that in thermal oxide after PMA except for the sample deposited at 350^oC[13]. The large positive charge generated in the sample deposited at 350^oC may be due to a large interface charge that existed initially[1]. The interface trap density at midgap was also increased during stressing as reported before[1][13].

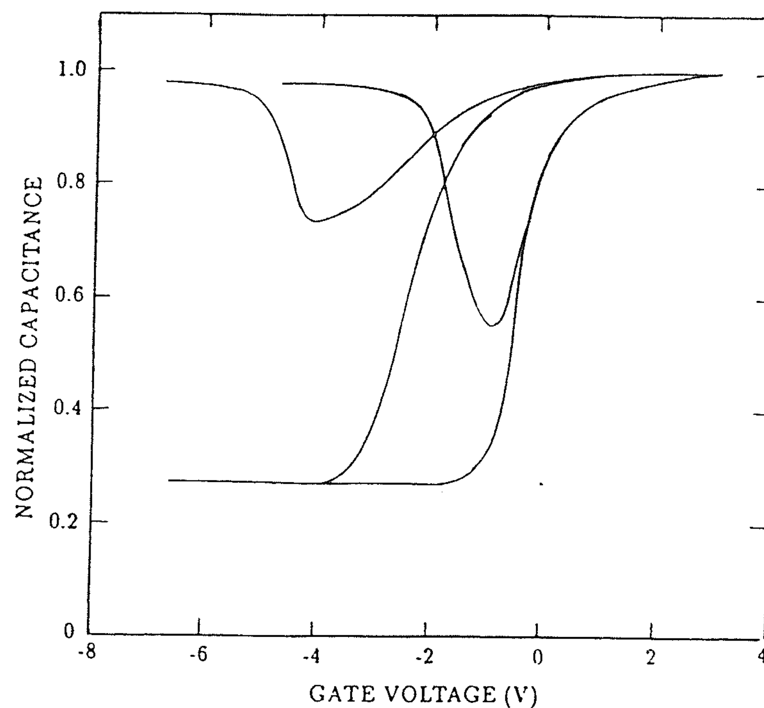

Figure 4.4.(a) High-low frequency C-V curves measured before (curves at right) and after (curves at left) HT stressing (-3 MV/cm) for 4 min on the sample deposited at 250°C after PMA.

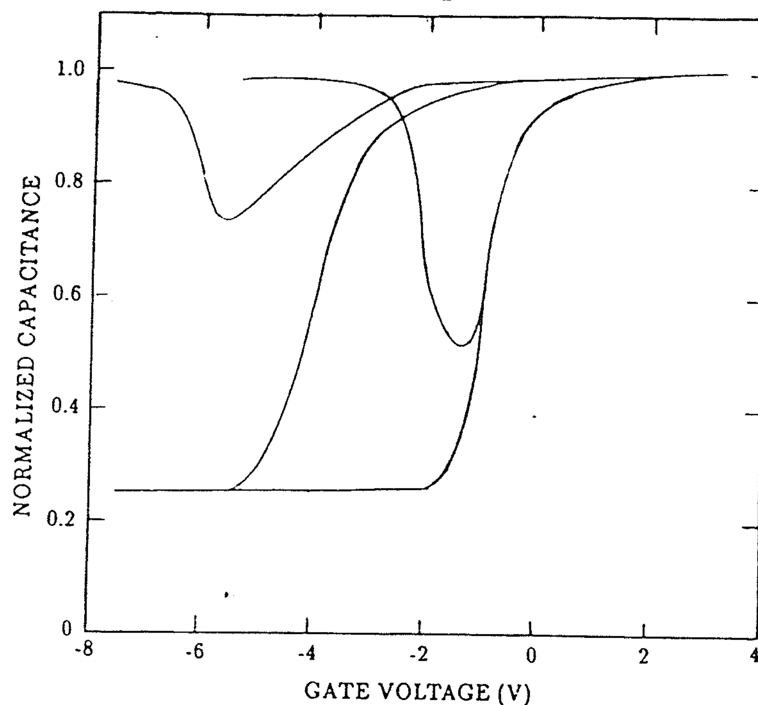

Figure 4.4.(b) High-low frequency C-V curves measured before (curves at right) and after (curves at left) HT stressing (-3 MV/cm) for 4 min on the sample deposited at 350°C after PMA.

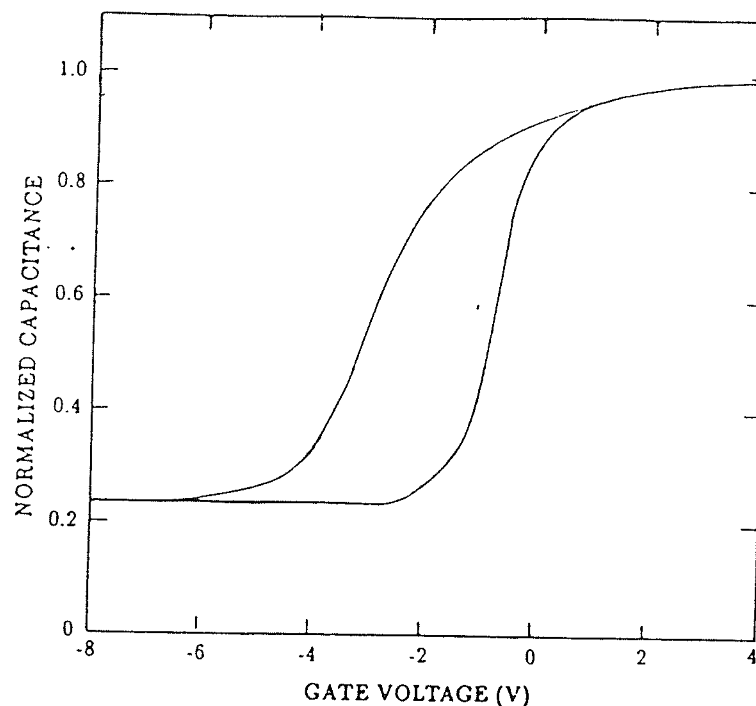

Figure 4.4.(c) High frequency C-V curves measured before (curve at right) and after (curve at left) negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 300°C after PMA.

Table 4.3 Positive charge and interface traps generated under negative bias stressing (-3 MV/cm) at 200°C for 4 min in the samples deposited at 250°C, 300°C and 350°C after PMA.

T_d (^{o}C)	HTNBTI ($10^{11}q/cm^2$)	$D_{it_{mg}}$ (unstressed) ($10^{11}cm^{-2}eV^{-1}$)	$D_{it_{mg}}$ (stressed) ($10^{11}cm^{-2}eV^{-1}$)
250	.4.18	4.30	11.96
300	8.35	not measured	not measured
350	12.45	4.89	13.77

4.4.4 HTNBTI in as-deposited PECVD SiO_2 after surface cleaning

It was found that the cleanliness of the sample surface had a significant effect on the NBTI in the MOS capacitors. The samples deposited at 225^oC, 250^oC, 275^oC, 300^oC, 325^oC and 350^oC were cleaned using acetone, methanol and trichloroethylene before metallization. Then the high temperature NBTI measurements were made on these samples using the high-frequency C-V technique. The experimental results are shown in Figure 4.5. The positive charge densities were calculated and listed in Table 4.4. Compared to the results in Table 4.2, the high temperature NBTI was reduced after the cleaning of the sample surface but still higher than that in thermal oxide[13].

Table 4.4 Positive charge generated under neagtive bias stressing (-3 MV/cm) at 200^oC for 4 min on the samples deposited at 225^oC, 250^oC, 275^oC, 300^oC, 325^oC and 350^oC after surface cleaning.

T_d (^{o}C)	225	250	275	300	325	350
HTNBTI (10^{11}q/cm^2)	4.00	2.17	11.94	10.88	11.00	13.56

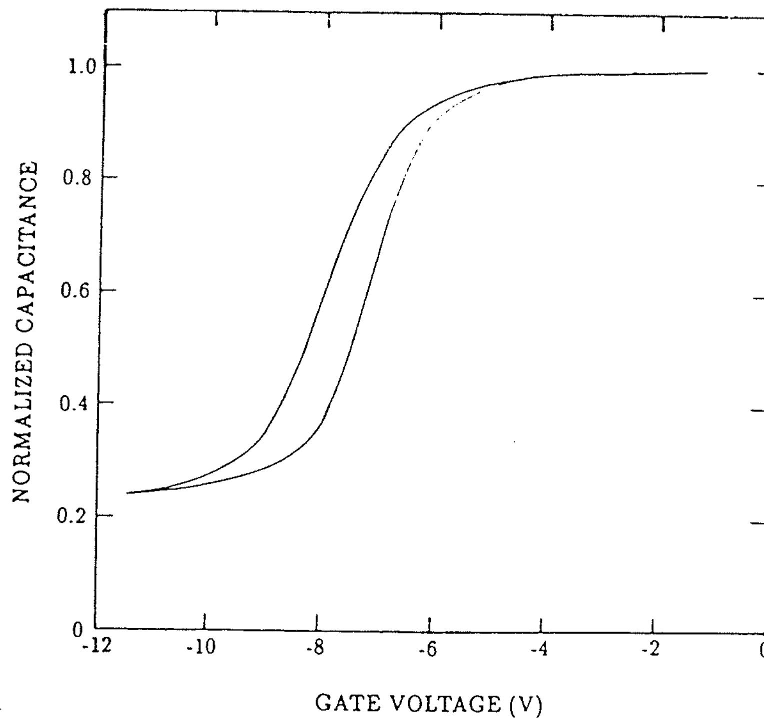

Figure 4.5.(a) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 225°C after surface cleaning.

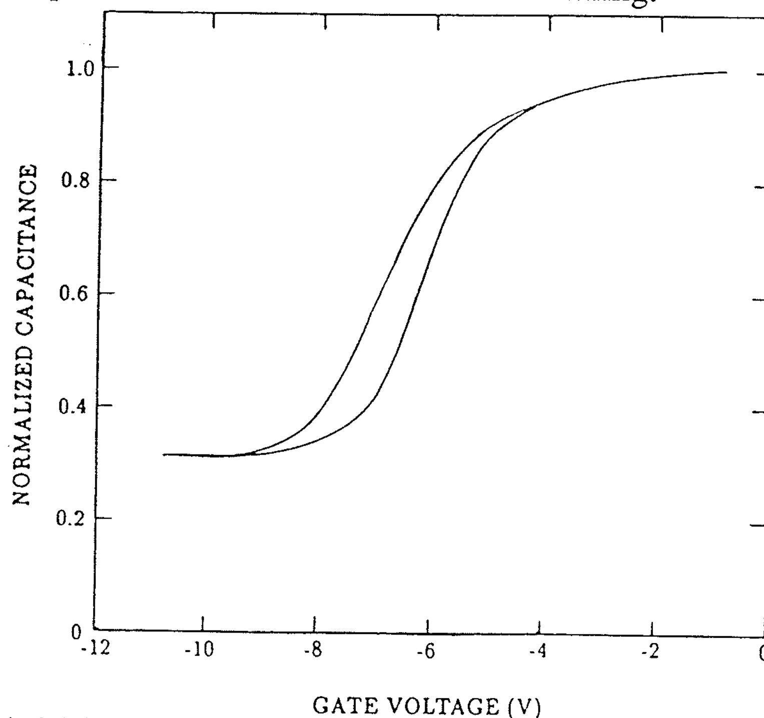

Figure 4.5.(b) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C foe 4 min on the sample deposited at 250°C after surface claening.

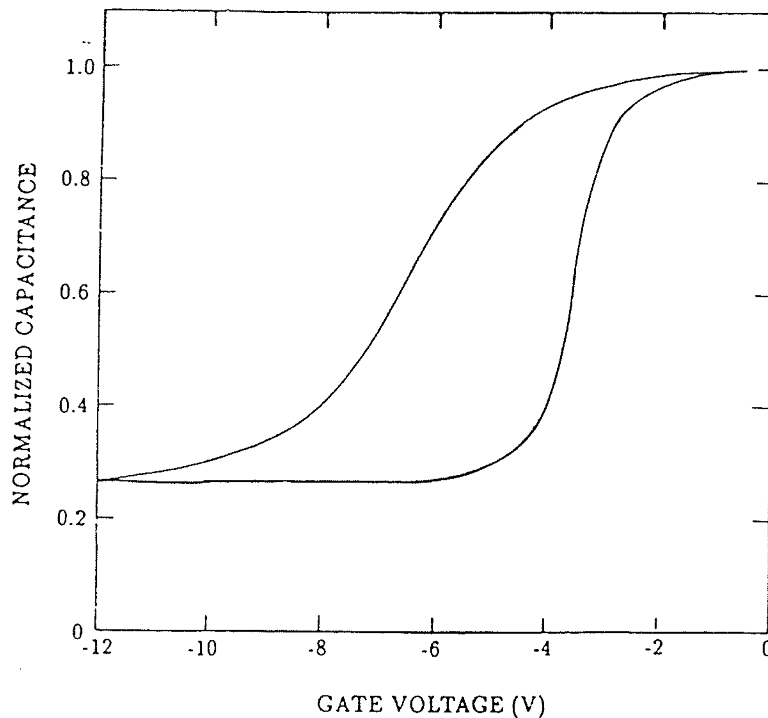

Figure 4.5.(c) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 275°C after surface cleaning.

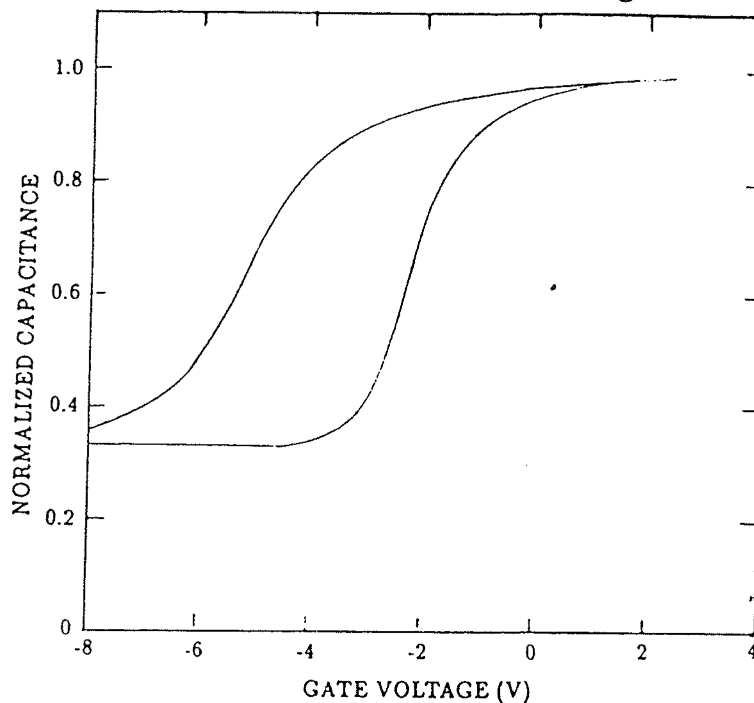

Figure 4.5.(d) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 300°C after surface cleaning.

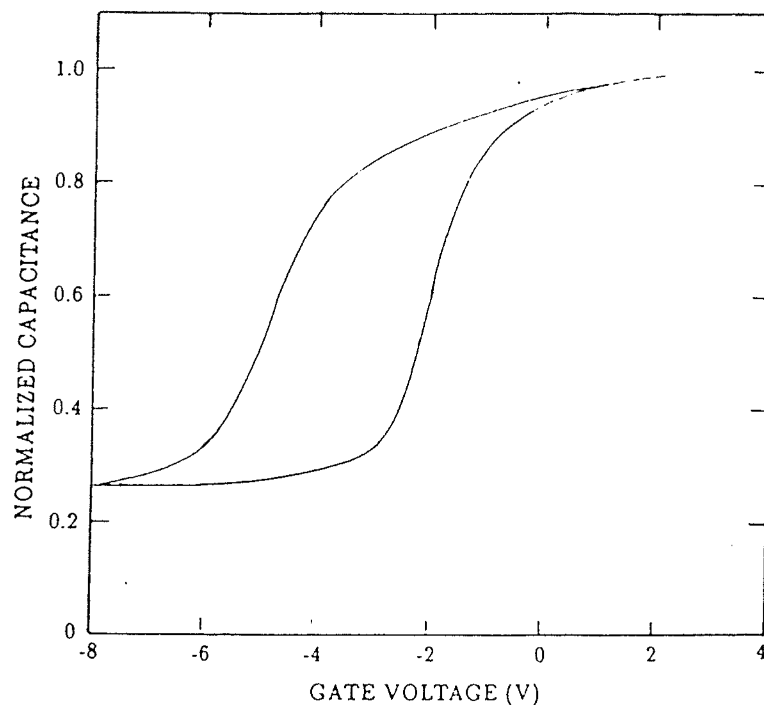

Figure 4.5.(e) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 mV/cm) at 200°C for 4 min on the sample deposited at 325°C after surface cleaning.

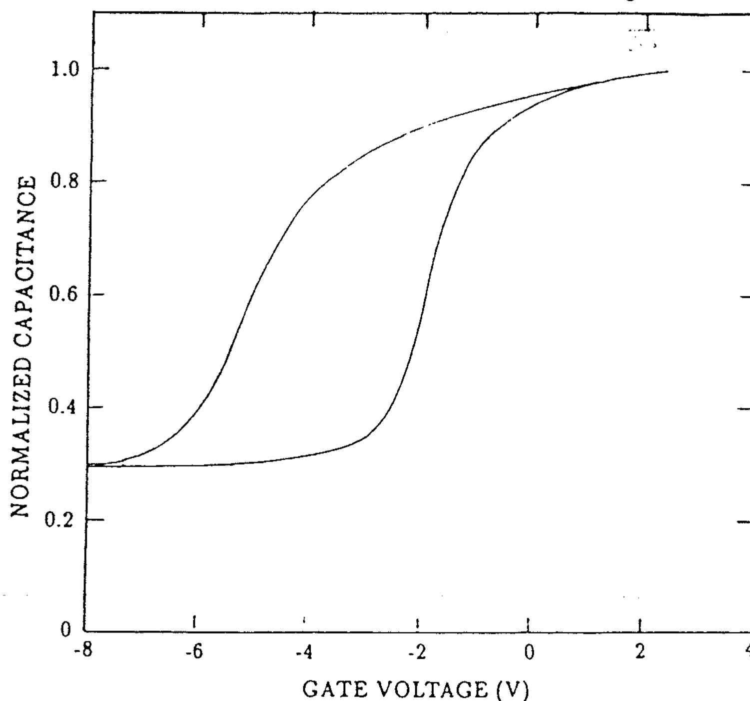

Figure 4.5.(f) The voltage shift in high-frequency C-V curve after negative bias stressing (-3 MV/cm) at 200°C for 4 min on the sample deposited at 350°C after surface cleaning.

4.4.5 Speculation on the mechanism for NBTI

As stated before, there are many models available to explain the generation of positive charge under negative bias stressing. A study was made in this thesis to investigate the possible mechanism responsible for the NBTI in PECVD SiO_2. A negative bias (-3 MV/cm) was applied on the gate of the sample. A dc current was detected during the stressing. The voltage shifts in the high-frequency C-V curves were qualitatively proportional to the magnitudes of the current for periods of time (0.5 min, 3.5 min, 13 min, 3 min). Finally the current decreased to zero while the voltage shift in the C-V curve approaching the maximum after negative bias stressing for about 20 min. Then the polarity of the current changed when the stressing continued. The C-V curve correspondingly shifted to the opposite direction. Afterwards, the current and C-V curve fluctuated around the zero and maximum respectively. A typical experimental result made on the sample deposited at 225^oC is shown in Figure 4.6. This result is consistent with the works of Haywood et al and Lu et al[4][13] and shows that the intrinsic hole traps preexist in PECVD SiO_2 and are filled by holes flowing into the oxide from the $Si-SiO_2$ interface under negative bias stressing. The trapping probability decreases and detrapping probability increases with the increase in the amount of filled traps. Eventually, the trapping and detrapping reaches a dynamic equilibrium. In the high temperature NBTI case, the situation is more complex. The positive charge generated in PECVD SiO_2 at high temperature under negative bias stressing was due to hole trapping at preexistent and newly created trap sites since the voltage shifts in C-V curves at high temperature were much larger than the maximum shifts at room temperature.

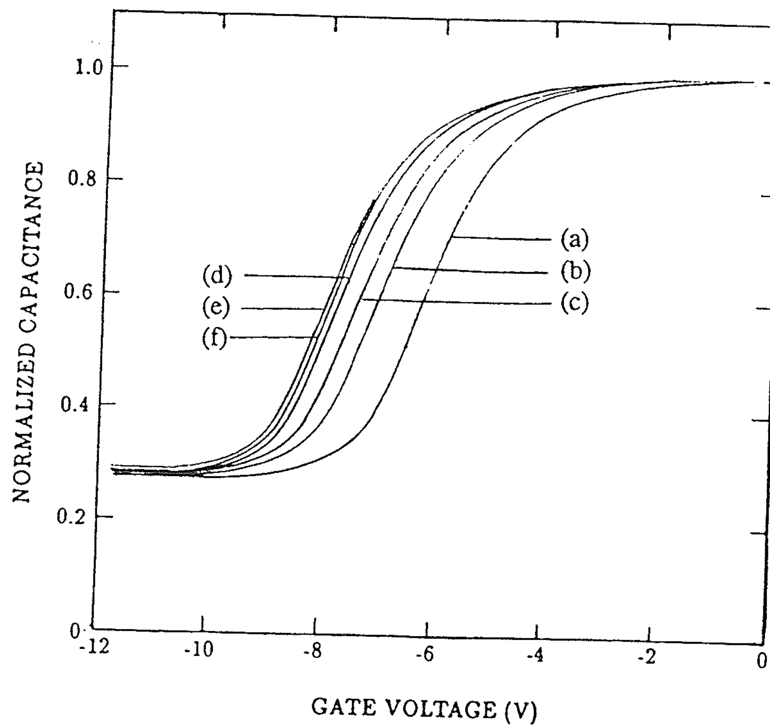

Figure 4.6 H-F C-V curves after negative bias stressing (-3 MV/cm) at room temperature for (a)0 min (b)0.5 min (c)3.5 min (d)13 min (e)3 min and (f)2 min on the sample deposited at 225°C before PMA.

4.5 Conclusions

NBTI was displayed even at room temperature in MOS capacitors fabricated by PECVD SiO_2 films. No measurable NBTI was found at room temperature when the samples underwent a standard postmetallization anneal. At high temperature NBTI was dramatic even after postmetallization anneal. High temperature NBTI was also sensitive to the cleanliness of the sample surface. High temperature NBTI was reduced after surface cleaning.

The positive charge generated at room temperature in PECVD SiO_2 film was due to filling of intrinsic hole traps preexistent in the oxide. At high temperature new trap sites were created in PECVD SiO_2 film under negative bias stressing. An increase in interface traps due to NBTI was also observbed.

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CHAPTER 5

CONCLUSIONS

The present investigation of thin SiO_2 films prepared by plasma-enhanced chemical vapor deposition (PECVD) techniques has revealed that, as a low-temperature process ($\leq 350^o C$), PECVD is a most promising technique to replace high-temperature furnace process ($\geq 900^o C$) for the growth of high quality SiO_2 film on silicon substrate in VLSI technology where low processing temperature is required. The experimental results of electrical measurements show that PECVD SiO_2 films can have near thermal oxide quality in terms of mobile ionic contamination ($\sim 10^{10} cm^{-2}$), oxide fixed charge ($\sim 10^{10} cm^{-2}$), interface trap density at midgap ($\sim 10^{10} cm^{-2} eV^{-1}$) and average electric field at breakdown (~6-7 MV/cm). These figures are very respectable for the SiO_2 films deposited at such low temperatures ($\leq 350^o C$) and satisfy several of the requirements for VLSI device applications. The electron trapping study of PECVD SiO_2 shows that no significant current injection occurs when the electric field across the oxide is $\leq$ 6 MV/cm and the density of electron traps in the bulk of PECVD SiO_2 is on the same order as that in thermal oxide ($\sim 10^{12} cm^{-2}$). The results also show that large negative bias-temperature instability (NBTI) in PECVD SiO_2 can be easily removed by a standard postmetallization anneal (PMA) or reduced by surface cleaning (same effect should be also achieved by avoiding making the sample surface dirty).

Work remains to be done to improve trapping properties in PECVD SiO_2 film by reducing electrically active defects. Further study is also needed to clarify the mechanism for the generation

of positive charge under negative bias stressing and simultaneous creation of interface traps during stressing.