THE UNIVERSITY OF MANITOBA

AN EVALUATION OF CONTROL SCHEMES FOR A HVDC SYSTEM FEEDING INTO A WEAK AC SYSTEM

BY
PREM KUMAR KALRA

A Thesis
Submitted to the Faculty of Graduate Studies
in Partial Fulfillment of the Requirements for the Degree
of Doctor of Philosophy

DEPARTMENT OF ELECTRICAL ENGINEERING

WINNIPEG, MANITOBA R3T 2N2
CANADA

June 1987

ISBN 0-315-37145-5

AN EVALUATION OF CONTROL SCHEMES FOR A HVDC SYSTEM FEEDING INTO A WEAK AC SYSTEM

BY

PREM KUMAR KALRA

A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

DOCTOR OF PHILOSOPHY

AN EVALUATION OF CONTROL SCHEMES FOR A HVDC SYSTEM FEEDING INTO A WEAK AC SYSTEM

BY

PREM KUMAR KALRA

A dissertation submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

DOCTOR OF PHILOSOPHY

To the late Mr. Parmanand Kalra (Father), the late

Mr. Bhagat Das (Professor) and the late

Mr. Shayamlal Sharma (Bank Manager)

ABSTRACT

This thesis is a prelude to the development of a knowledge based system (KBS) for controlling a hvdc system feeding into a weak ac system. Knowledge is generated by evaluating various control schemes and controller configurations. The evaluation of various control schemes and controller configurations is carried out by investigating the system stability and the system recovery from various faults.

The steady-state stability is determined at the inverter feeding to the weak ac system by using the root locus technique for various control schemes. It is observed that system stability may be improved by reducing controller gain, by reducing the sending ac system short circuit ratio, or by increasing the receiving ac system short circuit ratio. It is also observed that all control schemes may have the same stability margin and settling time provided an appropriate controller gain is used. Similar results are obtained for the detailed hvdc system.

The system recovery from various faults is investigated by evaluating individual control schemes at the inverter terminal. This study is performed on a real time, physical model simulator. The digital simulation is carried out using the EMTDC package for a detailed hvdc system feeding to the ac system with a 1.5 short circuit ratio. The transient performance of each control mode is examined by substituting the various control modes for a few cycles just after the fault and thereafter reverting the system operation to the extinction angle control to have minimum reactive power requirements during steady-state. It is found, through digital simulation, that the dc power recovery time for all control schemes may be the same with proper optimization of controller parameters. Further, it is determined that switching among the control schemes does not lead to instability. However, the dynamic overvoltage profile can be improved by using the dc or ac voltage control during transients.

Investigations show that the I-P controller has little value for hvdc systems because of the limitation on the choice of gain. Further, the modified I-P control is suggested to replace the P-I controller. The modified I-P controller improves the system stability but it worsens the system recovery from various faults in comparison to the P-I controller.

New state identification techniques are proposed to discriminate and identify various faults. It is shown that the right decision for identifying various faults may allow room for the KBS to change controller parameters, control schemes and controller configurations.

In addition, a technique is suggested to linearize non-linear equations involved in hvdc control systems over a wide range of system operation with ±5% error. The linearized expressions are used to investigate the system stability. It is observed that the system is less stable than what is predicted by small signal analysis.

ACKNOWLEDGEMENTS

The author expresses deep gratitude to Professors R. M. Mathur, G. W. Swift, M. M. Rashwan, D. A. Young and R. W. Menzies for serving on his Advisory Committee. Special acknowledgement goes to Professors Neil Popplewell and D. Trim from the Mechanical Engineering Department and Department of Applied Mathematics, respectively, for their valuable guidance and assistance in some parts of the research. A very special word of thanks is reserved for Dr. R. M. Mathur, Committee Chairman, for his contagious enthusiasm as a scholar and educator. Special appreciation and thanks are due Professor Menzies for his timely help with organizing the thesis.

The author also wishes to thank Vice President N. G. Hingorani of EPRI for his understanding and encouragement. Special appreciation is due to Mrs. Wanda Myers for her untiring effort in expertly typing the manuscript.

Thanks are also due to the Manitoba Hydro Electric Board and the Natural Sciences and Engineering Research Council of Canada for financial support for carrying out the research. Special thanks is due to Mr. Amit Chawla for help in organizing the thesis.

Finally, the author expresses sincere appreciation to his grandfather, mother, brothers, sister and friends for their patience, interest, encouragement and love. Very special thanks to the author's father for his special interest and encouragement to the author for higher studies.

TABLE OF CONTENTS

		Page
ABSTRACT		iii
ACKNOWLEDGEMENTS		iv
TABLE OF CONTENTS		v
LIST OF FIGURES		ix
LIST OF TABLES		xvii
LIST OF MOST-USED SYMBOLS		xx
Chapter		
I	INTRODUCTION	1
	1.1 Brief Review of HVDC Transmission Control Schemes	1
	1.2 Problem Statement	10
	1.3 Scope of the Thesis	12
	1.4 Test System	12
II	THEORETICAL INVESTIGATION OF THE STABILITY - SMALL DISTURBANCES	15
	2.1 Introduction	15
	2.2 System Model and Equations	16
	2.3 Development of Block Diagram and Characteristic Equation	22
	2.4 Results and Discussion	29
	2.5 Conclusions	36

Chapter		Page
III	AN APPROACH FOR HANDLING NON-LINEARITIES OF HVDC SYSTEMS FOR SYSTEM STABILITY ANALYSIS	37
	3.1 Introduction	37
	3.2 Converter Modelling	38
	3.3 Linearization of Real and Reactive Power Functions	42
	3.4 Basic Equations for Large Disturbance Stability Studies	45
	3.5 Block Diagram for Different Controls at the Inverter Terminal	48
	3.6 Results	55
	3.7 Discussion	57
	3.8 Conclusions	59
IV	EXPERIMENTAL STUDY OF HVDC CONTROLS AT THE INVERTER TERMINAL.	60
	4.1 Introduction	60
	4.2 Test System	61
	4.3 Faults for System Test	64
	4.4 Measure of Effectiveness of Various Controls	65
	4.5 Implementation of Various Control Modes	66
	4.6 System Response for Various Control Modes	68
	4.7 Discussion	79
V	DIGITAL SIMULATION STUDIES	80
	5.1 Introduction	80
	5.2 Modelling of AC-DC-AC System	81
	5.3 DC System Controls	86
	5.4 Interfacing of Various Control Modes with EMTDC . .	90

Chapter Page

5.5 Measures for Determining the Effectiveness of Various Control Schemes 93

5.6 Controller Design for Various Schemes 93

5.7 System Recovery for Some Faults with Various Control Schemes at the Inverter Terminal 95

5.8 Discussion 104

5.6 Conclusions 105

VI INFLUENCE OF THE SENDING END SHORT CIRCUIT RATIO ON THE PERFORMANCE OF HVDC CONTROLS 106

6.1 Introduction 106

6.2 Direct Current Step Response of HVDC System 107

6.3 System Recovery from Various Faults 111

6.4 Discussion 115

6.5 Conclusions 118

VII APPLICATION OF RECENT CONTROLLER CONFIGURATIONS TO A HVDC SYSTEM 119

7.1 Introduction 119

7.2 Direct Current Step Response for a Detailed Model of the HVDC System for I-P and P-I Controllers . . . 122

7.3 Modified I-P Controller 126

7.4 Direct Current Step Response for a Detailed Model of the HVDC System for Modified I-P and P-I Controllers 126

7.5 Influence of Controller Configuration on the System Starting and the System Recovery from Faults 130

7.6 Discussion 138

7.7 Conclusions 138

Chapter		Page
VIII	STATE IDENTIFICATION FOR HVDC SYSTEMS: SOME NEW PARAMETERS FOR SIGNAL PROCESSING	140
	8.1 Introduction	140
	8.2 Description of Various Discriminants	141
	8.3 Application of Various Discriminants for Fault Identification	142
	8.4 Log Transformation	144
	8.5 Results	145
	8.6 Decision Procedure	149
	8.7 Discussion	152
	8.8 Conclusions	154
IX	CONCLUSIONS	155
	APPENDIX A1	159
	APPENDIX A2	161
	APPENDIX A3	167
	APPENDIX B1	173
	APPENDIX B2	175
	APPENDIX B3	177
	APPENDIX C	186
	APPENDIX D1	192
	APPENDIX D2	196
	APPENDIX D3	200
	APPENDIX E	204
	BIBLIOGRAPHY	211

LIST OF FIGURES

Figure		Page
1.1	Control Hierarchy for a HVDC System	2
1.2	Steady-State Characteristics for Different Control Modes	4
1.3	Three Point Instability Due to the Extinction Angle Control	4
1.4	Modified Characteristics for the Inverter Control	6
1.5	Proposed System for Investigations	14
2.1	Model System Used for the Stability Analysis	17
2.2	Phasor Diagrams for the Sending AC System	17
2.3	Block Diagram for Stability Analysis of Various Control Schemes	23
2.4	Influence of Controller Gain of Various Control Schemes at the Inverter on the Dominant Roots	32
2.5	Influence of the Receiving AC System Short Circuit Ratio on the Dominant Roots	32
2.6	Influence of the Sending AC System Short Circuit Ratio on the Dominant Roots	34
3.1	Converter Model	39
3.2	Error in Linearizing 'cos α'	43
3.3	Modified Converter Model	43
3.4(a)	Error Due to Linearization of Active Power Expression . .	46
3.4(b)	Error Due to Linearization of Reactive Power Expression .	46
3.5	System Used for Determining Stability Boundaries	47

Figure		Page
3.6	Block Diagram for Determining System Stability	49
3.7	Influence of the System Gain on the Dominant Roots . . .	56
3.8	Influence of the Receiving AC System Short Circuit Ratio on the Dominant Roots	56
4.1	The System for Investigating the System Recovery from Various Faults	62
4.2	Complete Control System for the Inverter Terminal	69
4.3	Simplified Representation of Implementation of Various Control Schemes at the Inverter Terminal	70
4.4	AC Voltage Response for Three Phase to Ground Fault at the Inverter AC Bus	72
4.5	DC Power Recovery from the Three Phase to Ground Fault at the Inverter AC Bus	77
5.1	A HVDC System Used for Investigations	82
5.2	The Converter Transformer Model	84
5.3	AC Filter Representation	86
5.4	Block Diagram for the Pole Control Group	87
5.5	Block Diagram for the Valve Control Group	88
5.6	Control Characteristics of the HVDC System	89
5.7	Three Phase RMS Voltage Measurement	89
5.8	Functional Block Diagram to Realize the Various Control Schemes at the Inverter Terminal	94
5.9	Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Inverter Bus	98

Figure		Page
5.10	Three Phase RMS Voltage Response for the Three Phase to Ground Fault at the Inverter Bus	100
5.11	DC Power Recovery from the Three Phase to Ground Fault at the Inverter Bus	101
6.1	Direct Current Step Response for a Weak Receiving and Strong Sending AC System (Case (a))	110
6.2	Direct Current Step Response for a Weak Receiving and Weak Sending AC System (Case (b))	111
6.3	Direct Current Step Response for a Strong Receiving and Weak Sending AC System (Case (c))	110
6.4	Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Inverter Bus	112
6.5	Three Phase RMS Voltage Response for the Three Phase to Ground Fault at the Inverter Terminal	113
6.6	DC Power Recovery from the Three Phase to Ground Fault at the Inverter Bus	114
7.1	P-I Controller Configuration	121
7.2	I-P Controller Configuration	121
7.3	Direct Current Step Response of Detailed DC System with K_p = 0.045, and K_I = 30.0 for P-I Controller	123
7.4	Direct Current Step Response of Detailed DC System with K_p = 0.045, and K_I = 30.0 for I-P Controller	124
7.5	System Controlled by Modified I-P Controller	127

Figure		Page
7.6	Direct Current Step Response for Modified P-I Controller (K_p = 0.04, and K_I = 30.0)	129
7.7	Direct Current Step Response for Modified I-P Controller (K_p = 0.04, and K_I = 30.0)	129
7.8	DC System Starting with P-I Controller	131
7.9	DC System Starting with Modified I-P Controller	132
7.10	AC-DC-AC System Recovery from the Three Phase to Ground Fault at the Inverter AC Bus for P-I Controller	134
7.11	AC-DC-AC System Recovery from the Three Phase to Ground Fault at the Inverter AC Bus for Modified I-P Controller.	135
8.1	Frequency Spectra for Various Faults	147
8.2	Decision Tree for Identification of Various Faults . . .	153
A2.1	AC Voltage Response for Single Phase to Ground Fault at the Inverter AC Bus	161
A2.2	AC Voltage Response for the Remote Three Phase Fault on the Inverter AC System	162
A2.3	AC Voltage Response for the Remote Single Phase Fault on the Inverter AC System	163
A2.4	AC Voltage Response for the Single Phase to Ground Fault on the Rectifier System	164
A2.5	AC Voltage Response for the Three Phase to Ground Fault at the Rectifier AC Bus	165
A2.6	AC Voltage Response for the DC Fault at the Inverter Terminal	166

Figure		Page
A3.1	DC Power Recovery from the Single Phase to Ground Fault at the Inverter AC Bus	167
A3.2	DC Power Recovery from the Remote Single Phase Fault on the Inverter AC System	168
A3.3	DC Power Recovery from the Remote Three Phase Fault on the Inverter AC System	169
A3.4	DC Power Recovery from the Single Phase to Ground Fault at the Rectifier AC Bus	170
A3.5	DC Power Recovery from the Three Phase to Ground Fault at the Rectifier AC Bus	171
A3.6	DC Power Recovery from the DC Line Fault at the Inverter Terminal	172
B3.1	Instantaneous AC Voltage Response for the Single Phase to Ground Fault at the Inverter Bus	177
B3.2	Three Phase RMS Voltage Response for the Single Phase to Ground Fault at the Inverter Bus	178
B3.3	DC Power Recovery from the Single Phase to Ground Fault at the Inverter Bus	179
B3.4	Instantaneous AC Voltage Response for the DC Line Fault at the Inverter Terminal	180
B3.5	Three Phase RMS Voltage Response for the DC Line Fault at the Inverter Terminal	181
B3.6	DC Power Recovery from DC Fault at the Inverter Terminal	182

Figure		Page
B3.7	Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Rectifier Bus	183
B3.8	Three Phase RMS Voltage Response for the Three Phase Fault at the Rectifier Bus	184
B3.9	DC Power Recovery from the Three Phase To Ground Fault at the Rectifier Bus	185
C.1	Instantaneous AC Voltage Response for the Single Phase to Ground Fault at the Inverter Bus	186
C.2	Three Phase RMS Voltage Response for the Single Phase to Ground Fault at the Inverter Terminal	187
C.3	DC Power Recovery from the Single Phase to Ground Fault at the Inverter Bus	188
C.4	Instantaneous AC Voltage Response for DC Line Fault at the Inverter Terminal	189
C.5	Three Phase RMS Voltage Response for the DC Line Fault at the Inverter Terminal	190
C.6	DC Power Recovery from the DC Line Fault at the Inverter Terminal	191
D1.1	Influence of Increasing the Proportional Gain on the Direct Current Step Response for P-I Controller (K_p = 0.055, and K_I = 30.0)	192
D1.2	Influence of Increasing the Proportional Gain on the Direct Current Step Response for I-P Controller (K_p = 0.055, and K_I = 30.0)	193

Figure		Page
D1.3	Influence of Increasing Integral Gain on the Direct Current Step Response for P-I Controller (K_p = 0.055, and K_I = 40.0)	194
D1.4	Influence of Increasing Integral Gain on the Direct Current Step Response for I-P Controller (K_p = 0.055, and K_I = 40.0)	195
D2.1	Influence of Increasing Proportional Gain on the Direct Current Step Response for P-I Controller (K_p = 0.07, and K_I = 30.0)	196
D2.2	Influence of Increasing Proportional Gain on the Direct Current Step Response for I-P Controller (K_p = 0.07, and K_I = 30.0)	197
D2.3	Influence of Reducing Integral Gain on the Direct Current Step Response for P-I Controller (K_p = 0.07, and K_I = 25.0)	198
D2.4	Influence of Reducing Integral Gain on the Direct Current Step Response for I-P Controller (K_p = 0.07, and K_I = 25.0)	199
D3.1	AC-DC-AC System Recovery from the Single Phase to Ground Fault at the Inverter AC Bus for P-I Controller	200
D3.2	AC-DC-AC System Recovery from the Single Phase to Ground Fault at the Inverter AC Bus for Modified I-P Controller	201

Figure Page

D3.3 AC-DC-AC System Recovery from the DC Line Fault at the Inverter Terminal with P-I Controller 202

D3.4 AC-DC-AC System Recovery from the DC Line Fault at the Inverter Terminal with Modified I-P Controller 203

LIST OF TABLES

Table		Page
2.1	Base Case System Parameters	30
2.2	Effect of Variation of DC Line Resistance on the System Stability	35
3.1	The Expression of S_1 and S_2 for Various Control Modes . .	50
3.2(a)	Influence of Line Resistance on the System Stability for AC Voltage Control	58
3.2(b)	Influence of Line Resistance on the System Stability for Reactive Power Control	58
4.1(a)	System Response to the Three Phase to Ground Fault at the Inverter AC Bus	73
4.1(b)	System Response to the Single Phase to Ground Fault at the Inverter AC Bus	73
4.1(c)	System Response to the Remote Three Phase Fault at the Inverter AC Bus	73
4.1(d)	System Response to the Remote Single Phase Fault at the Inverter AC Bus	74
4.1(e)	System Response to the Single Phase to Ground Fault at the Rectifier AC Bus	74
4.1(f)	System Response to the Three Phase to Ground Fault at the Rectifier AC Bus	75
4.1(g)	System Response to the DC Line Fault at the Inverter Terminal	75

Table		Page
5.1(a)	System Response for the Three Phase to Ground Fault at the Inverter AC Bus	102
5.1(b)	System Response for the Single Phase to Ground Fault at the Inverter AC Bus	102
5.1(c)	System Response for the DC Line Fault at the Inverter Terminal	103
5.1(d)	System Response for the Three Phase to Ground Fault at the Rectifier AC Bus	103
6.1	System Response for the Three Phase to Ground Fault at the Inverter AC Bus	116
6.2	System Response for the Single Phase to Ground Fault at the Inverter AC Bus	116
6.3	System Response for the DC Line Fault at the Inverter Terminal	117
7.1	System Response for the Three Phase to Ground Fault at the Inverter AC Bus	136
7.2	System Response for the Single Phase to Ground Fault at the Inverter AC Bus	136
7.3	System Response for the DC Line Fault at the Inverter Terminal	137
8.1	Discriminants Value for Various Faults	148
8.2	Discriminants Value for Various Faults	150
8.3	Discriminants Value for Various Faults with Log-Transformation	150

Table		Page
8.4	Discriminants Value for Various Faults (Frequency Domain Analysis)	151
A1.1(a)	Parameters for the Receiving AC System	159
A1.1(b)	Parameters for the Sending AC System	159
A1.1(c)	AC Filter Data	160
A1.1(d)	Parameters for the Controller on the Rectifier Terminal .	160
B1.1(a)	Data for the Receiving AC System	173
B1.1(b)	Data for the Sending AC System	173
B1.2	DC Filters at the Inverter and Rectifier Terminals . . .	173
B1.3(a)	AC Filters Components at the Inverter Bus	174
B1.3(b)	AC Filters Components at the Rectifier Bus	174
B2.1	Controller Settings for Three Phase to Ground Fault at the Inverter Bus	175
B2.2	Controller Settings for Single Phase to Ground Fault at the Inverter Bus	175
B2.3	Controller Settings for DC Line Fault	176
B2.4	Controller Settings for Three Phase to Ground Fault at the Rectifier Bus	176
E.1	Discriminants Values for Various Faults	204
E.2	Discriminants Values for Various Faults for Different Sampling Rates with Log-Transformation	206
E.3	Discriminants Values for Various Faults (Frequency Domain Analysis)	209

LIST OF MOST-USED SYMBOLS

I_1	Magnitude of fundamental component of line current
I_d or I_{DC}	Direct current
i_a, i_b, i_c	Instantaneous three phase current
I_q	Reactive current
I_s	Integral square error
K	Kurtosis
K_I	Integral gain of a controller
K_p	Proportional gain of a controller
L_d	Smoothing reactor inductance
L_1 or L_s	AC system inductance
m	Number of bridges connected in series
n	Transformation ratio (secondary to primary)
P_L	Power supplied to load
P_d or P_{DC}	DC power
Q_L	Reactive power absorbed by load
Q_d	Reactive power absorbed by dc system
r_L	Load resistance
R_d	Smoothing reactor resistance
R_1 & R_2	AC system resistance
R_s or r_s	AC system equivalent resistance
S	Laplace Operator
S_k	Skewness
t_f	Fault duration
t_p	Peak instantaneous overvoltage duration

t_D	Dynamic overvoltage duration
t_r	DC power recovery time
t_i	Instant at which system operation reverts to the extinction angle control
t_s	Instant at which step change is made in the reference signal of direct current control system
t_{st}	Starting time for the system
V or V_R	RMS value of three phase ac voltage
v_a, v_b, v_c	Instantaneous three phase ac voltage
V_n	Normal steady-state instantaneous voltage
V_d or V_{DC}	Direct voltage
V_D	Peak of dynamic overvoltages
V_p	Highest peak of instantaneous overvoltages
x_c or X_c	Commutating reactance
X_s or x_s	AC system equivalent reactance
x'	Transient reactance of the machine
Y_c	Admittance
Z_s	AC system equivalent impedance
α	Firing angle
γ	Extinction angle
γ_{min}	Minimum extinction angle
β	Ignition angle
ϕ	Power factor angle
α_I	Firing angle for the inverter bridge
α_I'	Equivalent voltage of firing angle of inverter bridge

α_{min}	Minimum firing angle
αr	Firing angle for the rectifier bridge
α_r'	Equivalent voltage of firing angle of rectifier bridge
τ_c	Time constant of controller
μ	Mean
σ	Variance

CHAPTER I

INTRODUCTION

It is well known that hvdc schemes have distinct advantages over hvac schemes. One of the major advantages of the hvdc scheme is its fast controllability. The major part of this thesis is devoted to the evaluation of the performance of various control modes at the inverter terminal for a hvdc system feeding to an ac system having relatively high impedance.

The evaluation of various control modes is carried out for determining their effectiveness in terms of dc power recovery time, duration and magnitude of overvoltages. As well, the influence of the sending and the receiving ac system impedance on the system stability is studied. This is done in order to determine the effectiveness of various control modes for different operating conditions.

1.1 BRIEF REVIEW OF HVDC TRANSMISSION CONTROL SCHEMES.

Normally, in hvdc schemes, the complete control system is realized at three levels, i.e., master control, pole control, valve control. The details of each level of control are described in references [1-7]. The typical arrangement of these three levels of control is shown in Figure 1.1 [6]. The master controller generates the current order for the pole control system. It also provides the interface between the ac and dc system controls. The pole control system provides current margin, current limits, tap changer control and signals needed

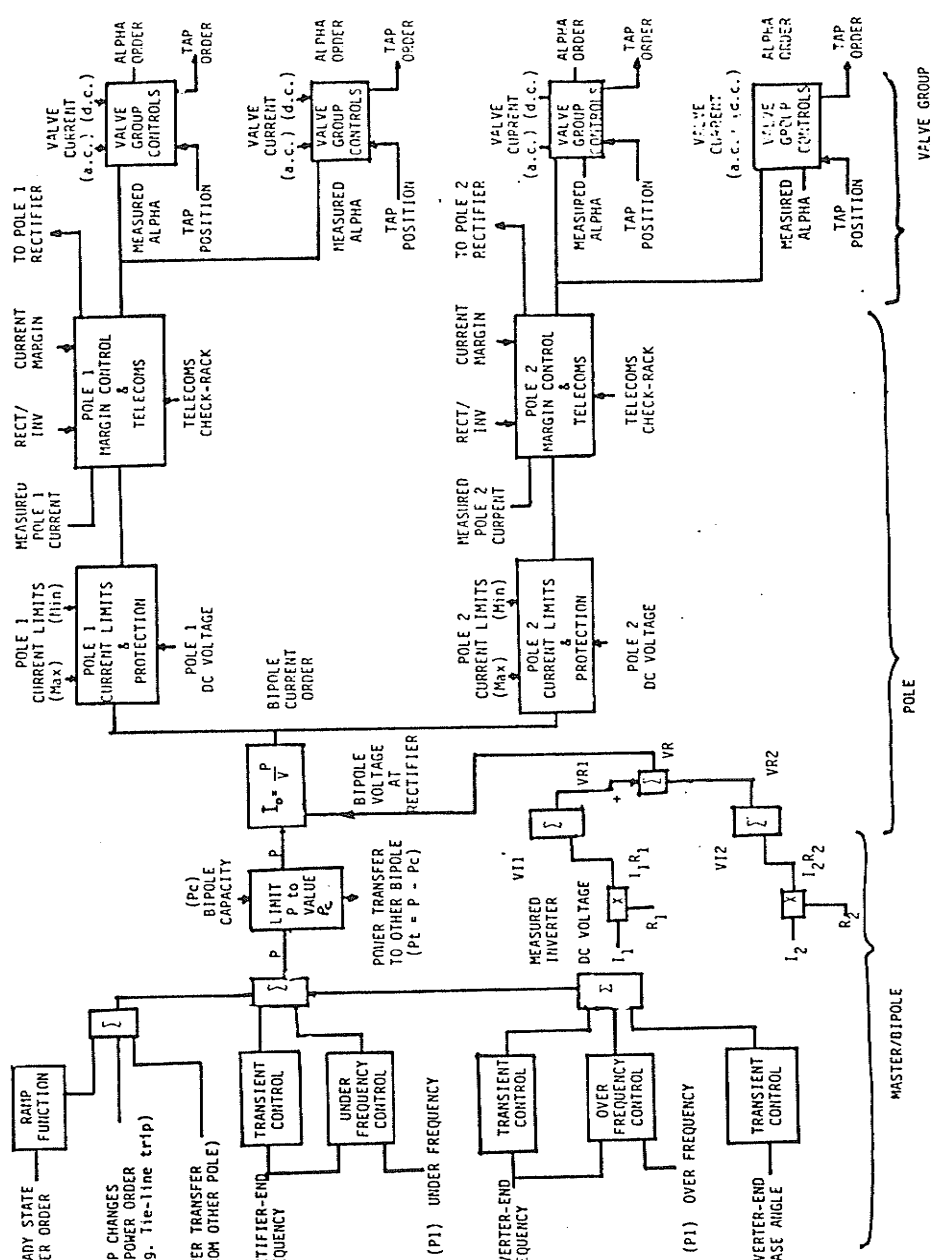


Figure 1.1 Control Hierarchy for a HVDC System

for the valve control. The valve control generates the firing angle to obtain the desired level of voltage and current in the system.

Rectifier Pole Control

The pole controller at the rectifier has two control modes, i.e., minimum firing angle control and constant current control (Figure 1.2).

Minimum Firing Angle Control: The minimum firing angle, α, is selected on the basis of minimum reactive power demand and sufficient positive voltage across non-conducting valve to ensure successful commutation. A typical value of α_{min} is 5° [6]. This control mode operates for low voltage levels on the rectifier terminal.

Current Control: The rectifier generally operates in this control mode during steady-state operation of a hvdc system. The current is kept constant in the dc system by making appropriate changes in the firing angle for changes in the system voltage.

Inverter Pole Control

The inverter may operate in one of the following control modes (Figure 1.2).

i) Extinction angle control [7]
ii) Current control [7]
iii) AC voltage control [8]
iv) Reactive current control [9-10]
v) Power factor control [11]
vi) DC voltage control
vii) Reactive power control
viii) Active power control

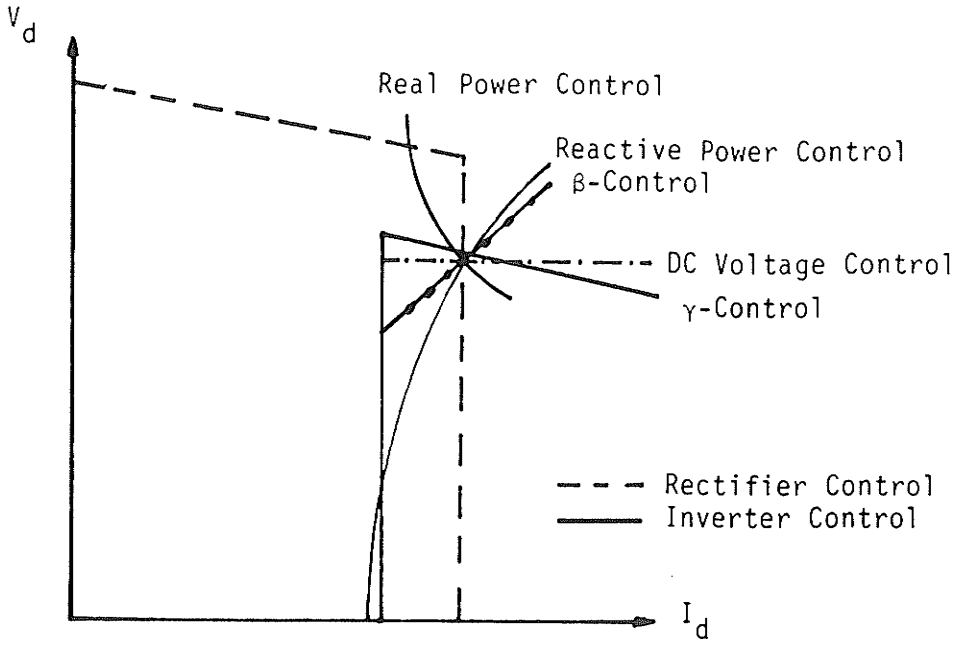


Figure 1.2 Steady-State Characteristics for Different Control Modes

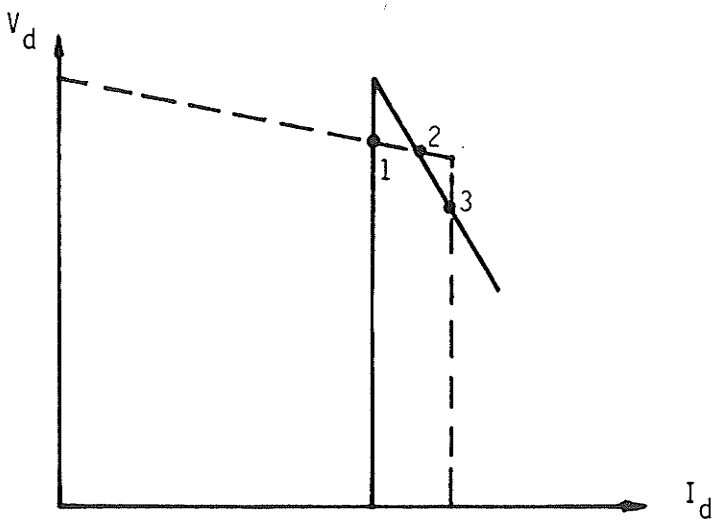


Figure 1.3 Three Point Instability Due to the Extinction Angle Control

Most hvdc schemes provide extinction angle and current control at the inverters. In order to cope with the special problems created by the connection of hvdc links to weak ac systems, other control modes (iii to viii) have been proposed in the recent literature [8-11].

Extinction Angle Control

There are two basic methods for this control to be realized, namely, predictive control and closed loop control [12]. The inverter normally operates with the control during steady-state. The advantage of using this control is essentially a minimum reactive power requirement and generation of minimal harmonics. The typical value of the extinction angle (γ) is 18° [6]. The major demerits associated with this control are:

i) The extinction angle control is usually prone to commutation failures. As the inverter side voltage drops, the extinction angle is reduced to normalize the voltage. This reduction in the extinction angle may reduce its value below the minimum extinction angle (18°), thereby causing a commutation failure.

ii) This control presents the negative resistance to the dc line as shown in Figure 1.2. The negative slope of V_d-I_d characteristics becomes steeper as the ac system impedance increases. Thus, it causes voltage/power instability [10].

iii) The extinction angle control can lead to a three point instability as shown in Figure 1.3. Most γ_{min} controllers are modified to prevent such instability. It is accomplished by modifying the slope of the γ_{min} characteristics in the current margin region as shown in Figure 1.4.

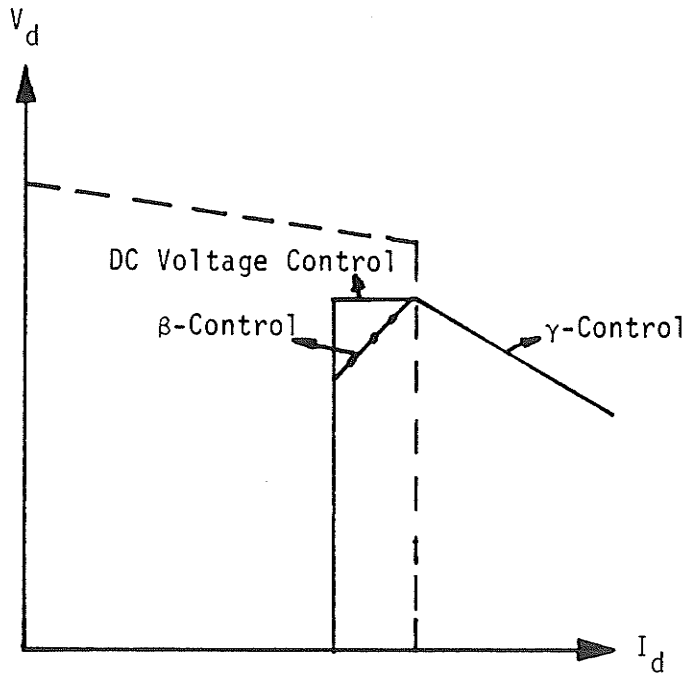


Figure 1.4 Modified Characteristics for the Inverter Control

Current Control

During disturbances such as dc line fault, starting of the system, and power reversals, the inverter operates on the current control. It has been demonstrated [13] that this control works efficiently in the power reversal mode. The probability of commutation failure is minimized in this control mode because the extinction angle is always greater than the minimum. Normally, the inverter is provided with a current margin of 10%-15% to allow the current controller to be operated at both the rectifier and the inverter ends independently [7].

AC Voltage Control

The fundamental component of the ac current at a hvdc terminal lags the commutating voltage. Consequently, the dc terminals absorb reactive power. If the host ac system has a relatively high source impedance, it becomes increasingly difficult to maintain the required voltage level at the ac bus. To overcome this problem of a load-dependent ac voltage fluctuation, compensating equipment is used at the ac bus. Alternatively, the inverter terminal can be controlled in such a manner that it strives to keep the ac bus voltage constant [14]. It has been suggested [8] that ac voltage control must operate only when the ac voltage level exceeds a pre-set value. The reason for implementing the overvoltage constraint is that in an overvoltage condition γ is increased, which leads to higher reactive power absorption (a corrective step). If a constant ac voltage is administered during undervoltage, the controller attempts to reduce γ which, if it falls below γ_{min}, will lead to commutation failure.

The ac voltage control offers advantages such as low losses and a low probability of commutation failure. However, it has the disadvantage of higher valve stresses due to its operation at the higher extinction angle.

Reactive Current Control

The firing angle of the inverter is regulated in a manner that the reactive current absorbed by the inverter remains constant [9]. This control scheme has two main advantages. First, there is a reduced probability of commutation failure because the inverter operates at a higher extinction angle. Second, it leads to a reduction in station cost by decreasing the size of VAR compensating equipment. However, this scheme operates at an extinction angle larger than γ_{min}. Hence, there is a larger reactive power demand during the steady-state operation.

Power Factor Control

To maintain the constant power factor at the inverter terminal, the dc voltage at the inverter terminal is controlled by controlling the firing angle, while ac voltage variations are compensated by a tap changer [11]. This control scheme operates on a high extinction angle during partial load conditions. Furthermore, at full load, its operating characteristics are exactly the same as the extinction angle control. This control scheme has a serious drawback, that is, the time needed to change the transformer tap during and soon after a disturbance is 1 to 2 s. This makes the control either respond slowly or to operate as a dc voltage control. Hence, it is a pseudo-power factor control.

A pure power factor controller has been developed [15] which is described later in the thesis. This control does not need a tap changer control. The power factor control offers the following advantages:

i) The extinction angle is increased as the direct current reduces and, hence, the probability of commutation failure is reduced.

ii) As the power factor remains constant, the real power transferred and the reactive power consumed are directly proportional to the direct current. Hence, the possibility of high reactive power consumption can be minimized.

DC Voltage Control

This control is designed by either controlling the mid-point dc line voltage [13] or by controlling the inverter terminal dc voltage [16]. This control has an advantage of minimizing the line losses (I^2R) and utilizing the insulation most effectively for the given power. It is also possible to maintain the extinction angle close to its minimum value with the help of the tap changer. However, this control responds slowly because of the slow tap changer movement which normally takes 1.00 to 2.0 s [6]. However, the dc voltage control discussed later in the thesis does not need the tap changer control.

Reactive Power Control

So far, the reactive power is used as a modulating signal for pole control to produce secondary signals, such as dc voltage at the inverter [17-18]. This control apparently has an advantage over the reactive current control because of its additional capability to suppress the variation in the ac bus voltage.

Active Power Control

This control shows two operating points in the steady-state as shown in Figure 1.2. Hence it causes two point instability. This control mode is not discussed any further for this reason.

1.2 PROBLEM STATEMENT

In the foregoing section, advantages and disadvantages of each control mode are briefly outlined. There is, however, a need to evaluate the effectiveness of each control scheme in comparison to others in greater detail. In the literature where new control modes have been proposed, the authors have, at most, compared their proposed control mode with one or two other modes. There is no consistency between the test systems used in separate papers. It is important, therefore, that a systematic comparative evaluation of all control modes be carried out, so as to develop a dependable guideline for the designers and users of hvdc systems feeding into weak ac systems. Also, it is believed that this study would produce a knowledge base for the future application of adaptive and knowledge based controllers.

The ultimate objective of this investigation is to lead towards the development of a knowledge based controller which would operate a dc inverter connected to a very weak ac system in a stable manner. At present, inverters operate principally with extinction angle and current controllers with numerous secondary modifications.

The controller switches from one control mode to the other by using a simple selection circuit which chooses the minimum of the two firing angles produced by the two control modes. For a more sophisticated

controller, if determined to be advantageous, initially several control modes can be programmed on a processor (or several processors). The selection of the output from the controller can be made dependent upon inference from several features such as system parameters and system state (disturbance). Additionally, the structure of each control mode can be altered to arrive at the optimal performance for a given set of system conditions. Finally, an off line learning loop can be incorporated in the controller to make it self tuning.

In an attempt to ultimately accomplish this larger objective, the investigation is subdivided into parts consistent with the requirements for a Ph.D. thesis.

For this thesis it was important to evaluate the effectiveness of various modes and study their sensitivity to system parameters. The comparison of various controller configurations has also been done. As well, system identification techniques have been investigated to discriminate and identify system faults.

In order to carry out a systematic comparative evaluation of various control modes at the inverter terminal of a hvdc system, the following tasks are set forth:

(a) Evaluation of steady-state stability of various control modes.

(b) Evaluation of the influence of system parameters on the performance of the control modes.

(c) Evaluation of the dc power recovery time, duration and magnitude of dynamic overvoltages, when system is subjected to various faults.

(d) Evaluation of the influence of the sending end ac system impedance on the system recovery and stability.

(e) Evaluation of the influence of various controller configurations on the system stability and recovery.

1.3 SCOPE OF THE THESIS

The first two tasks, (a) and (b), are achieved by carrying out a steady-state stability analysis using the root locus technique [Chapter II]. During the course of the investigation, a new approach for handling the non-linearities of the hvdc system has been developed [Chapter III]. A stability analysis is carried out using this approach. The results are compared with those from a conventional small signal analysis. Objective (c) is met by implanting various control modes on the real time physical component simulator [Chapter IV] and simulating a hvdc system on a digital computer using EMTDC (Electro-Magnetic Transient DC program) software package [Chapter V]. Objectives (d) and (e) are achieved by investigating the step response of the detailed system and the recovery of the system from some faults [Chapters VI and VII].

As a prelude to developing a knowledge based controller (where, depending upon the state of the system, the most appropriate control mode can be applied with optimized structure), it is necessary to develop real time, on line, system state identification techniques. Techniques have been developed which may discriminate and identify the type of system faults at high speed [Chapter VIII].

1.4 TEST SYSTEM

To test the effectiveness of various control modes, a simple test system is selected. It is characterized by a SCR of 4.0 at the sending

end and SCR of 1.5 at the receiving end of a dc system. The dc line is represented by a distributed model. Figure 1.5 shows the test system details.

It should be observed that the SCR at the inverter side is purposely chosen to be 1.5. At this time, this value may be regarded to be least acceptable because it results in a most difficult to operate system. The low SCR of 1.5 leads to unusual voltage fluctuations on the ac side due to load changes and system disturbances. Also, because of the high impedance of the receiving ac system, the inverter is prone to commutation failures. Dynamic overvoltages and slow system recovery are other characteristics of such a system. On the basis of the aforementioned problems, the selected system turns out to be most suitable for testing the effectiveness of conventional and newly proposed control modes. Systems of this kind can be made acceptable when furnished with dependable and effective controls.

Variations are made in the system parameters for some investigations. These are described in detail at appropriate places.

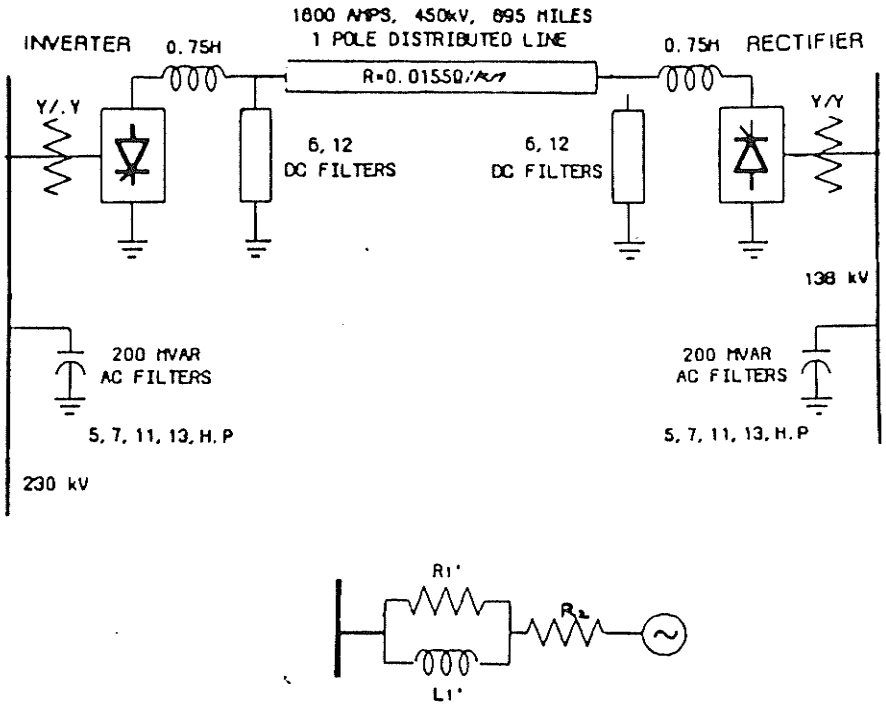


Figure 1.5 Proposed System for Investigations

CHAPTER II

THEORETICAL INVESTIGATION OF THE STABILITY - SMALL DISTURBANCES

2.1 INTRODUCTION

The steady-state stability of a hvdc system is investigated to determine the stability boundaries of various inverter control schemes. Further, the influence of the system and controller parameters on the stability boundaries of various control schemes at the inverter terminal is investigated. This study provides the information and knowledge about the trends of sensitivity of the system stability to controller gains and time constants, and system parameters. This study is also useful in determining the control system response in terms of system damping and settling time and providing information about controller design for various operating ranges. The controller settings obtained from the steady-state stability analysis are normally used as an initial guess for optimizing the controller parameters for system recovery from various disturbances [19-20].

A simplified model of a hvdc system was presented to design the current controller [19]. To modify the current controller, the influence of the lead-lag compensator was studied for the similar simplified hvdc system model [20]. These studies were based on the assumption that the inverter bus voltage does not change significantly. However, this assumption is not valid if the inverter is feeding to an ac system with relatively high impedance. Hence, this assumption was

dropped in the study reported in references [21-24]. These studies have not included details of the compensator and integral control. Hence, the results obtained in references [21-24] are not of very practical significance. Furthermore, the scope of these studies is limited only to the extinction angle control on the inverter terminal.

The technique presented in this chapter overcomes the above-mentioned drawbacks. In addition, the following control modes at the inverter terminal are also incorporated.

(a) Extinction angle control,

(b) Power factor control,

(c) DC voltage control,

(e) Reactive current control, and

(f) Reactive power control.

2.2 SYSTEM MODEL AND EQUATIONS

The following assumptions are made to determine the steady-state stability boundaries. The system considered for the study is shown in Figure 2.1.

i) The ac system of the rectifier is supplied by an infinite source. That is, the capacity of the system is much larger than that of the hvdc transmission. Hence, the voltage on the sending end ac bus can be considered to be constant.

ii) The receiving end ac system is represented by an equivalent machine. This equivalent machine is represented by a voltage source behind the machine transient impedance.

iii) The time constants of the excitation system of the receiving end equivalent machine are assumed to be much larger than those of the

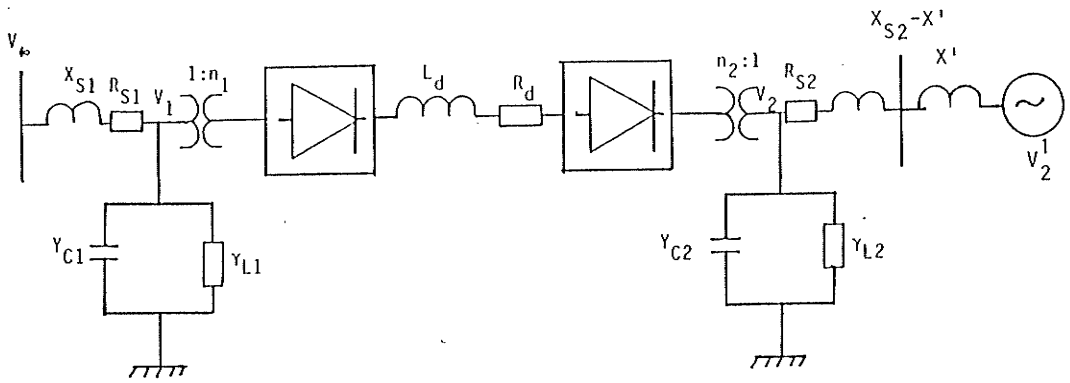


Figure 2.1 Model System Used for the Stability Analysis

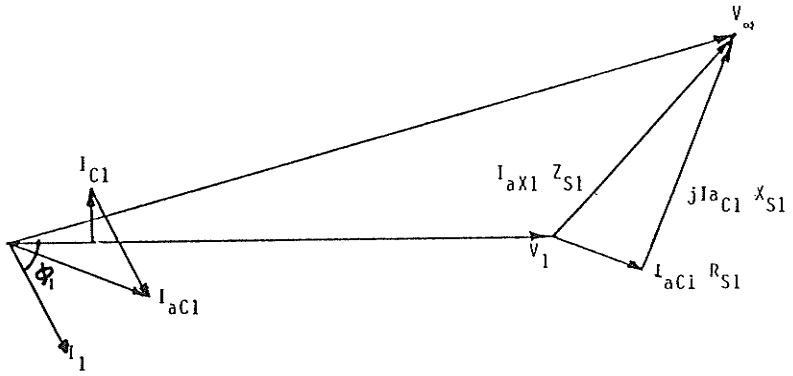


Figure 2.2 Phasor Diagram for the Sending AC System

dc system. Hence, the dynamics of the excitation system are ignored.

iv) The ac voltage is balanced and contains no harmonics. This implies that the filters absorb all harmonics generated by the dc system.

v) The impedance of the receiving ac system, including the machine transient reactance, is represented by an equivalent series connection of lumped resistance and reactance (R_{S2}, X_{S2}).

vi) Single capacitor (C_2) represents the capacitance of the ac system and the compensating equipment. The reactive power of loads can be considered as a reduction in the value of this capacitor.

vii) The total L_d and R_d represent inductance and resistance, respectively, of the dc line and the smoothing reactors on both sides.

The system shown in Figure 2.1 is used for investigating the steady-state stability of various control schemes at the inverter terminal. The phasor diagram at the rectifier end is shown in Figure 2.2. From the phasor diagram, the following set of equations are obtained.

$$V_{1\infty}^2 = (V_1 + \Delta V_1)^2 + (dV_1)^2$$

$$= \left(V_1 + \frac{(P_1 + P_{L1})\, R_{S1} + (Q_1 + Q_{L1})\, X_{S1}}{V_1}\right)^2$$

$$+ \left(\frac{(P_1 + P_{L1})\, X_{S1} - (Q_1 + Q_{L1})\, R_{S1}}{V_1}\right)^2 \qquad (2.1)$$

where

$V_{1\infty}$ = rms value of the generating station bus voltage

V_1 = rms value of the rectifier bus voltage

$P_1 = V_1 I_1 \cos\phi_1$

$P_{L1} = V_1^2 / r_{L1}$

$Q_1 = V_1 I_1 \sin\phi_1$

$Q_{L1} = -\omega C_1 V_1^2 = -Y_{C1} V_1^2$

I_1 = $\sqrt{3}x$ fundamental current component of the ac side current

$\cos\phi_1$ = power factor at the rectifier terminal

R_{S1} = equivalent resistance of the rectifier ac system

X_{S1} = equivalent reactance of the rectifier ac system

Equation (2.1) is further simplified to the following relationship by substituting expressions of the active and reactive power.

$$V_{1\infty}^2 = F_1 V_1^2 + 2V_1 I_1 (C_1' \cos\phi_1 + D_1 \sin\phi_1) + Z_{S1}^2 I_1^2 \qquad (2.2)$$

where

$$F_1 = \left(1 + \frac{R_{S1}}{r_{L1}} - X_{S1} Y_{C1}\right)^2 + \left(\frac{X_{S1}}{r_{L1}} + R_{S1} Y_{C1}\right)^2$$

$$Z_{S1} = \sqrt{R_{S1}^2 + X_{S1}^2}$$

$$C_1' = R_{S1} + \frac{Z_{S1}^2}{r_{L1}}$$

$$D_1 = X_{S1} - Y_{C1} Z_{S1}^2$$

During steady-state, the power factor is defined as [1]

$$\cos\phi_1 = \cos\alpha - \frac{X_{cr} I_d}{\sqrt{2} V_1 n_1} \qquad (2.3)$$

$$I_1 = \frac{3\sqrt{2}\,mn}{\pi} I_d = K_R I_d \tag{2.4}$$

where

X_{cr} = commutating reactance at the rectifier terminals

α = firing angle

n_1 = transformation ratio (secondary to primary side)

m = no. of bridges connected in series

I_d = direct current in the dc system

$$K_R = \frac{3\sqrt{2}\,mn}{\pi}$$

The linearized version of equation (2.2) is given below.

$$\Delta V_1 = - f_{dr}\,\Delta I_d - f_{\alpha r}\Delta\alpha \tag{2.5}$$

where

$$f_{dr} = \frac{f_2}{f_1}\,; \quad f_{\alpha r} = \frac{f_3}{f_1}$$

$$f_1 = F_1 V_{10} + K_R I_{do}\, C_1' \cos\alpha_o + D_1 K_R\, I_{do}\, \frac{K_R V_{10} - V_{do}\cos\alpha_o}{V_{ds}}$$

$$f_2 = K_R\, Z_s\, I_{do} + C_1'(V_{do} - R_{er} I_{do}) + D_1\left(V_{ds} + \frac{R_{er}\, I_{do}\, V_{do}}{V_{ds}}\right)$$

$$f_3 = K_R\, V_{10}\, I_{do} \sin\alpha_o \left(D_1 \frac{V_{do}}{V_{ds}} - C_1'\right)$$

$$R_{er} = \frac{3}{\pi}\, m\, X_{cr}$$

$$V_{do} = K_R V_{10} \cos\alpha_o - R_{er} I_{do}$$

$$V_{ds} = \sqrt{(K_R V_{10})^2 - V_{do}^2}$$

The subscript "o" represents the steady-state value of the variables.

Similar equations are obtained at the inverter end.

Modelling of DC Link

The following equation represents the dc link.

$$L_d \frac{d I_d}{dt} + R_d I_d = V_{dR} - V_{dI} \tag{2.6}$$

where

$$V_{dR} = K_R V_1 \cos\alpha - \frac{3}{\pi} X_{cr} I_d$$

$$V_{dI} = K_I V_2 \cos\beta + \frac{3}{\pi} X_{ci} I_d$$

The incremental equation of the dc link is written as below.

$$(T'_d S + 1) I_{do} = H_\alpha \Delta\alpha + H_\beta \Delta\beta \tag{2.7}$$

where

$$H_\alpha = \frac{-d_2}{R_d - d_1} \quad , \quad H_\beta = \frac{d_3}{R_d - d_1} \quad , \quad T'_d = \frac{L_d}{R_d - d_1}$$

$$d_1 = K_I f_{di} \cos\beta_o - K_R f_{dr} \cos\alpha - (R_{er} + R_{ei})$$

$$d_2 = K_R (f_{\alpha r} \cos\alpha_o + V_{10} \sin\alpha_o)$$

$$d_3 = K_I (f_{\alpha i} \cos\beta_o + V_{20} \sin\beta_o)$$

2.3 DEVELOPMENT OF BLOCK DIAGRAM AND CHARACTERISTIC EQUATION

Constant Extinction Angle (CEA) Control

In steady-state we have [1],

$$\cos\beta = \cos\gamma - \frac{\sqrt{2}\, X_{ci}}{V_2 n_2} I_d \tag{2.8}$$

where,

β = ignition angle

γ = extinction angle

X_{ci} = commutating reactance at the inverter bus

V_2 = the inverter bus voltage (rms)

n_2 = transformation ration

The incremental equation is obtained as follows using equation (2.8).

$$\Delta\gamma = S_2\, \Delta\beta - S_1\, \Delta I_d \tag{2.9}$$

where

$$S_1 = \frac{\sqrt{2}\, X_{cI}}{V_{20} \sin\gamma_o} \left(1 + \frac{f_{di}\, I_{do}}{V_{20}}\right)$$

$$S_2 = \frac{1}{\sin\gamma_o} \left(\sin\beta_o - \frac{\sqrt{2}\, f_{\alpha i}\, X_{ci}\, I_{do}}{V_{20}^2}\right)$$

Using equations (2.7) and (2.9), the block diagram of the complete system is obtained as shown in Figure 2.3. This block diagram is used to determine the steady-state stability of the hvdc system operating with various control schemes at the inverter terminal. The root locus technique [19] is used to determine the stability of the system as it

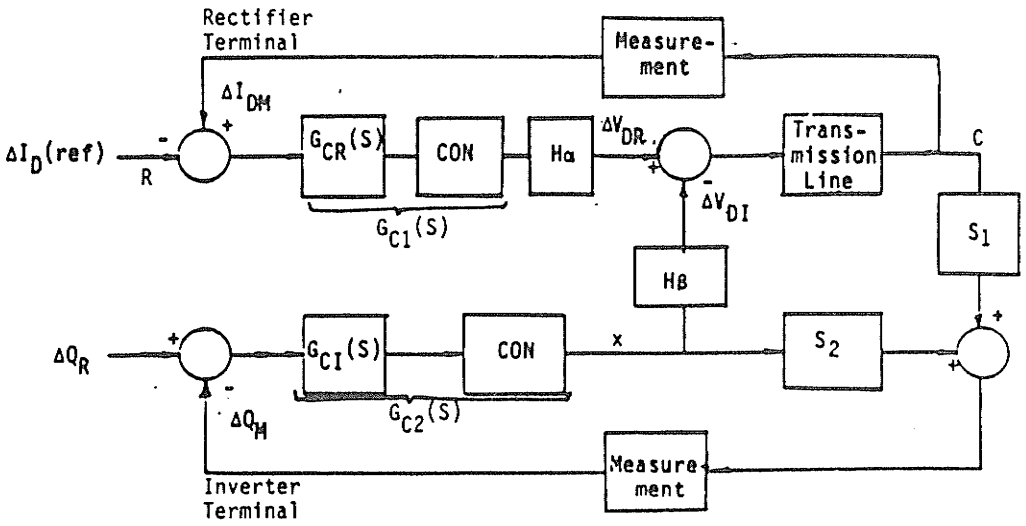


Figure 2.3 Block Diagram for Stability Analysis of Various Control Schemes

has been used successfully in the past [19-20]. To determine the locus of the most sensitive roots, the characteristic equation of the system has to be determined. The characteristic equation of the system using block diagram (Figure 2.3) is obtained in Section 2.3.2.

Characteristic Equation Derivation

The controller configuration at the rectifier and the inverter has been considered as follows.

$$G_C(S) = \left(\frac{SK_p + K_I}{S}\right)\left(\frac{1 + T_a S}{1 + T_b S}\right) \qquad (2.10a)$$

The converter is represented by the following transfer function [13].

$$T(S) = \left(\frac{1}{1 + T_{de} S}\right) \qquad (2.10b)$$

The transfer functions of measurement blocks

$$= \frac{K_o}{(1 + T_f S)} \text{ (Rectifier)}; \quad \frac{K_1}{1 + T_{f1} S} \text{ (Inverter)} \qquad (2.10c)$$

From Figure (2.3) we have

$$\left(\frac{-\, C\, Ko}{(1+T_f S)} + R\right) G_{C1}(S)\, H_\alpha + x\, H_\beta = (1 + T_d' S)\, C \qquad (2.11)$$

$$- (x\, S_2 + C S_1) \frac{K_1\, G_{C2}(S)}{(1 + T_{f1} S)} = x$$

$$- \frac{C\, S_1\, K_1\, G_{C2}(S)}{(1 + T_{f1} S) + K_1\, G_{C2}(S)\, S_2} = x \qquad (2.12)$$

where x = output of converter block at the inverter terminal.

Simplifying equation (2.11) with the help of (2.12) we get,

$$\frac{C}{R} = \frac{G_{C1}(S)\, H_\alpha\, (1 + T_f S)\, \{(1 + T_{f1} S) + K_1\, G_{C2}(S)\, S_2)\}}{(1+T'_d s)(1+T_f S)\, \{(1+T_{f1} S) + K_1\, G_{C2}(S)\, S_2\} + H_\beta\, S_1\, G_{C2}(S)\, (1+T_f S)\, K_1} \qquad (2.13)$$

$$+ K_o G_{C1}(S)\, H_\alpha\, \{(1+T_{f1} S) + K_1\, G_{C2}(S)\, S_2\}$$

Characteristic Equation Simplification

The following characteristic equation can be obtained from equation (2.13).

$$(1+T'_d S)(1+T_f S)(1+T_{f1} S) + K_1 (1+T'_d S)(1+T_f S)\, G_{C2}(S)\, S_2 + H_\beta S_1\, G_{C2}(S)(1+T_f S)$$

$$+ K_o G_{C1}\, H_\alpha\, (1+T_{f1} S) + K_1\, G_{C2}(S)\, K_o\, G_{C1}(S)\, H_\alpha S_1 \qquad (2.14)$$

The final form of the characteristic equation (C.E.) can be written as equation (2.15) by substituting for the converter model and controller as follows in equation (2.14).

$$G_{C1}(S) = \left(\frac{K_{I1} + K_{P1} S}{S}\right) \left(\frac{1 + T_{a1} S}{1 + T_{b1} S}\right) \frac{1}{(1 + T_{de1} S)}$$

$$G_{C2}(S) = \left(\frac{K_{I2} + K_{P2} S}{S}\right) \left(\frac{1 + T_{a2} S}{1 + T_{b2} S}\right) \frac{1}{(1 + T_{de2} S)}$$

C.E. =

$$(1+T'_d S)\, (1+T_f S)\, (1+T_{f1} S)\, (S)\, (1+T_{b2} S)\, (1+T_{de2} S)\, (S)\, (1+T_{b1} S)\, (1+T_{de1} S)$$

$$+ S_2\, K_1\, (1+T'_d S)\, (1+T_f S)\, (K_{I2}+K_{P2} S)\, (1+T_{a2} S)\, (S)\, (1+T_{b1} S)\, (1+T_{de1} S)$$

$$+ S_1\, H_\beta\, K_1\, (1+T_f s)\, (K_{I2}+K_{P2} S)\, (1+T_{a2} S)\, (S)\, (1+T_{b1} S)\, (1+T_{de1} S)$$

$$+ K_o\, H_\alpha\, (1+T_{f1} S)\, (K_{I1}+K_{P1} S)\, (1+T_{a1} S)\, (S)\, (1+T_{b2} S)\, (1+T_{de2} S)$$

$$+ K_o\, K_1\, H_\alpha\, S_2\, (1+T_{a1} S)\, (1+T_{a2} S)\, (K_{P1} S+K_{I1})\, (K_{P2} S+K_{I2}) \qquad (2.15)$$

The characteristic equation for various controls remains the same as equation (2.15) but the values of S_1 and S_2 change. The derivation to determine S_1 and S_2 for various control schemes is discussed below.

AC Voltage Control

The change in the ac bus voltage at the inverter terminal can be calculated in a fashion similar to that used in deriving equation (2.5), i.e.,

$$\Delta V_2 = - f_{di} \Delta I_d - f_{\beta i} \Delta\beta \tag{2.16}$$

where

$$f_{di} = \frac{f_5}{f_4}; \quad f_{\alpha i} = \frac{f_6}{f_4}$$

$$f_4 = F_2 V_{20} + C_2' K_I I_{do} \cos\beta_o + D_2 K_I I_{do} \frac{K_I V_{20} - V_{d20} \cos\beta_o}{V_{ds2}}$$

$$f_5 = K_R^2 Z_{Ss}^2 I_{do} + C_2'(V_{d20} - R_{ei} I_{do}) + D_2(V_{ds2} - \frac{R_{ei} V_{d20}}{V_{ds2}})$$

$$f_6 = K_I V_{20} I_{do} \sin\beta_o (\frac{D_2 V_{d20}}{V_{ds2}} - C_2')$$

$$V_{ds2} = \sqrt{(K_I V_{20})^2 - V_{d20}^2}$$

$$V_{d20} = K_I V_2 \cos\beta_o + R_{ei} I_{do}$$

$$R_{ei} = \frac{3 m X_{ci}}{\pi}$$

$$F_2 = (1 + \frac{R_{S2}}{R_{L2}} - X_{S2} Y_{C2})^2 + (\frac{X_{S2}}{R_{L2}} + R_{S2} Y_{C2})^2$$

$$Z_{S2} = \sqrt{(R_{S2}^2 + X_{S2}^2)}$$

$$C_2' = - R_{S2} - \frac{Z_{S2}^2}{R_{L2}}$$

$$D_2 = X_{S2} - Y_{C2} Z_{S2}^2$$

Power Factor Control

The power factor at the inverter terminal is defined as [1].

$$y = \cos\phi_i = \frac{\cos\gamma + \cos\beta}{2}$$

The incremental equation for the above expression of power factor is

$$\Delta y = - \frac{\Delta\gamma \sin\gamma - \Delta\beta \sin\beta}{2} \qquad (2.17)$$

Substituting $\Delta\gamma$ from equation (2.9) into equation (2.17), we get

$$\Delta y = 0.5 [S_1' \Delta I_d + S_2' \Delta\beta] \qquad (2.18)$$

where $S_1' = S_1 \sin\gamma$; $S_2' = - (S_2 \sin\gamma + \sin\beta)$

Reactive Current Control

The reactive current at the inverter terminal is defined as [1]

$$I_R = K_I I_d \sin\phi_i$$

The linearized equations around the operating point of the reactive current are obtained from the above equation as follows:

$$\Delta I_R = \Delta I_d S_1'' + \Delta\beta S_2'' \qquad (2.19)$$

where $S_1'' = K_I \ (\sin\phi_i + I_d \cos\phi_i \ (-0.5 \sin\gamma/\sin\phi_i))$

$S_2'' = K_I \ I_d \cos\phi_i \ (0.5 \ (S_2 \sin\gamma + \sin\beta)/\sin\phi_i))$

Reactive Power Control

The reactive power at the inverter bus is defined as

$$Q = I_R \ V_2$$

The equation representing small changes in reactive power is obtained from the above expression, i.e.,

$$\Delta Q = S_1''' \ \Delta I \ + S_2''' \ \Delta\beta \tag{2.20}$$

where $S_1''' = (S_1'' \ V_2 - f_{di} \ I_R)$

$S_2''' = (S_2'' \ V_2 - f_{\alpha i} \ I_R)$

DC Voltage Control

The dc voltage at the inverter terminal is given by the following expression.

$$V_{d20} = K_I \ V_{20} \cos\beta_o + R_{ei} \ I_d \tag{2.21}$$

The incremental equation of dc voltage given by equation (2.21) is

$$\Delta V_{d20} = S_1^{IV} \ \Delta I_d + S_2^{IV} \ \Delta\beta$$

$$S_1^{IV} = (R_{ei} - K_I \ f_{di} \cos\beta_o)$$

$$S_2^{IV} = (K_I \cos\beta_o \ f_{\alpha i} + K_I \ V_{20} \sin\beta_o)$$

2.4 RESULTS AND DISCUSSION

The influence of the system and controller parameters on system stability are discussed next. The following controller configuration is implanted at the inverter terminal.

$$G_{CI}(S) = \left(\frac{K_p S + K_I}{S}\right)\left(\frac{1 + T_a S}{1 + T_b S}\right)$$

$$= K_c \left(\frac{\tau_c S + 1}{S}\right)\left(\frac{1 + T_a S}{1 + T_b S}\right) \qquad (2.22)$$

where K_c = controller gain

τ_c = controller time constant

The system parameters used to investigate the steady-state stability for the base case are reported in Table 2.1.

The Influence of Controller Gain on the System Stability

The sending ac system and the receiving ac system impedances are fixed so that the ac systems of the receiving end and the sending end have short circuit ratios of 4.0 and 1.5. The dc line time constant is fixed to 0.167. This system data is used for the base case. The basic reason for choosing the low short circuit ratio for the inverter ac system is that it causes larger voltage fluctuations and can cause voltage and power instability. Consequently, the controller must be designed to achieve good performance for these operating conditions. For digital simulation the dc line is represented with distributed parameters. Hence, the equivalent inductance and resistance of the

Table 2.1 Base Case System Parameters.

Sending AC System					Receiving AC System				
SCR	R_{S1} (Ohms)	X_{S1} (Ohms)	Y_{C1} (mhos)	r_{L1} (Ohms)	SCR	R_{S2} (Ohms)	X_{S2} (Ohms)	Y_{C2} (mhos)	r_{L2} (Ohms)
4.0	0.5	5.7	0.0045	10^{18}	1.5	7.8	36.57	0.0080	10^{18}

Effective Inductance of DC Links = 2.5 Henry.
Effective Resistance of DC Links = 1.5 Ohms.
Line to Line Voltage at the Inverter AC Bus = 230 kV.
Line to Line Voltage at the Rectifier AC Bus = 138 kV.
Base Value of Controller Gain = 5.0.
Base Value of Controller Time Constant = 0.08.

distributed dc line is considered here so as to produce the same time constant.

The influence of the controller gain in the range 5.0 to 25.0 is shown in Figure 2.4. The most sensitive roots of the characteristic equation are plotted in Figure 2.4. The following conclusions are drawn:

(a) As the controller gain increases, the system becomes less stable for various control modes.

(b) It is possible to obtain the same settling time for all control modes but for different gains.

(c) The system damping for all ranges of gain is less than 0.707. Hence, to achieve a system damping greater than 0.707, the controller gains need to be reduced. However, lower gain values may produce sluggish response [25].

The Influence of Receiving AC System's Short Circuit Ratio of the System Stability

The controller gain for all control modes is fixed to 5.0 so that a sufficient stability margin is available to study the effect of the receiving ac system's short circuit ratio. The receiving end short circuit ratio is varied from 2.00 to 1.05 to investigate its influence on stability. The reason for selecting these values of short circuit ratio is to determine the stability of the system around the base case of short circuit ratio of 1.5. The dc line time constant is fixed to its base value of 0.167. The movement of the dominant roots (positive

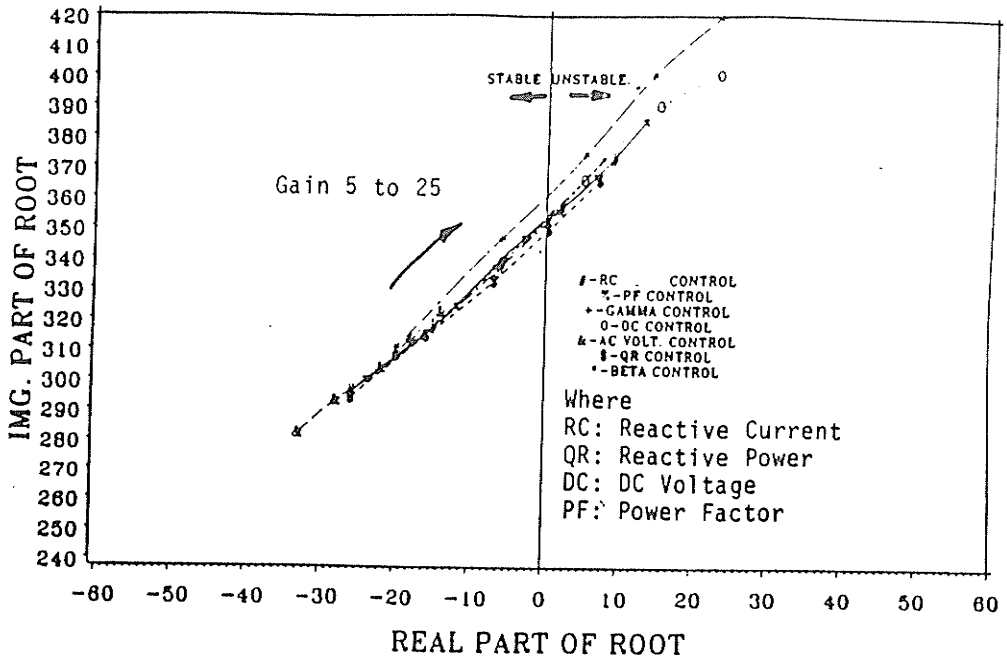


Figure 2.4 Influence of Controller Gain of Various Control Schemes at the Inverter on the Dominant Roots

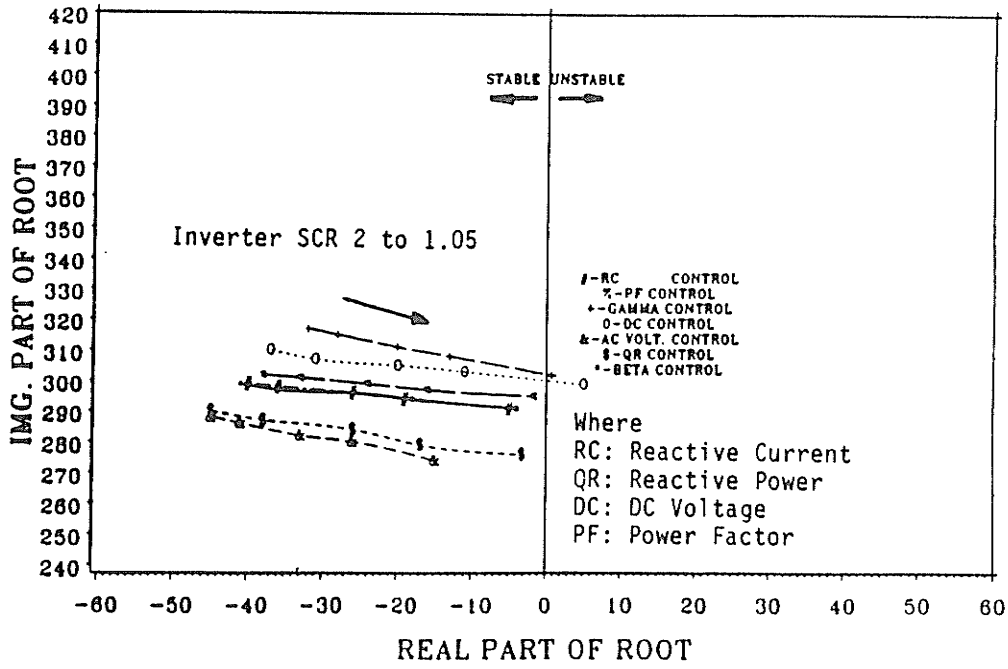


Figure 2.5 Influence of the Receiving AC Short Circuit Ratio on the Dominant Roots

imaginary part) is shown in Figure 2.5. The following conclusions may be drawn:

(a) As the short circuit ratio of the receiving ac system is reduced, the system response deteriorates and the system tends to become unstable.

(b) The controller gain must be lowered as the short circuit ratio of the receiving end reduces to achieve the desired response.

(c) The degree of stability varies for different control modes for the same controller setting. However, it can be forced to be the same by proper adjustments of gains as discussed in the previous section.

The Influence of the Sending AC System's Short Circuit Ratio on the System Stability

The receiving ac system impedance, dc line impedance, and controller gain are fixed to base values (Table 2.1). The sending ac system impedance is varied to obtained short circuit ratio 1.0 to 88.0. These numbers of short circuit ratios are chosen to represent very weak to very strong ac systems. Hence, this study will indicate the trend of stability within the two extremes.

The movement of the dominant roots (positive imaginary) is illustrated in Figure 2.6. It is observed from Figure 2.6 that, as the short circuit ratio of the sending end decreases, the system becomes more stable. This is a surprising result. It is further investigated in Chapter VI.

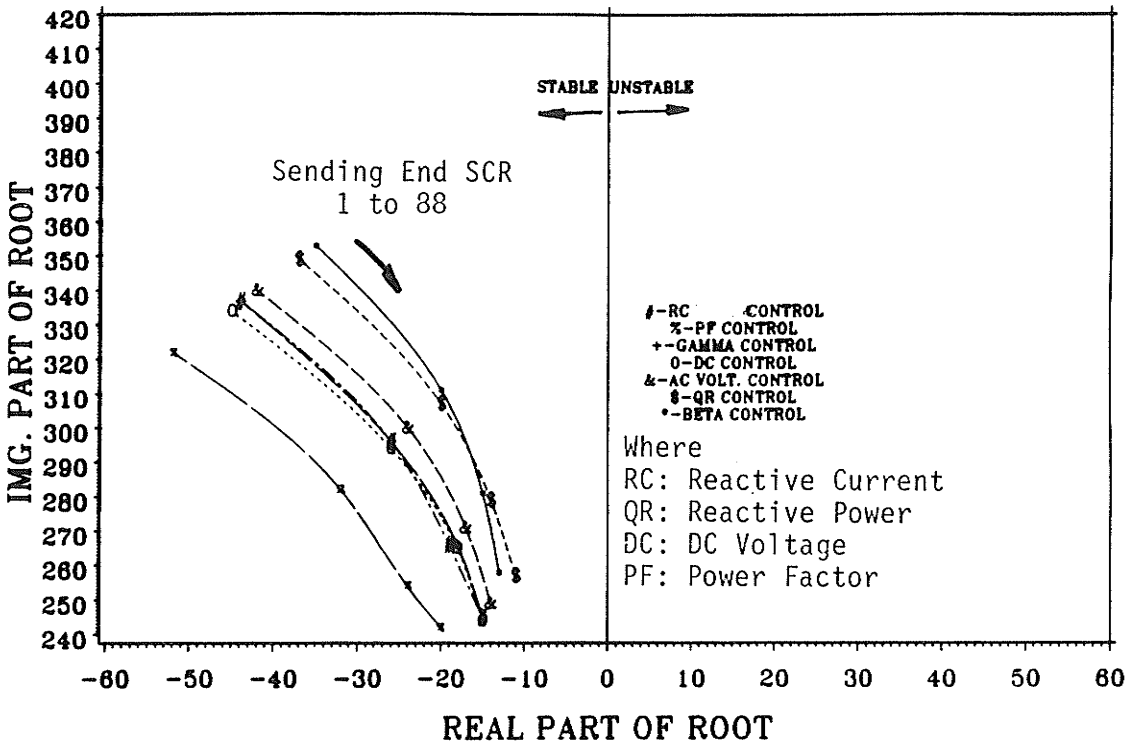


Figure 2.6 Influence of the Sending AC System Short Circuit Ratio on the Dominant Roots

The Influence of DC Line Resistance on the Stability of the System

The sending end and the receiving end short circuit ratios are fixed to base values of 4.0 and 1.5, respectively. The influence of the variation of dc line resistance is shown in Table 2.2. The lower value of dc line resistance indirectly indicates its length. It can be observed from Table 2.2 that an increase in the dc line resistance improves the system stability because the total loop gain is reduced as the dc system time constant becomes smaller.

2.5 CONCLUSIONS

With regard to improvement of the steady-state stability, the following conclusions are drawn from the study reported in this chapter.

i) High controller gains lead to instability.

ii) Higher short circuit ratio of the receiving ac system improves the stability.

iii) Lower short circuit ratio of the sending ac system improves the stability.

iv) Higher dc line resistance provides better damping.

Table 2.2 Effect of Variation of DC Line Resistance on the System Stability.

	Dominant Roots for Various Controls						
R_D in Ω	γ- Control	Power Factor Control	DC Voltage Control	AC Voltage Control	Reactive Current Control	Reactive Power Control	β-Control
5.0	-18±j306	-22±j295	-19±j303	-25±j289	-24±j291	-31±j278	-24±j291
15.0	-20±j311	-24±j300	-20±j308	-26±j294	-26±j296	-33±j282	-26±j296
30.0	-22±j319	-27±j306	-22±j315	-29±j300	-28±j303	-36±j289	-29±j303

CHAPTER III

AN APPROACH FOR HANDLING THE NON-LINEARITIES OF HVDC SYSTEMS FOR STABILITY ANALYSIS

3.1 INTRODUCTION

A hvdc system has many non-linear relationships among the different variables, e.g., the controller output 'α' relates to the converter output voltage through a relationship which contains the terms '$\cos\alpha$'. Therefore, the small perturbation technique has been used widely [26-28] for stability analysis. However, this technique takes into account only small changes around the operating point. Hence, a controller resetting may be needed for large changes in the operation. It has been shown that the converter [29-31] and the extinction angle control [13, 20] can be modelled as a linear system for large changes in the operating points, but the assumptions used are not realistic for this study. To overcome these limitations for the design of a control system for a hvdc scheme, a new approach is suggested to linearize the non-linearities of the hvdc system.

It is shown that the non-linearities introduced by the converter, real power and reactive power equations can be linearized over a wide range by using the integral square error (ISE) method. This chapter presents the modelling of each component of the hvdc system by using the ISE method for various control schemes described earlier on the inverter terminal (Chapter II).

A stability analysis of the reactive current control and the ac voltage control is reported in this chapter by using a new linearized model of a hvdc system. Power factor control modelling is also discussed. A stability analysis of the current control, the dc voltage control, and the predictive extinction angle control has been presented in reference [7], but the effects of linearized converter model and extinction angle equations are reported here.

The major assumption made for this study is that the voltage at the rectifier ac bus is constant. This assumption corresponds to the worst case for the stability analysis because the highest short circuit ratio of the rectifier ac system represents the least stable system (Chapter II). By using this assumption, the system modelling for stability analysis is discussed in subsequent sections.

3.2 CONVERTER MODELLING

The converter introduces non-linearity and delay [29] in the system as shown in Figure 3.1. Few attempts have been made for converter modelling [29-31]. The converter has been represented, so far, in the following three ways.

i) Simple delay [29]

ii) Transportation lag [30]

iii) Zero order hold [31]

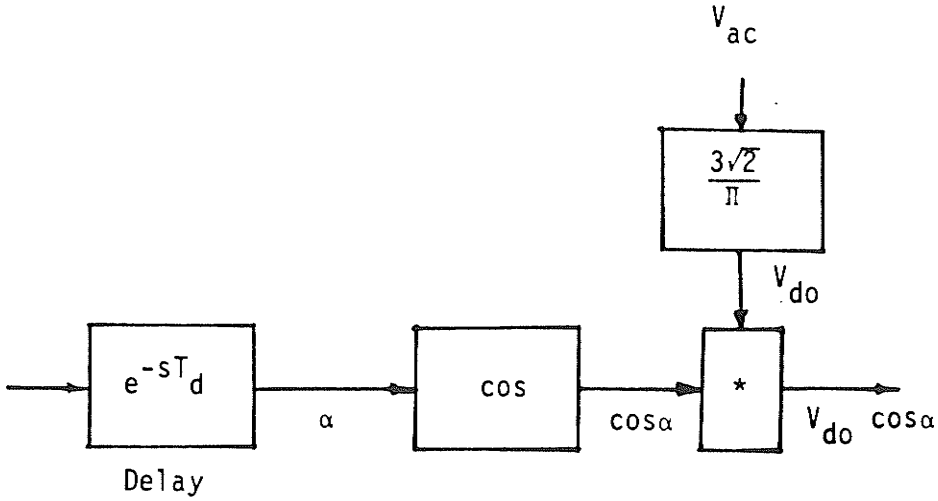


Figure 3.1 Converter Model

Bjarestem [29] relates the controller output to the converter output as shown in equation (3.1).

$$V_d = e^{-S\,T_o/2}\,V_r; \qquad (3.1)$$

i.e.,

$$T(S) = e^{-S\,T_o/2}$$

where

V_d = converter output voltage

V_r = control voltage

T_o = period by which output voltage of converter pulsates

However, the influence of the firing angle is ignored in the model. The model given by equation (3.1) has been simplified by Parrish and McVey [30] and the following transfer function has been suggested to represent the converter.

$$T(S) = \frac{1}{1 + T_d S} \qquad (3.2)$$

where T_d = 1/1440 for a twelve pulse converter.

The above model has been developed on the following assumptions.

i) The bandwidth is small in comparison to the sampling frequency.

ii) There is a limited excursion of the thyristor firing angle.

Hazell and Flower [31] derived the converter transfer function as Zero Order Hold, i.e.,

$$T(S) = \frac{1 - e^{-ST}}{S} \qquad (3.3)$$

where T = sampling time (T = 3.33 milliseconds typically for the six-pulse converter)

It is shown in reference [31] that the model given by equation (3.3) may cause large errors as the value of the firing angle, 'α', increases.

The relationship among the above-mentioned models is derived by applying Pade's approximation to equations (3.1) to (3.3),

$$e^{-S\,T_o/2} = \frac{1}{1 + S\,T_o/2} \text{ ; and } \frac{1 - e^{-ST}}{S} = \frac{T}{(1 + TS)} \qquad (3.4)$$

So, from the continuous system modelling viewpoint, these models are nearly the same, but all of the models include only small changes in firing angle.

A new converter model is presented here, which can include large changes in firing angle. The converter is represented as shown in Figure 3.1. The non-linearity in the model is introduced in terms of obtaining $\cos\alpha$ from α. The principle used for obtaining the equivalent linearizing function from the non-linear function is called minimization of the integral square error (ISE). Suppose '$\cos\alpha$' is to be linearized in the given range, then the problem can be defined as follows:

$$J = \min \int_{\alpha_1}^{\alpha_2} (A\alpha + B - \cos\alpha)\ d\alpha \qquad (3.5)$$

where J = cost function or error function

A = slope of the straight line

B = constant

The typical values of α_1 and α_2 are 15° to 60°. Then the following approximations of cosine and sine are obtained.

$$\cos\alpha = 1.16 - 0.58\alpha \tag{3.6}$$

$$\sin\alpha = 0.92\alpha - .0083 \tag{3.7}$$

Errors produced by the approximate linear relationship (equation (3.6)) are ±5% as shown in Figure 3.2. The important point indicated by equation (3.6) is that the converter model shows a negative slope.

The block shown in Figure 3.1 for the converter model shows delay, which is justified in the sense that the change in the firing angle can be observed only after T/p duration, where T is the period for fundamental ac voltage wave form and p is the pulse number of the converter. The influence of linearizing 'cos α' term on the converter model is shown in Figure 3.3.

3.3 LINEARIZATION OF REACTIVE AND REAL POWER FUNCTIONS

Reactive power and real power for the ac/dc/ac system can be represented as follows at the inverter terminal [1].

$$Q = V_1 I_1 \sin\phi_i \tag{3.8}$$

$$P = V_1 I_1 \cos\phi_i \tag{3.9}$$

where V_1 = rms line to line ac voltage at the inverter bus

$I_1 = \frac{\sqrt{6}}{\pi} I_d$, rms value of the fundamental component of line current

ϕ_i = power factor at the inverter terminal

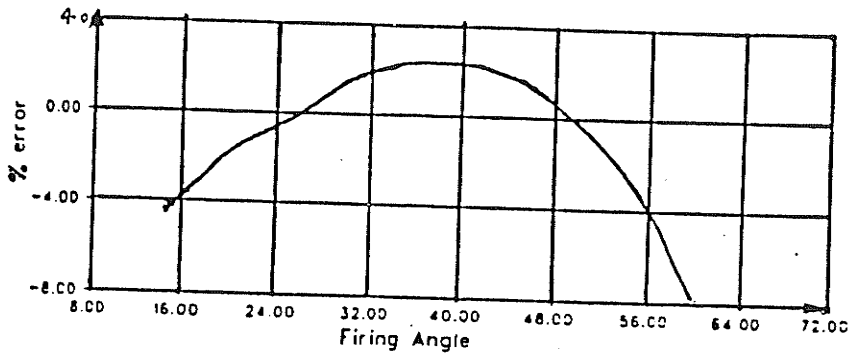


Figure 3.2 Error in Linearizing 'cos α'

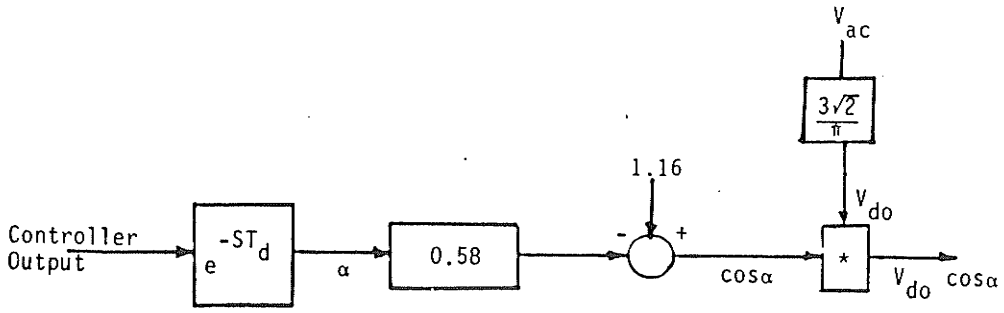


Figure 3.3 Modified Converter Model

Further, the power can be expressed as a function of the firing angle, direct current, commutation reactance, and ac voltage as shown in equation (3.10).

$$\cos\phi_i = \cos\beta + \frac{X_c I_d}{\sqrt{2}\, V_1} \tag{3.10}$$

The problem can be stated as follows:

$$\text{Min } J_1 = \int_{I_{d1}}^{I_{d2}} \int_{\beta_1}^{\beta_2} (Q - (A\beta + BI_d + C))^2 \, d\beta \, dI_d \tag{3.11}$$

and,

$$\text{Min } J_2 = \int_{I_{d1}}^{I_{d2}} \int_{\beta_1}^{\beta_2} (P - (A_1\beta + B_2 I_d + C_1))^2 \, d\beta \, dI_d \tag{3.12}$$

where

J_1, J_2 = error functions

Q = reactive power

P = real power

β = ignition angle

A, A_1, B, B_1, and C, C_1 = coefficients of the linearized expression

I_d = direct current

From equations (3.11) and (3.12), the following expressions of linearized P and Q are obtained for a commutating reactance, X_c = 10%.

$$Q = (0.7028\, I_d + 0.58\, \beta - 0.4225)\, V_1 \tag{3.13}$$

$$P = (0.6135\ I_d - 0.5996\ \beta + 0.4543)\ V_1 \qquad (3.14)$$

The errors between the non-linear and linearized functions for P and Q are shown in Figures 3.4(a) and 3.4(b). The error caused by a linear rate approximation is within ±5%. These linear relationships are used for the design of the controller and to determine the stability boundaries in the next section.

3.4 BASIC EQUATIONS FOR LARGE DISTURBANCE STABILITY STUDY

It has been assumed that the rectifier side ac system is strong, i.e., the variation in the ac voltage at the rectifier bus is neglected. It is proven by the small signal analysis of Chapter II that the system stability improves as impedance of the ac system of the rectifier end becomes higher. This means that the design of the controller parameters for the system provides the user the controller parameters which would give a better response than expected.

The ac system on the inverter end is represented as shown in Figure 3.5. The following relation is obtained on the inverter terminal from Figure 3.5.

$$V_2 = \left(V_1 + \frac{Pr_s + Qx_s}{V_1}\right) + \left(\frac{Px_s - Qr_s}{V_1}\right)^2 \qquad (3.15)$$

Suppose $\bar{V}_2 = V_2 \angle\theta$, $\bar{V}_1 = V_1 \angle 0$, then θ can be defined as

$$\tan\theta = \frac{x_s P - r_s Q}{V_1^2 + Pr_2 + Qx_2} \qquad (3.16)$$

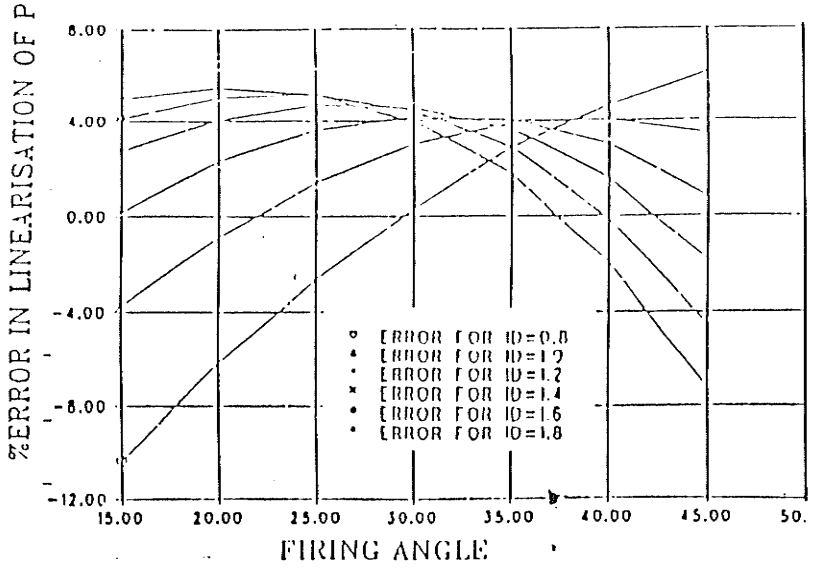


Figure 3.4(a) Error Due to Linearization of Active Power Expression

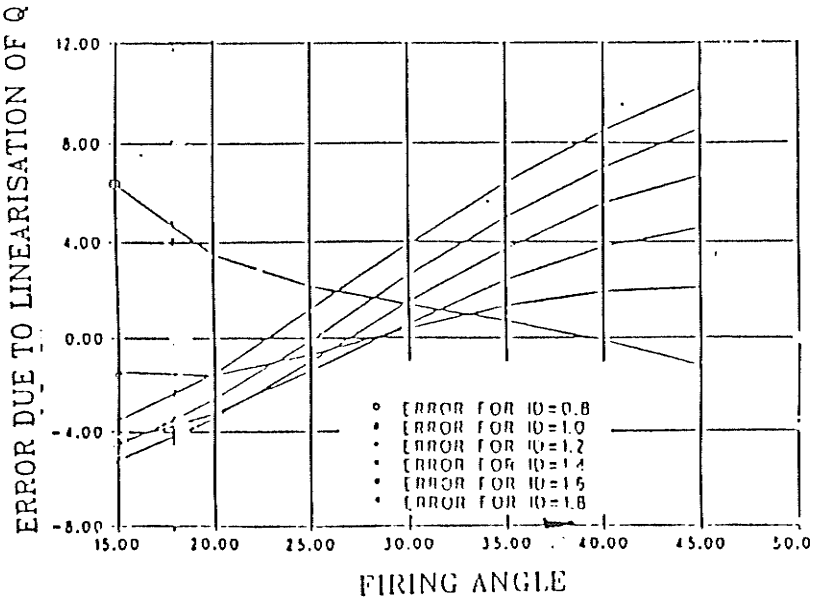


Figure 3.4(b) Error Due to Linearization of Reactive Power Expression

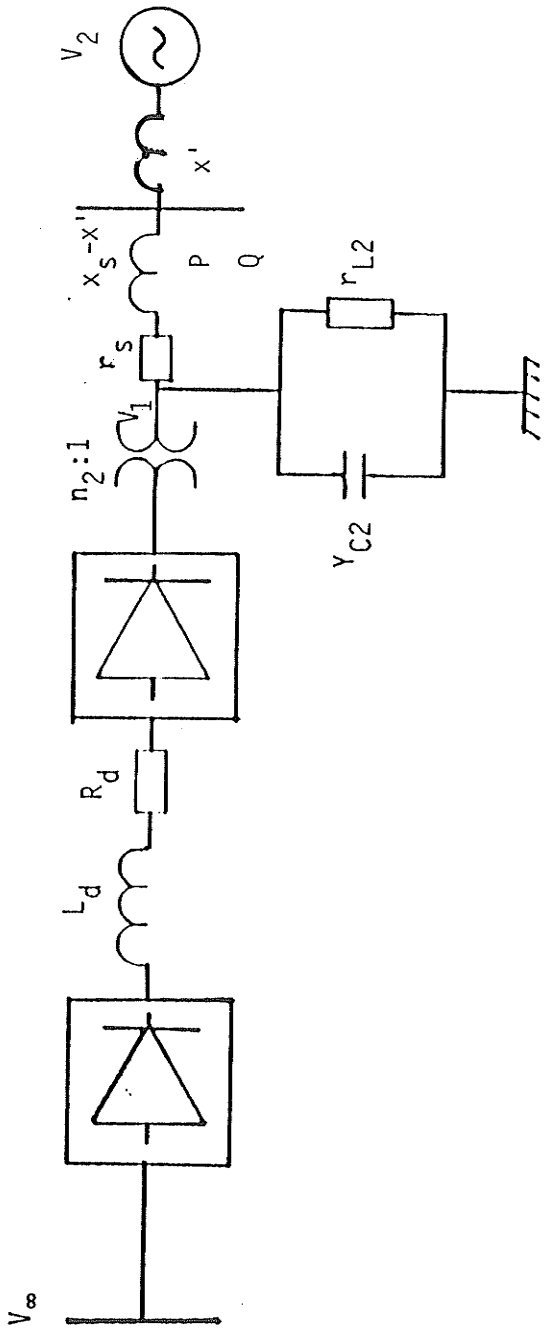


Figure 3.5 System Used for Determining Stability Boundaries

For small perturbations, equation (3.15) can be simplified to the following relationship.

$$\Delta V_1 = -\left(\frac{r_s + x_s \tan\theta}{V_1}\right)\Delta P - \left(\frac{x_s - r_s \tan\theta}{V_1}\right)\Delta Q$$

$$+ \{(r_s + x_s \tan\theta)\, P + (x_s - r_s \tan\theta)\, Q\}\frac{\Delta V_1}{V_1^2} \qquad (3.17)$$

3.5 BLOCK DIAGRAM FOR DIFFERENT CONTROLS AT THE INVERTER TERMINAL

The modelling for various control modes at the inverter terminal along with the constant current control at the rectifier terminal is discussed in this section.

Constant Current Control

During transients, it is possible that both the rectifier and the inverter operate in a constant current mode [20]. Hence, it is necessary to design a current controller at the inverter end. A block diagram can be obtained by substituting appropriate values from Table 3.1 into the block diagram of Figure 3.6.

Extinction Angle Control

This control is generally used with a minimum γ during a steady-state condition. The converter needs a minimum reactive power and generates the minimum magnitude of harmonics while operating in this control mode. The extinction angle is calculated from equation (3.18) as

$$\cos\gamma = \cos\beta + \frac{\sqrt{2}\, x_c I_d}{V_1} \qquad (3.18)$$

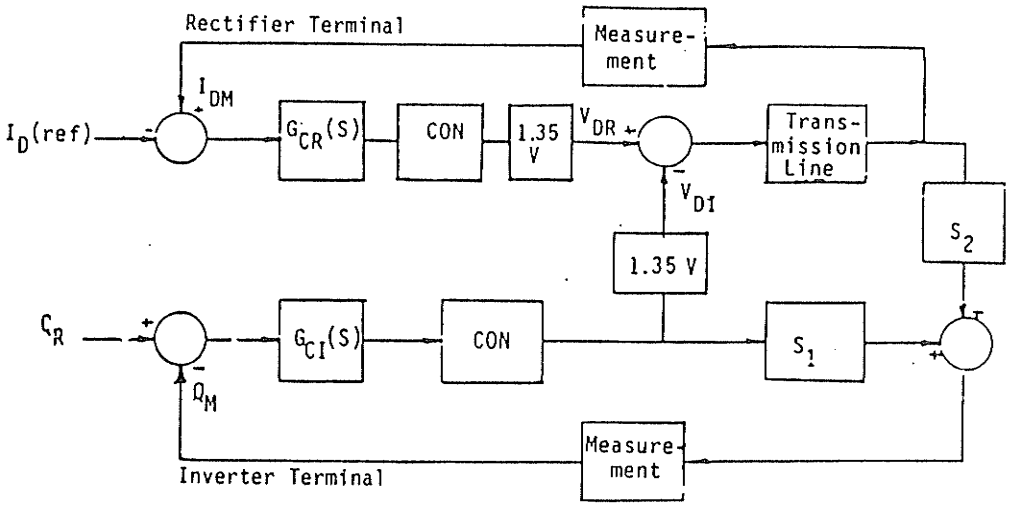


Figure 3.6 Block Diagram for Determining System Stability

Table 3.1 The Expression of S_1 and S_2 for Various Control Modes.

Type of Control	S_1	S_2
Extinction Angle Control	x_2	$+ \frac{\sqrt{2}\, x_c}{V_1}$
Current Control	0.0	1.0
Ignition Angle Control	1.0	0.0
DC Voltage Control	$1.35\, V_1$	0.0
AC Voltage Control	$(0.58 + 0.5996\, K_r)\, V_1$	$(0.702 + 0.6135\, K_r)\, V_1$
Reactive Power Control	$-\left(\frac{r_s + x_s \tan\theta}{K_s}\right) .599$	$\left(\frac{r_s + x_s \tan\theta}{K_s}\right) 0.632$
Power Factor Control	x_2	$\frac{x_c}{\sqrt{2}\, V_1}$

where $K_r = \frac{r_s + x_s \tan\theta}{x_s - r_s \tan\theta}$

The non-linear relationship of the extinction angle can be linearized by using equation (3.6) as

$$1.16 - 0.58\gamma = (x_1 - x_2\,\beta) + \frac{\sqrt{2}\,x_c I_d}{V_1} \qquad (3.19)$$

Values of x_1 and x_2 can be assigned depending upon the range of interest of the ignition angle and these values can be calculated by using equation (3.5). The simplified version of equation (3.19) is obtained as given below.

$$\gamma = 1.724\,\{(1.16 - x_1) + x_2\beta - \frac{\sqrt{2}\,x_c I_d}{V_1}\} \qquad (3.20)$$

The complete block diagram for obtaining the characteristic equation can be realized as shown in Figure 3.7. Appropriate values of S_1 and S_2 may be substituted from Table 3.1.

AC Voltage Control

This control has been suggested by Hammad [8] but its stability analysis has not been performed. Hence, system modelling is carried out to study the effectiveness of the control.

For ac voltage control, change in voltage would be zero. Hence, equation (3.17) reduces to the equation (3.21) as given below.

$$\Delta Q = -\frac{(r_s + x_s \tan\theta)}{(x_s - r_s \tan\theta)}\,\Delta P \qquad (3.21)$$

The integration of equation (3.21) produces equation (3.22).

$$Q = -\frac{(r_s + x_s \tan\theta)}{(x_s - r_s \tan\theta)} P + Q_{do} \qquad (3.22)$$

where Q_{do} = Constant of integration.

The non-linear equation (3.22) can be linearized by using equations (3.13) and (3.14). We get,

$$(0.702I_d + 0.58\beta - 0.4225)V_1 = V_1 \left[\frac{r_s + x_s \tan\theta}{x_s - r_s \tan\theta}\right]\{0.6135I_d - 0.5996\beta + 0.454\} + Q_{do} \qquad (3.23)$$

where Q_{do} is the reactive power required to maintain 1.0 p.u. ac voltage at the inverter bus at zero power factor, i.e., $P_d = 0.0$. The block diagram shown in Figure 3.6 has been obtained by substituting the value of S_1 and S_2 from Table 3.1. The influence of controller and system parameters has been investigated in the next section.

DC Voltage Control

Controlling the inverter at a constant dc voltage during certain operating range has been suggested so that the instability introduced by the negative slope of γ-control can be avoided [13]. The non-linearity in the dc voltage expression is due to the '$\cos\beta$' term. Linearization of this term has already been discussed in Section 3.2, and a complete block diagram can be obtained by substituting the appropriate values of S_1 and S_2 from Table 1 (Figure 3.6).

Reactive Current Control

This control has been suggested [10] for improving the power/voltage stability because of the positive slope characteristics.

Rewriting equation (3.17), we have

$$\Delta V_1 = - \frac{(r_s + x_s \tan\theta)}{V_1} \Delta P - \frac{(x_s - r_s \tan\theta)}{V_1} \Delta Q$$

$$+ \{(r_s + x_s \tan\theta) P + (x_s - r_s \tan\theta) Q\} \frac{\Delta V_1}{V_1^2}$$

where

$$\Delta P = \Delta P_L + \Delta P_d = \frac{2 V_1}{R_L} \Delta V_1 + \Delta P_d \qquad (3.24a)$$

$$\Delta Q = \Delta Q_d - \Delta Q_c = \Delta Q_d - 2 Y_c \Delta V_1 V_1 \qquad (3.24b)$$

The change in the ac voltage ΔV_1 can be further simplified, as given below, by using equation (3.17), (3.24a) and (3.24b).

$$\Delta V_1 = - (a \Delta P_d + b \Delta Q_d) \qquad (3.25)$$

where

$$a = (r_s + x_s \tan\theta)/K_s$$

$$b = (x_s - r_s \tan\theta)/K_s$$

$$K_s = \{1+2 \frac{(r_s + x_s \tan\theta)}{R_L} - (x_s - r_s \tan\theta) Y_c\} V_1$$

For constant reactive power control, $\Delta Q_d = 0$ and, hence, we get

$$\Delta V_1 = - a \Delta P_d \qquad (3.26)$$

By integrating equation (3.26), the following expression can be obtained.

$$V_1 = a P_d + K_o \tag{3.27}$$

where K_o is the constant of integration. It can be seen from equation (3.27) that the ac voltage support should be maintained in accordance with the dc power flow to obtain the constant reactive power control.

Linearization of equation (3.22) can be given as below by using equation (3.14). Thus,

$$V_1 = \frac{(r_s + x_s \tan\theta)}{V_1 K_s} \{0.6315 I_d - 0.5996 \beta + 0.4543\} V_1 + K_o \tag{3.28}$$

The block diagram for reactive power can be obtained by using appropriate values of S_1 and S_2 (Figure 3.6) from Table 3.1.

Power Factor Control

The power factor at the inverter terminal is normally given as

$$\cos\phi_i = \cos\beta + \frac{x_c I_d}{\sqrt{2}\, V_1} \tag{3.29}$$

Equation (3.29) can be linearized by using equations (3.6) and (3.19), which yields,

$$1.16 - 0.58\, \phi_i = (x_1 - x_2\, \beta) + \frac{\sqrt{2}\, x_c\, I_d}{V_i}$$

$$\phi_i = 1.724 \left\{(1.16 - x_1) + x_2\, \beta - \frac{\sqrt{2}\, x_c\, I_d}{V_i}\right\} \tag{3.30}$$

The block diagram for this control can be obtained by substituting appropriate values of S_1 and S_2 from Table 3.1.

Ignition Angle Control

The output of control circuit is firing angle (α) as shown in Figure 3.6. The ignition angle (β) can be calculated as

$$\beta = \pi - \alpha \tag{3.31}$$

The value of S_1 will be zero in this case.

3.6 RESULTS

The controller configuration at the rectifier and the inverter are considered similar to those given in Chapter II. The influence of the controller gains, the receiving ac system short circuit ratio, and line resistance on system stability is investigated. The results obtained from the steady-state stability are compared with results obtained from the new techniques.

Influence of Controller Gain on System Stability

The trends of system stability are similar to what has been demonstrated by a steady-state stability analysis. However, it is observed from Figure 3.7 that the new technique indicates that the system is less stable. It is justified because the controller parameters obtained from the steady-state stability analysis are always higher.

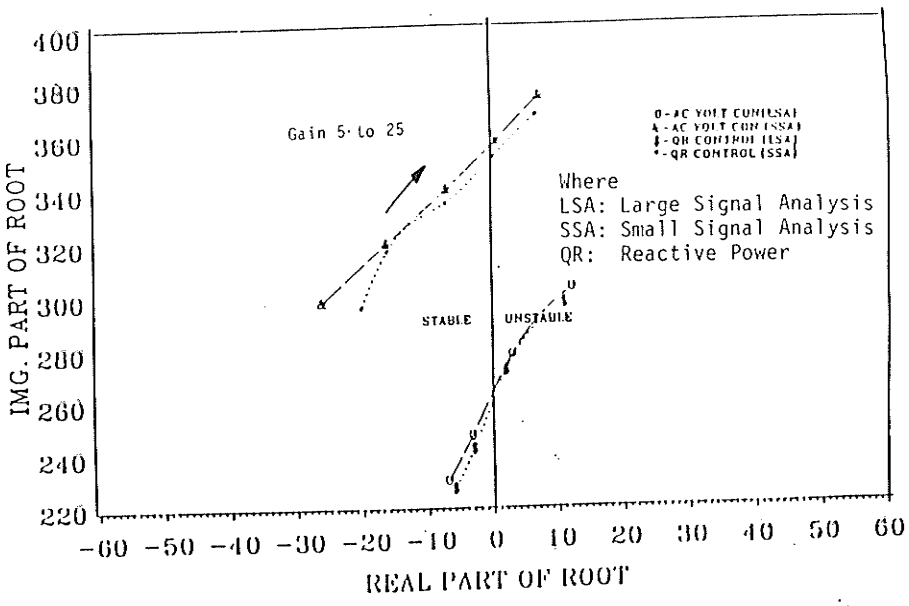


Figure 3.7 Influence of the System Gain on the Dominant Roots

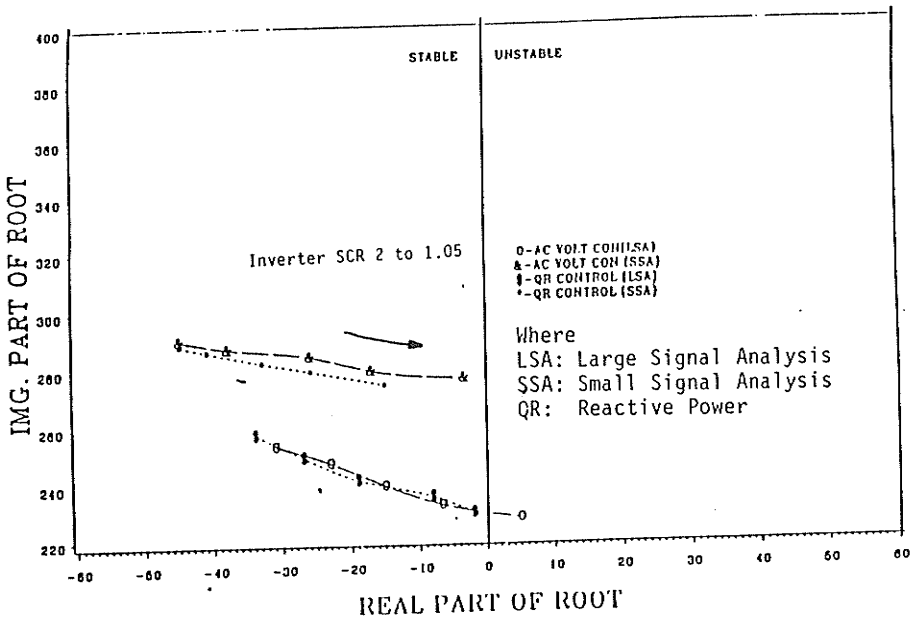


Figure 3.8 Influence of the Receiving AC System Short Circuit Ratio on Dominant Roots

Influence of the Receiving AC System Short Circuit Ratio on System Stability

As the short circuit ratio of the receiving ac system is raised, the system becomes less stable, as shown in Figure 3.8. It is also observed from Figure 3.8 that the value of the short circuit ratio at which the system becomes unstable is higher than that obtained from the steady-state stability analysis.

The Influence of Line Resistance on System Stability

As the dc resistance of the transmission line increases, the system stability improves (Table 3.2). Again, the new technique indicates that the system is less stable than what is indicated by the small signal analysis (Table 3.2.)

3.7 DISCUSSION

A new technique has been suggested to linearize the non-linearities involved in the converter equation, active and reactive power equations. The linearization of these equations is valid for a wide range of operation. The principle of integral square error (ISE) has been used to minimize the error between the non-linear equations and their corresponding versions. It has been determined that the influence of the firing angle (15°-55°) can be included in the model of the converter by just modifying the converter model gain to 0.58. The linearization of the active and reactive power expressions can be performed over a relatively wide region of operation of the hvdc system by minimizing the ISE. The direct current range of 0.8 p.u. to 1.5 p.u. is considered along with 5°-35° firing angle range to linearize the active and reactive power expressions. It has been observed that the error

Table 3.2(a) Influence of Line Resistance on the System Stability for AC Voltage Control.

DC Resistance in Ohms	Dominant Roots Small Signal Analysis	Dominant Roots Large Signal Analysis
15.0	-26.0 ± j294.0	-16.0 ± j273.0
30.0	-29.0 ± j300.0	-17.0 ± j277.5

Table 3.2(b) Influence of Line Resistance on the System Stability for Reactive Power Control.

DC Resistance in Ohms	Dominant Roots Small Signal Analysis	Dominant Roots Large Signal Analysis
15.0	-33.0 ± j282.0	-21.5 ± 249.0
30.0	-35.5 ± j289.0	-23.0 ± 257.0

produced by linearization of the converter, active and reactive power equations is only ±5%. These linearized expressions have been used to investigate system stability with ac and the reactive power control. The results obtained from the stability studies indicate that the system is relatively less stable than what has been shown by the small signal analysis in Chapter II. However, sensitivity to the controller gains, the sending ac system impedance, and receiving ac system impedance have been observed to be similar to small signal analysis studies. The control system analysis reported in this chapter provides the background for designing the controller for relatively larger changes in the operating points.

3.8 CONCLUSIONS

The following conclusions are drawn from the study in this chapter.

i) Non-linearities of the hvdc system can be linearized over a wide range with ±5% error.

ii) The effects of the firing angle for the stability analysis can be included by modifying the converter model by simple gain of 0.58 in the converter model block.

iii) Stability predicted by the steady-state stability analysis is on the higher side than what is determined from the new technique.

CHAPTER IV

EXPERIMENTAL STUDY OF HVDC CONTROLS AT THE INVERTER TERMINAL

4.1 INTRODUCTION

In Chapter II a theoretical study was performed to develop an understanding of the influence of various controls and system parameters on the system stability. In this chapter the results of an experimental study are described. The experimentation could not be very extensive because of hardware limitations. The purpose of this study was to develop a quick feel for the relative effectiveness of various control modes at the inverter terminal. Further, the study may be used to select critical faults. The effectiveness of various control modes is measured in terms of the dc power recovery time and magnitude and duration of overvoltages at the inverter ac bus. The study was carried out on the real time, physical component simulator available at the University. Various control schemes were considered at the rectifier and the inverter terminals.

Rectifier Terminal

a) Minimum firing angle control, and

b) Constant current control

Inverter Terminal

a) Extinction angle control

b) Constant current control

c) Power factor control

d) Reactive power control

e) DC voltage control

f) AC voltage control

Extinction angle and constant current controls are normally provided at the inverter terminal of hvdc schemes [1]. This combination of controls will hereafter be referred as the conventional control for the inverter terminal.

Time of the dc power recovery, magnitude and duration of over-voltages on the system are studied subsequent to the application of various system faults. These studies are repeated as the inverter operates with different controls. The system specifications and typical faults used for the investigations are discussed in subsequent sections.

4.2 TEST SYSTEM

The hvdc system shown in Figure 4.1 is used to investigate the effectiveness of various control modes at the inverter terminal. This is a very simple system because an extensive system cannot be represented on the real time physical component simulator on account of the limitations on the number of available components. The following simplifications are made to realize a hvdc system with six-pulse converters.

i) AC filters at the rectifier terminal are not modelled.

ii) DC line is represented by one lumped π section.

iii) DC filters at the dc side of the rectifier and the inverter are not modelled.

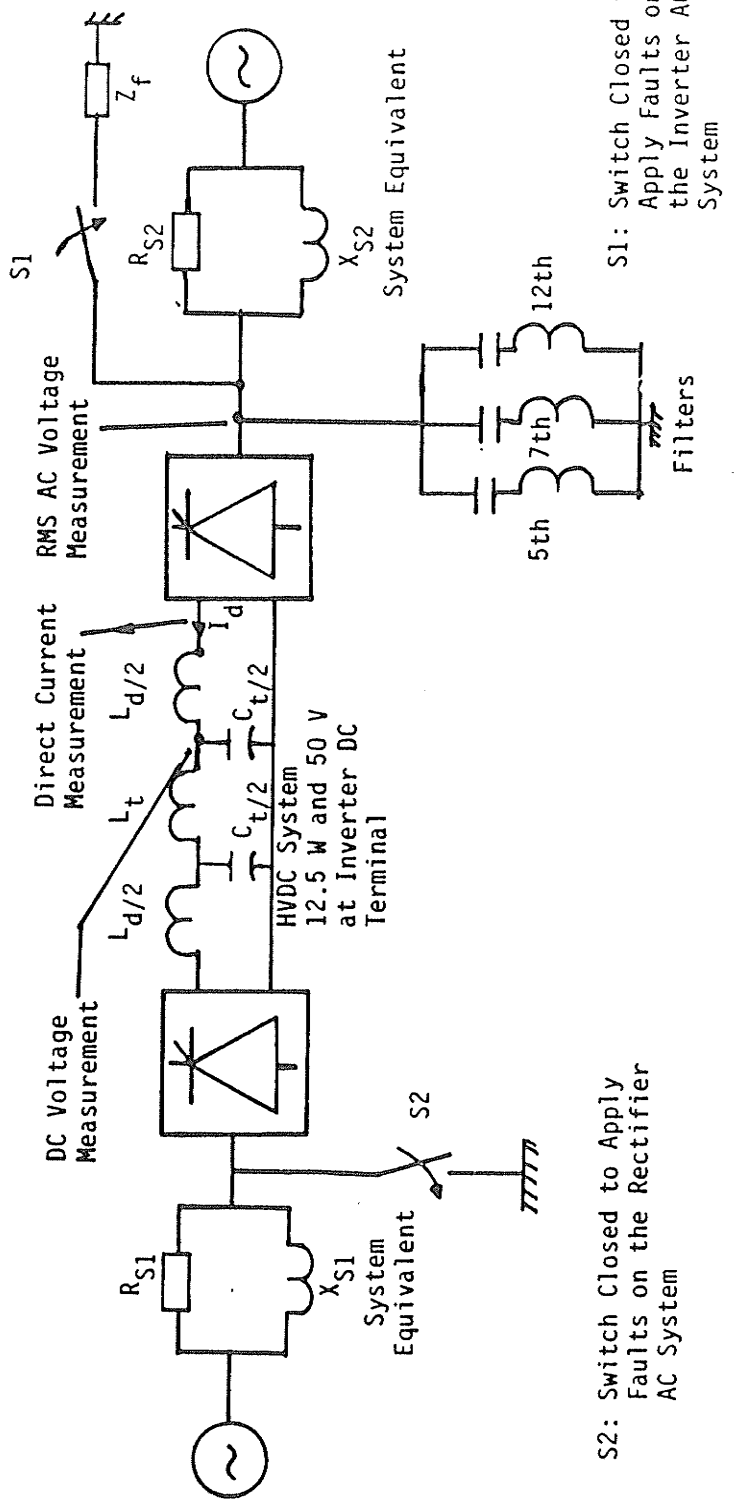


Figure 4.1 The System for Investigating the System Recovery from Various Faults

iv) AC filters at the inverter terminal are modelled as 5th, 7th, and 12th harmonic filters. The 12th harmonic filter is modelled in place of 11th and 13th harmonic filters.

v) VDCL and commutation dc ramp circuits are not implemented.

The elimination of the ac and dc filters at the rectifier terminal may cause distortion of voltage at the ac bus. This distortion may cause higher magnitude of 6th harmonics at the dc terminal. However, the 6th harmonic filter is provided in the voltage and current measurement circuits. Hence, the current control performance at the rectifier terminal may not be influenced. The influence of harmonics on the firing circuits and control system is normally significant only for high gains of control loops [1]. In addition, the ac and dc filters are also provided to reduce telephone interference with neighboring transmission lines and to minimize heating of capacitors and generators and noise on the telephone line [1]. However, in the simulator study of various inverter controls, the above-mentioned effects of ac and dc harmonics are not important. Hence, the influence of ac filters at the rectifier terminal and dc filters at both the rectifier and the inverter terminals may not influence the control characteristics at the inverter terminal since all measuring circuits are provided with low pass filters.

The voltage dependent current limit (VDCL) and direct current ramp circuits are normally implanted to improve the system recovery [32]. Since none of the control schemes is provided with these features, the relative performance of control schemes may not be influenced.

The ac systems, dc line, and ac filter parameters are listed in Appendix A1. The system is characterized by a short circuit ratio of

4.0 for the sending ac system and a short circuit ratio of 2.0 for the receiving ac system. Consequently, the influence of the low short circuit ratio of the receiving ac system on system recovery from various faults may be studied. Various faults and their durations are reported in the next section.

4.3 FAULTS FOR SYSTEM TEST

The following faults are applied to the system to determine the effectiveness of various control modes at the inverter terminal.

Three Phase to Ground Fault is the most severe fault [33]. Hence, it is necessary to determine the system recovery from the fault to evaluate various control modes. The direct and remote faults are applied at the inverter ac bus. As well, this fault is applied directly to the rectifier bus. Three phase ac faults applied directly at the inverter bus or rectifier bus depress the ac voltage at the ac bus to zero, whereas, a fault applied remotely from the inverter bus reduces the voltage at the inverter bus to a low value but not to zero. Remote faults are, therefore, applied in the model through impedance as shown in Figure 4.1. For the tests described in this chapter, the fault impedance (Z_f) is chosen in such a manner that for duration of the fault the ac voltage at the inverter bus is depressed to 0.5 p.u.

Single Phase to Ground Fault is the most frequent fault [33] which occurs on the system. Hence, this fault is applied directly and remotely at the inverter terminal as described above, and this fault is directly applied on the rectifier terminal.

DC Line Fault is applied on the dc terminal of the inverter as shown in Figure 4.1. The duration of this fault has been kept at 200 ms.

These faults are created by using the computer program available on the simulator written in Turbo-PASCAL. This software package has the facility to vary the duration and the type of the fault. The computer controlled relays are used to apply various faults.

4.4 MEASURE OF EFFECTIVENESS FOR VARIOUS CONTROL MODES

The following two measures are used in evaluating the effectiveness of various control modes at the inverter.

i) Peak Value of Overvoltages at the AC Bus of the Inverter: The magnitude of instantaneous overvoltages determines the insulation level and stresses on the valves. The voltage of only one phase (phase A) is shown in the results discussed in this chapter.

ii) DC Power Recovery Time: The faster the system recovers from faults to a healthy condition, the better it is for the consumer and for stable operation of the system. The dc power recovery time is defined as the time elapsed for the dc power to recover to 80% of its steady-state value.

The measurement of the dc power is performed by the use of a programmable oscilloscope. Two channels of the oscilloscope simultaneously scan the dc voltage at the inverter terminal and the direct current. The wave-forms in these two channels are multiplied to obtain the dc power.

The dynamic overvoltage trace was not recorded due to limitations on the number of available channels of oscilloscopes.

4.5 IMPLEMENTATION OF VARIOUS CONTROL MODES

Measurement Circuits

Standard measurements circuits were available on the simulator to measure currents, voltage and extinction angle [34].

Current Measurement: The direct current measurement at the inverter and the rectifier terminals is performed by using the LEM shunts. The magnetic flux in the iron-core of the LEM shunt is measured with a Hall probe and compensated to zero by means of subsequent electronic circuits. An additional circuit is available to compensate the dc offset [34].

Extinction Angle Measurement: The measurement of the extinction angle is performed by using an 8087 microprocessor chip. The voltage across the non-conducting valve is used to calculate the extinction angle [34]. The extinction angle measurement card is available in the simulator.

AC Voltage Measurement: The ac voltage in all three phases is measured by using a divider and compensation network at the inverter ac bus [34]. The outputs of all the three transducers are fed to the full wave diode rectifier to obtain the rms value of the three phase voltage. The smoothing of ripples is performed by using a filter tuned to the 6th harmonic frequency to eliminate the effect of the 6th harmonic component.

DC Voltage Measurement: DC voltage measurements are carried out in a manner similar to the ac voltage measurement at the dc terminal of the inverter.

Reactive Power Measurement: The instantaneous reactive power can be defined as follows [35].

$$Q = \frac{1}{\sqrt{3}} (v_{ab} i_c + v_{bc} i_b + v_{ca} i_b) \qquad (4.1)$$

Equation (4.1) is valid for a balanced circuit. It is evident from equation (4.1) that a multiplication chip is required. The analog multiplication chip No. MC1594L [36] is used. Three multiplications are carried out simultaneously and their outputs have been added through operational amplifiers with a proper gain of 0.577 to accommodate the factor of $1/\sqrt{3}$ of equation (4.1).

Power Factor Measurement: The power factor can be calculated approximately by the relationship given below [1].

$$\cos\phi = \frac{V_{di}}{K_i V_{ac}} \qquad (4.2)$$

where $\cos\phi$ = power factor

V_{di} = dc voltage at the inverter end

$K_i V_{ac}$ = no load dc voltage

The measurement of the power factor is carried out by using Chip No. MC1594L [36] and signals V_{di} and V_{ac}.

The complete block diagram representing the salient features of the real time, physical component simulator available at the University is shown in Figure 4.2. All control circuits are realized with the P-I controller. The P-I card is supplied by Brown Boveri. The functional block diagram for realization of various control modes at the inverter terminal is shown in Figure 4.3. Each control mode (c-f) is tested without the combination of the current control at the inverter terminal.

4.6 SYSTEM RESPONSE TO VARIOUS FAULTS

The system response to various faults is observed for each control scheme. The controller parameters are selected by repeating the experiments. However, the instant of the fault could not be controlled. Hence, the controller parameters were selected by observing the best response for the single phase to ground fault at the inverter bus.

The control parameters used for system recovery are listed in Appendix A1. The same controller parameters are used to investigate the system recovery for other faults.

AC Voltage Response: The following comparison can be made for different faults by considering only the ac voltage response at the inverter ac bus. The control mode which produces the minimum magnitude and duration of the ac overvoltage and minimum dc power recovery time is normally regarded best.

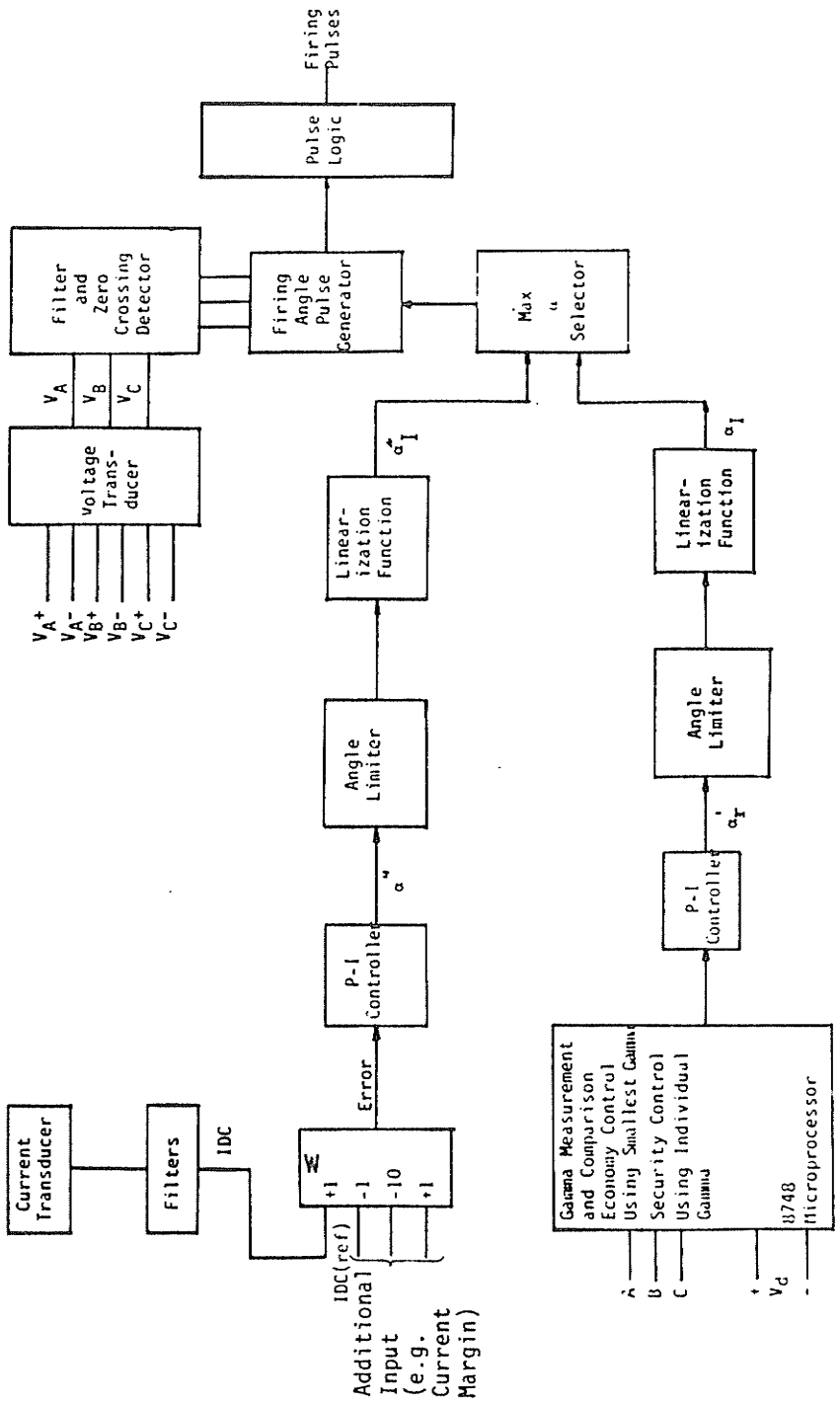


Figure 4.2 Complete Control System on the Inverter Terminal [34]

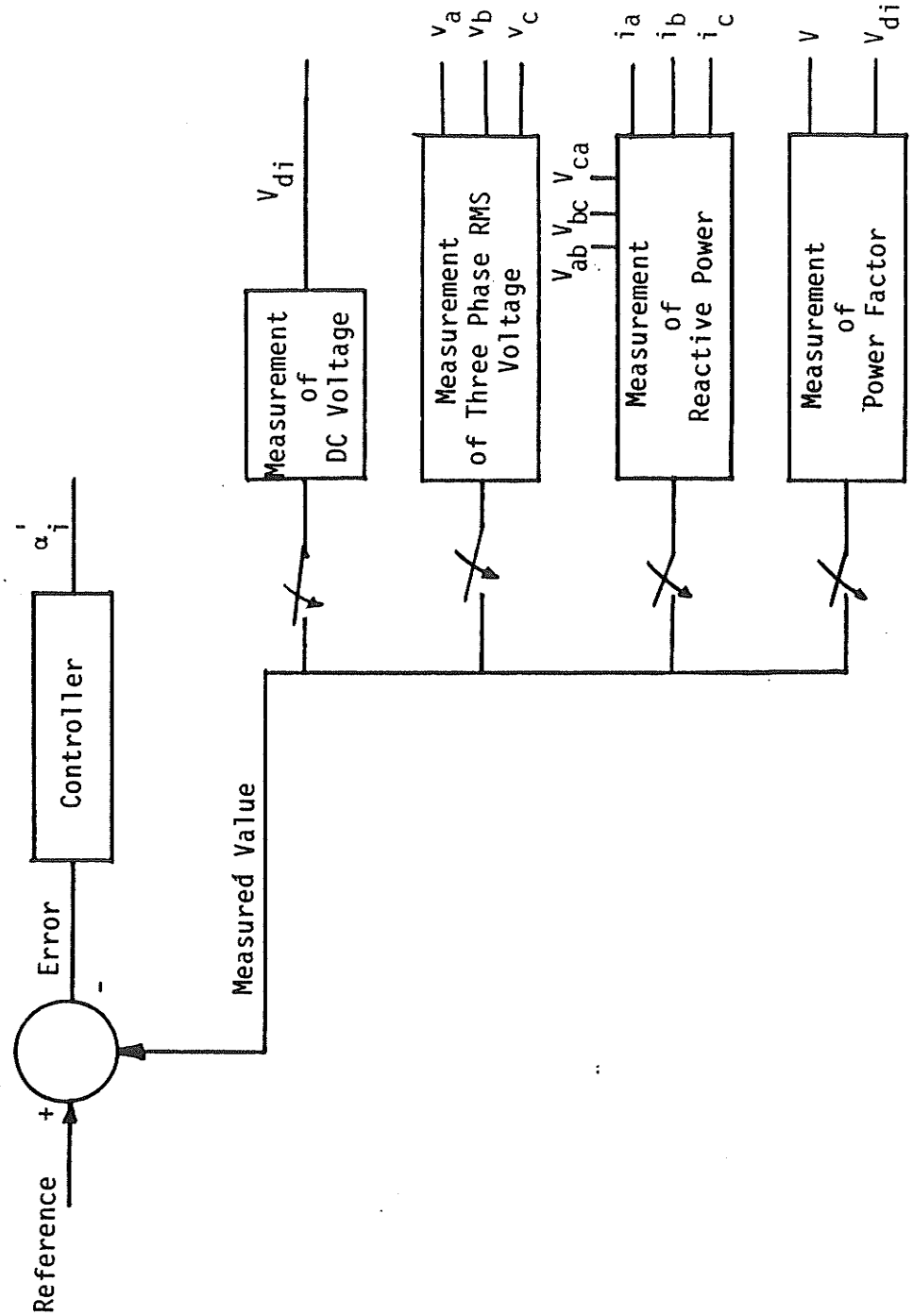


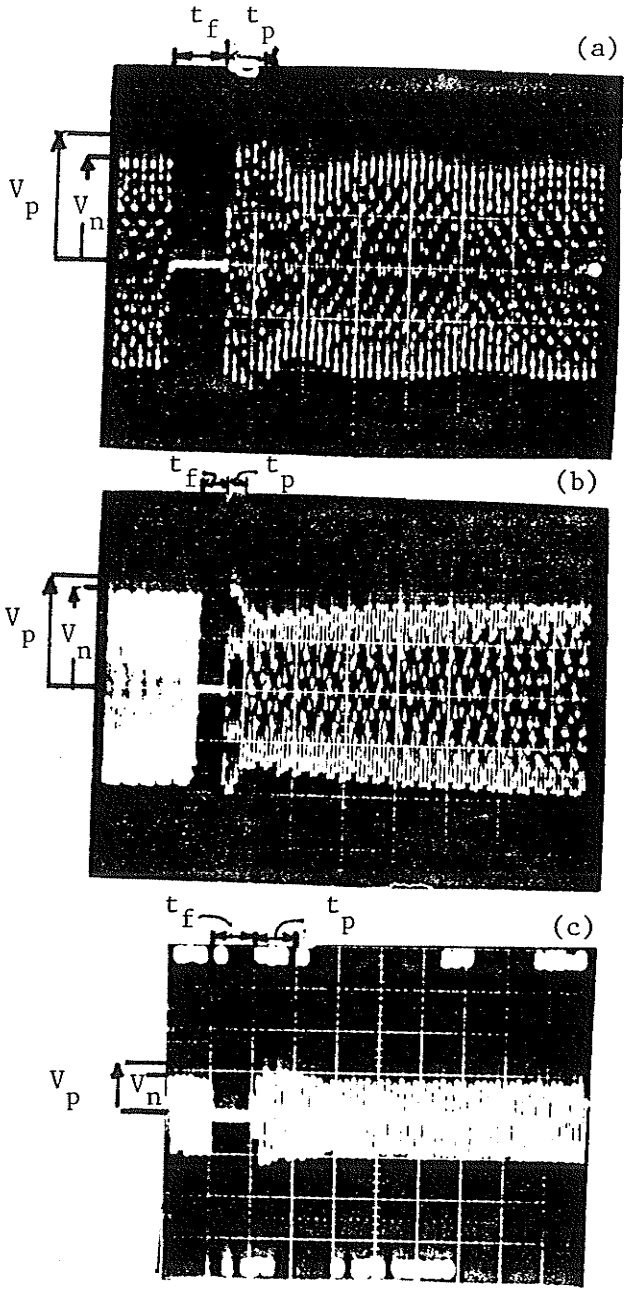
Figure 4.3 Simplified Representation of Implementation of Various Control Schemes at the Inverter Terminal

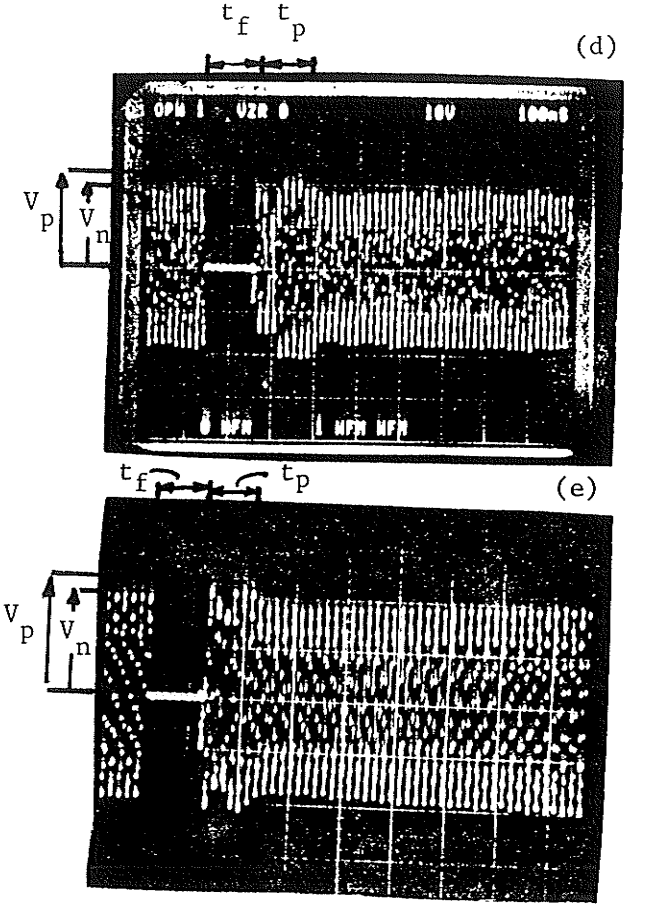
Three Phase Fault at the Inverter Bus: Records of the ac voltage for various control modes are shown in Figure 4.4. The following observations can be made from Figure 4.4.

a) The duration (100 ms) of overvoltages is the same for all cases.

b) The slowest recovery from ac voltages is observed for the power factor control. The reason is that the division circuit goes into saturation because of an undefined value of the power factor defined by equation (4.2). The solution to this problem is considered in Chapter V.

Similarly, the ac voltage response can be observed for other faults and traces of these faults are presented in Appendix A2. The results for the ac voltage response for all faults are summarized in Table 4.1(a) to Table 4.1(g).





Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	200	10
c.	DC Voltage	100	20
d.	AC Voltage	100	10
e.	Reactive Power	100	10

Figure 4.4 AC Voltage Response for the Three Phase To Ground Fault at the Inverter AC Bus

Table 4.1(a) System Response to the Three Phase to Ground Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.22	100	45
Power Factor	1.11	100	75
DC Voltage	1.18	100	75
AC Voltage	1.20	100	130
Reactive Power	1.22	100	75

Table 4.1(b) System Response to the Single Phase to Ground Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.20	58	85
Power Factor	1.20	70	45
DC Voltage	1.20	65	76
AC Voltage	1.20	100	135
Reactive Power	1.20	58	43

Table 4.1(c) System Response to the Remote Three Phase Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.17	50	62
Power Factor	1.17	80	62
DC Voltage	1.20	80	62
AC Voltage	1.21	130	85
Reactive Power	1.10	66	62

Table 4.1(d) System Response to the Remote Single Phase Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.15	50	36
Power Factor	1.15	65	25
DC Voltage	1.15	80	36
AC Voltage	1.15	50	64
Reactive Power	1.15	66	25

Table 4.1(e) System Response to the Single Phase to Ground Fault at the Rectifier AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.15	50	29
Power Factor	1.15	66	29
DC Voltage	1.15	0	29
AC Voltage	1.20	0	22
Reactive Power	1.20	30	29

Table 4.1(f) System Response to the Three Phase to Ground Fault at the Rectifier AC Bus.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.20	30	257
Power Factor	1.20	58	36
DC Voltage	1.20	58	50
AC Voltage	1.20	0	22
Reactive Power	1.20	16	29

Table 4.1(g) System Response to the DC Line Fault at the Inverter Terminal.

Control Scheme	Instantaneous Voltage Response		DC Power Recovery Time in ms t_r
	Highest Magnitude in p.u. V_p	Duration in ms t_p	
Conventional	1.10	500	671
Power Factor	1.15	580	671
DC Voltage	1.15	65	71
AC Voltage	1.20	0	128
Reactive Power	1.15	0	30

DC Power Recovery

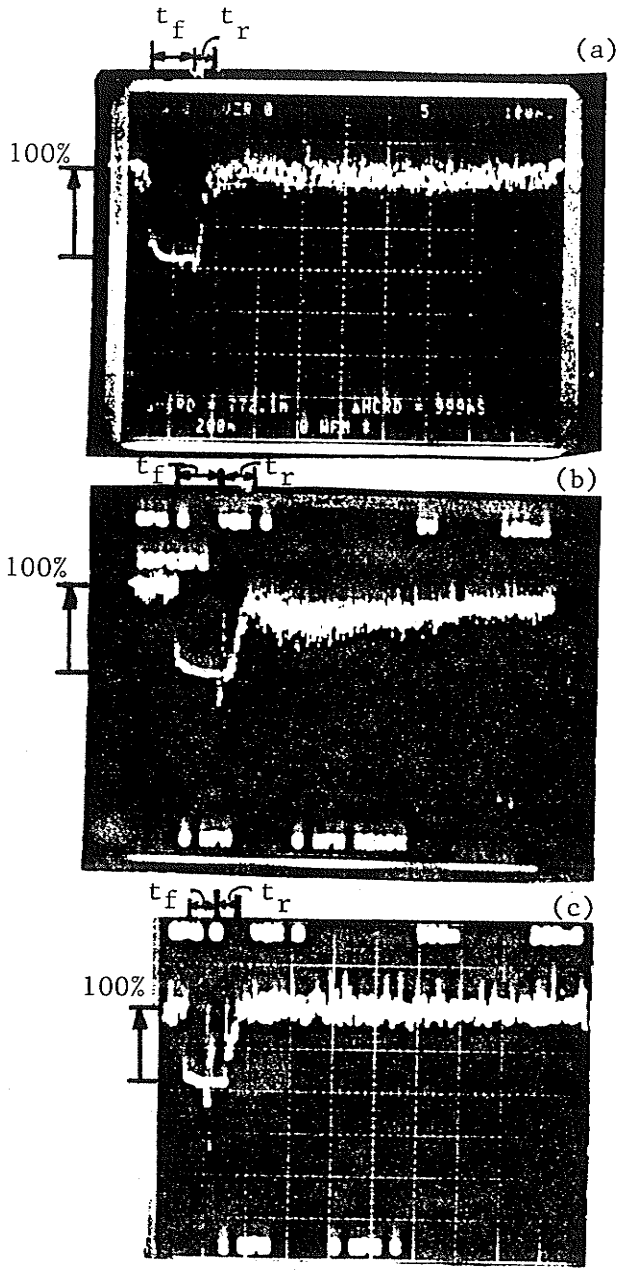
Shorter recovery time of the dc power indicates better system stability. Hence, the control scheme which produces the fastest recovery of the dc power without causing instability is regarded as the best control scheme. The dc power recovery from various faults is discussed below.

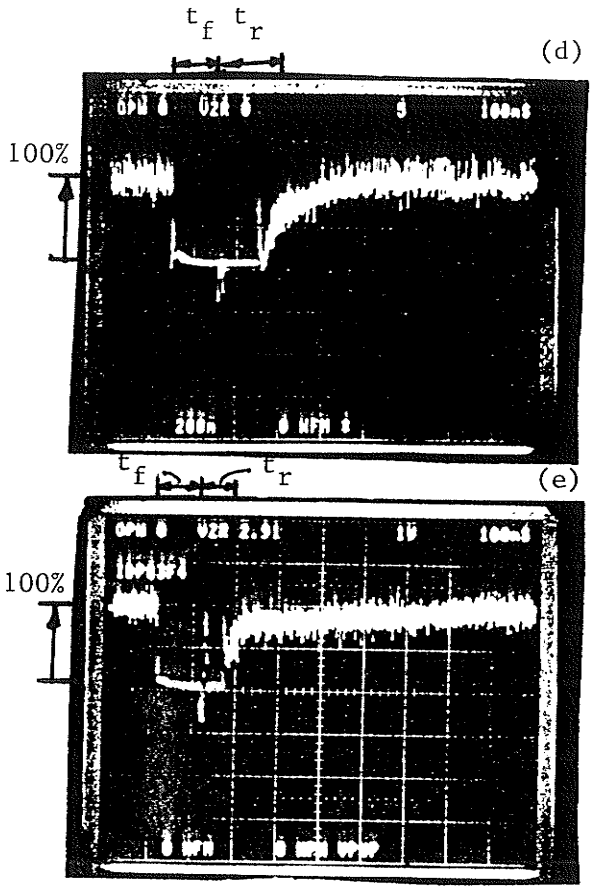
Three Phase to Ground Fault: The dc power recovery from the three phase to ground fault at the inverter is illustrated in Figure 4.5. The duration of recovery for each control scheme is listed in Table 4.1(a). The following observations may be made from Figure 4.5.

a) The recovery time for the reactive power control, the power factor control, and the dc voltage control is the same (75 ms). However, the dc power recovery is not acceptable for the power factor control because of longer settling time.

b) The slowest recovery is achieved through ac voltage control (130 ms).

Similarly, the dc power recovery can be observed for various faults. The traces of dc power for other faults are presented in Appendix A3. The dc power recovery time for all faults is summarized in Table 4.1(a) to Table 4.1(g).





Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	100	6.0
b.	Power Factor	100	6.0
c.	DC Voltage	200	6.25
d.	AC Voltage	100	6.0
e.	Reactive Power	100	6.25

Figure 4.5 DC Power Recovery from the Three Phase to Ground Fault at the Inverter AC Bus

4.7 DISCUSSION

Various control modes at the inverter terminal are implemented on the real time, physical component simulator available at the University. The effectiveness of each control mode is determined by the system ac voltage response and the dc power recovery time from various ac and dc faults.

The system response for the remote ac faults and the single phase to ground fault at the rectifier ac bus has been determined to be similar (Table 4.1(c) to Table 4.1(e)). Further, it has also been observed from Table 4.1(a) through Table 4.1(g) that the performance of the reactive power control and the dc voltage control is comparable. However, the value of the results obtained in this chapter is qualitative because of the limitation of the real time, physical component simulator. A more detailed representation is used for digital simulation in the next chapter. Hence, no attempt will be made to correlate the physical simulator and digital simulation results. Further, this study has been performed to generate a quick impression of the relative performance of various controls and to determine the possible critical faults.

The concept of operating the hvdc system during steady-state with any control mode other than the extinction angle control is undesirable because all other control modes operate at a higher extinction angle. The operation at the a higher extinction angle causes higher reactive power demand and stresses on the valves. Hence, it is decided to introduce any of the control modes during transients only. Once the steady-state is reached, the system operation is reverted to the extinction

angle control. Influence of the switching control modes on the operation of the system is reported in subsequent chapters.

CHAPTER V

DIGITAL SIMULATION STUDIES

5.1 INTRODUCTION

The steady-state stability analysis of the hvdc system with various control schemes at the inverter terminal has been reported in Chapter II. Further, an initial impression of the relative performance of various control schemes at the inverter terminal has been obtained for the system recovery from various ac and dc side faults at the rectifier and the inverter terminals in Chapter IV. The results obtained in Chapter IV are qualitative because of the limitation of the setup. Hence, a more detailed representation is used for digital simulation in this chapter, and no attempt is made to compare the results of the physical simulator and digital simulation.

There are various techniques available in the literature for simulating hvdc systems in detail on a digital computer [37-39]. However, the use of the EMTP and EMTDC packages has become more popular because of their versatility and user friendliness [40-42]. These simulation studies of hvdc systems are limited to conventional control modelling at the inverter terminal of the hvdc system. This chapter is devoted to the modelling of the hvdc system and its various control schemes using the EMTDC package for digital simulation and study of the system recovery for some of the critical faults reported in Chapter IV.

Power system dynamics is simulated in the time domain with three phase representation of an ac network in the EMTDC package. Subroutines

are available to model a frequency dependent distributed transmission line, generalized six-pulse thyristor bridge with damping circuits, transformer saturation, metering system, and the dc conventional controls. Various control schemes (c-f) are reported in Chapter IV in Section 4. In addition, the reactive current control is modelled at the inverter terminal and interfaced with the EMTDC package to complete the literature.

These computer programs can be used to interface various control schemes with the EMTDC package at the rectifier terminal by appropriately changing limits on the firing angles and controller gain and time constants.

5.2 MODELLING OF AC-DC-AC SYSTEM

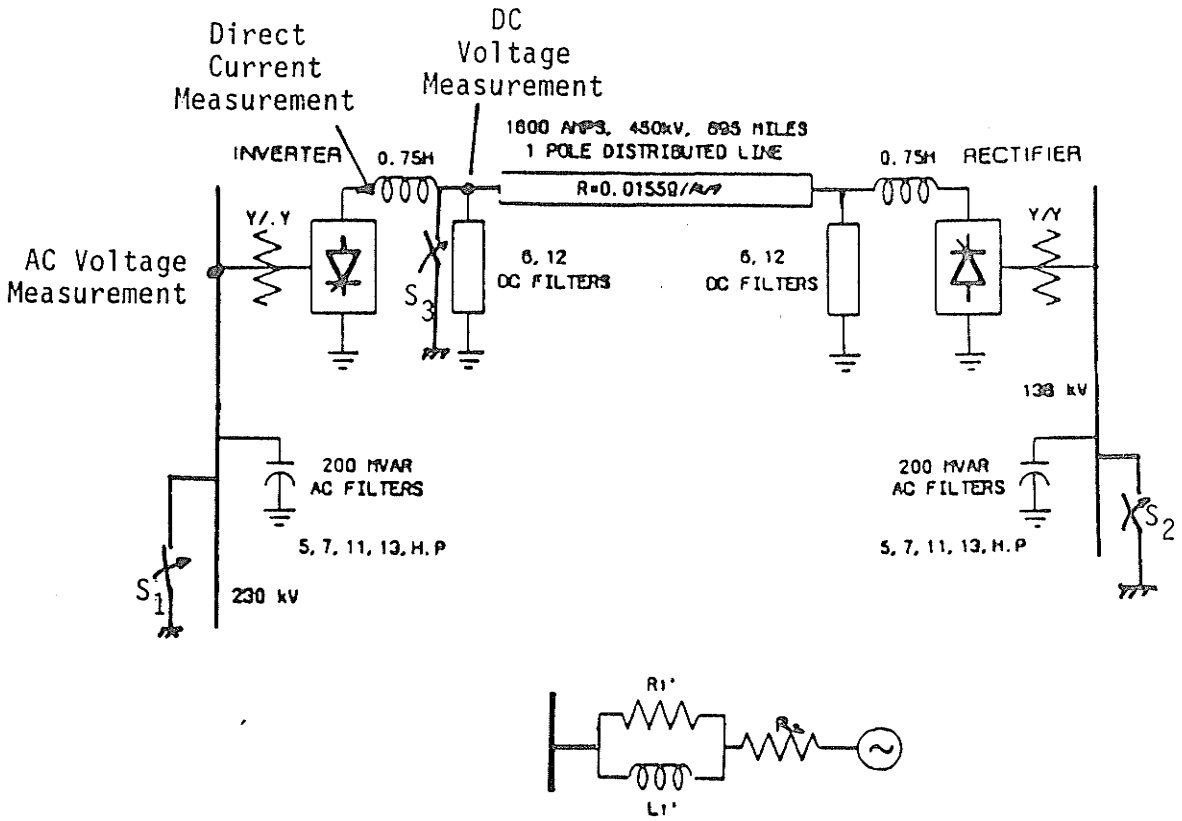
The point to point ac-dc-ac system shown in Figure 5.1 is modelled and simulated to investigate the system recovery from various faults by using different control schemes. The system with the following specifications at the inverter is modelled.

Rated active power = 810 MW

Current in the dc system = 1.8 kA

Length of dc transmission line = 895 km

The detailed representation of the ac system at the inverter/rectifier bus is shown in Figure 5.1 The ac system impedance (component values are given in Appendix B1) at the rectifier and the inverter is adjusted to provide short circuit ratios of 4.0 (rectifier) and 1.5 (inverter) with 138 kV at the rectifier ac bus and 230 kV at the inverter bus. These short circuit ratios are chosen to study the influence of a low short circuit ratio of the receiving ac system on the system recovery from



AC System Representation

S_1: Switch is closed to apply the ac faults at the inverter ac bus.
S_2: Switch is closed to apply the ac faults at the rectifier ac bus.
S_3: Switch is closed to apply the dc fault at the inverter terminal.

Figure 5.1 A HVDC System Used for Investigations

different faults for various control schemes. Further, each converter at the rectifier and the inverter terminal consists of:

i) Three series connected six-pulse valve groups per pole, each rated at 150 kV, 1.8 kA.

ii) Converter transformer with leakage reactance of 13% at its own base.

iii) Smoothing reactor of 0.75 H.

iv) DC filters tuned to 6th and 12th harmonics (component values are given in Appendix B1).

Each six-pulse converter at the rectifier and the inverter terminal is simulated using B6P110 subroutine [43]. In this subroutine, each valve is individually modelled with an equivalent R-C snubber circuit and phase lock oscillator, which is used to generate firing pulses for each valve [43]. Additionally, the converter transformers are modelled with saturation as shown in Figure 5.2. The saturation is accounted for by adding an additional flux dependent current to the current computed by the linear part of the model [44]. The V-I characteristics of the transformers are modelled with a knee point voltage of 1.2 p.u. and with an air core reactance double that of the leakage reactance.

The 895 km long dc transmission line separating the inverter and the rectifier stations is modelled as a frequency dependent, mutually coupled, distributed line with the following parameters.

Line resistance = 0.0155 ohms/km in the steady-state at 5.0 Hz

= 0.019 ohms/km in the steady-state at 90.0 Hz

Mode travelling time = 3.037 ms

Characteristic impedance = 300.00 ohms

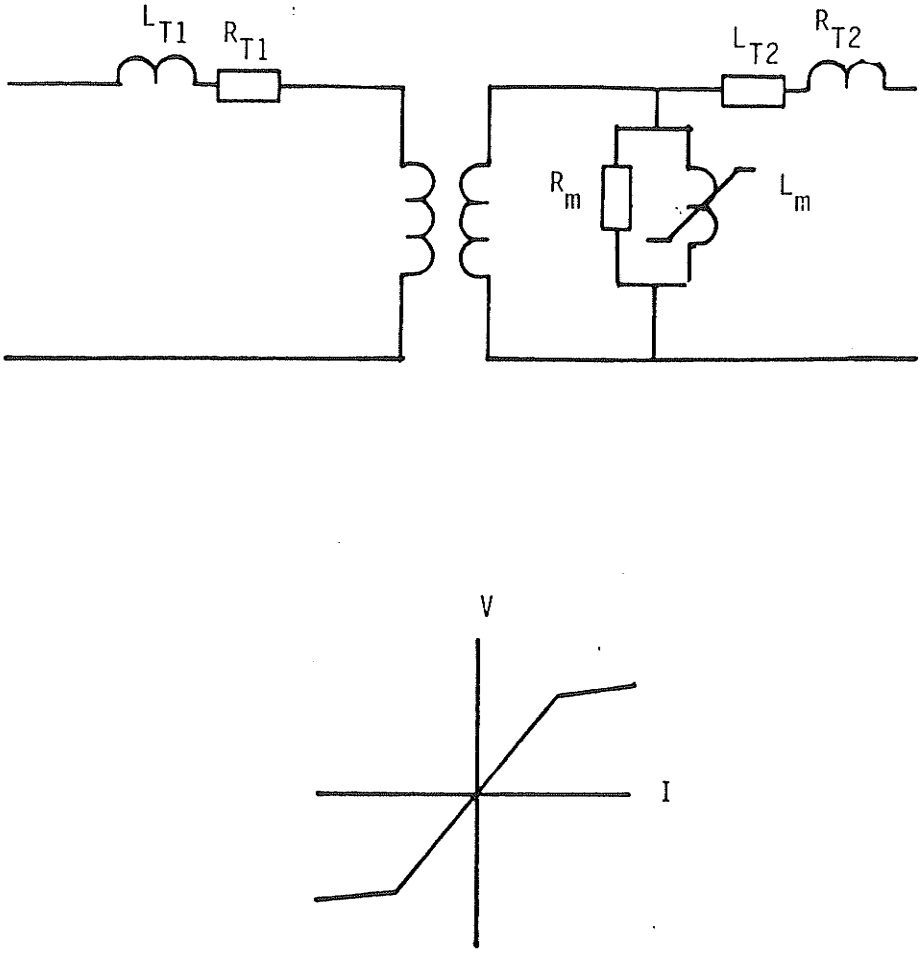


Figure 5.2 The Converter Transformer Model

The ac system feeding the converter bus at both ends is modelled as an infinite bus. The ac system impedances are represented by R-RL networks having the same damping at the fundamental and the second harmonic frequency. AC filters comprised of the 5th, 7th, 11th, 13th harmonics and high pass are connected at the converter buses as shown in Figure 5.3. The filter banks at each converter are divided into two equal sections to enable the switching out of 50% of filters after 6-cycles following the dc block for controlling dynamic overvoltages. The components values for ac filters are listed in Appendix B1.

5.3 DC SYSTEM CONTROLS

The dc system is assumed to be operating in the constant current mode without higher level controls. The rectifier operates on constant current control, whereas the inverter controls the voltage by operating at a constant extinction angle control under steady-state. The pole controller (POL1C6) determines the firing angle for the complete hvdc system by maintaining the direct current at a constant level [43]. The firing angle generated by the pole controller (Figure 5.4) is compared with the firing angle generated by the valve controller (VG1C18) [43] shown in Figure 5.5. The minimum of the two firing angles is selected to send the signal to the firing circuit.

The voltage dependent current limit is incorporated to modify the control characteristics as shown in Figure 5.6 in order to help the system recover from the faults by reducing the direct current order for low operating voltages. If the dc voltage at the rectifier terminal falls below V_{min} for more than 20 msecs, the VDCL is activated and, hence, the dc voltage at the rectifier end is limited by the current

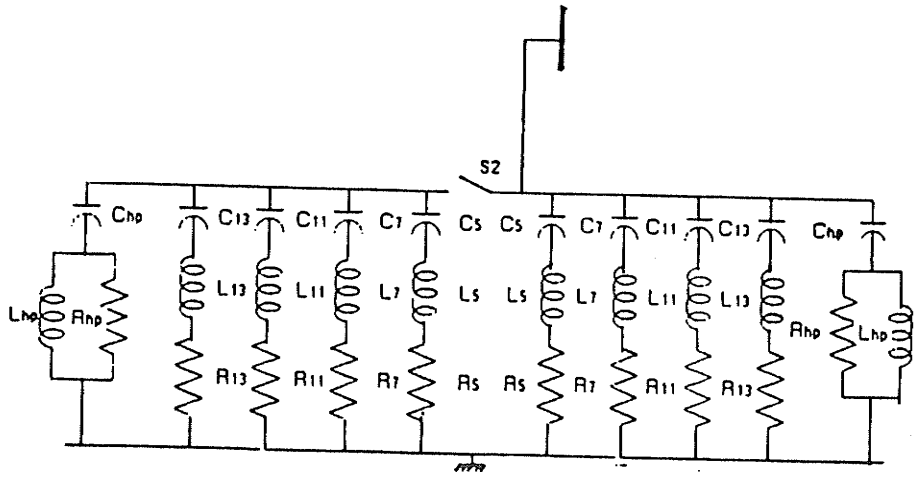


Figure 5.3 AC Filter Representation

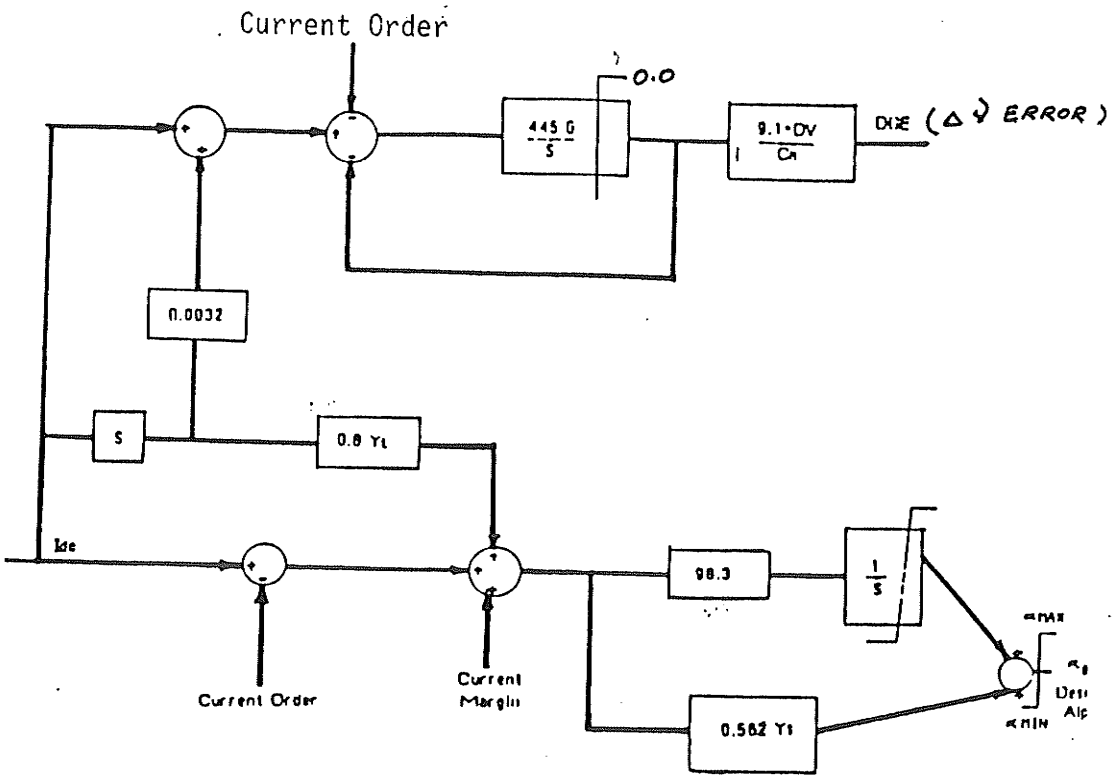


Figure 5.4 Block Diagram for the Pole Control Group [43]

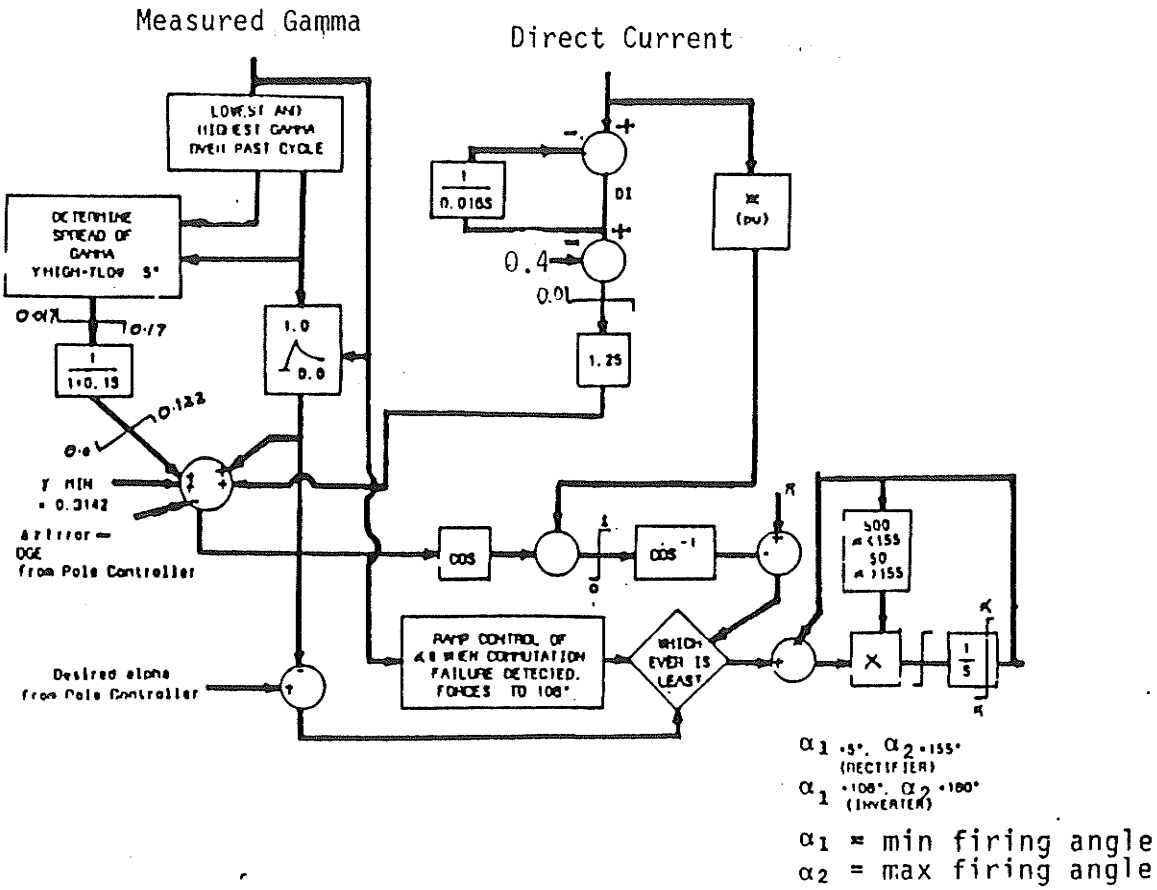
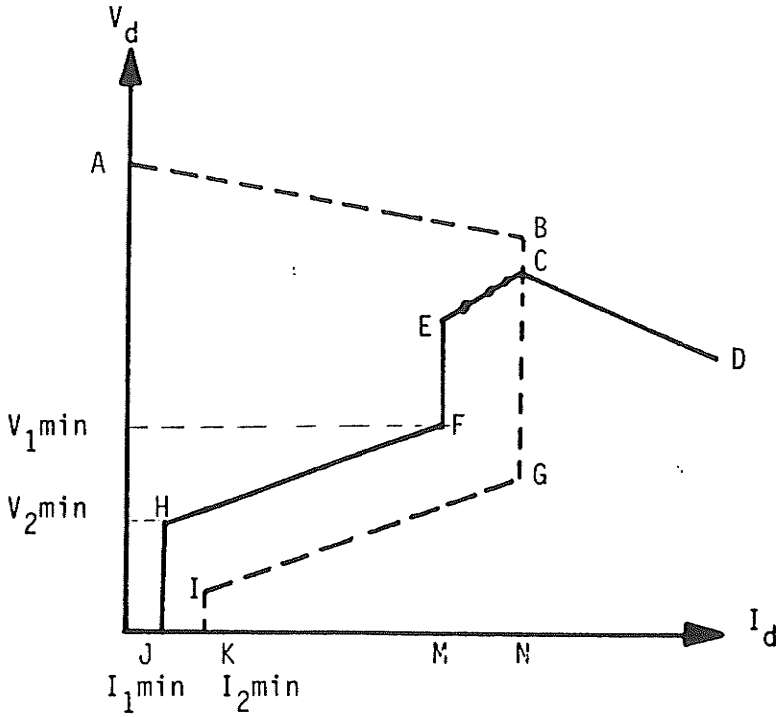


Figure 5.5 Block Diagram for the Valve Control Group [43]



A-B: α_{min} Control

C-D: γ_{min} Control

EC: β Control

JH, EF & EM: Current Control for the Inverter

IK, BC & GN: Current Control for the Rectifier

FH & GI: VDCL

Figure 5.6 Control Characteristics of the HVDC System

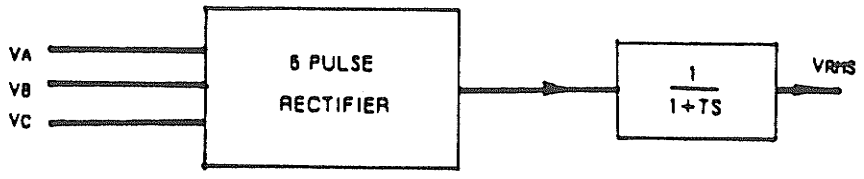


Figure 5.7 Three Phase RMS Voltage Measurement

order to I_{min}. This current order is maintained until the dc voltage on the rectifier is less than V_{min}. Once the rectifier voltage is greater than V_{min}, the current order is ramped to 1.0 p.u. The modified control characteristics are shown in Figure 5.5. The current is ramped from 0.3 to 1.0 p.u. in T_{vdcl} (70 ms). The commutation ramp is activated when commutation failure is detected. The current order at the inverter terminal is normally forced down to I_{min} and maintained there as long as the commutation failure persists. Once the inverter is free of commutation failures, the current order is ramped to the steady-state value. The duration of this ramp is chosen to be 150 ms.

5.4 INTERFACING OF VARIOUS CONTROL MODES WITH EMTDC

The following control modes are realized by writing computer programs in the FORTRAN programming language.

a) AC Voltage Control: The measurement of effective three phase voltage is performed by using a six-pulse diode bridge. The rectified voltage is passed through a low pass, first order filter network to model the delay introduced by the measurement circuit and filters as shown in Figure 5.8. This filtered signal is subtracted from the reference signal (1.0 p.u. voltage) to generate the error signal. The error signal is processed by the controller to generate the firing angle. The firing angle is limited between 108° and 180° [42]. The limiter circuit is realized by two IF statements.

b) DC Voltage Control: The dc voltage is measured before the smoothing reactor at the inverter terminal. The measured signal is passed through a delay circuit to simulate the measurement delay. The delay circuit is realized as follows.

$$\text{Delay Circuit} \equiv \left(\frac{1}{1 + T_d S}\right)$$

where T_d = delay in secs; S = Laplace operator.

The measured signal is compared with the reference signal to generate the error signal. The error signal is used by the controller to generate the firing angle.

c) Power Factor Control: The power factor at the inverter terminal has been calculated by the following relationship [1] and passed through delay circuits to simulate the measurement delay.

$$\cos\phi = \frac{V_{di}}{K_i V} \qquad (5.1)$$

where $K_i V$ = no load dc voltage

V_{di} = dc voltage at the inverter terminal

During faults, it is possible for 'V' to be zero. Hence, equation (5.1) causes an overflow. This problem has been overcome by setting the power factor at 1.0 for the duration of the disturbance. The power factor is frozen to 1.0 rather than a steady-state value to provide appropriate direction to the firing angle after the clearance of the fault. The error signal is generated by subtracting the measured signal and processing similar

to the above-mentioned control schemes. This control is realized without a tap changer control.

d) Reactive Current Control: The reactive current at the inverter terminal can be calculated by using equation (5.2).

$$I_q = K_i I_d \sin\phi \tag{5.2}$$

where $\sin\phi = \sqrt{1 - \cos\phi^2}$

$\cos\phi$ = power factor

I_q = reactive current

This calculated signal is passed through a simple delay circuit to simulate the measurement delay. The firing angle generated by this scheme is similar to that obtained from the ac voltage control.

e) Reactive Power Control: The reactive power absorbed at the inverter terminal is calculated by using equation (5.3).

$$Q = VI_q \tag{5.3}$$

where V = rms voltage for three phase ac voltage

I_q = reactive current

The measurement of 'V' is carried out exactly as mentioned for the ac voltage control. The 'I_q' is calculated by using equation (5.2). The calculated reactive power is passed through a delay network to simulate the measurement delay. The error is calculated by subtracting measured reactive power from the reference value of the reactive power. The firing angle is generated in a fashion similar to that described for the ac voltage control.

The functional block diagram to realize various control modes at the inverter terminal is shown in Figure 5.8. The measures to evaluate the performance of all control modes at the inverter terminal, controller design for each control scheme, and the system response to critical faults are discussed in subsequent sections.

5.5 MEASURES FOR DETERMINING THE EFFECTIVENESS OF VARIOUS CONTROL SCHEMES

A comparison of various control schemes is carried out on the basis of the measures discussed in Chapter IV (Section 4.4). In addition, the dynamic overvoltages (DOV) are considered.

Dynamic Overvoltages (DOV): The rms value of three phase ac voltage is measured to indicate the dynamic overvoltages. The effectiveness of various controls is measured on the basis of both the duration and magnitude of the dynamic overvoltages. The duration of the dynamic overvoltage is defined as the time elapsed in milliseconds for the magnitude of the overvoltages to remain at or above 1.1 p.u. [45] following a disturbance.

5.6 CONTROLLER DESIGN FOR VARIOUS SCHEMES

The following controller configuration is used for various control schemes at the inverter terminal of the hvdc system.

$$G_c(S) = k_c \left[\frac{\tau_c S + 1}{S}\right] \frac{(1 + T_a S)}{(1 + T_b S)} \qquad (5.4)$$

where $G_c(S)$ = controller transfer function

k_c = controller gain

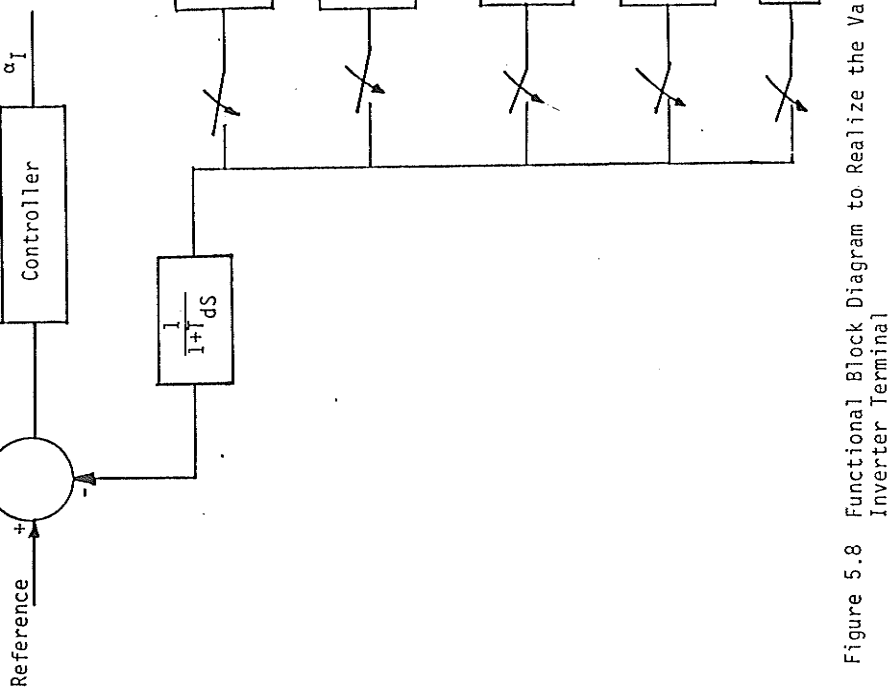


Figure 5.8 Functional Block Diagram to Realize the Various Control Schemes at the Inverter Terminal

τ_c = controller time constant

T_a, T_b = time constant of the lead-lag network

The controller optimization has also been carried out for the evaluation of the effectiveness of all control schemes. The controller for each control scheme is optimized by observing the system recovery for a given disturbance over a range of controller parameters. The selection of the controller parameters is performed on the basis of the optimum system recovery from the disturbance. The procedure of optimization is repeated for all control schemes for various faults. The optimized controller parameters for various faults are given in Appendix B2. However, the optimization of various control schemes is valid only for a given system configuration. Once the system configuration changes, the optimization of the controller parameters is to be carried out again for all control schemes and various faults as indicated by the small signal analysis in Chapter II.

5.7 SYSTEM RECOVERY FOR SOME FAULTS WITH VARIOUS CONTROL SCHEMES AT THE INVERTER TERMINAL

Extinction angle control operates best during the steady state because it minimizes harmonic generation and reactive power consumption. The suggestion of totally replacing [9] the conventional controls by one of the new control schemes is undesirable because these alternate control modes operate at higher extinction angle, which results in higher harmonic generation, reactive power demand and losses. Subsequently, the total cost of the station increases.

A better solution [8] is to introduce the new control just after the disturbance for a few cycles to limit overvoltages and minimize the

possibility of potential commutation failure. This technique has the merit that during the steady-state condition the system operates with minimum reactive power demand.

The concept used in this chapter to evaluate the effectiveness of various control modes is to replace the conventional control by one of the control schemes (b-f) for 300 ms just after a fault and then revert back to the original conventional control. This concept of replacing conventional control by ac voltage control has been reported in reference [8]. However, this latter study is limited only to three phase faults at the inverter ac bus. In this chapter the effectiveness of the ac voltage control is studied for some other faults. In addition, to complete the literature, the effectiveness of new control schemes like the dc voltage control, the reactive power control, and the power factor are also investigated.

The power factor control reported in reference [11] is not a real power factor control because it needs assistance from the tap changer control, which makes the power factor control response very slow. A pure power factor control, discussed in Section 5.4, which does not require the assistance of the tap changer is used for comparison.

The reactive current control [9] and the reactive power control have the same characteristics in steady-state. However, during transients, the ac bus voltage is not 1.0 p.u. and the characteristics of the reactive power control become different from the reactive current control. Hence, the investigations are also carried out for the reactive power control.

Effectiveness is determined in terms of the magnitude and duration of the dynamic overvoltages, dc power recovery time, and the peak overvoltages, which are discussed next.

The following faults are applied to the system to compare various control schemes mentioned in Section 5.4 because the previous investigations seem to show these faults to be critical.

a) Three phase to ground fault of 100 ms duration at the inverter and the rectifier ac bus.

b) Single phase to ground fault of 100 ms duration at the inverter and the rectifier.

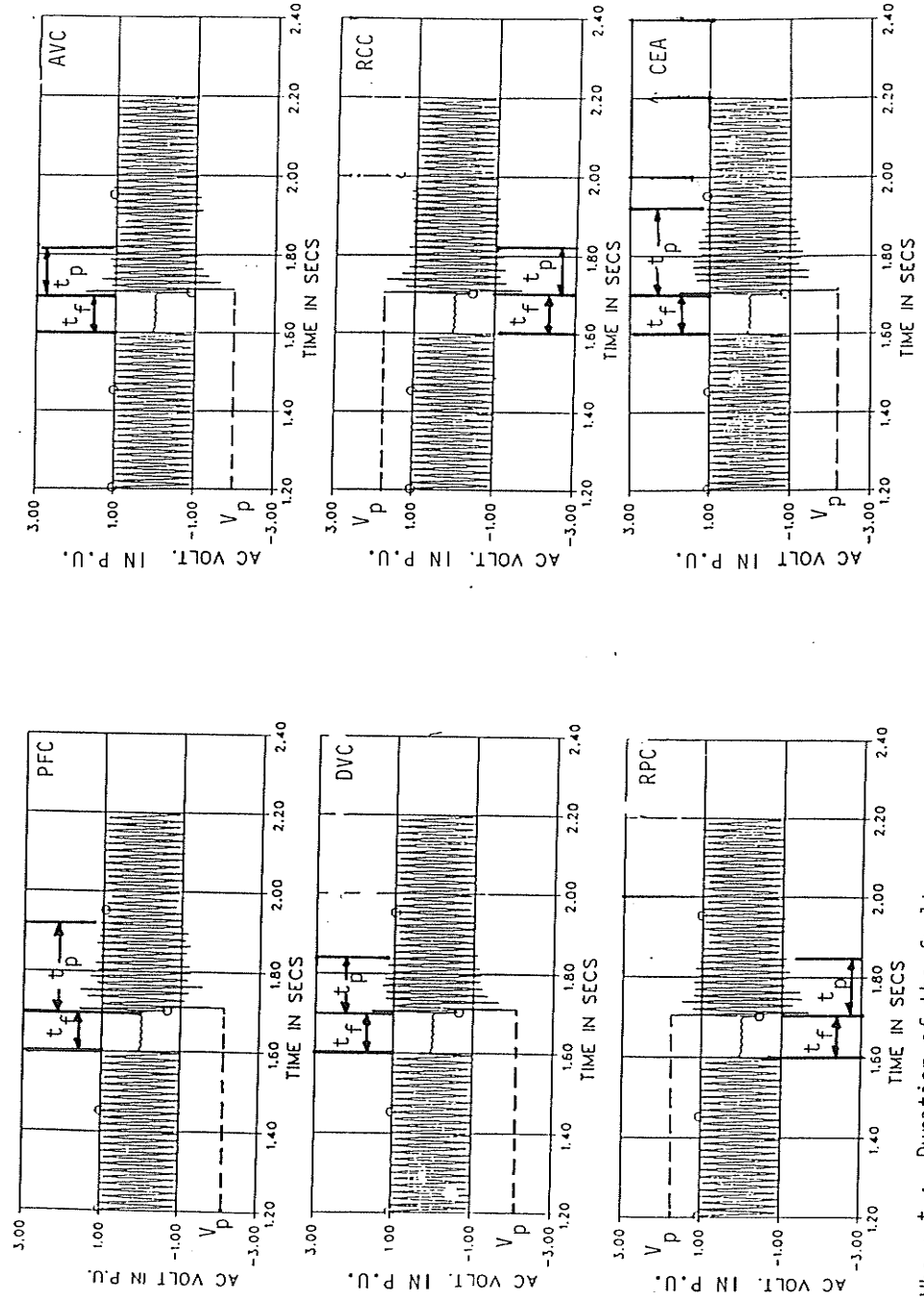
c) DC line fault of 200 ms duration at the inverter.

System Response for Various Faults

The system response for various control schemes is studied by time domain simulation on the EMTDC digital program. The results are summarized below.

a) Three Phase Fault on the Inverter Bus: The following variables are observed to determine the effectiveness of each control scheme.

   i) Instantaneous AC Voltage (Figure 5.9): The duration (200 ms) and magnitude of overvoltages (2 p.u.) are the same for the power factor and the conventional control. The ac voltage control, the dc voltage control, reactive current control, and reactive power control behave similarly. For these four control schemes, the duration of overvoltage is shorter by 5 cycles and the magnitude of peaks is smaller by 20% for the last 3 cycles in comparison to the conventional control.



Where t_f: Duration of the fault

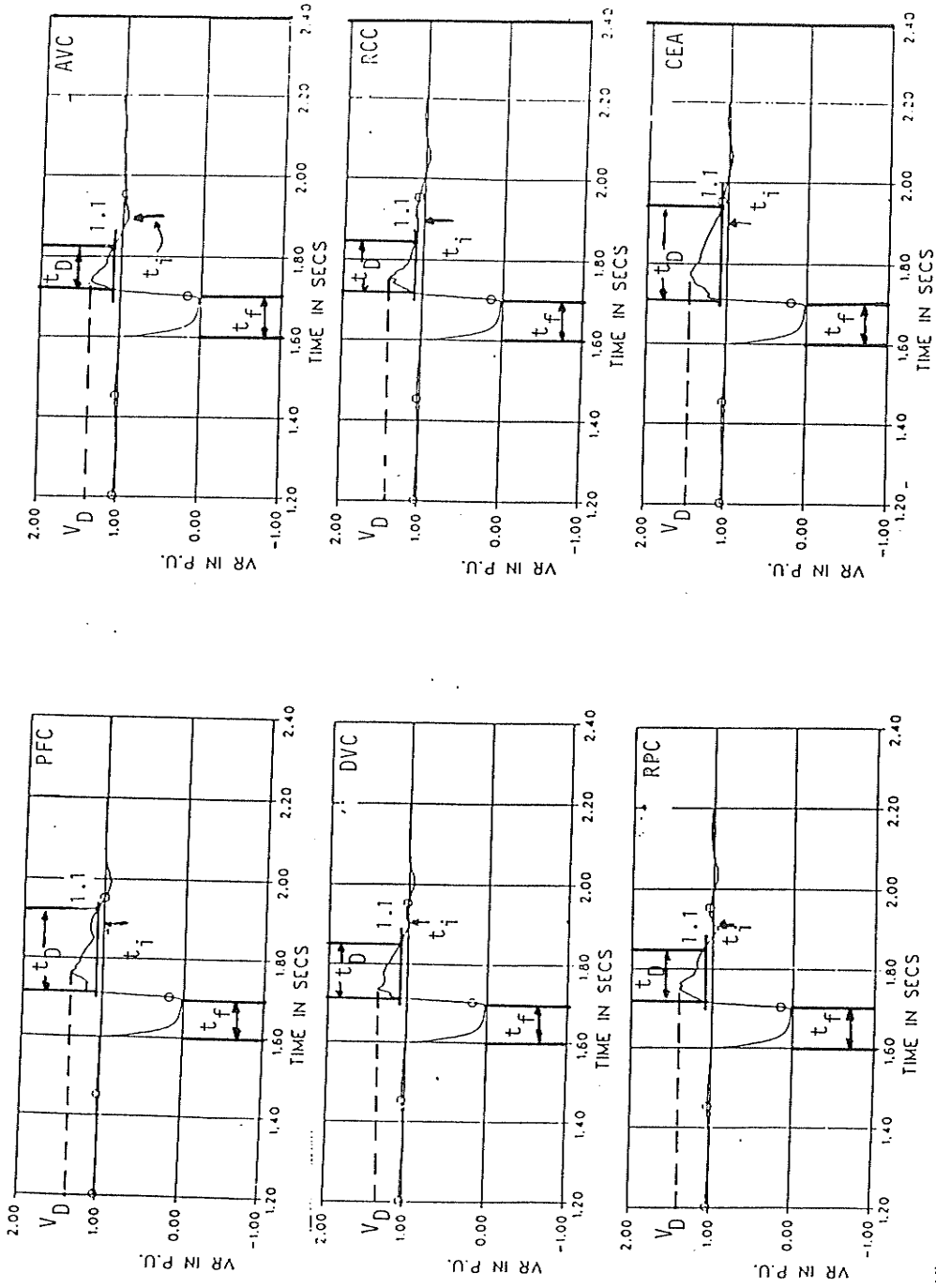
t_p: Duration of the peak instantaneous overvoltages

Figure 5.9 Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Inverter Bus

ii) Dynamic Overvoltage (DOV) (Figure 5.10): The most effective control to minimize DOV is the ac voltage control because it produces DOV for only 110 ms. The DOV characteristics for the dc voltage control and the reactive power control schemes are comparable in duration and magnitude (Table 5.1). The duration of DOV for the reactive current control is almost the same as the conventional or the power factor control. However, the relative magnitude if DOV is less by 10% in the case of the reactive current control in comparison with the conventional control.

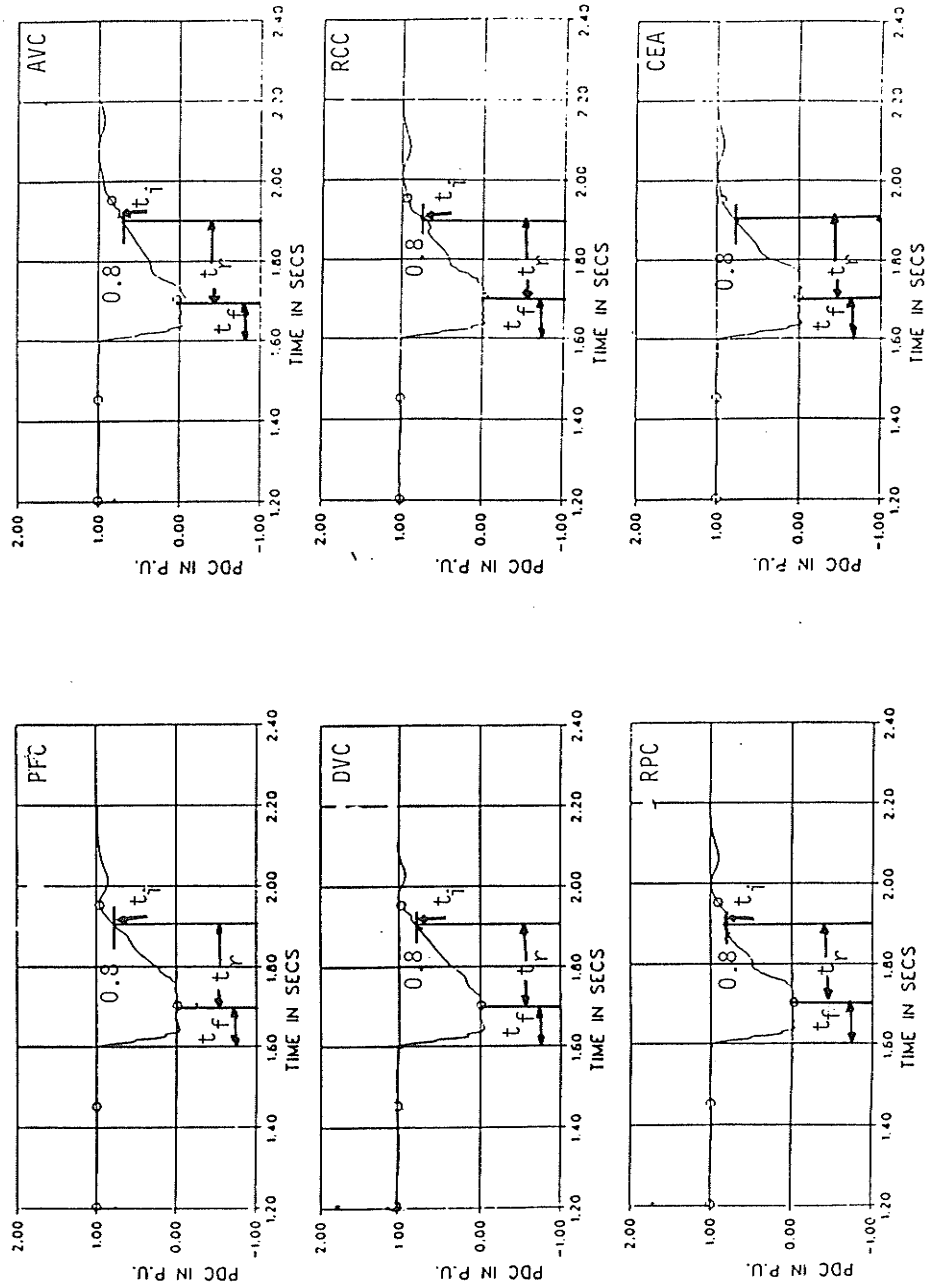
iii) DC Power Recovery (Figure 5.11): The duration of the dc power recovery is about 210 ms for all control modes.

Similarly, results are obtained for other faults and the traces of the above-mentioned variables are presented in Appendix B3. A summary of the durations and the magnitudes of overvoltages and the recovery time for the dc power for all faults is presented in Table 5.1(a) to Table 5.1(d).



Where t_f: Duration of fault
t_D: Duration of the dynamic overvoltage
V_D: Magnitude of the DOV

Figure 5.10 Three Phase RMS Voltage Response for the Three Phase to Ground Fault at the Inverter Bus



Where t_i: Time at which system is reverted to conventional control.
t_r: DC power recovery time.
t_f: Duration of the fault.

Figure 5.11 DC Power Recovery from the Three Phase to Ground Fault at the Inverter Bus

Table 5.1(a) System Response for the Three Phase to Ground Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
PFC	2.00	210	1.40	210	210
DVC	2.00	142	1.35	142	210
RPC	1.80	136	1.40	136	210
AVC	2.00	110	1.35	110	210
RCC	1.80	122	1.40	122	210
CEA	2.00	230	1.48	230	210

Table 5.1(b) System Response for the Single Phase to Ground Fault at the Inverter AC Bus.

Control Scheme	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
PFC	1.45	71	1.40	71	140
DVC	1.83	80	1.33	80	140
RPC	1.66	122	1.33	122	140
AVC	1.83	52	1.20	52	140
RCC	1.60	135	1.26	135	140
CEA	1.85	135	1.33	135	140

Table 5.1(c) System Response for the DC Line Fault at the Inverter Terminal.

Control Scheme	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
PFC	1.5	123	1.5	126	115
DVC	1.5	84	1.5	84	115
RPC	1.5	122	1.5	122	115
AVC	1.5	65	1.5	65	115
RCC	1.5	125	1.5	125	115
CEA	1.5	110	1.5	110	115

Table 5.1(d) System Response for the Three Phase to Ground Fault at the Rectifier AC Bus.

Control Scheme	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
PFC	1.41	70	1.5	70	132
DVC	1.41	100	1.5	100	132
RPC	1.5	128	1.5	128	132
AVC	1.5	55	1.5	55	132
RCC	1.5	128	1.5	128	132
CEA	1.5	85	1.5	85	132

5.8 DISCUSSION

The evaluation of the effectiveness of various control schemes at the inverter terminal of the hvdc system feeding to a relatively weak ac system has been carried out. The effectiveness of various control schemes is determined on the basis of system recovery from different ac and dc faults in terms of peak instantaneous overvoltages, dynamic overvoltages (magnitude and duration), and dc power recovery time. The concept used for determining the effectiveness of various control schemes is that each control scheme is introduced for 300 ms from the instant of the fault and thereafter the inverter operation is reverted to the conventional control. The concept is used because it has the advantages of the minimum reactive power demand and minimal harmonic generation during steady-state, and it minimizes the overvoltages following the faults. It is also found that switching from one control to another without producing significant voltage and power oscillation is possible (Figure 5.9 through Figure 5.11).

It is observed that when appropriately optimized controllers are used, similar power recovery is achieved (Table 5.1(a) through Table 5.1(d)). However, the dynamic overvoltage profile differs, as seen in the computed results shown in Table 5.1(a) through Table 5.1(d). Further, it is observed from Table 5.1(a) through 5.1(d) that the overvoltages can be minimized by introducing the dc or ac voltage control for 300 ms just after the fault.

5.9 CONCLUSIONS

The evaluation of all control schemes at the inverter terminal of the weak ac system has been performed. The following important conclusions can be drawn:

i) The same dc power recovery time can be achieved by proper optimization of the controller parameters for every control scheme.

ii) Dynamic overvoltages can be minimized by introducing either the dc voltage control or the ac voltage control for 300 ms immediately after the disturbance (Table 5.1(a) through Table 5.1(d)). The dc voltage control should be preferred over the ac voltage control because it minimizes the complexity of the control circuit by eliminating the need of a bridge rectifier and three ac voltage measurement circuits. In addition, there is no need for the 6th harmonic filter for the dc control because it already exists in the system.

iii) The dynamic overvoltage response is different for various control schemes. However, it is believed that economical devices like a metal oxide arrester (MOV) can be used to improve the DOV characteristics. Hence, the proper optimization of the conventional control scheme is sufficient to obtain a desirable system response and there is no need to replace the existing conventional control.

CHAPTER VI

INFLUENCE OF THE SENDING END SHORT CIRCUIT RATIO ON THE PERFORMANCE OF HVDC CONTROLS

6.1 INTRODUCTION

This chapter deals with the study for determining the influence of the sending ac system short circuit ratio on the performance of the controls of a hvdc system. This study is performed to investigate the system response to a step change in direct current and the system recovery from various faults. Several authors [46-49] have investigated the influence of system performance having a low short circuit ratio at the receiving end. However, the influence of lowering the short circuit ratio of the sending end ac system has not been studied in detail. To investigate the influence of the sending ac system short circuit ratio on the performance of the hvdc system, the following three cases are undertaken.

Case (a) A weak receiving and strong sending ac system.

Case (b) A weak receiving and weak sending ac system.

Case (c) A strong receiving and weak sending ac system.

The ac/dc/ac system is represented as mentioned in Chapter V. The following studies are carried out to evaluate the system performance for the conventional control.

Direct Current Step-Response: This study is performed to evaluate the system stability and to verify some of the results reported in Chapter II.

System Recovery: Some of the faults discussed in Chapter IV are applied to study the system recovery for the three cases aforementioned. The comparison of system recovery for all three cases is performed in terms of the instantaneous peak overvoltages, dynamic overvoltages and dc power recovery time.

6.2 DIRECT CURRENT STEP RESPONSE OF THE HVDC SYSTEM

The step change in the direct current is simulated for the three cases mentioned earlier by raising the current reference from 1.0 p.u. to 1.1 p.u.

DC Power Recovery: The step change in the direct current for case (a) causes oscillation in the dc power and it takes about 300 ms (Figure 6.1) to settle down to the steady-state value. For case (b) the dc power reaches to its steady-state value in 170 ms. This indicates that by lowering the short circuit ratio of the sending end improves the system response. Further, Figure 6.3 reveals for case (c) that the dc power takes 80 ms to settle down to its steady-state value, which shows the improvement in system response.

RMS Voltage Response: The rms voltage of the three phase system is measured to determine the influence of the sending ac system short circuit ratio on the dynamic overvoltages. It is observed from Figures 6.1 and 6.2 that the fluctuations in the rms voltage are almost eliminated by reducing the short circuit ratio of the sending ac system. However, further improvement in the rms voltage response is observed from Figure 6.3, which indicates that an increase in short circuit ratio of the receiving ac system also improves the voltage response.

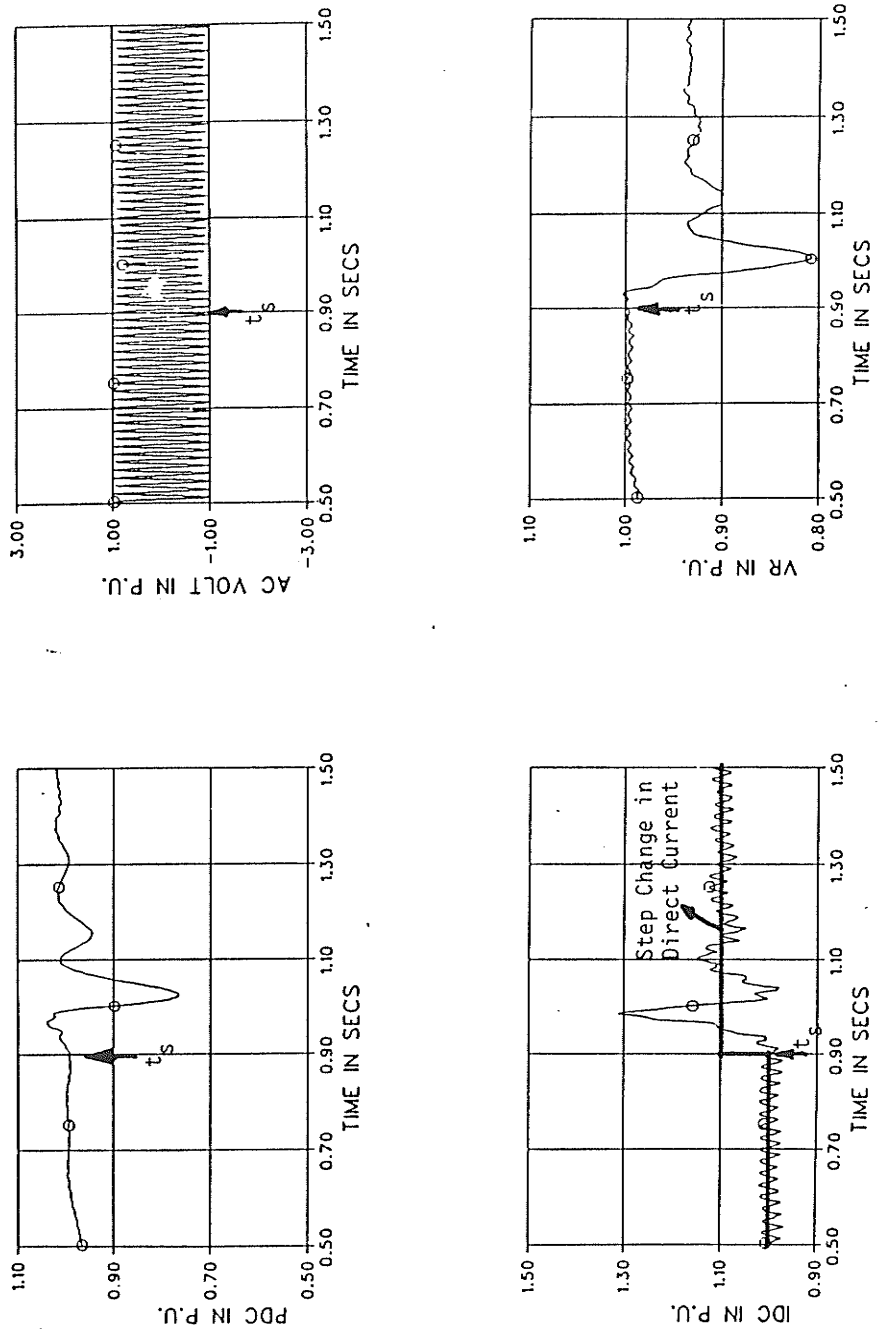


Figure 6.1 Direct Current Step Response for a Weak Receiving and Strong Sending AC System (Case (a))

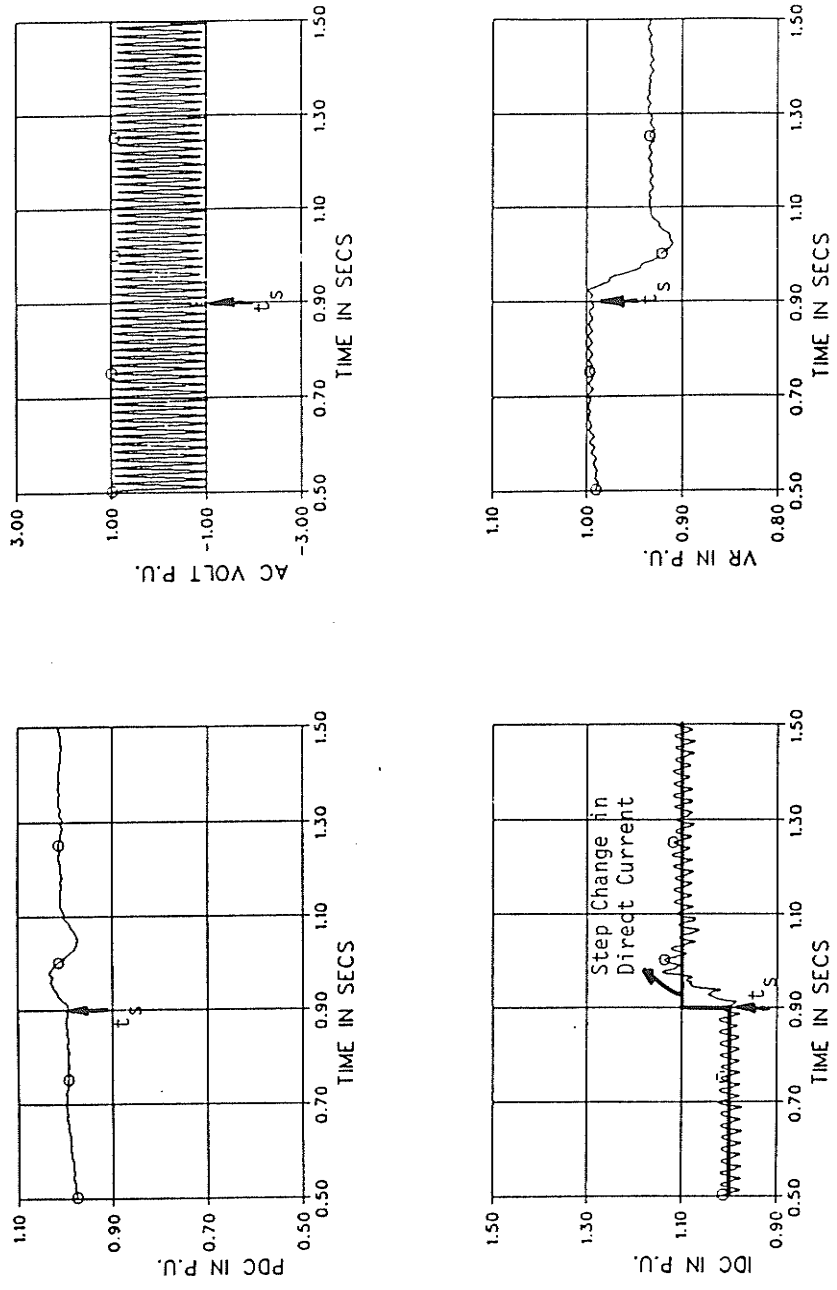


Figure 6.2 Direct Current Step Response for a Weak Receiving and Weak Sending AC System (Case (b))

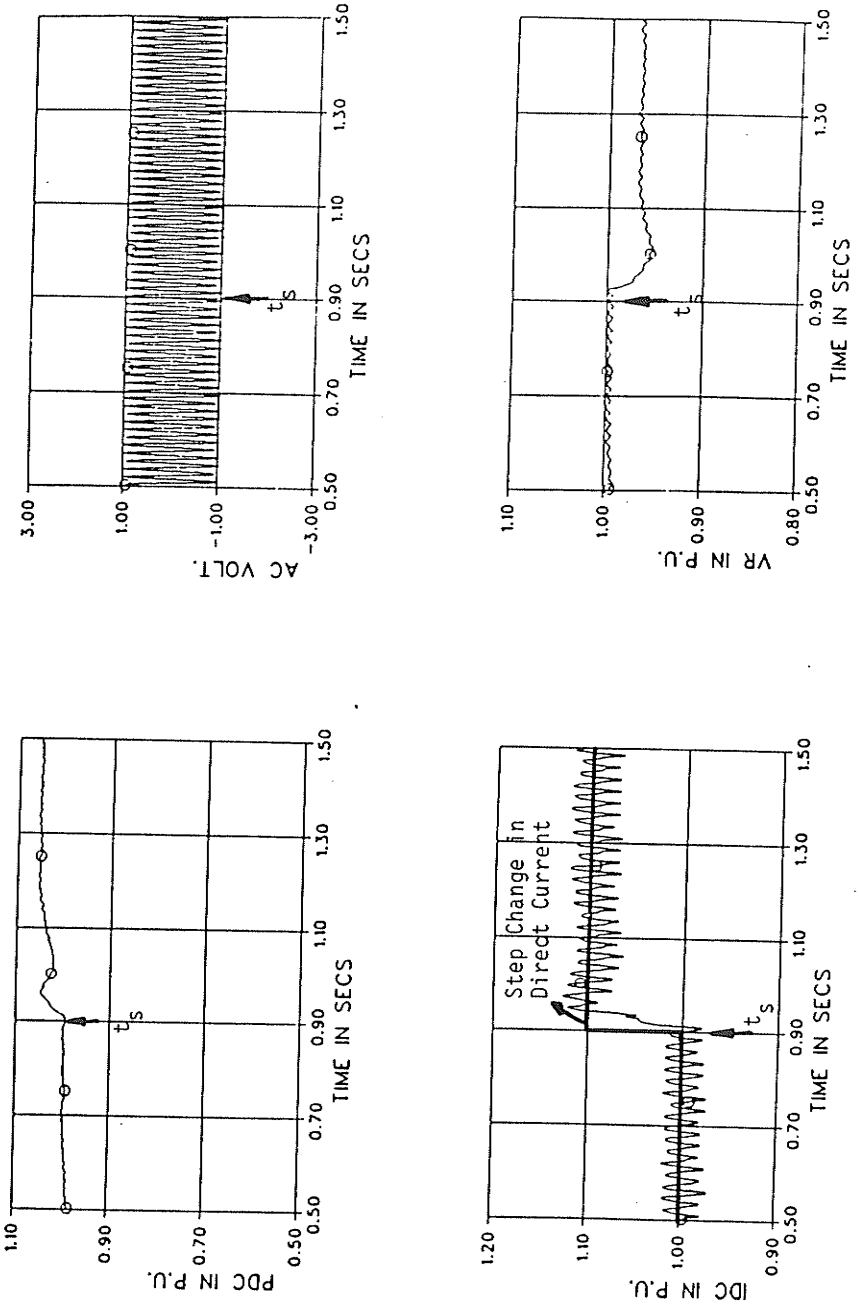


Figure 6.3 Direct Current Step Response for a Strong Receiving and Weak Sending AC System (Case (c))

Direct Current Response: A 18% overshoot is observed for case (a) only (Figure 6.1). The settling time for case (b) and case (c) is almost the same (Figures 6.2 and 6.3) and is shorter by 86 ms in comparison to case (a). This also indicates that lowering the short circuit ratio of the sending ac system or raising the short circuit ratio of the receiving ac system helps to improve the system response.

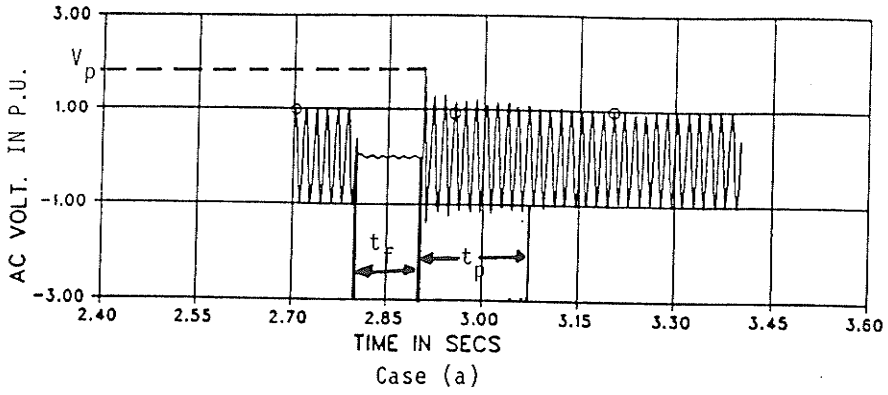
6.3 SYSTEM RECOVERY FROM VARIOUS FAULTS

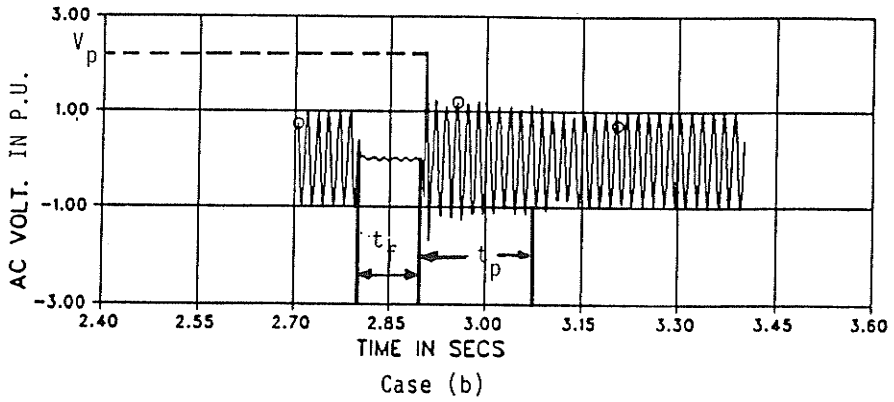
The three phase to ground fault, the single phase to ground fault, and dc line fault are applied at the inverter terminal to determine the influence of short circuit ratio of both the rectifier and the inverter ac systems on the system recovery. The system response to these faults is discussed next.

Three Phase to Ground Fault: The following observations can be made from Figure 6.4 through Figure 6.6 regarding system recovery from the fault.

a) The peak instantaneous ac overvoltage in the first cycle in phase-A shows a higher overshoot in cases (b) and (c) than case (a). However, the duration of the overvoltage is the lowest in case (c), while case (a) and case (b) have the same duration (Figure 6.4).

b) The rms voltage at the inverter bus indicates the lowest under and overvoltages for case (c). A comparison of case (a) with (b) shows that the overvoltages in Figure 6.5 are less in case (b) by 10 ms than case (a). However, the magnitude and duration of the undervoltages in case (b) are more than those in case (a). This





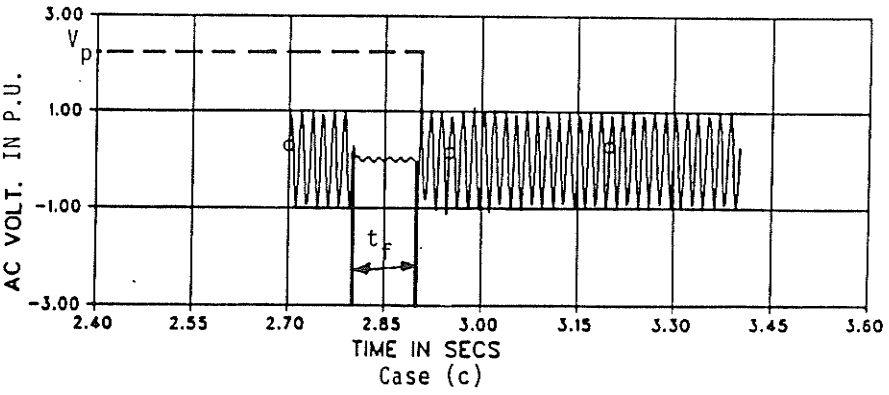
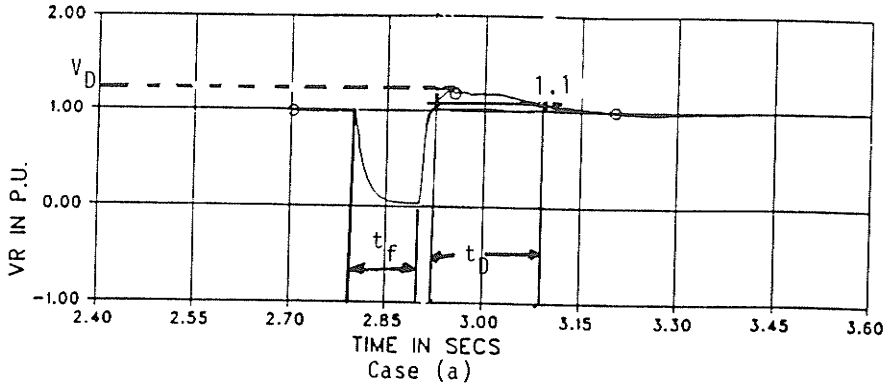
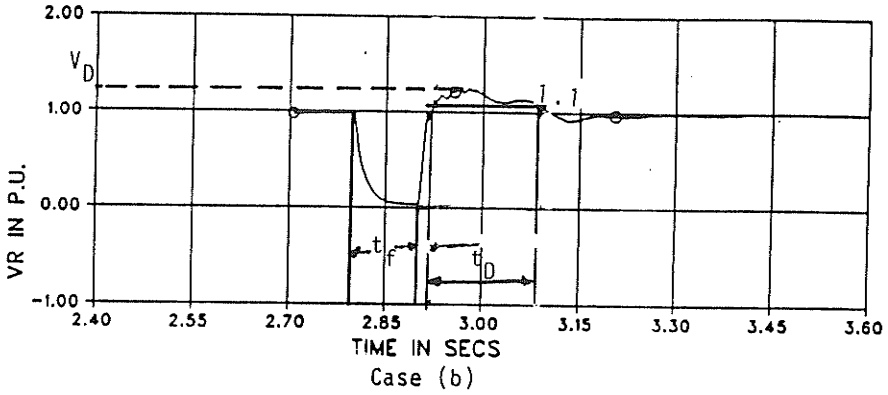


Figure 6.4 Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Inverter Bus





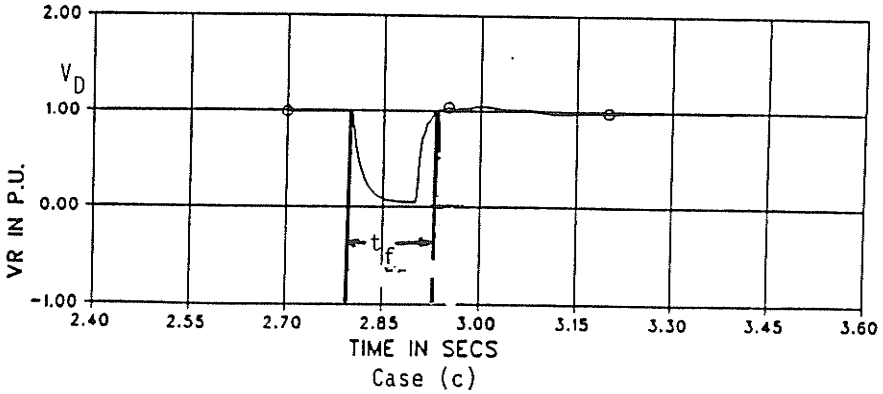
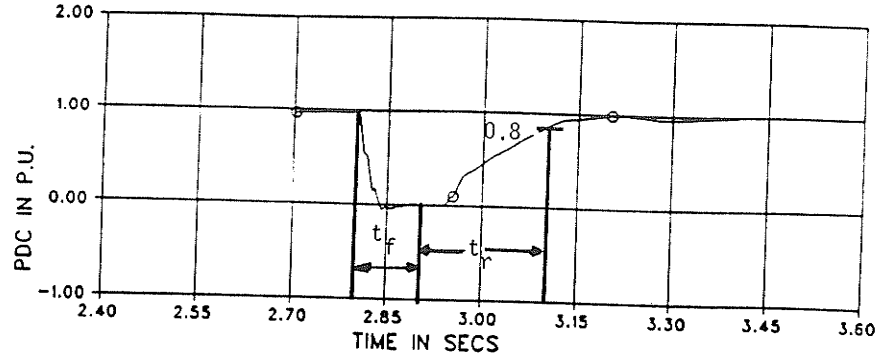
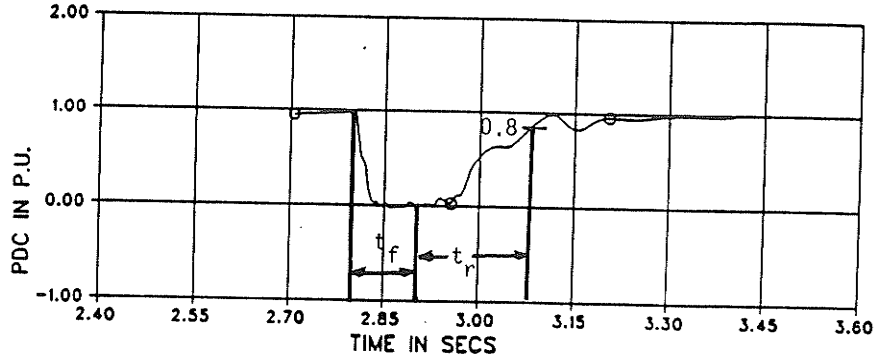


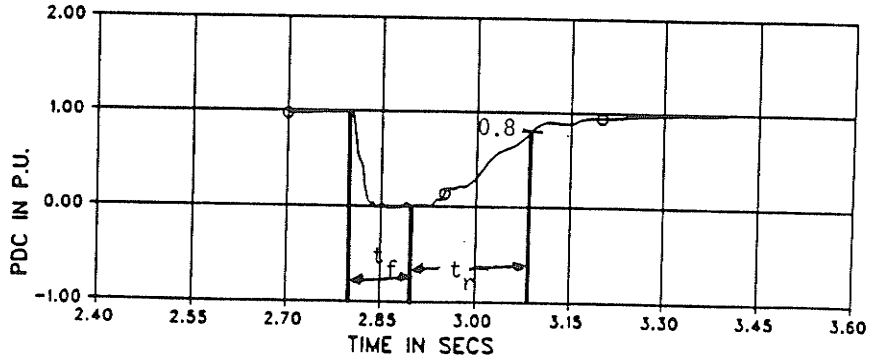
Figure 6.5 Three Phase RMS Voltage Response for the Three Phase to Ground Fault at the Inverter Terminal



Case (a)



Case (b)



Case (c)

Figure 6.6 DC Power Recovery from the Three Phase to Ground Fault at the Inverter Bus

indicates that the reactive power demand is higher for a few cycles following the fault in case (b) (Figure 6.5).

c) The dc power recovery time in case (b) and case (c) is almost 180 ms and, at the same time, it is 210 ms for case (a). Hence, the reduction in short circuit ratio of the sending ac system may decrease the dc power recovery time.

The traces of the peak instantaneous overvoltages, the dynamic overvoltages and the dc power recovery for the single phase to ground fault and the dc fault at the inverter terminal are presented in Appendix C. The results for the system recovery for various faults are summarized in Table 6.1 to Table 6.3

6.4 DISCUSSION

The influence of both the rectifier and inverter ac systems' short circuit ratios have been studied by investigating the direct current step response and the system recovery from various faults for the same controller settings. It has been determined that the reduction in the short circuit ratio of the sending ac system improves the direct current step response. This may be because the rise in the direct current is controlled by the sending ac system impedance.

The study of system recovery from various faults indicates that the dc power recovery time is reduced (Table 6.1 and Table 6.3) for the balanced faults by either reducing the short circuit ratio of the sending ac system or increasing the short circuit ratio of the receiving ac system. However, for the single phase to ground fault at the inverter ac system, the best dc power recovery is observed for case (a)

Table 6.1 System Response for the Three Phase to Ground Fault at the Inverter AC Bus.

Cases	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
Case (a)	1.88	170	1.25	170	200.0
Case (b)	2.13	180	1.25	180	169.0
Case (c)	2.10	0	1.10	0	178.0

Table 6.2 System Response for the Single Phase to Ground Fault at the Inverter AC Bus.

Cases	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
Case (a)	1.88	70	1.2	70	100.0
Case (b)	2.00	130	1.2	130	131.3
Case (c)	2.00	0	1.06	0	150.0

Table 6.3 System Response for the DC Line Fault at the Inverter Terminal.

Cases	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
Case (a)	1.25	100	1.2	100	103.0
Case (b)	1.25	100	1.2	100	94.0
Case (c)	1.07	60	1.12	60	85.0

(Table 6.2). This may be because asymmetrical faults cause higher harmonics [50-51]. These harmonics may influence the dc power recovery.

6.5 CONCLUSIONS

The study reported here has investigated the influence of the short circuit ratio of the sending ac system on the performance of the hvdc controls. The following conclusions can be drawn from the investigations.

i) A reduction in the short circuit ratio of the sending ac system improves the system damping. This is because the rise in direct current is controlled by the sending ac system impedance.

ii) The increase in the short circuit ratio of the receiving ac system improves the system stability.

iii) The system recovery improves for symmetrical faults as the sending ac system short circuit ratio decreases and/or the receiving ac system short circuit ratio increases.

iv) For asymmetrical faults, the system recovery worsens as the sending ac system becomes weaker or the receiving ac system becomes stronger. This trend can be due to the influence of non-characteristic harmonics generated due to the asymmetry of faults during the system recovery.

CHAPTER VII

APPLICATION OF RECENT CONTROLLER CONFIGURATIONS TO A HVDC SYSTEM

7.1 INTRODUCTION

The most commonly used controller configuration in a hvdc system is the proportional-integral (P-I) controller. This scheme is used because it has the following advantages.

a) The steady-state error is zero because of the integral term [52]. Hence, the system response can match the reference signal accurately [52].

b) It is not necessary to use the higher proportional gains required in the proportional-only controller [52].

c) Proportional-integral control has been found to be quite robust and satisfactory in a variety of applications and schemes [52].

However, the P-I controller scheme has the following drawbacks.

a) Higher gains are needed to be used for a fast system response. Hence, P-I control causes a relatively higher overshoot and longer transient duration [53].

b) The system can be designed without overshoot, but then the response to a load disturbance becomes very slow [53].

Recently, a new controller configuration called the I-P controller has been suggested for dc motor drives [53-54]. It has been claimed that the I-P controller allows a faster system response without a high overshoot [53-54]. The above-mentioned advantage of the I-P controller

over the P-I controller has motivated the investigation of the performance of the I-P controller for hvdc systems. The realization of P-I and I-P controllers for single input and single output systems is shown in Figure 7.1 and Figure 7.2. The following transfer functions can be obtained for both systems.

$$T(S) = \frac{K_I + K_p S}{S(1+TS) + K_p S + K_I} \tag{7.1}$$

where

$T(S)$ = transfer function for first order system controlled by the P-I controller.

$$T_1(S) = \frac{K_I}{S(1+TS) + K_p S + K_I} \tag{7.2}$$

where

$T_1(S)$ = transfer function for first order system controlled by I-P controller.

Comparing equations (7.1) and (7.2), it is evident that the I-P controller eliminates the "zero" of equation (7.2). However, the characteristic equation for both controllers is the same. The elimination of the "zero" causes smaller overshoot [51]. Hence, high gain values can be used to achieve a fast response [52]. The comparison of these two controllers is carried out in the next section for the detailed hvdc system. The detailed hvdc system representation and its controls are reported in Chapter V.

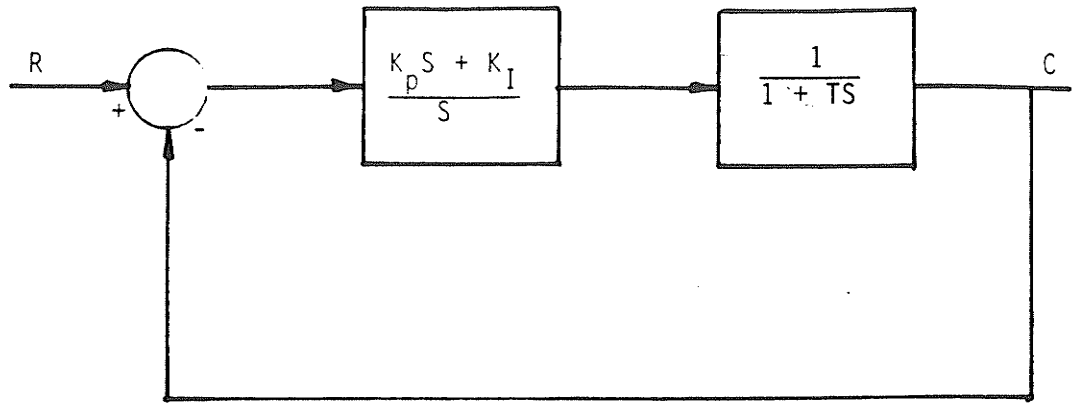


Figure 7.1 P-I Controller Configuration.

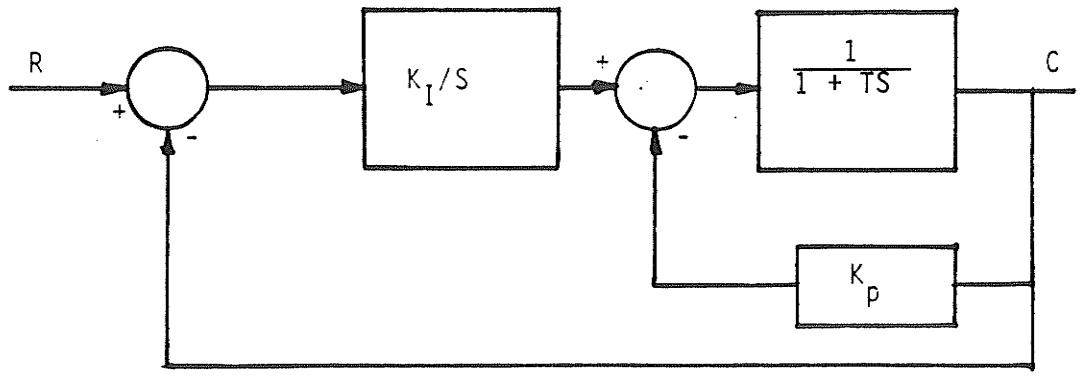


Figure 7.2 I-P Controller Configuration

7.2 DIRECT CURRENT STEP RESPONSE FOR A DETAILED MODEL OF THE HVDC SYSTEM FOR I-P AND P-I CONTROLLERS

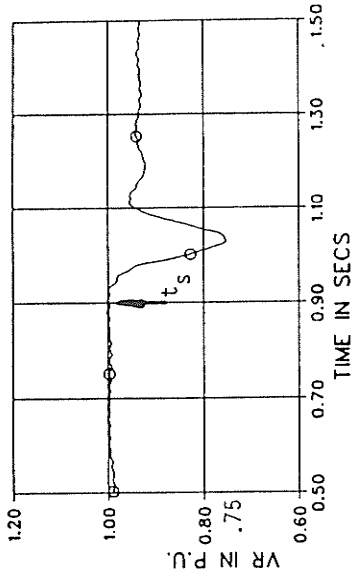
Only the current control configuration at the rectifier end has been changed from P-I to I-P controller because the inverter is operating in the predictive control. The following variables are observed for determining the effectiveness (Figure 7.3 and Figure 7.4).

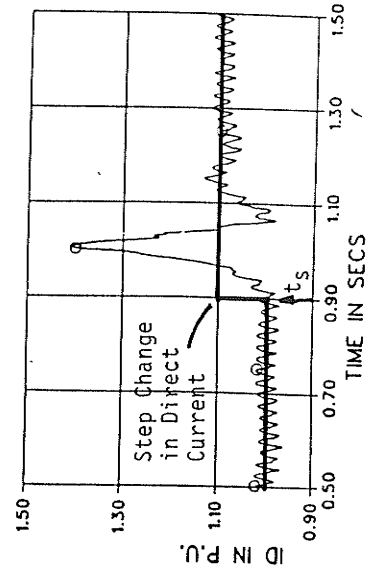
Instantaneous AC Voltage: The undervoltages produced by both the I-P and P-I controllers are similar in duration and magnitude.

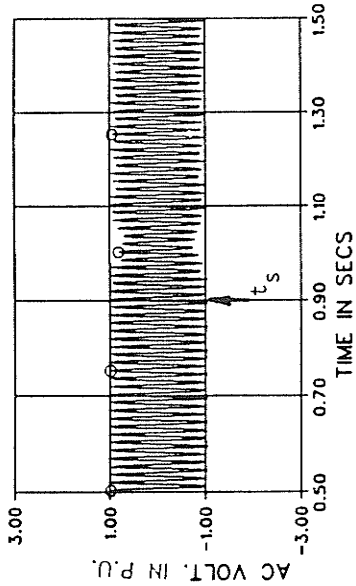
Three Phase RMS Voltage: The rms voltage response is superior to the P-I controller because of fewer fluctuations, as shown in Figure 7.3 and Figure 7.4.

D.C. Power: It can be observed from Figure 7.3 and Figure 7.4 that the dc power takes about 150 ms more for the I-P controller than the P-I controller to settle to the steady-state value. However, the smaller settling time is desirable for dc power from a stability point of view [6]. Hence, for the given gains for I-P and P-I controllers, the P-I controller performs better.

Direct Current: The direct current response would be affected the most because step change is made in the current reference. The overshoot in the direct current is reduced by 10% for the I-P controller. However, the settling time for the P-I controller is reduced by 150 ms, as shown in Figure 7.4.







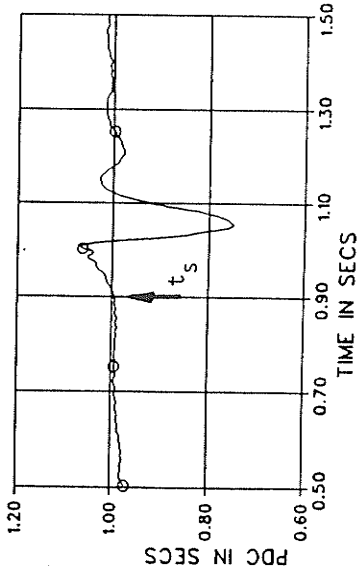


Figure 7.3 Direct Current Step Response of Detailed DC System with K_p = 0.045, and K_I = 30.0 for P-I Controller

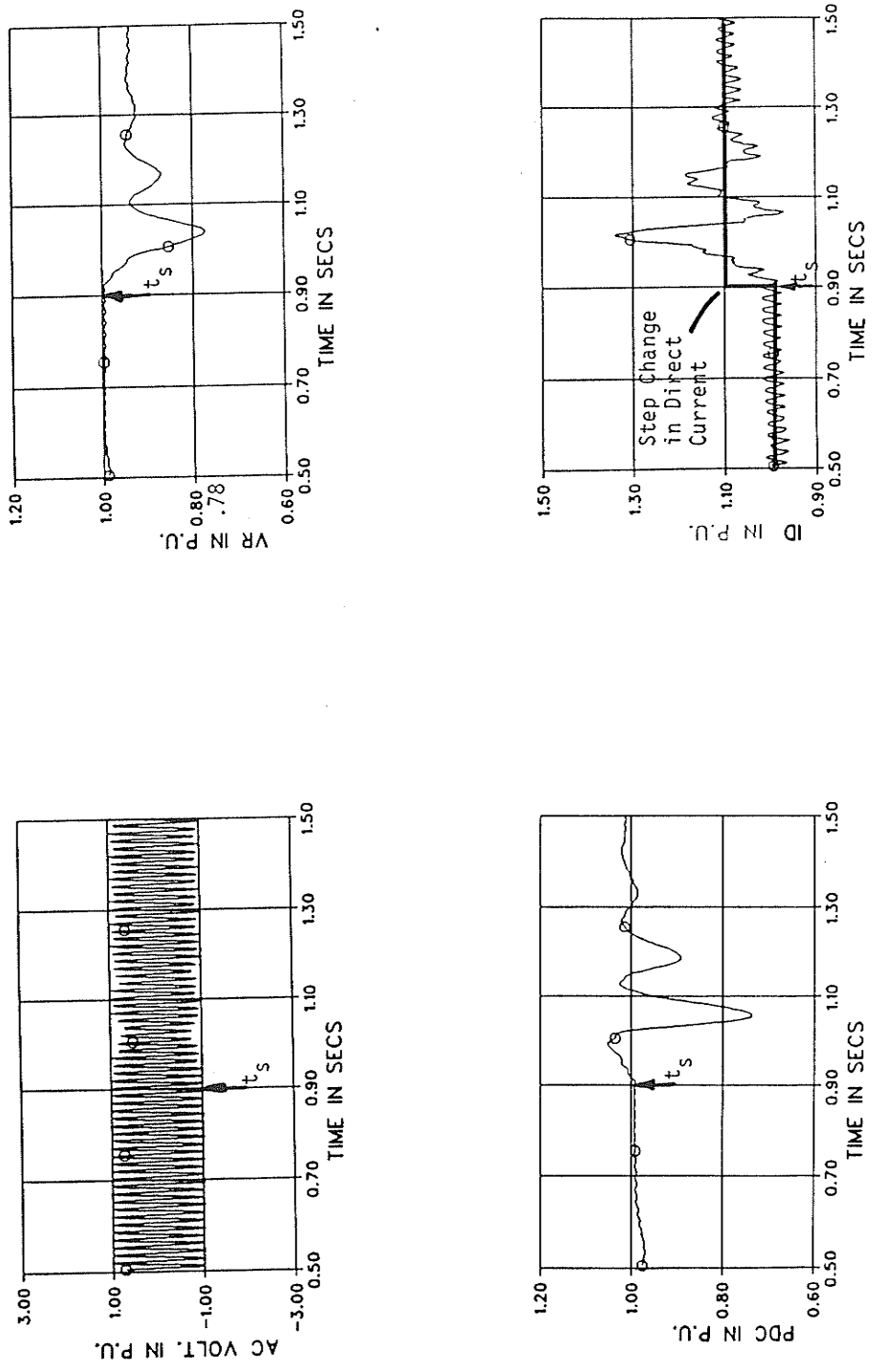


Figure 7.4 Direct Current Step Response of Detailed DC System with K_p = 0.045, and K_I = 30.0 for I-P Controller

Influence of the Controllers' Gains on the Direct Current Step Response

The traces of the instantaneous voltage, dynamic overvoltage, dc power and direct current showing the influence of the controllers' gains on the system response are presented in Appendix D1.

The current step response study indicates that the I-P controller can produce a better system response for high values of proportional gain. However, there is a limit to the proportional gain for the current control controller. The contribution to the firing angle from the gain should not exceed 5 to 8 degrees in steady-state operation because the normal operating firing angle is around 10 to 13 degrees and the minimum limit for the integral controller contribution is 5 degrees. Hence, the maximum proportional gain of 0.080 to 0.082 can be used. The proportional gain for the I-P controller is related to the firing angle as follows.

Firing angle due to proportional gain = $K_p * I_d$;

I_d = 1.0 p.u. in steady state.

The above-mentioned proportional gain range does not offer any advantages for the I-P controller over the P-I controller. Hence, the I-P controller has not been considered for further investigations. It is also observed that the increase in the integral gain for both the I-P controller and the P-I controller worsens the system response.

Another controller configuration is considered next which provides the transfer function similar to I-P controller with no restrictions on the gains.

7.3 MODIFIED I-P CONTROLLER

The modified I-P Controller configuration is shown in Figure 7.5. The transfer function can be written as follows (Figure 7.5).

$$T_2(S) = \frac{K}{TS^2 + S(1 + A_1K) + K} \tag{7.4}$$

Equation (7.4) is exactly the same as equation (7.3), provided

$$K = K_I$$

$$A_1 K_I = K_p; \text{ or } A_1 = \frac{K_p}{K_I}$$

The comparison of the modified I-P controller with the P-I controller is reported in subsequent sections.

7.4 DIRECT CURRENT STEP RESPONSE FOR DETAILED MODEL OF THE HVDC SYSTEM FOR MODIFIED I-P AND P-I CONTROLLERS

The proportional and integral gains are chosen to be the same for the P-I and modified I-P controllers, so that the characteristic equation for both cases has the same roots. Comparing Figure 7.6 and Figure 7.7, the following observations can be made.

i) The rms and dc power response is faster by 30 ms for the P-I controller.

ii) The overshoot in the current response is reduced by 1% in the case of the modified I-P controller. In addition, the settling time for the direct current is reduced by 50 ms for the modified I-P controller.

iii) The overshoot in the dc power for the modified I-P controller is reduced by 1%.

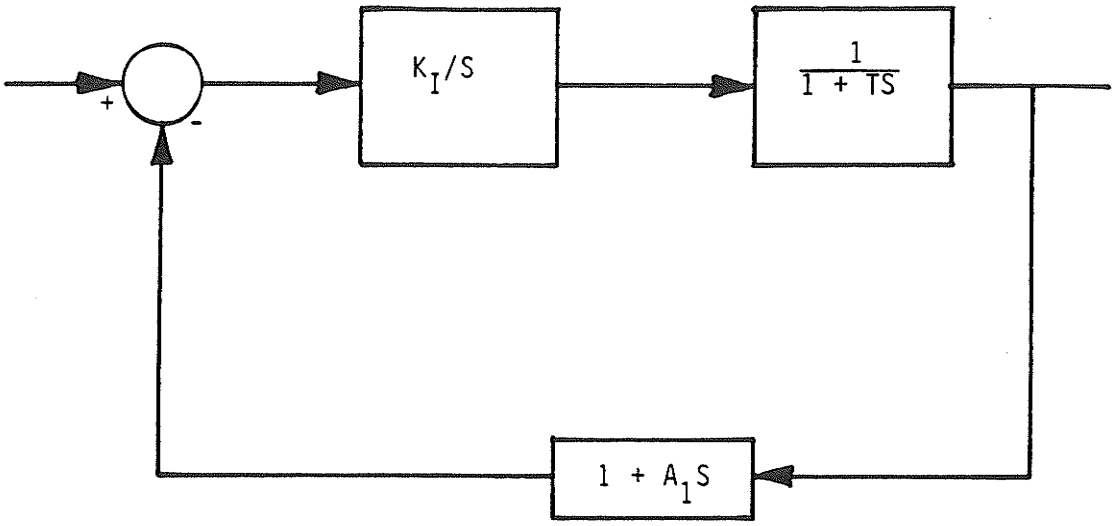


Figure 7.5 System Controlled by Modified I-P Controller

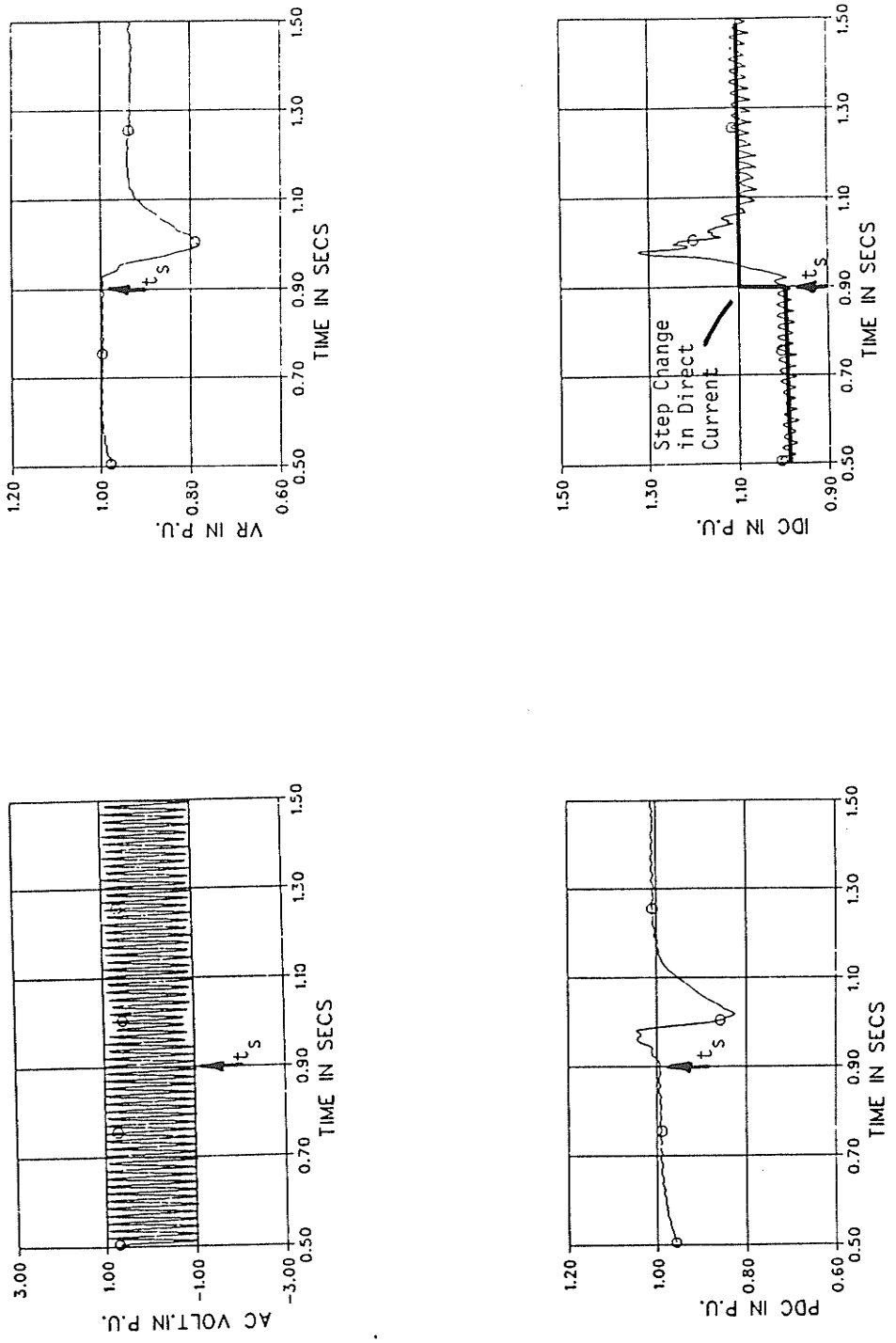


Figure 7.6 Direct Current Step Response for P-I Controller
(K_p = 0.04, and K_I = 30.0)

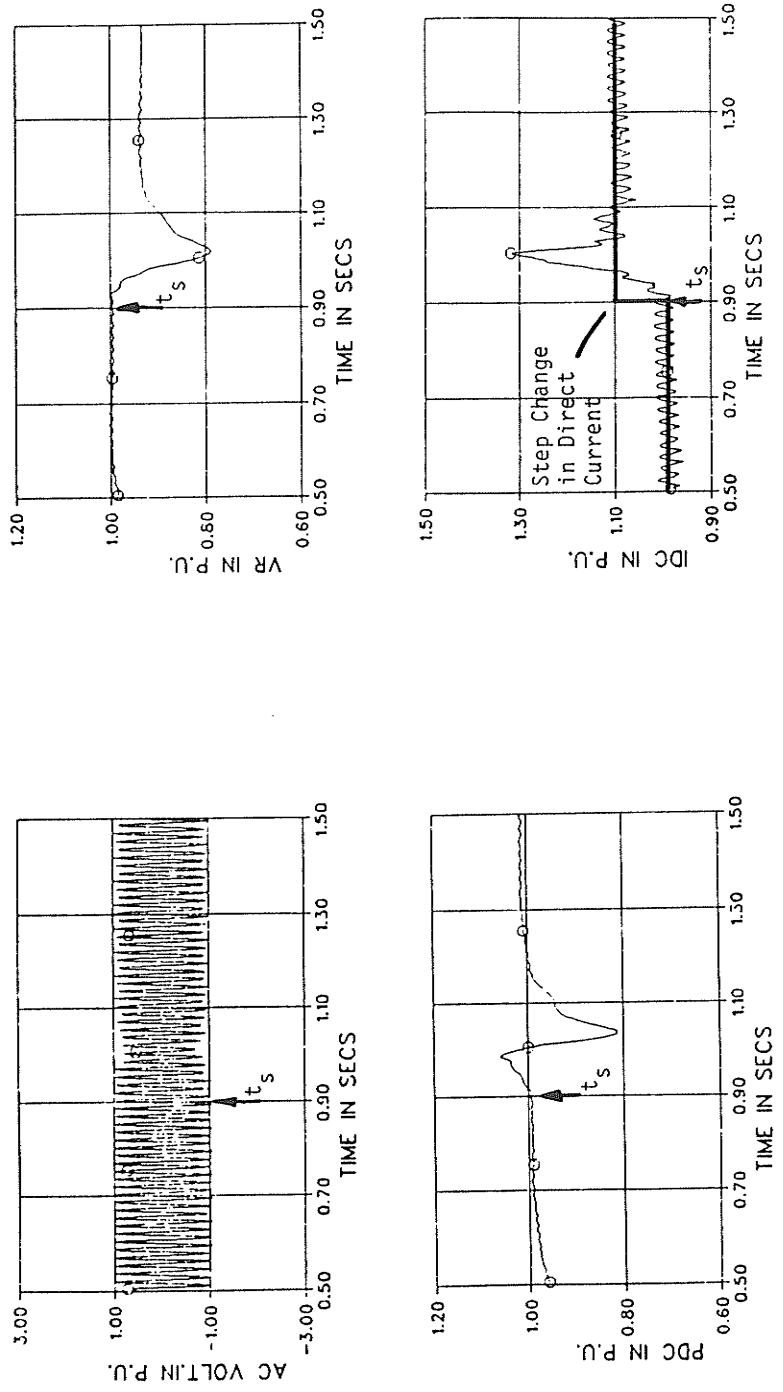


Figure 7.7 Direct Current Step Response for Modified I-P Controller
(K_p = 0.04, and K_I = 30.0)

Influence of Proportional and Integral Gains on the Direct Current Step Response

The system responses in terms of system variables discussed in previous sections for changed gains of controllers are presented in Appendix D2.

It is observed that the modified I-P controller offers the advantage of a faster system response without overshoots by using higher proportional gains. However, an increase in the integral gain for both modified I-P controller and P-I controller gains worsens the system response.

Further, investigations are carried out to determine the ability of the modified I-P controller to recover the system from some critical faults and its influence on system starting.

7.5 INFLUENCE OF CONTROLLER CONFIGURATION ON THE SYSTEM STARTING AND THE SYSTEM RECOVERY FROM FAULTS

System Startup: It is observed from Figure 7.8 and Figure 7.9 that the system starting time is shorter for the modified I-P controller by 30 ms. In addition, the overshoot is less by 10% in the direct current for the modified I-P controller.

The system recovery from the dc line fault, three phase to ground fault, and single phase to ground fault is investigated to compare the performance of the modified I-P controller to the P-I controller.

System Recovery: The system recovery from various faults reported in Chapter VI is studied to evaluate the relative performance for both the I-P and P-I controllers.

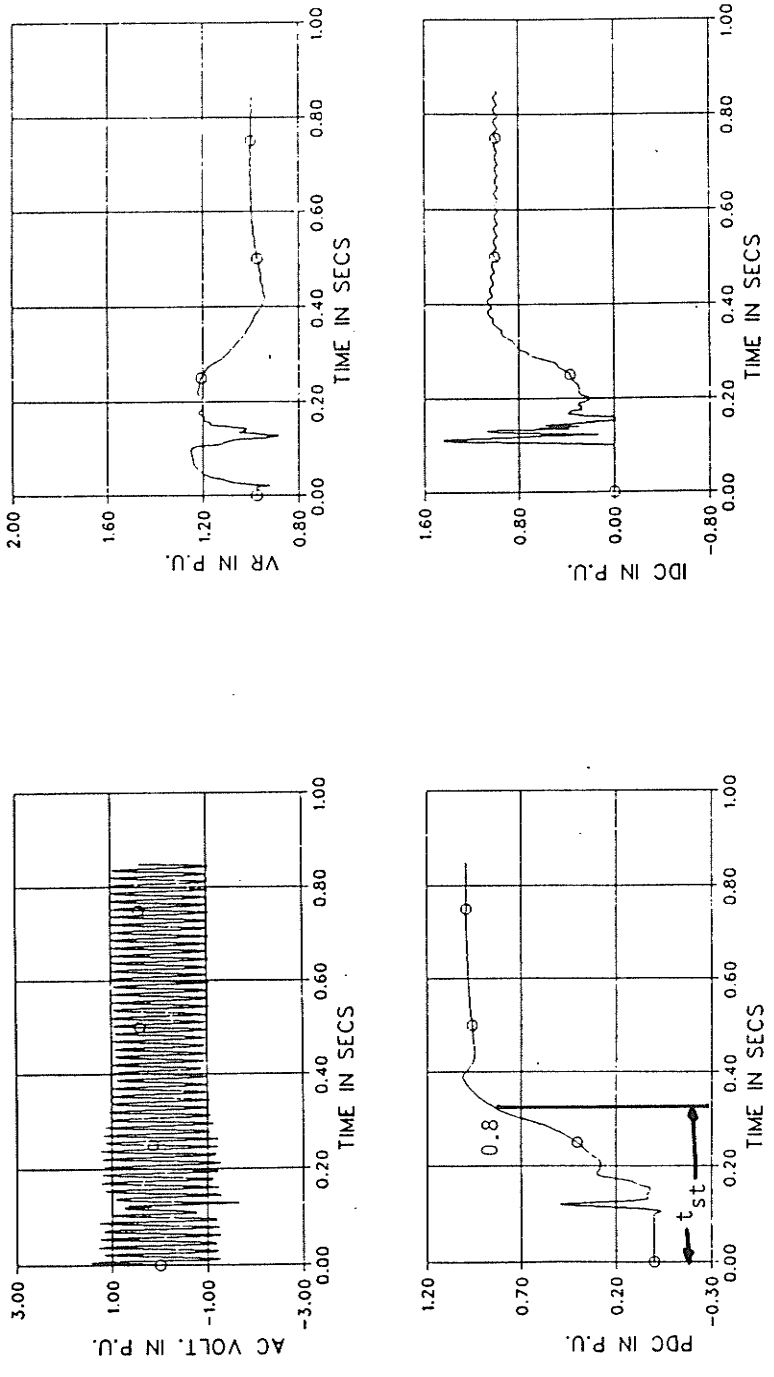


Figure 7.8 DC System Starting with P-I Controller

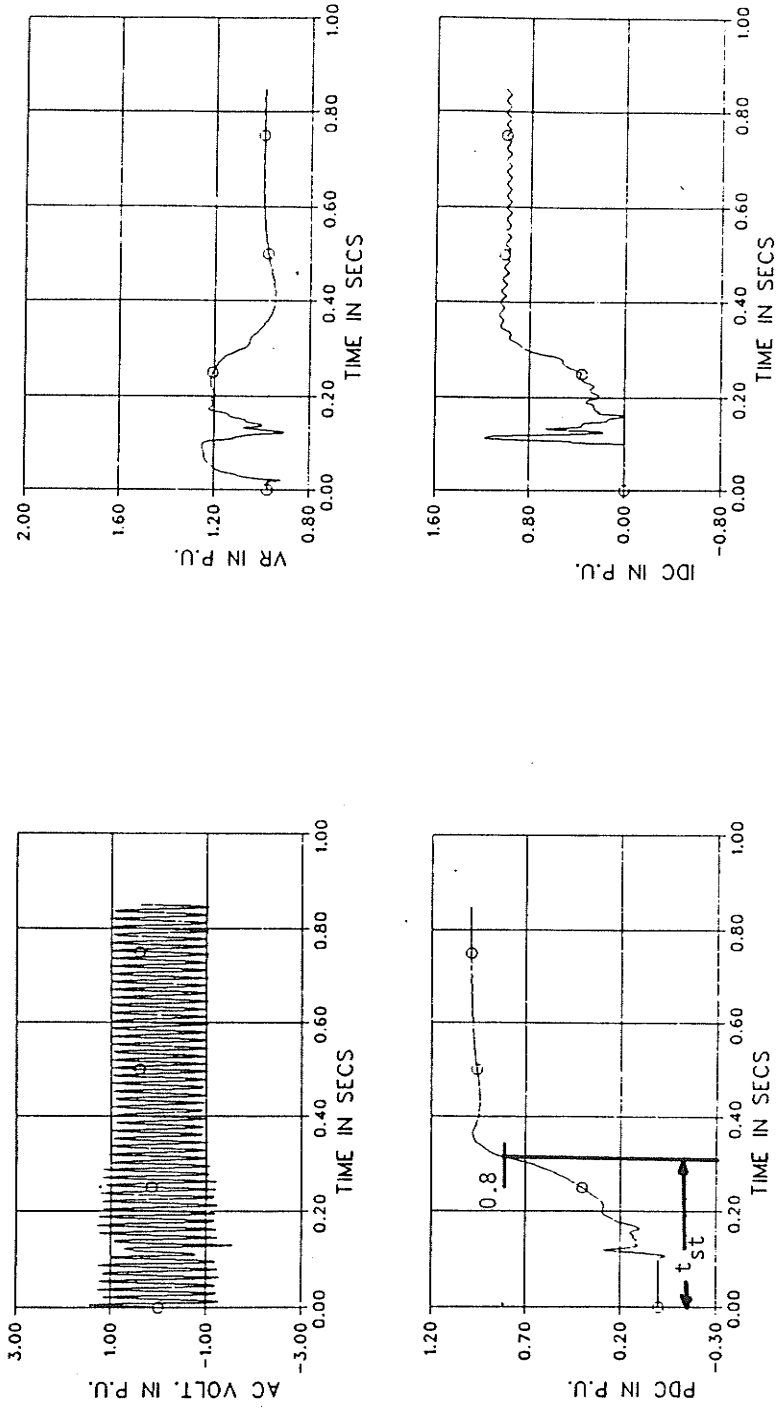


Figure 7.9 DC System Starting with Modified I-P Controller

Three Phase to Ground Fault at the Inverter Bus

The system recovery from the three phase fault at the inverter bus is shown in Figure 7.10 and Figure 7.11 for the modified I-P controller and the P-I controller in terms of variables discussed in Chapters IV and V. The following observations can be made from Figure 7.11 and Figure 7.11.

i) The dc power recovery is increased for the P-I controller by 200 ms.

ii) The dynamic overvoltage magnitude is the same, but the duration is reduced by 200 ms for the P-I controller.

iii) The duration of the peak instantaneous overvoltages is increased by 12 cycles for the modified I-P controller.

iv) Commutation failure is observed (Figure 7.10) for the I-P controller.

Similar results are obtained for the single phase to ground fault and the dc fault at the inverter terminal. The traces for various variables are presented in Appendix D3. The results for all three faults are summarized in Table 7.1 through Table 7.3.

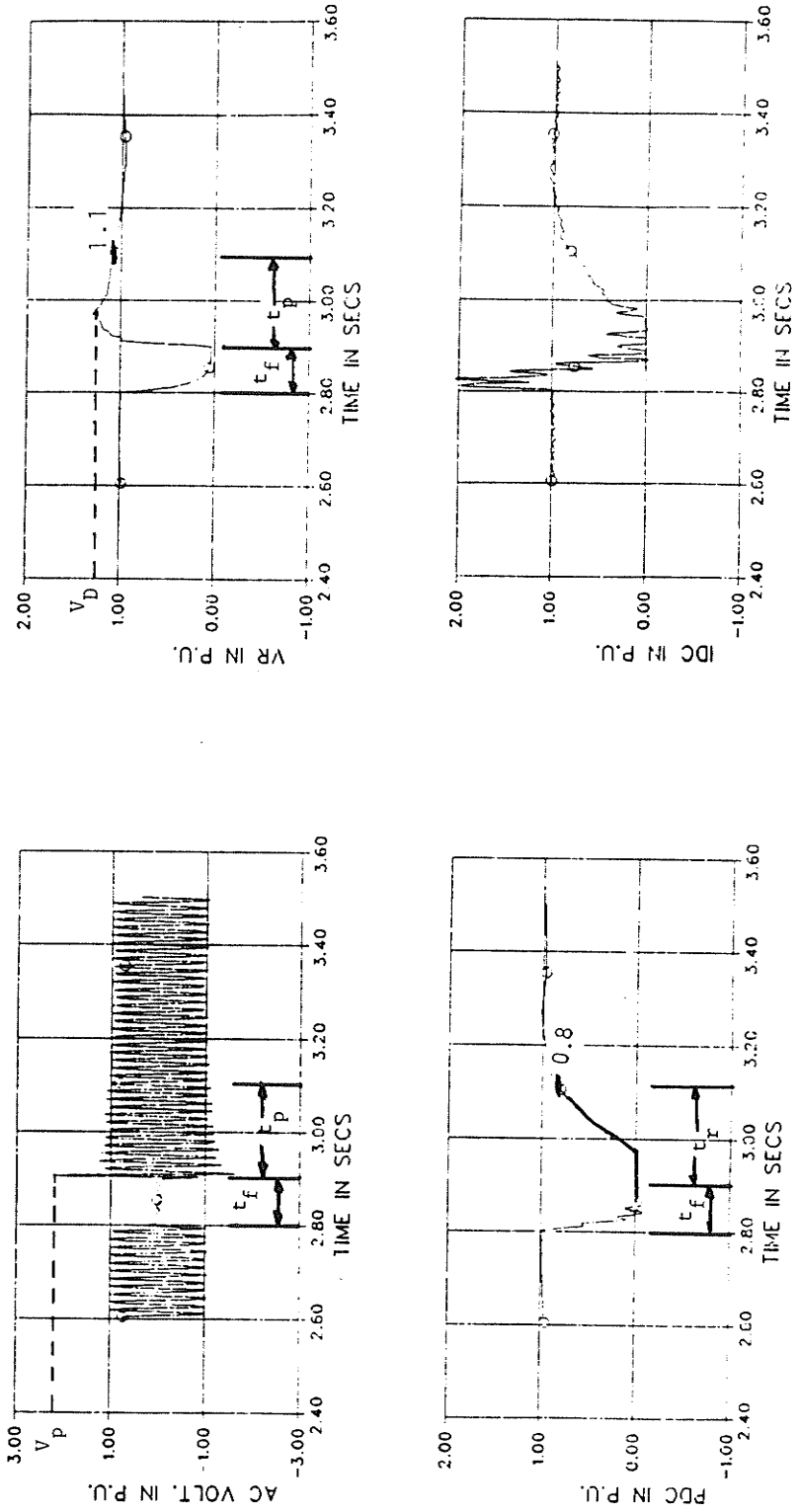


Figure 7.10 AC-DC-AC System Recovery from the Three Phase to Ground Fault at the Inverter AC Bus for P-I Controller

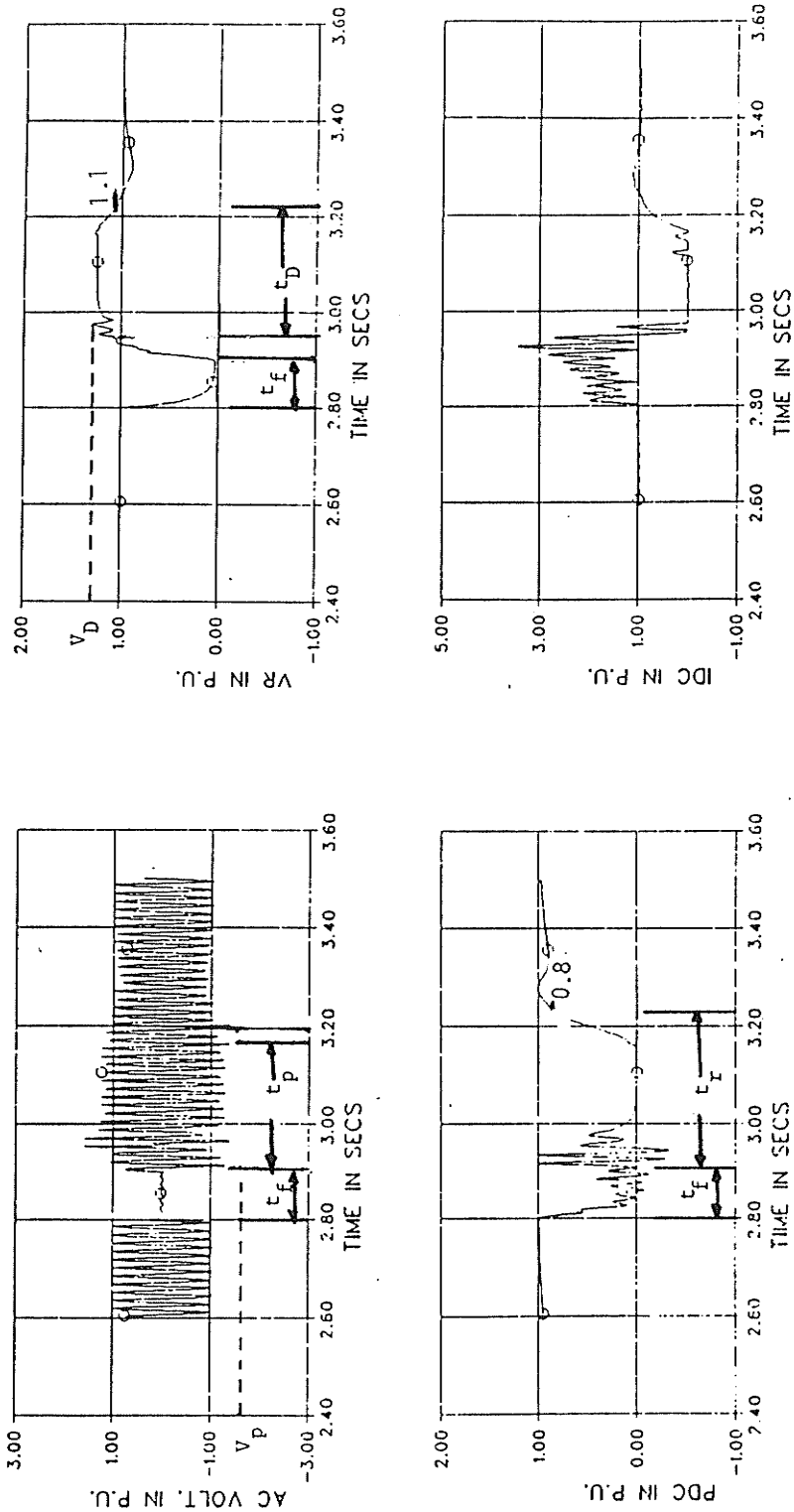


Figure 7.11 AC-DC-AC System Recovery from the Three Phase to Ground Fault at the Inverter AC Bus for Modified I-P Controller

Table 7.1 System Response for the Three Phase to Ground Fault at the Inverter AC Bus

Controller Name	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
Modified I-P	2.16	290	1.28	290	319
P-I	1.63	200	1.25	200	200

Table 7.2 System Response for the Single Phase to Ground Fault at the Inverter AC Bus.

Controller Name	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
Modified I-P	2.4	150	1.20	150	200
P-I	2.25	140	1.19	140	200

Table 7.3 System Response for the DC Line Fault at the Inverter Terminal.

Controller Name	Instantaneous Voltage Response		Dynamic Overvoltage Response		DC Power Recovery Time
	Highest Magnitude in p.u. V_p	Duration in ms t_p	Highest Magnitude in p.u. V_D	Duration in ms t_D	t_r in ms
P-I	1.25	170	1.25	170	175
Modified I-P	1.60	320	1.38	320	338

7.6 DISCUSSION

It is observed that the I-P controller provides a better current step response than the P-I controller. However, for the current controller on the rectifier terminal the steady-state firing angle normally is around 10 to 13 degrees. Hence, a small proportional gain can be used only for the I-P controller. It is found that the merits of the I-P controller are exploited only for high proportional gain. To overcome the limitation on the proportional gain, a modified I-P controller is used. It is understood from the investigations that the performance of the modified I-P controller is better than the P-I controller for the step change in the direct current. However, it is also observed from Table 7.1 to Table 7.3 that the system recovery from various faults is worse for the modified I-P controller.

7.7 CONCLUSIONS

Various controller configurations are examined in this chapter. The following conclusions are drawn.

i) The I-P controller performs better than the P-I controller for high proportional gain. However, the I-P controller cannot be used with high proportional gain due to the requirements of the current controller. Hence, it may be concluded that this controller is of little use in hvdc system applications.

ii) The modified I-P controller is proposed as a replacement for the I-P controller. The modified I-P controller improves the direct current step response. In addition, the system starting time is reduced by the use of the modified I-P controller. Further, there

is no limitation on the choice of proportional gains as existed for the I-P controller.

iii) It is also observed that the best system recovery cannot be achieved by just designing controllers by small signal analysis or the step response. This is due to the fact that the modified I-P controller performs better than P-I controller for the current step responses. However, the system recovery from various faults is poorer for the modified I-P controller.

iv) No significant advantage is gained by changing the P-I controller to the I-P controller.

CHAPTER VIII

STATE IDENTIFICATION FOR HVDC SYSTEM: SOME NEW PARAMETERS FOR SIGNAL PROCESSING

8.1 INTRODUCTION

Adaptive controls for hvdc systems show better results than fixed parameter controllers [55]. However, the convergence time required for the adaptive control algorithms can be significant [56]. To overcome the problem of slow convergence, the look-up table concept has been proposed [56] for real time applications. One of the essential steps for the application of a look-up table is the fast state identification in order to make decisions about the choice of controller parameters. However, state identification has not been well discussed in the power system control literature. Hence, some of the techniques used for other systems for state identification [57-58] are examined for hvdc systems.

This chapter is devoted to evaluating the effectiveness of various discriminants to identify various faults. It is assumed in the study that task-oriented VLSI chips can be designed to achieve the required speed of computation. The speed of computation is important because only 100 ms duration of fault is to be utilized to perform the following tasks:

i) Calculate the discriminants,

ii) Match patterns of the discriminants to identify the fault, and

iii) Change controller settings.

It is proposed that in order to perform the above-mentioned tasks, information about the signal may be utilized in the first two cycles.

8.2 DESCRIPTION OF VARIOUS DISCRIMINANTS

State identification is the most important aspect in the whole decision-making domain because the system status will confirm what decisions should/can be made and how the decision-making process' output has to be implemented.

The following class of state-identification techniques are considered:

i) Statistical Techniques:

This class can further be divided into subclasses as follows:

a) Mean value based decisions

b) Variance/standard deviation based decisions

c) Kurtosis value based decisions

d) Skewness value based decisions

ii) Frequency Domain Techniques:

Sometimes it is easy to obtain information in the frequency domain and, hence, the following parameters may be used as discriminants.

a) Spectrum

b) Harmonic and frequency factors

These techniques have been chosen from available techniques for the following reasons.

i) These can be implemented without performing the complex mathematical calculations. Consequently, the computer time needed to make decisions is small.

ii) Algorithms give different discriminant values for various faults. Hence its authenticity and reliability is high.

iii) Algorithms' output can easily be related to decision processes.

8.3 APPLICATION OF VARIOUS DISCRIMINANTS FOR FAULT IDENTIFICATION

Statistical Techniques

Mean, variance, skewness, and kurtosis functions as defined below have been used for fault discrimination [59].

$$\text{Mean} = \mu = \frac{\sum_{i=1}^{N} X_i}{N} \tag{8.1}$$

$$\text{Variance} = \sigma = \frac{\sum_{i=1}^{N} (X_i-\mu)^2}{N} \tag{8.2}$$

$$\text{Skewness} = S_k = \frac{1}{N} \frac{\sum_{i=1}^{N} (X_i-\mu)^3}{\sigma^{3/2}} \tag{8.3}$$

$$\text{Kurtosis} = K = \frac{1}{N} \frac{\sum_{i=1}^{N} (X_i-\mu)^4}{\sigma^2} \tag{8.4}$$

where X_i = value of signal at i^{th} instant.

Frequency Domain Techniques

The spectrum of each fault can also be used as one of the discriminants [58]. However, pattern matching for the spectrum is time intensive. Hence, new discriminants are defined which utilize the information contained in the spectrum.

$$\text{Harmonic Factor (HF)} = \sqrt{\frac{\sum_{i=1}^{N} G_i^2 f_i^2 \sum_{i=1}^{N} G_i^2/f_i^2}{\sum_{i=1}^{N} G_i^2}} \qquad (8.5)$$

$$\text{Frequency Factor (FF)} = \sqrt{\frac{\sum_{i=1}^{N} G_i^2 f_i^2}{\sum_{i=1}^{N} G_i}} \qquad (8.6)$$

where G_i = Power stored at the i^{th} frequency

f_i = i^{th} frequency

$\sum$ = summation over given interval

There can be a problem in calculating a spectrum because of wide variations or small changes in the signal of interest for various system disturbances. To amplify or limit these variations, a transformation is used, which is discussed next.

8.4 LOG-TRANSFORMATION

Normally, cepstrum is used [59] to extract information from a signal about its frequency contents. However, dual of cepstrum may be used to extract the information of characteristics of the signal in a time domain. The dual of cepstrum may be calculated by applying the log-transformation on the time domain signal. The log-transformation has the following properties:

a) Elimination of Convolution Problem in Frequency Domain

Any given function $x(n)$ can be any of the following forms:

i) $x(n)$ can be a simple function, i.e., $x(n) = \sin t_n$ or $x(n) = n$.

ii) $x(n)$ is the product of two or more functions, i.e., $x(n) = x_1(n) \cdot x_2(n)$.

The frequency domain information of $x(n)$ can be determined by taking Fourier transform of $x(n)$. However, in case (ii), the problem of frequency domain convolution is to be solved. One method of overcoming the convolution problem is to take log of $x(n)$, i.e.,

$$x(n) = x_1(n) \cdot x_2(n) \tag{8.7}$$

Taking log of equation (8.7), we get

$$\log x(n) = \log x_1(n) + \log x_2(n) \tag{8.8}$$

By defining, $y(n) = \log x(n)$; $y_1(n) = \log x_1(n)$; and $y_2(n) = \log x_2(n)$, we get,

$$y(n) = y_1(n) + y_2(n) \tag{8.9}$$

Equation (8.9) follows superposition. In this way, the convolution problem can be eliminated.

b) Fault Identifier

The properties of direct current are used to identify the faults because the frequency of short faults is much higher than open faults. During short faults the voltage may become zero and can cause a computation problem for spectrum analysis.

The direct current is generally normalized to 1.0 p.u. to represent the steady-state value and log of 1.0 is zero. Hence, any definite value of the log-transformed direct current will indicate the disturbance in the system.

c) Trending

Data which is segregated can be compressed and wide variations can be smoothed with the use of a log-transformation. For example, if the variation in the signal is taken between 10^{-6} to 100, this variation can be reduced to -6 to 2 by taking the log, and better trending can be obtained.

d) Frequency Domain Information

The frequency domain information of the signal remains unaltered, e.g., if $y = a + b \sin t$; then $\log y = \log (a + b \sin t)$.

8.5 RESULTS

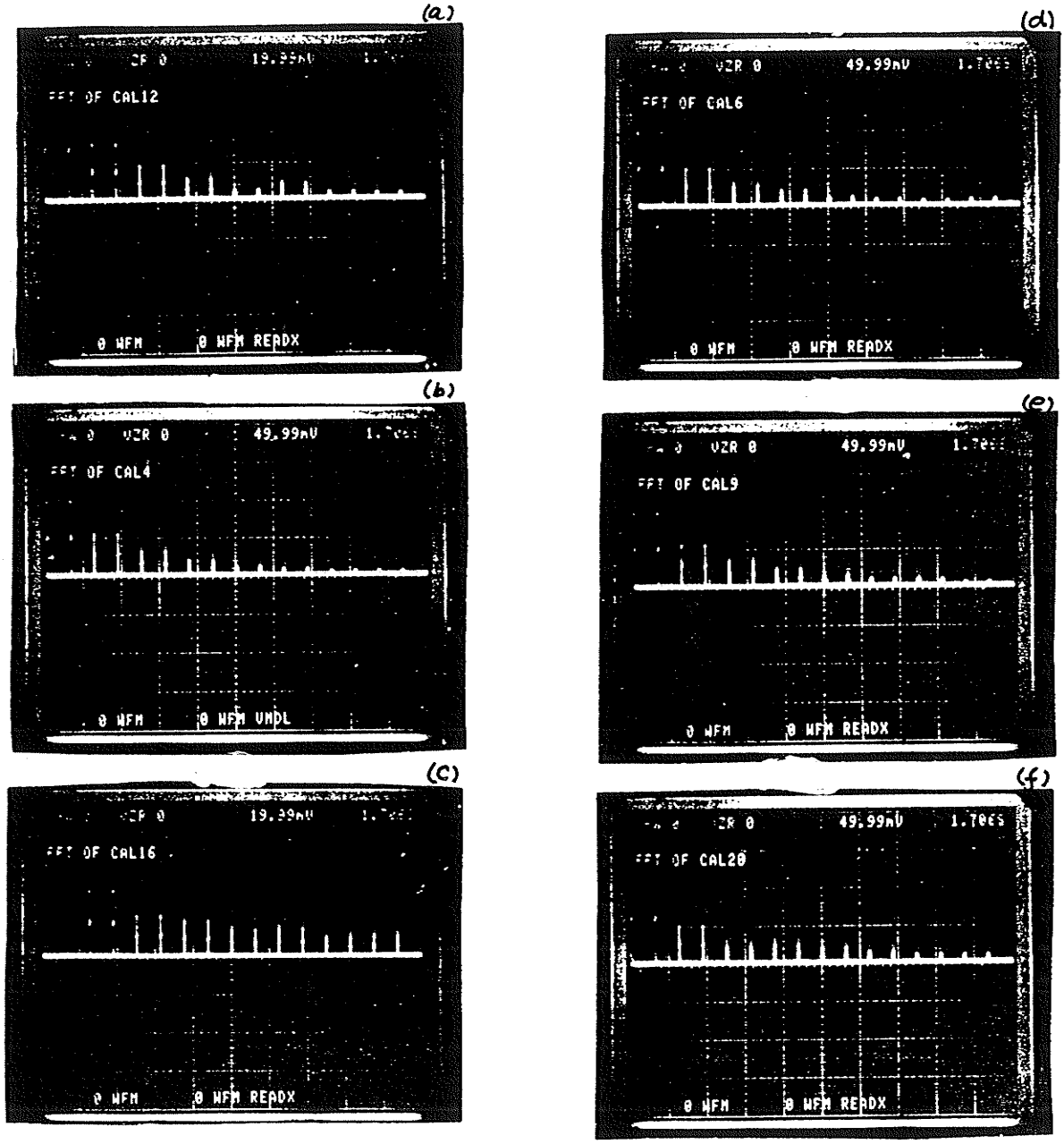
The direct current signal has been used to calculate different discriminants. The direct current signal has been used for two main reasons. First, the probability of short faults is much higher than open faults. Secondly, it represents the equivalent current of three

phases of the ac system of the rectifier and the inverter terminals. This minimizes the total number of measurements.

The spectra of the direct current for a fault duration of 100 ms are calculated for various faults. It is observed from Figure 8.1 that the spectrum for each fault is different. To improve the computational efficiency for pattern matching, the harmonic factor and frequency factors are calculated and tabulated in Table 8.1. It is observed that the harmonic factor is nearly the same for various faults, but the frequency factor is a good indicator for identifying the fault. The repetition of the experiment shows for different instants of faults a maximum of 1.0% variation in the value of the frequency factor. Hence, this factor is chosen as a viable discriminant for further investigation. Skewness and kurtosis are also calculated and their values are shown in Table 8.1. These factors are calculated without log-transformation. The difference in the values of kurtosis and skewness is not very significant for various faults. However, these discriminants can be used to confirm the decision.

These results are obtained on the real time, physical component simulator which has limitations for representing the system (Chapter IV). Hence, further investigations are carried out in the detailed system using EMTDC to determine the influence of sampling rate on the value of discriminant.

It is observed for various faults that the 64 samples/cycles is an optimum number because discriminants values do not change significantly for more than 64 samples/cycles (Appendix E).



a) D.C. Line Fault b) Single Phase to Ground Fault on the Inverter
c) Remote Single Phase Fault d) Remote Three Phase Fault
e) Single Phase to Ground Fault on Rectifier Bus f) Three Phase Fault on Rectifier Bus

Figure 8.1 Frequency Spectra for Different Faults

Table 8.1 Discriminants Values for Various Faults.

Case No.	Type of Fault	Skewness	Kurtosis	Harmonic Factor	Frequency Factor
1	Remote three phase fault on the inverter side	0.955	2.59	1.34	725.0
2	Remote single phase fault on the inverter side	0.97	2.56	1.58	735.0
3	Single phase to ground fault on the inverter ac bus	0.82	2.26	1.18	754.0
4	Three phase to ground fault on the inverter ac bus	0.995	2.63	1.22	844.92
5	Single phase to ground fault on the rectifier ac bus	0.149	2.06	1.18	685.50
6	Three phase to ground fault on the rectifier ac bus	1.079	3.15	1.17	651.00
7	DC line fault on the inverter end	-0.429	1.55	1.22	629.00

8.6 DECISION PROCEDURE

It is very important to make the right decision to identify the fault. It is observed from Table 8.2 through Table 8.4 that a good decision can be reached if more than one discriminant is used to identify the fault. The problem of computational time can be resolved by using a parallel processing technique because all five discriminants can be calculated independently and simultaneously.

The experiment was repeated only three times because of the required computer time for the simulation of hvdc systems for different instants of faults. It is observed that the trends of these discriminants remain unchanged. The values of the standard deviation, skewness, and kurtosis change within only 2%. Variations in the harmonic index are negligible, but the changes in the frequency factors lie in the 5% range. Hence, it is decided not to use the frequency domain technique.

The standard deviations, skewness, and kurtosis are also calculated by performing the log-transformation. It is determined that better resolutions of the discriminants can be obtained by using log-transformation, as can be observed by comparing case (3) and (5) shown in Table 8.2 and Table 8.3 respectively.

Table 8.2 Discriminants Values for Various Faults.

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
1	Steady State	0.01904	-0.66926	-0.80294	64
2	DC Line Fault at the Inverter	0.26314	1.04508	-0.18054	
3	Single Phase to Ground Fault at Inverter	0.16703	-0.70157	-0.67145	
4	Three Phase Fault at the Inverter Bus	0.41887	-1.08409	0.32083	
5	Single Phase to Ground Fault at the Rectifier Bus	0.17011	0.84698	-0.59688	
6	Three Phase to Ground Fault at the Rectifier Bus	0.38108	0.86997	-0.55785	

Table 8.3 Discriminants Values for Various Faults with Log-Transformation.

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
1	Steady State	0.02053	-0.69240	-0.76304	64
2	DC Line Fault at the Inverter	1.52101	-0.43476	0.02533	
3	Single Phase to Ground Fault at Inverter	0.14441	-0.89675	-0.23274	
4	Three Phase Fault at the Inverter Bus	0.50846	-2.32771	5.80805	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20897	0.64886	-0.97401	
6	Three Phase to Ground Fault at the Rectifier Bus	2.00063	-0.86988	-0.07058	

Table 8.4 Discriminants Values for Various Faults (Frequency Domain Analysis).

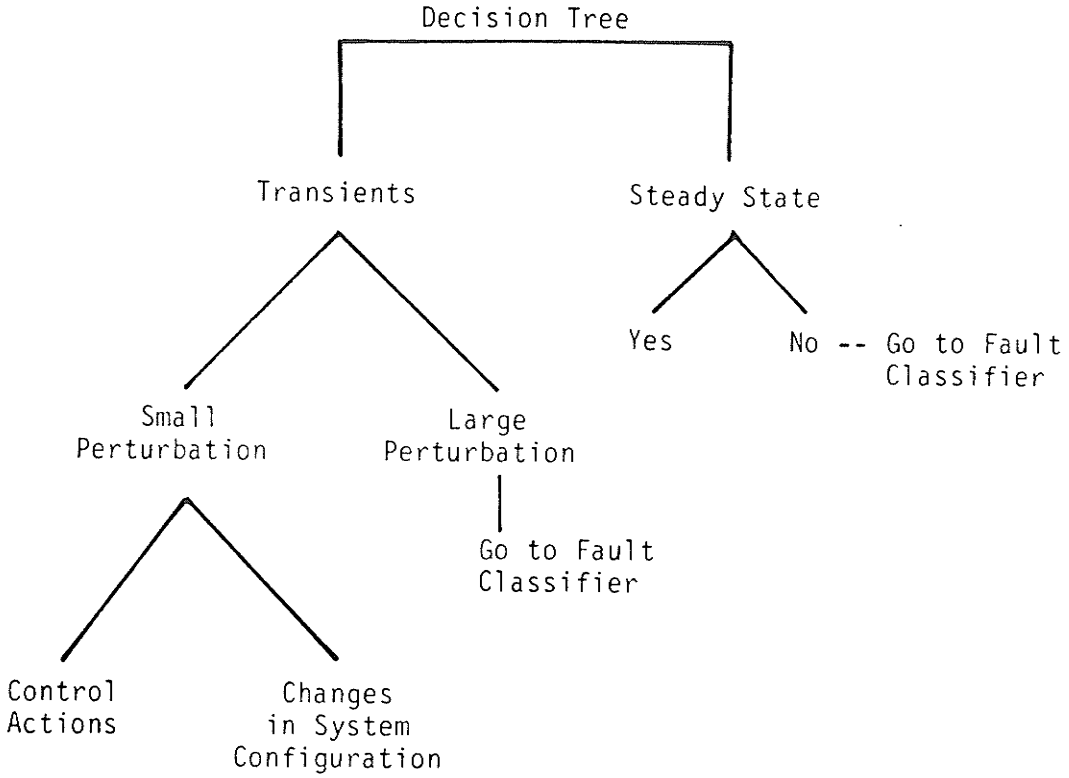
Case No.	Type of Fault	Harmonic Factor	Frequency Factor	Log Transformation Harmonic Factor	Log Transformation Frequency Factor	No. Samples/ Cycles
1	Steady State	1.26	128.9	1.27	129.2	64
2	DC Line Fault at the Inverter	1.13	124.0	1.31	131.2	
3	Single Phase to Ground Fault at Inverter	1.01	119.4	1.02	119.9	
4	Three Phase Fault at the Inverter Bus	1.04	120.4	1.40	135.2	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.2	1.13	124.1	
6	Three Phase to Ground Fault at the Rectifier Bus	1.18	126.0	1.14	124.2	

8.7 DISCUSSION

Various frequency and time domain discriminants have been examined for identifying different faults, using a pattern matching technique. The selection of these discriminants has been made on the basis of computational time and their resolution for discriminating various faults.

The study has been divided into two parts. The results are obtained on the physical component simulator for 100 ms fault duration. It has been determined that the frequency factor provides the better resolution for identifying various faults. However, the kurtosis, skewness and harmonic factor have not produced good resolution in their values for various faults. It has been observed that after determining the type of fault, one may need to change system and/or controller parameters for optimum system recovery. Hence, duration of the signal for which discriminants were calculated may be reduced. The second part of the study has been devoted to calculating these discriminants for two cycles duration, and the remaining duration of the fault can be used to make changes in the system and controller parameters.

It has been determined that the frequency domain discriminants have not produced the proper resolution for a signal of two cycles duration. Hence, another discriminant called standard deviation also has been considered. It has been observed that time domain discriminants provide better resolution. However, one should consider the standard deviation, skewness, and kurtosis together in reaching the decision of identifying the fault to improve its reliability. It has been determined that 64 samples/cycles have been adequate to calculate these discriminants.



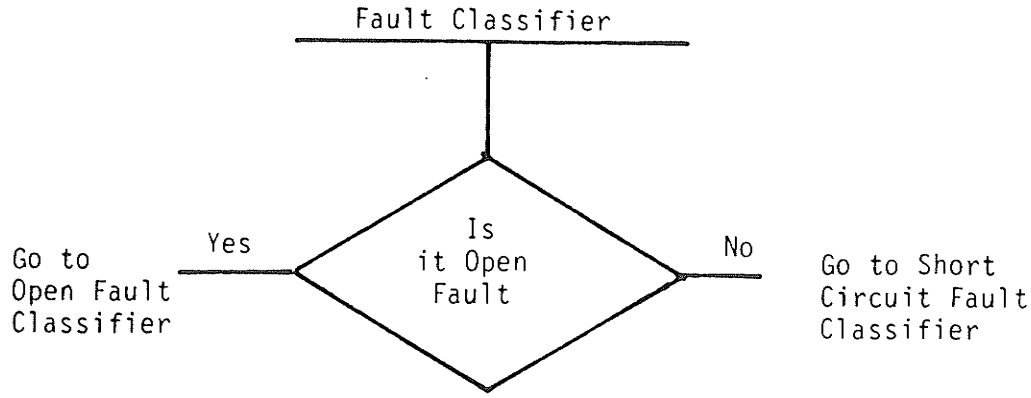


Figure 8.2 Decision Tree for Fault Detection

In addition, the log-transformation has also been suggested to improve the resolution of the various discriminants.

8.8 CONCLUSIONS

Various discriminants are discussed for fault identification for an hvdc system. The following conclusions may be drawn from the study reported in this chapter.

i) Frequency factor is a good discriminant for identifying various faults, provided that the duration of the signal is 100 ms.

ii) Harmonic index provides poor resolution for identifying various faults irrespective of the duration of the signal.

iii) It is determined that more than one discriminant must be used to identify the fault.

iv) The fault can be identified by pattern matching of standard deviation, skewness, and kurtosis.

v) The resolution of discriminant values may be improved by using log-transformation.

CHAPTER IX

CONCLUSIONS

This thesis is a prelude to building a knowledge base system (KBS) for the controller of a point-to-point hvdc scheme feeding to weak ac systems. A knowledge base about various control schemes at the inverter terminal is generated. Various controller configurations are evaluated to produce knowledge about the effectiveness of configurations to be used for different type of disturbances.

The effectiveness of various control schemes is evaluated by investigating the system stability and the system recovery from various faults at the ac and dc sides of the inverter and rectifier terminals. Furthermore, influence of the controller and system parameters is studied to determine sensitivity of the stability boundaries and the system recovery time. The system performance subjected to disturbances is evaluated by examining the instantaneous peak ac voltages, the dynamic overvoltages (their duration and magnitude), and the recovery time of the dc power.

The small signal stability of the system is carried out by using the root locus technique. The following conclusions may be drawn for all control schemes.

i) Lower values of controller gains improve the system stability.

ii) Higher values of the short circuit ratio of the receiving ac system improve the system stability.

iii) Lower values of the short circuit ratio of the sending ac system improve the system stability.

iv) All control schemes, if properly optimized, can provide essentially the same damping.

In addition, a new technique is suggested to handle the non-linearities of hvdc systems. It is concluded that the technique can be used to determine the system stability for relatively large changes in the system operating points with only ±5% error of linearization.

Several investigations have been carried out on the real time, physical component simulator to generate an impression about the relative performance of various control schemes. For simulating the detailed system, including converter transformers saturation, digital computer study using the EMTDC package has been performed. The following conclusions may be drawn from the investigations.

i) The same recovery time can be achieved for the dc power by the appropriate optimization of each control scheme.

ii) It is proposed to introduce a chosen control scheme for a few cycles (300 ms) just after the fault and then revert the system operation to the conventional control scheme. This technique retains the advantage that the system is operated with the conventional controls during steady-state, which keeps the reactive power demand and the harmonic generation to the minimum. Whereas, during transients the ac or the dc voltage control scheme can be inserted to improve the voltage characteristics at the inverter terminal. The switching among controls does not lead to system instability.

Investigations are carried out to determine the influence of the sending and the receiving ac system short circuit ratios on the system recovery. The following conclusions may be drawn:

i) The reduction of the short circuit ratio of the inverter ac system may degrade and slow down the system recovery.

ii) The reduction of the short circuit ratio at the rectifier side may improve the system recovery.

The investigations carried out for the rectifier terminal controller selections show that the modified I-P controller may be used to improve the system stability and system starting. Whereas, to improve the system recovery from various faults, the P-I controller may be used. An intelligent controller can make such switching practical.

From earlier discussions, it is observed that knowledge base systems must have the knowledge about each event and corresponding changes to be made in controller configuration, control schemes, and the controller parameters. To identify the event or the disturbance, new discriminants are suggested. It is determined that 64 samples over two cycles are sufficient to identify the faults. The use of log-transformation is suggested to improve the resolution of these discriminants.

SUGGESTED FUTURE WORK

The work presented in this thesis can be further extended in the following directions.

a) Possible application of expert system/knowledge base systems using the decision procedure may be suggested. However, the extent of the variation of these discriminants needs to be evaluated with

various configurations of the ac system at the receiving and the sending end. Areas of knowledge representation for fast computation of decision variables can be explored.

b) The reduction in short circuit ratio on the sending ac system improves the stability of the system. Hence, switching in/out extra resistance/impedance can be used as an alternative damping control.

c) Custom-designed microprocessor chips can be used for the implementation of various controls and forming an intelligent controller.

APPENDIX A1

Table A1.1(a) Parameters for the Receiving AC System.

SCR	R1 (Ohms)	L1 (mH)	AC Bus Voltage (Line to Line) (Volts)	Filter Ratings (VA)
2.0	69	45.6	25.0	5.0

Table A1.1(b) Parameters for the Sending AC System.

SCR	R2 (Ohms)	L2 (mH)	AC Bus Voltage (Line to Line (Volts)
4.0	16	5.0	25.0

Power flow in the dc line = 12.5 W.
Current at the rectifier end = 250 mA.
Smoothing reactor (Ld) = 300 mH.
DC resistance of the smoothing reactor = 2Ω.
The resistance of transmission line = 1Ω.
The inductance of transmission line = 54 mH.
The capacitance of transmission line = 0.676 μF.

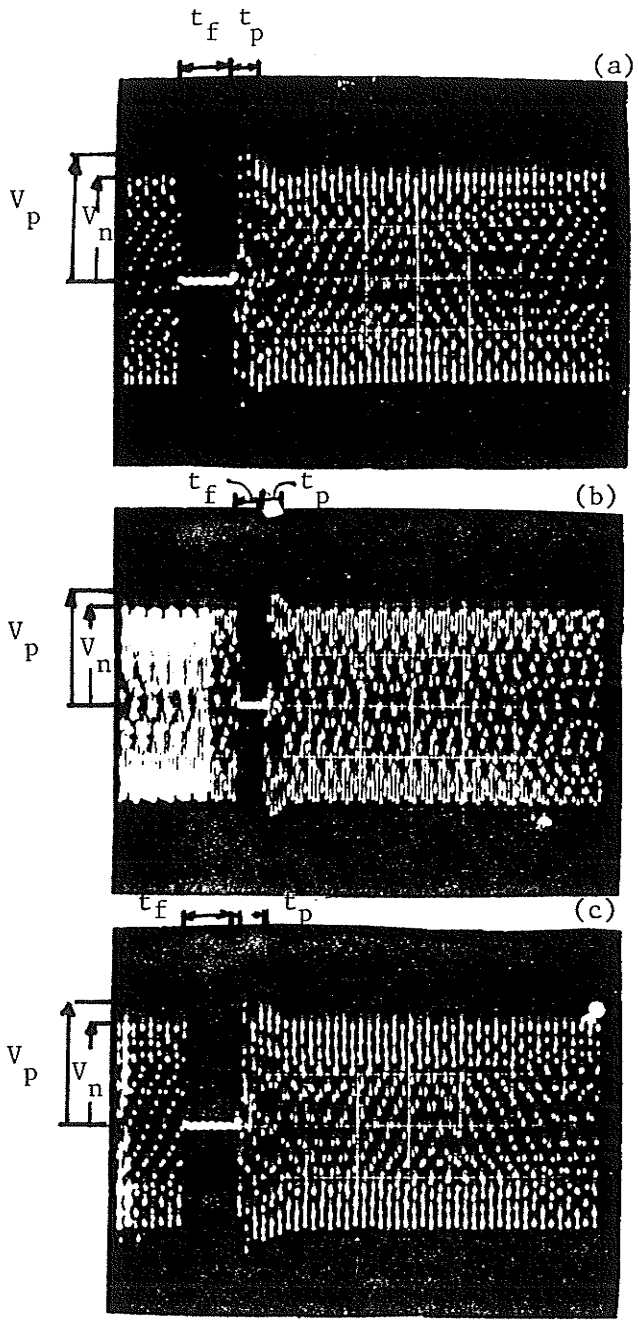
Table A1.1(c) AC Filter Data.

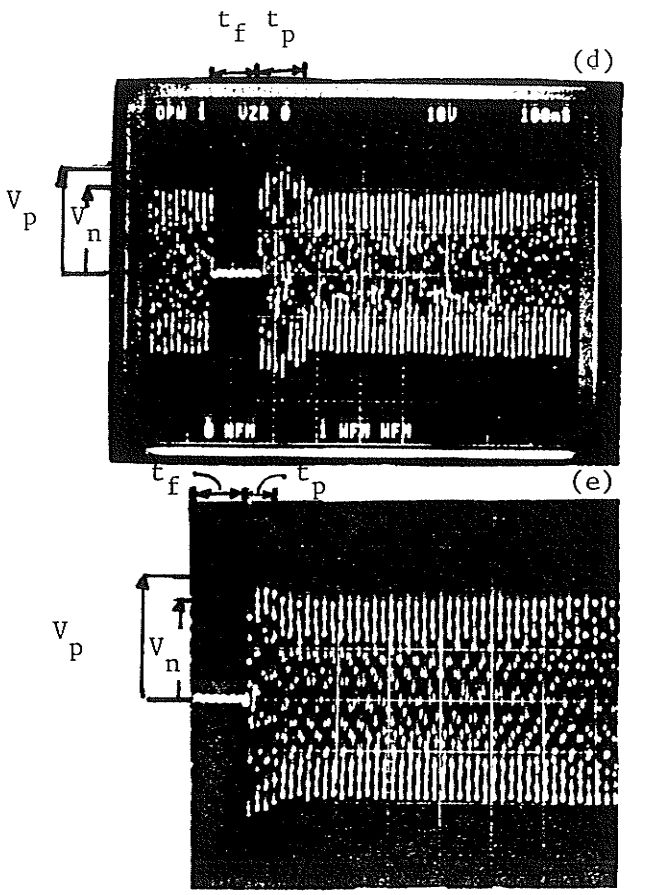
Harmonic	Resistance (Ohms)	Inductance (mH)	Capacitance (μF)
5th	1.1	41.4	6.8
7th	1.1	20.7	6.9
12th	46.9	15.55	7.1

Table A1.1(d) Parameters for the Controller on the Inverter Terminal.

S.No.	Type of Control	Integral Gain	Proportional Gain
1	Conventional Control		
	a) γ-control	10.0	0.8
	b) Current Control	40.0	0.75
2	P.F. Control	5.0	0.50
3	D.C. Voltage Control	10.0	0.60
4	A.C. Voltage Control	30.0	0.75
5	Reactive Power Control	15.0	0.60

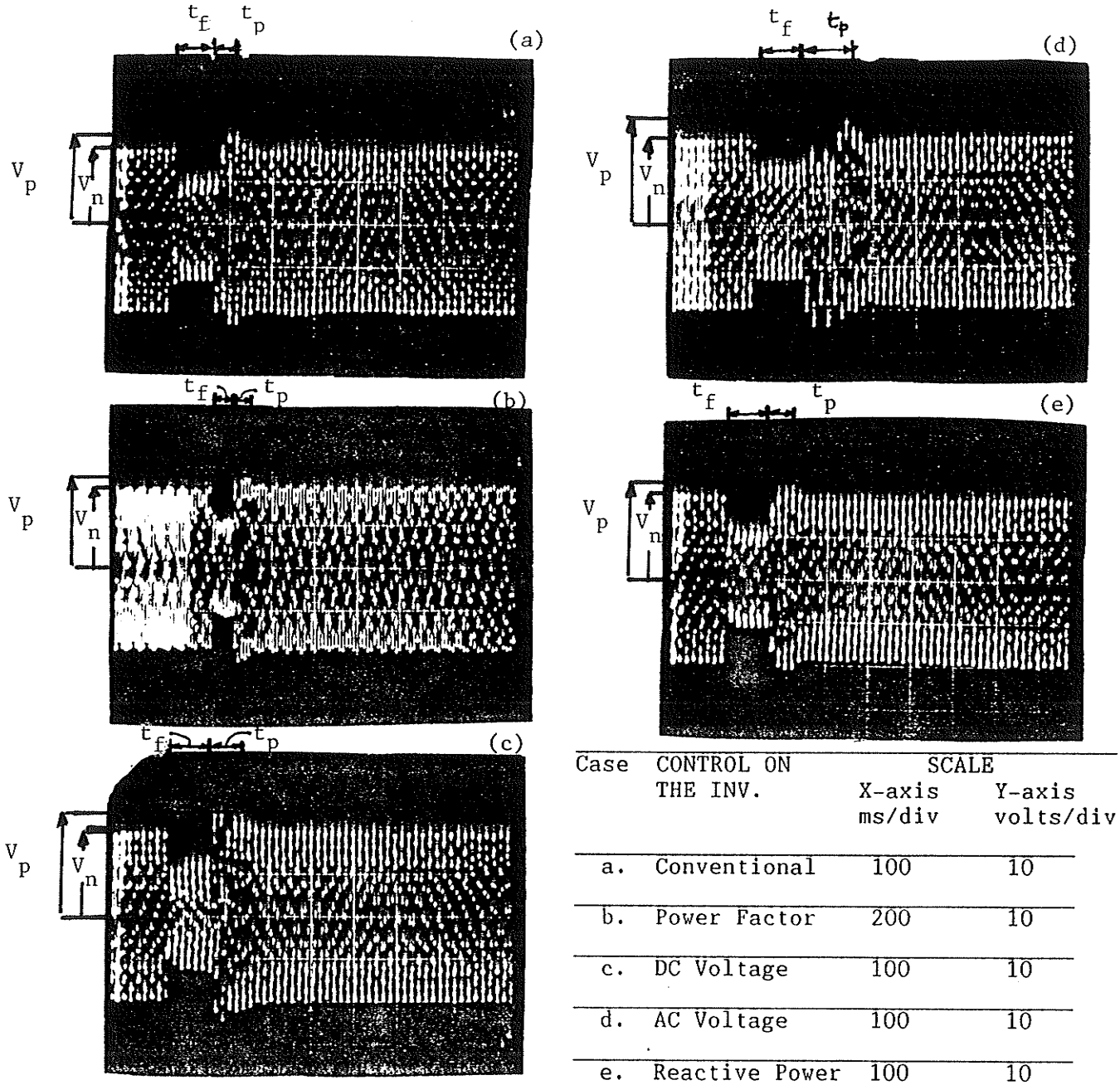
APPENDIX A2





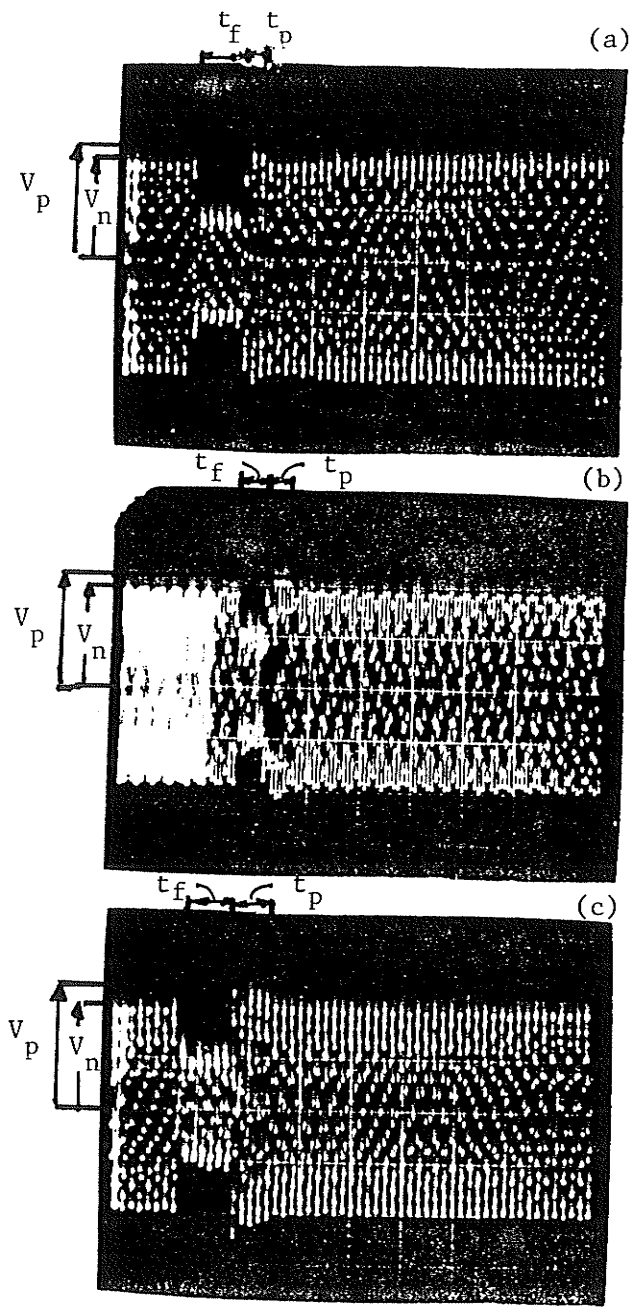
Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	200	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	100	10

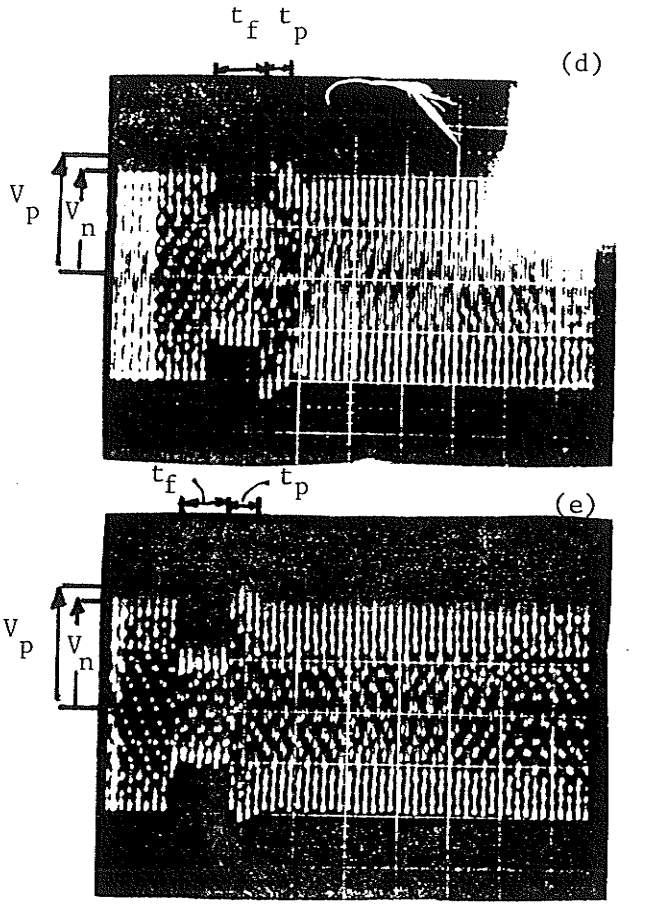
Figure A2.1 AC Voltage Response for the Single Phase To Ground Fault at the Inverter AC Bus



Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	200	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	100	10

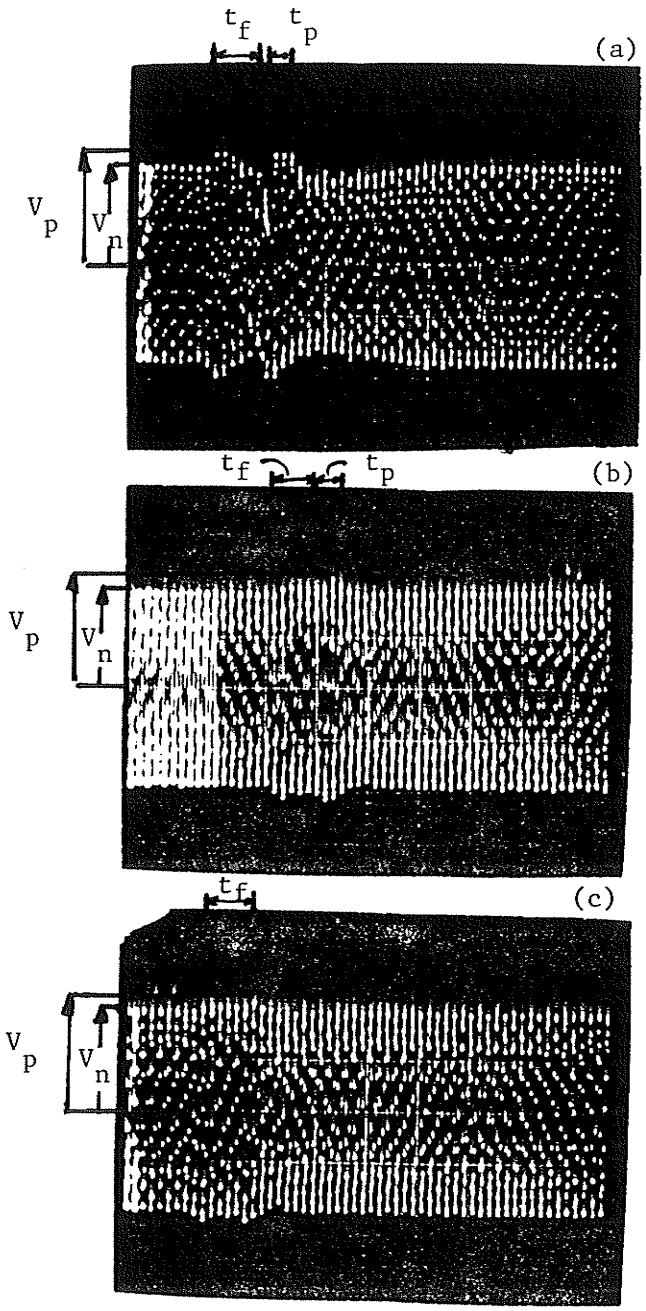
Figure A2.2 AC Voltage Response for the Remote Three Phase Fault on the Inverter AC System

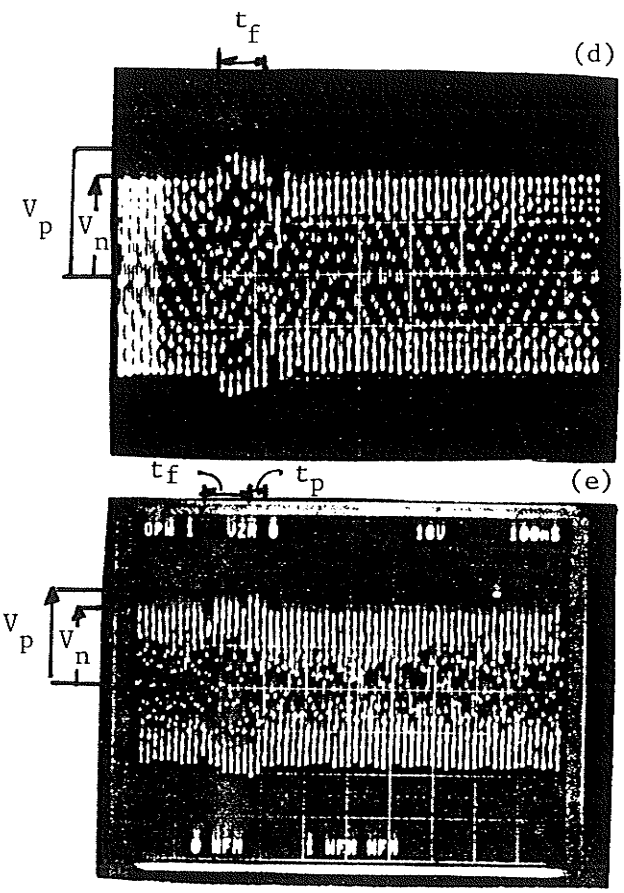




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	200	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	100	10

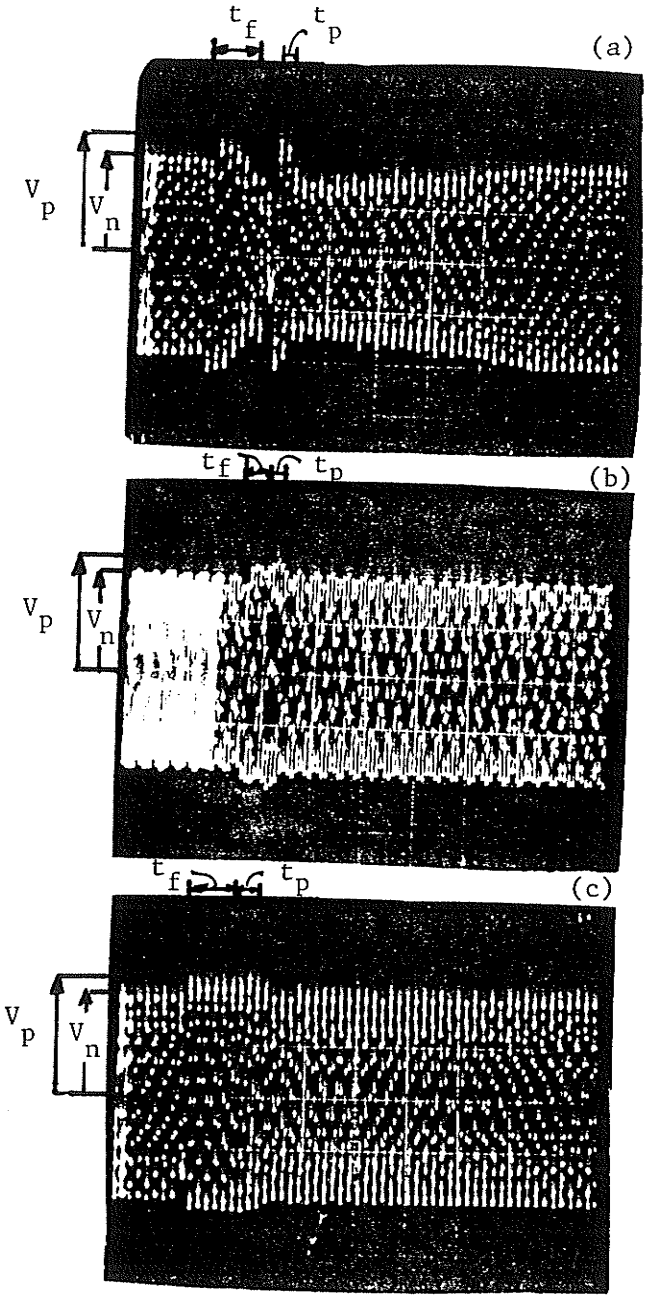
Figure A2.3 AC Voltage Response for the Remote Single Phase Fault on the Inverter AC System

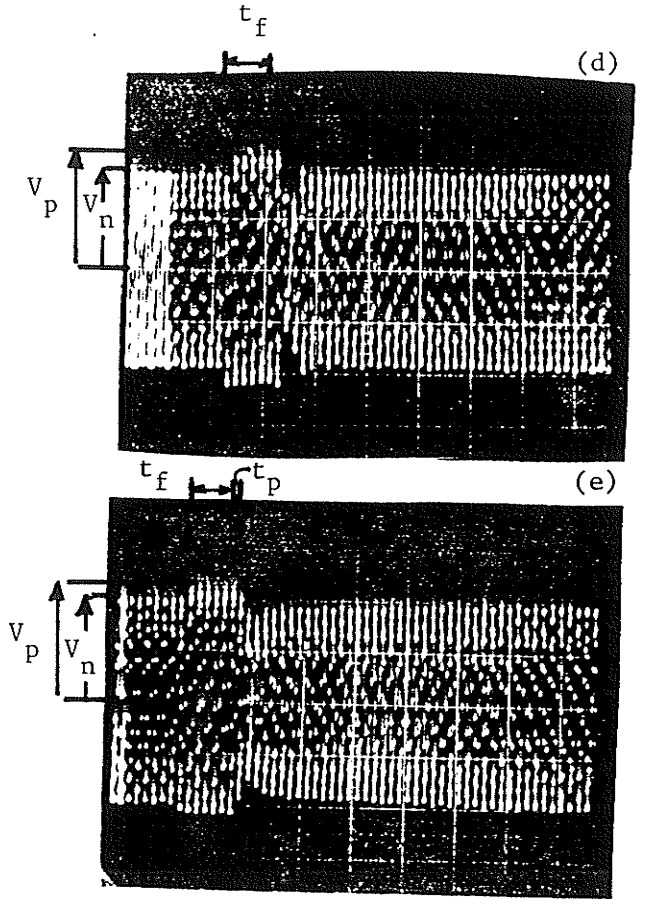




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	100	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	100	10

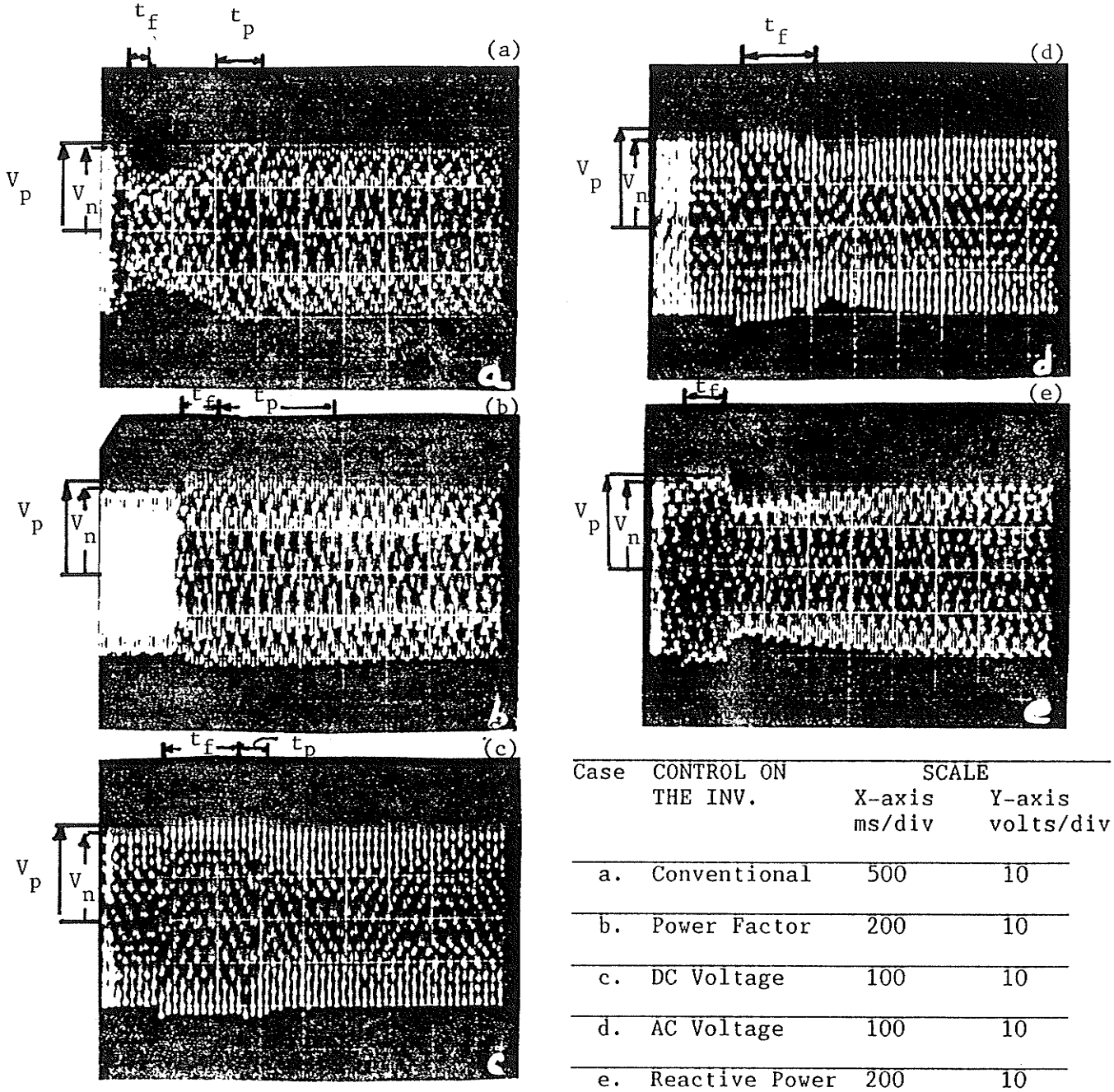
Figure A2.4 AC Voltage Response for the Single Phase to Ground Fault on the Rectifier AC System





Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	100	10
b.	Power Factor	200	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	100	10

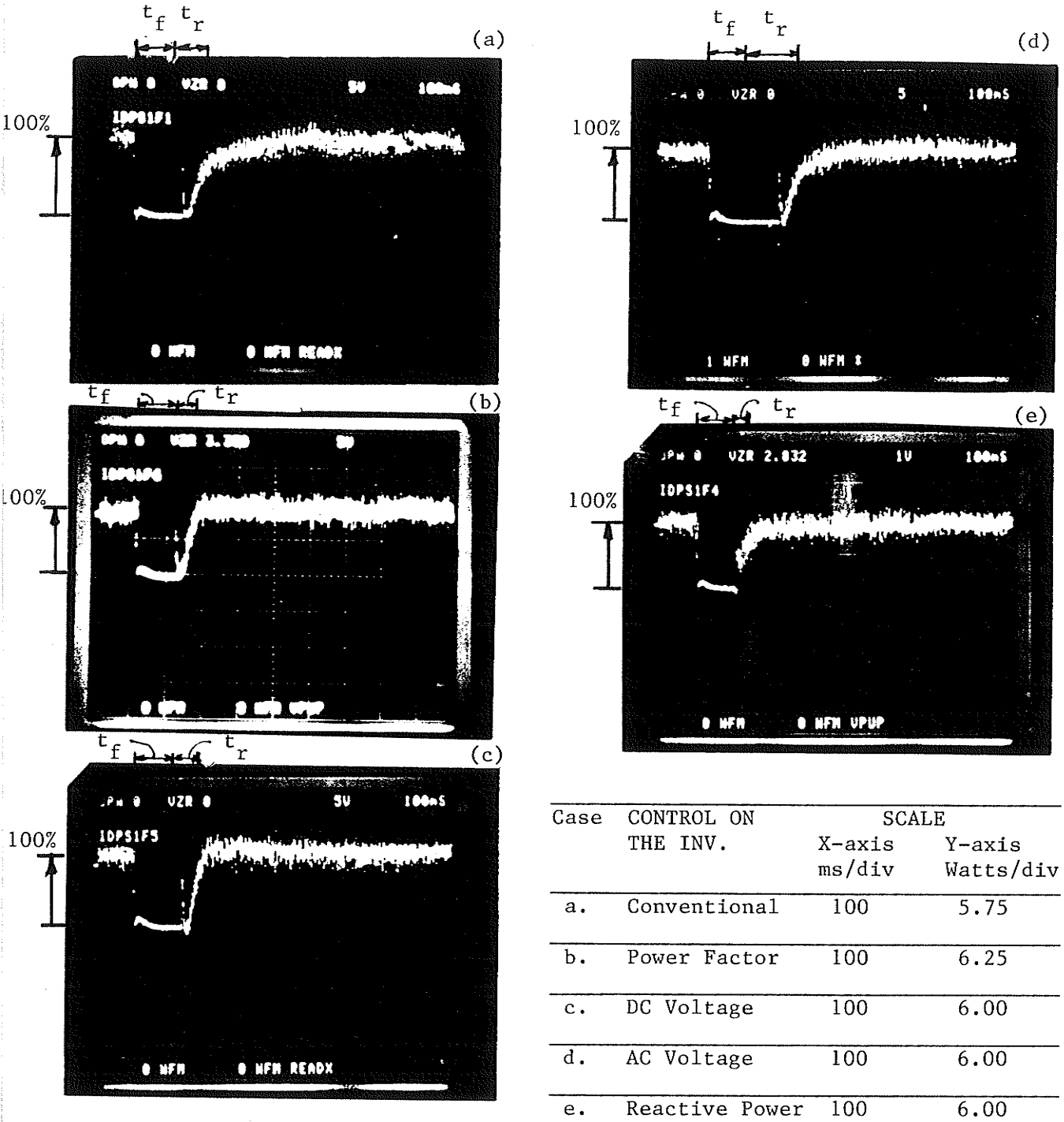
Figure A2.5 AC Voltage Response for the Three Phase to Ground Fault at the Rectifier AC Bus



Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis volts/div
a.	Conventional	500	10
b.	Power Factor	200	10
c.	DC Voltage	100	10
d.	AC Voltage	100	10
e.	Reactive Power	200	10

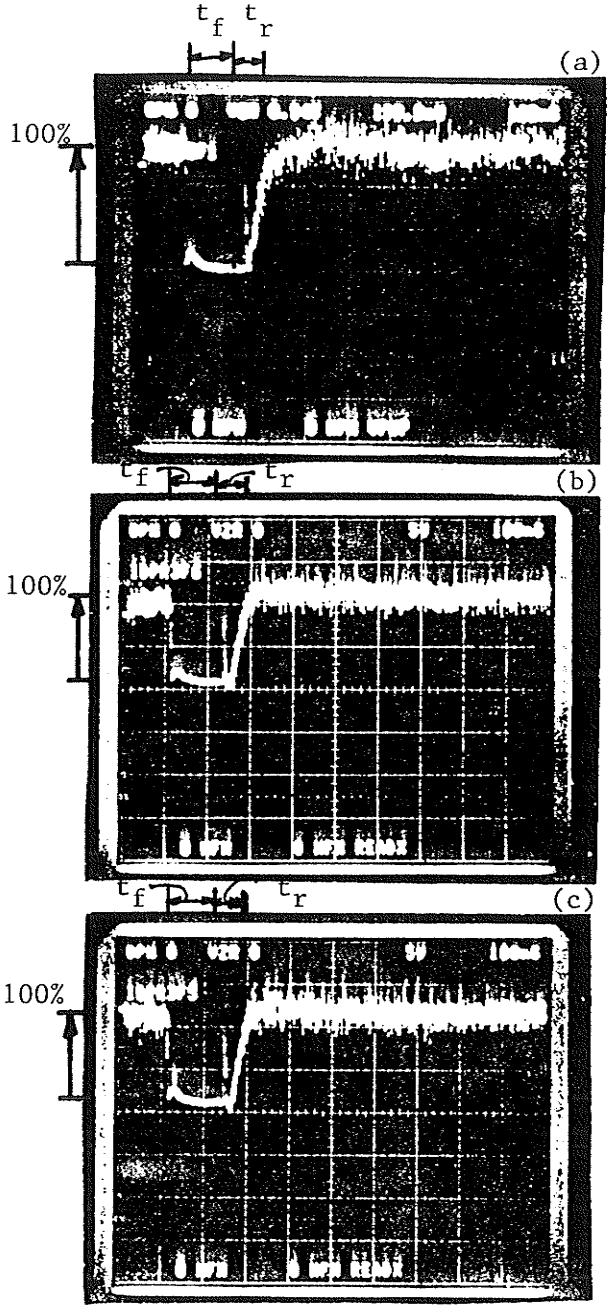
Figure A2.6 AC Voltage Response for the DC Fault at the Inverter Terminal

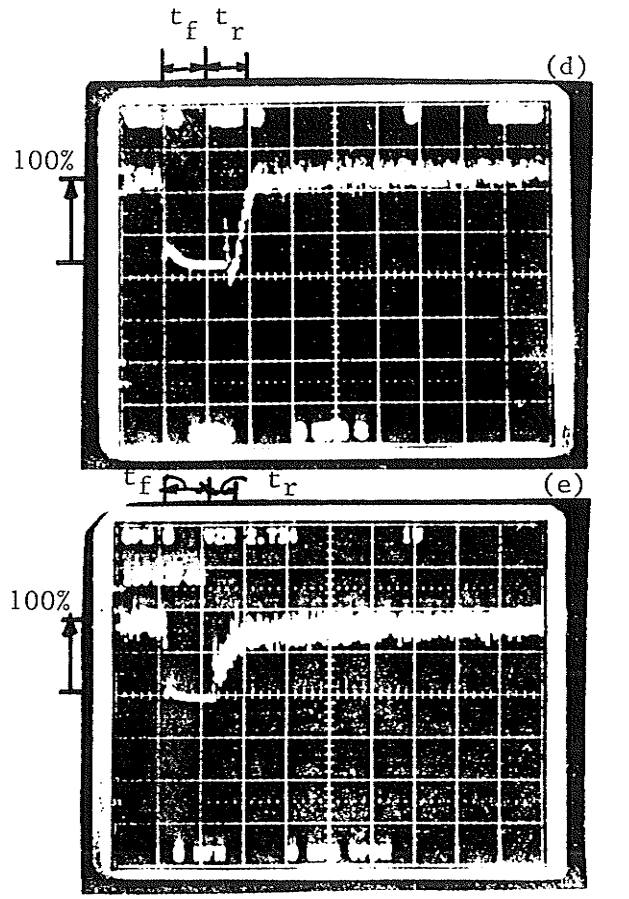
APPENDIX A3



Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	100	5.75
b.	Power Factor	100	6.25
c.	DC Voltage	100	6.00
d.	AC Voltage	100	6.00
e.	Reactive Power	100	6.00

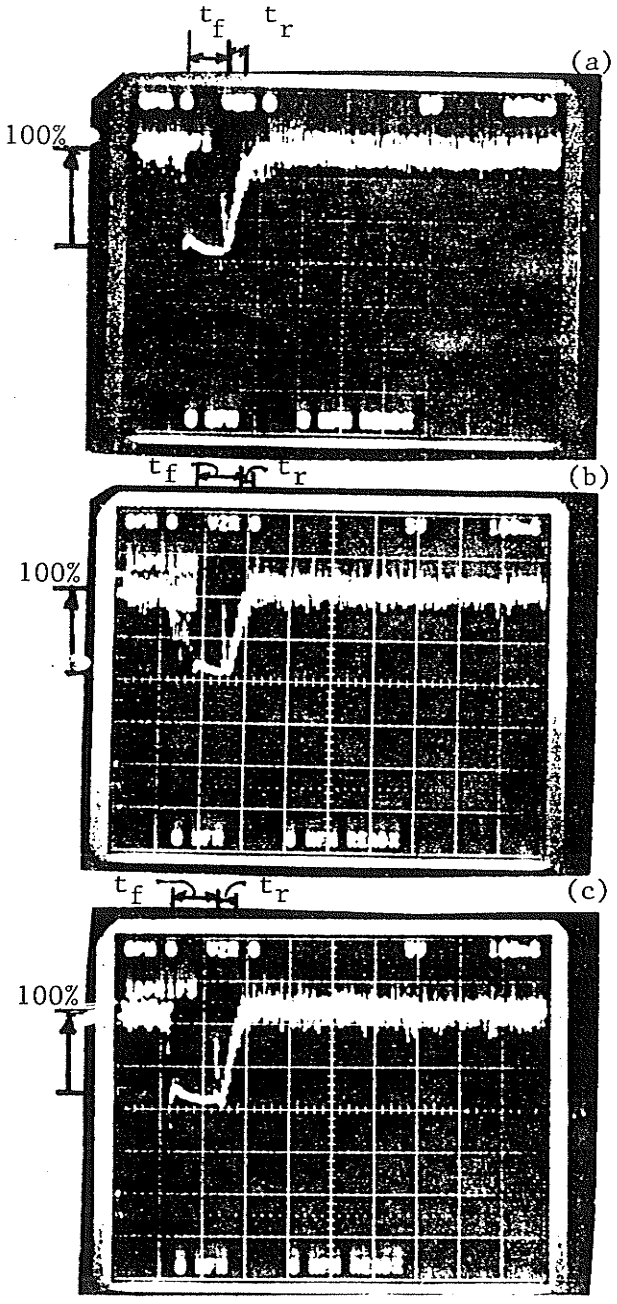
Figure A3.1 DC Power Recovery from the Single Phase to Ground Fault at the Inverter AC Bus

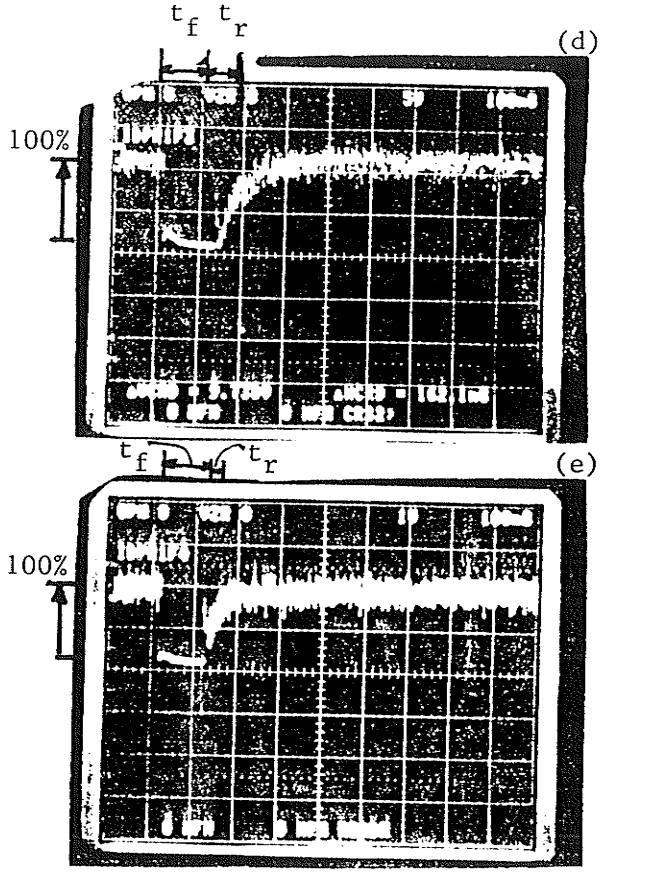




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	100	4.5
b.	Power Factor	100	6.0
c.	DC Voltage	100	6.0
d.	AC Voltage	100	6.0
e.	Reactive Power	100	6.50

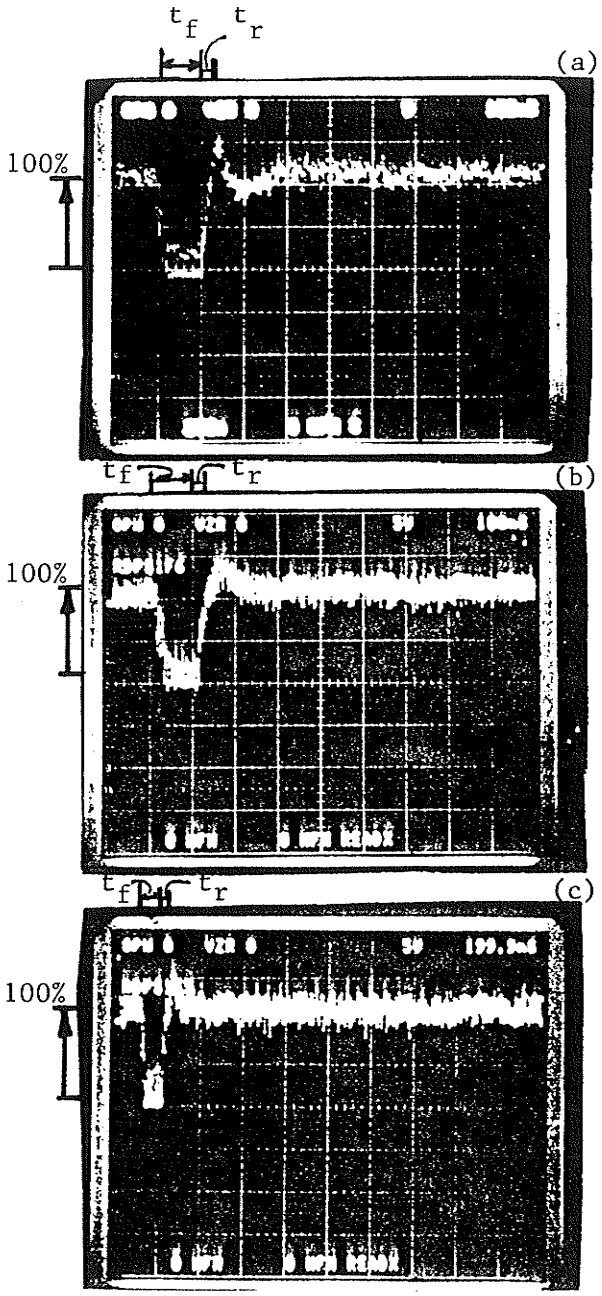
Figure A3.2 DC Power Recovery For the Remote Three Phase Fault at the Inverter AC System

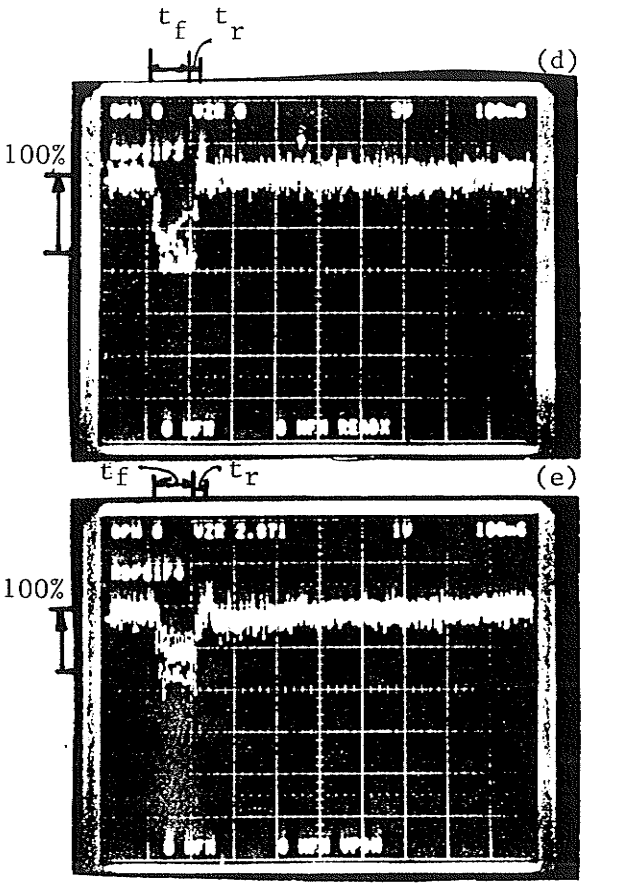




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	100	5.75
b.	Power Factor	100	6.0
c.	DC Voltage	100	6.0
d.	AC Voltage	100	6.0
e.	Reactive Power	100	6.25

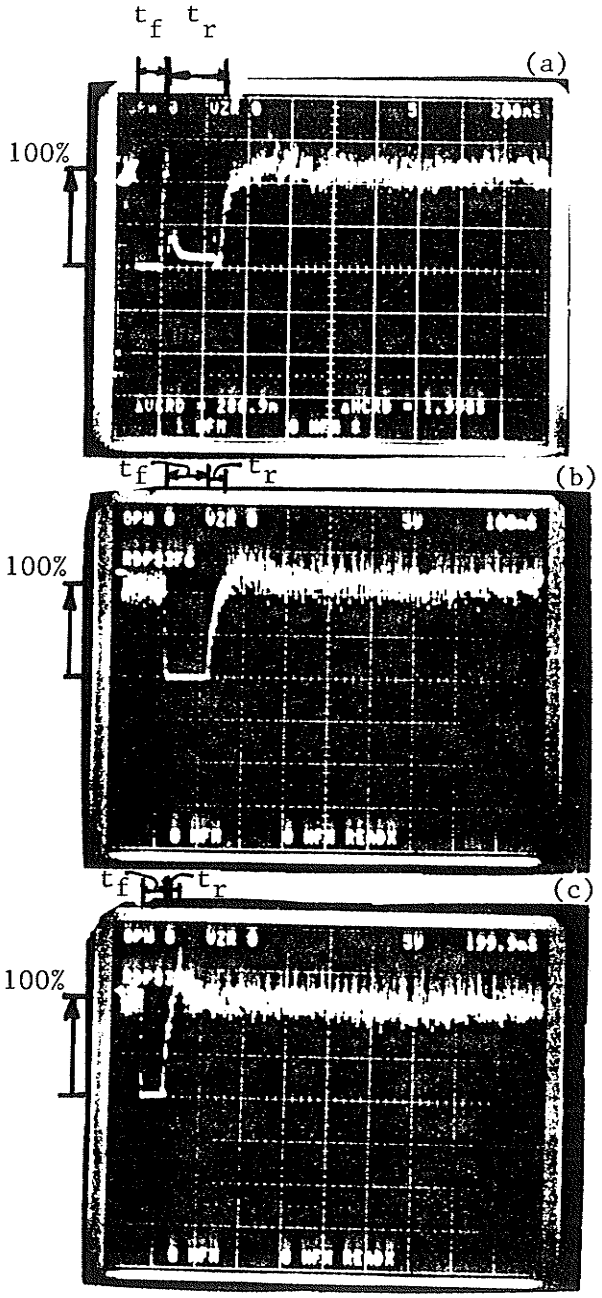
Figure A3.3 DC Power Recovery from the Remote Single Phase Fault on the Inverter AC System

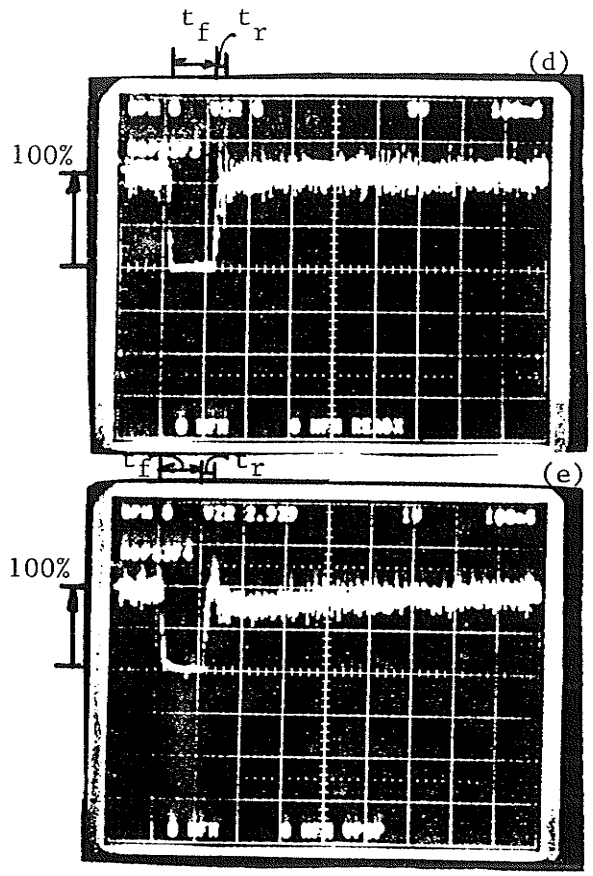




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	100	6.0
b.	Power Factor	100	6.0
c.	DC Voltage	200	6.0
d.	AC Voltage	100	6.0
e.	Reactive Power	100	6.50

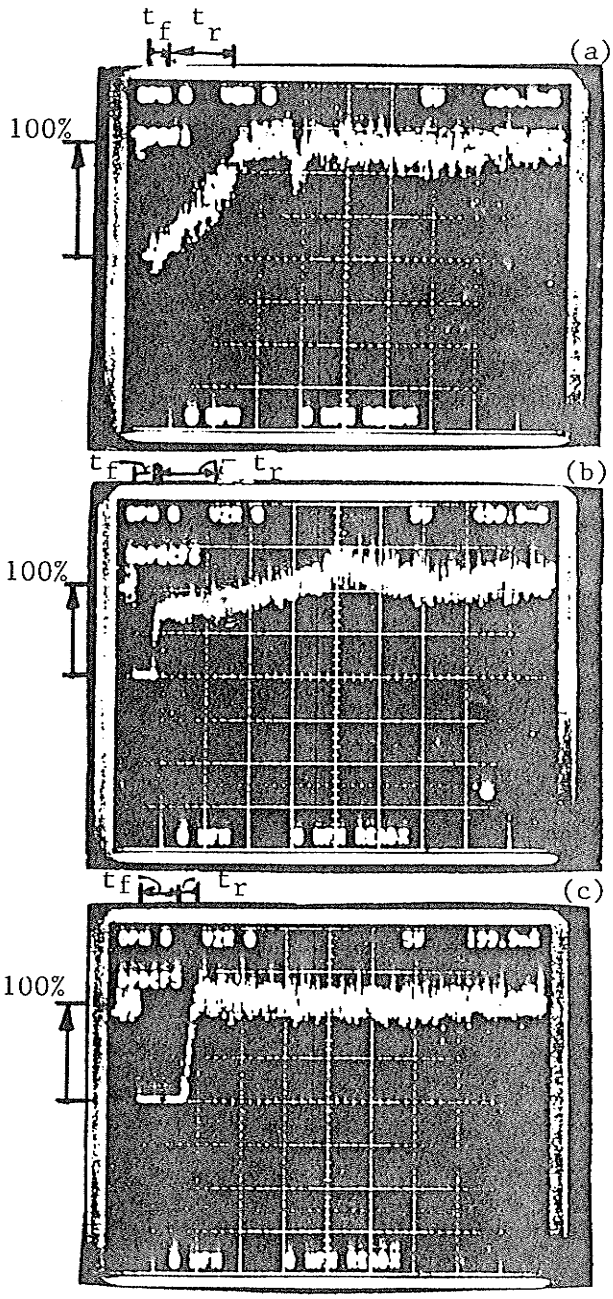
Figure A3.4 DC Power Recovery From the Single Phase to Ground Fault at the Rectifier AC Bus

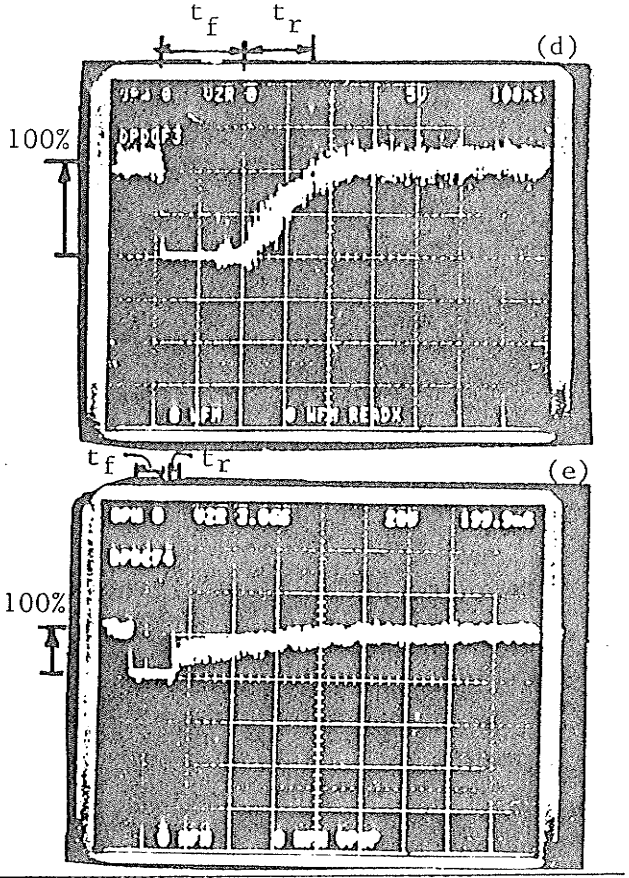




Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	200	6.0
b.	Power Factor	100	6.0
c.	DC Voltage	200	6.0
d.	AC Voltage	100	6.0
e.	Reactive Power	100	6.50

Figure A3.5 The DC Power Recovery for Three Phase to Ground Fault at the Rectifier AC Bus





Case	CONTROL ON THE INV.	SCALE X-axis ms/div	SCALE Y-axis Watts/div
a.	Conventional	500	5.0
b.	Power Factor	500	6.0
c.	DC Voltage	200	6.0
d.	AC Voltage	100	6.0
e.	Reactive Power	200	2.5

Figure A3.6 DC Power Recovery from the DC Line Fault at the Inverter Terminal

APPENDIX B1

Table B1.1(a) Data for the Receiving AC System.

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z Mag (Ohms)	Z Angle (deg)	SCP Mag. (MVA)	SCP Angle (deg)	L-L, Voltage (kv)	Filter Ratings (MVAR)
1.5	5.2074	523.81	0.0975	37.385	78	1415	78	230	200

Table B1.1(b) Data for the Sending AC System.

SCR	R1 (Ohms)	R2 (Ohms)	L2 (Henry)	Z Mag (Ohms)	Z Angle (deg)	SCP Mag. (MVA)	SCP Angle (deg)	L-L, Voltage (kv)	Filter Ratings (MVAR)
4.0	0.3059	180.16	0.0139	5.261	85	3620	85	138	200

Table B1.2 DC Filters at the Inverter and Rectifier Terminal.

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
6th	24.0	0.2444	0.80
12th	12.0	0.1222	0.40

Smoothing Reactor Inductance = 0.75 Henry.
Smoothing Reactor Resistance = 1.0 Ohms.

Table B1.3(a) AC Filters Components at the Inverter Bus.

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
5	14.22	0.2986	0.9425
7	14.22	0.2986	0.4810
11	5.32	0.0786	0.7395
13	5.32	0.0786	0.5280
HP	94.80	0.0072	2.2795

Total MVAR Supplied by Filters = 200 MVAR
Number of Each Filter = 2

Table B1.3(b) AC Filters Components at the Rectifier Bus.

Filter Tuned (Frequency)	Resistance (Ohms)	Inductance (Henry)	Capacitance (μf)
5	5.37	0.1094	2.5725
7	5.37	0.1094	1.3130
11	3.56	0.0207	2.1570
13	3.56	0.0207	1.544
HP	47.20	0.0026	6.1790

Total MVAR Supplied by Filters = 200 MVAR
Number of Each Filter = 2

APPENDIX B2

Table B2.1 Controller Settings for Three Phase to Ground Fault at the Inverter Bus.

Name of Control Scheme	K_p	K_I	T_a	T_b	Remarks
PFC	0.60	9.0	0.10	0.02	For conventional
AVC	0.65	18.00	0.06	0.01	control Y_s = 0.3,
DVC	0.20	3.00	0.03	0.01	Y_L = 0.5 has been
RCC	0.30	4.50	0.10	0.02	used.
RPC	0.250	5.50	0.05	0.01	

Table B2.2 Controller Settings for Single Phase to Ground Fault at the Inverter Bus.

Name of Control Scheme	K_p	K_I	T_a	T_b	Remarks
PFC	0.50	12.00	0.10	0.01	For conventional
AVC	0.45	30.00	0.10	0.03	control Y_s = 0.5,
DVC	0.30	4.50	0.10	0.01	Y_L = 0.70.
RCC	0.60	15.00	0.10	0.01	
RPC	0.70	8.00	0.10	0.01	

PFC: Power Factor Control
RCC: Reactive Current Control
AVC: AC Voltage Control
DVC: DC Voltage Control
RPC: Reactive Power Control

Table B2.3 Controller Settings for DC Line Fault.

Name of Control Scheme	K_p	K_I	T_a	T_b	Remarks
PFC	0.5	10.5	0.10	0.01	For conventional
AVC	0.40	40.0	0.10	0.03	control Y_s = 0.35,
DVC	0.35	5.0	0.10	0.01	Y_L = 0.55.
RCC	0.80	18.00	0.10	0.03	
RPC	0.85	9.00	0.05	0.02	

Table B2.4 Controller Settings for Three Phase to Ground Fault at the Rectifier Bus.

Name of control Scheme	K_p	K_I	T_a	T_b	Remarks
PFC	0.40	12.00	0.10	0.01	For conventional
AVC	0.50	38.00	0.07	0.01	control
DVC	0.40	7.00	0.10	0.01	Y_s = 0.3330,
RCC	0.75	16.00	0.10	0.02	Y_L = 0.450.
RPC	0.70	11.00	0.10	0.01	

PFC: Power Factor Control
RCC: Reactive Current Control
AVC: AC Voltage Control
DVC: DC Voltage Control
RPC: Reactive Power Control

APPENDIX B3

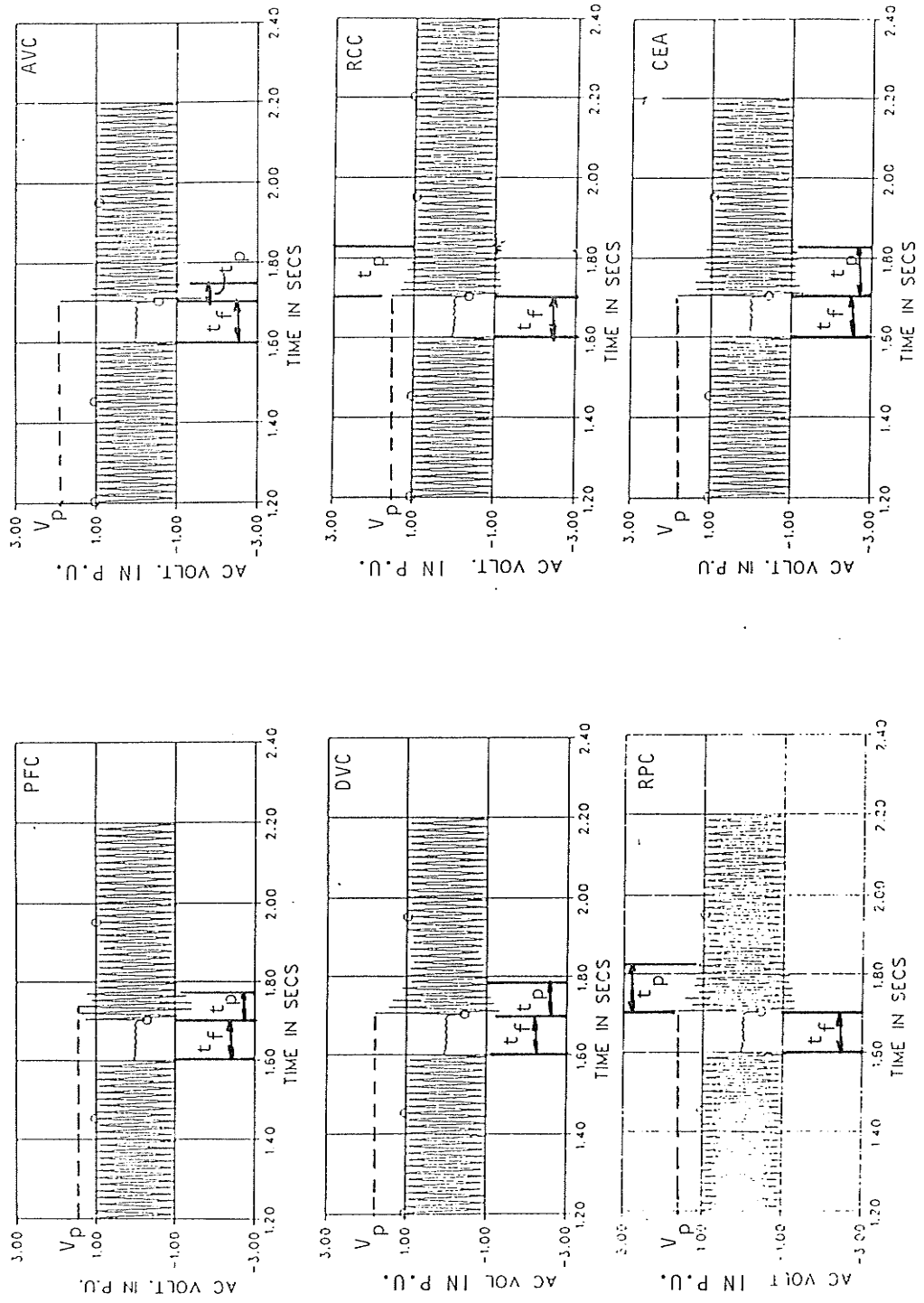


Figure B3.1 Instantaneous AC Voltage Response for the Single Phase to Ground Fault at the Inverter Bus

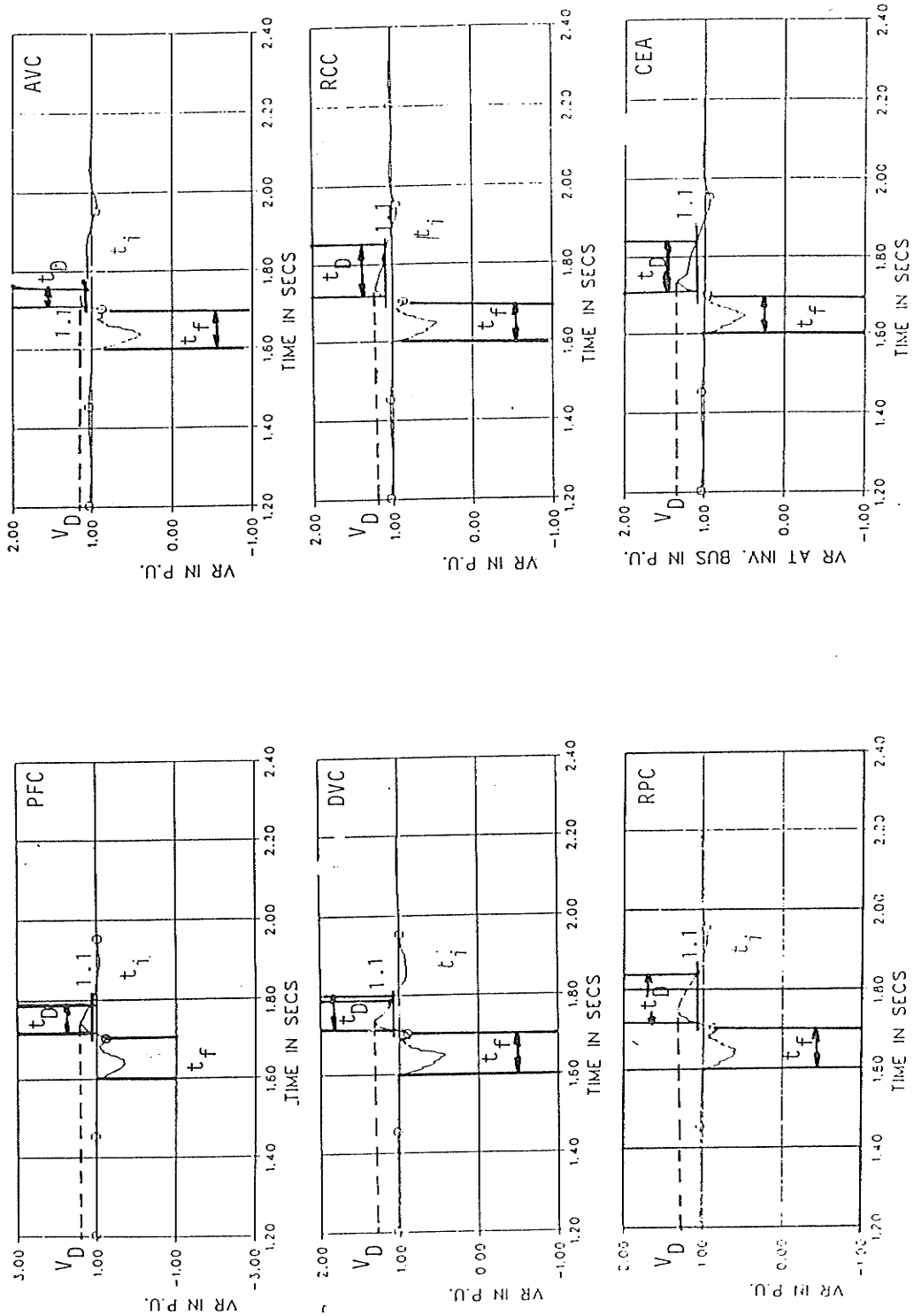


Figure B3.2 Three Phase RMS Voltage Response for the Single Phase to Ground Fault at the Inverter Bus

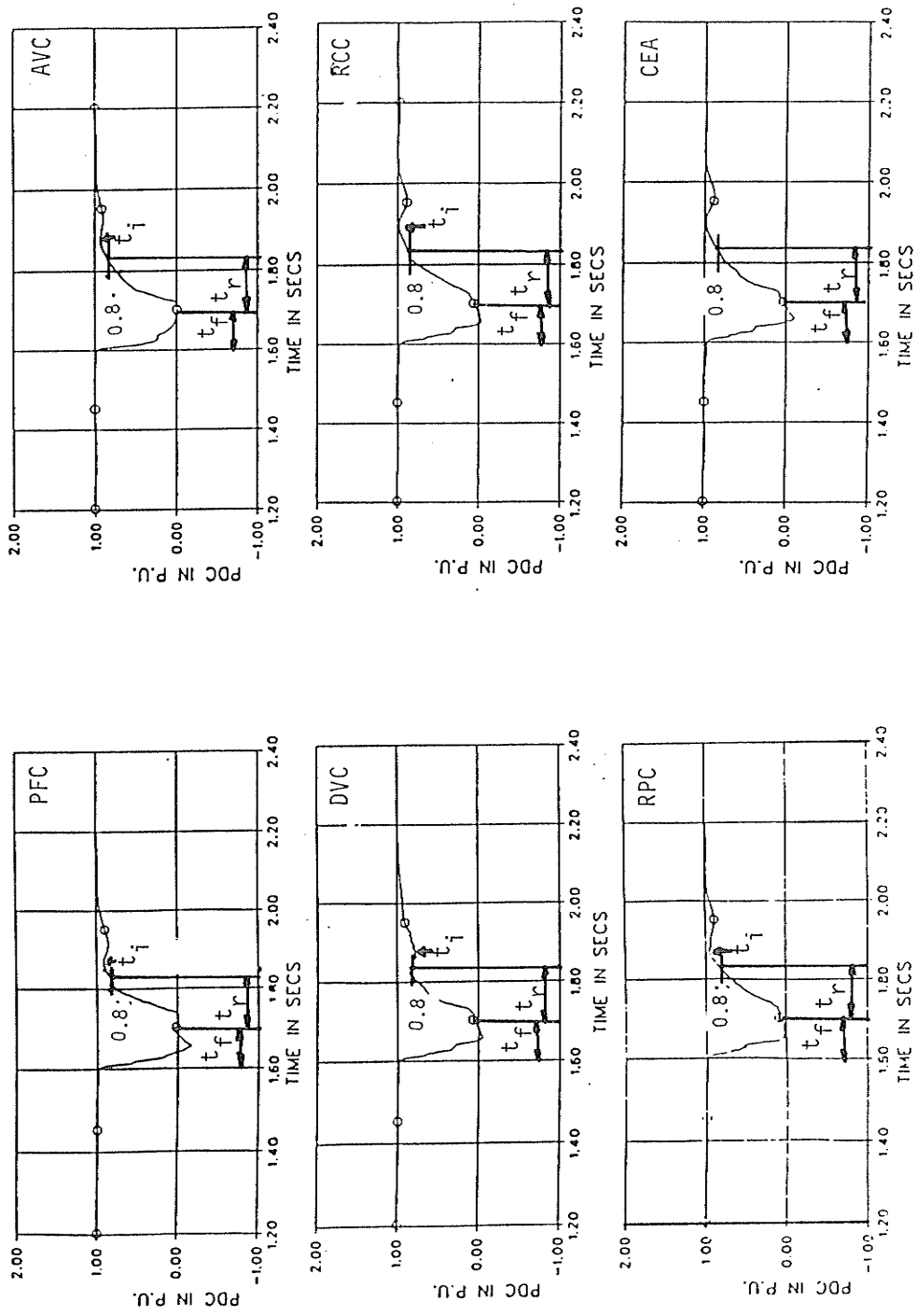


Figure B3.3 DC Power Recovery from the Single Phase to Ground Fault at the Inverter Bus

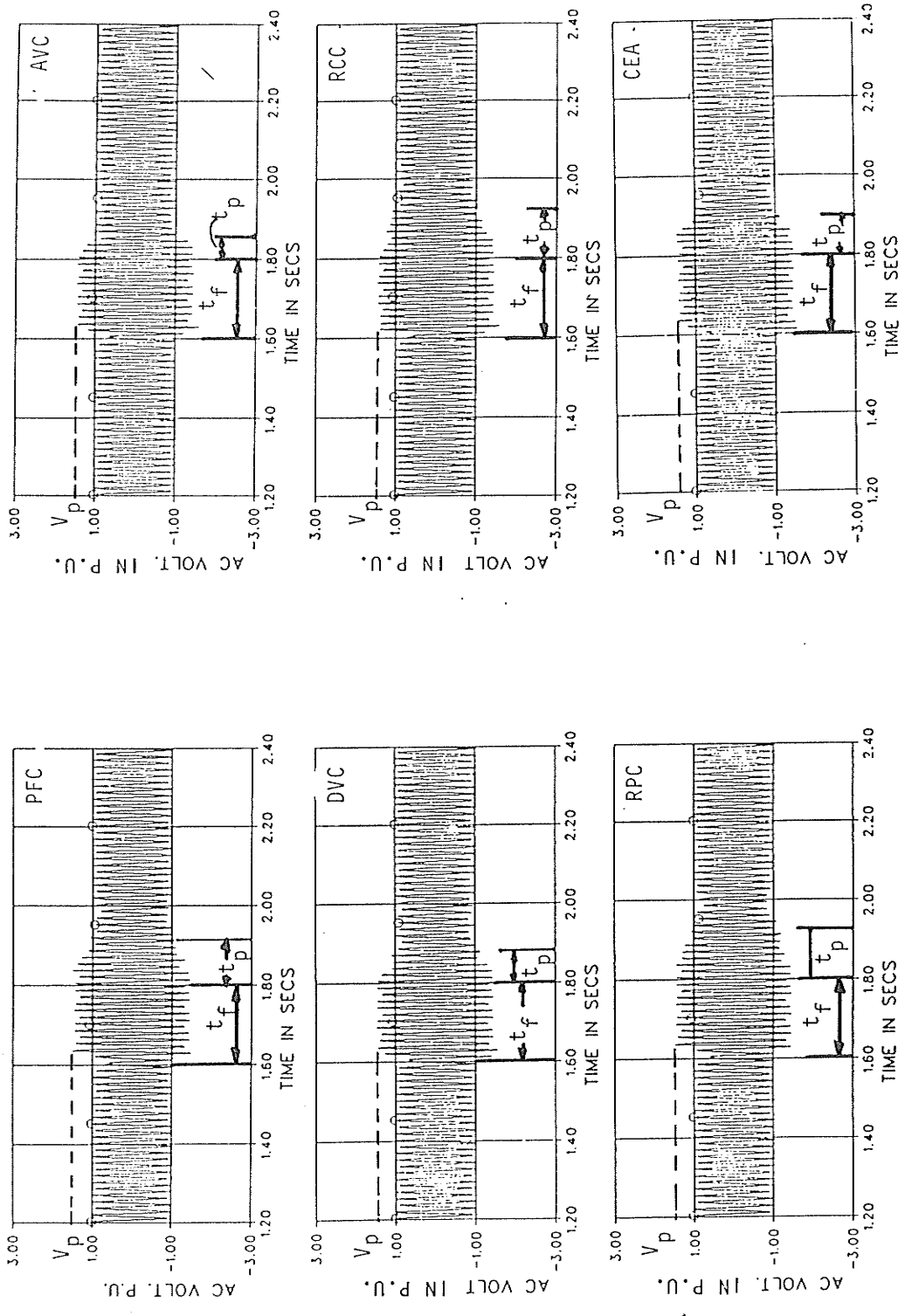


Figure B3.4 Instantaneous AC Voltage Response for the DC Line Fault at the Inverter Terminal

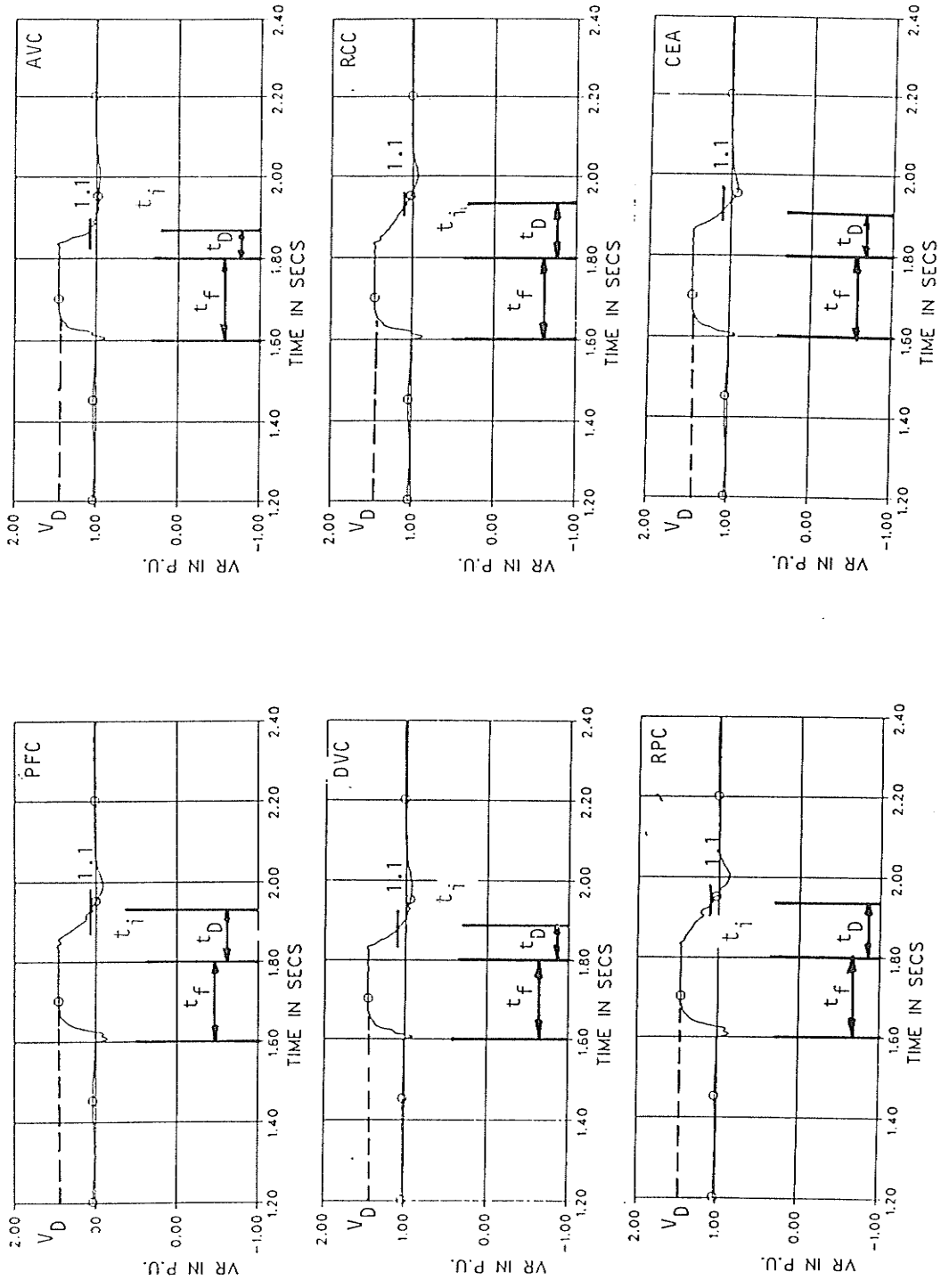


Figure B3.5 Three Phase RMS Voltage Response for the DC Line Fault at the Inverter Terminal

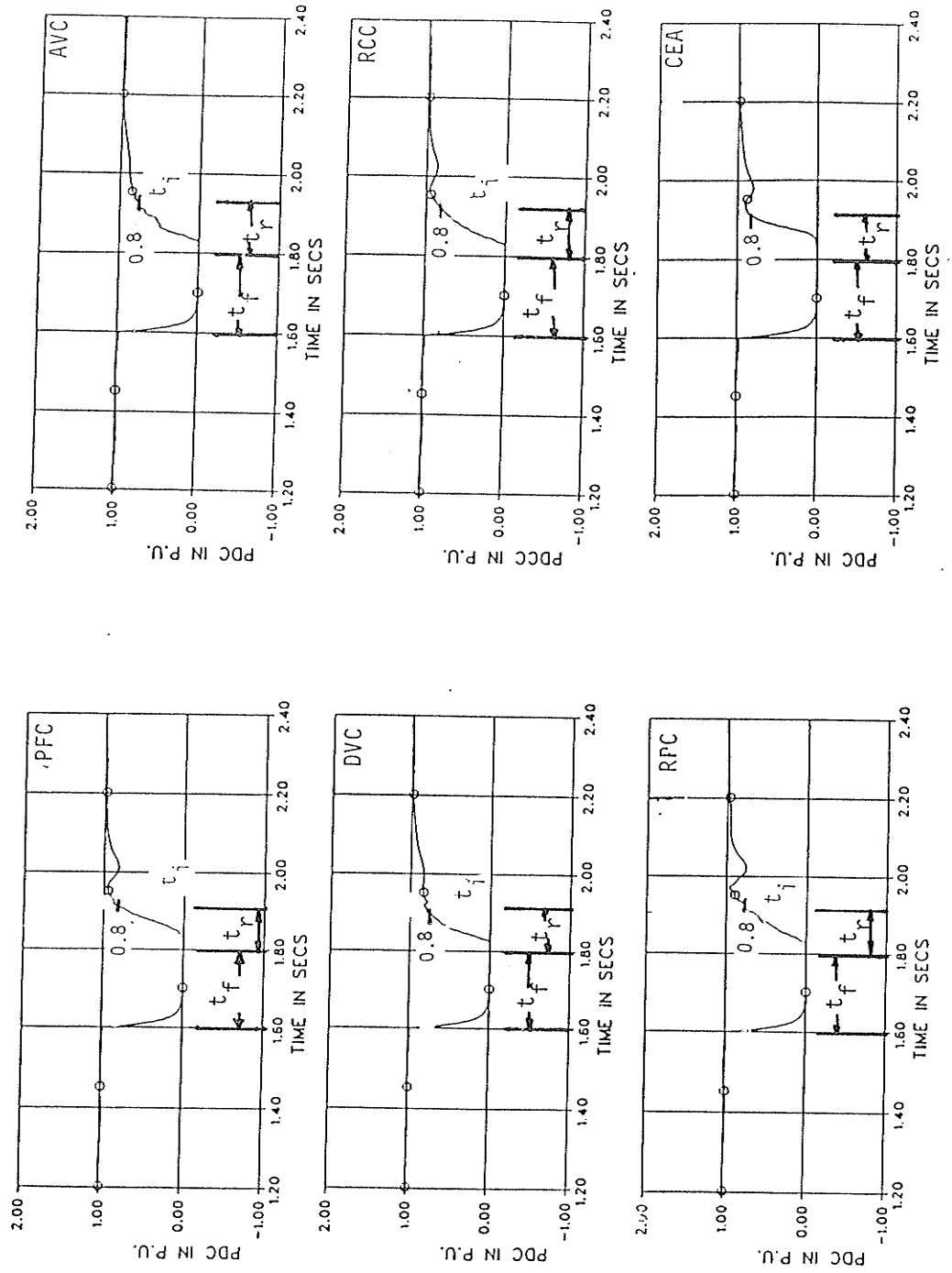


Figure B3.6 DC Power Recovery from DC Fault at the Inverter Terminal

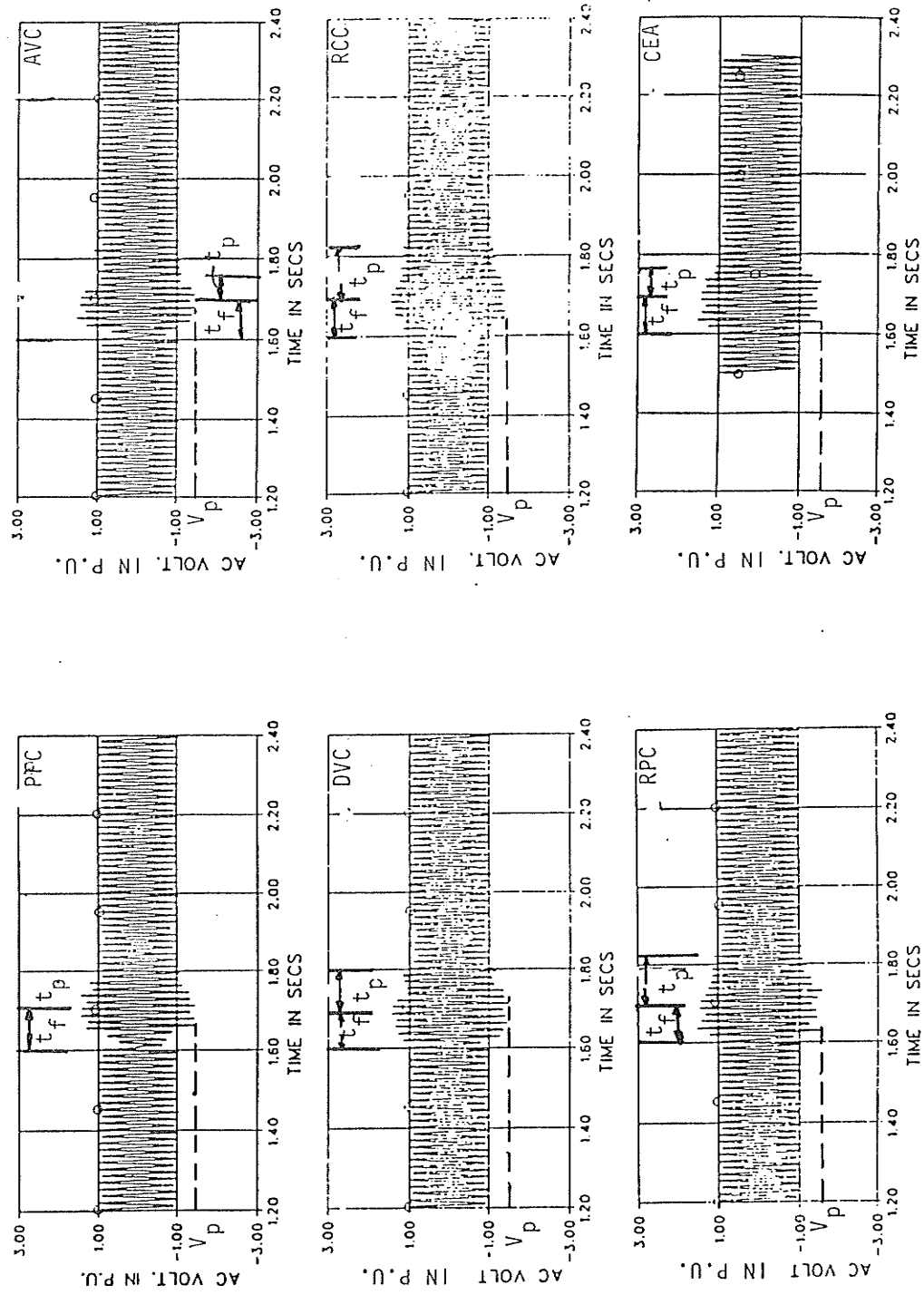


Figure B3.7 Instantaneous AC Voltage Response for the Three Phase to Ground Fault at the Rectifier Bus

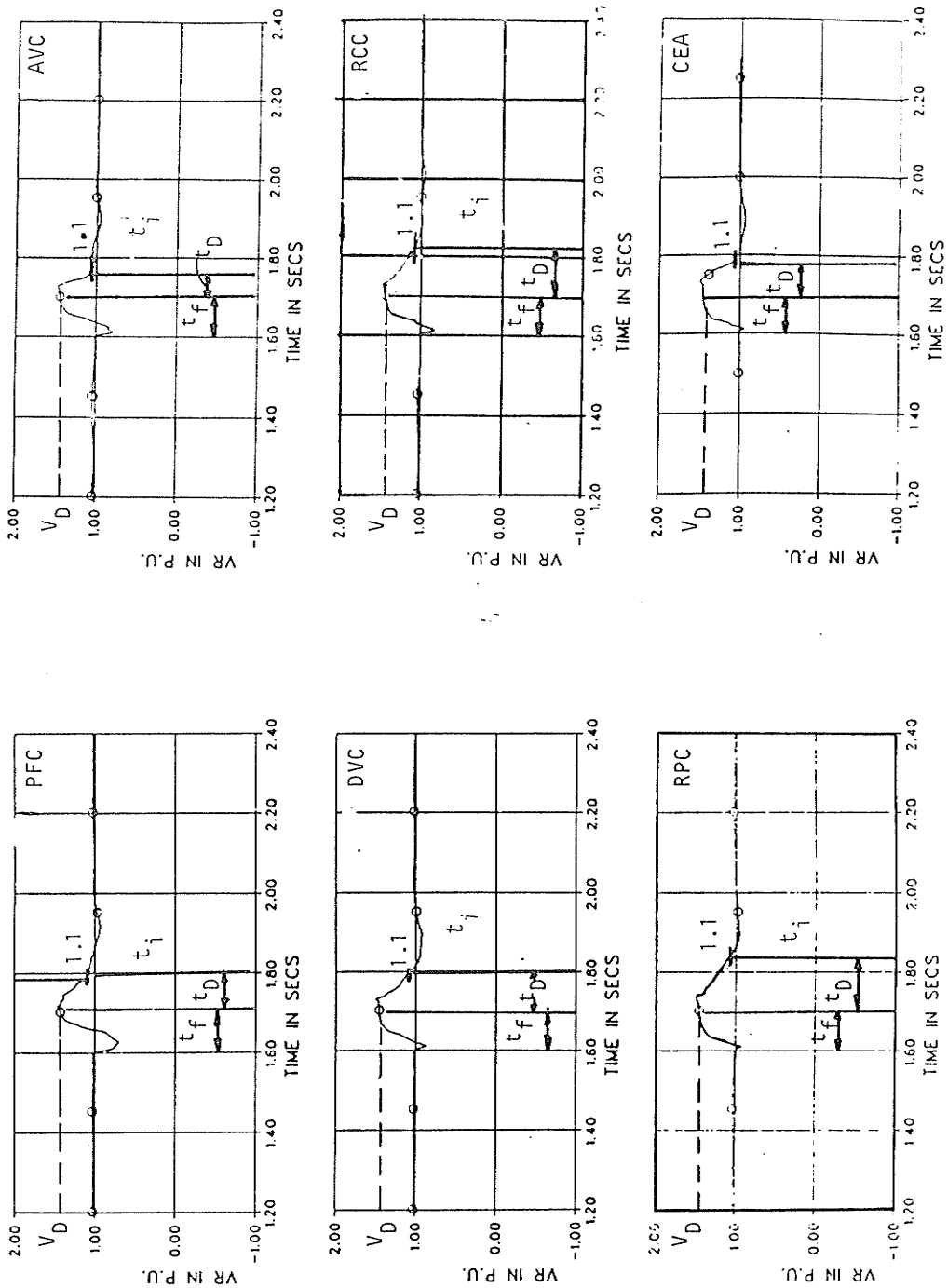


Figure B3.8 Three Phase RMS Voltage Response for the Three Phase Fault at the Rectifier Bus

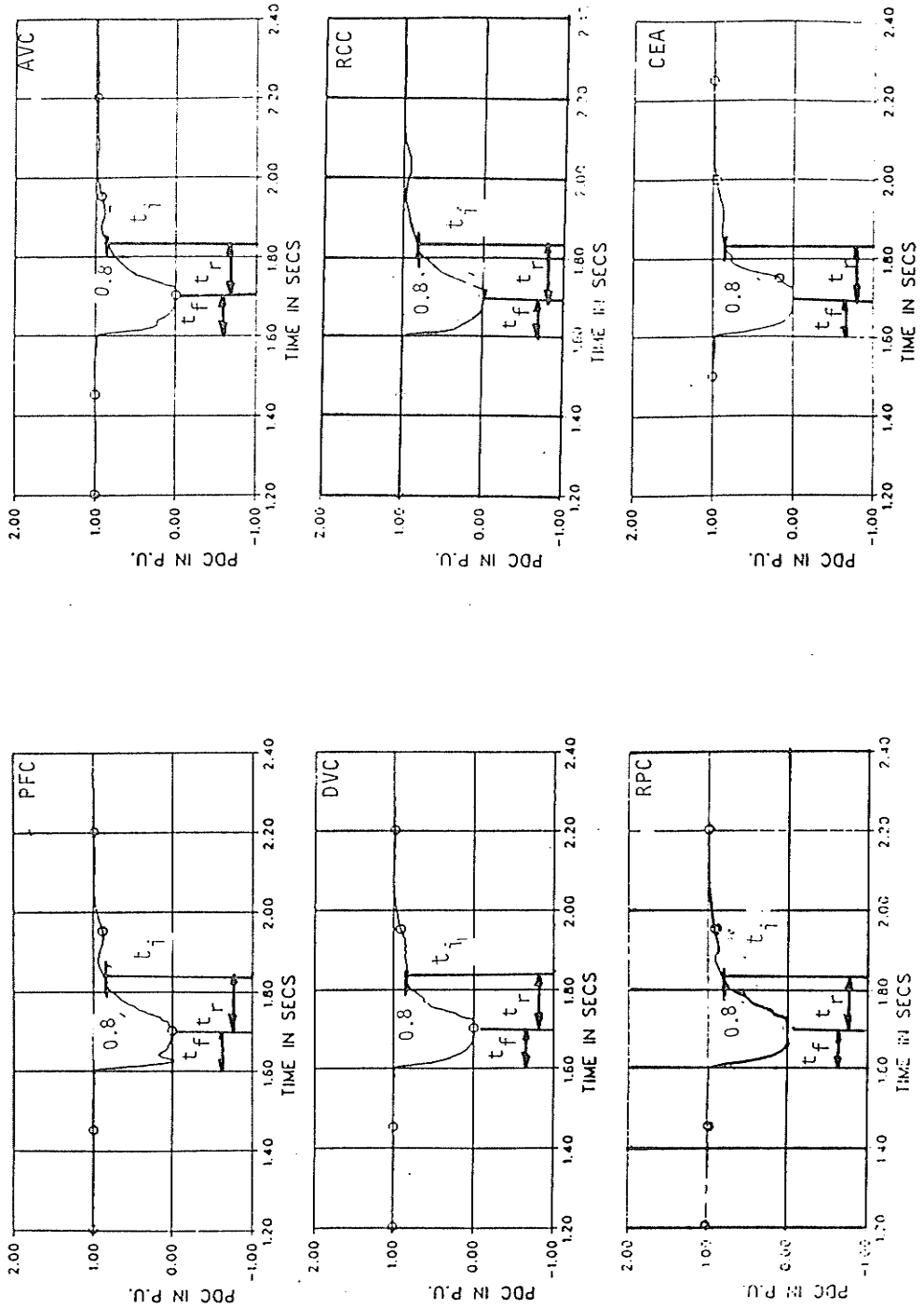
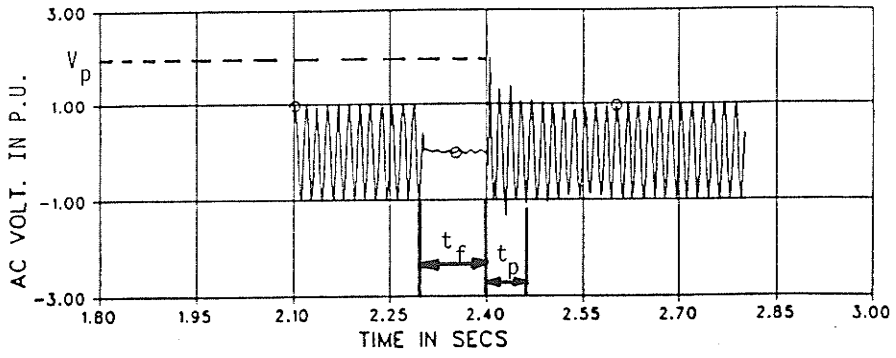
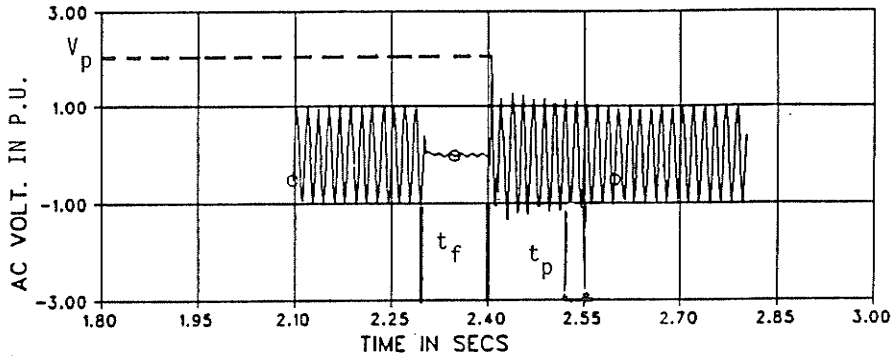


Figure B3.9 DC Power Recovery from the Three Phase To Ground Fault at the Rectifier Bus

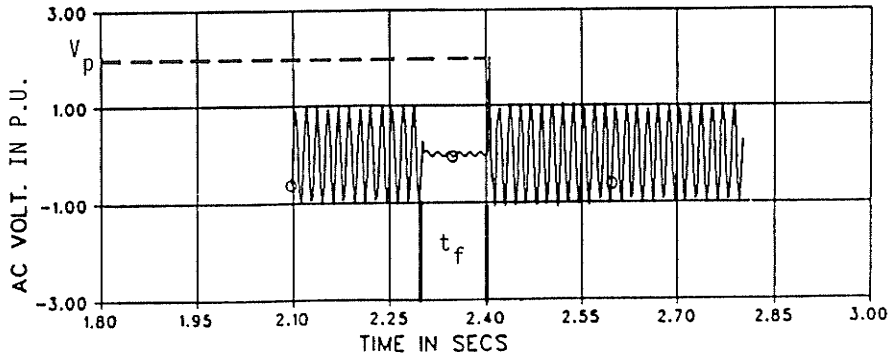
APPENDIX C



Case (a)

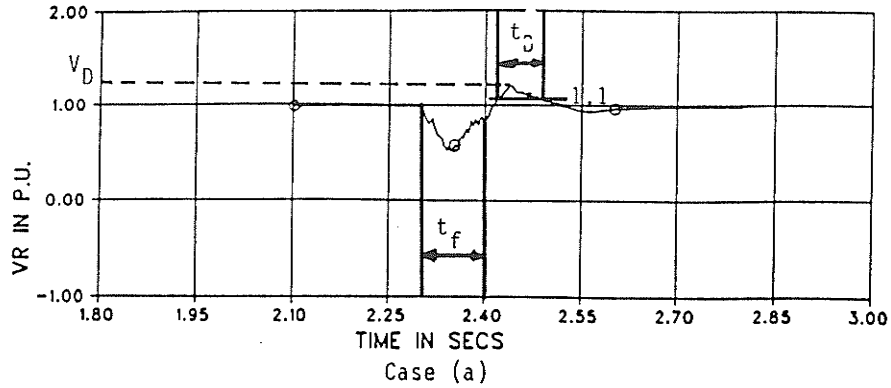


Case (b)

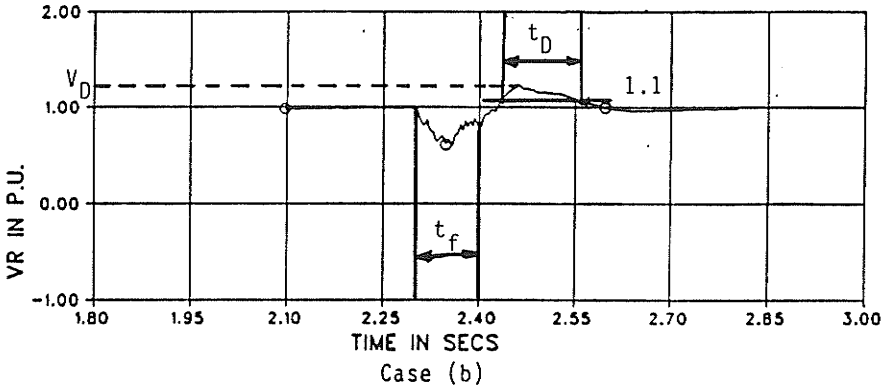


Case (c)

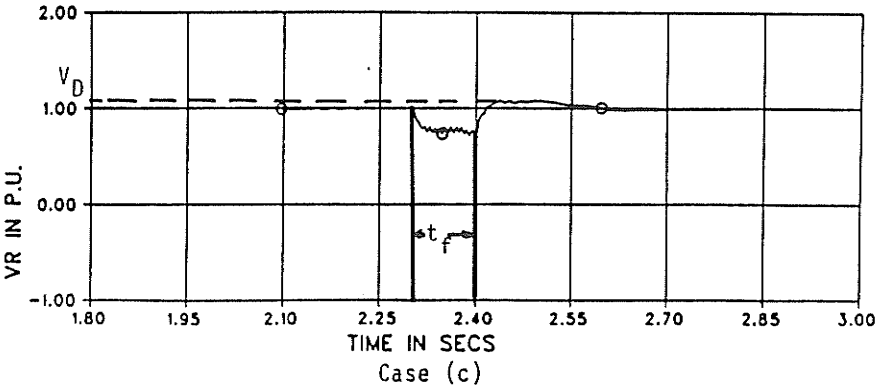
Figure C.1 Instantaneous AC Voltage Response for the Single Phase to Ground Fault at the Inverter Bus



Case (a)

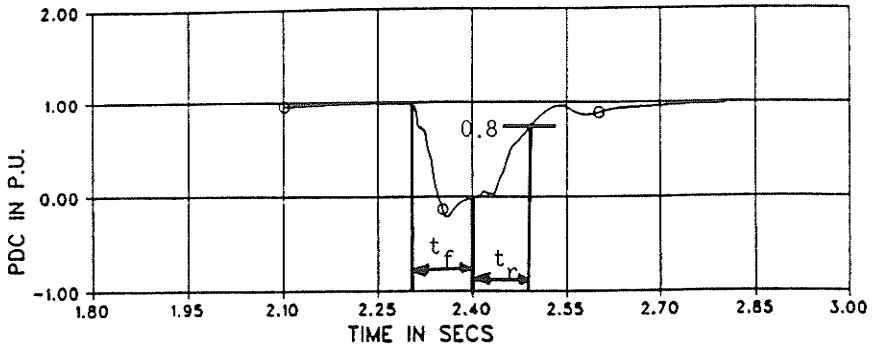


Case (b)

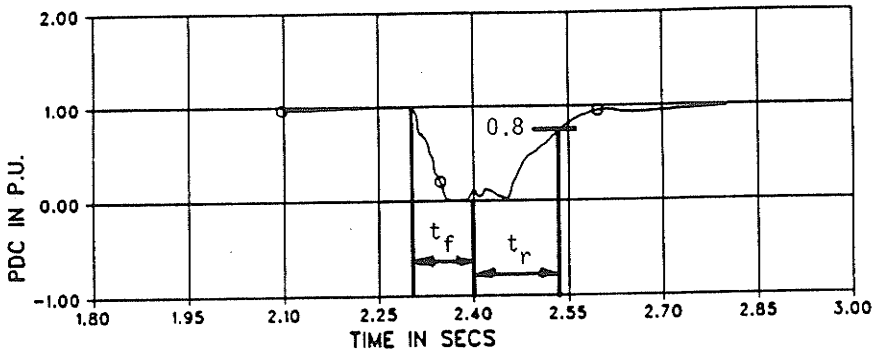


Case (c)

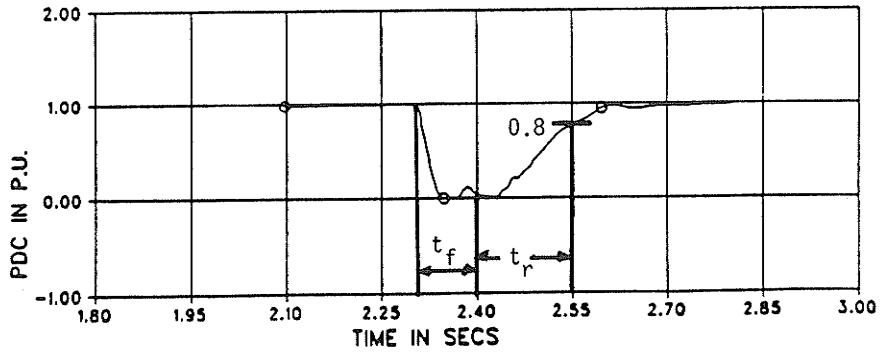
Figure C.2 Three Phase RMS Voltage Response for the Single Phase to Ground Fault at the Inverter Terminal



Case (a)

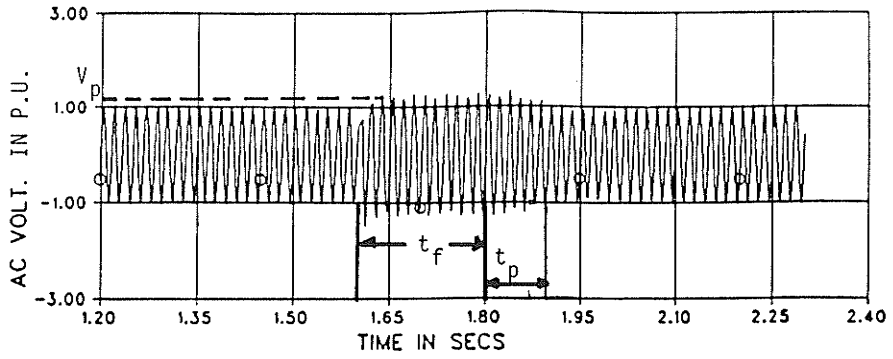


Case (b)

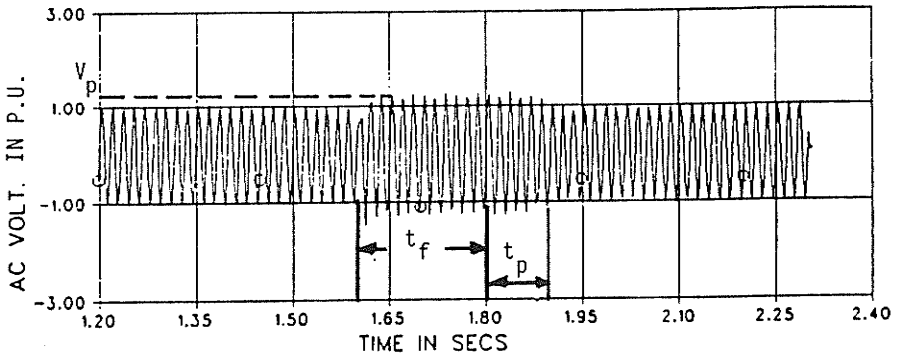


Case (c)

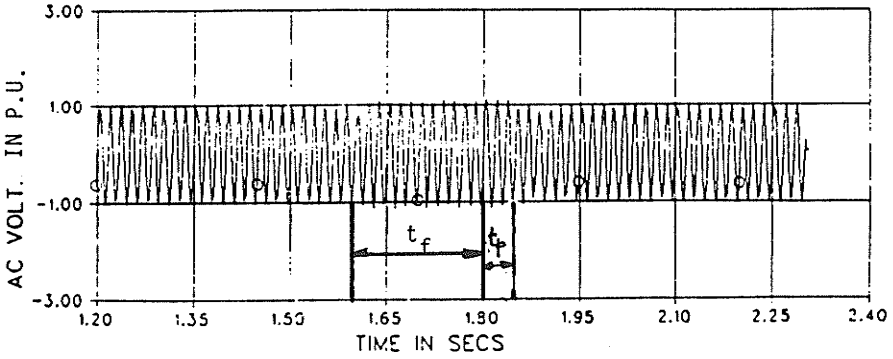
Figure C.3 DC Power Recovery from the Single Phase to Ground Fault at the Inverter Bus



Case (a)

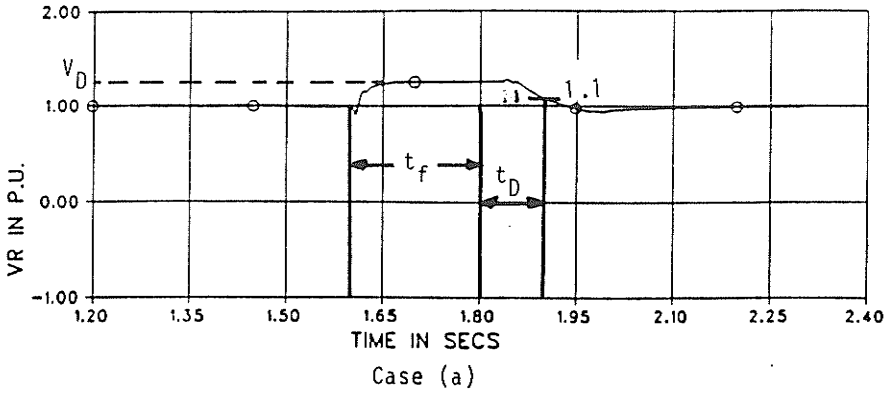


Case (b)

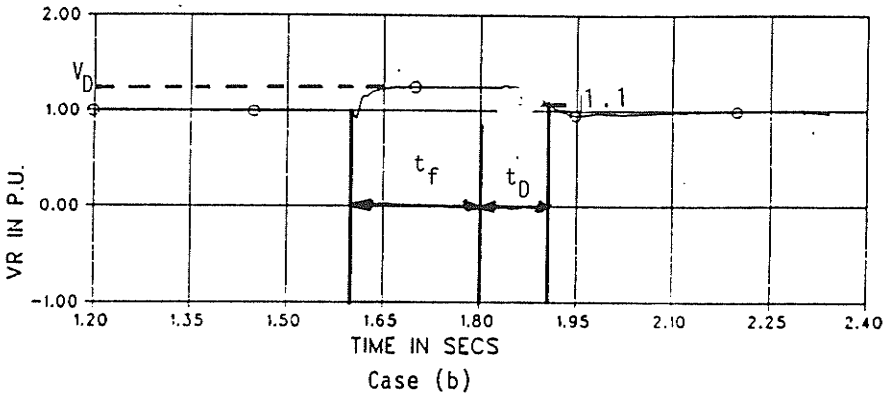


Case (c)

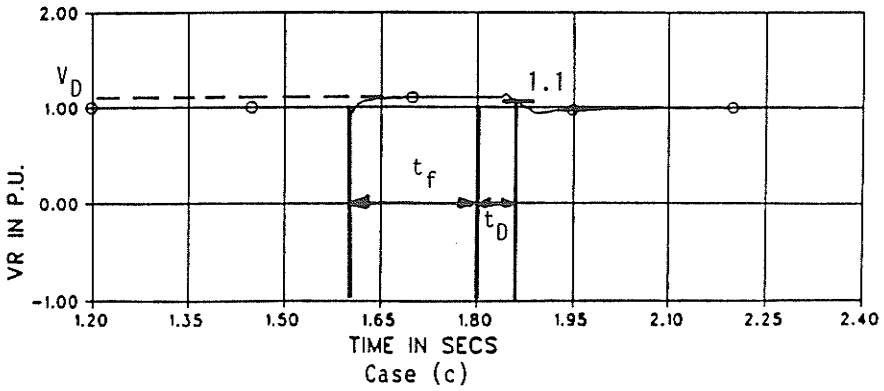
Figure C.4 Instantaneous AC Voltage Response for the DC Line Fault at the Inverter Terminal



Case (a)

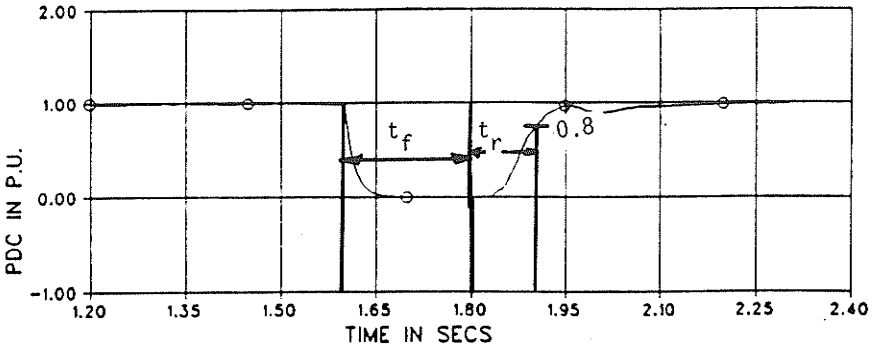


Case (b)

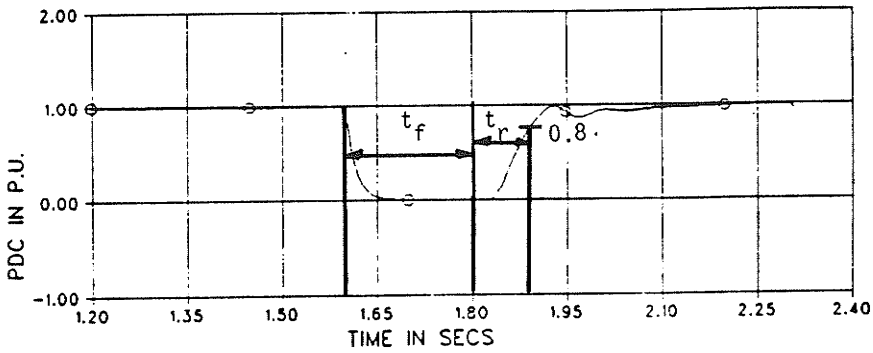


Case (c)

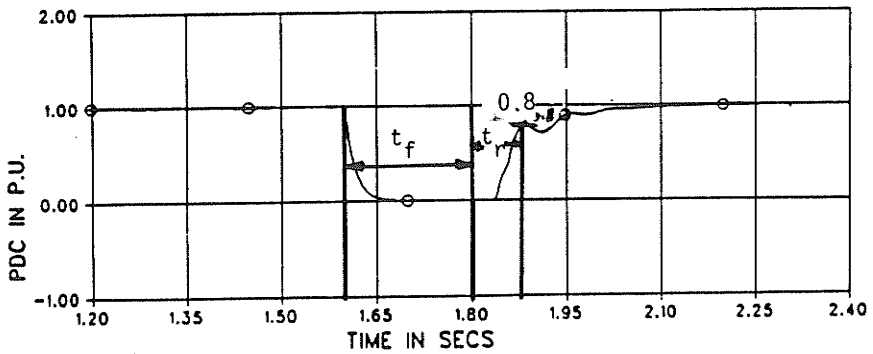
Figure C.5 Three Phase RMS Voltage Response for the DC Line Fault at the Inverter Terminal



Case (a)



Case (b)



Case (c)

Figure C.6 DC Power Recovery from the DC Line Fault at the Inverter Terminal

APPENDIX D1

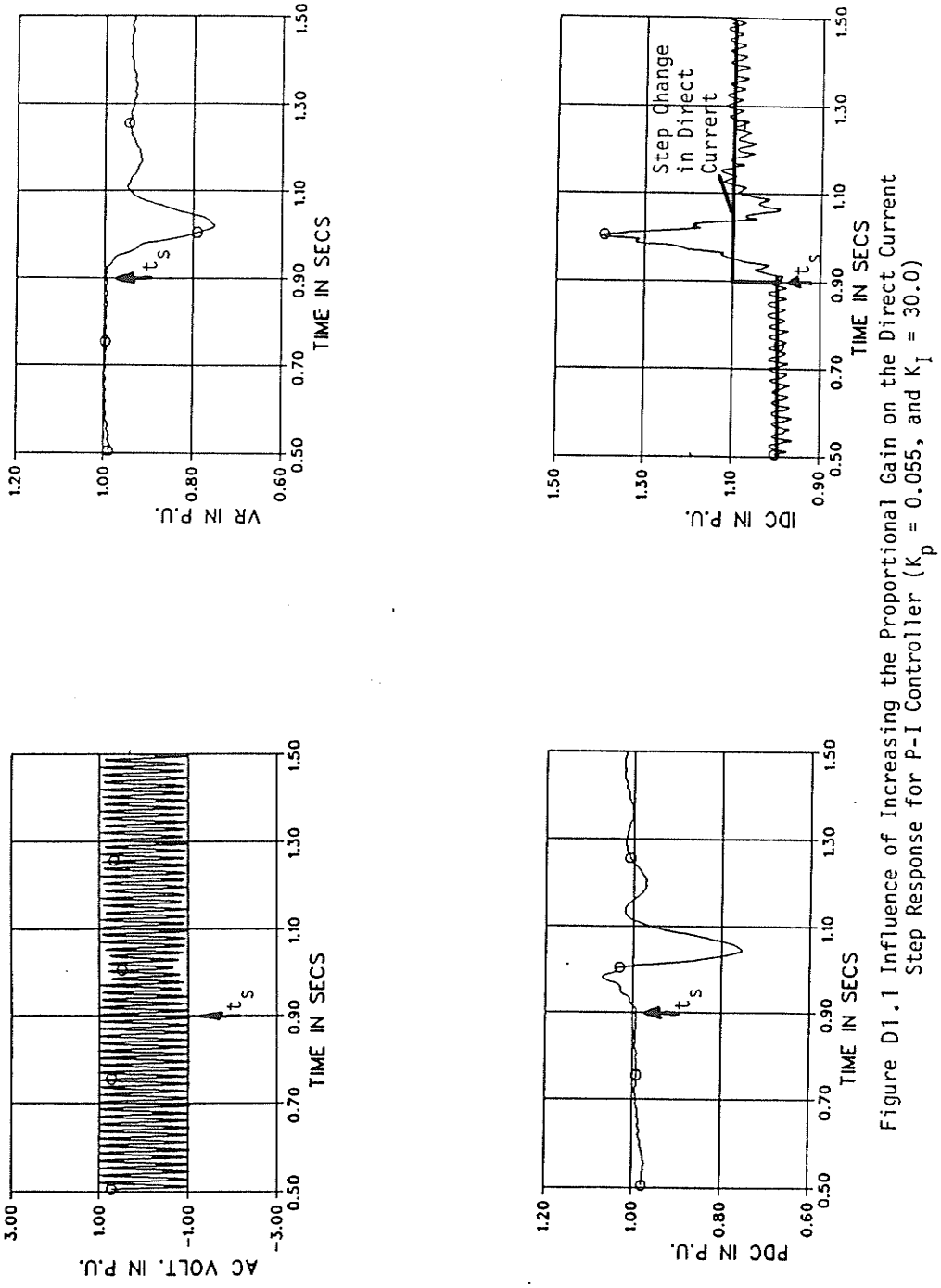
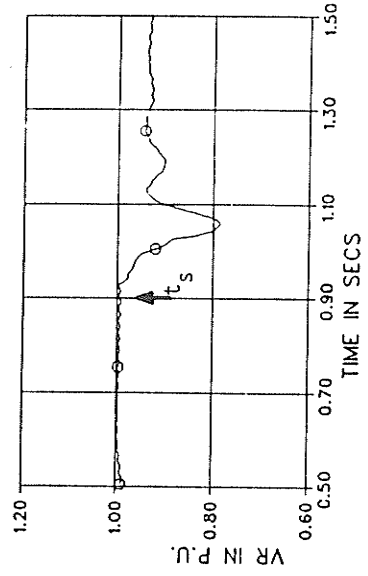
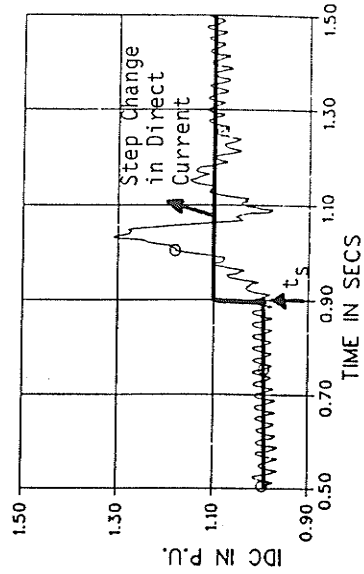
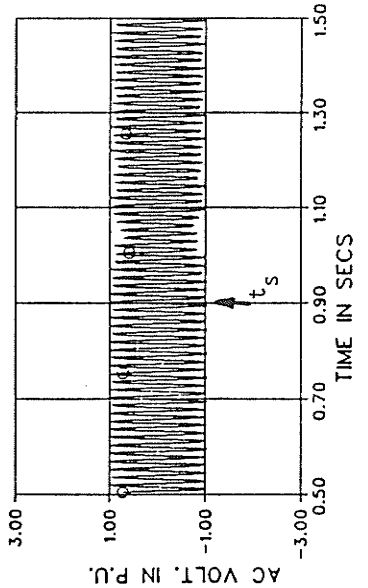


Figure D1.1 Influence of Increasing the Proportional Gain on the Direct Current Step Response for P-I Controller (K_p = 0.055, and K_I = 30.0)







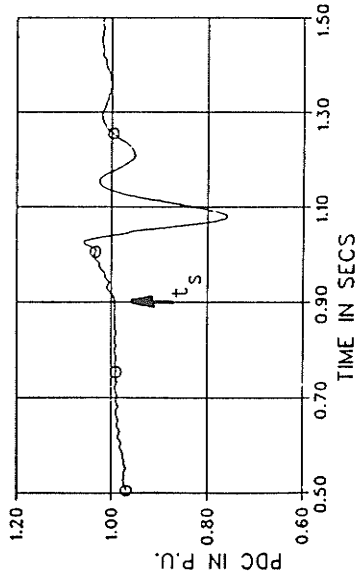


Figure D1.2 Influence of Increasing the Proportional Gain on the Direct Current Step Response for I-P Controller (K_p = 0.055, and K_I = 30.0)

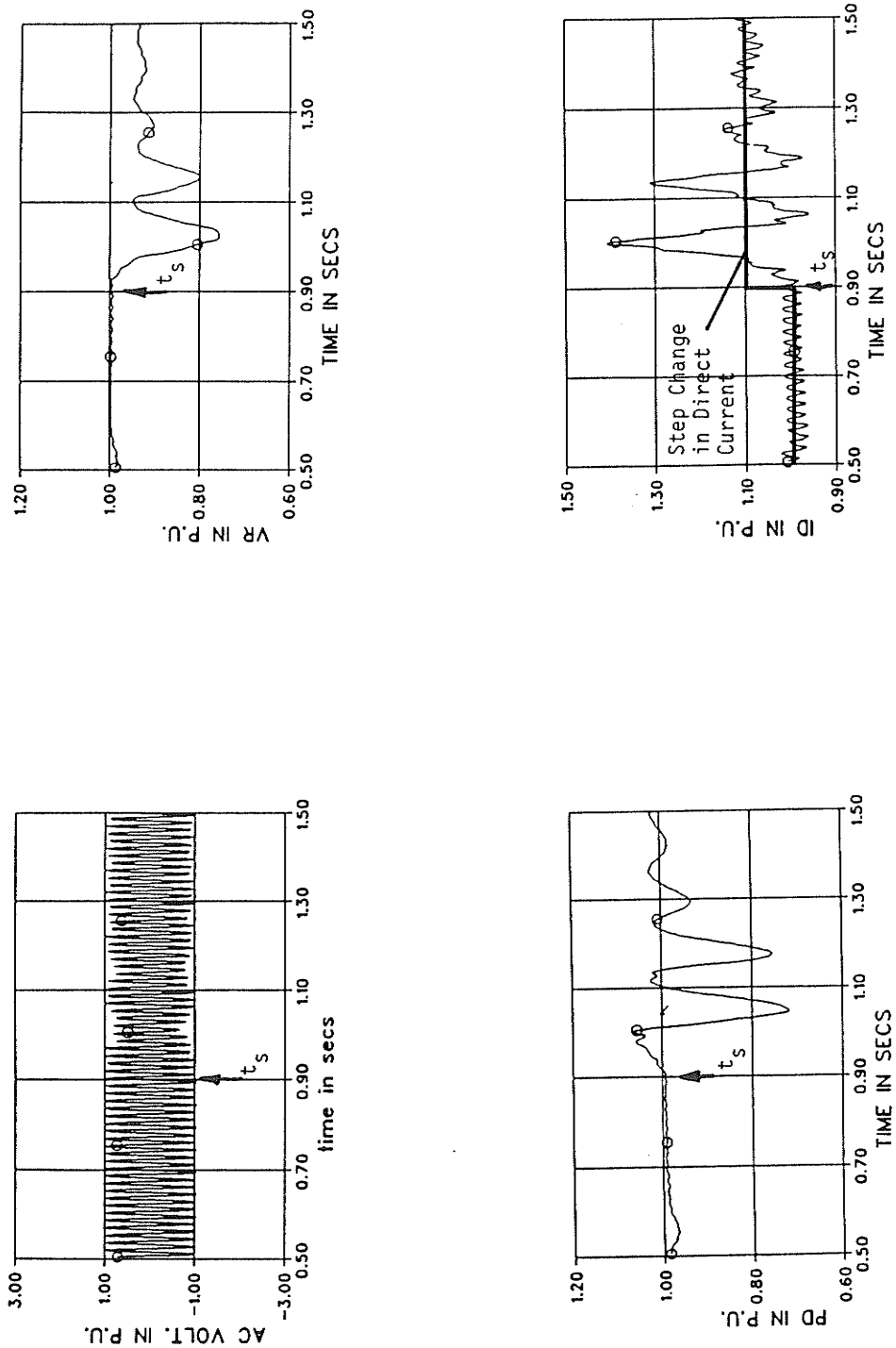


Figure D1.3 Influence of Increasing Integral Gain on the Direct Current Step Response for P-I Controller (K_p = 0.055, and K_I = 40.0)

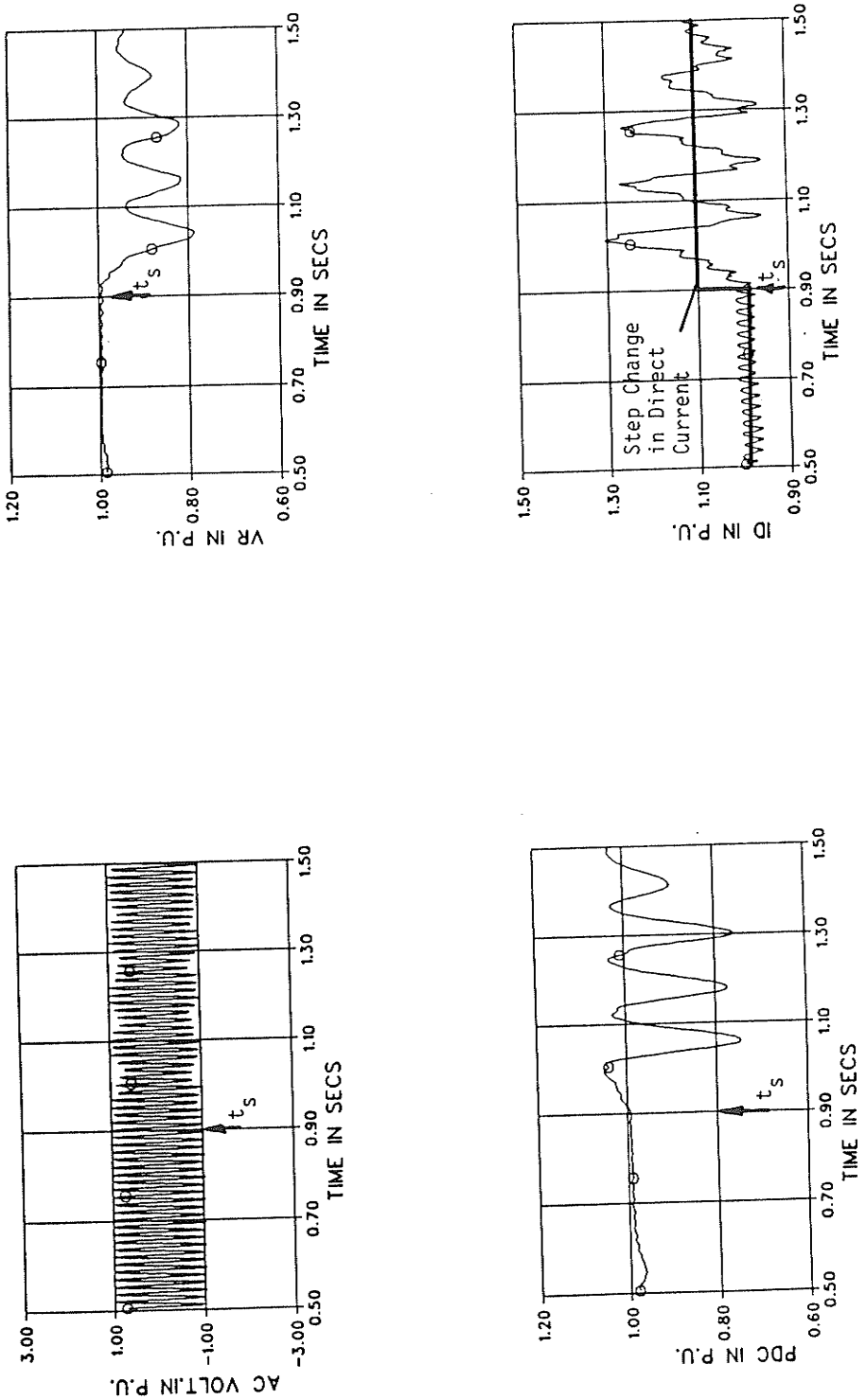


Figure D1.4 Influence of Increasing Integral Gain on the Direct Current Step Response for I-p Controller (K_p = 0.055, and K_I = 40.0)

APPENDIX D2

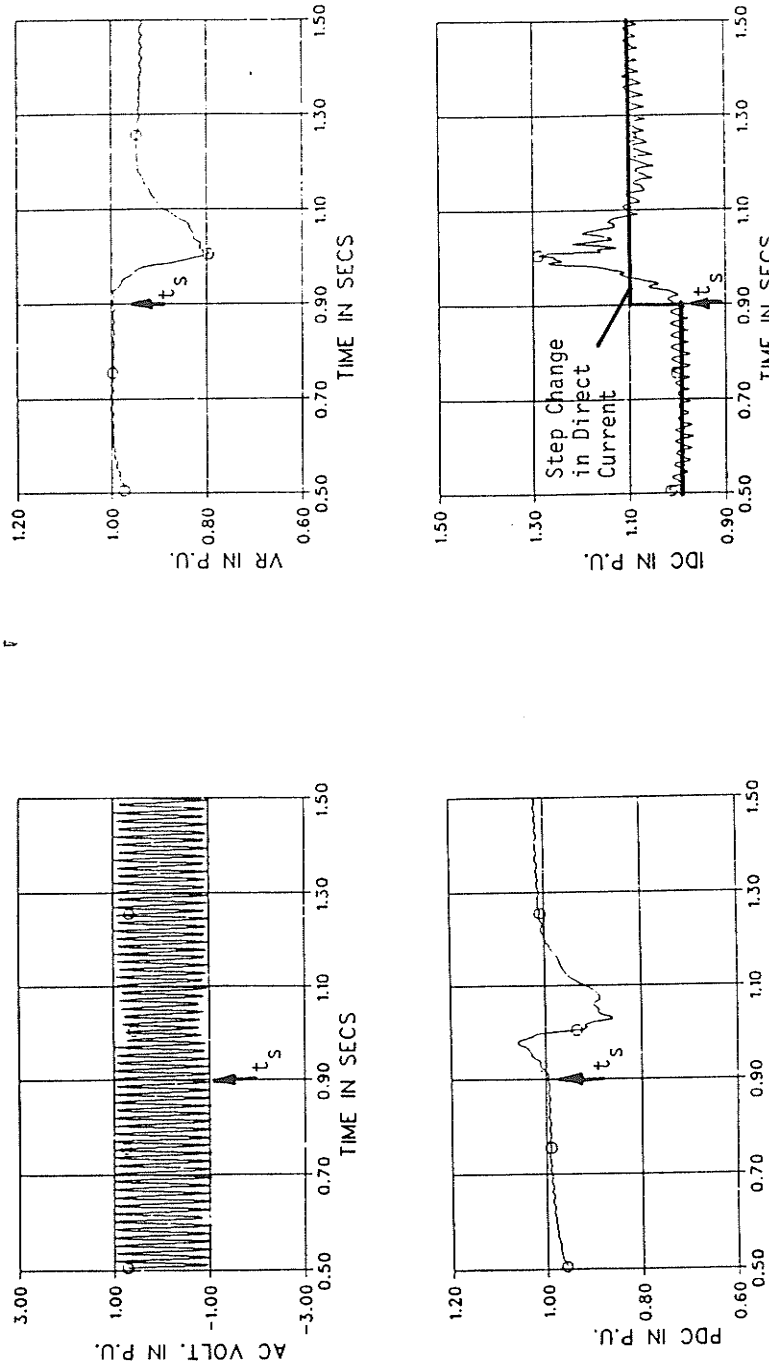


Figure D2.1 Influence of Increasing Proportional Gain on the Direct Current Step Response for P-I Controller (K_p = 0.07, and K_I = 30.0)

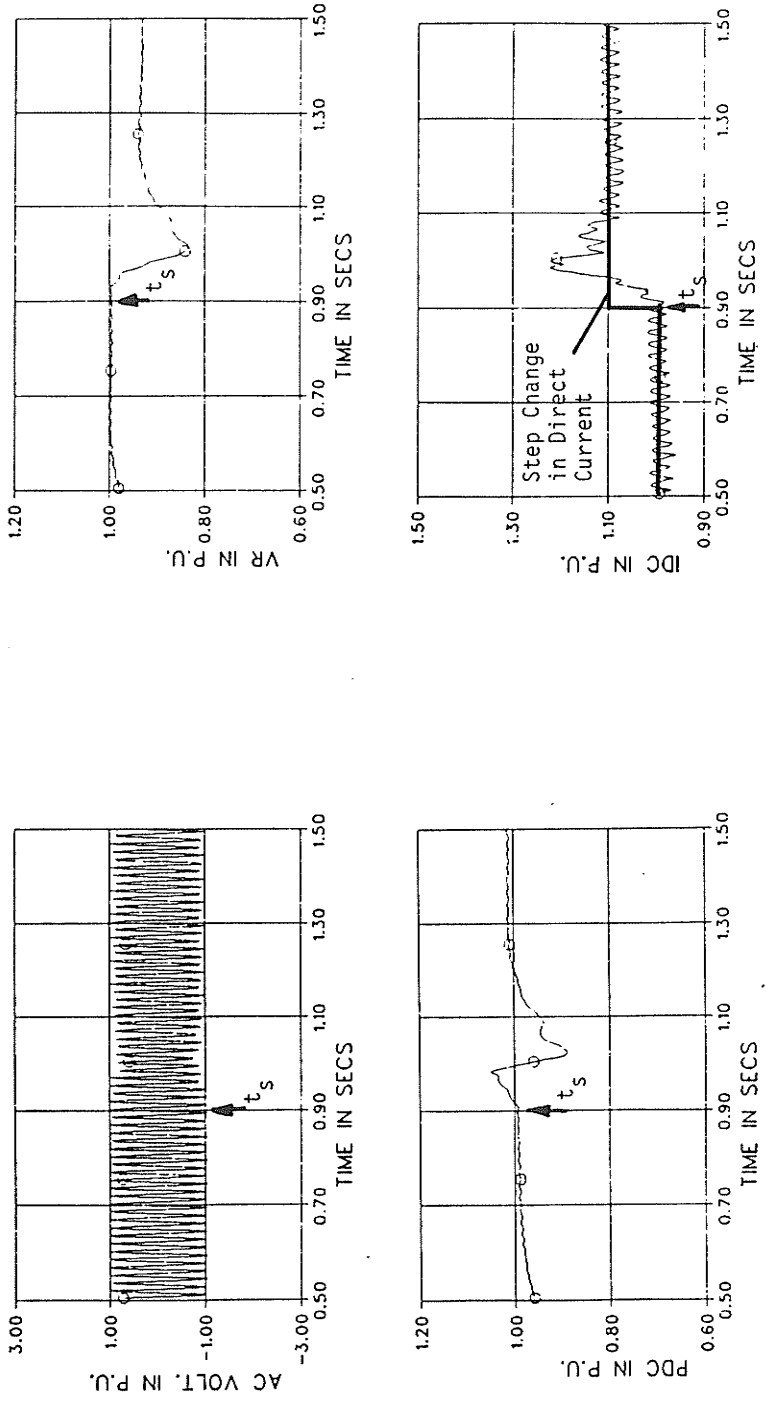


Figure D2.2 Influence of Increasing Proportional Gain on the Direct Current Step Response for Modified I-P Controller (K_p = 0.07, and K_I = 30.0)

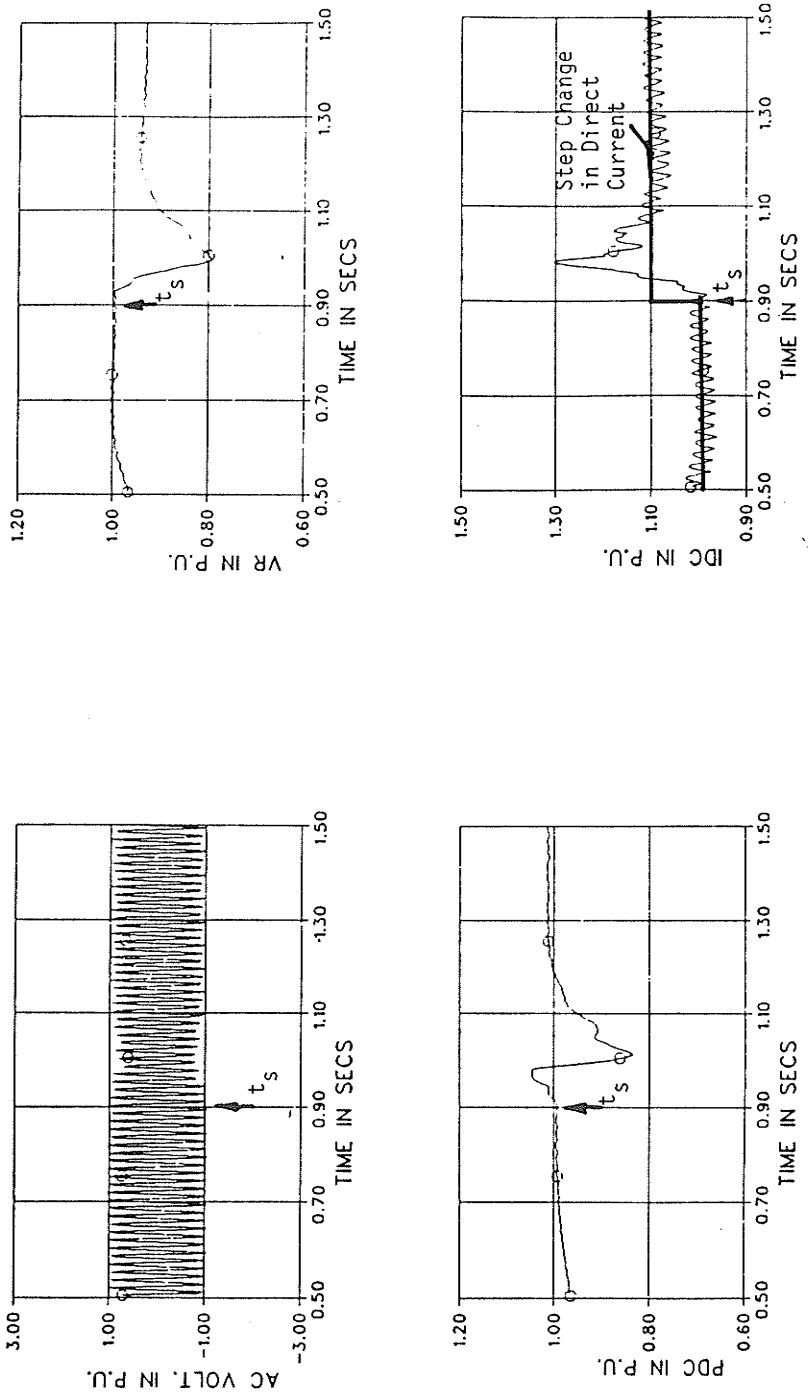


Figure D2.3 Influence of Reducing Integral Gain on the Direct Current Step Response for P-I Controller (K_p = 0.07, and K_I = 25.0)

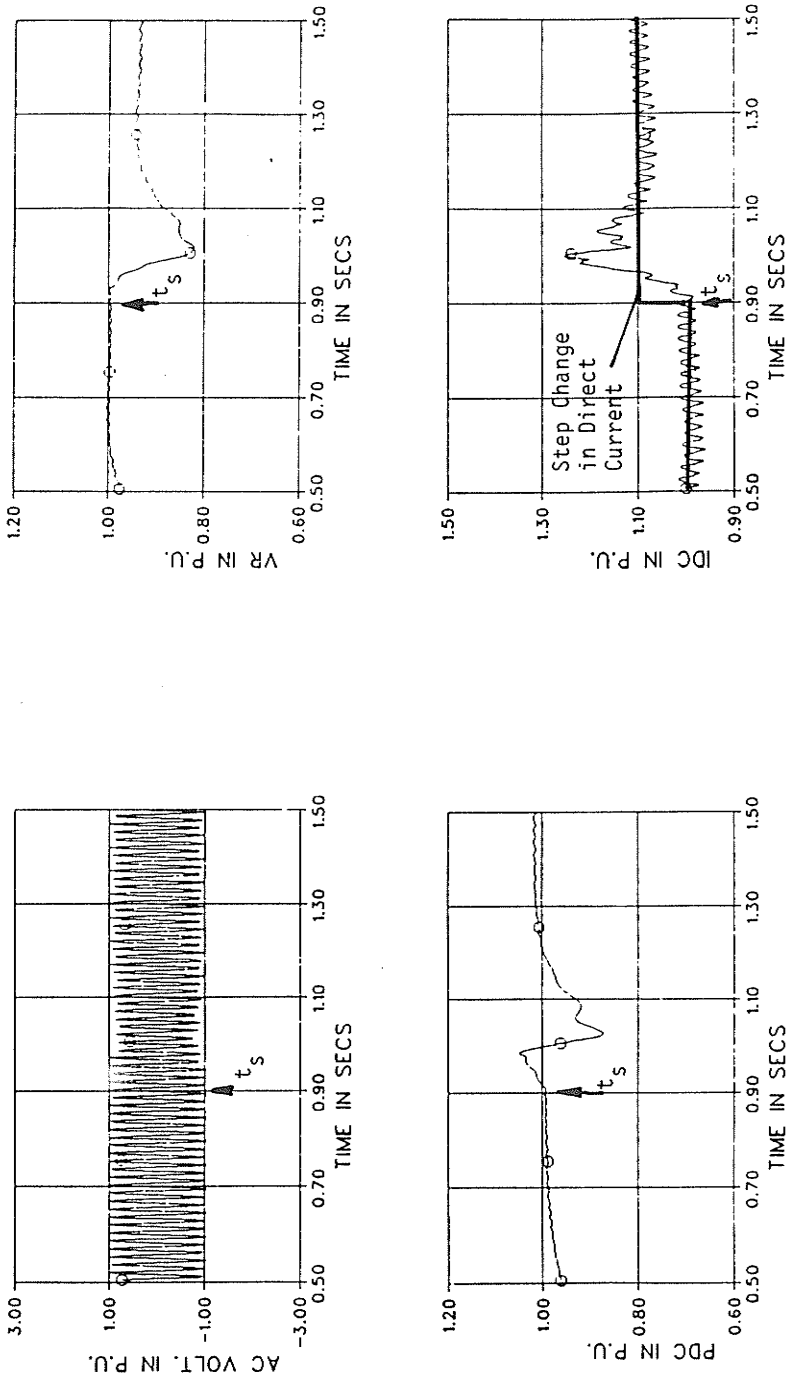


Figure D2.4 Influence of Reducing Integral Gain on the Direct Current Step Response for Modified I-P Controller (K_p = 0.07, and K_I = 25.0)

APPENDIX D3

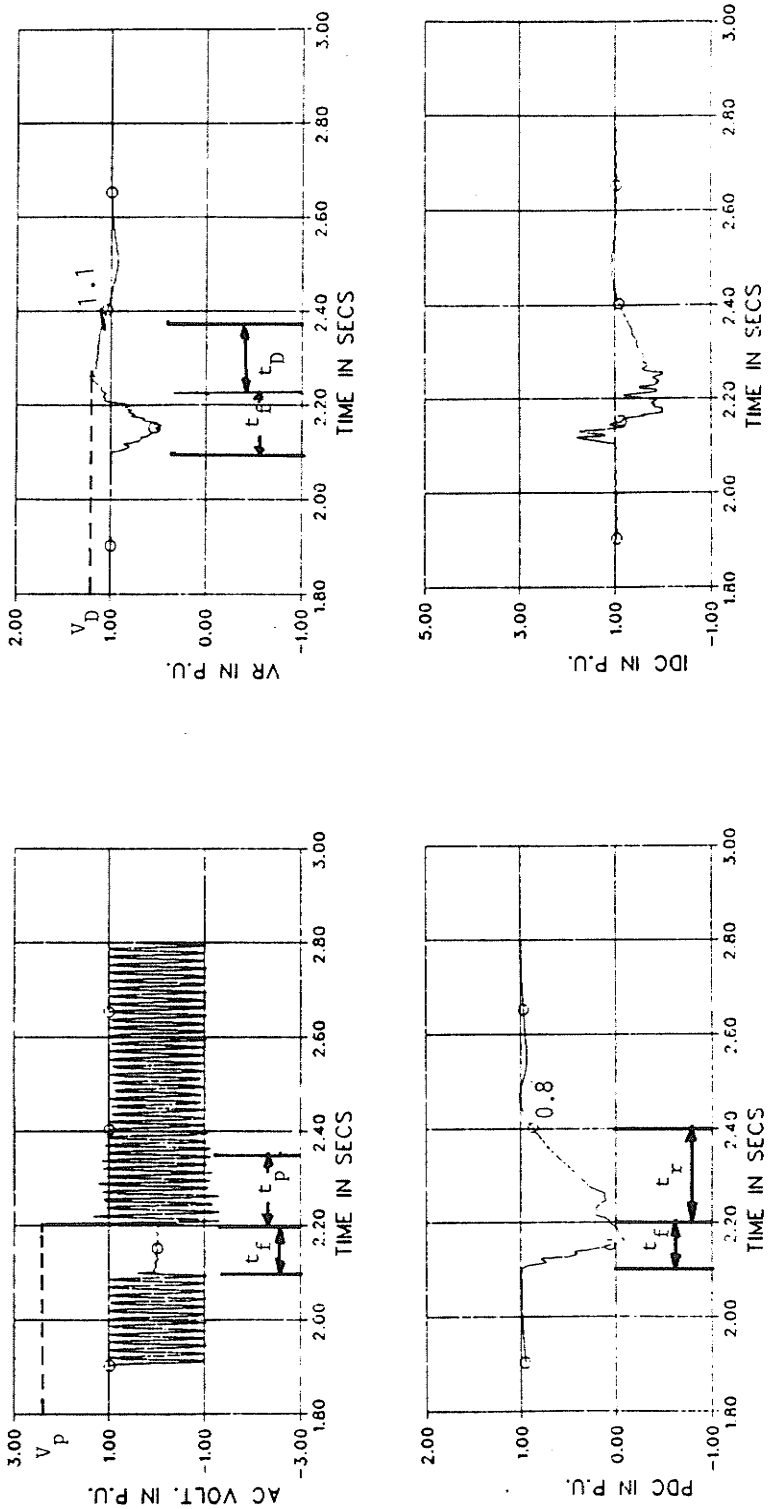


Figure D3.1 AC-DC-AC System Recovery from the Single Phase to Ground Fault at the Inverter AC Bus for P-I Controller

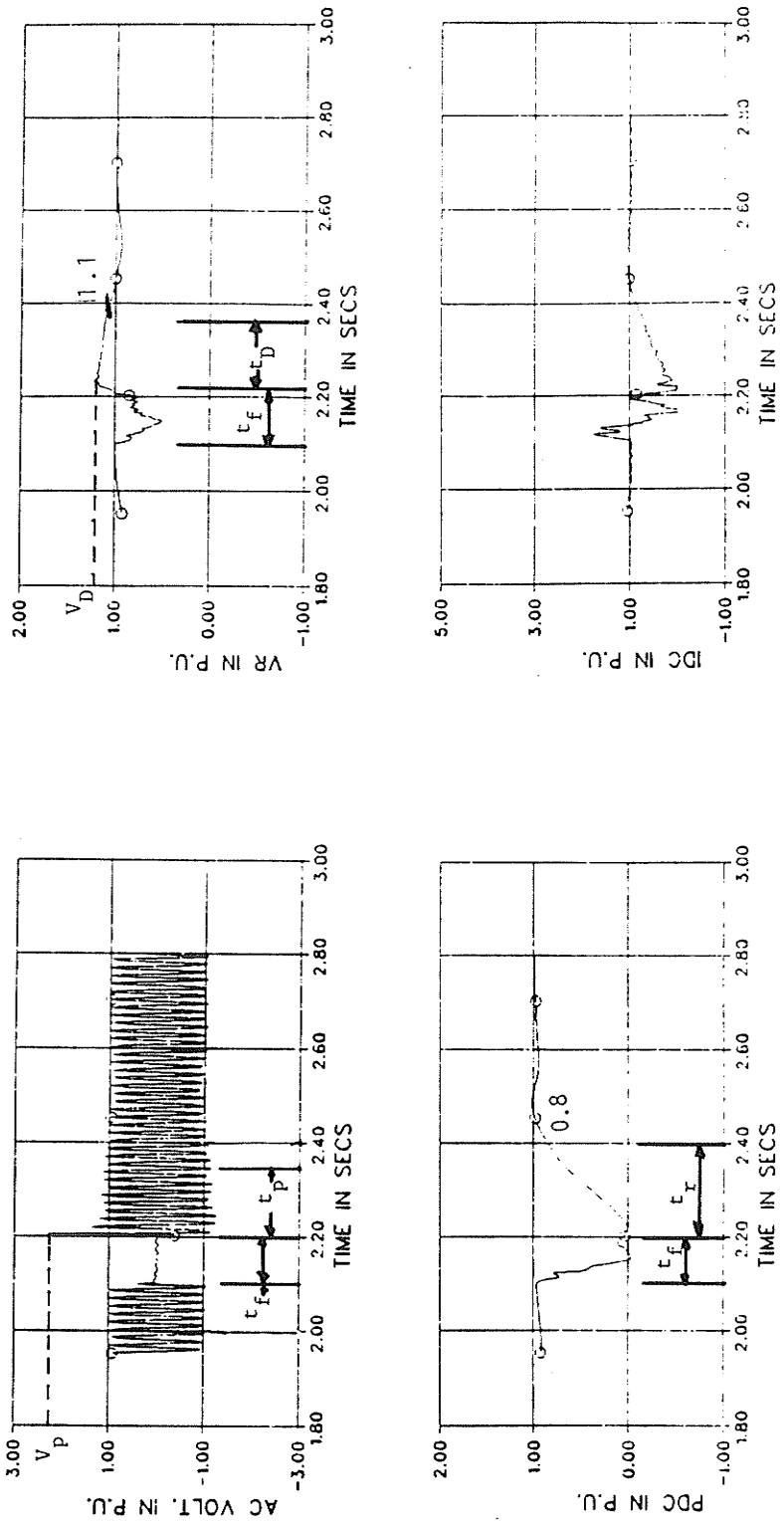


Figure D3.2 AC-DC-AC System Recovery from the Single Phase to Ground Fault at the Inverter AC Bus for Modified I-P Controller

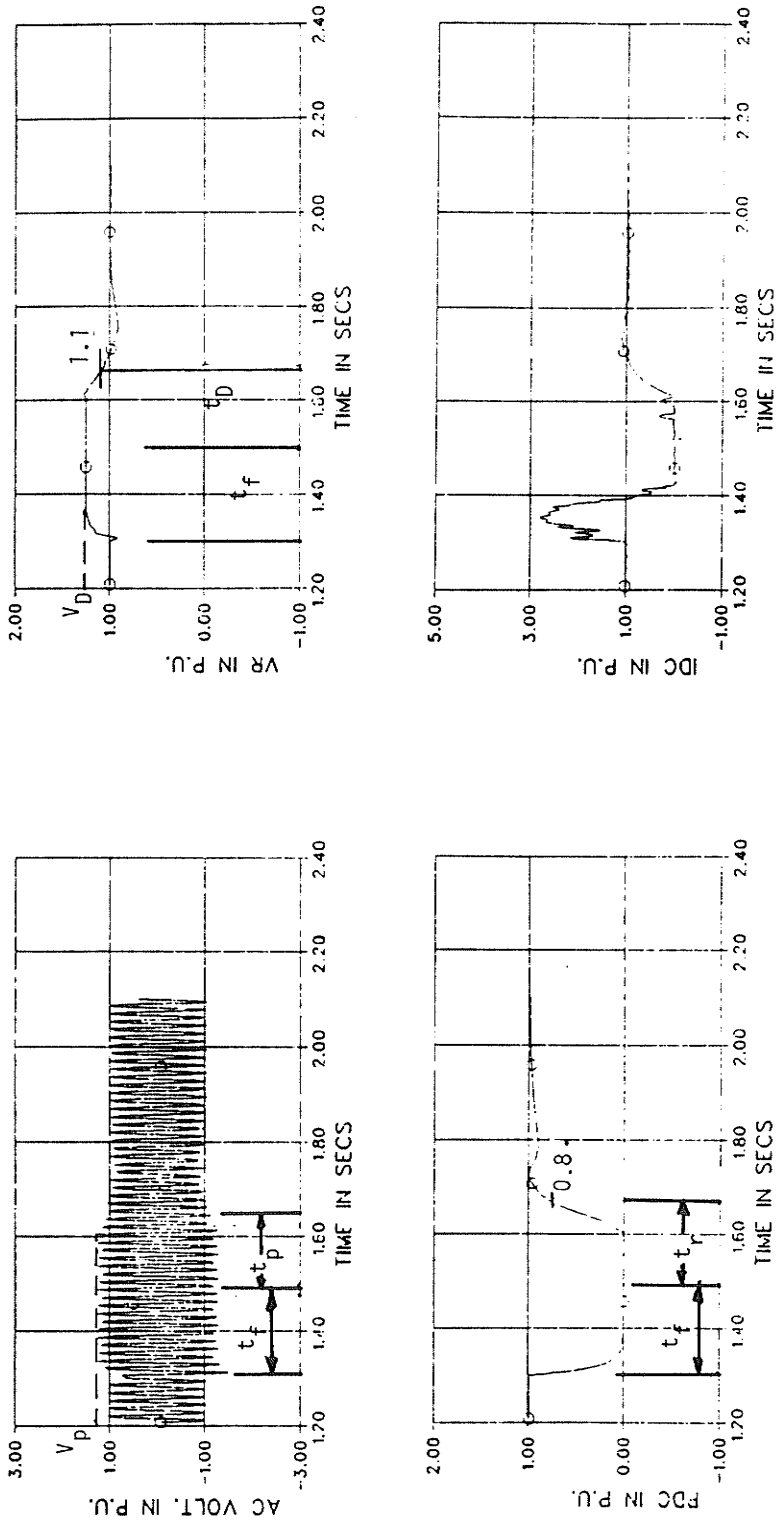


Figure D3.3 AC-DC-AC System Recovery from the DC Line Fault at the Inverter Terminal with P-I Controller

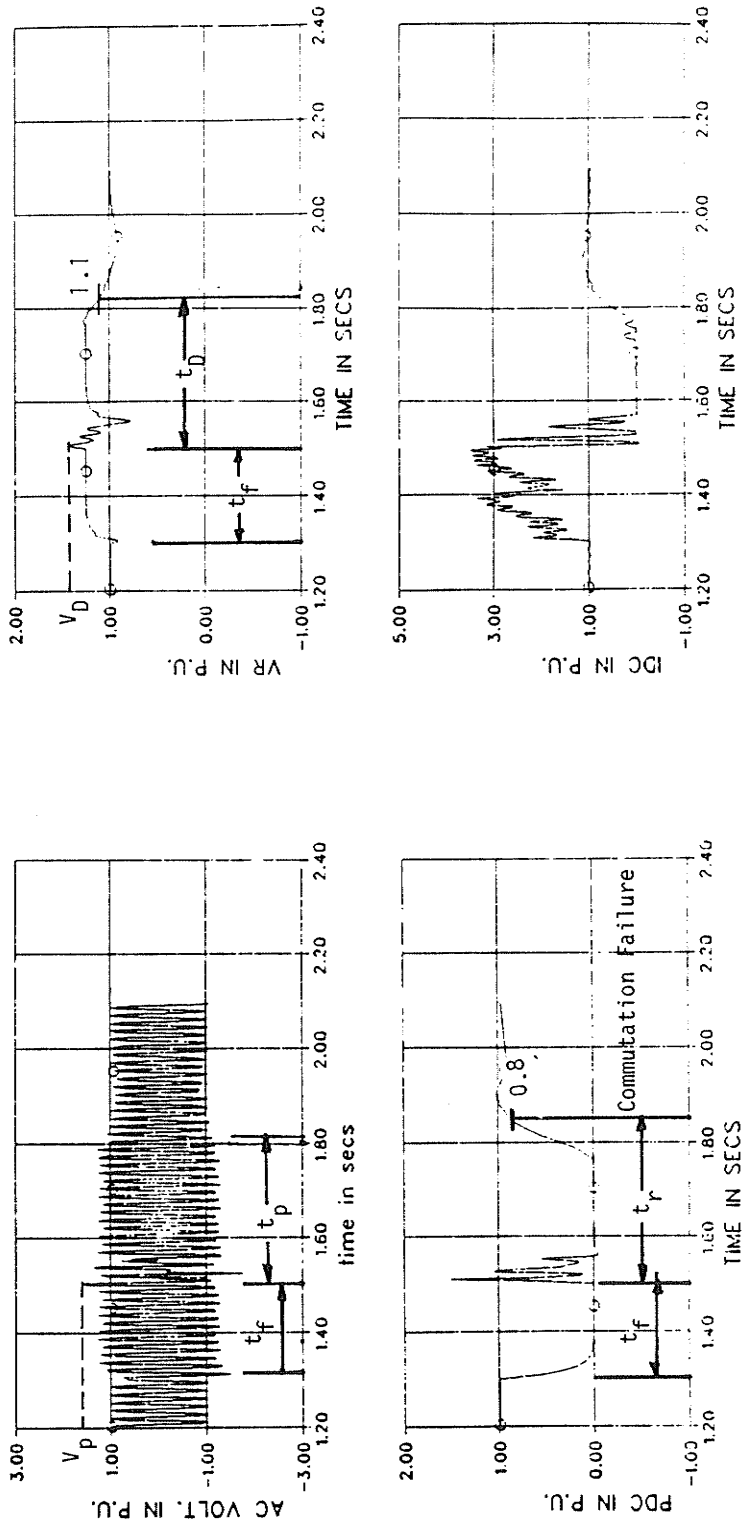


Figure D3.4 AC-DC-AC System Recovery from the DC Line Fault at the Inverter Terminal with Modified I-P Controller

APPENDIX E

Table E.1 Discriminants Values for Various Faults.

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
1	Steady State	0.02059	-0.63523	-0.85885	8
2	DC Line Fault at the Inverter	0.24602	1.07803	-0.09430	
3	Single Phase to Ground Fault at Inverter	0.16668	-0.60095	-0.96216	
4	Three Phase Fault at the Inverter Bus	0.47623	-1.17381	0.40806	
5	Single Phase to Ground Fault at the Rectifier Bus	0.16237	0.89047	-0.54031	
6	Three Phase to Ground Fault at the Rectifier Bus	0.36291	0.91433	-0.49629	
1	Steady State	0.01970	-0.65604	-0.82257	16
2	DC Line Fault at the Inverter	0.25599	1.06310	-0.13241	
3	Single Phase to Ground Fault at Inverter	0.16631	-0.64965	-0.82023	
4	Three Phase Fault at the Inverter Bus	0.44255	-1.13468	0.40285	
5	Single Phase to Ground Fault at the Rectifier Bus	0.16691	0.86735	-0.56667	
6	Three Phase to Ground Fault at the Rectifier Bus	0.37356	0.89082	-0.52522	
1	Steady State	0.01926	-0.66509	-0.80873	32
2	DC Line Fault at the Inverter	0.26079	1.05167	-0.16287	
3	Single Phase to Ground Fault at Inverter	0.16670	-0.68316	-0.72365	
4	Three Phase Fault at the Inverter Bus	0.42660	-1.10304	0.35611	
5	Single Phase to Ground Fault at the Rectifier Bus	0.16906	0.85404	-0.58590	
6	Three Phase to Ground Fault at the Rectifier Bus	0.37862	0.87720	-0.54603	
1	Steady State	0.01904	-0.66926	-0.80294	64
2	DC Line Fault at the Inverter	0.26314	1.04508	-0.18054	
3	Single Phase to Ground Fault at Inverter	0.16703	-0.70157	-0.67145	

Table E.1 (Continued)

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
4	Three Phase Fault at the Inverter Bus	0.41887	-1.08409	0.32083	64
5	Single Phase to Ground Fault at the Rectifier Bus	0.17011	0.84698	-0.59688	
6	Three Phase to Ground Fault at the Rectifier Bus	0.38108	0.86997	-0.55785	
1	Steady State	0.01893	-0.67126	-0.80034	128
2	DC Line Fault at the Inverter	0.26431	1.04157	-0.18995	
3	Single Phase to Ground Fault at Inverter	0.16723	-0.71111	-0.64472	
4	Three Phase Fault at the Inverter Bus	0.41509	-1.07386	0.30025	
5	Single Phase to Ground Fault at the Rectifier Bus	0.17062	0.84335	-0.60267	
6	Three Phase to Ground Fault at the Rectifier Bus	0.38229	0.86625	-0.56409	
1	Steady State	0.01887	-0.67224	-0.79913	256
2	DC Line Fault at the Inverter	0.26489	1.03977	-0.19478	
3	Single Phase to Ground Fault at Inverter	0.16734	-0.71594	-0.63125	
4	Three Phase Fault at the Inverter Bus	0.41318	-1.06855	0.28919	
5	Single Phase to Ground Fault at the Rectifier Bus	0.17088	0.84152	-0.60565	
6	Three Phase to Ground Fault at the Rectifier Bus	0.38289	0.86437	-0.56728	
1	Steady State	0.01885	-0.67272	-0.78954	512
2	DC Line Fault at the Inverter	0.26518	1.03886	-0.19724	
3	Single Phase to Ground Fault at Inverter	0.16740	-0.71838	-0.62448	
4	Three Phase Fault at the Inverter Bus	0.41224	-1.06584	0.28347	
5	Single Phase to Ground Fault at the Rectifier Bus	0.17101	0.84060	-0.60715	
6	Three Phase to Ground Fault at the Rectifier Bus	0.38319	0.86342	-0.56890	

Table E.2 Discriminants Values for Various Faults for Different Sampling Rates with Log-Transformation.

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
1	Steady State	0.02224	-0.65920	-0.82041	8
2	DC Line Fault at the Inverter	1.67518	-0.60154	-0.02200	
3	Single Phase to Ground Fault at Inverter	0.14216	-0.74419	-0.73821	
4	Three Phase Fault at the Inverter Bus	0.70071	-2.38890	5.08907	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20271	0.70728	-0.90367	
6	Three Phase to Ground Fault at the Rectifier Bus	2.10167	-1.02839	0.52254	
1	Steady State	0.02126	-0.67964	-0.78286	16
2	DC Line Fault at the Inverter	1.51929	-0.36785	-0.02372	
3	Single Phase to Ground Fault at Inverter	0.14275	-0.81853	-0.49150	
4	Three Phase Fault at the Inverter Bus	0.58892	-2.46791	6.24159	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20643	0.67489	-0.94181	
6	Three Phase to Ground Fault at the Rectifier Bus	2.01688	-0.88984	0.05386	
1	Steady State	0.02077	-0.68840	-0.76882	32
2	DC Line Fault at the Inverter	1.47865	-0.23804	-0.02663	
3	Single Phase to Ground Fault at Inverter	0.14375	-0.86925	-0.32284	
4	Three Phase Fault at the Inverter Bus	0.53444	-2.39734	6.13425	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20814	0.65769	-0.96300	
6	Three Phase to Ground Fault at the Rectifier Bus	2.00289	-0.86784	-0.06338	
1	Steady State	0.02053	-0.69240	-0.76304	64
2	DC Line Fault at the Inverter	1.52101	-0.43476	0.02533	
3	Single Phase to Ground Fault at Inverter	0.14441	-0.89675	-0.23274	

Table E.2 (Continued)

Case No.	Type of Fault	Standard Deviation	Skewness	Kurtosis	No. Samples/ Cycles
4	Three Phase Fault at the Inverter Bus	0.50846	-2.32771	5.80805	64
5	Single Phase to Ground Fault at the Rectifier Bus	0.20897	0.64886	-0.97401	
6	Three Phase to Ground Fault at the Rectifier Bus	2.00063	-0.86988	-0.07058	
1	Steady State	0.02041	-0.69431	-0.76047	128
2	DC Line Fault at the Inverter	1.52496	-0.45217	0.02122	
3	Single Phase to Ground Fault at Inverter	0.14478	-0.91085	-0.18709	
4	Three Phase Fault at the Inverter Bus	0.49596	-2.28600	5.58627	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20937	0.64439	-0.97961	
6	Three Phase to Ground Fault at the Rectifier Bus	1.99903	-0.87047	-0.07489	
1	Steady State	0.02035	-0.69523	-0.75929	256
2	DC Line Fault at the Inverter	1.51677	-0.40571	-0.02111	
3	Single Phase to Ground Fault at Inverter	0.14497	-0.91796	-0.16422	
4	Three Phase Fault at the Inverter Bus	0.48984	-2.26382	5.46453	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20957	0.64215	-0.98242	
6	Three Phase to Ground Fault at the Rectifier Bus	1.99829	-0.87098	-0.07632	
1	Steady State	0.02032	-0.69569	-0.75871	512
2	DC Line Fault at the Inverter	1.52055	-0.42971	0.02111	
3	Single Phase to Ground Fault at Inverter	0.14507	-0.92154	-0.15277	
4	Three Phase Fault at the Inverter Bus	0.48682	-2.25246	5.40155	
5	Single Phase to Ground Fault at the Rectifier Bus	0.20966	0.64102	-0.98383	
6	Three Phase to Ground Fault at the Rectifier Bus	1.99777	-0.87091	-0.07818	

Table E.3 Discriminants Values for Various Faults (Frequency Domain Analysis).

Case No.	Type of Fault	Harmonic Factor	Frequency Factor	Log Transformation Harmonic Factor	Log Transformation Frequency Factor	No. Samples/ Cycles
1	Steady State	1.37	133.2	1.38	133.6	4
2	DC Line Fault at the Inverter	1.12	123.5	1.46	136.9	
3	Single Phase to Ground Fault at Inverter	1.00	119.3	1.02	119.7	
4	Three Phase Fault at the Inverter Bus	1.13	123.9	2.10	159.4	
5	Single Phase to Ground Fault at the Rectifier Bus	1.23	127.8	1.15	124.9	
6	Three Phase to Ground Fault at the Rectifier Bus	1.21	127.3	1.03	120.2	
1	Steady State	1.32	131.3	1.33	130.2	8
2	DC Line Fault at the Inverter	1.13	124.1	1.54	132.2	
3	Single Phase to Ground Fault at Inverter	1.00	119.3	1.02	119.8	
4	Three Phase Fault at the Inverter Bus	1.05	121.7	1.96	146.1	
5	Single Phase to Ground Fault at the Rectifier Bus	1.20	127.2	1.15	124.3	
6	Three Phase to Ground Fault at the Rectifier Bus	1.20	126.9	1.32	123.7	
1	Steady State	1.29	129.2	1.30	130.2	16
2	DC Line Fault at the Inverter	1.13	124.0	1.33	132.2	
3	Single Phase to Ground Fault at Inverter	1.00	119.3	1.02	119.8	
4	Three Phase Fault at the Inverter Bus	1.05	120.8	1.69	146.1	
5	Single Phase to Ground Fault at the Rectifier Bus	1.20	126.6	1.14	124.3	
6	Three Phase to Ground Fault at the Rectifier Bus	1.19	126.4	1.13	123.7	

Table E.3 (Continued)

Case No.	Type of Fault	Harmonic Factor	Frequency Factor	Log Transformation Harmonic Factor	Log Transformation Frequency Factor	No. Samples/ Cycles
1	Steady State	1.27	129.3	1.28	129.5	32
2	DC Line Fault at the Inverter	1.13	124.0	1.26	129.4	
3	Single Phase to Ground Fault at Inverter	1.00	119.4	1.02	119.8	
4	Three Phase Fault at the Inverter Bus	1.04	120.4	1.52	138.7	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.2	1.14	124.1	
6	Three Phase to Ground Fault at the Rectifier Bus	1.19	126.0	1.13	123.9	
1	Steady State	1.26	128.9	1.27	129.2	64
2	DC Line Fault at the Inverter	1.13	124.0	1.31	131.2	
3	Single Phase to Ground Fault at Inverter	1.01	119.4	1.02	119.9	
4	Three Phase Fault at the Inverter Bus	1.04	120.4	1.40	135.2	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.2	1.13	124.1	
6	Three Phase to Ground Fault at the Rectifier Bus	1.18	126.0	1.14	124.2	
1	Steady State	1.26	128.8	1.27	129.0	128
2	DC Line Fault at the Inverter	1.13	124.0	1.32	131.6	
3	Single Phase to Ground Fault at Inverter	1.01	119.4	1.02	120.0	
4	Three Phase Fault at the Inverter Bus	1.04	120.3	1.38	133.7	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.1	1.13	124.0	
6	Three Phase to Ground Fault at the Rectifier Bus	1.18	125.9	1.14	124.3	

Table E.3 (Continued)

Case No.	Type of Fault	Harmonic Factor	Frequency Factor	Log Transformation Harmonic Factor	Log Transformation Frequency Factor	No. Samples/ Cycles
1	Steady State	1.26	128.7	1.26	128.9	256
2	DC Line Fault at the Inverter	1.13	124.0	1.30	131.1	
3	Single Phase to Ground Fault at Inverter	1.01	119.4	1.02	120.0	
4	Three Phase Fault at the Inverter Bus	1.03	120.3	1.37	132.9	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.1	1.13	124.0	
6	Three Phase to Ground Fault at the Rectifier Bus	1.18	125.9	1.14	124.4	
1	Steady State	1.26	128.7	1.26	128.9	512
2	DC Line Fault at the Inverter	1.13	124.0	1.31	131.3	
3	Single Phase to Ground Fault at Inverter	1.01	119.4	1.02	119.9	
4	Three Phase Fault at the Inverter Bus	1.03	120.3	1.36	132.6	
5	Single Phase to Ground Fault at the Rectifier Bus	1.19	126.1	1.13	124.0	
6	Three Phase to Ground Fault at the Rectifier Bus	1.18	125.9	1.15	124.4	

BIBLIOGRAPHY

1. Kimbark, E.W., "Direct Current Transmission," New York, Wiley Interscience, 1971.

2. Ulhmann, E., "Power Transmission by Direct Current," New York, Springer-Verlag, 1975.

3. Adamson, C. and Hingorani, N.G., "High Voltage Direct Current Power Transmission," Garroway, London, 1960.

4. IEEE Committee Report, "Functional Model of Two Terminal HVDC Systems for Transients and Steady-State Stability," IEEE PAS-103, No. 6, June 1984.

5. Bowles, J.P., et al., "Controls in HVDC Systems, The State-of-the-Art, Part 1, Two Terminal Systems," CIGRE Paper No. 14-10, 1978.

6. Canadian Electrical Association, "High Voltage Direct Current Control Guide," produced by CEA HVDC Control Committee, March 1983.

7. Tarnawecky, M.Z., "HVDC Transmission Control Schemes," Proceeding of Manitoba Power Conference on EHVDC, 1971, pp. 598-714.

8. Hammad, A., et al., "Advanced Scheme for Voltage Control at HVDC Terminals," 1985, PICA, San Francisco, California, May 6-10, 1985, pp. 431-438.

9. Szechtman, M., et al., "Unconventional HVDC Controls Techniques for Stabilization of a Weak Power System," IEEE PAS-103, Aug. 1984, pp. 2244-2248.

10. Bowles, J.P., "Alternative Technique and Optimization of Voltage and Reactive Power Control at HVDC Station," Proceeding of IEEE Conference on Overvoltages and Compensation on Integrated AC/DC System, Winnipeg, Canada, July 1980, pp. 5-5i.

11. Nishimura, J., et al., "Constant Power Factor Control Systems for HVDC Transmission," IEEE Vol. PAS-95, No. 6, 1976.

12. Rumf, E. and Rande, "Comparison of Suitable Converter Control Systems for HVDC Stations Connected to Weak AC Systems, Part 1: New Control Systems, Part 2: Operational Behavior of HVDC Transmission," IEEE Trans. PAS-91, 1972, pp. 549-564.

13. Yuki, M., et al., "Development of Digitilised Control Equipment for HVDC Transmission," IEEE Trans., Vol. PAS 103, Jan. 1984, pp. 190-196.

14. Mathur, R.M., et al., "AC Voltage Control at HVDC Converter Terminal," paper presented at Canadian Communication & Power Conference, Montreal, 1978, pp. 236-241.

15. Kalra, P.K. and Mathur, R.M., "Power Factor Control for HVDC Transmission System Feeding to Weak AC System," paper presented at IEEE Conference (MONTECH), Montreal, Sept. 29-Oct. 1, 1986.

16. Yoshida, Y., "Development of a Calculation Method of AC Voltage Stability in HVDC Transmission Systems," Elect. Engg. in Japan, Vol. 94, No. 2, 1978, pp. 77-85.

17. Grund, C.C., Pohl, R.V., Reeve, J., "Control Design of Active and Reactive Power HVDC Modulation Systems with Kalman Filtering," IEEE Trans., Vol. PAS-101, No. 10, Oct. 1982, pp. 4100-4111.

18. Hingorani, N.G., et al., "Active and Reactive Power Modulation of HVDC System," Proceeding IEEE Conference on Overvoltages and Compensation in Integrated AC-DC Systems, Winnipeg, July 1980, pp. 51-57.

19. Koske, S. and Masada, E., "Analytical Design of HVDC Link Control System," Elect. Engg. in Japan, Vol. 96, No. 2, 1976, pp. 80-86.

20. Carroll, D.P., et al., "The Use of Voltage Feedback in HVDC Converter Control," IEEE Trans., Vol. PAS-95, No. 5, 1976, pp. 1579-1589.

21. Hayashi, T., et al., "Voltage Regulation Characteristics of AC-DC Interconnecting Point and its Suppression Method: Application of Automatic Reactive Power Control to Converter Station," Elect. Engg. in Japan, Vol. 93, No. 4, 1973, pp. 110-116.

22. Zhou, B., "Steady-State Stability Analysis of HVDC Systems with Digital Controller," IEEE Trans., Vol. PAS-102, No. 6, June 1983, pp. 1764-1770.

23. Goudic, D.B., "Steady State Stability of Parallel HV AC-DC Power Transmission Systems," Proc. IEE, Vol. 110, No. 2, 1972, pp. 217-228.

24. Hingorani, N.G., Hay, J.L., and Bhatti, J.S., "Simplified Dynamic Simulation of HVDC Systems by Digital Computers," Part I: Computer Program, Part II: Design of Controller and Test Results; IEEE Trans., Vol. PAS-90, No. 2, 1971, pp. 859-870.

25. Kuo, B.C., "Automatic Control Systems," Prentice Hall of India, Pvt. Ltd.: New Delhi, India, 1976.

26. Sucene Paiva, J.P., Hernandez, R. and Freris, L.L., "Stability Study of Controller Rectifier Using New Discrete Converter Model," Proc. IEE, Vol. 199, 1972, pp. 1285-1295.

27. Sucene Paiva, J.P. and Freris, L.L., "Stability of Rectifiers with Voltage Controlled Firing System," Proc. IEE, Vol. 120, 1973, pp. 667-673.

28. Kovalsky, L.J. and Putokovich, R.P., "Microprocessor Based Controls for AC-DC Power Conversion Systems with DC Interrupters Protection," Report Submitted to U.S. Dept. of Electrical Energy Systems, Washington, 1982.

29. Bjarestem, N.A., "The Static Converter as High Speed Power Amplifiers," Direct Current, No. 8, June 1963, pp. 154-165.

30. Parrish, E.A. and McVey, E.S., "A Theoretical Model for Single Phase Silicon Controlled Rectifier System," IEEE Trans., Vol. AC-12, 1967, pp. 557-579.

31. Hazell, P.A. and Flower, J.O., "Stability Properties of Certain Thyristor-Bridge Control Systems," Part I: "Thyristor Bridge as a Discrete Control System," Proc. IEE, Vol. 117, No. 7, 1970, pp. 1405-1412.

32. Sood, V.K., et al., "Simulator Study of Hydro Quebec MTDC Line from James Bay to New England," Paper to be presented at IEEE-PAS Summer Meeting, July 1987.

33. Weedy, B.M., "Electric Power System," Third Edition, John Wiley & Sons: New York, 1979.

34. "A Manual on a HVDC Simulator," available at the University of Manitoba.

35. Mathur, R.M. (Editor), "Static Compensators for Reactive Power Control," CEA, Montreal, Canada.

36. "Motorola Linear Integrated Circuits," Fourth Printing, Motorola Inc., 1979.

37. Reeve, J. and Kapoor, S.C., "Dynamic Fault Analysis of HVDC Systems with AC Representation," IEEE Trans., Vol. PAS-91, No. 2, March/April 1972, pp. 508-515.

38. Reeve, J. and Carr, J., "Dynamic Simulation of HVDC Converter Control and its Application to System Studies," IEEE Trans., Vol. PAS-93, No. 1, 1974, pp. 295-302.

39. Hingorani, N.G., Kitchen, R.H. and Hay, J.L., "Dynamic Simulation of HVDC Power Transmission Systems on Digital Computers," IEEE Trans., Vol. PAS-87, No. 4, 1974 pp. 909-916.

40. Reeve, J. and Chen, S.P., "Versatile Interactive Digital Simulator Based on EMTP for AC/DC Power System Transients," Vol. PAS-103, No. 12, Dec. 1984, pp. 3625-3633.

41. Woodford, D.A., Gole, A.M. and Menzies, R.W., "Digital Simulation of DC Links and AC Machines," IEEE Trans., Vol. PAS-102, June 1983, pp. 1616-1623.

42. Woodford, D.A., "Validation of Digital Simulation of DC Links," IEEE Trans. Vol. PAS-104, No. 9, Sept. 1985, pp. 2588-2595.

43. Woodford, D., "Modelling of HVDC Systems Using EMTDC Package," a private communication.

44. Dommel, H.W., "Transformer Models in Simulation of Electromagnetic Transients," 5th Power System Computational Conference, Cambridge, England, Sept. 1-5, 1975, pp. 1-16.

45. Ontario Hydro Research Document, "Overvoltage Damage to Electronic Equipment in Homes," Ontario, Canada, Report No. 70-129-K, 1970.

46. Szechtman, M., et al., "HVDC Controls Affecting Stability of Low Short Circuit Ratio Networks," Symposium on Incorporating HVDC Power Transmission in System Planning, Phoenix, Arizona, March 24-27, 1980.

47. Kosiki, S. and Masada, E., "Control Characteristics of HVDC Link Connected to Weak AC Systems," Elect. Engg. in Japan, Vol. 96, No. 5, 1976, pp. 70-77.

48. Kauferle, J., et al., "HVDC Stations Connected to Weak AC Systems, "IEEE Trans., PAS-89, No. 7, Sept./Oct. 1970.

49. Harrison, R.E., "Type, Significance and Control of Overvoltages at Junction of AC-DC Systems," Overvoltage Compensation on Integrated AC-DC Systems Conference, Winnipeg, 1980, pp. 1-4.

50. Giesner, D.B. and Arrillaga, J., "Behavior of HVDC Link Under Balanced AC Fault Conditions,, Proc. IEE, Vol. 118, 1971, pp. 591-599.

51. Giesner, D.B. and Arrillaga, J., "Behavior of HVDC Link Under Unbalanced Faults," Proc. IEE, Vol. 119, No. 2, Feb. 1972.

52. Nagrath, J. and Gopal, M., "Control Systems Engineering," A Halsted Press Book, John Wiley & Sons: New York, 1979.

53. Nandam, P.K. and Sen, P.C., "A Comparative Study of Proportional-Integral (P-I) and Integral Proportional (I-P) Controller for DC Motor Drives," International Journal of Control, Vol. 44, No. 1, 1986, pp. 283-297.

54. Kaynak, O., et al., "Digital Speed Control of DC Motors with Integral Proportional Controller," Proc. of IFAC Conference on Control in Power Electronics and Electric Drives, Lausanne, Switzerland, 1983, pp. 501-506.

55. Lefebvre, S., Saad, M. and Hurtean, R., "Adaptive Control of HVDC Power Transmission Systems," IEEE Trans., Vol. PAS-104, No. 9, Sept. 1985, pp. 2329-2335.

56. Harris, C.J. and Billings, S.A. (Editors), "Self Tuning and Adaptive Control: Theory and Application," Peter Peregrinus Ltd., 1981.

57. Dyer, A. and Stewart, J., "Detection of Rolling Elements Bearings Damage by Statistical Vibration Analysis," Journal of Mechanical Design, Vol. 100, 1978, pp. 229-235.

58. Rabiner, L.R. and Schafer, R.W., "Digital Processing of Speech Signals," Prentice Hall Inc.: New Jersey, 1978.

59. Kalra, P.K. and Mathur, R.M., "A Way of Building Expert System for Power System for Monitoring and Control," Invited Paper for IASTED Conference on Emerging Technologies for Power System, Montana, U.S.A., Aug. 18-25, 1986.