

A New Adaptive Distance Relay

by

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A Thesis

submitted to the Faculty of Graduate Studies

in partial fulfilment of the requirements for the degree of

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A New Adaptive Distance Relay

BY

Hongwei Li

**A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University
of Manitoba in partial fulfillment of the requirements of the degree**

of

Doctor of Philosophy

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Summary

The Power System Research Group at the U of M has been developing a DSP based relay hardware. Numerous algorithms have already been written and proved on this hardware. The thesis focuses on improving the performance of the quadrilateral distance relay running on the hardware. An adaptive transmission line distance relay, referred to as the PT relay, is proposed in this thesis. The research includes the software modelling of the PT relay, PSCAD/EMTDC simulations, as well as hardware tests of the PT relay. An alternative hardware platform based on a Pentium is investigated and compared to the DSP hardware.

The thesis enhances the quadrilateral distance relay by adding some adaptive features. The new contributions of this work are as follows:

- 1). It allows the dynamic expansion of the quadrilateral characteristics and separate feature for the resistive and reactive expansion.
- 2.) It allows the direction element of the relay to control the expansion of the quadrilateral characteristics.
- 3). It allows the dynamic expansion of the quadrilateral to be viewed in the MATLAB model running in the PSCAD/EMTDC.
- 4). It presents a way to control the quadrilateral characteristics expansion according to the fault type by using the phase selection logic.
- 5). It allows a new platform board based on a Pentium to be compared with the present DSP platform.
- 6). It demonstrates the advantage in the speed and selectivity of the PT relay over the conventional Mho relay and quadrilateral relay.

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Finally, I would like to thank my wife and daughter. I could have finished this thesis without them, but without them my life would be empty and I would not care that I finished this thesis.

Lists of the symbols in the thesis

c_1, c_2 , and c_3 :	the coefficients which are used in the $S1$ signal composition.
DE:	direction element.
DI:	directional impedance element.
Dir :	fault direction signal.
E_m and E_n :	source voltage.
F1:	the fault point of the reverse fault.
F2:	the fault point of the forward point,
I_1, I_2, I_0 :	the positive sequence, negative sequence, and zero sequence current
IE:	the impedance element.
I_ϕ :	the phase current.
L :	the phase conductor inductance.
LI:	load impedance element.
K :	the zero sequence compensation coefficient.
M :	the mutual inductance between the phase conductors.
Mode:	one of the signals to control the characteristics of the PT relay.
PS:	the phase selection element.
PSII:	positive sequence incremental impedance.
PT relay:	the relay proposed in this thesis.
Relay:	the word to describe the power system protective device.
R_g :	the ground line resistance.
R_i :	a computed quantity for the PT relay characteristics.
R_l :	the phase conductor resistance.
$S1, S2$:	the two inputs of the Mho relay.
$u_a(t), u_b(t), u_c(t), i_a(t), i_b(t), i_c(t)$:	the instantaneous value of the three phase voltage and current.
$U_a, U_b, U_c, I_a, I_b, I_c$:	three phase voltage and current in phasor form.

U_{ag} : the phase A to ground voltage.
 $U_{c\phi}$: the cross polarized voltage.
 U_f : the voltage across the fault resistance.
 $U_{m\phi 1}$: the memory polarized positive sequence voltage.
 U_ϕ : the phase voltage.
 Z_{dir} : the directional impedance.
 Z_{ld} : the load impedance.
 Z_s and Z'_s : source impedance.
 Z_1, Z_2, Z_0 : the positive sequence, negative sequence, and zero sequence impedance.
 Z_{dir} : the measured directional impedance.
 Z_k : the measured impedance.
 ΔI_1 : the positive sequence incremental current.
 ΔU_1 : the positive sequence incremental voltage.
 $\phi_{ab1}, \phi_{ab2}, \phi_{bc1}, \phi_{bc2}, \phi_{ca1}, \phi_{ca2}$: the quantity used to select the fault phase.
 $S_A, S_B, S_C, S_{AB}, S_{BC},$ and S_{CA} : the phase selection signal.
 Vld_{dir}, Vld_{ld} : direction impedance available signal, and load impedance available signal.

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Chapter 1. Introduction

Electrical power distribution systems were first introduced toward the end of the last century. In comparison to today's systems, they were relatively simple, usually consisting of small generating stations that provided the needs of their immediate vicinities. As demand increased, larger systems were introduced and it became necessary to effectively protect both the electrical equipment and the continuity of supply.

Two separate instances of widespread system failure demonstrated that inadequate protection was in place. The first failure occurred in Britain in the winter of 1963[9], when an already heavily loaded system was subjected to a sudden increase in demand, coinciding with the simultaneous endings of separate programmes on both available television channels. The loss of a transmission line in the south-east of England led to overloads on other feeders in that area, which in turn were tripped out by their overload devices. Sequential tripping continued until sufficient load had been rejected for the remaining feeders to carry what little remained. The south-eastern area suffered a power cut lasting several hours while that part of the system was gradually reconnected. The second such failure occurred in November, 1965, in the CANUSE[15] system on the eastern seaboard of North America. A backup relay tripped out a heavily loaded, but healthy line which was one of several carrying power to the Toronto load area from the generating complex at Niagara. Its load was transferred to parallel feeders which tripped out and isolated the Toronto load area from its main source of power. The Ontario Hydro system was left with a net deficit of generation, and the Niagara Mohawk Power Corporation to the south with an excess of generation. Both systems gradually disintegrated: one due to a lack of power and the other due to a power surge. The southern system, including New York city, took about twelve hours to rebuild.

1.1. The transmission line protection

The widely scattered and numerous substations and generating plants are connected by transmission lines into a vast network. The direct benefit of these connections is to enable the transfer of electric power from the producer to the consumer across regions. For this reason, the proper functioning of a modern power system is heavily dependent upon the healthy operation of the trans-

mission lines within it.

When today's EHV and UHV transmission lines, (generally 132 KV or above) are exposed to treacherous weather, they are very likely to be subject to faults. Insulator failure may result in short circuits among phases and ground conductors. A lightning strike may break down the dielectric between phases and cause a short circuit between the phase and the ground conductors via arcing. A fault occurring on the transmission line might subsequently lead to a collapse at the system level if it were improperly handled.

The first relays used to handle line faults were either over-current or under-voltage detectors. As power demand and the resultant system complexity increased, these too were found to be lacking. The classic example used to demonstrate this is the case of two generators providing power to a common load. When a fault on one generator prevents it from supplying current, the second generator provides not only the load current but also the fault current for the first generator. The protection on the second generator would then operate and the supply would be lost. Even worse, if there were other supply points, the faulted generator would still be connected.

Further development produced more selective relays, designed to protect particular pieces of equipment. The relays' main consideration became whether a fault existed on the immediate piece of equipment which was being protected. Only in cases of protection failure would they be required to trip for faults on other parts of the system. This thesis is concerned with aspects of one such relay: the distance relay.

Distance relaying is now a well established technique for protecting power transmission lines against electrical fault conditions. By monitoring the line voltage and current as measured at the relaying point, the distance relay compares the system impedance with a pre-set reference representing the impedance of the protected line, and decides whether or not a fault condition exists on that line. If a fault is detected, the relay output provides instruction to the relevant circuit isolation equipment to disconnect the faulted section. Fig.1.1 is a typical power system protective relay for UHV and EHV transmission line.

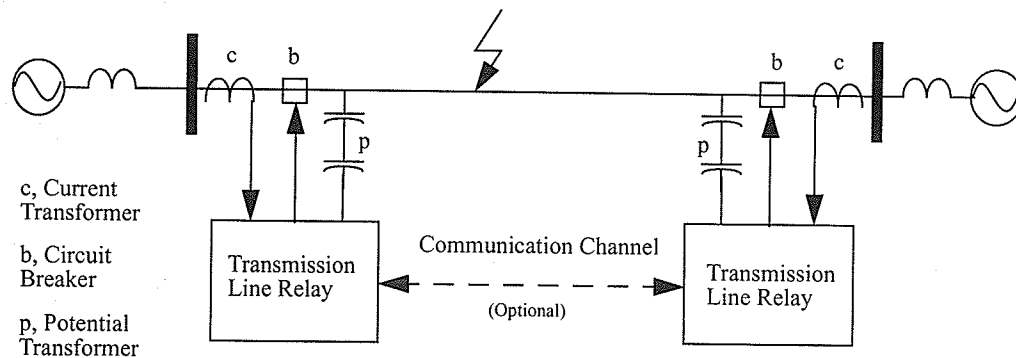


Figure 1.1. The Transmission Line Protective Relay.

The relay's decision to trip is made if the impedance measured by the relay is less than the total line impedance. Under most fault conditions the fault impedance is not simply that of the line up to the fault point, but also includes both arc and earth impedances which lie within the protected area of the impedance diagram and contain all the probable fault impedance associated with the protected line. This area is the trip or polar characteristic for the relay[15].

Trip characteristics are chosen to provide fault clearance for all possible fault conditions on the protected line, but not to include impedances resulting from faults on the associated circuits or abnormal operating conditions, and to optimize the relay technique used.

1.2. The conventional distance relay

For the distance relay, the measured impedance of the faulty phase element is expected to be the actual impedance involved in the fault loop. Since the distance relay works according to the length of the faulty line, it can monitor an effectively fixed reach in a variety of system configurations. This is the characteristic that makes the distance relay a favourite in the EHV and UHV line protection schemes.

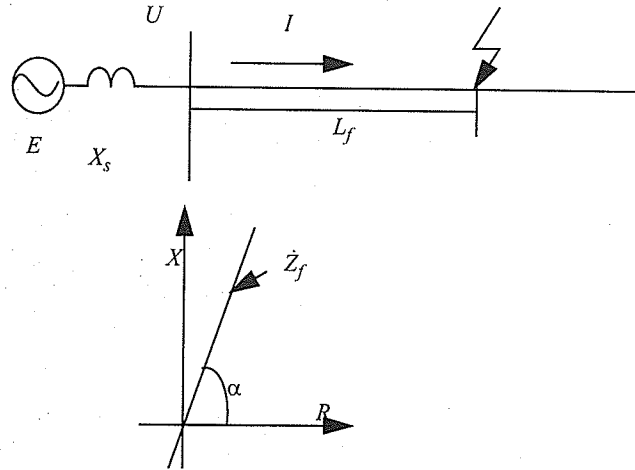


Figure 1.2. The Measured Impedance in the Fault Loop.

Figure 1.2 shows a fault on the transmission line and the measured impedance within the fault loop. Z_f is the actual impedance in the fault loop and L_f is the length of transmission line in the fault loop. Z_f equals the product of the impedance per length unit (a complex constant), and L_f . Z_f keeps a constant impedance angle α on the impedance plane.

Two types of distance relay characteristics are widely used in the protection of transmission lines. They are the Mho characteristic and the quadrilateral characteristic. Immediately following is a brief introduction of their features during fault.

1.2.1. The Mho distance relay

A popular trip characteristic is the Mho circle. The Mho characteristic is the inversion of a straight line "ohm" characteristic with respect to the origin[9]. The Mho relay generally takes in two phasor signals as its inputs. The Mho relay typically compares the phase angle and trips only when the angle difference is within a specific range. The Mho relay can also be implemented by comparing the phasor amplitudes. Fig. 1.3 shows a power system in which the Mho samples the voltage at the busbar and current from the line it is protecting.

Developed in the early 1930's, the Mho circle was found to be better suited to long transmission lines than the then popular conventional reactance and impedance characteristics. It was found to be less susceptible to trip on power swings or on reverse fault on associated phases. Due to a

tighter fit around the possible fault area, it had an immunity to load encroachment. The Mho characteristic has several advantages: the first, the Mho characteristic can provide a closed characteristic covering the fault zone with one comparator while the quadrilateral relay needs two comparators; the second practical advantage is that the Mho circle combines functions of both directional and measuring relays, and therefore the protection requires only one relay element. The characteristics of the Mho relay are somewhat adaptive during the fault. In figure 1.3, a fault at F2 represents a forward fault and at F1 a reverse fault. For a forward fault, the protection zone is the inner area of circle b before the fault and transforms into the inner area of circle a at the initiation of the fault. The measured impedance of the Mho relay is located in the first quadrant of the impedance plane. For a reverse fault, the protection zone is the inner area of circle b before the fault and transforms into the inner area of circle c at the initiation of the fault. The measured impedance of the Mho relay is located in the third quadrant of the impedance plane. In this way, the Mho relay can have a large trip zone for the forward fault which enhances its identifying ability during forward fault and reduces its misoperation opportunity during a reverse fault.

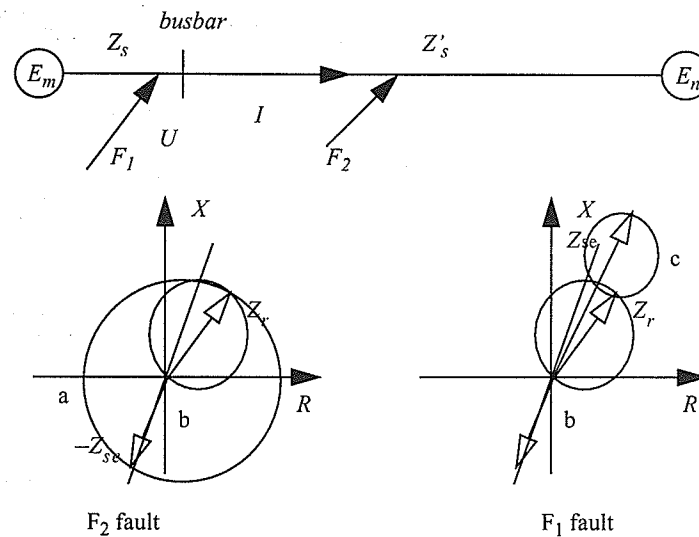


Figure 1.3. Behaviour of the Mho Relay.

1.2.2 The quadrilateral distance relay

With the expansion of power supply networks, an even tighter fitting characteristic than that of the Mho circle has become desirable. Examining the anticipated fault areas for long and short lines,

Rushton and Humpage[15] demonstrated the limitations of the Mho circles. This is illustrated in fig.1.4, where it is shown that for very long lines, the Mho circle includes too great a fault area, and that for a short line, it fails to include a proportion of the anticipated fault area. In both cases the anticipated fault area approximates to a quadrilateral shape. For such a situation, a quadrilateral characteristic is preferable to the Mho circle.

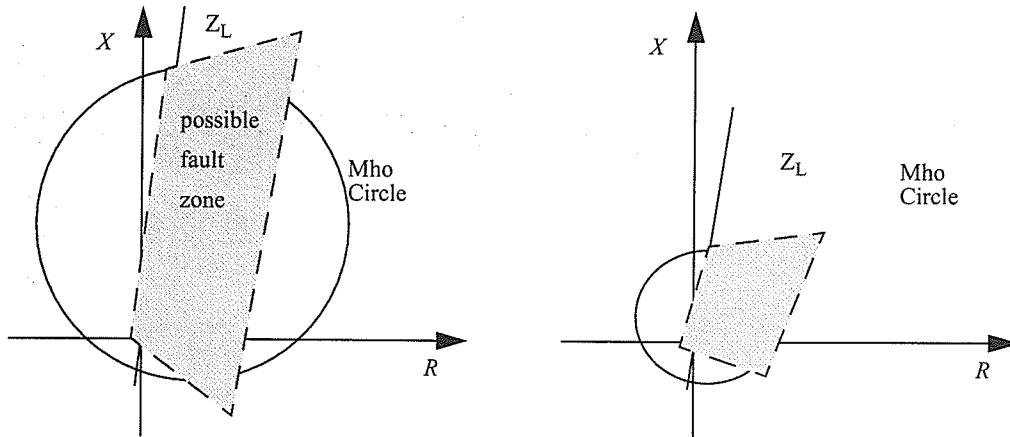


Figure 1.4. Possible Fault Impedance & Mho Circle.

The quadrilateral distance relay has a quadrilateral trip zone. When the measured impedance of the relay locates in its trip zone, it will trip.

1.3. Improving the performance of the quadrilateral relay

Although the quadrilateral relay fits a possible fault more tightly, it is slower in a fault. Figure 1.5 shows the Mho relay and the quadrilateral relay's characteristics in the impedance plane, as well as the impedance locus obtained during a forward fault in the power system simulation. The impedance locus traverses into the trip zone of the relay in the horizontal direction. In such a case, the Mho relay gives a faster trip than the quadrilateral relay.

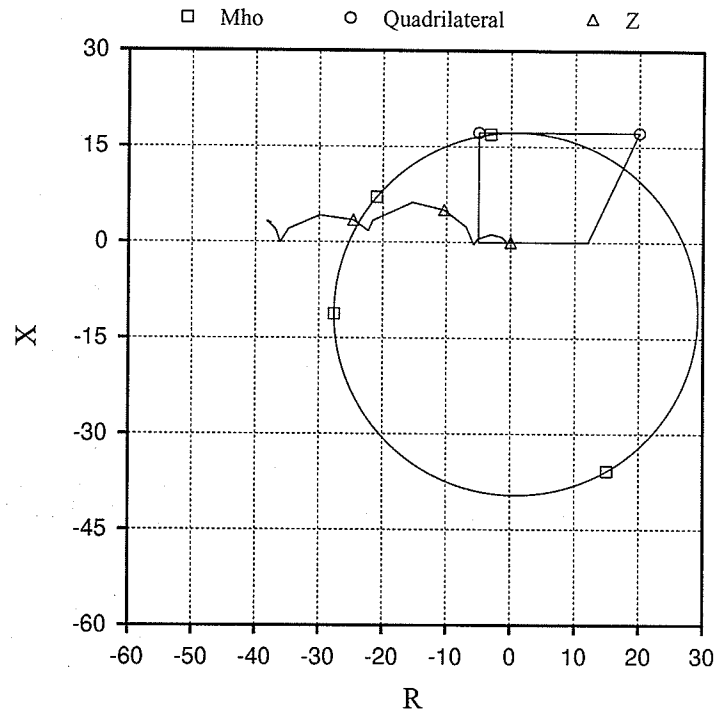


Figure 1.5. Relay Characteristics & Impedance Locus.

In addition to the disadvantage of lesser response speed, the inadequacy of the quadrilateral relay in the presence of series compensation is evident. When a capacitor is installed in front of the quadrilateral relay, the relay measures a capacitive impedance in a forward fault. If the relay is set to trip this fault, the relay will misoperate in the reverse close in fault (in the worst case, the impedance is zero).

However, a quadrilateral characteristic does have a tighter fit with possible fault impedance in non series compensated cases. This nature makes it less likely to misoperate than Mho characteristics. With most electrical supply equipment, it is possible to mitigate the effects of electrical faults, notably the short circuit, simply by disconnecting the faulty equipment as quickly as possible. This ensures that system stability is maintained, unfaulty circuits are not interfered with and that the fault current causes the minimum destruction.

This thesis proposes a new adaptive quadrilateral relay to improve the quadrilateral relay's response in a fault. In subsequent chapters, this relay is termed "PT relay" short for the Power

Tower, the place where it was created.

1.4. The tools used in the thesis

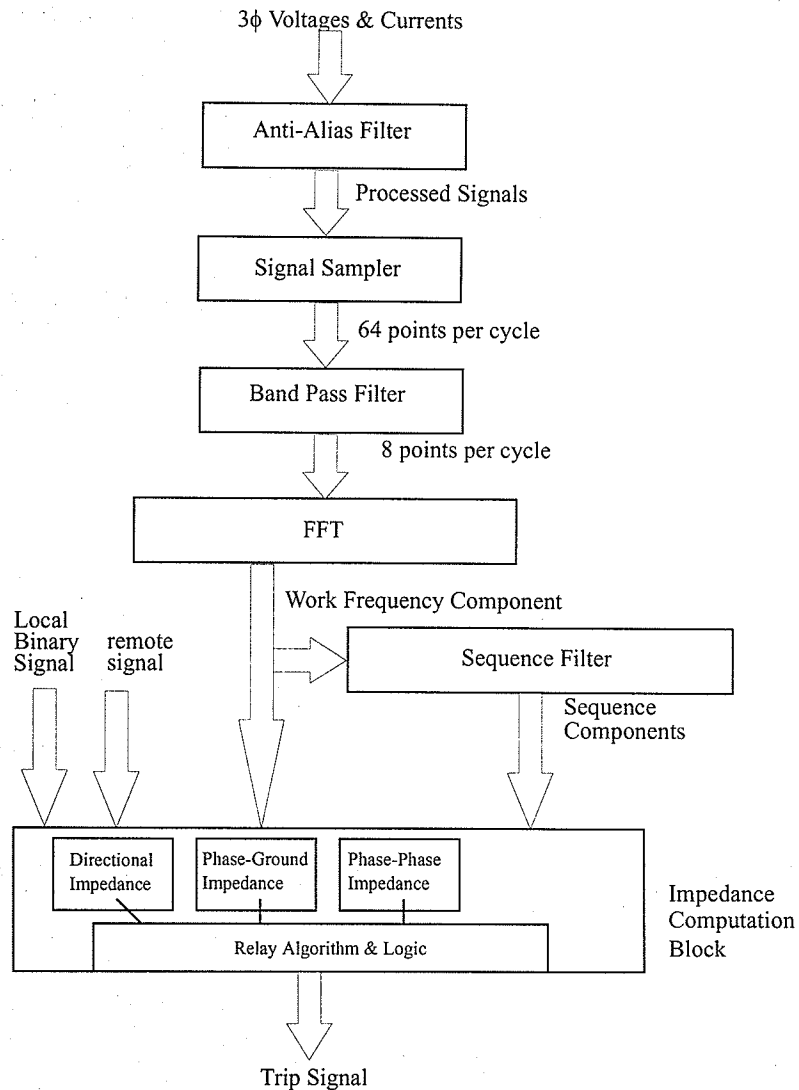


Figure 1.6. The Existing Digital Relay Structure.

Figure 1.6 demonstrates the existing software model of the digital relay at the start of this project[47]. Starting from this point, the PT relay specific components will be added into the software model. The additions include load impedance element, phase selection element, adaptive zone control algorithm. To test the PT relay components, Fortran models of the PT relay will be

developed. To demonstrate the adaptive feature, a MATLAB software model embedded in the PSCAD/EMTDC simulation will be created. The PT relay performance in the EHV single transmission line and double transmission line fault is evaluated in this chapter. Finally, the PT relay algorithm is implemented in two hardware applications.

PSCAD is a graphical user interface, providing a very flexible interface to the electromagnetic transients simulation software EMTDC. EMTDC is the library of power system component models and procedures which constitutes the simulation software. Together, these two software packages are referred to as "PSCAD/EMTDC" and the combination allows the engineer to set up and run a wide variety of power system simulation.

MATLAB is an integrated technical computing environment that combines numeric computation, advanced graphics and visualization, and a high-level programming language.

TMS320 DSP is a microprocessor developed by the Texas Instrument for real time application.

Pentium is a microprocessor developed by Intel. TMS320 and Pentium are used as the microprocessors of the hardware application.

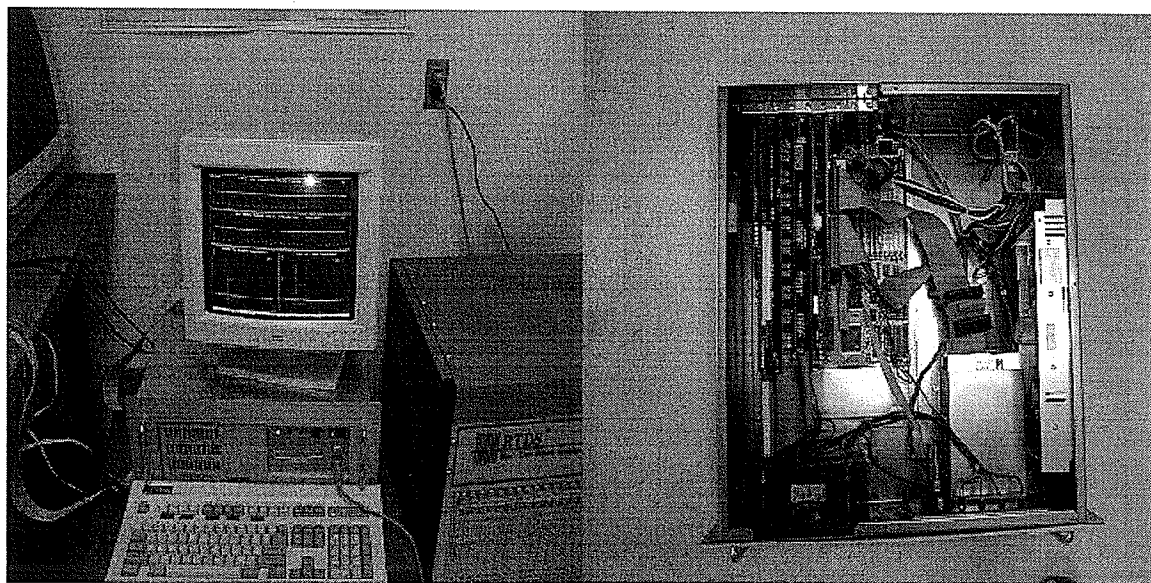


Figure 1.7. The TMS320 DSP Relay Apparatus.

Figure 1.7 shows the TMS320 DSP relay apparatus. The left hand part of the figure is the relay which is an industrial grade PC with an embedded TMS320 board. The right hand part of the figure shows the 286 motherboard with a number of vertical plug in boards including the DSP board. Playback(RTP) is a relay test package developed by the Manitoba HVDC Research Center. Play-

back along with conditioning amplifiers can produce the secondary side voltage and current based on the input file.

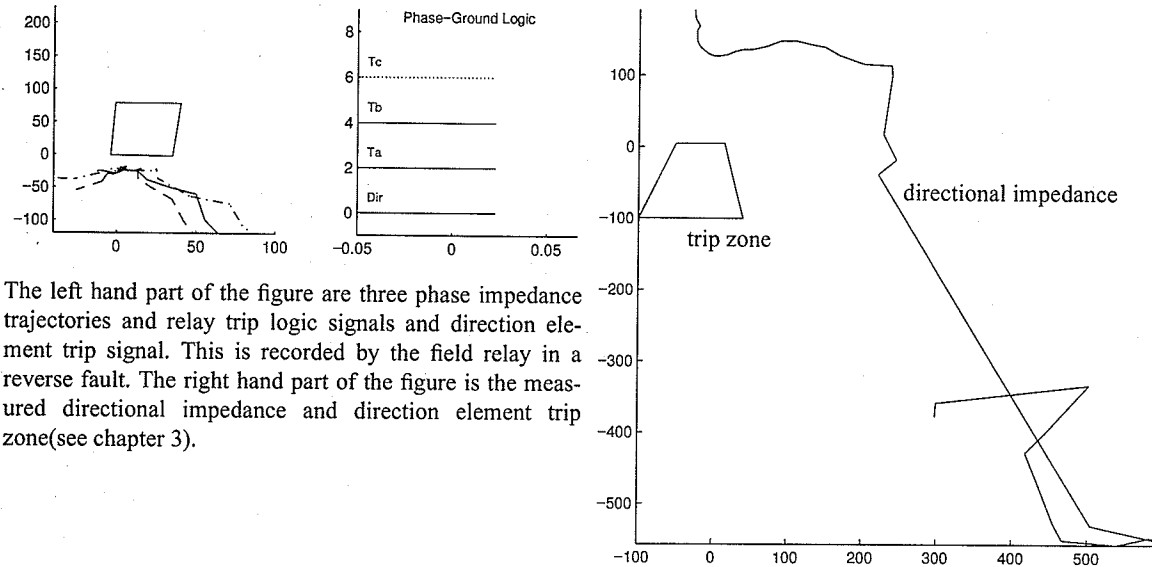


Figure 1.8. The Reverse Field Fault Case on Dorsey-Forbes 500KV System.

Figure 1.8 demonstrates a case from the Dorsey-Forbes 500KV system[1] prior to the start of this thesis. A practical PT relay is installed at the Dorsey end of the 500KV line from Dorsey to Forbes. The relay is not connected to the breaker but serves as a test bed in which new algorithms developed in the research can be run with real input waveforms from the 500KV line. The relay is linked to the Power Tower in the U. of M. by modem.

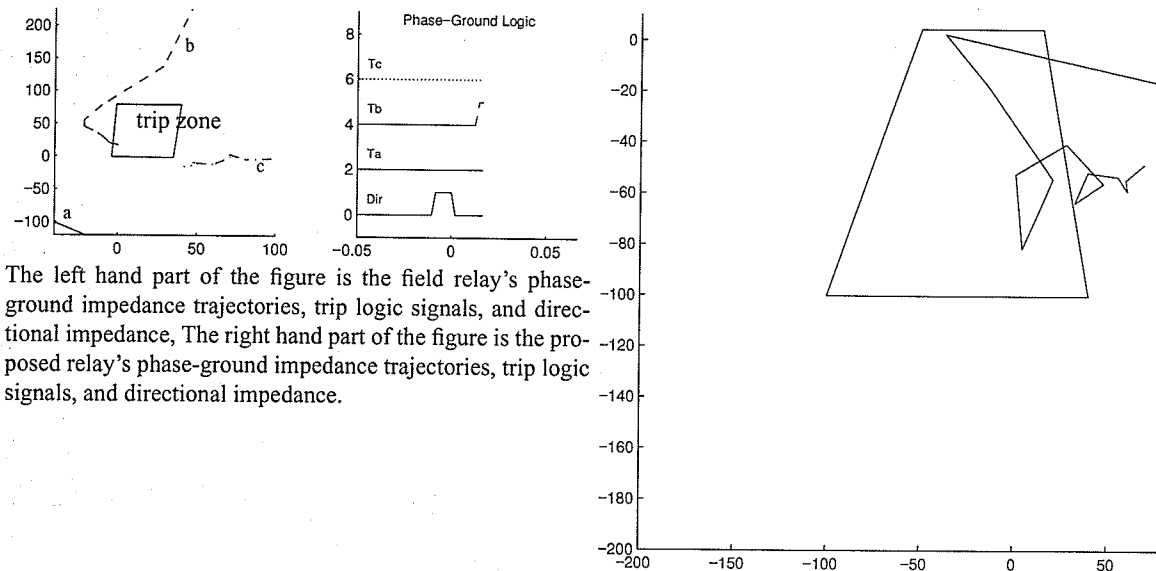


Figure 1.9. The Forward Field Fault Case on Dorsey-Forbes 500KV System.

Figure 1.9 is a forward case recorded by the field relay. The field relay is a quadrilateral relay which has a trip zone shown in the figure. In the field relay, the trip signal is gated by the directional element (Dir). In this fault, when the measured impedance of phase B comes into the trip zone, the directional element has dropped down, so the relay is not tripped in the forward fault. Improvements are therefore required in the relay performance.

1.5. An overview of the remaining chapters of this thesis

Chapter 2 presents the introduction of the basic power system protective relay theory.

Chapter 3 introduces the PT relay principle.

Chapter 4 presents the simulation cases to investigate the direction impedance element.

Chapter 5 presents the simulation cases to verify the components of the PT relay.

Chapter 6 presents the simulation cases to verify PT relay.

Chapter 7 presents a method to evaluate a relay's behaviour using an accurate software model.

Chapter 8 presents two hardware applications of the PT relay.

Chapter 9 presents the conclusion of the thesis and future work.

Chapter 2. Overview of the Distance Relay

This chapter consists of a discussion of the theory of the measurement of fault impedance, the Mho relay's characteristics, the quadrilateral relay's characteristics, and finally, the principle of the PT relay. It is general practice to employ two sets of relay elements to protect a transmission line. One set of three relay elements is connected to protect against phase-phase faults, while the other set is connected to protect against phase-ground faults. All six elements measure simultaneously and discriminate between faulted and healthy phases. This chapter confines its analysis to the case of the relays described above.

2.1. The measurement of the fault impedance

The measurement of impedance is essential if the distance relay is to safeguard the transmission line by evaluating the relationship between its trip zone and the location of its perceived impedance in the impedance plane. For a single lumped impedance object, the impedance value can be obtained by dividing the voltage across it by the current through it. However, a typical power system is a three phase system with mutual coupling among phases. Due to the mutual coupling among three phases, all three phase currents contribute to the voltage across a segment of line conductor. The resultant measurement of line impedance is more complicated than the lumped impedance model. Beneath the complexity of measurement lies the actual workings which will be analysed in the remainder of this section.

Figure 2.1 illustrates a typical power system with two sources, modelled with ideal voltage sources, and a three phase transmission line, modelled with lumped parameters. Analysis will focus on the segment of transmission line from the left hand busbar to point F. The resistance is identical in the conductor of each phase and is represented by R_l . The resistance of the ground line is represented by R_g . The inductance is identical in the conductor of each phase and is represented by L , and the mutual inductance is identical for any two lines and is represented by M . The instantaneous current through the line of each phase is represented by $i_a(t)$, $i_b(t)$, $i_c(t)$ and the instanta-

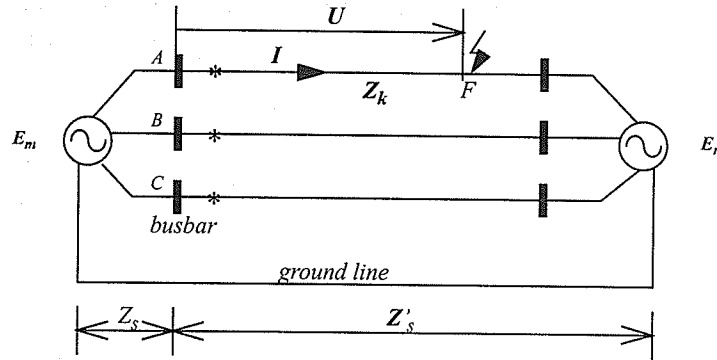


Figure 2.1. A Typical Power System.

neous voltage is represented by $u_a(t), u_b(t), u_c(t)$.

Equation 2.1 describes the relationship among the voltages, currents, and impedance.

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} R_l + R_g & R_g & R_g \\ R_g & R_l + R_g & R_g \\ R_g & R_g & R_l + R_g \end{bmatrix} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \begin{bmatrix} \frac{d}{dt} i_a(t) \\ \frac{d}{dt} i_b(t) \\ \frac{d}{dt} i_c(t) \end{bmatrix} \quad 2.1$$

In the fundamental phase domain, equation 2.1 is transformed into equation 2.2 in which three phase currents and voltages are represented by: I_a, I_b, I_c and U_a, U_b, U_c in phasor form.

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} R_l + R_g & R_g & R_g \\ R_g & R_l + R_g & R_g \\ R_g & R_g & R_l + R_g \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} + j\omega \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \quad 2.2$$

By applying the abc-120 transformation as in equation 2.3 to equation 2.2, equation 2.4 is obtained. Equation 2.4 is a succinct description of the relationship between sequence variables and the sequence network parameters of the lines. U_{a1}, U_{a2}, U_0 represent the positive sequence voltage of phase A, the negative sequence voltage of phase A, and the zero sequence voltage. I_{a1}, I_{a2}, I_0 represent sequence currents.

$$\begin{bmatrix} U_{a1} \\ U_{a2} \\ U_0 \end{bmatrix} = T \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix}, \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_0 \end{bmatrix} = T \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix}, T = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix}, T^{-1} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix}, a = e^{\frac{j2\pi}{3}} \quad 2.3$$

Here, $Z_1 = Z_2 = R_l + j\omega(L - M)$, $Z_0 = (R_l + 3R_g) + j\omega(L + 2M)$.

$$\begin{bmatrix} U_{a1} \\ U_{a2} \\ U_0 \end{bmatrix} = \begin{bmatrix} Z_1 & 0 & 0 \\ 0 & Z_2 & 0 \\ 0 & 0 & Z_0 \end{bmatrix} \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_0 \end{bmatrix} \quad 2.4$$

Applying the 120-abc transformation to equation 2.4, equation 2.5 is obtained.

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = T^{-1} \begin{bmatrix} U_{a1} \\ U_{a2} \\ U_0 \end{bmatrix} = T^{-1} \begin{bmatrix} Z_1 & 0 & 0 \\ 0 & Z_2 & 0 \\ 0 & 0 & Z_0 \end{bmatrix} \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_0 \end{bmatrix} = T^{-1} \begin{bmatrix} Z_1 & 0 & 0 \\ 0 & Z_2 & 0 \\ 0 & 0 & Z_0 \end{bmatrix} \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_0 \end{bmatrix} + T^{-1} \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & Z_0 - Z_1 \end{bmatrix} \begin{bmatrix} I_{a1} \\ I_{a2} \\ I_0 \end{bmatrix} \quad 2.5$$

Simplifying equation 2.5, equation 2.6 is obtained.

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} I_a Z_1 + I_0 (Z_0 - Z_1) \\ I_b Z_1 + I_0 (Z_0 - Z_1) \\ I_c Z_1 + I_0 (Z_0 - Z_1) \end{bmatrix} = \begin{bmatrix} (I_a + KI_0) Z_1 \\ (I_b + KI_0) Z_1 \\ (I_c + KI_0) Z_1 \end{bmatrix}, K = \frac{Z_0 - Z_1}{Z_1} \quad 2.6$$

In equation 2.6, symbol K represents the zero sequence compensation coefficient.

A distance relay normally requires six elements to measure impedance. These elements are three phase-ground elements for phase A, B, and C and three phase-phase elements for AB, BC, and CA.

2.1.1. The impedance “seen” by a phase relay in a phase-ground fault

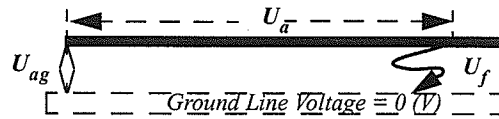


Figure 2.2. The Phase-Ground Voltage in a Ground Fault.

A phase-ground fault results from an undesired connection between a phase conductor and a ground conductor. The resistance involved in such a connection is called fault resistance. If phase A is involved in a phase-ground fault, the voltage referred to ground of phase A at the busbar is expressed as equation 2.7.

$$U_{ag} = U_a + U_f = (I_a + KI_0) Z_1 + U_f \quad 2.7$$

U_{ag} is the phase-ground voltage at the busbar for phase A, U_f is the voltage across the fault resistance. The measured impedance is obtained as Z_k equation 2.8.

$$Z_k = \frac{U_{ag}}{I_a + KI_0} = Z_1 + \frac{U_f}{I_a + KI_0}, I_0 = \frac{I_a + I_b + I_c}{3} \quad 2.8$$

In a metallic ground fault, $U_f = 0$, so that the measured impedance is the line positive sequence impedance in the fault loop.

2.1.2. The impedance “seen” by a phase-phase relay in a phase-phase fault

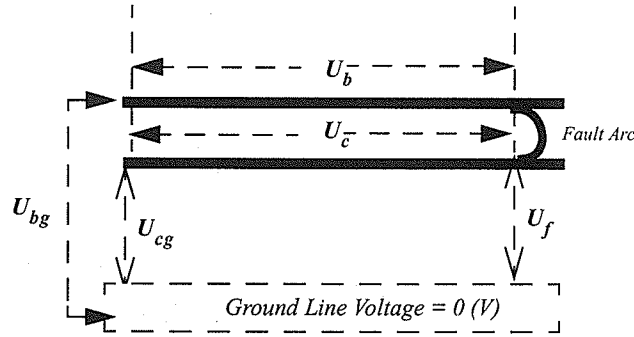


Figure 2.3. The Phase-Ground Voltage in a Phase-Phase Fault.

A phase-phase fault results from an undesired connection between phase conductors. When a phase-phase fault happens at phase B and C, the fault arc resistance between the two fault phases is usually very small and the voltage across the fault resistance is negligible, so the voltage at the fault point of phase B and phase C are equal. The measured impedance is obtained through equation 2.9.

$$Z_k = \frac{U_{bg} - U_{cg}}{I_b - I_c} = \frac{(U_b + U_f) - (U_c + U_f)}{I_b - I_c} = \frac{U_b - U_c}{I_b - I_c} = \frac{(I_b + KI_0)Z_1 - (I_c + KI_0)Z_1}{I_b - I_c} = Z_1 \quad 2.9$$

In phase-ground, phase-phase-ground, and three-phase metallic faults, the measured impedance Z_k of a phase-ground relay is the line positive sequence impedance Z_1 up to the fault. In phase-phase, phase-phase-ground, and three-phase metallic faults, the measured impedance Z_k of a phase-phase relay is the line positive sequence impedance Z_1 up to the fault.

Faults on a single transmission line can be classified as four types according to the phase pattern involved in the fault. The fault types include phase-ground, phase-phase, phase-phase-ground, and three-phase fault. In a phase-phase-ground fault, the phase-phase element and phase element in the faulted phases can measure the line positive sequence impedance in the fault loop. In a three-phase fault, all of the six elements can measure the impedance in the fault loop. Therefore, six phase elements, A, B, C, AB, BC, and CA can cover all possible faults on a single line.

Later in this thesis, the distance relay's behaviour will be explored in terms of the faults AG, BC, BCG, and ABC since they represent all the possible transmission line fault types.

2.2. The characteristic of the Mho relay

The Mho relay is among the most frequently used distance relays for transmission line protection. The popularity of its application is due to its adaptive nature and technical simplicity. The Mho relay can be implemented in the form of either a phase comparator or an amplitude comparator. Since these two implementations are equivalent, we will only introduce the phase comparator. In this thesis, the Mho relay refers to the phase comparator Mho relay.

2.2.1. The theory of the Mho distance relay

The Mho relay has two phasor inputs. The Mho relay trips only when the angle difference of its inputs falls within a specific range. The two common phasor inputs are $S1 = U_\phi - I_\phi Z_r$ and $S2 = c_1 U_{m\phi 1} + c_2 U_{c\phi} + c_3 U_\phi$. Here, Z_r is the reach or setting impedance. U_ϕ and I_ϕ are the phase voltage and current, respectively. For examples, $U_\phi = U_{AB}$ and $I_\phi = I_{AB}$ for the AB phase. $U_{c\phi}$ is the cross polarized voltage. For the phase A element, $U_{c\phi} = jU_{AB}/\sqrt{3}$. For the phase BC element, $U_{c\phi} = -\sqrt{3} \cdot jU_A$. $U_{m\phi 1}$ is the memorized positive sequence voltage of the phase. $U_{m\phi 1}$ equals the positive sequence voltage of several cycles ago. c_1, c_2 and c_3 are real or complex constants. The presence of $U_{m\phi 1}$ and $U_{c\phi}$ in $S2$ prevents the Mho relay from using zero $S2$ in a close-up fault where U_ϕ is zero.

The operational criterion of a Mho relay is $\pi/2 \leq \angle(S1/S2) \leq 3\pi/2$.

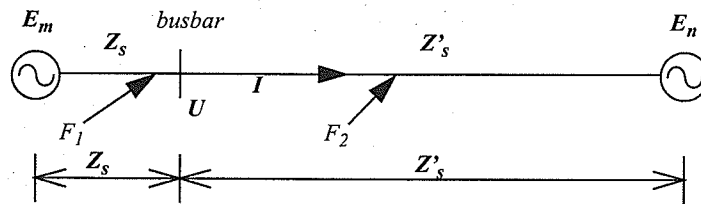


Figure 2.4. The Simple Power System.

Let $Z_k = U_\phi / I_\phi$, $Z_{e1} = U_{m\phi1} / I_\phi$ and $Z_{ec} = U_{c\phi} / I_\phi$, the value $S1/S2$ can be found through equation 2.10.

$$S1/S2 = \frac{U_\phi - I_\phi Z_r}{c_1 U_{m\phi1} + c_2 U_{c\phi} + c_3 U_\phi} = \frac{Z_k - Z_r}{c_3 Z_k + c_1 Z_{e1} + c_3 Z_{ec}} \quad 2.10$$

The characteristic can be obtained by examining the two impedances Z_{e1} and Z_{ec} (appendix A will explain how to calculate the two impedances). To simplify the analysis, the ABC fault is used to exhibit the Mho relay's behaviour. In this fault, its measured impedance is the line positive sequence impedance up to the fault.

The distance relay usually identifies and trips a fault located inside its protection zone within one or two cycles when it is used as zone one protection, hence the Mho characteristic at the moment of fault are of particular interest.

The power system illustrated in figure 2.4 is used to analyse the characteristic of the Mho relay.

2.2.2. The characteristic in a forward fault

A fault at point F2 in the power system in figure 2.4 is designated as a forward fault. The Mho relay has different trip zones before the fault and at the initiation of the fault. The discussion of its trip zones involves two steps (see appendix A for detailed discussion).

Step 1: Finding the trip zone before the fault

Before the fault, $Z_k = Z_{e1} = Z_{ec}$. By replacing the variables Z_{e1} and Z_{ec} in equation 2.10, equation 2.11 is obtained. The trip zone is the inner area of the dashed circle in figure 2.5, and the prefault load impedance indicated by the dashed line falls far outside the trip zone.

$$S1/S2 = \frac{Z_k - Z_r}{(c_1 + c_2 + c_3) Z_k} \quad 2.11$$

Step 2: Finding the trip zone at the initiation of the fault

The two equivalent impedances can be expressed in equation 2.12.

$$\begin{aligned} Z_{e1} &= U_{m\phi1} / I_\phi = r E_{m\phi} / I_\phi = r (Z_k + Z_s) \\ Z_{ec} &= U_{c\phi} / I_\phi = I_\phi Z_k / I_\phi = Z_k \end{aligned} \quad 2.12$$

$U_{m\phi1}$ is constant before the fault. $E_{m\phi}$, the power source internal voltage behind the source impedance Z_s , is always constant. Therefore, $U_{m\phi1}$ can be expressed by the multiplication of r , a com-

plex constant, and $E_{m\phi}$.

After replacing the z_{e1} and z_{ec} in equation 2.10 with equation 2.12, equation 2.13 is derived,

$$S1/S2 = \frac{Z_k - Z_r}{c_3 Z_k + c_1 r (Z_k + Z_s) + c_2 Z_k} = \frac{Z_k - Z_r}{(c_1 r + c_2 + c_3) (Z_k + Z_{se})} \quad 2.13$$

Here $Z_{se} = \frac{c_1 r Z_s}{c_1 r + c_2 + c_3}$.

The inner area of the solid circle crossing the points $-Z_{se}$ and Z_r in the impedance plane is the trip zone of the Mho relay[7]. The measured impedance Z_k should locate itself in the first quadrant somewhere. A fault within the reach of the Mho relay causes Z_k to move into the solid circle. The benefit of the Mho characteristic is that a zero impedance in the close-up forward fault is well inside the trip zone as opposed to being on the boundary of the prefault zone.

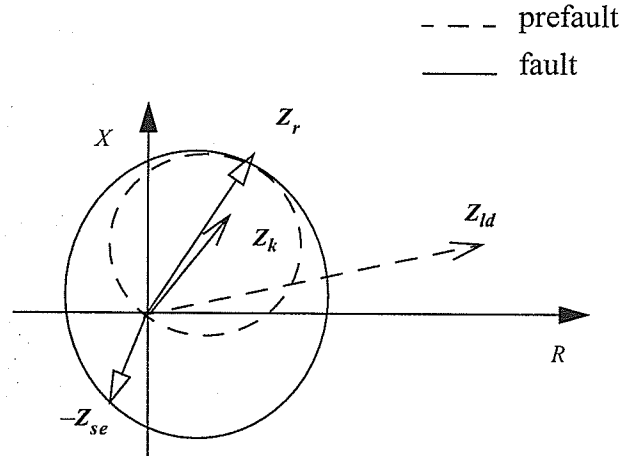


Figure 2.5. Behaviour of the Mho Relay in the ABC Forward Fault.

2.2.3. The characteristic in a reverse fault

A fault at point F1 in the power system in figure 2.4 is designated as a reverse fault. As in the analysis of the Mho characteristic in a forward fault, the Mho characteristic in a reverse fault is analysed by two steps.

Step 1: Finding the trip zone before the fault

Before the fault, the power system operates under the same conditions and the relay senses the same voltage and current as in the prefault condition in a forward fault. Accordingly, the trip zone of the Mho relay is the inner area of the dashed circle in figure 2.6 and the prefault impedance falls outside the trip zone.

Step 2: Finding the trip zone at the initiation of the fault

The two equivalent impedances can be expressed by equation 2.14 and equation 2.15(appendix A).

$$Z_{e1} = U_{m\phi 1}/I_{\phi} = rE_{n\phi}/I_{\phi} = r(Z_k - Z_s) \quad 2.14$$

$$Z_{ec} = U_{c\phi}/I_{\phi} = I_{\phi} Z_k / I_{\phi} = Z_k \quad 2.15$$

By replacing the Z_{e1} and Z_{ec} in equation 2.9 with equation 2.14 and 2.15, equation 2.16 is derived.

$$S1/S2 = \frac{Z_k - Z_r}{c_3 Z_k + c_1 r(Z_k - Z_s) + c_2 Z_k} = \frac{Z_k - Z_r}{(c_1 r + c_2 + c_3)(Z_k - Z_{se})} \quad 2.16$$

$$\text{with } Z_{se} = \frac{c_1 r Z_s}{c_1 r + c_2 + c_3}$$

The inner area of the solid circle is the trip zone of the Mho relay at this moment. The measured impedance Z_k locates itself somewhere in the third quadrant. The benefit of the Mho characteristic is that a zero impedance in the close-up reverse fault is well outside the trip zone as opposed to being on the boundary of the prefault zone.

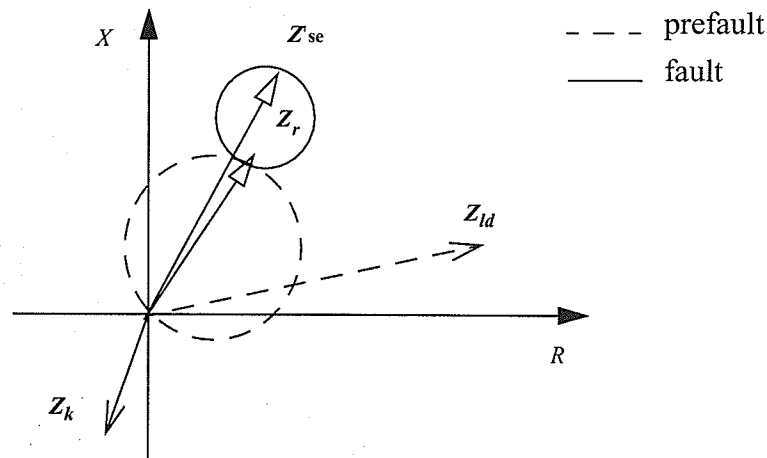


Figure 2.6. Behaviour of the Mho Relay in the ABC Reverse Fault.

2.3. The quadrilateral distance relay

The analysis of the characteristic of the quadrilateral relay is much simpler than that of the Mho relay. As its name implies, the trip zone of the quadrilateral relay is a quadrilateral zone in the impedance plane. For the phase-comparator quadrilateral relay, if the polarized voltage is added into its input phasors, the quadrilateral relay can also be adaptive to the fault direction. However the speed of the phase-comparator quadrilateral is slow[17]. Another quadrilateral relay uses fixed quadrilateral zone as its characteristic. The trip zone of such a relay is not influenced by the fault type and the fault direction.

The quadrilateral distance relay trips when the measured impedance falls inside its trip zone.

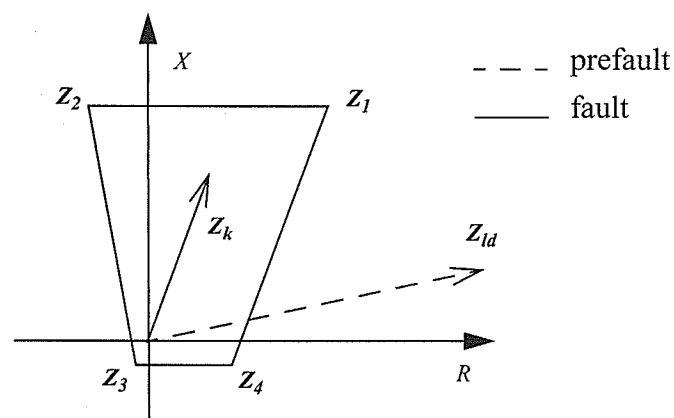


Figure 2.7. The Trip Zone of the Quadrilateral Relay.

Chapter 3. The PT Relay

The polarized Mho relay is adaptive to the fault since the Mho circle boundary shifts away from the origin according to the fault direction. This shift changes the trip zone in both the horizontal and the vertical direction.

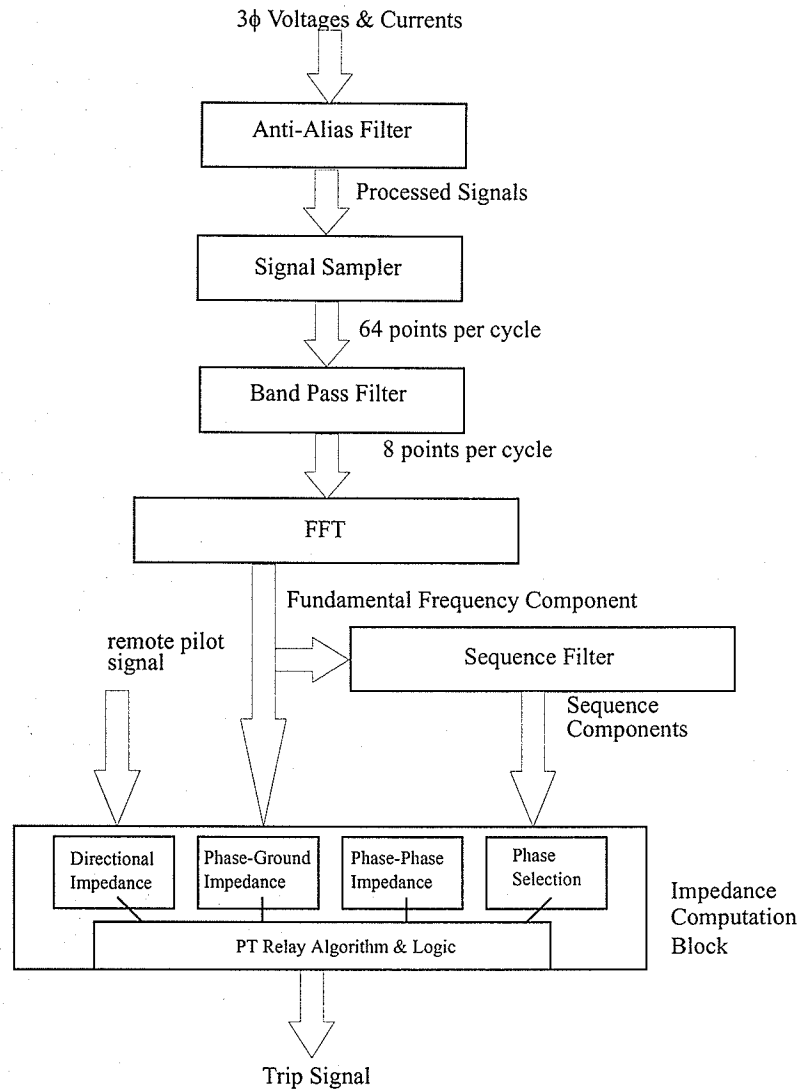


Figure 3.1. The PT Relay Structure.

The characteristic of the simple quadrilateral relay is not influenced by the fault direction, as stated in chapter 2. The PT relay will be adaptive by modifying its trip zone in the vertical direction and the horizontal direction in the similar way. In the forward fault, the expansion of the trip

zone of the phase-phase elements in the phase-ground fault may cause the phase-phase element to misoperate because of the horizontal expansion of the trip zone of the unfaulted phase. To eliminate the undesired expansion in the unfaulted phase, the phase selection element is added into the original software model. Unlike the Mho relay, the modification amount of the trip zone is independent in the vertical direction and the horizontal direction in a fault.

Figure 3.1 shows the software model structure of the PT relay. It differs the existing digital relay structure in figure 1.6. The PT relay has phase selection algorithm, and the relay implements the relay algorithm and logic specific for the PT relay.

3.1. The algorithm of the PT relay

The PT relay is a microprocessor-based adaptive relay. Before the advent of the microprocessor in the relay industry, the relay algorithm was implemented by analog hardware. It was rather difficult to implement any sophisticated method since the complexity of the hardware connection required by the algorithm's complexity was not affordable. Moreover, the distance relay was implemented either as a phase comparator or as an amplitude comparator because calculating the fault loop impedance was an impossible task.

With the development of modern electronic and digital processing technology, long awaited changes took place. The digital relay is a combination of software and hardware. By changing the software of the digital relay, the relay performs different functions. The computational ability of the digital relay allows sophisticated and complicated computation, such as Fast Fourier Transformation(FFT), sequence phasor computation. The digital memory component of the relay make it possible to calculate the incremental phasor computation. Together, the relay is qualified to meet the increasing system demands.

The PT relay enhances the quadrilateral relay's characteristics by realizing the virtues of both the quadrilateral relay and the Mho relay into one entity. The PT relay is a quadrilateral relay, but its protection zone is adaptive to the faults like the Mho relay. In other words, the PT relay dynamically changes its trip zone according to the fault. To improve faulted phase protection, the faulted phase elongates its trip zone into the 3rd and 4th quadrants during a forward fault and flips up its trip zone into the 1st and 2nd quadrants during a reverse fault. Since the directional impedance(Section 3.2) of the PT relay can reflect the system impedance from the relay to the source

and fault direction, this feature is implemented by adding the positive sequence incremental reactance to the lower two setting points Z_3 and Z_4 in figure 2.7. To quickly capture a forward fault, the protection zone is also expanded horizontally, and the prefault load impedance is used as an index to determine the expanding amount. To reduce the possibility of misoperation of the relay in the unfaulted phases, the expansion is confined to the faulted phase and a phase selection algorithm is used to select the faulted phase. Together, these requirements describe the architecture of the PT relay.

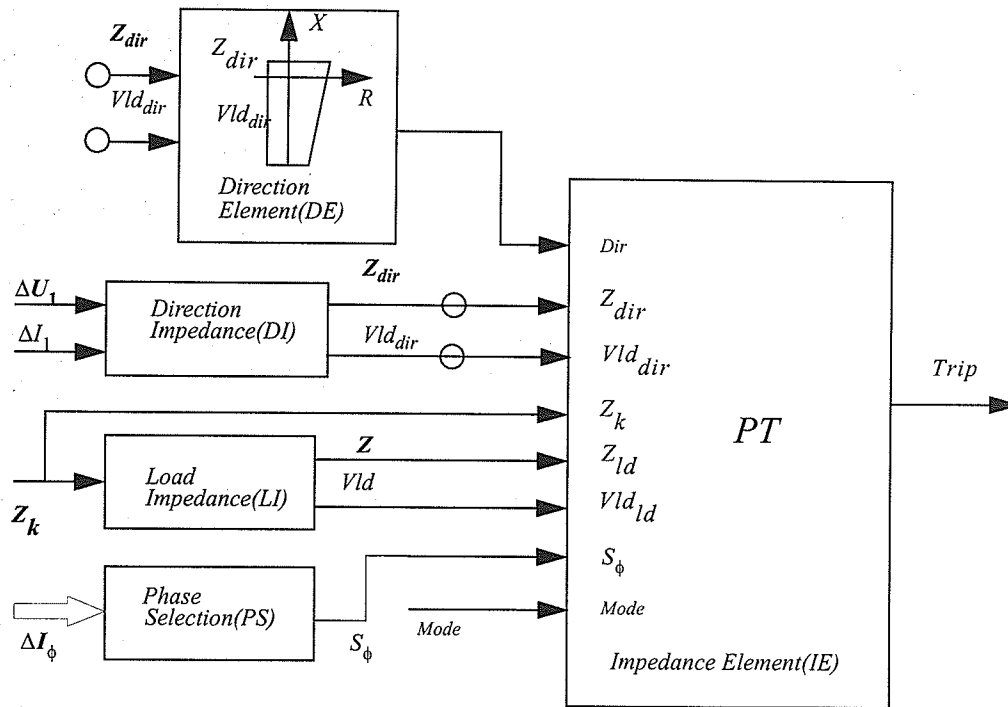


Figure 3.2. The Structure Diagram of the PT Relay.

The structure of one phase of the PT relay is illustrated in figure 3.2. It is composed of five parts: the direction impedance element DI, the direction element DE, the load impedance element LI, the phase selection element PS, and the impedance element IE. Their functions will be discussed in the following sections. The mode can take a value 1 or 2, the significance of which will be explained in section 3.6.1.2.

3.2. The direction impedance (DI) element

The DI element measures the system positive sequence impedance during the fault. The DI element has two phasor input signals: the incremental positive sequence voltage ΔU_1 and the incremental positive sequence current ΔI_1 . The incremental positive sequence voltage ΔU_1 and current ΔI_1 are the difference between the positive sequence voltage and current of present cycle and that of several cycles ago. It has two output signals: the first is Z_{dir} , and the second is the logic output vld_{dir} . If vld_{dir} is high, Z_{dir} is valid.

Figure 3.3 is the positive sequence network of the system in figure 2.4.

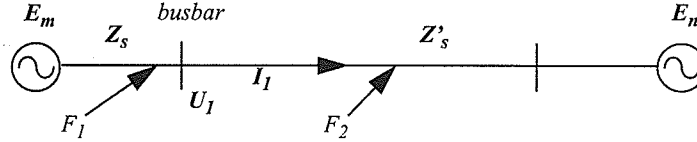


Figure 3.3. The Positive Sequence Network.

Before the fault, equation 3.1 and equation 3.2 are true.

$$U_1 = E_m - I_1 Z_s \quad 3.1$$

$$U_1 = E_n + I_1 Z'_s \quad 3.2$$

When a fault occurs on the system, the incremental positive sequence current ΔI_1 is detected by the DI element. If $|\Delta I_1|$ is large enough, the vld_{dir} is set to logic high and $Z_{dir} = \Delta U_1 / \Delta I_1$ is calculated. Otherwise the vld_{dir} is set to logic low.

For a forward fault, equation 3.1 is true, and $\Delta U_1 / \Delta I_1 = -Z_s$.

For a reverse fault, equation 3.2 is true, and $\Delta U_1 / \Delta I_1 = Z'_s$.

The flowchart for the DI element is in figure 3.4.

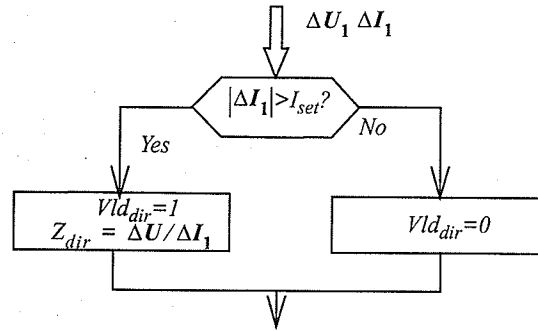


Figure 3.4. The Flowchart of the DI Element.

3.3. The direction element (DE)

The DE element is designed to determine the direction of a fault. The DE element has two inputs which are the complex input z_{dir} , and the logic input vld_{dir} . If vld_{dir} is high, z_{dir} is valid. The DE element has one logic output Dir , its logic high indicates a forward fault. The DE element sets Dir to a logic high only when the logic input vld_{dir} is high and z_{dir} falls within its setting zone. Figure 3.5 is the flowchart of the DE element.

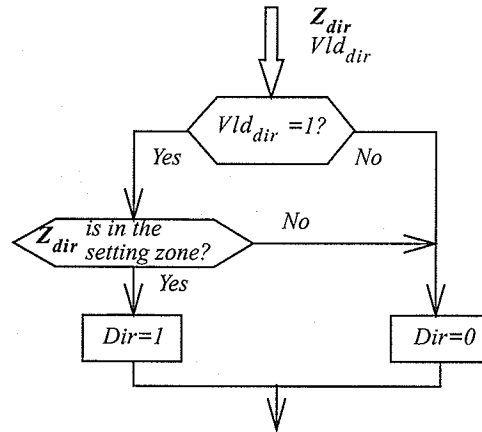


Figure 3.5. The Flowchart of the DE Element.

3.4. The load impedance (LI) element

The LI element provides the prefault load impedance. The LI element has one complex input z_k .

It has two outputs: the complex output Z_{ld} , and the other logic output Vld_{ld} . A high level of Vld_{ld} indicates that Z_{ld} is valid. Vld_{ld} is set to high when the input Z_k keeps constant for a time period. The high level Vld_{ld} lasts for a short time period when the disturbance is detected in the input Z_k . A fixed-length queue is used to buffer the input Z_k . When the LI element accesses the queue, it fetches the value at the head of the queue and set to output Z_{ld} . The head of the queue is then removed and every element in the queue is moved one slot ahead. The input Z_k is inserted at the tail. If the difference of Z_k and Z_{ld} is detected to be smaller than a preset value, the internal logic signal $flag$ is set to high. It takes time, t_1 , for the input Z_k to move to the head of the queue. The high level $flag$ sets Vld_{ld} immediately and the low level $flag$ sets Vld_{ld} after an time delay, t_2 , which is less than t_1 . In the fault, this mechanism will provide the PT relay with the valid load impedance within the period of t_2 after the fault. The right part of figure 3.6 shows the signal time sequence of this element in the fault.

Before the fault, the $flag$ is high. After the fault, the Z_{ld} is valid within t_2 period and Vld_{ld} is high within t_1 period, thus this feature ensures that the LI element can produce the valid Z_{ld} when Vld_{ld} is high. The left part of figure 3.6 is a flowchart of the LI element.

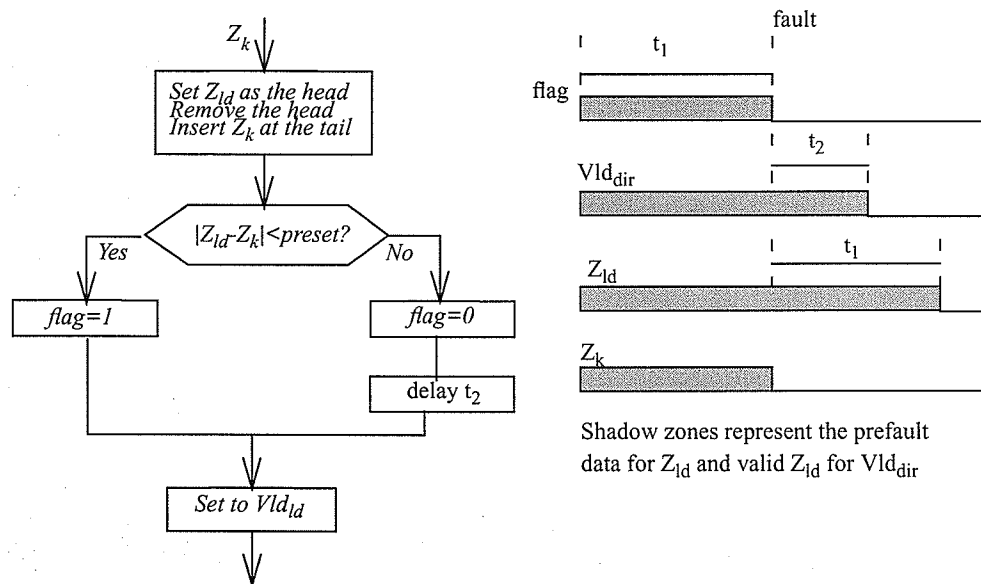


Figure 3.6. The Flowchart of the LI Element.

3.5. The phase selection (PS) element

The PS element selects the phases where the measured impedance represents the impedance in the fault loop. The PS element has three phasor inputs, the three phase incremental currents, ΔI_a , ΔI_b and ΔI_c which represent the differences between prefault and fault current. It has a group of logic outputs S_ϕ which is used to control the adaptive feature of the IE element.

Table 3.1. The Expected Behaviour of the PS Element in Fault

Fault/ S_ϕ	S_a	S_b	S_c	S_{ab}	S_{bc}	S_{ca}
AG	Y	N	N	N	N	N
BC	N	N	N	N	Y	N
BCG	N	Y	Y	N	Y	N
ABC	Y	Y	Y	Y	Y	Y

In table 3.1, the first column is the fault type, and the first row is phase. The columns intersect the rows at cells which contain the value 'Y' or 'N'. Value 'Y' indicates that the phase identified by the column is selected in the fault identified by the row. Value 'N' indicates the phase is not selected in that particular fault.

3.5.1. The principle of the PS element

The discussion will focus on the relationship between the incremental phase-phase currents in such fault types as AG, BC, BCG, and ABC. The 120 sequence current and voltage can be computed by connecting the 120 sequence network in the topology determined by the fault type.

3.5.2. The ratio of the phase-phase current

The incremental phase-phase current of the network to the left hand side of the fault is expressed in the form of the incremental positive sequence current and the negative sequence current of

phase A, as in equation 3.3.

$$\begin{aligned}
\Delta I_{mab} &= (1-a^2) \Delta I_{ma1} + (1-a) I_{ma2} \\
\Delta I_{mbc} &= (a^2-a) \Delta I_{ma1} + (a-a^2) I_{ma2} \\
\Delta I_{mca} &= (a-1) \Delta I_{ma1} + (a^2-1) I_{ma2}
\end{aligned} \tag{3.3}$$

If we assume that $I_{ma2} = \lambda \Delta I_{ma1}$, then we obtain the amplitude of the phase-phase incremental currents $|\Delta I_{mab}| = |\Delta I_{mca}| = \sqrt{3(1+\lambda+\lambda^2)} |\Delta I_{ma1}|$, $|\Delta I_{mbc}| = (1-\lambda) \sqrt{3} |\Delta I_{ma1}|$. The value λ for all fault types is displayed in table 3.2 (See appendix B).

Table 3.2 Value of λ in fault

Fault	AG	BC	BCG	ABC
λ	1	-1	(-1,0)	0

Two ratios $\phi_{bc1} = \frac{|\Delta I_{mab}|}{|\Delta I_{mbc}|}$, $\phi_{bc2} = \frac{|\Delta I_{mca}|}{|\Delta I_{mbc}|}$ are calculated against the fault type. We obtain

$\phi_{bc1} = \phi_{bc2} = \frac{\sqrt{(1+\lambda+\lambda^2)}}{(1-\lambda)}$. $\phi_{bc1} = \phi_{bc2} = \infty$ in an AG fault, $\phi_{bc1} = \phi_{bc2} = 1$ in an ABC fault,

$\phi_{bc1} = \phi_{bc2} = \frac{\sqrt{(1+\lambda+\lambda^2)}}{(1-\lambda)}$, $-1 < \lambda < 0$ in a BCG fault and the values of ϕ_{bc1}, ϕ_{bc2} reside in the range (0.5,1). $\phi_{bc1} = \phi_{bc2} = 0.5$ in a BC fault.

A similar analysis can be conducted for phase B and C to give $\phi_{ca1}, \phi_{ca2}, \phi_{ab1}, \phi_{ab2}$.

In the table 3.3, $\phi_{ab1}, \phi_{ab2}, \phi_{bc1}, \phi_{bc2}, \phi_{ca1}, \phi_{ca2}$, and $|I_0|$ are tabulated.

Table 3.3 The Ratio of the Incremental Phase-Phase Current

Fault	I_0	Φ_{ab1}	Φ_{ab2}	Φ_{bc1}	Φ_{bc2}	Φ_{ca1}	Φ_{ca2}
AG	>0	1	0	∞	∞	0	1
BG	>0	0	1	1	0	∞	∞
CG	>0	∞	∞	0	1	1	0
AB	0	0.5	0.5	2	1	1	2
BC	0	1	2	0.5	0.5	2	1
CA	0	2	1	1	2	0.5	0.5
ABG	>0	(0.5,1)	(0.5,1)	(1,2)	1	1	(1,2)
BCG	>0	1	(1,2)	(0.5,1)	(0.5,1)	(1,2)	1
CAG	>0	(1,2)	1	1	(1,2)	(0.5,1)	(0.5,1)
ABC	0	1	1	1	1	1	1

3.5.3. The algorithm & flowchart of the PS element

The PS algorithm is based on the ratios in table 3.3. The flow chart is shown in the figure 3.7.

At the beginning, the phase selection flags: S_A , S_B , S_C , S_{AB} , S_{BC} , and S_{CA} are reset. If the maximum of the three phase-phase incremental current amplitude is over a predetermined threshold, go to step 1. Otherwise go to step 6.

Step 1: If any pair of $\phi_{bc1} > 10$, $\phi_{bc2} > 10$, $\phi_{ca1} > 10$, $\phi_{ca2} > 10$, or $\phi_{ab1} > 10$, $\phi_{ab2} > 10$ is true, the corresponding phase selection flag S_A , S_B , or S_C is set to the high level, and the algorithm goes to step 6.

Step 2: I_0 is calculated. If the amplitude of the zero sequence current is larger than a predetermined threshold, go to step 5.

Step 3: If any pair of $\phi_{bc1} < 0.75$, $\phi_{bc2} < 0.75$, $\phi_{ca1} < 0.75$, $\phi_{ca2} < 0.75$, or $\phi_{ab1} < 0.75$, $\phi_{ab2} < 0.75$ is true, the corresponding phase selection flag S_{BC} , S_{CA} , or S_{AB} is set to the high level, and the algorithm goes to step 6.

Step 4: Set S_A , S_B , S_C , S_{AB} , S_{BC} , and S_{CA} , go to step 6.

Step 5: Find the phase with the maximum amplitude of the incremental phase-phase current, and set its associated selection flag.

Step 6: Quit the selection procedure.

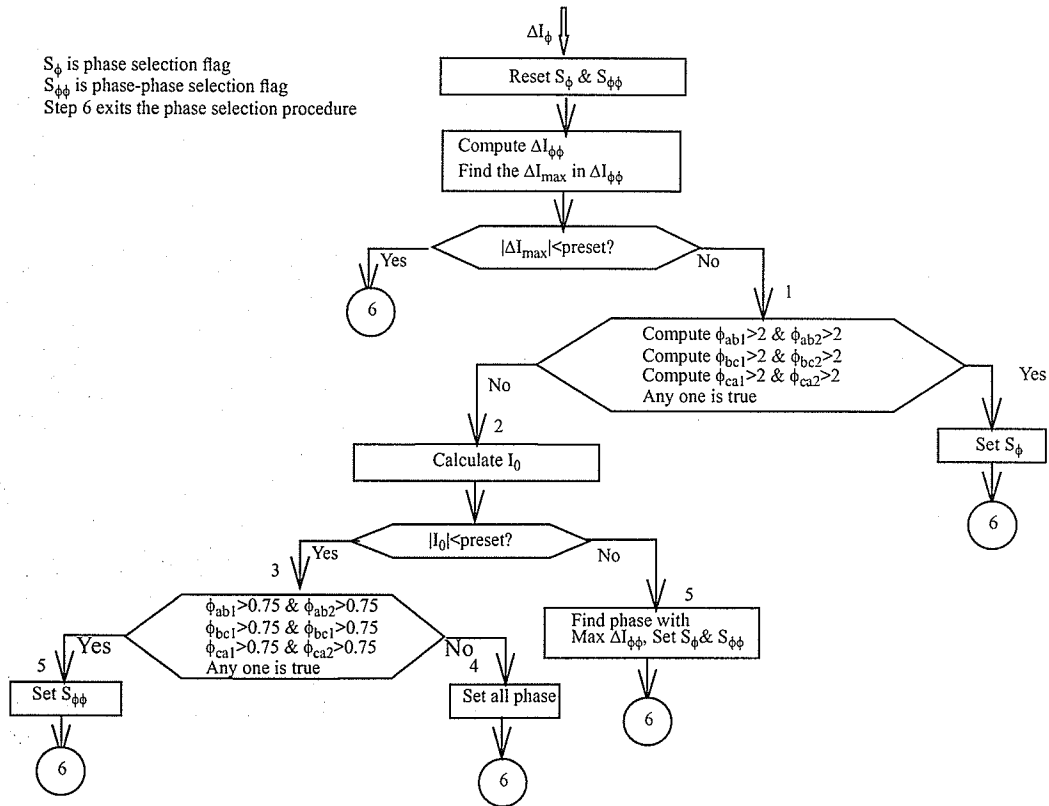


Figure 3.7. The Algorithm Flowchart of the PS Element.

3.6. The impedance element(IE)

The purpose of the IE element is to trip the circuit breaker in the event of a fault. The impedance element has eight inputs, of which four are logic signals, Dir , Vld_{dir} , Vld_{ld} , S_ϕ , three are complex inputs, Z_{dir} , Z_k , Z_{ld} , and one integer input, $Mode$. It has only one output signal, $Trip$, a high level trips the circuit breaker. $Mode$ is used to disable or enable the vertical modification of the protection zone.

3.6.1. The algorithms of the IE element

This element is able to operate adaptively in the system configuration by conditioning its quadrilateral protection zone with its own embedded logic. Its adaptive features are exhibited by modifying the trip zone in both horizontal and vertical direction during a fault.

3.6.1.1. The horizontal expansion of the trip zone

The horizontal modification is controlled by its logic input combination Hor which is derived from Equation 3.4.

$$Hor = Vld_{ld} + Dir + S_{\Phi} \quad 3.4$$

When Hor is logic high, the algorithm will expand the protection zone along the R axis.

The algorithm first finds intersection point P of the protection zone boundary on the R axis on the Z_{ld} side. If Z_{ld} is in the left hand side of the impedance plane, the intersection point is $P2$, otherwise it is $P1$. R_i is calculated by using the formula $R_i = \eta \cdot (R_{ld} - R_p)$, where η is a number between 0 and 1.

The value R_i is then compared with a preset value. Since the expanded trip zone of the relay should not encompass the minimum load impedance, R_i equals the lesser of R_i and the preset value.

The PT relay expands its protection zone in both directions along the R axis. The expansion is illustrated in figure 3.8. The expansion of the protection zone should keep the PT relay from misoperating during a load transition.

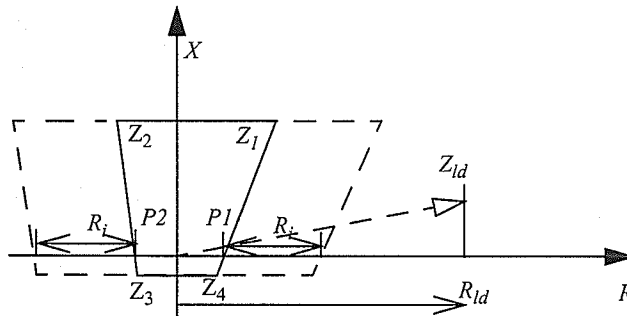


Figure 3.8. The Horizontal Expansion of the Trip Zone.

3.6.1.2. The vertical feature of the trip zone

The value of $Mode$ can be either 1 or 2 depending whether the vertical modification of the trip zone is wanted. The vertical modification is designed for all phases during the reverse fault, but only for the faulted phase in the forward fault when $Mode = 1$, thus the IE element can expand its trip zone in the faulted phase in the forward fault and flip up its trip zone in the reverse fault.

The vertical feature of the IE element is under the control of the input combination Ver which is calculated by equation 3.5.

$$Ver = (Vld_{dir} \cdot (Mode = 1)) \cdot ((S_{\Phi}) + (Dir = 0)) \quad 3.5$$

The PT relay modifies two setting points Z_3, Z_4 by adding the inductance part of Z_{dir} to them when Ver is true. When Z_k falls within the modified protection zone, an internal logic signal Tin is set to logic high. The output $Trip = Tin \cdot Dir$.

Figure 3.9 illustrates how the protection zone is modified in a forward fault (figure 3.9a) and in a reverse fault (figure 3.9b).

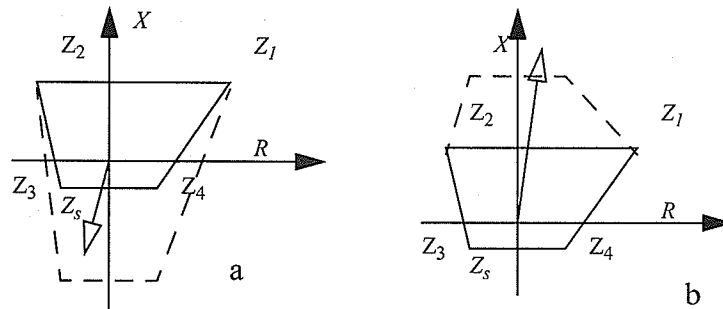
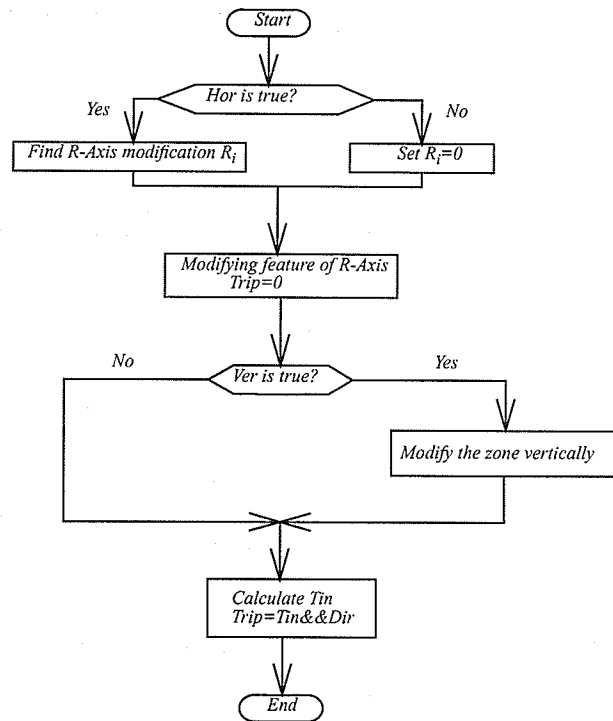


Figure 3.9. The Vertical Modification of the Protection Zone.

3.6.2. The algorithm flowchart of the IE element

The flowchart of the IE element is depicted by figure 3.10.



Hor is calculated in equation 3.4

Ver is calculated in equation 3.5

Figure 3.10. The Flowchart of the IE Element.

In figure 3.11, the zone enclosed by the dashed line is the setting zone, while the zone enclosed by solid line is the practical trip zone after the modification. In figure 3.11a, the IE element operates in mode 1 during a forward fault, with the trip zone of the faulted phase expanding in both directions. In figure 3.11b, the IE element operates in mode 1 during a reverse fault, and the trip zone is modified only in the vertical direction. In figure 3.11c, the IE element operates in mode 2 in a forward fault, and the trip zone of the faulted phase is modified only in the horizontal direction. In figure 3.11d, the IE element has a trip zone which is identical with the setting zone when it runs in mode 2. During a forward fault, the IE elements of unfaulted phases have such trip zones. During reverse fault, the IE element also has such a trip zone.

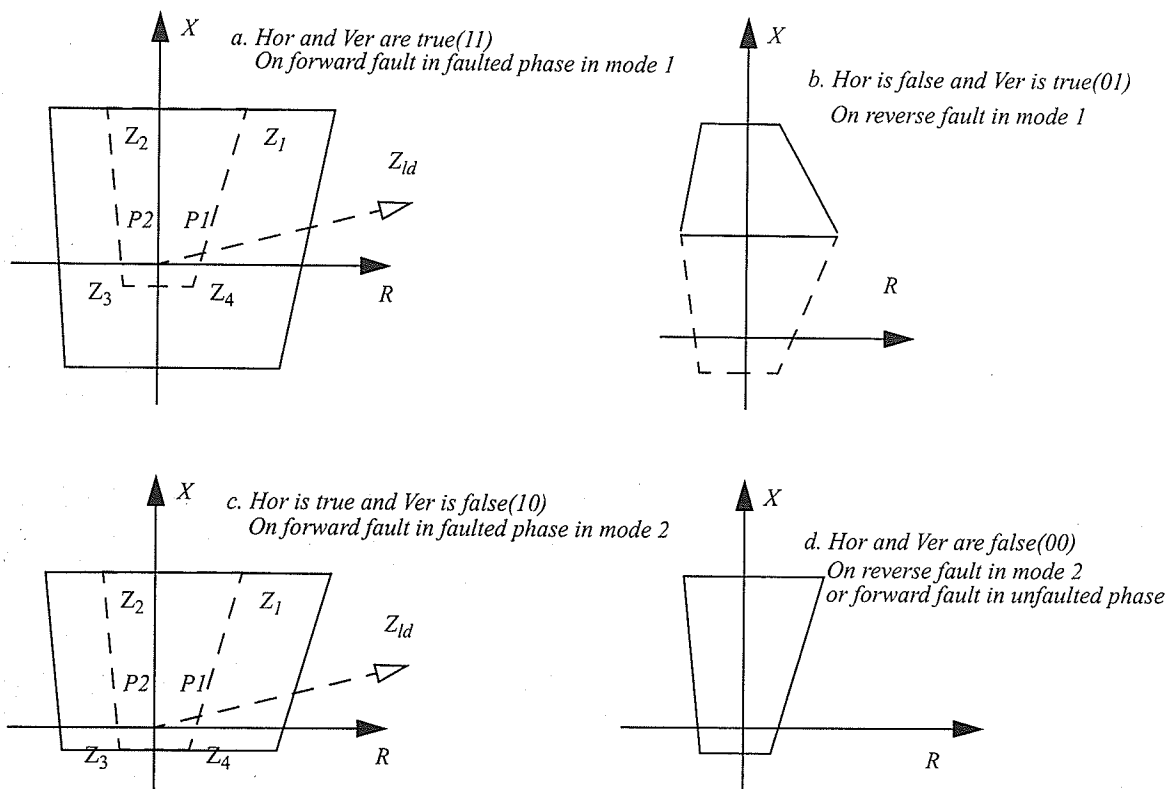


Figure 3.11. The Trip Zone of the IE Element in the fault.

Chapter 4. The Selection of the Directional Impedance

The DI element is used to control and activate the adaptive protection zone in the PT relay model. The quadrilateral distance relay, in most cases, can identify a fault within its protection zone within one or two cycles, hence the DI element must be able to provide a fast enough fault response to activate the adaptive feature of the PT relay. Besides its response speed, the selected DI element is expected to have two other important attributes: *availability* and *convergence*. *Availability* means that the DI element is able to be measured during any faults. *Convergence* means that the measurement of the DI element converges to a distinct impedance associated with fault direction when it is available.

The DI element activates the adaptive feature of the PT relay by providing the relay with the expanding quantity and helping other elements to produce the zone control signal. The impedances calculated by $\Delta U/\Delta I$ can provide fast responses in a fault. Since the impedance is calculated by dividing the incremental voltage by the incremental current, we call it incremental impedance. The positive sequence incremental impedance(PSII) calculated by $\Delta U_1/\Delta I_1$ is adopted in the PT relay model. It is selected from nine incremental impedances that include three sequence incremental impedances calculated by $\Delta Z_s = \Delta U_s/\Delta I_s, s \in \{1, 2, 0\}$, three phase incremental impedances calculated by $\Delta Z_\phi = \Delta U_\phi/\Delta I_\phi, \phi \in \{a, b, c\}$, and three phase-phase incremental impedances calculated by $\Delta Z_{\phi\phi} = \Delta U_{\phi\phi}/\Delta I_{\phi\phi}, \phi\phi \in \{ab, bc, ca\}$.

This chapter begins with a comprehensive analysis of the measurement of nine possible incremental impedances, followed by inspecting the *convergence* and *availability* of these nine incremental impedances. Then, the measurement of PSII is observed in the presence of a salient-pole synchronous generator, and the measurement of PSII in different fault directions is presented. Finally, a summary will confirm the eligibility of PSII to serve as the directional impedance of the PT relay.

The powerful power system simulation software PSCAD/EMTDC software package is used in the investigation of these methods. The PSCAD is the graphical front end of the package. The PSCAD provides a GUI environment where the user can create the power system device module and associate an icon with it. As well, the user can incorporate the icon which represents the specific system device into a complex system draft. The user can then compile the system draft into

the simulation source code. EMTDC uses the source code to build the executable code and proceed with simulations. The PSCAD/EMTDC software simplifies the power system simulation procedure in several ways: firstly, it provides a visual way to create simulations; secondly, the module created for one case is reusable in later simulations; thirdly, it allows a complex simulation case to be built up gradually.

4.1. The phase incremental current and voltage

Figure 4.1 is a simple system with two sources connected by a protected transmission line. The measurement of directional impedance is illustrated by this system. The relay acquires the busbar voltage and current flowing down the line with the reference direction from source E_m to source E_n . These sources are ideal voltage sources which have constant internal voltage and constant internal impedance.

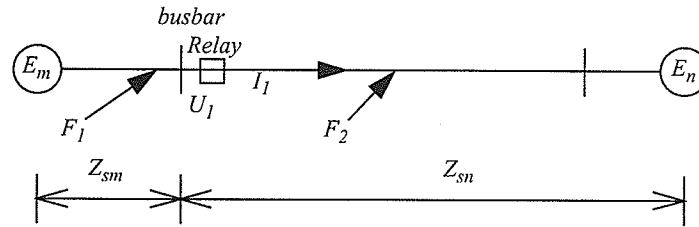


Figure 4.1. The Power System for Analysis Purpose.

Figure 4.2 is the sequence network for phase A incremental currents during a forward fault. Various fault types in the system can be represented by proper connection of this network. The sequence networks are separated into two parts by fault point F2. The relay busbar is located on the left hand(M) side of the system, with the equivalent impedance and incremental currents flowing on the two sides of the sequence network. This is shown in figure 4.2. The impedances $Z_{sm1}, Z_{sm2}, Z_{sm0}$, represent the total sequence impedance from the relay busbar to the source E_m , the impedances Z_{m1}, Z_{m2}, Z_{m0} , represent the sequence impedance from the fault point to the relay busbar, and the impedances Z_{n1}, Z_{n2}, Z_{n0} , represent the sequence impedance from the fault point to the source E_n . In this case, the incremental sequence currents sensed by the relay are $\Delta I_{ma1}, I_{ma2}$

and I_{ma0} .

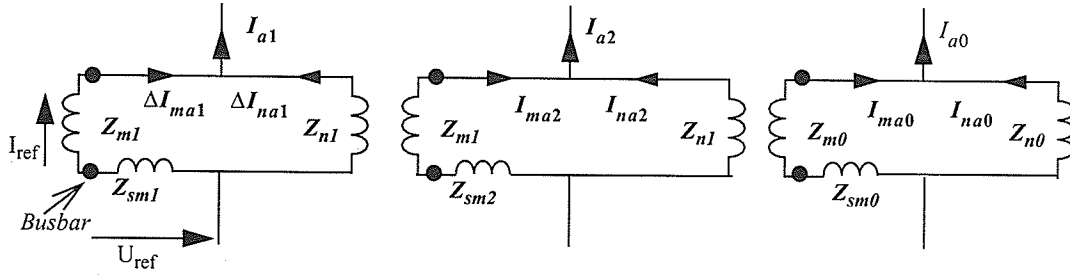


Figure 4.2. The Incremental Current and Voltage in Sequence Network in the F2 Fault.

Figure 4.3 is the sequence network for phase A incremental currents in a reverse fault. The sequence networks are separated into two parts by fault point F1, with the busbar located on the right hand side of the system, as in figure. 4.4. The impedances Z_{sn1} , Z_{sn2} , Z_{sn0} , represent the total sequence impedance from the relay busbar to the source En, the impedances Z_{n1} , Z_{n2} , Z_{n0} , represent the sequence impedance from the fault point to the relay busbar, and the impedances Z_{m1} , Z_{m2} , Z_{m0} , represent the sequence impedance from the fault point to the source Em. In this case, the incremental sequence currents sensed by the relay are $-\Delta I_{na1}$, $-I_{na2}$ and $-I_{na0}$.

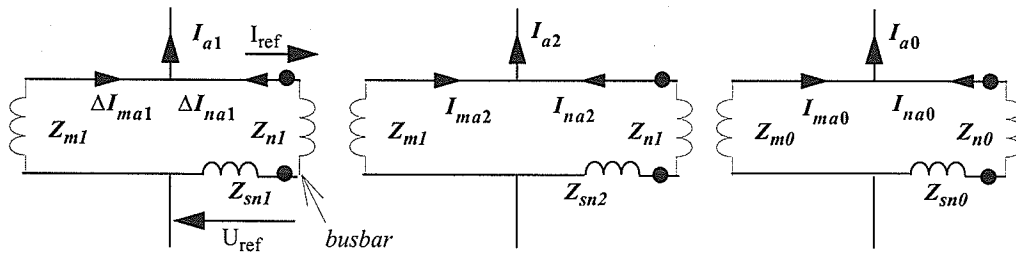


Figure 4.3. The Incremental Current & Voltage in Sequence Network in the F1 Fault.

4.1.1. The forward fault

In a forward fault, the relay busbar is located in the left hand side of the system as in figure. 4.2, the sequence incremental currents are ΔI_{ma1} , I_{ma2} , I_{ma0} and the phase incremental currents measured by the relay are in equation 4.1.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} \Delta I_{ma1} \\ I_{ma2} \\ I_{ma0} \end{bmatrix}, a = e^{j\frac{2\pi}{3}} \quad 4.1$$

In addition, the incremental voltages on the relay busbar, as measured by the relay are in equation 4.2.

$$\begin{bmatrix} \Delta U_{ma} \\ \Delta U_{mb} \\ \Delta U_{mc} \end{bmatrix} = - \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} Z_{sm1} & 0 & 0 \\ 0 & Z_{sm2} & 0 \\ 0 & 0 & Z_{sm0} \end{bmatrix} \begin{bmatrix} \Delta I_{ma1} \\ I_{ma2} \\ I_{ma0} \end{bmatrix} = - \begin{bmatrix} Z_{sm1} & Z_{sm2} & Z_{sm0} \\ a^2 Z_{sm1} & a Z_{sm2} & Z_{sm0} \\ a Z_{sm1} & a^2 Z_{sm2} & Z_{sm0} \end{bmatrix} \begin{bmatrix} \Delta I_{ma1} \\ I_{ma2} \\ I_{ma0} \end{bmatrix} \quad 4.2$$

4.1.2. The reverse fault

In a reverse fault, the relay busbar is located in the right hand side of the diagram as in figure 4.3, the sequence incremental currents are $-\Delta I_{na1}, -I_{na2}, -I_{na0}$ since the current reference direction is from Em to En. The phase incremental currents measured by the relay are in equation 4.4.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} -\Delta I_{na1} \\ -I_{na2} \\ -I_{na0} \end{bmatrix} = - \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} \Delta I_{na1} \\ I_{na2} \\ I_{na0} \end{bmatrix} \quad 4.3$$

equation 4.4 describes the incremental voltages on the relay busbar as measured by the relay.

$$\begin{bmatrix} \Delta U_{ma} \\ \Delta U_{mb} \\ \Delta U_{mc} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} Z_{sn1} & 0 & 0 \\ 0 & Z_{sn2} & 0 \\ 0 & 0 & Z_{sn0} \end{bmatrix} \begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = - \begin{bmatrix} Z_{sn1} & Z_{sn2} & Z_{sn0} \\ a^2 Z_{sn1} & a Z_{sn2} & Z_{sn0} \\ a Z_{sn1} & a^2 Z_{sn2} & Z_{sn0} \end{bmatrix} \begin{bmatrix} \Delta I_{na1} \\ I_{na2} \\ I_{na0} \end{bmatrix} \quad 4.4$$

4.1.3. The availability of incremental current

The incremental impedance is measured by dividing the incremental voltage by the incremental current. When the incremental current is zero, the measured impedance is meaningless. The *availability* of the directional impedance is determined by the *availability* of the incremental current. Our discussion of the incremental currents focuses on the forward AG, BC, BCG, and ABC faults.

By borrowing the analysis from section 2.4.4, the following are true:

in an AG fault, $\Delta I_{ma1} = I_{ma2}$ and I_{ma0} is not zero;

in a BC fault, $\Delta I_{ma1} = -I_{ma2}$ and $I_{ma0} = 0$;

in a BCG fault, $I_{ma2} = \lambda \Delta I_{ma1}$, $-1 < \lambda < 0$ and I_{ma0} is not zero;

in an ABC fault, ΔI_{ma1} is not zero, but I_{ma2} and I_{ma0} are zero.

Here, we define $\sigma = \Delta I_{ma1}/I_{ma0}$, so $I_{ma0} = \sigma \Delta I_{ma1}$.

With these results, we derive the incremental phase currents and incremental phase-phase currents for the four cases using equation 4.1.

For the AG fault, equation 4.5 is the analytical result. ΔI_{mb} and ΔI_{mc} depend on λ and σ . Since the current distribution factor of the negative sequence network equals the current distribution factor of the positive sequence network, $\lambda = 1$ and equation 4.5 is true.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} (2 + \sigma) \Delta I_{ma1} \\ (\sigma - 1) \Delta I_{ma1} \\ (\sigma - 1) \Delta I_{ma1} \end{bmatrix}, \begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} 3 \Delta I_{ma1} \\ 0 \\ -3 \Delta I_{ma1} \end{bmatrix}, \lambda > 0 \quad 4.5$$

For the BC fault, equation 4.6 is the analytical result.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} 0 \\ (a^2 - a) \Delta I_{ma1} \\ (a - a^2) \Delta I_{ma1} \end{bmatrix}, \begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} (a - a^2) \Delta I_{ma1} \\ 2(a^2 - a) \Delta I_{ma1} \\ (a - a^2) \Delta I_{ma1} \end{bmatrix} \quad 4.6$$

For the BCG fault, equation 4.7 is the analytical result.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} (1 + \lambda + \sigma) \Delta I_{ma1} \\ (a^2 + a\lambda + \sigma) \Delta I_{ma1} \\ (a + a^2\lambda + \sigma) \Delta I_{ma1} \end{bmatrix}, \begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} (1 - a^2 + \lambda - a\lambda) \Delta I_{ma1} \\ (a^2 - a)(1 - \lambda) \Delta I_{ma1} \\ (a - 1 + a^2\lambda - \lambda) \Delta I_{ma1} \end{bmatrix}, -1 < \lambda < 0 \quad 4.7$$

For the ABC fault, the analytical result is in equation 4.8.

$$\begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} \Delta I_{ma1} \\ a^2 \Delta I_{ma1} \\ a \Delta I_{ma1} \end{bmatrix}, \begin{bmatrix} \Delta I_{ma} \\ \Delta I_{mb} \\ \Delta I_{mc} \end{bmatrix} = \begin{bmatrix} (1 - a^2) \Delta I_{ma1} \\ (a^2 - a) \Delta I_{ma1} \\ (a - 1) \Delta I_{ma1} \end{bmatrix} \quad 4.8$$

Table 4.1 tabulates the amplitudes of the incremental currents of the four cases.

Table 4.1 The Amplitude of the Incremental Currents

Fault	ΔI_1	I_2	I_0	ΔI_a	ΔI_b	ΔI_c	ΔI_{ab}	ΔI_{bc}	ΔI_{ca}
AG	>0	>0	>0	>0	?	?	>0	0	>0
BC	>0	>0	0	0	>0	>0	>0	>0	>0
BCG	>0	>0	>0	?	>0	>0	>0	>0	>0
ABC	>0	0	0	>0	>0	>0	>0	>0	>0

The cells contain the amplitudes of the incremental currents, identified by the column, during the faults, identified by the row. The mark ‘?’ means that the amplitude of the incremental current may be or may not be zero. The mark ‘0’ means that the amplitude of the incremental current is zero. The mark “>0” means that the amplitude of the incremental current is not zero. When the amplitude of an incremental current is zero during a fault, its associated incremental impedance can not be calculated.

4.2. The measurement of the sequence incremental impedance

When the sequence incremental current is not zero, the sequence directional impedance is measured by equation $\Delta Z_s = \Delta U_s / \Delta I_s, s \in \{1, 2, 0\}$.

4.2.1. The measurement in the forward fault

The incremental sequence currents sensed by the relay are $\Delta I_{ma1}, I_{ma2}, I_{ma0}$, and the measured impedances are shown in equation 4.9.

$$\begin{bmatrix} \Delta Z_1 \\ \Delta Z_2 \\ \Delta Z_0 \end{bmatrix} = \begin{bmatrix} \Delta U_{ma1} / \Delta I_{ma1} \\ \Delta U_{ma2} / I_{ma2} \\ \Delta U_{ma0} / I_{ma0} \end{bmatrix} = - \begin{bmatrix} Z_{sm1} \\ Z_{sm2} \\ Z_{sm0} \end{bmatrix} \quad 4.9$$

4.2.2. The measurement in the reverse fault

The incremental sequence currents sensed by the relay are $-\Delta I_{na1}, -I_{na2}, -I_{na0}$, and the measured impedances are shown in equation 4.10.

$$\begin{bmatrix} \Delta Z_1 \\ \Delta Z_2 \\ \Delta Z_0 \end{bmatrix} = \begin{bmatrix} \Delta U_{ma1} / (-\Delta I_{na1}) \\ \Delta U_{ma2} / (-I_{na2}) \\ \Delta U_{ma0} / (-I_{na0}) \end{bmatrix} = \begin{bmatrix} Z_{sn1} \\ Z_{sn2} \\ Z_{sn0} \end{bmatrix} \quad 4.10$$

4.3. The measurement of the phase incremental impedance

The phase incremental impedances are measured by equation $\Delta Z_\phi = \Delta U_\phi / \Delta I_\phi$, $\phi \in \{a, b, c\}$ when the phase incremental currents are not zero.

4.3.1. The measurement in the forward fault

The incremental phase currents sensed by the relay are $\Delta I_a, \Delta I_b, \Delta I_c$, and the measured impedances are given in equation 4.11.

$$\begin{bmatrix} \Delta Z_a \\ \Delta Z_b \\ \Delta Z_c \end{bmatrix} = \begin{bmatrix} \frac{\Delta U_{ma}}{\Delta I_{ma}} \\ \frac{\Delta U_{mb}}{\Delta I_{mb}} \\ \frac{\Delta U_{mc}}{\Delta I_{mc}} \end{bmatrix} = \begin{bmatrix} \frac{-(Z_{sm1}\Delta I_{ma1} + Z_{sm2}I_{ma2} + Z_{sm0}I_{ma0})}{\Delta I_{ma1} + I_{ma2} + I_{ma0}} \\ \frac{-(a^2 Z_{sm1}\Delta I_{ma1} + aZ_{sm2}I_{ma2} + Z_{sm0}I_{ma0})}{a^2 \Delta I_{ma1} + aI_{ma2} + I_{ma0}} \\ \frac{-(aZ_{sm1}\Delta I_{ma1} + a^2 Z_{sm2}I_{ma2} + Z_{sm0}I_{ma0})}{a\Delta I_{ma1} + a^2 I_{ma2} + I_{ma0}} \end{bmatrix} \quad 4.11$$

4.3.2. The measurement in the reverse fault

The incremental phase currents sensed by the relay are $-\Delta I_{na}, -\Delta I_{nb}, -\Delta I_{nc}$, and the measured impedances are given in equation 4.12.

$$\begin{bmatrix} \Delta Z_a \\ \Delta Z_b \\ \Delta Z_c \end{bmatrix} = \begin{bmatrix} \frac{\Delta U_{ma}}{-\Delta I_{na}} \\ \frac{\Delta U_{mb}}{-\Delta I_{nb}} \\ \frac{\Delta U_{mc}}{-\Delta I_{nc}} \end{bmatrix} = \begin{bmatrix} \frac{Z_{sn1}\Delta I_{na1} + Z_{sn2}I_{na2} + Z_{sn0}I_{na0}}{\Delta I_{na1} + I_{na2} + I_{na0}} \\ \frac{a^2 Z_{sn1}\Delta I_{na1} + aZ_{sn2}I_{na2} + Z_{sn0}I_{na0}}{a^2\Delta I_{na1} + aI_{na2} + I_{na0}} \\ \frac{aZ_{sn1}\Delta I_{na1} + a^2 Z_{sn2}I_{na2} + Z_{sn0}I_{na0}}{a\Delta I_{na1} + a^2 I_{na2} + I_{na0}} \end{bmatrix} \quad 4.12$$

4.4. The measurement of the phase-phase incremental impedance

When the phase-phase incremental currents are not zero, the phase-phase incremental impedances are measured with equation $\Delta Z_{\phi\phi} = \Delta U_{\phi\phi} / \Delta I_{\phi\phi}$, $\phi\phi \in \{ab, bc, ca\}$.

4.4.1. The measurement in the forward fault

The incremental phase-phase currents sensed by the relay are ΔI_{mab} , ΔI_{mbc} , ΔI_{mca} , and the measured impedances are given in equation 4.13 with the assumption that $Z_{sm1} = Z_{sm2}$,

$$\begin{bmatrix} \Delta Z_{ab} \\ \Delta Z_{bc} \\ \Delta Z_{ca} \end{bmatrix} = - \begin{bmatrix} Z_{sm1} \\ Z_{sm1} \\ Z_{sm1} \end{bmatrix} \quad 4.13$$

4.4.2. The measurement in the reverse fault

The incremental phase-phase currents sensed by the relay are $-\Delta I_{nab}$, $-\Delta I_{nbc}$, $-\Delta I_{nca}$, and the measured impedances are in equation 4.14 with the assumption that $Z_{sn1} = Z_{sn2}$.

$$\begin{bmatrix} \Delta Z_{ab} \\ \Delta Z_{bc} \\ \Delta Z_{ca} \end{bmatrix} = \begin{bmatrix} Z_{sn1} \\ Z_{sn1} \\ Z_{sn1} \end{bmatrix} \quad 4.14$$

4.5. The availability and convergence of the incremental impedance

In this section, the power system simulation used to test the *availability* and *convergence* of the incremental impedances is shown in figure 4.4. Four faults AG, BC, BCG, and ABC, are applied at point F2. The figures showing the measured incremental impedances are provided to demonstrate the method's convergence for these faults.

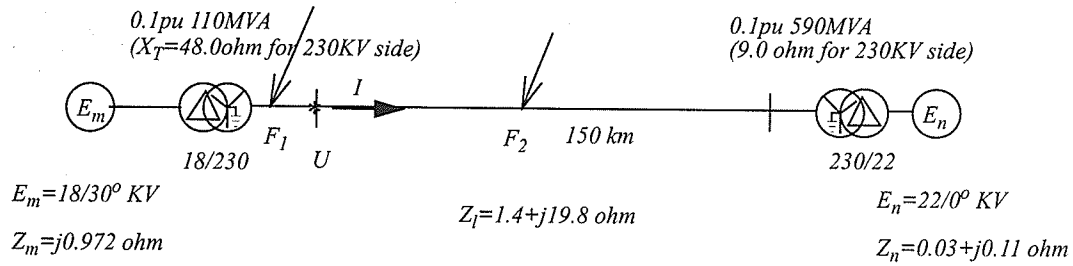


Figure 4.4. The Power System for Analysing Incremental Impedance.

4.5.1. The sequence incremental impedance

4.5.1.1. The positive sequence incremental impedance

Figure 4.5 shows the PSII in AG, BC, BCG, and ABC faults at point F2. These faults are applied to the system at 0.75 second. The simulation results from 0.76 second to 0.8 second are collected to observe the PSII. The upper part of the figure is the resistive part of ΔZ_1 , and lower part is the inductive part of ΔZ_1 . The measured ΔZ_1 converges to the same value in four cases.

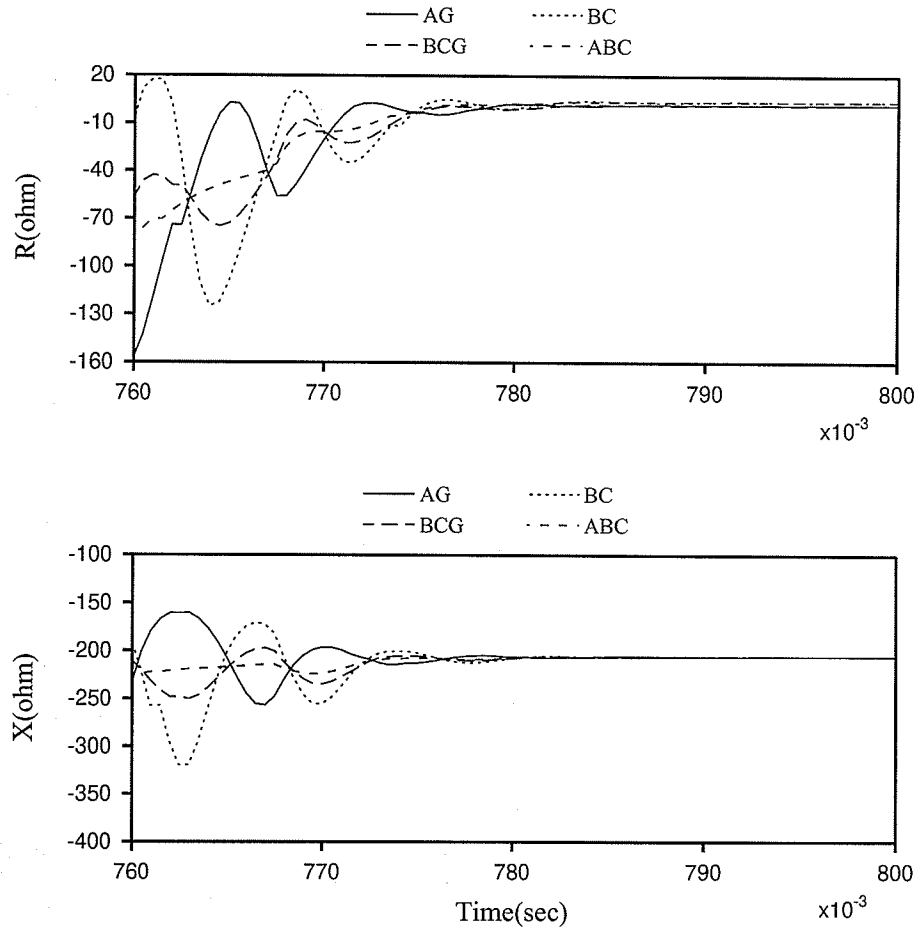


Figure 4.5. The Measured Positive Sequence Incremental Impedance.

4.5.1.2. The negative sequence incremental impedance

The negative sequence voltage and current are zero during an ABC fault, therefore the measured negative sequence incremental impedance in the ABC fault is absent in figure. 4.6. The time window is from 0.76 seconds to 0.8 seconds. The measured ΔZ_2 converges to the same value.

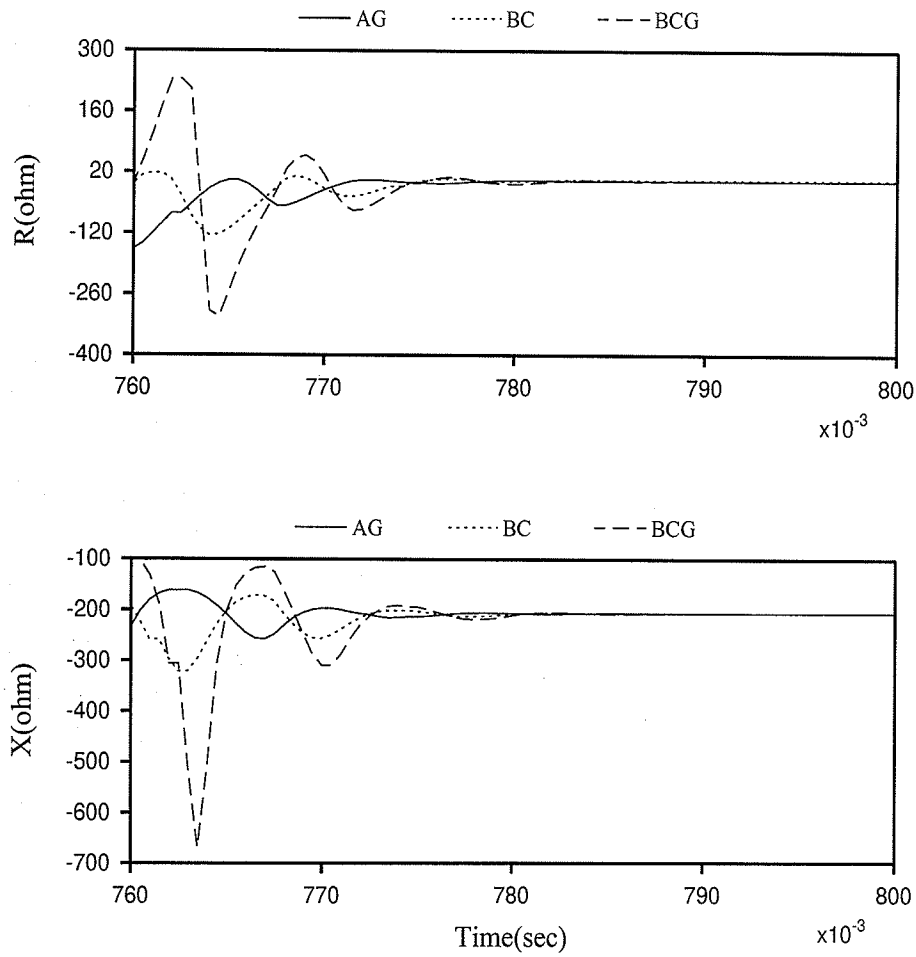


Figure 4.6. The Measured Negative Sequence Incremental Impedance.

4.5.1.3. The zero sequence incremental impedance

The zero sequence voltage and current are zero during the ABC and BC faults, therefore only the measured zero sequence incremental impedance in AG and BCG faults are presented in fig. 4.7.

The time window is from 0.76 second to 0.8 second. The measured ΔZ_0 converges to same value.

Since the ΔZ_0 is not available in ABC or BC fault, it can not be used as the directional impedance for PT relay.

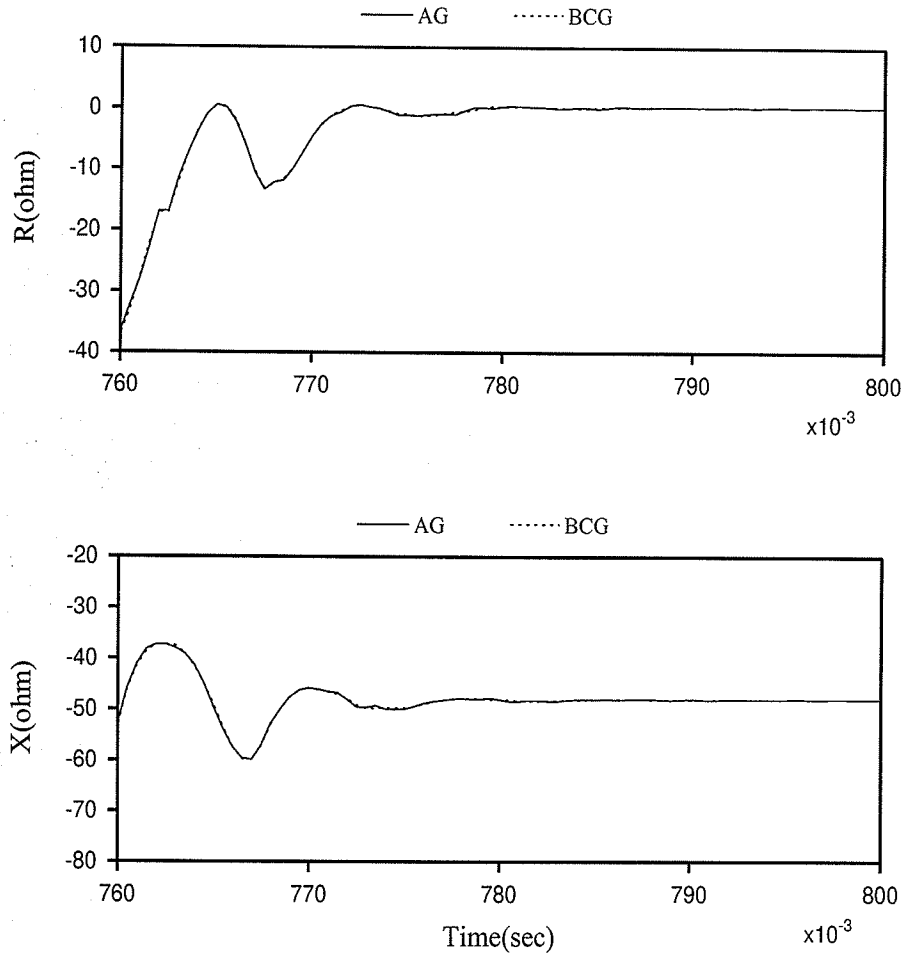


Figure 4.7. The Measured Zero Sequence directional impedance.

4.5.2. The phase incremental impedance

4.5.2.1. The phase incremental impedance of phase A

The incremental current of phase A is zero during a BC fault according to both table 4.1 and the simulation, hence the measured phase incremental impedance for faults, AG, BCG, ABC are presented in figure. 4.8. The time window is from 0.76 seconds to 0.8 seconds. The measured ΔZ_a does not converge to a uniform value in all faults.

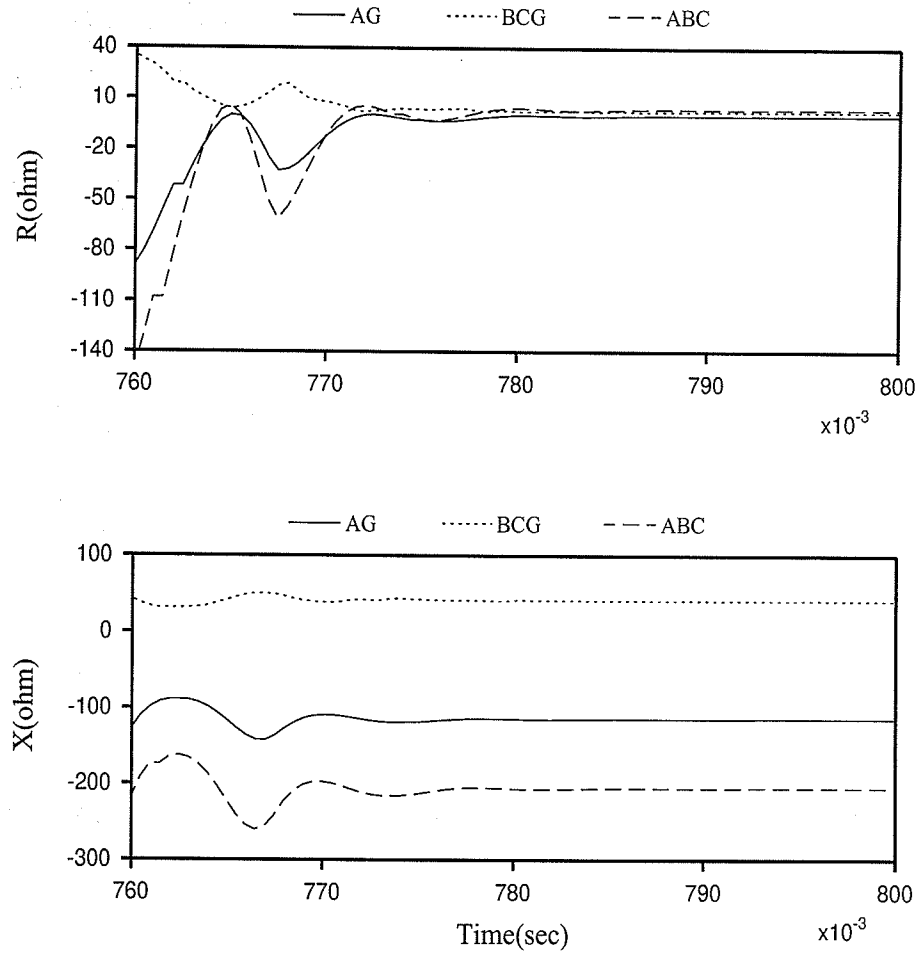


Figure 4.8. The Measured Incremental Impedance of Phase A.

4.5.2.2. The phase incremental impedance of phase B

The measured phase incremental impedances in the AG, BC, BCG, and ABC faults are presented in figure 4.9. The time window is from 0.76 seconds to 0.8 seconds. The measured ΔZ_b does not converge to a uniform value in all faults.

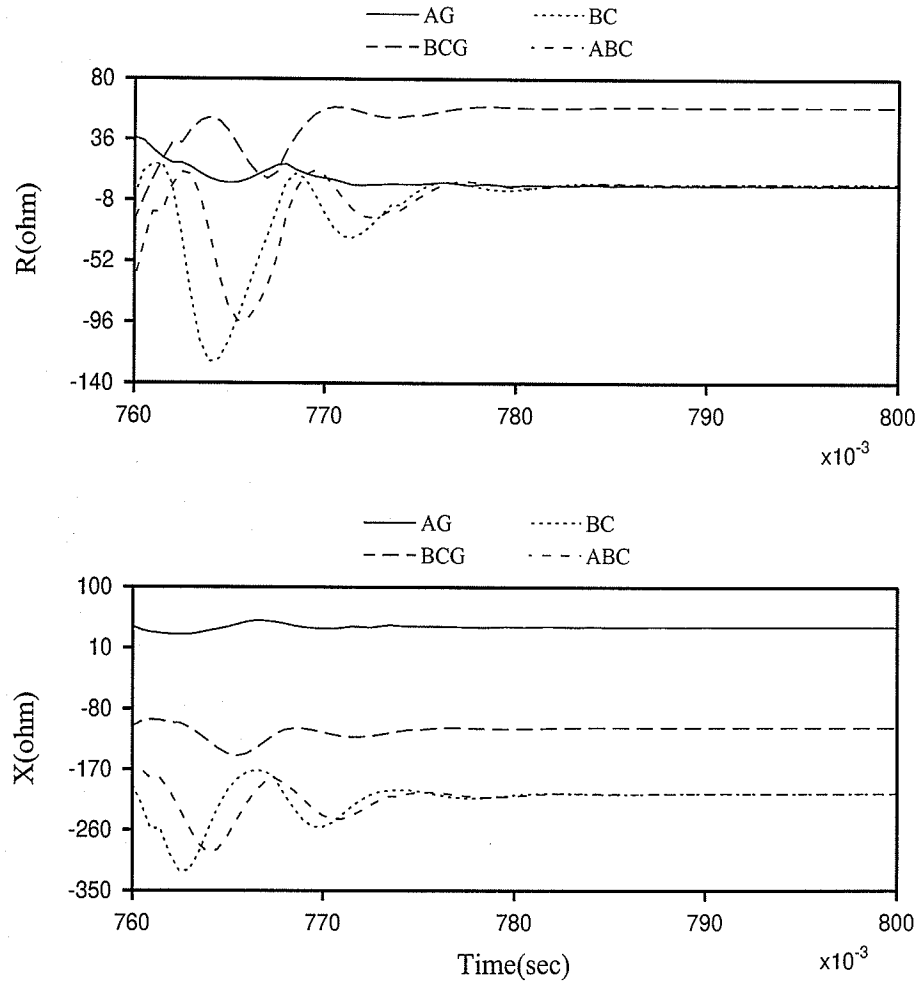


Figure 4.9. The Measured Incremental Impedance of Phase B.

4.5.2.4. The phase incremental impedance of phase C

The measured phase incremental impedances in the AG, BC, BCG, and ABC faults are presented in figure. 4.10. The time window is from 0.76 seconds to 0.8 seconds. The measured ΔZ_c does not converge to a uniform value in all faults.

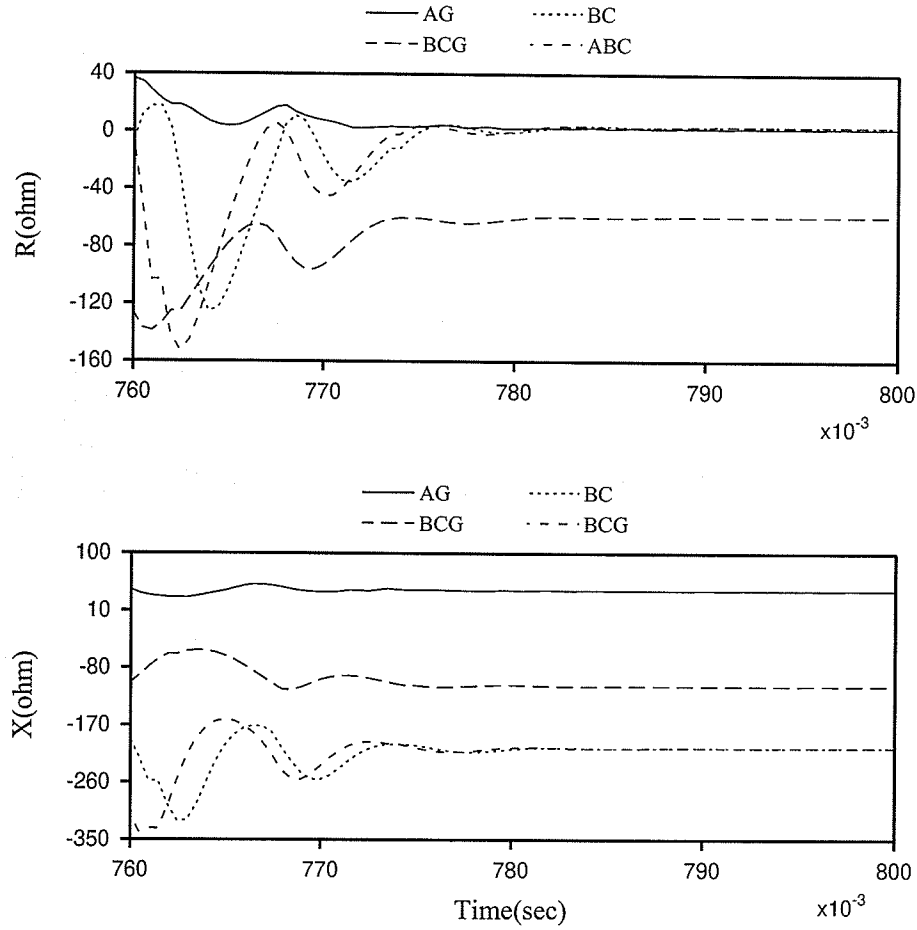


Figure 4.10. The Measured Incremental Impedance of Phase C.

4.5.3. The phase-phase incremental impedance

4.5.3.1. The phase-phase incremental impedance of phase AB

The measured phase-phase incremental impedances for AG, BC, BCG, and ABC faults are presented in figure. 4.11 The time window is set from 0.76 seconds to 0.8 seconds. The measured ΔZ_{ab} converges.

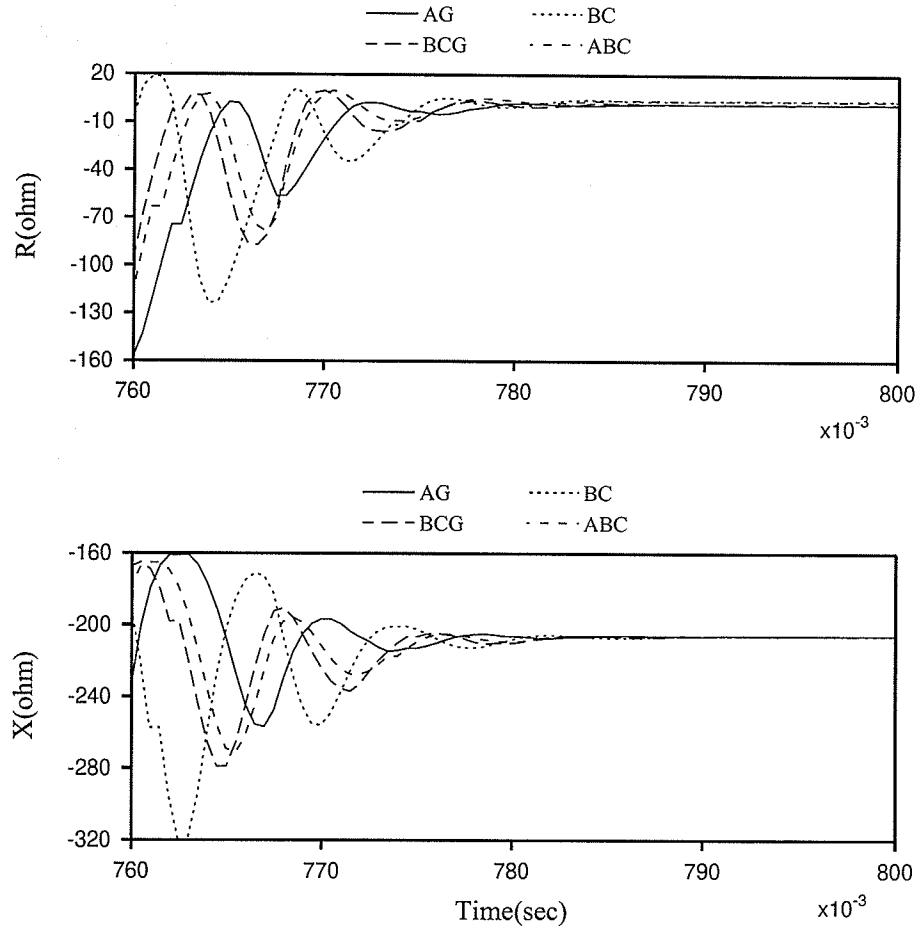


Figure 4.11. The Measured Incremental Impedance of Phase AB.

4.5.3.2. The phase-phase incremental impedance of phase BC

The incremental current of phase BC is zero in fault AG according to both analysis and simulation, therefore the measured phase-phase incremental impedances during fault BC, BCG, and ABC are presented in figure 4.12. The time window is from 0.76 seconds to 0.8 seconds. The measured ΔZ_{bc} converges.

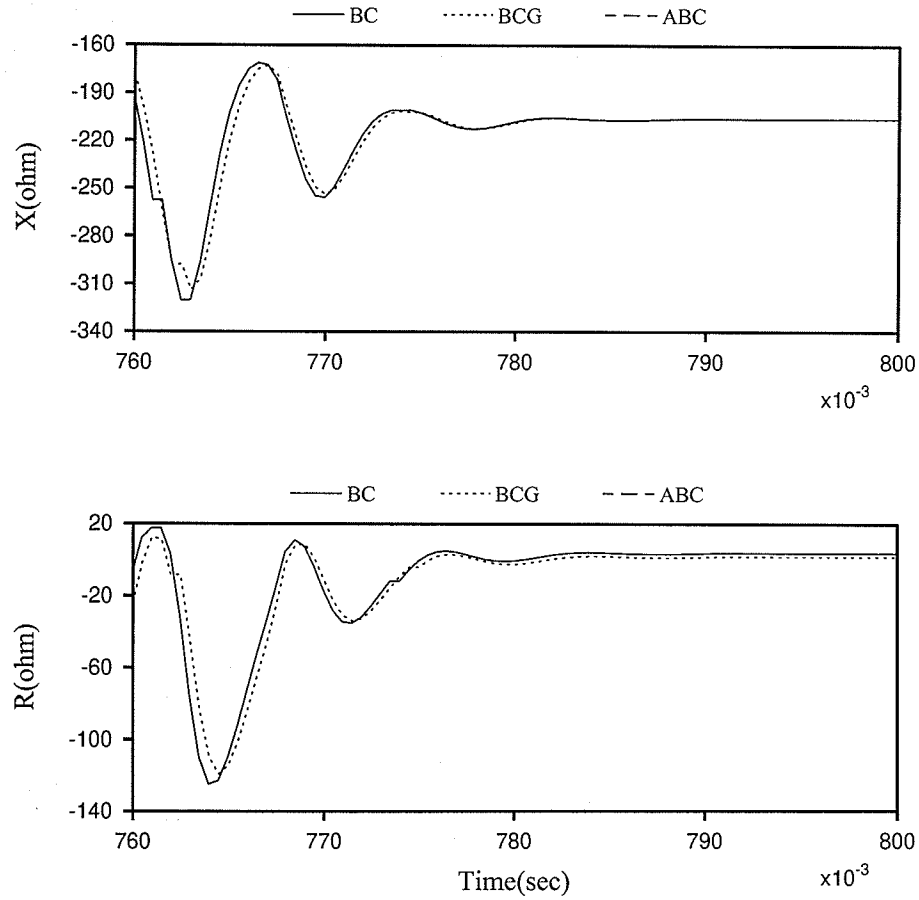


Figure 4.12. The Measured directional impedance of Phase BC.

4.5.3.3. The phase-phase directional impedance of phase CA

The measured phase-phase incremental impedances for AG, BC, BCG, ABC faults are presented in figure. 4.13 The time window is from 0.76 second to 0.8 second. The measured ΔZ_{ca} converges.

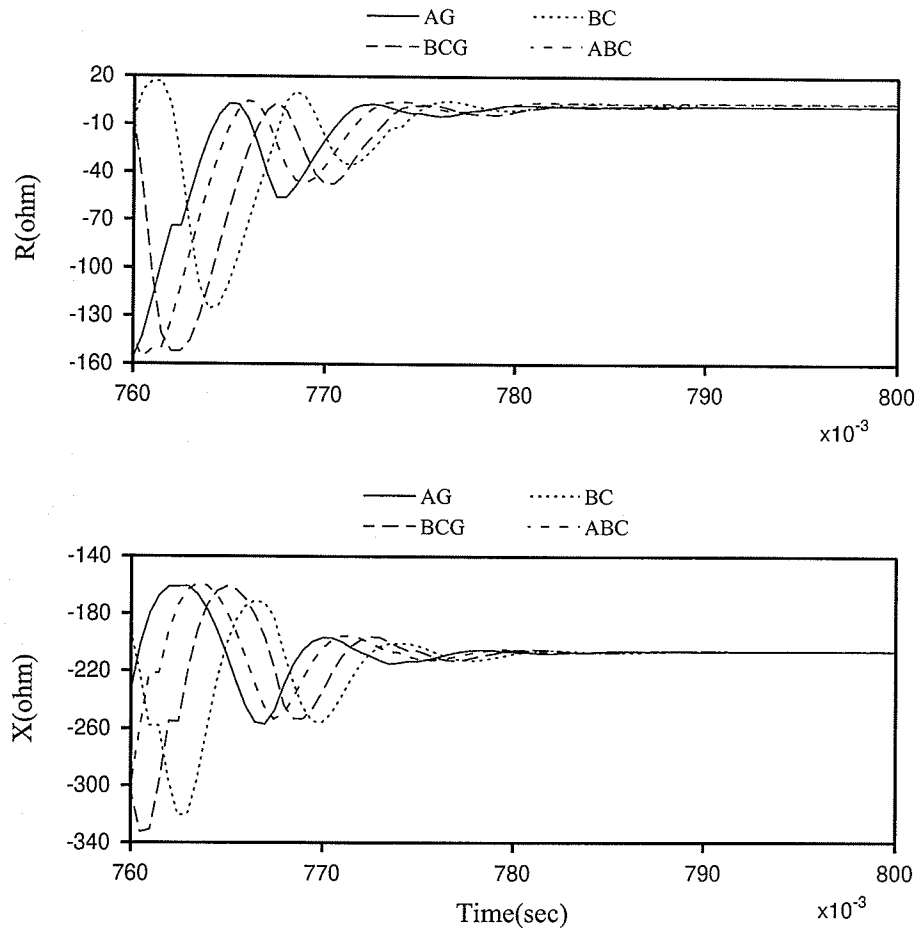


Figure 4.13. The Measured Directional Impedance of Phase CA.

4.5.4. The comparison of the methods of measuring incremental impedance

In the preceding three sections, the measured incremental impedances during faults are presented. The *availability* and *convergence* of measuring methods for the directional impedance during faults are shown in table 4.2.

Table 4.2 The *Convergence/Availability* of Methods

Fault	ΔZ_1	ΔZ_2	ΔZ_0	ΔZ_a	ΔZ_b	ΔZ_c	ΔZ_{ab}	ΔZ_{bc}	ΔZ_{ca}
AG	C	C	C	NC	NC	NC	C	NA	C
BC	C	C	NA	NC	NC	NC	C	C	C
BCG	C	C	C	NC	NC	NC	C	C	C
ABC	C	NA	NA	NC	NC	NC	C	C	C

In table 4.2, the measuring method is identified by column and the fault type is identified by row. Each cell contains the convergence/availability value pair for a method in a fault. The value 'C' means the a method is converged and available in the fault, the value 'NA' means a method is unavailable in that fault, value 'NC' means a method is not converged but available.

Table 4.2 shows that the sequence incremental impedance always converges if it is available, especially for the positive sequence incremental impedance which is available and converged in every fault. The phase incremental impedance does not converge and is unavailable sometimes. The phase-phase incremental impedance converges but is unavailable sometimes. Although the simulation does not cover all faults, the measurement of ΔZ_{ab} in a fault BG is the same as the measurement of ΔZ_{ca} in a fault AG, the measurement of ΔZ_a in a fault BG is the same as the measurement of ΔZ_c in a fault AG. Therefore table 4.2 contains the information for the phase incremental impedances and the phase-phase incremental impedances for all faults.

Results in table 4.2 prove that the method of ΔZ_1 is always available and converges during all faults.

4.6. The influence of generator source on the measurement of PSII

The analysis and simulation of ΔZ_1 in the former section are based on the assumption that the sources in a power system are ideal voltage sources. In fact, synchronous machines are the major power system sources, and the majority of them are salient-pole synchronous machines. A machine differs from an ideal voltage source because its internal voltage and internal impedance

are not constant during a fault. Does this fact constitute a practical challenge to the application of the PSII? Figure 1.9 illustrates a case from the practical system where the ΔZ_1 trajectory does not converge to the expected value. This section repeats the simulation of PSII for different fault types and pre-fault load conditions by replacing the left hand source with a salient-pole synchronous machine. The simulation investigates the influence of the fault type, the exciter condition, and the power angle on the measured PSII.

4.6.1. The influence of fault type

The measured PSII in figure 4.14 are very close to each other after 2.475s. The pre-fault conditions of the machine are a 0.5 radian power angle and 1.15pu exciter reference. Faults are applied at point F2 at 2.3 seconds.

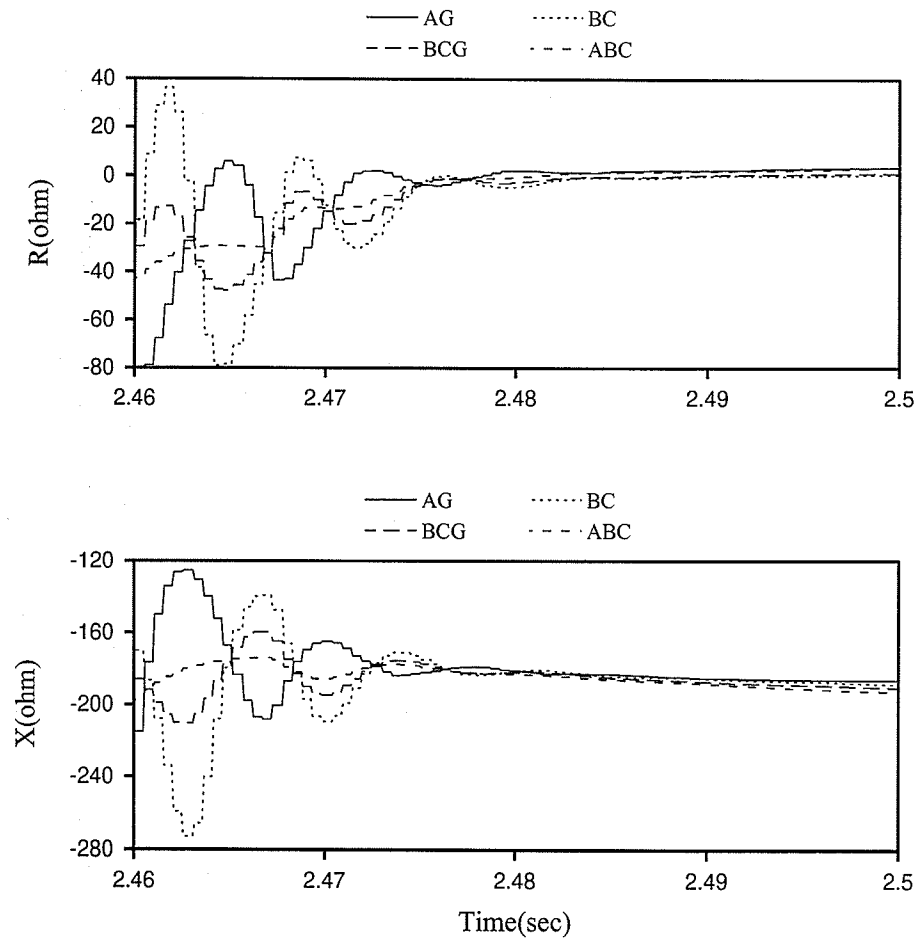


Figure 4.14. The Measured PSII in the Different Faults.

4.6.2. The influence of load flow

Figure 4.15 presents the measured PSII for different pre-fault power angles when an ABC fault is applied on the system at point F2. The largest difference in reactance is only about 10 ohm. The imaginary part of ΔZ_1 can be used to expand the PT relay protection zone in these forward faults. The imaginary part of ΔZ_1 is increasing during the fault because the source impedance of the generator changes from subtransient impedance to transient impedance, and steady state impedance. The time constant from transient to steady state is about 0.3~2.0 second, so the PSII keeps changing in the time window of figure 4.15.

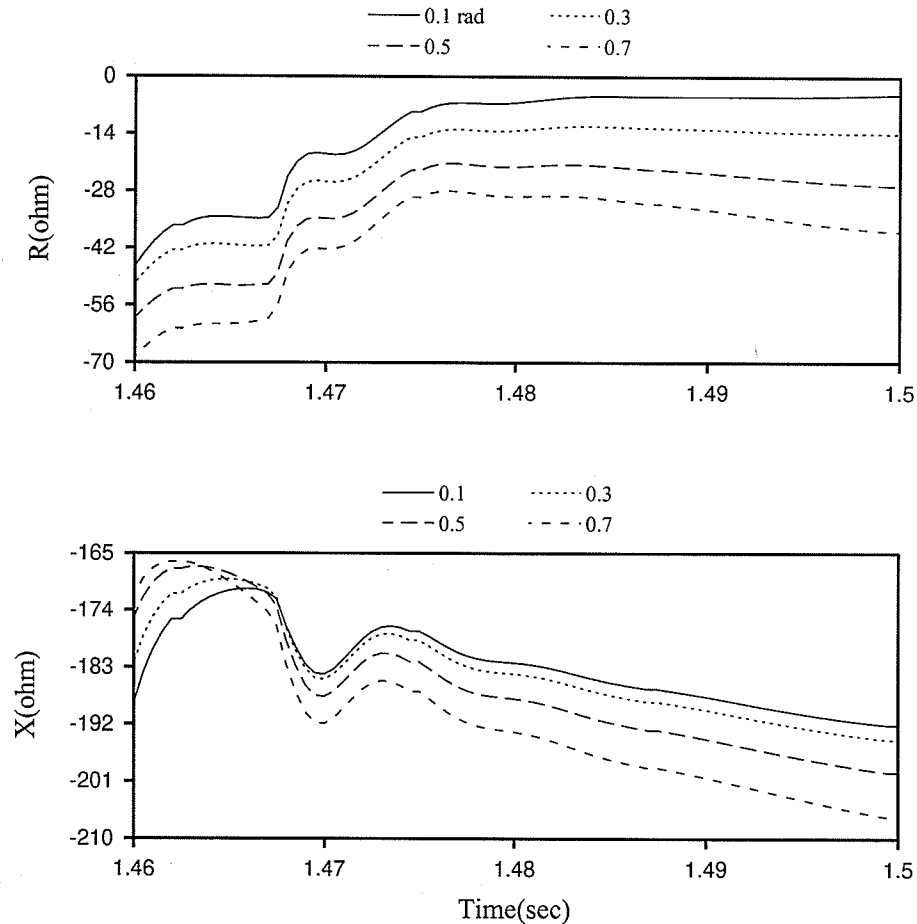


Figure 4.15. The Measured PSII in the Different Load Conditions.

4.6.3. The influence of exciter reference

Figure 4.16 displays the measured PSII for different pre-fault Exciter reference when an ABC fault is applied on the system at point F2. In these cases, the difference of reactance is small. The reactive part of ΔZ_1 can be used to expand the PT relay protection zone in these forward faults.

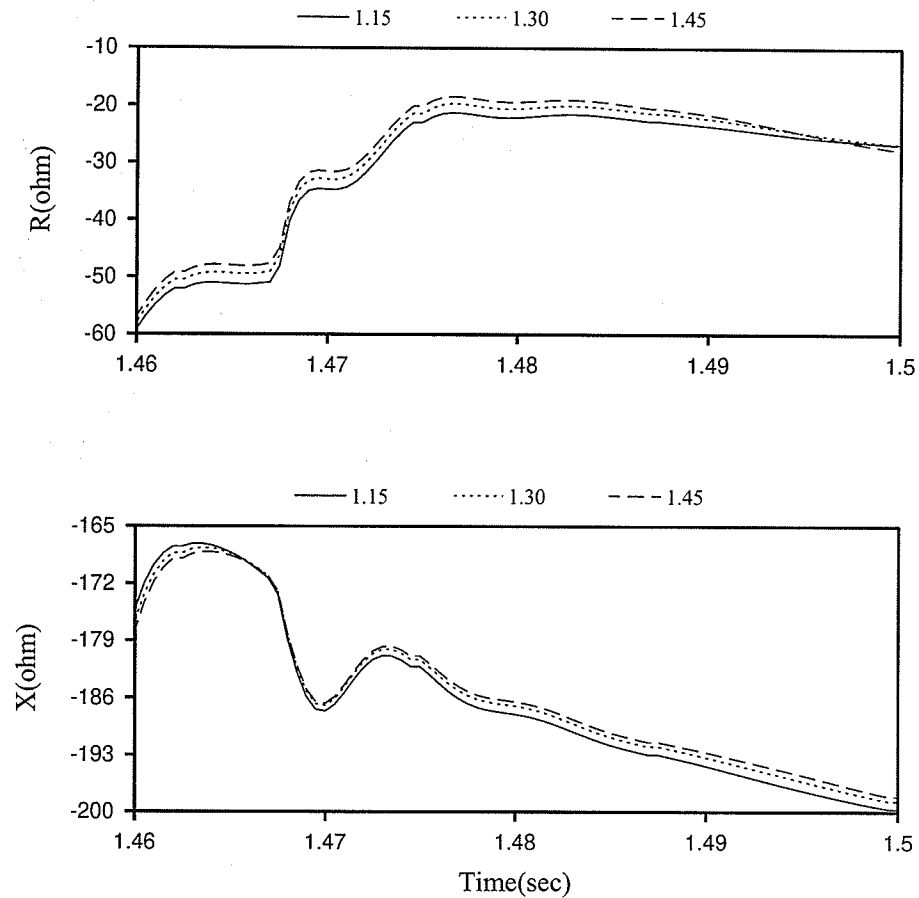


Figure 4.16. The Measured PSII in the Different Excitor Reference.

4.7. The measurement of the PSII in the different fault directions

Figure 4.17 shows the measured PSII in the forward and reverse AG faults. The reactive part is negative in the forward fault and positive in the reverse fault.

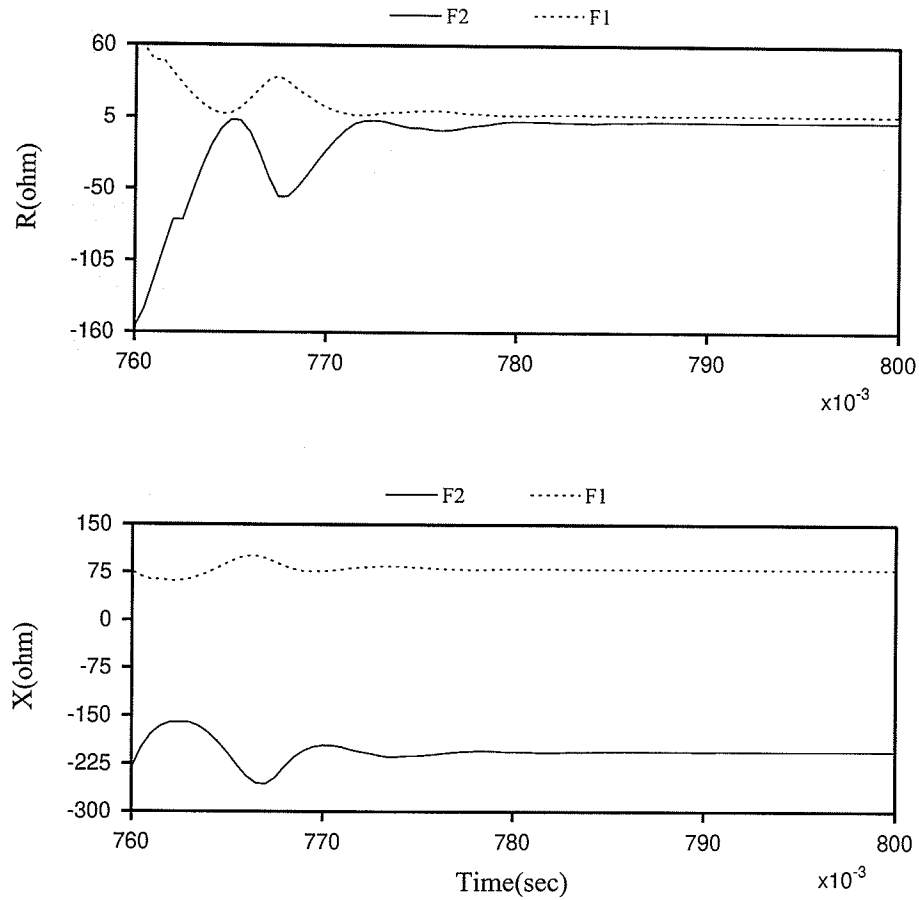


Figure 4.17. The Measured PSII in the F2 & F1 AG Fault.

4.8. Summary

1. In this chapter, the detailed analysis and simulation of incremental impedances are carried out under the assumption that all sources in the power system are ideal voltage sources.
2. The PSII possessed both *convergence* and *availability* in various fault simulations. The phase incremental impedance did not converge in different fault types and some times was unavailable. The phase-phase incremental directional impedance possessed good convergence in different fault types but was unavailable in some cases. Therefore the PSII was selected as the directional impedance of PT relay. This conclusion is based on the analysis and simulation in the ideal voltage source system.
3. The presence of generator in the power system has no significant adverse impact on the PSII.

The PSII theory is founded on the basis of a time invariant power system. Since the source impedance and voltage are not constant for a salient-pole machine during the fault, the PSII does not converge. However, the PSII can still present the information associated with the fault direction. The supporting evidence was found in the simulation for different faults and load conditions when the left hand source was replaced by a salient-pole synchronous generator.

4. The simulation in section 4.6 shows that the real part of the PSII can be positive in the fault when a generator is present. So the setting zone of the DE element of the PT relay should stretch into the fourth quadrant. The imaginary part of the PSII increases during the fault since the source impedance for the generator is changing from the subtransient impedance, to transient impedance, to the steady state impedance.

Chapter 5. The Verification of the PT Relay

The PT relay's structure is typical of digital relays, as exhibited in figure 5.1.

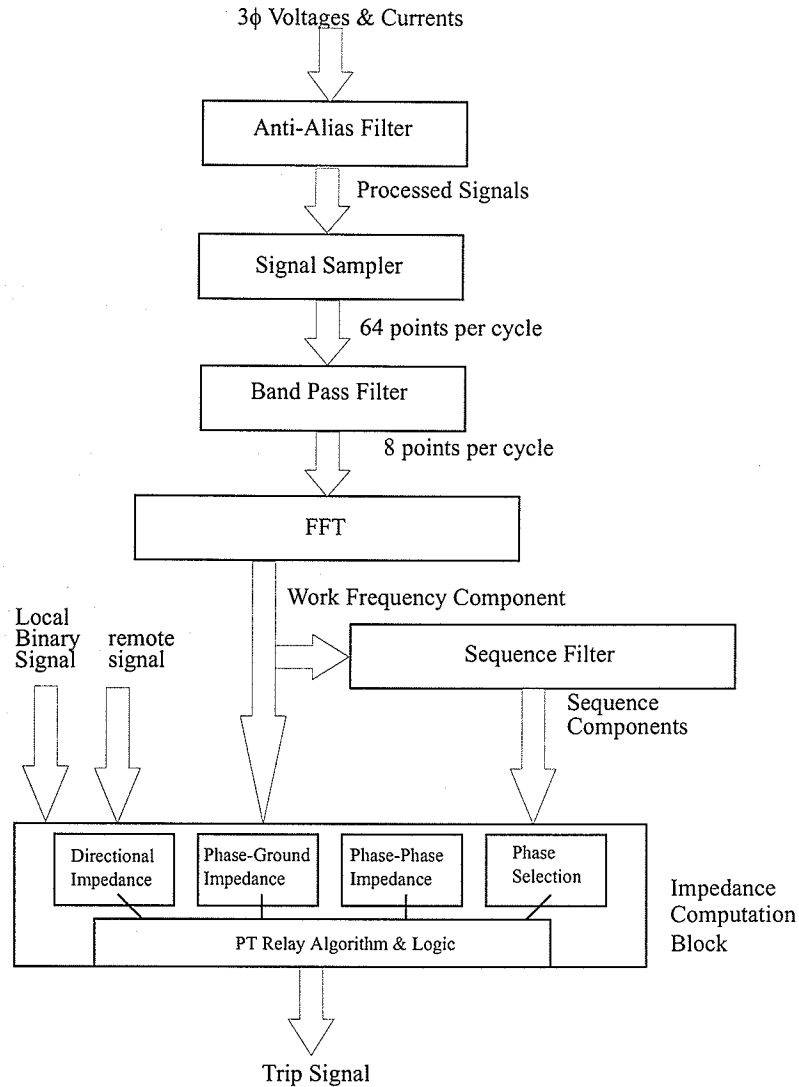


Figure 5.1. The PT Relay Structure.

The system voltage and current are fed into the analogue anti-aliasing filter which limits the frequency in its output for the A/D sampler. The processed signals are sampled at a rate of 2^n per cycle. In the PT relay, we use 64 points per cycle. The samples are then fed into bandpass decimating filter to limit the bandwidth of the voltage and current signals. After the bandpass filter, eight points of the samples are extracted and fed into the FFT routine which computes the fre-

quency components. The computed fundamental frequency phasors are fed into the sequence filter to produce the positive, negative and zero sequence phasors. The three sequence voltages, three sequence currents, the voltage and current components, and local binary inputs and remote signals are fed into the impedance computation block to calculate ΔZ_1 , phase-ground impedance, phase-phase impedance, and phase selection signals. These computation results are used by the PT relay algorithm and logic to determine the relays' behaviour.

The components of the PT relay have been fully illustrated in chapter 2. This chapter will verify the algorithm of these components by observing their behaviours during the faults. The verification scenario includes the verification of the DI, DE, LI, PS, and IE elements in various operating modes.

Figure 5.2 illustrates the power system simulation. The fault at F2 is called the forward fault and the fault at F1 is called the reverse fault.

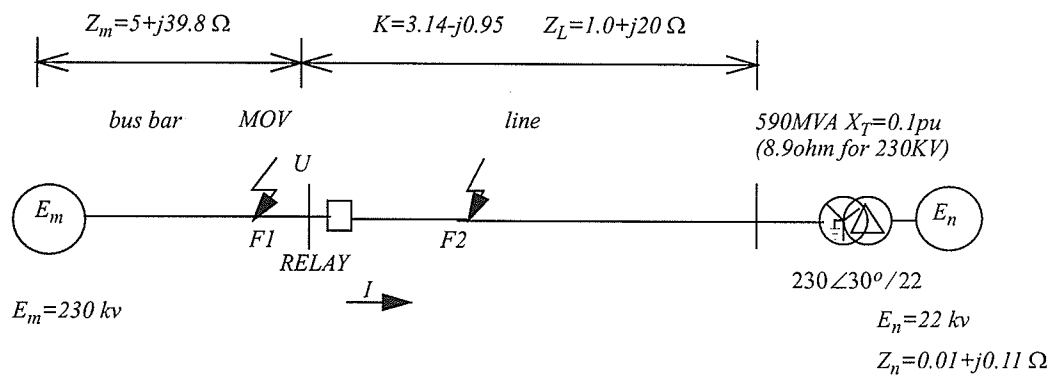


Figure 5.2. PSCAD/EMTDC Simulation System.

5.1. The validity of the DI and the DE elements

The DI and the DE elements are modelled in chapter 3. The advantage of PSII over other incremental impedances was thoroughly investigated in chapter 4. This section will prove its suitability to identify the fault direction for the PT relay.

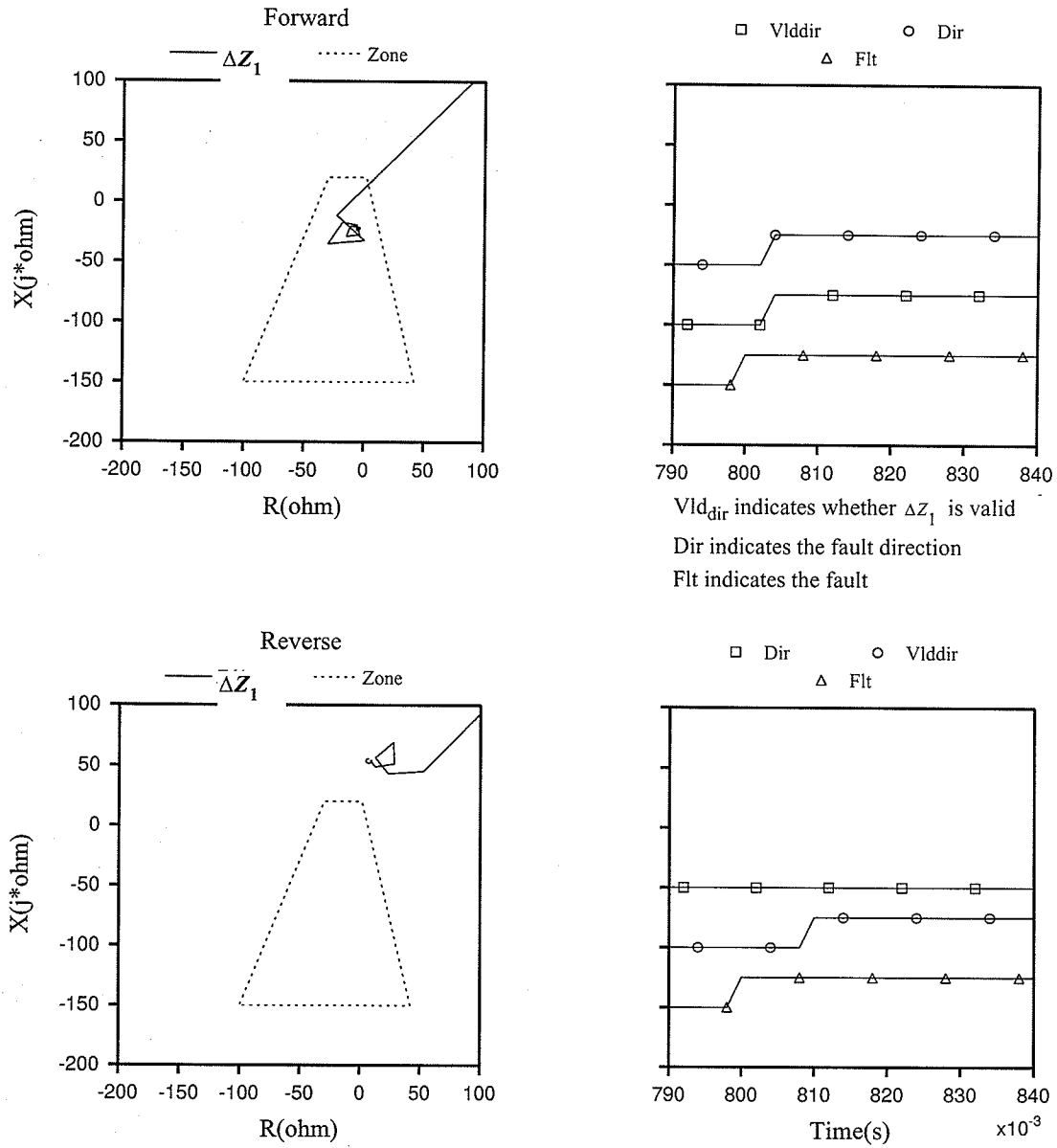


Figure 5.3. The DI & the DE Elements.

Figure 5.3 is a graph matrix. The first row of the matrix records the behaviour of the DI and DE elements in a forward AG fault, and the second row records the information of the DI and DE elements in a reverse AG fault. The left sub-figure of each row shows the trajectory of ΔZ_1 and the trip zone of the DE element. The right sub-figure of each row shows the logic output of the DI and DE elements.

Δz_1 is valid for both the forward and the reverse faults since the signal 'Vlddir' jumps up to a high level, and the signal 'Dir' jumps up to a high level only during the forward fault. These facts prove that the DI and DE elements both work well.

5.2. The validity of the LI element

In figure 5.4, the left part contains two curves. Curve 'Rk' describes the resistance of z_k and curve 'Rld' resistance of the z_{ld} . The right part contains two logic curves. Curve 'Flt' indicates a fault by its rising edge, and curve 'Vld' indicates a valid z_{ld} by its high level.

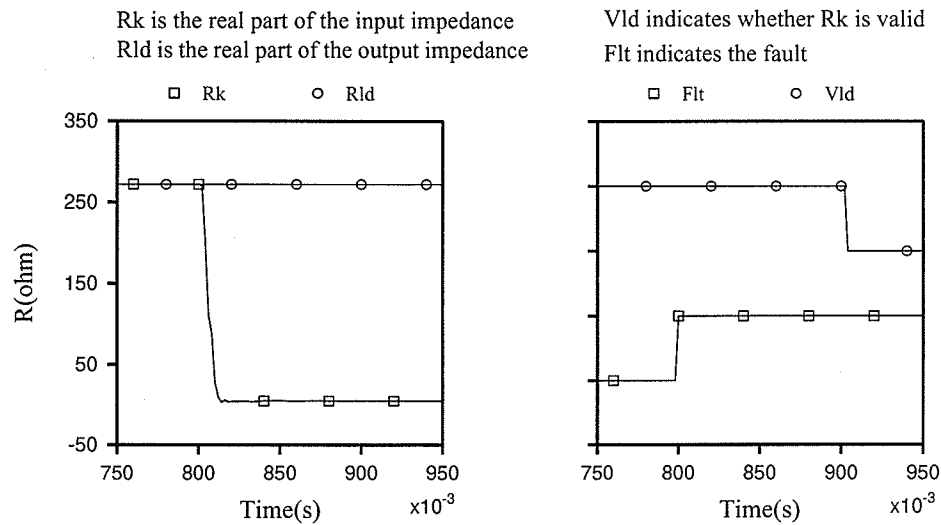


Figure 5.4. The LI Element Performance in Fault.

The theory of the LI element is first introduced at section 3.4. Here, t_1 sets to 200ms, t_2 sets to 100ms. Within the first post-fault 100ms, the output resistance maintains the pre-fault load resistance and the 'Vld' signal remains at logic high. So the LI element can effectively produce pre-fault impedance.

5.3. The validity of the PS element

The PS element provides the ancillary signal used to control the adaptive feature of the PT relay.

In order to improve the characteristic of the quadrilateral relay, the PS element is expected to have the following properties:

1. Quick response in fault

Since the quadrilateral distance relay can capture a fault in one or two cycles even without the adaptive feature, the phase selection element should respond before the setting zone quadrilateral relay captures the fault.

2. Determination of fault type

The PS element should be able to identify the phase where the measured impedance is the impedance in the fault loop. Figure 5.5 illustrates the detailed performance of the PS element in the system fault. Each row of the figure matrix represents the record of the performance of the element in a case, so that there are a total of four cases that can be identified from the title of the sub-figure in the first column. The sub-figures in the first column show the three phase currents in the simulation. The sub-figures in the second column shows the amplitude of three phase-phase incremental currents. The sub-figures in the third column records the phase selection logic signal in the fault. In this figure, the faults are applied to the system at 800ms. During the first 10ms after the fault, the phase-phase incremental currents have reached a significant level, and transient behaviour occurs in the logic output of the PS element. At 810ms, the PS element produces a stable output after the phase-phase incremental currents have been built up to a significant level. The relationship among these quantities correlates to the analysis of the PS element in chapter 3.

In an AG fault, the incremental currents of phase AB and CA are equal, and that of phase BC is zero. In the BC and BCG fault, the incremental current reaches maximum in phase BC and is equal in phases AB and CA. In the ABC fault, the incremental current amplitude is equal in the three phases AB, BC, and CA.

The findings from the investigation of this figures indicate that the PS element can correctly identify a fault type in less than 10ms, even in the worst case, the BCG fault. And the measuring element selected by the PS element can measure the exact impedance in the fault loop. These findings are the evidence which supports the use of the PS element as the adaptive control signal for the IE element.

5.4. The validity of the IE element

The IE element of the PT relay has a dynamic protection zone. This feature makes it different from the simple quadrilateral relay. The PT relay's trip zone is modified by its built-in algorithm in both the horizontal and vertical directions. The amount of horizontal modification is decided by the load condition, fault direction and phase selections. The PT relay can run in Mode 1 or Mode 2 as stated in chapter 3. The vertical modification feature of the PT relay is enabled when the relay operates in Mode 1 and is disabled in Mode 2. The amount of vertical modification is determined by the directional impedance, the fault direction, and the operation mode.

This section will show a series of impedance figures to illustrate the trip zone of the PT relay in faults. In these figures, the setting zone of the impedance element is the dashed line zone, and the actual trip zone is the solid line zone. In order to distinguish the setting zone from the protection zone, both are shown in the same figure.

5.4.1. The IE element in the forward fault in mode 1

If the PT relay operates in mode 1, the horizontal modification of the protection zone of a phase is enabled when this phase is selected as a faulted phase. The DE element can identify a forward fault and the LI element can produce valid pre-fault resistance. The vertical modification of the protection zone of a phase is started when a forward fault is detected and this phase is selected as the faulted phase.

In order to demonstrate the dynamic feature of the IE element in the impedance plane, the MATLAB relay model is used in the simulation. The MATLAB relay model is an accurate implementation of the PT relay algorithm in the MATLAB language. The MATLAB provides a Fortran interface function which can call the MATLAB model, thus it allows that PSCAD/EMTDC simulation seamlessly incorporates the MATLAB relay model. In the simulation, by calling the Fortran interface, the PSCAD/EMTDC runtime will invoke the MATLAB relay model which receives the samples from the simulation and processes the data in the PT relay algorithm. The computation results of the impedance and the dynamic protection zone is shown in a figure.

figure 5.6 is obtained when the relay operates in Mode 1 and a forward AG fault is applied to the system at 800ms. This figure is a graph matrix where the upper six sub-figures describe the adap-

tive protection zones of the six phase IE elements and the sub-figure in the third row shows ΔZ_1 and the trip zone of the DE element.

The relay identifies a forward fault since falls within the trip zone of the DE element. The PS element identifies phase A as the faulted phase, so the protection zone of the IE element of phase A expands from the setting zone into the trip zone as shown in the sub-figure of phase A. The protection zones of all unfaulted phases are not modified.

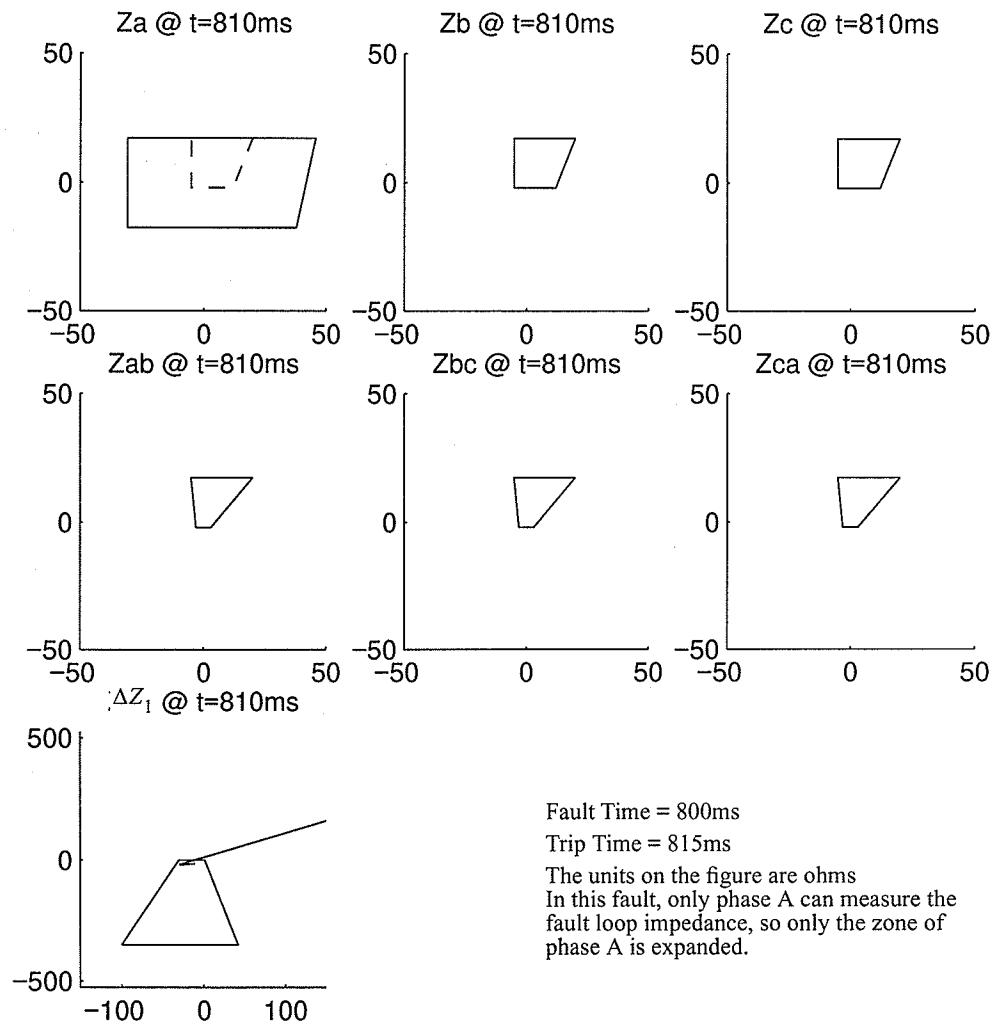


Figure 5.6. The Protection Zone in Mode 1 at a Forward AG Fault.

Figure 5.7 is obtained when the PT relay operates in mode 1 and a forward BC fault is applied to the system at 800ms. The relay identifies a forward BC fault and the protection zone of the IE element of phase BC is expanded during the fault.

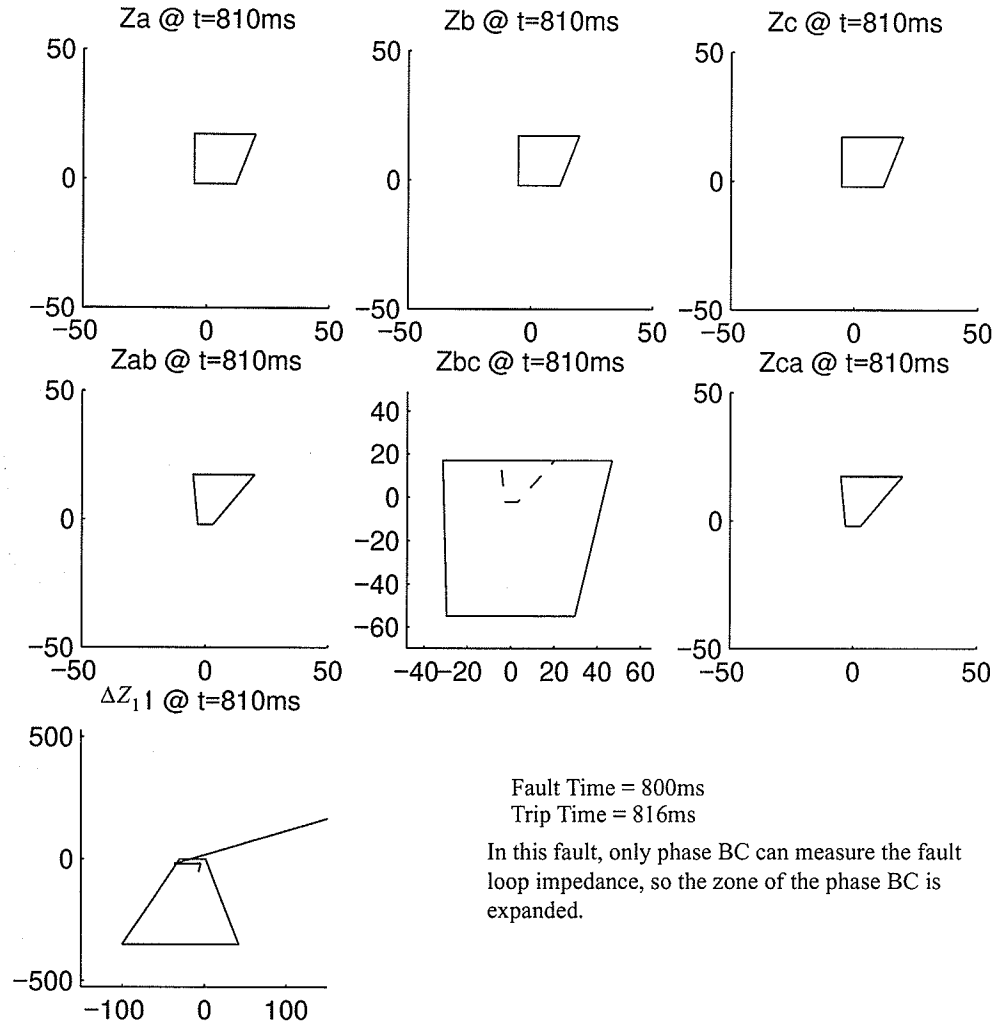


Figure 5.7. The Protection Zone in Mode 1 at a Forward BC Fault.

Figure 5.8 is obtained when the PT relay operates in mode 1 and a forward BCG fault is applied to the system at 800ms. The relay identifies a forward fault and the protection zones of the IE elements of phases B, C, and BC are expanded during the fault.

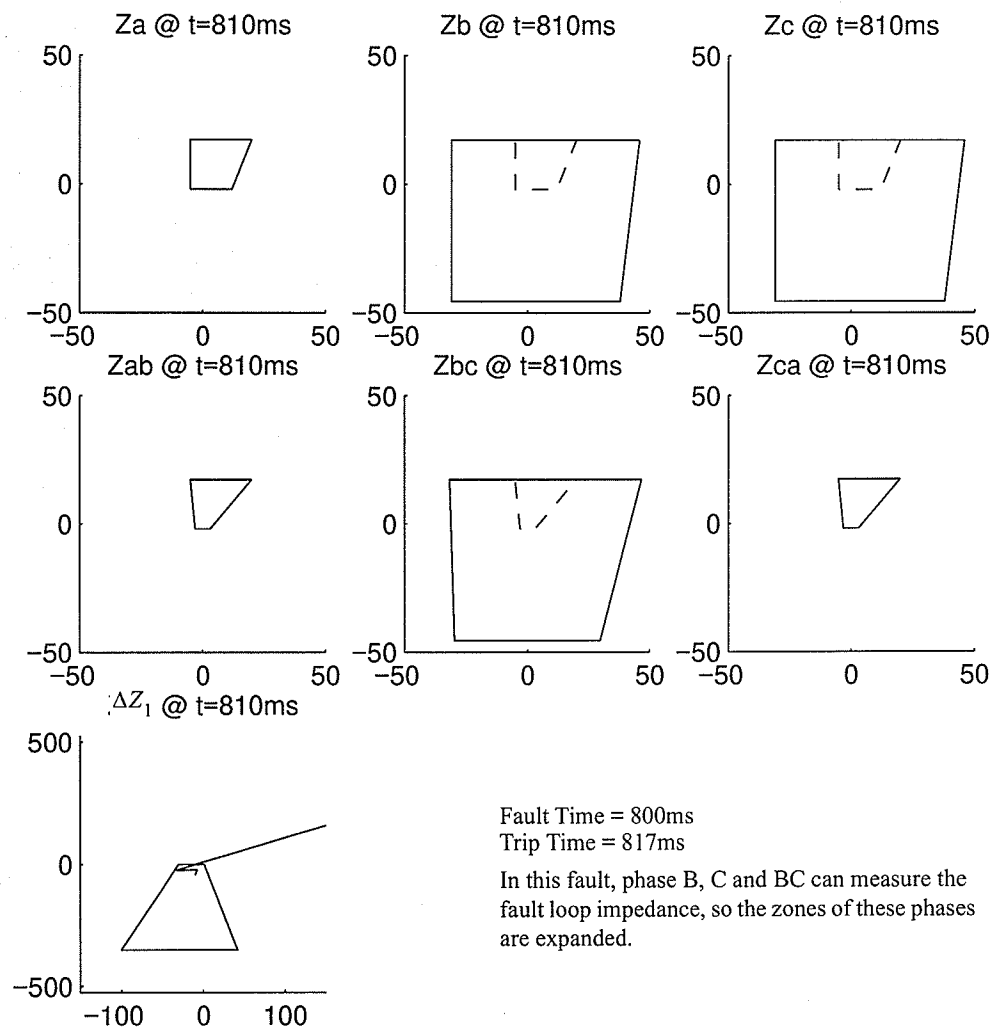


Figure 5.8. The Protection Zone in Mode 1 at a Forward BCG Fault.

Figure 5.9 is obtained when the PT relay operates in mode 1 and a forward ABC fault is applied to the system at 800ms. The relay identifies a forward fault and the protection zone of the IE elements of all phases are expanded during the fault.

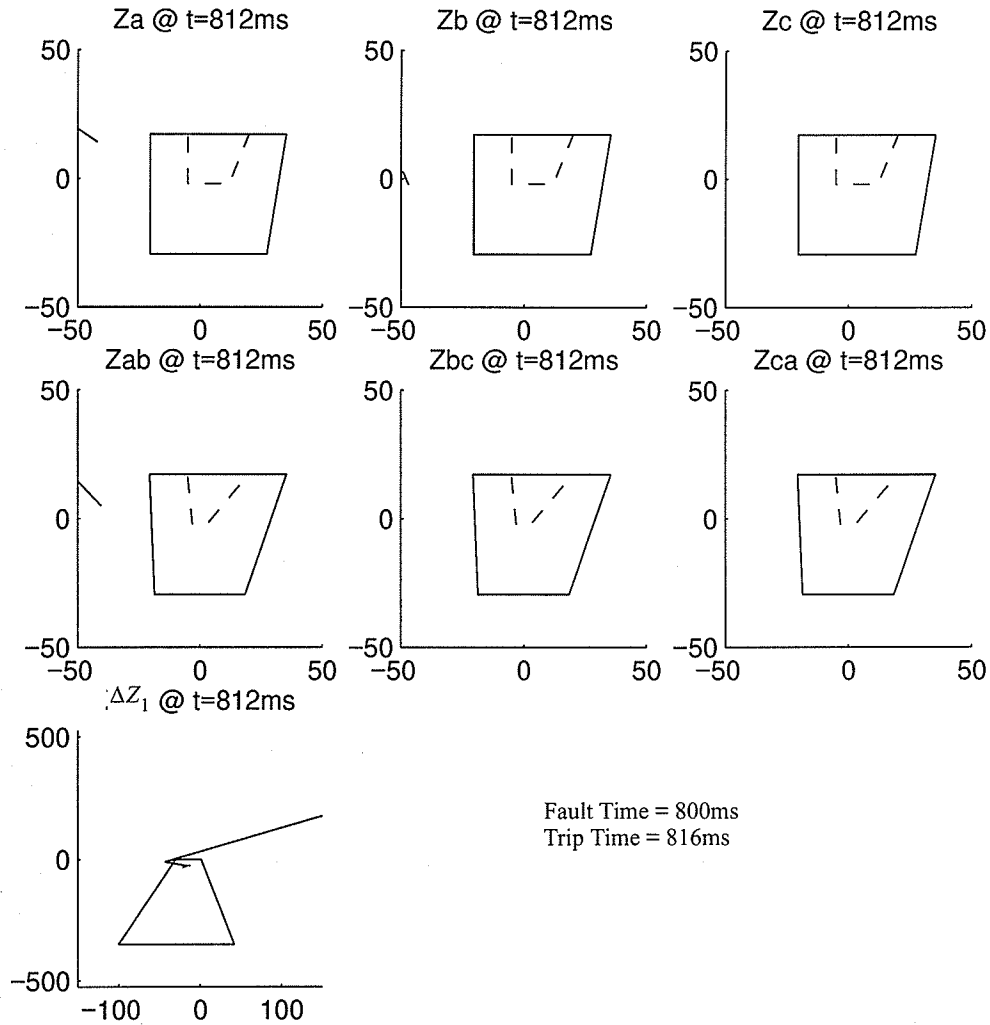


Figure 5.9. The Protection Zone in Mode 1 at a Forward ABC Fault.

5.4.2. The IE element in the reverse fault at mode 1

Figure 5.10 is obtained when the PT relay operates in mode 1 and a reverse AG fault is applied to the system at 800ms. Since the trajectory of ΔZ_1 locates outside the trip zone of the direction element, the relay identifies a reverse fault, and horizontal modification of the protection zone does not occur. Vertical modification of the protection zone takes place in the IE elements of all phases in a reverse fault. The actual trip zones of the IE elements are flipped up in the reverse fault.

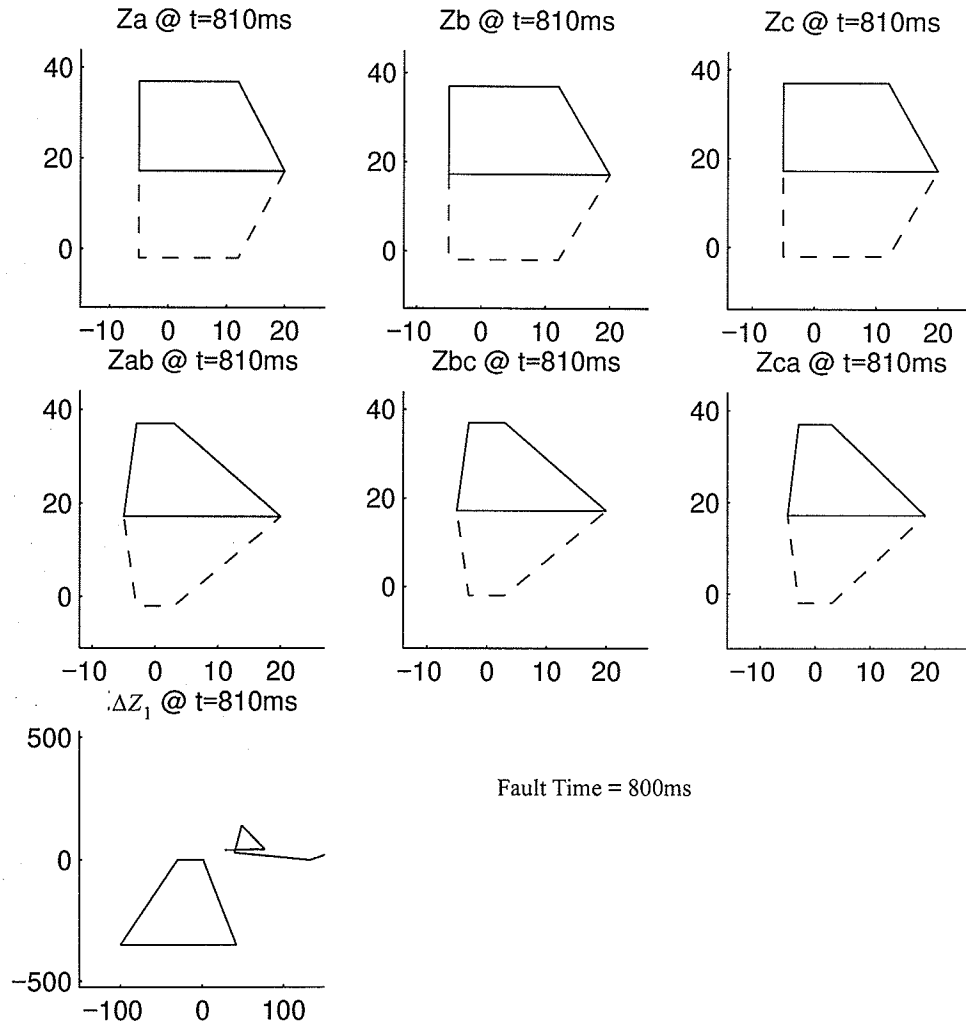


Figure 5.10. The Protection Zone in Mode 1 at a Reverse AG Fault.

5.4.3. The IE element in the forward fault at mode 2

If the PT relay operates in mode 2, the horizontal modification of the protection zone of a phase is enabled when this phase is selected as the faulted phase, the DE element identifies a forward fault, and the LI element produces the valid pre-fault resistance. The vertical modification of the protection zone of the phase is disabled.

Figure 5.11 is obtained when the PT relay operates in mode 2 and a forward AG fault is applied to the system at 800ms. Since the DE element identifies a forward fault and phase A is selected as the faulted phase, horizontal expansion of the protection zone takes place in phase A.

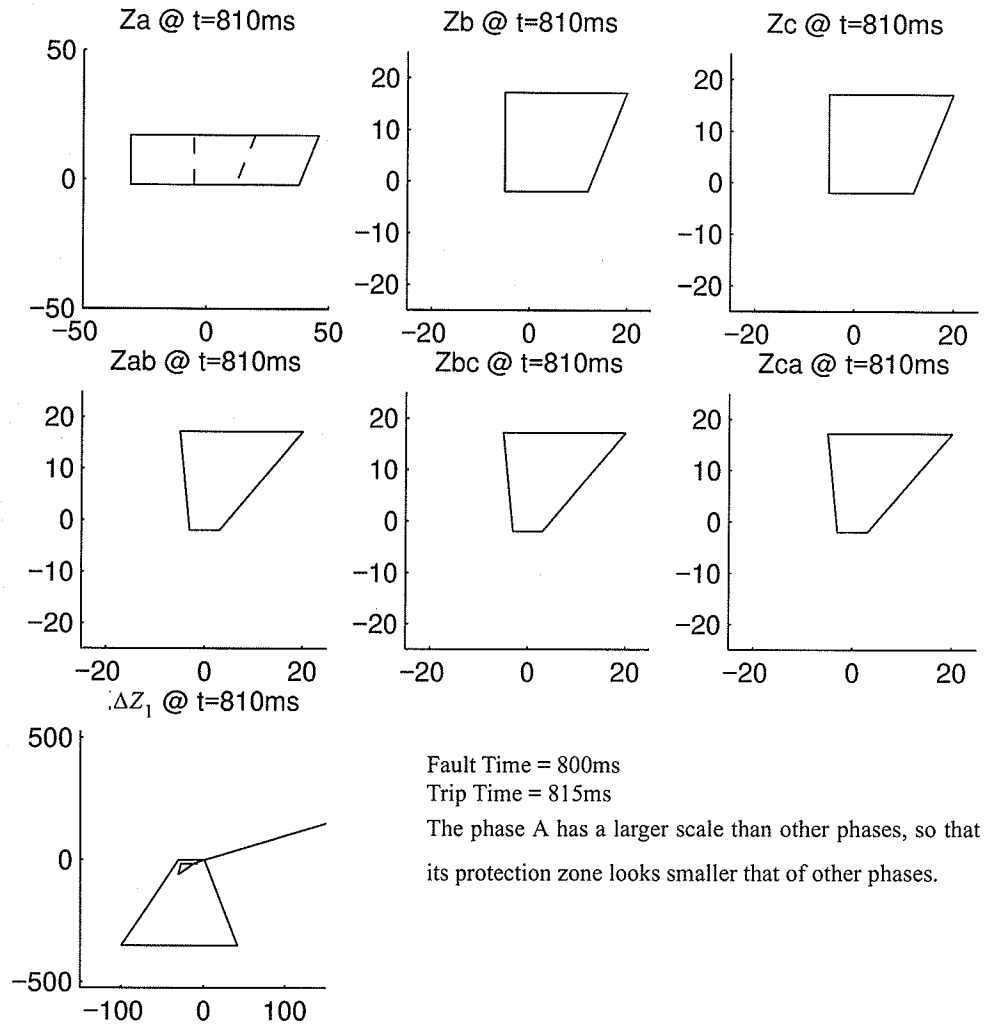


Figure 5.11. The Protection Zone in Mode 2 at a Forward AG Fault.

Figure 5.12 is obtained when the PT relay operates in mode 2 and a forward BC fault is applied to the system at 800ms. The relay identifies a forward fault and the trip zone of the IE element of phase BC is expanded.

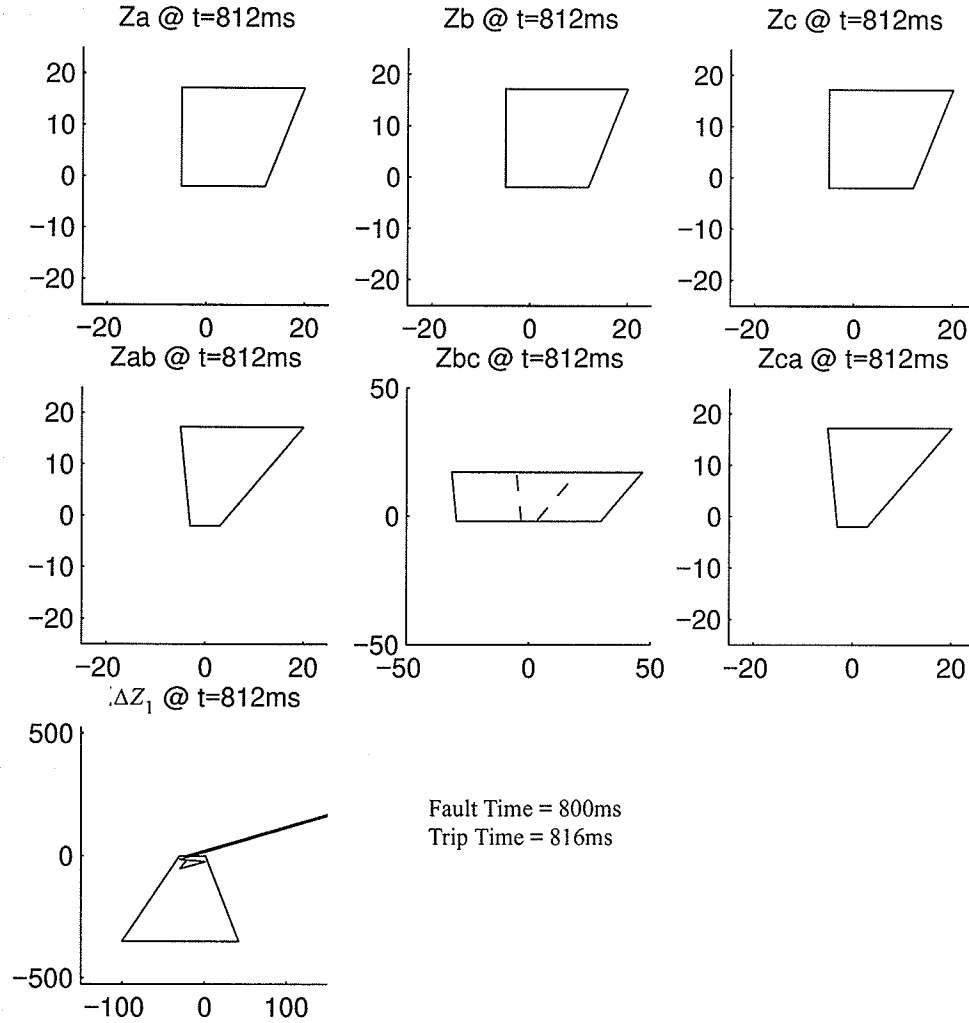


Figure 5.12. The Protection Zone in Mode 2 at a Forward BC Fault.

Figure 5.13 is obtained when the PT relay operates in mode 2 and a forward BCG fault is applied to the system at 800ms. The relay identifies a forward fault and the PS element selects phase BC, B, and C as the faulted phases. The protection zones of the IE elements of these phases are expanded.

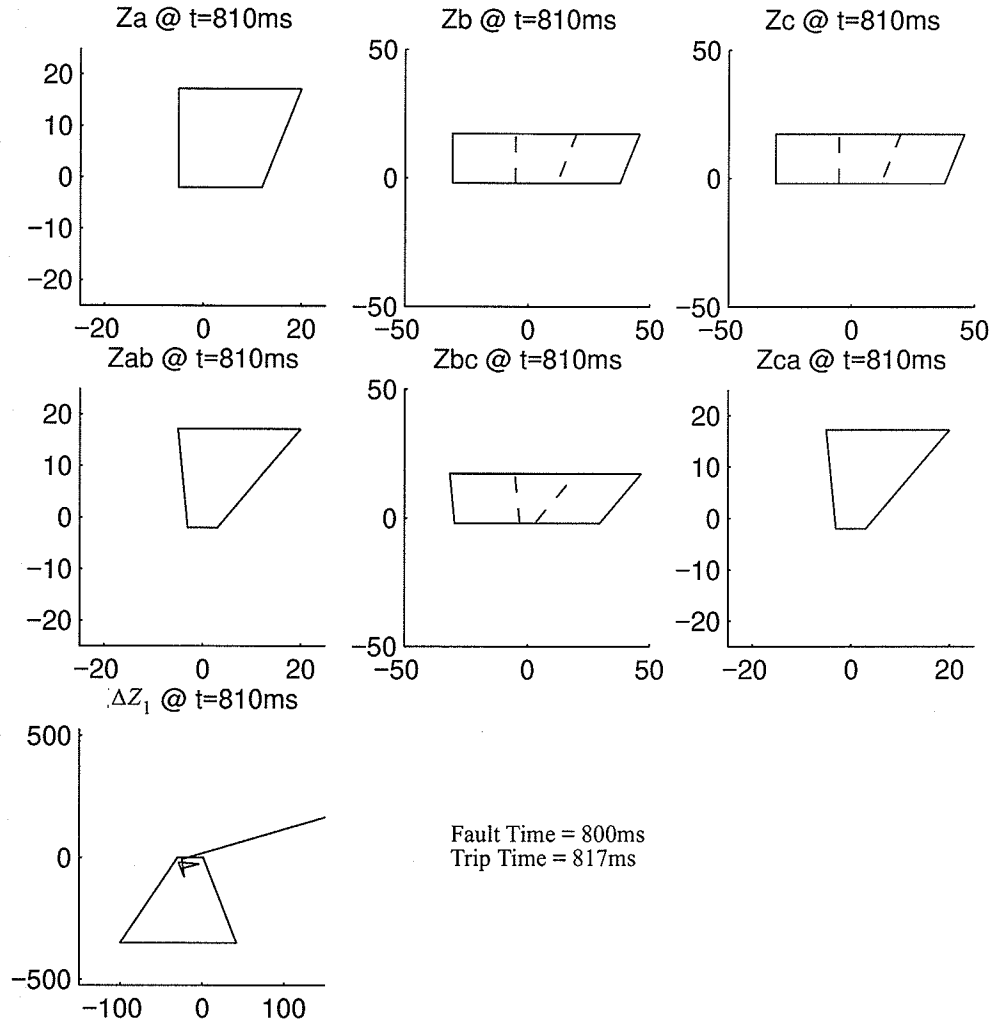


Figure 5.13. The Protection Zone in Mode 2 at a Forward BCG Fault.

Figure 5.14 is obtained when the PT relay operates in mode 2 and a forward ABC fault is applied to the system at 800ms. Since the relay identifies a forward fault and the PS element selects all phases as the faulted phases, the protection zones of the IE elements of all phases are expanded.

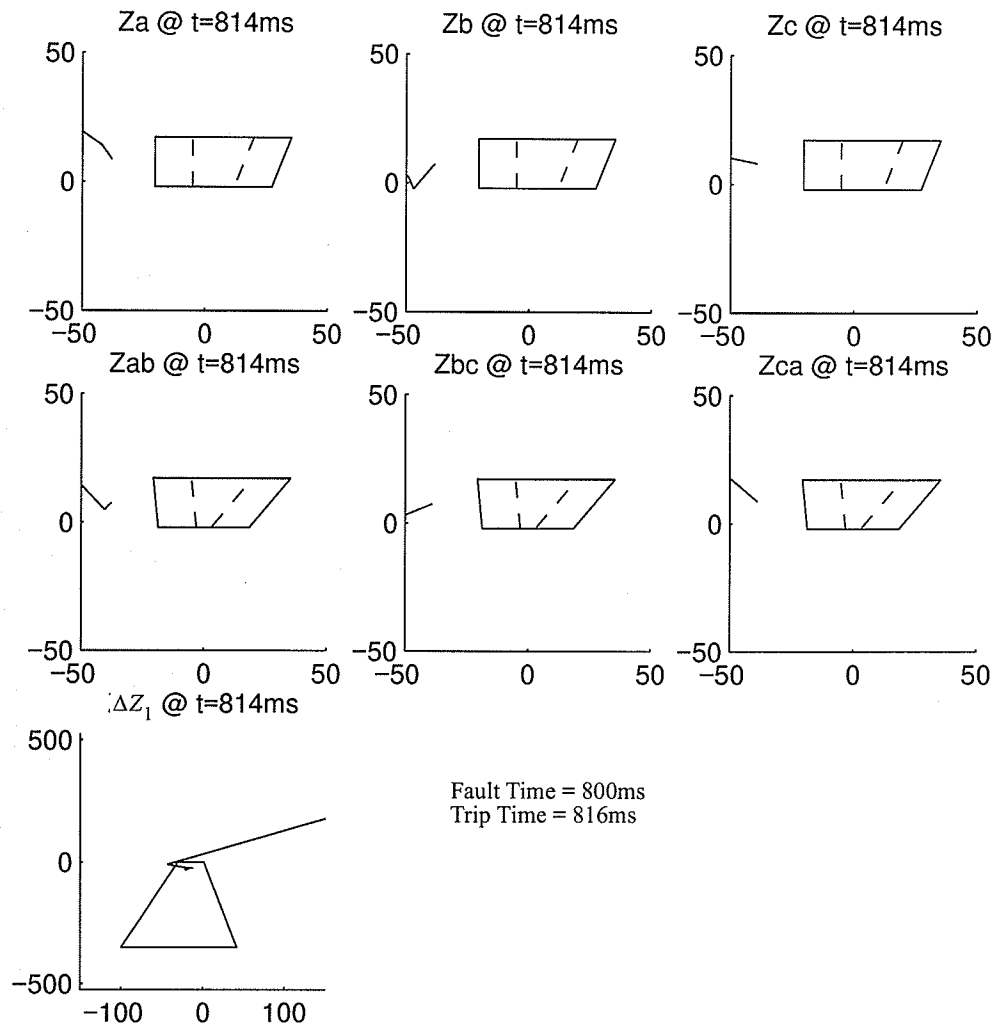


Figure 5.14. The Protection Zone in Mode 2 at a Forward ABC Fault.

5.4.4. The IE element in the reverse fault at mode 2

Figure 5.15 is obtained when the PT relay operates in mode 2 and a reverse AG fault is applied to the system at 800ms. Since the trajectory of ΔZ_1 locates outside the trip zone of the DE element and the relay identifies a reverse fault, modification of the protection zone does not occur.

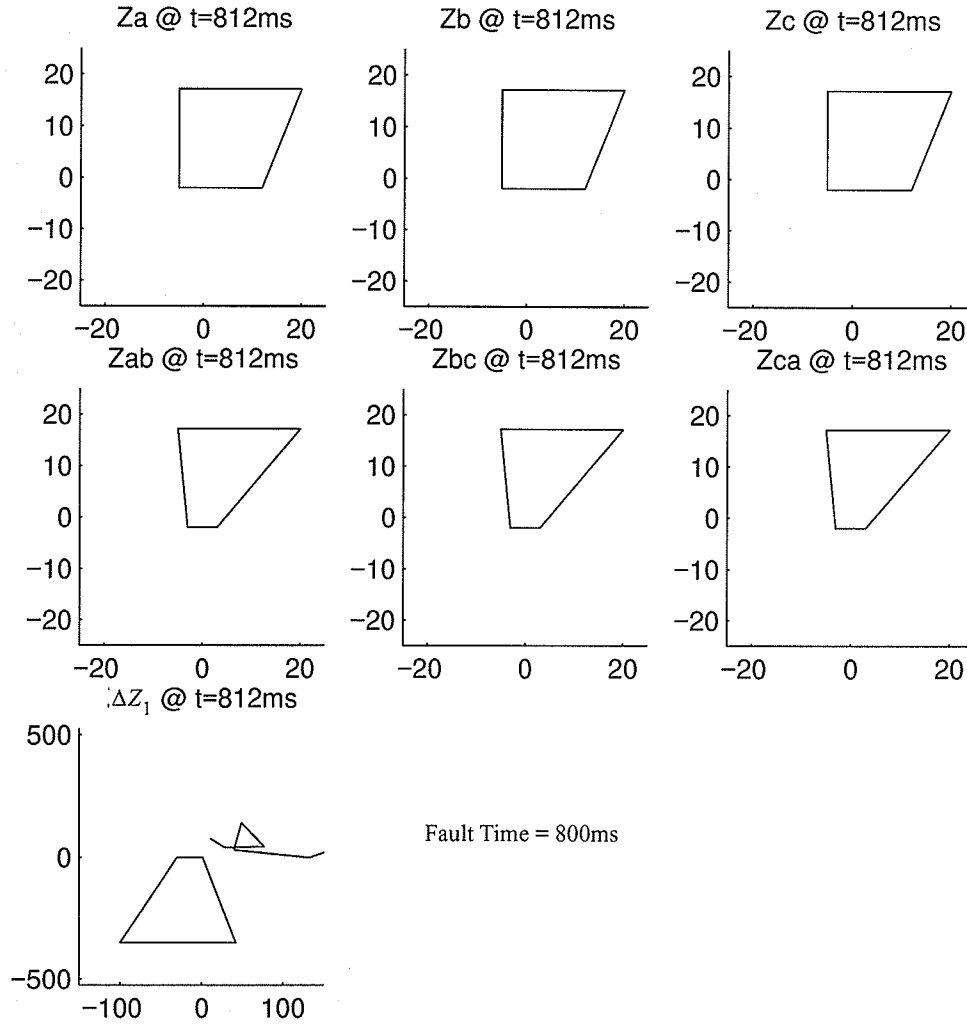


Figure 5.15. The Protection Zone in Mode 2 at a Reverse AG Fault.

5.5. Summary

The work in this chapter is mainly concentrated on verifying the modules of the PT relay using the PSCAD/EMTDC simulation. The verified models include the DI element, DE element, LI element, PS element, and IE element. The simulation proves that these models work as designed. The models of the DI element, DE element, and PS element, based on the incremental current or voltage, quickly responds during the fault, and can thus be used to control the adaptive protection zone.

Chapter 6. The Performance of the PT Relay

This chapter will compare the performance of the PT relay with that of the Mho relay. Several Mho relays are simulated. The Mho relay with the best performance is selected as the candidate. The performance of the PT relay is compared with that of the selected Mho relay.

6.1. The selection of the Mho relay

The inputs of the Mho relay are two phasors: $S1 = U_\phi - I_\phi Z_r$ and $S2 = c1U_{m\phi 1} + c2U_{c\phi} + c3U_\phi$. The operational criterion of a conventional Mho relay is $\pi/2 \leq \angle(S1/S2) \leq 3\pi/2$. The protection zone of the Mho relay, according to the discussion in chapter 2, is a circle which crosses Z_r and $-Z_{se}$ in a forward fault or crosses Z_r and Z_{se} in a reverse fault on the impedance plane during a three-phase fault(Section 2.2). Figure 6.1 illustrates such a scenario. Z_r is the reach of the relay, and $-Z_{se}$ or Z_{se} are associated with the coefficients in $S2$.

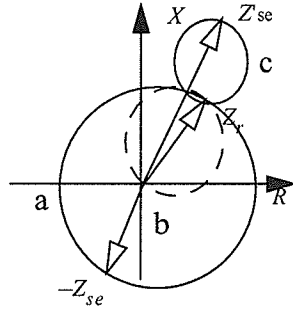


Figure 6.1. The Behaviour of the Mho Relay in the Three Phase Fault.

The behaviour of a Mho relay in an unbalanced fault is very complicated. We will employ PSCAD/EMTDC as the analysis tool to investigate its behaviour during the fault.

The performance of the Mho relay is closely associated with the composition of the phasor $S2$ in the fault. This association necessitates the investigation of the effects of the coefficients in the phasor $S2$. The investigation includes two parts. The first part concentrates on the effects of the memory positive sequence voltage on the performance of the Mho relay, and the second part focuses on the effects of the cross polarizing voltage on the performance of the Mho relay.

We use the power system in figure 6.2. to analyse the behaviour of the Mho relay in the fault.

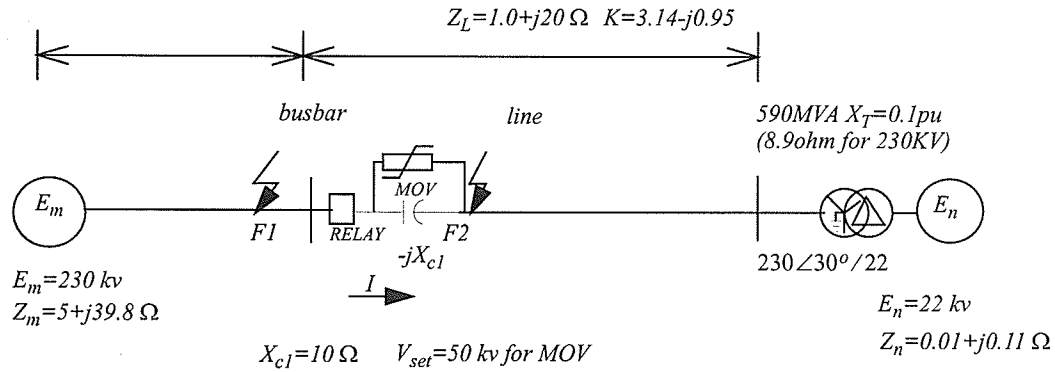


Figure 6.2. PSCAD/EMTDC Simulation System.

In normal case, the MOV conducts in the close fault and bring the measured impedance close to the line positive sequence impedance. The Mho relay can successfully handle this situation. However if the MOV fails in a fault, the Mho characteristic is seriously challenged. The simulation in this section will investigate the Mho relay performance in such a situation.

6.1.1. The effect of the memory voltage on the Mho relay

The presence of the memory positive sequence voltage and cross polarizing voltage in $S2$ can prevent the Mho relay from losing its reference voltage during a close-up fault.

6.1.1.1. In a three phase fault

In this part of the simulation, a three-phase fault is applied to the system at $F2$ at 0.8045 seconds. The MOV is kept out of the circuit during the fault. The power sources in the system are the ideal voltage sources, $E_m = 220 \angle 0^\circ \text{KV}$ and $E_n = 24 \angle 0^\circ \text{KV}$. The source at the left hand side of the system absorbs real power because the Y/Δ transformer shifts the voltage 30° ahead.

The performance of the Mho relays is observed when the ratio $c3/c1$ is adjusted and the coefficient $c2$ is zero.

The protection zone of the Mho relay shrinks in a forward fault when the reduction of $c1$ makes Z_{se} move to the origin.

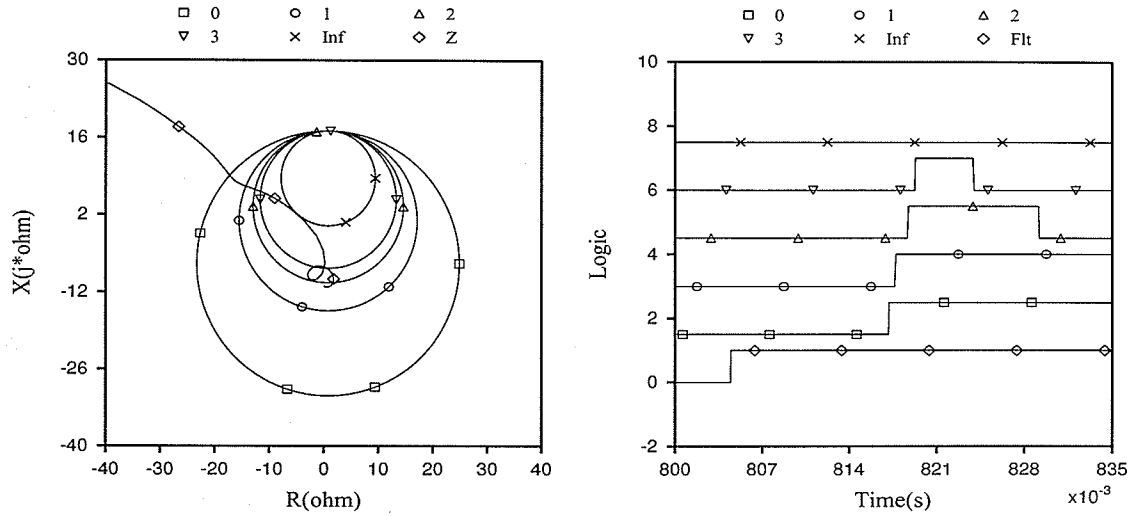


Figure 6.3. The Effect of the Memory Polarizing Voltage on the Mho in a Forward ABC Fault.

Figure 6.3 shows the PSCAD/EMTDC simulation result for the performance of several Mho relays when a three-phase fault occurs at point F2. In the simulation case, the capacitor is in the system and the MOV is not active during the fault. The Mho relay samples the voltage at the bus bar. The figure consists of two sub-figures. The numbers along with the marks that identify the curves are the ratios $c3/c1$. The left sub-figure demonstrates the protection zone of the Mho relays during faults and the impedance trajectory measured by the phase A element. The right sub-figure shows the trip logic of those Mho relays. The rising edge of curve “Flt” is the moment when the faults occur.

In these forward faults, the Mho relay is expected to trip. However, the relay gradually fails to trip when the ratio $c3/c1$ increases. Reducing the weight of memory positive sequence voltage ($s2 = c1U_{m\phi1} + c2U_{c\phi} + c3U_{\phi}$) in $s2$ gradually reduces the protection zone of the Mho relay as shown in figure 6.3.

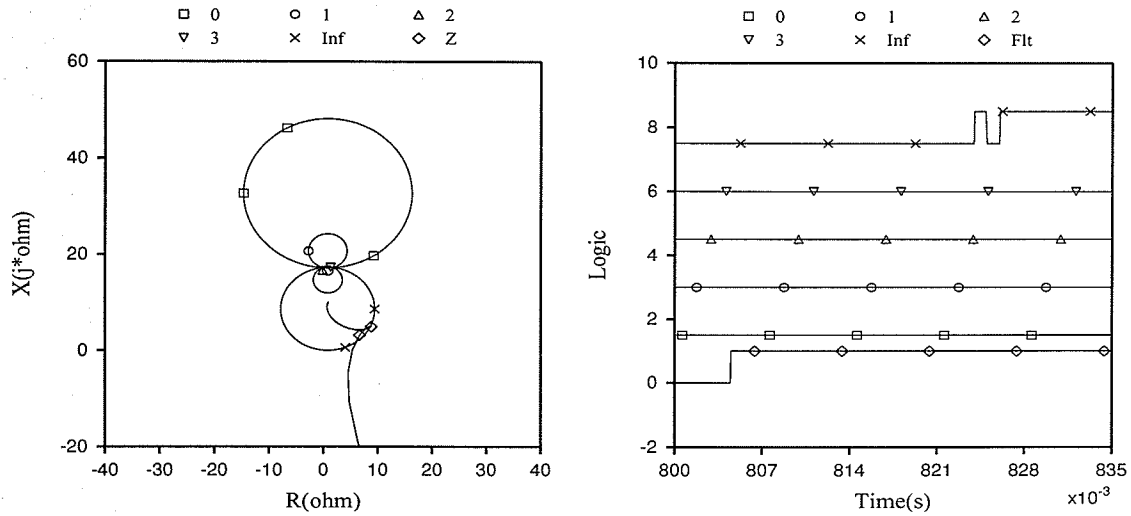


Figure 6.4. The Effect of the Memory Polarizing Voltage on the Mho in a Reverse ABC Fault.

When the relay samples the line side voltage of the capacitor, a fault on the busbar is a reverse fault for the relay. Such a fault is used to investigate the performance of the Mho relay in a reverse fault. Figure 6.4 shows the simulation results of the performance of several Mho relays when a three-phase reverse fault happens in the system.

For a reverse fault, the relays are expected to remain stable, however they trip when the ratio $c3/c1$ increases. Decreasing the weight of the memory voltage in $s2$ is the primary factor that deteriorates the performance of the Mho relay in the reverse three-phase fault.

6.1.1.2. In the phase A fault

In order to observe the effect of the memory positive sequence voltage on the performance of the Mho relay, two AG cases are simulated in this section. Figure 6.5 presents the protection zone, the impedance trajectory, and the trip logic in a forward AG fault when the series capacitor is switched into the circuit and the MOV is not active during the forward AG fault. The Mho relay samples the voltage at the busbar. Figure 6.5 shows that the relay fails when the ratio $c3/c1$ increases.

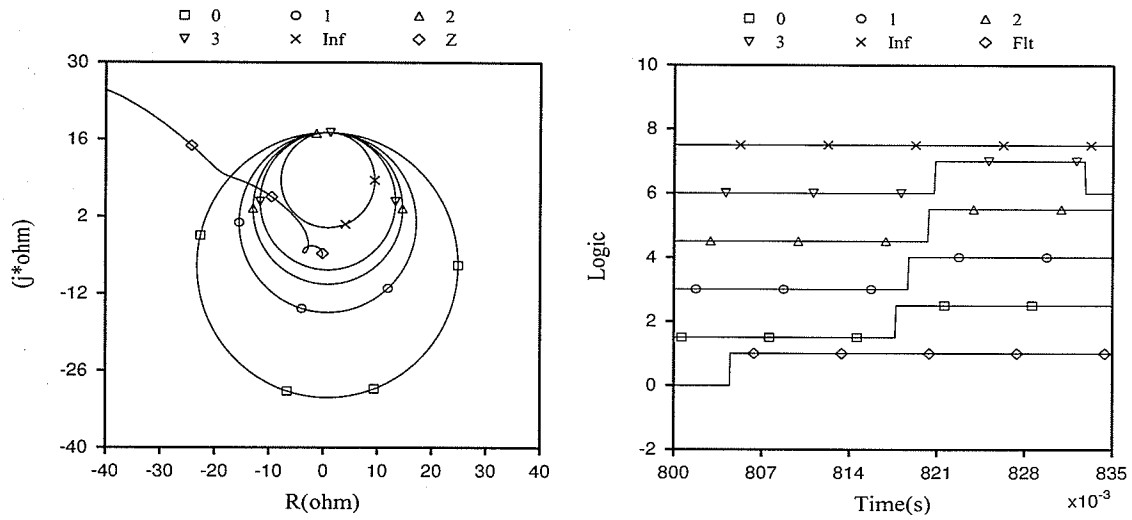


Figure 6.5. The Effect of the Memory Polarizing Voltage on the Mho in a Forward AG Fault.

When the relay samples the line side voltage of the capacitor, a fault on the busbar is a reverse fault for the relay. Such a fault is used to investigate the performance of the Mho relay in a reverse fault. Figure 6.6 demonstrates such a reverse fault case. The series compensation capacitor is switched into the circuit and the MOV is not active during the fault. Figure 6.6 shows that the relay tends to misoperate in the reverse fault as the ratio $c3/c1$ increases.

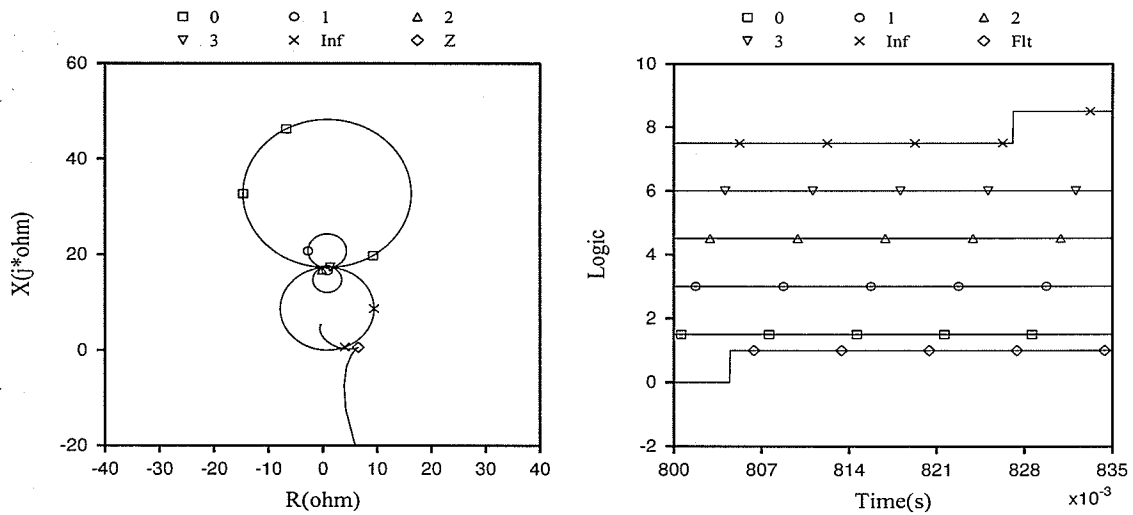


Figure 6.6. The Effect of Memory Polarizing Voltage on the Mho in a Reverse AG Fault.

6.1.2. The effect of the cross polarizing voltage on the Mho relay

6.1.2.1. In the three phase fault

In this part of the simulation, the effect of the cross polarizing voltage for the performance of the Mho relay is investigated. The system condition is identical to the previous section.

The coefficient c_3 is set to zero in order to isolate the effect of the cross polarizing voltage. At the same time, the value of the ratio c_2/c_1 is adjusted and the trip signals of the Mho relay and the measured impedance trajectory for phase A are recorded for the comparison.

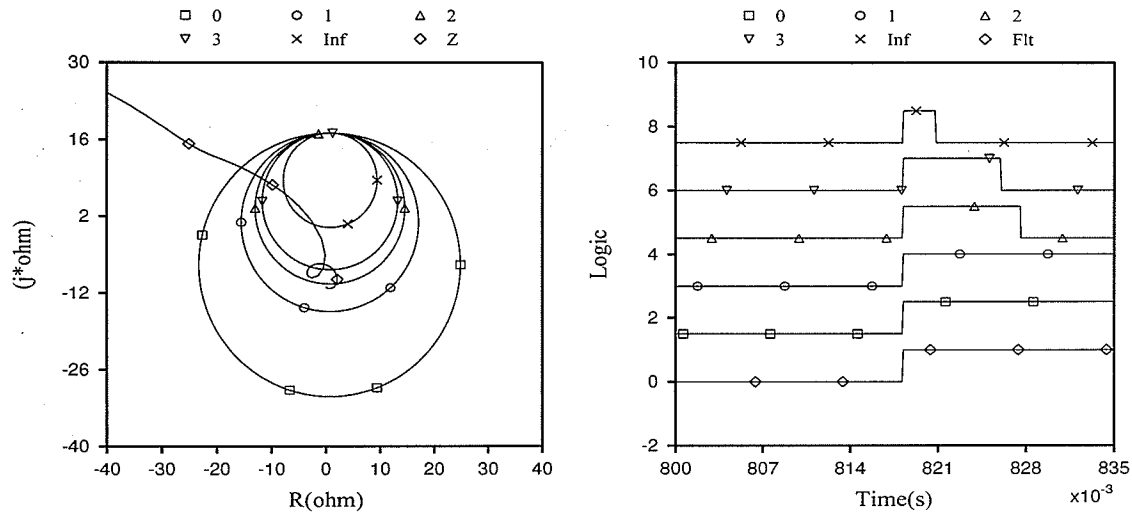


Figure 6.7. The Effect of the Cross Polarizing Voltage on the Mho in a Forward ABC Fault.

The information in figure 6.7 reflects the Mho relay behaviour for a forward ABC fault at F2 and the series capacitor is switched into the circuit, MOV is not conducting, and the relay samples the voltages at the busbar. The number behind the identity marks has the value of the ratio c_2/c_1 . The relay tends to fail in the fault when the ratio c_2/c_1 increases.

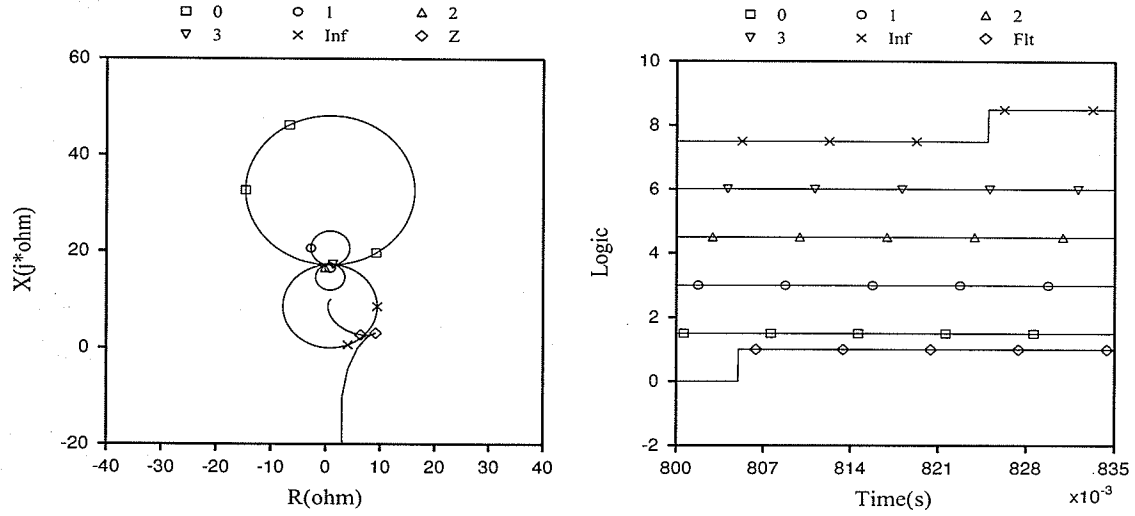


Figure 6.8. The Effect of the Cross Polarizing Voltage on the Mho in a Reverse ABC Fault.

When the relay samples the line side voltage of the capacitor, a fault on the busbar is a reverse fault for the relay. Such a fault is used to investigate the performance of the Mho relay in a reverse fault. The information in figure 6.8 reflects the Mho relay behaviour in a reverse ABC fault at point F1 and the series capacitor is in the circuit, the MOV is not active, and the relay samples the voltages at the line side of the capacitor. The number behind the identity marks is the value of the ratio $c2/c1$ ($S2 = c1U_{m\phi1} + c2U_{c\phi} + c3U_{\phi}$). The relay tends to misoperate in the fault when the ratio $c2/c1$ increases.

6.1.2.2. In the phase A fault

In this part of the simulation, the effect of cross polarizing voltage on the performance of the Mho relay is observed. An AG fault is applied to the system.

The coefficient $c1$ is set to zero in order to isolate the effect of the cross polarizing voltage. At the same time, the value of the ratio $c3/c2$ is adjusted, and the trip signals of the Mho relay and the measured impedance trajectory of phase A are recorded for the purpose of comparison.

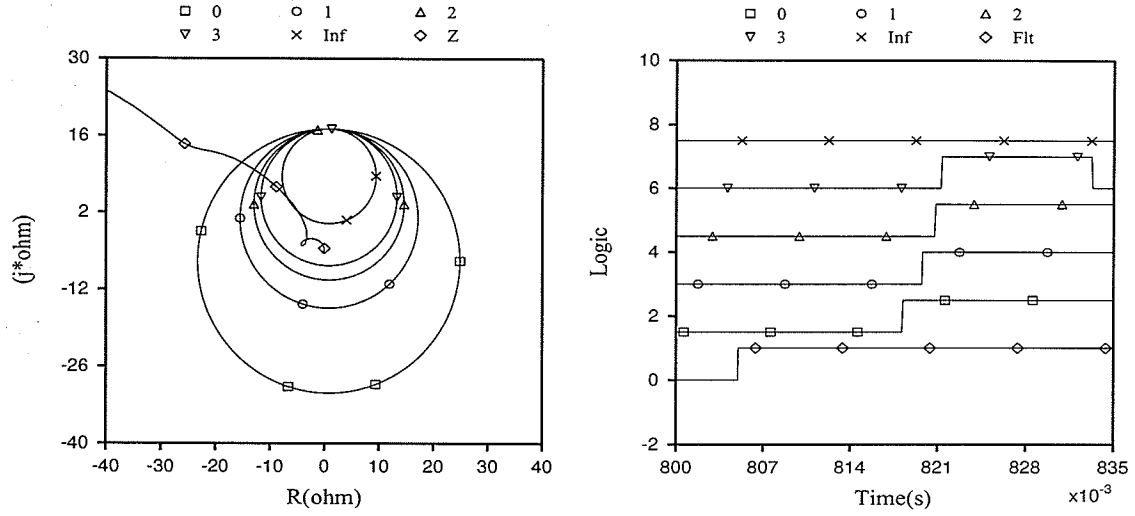


Figure 6.9. The Effect of the Cross Polarizing Voltage on the Mho in a Forward AG Fault.

Figure 6.9 shows the PSCAD/EMTDC simulation result for the performance of the Mho relay acquired by varying the ratio c_3/c_2 . In this case, a forward AG fault occurs ahead of the capacitor and the MOV is not active during the fault. The Mho relay samples the voltage at the busbar. In order to research the effect of the cross polarizing voltage on the Mho relay, coefficient c_1 is set to zero. When the ratio c_3/c_2 ($S_2 = c_1 U_{m\phi 1} + c_2 U_{c\phi} + c_3 U_{\phi}$) increases, the trip zone of the relay shrinks so that the response of the Mho relay to the fault slows down and the Mho relay finally fails to trip at the moment that the ratio c_3/c_2 reaches infinity ($c_2 = 0$). In such a case, the measured impedance is about $-j10\text{ohm}$, when the ratio c_3/c_2 is infinity, and the trip circle passes through the origin and its reach point. This trip circle excludes this impedance, $-j10\text{ohm}$, so the relay fails.

When the relay samples the line side voltage of the capacitor, a fault on the busbar is a reverse fault for the relay. Such a fault is used to investigate the performance of the Mho relay in a reverse fault. Figure 6.10 shows the performance of the Mho relay acquired by varying the ratio c_3/c_2 . In this case, a reverse AG fault occurs at the busbar with the series capacitor switched into the system and the MOV not active during the fault. The Mho relay samples the voltage at the line side of the capacitor. Such a fault is a reverse fault for the relay. As the ratio c_3/c_2 ($S_2 = c_1 U_{m\phi 1} + c_2 U_{c\phi} + c_3 U_{\phi}$) increases to infinity, the relay tends to misoperate in the reverse fault. In such a case, the measured impedance is about $j10\text{ohm}$, when the ratio c_3/c_2 is infinity ($c_2 = 0$), the trip circle passes through the origin and its reach point. This trip circle includes

the impedance, $j10\text{ohm}$, so the relay misoperates.

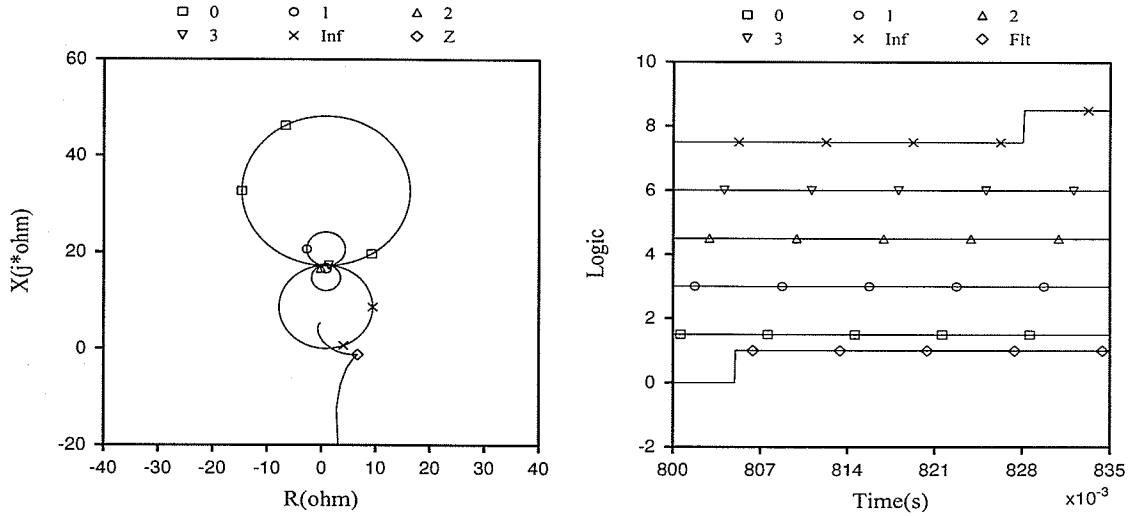


Figure 6.10. The Effect of the Cross Polarizing Voltage on the Mho in a Reverse AG Fault.

The conclusion from the simulation is that:

- (1) The cross polarizing voltage influences the Mho in the same way that memory polarizing voltage does in an unbalanced fault, and the same way as phase voltage does in a balanced fault.
- (2) The memory polarizing Mho ($c_3 = c_2 = 0$) has the maximum protection zone coverage in the forward fault and better performance for the reverse fault than other Mho relays.

Therefore a memory polarizing Mho ($S_2 = c_1 U_{m\phi 1}$) is selected as the counterpart of the PT relay. Their performance is compared in the rest of this chapter.

6.2. The mode-1 PT relay vs the Mho relay

In the previous section, the memory polarizing Mho relay was proven to have the best performance among the Mho relays during the fault. In an effort to evaluate the relay, the performance of the PT relay is compared with the performance of the memory polarized Mho relay. The observed cases include the full combination of system configurations and fault type.

The system in figure 6.2 is the simulation system. The PT relay operates in mode 1. The behaviour of the PT relay and the memory polarized Mho relay will be presented together to demon-

strate their difference during the faults. In order to exhibit the dynamics of the PT relay's trip characteristics, the MATLAB relay model was used. The simulation will test the relay in all fault types and system configurations.

6.2.1. The system with capacitor switched out

In this section, the series capacitor is not switched in the system during the simulation. The fault point is set close to the location of the relays in either the forward fault or the reverse fault, and the fault is applied to the system at 804ms. Several cases are included to investigate the performance of the PT relay and the Mho relay. Each case is represented by a figure which assembles the behaviours of the six IE elements, and DI element, and the three phase voltages, the three phase currents, and trip logic for both the PT and Mho relays in the fault.

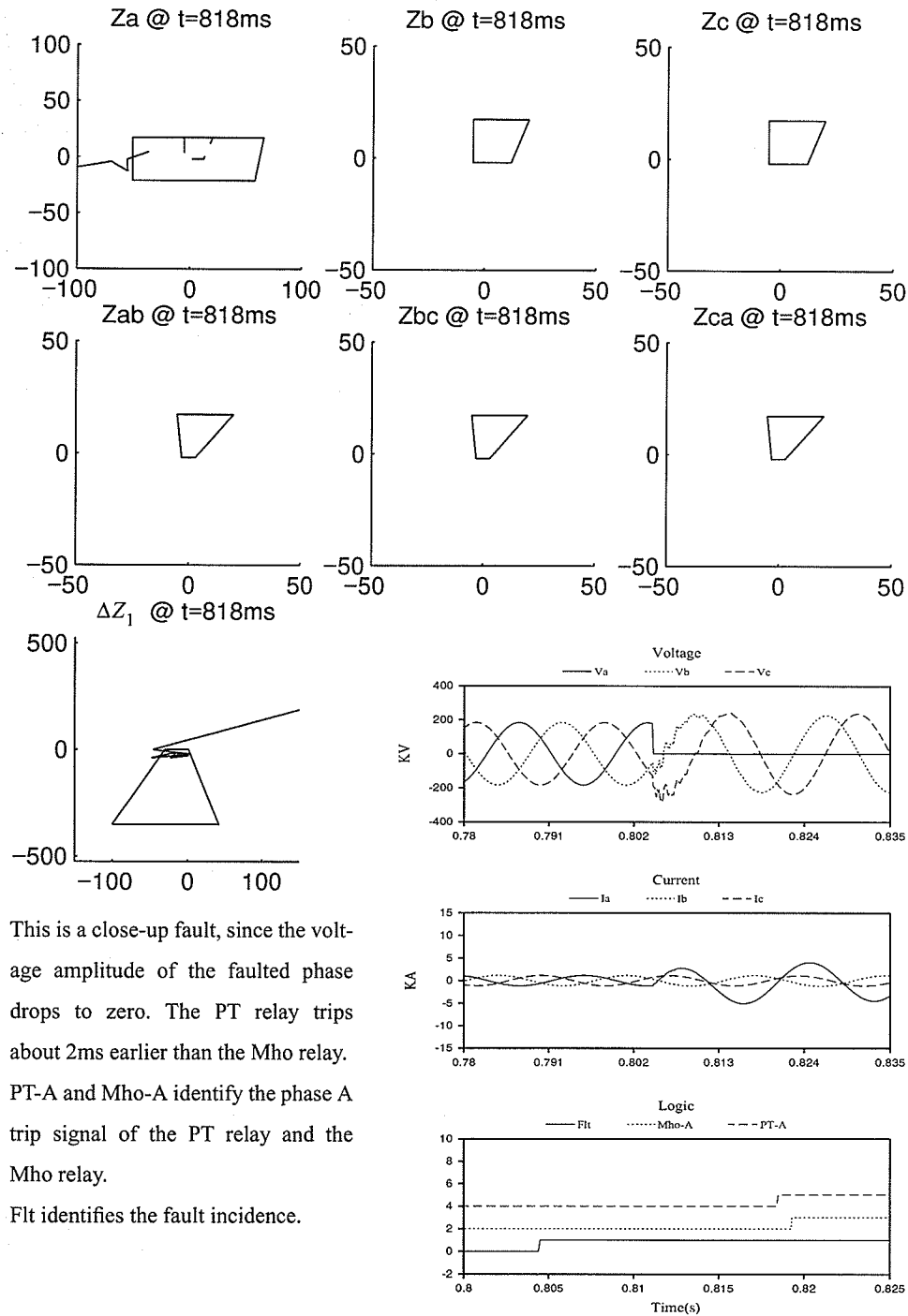
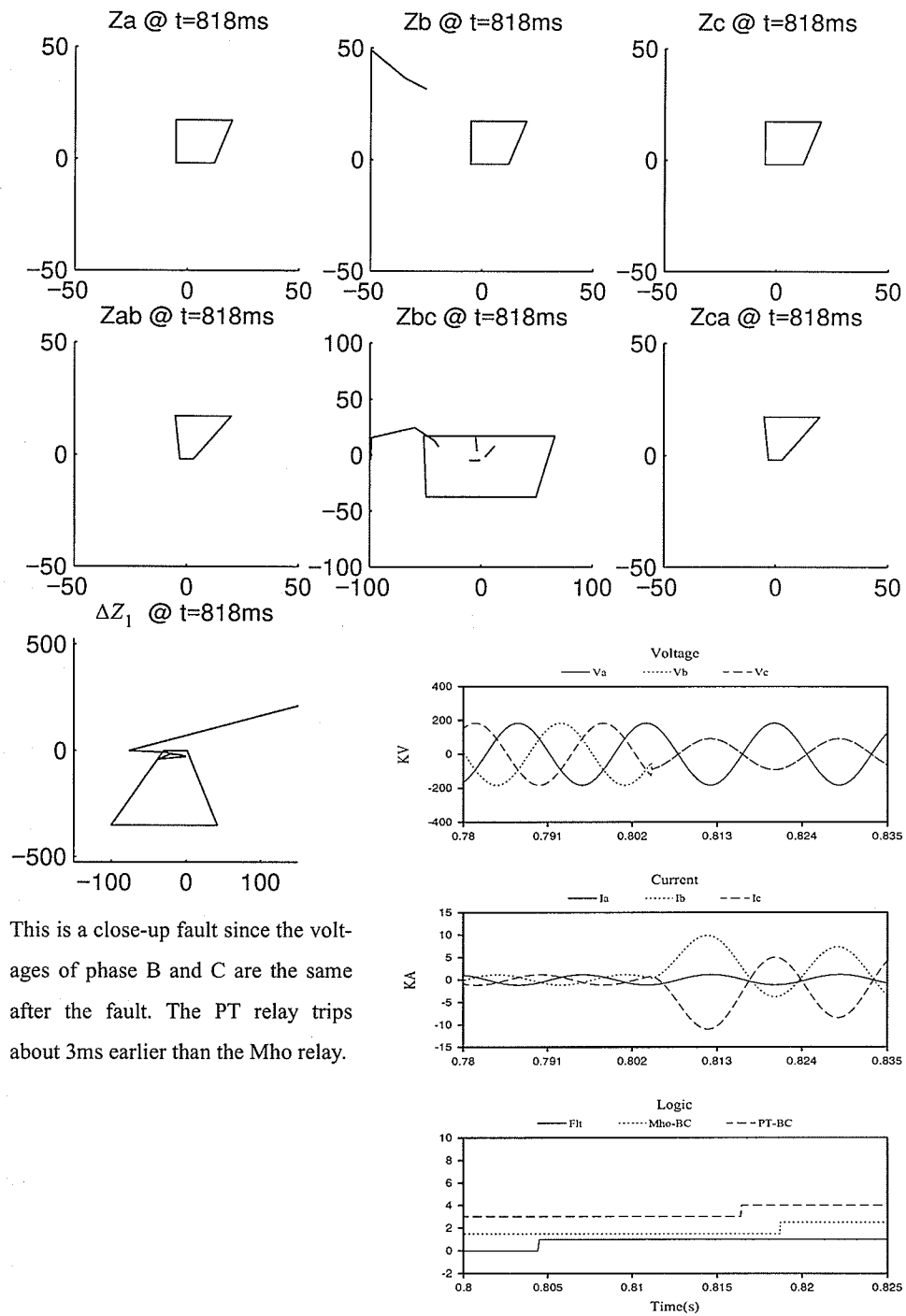
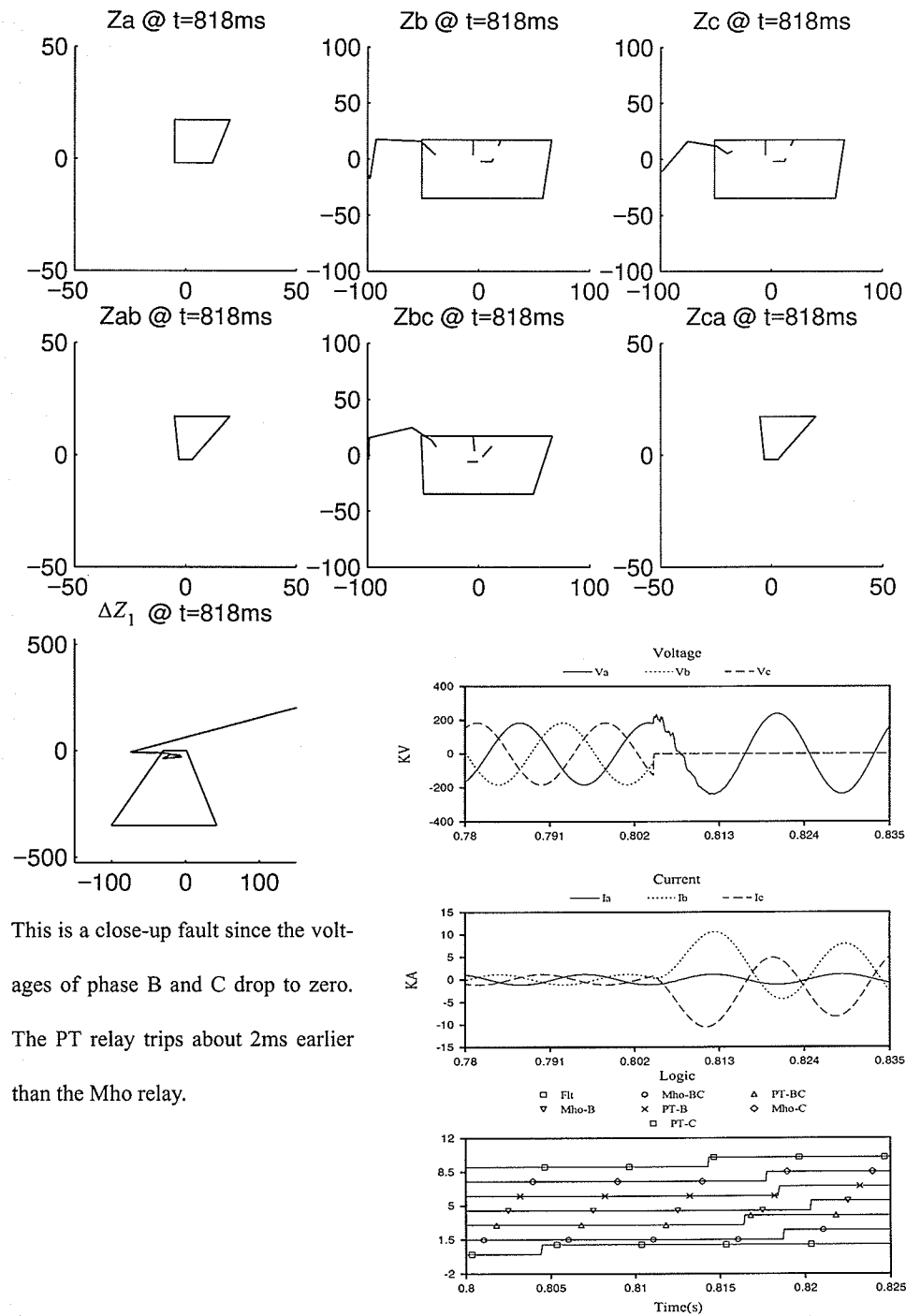


Figure 6.11. The Relays' Behaviour in a Forward AG Fault with Capacitor Switched out.



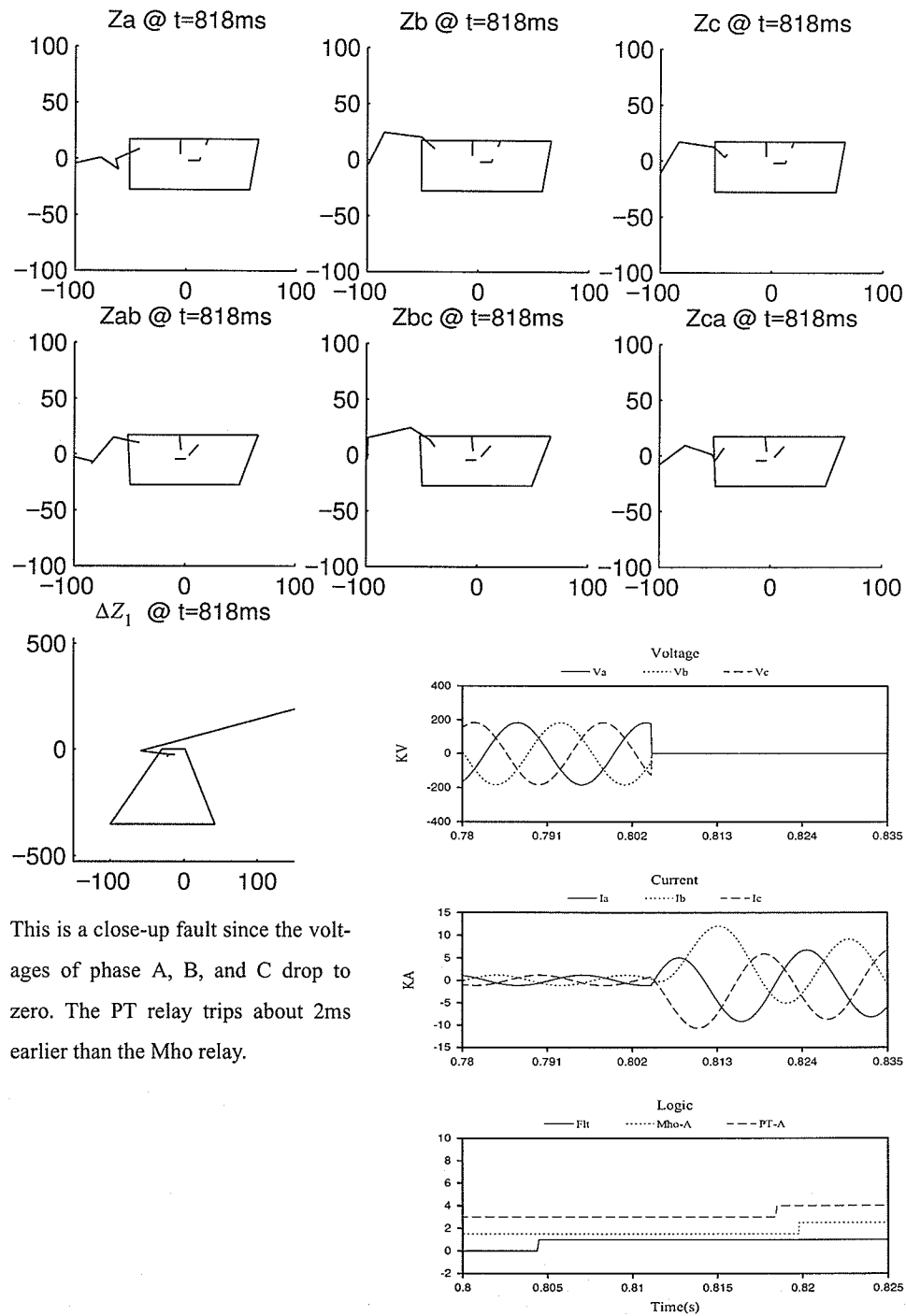
This is a close-up fault since the voltages of phase B and C are the same after the fault. The PT relay trips about 3ms earlier than the Mho relay.

Figure 6.12. The Relays' Behaviour in a Forward BC Fault with Capacitor Switched out.



This is a close-up fault since the voltages of phase B and C drop to zero. The PT relay trips about 2ms earlier than the Mho relay.

Figure 6.13. The Relays' Behaviour in a Forward BCG Fault with Capacitor Switched out.



This is a close-up fault since the voltages of phase A, B, and C drop to zero. The PT relay trips about 2ms earlier than the Mho relay.

Figure 6.14. The Relays' Behaviour in a Forward ABC Fault with Capacitor Switched out.

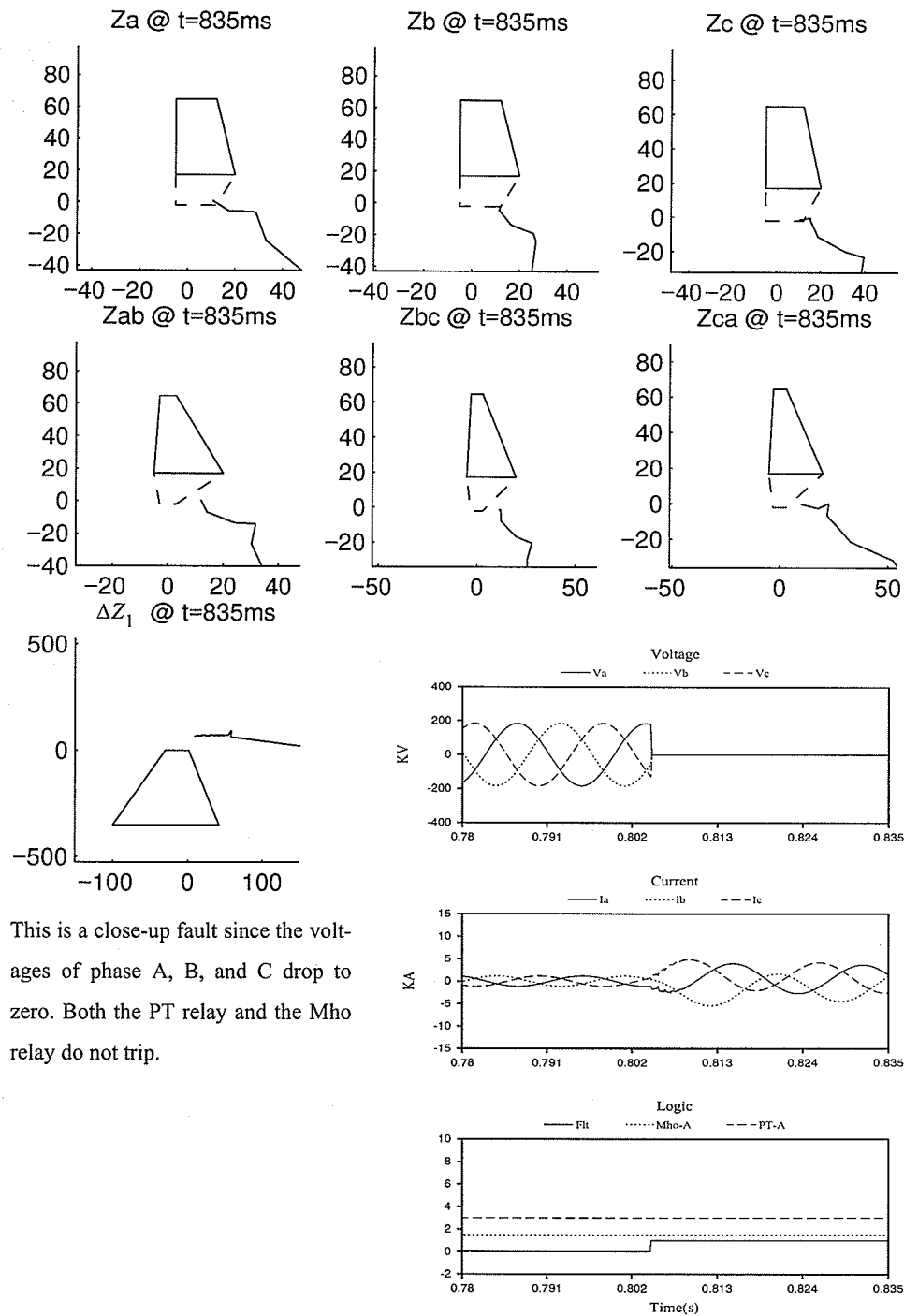


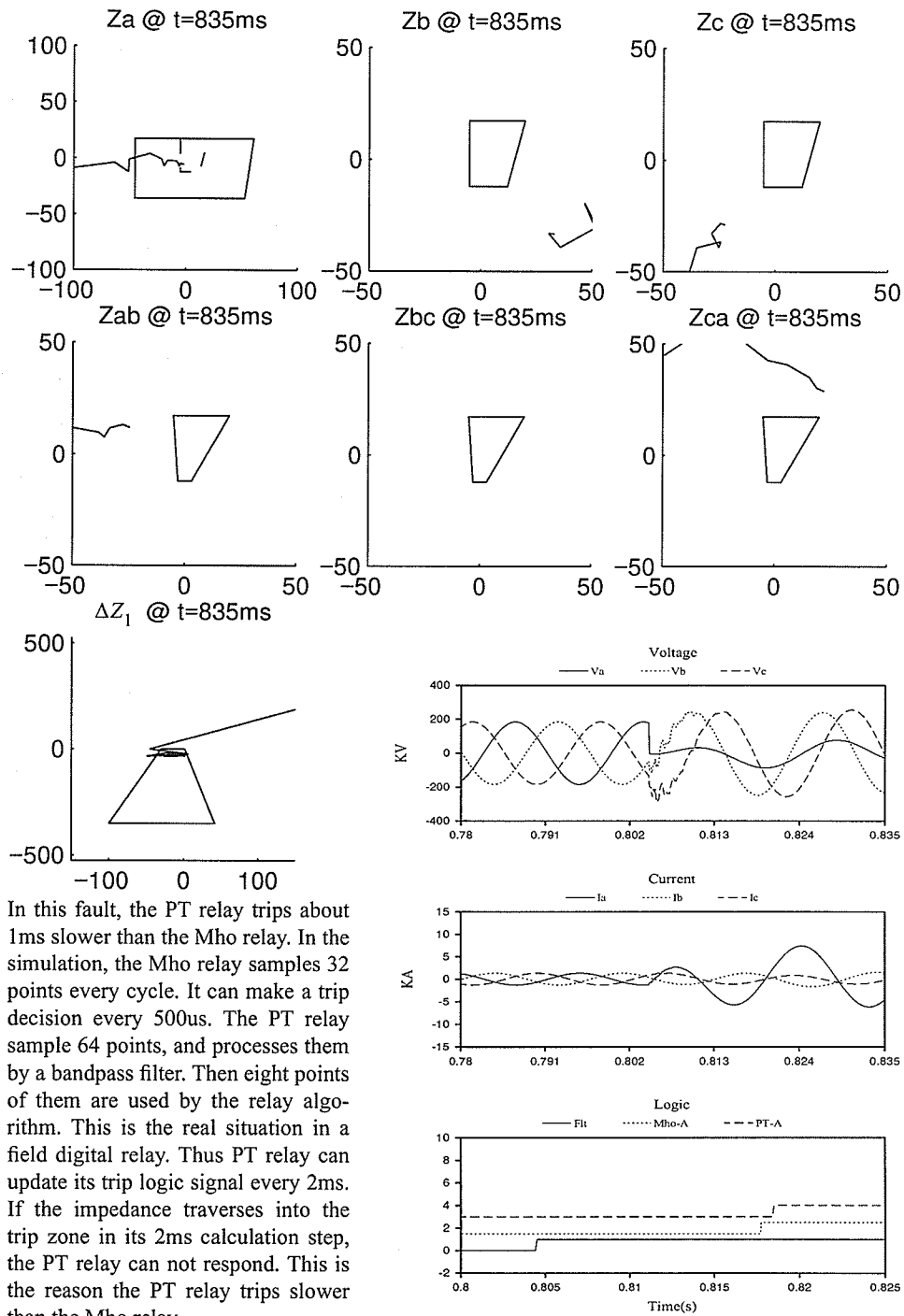
Figure 6.15. The Relays' Behaviour In a Reverse ABC Fault with Capacitor Switched out.

In the simulation cases of this section, the PT relay demonstrates a slight advantage in reaction time over the Mho relay during a forward fault. Since the PT relay has the same trip zone in reverse fault, only one reverse fault case is presented even though the PT relay was tested for all

reverse fault types. Both relays respond correctly in the reverse fault.

6.2.2. The system with capacitor switched in and MOV not active

In this section, the series capacitor is in the system circuit during the simulation and MOV is kept not conducting in the fault. The relays sample the voltage at the busbar. The fault point is set close-up to the line side of the series compensation capacitor in the forward faults. The faults are applied to the system at 804ms. Several cases are included to investigate the performance of the PT and Mho relays.



In this fault, the PT relay trips about 1ms slower than the Mho relay. In the simulation, the Mho relay samples 32 points every cycle. It can make a trip decision every 500 μs . The PT relay sample 64 points, and processes them by a bandpass filter. Then eight points of them are used by the relay algorithm. This is the real situation in a field digital relay. Thus PT relay can update its trip logic signal every 2ms. If the impedance traverses into the trip zone in its 2ms calculation step, the PT relay can not respond. This is the reason the PT relay trips slower than the Mho relay.

Figure 6.16. The Relays' Behaviour in a Forward AG Fault with the Capacitor Switched in.

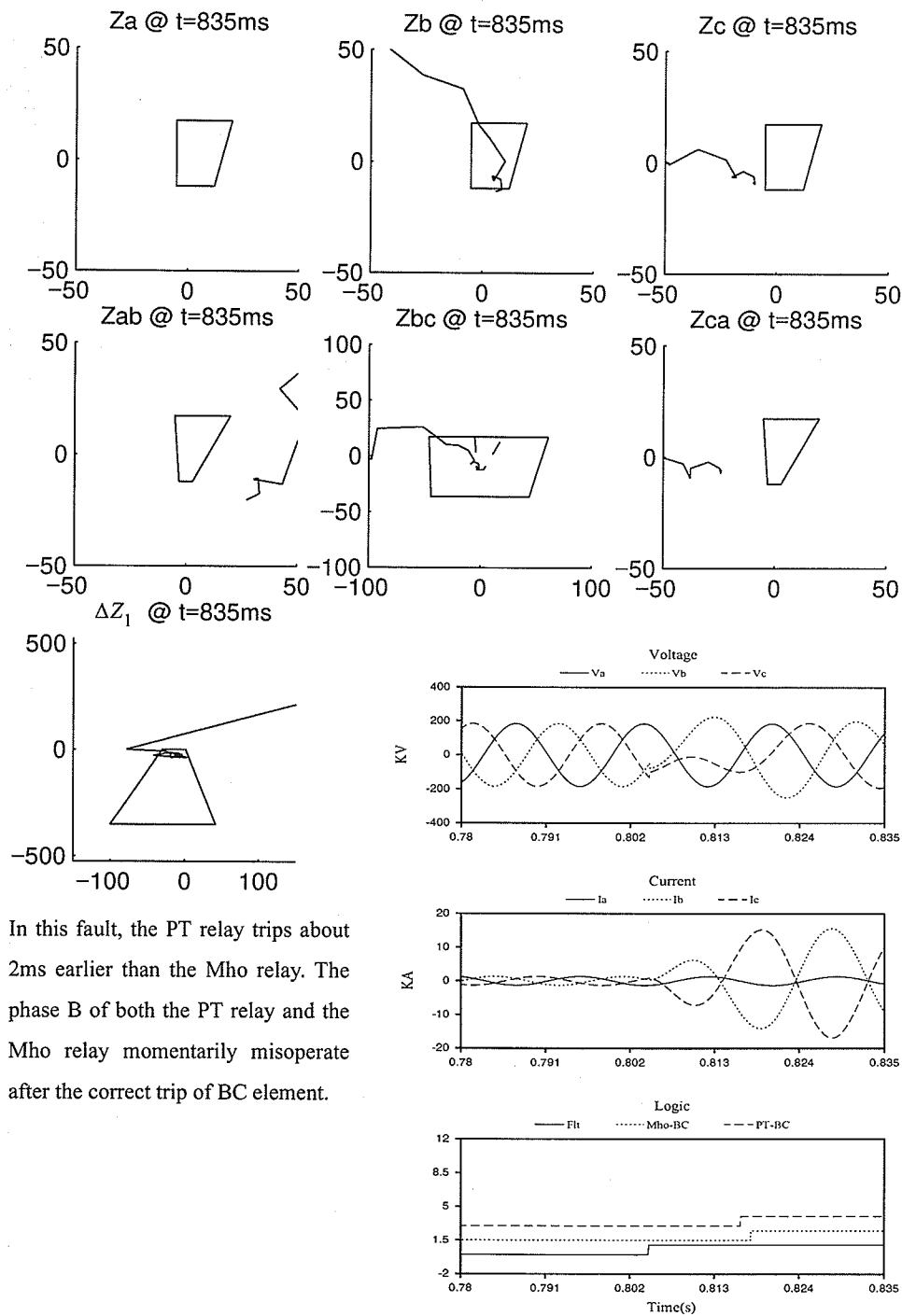
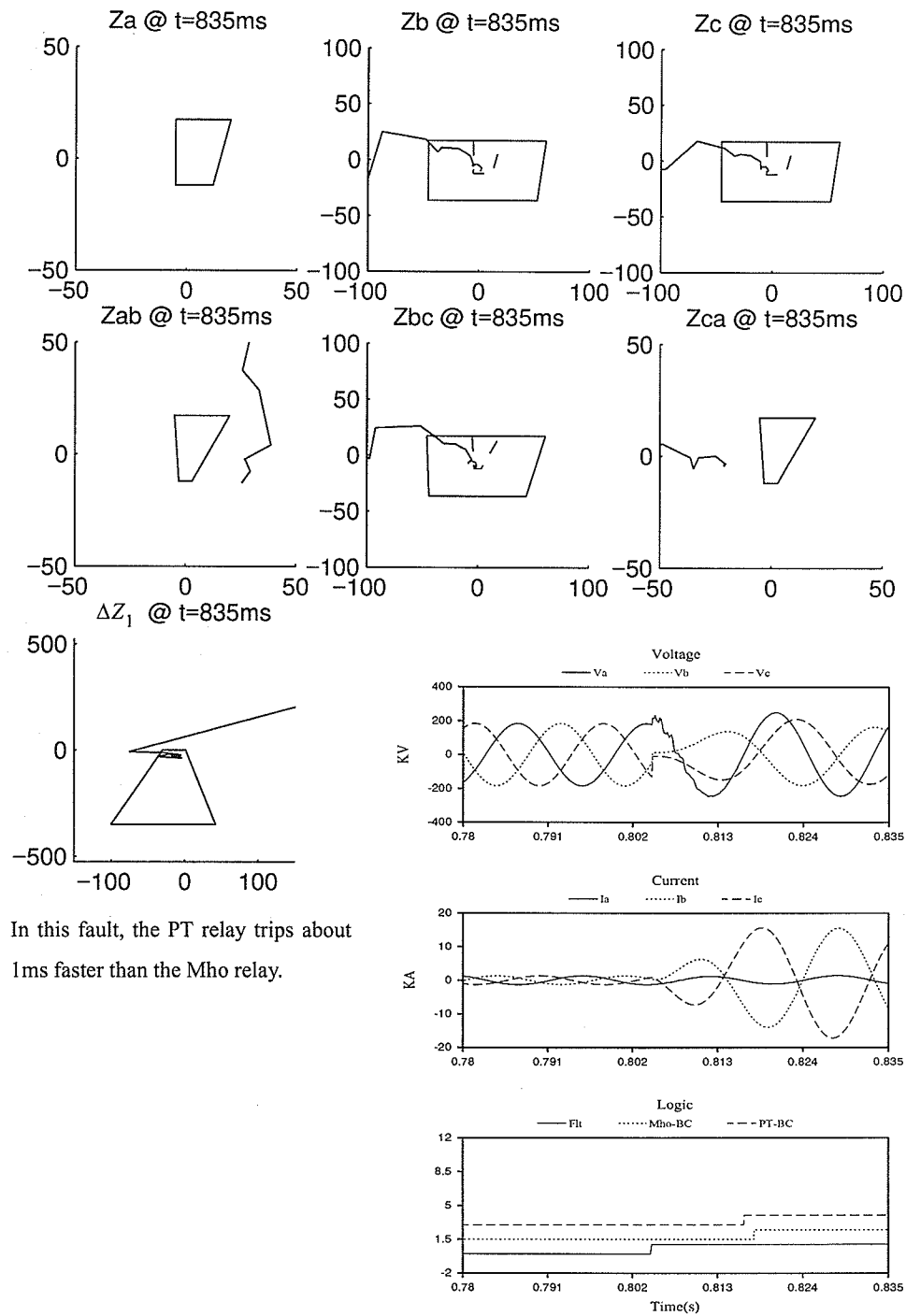
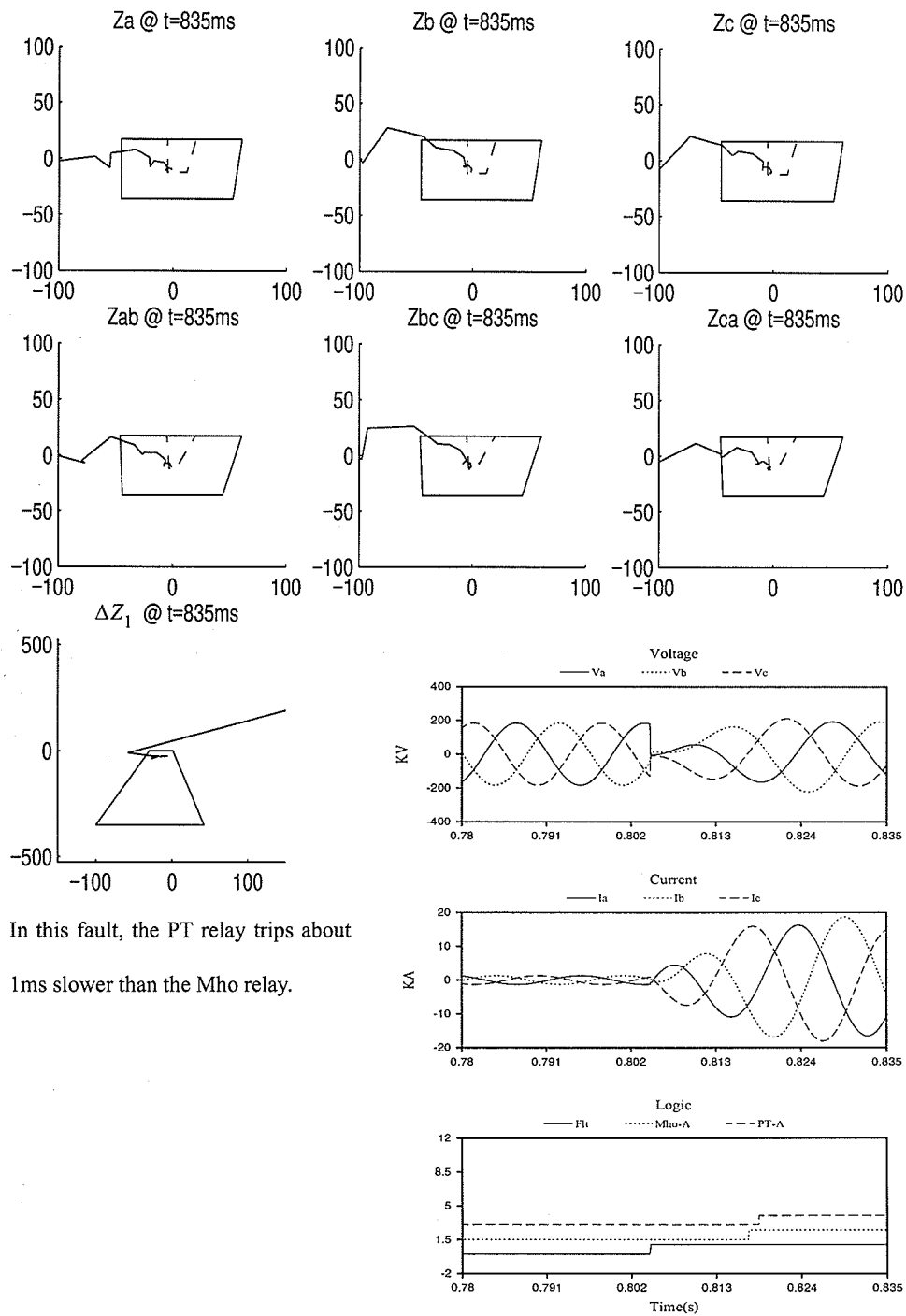


Figure 6.17. The Relays' Behaviour in a Forward BC Fault with the Capacitor Switched in.



In this fault, the PT relay trips about 1ms faster than the Mho relay.

Figure 6.18. The Relays' Behaviour in a Forward BCG Fault with the Capacitor Switched in.



In this fault, the PT relay trips about 1ms slower than the Mho relay.

Figure 6.19. The Relays' Behaviour in a Forward ABC Fault with the Capacitor Switched in.

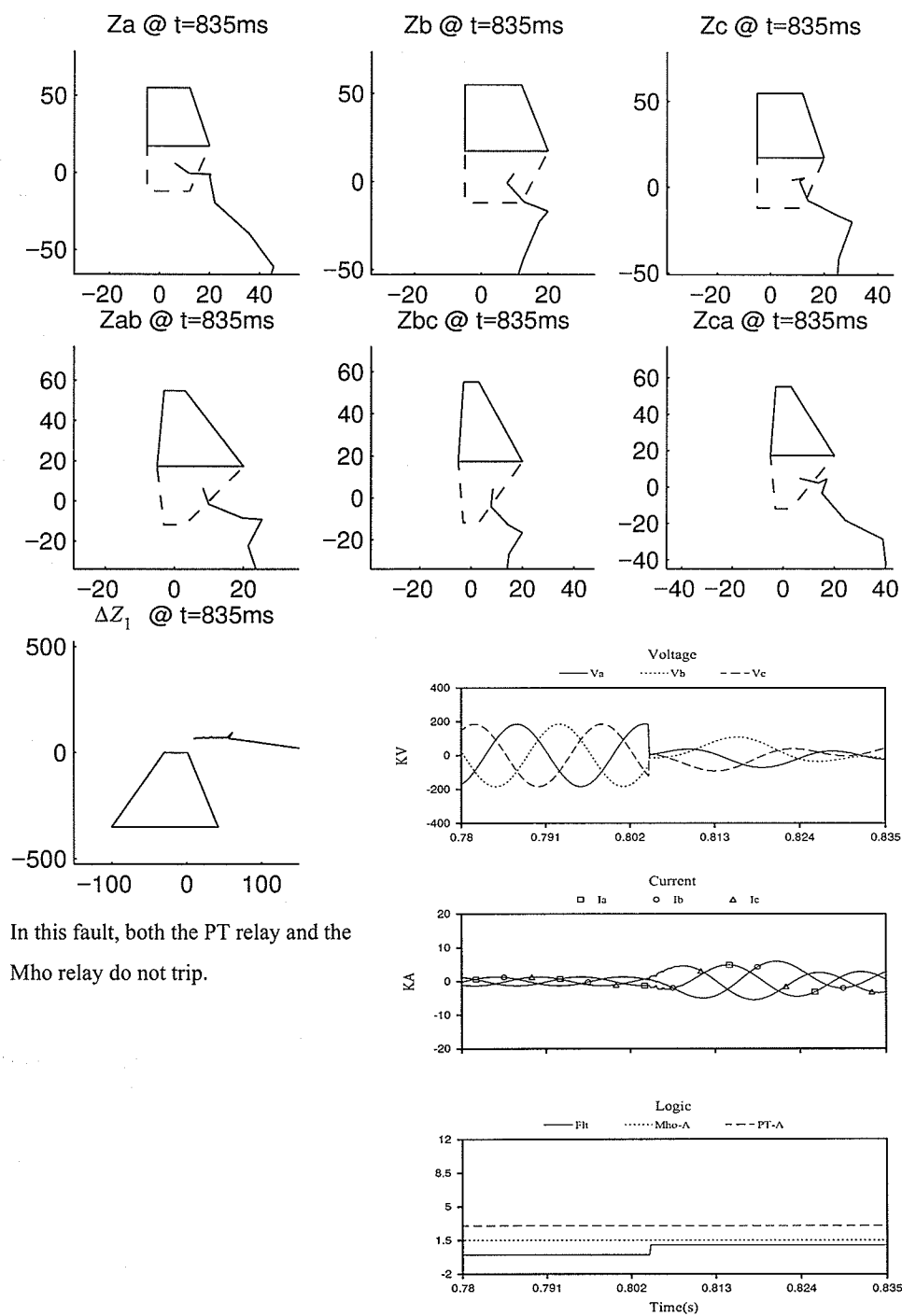
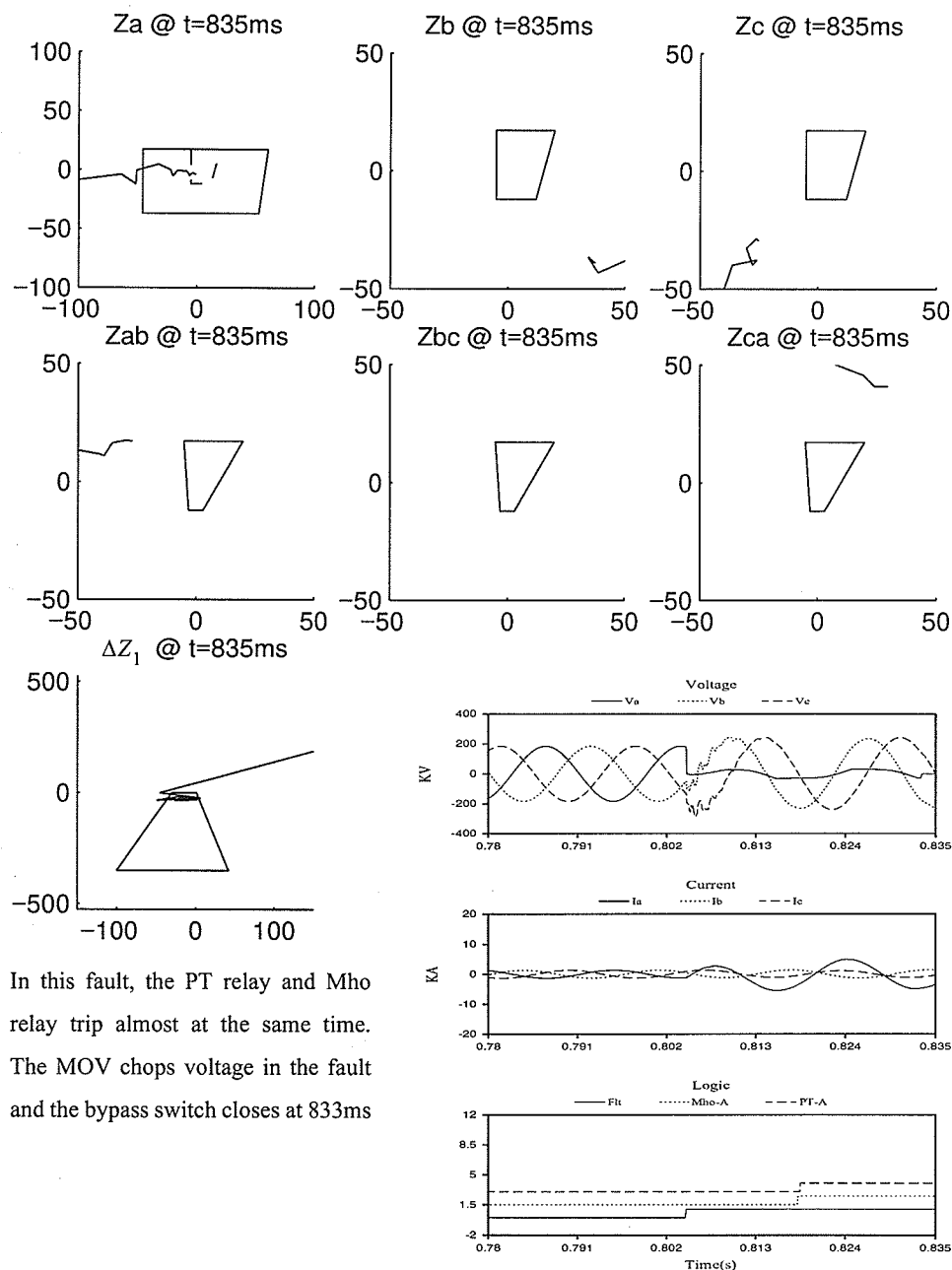


Figure 6.20. The Relays' Behaviour in a Reverse ABC Fault with the Capacitor Switched in.

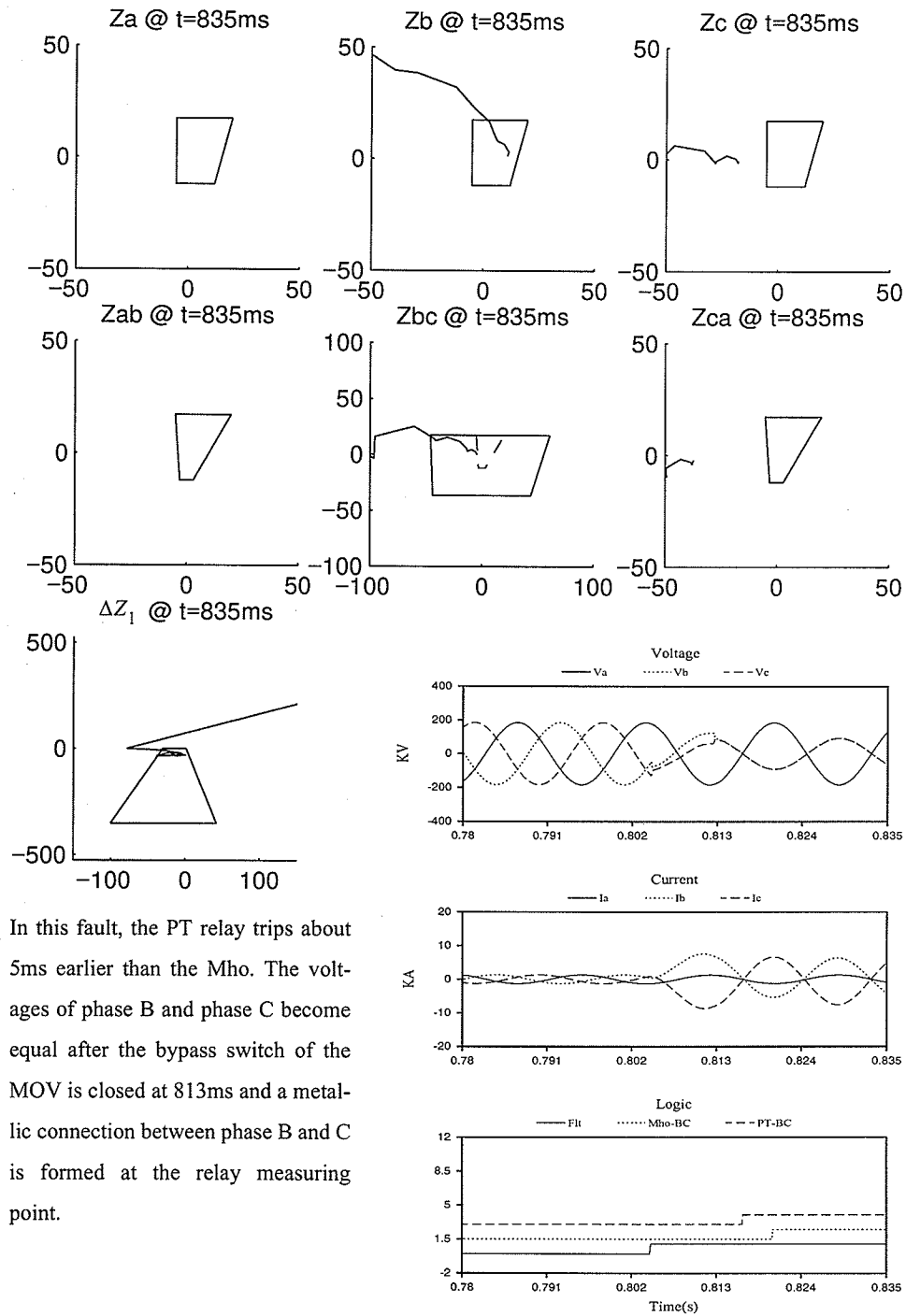
6.2.3. In the system with capacitor switched in and MOV action in the fault

In this section, the MOV is switched into the system and conducts in the fault. The fault occurs at the same point as in section 6.2.2.



In this fault, the PT relay and Mho relay trip almost at the same time. The MOV chops voltage in the fault and the bypass switch closes at 833ms

Figure 6.21. The Relays' Behaviour in a Forward AG Fault with MOV Action.



In this fault, the PT relay trips about 5ms earlier than the Mho. The voltages of phase B and phase C become equal after the bypass switch of the MOV is closed at 813ms and a metallic connection between phase B and C is formed at the relay measuring point.

Figure 6.22. The Relays' Behaviour in a Forward BC Fault with MOV Action.

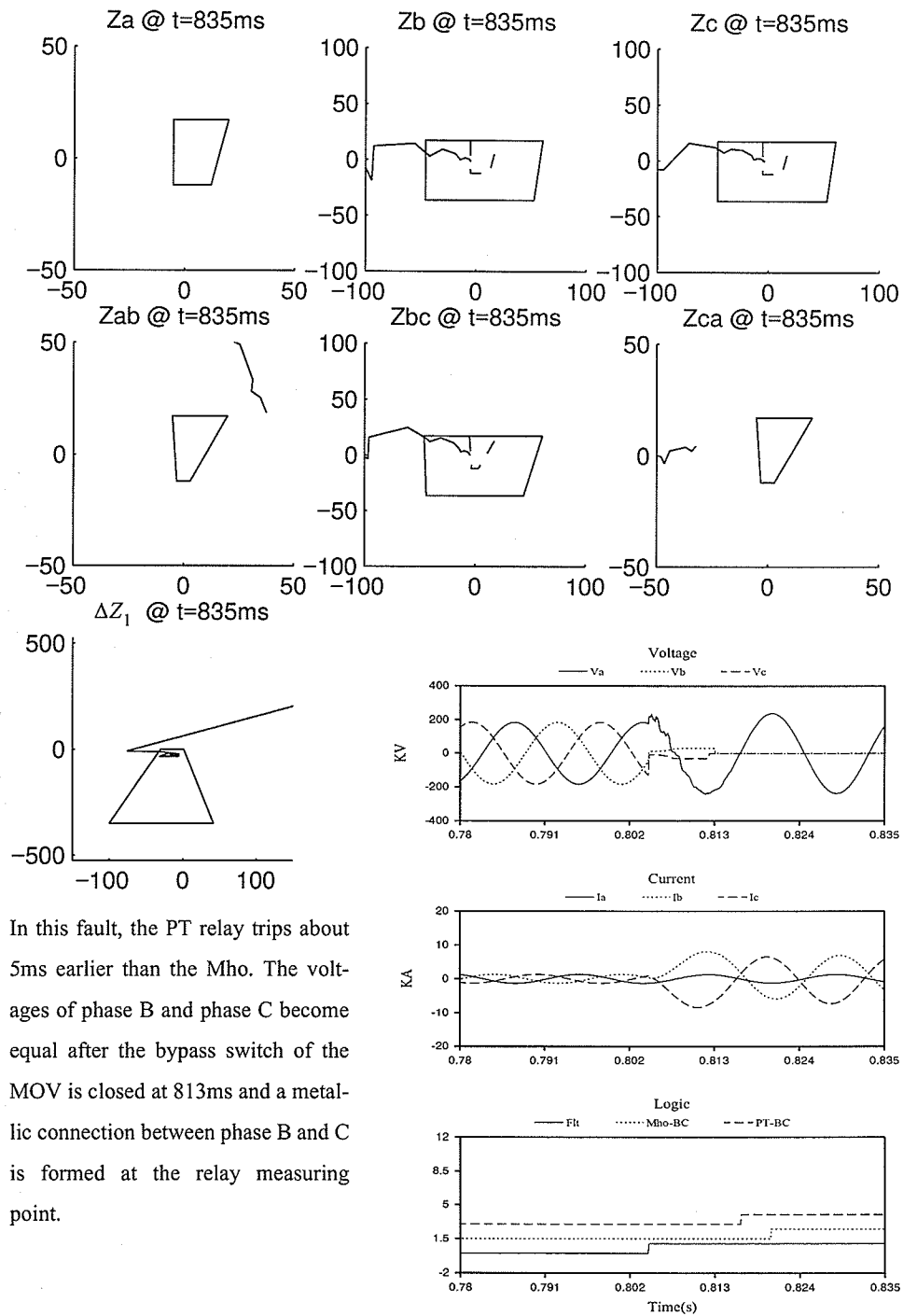


Figure 6.23. The Relays' Behaviour in a Forward BCG Fault with MOV Action.

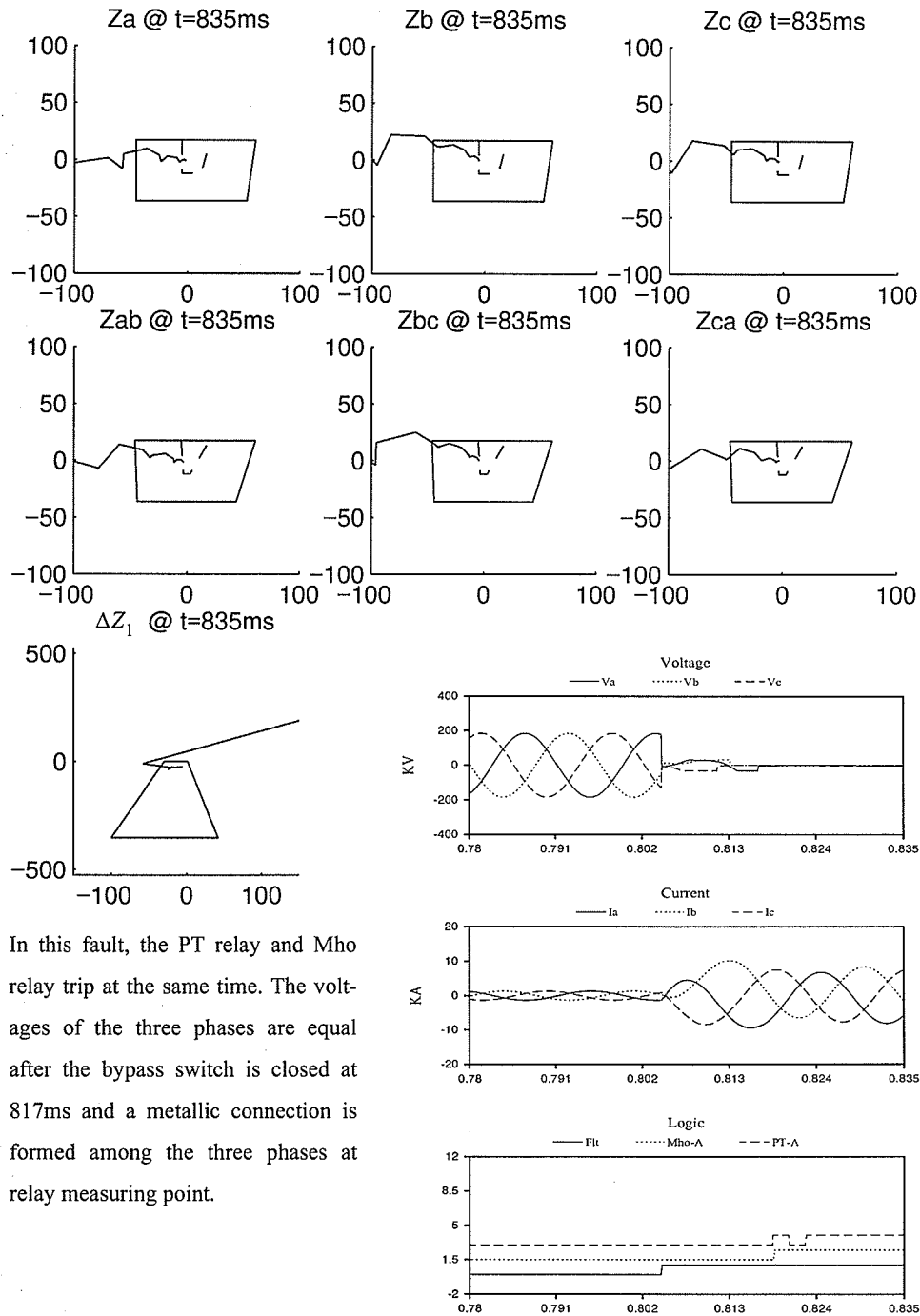


Figure 6.24. The Relays' Behaviour in a Forward ABC Fault with MOV Action.

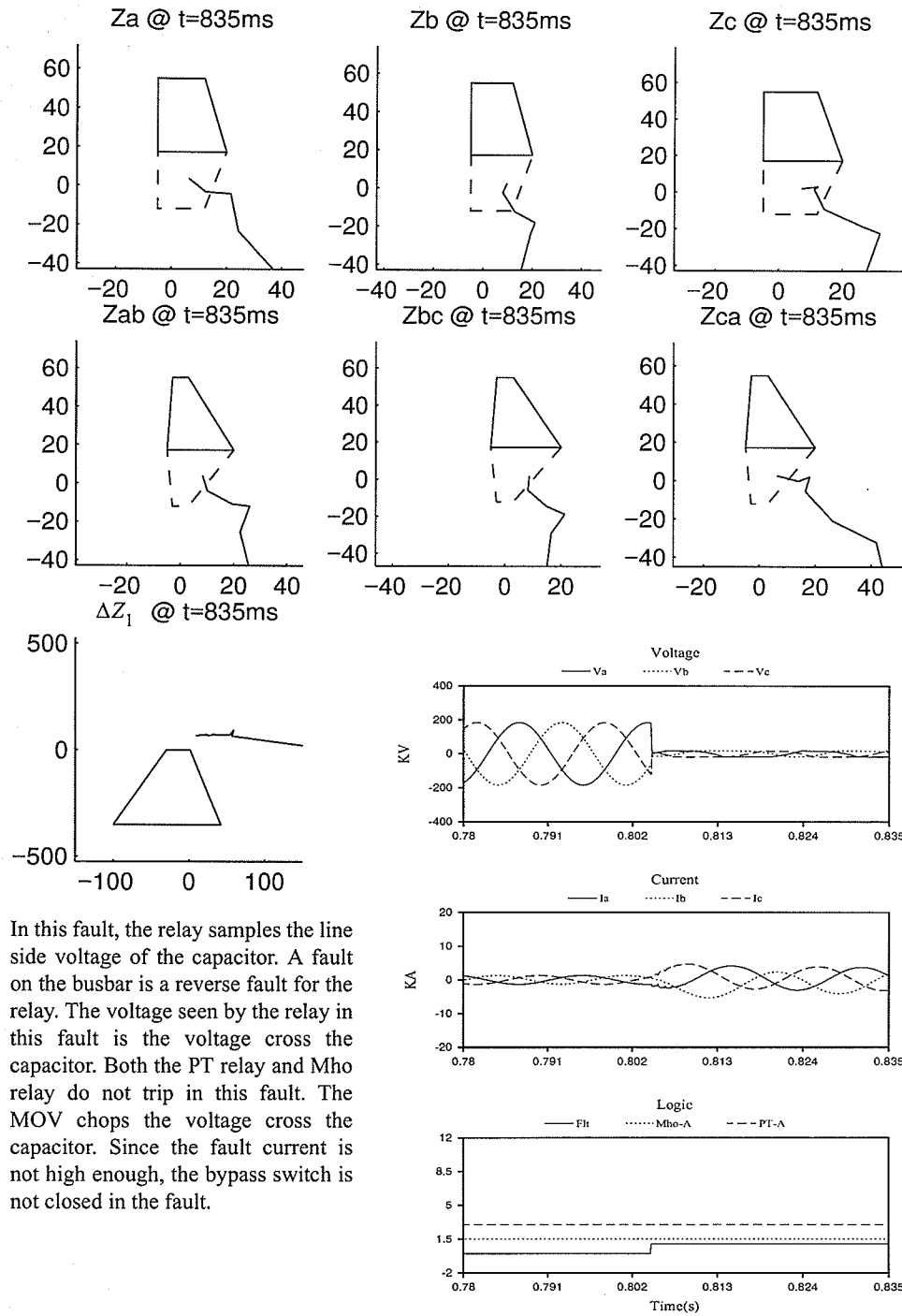


Figure 6.25. The Relays' Behaviour in a Reverse ABC Fault with MOV Action.

6.3. The mode-2 PT relay vs the Mho relay

The PT relay runs in mode 2 in the simulation cases of this section. When the PT relay operates in mode 2, the control mechanism of the horizontal expansion of the protection zone is exactly the same as in mode 1, the vertical modification of protection zone is disabled, and the PT relay does not trip unless both the IE element and DE element trip.

6.3.1. The setting of the DE

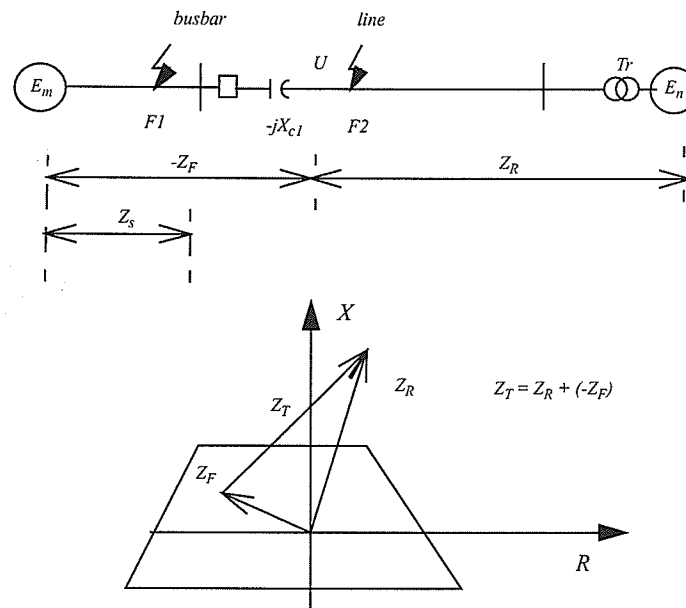


Figure 6.26. The DE Element Trip Zone in the Non Inductive-Dominated System.

If the total impedance from an arbitrary point of the transmission line to either source of the system is inductive, the system is called an inductive-dominated system. Alternatively, if the system is not an inductive-dominated system, it is called a non inductive-dominated system. In the inductive-dominated system, the setting of the DE element never appears to be a problem. The ΔZ_1 locates either in the third or fourth quadrant of the impedance plane in a forward fault or in the first or second quadrant of the impedance plane in a reverse fault, so that ΔZ_1 can be used to expand the protection of the impedance element in a forward fault and modify the protection in a reverse fault. In this kind of system, the PT relay is able to operate in mode 1 (See chapter 3).

In contrast, ΔZ_1 can settle down above the R axis of the impedance plane in both forward and reverse faults in a non inductive-dominated system as can be seen in figure 6.26. However, a proper trip zone for the DE element remains in existence in this situation. For example, the system in figure. 6.26 becomes a non inductive-dominated system if the total impedance from the line side of the capacitor to source E_m is capacitive. Suppose ΔZ_1 for a forward fault is Z_F , and ΔZ_1 for a reverse fault is Z_R . The total system impedance from source E_m to source E_n is $Z_T = Z_R - Z_F$, and should be inductive. This fact implies that a zone that separates ΔZ_1 in the forward fault from ΔZ_1 in the reverse fault does exist, as shown in figure 6.26.

6.3.2. Cases in the non inductive-dominated system

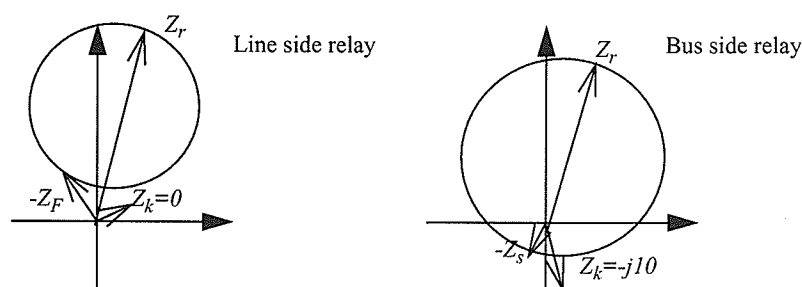
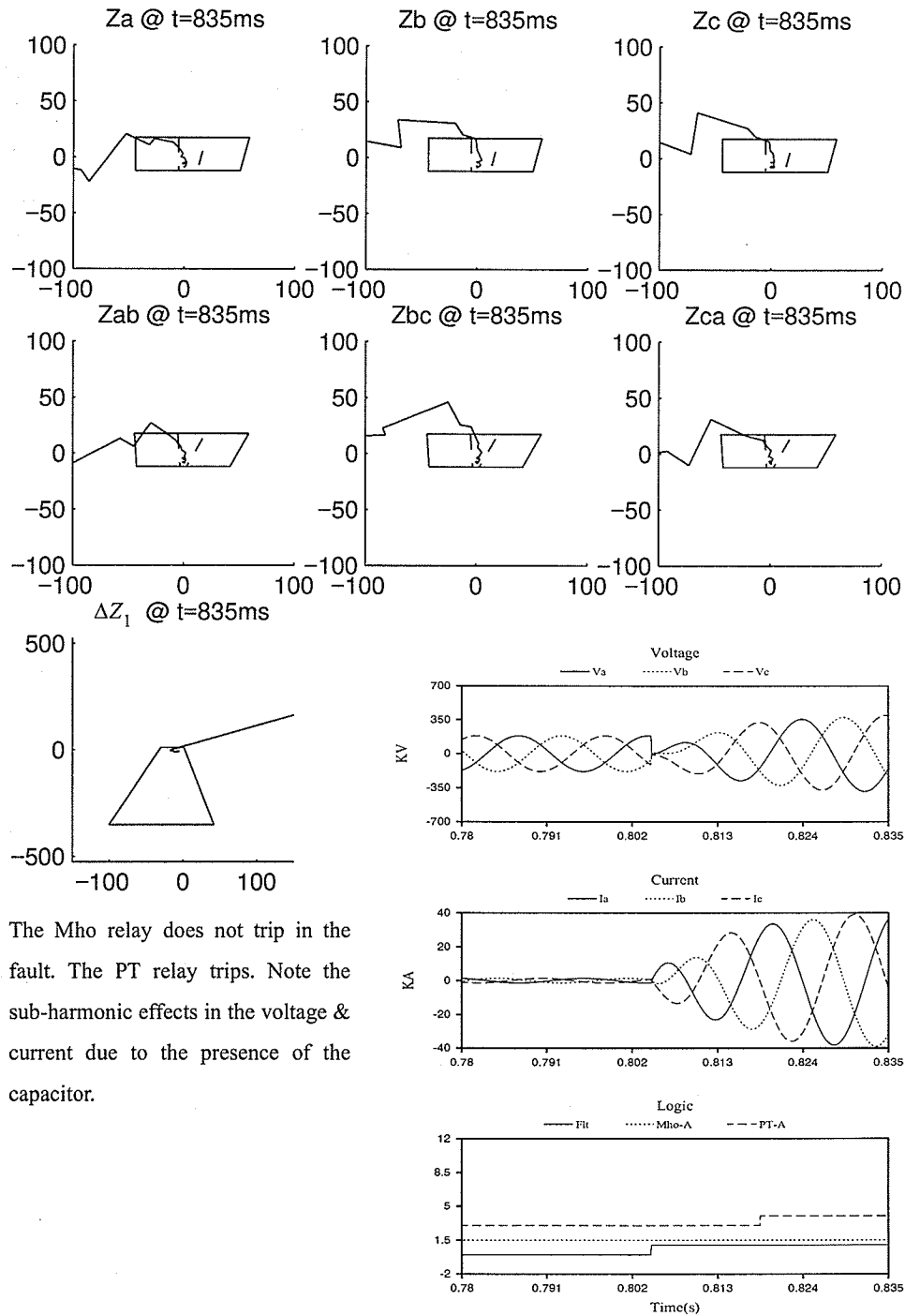


Figure 6.27. Line Side Mho Relay & Bus Side Mho Relay.

The source impedance of E_m is changed to $3.32 + j7.28\Omega$. Thus, this system becomes a non inductive-dominated system since the total impedance from the E_m to F2 is $3.32 - j2.72\Omega$.

A three phase fault happens just on the line side of the capacitor. The memory polarizing Mho relay fails in this case. In fact, the PT relay would have failed if it ran in Mode 1. The PT relay works correctly in mode 2.

In this case in figure 6.28, the forward ABC fault is applied to the system at F2, and the relay samples voltage at the busbar. The $Z_k = -j10\Omega$ falls outside of the protection zone of the Mho relay, so that the Mho relay fails in the fault (the right part of figure 6.27). By providing proper setting for the IE element of the PT relay, the PT relay is able to guard the system against this fault. The vertical setting of the bottom two points is set down to $-j12\Omega$, so that the Z_k can be contained in the protection zone. At the same time the DE element can identify this fault as a forward fault, so that the PT relay will trip this fault.



The Mho relay does not trip in the fault. The PT relay trips. Note the sub-harmonic effects in the voltage & current due to the presence of the capacitor.

Figure 6.28. The Bus Side Mode-2 PT vs Mho Relay in a Forward ABC Fault.

In the case in figure 6.29, the forward ABC fault is applied at the line side of the capacitor, but the relays sample voltage at the line side, so that the fault residual voltage is zero. The $Z_k = 0\Omega$ will fall outside the trip zone of the Mho relay since the expected source impedance is capacitive(the

left part of figure 6.27). The PT relay can identify the forward fault.

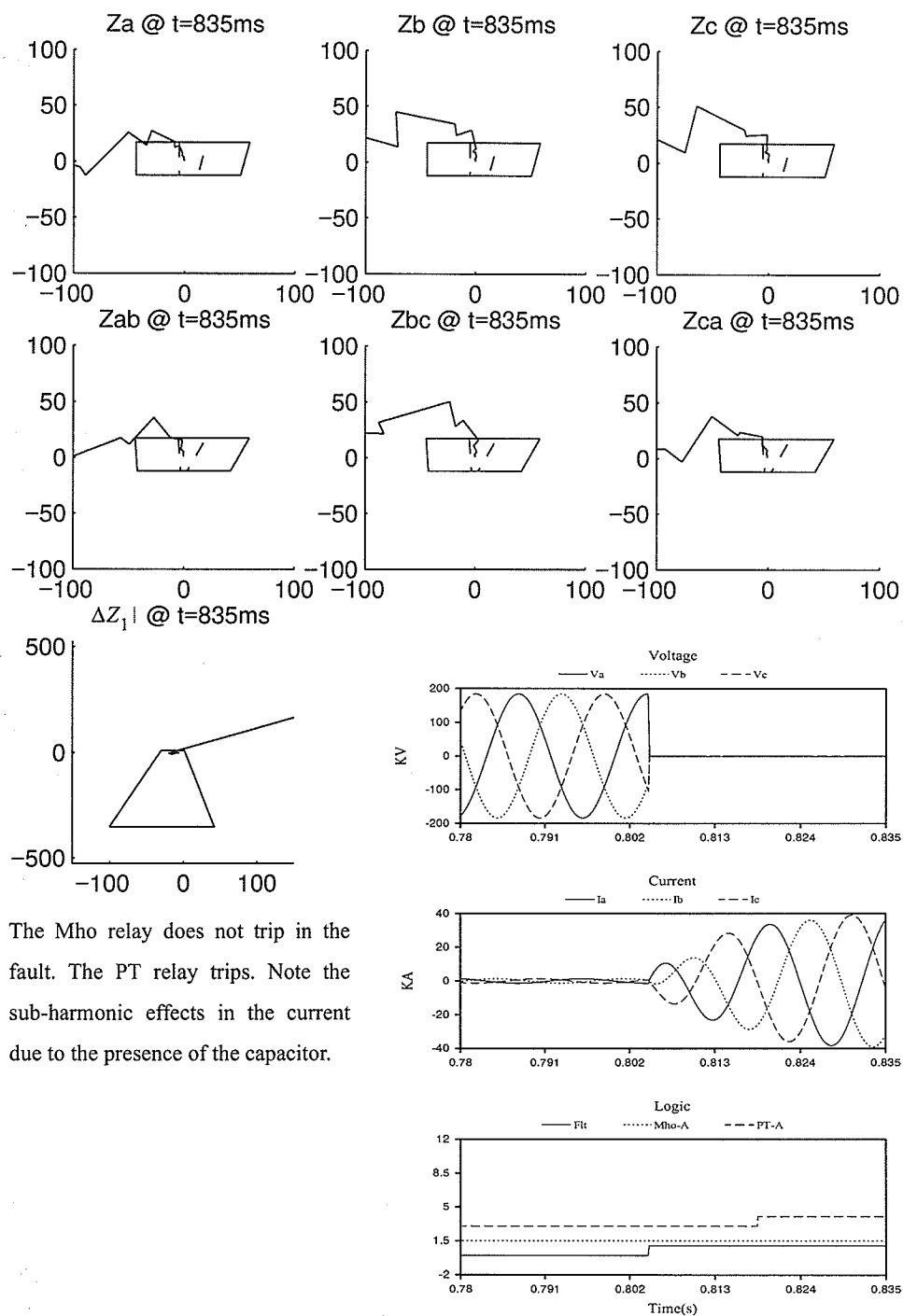


Figure 6.29. The Line Side Mode-2 PT vs Mho Relay in a Forward ABC Fault.

6.3.3. Cases in the reverse fault

A reverse fault with the capacitor in the fault loop may constitute a challenge to a distance relay since the measured impedance is in the first or second quadrant. Such a situation can happen when the series compensated neighbouring line has a close-up fault on the line side of the capacitor. This situation is similar to the situation of a fault occurring on the busbar when the relay samples the voltage on the line side of the capacitor. Figure 6.31 is to test the PT relay in the reverse fault. The MOV is not active, the voltage is sampled at the line side, the fault point is applied at the busbar, and the reach of the relays is changed to $j7\Omega$. Since this is a reverse fault, $Z_k = j10\Omega$ enters the trip zone of the Mho relay and causes its misoperation (figure 6.30), but the DE element of PT relay is able to identify the reverse fault.

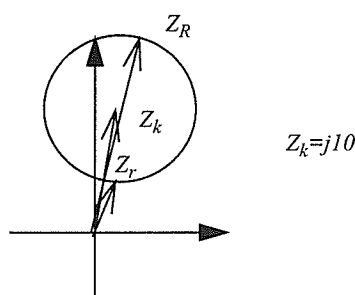


Figure 6.30. The Mho Relay in the Reverse Fault in a non Inductive-Dominated System.

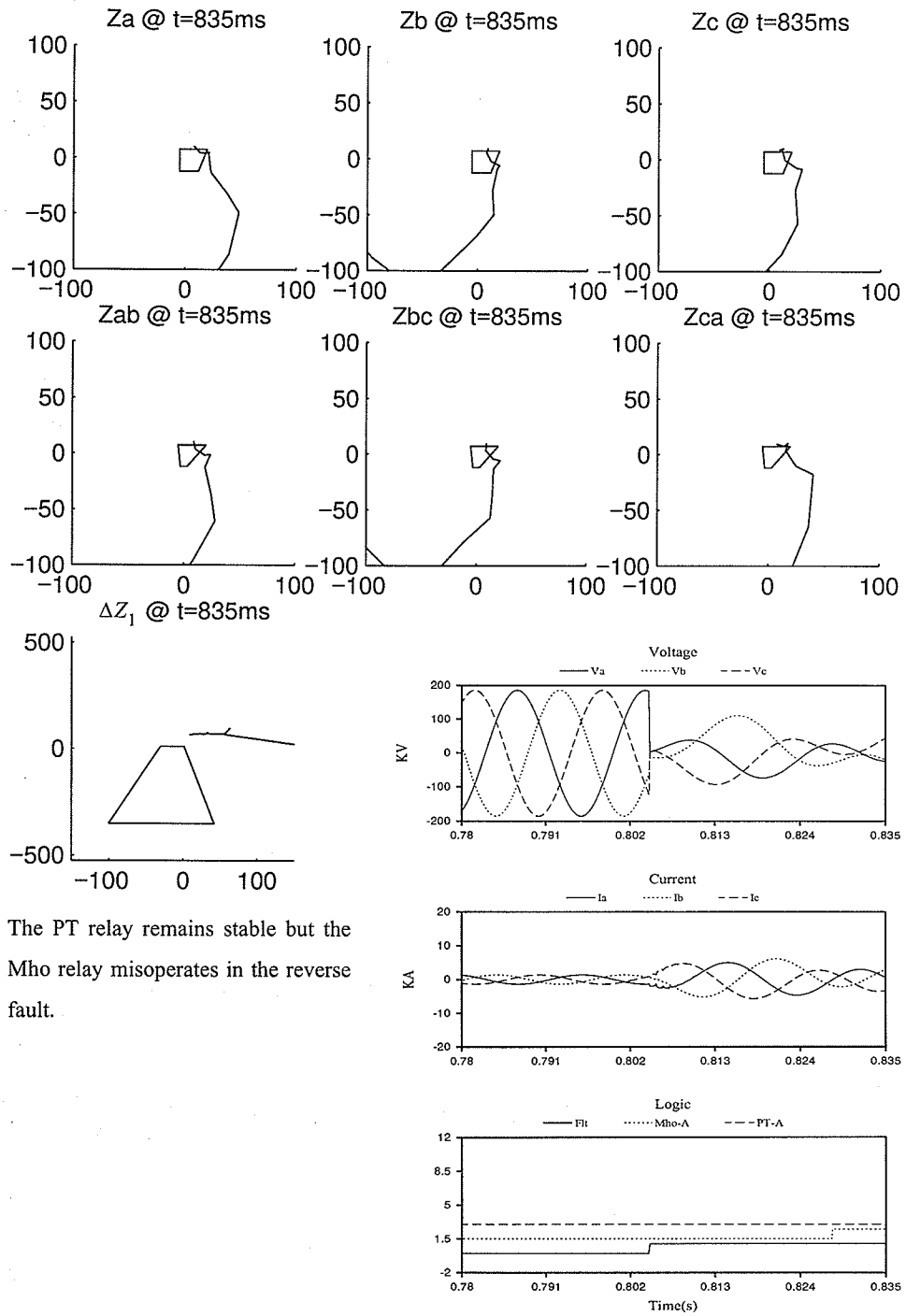


Figure 6.31. The Line Side Mode-2 PT vs Mho Relay in a Reverse ABC Fault.

6.4. Summary

1. The mode-1 PT relay is better in performance than the Mho relay in most cases.

In section 6.2, the mode-1 PT relay has a little advantage in response time over the Mho relay in most cases.

2. The Mode-2 PT relay has the advantage over the Mho relay in special system configurations.

In the cases in section 6.3, the mode-2 PT relay worked correctly but the Mho relay failed to respond to the fault. In these faults, the Mho relay either misoperates in the reverse fault or fails to trip in forward fault. However, when the PT relay runs in mode 2, the fault direction is used to control the trip signal. Since the DE element can determine the correct fault direction in any system configuration, the PT relay never misoperate in these faults.

3. In the series compensated system, the series capacitor may be switched in and out of the system. Such a situation may cause the relay's setting to be inconsistent with the system operating condition. In the inductive-dominated system, the PT relay operating in mode 1 can successfully handle the fault. In the non inductive-dominated system, in cases where the relay is set with the capacitor in the system and the capacitor is switched out of the system for some reason, the direction element of the PT relay still can identify the fault direction. Therefore the mode-2 PT relay can handle this case.

Chapter 7. The PT Relay Model in the EHV System Protection

This chapter demonstrates a method to evaluate a relay's behaviour using an accurate software model[3]. Traditionally, relay engineers test an actual relay by either relay test set or Transient Network Analyser (TNA). This kind of equipment is usually very expensive, moreover it is difficult to understand a relay's behaviour since the internal trip logic signals of the actual relays are not available.

PSCAD/EMTDC provides a useful off-line simulation to help with the evaluation of a relay if the accurate software relay model exists. In the PSCAD simulation, even internal signals and variables of the relay can be monitored. This is a valuable property when the evaluation is focused on relay modelling, and it is a very convenient way to detect the weaknesses of the relay at the research stage. It also provides the relay engineer with a very useful approach to understand the interaction between the relay and the power system.

Two cases will be shown in this chapter. In the first, the simulation system is a single transmission line system. In the second, the simulation system is a double line system. In both systems, the protection scheme is planned to provide fast fault coverage on the full line. The PT relay is used as the zone 1 of the transmission line protection scheme, and zone 2 is a simple quadrilateral distance relay with the pilot signals exchanged between the relays to accelerate zone 2.

The block average phase comparator polarized Mho relay[17] is used as the reference to evaluate the PT relay model in the protection scheme.

7.1. The general relay configuration for UHV transmission line protection

The relays are installed at the two ends of the transmission line. In EHV and UHV transmission line protection, the relay is designed to provide a quick trip over the full length of the line without losing selectivity. In the protective scheme of an EHV or UHV transmission line, the protective relay scheme is configured with a suite of protective relays. Normally, when the distance relay is involved in the protection of an EHV or UHV transmission line, the following are the minimum

configurations selected from the relay suite:

A zone 1 element for each phase to cover 85% of the line;

a zone 2 element for each phase to cover the full line and part of the neighbouring line;

a communication channel to exchange the pilot signal of the relays at the two ends of the line. The local pilot signal is sent to the remote relay when zone 1 or zone 2 elements are triggered. When zone 2 is triggered and the remote pilot signal is received, the relay trips.

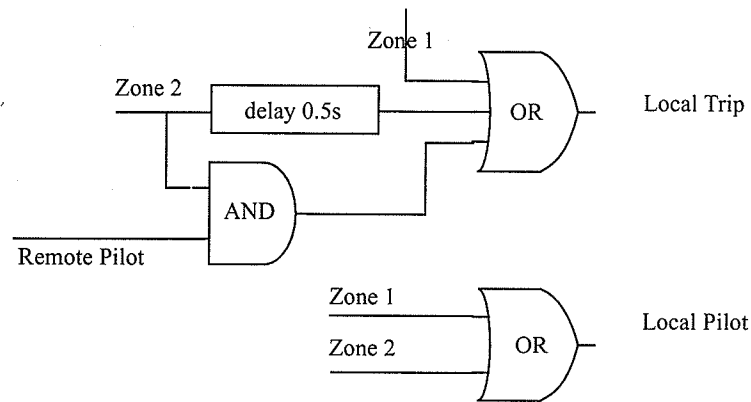


Figure 7.1. The Logic of an UHV Line Relay.

7.2. The block average comparator relay

The success and industrial acceptance of the block average comparator make it an ideal reference for the PT relay. A detailed block diagram of the two-input block average comparator is shown in figure 7.2. Input waveforms S1 and S2 are derived from the power system's voltages and currents measured by the relay, using replica impedances and mixing circuits. Accurate zero crossing detectors, Schmitt triggers, convert the input sinusoidal waves into square waves. Polarity coincidence of the square waves is detected with an 'Exclusive OR' gate, which gives a zero output level when P1 and P2 are in the same polarity. The output of the 'Exclusive OR' gate is applied to the integrator circuit. The output of the integrator increases when the 'Exclusive OR' output is zero and decreases when the output is positive. Suppose the voltage input signal is between the level 0 and 1, then the relationship between the output and input signal can be described by the equation 7.1:

$$acu = -\frac{2}{T} \cdot \int (in - 0.5) \cdot dt \quad 7.1$$

T is the period of the power system. acu has an upper and lower limit.

The integrator output is monitored by a level detector which trips if the integrator exceeds a preset threshold. The block average comparator generates the trip signal by evaluating the long term polarity coincidence, not by momentary measurement. This feature ensures its reliability and security.

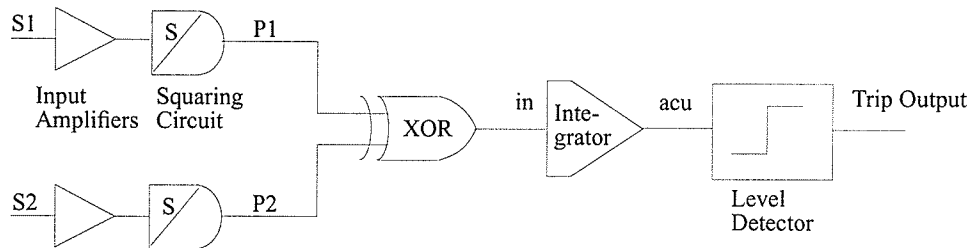


Figure 7.2. The Block Average Comparator Relay.

7.3. The single transmission line system

In the simulation system, zone 1 of the PT relay is adaptive, and zone 2 is the simple quadrilateral relay. The relay side source is a generator. This section will observe the PT relay's behaviour as part of the integrated protection scheme and in postfault power swings. During the simulation, the relays use the primary side quantities, and the current transformer and voltage transformer of the relay are omitted.

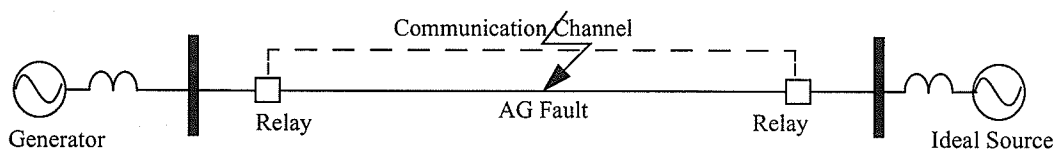


Figure 7.3. The Single Transmission Line System.

An AG fault happens at 0.8s and is removed when the relay trips. The auto-recloser recloses the breaker of the phase at 1.15s and the power system enters a severe power swing. Figure 7.4 shows the voltages and currents measured by the relay at the generator side. The fault is cleared at the time when the current crosses zero. Before the breaker is opened during fault and after the breaker is reclosed, there are travelling waves.

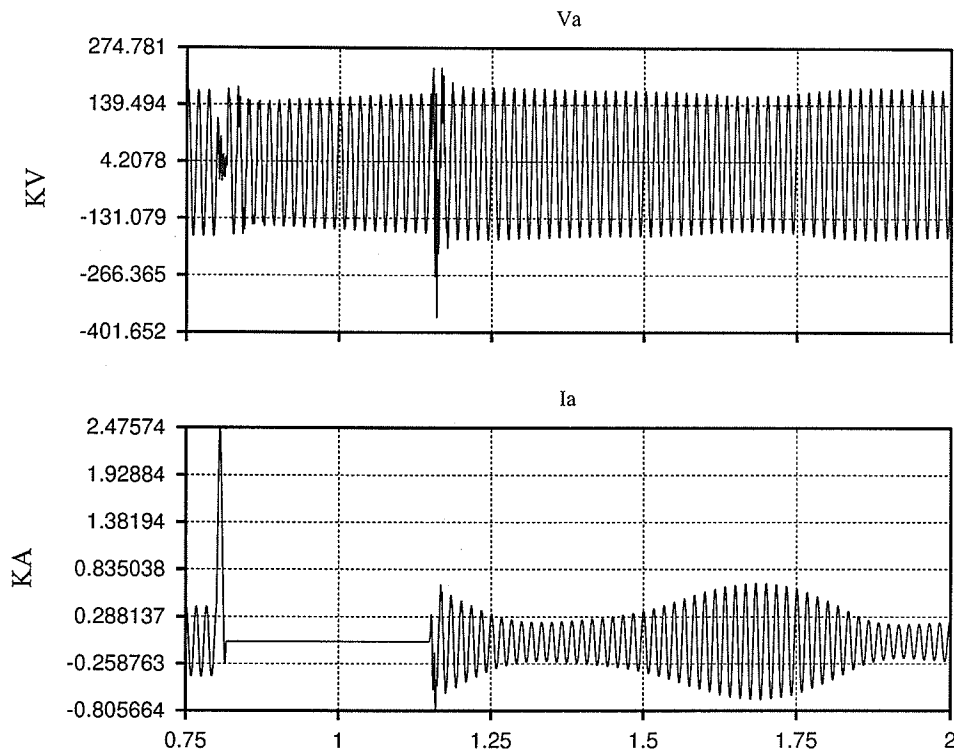


Figure 7.4. Voltage & Current of System in Fault & Power Swing.

The impedance of phase A is shown in figure 7.5. The top part of the figure is the impedance trajectory(R-X), and the lower part is the measured R and X of phase A vs time.

Mark 'O' marks the steady state impedance, mark 'T' marks the fault impedance and the relay setting zone, mark 'X' marks the area where the Z_a whirls due to the power swing after the breaker recloses.

This case demonstrates that the PT relay is able to function well in a fault and survive the power swing since the measured impedance is far from the setting zone of the PT relay.

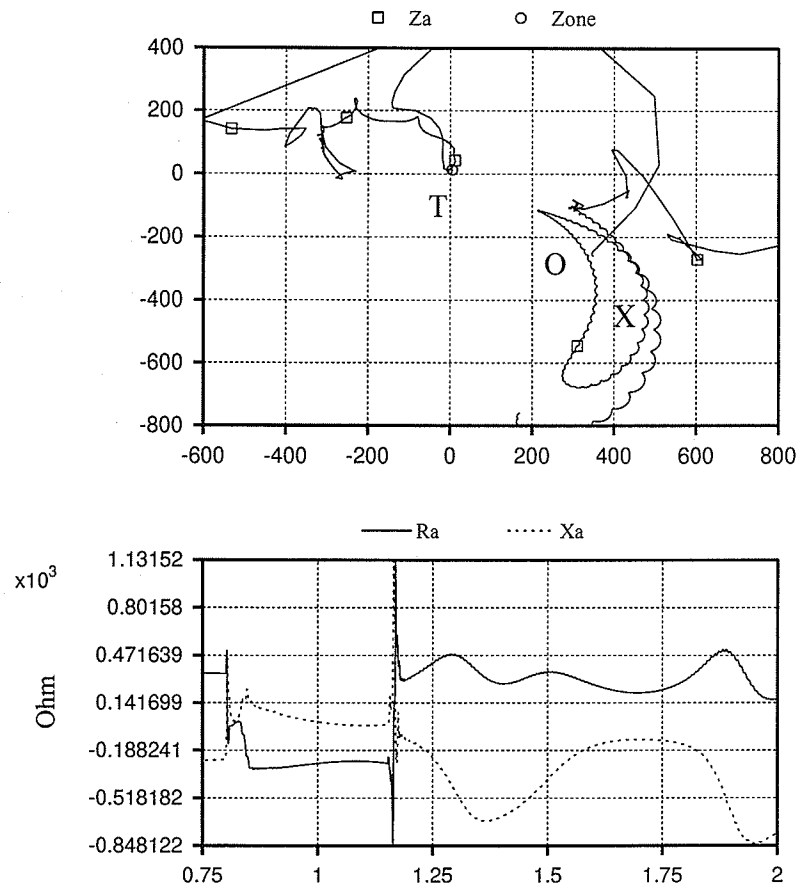


Figure 7.5. Impedance of Phase A in Fault & Power Swing.

7.4. The double transmission line system

The prototype of the double line system is the McCalmont-Springdale 500KV system[48]. The total length is 150km and the line is transposed three times. The two sources of the system are modelled by an ideal source. In the prefault steady state, the source at Springdale leads the source at McCalmont by 30 degrees.

In this system, a relay is installed at the end of each line. The protection relay is supposed to provide the full line fault coverage, so the communication channels are in place for the relay. figure 7.6 shows the system configuration.

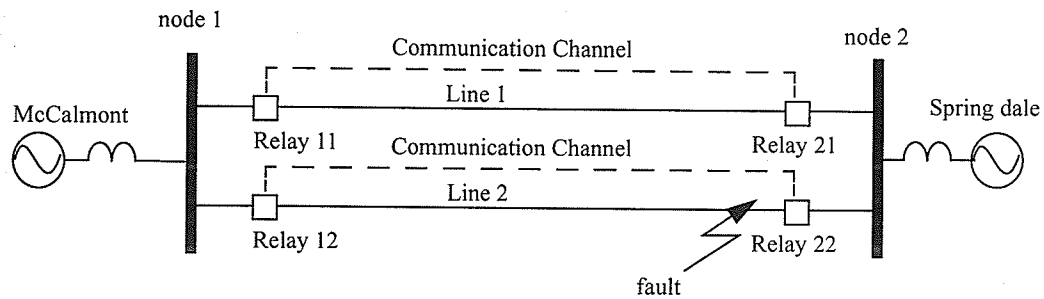


Figure 7.6. The Double Transmission Line System.

In this simulation, an AG fault is applied to the system at 0.7 seconds. The voltages and currents of line 1 at node 1 are displayed in figure 7.7.

7.4.1. The block average Mho during a system fault

The first protective relay tested is the block average Mho. acu is limited to range between 0 and 2. The level detector's threshold is set to 1.05. The acu of zone 1 and of zone 2, and the breaker trip signals of phase A are displayed in figure 7.8. Single pole trip logic is used in this system.

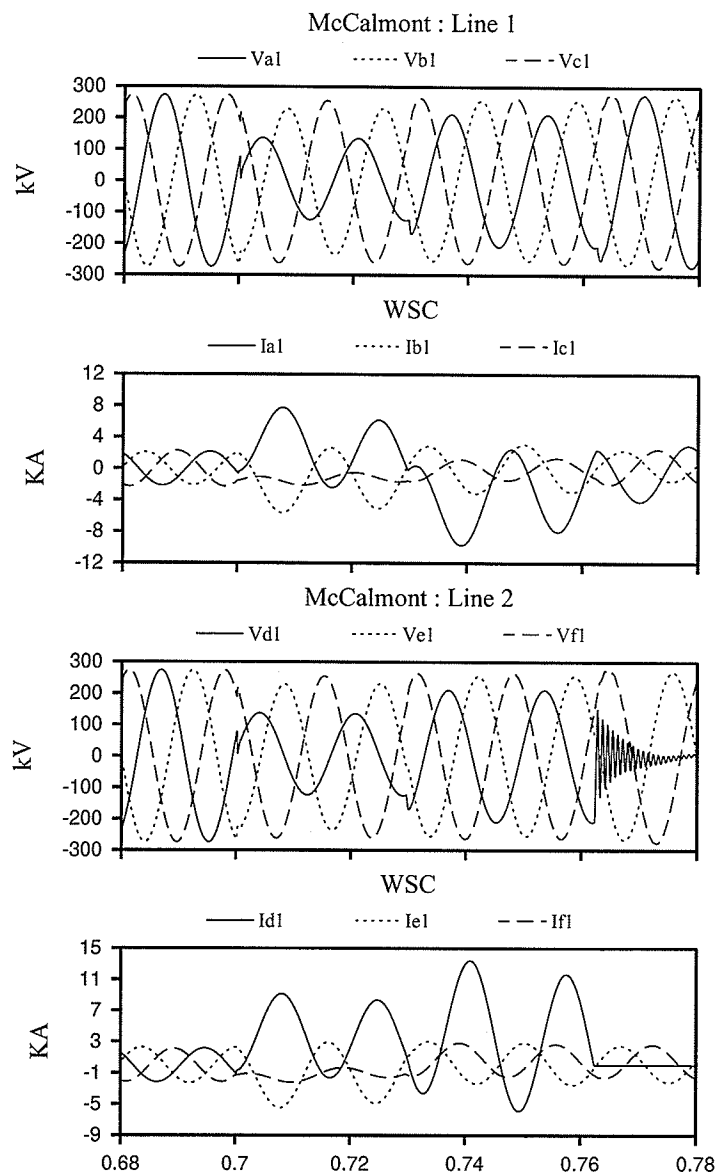


Figure 7.7. The Voltage & Current of Lines at Node 1.

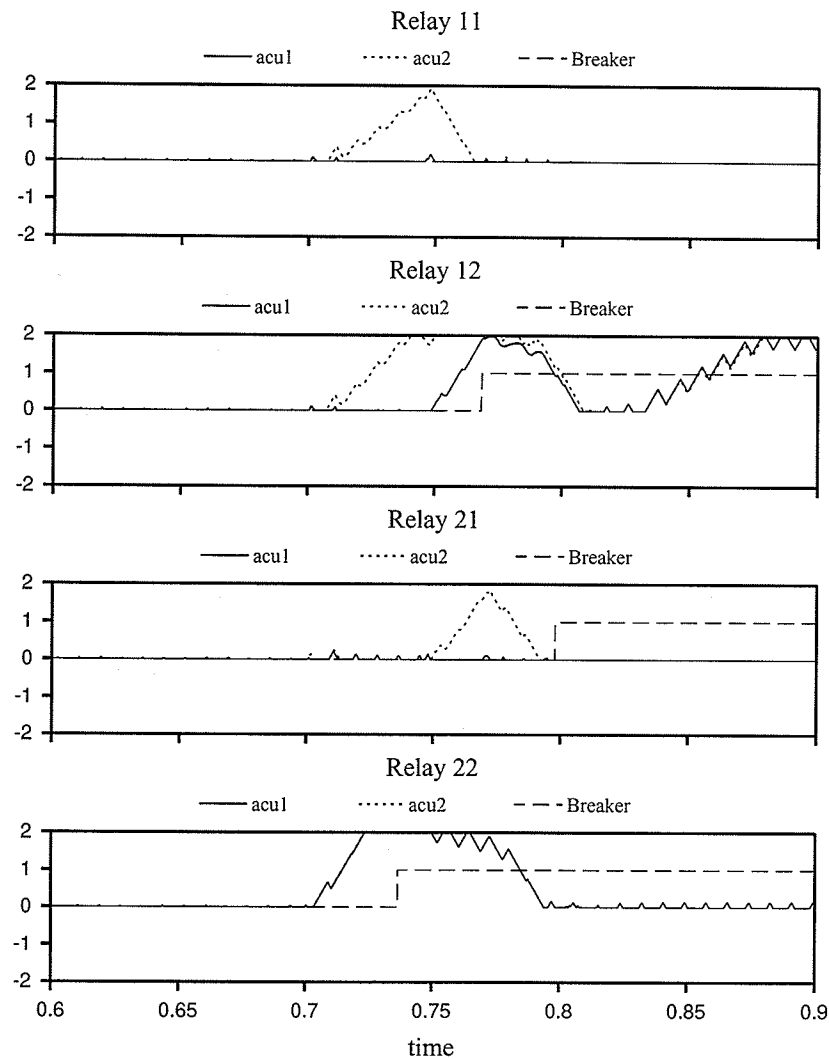


Figure 7.8. The Behaviour of Block Average Mho in Double Line System Fault.

To simulate a practical situation, the pilot signal is delayed 10 ms in the communication channel, and the breaker trip signals are issued about 10ms to 15ms after the relay trip signal to simulate the operating circuit time delay. The breaker is tripped at the first zero crossing point of the current through the breaker.

Since the fault occurred on line 2, relay 12 and relay 22 tripped correctly. However, figure 7.8 shows that relay 21 misoperated in the fault. The misoperation is caused by the interaction between the four relays. A simulation can help us to analyse the reason of misoperation. The zone

2 of relay 11 triggers in the fault. This behaviour is reasonable because the fault point is at the end of the line from its point of view, so its pilot signal is sent to relay 21. After breaker 22 opens, relay 21 experiences a current phase reversal which causes its zone 2 to trigger. The pilot signal from relay 11 accelerates the zone 2 of relay 21 and results in the misoperation. The zone 2 of relay 11 has come down when the pilot signal of relay 21 arrives, so that relay 11 does not misoperate.

It is impossible to examine this scenario with a real relay, since these internal variables of the relay are not usually available.

7.4.2. The PT relay in the double line system fault

This section investigates the performance of the PT relay in the same fault. Figure 7.9 shows the impedance trajectory of phase A measured by the PT relay during the fault. The figure also shows the setting zone of zone 1 and setting zone of zone 2 of the relay. Actually, zone 1 of the PT relay changes dynamically and is different from its setting zone. However we still present the setting zone since presentation of the dynamic zone would use much more room.

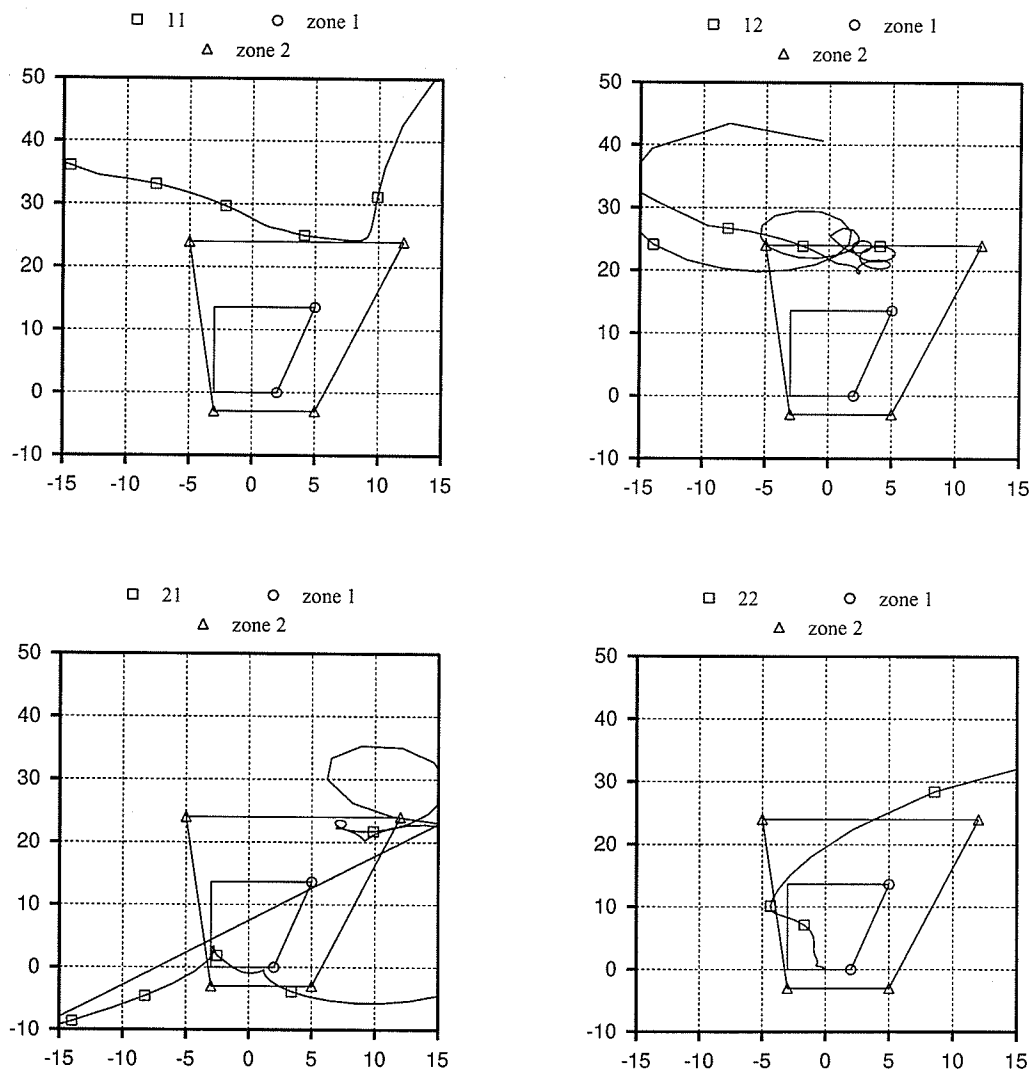


Figure 7.9. Impedance Trajectory in Double Line Fault.

Figure 7.10 shows the circuit breaker trip signal. The pilot signal time delay and operating circuit time delay are in place to keep this case consistent with the case for the block average Mho.

In this case, zone 1 of relay 22 trips, zone 2 of the relay 12 is accelerated by the pilot signal from relay 22. The impedance enters the setting zone of zone 1 of relay 21(not its trip zone), but the relay senses a reverse fault since the voltage and current sensed by relay 21 in this fault is the

same as that sensed in a busbar fault and the relay trip zone will flip up in this fault. So relay 21 does not trip. Relay 11 does not trip since the impedance does not enter its trip zone.

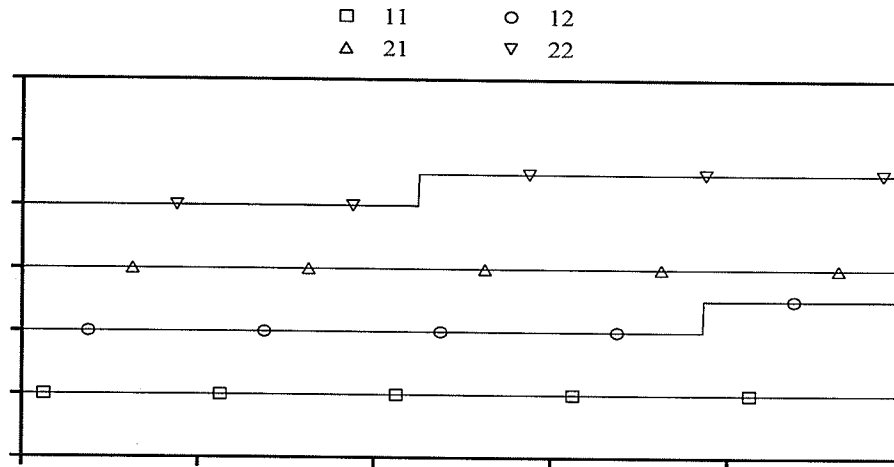


Figure 7.10. Breaker Open Signal in Double System Fault.

In this fault, the protection suite based on the PT relay functions well.

7.5. Conclusion

This chapter demonstrates an off-line relay model test method. This method has several advantages over the traditional test approaches in which a TNA or a relay test set are involved using a real relay.

This method is less expensive than the traditional method, and is more effective in finding out the design flows, since it allows the tester access to as much information from the relay as is possible. This method is also very useful in the analysis and diagnosis of misoperations caused by the interaction among the power system components. It can only be used if an accurate software model of the relay is available.

In the double line fault, the PT relays are able to function well and the Mho relay misoperates. The detail is explained in section 7.4. The misoperation of the Mho relay results from the very specific combination of the communication channel delay, trip level, and operating circuit delay, and a different result may be obtained if any of them is changed.

Chapter 8. The Hardware Application of the PT Relay

To test the PT relay algorithm, two hardware applications have been completed in this thesis. This chapter introduces these two hardware applications of the PT relay. The first application is an implementation of the relay based on the TI TMS320C32 CPU. The second application is an implementation based on the Pentium CPU.

8.1. The hardware of the TMS320C32 & Pentium system

The TMS320C32 system was started at the time when Intel 386 was used as the CPU of the IBM compatible PC. The relay hardware is a DSP board embedded in an Intel 386 PC host since the Intel 386 CPU can not handle the complicated computation of the relay. The DSP board is dedicated to relay algorithm while the 386 PC is selected to do some back ground tasks for the relay, such as communication with the external world, displaying the data or recording the fault event. However, the Pentium CPU can handle the complicated floating point computation. Its embedded floating point coprocessor gives it powerful floating point computation ability. Moreover, there are also many off-the-shelf operating systems which support the application on the Pentium. The investigation of the Pentium system is motivated by seeing whether a Pentium system alone can be used as a relay.

8.1.1. The hardware of the TMS320C32 system

TMS320 is a product of Texas Instrument (TI) which has been the digital signal processor (DSP) market leader since 1982, and continues to be the largest manufacturer of programmable DSPs. The TMS320 family of 16/32-bit single-chip digital signal processors combines the flexibility of a high-speed controller with the numerical capability of an array processor. The highly paralleled architecture and efficient instruction set provide speed and flexibility to produce a MOS micro-processor family that is capable of executing more than 12.5 MIPS (million instructions per second). The TMS320 family optimizes speed by implementing functions in hardware that other processors implement through microcode or software. This hardware-intensive approach provides

the design engineer with processing power previously unavailable on a single chip. The powerful floating point computational capability makes the DSP a suitable choice for building a power system digital protective relay. A host PC, a target TMS320C32 based board, and analog to digital convertor comprise the PT relay hardware. The host PC provides an ISA slot to receive the TMS320C32 board. The PC and TMS320C32 share a 4K dual port memory which can be accessed by both the PC and TMS320C32. The PC and TMS320C32 exchange data via the dual port memory. When the system boots, the PC puts the application code into the dual port memory and the TMS320C32 loads and runs it. When the target board records a power system fault, it puts the recorded data into the dual port memory and the PC saves the data into a recording file.

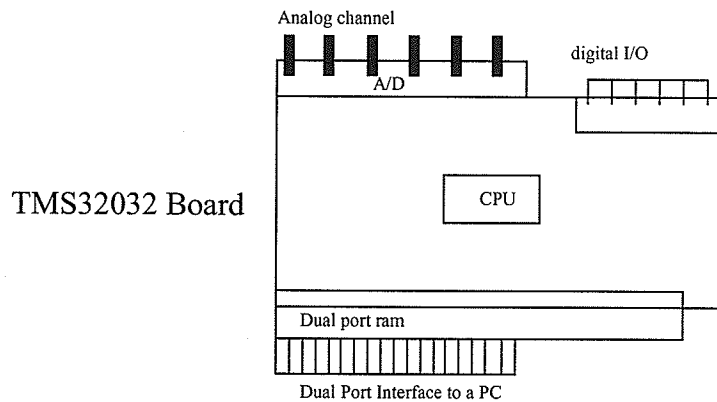


Figure 8.1. The Hardware Structure of the TMS32032 Board.

8.1.2. The hardware of the Pentium system

This application of relay algorithms is based on the PCM-5862 Pentium motherboard and the DM6420 A/D board.

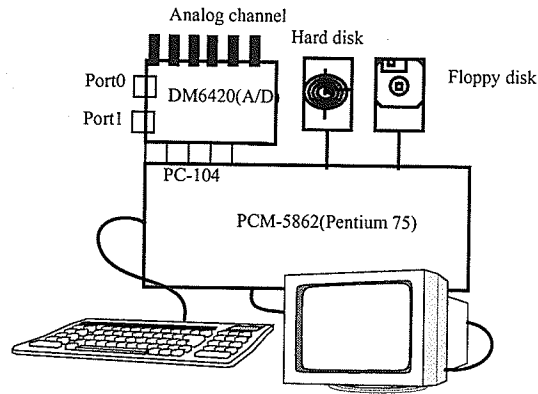


Figure 8.2. The Hardware Structure of the Pentium System.

8.1.2.1 The PCM-5862 motherboard

The PCM-5862 is a 75Mhz Pentium processor-based single board computer manufactured for industrial stand alone applications.

On-board features includes 512KB 2nd level cache, four serial ports(three RS-232, one RS-232/422/285), one multi-mode parallel(ECP/EPP/SPP) port, two USB(Universal Serial Bus) ports, a floppy drive controller and a keyboard/PS/2 mouse interface, and watchdog timer. The built-in high speed PCI IDE devices can be connected, including large hard disk, and tape backup drives.

The PCM-5862 motherboard also provides the following features to fit a specific application.

Accepts Intel MMX Pentium, AMD K5, and Cyrix 6x86 processors up to 200MHz.

32-bit PCI-bus SVGA/LCD controller supports LCD & CRT display.

10Base-T Ethernet interface, Novell NE-2000 compatible.

16-bit audio interface, Sound Blaster Pro compatible.

PCI slot, and PC-104 connector for flexible expansion capability.

8.1.2.2 The DM6420 A/D board

The DM6420 analog I/O data Module turns the PCM-5862 motherboard into a high-speed, high-performance data acquisition and control system. Ultra-compact for embedded and portable applications, the DM6420 module features:

8 differential or 16 single-ended analog input channels,
12-bit, 2 microsecond analog-to-digital converter with 500 kHz throughput,
Programmable input ranges: -5/5, or -10/10 volts,
Programmable gains of 1, 2, 4 & 8,
1024 x 24 channel-gain scan memory with skip bit,
Software, pacer clock and external trigger modes,
Scan, burst and multiburst using the channel-gain table,
16-bit programmable high speed sample counter,
A/D DMA transfer,
1024 sample A/D buffer for gap-free high speed sampling
Pre-, post- and about-trigger modes,
3-bit analog input data/trigger marker,
8 bit programmable digital I/O lines with Advanced Digital Interrupt modes,
1024 sample digital input buffer for gap-free high speed sampling
8 port programmable digital I/O lines,
Six 16-bit timer/counters (two available to user) and on-board 8 MHz clock,
Two 12-bit digital-to-analog output channels,
-5/5, or -10/10 volt analog output range,
Programmable interrupt source,
+5 volt operation.

The following paragraphs briefly describe the major functions of these modules.

Analog-to-Digital Conversion

The DM6420 is software configurable on a channel-by-channel basis for up to 16 single-ended or 8 differential analog inputs. Software programmable unipolar and bipolar input ranges and gains allow easy interfacing to a wide range of sensors. A/D conversions are typically performed in 2 microseconds, and the maximum throughput rate of the board is 500 kHz. Conversions are controlled by software command, by an on-board pacer clock, by using triggers to start and stop sampling, or by using the sample counter to acquire a specified number of samples. Several trigger

sources can be used to turn the pacer clock on and off, giving the user exceptional flexibility in data acquisition. Scan, burst, and multiburst modes are supported by using the channel-gain scan memory. A first-in-first-out (FIFO) sample buffer helps PCM-5862 manage the high throughput rate of the A/D converter by acting as an elastic storage bin for the converted data. Even if the computer does not read the data as fast as conversions are performed, conversions can continue until the FIFO is full.

The converted data can be transferred to PC memory in one of three ways. Direct memory access (DMA) transfer supports conversion rates of up to 500,000 samples per second. Data also can be transferred using the programmed I/O mode or the interrupt mode. A special interrupt mode using a REP INS (Repeat Input String) instruction supports very high speed data transfers. By generating an interrupt when the FIFO's half-full flag is set, a REP INS instruction can be executed, transferring data to PC memory and emptying the FIFO buffer at the maximum rate allowed by the data bus.

The mode of transfer and DMA channel are chosen through software. The PC data bus is used to read and/or transfer data to PC memory. In the DMA transfer mode, you can make continuous transfers directly to PC memory without going through the processor.

8254 Timer/Counters

Two 8254 programmable interval timers provide six (three each) 16-bit 8 MHz timer/counters to support wide range of board operations and user timing and counting functions. The Clock TC is used for board operations. Two of the 16-bit timer/counters in the Clock TC are cascaded and used internally for the pacer clock. The third timer/counter is used as the burst clock. The User TC has two 16-bit timer/counters for user functions and one 16-bit timer/counter for the sample counter.

8.1.2.3 The application system

The PCM-5862 motherboard provides an ISA-like PC-104 port to accept the DM6420 A/D board as shown in fig.7.2.

The PC-104 links the PCM-5862 motherboard and DM6420 A/D board into the hardware environment of the PT relay application. A/D acquisition data, digital input, and relay trip

command are exchanged between the two boards via the PC-104 port. The PCM-5862 can also query and modify the DM6420 operation via the PC-104.

The DM6420 board provides six analog-to-digital channels to sample the voltages and currents. The two 8-bit ports on the DM6420 board are programmed to serve as either input or output ports. In the PT relay application, one is configured as the digital input to allow the relay to sample the binary signal and the other is configured as the output to allow the relay to send the trip or reclose commands.

A watch dog timer on the PCM-5862 board is programmed to provide protection for the PT relay system. The watch dog reduces the chance of disruptions caused by EMP(electro-magnetic pulse) interference. The watch dog is an invaluable protective device for a stand alone or unmanned application. Normally, the relay resets the watch dog timer before the timer times out. When the relay system crashes, the watch dog timer times out and the relay system is reset. A watch dog provides a relay with the mechanism to recover from an abnormal condition.

The floating point co-processor in the Pentium CPU ensures that the PCM-5862 finishes the relay's computation load in real time.

The VRTX operating system is used to manage the hardware of the Pentium system and software operation. A floppy drive is installed in the system. When the system powers up, it allows the VRTX bootable floppy disk to boot the Pentium system into the VRTX environment and run the relay application. The floppy drive also allows the Pentium system to exchange data with the external world.

A hard drive is installed to save the relay recording data.

The monitor and keyboard are used to give user access to the relay.

The system can also be configured to use the serial port as its input and output. In such a situation, the Pentium system can be connected to a PC via serial port and a Hyperterminal application running under Windows can serve as the console of the Pentium system.

8.2. The software of the TMS320C32 & Pentium system

The interrupt is widely used to program the microprocessor-based relay device. An interrupt is an event that causes the processor in the computer to temporarily halt its current process and execute another routine. Upon completion of the new routine, control is returned to the original routine at

the point where its execution was interrupted. Interrupts are very handy for dealing with asynchronous events. Keyboard activity is a good example; the computer cannot predict when a user might press a key and it would be a waste of processor time for it to do nothing while waiting for a keystroke to occur. Thus, the interrupt scheme is used and the processor proceeds with other tasks. Then, when a keystroke does occur, the keyboard 'interrupts' the processor, and the processor gets the keyboard data, places it in memory, and then returns to what it was doing before it was interrupted.

8.2.1. The software of the TMS320C32 system

The software of TMS320C32 includes two parts. The first part of the software runs in DOS mode on the host PC to serve as the foreground of the relay. It is the responsibility of this software to load the boot code of the target DSP board into the dual port memory, load the settings of the relay into the dual port memory, dump the fault data from the dual port memory into a recording file, show the run time data on the monitor of the PC, and receive and handle the user command. This software is created with Borland C++.

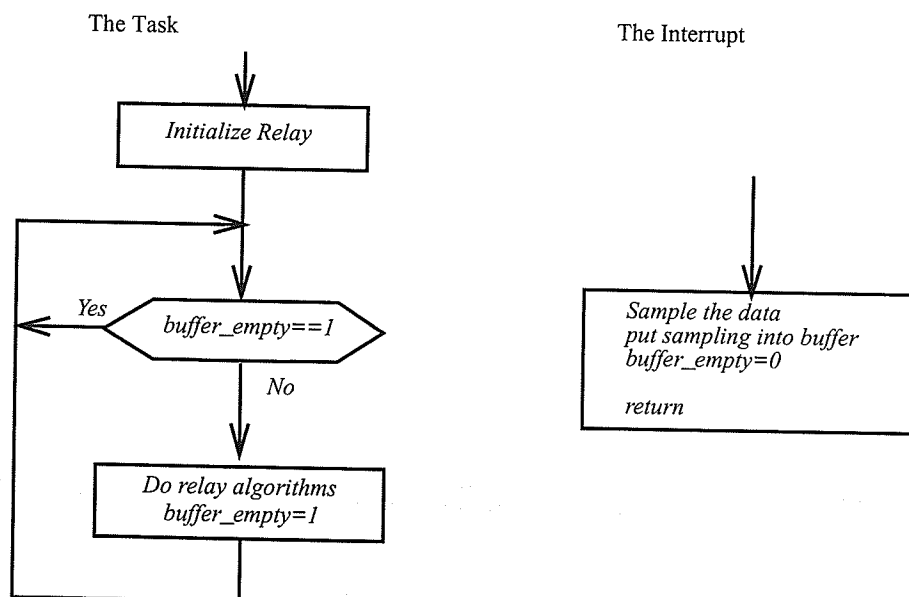


Figure 8.3. The Relay Software Flow Chart of TMS320 System.

The other software runs on the target system, and this software is responsible for handling data

acquisition and processing data. The relay algorithm is implemented in this software. The PT relay algorithm is programmed with the C-language. The machine code can be created by running the C31 compiler and linker. The flow diagram for the algorithm is shown in figure 5.1.

Loading of the relay code into the target DSP board is an interaction between the host PC and target board. When the PC application launches on the host system, it first resets the target system, then it puts the relay code of the target system into the dual port memory. In the DSP target system, after being reset, the DSP moves the relay code out of the dual port memory. Then the PC application puts the settings into the dual port memory and the DSP loads the settings from the dual port memory. At this moment, the whole system setup has been completed and the relay begins to function.

The software structure of DSP board is simple. It only has one task and one interrupt. When the interrupt happens, the target system samples the voltages and currents and puts the samples into a buffer. After the interrupt is finished, the task takes the samples from the buffer and processes them with the PT relay algorithms.

8.2.2. The software of the Pentium system

8.2.2.1. The run-time architecture of the VRTXsa system

In the Pentium system, the software of the PT relay is programmed under a real-time executive operating system(VRTXsa), which is a commercial product of Microtec, Mentor Graphics Cooperation. The VRTX OS provides the system service API(application program interface) supports for the relay software development. Figure 8.3 shows the run-time architecture of the VRTSsa system.

A system based on VRTXsa x86/fpm is layered according to function, with each level making use of the functions provided by the level below. The system hardware occupies the lowest level. The next level contains the simplest, most hardware-dependent operating system functions; on top is the application.

Each level defines a virtual machine for the level above it. At higher levels, the functions provided by a software level are not distinguishable from those provided by the hardware. Each software

level adds several instructions to the processor's instruction set. For the application program, VRTXsa adds high-level instructions(system call) to the architecture of the microprocessor.

Level		Components				RTL
User		Application Program				
Software Runtime	OS	Other Microtec Components				RTL
		VRTXsa x86/fpm				
	Nanokernel	Nanokernel Libraries				
	Board Support	Process/Device-Dependent Libraries				
Hardware	Machine	CPU	Memory	FPU	I/O	CLK

Figure 8.4. The Run-Time System Architecture.

VRTXsa supports real-time systems with a set of basic multitasking mechanisms. The basic process object in VRTXsa is a task, a logically complete path of application code. A task is a collection of actions that deals with one issue asynchronously and in real-time. Physically, the task is a section of application code, for example a C procedure, that exists as a process only after it has been created and only until it is deleted from the system. A task executes subject to scheduling policies embodied in VRTXsa.

Several tasks can operate autonomously from the same piece of code, or tasks can be located in separate code modules. In a multitasking system, several tasks appears to execute simultaneously, although VRTXsa actually allocates CPU control among tasks in an interleaved fashion.

Tasks are active or inactive. Active tasks have executing, suspended, and ready task states; inactive tasks are dormant tasks. An application can have as many tasks as required. All active tasks have priority levels, and a configurable number of the active tasks can have unique identification numbers. VRTXsa moves tasks from one task state to another based on the priority level and as the result of system calls that cause rescheduling. Figure 8.5 shows four task states, the possible transition between states, and the event which triggers the transition.

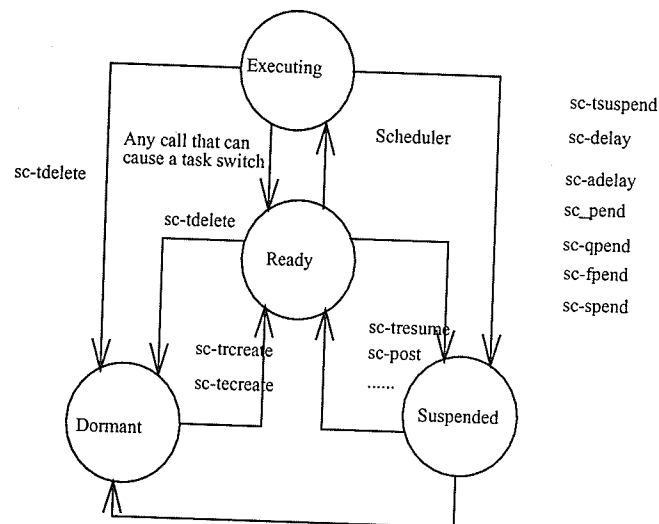


Figure 8.5. Task State Transition.

The circles in the figure 8.5 represent the possible states of a task. The arrow lines represent the switch path of task state. Beside the lines are the function calls which can trigger the state switch. The software of the PT relay for the Pentium system consists of the recording task, the command task and an interrupt handler. Two tasks run at the application level in the VRTXsa x86/fpm in run-time architecture. The interrupt handler is installed at board support level in the run-time architecture. The recording task runs in higher priority than the command task.

8.2.2.2 The recording task

The recording task is created by the relay application and never deleted. The recording task is a code loop. The first line code in the loop calls the `sc_qpend()` which puts the task in the suspended state after it is created.

Normally, the recording task is in suspended state and pending on an empty queue by calling the `sc_qpend()`. It becomes ready only when the queue is not empty.

In the PT relay algorithms, there are two reasons to post a message to the queue. The first, when the user issues a recording data command at the console, the command task posts a message to the recording queue. The second, when the PT algorithm detects an event which needs to be recorded, for example, a fault, the interrupt handler will post a message to the recording queue. The message

is posted to the queue by calling the `sc_qpost()`. This event triggers the recording task into the ready state.

The system scheduling procedure is invoked periodically by the system timer interrupt. When the system scheduler is executing, it selects the tasks in the ready state by the priority. The task with the highest priority will take over the CPU when system scheduling procedure is finished. In this system, if the recording task is in the ready state, it will move into the executing state and runs after the scheduling procedure. The system scheduler removes the first message in the queue.

If the recording task is in the executing state, it will save the recorded data into a file on the hard driver. After finishing saving, it calls the `sc_qpend()` and the system scheduling procedure is invoked. If there remain messages in the queue, the recording task runs again. The recording task release the CPU when the queue is empty.

8.2.2.3 The command task

The command task is created by the relay application and never deleted. The command task is a code loop. The command task is in charge of accepting and executing the user command and runs in a lower priority. The command task is normally in the executing state. When the system scheduling procedure happens and the recording task is in the ready state, it moves to the ready state. When the system scheduling procedure happens and the recording task is in the suspended state, it moves into the executing state from the ready state after the system scheduling procedure is finished.

At present, the relay calibration, data recording, and some debug functions have been implemented in the command task.

8.2.2.4 The interrupt handler

To allow different peripheral devices to generate interrupts on the CPU, the PCM-5862's bus has 16 different interrupt request (IRQ) lines. A transition from low to high on one of these lines generates an interrupt request which is handled by one of the AT's two interrupt control chips. One chip handles IRQ0 through IRQ7 and the other chip handles IRQ8 through IRQ15. The controller which handles IRQ8-IRQ15 is chained to the first controller through the IRQ2 line. When an IRQ

line is brought high, the interrupt controllers check to see if interrupts are to be acknowledged from that IRQ and, if another interrupt is already in progress, they decide if the new request should supersede the one in progress or if it has to wait until the one in progress is done. This prioritizing allows an interrupt to be interrupted if the second request has a higher priority. The priority level is determined by the number of the IRQ. Because of the configuration of the two controllers, with one chained to the other through IRQ2, the priority scheme is a little unusual. IRQ0 has the highest priority, IRQ1 is second-highest, then priority jumps to IRQ8, IRQ9, IRQ10, IRQ11, IRQ12, IRQ13, IRQ14, and IRQ15, and then following IRQ15, it jumps back to IRQ3, IRQ4, IRQ5, IRQ6, and finally, the lowest priority, IRQ7. This sequence makes sense if you consider that the controller that handles IRQ8-IRQ15 is routed through IRQ2.

The chips responsible for handling interrupt requests in the PCM-5862 are the 8259 Programmable Interrupt Controllers. The 8259 that handles IRQ0-IRQ7 is referred to as 8259A, and the 8259 that handles IRQ8-IRQ15 is referred to as 8259B.

The VRTX OS reserves IRQ0 and IRQ1 for OS usage, therefore the IRQ8 is assigned to sampling interrupt. The 8254 timer of the DM6420 is configured to generate the interrupt at rate 38400/sec(64 points/cycle) to invoke the sampling interrupt handler. When the sampling interrupt happens, the voltages and currents are sampled, and the sampled data is processed by the PT relay algorithm during this interrupt.

When a fault event is detected in the interrupt handler or the user issues a record command at the console, the interrupt handler begins to prepare the recording data. After the recording data is prepared, the interrupt handler posts a message to the queue on which the recording task is pending.

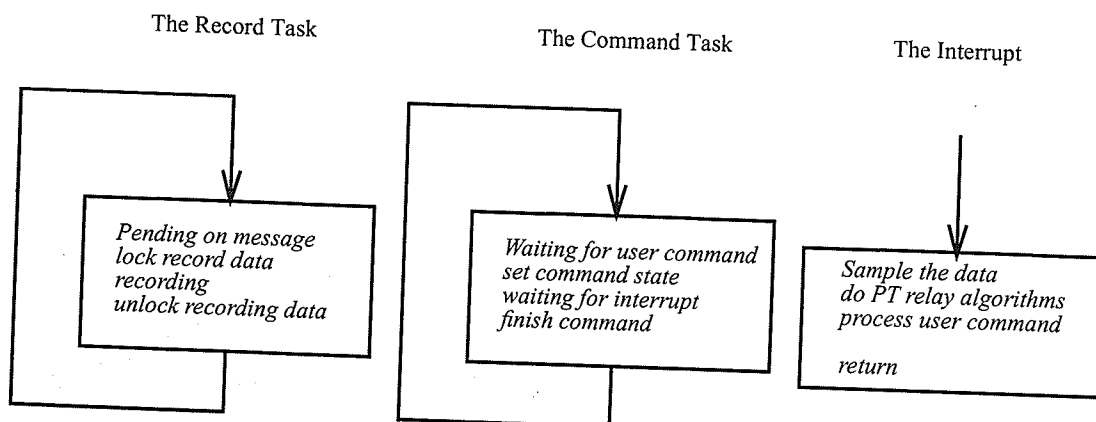


Figure 8.6. The Relay Software Flow Chart of Pentium System.

8.2.2.5. The processing of user command

A user may issue a command at the console. The command string is first received by the command task and then processed provided the command is recognized by the command task. Almost all the commands need to access data sampled or calculated by the interrupt handler. In the relay application, a synchronizing mechanism is employed in realizing the user command since the synchronized access of data is the typical concern in the real-time application.

The synchronization problem can be demonstrated by this example in which a simple command is used to show the sampling data. If the task directly displays the data in the sampling buffer, the data will change during the displaying procedure because a sampling interrupt happens. This situation may happen in other conditions. To prevent the unwanted data discrepancy, the command states are implemented in the software.

To provide a solution for the above example, a global variable is used to represent the command state, and the command can be in one of the three states: idle, active, and done state.

Normally the command is in idle state. In the command task, when the user issues the command, the state is change from an idle state into an active state in the task. The command task then enters the loop to check the command state. The loop will be broken if the command state is not active. In the sampling interrupt routine, the command state is checked. If the command state is active, then the CPU copies the samples into the buffer provided by the command and changes the state variable to a done state. In the command task, the loop is broken since the command is in a done state. The command task then displays the samples in its buffer and change the command state into an idle state.

The above is the possible scenario for processing a simple command. Some commands may involve more states. For example, to process the calibration command, the command task instructs the interrupt handler to provide the calculated RMS value of the voltages and currents. Then the user inputs the expected RMS value of the voltages and currents and instructs the interrupt handler to calculate the calibration coefficients and put the results into the buffer provided by the command, and the command task saves these coefficients. In such a situation, using more states is the solution to process the command. The whole idea of the mechanism is peddling the command state from one to the other by the command task and interrupt handler, and each of them can do something only in the designated states. This mechanism ensures the expected sequence of

processing the command. Figure 8.6 shows the flow chart for processing a command.

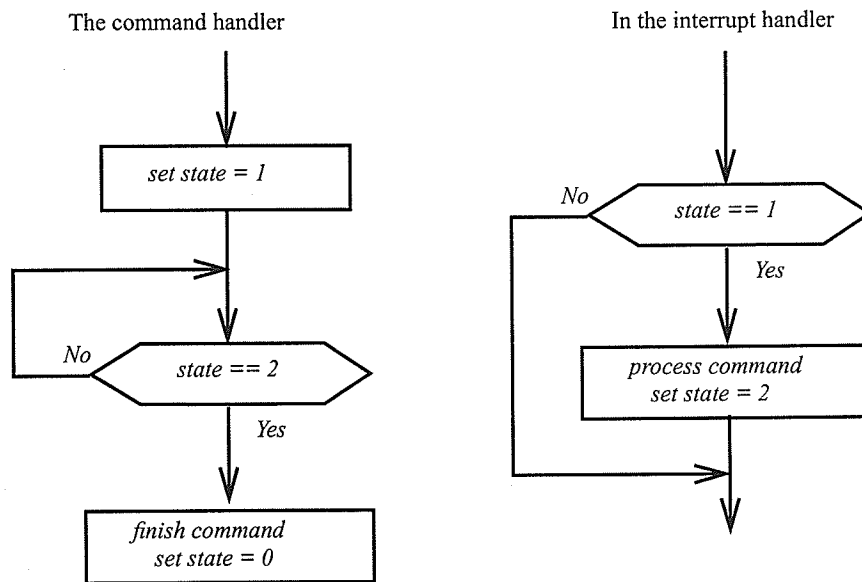


Figure 8.7. The Command Processing of The Pentium System.

This model is widely used in processing the user command.

8.2.2.6. The configuration of the relay application

Configuring the relay application with the VRTXsa operating system is referred to as the system configuration. The Xconfig utility provided by Micritec is an automatic configuration utility which assists the developer in defining the system parameters. During this process the developer sets system parameters which determine:

The characteristics of the target hardware,
specific operating system feature the application needs to use,
control of the make process.

The Xconfig utility reads these system parameters from a set of definition files and uses these parameters to convert a set of template files into C language files, a make file, and command files to the binder and builder utility, which are customized for a particular target environment and system configuration.

Output files from the Xconfig are used by the make process to build an absolute system image. The C language files are compiled, linked with the application code including the required system libraries, and located to a specified absolute location.

The system parameters that are provided to the Xconfig are in the form of variables that specify information required by the various system modules in the application. The hardware characteristics and operating system features are determined by these parameters. For example, the CPU type on the target hardware, the presence of the floating co-processor, the memory size, and the physical system input and output device can be determined by these parameters. The set of input files required by Xconfig is as follows:

A set of default configuration files.

A set of template files.

Project configuration file that the developer provides to change default values or add new configuration variables.

The following figure shows an example of a standard Xconfig configuration process.

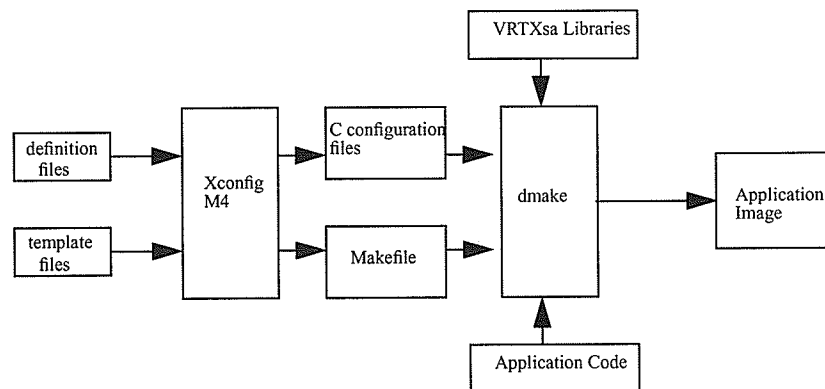


Figure 8.8. Xconfig Configuration Process(Default Image).

8.2.2.7. The cautions for the developer

1. Do not access the sampled or calculated data directly. When the data shared between the task and interrupt is accessed, always use the state transition mechanism.
2. VRTXsa provides a file system to support the developer to make use of the floppy drive and hard drive. To use the file system, the developer should always open file 0,1 and 2 first in every task.

Every task has the stdin, stdout, and stderr which correspond to file 0, 1, 2. After these three files are opened, the task can create the file it needs. Any attempt to open a file before file 0, 1, 2 in the task can cause unexpected problems.

3. Do not do floating point computation in the task if you do it in the interrupt. The floating coprocessor is not reentrant. If the floating point computation is under way in the task while the interrupt happens, the interrupt preempts the task. When the interrupt does the floating point computation, the internal registers of the floating coprocessor may not in be the initial state, hence unexpected problems may happen.

4. Do not create large data structures in the stack in the interrupt. If you do need the large data structure, define it as the global variable. The interrupt handler uses the stack of the task it interrupts. The interrupt handler is never aware of the size of the task stack, thus it may cause the run-time stack to overflow.

5. Be careful with the system call and run-time library function provided by VRTXsa when calling them in the interrupt. Only call the function permitted by the VRTXsa in the interrupt. Calling a unpermitted function in the interrupt may cause the system to crash or hang. For example, calling the printf(), sc_lock() may cause a problem in the system.

6. Keep in mind that when a user command is issued at the console or a task generates an output to the console or accesses the hard drive or floppy drive, the VRTXsa may disable the system interrupt to synchronize the system procedures involved in these commands. These commands may cause the relay to lose points of samples.

8.3. Cases of the PT relay

The relay algorithm structure of the two applications are shown in figure 4.1.

We used a case recorded in the PSCAD simulation to test the PT relay. The case is the three phase forward fault in fig5.14. In the PSCAD simulation, the runtime data of voltages and currents are saved into a file. The playback software developed by the Manitoba HVDC Research Center is used to reproduce the voltages and currents based on the simulation recorded data. The playback software runs on a PC. It interprets the simulation data file and instructs a D/A hardware to convert the data into analog signals which represent the currents and voltages. The relay samples the voltages and currents produced by the playback system and then its algorithms are tested.

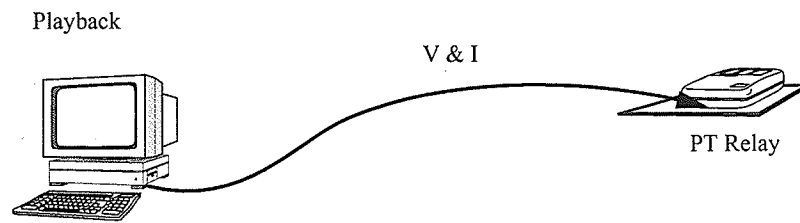


Figure 8.9. The Realtime Application Environment.

The adaptive feature of the PT relay in mode 1 was closely investigated. The investigation of the adaptive feature is shown in figure 8.10. The case was recorded by the TMS320 application. The variation of the protection zone of the PT relay vs time is displayed in figure 8.10 to figure 8.13.

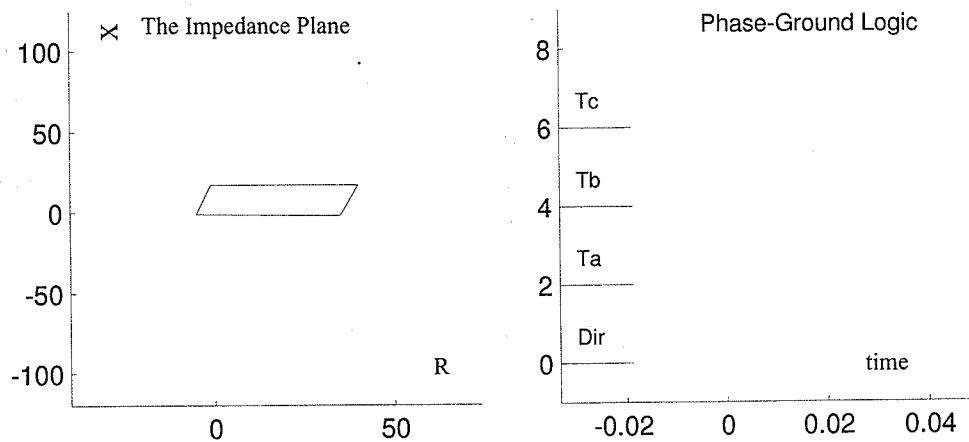


Figure 8.10. The Adaptive Feature of PT Relay.

Figure 8.10 shows the protection zone of the PT relay before the fault. The PT relay's trip zone has not expanded.

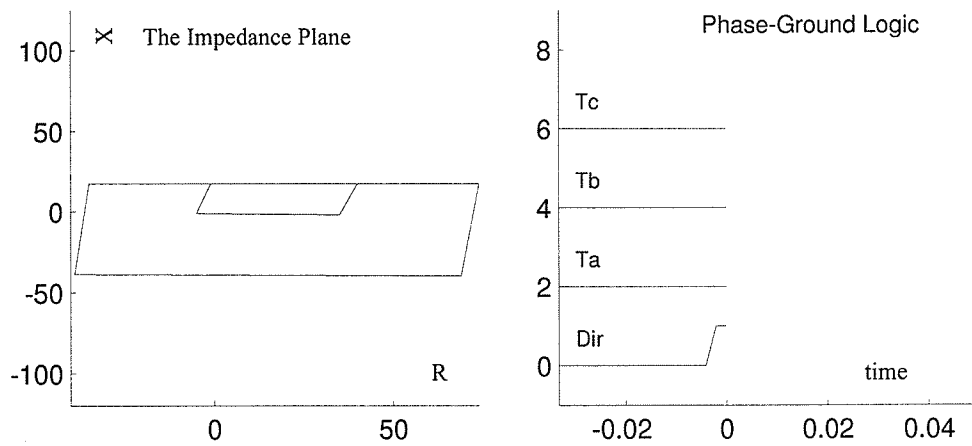


Figure 8.11. The Adaptive Feature of PT Relay.

Figure 8.11 shows the protection zone of the PT relay which has fully expanded. It takes about 4ms for the trip zone to expand. At this moment, the measured impedance trajectories remain outside of the scope of the graph.

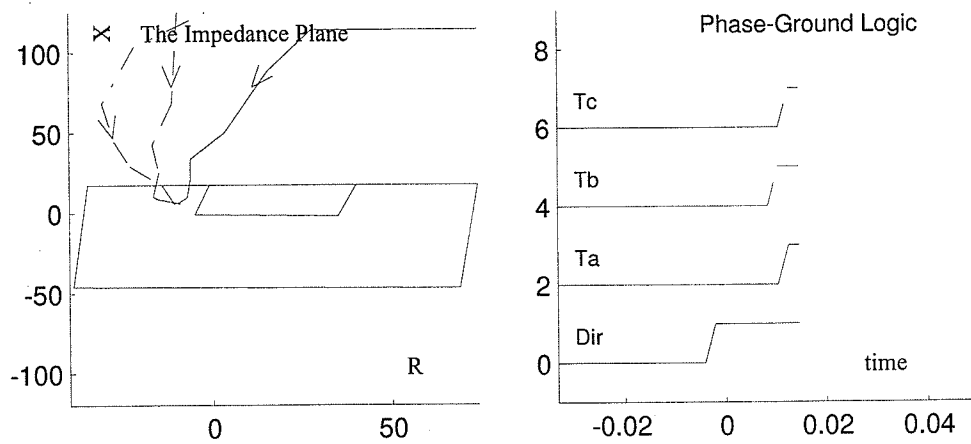


Figure 8.12. The Adaptive Feature of PT Relay.

Figure 8.12 illustrates the moment when the impedance trajectories just come into the dynamic protection zone of the PT relay.

Figure 8.13 illustrates the moment the impedance has just entered the setting zone of the PT relay,

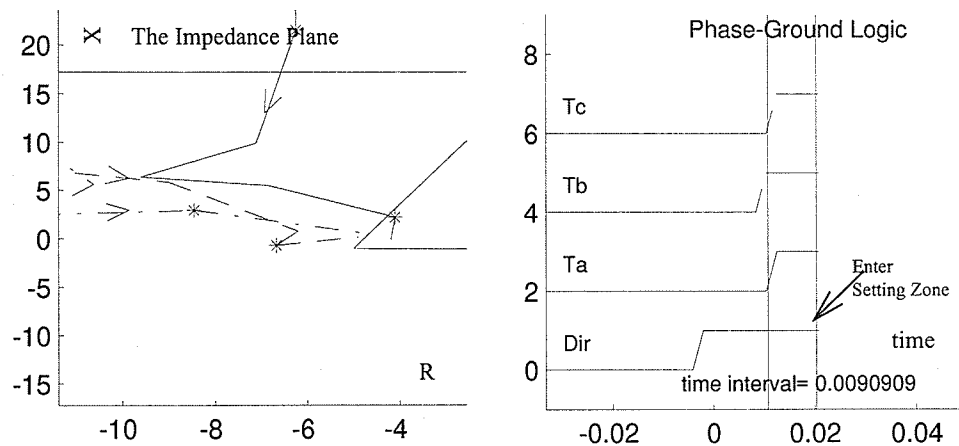
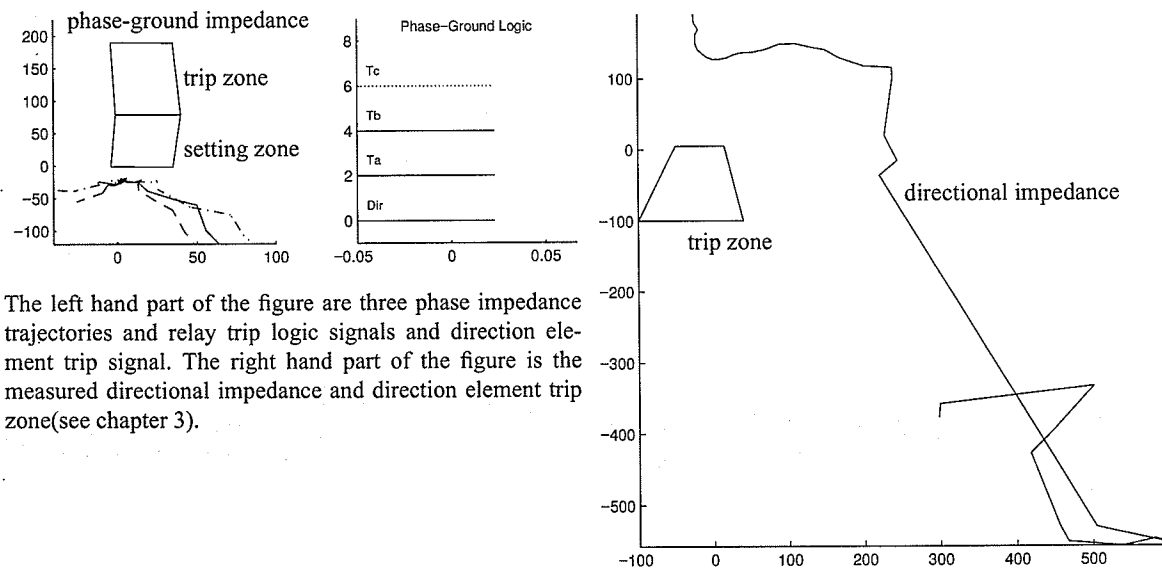


Figure 8.13. The Adaptive Feature of PT Relay.

which is also the protection zone of a conventional quadrilateral relay. In the right part of the graph, the phase-ground logic graph shows that the time interval between the time the impedance entered the dynamic protection zone of the PT relay and the time the impedance entered the setting zone (which is about 9ms). This is a significant advantage over the conventional quadrilateral relay.

8.4. Cases from the 500KV dorsey-forbes system



The left hand part of the figure are three phase impedance trajectories and relay trip logic signals and direction element trip signal. The right hand part of the figure is the measured directional impedance and direction element trip zone (see chapter 3).

Figure 8.14. The Reverse Field Fault Case on Dorsey-Forbes 500KV System.

Figure 8.14 shows a cases of the PT relay in a revers fault of the 500KV system. The playback uses the recorded voltages and currents in the case of figure 1.7 to test the PT relay. The trip zone is flipped up.

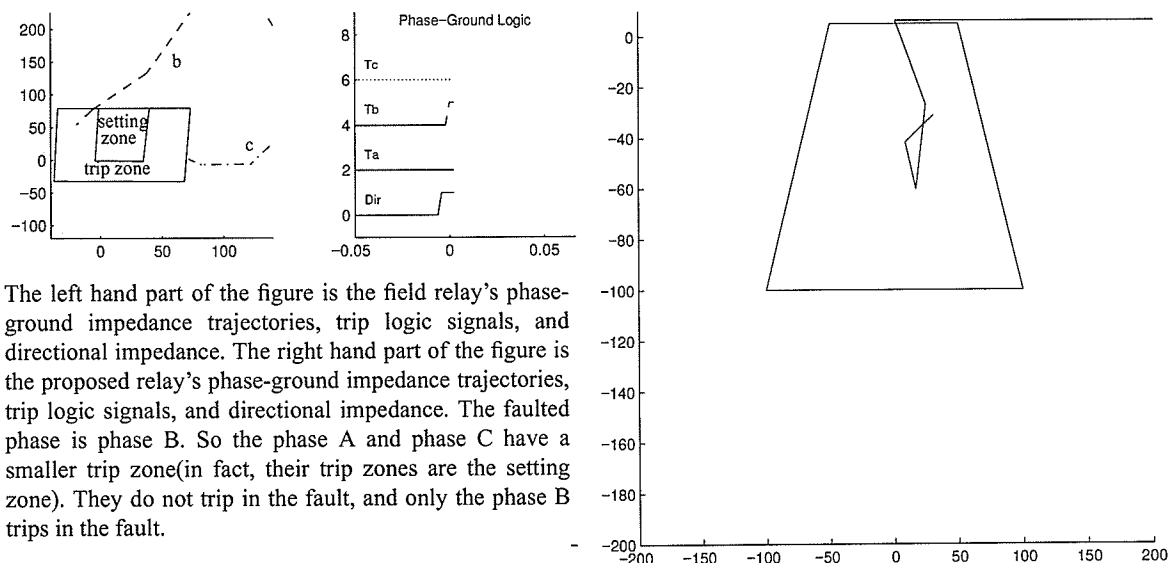


Figure 8.15. The Forward Field Fault Case on Dorsey-Forbes 500KV System.

The case in figure 8.15 is produced by using the voltages and currents of the case in figure 1.9 to test the PT relay. The trip zone of the directional element stretch into the forth quadrant comparing to that in figure 1.9.

8.5. Comparison of the TMS320C32 & Pentium system

The comparison of the two relay platforms focuses on the following aspects: software programming, hardware capability, cost, and operating system selection.

Most of the application code is written with the C language in both systems and a minor part of the code is written with the hardware dependent assembly language. To make sure that they can be compiled for a different platform, the developer must follow a few simple rules in declaring and using variables. Variable declaration is important, because different implementations of the C language use different lengths for integer variables. For example, implementations of C for some processors uses 32 bits while for other processors uses 16 bits.

Both the TMS320 and the Pentium have powerful floating computational capability which allows

them to finish the relay's complicated computations in real time. From the hardware point of view, they are both capable of satisfying the real time demands of the power system protective relay.

In the TMS320 system, the hardware involves a PC and a TMS320 DSP board. The cost of such an application can be reduced by eliminating the PC and realizing the relay in stand alone hardware.

The operating system(OS) is an important consideration when a relay is designed. Many commercial real time OS products are available for either the TMS320 or the Pentium system. However, it is hard to find an OS which is very suitable for the relay. Many real time applications only need to handle the external event in a reasonable time. An OS like VRTX can satisfy this kind application, such as a network router. But the power system relay requires a rigid sampling rate, which means the sampling interrupt must have the highest interrupt priority and can not be disabled at any time. Many OS can not satisfy the demands of the relay application. Normally in an OS, the system timer has the highest interrupt priority. Moreover, in the interrupt handler coming with the OS, the CPU may disable the interrupt while the CPU processes an interrupt, and this means an interrupt with a priority lower than the sampling interrupt could also disable the sampling interrupt. The Pentium has a very complicated memory access mechanism. When a Pentium CPU runs in the protected mode, global descriptor, local descriptor, two level page table, and interrupt descriptor are used to access the code and data. The management of these descriptors is very complicated. When an OS like VRTX is used, this detail is covered by the OS. The TMS320 uses a simple memory access mechanism which makes a start from scratch easy.

In the Pentium system, it is found that when a user issues a command at the console or the VRTX accesses the hard disk, the VRTX may disable the system interrupt briefly in order to synchronize some system procedures. This fact constitutes a challenge to the idea that a Pentium alone undertakes a relay task since the VRTX operating system can not ensure the Pentium system maintains the sampling rate constant. There are two solutions for this problem: the first, dedicating the Pentium board for the relay algorithm and using another CPU do the back ground chores for the Pentium CPU. The second, creating a simple and customized operating system for the relay which may allow the Pentium system to be a stand alone relay.

Chapter 9. Conclusions And Future Work

9.1. Conclusions

In this thesis, the adaptive PT relay model is presented. The components of the PT relay are investigated in detail in the PSCAD/EMTDC simulation. To test the PT relay, the PSCAD/EMTDC simulation model and the MATLAB model embedded in the PSCAD/EMTDC simulation are created. The PT relay is also realized in two hardware platforms, one is the TMS320 DSP board, another is the Pentium based board. To investigate the PT relay's performance, the PT relay and the Mho relay, and the simple quadrilateral relay are tested together in the PSCAD/EMTDC simulation.

This work leads to the following conclusion.

1. The direction element of the PT relay distinctly classifies the fault direction.

The positive sequence incremental impedance is always available in the system fault. Theoretically, the impedance is the negative of the positive sequence impedance from the relay to the local source in the forward fault and is the positive sequence impedance from the relay to the remote source in the reverse fault. The difference of the positive sequence incremental impedance in the reverse fault and in the forward fault is the total positive sequence impedance between the system sources. This is the foundation to employ the positive sequence incremental impedance to classify the fault direction. Other incremental sequence or phase impedance is either not always available or not converged in different fault types. Chapter 4 gave a detailed analysis of the direction element.

2. The phase selection algorithms of the PT relay quickly and correctly identify the fault type.

The simulation in Chapter 5 illustrates, in the worst case, that the PS element can identify the fault type correctly in 10ms. In a normal fault, a quadrilateral relay can not trip in 10ms, so that the PT relay can be improved from the response of the phase selection.

3. The PT relay performs well.

Chapter 3 gives the theory of the PT relay, chapter 4 and chapter 5 have very detailed simulation tests of the components of the PT relay model, and Chapter 6 tests the whole PT relay. The PT relay works as expected in these test.

4. The PT relay performs better than the Mho relay to protect a transmission line.

Chapter 6 demonstrates a series of cases. In most of these inductive-dominated cases, The PT relay in mode 1 is proved to perform better than or as well as the polarized Mho. The PT relay provides the trip signal faster than a Mho in most cases. In the non-inductive-dominated cases, the Mho relay may fail in the fault, but the PT relay in mode 2 always demonstrates correct action.

5. The PT relay performs better than the simple quadrilateral relay to protect a transmission line. In most cases of chapter 6, the impedance trajectory traverses into the dynamic trip zone first and into the setting zone later. This means that the PT relay provides quicker fault clearance than the simple quadrilateral relay.

6. The TMS320 & Pentium processor are suitable to run the PT relay algorithm.

Chapter 7 presents demos based on the TMS320 and Pentium processors. Both the TMS320 and Pentium processor can handle the complicated PT relay computation. However, the Pentium board alone can not be used as a stand alone relay unless the specific operating system is developed.

9.2. Future Work

Some work is still required to be done about this project in future:

1. Implement a graphic tool to configure the algorithm in a field relay.

At present, the relay algorithm running on the Pentium or DSP board is manually coded. A graphic tool, similar to PSCAD, can allow the versatile sophisticated algorithm to build up gradually and can offer the relay engineer more flexibility to configure the field relay.

2. Build a stand alone relay hardware.

Such a hardware will have two CPUs on one board. One is dedicated to the relay algorithm, and the other is designated to do background tasks, such as communication with the external world. Such an implementation of the relay will be smaller and less expensive than a DSP board embedded in an industrial grade PC. A serial port may serve as the communication window.

Appendix A

1. The Z_{e1} and Z_{ec} in the forward ABC fault:

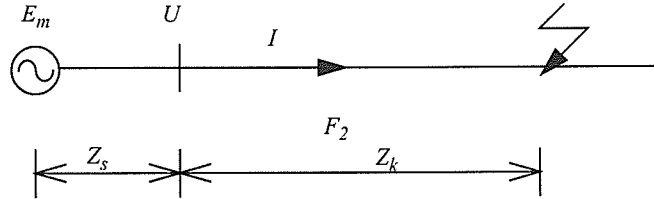


Figure A.1. The forward fault

Figure A.1 shows a forward fault. Figure 2 shows the prefault system voltage.

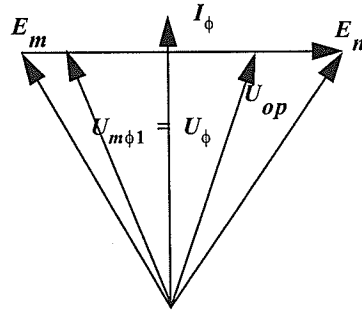


Figure A.2. The prefault system condition

Before the system fault, the $U_\phi = U_{m\phi1} = U_{c\phi}$, so the equation A.1 is true.

$$Z_k = Z_{e1} = Z_{ec} = \frac{U_\phi}{I_\phi} \quad \text{A.1}$$

During the fault, the $U_{m\phi1}$ keeps its prefault value which is constant. The $U_{m\phi1}$ can be expressed in terms of the left hand system source as shown in figure A.2.

$$U_{m\phi1} = r \cdot E_m \quad \text{A.2}$$

As show in the figure A.1, the equation A.3 is true.

$$E_m = U_\phi + I_\phi Z_s = I_\phi (Z_k + Z_s) \quad \text{A.3}$$

If we substitute the equation A.2 into equation A.1, equation A.4 is obtained.

$$U_{m\phi 1} = r \cdot E_m = r \cdot I_\phi (Z_k + Z_s) \quad \text{A.4}$$

The Z_{e1} can be calculated by equation A.5.

$$Z_{e1} = U_{m\phi 1} / I_\phi = r \cdot (Z_k + Z_s) \quad \text{A.5}$$

In the three phase fault, the cross polarized voltage equals the phase voltage.

$$U_{c\phi} = U_\phi \quad \text{A.6}$$

The Z_{ec} can be calculated by equation A.7.

$$Z_{ec} = U_{c\phi} / I_\phi = Z_k \quad \text{A.7}$$

2. The Z_{e1} and Z_{ec} in the reverse ABC fault:

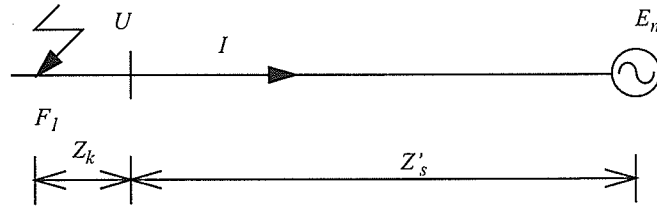


Figure A.3. The Reverse Fault

In the reverse fault, equation A.8 is true.

$$U_{m\phi 1} = r \cdot E_n \quad \text{A.8}$$

$$E_n = U_\phi - I_\phi Z_s = I_\phi (Z_k - Z_s)$$

The Z_{e1} can be calculated by equation A.9.

$$Z_{e1} = U_{m\phi 1} / I_\phi = r \cdot (Z_k - Z_s) \quad \text{A.9}$$

The Z_{ec} can still be calculated by equation A.7.

Appendix B

In the system in figure 2.3, suppose there is a fault at F2, and the positive sequence impedance from source E_m to F2 is Z_{m1} , from source E_n to F2 is Z_{n1} . The negative sequence impedance of the system equals the positive sequence impedance. Z_{m0} and Z_{n0} are the zero sequence impedances of the system on either side of the fault point F2.

1. The incremental current of the AG fault

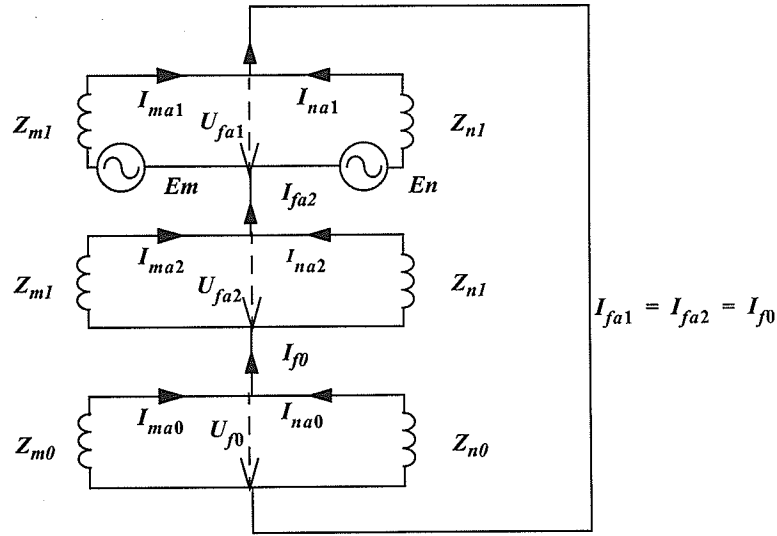


Figure B.1. The Sequence Networks in the AG Fault

In an AG fault, the voltage and current at the fault point are subject to the constraints: $U_{fa} = 0$, $I_{fb} = 0$ and $I_{fc} = 0$. When the abc-120 transformation is applied to them, the boundary condition of the 120 sequence network is: $I_{fa1} = I_{fa2} = I_{f0}$ and $U_{fa1} + U_{fa2} + U_{f0} = 0$. These boundary constraints indicate that the three sequence networks are connected in series, as in figure B.1.

The current in the sequence network is actually composed of two parts: the prefault load flow component and the fault injection component. The prefault current in the negative and zero sequence networks is zero. The prefault current in the positive sequence networks is the load current. Provided we bypass the electrical sources in the circuit and replace the fault current injected into the positive sequence network at the fault point with a current source of the same amplitude

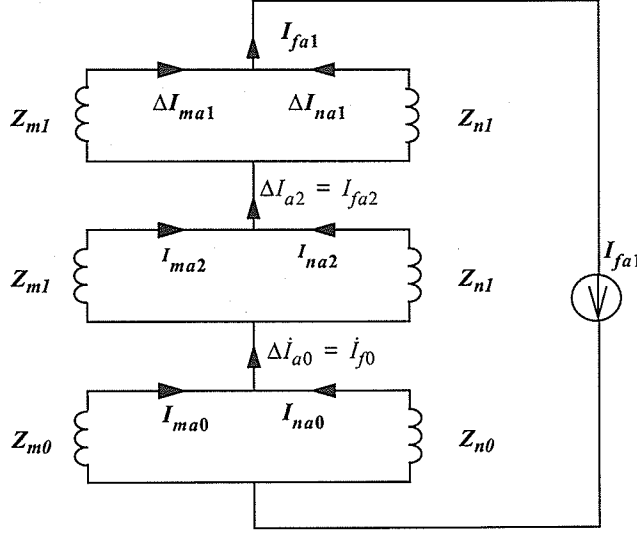


Figure B.2. The Incremental Currents in the Sequence Networks in the AG Fault and phase angle, the currents flowing in the sequence network are the incremental sequence currents, as shown in figure B.2.

Since the impedance parameter in the positive and the negative sequence networks is the same, the current distribution is also the same in the positive and negative sequence network. In the AG fault, we can conclude that $\Delta I_{ma1} = I_{ma2}$.

2. The incremental current of the BC fault

The voltage and current at the fault point are subject to the constraints $I_{fa} = 0$, $I_{fb} + I_{fc} = 0$ and $U_{fb} = U_{fc}$. After the abc-120 transformation is applied, the new constraint: $I_{f0} = 0$, $I_{fa1} + I_{fa2} = 0$ and $U_{fa1} = U_{fa2}$ are found. The new constraint indicates that the positive and negative sequence networks are connected in parallel at the fault location and the zero sequence network is not involved in the connection. Since there is no generator in the zero sequence network, there is no zero sequence current in the fault. When the incremental currents in the sequence networks are considered alone, the voltage sources are bypassed in the positive sequence network and the fault injection current is replaced by a current source, as in figure B.3.

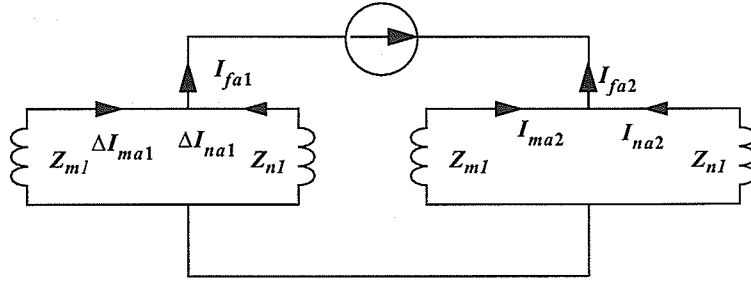


Figure B.3. The Incremental Currents in the Sequence Networks in the BC Fault

From the sequence network topology, we know that in a BC fault, the incremental positive sequence current and negative sequence current are subject to the constraint $\Delta I_{ma1} = -I_{ma2}$.

3. The incremental current of the BCG fault

For a BCG fault, the voltage and current at the fault point are subject to the constraint $I_{fa} = 0, U_{fb} = U_{fc} = 0$. After the abc-120 transformation to the constraint is applied, the result is $I_{fa1} + I_{fa2} + I_{f0} = 0$ and $U_{fa1} = U_{fa2} = U_{f0}$. The sequence network topology which satisfies the constraints is a parallel connection of all three sequence networks. When the incremental currents in the sequence networks are considered alone, the voltage sources are bypassed in the sequence network and the injection branch is replaced by an equivalent current source.

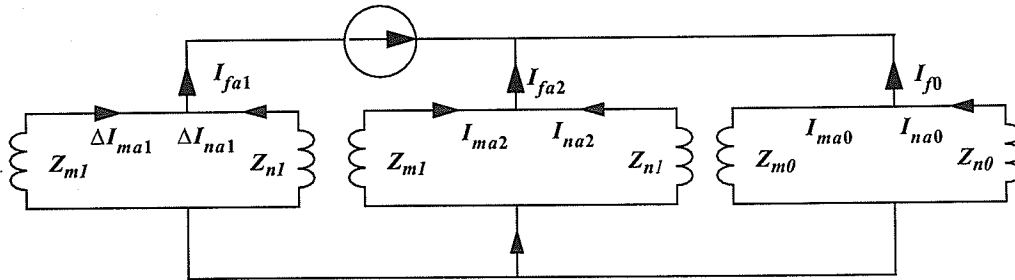


Figure B.4. The Incremental Currents in the Sequence Networks in the BCG Fault

From figure B.4, we know that the negative sequence current is some proportion of the incremen-

tal positive sequence current $I_{ma2} = \lambda \Delta I_{ma1}$, $-1 < \lambda < 0$ in the BCG. λ will depend on the proportion of the injection current which flows into the negative sequence network.

4. The incremental current of the ABC fault

For ABC fault, the voltage and current at the fault point are subject to the constraint $U_{fa} = U_{fb} = U_{fc} = 0$. After the abc-120 transformation is applied, the result is $U_{fa1} = U_{fa2} = U_{f0} = 0$. This result shows that the three sequence networks are isolated from each other. The negative and zero sequence current in the network is zero since there is no generator in the negative and zero sequence networks.

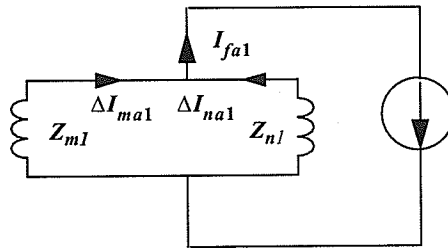


Figure B.5. The Incremental Currents in the Sequence Networks in the ABC Fault

When the incremental currents in the sequence networks are considered alone, the voltage sources are bypassed and the fault injection current is replaced by an equivalent injection current source. So, the conclusion is that $I_{ma2} = 0$.

Appendix C.

This section introduces the major subroutines and files developed or revised for this thesis.

1. Fortran subroutine for PSCAD/EMTDC simulation:

PhSlct(...) is developed to identify the fault phase.

BndRly(...) is developed to implement the IE element of the PT relay.

LdImp(...) is developed to produce the prefault load impedance.

DIR642(...) is used to calculate the positive sequence increment impedance and revised.

UopSyn(...) is developed to produce the S2 signal for the Mho relay.

U1Plrzd(...) is developed to produce the S1 signal for the Mho relay

CirMho(...) is developed to implement the phase-comparator for the Mho relay.

2. MATLAB files for the PSCAD/EMTDC simulation:

BPdecim.m is developed to implement the bandpass filter.

LoadImp.m is developed to produce the load impedance.

PTImp.m is developed to implement the IE element of the PT relay.

PhSlct.m is developed to implement the PS element of the PT relay.

ZPosDIr.m is developed to implement the DI element of the PT relay.

Sampler.m is developed to sample the simulation waveforms.

MatFig.m is developed to show the dynamic feature.

3. Software revised for the DSP board:

CB8D.c is revised to incorporate the PT algorithm in the field relay.

4. Software developed for the Pentium board:

Many files for the DSP board are revised for the Pentium board.

5. Software developed to analyse the PT dynamic feature off-line.

Viewer.m and some auxiliary programs are developed to analyse the relay recording.

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