Fault Detection, Discrimination, and Recovery in Multi-Terminal HVDC Transmission Systems

By

Naushath Mohamed Haleem

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Department of Electrical and Computer Engineering
Faculty of Faculty Engineering
University of Manitoba
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Abstract

Multi-terminal high voltage direct current (MT-HVDC) grids enable integration of large-scale renewable energy resources and facilitate flexible bulk power transfer for energy markets extending over political boundaries. Preserving the integrity of MT-HVDC grids during DC faults remains a major challenge, primarily due to the lack of effective DC circuit breakers (DCCBs) capable of interrupting the expected fault currents. These DCCB limitations and stringent reliability requirements mandate identification of faulted transmission lines and the faulty conductors at extreme speeds with highly sensitivity.

Two techniques were developed to improve the sensitivity and the reliability of fault discrimination while meeting these speed requirements. The first technique introduces directional properties for line and bus protection algorithms that rely on the rate of change of local voltage measurements to improve the fault discrimination. The second technique uses locally measured conductor currents to quickly identify the fault type and faulted conductors. This algorithm makes the decisions based on the ratios of the rate of change of currents computed considering a pair of conductors at a time, and therefore, independent of the fault resistance. Versatility and reliability of the proposed fault type discrimination algorithm was demonstrated by applying it to different transmission configurations.

Fault recovery aspects of a novel class of hybrid LCC-VSC MT-HVDC transmission systems in which a number of VSC inverters and rectifiers are connected to an LCC HVDC link was investigated. Two possible fault clearing schemes were proposed. The first approach avoids

DCCBs, employs series-connected high power diodes at VSC inverter terminals to block the fault current contributions, and clears faults by de-energizing VSC rectifiers and applying force retardation to LCCs. The second approach utilizes DCCBs installed on the branch lines. These DCCBs activated by the proposed fault discrimination schemes minimize the disruption of power flow through the LCC HVDC link due to faults on the lines branched out to connect VSCs. The capability, speed, and sensitivity of each fault clearing scheme were evaluated considering practical designs.

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List of Abbreviations

AC	Alternating current
ADC	Analogue-to-digital converter
CB	Circuit breaker
DC	Direct current
DMR	Dedicated metallic return
EMT	Electro-magnetic transient type
EMTP	Electro-magnetic transient type program
FMSW	Fast mechanical switch
GND	Ground
HB-SM	Half-bridge sub-module
HVAC	High voltage ac
HVDC	High voltage dc
IED	Intelligent electronic device
IGBT	Insulated gate bipole transistors
LCC	Line commutated converter
LPF	Low pass filter
MMC	Modulo multi-level converter
MPC	Master power controller
MT-HVDC	Multi-terminal high voltage dc
PSCAD®	Power system computer aided design
OHL	Overhead line
ROCOC	Rate of change of current
ROCOV	Rate of change of voltage
STATCOM	Static synchronous compensator
VSC	Voltage source converter

Chapter 1

Introduction

1.1. Background and Motivation

Functional requirements of the large interconnected power transmission systems that deliver electricity from the remote and renewable sources to load centers stretch beyond the capability of high voltage alternating current (HVAC) power transmission [1-3]. High voltage DC transmission (HVDC) is the preferred choice for bulk power transmission between very long distances and when it is required to cross water bodies [4]. For example, Rio Madeira transmission link in Brazil transfers about 7000 MW along 2,385 km transmission line and Jinping-Sunnan HVDC link transfers 7200 MW between two converter stations 1935 km apart [5]. When it is needed to extract energy from multiple energy resources dispersed in a large geographic area and share among load centers located far apart, two-terminal HVDC systems cannot be used. Therefore, multi-terminal high voltage direct current (MT-HVDC) grids are proposed [6-7] for future continental bulk power transmission.

The world's first VSC based three-terminal HVDC grid, Nanao HVDC grid, was commissioned in 2013 [8-10] and the first five-terminal VSC-HVDC grid, Zhoushan MT-HVDC,

was placed in service in 2014, [11-13]. Zhangbei four-terminal HVDC grid, which will be the world's first large scale MT-HVDC grid, will be commissioned in 2022 [14-17]. Some other MT-HVDC proposals include European Super Grid [18-19] and Atlantic Wind Connection [20] . Several HVDC converter stations in Europe are designed with provisions for connecting to a future MT-HVDC grid [21].

The expected benefits of MT-HVDC are increased redundancy [4], increased flexibility for power trading [4, 22], and lower investment and operational costs [22]. Furthermore, MT-HVDC grids will play a key role in renewable energy integration since MT-HVDC grids enable interconnecting dispersed green resources distributed over large geographic area to load centers located beyond single political boundaries [2-4]. A great contribution to the future clean energy goals is expected from the enormous energy potential of offshore wind. Therefore, offshore wind energy generation plays a key role in satisfying the ever-growing energy demand without affecting the sustainability of the environment. Submarine cables are inevitable in bringing electrical energy generated in offshore to onshore grids, and when the distances are longer than a few hundred kilometers, HVDC cables are the only technically feasible option. Therefore, MT-HVDC technology is being seriously considered for connecting offshore wind farms.

In order to achieve the true advantage of a large MT-HVDC grid transporting bulk energy, it is essential to have the capability of preserving the integrity of the grid during transmission system faults. DC fault protection of MT-HVDC grids is of utmost importance to ensure the safety of equipment [23], attain the full reliability benefits of MT-HVDC grids [24], and to preserve the stability of power system. However, DC side fault protection remains a main challenge in securing the smooth operation of the MT-HVDC grids already in operation, and for the development of high capacity MT-HVDC grids [25]. This is because the current increases rapidly during a DC

side fault in HVDC transmission systems and therefore, the faulty section of the transmission line should be isolated within a very short interval [26].

1.1.1 Converters Used in MT-HVDC Grids

Two main converter technologies, line commutated converters (LCCs) and voltage source converters (VSCs) implemented using multi-level modular converter (MMC) technology, are utilized for HVDC transmission [2, 27]. The type of electronic switching device used in LCC converters is thyristors while IGBTs are used in VSC stations. The VSC technology enables the realization of MT-HVDC grids by offering the flexibility in changing power flow direction and the possibility of connecting to weak AC systems [27-28]. The DC voltage in an MMC is created by inserting a number of charged capacitors, called sub-module capacitors, with the help of power electronic switching devices. A sub-module capacitor together with the associated electronic switches is called a sub-module. As depicted in **Fig. 1.1,** each arm connected to each phase of AC supply is made up by connecting a number of independent switching modules (SM) [29], each of which is capable to withstand only a fraction of the arm voltage.

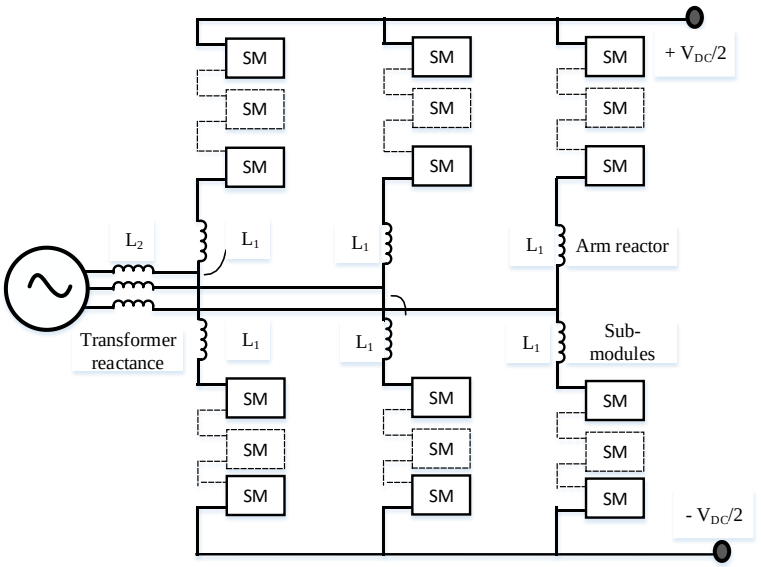


Fig. 1-1. MMC VSC station

Although a number of improved SM configuration can be found in literature, they are practically implemented using half-bridge or full-bridge submodules shown in **Fig. 1.2** [30].

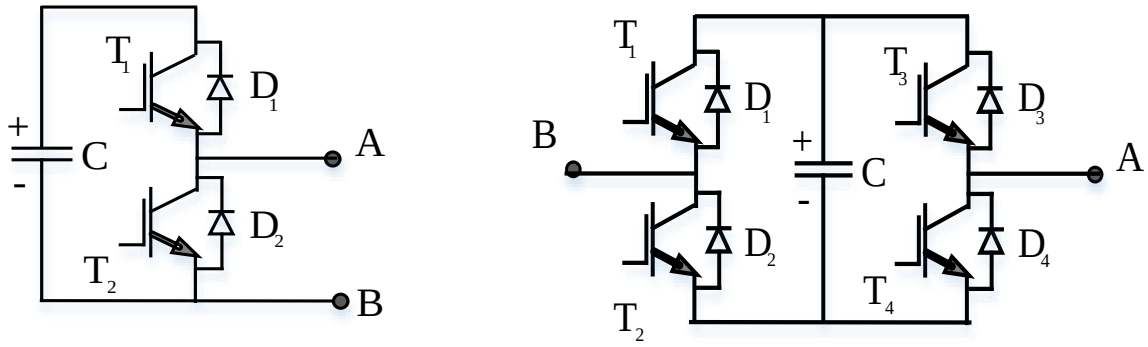


Fig. 1-2. Submodules, (a) Half- bridge sub-module (HBSM), (b) Full bridge submodules (FBSM)

The capacitor voltage is maintained nearly constant using a voltage balancing mechanism. Therefore, the capacitor is used as a constant voltage source [31]. As it can be seen from **Fig. 1.2**, half-bridge MMC station requires only half of the number of power electronic switching devices that are required for a full-bridge converter station [32]. Therefore, due to lower capital cost and switching loss, most of the practical VSC based HVDC systems use modular multilevel converter (MMC) technology based on half-bridge sub-modules [32].

During a DC side fault, sub-module capacitors discharge rapidly into the transmission line and therefore, fault current rises very rapidly [4, 33]. The inherent weakness of the MMC-VSC HVDC systems based on half-bridge switches is the inability block fault currents during a DC side fault [34]. Hence, it is required to promptly isolate the faulty section to sustain the converter operation. However, fault isolation requires few sub-functionalities and all sub-functions are required to be completed within a very short interval [35-36]. This is challenging as described in the next section.

1.1.2 Protection Requirements of MT-HVDC Grids and Challenges

The availability of more than one possible path is a key reliability feature of MT-HVDC grids when compared with a two-terminal transmission system. In order to facilitate power transfer through the healthy transmission line(s) when more than one transmission line is connected to a bus, only the transmission line involved in the fault should be isolated [33]. Therefore, fault clearing involves identification of the faulty transmission line or sections of a transmission line that are separated by isolating devices such as DC circuit breakers (DCCB). However, a strong transient can be created on a healthy transmission line when a DC side fault occurs in another transmission line connected to the same bus, during the reverse faults, or during the opening of a DCCB on an adjacent line to clear a fault. Discriminating close-up reverse faults from the forward faults in the protected transmission lines within a short time interval is one of the protection challenges of future MT-HVDC grids.

The configuration of HVDC transmission that uses two conductors, termed pole conductors, kept at the same voltage magnitude and opposite polarity is called bipole HVDC transmission configuration. Having a third conductor, called dedicated metallic return conductor (DMR), improves the reliability [37] as described below and therefore, is considered to be the most likely MT-HVDC transmission configuration [38]. During normal operation, the metallic return wire carries a zero current and has zero voltage with respect to the ground. When only one pole conductor is involved in a fault, a single pole-to-ground fault, a half of the rated power can be transferred with the help of the healthy pole conductor and the DMR [39]. However, in order to exploit the above advantage, only the pole involved in the fault should be isolated during a single-pole fault and ensure that the metallic return wire is not involved the fault. Therefore, fault clearing requires identification of the faulty pole conductor(s) and determination whether the metallic

return wire is also involved in the fault, in order to decide the post fault configuration [40]. The above function is called fault type identification, fault type classification, or fault type discrimination. A number of techniques have been recently proposed to detect DC faults and identify the faulted section in MT-HVDC grids within a sub-millisecond time frame [41-42]. These techniques, however, do not explicitly address the issue of fault type identification.

Fault type identification is difficult due to electromagnetic coupling between the conductors of a bipolar HVDC transmission system; a close-up pole-to-ground short circuit can cause a strong induced transient on the conductor of the healthy pole [43]. Since the coupling is more prevalent at higher frequencies, the independent pole wise fault detection schemes based on high-frequency current components or derivatives of voltages [43-44] are prone to false operation during the faults on the other pole. Therefore, in order to improve the security, protection sensitivity is decreased. However, if the direction and the type of a fault can be identified, the sensitivity can be increased without degrading the security. Any practical solution for fault type identification suitable for a MT-HVDC grid should be both reliable and fast.

In most of the proposed DC fault discrimination schemes, the chances of mal-operation has been avoided by decreasing the sensitivity, that is by compromising the sensitivity to achieve security, often with the help of conservatively selected threshold settings. There is a potential to improve the effectiveness of DC fault discrimination schemes by minimizing such compromises. For example, in AC line distance protection schemes, various strategies such as directional supervision and faulted phase identification, have been successfully used to improve the security and sensitivity. Application of similar means can be explored for the case of DC fault protection in MT-HVDC grids. However, determining directionality or identifying the faulted conductors within the extremely short response time required for DC fault protection has not been successfully

achieved. The first half of the thesis aims to address this gap in state-of-the-art and explores the development of fast local measurement-based algorithms to identify the direction of a fault with respect to a protection relay and determining the conductors involved in a fault.

1.1.3 Converter Behavior during a DC Fault and Fault Clearing

Once a DC fault is detected, and the faulty section and the conductors involved in the fault are identified, the following means are available to deal with the converter safety and clearing of the DC fault. Since IGBTs in an MMC-VSC station are very susceptible to over-currents, they are immediately blocked when an over-current is detected [35]. After blocking the IGBT's, a sub-module and a VSC station can be represented as in **Fig. 1.3(a)** and **Fig 1.3(b)** respectively [42].

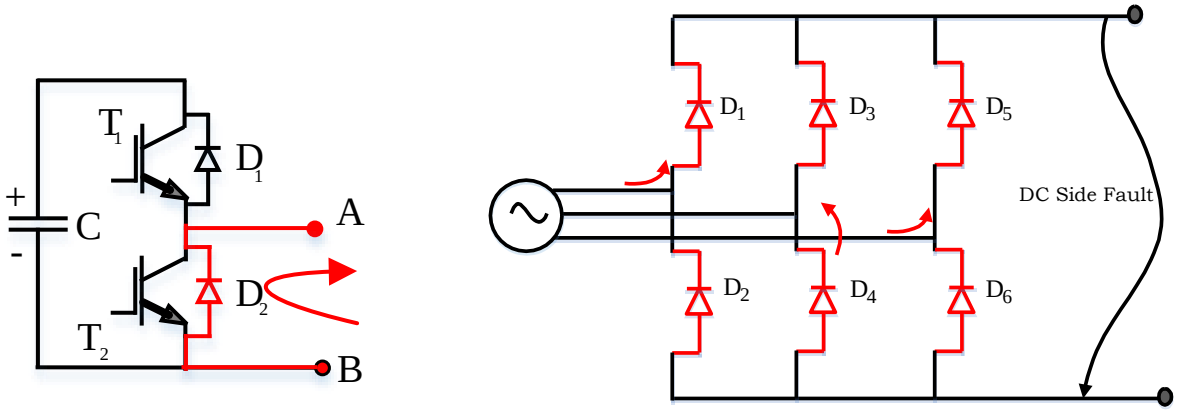


Fig. 1-3. Equivalent of VSC after blocking IGBT's (a) Equivalent of a sub-module, (b) Equivalent of VSC

During the interval between the fault and the IGBT blocking, sub-module capacitors are discharging to the fault. Therefore, as depicted in **Fig. 1.4(b),** the fault current rises to a very high level at a very rapid rate [45]. Where V_{DCP} and V_{DCN} are respectively P-pole and N-pole voltages. I_{DCVRP} and I_{DCVRN} are respectively P-pole and N-pole converter currents. As depicted in **Fig. 1.3(b)**, even after the sub-module capacitors are taken away from the fault circuit by blocking IGBTs, the fault is continued to be fed from the AC side through the free-wheeling diodes in half-bridge sub modules [33, 46].

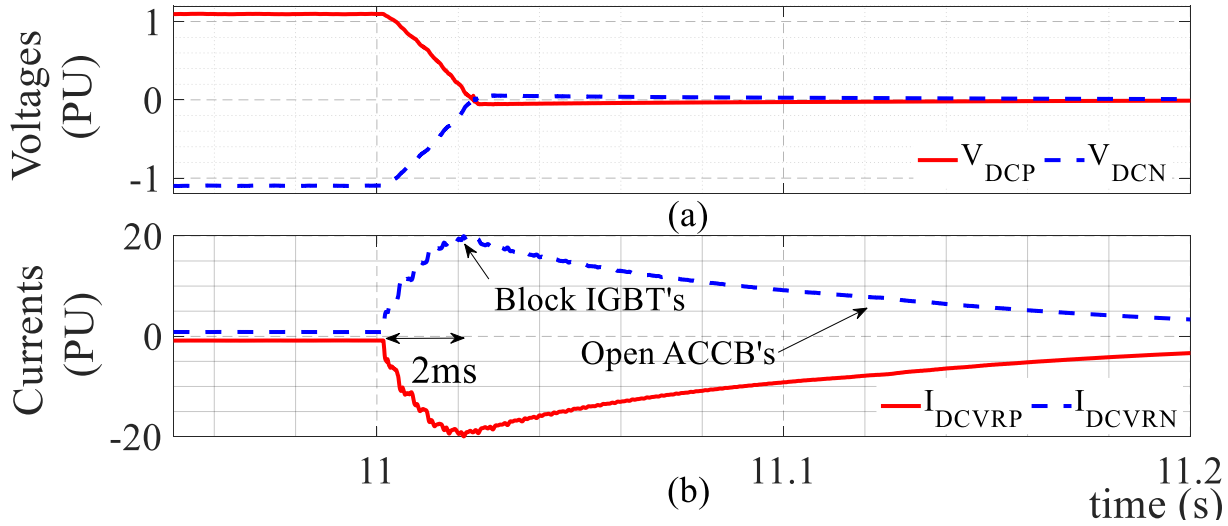


Fig. 1-4. DC side measurement of bipole VSC station for a DC side fault (a) Voltages, (b) Current

Therefore, as depicted in **Fig. 1.4(b),** the fault current will not drop to zero after blocking the IGBT's, but settle into a steady-state value. During this period, freewheeling diodes may subject to very high stress [47]. Therefore, to avoid potential damages to the freewheeling diodes, protective thyristors are used in parallel to the freewheeling diodes of practical converters; these thyristors are fired once a fault is detected [47-49]. **Fig. 1.5** shows the half-bridge sub-module together with its protective thyristor [47].

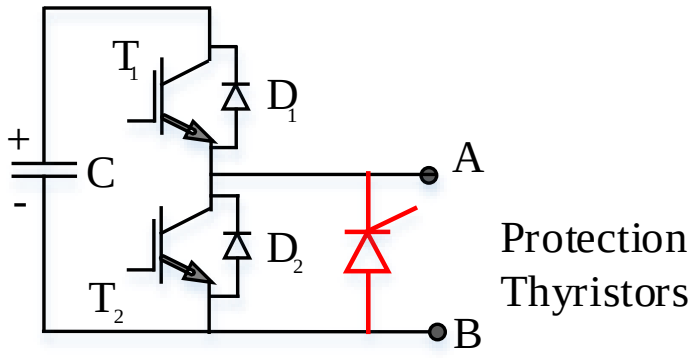


Fig. 1-5. Single thyristor switch

DC side faults could be temporary faults or permanent faults. Temporary faults are self-cleared when the current through the arc is reduced. Fault current limiters such as those presented in [50-53], and fault-tolerant converters such as those presented in [54-59], are proposed to

extinguish temporary fault arcs rapidly and help to clear temporary faults. In contrast, DCCB are used for rapid interruption of fault currents resulting from both temporary and permanent faults. Design, fabrication, and application of high voltage DCCBs is an extensively investigated research topic [60-64]. A prototype of a DCCB capable of interrupting 8 kA in 2 ms delay has been tested in the year 2012 [64]. Another DCCB design capable of interrupting 15 kA in 3 ms has been field-tested in the five-terminal Zhoushan HVDC grid in the year 2016 [65]. However, a practical DCCB design having the capability of interrupting the expected level of fault current within the allowed time frame is still not commercially available from any of the leading manufactures. In the absence of a means to interrupt fault currents, the only means to clear a fault in half-bridge MMC-VSC station is to open the ACCB at the converter transformers and de-energized the affected converter pole(s). This requires the whole MT-HVDC grid to be de-energized when there is no DC side fault current interruption devices [66-67]. The absence of a dependable protection system for DC side faults coupled with the absence of DCCBs having adequate performance is a major obstacle to the practical implementation of MMC-VSC based MT-HVDC grids. Due to huge investment in building a number of MMC-VSC based converter stations together with transmission system and the aforementioned protection challenges has led to focus on alternative MT-HVDC transmission system configurations. A multi-terminal HVDC system containing more than two converter stations with at least one loop in the DC transmission network is referred to as a MT-HVDC grid in this thesis. A multi-terminal HVDC system with more than two converter stations but with no loops in the DC transmission network is referred to as a MT-HVDC transmission system.

1.1.4 LCC-VSC Hybrid MT-HVDC Systems

A hybrid LCC-VSC MT-HVDC transmission system is a multi-terminal HVDC transmission system comprising of both LCC stations and VSC stations. This hybrid configuration exploits the advantages of both converter technologies. Particularly, the abilty of LLC rectifiers to control the DC fault currents through force retardation process can provide both technical and economic benefits in designing DC fault protection. A number of different hybrid LCC-VSC MT-HVDC systems are proposed in [68-79]. Two main classes of hybrid multi-terminal HVDC systems are

1. A number of VSC rectifier stations, typically connected to offshore wind farms, linked to a one large onshore LCC inverter station, connected to the load center,
2. One large LCC rectifier, typically connected to a large hydro power station, linked to a number of small VSC inverters, typically connected to urban load stations.

In the first configuration, the advantages of VSC stations such as small footprint, ability to connect to a weak AC system are exploited in the offshore rectifiers, and the economy of LCC station in building large converter station is exploited in the onshore inverter [80-82]. In the second configuration, the economy of LCC station is exploited in building a large rectifier station connected to a strong system and the advantage of small footprint of VSC stations is exploited in building converters supplying urban load centers [83-84]. A real-world example for the second type is Woudong hybrid three-terminal transmission system which comprises an 8 GW LCC rectifier, and two VSC inverters rated 5 GW and 3 GW. This scheme is under construction and will be commissioned in the year 2022 [14].

All over the world, there are many long, high capacity, point-to-point LCC-HVDC links connecting large generating stations and load centers. Often, these transmission lines are built with

some spare capacity for future expansion or to meet other design requirements. The spare capacity of these transmission lines can be utilized to collect renewable energy generation from wind or solar farm sites located close to these HVDC lines in an economical manner. This requires feeding into the LCC HVDC line using a rectifier [85]. Furthermore, it is possible to supply energy for small cities or load centers located near the path of the HVDC line, if it is possible to tap into an LCC HVDC line using an inverter. Three possibilities exist:

1. Tapping into an LCC-HVDC link using VSC inverters
2. Feeding into an LCC-HVDC link using VSC rectifiers, and
3. Tapping into an LCC HVDC line using both VSC rectifiers and VSC inverters

Such hybrid MT-HVDC transmission systems are attractive due to the lower initial investment requirement. Some example studies are reported in [69, 85-87]. The more general structure comprises of a number of tapping stations capable of operating either as rectifier or inverter.

1.1.5 Protection and Control of Hybrid MT-HVDC Systems

In such hybrid LCC-VSC multi-terminal HVDC transmission systems, the control of converter stations needs to be properly coordinated for stable and smooth normal operation and to enable fast recovery during faults. Therefore, a centralized control strategy is required to coordinate the converter stations. When retrofitting an existing point-to-point LCC HVDC system to form a hybrid MT-HVDC system, modifications to existing LCC converter control need to be minimized. The fault ride-through capability of the newly formed hybrid LCC-VSC HVDC multi-terminal transmission system needs to be thoroughly examined.

Hybrid LCC-VSC MT transmission systems are an emerging area of MT-HVDC transmission systems due to the advantages discussed earlier. Some utilities are keenly interested

in converting existing point-to-point LCC HVDC links to multi-terminal systems. However, the literature on DC side fault behavior and fault clearing in a hybrid LCC-VSC MT-HVDC transmission systems is not common and is an area that requires further investigations. Converter station internal protection may activate during a DC side fault and the fault clearing may involve converter re-energization. A proper understanding of both LCC and VSC converter station protection and control is required to develop a practical DC side fault protection strategy to recover the system through a coordinated sequence of actions involving all converter stations. Since the converter station designs of both LCC only and VSC only schemes are well established, it is best to implement the coordinated controls using the existing control interfaces provided by each type of converter.

1.2. Problem Definition

The discussion presented in Section 1.1 highlighted that the DC side fault protection in MT-HVDC grids is recognized as a main barrier to build large-scale MT-HVDC grids. In order to achieve the expected reliability of future MT-HVDC grids, the section of the transmission line involved in a fault and the faulted conductors should be identified and selectively isolated. However, fault discrimination to achieve the above requirement is challenging under many situations as discussed in Section 1.1. Most of the DC fault protection algorithms proposed in the literature discriminate the faulty line by the strength of the fault induced transient, observed through the measured currents or voltages at the individual pole terminals, and typically by comparing against predetermined thresholds. The sensitivity and reliability of such schemes can be improved by 1) identifying the direction of the fault with respect to the relay (directional discrimination), and 2) identifying the fault type explicitly (identifying the conductors involved in

the fault. In order to satisfy the speed requirements, directional discrimination and faulted conductor identification need to be achieved using the local current/voltage measurements.

The second problem addressed is the DC fault clearing in hybrid LCC-VSC MT transmission systems. DC fault clearing in LCC HVDC schemes is achieved by actively reducing the DC fault currents through force retardation procedure. More common temporary faults are readily cleared through this process and a system can return to normal operation within hundreds of milliseconds. This situation changes when a VSC, typically a half-bridge submodule based MMC which allows continuous DC fault current contribution, is interconnected to an LCC HVDC system. Therefore, the possible ways of clearing DC faults in hybrid LCC-VSC HVDC systems and the fault discriminating requirements to implement the potential fault clearing procedures need to be investigated. Furthermore, understanding how converter stations should be coordinated during the DC faults is also important.

1.3. The Objective of the Research

The main aim of this research is to investigate the methods for handling DC faults in MT-HVDC grids and MT-HVDC transmission systems. In order to achieve the goals of this research, the following major sub-objectives are proposed.

a) To develop suitable simulation models of multi-terminal HVDC transmission systems and study the behavior of MT-HVDC transmission systems for different types of DC side faults.

b) To investigate the possibility of improving the sensitivity of DC side fault discrimination in MT-HVDC system through introducing directional properties, and develop fast, local measurements based methods to determine the directionality of DC fault currents.

c) To investigate the potential for improving the DC fault protection sensitivity while minimizing the inadvertent disconnection of the healthy pole during faults involving only a single pole, and develop a fast local measurement-based method for DC fault type discrimination in an MT-HVDC grid.

d) To develop a strategy for DC fault clearing in a hybrid LCC-VSC MT-HVDC transmission system relying upon the force retardation capability of LCCs and without using DC circuit breakers, evaluate the fault clearing performance and identify potential issues.

e) To investigate the potential for improving fault clearing performance in a hybrid LCC-VSC MT-HVDC transmission system by using DC circuit breakers operated with the protection techniques developed under previous objectives.

1.4. Thesis Overview

The first chapter provides the background, motivation, and objectives of the thesis along with the details of the thesis organization. The next four chapters present the main contributions of the thesis with each chapter addressing one or more major objectives: Objectives a) and b) are addressed in Chapter 2; Objective c) is addressed in Chapter 3; Objectives a) and d) are addressed in Chapter 4; and Objective e) is addressed in Chapter 5. Each of these chapters is based on one or more publications and presented with a background and brief literature review related to the aspects focused in the chapter.

A fault direction identification algorithm for VSC-MMC MT-HVDC grid is proposed in Chapter 2. The method compares the rate of change of voltage (ROCOV) values at either side of di/dt limiting inductor at the terminals. This directional information is utilized to develop a more

secure ROCOV based transmission line and bus protection scheme for MMC-VSC based MT-HVDC grids. The results of simulation-based analysis that conducted with the help of a detailed electro-magnetic type program (EMTP) model of a three-terminal MMC-VSC HVDC grid is presented in the chapter.

A fault type discrimination scheme for HVDC transmission systems is proposed in Chapter 3. The proposed fault type discrimination scheme is capable of identifying conductors involved in the DC side fault using a 1 ms window of the locally measured currents through the transmission conductors. Expected performance of the proposed fault type discrimination scheme is evaluated in various transmission line configurations and converter technologies with the help of simulation-based analysis. The results are also presented in Chapter 3.

A study on clearing temporary faults in a hybrid LCC-VSC MT-HVDC transmission system is presented in Chapter 4. An EMT type simulation model of a hybrid LCC-VSC MT-HVDC transmission system is developed. A master power controller (MPC) is designed to maintain the energy balance in the considered grid and the EMT model is added to the MT-HVDC model. The presently utilized means of handling temporary faults in LCC stations and VSC stations are modeled and added to the grid model. A coordinated temporary fault clearing strategy is developed for hybrid MT-HVDC transmission system in order to obtained smooth fault recovery after a temporary fault. Chapter 4 summarize the above steps and the simulation-based verification results of the study.

A selective fault clearing strategy is developed for an LCC-VSC hybrid MT-HVDC transmission system configuration. It is proposed to place a DCCB along each tapping line at the tapping point to avoid the impact of taping on the original LCC-HVDC link. A fault discrimination strategy based on objectives 1.3.2 and 1.3.3 is developed to discriminate the faults on the main

transmission line from the faults on the tapping lines. The possible improvements are accessed with the help of EMTP simulations performed in PSCAD. The expected recovery waveforms and recovery delays are assessed for faults between poles and for pole-to-ground faults. A summary of selective fault isolation scheme and recovery waveforms, recovery delays together with required performances of DCCB, etc. are presented in Chapter 5.

Conclusions and future directions of the research are presented in Chapter 6.

Chapter 2

ROCOV Based Directional Algorithm for Protection of MT-HVDC Grids

2.1. Introduction

In order to facilitate uninterrupted delivery of power through the healthy part of an MT-HVDC grid during a DC side fault, it is essential to selectively isolate the faulty line or the busbar by interrupting DC fault currents. The inability of MMC-HVDC systems based on half-bridge submodules to block the fault currents and the limitations the DC circuit breakers make it required to complete the fault detection and discrimination within a few milliseconds. This chapter proposes a method to augment the rate of change of voltage (ROCOV) based protection with directional properties. The performance of the proposed new fault detection and discrimination schemes is verified by applying to a simulated MT-HVDC grid and it is shown that the proposed directional ROCOV protection enables more secure and sensitive transmission line and bus protection using only local measurements. The work presented in this chapter is based on the following publication.

[A] M. H. Naushath, A. D. Rajapakse, "Local measurement based ultra-fast directional ROCOV scheme for protecting Bi-pole HVDC grids with a metallic return conductor", Int. J. Elec. Power, vol. *98*, pp. 323–330, June 2018.

2.2. Background and Literature Review

In order to facilitate the uninterrupted power delivery through the healthy part of a multi-terminal HVDC grid during a fault, it is essential to selectively isolate the faulty cable, overhead line or the busbar in a rapid manner by breaking the DC fault currents [4, 88]. Interruption of the DC fault currents is challenging due to the absence of zero crossings in the fault current and its rapid rate of rising resulting due to the discharge of converter, filter and cable capacitances [4, 89]. Therefore, the capability of discriminating faults in different line segments or the selectivity, and the speed are vital for HVDC grid protection [89]. Protection schemes specifically designed for line commutated converters (LCCs) [90] cannot be applied to VSC based MT-HVDC grids. Current differential protection and similar schemes are too slow to protect against the short-circuit faults on typically long HVDC cables and overhead lines due to communication delays [91]. The gradient of the voltage disturbance caused by the fault along with some other measures have been utilized to detect and discriminate the faults in the HVDC transmission systems [43, 91-92]. A protection scheme with a directional unit and a boundary unit has been developed in [43] for a point to point HVDC scheme, but its ability to discriminate faults in an MT-HVDC grid has not being evaluated. Most MT-HVDC grids are expected to contain only the buses that are directly connected to a converter, and therefore, most published studies are confined to test networks with only converter connected busses.

However, in certain situations, a network structure with floating busses, which are solely used to share energy between lines connected to the bus, could be advantages. On the other hand, a converter connected bus can become a floating bus during the converter outages, forced or scheduled. It is more challenging for the relays located at a floating bus to discriminate faults [93].

In this chapter, a method developed to identify the direction of fault currents at a given relay location using the local voltage measurements. The directional information derived from the method is used to improve the sensitivity, speed, and the reliability of the ROCOV based HVDC grid protection. Where the term reliability refers to two performance aspects, the dependability and the security, of a relay. The dependability is the certainty of the relay to operate during a fault in the protected zone of the relay. The security of a relay is the certainty that the relay will not operate incorrectly for faults beyond the protected zone. This directional protection scheme can detect and discriminate faults well before the fault currents reach the maximum breakable current. For example, it is much faster than the method proposed in [94]. The proposed scheme is applicable as the primary protection scheme.

2.3. Detection and Discrimination of Faults in HVDC Transmission Lines Terminated with Inductors

In order to reap full reliability benefits, a DC grid need to be provided with DCCBs to isolate each line/cable segment and busbar, as shown in **Fig. 2.1**.

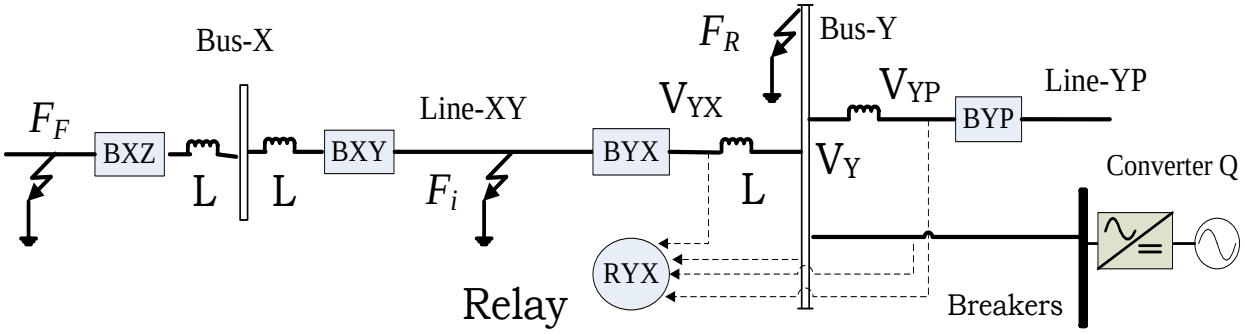


Fig. 2-1. A section of an HVDC grid (© Elsevier)

An inductor is usually placed between an HVDC transmission line and a DCCB to control the rate of rising of fault currents [42]. The terminal inductors, which are designed to allow

sufficient time for DCCBs to operate before the fault currents exceed their ratings, play an important additional role in fault discrimination [42]. To analyze the behavior of DC line terminal voltage during a fault, assume that the internal fault F_i on Line-XY creates a step change of -ΔV_F in the voltage at the location of the fault [95]. The resulting voltage waves travel towards the line terminals. The very first incident wave arriving at the terminal inductor associated with the DCCB named BYX is described in Laplace domain by:

$$\Delta V_{YX}^{+}(l,s) = \frac{-\Delta V_F}{s} e^{-\gamma(s)l} \tag{2.1}$$

The magnitude of the incident wave depends on the propagation function γ and the distance from the fault to the line terminal, l. At the terminal inductor, the voltage wave is reflected back, and the frequency-dependent reflection coefficient Γ is given by [95]:

$$\Gamma(s) = (sL - Z_c)/(sL + Z_c) \tag{2.2}$$

where, L is the terminal inductance and Z_c is the characteristic impedance of the line, which is real and approximately constant at high frequencies. The change in line terminal voltage ΔV_{YX} is the sum of incident and reflected waves [91][95] , and given by:

$$\Delta V_{YX}(l,s) = \frac{-\Delta V_F}{s}\left[\frac{2s}{s+\frac{Z_c}{L}}\right] e^{-\gamma(s)l} \tag{2.3}$$

When the voltage wave hits the terminal inductor, voltage V_{YX} drops rapidly: thus the rate of change voltage (ROCOV) at the line side of the inductor is a very good indicator of transmission line faults. On the other hand, the transmitted component measured at Busbar-Y due to the fault F_i is given by (2.4) .

$$\Delta V_{Y}(l,s) = \frac{-\Delta V_F}{s}\left[\frac{2\cdot\frac{Z_c}{L}}{s+\frac{Z_c}{L}}\right] e^{-\gamma(s)l} \tag{2.4}$$

The inductor acts as a low pass filter. Therefore, high-frequency components of the transmitted wave are attenuated when passing through the inductor.

2.3.1. Peak ROCOV Based Line Protection

In the simple ROCOV based DC line protection scheme proposed in [42], an internal fault in the protected zone is discriminated from the faults in the adjacent zones by the observed peak |dv/dt| values. The voltages waves due to faults in the other line or busbar zones are transmitted through at least one series inductor. As a result, the peak |dv/dt| values observed for external faults are considerably smaller compared to the internal faults, allowing fault discrimination. For example, peak $|dV_{YX}/dt|$ in **Fig. 2.1** is considerably smaller for external faults such as F_F or F_R, compared to the internal fault F_i. A simple threshold, which is determined from a systematic fault study, is used for discrimination.

Any internal fault which causes a steady-state fault current higher than the maximum breaking current of DCCB must be quickly cleared. However, the simple peak |dv/dt| based fault discrimination is valid only up to certain fault resistance. The fault generated voltage wave attenuates as it travels along the line as per (2.1), and the faults at the far-end of a transmission line produce lower peak |dv/dt| values. When the fault resistance is high, the faults at the far end of the protected line become difficult to be discriminated from the low resistance reverse faults on the busbar or lines behind the relay point. A larger inductor is required to enhance the fault discrimination when a simple peak |dv/dt| scheme is used. However, a larger terminal inductor deteriorates the performances of DC voltage controller and might cause instability [96]. Furthermore, high peak |dv/dt| produced during the opening of breakers of adjacent lines prevents

setting the thresholds sensitively [97]. Therefore, a fault detection scheme based on local measurements, having higher sensitivity and security is desired.

2.3.2. ROCOV Based Directional Protection

Consider an internal fault (such as F_i) in the forward direction with respect to DCCB BYX in **Fig. 2.1**. The typical behavior of the fault current is such that it goes through a rapidly increasing phase before reaching a maximum and then settles down to its steady-state value, as illustrated in **Fig. 2.2**. The rate of change of current through the terminal inductor (on the positive pole) into the line is given by:

$$sI(s) = \frac{1}{L}[V_Y(l,s) - V_{YX}(l,s)] \tag{2.5}$$

An initial high positive rate of change of current through the inductor indicates a forward fault, and according to (2.5), it is possible only when the voltage V_{YX} is smaller than V_Y.

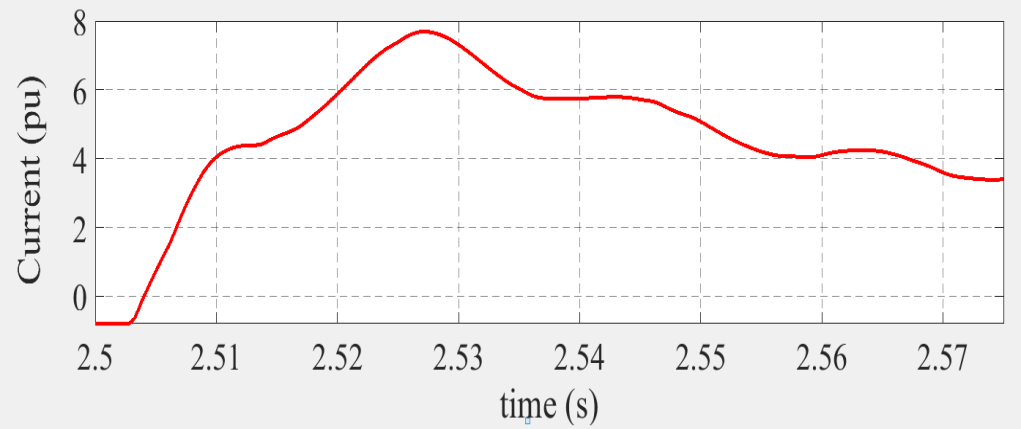


Fig. 2-2. Converter currents during a DC side fault

This property can be easily used to assert the direction of fault current: at steady state, $V_Y = V_{YX}$; during a forward fault, $V_Y > V_{YX}$; and during a reverse fault, $V_Y < V_{YX}$. However, if this logic is applied it is necessary to ensure that the measurements are taken during the initial rise of the current. The observations show that the peak |dv/dt| values occur during this initial period and the

measurements taken at the peak |dv/dt| point can be used to determine the fault direction. Alternatively, it is also possible to determine the fault current directions from the peak |dv/dt| values observed at either side of the terminal inductor. During the forward faults, a much larger peak |dv/dt| is observed in V_{YX} compared to the peak |dv/dt| observed in V_Y. The opposite happens during the reverse faults. Since the peak |dv/dt| values are used in the main protection function, it is advantageous to use the same quantity to find the direction of the fault current. Thus the condition for a forward fault can be expressed as:

$$\left|\frac{dV_{YX}}{dt}\right|_{peak} \Big/ \left|\frac{dV_Y}{dt}\right|_{peak} > 1 \tag{2.6}$$

In practice, the ratio of peak |dv/dt| values can be compared against a threshold higher than 1 to improve the security. Since the absolute values of dv/dt are considered, a common logic can be applied to both positive and negative poles.

If the fault direction can be determined, the peak |dv/dt| threshold can be set sensitively and the operation of the DCCB can be blocked for the reverse faults. The transient voltage ratio V_{YX}/V_Y can also indicate forward faults, and therefore, can be used for fault discrimination as proposed in [94]. However, much faster fault discrimination can be achieved by using $\left|\frac{dV_{YX}}{dt}\right| \Big/ \left|\frac{dV_Y}{dt}\right|$, because the ROCOV values change almost instantly when a traveling wave reaches the terminal, whereas it takes a comparatively longer time to see a change in voltage.

The peak |dv/dt| threshold and the directional logic (as applicable to line XY at Bus-Y) can be combined using the relay characteristics shown in **Fig. 2.3(a)**. In the relay, the peak |dv/dt| at the line side of the terminal inductor is used as the operating quantity while the peak |dv/dt| at the bus is used as a restraining quantity. The threshold "$ROCOV_L$" can be set lower than a non-directional ROCOV relay [42]. The lower limit of the "$ROCOV_L$" is dictated by the peak |dv/dt| created at the relay point during a short circuit fault on the remote bus in the forward direction.

For example, "$ROCOV_L$" of relay RYX should be higher than the peak |dv/dt| recorded for a short circuit fault on Bus-X. To enhance security, the proposed ROCOV based directional scheme can be supervised by an under-voltage element as in [91].

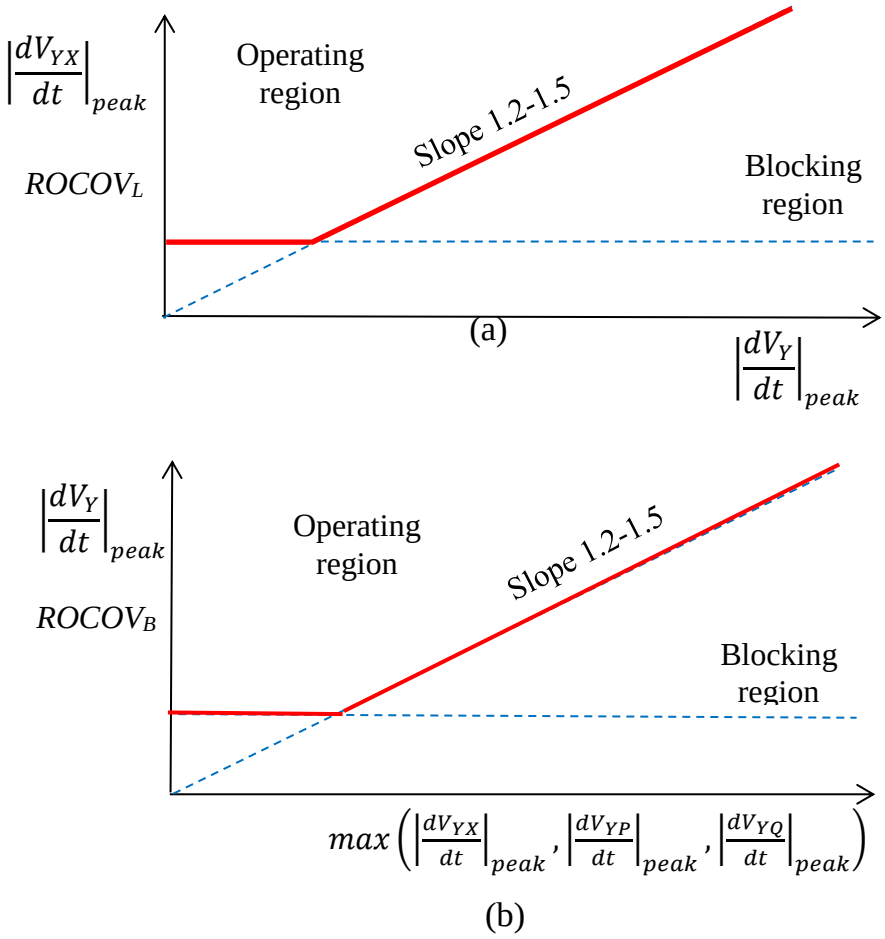


Fig. 2-3. Local voltage measurement based directional ROCOV relay characteristics, (a) Line protection scheme, (b) Bus protection scheme (© Elsevier)

Furthermore, it can be integrated with a lightning detector proposed in [43]. Essentially the same concept can be applied for bus fault detection. The voltage wave created by a bus fault is highly attenuated when it is passing through the terminal inductors on the lines connected to the faulted bus. Thus, if the peak |dv/dt| values at the line side of all terminal inductors are smaller than the peak |dv/dt| on the bus, a bus fault can be declared. Thus the bus fault detection relay

characteristics, as applicable to Bus-Y, can be developed as shown in **Fig. 2.3(b)**. In this scheme, the operating quantity is the peak |dv/dt| value at the bus and the restraining quantity is the maximum of the peak |dv/dt| measured at line side of the terminal inductors connected to the bus.

2.3.3. Security of Bus Protection in Bi-pole Transmission Systems with a Return Conductor

Bi-pole HVDC transmission with a dedicated metallic return conductor (DMR) is considered as one of the most likely practical configurations for MT-HVDC grids [42, 92]. The DMR conductor in a bi-pole HVDC grid is usually earthed only at a single point to eliminate the stray ground currents and the flow of geomagnetically induced currents. Unlike in the radial symmetrical monopole test system used in [94], the DMR wire provides a very convenient path for induced traveling waves. These induced waves can interfere with the bus side measurements if di/dt limiting inductors are not present on the return conductor, as limiting of the rate of rising of current in the return conductor is not essential for the current interruption purposes. This can reduce the security of the proposed peak |dv/dt| based busbar protection and make the faults discrimination more challenging.

During a pole-to-ground fault on a bus connected to a converter located far from the earthing point, the fault creates a step voltage of magnitude equals to nominal pole voltage on the DMR conductor (at the faulty bus) as the DC voltage of the converter will not change instantaneously. The resulting voltage wave travels along the DMR conductor towards other converter buses. A sudden change occurs in the pole voltages when this wave reaches another converter bus located away from the earthing point (again due to the fixed converter DC voltage at the wave incident bus). As a result, a considerable peak |dv/dt| values are generated. Thus a condition very similar to

a bus fault is created because the line side voltages are not much affected by the waves in the DMR conductor due to the terminal inductors. False operation of busbar protection due to the impact of waves traveling along the DMR conductor can be eliminated simply by inserting an inductance on the return wire at each terminal. This inductance is not necessary to be as large as the terminal inductances on the pole conductors, as they have no di/dt limiting function. It will be shown in **Section 2.4.2** that an inductance of a few milli-Henrys is sufficient to block the traveling waves.

2.4. Simulation Studies

The dependability and the security of protection algorithms need to be evaluated rigorously under the actual environment which they are operated. However, it is impossible to test protection relays deployed in actual HV power systems since access to such systems is often restricted for security and safety reasons. Faults are very rare events and purposely staging faults in actuial power systems is not justifiable except for very specific situations. Development of scaled porotypes is not very common due to cost. Possible damages to expensive equipments and the challenges of creating required scenarios forces evaluation of protection algorithms to be done through simulations. Detailed EMT type computer models evolved over the time can produce voltage and current waveforms which are very similar to those observed in actual power systems. Hence, EMT type simulation is the common industry practice used for evaluating the performance protection algorithms. When the hardware prototypes are built, real time simulators, which are also based on EMT models, can be used to further evaluate the practical aspects of algorithm implimentations. Injecting simulated or synthesized waveforms using test sets is another approach for testing prototypes. However, this thesis mainly focuses on the algorithm development and

therefore off-line EMT simulations are used test the proposed algorithms throughout the thesis. This is also the currently established practice in industry.

The bi-pole MT-HVDC grid example shown in **Fig. 2.4** was used for simulation-based verification. The test grid consists of three MMCs connected to Buses-1, 2 and 3. The operating voltage is set to 320 kV by considering famous VSC based Caprivi HVDC link, which is a 950 km long HVDC link operating at 350 kV.

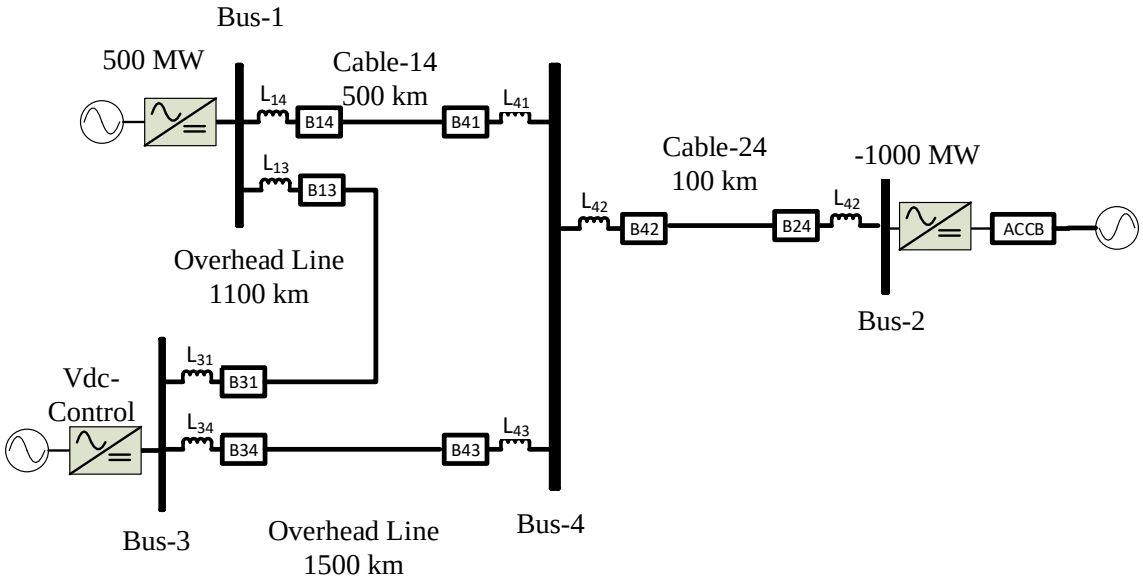


Fig. 2-4. The bipole-HVDC test grid (© Elsevier)

They were modeled with sufficient details and the required basic controls for stable operation [98], with the double closed-loop vector control [99] being the approach used for realizing VSC controls. The diagram of the d-q vector controller is shown in **Fig. A-1** in **Appendix-I**. Under normal situations, the MMC at Bus-3 operates in DC voltage control mode, while the other two operate in the constant power control mode to ensure stable grid operation and power balance. The capacitor voltage balancing algorithm is modelled in the MMC control and the ripple of capacitor voltage is taken into account in designing the control and selecting the capacitor value. The DMR conductor is grounded near the voltage-controlled Bus-3.

Fault direction identification is challenging when alternative paths are available for travelling waves. Therefore, to evaluate the security of the proposed method, a test system having a loop structure is considered. Fault discrimination becomes more difficult when the transmission lines are long. Therefore, a 1500 km long overhead is included to test worse case scenarios. This legth is no unusual for HVDC systems, for example the length of Manitoba Hydro Bipole-III HVDC link is 1400 km. The transmission system parameters are given in **Table A.3**, **Table A.4**, **Fig. A-4**, and **Fig. A-5** of the **Appendix-I**. The frequency-dependent phase domain models available in PSCAD [100] were used to simulate the cables and transmission lines. A 5 μs simulation time step was used to adequately capture the high-frequency behavior during the simulation of faults. The basic data of the grid are given in **Table-2.1**. As it is shown with calculation in **Section-1** of **Appendix-I**, the MMC sub-module capacitor value is selected to achieve Energy/Power ratio to 10 J/kVA and the converter side voltage of the transformer is selected to limit the maximum modulation index to 1.15.

Table 2-1 Test grid details (© Elsevier)

Parameter	Value	Units
Nominal DC Grid Power	1,000	MW
Nominal AC Voltage (V_{LL})	230	kV
Nominal DC Voltage	±320	kV
Equivalent MMC DC Capacitance	100	μF
di/dt limiting reactor on poles	40	mH
Power injected from Converter @ bus-1	250	MW/pole
Power injected from Converter @ bus-2	-500	MW/pole

The di/dt limiting inductors on the cable and overhead line terminals were set to 40 mH so that fault currents do not exceed 16 kA within 2 ms after the fault: this is the assumed capability

of the DCCBs. Although use of wide range of inductor values such as 50 mH [101], 100 mH [42], 150 mH [102] or 200 mH [44] can be found in literature, a 40 mH inductor was used to show that the proposed scheme works with even smaller terminal inductors, which is the worst case for fault discrimination point of view. As it is shown with calculation in **Section-2** of **Appendix-I**, a 40 mH offers a 2 ms delay to the DCCB before it reaches the peak current 16 kA.

2.4.1. Implementation of Peak ROCOV Calculation

The signal processing involved in estimating the peak |dv/dt| of a measured voltage should be represented in the simulations when evaluating a ROCOV based protection scheme. A fault at the far end of a line or cable creates the lowest ROCOV values due to attenuation during traveling. Therefore, the minimum bandwidth requirement of the sensor is determined to avoid further attenuation for far-end faults. Assuming a minimum bandwidth of 10 kHz for practical high voltage sensors, an 8 kHz fourth-order Butterworth low pass filter was employed to alleviate any effects from the variations in the bandwidth of different sensors and high-frequency noise. The bandlimited voltage signal was then sampled at 25 kHz (sampling interval 40 μs > simulation time step 5 μs) with a 12-bit analog-to-digital converter (ADC). For far end faults, this ADC resolution and sampling frequency ensure that the difference between peak |dv/dt| before and after the sampling remains less than 5%. ROCOV values are calculated as:

$$(dv/dt)_{t=t_n} = (v_n - v_{n-1})/\Delta T_s \tag{2.7}$$

where v_n and v_{n-1} are the sampled voltages at the current and previous sampling instants respectively, and ΔT_s is the sampling interval (40 μs). A peak detector was then used to detect the peak |dv/dt| values. In order to speed up fault detection, unlike in [94], a time window was not used. Therefore, a trip signal may be generated whenever $\frac{dV_{YX}}{dt}$ exceeds the threshold and satisfy

the criteria $\left|\frac{dV_{YX}}{dt}\right| / \left|\frac{dV_Y}{dt}\right| \geqslant 1.2$, even before the final peak ROCOV for the given fault occurs, as the output of peak detector keeps on increasing after the fault, until its final peak value is reached. The peak detector was configured to reset 4 ms after detecting a peak above the threshold.

2.4.2. Influence of Inductors on Return Wire

To demonstrate the impact of waves traveling through dedicated the return wire, an N-pole-to-ground fault was applied at Bus-1, and the results are shown in **Fig. 2.5**. A steep voltage rise is observed on the DMR conductor, whereas the voltage rise on the N-pole conductor (line side of the terminal inductor) is very slow. According to **Fig. 2.5(a)** which shows the calculated |dv/dt| values at Bus-1 with the help of simulation, a very high peak |dv/dt| occurs on the DMR conductor voltage. As depicted in **Fig. 2.5(b)** and **Fig. 2.5(c),** the voltage wave on the DMR conductor travels uninhibited through Bus-4 and reaches Bus-2. When the wave hits Bus-2, the voltage at Bus-2 increases rapidly by creating a high peak |dv/dt| as shown in **Fig. 2.5(c)**. This can cause mal-operation of the bus fault detection relay at Bus-2. The effects of the waves travelling through the DMR conductor can be mitigated by inserting a small inductance in series with the return wires, when connecting to a converter neutral point. According to **Fig. 2.5(a),** the observed |dv/dt| value of the return wire voltage at Bus-1 is considerably reduced when 2.5 mH inductors are placed on the return wire. **Fig. 2.5(b)** and **Fig. 2.5(c)** show the estimated |dv/dt| values of the voltages at Bus-4 and Bus-2: observed peak |dv/dt| value at Bus-2 due to the wave reaching through the DMR conductor can be reduced to half by adding a 2.5mH inductor. Although having a DMR conductor inductor at Bus-3 (where the DMR conductor is earthed) is not helping to limit rate of rising fault current, having a DMR inductor enables changing the location of the earthing if required.

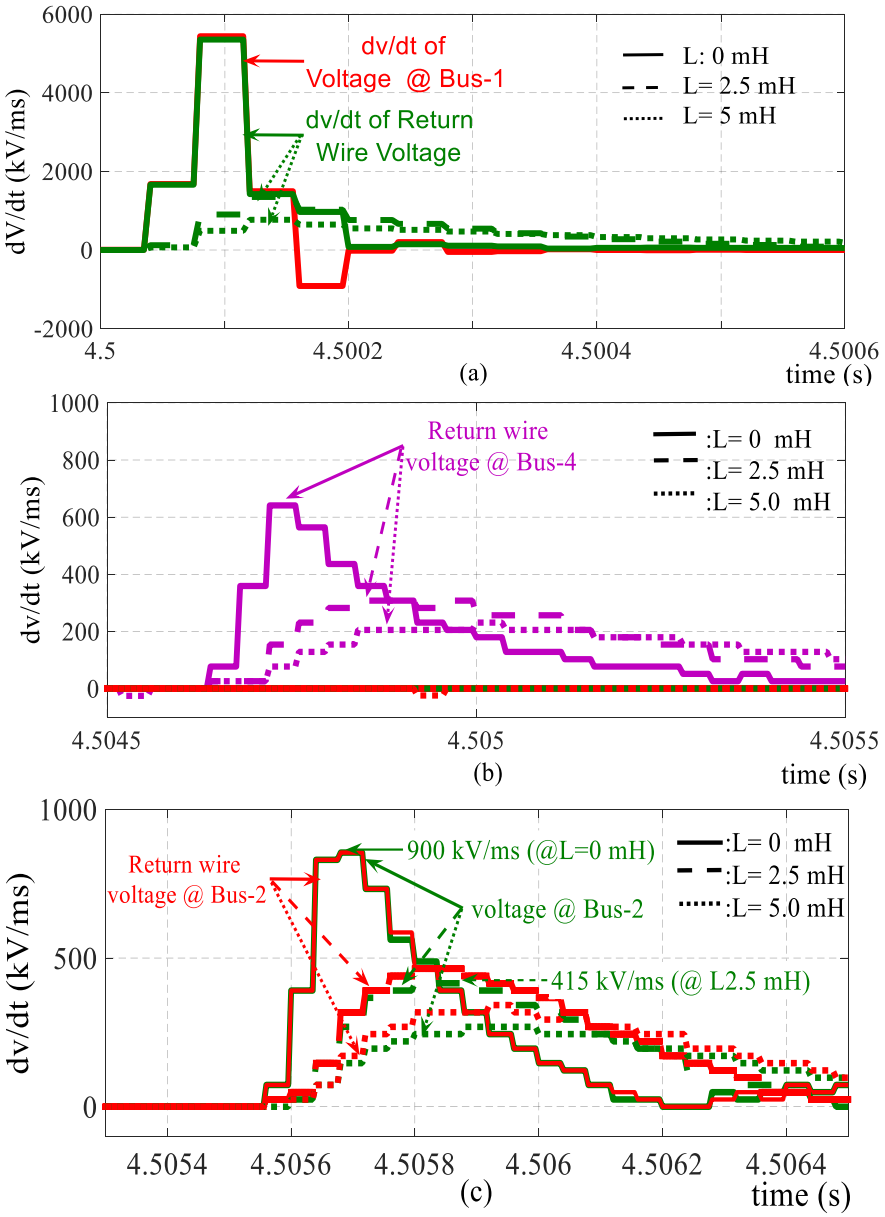


Fig. 2-5. dv/dt values with different return wire inductor values for an N pole-ground fault at Bus-1 (© Elsevier), *(a) Bus-1, (b) Bus-4, (c) Bus-2*

In the simulations presented in **Section 2.5**, a 2.5 mH series inductor was included at the terminals of each return conductor.

2.4.3. Protection Settings

The values of $ROCOV_L$ and $ROCOV_B$ were set after a fault study using the developed simulation model, considering the criteria described in **Section-2.3**. The $ROCOV_L$ threshold was set above the peak |dv/dt| value observed for a short circuit pole-to-pole fault on the remote bus in the forward direction. A 30% margin was considered in this study. For the directional characteristics, a slope of 1.2 was considered for improved security. **Table-2.2** shows the settings of all transmission line and bus protection relays.

Table 2-2 Relay settings (© Elsevier)

Relay	$ROCOV_L$ **(kV/ms)**	**Relay protecting**	$ROCOV_B$ **(kV/ms)**
R14/R41	150	Bus-1	600
R24/R42	600	Bus-2	600
R34	1780	Bus-3	600
R43	1400	Bus-4	3000
R13	1730		
R31	940		

These protection settings are applicable even when the network topology is changed, as it will be demonstrated in **Section-2.5.5**.

2.5. Simulation-Based Verification of the Proposed Directional Peak ROCOV Protection Algorithm

The current and voltage waveforms for a 0.01Ω N-pole-to-ground fault on Cable-14 at about 100 km away from L_{41} are shown in **Fig. 2.6(a)**. The peak |dv/dt| values of the line and bus side voltages at L_{41}, as observed by Relay-R41, are 6568 kV/ms and 2344 kV/ms respectively. Based

on the trajectory of operating point plotted on the R41 relay characteristics shown in **Fig. 2.6(b)**, relay R41 declares a fault in Cable-14.

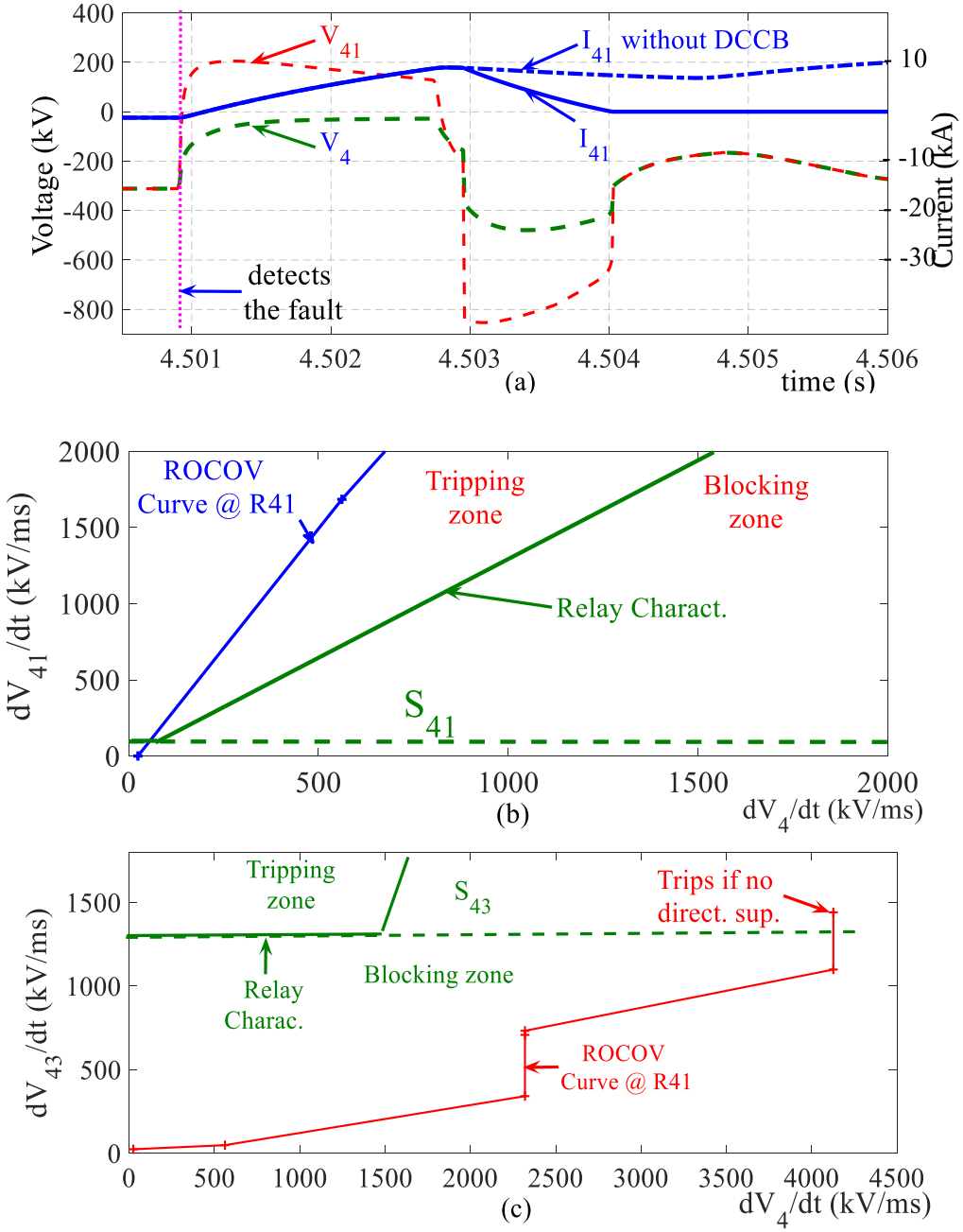


Fig. 2-6. Responses during a 0.01Ω N-pole-to-ground fault on Cable-14 (© Elsevier), (a) Voltages and current seen by R41, (b) Operating characteristics of R41 and responses for the fault, (c) Operating characteristics of R43 and responses for the fault

Similarly, the relay associated with L_{14} declares a fault in the direction of Cable-14 since the peak |dv/dt| values of the line and bus side voltages are 1916 kV/ms and 122 kV/ms respectively.

As the peak |dv/dt| values of the line side voltages are greater than the bus side peak |dv/dt| values at both ends of Cable-14, it can be concluded that the fault is within the Cabale-14. Note that the fault is detected almost instantly ($\approx 100\ \mu s$) after the arrival of the traveling wave at the inductor L_{41}. The current is interrupted by opening B14 and B41 after the 2 ms operational delay assumed in the DCCB model. The peak ROCOV observed at R43 due to the opening of B41 is 1660 kV/ms. This is greater than the ROCOV setting of relay R43. Without the directional supervision, as depicted in **Fig. 2.6(c)**, R43 would have issued an unnecessary trip to B43. The current I_{41} in **Fig 2.6(a)** includes the current through the surge arrester in the hybrid DCCB [88], thus does not become zero immediately after the opening of B41. In the second test, a pole-to-pole fault with a resistance of 200 Ω is applied on the overhead line OHL-34, 800 km away from Bus-4. The current and voltage waveforms observed at the relay associated with B43 (N-pole) are shown in **Fig. 2.7(a)**, and the corresponding variation of the operating point on relay characteristics is shown in **Fig. 2.7(b)**.

The positive pole voltage and the current are not shown as those are nearly the mirror images of the negative pole voltage and the current. To demonstrate the functioning of the bus protection scheme, an N-pole-to-DMR conductor fault of 50 Ω resistance was simulated at Bus-4. The results are shown in **Fig. 2.8(a)** and **Fig. 2.8(b).** The bus side peak |dv/dt| value is higher than the threshold ($ROCOV_B$) and all peak |dv/dt| values measured at the line sides; according to the proposed directional criteria, decision will be made based on the peak |dv/dt| at line side of L43, which is the highest. In order to confirm the proper operation of the protection scheme, a large number of faults were simulated at different locations.

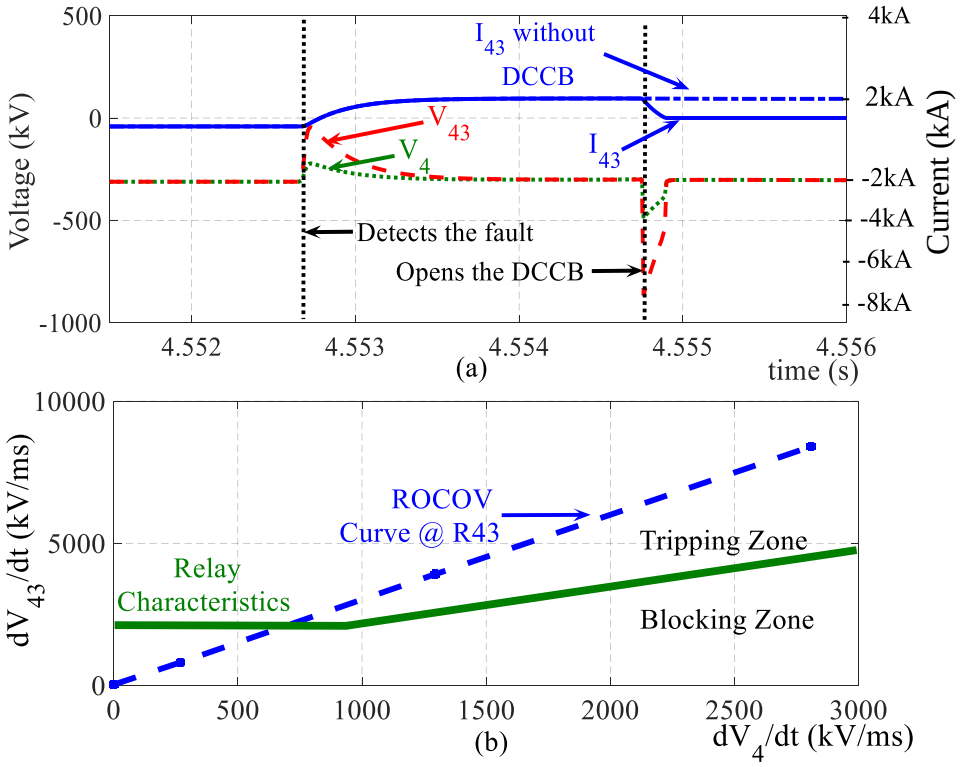


Fig. 2-7. Responses for a 200 Ω pole-to-pole fault on OHL-34 (© Elsevier), (a) Voltages and current seen by R43, (b) Operating characteristics of R43 and responses for the fault

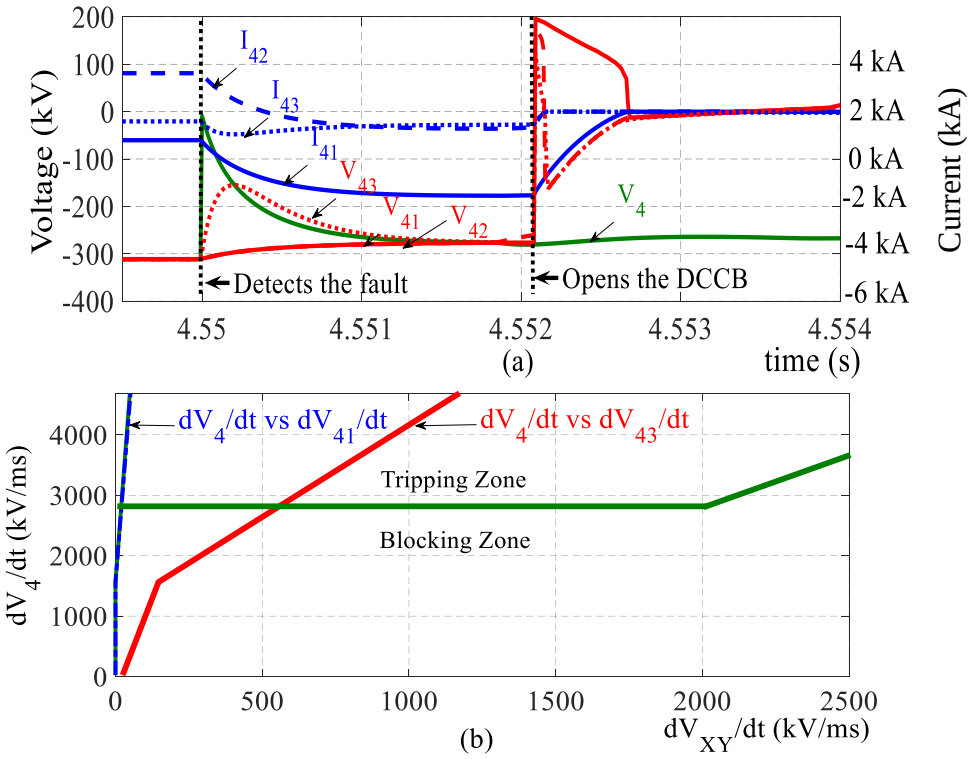


Fig. 2-8. Observations for a 50Ω pole-to-return wire fault a Bus-4 (© Elsevier), (a) Voltages and currents at Bus-4, (b) Corresponding operating characteristics

2.5.1. Responses for Cable Faults

In order to evaluate the dependability and security of the proposed method, responses of all IEDs are recorded after applying variety of fault scenarios. **Table 2.3** summarizes the performance of the line protection scheme for faults on Cable-14 and Cable-24. In the tables, the first column indicates the distance to the fault measured from the relay associated with the voltage shown in the third column and R_F denotes the fault resistance. The columns labeled $\dot{V}_{ij}$ and $\dot{V}_i$ give the estimated peak |dv/dt| values observed at the line side of the terminal inductor L_{ij} and Bus-i, respectively. The first raw corresponding to a fault indicates observed peak ROCOV due to the fault and the second raw indicates the observed peak ROCOV after clearing the fault. The letter T or NT in the last columns indicates whether a trip signal is generated (T) or not (NT) by the corresponding relay. The observed peak |dv/dt| values at two ends of a cable are very close to each other when the fault is in the middle.

Table 2-3 Relay responses for faults on cable C-14

Loc.(km)	**R_F (Ω)**	**Peak |dv/dt| (kV/ms) at**					**Responses**		
C-14		$\dot{V}_{14}$	$\dot{V}_1$	$\dot{V}_{41}$	$\dot{V}_4$	$\dot{V}_{43}$	R_{14}	R_{41}	Other
0	0.01	5432	323	1318	488	317	T	T	NT
		11176	610	10866	3907	1318			NT
100	10	2545	146	757	293	170	T	T	NT
		10944	634	10541	3760	1221			NT
250	50	390	24	390	146	73	T	T	NT
		10620	622	439	146	73			NT
500	50	268	18	1098	24	122	T	T	NT
		10700	628	3052	976	390			NT

Table 2-4 Relay responses for faults on cable C-24

Loc. (km)	R_F (Ω)	Peak |dv/dt| (kV/ms) at					Responses		
C-24		$\dot{V}_{24}$	$\dot{V}_2$	$\dot{V}_{42}$	$\dot{V}_4$	$\dot{V}_{43}$	R_{42}	R_{24}	Other
0	0.01	6568	415	5410	1974	683	T	T	NT
		11404	757	11025	3974	1318			NT
50	0.01	7032	522	7076	2692	1074	T	T	NT
		10866	610	10769	3743	1074			NT
50	10	2759	170	2769	1025	415	T	T	NT
		10866	683	10923	3948	1318			NT
100	0.01	5396	366	6564	2333	879	T	T	NT
		11062	659	11487	4282	1358			NT
100	50	1074	73	1307	487	170	T	T	NT
		9377	58	10717	3871	1294			NT

Also note that high peak |dv/dt| values are observed at the line side of L_{43} connected to the overhead line ($\dot{V}_{43}$). These values occur when B41 opens to clear the faults on Cable-14. According to **Table 2.3** and **Table 2.4**, the relays protecting the cables are capable of detecting all line faults. No false trip signals were generated by any other relay.

2.5.2. Responses for Faults on Overhead Lines

Table 2.5 summarizes the performance of the protection scheme for faults in OHL-34. The observed peak |dv/dt| values for the overhead line shown in **Table 2.5** are much higher than the observed peak |dv/dt| for cables shown in **Table 2.3** and **Table 2.4**. This is due to the lower attenuation constant of an overhead transmission line than the cables.

Table 2-5 Relay responses for faults on OHL-34

Loc. (km)	R_F (Ω)	Peak |dv/dt| (kV/ms)					Responses		
		$\dot{V}_{34}$	$\dot{V}_3$	$\dot{V}_{31}$	$\dot{V}_{43}$	$\dot{V}_4$	R_{34}	R_{43}	Other
0	0.01	5470	317	97	4322	1440	T	T	NT
		11282	586	170	8522	2857			NT
0	100	3809	244	73	3003	1001	T	T	NT
		10134	534	170	5616	1855			NT
300	10	4249	122	48	3540	1196	T	T	NT
		7106	366	97	8424	2808			NT
600	100	2222	73	24	2222	757	T	T	NT
		7960	390	122	7960	2661			NT
1200	0.01	3467	122	48	4737	1611	T	T	NT
		8766	350	122	7594	2564			NT
1500	100	2881	122	48	3858	1318	T	T	NT
		7032	341	97	10134	3394			NT

2.5.3. Responses for Bus Faults

Table 2.6 summarizes the performance of the protection scheme for bus faults. The tests showed that all the bus protection relays operate as intended. The highlighted cells in **Table 2.6** show that when clearing the bus faults, remote relays protecting the overhead lines connected to the faulted bus tend to operate due to the high peak |dv/dt| caused by the breaker opening. This can be avoided by increasing the respective $ROCOV_L$ settings, slightly trading off the sensitivity. On the other hand, although this breaker operation is unnecessary, opening of the breaker does not have any impact on the power flow. Therefore, the $ROCOV_L$ settings were left unchanged.

Table 2-6 Relay responses for bus faults

Loc.	$R_F(\Omega)$	Peak |dv/dt| (kV/ms)					Responses	
		$\dot{V}_1$	$\dot{V}_{13}$	$\dot{V}_{14}$	$\dot{V}_{31}$	$\dot{V}_{41}$	R_{1Y}	Other
Bus-1	0.01	5445	2271	109	634	97	T	NT
		5445	7252	10321	3321	146		R_{31}
Bus-1	50	2564	1050	48	341	24	T	NT
		2564	6836	7544	2197	24		R_{31}
Bus-1	200	670	439	18	146	24	T	NT
		670	7765	5896	3003	24		R_{31}
		$\dot{V}_4$	$\dot{V}_{41}$	$\dot{V}_{42}$	$\dot{V}_{43}$	$\dot{V}_{34}$	R_{4Y}	Other
Bus-4	0.01	5421	97	102	1782	1489	T	NT
		5421	7106	10207	10119	2808		R_{34}
Bus-4	50	4734	97	76	1489	1269	T	NT
		4737	10749	9871	6882	1611		NT
Bus-4	200	3247	48	51	927	781	T	NT
		3247	10329	10589	5592	1343		NT

2.5.4. Fault Detection Time

A bipolar low resistance grounded HVDC scheme requires a faster protection than a high resistance grounded or symmetrical monopole HVDC grids [38]. The time taken by the proposed ROCOV based relays to detect a fault ($T_{Proc.}$) can be estimated by [38]:

$$T_{Proc.} = T_{Detection} - T_{Travel} \tag{2.9}$$

where $T_{Detection}$ is the period between the fault occurrence and the detection, T_{Travel} is the time taken by the fault generated voltage waves to travel from the location of the fault to the terminal. The estimated velocities are 300 km/ms and 110 km/ms respectively for OHL-34 and

Cable-14. **Fig. 2.9** shows the estimated processing delay for different fault locations in Cable-14 and OHL-34. The maximum processing delays are 130 μs and 165 μs for Cable-14 and OHL-34 respectively. Simulation results show that the proposed peak |dv/dt| based directional scheme detects and discriminates faults reliably within a much shorter time compared to the methods that use other indicators such as transient voltages [94] or derivatives of currents [44]. The proposed algorithm detects and discriminates all types of faults in less than 200 μs.

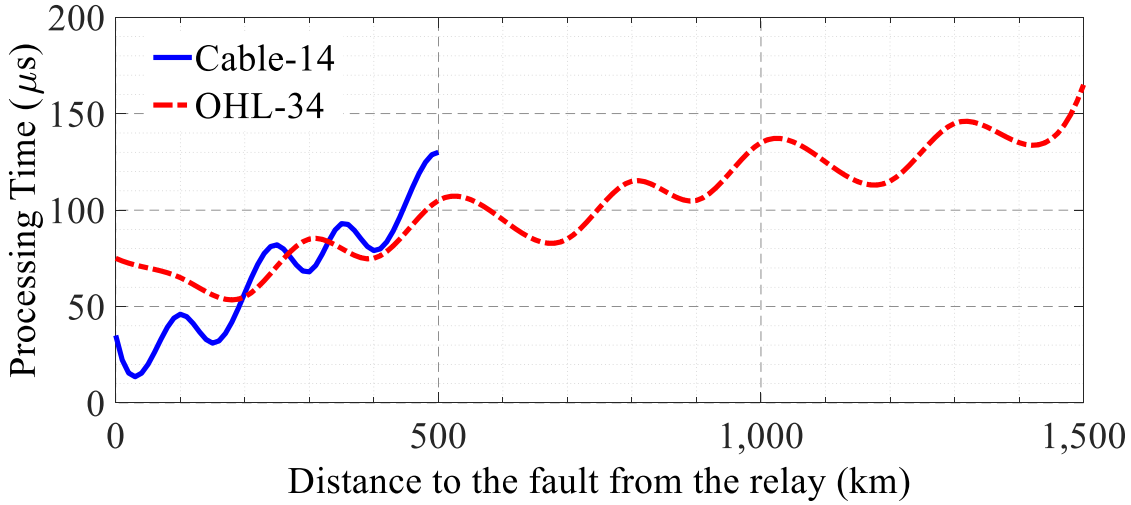


Fig. 2-9. Processing delay for different fault locations (© Elsevier)

In contrast, the algorithm proposed in [101] may take over 1 ms to detect a fault and the method proposed in [94] requires 1.74 ms to detect a fault located at about 100 km away from the relay in a cable.

2.5.5. Performance during an Outage of OHL-31

The capability of maintaining the protection performance despite the changes in network configuration or operating conditions is a vital characteristic of a robust grid protection system. To evaluate the performance of the proposed protection scheme at a network reconfiguration, a radial grid was created by opening B13 and B31. The peak |dv/dt| values and the relay responses were recorded. Selected sample results are presented in **Table 2.7, Table 2.8,** and **Table 2.9**.

Table 2-7 Responses for bus faults in the radial network (© Elsevier)

Loc.	R_F (Ω)	Peak |dv/dt| (kV/ms)					Responses	
		$\dot{V}_1$	$\dot{V}_{14}$	$\dot{V}_{41}$	$\dot{V}_2$		R_{1Y}	Other
Bus-1	0.01	5389	109	97	463		T	NT
		5389	10285	97	463			NT
Bus-1	50	2722	48	48	146		T	NT
		2722	10083	48	146			NT
		$\dot{V}_4$	$\dot{V}_{41}$	$\dot{V}_{42}$	$\dot{V}_{43}$	$\dot{V}_{34}$	R_{4Y}	Other
Bus-4	0.01	5372	97	102	1782	1465	T	NT
		5372	10207	10133	7081	2808		R_{34}
Bus-4	200	3223	73	76	952	757	T	NT
		3223	10150	11564	7789	2173		R_{34}

Table 2-8 Responses for line faults on C-14 in radial network (© Elsevier)

Loc. (km)	R_F(Ω)	Peak |dv/dt| (kV/ms)					Responses		
C-14		$\dot{V}_{14}$	$\dot{V}_1$	$\dot{V}_{41}$	$\dot{V}_4$	$\dot{V}_{43}$	R_{14}	R_{14}	Other
0	0.01	5432	342	1294	488	317	T	T	NT
		11133	665	10891	3907	1318			NT
250	10	1342	91	1343	488	219	T	T	NT
		10834	714	10749	3858	1294			NT
500	50	256	24	1074	390	146	T	T	NT
		10559	720	9474	3443	927			NT

Table 2-9 Responses for line faults on OHL-34 in radial network(© Elsevier)

Loc.(km)	**R_F (Ω)**	**Peak |dv/dt| (kV/ms)**					**Responses**		
OHL-34		$\dot{V}_{34}$	$\dot{V}_3$	$\dot{V}_{43}$	$\dot{V}_4$	$\dot{V}_{41}$	R_{34}	R_{43}	Other
0	0.01	5470	341	4249	1416	24	T	T	NT
		11257	634	8278	2759	48			NT
300	10	4224	244	3492	1172	24	T	T	NT
		7301	439	7203	2417	48			NT
1500	100	2808	146	3833	1269	24	T	T	NT
		7472	439	9987	3345	73			NT

The results show that the network reconfiguration does not considerably change the peak |dv/dt| values measured during the faults. This is because the di/dt limiting inductors installed at line ends acts as low pass filters (as theoretically explained in **Section-2.3**) and essentially isolate the different sections of the network for high-frequency transients. Thus, the removal of one network element has only a minor effect on the magnitudes of the traveling waves observed at the line side of the di/dt limiting inductor of an in-service line (for faults on that line).With the proposed directional supervision, the peak |dv/dt| observed at the line side of the inductor is the most important factor for fault detection and discrimination. As the peak |dv/dt| is not affected by the network topology changes, the proposed protection scheme is robust against minor network topology changes. However, changes in the line flows alter the peak |dv/dt| values due to the breaker opening. Note that the column corresponding to the R_{1Y} indicates the responses of bus protection logic at all relays connected to Bus-1.

2.5.6. Performance Under Different Earthing Points

Transmission lines and/or converter outages may demand a change of earthing point on the metallic return conductor. The influence of earthing point changes on protection settings and the operation of the proposed method was evaluated. Some sample results taken after moving the earthing point from Bus-3 to Bus-2 are presented in **Table 2.10** –**Table 2.12**. A reduction of peak |dv/dt| at the line side of the terminal inductors was observed when the earthing point is moved away from a line. In contrast, a reduction of peak |dv/dt| on a bus was observed when the earthing point is moved closer to the bus. However, most of the times these reductions are less than 10% and did not require a change of $ROCOV_L$ or $ROCOV_B$ settings.

Table 2-10 Relay responses for faults on OHL-34 when the earthing point is changed

Loc. (km)	R_F (Ω)	Peak |dv/dt| (kV/ms)					Responses		
OHL-34		V'_{34}	V'_3	V'_{31}	V'_{43}	V'_4	R_{34}	R_{43}	Other
0	0.01	5470	1367	634	3589	1196	T	T	NT
		10769	1587	903	3589	1196			NT
900	0.01	3003	360	244	3785	1268	T	T	NT
		8278	1001	488	8498	2892			NT
1500	100	2588	463	219	3858	1294	T	T	NT
		7326	1025	488	10134	3594			NT

Table 2-11 Relay responses for faults on cables when the earthing point is changed (© Elsevier)

Loc.(km)	**R_F (Ω)**	**Peak |dv/dt| (kV/ms)**					**Responses**		
C-24		$\dot{V}_{24}$	$\dot{V}_2$	$\dot{V}_{42}$	$\dot{V}_4$	$\dot{V}_{43}$	R_{42}	R_{24}	Other
0	50	1318	75	1076	410	122	T	T	NT
		10462	586	10794	3871	1269			NT
50	10	2759	170	2769	1025	415	T	T	NT
		10940	586	10923	3748	1343			NT
100	0.01	5396	317	6564	2332	879	T	T	NT
		11184	586	11487	4282	1309			NT
C-14		V'_{14}	V'_1	V'_{13}	V'_{41}	V'_4	R_{14}	R_{41}	Other
0	50	1086	67	24	268	97	T	T	NT
		10718	634	293	19104	610			NT
250	10	1355	79	98	1367	488	T	T	NT
		16884	622	268	10647	3858			NT
500	0.01	1300	85	97	5421	1978	T	T	NT
		11060	622	219	10940	3907			NT

Table 2-12 Relay responses for bus faults when the earthing point is changed (© Elsevier)

Loc.(km)	R_F (Ω)	Peak |dv/dt| (kV/ms)					Responses	
Bus-2		V'_2	V'_{24}	V'_{42}	V'_4	V'_1	R_{24}	Other
	0.01	5396	122	179	102	24	T	NT
		5396	9816	205	102	24		NT
	10	4590	73	102	51	24	T	NT
		4590	10818	256	128	24		NT

Bus-3		V'_3	V'_{31}	V'_{34}	V'_{43}	V'_{13}	R_{3Y}	Other
	0.01	5445	2246	2466	1245	1758	T	NT
		5445	2246	2466	1245	1758		R_{13}
	200	2002	796	1074	488	683	T	NT
		2002	4126	3321	1123	1391		NT
Bus-4		V'_4	V'_{41}	V'_{42}	V'_{43}	V'_{34}	R_{4Y}	Other
	0.01	5421	97	102	1782	1318	T	NT
		5421	10207	10719	7130	2490		R_{34}
	200	3247	48	51	952	684	T	NT
		3247	10329	10589	8567	1245		NT

2.6. Discussion

The protection scheme was further evaluated by changing the power flow direction and the power transfer level. However, regardless power flow direction and the power transfer level, the proposed protection scheme was capable of accurately detecting all the simulated faults. For the test grid considered, a fault with 50 Ω or more resistance at any location on a cable or overhead line, resulted a steady-state fault current less than 6.4 kA, which is assumed less than 50% of the DCCB breaking capacity. Thus, the proposed protection scheme is capable of detecting any fault causing a steady-state fault current above the breaker capacity in less than 200 μs, regardless of changes in the operating conditions or network topologies.

2.7. Concluding Remarks

A peak ROCOV based protection scheme for an MT-HVDC grid was proposed. The line end di/dt limiting inductors, which are essential for allowing sufficient operating time for DCCBs, enable the fault discrimination based on the peak |dv/dt| values observed at the line side of the inductors. The direction of a fault with respect to a terminal inductor can be reliably determined by comparing the peak |dv/dt| values observed at its two ends. The fault direction determined with the local measurements can be combined with the peak |dv/dt| thresholds to develop a sensitive and secure line and bus protection relays. It was shown that the inclusion of a small inductor of about 2.5 mH-5 mH in the DMR conductor improves the directional protection function in bipole HVDC grids with a single point earthed return wire. The proposed protection scheme was tested on an MT-HVDC grid which was simulated in PSCAD/EMTDC. It was shown that the proposed protection scheme is capable of detecting any fault that is causing a steady-state fault current beyond the breaker rating in less than 200 μs by using only local measurements. With the proposed method, better fault discrimination can be achieved by introducing a small terminal inductor. A protection system with the settings determined under the normal operation is capable of detecting faults even after changes in the operating conditions or the HVDC grid configuration. The proposed protection scheme can be easily implemented with readily available hardware: a voltage sensor having a bandwidth of 10 kHz, 25 kHz sampler, and a 12 bit analog to digital converter.

Chapter 3

Fault Type Identification in HVDC Transmission Systems

3.1. Introduction

In this chapter, the problem of identifying the fault type in HVDC transmission systems is investigated. The knowledge of faulted conductors is especially important in bipole HVDC systems for exploiting the redundancy, and in MT-HVDC grids, identification of fault type needs to be completed within an extremely short time interval as discussed in the previous chapters. In the next few sections, the related background and the related past work are examined, a novel generic approach for identifying the conductors involved in a fault is developed, and its applicability for a verity of HVDC transmission configurations is verified using detailed simulations. The robustness of the method, its advantages and limitations are also discussed. The work presented in this chapter is based on the following publications:

[B] M. H. Naushath, A. D. Rajapakse, "Fault Type Discrimination in HVDC Transmission Lines Using Rate of Change of Local Currents," *IEEE Trans. Power Del.*, vol. 35, no. 01, pp. 117-129, Feb. 2020.

[C] M. H. Naushath, A. D. Rajapakse, "A single pole to ground fault location method for HVDC transmission lines based on coupling characteristics," *In Proc. IET International Conference on AC and DC Power Transmission*, Coventry, UK, Feb. 2019.

[D] M. H. Naushath, A. D. Rajapakse, " Identification of Faulty Conductors in HVDC Links Connecting Future Offshore Wind Sites," *In Proc. IET International Conference on Developments in Power System Protection*, Liverpool, UK, Mar. 2019.

3.2. Background and Literature Review

Prompt identification of the conductors involved in a fault is vital to exploit the redundancy in the bipole HVDC transmission configuration and thereby to minimize the disruption to power flow in the healthy parts of the system [40]. The speed of fault type identification is particularly important in VSC based bipole MT-HVDC transmission systems where the fault clearing needs to be accomplished within several milliseconds. This is because the fault currents in VSC HVDC systems rise rapidly and the overcurrent capacity of semiconductor switching devices used in VSCs is limited [104].

A number of techniques have been recently proposed to detect DC faults and identify the faulted section in MT-HVDC transmission systems within a sub-millisecond time frame [41-42]. These techniques, however do not explicitly address the issue of fault type identification, which is difficult due to electromagnetic coupling between the conductors of a bipole HVDC transmission system; a close-up pole-to-ground short circuit can cause a strong induced transient on the conductor of the healthy pole [43]. Since the coupling is more prevalent at higher frequencies, the independent pole by pole fault detection schemes based on the high-frequency current components or the derivative of voltages [43, 106] is more prone to false operation during the faults on the other pole. A typical approach to avoid false responses is to use less sensitive thresholds. The use of higher thresholds to prevent false operations (as in [41-42]) will lower the sensitivity and selectivity. If a reliable fault type discrimination algorithm is available to supervise the main protection functions, more sensitive settings can be applied to improve the protection performance.

Successful identification of the faulty pole is only a part of the information required to make a protection decision. When a DMR conductor is present, if a pole-to-DMR fault cannot be discriminated from a pole-to-ground fault, it is not possible to decide whether the monopole operation is safe [40]. This is also important to identify potential safety hazards for the repair crews [104]. Due to the challenging nature of the problem, artificial intelligence-based fault classifiers [106] are often proposed in the literature for identifying the fault type in HVDC transmission systems.

A novel fault type discrimination scheme is developed in this chapter using only the local current measurements through all of the conductors accessible at the DC line terminal. The scheme depends on relatively low-frequency components (< 1 kHz) in the measured terminal currents. The decisions are based on a simple set of indices computed considering a pair of conductors at a time. Each index, computed as the ratio between the maximum rates of change of currents (ROCOC) observed in the corresponding conductor pair, is used to determine whether the fault is in the two respective conductors. Therefore, the implementation is straightforward when compared to the previously published methods such as the one in [40], and does not involve laborious training phases required in the machine learning-based methods [107]. The method is reliable, because these indices are more or less independent from the fault resistance, unlike the parameters proposed in [40]. Since the local current measurements are required for both converter control and fault detection [108-109], the proposed low-frequency current measurement based fault discrimination algorithm can be implemented with little or no additional cost using already available measurements. As the proposed method relies only on local measurements, communication links are not necessary as in the current differential schemes [40] and therefore it operates faster. Since it is fast, the method can be used for supervising protection and blocking converter poles. Notably,

the proposed method is applicable for discriminating pole-to-ground faults from pole-to-DMR faults. Therefore, it can also be used for control purposes and to warn repair crews on possible health hazards.

The method proposed is more generic, more reliable, and simpler compared to the previously published algorithms for identifying the poles and the conductors involved in a DC fault; yet it is very fast and accurate. Furthermore, the proposed method is applicable to discriminate all possible types of faults in a given transmission configuration. The method can be applied to bipole two-wire or three-wire systems, LCC or VSC systems, overhead lines or cables, or two terminal or multi-terminal systems. In this thesis, the method is verified in following HVDC transmission configurations.

1. Two-conductor and three-conductor HVDC link terminated with LCC stations.
2. Three-conductor overhead transmission line and cables terminated with VSC stations or non-converter buses in a multi-terminal HVDC transmission system.
3. Non-homogeneous transmission system where two-conductor submarine cable system originating from a VSC rectifier station connected to an LCC inverter station through a three-conductor overhead transmission.

One of the indices calculated for a pole-to-ground fault is a single-valued function of fault location and independent of the fault resistance. Therefore, the ability to locate single pole-to-ground faults using this index is also investigated.

3.3. Fault Type Identification Logic

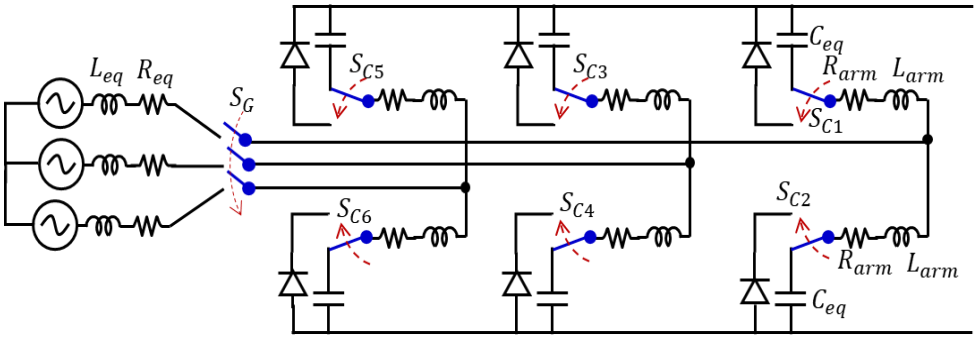
In order to demonstrate the logic behind the proposed fault type identification, the expected variation of terminal currents in a three-conductor bipole HVDC transmission systems during the

DC side faults is investigated. Different types of DC side faults are simulated with the help of a simplified circuit model. DC fault characteristics of an MMC is considered for this demonstration. With the help of observations, the expected nature of the fault current variation is explained and the logic is developed.

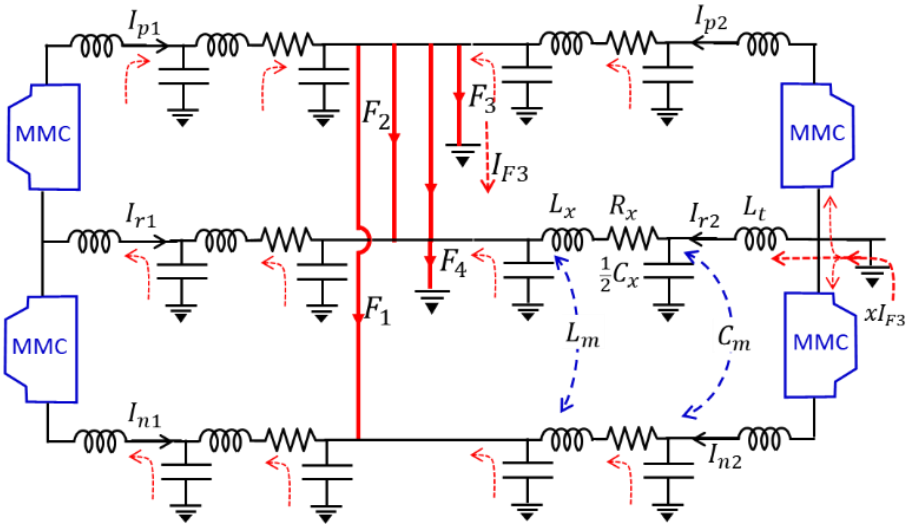
The logic is based on the calculated values of a number of indices that compare the maximum rates of change of currents through each conductor for a short time window of measurement after a fault. With the help of calculated values for indices, the faulty pole(s) and the involvement of DMR conductor in the fault are determined.

3.3.1. Modeling the Behavior of Faulted MMC-HVDC Systems

Due to economic reasons, most of the MMC-HVDC converter stations are built using half-bridge submodules. The DC side fault current from a half-bridge MMC follows three distinct stages [109]. Immediately after the DC fault, a very high rate of change of current is observed as the DC capacitors of connected submodules discharge rapidly. The fault behavior of the converter during this phase can be represented in the form of a series RLC circuit as shown in **Fig. 3.1(a)** [109]. The capacitor initial voltage can be determined considering the pre-fault submodule voltages. The low-level internal protection of the converter detects this rapid rise of current and turns-off IGBT switches. Once all the submodule capacitors are blocked, the second stage of fault transient begins. During this second stage, the lower and upper arms of the converter are effectively shorted and therefore, the stored energy in the arm inductors and line inductance decays through the IGBT anti-parallel diodes. Eventually, MMC becomes an uncontrolled rectifier in Stage-3. During Stage-3, the fault current becomes steady and contains only the contribution from the AC grid.



(a)



(b)

Fig. 3-1. Simplified representation of a faulted MMC HVDC system (a) MMC, (b) three-conductor transmission system (©IEEE)

The duration of stage-1 could be less than 1 ms (2 pu current threshold is typical [110]), while stage-2 could extend well over 100 ms [111]. The circuit shown in **Fig. 3.1(a)** can be used to mimic the fault behavior of a half-bridge submodule based MMC [109]. At the end of Stage-1, the positions of switches S_{CN} (N=1… 6) are changed and the ganged switch S_G is closed to simulate the changing circuit conditions, as shown in **Fig. 3.1(a)**.

The simplified HVDC transmission system shown in **Fig. 3.1(b)** consists of a three-conductor transmission line and MMCs represented using the converter model shown in **Fig. 3.1(a)**. This circuit can be used to predict the typical fault behavior of a bipole VSC based HVDC transmission system with a DMR conductor. Typically, the DMR conductor is grounded only at

one point. In this example, the DMR conductor is grounded at end-2, which is the inverter side. For simplicity, the transmission line in **Fig. 3.1(b)** is represented as two π-equivalent circuits. All conductors are assumed to be terminated with series di/dt limiting inductors [91].

3.3.2. Basis of Identifying the Conductors Involved in a Fault

The fault currents shown in **Fig. 3.2** demonstrate the typical variations observed immediately after a metallic P-pole-ground fault. For this fault, only the IGBTs in P-pole MMCs were blocked, because N-pole is not involved in the fault. The possible fault current paths for a P-pole-to-ground fault are indicated in **Fig. 3.1(b)**.

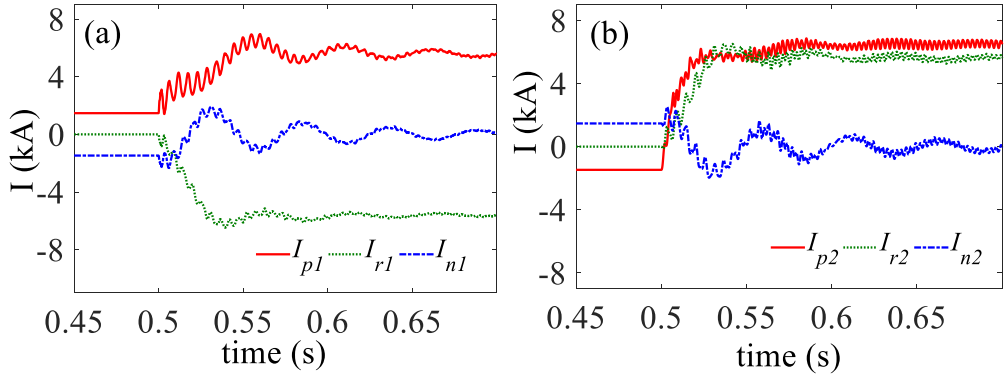


Fig. 3-2. Current waveforms during a P-pole-to-ground fault (a) at ungrounded MMC (b) at grounded MMC (© IEEE)

During Stage-1 and at the beginning of Stage-2, the fault current contribution from the ungrounded converter can come through both N-pole and DMR conductors as well as through the line capacitances. Although only the P-pole conductor is involved in the fault, currents in all three conductors are subjected to transient variations, making it difficult to determine the type of fault. In a longer time scale, the currents in the healthy pole will be restored by the converter controls, which are not modeled in this simplified representation. In **Fig. 3.3**, the computed changes in the currents, i.e. the fault current minus the respective pre-fault current ($\Delta I_{p1}, \Delta I_{n1}, \Delta I_{r1},$), are shown

for the ungrounded MMC (rectifier) side for four different types of faults. The considered faults are (i) P-pole-to-N-pole, F_1, (ii) P-pole-to-DMR, F_2, (iii) P-pole-to-ground, F_3, and (iv) P-pole-to-DMR-to-ground, F_4, faults. The plots show the variations of current changes immediately after the faults, over a much shorter period (about 3 ms). To illustrate the effects of mutual coupling and the details of the line model on the transient response, the plots in **Fig. 3.3** show three different curves for the same quantity, obtained using three different line models. The line models are: (i) distributed parameter line model, noted as "*tl*", (ii) coupled π-model, noted as 'π1", and (iii) uncoupled π-model, noted as 'π2".

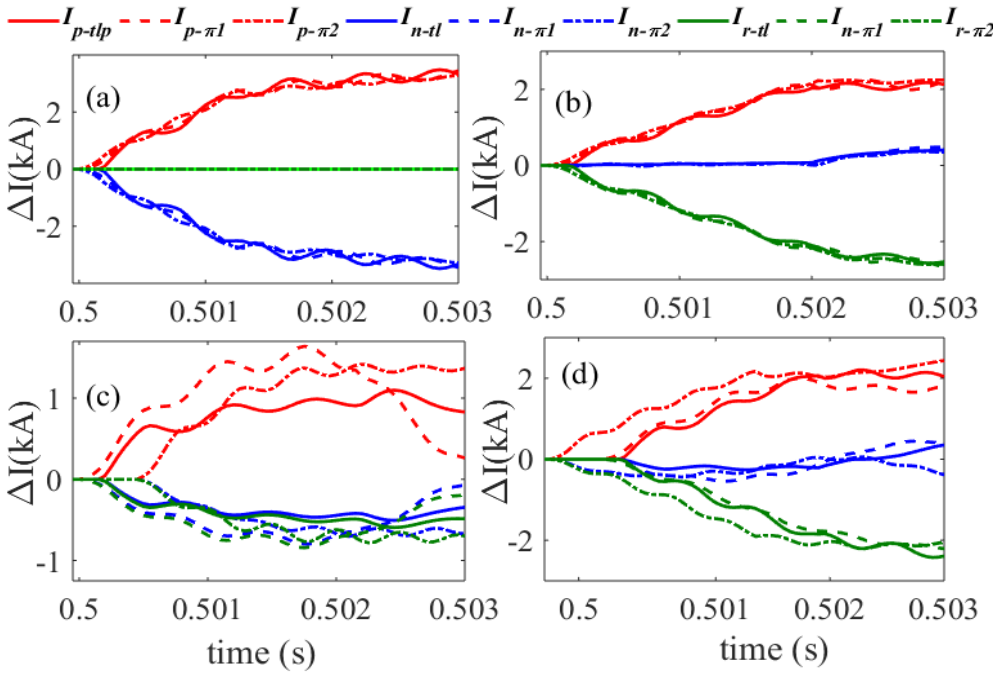


Fig. 3-3. Changes in the conductor currents at the ungrounded MMC for (a) F_1 (b) F_2, (c) F_3, and (d) F_4 (© IEEE)

The parameters used for the simulations are given in **Table A.1** and **Table A.2** of the **Appendix-I**. **Fig. 3.4** shows the corresponding changes in currents observed at the grounded MMC (inverter side $\Delta I_{p2}, \Delta I_{n2}, \Delta I_{r2}$) for four different fault types.

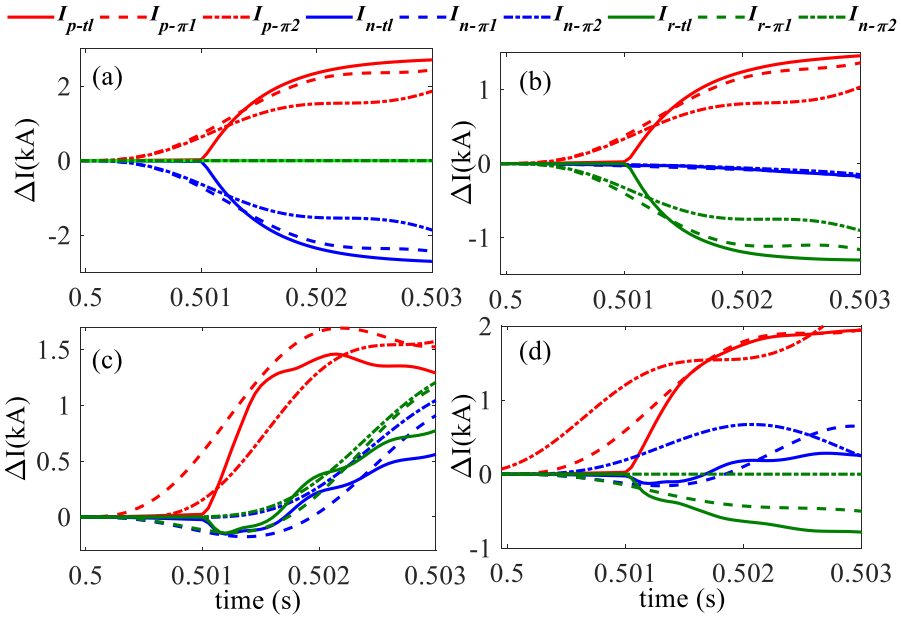


Fig. 3-4. Changes in the conductor currents at the grounded MMC for (a) F_1 (b) F_2, (c) F_3, and (d) F_4 (© IEEE)

Based on the results shown in **Fig. 3.3** and **Fig. 3.4**, the following conclusions can be made:

1. For pole-to-pole faults (such as F_1), as shown in **Fig. 3.3(a)** and **Fig. 3.4(a)**, the initial changes in the faulted conductor (P- and N-pole conductor) currents follow the same pattern, but in opposite directions. The healthy conductor (DMR) current remains unchanged.
    a. These observations are true, regardless of (i) whether the MMC is grounded or not, (ii) the type of line model used.
    b. Although, the line model causes differences in the actual variations, for example, the distributed parameter line model clearly shows current wave travel delays, the general observation is still true.
2. For pole-to-DMR faults (such as P-pole-to-DMR fault F_2) shown in **Fig. 3.3(b)** and **Fig. 3.4(b)**, the initial change in the faulted conductor currents follow the same pattern, but in opposite directions. The healthy conductor (N-pole in the case of F_2) current remains more or less unchanged during the initial period.

a. Again, the observations are true for both grounded and ungrounded MMCs, regardless of the line model used.

3. During pole-to-ground faults (such as P-pole-to-ground fault F_3) shown in **Fig. 3.3(c)** and **Fig. 3.4(c)**, the initial changes in the healthy conductor currents follow the same pattern and vary in the same direction. The faulted conductor (P-pole in the case of F_3) current changes faster than the healthy conductor currents in the opposite direction.
   a. When the distributed line model or coupled π-model is used, the healthy conductor currents at the grounded and ungrounded MMCs show the same initial direction of variation.
   b. If the coupling between the conductors is ignored, the directions of the initial current variations are different for the grounded MMC.
4. During the pole-to-DMR-to-ground faults (such as P-pole-to-DMR-to-ground fault F_4), as shown in **Fig. 3.3(d)** and **Fig. 3.4(d)**, the faulty pole conductor (P-pole in the case of F_4) current changes much faster than the healthy pole conductor (N-pole in the case of F_4) current, regardless of whether the MMC is grounded or not.
   a. If the inter-conductor coupling is considered, the DMR current changes in the direction opposite to that of the faulted pole-conductor current at both the grounded and ungrounded MMCs.
   b. When the inter-conductor coupling is ignored, the DMR current at the grounded MMC remains unchanged.

The reasons for the above observations arise from the paths of the fault currents during Stage-1 and at the beginning of Stage-2. The possible paths for P-pole-to-ground fault currents are indicated in **Fig. 3.1(b)**. Based on the above observations, a procedure can be formulated to

identify the type of fault and the conductors involved, considering the initial change of conductor currents after a fault. The ROCOC facilitates detecting the trend of a current variation faster than the magnitude of the current could, and therefore, the initial rate of change of conductor currents can be used in place of the magnitudes of the current changes. In fact, ROCOC has been commonly used as a fault indicator in HVDC systems [101-102]. A technique capable of identifying the fault type using the above-mentioned features of fault currents is developed next.

3.3.3. ROCOC Based Fault Type Indices

Although the fault resistance and the fault location can influence the actual magnitudes of the initial rate of change of conductor currents, the conclusions made in **Section-3.3.2** are all based on the relative variations in the change of currents; therefore, they should hold true regardless of the fault resistance or the fault location. In order to formulate the necessary logic using the relative rate of change in currents, the index F_{XY} is defined to express the rate of change of current in Conductor-X relative to that of Conductor-Y [112].

$$F_{XY} = \frac{\left|\frac{d\Delta I_x}{dt}\right|_{initial}}{\left|\frac{d\Delta I_y}{dt}\right|_{initial}} = \frac{\left|\frac{dI_x}{dt}\right|_{initial}}{\left|\frac{dI_y}{dt}\right|_{initial}} \tag{3.1}$$

The pre-fault ROCOC is assumed to be insignificant when compared with the initial ROCOC during a fault. According to the observations presented in the previous section, F_{XY} is closer to unity when:

1. the fault is between Conductor-X and Conductor-Y (hereafter referred to as the criterion for identifying faulty conductors during inter-conductor faults) or
2. both Conductor-X and Conductor-Y are not involved in the fault, for example during a

ground fault on the remaining conductor (hereafter referred to as the criterion for identifying healthy conductors during single conductor faults).

This approach of pairwise comparison can also be identified as a test whether or not a fault is inside the loop between the two terminals where measurements are taken. In the latter case, both conductors are not involved in the fault. Furthermore, F_{XY} is greater than unity when Conductor-*X* is involved in the fault while Conductor-*Y* is not; and F_{XY} is less than unity when Conductor-*X* is not involved in the fault while Conductor-*Y* is involved.

Faulty conductor identification is greatly simplified when using an index such as F_{XY} defined in (3.1). The pairwise comparison approach avoids the impact of fault resistance and mitigates the influence of the fault location to a certain extent. It should be noted that the above observations made considering the initial changes in currents during the transient period immediately after a fault and may not hold for steady-state fault currents.

In order to arrive at robust decisions which are less prone to noise, the index defined in (3.2) is proposed [112]:

$$F_{XY}(t) = \frac{\max\left(dI`_x/dt\right)}{\max\left(dI`_y/dt\right)} \tag{3.2}$$

The currents $I`_x$ and $I`_y$ in (3.2) are acquired by applying a low pass filter to the current measurements I_x and I_y in Conductors-*X* and -*Y* respectively. The maximum rates of change of $I`_x$ and $I`_y$ are calculated considering a short time window after the fault detection. Higher conductor coupling at higher frequencies (> 5kHz) makes it difficult to discriminate the faulty pole from the healthy pole. Complete elimination of mutual coupling may make it impossible to identify the ground faults at the grounded converter. As explained in **Section-3.3.2**, the initial direction of the change of current observed at the grounded MMC was different when the mutual coupling is

ignored. Therefore, the cutoff frequency of the filter should be carefully selected so that the right degree of variation in the currents due to mutual coupling between the conductors is captured. More details on selecting a proper cut-off frequency will be presented in **Section-3.4.1.2**.

Several indices are defined for three-conductor configuration (i) considering a pair of current measurements in a possible fault current loop, or (ii) considering a pair of current measurements in healthy conductors, as illustrated in **Fig. 3.5**. As the aim of calculating each index is to capture the ratio between the first positive peaks of the rate of change of current observed at the two ends of a possible fault current loop, the direction of measurement is important in calculating the index defined in (3.2). Indices defined in **Section-3.3.5** are based on the assumption that all currents are measured from a converter toward the line, as indicated in **Fig. 3.5**.

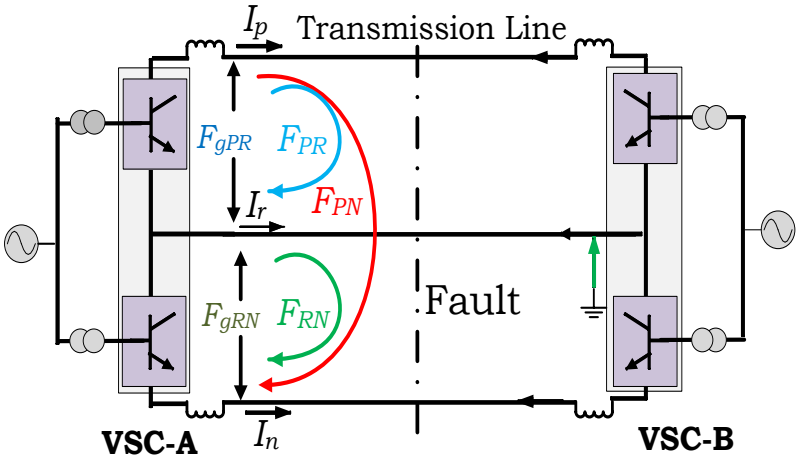


Fig. 3-5. Current measurements considered for different indices (© IEEE)

3.3.4. Signal Processing and Calculation of Indices

The signal processing functions involved in calculating the indices are shown in **Fig. 3.6**. After applying a polarity correction, each measured current is sent through a low pass filter.

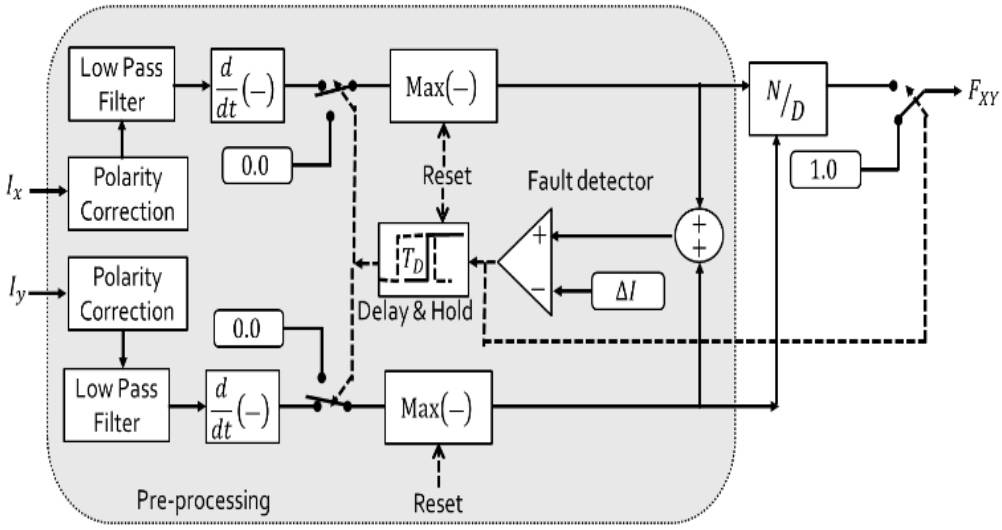


Fig. 3-6. Signal processing involved in calculating F_{XY} (© IEEE)

Then the maximum rate of change of each filtered current signal is computed and passed on to trigger the logic and ratio calculation blocks. The di/dt based fault detection logic triggers the algorithm when the sum of two maximum di/dt values exceeds a pre-set threshold, ΔI, and starts a timer. This trigger signal can be replaced with the output of an alternative fault detection method such as [42, 113-120], if needed. The output of the delay and hold is set to high after a short time delay of T_D. When the delay and hold output is set, inputs to the maximum value detectors are switched to zero, causing the outputs of the maximum di/dt detectors to freeze at their values after a delay of T_D from the time of detecting the fault. The fault detector also directs the ratio of the outputs of two maximum detectors to the final output as the value of F_{XY}. The maximum value detectors need to be reset after detecting a fault.

3.3.5. Faulty Conductor Identification Logic

The criteria used to identify the faulted conductor is developed in this section. Five indices are defined. The first index, F_{PN}, is defined to identify the faulty pole. The next two indices, F_{PR}

and F_{RN}, are used to identify P-pole-to-DMR faults and N-pole-to-DMR faults. The remaining two indices F_{gRN} and F_{gPR} are used to identify P-pole-to-ground faults and N-pole-to-ground faults.

3.3.5.1. The Logic for Identification of Faulty Pole(s)

The index F_{PN} used to identify the faulty pole(s) is defined as

$$F_{PN} = \frac{Max\left(dI`_p/_{dt}\right)}{Max\left(-dI`_n/_{dt}\right)} \quad \textbf{(3.3)}$$

According to the discussion in **Section-3.2.3**, the following criteria hold:

Criterion-A1: for a P-pole-to-N-pole fault,

$$(1 - k_1) \leq F_{PN} \leq (1 + k_2)$$

Criterion-A2: for P-pole-to-ground or P-pole-to-DMR faults,

$$F_{PN} \geq (1 + k_2)$$

Criterion-A3: for N-pole-to-ground or N-pole-to-DMR faults,

$$F_{PN} \leq (1 - k_1)$$

where $k_1$to k_2 are positive tolerance settings. *Criterion-A1* helps to discriminate a P-pole-to-N-pole fault from a single-pole-to-ground fault or a single-pole-to-DMR fault.

3.3.5.2. The Logic for Identification of Pole-to-DMR Faults

A P-pole-to-DMR fault can be identified by comparing the maximum ROCOC values of P-pole current and DMR current. Therefore, index F_{PR} defined in (3.4), which compares the loop current through a P-pole and DMR conductors, can be used to identify P-pole-DMR [112].

$$F_{PR} = \frac{Max\left(dI`_p/_{dt}\right)}{Max\left(-dI`_r/_{dt}\right)} \tag{3.4}$$

The negative of the DMR current is considered in (3.4) since the fault current flows along the DMR conductor into the converter during a P-pole-to-DMR fault. Similarly, the index to identify an N-pole-to-DMR fault, F_{RN}, is defined in [112] as

$$F_{RN} = \frac{Max\left(dI`_r/_{dt}\right)}{Max\left(-dI`_n/_{dt}\right)}. \tag{3.5}$$

The following criteria hold for pole-to-DMR faults.

Criterion-B1: for a P-pole-to-DMR fault,

$$(1 - k_3) \leq F_{PR} \leq (1 + k_4)$$

Criterion-B2: for an N-pole-to-DMR fault,

$$(1 - k_3) \leq F_{RN} \leq (1 + k_4)$$

where $k_3$and k_4 are positive tolerance settings.

3.3.5.3. The Logic for Identification of Pole-to-ground Faults

According to **Section-3.3.3**, the similar magnitudes of ROCOC is expected in healthy conductors during a single pole-to-ground fault. Two indices, F_{gRN} and F_{gPR}, which compare the maximum rates of change of currents through the healthy conductors, can be defined to identify P-pole-to-ground faults and N-pole-to-ground faults respectively using the criterion for healthy conductors during a single-pole-to-ground fault [112].

$$F_{gRN} = \frac{Max\left(-dI`_r/_{dt}\right)}{Max\left(-dI`_n/_{dt}\right)} \tag{3.6}$$

$$F_{gPR} = \frac{Max\left(dI`_p/dt\right)}{Max\left(dI`_r/dt\right)} \tag{3.7}$$

Criterion-C1: for a P-pole-to-ground fault,

$$(1 - k_5) \leq F_{gRN} \leq (1 + k_6)$$

Criterion-C2: for an N-pole-to-ground fault,

$$(1 - k_5) \leq F_{gPR} \leq (1 + k_6)$$

where k_5 and k_6 are positive tolerance settings.

3.3.6. Application to Two-conductor HVDC System

In a bipole HVDC transmission system without a DMR, only the pole conductors are available. Therefore, only the index F_{PN} is computed and the pole(s) involved in the fault is identified with the help of Criterion A1-A3. *Criterion-A1* is used to identify P-pole-to-N-pole faults, and *Criteria-A2* and *-A3* can be used to identify P-pole-to-ground faults and the N-pole-to-ground faults respectively.

3.3.7. Application to a Bipole HVDC Transmission System with a DMR

The number of comparisons and threshold settings used in the basic criteria presented in **Section-3.3.5** can be reduced, if the testing of criteria is performed in an orderly manner. As presented in the flow chart of **Fig. 3.7**, one side of *Criterion-B1*,*-B2*, *-C1*, and *-C2* can be omitted once the faulty pole is identified. *Criteria A1* allows for identifying P-pole-to-N-pole faults.

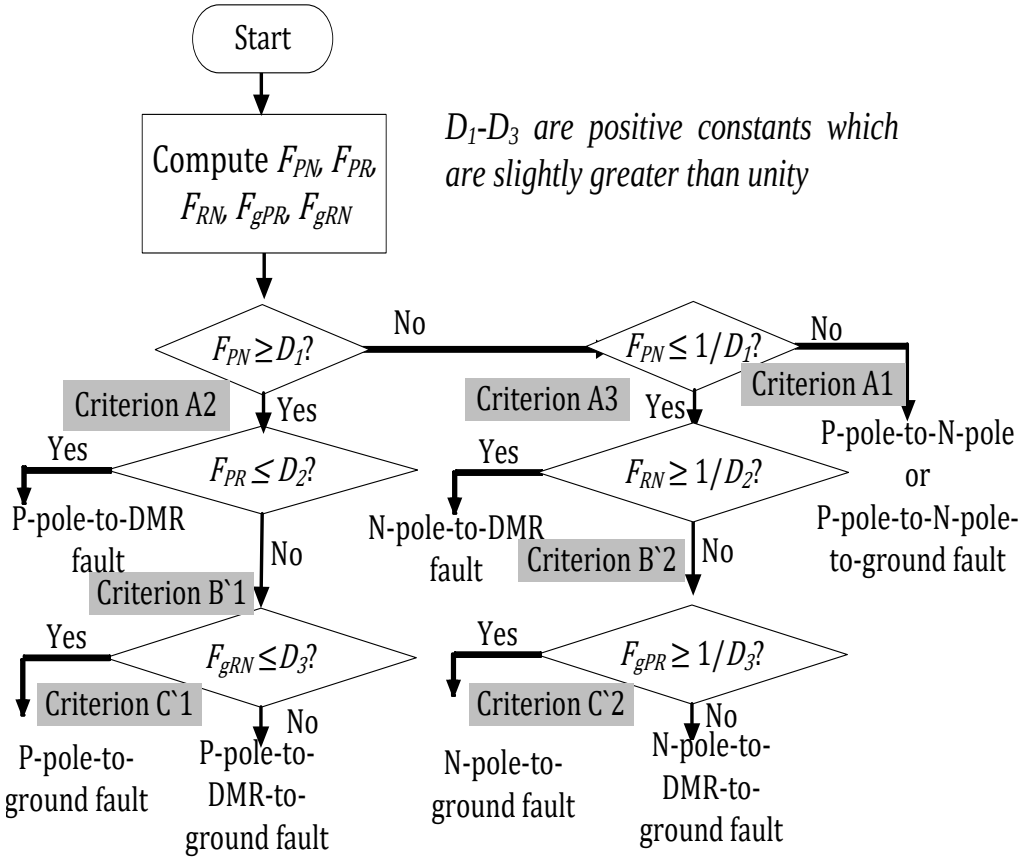


Fig. 3-7. Proposed fault classification algorithm (© IEEE)

When it is not a pole-to-pole fault, the pole involved in a single-pole fault can be identified with the help of *Criteria A2-A3*. The $Max(dI`_p/dt)$ is greater than the $Max(dI`_r/dt)$ for a fault involving the P-pole and the ground with or without DMR. Therefore, F_{PR} is greater than unity for any fault involving the P-pole and the ground while a close to unity F_{PR} is expected for a P-pole-to-DMR fault. Therefore, once the faulty pole is identified, pole-to-DMR faults can be identified by considering the only right-hand side of *Criterion-B1*. Thus, it is only necessary to check whether F_{PR} is less than a threshold to identify P-pole-to-DMR faults. Similarly, only left-hand side of *Criterion*-B2 is considered in identifying an N-pole-to-DMR fault. Thus, it is only necessary to check whether F_{RN} is greater than a threshold which is slightly less than 1.0 to identify N-pole-to-DMR faults. These modified criteria are denoted as *Criterion-B`1* and *Criterion-B`2* in **Fig. 3.7**.

In practical HVDC transmissions systems, the DMR conductor may have a small series inductors than those on the pole conductors or no series inductors. Therefore, due to asymmetrical termination, the rate of change of current in DMR could be higher than that of P- or N-conductors, making the index F_{PR} slightly less than unity during a P-pole-to-DMR fault, and the index F_{RN} slightly higher than unity during an N-pole-to-DMR fault. However, the one-sided comparison also helps to identify the deviations in F_{PR} and F_{RN} from their ideal value, unity, during pole-to-DMR faults due to asymmetry in the terminations.

Any fault which is not a pole-to-pole or a pole-to-DMR fault could be a pole-to-ground fault or a pole-to-ground-to-DMR fault. For a P-pole-to-DMR-to-ground fault, $Max(dI`_r/dt)$ is higher than that of the healthy pole, i.e. $Max(dI`_n/dt)$. Therefore, checking the right-hand side of *Criterion-C1* is sufficient to discriminate a P-pole-to-ground fault from a P-pole-to-DMR-to-ground fault. Using a similar argument, as depicted in **Fig. 3.7**, only left-hand side of the *Criterion-C2* can be used to identify an N-pole-to-ground fault. The thresholds in the modified criteria can be related to k_i values in the original criteria as:$D_1 = 1 + k_2$;$1/D_1 = 1 - k_1$; $D_2 = 1 + k_4$;$1/D_2 = 1 - k_3$; $D_3 = 1 + k_6$; and $1/D_3 = 1 - k_5$.

3.4. Application to Different HVDC Transmission Systems

The algorithm is evaluated by simulating detailed EMT type models of several HVDC transmission systems. Fault type identification is important in bipole MT_HVDC transmission systems as well as in bipole two-terminal HVDC transmission systems. Therefore, the proposed

fault type identification algorithm is validated in the following bipole HVDC transmission system configurations:

1. An LCC based point-to-point bipole HVDC system with overhead transmission lines. Application in the two-conductor system is validated with the test system described in **Section-3.4.1**. Validation of application in a three-conductor system is carried by replacing two-conductor transmission line in the same test system with a three-conductor transmission line. The results are presented in **Section-3.4.1** and **Section-3.4.4**.
2. A VSC based three-terminal bipole HVDC transmission system with three-conductor overhead transmission lines and underground cables. The test system is described in **Section-3.4.2.1**, and the results are presented in **Section-3.4.2** and **Section-3.4.3**.
3. A three terminal hybrid HVDC system with two VSC rectifiers, an LCC inverter and a non-homogeneous link, which consists of a two-conductor cable section and a three-conductor overhead transmission line section. The test system and the results are presented in **Section-3.4.5**.

3.4.1. Faulty Pole(s) Identification in Two-conductor LCC HVDC Transmission Systems

Although the analysis presented in **Section-3.3.2** considered an MMC-HVDC scheme, similar behavior can be observed in LCC-HVDC systems too. This is because the DC side filters in LCC stations provide fault current paths that are similar to those observed during stage-1 of faulted MMCs.

3.4.1.1. Two-Conductor Bipole LCC Test System

This test system features a point-to-point bipole HVDC scheme consisting of twelve-pulse LCCs and a two-conductor overhead transmission line as shown in **Fig. 3.8**. The parameters of the test system shown in **Fig. 3.8** are given in **Table 3.1**.

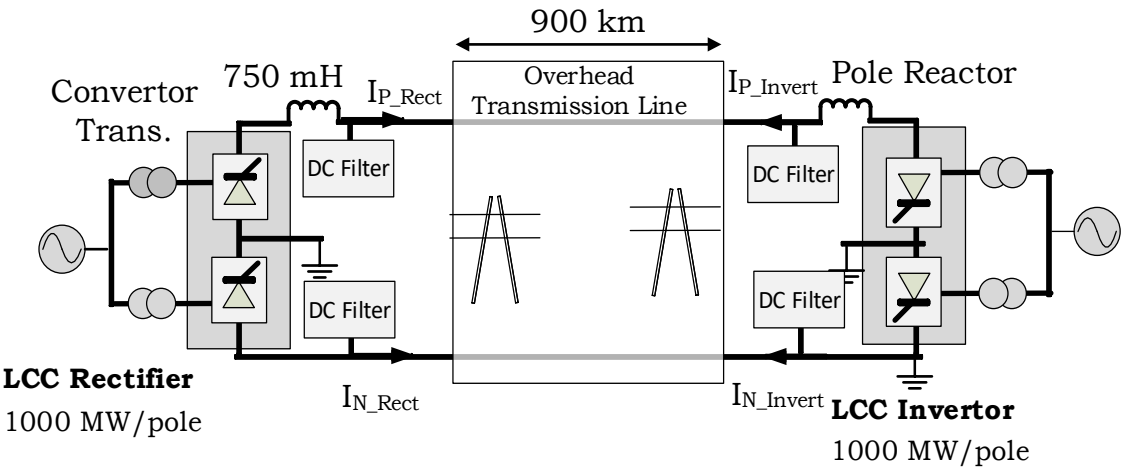


Fig. 3-8. Bipole LCC based two-terminal HVDC test system (© IET)

Table 3-1 LCC test system data (© IEEE)

Parameter	Value	Units
Nominal DC Voltage	±500	kV
Operating point	600	MW/pole
Length	900	km
AC Sys. SCR Rectifier	2.9	
AC Sys. SCR Inverter	5.0	
DC reactor	0.75	H
Cut-off frequencies of DC side shunt filer	720 & 1440	Hz
Cut-off frequencies of AC side shunt filter	540 & 780	Hz
Transformer Data		
MVA	600x2	MW/pole
Leakage Reactance	0.15	pu
Transformer Ratio	230kV/209kV	

The two-conductor overhead transmission line design is similar to that used in Manitoba Hydro's Bipole-II [122] HVDC system. The line length, converter rating, filter design of the test system are the same as Manitoba Hydro's Bipole-II. The details of the transmission line design are given in **Table A3.3** and **Fig. A3-1 of Appendix-I**. Diagrams of the LCC rectifier and inverter are respectively shown in **Fig. A-2** and **Fig. A-3** in **Appendix-I**.

3.4.1.2. Selection of LPF Cut-off Frequency

The indices proposed for fault type identification were computed using low pass filtered current signals. The passband of the low pass filter (LPF) directly affects the computed index. Therefore, it is important to understand the impact of LPF cut-off frequency. This was investigated with the help of calculated values of F_{PN} for different cut-off frequencies of the low pass filter, and the results are shown in **Fig. 3.9**. **Fig. 3.9(a)** shows the calculated values of F_{PN} for metallic N-pole-to-ground faults at three different locations. **Fig. 3.9(b)** shows the variation of calculated values of F_{PN} with the fault location at different cut-off frequencies. According to **Fig. 3.9(a)**, when the cut-off frequency is increased, the value of the F_{PN} computed for N-pole-to-ground faults becomes closer to unity, which is the value of the index corresponding P-pole-to-N-pole faults.

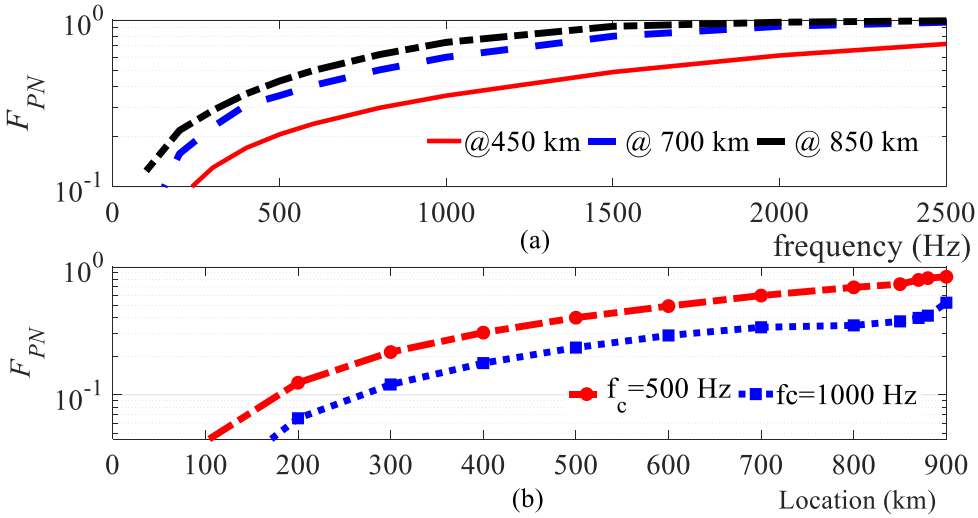


Fig. 3-9. F_{PN} for N pole-to-ground faults in Test System-1 (a) Variation of F_{PN} with LPF cut-off frequency f_c, (b) Variation of F_{PN} with distance (© IEEE)

In order to use *Criteria A1-A3* to distinguish the P-pole-to-N-pole faults from the N-pole-to-ground faults with a satisfactory discrimination margin, the value of F_{PN} should be sufficiently smaller than 1.0 for far-end faults. In order to have at least a 100% margin between N-pole faults and P-pole-to-N-pole faults, the threshold $1/D_1$ needs to be set to ½. As per **Fig. 3.9(a)**, 100% margin for discriminating a solid N-pole-to-ground fault at line end (~850 km) from a P-pole-to-N-pole fault (which result in $F_{PN} \approx 1.0$) can be achieved when the bandwidth of the current signal is limited to about 500 Hz, before computing the ROCOC.

According to **Fig. 3.9(b)**, with a 500 Hz cut-off, F_{PN} is about 0.5 for a fault at the far end (900 km). Thus, 500 Hz was selected as the LPF cut-off frequency. Although even lower LPF cut-off frequency may be used, it would require longer tracking times to capture the peak ROCOC values, leading to delayed decisions. The ROCOC values were computed using the derivative transfer function (sT) with a time constant of 0.01s. The tracking period, T_D, was set to 1 ms to enable tracking the first peak of any signal having a frequency of 250 Hz or higher. The trigger level ΔI was set, to 20 A/ms, considerably higher than the fastest possible current ramping rates.

3.4.1.3. Faulty Pole Identification Using Index *FPN*

The observed rectifier side current transients for a metallic P-pole-to-ground fault at 500km away from the rectifier is depicted in **Fig. 3.10**. As depicted in **Fig. 3.10(b)**, if the frequency band of the filter is not limited (bandwidth > 10 kHz with the simulation time step used), the peak ROCOC values calculated for both P- and N-pole conductors are almost equal. However, in **Fig. 3.10(c)**, a large difference in the peak ROCOC values can be seen when the low pass filtered current measurements (cut-off frequency 500 Hz) are used for ROCOC calculation. Variation of F_{PN} computed using the waveforms in **Fig 3.10(c)** is shown in **Fig. 3.10(d)**.

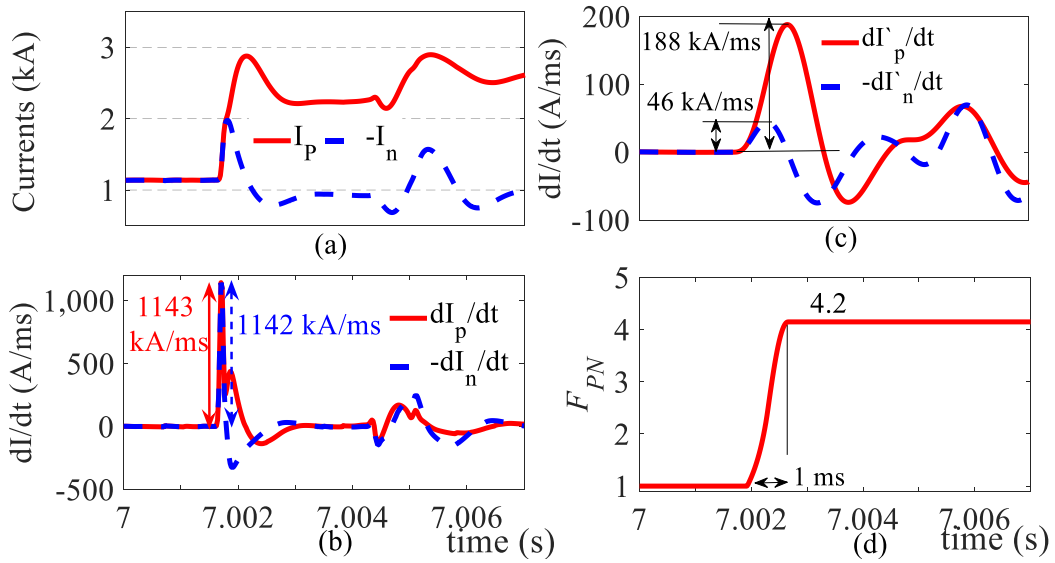


Fig. 3-10. Computing F_{PN} for a P-pole-to-ground fault in bipole, two-conductor system (a) P-pole current, I_p, and N-pole current I_n, (b) ROCOC values, (c) ROCOC values for band limited measurements $I`_p$ and $I`_n$, (d) F_{PN} (© IEEE)

The algorithm follows the ratio between the maximum ROCOC values of P- and N-conductors and freezes its value 1 ms after the detection of a fault. The involvement of P-pole in the fault is indicated by the fulfillment of *Criterion-A2* with a considerable margin (4.2 >> D_1).

Fig. 3.11 shows responses for a solid N-pole-to-ground fault at 300 km away from the rectifier.

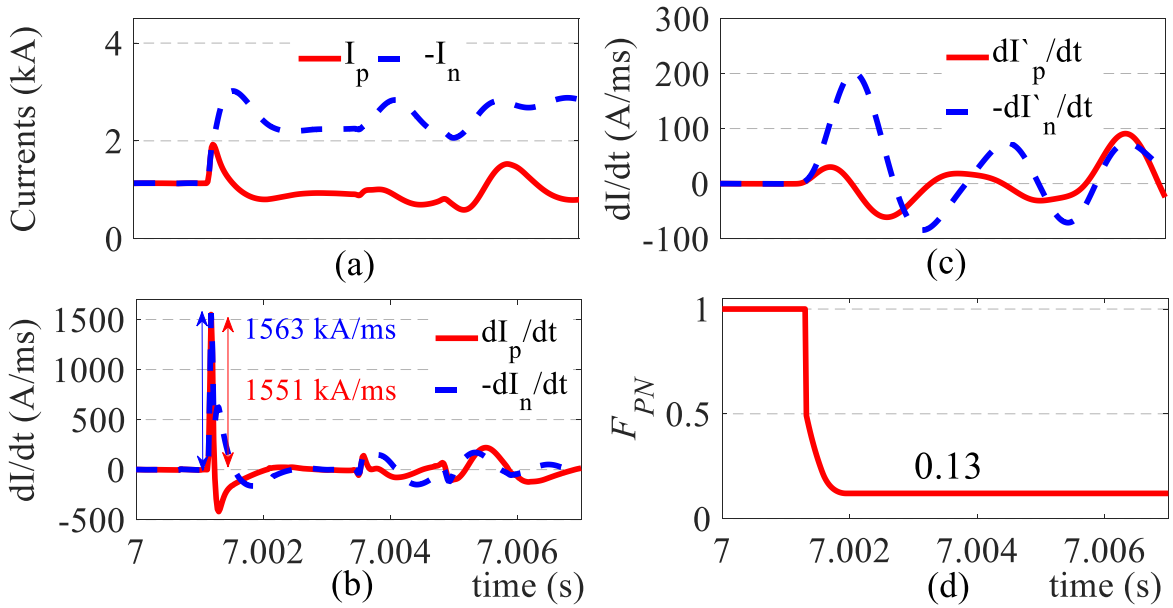


Fig. 3-11. F_{PN} for an N-pole-to-ground fault in bipole, two-conductor system (a) Currents, (b) ROCOC values, (c) ROCOC values for bandlimited signals, (d) F_{PN} (© IEEE)

Although the first peaks of the ROCOC values of the unfiltered measurements are almost equal, the difference becomes clear when the low pass filtered currents (**Fig. 3.11(c)**) are used. Due to the fulfillment of *Criterion-A3* with a good margin ($0.13 << 1/D_1$), it is possible to identify the involvement of N-pole in the fault with the filtered signals. **Fig. 3.12** shows the variation of F_{PN} with fault location for the bipole-two conductor LCC based test system for different fault types.

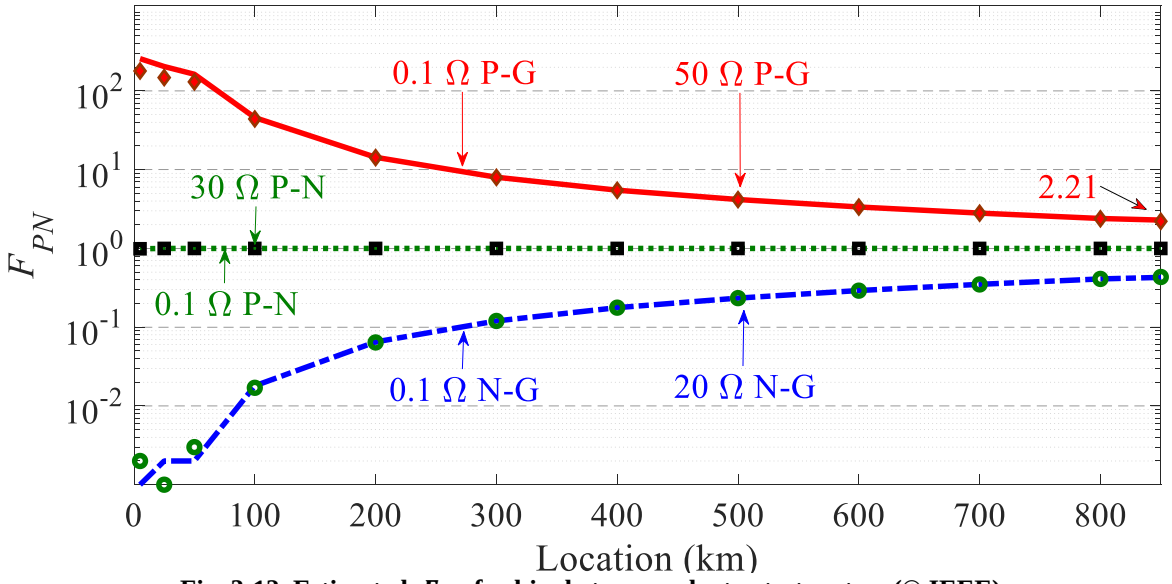


Fig. 3-12. Estimated F_{PN} for bipole two-conductor test system (© IEEE)

In the legend of **Fig. 3.12**, '0.1Ω P-G' indicates the calculated value F_{PN} for 0.1Ω P-pole-to-ground faults and '0.1Ω P-N' shows the index for 0.1Ω P-pole-to-N-pole faults. Based on the results shown in **Fig. 3.12**, the following conclusions can be made:

1. F_{PN} is dependent only on the fault location and the type,
2. F_{PN} is not affected by the fault resistance, and
3. the poles involved in the fault can be easily determined with a sufficient margin. Therefore the thresholds can be easily set.

The narrow margin between the calculated peak di/dt values for the healthy and the faulty conductors shown in **Fig. 3.10(b)** and **Fig. 3.11(b)** indicates the possibility of false triggering of

the HVDC line protection schemes based on di/dt. The proposed method can be used to identify the faulty pole(s) reliably and promptly to enable the relevant protection actions such as blocking the converter of the affected pole, triggering force retardation procedures, etc. Although the earth return mode is not allowed in some parts of the world, faulty pole identification helps to utilize the 50% redundancy during the single-pole-to-ground faults in jurisdictions where it is allowed on a temporary basis during the contingencies.

3.4.2. Fault Type Identification in Three-conductor Overhead Transmission Lines in VSC MT-HVDC Transmission System

For this study, the three-terminal VSC based MT-HVDC transmission system described in **Section-2.5** was modified by opening the breakers across Line-31 because the presence of loop is not important in validating proposed fault type identification scheme. Therefore, the modified test system appears as shown in **Fig. 3.13**. In this test system, all lines are of three-conductor configuration, and the DMR conductor is grounded at station VSC-3 which controls the DC voltage.

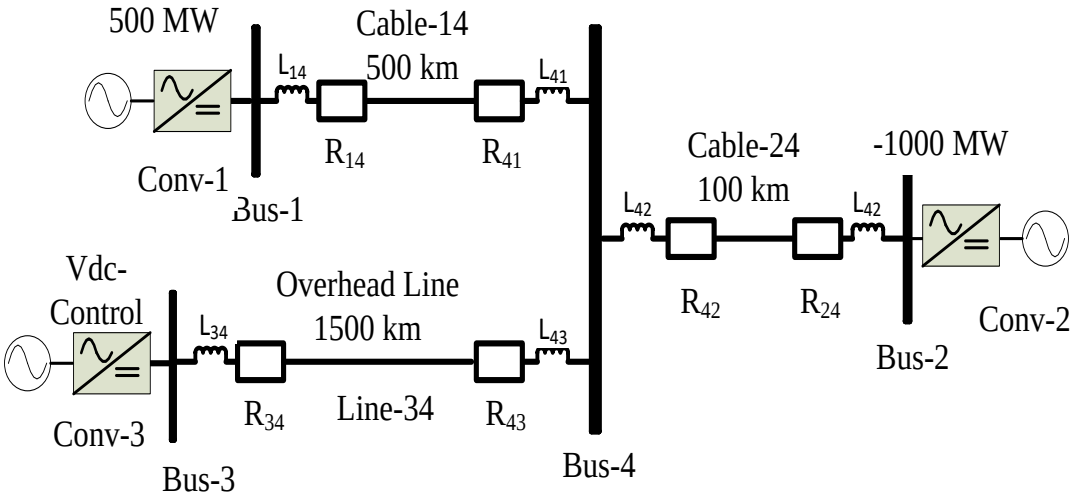


Fig. 3-13. Three-conductor three-terminal VSC HVDC test system model (© IEEE)

The possibility of using the proposed method for identifying

1. the pole(s) involved in a fault, and

2. the involvement of DMR conductor in the fault

is investigated considering the overhead transmission line labeled as Line-34. Note that one end of the considered overhead transmission line is terminated at a converter bus and the DMR conductor is grounded at the same side. The other end is terminated at a floating bus having no converter support and the DMR conductor is not grounded in this end. The converters were simulated using the model described in [98]. The frequency-dependent phase domain transmission line model available in PSCAD was used to simulate the transmission lines and the cables. Transmission system parameters are given in **Table A.3**, **Table A.4**, **Fig. A-1**, and **Fig. A-2** of the **Appendix-I**. The front end processing involved in computing the fault discrimination indices (LPF cut-off frequency, fault detection threshold, time delay, etc.) are the same as those used in **Section-3.4.1**.

3.4.2.1. Faulty Pole Identification Using Index F_{PN}

The ROCOC values computed after the low pass filtering (cut-off frequency = 500 Hz) of the currents in P-pole, N-pole and the DMR conductors measured at relay R34 were used to calculate the values of F_{PN} and F_{PR}, for a metallic P-pole-to-ground fault in the middle of Line-34. The results are shown in **Fig. 3.14**. The value of F_{PN} (i. e. 3.4), satisfies the *Criterion-A2* and confirms the involvement of P-pole in the fault. *Criterion-A3* is automatically violated when C*riterion-A2* is satisfied and that rules out the involvement of N-pole in the fault.

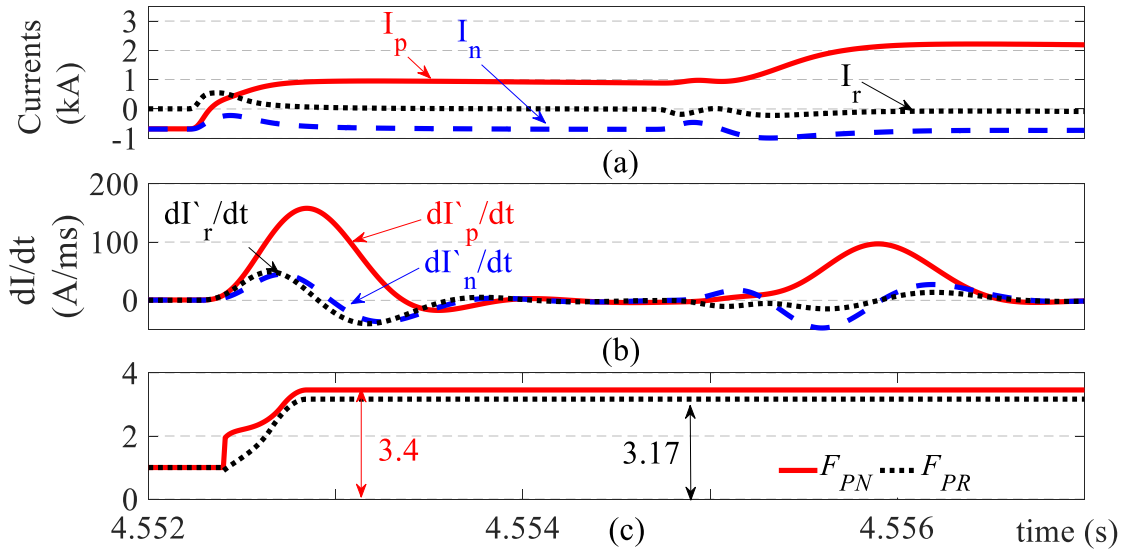


Fig. 3-14. F_{PN} and F_{PR} calculated at R34 for a P-pole-to-ground fault (a) Current measurements, I_r is the DMR current, (b) ROCOC values for bandlimited signals, (c) F_{PN} and F_{PR} (© IEEE)

The variation of ROCOC values for a metallic P-pole-DMR fault on the middle of Line-34 is shown in **Fig. 3.15**. The value of F_{PN} (i. e. 63.5) reflects a P-pole fault. Based on the observations of **Fig. 3.14** and **Fig. 3.15**, it can be concluded that regardless of the fault type, a pole-to-ground or a pole-to-DMR fault, the faulty pole can be identified with a large margin.

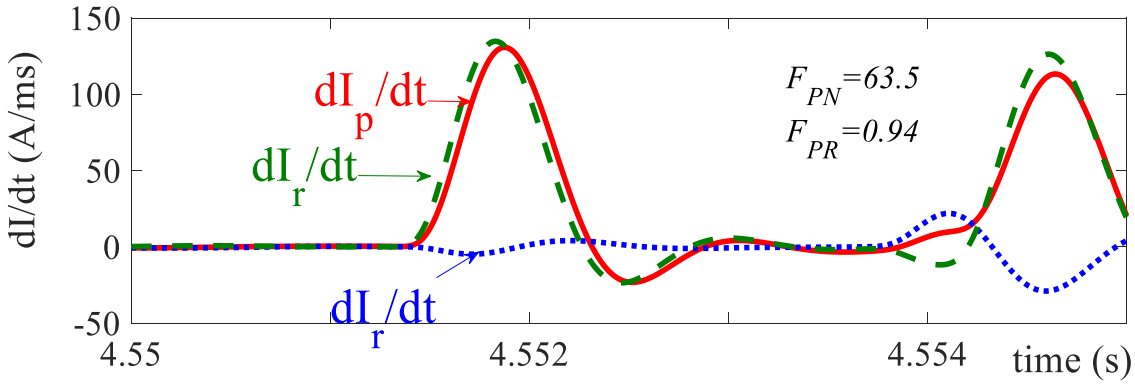


Fig. 3-15. ROCOC values and indices at R34, for a P-pole-to-DMR fault on Line 34 (© IEEE)

The variation of F_{PN} with the fault location is shown in **Fig. 3.16** for various types of faults involving the N-pole. Note that '0.01Ω N-R' indicates N-pole-to-DMR faults with fault resistance of 0.01Ω. As observed in **Fig. 3.12**, curves for P-pole faults are mirror images of the N-pole faults and therefore, omitted for clarity.

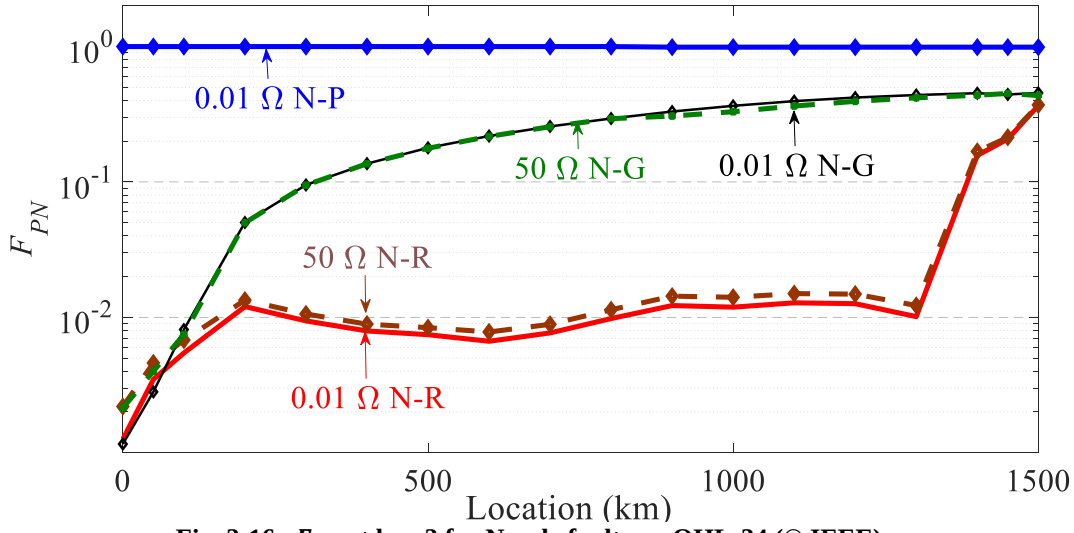


Fig. 3-16. F_{PN} at bus-3 for N-pole faults on OHL-34 (© IEEE)

The maximum value observed for F_{PN} for N-pole faults was 0.47 and the minimum value observed for F_{PN} for P-pole faults was 2.14. F_{PN} values are within 1±0.02 for P-pole-to-N-pole faults. Therefore, D_1 can be fixed to 1.5 for Line-34. This value of D_1 sets, k_1 to 0.33 and k_2 to 0.5.

3.4.2.2. Identifying Pole-to-DMR Faults Using F_{PR} or F_{RN}

The simulated responses for a P-pole-to-DMR fault and an N-pole-to-DMR fault on Line-34 are shown in **Fig. 3.15** and **Fig. 3.17(a)** respectively.

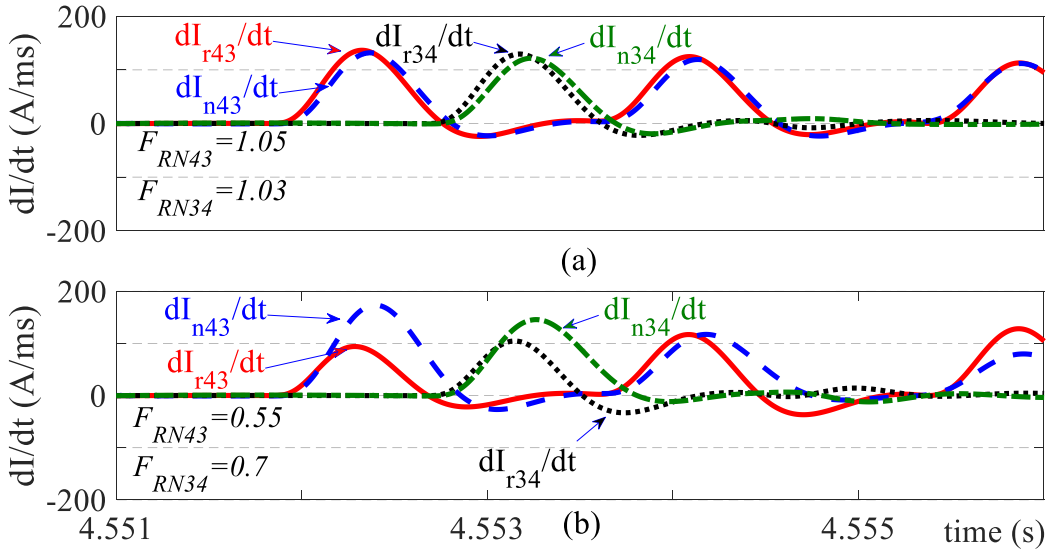


Fig. 3-17. ROCOC and F_{RN} values for N-pole faults, (a) A solid N-pole-to-DMR fault at 1000 km on Line-34, (b) A solid N-pole-to-DMR-to-ground fault at 1000 km on Line-34(© IEEE)

The faulted poles and the DMR conductors have almost equal ROCOC values in both cases. Therefore, P-pole-to-DMR fault satisfies *Criterion-B1* and N-pole-to-DMR fault fulfils *Criterion-B2*. However, as it can be seen in **Fig. 3.14(b)**, the peak ROCOC value of the faulty pole is considerably larger than the peak ROCOC values in the other two conductors during a pole-to-ground fault. Therefore, *Criterion-B1* or *Criterion-B2* is not satisfied for a pole-to-ground fault. Furthermore, F_{RN} is less than 1.0 for an N-pole-to-DMR-to-ground fault as depicted in **Fig. 3.17(b)**. The values of F_{RN} calculated at relay R34 and relay R43 for faults on Line-34 are shown in **Fig. 3.18(a)** and **Fig. 3.18(b)** respectively. In order to evaluate the dependability, metallic as well as high resistance pole-to-DMR faults are applied at regular intervals along the lines. Meantime security of the proposed scheme is evaluated by recording the responses to other fault types, N-pole-to-ground faults and N-pole-to-ground-to-DMR-faults.

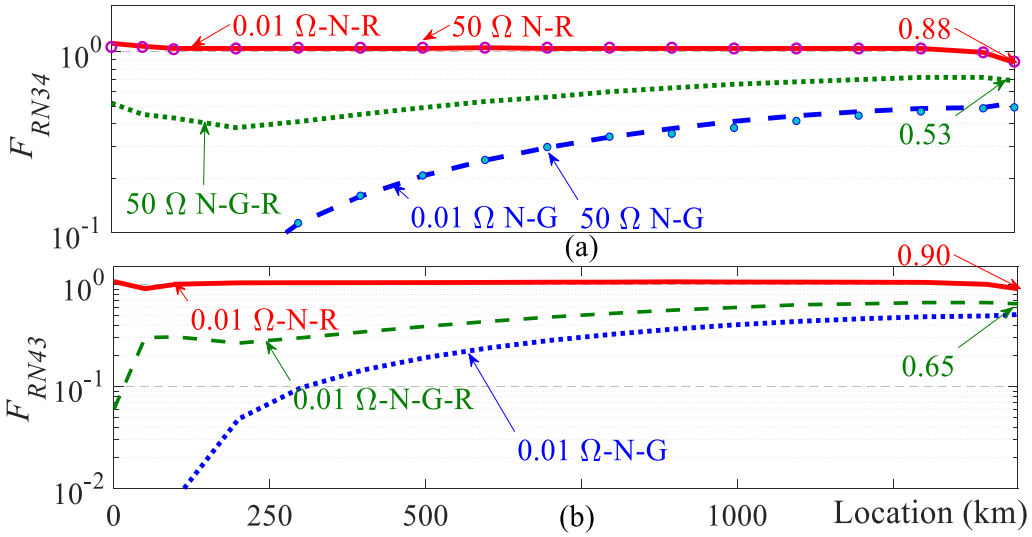


Fig. 3-18. F_{RN} for N-pole faults on overhead Line-34, computed from measurements (a) at relay R34, (b) at relay R43 (© IEEE)

The curve corresponding to N-pole-to-DMR faults is clearly separated from and stays above the curves of other types of faults, including N-pole-to-DMR-to-ground faults. Therefore, any N-pole-to-DMR fault can be identified with the help of *Criterion-B`2* after identifying the faulty pole using *Criterion-A3*. (Similarly, any P-pole-to-DMR faults can be identified with the help of

Criterion-B`1 after identifying the faulty pole using *Criterion-A2.)* **Fig. 3.18** also confirms the fact that the proposed method is applicable to grounded converter connected buses (bus-3) as well as at non-grounded buses that do not have converter support (bus-4) without any modifications. At relay R34, the observed minimum value of F_{RN} for N-pole-to-DMR faults is 0.88 and the maximum value of F_{RN} calculated for N-pole-to-ground-to-DMR faults is 0.53. The observed maximum value of F_{PR} is 1.14 for P-pole-to-DMR faults and the minimum value of F_{PR} for P-pole-to-ground-to-DMR faults is 1.48. Therefore, the threshold D_2 can be set to 1.3. This value of D_2 sets k_3 to 0.23 and k_4 *to* 0.3.

3.4.2.3. Identifying Pole-to-ground Faults Using F_{gRN} or F_{gPR}

Calculated ROCOC values for a P-pole-to-ground and an N-pole-to-ground fault on the overhead transmission line are shown in **Fig. 3.14(b)** and **Fig. 3.19(a)** respectively.

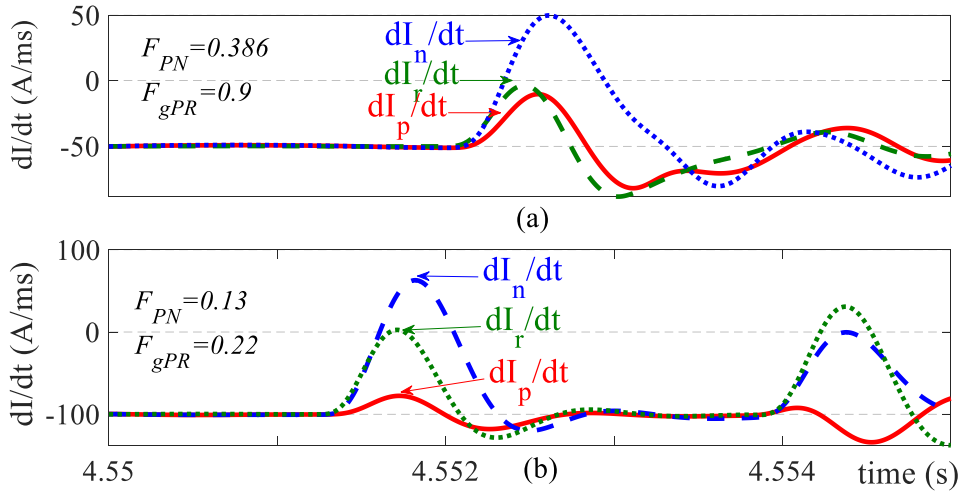


Fig. 3-19. ROCOCs at R43 for faults on Line-34, (a) An N-pole-to-ground fault at 1200 km, (b) A N-pole-to-DMR-to-ground fault at 750km (© IEEE)

Nearly equal magnitudes of peak ROCOC values of the DMR current and the healthy pole currents shown in **Fig. 3.14(b)** and **Fig. 3.19(a)** demonstrate the fulfillment of *Criteria-C1* and *–C2* for healthy conductors during a P-pole-to ground fault and an N-pole-to-ground fault

respectively. As per **Fig. 3.19(b)**, an N-pole-to-DMR-to-ground fault does not satisfy *Criterion-C2* since the estimated F_{gPR} is considerably smaller than unity. As depicted in **Fig. 3.20(a)**, the index F_{gPR} is close to 1.0 for solid and high resistance N-pole-to-ground faults (*Criterion-C`2*). $F_{gPR}$ is lower than 1.0 for N-pole-to-DMR faults and N-pole-to-DMR-to-ground faults. Fulfillment of *Ctririon-C`1* for P-pole-to-ground faults can be verified from **Fig. 3.20(b)** which shows calculated F_{gRN} for P-pole faults at relay R34. For Line-34, the minimum observed F_{gPR} for N-pole-to-ground faults and the maximum observed F_{gRN} for P-pole-to-ground faults were 0.85 and 1.28 respectively. The maximum observed of F_{gPR} for pole-to-ground-to-DMR faults was 0.45 and the minimum F_{gRN} was 1.86.

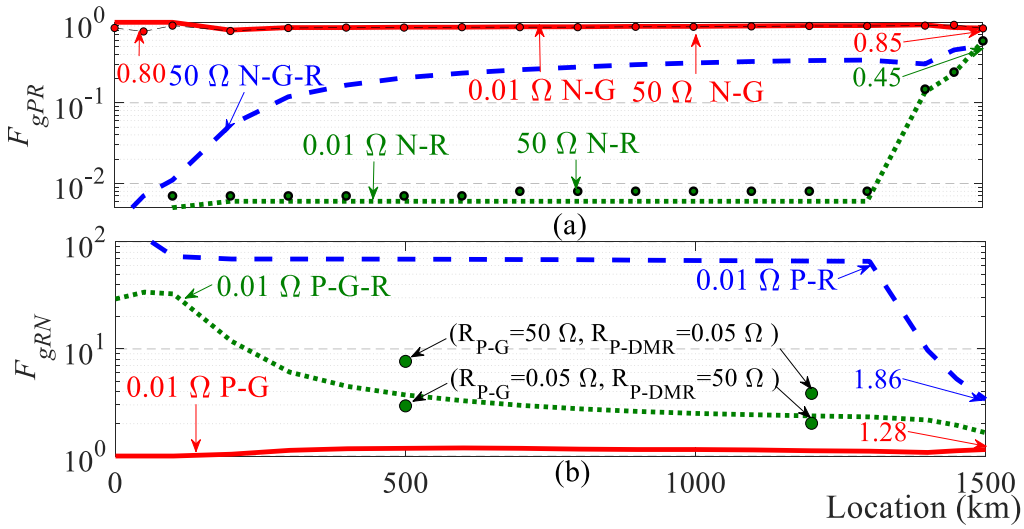


Fig. 3-20. Ground fault discrimination at R34 (a) F_{gPR} for different types of N-pole faults (b) F_{gRN} for different types of P-pole faults on Line-34(© IEEE)

Hence, D_3 can be set between 1.28 and 1.86. D_3 is proposed to set to 1.6. This value of D_3 sets k_5 to 0.375 and k_6 *to* 0.6.

3.4.3. Fault Type Identification for Cables

The proposed fault type identification method was applied to Cable-14 in the MMC-VSC based MT-HVDC shown in **Fig. 3.13**. Although pole-to-DMR faults are rare in

underground/submarine cable systems, in evaluating the applicability of the proposed method for cables, pole-to-DMR faults were also considered.

3.4.3.1. Identification of the Faulty Pole Using F_{PN}

The calculated ROCOC values for a P-pole-to-ground fault and a P-pole-to-DMR fault applied in the middle of the Cable-14 are shown in **Fig. 3.21(a)** and **Fig. 3.21(b)** respectively. It can be seen from **Fig. 3.21** and **Fig. 3.17(a)**, the peak ROCOC values for cables faults are considerably higher than the peak ROCOC values for faults on overhead lines. Furthermore, in cables, the DMR conductor ROCOC variation does not closely follow that of the healthy pole conductor as in overhead lines.

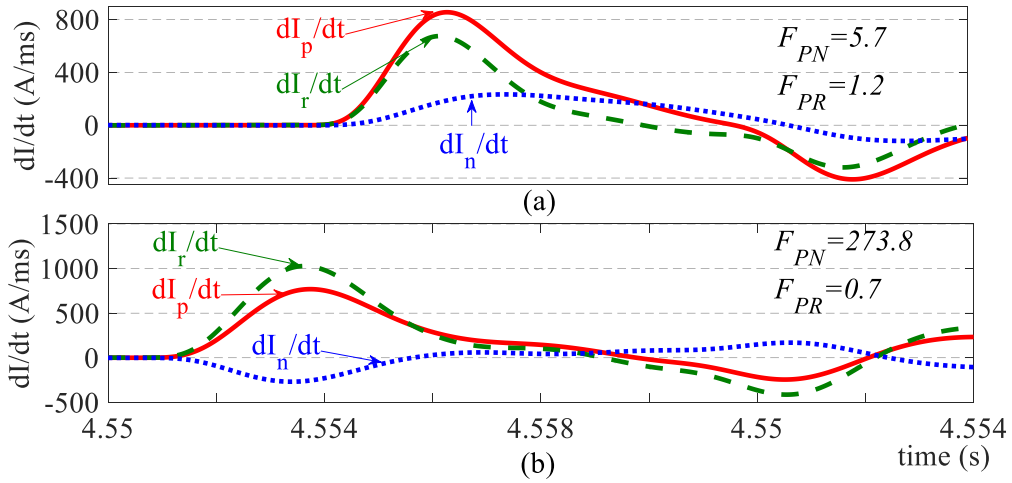


Fig. 3-21. ROCOC values and indices for faults on cable, (a) At R14, for a P-pole-to-ground fault on Cable-14, (b) At R14, for a P-pole-to-DMR fault on Cable-14 (© IEEE)

However, this does not hinder the faulty pole identification, as the values of F_{PN} are still well above 1.0. According to **Fig. 3.21**, the faulty pole can be identified using F_{PN} for any type of fault on the cable.

The variation of calculated values of F_{PN} for faults on Cable-14 is shown in **Fig. 3.22**. The maximum value of F_{PN} observed for N-pole faults was 0.47 and the minimum value for P-pole faults was 4.7. Therefore, D_1 can be fixed to 1.2 for Cable 14.

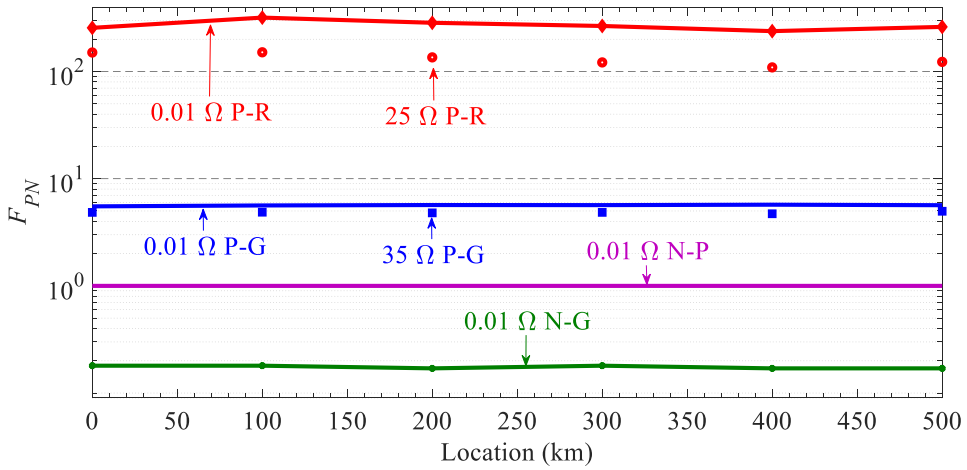


Fig. 3-22. $\boldsymbol{F_{PN}}$ at bus-1 for faults on Cable-14(© IEEE)

3.4.3.2. Discriminating Pole-to-ground Faults from Pole-to-DMR Faults with the Help of F_{PR}

As it can be seen from **Fig. 3.21(a)** and **Fig. 3.21(b)**, the calculated value of F_{PR} is smaller for P-pole-to-DMR faults when compared with P-pole-to-ground faults. Therefore, *Criterion-B`1* can be successfully used to discriminate a P-pole-to-DMR fault on a cable from a P-pole-to-ground fault. **Fig. 3.23** shows the estimated value of F_{PR} for faults on Cable-14.

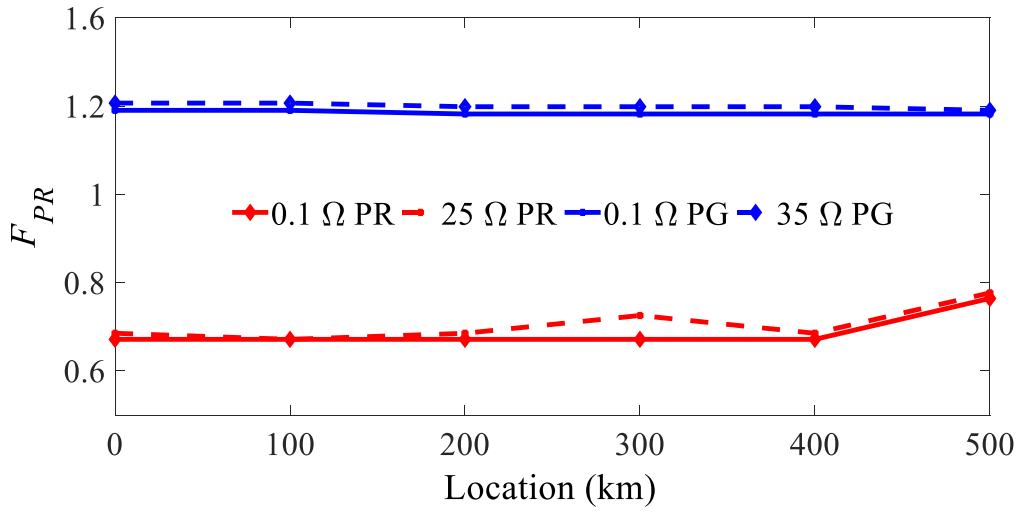


Fig. 3-23. F_{PR} for P→R and P→G faults at VSC-1 in Cable-14

Fig. 3.23 shows an almost uniform margin between the F_{PR} values computed for P-pole-to-ground faults and P-pole-to-DMR faults. There is a safety margin of 50% to discriminate against these two types of faults as the minimum value of F_{PR} for P-pole-to-ground faults and P-pole-to-DMR faults are respectively 1.2 and 0.8.

3.4.4. Fault Type Identification in Three-conductor Transmission System Terminated at LCC Stations

The presence of a large DC reactor in pole conductors of LCC-HVDC system causes a noticeably lower di/dt in the pole conductor compared to DMR conductors when subjected to similar conditions. Therefore, when compared with indices calculated for VSC systems, it was observed that the respective indices for LCC systems tend to deviate from their ideal values, sometimes violating the criteria *B1, B2, C1,* and *C2*. However, still the faults can be discriminated with the help of modified Criteria-*B`1, B`2, C`1,* and *C`2*. To demonstrate the capability of applying the method in systems with highly asymmetric conductor terminations, the method was applied for discriminating pole-to-ground faults from pole-to-DMR faults in an LCC HVDC system with a DMR. This test system is created by replacing the two-conductor transmission line described in **Section-3.4.1.1** with a three-conductor overhead transmission line and by only grounding the DMR at the rectifier end. Although inductors may be installed on the DMR, in order to simulate the worst case for fault type discrimination, a system without terminal inductors on DMR conductor was considered. Calculated indices F_{RN} and F_{gPR} for N-pole-to-ground faults and N-pole-to-DMR faults at the rectifier side are shown in **Fig. 3.24**. As seen in **Fig. 3.24(a)**, due to large asymmetry in the terminations, calculated F_{RN} is slightly higher than unity for N-pole-to-

DMR faults. On the other hand, as depicted in **Fig. 3.24(b)**, F_{gPR} is slightly less than unity for N-pole-to-ground faults, although the expected value is 1.

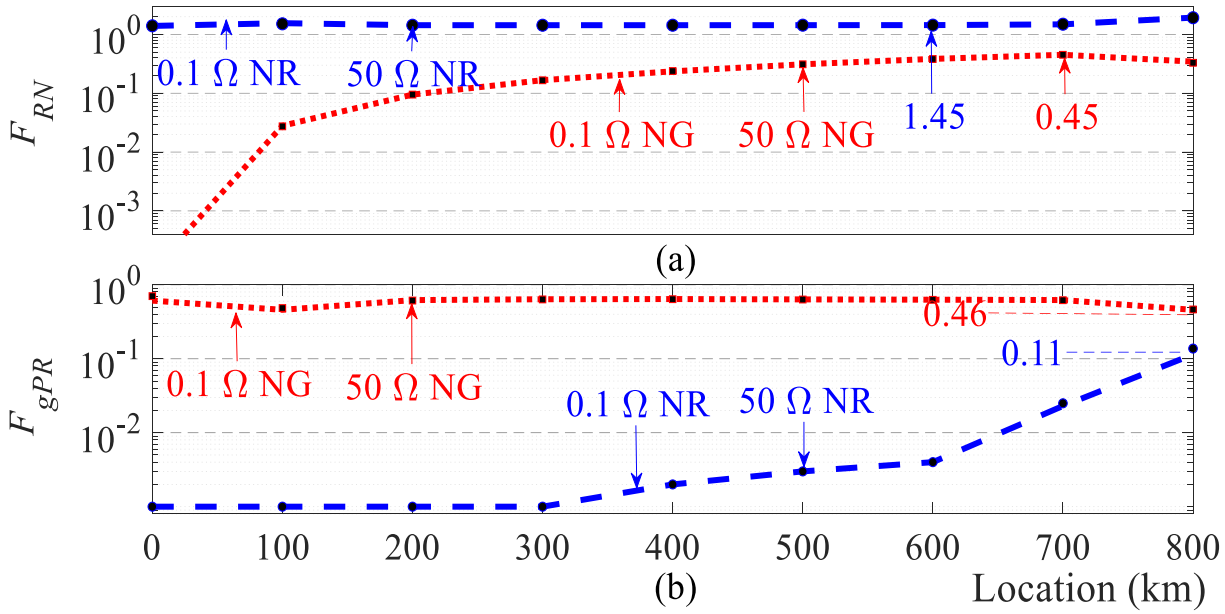


Fig. 3-24. Discriminating N-pole-to-DMR faults from N-pole-ground faults in an LCC-HVDC system with DMR (a) F_{RN} for N-pole-to-ground faults and N-pole-to-DMR faults, (b) F_{gPR} for N-pole-to-ground faults and N-pole-to-DMR faults (© IEEE)

However, N-pole-to-DMR faults can be discriminated from N-pole-to-ground faults using the *Criterion-B`2* since there is a sufficient margin between the values of $F_{RN}$ calculated for these two types of faults. Similarly, any N-pole-to-ground fault can be distinguished from a fault where the DMR is involved with the help of the calculated value of $F_{gPR}$ and *Criterion-C`2*. Therefore, it can be concluded that despite the high degree of the asymmetry in termination, the algorithm shown in **Fig. 3.7** is still capable of correctly identifying the faulted conductors.

3.4.5. Fault Type Identification in HVDC Transmission System with Non-homogeneous Lines

In this section, a hybrid three-terminal HVDC transmission system with a non-homogeneous network is considered since the fault type identification is challenging in non-homogeneous systems. The configuration of the test system is shown in **Fig. 3.25**, and features are

1. Two offshore MMC-VSC rectifier stations
2. Onshore LCC inverter station
3. Two-conductor submarine cable system
4. Three-conductor overhead transmission line
5. DMR earth electrode located at the shoreline

This type of HVDC transmission system could be used to exploit the advantages of individual converter technologies in connecting multiple offshore wind sites to an onshore HVAC grid. Furthermore, the bipole HVDC transmission is favored over the monopole as it is possible to transfer a half of the rated power during a single-pole fault and such a redundancy is important [40]. Since the prolong ground currents are often not allowed in onshore applications, a dedicated metallic return wire is required to utilize the above redundancy [40]. However, great savings can be made by using two-conductor submarine cables when earth currents through offshore water bodies is not a major issue. Prompt identification of fault type in the transmission structure shown in **Fig. 3.25** is a novel class of challenging problem due to the presence of both overhead transmission lines and submarine cables, two-conductor and three-conductor configurations, and LCC and VSC stations within the same transmission system. The possibility of applying the proposed fault discrimination method in such a complex hybrid configuration is investigated in this section. The three-terminal hybrid HVDC transmission system was simulated in PSCAD using

detailed EMT models. The parameters of the LCC inverter and the VSC rectifier are given in **Table 3.2** and **Table 3.3** respectively.

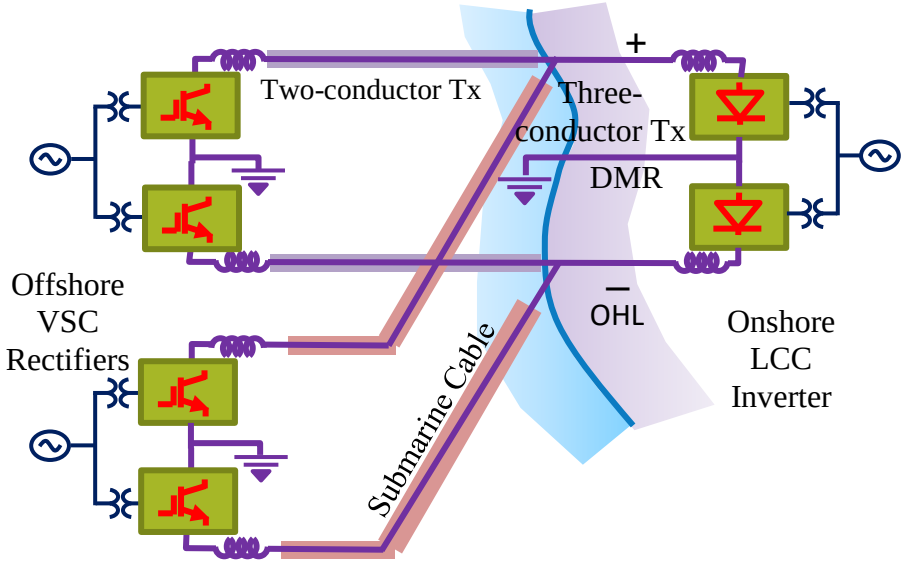


Fig. 3-25. Hybrid VSC-LCC bipole HVDC interconnection between offshore windfarms and mainland AC grid (© IET)

Each inverter pole is assumed to be made of a twelve pulse LCC which is operated in constant extinction angle control mode. Each cable was assumed to be 200 km long and the overhead transmission line was assumed to be 500 km long. In calculating indices, 1 ms fixed time window of current measurements that are taken through a third order low pass filter having 1 kHz cut-off frequency was considered

Table 3-2 LCC inverter parameters (© IET)

Parameter	Value	Units
Nominal DC Voltage	±500	kV
Operating point	700	MW/pole
DC reactor	0.75	H
Cut-off frequencies of DC side shunt filer	720 & 1440	Hz
Transformer Data		
Leakage Reactance	0.15	Pu
Transformer Ratio	230kV/209kV	

Table 3-3 VSC rectifier parameters (© IET)

Parameter	Value	Units
Nominal DC Voltage	±500	kV
Nominal DC Power	300	MW/pole
Nominal AC Voltage (VLL)	230	kV
Equivalent DC Capacitance	100	μF
Number of levels	98	
Arm reactor	25	mH
di/dt limiting reactor	40	mH
Terminal reactor on DMR	2.5	mH

.

3.4.5.1. Faulty Pole Identification at Each Converter Station

The index F_{PN} was calculated for different types of faults applied at every 50 km along the line using the currents measured in P-pole and N-pole conductors at the LCC inverter terminals, and the results are shown in **Fig. 3.26**.

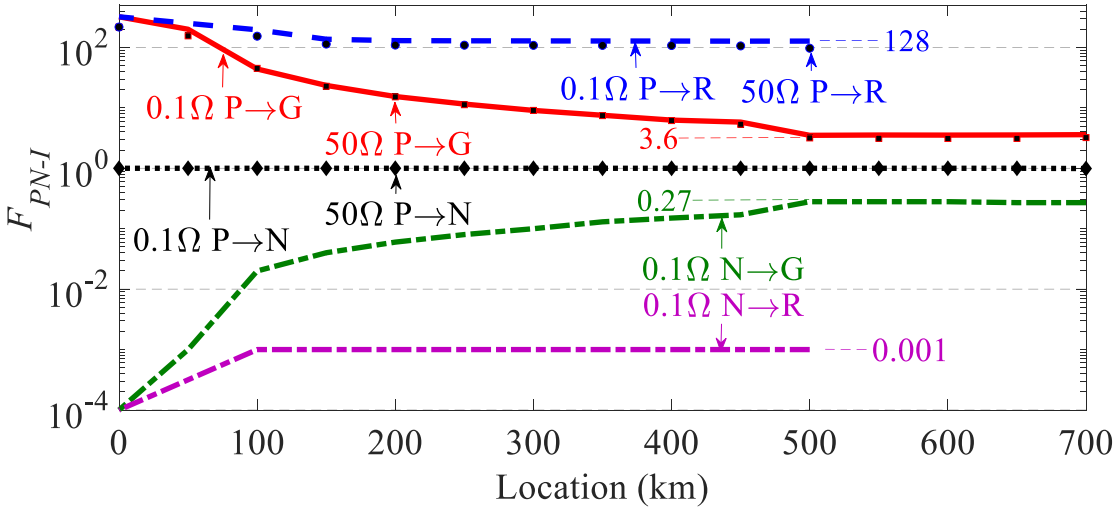


Fig. 3-26. Calculated faulty pole identification index at the LCC inverter (© IET)

The distance to the fault shown in figures is measured from the respective converter terminal (in this case from the inverter). As evident from **Fig. 3.26**, *Criterion-A1* is satisfied for P-pole-to-N-pole faults; *Criterion-A2* is held for any fault that involves P-pole except for P-pole-to-N-pole faults, and *Criterion A3* is satisfied for any fault involving the N-pole except for P-pole-to-N-pole faults. As depicted in **Fig. 3.26**, calculated F_{PN} for a given fault type for given fault location does not considerably change with the fault resistance (e. g.: curves 0.1Ω P→G and 50Ω P→G are coincident). Note that the minimum value of the F_{PN} evaluated at the inverter for a P-pole fault is 3.6 and the maximum value of F_{PN} for N-pole faults is about 0.27. Therefore, it can be concluded that pole(s) involved in a fault can be identified at the onshore LLC based inverter with the help of faulty pole identification index, F_{PN}, with a considerable safe margin regardless of the fault resistance and the fault location. **Fig. 3.27** shows the calculated values for F_{PN} using the local current measurements at one of the offshore VSC based rectifier stations shown in **Fig. 3.25**.

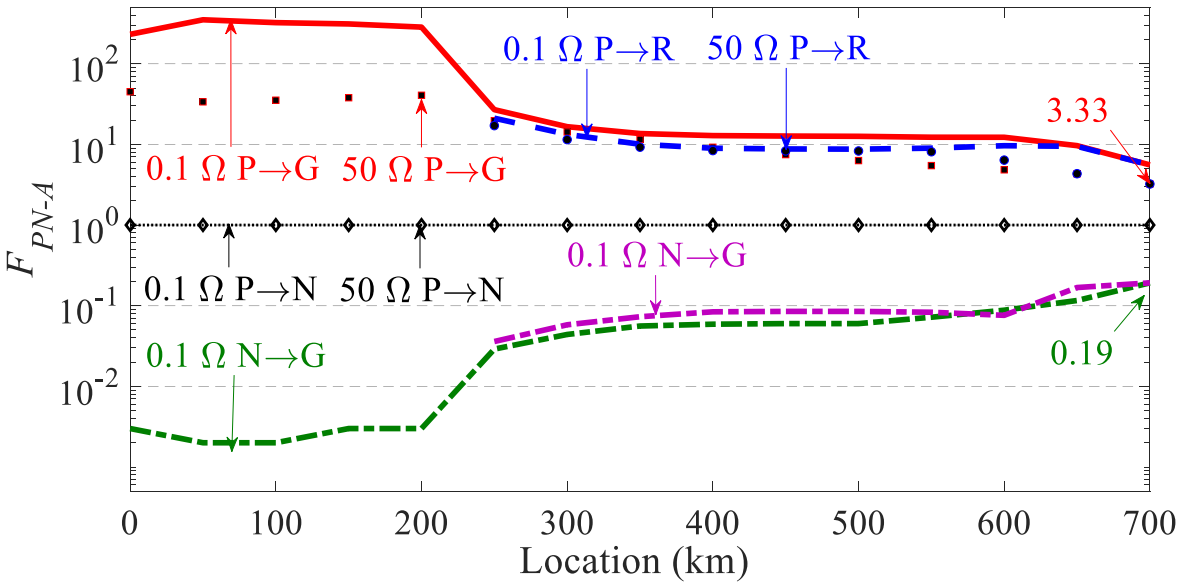


Fig. 3-27. Calculated faulty pole identification index using the local current measurements at rectifier-A (© IET)

As per **Fig. 3.27**, conclusions made using the calculated values F_{PN} (*Criteria A1-A3*) holds. However, when compared with the calculated values of F_{PN} at the inverter terminal, a noticeable change with the fault resistance is apparent for the faults occurring on the cable.

3.4.5.2. Discriminating Pole-to-DMR Faults from Pole-to-ground Faults at the Inverter

Fig. 3.28 shows the calculated F_{PR} for P-pole-to-ground faults and P-pole-to-DMR faults at the onshore LCC inverter. The F_{PR} is somewhat less than the unity for P-pole-to-DMR faults as the large DC reactor in the LCC inverter causes somewhat smaller ROCOC values at the pole conductors when compared with ROCOC values of DMR current. However, F_{PR} remains more or less constantly around 0.7 for P-pole-to-DMR faults while the calculated values of F_{PR} decrease to a minimum of 2 with the distance for P-pole-to-ground faults. As depicted in **Fig. 3.28**, due to distinct range of values and considerable margin, a P-pole-DMR fault can be discriminated from P-pole-to-ground faults and P-pole-to-DMR-to-ground faults with the help of index F_{PR}.

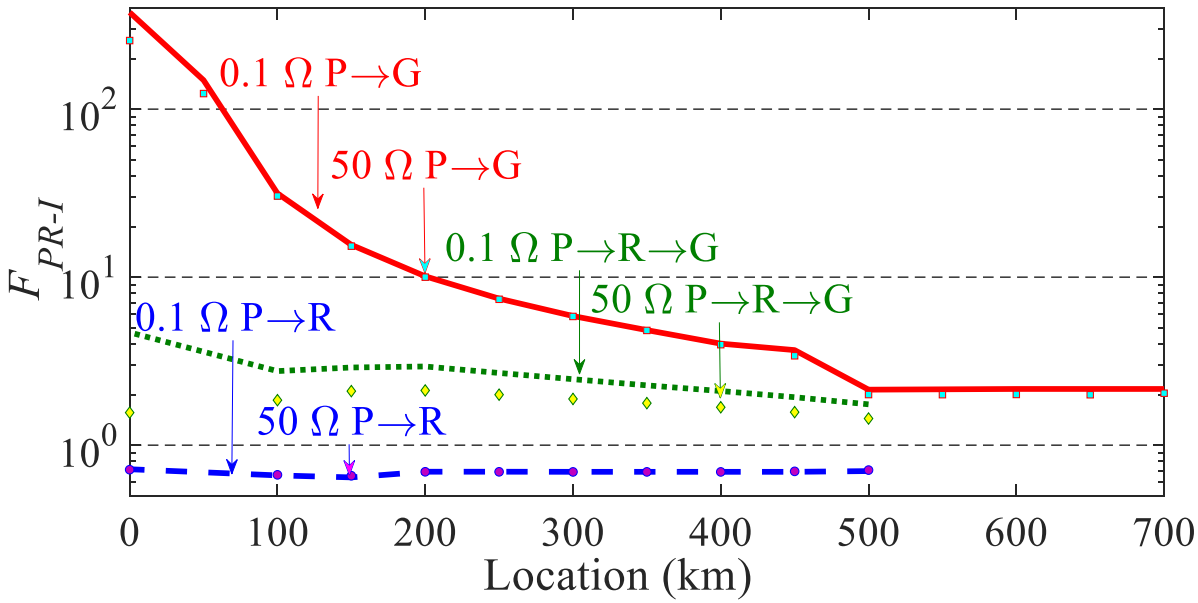


Fig. 3-28. Calculated F_{PR} at the offshore LCC inverter (© IET)

Similar to **Fig. 3.28**, a distinct range of values of F_{RN} are observed for N-pole-to-DMR faults and N-pole-to-ground faults.

The calculated F_{gPR} for N-pole-to-ground faults, N-pole-to-DMR faults, and N-pole-to-DMR-to-ground faults are shown in **Fig. 3.29**.

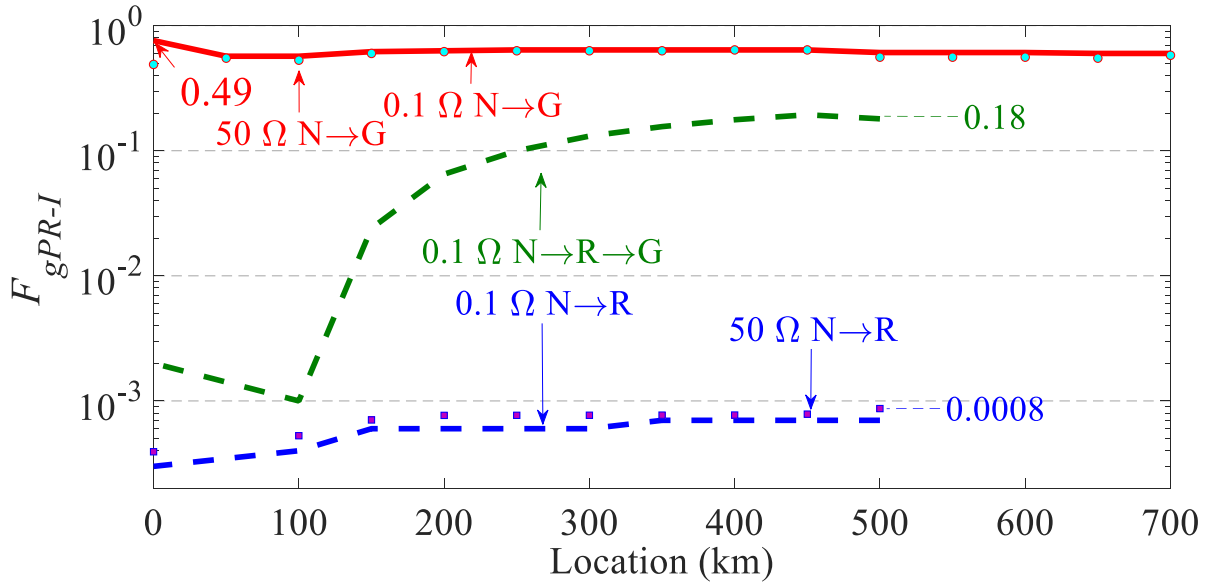


Fig. 3-29. Calculated F_{gPR} at the offshore LCC inverter (© IET)

The index is closer to unity for N-pole-to-ground faults, and its value is much smaller than unity for the other two types of faults. Therefore, it can be concluded that a pole-to-DMR fault can be identified with the help of the local current measurements at the LCC inverter. Therefore, a P-pole-to-ground fault can be identified with the help of near unity test for F_{gPR} (F_{gRN} in case of N-pole-to-ground faults). If near unity test fails, DMR is also involved in the fault. For a permanent fault, this a crucial piece of information for the repair crew to prepare for the type of repair task to be performed. Furthermore, the calculated values of indices reflect whether the fault is in the overhead transmission line segment or in the submarine cable segment.

3.5. Possible Use of Index F_{PN} for Pole-to-Ground Fault Location

It is obvious from the results presented for various test systems, the index F_{PN} is independent of the fault resistance and only dependent on fault location. As it can be seen in **Fig. 3.12** and **Fig. 3.16**, the index F_{PN} is a smooth and continuous single-valued function of fault distance for pole-to-ground faults in overhead transmission lines. Therefore, the index can be used as an indicator of the location of pole-to-ground faults. However, it is necessary to pre-establish the nonlinear relationship between F_{PN} and the distance to fault through simulations or test measurements, to use as a calibration curve. This possibility was investigated with the two-conductor LCC based test system described in **Section 3.5.1.**

3.5.1. F_{PN} as Function of Fault Location

Fig. 3.30 shows the F_{PN}^{-} values calculated for a few metallic pole-to-ground faults applied in regular intervals along the line. The figure also shows the F_{PN} for a few faults having different fault resistances, applied at random locations. As depicted in **Fig. 3.30**, despite the fault resistance value, the estimated F_{PN}^{-} for selected fault scenarios coincides with the F_{PN}^{-} estimated with metallic faults. Therefore, as F_{PN}^{-} and its reciprocal, F_{PN}^{-1} can be practically considered as independent from the fault resistance. Thus the pre-calculated F_{PN}^{-1}, estimated with metallic faults, can be used to estimate the distance to high resistance faults. In order to minimize the error due to numerical underflow, F_{PN}^{-} and F_{PN}^{-1} are respectively used for P-pole-to-ground and N-pole-to-ground fault locations. The method is straightforward and convenient: once the fault type is identified to be a

P-pole-to-ground or an N-pole-to-ground type, the location of the fault corresponding to the computed F_{PN}^{-} can be directly read from the pre-calculated F_{PN}^{-1} using the metallic faults.

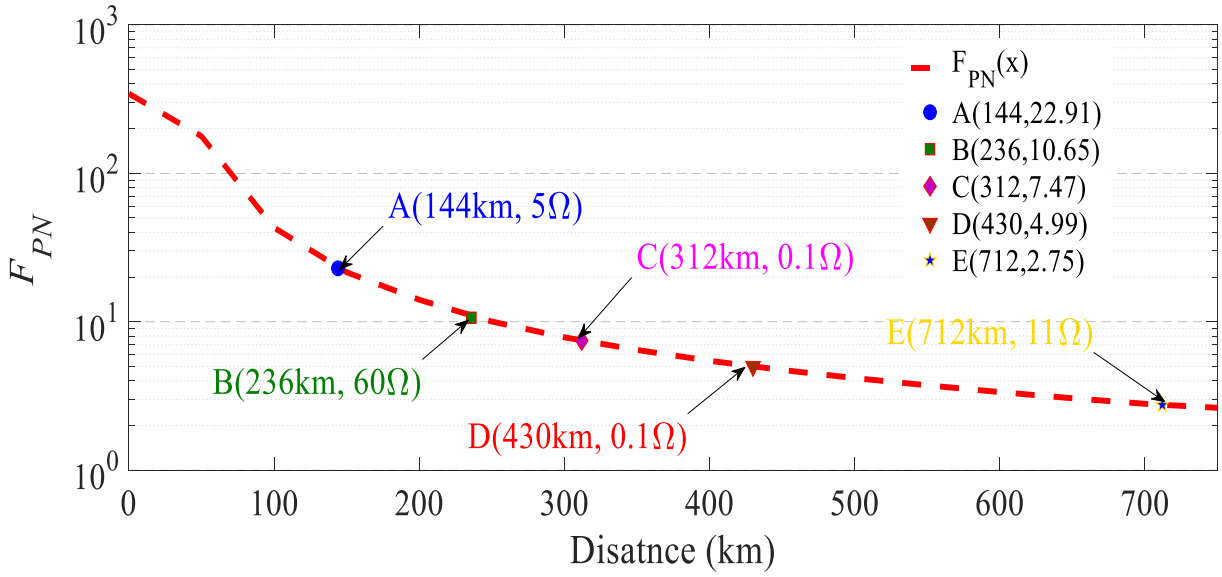


Fig. 3-30. F_{PN} estimated with metallic faults and estimated F_{PN} for random fault scenarios (© IET)

3.5.2. Single-pole-to-ground Fault Location in Two-conductor LCC-HVDC Link

The calculated $F_{PN}^{-}(x)$ and $F_{PN}^{-1}(x)$ at the rectifier end of the two-conductor bipole test system are shown in **Table 3.4**. Calculated fault locations for P-pole-to-ground faults and N-pole-to-ground faults applied to some randomly selected locations are shown in **Table 3.5** and **Table 3.6** respectively. With the help of $F_{PN}^{-}(x)$ or $F_{PN}^{-1}(x)$ calculated for the given fault, Matlab interpolation function using the cubic interpolation option is used to locate the fault. For each of the fault scenario described in the first two columns of **Table 3.5** and **Table 3.6**, the calculated $F_{PN}^{-}(x)$ or $F_{PN}^{-1}(x)$ using the transient current measurements are shown in the third column. As the rate of change of $F_{PN}^{-}(x)$ or $F_{PN}^{-1}(x)$ with the distance is smaller for far away faults when compared with close-up faults, four decimal points precision was used to maintain the accuracy.

Table 3-4 Estimated $F_{PN}^{-}(x)$ and $F_{PN}^{-1}(x)$ for the test system(© IET)

Loc. (km)	$F_{PN}^{-}(x)$	$F_{PN}^{-1}(x)$	Loc. (km)	$F_{PN}^{-}(x)$	$F_{PN}^{-1}(x)$
0	344.0690	2422.689	450	4.732842	4.878133
50	177.6568	474.9237	500	4.172521	4.288561
100	43.04042	54.9398	550	3.730998	3.825307
150	21.55040	24.33007	600	3.357883	3.441351
200	14.07274	15.15696	650	3.051066	3.125217
250	10.03818	10.66607	700	2.799645	2.869266
300	7.856659	8.258868	750	2.630967	2.681031
350	6.457271	6.702997	800	1.85992	1.890377
400	5.457357	5.649014	-		

The fourth and fifth columns of **Table 3.5** and **Table 3.6** indicate the estimated distance to the fault and the error in kilometers.

The percentage error is calculated using (3.8) [123].

$$Error\ (\%) = \frac{Esti.\,Fault\ Loc. - Act.\,Fault\ Loc.}{Transmission\ Line\ Length} \times 100 \tag{3.8}$$

Table 3-5 Fault locations for low resistance P-pole-to-ground faults (© IET)

Act. Loc. (km)	R_F (Ω)	$F_{PN}^{-}(x)$	Est. Loc. (km)	Error (km)	Error (%)
48	0.3	194.1777	44.536	3.46	0.43
144	5.0	22.74165	145.003	-1.00	-0.12
192	1.5	14.82150	193.420	-1.42	-0.18
390	4.0	5.6301	390.164	-0.16	-0.02
654	0.8	3.02038	653.602	0.40	0.05
760	0.3	2.56451	758.284	1.72	0.21

Table 3-6 Fault locations for high resistance faults (© IET)

Pole	Loc. (km)	R_F (Ω)	Est Loc (km)	Error (km)	Error (%)
P	118	9.0	118.9965	-0.9865	-0.1233
N	162	12.0	162.3993	-0.3993	-0.0499
P	294	7.0	294.4515	-0.4515	-0.0564
N	420	50.0	419.7603	0.2397	0.0300
P	480	9.0	480.3729	-0.3729	-0.0466
P	712	7.0	714.5440	-2.5440	-0.3180
N	762	8.0	760.6705	1.3295	0.1662

An average error of about 0.12 % or 0.95 km is observed for the considered fault location scenarios. Therefore, it is possible to locate low resistance faults at an accuracy of about 99.88%. Therefore, if three tower spans are assumed to be spread along 1 km, the fault could be expected within three spans of the located span. The error is higher for faults near the converters when compared to the faults away from the converters. The estimated error for faults having a resistance between 5 Ω-70 Ω, is about 1.22 km or 0.15 %, is slightly higher than the observed error for low resistance faults.

3.6. Concluding Remarks

The fault types in HVDC transmission systems can be identified by comparing the maximum rates of change of bandlimited current measurements in a pair of conductors at a time. Therefore, for different conductor pairs, five indices are defined to compare the observed maximum ROCOC values of current through each pair of conductors for a short time window of current measurements. The proposed indices were shown to be dependent on the fault type and location, but independent of the fault resistance. Although three possible fault types in two-conductor systems can be

distinguished with one index, all five indices are necessary to distinguish all possible fault types in three-conductor systems. A systematic procedure with a set of criteria is developed for fault type identification.

With the help of detailed PSCAD models, the method is validated for two-conductor and three-conductor transmission configurations terminated with LCC stations as well as for VSC stations. The test systems used for verification comprised of overhead transmission lines as well as underground cables. The method is capable of determining the fault type promptly and reliably only with the help of locally measured currents. Therefore, the method can be utilized in existing and future VSC based HVDC transmission systems that comprises of overhead lines and/or cables. Furthermore, the method is successfully validated for a mix HVDC transmission system comprising of both LCC and VSC stations, and a transmission system having a two-conductor cable portion and a three-conductor overhead line portion. The method can be applied in both point-to-point HVDC systems and MT-HVDC transmission system. The fault type information provided by the method can be used for supervising protection function as well as control functions related to fault recovery. Furthermore, maintenance crews can be informed whether a DMR conductor is involved in a fault, which can be critical for safety. The method can be easily implemented at low cost since (i) the threshold settings can be easily set as indices are almost independent of fault resistance; and (ii) uses only locally measured low-frequency current measurements. Furthermore, the ability to locate pole-to-ground faults in overhead transmission lines with the help of F_{PN} was also demonstrated.

Chapter 4

Fault Recovery in Hybrid LCC-VSC HVDC Multi-Terminal Transmission Systems

4.1 Introduction

Force retardation is used in LCC-HVDC links to control the DC fault currents and clear temporary faults without needing DC circuit breakers. As the DC breaker technology is still matuaring and expensive, hybrid LCC-VSC HVDC schemes can provide an alternative arrangement for overcoming the issues associated with DC faults in VSC based MT-HVDC systems. Another major barrier that hinder the building of MT-HVDC transmission systems is the reluctance to make huge investments in an unproven technology. Building hybrid LCC-VSC MT-HVDC systems could be a safer intermediate stage in mowing towards entirely VSC based MT-HVDC grids having full benefits redundency. A huge portion of initial investment can be cut-down if an MT-HVDC transmission can be developed around an existing LCC HVDC link with spare transmission capacity. Furthermore, terminals can be added step by step after the technical feasibility of the initial VSC terminals is verified. Feasibility of parallel taping of an LCC-HVDC link has been investigated in the industry. Two practical examples are consideration of tapping a LCC-HVDC link to connect a geothermal site in Queensland (QLD) [124] and tapping of

Manitoba Hydro Bipole-III link. However, handling of DC faults in hybrid LCC-VSC MT-HVDC transmission system has not been properly examined and documented. Hence, fault clearing in hybrid LCC-VSC MT-HVDC transmission system is a timely research topic.

In this chapter, the clearing of DC faults in a hybrid multi-terminal HVDC transmission system consisting of LCCs and VSCs implemented using half-bridge MMC technology is investigated. While the hybrid HVDC system has several possible configurations, the particular configurations considered in this thesis are 1) a half-bridge MMC-HVDC link sharing a section of the transmission line of an LCC-HVDC link and 2) an LCC-HVDC link tapped by half-bridge MMC inverters. A DC fault recovery strategy that employs (i) a high rating series diode valve placed at each VSC inverter pole to block fault currents, (ii) ACCBs to isolate the faulty VSC rectifier pole, and (iii) force retardation at LCC rectifier to extinguish the arc, is proposed. The fault recovery performance of the proposed strategy is demonstrated through simulations. The work presented in this chapter is based on the following publications.

[E] M. H. Naushath, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "Energization and regulation of a hybrid HVDC grid with LCC and VSC," In Proc. IEEE Electrical Power and Energy Conference (EPEC), Saskatoon, Canada, Oct. 2017.

[F] M. H. Naushath, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "Investigation of Fault Ride-Through Capability of Hybrid VSC-LCC Multi-Terminal HVDC Transmission Systems," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 241-250, Feb. 2019.

4.2 Background and Literature Review

Despite the need for additional equipment such as harmonic filters and reactive power support, the well-proven LCC technology is still relatively economical when building high capacity converters [92]. Thus, even after the emergence of commercial VSC technology, most of the two-terminal HVDC transmissions systems are built using LCC technology. All over the world,

there are many long, high capacity, point-to-point LCC-HVDC links connecting large generating stations and load centers. Often, they are built with some spare capacity in the transmission line for future expansion or to meet other design requirements. The spare capacity of these transmission lines can be utilized to integrate potential renewable energy resources and supply energy for the small cities or load centers which are located close to the path of these HVDC lines. Cost can be considerably reduced, if it is possible to tap into the HVDC line [124-126] to supply those load centers. When compared to the potential options such as using DC-DC converters [127-128] or using series tapping with current source converters [129], currently it is more practical and economical to use VSCs to tap into an LCC HVDC line. This is because the VSC technology is relatively mature and commercially available. An example of such a hybrid LCC-VSC multi-terminal HVDC system is shown in **Fig. 4.1**. The rating of the LCC stations of such a multi-terminal transmission system could be much greater than those of the VSC stations. The high capacity main transmission line connecting the LCC stations, which will be referred to as the mainline hereafter, is typically very long and could be well over 1000 km.

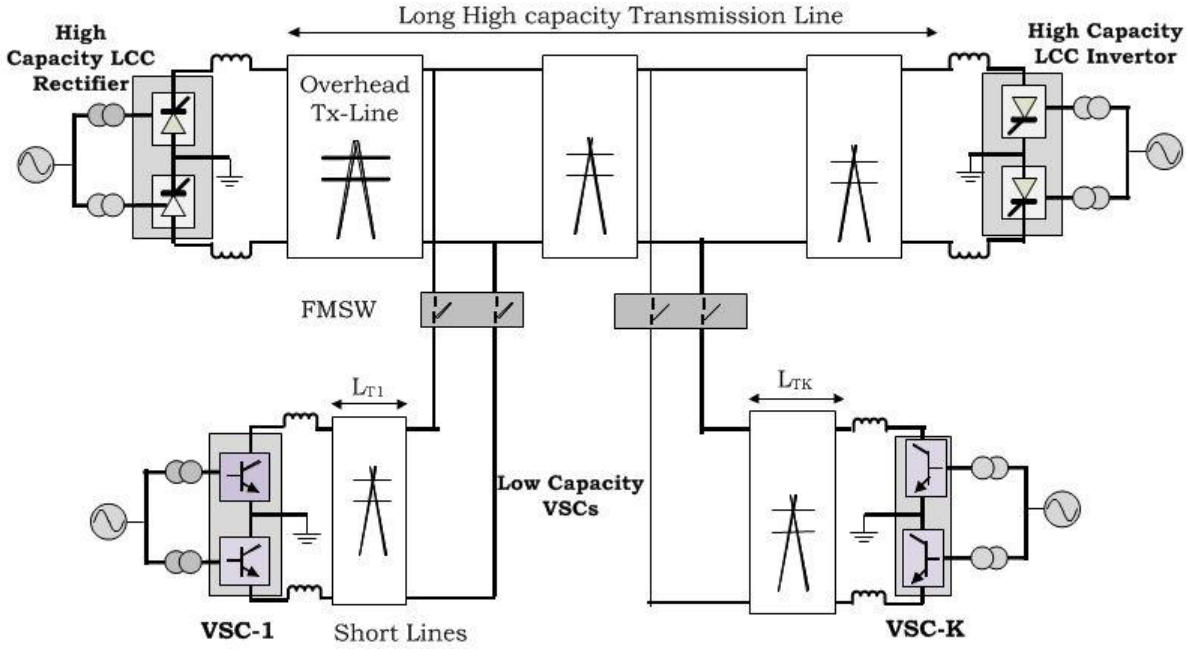


Fig. 4-1. Bipole hybrid LCC-VSC MT-HVDC transmission system (© IEEE)

The sharing of an existing high capacity mainline to transfer power among VSC stations is feasible only when the VSC stations are not far away from the mainline. Therefore, the transmission lines that connect the VSCs to tapping points, which will be referred to as VSC branches hereafter, are assumed not to be longer than a few hundreds of kilometres.

There are many possible hybrid MT-HVDC configurations: (i) all VSCs operating as inverters can tap into an LCC link which forms the backbone of the multi-terminal system; (ii) all VSCs operating as rectifiers can feed power into an LCC link; or (iii) some VSCs operating as rectifiers can feed power into an LCC link while the others operating as inverters draw power from the LCC link. The third configuration, being the most generic, is investigated in this chapter.

One major design challenge encountered when tapping into an LCC-HVDC link using the more viable half-bridge MMC technology is the response of VSCs to DC side faults. A DC side fault appears as a three-phase short circuit to the AC systems connected through VSCs [42]. The energy stored in the capacitors of the VSC is rapidly discharged into the fault giving rise to extremely high initial fault currents. A simple but elegant solution to block the fault currents when a VSC is operating only as an inverter is proposed in [80, 131]. The fault current from a VSC inverter can be blocked by placing a series protective diode at each pole of the station [80, 131]. The reliability, robustness, and longevity of DCCBs suitable for HVDC applications is neither fully proven in the field nor they are commercially available from a range of manufacturers. Therefore, DC fault currents interruption from a VSC rectifier is typically achieved by de-energizing the VSC rectifier by opening its ACCB as proposed in [132]. A fast mechanical switch (FMSW) is used to connect/disconnect tapping lines at the tapping point. However, FMSW can be opened only when the current through it is very small as 50 A-100 A. Although the resulting interruptions are longer, this approach can be foreseen as the most economically viable option for

some time into the future. A control procedure for clearing DC faults in an LCC-VSC hybrid MT-HVDC scheme without using DCCBs, and restoring the HVDC system with minimum disruption to the backbone LCC link is developed in this chapter. The feasibility of the proposed control procedures, implemented through a high-level centralized master controller, was verified using detailed electromagnetic transient (EMT) simulations carried out in PSCAD/EMTDC.

4.3 Coordinated Control of Hybrid LCC-VSC Multi-Terminal HVDC Systems

The DC side fault behavior and recovery process depend on the converter controls, including operating modes, converter station coordination method, and controller settings. In this section, a co-ordination controller is developed for a hybrid LCC-VSC multi-terminal HVDC transmission system shown in **Fig 4.1**. Control sequences required for the energization and regulation of the MT-HVDC transmission are developed and added to the co-ordination controller. The fault recovery strategy should be implemented by considering the interface of the station controls and other fault recovery sub-functions at the converter level. The following sections describe the considered converter controls, co-ordination controller, and the proposed MT-HVDC transmission system energization procedure.

4.3.1 Controlling Converter Stations and Control Interfaces

When d-q domain decoupled controllers are used, VSC stations can be operated in either constant DC voltage control (V-control) mode or constant power control (P-control) mode. Hence, the controller interface of VSC stations should have necessary control inputs to switch between

the appropriate DC side control modes. During the energization and fault recovery periods when the VSC stations are not connected to the LCC-HVDC link, the VSC stations are operated in V-control mode with a pre-defined reference voltage. However, when the reference voltage is continuously changed, the control mode is referred to as the voltage tracking mode. Since ratings of the VSC converter stations are considerably less than LCC stations, they are not assigned to control the DC voltage when connected to the LCC-HVDC link. Whenever a VSC is connected to the LCC-HVDC link, it is operated under the constant power control mode. To protect from possible damages due to larger currents, all VSC stations are assumed to be equipped with an external input to block IGBTs. Therefore, the VSC control interface shown in **Fig. 4.2** was considered in this study. An LCC inverter station is typically connected to a strong AC system and operated under constant extinction angle control mode to regulate the DC voltage. The LCC rectifier is operated under current control mode. Since the current cannot flow in the reverse direction through thyristors, only the LCC rectifier feeds a DC side fault. Therefore, only the LCC rectifier influences the DC fault current behavior and involves in the fault recovery.

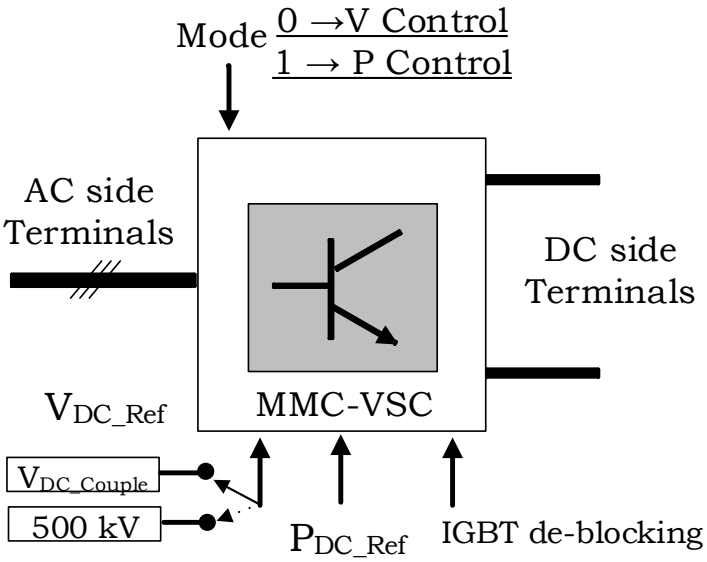


Fig. 4-2. The control interface of the VSC (© IEEE)

In the fault clearing process, force retardation is applied at the LCC rectifier and the thyristors in LCC inverter are blocked. The control interface shown in **Fig. 4.3** is assumed for an LCC rectifier station.

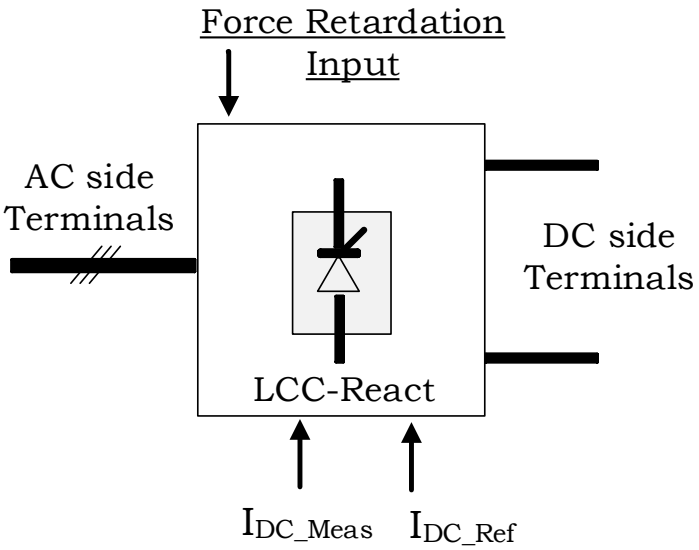


Fig. 4-3. Control interface for an LCC station operating under current control mode

When the fault signal is set, it is assumed that the firing angle is increased linearly at a pre-defined rate to decrease the voltage across the fault. When the fault input is reset after a force retardation period, the firing angle is assumed to decrease at a rate lower than the rate of increasing the firing angle during the force retardation. An LCC inverter interface is assumed to be similar, but instead of the DC current measurement and the reference, it takes in the measured DC voltage and its reference. When the logical input "Fault" is true, an inverter blocks the thyristors.

4.3.2 Co-ordination Controller

Coordination of the converter stations connected to a MT-HVDC transmission system is important for stable normal operation and for the fault recovery process. A centralized controller hereafter referred to as master power controller (MPC), was developed for this purpose. In the normal steady-state operation, the MPC calculates the current order for the LCC rectifier to

maintain the power balance in the MT-HVDC transmission system, considering the power demands of the LCC inverter and the VSCs. In the transient period during the energization and fault recovery, the MPC plays a significant role in maintaining the stability of the whole system by balancing the power. The functional block diagram of the proposed MPC is shown in **Fig. 4.4**. In the notation used for measured DC pole voltages in **Fig. 4.4**, the third, fourth and the fifth letters in the subscripts of voltages denote the converter type (L:LCC, V:VSC), operating mode (R: rectifier, I:inverter) and pole (P: positive, N:negative) respectively.

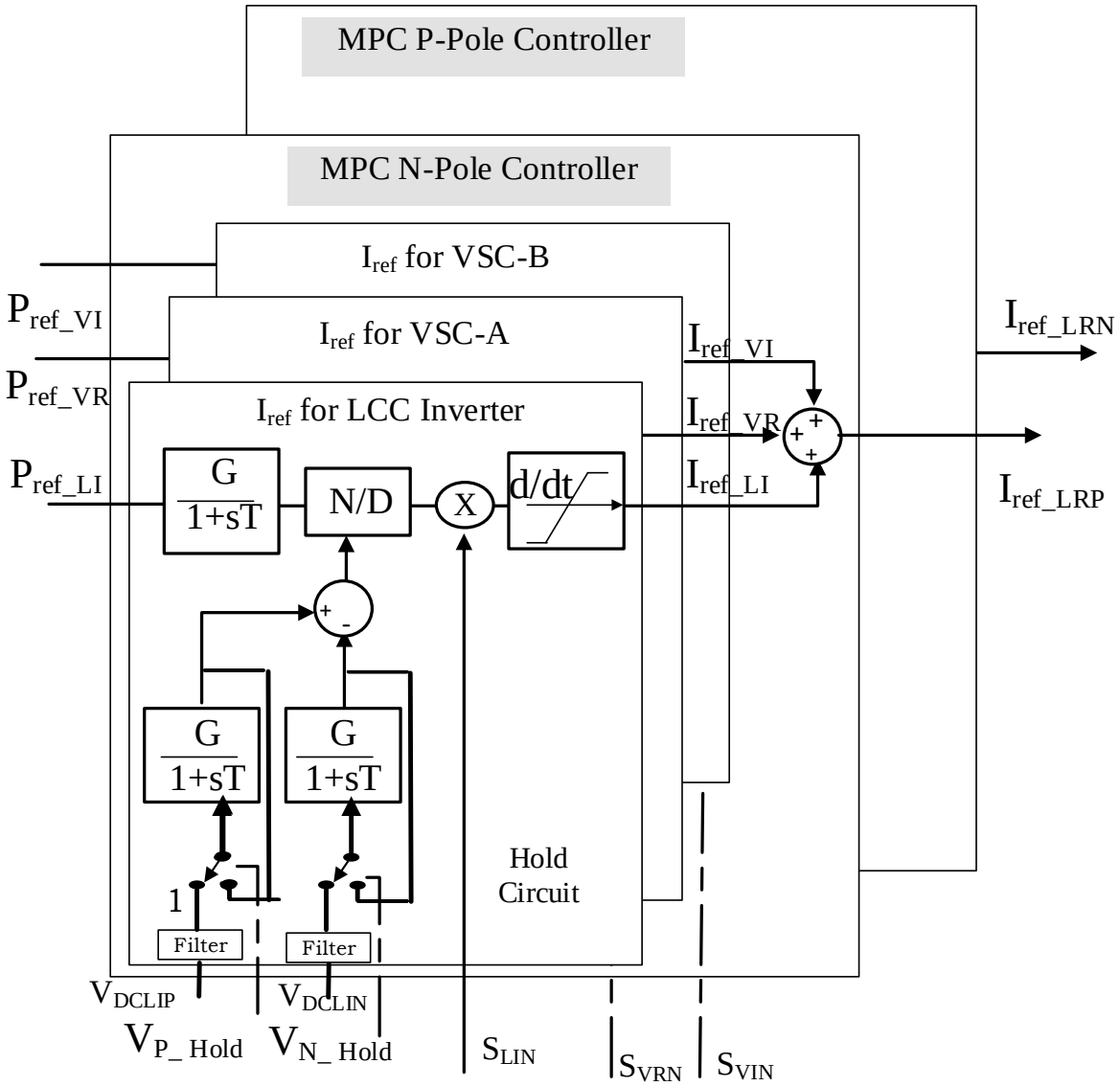


Fig. 4-4. Master power controller with the features required for fault recovery process (© IEEE)

To avoid unrealistic current orders due to low DC voltages that may occur during faults, the input voltage measurements are conditioned by passing through a first-order filter having a 200 ms delay and a hold circuit (activated by signals V_{P_Hold} or V_{N_Hold}). To balance the power demands of the converter stations, the MPC estimates the current order for the LCC rectifier as the sum of currents at the other converters.For example, for N-pole of LCC rectifier, the current order is computed as [133]:

$$I_{ref\_LRN} = \frac{S_{LIN} \cdot R_{LI} \cdot P_{ref\_LI}}{V`_{DCLIP} - V`_{DCLIN}} + \frac{S_{VRN} \cdot R_{VR} \cdot P_{ref\_VR}}{V`_{DCVRP} - V`_{DCVRN}} + \frac{S_{VIN} \cdot R_{VR} \cdot P_{ref\_VI}}{V`_{DCVIP} - V`_{DCVIN}} \quad (4.1)$$

where $V`_{DCLIN}$ etc. are conditioned pole voltage measurements, P_{ref_VR} etc. are power reference values. The binary signals S_{LIP}, S_{VRP}, and S_{VIP} are generated by a fault recovery supervisory function (will be described in **Section-4.5**) to reset the respective current component to zero after detecting a fault. The ramp rate weighting factors R_{LI}, R_{VR}, and R_{VI} are used to match the instantaneous current order of the LCC rectifier with those of the other converter stations. Current orders are computed independently for the positive and negative poles to facilitate single-pole operation and to prevent disturbances to the healthy pole during single-pole-to-ground faults. The MPC is assumed to be located at the LCC inverter and the delays in signal communication should be accounted for.

4.3.3 Energization and Regulation

The LCC link is energized in a similar manner to a two-terminal LCC HVDC link. A control sequence was developed to connect VSC stations to the LCC link to form the multi-terminal system with a minimum undesirable transient. Therefore, the LCC link is first energized with the LCC rectifier operating in current control mode while the LCC inverter controlling the DC voltage through constant extinction angle control. Meanwhile, the VSCs are started in voltage control

mode. Upon reception of a signal indicating that the LCC link has reached it's normal operation condition, as depicted in **Fig. 4.5**, VSCs are switched to voltage tracking mode.

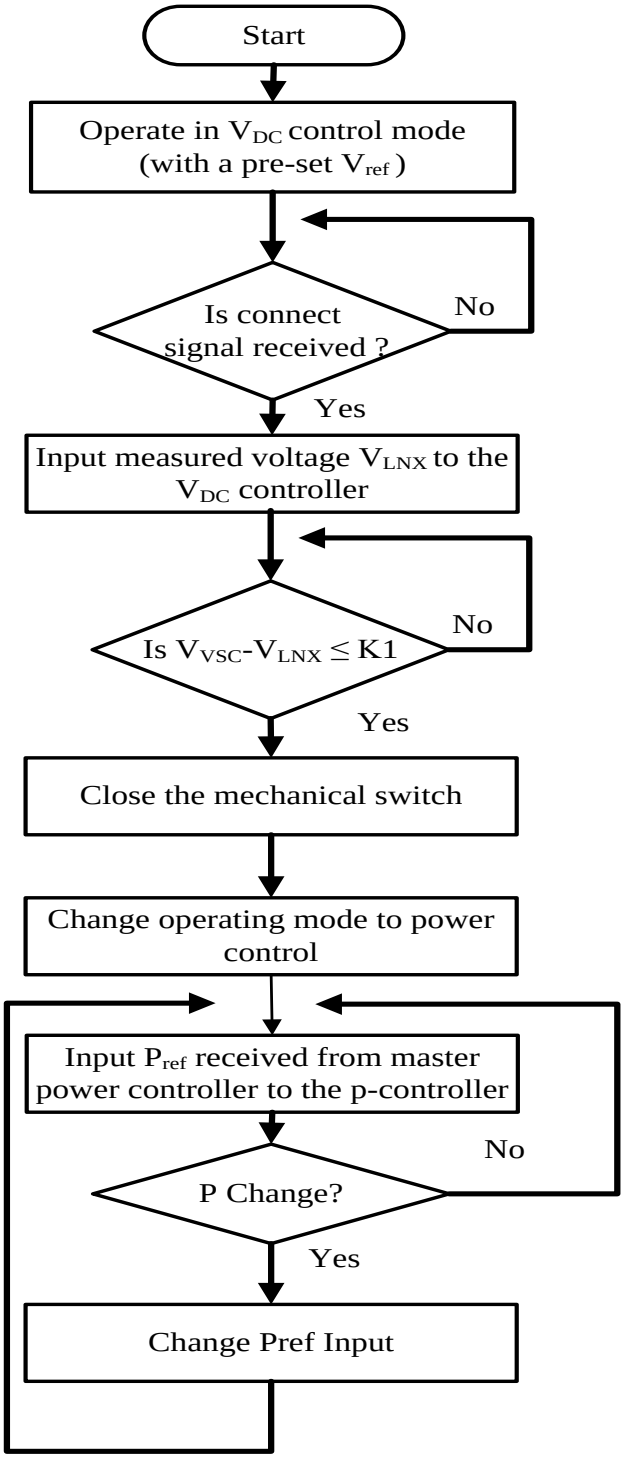


Fig. 4-5. Control sequence applied at VSC station to energize the system and for normal operation (© IEEE)

The voltage tracking mode is achieved by replacing V_{ref} with half of the pole to pole voltage measured at the main transmission line side of the FMSW, $V_{LNA/B}$. A VSC is connected to the LCC link once its DC voltage is approximately equal to the LCC link voltage at the point of coupling. The operating mode of the VSC is changed to the power control mode after a short delay T_{d1}. After connecting to the LCC-HVDC link through mechanical switches, VSCs are operated in power control mode as long as there are no faults.

4.4 MT-HVDC Transmission System Design

The design features of the hybrid multi-terminal HVDC transmission system and controlled by the MPC is described in this section.

4.4.1 Key Features of Hybrid Multi-terminal System

The key features of the multi-terminal HVDC system considered in this study are:

1. A conventional point-to-point LCC HVDC link forms the backbone of the multi-terminal network. No modifications are necessary for the low-level controls of the LCCs.
2. Due to economics, all VSC stations are assumed to be based on the proven and economical half-bridge MMC technology.
3. Due to the high cost and lack of proven commercial technology, DC circuit breakers are avoided. Fast mechanical switches (FMSWs) with no load or fault current interruption capability are used for system reconfiguration.
4. When operating as inverters, high rating diode valves are connected in series with VSC terminals for blocking DC fault currents as proposed in [131]. These diodes need to be bypassed when a VSC operates in the rectifier mode.

Thus, this is a highly practical hybrid MT-HVDC configuration that can be implemented with current commercial technology. The only exception is the high rating diode valves at VSC terminals. **Fig. 4.6** shows the essential elements of the proposed VSC-LCC hybrid multi-terminal HVDC transmission system where two VSCs are connected to an LCC link. Although only two VSCs are considered for the ease of demonstration, the findings can be directly applied to the cases where there are more than two VSCs. In this example, the bypass switch can be used to turn the VSC-A terminal to a rectifier or an inverter to facilitate the two different topologies.

The two specific configurations considered for this MT-HVDC system are:

1. Configuration-1: Both VSCs operate as inverters tapping into the LCC link.
2. Configuration-2: VSC-A operates as a rectifier and VSC-B operates as an inverter in a coordinated fashion injecting and drawing the same amount of power. This is essentially a VSC link piggy-backing on a section of the LCC link.

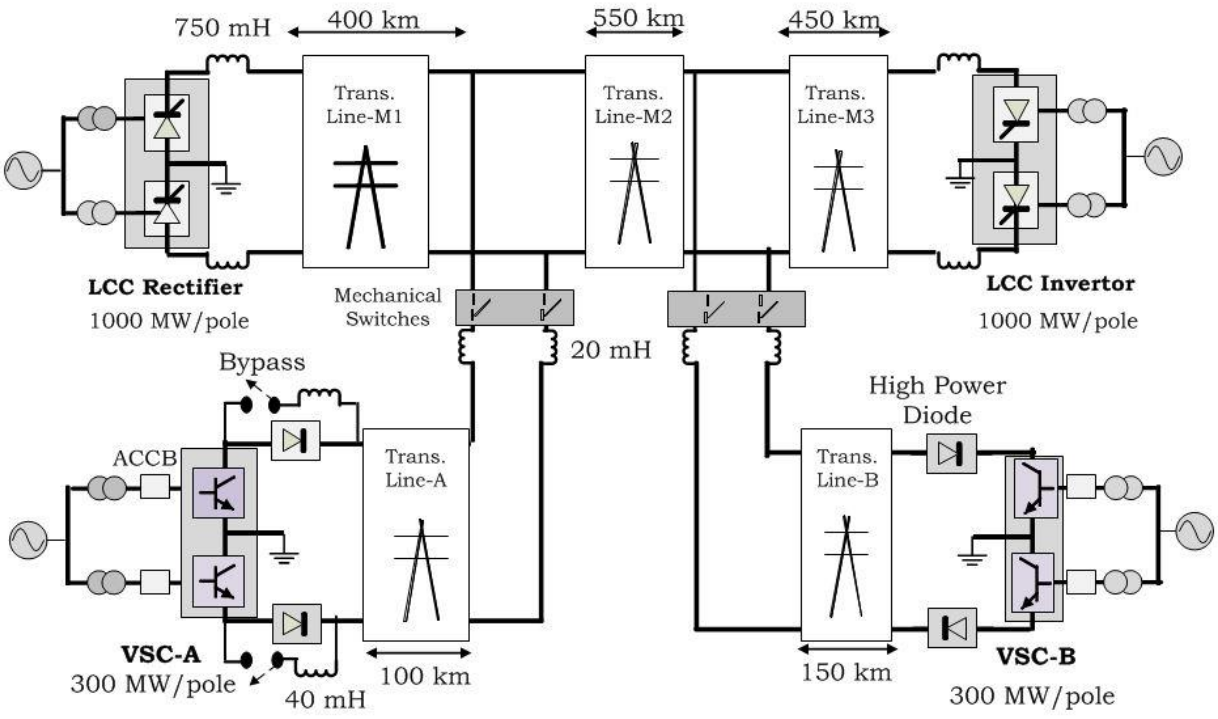


Fig. 4-6. Hybrid VSC-LCC transmission system with two VSCs connected to an LCC-HVDC link (© IEEE)

4.4.2 Fault Recovery Actions at the Converters

A DC side fault can be a temporary fault such as an arcing fault caused by momentary reduction of space between conductors due to wind or a permanent fault such as an insulation break down. Temporary faults in LCC HVDC systems are cleared by reducing the voltage to extinguish the arc. Therefore, once a fault is detected in an LCC HVDC system, the firing angle of the thyristors in the LCC rectifier is increased (the process is called force retardation) to decrease the voltage across the fault. After a short time delay, the firing angle is decreased for restoration while monitoring line voltage and currents (known as reclosing). If the DC line voltage does not increase or a large current is observed, the fault is assumed to be still existing and the force retardation is applied again. When two or three reclosing attempts fail, the fault is assumed to be a permanent fault, and the converters are shutdown.

On the other hand, once a DC side fault is detected, an HB-SM based VSC immediately blocks its IGBTs to avoid possible damages from high fault currents. The converter station is de-energized by opening the ACCB. After allowing the stored energy in the system to dissipate, the VSC can be re-energized while checking whether the fault is still existing. In order to preserve the operation of the healthy pole during a single-pole-to-ground fault, the proposed DC fault recovery process is applied independently for positive and negative poles.

4.5 Fault Recovery Using Fast Mechanical Switches

A procedure of clearing DC side faults via rapid reduction of the fault current with proper co-ordination of recovery actions at each converter station is explained in this section. The procedure presented in [108] is followed to re-energize the MT-HVDC transmission system after clearing the fault.

The objective of the proposed DC fault clearing strategy is to minimize the extent of outages, with priority being the continuation of the operation of the LCC link. It is assumed that there are no DC circuit breakers and the fault isolation is achieved with the fast mechanical switches (FMSWs). All VSCs that may operate in inverter mode are provided with high rating series diode valves as illustrated in **Fig. 4.6**. The FMSW is capable of opening only after its through-current becomes negligibly small. Therefore, fault clearing involves a rapid reduction of current through the FMSW and quick opening of FMSW to disconnect the VSCs and the branch lines from the mainline. During this de-energization, temporary faults are likely to be self-cleared.

Since the priority is to continue operation of the main LCC link, FMSWs are installed at the tapping points on the VSC branches as shown in **Fig 4.6**. The presence of any permanent fault can be identified during the re-energization. The LCC link is re-energized first, if no fault is identified during the re-energization, existence of any permanent fault on the LCC link can be ruled out. Therefore, the LCC link can continue its operation even if there is a permanent fault on a VSC branch, as they are already isolated by opening the FMSWs. A permanent fault on a VSC branch can be identified when re-energizing the respective VSC station, and the faulted branch can be left isolated from the rest of the system by leaving the FMSW open. Therefore, during a permanent fault on any VSC branch, the operation of the rest of the transmission system can be continued with the proposed switching arrangement.

4.5.1 Recovery Actions in the LCC Stations

The overall fault recovery procedure applied at the LCCs is demonstrated for P-pole in **Fig. 4.7**. As depicted in **Fig. 4.7**, upon detection of a fault at the LCC rectifier, force retardation is

applied by increasing the firing angle of the rectifier. The fault detection signals that initiate the fault clearing and recovery process are assumed to have a time delay t_{DX} given by (4.2) [133].

$$t_{DX} = v \cdot l_{FX} + t_D \tag{4.2}$$

where l_{FX} is the distance to fault from the station, v is the propagation velocity of the fault generated surge and t_D is the time to detect the fault upon arrival of the fault wave [103]. Upon detecting a fault, the signal S_{LIX} and V_{X_hold} are sent by the rectifier to the MPC to notify the fault. During the force retardation, the power reference switching function of the faulty pole-x, S_{LIX}, is set to zero, and the voltage inputs are held at pre-fault values (by setting the V_{X_hold}=0) until the fault recovery is completed. When the firing angle reaches to 140°, it is held for a specified period to quench the fault arc. Then, the rectifier firing angle is decreased while checking if the voltage increases (also, the current can be tested).

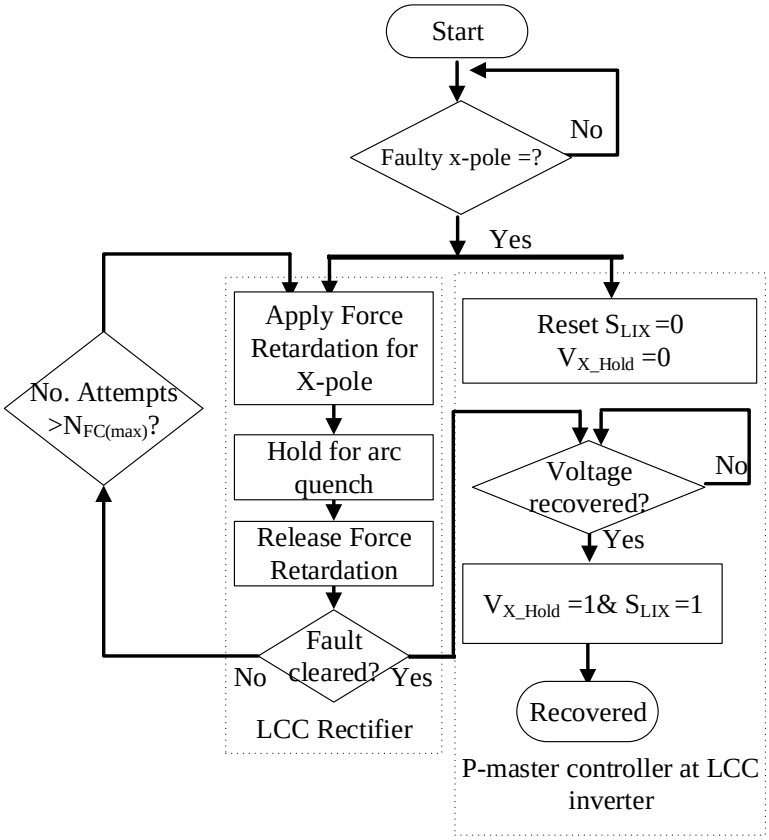


Fig. 4-7. Fault recovery process of LCC-link (X = P or N depending on the pole) (© IEEE)

4.5.2 Fault Recovery Actions in the VSC Stations

Fig. 4.8 shows the procedure proposed for VSCs during the fault clearing and recovery. When an overcurrent is detected, IGBTs in a VSC converter are immediately blocked by the internal protection.

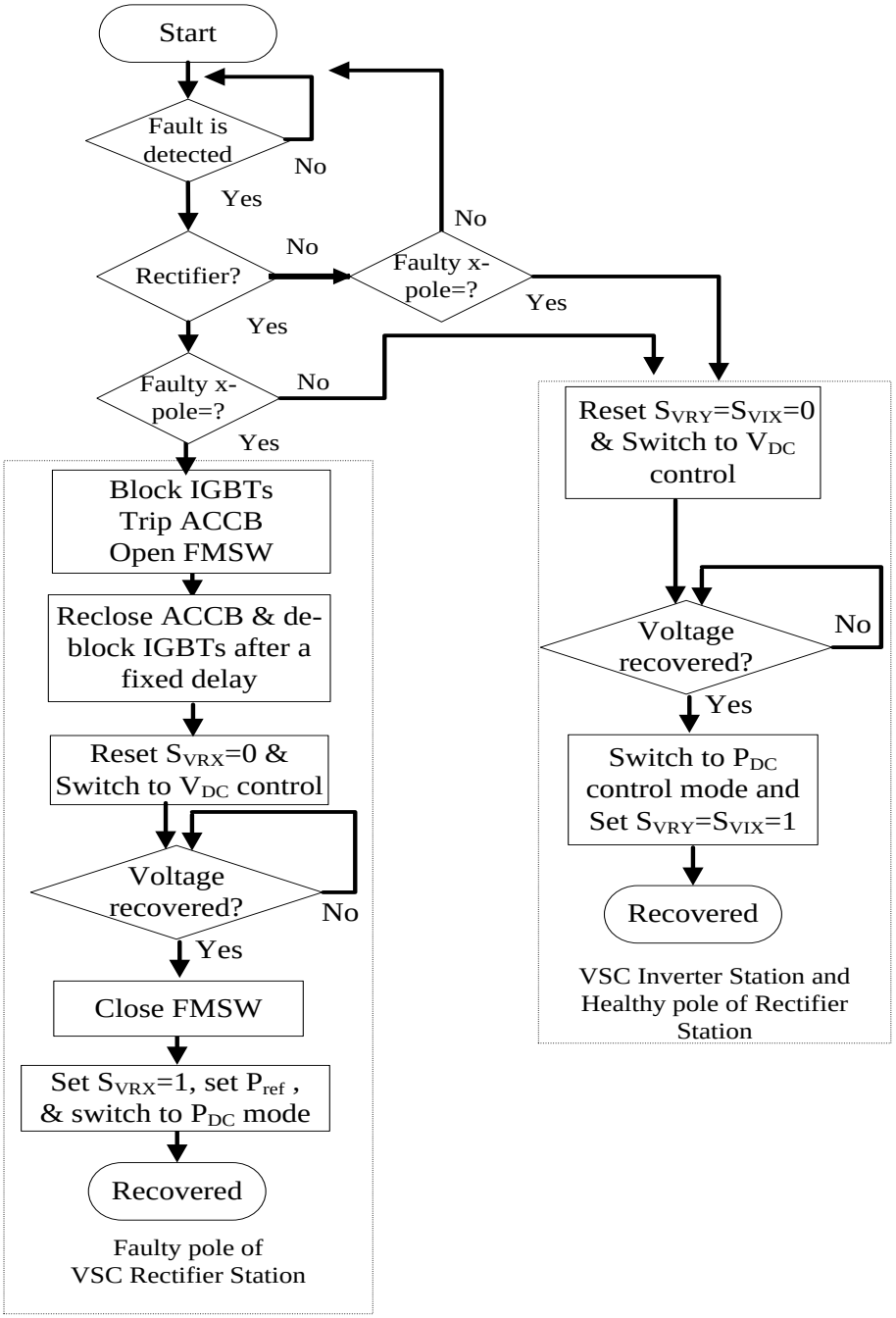


Fig. 4-8. Fault recovery process at VSCs (© IEEE)

Due to the high rating series diode valves, which are now reverse biased, there will be no fault current contribution from the VSC inverters. When a VSC converter is operating as a rectifier, the diode valves remain bypassed. Thus, the faulty pole of the VSC rectifier is de-energized by opening the corresponding AC side CB. Then the FMSW on the faulty pole of the line connecting the VSC rectifier and the LCC link is commanded to open. However, FMSW actually opens only when the current through it drops below the maximum interruptible current (assumed 0.05 kA in this study). After a short time delay, the ACCB is reclosed. If the reclosing is successful, i.e. no permanent fault exists in the line segment connected to the particular VSC rectifier, it is re-started in the voltage control mode. Once the LCC link is restored, VSC terminals are connected to the LCC link following the same process as during the initial start-up. The described fault recovery process requires input signals for initiating force retardation, switching VSC operating mode, resetting power reference of the master power controller (S_{LIX}) and VSCs, and holding voltage measurements (V_{P_hold}). Also, if a VSC rectifier is involved, additional signals are required to open the ACCB and the FMSW.

4.6 Test System

The LCC scheme considered in this study is based on the Bipole-II of Manitoba Hydro's Nelson River HVDC system [122]. There is no DMR conductor in the transmission system and any single-pole operation is assumed temporary. Although ground return operation may be objectionable in some jurisdictions, temporary monopole operation is allowed in many places like Manitoba. Therefore, it is assumed that the earth return mode is allowed for a short period, about one second, for single pole fault recovery. Important parameters of the test system are given in **Table 4.1**.

Table 4-1 Test system details (© IEEE)

Parameter	Value	Units
Nominal DC Voltage	±500	kV
AC Sys. SCR LCC-Rectifier	2.9	
AC Sys. SCR LCC-Inverter	5.0	
AC Sys. SCR VSC-A/B	3.0	
Power ramping rate (per pole)	200	MW s^{-1}/pole
Power ramping rate in LCC during fault recovery	1000	MW s^{-1}/pole
Power ramping rate in VSC during fault recovery	500	MW s^{-1}/pole
Transformer Data		
Apparent Power -LCCs	600x2	MVA/pole
Apparent Power -VSC-A/B	200	MVA/pole
Leakage Reactance-LCCs	0.15	pu
Leakage Reactance-VSCs	0.1	pu
Transformer Ratio LCCs	230 kV/209 kV	
Transformer Ratio VSCs	315 kV/375 kV	
VSC Data		
MMC cell capacitance	2000	µF
MMC cell switch on resistance	0.05	Ω
Arm reactor	50	mH

Each LCC converter station consists of two-twelve pulse LCCs supplied by two separate converter transformers. As the VSC interconnection is proposed for both existing and new LCC-HVDC links, the conventional LCC controls are used. The control diagrams of LCC rectifier and the LCC inverters are respectively shown in **Fig. A-2** and **Fig. A-3** of **Appendix-I**. During the force retardation, the firing angle of the rectifier is increased at a rate of 0.5 °/ms and force retardation is released at a slower rate, which is about 1/3 of the rate used to increase the angle. Both DC and AC side filters are included in the model. This work builds on the control sequence discussed in [108] that shows the safe and smooth operation of the MT-HVDC transmission

system. A voltage-dependent current order limit (VDCOL) is implemented at the inverter to protect the thyristor valves during AC side faults. As it is depicted in **Section-2** of **Appendix-I**, the MMC cell capacitance is selected in such a way that the energy to power ratio [132] is 25 J/kVA. A 20 mH di/dt limiting series inductor (with 0.05 Ω resistance) is connected in series with each mechanical switch and a 40 mH di/dt limiting inductor (with 0.1 Ω resistance) is inserted at each VSC terminal when operating as a rectifier. IGBT blocking logic is generated using an overcurrent fault detection logic which picks up when the current through any IGBT increases above 2 pu. A fixed detection delay of 30 μs was assumed conservatively. Fast mechanical switches (FMSW) were assumed to be capable of breaking 0.05 kA within 2 ms. An ACCB can break currents only at a zero crossing and was modeled with a three-cycles opening delay.

4.7 Validation of Normal Operation

In this sub-section, the performances of proposed energization and regulation scheme is evaluated. Two possible operating modes explained in **Section-4.4.1** are considered.

4.7.1 Unidirectional Operation: LCC Link Tapped by VSC Inverters

The following sequence of inputs was applied with controls to evaluate the configuration where both VSC stations operate as inverters (Configuration-1) tapping-off power from the main LCC link.

3. LCC inverter is energized with –600 MW/pole @t=0 sec.
4. VSCs are started up in DC voltage control mode. Reference inputs for VSC-A and VSC-B are set to 515 kV and 520 kV respectively.

5. At t=1.75s, VSCs are switched into tracking mode.
6. At t=3.25s, after LCC link is successfully energized, two fast mechanical switches are closed.
7. Thereafter, the power orders of the VSC inverters are changed in the following sequence:
    (i) set P_{refB} to −200 MW/pole @t=4.5 sec,
    (ii) set P_{refA} to −100 MW/pole @t=6.5 sec.

Figs. 4.9 - 4.12 show the measured DC side responses at each converter station for the above sequence of inputs. According to **Fig. 4.9(b)** and **Fig. 4.10(b)**, the LCC inverter current increases at the same rate as the rectifier current till the VSCs are connected. No undesirable transients were observed in the voltages or currents of the LCC rectifier and the LCC inverter. **Fig. 4.11(b)** and **Fig. 4.12(b)** show ramping of currents at the VSC terminals. The LCC rectifier current gradually increases to accommodate the power delivered to VSC inverters, but no noticeable change in current is observed at the LCC inverter during this period as depicted in **Fig. 4.10(b)**. According to figures showing the converter voltages, no noticeable transients were observed in the voltages during the startup or when closing the fast mechanical switches.

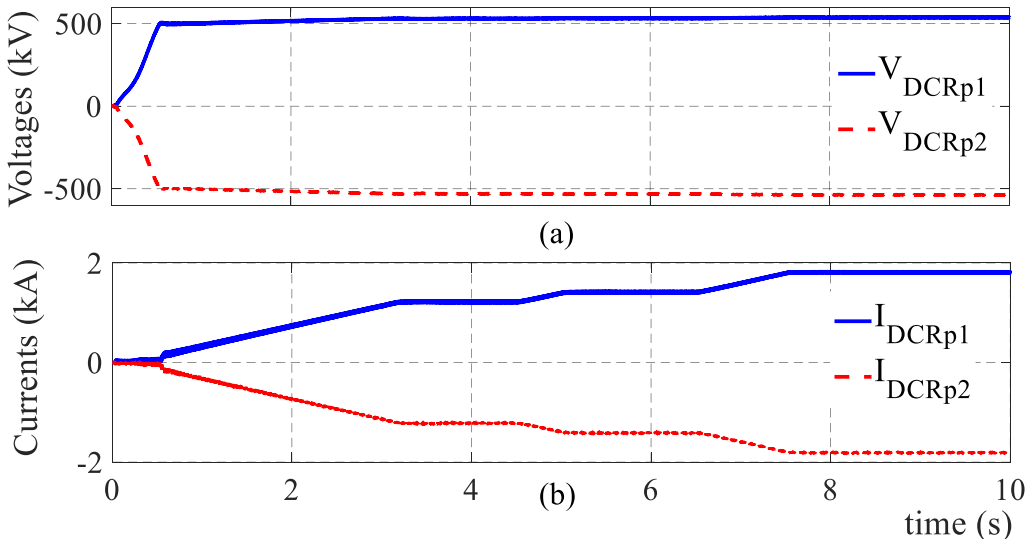


Fig. 4-9. DC side measurements at LCC Rectifier (a) Voltages, (b) Currents (© IEEE)

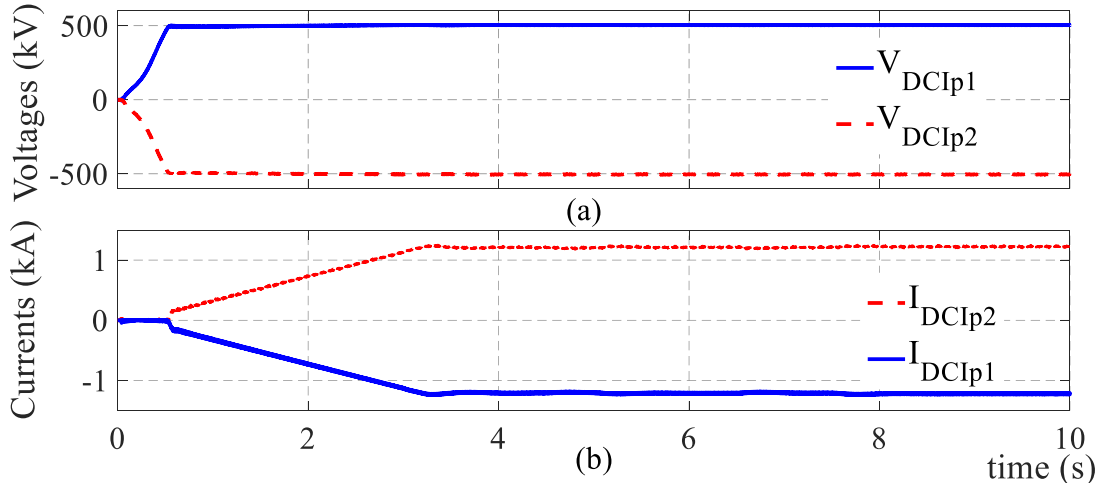


Fig. 4-10. DC side measurements at LCC Inverter (a) Voltages, (b) Currents (© IEEE)

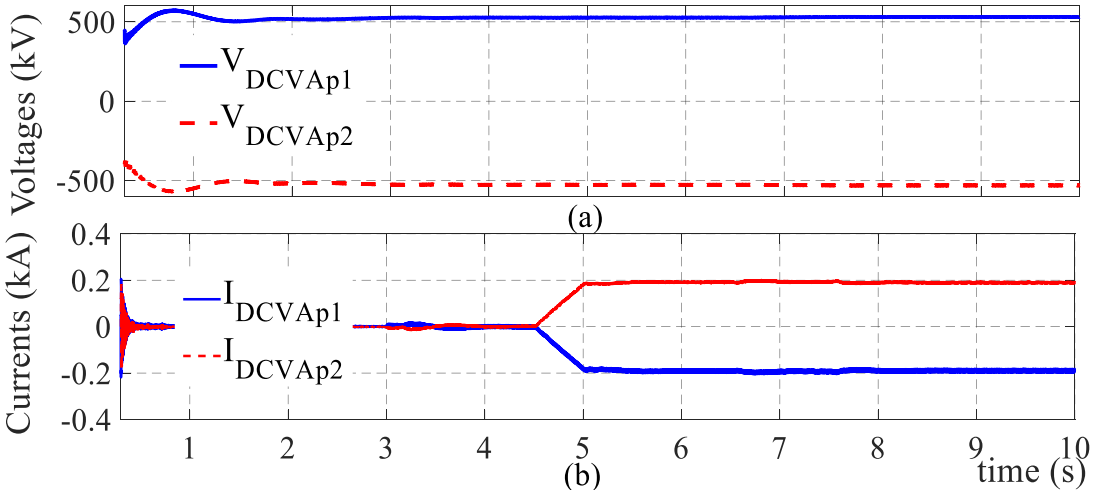


Fig. 4-11. DC side measurements at VSC-A (a) Voltages, (b) Currents (© IEEE)

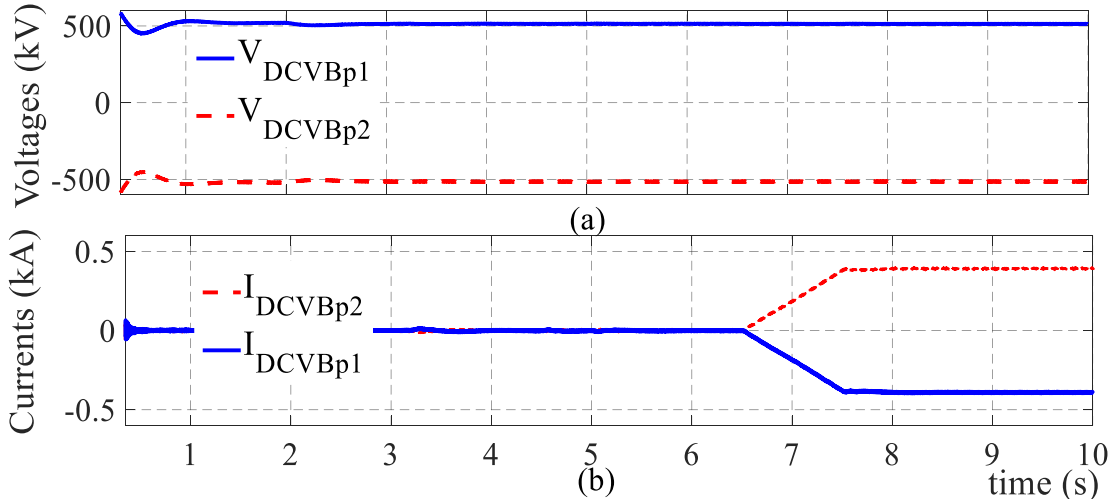


Fig. 4-12. DC side measurements at VSC-B (a) Voltages, (b) Currents (© IEEE)

Note that the power order was ramped up by the MPC at the rate of 200MW/s per pole. Therefore, as depicted in **Fig. 4.13(a)**, it took about 3s to reach the required power flow in the LCC link (For ease of comparison, the negated LCC rectifier output power is shown in **Fig. 4.13(a)**).

A difference in power between the LCC rectifier and the LCC inverter shown in **Fig. 4.13(a)** during 3s-4.5s represents the transmission losses. However, when the VSCs switched to power control mode, this difference widened due to the power demand of the VSCs. **Fig. 4.13(b)** shows a transient during the mechanical switch closing. Just after ramping the power in VSCs, a slight change in LCC inverter power is observed in **Fig. 4.13(a)**.

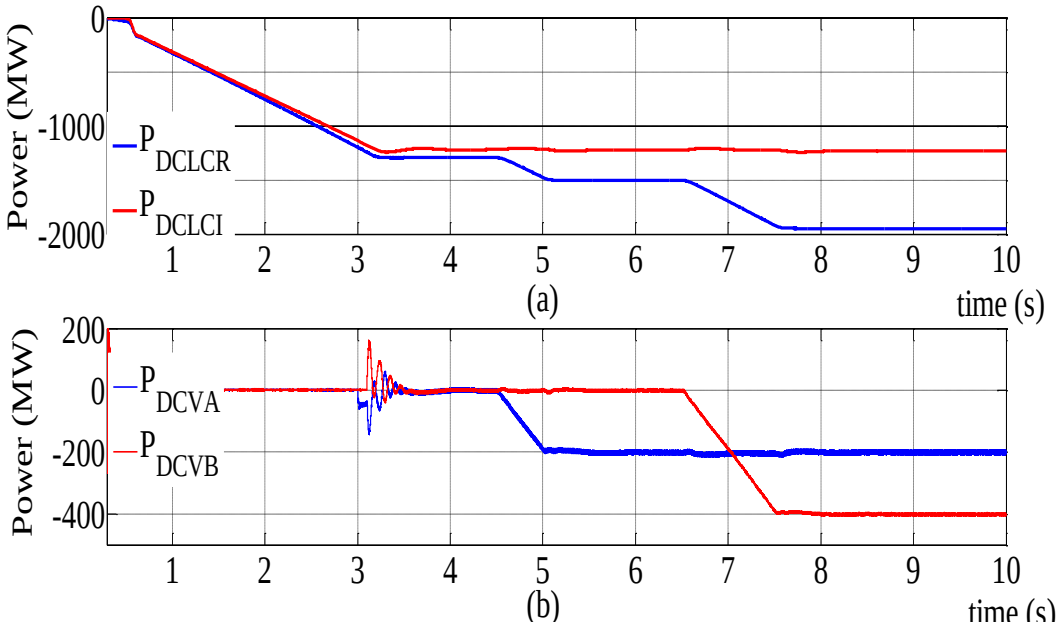


Fig. 4-13. Estimated power injection at each converter terminal (© IEEE)

The AC side voltages and currents during the considered operation are shown in **Fig. 4.14**. A transient in AC current was observed at the VSCs during the energization. However, no undesirable transients were observed at the AC side of any of the converters during the normal operation except for a gradual drop in AC voltage at the LCC rectifier with increasing current.

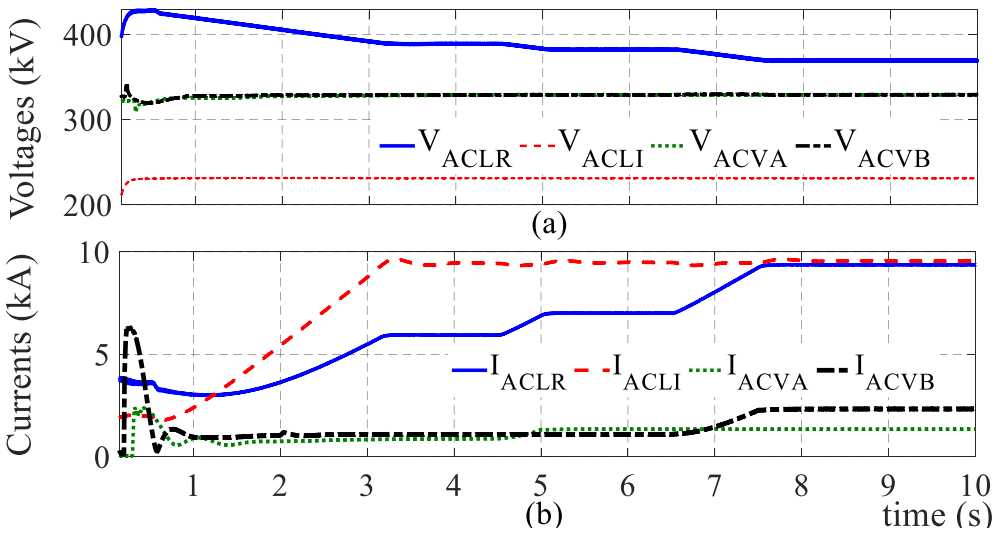


Fig. 4-14. AC side rms measurements (a) line voltages, (b) line currents (© IEEE)

4.7.2 Main Transmission Line Shared by LCC and VSC Links

In Configuration-2, VSC-A is operated as a rectifier and while VSC-B is operated as an inverter. Observations were taken when the transmission system was shared in such a way that the LCC rectifier feeds the power demanded by LCC inverter and VSC-A feeds the power to VSC-B. The following sequence of events was simulated.

1. LCC link is energized with -850 MW/pole @t=0 sec.
2. VSCs are connected to the main transmission line as explained in the **Section-4.3.3**.
3. At t=5s, VSC-A is issued 250 MW/pole power command.
4. In order to evaluate the impact of any difference of communication delay between the VSC rectifier and the inverter, VSC-B is issued -250 MW/pole command 100 ms after VSC-A.

Figs. 4.15 – **4.19** show measured DC side responses at each converter station. According to **Fig. 4.15(b)** and **Fig. 4.19(b)**, no impact of connecting VSCs or power flow between VSCs is visible at LCC converter terminals.

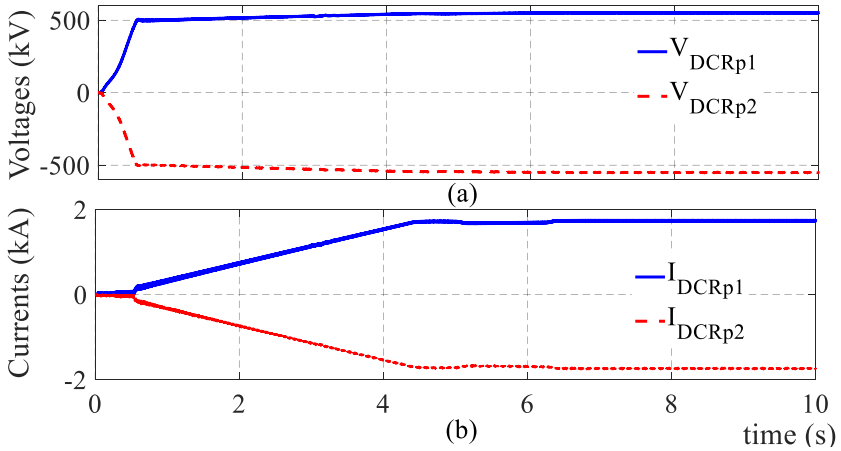


Fig. 4-15. DC side measurements at LCC Rectifier (a) Voltages, (b) Currents (© IEEE)

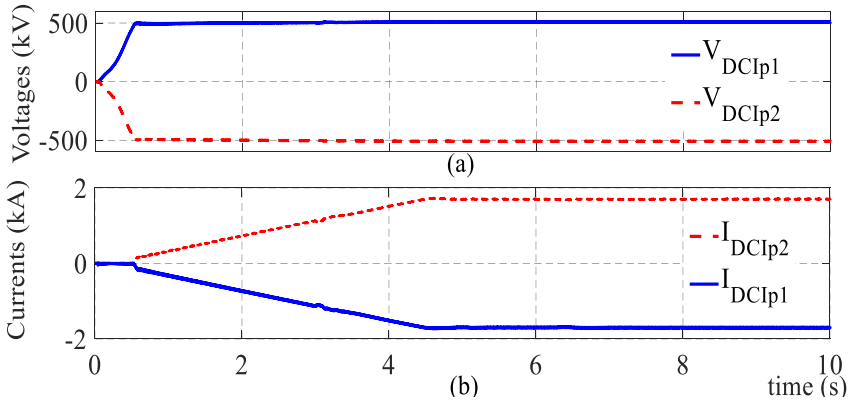


Fig. 4-16. DC side measurements at LCC invertor (a) Voltages, (b) Currents (© IEEE)

According to **Fig. 4.17(b)** and **Fig. 4.18(b)**, almost similar magnitudes of current were observed in VSC-A and VSC-B. Therefore, it can be concluded that the VSC link and the LCC link can be operated almost independently with the help of the proposed controller scheme.

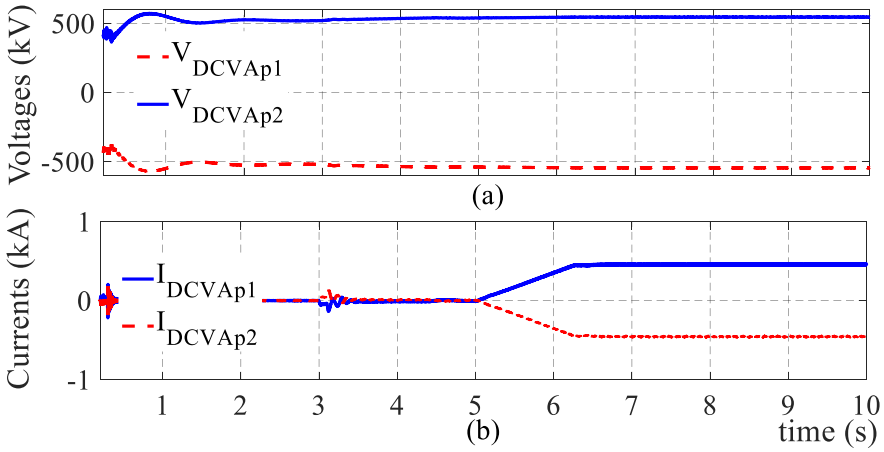


Fig. 4-17. DC side measurements at VSC-A (a) Voltages, (b) Currents (© IEEE)

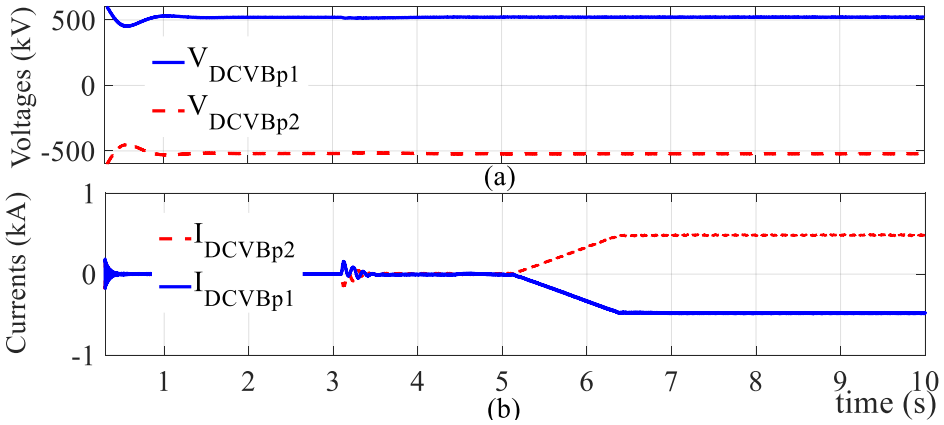


Fig. 4-18. DC side measurements at VSC-B (a) Voltages, (b) Currents (© IEEE)

Fig. 4.19 compares the rectifier and inverter station power levels at each type of converter stations (For ease of comparison, negative of the rectifier power is drawn). Due to different time delays in receiving power order commands at each converter station, as seen in **Fig. 4.19(b)**, there was a small difference in power (about 20MW or 4%) between the inverter and rectifier stations of the VSC link during power ramp-up.

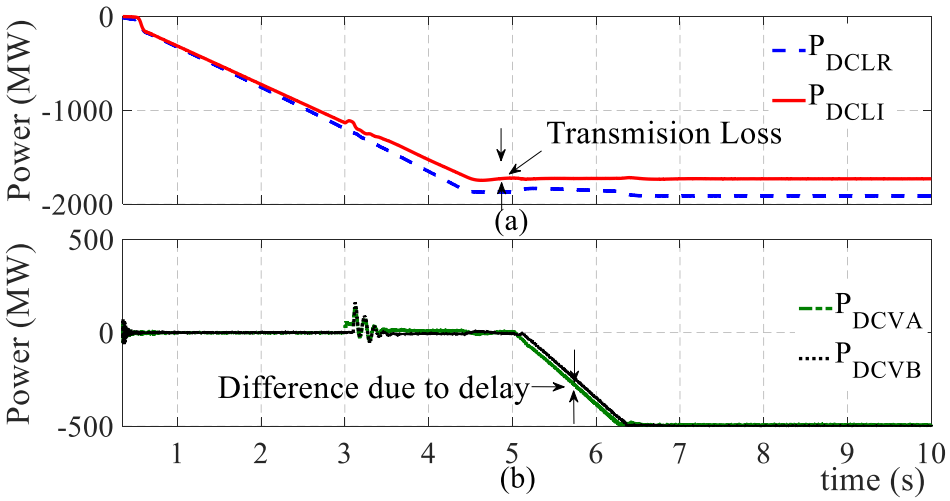


Fig. 4-19. Power through each station (a) LCC stations, (b) VSC stations (© IEEE)

Changes in power level at the inverter due to a sharing transmission system with a VSC link was investigated by plotting the power difference between the instantaneous reference value and the measured power at the terminals as shown in **Fig. 4.20**. According to **Fig. 4.20**, the highest error of about 50MW (0.029 pu) occurred at the LCC inverter during the transient.

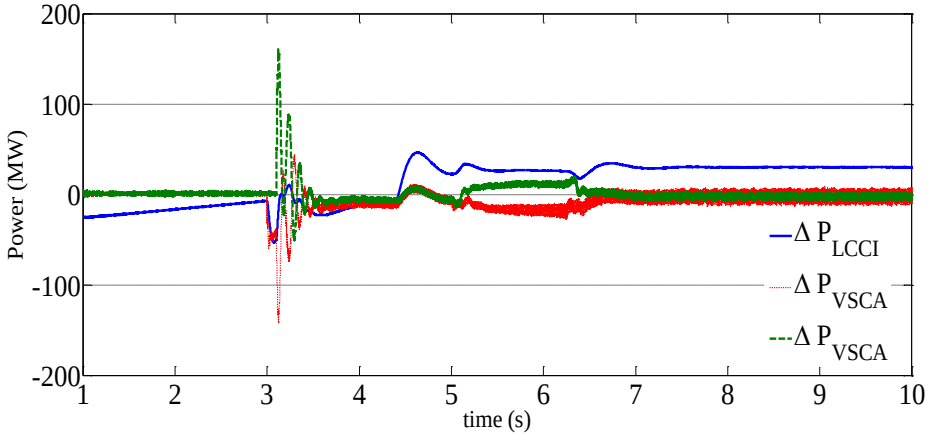


Fig. 4-20. Difference between the reference and received power levels (© IEEE)

Fig. 4.21 shows the AC side voltages and currents during the considered operation. Therefore, it can be concluded that the proposed coordination controller, and the energization and regulation procedures for MT-HVDC system proposed in **Section-4.3.3** provides a commendable level of performance during the normal operation of the hybrid LCC-VSC MT-HVDC system.

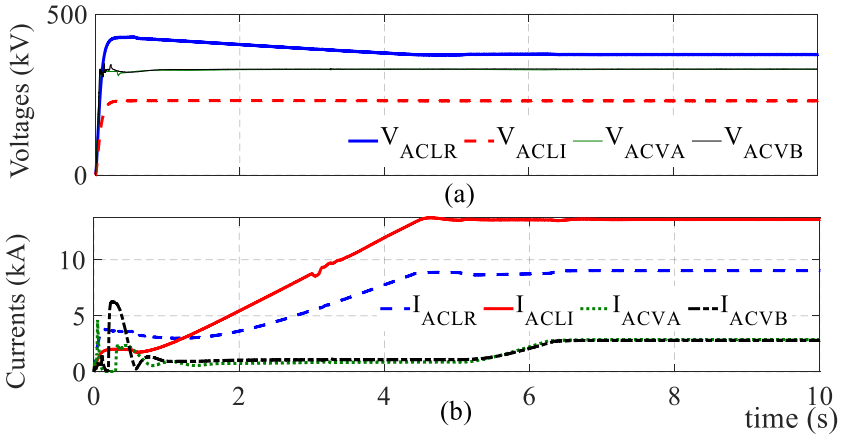


Fig. 4-21. AC side rms measurements (a) line voltages, (b) line currents

4.8 Validation of Fault Recovery Scheme

In this section, the fault recovery scheme described in **Section-4.5** is evaluated with both symmetrical (P-pole-to-N-pole) and asymmetrical (single-pole-to-ground) faults on different sections of the transmission system. The simulation results for the fault scenarios listed in **Table 4.2** is presented in this section. Configuration-2, which is the more general and difficult case, is

considered first for detailed investigation, and some results are presented for Configuration-1. For simplicity, arcing faults were simulated as fixed-resistance faults which self-clear when the fault current drops below 100 A. Since the temporary faults are considered in this section, all converters return to their pre-fault operating condition after recovering from a fault. Following the energization procedure discussed in **Section-4.3.3**, faults are applied at 11s. First two fault scenarios are simulated when the LCC link is operating at 600 MW/pole and the VSC link is operating at 300 MW/pole. The last two fault scenarios described in **Table 4.2** are simulated when the LCC inverter draws 600 MW/pole and each VSC inverters draws 200 MW/pole.

Table 4-2 Demonstrated fault scenarios (© IEEE)

Scenario	Config.	Fault	
		Type	Location
A	2	P→N	Line-M @ 400 km from LCCR
B	2	P→G	Line-B @ 100 km from VSC-B
C	1	P→N	Line-A @ 50 km from VSC-A
D	1	N→G	Line-M @ 200 km from LCCI

Since the FMSW has no-fault current interruption capability, the recovery procedure involves quick re-energizing of the whole transmission system despite of the location of the fault. Furthermore, very accurate fault detection delay is not critical to the process, except for the fault behavior of VSC stations which is influenced by the IGBT blocking delay time. Fault recovery actions are initiated after the delay described in (4.2). Considering the worst case, it was assumed that the propagation velocity $v = 200\ \mathrm{km/ms}$ and the fault detection delay $t_D = 0.5\ \mathrm{ms}$ [103]. However, fault detection and IGBT blocking logic were incorporated into the VSC models.

4.8.1 Fault Recovery in Configuration-2: Symmetrical Faults

To evaluate fault recovery performance of Configuration-2 (where the VSC link piggy-backs on the LCC link) during a symmetric fault, fault Scenario-A described in **Table 4.2** was simulated. After the detection delay described in (4.2), as depicted in **Fig. 4.22(a)** and **Fig. 4.22(b)**, a 250 ms force retardation pulse was applied to the LCC rectifier firing angle controller and a 300 ms wide reset pulse (S_{LIX}) was sent to the master power controller.

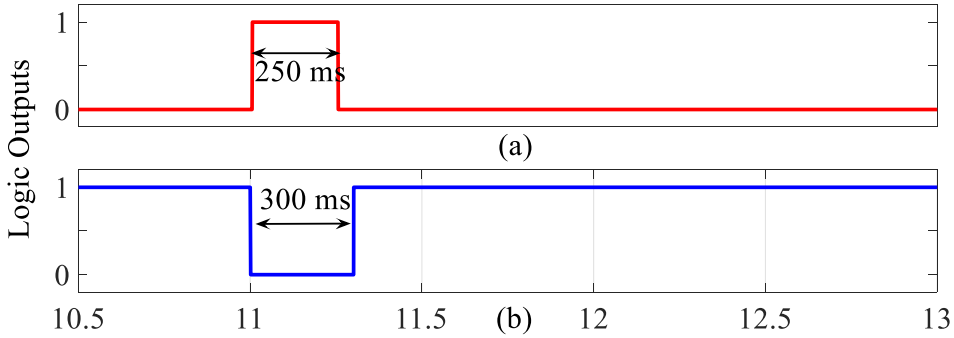


Fig. 4-22. Control signals (a) Force retardation pulse, (b) S_{LIX} signal (© IEEE)

Fig. 4.23(a) depicts the trip signal to ACCB connected to VSC-A. The ACCB opened after a 3-cycle delay, remained open for about 450 ms and then reclosed. As depicted in **Fig. 4.23(b)**, IGBTs were blocked immediately after detecting the fault and de-blocked after reclosing the ACCB.

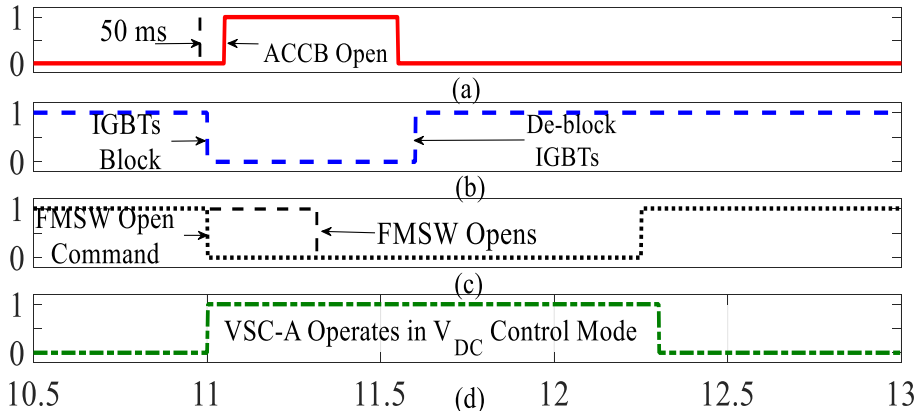


Fig. 4-23. (a) ACCB status, (b) IGBT blocking signal, (c) State of FMSW, (d) Control mode of VSC-A (© IEEE)

A trip signal was issued to FMSW immediately after detecting a fault at the terminal of VSC-A, but it actually opened only when the fault current drops below 0.05 kA, after about 300 ms. FMSW reclosed when the LCC link was fully recovered and the VSC-A voltages were brought up to the connection point voltages. **Fig. 4.23(d)** shows the command for VSC-A to change its operating mode. VSC-A changes to voltage control mode when the fault was detected and reverted to power control mode about 50 ms after the reclosing of FMSW. **Fig. 4.24** shows the sudden increase of LCC rectifier current from 0.6 pu to 2 pu when the fault occurred. However, force retardation brought the rectifier current to zero within 130 ms. As shown in **Fig. 4.25**, the VSC fault current rose very rapidly up to about 8 pu. Until the IGBTs were blocked (instant shown by marker-A), both the transmission line capacitance and MMC capacitors contributed to the fault current. Following that, until the ACCBs were opened (marker-B and can be verified by **Fig. 4.27(b)**), the fault current was all due to contribution by the AC grid. The trailing part of the fault current is the discharging of energy on the DC line through the anti-parallel diodes. It took about 300 ms for this fault current to decay to a level that allows the temporary fault to extinguish. Thereafter, the DC voltage of the LCC link was restored (in about 0.7 s).

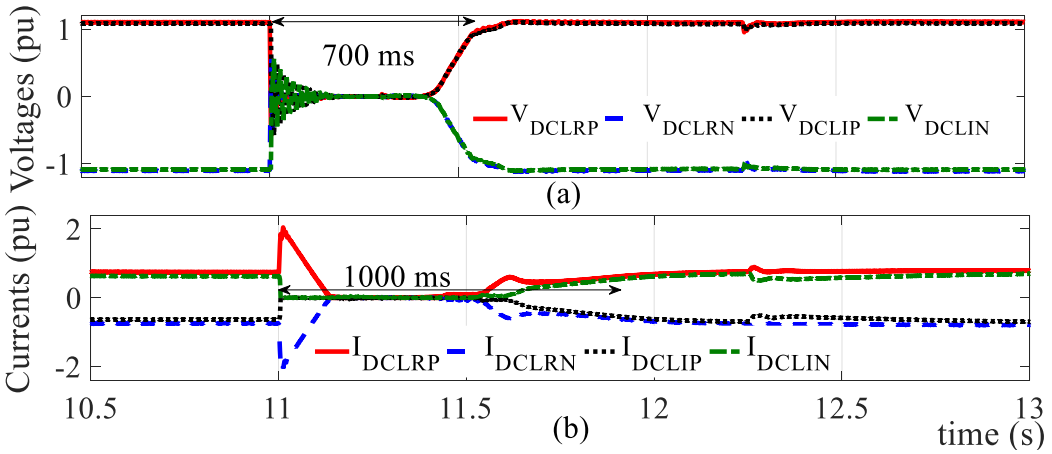


Fig. 4-24. DC side measurements at LCC stations during a P-Pole to N-Pole faults on the mainline (a) Voltages, (b) Currents (© IEEE)

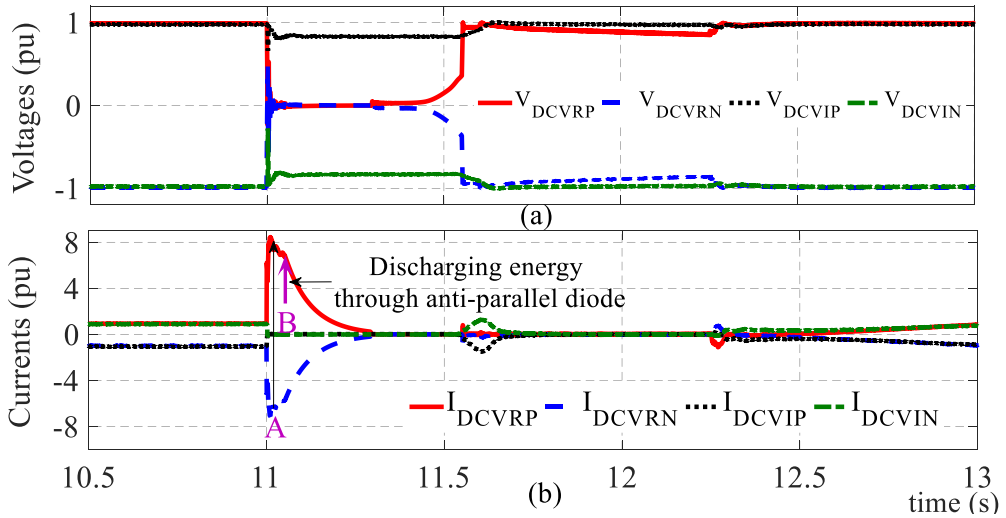


Fig. 4-25. DC side measurements at VSC stations during P-pole to N-pole faults on the mainline (a) Voltages, (b) Currents (© IEEE)

Another 0.25 s was needed to restore the pre-fault state by ramping up the power order. The time taken from the fault inception to complete the recovery to the pre-fault state is given in **Table 4.3**.

As seen in **Fig. 4.25**, there was no fault current contribution from VSC-B and its DC voltage remained almost unchanged during the fault recovery process due to high rating series diodes. According to **Fig. 4.26(a)**, voltages across sub-module capacitors did not completely discharge as the IGBTs were blocked immediately after detecting the fault.

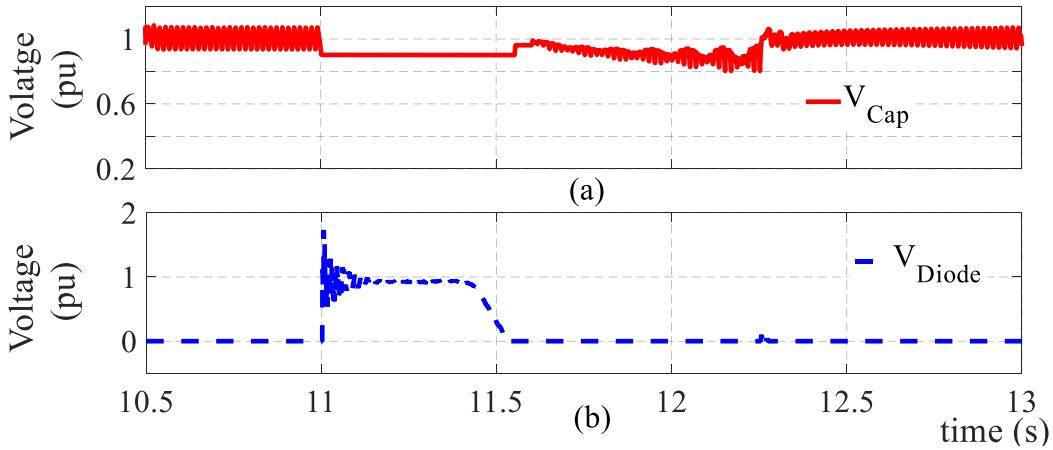


Fig. 4-26. (a) Sub-module capacitor voltage, (b) Voltage across the protection diode of VSC-B (any pole) (© IEEE)

The reverse transient voltages across the high rating series diode valves at VSC-B were as high

as 1.5 pu during the fault, as seen in **Fig. 4.26(b)**. The peak fault current at VSC-A was very large compared to the fault current injected by the LCC rectifier which has a very large inductor (750 mH). Note that this fault current was flowing through the freewheeling diodes of MMC switching cells as the IGBTs were kept blocked after the fault was detected [135]. Shunt connected thyristors that fire during DC side faults were used to protect freewheeling diodes from prolong large fault currents [135-136]. After clearing the fault, VSC-A was re-energized by re-closing ACCB and de-blocking IGBTs after 50ms. After bringing the DC voltage of VSC-A to the proper level, FMSW was closed to re-connect VSC-A to the LCC-HVDC link.

Fig. 4.27 shows the observed variations of AC side voltages and currents (rms values) during the fault clearing and recovery process. The base quantities for per unitizing AC side measurements were the rated converter power and the rated AC side winding voltage of the transformer.

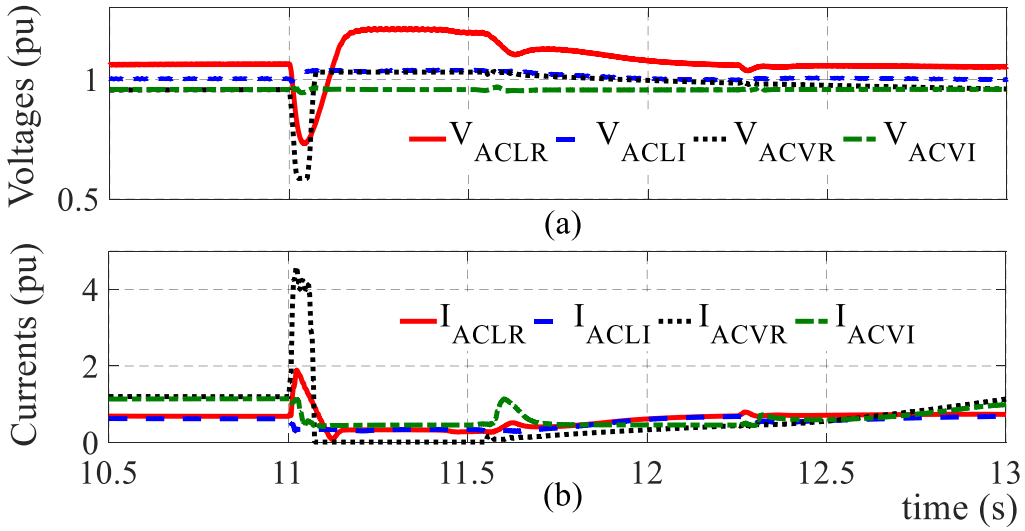


Fig. 4-27. AC side measurements during P-pole to N-pole faults on the mainline (a) Voltages, (b) Currents (© IEEE)

According to **Fig. 4.24**, the rectifier AC currents (both VSC and LCC), increased rapidly during the fault (up to about 4 pu and 2 pu respectively) and as a result, the AC voltage of VSC-A dropped to 0.6 pu. As seen in **Fig. 4.27**, a safe and stable restoration was achieved utilizing a delay before

issuing the power orders for VSC link following the restoration of the LCC link. On the other hand, the sudden re-energization of VSC-A can cause a drop in AC side voltage due to the sudden rise in current drawn from the AC system.

4.8.2 Fault Recovery in Configuration-2: Asymmetrical Faults

Fig. 4.28 shows the observed DC side voltages and currents at LCC station terminals during fault Scenario-B, a solid P-pole-to-ground fault at the middle of LCC and VSC-B interconnection. As depicted in **Fig. 4.29**, the fault current contribution from the faulty pole of VSC rectifier reached to a peak value of 8 pu. A strong transient is visible in the healthy pole current as well. **Fig. 4.30(a)** depicts a substantial drop in the AC side voltage of the VSC rectifier. This drop in voltage is caused by the large AC current drawn by the VSC rectifier. This drop in AC voltage makes it difficult to preserve power flow through the healthy pole of the VSC rectifier. Therefore, the power order of the healthy pole of VSC rectifier is reduced to zero. Hence, the power received by the voltage controlling converter station, LCC inverter, is suddenly dropped.

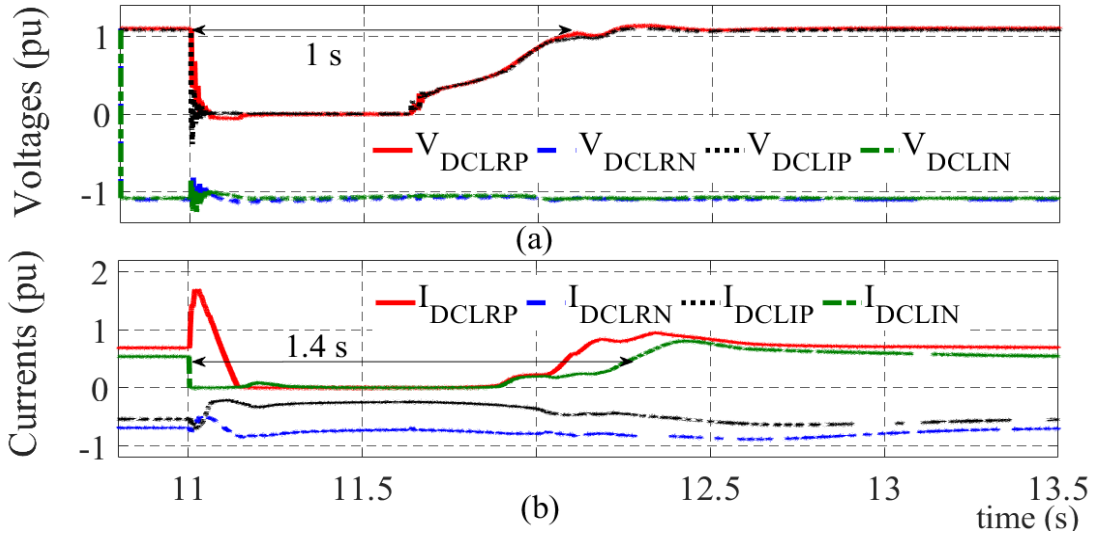


Fig. 4-28. DC side measurements at LCC stations during P-pole-to-ground faults on Line-B (a) Voltages, (b) Currents (© IEEE)

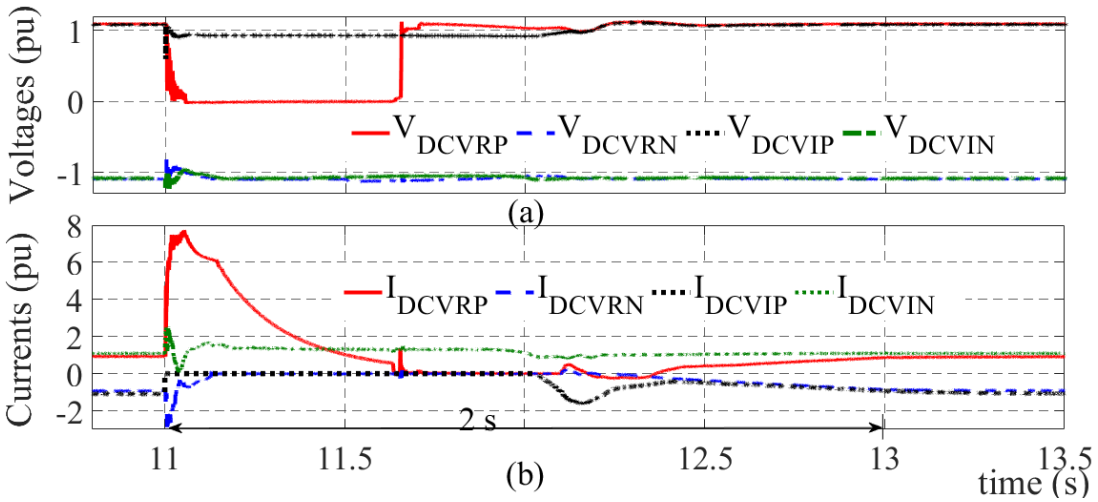


Fig. 4-29. DC side measurements at VSC stations during P-pole to ground faults on Line-B (a) Voltages, (b) Currents (© IEEE)

The low pass filters and the hold circuits in the voltage inputs to the MPC shown **Fig. 4.4** helps to maintain a stable current order during the transient variations in DC voltages. As depicted in **Fig. 4.31**, half of the power is delivered to the healthy pole of the LCC link during the fault.

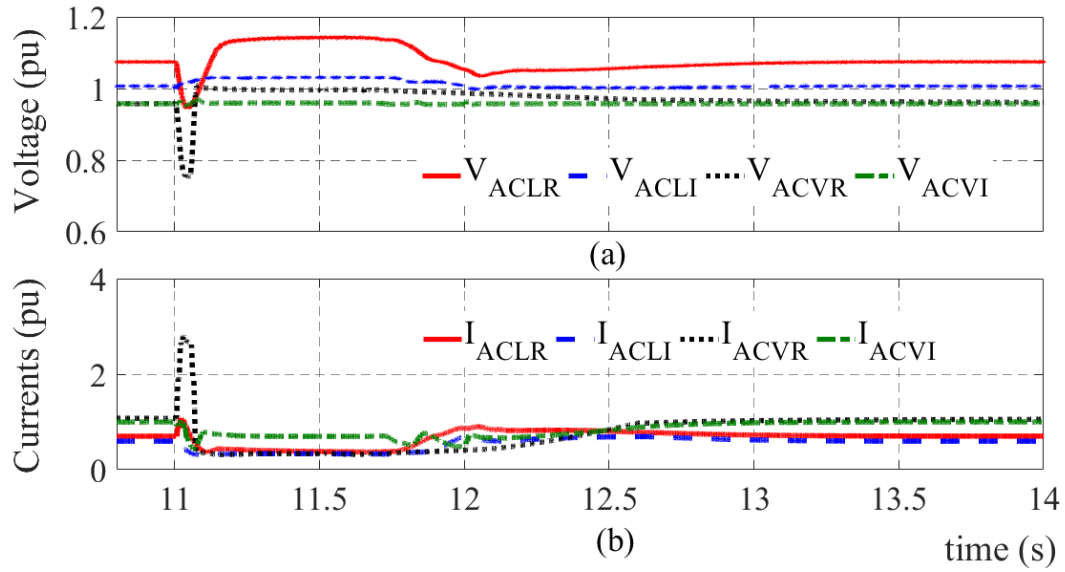


Fig. 4-30. AC side measurements during P-pole-to-ground faults on Line-B (a) Voltages, (b) Currents (© IEEE)

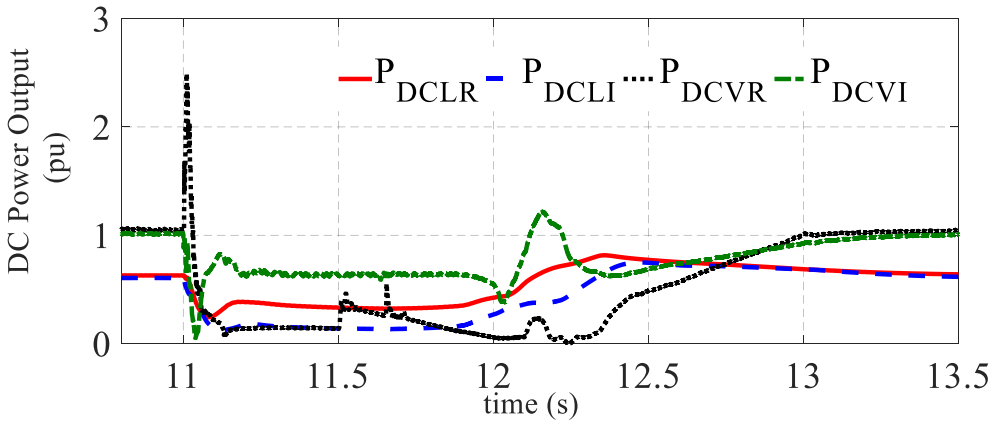


Fig. 4-31. DC power measurements during P-pole-to-ground faults on Line-B (© IEEE)

Fault recovery delays for all fault scenarios are given in **Table 4.3.**

Table 4-3 Comparison of recovery times

Scenario	Config.	T_{FC} (s)	T_{LVR} (s)	T_{LPR} (s)	T_{VAPR} (s)	T_{VBPR} (s)
A	1	0.3	0.7	1.0	2.0	2.0
B	1	0.6	1.1	1.4	2.0	2.0
C	2	0.2	0.4	0.8	1.4	1.8
D	2	0.25	0.4	0.8	1.5	1.8

Where T_{FC} is the fault clearing time, T_{LVR} is the time between the fault and restoration of the LCC link voltage, T_{LPR} is the total time taken to restore power flow in LCC link, T_{VACR} is the total time taken to restore power flow in VSC-A.

4.8.3 Fault Recovery in Configuration-1: Symmetrical Faults

The fault recovery performance of Configuration-1 is evaluated in this section. As it will be shown, Configuration-1, where all VSC terminals operate as inverters, has its own merits when the requirement is only to tap energy from an LCC link. The pole-to-pole fault is on line segment A (**Fig. 4.2**). As depicted in **Fig. 4.32(b)**, the current through LCC rectifier rises from 1pu to 2 pu during the fault. The high rating series diode valves become reverse biased after the fault causes due to the drop in DC voltage.

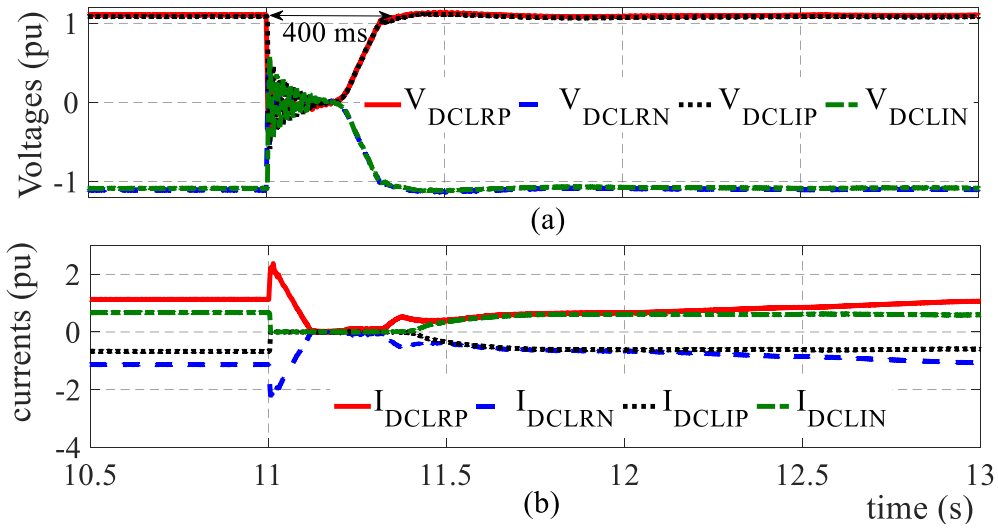


Fig. 4-32. DC side measurements at LCC stations during P-pole to N-pole faults on Line-A (a) Voltages, (b) Currents (© IEEE)

Therefore, the currents through the VSC inverter stations suddenly drop to zero as can be seen in **Fig. 4.33(b).** Note that, for this configuration, any measurements taken at VSC-A and VSC-B are labeled with subscript VA and VB. As depicted in **Table 4.3**, since the fault current contribution from the VSCs is zero in Configuration-1, the fault current can be reduced to a negligible value in less than 200 ms. As a result, the voltage in the LCC link can be restored faster.

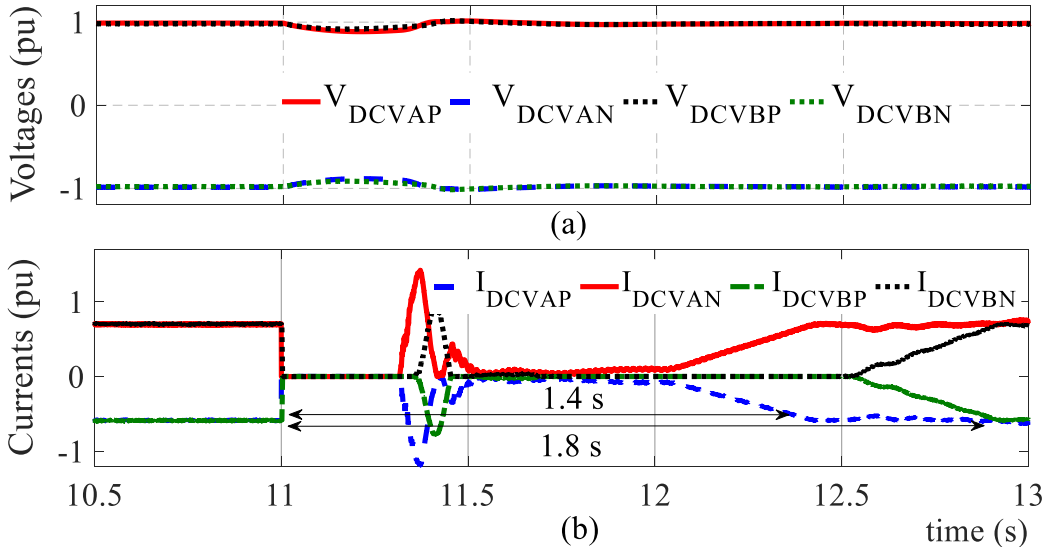


Fig. 4-33. DC side measurements at VSC stations during P-pole-to-N-pole faults on Line-A (a) Voltages, (b) Currents (© IEEE)

As depicted in **Fig. 4.34**, no noticeable rise in AC side current or a drop in AC side voltage is observed in any of the inverter stations. However, as shown in **Fig. 4.34**, a momentary rise of AC current from 1 pu to 2.2 pu and therefore AC side voltage drop to 0.675 pu is observed at the AC system connected to the LCC rectifier.

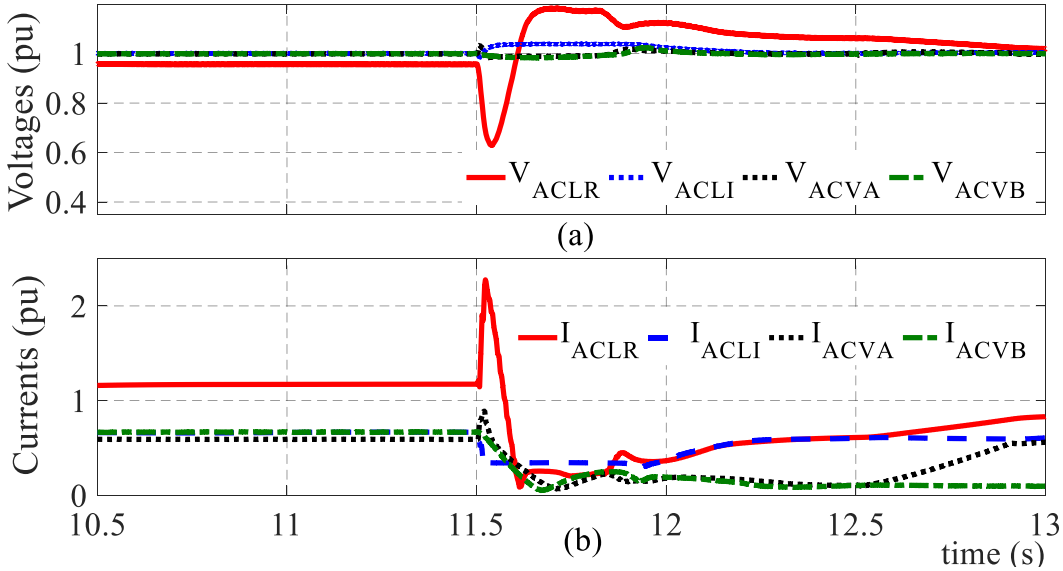


Fig. 4-34. AC side measurements during P-pole to N-pole faults on Line-A (a) Voltages, (b) Currents (© IEEE)

4.8.4 Fault Recovery in Configuration-1: Asymmetrical Faults

Fig. 4.35 and **Fig. 4.36** show the DC side measurements taken at each station during the fault Scenario-D described in **Table 4.2**. A momentary oscillation of current that lasted for a period of less than 0.1 ms is observed at the healthy pole of the LCC link. Furthermore, as depicted in **Fig. 4.36(b)**, an oscillation of power flow between VSC-A and VSC-B is observed for about half a second. Technically, VSCs should not cause any extra impact on the restoration of LCC link to full power in Configuration-1. The series high rating diode valves are very effective in blocking the fault current from VSC inverters. This is visible in simulation results and the voltage recovery of the LCC link to pre-fault status when operating in this mode is very fast.

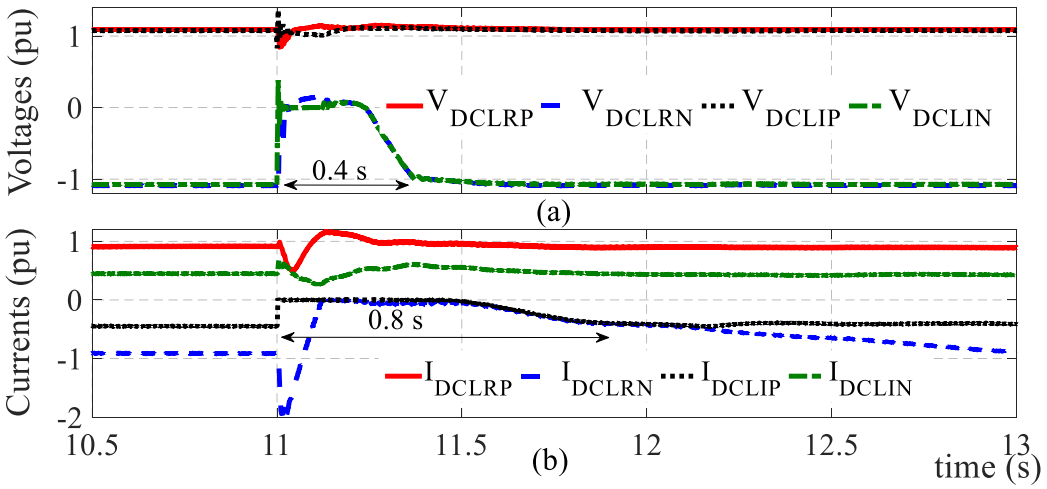


Fig. 4-35. DC side measurements at LCC stations during N-pole-to-ground faults on mainline near LCCI (a) Voltages, (b) Currents (© IEEE)

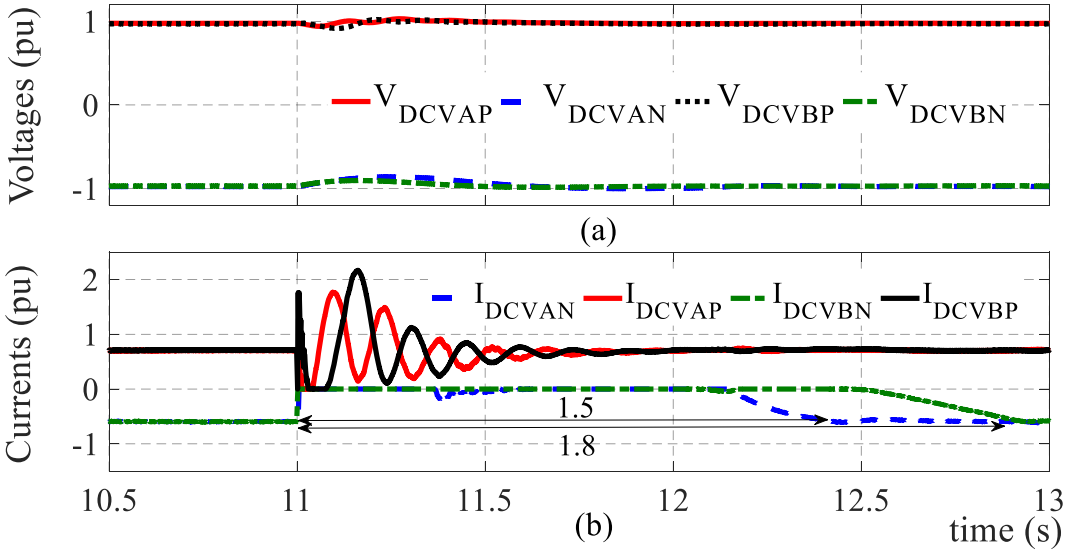


Fig. 4-36. DC side measurements at VSC stations during N-pole-to-ground faults on the mainline near LCCI (a) Voltages, (b) Currents (© IEEE)

In both configurations, clearing of single-pole-to-ground faults take slightly longer time than the clearing time of pole-to-pole faults. The clearing of faults take longer time when operating in Configuration-2, due to fault current contributions from the VSC rectifier.

4.9 Concluding Remarks

A novel LCC-VSC hybrid multi-terminal HVDC transmission structure that can be implemented with proven LCC and half-bridge MMC technologies with a minimum or no changes to low-level control was proposed. The proposed topology has potential advantages in certain applications. The new topology does not demand any changes in controllers of the present converter technologies. The coordination among the converters was achieved through a higher-level master power controller. With the proposed controls and procedures, smooth and safe converter start-up and energization can be achieved, as demonstrated through PSCAD/EMTDC simulations of a detailed model of the multi-terminal hybrid HVDC transmission system and presented in **Section-4.7**. Undisturbed power flow was observed in one converter while changing the power order of the other converter stations. However, a change in power at one inverter station at a time was assumed.

A strategy to clear DC faults utilizing a combination of actions including forced retardation of LCCs, the opening of ACCBs of VSCs and blocking fault currents using protection diodes was proposed. The expected DC fault recovery behavior of the hybrid multi-terminal HVDC system was investigated with an emtp model simulated in PSCAD/EMTDC. The simulation results demonstrated the (i) effectiveness of the proposed procedure for recovering from both pole-to-pole faults and pole-to-ground faults with minimum delay; (ii) the ability of protection diodes to block DC fault currents from VSC inverters without having to open ACCBs.

In the piggy-backing configuration where a common transmission segment is shared by both LCC and VSC HVDC links, the VSC rectifier injects a large initial fault current due to the discharge of MMC cell capacitors. This current decay over several hundreds of milliseconds, even after opening ACCBs, delaying the fault recovery compared to an LCC link. Due to considerable

dip in AC voltage during this initial fault current, the operation of the healthy pole of a VSC is severely affected during single pole-to-ground faults. Therefore, it is suggested to ramp down the power flow through the healthy pole of VSC link to ensure power delivery on the healthy pole of the LCC link.

In the configuration where VSC inverters with protection diodes tapping into the LCC-HVDC link, VSCs do not contribute to the fault current and the recovery performance is similar to that of the LCC-HVDC link. In this configuration, single pole-to-ground faults can be cleared without affecting the healthy pole. The protection diodes need to be rated to withstand transient reverse voltages up to 2 pu during the faults.

In conclusion, the study demonstrates the technical feasibility of the proposed MT-HVDC transmission configuration. It is decided to further investigate the possibility of minimizing the long recovery period in the presence of VSC rectifier with the help of a high voltage DC circuit breaker. The results of the study are presented in the next chapter.

Chapter 5

A Selective Fault Clearing Scheme for Hybrid VSC-LCC Multi-Terminal System using DC Circuit Breakers

5.1 Introduction

The possibility of fast recovery of the main LCC HVDC link from DC side faults using high voltage DC circuit breakers is examined in this Chapter. The fault discrimination and faulted conductor identification algorithms developed in Chapters 2 and 3 are applied to the hybrid LCC-VSC MT-HVDC transmission system considered in Chapter 4 to generate trip signals for the DCCBs. The performance of this new topology is examined through the simulations and the results are presented with comparisons to the method discussed in Chapter 4. The work presented in this chapter is based on the following publications.

[G] M. H. Naushath, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "A Selective Fault Clearing Scheme for a Hybrid VSC-LCC Multi-terminal HVDC Systems," *Energies,* vol. 13, pp. 01-21, July 2020.

5.2 Background and Literature Review

The well-documented weakness of HB-SM MMC station is the very high initial fault current that cannot be stopped by blocking IGBTs [4, 33]. The steady-state component of DC fault current can be interrupted by opening ACCBs, but the stored energy in elements continues to decay through the transmission line resistance for a several hundreds of milliseconds even after the opening of AC side CBs [133]. As demonstrated in Chapter 4, this can prolong the time to extinguish arcing faults. This is in contrast to LCC HVDC systems, which can quickly reduce the DC fault current by applying forced retardation procedure. Therefore, when a hybrid multi-terminal HVDC transmission system is created by tapping an LCC HVDC line using a VSC, DC side fault clearing time tends to increase in comparison to the fault recovery period of the original LCC HVDC link, if the VSC relies on ACCBs to interrupt DC side fault currents [133]. This degradation of fault clearing performance of a hybrid LCC-VSC system can be avoided if high voltage DC circuit breakers (DCCB) are employed for fast selective fault isolation. The recent developments in high voltage DCCB technology include full-scale prototypes and field installations [88, 137]. Technically viable commercial DCCB solutions are expected to emerge in the near future.

Although selective fault clearing in purely VSC based MT-HVDC systems has been an active research area in the recent years [42, 44, 138, 139], the technology is not well established, especially for hybrid LCC-VSC MT-HVDC transmission systems that comprise of multiple zones, and gaps exist in the understanding. In contrast to the DC fault clearing approach proposed in Chapter 4, a selective fault clearing scheme needs a fault detection and discrimination scheme suitable for hybrid LCC-VSC multi-terminal systems having multiple protection zones.

Furthermore, without having a complete protection scheme that discriminates the faults in different zones and a fault recovery scheme that invokes appropriate actions depending on the faulted zone and fault type, the potential fault recovery performances cannot be evaluated. The fault discrimination scheme should be capable of discriminating faults at each zone, up-to a fair value of fault resistance expected in a typical hybrid LCC-VSC based multi-terminal system. In addition, the fault discrimination should be able to make decisions within an extremely short duration dictated by the DCCB limitations. This is because a DCCB has to interrupt the rapidly rising fault currents before they exceed the maximum breakable current. The fault current injected through a VSC branch could reach its peak value within a couple of milliseconds. Therefore, the fault discrimination speed of the schemes such as the one presented in [139], which needs 5 ms time window, may not be adequate with respect to the typical DCCB performance cited in the literature [65, 88].

This chapter examines the fault discrimination, DCCB assisted fault clearing, and the post-fault recovery performance of the hybrid LCC-VSC MT-HVDC scheme presented in Chapter 4 in a holistic manner.

5.3 Protection Design

Fig. 5.1 shows the considered MT-HVDC transmission system layout and the essential elements of the proposed protection scheme. The two VSC stations with lower ratings compared to the LCC stations are connected through short transmission lines, which are referred to as VSC branches, to a 1400 km long main transmission line. This is a more generic and challenging configuration, but the method is applicable to a system with zero-length VSC branches, where the DCCB is located in a VSC station adjacent to the LCC link. A bipole HVDC transmissions system

without a DMR conductor similar to Manitoba Bipole-I or -II [122] is considered. It is assumed that earth return mode is allowed for a short period for single-pole fault recovery. The VSC stations are assumed to be based on more economical HB-SM technology.

A key requirement is to ensure that the reliability of the original LCC line is not degraded due to tapping. In order to avoid the prolong fault clearing and recovery time for temporary DC faults, all HB-SM based MMCs on the affected pole(s) must be immediately disconnected from the DC network. Also, during all permanent faults on the VSC branches, the faulted line segment must be disconnected before the stability of the LCC link is affected. This is only possible by using DCCBs for selective fault isolation. In order to maximize the fault recovery performance with a minimum number of DCCBs (which are high cost items), it is proposed to place a DCCB at each tapping point on VSC branches. In this configuration, the DCCBs perform two main roles.

1. For both temporary and permanent faults on the VSC branches: Avoid the impact on LCC link by promptly disconnecting faulty conductor(s) from the main LCC link.
2. For temporary faults on the main LCC link: Avoid the need for a complete shutdown and restarting of VSC stations by promptly disconnecting faulty conductor(s) from the VSCs. The VSCs that are connected to the faulty pole(s) could be switched to STATCOM (static synchronous compensation) mode till the fault on mainline is cleared.

It is necessary to have DCCBs on both poles to perform the above roles. With this arrangement, a VSC station connected to the faulted pole(s) is completely de-energized for all faults on the line segment connecting it to the main LCC link. De-energization of a VSC during temporary faults can be avoided by providing additional DCCBs at the VSC terminals. However, this is an expensive solution with an only marginal contribution to improve the reliability or the safety of the system:

1. As there is no alternative path for power transfer during a VSC branch fault in the considered layout, isolation of the faulty conductor to preserve the continuity of VSC operation is not offering any important advantage.
2. The converter has its own low level protection such as blocking IGBTs upon detecting a fault and protecting freewheeling diode by firing parallel thyristors [136].

The possibility of using DCCBs on the main LCC line to improve the reliability is not considered as the LCCs are capable of blocking fault currents. Also, in order to minimize the cost, the number and capacity of the required DCCBs should be selected carefully. Based on the above reasoning, DCCB placement shown in **Fig. 5.1** is considered as the arrangement that needs the least number of dc CBs for the proposed hybrid LCC-VSC multi-terminal HVDC topology, and it divides the dc network in to three protection zones. In order to apply this scheme, it is necessary to discriminate against the faults on the main transmission line (Zone-M) from those on the branches connecting VSC-A (Zone-A), and VSC-B (Zone-B); and identify the pole(s) involved in the fault. An intelligent electronics device (IED) capable of the above tasks can be implemented at each tapping point as indicated in **Fig 5.1**, with the help of series di/dt limiting inductors that comes as an integral part of DCCBs [141-143]. The protection IED-A at the tapping point-A comprises of two functional units: one denoted as IED-AM to detect faults on the mainline, and the other denoted as IED-AI to detect faults on the line connecting the VSC. A similar protection IED is employed at the tapping point B as well. Coordination of the converter stations in this multi-terminal transmission system is important for stable normal operation and fault recovery. The centralized master power controller proposed in Chapter 4 is considered in this study. Transmission system energization and co-ordination is assumed to be carried as in Chapter 4, in which the LCC inverter is operated under constant extinction angle control mode controlling the

DC voltage, while VSC stations are operated under constant power control mode during normal operation. LCC rectifier is operated under constant current control mode.

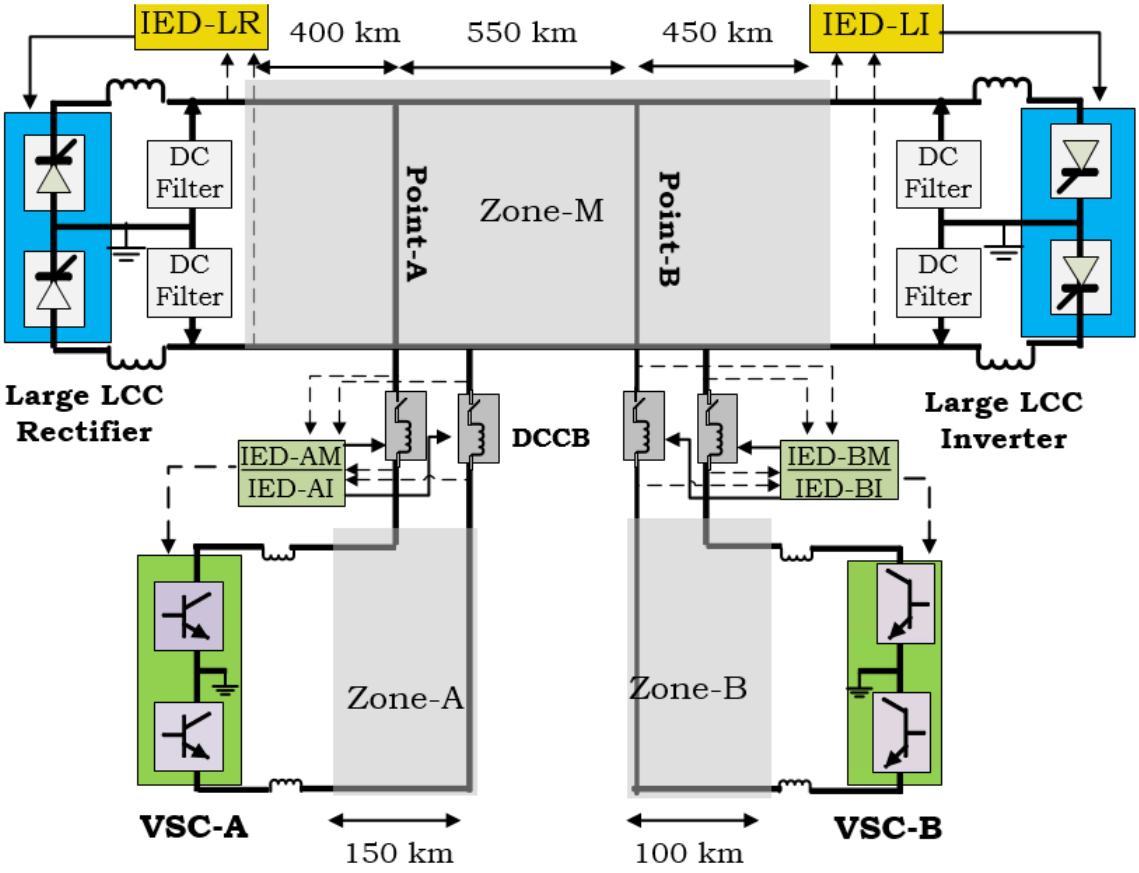


Fig. 5-1. Hybrid LCC-VSC transmission system with two VSCs connected to an LCC-HVDC link

The primary function of the MPC is to calculate the current order for the LCC rectifier to fulfil power demand at the LCC inverter while considering the instantaneous current injections from each VSC station. For example, the current order for P-pole is calculated using (5.1), which is a slightly modified version of (4.1).

$$I_{O\_P} = S_{LIP}\left[\frac{R_{LI}\cdot P_{ref_{LIP}}}{V`_{DCLIP} - V`_{DCLIN}} + \frac{S_{VAP}\cdot R_{VA}\cdot P_{ref_{VAP}}}{V`_{DCVAP} - V`_{DCVAN}} + \frac{S_{VBP}\cdot R_{VB}\cdot P_{ref\_VBP}}{V`_{DCVBP} - V`_{DCVBN}}\right] \quad (5.1)$$

where, $P_{ref\_LIP}, P_{ref\_VAP}, P_{ref\_VBP}$ are power reference values, and R_{LI}, R_{VA}, R_{VB} are ramping rates of the LCC inverter, VSC-A, and VSC-B respectively. The binary signals S_{LIP}, S_{VAP}, and S_{VBP} are

generated by a fault recovery supervisory function to reset the respective current component to zero after detecting a fault on P-pole conductor connected to the LCC inverter, VSC-A, and VSC-B respectively. $V`_{DCLIP}$, $V`_{DCLIN}$, $V`_{DCVAP}$, $V`_{DCVAN}$, $V`_{DCVAP}$, and $V`_{DCVBN}$ are conditioned pole voltage measurements taken through the signal pre-processing arrangement shown in **Fig. 4.4**. This includes a hold circuit which holds the pre-fault voltage measurement during the fault recovery period and a first-order filter with 200 ms time constant to avoid erratic current orders due to low DC voltages that may occur during faults.

Note that (5.1) is derived by modifying (4.1) to take in to account that the LCC rectifier current is zero when S_{LIP}=0 during a fault on Zone-M. According to (5.1), the current order is set to zero during a fault on Zone-M by setting S_{LIP}=0. During a fault on a VSC branch, the respective term is set to zero via S_{VAP} and S_{VBP}. During a single-pole fault, the healthy pole current order is frozen at the pre-fault value until recovery. The current order for N-pole is calculated independently in the same manner.

5.4 Proposed Selective Fault Isolation Scheme

In this section, a selective fault isolation scheme is proposed for a hybrid HVDC multi-terminal containing the elements shown in **Fig. 5.1** and a centralized MPC similar to the one described in **Section-4.3.2**.

5.4.1 DC Side Fault Clearing Strategy

The DC side fault clearing involves functions such as opening and reclosing the DCCB, applying force retardation at the LCC rectifier, de-energizing or re-energizing of the VSC stations, etc. However, unlike the scheme described in **Chapter 4**, the set of actions activated in the

proposed scheme is different for the faults on the VSC branches and the faults on the mainline. The proposed fault clearing procedure is shown in **Fig. 5.2**. Similar to the approach presented in **Chapter 4**, in order to preserve the operation of the healthy pole during single-pole-to-ground faults, the fault recovery process is applied independently for positive and negative poles. As depicted in **Fig. 5.2(a)**, upon detecting a fault in Zone-M, force retardation is applied to the respective pole(s) of the LCC rectifier. For example, if only P-pole is involved in the fault, S_{LIP} in Equation (1) is reset (S_{LIP}=0) to notify the MPC of the cease of power transmission in P-pole. After a fixed time delay of T_{FR}, which should be carefully selected by considering the worst case, the force retardation is released. If the voltage is recovering, S_{LIP} is set (S_{LIP}=1) again and the firing angle of the LCC rectifier is gradually decreased to its pre-fault value. If the voltage does not recover in three attempts, the fault is declared as a permanent fault and the operation of LCC is stopped. As depicted in **Fig. 5.2(b)**, for a fault on the main transmission line, the DCCB of each faulted pole is disconnected immediately. Then the operating mode of the faulted poles of the VSC stations are changed to DC side voltage control mode till the fault is cleared. For a fault on a VSC branch, say on Zone-A as depicted in **Fig. 5.2(b)**, the relevant DCCBs (DCCB on P-pole, N-pole or both) are immediately opened to isolate the faulted pole(s) from the main transmission line. The IGBTs of the faulted pole of VSC-A (say P-pole) are immediately blocked by the converter internal protection. Subsequently the faulted pole, P-pole in this case, is de-energized by opening the corresponding ACCB, and the MPC is notified about the de-energization by resetting S_{VAP} (S_{VAP}=0). Before enabling the reclose operation, a fixed delay of T_{RC1} is allowed to rule out the possibility that the fault is permanent because reclosing onto a fault is hazardous to converter IGBTs. This safety check may require communicating with protection IEDs [144-146]. Therefore communication delays should be taken into account in setting T_{RC1}.

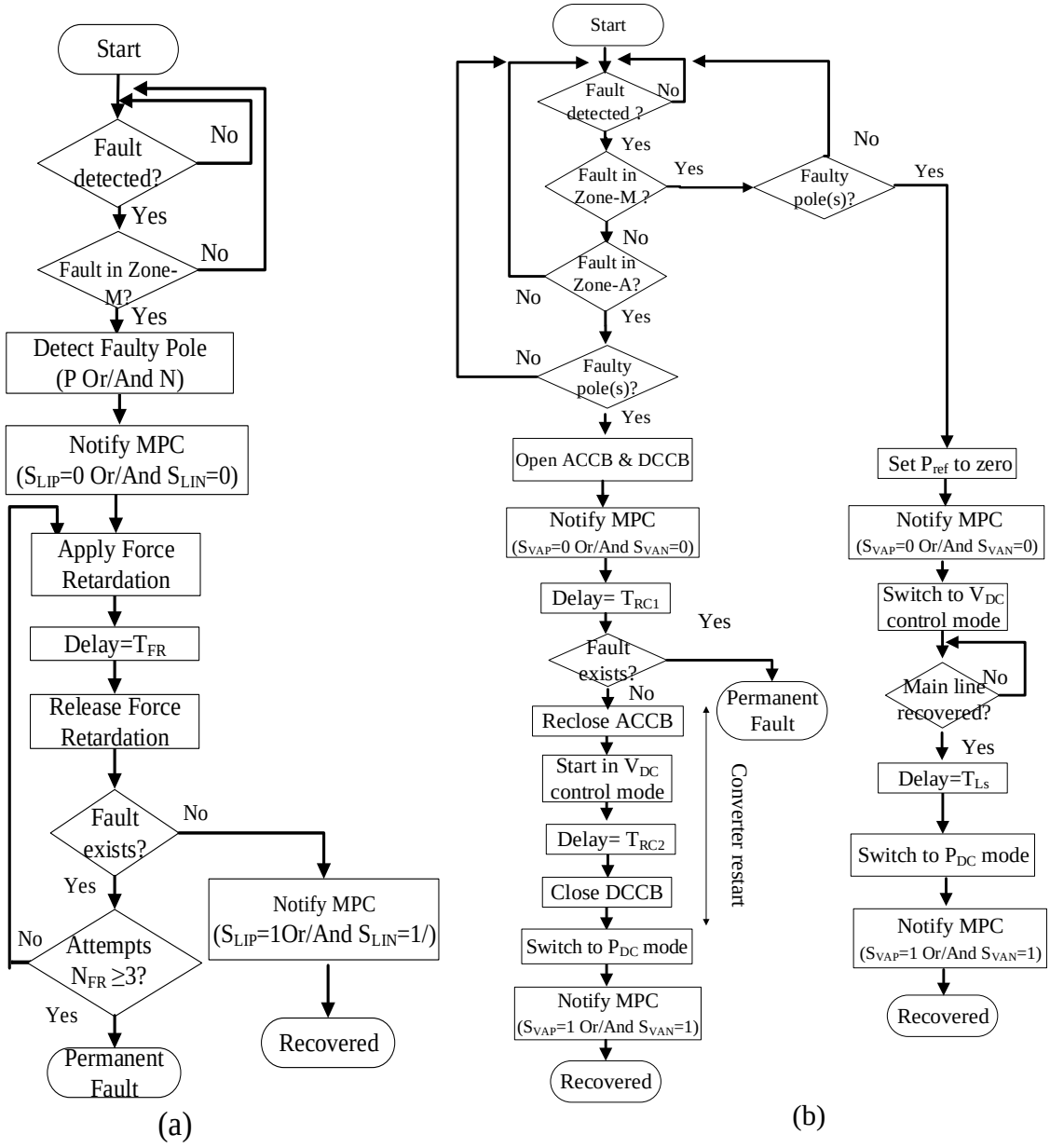


Fig. 5-2. Fault recovery process, (a) at LCC rectifier station, (b) at VSC-A station (the same procedure is used at VSC-B station)

If the fault has been cleared, ACCB is reclosed and the operating mode of the relevant pole of VSC-A is changed from STATCOM mode to voltage control mode.Thereafter, MPC is notified by setting S_{VAP} (S_{VAP}=1) back to its normal value. The operating mode of P-pole of VSC-A is changed to P_{DC} control mode and the pre-fault power reference is re-established. The same process

is applied to N-pole or both poles of VSC-A depending on the fault type. The same procedure is applicable to VSC-B for faults on Zone-B. Details of the energization procedure of MT-HVDC transmission system were described in Chapter 4.

5.4.2 Faulty Line and Faulty Pole Selection Algorithm

As a breaker must isolate only the faulty pole(s) of the transmission line segment involved in the fault (protection zone), a highly secure fault discrimination strategy is important to achieve the desired improvement of reliability. The DCCBs separate the different protection zones and are associated with di/dt limiting inductors as shown in **Fig. 5.1.** These inductors are referred to as the boundary inductors due to their location at the boundaries of adjacent protection zones. Due to the existence of a boundary inductor between the main line and a VSC branch, during a fault on the main line, the maximum rate of change of voltage (ROCOV) observed at any terminal of the main line is considerably higher than the maximum ROCOV observed on any terminal of a VSC branch [42, 103]. The opposite is true during a fault on a VSC branch. This enables discrimination of faults and therefore maximum ROCOV is selected as the main fault indicator [42, 108]. The sensitivity of ROCOV based fault discrimination is improved by incorporating the directional logic presented in **Chapter 2** and using the aerial voltage components. The directional logic is employed only on IEDs -AM, -AI, -BM, and -BI. The directional logic is not relevant for IED-LR and IED-LI, since there are no other dc protection zones behind them. The faulty pole is identified using the logic described in **Chapter 3**. The proposed fault discrimination algorithm with combined features is shown in **Fig. 5.3**. The algorithm is run on an IED located at the boundary of a protected line. An IED takes voltage measurements at either side of the boundary inductors of P- and N-poles, and the currents through the inductors on both poles as inputs.

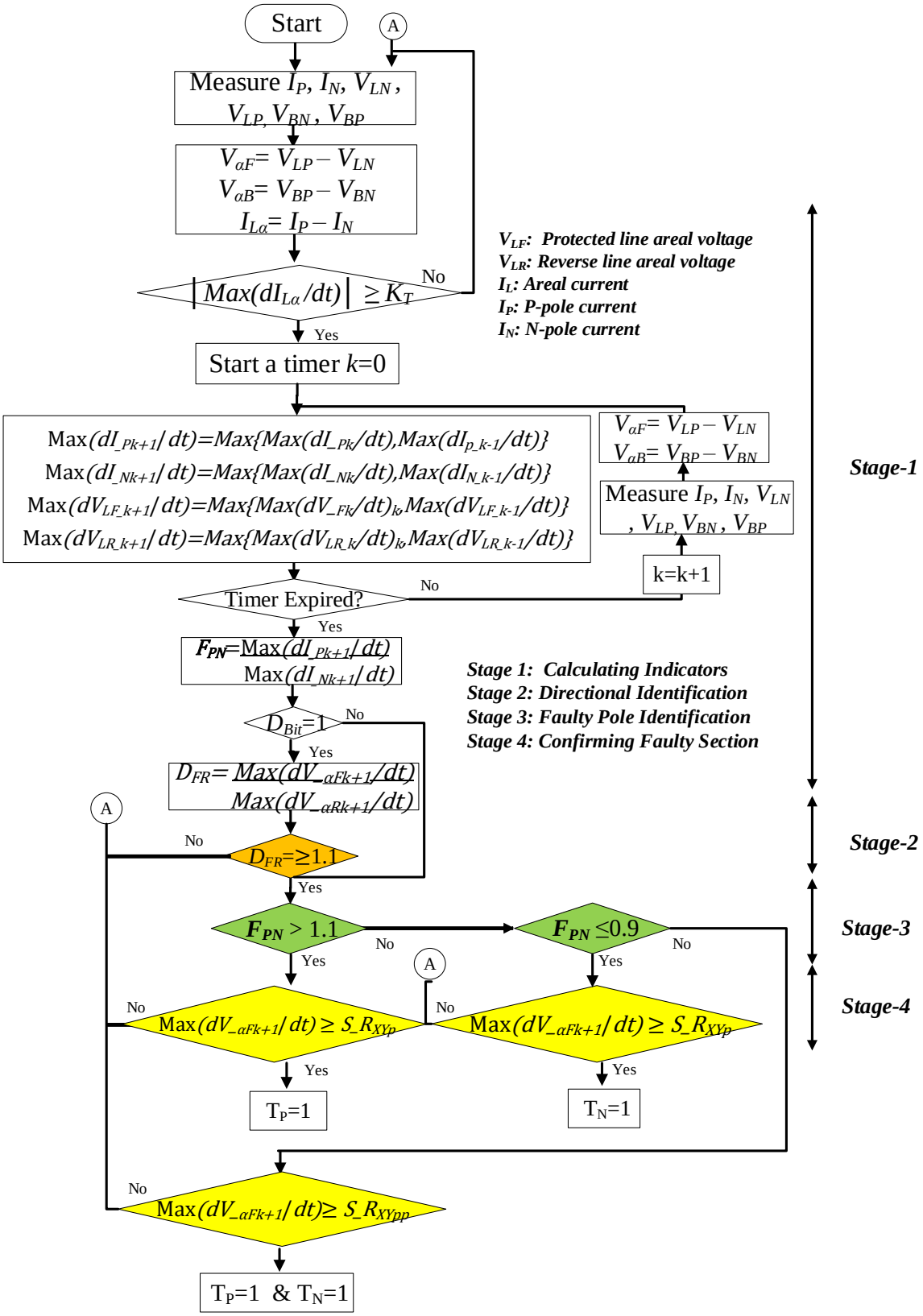


Fig. 5-3. Fault discrimination algorithm

V_{LN}, V_{LP}, are respectively N-pole and P-pole voltages on line side of the boundary inductors and V_{BN}, V_{BP} are N-pole and P-pole voltages of the bus side of the boundary inductors. It then extracts the aerial components of the input voltages and the currents: $V_{L\alpha}(= V_{LP} - V_{LN})$, the aerial component of the voltages at the line side of boundary inductors, $V_{B\alpha}(= V_{BP} - V_{BN})$, the aerial component of the voltages at the bus side of the boundary inductors, and $I_{L\alpha}(= I_P - I_N)$, the aerial component of the current. The currents I_P and I_N are respectively the currents through the P-pole and the N-pole.

The algorithm is triggered when any of the observed rate of change of current (ROCOC) value is greater than the threshold K_T. The maximum values of ROCOV and ROCOC are tracked over a short time window, and the respective maximum values observed at the end of the time window are sent to calculate the fault discrimination indices.Two indices, D_{FR} and F_{PN}, are calculated using the maximum values of ROCOV and ROCOC.

$$D_{FR} = \frac{\text{Max}(dV_{L\alpha}/dt)}{\text{Max}(dV_{B\alpha}/dt)} \tag{5.2}$$

$$F_{PN} = \frac{\text{Max}(dI_P/dt)}{\text{Max}(dI_N/dt)} \tag{5.3}$$

If D_{FR} is greater than a pre-set threshold ($D_{FR} > 1+\varepsilon$), the fault is declared to be on the forward side [103]. The faulty poles are identified by considering the fact that index F_{PN} is close to unity for pole-to-pole faults ($1+\varepsilon > F_{PN} \geq 1-\varepsilon$), considerably greater than unity for P-pole-to-ground faults ($F_{PN} > 1+\varepsilon$), and considerably less than unity for N-pole-to-ground faults ($1-\varepsilon > F_{PN}$) [112]. Where, ε is a positive tolerance value.

Once the fault type is identified, depending on whether the fault is a single-pole fault or a pole-to-pole fault, the maximum rate of change of $V_{\alpha F}$ is compared with a threshold (S_R_{XYp} for

pole-to-ground and S_R_{XYpp} for pole-to-pole) to determine whether the fault is within the protected line.

5.5 Test System

The test system described in **Section-4.6,** the configuration and protection design are shown in **Fig. 5.1,** was used to evaluate the performances of the fault recovery scheme with the following additions and revisions.

The DCCBs were considered to have a 2 ms operating delay and a 6 kA maximum breaking current. The series inductors placed at each pole of the VSC stations and in series with DCCBs were assumed to be 60 mH. IGBTs are blocked when the current through any arm increased beyond 3 pu and for longer than 20 μs. Fault recovery performances were evaluated when the LCC inverter is receiving 600 MW/pole, VSC-A is injecting 200 MW/pole, and VSC-B is receiving 200 MW/pole. After recovering from a temporary fault, each converter is returned to its pre-fault operating state.

5.5.1 Relay Settings

The single-pole-to-ground fault ROCOV threshold setting, S_R_{XY}, was calculated as in (5.4).

$$S\_R_{XYp} = \frac{1}{2}\left(ROCOV_{pMx\_A} + ROCOV_{pMx\_B}\right) \tag{5.4}$$

where $ROCOV_{pMx\_B}$ is the observed maximum ROCOV value for a high resistance single-pole-to-ground fault at the far end of the protected transmission line. $ROCOV_{pMx\_A}$ is the observed maximum ROCOV for a single-pole-to-ground short circuit fault in the forward direction, just outside the protected zone. Since the zone boundary is demarcated by the terminal inductor, the

maximum ROCOV value are measured at either side of the terminal inductor at the far end of the line. The expected maximum fault resistance to be detected should be selected by considering the constraint $ROCOV_{pMx\_B} > ROCOV_{pMx\_A}$. The pole-to-pole settings were calculated in a similar manner by considering the pole-to-pole faults instead of the single-pole-to-ground faults. The setting S_R_{XYpp} for pole-to-pole faults is greater than the threshold settings for single-pole faults, S_R_{XYp}. **Table 5.1** shows the maximum ROCOV values used to determine the settings S_R_{XYpp} and S_R_{XYp}. The maximum ROCOV settings of the protection IEDs, S_R_{XYpp} and S_R_{XYp}, are given in **Table 5.2**.

Table 5-1 Maximum ROCOV values used with (5.4)

IED	$\mathbf{ROCOV_{ppMx\_A}}$ (kV/ms)	$\mathbf{ROCOV_{ppMx\_B}}$ (kV/ms)	$\mathbf{ROCOV_{pMx\_A}}$ (kV/ms)	$\mathbf{ROCOV_{pMx\_B}}$ (kV/ms)
IDE-LR	2230	3028	971	1077
IDE-LI	1413	2903	586	1068
IDE-AM	1394	3759	538	1346
IDE-BM	2019	3932	875	1538

Table 5-2 IED Settings

IED	$\boldsymbol{S\_R_{XYpp}}$ (kV/ms)	$\boldsymbol{S\_R_{XYp}}$ (kV/ms)	IED	$\boldsymbol{S\_R_{XYpp}}$ (kV/ms)	$\boldsymbol{S\_R_{XYp}}$ (kV/ms)
IED-LR	2630	1023	IED-BM	2975	1206
IED-LI	2158	827	IED-AI	8518	3542
IED-AM	2576	942	IED-BI	8838	3663

The threshold settings for the directional discrimination index, D_{FR}, and the faulty pole(s) identification index, F_{PN}, were selected considering a 10% tolerance and common for all IEDs. The ideal value for these two indices is 1, and the 10% tolerance provides an added security. Based

on the simulation studies, the fault detection threshold parameter K_T is set to 2 kA/ms and the time window for computing the maximum ROCOC and ROCOV values, T_{w-max}, was set to 0.5 ms. This is the expiry time of the timer shown in **Fig. 5.3.** When selecting the time delay, T_{RC1}, the expected maximum fault clearing time and the time to run an appropriate checking mechanism to determine whether a fault on a VSC branch is permanent or not should be considered. The discrimination between a temporary arc fault and a permanent fault can be done in two ways in this application. The extinction of a temporary arc can be confirmed by looking at the reflected wave after injecting an active signal with the help of VSC, as proposed in [147-148]. Alternatively, temporary faults can be discriminated against the permanent faults with the help of residual voltage characteristics of DCCBs at the tapping point as proposed in [144-146]. According to [144, 146], the temporary faults can be discriminated from the permanent faults within a several tens of mille-seconds. Assuming the confirmation of extinction of fault is done at the DCCB, the time required assess and to inform the converter station are considered. The communication delay is estimated assuming that the velocity of signal propagation is 150 km/ms. The time delay, T_{del}, for communication between two entities separated by l km distance, is approximated by (5.5).

$$T_{del} = \frac{l}{150} + 1\ ms \tag{5.5}$$

The time delay T_{RC1} shown in **Fig. 5.2(b)** is set to 362 ms by considering a 330 ms duration for extinction of the temporary fault, a 30 ms worst-case delay for confirmation of the extinction of the temporary fault, and 2 ms communication delay. The time delay T_{FR} shown in **Fig. 5.2(a)** is set to 150 ms. The delay T_{RC2} is the time delay to settle the VSC-A terminal voltage once it is re-started in DC voltage control mode by de-blocking the IGBT after re-closing AC circuit breakers. T_{RC2} is set to 50ms.

5.6 Validation of Fault Discrimination Scheme

The fault discrimination scheme presented in **Section-5.4.2** is validated using the test system described in **Section-5.5**.

5.6.1 The Capability of Discriminating Faults on the Mainline

Determination of the fault direction using the calculated value of D_{FR} at IED-A is demonstrated in **Fig. 5.4** for faults inside Zone-M and Zone-A. To avoid the ambiguity of having two curves for the same location, the distance to the fault is measured from the LCC rectifier end. The label 0.1ΩP→G@M indicates a P-pole-to-ground fault inside Zone-M simulated with a 0.1Ω fault resistance and 0.1ΩP→N@M indicates a P-pole-to-N-pole fault with a 0.1 Ω fault resistance.

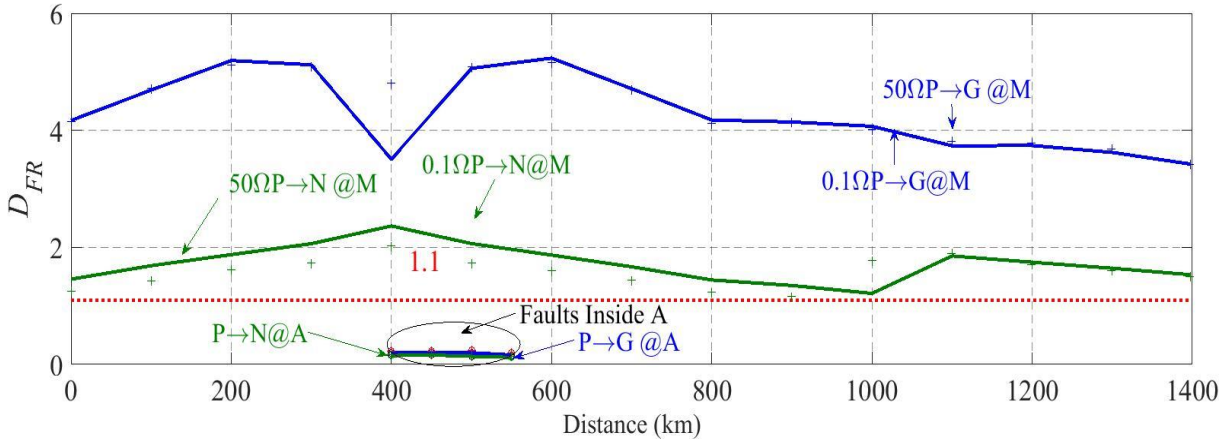


Fig. 5-4. Calculated D_{FR} at IED-AM for faults inside Zone-M and Zone-A

The same convention is used for 50 Ω faults. The respective threshold is also indicated on the graphs. As depicted in **Fig. 5.4**, the minimum calculated D_{FR} for the faults inside Zone-M is 1.2 whereas the highest calculated value of D_{FR} for faults inside Zone-A is 0.24. Therefore, as per the directional criterion depicted in **Fig. 5.3**, any fault inside Zone-A is discriminated against reverse faults at IED-AM while any fault inside Zone-M is declared as a fault in the forward

direction. As depicted in **Fig. 5.5(a)** and **5.5(b)**, pole(s) involved in the fault can be recognized with the help of faulty pole(s) identification criterion applied at IED-LR at LCC rectifier and IED-AM at tapping point-A. As depicted in **Fig. 5.5(a)**, pole(s) involved in the fault can be identified using F_{PN} with an adequate margin even though the transmission line is very long. Similar observations were made for the protection IED located near the LCC inverter.

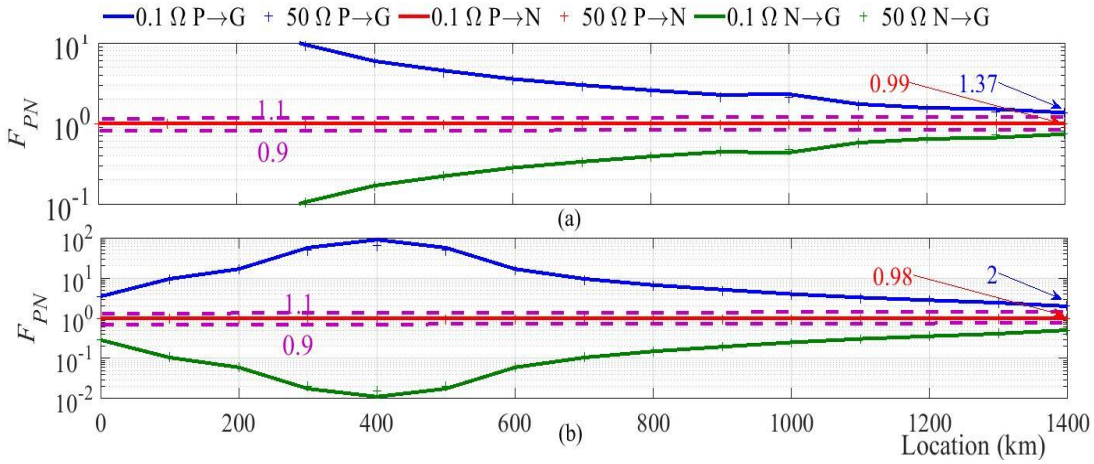


Fig. 5-5. Calculated F_{PN} for faults in Zone-M (a) At IED-LR, (b) At IED-AM

All P-pole-to-N-pole faults resulted in F_{PN} values between the thresholds 0.9 and 1.1; F_{PN} values for all P-pole-to-ground faults are above 1.1; and F_{PN} values for all N-pole-to-ground faults are below 0.9. Similar observations were made for the protection IEDs located near the LCC inverter and Point-B. The minimum margin of discrimination of faulty pole(s) at IED-A is 82%, and despite the extreme line length, IED-LR manages to recognize the faulty pole even for remote faults. As depicted in **Fig. 5.6(a)** and **Fig. 5.6(b)**, the maximum ROCOV is greater than the respective thresholds up to a fault resistance of 50 Ω. The discrimination margin for end of line faults is higher for pole-to-pole faults (15%) when compared with the single pole-to-ground faults (5%). The margin is calculated using (5.6)

$$(ROCOV_{pMx\_B} - S\_R_{XYp}) \text{ x } 100 / S\_R_{XYp} \quad (5.6)$$

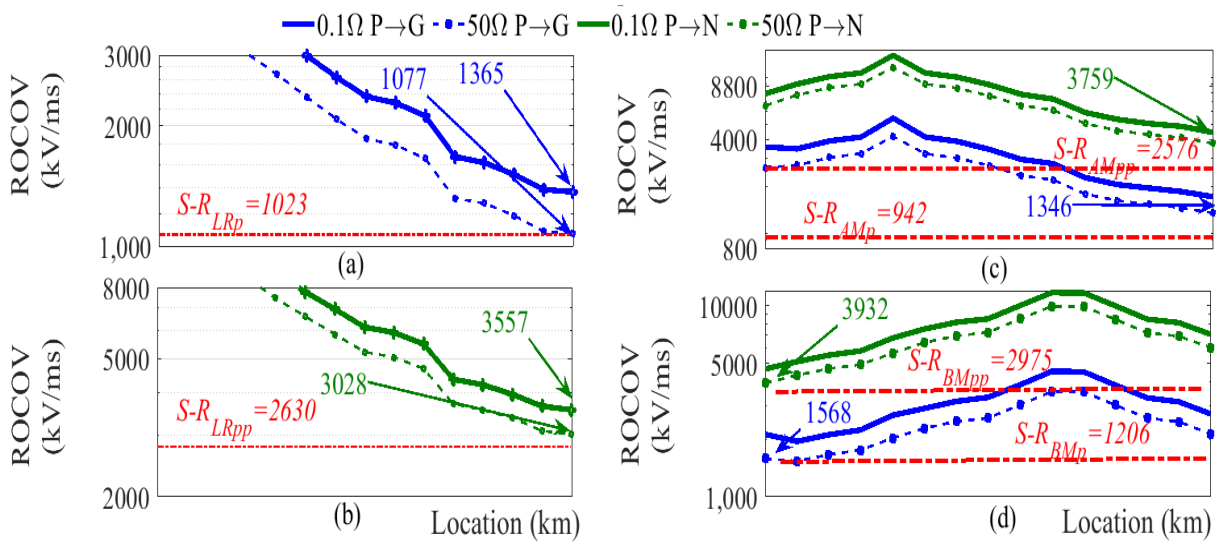


Fig. 5-6. Calculated maximum ROCOV values (a) At IED-LR for P→G faults, (b) At IED-LR for P→N faults, (c) At IED_AM, (d) At IED-BM

If higher margin is desired for single-pole-to-ground faults, the highest fault resistance considered for calculating the threshold setting in (5.4) can be lowered, leaving high resistance faults at the end of the transmission line to be dealt using a transfer trip scheme or a line differential type backup protection scheme. Clearing time is not critical for such faults as the current rises slower and the peak fault current is lower for remote high resistance faults. Furthermore, as depicted in **Fig. 5.6(c)**, the faulty section can be identified using the maximum ROCOV criterion with ample margin for both pole-to-pole (46%) and single-pole-to-ground (43%) faults at IDE-AM. The variation of Maximum ROCOV for N-pole-to-ground faults is similar to that of P-pole-to-ground faults.

Therefore, the results presented in **Figs. 5.4-5.6** confirm the ability of protection IEDs located at LCC stations and tapping points to identify any fault in Zone-M having a resistance up to 50Ω, and the pole(s) involved. Furthermore, settings calculated using (5.4) avoids false tripping for any fault in the forward direction beyond the protected zones.

The results shown in **Table 5.3** confirm the capability of IED at the tapping point to detect and discriminate the faults on Zone-A using the proposed fault discrimination criteria. In **Table 5.3**, distance to the fault is measured from the IED. The fourth and fifth columns indicate maximum ROCOV value for metallic fault and for a 50 Ω fault at the specified location. The first two faults cause higher maximum ROCOV than the threshold S_R_{AIp}, 3542 kV/ms, and the last two fault scenarios cause higher maximum ROCOV than S_R_{AIpp} , 8578 kV/ms. According to the fifth column, all the faults are identified as in the right direction.

Table 5-3 Identifying faults in Zone-A at IED-AI

Loc. (km)	**Fault type**	$ROCOV_{Max1}$ (kV/ms)	$ROCOV_{Max2}$ (kV/ms)	D_{FR}	F_{PN}
100	P→G	7393	5797	9.5	11.9
50	P→G	8518	6682	10.4	56.6
100	P→N	19035	16030	9.4	1
50	P→N	22053	18718	10.4	1

The pole(s) involved in the faults are also accurately identified for considered all fault scenarios with the help of calculated values for F_{PN}.

5.7 Validation of Fault Clearing Performance

In the following simulation studies, a temporary metallic fault was considered and the fault was assumed to be self-cleared when the current through the fault falls below 0.1kA. The fault recovery sub-functions were initiated at the respective locations with the help of fault information predicted by the fault discrimination approach described in **Section-5.4.2**. Fault recovery

performances are demonstrated for symmetrical and asymmetrical faults on the main transmission line and VSC branches which are listed in **Table 5.4**. For each fault scenario, similar to **Section-4.8**, simulation-based predictions are presented in a separate section.

Table 5-4 Demonstrated fault scenarios

Scenario	Fault	
	Type	Location
A	P→N	Line-M @ 100 km from LCCR
B	P→G	Line-M @ 700 km from LCCR
C	P→N	Line-A @ 50 km from VSC-A
D	N→G	Line-A @ 50 km from VSC-A

5.7.1 Clearing Temporary Faults on the Main Line

5.7.1.1. Pole-to-Pole Faults

Figs. 5.7 and **5.8** show the DC voltages and currents observed at VSC stations and LCC stations during a P-pole-to-N-pole fault on the mainline, 100 km away from the LCC rectifier (Scenario-A). According to **Fig. 5.7**, the fault currents through VSC rectifiers rapidly rose after the fault, until the DCCBs were opened as per the procedure described in the flowchart of **Fig. 5.2(b)**. Operation of the DCCBs quickly eliminated the fault current contributions from the VSCs and enabled clearing of this temporary fault through force retardation of LCCs. This can be seen from **Fig. 5.8**. Moreover, **Fig. 5.7** shows that both VSCs managed to hold the DC voltage operating in the DC voltage control mode, fulfilling the requirement II listed in **Section-5.3**, and quick reconnect to the mainline after its restoration.

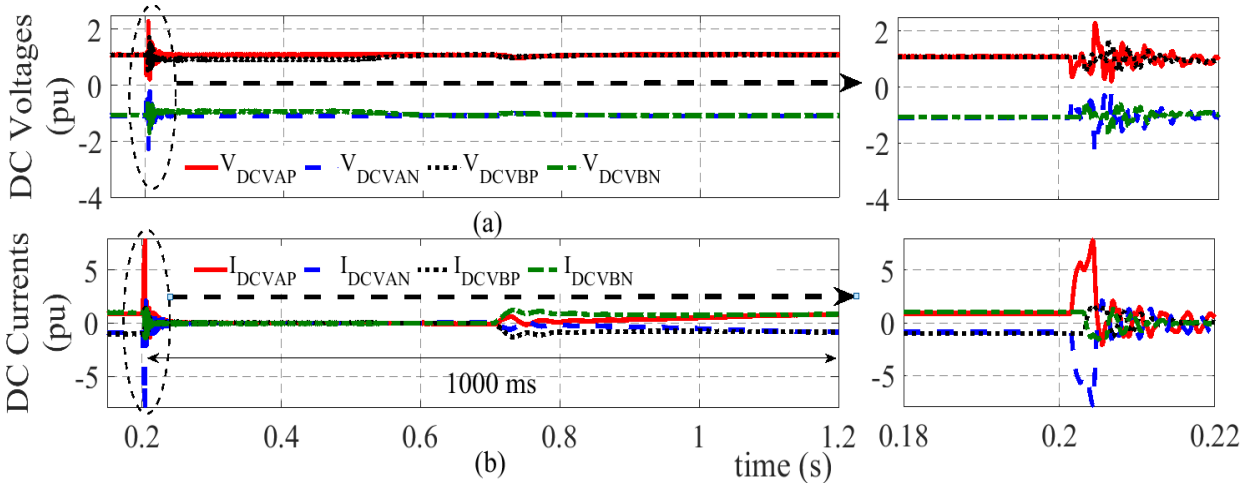


Fig. 5-7. DC side measurements at VSC stations for a P-Pole-to-N-Pole fault on main line (a) Voltages, (b) Currents

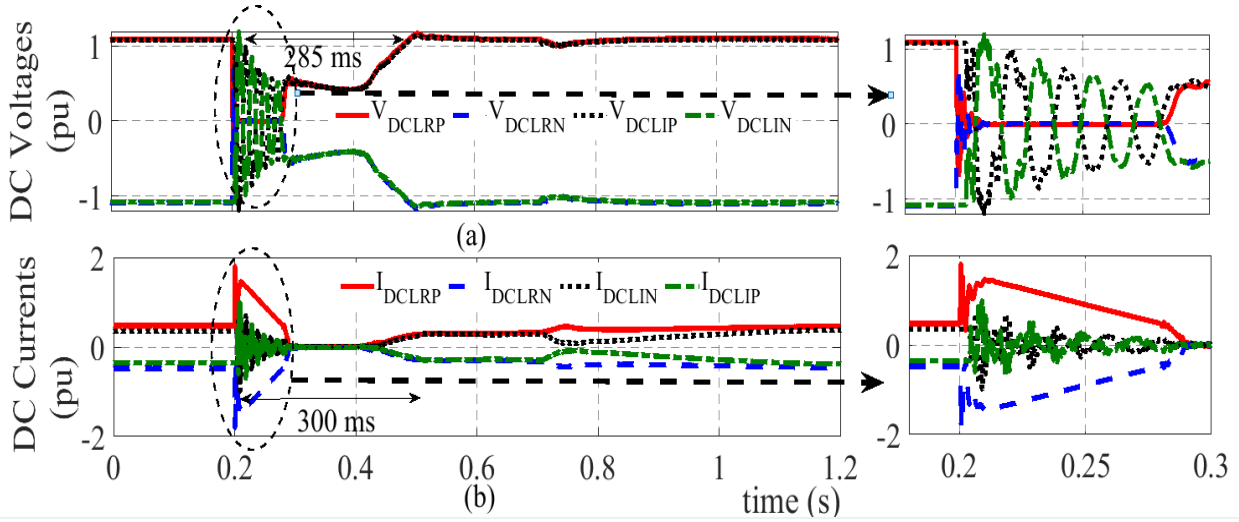


Fig. 5-8. LCC stations DC measurements for a P-Pole-to-N-Pole fault on the mainline (a) Voltages, (b) Currents

As depicted in **Fig. 5.9**, only the AC system connected to the LCC rectifier was noticeably affected by the fault. In contrast to the topology without DCCB studied in Chapter 4, the AC system connected to the VSC rectifier was not affected by the fault. A 0.26 pu drop in AC voltage at the LCC rectifier was due to 3.2 pu rise in AC current during the fault. However, unlike in the results of the fault recovery scheme presented in Chapter 4, nearly no transient is apparent in the AC system connected to VSC rectifier.

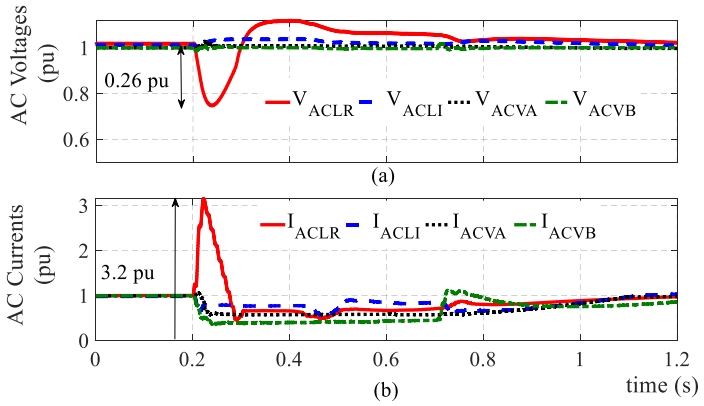


Fig. 5-9. AC side measurements for a P-Pole-to-N-Pole fault on the mainline (a) Voltages, (b) Currents

According to **Fig. 5.8**, the fault clearing time, voltage recovery time, and pre-fault state recovery times for the LCC link were observed to be 120 ms, 285 ms, and 300 ms respectively. These recovery time durations are less than a half of those achievable with DCCB-less topology presented **Chapter 4** (i.e. 300ms, 700ms, and 1000ms respectively). Without DCCBs, the VSC rectifier injects fault currents for several AC cycles until the ACCB opens and interrupts the VSC [133]. Furthermore, the VSC rectifier needs restarting and regaining controls to restore the pre-fault power level of VSC stations and this complete process required about 1200 ms as depicted in **Fig. 4.25**.

5.7.1.2. Pole-to-Ground Faults

The single-pole-to-ground fault recovery performance was studied considering a metallic P-pole-to-ground fault on the mainline, 700 km away from the LCC rectifier. As per the results shown in **Figs. 5.10** and **5.11**, strong transients are visible in healthy pole voltages and currents observed at both LCC and VSC stations. However, application of the fault recovery process in **Fig. 5.2**, stabilizes the voltages and currents of the healthy pole within about 200 ms. The power ramping up through the recovered pole begins about 500 ms after the fault. As visible in **Fig. 5.12**, the drop in AC side voltage of the LCC rectifier is smaller than that for the pole-to-pole fault.

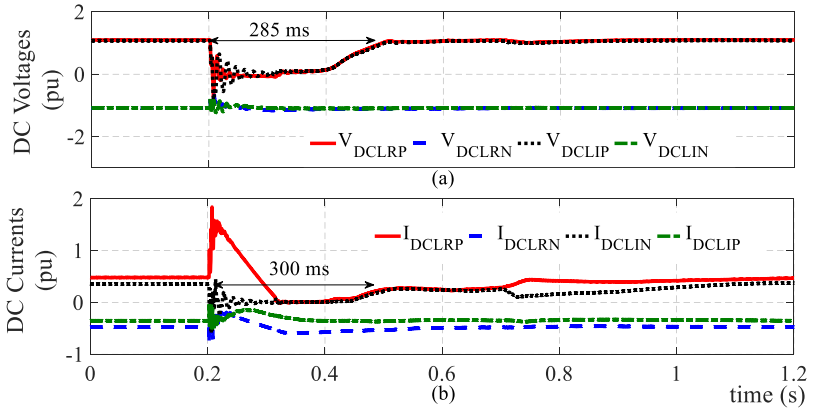


Fig. 5-10. LCC stations DC measurements for a P-Pole-to-ground fault on the mainline (a) Voltages, (b) Currents

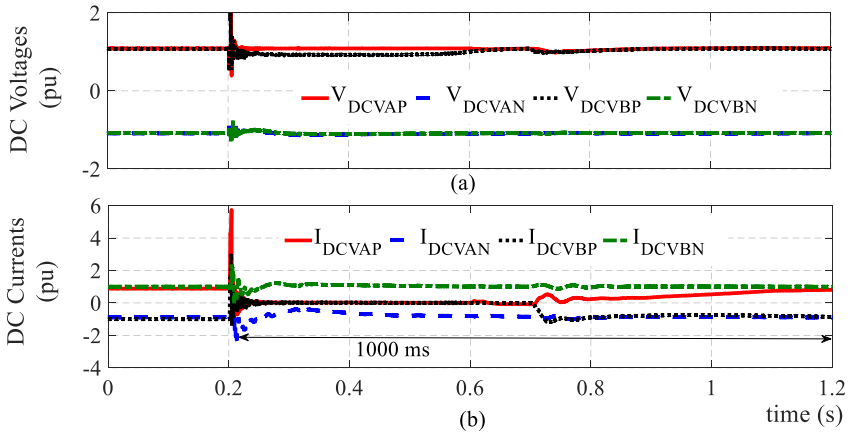


Fig. 5-11. DC side measurements at VSC stations for a P-Pole-to-ground fault on the mainline (a) Voltages, (b) Currents

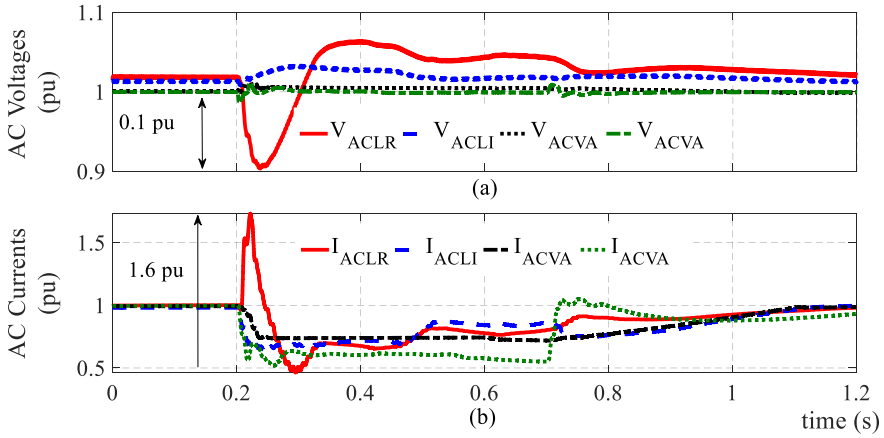


Fig. 5-12. AC side measurements for a P-Pole-to-ground fault on the mainline (a) Voltages, (b) Currents

Therefore, as depicted in **Fig. 5.13**, power can be transferred through the healthy pole during a single-pole-to-ground fault.

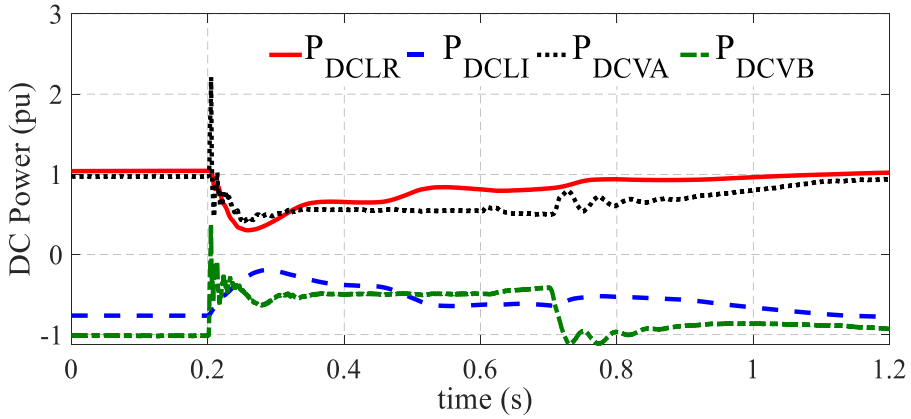


Fig. 5-13. DC power for a P-Pole-to-ground fault on the mainline

In addition to the recovery speed, the capability of transferring power through the healthy pole of VSC stations is another advantage of the proposed scheme when compared with the DCCB less scheme in Chapter 4.

5.7.2 Clearing Faults in VSC Branches

5.7.2.1. Pole-to-Pole Faults

Figs. 5.14 and **5.15** show the DC side measurements at converter stations for a metallic pole-to-pole fault on VSC branch-A, 50 km away from VSC-A (in Zone-A). According to **Fig. 5.14**, the LCC link was not impacted and the requirement I listed in **Section-5.3** was fulfilled. The fault recovery process of VSC-A is depicted in the vertical scale in **Fig. 5.15**. Note that this momentary peak fault current of 10.5 kA fed by VSC-A is shared by three arms of the VSC. As depicted in **Fig. 5.15** and **5.17**, it takes about 1000 ms to restore the pre-fault state. According to **Fig. 5.16**, as expected, only the AC side of VSC-A was affected by the fault. **Fig. 5.17** shows that a fraction of power was diverted from LCC inverter to VSC-B (inverter) during the fault recovery procedure.

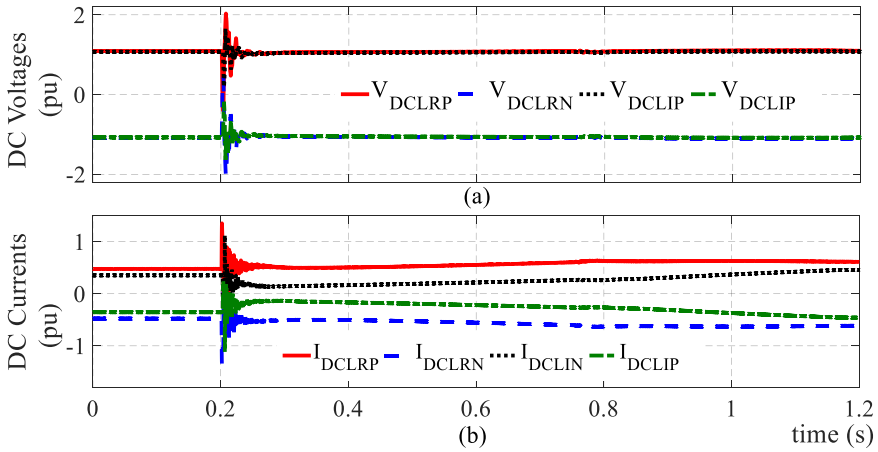


Fig. 5-14. LCC station DC measurements for a P-Pole-to-N-Pole fault on VSC branch-A (a) Voltages, (b) Currents

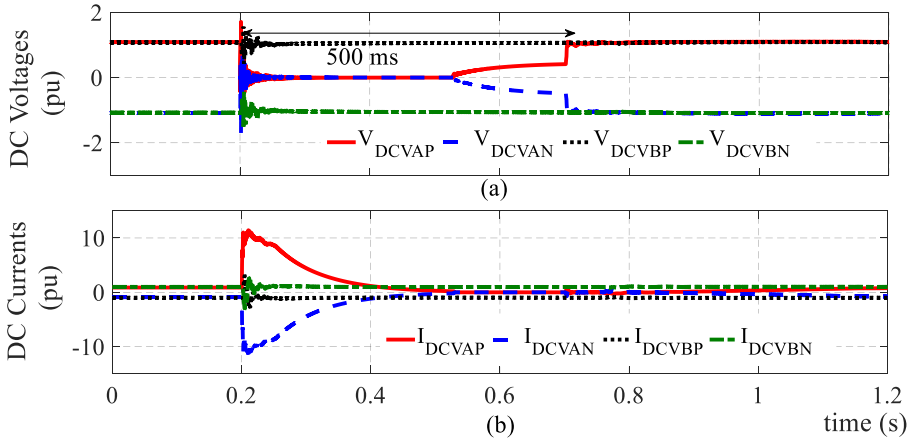


Fig. 5-15. VSC station DC measurements for a P-Pole-to-N-Pole fault on VSC branch-A (a) Voltages, (b) Currents

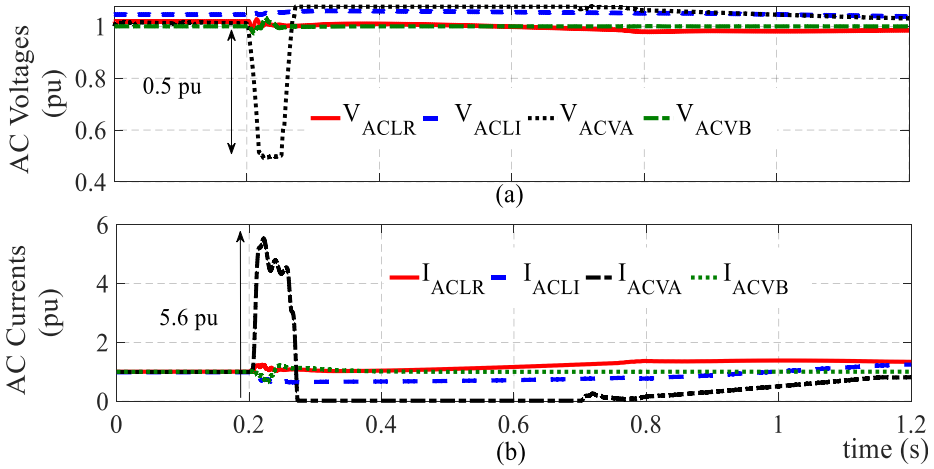


Fig. 5-16. AC side measurements for a P-Pole-to-N-Pole fault on VSC branch-A (a) Voltages, (b) Currents

The only major effect on the LCC link was the reduction of the power received to LCC inverter due to the sudden disconnection of VSC-A (rectifier). However, the amount of power delivered to the LCC inverter was restored to the pre-fault level within 1000 ms.

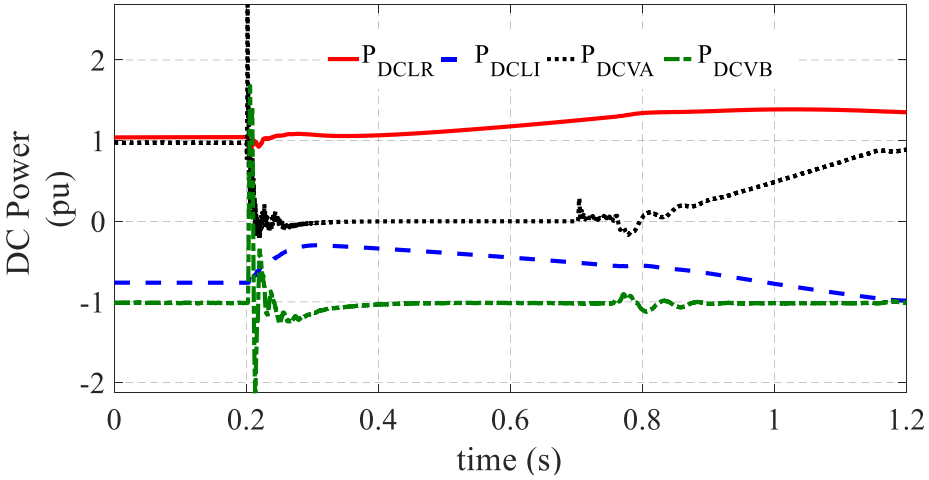


Fig. 5-17. DC power measurements for a P-Pole-to-N-Pole fault on VSC branch line-A

5.7.2.2. Pole-to-Ground Faults

Recovering from asymmetrical faults is more challenging, however, the successful application of the fault recovery procedure proposed in **Fig. 5.2** to recover from a single-pole-to-ground fault on VSC branch-A (Zone-A) is depicted in **Figs. 5.18** and **5.19**.

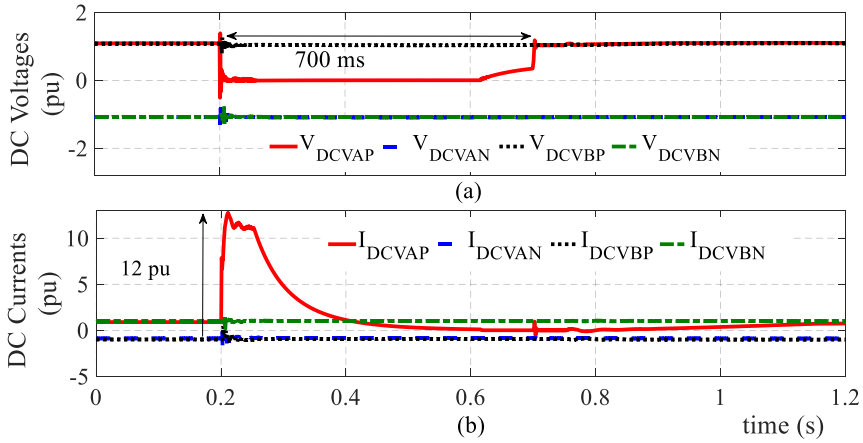


Fig. 5-18. VSC station DC measurements for a P-Pole-to-ground fault on VSC branch-A (a) Voltages, (b) Currents

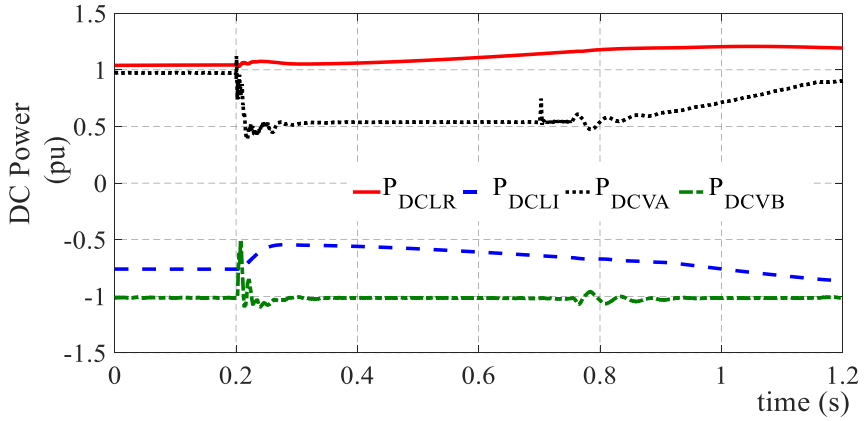


Fig. 5-19. DC power measurements for a P-Pole-to-ground fault on VSC branch-A

The healthy pole of VSC-A was capable of continuing the power transfer with ground return mode until the recovery from the fault.

Since the AC side voltage depression at VSC-A shown in **Fig. 5.20** was not noticeable, the healthy pole of the VSC was able continue power transfer in ground return mode, for about one second until the recovery from fault was complete.

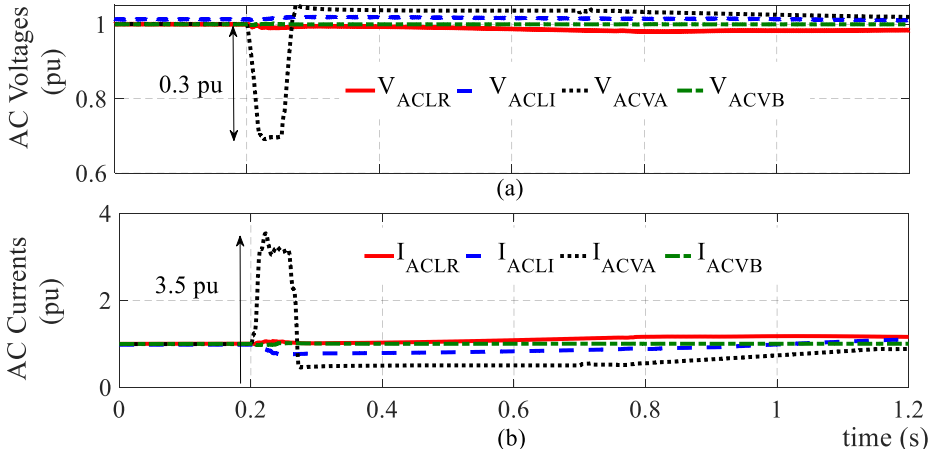


Fig. 5-20. AC side measurements for a P-Pole-to-ground fault on VSC branch-A (a) Voltages, (b) Currents

5.7.3 Performances Comparison

Fault recovery delays and possible improvements of the selective isolation when compared to the re-energization scheme described in **Chapter 4** is shown in **Table 5.5**, where T_{LPR} and T_{VPR} are respectively the total time taken to restore power flow in LCC link and VSC stations.

Table 5-5 Fault recovery times and improvement

F. Loc.	Type	T_{LPR} (ms)	η_{TL}	T_{VPR} (ms)	η_{TV}
Tap	P→N	0	1.00	1000	0.55
Tap	P→G	0	1.00	1000	0.50
Main	P→N	300	0.80	1000	0.55
Main	P→G	300	0.78	1000	0.50

For LCC link, the possible reduction of fault recovery time with DCCB compared to the approach without DCCBs was calculated using (5.7). The last column shows the possible reduction of recovery time for VSC link calculated in similar manner fourth column. In addition to the faster fault recovery, zero impact on the healthy pole during single pole faults is a major advantage of the fault recovery scheme with DCCBs.

$$\eta_{TL} = \frac{T_{Recovery\ without\ DCCB} - T_{Recovery\ with\ DCCB}}{T_{Recovery\ without\ DCCB}} \tag{5.7}$$

5.7.4 Fault Detection Speed and Breaker Rating

Fig. 21(a) shows the fault detection times for P-pole-to-N-pole faults and P-to-ground faults at increasing distance to the fault. It shows any metallic fault can be detected within 1.09 ms. The pole-to-pole faults on the mainline which results in higher maximum fault currents are detected a little faster than the single pole-to-ground faults and this is more desirable. Fig. 21(b) shows the observed maximum fault current through the DCCBs, 2ms after detecting the fault. Accordingly, a DCCB capable of interrupting 6 kA within 2 ms is adequate for the considered hybrid HVDC system.

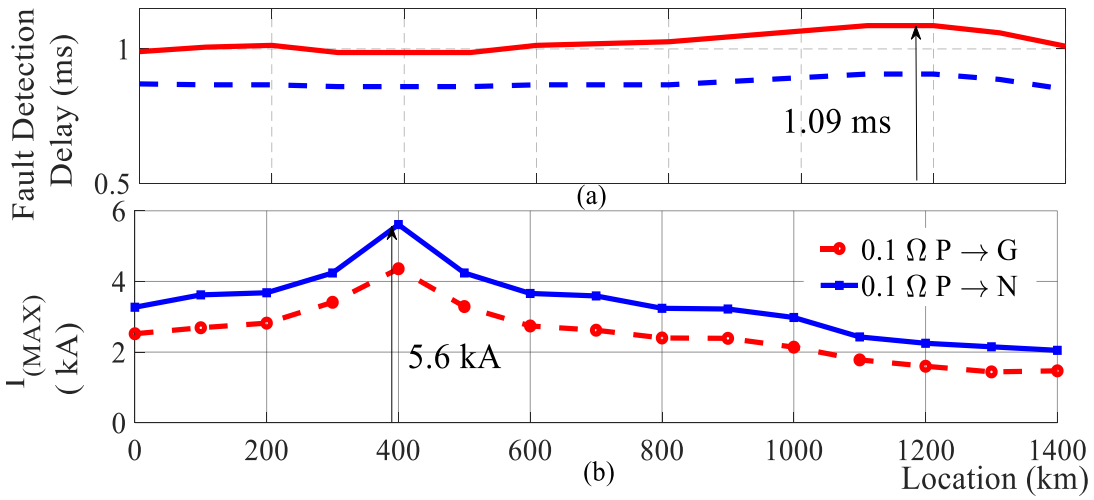


Fig. 5-21. (a) Fault detection speed, (b) Maximum DCCB current

As depicted in **Fig. 4.25**, the peak fault current occurs around the instant of blocking VSC IGBTs, which happens before breaking the current with DCCBs. Therefore, the required maximum breaking current is not increasing even if the DCCB operating delay is slightly increased. In order to test this, fault Scenario A was repeated by increasing the DCCB operating delay to 3 ms. No collapse of voltage or disruption of power flow through the LCC link was observed.

5.8 Concluding Remarks

A selective fault clearing scheme was proposed for a possible hybrid LCC-VSC multi-terminal HVdc transmission structure in which the spare capacity of an LCC transmission line is shared with a smaller VSC scheme. The proposed fault discrimination and fault clearing procedure allows tapping of the main LCC link without significant degradation of the fault recovery performances. This was achieved by optimally placing a DCCB on each VSC branch at the point of interconnection to the mainline. The chapter presented the development of a complete protection scheme based on the local voltage and current measurements to identify the faulted segment and

the conductors involved in the fault within a short time interval after a dc side fault, and a detailed fault recovery procedure that minimizes the extent of outages. Detailed simulations of variety of possible fault scenarios with the hybrid LCC-VSC MT-HVDC test system confirmed the

(i) ability of successfully discriminating the faults at different sections at a speed fast enough for successful fault recovery,

(ii) ability of identifying the faulted pole(s) to enable single-pole operation during the single-pole-to-ground faults,

(iii) successful recovery from temporary faults at various locations, and

(iv) the requirements of the DCCB can be met by a DCCB with a 6 kA maximum interruption capability and a maximum time delay of 2 ms, for the test system considered.

Chapter 6

Conclusions, Contributions, and Future Works

6.1 Conclusions

The thesis addressed the issue of DC side fault detection, discrimination and clearing in MT-HVDC grids. The research considered VSC based multi-terminal grids and LCC-VSC hybrid multi-terminal HVDC systems. The conclusions made from the studies presented in each chapter are presented here, accompanied by a brief summary.

Chapter 2 of the thesis presented a study on directional discrimination of faults in MT-HVDC grids, and application of directional discrimination to improve the dependability, security, and sensitivity of a peak ROCOV based protection proposed for an MT-HVDC grids. The line end di/dt limiting inductors, which are essential for allowing sufficient time for DCCBs to operate, facilitate fault discrimination based on the peak |dv/dt| observed at the line side of these inductors. It was shown that the direction of a fault with respect to a terminal inductor can be reliably determined by comparing the peak |dv/dt| values observed at its two ends. A simple characteristic curve to combine the fault directions determined using local measurements with peak |dv/dt| thresholds was proposed to develop sensitive and secure transmission line and bus protection algorithms. The proposed protection scheme was applied to a three-terminal HVDC grid, and its performance was verified through electromagnetic transient simulations conducted using PSCAD.

With the proposed protection scheme, it was shown that any fault that causes steady-state fault current beyond the breaker rating could be detected in less than 200 μs with the help of only local measurements. Simulation studies demonstrated that protection settings determined under normal operation gives correct decision even after changes in the operating conditions or configuration of the HVDC grid. The study also included an investigation of the appropriate signal frequency band and the parameters of the required hardware. From this study, the following conclusions can be made:

- The direction of a fault with respect to the terminal inductor can be reliably determined by comparing the peak |dv/dt| values observed at its two ends.
- The induced waves traveling along the dedicated metallic return wire can interfere with the bus side measurements if a di/dt limiting inductor is not present on the return conductor, and reduce the security and sensitivity of the peak |dv/dt| based protection.
- The security and sensitivity of directional protection in bi-pole HVDC grids with a single point earthed return wire can be greatly improved by including a di/dt limiting inductor of about 2.5-5.0 mH in the return wire.
- The proposed protection scheme based on directional and peak |dv/dt| based discrimination is applicable to HVDC grids consisting of both overhead lines and cables, loops and radial sections, and converter and floating buses. It is robust against minor network topology changes since peak |dv/dt| values are not considerably affected by the changes in the network topology.
- The proposed protection scheme can be easily implemented with practical hardware such as a voltage sensor having a bandwidth of 10 kHz, 25 kHz sampler, and a 12 bit analog to digital converter.

Chapter 3 of the thesis examined the problem of identifying the fault type and faulted conductors in an MT-HVDC grid and showed that this can be solved by comparing the maximum rates of change of bandlimited current measurements in a pair of conductors at a time. For a bipole grid with a dedicated metallic return conductor, five indices were introduced to compare the observed maximum ROCOC values of each pair of conductors. The proposed indices were shown to be independent of the fault resistance. A systematic procedure was developed for fault type identification using the proposed indices. With the help of detailed PSCAD simulations, the method was validated for several test systems consisting of both cables and overhead lines, two-conductor and three-conductor transmission configurations, and LCC and VSC stations. The method is capable of determining the fault type promptly and reliably only with the help of locally measured currents. The fault type information provided by the method can be used for supervising protection functions as well for deciding the response of control functions related to fault recovery. Main conclusions of the study in Chapter 3 are:

- The ratios between the maximum rates of change of bandlimited current measurements for different conductor pairs can provide information on fault types in HVDC transmission systems.
- The proposed algorithm can correctly identify the faulty type and the faulted conductors for long overhead transmission lines and cables, in point to point and multi-terminal HVDC systems,
- The method is applicable to both two-conductor and three-conductor systems. For two-conductor systems, only one index can be defined, and it is sufficient to distinguish between three possible fault types. For three-conductor systems, all five indices are necessary to distinguish all possible fault types involving the three conductors.

- The method can be easily implemented since (i) the threshold settings can be easily determined as indices are almost independent of fault resistance; and (ii) uses only locally measured low frequency current measurements.
- The proposed fault type discrimination method can identify the faulty conductors using a 1 ms data window.

Chapter 4 of the thesis investigated the development of a controller and control procedures to form a hybrid LCC-VSC grid, maintain its stable operation, and clear any faults with the help of existing control interfaces of the converter station controllers. A simple centralized master power controller, MPC, and a sequence of inputs were developed to energize and regulate the hybrid MT-HVDC transmission system. In order to make the hybrid multi-terminal configuration under study practically feasible, high level controls that coordinate the different converters in the grid were implemented without any significant modification to converter hardware or the lower level converter control interfaces. With the help of a detailed EMTP based simulation model executed in PSCAD, it was shown that a hybrid LCC-VSC multi-terminal HVDC transmission system can be formed and its operating conditions can be changed smoothly. A procedure to extinguish the fault arc and re-form the grid after clearing the fault was developed and investigated in Chapter 4. The proposed fault clearing procedure was validated with the simulations in PSCAD and the fault ride-through capability of the hybrid configuration understudy was confirmed. Based on the investigations carried in Chapter 4, the following conclusions are made.

- The proposed coordinated grid controller approach is capable of energizing the grid, regulating energy balance and ensuring smooth normal operation.

- Co-ordinated grid controller for hybrid LCC-VSC MT-HVDC transmissions system is capable of maintaining grid energy balance during transient states such as fault recovery periods and grid energization.
- The temporary fault recovery scheme enables smooth and fast clearing of temporary faults in a hybrid LCC-VSC MT-HVDC transmission system with the help of currently available means of clearing faults. Therefore, ensures the stability of the hybrid HVDC transmission system.
- When an LCC HVDC link is connected to VSC rectifier stations, the fault recovery time of the system becomes longer due to prolong fault current injection from the VSC rectifier station, which is de-energized using ACCBs.
- The series diode valves are capable of blocking the fault current injection from VSC inverter stations and avoid the need of restarting VSC inverters. However, they can be subjected up to 2 pu reverse voltage during the faults.
- It is observed that the operation of the healthy pole of a VSC rectifier station is severely affected during single pole-to-ground faults due to considerable dip in AC voltage during the initial period of fault current.

A practically implementable fault recovery scheme with the current means and technology was the main motto of fault clearing procedure developed in Chapter 5. However, due to the prolong fault current injection from VSC rectifiers, the fault recovery time of the hybrid LCC-VSC multi-terminal system is longer than the fault recovery time of the original LCC based HVDC link. The possibility of avoiding the above drawback was investigated in Chapter 5. A selective fault clearing scheme that avoids degradation of fault recovery performances of the LCC link due to tapping was presented in Chapter 5. A fault discrimination scheme was developed based on the

methods presented in Chapters 2 and 3, and used for operating DCCBs placed at the tapping points. With the proposed selective fault isolation scheme it was possible to eliminate the discontinuities of power transfer through the LCC link during the faults on tapping lines. The following conclusions can be made from the study presented in Chapter 5.

- The fault discrimination scheme presented in Chapter 5, developed using the concepts proposed in Chapters 2 and 3, fulfill the challenging fault discrimination requirements of hybrid LCC-VSC MT-HVDC transmission systems.
- The selective fault isolation scheme that uses a DCCB at each tapping point significantly improves the fault recovery performance of the hybrid LCC-VSC MT-HVDC transmission systems: discontinuity of power flow through the LCC link can be avoided during the faults on the branched out lines or VSC converters; recovery times of temporary faults on the mainline can be kept close to the fault recovery times of the original LCC link; and the continued operation of the healthy pole can be maintained after a single pole-to-ground fault.

A DCCB capable of breaking 6 kA in 2 ms is adequate for the considered LCC-VSC MT-HVDC transmission system example. Construction of a DCCB with similar capacity is not beyond the current technology, for example, ABB has reported testing a prototype of DCCB capable of breaking 8 kA in 2 ms in the year 2012.

6.2 Publications and Patents Arising from the Thesis

6.2.1 Journal Publications

1. M. H. Naushath, A. D. Rajapakse. "Application of new directional logic to improve DC side fault discrimination for high resistance faults in HVDC grids." *J. Mod. Power Syst. Cle.*, vol. 5, no.4, pp. 560-573, June 2017..

2. M. H. Naushath, A. D. Rajapakse, “Local measurement based ultra-fast directional ROCOV scheme for protecting Bi-pole HVDC grids with a metallic return conductor”, *Int. J. Elec. Power*, vol. *98*, pp. 323–330, June 2018.

3. M. H. Naushath, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "Investigation of Fault Ride-Through Capability of Hybrid VSC-LCC Multi-Terminal HVDC Transmission Systems," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 241-250, Feb. 2019.

4. M. H. Naushath, A. D. Rajapakse, "Fault Type Discrimination in HVDC Transmission Lines Using Rate of Change of Local Currents," *IEEE Trans. Power Del.*, vol. 35, no. 1, pp. 117-129, Feb. 2020.

5. M. H. Naushath, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "A Selective Fault Isolation Scheme for Hybrid VSC-LCC Multi-Terminal HVDC Transmission Systems," *Energies*, vol. 13, pp. 001-021, July 2020.

6.2.2 Conference Publications

1. Naushath M. Haleem and A. D. Rajapakse,," Challenges in Fault Detection and Discrimination in Multi-terminal HVDC Grids and Potential Solutions," *In Proc. International Conference on Power Systems Transients,* Seoul, South Korea, Jun, 2017.

2. Naushath M. Haleem, A. D. Rajapakse, A. M. Gole and I. T. Fernando, "Energization and regulation of a hybrid HVDC grid with LCC and VSC," *In Proc. IEEE Electrical Power and Energy Conference*, Saskatoon, Canada, Oct., 2017.

3. Naushath M. Haleem and A. D. Rajapakse, "A single pole to ground fault location method for HVDC transmission lines based on coupling characteristics," *1In Proc. IET International Conference on AC and DC Power Transmission*, Coventry, UK, Feb, 2019.

4. Naushath M. Haleem, A. D. Rajapakse, A. M. Gole and I. T. Fernando, " *Investigation of Fault Ride-Through Capability of Hybrid VSC-LCC Multi-Terminal HVDC Transmission Systems*, " In Proc. *IEEE PES General Meeting*, Atlanta, USA, Aug., 2019.

5. Naushath M. Haleem and A. D. Rajapakse, "Identification of Faulty Conductors in HVdc Links Connecting Future Offshore Wind Sites," In Proc. *IET International Conference on Developments in Power System Protection*, Liverpool, UK, Mar. 2020.

6.2.3 Patents

A PCT application (App. No: 62/54,005 Filling Date: 11/01/2018) has been filed for Method of Determining the Conductors Involved in a Fault on a Power transmission line and Fault Locating Using Local Current Measurements

- Inventors: Naushath M. Haleem, Athula D. Rajapakse, and Jagannath Wijekoon.
- Assignee: University of Manitoba.

6.3 Future Work

The thesis proposed some elegant solutions related to the problem of MT-HVDC grid protection. However, there are many aspects to further studies. Some directions for future research that arise from the research reported in this thesis are:

1. Evaluate the effect of sensing errors such as non-linearities, limited bandwidth, and measurement noise on the algorithms presented in Chapter 2 and Chapter 3.
2. Evaluate the impact of lightning on the transmission line fault discrimination algorithms presented in Chapter 2 and Chapter 4
3. Develop a complete fault discrimination scheme to protect MT-HVDC grids by developing algorithms to identify AC side faults, converter internal faults, and discriminating against those from the DC transmission system faults.
4. Placing HVDC transmission systems on the existing transmission towers may reduce the cost of a new HVDC project and turn a project into a feasible one from infeasible. Similarly, in some situations, the cost can be reduced by using the right of way of an existing HVAC transmission corridor. Fault between HVDC transmission conductors and HVAC transmission conductors are possible in such transmission systems. A worthy research direction is to extend the fault type discrimination algorithm presented in Chapter 4 to identify and classify inter-circuit faults between HVDC and HVAC conductors.

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Appendix-I

Appendix-I

Section -1

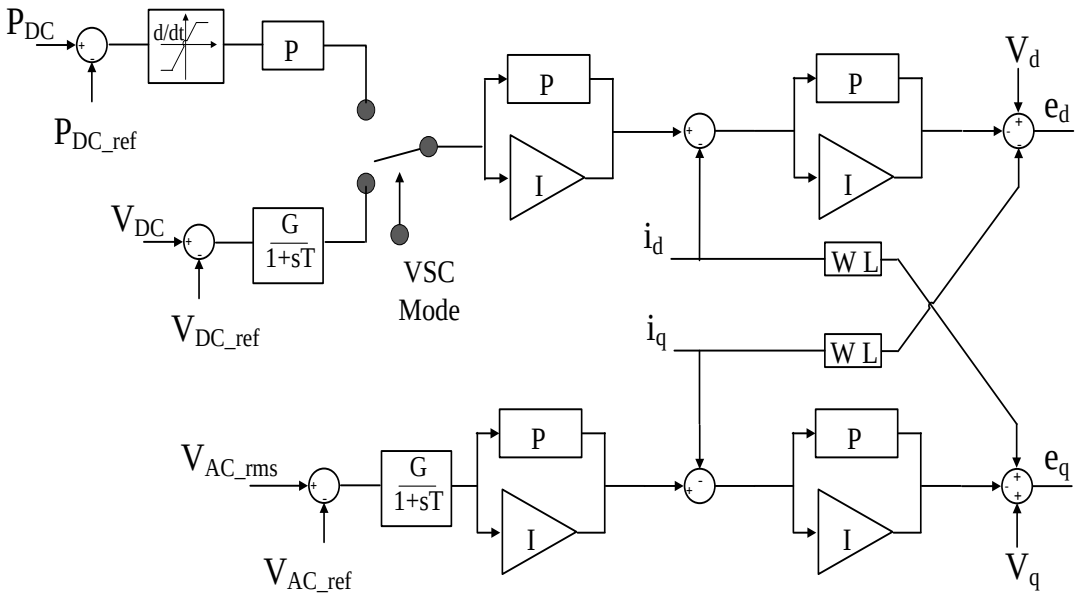


Fig. A-1 Decouple D-Q controller used in VSCs

- Mode selection switch at the input of PI-controller assure smooth transition between modes
- DC power or DC voltage is controlled through d-axis control
- AC side voltage is controlled through the q-axis control

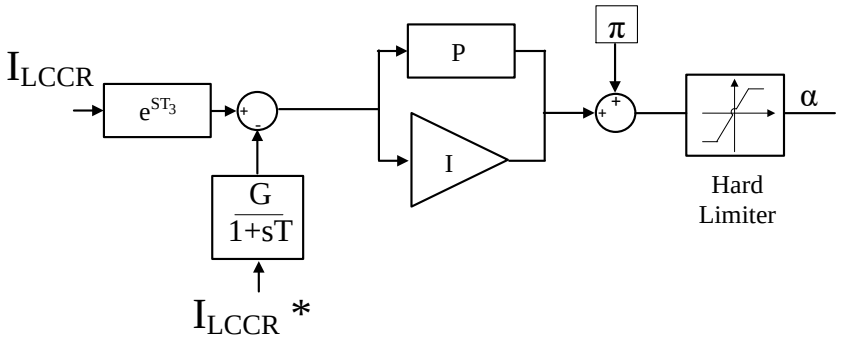


Fig. A-2 Constant current controller used in LCC rectifier.

- The current order I_{LCCR} is calculated at LCC inverter using the power order
- The current order I_{LCCR} is reduced to 1/3 of the reference value if the estimated voltage of rectifier terminal at the inverter is less than 0.4 pu.
- The ramping rate of LCC rectifier is set with the rate limiter at the output

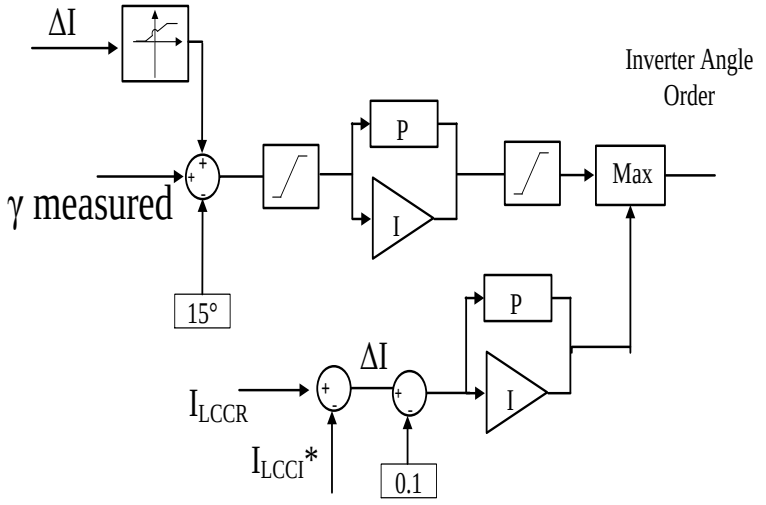


Fig. A-3 Constant extinction angle control used in LCC inverter.

- During the normal operation, extinction angle is maintained at 15°
- Extinction angle is increased if the measured current at inverter is considerably greater than the current order issued to LCC rectifier at the inverter

Section -2

A.2.1. Converter Side Voltage of the Transformer Connected to VSC stations

- The modulation index *m* is defined in (A.1),

$$m = \frac{V_{ac\_p}}{V_{DC}/2} \tag{A.1}$$

Where peak converter voltage, V_{ac_p}, and line-to-line rms voltages, $V_{ac\_LL}(rms)$, are related by (A.2),

$$V_{ac\_LL}(rms) = \sqrt{\frac{3}{2}} V_{ac\_p} \tag{A.2}$$

- Line-to-line rms voltage of the converter side of the transformer is given by (A.3),

$$V_{ac\_LL}(rms) = m\sqrt{\frac{3}{2}}\frac{V_{DC}}{2} \tag{A.3}$$

- Example: for the test system in Section 2.4, the converter side line-to-line rms voltage when V_{DC}=320 kV and *m* is 1.15,

$$V_{ac\_LL}(rms) = 1.15 \times \sqrt{\frac{3}{2}} \times \frac{320}{2} = 225\ kV$$

A.2.2. Capacitor Selection

- The capacitor C_{SM} is related to change in voltage across the capacitor voltage ΔV is given by (A.4).

$$\Delta V = \frac{I\Delta T}{C_{SM}} \tag{A.4}$$

Where ΔT is the period of charging/discharging cycle and *I* is the average current through the capacitor.

- The fault current behavior characterized by maximum energy stored in capacitors to power ratio, *E/P*, defined in (A.5).

$$E/_P = \frac{6\,E_{arm}}{S_{Cov}} \tag{A.5}$$

Where S_{con} is the apparent power of each converter pole and E_{arm} is the sum of energy stored in capacitors of each arm.

- The stored energy in each arm, $E_{arm,}$ can be find using (A.6),

$$E_{arm} = \frac{1}{2} N C_{SM} \left(\frac{V_{DC}}{N}\right)^2 \tag{A.6}$$

Where N is the number of sub-modules per arm

- Therefore, capacitor size and number of capacitors influence the fault current behavior and E/P between 10 J/kVA to 50 J/kVA is considered as suitable selection.
- Example1: To fix E/P ratio to 25 J/kVA for test system in Section 4.6 in which V_{DC}=500 kV, N=200, S_{Con}=300 MVA.
    - With (A.5), E_{arm}=1.25 MJ and using (A.6), C_{SM}=2 mF
- Example2: For the test system described in Section 2.4, N=98, S_{Con}=500 MVA and C_{eqv}. The C_{SM} is, N x C_{eqv} /6, 1.63 mF.
    - With (A.5), E_{arm}=0.85 MJ and using (A.6), E/P=10.24 J/kVA

A.2.3. Number of IGBTs in an Arm

- Half of the pole voltage appear across each arm. Therefore, voltage across each IGBT, V_{IGBT}, is given by (A.7).

$$V_{IGBT} = \frac{V_{DC}}{2N} \tag{A.7}$$

- For test system described in Section 2.4, V_{DC}=320 kV and N=98. Therefore, IGBT voltage is 1.63 kV.

- For test system described in Section 4.6, V_{DC}=500 kV and N=200. Therefore, IGBT voltages is 1.25 kV.

A.2.4. Terminal Inductor Selector

- Inductor limit the rate of rising fault current.
- The size of the inductor, L, required delay occurrence of peak current I_{Peak} by ΔT_B during a fault just outside of the inductor can be found by (A.8).

$$L = \Delta T_B \frac{V_{DC}}{I_{Peak}} \quad \text{(A.8)}$$

- Example: For the test system in Section 2.4, V_{DC}=320 kV and a DCCB capable of breaking 16 kA and 2 ms is considered. Therefore, L=40 mH fulfils the need.

Section -3

Table A.1 Converter parameters of the circuit given in Fig. 3.1(a)

Parameter	Value	Units
Arm inductor (L_{arm})	37	mH
Series resistance (R_{arm})	0.5	Ω
Terminal inductor (L_t)	50	mH
Equivalent capacitance (C_{eq})	300	µF
IGBT blocking threshold	2	pu
Blocking delay	500	µs

Table A.2 Equivalent transmission system parameters of Fig. 3.1(b)

Parameter	Value	Units
Line series inductance (L_x)	0.40	mH/km
Mutual inductance (L_m)	0.19	mH/km
Line series resistance (R_x)	0.45	mΩ/km
Shunt capacitance (C_x)	2.70	nF/km
Mutual capacitance (C_m)	0.16	nF/km
Length from converter-1 to fault	100	km
Length from converter-2 to fault	300	km

Table A.3 Overhead transmission line parameters

Parameter	Value	Units
Conductor type	Chukar	
Sag	10	m
Ground resistivity	100	Ω-m
Shunt conductance	1.0×10^{-11}	Ω/m
Relative permeability	1	
Main Conductors		
DC resistance	0.010714	Ω/km
Radius	0.0406	m
Shielding wire		
DC resistance	0.034	Ω/km
Radius	0.00825	m

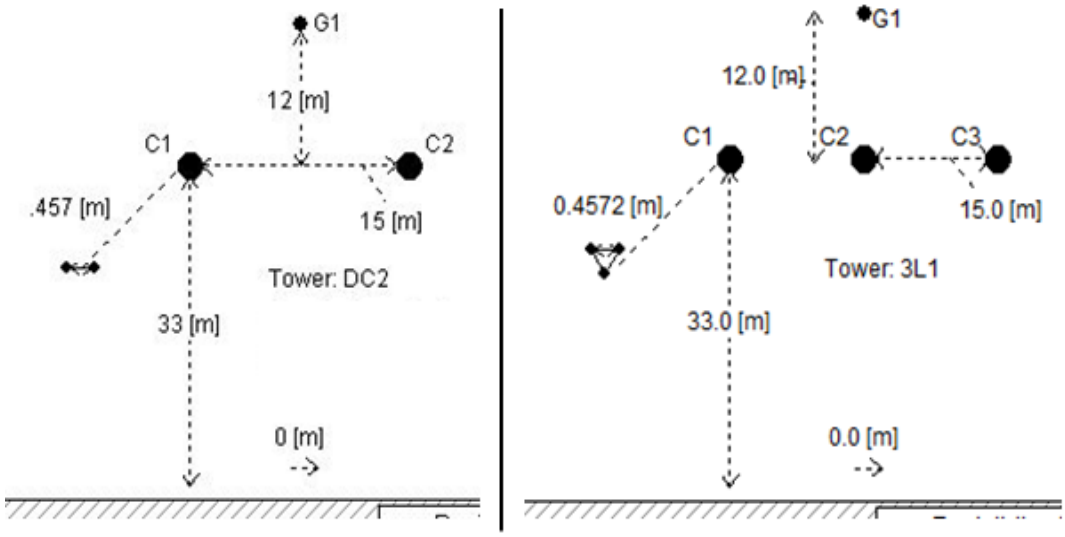
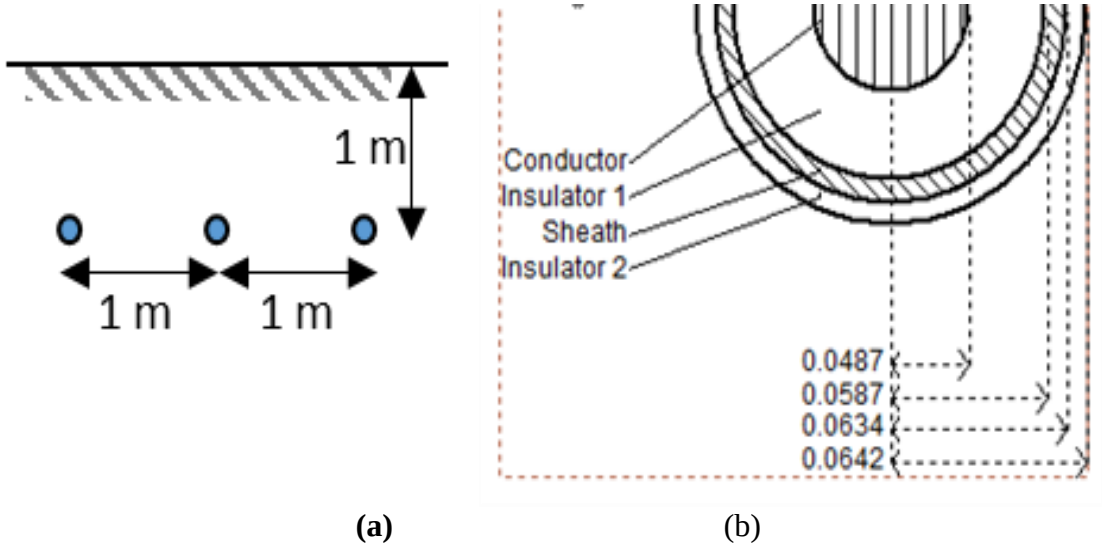


Fig. A-4 Conductors and tower configuration of two-conductor and three-conductor overhead transmission lines.



(a) (b)

Fig. A-5 Cable design, (a) Cable configuration, (b) Dimension of each cable

Table A.4 Cable parameters

Parameter	Value	Units
DC resistance of conductors	0.0282	mΩ/km
DC resistance of sheath	0.0186	mΩ/km
Relative permeability of conductors and sheath	1	
First insulation layer		
Relative permeability	3	
Relative permittivity	2.5	
First insulation layer		
Relative permeability	1	
Relative permittivity	2.3	