Design and Implementation of a High-Bandwidth Switching Power Amplifier Using FPGA-Based Boundary Control

by

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Abstract

Power amplifiers are critical components for audio, grid simulator and Power Hardware-in-the-Loop (PHIL) applications with the requirement of low cost, high bandwidth and fast dynamics. This thesis proposed an innovative combination of a GaN-based inverter and boundary control implemented in an FPGA to realize a high-bandwidth switching power amplifier with high bandwidth-switching frequency ratios. The control strategy, implementation considerations and the experimental results are presented in this thesis.

The influences of the non-ideal factors, including the limited bandwidth of the components and the limited resolution of the analog-to-digital converter when implementing boundary control in a system, have been discussed and analyzed. A proposed compensation method to mitigate the negative impact on the performance of the boundary control from the overall delay has been verified experimentally.

This thesis has proposed an analytical method to estimate system bandwidth with boundary control based on the frequency response of the RLC circuit and the specification of the system. Experiment results have verified the proposed method.

The Power Amplifier achieves a 30 kHz average switching frequency with the bandwidth of 7.1 kHz, the rated power of 1000 W, amplifier gain of 100 V/V and the power efficiency of 97.78%. The experimental results show that the system can track the step changes of the reference and the load in tens of microseconds.

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Dedication

To my dear parents and beloved husband.

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List of Abbreviations

AC	Alternating current
ADCs	Analog to digital converters
CHL	Controller hardware in the loop
DACs	Digital to analog converters
DC	Direct current
IGBT	Insulated-gate bipolar transistor
MACS	Multiply-accumulate operations per second
MOSFET	Metal-oxide-semiconductor field-effect transistor
MW	Megawatts
HEMT	High-electron-mobility transistor
WBG	Wide-bandgap
RTS	Real-time simulator
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
IC	Integrated circuit
USB	Universal Serial Bus
PC	Personal computer
PHIL	Power hardware in the loop
PI	Proportional-integral

PID	Proportional-integral- derivative
PR	Proportional resonant
PWM	Pulse width modulation
VSC	Voltage source converters

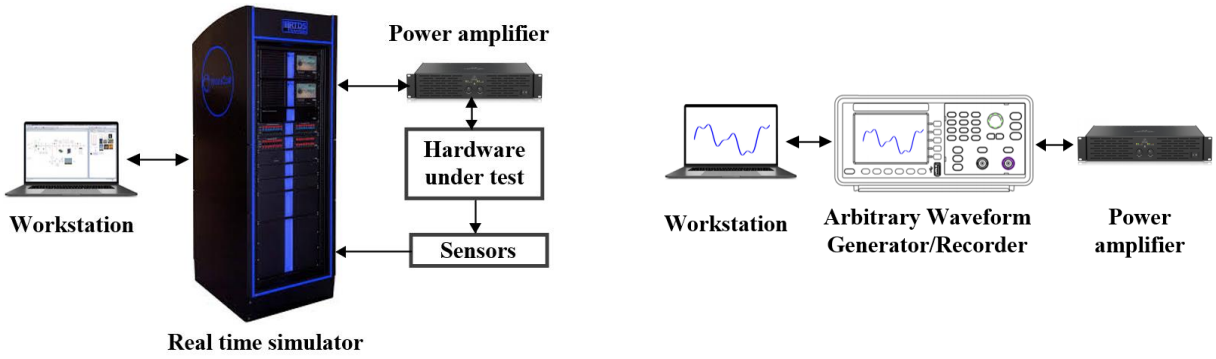
Chapter 1 Introduction

1.1 Background

High bandwidth power amplifiers aim at reproducing the inputs from signal formats into power formats in the applications that require fast response and high fidelity in a relatively broad input frequency range dependent on the applications. The bandwidth of a power amplifier is the frequency range of the output, usually from DC to a specific frequency, for which the output power can be maintained at least half of the rated power. Commonly, the bandwidth of a power amplifier refers to the output frequency when the output power equals to half of the rated power.

One application of high bandwidth power amplifier is as the power interface in Power-Hardware-in-the-loop (PHIL) simulations [1][2][3][4]. Figure 1-1 (a) shows a typical configuration of PHIL simulations. The power system simulation software installed in the workstation is an interface to the real-time simulator (RTS) building the working environments. The RTS simulates complex power systems with a typical time step of 25μs ~50μs. The power amplifiers and sensors provide the interfaces between the hardware under test and the simulated power systems [5][9]. The power amplifier interface is a critical component in PHIL simulations. The ideal case for the power amplifier interface of PHIL should have a unity gain with infinite bandwidth and no delay [7]. However, the practical power amplifier will have limited bandwidth and introduce latency and errors. These unrealities which are not exited in the original power system will affect the accuracy and the stability of the PHIL simulations [1][2][3][4] [7][14]. Therefore, to increase the fidelity, validity and stability of the PHIL simulations, it is essential to design a high bandwidth power amplifier.

The other applications include grid simulators, audio power amplifiers and servomotor drives [6][9]. The grid simulators in Figure 1-1 (b) provide a line voltage with harmonics by the amplification of a voltage signal from a programmable reference generator. The reference generator can be an RTS with a more sophisticated power system inside and the output can be connected hardware under the test, which essentially makes the grid simulator one application of the PHIL[9]. With the penetration of more power converters and nonlinear loads into the grid, high-order harmonics should be emulated in the grid simulators, which require a high-bandwidth power amplifier to reproduce the high-order harmonics [3].



(a) PHIL Simulation (b) Grid simulator

Figure 1-1: Typical High Bandwidth Power Amplifier Applications [10][15]

1.1.1 Practical Power Amplifier Options

Practical power amplifiers for the intended applications are linear amplifiers [17][18] and switching power amplifiers realized by power electronics converters, usually voltage source converters (VSC) or inverters [3][14][16]. In the applications of testing a balanced three-phase grid, the synchronous generator type amplifier is an option as well [7].

Linear power amplifiers operate in the linear region of the semiconductors while the switching power amplifier operates in the saturation region of the semiconductors. The difference between the natures of these two types of power amplifiers leads to different key characteristics listed in

Table 1-1. The power rating or operation range is limited for linear power amplifiers due to the high power loss and the manufacturing difficulty[7]. While switching power amplifiers have a high power-rating from kW to MW [5][13]. The bandwidth of linear power amplifiers is high, usually more than 10 kHz[11], and the dynamic response is fast, generally less than 6 μs including propagation delay and the phase shift [10][12]. Compared with linear counterparts, switching power amplifiers have a lower bandwidth due to the additionally complex control circuits, and the bandwidth is depending on the control algorithm, switching frequency and filter parameters. The bandwidth of switching power amplifiers is usually less than 3 kHz [11], and the response time is more than ten times of that for linear power amplifiers [5]. Simple transfer functions can be derived to represent Linear power amplifiers' dynamics and the linear-controlled switching power amplifiers' dynamics, which provide an easy way to theoretical analyze the simulated power systems [5][7]. In terms of the cost and size, switching power amplifiers have more advantages.

Table 1-1: Comparison of Linear and Switching Power Amplifiers [5][9][10][11]

Features	**Linear Power Amplifier**	**Switching Power Amplifier**
Power rating	Low	High
Bandwidth	High	Low
Response time	Short	Long
Power Efficiency	Low (~70%)	High (~95%)
Cost Efficiency	High	Low
Size	Large	Small

To summarize, linear power amplifiers are preferred in the applications with the requirements of high system bandwidth, short delay time and fast dynamic response. However, the drawbacks are high costs, large sizes and high power losses. Switching amplifiers are preferred due to lower cost, higher power rating, smaller size and less complicated manufacture.

The designed switching power amplifier has to take advantage of the higher efficiency, lower cost and smaller size and meanwhile overcome challenges of reduced bandwidth and slow response of the switching power amplifiers. To achieve that, the characteristics of the power semiconductor switches are critical to realizing high switching frequency, and the control algorithm is the key to fast dynamic responses. Moreover, high-performance controller hardware is essential to implement the control algorithm and generate the switching signals.

1.1.2 Power Semiconductor Switches

Power semiconductor switches are the heart of power electronic converters due to their high conversion efficiency. Modern power electronics era started in the late 1950s, when Bell Lab invented the first Thyristor and General Electric Company developed the first commercial Thyristor. After that, the power semiconductor devices, i.e. Thyristors, IGBTs, MOSFETs, have appeared and dominated the power electronics and power system market [19]. In recent decades, Wide Bandgap (WBG) materials were introduced to the semiconductor device fabrication and SiC devices and GaN devices are the products of the WBG materials.

Figure 1-2 shows the power rating and switching frequency range of Thyristor, IGBTs, MOSFETs, SiC devices and GaN devices. Because of the different operation ranges, different types of semiconductor devices have their major application domains. Thyristors are used for low switching frequency (up to 1 kHz) and high-power rating (up to tens of MW) applications. IGBTs are used for medium switching frequency (between 1 kHz to 20 kHz) and medium power rating (up to several MW) applications. MOSFETs are used for high frequency (between 10 kHz to hundreds of kHz) and low to medium power rating (up to 10 kW at a relatively low switching frequency) applications. The WBG devices push the switching frequency to be even higher (up to several MHz) and the power rating to be higher at a high switching frequency region. Especially GaN

high-electron-mobility transistors (HEMTs) have more applications, including commercialized evaluation boards and prototype, since it can achieve high frequency and high-density power conversion [21][22][23].

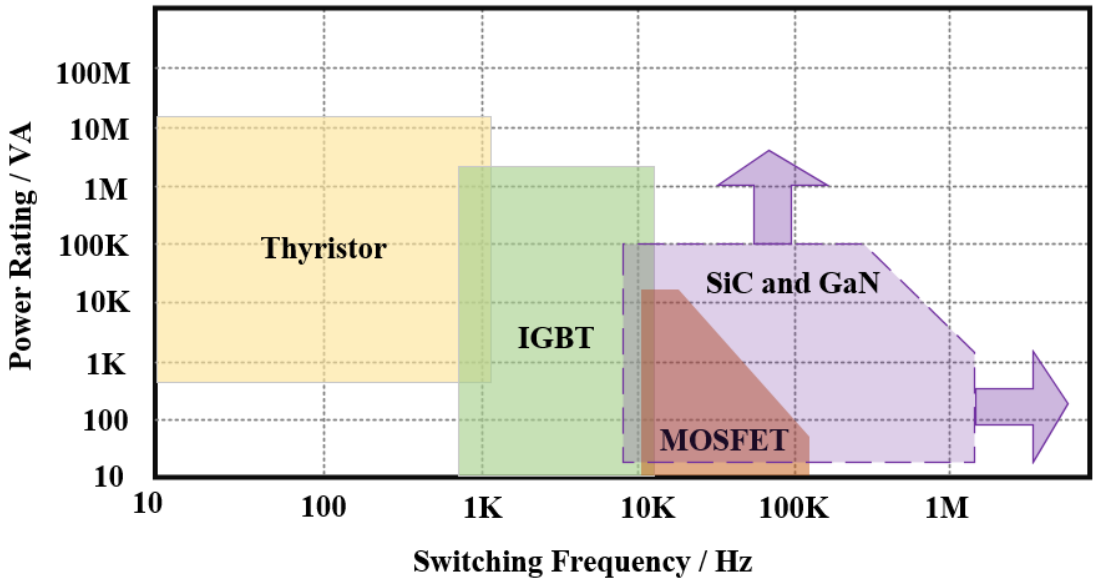


Figure 1-2: Operating Regions of Typical Power Semiconductor Switches [19][20]

In a switching power amplifier application, the switching devices are usually IGBTs and MOSFETs. IGBTs-based power amplifiers have a higher power rating, lower switching frequency and lower system bandwidth compared to MOSFETs-based power amplifiers [3]. [24] used MOSFETs-based power amplifiers to achieve a switching frequency of 55 kHz with the system bandwidth 11 kHz and power rating less than 100W. [3] used a cumulated way to have an IGBTs-based power amplifier and a MOSFETs-based one both to achieve both high switching frequency and high power rating. In [3], the IGBT-based amplifier had the switching frequency of 8 kHz, bandwidth of 1 kHz and the power rating of 5 kVA while the MOSFETs-based one had the switching frequency of 50 kHz and power rating of 250 VA. New switching amplifier designs

have the potential to reach a bandwidth of more than 5 kHz and a power rating of more than 1 kW using GaN HEMTs due to their high switching frequency with low power loss [11].

In summary, different semiconductor switches have their dominating applications, and to build a high bandwidth switching power amplifier with a reasonable power rating, the use of WBG semiconductors like GaN HEMTs is necessary.

1.1.3 Control Method for Switching Power Amplifier

The control for the power electronic converters is commonly linear control, i.e. Proportional-Integral (PI) control. Linear control using Laplace transform and transfer function concepts is firmly established in the control theory and suitable for linear systems. Small signal-averaged transfer functions based on state-space averaged models of the power circuits and pulse width modulation technique are used together to design the transfer function of the linear controller and generate the switching signal. Figure 1-3 shows a typical power electronic system with a linear controller. However, power electronic converters are highly nonlinear systems because of the power semiconductor switches. The small-signal analysis of linear control ensures the prescribed dynamics around a specific operating point. The system performances need more considerations for a range of operating points and large transients and disturbances [28][29].

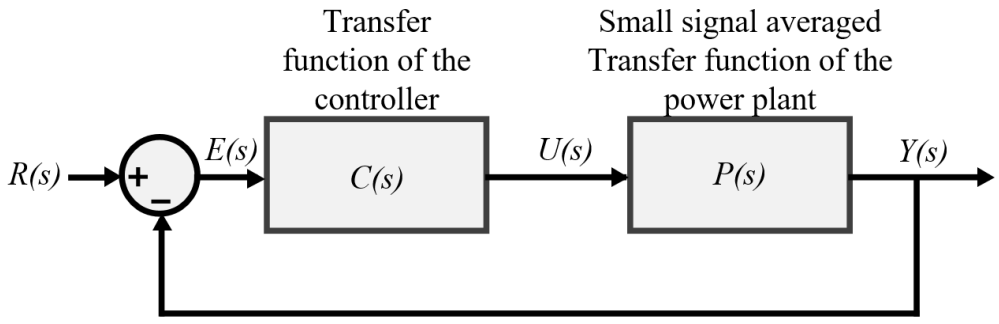


Figure 1-3: A Brief Block Diagram of Power Electronic Systems with a Linear Controller [28]

Nonlinear control based on state trajectory is born to optimize large-scale dynamics. This nonlinear control method is a geometric control method, which suits the power electronic converters with time-varying structures [35]. It takes advantage of all available information in the power electronic converters, including the topology, the filter parameters and all the possible behaviours when switching states change [30]. Therefore, it can generate the exact switching sequence to move the state of the converters from the initial operating point to the desired operating point without differentiating transient and steady-state [37]. This nonlinear control uses the switching surface and generally provides fast large-signal dynamics and stability [35]. Figure 1-4 shows the state plane of a full-bridge inverter with an LC filter, the yellow line shows the ideal switching surface, and the blue line is the load line. The points on the state plane are located into three regions: reflective region, refractive region and rejective region. Points in the reflective region are on the trajectories towards the switching surface on both sides of the switching surface. Points in the refractive region are on the trajectory towards the switching surface, and after the trajectory reaches the switching surface, the trajectory will lead away from the switching surface. Points in the rejective region are on the trajectories away from the switching surface [31][43]. By design the switching surface between the refractive region and reflective region, the controller is stable inherently because the system state will always move toward the switching boundary and to the desired operating point consequently [30][43]. The controller has a better dynamic response when the switching surface is proximate to the boundary of the refractive region and the reflective region [37][38]. With the guide form the boundary control law, the system reaches the target operating point in two switching actions from the original operating point shown in red lines in Figure 1-4 [41].

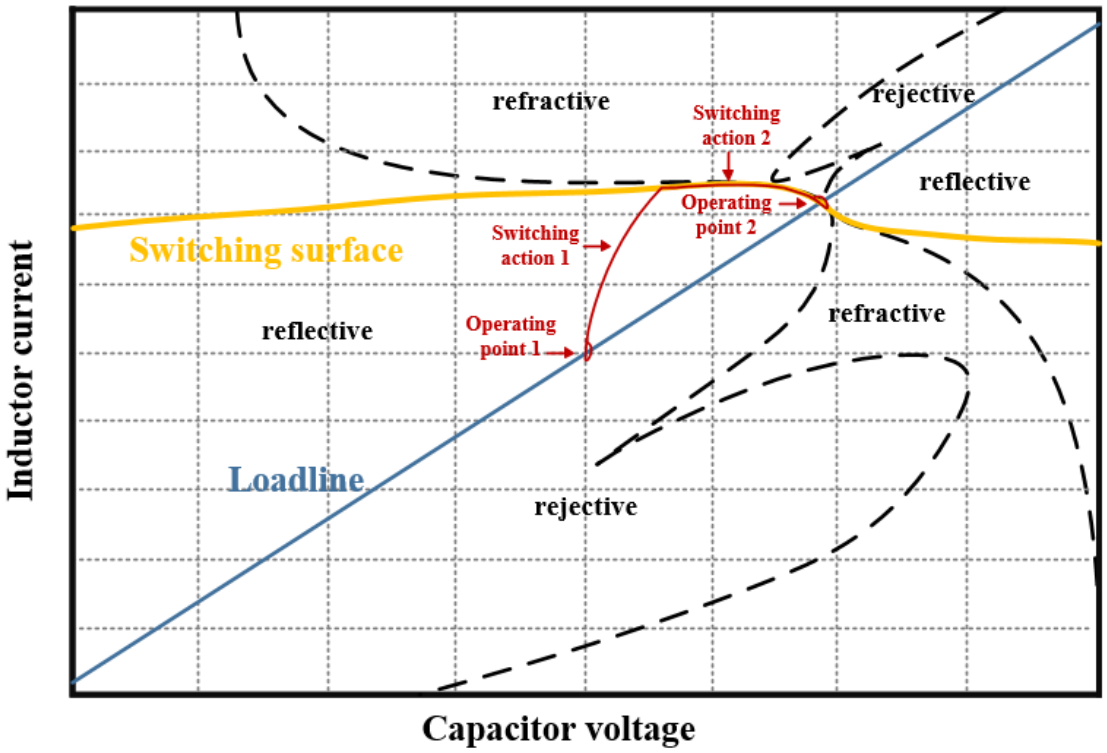


Figure 1-4: The State Plane of an Inverter with an LC Filter [37]

The different control methods with the same concept of using switching surfaces have emerged by applying different approximations, assumptions and switching surfaces. The methods include hysteresis control, sliding-mode control, second-order boundary control and N-order boundary control [27][30][34]-[40]. Compared to high-order boundary control, hysteresis control and sliding-mode control have a slower transient response. The high-order boundary control has the switching surface nearly along the boundary between the reflective and refractive regions, which improves the tangential velocity of the trajectories along the switching surface [35][37]. Furthermore, the boundary control law's parameters are from the power circuits directly, while the sliding-mode control usually uses a trial-and-error method to avoid instability in the rejective region [31][43]. High-order boundary control requires more computing power than first-order control. The need for higher computing power results in longer computing time and reduced

accuracy since the nonlinear control based on state trajectories desires an instantaneous computation and control. Second-order boundary control is preferred to maintain fast dynamic performances and meanwhile reduce the requirement of computing power [35]-[40].

The stability of linear control is analyzed using small-signal analysis and transfer functions. A carefully designed linear control with proper control parameter to provide the desired properties, i.e. enough phase margin (at least 45 degrees typically), of the open-loop transfer function, will be stable according to the control theory [28]. The power electronic converters ruled by the second-order or higher-order boundary control law are inherently stable because the switching surface is between the refractive region and the reflective region [35].

1.1.4 The bandwidth-switching frequency ratios

The dynamic characteristics during a large transient depend on both the rising time related to the large-signal bandwidth and the settling time associated with the small-signal bandwidth. The ratio of bandwidth (BW) and the switching frequency (f_{SW}) can be presented by the bandwidth-switching frequency ratio as $\frac{BW}{f_{SW}}$. The large-signal bandwidth-switching frequency ratio can be presented as $\frac{f_{BW}}{f_{SW}}$, where f_{BW} is the large-signal bandwidth or power bandwidth. The small-signal bandwidth-switching frequency ratio can be presented as $\frac{f_{BW,s}}{f_{SW}}$, where $f_{BW,s}$ is the small-signal bandwidth. A high $\frac{BW}{f_{SW}}$ indicates a fast dynamic response when the switching frequency remains the same or a lower switching frequency when the dynamic response is similar.

Theoretically, the small-signal bandwidth-switching frequency ratio when using the linear control is around 10% to 20% [28][29], while the small-signal bandwidth-switching frequency ratio of the nonlinear control using second-order boundary control can achieve 60% approximately [46].

Linear control needs a much higher switching frequency than nonlinear control to accomplish the same small-signal bandwidth, which will lead to higher switching loss as well as a more significant heat sink requirement. With the same switching frequency, linear control's lower small-signal bandwidth indicates a longer settling time.

The large-signal bandwidth-switching frequency ratio ($\frac{f_{BW}}{f_{SW}}$) is much smaller than the small-signal bandwidth-switching frequency ratio ($\frac{f_{BW,s}}{f_{SW}}$) since the slew rate of the system limits the large-signal bandwidth. For example, the commercial switching power amplifier with a switching frequency of 125 kHz from EGSTON has a small-signal bandwidth-switching frequency ratio ($\frac{f_{BW,s}}{f_{SW}}$) of 16% while a large-signal bandwidth-switching frequency ratio ($\frac{f_{BW}}{f_{SW}}$) of 4% [55]. Therefore, a linear controller can realize a large-signal bandwidth-switching frequency ratio ($\frac{f_{BW}}{f_{SW}}$) much lower than 10%. Boundary control using the ideal switching surface will have the fastest dynamic response, minimum delay time and no settling time when the transients happen [6][25][26], which also indicates a high $\frac{f_{BW}}{f_{SW}}$ and $\frac{f_{BW,s}}{f_{SW}}$.

To summarize, the inherent stable boundary control has the fastest dynamic response and minimum delay time for a transient step. Compared to linear control, it will have a higher bandwidth with the same switching frequency and no settling time during a transient. Therefore, designing a fast power amplifier, boundary control is preferred.

However, instantaneous computation is the ideal case to realize boundary control accurately. The control law of boundary control requires high computing power and the controller hardware to implement the boundary control algorithm is critical to achieving a real-time computation.

1.1.5 Controller Hardware Implementation

The controller hardware to implement the control algorithm can be an analog circuit or a digital processor. Analog controllers have been widely used in past years in the power electronic system [32]. Analog controllers have the advantages of continuous signal processing and instant calculation [33]. However, digital control implements have dominated in recent years due to its benefits, including high flexibility, compatible with a digital system, less sensitive to noise, the ability of reprogramming, less cost and less developing time[32][33][38]. Typically, there are three types of digital processors: general-purpose microcontrollers, Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs). Since general-purpose microcontrollers have relatively less cost-efficiency than DSPs and FPGAs, the primary hardware solutions are DSPs and FPGAs in power electronic applications [33].

DSP is a specialized CPU in signal processing and a software solution, which enables it processing a large number of diverse functions by given enough processing time. FPGA is a hardware solution with the ability of gate-level reconfiguration, which allows the processing of the tasks in the fastest way, a quasi-instantaneous calculation, by sacrificing the hardware or the gate resources. Figure 1-5 shows the use domain of DSPs and FPGAs. Algorithm complexity indicates there are a considerable number of functions, and most of them are different functions. DSP is more suitable for high algorithm complexity than FPGA. Different functions occupy a part of the hardware resources and the employed hardware resource is functionally specific and can be used to process other functions. Therefore, FPGA will fail to achieve all the functions because of a lack of resources. Time constraint is another factor of controller design. FPGA is preferred when the control algorithm has more parallel functions and fewer data-dependent process or series process since it has the parallel architecture and can be configured multicores to process the parallel

functions. Figure 1-6 shows a case that both DSP and FPGA processes two groups of tasks. Each group has three tasks. The tasks in the same group are independent with each other, while the second group of tasks relies on the results of the first group. The T_{FPGA} and T_{DSP} are the period for FPGA and DSP to complete one task, respectively. Since the FPGA can configure and optimize the hardware structure to minimize the processing time for each task, T_{FPGA} is less than T_{DSP}. Furthermore, the tasks in the same group can be parallel processed. Therefore FPGA's execution time for all the tasks is much less than DSP's. However, if the tasks are large and complicated and the resources of FPGA are not sufficient to fit all the tasks, then FPGA is a failure for the control algorithm, while DSP can still successfully implement all the tasks. Furthermore, if all the tasks are in a serial calculation architecture, the programming in FPGA will be difficult and complicated.

For power electronic applications, the control algorithms are mostly located in the intersection area shadowed in Figure 1-5, which means both solutions are capable [33]. The designer has to choose between these two possible solutions to maximize the benefits from the controller hardware based on the nature and characteristics of the control algorithm, the desired performance and the cost.

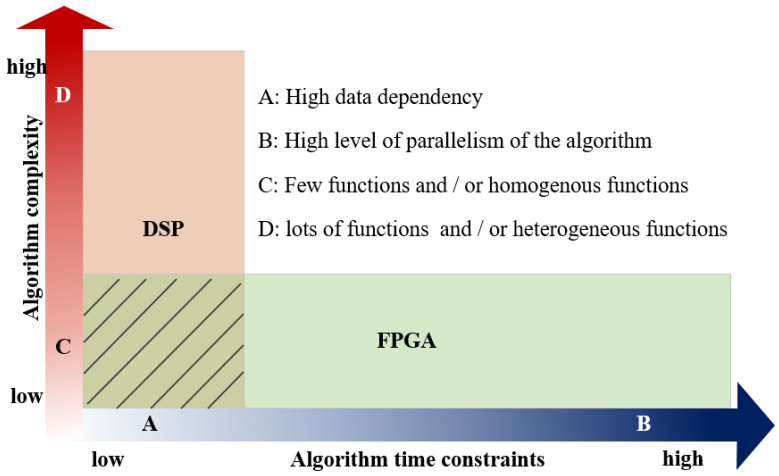


Figure 1-5: The Use Domain of DSP and FPGA Controllers [33]

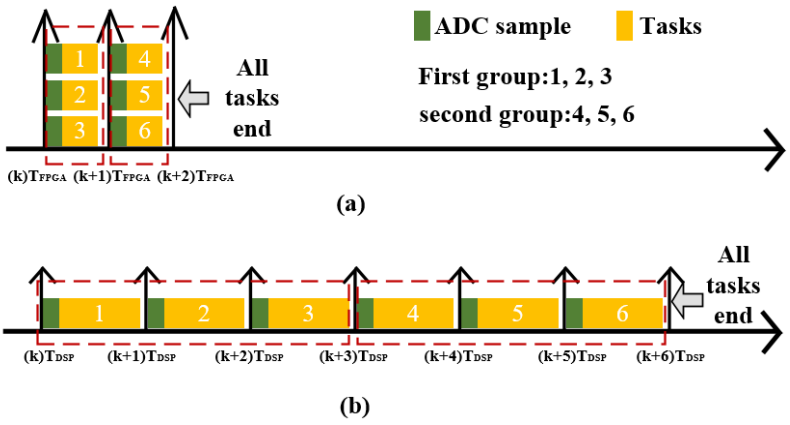


Figure 1-6: Timing Distribution of DSP and FPGA Controllers

Second-order boundary control is preferred to design a high bandwidth power amplifier, as mentioned in section 1.1.3. The control algorithm has two control criteria to guide the turn-on and turn-off switching actions respectfully and request instantaneous calculations to receive all the advantages. Fast control hardware is preferred. FPGA-based controllers with the parallel execution architecture shorten the processing time extremely and can reach a similar performance of analog counterparts without their drawbacks, i.e. lack of flexibility and vulnerable to noises [33]. Nevertheless, high-speed and accurate sampling components are also essential to build a fast system with digital solutions, which requires analog-to-digital converters (ADCs) with a high sampling rate. Most DSPs have a built-in ADC with multiple channels. Because the multiple channels have to share the same ADC, the sampling rate of each channel reduces. Using external ADCs is hard for DSPs since they have limited GPIOs and fixed peripheral connections, while it is easy for FPGAs since it has abundant GPIOs and flexible peripheral connections. However, FPGA is not as popular as DSP, the software solution due to the complexity of hardware programming.

A high bandwidth power amplifier is essentially a fast power electronics converter, most commonly VSC or inverter. Researchers have implemented inverters using second-order boundary control, which will be reviewed in the next section.

1.1.6 Boundary Control Implementation

Boundary control first proposed in the 1970s is a geometric control method based on a large-signal approach [30]. It aims at improving the transient response and the robustness of the power electronic converters. Second-order boundary control has the advantage of fast dynamic performances compared to first-order ones and less complexity compared to high-order ones, which is preferred in the design of a high bandwidth power amplifier, as mentioned in section 1.1.3. Researchers have implemented second-order boundary control in the various topology of power electronic converters, i.e. DC-DC, DC-AC converters, to improve dynamic responses [34]-[49].

Table 1-2 lists the implementation of second-order boundary control for inverters. In the early years, researchers implemented the control algorithm using analog circuits since the analog controller has fast reactions [36] [37]. In this analogue implementations, the switching frequency can achieve 25 kHz and the change from one operating point to another is completed in two switching actions within a minor period, i.e. in microseconds. In [39], the authors employed a high-end ARM-based processor with high-sampling-rate ADCs externally as the controller hardware to achieve a similar switching frequency as the analog controllers. Different types of low-cost DSPs with built-in ADCs were employed to implement the second-order control algorithm in [40] [41][45]-[49]. The switching frequency of the inverters with a DSP-based controller achieved no more than 20 kHz. Meanwhile, the transient responses were not as good as the ones with analog controllers. In [49], the authors have compared the dynamic performance

between boundary control and PI and PR control showing the transient period of the inverter with PI or PR control is ten times longer of that with boundary control. In [46] and [48][39], the authors inspected the system bandwidth. A small-signal transfer function was developed to represent the second-order boundary control, and the small-signal bandwidth-switching frequency ratio is 0.625 in [46].

Table 1-2: Implementation of Second-order Boundary Control for Inverter

Paper	*Year*	*Control Platform*	*Switching Frequency*	*Sampling rate*	*Transient time*	$\frac{f_{BW,s}}{f_{SW}}$
[36]	2005	analog circuit	11kHz to 25kHz[1]	-	400 us[3]	-
[37]	2007	analog circuit	25kHz	-	73 us[4]	-
[39]	2007	ARM-Based Processor [5]	12kHz to 22kHz	10MHz[6]	150 us[7]	-
[40]	2008	DSP[8]	3.6kHz	360 kHz[9]	-	-
[41]	2009	DSP[10]	2.5kHz(average)	40kHz	512.5 us[11]	-
[45]	2014	DSP[12]	20kHz	-	66us (simulation) [13]	-
[46]	2016	DSP[14]	8 kHz	450 kHz	shorter than 1 ms[15]	0.625
[49]	2019	DSP[16]	4kHz(average)	300 kHz	320 μs[17]	-

The notes, including the explanations and the details, are attached in Appendix A.

In conclusion, the previous researches have proved the boundary control has a much better dynamic response than the linear control, i.e. PI control and PR control. A higher switching frequency indicates a higher bandwidth [46]. The existing researches have achieved the switching frequency around 25 kHz. A switching power amplifier or inverter using second-order boundary control with the switching frequency above 25 kHz is not yet available. Moreover, the frequency

response and large-signal bandwidth of second-order boundary control need more inspection and analysis.

1.2 Motivations of the Thesis

The advanced power electronic technology allows switching power amplifiers applicable for industrial applications like the power interface of PHIL simulations. However, in comparison with linear amplifiers, the bandwidth and the dynamic response are significantly lower and slower, respectively. Therefore, a fast control technique is in demand for the switching power amplifier with high control bandwidth and fast dynamic response.

Conventionally, there are three general limitations of control bandwidth for a switching power amplifier. Firstly, control hardware is usually a low-cost DSP, for which the built-in ADC and computation speeds are limited. Secondly, the control algorithm is typically a Proportional-Integral (PI) or similar type of linear controller. The dynamic response is limited by the "Integral" stage, which contributes to a long settling time after a transient. Thirdly, the semiconductor switches are not able to switch at high frequency with high power operation due to high switching losses and challenging thermal requirements.

Recently, three key technologies have been developed to solve the above problems. First, an FPGA is a fast and programmable control hardware platform. It can give quick actions since they are hardware switches internally [50]. Secondly, Boundary Control is a kind of non-linear control based on the converter switching trajectories to determine switching actions. Although the controller can give a swift dynamic response in principle, the control algorithm needs high computing power, which is relatively heavy for a DSP controller [34]. Finally, the development of Wide Bandgap power semiconductors allows converters to work at high switching frequency with

high power ratings [22]. This innovative combination can minimize transient time and realize a high bandwidth power amplifier for industrial applications.

The research objective of this thesis is using a GaN-based inverter with a boundary control scheme in an FPGA platform to realize a high bandwidth switching power amplifier with high bandwidth-switching frequency ratios.

1.3 Organization of the Thesis

This thesis is organized into five chapters. A brief introduction of the chapters is as follow:

Chapter 1: Introduction – This chapter presents background information related to the research work described in this thesis, review of literature and research motivation and objectives. The three key considerations to build a high bandwidth power amplifier are the semiconductor, the control method and the controller hardware. The introduction, review and comparison are presented in terms of power semiconductor switches, the linear control and nonlinear control, precisely boundary control, and the different controller hardware. A literature review of boundary control based inverters summarizes the existing work, and together with the three key considerations, the research objective of the thesis is formulated accordingly. The contribution of the thesis concludes this chapter.

Chapter 2: Operation Principle – This chapter focuses on the operation principle of the high system bandwidth power amplifier proposed in the thesis. The control theory for the proposed system is presented. Operation principle of the second-order boundary controller is explained, and the control criteria to guide the turn-on and turn-off switching actions are derived. The steady-state, dynamic characteristics and system bandwidth are discussed.

Chapter 3: Implementation Consideration – This chapter discusses the limitations of second-order boundary control, including the load limitation due to the assumptions and the non-ideal factors affecting the performance of the controller. The load limitation determines the operation range of the boundary control; the non-ideal factors include measurement inaccuracy and delay time; the methods of delay time compensation are discussed. The existence of the delay time limits the ceiling of the switching frequency.

Chapter 4: Experiments and Results – The complete experimental results are present in this chapter. The experimental setup and the design specification is described. The waveforms from oscilloscope, plots and figures from gain-phase analyzer are used to understand the dynamic behaviour of the proposed power amplifier.

Chapter 5: Conclusion and Future Work – This chapter summarizes the contribution of this thesis as well as key conclusions that are drawn from the studies conducted. It also discusses some of the potential future extensions.

1.4 Research Contributions

This thesis proposed an innovative combination of a GaN-based inverter and a boundary controller implemented in an FPGA to realize a high bandwidth power amplifier for industrial applications. The main contributions of this research are summarized below:

- A thorough literature review has been conducted to gather background information on the three critical units to build a high-bandwidth power amplifier with high bandwidth-switching frequency ratios to conceive the original research idea and present the motivation behind this research work.

- The proposed power amplifier platform shows fast dynamic responses and a higher switching frequency than that of systems with DSP-Based or analog controllers in the current research work of boundary control inverters.

- The influences of the non-ideal factors when implementing boundary control in a hardware device are discussed and analyzed firstly in the research area of boundary control. The proposed compensation method to mitigate the negative influence on the performance of the boundary control from the delay time in the measurement and computation has been verified experimentally. This research result is a guide for designers to select hardware components for design a high bandwidth power amplifier, i.e. ADC, current sensor, operational amplifier and controller hardware, for realizing specific performance by a power electronic system with boundary control.

- The proposed analytical method to estimate system bandwidth with boundary control based on the frequency response of the RLC circuit and the specification of the system has been discussed and verified by experiment results. This estimation method is useful to analyze the bandwidth in the design stage.

- These contributions led to the following conference paper.

  Z. Zhang, C. Ho, and W. Xiao, "An FPGA-based Switching Power Amplifier using Boundary Controller to achieve High System Bandwidth," *IEEE ECCE2019*, Sept. 2019.

Chapter 2 Operation Principle

The objective of this chapter is to review the operation principle of the second-order boundary controller, derive control criteria to guide the turn-on and turn-off switching actions, and discuss the steady-state, dynamic characteristics and the system bandwidth.

2.1 System Architecture

A typical full-bridge voltage source inverter has been used in this thesis shown in Figure 2-1. It consists of a DC voltage source, full-bridge switches, an LC filter and an output load. The bipolar technique has been used to generate the gate signals to the full-bridge switches; therefore, the two switches in the same leg are switching alternately. Figure 2-2 shows the operating mode of the system: *Mode I* is the circuit configuration when the switches S1, S4 are on and S2, S3 are off, and *Mode II* is the circuit configuration when the switches S2, S3 are on and S1, S4 are off. From the power amplifier point of view, the reference (v_{ref}) is required to be amplified and the output voltage (v_O) is the amplified result. *G* is the gain of the amplifier.

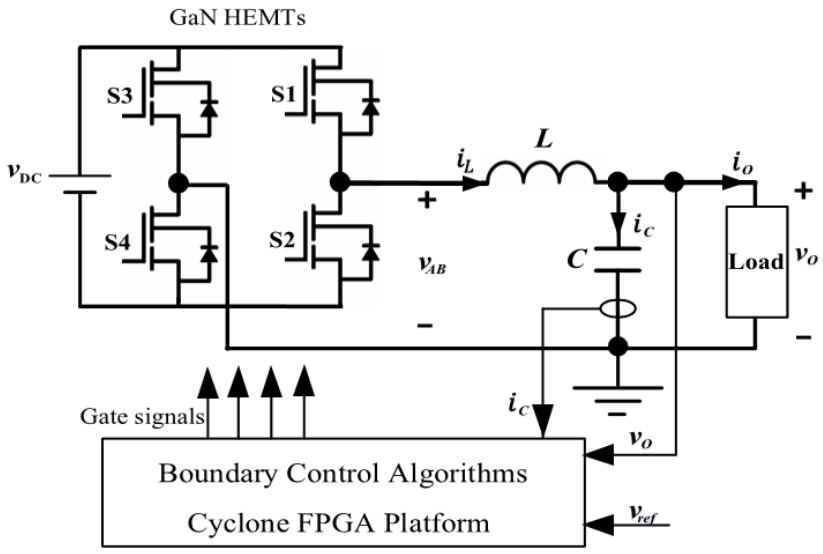
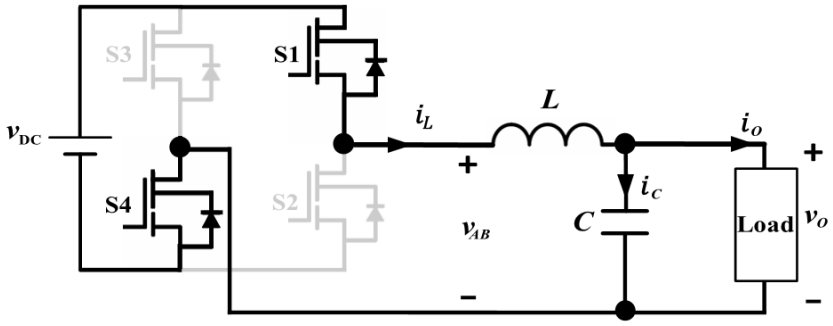
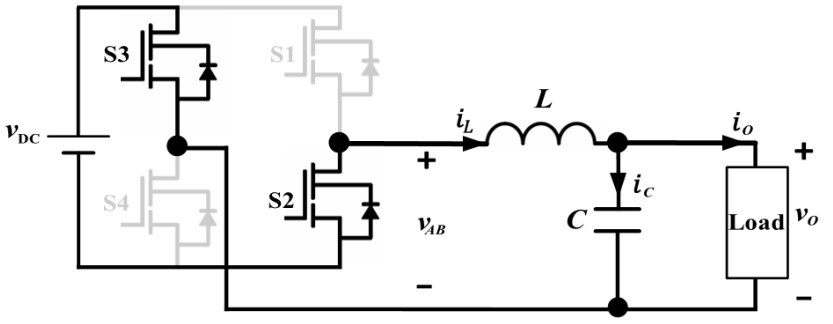


Figure 2-1: The Block Diagram of a High System Bandwidth Power Amplifier



(a)



(b)

Figure 2-2: The Operating Mode: (a) *Mode I*, (b) *Mode II*

2.2 Control Strategy

The second-order boundary control law is employed to control the output voltage in this thesis. A similar method has been used in [34]-[39]. The assumptions for the second-order boundary law are constant output current and voltage in steady-state, as follow:

$$\frac{di_o}{dt} = 0 \text{ and } \frac{dv_o}{dt} = 0$$

The ideal waveforms in steady-state operation are shown in Figure 2-3.

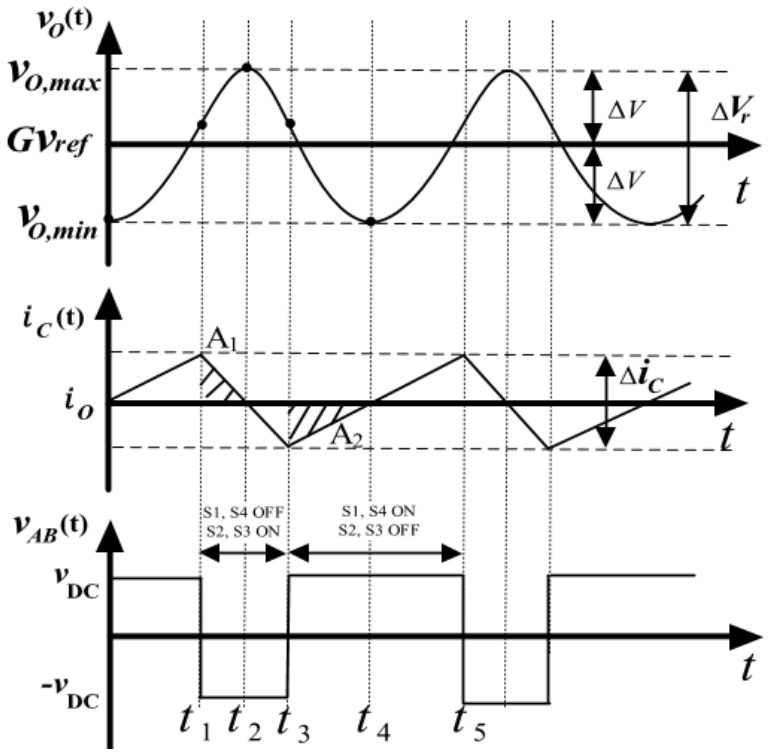


Figure 2-3: Waveforms in Steady-State Operation

The turn-on criteria guide the system to change from operating in *Mode II* to *Mode I* and turn-off criteria guide the system to change from operating in *Mode I* to *Mode II.* The turn-on criteria and turn-off criteria are indicated in (1) and (2), respectively. The upper limit ($v_{O,max}$) and lower limit ($v_{O,min}$) for the output voltage (v_O) are calculated from reference (v_{ref}) and a voltage band (ΔV). i_C represents the capacitor current. The output voltage (v_O) is also the capacitor voltage (v_C).

$$v_O(t) \leq v_{O,min} + \frac{L}{2C}\frac{i_C^2(t)}{v_{DC}-v_O} \text{ and } i_C(t) \leq 0 \quad (1)$$

$$v_O(t) \geq v_{O,max} - \frac{L}{2C}\frac{i_C^2(t)}{v_{DC}+v_O} \text{ and } i_C(t) \geq 0 \quad (2)$$

Where $v_{O,min} = Gv_{ref} - \Delta V$ and $v_{O,max} = Gv_{ref} + \Delta V$

$v_{O,max} - v_O(t_1)$ is equal to $\frac{A1}{C}$, where $A1$ is the integration of $i_C(t)$ from t_1 to t_2. Since $\frac{di_o}{dt} = 0$, $\frac{di_C}{dt} = \frac{di_L}{dt} - \frac{di_o}{dt} = \frac{di_L}{dt} = \frac{v_{DC} - v_O}{L}$ and $\frac{1}{C}\int_{t_1}^{t_2} i_C(t)dt = (\frac{L}{2C}\frac{1}{v_{DC}-v_O})i_C^2(t)$. When the turn-off criteria in (2) are satisfied, the controller will send gate signals to turn off S1 and S4 and turn on S2 and S3.

$v_O(t_3)$ -$v_{O,min}$ is equal to $\frac{A2}{C}$, where $A2$ is the integration of $i_C(t)$ from t_3 to t_4. Since $\frac{di_o}{dt} = 0$, $\frac{di_C}{dt} = \frac{di_L}{dt} - \frac{di_o}{dt} = \frac{di_L}{dt} = \frac{v_{DC} + v_O}{L}$ and $\frac{1}{C}\int_{t_1}^{t_2} i_C(t)dt = (\frac{L}{2C}\frac{1}{v_{DC}+v_O})i_C^2(t)$. When the turn-on criteria in (1) become true, the controller will send gate signals to turn on S1 and S4 and turn off S2 and S3.

2.2.1 Steady State

In the steady-state, the output voltage (v_O) and current (i_O) consider being constant. Based on Figure 2-3, the duty ratio (*D*), inductor current ripple (Δi_L) capacitor voltage ripple (Δv_C) and switching frequency (f_{sw}) can be derived as (5), (7), (8) and (11).

Duty ratio

The output voltage v_O is the average value of v_{AB}. The duty ratio is the ratio of the Mode I period and the whole switching period T_{sw}. During DT_{sw}, the value of v_{AB} is v_{DC} and during (*1- D*)T_{sw}, the value of v_{AB} is -v_{DC}, therefore v_O will be

$$v_O = v_{DC}D + (-v_{DC})(1 - D) \quad (3)$$

$$D = \frac{1}{2}\left(\frac{v_O}{v_{DC}} + 1\right) \quad (4)$$

When considering the output voltage v_O controlled to be a sinewave $v_O(t) = V_o\sin(\omega t)$, where the V_o is the peak value of the output voltage. The duty ratio in this case is

$$D = \frac{1}{2}\left(\frac{V_o\sin(\omega t)}{v_{DC}} + 1\right) \quad (5)$$

Inductor current ripple

The inductor current ripple is the same as the capacitor current ripple since the output current is constant. Since $2\Delta V = \frac{1}{C}\int_{t_2}^{t_4} i_C(t)dt = (\frac{L}{2C}\frac{1}{v_{DC}+v_O})(\frac{1}{2}\Delta i_C)^2 + (\frac{L}{2C}\frac{1}{v_{DC}-v_O})(\frac{1}{2}\Delta i_C)^2$, the ripple can be calculated as follow

$$\Delta i_L = \Delta i_C = 2\sqrt{\frac{4\Delta VC}{\frac{1}{k_1}+\frac{1}{k_2}}} = \sqrt{\frac{8C({v_{DC}}^2-{v_o}^2)\Delta V}{Lv_{DC}}} \tag{6}$$

$$\Delta i_L = \Delta i_C = \sqrt{\frac{8C({v_{DC}}^2-{V_O}^2\sin^2(\omega t))\Delta V}{Lv_{DC}}} \tag{7}$$

Where $k_1 = \frac{v_{DC}-v_C}{L}$, $k_2 = \frac{v_{DC}+v_C}{L}$

Capacitor voltage ripple

The capacitor voltage ripple is the same with the output voltage ripple controlled by the hysteresis band ΔV, and the equation is as follow:

$$\Delta v_C = 2\Delta V \tag{8}$$

Switching frequency

One of the characteristics of a boundary controller with a fix hysteresis band is the varying switching frequency since there is not a clock but the turn-on and turn-off criteria to govern the switching period. The switching frequency has reciprocated relation with the inductor current ripple and the capacitor voltage ripple. The derivation of switching frequency is as follow:

From t_2 to t_4, the output voltage difference is:

$$v_C(t_4) - v_C(t_2) = -\Delta v_C = -2\Delta V = \frac{1}{C}\int_{t_2}^{t_4} i_C dt$$

$$2\Delta V = \frac{T_{sw}\Delta i_C}{8C} = \frac{T_{sw}(\Delta i_L - \Delta i_O)}{8C} = \frac{T_{sw}\Delta i_L}{8C} \quad (9)$$

Take the equation (6) into (9)

$$f_{sw} = \sqrt{\frac{(v_{DC}+v_C)(1-D)}{16LC\Delta V}} \quad (10)$$

The average switching frequency $f_{sw,avg}$ can be calculated as (11). M=$\frac{V_o}{v_{DC}}$ is the modulation index, 0<M<1, and *T* is the signal Period. From the relationship between the modulation index and the switching frequency in (11), when the modulation index is larger the $f_{sw,avg}$ will be smaller.

$$f_{sw,avg} = \frac{1}{T}\int_0^T \sqrt{\frac{(1-\mathrm{M}^2\sin^2(\omega t))v_{DC}}{32LC\Delta V}}\, dt \quad (11)$$

2.2.2 Dynamic Characteristic

The output voltage is governed in the hysteresis band by the two control criteria. During the transient, only two switch actions are needed from one operating point to another operating point, which is the least switch actions to realize the change of the operating point. Figure 2-4 shows the system trajectories, which are the movements of capacitor voltage and inductor current when the switches turn on and turn off. There is a transient when the operating point changes from 1 to 2 with two switching actions indicated in the blue line with arrows.

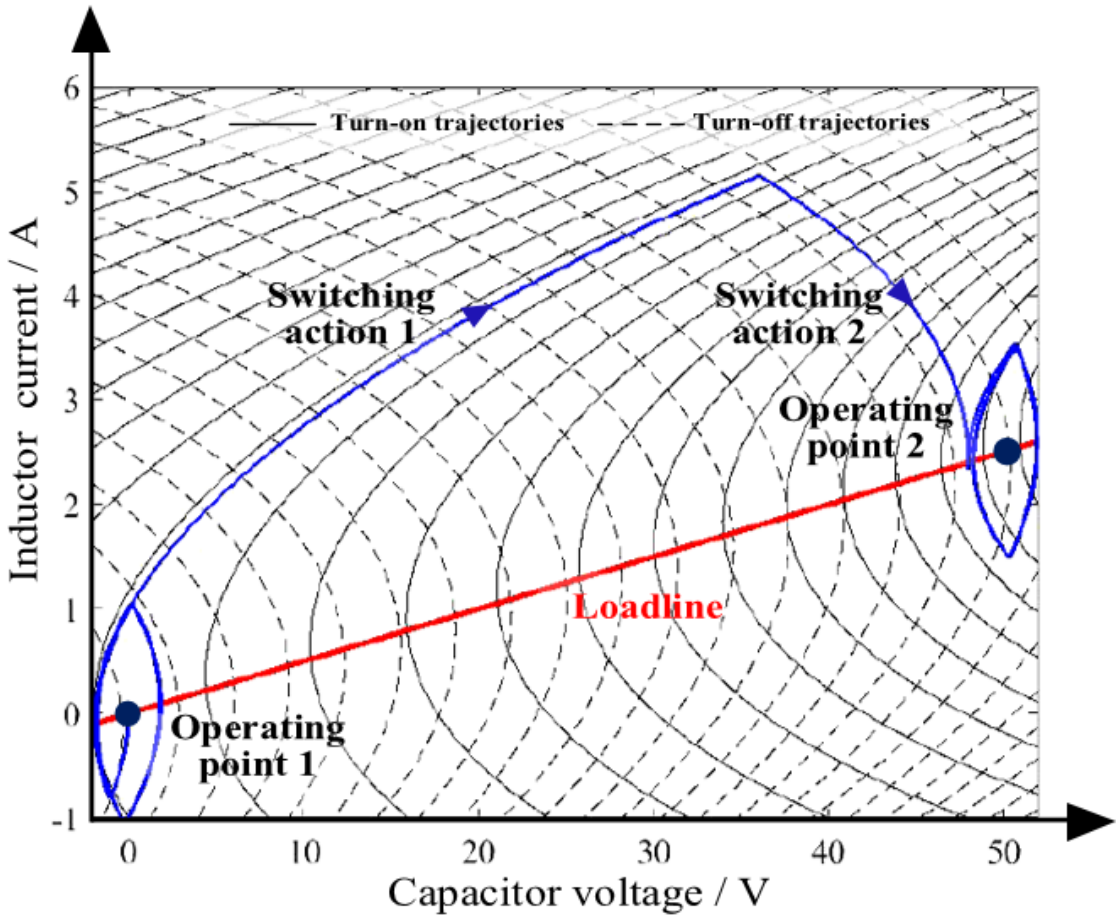


Figure 2-4: System Trajectories with Transient Actions

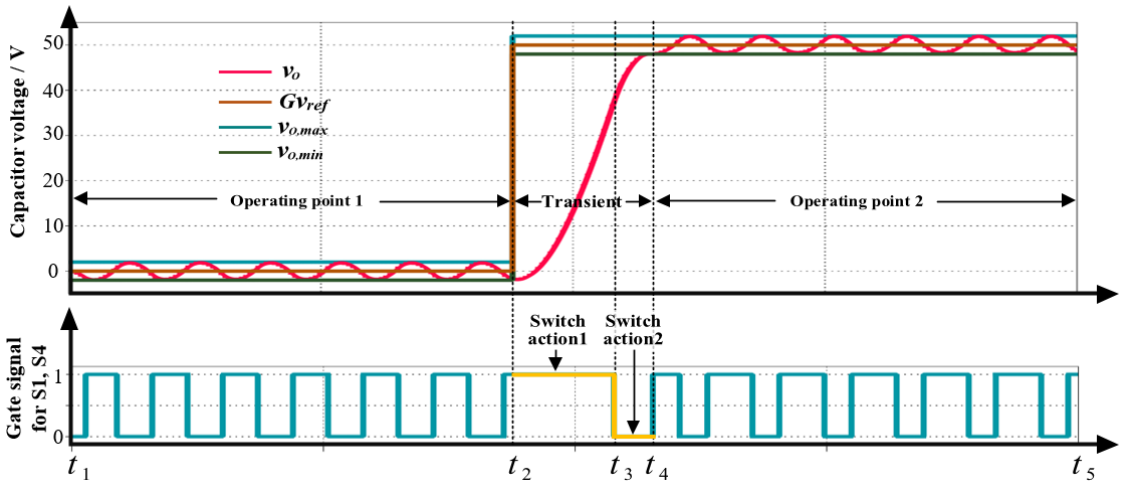


Figure 2-5: Transient Response in Time Domain

Figure 2-5 shows the switching sequences and the output voltage before, during and after a transient. The scenario is the same as Figure 2-4. From t_1 to t_2 , the system is in the operating point 1. At t_2 a step change of the reference appears, and the transient is from t_2 to t_4. From t_4 to t_5 , the system is in the operating point 2. Note that when the reference voltage suddenly changes at t_2, the system starts to track the new operating point without the need to complete the switching cycle and the switching actions and the system will stay in *Mode I* long enough to reach the new operating point within two switching actions.

2.2.3 System Bandwidth

The overall system bandwidth is the frequency range that the output power maintains at least half of the full rating power. The output voltage is $\frac{\sqrt{2}}{2}$ of the rated voltage when the power is half of the rating power, indicating that the system bandwidth (f_{BW}) is the frequency at the -3dB point in the frequency response of output voltage. Figure 2-6 shows the simulation waveform when the output voltage reduces to $\frac{\sqrt{2}}{2}$ of the rated voltage under the second-order boundary control. At this scenario, the switching frequency is equal to the frequency of the reference signal and the v_{AB} is a square wave with the frequency of f_{BW} and the duty ratio of 50%.

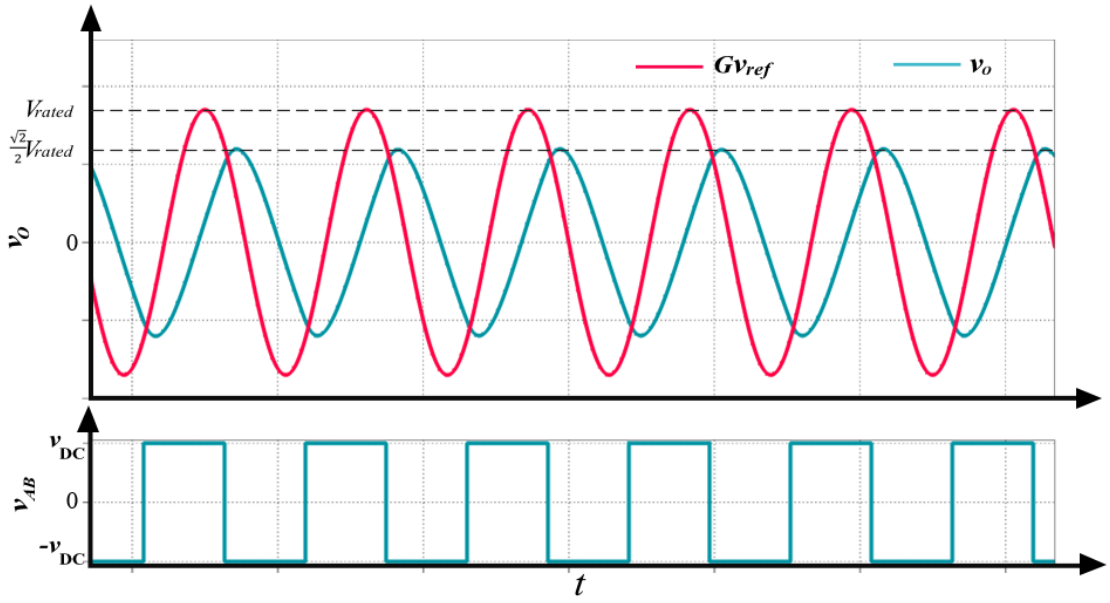


Figure 2-6: The Waveform of the Output Voltage at -3dB Point

The RLC circuit shown in Figure 2-1 has a low-pass filter feature. Each frequency component of voltage v_{AB} will has a certain gain when passing through this RLC circuit. The gain is less or equal to one since the circuit is a low pass filter. The magnitude of the component at f_{BW} in pulsating voltage v_{AB} provides is $\frac{4}{\pi}v_{DC}$ according to the Fourier series analysis of v_{AB} in ((12).

$$v_{AB}(t) = \frac{4}{\pi}v_{DC}\sum_{k=1}^{\infty}\frac{sin((2k-1)\omega t)}{2k-1} = \frac{4}{\pi}v_{DC}\left(sin(\omega t) + \frac{1}{3}sin(3\omega t) + \frac{1}{5}sin(5\omega t) + \cdots\right) \quad (12)$$

Where $\omega = 2\pi f_{BW}$.

Therefore, the gain (G_{AB}) for the reference signal with the frequency of f_{BW} from v_{AB} is $20\log(\frac{4}{\pi}\frac{v_{DC}}{Gv_{ref}})\ dB$ in the logarithmic scale. This gain comes from the power plant with the second-order boundary control. RLC circuit acting as a low-pass filter will degrade the magnitude of components with different frequency in v_{AB}. By adding G_{AB}, overall gain at f_{BW} will exactly reach -3 dB. Then the system bandwidth of the proposed system is the frequency when the RLC circuit gain is $-3\text{dB} - G_{AB}$ in (13), when the switching frequency is equal to the

signal frequency. f_{cutoff} is the cutoff frequency of the RLC filter. $F_{RLC}(gain)$ represents the RLC circuit frequency response, in this function, the gain is the variable, and the frequency is the result. Then the system bandwidth will be observed from the RLC circuit frequency response indicated in Figure 2-7. The LC value will limit the system bandwidth when $\frac{v_{DC}}{Gv_{ref}}$ maintains the same based on (13). When the LC value is smaller, the system bandwidth is larger.

$$f_{BW} = F_{RLC}(-3\text{dB} - G_{AB}) \approx f_{cutoff} + \frac{G_{AB}}{40\text{dB/decade}} \tag{13}$$

Where $G_{AB} = 20\log(\frac{4}{\pi}\frac{v_{DC}}{Gv_{ref}})\ dB$, $f_{cutoff} = \frac{1}{2\pi\sqrt{LC}}$

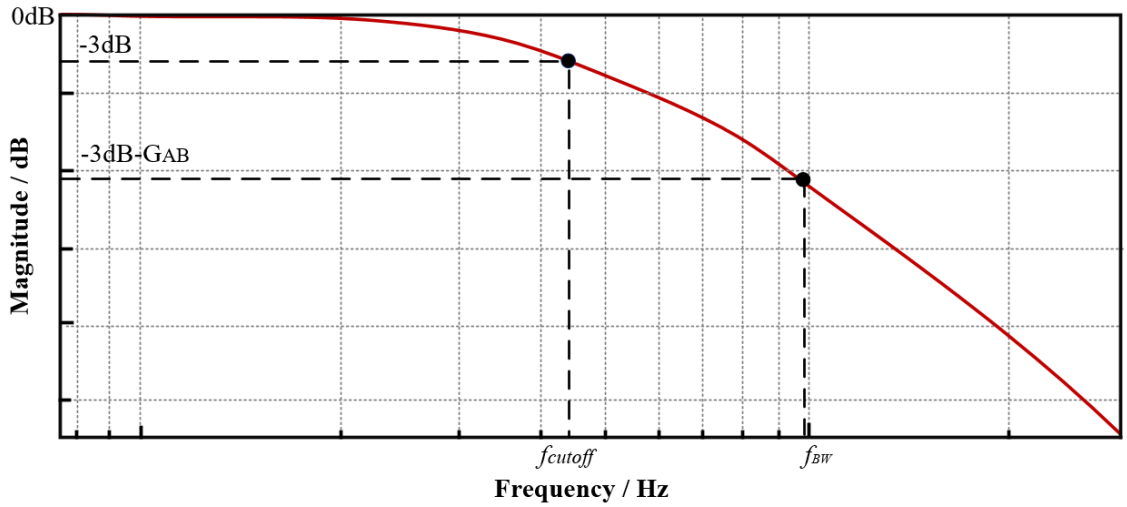


Figure 2-7: The Frequency Response of the RLC Circuit

The boundary controller system can work at the signal frequency to get a high gain, which will ensure the overall system bandwidth to reach a high bandwidth under specific R, L, C parameter values.

2.3 Chapter Summary

In this chapter, the operation principle of the proposed system and the control law of the second-order boundary control has been presented. The formulas for duty ratio, inductor current ripple, capacitor voltage ripple and switching frequency have been derived in the steady-state. The

dynamic characteristics of the system have been analyzed with the system trajectories. The system bandwidth has been analyzed by observing the simulation waveforms, and it can be determined by the frequency response of the RLC circuit, the DC source voltage and the output voltage. The estimation of the system bandwidth is vital in the design stage since the designer can use this information to design the parameters and specifications to fulfil the desired performances.

Chapter 3 Implementation Consideration

The objective of this chapter is to discuss implementation consideration of the system, including the load range, the output ripple size and the switching frequency. Firstly, the controller has a limited operating load range due to the assumption of second-order boundary control. Therefore, it is necessary to determine a suitable load range for the system. Secondly, the proposed controller requires accurate and instantaneous calculations and generates the gate signals immediately; however, non-ideal factors, especially the delay time, always exist, which will deteriorate the performance of the controller. The impact of the non-ideal factors is presented, and a delay time compensation method is proposed.

A brief block diagram of the system for implementation is shown in Figure 3-1.

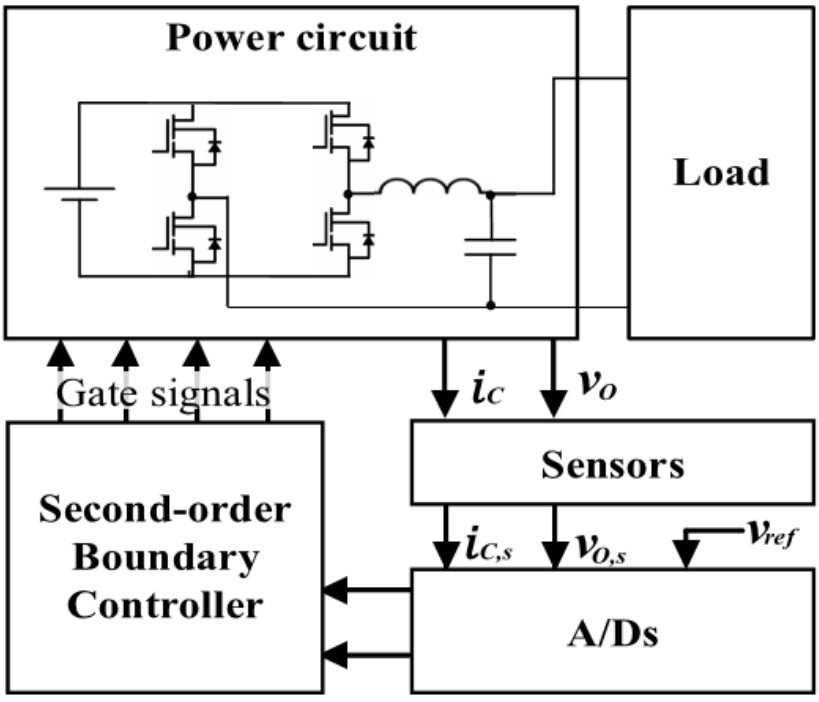


Figure 3-1: System Brief Block Diagram

3.1 Load Limitation

The second-order boundary control law assumes the output current constant in the steady-state in order to be independent of the load. The switching surface of the second-order boundary controller is an approximation to the ideal switching surface, which considers all the information of the circuit, including the load information. Since the load can be arbitrary, the second-order boundary control law is more practical. However, the deviation between the second-order switching surface and the ideal switching surface results in a longer transient period and more switching actions during large-signal disturbances.

Figure 3-2 shows the comparison of the second-order switching surface and the ideal switching surface under different load conditions in the plane of normalized capacitor voltage ($v_{C,N}$) and normalized capacitor current ($i_{C,N}$). R is the load and Z_C is the load when the RLC circuit is in critical damping, i.e. the damping factor $\zeta = 1$ and $Z_C = \frac{1}{2}\sqrt{\frac{L}{C}}$. The capacitor voltage is normalized by the voltage at the operating point as (14)

$$v_{C,N} = \frac{v_C}{Gv_{ref}} \tag{14}$$

The capacitor current is normalized as (15):

$$i_{C,N} = \frac{i_C}{Gv_{ref}/Z_C} \tag{15}$$

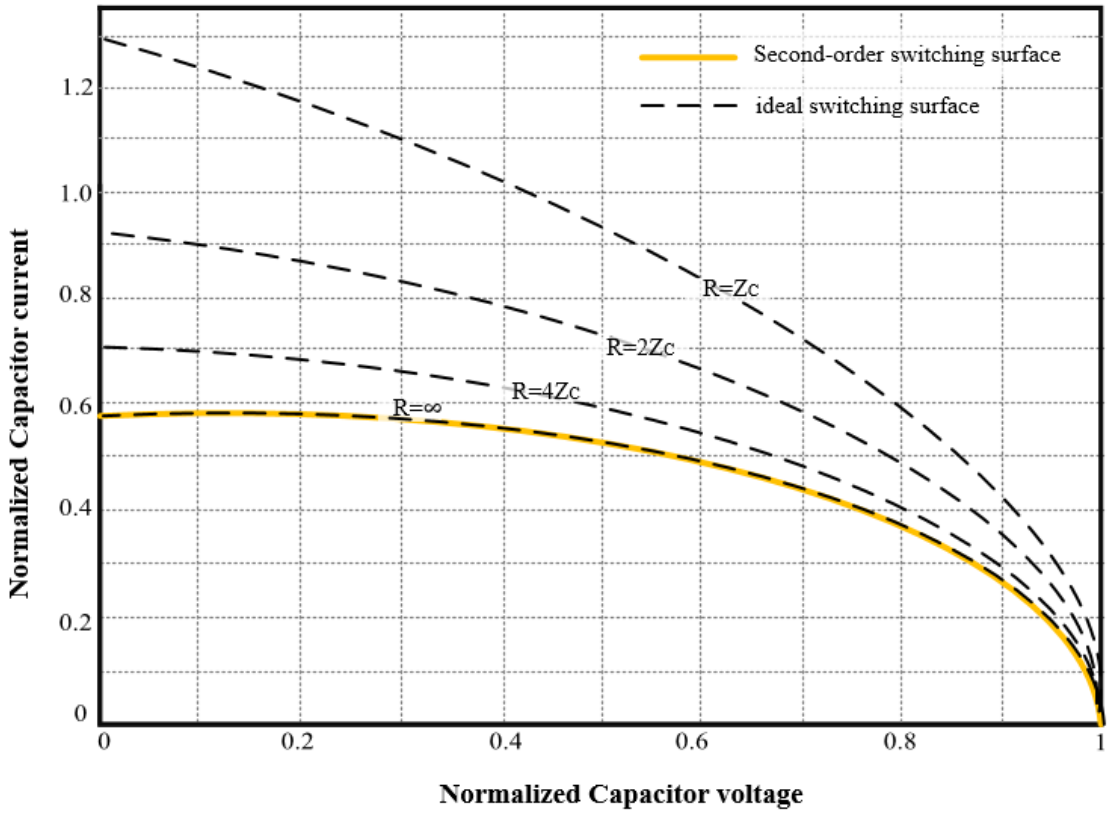


Figure 3-2: The Comparison of the Second-Order Switching Surface and the Ideal Switching Surface (Turn-Off Trajectories) under Different Load Conditions [37][42]

When the load is infinite, the second-order switching surface is the same as the ideal switching surface. As the load decreases, the deviation between the second-order switching surface and the ideal switching surface increases. These switching surfaces converge at $v_{C,N} = 1$, indicating that the behaviours of the system under different load conditions around the operating point with second-order boundary control is closed to the ideal case. The discrepancy when $v_{C,N}$ is away from 1 indicates second-order boundary control has performance deteriorations during large disturbances. To alleviate the performance deteriorations, the load to the system has a limitation. Z_C is considered the minimum resistive load (R_{min}) as (16) for the system since the system will be a critical damping system and have a fast transient without the expense of overshoot[37][42]. With the value of L and C, the maximum resistive load can be calculated.

$$R \geq R_{min} = Z_C = \frac{1}{2}\sqrt{\frac{L}{C}} \tag{16}$$

3.2 Non-Ideal Factors of Implementation

The fast response of second-order boundary control depends on accurate and instantaneous calculations. In reality, non-ideal factors of the control loop implementation make it impossible to realize accurate calculations instantaneously. The non-ideal factors include the measurement shifts, the limited-bandwidth of the sensors, discrete sampling, limited resolution and sampling rates, and computation time of the controller hardware. The non-ideal factors lead to either inaccurate data or a delay time substantially, which brings a phenomenon of a lower switching frequency and a more giant output voltage ripple. Section 3.2.1 will discuss the influence of ADC accuracy without considering the impact of the delay time. Section 3.2.2 will discuss the influence of delay time, and section 3.2.3 will introduce methods for the delay time compensation.

3.2.1 ADC Accuracy

There are two feedback signal measurements in the system, i_C and v_o. Since i_C has an average value of zero, the measurement is the ripple of i_C, whereas both the ripple and the average value of v_o need to be measured simultaneously, the accuracy of ADC for sampling output voltage is more critical to the boundary controller.

As a rule of thumb, the selected ADC should be at least five times more accurate of the total system accuracy as (17)[51].

$$\sigma_{ADC} \leq \frac{\sigma_{SYM}}{5} \tag{17}$$

σ_{SYM} describes the accuracy of the system and σ_{ADC} represents the accuracy of the ADC. In this thesis, the control objective is to keep the output voltage within the band, then σ_{SYM} can be represented as (18) and σ_{ADC} is presented in (19). $V_{r,o}$ is the observed ripple peak-to-peak value and $V_{r,d}$ is the designed ripple peak-to-peak value, which is $2\Delta V$ in Figure 2-3. The least significate bit (LSB) voltage V_{LSB} presents the output voltage resolution, and the ADC accuracy is usually 1LSB.

$$\sigma_{SYM} = \frac{V_{r,o} - V_{r,d}}{V_{r,d}} \times 100\% \tag{18}$$

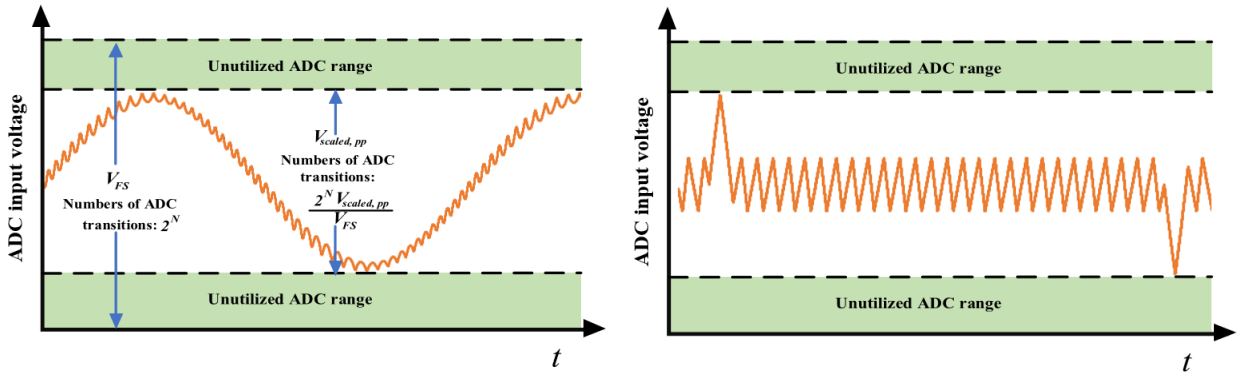
$$\sigma_{ADC} = \frac{V_{LSB}}{V_{r,d}} \times 100\% \tag{19}$$

The output voltage range ($V_{o,pp}$), i.e. 340V peak-to-peak is far higher than the full input range of ADC (V_{FS}), i.e. 4.096V peak-to-peak; therefore, it is necessary to scale down the output voltage to accommodate the input range of the ADC. The least significate bit (LSB) voltage V_{LSB} presenting the output voltage resolution is in (20).

$$V_{LSB} = \frac{r_{scale} * V_{FS}}{2^N} = \frac{V_{o,pp}}{2^N \eta} \tag{20}$$

$$\text{Where } r_{scale} = \frac{V_{o,pp}}{V_{scaled,pp}}, \eta = \frac{V_{scaled,pp}}{V_{FS}}$$

$V_{scaled,pp}$ is the scaled-down value of the output voltage and r_{scale} is the scale-down rate. *N* is the number of bits of the digital output of ADC, which presents the resolution of ADC. η is the utilization rate of the ADC input range shown in Figure 3-3. To leave a margin, i.e. 10%, for disturbances, η should be less than 100%, i.e. 90%.



(a) (b)

Figure 3-3: The Utilization of the ADC Input Range. (a) Sampled Capacitor Voltage, (b) Sampled Capacitor Current

The designed ripple size can be calculated as (21) from (17), (19) and (20).

$$2\Delta V \geq \frac{5V_{o,pp}}{2^N \eta \sigma_{SYM}} \tag{21}$$

To reach a certain σ_{SYM} with a designed $V_{o,pp}$, the ripple size is limited by (21). This relationship can be used to selected ADCs for sampling the signals.

3.2.2 Delay Time

In reality, the delay time (τ) always exists in signal sensing and sampling, computing and components' response. The overall delay time (τ_{total}) as (22) includes the delay time of the sensor circuits (τ_s), the sampling zero hold time (τ_z), the computation time (τ_c), dead time (τ_{dt}) and the response time of the semiconductor (τ_r).

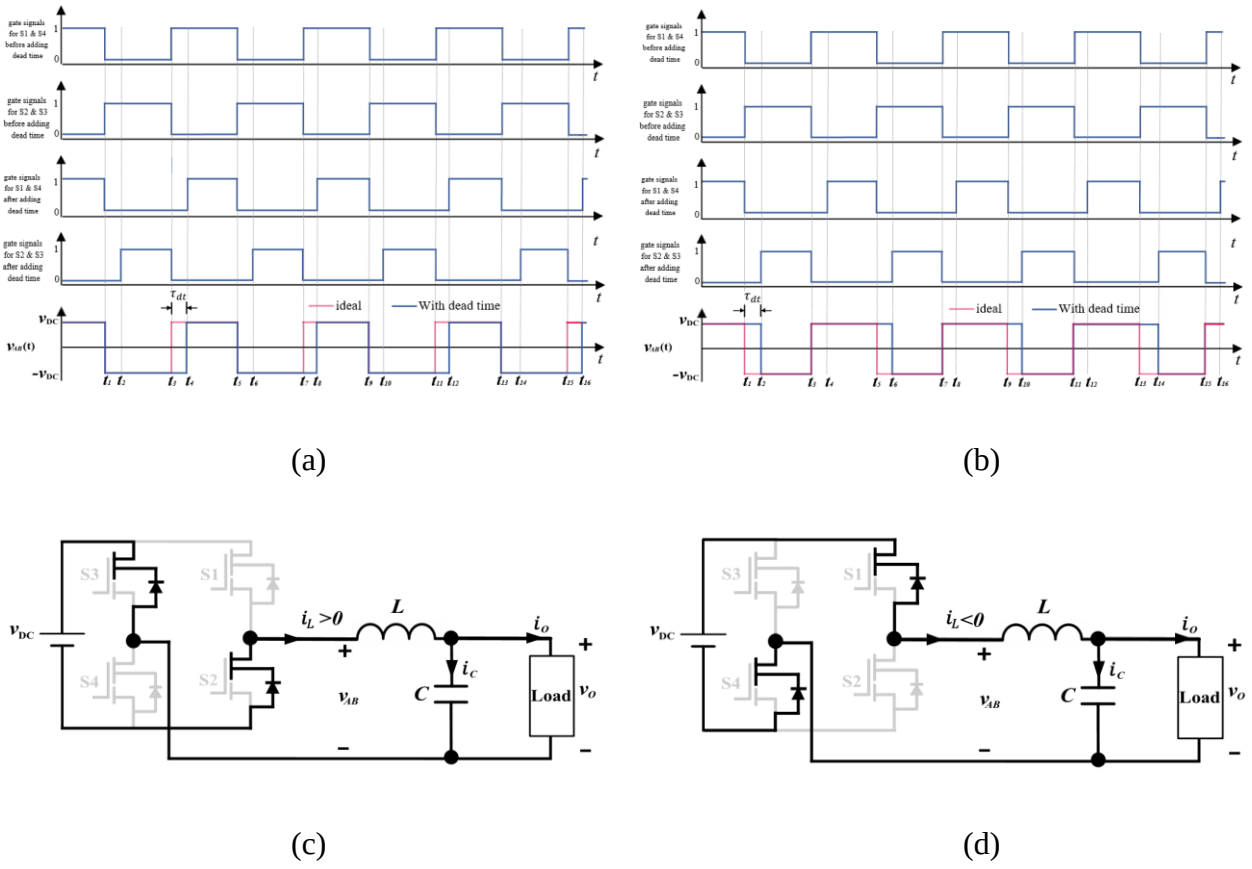
$$\tau_{total} = \tau_s + \tau_z + \tau_c + \tau_r + \tau_{dt} \tag{22}$$

In the implementation for boundary controller, the two feedbacks are i_C and v_o, the delays for sensing these two signals are $\tau_{s,i}$ and $\tau_{s,v}$. From the control laws in (1) and (2), i_C and v_o should be synchronized, therefore τ_s takes the larger value from $\tau_{s,i}$ and $\tau_{s,v}$ as in (23). The difference

between the $\tau_{s,i}$ and $\tau_{s,v}$ can be eliminated in the computing progress by shifting the sampling values of the signal with a delay of $|\tau_{s,i} - \tau_{s,v}|$.

$$\tau_s = \max(\tau_{s,i}, \tau_{s,v}) \tag{23}$$

The sampling zero hold time (τ_z) and the computation time (τ_c) will be the same for sampling both signal and for calculating the criteria of both *Mode I* and *Mode II* respectfully. The response time of the semiconductor (τ_r) depends on the semiconductor device.



(a) (b)

(c) (d)

Figure 3-4: Waveforms with Dead Time: (a) When $i_L > 0$, (b) When $i_L < 0$ and Circuit Topology During Dead Time: (c) When $i_L > 0$, (d) When $i_L < 0$

The dead time (τ_{dt}) is added between the switch of the *Mode I* and *Mode II* when all the semiconductor switches are turned off to prevent the possibility of a short circuit. Due to the dead

time, a delay time for v_{AB} exists shown in Figure 3-4. When $i_L > 0$ the circuit topology is shown in Figure 3-4 (c) and the dead time becomes a delay time when v_{AB} switches from $-v_{DC}$ to v_{DC} shown in Figure 3-4 (a) and when $i_L < 0$ the circuit topology is shown in Figure 3-4 (d) and the dead time becomes a delay time when v_{AB} switches from v_{DC} to $-v_{DC}$ shown in Figure 3-4 (b).

The delay time can be classified as two categories, τ_1 and τ_2 . $\tau_1 = t_2 - t_1$ is the delay time before the actual v_C reaches the peak and it comes from τ_{dt} , τ_c and τ_r and $\tau_2 = t_3 - t_2$ is the delay time after the actual v_C reaches the peak and it comes from τ_s and τ_z. Due to the difference between the τ_{dt} and τ_r when the value of v_{AB} switches, the delay time is τ_{on} when v_{AB} switches from v_{DC} to $-v_{DC}$ and τ_{off} when v_{AB} switches from $-v_{DC}$ to v_{DC}.

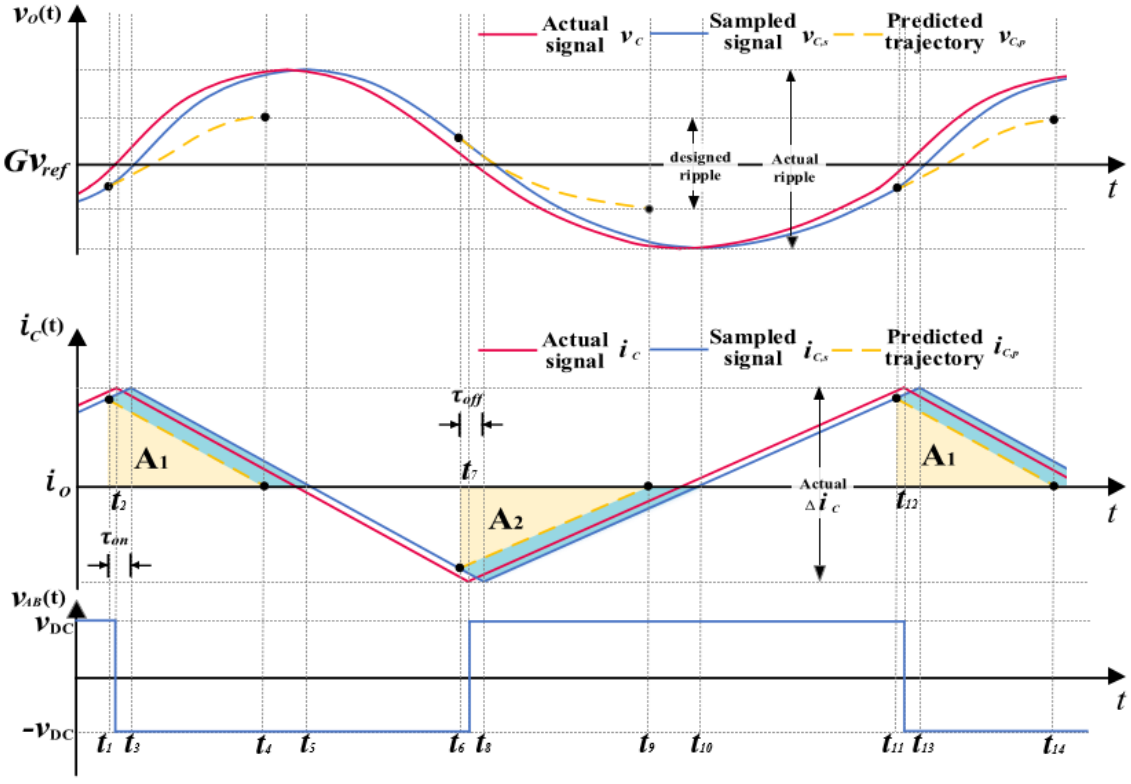


Figure 3-5: The Influence of the Delay Time on Boundary Control

The present delay time will defer the controller performance in practical from the ideal case, as shown in Figure 3-5. When the controller calculated (1) and (2) using the sampled the capacitor current and capacitor voltage at t_1, the turn-off criteria was fulfilled, and the controller predicted the trajectory would follow the yellow dash line as Figure 3-5 and the output ripple peak would reach the designed ripple peak at t_4. However, due to the delay time, the actual trajectory is following the red line. The blue line is the sampled signal with sensing delay and zero hold delay. The similar phenomenon happens when the turn-on criteria are fulfilled at t_6. From Figure 3-5, the actual output ripple ($V_{r,a}$) is larger than the designed ripple ($V_{r,d}$). Due to the relationship between the ripple and the switching frequency in (11), a larger ripple size contributes to a lower switching frequency. The difference ($V_{r,dff}$) of $V_{r,a}$ and $V_{r,d}$ can be calculated in (24) and the derivation of (24) is presented in Appendix A3 with the assumption of the output current and output voltage being constant and an implied condition that $V_{r,d} \geq 0$ or $V_{r,dff} \leq V_{r,a}$.

$$V_{r,dff} = \frac{1}{2C}\left(\frac{1}{k_2} + \frac{1}{k_1}\right)\left(2\left(\frac{1}{2}\Delta i_{C,a}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_1\tau_{on}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_2\tau_{off}\right)^2\right) \quad (24)$$

Where $k_1 = \frac{v_{DC}-v_C}{L}$, $k_2 = \frac{v_{DC}+v_C}{L}$

$\Delta i_{C,a}$ is the actual capacitor current and it can be calculated from (6) with the $\Delta V = 0.5V_{r,a}$ as (25).

$$\Delta i_{C,a} = \sqrt{\frac{4C(v_{DC}{}^2 - v_C{}^2)V_{r,a}}{Lv_{DC}}} \quad (25)$$

From (24), when τ_{total} is larger, $V_{r,dff}$ is larger. When $V_{r,d}$ is not far greater than $V_{r,dff}$, the delay time will have a dominated influence on the boundary controller. A large ripple is not desirable since it deteriorates the power quality. Therefore it is essential to compensate for this delay time.

3.2.3 Delay Time Compensation

One method for delay time compensation is to implement the output voltage ripple as $2\Delta V - V_{r,dff}$ into the digital controller, and then the actual ripple size or the observed ripple size is $2\Delta V$.

The implied condition that the implemented ripple $V_{r,i} \geq 0$ leads to a limitation for $V_{r,a}$ as (26) derived in Appendix B. To simplified the calculation, assume $\tau_{on} = \tau_{off} = \tau$.

$$V_{r,a} \geq \frac{\tau^2}{LC}\left(\sqrt{2v_{DC}} + \frac{2\sqrt{{v_{DC}}^3}}{\sqrt{{v_{DC}}^2 - {v_C}^2}}\right)^2 \tag{26}$$

$$\tfrac{1}{2}\Delta i_{C,a} = \left(k_1 + k_2 + \sqrt{2k_1k_2}\right)\tau \tag{27}$$

From (26), the actual output voltage ripple reached the minimum when the implemented ripple is zero and when the delay time increases the minimum value of $V_{r,a}$ increases when the other parameters are fixed. When $\frac{LC}{\left(\sqrt{2v_{DC}} + \frac{2\sqrt{{v_{DC}}^3}}{\sqrt{{v_{DC}}^2 - {v_C}^2}}\right)^2}$ is not much greater than τ^2, the delay time will have a dominated influence on the boundary controller. When implementing a zero ripple in the controller, the actual ripple can be observed experimentally, and the delay time can be derived from (26).

Another method delay time compensation is to turn on and turn off the switches using the corrected control criteria that include the delay information as (28) and (29). A similar delay time compensation concept is applied in [52][53][54]. Instead of using the area of the yellow part, the corrected criteria use the area of the shaded region to calculate the voltage difference between $v_O(t)$ and $v_{O,min}$ or $v_{O,max}$. Therefore, the actual trajectories of $i_C(t)$ and $v_C(t)$ will follow the predicted trajectories and the designed ripple size $V_{r,d} = 2\Delta V$ can be realized, as shown in Figure 3-6.

$$v_O(t) \leq v_{O,min} + \frac{1}{2C}\left(\frac{1}{k_2} + \frac{1}{k_1}\right)\left(\left(i_C(t) + \tau_{off}k_2\right)^2 - i_C^2(t)\right) \text{ and } i_C(t) \leq 0 \tag{28}$$

$$v_O(t) \geq v_{O,max} + \frac{1}{2C}\left(\frac{1}{k_2}+\frac{1}{k_1}\right)\left((i_C(t)+\tau_{on}k_1)^2 - i_C^2(t)\right) \text{ and } i_C(t) \geq 0 \quad (29)$$

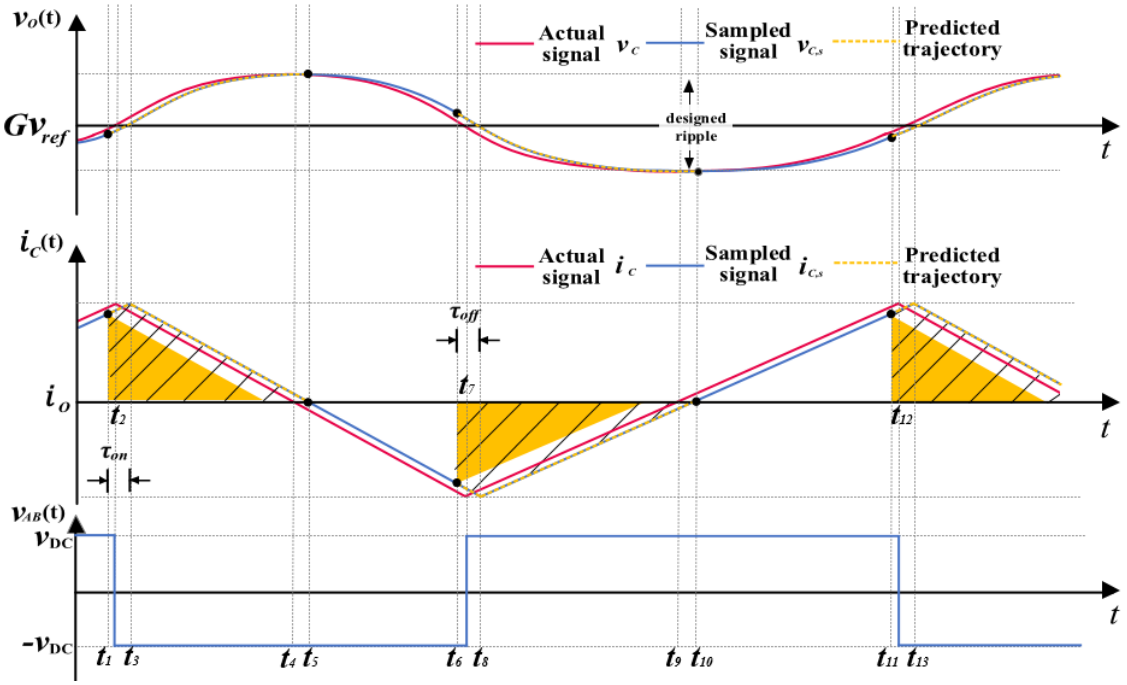


Figure 3-6: Waveforms Using the Corrected Control Criteria

The implied conditions of the corrected criteria are that at t_1 when the turn-on criteria are satisfied, $i_C(t_1) \geq 0$ and at t_6 when the turn-off criteria are met, $i_C(t_6) \leq 0$. The implied conditions limit the feasible V_r as (31) and when $i_C(t_1) = i_C(t_6) = 0$, the minimum V_r can be reached.

$$V_r \geq \max\left(\frac{1}{2C}\left(\frac{1}{k_2}+\frac{1}{k_1}\right)\left(\tau_{off}k_2\right)^2,\ \frac{1}{2C}\left(\frac{1}{k_2}+\frac{1}{k_1}\right)\left(\tau_{on}k_1\right)^2\right) \quad (30)$$

Since $k_1 = \frac{v_{DC}-v_C}{L}$ and $k_2 = \frac{v_{DC}+v_C}{L}$, and τ_{off} and τ_{on} will have similar value, i.e. assume $\tau_{on} = \tau_{off} = \tau$, the V_r is as (31).

$$V_r \geq \frac{1}{2C}\left(\frac{1}{k_2}+\frac{1}{k_1}\right)\left(\tau k_2\right)^2 = \frac{\tau^2}{LC}\frac{(v_{DC}+|v_C|)^2 v_{DC}}{v_{DC}{}^2 - v_C{}^2} \quad (31)$$

By calculating the difference between the minimum feasible V_r from both methods, the method with the corrected control criteria can realize a smaller V_r. Therefore, the minimum feasible V_r is

$\frac{\tau^2}{LC}\frac{(v_{DC}+|v_C|)^2 v_{DC}}{{v_{DC}}^2-{v_C}^2}$ as (31). To realize a certain V_r, the existing delay time (τ) will contribute a restriction for the value of LC and consequently the bandwidth of the system due to the relationship between the LC value and the system bandwidth in (13).

3.3 Chapter Summary

In this chapter, the implementation consideration of the system has been discussed. The implementation consideration is a guide to design the system parameters and select the components under a specification. ADCs with enough resolution should be selected to realize a particular voltage ripple with a reasonable system accuracy. To achieve a high-bandwidth system, a smaller L and C should be chosen; however, the value of L and C are bounded by the load limitation and the influence of the delay time. After defining the power rating and the source voltage the load value can be calculated and a suitable value of $\frac{L}{C}$ can be selected. The existence of the delay time worsens the performance of the boundary controller since the ripple size, and the switching frequency is limited. By using the corrected control criteria, a minimum voltage ripple can be realized, and after defining the voltage ripple, a suitable value of L and C can be selected. Note that the load limitation also bounds the value of L/C. The impact of the delay time also emphasizes the importance of using high-speed devices, i.e. using FPGA, for reducing the calculation time.

Chapter 4 Experiments and Results

In the previous chapters, the operation principle and the implementation consideration of the system have been presented. In this chapter, the theories and ideas are put into practice by subjecting the power amplifier prototype to various tests to verify and validate the design principles.

4.1 Experimental Setup

The boundary controller has been implemented with the Cyclone IV DE2-115 FPGA Board, as shown in Figure 4-1. The AD card EVAL-AD7356 and AD card DC1186A connect the FPGA board through the GPIO interface using the Serial Peripheral Interface (SPI) communication protocol. The AD card EVAL-AD7356 has two independent channels sampling at 5 MSPS, and the two channels will sample the output voltage (v_O) and the capacitor current (i_C). The AD card DC1186A is sampling at 500 KSPS which is used to sample the reference (v_{ref}) from a function generator or the Gain-Phase analyzer for frequency response study. The FIFO module synchronizes the sampled signals. The control algorithm generates signals indicating the correct time to turn on or turn off the switch pairs and an SR latch with a dead-time module is used to generate the gate signals to the switch pairs. The dead time is realized by adding a delay time before every turn-on action.

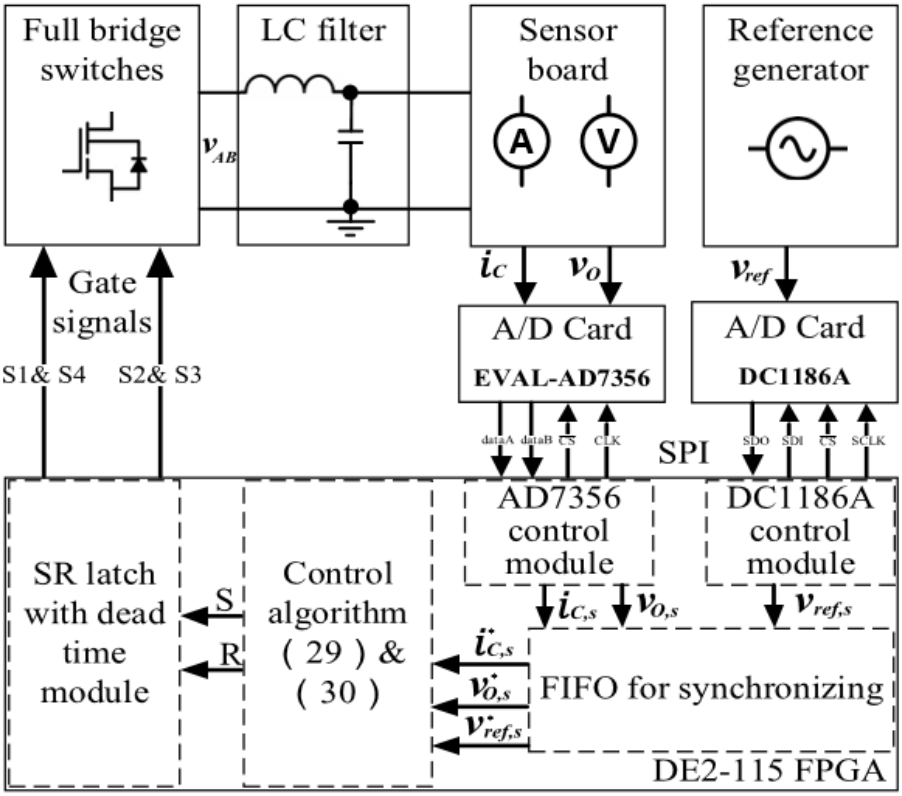


Figure 4-1: System Overall Block Diagram

The TDINV3000W050 from Transphorm is used as the power stage. The circuit block diagram is shown in Figure 2-1, including four cascade GaN-HEMTs and an LC filter. The power board has been verified under the open-loop test from the default demonstration. The current sensing circuit includes an LAH 25-NP current sensor and an operational amplifier circuit adjusting the scale ratio. The voltage sensing circuit consists of a voltage divider and a differential amplifier circuit. Table 4-1 listed the technical specifications of the experimental setup.

Table 4-1: Technical Specifications of the Experimental Setup

Parameters	**Symbol**	**Value / Maximum Rating**	**Units**
DC source voltage	V_{DC}	200	V
Rated output power	P_{rated}	1000	W
Rated output voltage RMS value	$V_{O,RMS}$	120	V

Voltage ripple peak to peak	V_r	12	V
Rated load	R	14.4	Ω
Amplifier gain	G	100	V/V
Reference signal RMS value	$V_{ref,RMS}$	1.2	Vrms
Reference signal frequency	f_{ref}	60	Hz
Output filter inductance	L	670	μH
Output filter Capacitor	C	1	μF

The ADC AD7356 used to sample the output voltage has a twelve-bit resolution. The system accuracy σ_{SYM} is set to be 10%. The output range is 352 V, which is the peak-to-peak output voltage plus the ripple size. The utilization rate of ADC η is 90%. According to (22) in section 3.2.1, $\frac{5V_{o,pp}}{2^N \eta \sigma_{SYM}} = 4.77V$, which is smaller than the designed voltage ripple. Therefore, the AD7356 is suitable to sample the feedback signals.

The value of the *L* and *C* is selected based on the load limitation and output voltage size limitation due to the overall delay time. According to (16) in section 3.1 , $\frac{1}{2}\sqrt{\frac{L}{C}} \leq R = 14.4$ as (32).

$$\frac{L}{c} \leq 829\ H/F \tag{32}$$

According to (31) in section 3.1 , with the delay time compensation by using the corrected control criteria, the minimum ripple is $\frac{\tau^2}{LC}\frac{(v_{DC}+|v_C|)^2 v_{DC}}{{v_{DC}}^2-{v_C}^2}$. Table 4-2 lists the breakdown delay time in the system. The ADC sampling zero hold time is the reciprocal of the sampling rate. The computation time is the number of clocks to complete the whole program in FPGA divided by the clock frequency. The delay time of the sensing circuits is measured by the gain-phase

analyzer (bode 100). The dead time is designed in the FPGA. The semiconductor response time is from the datasheet of the GaN switches. The current sensing circuit has a longer delay time and according to (23) in section 3.2.2 $\tau_s = \tau_{s,i} = 1.35\text{us}$. Considering the worst case when $v_C = \pm 170V$, $\frac{\tau^2}{LC}\frac{(v_{DC}+|v_C|)^2 v_{DC}}{v_{DC}{}^2 - v_C{}^2} = \frac{7676}{LC}$. The designed ripple must be larger than $\frac{7676*10^{-12}}{LC}$ as (33).

$$LC \geq 640 * 10^{-12}\ H * F \tag{33}$$

The selection of *L* and *C* must satisfy (32) and (33) and to achieve the highest system bandwidth the LC filter cutoff frequency should be the largest According to (13) in section 2.2.3, then the value of LC should be $640 * 10^{-12}$. However, considering the available choices for L and C in the laboratory, the final value for L and C is 670 uH and 1 uF, respectively, as in Table 4-1.

Table 4-2: The Breakdown Delay Time in the System

Parameters	**Symbol**	**Value / us**
ADC sampling zero hold	τ_z	0.2
FPGA computation	τ_c	0.1
Current sensing circuit latency	$\tau_{s,i}$	1.35
Voltage sensing circuit latency	$\tau_{s,v}$	0.7
Sensing circuit delay time	τ_s	1.35
Dead time	τ_{dt}	0.06
Semiconductor response time	τ_r	0.054
Overall delay time	τ_{total}	1.764

The physical power amplifier is implemented as the experimental setup shown in Figure 4-2. The DE2-115 FPGA board realizes the controller. The Transphorm GaN inverter forms the power circuit. The 5MSPS EVAL-AD7356 AD card samples the capacitor current and voltage. The 500KSPS DC1186A AD card samples the reference signal. Finally, a designed sensing board

measures and scales down the capacitor current and voltage to adapt the input range of the AD card.

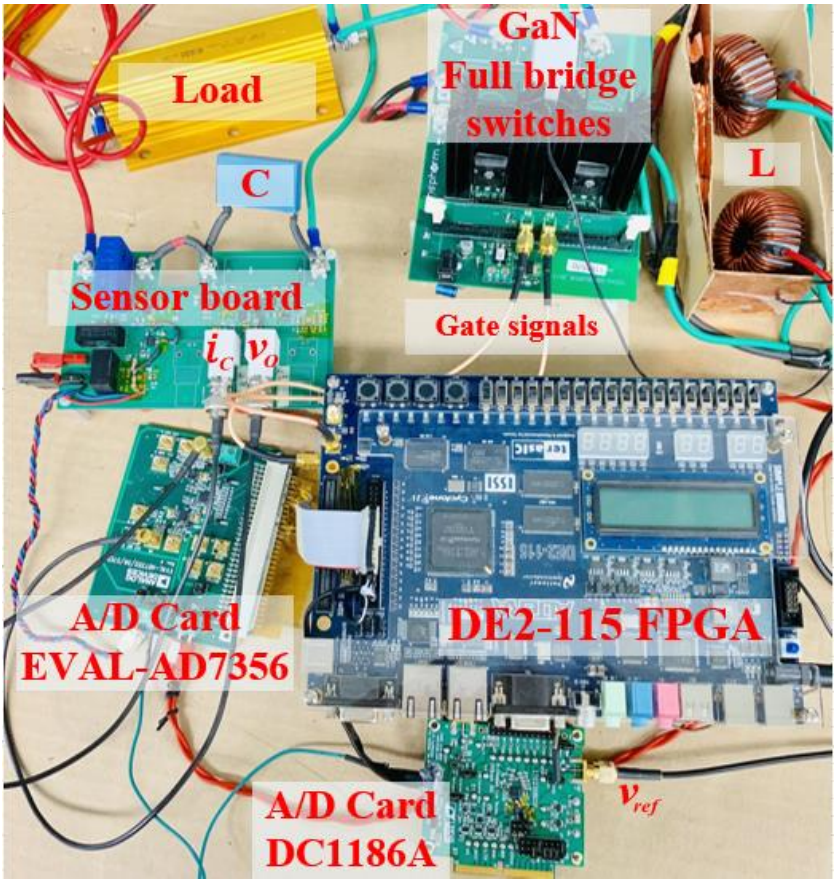


Figure 4-2: Experimental Setup

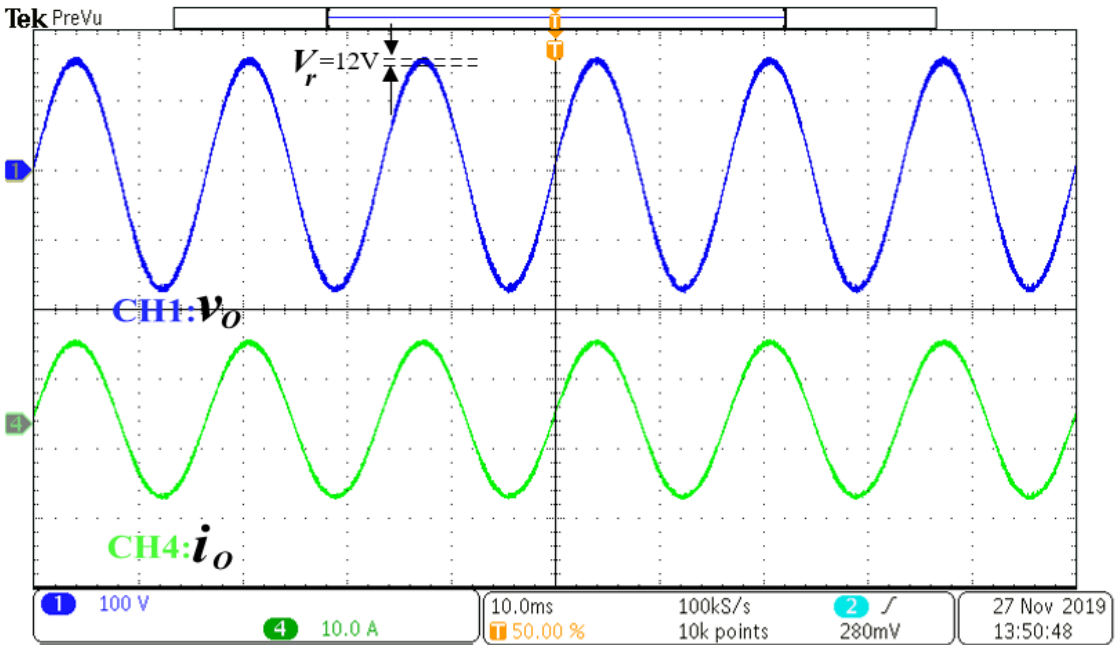
4.2 Experimental Results

4.2.1 Steady State

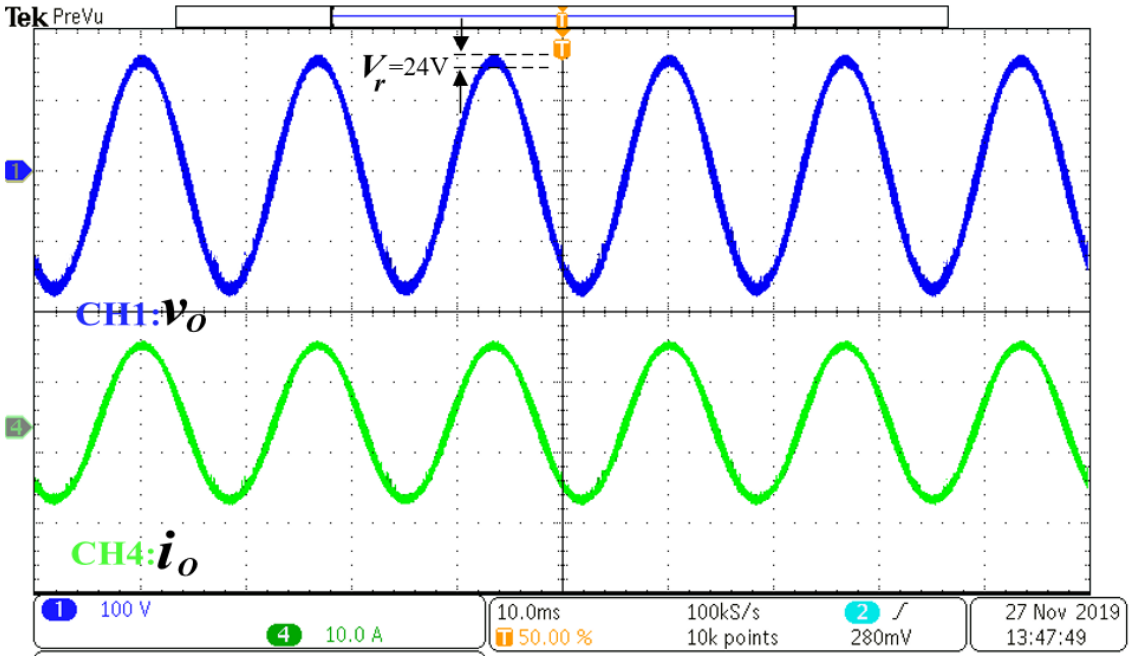
Figure 4-3 (b) shows the steady-state waveforms using the corrected boundary control criteria as (28) and (29) at the rated power with the output voltage of 120 Vrms and the load resistor of 14.4 Ω. The total harmonics is 1.2%, and the power efficiency is 97.78% measured by WT332E Yokogawa.

Figure 4-3 (a) shows the results using the corrected boundary control criteria as (28) and (29). The output ripple size is 12 V, and the average switching frequency is 30 kHz. Figure 4-3 (b) shows the results using traditional boundary control criteria as (1) and (2) with the implemented ripple size of zero. The realized ripple size is 24 V, and the average switching frequency is 21 kHz. Figure 4-3 (c) shows the results using traditional boundary control criteria without any delay compensation. The ripple size is 42 V, and the average switching frequency is 16 kHz. The switching frequency results match with the results calculated from (11), which are 30.8 kHz, 21.8 kHz and 16.5 kHz, respectively for (a), (b) and (c). Due to delay, the traditional boundary control criteria bring a more significant voltage ripple and lower switching frequency than the corrected boundary control criteria.

The overall delay time can be calculated analytically by (26) when using the traditional boundary control law with a zero ripple implemented in FPGA as the case in Figure 4-3 (b). The calculated delay is 1.721 us, which matches the measured delay. The difference between the actual ripple and design ripple at the reference peak can be calculated analytically from (24) and (25) to be 31.6 V. From the results in Figure 4-3 (c), the difference is 30V, which verifies the analytical method.


Tek PreVu
V_r=12V
CH1:v_o
CH4:i_o
1 100 V
4 10.0 A
10.0ms
50.00 %
100kS/s
10k points
2 280mV
27 Nov 2019
13:50:48

(a)


Tek PreVu
V_r=24V
CH1:v_o
CH4:i_o
1 100 V
4 10.0 A
10.0ms
50.00 %
100kS/s
10k points
2 280mV
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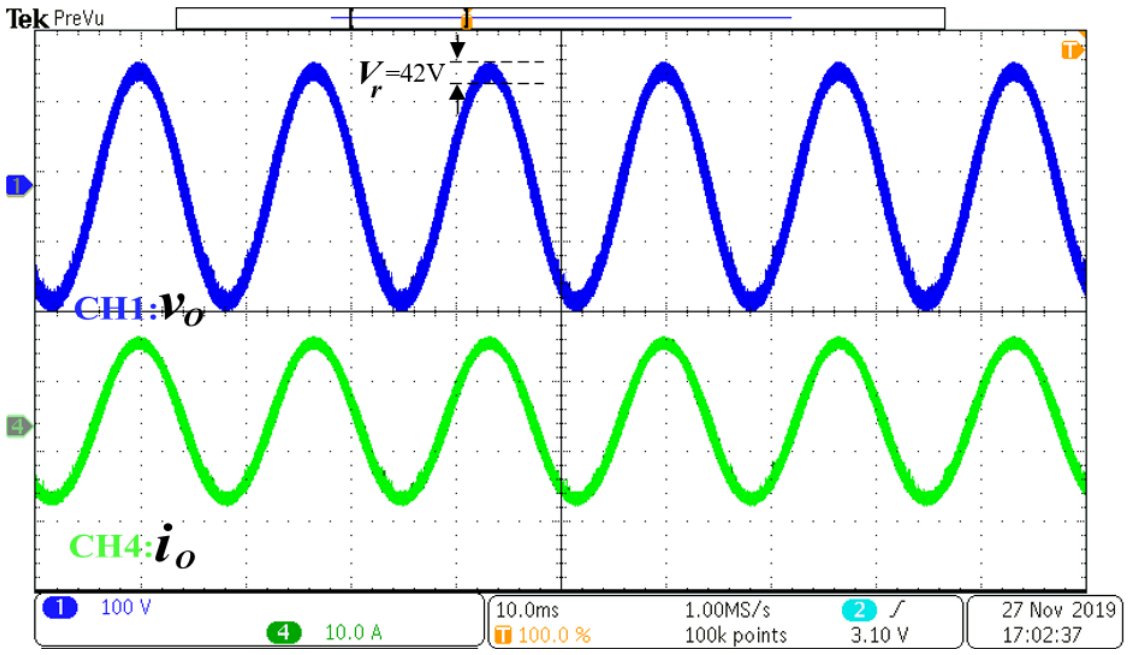
13:47:49

(b)



(c)

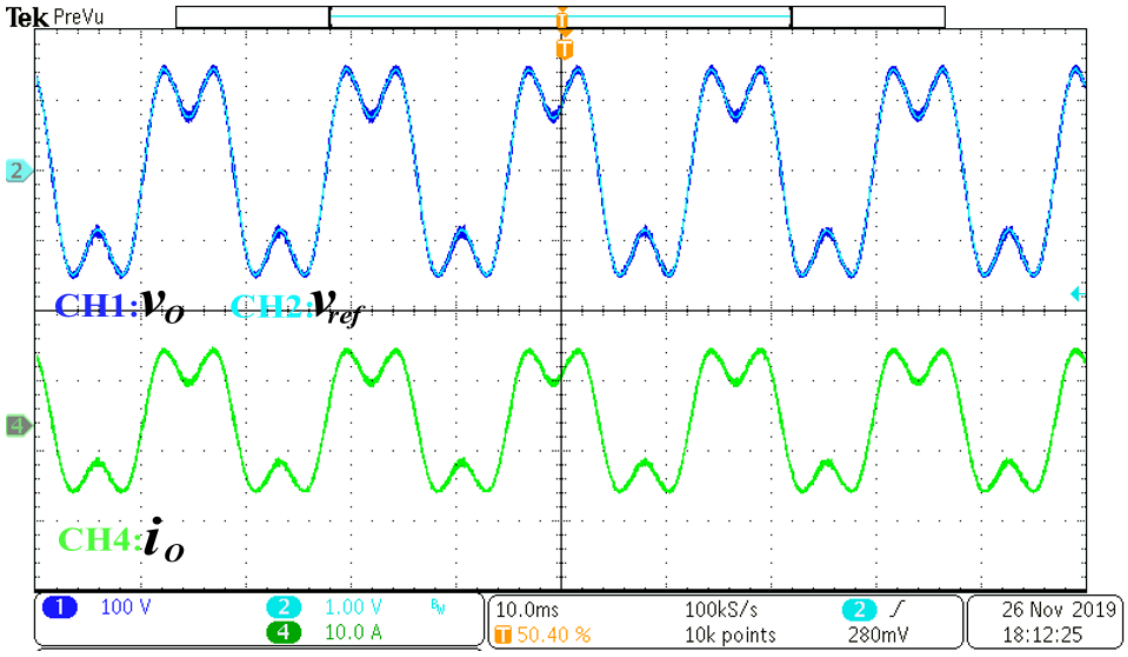
Figure 4-3: Steady-State Performance at the Rated Power: (a) with the Delay Time Compensation by the Corrected Control Criteria, (b) with the Delay Time Compensation by Zero Ripple Implemented, (c) with the Traditional Boundary Control Criteria

The switching frequency varies from 20 kHz to 40 kHz, and the average switching frequency reaches 30 kHz by using the proposed system platform with the corrected control criteria. While the reported maximum f_{sw} of boundary control implementing in a DSP is under 20 kHz, as shown in section 1.1.6.

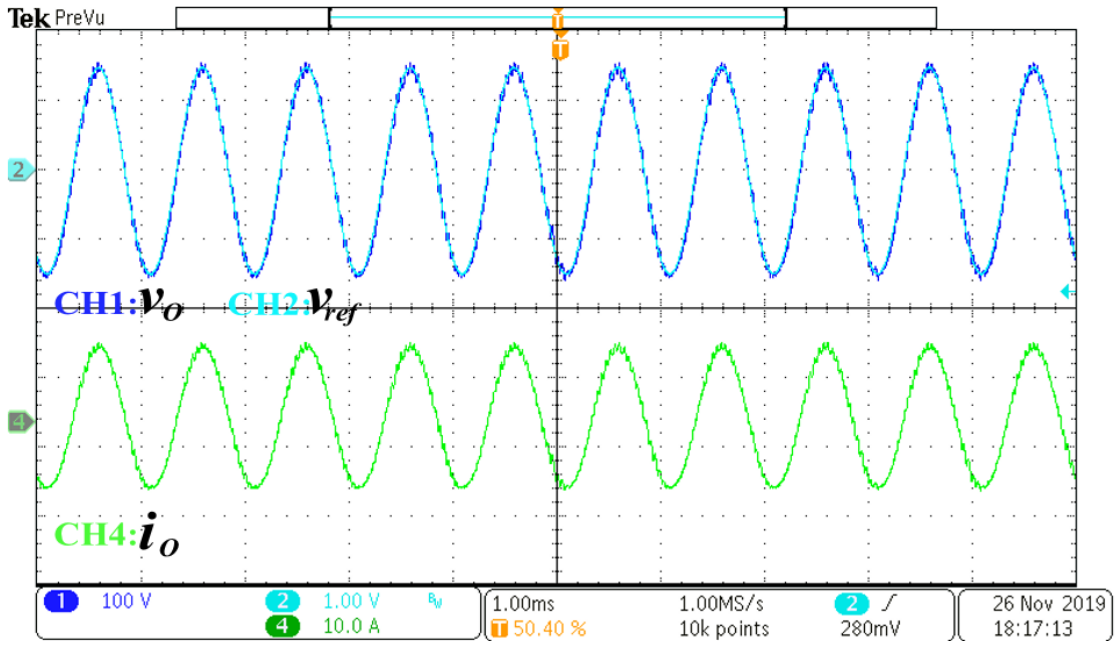
To complete the calculation of the boundary control criteria, an F28M35H52C DSP from Texas Instruments requires 1.25 us, which is 12 times longer than the DE2-115 FPGA. When replacing the DE2-115 FPGA with this F28M35H52C DSP, the total delay increases from 1.764 to 2.914 us. To realize the same ripple size, the value of LC requires increasing to at least $1746 * 10^{-12}$ (HF). And then, the LC cutoff frequency will reduce so to the system bandwidth, and the maximum

average switching frequency is 24 kHz with the corrected boundary control criteria. The output voltage ripple will be 33 V when keeping the same value of LC for maintaining the bandwidth.

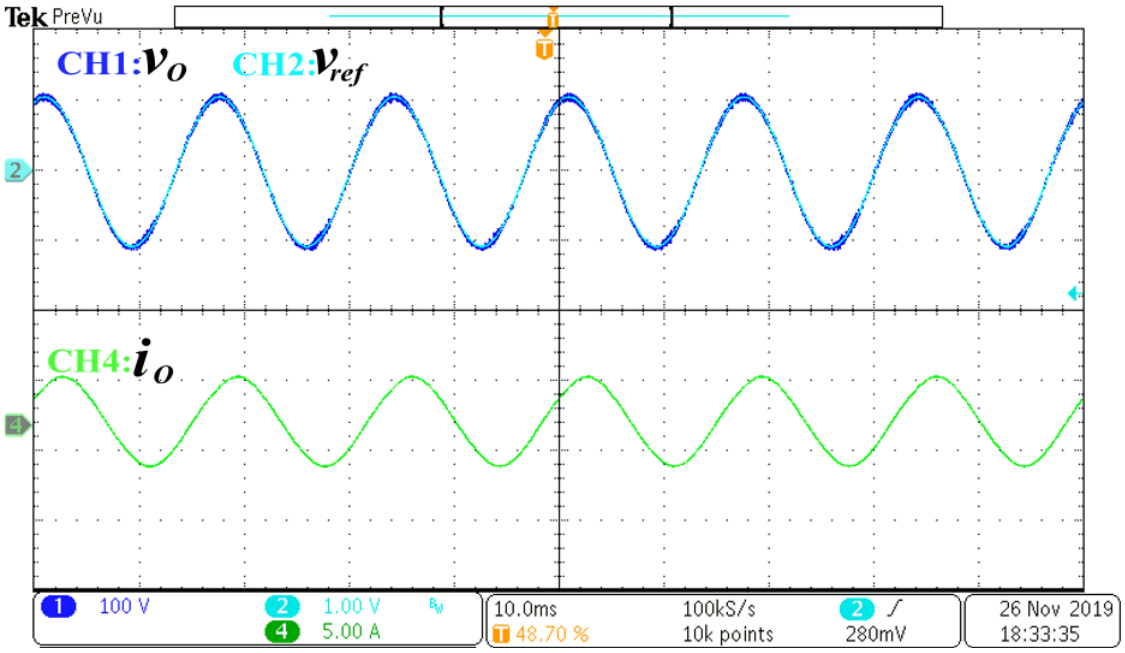
Figure 4-4 (a) shows the steady-state waveforms when the reference has a third-order harmonic component. Figure 4-4 (b) shows the steady-state waveforms when the reference has a high frequency, i.e.1 kHz. Figure 4-4 (c) shows the steady-state waveforms with an inductive load with the current lagging 37.5°. The waveforms indicate the output of the power amplifier follows the reference under different conditions.



(a)



(b)

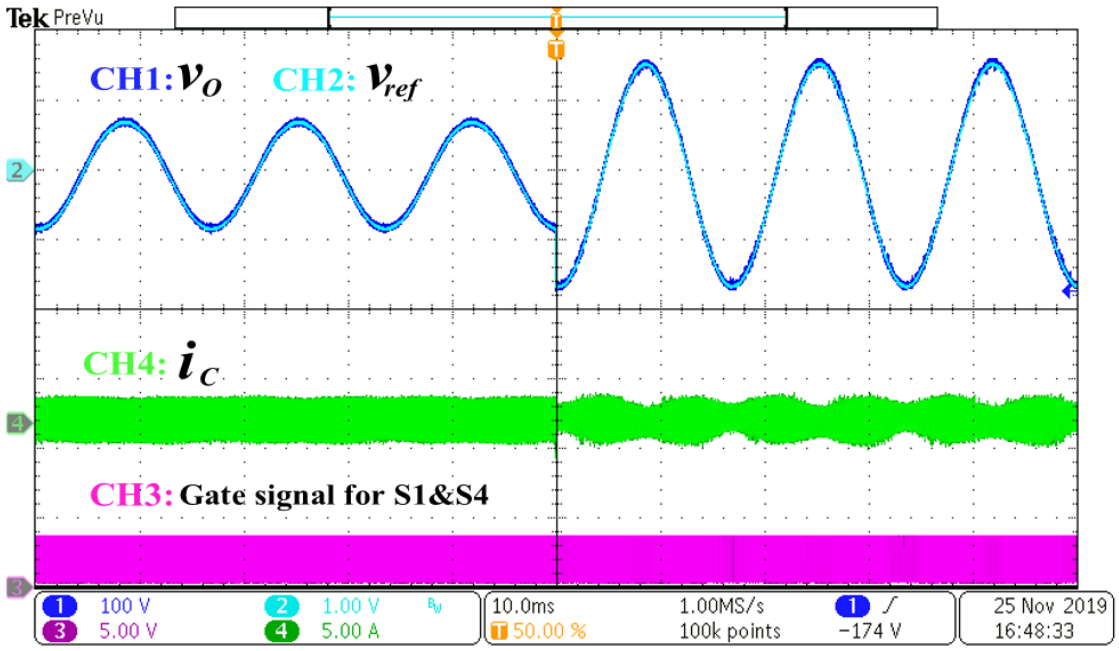


(c)

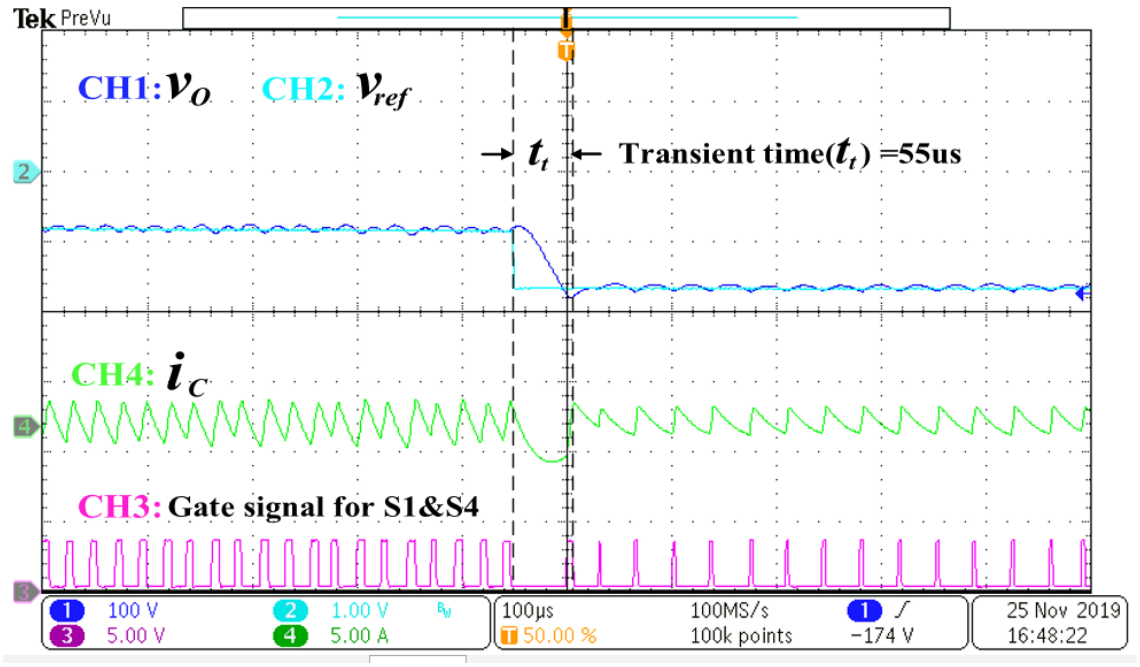
Figure 4-4: Steady-State Performance with (a) Reference with Third-Order Harmonic, (b) Reference with Frequency of 1 kHz (c) Inductive Load with Current Lagging 37.05°

4.2.2 Transient Response

Figure 4-5 shows the output voltage waveform under reference (v_{ref}) transient. The rms value of the reference doubles from 0.6 Vrms to 1.2 Vrms and the output voltage doubles from 60 Vrms to 120 Vrms. The output voltage follows the reference immediately within two switching actions. The transient period is 55 us. Figure 4-6 shows the results under the load resistance transient. The load resistance changes from 25.6 Ω to 14.4 Ω. It shows that v_o remains the same and i_o changes with the load. The transient also completes by two switching actions, and the transient period is 73 us.

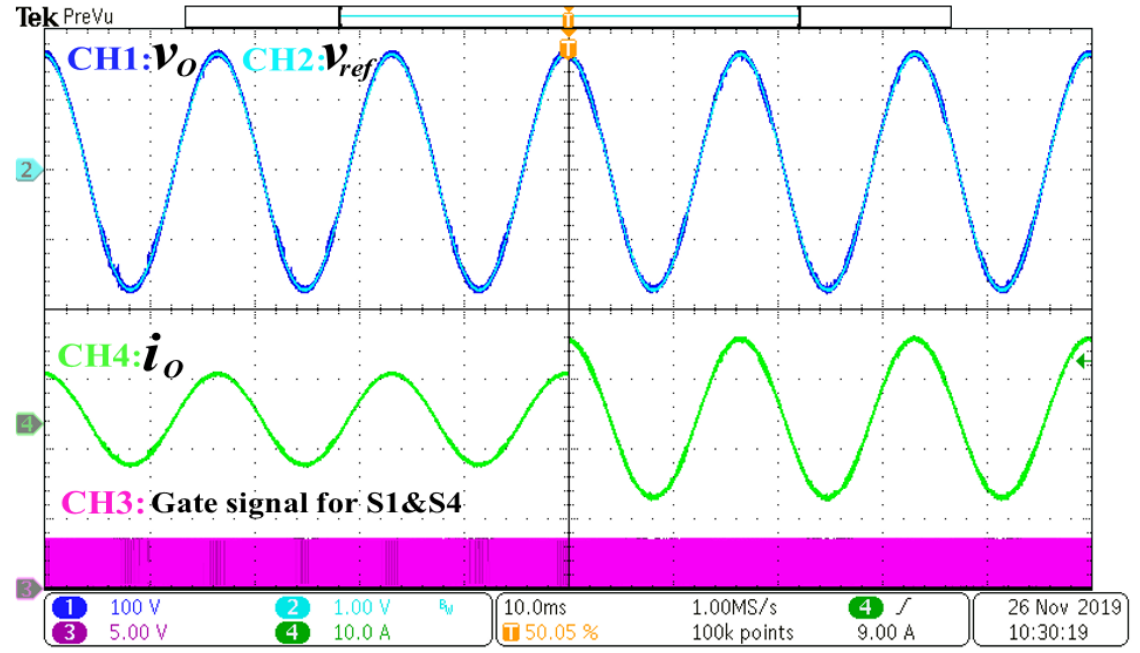


(a)

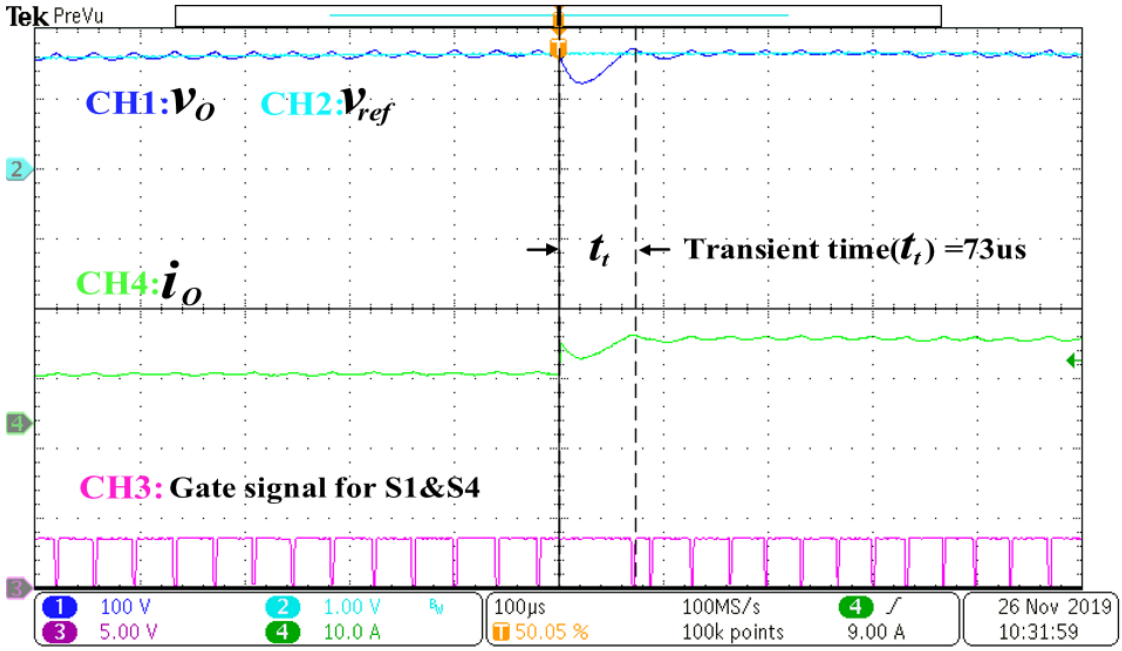


(b)

Figure 4-5: Transient Performance: the Voltage Reference Scaled up by 2



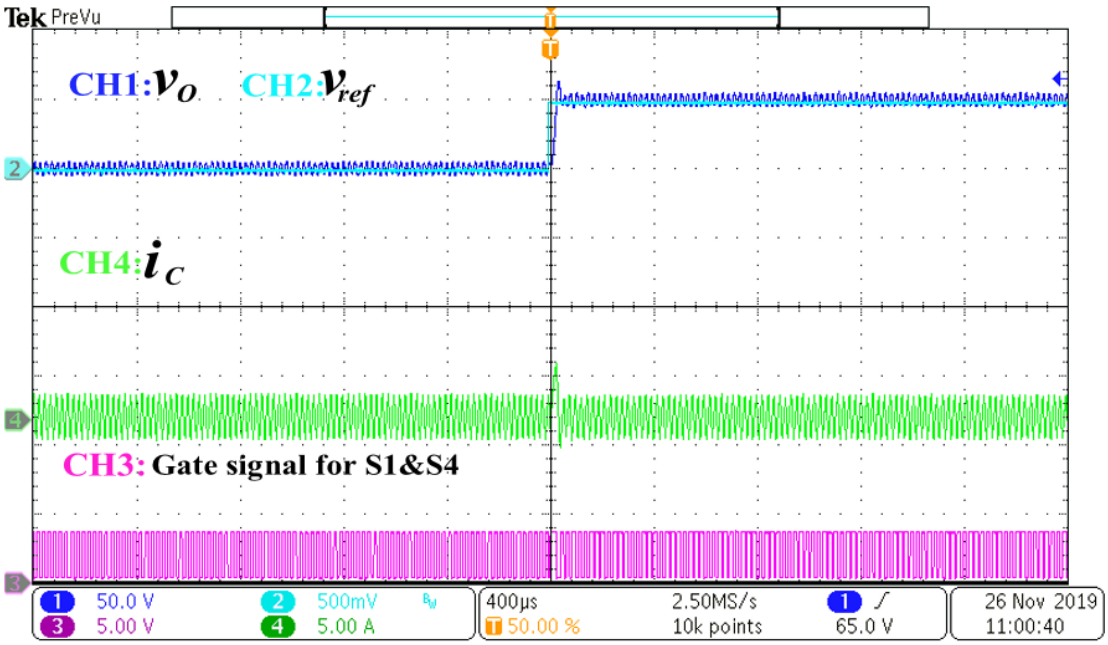
(a)



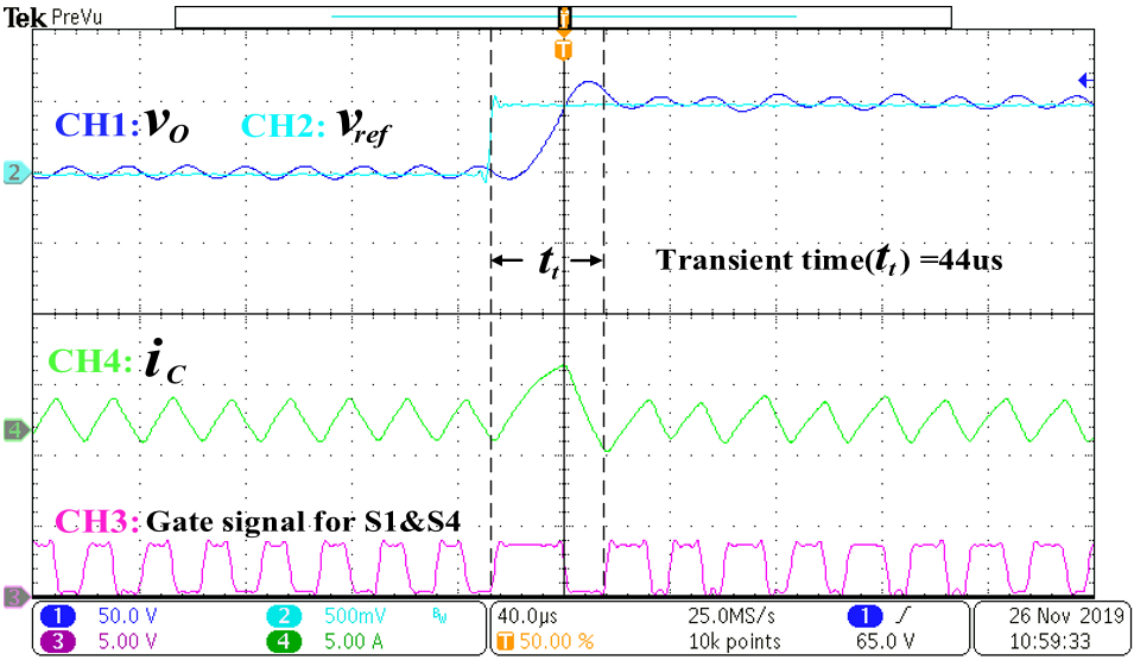
(b)

Figure 4-6: Transient Performance: The Load Reduced from 25.6 Ω to 14.4 Ω at 120 Vrms

Step response of the system is shown in Figure 4-7 when the reference changes from zero to 0.5 V; as a result, the output changes from zero to 50 V. The transient time is 44 us, and there is no settling time between the two operating points. Figure 4-8 shows the system trajectories. The boundary control guides the system to reach the new operation point by two switching actions.



(a)



(b)

Figure 4-7: Step Response: the Voltage Reference Jumps from 0 V to 0.5 V

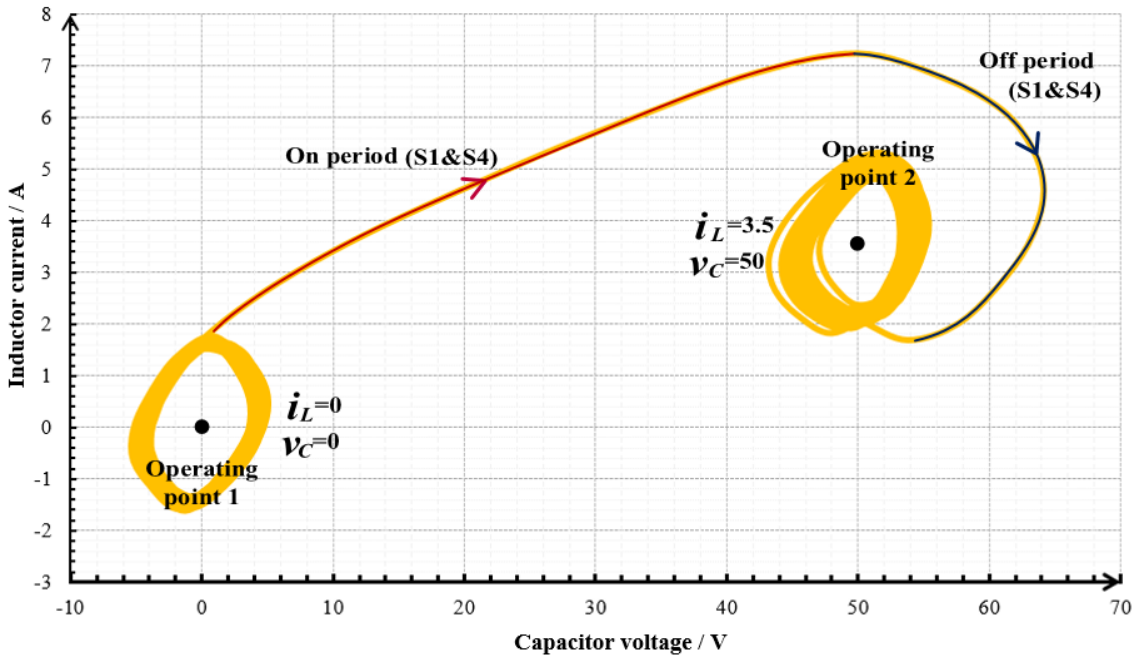


Figure 4-8: System Trajectories for the Transient

4.2.3 System Bandwidth

A Gain-Phase Analyser (Bode100) is used to measure the frequency response of the power amplifier. Figure 4-9 shows the system response at the rated power. The gain in the operation range has been adjusted to 0 dB. The power amplifier full power bandwidth is 4.43 kHz, and the half-power (-3 dB) bandwidth is 7.1 kHz. Figure 4-10 shows the power amplifier magnitude response at different modulation index (M) and indicates that when M is smaller, the power amplifier half-power (-3 dB) bandwidth is higher.

Table 4-3 shows the different maximum gain by the controller together with the power circuit under different modulation index. With these values, the analytical bandwidth can be observed from the bode plot of the RLC circuit shown in Figure 4-11.

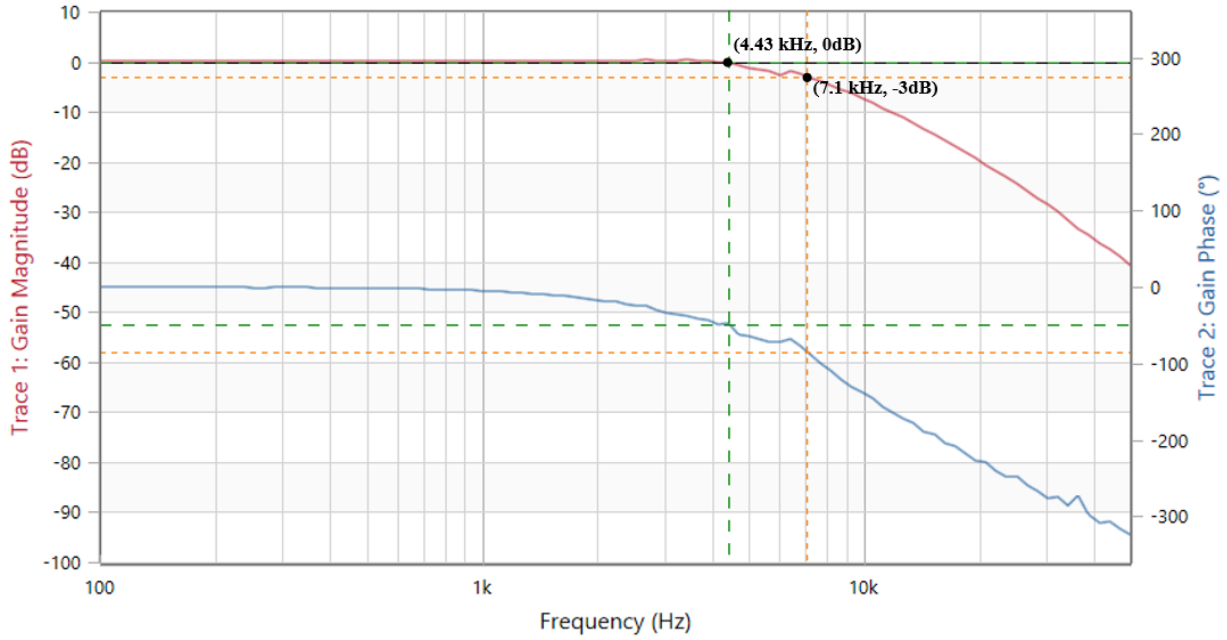


Figure 4-9: Power Amplifier Frequency Response at Rated Power Rating

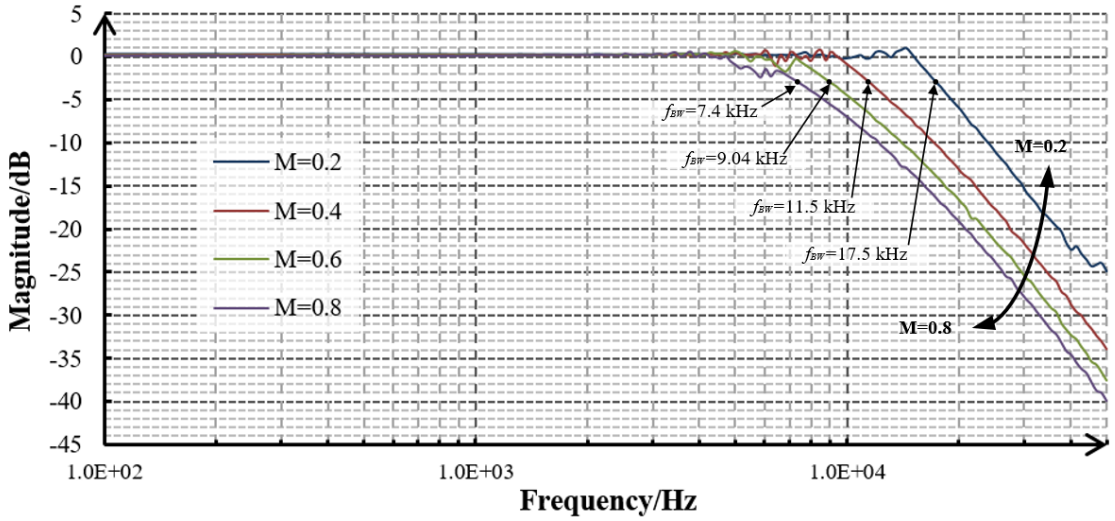


Figure 4-10: Power Amplifier Frequency Response at Different Modulation Indices

Table 4-3: Modulation Index vs Max Lifting Value

Modulation Index	**G_{max} (dB)**	**-3 dB- G_{max}**
0.2	15.99	-18.99
0.4	9.97	-12.97

0.6	6.44	-9.44
0.8	3.95	-6.95
0.85	3.42	-6.42

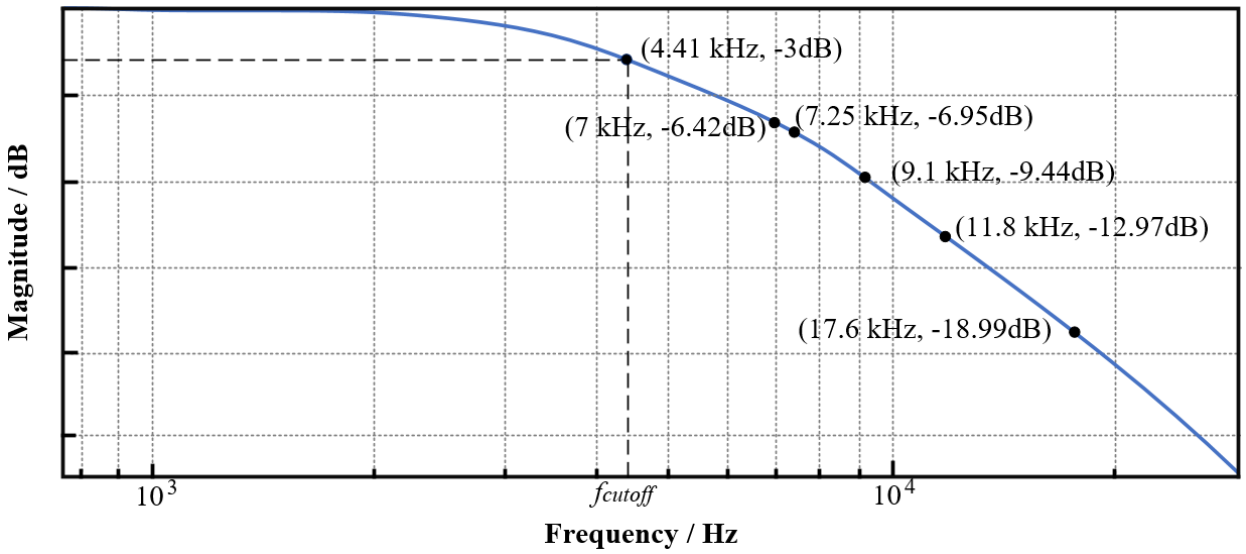


Figure 4-11: Bode Plot of the RLC Circuit

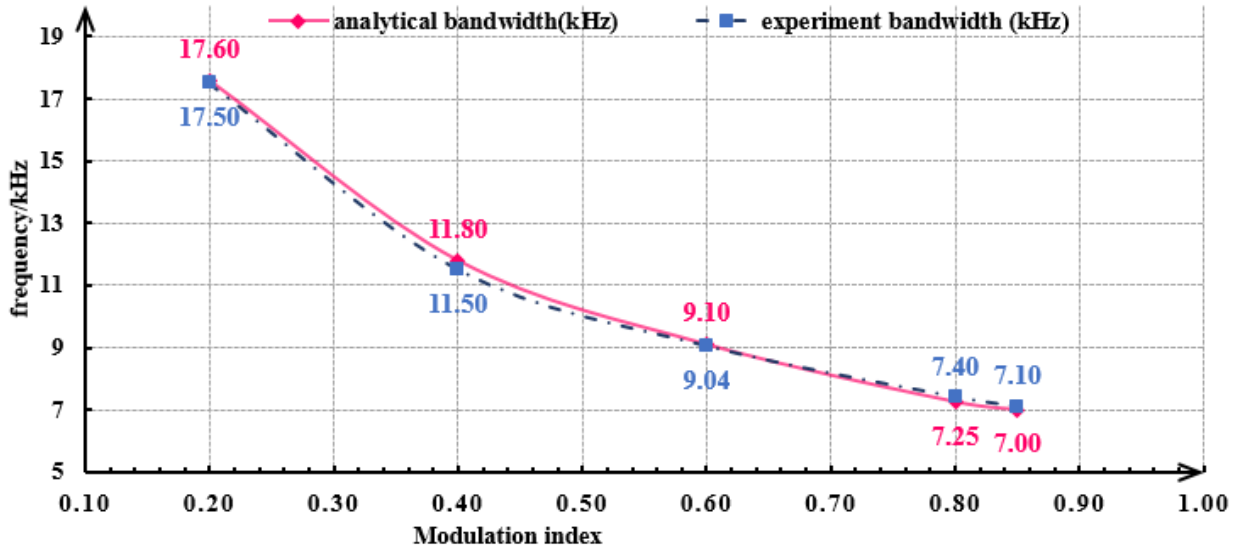


Figure 4-12: Analytical Bandwidth vs Experimental Bandwidth

Figure 4-12 shows the comparison of the analytical bandwidth and the experimental bandwidth. The two groups of values almost coincide, which verifies the analytical method to calculate the system bandwidth.

For the PHIL application, [11] suggested that a reasonable bandwidth of the switching power amplifier to adapt several applications for PHIL should be 5 kHz~10 kHz. The proposed power amplifier is working at an average switching frequency of 30 kHz, and the system bandwidth is 7.1 kHz. Therefore, the proposed power amplifier is feasible for PHIL applications.

The large-signal bandwidth-switching frequency ratio ($\frac{f_{BW}}{f_{SW}}$) of the proposed power amplifier is 0.237, and the small-signal bandwidth-switching frequency ratio ($\frac{f_{BW,s}}{f_{SW}}$) is 0.583 using the bandwidth when the modulation index is 0.2. Both $\frac{f_{BW}}{f_{SW}}$ and $\frac{f_{BW,s}}{f_{SW}}$ of the proposed system are higher comparing with the system using a linear controller, i.e. 0.04 and 0.16, respectively.

4.3 Chapter Summary

This chapter successfully demonstrates the operation as well as the intent for developing the proposed high bandwidth power amplifier. The proposed power amplifier is working at an average switching frequency of 30 kHz, and the system bandwidth is 7.1 kHz with high bandwidth-switching frequency ratios. The proposed power amplifier platform shows a fast dynamic response within tens of microseconds and a higher switching frequency in comparison with systems using DSP-Based or analog controllers in the existing literature. The experiment results have verified the corrected control criteria proposed in this thesis to compensate delay time and the analytical methods to calculate system bandwidth. All the experimental results agree with the analytical results within the system accuracy.

Chapter 5 Conclusions and Future Work

5.1 Conclusion

This thesis presents an innovative combination of a GaN-based inverter and a boundary controller implemented in an FPGA to realize a high bandwidth switching power amplifier with high bandwidth-switching frequency ratios. The shortcomings of the conventional semiconductor switches, control hardware devices and control methods identified during the literature review serve as a basis for conceiving the original research idea as well as the motivation for this research work. The main conclusions of this thesis are as follows:

- The three key considerations to build a high bandwidth power amplifier are the semiconductor, the control method and the controller hardware. This thesis has compared different types of power semiconductor switches and their major operation regions, the linear control and nonlinear control, precisely boundary control and the different controller hardware.

- This thesis proposed an innovative combination of GaN-based inverter, boundary control and FPGA to minimize transient time and realize a high bandwidth power amplifier for industrial applications. The proposed power amplifier platform has been successfully implemented, and it shows a fast dynamic response within tens of microseconds and a higher switching frequency of 30 kHz in comparison with systems using DSP-Based or analog controllers in existing research work of boundary control inverters. The power amplifier has a high system bandwidth of 7.1 kHz with high bandwidth-switching frequency ratios. The large-signal bandwidth-switching frequency ratio is 0.237, and the

small-signal bandwidth-switching frequency ratio is 0.583. The efficiency of the power amplifier is 97.78%.

- The influences of the non-ideal factors, including the ADC accuracy and the delay in the physical system, have been discussed and analyzed firstly in the boundary control research area. The delay time of the system contributes to an actual ripple, which is much larger than the designed ripple. The proposed compensation method to mitigate the negative impact on the performance of the boundary control from the delay time has been verified experimentally.

- This thesis has proposed an analytical method to estimate system bandwidth with boundary control. The system bandwidth will only depend on the frequency response of the RLC circuit and the ratio of the DC source and output voltage of the system. The experiment results verified the theory for estimating the system bandwidth. This estimation of the system bandwidth is informative in the design stage.

- From the research, realizing a certain ripple, the LC value can be smaller when the delay time is less. A higher system bandwidth can be achieved when the LC value is smaller. The result is a guide for designers to select proper hardware components, i.e. ADC, current sensor, operational amplifier and controller hardware, for realizing specific performance by a power electronic system with boundary control. ADCs with enough resolution should be selected to achieve a specific voltage ripple with a reasonable system accuracy. High-speed controller hardware, sensor circuits, ADCs, Semiconductor switches should be employed to realize a high-bandwidth system.

5.2 Future Work

As with any study, the work presented in this thesis can be extended. Several extensions of this thesis can be suggested in the following ways:

- The system frequency response has been evaluated experimentally but not analytically. More research work can be done to derive the transfer functions of the whole system and boundary control. The transfer function of boundary control is necessary for design the system and stability analysis when implementing boundary control together with other controllers, i.e. linear controllers, to achieve multiple control objectives. The method of applying curve fitting to the experimental results of the system frequency response provides a potential solution to find the transfer function of the whole system and the transfer function of boundary control.

- During this thesis work, the power amplifier has been implemented with a separate control board, sensor board and power board. Now that the design principles are verified, the whole system can be redesigned by integrating the controller, sensor and power switches, which will result in a considerable reduction of noise and latency and a more professional outlook. A high-speed digital interface can be developed using Aurora protocol and optical fibres to provide a direct connection between the real-time simulator, i.e. RTDS and Opal-RT and the power amplifier for the information exchange and sending reference. With this digital interface, the exchanged information and the references are immune from noises, and faster communications can be achieved by avoiding the ADCs or DACs. Higher bandwidth power amplifiers can be designed by selecting higher speed and accuracy components, i.e. current sensor and ADCs.

- The proposed power amplifier has been compared with the inverters using boundary in the existing literature. The benefits of the system can be further evaluated experimentally in terms of the comparison of GaN switches and traditional power switches, the comparison of FPGA and DSPs and the comparison of the boundary control and other linear controllers.

- The proposed power amplifier is a voltage amplifier operating in two quadrants, which can only provide power. In the future study, a four-quadrant voltage and current amplifier can be developed for more applications.

- The proposed power amplifier has been tested with resistive loads and inductive loads, and further research can be testing the power amplifier with other loads, such as capacitive loads and power electronics converters.

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Appendix

A. The notes for Table 1-2

Note:

1. The number is observed from the figures in the paper.
2. The number is observed from the figures in the paper, and the load is changed from 2.4Ω (60 W) to 24 Ω (6 W) for the transient time measurement.
3. The number is observed from the figures in the paper. The transient is measured when the reference voltage is changed from 10 Vrms to 1 Vrms.
4. The transient is measured when the reference voltage is changed at the peak of the reference signal from 70 Vrms to 110 Vrms. The transient periods of the inverters with the first order, second order control and N-order control are 75 us, 73 us, and 35 us, respectively.
5. The digital controller is implemented with an S3CEB2410 ARM-based Development Board.
6. The sampling rate is the ADC sampling rate for the capacitor current and voltage.
7. The number is observed from the figures in the paper. The transient is measured when the reference voltage is changed at near the peak of the reference signal from 25 Vrms to 80 Vrms with the resistor of 2kohm 3w
8. The digital controller is implemented with a TMS320C28x fixed-point DSP.
9. The sampling rate is the dominating rate considering both the sampling frequency and computation of the control law.
10. The digital controller is implemented with a dSPACE DS1005 DSP board.
11. The transient is measured when the reference voltage is changed to one-half of the original value for a hybrid seven-level inverter.
12. The digital controller is implemented using a TMS320F2812 fixed-point DSP.
13. The number is observed from the figures in the paper. The transient is measured when the reference is changed from 50 to 70 V.
14. The inverter is controlled by using the digital controller TMS320F2808.
15. The transient is measured when the grid current reference is suddenly changed from 4.6 to 9.1 A.

16. The digital controller is implemented with Texas Instruments F28M35H52C DSP.
17. The transient is measured when the output voltage reference is changed by 80%.

B. The derivation of (25) and (27)

The difference between $V_{r,a}$ and $V_{r,d}$ can be calculated in (A7)

$$V_{r,dff} = V_{r,a} - V_{r,d} = \frac{1}{C}(|\int_{t_1}^{t_5} i_{C,s}dt - \int_{t_1}^{t_4} i_{C,p}dt| + |\int_{t_6}^{t_{10}} i_{C,s}dt - \int_{t_6}^{t_9} i_{C,p}dt|) \quad \text{(A7)}$$

$\int_{t_1}^{t_5} i_{C,s}\,dt - \int_{t_1}^{t_4} i_{C,p}dt$ is the area of the blue quadrilateral from t_1 to t_5 and $\int_{t_6}^{t_{10}} i_{C,s}\,dt - \int_{t_6}^{t_9} i_{C,p}\,dt$ is the area of the blue quadrilateral from t_6 to t_{10} Shown in Figure 3-5. Here, the same assumption of constant output current is applied. An implied condition is that $V_{r,d} \geq 0$ or $V_{r,dff} \leq V_{r,a}$.

$$\int_{t_1}^{t_5} i_{C,s}\,dt - \int_{t_1}^{t_4} i_{C,p}\,dt = \int_{t_1}^{t_3}(i_{C,s} - i_{C,p})\,dt + \int_{t_3}^{t_4}(i_{C,s} - i_{C,p})\,dt + \int_{t_4}^{t_5} i_{C,s}\,dt \quad \text{(A8)}$$

$$\int_{t_1}^{t_3}(i_{C,s} - i_{C,p})\,dt = \int_{t_1}^{t_3} k_1(t - t_3) + i_{C,s}(t_3)dt - \int_{t_1}^{t_3} -k_2(t - t_1) + i_{C,s}(t_1)dt \quad \text{(A9)}$$

$$\int_{t_3}^{t_4}(i_{C,s} - i_{C,p})\,dt = \int_{t_3}^{t_4} k_2(t - t_3) + i_{C,s}(t_3)dt - \int_{t_3}^{t_4} -k_2(t - t_1) + i_{C,s}(t_1)dt \quad \text{(A10)}$$

$$\int_{t_4}^{t_5} i_{C,s}\,dt = \int_{t_4}^{t_5} -k_2(t - t_3) + i_{C,s}(t_3)dt \quad \text{(A11)}$$

Where $k_1 = \frac{v_{DC} - v_C}{L}$, $k_2 = \frac{v_{DC} + v_C}{L}$, $i_{C,s}(t_3) = 0.5\Delta i_{C,s} = 0.5\Delta i_{C,a}$ and $i_{C,s}(t_1) = i_{C,s}(t_3) - k_1\tau_{on}$

By solving the simultaneous equations (A9), (A10) and (A11), $|\int_{t_1}^{t_5} i_{C,s}\,dt - \int_{t_1}^{t_4} i_{C,p}\,dt|$ can be derived as (A12).

$$\int_{t_1}^{t_5} i_{C,s}\,dt - \int_{t_1}^{t_4} i_{C,p}\,dt = \frac{1}{2}(\frac{1}{k_2} + \frac{1}{k_1})\left(\left(\frac{1}{2}\Delta i_{C,a}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_1\tau_{on}\right)^2\right) \quad \text{(A12)}$$

$|\int_{t_6}^{t_{10}} i_{C,s}dt - \int_{t_6}^{t_9} i_{C,p}dt|$ can be calculated similarly.

$$|\int_{t_6}^{t_{10}} i_{C,s}dt - \int_{t_6}^{t_9} i_{C,p}dt| = \frac{1}{2}(\frac{1}{k_2} + \frac{1}{k_1})\left(\left(\frac{1}{2}\Delta i_{C,a}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_2\tau_{off}\right)^2\right) \quad \text{(A13)}$$

Put (A12) and (A13) into (A7), the equation (A14) is as follow.

$$V_{r,dff} = \frac{1}{2C}(\frac{1}{k_2} + \frac{1}{k_1})\left(2\left(\frac{1}{2}\Delta i_{C,a}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_1\tau_{on}\right)^2 - \left(\frac{1}{2}\Delta i_{C,a} - k_2\tau_{off}\right)^2\right) \quad \text{(A14)}$$

When $V_{r,d} = 0$,

$$V_{r,dff} = V_{r,a} = \frac{1}{2C}\left(\frac{1}{k_2} + \frac{1}{k_1}\right)\left(\frac{1}{2}\Delta i_{C,a}\right)^2 \quad \text{(A15)}$$

From (A14) and (A15) and assume$\tau_{on} = \tau_{off} = \tau$, $\frac{1}{2}\Delta i_{C,a}$ and $V_{r,a}$ can be calculated as (A16) and A(17).

$$\frac{1}{2}\Delta i_{C,a} = \left(k_1 + k_2 + \sqrt{2k_1k_2}\right)\tau \quad \text{(A16)}$$

$$V_{r,a} = \frac{\tau^2}{LC}\left(\sqrt{2v_{DC}} + \frac{2\sqrt{v_{DC}{}^3}}{\sqrt{v_{DC}{}^2 - v_C{}^2}}\right) \quad \text{(A17)}$$