Minimum Power Operation of Cascade Inverter Based Dynamic Voltage Restorer for Power Quality Improvement

By

Husam Al-Hadidi

A Thesis

submitted to the Faculty of Graduate Studies
in partial fulfillment of the requirements for the Degree of
Doctor of Philosophy

Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Manitoba, CANADA

THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

*****

COPYRIGHT PERMISSION

Minimum Power Operation of Cascade Inverter Based Dynamic Voltage Restorer for Power Quality Improvement

by

Husam Al-Hadidi

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirement of the degree of

Doctor of Philosophy

Husam Al-Hadidi © 2006

Permission has been granted to the Library of the University of Manitoba to lend or sell copies of this thesis/practicum, to the National Library of Canada to microfilm this thesis and to lend or sell copies of the film, and to University Microfilms Inc. to publish an abstract of this thesis/practicum.

This reproduction or copy of this thesis has been made available by authority of the copyright owner solely for the purpose of private study and research, and may only be reproduced and copied as permitted by copyright laws or with express written authorization from the copyright owner.

Acknowledgements

The encouragement, guide, support and incredible enthusiasm provided by Prof. A. M. Gole have been very crucial in making this thesis a reality. Thanks are due to the HVDC Centre for providing me a space and equipment during the experimental phase of this thesis and their staff members Mr. Randy Wachal, P.Eng. and Mr. Paul Wilson P. Eng. I would also like to thank my University colleague and fellow Ph.D student Mr. F. Mosallat. To all staff and colleagues of the Power Group for their kindness and friendship which have made this period a memorable and enlightening experience. I also thank my family back home, especially my parents who have devoted most of their time and energy for the well being of their children.

Finally, I express my deep appreciation to my beloved wife whose love, understand and support, were the essential ingredients in completing this work. To my two kids Samer and Sally, the tremendous joy of your presence has certainly given me an inspara-tion.

Abstract

This thesis introduces an enhanced implementation of a dynamic voltage restorer (DVR) based on a Voltage Sourced Converter (VSC) topology, for power quality improvement in a power network. Building on earlier research that has shown that sag compensation ability is greatly enhanced by permitting energy storage on the dc side of the VSC, a new control method is introduced which mitigates sag with minimum real power injection. This technique requires a much smaller energy reservoir on the dc side. It also permits the energy reservoir to be a capacitor instead of higher capacity reservoir such as a battery. A modular H-bridge mulilevel cascade converter topology is used which has the benefits of one-phase compensation as well as transformerless operation.

The thesis also introduces a modified new topology and the corresponding control system where the capacitor energy storage can be even further reduced by active modulation of the power factor during a sag. The thesis also demonstrates that the auxiliary function of harmonic compensation can be easily integrated into the control of the DVR.

The operational limits and the component selection of the circuit parameters is conducted from simplified analytical formulation of the circuit equations.

Extensive analysis of the dynamic performance is conducted using electromagnetic transients simulation on the PSCAD/EMTDC program.

Finally, all key conclusions are supported by small scale physical implementation in the laboratory.

Contents

Chapter 1 - Introduction

Chapter 2- Power Quality Problems

Chaper 4 - SYSTEM MODELING AND CONTROL STRATEGIES

List of Figures

List of Tables

List of Abbreviations

DFT	Discrete Fourier Transform
FFT	Fast Fourier Transform
VSC	Voltage Sourced Converter
PWM	Pulse Width Modulation
PS-PWM	Phase Shift Pulse Width Modulation
SHPWM	SubHarmonic Pulse Width Modulation
SFOPWM	Switch Frequency Optimal PWM
PLL	Phase l

UPS	Uninterruptible Power Supplies
FFS	Fundamental Frequency Switching
DVR	Dynamic Voltage Restorer
PLL	Phase Locked-Loop
PFG	Programmable Function Generator
RTP	Real Time Playback
TVSS	Transient Voltage Surge Suppression
UPS	Uninterruptible Power Supplies
THD	Total Harmonic Distortion
IGBT	Insulated Gate Bipolar Transistors
GTO	Gate Turnoff Thyristor
HBI	H-bridge Inverter
SMES	Superconductive Magnetic Energy Storage

List of Symbols

ac	Alternating current
$\mathbf{A_m}$	Amplitude of the modulation waveform
$\mathbf{A_c}$	Amplitude of carrier waveform
dc	Direct current
$\mathbf{f_c}$	Frequency of the carrier
$\mathbf{f_m}$	Frequency of the modulation waveform
K	Frequency ratio

kA	Kiloampere
kV	Kilovolt
m	Modulation index
p.f	Load power factor
$\mathbf{V_s}$	Supply voltage
$\mathbf{V_l}$	Load voltage
$\mathbf{V_{dvr}}$	Dynamic Voltage Restorer voltage
$\mathbf{I_l}$	Load current
$\Delta\mathbf{V_{s\_sag}}$	Sag voltage
α	Dynamic Voltage Restorer injection angle
θ	Phase Locked-Loop angle
ϕ	Load power factor angle
Xp	Shunt inductance
$\mathbf{R_l}$	Load resistor
$\mathbf{L_f}$	Filter inductance
$\mathbf{C_f}$	Filter capacitor

CHAPTER 1

Introduction

1.1 Introduction

This chapter introduces the definition of power quality and the importance of maintaining power quality. The basic dynamic voltage restorer (DVR) and the research objectives will be presented in this chapter.

The term power quality has come into the vocabulary of many industrial and commercial electricity end-users in recent years has many definitions and terminologies, which vary according to IEEE and IEC standards, utilities, and consumers [1-4]. However it may be defined as the degree to which both the utilization and delivery of electric power affect the performance of electrical equipment [5].

Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage. Sensitive equipment and non-linear loads are now more common place in both the industrial sectors and the domestic environment. Because of this a heightened awareness of power quality is developing amongst electricity users. Occur-

rences affecting the electricity supply that were once considered acceptable by electricity companies and users are now often considered a problem to the users of everyday equipment. Voltage sag, swell and harmonics can cause equipment to fail, or shutdown, as well as create a large current unbalance that could blow fuses or trip breakers. These effects can be very expensive for the customer, ranging from minor quality variations to production downtime and equipment damage [6]. With the dawn of a competitive environment, the utility company has much more interest in power quality. Utilities are interested in keeping their customers satisfied, as well as keeping them on-line and drawing kilowatts, creating more revenue for the utility. All of this interest has resulted in a variety of devices designed for mitigating power disturbances such as voltage sags [l]. One class of these devices is the DVR, which has been developed and applied to the critical loads such as found in semiconductor or chemical plants.

1.2 Conventional Dynamic Voltage Restorer (DVR)

A conventional dynamic voltage restorer (DVR)[7, 10], with its excellent dynamic capabilities, when installed between the supply and a critical load feeder, can compensate for voltage sags, restoring line voltage to its nominal value within a few milliseconds and hence avoiding any power disruption to that load. Fig. 1.1 shows the schematic diagram of a typical DVR used for voltage correction. When the supply voltage V_S changes, the DVR injects a voltage V_{dvr} in series with the supply voltage as shown in Fig. 1.2 so that the desired load voltage magnitude can be maintained. The DVR is simply a voltage source inverter that produces an ac output voltage and injects in series with the supply voltage through a booster transformer.

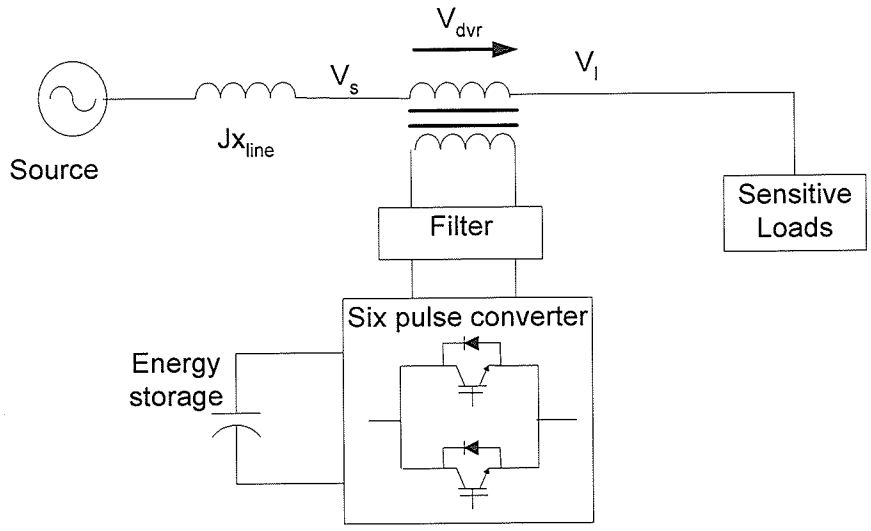


Fig. 1.1: Schematic diagram of a *Conventional* DVR

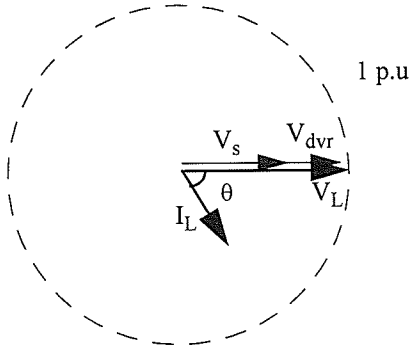


Fig. 1.2: Phasor diagram for compensation of sag

1.2.1 Major Components of a Conventional DVR

From Fig 1.1 the major conventional DVR components and their function can be listed as follows:

- Injection / Booster transformer:

  It's main tasks are connects the DVR to the distribution network via the HV-windings and transforms and couples the injected compensating voltages generated by the volt-

age source converters to the incoming supply voltage. It is one unit three phase construction.

- Harmonic filter:

  The main tasks of harmonic filter is to keep the harmonic voltage content generated by the voltage source converters to the permissible level. It has a small rating approximately 2% of the load MVA connected to delta-connected tertiary winding of the injection transformer.

- Energy source e.g. storage capacitor bank.

  The purpose is to supply the necessary energy to the VSC via a dc link for the generation of injected voltages. Different kinds of energy storage devices exist like superconductive magnetic energy storage (SMES), batteries, and capacitance. In fact, the capacity of the stored energy directly determines the ride-through capability; therefore it can affect the duration of the sag which can be mitigated by the DVR. The focus of this research is not to give a justification for selection of energy storage device, but to develop a control algorithm to minimize the amount of energy required to mitigate a voltage sag. Essential control aspects are considered in Chapter 4 and Chapter 6.

- DC charging circuit:

  The main tasks of the dc charging circuit are to charge the energy source after a sag compensation event and maintain dc link voltage at the nominal dc link voltage.

- Control and protection system.

- Voltage source converters

The main task of the voltage source converter is to generate the required injected voltage to compensate for the supply voltage sags. A six-pulse voltage source converter with its ac output connected to the low voltage windings of the injection transformer is the simplest implementation of such a converter, as shown in Fig. 1.3. In normal operation, a 6-pulse bridge voltage source inverter with a charged dc capacitor will give a balanced set of three quasi-square waveforms of the voltages at the output terminal, as shown in Fig. 1.4 [9]. This simple form is usually not adequate for utility application as it has harmonics, needs a series transformer and has a single dc storage for all three phases. This research proposes cascade multilevel inverter based DVR. The proposed configuration will be discuss in detail in Chapter 3.

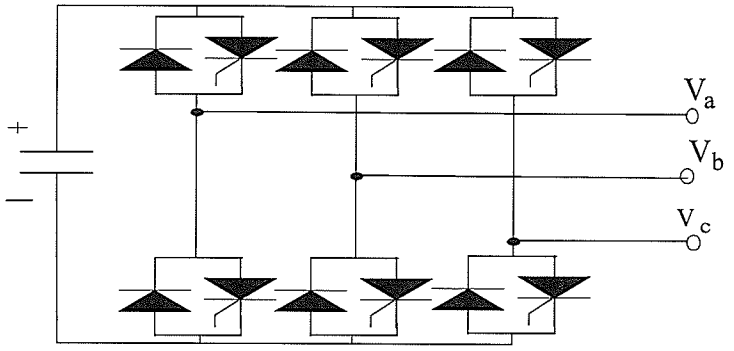


Fig. 1.3: Six-Pulse **GTO voltage source inverter**

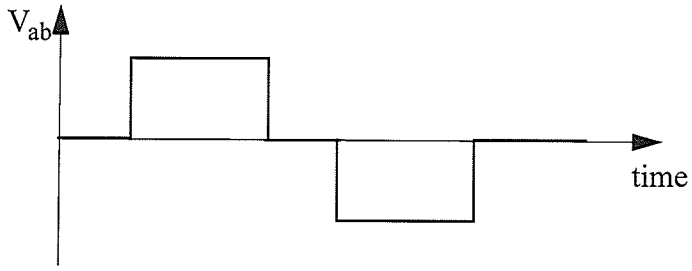


Fig.1.4: Inverter output line-to-line voltage waveform

The customer's requirements dictate the design and performance of the DVR. In the third chapter; the considerations that must be taken into account for the design of the DVR in order to fulfil the required specifications will be investigated. Design considerations that influence the rating and performance of the DVR such as the load MVA, power factor, magnitudes of single and three phase voltage sags and fault duration, three phase fault level at the incoming bus, etc. are discussed in detail in Chapter 4. In Fig. 1.3 the switching device is shown as a Gate Turnoff Thyristor (GTO). However, for ratings typical for distribution system application the Insulated Gate Bipolar Transistors (IGBT) device is adequate. Individual IGBT ratings are now upto 4.5kV, 2.0kA [44].

1.3 Research Objectives

The main objective of this research is to develop a new cascade multi-level based topology and control strategy for compensating and mitigating voltage disturbances and improving the power quality in distribution systems while optimizing the dc-side energy storage. To achieve the above objective the following tasks were carried out:

- Investigation of different topologies of multilevel inverters
- Identification and development of PSCAD/EMTDC models for the prototype network configurations. The converter devices will be tested on these network configurations.
- Development of suitable control strategies which will be aimed at:
  1- Maintaining individual capacitor voltages at desired levels.
  2- Optimizing the dc-side energy storage requirements by controlling the amount of active power injected to the system.
  3- Obtaining adequate dynamic performances with high control stability.
  4- Charging ability of the capacitors with energy drawn from the system without any connection on the dc side of the DVR.
- Investigation of the switching methods. Both the fundamental frequency switching (FFS) and pulse width modulation (PWM) techniques will be studied.
- Develop DVR circuit topology, which has the ability to mitigate severe and long duration voltage sags with comparatively small energy storage capacitors.
- Develop a novel control strategy to add a harmonic elimination ability to the DVR
- Additional Considerations.
  1. Implications of additional capacitor sizing for energy storage.
  2. Using PWM for harmonic quality improvement.

1.4 Digital Simulations

The models for the prototype network configurations were further evaluated and analyzed by using the electromagnetic transient simulation program PSCAD/EMTDC.

1.5 Thesis Organization

This thesis includes nine chapters. Chapter 2 discusses some of the power quality problems and their definitions according to IEEE Standards. In Chapter 3, there is a full analysis of multilevel inverters with a focus on cascade multilevel inverters and their operating principles and control strategies. Chapter 4 introduces the DVR operating principle, mathematical analysis of the required active and reactive power needed by the DVR to mitigate a certain sag and a proposed control strategy to optimize the dc energy storage of the DVR. Chapter 5 provides the simulation results for the mitigation of balance and unbalanced voltage sags. Chapter 6 presents a proposed novel DVR configuration and compares it with the existing configuration to demonstrate the superiority of the proposed configuration. Chapter 7 presents an extensive study about harmonic compensation techniques and there suitability for integrating into DVR configurations. The hardware and the software for the experimental work and results are presented in Chapter 8. Finally, Chapter 9 summarizes and concludes the contribution of this thesis, and suggests some topics for future research.

CHAPTER 2

Power Quality Problems

2.1 Introduction

Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage. Sensitive equipment and non-linear loads are now more commonplace in both the industrial/commercial sectors and the domestic environment. Hence, a heightened awareness of power quality is developing amongst electricity users. Occurrences affecting the electricity supply that were once considered acceptable by electricity companies and users are now often considered a problem to the users of everyday equipment [4-6].

2.2 Transients

"The term transients has been used in the analysis of power system variations for a long time. Its name immediately conjures up the notion of an event that is undesirable but momentary in nature" [1]. The IEEE Std. 100-1992 definition of transient reflects this understanding. The primary definition uses the word "rapid" and talks of frequencies up to

3 MHz when defining the transient in the context of evaluating cable systems in substations. Other definitions in IEEE Std. 100-1992 are broader in scope and simply state that a transient is that part of the change in a variable that disappears during transition from one steady-state operating condition to another. Unfortunately, this definition could be used to describe just about anything unusual that happens on the power system.

2.3 Short-duration variations

"This category encompasses the IEC category of voltage dips and short interruptions as well as the antithesis of dip, or swell" [1]. Each type of variation can be designated as instantaneous, momentary, or temporary, depending on its duration as defined in Table 2.1. Short-duration voltage variations are almost always caused by fault conditions, the energizing of large loads that require high starting currents, or intermittent loose connections in power wiring. Depending on the fault location and the system conditions, the fault can cause either temporary voltage rises (swells) or voltage drops (sags), or a complete loss of voltage (interruptions).

2.3.1 Interruption

An interruption occurs when the supply voltage or load current decreases to less than 0.1 pu for a period of time not exceeding 1 min. Interruptions can be the result of power system faults, equipment failures, and control malfunctions[1, 5]. The interruptions are measured by their duration since the voltage magnitude is always less than 10% of nominal. The duration of an interruption due to a fault on the utility system is determined by utility protective devices and the particular event that is causing the fault. The duration

of an interruption due to equipment malfunctions or loose connections can be irregular. Some interruptions may be preceded by voltage sag when these interruptions are due to faults on the source system. The voltage sag occurs between the time a fault initiates and the protective device operates. On the faulted feeder, loads will experience a voltage sag followed immediately by an interruption.

2.3.2 Voltage Sags

A momentary voltage dip that lasts for a few seconds or less is classified as a voltage sag. Voltage sags may be caused by faults on the transmission or distribution system or by the switching of loads with large amounts of initial starting/ inrush current (motors, transformers, large dc power supplies). Voltage sags may be sufficiently severe, especially in the case of faults, to cause sensitive loads (computers, VCRs, clocks, etc.) to reset [8]. The term sag has been used in the power quality community for many years to describe a specific type of power quality disturbance; a short duration voltage decrease. Clearly, the notion is directly borrowed from the literal definition of the word sag. The IEC definition for this phenomenon is called dip.

2.3.3 Swells

A swell is defined "as an increase in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 min. Typical magnitudes are between 1.1 and 1.8 pu" [1]. As with sags, swells are usually associated with system fault conditions, but they are much less common than voltage sags. A swell can occur due to a single line-to-ground fault on the system resulting in a temporary voltage rise on the unfaulted phases. Swells

can also be caused by switching off a large load or switching on a large capacitor bank. A formal definition of swell in IEEE Std. C62.41-1991 is a momentary increase in the power-frequency voltage delivered by the mains, outside of the normal tolerances, with duration of more than one cycle and less than a few seconds [6].

2.4 Long duration variations

Long duration variations encompass rms deviations at power frequencies for longer than 1 min. The steady-state voltage tolerances expected on a power system are specified. These magnitudes are reflected in Table 2.1. Long duration variations are considered to be present when the ANSI limits are exceeded for greater than 1 min. Long duration variations can be either overvoltages or undervoltages, depending on the cause of the variation. Overvoltages and undervoltages generally are not the result of system faults. They are caused by load variations on the system and system switching operations. These variations are characterized by plots of rms voltage versus time.

2.4.1 Overvoltages

Overvoltages can be the result of load switching (e.g., switching off a large load), or variations in the reactive compensation on the system (e.g., switching on a capacitor bank). Poor system voltage regulation capabilities or controls result in overvoltages. Incorrect tap settings on transformers can also result in system overvoltages.

2.4.2 Undervoltage

Undervoltages are the result of the events that are the reverse of the events that cause overvoltages. A load switching on, or a capacitor bank switching off, can cause an undervoltage until voltage regulation equipment on the system can bring the voltage back to within tolerances. Overloaded circuits can result in undervoltages also.

2.5 Sustained interruptions

The decrease to zero of the supply voltage for a period of time in excess of 1 min is considered to be a sustained interruption. Voltage interruptions longer than 1 min. are often permanent in nature and require manual intervention for restoration. Sustained interruptions are specific power system phenomena and have no relation to the usage of the term outage. Outage, as defined in IEEE Std. 100-1992, does not refer to a specific phenomenon, but rather to the state of a component in a system that has failed to function as expected. Also, use of the term interruption in the context of power quality monitoring has no relation to reliability or other continuity of service statistics.

2.6 Voltage imbalance

Voltage imbalance (or unbalance) is defined as the ratio of the negative or zero sequence component to the positive sequence component. The negative or zero sequence voltages in a power system generally results from unbalanced loads causing negative or zero sequence currents to flow. Imbalance can be estimated as the maximum deviation from the average of the three-phase voltages or currents, divided by the average of the

three-phase voltages or currents, expressed in percent. In equation form voltage imbalance = 100 ´ (max deviation from average voltage)/average voltage [6].

2.7 Waveform distortion

Waveform distortion is a steady-state deviation from an ideal sine wave of power frequency principally characterized by the spectral content of the deviation. There are five primary types of waveform distortion as follows:

- DC offset
- Harmonics
- Interharmonics
- Notching
- Noise

2.7.1 Harmonics

Harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate (termed the fundamental frequency; usually 50 Hz or 60 Hz) [IEC 1000-2-1 (1990)]. Harmonics combine with the fundamental voltage or current, and produce waveform distortion. Harmonic distortion exists due to the nonlinear characteristics of devices and loads on the power system. These devices can usually be modeled as current sources that inject harmonic currents into the power system. Voltage distortion results as these currents cause nonlinear voltage drops across the system impedance. Harmonic distortion is a growing concern for many customers and for the overall power system due to the increasing application of

power electronic equipment. Harmonic distortion levels can be characterized by the complete harmonic spectrum with magnitudes and phase angles of each individual harmonic component. It is also common to use a single quantity, the Total Harmonic Distortion (THD), as a measure of the magnitude of harmonic distortion. Harmonic currents result from the normal operation of nonlinear devices on the power system.

Table 2.1. Categories of Power quality variation- IEEE Std. 1159-19995

Categories	Typical Duration	Typical Magnitudes
1. Transients		
1.1 Impulsive	< 200 μs	
1.2 Oscillatory	< 30 cycles	
2. Short-Duration Variations		
2.1 Sag		
2.1.1 Instantaneous	0.5-30 cycles	0.1-1.0 pu
2.1.2 Momentary	30-120 cycles	0.1-1.0 pu
2.1.3 Temporary	2 sec.-2 min.	0.1-1.0 pu
2.2 Swells		
2.2.1 Instantaneous	0.5-30 cycles	0.1-1.8 pu
2.2.2 Momentary	30-120 cycles	0.1-1.8 pu
2.2.3 Temporary	2 sec.-2 min.	0.1-1.8 pu
3. Long-Duration Variations		
3.1 Overvoltages	> 2 min.	0.1-1.2 pu
3.2 Undervoltages	> 2 min.	0.8-1.0 pu
4. Interruptions		
4.1 Momentary	< 2 sec.	0
4.2 Temporary	2 sec.- 2 min.	0
4.3 Long-Term	> 2 min.	0
5. Waveform Distortion		
5.1 Voltage	steady-state	0-20%
5.2 Current	steady-state	0-100%
6. Waveform Notching	steady-state	
7. Flicker	intermittent	0.1-7%

2.8 Power quality standards

IEEE attempts to fix a set of standards to accurately define and quantify the quality of power supplied to the customer. But these standards vary with the type of load and the magnitude of the disturbance. The most important voltage quality indices are listed as follows:

The CBEMA Curve: In the early 1980's, the Computer Business Manufacturers Association (CBEMA, and now the ITI Council) established a susceptibility profile curve as shown in Fig. 2.1 to aid manufacturers in the design of power supply protection circuits. This curve has since become a standard reference within the industry. It describes an AC input voltage boundary, which typically can be tolerated (no interruption in function) by most Information Technology Equipment (ITE).

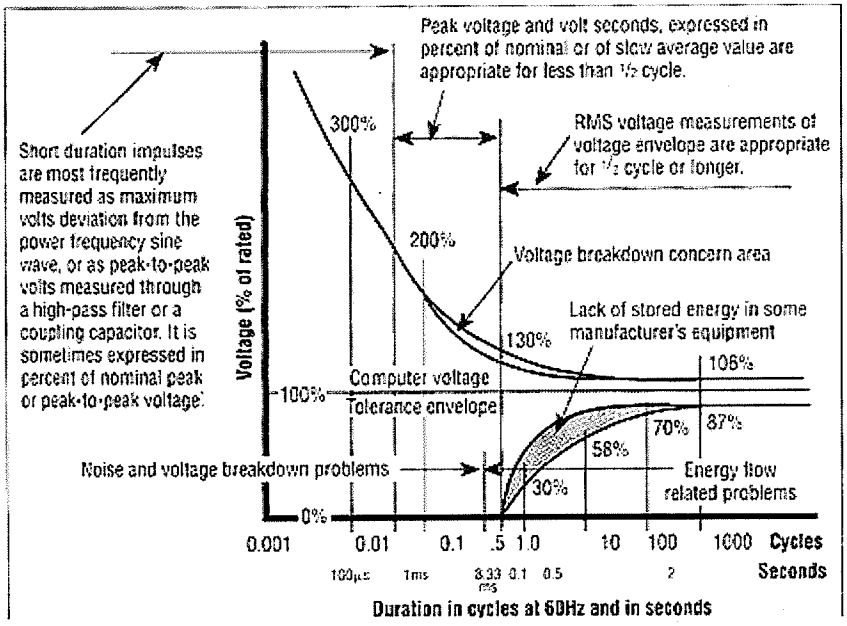


Fig. 2.1 The CMEBA plot for voltage tolerance

Total Harmonic Distortion (THD): Total Harmonics Distortion factor, which was defined as the ratio of the root-mean-square of the harmonic content to the root-mean-square of the fundamental quantity [6], which is expressed as a percent of the fundamental, that is

$$THD = 100\sqrt{\sum_{n\neq 1,3n}\left(\frac{V_n}{V_1}\right)^2} \quad (2.1)$$

Flicker Limit Curve: This is used to assess the visibility that is produced by the voltage fluctuations, based on the voltage fluctuations definition. IEEE publishes this curve in the IEEE standards 519-1992 and 141-1993 as shown in Fig 2.2.

Short-term flicker indicator, P_{st}: The flicker severity evaluated over a short period (in minutes); Pst = 1 is the conventional threshold of irritability. A Pst value is obtained every 10 min. There are 144 Pst samples each day [3].

Long-term flicker indicator, P_{lt}: The flicker severity evaluated over a long period (a few hours) using successive Pst values [3]. Each P_{lt} value is calculated from 12 successive Pst values using this formula:

$$P_{lt} = \sqrt[3]{\frac{1}{12}\sum_{j}^{12} P_{stj}} \quad (2.2)$$

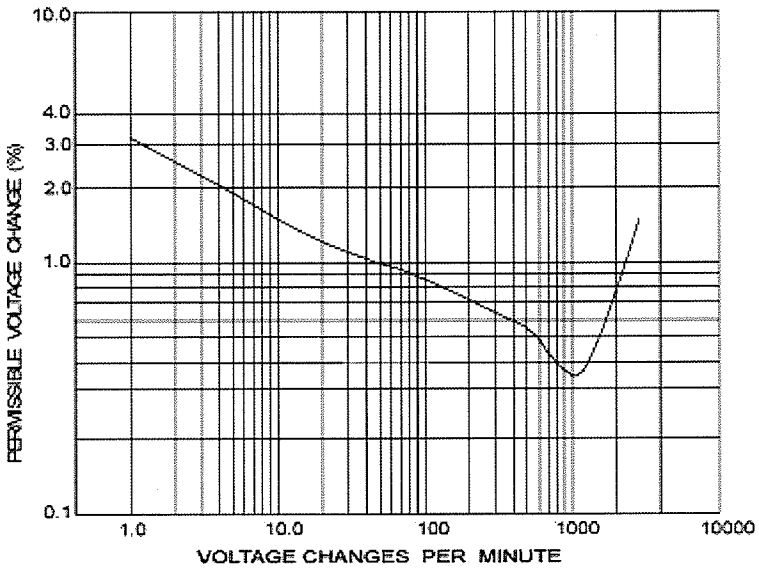


Fig. 2.2 Flicker limit curve of 519-1992 and 141-1993

2.9 Mitigation Methods Currently in Use

The remainder of this chapter provides an overview of each of the current mitigation technologies.

2.9.1 Transient Voltage Surge Suppression (TVSS)

TVSS devices are used to protect other equipment from the dangers of brief but potentially harmful voltage surges, which can be caused by lightning and the switching of inductive or capacitive devices [9]. TVSS devices are best understood as high-voltage, high-power semiconductors. At normal voltages, they conduct little or no electrical current. As voltage climbs, they begin conducting current. For example, a surge arrester designed for a 3 kV system may conduct 1 milliamp at 5 kV and 10,000 amps at 10 kV—a 7-fold increase in current magnitude after a mere doubling of applied voltage.

2.9.2 Uninterruptible Power Supplies (UPS)

UPSs use energy storage, usually in the form of lead-acid batteries, to store energy in the event that utility power is interrupted. Some newer UPS topologies use alternative energy storage such as flywheels, super conducting inductance ultracapacitors, or advanced chemical batteries. There are basically three different types of devices that are commonly referred to as UPSs: offline (standby), line-interactive, and online.

2.9.3 Dynamic Voltage Correction or Restoration (DVC, DVR)

Dynamic voltage restorers as shown in Fig. 1.1 augment voltage during voltage sags by adding missing voltage at critical times[7]. The theory is that because end users suffer many more voltage sags than outages, having a device that mitigates only sags can become cost-effective than conventional technologies. These devices can have different configuration and the focus of this research is to investigate one promising topology that achieves sags/swells compensation with minimum stored energy. Different kinds of energy storage devices are exist like superconductive magnetic energy storage (SMES), batteries, and capacitance. In fact, the capacity of the stored energy directly determines the ride-through capability therefore it can effect the duration of the sag which can be mitigate by the DVR.

CHAPTER 3

Multilevel Inverter Topologies

3.1 Introduction

Multilevel power conversion has been receiving increased attention in the past few years for high-power applications [8]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature [9]. These converters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with an improved harmonic spectrum and attain higher voltages with a limited maximum device rating. In this multilevel Voltage Source Inverter (VSI) based dynamic voltage restorer (DVR) category, there are mainly two different system configurations. They are 1) diode-clamped converter configuration [11], and 2) cascading converter configuration [14]. In this chapter will analyze the first configuration in brief and focus will be given to the second configuration to develop DVR system.

3.2 Diode-Clamped Multilevel Inverter

The diode-clamped multilevel inverter uses one DC bus subdivided into a number of voltage levels by a series string of capacitors [11]. A generalized structure of one phase of a 5-level inverter with a gate turnoff switch (GTO) is shown in Fig. 3.1. The dc capacitors are shared by the other phases, and possibly by the other bridges in higher pulse number designs. In a three-phase bridge configuration the number of levels in the line-to-line voltage will be 2N+1. The advantages of such a structure are each thyristor voltage stress will be limited to one capacitor voltage level, Vdc/(N-1), through clamping diodes. Furthermore, each GTO thyristor is well protected against overvoltage by the clamping action of the dc capacitors. There are N-1 complementary switch pairs in each phase, i.e., T_1-T'_1, T_2-T'_2, ...,T_{N-1}-T'_{N-1}. It should be mentioned that for each voltage step only one GTO thyristor must turn on and one GTO thyristor must turn off. For example, if T_1 is off, then $T_2, T_3, \ldots T_{N-1}$ and T'_1 are on, and the terminal voltage V_1 is connected to the output terminal through $Dp_1, T_2, T_3, \ldots\ldots T_{N-1}$ for positive current, or through T'_1 and DN_1 for negative currents. As described above, take one single phase into account, the five voltage levels could be achieved at the output terminal if the gate logic in Table 3.1 is followed, a stepped output voltage of the five level inverter shown in Fig. 3.2, which is a simple sum of the two rectangular waveforms. It should be noted that the clamping diodes are required to block different voltages, e.g. DP_1 must block the voltage of a single dc level, V, while DP_{N-2} must block (N-2)Vc, assuming that all the capacitor voltages are equal to Vc.

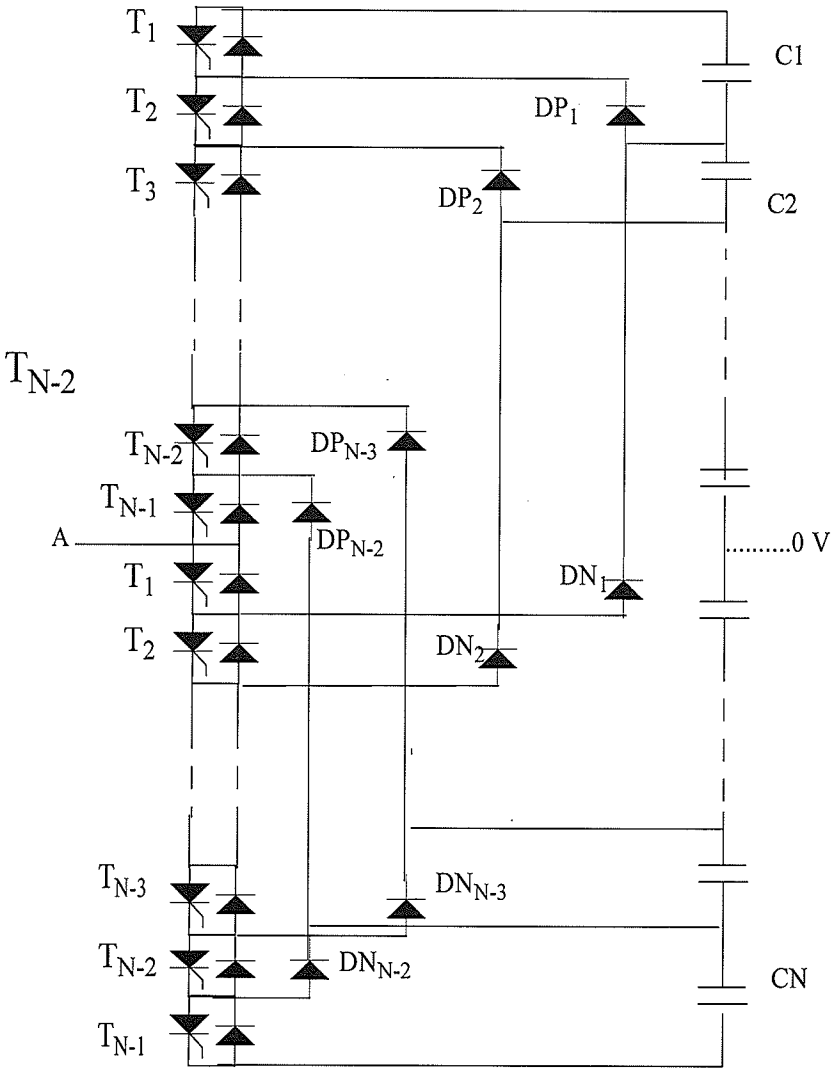


Fig. 3.1 One phase of diode-clamped N-level inverter

Table 3.1. The Gate Logic for Five-level Diode-clamped Inverter

output	The state of GTO thyristors							
(E_a)	T_1	T_2	T_3	T_4	T'_1	T'_2	T'_3	T'_4
$+2V_c$	1	1	1	1	0	0	0	0
$+V_c$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_c$	0	0	0	1	1	1	1	0
$-2V_c$	0	0	0	0	1	1	1	1

In the above Table we assumed that $V_{c1} = V_{c2} = V_{c3} = V_{c4} = V_c$.

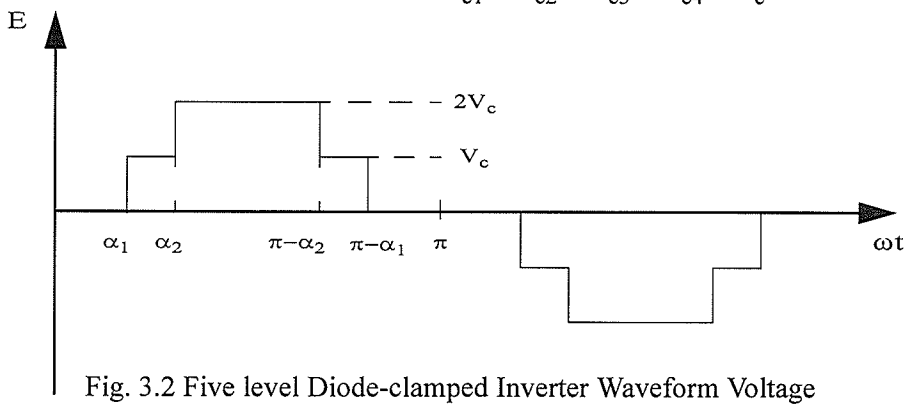


Fig. 3.2 Five level Diode-clamped Inverter Waveform Voltage

3.3 Cascade Multilevel Inverters

3.3.1 Circuit and Working Principle

The cascade inverter is made up from series connected single phase full bridge inverters, each with their own isolated dc bus [12, 13]. Fig. 3.3 illustrates the connection diagram for a wye connection 7-level inverters using the cascade voltage source H-bridge inverters. It is clear from Fig. 3.3 that to have M-level cascade multilevel inverters we need $\left(\frac{M-1}{2}\right)$ H-bridge units in each phase. Each H-bridge inverter can generate three level outputs, V_{dc}, 0, and $-V_{dc}$. Fig. 3.4 shows the structure of one unit of H-bridge inverter and

its three level output voltage waveform. And the output voltage of M-level inverter is a simple sum of the M-rectangular waveforms from each H-bridge inverter for each phase. There are many switching techniques possible to control the output voltage of the H-bridge inverter. Four of them will be discussed in a later section: the Fundamental Frequency Switching (FFS) method and three different Pulse Width Modulation (PWM) techniques.

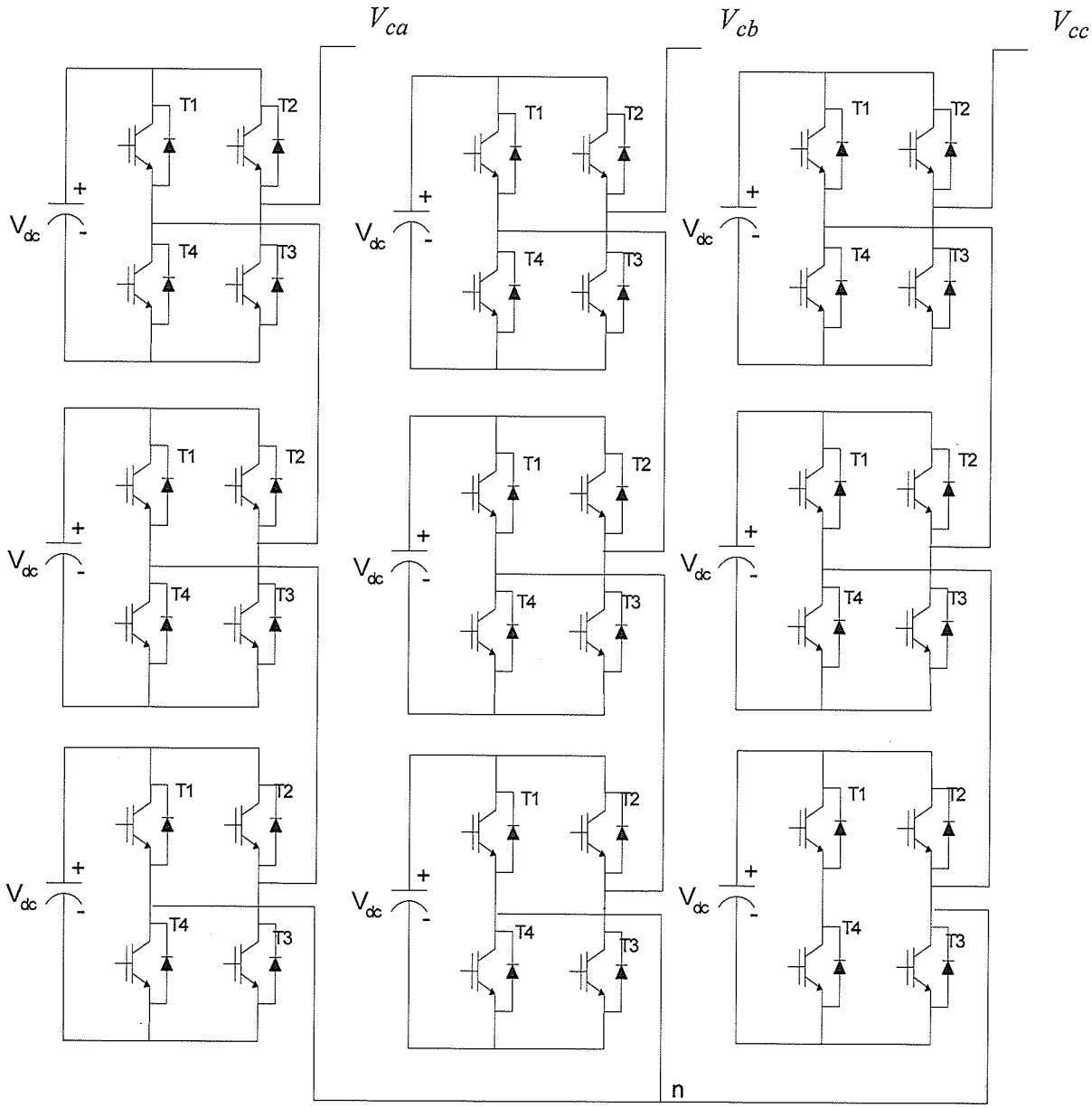


Fig. 3.3 The Three Phase Y-structure 7-level Cascade Inverter

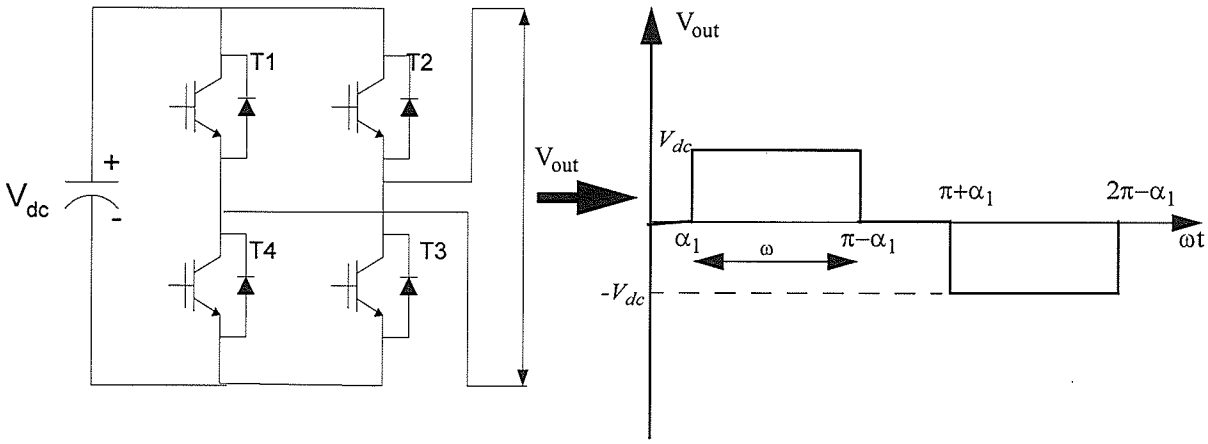


Fig. 3.4. The H-bridge Inverter and its Three Level Output Voltage Waveform

3.3.2 The Advantage of Cascade Multilevel Inverter

There are mainly three types of multilevel inverters, the two most common being the Cascade type and the Diode-clamped type. Listed below are some of the advantages of the cascade type

1- The diode-clamped configuration requires a very large number of clamping diodes whereas the cascade configuration requires a smaller number of diodes.

2- In case of cascade configuration packaging and physical layout is very simple in comparison with diode-clamped configuration due to its modular structure. It is constructed by cascading several voltage source H-bridge inverters.

3-The dc voltage unbalancing between the capacitors can be more severe in the case of the diode-clamped configuration in comparison with the cascade configuration. This is because in the cascade topology, each H-bridge can be controlled independently.

3.3.3 Output Voltage Control of the Cascade Multilevel Inverter

It is clear by examining the cascade inverter structure as described in Section 3.3.1 that the H-bridge inverter forms the building block of the cascade multilevel inverter, therefore by controlling the voltage of each individual H-bridge, the total output voltage of the cascade inverter can be regulated. There are mainly three methods to control the output voltage of the H-bridge inverter as in Fig. 3.4. These are listed below:

1- Controlling the output voltage pulse width (ω) by Fundamental Frequency Switching (FFS) method or PWM technique while keeping the dc voltage fixed. This can be done by controlling the firing angle value of the IGBT or by controlling the modulation index in case of PWM is used as will be discussed later.

2- Controlling the dc voltage (V_{dc}) while keeping the output voltage pulse width (ω) fixed.

3- Controlling both the dc voltage (V_{dc}) and the output voltage pulse width (ω).

In this thesis the first method is used because one objective of the proposed method is to maintain the dc voltage (V_{dc}) across each H-bridge fixed.

3.4 Fundamental Frequency Switching (FFS) of IGBT'S

Using the fundamental frequency switching (FFS) method [14], each IGBT thyristor is switched on and off once during a power frequency (60 Hz) cycle.

As mentioned earlier, the H-bridge inverter forms the building block of the cascade multilevel inverters. For simplification let us consider one phase 7-level cascade multilevel inverter as shown in Fig. 3.5, which consists of three H-bridge inverters [(7-1)/2)) =3] called HBI-1, HBI-2 and HBI-3.

A 7-level voltage waveform can be generated at the output terminal of the 7-level, single phase cascade inverter shown in Fig. 3.5, by applying FFS technique to each H-bridge inverter. Let us start by examining the first H-bridge inverter (HBI-1). It can be seen that the main switching devices T_1, T_2, T_3 and T_4 can be any self-commutated devices such as a Gate-Turn-Off thyristors (IGTO) or an IGBT transistors (for lower rating). In one period T, each switch must be turned on for a half period [0,T/2] and turned off for the remaining period [T/2,T]. For each H-bridge, consider a half cycle duration(π radian). The switching sequence is as follows: Turnon T_1 at $-\alpha_1$, T_4 at $(\pi-\alpha_1)$, T_3 at α_1 and T_2 at $(\pi+\alpha_1)$. Turnoff T_1 at $(\pi-\alpha_1)$, T_4 at $(2\pi-\alpha_1)$, T_3 at $(\pi+\alpha_1)$, and T_2 at $(2\pi+\alpha_1)$. By this way three level outputs + V_{dc}, 0, and - V_{dc} can be generated, as shown in Fig. 3.6(a). If the same role is applied to other two H-bridge inverters HBI-2 and HBI-3 but with different firing angles α_2 and α_3, where $\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$, then

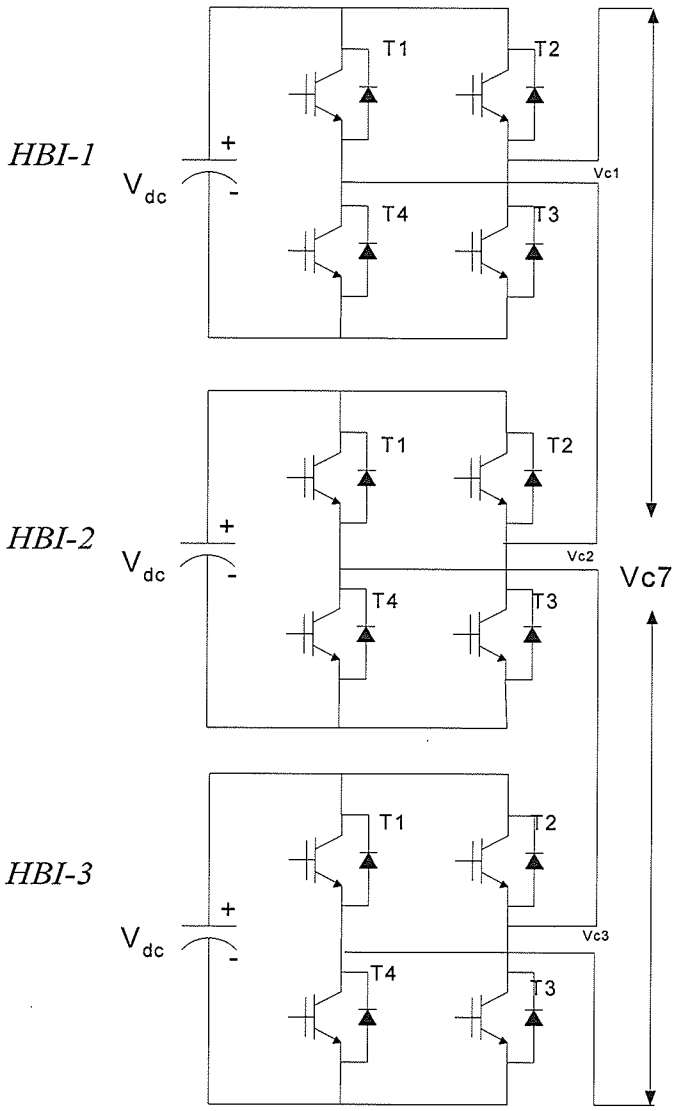
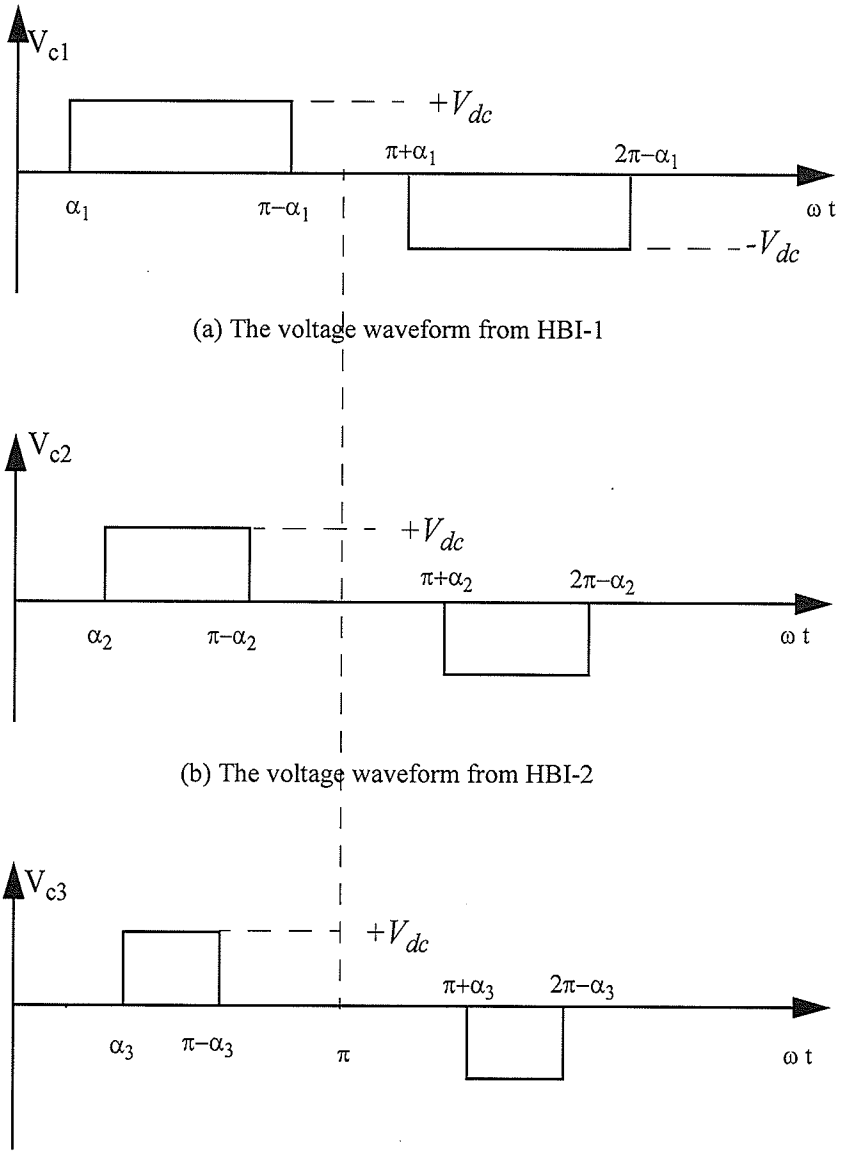


Fig. 3.5: One Phase of a 7-Level Cascaded Multi-level Inverter

an output voltage can be generated from each H-bridge as shown in Fig. 3.6 (b & c). The sum of the three rectangular waveforms generated from HBI-1, HBI-2 and HBI-3 is then

the total output voltage V_{c7} of Fig. 3.5. The 7-level voltage waveform can be achieved as shown in Fig. 3.7.



(a) The voltage waveform from HBI-1

(b) The voltage waveform from HBI-2

(c) The voltage waveform from HBI-3

Fig. 3.6 The Output Voltage Waveform for Each H-bridge

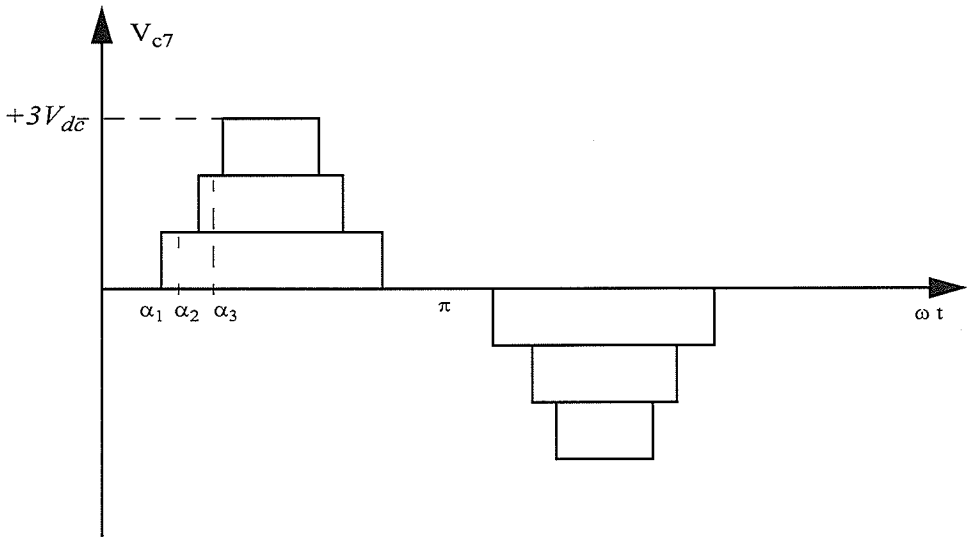


Fig. 3.7 The 7-level Stepped-waveform

Performing the Fourier Transform for this waveform, the total output voltage can be obtained as follow:

$$E(\omega t) = V_c(\alpha_1, \omega t) + V_c(\alpha_2, \omega t) + V_c(\alpha_3, \omega t)$$

Where

$$V_c(\alpha_x, \omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_x\right)\sin(n\omega t)$$

Where $x = 1,2$ or 3
$n = 1, 3, 5, 7,.....$

$$E(\omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_1\right)\sin(n\omega t) + \frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_2\right)\sin(n\omega t)$$

$$\frac{4V_c}{\pi}\sum_n \frac{1}{n}\sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{2} - n\alpha_3\right)\sin(n\omega t)$$

$$E(\omega t) = \frac{4V_c}{\pi}\sum_n \frac{1}{n}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)]\sin(n\omega t) \quad (3.1)$$

Where n = 1, 3, 5, 7,.....

From the formula (3.1), the magnitude of the Fourier coefficients can be obtained, which is equal to the magnitude of the n^{th} harmonic normalized to V_c as follows:

$$H(n) = \frac{4}{\pi n}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] \quad (3.2)$$

Where n = 1, 3, 5, 7,.....

As mentioned before the angles α_1, α_2, and α_3 can be chosen arbitrarily subject to the constraint of $\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$. If suitably selected, these degrees of freedom can be used to obtain a lower harmonic content or a larger fundamental voltage. The degrees of freedom, in choosing the switching angle are equal to ((M-1)/2), where M is the level of the multi-level inverter. In the present case with M = 7, the system has three degrees of freedom. Therefore α_1, α_2, and α_3 can be selected at such values to control the magnitude values of any three harmonics. To entirely eliminate the n^{th} harmonic Equation (3.2) is set to zero for that particular value of n. For example, if it is decided to eliminate the 5^{th}, 7^{th} and the 11^{th} harmonics, three equations can be written, by substituting n=5, 7, 11 in Equation (3.2):

$$\begin{aligned} \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) &= 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) &= 0 \\ \cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) &= 0 \end{aligned} \quad (3.3)$$

The Equations (3.3) are nonlinear transcendental equations which can be solved by an iterative method. By using Newton-Raphson method to solve these equations, different sets of solutions can be obtained. It is obvious that the magnitude of the fundamental component and the harmonic content in the inverter output voltage will change with these switching angles as listed in Table 3.2. In other words, the inverter waveform can be optimized to achieve the larger fundamental component and / or best Total Harmonics Distortion (THD) factor which was defined as the ratio of the root-mean-square of the harmonic content to the root-mean-square of the fundamental quantity [12], which is expressed as a percent of the fundamental, that is:

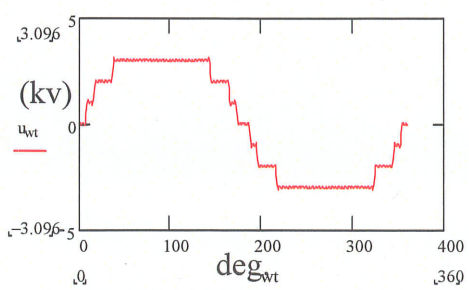
$$THD = 100\sqrt{\sum_{n\neq 1,3n}\left(\frac{V_n}{V_1}\right)^2} \tag{3.4}$$

Table 3.2. Calculated Switching Angles for Different modulation index

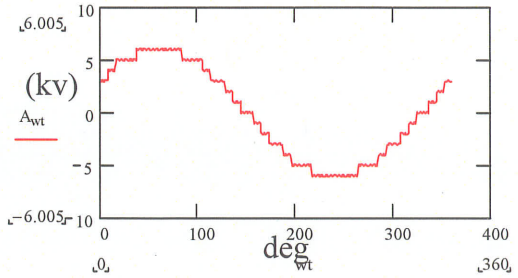
α_1 **(degree)**	α_2 **(degree)**	α_3 **(degree)**	Fundamental component **pu**	**THD**
7.09	15.68	36.17	0.9	5.9%
22.77	49.38	64.57	0.85	9%

Fig. 3.8 shows the line-to-neutral output voltage waveform of 7-level cascaded inverter using the FFS method with α_1= 7.09 degrees, α_2= 15.68 degrees, and α_3= 36.17 degrees. Fig.3.9 illustrates the Fourier analysis of the obtained waveforms. From Fig.3.8(a), it can be seen that the 5, 7, and 11 harmonic orders can be eliminated. The triplen order harmonics, such as third, and ninth, in the line-to-neutral voltage waveform are allowed to exist in

the line-to-neutral waveforms as they will automatically be cancelled in the line-to-line waveform as shown in the spectrum of Fig. 3.9 b.

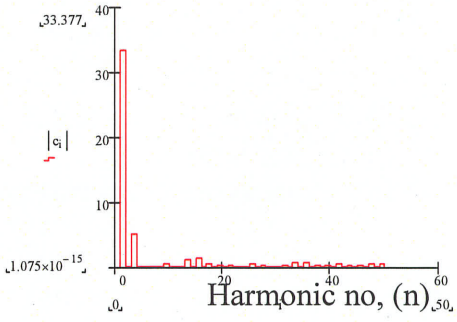


(a) Line-to-neutral

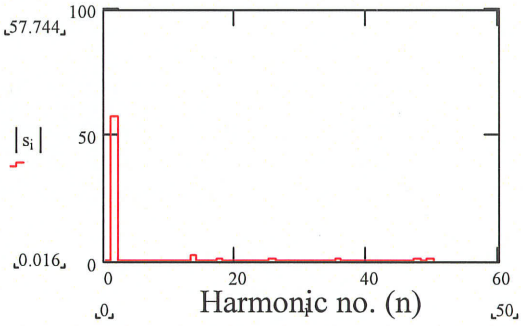


(b) Line-to-line

Fig. 3.8: line-to-neutral& line-to-line output voltage waveform of 7-level cascaded inverter using the FFS method



(a) Line-to-neutral



(b) Line-to-line

Fig. 3.9: Harmonic spectra for line-to-neutral & line-to-line output voltage waveform of 7-level cascaded inverter using the FFS method

3.5 Pulse Width Modulation (PWM) Switching Techniques

Many multilevel PWM techniques [14] have been studied and investigated during the past two decades. Generally, these techniques are the extensions of the traditional two-level PWM strategies. The PWM techniques can be classified into the two categories: the triangle intersection techniques and the direct digital techniques. Recently, with the development of digital technology, the space vector PWM is widely used, due to not only it's relatively easy hardware implementation, but also due to its features of good dc-link voltage utilization and low current

ripple. But this method has a very significant drawback that if the voltage level is more than five, the control algorithm becomes too complex to implement. So it is reasonable to adapt the triangle intersection techniques in applications with a higher number of levels. In this section the principles and the features of three kinds of triangle intersection PWM techniques applied to the cascade multilevel inverter will be described.

3.5.1 Subharmonic Pulse Width Modulation (SHPWM)

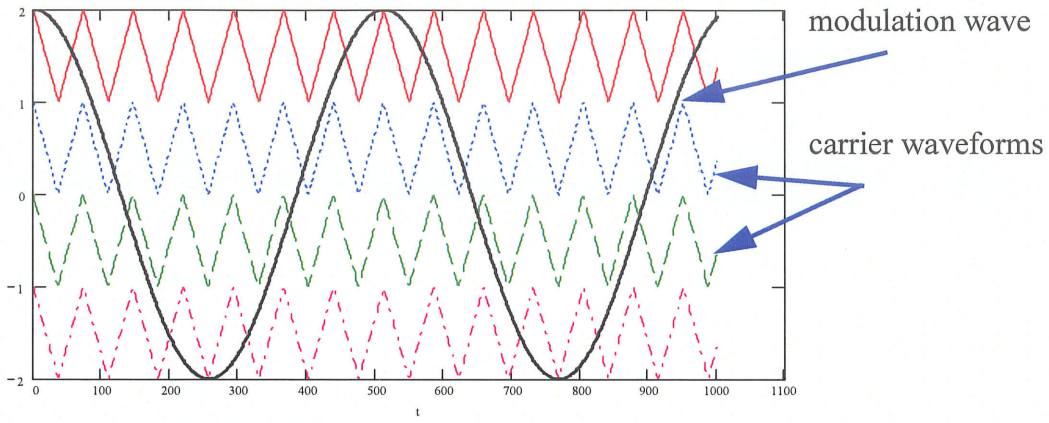
The SHPWM [13] method is an extensions of the traditional two-level PWM strategies, but instead of using one triangular carrier signal it use several triangular carrier signals with only one modulation waveform per phase. For an n-level inverter, n-1 triangular carriers of the same frequency f_c and peak-to-peak amplitude A_c, are arranged so that they fully occupy are contiguous bands in the range of +Vdc and -Vdc. A modulation waveform centered in the middle of the carrier set is then compared with each carrier to determine the voltage level that the converter should switch to. In n-level inverters, the amplitude modulation index (m) and the frequency index (K) are defined as:

$$m = \frac{A_m}{(n-1)A_c} \qquad (3.5)$$

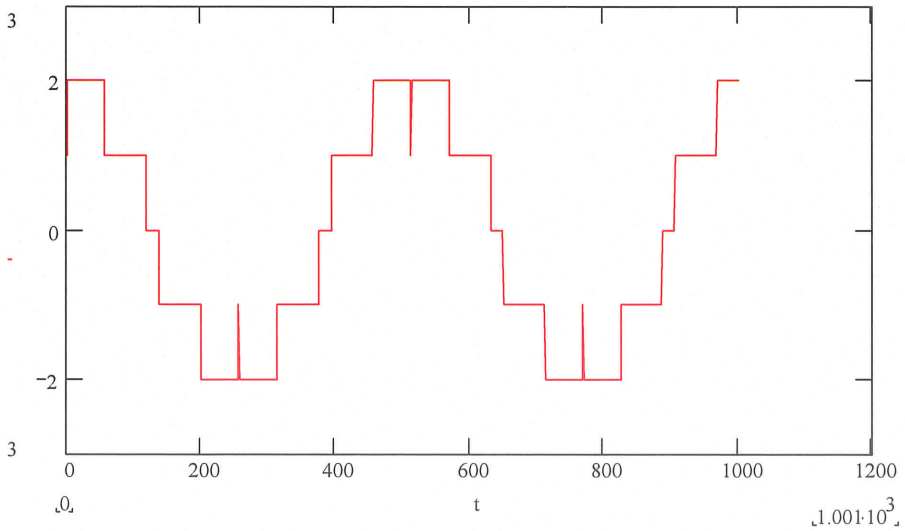
$$K = \frac{f_c}{f_m}$$

Where A_m: The amplitude of the modulation wave
A_c: The amplitude of the carrier wave
f_m: The frequency of the modulation wave
f_c: The frequency of the carrier wave

Fig. 3.10(a) shows the principle of the SHPWM for n=5, k=7, and m =1.0 from the Fig.. It can be seen that there are 4 carrier waveforms, the two carrier which are above the zero reference controlling the switching of the HB-1 and HB-2 during the positive period of the fundamental cycle, while the other two carrier which are below the zero reference take care of the negative period as shown in Fig. 3.10(a).



(a)



(b)

Fig. 3.10 The Principle of the SHPWM for n=5, k=7 and m =1.0

Note that for small m, HB-2 may never switch however, to make sure each H-bridge faces equal stress, the switching patterns are rotated every cycle.

3.5.2 Triangular Carrier Phase Shifting PWM Technique (PS PWM)

For the cascaded inverters, phase-shifted carrier PWM (PSPWM) is the most common strategy. The PS PWM can be considered as a generalization of the traditional pulse width modulation principles, but The PS PWM technique uses 2(n-1) carrier signals of the same amplitude and frequency which are phase shifted by $\theta_{sh} = \frac{\pi}{n}$ to one another to generate the n-level inverter output voltage (n is the number of H-bridge inverters in a multilevel phase leg). This strategy leads to cancellation of all carrier and associated sideband harmonics up to the 2nth carrier group. This effective increase of sampling frequency is highly interesting, since it can be used effectively to reduce the switching frequency in each switching leg. Fig. 3.11 illustrates the carrier and reference arrangements for a single multilevel phase leg of a five level cascaded structure.

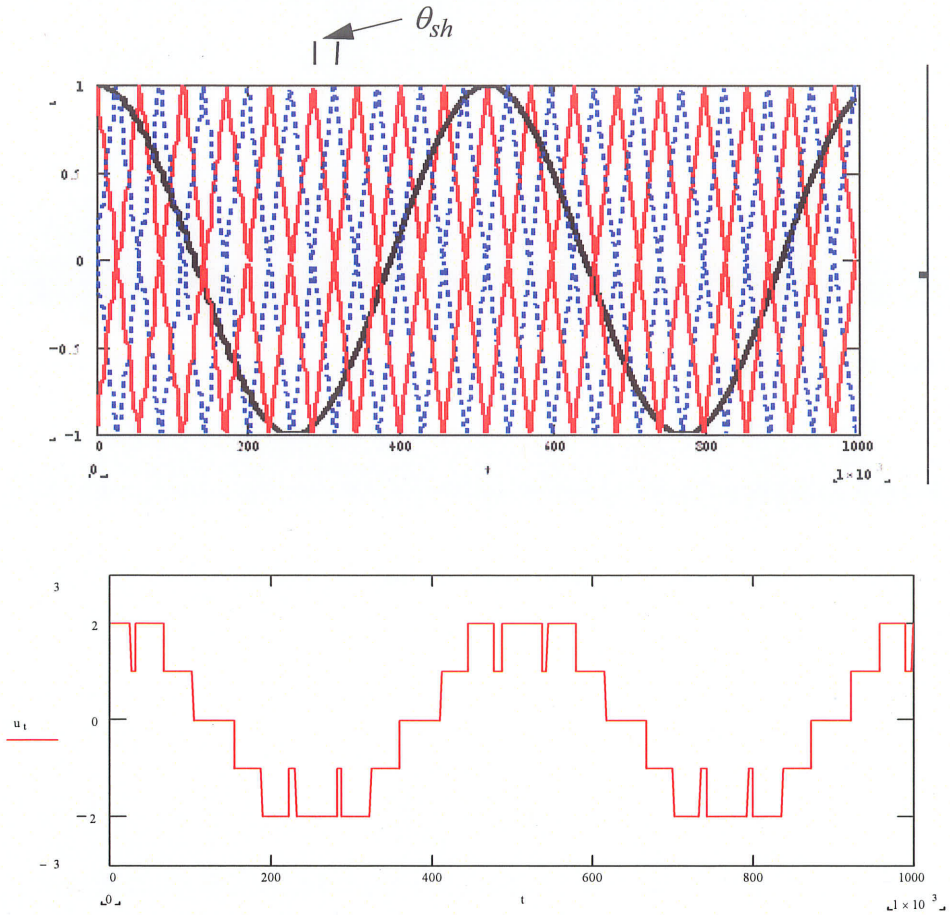


Fig. 3.11 The Principle of the PS-PWM for n=5, k=9 and m =1.0

3.5.3 Switch Frequency Optimal PWM

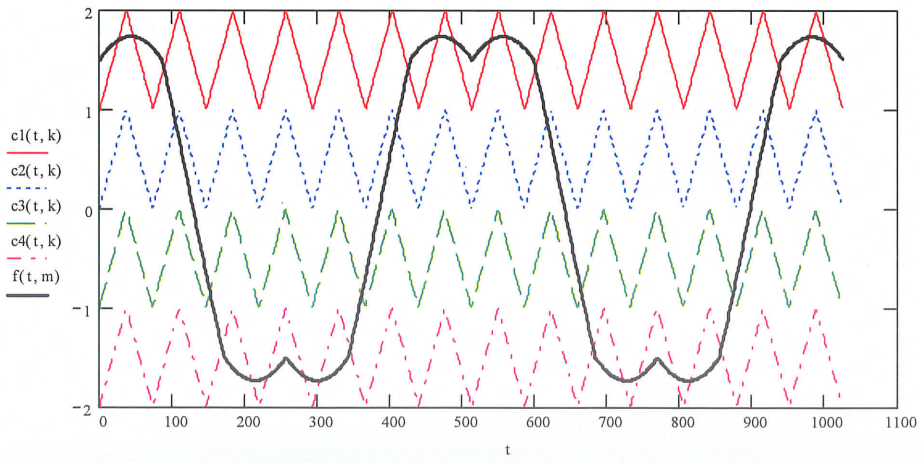
Switch Frequency Optimal PWM (SFO PWM) [14] is something like the SHPWM, except that the modulation waveform for each phase are obtained by subtracting the means instantaneous average of the maximum and minimum of the three reference voltage (V_a, V_b, V_c) as shown in (3.6) from each of the individual reference as shown in (3.7). The addition of the zero sequence (triplen harmonic) voltage continuously centers all of the three reference waveforms in the carrier band. This method can only be used for three

phase system, and it has the advantage of increasing the modulation index by 15% before over modulation occurs.

$$V_{zero} = \frac{max(V_a, V_b, V_c) + min(V_a, V_b, V_c)}{2} \tag{3.6}$$

$$\begin{aligned} V_a'' &= V_a - V_{zero} \\ V_b'' &= V_b - V_{zero} \\ V_c'' &= V_c - V_{zero} \end{aligned} \tag{3.7}$$

The algorithm above is convenient for microprocessor implementation and also analog implementation. The principle of SFO PWM is illustrated in Fig. 3.12.



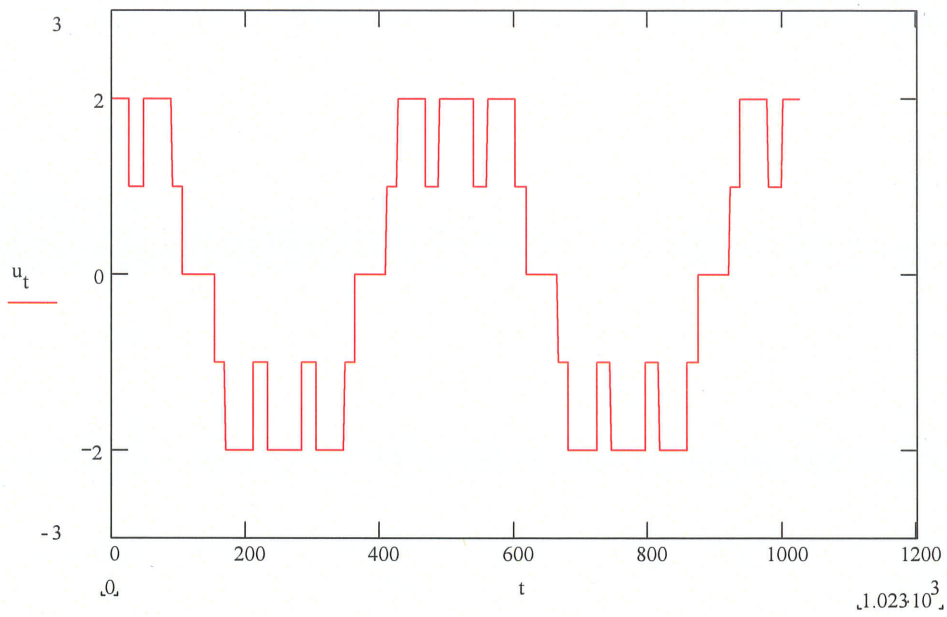


Fig. 3.12 The Principle of the SOF PWM for n=5, k=7 and m=1.0

3.6 Comment on Different Techniques of PWM

- SHPWM and PS PWM are extensions of traditional triangle carrier two-level SPWM strategies to multilevel.
- PS PWM is superior to SHPWM, this is due to it's higher effective carrier frequency, which is n times of carrier frequency of the SHPWM for n-level multilevel converter. That means the harmonics of PS PWM are the lowest.
- The modulation index SFO-PWM method can be increased by about 15% before over modulation due to its modified modulation waveform.
- PS PWM especially suitable for cascaded multilevel inverters.It has better control effect as each phase can be controlled independently.

- In general it can be concluded that in multilevel triangular carrier PWM strategies, there are at least three control degrees of freedom in triangular carrier: frequency, phase and amplitude and also at least three control degrees of freedom in modulation waveform: amplitude, frequency and zero sequence. Composite of some of these control degrees of freedom can generate a good number of PWM strategies.

3.7 Comparison between FFS Method and PWM Techniques

In this section FFS method will be compared with other two types of PWM methods the SHPWM method and SFO PWM method as the PS PWM is special case of the SHPWM, our comparison are based on reducing Total Harmonic Distortion (THD), power loses, and transient response. Off course, the best control strategy is the one which has the lowest harmonic distortion, lowest power loses, and the faster transient response.

3.7.1 Total Harmonic Distortion (THD)

THD is a measure of voltage quality. It is important to a voltage waveform with a low THD. To show the performance of the various techniques FFS method, the SH-PWM and SFO-PWM techniques with respect to the Total Harmonics Distortion (THD) of the output line voltage, the sample Mathcad programs are listed in Appendix A. By running the above mention programs for 5-level inverters, and 7-level inverters, the THD was calculated with different modulation index for each switching technique. The results are sum-

marized as shown: Table 3.3 for FFS method, Table 3.4 for SH-PWM technique, and Table 3.5 for SFO-PWM technique.

Table 3.3: Typical Calculation Results Using FFS

Waveform level	THD
5	10.9%
7	7.6%

Table 3.4: Typical Calculation Results Using SH-PWM

Waveform level	Frequency ratio (k)	Modulation Index (m)	THD
5	9	1	12.1%
		0.9	14%
		0.85	15.2%
		0.8	15.7%
		0.7	19.6%
		0.6	20.3%
		0.5	33.0%
		0.4	37.6%
7	9	1	6.8%
		0.9	10.1%
		0.85	11.6%
		0.8	9.5%
		0.7	14.5%
		0.6	14%
		0.5	11.6%
		0.4	16.6%

Table 3.5: Typical Calculation Results Using SFO-PWM

Waveform level	Frequency ratio (k)	Modulation Index (m)	THD
5	9	1	13.1%
		0.9	13.4%
		0.85	16%
		0.8	18.4%
		0.7	19.2%
		0.6	27%
		0.5	35.6%
		0.4	39.2%
7	9	1	12.4%
		0.9	12.8%
		0.85	12.9%
		0.8	11%
		0.7	12.8%
		0.6	13.4%
		0.5	19.6%
		0.4	21.3%

From the above Tables it can be concluded that:

- As the number of levels in a multilevel inverter is increased, the THD observed to decrease in all types of switching techniques.
- For SH-PWM technique, the modulation index m=1 will give the best THD shown in Table 3.4 which is equal to 6.8% for 7-level waveform.
- For SFO-PWM technique, the modulation index m = 1 will not always give the best THD as shown in Table 3.5 the best THD value is at m = 0.8 for 7-level waveform.

- For 5-level waveform the FFS method has the best THD which equal to 10.9%,on the other hand, for 7-level waveform SFO-PWM technique has the best THD at m=1 which is equal to 6.8%. In general the THD value depends on the m and the level order.

3.7.2 Power Losses

The main element in determining the power losses is that the power losses due to switching of the power electronics switch on and off, therefore to compare the power losses for the different switching methods, the number of IGBT thyristor switched per fundamental cycle should be calculated. By referring to section 3.3 where the principle of each switching techniques was discuss it can be concluded:

- The FFS method has the minimum number of IGBT thyristor switched per fundamental cycle, which is equal to 12 in case of 7-level waveform.
- In case of different techniques of PWM, the number of switches is dependent on the modulation index as well as on the frequency ratio (K) but in general under the same condition the SH-PWM has the minimum switching number in comparison with other PWM techniques.

3.8 Summary

Two multilevel inverter topologies: the diode-clamped multilevel inverter and the H-bridge cascade multilevel inverter were presented in this chapter. The advantages offered by the cascade multilevel inverter were listed such as each bridge can be controlled independently, the inherent energy storage capability of the capacitors, transformer-free opera-

tion, modularized circuit layout, voltage level can be increased without series connection of IGBT thyristors and improved harmonic spectrum.

Three PWM techniques applied to multilevel converter have been studied in this chapter. It is seen that the PS PWM technique offer a good performance with the H- bridge cascade multilevel inverter such as the harmonics of PS PWM are the lowest, PS PWM has better control effect as each level and phase can be controlled independently and the dc voltage for each h-bridge can be control independently as each H-bridge module receives its unique triangular carrier.

CHAPTER 4

SYSTEM MODELING AND PROPOSED CONTROL STRATEGIES

4.1 Introduction

This Chapter describes the one of the original contributions of this thesis. A new DVR configuration and control strategy are presented. The mitigation of a given sag can be achieved with several combinations of reactive and real power. To optimize DVR energy storage the reactive and real powers that must be injected to mitigate sag under various load magnitude and power factor conditions are analytically computed. Based on analytically computed results, a control strategy is proposed where the sag compensation is achieved with minimum real power injection, thereby minimizing the energy storage requirement on the capacitors. Special consideration is also given to the case when the injected voltage attains its ceiling. The proposed mitigation method has the capability to mitigates longer duration sags while maintaining minimal capacitor energy storage

Voltage magnitude, waveform, and frequency are the major factors that dictate the quality of a power supply [11]. Faults at either the transmission or distribution level may cause transient voltage sag or swell in the entire system or a large part of it. Also, under

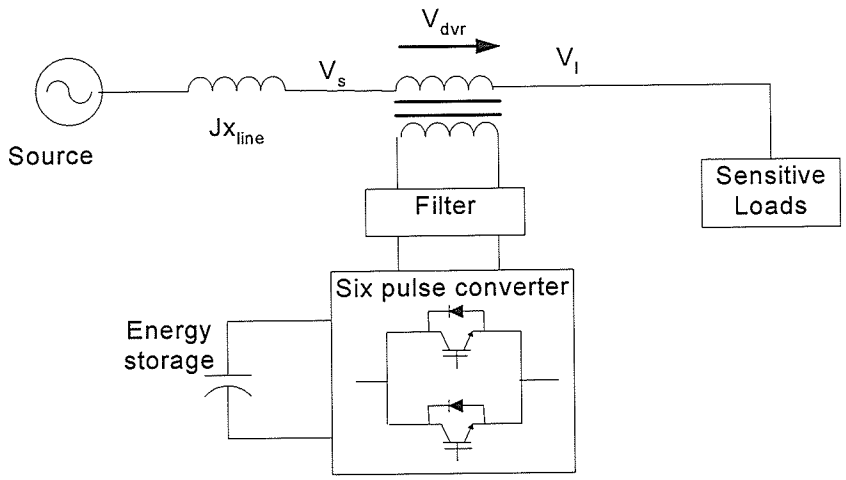


Fig. 4.1: Schematic diagram of a DVR

heavy load conditions, a significant voltage drop may occur in the system. Such voltage variations are not desirable for sensitive loads. The mitigation of a voltage sag requires a fast mitigation control strategy and a convenient topology for the mitigation device. The voltage swells are not as important as voltage sags because voltage swells are less common in distribution systems. The topologies of the mitigating devices that are utilized for voltage sags and swells are confined to a series devices which are commercially called, Dynamic Voltage Restorers (DVRs).

4.2 A dynamic voltage restorer (DVR)

A typical dynamic voltage restorer (DVR) [15-18] as shown in Fig. 4.1 is a power-electronic converter based device capable of protecting sensitive loads from all supply-side disturbances [20]. The basic operating principle of a DVR is to insert a voltage (V_{dvr}) of required magnitude and frequency in series with a distribution feeder to maintain a desired amplitude and waveform for the load voltage (V_l) even when the source voltage (V_s) is unbalanced or distorted. Voltage sag can occur at any instant of time and with dif-

ferent amplitudes and duration. Also, voltage restoration involves energy injection into the distribution systems and this determines the capacity of the energy storage device required in the restoration scheme. A certain amount of voltage restoration is sometimes possible with purely reactive power injection; however in the general case there is also the need to inject real power using a source of dc voltage such as a battery. In many cases, the real power injection is needed only transiently i.e., during a system disturbances. It then becomes possible to use an energy storage device such as a capacitor or superconductive inductor for such energy storage

4.2.1 Major Components of a Conventional DVR

From Fig 4.1 the major conventional DVR components and their function can be listed as follows:

- **Injection / Booster transformer**:

  a) One unit three phase construction.

  b) Connects the DVR to the distribution network via the HV-windings.

  c) Transforms and couples the injected compensating voltages generated by the voltage source converters to the incoming supply voltage

- **Harmonic filter:**

In the design of a DVR, special attentions must be paid to the filtering scheme as it is related to the system dynamic response. Two filtering schemes were seen from the recent literature, which are the inverter-side filter and the line-side filter [19]. Fig. 4.2(a) shows

the configuration of the inverter-side filter, and Fig. 4.2(b) depicts that of the line-side filter. In the scheme of inverter-side filter, a series inductor L_f and a shunt capacitor C_f

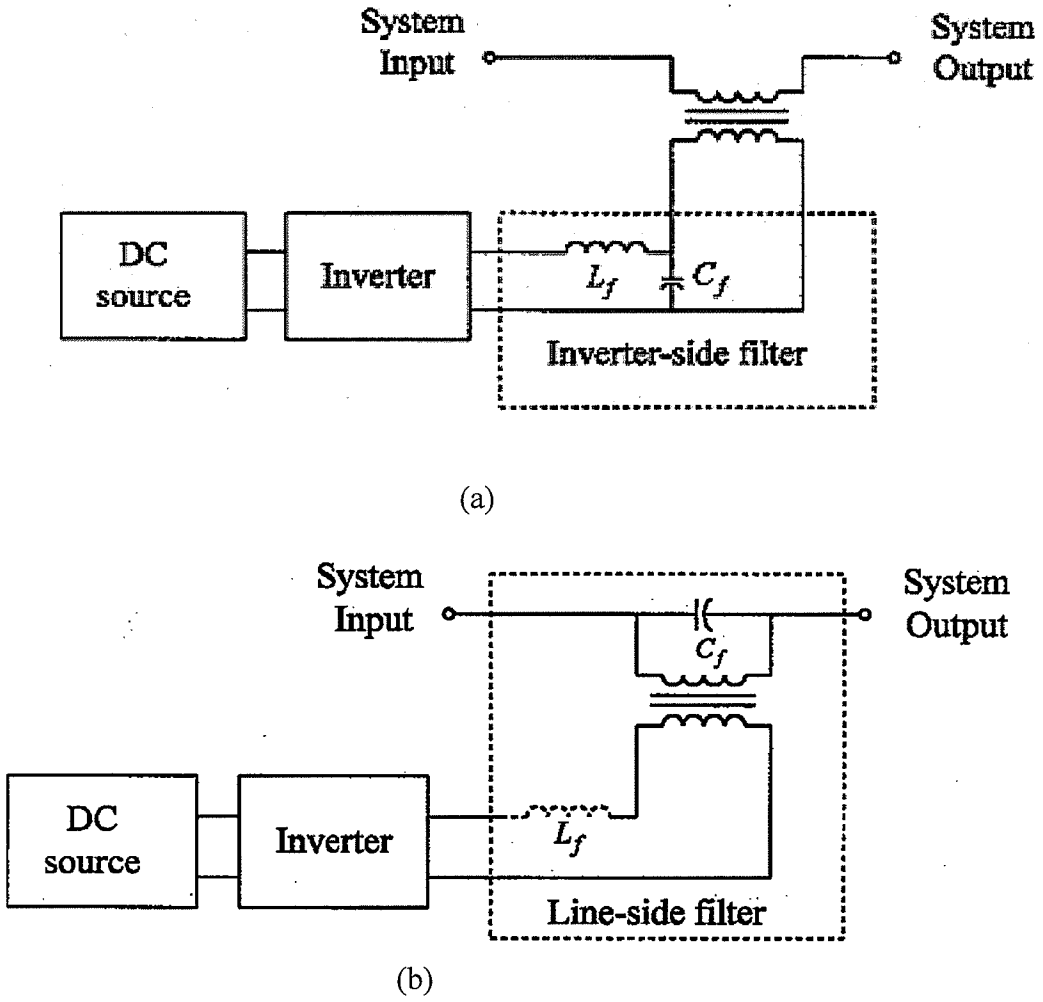


Fig. 4.2 Filtering scheme of the conventional DVR: (a) inverter-side filter and (b) line-side filter.

are inserted between the transformer and switching devices. From the viewpoint of harmonic elimination, the inverter-side filter scheme may be a preferable one. Yet, the insertion of the inductor may introduce an additional voltage-drop component across the series transformer. As for the DVR design of line-side filter, it can be implemented by placing

the filtering scheme on the line-side of the series transformer depicted in Fig. 4.2(b). In such a line-side filter scheme, the leakage flux of series transformer served as the filtering inductance, and the capacitor is placed across the transformer winding. By use of this design, the system will no longer require a physical inductor, avoiding the problem encountered in the inverter-side filter. However, a transport lag delay is encountered between the input and output of the filter network that may be attributed to the utilization of the line-side filter. Note that while the DVR along with the filtering scheme is devoted to cancel out the incoming nuisance harmonics, this resultant transport delay may instead offset the dynamic response in a significant manner, or even lead to a system compensation failure. As the proposed DVR configuration has no transformer it is not possible to utilize transformer inductance as a filter. Hence an external inductor must be added and therefore an inverter-side filter is used.

There are several unique design aspects in the DVR filter. First, the fundamental frequency component of the output voltage of the dc/ac inverter may range from 0.0 to 1.0 p.u., the exact value of which depends on the required operating mode of the DVR. Thus, the commonly used voltage total harmonic distortion (THD) indexes cannot be applied directly on the DVR output voltage (V_{dvr}) as design criteria. Second, under normal operating conditions, the DVR appears as a series load to the system source shown in Fig. 4.1. It should have negligible effect on the source. Third, the restored voltage (V_l) is the composite voltage of the supply voltage (V_s) and the DVR output voltage (V_{dvr}). The introduction of the filter should not result in excessive voltage drop and phase angle difference between the fundamental components of V_{dvr} and the inverter output voltage before the filter. Oth-

erwise, the control scheme of the DVR will be jeopardized. Finally, when investigating the influence of the filter on the inverter rating, contributions both from the power system and the inverter should be considered simultaneously.

- **Energy source e.g. storage capacitor bank.**

  A certain amount of voltage restoration is sometimes possible with purely reactive power injection; however in the general case there is also the need to inject real power using a source of dc voltage such as a battery to supply the necessary energy to the VSC. The different kinds of energy storage devices are superconductive magnetic energy storage (SMES), batteries, and capacitance. In fact, the capacity of the stored energy directly determines the duration of the sag which can be mitigating by the DVR. Batteries are the common choice and can be highly effective if a high voltage battery configuration is used. This high voltage string of batteries can be placed across the regulated dc bus with little or no additional circuitry. However, batteries in general have a short lifetime and often require some type of battery management system, which can be quite costly. An interesting alternative to batteries is the use of ultracapacitors, which have a wider voltage range than batteries and can be directly paralleled across the input bus. Ultracapacitors have a specific energy density less than that of a battery, but a specific power greater than a battery, making them ideal for short (up to several seconds) pulses of power. Certain ultracapacitors (unsymmetrical electrochemical) can hold charge over extended periods of time, so as to act like a battery. However, unlike batteries, these ultracapacitors have a short charge time and much longer lifetime.

The focus of this research is not to give a justification for selection of the energy storage device, but to develop a control algorithm to minimize the amount of energy need to mitigate voltage sags. Essential control aspects are considered in the next section.

In general the main factors determining the size of the capacitor are:

- The maximum capacitor ripple
- The selected steady-state and the allowed transient overvoltage across the capacitor.
- The required energy storage

- **DC charging circuit:**

The dc charging circuit has two main tasks. The first task is to charge the energy source after a sag compensation event. The second task is to maintain dc link voltage at the nominal dc link voltage. Different topologies are used to charge the dc-link such as an external power supply or by connecting the dc side of the DVR to the controlled or uncontrolled rectifier to maintain the dc voltage. The other side of the rectifier can be from a main power line or from an auxiliary feeder. In this research the proposed dc charging method is based on the ability to charge the capacitors by energy drawn from the ac network itself without any connection on the dc side of the DVR which leads to cost reduction of DVR. The proposed method is discussed in detail on the control section.

- **Voltage sourced converters**

A six-pulse voltage sourced converter with its ac output connected to the low voltage windings of the injection transformer is the simplest implementation of such a con-

verter, as shown in Fig. 1.3 of Chapter 1. In normal operation, a 6-pulse bridge voltage source inverter with a charged dc capacitor will give a balanced set of three quasi-square waveforms of the voltages at the output terminal.

Numerous circuit topologies are available for the DVR [22-24]. A widely used method is the two level or multilevel three-phase converter which shares a dc capacitor between all phases. The purpose of this capacitor is mainly to absorb harmonic ripple and hence it has a relatively small energy storage requirement, particularly when operating in balanced conditions. The size of this capacitor has to be increased if needed to provide voltage support in unbalanced conditions. Also, as the capacitor is shared between the three phases, a sag on only one phase may cause a distortion in the injected current waveforms on the other phases.

Another popularly used converter topology is the H-bridge cascade inverter [12, 14]. A single phase of this converter is shown in Fig. 4.3. Converters with this topology are suitable in high-voltage and power system applications due to their ability to synthesize waveforms with better harmonic spectrums, and attain higher voltages with a limited maximum device rating.

1) Modularized circuit layout and packaging is possible because each level has the same structure. Thus adapting the converter for use in various systems with different operating voltages can be achieved by increasing or reducing the number of modules. This also permits transformer-free operation as the voltage of the converter can be matched to the system.
2) Each bridge can be controlled independently permitting efficient single phase voltage compensation.

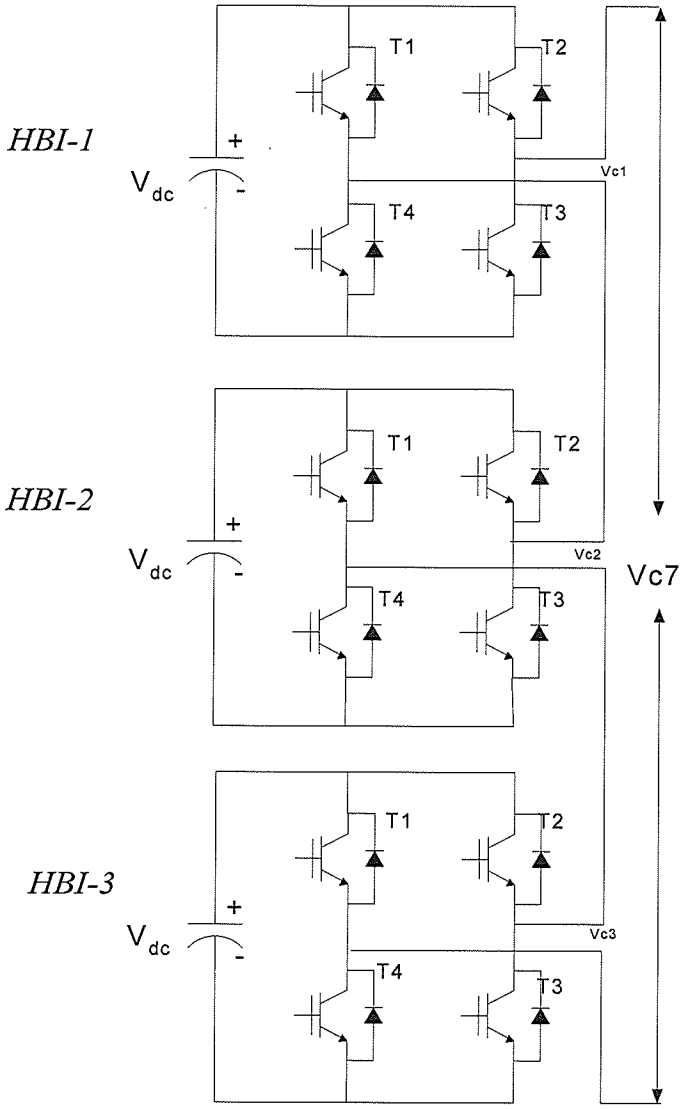


Fig. 4.3: One Phase of a 7-Level Cascaded Multi-level Inverter

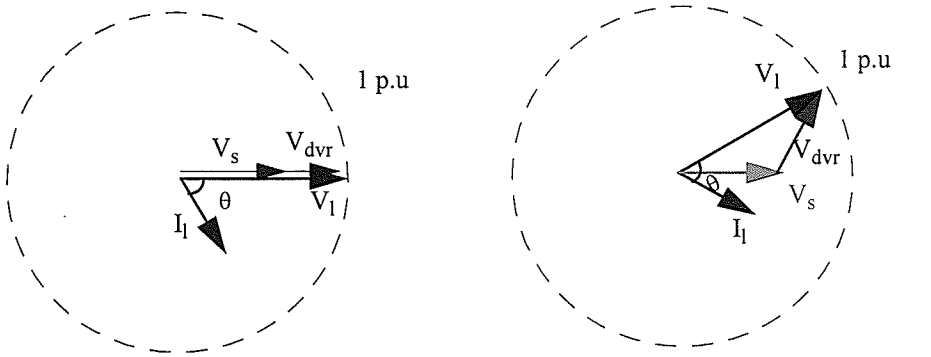
3) The inherent energy storage capability of the capacitors makes this topology ideal for transient injection of real power.

4.3 DVR Operation for Voltage Sag Correction

A typical DVR [25] as shown in Fig. 4.1 is used for voltage correction. When the supply-side voltage V_s changes, the DVR injects a voltage V_{dvr} in such a way that the

desired load voltage magnitude can be maintained. The DVR is essentially a voltage source inverter that produces an ac output voltage and injects it in series with the supply voltage. Note that the voltage injection also typically results in the supply of real and reactive powers. Reactive power can be supplied without taking energy from the dc side capacitor; however the active power must involve the transfer of stored energy. A strategy that permits voltage regulation while minimizing injected active power is attractive because it can prolong the duration over which voltage regulation can be performed.

The phasor diagrams in Fig. 4.4 show the required injected voltage for correcting a given amount of sag. V_s and V_l are the magnitudes of the supply voltage (with sag) and the load voltage (which is to be maintained constant) respectively. It is evident that the injected voltage is smallest when it is in phase with the supply voltage as in Fig. 4.4(a). However, this minimum injected voltage solution is usually not the minimum energy solution. As shown in Fig. 4.4(b), if the injection is carried out in quadrature with the load current I_l, the compensation is achieved with the injection of zero real power. This compensation is achieved at the cost of an increased magnitude for the injected voltage V_{dvr}. Unfortunately the ability to provide complete compensation with zero real power is compromised if the sag voltage exceeds certain limits. The objective of this paper is to develop a control strategy which generates a suitable DVR injection voltage so that a given voltage sag can be corrected with minimum active power injection, taking into account the ceiling on the injected voltage. To develop this strategy, the following analysis



(a) For a in-phase sag correction method

b) For zero active power sag compensation

Fig. 4.4: Phasor diagram for compensation of sag

first investigates the relationship between the injected voltage and real/reactive powers as a function of the magnitude and power factor of the load.r

4.4 Voltage sag Correction by DVR

This section described and analytically analysis three possible control approaches for controlling the DVR. The first approach is by injecting real power only to mitigate the voltage sag. The second approach is by injecting reactive power only to mitigate the voltage sag. Finally, the third approach is the proposed control strategy that optimizes the real energy injected by the DVR. Special consideration is also given to the case when the injected voltage attains its ceiling. The proposed mitigation method has the capability to mitigate longer duration sags while maintaining minimal capacitor energy storage. The analytically analyses are presented below for these three approaches.

The series injected voltage of the DVR as shown in Fig. 4.1 is:

$$V_{dvr}\angle\alpha = V_l\angle 0 - V_s\angle -\delta \tag{4.1}$$

where α and δ are the angle of V_{dvr} and V_s respectively, with the load voltage V_l as the

reference. The complex power injection of the DVR is then:

$$S_{dvr} = V_{dvr}\angle\alpha \times I_l\angle\phi \tag{4.2}$$

Here $I_l\angle(\phi)$ is the load current with

$$I_l = \left(\frac{P_l + jQ_l}{V_l}\right)^* \qquad \phi = \tan^{-1}\left(\frac{Q_l}{P_l}\right) \tag{4.3}$$

4.4.1 Minimum Injected Voltage (Real Power Injection only)

This is the most straight forward and used approach which is to inject the DVR voltage in-phase with the supply side voltage as shown in Fig. 4.4a. However, this approach requires large amounts of real power to mitigate the voltage sag, which means a large energy storage device. Without the larger device is needed, the DVR will not be able to correct sags over a large duration as the energy storage may be depleted sooner. The magnitude of the injected voltage from (4.1) for compensating the sag is:

$$V_{dvr}| = \sqrt{V_l^2 - 2(V_l V_s \cos\delta) + V_s^2} \tag{4.4}$$

For minimum voltage magnitude injection, the injection angle δ can be obtained from (4.4) as:

$$\frac{\partial}{\partial\delta}|V_{dvr}| = 0, \delta = 0 \tag{4.5}$$

From the above result it is clear that if the injection voltage and the supply-side voltage are in-phase the magnitude of the injected voltage is minimum as indicated below:

$$|V_{dvr}| = \sqrt{V_l^2 - 2V_lV_s + V_s^2} = |V_l - V_s| \tag{4.6}$$

It can be seen this (minimum) injected voltage is only a function of the magnitude of the voltage sag, and does not depend on the load's power factor. Unfortunately, this injection is achieved at the cost of real power injection. Naturally the condition

$$|V_{dvr}| < V_{dvrmax} \tag{4.7}$$

must also be satisfied, where V_{dvrmax} is the maximum voltage rating of the DVR. For $V_l = 1$ pu. the magnitude of sag can be defined as:

$$\Delta V_{sag} = 1 - V_s \tag{4.8}$$

from which, the maximum sag that can be compensated is:

$$\Delta V_{sagmax} = V_{dvrmax} \tag{4.9}$$

4.4.2 Compensation with Zero Real Power

Unlike the previous approach this method does not use real power. It uses only reactive power to mitigate the sag by injecting V_{dvr} perpendicular to I_l as shown in Fig. 4.4b. Unfortunately, not all the sags can be mitigated without real power as this method has a limitation as discussed below.

From (4.2) it is evident that if V_{dvr} is perpendicular to I_l (as indicated by (10)) no active power injection by the DVR is required to correct the voltage sag.

$$\alpha = \frac{\pi}{2} - \phi \tag{4.10}$$

Compensation with zero injected real power is only possible for a limited range of sags as indicated below.

From Eqns. (4.1) and (4.10) the supply-side phase angle δ can be written as: (4.11)

$$\delta = \cos^{-1}\left[V_l / \left(\sqrt{V_s^2(1 + \tan\phi^2)}\right)\right] - \phi \tag{4.12}$$

For a feasible value of δ, the argument of the inverse trigonometric function must be less than unity:

$$V_l / \left(\sqrt{V_s^2(1 + \tan\phi^2)}\right) \leq 1 \tag{4.13}$$

from which:

$$V_s \geq V_l \cos\phi \tag{4.14}$$

By substituting (4.8) into (4.14) with $V_l = 1$ pu. we obtain the maximum sag that can be compensated is:

$$\Delta V_{sag} \leq (1 - \cos\phi) \tag{4.15}$$

The injected voltage is as given in (4.4) with δ as specified in (4.12). Comparing this with (4.6) (specifically for minimum voltage injection), it is seen that mitigating the sag by purely reactive power is achieved at the cost of a larger injected voltage. Hence considering the maximum rating of the DVR as given by (4.7), the largest sag which can be compensated by zero active power is:

$$|\Delta V_{sag}|_{max} = \sqrt{V_l^2 - 2V_l V_{dvrmax} \cdot \sin(\phi)} \tag{4.16}$$

Note that the above sag is smaller than that which can be compensated by the minimum voltage injection method (refer to (4.9)).

If the sag (ΔV_{sag}) is small enough as required by (4.14), the desired voltage correction can be achieved without injecting any active power into the system. It can be seen also that (4.14) is a function of load power factor.

A new strategy is developed below which attempts to compensate the sag with zero active power as long as the conditions of (4.14) and (4.16) are satisfied; and uses minimum real power injection otherwise.

4.5 Proposed Minimal Active Power Mitigation Strategy

As seen in the earlier sections, compensation with real power injection dose not permit the mitigation of long duration sags with capacitive energy storage. The method proposed in the above section achieves compensation with zero real power injection and can sustain longer sags only if the sag is not above its critical level $(1 - \cos\phi)$ as in (4.14). For more severe sags, some amount of real power injection is inevitable, but should be minimized. This section proposes such a modified approach.

4.5.1 Sag smaller than that limiting value from (14)

As long the sag is sufficiently small so that (4.14) is satisfied, it is possible to compensate the sag with the injection of reactive power only. This is achieved by injecting V_{dvr} perpendicular to I_l.

4.5.2 Sag larger than the limiting value from (14)

When the sag is larger than the limit from (4.14), V_{dvr} is injected with an angle calculated to minimize the active power injected by the DVR.

The active power flows at the supply and the load sides in Fig. 3(b) are:

$$P_s = V_s I_l \cos(\phi - \delta), \quad P_l = V_l I_l \cos\phi \tag{4.17}$$

The DVR injected active power (P_{dvr}) can be expressed as:

$$P_{dvr} = P_l - P_s = V_l I_l \left(\cos\phi - \left(\frac{V_s}{V_l} \right) \cos(\phi - \delta) \right) \tag{4.18}$$

If the load voltage and current V_l and I_l are used as base quantities (1 pu) the injected active power is:

$$P_{dvr} = \cos\phi - V_s \cos(\phi - \delta) \tag{4.19}$$

which is a minimum when

$$\cos(\phi - \delta) = 1 \qquad ie \qquad \phi = \delta \tag{4.20}$$

This implies that the injected voltage should keep the load current I_l in phase with the supply voltage V_s while compensating for the sag. As V_l leads I_l (and hence V_s) by the power factor angle ϕ as shown in Fig. 4(a). The injected voltage V_{dvr} can thus be written as:

$$V_{dvr}\angle\alpha = V_l\angle 0 - V_s\angle -\phi \tag{4.21}$$

from which:

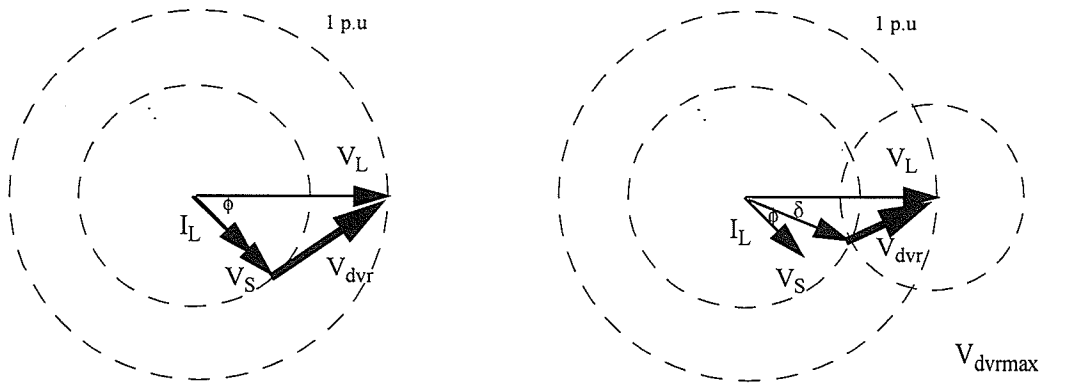
$$\alpha = \tan^{-1}\left(\frac{V_s \sin\phi}{V_l - V_s \cos\phi}\right) \tag{4.22}$$

$$\left|V_{dvr}\right| = \sqrt{V_l^2 - 2V_l V_s \cos\phi + V_s^2} \tag{4.23}$$

It can be seen that Eqns. (4.21) and (4.22) are function of the load power factor and the (sagged) supply voltage.

4.5.3 Sag compensation when DVR voltage rating is breached

The above voltage is of course, constrained by the DVR rating (4.7). If the constraint boundary is attained, the load current I_l can no longer be in phase with the supply voltage V_s as shown in Fig.4.5(b) where V_{dvrmax} =0.6 pu. In this case the strategy requires some



(a) Minimum Real Power Injection with V_{dvrmax} = 1.0 pu (b) With voltage limit imposed by DVR rating (V_{dvrmax} =0.6 pu)

Fig. 4.5. Phasor diagram proposed method for sag compensation

modification as indicated below. When the ceiling (See (4.7)) is reached, (4.4) can be rewritten with $V_{dvr} = V_{dvrmax}$ as:

$$\left|V_{dvrmax}\right| = \sqrt{V_l^2 - 2(V_l V_s \cos\delta) + V_s^2} \tag{4.24}$$

From (4.24) the supply-side phase angle δ can be written as:

$$\delta = \cos^{-1}\left(\frac{V_L^2 + V_s^2 - V_{dvrmax}^2}{2V_s V_l}\right) \tag{4.25}$$

After some mathematical simplification, the angle and the magnitude required for the injected voltage can be shown to be:

$$\alpha = \sin^{-1}\left(\frac{V_s \sin\delta}{V_{dvrmax}}\right) \tag{4.26}$$

$$|V_{dvr}| = V_{dvrmax} \tag{4.27}$$

4.6 Comparison between the above methods of sag mitigation

To demonstrate the effect of load power factor and sag depth on the above discussed three mitigation methods, the minimum injection method, the no real power injection method and the proposed minimum active injected power method. The three methods were tested under four different load power factor with varying the sag depth from zero to one per unit

For the proposed strategy, the required DVR injected active power and injected voltage magnitude is plotted against the voltage sag of the supply-side voltage (with V_{dvrmax} = 1.0 pu) as shown in Figs. 4.6 & 4.7 respectively. The DVR's injected voltage rating is large enough (1.0 pu) so that this limit is not exceeded in the cases considered. Four different load power factors (0.5 pu, 0.6 pu, 0.8 pu and 0.9 pu) are considered in the plots. It is evident from (4.14) (with $V_l = 1\ pu$) that if the voltage sag is less than $(1 - \cos\phi)$, no active power injection is required to correct the voltage. Curiously this means that for a given sag magnitude, the poorer the power factor, the easier it is to compensate without real power injection.

Fig. 4.7 shows how the required injected voltage magnitude varies as a function of the sag for the four different power factors. The initial part of each curve corresponds to compensation without real power injection. As seen from Fig. 4.6, this can only be achieved as

long as the sag does not exceed $(1-\cos\phi)$. Beyond this value, both real and reactive power injection is needed and the injected voltage follows a different characteristic with a much reduced slope.

Fig. 4.8 shows the injected voltages as functions of sag for the in-phase compensation method as well as the proposed energy conserving method for a typical load power factor of 0.6. As can be observed, the saving in energy is achieved at the expense of a larger injected voltage magnitude. Fig. 4.9 shows a plot of the required power in the two alternatives, where the considerable power savings from the proposed approach are clearly evident. Indeed, no real power is needed to compensate sags < 0.4 p.u.

In the above cases, the DVR's rating was large (1.0 pu), so it was never reached. The examples below demonstrate what happens when this limit is reached. In the particular case considered, a DVR with a lower rating of V_{dvrmax} = 0.6 pu is compared against one with a larger rating of V_{dvrmax} =1.0 pu. Fig.4.10 shows the injected voltage as a function of sag for the proposed method for a typical load power factor of 0.6. Note that the DVR rated at 1.0 pu always operates within its rating (as also seen in Fig.4.7). In contrast, for the DVR rated at 0.6 pu, the rating is reached when the sag exceeds 0.35 pu (approx.). Fig. 4.11 shows the corresponding real power injections for the two different ratings. As expected, the DVR with the smaller (0.6 pu) rating requires more real power for the same level of compensation and hence will not be able to correct sags over a large duration as the energy storage may be depleted sooner.

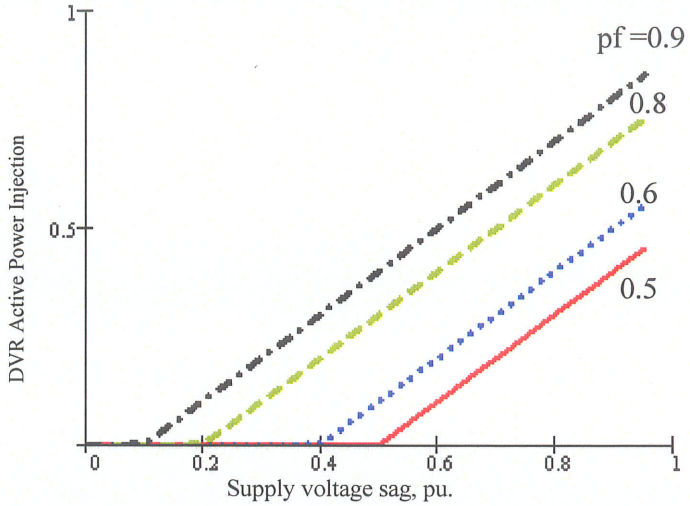


Fig.4.6. Injected DVR active power verses the voltage sag for four different power factors

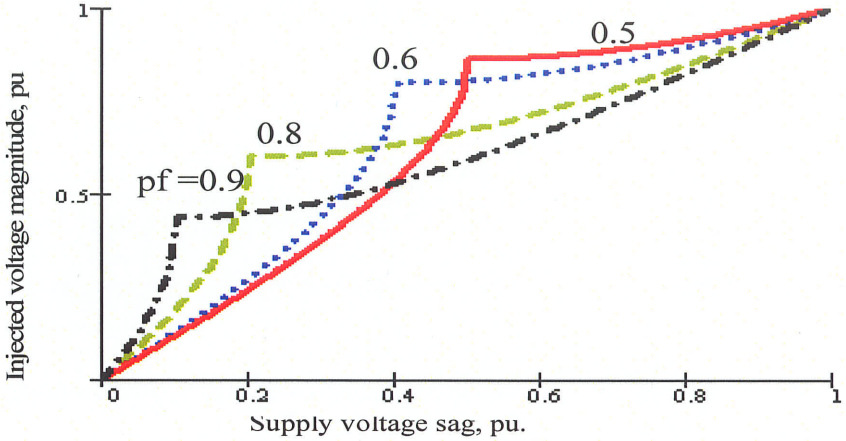


Fig.4.7. Injected voltage magnitude of DVR verses the voltage sag for four different power factors

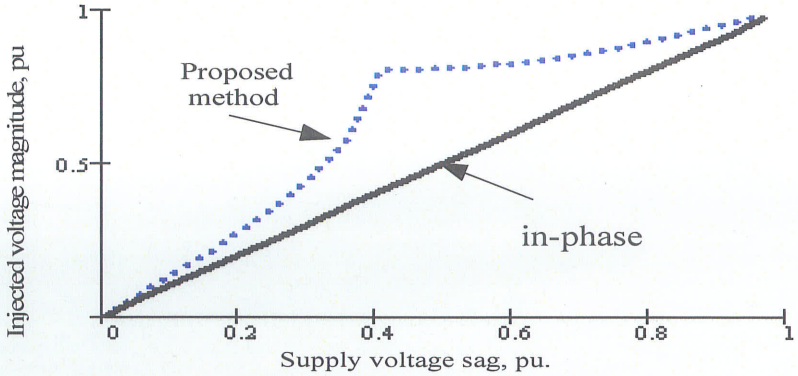


Fig. 4.8: Comparison between in-phase with minimum active power injection based on the voltage magnitude injected by DVR

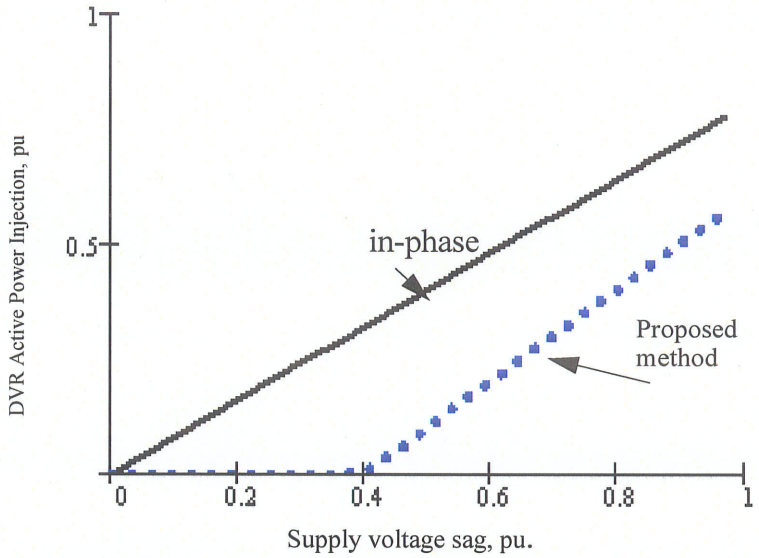


Fig. 4.9: Comparison between in-phase with minimum active power injection based on active power injected by DVR

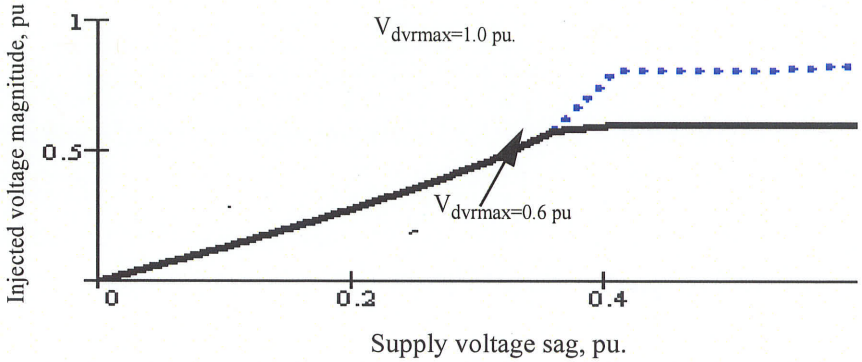


Fig. 4.10 The injected voltage magnitude for the proposed compensation method with two different ceiling rating (V_{dvrmax})

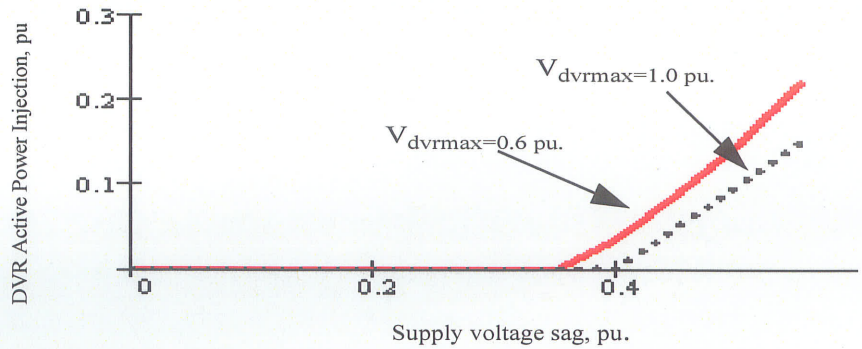


Fig.4.11. The active power injection for the proposed compensation method with two different ceiling rating (V_{dvrmax})

4.7 Control Method

Two commonly used control approaches applied to DVR's include open loop control and closed loop control [24-26]. The open loop methods are generally faster as the required injected voltage can be calculated from the sag magnitude and quickly applied. The closed loop methods are better at reducing steady state error, but are not as fast in correcting the sag. The principal control system is shown in Fig. 4.12 and is essentially an open loop system. A slower feedback loop (not shown can be used to change the reference settings so as to eliminate all steady state error). The various components of the controller are described below.

4.7.1 Synchronization and voltage measurement

This block uses a phase locked loop that generates a reference angle θ in phase with the fundamental positive sequence component of the supply side voltage of the DVR [24]. It also generates the voltage measurement signals of the supply voltage. It is convenient to use a rotating reference frame to express the DVR variables, as then these quantities become dc in the steady state. This is achieved using a two step procedure as shown in (4.28) and (4.29), first by reducing from three to two variables (the α β frame) and then resolving these time varying vectors u_α and u_β on the instantaneous phase angle θ of the reference voltage.

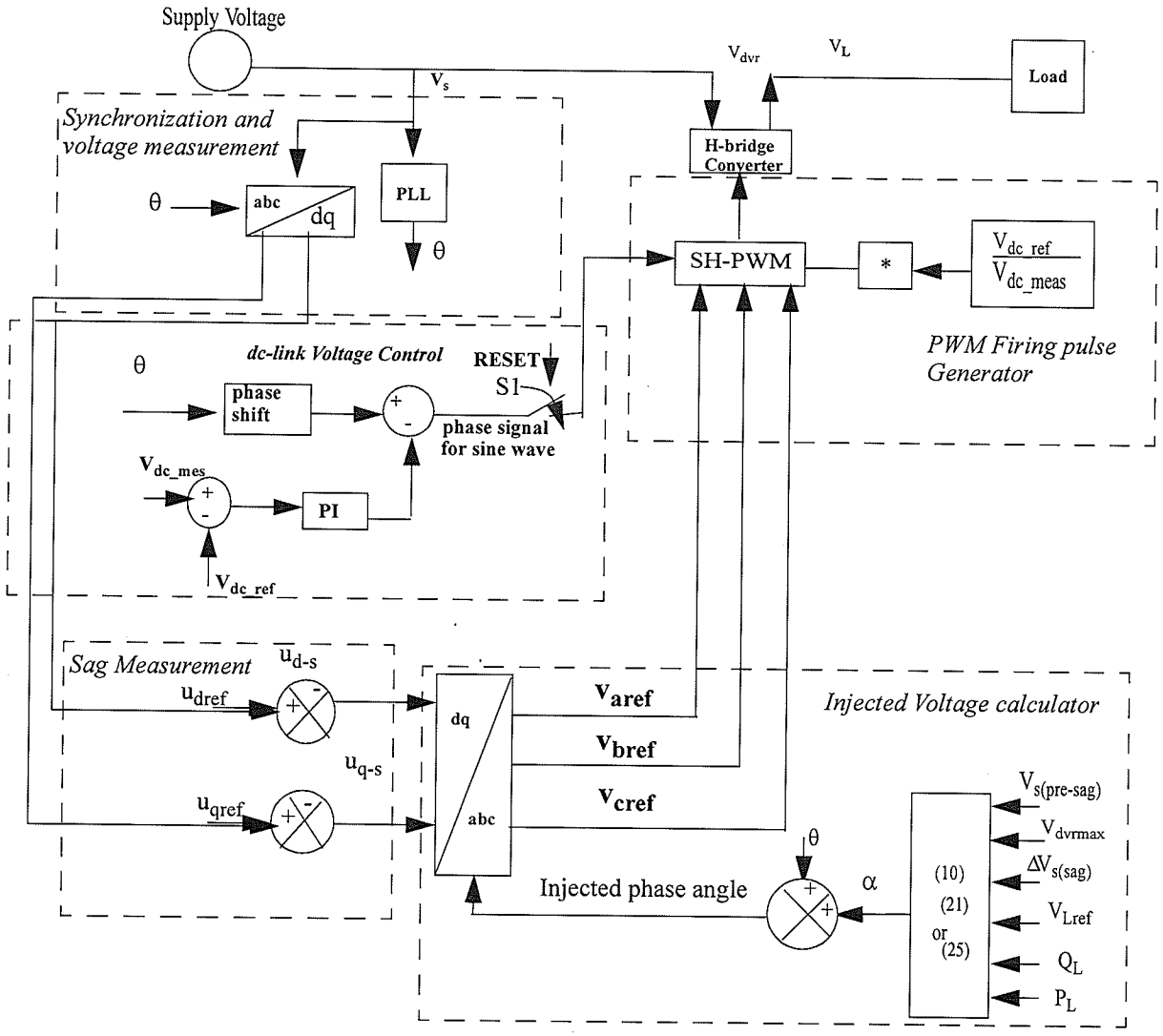


Fig. 4.12 Control structure of DVR with rotating dq-reference frame

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{4.28}$$

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{4.29}$$

4.7.2 Sag Measurement

The sag is calculated by subtracting the long term steady state value (u_{dref}, u_{qref} in d-q components) of the supply voltage with the instantaneous voltage ($u_{s\text{-}d}$ and $u_{s\text{-}q}$). This allows for detection of symmetrical and nonsymmetrical sags, as well as any associated phase jump. In order to prevent undue control action, the undervoltage is only considered to be sag if it exceeds a certain threshold as in (4.30).

$$\left|\bar{u}_{sag,dq}\right| > (u_{threshold}) = 0.05pu \tag{4.30}$$

where

$$\left|\bar{u}_{sag,dq}\right| = \sqrt{(u_{ref,d} - u_{s,d})^2 + (u_{ref,q} - u_{s,q})^2} \tag{4.31}$$

in which $u_{red,d}$ *and* $u_{ref,q}$ are the reference values for the d and q voltages.

4.7.3 Injected Voltage Calculator

Depending on the operating regime, in this block of Eqns (4.10), (4.21), or (4.26) are used to determine the angle at which the compensating voltage is to be injected. On the other hand, Eqns (4.4), (4.22), or (4.27) are used to determine the magnitude of the injected voltage. The block calculate the angle and the magnitude by considering the load voltage

reference (V_{Lref}, which is nominally 1 pu), V_{dvrmax}, sag voltage and the load power factor which is determined by measurement of the steady state (pre-sag) real and reactive powers in the load. The reference values for the compensating voltages are essentially the sag voltages obtained through the dq to abc transformation (inverse of eqns (4.28) and (4.29)).

4.7.4 Dc-link (Capacitor) Voltage Control

During system normal operation (switch S1 is closed) the dc-links for each H-bridge are maintained and recharged to the dc-link reference value by controlling the phase angle between the inverter output and supply voltage to control the flow of the real power into and out of the capacitors of each H-bridge. Balance and equal dc voltage across each H-bridge capacitor is done by controlling the phase angle for each H-bridge carrier waveform of the triangular carrier phase-shifting PWM technique described below. This mechanism prevents unbalance of capacitors voltages from system condition and disturbances.

4.7.5 PWM Based Firing Pulse Generators

The purpose of this block is to derive the firing pulses to the IGBT switches of the series cascade converter so that the desired reference voltages v_{aref}, v_{bref}, v_{cref} calculated in the previous block are actually applied by the converter. This is achieved by using these three phase voltages as the modulation signals for the Phase-Shifting Pulse Width Modulation technique (PS-PWM) described below.

The triangular carrier phase-shifting PWM techniques is a PWM technique [14] especially suitable for cascaded multilevel inverters. The control principle of the PS PWM

method is the switching logic controller, in which each H-bridge module receives its unique triangular carrier, which is phase shifted with the respect to its neighbors with only one modulation wave per phase. For an n-level inverter, n-1 triangular carriers of the same frequency f_c and the same peak-to-peak amplitude A_c, are used so that the bands they occupy are contiguous. Although in this research, a n=7 level converter has been used, the 5 level converter is easier to elucidate the basic concepts. As illustrated in Fig. 4.13, this method is to use multiple converter modules, the device's of which are switched in staggered intervals to create the effect of a high sampling rate, its effective triangular carrier number is equal to n*k, where n is the number of converter modules. The triangular carrier phase shift for n modules is $\theta_{sh} = \frac{2\pi}{nk}$. Effectively this method produces at the output of the bridge (ac side) a pulsed waveform, which is essentially a replica of the desired modulating wave. The undesirable harmonics are of high order (typically clustered around the carrier frequency) and hence are easy to filter. One additional enhancement over the conventional PS-PWM method is the inclusion of an additional compensation signal that is inversely proportional to the dc voltage. The modulating waves are multiplied by this signal to ensure that the final output of the bridge has the desired magnitude even when the dc capacitor voltage is discharging, i.e., when the bridge is transiently supplying real power.

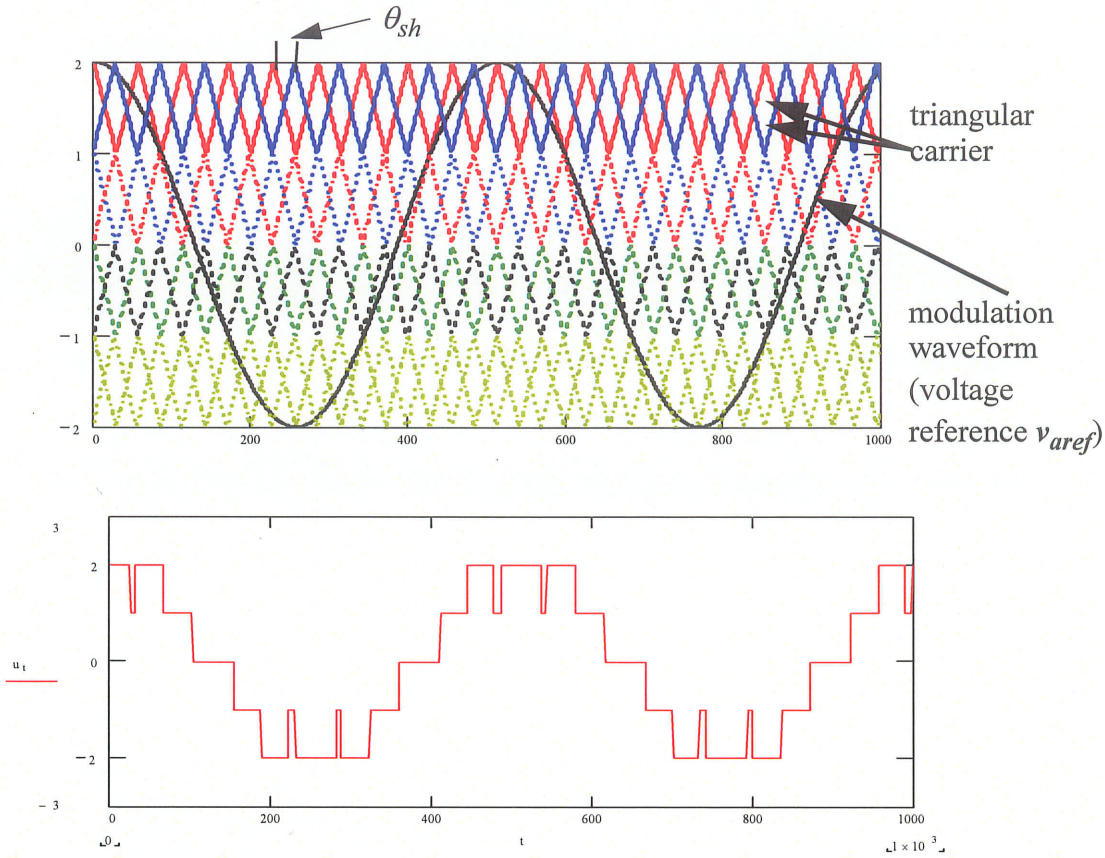


Fig. 4.13 The Principle of the PS-PWM for n=5, k=9 and MI=1.0

The triangle wave frequency used was selected as 1.5 kHz, which is typical for many Power Electronic Applications for Power Systems. This frequency is large enough to provide a harmonic spectrum with minimal low order harmonics, yet small enough not to cause excessive switching losses

4.8 Sags Detection Methods

Detection of sag is an important first step in sag correction. The faster a sag can be detected, the quicker it can be compensated. Discussed below are a number of detection methods in literature [26].

- Monitoring the peak values of the supply.

- Monitoring of $\sqrt{V_d^2 + V_q^2}$ or V_d in a vector controller.
- Locking a narrow band-pass filter or Phase-Locked-Loop (PLL) to each phase.
- Applying the Fourier Transform to each phase.
- Applying the Wavelet Transformer to each phase.

Apart from the vector controller, the other sag detection methods can to be applied to each of the three supply phases separately.

4.8.1 *Monitoring the peak values of the supply*

The simplest method of monitoring the supply is to monitor the peak, or amplitude, of the supply. This can be achieved by simply finding the point at which the gradient of each of the supply phases is zero, then comparing the supply value at that instant with a reference. A controller could be set to recognize if there is a difference greater than 5% and switch in a DVR or appropriate corrective device. The gradient is found for example from (4.32).

$$Gradient = \frac{V_t - V_{t-\Delta T}}{\Delta T} \tag{4.32}$$

where V_t is the voltage value at the time instant t, and $V_{t-\Delta T}$ is the voltage value at the time instant $t - \Delta T$.

This method returns the sag depth, start and end times although no phase shift information is readily available. The drawback is that it can take up-to half a cycle for the sag depth information to become available and the possibility of noise affecting the differential function. The lack of readily available phase shift information is also less than desirable.

4.8.2 *Monitoring of $\sqrt{V_d^2+V_q^2}$ or V_d in a vector controller.*

This is an obvious method as it utilizes the Vector Control method, which is part of the core DVR control system. The three supply phases are converted into one phasor *Vs* which itself is comprised of two orthogonal components V_α *and* V_β. A synchronous reference frame is locked to *Vs* via a Phase-Locked-Loop, Fig 4.9. The vectors are generated by the following formulae:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & 0.866 & -0.866 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.33}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{4.34}$$

If the sag is not accompanied by any phase shift then the following expression is true

$$\left(|V_s| = V_d = \sqrt{V_d^2+V_q^2}\right) \quad , V_q = 0 \tag{4.35}$$

This is simplest type in terms sag detection and control, where monitoring either $\sqrt{V_d^2+V_q^2}$ *or* V_d will return the state of the supply at any instant in time and hence detect whether or not a sag has occurred. If the balanced sag is accompanied by a balanced phase jump then (4.35) is no longer valid, because the PLL has to first track the new angle. Hence initially

$$|V_s| = \sqrt{V_d^2 + V_q}^2 \tag{4.36}$$

Monitoring 'Vd' will return the sag depth while monitoring and manipulation of 'Vq' will return the initial phase jump information.

If unbalanced sag occurs the ability for this method to return information regarding the individual supply phases is compromised.

4.8.3 Locking a narrow band-pass filter or Phase-Locked-Loop (PLL) to each phase.

This sag detection method is similar to the previous method, except that the PLL is applied to each supply phase independently and is tuned to respond to phase jumps in the supply quickly.

Although this method can track changes in supply phase it cannot directly return information regarding sag depth. As with the previous PLL method it can be easily be implemented in real-time and can be used if only phase jump information is required.

4.8.4 Applying the Fourier Transform (FFT) to each phase.

A technique that can return information regarding the state of a system supply is the Fourier Transform to each supply phase. The advantage of this method is that it can return magnitude and phase of each frequency component within the supply, which is particularly important if there are harmonics present, such as 5th or 7th. In order to prevent errors occurring with the information returned regarding the fundamental (50Hz) the previous

methods effectively filter out harmonics other than the fundamental. The effect of doing so can be to introduce transient delays in detecting changes in the phase of the fundamental. The Fourier Transform or the practical digital implementation of it, the 'Windowed Fast Fourier Transform' (WFFT) automatically accounts for all frequencies

4.9 Phase-Locked-Loop

As seen in section 4.7, the PLL as shown in Fig. 4.14 is an important component in several of the methods. Its purpose and operation are briefly discussed here. The output of the compensator must be able to stay synchronized with the source-voltage and quickly keep up with external phase-shifts or frequency variations. A phase-locked-loop is used to feed the angular displacements ($\theta_a, \theta_b, \theta_c$) of the source voltage to the control system. Fig. 4.15 overleaf shows the outputs of this phase-locked-loop.

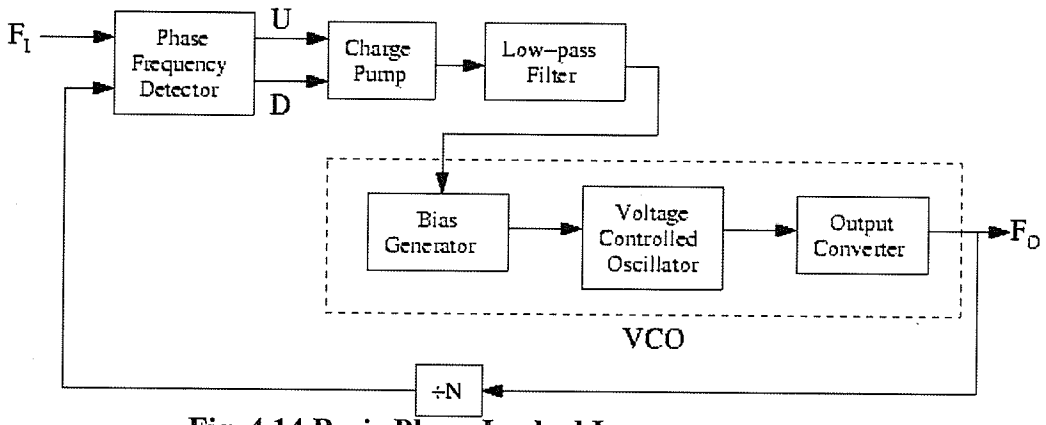


Fig. 4.14 Basic Phase Locked Loop

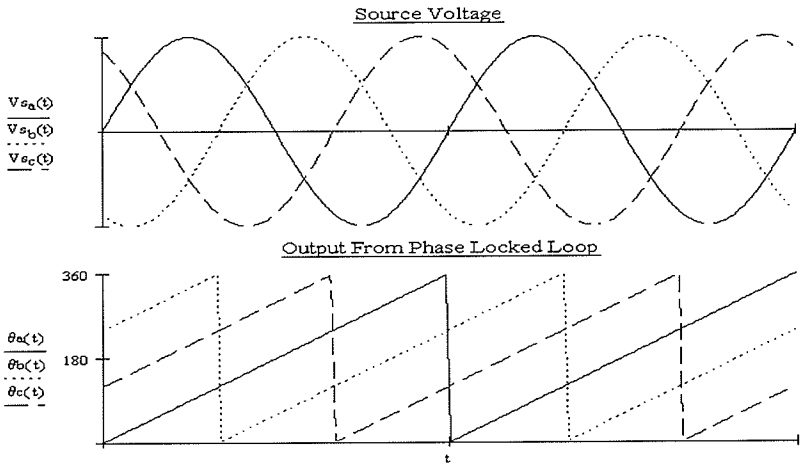


Figure: 4.15: Output Signals from Phase Locked Loop

4.10 Method of Pre-Charging The Inverter

An economic and convenient approach is to use the ac system to start-up the system directly because the reverse- conducting diodes of the IGBT in the H-bridge inverter, form an ideal single phase full wave rectifier. If the inverter is connected to the ac system while the IGBT are blocked, the dc capacitor of the inverter will be charged by the ac system voltage through the reverse-conducting diodes of the IGBT, thereby the constant dc capacitor voltage can be established. However, there may be overcurrent problems caused by the charging current of the dc capacitor or overcharging of the capacitors because of the leakage reactance of the transformer. To avoid these problems, a pre-insertion resistor is used in commercial pre-charging circuits. However, as shown in section 4.7.4 the proposed in this circuit uses an additional feedback loop which adjusts the dc capacitor voltage to the reference value. Hence the pre-insertion resistor is not needed.

CHAPTER 5
Sag Mitigation Simulation Results

5.1 Introduction

In Chapter 4, three methods were presented to control DVR, the minimum injection method, the no real power injection method and the proposed minimum active injected power method. This Chapter investigates the applicability of the three methods and validates the effectiveness of the control strategies and the analytical results using an electromagnetic transient simulator. The simulations were carried out using the PSCAD/EMTDC program.

5.2 Test System

The system schematic diagram shown in Fig.5.1 is used as the test system. The test system is a typical distribution system rated at 13.8 kV with a load approximately 15 MVA, power factor of 0.61, comprising of an infinite power source of 115 KV, a step down transformer has a secondary of 13.8 KV with leakage inductance, an inductance and

resistance representing the transmission line and resistive / inductive load. The system parameters are given in Table 5.1. The dc capacitor size was selected by simulation using the design criteria described in section 4.2.1. The filter parameter was selected using the design criteria described in section 4.2.1. The controls were optimized by simulation and gave stable performance for all tested cases. The capacitors on the dc link of the 7-level cascade inverter were precharged to a voltage of 5 kV each and then maintained to that level.

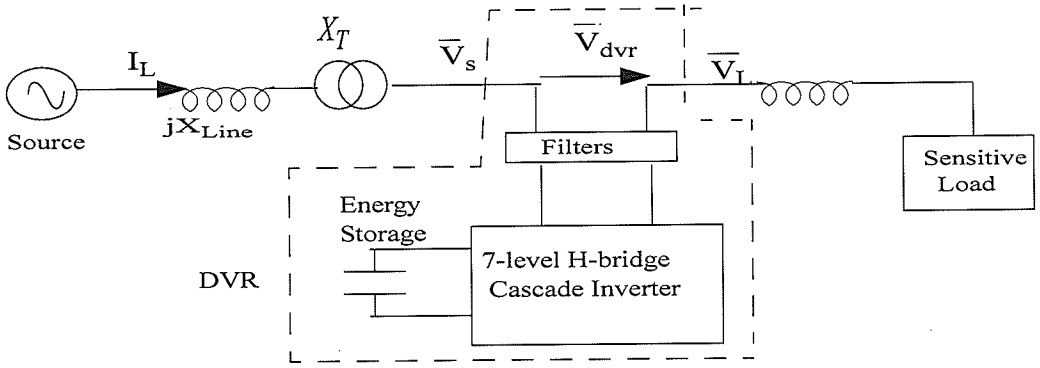


Fig. 5.1: Schematic diagram of the simulation test system

Table 5.1. Main test system parameters

Item	Values
Line voltage	13.8 kV /50 Hz
Line inductance X_{Line}	0.5 ohm
Filter inductor L_f	2 mH
Filter capacitor C_f	15 μF
Load inductance L_l	41 mH
Load resistor R_l	20 ohm
Transformer	115/13.8 KV
DC link capacitor	2000 μF

Table 5.1. Main test system parameters

Item	Values
Switching frequency	1950 Hz
Load power factor	0.61
Filter cut-off frequency	920Hz

5.3 Results of Simulations:

The proposed control system for the DVR is validated in this section via electro-magnetic transients simulation using the PSCAD/EMTDC simulation program. Results are first shown for the in-phase injection method and compared with those for the new proposed minimum real power injection method. The waveforms are shown for a system with a 1 pu load (at rated voltage) and a somewhat poor power factor of 0.6. A 40% voltage sag is applied for 5 and 8 cycle durations

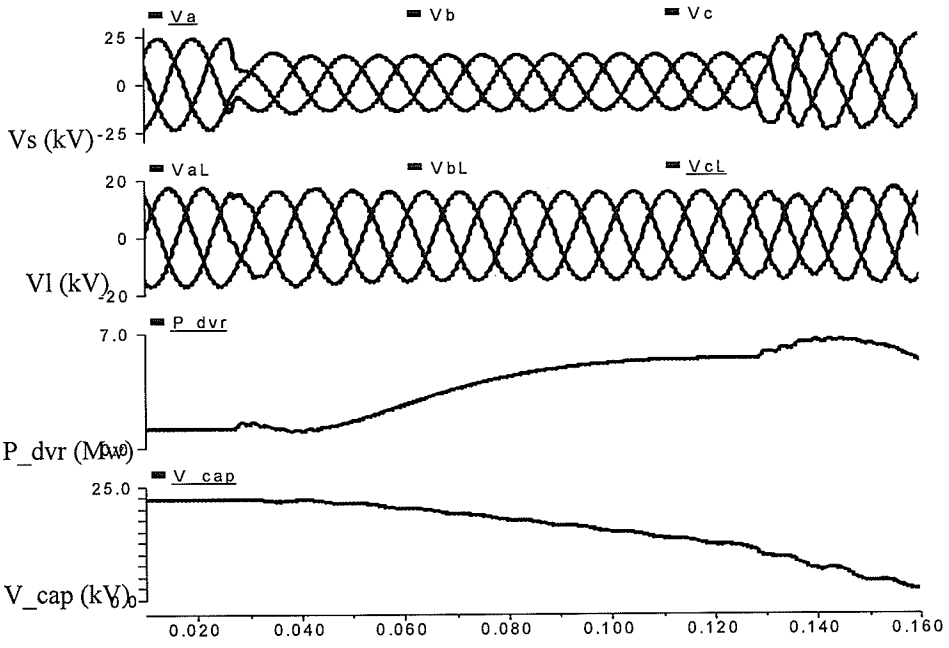


Fig. 5.2: Simulation results by using in-phase DVR

Fig. 5.2 shows the results for the in-phase injection method for compensating a relatively short 5-cycle sag. The first two sets of curves (Fig. 5.2 a and b) show the supply and load side voltages. It can clearly be seen that apart from a half cycle transient on sag application and removal, the load voltage is maintained at 1 pu during the sag. However, since the in-phase method requires real power injection as seen from Fig 5.2d, there is a discharge of the dc capacitor voltage (Fig 5.2c).

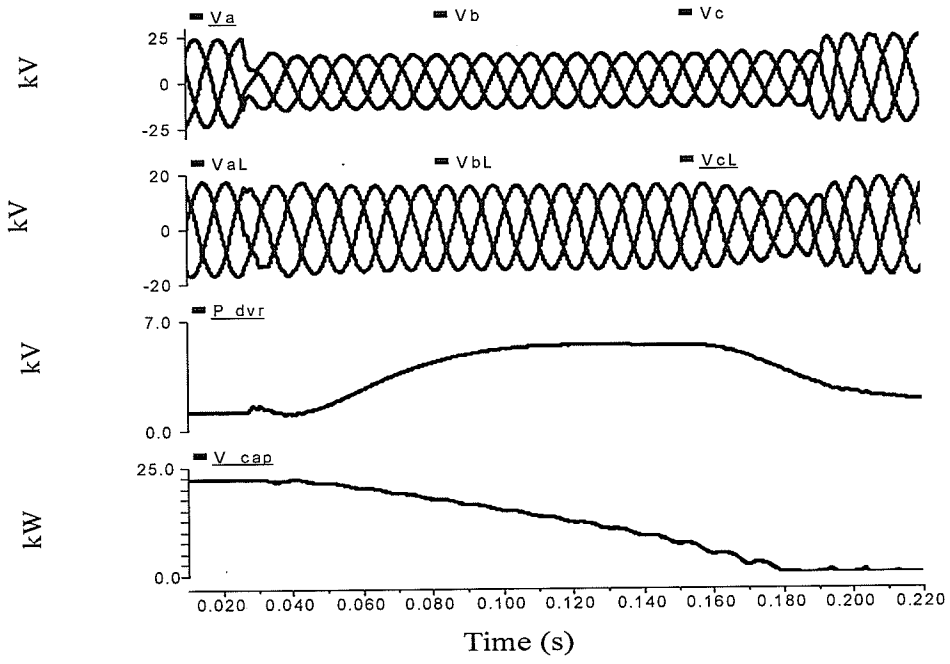


Fig. 5.3: Simulation results by using in-phase DVR for long duration sag

Note that if the sag duration were longer, the capacitor would discharge completely, thereby limiting the ability of the DVR to control the sag. Fig 5.3 shows sag compensation waveforms for of a longer duration (8-cycle) sag with the in-phase injection method. The DVR does a reasonable job of voltage control for the first 6 cycles, but subsequently loses control when the dc side capacitor discharges further.

Fig. 5.4 shows the waveforms for compensating the 5-cycle sag with the proposed minimum power injection method. As can be seen, the sag compensation is achieved with the injection of much reduced real power in comparison with the case in Fig. 5.2. The capacitor voltage is thus essentially constant.

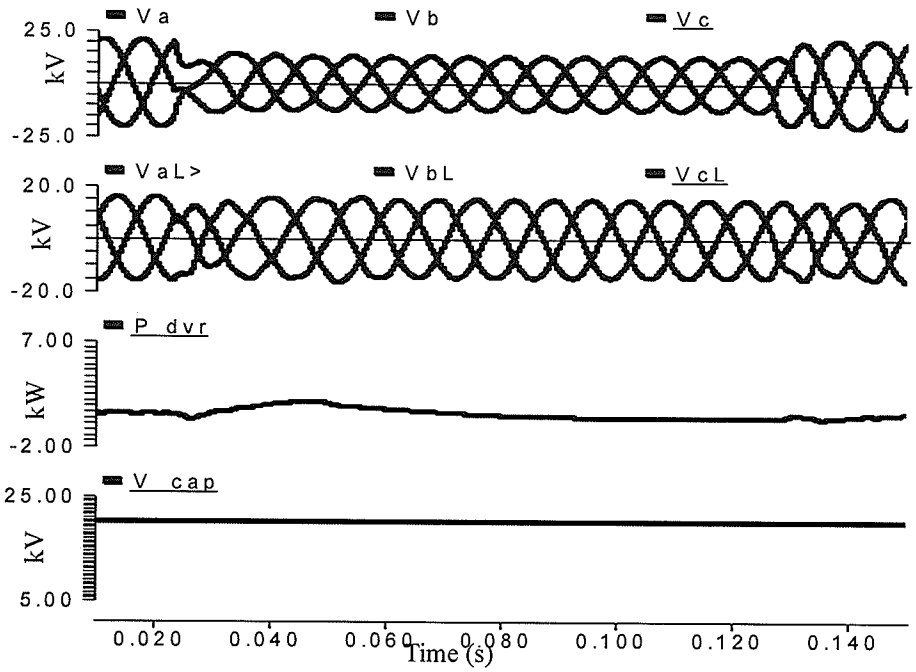


Fig 5.4: Sag Correction by Minimum Power Injection for a 5 cycle sag

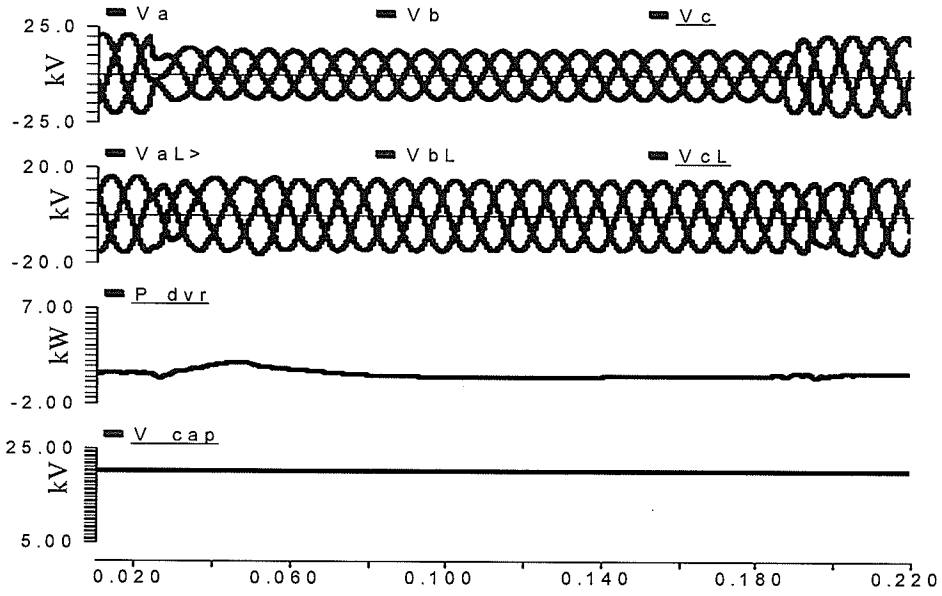


Fig 5.5: Sag Correction by Minimum Power Injection for a 8 cycle sag

Similarly, as seen from Fig. 5.5, the proposed method is superior to the in-phase method (see Fig. 5.3) also for the longer duration (8-cycle) sag, as it effectively regulates the voltage over the entire sag duration. It should be noted that in order to avoid sudden disturbance to the system, the change of injection angle (α) from in-phase to the proposed minimum real power injection angle is conducted over a 1-cycle period which gives marginal non-zero real power injections at the onset and removal of the sag (Figs 5.4and 5.5 c).

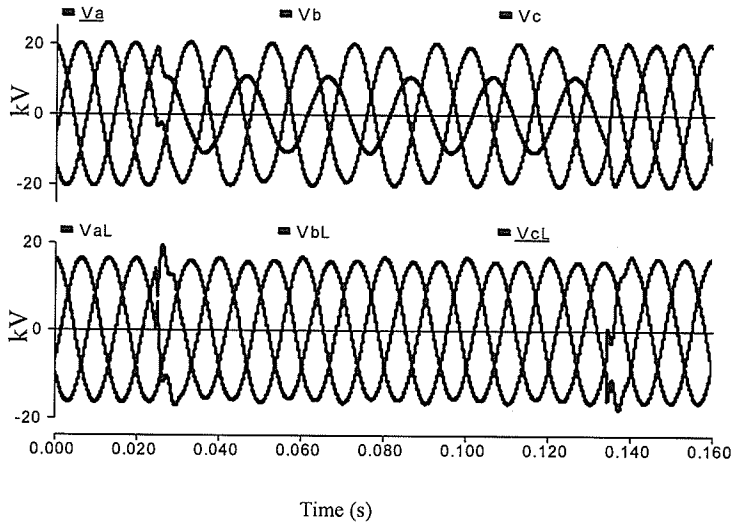


Fig 5.6: unbalance Sag Correction by Minimum Power Injection

Due to the decoupled topology of the cascade inverter, compensation for single phase sags (which are in fact more common than three phase sags) is readily achieved. Fig 5.6 shows source and load side voltage waveforms for a single phase sag caused by a resistive line-ground fault at the source.

The simulation results confirm the efficiency of the proposed mitigation controller and configuration for balance and unbalance voltage sag.

5.4 Effect of Filter

All the cases discussed so far use a filter. The question may be asked as to whether this filter modifies the dynamic response in a significant manner. The following section shows that the filter has a minimum effect on the DVR dynamic response. Fig. 5.5 & Fig. 5.6 demonstrated the effect of the filter on the quality of the DVR output voltage. Fig. 5.6 shows DVR output line-to-line voltage waveform with the filter and its harmonic spec-

trum, where Fig. 5.7 shows DVR output line-to-line voltage waveform without the filter and its harmonic spectrum.

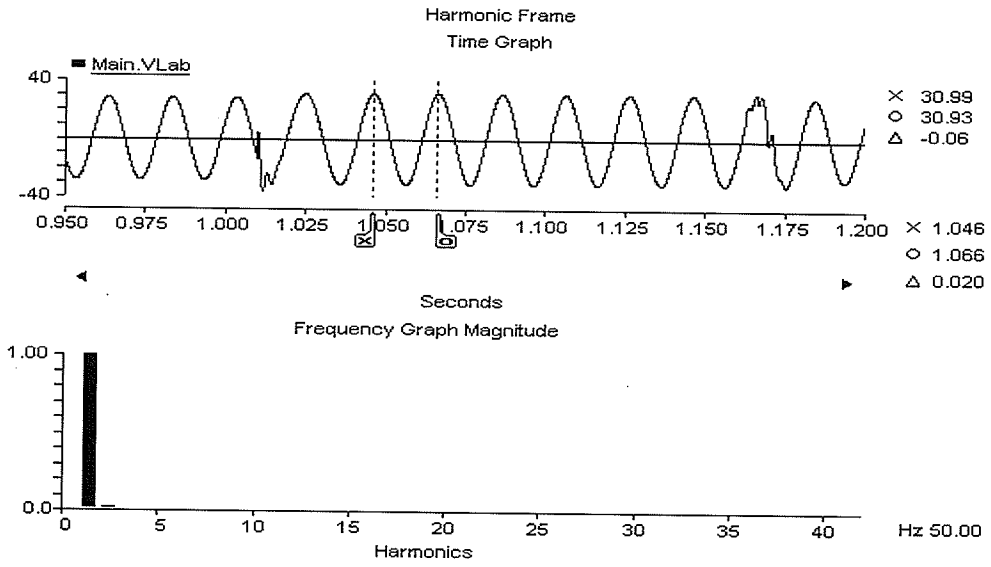


Fig. 5.7: DVR output line-to-line voltage waveform after the filter & its harmonic spectrum

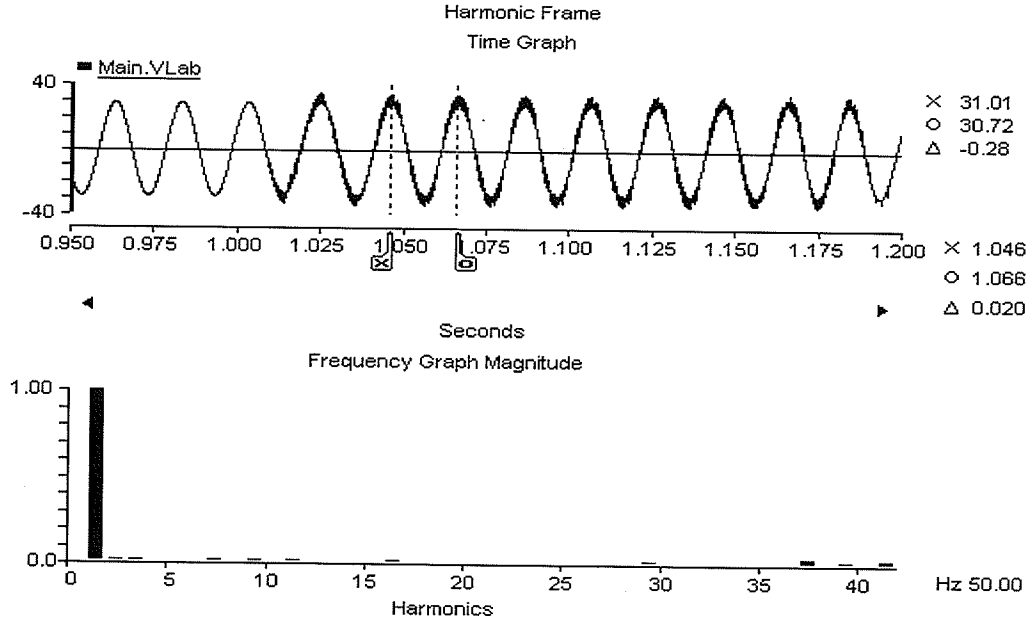


Fig. 5.8: DVR output line-to-line voltage waveform before the filter & its harmonic spectrum

5.5 Voltage Stability

As the proposed DVR topology is transformer-free, it offers improved voltage stability performance. Fig. 5.9 shows two PV curves one for a conventional converter based DVR configuration with a series transformer with leakage impedance of 15% and the other for the proposed configuration. The vertex of the parabola, which determines the maximum power that can be transmitted, is increased from 2.1 pu to 2.8 pu. with the proposed topology.

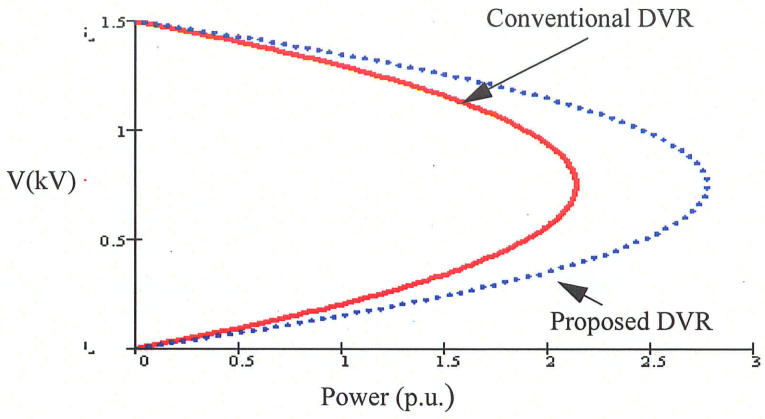


Fig. 5.9: PV curves for system with typical DVR configuration and proposed configuration

5.6 Capacitor voltage Control

Fig 5.10 shows sag compensation waveforms for of a (8-cycle) sag with the in-phase injection method. The sag mitigation is achieved for the first few cycles by injecting real power, but subsequently the DVR loses control when the dc side capacitor discharges. Fig. 5.10c shows the capacitor voltage during the sag and that after the sag was cleared. The

Fig. also verifies the effectiveness of the control system described in section 4.7.4 for maintaining and recharging the capacitance during normal operation of the system.

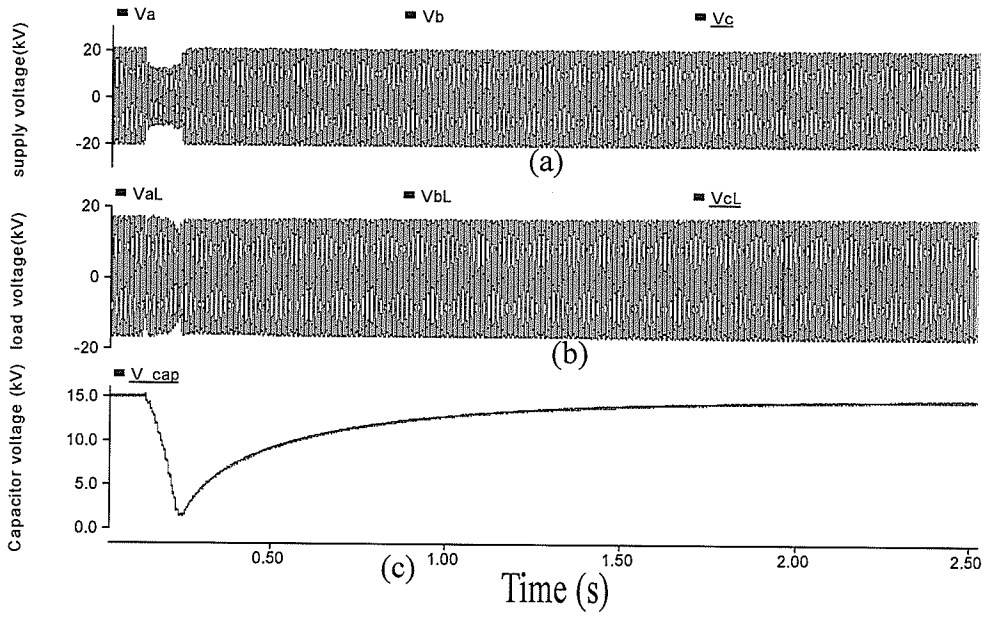


Fig.5.10: Charging of the capacitor voltage

CHAPTER 6

A New Configuration for a Cascade Inverter Based DVR with Reduced Energy Storage Requirements

---

6.1 Introduction

Earlier analysis and results in Chapter 4 and Chapter 5 have shown that with the appropriate control system, the device can mitigate longer duration sags as the size (energy storage capacity) of the capacitors is increased. It is also known that the sag mitigation is achievable with less energy storage for a system with poorer power factor. The proposed DVR exploits the above property by purposely decreasing power factor during a sag. This chapter introduces a new configuration for a Cascade (H-bridge) Inverter Based Dynamic Voltage regulator, in which the proposed cascade inverter topology as shown in Chapter 4 is modified by adding a shunt thyristor switched inductor. The proposed topology is shown to possess the ability of mitigating severe and long duration voltage sag with a significantly smaller energy storage requirement in the dc side capacitors. A suitable control system is designed, and the operation of the new device analyzed using electromagnetic transients simulation as well as mathematical analysis.

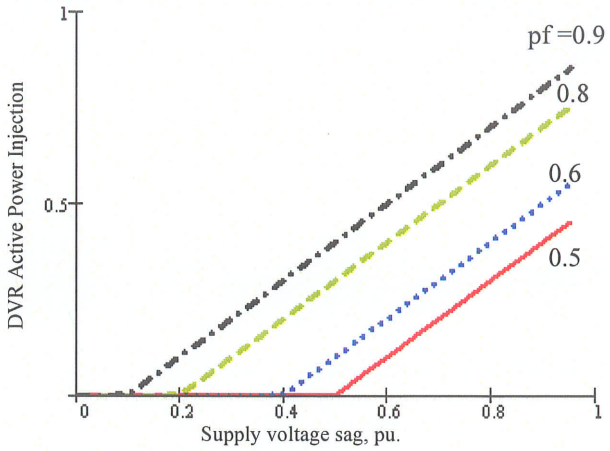


Fig. 6.1: Injected DVR active power verses the voltage sag for four different power factors

6.2 The New Proposed DVR Circuit Configuration

Earlier research presented in Chapter 4 has shown that if the sag (ΔV_{sag}) is small enough as required by (6.1), the desired voltage correction can be achieved without injecting any active power into the system. It can be seen also that (6.1) is a function of the voltage sag as well as the load power factor

$$\Delta V_{sag} \leq (1 - \cos\phi) \tag{6.1}$$

A sag larger than that indicated by (6.1) will require real power injection. In that case earlier research in Chapter 4 has shown that sag mitigation can be achieved with using minimum active power injection. The required injected voltage angle and magnitude are given in (6.2) and (6.3).

$$\alpha = \tan^{-1}\left(\frac{V_s \sin\phi}{V_l - V_s \cos\phi}\right) \tag{6.2}$$

$$\left|V_{dvr}\right| = \sqrt{V_l^2 - 2V_l V_s \cos\phi + V_s^2} \tag{6.3}$$

For the proposed strategy, Fig.6.1 shows the required DVR injected active power is plotted against the voltage sag of the supply-side voltage. Four different load power factors (0.5 pu, 0.6 pu, 0.8 pu and 0.9 pu) are considered in the plots.

As shown in (6.1) and Fig 6.1, it is clear that the compensation can be done with smaller energy storage and with smaller injected real power for loads of poorer power factor. This suggests a strategy could be developed where the power factor is deliberately reduced to achieve compensation with purely reactive power. As most industrial loads are lagging power factor loads, the strategy would require placing shunt inductance at the load. However, purposely reducing the load's power factor is contrary to proper distribution system practice, hence this reduction of power factor should only be carried out when the DVR is compensating severe sags.

The proposed approach to achieve this objective is shown schematically in Fig. 6.2. It can be seen that the proposed configuration differs from a typical DVR in the following manner:

- The H-bridge inverter topology is employed because of the advantages discussed earlier in Chapter 3 & 4.
- A thyristor switch can be turned on to add an inductance (X_p) in shunt with the load to lower the power factor seen from the system side. Note that the thyristor switch is off during normal operation, thereby maintaining normal (better) power factor during normal operation.

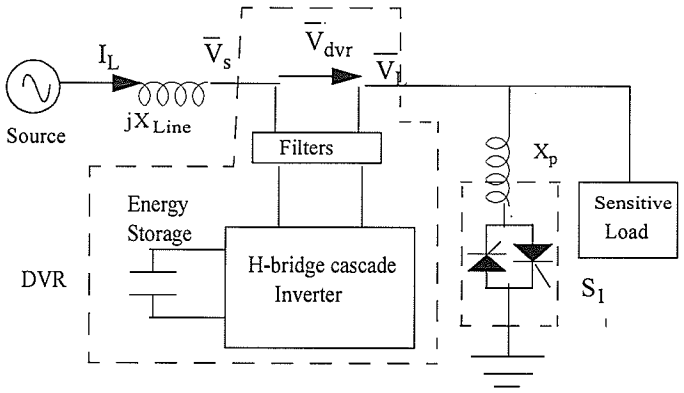


Fig. 6.2: Schematic Diagram of Proposed New DVR

6.2.1 Voltage Sag Correction by Proposed DVR

It can be also observed from Fig. 6.1 that for a system with poor power factor the DVR can handle larger sags without injection of active power to the system. The proposed DVR topology is built on the above observations. During the sag period the shunt inductance is switched into the circuit and lowers the power factor as seen by the source side. Considering the inductor-load shunt circuit as the "new" load, the net power factor angle is:

$$\phi_{new} = \text{atan}\left(\frac{X_p\left(R_l^2 + X_l(X_l + X_p)\right)}{R_l \times X_p^2}\right) \tag{6.4}$$

Where X_l, X_p and R_l are the load inductance, the shunt inductance and the load resistance, respectively. Assuming sufficient DVR rating, the maximum compensatable sag with pure reactive power injection is:

$$\Delta V_{sag} \leq (1 - \cos\phi_{new}) \tag{6.5}$$

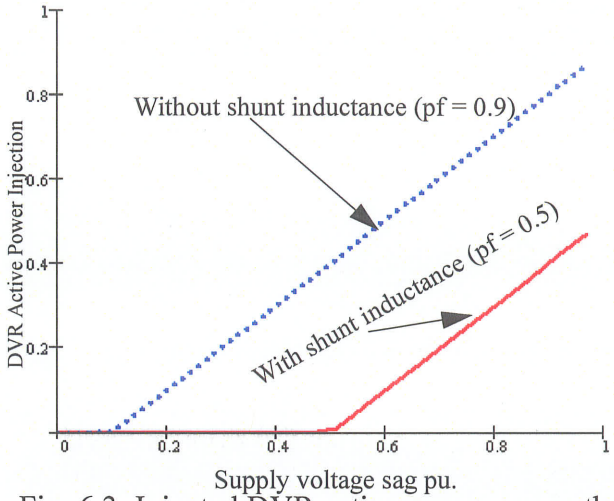


Fig. 6.3: Injected DVR active power verses the voltage sag for system without shunt inductance and with shunt inductance

Note this new approach mitigates larger sags without energy injection, but in addition, those sags which require energy injection can be compensated over a longer duration. In Fig. 6.3 the required DVR injected active power is plotted against the voltage sag of the supply-side voltage (with V_{dvrmax} = 1.0 pu) for two cases, first for a system with 0.9 power without the shunt inductance and the second with the same system but with proposed shunt inductance to lowers the power factor to 0.5, where the considerable power savings from the proposed approach are clearly evident.

For pure resistive load (1.0 load power factor) case which is the worst case to mitigate, (6.4) can be written as

$$\phi_{new} = \operatorname{atan}\frac{R_l}{X_p} \tag{6.6}$$

From (6.6) it is evident that the new load power factor depends on the ratio of the load resistance to the shunt indactance.

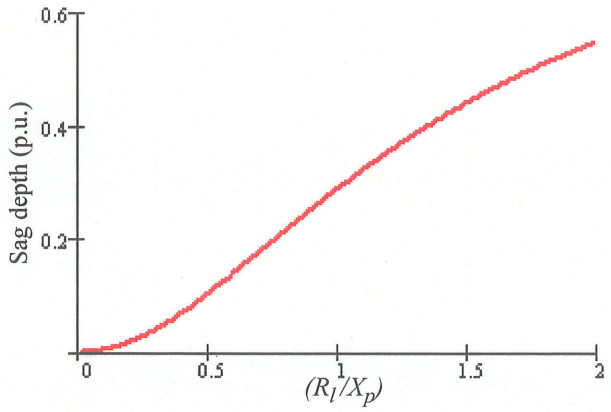


Fig. 6.4 Shows the sag depth which can be mitigated without injecting real power for different (R_l/X_p) ratio

Fig. 6.4 shows the sag depth which can be mitigated without injecting real power for different R_l/X_p ratio. From Fig. 6.4 it is clear that as R_l/X_p ratio goes higher a more severe sag can be mitigated without injection of real power.

The energy stored by the capacitor could be calculated from $E = \frac{C \cdot V_{dc}^2}{2}$ J, where C is the value of the dc side inverter capacitance and V_{dc} is the voltage developed across it. The power delivered by it could be approximately calculated as the maximum energy stored divided by the total time required for complete discharge while compensating a sag. Therefore, if real power is needed to mitigate a sag then the ability of the DVR to mitigate it depends on the sag level, duration and the size of the capacitor for given DVR voltage rating.

6.3 Control Method

The control system for the new configuration is easily adapted from the control system for the earlier proposed DVR in Chapter 4 (see Fig. 4.12). The main aspects of the control system are shown in Fig. 6.5 and include the following blocks: synchronization and voltage measurement, sag detection, injected voltage phase angle calculation, dc-link control voltage and firing pulse generation. These blocks are as discussed in Chapter 4. The essential different from the earlier control is the additional step of switching on and off the shunt inductance.

6.3.1 Sag detection

The sag is calculated by comparing the long term steady state value (in *d, q* components) of the supply voltage with the instantaneous voltage (*d, q* components). This allows for detection of symmetrical and nonsymetrical sags, as well as the associated phase jump. In order to prevent undue control action, the undervoltage is only considered to be sag if it exceeds a certain threshold as in (6.9).

$$\left|\bar{u}_{sag,dq}\right| > (u_{threshold}) = 0.05pu \tag{6.7}$$

where

$$\left|\bar{u}_{sag,dq}\right| = \sqrt{(u_{ref,d} - u_{s,d})^2 + (u_{ref,q} - u_{s,q})^2} \tag{6.8}$$

in which u_{refd} *and* u_{refq} are the reference values for the d and q voltages. If sag is detected S2 open and S3 and S1 are closed. The system will have a new load power factor as expressed on (6.4) as result of the shunt inductance being part of the system.

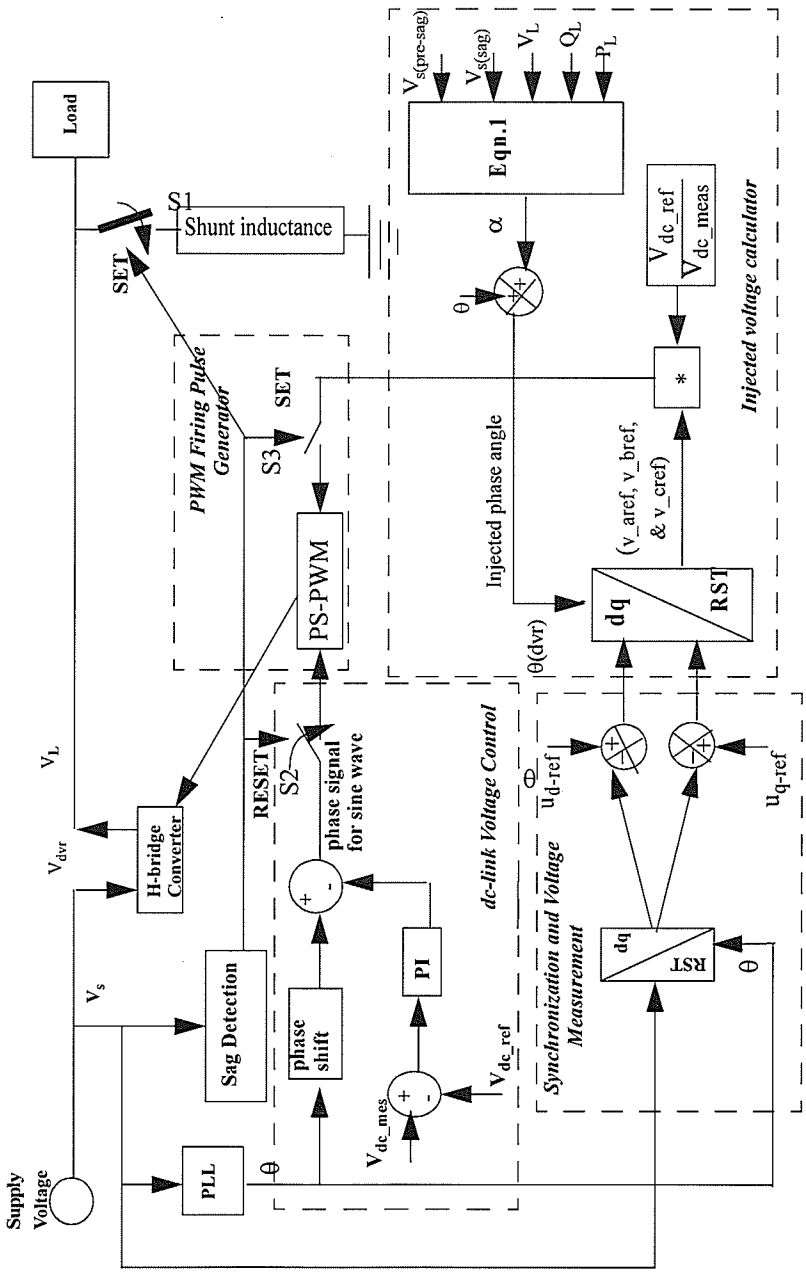


Fig. 6.5 Control structure of the proposed DVR with rotating dq-reference frame

6.4 Simulation Results

The proposed control system for the DVR is validated in this section via electromagnetic transients simulation using the PSCAD/EMTDC Simulation program. The test system is a typical distribution system rated at 13.8 kV with a load approximately 32 MVA, power factor of 0.98, comprising of an infinite power source of 115 KV, a step down transformer has a secondary of 13.8 KV with leakage inductance, an inductance and resistance representing the transmission line and resistive / inductive load. The system parameters are given in Table 6.1.

Table 6.1. Main test system parameters

Item	Values
Line voltage	13.8 KV /50 Hz
Line inductance X_{Line}	0.5 ohm
Filter inductor L_f	2 mH
Filter capacitor C_f	15 μF
Load inductance L_l	.001 mH
Load resistor R_l	10 ohm
Transformer	115/13.8 KV
DC link capacitor	2000 μF
Switching frequency	1950 Hz
Load power factor	0.98

Results are first shown for minimum real power injection method without connecting the shunt inductance to the system and compared with those for the new proposed DVR configuration. A 40% voltage sag is applied. Figure 6.6 shows the results for without connecting the shunt inductance to the system method. The first two sets of curves (Fig. 6.6 a and b) show the supply and load side voltages and it can clearly be seen that apart from a tran-

sient on sag application and removal, the load voltage is maintained at 1 pu during first 5 sag cycles. However, since without connecting the shunt inductance to the system can result in real power injection as seen from Fig 6.6d, there is a discharge of the dc capacitor voltage to zero after 5 cycles as seen in Fig 6.6e. Note that for sag duration longer than 5 cycles, the capacitor would discharge completely, thereby revoking the ability of the DVR

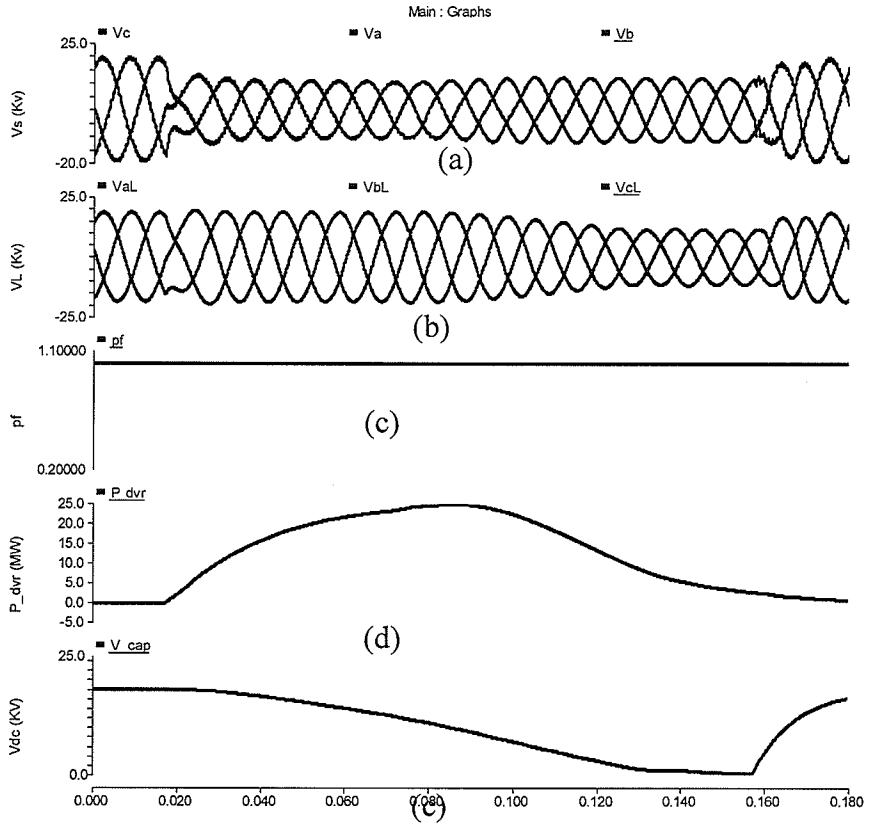


Fig. 6.6: Simulation results without shunt inductance in the circuit for 40% 7 cycles sag

to control the sag as shown in Fig. 6.6. Figures 6.7 and 6.8 show the corresponding curves for the proposed DVR configuration with connecting the shunt inductance to the system (R_l/X_p =0.8) with new load power factor 0.78. The load power factor is measured as ($pf = \cos(\text{atan}\, Q_l/P_l)$), and hence relies on measurements of P_l and Q_l. The Q_l meter used measures the three phase reactive power in the steady state, but has its own transient response. Consequently the load power factor curve shown in Figures 6.7c and 6.8c is only valid when it reaches the steady state. As can be seen form Fig. 6.7, the sag compensation of 7 cycles is achieved with the injection of reduced real power and the capacitor voltage is slowly discharged, suggesting that this method would be suitable even for long duration sags. Fig 6.8 shows what happens if the sag duration is increased to 14 cycles. As can be seen, approximately 100% sag compensation is achieved for the first 12 cycles. Then due to capacitor discharge, the compensation ability is compromised and only 85% sag compensation is achieved. Fig. 6.9 shows the corresponding curves for the proposed new DVR configuration with connecting the shunt inductance to the system (R_l/X_p =1.3) with new load power factor 0.6. As can be seen form Fig. 6.9, the sag compensation of 7 cycles is achieved with the injection of much reduced real power and the capacitor voltage is approximately constant, indicating that this method is suitable for sags of even long duration. Fig. 6.10 shows, that the proposed DVR configuration injection method can effectively regulate the voltage over the entire sag duration (14 cycles) or more without injecting any real power.

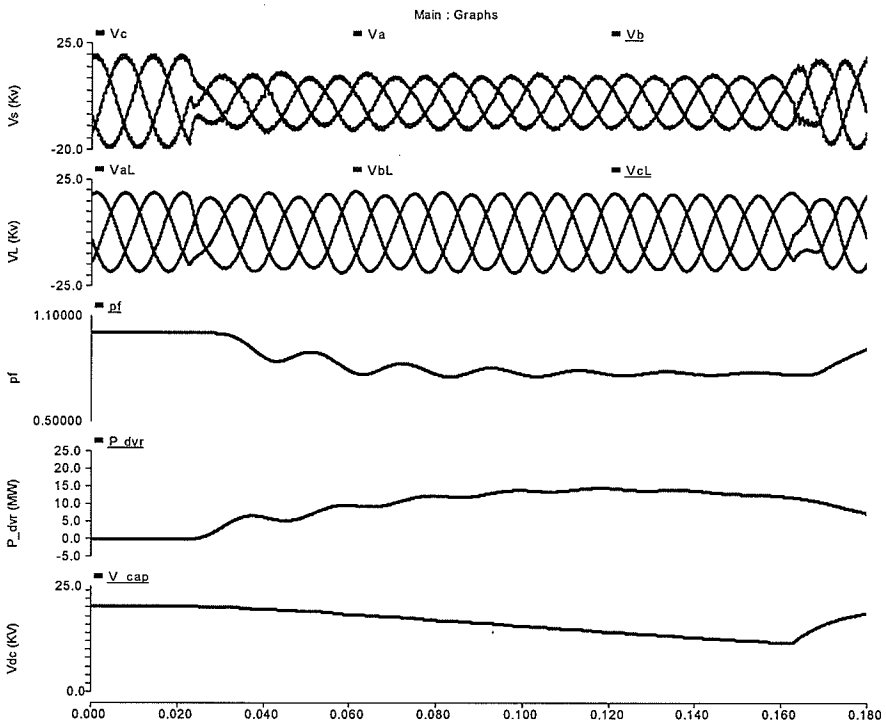


Fig. 6.7: Simulation results for the proposed DVR configuration for 40% 7 cycle sag correction with (R_l/X_p =0.8)

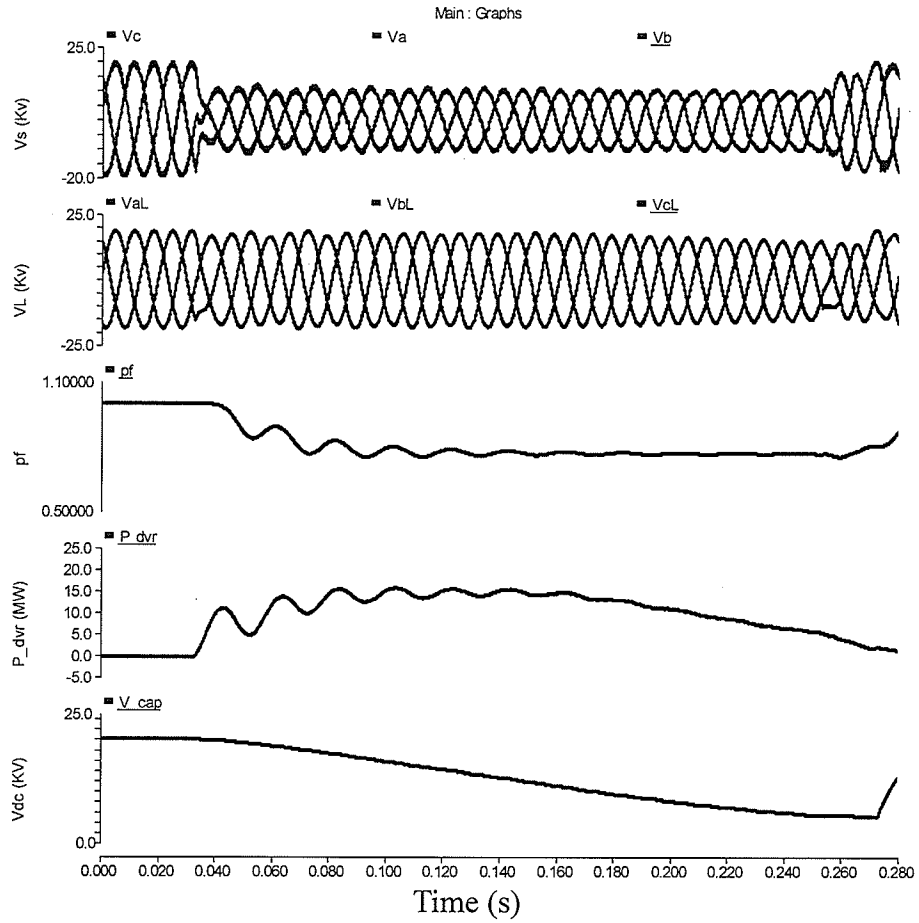


Fig. 6.8: Simulation results for the proposed DVR configuration for 40% 14 cycles sag correction with (R_l/X_p =0.8)

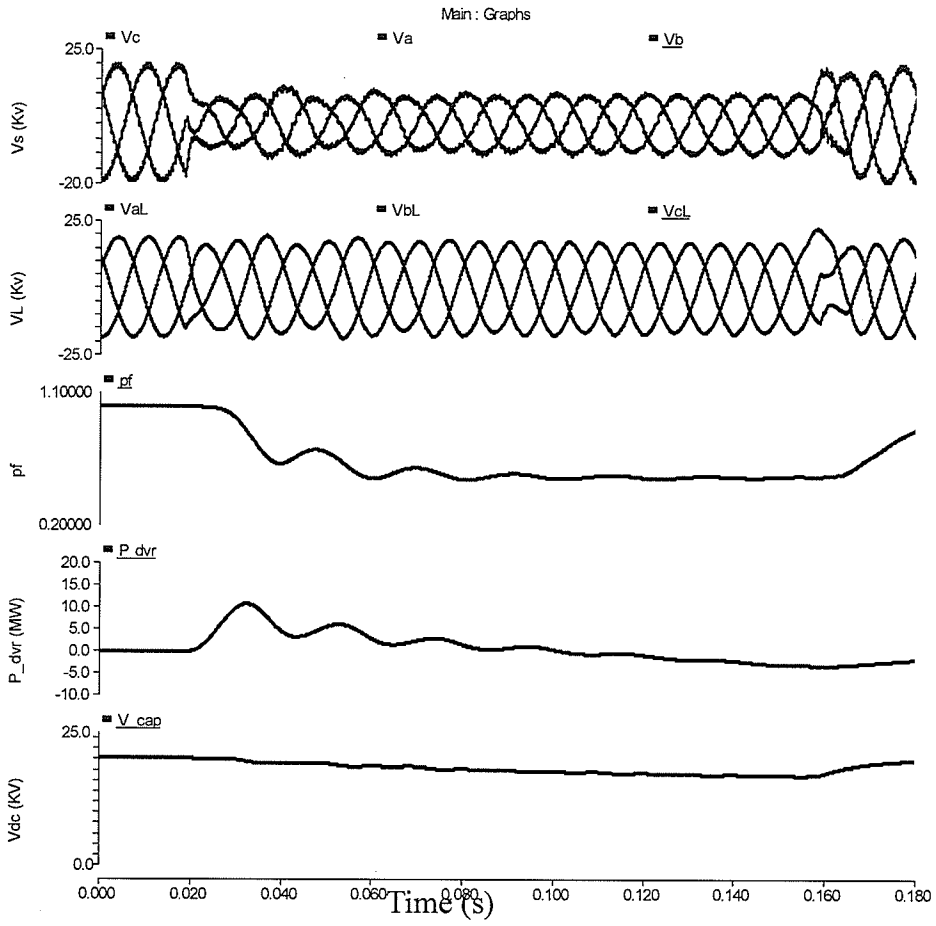


Fig. 6.9: Simulation results for the proposed DVR configuration for 40% 7 cycle sag correction with (R_l/X_p =1.3)

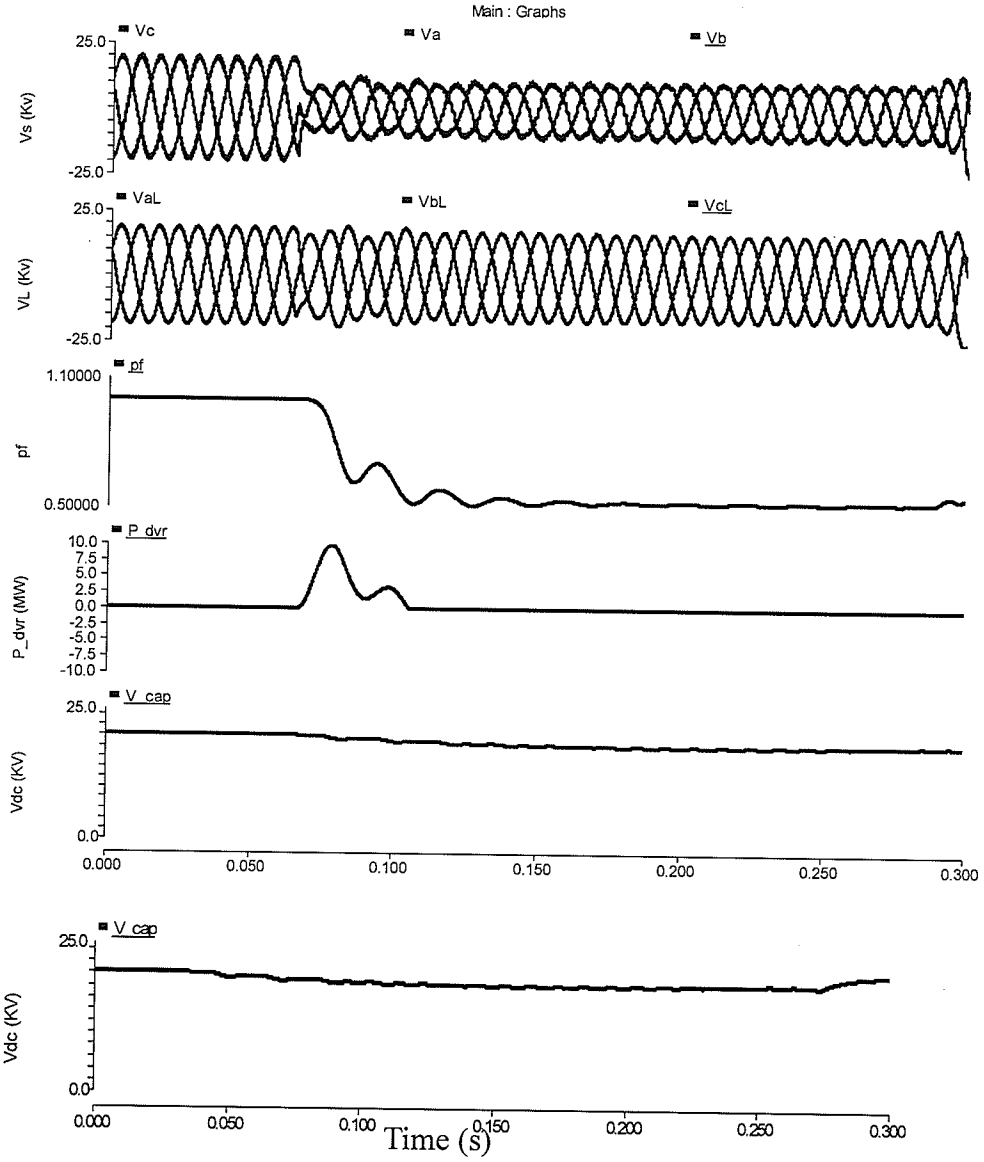


Fig. 6.10: Simulation results for the proposed DVR configuration for 40% 14 cycles sag correction with (R_l/X_p = 1.3)

6.5 Summary

A modification was introduced to the basic cascade inverter topology and the corresponding control system where the capacitor energy storage can be even further reduced by active modulation of the power factor during a sag by adding a thyristor switched

inductor in shunt with H-bridge converter. It is evident from the above simulation results that the proposed DVR configuration has the ability to mitigate severe and long duration voltage sags with comparatively small energy storage capacitors.

CHAPTER 7

Harmonic Compensation

7.1 Introduction

This chapter discusses the adaptation of the DVR proposed in the thesis to provide the auxiliary function of voltage harmonic compensation. The advantage of the proposed DVR topology with the resonant harmonics extraction in comparison with the conventional DVR configuration is demonstrated. In recent decades the growing and widespread use of electronic equipment by different segments of society is perceptible. This equipment presents itself as non-linear impedances to its supplying electrical systems and generates harmonic currents with well-known adverse effects, such as excessive heat which effects the life of equipment, electromagnetic interference, voltage distortions, etc. These disturbances have required researchers and power electronics engineers to present solutions to minimize or eliminate them [27]. Therefore, the quality of the electrical system, nowadays, is an important matter and, within this context, voltage distortion is the focus of this chapter.

Passive filters have traditionally been used to absorb harmonics generated by large industrial loads, because of their relatively low cost and high efficiency. However, they have several drawbacks. The supply impedance strongly influences the compensation characteristics of passive filters, and they are highly susceptible to undesirable series and parallel resonances with the supply and load. Because the incidence of harmonic-related problems in utility and industrial power systems is increasing, active power filters have attracted great attention and have been expected to be an effective remedy. Generally, an active filter has been considered to be a current source connected in parallel with the load (harmonic source) as shown in Fig. 7.1. The approach is based on the principle of injecting harmonic current into the ac system, of the same amplitude and reverse phase to that of the load current harmonic, so that the harmonic current in the source is cancelled.

7.2 Application considerations of parallel active filters

A parallel active filter as shown in Fig. 7.1, is considered to be a current source connected in parallel with the load. The approach is based on the principle of injecting harmonic current into the ac system, of the same amplitude and reverse phase to that of the load current harmonic, so that the harmonic current in the source is cancelled. This section discusses the characteristics and application considerations of parallel active filters [27, 32-33] when they are applied to nonlinear loads that are voltage-source type of harmonic source ("harmonic voltage source"), such as diode rectifiers with direct smoothing dc capacitors for ac drives, etc. Today more and more diode rectifiers with smoothing dc capacitors are used in electronic equipment, household appliances, and ac drives. Harmonics generated by these loads have become a major issue. Naturally, attempts have been

made to use parallel active filters for harmonic compensation of these diode rectifiers. However, it has been found in the field that the parallel active filter is not only unable to cancel the harmonics completely but it also causes problems, such as enlarging the dc voltage ripple and ac peak current of the rectifier. This is because a diode rectifier with smoothing dc capacitors behaves like a harmonic voltage source rather than as a harmonic current source. Another aspect is that there may be LC passive filters or power-factor correction capacitor banks connected on the load side (downstream) from the point where an active filter is connected. In this case, the equivalent circuit downstream seen from the connection point of the active filter would not be a current source even if the main loads are a harmonic current source. Care must be taken when an parallel active filter is connected across a load which already has a diode rectifier or a power system such that downstream contains passive filters and/or capacitor banks, the current injected by the active filter will flow into the diode rectifier or the load side that presents low impedance.

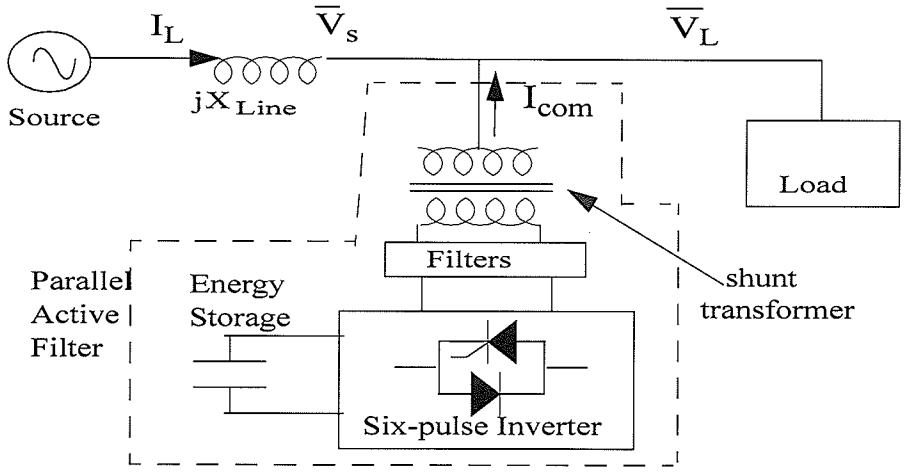


Fig.7.1 Schematic diagram of a parallel active filter

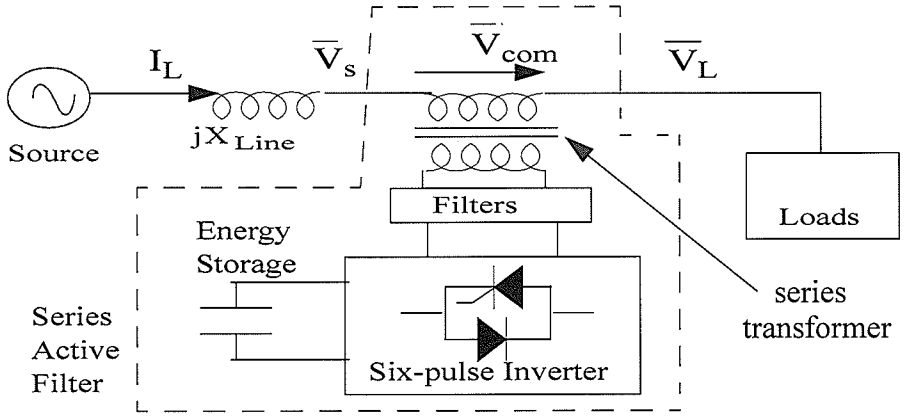


Fig.7.2 Schematic diagram of a series active filter

As a result, harmonics of the source current cannot be completely canceled. Moreover, harmonic current flowing into the diode rectifier or the system downstream increases greatly, and when added to the fundamental current can result in a current overload. A series active filter has been proposed to compensate for voltage-source type of harmonic source [29, 31].

7.3 Series Active Filters

A series active filter as shown in Fig. 7.2, is to be placed in series between the ac source and the load (or harmonic source) to force the source current to become sinusoidal. The approach is based on a principle of harmonic isolation by controlling output voltage of the series active filter. In other words, the series active filter presents a high impedance to harmonic current, therefore blocking harmonic current flow from the load to the ac source and from the ac source to the load side. This prevents supply-load interaction and resonance problems. Sometimes the series active filter is used to enhance the performance of the passive filter. This requires less rating from passive filter. Also, the harmonic isola-

tion feature reduces the need for precise tuning of the passive filters and allows their design to be insensitive to supply impedance and eliminates the possibility of filter overloading due to ambient voltage harmonics and/or ambient harmonic loads.

7.4 Comparison of Parallel Active Filters and Series Active filters

In the previous sections, compensation characteristics of parallel active filters and series active filters were introduced. Table 7.1 is a summary comparison of parallel and series active filters, when applied in different system configuration.

Table 7.1. Comparison of Parallel Active Filters and Series Active filters

System Configuration	Parallel Active Filter	Series Active Filter
Basic operating principle	Operates as a current source	Operates as a voltage source
Adaptive loads	Inductive or current-source loads or harmonic sources, e.g., phase-controlled thyristor rectifiers of dc drives	Capacitive or voltage-source loads or harmonic voltage sources e.g., diode rectifiers with direct smoothing capacitors for ac drives
Required operation conditions	Load impedance, Z_L, should be high	Load impedance, Z_L, should be low
Compensation characteristics	Excellent and independent of the source impedance, Z_s, for current-source loads, but depend on Z_s, when the load impedance, Z_L, is low	Excellent and independent of the source impedance, Z_s, and the load impedance, Z_L, for voltage-source loads, but depend on Z_L, when the loads are a current-source type
Application Considerations	Injected current flows into the load side and may cause overcurrent when applied to a capacitive or voltage-source load	A low impedance parallel branch (parallel passive filter or power factor improvement capacitor bank) is needed when applied to an inductive or current-source load

7.5 Harmonics Measurement Techniques

Measurements of harmonics require an algorithm for extracting the harmonic components form the total waveform. There are several extraction and estimation techniques: time domain techniques, frequency domain techniques and state (digital) estimation techniques as shown in Fig.7.3. All the techniques, cited in the chart shown in Fig. 7.3, give satisfactory results for harmonics extraction and estimation but present different levels of complexity in the implementation. Next in this section, two of the more popular extraction techniques will be thoroughly investigated to show not only their principles but also the conditions and constraints under which these techniques work efficiently. The resonant controller extraction technique is selected for harmonic extraction in this chapter to overcome some of drawbacks of these two techniques.

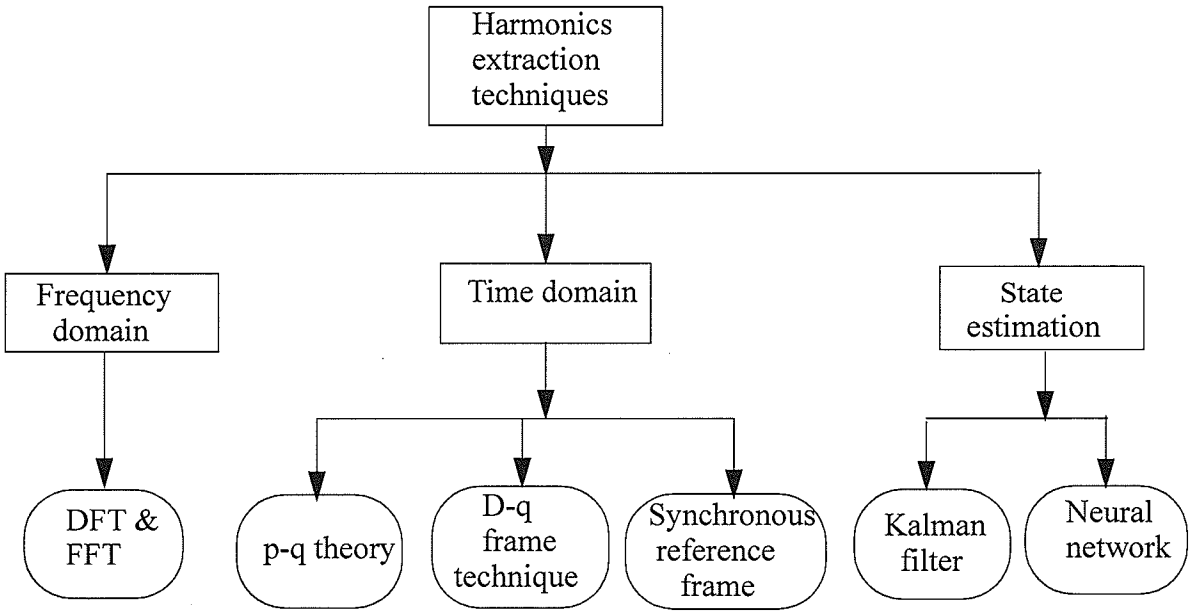


Fig.7.3 Harmonics extraction and estimation techniques

7.5.1 DFT and FFT

The Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT) are commonly used to extract harmonics. There are some basic assumptions for the application of each of these [36]. These assumptions are: (i) the sampling frequency is greater than twice the highest frequency in the signal to be analyzed and (ii) each frequency in the signal is an integer multiple of the fundamental frequency. The harmonics are extracted by the DFT according to the following formula:

$$F(k) = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} f(n) e^{-j2\pi k \frac{n}{N}} \quad (7.1)$$

For a sequence of N samples in *f(n)* indexed by *n= 0....,N-1, F(k)* is referred to as the set of "Fourier Coefficients" or "Harmonic". Although the DFT and FFT are still popular, they have the following disadvantages:

- Aliasing Effect: This phenomenon occurs at low sampling rates in which the high frequency components translate into low frequency ones. Consequently, the extracted magnitudes of the low frequency components are inaccurate.
- Picket-Fence Effect: This event occurs, if the analyzed waveform includes a frequency which is not an integer that is multiplied by the fundamental frequency. If this case exists, the extracted magnitude will not be accurate, especially for harmonic components lying close to the non-characteristic harmonics.
- A minimum of one fundamental cycle is required for the transformation process.

7.5.2 D-q Orthogonal Rotating Frame

The d-q orthogonal rotating frame technique is employed for harmonics extraction, and consequently, for harmonics mitigation, and has the advantage of simplicity. The d-q rotating technique transformed the three phase quantities (say V_a, V_b, V_c) into three quantities (V_d, V_q, V_o), which are constants when V_a, V_b, V_c are balanced and only contain fundamental frequency. (7.2) shows the transformation:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t - 4\pi/3) \\ \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t - 4\pi/3) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (7.2)$$

Table 7.2. D-q disturbance extraction table

Parameters in d-q coordinates	Physical meaning in the three-phase system
$\omega=0$ (DC components)	Positive phase sequence components
$\omega=2\omega_0$ (twice the fundamental frequency)	Negative phase sequence components
$\omega=\omega_0$ +/– 1 (and frequency > $2\omega_0$)	Harmonics components

In the d-q rotating frame, the voltage can be filtered to extract the fundamental and disturbance according to Table 7.2. This method has some problems that are associated with the use of passive filters and the Phase Looked Loop (PLL). In addition to the previous problems, the d-q technique does not have the capability to directly extract the individual components of the harmonics.

7.6 Proposed Harmonics Compensation Topology

Instead of adding extra harmonic cancellation hardware, the DVR proposed in thesis provides the opportunity for conducting the additional duty of steady state load voltage harmonics cancellation, with the benefit of further increasing the Power Quality with minimal increase in complexity. This is the principal focus of this chapter.

In the conventional DVR as shown in Fig. 1.1 there are some drawbacks in achieving this objective. The main drawback is the poorer controller performance resulting from the low values of modulation index that must be used for harmonic compensation. The low modulation index is required because the effort required to cancel the harmonics is an order of magnitude smaller than that required for the primary objective of sags compensation. Also, a conventional DVR uses a converter transformer whose leakage inductance further constrains the power flow.

The H-bridge DVR configuration proposed in this thesis and discussed in the earlier chapters is redrawn in Fig. 7.4. It presents a practical solution for the above mentioned limitations. Consider the case of a DVR with a maximum voltage injection ceiling of 50% of the supply voltage. In order to compensate for harmonics which have much lower magnitudes than the fundamental, the system must operate at very low modulation index values, typically around 5% (or less). However, it is difficult to achieve high accuracy in injected voltage phase and magnitude when the converter is operating at a small fraction of it is an available voltage level, as result of that DVR performance as harmonics compensation will be poor. On the other hand, the proposed DVR based cascade multilevel topology with several (say, n), H-bridge converters connected in series. During normal operation

with near-zero fundamental frequency injection, only one of these can be assigned the job of harmonic elimination. The modulation index required for the single H-bridge of the n-level system is (n-1)/2 times larger than that in a conventional topology which reduces the sensitivity and improves the performance of the harmonic compensation ability of the DVR. The other converters can be bypassed during such operation so as to limit the device losses to the minimum. In order to equalize the stresses and maintain an equal dc voltage across each H-bridge, the role of harmonic elimination can be rotated amongst all the converters.

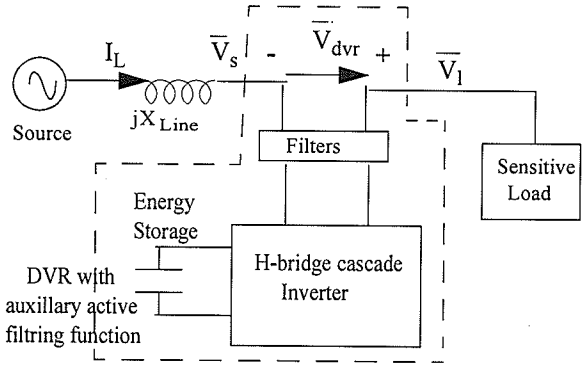


Fig. 7.4: Schematic diagram of a proposed DVR f or sags and harmonics mitigation

7.6.1 Proposed Selective Harmonic Compensation Control

It is possible to modify the reference signal to the PWM controller in Chapter 4 Fig. 4.12 to compensate for sag as well as harmonics. The modified controller is shown in Fig.7.5. The harmonic cancellation duty is required even during normal operation, when the sag is absent. In this situation, the nominal modulation index (ratio of peak modulation signal to peak of triangular wave) of the PWM controller is close to zero and the sensitivity of the circuit to harmonic cancellation signal is very high; making the compensation difficult. This also adds additional conduction and switching losses

as all IGBT switches are being fired merely to achieve harmonic compensation. The H-bridge topology (Fig.4. 3) provides the unique opportunity for only using one (or few) of the H-bridges to provide harmonic compensation, thereby reducing the sensitivity and also the losses. During normal operation, it is also possible to keep the other series converters bypassed to reduce switching and conduction losses.

A. Generation of Harmonic References

It is necessary that the harmonic compensation scheme has a net real power flow of zero (or close to zero) at all times. Otherwise, a net power flow out of inverter will deplete the available energy stored in the capacitors, and a net power flow into the inverter will increase the dc_link voltage past its ratings. To minimize the net real power flow, narrow-band resonant based controllers [37-42] are used to compensate for a number of selected harmonic. The output of these controllers is added to the sag compensation reference signal set of one (or a limited few) of the H-bridges to create a 'power quality' compensation signal set $\{v_{aref}, v_{bref}, v_{cref}\}$, which addresses both sag and harmonic mitigation requirements.

The controller includes a proportional gain and a resonant term. For the harmonic of order n, the controller transfer function is:

$$H_n(s) = K_n \omega_c \frac{s + \omega_c}{s^2 + 2\omega_c s + \omega_n^2 + \omega_c^2} \quad (7.3)$$

It has a resonant band-pass characteristic ω_n with a finite width that allows the controller to tolerate variations in the supply frequency. The band-pass tolerance is determined by

the value of ω_c. Fig. 7.5 shows an implementation with H_5 and H_7 used to target 5^{th} and 7_{th} harmonics.

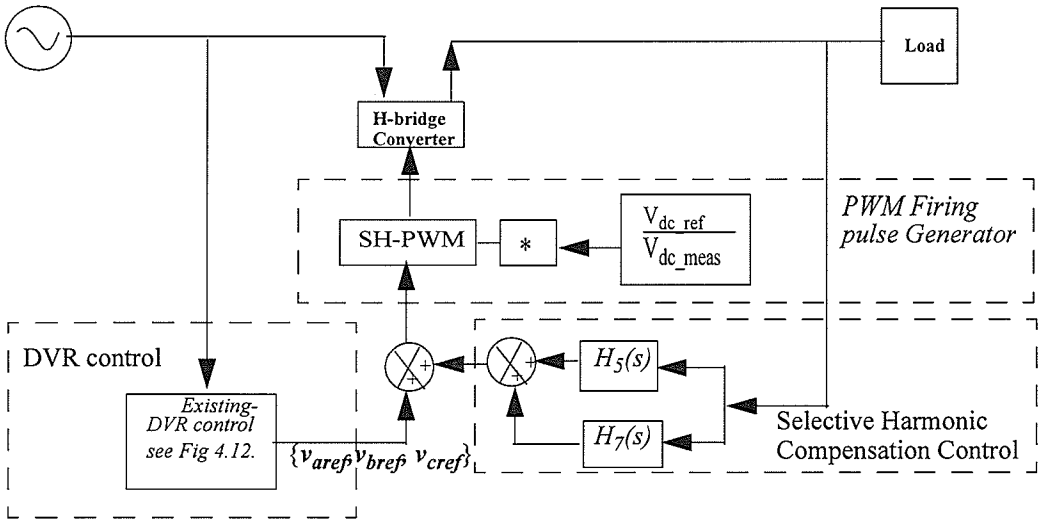


Fig. 7.5: Control structure of DVR with harmonic compensation

When digitally implemented the resonant controllers has significant computational advantages that are achieved when stacking multiple controllers and also due to their combined positive and negative sequence compensation [38]. A further advantage of using resonant controllers is that they are applied on each phase independently, with no cross coupling between phases, and will therefore work directly on single-phase systems. The scheme is less sensitive to noise. Dq based approaches are more computational intensive and are more sensitive to noise. They are also more difficult to implement on a 1-phase systems due to the poor dynamic performance of a single-phase comparator.

The full harmonic compensation feed-back controller to compensate the k targeted harmonics $\{n_1, n_2, \ldots n_k\}$ is therefore:

$$H_{total}(s) = \sum_{n \in N} H_n(s) \qquad N = \{n_1, n_2, \ldots n_k\} \tag{7.4}$$

In the example shown in this chapter, only the 5^{th} and 7^{th} harmonics were targeted, i.e. $N = \{5, 7\}$.

Fig. 7.6 shows the frequency response of the resonant controllers designed for compensating 5^{th} and 7^{th} harmonics with two different band-pass tolerance frequencies ω_c. The figure clearly shows high pass peaks at the targeted 5^{th} and 7^{th} harmonics and a high attenuation of fundamental frequency. Thus, any impact on the fundamental frequency DVR function is minimal. Also, the phase at the fundamental frequency is close to 90 degrees, thereby indicating that very little power is drawn from the dc capacitor. The choice of the band-pass tolerance frequencies ω_c is made with the following considerations. The frequency response for two different band-pass tolerance frequencies ω_c 0.5 Hz and 3.5Hz is shown in Fig. 7.6. A large a value of ω_c means, that the phase angle at the fundamental frequency is far from 90 degrees, and a small a value of ω_c means, the control will more sensitive to any variation on the supply frequency. For the above two reasons the f_c is selected to be equal to 1.5Hz.

Note that when sag compensation as well as harmonic filtering is required, the output signal from the harmonic compensation controllers are added to the sag compensation signal only for one converter. Effectively this means that the modulation waveforms shown in Fig. 7.5 are generated in two parts. The first part only gets the modulating compensation signal for

voltage sags as shown in Fig. 4.12. The second part contains the harmonic compensation signal which generated by the resonant controller. However, in case of sag free operation the modulating signal containing the harmonic compensation signal, which is compensated by the bridge that is doing harmonic compensation only.

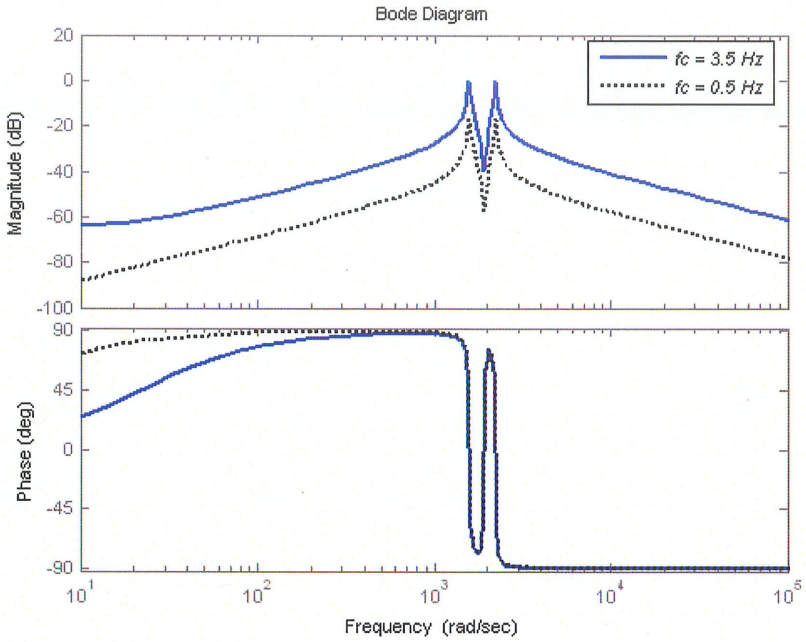


Fig. 7.6 Open loop frequency response of the voltage harmonic controllers

7.6.2 PWM Based Firing Pulse Generators

The PWM based firing control system was discussed earlier in Chapter 4 and 6. This section describes how this system behaves when the additional active filter signal is added to the existing sag mitigation signal (v_{aref}, v_{bref}, v_{cref}) generated by the sag control strategy shown in Fig.4.12 in Chapter 4. The purpose of this block is to derive the firing pulses to

the IGBT switches of the series cascade converter so that the desired reference voltages as demanded by the sag or/ and harmonics mitigate controllers are actually generated by the converter. This is achieved by using these three phase voltages as the modulation signals for the Subharmonics Pulse Width Modulation technique (SHPWM) described earlier in Chapter 4.

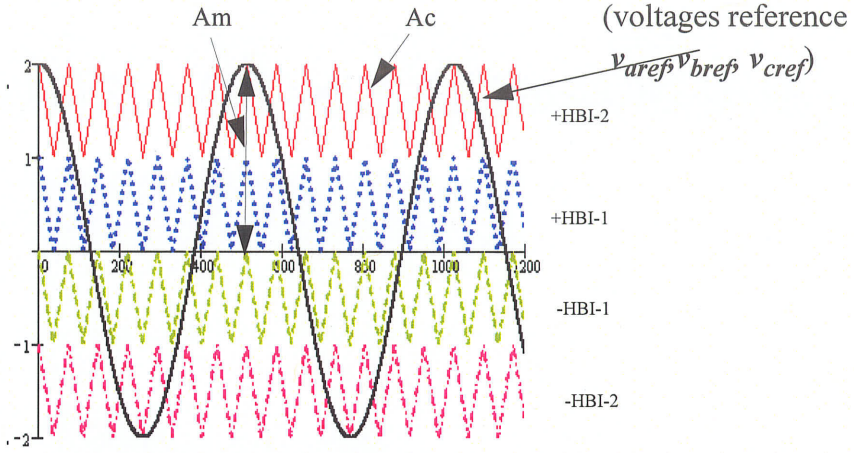


Fig.7.7: SHPWM for five level cascade inverter (during the sag mitigation only)

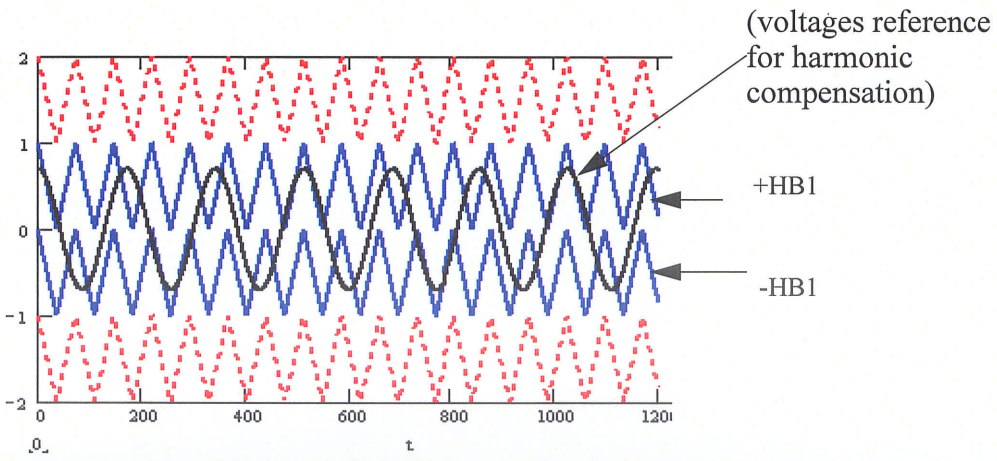


Fig.7.8: SHPWM for five level cascade inverter (during the harmonic compensation only)

To see how the system behaves two modes of operation were considered. The first mode of operation is during the sag mitigation control as discussed in Chapter 4, the modulation

index value and the level of the injection voltage can vary depending on the sag depth. From Fig. 7.7 during this control mode the modulation index (M) is defined as

$$M = \frac{2A_m}{(n-1)A_c} \quad (7.5)$$

A_m: The amplitude of the modulation wave (voltages reference $v_{aref}, v_{bref}, v_{cref}$).

A_c: The amplitude of the carrier wave

The second operating mode is during the harmonic compensation. The typical voltage injection capability of DVR is assumed to be in the range of 50%. Hence, to compensate for harmonics as low as 2% (or lower) the system must operate at modulation index of around 4% (or less) therefore only HBI-1 as shown in Fig. 4.3 of the multilevel cascade inverter will operate during the harmonics compensation. During this control mode the modulation index (MI) from Fig. 7.8 is defined as

$$M_{Harmonic} = \frac{A_m}{A_c} \quad (7.6)$$

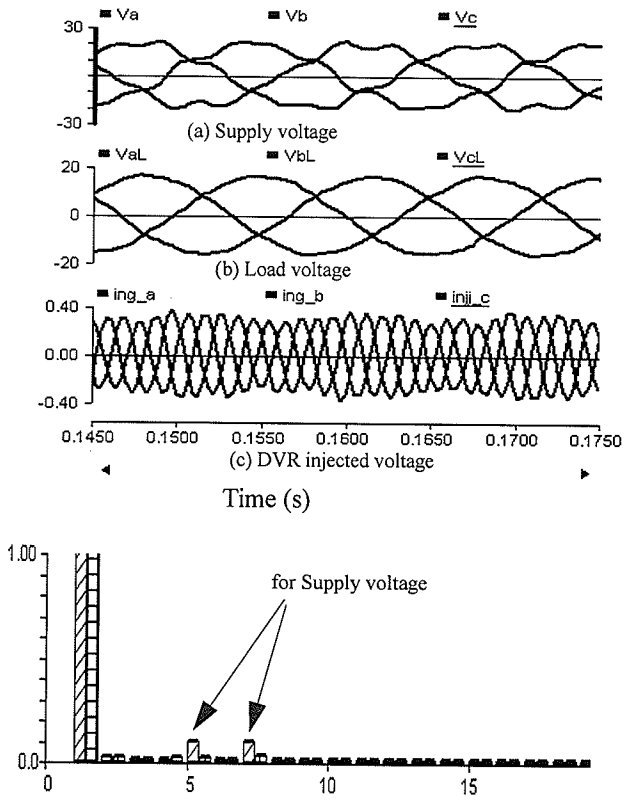
From (7.5) and (7.6) It is clear that due to assignment of harmonics cancellation to a single H-bridge, the modulation index for harmonic compensation is (n-1)/2 times larger than modulation index for sag mitigation. Thus reduces the sensitivity and improves the performance of the harmonic compensation ability of the DVR. The other converters can be bypassed during such operation so as to limit the device losses to the minimum. In order to equalize the stresses and maintain an equal dc voltage across each H-bridge, the role of harmonic elimination can be rotated amongst all the converters.

7.7 Validation of Proposed Method by Simulation

The proposed control system for the DVR is validated in this section using electromagnetic transients simulation using the PSCAD/EMTDC Simulation program.

Chapter 5 demonstrates the voltage sag mitigation for a single line fault and three phase fault in which the sag compensation is achieved with the transient injection of a small amount of real power and the capacitor voltage is reasonably constant. This section presents the results when the same DVR is used for compensating harmonics with different balanced and unbalanced levels of distortion in the supply voltage.

Figures 7.9 -7.11 show the harmonics compensation results for balanced and unbalanced supply voltages and with a non-linear load current. The non-linear current causes supply-side voltage distortion due to the source's impedance. The harmonic cancellation method described in Section 7.6 is used to cancel the 5th and 7th harmonics.



(d) Harmonic spectrum for supply and load voltage

Fig. 7.9:Selective harmonic compensation for System with balanced supply voltage THD of 20%

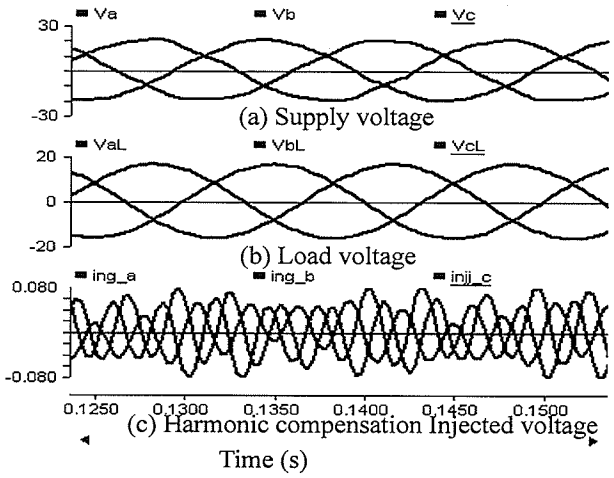


Fig. 7.10:Selective harmonic compensation for System with balanced supply voltage THD of 6.5%

Figs. 7.9 a and b show the supply and load side voltage waveforms. The supply side has a large total harmonic distortion (THD) of 20% (5^{th} =12%, 7^{th}= 10%) which is compensated out resulting in the load voltage having a much reduced THD of only 1.5% (5^{th} =1.5%, 7^{th}= 0.5%). The injected voltage waveforms are shown in Fig. 7.9c, and can be seen to have a predominant 5th and 7th frequency content. Figures 7.9d show the frequency spectra of the supply and load phase voltages.

The approach also works well with a much smaller level of distortion. If the harmonic compensation function is assigned to the entire converter, it can be shown that this situation is difficult to rectify due to the high sensitivity of the converter. By assigning the harmonic cancellation duty to only one converter, the sensitivity is reduced and control becomes straightforward. Fig. 7.10 a and b show the supply voltage with a THD of a smaller THD of 6% (5^{th} = 3%, 7^{th}= 2%). The load voltage is seen to have much reduced THD of (0.5% 5^{th} =.2%, 7^{th}= 0.1%).

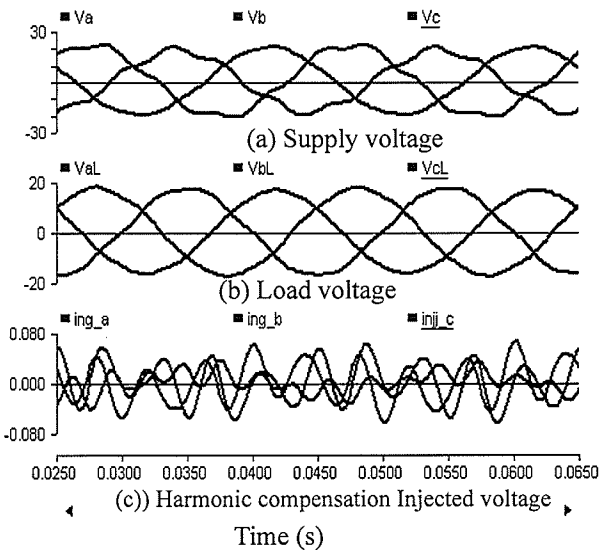


Fig. 7.11: System with unbalanced supply voltage (phase a with THD of 0.5%, phase b with THD of 6.5%, and phase c with THD of 9%)

In the simulation results shown in Fig. 7.11, the non-linear load in each phase was modified so as to produce unbalanced THD values of 20%, 10% and 2% in supply side voltage phases a, b and c respectively. Fig 7.11b shows the load voltages after harmonic compensation, with much reduced harmonic distortion of 1.2%, 0.9% and 0.3% in load side voltage phases a, b and c respectively. These waveforms show that the compensation is possible individually in each phase.

CHAPTER 8
Experimental Setup and Results

8.1 Introduction

The proposed DVR concepts described in Chapters 5, 6 and 7 was constructed and tested in the lab. The details of this process are described in this Chapter. Due to limited availability of components, and rating of the lab equipment it was not possible to build the 13 KV circuit described in Chapter 5, 6 and 7. Instead, a single phase circuit with scaled down rating was built.

This chapter is consist of two main sections. The first section describes the experimental setup and the hardware circuits for the compensation of the voltage sags, voltage swells and voltage harmonics. The second section presents the experimental results of the mitigating and compensating process.

8.2 Experimental Setup

The circuit topology is illustrated in Fig. 8.1.The system parameters are given in Table 8.1

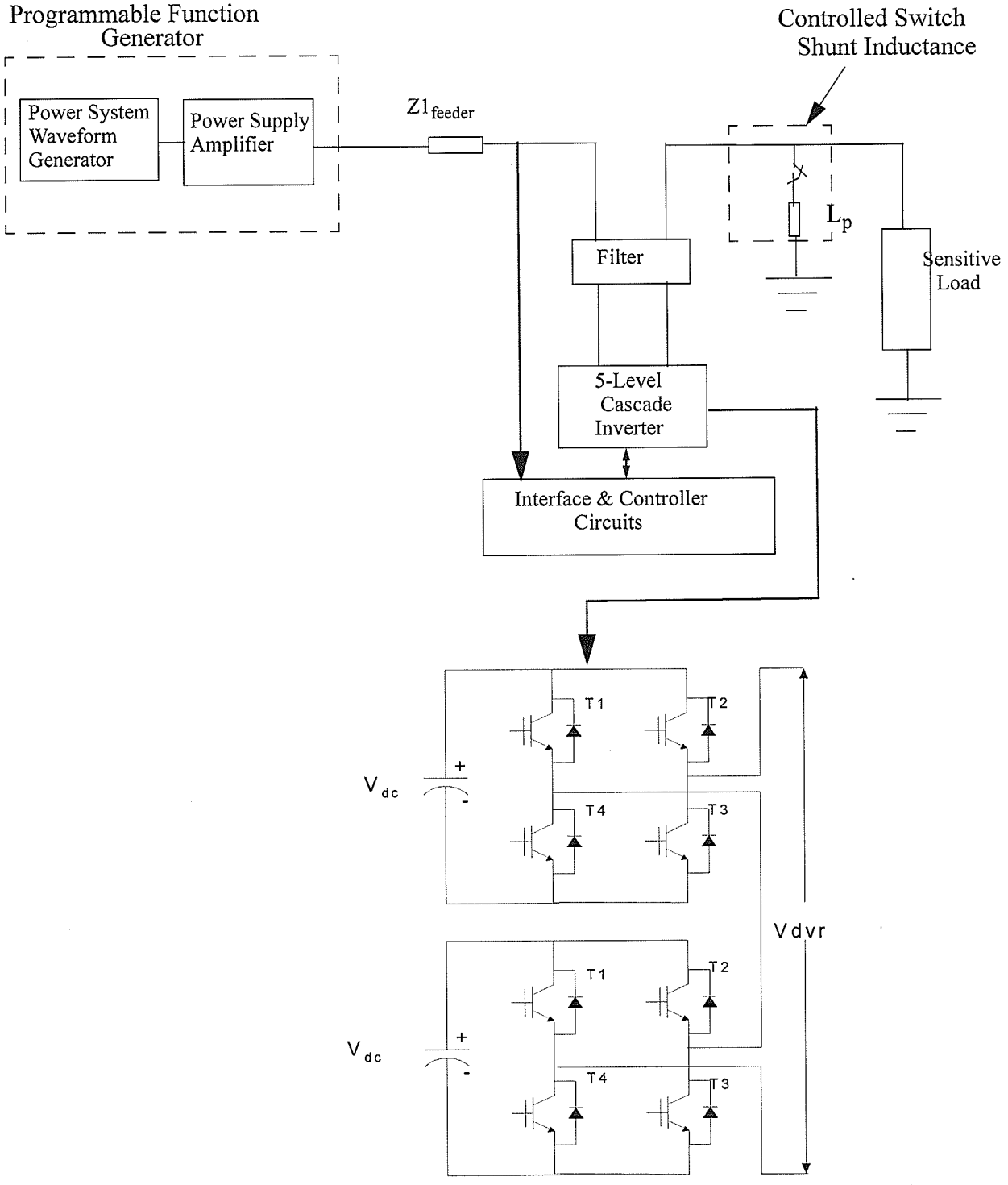


Fig. 8.1 Experimental setup for voltage sags, swells and harmonics mitigation

Table 8.1. Main test system parameters

Item	Values
Line voltage	40V /60 Hz
Line resistor R_{line}	1 ohm
Line inductance X_{Line}	0.5 ohm
Filter inductor L_f	2 mH
Filter capacitor C_f	15 μF
Load inductance L_l	(1 to 60) mH
Load resistor R_l	20 ohm
DC link capacitor	2600 μF
Switching frequency	1800 Hz
Load power factor	(0.6 to 0.99)
Filter cut-off frequency	920Hz
Shunt inductance L_p	40 mH

8.2.1 Programmable Function Generator (PFG)

The programmable function generator is capable of producing source side sags or swells and also has the ability to create harmonics distortion. The PFG consists of a Real Time Playback (RTP) unit and Power Supply Amplifier (PSA) as shown in Fig. 8.2. The Real Time Playback (RTP) suite of tools is a computer based testing environment useful for testing power system protection, control and monitoring systems. Best described as a 12-channel arbitrary waveform generator, the RTP can generate waveforms from COMTRADE [44] data files or by using the RTP STATE program [44]. The STATE simulator program is used to produce the testing waveforms. Each of the 12 analog channels can be programmed with a fundamental frequency, voltage sags with different magnitude

and duration, voltage swells with different magnitude and duration and harmonic content values.

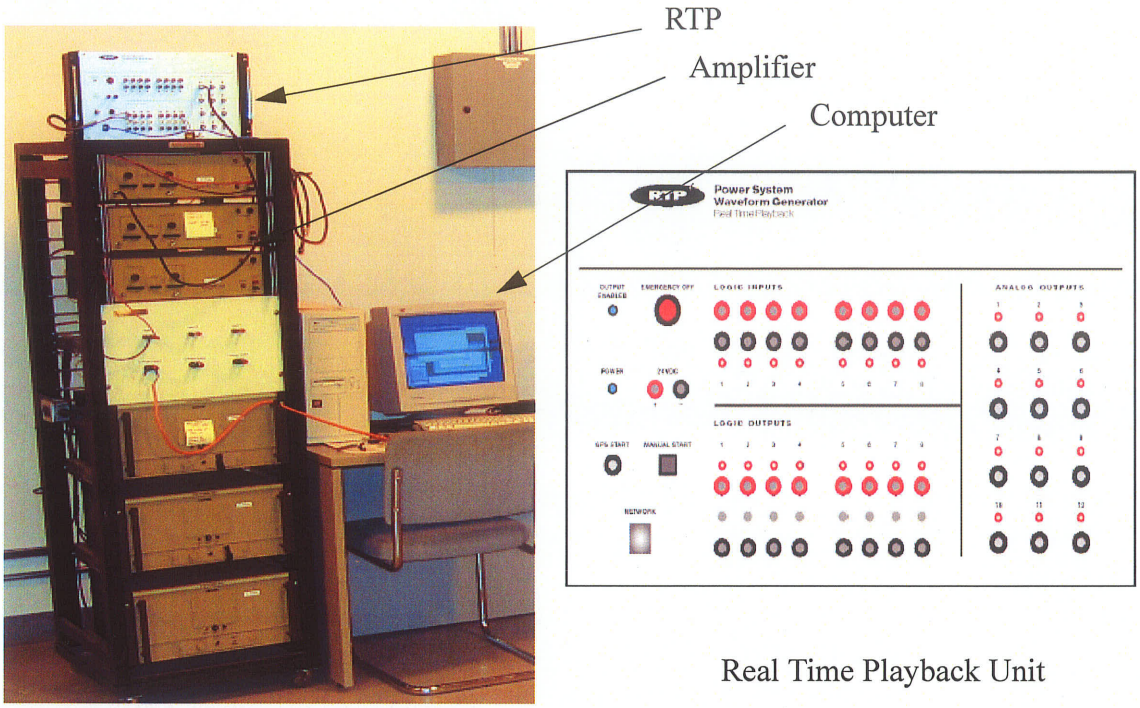


Fig. 8.2 Programmable Function Generator (PFG)

The output voltage is +/- 10 V peak. The RTP output voltage waveform is amplified using an external amplifier as shown in Fig. 8.2. An rms voltmeter, is used to determine or adjust the amplifier gain.

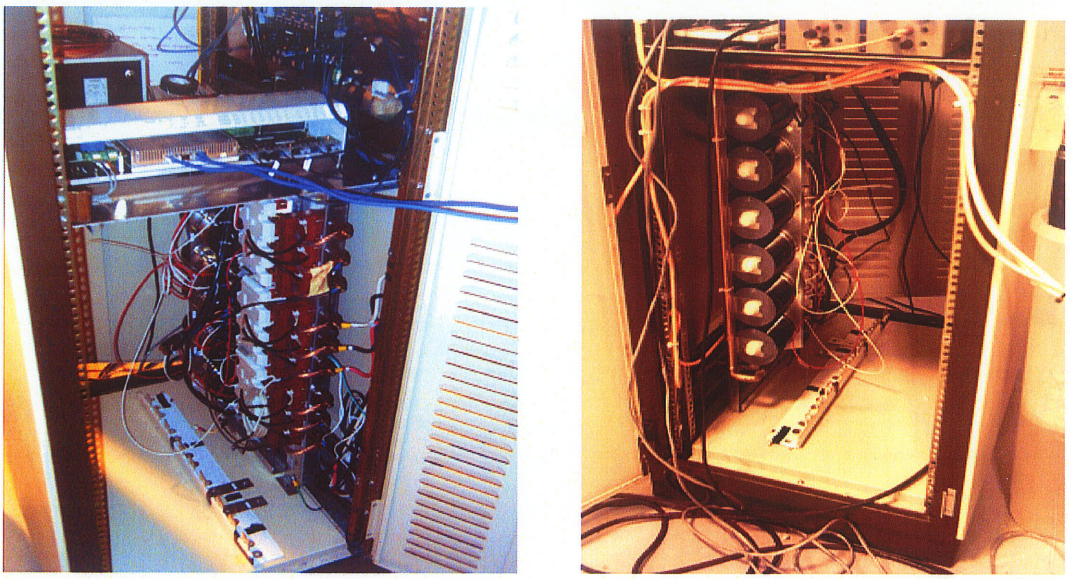
8.2.2 The Filter Circuit

The adopted filter is a second order low-pass filter which consists of a coil of 2mH and a capacitor of 15μF. The filter is design to work for both the voltage sag mitigation and harmonics compensation, because in voltage sags, the injected voltage by the cascade inverter has a frequency equal to the fundamental frequency; while in the harmonics com-

pensation the injected voltage by the cascade inverter has a frequency that is higher than the fundamental frequency.

8.2.3 The 5-Level Cascade Inverter

A single-phase 5-level cascade voltage source converter is connected in series with the system. The 5-level cascade inverter consists of two SKiM 5 IGBT modules(300A, 600V), Fig. 8.3 (a) shows three SKiM 5 IGBT modules. Two of them are used for designing the 5 -level cascade inverter. Each SKiM 5 IGBT module is connected as H-bridge configuration with separate dc-storage in the form of two 5200μF capacitors connected in series. Six of these capacitors are shown in Fig. 8.3(b). SKHI 65 gate driver, is used to drive SKiM 5 IGBT modules. This driver provides a complete solution with integrated protection and monitoring functions, potential isolation and an interface for controllers. Fiber optical serial links are used to isolate the control circuits from the power circuit. The dc charging method is based on the ability of charging the capacitors by energy drawn



(a) Three SKiM 5 IGBT modules (b) Dc-storage (6 5200μF capacitor)

Fig. 8.3 5-Level cascade inverter

from the system it self without any connection on the dc side of the DVR, the proposed method is discussed in detail on the control section of Chapter six.

8.2.4 The Loads

These loads consist of groups of linear loads; resistors and inductors. They are interconnected so as to produce a required load where the load power factor and magnitude can be changed as required.

8.2.5 Interface Circuits and Controllers

The interface circuits and controllers as shown in Fig. 8.4. They consist of a Power Electronic Controller (PEC), two Power Electronic Controller Measurement Interfaces (PECMI) with two Low Voltage Divider (LVD) and Power Electronic Building Block (PEBB) interface. The two PECMI and the PEBB are connected to the PEC via optical links. The control software is programmed with Matlab/Simulink and is running on the PEC.

Power Electronic Controller (PEC): The PEC as shown in Fig. 8.5 is ABBs [45] high-end process control system. The AC 800PEC controller is configured and programmed

using MATLAB/ Simulink with Real-Time The AC 800PEC is a modular high-speed con-

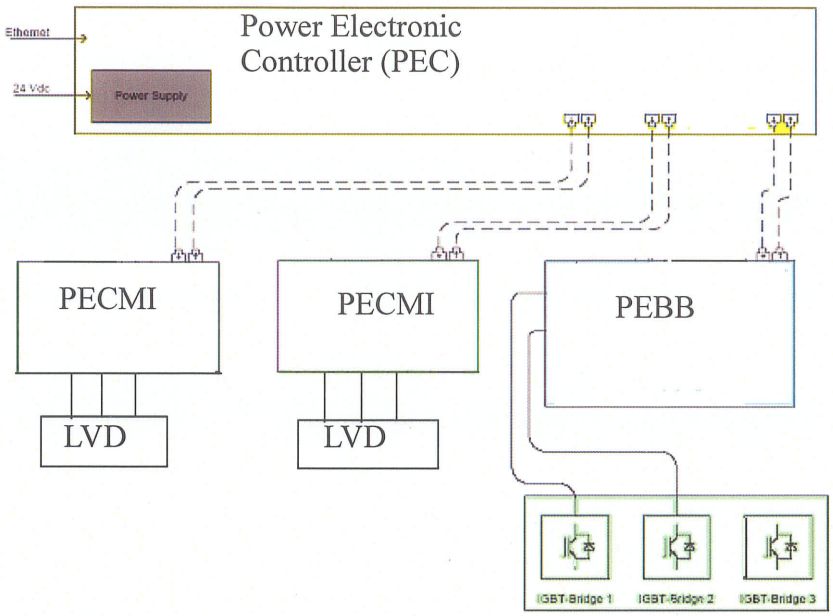


Fig. 8.4 The interface circuits and controllers (ABB)

trol system. The modules are arranged according to the required I/O configuration and the process. The controller combines a very powerful CPU and large Field-Programmable Gate Array, which suits AC 800PEC to control demanding power electronics systems.

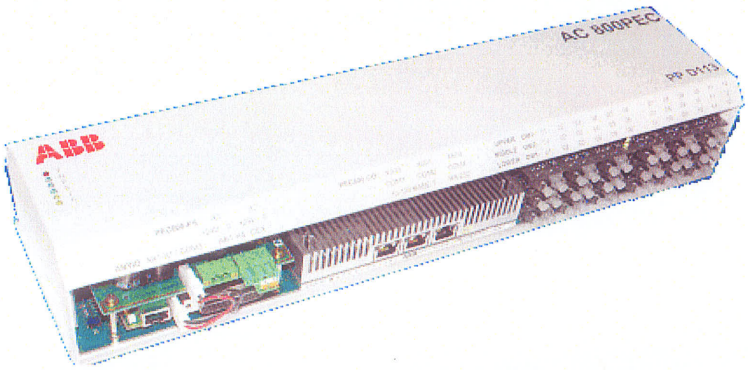


Fig. 8.5 A Power Electronic Controller (PEC) [45]

Power Electronic Controller Measurement Interfaces (PECMI) Circuit: The PECMI UA D140 [45] is a current- and voltage-measurement device. The module provides three

Hardware (HW) interface types, a digital (optical) for communication, analog data interfaces for measurement inputs. Three channels have been used the first one to measure the supply voltage, the second one to measure the load voltage and the last one to measure the load current.

Low Voltage Divider (LVD) Circuit: The LVD is a resistive voltage divider with 4 channels for low voltage applications up to 1000Vrms or 1500VDC. The design of the resistive divider part is such as to ensure best frequency response and still meeting the safety requirement according to EN50178.

Power Electronic Building Block (PEBB) Interface Circuit: The PEBB Interface is an universal remote I/O device to drive directly two PEBB channels with up to 2 * 6 pulses and to measure and monitor all analog and digital signals of two H-bridge inverter via 2 optical links. Each H-Bridge inverter receives PWM firing pulse with a carrier frequency of 1800Hz.

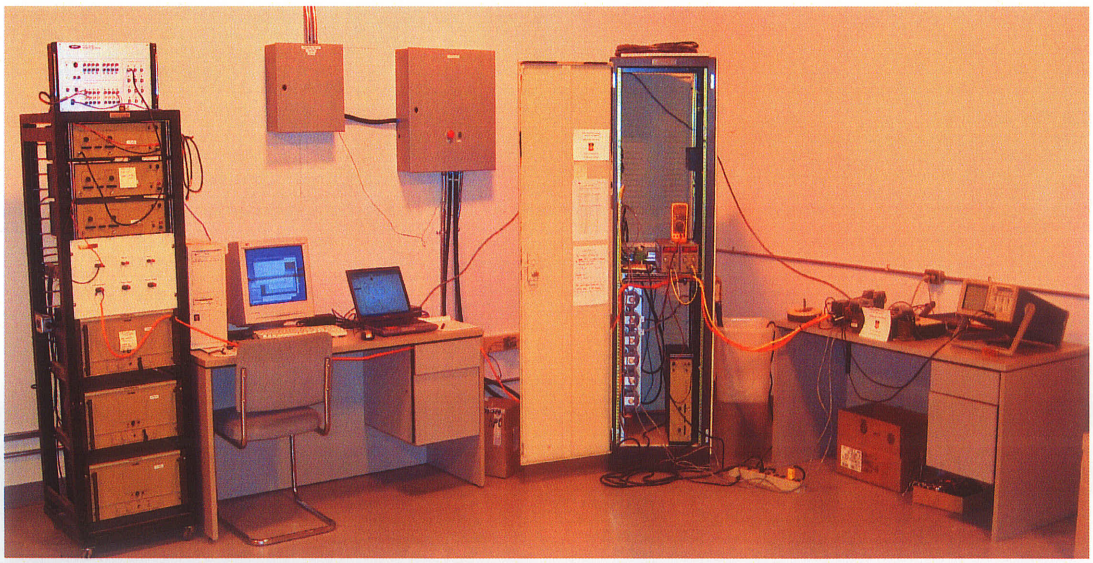


Fig. 8.6 The hardware for the experimental setup

8.3 Experimental Results

8.3.1 Voltage Sag and Swell Mitigation

This section provides the experimental results for mitigating the voltage sags and swells by using the experimental setup that is displayed in Fig. 8.6. The experimental results will be focused on examining the ability of the proposed control methods to mitigate the sags with minimum or zero real power injection and the ability of charging the capacitors and maintains an equal dc voltage across each H-bridge. To achieve this objectives 40% supply voltage sag will be introduced to the supply voltage with two different load power factors. In first case, 40% supply voltage sag will be introduced to system with 0.6 load power factor. In the second case, 40% supply voltage sag will be introduced to system with 0.98 load power factor. In the second case the benefit of the shunt controlled inductance will be presented. The sag detection circuit was not used. The sag mitigation method was initiated as soon as the sag was applied at a preset time. This is completely adequate because we are only investigating the sag mitigation (not detection) capability of the DVR.

For the first case, the voltage sag is 40% and 0.6 load power factor. Fig. 8.7 shows 0.2 sec. sagged supply voltage waveform with the mitigated load voltage waveform. It is evident that 100% sag mitigation is achieved. While Fig. 8.8 shows a zoom waveform for Fig. 8.10 which shows a smooth the transient stage between sag and normal operation and a switching harmonics free load voltage waveform

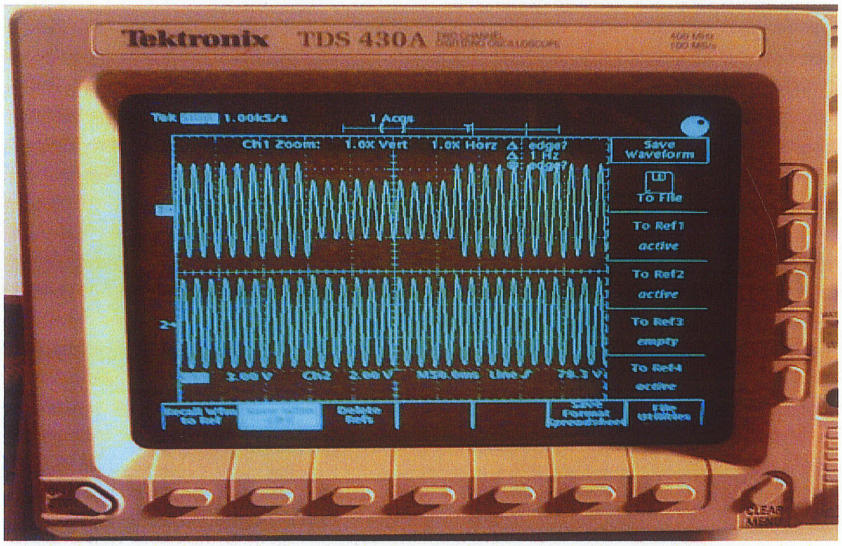


Fig. 8.7 40% supply voltage sag with mitigated load voltage waveforms

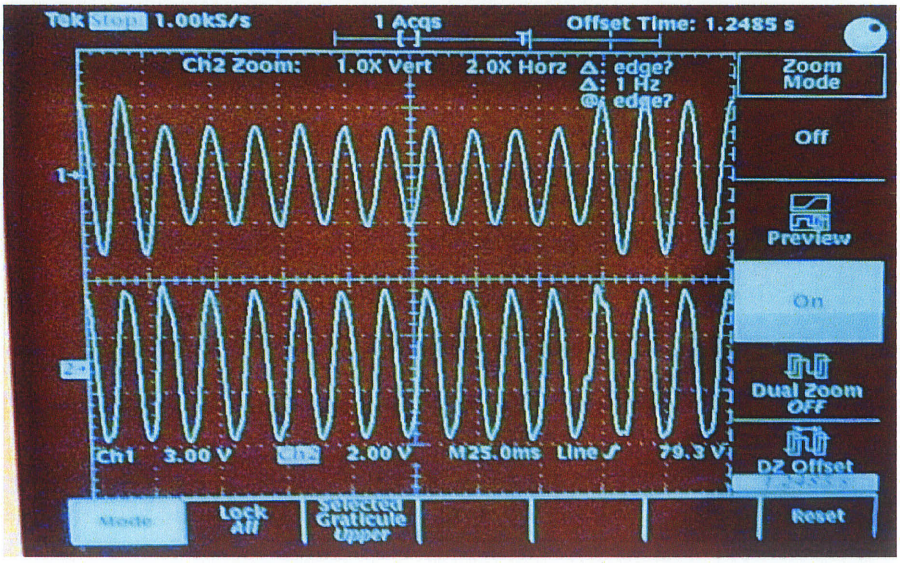


Fig. 8.8 Zoom in of Fig. 8.7

Fig. 8.9 and Fig.8.10 show the 0.5 sec. 40% supply voltage sag and 1 sec. of 40% supply

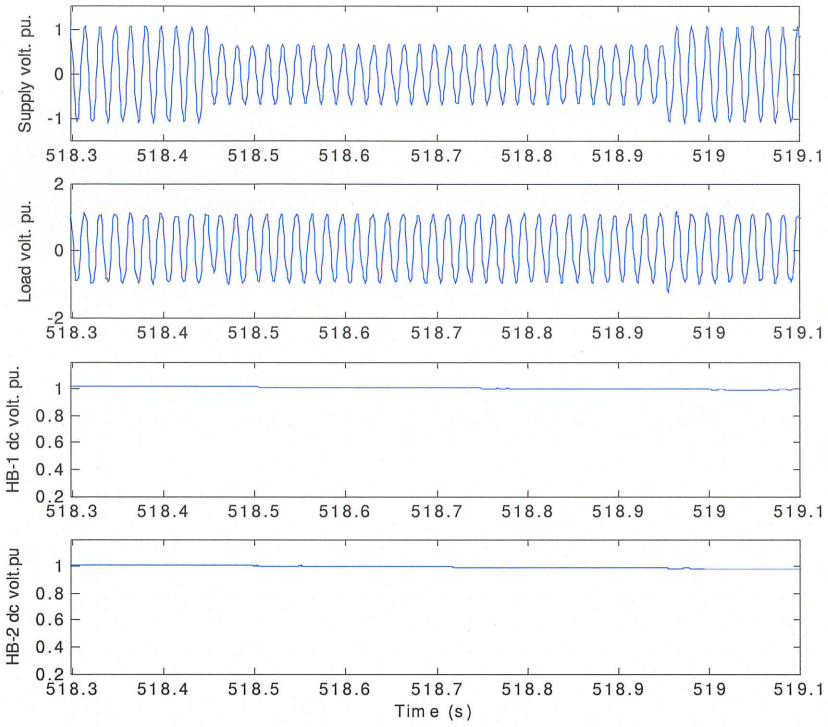


Fig. 8.9 Supply voltage with 0.5 sec. 40% sag, load voltage, HB-1 dc voltage and HB-2 dc voltage Waveforms respectively

voltage sag. By observing the capacitors dc voltage across each H-bridge, it is evident that the sag mitigation was achieved with zero real power injection and the controls were able to maintain equal dc voltages across each H-bridge. It is also evident that for system with poor load power factor the proposed method can mitigate long sags with zero real power injection and with significant smaller dc voltage storage.

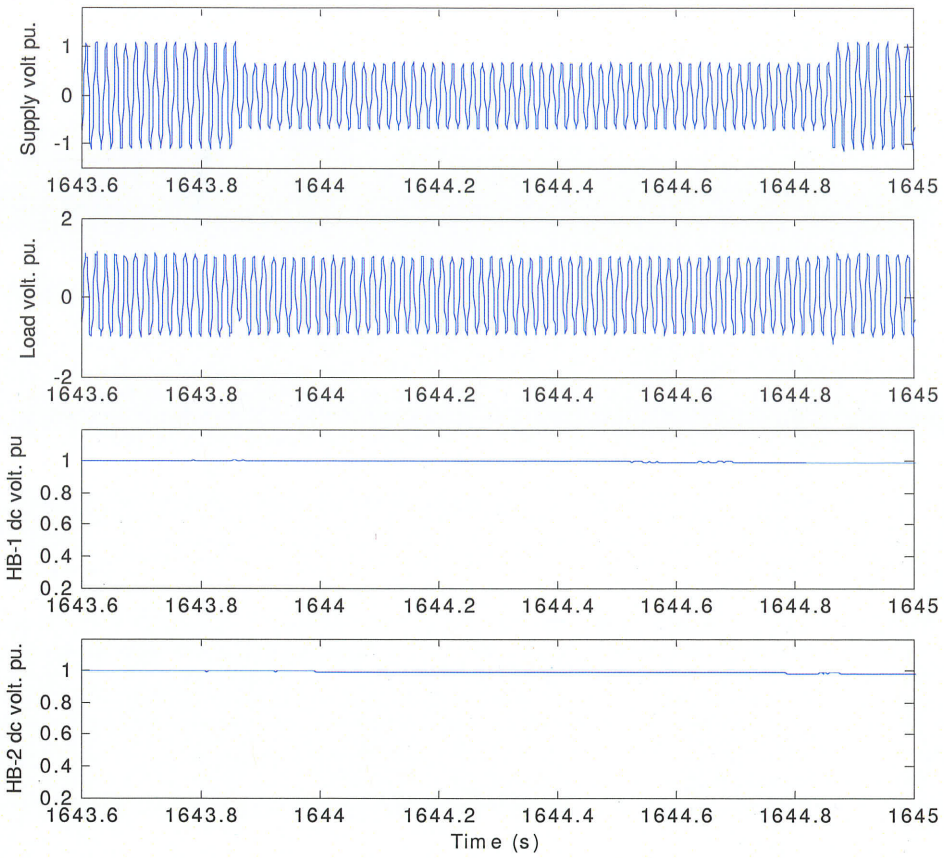


Fig. 8.10 Supply voltage with 1 sec. 40% sag, load voltage, HB-1 dc voltage and HB-2 dc voltage Waveforms respectively

For second case, 40% supply voltage sag for system with 0.95 load power factor. During the sags the shunt inductance is switched on as discussed in Chapter 6. The shunt inductance is selected (R_l/X_p =*1.32*) so that creating a new load power factor 0.602. Fig. 8.11 shows 0.4 sec. sagged supply voltage waveform with the mitigated load voltage waveform after introducing the controlled switch shunt inductance to reduce the load power factor to be 0.602 during the sag event. It is evident that 100% sag mitigation is achieved. Fig. 8.12 shows shorter duration supply voltage waveform of 0.2 sec. with the mitigated load volt-

age waveform after introducing the controlled switch shunt inductance to reduce the load power factor to be 0.602 during the sag event. It is evident from Fig 8.12 the smooth the transient stage between sag and normal operation, the smooth introducing of the switch control inductance and a switching harmonics free load voltage waveform.

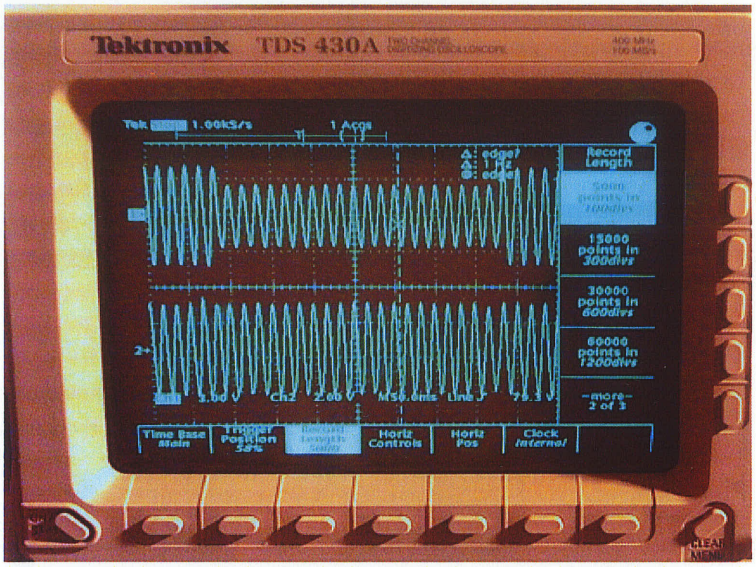


Fig. 8.11 0.4 sec. 40% supply voltage sag with mitigated load voltage waveforms

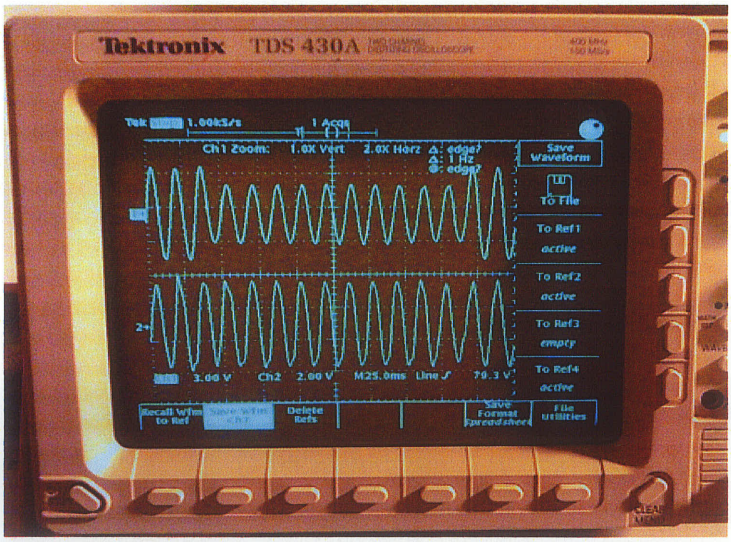


Fig. 8.12 0.2 sec. 40% supply voltage sag with mitigated load voltage waveforms

Fig.8.13 shows the 0.3 sec, 40% supply voltage sag for system with 0.95 load power factor. The DVR attempts to mitigate the voltage sag without modifying the load power factor as seen by the DVR by introducing the controlled switch inductance. As expected real power was injected to mitigate the sag because the ability of the DVR to mitigate the voltage sag without real power injection is dependent on the load power factor as discussed in Chapter 4. It is evident from Fig 8.13 that due to injecting the real power from the dc voltage storage there is a significant drop in the dc voltage to the point where the DVR is no longer are able to mitigate the voltage sag.

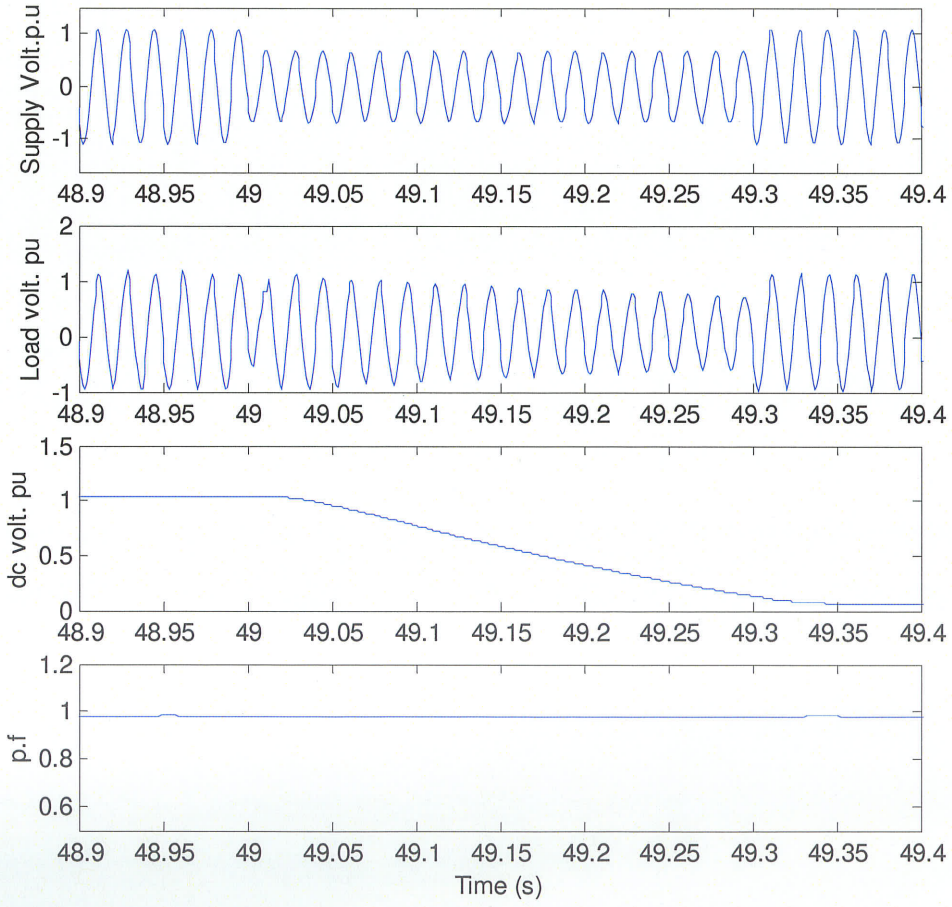


Fig. 8.13 Sag voltage mitigation without the control switch inductance

Fig.8.14 shows a 1 sec, 40% supply voltage sag for the system with 0.95 load power factor. The DVR attempt to mitigate the voltage sag by modifying the load power factor as described in Chapter 6 to 0.602 by switching in the shunt inductance during the sag event. As expected no real power was injected to mitigate the sag because the ability of the DVR to mitigate the voltage sag without real power injection is depend on the load power factor as discussed in Chapter 4. It is clear from Fig 8.14 that both of the H-bridges have constant and balanced dc voltage and the load power factor as seen by the DVR is changed from 0.95 to 0.59 during the sag event. It is evident from Fig. 8.14 that the proposed DVR voltage sags mitigation ability to mitigate long sags has improved significantly by introducing the controlled switched shunt inductance during the sag event.

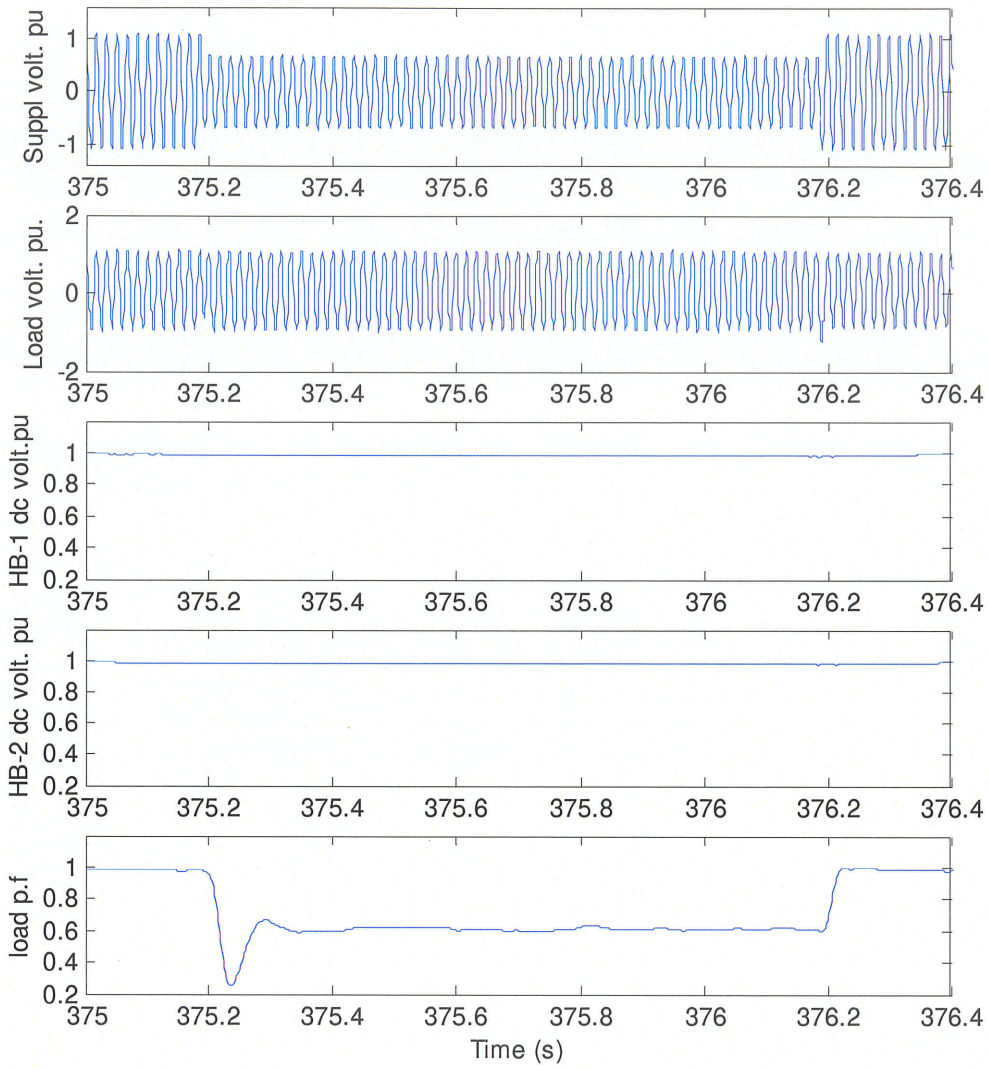


Fig. 8.14 Sag voltage mitigation with the control switch inductance

Fig. 8.15 shows waveform of 30% supply voltage swell for 0.3 sec. with a mitigated load voltage waveform. It is evident from Fig.8.18 that the proposed DVR has an excellent capability to mitigate a voltage swells.

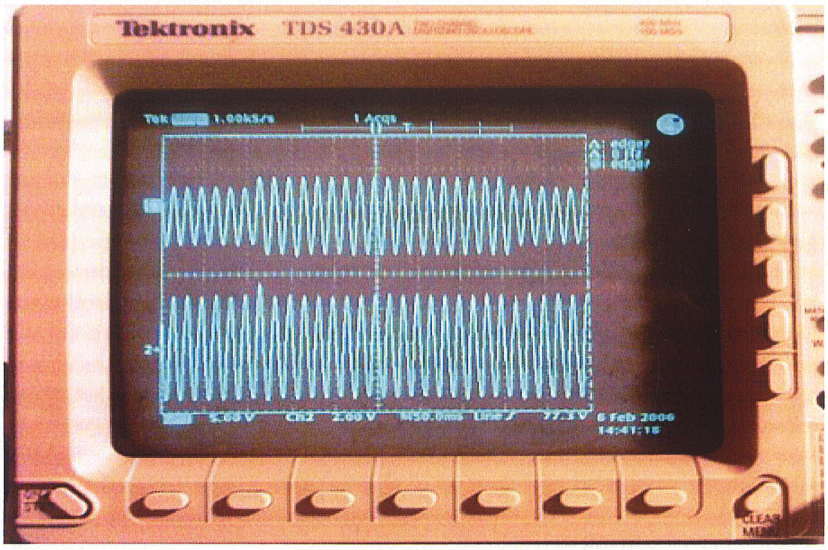


Fig. 8.15 0.4 sec. 30% supply voltage swell with mitigated load voltage waveforms

8.3.2 Voltage Harmonic compensation

Here, the results of the three cases for the compensation of harmonics at the voltage level of 40V. In the first case, the distorted supply voltage waveform, which is principally produced by the Real Time Playback (RTP) and the compensated load voltage waveform are depicted in Fig. 8.16. The distorted supply voltage waveform has 15% 5^{th} harmonic with 90 degree phase shift from the fundamental 60 Hz voltage. It is clear from the load voltage waveform that the 5^{th} harmonic compensation was successfully achieved. The experiment was repeat with different harmonics presented in the supply voltage and harmonics com-

pensation results are depicted in Figures (Fig. 8.17, Fig. 8.18 and Fig. 8.19) where the supply voltage harmonics are 15% 7^{th} harmonic with zero degree phase shift, 15% 5^{th} harmonic with 90 degree phase shift and 15% 7^{th} harmonic with 45 degree phase shift, and 10% 4^{th} and 15% 7^{th} harmonic with 90 degree phase shift respectively. From the above Figures it is evident that the selective harmonics compensation method was successfully achieved.

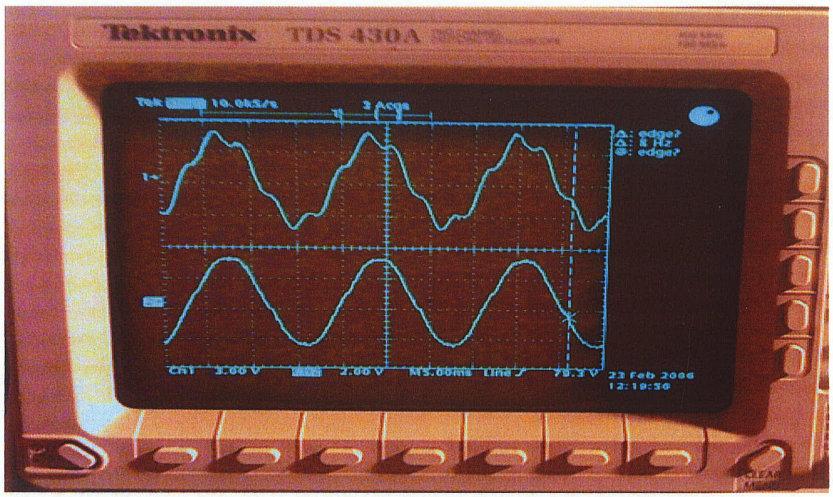


Fig. 8.16 Distorted supply voltage with 15% 5^{th} harmonic with 90 degree phase shift and the compensated load voltage

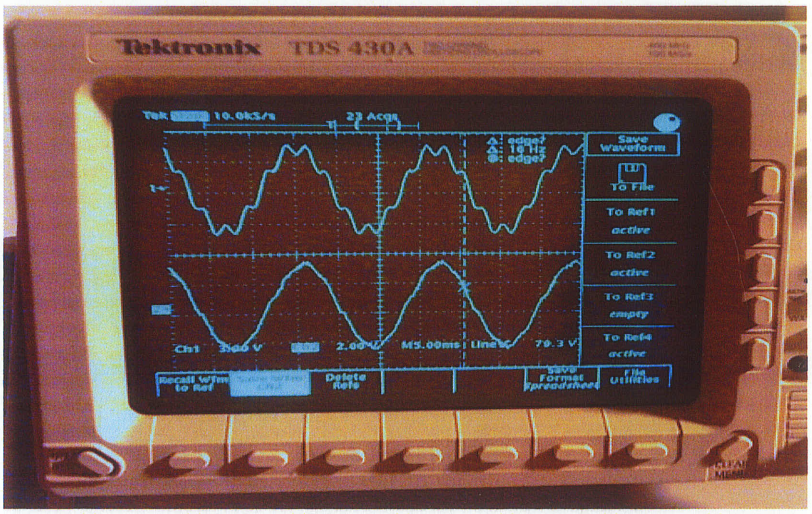


Fig. 8.17 Distorted supply voltage with 15% 7th harmonic with 90 degree phase shift and the compensated load voltage waveform

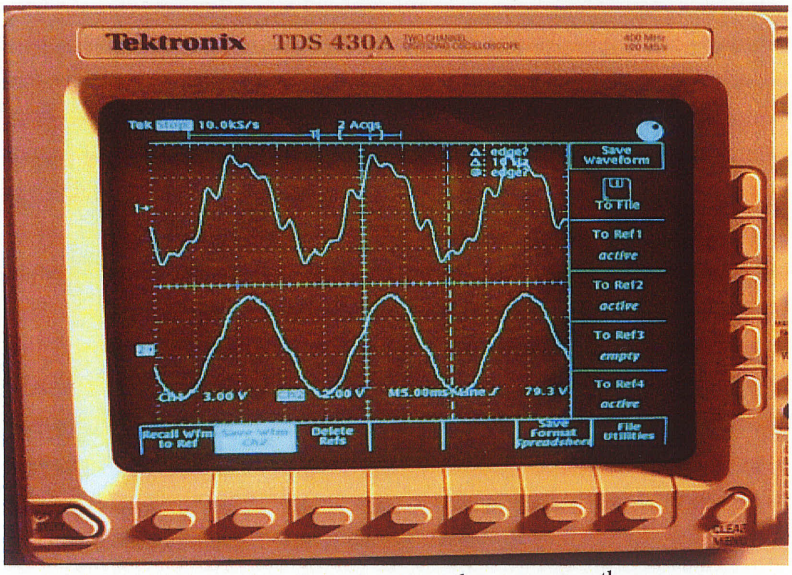


Fig. 8.18 Distorted supply voltage with 15% 5th and 15% 7th harmonics and the compensated load voltage waveform

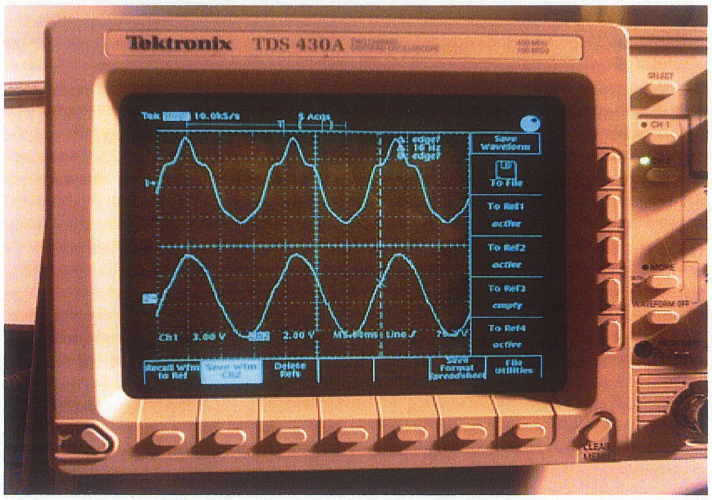


Fig. 8.19 Distorted supply voltage with 10% 4th and 10% 5th harmonics and the compensated load voltage waveform

8.4 Summary

This chapter presents the experimental setup and results of the proposed DVR circuit topologies and the proposed mitigation control strategies described in Chapter 4, 6 and 7. The voltage sags are mitigated to be approximately 1 pu. with minimum injection of real power. The proposed DVR voltage sags mitigation ability to mitigate long sags has improved significantly by introducing the controlled switched shunt inductance during the sag event. The selective harmonies compensation are successfully achieved. The results are in good agreement with the simulation results that are demonstrated in Chapter 5, 6 and 7. The experimental results prove the feasibility and the practicality of the proposed novel strategies and novel topology.

CHAPTER 9

Contributions and Future Research Work

This chapter lists the contributions and conclusions of the research work. Also areas for future research, based on the proposed concepts and techniques, are suggested.

9.1 Conclusions and Contributions

The conclusions and contributions of this thesis relating to the DVR mitigation strategy, the modified DVR topology and the DVR auxiliary function of harmonics compensation are itemized as follows:

- **Selection of an Appropriate Topology:** The thesis conducted a critical analysis of various available DVR options that included energy storage possibilities. The H-bridge cascade converter topology was employed to develop the DVR system because of the following advantages. The first advantage is that each bridge can be controlled independently permitting efficient single phase voltage compensation. The second aspect of

particular interest in this research is the inherent energy storage capability of the capacitors which makes this topology ideal for transient injection of real power. The third advantage is the modularized circuit layout and the property of transformer-free operation resulting from the fact that the voltage of the converter can be matched to the system, that means less cost and no leakage inductance which further constrains the power flow.

- **Selection of the Switching Method**: Both the fundamental frequency switching (FFS) and pulse width modulation (PWM) techniques for the multilevel cascade inverter were investigated. The triangular carrier phase-shifting PWM technique is especially suitable for cascaded multilevel inverters because each H-bridge module receives its unique triangular carrier, which is phase shifted with respect to its neighboring bridge.
- **Mitigation Strategy:** A parametric analysis of the sag-control capability as a function of the load power factor was first conducted, and then used to design a new control strategy that minimized the real energy injected by the DVR. The proposed mitigation method has the capability to mitigate longer duration sags without the requirement of having large capacitor banks. Special consideration is also given to the case when the injected voltage attains its ceiling.
- **The Control System:** Based on the mathematical and simulation based analysis, a control strategy for compensating and mitigating voltage disturbances in distribution system while optimizing the dc-side energy storage was developed. The proposed control strategy shows the following promising features.

  1- The new control mitigating strategy is simple to implement.

2- The capacitors have the ability to charge using energy drawn from the system itself without any connection to the dc side of the DVR.

3- It is easy to maintain the individual capacitor voltages at desired levels by controlling the phase angle for each H-bridge carrier waveform of the triangular carrier phase-shifting PWM technique.

4- Adequate dynamic performance was obtainable with high control stability.

- **Unbalanced Operation**: The simulation studies confirm that the proposed DVR topology has excellent performance for mitigating balanced and unbalanced voltage sags.
- **Topology Enhancements for Further Reduction of Real Power:** A modification was introduced to the basic cascade inverter topology and the corresponding control system where the capacitor energy storage can be even further reduced active modulation of the power factor during a sag. The modification consists of adding a shunt thyristor switched inductor. The modified DVR circuit topology has the ability to mitigate severe and long duration voltage sags with comparatively small energy storage capacitors.
- **Parametric Analysis of Operating Limits of the New Topology**: For the modified DVR circuit topology analytical formulation was conducted to find the sag depth which can be mitigated without injecting real power for different ratios of load resistance to shunt indolence (R_l/X_p). The analysis show that as the R_l/X_p ratio goes higher a more severe sag can be mitigated without injection of real power.
- **DVR auxiliary function of harmonic compensation**: A novel feedback control strategy was added to the proposed DVR system to provide the additional duty of steady state load voltage harmonics cancellation (active filter). A novel control method where

only one of the H-bridge converters in the multilevel cascade converter is assigned the additional duty of harmonic cancellation was successfully implemented. Due to the considerable difference between the voltage injection levels required for the primary DVR function and the auxiliary DVR function, such a strategy is much more difficult to implement on a conventional DVR. The proposed auxiliary function can improve the power quality even further without any significant extra cost or any adverse impact on the primary sag control function. The simulation studies confirm that the proposed compensation method were able to compensate harmonics with different balanced and unbalanced levels of distortion in the supply voltage without any cross-coupled effect on other phases.

- **Finally, Validation Through Lab Prototype:** an important contribution of this research work is the hardware validation of the proposed DVR circuit topologies in the laboratory. The experimental results are provided to prove the feasibility and the practicality of the proposed novel strategies and novel topology.

9.2 Future Research Work

Future research can be carried out along these lines:

- Extending the capability of the proposed novel DVR circuit topology by controlling the shunt inductance value as a function of sag depth to enhance the performance and further optimize the real power injection.
- Further investigating for switching and conduction losses are needed to critically asses the efficiency of the proposed topology.

- For actual implementation, a cost / performance analysis is necessary to select the operation limits and other parameters.

References

[1] IEEE std.1159-1995, Recommended Practice on Monitoring Electrical Power.

[2] Electrical Power Research Institute (EPRI), Power Quality in Commercial Building, BR-I05018, Palo Alto, California, 1995.

[3] Keppler, T.; Watson, N.; Arrillaga, J.; "Computation of the short-term flicker severity index," IEEE Transactions on Power Delivery, Volume: 15, Issue: 4, Oct. 2000 Pages:1110 - 1115

[4] Stones, J.; Collinson, A.; "Power Quality," Power Engineering Journal, Volume: 15, Issue: 2, April 2001 Pages:58 - 64

[5] Fayyaz Akram, M.; Mumtaz Bajwa, S.; "A sample power quality survey for emerging competitive electricity market in Pakistan," Multi Topic Conference, 2001. IEEE INMIC 2001. Technology for the 21st Century. Proceedings. IEEE International, 28-30 Dec. 2001 Pages:38 - 44

[6] El Mofty, A.; Youssef, K.; "Industrial power quality problems Electricity Distribution," 2001. Part 1: Contributions. CIRED. 16th International Conference and Exhibition on (IEE Conf. Publ No. 482), Volume: 2, 18-21 June 2001 Pages:5 pp. vol.2

[7] M. H. J. Bollen, "Understanding Power Quality Problems, Voltage sags and Interruptions," IEEE press, 2001.

[8] G. T. Heydt, Electric Power Quality. Indianapolis, IN: Stars in a Circle Publications, 1990.

[9] Arindam Ghosh, "Power Quality Enhancement Using Custom Power Devices," Kluwer Academic Publishers, pp. xv-xvii, 2002

[10] Van Zyl, A.; Enslin, J.H.R.; Spee, R. "Converter-based solution to power quality problems on radial distribution lines" , IEEE Transactions Industry Applications. Volume 32, Issue 6, Nov.-Dec. 1996 Page(s):1323 - 1330

[11] R. W.Menzies, Y. Zhuang, "Advanced Static Compensation Using a Multilevel GTO Inverter," IEEE Transactions on Power Delivery, April, 1995, pp. 732-738.

[12] J.S.Lai, and F.Z. Peng, "Multilevel converters- A new breed of power converters," in Conf. Rec. IEEE-IAS Annu. Meeting, 1995, pp. 2348-2356.

[13] Al-Hadidi, H.K., and Menzies, R.W.,"Investigation of a cascade multilevel inverter as an STATCOM", Power Engineering Society General Meeting, 2003, IEEE, Volume: 1, 13-17 July 2003, pp. 193 Vol. 1.

[14] Wu Hongyang; He Xiangning, "Research on PWM control of a cascade multilevel converter," Power Electronics and Motion Control Conference", 2000. Proceedings.

PIEMC 2000. The Third International, Volume: 3, 15-18 Aug. 2000 Pages:1099 - 1103 vol.3

[15] Ming Fang, Gardiner A.I., MacDougall A., and Mathieson, G.A., "A novel series dynamic voltage restorer for distribution systems," in Proc. Power System Technology. POWERCON 98, Beijing, Aug. 1998, pp. 38 - 42.

[16] Chan, K., "Technical and performance aspects of a dynamic voltage restorer Dynamic voltage Restorers - Replacing Those Missing Cycles," (Digest No. 1998/189), IEE Half Day Colloquium on, 11 Feb. 1998, pp. 5/1 - 525.

[17] A. Ghosh, and G. Ledwich, "Compensation of distribution system voltage using DVR," IEEE Trans. Power Delivery, Vol. 17, No. 4, pp. 1030-1036, 2002.

[18] Vilathgamuwa D.M., and Wijekoon H.M., "Control and analysis of a new dynamic voltage restorer circuit topology for mitigating long duration voltage sags," 37th IAS Annual Meeting, Oct. 2002, pp.1105 - 1112, vol.2.

[19] Hyosung Kim, Jang-Hwan Kim, Seung-Ki Sul, "A design consideration of output filters for dynamic voltage restorers," Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, Volume 6, 20-25 June 2004 Page(s):4268 - 4272 Vol.6

[20] Heydt, G.T., Tan, W., LaRose, T., and Negley, M., "Simulation and analysis of series voltage boost technology for power quality enhancement," IEEE Transactions on Power Delivery, Volume: 13, Issue: 4, Oct. 1998, pp.1335 - 1341.

[21] Woodley N.H., Morgan L.,and Sundaram A., "Experience with an inverter-based

dynamic voltage restorer," IEEE Transactions on Power Delivery, Volume: 14, Issue: 3, July 1999, pp.1181 - 1186.

[22] Nielsen, J.G., Newman, M., Nielsen, H., and Blaabjerg, F.,"Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," Power Electronics, IEEE Transactions on, Volume: 19, Issue: 3, May 2004, pp. 806 - 813.

[23] Tolbert L.M., and Habetler T.G., "Novel multilevel inverter carrier-based PWM methods," Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE, Volume: 2, 12-15 Oct. 1998, pp.1424 - 1431 vol.2.

[24] A.M. Gole, V.K. Sood, "A Static compensator model for use with electromagnetic transients simulation program", IEEE Transactions on Power Delivery, Vol 5, No 3, July 1990, pp 1398-1407.

[25] Ding Hongfa; Gao Jun; Duan Xianzhong; "New concepts of dynamic voltage restoration for three-phase distribution systems", Power Engineering Society Summer Meeting, 2000. IEEE, Volume: 3, 16-20 July 2000 Pages:1427 - 1432 vol. 3

[26] Haque, M.H.; "Compensation of distribution system voltage sag by DVR and D-STATCOM", Power Tech Proceedings, 2001 IEEE Porto, Volume: 1, 10-13 Sept. 2001 Pages:5 pp. vol.1

[27] H. Akagi, "New trends in active filters for power conditioning," IEEE Trans. Industry Applications, vol. 32, pp. 1312-1322, Nov./Dec. 1996.

[28] N. G. Hingorani, "Introducing custom power," IEEE Spectrum, vol. 32, No.6, pp.41-49, 1995.

[29] F. Z. Peng, H. Akagi, and A. Nabae, "Compensation characteristics of the combined system of shunt passive and series active filters," IEEE Trans. Industry Applications, Vol. 29, No. 1, pp. 144-152, 1993.

[30] Z. Wang, Q. Wang, W. Yao, and J. Liu, "A series active power filter adopting hybrid control approach," IEEE Trans. Power Electron., vol. 16, pp. 301-310, May 2001.

[31] J. H. R. Enslin, R. SpBe, and R. G. Koch, "Using FACTS on the Southern African power grid," EZektron J., vol. 11, no. 11, pp. 16-17, Nov. 1934.

[32] H. Fujita and H. Akagi, "A practical approach to harmonic compensation in power systems-series connection of passive and active filters," IEEE Transactions on Industry applications, Vol.

[33] Truns. lrid. Applicai., vol. '27,p p. 1020-1025, Nov.lDec. 1991. [4] H. Akagi, "Trends in active power line conditioners," IEEE Trans. Power Electron., vol. 9, pp. 263-268, May 1994.

[34] N. Balbo et al., "Hybrid active filter for parallel harmonic compensation," in EPE 1993, Brighton, GB, Sept. 1993, pp. 133-138.

[35] T. J. E. Miller, Reactive Power Control in Electric Systems. New York: Wiley, 1982.

[36] Bhattacharya, D. M. Divan and B. Banerjee, "Synchronous frame harmonic isolator using active series filter," in EPE 1991, vol. 3, pp, 30-35, Firenze, Italy, Sept. 1991.

[37] D. Halim and S. O. R. Moheimani, "Spatial resonant control of flexible strucures -

application to a piezoelectric laminate beam," IEEE Transactions on Control Systems Technology, vol. 9, no. 1, pp. 37–53, January 2001.

[38] B. Singh, K. Al-Haddad, and A. Chandra. A review of active filters for power quality improvements. IEEE Transactions on Industrial Electronics, 46(5):960–971, October 1999.

[39] P. Hsu and M. Behnke, "A three phase synchronous frame controller for unbalanced load," in Proc. IEEE PESC, 1998, pp. 1369–1374.

[40] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady state error," in Proc. IEEE PESC, 1999, pp. 1185–1190.

[41] D. N. Zmood, D. G. Holmes, and G. Bode, "Frequency domain analysis of three phase linear current regulators," in Proc. IEEE IAS Conf., 1999, pp. 818–825.

[42] J. Zeng, X. Guillaud, P. Degobert, "Control of AC machines with Multi-Frequency Resonant Controller," in proceeding of the 11th International Power Electronics and Motion Control Conference (EPE-PEMC 2004), September 2004, Riga, Latvia.

[43] Manitoba HVDC Research Centre, "RTP Operation Manual, Use and Testing", Version 3.3.

[44] ABB Switzerland Ltd. ,"4.5kV Press Pack IGBT Designed for Ruggedness and Reliability", October 2004.

[45] ABB Switzerland Ltd., "Control AC 800PEC. User Guide software version 3.4", October 2004.

APPENDIX A

Mathcad Programs for the Analysis of 7-level Inverter

1. FFS Method

2. SH-PWM Technique

3. SFO-PWM Technique

4. PS-PWM Technique

FFS Method for 7-level Inverter

$$deg := \frac{\pi}{180}$$

$wt := 0..360$ $\quad$ $n := 1, 3..1000$

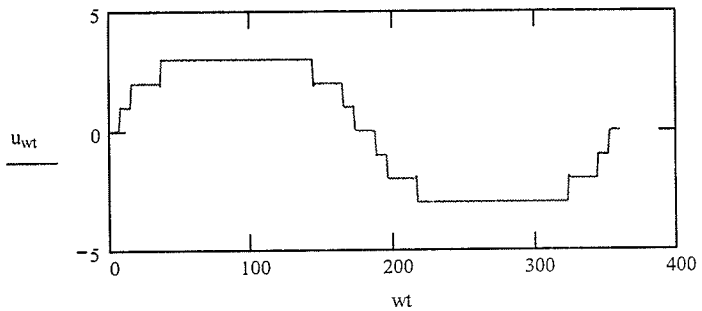
$\alpha 1 := 7.09$ $\quad$ $\alpha 2 := 15.68$ $\quad$ $\alpha 3 := 36.17$

$$ud1_{wt} := \frac{4}{\pi} \cdot \sum_{n} \frac{1}{n} \cdot (\cos(n \cdot \alpha 1 \cdot deg)) \cdot \sin(n \cdot wt \cdot deg)$$

$$ud2_{wt} := \frac{4}{\pi} \cdot \sum_{n} \frac{1}{n} \cdot (\cos(n \cdot \alpha 2 \cdot deg)) \cdot \sin(n \cdot wt \cdot deg)$$

$$ud3_{wt} := \frac{4}{\pi} \cdot \sum_{n} \frac{1}{n} \cdot (\cos(n \cdot \alpha 3 \cdot deg)) \cdot \sin(n \cdot wt \cdot deg)$$

$$u_{wt} := ud1_{wt} + ud2_{wt} + ud3_{wt}$$



Total Harmonic Distortion Calculation

$p := 5, 11 .. 50$ $\qquad$ $q := 7, 13 .. 50$

$$THD1(p) := \left(\frac{1}{p}\cdot\cos(p\cdot\alpha1\cdot deg)\right) + \frac{1}{p}\cdot\cos(p\cdot\alpha2\cdot deg) + \frac{1}{p}\cdot\cos(p\cdot\alpha3\cdot deg)$$

$$THD2(q) := \left(\frac{1}{q}\cdot\cos(q\cdot\alpha1\cdot deg)\right) + \frac{1}{q}\cdot\cos(q\cdot\alpha2\cdot deg) + \frac{1}{q}\cdot\cos(q\cdot\alpha3\cdot deg)$$

$$THD := \frac{\sqrt{\sum_p (THD1(p))^2 + \sum_q (THD2(q))^2}}{\cos(\alpha1\cdot deg) + \cos(\alpha2\cdot deg) + \cos(\alpha3\cdot deg)}$$

$THD = 0.059$

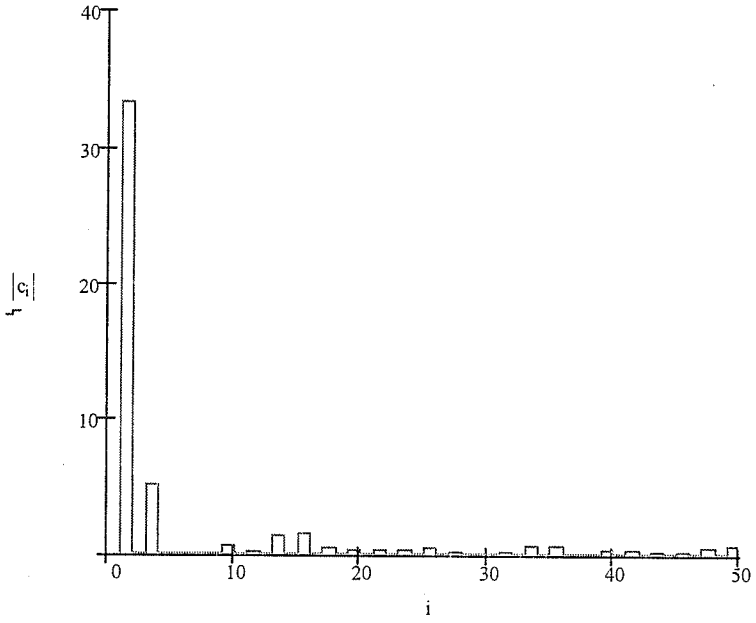
$i := 0 .. 50$

$$F(u) := \frac{2j}{\sqrt{512}}\cdot(fft(u) - 2j\cdot Im(fft(u)))$$

$$H1(p) := \frac{4}{\pi}\cdot|THD1(p)|$$

$c := cfft(u)$

Harmonic Spectra



SH-PWM Technique for 7-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 511$ $m := 1$ $k := 9$

$$c(t,k) := \frac{-1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

$c1(t,k) := 1.5 + c(k,t)$

$c5(t,k) := 2.5 + c(k,t)$

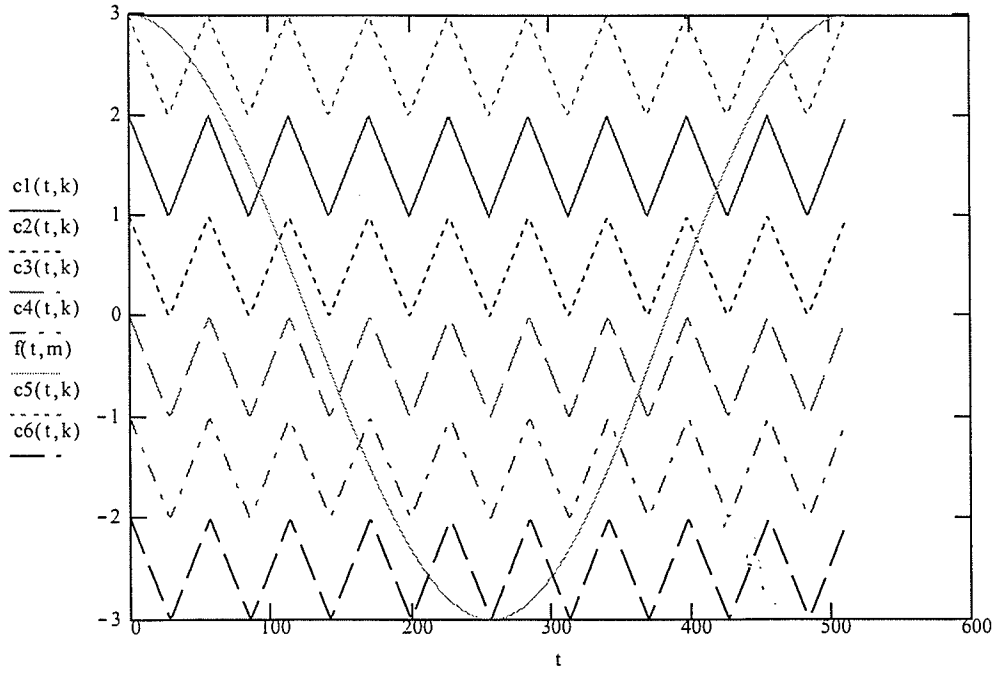
$c2(t,k) := .5 + c(k,t)$

$c3(t,k) := -0.5 + c(k,t)$

$c4(t,k) := -1.5 + c(k,t)$

$c6(t,k) := -2.5 + c(k,t)$

$f(t,m) := 3 \cdot m \cdot \cos(\omega \cdot t)$



$$u1(t,k,m) := -\left(\Phi(c1(t,k) - f(t,m)) - 1\right)$$

$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

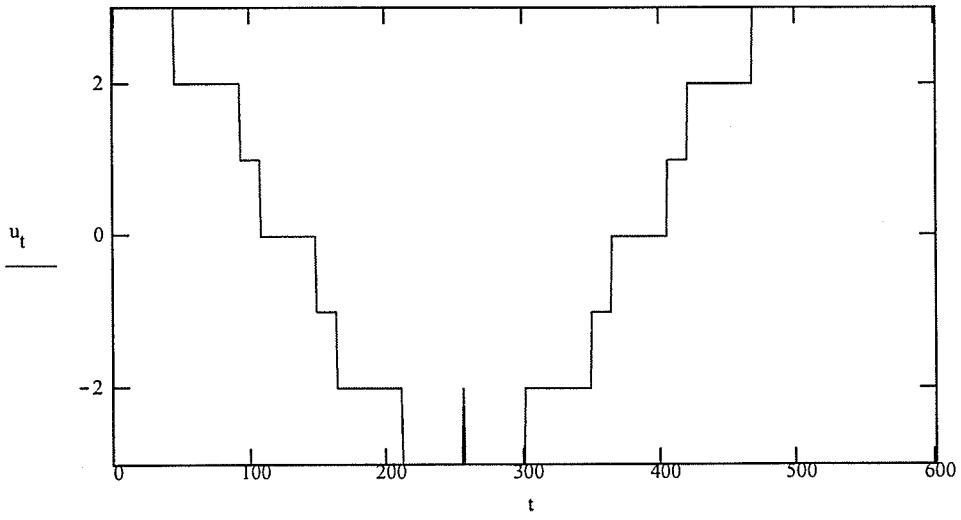
$$u5(t,k,m) := -\left(\Phi(c5(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \left(\Phi(f(t,m) - c4(t,k))\right) - 1$$

$$u6(t,k,m) := \left(\Phi(f(t,m) - c6(t,k))\right) -$$

$$u_t := ((((u1(t,k,m) + u2(t,k,m)) + u5(t,k,m)) + u6(t,k,m) + u4(t,k,m)) + u3(t,k,m))$$



Total Harmonic Distortion

$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (fft(u) - 2 \cdot i \cdot Im(fft(u)))$$

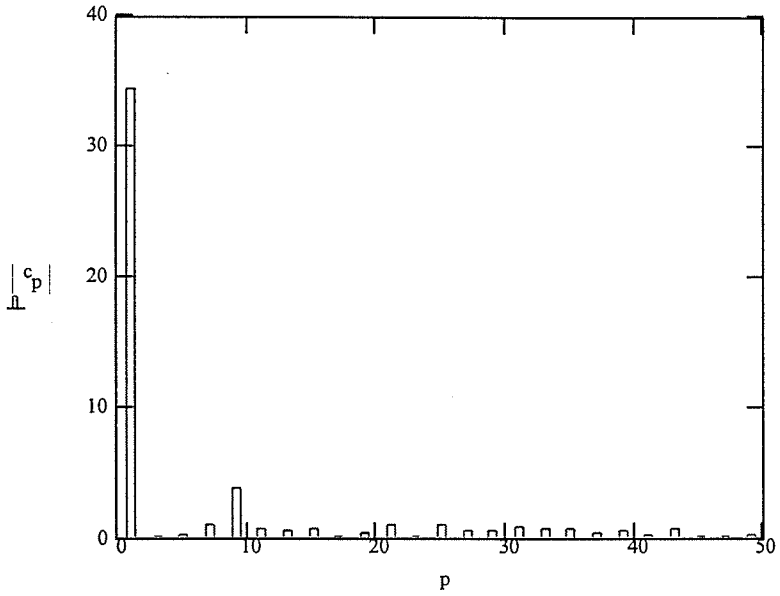
$j := 5, 11 .. 50$ $q := 7, 13 .. 50$

$$DF := \frac{\sqrt{\sum_j \left[\left(\left(\left| F(u)_j \right| \right) \right)^2 \right] + \sum_q \left[\left(\left| F(u)_q \right| \right)^2 \right]}}{\left| F(u)_1 \right|}$$

DF = 0.068

Harmonic Spectra

$c := cfft(u)$



SFO-PWM Technique for 7-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 511$ $m := 1$ $k := 9$ $\beta := 2 \cdot \frac{\pi}{3}$

$$c(t,k) := \frac{1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

$$c1(t,k) := 1.5 + c(k,t)$$

$$c2(t,k) := .5 + c(k,t)$$

$$c3(t,k) := -0.5 + c(k,t)$$

$$c4(t,k) := -1.5 + c(k,t)$$

$$c5(t,k) := 2.5 + c(k,t)$$

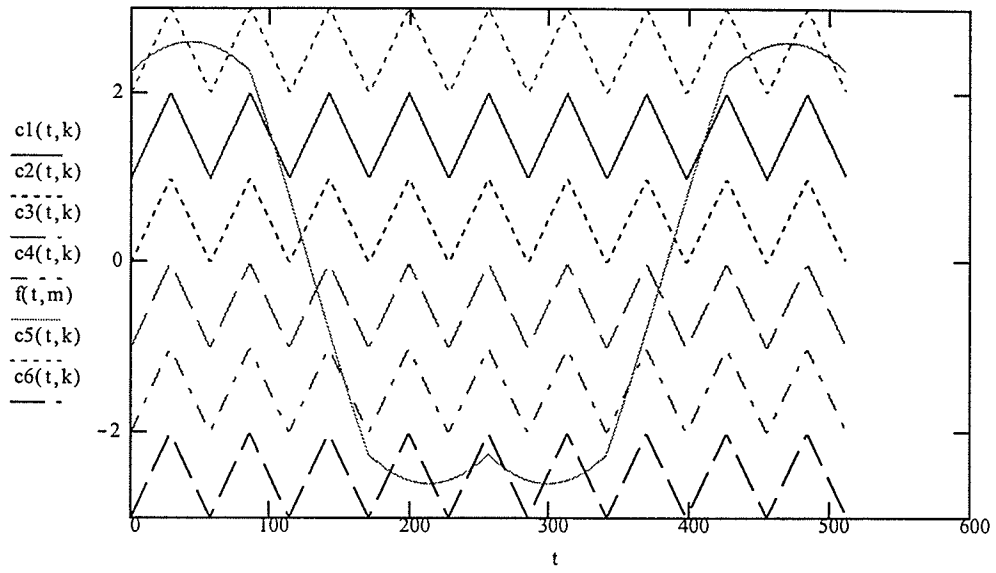
$$c6(t,k) := -2.5 + c(k,t)$$

$$f1(t,m) := 3 \cdot m \cdot \cos(\omega \cdot t)$$

$$f3(t,m) := \begin{bmatrix} 3 \cdot m \cdot \cos(\omega \cdot t) \\ 3 \cdot m \cdot \cos(\omega \cdot t - \beta) \\ 3 \cdot m \cdot \cos(\omega \cdot t + \beta) \end{bmatrix}$$

$$f0(t,m) := \frac{\max(f3(t,m)) + \min(f3(t,m))}{2}$$

$$f(t,m) := f1(t,m) - f0(t,m)$$



$$u1(t,k,m) := -\left(\Phi(c1(t,k) - f(t,m)) - 1\right)$$

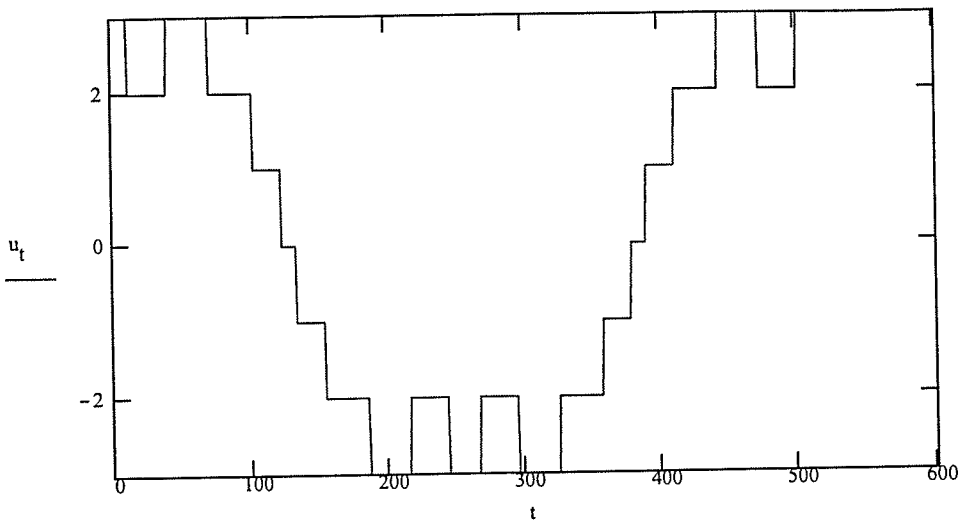
$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

$$u5(t,k,m) := -\left(\Phi(c5(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \left(\Phi(f(t,m) - c4(t,k))\right) - 1 \qquad u6(t,k,m) := \left(\Phi(f(t,m) - c6(t,k))\right) - 1$$

$$u_t := ((((u1(t,k,m) + u2(t,k,m)) + u5(t,k,m)) + u6(t,k,m) + u4(t,k,m)) + u3(t,k,m))$$



$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (\mathrm{fft}(u) - 2 \cdot i \cdot \mathrm{Im}(\mathrm{fft}(u)))$$

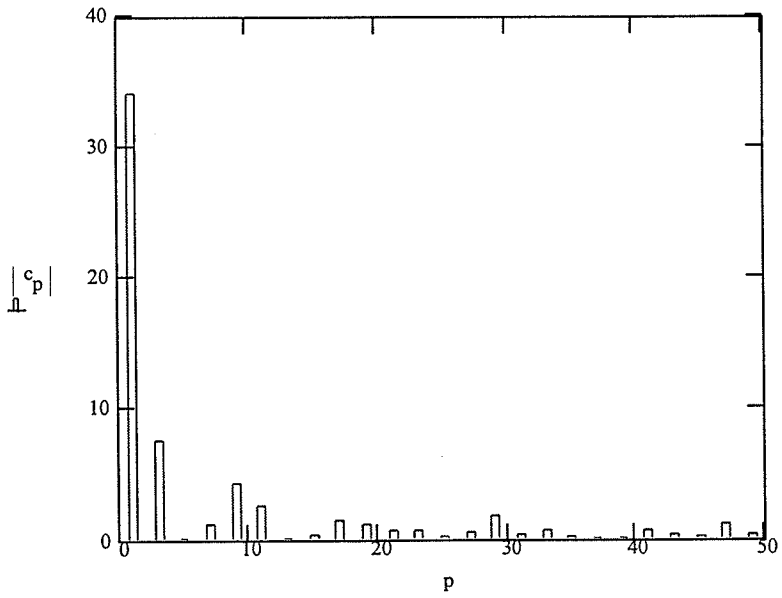
$j := 5, 11 .. 50$ $\qquad$ $q := 7, 13 .. 50$

$$DF := \frac{\sqrt{\sum_j \left[\left(\left| F(u)_j \right| \right)^2 \right] + \sum_q \left[\left| F(u)_q \right|^2 \right]}}{\left| F(u)_1 \right|}$$

$DF = 0.124$

Harmonic Spectra

$c := cfft(u)$



PS-PWM Technique for 5-level Inverter wit M.I=1,and k=9

$\omega := \frac{\pi}{256}$ $t := 0 .. 1022$ $m := 1$ $k := 9$

$$c(t,k) := \frac{-1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$$

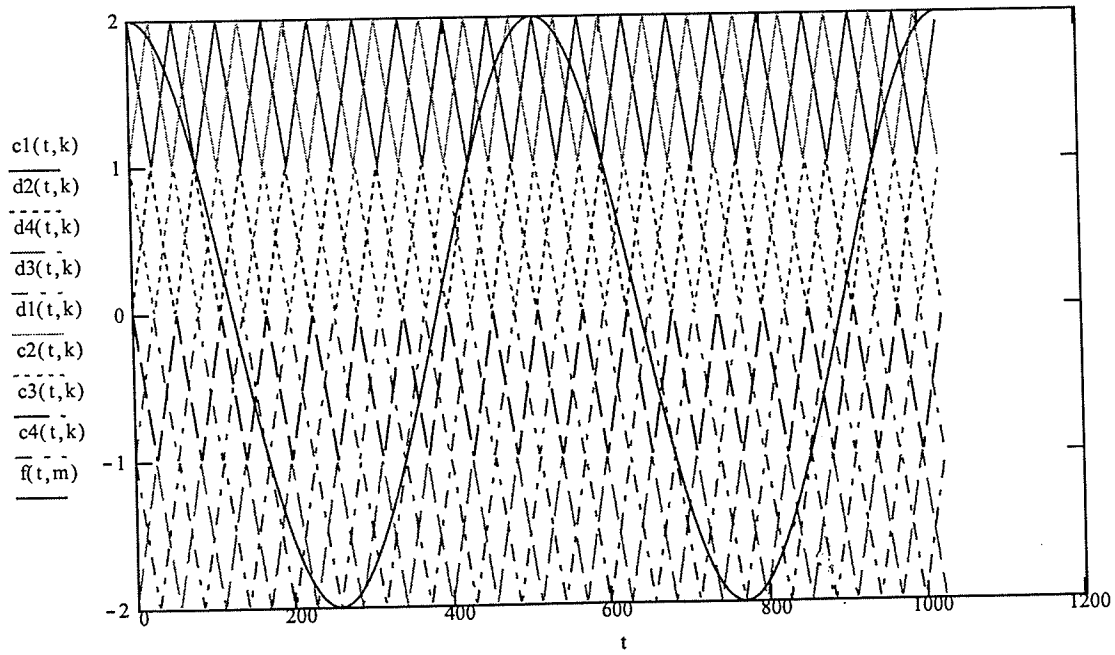
$c1(t,k) := 1.5 + c(k,t)$ $d1(t,k) := c1(k,(t+30))$

$c2(t,k) := .5 + c(k,t)$ $d2(t,k) := c2(k,(t+30))$

$f(t,m) := 2 \cdot m \cdot \cos(\omega \cdot t)$

$c3(t,k) := -0.5 + c(k,t)$ $d3(t,k) := c3(k,(t+30))$

$c4(t,k) := -1.5 + c(k,t)$ $d4(t,k) := c4(k,(t+30))$



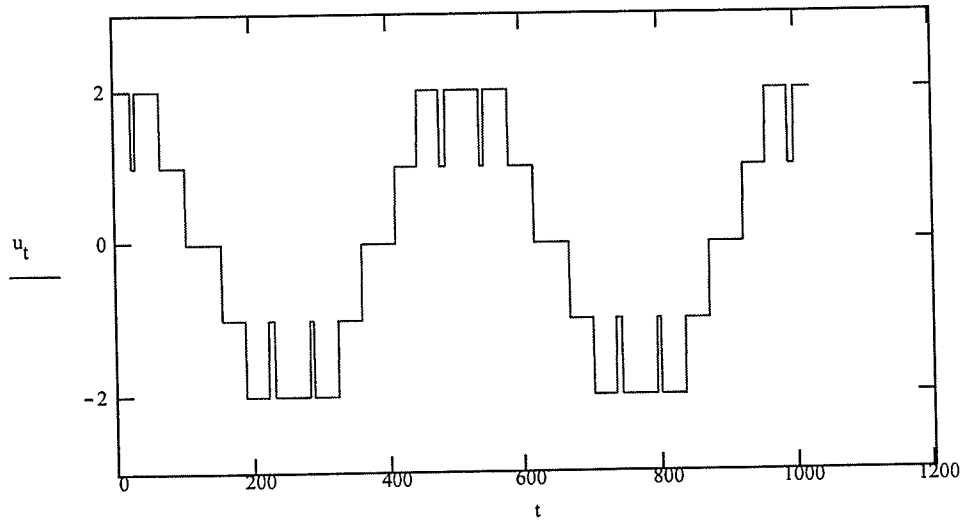
$$u1(t,k,m) := -\left(\Phi(d1(t,k) - f(t,m)) - 1\right) + 1$$

$$u2(t,k,m) := -\left(\Phi(c2(t,k) - f(t,m)) - 1\right)$$

$$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$$

$$u4(t,k,m) := \Phi(f(t,m) - d4(t,k)) - 2$$

$$u_t := (u1(t,k,m) \cdot u2(t,k,m)) - u3(t,k,m) \cdot u4(t,k,m)$$

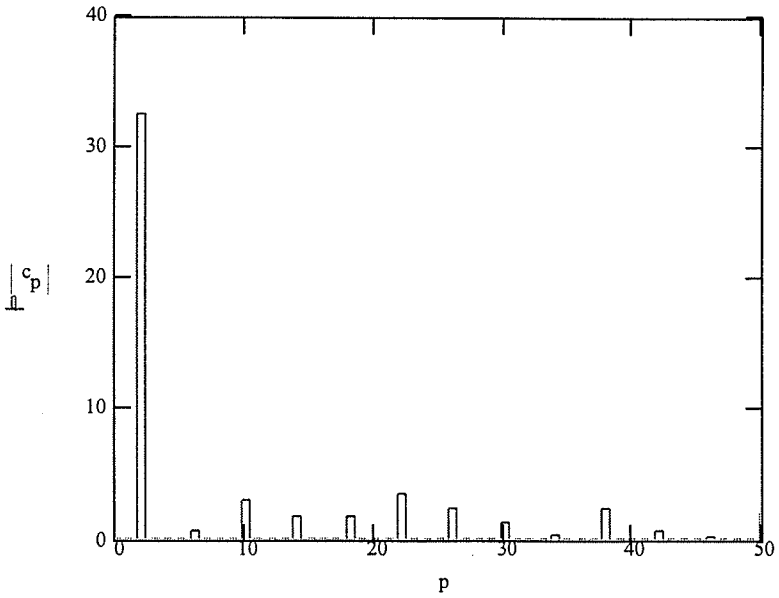


Harmonic Spectra

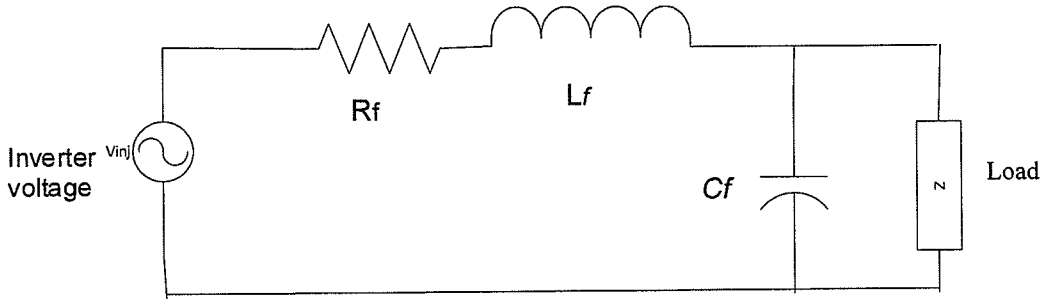
$p := 0 .. 50$

$$F(u) := \frac{2 \cdot i}{\sqrt{512}} \cdot (fft(u) - 2 \cdot i \cdot Im(fft(u)))$$

$c := cfft(u)$



Filter Design for DVR



Single phase equivalent circuit of the proposed DVR

Where the Lf, Cf and the Rf are the filter inductance, the filter capacitor and the equivalent resistance of inverter switches

$$Lf := 2 \cdot 10^{-3}$$

$$Cf := 15 \cdot 10^{-6}$$

$$Rf := 0.5$$

The filter cutoff frequency

$$wf := \frac{1}{\sqrt{Lf \cdot Cf}}$$

$$wf = 5.774 \times 10^{3}$$

The filter cutoff frequency in Hz

$$fc := \frac{wf}{2 \cdot \pi}$$

$$fc = 918.881 \quad Hz$$

The LC filter in ideal controlled DVR system can be regarded as a time delay component with a delay time of

$$time\_delay := \frac{2}{wf}$$

$$time\_delay = 3.464 \times 10^{-4}$$

The filter damping cofficient

$$damp := \frac{Rf}{2} \cdot \sqrt{\frac{Cf}{Lf}} \qquad damp = 0.022$$