# INVESTIGATION OF THE MULTILEVEL GTO INVERTER AS AN ADVANCED STATIC COMPENSATOR

by

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# INVESTIGATION OF THE MULTILEVEL GTO INVERTER AS AN ADVANCED STATIC COMPENSATOR

BY

YIPING ZHUANG

A Thesis/Practicum submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

The author dedicates this work

to the memory of

his father, *Zhuang Aisheng,*

his mother, *Yu Xulan*

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# Abstract

The thesis investigates the possibility of using the multilevel GTO thyristor inverter as an advanced static compensation or STATCOM, in which the design of the five, seven and nine level inverters as well as corresponding switching methods, power loss, dc ripple calculation, harmonic spectrum and control strategies are carefully developed. The basic operation features of the STATCOM is simulated in a simple ac system and the dynamic performance is tested at an HVDC converter terminal when the ac system has a very low short circuit ratio. The results have been compared to other reactive power compensation options available for such applications. These studies are based on an electromagnetic transient simulation program.

Great promise has been shown in the application of the multilevel GTO thyristor inverter as a STATCOM. The main advantage of the multilevel inverter type of design over other current types of STATCOM is that each individual GTO thyristor is clamped to a dc voltage and can be switched independently. Hence a staircase type of output voltage can be obtained and used to reduce the harmonics and the switching losses. An additional merit of the multilevel STATCOM is that the design is able to increase the voltage ratings of the GTO thyristor inverters for the applications of transmission systems without having to use series connections of the GTO thyristors.

The simulation results indicate that the proposed design of the multilevel STATCOM and corresponding control strategies are successful. The nine level STATCOM could be rated ± 92 Mvar at 15 kV using currently available GTO thyristors without using high–pulse number connections. It has been confirmed that the application of the STATCOM in a very weak HVDC system is superior to other reactive power supply options under severe ac and dc disturbances in areas of limiting temporary overvoltages and fault recovery time. These performance benefits lead to the ability to solve specific application problems with smaller equipment ratings and with better stability than with more conventional devices.

# Table of Contents

# List of Figures

# List of Tables

# List of Symbols

Some of the most frequently occurring abbreviators and symbols used in the Thesis are tabulated below. Others are explained where they are used.

$A_c$ ... Peak–to–peak amplitude of the carriers

ac .. Alternating current

$A_m$ . Amplitude of the modulating signal

dc .. Direct current

DF . Distortion factor of harmonics

EMTDC .. Electromagnetic Transient Program for dc systems

F.C. . % of the fundamental component on the basis of that produced by the square wave

$f_c$ ... Frequency of the carriers

FC .. Fixed capacitor

FFS . Fundamental frequency switching

FLI . Five–level GTO thyristor inverter

$f_m$ .. Frequency of the modulation signal

GTO ..... Gate Turn Off thyristor

HVDC ... High voltage direct current

k ... Frequency ratio

kA .. Kiloampere

kg .. Kilogram

kV .. Kilovolt

M .. Modulation index

M–STATCOM . Multilevel GTO thyristor inverter type of STATCOM

Mvar ..... Mega–var

NLI . Nine–level GTO thyristor inverter

PI .. Proportional integral

PLL Phase locked loop

PWM .... Pulse width modulation

rms . Root–mean–square

SC .. Synchronous condenser

SCR ..... Short circuit ratio

SFO–PWM .... Switching frequency optimal PWM

SH–PWM . Subharmonic PWM

SLI . Seven–level GTO thyristor inverter

S.No. .... Number of the GTO thyristor switched per fundamental cycle

STATCOM .... Voltage source inverter type of the var compensator

SVC ..... Static var compensator

TCR ..... Thyristor controlled reactor

TOV ..... Temporary overvoltage

TSC Thyristor switched capacitor

var . Volt–ampere reactive

VCO ..... Voltage controlled oscillator

VSI . Voltage Source Inverter

$\mu$F .. Micro farad

$\omega$ ... System frequency

# *Chapter 1*
# Introduction

## 1.1 BACKGROUND

It is known that the static var compensator ( SVC ) can increase the utilization of existing transmission systems by providing controlled reactive power to enhance the operating flexibility of the power system under normal conditions and improve significantly its dynamic behavior during severe voltage variations and transients. Worldwide, there is a steady increase in the number of installations [1].

The traditional static var compensators use either banks of shunt connected capacitors or thyristor–switched capacitors with thyristor–controlled reactors to provide the needed controlled shunt reactive power compensation. A simplified diagram of a fixed capacitor/thyristor control reactor ( FC/TCR ) type is shown in Figure 1.1 . In such installations, ac capacitors are used as the reactive power source, and shunt connected controlled reactors are used to absorb reactive power. The disadvantages of the SVC here are [2] :

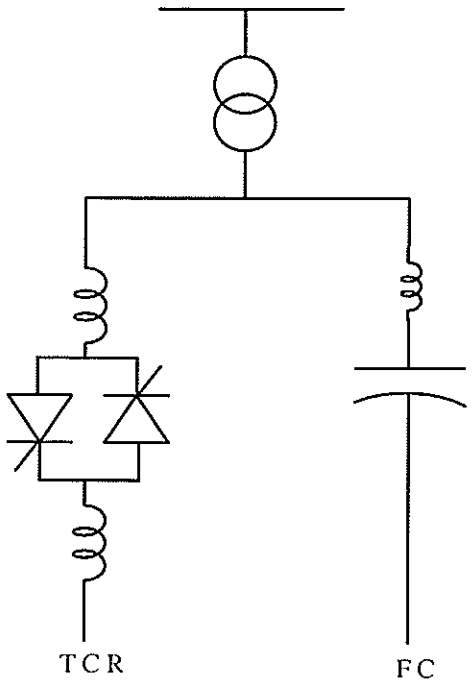



*Figure 1 .1 : A Simplified Diagram of FC/TCR SVC*

1. The ac reactors have a large diameter ( up to 4 meter ) and are rather heavy ( up to 15,000 kg ).

2. The ac capacitor banks consist of capacitor units in parallel. Therefore, particular care must be exercised to ensure proper separation between capacitor groups in the event of an external flashover.

3. Due to their physical size and other considerations, the reactor and the capacitor banks are mounted outdoors, in the switchyard. Their insulation system must withstand harsh environmental conditions.

For these reasons, the traditional static var compensators form quite a large system, requiring considerable equipment at significant cost. This may limit their application in densely populated areas where severe environmental restrictions are imposed. Thus, an advanced static var compensator or STATCOM, in which both the generation and control of reactive power are accomplished by solid–state means, without the use of large ac capacitor and/or reactor banks, has been realized and studied [3–6]. Several candidate schemes of this kind of STATCOM have been implemented using various power electronic switching

inverter configurations with the use of new gate turn–off ( GTO ) thyristors [5–10]. These inverters are operated as either voltage or current sources and they produce reactive power essentially by circulating energy among the phases of the ac system.

Figures 1 .2 and 1 .3 show the basic 6–pulse bridge current source inverter and voltage source inverter. The dc supply of the current source inverter is supposed to be an ideal current source which, in practice, is a regulated rectifier with filters and sufficient inductance. On the ac side there are normally capacitors across the inverter output terminals to absorb the energy released from the inductance because there is a period during switching current from one phase to another which causes high stress on the outgoing valve due to the source inductance in the circuit. By contrast, in the voltage type inverter, there must be a dc capacitor across the inverter input and a free–wheeling diode connected in parallel with each GTO thyristor valve. Comparing the current source inverter with the voltage source inverter, the former requires the power device with a symmetrical bidirectional voltage blocking capability, while the later requires only unidirectional voltage blocking. The availability of a fully–controlled power device with a symmetrical bidirectional blocking capability in the power range required is limited in practice. Therefore, the voltage source inverter using GTO thyristors as the STATCOM has found wide application in this field.

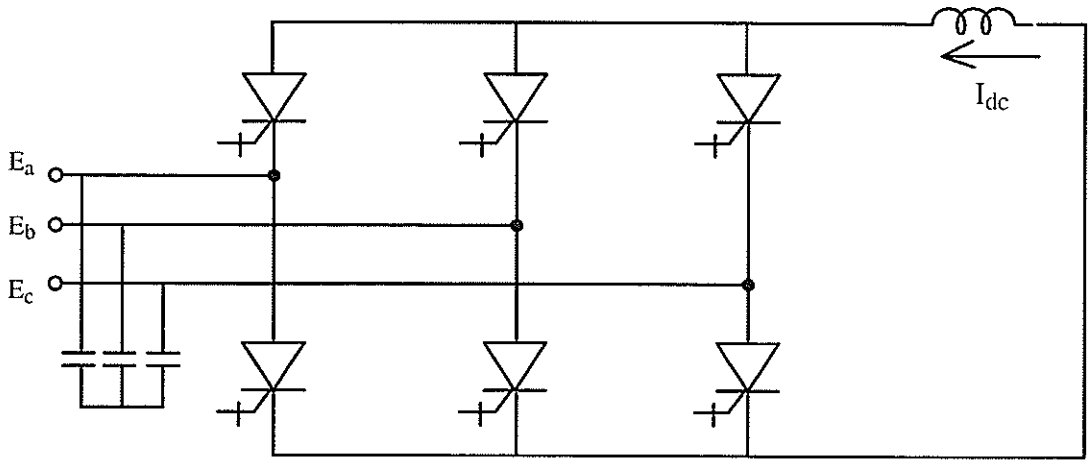



*Figure 1 .2 : A Basic 6–pulse Bridge Current Source Inverter*

In normal operation, a 6–pulse bridge voltage source inverter with a charged dc capacitor will give a balanced set of three quasi–square waveforms of the voltages at the output terminal, which is shown in Figure 1 .4 . The magnitude of these square waves depends on the dc voltage, and the width can be controlled by the firing angles.

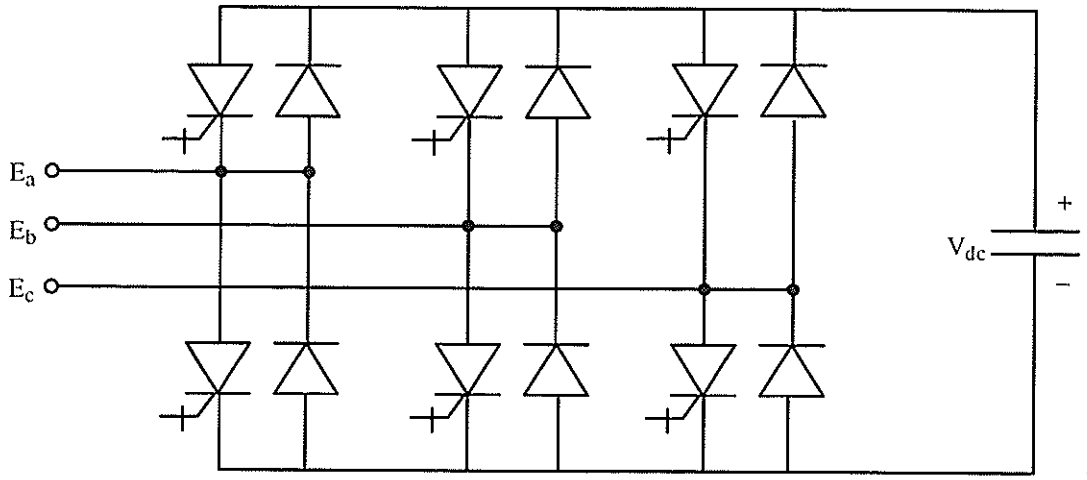



*Figure 1 .3 : A Basic 6–pulse Bridge Voltage Source Inverter*

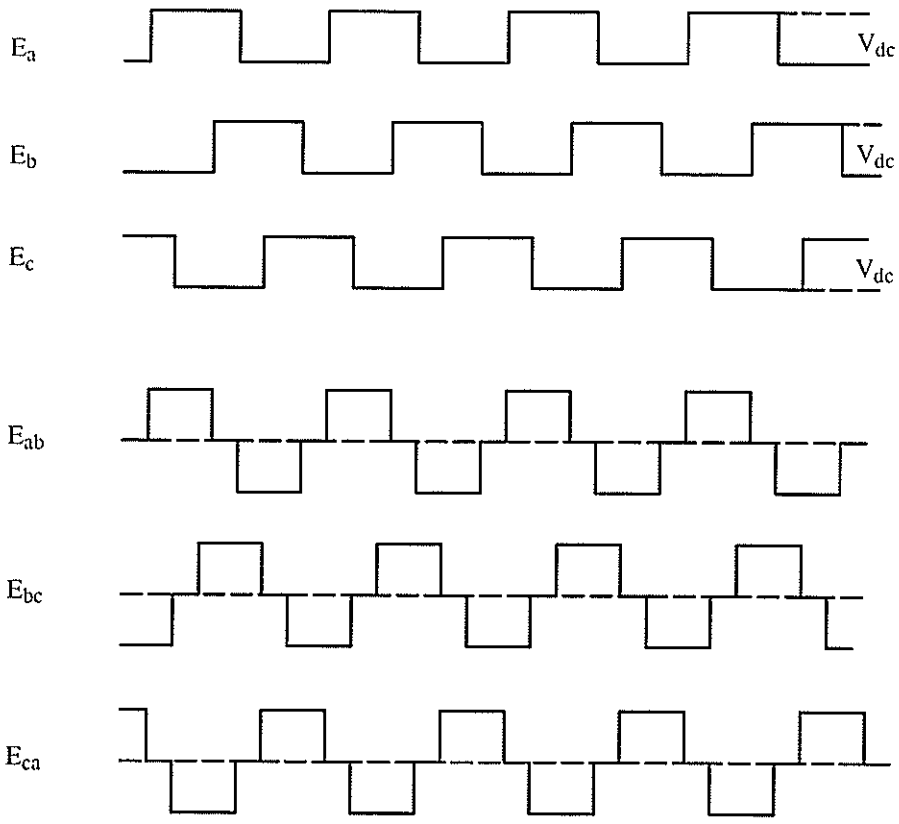



*Figure 1 .4 : Output Voltages of the STATCOM*

The advantages of the STATCOM design over the traditional fixed capacitor/ thyristor controlled reactor ( FC/TCR ) or thyristor switched capacitor / thyristor controlled reactor ( TSC/TCR ) type design are :

a. The voltage source design is more compact and requires a small coupling reactance, usually the ac system transformer leakage and a single dc capacitor about one–eighth of the size of the capacitor in a SVC of the same rating [5]. This leads to a significant reduction in equipment size and installation cost.

b. The design offers a fast continuous variation of reactive output power from capacitive to inductive, and a more effective reactive power generation during undervoltages. This ability to support the system voltage is much better than that obtained with a conventional SVC because the current in the capacitors falls in proportion to the voltage. The improvement in var output of the STATCOM under undervoltage conditions is illustrated in Figure 1 .5 .

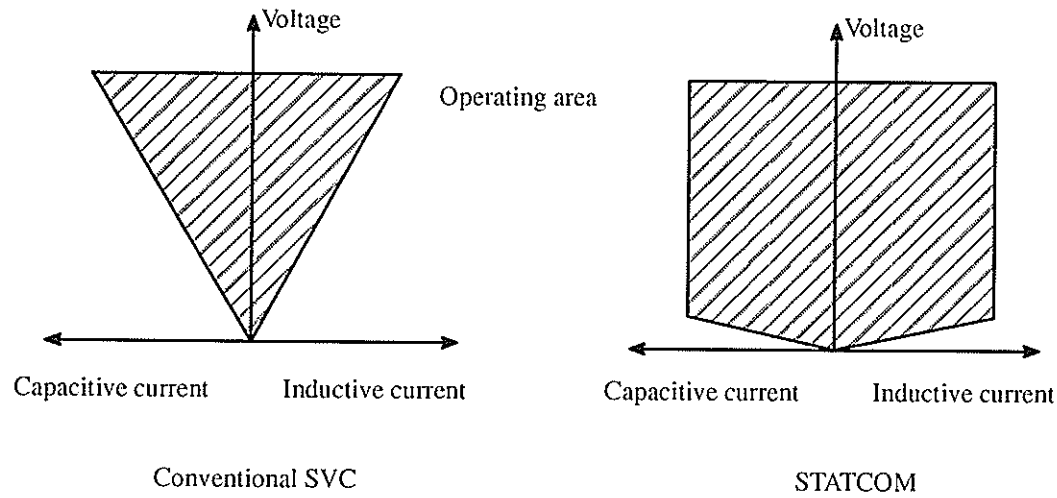



*Figure 1 .5 : Comparison of VAR Output between Conventional SVC and STATCOM*

c. Better control stability [11] which translates to superior performance during major transients and, ultimately, increased system transient stability and improved damping.

However, many design considerations lie in the path of the development of the STATCOM, such as system configuration, series connection technology of the

large–capacity GTO thyristors during turn–off, control of the switching losses and harmonic distortion, and high power ratings for utility applications. The present solution relies on a higher pulse number connection ( two or more basic 6–pulse bridge inverters need to be combined by use of special transformers ) or pulse width modulation.

For this reason, a new type of inverter arrangement used for the STATCOM using multilevel GTO thyristor inverter type of STATCOM, or simply called M–STATCOM is studied in this thesis, which will offer an interesting alternative to other circuit topologies being considered for the STATCOM.

## 1 .2 PRINCIPLES OF THE STATCOM

The basic principle of the STATCOM is similar to the operating principle of the conventional rotating synchronous condenser. The equivalent circuit and vector diagram of the synchronous condenser are shown in Figure 1.6. By varying the magnitude of the exciting, or field, current, both the amount and direction of the reactive power produced by the synchronous condenser can be changed. That is, if the excitation current is increased up to such level that the amplitude of the internal voltage of the synchronous condenser is higher than the voltage of the equivalent ac system ( E>U ), then the current flows through the synchronous reactance and winding resistance from the synchronous condenser to the ac system, and the synchronous condenser generates reactive power for the ac system (capacitive). If the excitation current is decreased to a level such that the amplitude of the internal voltage of the synchronous condenser is lower than the voltage of the equivalent ac system ( E<U ), then the current flows through the reactance and resistance from the ac system to the synchronous condenser,and the synchronous condenser absorbs reactive power from the ac system (inductive). If the amplitude of the internal voltage of the synchronous condenser is equal to the voltage of the equivalent ac system ( E=U ), the reactive power exchange is zero.

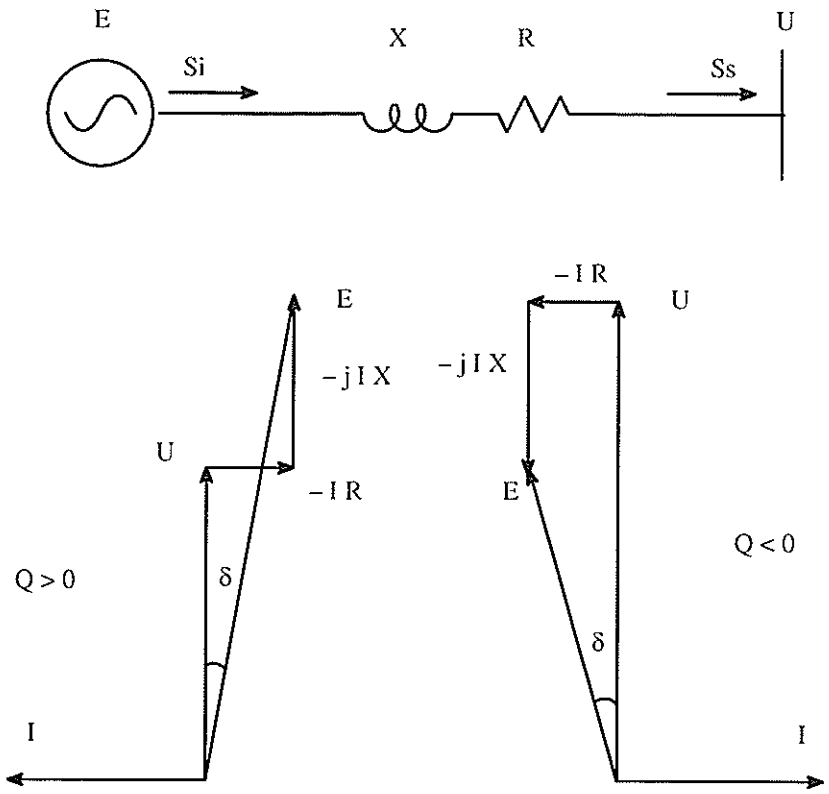



*Figure 1 .6 : A Equivalent Circuit and Vector Diagram of the Synchronous Condenser*

According to this principle, the STATCOM is designed. Figure 1 .7 shows a simplified equivalent circuit of the STATCOM, in which E represents the output voltage of the GTO thyristor inverter.

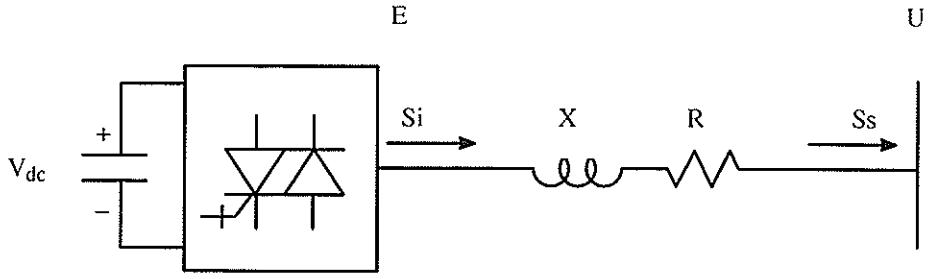



*Figure 1 .7 : A Simplified Equivalent Circuit of STATCOM*

In this configuration, the GTO thyristor inverter converts a dc voltage into a three–phase ac voltage ( E ) which is synchronized with, and connected to, the ac system

through a small tie reactance (X) and a resistance (R), which usually is the leakage reactance of a transformer and the equivalent losses of the circuit. When the inverter's output voltage is higher than the ac system's voltage, a leading reactive current is drawn from the system ( vars are generated ). When the the inverter output voltage is lower than the ac system voltage, lagging reactive current is drawn from the system ( vars are absorbed ). When the inverter's output voltage is equal to the ac system's voltage, the reactive power exchange is zero. From this point of view, the STATCOM is an electronic equivalent of the conventional rotating synchronous condenser. The difference being that the reactive power output of the STATCOM is controlled by varying the magnitude of the inverter output voltage rather than by varying the excitation current. One way to change the magnitude of the inverter output voltage is to change the dc capacitor voltage. This can be achieved by making the output voltage of the inverter lag or lead the system voltage by a small angle. For example, when the inverter output voltage lags the system voltage, the inverter will absorb a small amount of real power from the ac system to charge dc capacitor and keep the capacitor voltage at the desired level and vice versa. Thus, we could say that a function of the dc capacitor is to establish an energy balance between the input and output during the dynamic changes of the var output.

## 1 .3 DESCRIPTION OF THE MULTI LEVEL GTO INVERTER

The multilevel inverter used for high power drive applications has been investigated [12–16]. Recent studies have shown that multilevel GTO thyristor inverters for drive applications can increase the output voltage and decrease the effect of harmonics, but at the expense of individual dc supplies to each voltage level of the inverter [17]. However, the STATCOM does not require a separate dc supply and this makes the multilevel GTO thyristor inverter ideally suited to this application.

A generalized structure of one pole ( or phase ) for an N–level GTO thyristor inverter (N odd) is shown in Figure 1 .8 , where $N' = (N-1)/2$. Two additional poles would be

required for the three phase inverter, with the dc capacitors common to all poles.A similar structure can be realized with N even.

The advantages of such a structure is that the problem of series connection of GTO thyristors has been avoided, because the thyristor need only block the voltage of its own level and not the full dc voltage, i.e. GTO thyristor $Q_1$ is only required to block the voltage of $V_{c1}$, $Q_2$ is required to block the voltage of $V_{c2}$, and so on. Furthermore, each GTO thyristor is well protected against overvoltage by the clamping action of the dc capacitors. The lower group of GTO thyristors requires the complementary gating pulses of the upper group of the same number. That is if $Q_2$ is on, then $Q_2'$ must be off. It should be mentioned that, for each voltage step, only one thyristor must turn on and one thyristor turn off. For example, if $Q_1$ is off, then $Q_2$, $Q_3$, ... $Q_{N-1}$ and $Q_1'$ are on, and the terminal + (N'–1)E is connected to the output terminal through $DP_1$, $Q_2$, $Q_3$, ... $Q_{N-1}$ for positive current, or through $Q_1'$ and $DN_1$ for negative currents. In order to obtain the various output voltage levels the correct switching logic is necessary, as shown in Table 1 .1 . It should be noted that the clamping diodes are required to block differing voltages, e.g. $DP_1$ must block the voltage of a single dc level, E, while $DP_{N-2}$ must block (N–2)E, and so on.

As explained later in this thesis, the advantages of this design over the current design of the inverter used for the STATCOM are:

a. The voltage level can be increased without series connection of GTO thyristors and the necessity of simultaneous switching. Therefore, the reactive power output of the STATCOM approaches a practical level for utility applications without high–pulse number transformer connections.

b. The harmonic content of the output current can be greatly reduced without the use of harmonic filters and/or high–pulse bridge inverter connections [6],[18] as well as multiple winding transformers [19], and thereby the losses and filter requirements are reduced.

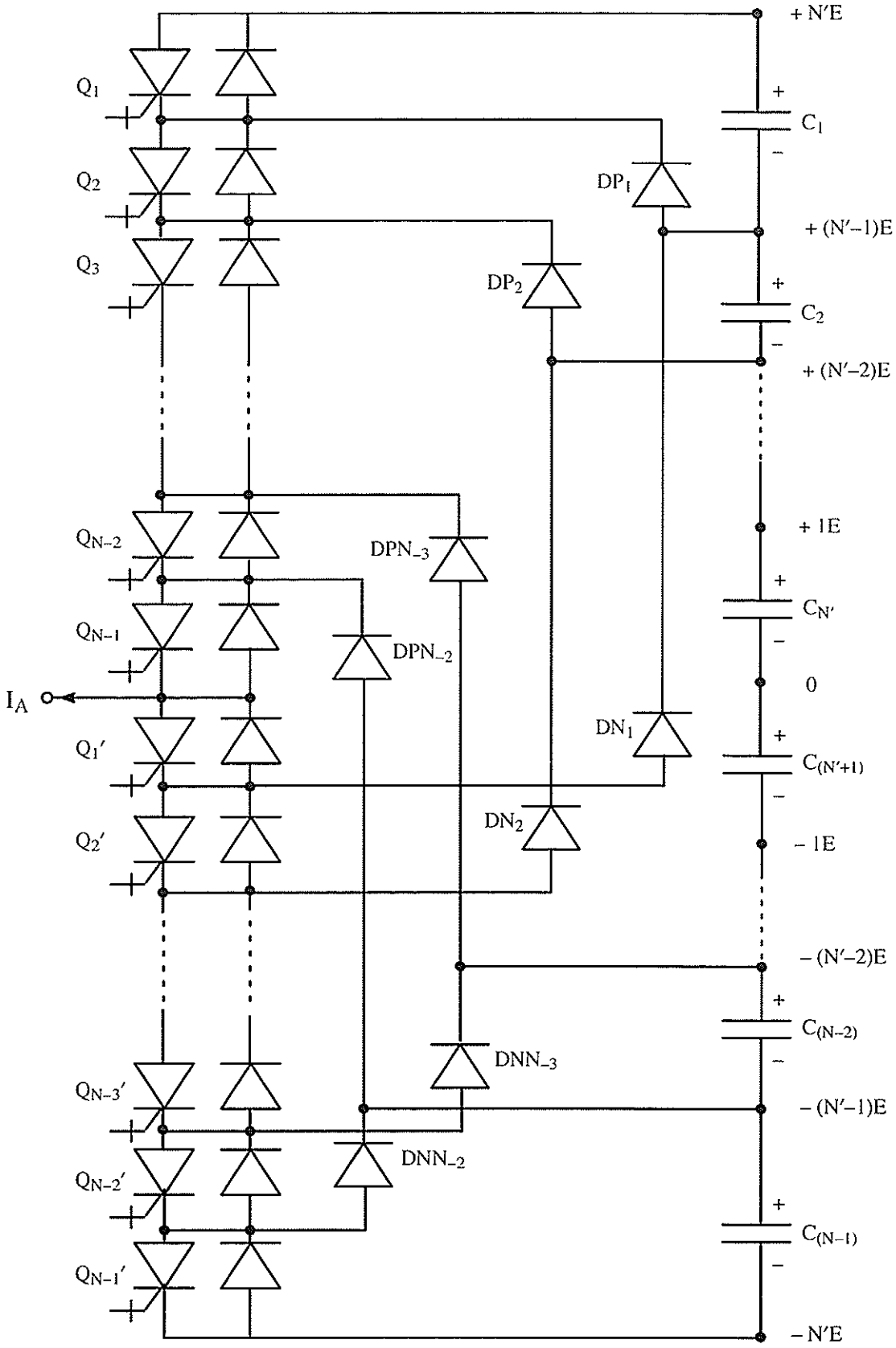



*Figure 1 .8 : One Phase of a Multilevel GTO Inverter*

The multilevel inverter also has advantages over designs which may use a series connection of GTO thyristors by virtue of the fact that the peak current occurs at minimum voltage and vice versa. This means that fewer GTO thyristors will be in series in the M–STATCOM during peak current intervals than in the STATCOM where all GTO thyristors operate together. This should considerably reduce the on state losses as the diodes have a smaller forward voltage drop.

Table 1 .1 : The Switching Logic for M–STATCOM

| Output | GTO Thyristor State | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $Q_1$ | $Q_2$ | ..... | $Q_{N-2}$ | $Q_{N-1}$ | $Q_1'$ | $Q_2'$ | ..... | $Q_{N-2}'$ | $Q_{N-1}'$ |
| N'E | 1 | 1 | ..... | 1 | 1 | 0 | 0 | ..... | 0 | 0 |
| (N'–1)E | 0 | 1 | ..... | 1 | 1 | 1 | 0 | ..... | 0 | 0 |
| . . . | . . . | . . . | ..... ..... ..... | . . . | . . . | . . . | . . . | ..... ..... ..... | . . . | . . . |
| E | 0 | 0 | ..... | 1 | 1 | 1 | 1 | ..... | 0 | 0 |
| 0 | 0 | 0 | ..... | 1 | 1 | 1 | 1 | ..... | 0 | 0 |
| –E | 0 | 0 | ..... | 1 | 1 | 1 | 1 | ..... | 0 | 0 |
| . . . | . . . | . . . | ..... ..... ..... | . . . | . . . | . . . | . . . | ..... ..... ..... | . . . | . . . |
| –(N'–1)E | 0 | 0 | ..... | 0 | 1 | 1 | 1 | ..... | 1 | 0 |
| –N'E | 0 | 0 | ..... | 0 | 0 | 1 | 1 | ..... | 1 | 1 |

## 1 .4 SCOPE OF THE THESIS

The study was organized into the following sections:

### 1 .4 .1 INVESTIGATION OF THE SWITCHING METHODS

Starting with the five level inverter, both the fundamental frequency switching (FFS) and pulse width modulation (PWM) techniques will be studied to determine which switching method is best. Points to be examined are:

a. FFS method.

b. PWM techniques.

c. Types of carrier and modulation waveforms.

d. Harmonic distortion and ratings.

### 1.4.2 EXPANSION TO HIGHER LEVEL INVERTERS

Expansion of the above procedure to higher level inverters in order to optimize, on the basis of filter requirements and operating losses, the voltage level and operation will include:

a. Seven level GTO inverter;

b. Nine level GTO inverter;

c. A comparison of 5, 7 and 9 level inverters;

d. Ratings of the M–STATCOM.

### 1.4.3 POWER LOSSES

The method to analyze and calculate power losses (including on–state losses, off–state losses, switching transient losses, and the snubber circuit losses) in the M–STATCOM will be presented based on the selected switching technique.

### 1.4.4 EFFECT OF DC CAPACITOR SIZE ON THE STATCOM

Establishing of the relationship between the dc capacitor and the ripple current, which will be focused on how the dc capacitor size affects the harmonic content of the inverter output voltage.

### 1.4.5 CONTROL STRATEGY STUDY

Development of suitable control strategies which will be aimed at:

a. Maintaining individual capacitor voltages at desired levels.

b. Realizing the reactive current output control.

c. Obtaining excellent dynamic performances with high control stability.

### 1.4.6 DIGITAL SIMULATION

Based on the above results, a M–STATCOM inverter will be simulated using the EMTDC$^{TM}$ package to study the operation of the design during the following conditions:

a. Start–up of the inverter with and without pre–charging equipment.

b. Steady–state operation of the M–STATCOM with the selected switching method and unbalanced dc capacitors.

c. Dynamic performance of the M–STATCOM under fault conditions.

d. Factors affecting the behavior of the M–STATCOM.

e. Comparisons with existing reactive power compensators.

# *Chapter 2*
# Analysis of a five–level inverter

## 2.1 BASIC SCHEME

Figure 2.1 shows a three–phase arrangement of the five–level GTO thyristor inverter used as a STATCOM, in which the ac system is connected through a wye/delta transformer to the inverter. The transformer provides the required isolation voltage to match the inverter's output. The gate switching logic to achieve the five voltage levels at the output terminal of this five level GTO thyristor inverter are shown in Table 2.1 . As mentioned above, for each voltage step only one thyristor must turn on and one thyristor turn off.

## 2.2 FUNDAMENTAL FREQUENCY SWITCHING ( FFS ) OF GTO'S

Using the fundamental frequency switching ( FFS ) method [17], each GTO thyristor is switched on and off only once during a power frequency ( 60 Hz ) cycle.

As is described in the preceding sections, taking one single phase into account, the five voltage levels could be achieved at the output terminal if the gate logic in Table 2.1 is followed.

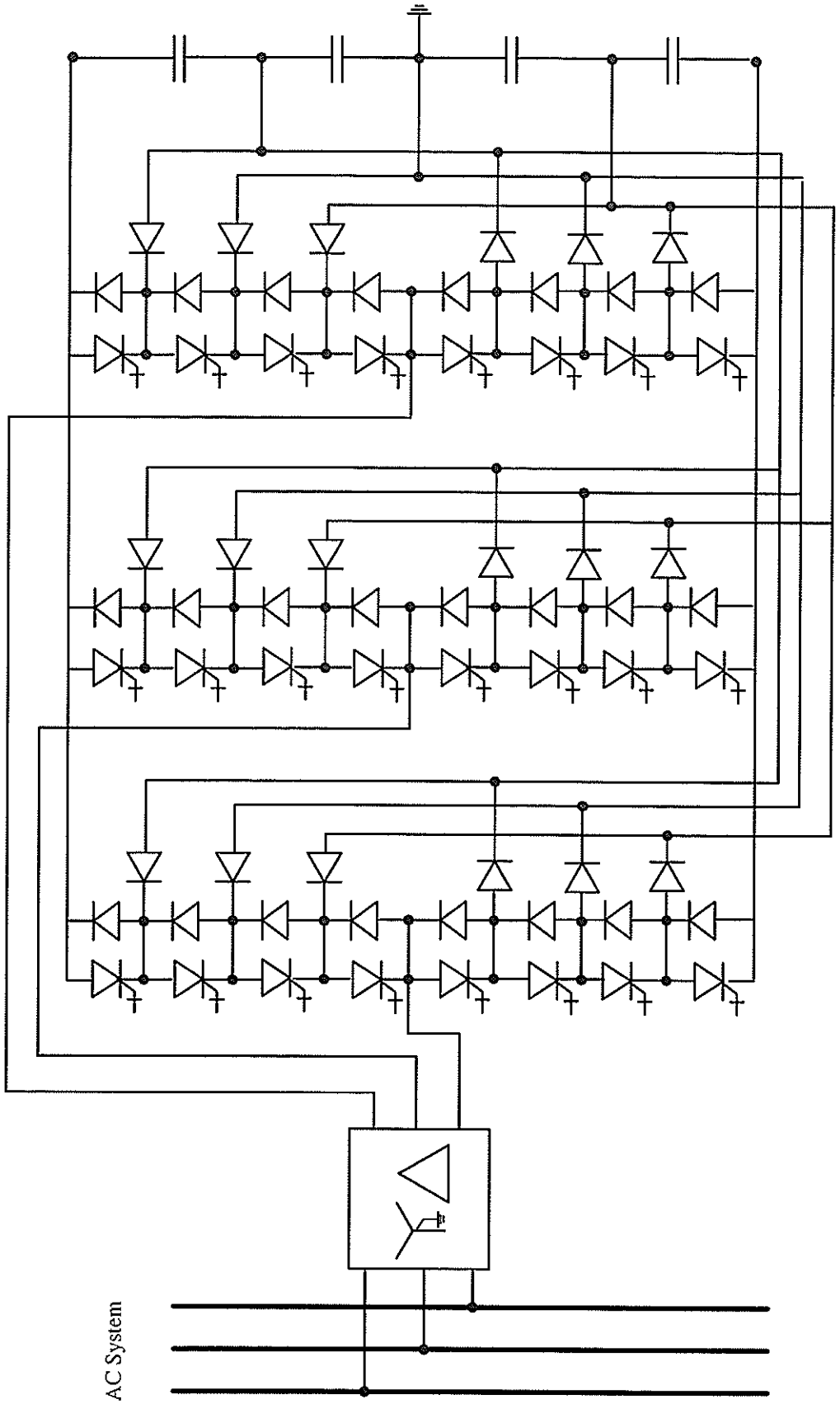



*Figure 2 .1 : A Three Phase Arrangement of a Five Level GTO Inverter*

Table 2 .1 : The Gate Logic for Five–level GTO Inverter

| Output ( $E_a$ ) | The state of GTO thyristors | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_{1'}$ | $Q_{2'}$ | $Q_{3'}$ | $Q_{4'}$ |
| $+V_{c1}+V_{c2}$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $+V_{c2}$ | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| *0* | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| $-V_{c3}$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| $-V_{c3}-V_{c4}$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

The voltage across each capacitor, as explained later, could be either identical or different depending on each capacitor value and the individual control. However, to make things easy we may simply select the same size capacitor for each level, and maintain the voltage across each capacitor at the identical value by means of the specific control loop. In this case, we have $V_{c1} = V_{c2} = V_{c3} = V_{c4} = V_c$. If we switch to an intermediate voltage $V_c$ at $\alpha_1$, and switch to a full voltage $E = V_{c1} + V_{c2} = 2V_c$ at $\alpha_2$, a stepped output voltage of the five level inverter as shown in Figure 2 .2 is achieved, which is a simple sum of the two rectangular waveforms.

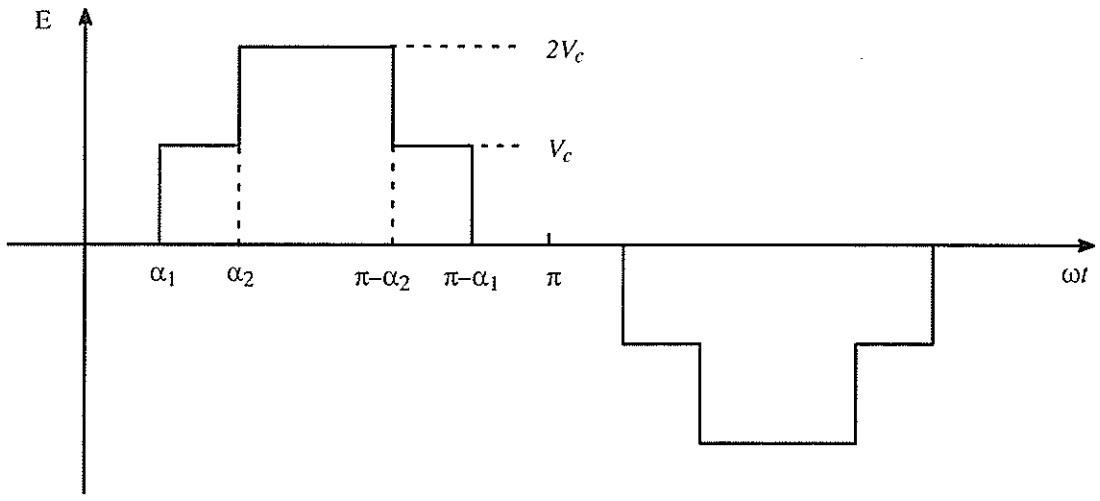



*Figure 2 .2 : A Stepped Output Voltage of the FLI*

Performing the Fourier Transform for this waveform, we get :

$$E(\omega t) = V_c(\alpha_1, \omega t) + V_c(\alpha_2, \omega t) \qquad (2.1)$$

$$= V_c \frac{4}{\pi} \sum_n \frac{1}{n} \sin \frac{n\pi}{2} \sin\left(\frac{n\pi}{2} - n\alpha_1\right) \sin(n\omega t)$$

$$+ V_c \frac{4}{\pi} \sum_n \frac{1}{n} \sin \frac{n\pi}{2} \sin\left(\frac{n\pi}{2} - n\alpha_2\right) \sin(n\omega t)$$

$$= V_c \frac{4}{\pi} \sum_n \frac{1}{n} [\cos(n\alpha_1) + \cos(n\alpha_2)] \sin(n\omega t)$$

where n = 1 , 3 , 5 , 7 , .....

From the formula ( 2 .1 ) , we can obtain the magnitude of the Fourier coefficients as follows ( which is equal to the magnitude of the nth harmonic normalized to $V_c$ ) :

$$H(n) = \frac{4}{\pi} \frac{1}{n} [\cos(n\alpha_1) + \cos(n\alpha_2)] \qquad (2.2)$$

where n = 1 , 3 , 5 , 7 , .....

It should be mentioned that the $\alpha_1$ and $\alpha_2$ can be chosen at any angle within the range of $0^0$ to $90^0$, ( $\alpha_1 < \alpha_2$ ), on the basis of getting a lower harmonic content or a larger fundamental voltage. We can therefore switch $\alpha_1$ and $\alpha_2$ at such values that two harmonics will sum to zero. For example, if we wish to cancel the 5th and 7th harmonic , we can simply let the equations from the formula ( 2 .2 ) be :

$$\cos(5\alpha_1) + \cos(5\alpha_2) = 0$$
$$\cos(7\alpha_1) + \cos(7\alpha_2) = 0 \qquad (2.3)$$

Equation ( 2 .3 ) is a non–linear transcendental equation which can be solved by the Newton–Raphson method, to obtain :

$\alpha_1 = 5.14^0$

$\alpha_2 = 30.86^0$

That is to say that if we switch to the voltage $V_c$ at $5.14^0$, and to the voltage $2V_c$ at $30.86^0$ in the positive half cycle of the fundamental, and similarly in the negative half cycle of the fundamental, we switch to the voltage $-V_c$ at $185.14^0$, and to the voltage $-2V_c$ at $210.86^0$, the output voltage of the five level inverter will not contain the 5th harmonic and the 7th harmonic components.

It should be noted that, as shown in the formula ( 2 .2 ), although the 5th harmonic and the 7th harmonic are summed to zero, the fundamental output voltage is also reduced when $\alpha 1 = 5.14^0$ and $\alpha 2 = 30.86^0$, which in this case the magnitude of the fundamental voltage should be :

$$H(1) = \frac{4}{\pi} [\cos(5.14^0) + \cos(30.86^0)] \qquad (2.4)$$
$$= 2.36$$

Fortunately, it is reduced to only 93% of that produced by the square wave ( 2.55 ).

Figure 2 .3 shows the output voltage waveform of the five–level inverter using the FFS method with $\alpha 1 = 5.14^0$ and $\alpha 2 = 30.86^0$, in which two unit height rectangular waveforms are considered.

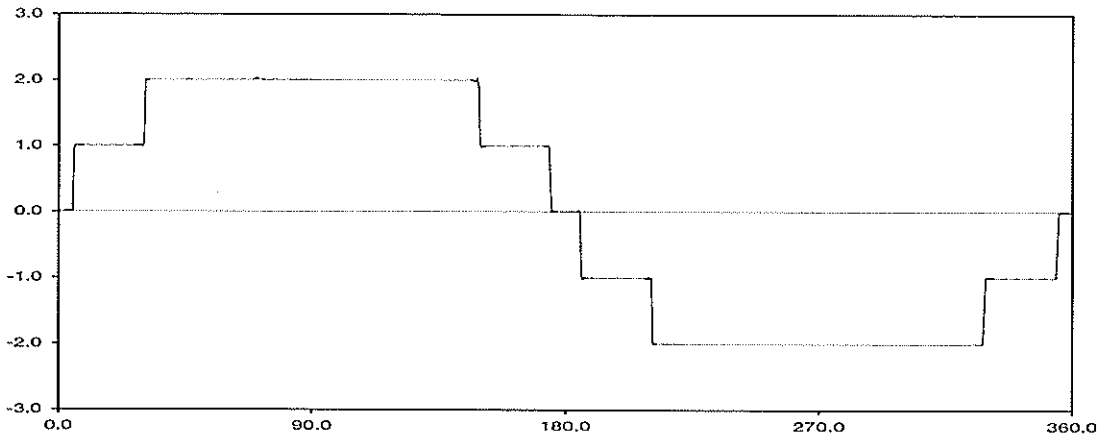



*Figure 2 .3 : The Output Voltage with $\alpha 1 = 5.14^0$ and $\alpha 2 = 30.86^0$*

## 2.3 APPLICATIONS OF THE PWM TECHNIQUES

It is well known that the pulse width modulation ( PWM ) technique has been widely accepted as a good control strategy, because of its simplicity and high ability of harmonic content reduction. A literature review of PWM techniques for multilevel inverters indicates that there are two PWM methods which show better modulation results [17]. One is called the subharmonic PWM ( SH–PWM ) technique presented in [16],[20], the other is called the switching frequency optimal PWM method ( SFO – PWM ) [21].

The control principle of the SH–PWM method is to use several triangular carrier signals keeping only one modulating, sinusoidal signal. For the five level GTO inverter, 4 triangular carriers are needed. ( Generally speaking, if an N–level GTO inverter is employed, N–1 carriers will be needed. ) The carriers have the same frequency, $f_c$, and the same peak–to–peak amplitude, $A_c$, and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency $f_m$ and amplitude $A_m$. Each carrier is compared at every instant with the modulating signal. Each comparison switches the thyristor on if the modulating signal is greater than the triangular carrier assigned to that thyristor. That is, thyristor $Q_1$ is switched by the uppermost carrier and $Q_2$ by the next lower carrier. Obviously, the actual driving signals for the power devices can be derived from the results of the modulating–carrier comparison by means of a logic circuit.

The main parameters of the modulation process are :

a) The frequency ratio $k = f_c/f_m$ , where $f_c$ is the frequency of the carriers, and $f_m$ is the frequency of the modulating signal.

b) The modulation index $M = A_m/(N'A_c)$, where $A_m$ is the amplitude of the modulating signal, $A_c$ is the peak–to–peak amplitude of the carriers, and $N' = (N-1)/2$, where N is the number of the inverter level ( which is odd ).

We have also other degrees of freedom about the dispositions among the triangular carriers, in which there are three very simple cases which seem the most interesting :

1) All the carriers are alternatively in opposition, see Figure 2 .4 .a.

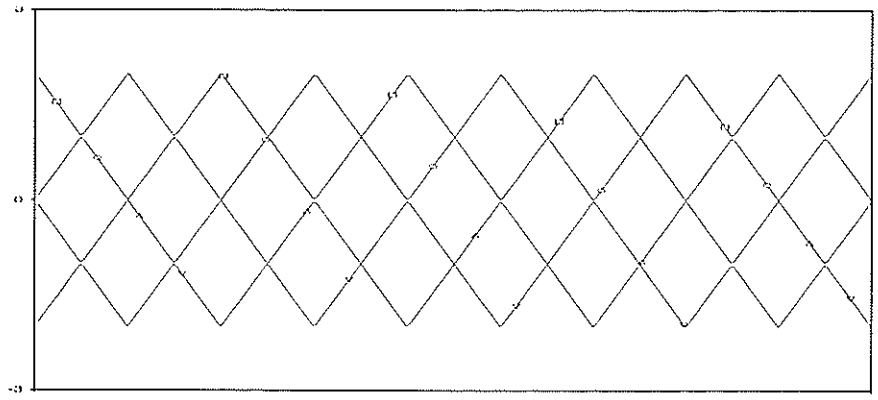


*Figure 2 .4 .a : All the Carriers Are Alternatively in Opposition*

2) All the carriers above the zero reference are in phase among them, but in opposition with those below, see Figure 2 .4 .b.

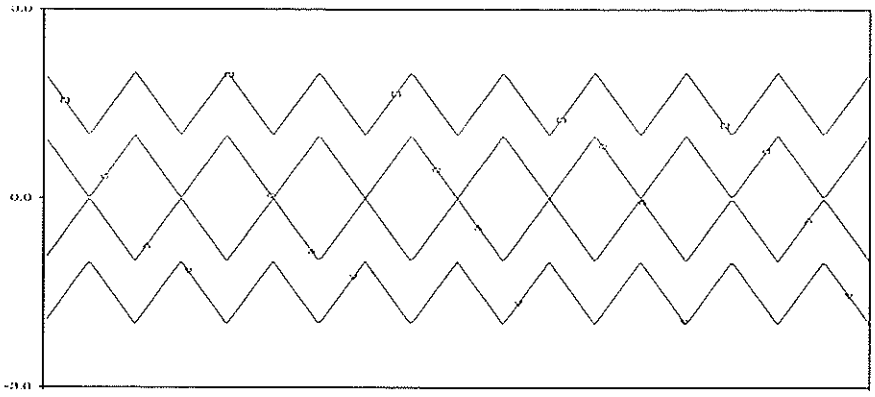


*Figure 2 .4 .b : All the Carriers above Zero Are in Phase, but in Opposition with those below Zero*

3) All the carriers are in phase, see Figure 2 .4 .c.

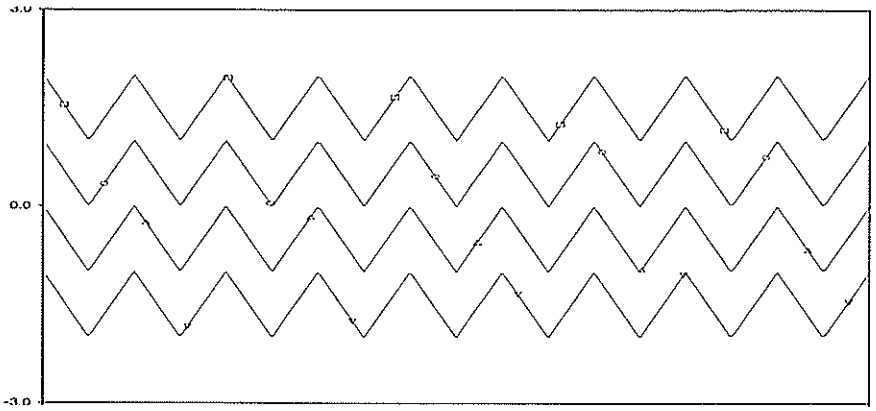


*Figure 2 .4 .c : All the Carriers Are in Phase*

In comparison with above three cases, Carrara et.al. [20] have shown that for Case 1) or 2) no harmonics exist at the carrier frequency but odd order harmonics exist in each sideband. For Case 3) an harmonic exists at the carrier frequency and at odd multiples of it and at even numbered sidebands centered around odd harmonics of the carrier and vice–versa. Although this case gives a higher frequency spectrum in general, in three–phase systems with k being a multiple of three, the harmonics of the carrier frequency are co–phasal and have no effect.

As an example, Figure 2 .5 shows the modulation results using the SH–PWM method for the five level GTO inverter, where, $f_m = 60$ Hz, $k = 9$, $A_c = 1$ and $M = 75\%$.

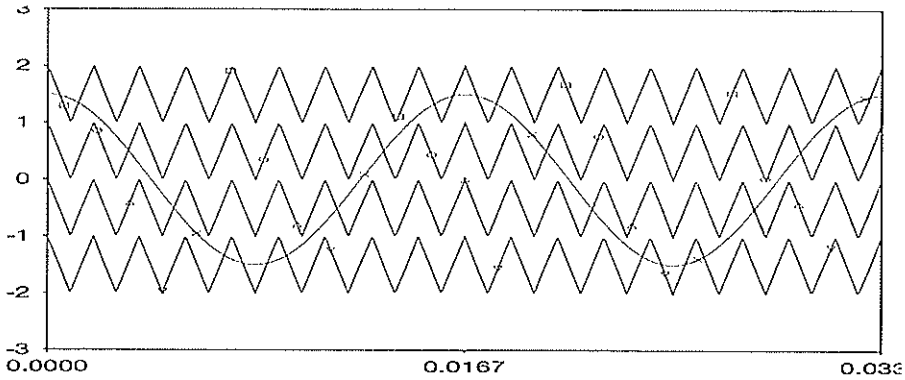



*Figure 2 .5 .a : Carrier and Modulation Waveforms Using SH–PWM*

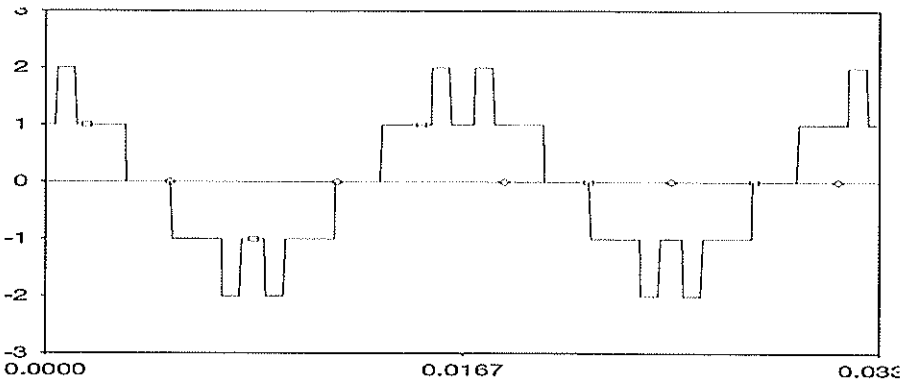



*Figure 2 .5 .b : Output Voltage of the FLI Using SH–PWM*

Besides the things we explained above, in order to get better modulation results, we still have some choices here :

First, the carrier waveform can be chosen in either M–type or W–type [17]. The M–type carrier waveform means the carrier has a minimum at the peak of the modulation signal, while the W–type carrier waveform means the carrier has a maximum at the peak of the modulation signal.

Secondly, when the frequency ratio k and the modulation index M are changed, the frequency and the amplitude of the carriers will be changed, and thereby the modulating results will be different. In other words, the magnitude of the fundamental component and harmonic content in the output voltage of the inverter as well as the switching losses can be controlled by simply changing the k and M.

All of these cases were analyzed further using the Mathcad program. Typical results are tabulated in Table 2 .2 , in which the number of GTO thyristors switched per fundamental cycle (S. No.) and the harmonic distortion factor (DF) were compared for each case.

The harmonic distortion factor was defined as the ratio of the root–mean–square of the harmonic content to the root–mean–square of the fundamental quantity [22], which is expressed as a percent of the fundamental, that is :

$$DF = \left( \frac{\textit{Sum of squares of amplitudes of all harmonics}}{\textit{Square of amplitude of fundamental}} \right)^{1/2} \cdot 100\ \% \qquad (2.5)$$

It should be noted that the disposition of the carriers used here is limited to case 3). That is all four carriers are in phase, because this type of carrier was superior to all other cases in reduction of the harmonic contents which is analytically proven in [20].

To summarize the results of Table 2 .2 , we found :

1. For balanced three–phase operation, the modulation index M = 1 will always give the best results for different frequency ratios.

2. If the frequency ratio k = 9 is chosen, the harmonic distortion factor will be much smaller compared with other low values of k.

Table 2 .2 : Typical Calculating Results Using SH–PWM Method

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.625 | W | 10 | 48% |
| | | M | 4 | 32% |
| | M = 0.75 | W | 10 | 38% |
| | | M | 4 | 29% |
| | M = 0.875 | W | 6 | 27% |
| | | M | 8 | 35% |
| | M = 1.0 | W | 6 | 19% |
| | | M | 8 | 29% |
| k = 9 | M = 0.625 | W | 8 | 20% |
| | | M | 8 | 27% |
| | M = 0.75 | W | 6 | 17% |
| | | M | 12 | 22% |
| | M = 0.875 | W | 6 | 15% |
| | | M | 12 | 19% |
| | M = 1.0 | W | 6 | 12% |
| | | M | 8 | 13% |
| k = 11 | M = 0.625 | W | 10 | 38% |
| | | M | 12 | 38% |
| | M = 0.75 | W | 10 | 38% |
| | | M | 12 | 32% |
| | M = 0.875 | W | 14 | 36% |
| | | M | 8 | 28% |
| | M = 1.0 | W | 10 | 27% |
| | | M | 8 | 20% |

3. The best modulation result was achieved when k = 9 and M = 1 with the W–type carrier, which in this case, the number of GTO thyristors switched per cycle is equal to 6 and the harmonic distortion factor is equal to 12%.

The operating principle of the SFO–PWM method is similar to the SH–PWM method, except that the reference modulation waveform has a zero sequence component subtracted from it. The zero sequence component is given as the average of the maximum and minimum values of the three reference modulation waveforms.

The addition of the zero sequence voltage does not produce zero sequence currents in the three–phase, three–wire configuration. The advantage of this technique is that it will allow the modulation index to increase by about 15% before overmodulation and pulse dropping occurs.

Figure 2 .6 shows an example of the output waveforms using the SFO–PWM method for the five level GTO inverter. To show a difference, the four triangular carriers here are alternately in opposition ( case 1 ) ), and the parameter $f_m$, k, $A_c$ and M are all the same except using the new reference modulation waveform.

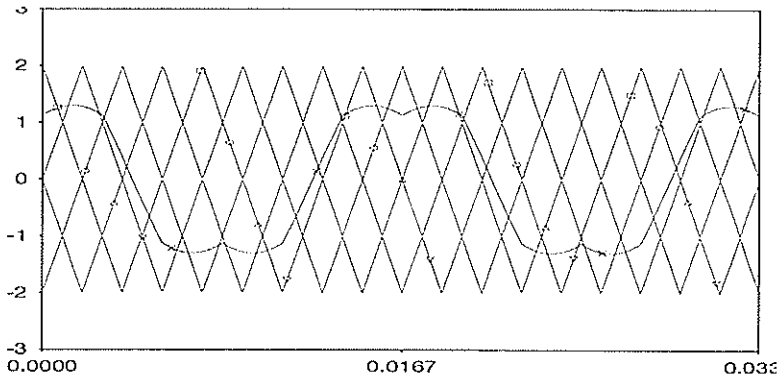



*Figure 2 .6 .a : Carrier and Modulation Waveforms Using SFO–PWM*

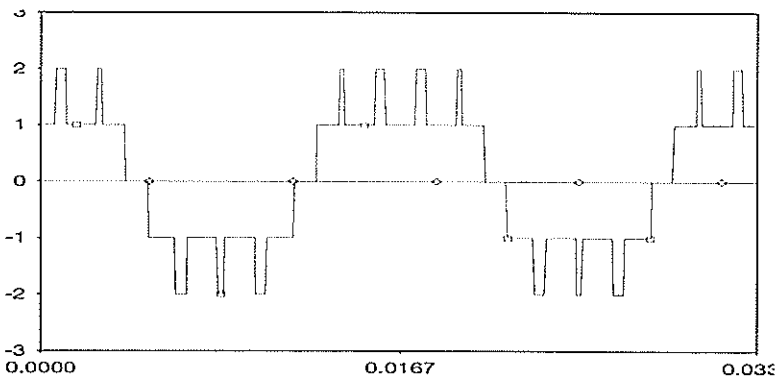



*Figure 2 .6 .b : Output Voltage of the FLI Using SFO–PWM*

The same analysis and calculation procedure using the Mathcad program were performed based on the SFO–PWM method. Again, the disposition of the carriers used here

is for case 3), i.e. all four carriers are in phase. Typical calculation results are tabulated in Table 2 .3 .

Table 2 .3 : Typical Calculating Results Using SFO–PWM Method

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.625 | W | 8 | 25% |
| | | M | 6 | 20% |
| | M = 0.75 | W | 6 | 31% |
| | | M | 8 | 34% |
| | M = 0.875 | W | 6 | 31% |
| | | M | 8 | 38% |
| | M = 1.0 | W | 6 | 27% |
| | | M | 8 | 29% |
| k = 9 | M = 0.625 | W | 8 | 19% |
| | | M | 10 | 24% |
| | M = 0.75 | W | 10 | 20% |
| | | M | 8 | 20% |
| | M = 0.875 | W | 10 | 15% |
| | | M | 8 | 15% |
| | M = 1.0 | W | 10 | 15% |
| | | M | 8 | 13% |
| k = 11 | M = 0.625 | W | 16 | 33% |
| | | M | 6 | 19% |
| | M = 0.75 | W | 14 | 34% |
| | | M | 8 | 29% |
| | M = 0.875 | W | 10 | 32% |
| | | M | 12 | 36% |
| | M = 1.0 | W | 10 | 25% |
| | | M | 12 | 30% |

To summarize the results of Table 2 .3 , we found :

1. Differing from what we got in Table 2 .2 , M = 1 will not always give the best modulation results when the frequency ratio k changes.

2. However, in comparison with other k values, the harmonic distortion factors are obviously smaller if the frequency ratio, k = 9.

3. The best modulation result was achieved when k = 9 and M = 1 with the M–type carrier, which in this case, the number of GTO thyristors switched per fundamental cycle is equal to 8 and the harmonic distortion factor is equal to 13%.

## 2 .4 COMPARISON BETWEEN FFS METHOD AND PWM TECHNIQUES

The better control strategies are based on reducing harmonic distortion, power losses, and speeding transient response. Of which, the FFS method and PWM techniques show great advantages. However, our objective is to determine their characteristics and to choose the one giving the best overall performance for a given number of the GTO inverter level. Thus a detail comparison between the FFS method and the PWM techniques will be given in this section.

### 2 .4 .1 HARMONIC ELIMINATION AND SWITCHING LOSSES

To show a comparison within the FFS method, the SH–PWM and the SFO–PWM technique, the sample Mathcad programs are listed in Appendix A. Typical calculation results were tabulated in Table 2 .4 again, in which the number of GTO thyristors switched per cycle and the overall harmonic distortion factor were compared individually. In the PWM analysis, the frequency ratio k was equal to 9, and the modulation index M was equal to 1 for both W–type carrier and M–type carrier as these two switching states are relatively better, as shown in previous sections.

Table 2 .4 : Comparison between FFS Method and PWM Techniques

| Calculation Results | FFS | SH–PWM | | SFO–PWM | |
|---|---|---|---|---|---|
| | | W | M | W | M |
| DF | 11% | 12% | 13% | 15% | 13% |
| S. No. | 4 | 6 | 8 | 10 | 8 |

As seen from the Table 2 .4 , for balanced three–phase operation the SH–PWM method with k=9, M=1, and W–type carrier gave the better results as compared to the other

PWM switching techniques. However, the FFS method showed clear advantages on the basis of the harmonic elimination and a lower number of switching of the GTO thyristors.

### 2 .4 .2 CONTROL SPEED

As mentioned in the preceding chapter, the reactive power output of a STATCOM is controlled by varying the magnitude of the fundamental component of the inverter output voltage. It can be achieved only by increasing or decreasing the dc capacitor voltages when the FFS method is used. Using PWM techniques, however, the magnitude of the fundamental component can also be changed by varying the modulation index ( M ), which gives more degrees of freedom in the control. Moreover, it takes less time to change M than to charge or discharge the dc capacitors. Therefore, from a rapid control point of view, there are advantages in using PWM techniques. A control system analysis to determine the response of a STATCOM using either FMS or PWM techniques is given in [25].

## 2 .5 CHAPTER SUMMARY

In this chapter, both FFS method and PWM techniques have been proven to be suitable for controlling the output voltage of the inverter. However, using the FFS method, the 5th and 7th harmonics (which are usually the largest) can be cancelled in the five–level inverter. The implication of the harmonic elimination is that the switching losses are kept to a minimum while the rms current through the devices and the transformer windings is considerably reduced. In this control scheme, each GTO thyristor is switched on and off only once during a power frequency cycle. Moreover the filter losses are also reduced because this switching patten does not shift the lower order harmonics to the higher orders which will pass through the high pass filters and thereby increase the power losses.

For the PWM techniques, they are usually considered as the most common methods for controlling the amplitude of the output voltage and the harmonic contents in the voltage

source inverter applications because of their simplicity. In these studies, however, after comparing them with the FFS method, the PWM techniques did not show advantages on the basis of the harmonic elimination and the switching losses apart from the fact of a faster response time.

# *Chapter 3*

# Optimization of the inverter levels

In the last chapter a five level GTO thyristor inverter used as a STATCOM was studied carefully. The results show that the output voltage of the inverter, harmonic distortion, switching losses, and transient speed depend upon the control strategies. In this chapter, the inverter voltage levels will be expanded to higher numbers. For the purpose of optimization, a comparison between five–level, seven–level and nine–level inverter will also be made on the basis of the switching losses, filter requirements, control speed and ratings.

## 3.1 INVESTIGATION OF HIGHER LEVEL INVERTERS

The structure of GTO thyristor inverters with a higher voltage level can be acquired easily from Figure 1.8. Based on the previous analysis, to control the output voltage of these inverters, both the FFS method and the PWM techniques can be used.

Take a seven–level GTO thyristor inverter, for an example, with the fundamental frequency switching of the GTO thyristors, the shape of the output voltage is a staircase type waveform as shown in Figure 3.1, in which the leading reactive current is assumed.

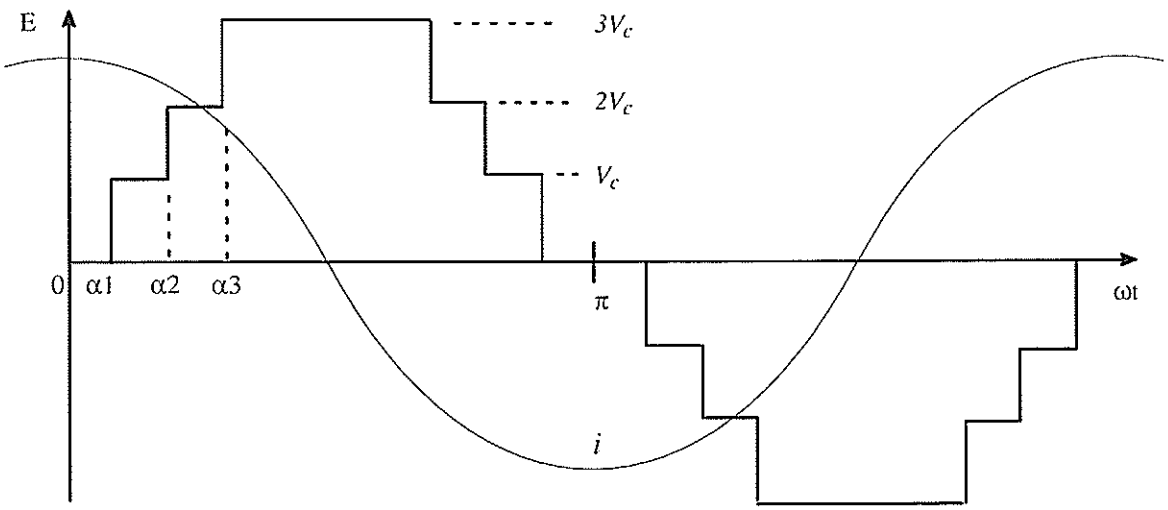



*Figure 3 .1 : A Stepped Output Voltage of the Seven–level Inverter*

The Fourier coefficient for the nth voltage harmonic is:

$$H(n) = \frac{4}{\pi}\frac{V_c}{n}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\right] \qquad (3.1)$$

where n = 1 , 3, 5 , 7 , .....

Now the three values for alpha can be chosen from ( 3 .1 ) to eliminate three harmonics, usually the dominant lower non–triple harmonics, 5th, 7th and 11th. The solution for the seven level inverter gives the three switching angles as: $\alpha_1$=7.1$^0$, $\alpha_2$=15.9$^0$ and $\alpha_3$=36.2$^0$. In the same way, the 5th, 7th, 11th and 13th harmonics can be eliminated in the nine–level GTO thyristor inverter.

It should be mentioned that the solution of the above switching angles could be different. For example, to cancel the 5th, 7th, 11th and 13th harmonics in the nine–level inverter, the solutions can be as follows:

| | | | | |
|---|---|---|---|---|
| $\alpha 1 = 9.05^0$ | $\alpha 2 = 18.56^0$ | $\alpha 3 = 34.17^0$ | $\alpha 4 = 57.88^0$ | or |
| $\alpha 1 = 5.48^0$ | $\alpha 2 = 34.72^0$ | $\alpha 3 = 44.44^0$ | $\alpha 4 = 78.43^0$ | or |
| $\alpha 1 = 12.94^0$ | $\alpha 2 = 35.36^0$ | $\alpha 3 = 58.75^0$ | $\alpha 4 = 88.06^0$ | or |
| $\alpha 1 = 13.98^0$ | $\alpha 2 = 29.93^0$ | $\alpha 3 = 51^0$ | $\alpha 4 = 64.22^0$ | . |

It is obvious that the magnitude of the fundamental component and the harmonic content in the inverter output voltage will change with these switching angles. In other words, these angles and voltage levels can be optimized for better harmonic distortion factors and/or larger fundamental voltages. For instance, the first group of the switching angles ($\alpha_1$=9.05$^0$, $\alpha_2$=18.56$^0$, and $\alpha_3$=34.17$^0$, $\alpha_4$=57.88$^0$) shows the best performance compared with others.

For the application of the PWM techniques, the basic control principle is the same as that discussed in the last chapter. The only difference is that more triangular carriers are needed here. For this reason, a higher number of switching of GTO thyristors may be required as the voltage level increases.

As an example of the SH–PWM method, Figure 3 .2 shows the modulation results used in the seven–level GTO thyristor inverter for the case of k = 9 and M = 75% with W–type carriers which are all in phase.

Figure 3 .3 shows an example of the output waveforms using the SFO–PWM method for the nine–level GTO thyristor inverter, in which the M–type carriers are all in phase, and the frequency ratio k was equal to 9 and the modulation index M was equal to 100%.

The detailed analysis for both the seven–level and nine–level GTO thyristor inverter, based on the FFS method and the PWM techniques, has been performed with the Mathcad program. The results tell us:

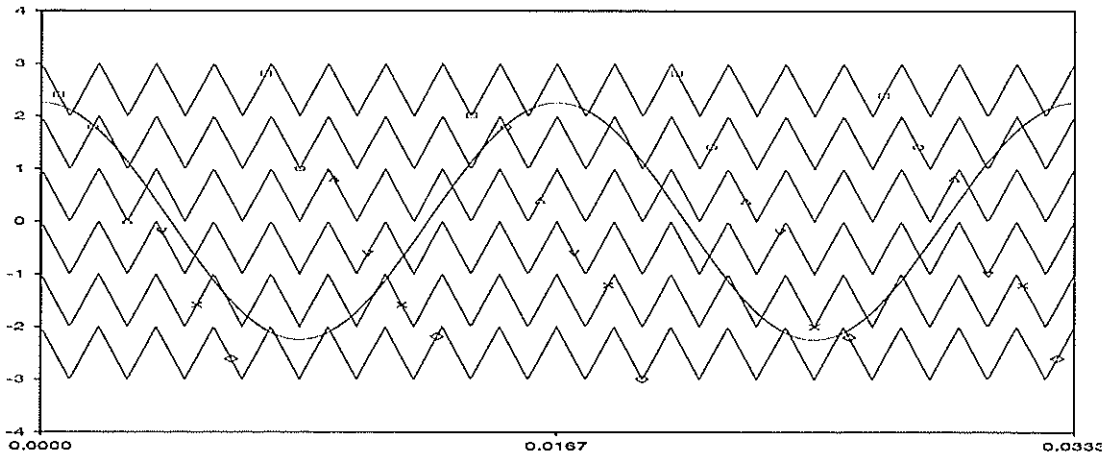
1. The frequency ratio k = 9 always gives the best modulation results for either PWM technique.

2. Using W–type carriers is better than using M–type carriers in consideration of reducing harmonic distortion factor if the PWM techniques are used.

3. There is little difference between the SH–PWM and SFO–PWM method.

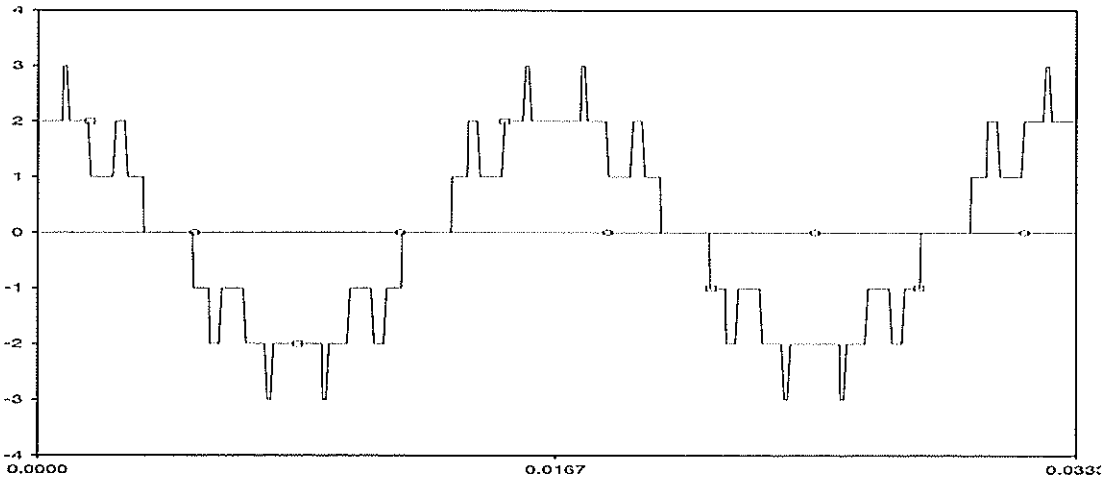
4. The FFS method shows clear advantages over the PWM techniques in this application on the basis of harmonic elimination and a lower number of switching of the GTO thyristors.

Typical calculation results are summarized in Appendix B for reference.




*Time (s)*

*Figure 3 .2 .a : Carrier and Modulation Waveforms Using SH–PWM*




*Time (s)*

*Figure 3 .2 .b : Output Voltage of the SLI Using SH–PWM*

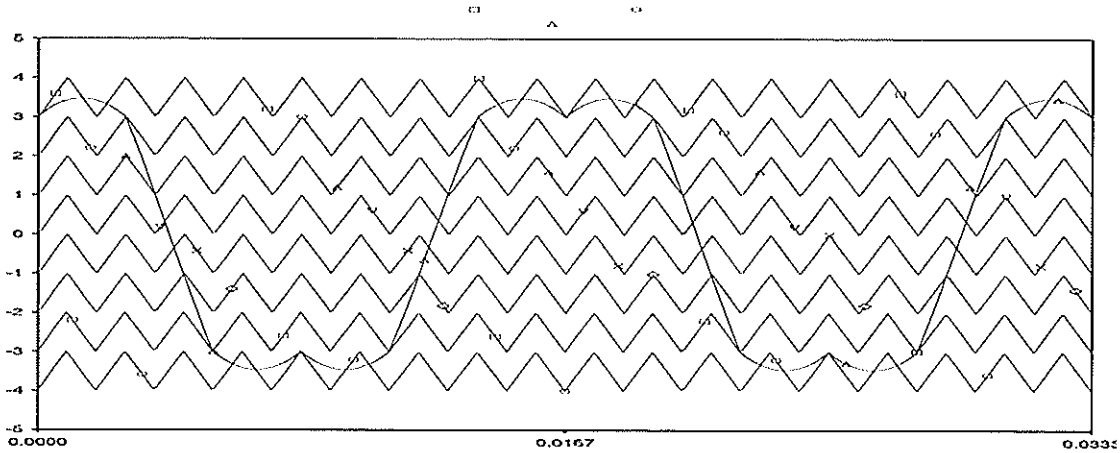



*Figure 3 .3 .a : Carrier and Modulation Waveforms Using SFO–PWM*

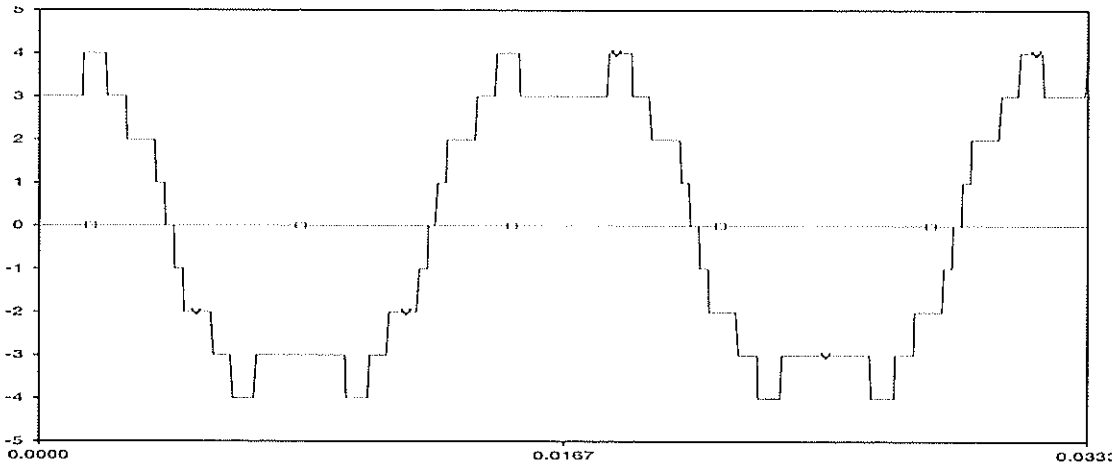



*Figure 3 .3 .b : Output Voltage of the NLI Using SFO–PWM*

## 3 .2 RATINGS OF M–STATCOM

GTO thyristors currently have ratings in the range of 4.5 kV and 3.0 kA (MITSUBISHI ELECTRIC FG3000AV). Based on these, the dc off–state voltage can be as high as 3.6 kV. Leaving a 20% safety range, the maximum steady state dc voltage of the STATCOM can be set to 2.88 kV giving $V_c = 2.88$ kV per level. The current rating of this device is 800 A ( average ). Then the rms phase current of the device can be calculated as follows:

Taking Figure 3 .1 as an example, the phase current is assumed to be:

$$i = \sqrt{2}\, I_{rms}\, cos\ (\ \omega t\ )$$

Because each GTO thyristor and reverse conducting diode carries alternatively a 90–degree segment of the output current in each cycle, the average current can be expresses as follows:

$$I_{ave} = \frac{1}{2\,\pi}\int_{0}^{\frac{\pi}{2}} \sqrt{2}\, I_{rms}\, cos\ (\ \omega t\ )d(\ \omega t\ ) = \frac{I_{rms}}{\sqrt{2}\ \pi} = 800\ A \quad (3.2)$$

This gives an rms phase current of 3.554 kA.

It is also important to note that the GTO thyristor has to be turned off at the peak of the current when the output is capacitive, but it commutes naturally (being switched off) at the zero of the current when the reactive power is absorbed. Therefore, the STATCOM can absorb vars transiently well above its steady state rating, and therefore be effective in limiting the overvoltage during load rejections.

The reverse conducting diodes should have equivalent voltage ratings to the GTO thyristors. At the same time, as explained in Chapter 1, in order to block different voltages, series connections of the clamping diodes are required. However, the current ratings between the reverse conducting diodes and the clamping diodes in the STATCOM are different. All reverse diodes should have same current ratings as the GTO thyristors while the current ratings of the clamping diodes can be much smaller. For example, the average current of the clamping diodes for blocking the intermediate voltage ( say between $a1$ and $a2$, as shown in Figure 3 .1 ) based on the rms phase current of $I_{rms}$ can be calculated as follows:

$$I_{c-ave} = \frac{1}{2\,\pi}\int_{a1}^{a2} \sqrt{2}\, I_{rms}\, cos\ (\ \omega t\ )d(\ \omega t\ ) = \frac{I_{rms}}{\sqrt{2}\ \pi}(\ \sin a2 - \sin a1\ ) \quad (3.3)$$

It is clear that the current ratings of the clamping diodes will depend on the inverter voltage levels and the switching angles. For instance, in a seven–level inverter, if a voltage of zero is blocked, the switching angles are $0^0$ and $7.1^0$ , respectively. Then the average current of clamping diodes in this state is equal to 89 A, which is only 11% of the GTO thyristor current.

Using the above devices as reference, the five–level, seven–level and nine–level GTO thyristor inverters will give the three phase ratings of ± 50 Mvar, 8.5 kV ; ± 77 Mvar, 12.6 kV and ± 92 Mvar, 14.9 kV, respectively, if the FFS method is used ( because the STATCOM behaves symmetrically the inductive rating is equal to the capacitive rating ).

On the basis of the PWM techniques, the overall ratings of the inverters may differ from that using FFS method as the fundamental component of the output voltage varies with the modulation index, M. However, roughly speaking, they can be considered as having the same ratings.

## 3 .3 DETERMINATION OF THE OPTIMUM VOLTAGE LEVEL

Based on the above analysis, we know that, theoretically, the level of the GTO thyristor inverter could reach any number by simply adding capacitors and GTO thyristors with corresponding diodes. However, experience from the field of high power electronics indicates that voltage levels greater than nine may have problems because of the limits of the circuit complexity from many aspects, such as valve design, mechanical layout, and the overall loss figures. On the other hand, an extremely low number of levels makes no sense in terms of harmonic elimination. From this point of view, the five–level, seven–level and nine–level GTO thyristor inverters will only be considered in the next discussion.

To determine the optimum voltage level, typical results are tabulated in Table 3 .1. In Table 3 .1 three voltage inverter levels were considered, and the number of GTO thyristor switched per fundamental cycle (S.No.), the percentage of the fundamental component on the basis of that produced by the square wave ( F.C. ) and the harmonic distortion factor ( DF ) were compared. The data used here are all representative of the best switching patten for each case.

From the Table 3 .1 , it was found:

Table 3 .1 : Comparison for 5–level, 7–level and 9–level GTO Inverter

| Control State | | | S. No. | F.C. | DF |
|---|---|---|---|---|---|
| 5–level Inverter | F.F.S. | | 4 | 93% | 11% |
| | SH–PWM | W–type carrier | 6 | 75% | 12% |
| | | M–type carrier | 8 | 82% | 13% |
| | SFO–PWM | W–type carrier | 10 | 79% | 15% |
| | | M–type carrier | 8 | 79% | 13% |
| 7–level Inverter | F.F.S. | | 6 | 92% | 5.9% |
| | SH–PWM | W–type carrier | 8 | 80% | 6.8% |
| | | M–type carrier | 10 | 78% | 8.6% |
| | SFO–PWM | W–type carrier | 12 | 79% | 8.6% |
| | | M–type carrier | 8 | 62% | 11% |
| 9–level Inverter | F.F.S. | | 8 | 83% | 4.8% |
| | SH–PWM | W–type carrier | 10 | 82% | 6.9% |
| | | M–type carrier | 8 | 70% | 6.1% |
| | SFO–PWM | W–type carrier | 12 | 78% | 5.6% |
| | | M–type carrier | 10 | 77% | 6.8% |

1. For the application of the PWM techniques, not much difference could be seen within various switching patterns.

2. When the inverter level is increased from five to seven, the harmonic distortion is reduced greatly. However, increasing the number of levels beyond seven seems to reduce the harmonic distortion very little.

3. For all three types of inverters, the FFS method always gives the best results, i.e. the lowest GTO thyristor switching numbers, the highest percentage of the fundamental components and the lowest harmonic distortion factors.

4. Comparing the nine–level inverter with the seven–level inverter, when the FFS method was used, the harmonic distortion factor could be further reduced by 1%. However, in addition to the increase of the GTO thyristor switching numbers, the fundamental component was down to 83% of that produced by the square wave, which shows that there may not be much attraction to using a nine–level GTO thyristor inverter as the benefit seems to be small compared to increasing the complexity of the valve.

However, the increase of the inverter level means that a higher reactive power output can be achieved, which is more attractive for transmission system applications. On the other hand, as explained earlier, concerning the increase of the transient response speed of the device, PWM techniques may be a better choice because the reactive power output of the STATCOM can be adjusted easily and quickly by simply changing the modulation index while reducing the lower order harmonics.

## 3.4 CHAPTER SUMMARY

From the above discussion, it may be concluded that various options are available in selecting the optimum structure of the M–STATCOM, which depend mainly on the demand of the reactive power, the tolerance of the harmonic distortion, the limitation of the switching losses, and the transient response time of the output voltage. For a larger percentage of the fundamental voltage, fewer switching of the GTO thyristors, and better results of harmonic elimination, the FFS method shows clear advantages. For the maximum size of the M–STATCOM, a nine–level GTO thyristor inverter has the ability to supply 92 Mvar reactive power at the voltage of 14.9 kV without higher pulse number connections. All these options provide ideal control of the output voltages, in which the PWM techniques are even faster.

For further studies, I would recommend using seven–level or nine–level GTO thyristor inverter with the FFS method as a candidate STATCOM for the simulation studies.

# *Chapter 4*
# Power losses

During the operation of a M–STATCOM, the principle source of losses arise from the current flow through the GTO thyristors. However, other components in the inverter will also have their losses. In other words, there are various amounts of power dissipated in the switching devices, associated snubber circuits and clamping diodes. Moreover, the actual amounts of power losses will depend on the design of the device, the switching pattens, harmonic spectrum, operating conditions of the M–STATCOM, and so on. Investigations of all these factors can be a large topic which is beyond the scope of this thesis. Therefore, the efforts of this Chapter will be only focused on analyzing and calculating the principle losses in the M–STATCOM, in which a nine–level GTO thyristor inverter with the FFS method is assumed.

## 4.1 PRINCIPLES OF CALCULATION

Prior to developing detailed methods to analyze and calculate the power losses in the M–STATCOM, we will begin to review some basic principles. Generally speaking, there are

two categories of power losses in the switching device. One is the steady state loss and another is the switching loss. Theoretically, the average steady state power loss, including the on–state loss and off–state loss, can be obtained by:

$$p_t = \frac{1}{T} \int_0^T u\, i\, dt \tag{4.1}$$

Where $T$ is the switching cycle, $u$ is either the on–state voltage or the off–state voltage across the device and $i$ is either the corresponding on–state current or off–state current through it. The device can be a GTO thyristor or a diode.

For the switching loss, about 10% of the steady state loss per pulse was suggested [23]. Associated with the switching loss of a GTO thyristor is the snubber circuit loss. For the polarized snubber shown in Figure 4 .1 , the capacitor is fully charged with the voltage equal to the blocking voltage of the GTO thyristor when GTO thyristor is off.

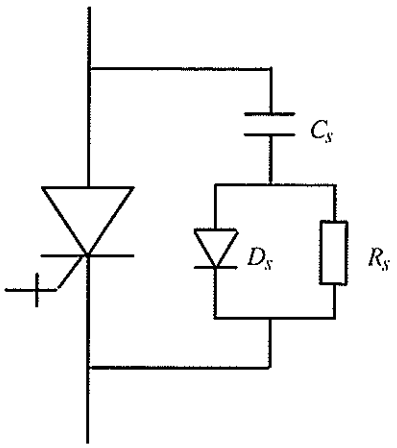



*Figure 4 .1 : Snubber Circuit for a GTO Thyristor*

The energy stored in the capacitor can be calculated by:

$$E_c = \frac{1}{2} C_s V^2 \tag{4.2}$$

Where $C_s$ is the value of the snubber capacitor and $V$ is the voltage across it. This energy will be absorbed by the snubber resistor, $R_S$, in the form of heat when the GTO thyristor turns on. The corresponding average power loss per pulse is:

$$p_r = \frac{E_c}{T} \tag{4.3}$$

The amount of the loss $p_r$ varies with the value of $C_s$ which is chosen on the requirement for *dv/dt* protection of the GTO thyristor and the load current to be connected to the capacitor when the GTO thyristor turns off. The total switching transient loss, including snubber loss, is proportional to the pulse number of the inverter scheme.

In summary, the total power loss in the GTO thyristor inverter will be:

$$P = p_1 + 10\% \, p_1 + p_r \tag{4.4}$$

## 4 .2 DETAIL CONSIDERATION

In this Section, a nine–level GTO thyristor inverter with the FFS method will be discussed. Particularly, a detailed analytical method for calculating the on–state and off–state losses in the M–STATCOM will be given. Figure 4 .2 shows a schematic arrangement of one phase for this inverter, in which $Q_1$, $Q_2$, ,, $Q_8$ represent the upper group of the GTO thyristors, $Q_1'$, $Q_2'$, ,, $Q_8'$ represent the lower group of the GTO thyristors, and *D* represents the clamping diode. It should be noted that the number of the clamping diodes is not the same in different voltage levels, because they are required to block different voltages. For example, *1D* represents one diode as its blocking voltage is only a single dc level while *2D* represents two diodes because it must block two dc levels, and so on.

### 4 .2 .1 ON–STATE LOSS

As mentioned earlier, the on–state loss depends directly on the on–state voltages across the switching devices and the on–state current through them. Talking about GTO thyristors and diodes, the on–state voltages can be simply determined by the on–state currents through them. In other words, the on–state loss in the M–STATCOM can be calculated based on the reactive output current of the inverter.

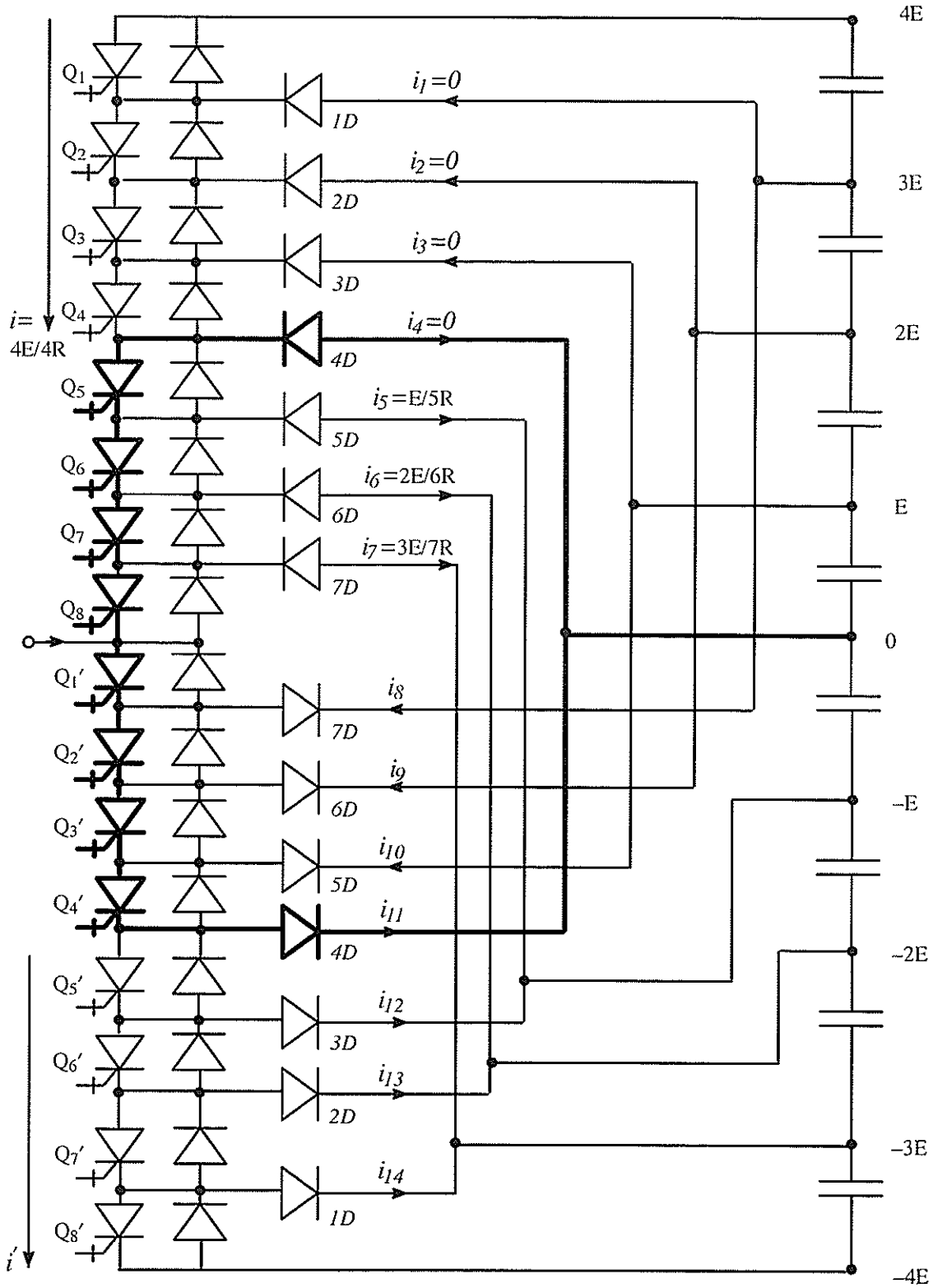



*Figure 4 .2 : One Phase Arrangement of a Nine–level GTO Inverter*

Now, supposing the reactive current generated by the inverter contains no harmonics, which, in this case, is equal to :

$$i = I_m \cos(\omega t) \tag{4.5}$$

Where, $I_m$ is the peak value of the phase current.

Then, the on–state voltages [24] across a GTO thyristor and a diode with respect to the current through them are:

$$v_{GTO-on} = 1.8 + 0.0006\, i \tag{4.6}$$

$$v_{Diode-on} = 1.5 + 0.0005\, i \tag{4.7}$$

As a result, during the on–state, the instantaneous power losses in the GTO thyristors and the diodes can be expressed as follows:

$$p_{GTO-on} = G_{no} ( 1.8 + 0.0006\, i )\, i \tag{4.8}$$

$$p_{Diode-on} = D_{no} ( 1.5 + 0.0005\, i )\, i \tag{4.9}$$

Here $G_{no}$ represents the number of conducting GTO thyristors involved and, similarly, $D_{no}$ represents the number of conducting diodes.

Therefore, the average on–state power loss in the M–STATCOM during any interval of the switching angles ( say, between $\alpha 1$ and $\alpha 2$ ) can be expressed as follows:

$$P_{on} = \frac{1}{2\pi} \int_{\alpha 1}^{\alpha 2} ( p_{GTO-on} + p_{Diode-on} )\, d(\omega t) \tag{4.10}$$

Based on this formula, the total on–state power loss in the M–STATCOM can be obtained if the switching angles and the number of conducting GTO thyristors and diodes are known. The switching angles using the FFS method are fixed because of the requirements of eliminating the dominant lower non–triplen harmonics. The number of conducting GTO thyristors and diodes are different, depending on the switching voltage levels. It should be mentioned that, at any time, there are always eight GTO thyristors in the on–state for the

nine–level inverter, but not all are carrying the current. For example, as seen in Figure 4 .2 , if zero voltage is connected to the inverter terminal, the GTO thyristors $Q_5$, $Q_6$, ,, $Q_4'$ will be conducting. However, only four GTO thyristors will carry the current in the defined direction of the current in the figure ( $Q_1'$, $Q_2'$, $Q_3'$, and $Q_4'$ in this case ). The switching angle range and the corresponding number of the on–state GTO thyristors and diodes in the positive half cycle of the fundamental are given in Table 4 .1 based on the nine–level inverter type of STATCOM with the FFS method. The results in the negative half cycle of the fundamental will be the same because of the symmetrical circuits.

Table 4 .1 : Switching Angles and Corresponding Number of Conducted GTO Thyristors and Diodes

| Range of firing angles | Number Conducting |
|---|---|
| $0^0$ to $9.05^0$ | 4 GTO thyristors + 4 Diodes |
| $9.05^0$ to $18.56^0$ | 3 GTO thyristors + 5 Diodes |
| $18.56^0$ to $34.17^0$ | 2 GTO thyristors + 6 Diodes |
| $34.17^0$ to $57.88^0$ | 1 GTO thyristors + 7 Diodes |
| $57.88^0$ to $90^0$ | 0 GTO thyristors + 8 Diodes |
| $90^0$ to $122.12^0$ | 8 GTO thyristors + 0 Diodes |
| $122.12^0$ to $145.83^0$ | 7 GTO thyristors + 1 Diodes |
| $145.83^0$ to $161.44^0$ | 6 GTO thyristors + 2 Diodes |
| $161.44^0$ to $170.95^0$ | 5 GTO thyristors + 3 Diodes |
| $170.95^0$ to $180^0$ | 4 GTO thyristors + 4 Diodes |

## 4 .2 .2 OFF–STATE LOSS

In order to calculate the off–state loss, the following assumptions are made.

1. The blocking device is equal to a very large resistor ( R ).

2. The blocking resistance of a GTO thyristor is same as that of a diode.

3. The dc voltage at each level is constant ( E ).

Based on the above assumptions, the off–state loss in the inverter can be simply computed by solving for the heat losses in the blocking devices because of the effect of the dc leakage currents in the inverter. That is, the square of the leakage current times the corresponding blocking resistance during each range of the switching angles. For instance, under the condition of the zero voltage at the output terminal ( i.e., the switching angle is between $0$ to $\alpha 1$ in the positive quarter cycle of the fundamental ), the blocking and the conducting state of the inverter have been shown in Figure 4 .2 . Because the zero voltage is connected to the output terminal, the devices shown in bold lines are in the conduction state. Checking the top four GTO thyristors in the upper group of the inverter, it is found that the leakage current $i$ is equal to 4E/4R as the GTO thyristors $Q_1$, $Q_2$, $Q_3$, and $Q_4$ are blocked by their own dc voltages. In other words, the voltages across $Q_1$, $Q_2$, $Q_3$, and $Q_4$ are all equal to E. Therefore the branch current $i_1$, $i_2$, and $i_3$ are zero. However, $i_5$ is not zero as the GTO thyristor $Q_5$ is in conduction. The five diodes in the branch of $i_5$ are blocked by one dc voltage (E), so $i_5$ is equal to E/5R. Similarly, there are six and seven diodes in the branches of $i_6$ and $i_7$. Their blocking voltages are two and three dc levels in the order given. Therefore, $i_6$ and $i_7$ are expressed as 2E/6R and 3E/7R respectively. The same results can be obtained in the lower group devices of the inverter because of the symmetrical circuit.

After calculating the leakage current in each loop, the off–state loss can be computed in this case as follows:

$$p_{b1} = 2 [ i^2 ( 4 R ) + i_5^2 ( 5 R ) + i_6^2 ( 6 R ) + i_7^2 ( 7 R ) ] \qquad (4.11)$$

The identical analytical method is applied to calculate the off–state loss in other switching voltage levels. It is clear that the leakage currents and the corresponding blocking devices depend on the the switching state to the switching state. Because the computation of the off–state loss is symmetrical about $\pi/2$, there are five switching voltage stages

involved in the nine–level inverter. Therefore the five different off–state losses can be obtained based on the above analysis.

It should be noted that the off–state losses obtained above are the instantaneous losses. The average off–state power loss in a fundamental cycle is:

$$p_{off} = \frac{2}{\pi} [ P_{b1} \alpha_1 + P_{b2} ( \alpha_2 - \alpha_1 ) + P_{b3} ( \alpha_3 - \alpha_2 ) + P_{b4} ( \alpha_4 - \alpha_3 ) + P_{b5} ( \frac{\pi}{2} - \alpha_4 ) ] \quad (4.12)$$

Where, $\alpha_1$, $\alpha_2$, $\alpha_3$, and $\alpha_4$ are four fixed switching angles for eliminating 5th, 7th, 11th and 13th harmonics on the basis of the FFS method. $P_{b1}$, $P_{b2}$, $P_{b3}$, $P_{b4}$, and $P_{b5}$, are the corresponding total off–state loss during each switching voltage level in the nine–level GTO thyristor inverter.

## 4.3 RESULTS

Based on the above discussion, the total power loss in the nine–level inverter type of STATCOM is computed. The detailed calculation procedure is attached in Appendix C. The results show that the loss in the nine–level GTO inverter type of STATCOM is less than 0.4%, which is much smaller than that of the conventional STATCOM ( 1% ) [9]. Part of the reason is that, in the M–STATCOM, the peak current occurs at minimum voltage and the peak voltage occurs at minimum current, which means that there are the lowest number of GTO thyristors in series during peak current intervals, while with the number of conducting GTO thyristor increasing, the current decreases. However, in the conventional STATCOM design all GTO thyristors operate together.

## 4.4 CHAPTER SUMMARY

It is not simple to get a numerical solution for the power losses of the M–STATCOM. The method introduced in this Chapter was concentrated on a nine–level inverter type of

STATCOM. However, the concept and the procedure performed can be easily expanded to determine the power losses for other levels. The study result indicated that the design of the M–STATCOM has advantages to reduce overall power losses compared with the conventional STATCOM. For further investigation, the effect of the harmonics in the reactive current should be included.

# *Chapter 5*
# Effect of capacitor size on the STATCOM

Unlike traction and motor drive applications, the STATCOM does not require a separate dc supply. A small dc capacitor can maintain the dc voltage. Additional functions of the dc capacitor include the establishment of an energy balance between the input and output during the dynamic changes of the var output and the limitation of the ripple component in the output voltage of the inverter. Therefore, the dc capacitor plays a very important part in the design and operation of the STATCOM. This chapter will study the interactions within the STATCOM on the issue of the dc capacitor size, the dc current and voltage ripples, and corresponding harmonic content in the inverter's output voltage. A simple analytical method to calculate the current ripple on the dc capacitor of the STATCOM will be introduced. The solutions will benefit the further investigation, design and operation of the STATCOM.

## 5.1 BASIC THEORY

In order to study the effect of the dc voltage ripple on the performance of the STATCOM, first, let us consider a basic voltage pulse of the inverter, in which the dc

capacitor voltage is equal to $V_c$ and the firing angle is $\alpha$ ( $0 < \alpha < \pi/2$ ). In this case, the waveform of one phase of the inverter output voltage ( say, phase A ) is shown in Figure 5 .1

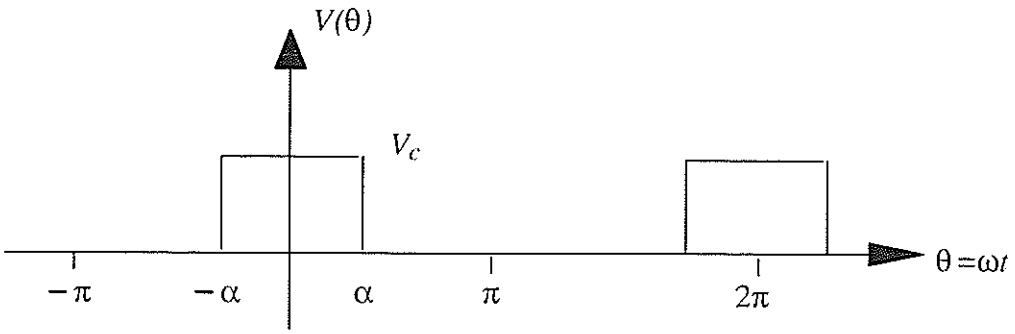



*Figure 5 .1 : Basic Voltage Pulse of the Inverter*

Performing the Fourier Transform for this waveform, we get :

$$v_a(\theta) = a_0 + \sum_n a_n \cdot \cos(n \cdot \theta) \tag{5.1}$$

where : $$a_0 = \frac{1}{2 \cdot \pi} \cdot \int_{-\alpha}^{\alpha} V_c d\theta = \frac{V_c}{\pi} \cdot \alpha \tag{5.2}$$

and : $$a_n = \frac{1}{\pi} \cdot \int_{-\alpha}^{\alpha} V_c \cdot \cos(n \cdot \theta) d\theta = \frac{2 \cdot V_c}{\pi} \cdot \frac{1}{n} \cdot \sin(n \cdot \alpha) \tag{5.3}$$

and : $$n = 1, 2, \ldots, \infty$$

Similarly, we have : $$v_b(\theta) = v_a\left(\theta - \frac{2\pi}{3}\right) \tag{5.4}$$

$$v_c(\theta) = v_a\left(\theta - \frac{4\pi}{3}\right) \tag{5.5}$$

Now suppose the leading reactive current is : $$i_a(\theta) = -\sqrt{2} I \sin(\theta) \tag{5.6}$$

$$i_b(\theta) = -\sqrt{2} I \sin\left(\theta - \frac{2\pi}{3}\right) \tag{5.7}$$

$$i_c(\theta) = -\sqrt{2} I \sin\left(\theta - \frac{4\pi}{3}\right) \tag{5.8}$$

So, the current flowing in the dc capacitor is :

$$i_{ca}(\theta) = \frac{v_a(\theta) i_a(\theta)}{V_c} + \frac{v_b(\theta) i_b(\theta)}{V_c} + \frac{v_c(\theta) i_c(\theta)}{V_c} \tag{5.9}$$

Then, the dc voltage ripple produced by $i_{ca}(\theta)$is :

$$v_{cr}(\theta) = \frac{1}{C} \cdot \int_0^{\theta} i_{ca}(\theta) d\theta \qquad (5.10)$$

where C is the dc capacitance used in the inverter.

In order to set a reference dc voltage, the average value of the dc voltage ripple should be calculated:

$$V_{cr} = \frac{1}{2\pi} \cdot \int_0^{2\pi} v_{cr}(\theta) d\theta \qquad (5.11)$$

Therefore, the real dc voltage with ripple included is : $v_{dc}(\theta) = v_{cr}(\theta) - V_{cr} + V_c$ (5.12)

In which, the reference dc voltage is assumed to be $V_c$.

Substituting (5.12) for $V_c$ of equations (5.2) and (5.3), the real inverter output voltage with ripple included can be determined.

## 5.2 CALCULATION OF DC RIPPLE

Based on the above analysis, the dc ripple values in the multi–level GTO thyristor inverter type of STATCOM can be calculated. Consider a six–pulse, nine–level inverter as an example. The dc capacitive voltages on the upper four levels can be expressed as follows:

$$v_{c1}(\theta) = a_0(\alpha 1) + \sum_n a_n(\alpha 1) \cdot \cos(n \cdot \theta) \qquad (5.13)$$

$$v_{c2}(\theta) = a_0(\alpha 2) + \sum_n a_n(\alpha 2) \cdot \cos(n \cdot \theta) \qquad (5.14)$$

$$v_{c3}(\theta) = a_0(\alpha 3) + \sum_n a_n(\alpha 3) \cdot \cos(n \cdot \theta) \qquad (5.15)$$

$$v_{c4}(\theta) = a_0(\alpha 4) + \sum_n a_n(\alpha 4) \cdot \cos(n \cdot \theta) \qquad (5.16)$$

where, $a_0$ and $a_n$ were given by (5.2) and (5.3), and $n = 1, 2, \ldots, \infty$

$\alpha 1$, $\alpha 2$, $\alpha 3$, and $\alpha 4$ can be chosen at such values that any angle within the range of 0 to $\pi/2$ on the basis of getting a lower harmonic content.

Then, the positive inverter voltage should be $v_p(\theta) = v_{c1}(\theta) + v_{c2}(\theta) + v_{c3}(\theta) + v_{c4}(\theta)$ (5.17)

And, the negative is : $v_n(\theta) = v_p(\theta - \pi)$ (5.18)

Equation (5.19) subtracted by (5.18), we have : $v_a(\theta) = v_p(\theta) - v_n(\theta)$ (5.19)

Equation (5.20) gives the inverter output voltage of the phase A.

Similarly, for the phase B and C we have : $v_b(\theta) = v_a\left(\theta - \frac{2\pi}{3}\right)$ (5.20)

$$v_c(\theta) = v_a\left(\theta - \frac{4\pi}{3}\right) \quad (5.21)$$

Based on equations (5.13) through (5.16), the current ripple flowing in each capacitor can be obtained as follows:

$$i_{c1}(\theta) = \frac{v_{c1}(\theta)\ i_a(\theta)}{V_c} + \frac{v_{c1}\left(\theta - \frac{2\pi}{3}\right)\ i_b(\theta)}{V_c} + \frac{v_{c1}\left(\theta - \frac{4\pi}{3}\right)\ i_c(\theta)}{V_c} \quad (5.22)$$

where $i_a(\theta)$, $i_b(\theta)$, and $i_c(\theta)$ were given by equations (5.6), (5.7), and (5.8), respectively. Similarly, the $i_{c2}(\theta)$, $i_{c3}(\theta)$, and $i_{c4}(\theta)$ can be obtained in the same way ( while $i_{c5}(\theta)$, $i_{c6}(\theta)$, $i_{c7}(\theta)$, and $i_{c8}(\theta)$ of lower capacitor group can be determined by $i_{c1}(\theta)$, $i_{c2}(\theta)$, $i_{c3}(\theta)$, and $i_{c4}(\theta)$ as they are symmetrical).

After the current ripples are obtained, the real dc voltage with the ripple included on each capacitor can be obtained using equations (5.10), (5.11) and (5.12). The same is true of the inverter output voltage with ripple considered.

As mentioned earlier, the M–STATCOM can be connected in higher pulse number arrangements just like the two–level inverter type of STATCOM. For the high–pulse connection of the multi–level inverters, the ripples on the dc capacitors can be calculated in the same way. For instance, the current ripple flowing on the first capacitor from the top in the twelve–pulse, nine–level inverter can be simply expressed by expanding the equation (5.22) :

$$i_{c1}(\theta) = \frac{v_{c1d}(\theta)\, i_{ad}(\theta)}{V_c} + \frac{v_{c1d}\left(\theta - \frac{2\pi}{3}\right) i_{bd}(\theta)}{V_c} + \frac{v_{c1d}\left(\theta - \frac{4\pi}{3}\right) i_{cd}(\theta)}{V_c}$$

$$+ \frac{v_{c1y}(\theta)\, i_{ay}(\theta)}{V_c} + \frac{v_{c1y}\left(\theta - \frac{2\pi}{3}\right) i_{by}(\theta)}{V_c} + \frac{v_{c1y}\left(\theta - \frac{4\pi}{3}\right) i_{cy}(\theta)}{V_c} \qquad (5.23)$$

The difference between $V_{c1d}(\theta)$ and $V_{c1y}(\theta)$ is a $30^0$ phase shift, and the same is true of other phases.

Based on the above method, capacitive current ripples, dc voltage ripples and the corresponding output voltage of a six–pulse, nine–level inverter type of STATCOM of $\pm$ 50 Mvar are examined for the case of $V_c$ =3 kV, I=1.873 kA and C=1000 μF. The results are shown as follows, in which Figures 5 .2 , 5 .3 , 5 .4 and 5 .5 give current ripples in upper four dc capacitors respectively, and Figure 5 .6 is the inverter output voltage with the ripple included. It is observed that the current ripple flowing in each capacitor is not identical. The smallest dc current ripple is on the first capacitor from the top and the largest one is on the second capacitor from the top. It implies that both the waveforms and the peak to peak values of the dc voltage ripples on different voltage levels can be quite different. The same results apply to the lower four levels.

## 5 .3 HARMONIC SPECTRUM WITH DC RIPPLES INCLUDED

As seen from the last section, comparing an assumption of a constant dc voltage with that including dc voltage ripples the waveform of the inverter output voltage is quite different. As a result, the harmonic spectrum in the inverter output voltage and the overall performance of the STATCOM might be affected. Therefore, it will be interesting to discuss it in depth. According to the above analysis, factors that may effect the dc voltage ripples include the dc capacitor values, circuit configurations and the inverter's output currents.

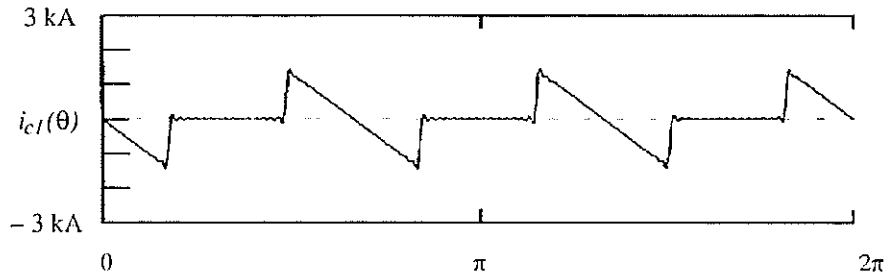



*Figure 5 .2 : Current Ripple in the First Capacitor from Top of a Nine–level Inverter*

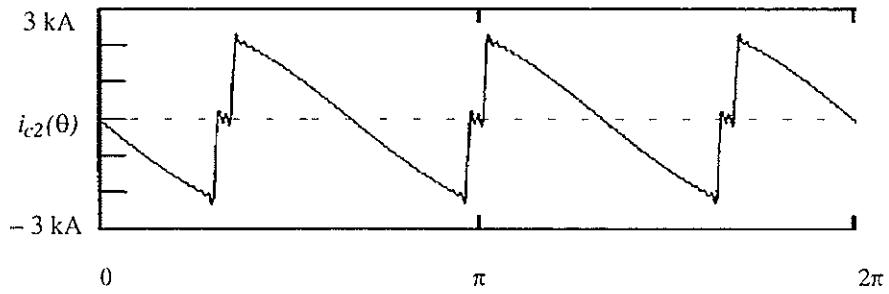



*Figure 5 .3 : Current Ripple in the Second Capacitor from Top of a Nine–level Inverter*

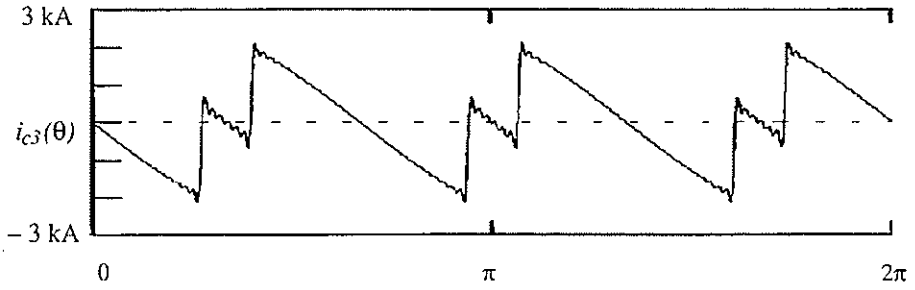



*Figure 5 .4 : Current Ripple in the Third Capacitor from Top of a Nine–level Inverter*

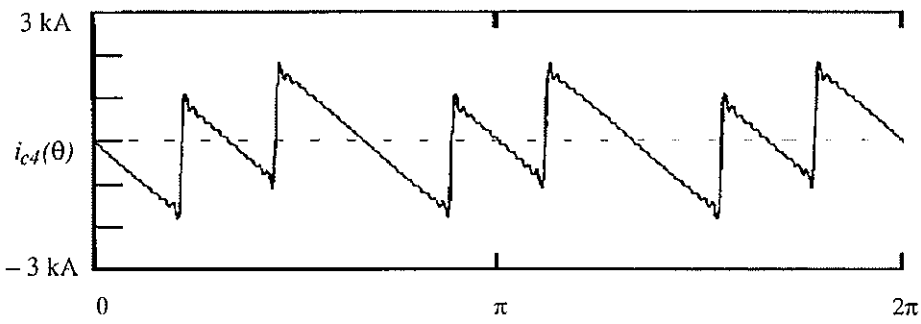



*Figure 5 .5 : Current Ripple in the Fourth Capacitor from Top of a Nine–level Inverter*

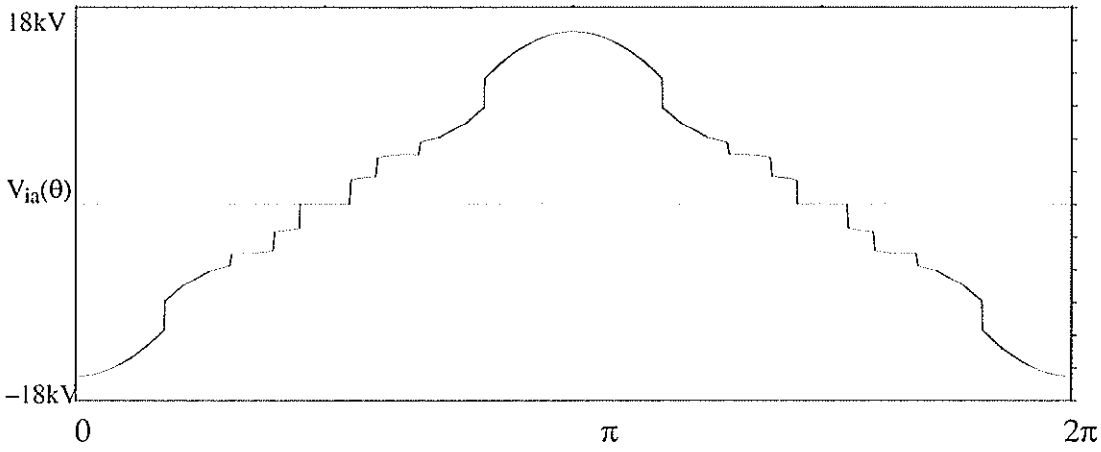



*Figure 5 .6 : Output Voltage of a Nine–level Inverter with Ripples Included*

It is obvious that the dc capacitance makes a direct contribution in controlling the dc voltage ripple as the dc voltage ripple is inversely proportional to the dc capacitor's value, as seen in equation (5.10).

The circuit configuration of the STATCOM can be either a basic six–pulse, two–level GTO thyristor inverter or a six–pulse, multi–level inverter, and corresponding high–pulse number connections. In contrast with the M–STATCOM, it is easier to investigate the effect of the dc voltage ripple on the operation of the two–level inverter type of STATCOM although the analytical techniques are identical.

To investigate the effect of the dc current ripple on the harmonic spectrum of the inverter output voltage, detailed calculations have been conducted. Some typical analytical results are tabulated in Table 5 .1 , in which the harmonic distortion factors are compared based on the configurations of the pulse number, dc capacitor values and the inverter voltage levels. The harmonic distortion factor defined below (5.24) gives the ratio of the rms value of the harmonic content normalized to the fundamental over the range of non–triple odd harmonics from 5th to 103th while for the arrangement of the twelve–pulse inverter, all of the $6(2n+1)\pm1$ harmonics are counted out as they can be cancelled by the star–delta transformer connections.

$$DF = \sqrt{\sum_{n=5}^{103}\left(\frac{H(n)}{n \cdot H(1)}\right)^2} \qquad (5.24)$$

Table 5 .1 : Effect of dc ripple on harmonic spectrum of the nine–level inverter

| Configuration | Capacitor | Inverter level | DF % |
|---|---|---|---|
| Six–pulse Inverter | ∞ (No ripple) | Two | 4.64 |
| | | Nine | 0.19 |
| | 1000 μ F | Two | 4.32 |
| | | Nine | 1.35 |
| Twelve–pulse Inverter | ∞ (No ripple) | Two | 1.50 |
| | | Nine | 0.05 |
| | 1000 μ F | Two | 1.48 |
| | | Nine | 0.17 |

To summarize the above results, we found:

- It was obvious that the high–pulse number connections could significantly reduce the harmonic components in the inverter output voltages. The larger the pulse number is, the better the performance will have.
- There were clear advantages in the decrease of the harmonic distortion factors by using the multi–level inverter.
- It seemed that the dc voltage ripples had no big effect on the harmonic spectrum of the output voltage for the two–level inverter. However,

it became clear that the harmonic distortion factors of the multilevel inverter output voltages would be greatly increased when dc voltage ripples were included. In other words, the dc capacitor size of the M–STATCOM would affect the harmonic spectrum of the inverter output voltage.

- The further investigation of the multilevel inverter indicated that a large ripple on the dc capacitor could re–introduce those lower order dominant harmonics which had been eliminated by the fundamental frequency switching method on the basis of the constant dc voltages.

## 5.4 CHAPTER SUMMARY

This chapter presents a simple analytical method to calculate the current ripple on the dc capacitor of the STATCOM, which is suitable for the analysis of all types of configurations, including the basic two–level, six–pulse structure, multilevel inverter arrangement, and their corresponding high–pulse number connections. The conclusions indicate that the dc voltage ripple and the corresponding harmonic spectrum in the STATCOM will be affected by the circuit configuration and the dc capacitance of the inverter. It is easy to limit the dc voltage ripple and the harmonic components by simply using high–pulse number connections. It is also found that the advantage of having a lower harmonic distortion factor could be damaged by using a smaller dc capacitance in the design of the M–STATCOM as a large ripple on the dc capacitor could re–introduce those lower order dominant harmonics which have been eliminated by the FFS method on the basis of the constant dc voltages. The analytical method and the solutions presented in this paper can be useful to conduct further investigation of the subject.

# *Chapter 6*
# Control of the multilevel inverter

## 6.1 CONTROL STRATEGIES

The detailed control system analysis to determine the response of a STATCOM using either the fundamental frequency switching or PWM techniques is given in [25] which also includes the analysis of negative sequence and harmonic voltage components in the transmission system.

Generally speaking, there are two types of control strategies which can be used in the voltage–sourced STATCOM. One is to keep the amplitude factor of the dc–side voltage to the ac–side voltage constant. The only available control input is the angle of the inverter voltage corresponding to the ac source voltage. The other varies instantaneous values of both the amplitude factor of the dc–side voltage to the ac–side voltage and the phase angle between the two voltages for control purposes.

For the multilevel inverter type of STATCOM, the balanced control of the individual dc capacitor voltage is also needed, especially during abnormal conditions.

## 6.2 MAIN CONTROL LOOP

The main control loop for the M–STATCON is shown in Figure 6.1 , in which there are two basic control loops. One establishes and maintains synchronism between the output voltage of the inverter and the ac system voltage. The other adjusts the phase angle between them to control the flow of real power into and out of the capacitor to vary the capacitor's voltage and, hence, the inverter's output voltage and the reactive power flow.

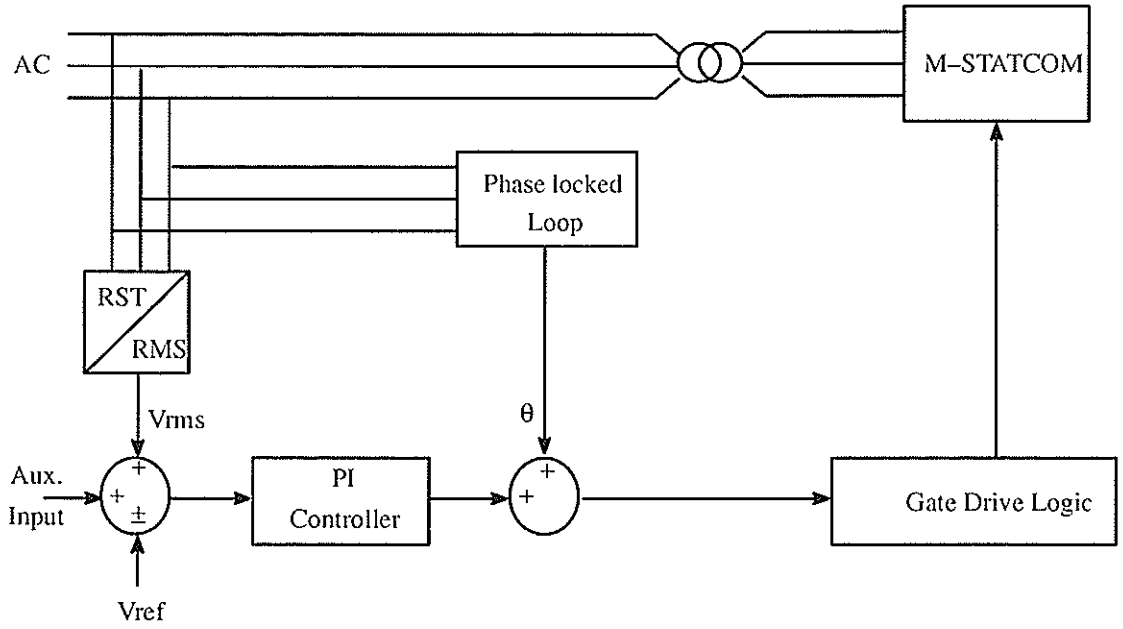



*Figure 6.1 : Basic Control Loop for the M–STATCOM*

To establish and maintain synchronism between the output voltage of the inverter and the ac system voltage, a phase locked loop ( PLL ) is used. The input to the PI controller is the error signal resulting from the difference between the rms value of the measured ac system voltage and the voltage reference. The dynamic adjustment of this reference can be achieved by the auxiliary input signal. The output of the PI controller, representing the var demand of the ac system, is added together with the output of the phase locked loop to adjust the angular reference signal fed to the Gate Drive Logic. The main function of the Gate Drive Logic is to maintain the FFS angles and produce the desired firing pulse order. One important

element of this control is the PLL. As explained later, the continuous sampling or d–q–z grid control circuit type of PLL is used in this scheme because it offers superior immunity from disturbances and harmonic distortion on the commutation voltage [26].

## 6 .3 PHASE LOCKED LOOP

In order to convert the firing angle order demanded by the control system into accurate firing pulses, it is important to extract the positive sequence fundamental frequency waveform from the system voltage. However, voltage distortions due to harmonics, faults and other disturbances may make extraction of this fundamental component very difficult. Traditional PLL circuits are based on the equidistant pulse firing techniques using a voltage controlled oscillator (VCO) which gives a satisfactory performance in most situations [27]. However, harmonic instability problems are noted when the ac systems are very weak.

The PLL, called d–q–z grid control circuit, used in this study was described in [26], which is shown in Figure 6 .2 .

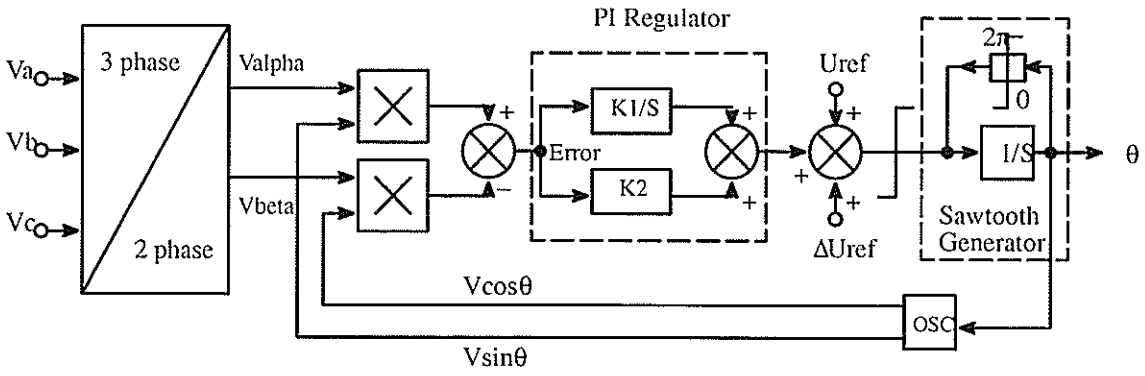



*Figure 6 .2 : A d–q–z Grid Control Circuit*

The three phase system voltages are transformed into two phase voltages in quadrature using a three–phase to two–phase transformation. The values of sinθ and cosθ are calculated and compared to the two phase voltages from the systems to close the control loop. The Error signal is acted upon by a PI controller which is followed by a VCO to derive

the reference angle, θ, of the system voltage. The nominal frequency of the VCO is controlled by a reference voltage. The dynamic modulation of this reference voltage can be accomplished by the input $\Delta U_{ref}$. The output of the VCO, which is limited between 0 to $2\pi$, generates the reference angle, θ, which is used to derive the firing pulses for the STATCOM.

The d–q–z control type of PLL has excellent immunity from either loss of synchronizing voltages or harmonic distortion. This is useful for the STATCOM which is often required to operate with weak ac systems that are subject to distorted synchronizing voltages.

## 6.4 SECONDARY CONTROL LOOP

Besides the above controls, the series connection of the capacitors in the M–STATCOM will require additional control loops for the following reasons.

1. The voltage across each level is subject to drift if there is any jitter in the gate firing or PLL circuits, or if there are non–characteristic harmonics on the system.

2. If each capacitance is not exactly equal, the voltage of each level will be different and require a control to establish a balance.

In order to maintain the voltage balance within the capacitors, secondary control loops are required to measure and compare the voltage of each capacitor level to the set value and to adjust the firing angle of the thyristors at that level only.

As an example, Figure 6.3 shows a simple principle loop for the balance control of the capacitor voltages, in which each capacitor voltage is measured and compared with an average capacitor voltage and then, passing through a limiter, the signal is fed to a PI controller. The output of the PI controller is used as an auxiliary input to adjust the firing angle of the thyristor which is clamped by the specific capacitor. Because of the difference of the operating condition, the reactive current may flow in or out of the compensator, and hence the sign of this input signal will vary with the sign of the vars. For example, if thyristor

$Q_2$ is switched on and off slightly earlier than prescribed, the capacitor $C_2$ alone will charge if the compensator is supplying reactive power. As a result, the voltage across capacitor $C_2$ will be increased slightly. On the other hand, if the compensator is absorbing reactive power, then advancing the firing of $Q_2$ will discharge capacitor $C_2$ only.

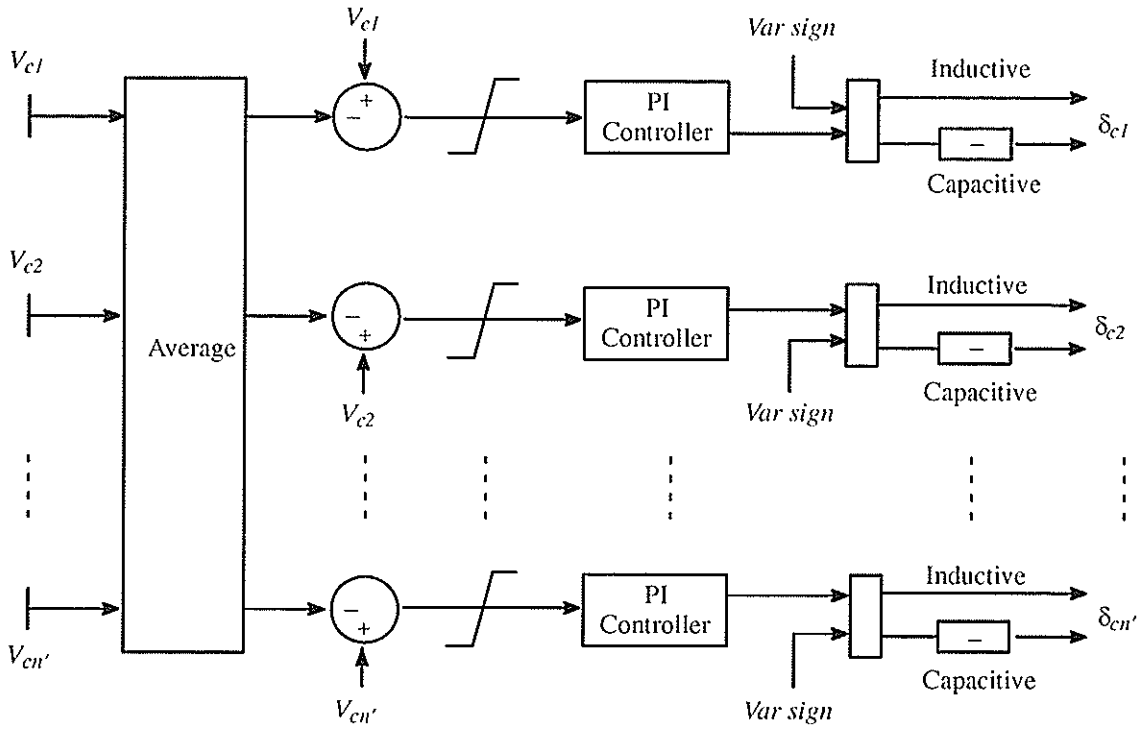



*Figure 6 .3 : The Capacitive Voltage Control Loop*

## 6 .5 METHOD OF PRE–CHARGING THE INVERTER

Traditionally, the start–up of the STATCOM requires a separate dc power source and a start–up converter to charge the dc capacitors and energize the connected transformer of the inverter. One economic and convenient approach is to use the ac system to start–up the system directly because the reverse–conducting diodes of the GTO thyristors in the inverter, form an ideal six–pulse bridge rectifier. If the inverter is connected to the ac system while the GTO thyristors are blocked, the dc capacitor of the inverter will be charged by the ac system voltage through the reverse–conducting diodes of the GTO thyristors, thereby the

constant dc capacitor voltage can be established. However, there may be overcurrent problems caused by the charging current of the dc capacitor or overcharging of the capacitors because of the leakage reactance of the transformer.

To avoid these problems, a pre–insertion resistor is used in the pre–charging circuit.

## 6.6 CHAPTER SUMMARY

The nature of the control for the M–STATCON is the same as used in the traditional STATCOM, which can be viewed as producing a voltage phasor behind a reactance, with the ability to adjust both magnitude and phase in a rapid manner. However, to achieve fast transient response speed and superior immunity from disturbances and harmonic distortions, a d–q–z control type of PLL is selected in the main control. The system side start–up of the M–STATCOM method is investigated in order to reduce the overall size and cost. Particularly, for the purpose of the balanced control of the individual dc capacitor voltage, a special control loop is developed.

The design principles and actual functions of above control systems will be tested in the next chapter for the cases of the steady state and the transient state operation of the M–STATCOM.

# *Chapter 7*
# Test studies

Based on the above analysis and discussion, a seven–level GTO thyristor inverter ( SLI ) using the fundamental frequency switching method was chosen as a candidate design of M–STATCOM in this chapter. The investigation will study the operating characteristics of the M–STATCOM in areas such as: start–up of the inverter, steady state performance of the device, transient response of the PLL, dynamic behavior of the STATCOM, and balance control of the capacitor voltages. The study results are obtained through electromagnetic transient simulation using the EMTDC$^{TM}$ program [28].

## 7 .1 TEST SYSTEM

To demonstrate the basic operation features of the design and to show the effects of the suggested control strategies, a single phase equivalent circuit of the test system used in this study is shown in Figure 7 .1 . The system consists of an infinite power source, an inductance representing the transmission line and a switched resistive / inductive load. The

M–STATCOM is situated at the load with a transformer. When the load is changed, the reactive power output of the compensator has to change in order to maintain the system voltage at the desired level. The scale of this compensator is set so that the load change would result in a swing from fully inductive to fully capacitive operation. The parameters of this test system and of the controls are given in Appendix D.

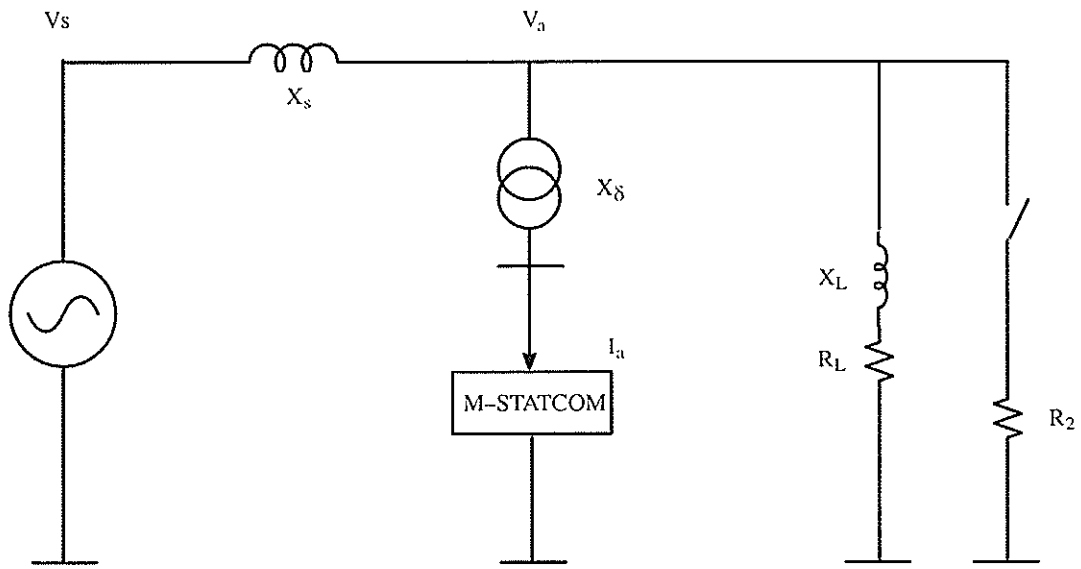



*Figure 7 .1 : A Schematic Diagram of the Test System*

## 7 .2 OPERATIONAL CHARACTERISTICS

### 7 .2 .1 START–UP OF THE STATCOM

To evaluate the possibility of starting the M–STATCOM from the ac system side directly, two tests were performed using a switch between the ac system and the STATCOM. Figure 7 .2 shows the current and voltage of the inverter during the start–up of the STATCOM without including a pre–insertion resistor, in which the switch between the ac system and the STATCOM is turned on at 0.02s. The STATCOM is fired at around 0.05s thereby the inverter voltage is established. As expected, the pre–charging current of the inverter is noticed, which gives the peak of 1.5 pu. It should be mentioned that the capacitor

size of the inverter has been reduced to limit the charging current. In other words, using large capacitance on the dc side of the inverter will result in increasing the peak value of the pre–charging current.

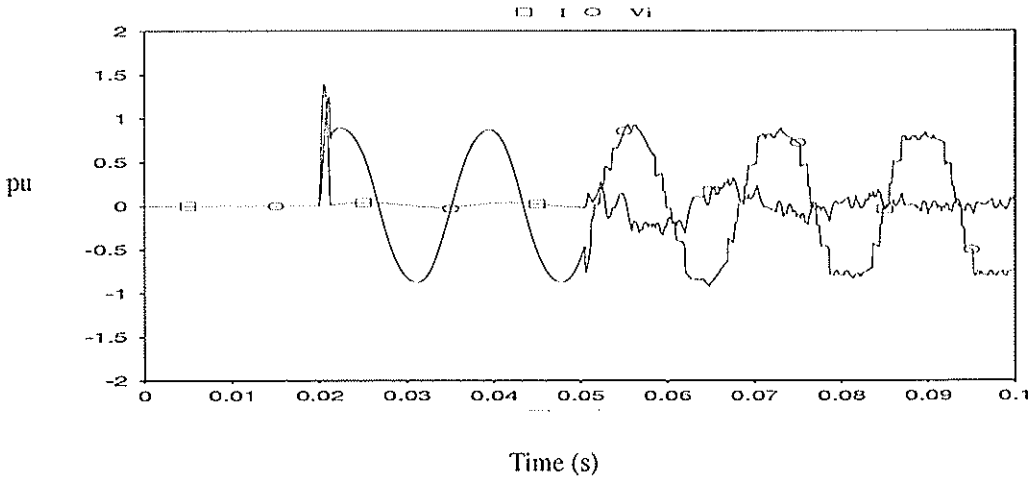



*Figure 7 .2 : The Current and Voltage of the Inverter during the Start–up without a Pre–insertion Resistor*

In contrast with the above case, the pre–charging current of the inverter is eliminated when a pre–insertion resistor is used. As shown in Figure 7 .3 , the pre–insertion resistor is first connected between the ac system and the STATCOM at 0.01s, then, at 0.02s, the main switch between the ac system and the STATCOM is turned on while the resistor circuit is shorted. It is clear that the start–up of the STATCOM from the ac system side is very successful when the pre–insertion resistor is used.

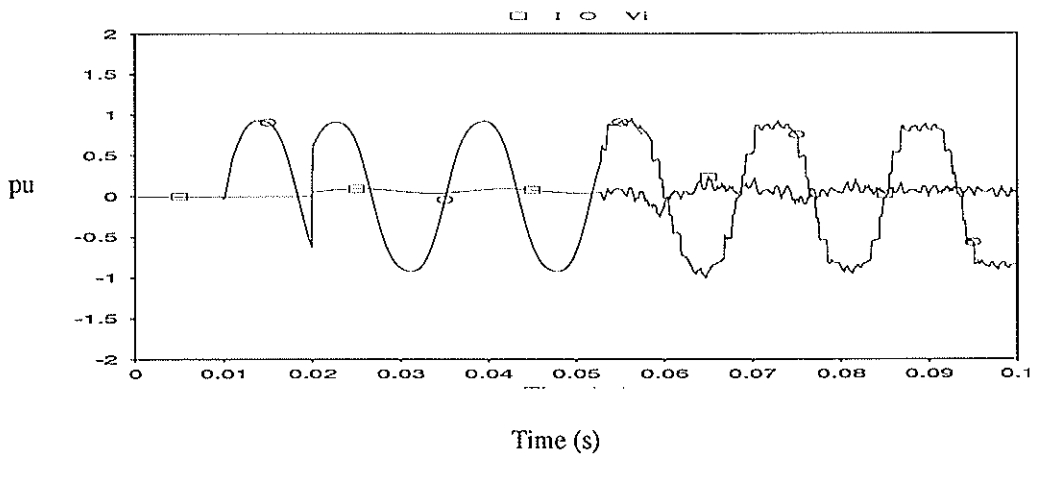



*Figure 7 .3 : The Current and Voltage of the Inverter during the Start–up with a Pre–insertion Resistor*

## 7 .2 .2 STEADY STATE OPERATION

Figure 7 .4 and 7 .5 show the inverter voltage and current of the compensator at both inductive and capacitive operating points during steady state operations. As expected, the staircase type of the inverter voltage is clearly seen because of the application of the fundamental frequency switching method. Both the lagging and the leading reactive currents are also shown in the figures. The results also show that the currents were very sinusoidal without filters or a high pulse number connection. The Fourier analysis of the currents tells us that the highest noticeable harmonic is the 13th as the 5th, 7th, and 11th harmonics are cancelled by the FFS method, which shows the advantage of this type of design and control strategy.

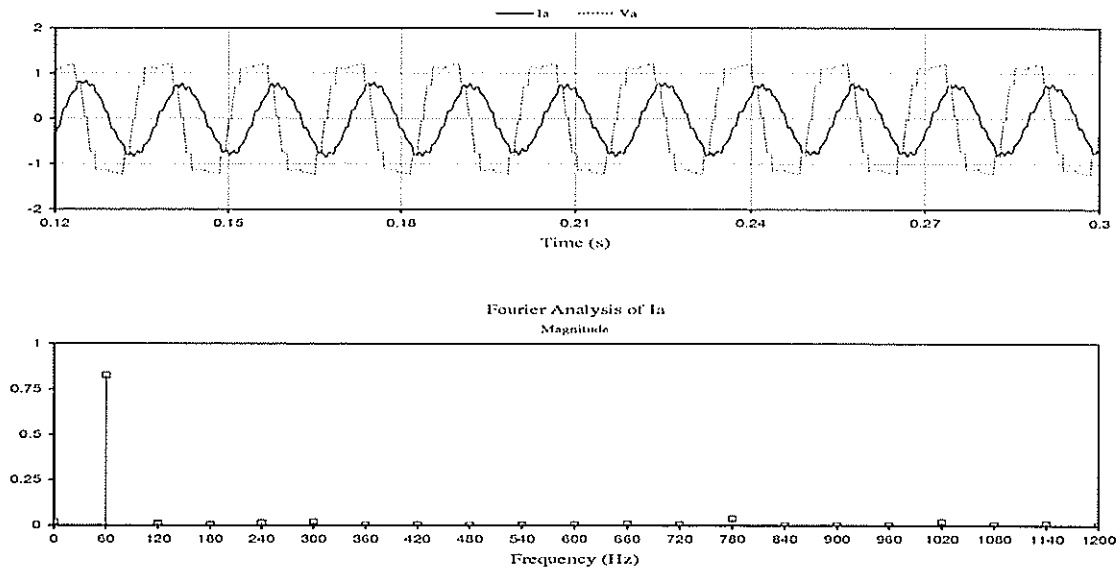



*Figure 7 .4 : Output Voltage and Current of SLI using FFS : Inductive Operation*

## 7 .2 .3 TEST ON THE PLL

The operational characteristics of the d–q–z grid control type of PLL when subjected to the loss of synchronizing voltages or harmonic distortion in the synchronizing voltages were discussed carefully in [26]. The following test was performed when the ac system was

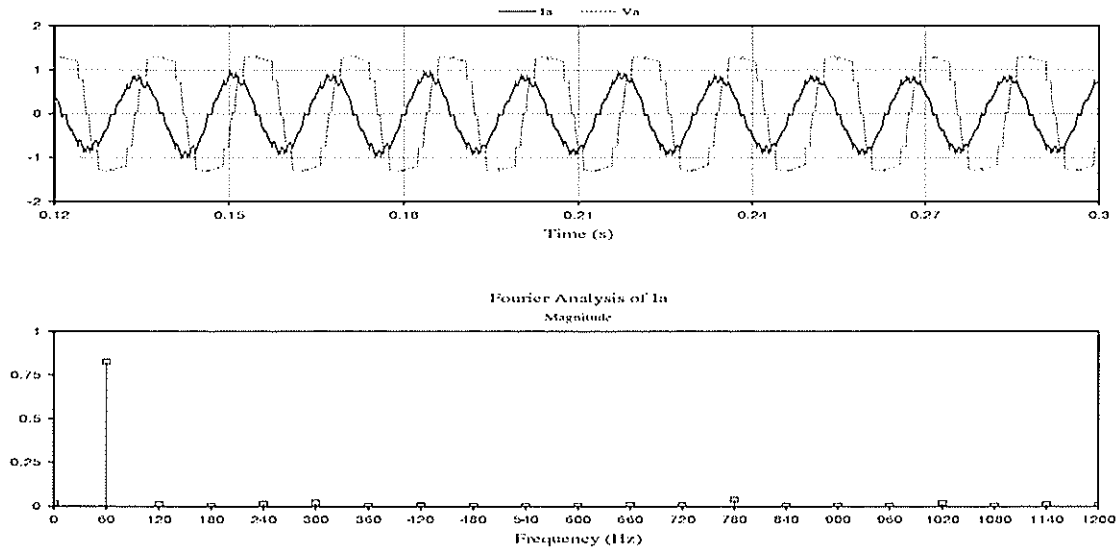



*Figure 7 .5 : Output Voltage and Current of SLI Using FFS : Capacitive Operation*

connected to the STATCOM. As shown in Figure 7 .6 , the synchronization of the fundamental voltage ( V_fund ) and the output signal of the PLL ( V_Theta ) occurred within one cycle after close of the switch. It indicated that the transient response of the PLL is rapid.

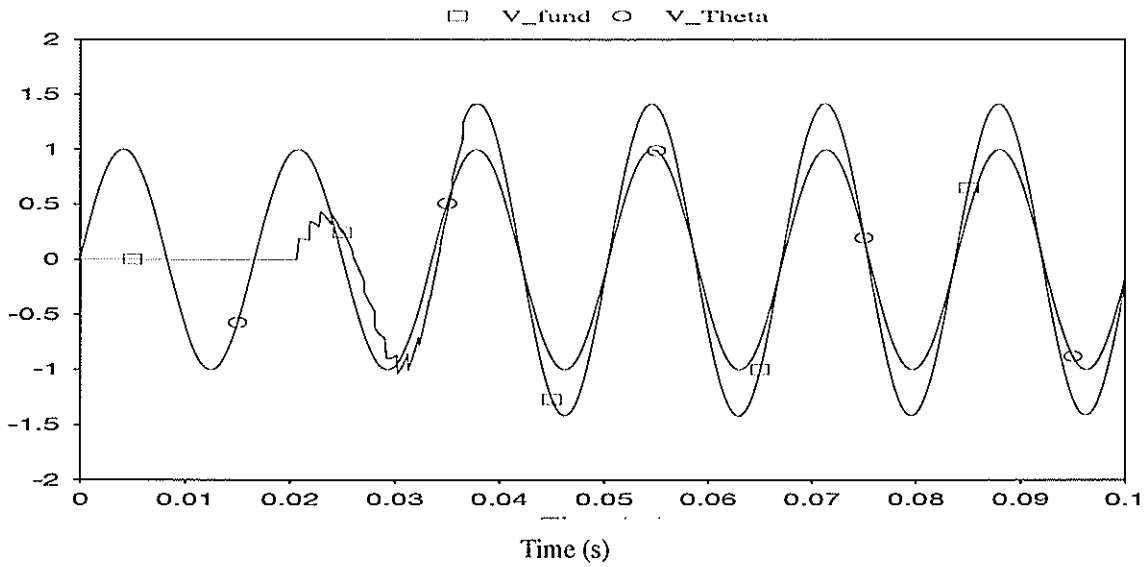



*Figure 7 .6 : Test on the PLL when the STATCOM Is Switched on*

## 7 .2 .4 TRANSIENT OPERATION

To illustrate the transient response of the compensator, Figure 7 .7 shows waveforms of the terminal voltage, $V_a$, and compensator current, $I_a$, during the switching of the load as well as the rms load voltage, $V_{rms}$. The figure indicates that when the load is suddenly increased, both the load voltage and its phase change dramatically, which requires the phase locked loop and voltage control loop to follow these changes rapidly. The simulation results show that the phase locked loop and simple proportional–integral controller can respond to load voltage changes and because of that, the reactive current of the compensator is quickly adjusted from the lagging to the leading state so that the load voltage is returned to rated value within two cycles of the system frequency (60 Hz).

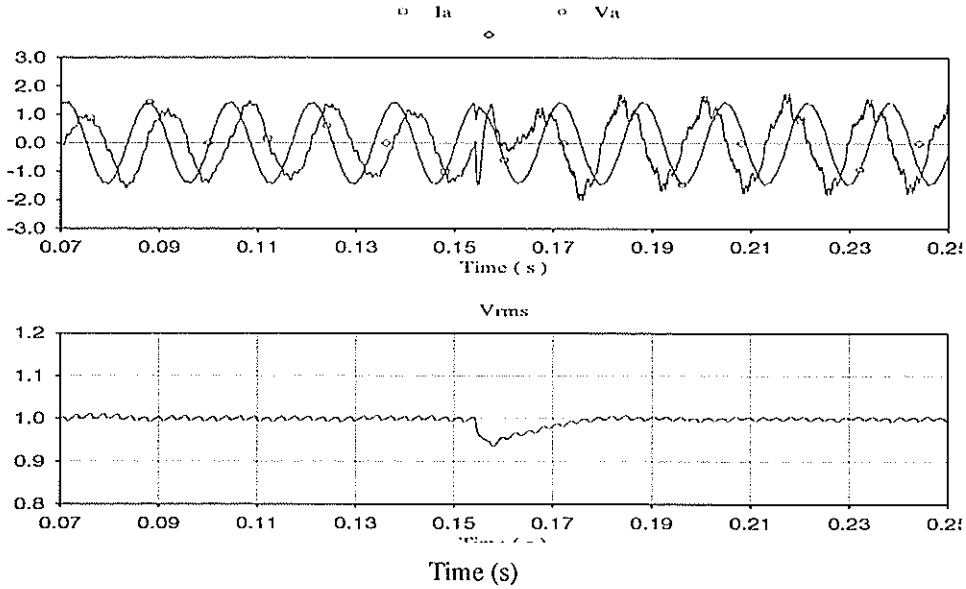



*Figure 7 .7 : Transient response of the M–STATCOM*

## 7 .2 .5 VOLTAGE BALANCE CONTROL FOR CAPACITORS

To illustrate the capacitor voltage balancing controls, one capacitor, $C_2$, was set 10% smaller than other five capacitors. As a result, the voltage on $C_2$ was little bit higher than that on other capacitors before the switching of the GTO thyristors. After the GTO thyristors were fired, the capacitor voltages would drift without the secondary control loops, as shown

in Figure 7 .8 . For the convenience of observation, the upper three capacitor ( i.e. $C_1$, $C_2$ and $C_3$ ) voltages and the lower three capacitor ( $C_4$, $C_5$ and $C_6$ ) voltages are separated in the figure. As a comparison, Figure 7 .9 gives the same results with the secondary control loops on. It is clear that the drift voltages can be returned to the desired level, and all six capacitor voltages can also be maintained at the same value because of the efficient control action of the secondary control loops.

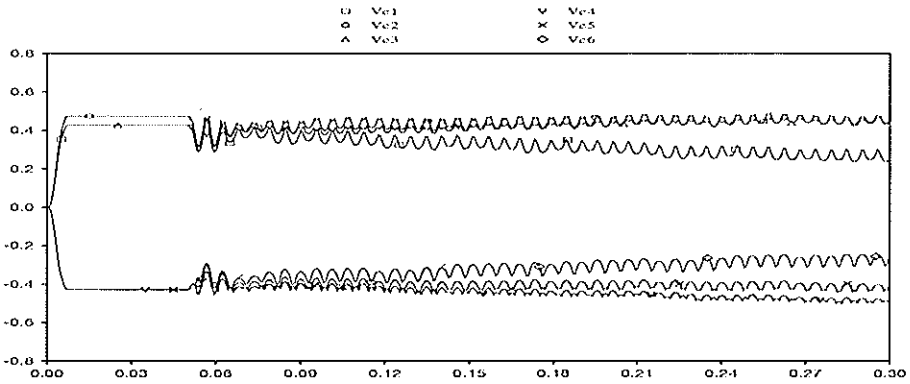



*Figure 7 .8 : Capacitive Voltages Without the Secondary Control Loop*

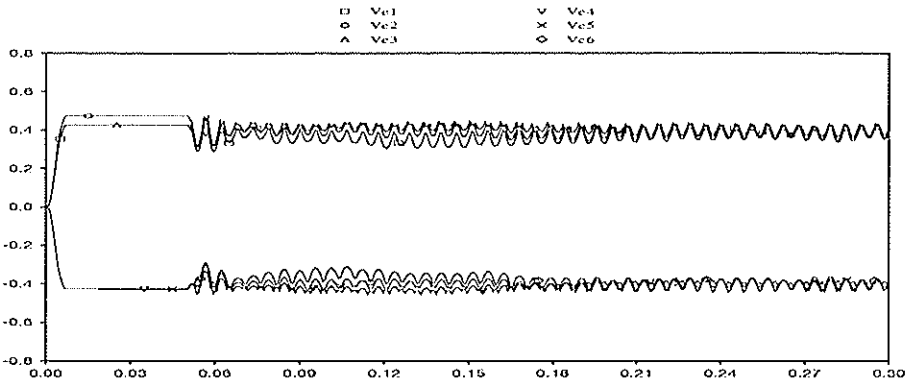



*Figure 7 .9 : Capacitive Voltages With the Secondary Control Loop*

## 7 .3 CHAPTER SUMMARY

In this chapter, a candidate design of M–STATCOM was tested using the EMTDC™ program. The simulation results indicated that the design of the M–STATCOM is technically and practically feasible. The points which have been confirmed can be summarized as follows:

- The M–STATCOM is able to start–up from the ac system side directly without overcurrent.
- The fundamental frequency switching of the GTO thyristor inverter produces a staircase type waveform which has benefits in reducing the harmonic distortion and the switching losses.
- The superior performance of the steady state and the dynamic state operation of the M–STATCOM can be achieved with the simple control loops.
- The fast continuous variation of the output power from fully capacitive to inductive is possible.
- The design of the capacitor balancing control loop is very effective.

Based on above study results, the M–STATCOM will be put in a large system for further testing in order to demonstrate the operation characteristics of the design over a wider range.

# *Chapter 8*
# Performance at an HVDC Inverter

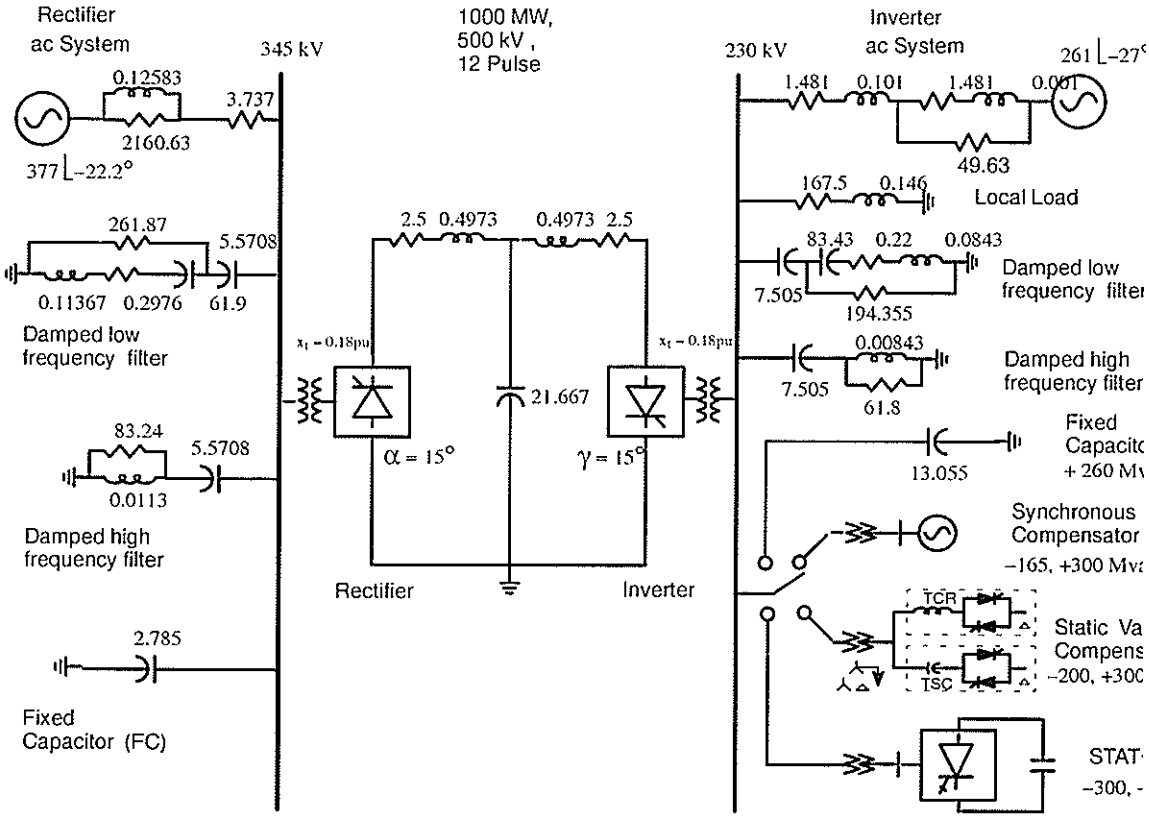
This chapter will investigate the dynamic performance of the M–STATCOM at a high voltage direct current (HVDC) converter terminal where the ac system has a very low short circuit ratio (SCR). The STATCOM is based on a nine–level GTO thyristor inverter. The studies include operating characteristics of the M–STATCOM under various ac and dc disturbances. The simulation results are compared with other types of reactive power compensation options available for such applications.

## 8.1 STUDY SYSTEM

This study is an extension of Dr. O.B. Nayak's research work [29], in which three conventional compensators were considered for the purpose of comparison: fixed capacitors (FC), a synchronous condenser (SC), and a static var compensator (SVC). The settings and controls of these compensators are the same as those used in above reference paper. In this study the operation of the STATCOM as the compensation device is compared to the best results achieved in the paper [29].

The study system is identical to the system described in [29], which was developed using the CIGRE benchmark model [30] as a reference system since it is easy to establish a common basis for comparative performance studies.

As shown in Figure 8 .1 , the study system is a 1000 MW, 500 kV, 12 pulse, monopolar cable HVDC system. The following are the most significant differences between the benchmark system and the study system:




All Resistances in Ω, Inductances in *H*, Capacitances in μ *F*

*Figure 8 .1 : Study System*

1. The study system has a very weak receiving ac system (SCR = 1.5) whereas the benchmark system has a relatively stronger receiving end (SCR = 2.5).

2. In order to keep the reactive power generated locally to the same level as the var demand of the inverter, the ac filters at the inverter side were resized to 300 Mvar while keeping their impedance profile very similar to that in the benchmark.

3. The study system has the ability to choose between the fixed capacitor, FC, of the benchmark and the other dynamic reactive power compensators (SC, SVC, M–STATCOM) as shown in Figure 6 .1.

4. The following modifications to the dc controls were made for the proper operation of the system:

i. Introduction of a 20 ms lag in the measurement of the current error signal to the gamma regulator.

ii. The converter firing angle is forced to 135° and gradually ramped back for clearing the dc faults.

iii. To avoid multiple commutation failures, the inverter firing angle was forced to a minimum value on detection of the first commutation failure, and then gradually ramped up so that the control is smoothly transferred back to the valve group controller.

The study system has been scaled to operate at 60 Hz (North American Standard) as comparing to 50 Hz in the benchmark system. Further details can be obtained from [29].

## 8 .2 STUDY CASES

### 8 .2 .1 RATINGS OF COMPENSATORS

The highest temporary overvoltage (TOV) at the inverter ac bus during permanent dc block is 1.7 pu with fixed capacitors and filters connected. A dynamic compensator of 160 Mvar inductive can bring the TOV to 1.1 pu without switching the filters. The capacitive rating of the compensators to fully compensate for the reactive power requirement at the inverter bus at rated power and voltage (so as to obtain unity power factor at the inverter bus looking into the ac system) is 260 Mvar. Hence a compensator of –160, +260 Mvar will meet the above requirements. However, dynamic compensators of slightly higher ratings than this

have been used here to provide some additional control range, especially during undervoltage conditions.

### 8.2.2 COMPENSATION SCHEMES

1. Fixed Capacitors (FC) Only, Base Case: This scheme will be used as the base case for comparing the performance of other schemes. Only fixed capacitors of 260 Mvar are used in this scheme along with 300 Mvar filters to fully compensate the inverter at the rated power.

2. Synchronous Condenser (SC) Only: In this scheme only a synchronous condenser of rating –165, +300 Mvar is used as the dynamic voltage control device at the inverter bus of the study system. At steady state, the filters supply 300 Mvar and the synchronous compensator supplies the remaining 260 Mvar.

3. Static Var Compensator (SVC) Only: Here, two static var compensators of rating –100, +150 Mvar each are used as the dynamic voltage control devices at the inverter bus of the study system. At steady state, the filters supply 300 Mvar and the SVCs supply the remaining 260 Mvar. The SVC controller uses a 3% droop as in the case of the SC. The proportional and integral gains of the SVC controller [31] are chosen to obtain the fastest possible SVC response without jeopardizing the stability of the system.

4. SC and SVC Sharing Equally: The synchronous condenser and one SVC are connected to the inverter bus in this scheme with the rating of the SC halved to 150 Mvar. In steady state the SC and SVC each supply 130 Mvar. Filters supply 300Mvar, as in other two cases.

5. STATCOM Only: In this study, a basic six–pulse, nine–level STATCOM with a step down transformer ( the turns ratio is 230 kV / 13.8 kV ) is used. This STATCOM has the ability to supply 90 Mvar reactive power. However, for comparison purposes a 300 Mvar STATCOM is needed. To meet this demand, an increased number of levels or multiples of

the basic STATCOM probably in a multi–pulse connection would be used. To limit the complexity of the model, a basic six–pulse, nine–level STATCOM with an ability to produce $\pm$ 300 Mvar reactive power is assumed in this study. Since the STATCOM behaves symmetrically the inductive rating is equal to the capacitive rating.

A disadvantage of using a six–pulse STATCOM is that the harmonics on the dc side are not reduced and, hence, there is a considerable voltage ripple on the capacitors. In order to keep the voltage ripple on the dc side down to an acceptable level, an increased capacitive value ( C = 200, 000 μF ) is used. In this case the total energy stored in the dc side of the inverter is equal to 4.34 Mvar. However, compared with the 300 Mvar reactive power rating of the STATCOM, the dc capacitor size is small and can be reduced significantly if the multi–pulse bridge connections are used.

A STATCOM of $\pm$ 300 Mvar rating is used only for the dynamic control of the inverter voltage in this case. At steady state, the filters supply 300 Mvar and the STATCOM supplies the remaining 260 Mvar.

### 8 .2 .3 TYPES OF FAULTS STUDIED

The following types of disturbances are examined in this chapter:

1. Permanent dc Block
2. Inverter Close–in Faults
3. DC Line Fault
4. Inverter Remote Faults
5. Rectifier Close–in Faults

## 8 .3 SIMULATION RESULTS

The results presented next for the conventional compensation devices are taken directly from the models developed in the Ph.D thesis of O.B. Nayak [32].

## 8 .3 .1 PERMANENT DC BLOCK

When a permanent dc block is applied to the inverter, a temporary overvoltage will take place for all schemes of conventional compensation. The best option is the SC and SVC combination, which gives a first peak of 1.5 pu. The response time is 173 ms. The oscillations exist for both the SC case and the mixed case as well.

Figure 8 .2 shows a comparison of the inverter rms voltage between the STATCOM and the mixed scheme of the SC and SVC. The interesting observation is that there is no temporary overvoltage at all with the STATCOM. This is because when terminal voltage attempts to increase while the inverter voltage of the STATCOM remains constant, the current flow is automatically reversed and the STATCOM serves as an inductor. There is also other phenomena occurring at the same instant such as a phase shift between the system and inverter voltage which causes a momentary discharge of the dc capacitors until the phase lock loop firing controls return to synchronization, and this leads to further inductive action.

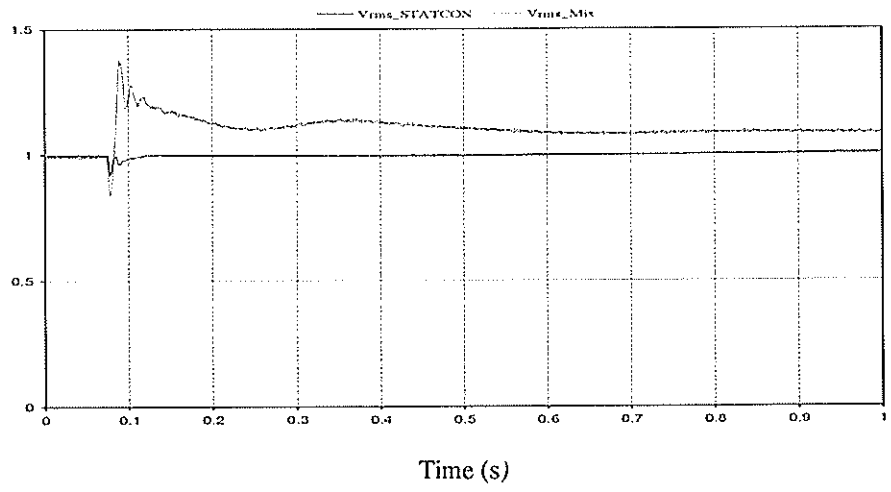



*Figure 8 .2 : Inverter ac rms Voltage during a Permanent dc Block*

Figure 8 .3 shows the instantaneous voltages in one phase in order to see the difference of the magnitude of the first peak.

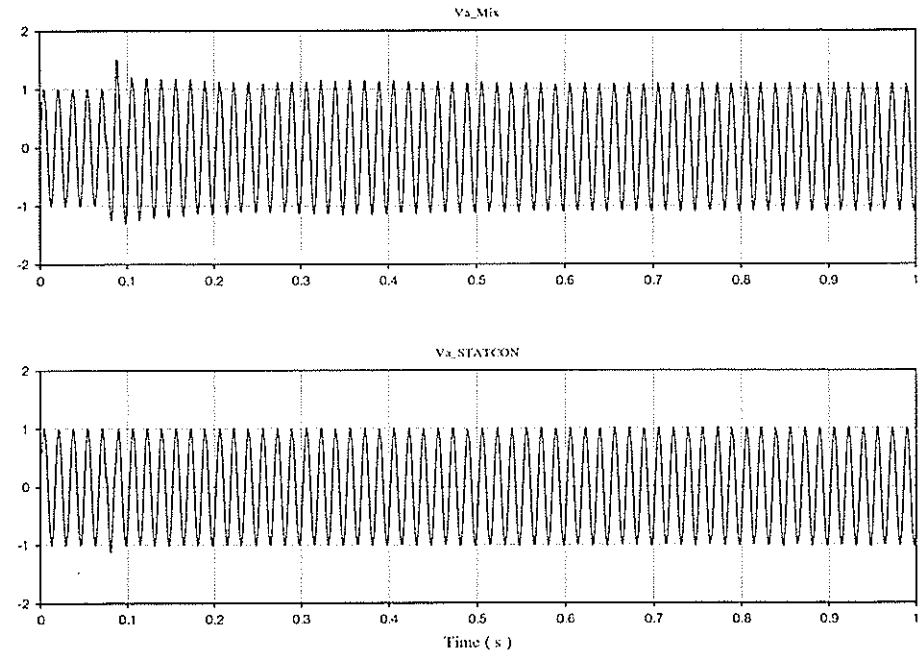



*Figure 8 .3 : Phase A Voltage during a Permanent dc Block*

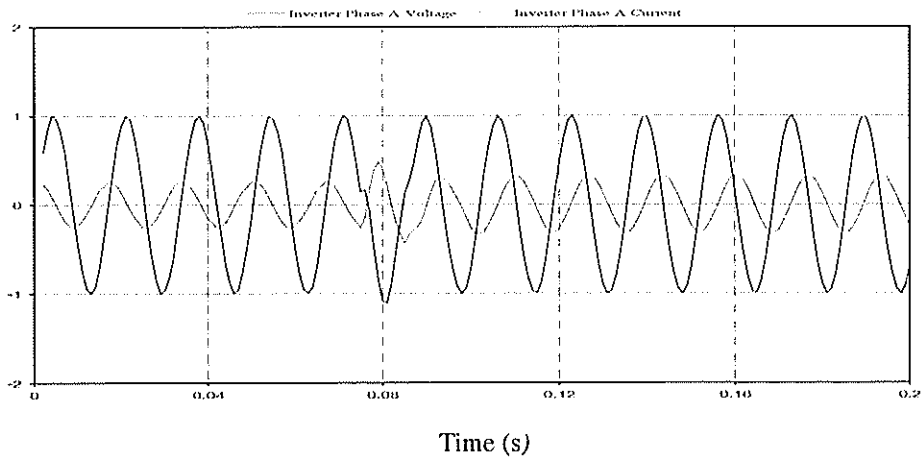



*Figure 8 .4 : Phase A Voltage and Current of STATCOM during a Permanent dc Block*

Figure 8 .4 gives a clear picture of dynamic performance of the STATCOM during a permanent dc block. It is obvious that the phase angle of the system voltage is suddenly shifted with respect to the inverter voltage when the disturbance happens. As a result, the output reactive current of the STATCOM is quickly changed from leading to lagging, which brings the terminal voltage back to the normal within one cycle. Another observation can be made here is that the output current of the STATCOM is very sinusoidal without any filters.

### 8 .3 .2 INVERTER CLOSE–IN FAULTS

The study of the inverter faults includes a three–phase to ground fault and a single line to ground fault. The investigation using the conventional compensation found that the cases with the SC or the mix of the SC and the SVC gave the fastest power recovery time. However, the SVC only case exhibited the poorest dynamic performance. This is due, in part, to the action of the commutation failure protection circuit, which is necessary for preventing repeated commutation failures. The reason for the resulting multiple commutation failures is that the ESCR of the system is suddenly reduced by the dynamic contribution of the SVC. Immediately after the fault is cleared, the SVC senses the low voltage as the ac voltage is recovering, causing the thyristor controlled reactors to back off while keeping all the capacitors on.

Unlike the SVC, the use of the STATCOM for the inverter close–in faults will not result in repeated commutation failures because of its different structure. The equivalent circuit of the STATCOM during the inverter faults is that of a voltage source behind a small inductance (the transformer leakage). This feature increases the system ESCR rather than decreasing it. From this point of view, the STATCOM behaves like the SC. Furthermore, if the case is of concern only for a short time, even better performance than the SC can be achieved because the leakage inductance of the transformer is usually of the same order as the sub–transient reactance of the SC, which will make the ac system much stronger (higher ESCR) during transients. The simulation studies have confirmed that this is true.

#### 8 .3 .2 .1 Three–Phase to Ground Fault

Figure 8 .5 shows the inverter dc power during a five cycle three–phase to ground fault at the inverter bus for the cases of the SC and the STATCOM. As shown in the figure, the power recovery time of the STATCOM is shorter than the SC. Table 8 .1 gives the dc power recovery time to 80% of pre–fault power in all schemes.

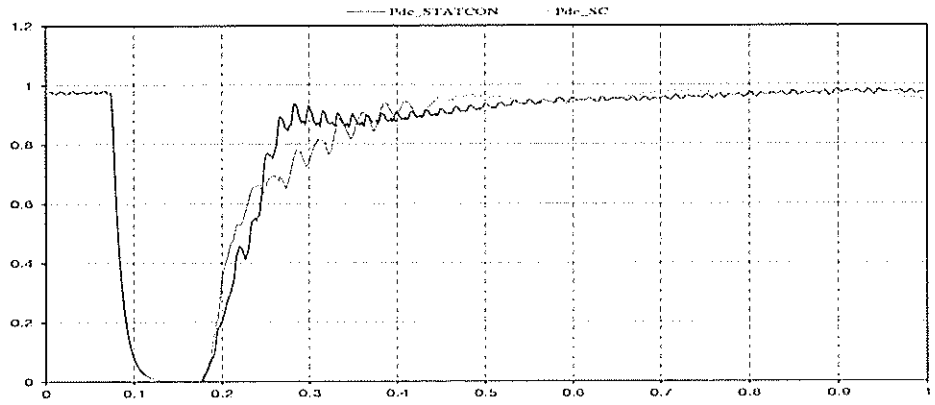



*Figure 8 .5 : Inverter dc Power during a Five Cycle Three Phase to Ground Fault at the Inverter Bus*

Table 8 .1 : Recovery Times of the dc Power during a Three Phase to Ground Fault at Inverter Bus

| FC | SC | SVC | SVC+SC | STATCOM |
|---|---|---|---|---|
| 235 ms | 135 ms | 485 ms | 135 ms | 100 ms |

## 8 .3 .2 .2 Single–Phase to Ground Fault

Figure 8 .6 shows the inverter dc power during a five cycle single line to ground fault at the inverter bus for the cases of the mix of the SC and the SVC, and the STATCOM. Like the three–phase to ground fault, the dc power recovery with the STATCOM is better than the mix of the SC and the SVC during the single line to ground fault (In order to maintain the terminal voltage at the rated value, the recovered dc power is slightly less than the original value). And also, the oscillation of the power is greatly reduced because of the smooth adjustment of the firing angle in the control of the STATCOM. Table 8 .2 gives the dc power recovery time to 80% of pre–fault power in all schemes.

Table 8 .2 : Recovery Times of the dc Power during a Single Phase to Ground Fault at Inverter Bus

| FC | SC | SVC | SVC+SC | STATCOM |
|---|---|---|---|---|
| 235 ms | 135 ms | 485 ms | 135 ms | 100 ms |

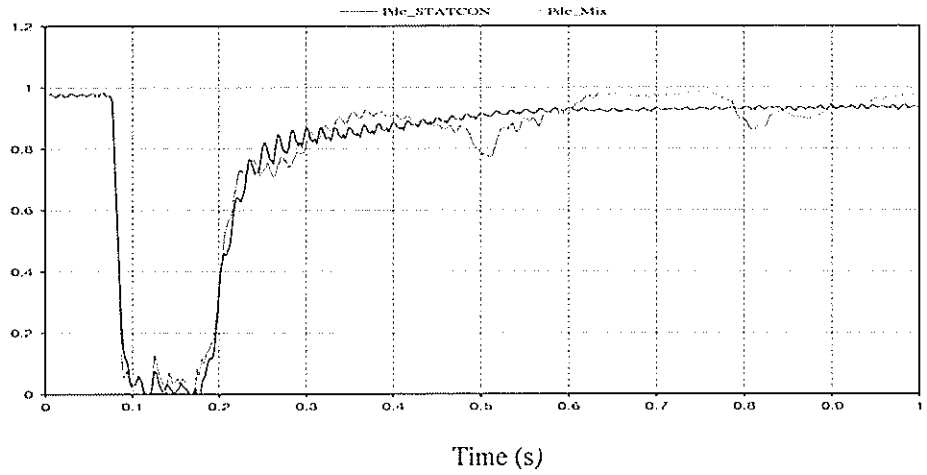



*Figure 8 .6 : Inverter dc Power during a Five Cycle Single Phase to Ground Fault at the Inverter Bus*

## 8 .3 .3 DC LINE FAULT

The dc fault studied is created by short circuiting the dc line to ground at the mid–point of the dc cable. The faults on the dc side are cleared by the force–retard circuit, by which the converter firing angle is forced to 135° and gradually ramped back so that the normal control modes take over.

The studies indicated that there was overvoltage for all conventional compensation schemes during the dc line fault because the dc power was reduced to zero and the reactive power consumption of the inverter is dramatically reduced. The studies also showed that the FC option had the best voltage recovery ability in this case.

Figure 8 .7 gives a comparison of the inverter rms voltage between the STATCOM and the FC during the dc line fault. Obviously, the behavior of the STATCOM is not the same as the conventional compensators. There is no overvoltage here because the STATCOM functions as an inductor when the dc power is suddenly reduced. With the faster response of the control, the inverter voltage can be quickly recovered after the fault is cleared.

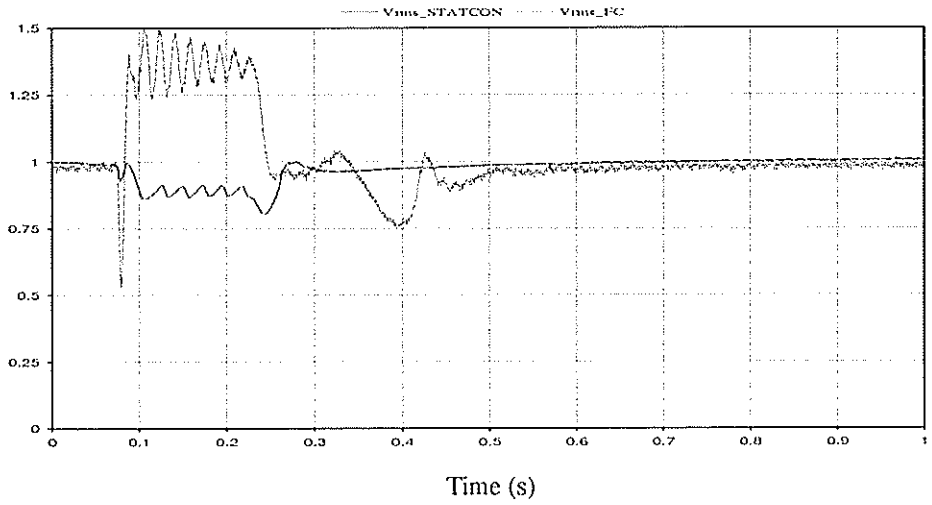



*Figure 8 .7 : Inverter rms Voltage during a dc Line Fault*

## 8 .3 .4 INVERTER REMOTE FAULTS

In the simulation, the ac system equivalent circuit was modelled in two identical sections connected in series. The remote faults are created by applying either a three–phase to ground or a single line to ground fault for five cycles at the junction of the two sections.

The dynamic performance of the remote faults is generally the same as that of the inverter close–in faults but with a smaller effect. As with the close–in faults the performance of the STATCOM is superior to all other conventional types of compensation.

## 8 .3 .5 RECTIFIER CLOSE–IN FAULTS

The single phase and three–phase to ground faults at the rectifier bus have been analyzed in the simulation. In general, the rectifier faults are not as severe as the corresponding inverter faults because the rectifier ac system is relatively stronger. Comparing the STATCOM with the conventional compensation, the former also exhibits clear advantages on the basis of the dynamic response time, voltage stabilization and dc power recovery.

## 8.4 CHAPTER SUMMARY

This chapter investigates the dynamic performance of the M–STATCOM at an HVDC converter terminal where the ac system has a very low short circuit ratio. The studies include operation characteristics of the M–STATCOM under various ac and dc disturbances. The simulation results are compared with other types of reactive power compensation options available for such applications. It is shown that the M–STATCOM offers superior performance in areas such as fault recovery time, limiting of temporary overvoltages and dc power recovery. While the other reactive power compensation devices, alone or in combination, may provide good dynamic performance for a certain type of fault, the M–STATCOM provides consistently equal or better performance under every type of disturbance studied.

# *Chapter 9*
# Conclusions and Future Work

## 9.1 CONCLUSIONS

Investigation of the multilevel GTO thyristor inverter as a STATCOM opens a new application area of GTO thyristor in power systems. The studies presented in this paper especially revealed the aspects of the design, control and the performances of the M–STATCOM, which have offered an interesting alternative to other circuit topologies being considered for the STATCOM. In other words, the development of the M–STATCOM shows great promise for the dynamic compensation of power transmission systems in both HVAC and HVDC systems.

The major conclusions, in itemized form, are now stated below:

1. Although the design of the multilevel GTO thyristor inverter was originally considered for motor applications, our studies have proven that it is practically and technically feasible as a STATCOM. On the other hand, the expensive individual dc supplies

to each voltage level of the inverter are necessary when it is used for a motor driver. However, the STATCOM does not require a separate dc supply and this makes the multilevel GTO thyristor inverter ideally suited to this application.

2. To control the output voltage of the multilevel GTO thyristor inverter, both the FFS method and PWM techniques were found to be ideally suited for this application. After a lot of calculation and analysis work was carried out, it is suggested that FFS method should be taken into first consideration as it results in a lower harmonic distortion and reduced switching losses.

3. Various options are available in selecting the optimum structure of the M–STATCOM, which depend mainly on the demand of the reactive power, the tolerance of the harmonic distortion, the limitation of the switching losses, and the transient response time of the output voltage. For the maximum size of the M–STATCOM (except higher pulse number connections), a nine–level GTO thyristor inverter should be considered. For getting a larger percentage of the fundamental voltage, a lower number of switching of the GTO thyristors, and better results of harmonic elimination, the FFS method shows clear advantages. For getting faster controllability, the PWM techniques may be better.

4. The overall control strategies for the M–STATCOM can be same as those of conventional STATCOM. It is found that good control response can be achieved by using a d–q–z grid controlled PLL and simple PI regulators. An extra secondary control loop for the capacitor voltage balance is required and was developed.

5. It is possible to use the system side start–up method to pre–charge the M–STATCOM without the need of a separate dc power source and a start–up converter, which could reduce the physical size of the device and the overall cost.

6. Functions of the dc capacitor in the STATCOM include to maintain the desired dc voltage, to establish an energy balance between the input and output during the dynamic

changes and to limit the ripple component in the output voltage of the inverter thereby the harmonic spectrum.

7. The main advantages of M–STATCOM over the current design of the inverter used for the STATCOM are:

- The voltage level can be increased without series connection of GTO thyristors and the necessity of simultaneous switching. Therefore, a higher reactive power output can be achieved (A nine–level STATCOM could have a rating of 92 Mvar reactive power at the voltage of 14.9 kV using currently available GTO thyristors without higher pulse number connections), which means this type of design is more practical for power transmission systems.
- The harmonic content of the output current can be greatly reduced without large harmonic filters and/or multiple–pulse bridge inverter connections, and thereby the harmonic losses and filter requirements are reduced.
- The preliminary study of the power loss in the M–STATCOM shows that the design of the multilevel GTO inverter has advantages to reduce overall power losses compared with the conventional structure of the STATCOM.
- The GTO thyristors in the M–STATCOM are well protected against the overvoltage as each individual GTO thyristor of the inverter is clamped to a dc capacitor voltage via clamping diodes.

8. The various simulation studies have shown that the M–STATCOM can provide for fast continuous variation of leading or lagging reactive power to power systems, and is very effective as a dynamic compensator for supporting the system voltage, increasing transient stability, and improving damping.

9. Application of the M–STATCOM at the commutation bus of a HVDC converter terminal feeding a very weak ac system indicates that the M–STATCOM is able to offer superior performance in areas such as fault recovery time, limiting of temporary overvoltages and dc recovery compared to other reactive power control devices available for such applications under every type of disturbance.

## 9.2 FUTURE WORK

The establishment and test of an experimental model of a M–STATCOM is recommended for the future work of this project.

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# APPENDIX A

Mathcad Programs for the Analysis of Five–level GTO Inverter

1. FFS method

2. SH–PWM technique

3. SFO–PWM technique

FFS Method for Five-level GTO inverter

$deg := \frac{\pi}{180}$ $wt := 0..360$ $n := 1,3..50$

Guess $\alpha 1 := 5$ $\alpha 2 := 30$

Given $\alpha 1 > 0$ $\alpha 2 > \alpha 1$ $\alpha 2 < 90$

$\cos(5 \cdot \alpha 1 \cdot deg) + \cos(5 \cdot \alpha 2 \cdot deg) = 0$

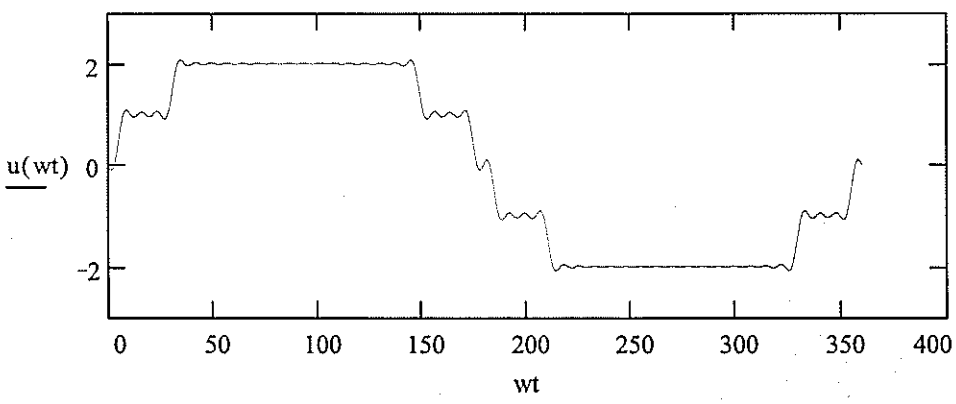
$\cos(7 \cdot \alpha 1 \cdot deg) + \cos(7 \cdot \alpha 2 \cdot deg) = 0$

$\begin{pmatrix} \alpha 1 \\ \alpha 2 \end{pmatrix} := Find(\alpha 1, \alpha 2)$ $\alpha 1 = 5.143$ $\alpha 2 = 30.857$

$$ud1(wt) := \frac{4}{\pi} \cdot \sum_n \frac{1}{n} \cdot \cos(n \cdot \alpha 1 \cdot deg) \cdot \sin(n \cdot wt \cdot deg)$$

$$ud2(wt) := \frac{4}{\pi} \cdot \sum_n \frac{1}{n} \cdot \cos(n \cdot \alpha 2 \cdot deg) \cdot \sin(n \cdot wt \cdot deg)$$

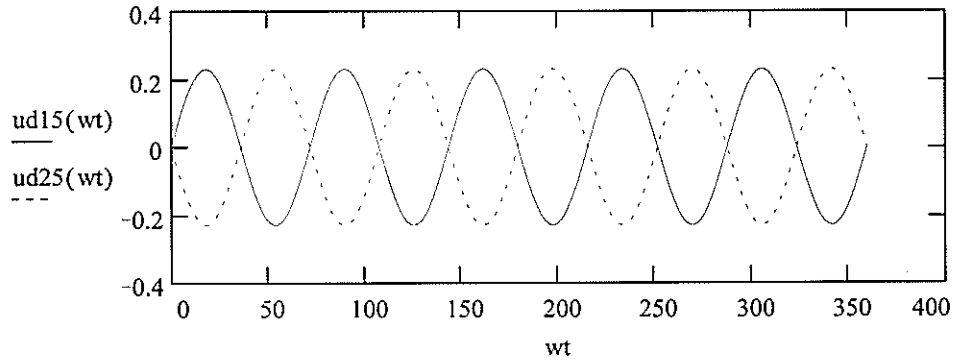
$u(wt) := ud1(wt) + ud2(wt)$

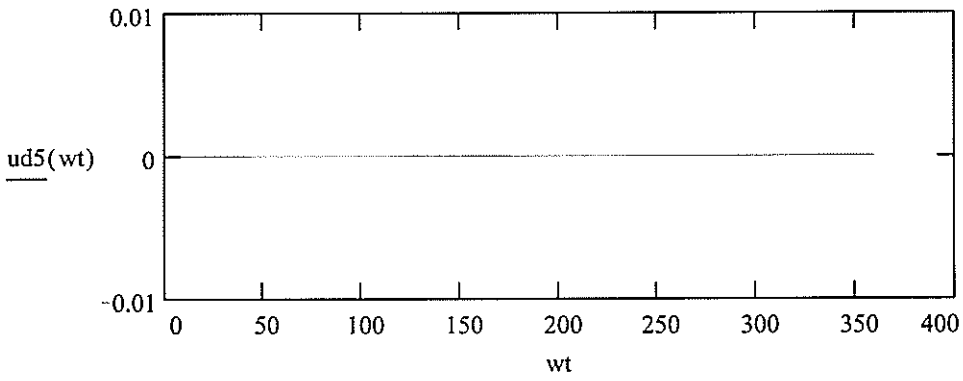


$$ud15(wt) := \frac{4}{\pi}\cdot\frac{1}{5}\cdot\cos(5\cdot\alpha1\cdot deg)\cdot\sin(5\cdot wt\cdot deg)$$

$$ud25(wt) := \frac{4}{\pi}\cdot\frac{1}{5}\cdot\cos(5\cdot\alpha2\cdot deg)\cdot\sin(5\cdot wt\cdot deg)$$

$$ud5(wt) := ud15(wt) + ud25(wt)$$

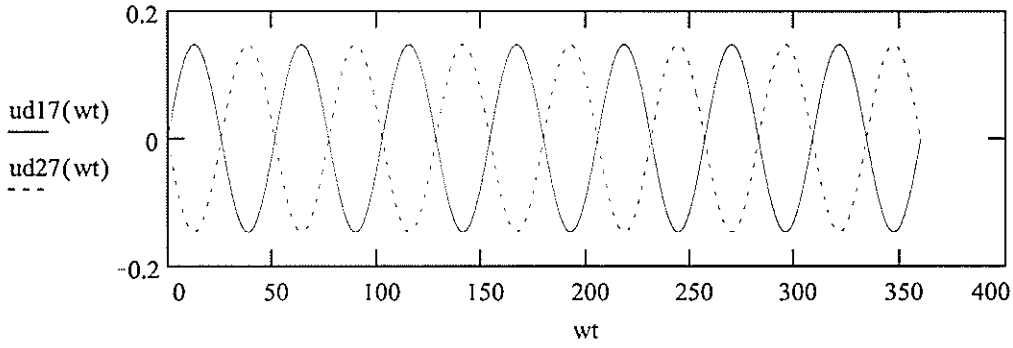


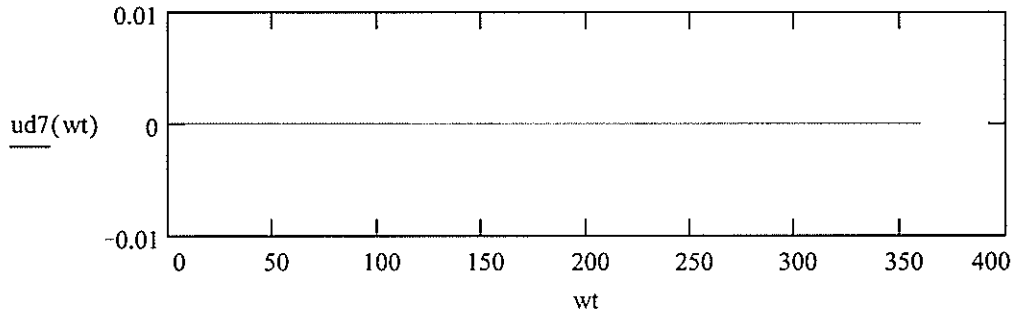




$$ud17(wt) := \frac{4}{\pi}\cdot\frac{1}{7}\cdot\cos(7\cdot\alpha1\cdot deg)\cdot\sin(7\cdot wt\cdot deg)$$

$$ud27(wt) := \frac{4}{\pi}\cdot\frac{1}{7}\cdot\cos(7\cdot\alpha2\cdot deg)\cdot\sin(7\cdot wt\cdot deg)$$

$$ud7(wt) := ud17(wt) + ud27(wt)$$



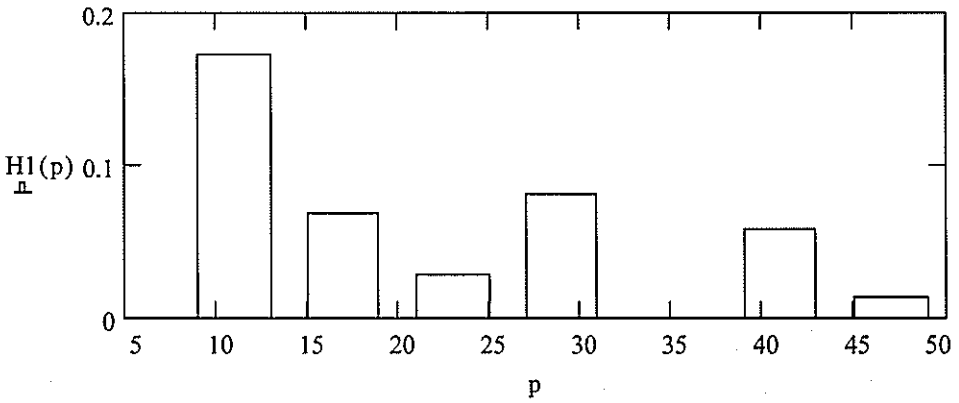



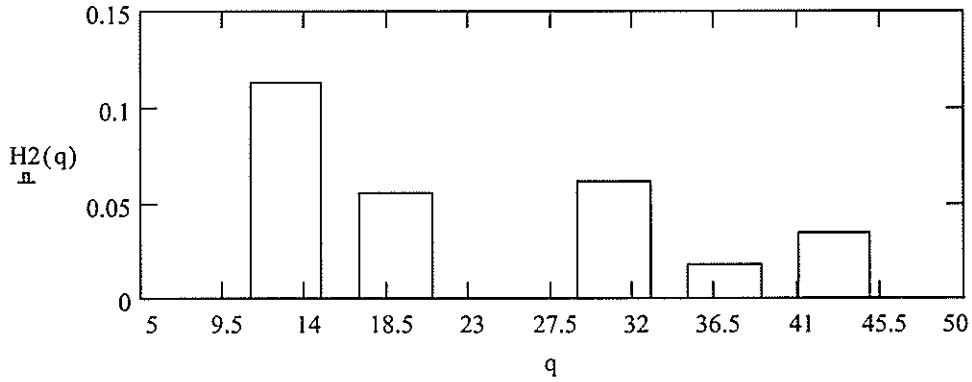

$p := 5, 11 .. 50$ $\quad q := 7, 13 .. 50$

$$DF1(p) := \frac{1}{p}\cdot\cos(p\cdot\alpha1\cdot deg) + \frac{1}{p}\cdot\cos(p\cdot\alpha2\cdot deg)$$

$$DF2(q) := \frac{1}{q}\cdot\cos(q\cdot\alpha1\cdot deg) + \frac{1}{q}\cdot\cos(q\cdot\alpha2\cdot deg)$$

$$H1(p) := \frac{4}{\pi}\cdot|DF1(p)| \qquad H2(q) := \frac{4}{\pi}\cdot|DF2(q)|$$






$$DF := \frac{\sqrt{\sum_{p}(DF1(p))^2 + \sum_{q}(DF2(q))^2}}{\cos(\alpha 1 \cdot deg) + \cos(\alpha 2 \cdot deg)}$$

$DF = 0.109$

SFO-PWM technique for FL1 with M=1, and K=9 and W-type carrier

$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 9$

$c(t,k) := \frac{-1}{\pi} \cdot \operatorname{asin}\left(\sin\left(k \cdot \omega \cdot t - \frac{\pi}{2}\right)\right)$

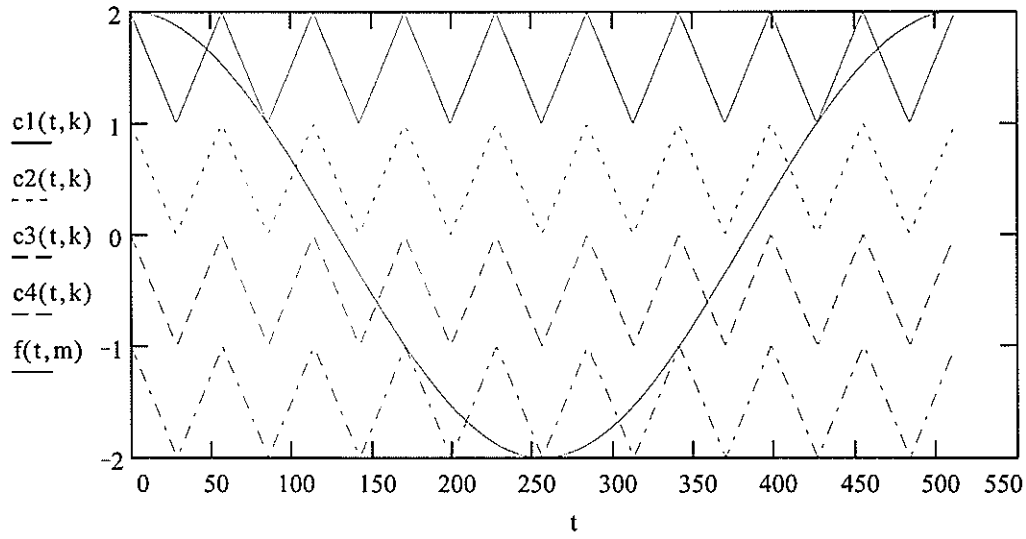
$c1(t,k) := 1.5 + c(t,k)$

$c2(t,k) := 0.5 + c(t,k)$

$c3(t,k) := -0.5 + c(t,k)$

$c4(t,k) := -1.5 + c(t,k)$

$f(t,m) := 2 \cdot m \cdot \cos(\omega \cdot t)$



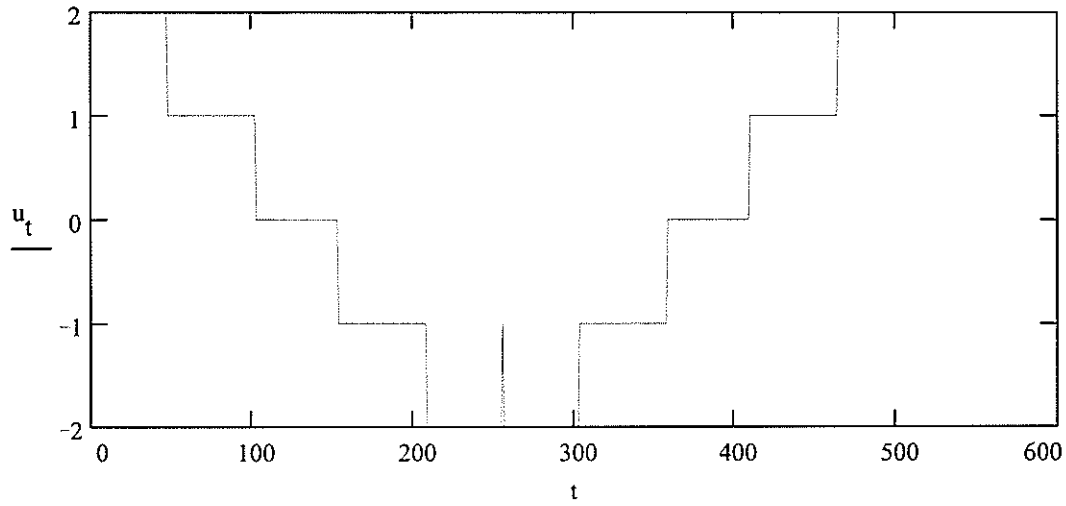

$u1(t,k,m) := -(\Phi(c1(t,k) - f(t,m)) - 1) + 1$

$u2(t,k,m) := -(\Phi(c2(t,k) - f(t,m)) - 1)$

$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$

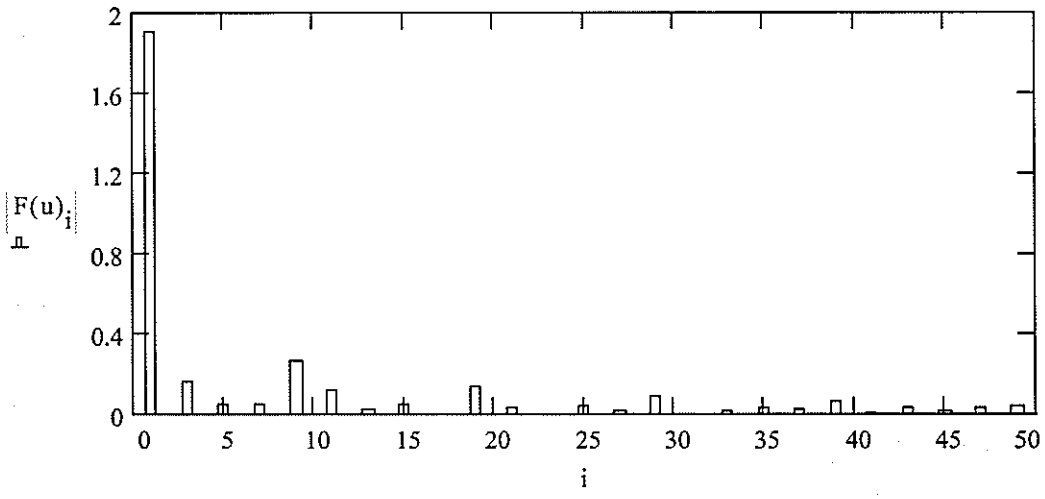
$u4(t,k,m) := \Phi(f(t,m) - c4(t,k)) - 2$

$u_t := u1(t,k,m)\cdot u2(t,k,m) - u3(t,k,m)\cdot u4(t,k,m)$

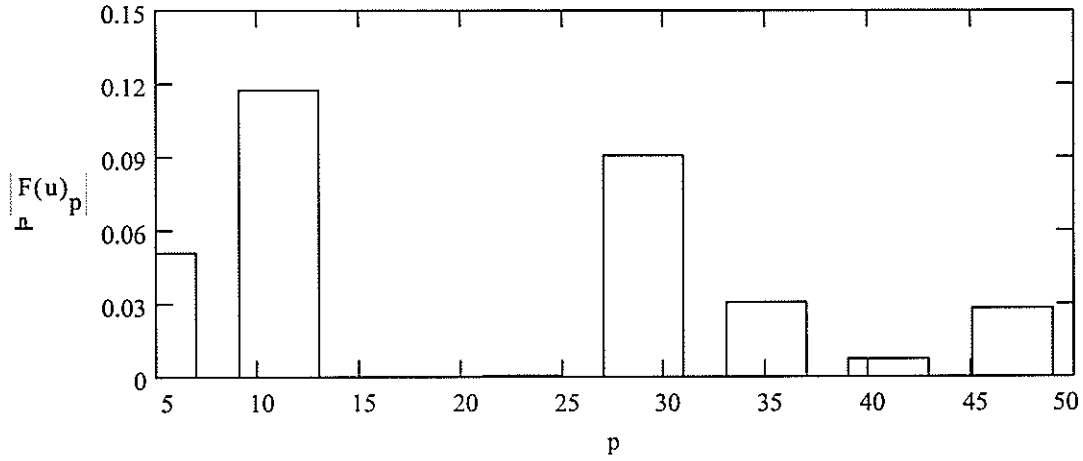


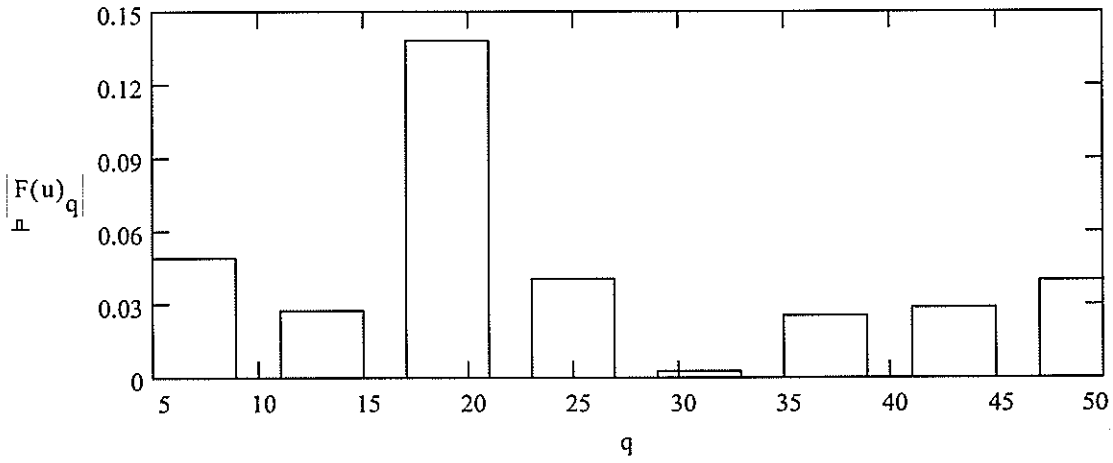

$i := 0..50$

$$F(u) := \frac{2j}{\sqrt{512}}\cdot(fft(u) - 2j\cdot Im(fft(u)))$$



$p := 5, 11 .. 50$ $q := 7, 13 .. 50$




$$DF := \frac{\sqrt{\sum_p \left(\left|F(u)_p\right|\right)^2 + \sum_q \left(\left|F(u)_q\right|\right)^2}}{\left|F(u)_1\right|}$$

$DF = 0.121$

SFO-PWM technique for FL1 with M=1, and K=9 and M-type carrier

$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 9$ $\beta := \frac{2\cdot\pi}{3}$

$f1(t,m) := 2\cdot m\cdot\cos(\omega\cdot t)$

$c(t,k) := \frac{1}{\pi}\cdot\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)$

$f3(t,k) := \begin{pmatrix} 2\cdot m\cdot\cos(\omega\cdot t) \\ 2\cdot m\cdot\cos(\omega\cdot t - \beta) \\ 2\cdot m\cdot\cos(\omega\cdot t + \beta) \end{pmatrix}$

$c1(t,k) := 1.5 + c(t,k)$

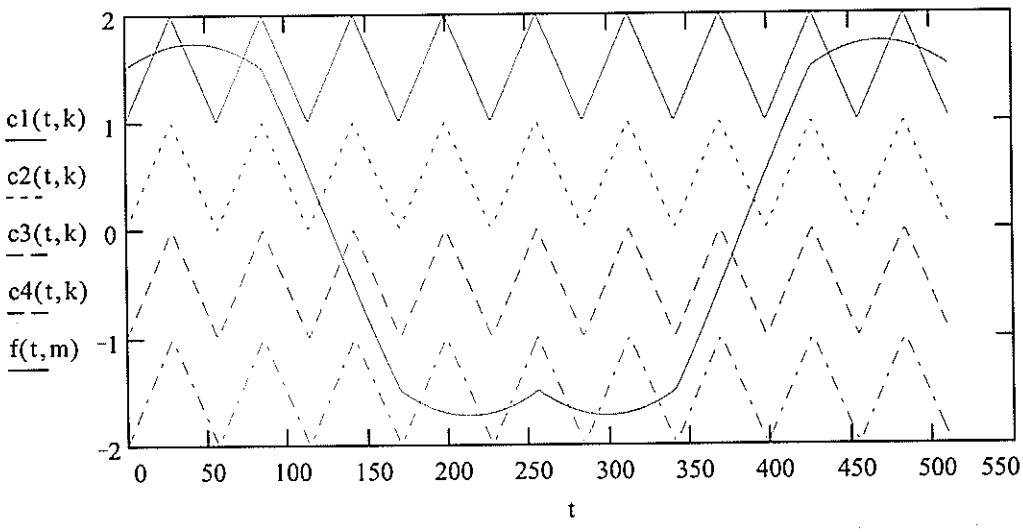
$c2(t,k) := 0.5 + c(t,k)$

$c3(t,k) := -0.5 + c(t,k)$

$c4(t,k) := -1.5 + c(t,k)$

$f0(t,m) := \frac{\max(f3(t,m)) + \min(f3(t,m))}{2}$

$f(t,m) := f1(t,m) - f0(t,m)$



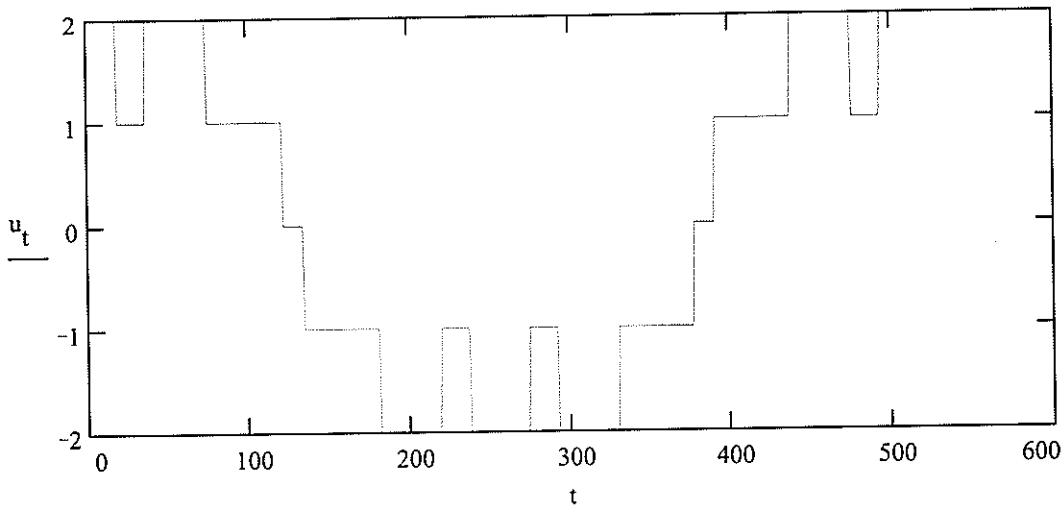

$u1(t,k,m) := -(\Phi(c1(t,k) - f(t,m)) - 1) + 1$

$u2(t,k,m) := -(\Phi(c2(t,k) - f(t,m)) - 1)$

$u3(t,k,m) := \Phi(f(t,m) - c3(t,k)) - 1$

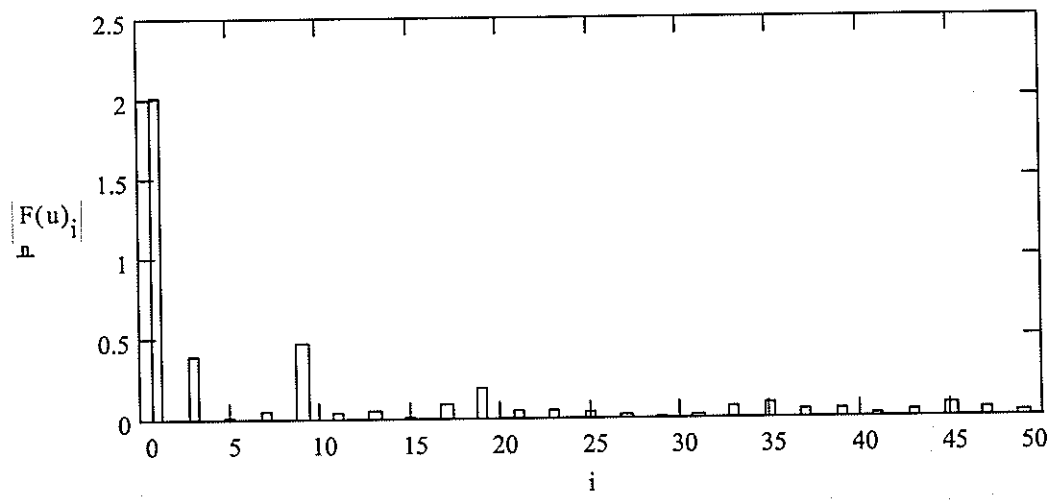
$u4(t,k,m) := \Phi(f(t,m) - c4(t,k)) - 2$

$u_t := u1(t,k,m)\cdot u2(t,k,m) - u3(t,k,m)\cdot u4(t,k,m)$

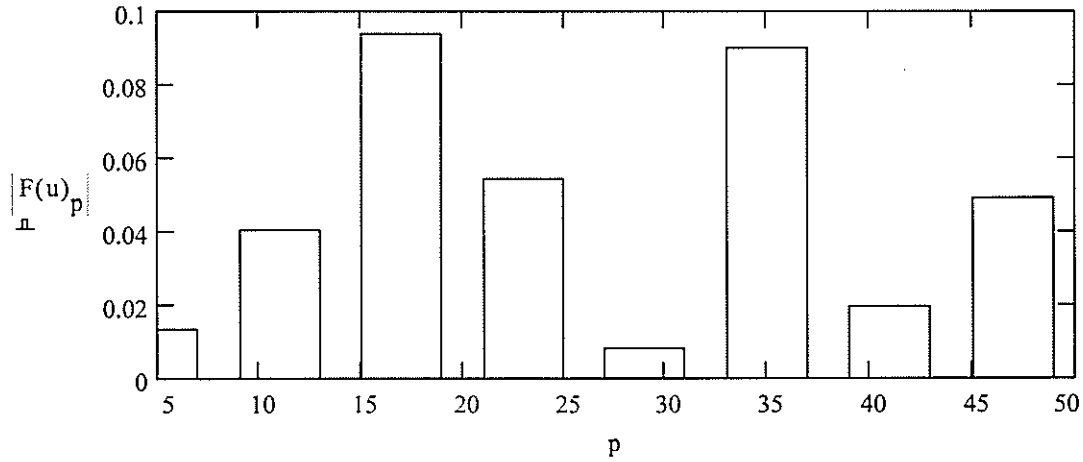


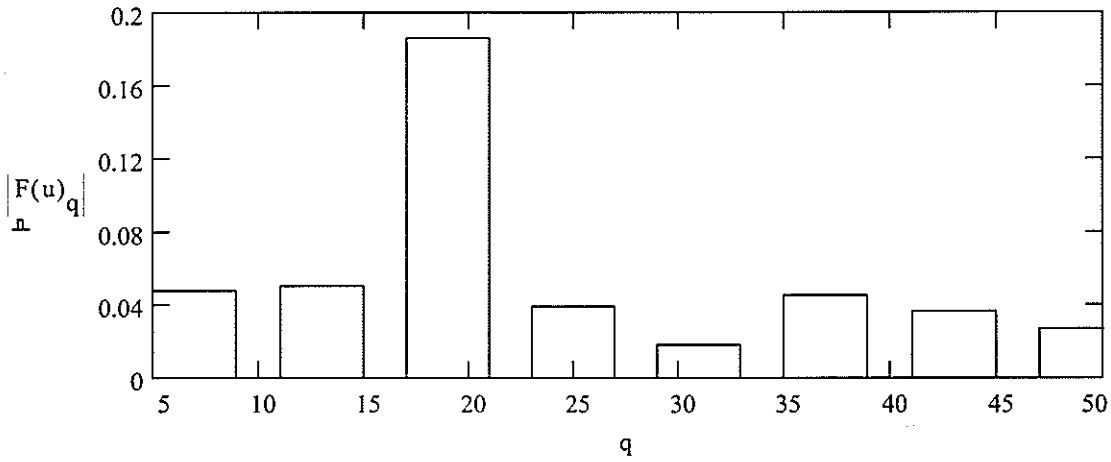

$i := 0..50$

$$F(u) := \frac{2j}{\sqrt{512}}\cdot(fft(u) - 2j\cdot Im(fft(u)))$$



$p := 5, 11 .. 50$ $q := 7, 13 .. 50$




$$DF := \frac{\sqrt{\sum_p \left(|F(u)_p|\right)^2 + \sum_q \left(|F(u)_q|\right)^2}}{|F(u)_1|}$$

$DF = 0.131$

# APPENDIX B

Typical Calculation Results for Both Seven–level and Nine–level Inverter

The typical calculating results using SH–PWM method for SLI

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.8 | W | 8 | 23% |
| | | M | 6 | 19% |
| | M = 0.875 | W | 8 | 23% |
| | | M | 6 | 19% |
| | M = 0.95 | W | 8 | 18% |
| | | M | 6 | 17% |
| | M = 1.0 | W | 8 | 14% |
| | | M | 6 | 15% |
| k = 9 | M = 0.8 | W | 12 | 9.4% |
| | | M | 6 | 10% |
| | M = 0.875 | W | 8 | 11% |
| | | M | 10 | 11% |
| | M = 0.95 | W | 8 | 6.9% |
| | | M | 10 | 9.3% |
| | M = 1.0 | W | 8 | 6.8% |
| | | M | 10 | 8.6% |
| k = 11 | M = 0.8 | W | 8 | 18% |
| | | M | 10 | 17% |
| | M = 0.875 | W | 8 | 18% |
| | | M | 14 | 24% |
| | M = 0.95 | W | 8 | 16% |
| | | M | 14 | 20% |
| | M = 1.0 | W | 8 | 14% |
| | | M | 14 | 15% |

The typical calculating results using SFO–PWM method for SLI

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.8 | W | 14 | 15% |
| | | M | 4 | 12% |
| | M = 0.875 | W | 10 | 17% |
| | | M | 8 | 17% |
| | M = 0.95 | W | 8 | 17% |
| | | M | 10 | 22% |
| | M = 1.0 | W | 8 | 18% |
| | | M | 10 | 23% |
| k = 9 | M = 0.8 | W | 10 | 11% |
| | | M | 8 | 11% |
| | M = 0.875 | W | 10 | 9.8% |
| | | M | 8 | 13% |
| | M = 0.95 | W | 12 | 11% |
| | | M | 10 | 13% |
| | M = 1.0 | W | 12 | 8.6% |
| | | M | 10 | 12% |
| k = 11 | M = 0.8 | W | 10 | 13% |
| | | M | 12 | 12% |
| | M = 0.875 | W | 14 | 18% |
| | | M | 8 | 15% |
| | M = 0.95 | W | 12 | 21% |
| | | M | 10 | 18% |
| | M = 1.0 | W | 12 | 21% |
| | | M | 10 | 18% |

The comparison between FFS method and PWM techniques for SLI

| Harmonic order | FFS | SH–PWM | | SFO–PWM | |
|---|---|---|---|---|---|
| | | W | M | W | M |
| 5 | 0 | 0.9% | 3.5% | 1.4% | 0.2% |
| 7 | 0 | 3.1% | 2.3% | 1.0% | 3.2% |
| 11 | 0 | 1.9% | 0.7% | 1.3% | 7.8% |
| 13 | 2.8% | 1.5% | 1.5% | 2.5% | 0.4% |
| 17 | 1.6% | 0.1% | 4.7% | 2.0% | 4.5% |
| 19 | 1.0% | 1.3% | 2.1% | 2.8% | 3.4% |
| 23 | 0.5% | 0.4% | 1.6% | 0.1% | 2.2% |
| 25 | 1.4% | 2.7% | 0.8% | 5.4% | 0.5% |
| 29 | 0.3% | 1.8% | 0 | 0.8% | 5.2% |
| 31 | 0.6% | 2.4% | 2.8% | 0.9% | 0.9% |
| 35 | 2.4% | 2.1% | 2.9% | 1.2% | 0.8% |
| 37 | 0.8% | 1.3% | 1.5% | 1.5% | 0.1% |
| 41 | 1.3% | 0.7% | 0.8% | 0.8% | 2.0% |
| 43 | 0.6% | 2.0% | 1.3% | 1.2% | 1.2% |
| 47 | 1.3% | 0.4% | 1.2% | 3.8% | 3.3% |
| 49 | 1.4% | 0.8% | 0.4% | 0.8% | 1.0% |
| DF | 5.9% | 6.8% | 8.6% | 8.6% | 12% |
| S. No. | 6 | 8 | 10 | 12 | 10 |

The typical calculating results using SH–PWM method for NLI

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.85 | W | 10 | 14% |
| | | M | 8 | 14% |
| | M = 0.9 | W | 10 | 13% |
| | | M | 8 | 15% |
| | M = 0.95 | W | 10 | 12% |
| | | M | 8 | 14% |
| | M = 1.0 | W | 10 | 11% |
| | | M | 8 | 12% |
| k = 9 | M = 0.85 | W | 10 | 7.2% |
| | | M | 8 | 7.2% |
| | M = 0.9 | W | 10 | 7.4% |
| | | M | 8 | 6.1% |
| | M = 0.95 | W | 10 | 8.6% |
| | | M | 8 | 7.8% |
| | M = 1.0 | W | 10 | 6.9% |
| | | M | 12 | 8.5% |
| k = 11 | M = 0.85 | W | 14 | 17% |
| | | M | 8 | 13% |
| | M = 0.9 | W | 10 | 14% |
| | | M | 12 | 14% |
| | M = 0.95 | W | 10 | 12% |
| | | M | 12 | 15% |
| | M = 1.0 | W | 10 | 11% |
| | | M | 12 | 12% |

The typical calculating results using SFO–PWM method for NLI

| Frequency ratio | Modulation index | Carrier type | S. No. | DF |
|---|---|---|---|---|
| k = 7 | M = 0.85 | W | 8 | 15% |
| | | M | 10 | 12% |
| | M = 0.9 | W | 16 | 13% |
| | | M | 6 | 7.7% |
| | M = 0.95 | W | 12 | 12% |
| | | M | 10 | 9.9% |
| | M = 1.0 | W | 12 | 12% |
| | | M | 10 | 13% |
| k = 9 | M = 0.85 | W | 12 | 8.8% |
| | | M | 10 | 9.3% |
| | M = 0.9 | W | 12 | 7.4% |
| | | M | 10 | 8.2% |
| | M = 0.95 | W | 12 | 7.2% |
| | | M | 10 | 7.8% |
| | M = 1.0 | W | 12 | 5.6% |
| | | M | 10 | 6.8% |
| k = 11 | M = 0.85 | W | 12 | 10% |
| | | M | 14 | 15% |
| | M = 0.9 | W | 12 | 8.1% |
| | | M | 14 | 10% |
| | M = 0.95 | W | 16 | 11% |
| | | M | 10 | 12% |
| | M = 1.0 | W | 16 | 13% |
| | | M | 10 | 12% |

The comparison between FFS method and PWM techniques for NLI

| Harmonic order | FFS | SH–PWM | | SFO–PWM | |
|---|---|---|---|---|---|
| | | W | M | W | M |
| 5 | 0 | 1.2% | 3.6% | 0 | 3.2% |
| 7 | 0 | 5.0% | 2.9% | 2.2% | 2.0% |
| 11 | 0 | 0.5% | 2.9% | 1.1% | 1.8% |
| 13 | 0 | 1.2% | 1.4% | 1.7% | 1.1% |
| 17 | 2.5% | 0.5% | 2.2% | 2.9% | 1.1% |
| 19 | 3.8% | 0.4% | 1.2% | 1.1% | 3.9% |
| 23 | 3.6% | 1.4% | 0.8% | 0.9% | 0.2% |
| 25 | 0 | 1.0% | 0.8% | 0.6% | 1.1% |
| 29 | 1.3% | 0.4% | 2.3% | 0.2% | 2.2% |
| 31 | 2.6% | 1.2% | 3.8% | 1.8% | 1.6% |
| 35 | 1.2% | 2.5% | 2.2% | 2.0% | 1.4% |
| 37 | 0.7% | 1.1% | 0.2% | 0.6% | 0.3% |
| 41 | 1.4% | 1.7% | 2.4% | 1.5% | 0.2% |
| 43 | 0.8% | 1.5% | 1.5% | 0.7% | 1.0% |
| 47 | 0 | 0.8% | 0.1% | 1.3% | 0.4% |
| 49 | 1.8% | 0.9% | 0.2% | 0.5% | 0.2% |
| DF | 7.1% | 6.9% | 8.5% | 5.6% | 6.8% |
| S. No. | 8 | 10 | 12 | 12 | 10 |

# APPENDIX C

Power Losses Calculation for the Nine–level Inverter

# Loss Calculation of On-state in a Nine-level STATCOM

==========

Assume : The voltage is sinusoidal and the reactive current is a cosin curve

During on state, the power loss in a GTO thyristor is Pon = 1.8*i + 0.0006*i*i

and the power loss in a diode is Pon = 1.5*i + 0.0005*i*i

where i = Im*cos(ωt)

$Vc := 2880$ $R := 50000$ $Cg := 0.0006$ $Cd := 0.0005$

$Im := \sqrt{2} \cdot 3554$ $rad := \frac{\pi}{180}$

$\alpha 1 := 9.05 \cdot rad$ $\alpha 2 := 18.56 \cdot rad$ $\alpha 3 := 34.17 \cdot rad$ $\alpha 4 := 57.88 \cdot rad$

$$Pong = Ng \cdot \left(1.8 \cdot Im \cdot \cos(\omega t) + Cg \cdot Im^2 \cdot \cos(\omega t)^2\right)$$

$$Pond = Nd \cdot \left(1.5 \cdot Im \cdot \cos(\omega t) + Cd \cdot Im^2 \cdot \cos(\omega t)^2\right)$$

$$Pon = \frac{1}{2 \cdot \pi} \cdot \int_{\alpha s}^{\alpha f} (Pong + Pond)\, d(\omega t)$$

$$P1(\alpha s, \alpha f, Ng, Nd) := (1.8 \cdot Ng + 1.5 \cdot Nd) \cdot Im \cdot \left|\sin(\alpha f) - \sin(\alpha s)\right|$$

$$P2(Ng, Nd) := (Cg \cdot Ng + Cd \cdot Nd) \cdot \frac{Im^2}{2}$$

$$P3(\alpha s, \alpha f) := \left|\alpha f - \alpha s + (\cos(\alpha f) \cdot \sin(\alpha f) - \cos(\alpha s) \cdot \sin(\alpha s))\right|$$

$$Pon(\alpha s, \alpha f, Ng, Nd) := \frac{1}{2 \cdot \pi} \cdot (P1(\alpha s, \alpha f, Ng, Nd) + P2(Ng, Nd) \cdot P3(\alpha s, \alpha f))$$

During 0 to $\alpha 1$, there are 4 GTO thyristors and 4 diodes in conduction

$Pon(0,\alpha 1,4,4) = 4.432 \cdot 10^3$ $\quad$ $Pon1 := Pon(0,\alpha 1,4,4)$

During $\alpha 1$ to $\alpha 2$, there are 3 GTO thyristors and 5 diodes in conduction

$Pon(\alpha 1,\alpha 2,3,5) = 4.362 \cdot 10^3$ $\quad$ $Pon2 := Pon(\alpha 1,\alpha 2,3,5)$

During $\alpha 2$ to $\alpha 3$, there are 2 GTO thyristors and 6 diodes in conduction

$Pon(\alpha 2,\alpha 3,2,6) = 6.129 \cdot 10^3$ $\quad$ $Pon3 := Pon(\alpha 2,\alpha 3,2,6)$

During $\alpha 3$ to $\alpha 4$, there are 1 GTO thyristors and 7 diodes in conduction

$Pon(\alpha 3,\alpha 4,1,7) = 6.099 \cdot 10^3$ $\quad$ $Pon4 := Pon(\alpha 3,\alpha 4,1,7)$

During $\alpha 4$ to 90 degree, there are no GTO thyristors and 8 diodes in conduction

$Pon\left(\alpha 4,\frac{\pi}{2},0,8\right) = 2.356 \cdot 10^3$ $\quad$ $Pon5 := Pon\left(\alpha 4,\frac{\pi}{2},0,8\right)$

During $\pi/2$ to $\pi$-$\alpha 4$, there are 8 GTO thyristors and no diodes in conduction

$Pon\left(\frac{\pi}{2},\pi - \alpha 4,8,0\right) = 2.827 \cdot 10^3$ $\quad$ $Pon6 := Pon\left(\frac{\pi}{2},\pi - \alpha 4,8,0\right)$

During $\pi$–$\alpha 4$ to $\pi$-$\alpha 3$, there are 7 GTO thyristors and 1 diodes in conduction

$Pon(\pi - \alpha 4,\pi - \alpha 3,7,1) = 6.992 \cdot 10^3$ $\quad$ $Pon7 := Pon(\pi - \alpha 4,\pi - \alpha 3,7,1)$

During $\pi-\alpha 3$ to $\pi-\alpha 2$, there are 6 GTO thyristors and 2 diodes in conduction

$Pon(\pi - \alpha 3, \pi - \alpha 2, 6, 2) = 6.713 \cdot 10^3$ $\quad$ $Pon8 := Pon(\pi - \alpha 3, \pi - \alpha 2, 6, 2)$

During $\pi-\alpha 2$ to $\pi-\alpha 1$, there are 5 GTO thyristors and 3 diodes in conduction

$Pon(\pi - \alpha 2, \pi - \alpha 1, 5, 3) = 4.565 \cdot 10^3$ $\quad$ $Pon9 := Pon(\pi - \alpha 2, \pi - \alpha 1, 5, 3)$

During $\pi-\alpha 1$ to $\pi$, there are 4 GTO thyristors and 4 diodes in conduction

$Pon(\pi - \alpha 1, \pi, 4, 4) = 4.432 \cdot 10^3$ $\quad$ $Pon10 := Pon(\pi - \alpha 1, \pi, 4, 4)$

The total on state power loss should be

$Pon := 2 \cdot (Pon1 + Pon2 + Pon3 + Pon4 + Pon5 + Pon6 + Pon7 + Pon8 + Pon9 + Pon10)$

$Pon = 9.781 \cdot 10^4$

Loss Calculation of Off-state in a Nine-level STATCOM

Switching angle between 0 to $\alpha 1$

$$Pb1 := \left(\frac{Vc}{R}\right)^2 \cdot 8 \cdot R + \left(\frac{Vc}{5 \cdot R}\right)^2 \cdot 10 \cdot R + \left(\frac{2 \cdot Vc}{6 \cdot R}\right)^2 \cdot 12 \cdot R + \left(\frac{3 \cdot Vc}{7 \cdot R}\right)^2 \cdot 14 \cdot R \qquad Pb1 = 2.041 \cdot 10^3$$

Switching angle between $\alpha 1$ to $\alpha 2$

$$Pb2 := \left(\frac{Vc}{R}\right)^2 \cdot 8 \cdot R + \left(\frac{Vc}{4 \cdot R}\right)^2 \cdot 4 \cdot R + \left(\frac{2 \cdot Vc}{5 \cdot R}\right)^2 \cdot 5 \cdot R + \left(\frac{3 \cdot Vc}{6 \cdot R}\right)^2 \cdot 6 \cdot R + \left(\frac{4 \cdot Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R \ldots + \left(\frac{2 \cdot Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R + \left(\frac{Vc}{6 \cdot R}\right)^2 \cdot 6 \cdot R$$

$$Pb2 = 2.252 \cdot 10^3$$

Switching angle between $\alpha 2$ to $\alpha 3$

$$Pb3 := \left(\frac{Vc}{R}\right)^2 \cdot 8 \cdot R + \left(\frac{Vc}{3 \cdot R}\right)^2 \cdot 3 \cdot R + \left(\frac{2 \cdot Vc}{4 \cdot R}\right)^2 \cdot 4 \cdot R + \left(\frac{3 \cdot Vc}{5 \cdot R}\right)^2 \cdot 5 \cdot R + \left(\frac{4 \cdot Vc}{6 \cdot R}\right)^2 \cdot 6 \cdot R \ldots + \left(\frac{5 \cdot Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R + \left(\frac{Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R$$

$$Pb3 = 2.905 \cdot 10^3$$

Switching angle between $\alpha 3$ to $\alpha 4$

$$Pb4 := \left(\frac{Vc}{R}\right)^2 \cdot 8 \cdot R + \left(\frac{Vc}{2 \cdot R}\right)^2 \cdot 2 \cdot R + \left(\frac{2 \cdot Vc}{3 \cdot R}\right)^2 \cdot 3 \cdot R + \left(\frac{3 \cdot Vc}{4 \cdot R}\right)^2 \cdot 4 \cdot R + \left(\frac{4 \cdot Vc}{5 \cdot R}\right)^2 \cdot 5 \cdot R \ldots + \left(\frac{5 \cdot Vc}{6 \cdot R}\right)^2 \cdot 6 \cdot R + \left(\frac{6 \cdot Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R$$

$$Pb4 = 4.08 \cdot 10^3$$

Switching angle between $\alpha 4$ to $\pi/2$

$$Pb5 := \left(\frac{Vc}{R}\right)^2 \cdot 8 \cdot R + \left(\frac{Vc}{R}\right)^2 \cdot R + \left(\frac{2 \cdot Vc}{2 \cdot R}\right)^2 \cdot 2 \cdot R + \left(\frac{3 \cdot Vc}{3 \cdot R}\right)^2 \cdot 3 \cdot R + \left(\frac{4 \cdot Vc}{4 \cdot R}\right)^2 \cdot 4 \cdot R \ldots$$
$$+ \left(\frac{5 \cdot Vc}{5 \cdot R}\right)^2 \cdot 5 \cdot R + \left(\frac{6 \cdot Vc}{6 \cdot R}\right)^2 \cdot 6 \cdot R + \left(\frac{7 \cdot Vc}{7 \cdot R}\right)^2 \cdot 7 \cdot R$$

$$Pb5 = 5.972 \cdot 10^3$$

Total Off-state loss is :

$$Poff := \frac{2}{\pi} \cdot \left[ Pb1 \cdot \alpha 1 + Pb2 \cdot (\alpha 2 - \alpha 1) + Pb3 \cdot (\alpha 3 - \alpha 2) + Pb4 \cdot (\alpha 4 - \alpha 3) + Pb5 \cdot \left(\frac{\pi}{2} - \alpha 4\right) \right]$$

$$Poff = 4.153 \cdot 10^3$$

Total Losses Analysis for a Nine-level STATCOM

On-state Loss $Pon = 9.781 \cdot 10^{4}$

Off-state Loss $Poff = 4.153 \cdot 10^{3}$

Steady-state Loss $Ps := Pon + Poff$ $Ps = 1.02 \cdot 10^{5}$

Snubber Loss Calculation :

$Cs := 4 \cdot 10^{-6}$ $psn := \frac{60}{2} \cdot Cs \cdot Vc^{2}$

Because there are always 8 GTO thyristors in blocking :

$Psn := 8 \cdot psn$ $Psn = 7.963 \cdot 10^{3}$

Switching Loss : $Psw := 0.1 \cdot Ps + Psn$ $Psw = 1.816 \cdot 10^{4}$

Total losses of GTO thyristors in the circuit: $P := Ps + Psw$

$P = 1.201 \cdot 10^{5}$

For the three phases : $P3 := 3 \cdot P$ $P3 = 3.604 \cdot 10^{5}$

Conclusions :

Calculation of the total reactive power output for a Nine-level STATCOM

$Vc = 2.88 \cdot 10^3$ $\quad Irms := \frac{Im}{\sqrt{2}}$ $\quad Irms = 3.554 \cdot 10^3$

$$Vpeak := \frac{4}{\pi} \cdot (Vc \cdot (\cos(\alpha 1) + \cos(\alpha 2) + \cos(\alpha 3) + \cos(\alpha 4)))$$

$$Vrms := \frac{Vpeak}{\sqrt{2}} \qquad Vrms = 8.543 \cdot 10^3$$

$Q := 3 \cdot Irms \cdot Vrms$ $\quad Q = 9.108 \cdot 10^7$

The Loss Ratio of the STATCOM : $\eta := \frac{P3}{Q}$ $\quad \eta = 0.396 \cdot \%$

# APPENDIX D

## The Parameters of The Test System

$V = 1.000$ pu.

$V_s = 1.130$ pu.

$X_s = 0.050$ pu.

$X_\delta = 0.250$ pu.

$R_L = 0.235$ pu.

$R_2 = 0.160$ pu.

$X_L = 0.086$ pu.

## The Parameters of Controls

| PI Regulator | Proportional Gain | Integral Gain |
|---|---|---|
| Phase Locked Loop | 50 | 2000.0 |
| DC Voltage Balance Control | 2.4 | 0.1 |
| AC Terminal Voltage Control | 3.4 | 0.006 |
| Reactive Power Output Control | 2.0 | 0.008 |
| Current Limiting Control | 0.45 | 0.04 |