Work Function Tuning of Reactively Sputtered $Hf_xSi_yN_z$ Metal Gate Electrodes for Advanced CMOS Technology

by

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Abstract

The aim of this research is to study the work function (Φ_m) tuning of the $Hf_xSi_yN_z$ metal films through the incorporation of nitrogen. The Hf and the Si targets were co-sputtered in nitrogen (N_2) and argon (Ar) plasma at 12mTorr. The gas flow ratio, $R_N = N_2/ (N_2+Ar)$, was adjusted to vary the nitrogen concentration in HfSiN films.

The work function (Φ_m) of HfSiN gate extracted from the capacitance-voltage (CV) and the internal photoemission (IPE) measurements was found to decrease (from ~ 4.64eV to ~ 4.42eV) for increasing gas flow ratios (from 10% to 30%).

X-ray photoelectron spectroscopy (XPS) was used for material characterization. During XPS analysis, the nitrogen (N 1s) peak intensity was observed to increase with increasing gas flow ratios.

The results indicate that adjusting the nitrogen concentration in HfSiN films can be used to tune the HfSiN gate work function over ~ 0.2 eV tuning window.

Dedicated to

My Parents

Asha and Baldev Meelu

My Husband

Manoj Chaudhari

And

My son

Rishaan Chaudhari

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First of all, I wish to sincerely thank my advisor, Dr. Douglas A. Buchanan for his invaluable support, guidance and encouragement during the course of this research. His continuous support has made this project possible. I hope I have lived up to his expectations.

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I would like to thank my parents-in-law Vidya and Gopal Dass Chaudhari for their support. I would also like to dedicate this work to my brother Taranpreet Meelu and nephew Armaan Chaudhari. Also, I wish to express my deepest thanks to all my family members for their love and appreciation.

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Symbol	Unit	Description
A	cm^2	Area
Φ_b	eV	Barrier Height
Φ_{beff}	V	Effective barrier height
Φ_F	V	Fermi Potential
E_C	eV	Conduction Band Edge
C_d	F or F/cm^2	Depletion Capacitance
J_g	A/cm	Current Density
L_D	cm	Debye's Length
F	V/cm	Electric field across the gate oxide
χ	eV	Electron Affinity
χ_i	eV	Electron Affinity for insulator
χ_{si}	eV	Electron Affinity for silicon
E_g	eV	Energy band gap of Silicon
E_F	eV	Fermi Energy
C_{ox}	F or F/cm^2	Oxide Capacitance
ε_0	F/cm	Permittivity of free space
I_{ph}	A	Photocurrent
ε_{0x}		Relative Dielectric Permittivity for SiO_2
ε_{si}		Relative Dielectric Permittivity for silicon
E_V	eV	Valence Band Edge

Φ	eV	Work Function
Φ_m	eV	Work Function of Metal Gate
Φ_{ms}	eV	Work Function Difference
Φ_s	eV	Work Function of Silicon Substrate
N_a	cm^{-3}	Acceptor doping concentration in Silicon
n_i	cm^{-3}	Intrinsic carrier concentration in silicon
q	C	Magnitude of electron charge
λ	nm	Wavelength
ν	cm/sec	Frequency of Light
ψ_B	V	Bulk Potential of Silicon
ψ_s	V	Surface Potential or band bending in Silicon
ρ	Ω.cm	Electrical Resistivity
h	J.s	Planck's constant (6.626×10^{-34} J.s)
R_s	Ω /□	Sheet Resistance
T	K	Temperature
t_{ox}	nm	Oxide thickness
V_g	V	Gate Voltage
V_{FB}	V	Flatband voltage
W	nm	width or thickness of sputtered film
W_d	nm	Depletion layer width in depletion
W_{dmax}	nm	Maximum depletion layer width in inversion
x_o	Å	Zero field distance
Y		Quantum Yield

Chapter 1 Introduction

1.1 Background

The aggressive reduction of the transistor dimensions has been the key driving force in the success of silicon semiconductor industry, as outlined by the International Technology Roadmap for semiconductors (ITRS) [1]. This scaling trend has led to the development of metal oxide semiconductor based devices with continually decreasing physical dimensions be it a length, width, depth or thickness [2]. Furthermore, the introduction of new materials and innovations in the fabrication processes has allowed the chipmakers to follow the so-called "Moore's law" for 4 decades which (in 1965) stated that the density of devices of an integrated circuit would double every 18-24 months with a subsequent reduction in the cost per transistor [3]. In Figure 1-1, the number of metal oxide semiconductor field effect transistors (MOSFETs) in Intel processors is shown to have doubled with each technology generation as the printed gate lengths have shrunk exponentially [4].

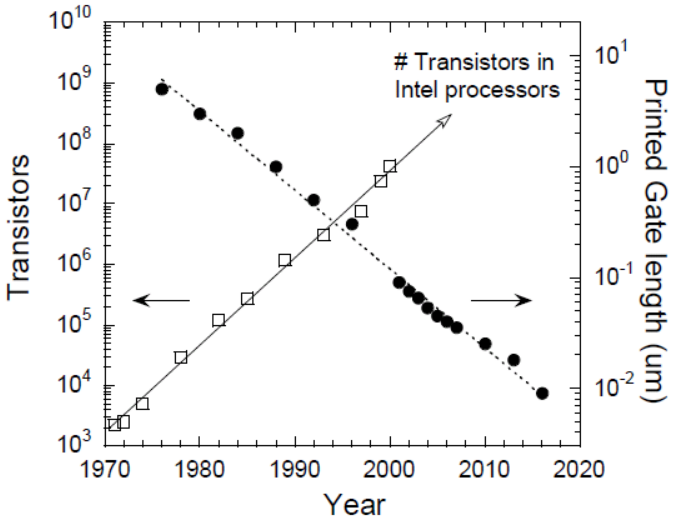

Figure 1-1: The number of transistors in Intel processors increases as the gate length decreases from 1970-2012 [4].

Due to this continuous scaling of transistor dimensions, some problems have been revealed in the conventional poly-silicon (poly-Si) gated CMOS devices [1]. These include poly depletion, high gate resistance, a high gate tunneling current, and dopant penetration, all of which will be discussed in the next section. Therefore, there is an immense interest in alternative metal gates to replace the poly-Si gates used in advanced CMOS devices.

1.2 Motivation for Metal Gates

Since the 1970s, heavily doped poly-silicon (poly-Si) has been used as a metal gate electrode in MOSFET devices. A poly-Si gate in a field effect transistor (FET) may suffer from depletion; when the gate is biased in inversion (of the substrate) if the surface field is very high. As the gate dielectric has continually been scaled, the operating biases have not been. As such the surface field has continually been increased. Due to the limited number of dopants in the poly-silicon, which results from the limit in the solid solubility and the high surface field, the poly-silicon starts to react more like a semiconductor than the desired metal. Therefore, when a large field is applied, the carrier density is now insufficient and can react to the applied field.

As a result a layer depleted of charge carriers (a depletion region) is formed at the poly-Si/oxide interface. This thin depletion layer adds (in series and reduces) the total effective capacitance. This capacitance may be thought of as an "extra" oxide thickness of (~3-4 Å) and therefore effectively reduces the total gate capacitance which in turn causes a decrease in the drain current [5].

Since it is the drain current, for the given operating bias, that determines the speed of the transistor, a reduction in performance will be seen. For very thin gate dielectrics (i.e. EOT ≤ 20Å), this depletion layer that causes an effective increase in EOT be neglected [6]. Practically it is very difficult to achieve doping densities beyond 1×10^{19} cm^{-3} for a poly-Si [7]. Therefore, a metal gate, with a much higher concentration, has been used extensively to avoid this gate depletion effect.

Aside from the depletion effect, the penetration of dopants from the gate through the dielectric into the substrate (referred to as "dopant penetration") and the increased resistance that arises with this scaling all require the use of alternative metal gates in place of poly-silicon in MOSFET devices [7].

1.3 Requirements for alternative metal gates

The metal gates that might potentially be used must satisfy several requirements for integration into fully processed CMOS devices. These include the appropriate work function (i.e. threshold voltage) for nFETs and pFETs, thermal/chemical stability with the underlying dielectric, and the process compatibility with the CMOS devices. These will be discussed in the following sections.

1.3.1 The effective work functions of candidate metal gates for CMOS technology

As the channel length is scaled down, threshold voltage and the supply voltage are also scaled to maintain large overdrive currents and reduce high field effects respectively. This

threshold voltage decreases with decreasing channel lengths but can, to some degree, be compensated by increasing the depletion charge density for bulk CMOS devices [8]. In order to tailor the threshold voltage, it is important that the gate material should have a tunable work function [9].

A key challenge for the MOSFET devices is to find the gate materials with appropriate work functions for desired threshold voltages [10]. Therefore, a gate material with a work function that places it Fermi level close to the middle of the silicon bandgap is desired so that the work function difference between the gate electrode and the near intrinsic film can be adjusted to optimize the threshold voltages of both n and p channel devices in a CMOS circuit. In Figure 1-2, a plot is shown that illustrates the relationship between the threshold voltage and the work function.

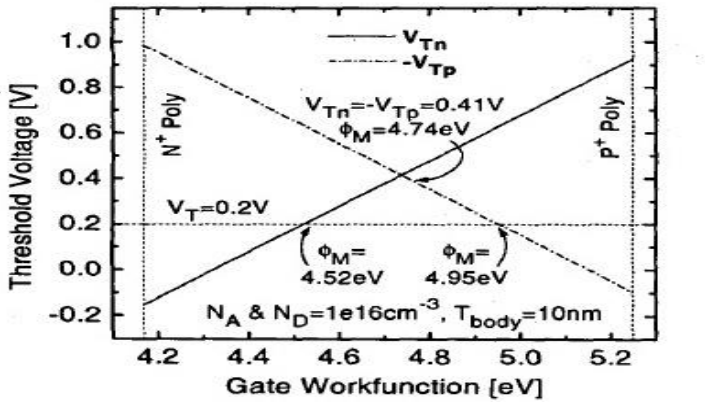

Figure 1-2: Threshold voltage versus gate work function [11]

Due to continuous scaling, it is desired to have low (~ ±0.2eV) threshold voltage for both transistor types [11]. This can be achieved by the appropriate "tuning" of the work function of the gate materials. By definition, the effective work function (EWF) of a metal is the energy that is required to remove an electron from metal Fermi level to vacuum.

The reason for having a tunable work function is that, there would be the possibility of making both p+ and n+ gates from the same base metal. This would reduce the processing required to integrate two completely different metals.

The work function tuning can be achieved by many approaches including implantion, fully-silicided gates and metal alloys [7]. A dual metal gate approach used for CMOS processing may require a complicated selective deposition and/or etching processes for integration [13]. In this context, using a common work function both for NMOSFETs and PMOSFETs with a value around the mid-gap (~4.5eV) seems very attractive [14].

Aside from these work function requirements, the candidate metal gates must be highly conductive and have a high melting point to withstand the high processing temperatures, commonly used for CMOS fabrication [15, 16]. Considering all these factors, a substantial amount of research is going on regarding the alternative metal gate electrodes which include research on elemental metal, metal nitrides, metal silicides and alloys thereof [17] – [20].

1.4 Potential Candidates

There are various PMOS metal candidates with work functions near 5 eV. These include Co, Pd, Ni, Re, Ir, Ru, Pt. For NMOS, the metal candidates with a work function close to 4 eV include such metals as Al, Hf, Mo, Ta, V, Ti, Zr. Aside from the pure metals, other metal alloy systems such as metallic oxides, nitrides, silicides, for example TiN, TaN, MoN, TaSiN, MoSiN, and HfSiN could also be used if the correct work functions and therefore the threshold voltages can be obtained. The work function of the metals can be tuned by adjusting the alloy concentration; for example, adjusting the nitrogen (N) and/or silicon (Si) composition in the alloy [19, 20].

1.5 Aim of the Research Project

The goal of this research is to produce and investigate the tuned metal gate electrodes integrated with SiO_2 as a gate dielectric. In this work, co-sputtered HfSiN was chosen as a metal gate electrode. The fabrication steps for making this metal alloy will be discussed in Chapter 3. The work function of this alloy has shown the dependence on the N_2 partial pressure and the subsequent thermal processing. By incorporating different concentration of nitrogen in films, the HfSiN work function was altered. The amount of nitrogen was varied by changing the gas flow ratio ((N_2/ (N_2 + Ar)) during the gate deposition.

1.6 Outline

This dissertation is divided into 6 chapters which are organised as follows. A brief introduction of the concepts and theories of the MOS capacitor will be presented in Chapter 2. Furthermore, Chapter 3 provides a detailed description of the fabrication processes of the MOS capacitor. An experimental apparatus and measurement techniques used for the MOS devices will be given in Chapter 4. The experimental results and discussion will be provided in Chapter 5. The basic principles, instrumentation and characterization results obtained from X-ray Photoelectron Spectroscopy (XPS) surface analysis will be presented in Chapter 6. The last Chapter will provide a summary and suggested future work.

Chapter 2 MOS Capacitor Theory and Measurement

2.1 Introduction

In this chapter, a review of the basic theory of a metal oxide semiconductor (MOS) capacitor and its three regions of operation (accumulation, depletion and inversion) are introduced. The capacitance voltage (CV) characteristics of an MOS capacitor will be discussed in the following sections. Typically, the CV measurements provide important information regarding the MOS device parameters, for example, oxide thickness, oxide charge, flat band voltage, and work function difference.

An introduction to the internal photoemission (IPE) technique, its application for the barrier height extraction and the method for extracting the effective barrier height (Φ_{beff}) from quantum yield and incident photon flux density will also be presented in this chapter. From these measurements it will be shown that the work function (Φ_m) of the metal gate is obtained from which the extracted value of the effective barrier height value is obtained.

2.2 MOS Capacitor

The MOS capacitor is an important test structure in the semiconductor industry. In this study, the MOS capacitor was used for investigating all of the electrical properties of the MOS system. Basically, an MOS capacitor is a parallel plate capacitor which consists of two electrodes separated by a thin insulating layer. For typical MOS devices, one of the electrodes is called the gate and is typically made of poly-Si. The other electrode is a semiconducting Si substrate typically with silicon dioxide ($SiO_{2)}$ as the insulating layer [21]. In this study, p-type silicon

wafers with a doping concentration of $N_a = 1.5 \times 10^{15}$ cm^{-3} were used as a semiconductor substrate, SiO_2 was used as the gate dielectric and $Hf_xSi_yN_z$ as the metal gate electrode.

2.3 Energy Band Diagram of an MOS Capacitor

The energy band diagram is very important in the understanding of the operation of an MOS capacitor. The components of the capacitor can be represented with the help of the band diagram as shown in Figure 2-1 below:

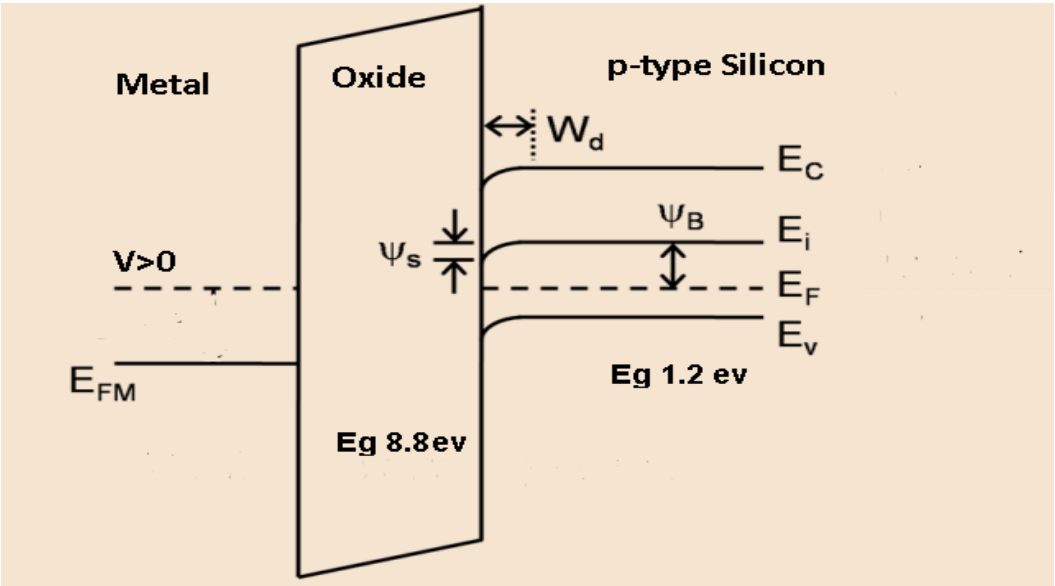

Figure 2-1: The energy band diagram of an MOS capacitor with a p-type semiconductor.

In Figure 2-1, the band diagram of a p-type MOS capacitor is shown depicting the electron energies and the potentials of this MOS device. The energy band edge in this diagram consists of the conduction band energy level (E_c), the valence band energy level (E_v) and the intrinsic energy level (E_i). The intrinsic energy level lies approximately halfway between the conduction band energy level and valence band energy level. The difference between the Fermi energy level and the intrinsic energy level is defined as the Fermi potential [21].

2.4 Capacitance-Voltage Measurements

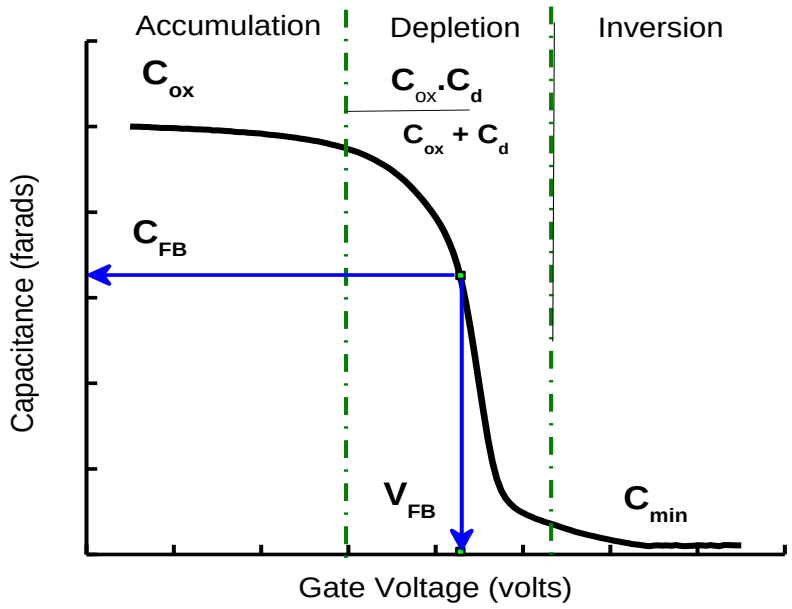

Figure 2-2: The measured high frequency capacitance-voltage (HFCV) curve of an MOS capacitor on a p-type silicon substrate. The three distinct regions of operation: accumulation, depletion and inversion are also shown.

In this work, the CV measurements were performed by super imposing a small AC signal at high frequency (100 kHz) on a DC gate bias sweep. A CV response is obtained by slowly varying DC gate voltage. As the voltage was varied, the capacitor operates in three different regimes [21] which are shown in Figure 2-2. These three operating regimes will be discussed in the next section.

2.4.1 Accumulation

The accumulation regime is so named because when a negative gate bias ($V_g<0$) is applied to the gate, the majority carriers (holes for a p-type substrate) "accumulate" at the surface to form a sheet charge at the interface. The total capacitance that is measured in this regime is

the oxide capacitance (C_{ox}), because the substrate capacitance is not affected by the changing AC bias as it is effectively "screened" by the accumulation charge at the surface [21, 24]. Therefore, the maximum capacitance (C_{max}) is simply the dielectric capacitance of the oxide and is related to the gate electrode area A, the gate oxide thickness (t_{ox}) and the relative dielectric permittivity ($\varepsilon_{ox} = 3.9$ for SiO_2) by

$$C_{MOS} = C_{max} = C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}}, \qquad (2.1)$$

where, ε_o is the permittivity of free space.

2.4.2 Depletion

The central region as depicted in the CV curve (Figure.2-2) is called as the depletion regime. When a positive bias ($V_g>0$) is applied to the gate, the majority carriers (holes for a p-type silicon substrate) are depleted at semiconductor interface leaving behind the ionised acceptor ions. As a result a net negative charge emerges and produces a "space charge region". The width of this "depleted area" (called a "depletion width") increases as the gate bias increases negatively. Since the "depletion layer" capacitance is inversely proportional to its width, this increase in bias results in a reduction in the depletion layer capacitance [21, 24]. The MOS capacitance in this region is given as:

$$C_{MOS} = C_{dep} = \frac{C_{ox}.C_d}{C_{ox} + C_d}, \qquad (2.2)$$

where C_{ox} and C_d are the oxide and depletion capacitances.

2.4.3 Inversion

The other region of operation of an MOS capacitor is called “inversion”. The inversion regime occurs when a very large positive voltage (for a p-type substrate) is applied at the gate. While the depletion region remains, as a result of the large voltage, minority carriers (electrons) collect at the semiconductor surface. At a voltage beyond what is referred to as the “threshold voltage”, the semiconductor surface is said to be fully depleted of its majority carriers but there remains a large concentration of minority carriers. Therefore, the surface is said to be “inverted” when the minority carrier concentration, at the surface, is greater than the majority carrier concentration in the bulk. Moreover, a strong inversion occurs when the surface potential(ψ_s) equals twice the bulk potential (ψ_B). The depletion layer attains its maximum width (W_{dmax}) as the gate bias is further increased. This in turn reduces the depletion capacitance to its minimum value ($C_{d,min}$) [21, 24]:

$$C_{d,min} = \frac{\varepsilon_o \varepsilon_{si} A}{W_{dmax}}, \quad W_{dmax} = \sqrt{\frac{2\varepsilon_o \varepsilon_{si} \psi_s}{qN_a}}, \tag{2.3}$$

where, ε_o is the free space permittivity, ε_{si} (=11.9) is the relative permittivity of the silicon, ψ_s is the band bending or the surface potential of silicon, q is the electronic charge and N_a is the acceptor doping concentration within the depletion region which is assumed to be uniform.

At very high frequencies, the charge density in the inversion layer cannot respond to the rapidly changing (high frequency) AC gate bias due to the limited minority carrier lifetime. The minority carriers at the surface shield the bulk silicon and therefore the depletion region is fixed. Since the minority carrier concentration cannot follow the HF signal, the effective change in the charge – i.e. dQ, as measured by with the capacitance meter, is constant. Therefore, the depletion capacitance also becomes constant. The total capacitance in the inversion regime, like in the

accumulation regime, is simply the oxide capacitance (C_{ox}) plus (in series with) the minimum depletion capacitance ($C_{d,min}$) ,given as :

$$C_{MOS} = C_{min} = \frac{C_{ox} C_{d,min}}{C_{ox} + C_{d,min}} \quad (2.4)$$

2.5 Determination of the MOS device parameters

Capacitance voltage (C-V) and current voltage (I-V) measurements were performed on the MOS capacitors from which many device parameters were extracted. These parameters, which will be discussed in some detail in following sections, include the flatband voltage, the trapped interfacial and the trapped oxide charge, the oxide thickness, the substrate doping concentration, and the metal semiconductor work function difference (Φ_{ms}).

2.5.1 Oxide Charge

The presence of charge within the gate oxide or trapped at the interface affects the electric field within the oxide as well as the silicon surface potential and band bending, which causes a shift in the CV characteristic [21]. This charge is divided up into several types of charge: the oxide fixed charge, mobile oxide charge and the trapped charge either in the oxide or at its interface with the substrate. Using a low temperature anneal (5% H_2, 95% N_2 at 400°C) most of the oxide fixed and the interface trapped charge can be passivated. This is commonly referred to as a “forming gas anneal” (FGA) [21, 24]. These different types of charge and their effect on the measured characteristic will be discussed in following section.

2.5.1.1 Fixed Oxide Charge

The oxide charge which remains even after annealing is the fixed oxide charge and is referred to as "fixed" as the charge concentration does not change under the typical bias conditions. This type of charge typically results from structural defects_ --often oxygen vacancies within the SiO_2 matrix_ --which often occur in low temperature oxides. Normally, this charge manifests itself as positive charge located in the oxide layer, near, but not at the semiconductor/oxide interface. As the name implies, this fixed oxide charge is immobile and independent of the gate bias [21, 24]. Often, this type of charge was referred to as "anomalous positive charge (APC)" as its origins were unclear for many decades.

2.5.1.2 Mobile charge

The mobile oxide charge is able to respond to the change in applied electric field by moving across the oxide typically at elevated (>200°C) temperatures. The mobile charge is not very common in modern oxides and was historically the result of sodium and potassium impurities that had been introduced during the fabrication process. This ionic charge is positive and therefore, under a positive bias would move away from the gate eventually piling up at the oxide/semiconductor interface. With the opposite bias on the gate, the positive charge would be attracted towards the gate side of the dielectric. A hysteresis in the CV curve can result from the movement of this charge when the gate voltage is changed [21, 24].

2.5.1.3 Oxide trapped charge

The oxide trapped results from electrons or holes being trapped in the bulk SiO_2 either as a result of some electrical stress or due to processing. These charges lie inside the oxide layer

and may be introduced through the injection of hot electrons or holes, - from UV or highly energetic particles in a plasma or by exposure to X-ray radiation [21, 24]. This charge can shield a part of the applied gate bias and may introduce a voltage shift in the HFCV curve. This shift which is often extracted by measuring the change in the extracted flatband voltage (V_{FB}) is shown in Figure 2-3.

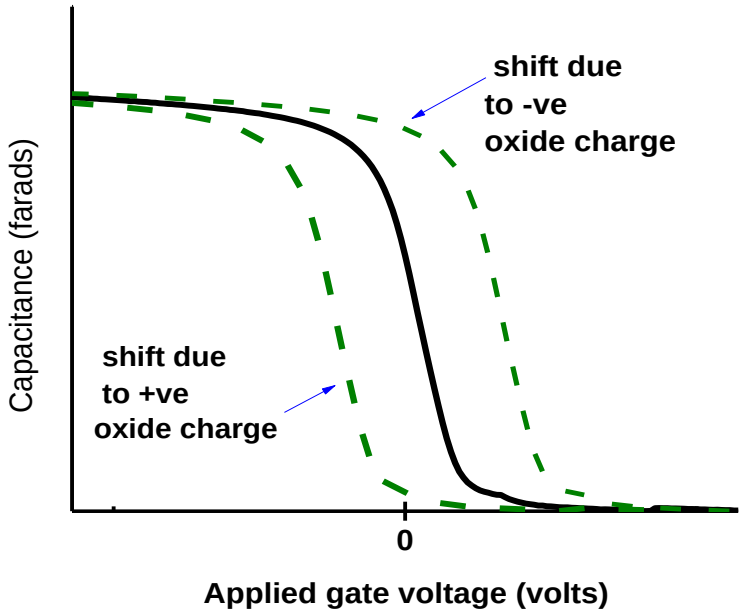

Figure 2-3: Due to presence of either positive or negative oxide charge, the CV curve shifts along the voltage axis.

2.5.2 Interface States or Trap Charge

Interface trapped charge is located at SiO_2/Si interface. These electronically active defects affect the band bending, and its dependence on the applied bias, at the silicon surface. Defects at the interface are said to be electrically active if the charge state of the defect changes in response to a change in applied bias. These defects may exchange charge with either the conduction (electrons) or the valence (holes) band [21]. The interface trapped charge produces a

"streched out" voltage shift in CV curve as illustrated in the Figure 2-4. These defects may often be annealed out using a 30 min. forming gas FG) which is usually 5% H_2 in N_2.

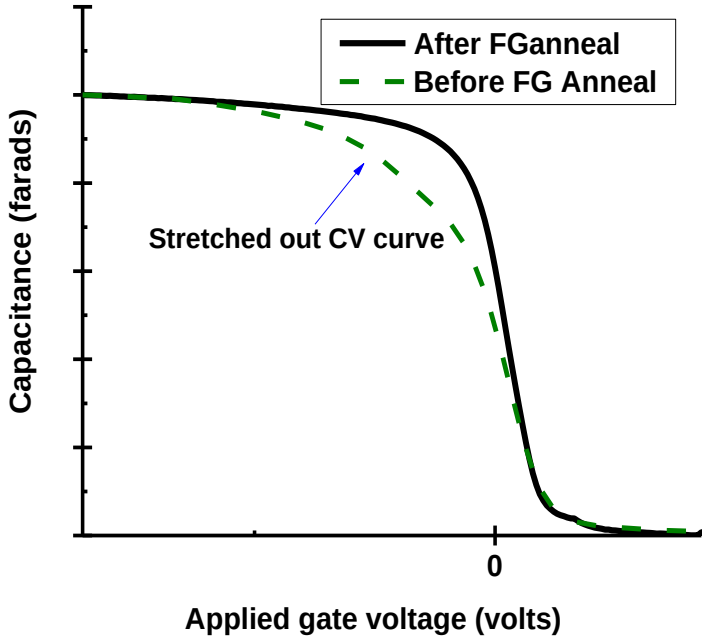

Figure Error! No text of specified style in document.**-4**: The interface trap charge affects the high frequency capacitance voltage (HFCV) characteristics of a MOS capacitor.

2.5.3 Oxide Thickness (t_{ox})

The oxide thickness is one of the important parameter of a MOS device, and it needs to be measured precisely. In this work, the oxide thickness was determined by different electrical and optical methods. To calculate the gate oxide thickness, the oxide capacitance (C_{ox}) was measured in accumulation regime where the capacitance is constant and not the function of the applied bias. Given the gate area (A) and the material permittivity, the oxide thickness may be calculated using equation 2.1. Some other methods for extracting gate oxide thickness will be discussed in Chapter 3.

2.5.4 Doping Concentration (N_a) of the Silicon Substrate

By measuring the maximum capacitance (C_{max}) in accumulation and minimum capacitance (C_{min}) in inversion, an average activated doping concentration, N_a can be calculated. In this work, the doping concentration was calculated for a p-type semiconductor which was used as a substrate [21]. Using a high frequency- (1 MHz), the minimum capacitance (C_{min}) may be measured in strong inversion, where the depletion width is at its maximum. In this discussion the frequency used for CV measurement is considered "high", if it is fast enough such that the minority carriers (electrons for a p-type substrate) do not respond to the charging AC signal [21]. The average doping concentration (N_a), the relationship between C_{min} and W_{dmax} is given as:

$$C_{min} = \frac{\varepsilon_o}{t_{ox} + \frac{\varepsilon_o}{\varepsilon_{si}} W_{d\,max}} = \frac{\varepsilon_o}{t_{ox} + \frac{\varepsilon_o}{\varepsilon_{si}} \sqrt{\frac{2\varepsilon_o \varepsilon_{si} \psi_s}{qN_a}}}, \qquad (2.5)$$

The average doping concentration N_a, was then calculated from the equation 2.5.

2.5.5 Flat-band Voltage (V_{FB}) Measurement

To determine the flatband voltage (V_{FB}), a calculation of the silicon flatband capacitance (C_{FBS}) can be used for substrates with uniform doping profiles. The flatband capacitance (C_{FB}) may then be used to locate the flatband voltage (V_{FB}) on the HFCV curve [21]. The silicon flatband capacitance and the corresponding high frequency capacitance can be calculated using:

$$C_{FB} = \frac{C_{FBS} C_{ox}}{C_{FBS} + C_{ox}}, \qquad C_{FBS} = \frac{\varepsilon_s}{\lambda_p}, \qquad (2.6)$$

where, C_{ox} is the oxide capacitance, λ_p is the Debye length in silicon and ε_s is the permittivity of silicon.

The Debye length (λ_p is related to the uniform doping concentration (N_a) by

$$\lambda_p = \sqrt{\frac{\varepsilon_s k T}{q^2 N_a}}, \qquad (2.7)$$

where, kT is the thermal energy at a temperature T and q is the electron charge.

Therefore, the flat band voltage is affected by the charge present in oxide or at the oxide/semiconductor interface. By definition, the flat band voltage is an external voltage applied to the gate electrode, which produces a flat band condition by balancing out the difference between the work function in the metal and that in the semiconductor, and the charge present in the oxide. The flat band voltage is given by [21]

$$V_{FB} = \Phi_{ms} + \frac{Q_{ox}}{C_{ox}} = \left(\Phi_m - \Phi_s\right) + \frac{Q_{ox}}{C_{ox}}, \qquad (2.8)$$

where, Φ_m is the work function of the metal gate, Φ_s is the work function of the silicon and Q_{ox} is the total oxide charge density present within the oxide and at the oxide/semiconductor interface.

2.5.6 Work Function difference

The work function difference (Φ_{ms}) between the metal gate and the p-type silicon substrate is expressed as:

$$\Phi_{ms} = \Phi_m - \Phi_s, \qquad (2.9)$$

where, Φ_m is the work function of the metal gate and Φ_s is the work function of the silicon.

The work function difference (Φ_{ms}) of an MOS capacitor can be obtained from the relationship between the flat band voltage (V_{FB}) and the oxide capacitance (C_{ox}), which was discussed in section (2.4.5). The flatband voltage (V_{FB}) may be obtained from the CV curves of capacitors with different oxide thicknesses. If the flatband voltage is plotted as a function of an oxide thickness (t_{ox}), a linear fit may be applied to the data and is extrapolated to zero oxide

thickness. The slope of the linear fit provides the oxide charge density and at the y intercept, the flatband voltage value is equal to the the work function difference (Φ_{ms}) [21]. In Figure 2-5, the energy band diagrams of a metal and a p-type Si substrate are shown. The vacuum level is used as a reference point.

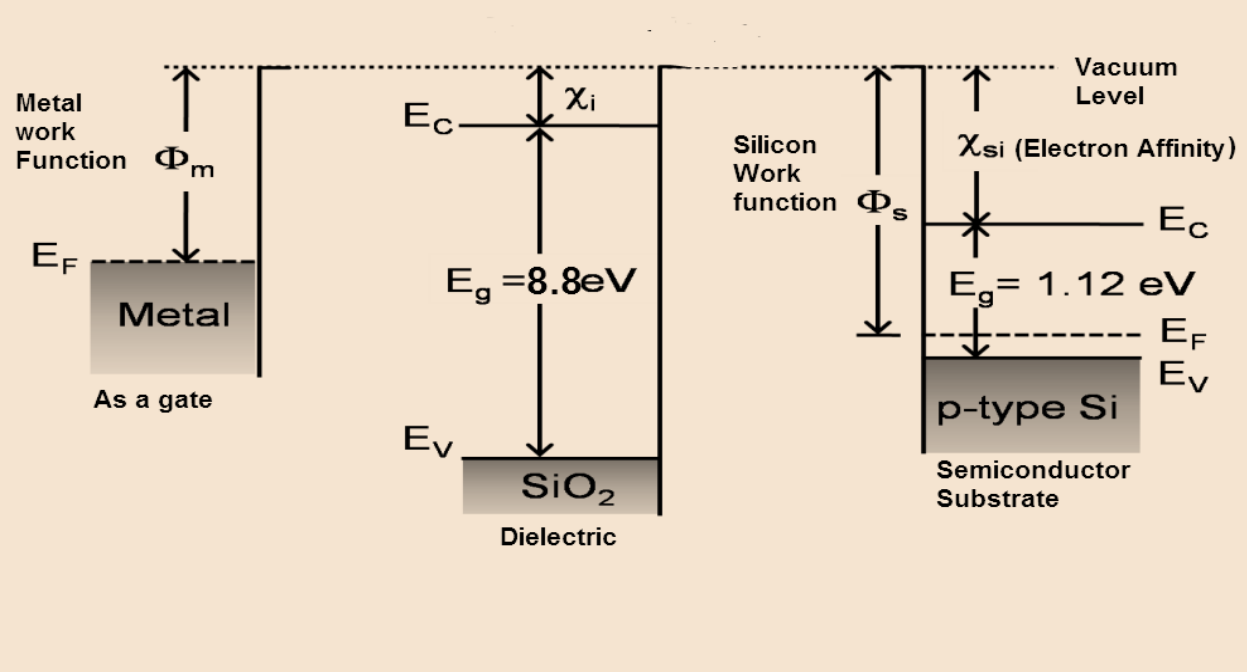

Figure 2-5: The energy band diagram illustrating the work function of metal (Φ_m), the work function of p-type silicon (Φ_s) and the electron affinities of SiO_2 (χ_i) and silicon (χ_{si})

2.6 Current-Voltage Measurement

Current voltage measurements of MOS capacitors have been used to assess the quality of the gate oxides. These measurements are very sensitive to the electronically active defects which could lead to a "leakage current" through the oxide. When a very high electric field is applied,

carriers are injected into the gate oxide as a result of charge tunneling through or being injected over the insulator barrier [24].

There are two types of tunneling which occurs in SiO_2 gate oxides used in this work: – direct tunnelling and Fowler Nordheim (FN) tunnelling as shown in Figure 2-6 [25].

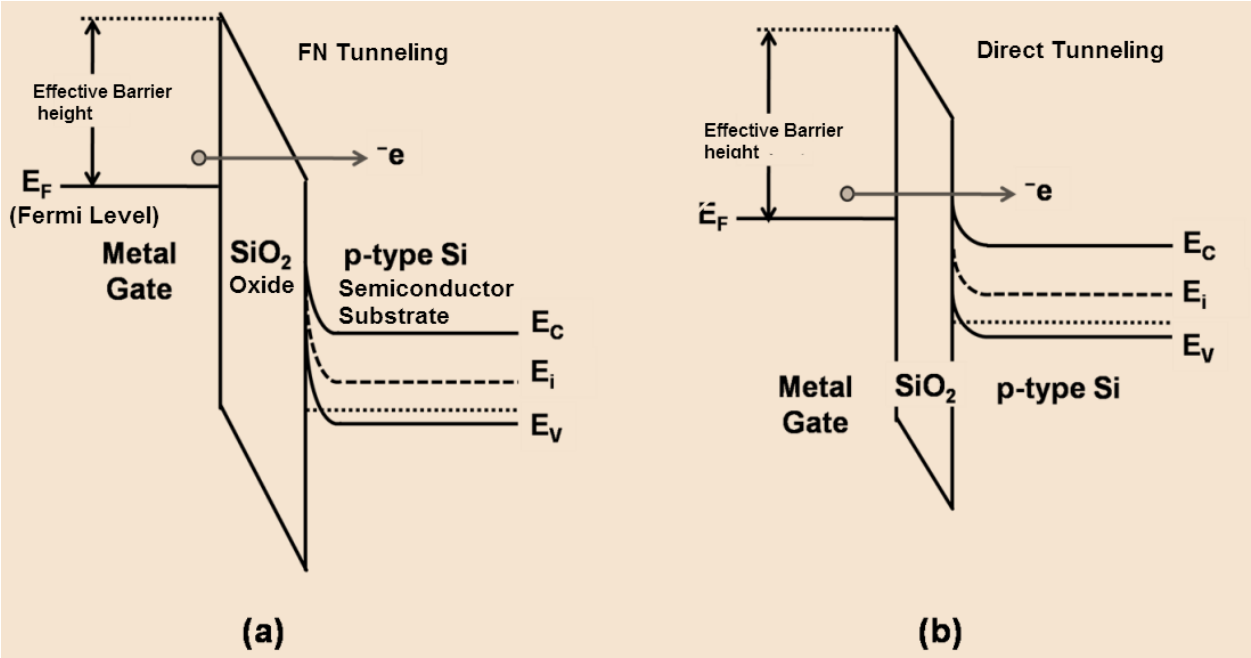

Figure 2-6: (a) Fowler-Nordheim (FN) Tunneling and (b) Direct Tunneling from the metal gate electrode.

2.6.1 Direct tunneling

The direct tunneling occurs in very thin gate oxides (<4nm) at a relatively low electric field where the carriers can penetrate the insulator directly and be transported from one electrode to the other, resulting in exponentially increasing gate (with a linear gate bias) leakage current. This leakage degrades the device performance [25]. In this work, the oxide thickness is greater than 10 nm, therefore, direct tunneling was not a problem [26].

2.6.2 Fowler-Nordheim (FN) tunneling

Fowler-Nordheim (FN) tunnelling occurs in thicker gate oxides and at higher electric fields. The electrons with sufficient energy may tunnel through the top triangular portion of the barrier into the SiO_2 conduction band as shown in Figure 2-6(b). For SiO_2 films, for an oxide field of ($5\text{-}7\times10^6$ V/cm), FN tunneling will result. The maximum electric field applied across the gate oxides used in this work was limited to 5×10^6 V/cm for all current voltage measurements [25].

2.7 Internal Photoemission

The internal photoemission (IPE) is a valuable technique for optical/electrical characterization in an MOS system. This technique is used for exciting carriers in the gate or substrate with energy high enough to inject them into the oxide conduction or valence band without the use of large electric fields. One application for this internal photoemission emission technique (IPE) is to determine the energy barrier at a metal/SiO_2 or a SiO_2/Si interface. This is done adjusting the energy of phonons (i.e. the wavelength of the light source) which in turn will produce the photo-excitation of carriers within the metal or substrate. When the energy of photo-generated carriers is greater than the barrier, a measurable current will result [28].

It is important to have a theoretical understanding of an interfacial energy barrier and the internal photoemission (IPE) technique, before discussing the use of IPE. A theoretical discussion on the effect of image force on the barrier height lowering (i.e. Schottky effect) will be discussed in the following section. It is also assumed that there is a sufficiently low concentration of oxide charge, present at the Si/SiO_2 interface and as such - has no effect on the barrier height lowering at the metal/SiO_2 interface. In theory, the internal photoemission of both holes and electrons is possible. However, it has been shown that the measured photocurrent is

mostly due to electrons coming from the gate for a negative gate voltage i.e. $V_g < 0$ and from the silicon substrate for a positive gate voltage i.e. $V_g > 0$. This is the direct result of higher barrier height for holes. Hence, the effective metal/SiO_2 barrier height (Φ_{beff}) can be extracted by applying a negative bias on the gate and optically exciting electrons from gate fermi level (E_F) into SiO_2 conduction band (E_C). The extracted barrier height (Φ_{beff}) is used to compute the work function of the metal gate (Φ_m) [28].

2.7.1 The Schottky Effect

In presence of an external electric field, the effective barrier height is controlled by the applied field and the "Schottky effect". When an electron travels a distance 'x' (within the oxide) from the metal-oxide interface, a positive image charge is induced in the metal. An attractive image force prevents the electron from being emitted into the SiO_2 conduction band. Under the influence of the image force, the energy barrier is no longer equal to Φ_b at the metal/SiO_2 interface and varies with distance 'x'.

When an external electric field (F) is applied across the oxide, the energy barrier (E_x) is equal to the sum of the external field component (qFx) and the image force ($q^2/ (16\pi\varepsilon_i x)$) component:

$$E_x = \frac{q^2}{16\pi\varepsilon_i x} + qFx \ , \qquad (2.11)$$

where F_x is the external field applied, ε_i is the permittivity of an oxide. This is shown schematically in Figure 2-7.

The effective energy barrier (Φ_{beff}) is slightly lower than the theoretical barrier height (Φ_b) due to the applied field and the presence of image charge. This effect is known as the

Schottky effect. Due to image force lowering, the oxide cannot completely screen the effect of the image force on the emitted carriers and hence, the dielectric permittivity for SiO_2 ($\varepsilon_i = 2.2\varepsilon_o$), used in the image force component, is slightly lower than its dc value ($\varepsilon_i = 3.9\varepsilon_o$) [21].

The energy distribution $N_i(E, h\nu)$ of the photo-excited electrons for incident photon energies ($h\nu$) greater than the theoretical barrier height (Φ_b), is illustrated in Figure 2-7.

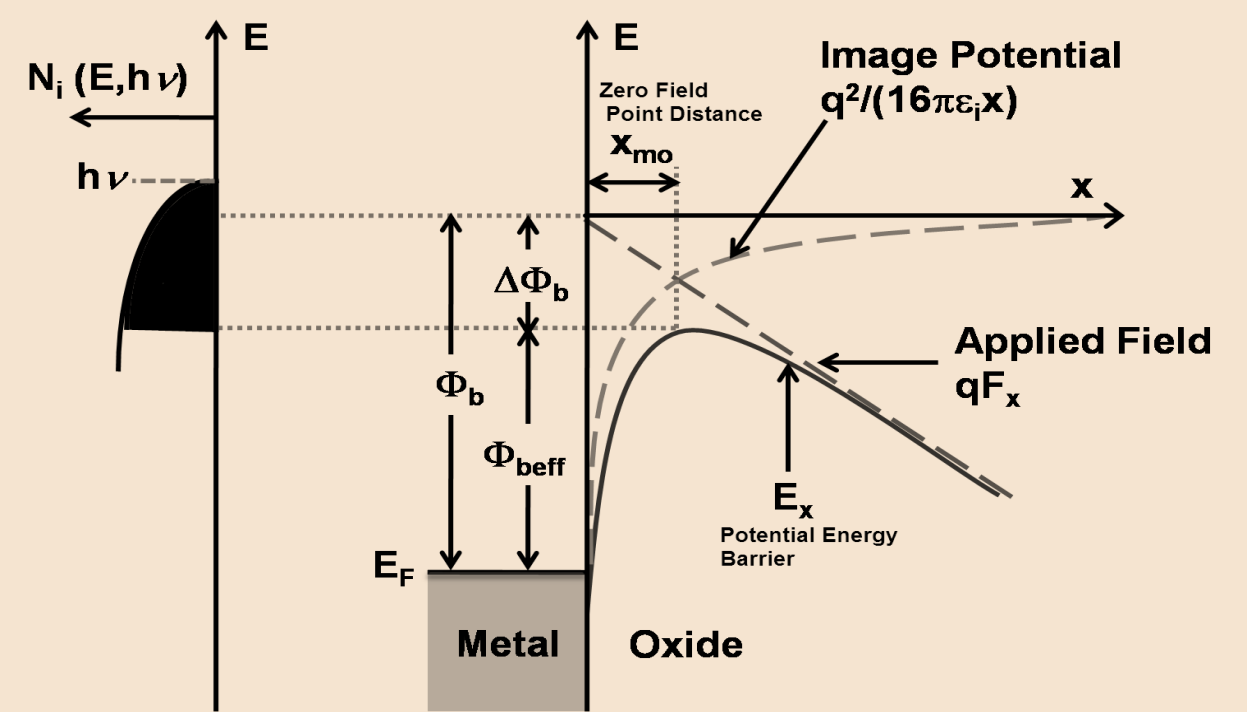

Figure 2-7: The energy band diagram of a metal/oxide interface under the influence of image force and applied field across the oxide [31].

The density of photo-excited electrons with energy greater than the effective barrier, are likely to be injected into the SiO_2 conduction band. This is indicated in the shaded portion of the distribution on the left side of the Figure 2-7. The zero field point distance (x_{mo}) is the point within the oxide from the injecting contact that corresponds to an effective electric field of zero. The zero field point is given by:

$$x_{mo} = \sqrt{\frac{q}{16\,\pi\varepsilon_i F}}, \qquad (2.12)$$

The effective barrier height (Φ_{beff}) for photoinjection is given by [24] :

$$\Phi_{beff} = \Phi_b - \Delta\Phi_b, \quad (2.13)$$

where $\Delta\Phi_b$ is the Schottky barrier lowering. The relationship between the Schottky barrier lowering and an applied electric field [21] is given as:

$$\Delta\Phi = 2Fx_{mo} = K\sqrt{F}, \quad (2.14)$$

where, K is a constant given by:

$$K = \sqrt{\frac{q}{4\pi\varepsilon_i x_{mo}}}. \quad (2.15)$$

For fields exceeding 5MV/cm, the FN tunnelling and Schottky barrier height lowering are very significant. Again, as was mentioned previously, the electric fields used were kept below 5 MV/cm for the barrier height extraction [29].

2.7.2 Barrier Height Measurement

The internal photoemission technique requires a model to account for the current as a function of electric field and illumination energy for the extraction of barrier height. At $V_g<0$ (injection of electrons from the gate), the dependence of the interface barrier heights on the applied field may be extracted with variation of energy of the photo-injection of electrons from an electrode. When a negative bias is applied at the metal gate electrode, the photo-excited electrons move towards the metal/oxide interface by an induced electric field in the oxide. The electrons in metal gate get excited by the high energy photons supplied by the illumination of a the metal gate with a beam of monochromatic ultra violet light as shown in Figure 2-8.

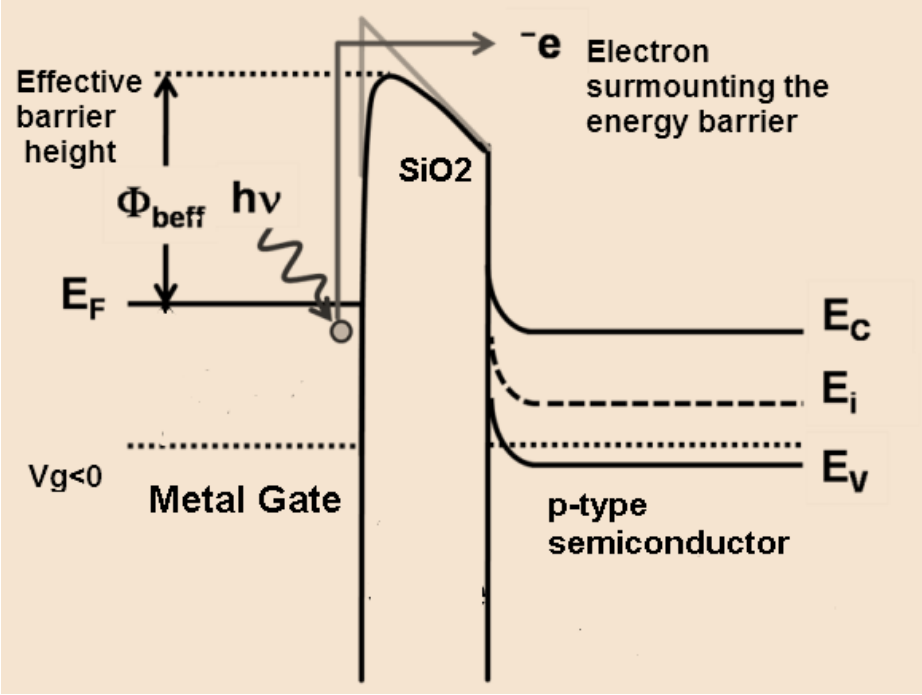

Figure 2-8: MOS capacitor illuminated with high energy photons during internal photoemission (IPE). The photo-excited electrons which have higher energy than the effective barrier height may surmount the barrier and contributes to the measured photocurrent [32]

2.7.3 Quantum yield

The quantum yield (Y) is defined as the average number of photo-excited electrons emitted per photons absorbed in the gate. [27] The quantum yield can be experimentally measured using:

$$Y = \frac{I_m h\nu}{qP_a}, \qquad (2.16)$$

where I_m is the measured photocurrent of the MOS capacitor and P_a is power of the photons absorbed by the metal gate. A plot of the photocurrent (I_m) as a function of photon energy ($h\nu$) spectrum is used to calculate the quantum yield (Y). With the increase in field, the effective barrier height is lowered and, the photocurrent and quantum yield increases [30]. The relationship between the quantum yield (Y) and the effective barrier height is given by

$$Y \propto (h\nu - \Phi_{beff})^{P}, \qquad (2.17)$$

where the values of P=2 for a metal/semiconductor interface, and P=3 for insulator/semiconductor interface have been found [27].

The effective barrier height (Φ_{beff}) is related to quantum yield by equations through:

$$\sqrt[P]{\frac{I_m h\nu}{qP_a}} \propto h\nu - \Phi_{beff} \propto h\nu - (\Phi_b - K\sqrt{F}), \qquad (2.18)$$

The effective barrier height can be extracted using above relation (2.18) by varying electric fields and plotting quantum yield $Y^{1/P}$ as a function of the photon energy ($h\nu$). This plot can be extrapolated to zero yield i.e. Y = 0 for a given applied electric field and the intercept provides the effective barrier height (Φ_{beff}) at the oxide interface. The effective barrier height (Φ_{beff}) was measured by the procedure, outlined by Felnhofer [31] and Afanas' ev [32].

A Schottky plot (Φ_{beff} vs. F) can be extrapolated to a zero field, where the intercept at F = 0, gives the zero field barrier height (Φ_b).

The sum of the zero field barrier height (Φ_b) at the metal/SiO_2 interface and the electron affinity of SiO_2 (χ_i ~ 0.9 eV) give the work function of the metal [24] as given by:

$$\Phi_m = \Phi_b + \chi_i \qquad (2.19)$$

Chapter 3 Device Fabrication

3.1 Introduction

In this chapter, the fabrication steps for a test MOS capacitor will be discussed in detail. A set of test MOS capacitors was fabricated on p-type silicon substrates. These Si substrates were chemically cleaned to remove organic contaminants and the native oxide from the silicon surface. Further, the clean silicon wafers were thermally oxidized to grow a thin layer (<50nm) of a high quality gate oxide (SiO_2).

A reactive co-sputtering deposition technique was used to deposit a blanket metal gate film on the oxidized wafer. In this work, the Hf and the Si targets were co-sputtered in plasma consisting of nitrogen (N_2) and argon (Ar). The nitrogen gas flow ratio (N_2/ (N_2 + Ar)) was varied from 10% to 30% to alter the nitrogen concentration in the HfSiN films. A lift-off process was used to define these blanket HfSiN films. This lift-off process will be defined in section 3.4. Furthermore, the test wafers were annealed in forming gas (5% H_2 in N_2) at 400^{o}C for 30 minutes to reduce the fixed oxide charge and the interface trapped charge. After annealing, the backside of the silicon wafers was etched with buffered oxide etch (BOE) and a thin layer of gallium-indium (Ga-In) was applied onto the etched areas of the silicon wafer. The Ga-In eutectic mixture diffuses into the silicon surface to create an ohmic contact.

3.2 Silicon Substrate

In this research, p-type silicon {100} wafers were used as a substrate. These 3'' diameter wafers were grown using the Czochralski (CZ) method. They were 350 μm thick and had a resistivity of ρ~ 1-10 Ω·cm.

3.2.1 RCA clean

In this section, one of the most important tasks of the fabrication, the silicon wafer cleaning, will be discussed. Since the 1950s, the cleaning of silicon wafers has been essential for the successful fabrication of VLSI devices [33]. It is necessary to remove all contamination from the semiconductor surface,-_- since 50% of the yield lossed in integrated circuit fabrication is due to the micro-contamination [34]. Wet chemical cleaning using hydrogen peroxide chemistry is one of the most used and successful techniques [33].

3.2.1.1 Wet Chemical clean method

In this work, the silicon wafers were cleaned using the recipe summarised in Table 3-1. The wafers were cleaned using an acid piranha followed by a basic piranha etching solution. To remove the native oxide from the silicon surface, hydrofluoric (HF) acid was used. Hydrochloric (HCl) acid was then used to remove any metallic contamination introduced by the HF acid.

Step 1 The acid piranha solution (5:1 H_2SO_4: H_2O_2) was prepared by adding one part of

Table 3-1: The pre-oxidation clean for the silicon wafers is shown.

Step	Process	Solutions used	Temp.(^oC)	Time (Min)
1	Acid Piranha: to remove organic residues	5:1 H_2SO_4: H_2O_2	100 ^oC (Exothermic reaction)	5
2	Wafer rinse	DI water	Room temperature	5
3	Base piranha, organic clean removes insoluble contaminants	25:2:1 H_2O : H_2O_2 : NH_4OH	60 ^oC (Heated)	5
4	Wafer rinse	DI water	Room temperature	5
5	Oxide strip – to removes thin layer of native oxide	100:1 H_2O : HF	Room temperature	3
6	Ionic clean – removes metal contaminants present in HF	100:1 H_2O : HCl	Room temperature	1

hydrogen peroxide (H_2O_2) to 5 parts of sulphuric acid (H_2SO_4). The H_2O_2 was added slowly because the chemical reaction between the sulphuric acid and the hydrogen peroxide is an exothermic process (~ 100°C) [35]. The duration of the piranha etch was 5 minutes. The wafers were oxidized during the acid piranha, because H_2O_2 is a strong oxidant. This oxide is removed with an HF etch in step 5.

Step 2 After etching the silicon wafers in acid piranha, the wafers were rinsed in DI water for 5 minutes.

Step 3 The base piranha solution (25:2:1 H_2O: H_2O_2: NH_4OH), was prepared by adding 1 part of ammonium hydroxide (NH_4OH) and 2 parts of hydrogen peroxide (H_2O_2) to 25 parts of water. To start the reaction, the solution was heated to 60°C. The duration of the etching was 5 minutes.

Step 4 After etching the substrates in base piranha, the wafers were again rinsed in DI water for 5 minutes.

Step 5 The silicon wafers were etched in a dilute (100:1) HF acid solution for approximately 3 minutes. After Hf acid etching, the silicon substrates were assumed to be very clean.

Step 6 Any metal contaminations left after the HF clean, were removed by etching the wafers in dilute hydrochloric (HCl) acid 100:1, for a minute.

3.3 Thermal Oxidation (Dry)

Oxidation is a very important process, because a stable gate oxide provides an excellent oxide/semiconductor interface that is, required for MOS technology [36]. Thermal oxidation produces the best oxides with few defects at oxide/silicon interface. The silicon wafers used in

this work, following cleaning were thermally oxidised at 1000^{o}C at atmospheric pressure in oxygen O_2. The overall reaction is given by:

$$Si(solid) + O_2(gas) = SiO_2 \quad (3.1)$$

The process of growing the oxide began with placing the silicon wafers, reaction side up, on a fused quartz boat. A 6''horizontal oxidation furnace was used for the oxidation. Before loading the samples, the temperature of the furnace was set to 800° C. The furnace was purged with nitrogen until it reached the desired temperature. After the quartz boat and the quartz rod were cleaned using the isopropyl alcohol (IPA), the quartz boat was placed at the end of the furnace tube and pushed into the furnace with the quartz rod.

After loading the wafers, the furnace was set to ~1000^{o}C. To initiate the oxidation process, ultra-pure dry oxygen (O_2) was introduced into the furnace tube. The silicon surface reacted with the oxygen molecules which diffuse to the silicon surface and form a silicon dioxide film [37].

Once the oxidation process was finished, the reaction was stopped by cutting the oxygen supply and the power supply to the furnace. While the furnace was cooling down, it was purged with N_2. When the furnace had cooled to room temperature, the samples were unloaded from the furnace. This process was repeated for a variety of times to produce a series of samples with different oxide thickness.

3.3.1 Oxide Thickness Measurement

There are several ways for characterizing the oxide thickness [35]. In this work, one of the methods used was the Nanometrics Nanospec 210 measurement system which is an optical, non-contact and a non-destructive technique. In this technique, a beam of light is incident normal

to the surface of the film. The thickness of a film is characterized by measuring the intensity of the reflected light as a function of incident wavelength (λ). When the incoming and outgoing waves interfere constructively, an optical maximum will be observed and when the waves interfere destructively, a minimum is observed. The thickness of the film can be determined by taking the difference between the maxima and the minima [35]. Using the Nanospec, films in this work were found to be between ~10nm to ~50 nm (O_2 at 1000° C), for oxidation times ranging from 20 minutes to 1 hour.

Another method, from which the oxide thickness may be extracted, is the high frequency capacitance voltage (HFCV) technique. The value of the oxide thickness was obtained from the measured oxide capacitance (C_{ox}) in accumulation using the equation:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}}, \qquad (3.2)$$

where ε_o is permittivity in free space, ε_{ox} is the relative permittivity of the dielectric (ε_{ox} =3.9 for SiO_2), A is the area of the gate electrode and t_{ox} is the gate oxide thickness.

3.4 Lift-off Process

A lift off process was used in this work, for patterning the metal gate films which used a sacrificial layer of photoresist (PR) [38]. To pattern a film using a "lift off" process, an inverse pattern (negative mask) of the desired shape must be used. The steps for this process are described below and are illustrated in Figure 3-1 below.

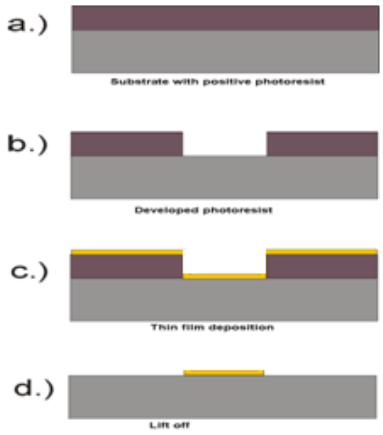

Figure 3-1: Lift off process used for gate metal patterning.

3.4.1 Photoresist Spin Coating

For the lift off process used in this work, a thick coating of a photoresist was used to pattern the metal gate films for the test MOS capacitors. The positive resist used in this work was HPR- 504. One of the conventional methods used to deposit a photoresist layer onto the flat silicon wafer is via spin coating [39]. For the capacitors, the positive resist was spin-coated onto the wafer using a Machine World photoresist spinner at 2500 rpm (rotations per minute) for 40 seconds. The test wafers were held by a "vacuum chuck" during the entire spinning process. A surface profiler was used to measure the thickness of the spin coated photoresist. It was found to be ~1.8 µm thick. The photoresist was baked at 110°C for ~ 60 seconds to harden the photoresist. The samples were then cooled to the room temperature.

The photoresist coated wafer was developed in a developer solution to open the pattern deposited films which follow the desired thin metal gate film (HfSiN) deposition onto the patterned wafer using the co-sputtering technique. The metal gate film deposition is described in section 3.5. The "lift off", of the unwanted material, was performed using acetone solution. The unwanted metal deposited on the resist, "lifted off" the wafer as the acetone dissolved the

photoresist using ultrasonic agitation. The samples were immersed in the ultrasonic acetone bath until the photoresist film was completely removed [35].

3.4.2 Mask

A mask is a substrate with several sets of shaded geometric features. For standard process, it is a glass plate with chrome shapes. This mask is used to transfer the geometric shapes onto the photo-resist and subsequently onto the metal film. To expose the positive photoresist, a positive mask, where the desired shapes are the opaque regions of the mask, was used. For this research project, a set of square features with areas (2.5×10^{-3}, 4×10^{-4}, and $1\times10^{-4)}$) cm^2 were used to transfer the patterns onto the blanket films. An enlarged view of the square features (on the mask), is shown in Figure 3-2.

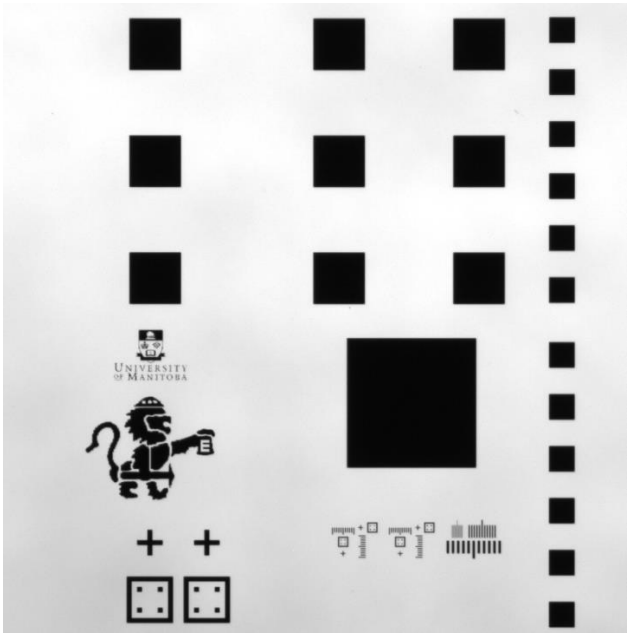

Figure 3-2: Top view of a positive mask with squares varying in sizes, 2.5×10^{-3}, 4×10^{-4}, and 1×10^{-4} $cm^{2.}$

3.4.3 Contact-mode Photo-Lithography

In this work, contact mode photolithography was used. In this form of lithography, the mask is pressed against the photoresist coated wafer during exposure. An ABM 6-inch two-sided Mask Aligner was used where the mask was placed chrome side down on the vacuum mask holder. The wafer was then placed onto vacuum chuck.

The wafer and mask were aligned using vernier screws. After aligning the mask with the wafer, the wafer and the mask were clamped together to make a contact. Ultra-violet (UV) radiation, from a high intensity 200W Hg Arc lamp, was used to expose the wafer through the mask for 12 seconds. The areas of the wafer not shaded by the opaque features on the mask were exposed to the UV light. The UV light exposure changes the PR bonding, reducing the cross-linking photoresist making it removable with the developer.

After the exposure, the wafer was unloaded from mask aligner and placed in a bath containing a Microposit™ 352 positive photoresist developer solution for 30 seconds. The samples were then immediately rinsed in DI water and blown dry with N_2. A final hard bake, at 120°C for 30 minutes, assisted in hardening of the photoresist for the following sputtering deposition of the metal films.

3.5 Metal Gate Deposition

In order to create the test MOS capacitors, a deposition of a metal onto the gate dielectric is required. In this research, the $Hf_xSi_yN_z$ (HfSiN) film was used as the metal gate material for the MOS capacitors. To deposit the blanket HfSiN films, a sputtering method was chosen over other deposition methods because sputtering provides high quality thin films and an inexpensive and controllable deposition method.

The process of sputtering, involves the ejection of molecules from the target surface of material to be deposited by the action of the positive ions of an inert gas like argon [40] as shown in Figure 3-3. The blanket HfSiN films were deposited using a reactive (simultaneous) co-sputtering of Hf and Si in argon/nitrogen plasma. The Hf and Si targets were sputtered using DC and RF biases respectively. The different sputtering techniques are described in the following sections.

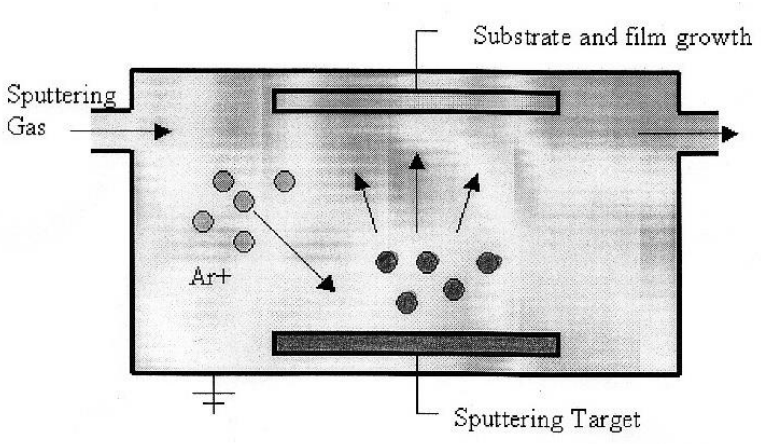

Figure 3-3: A basic reactive sputtering process

After annealing, the blanket HfSiN films were found to be thermally stable and had good physical and electrical properties.

3.5.1 Co-Sputtering

Co- Sputtering may be performed by sputtering two or more targets at the same time, each sputtering a different material on to the same substrate [40].

The required HfSiN films were deposited by co-sputtering Hf and Si targets in the presence of an Ar/N_2 plasma. After loading the sample into the chamber, the pressure was reduced to 2×10^{-6} Torr. A 50W DC bias and 75W RF bias were applied to generate the

plasma in the chamber. Mass flow controllers were used to control the flow of the N_2 and Ar ultimately controlling the chamber pressure. In order to vary nitrogen content in films, the gas flow ratio (N_2/ (N_2 +Ar)) was varied from 10%-30% as shown in Table 3-2. The deposition pressure was 12mTorr and the deposition time was 30 minutes. The deposition pressure was kept low, so as to deposit low resistivity thin films by sputtering [42].

Table 3-2: The gas phase ratio (R_N) was varied from 10% to 30% by regulating the flow rate (sccm) of the argon and nitrogen.

Ar (sccm)	**N_2 (sccm)**	**Gas flow ratio $R_N = (N_2/ (N_2 + Ar))$**
54	6	10%
48	12	20%
37.28	16	30%

3.5.2 DC and RF Sputter Deposition

The DC sputtering involves bombarding a target material by the energized ions. The particles from the target are deposited onto the substrate. The negative DC bias produces an electric field which ionises the gas in the chamber to create "plasma". The positively charged ions are attracted towards the negatively biased target plate. The sputter deposition was carried out using the Semicore DC/RF sputtering system.

The Semicore sputtering system uses powerful magnets (Magnetron Sputtering), which confine the plasma along the magnetic field lines. These magnets assisted in maintaining higher density plasma near target which enhanced the deposition rate. The magnetron sputtering allows the plasma to sustain at lower deposition pressures.

The wafer was placed on a rotating substrate plate inside vacuum chamber. For uniform deposition, the chamber pressure was pumped down to a base pressure of 2×10^{-6} Torr. A noble

gas such as argon was let into the chamber raising the chamber to desired deposition pressure of ~10^{-3} Torr. The DC sputtering is used for deposition of conductive materials.

Like DC sputtering, the RF sputtering process involves the physical removal of particles from the target material by the striking of high velocity ions (argon ions). These positive ions strike the target material, causing material from the target to be ejected and form a thin film coating on the substrate. RF sputtering can be used for deposition of non-conductive materials.

3.5.3 Film Thickness Measurement

A Veeco Multimode scanning probe microscope (SPM,-in contact AFM mode) was used to measure the film thickness. The microscope tip was scanned in close contact, across a step at the edge of the patterned region. The step height was equivalent to the thickness of the deposited film. It was found that an increase in gas flow ratio reduced the deposition rate and therefore the thickness of HfSiN films. The results are shown in Table 3-3.

Table 3-3: The thickness of HfSiN films decreased for gas flow ratios from 10% to 30%

Gas flow ratio	**HfSiN Film Thickness (nm)**				**Avg. HfSiN Thickness (nm)**	**Deviation (nm)**
	A	**B**	**C**	**D**		
10%	107	112	105	118	110.5	5.02
20%	79	66	71	74	72.5	4.71
30%	58	49	57	54	54.5	3.5

The HfSiN deposition rate (nm/min) was calculated by taking a ratio of the average film thickness (nm) over the deposition time (min). These deposition rates were used to limit the thickness of the reactively sputtered HfSiN films to ~110nm for all gas flow ratios. As the gas flow ratio increased from 10% to 30% the thickness of HfSiN films decreased from 110 ± 5 nm to 54.5 ± 3.5 for a 30 minute deposition.

3.6 Electrical Resistivity (ρ) Measurement

A 4 point probe was used for measuring the sheet resistance of the sputtered films. A schematic diagram of a four point probe resistance measurement setup is shown in Figure 3-3. With four equally spaced probes, in contact with a material, the outer two probes (1 and 4) were used to source a small current and the inner two probes (2 and 3) are used to measure the voltage drop across the sample. The electrical resistivity (ρ) of the HfSiN films was calculated using the equation

$$\rho = R_s W \ , \qquad (3.2)$$

where R_s is the sheet resistance measured using 4 point probe measurement and W is the thickness of the HfSiN sputtered film.

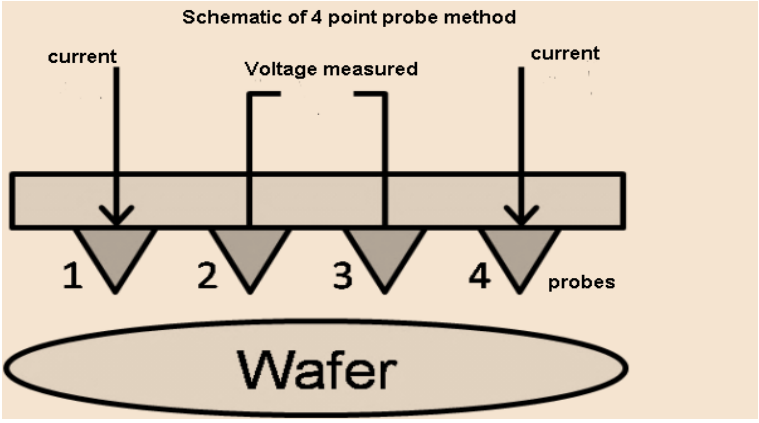

Figure 3-4: The schematic diagram of a four point resistance method.

Table 3-4: The average electrical resistivity (ρ) of the HfSiN films, measured using the 4-point probe method.

Gas flow ratio	**Avg. Dep. Rate (± 0.5 nm/min)**	**Film thickness (± 5 nm)**	**Elec. Resistivity (ρ) (± 4 μΩ.cm)**
10%	4	121	41 ± 4
20%	3.2	95	72 ± 2
30%	3	91	120 ± 5

In Table 3-4, the measured electrical resistivity and the deposition rate of the HfSiN films are shown to be dependent on gas flow ratios. With increasing gas flow ratios, the electrical resistivity (ρ) of the HfSiN films was found to be increasing steadily. Various electrical measurements were performed to optimize the HfSiN work function by adjusting the N_2 contents during the reactive co-sputtering. It is clear that the sputtering gas composition affects the electrical resisitivity of these reactively sputtered HfSiN films.

3.7 Aluminum gate Deposition

As a reference metal with known work function, aluminum (Al) blanket films (Φ_m ~ 4.1eV) were deposited on the same gate oxides as the HfSiN films. Aluminum can be deposited by thermal evaporation or the conventional DC sputtering technique. For this work, both the methods were used for aluminum deposition.

For the thermal evaporation, the already oxidised wafers were placed in an evaporation chamber. The base pressure in the deposition chamber was maintained at 10^{-6} Torr. The wire of

aluminum was wrapped onto tungsten rod from which it was evaporated and deposited onto the wafer. The thickness of the deposited aluminum film was measured as 120 Å. The deposition rate was measured using the crystal oscillator thickness monitor inside the evaporator and was found to be approximately 1.8A°/s.

The other method used for aluminum deposition was DC sputtering. The oxidised wafers were placed in the sputtering chamber. The chamber was pumped down to 10^{-6} Torr. Argon gas was then directed into the chamber. Using a power of 200 W DC, the aluminum target was exposed to the bombarded argon plasma forming a thin film of aluminum on the surface of the wafer. The deposition time was 2 minutes. During the deposition, the pressure was 10mTorr; the argon flow rate was 40 sccm. A 200 W DC power setting was applied between the aluminum target and the substrate plate.

3.8 Forming Gas Anneal

A forming gas (5% H_2 in N_2) anneal at 400 °C for 30 minutes was used to passivate the SiO_2/Si interface. At Si/ SiO_2 interface, the unsatisfied Si bonds can be electronically nuetralised if they are bonded to hydrogen from the FGA. This FGA reduces the interface state density.

In Figure 3-5, the high frequency capacitance voltage curve of HfSiN metal gate MOS capacitor is shown before and after a 30 minute forming gas anneal. This shift in the CV curve is indicative of a reduction in defects in the film or at the silicon interface.

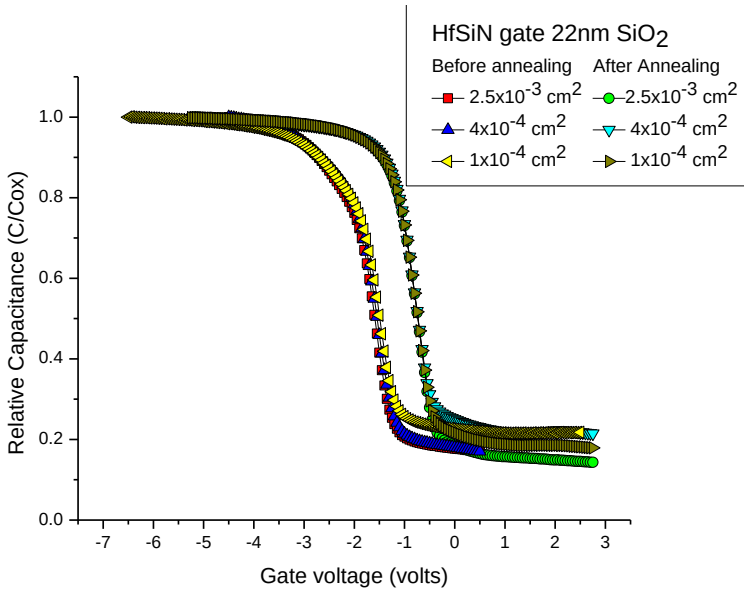

Figure 3-5: MOS capacitor (HfSiN/ SiO_2/Si) before and after forming gas anneal at 400° C for 30 minutes.

Chapter 4 Experimental Setup

4.1 Introduction

The measurement setup, apparatus and the testing procedures for the various experiments used in this research will be introduced in this chapter. Several electrical and the optical characterization measurement techniques that were used will be described. These measurement techniques were controlled from a computer using an off-the-shelf measurement program called "LabVIEW". For each measurement technique, a schematic description of the devices under test (DUT) is provided in the following sections.

4.2 Basic Experimental Setup

A personal computer (PC) was used to carry out several automated measurements. For all these tests, the equipment was connected to the device under test (DUT) through a Keithley 7002 switch matrix which allowed switching between each of the different measurements. The measurements used included several techniques such as the current-voltage (IV) measurements and the high frequency (100 KHz) capacitance-voltage (HFCV) measurements. During these measurements, contact to the DUT the MOS capacitors was facilitated by a Cascade Microtech probe station. For the optical measurements, a photo-detector was used with a monochromator to obtain the optical spectra of the UV mercury arc light source. This light was used for internal photoemission barrier height measurements. All of this equipment was interfaced to a PC via either a GPIB (IEEE488) or an RS-232 bus.

4.2.1 Probe Station

The current-voltage and the capacitance-voltage measurements were performed using Keithley 237 high voltage source measurement unit (SMU) and the Hewlett-Packard HP 4284A (Precision LCR meter, respectively). These measurements were carried out with the sample inside the probe station which had a light-tight shielded box, to avoid electrical and optical interference.

To create a good ohmic back contact on the devices to be measured, a thin layer of gallium-indium (Ga-In), was applied on the backside of the sample. The sample was then placed on a sample holder. The sample holder consisted of an aluminum vacuum chuck and a copper plate to make an electrical contact to the substrate. For all electrical measurements, a small tungsten probe was used to contact the top contact of the test MOS capacitor. The tungsten probes have a very small tip (~ 1μm-radius of curvature) and were aligned for contact to our devices using the microscope in the probe station. This allowed the measurements of even the smallest devices on the wafer to be tested. The CV and IV measurements were both performed in the dark with the sample enclosed in the probe station. The schematic diagram of the apparatus for these measurements is shown in **Figure**.

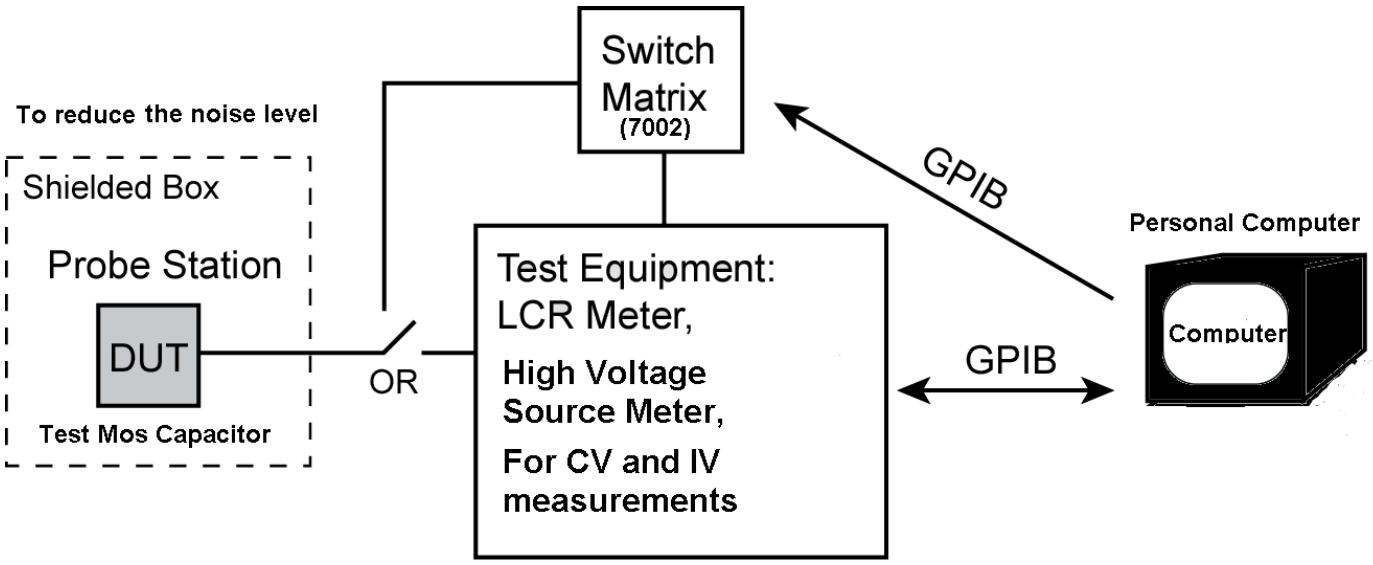

Figure 4-1: The measurement setup for capacitance-voltage (CV) and current-voltage (IV) measurements. The test capacitors were connected to the test equipments through a Keithley 7002 switch matrix .

4.3 Experimental Set up

4.3.1 HFCV Measurement

The HP 4284A LCR meter was used to measure the MOS capacitance as a function of applied gate voltage. The flat-band voltage (V_{FB}), the work function difference (Φ_{ms}) and other important electrical parameters of a MOS capacitor, including the oxide thickness, oxide charge, and doping concentration, were extracted from these HFCV data. The high frequency capacitance-voltage measurements were taken using a small peak to peak AC signal (typically 30mVat 100 KHz) which was superimposed upon the applied DC gate voltage. The silicon substrate of a test MOS capacitor was grounded and the bias was applied to the gate electrode. The DC voltage was slowly swept from the "inversion regime" into the accumulation regime of the MOS capacitor, as described previously in Chapter 2.

4.3.2 Current-Voltage Measurement

Using the Keithley 237, the ramped voltage was applied to the gate electrode and the silicon substrate was grounded. The measured current consists of a displacement current and a particle current. This particle current results from the charge that passes through the oxide while the displacement current results due to the movement of charge to "charge the plates" of the capacitor which results when there is a change in the applied potential. The displacement is given by

$$I = CdV/dt \tag{4.1}$$

4.3.3 Photo-detector Measurement

An external light source was required for the photoemission measurements. To calibrate the photoemission apparatus, a detailed knowledge of the Hg-lamp spectra was required. The apparatus used for these calibration measurements is shown in Figure 4-2. A Keithly 237 high voltage source measurement unit (SMU) was used to measure the photodiode current while the mercury arc lamp (Oriel 6823), provided the photons with energies in the spectral range varying from (1.5 eV to 6.0 eV). The spectrum of this mercury arc lamp has a series of high intensity peaks in the near-UV region (200-600nm). A focussing lens was used to focus the output of a lamp onto the input of the monochrometer to ensure maximum possible photo intensity .A shutter was also used to enable the measurements that could be done in the dark.

For barrier height measurements, a high resolution (~2nm) diffraction grating obtained from the monochrometer, was used. A linear wavelength sweep was performed varying the wavelength of the light from 200nm to 600nm. To measure the intensity of photons at a given wavelength and therefore energy, a calibrated silicon photodiode (Newport 818-UV) was used.

These photodiode measurements were performed for calibration of the light source. Many measurements of the spectra were performed.

To be able to perform and the photo-emission measurements and extract barrier heights and work-function, a detailed knowledge of the photon flux impinging on the sample is required. This is required to enable the calculation of the internal quantum efficiency (i.e. number of electrons excited per photon) of our devices. The silicon photodiode is responsive to energetic photon with energies greater than the Si band gap ~ 1.12 eV. The incident photons, with enough energy excite the carriers within the silicon photodiode and produce a photodiode current (I_{diode}). The absorbed power (P_a) of these incident photons and the incident photon flux (F_{ph}) was calculated using the photodiode current.

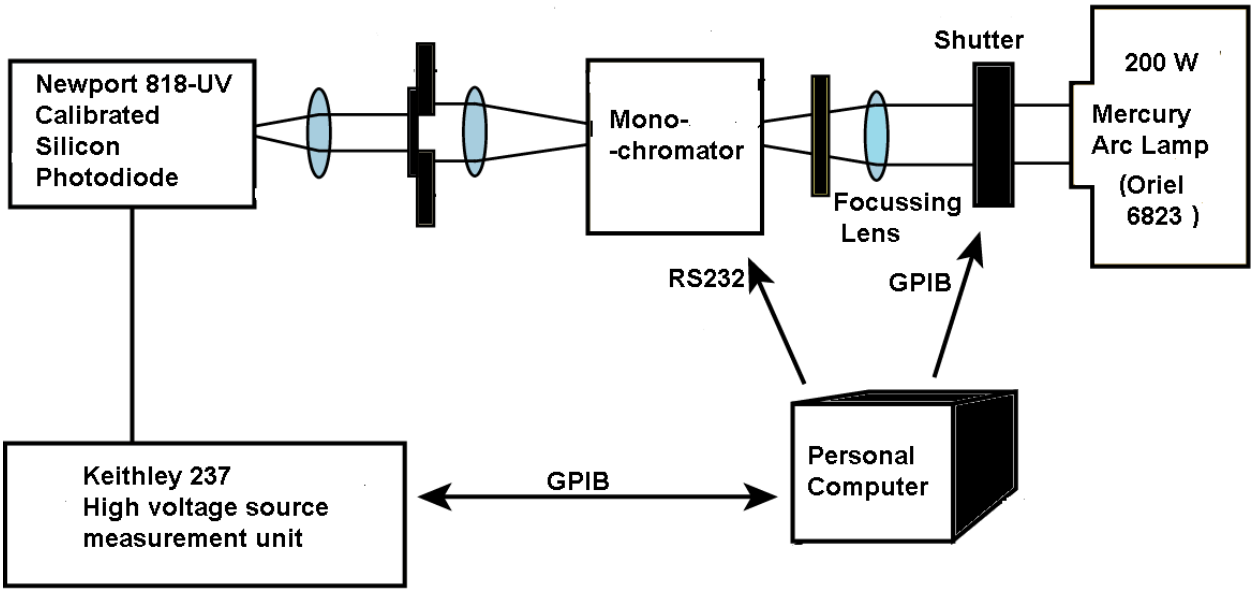

Figure 4-2: The apparatus for the photo-detector measurements. The optical spectra of the light source were obtained using these measurements.

4.3.4 Barrier-Height Measurement

The effective barrier height may be determined using the photoinjection and/or optical absorption measurements. For this work, the measurement apparatus for the barrier height measurements, similar to that used for calibration, is shown in Figure 4-3. As with the calibration, the apparatus consisted of an external light source, an arc lamp, a monochrometer, shutters, filters, lenses and a sample holder. For the duration of the barrier height measurements, a constant bias (no displacement current) was used to measure the electron particle current. The output slit of monochrometer was connected to an optical fibre bundle (Newport 77577). This optical fibre bundle consisted of a light guide and a focussing lens at the output end.

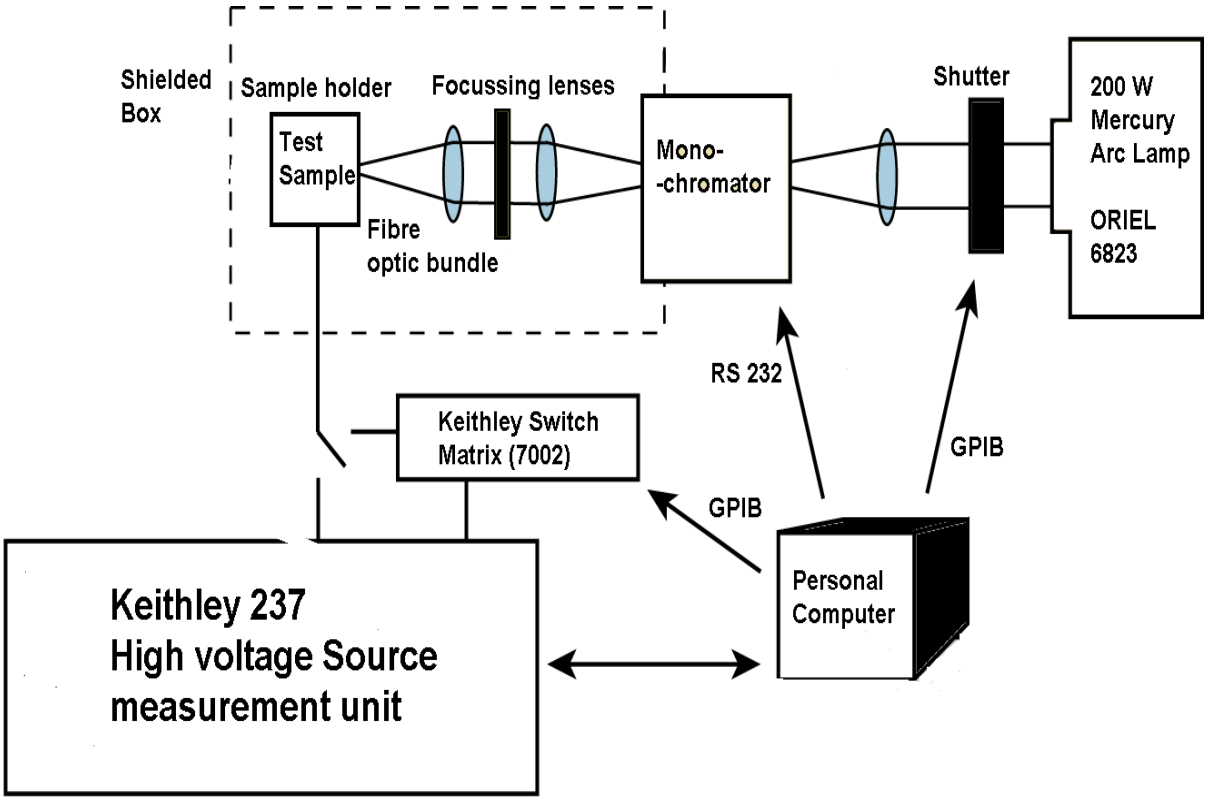

Figure 4-3: The measurement setup for the barrier height measurements.

A lens was placed near the exit slit of the monochrometer to collimate the beam before it is focused onto the sample. The output of the fibre bundle was then focussed onto the sample to

obtain the maximum photon intensity. When the external light source illuminated the gate electrode area, the electrons in the gate electrode were optically excited. If the electrons had gained enough energy from the absorbed photons, they would be emitted over the barrier into the gate dielectric and generate a current. For these measurements, the substrate was grounded and the DC bias (-ve) was applied to the gate continuously. The wavelength of the optical source was swept from high (200nm) to low (600nm) photon energy (hν). A Keithley 237 High voltage source measurement (SMU) was used to measure the photocurrent.

Chapter 5 Electrical and Optical Characterization Results

5.1 Introduction

In this research, the HfSiN metal gate MOS capacitors were characterized electrically and optically using high frequency capacitance voltage (HFCV) and internal photoemission (IPE) characterization techniques, respectively. The basic theory and the measurement setup for both the techniques have already been discussed in Chapter 2 and Chapter 4, respectively. These electrical and optical characterization techniques were used to determine the work function tuning of reactively co-sputtered HfSiN metal gate films that were adjusted through the adjustment of the nitrogen incorporation (see Chapter 2).

5.2 High Frequency Capacitance-Voltage (HFCV) Characterisation Results

The high frequency capacitance-voltage (HFCV) response and the various measurement parameters of a MOS capacitor will be discussed in this section. As an example, the measurement results of 10% ($HfSiN/SiO_2/Si$) device will be discussed in this chapter. This device had HfSiN as a metal gate, which was reactively co-sputtered at 10% (N_2/ (N_2+Ar)) gas flow ratio, on a 22nm SiO_2 over p-type silicon substrate.

5.2.1 Oxide Thickness (t_{ox})

The oxide thickness measurements were obtained from the high frequency capacitance voltage (HFCV) curve and from the Nanospec system. The thickness of gate oxide (t_{ox}) of a

MOS capacitor was extracted from a high frequency capacitance voltage (HFCV) curve using a relationship between the maximum capacitance (C_{ox}) in accumulation and the oxide thickness (t_{ox}) which is given by:

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}}, \qquad (5.1)$$

where ε_o (= 8.854×10^{-14} F/cm^2) is permittivity of free space, ε_{ox} (= 3.9 for SiO_2) is the relative dielectric permittivity of the SiO_2 and A is the area of the gate electrode.

For the devices used in this study (p-type MOS capacitors), the oxide capacitance was measured in accumulation regime of the HFCV curve. The measured oxide capacitance (C_{ox}) is linearly dependent on the gate area. The HFCV measurement results were primarily extracted from capacitor with three different areas; 2.5×10^{-3} cm^2, 4×10^{-4} cm^2 and 1×10^{-4} cm^2 for the same oxide sample.

The HFCV response of MOS capacitors for the three different gate areas is shown in Figure 5-1. The area scaling of the capacitors is evident from the overlapping of the curves.

The oxide thicknesses (t_{ox}) obtained from Nanospec measurements are listed in Table 5-1 and the HFCV measurement results are listed in Table 5-2. These two independent measurements of the oxide thickness are in good agreement with each other.

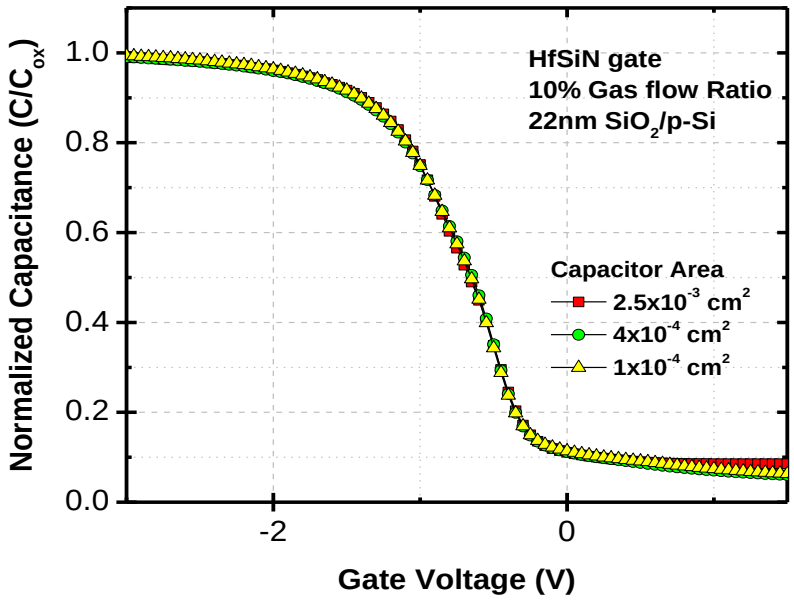

Figure 5-1: The oxide capacitance per unit area as a function of applied gate bias for an HfSiN/SiO_2/p-Si capacitor. The gate oxide thickness was 22 nm.

Table 5-1: The average oxide thickness obtained using the Nanospec system from the dry oxidation of silicon at 1000°C. The oxidation time ranged from 20 minutes to an hour.

Oxidation time (min)	Oxide Thickness (nm) obtained from Nanospec						
	Wafer Samples					Average (nm)	Std. Dev. (nm)
	A	B	C	D	E		
20	16.1	17.4	15.0	15.6	16.3	16.08	0.72
30	19.5	22	19.9	21.9	20.7	20.8	1.1
40	22.9	23.9	24.5	23.4	22	23.34	1.12
50	28.5	27.8	28.2	28.4	27.8	28.14	0.71
60	31.8	34.2	33.6	34.9	34.7	33.84	1.21

Table 5-2: The average oxide thickness obtained from the HFCV measurements from the dry oxidation of silicon at 1000°C. The oxidation time ranged from 20 minutes to an hour.

Oxidation time (min)	Oxide Thickness (nm) obtained from HFCV Measurement						
	Wafer Samples					Average (nm)	Std. Dev. (nm)
	A	B	C	D	E		
20	17.2	16.5	17.1	16.4	17.2	16.88	0.38
30	20.3	21.2	21.8	20.7	20.6	21	0.5
40	23.9	23.7	24.6	24.1	23	23.86	0.588
50	29.4	28.5	29.4	29.7	27	28.56	1.1
60	35.6	36.1	34.7	34.5	34	34.98	0.93

5.2.2 Substrate Doping Concentration (N_a)

As previously discussed in Chapter 2, the HFCV measurement results can also be used to calculate the average acceptor doping concentration (N_a). For this calculation, the maximum capacitance (C_{ox}) in accumulation, and the minimum capacitance (C_{min}) in inversion are required and were extracted from the HFCV curve. To obtain these maximum and minimum capacitance values, the measurements were performed on the samples from the same oxide film and averaged them. From the maximum-minimum capacitance method, an average value of the acceptor doping for a uniformly doped p-type silicon substrate was calculated as shown in Table 5-3. The substrate used in this work, was a p-type silicon wafer, which had a resistivity (ρ) of ~1-10 Ω·cm. This resistivity value corresponds to a doping concentration (N_a) between 1.5×10^{16} and 1.3×10^{15} cm^{-3}. The minimum capacitance (C_{min}) is inversely dependent on the maximum depletion width (W_{dmax}) and hence, to the doping concentration (N_a), which is shown as:

$$C_{\min} = \frac{\varepsilon_o}{t_{ox} + \frac{\varepsilon_o}{\varepsilon_{si}} W_{d\max}} = \frac{\varepsilon_o}{t_{ox} + \frac{\varepsilon_o}{\varepsilon_{si}} \sqrt{\frac{2\varepsilon_o \varepsilon_{si} \psi_s}{qN_a}}}, \quad (5.2)$$

Table 5-3: Using the maxima-minima capacitance method, the average acceptor doping concentration (N_a) for p-type Si substrate was calculated.

Oxide Thickness t_{ox} ± 0.7 (nm)	**Gate Area (cm^2)**	**Oxide Capacitance C_{ox} ($\times 10^{-7}$ F/cm^2)**	**Min Capacitance C_{min} ($\times 10^{-7}$ F/cm^2)**	**Sub. Doping N_a ($\times 10^{15}$ cm^{-3})**
16.08	2.5×10^{-3}	1.74	0.29	1.21
16.08	4×10^{-4}	1.89	0.31	1.24
16.08	1×10^{-4}	1.85	0.32	1.19
Avg. Doping Concentration (N_a) = (1.21 ± 0.03) × 10^{15} cm^{-3}				
20.8	2.5×10^{-3}	2.22	0.26	1.20
20.8	4×10^{-4}	2.31	0.28	1.22
20.8	1×10^{-4}	2.26	0.25	1.25
Avg. Doping Concentration (N_a) = (1.22 ± 0.03) × 10^{15} cm^{-3}				
23.34	2.5×10^{-3}	1.96	0.21	1.18
23.34	4×10^{-4}	1.85	0.19	1.16
23.34	1×10^{-4}	2.00	0.23	1.15
Avg. Doping Concentration (N_a) = (1.16 ± 0.03) × 10^{15} cm^{-3}				
28.14	2.5×10^{-3}	1.62	0.21	1.19
28.14	4×10^{-4}	1.71	0.24	1.22
28.14	1×10^{-4}	1.68	0.18	1.21
Avg. Doping Concentration (N_a) = (1.20 ± 0.03) × 10^{15} cm^{-3}				
33.84	2.5×10^{-3}	1.12	0.17	1.17
33.84	4×10^{-4}	1.29	0.19	1.23
33.84	1×10^{-4}	1.22	0.20	1.16
Avg. Doping Concentration (N_a) = (1.18 ± 0.05) × 10^{15} cm^{-3}				

The extracted average value is 1.2×10^{15} $cm^{-3,}$ which is close to the expected doping concentration range (1.5×10^{16} cm^{-3} to 1.35×10^{15} cm^{-3}).

5.2.3 Flat-Band Voltage (V_{FB})

As a bias is applied, the energy bands in the semiconductor change and "bend". At a particular bias, the bands are "flat". This bias is the "flatband" voltage. One of the methods to calculate the flatband voltage is through the flatband capacitance (C_{FB}). As discussed in Chapter 2, the flatband capacitance can be calculated by using the values of extracted oxide thickness (t_{ox}) and average doping concentration (N_a).

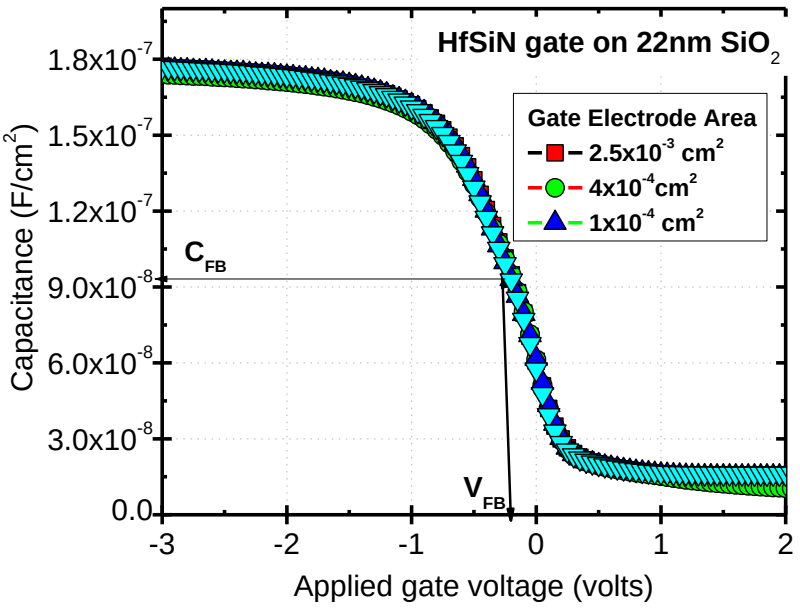

Figure 5-2: The flat band capacitance and the flatband voltage determined from the high frequency capacitance-voltage (HFCV) curve of the HfSiN,SiO_2/Si.

Furthermore, the flatband voltage (V_{FB}) can be extracted from the HFCV curve and is the bias at which the capacitance is equal to the "flatband" capacitance (see Figure 5-2).

Another method that may be used to calculate the flatband voltage is to use a reference metal with a known work function. When both the metal gates are deposited onto the same oxidized wafer, the difference between the two HFCV curves will represent the difference in their work functions. As the work function of the reference metal is known, the work function of the other metal can be easily calculated from the voltage shift. In this work, Aluminum with known work function (Φ_m ~ 4.1eV) was used as a reference metal gate.

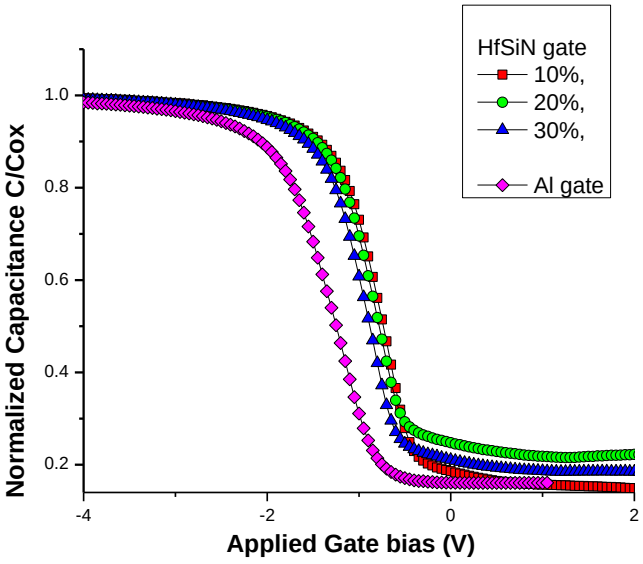

Figure 5-3: The HFCV curves for HfSiN/22nm SiO_2/Si and Al capacitors. For comparison, aluminum gate reference capacitors were also fabricated on the same oxide.The area of capacitor is 2.5×10^{-3} cm^2.

In Figure 5-3, the HFCV response of the different HfSiN gate MOS capacitors, is shown for metal gates, which were reactively co- sputtered with varying nitrogen and argon partial pressures. When the gas flow ratio (N_2/ (N_2 + Ar)) increased from 10% to 40%, the HFCV curves were found to shift towards greater negative values in a parallel manner.

5.2.4 Work Function Difference (Φ_{ms})

Assuming there that the, interface or oxide charge is negligible, the measured flatband voltage (V_{FB}) may be considered to be "ideal" and therefore is simply equal to the work function difference (Φ_{ms}). If a metal work function (Φ_m) in a MOS device is greater than the silicon work function (Φ_s) i.e. $\Phi_m > \Phi_{s,}$ the work function difference Φ_{ms} will be positive and the flatband voltage will shift towards greater positive voltages. If the work function difference is negative for $\Phi_m < \Phi_s$, the flatband shifts towards greater negative voltages.

In MOS devices, while the work function of the metal gate can cause a change in the flatband voltage, the charge trapped within the film or at the interface will also affect the V_{FB}. As discussed in Chapter 2, the flatband voltage (V_{FB}) and the oxide thickness (t_{ox}) relationship can be used to calculate both the work function difference (Φ_{ms}) and the oxide charge density (Q_{ox}). The flatband voltage method requires capacitors with several oxide thicknesses.

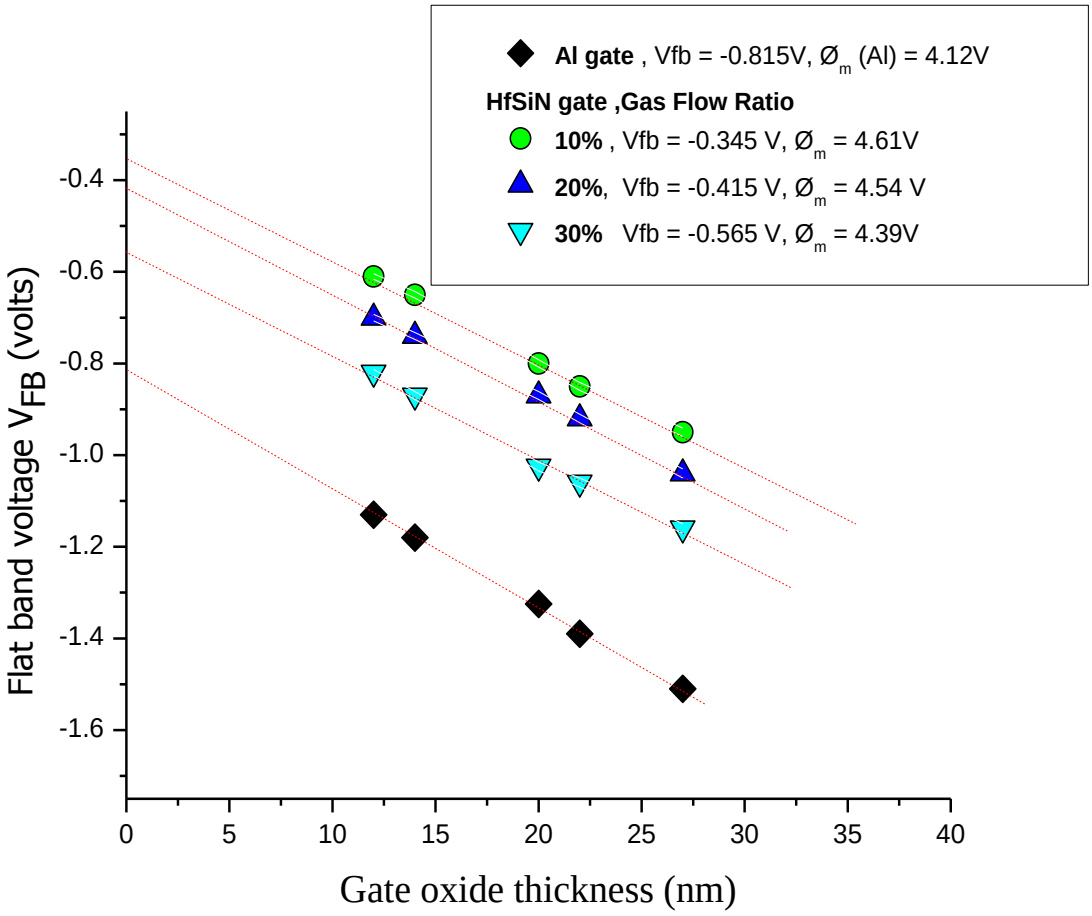

Figure 5-4: A plot of flat-band voltage(V_{FB}) as a function of SiO2 thickness for HfSiN and Al gate capacitors. A linear fit to the data are shown by the dashed lines.

In Figure 5-4, the extracted flatband voltages (V_{FB}) are plotted as function of the oxide thickness (t_{ox}). In this case, the V_{FB} vs. t_{ox} plot exhibits a linear relationship for all gate stacks. From the extrapolation of the linear data at zero oxide thickness (t_{ox} = 0), the flatband voltage may be extracted. This flatband voltage (V_{FB})at this point- is equal to the work function difference (Φ_{ms}), from which the workfunction of a metal may be obtained. The oxide charge density (Q_{ox}), can be extracted from the slope of this data. In Table 5-4, the extracted values of

flatband voltage (V_{FB}) for the aluminum gate electrode for the different oxide thicknesses (t_{ox}) are shown.

Table 5-4: The extracted flat-band voltages (V_{FB}) and the work function of the Aluminum gate capacitors.

Flatband Voltages (V_{FB}) and Work Function (Φ_m) for the Aluminum Gate						
Oxide Thickness t_{ox} ± 0.7 (nm)					**V_{FB} @ t_{ox} = 0 (V)**	**Φ_m (eV)**
12	**14**	**20**	**22**	**27**		
-1.13	-1.18	-1.319	-1.39	-1.51	-0.815 ± 0.011	4.12 ± 0.03

Table 5-5: The extracted flat-band voltages and the work function of HfSiN gate MOS capacitors.

Flatband Voltages (V_{FB}) and Work Function (Φ_m) for the HfSiN Gate							
Gas Flow Ratio (%)	**Oxide Thickness t_{ox} ± 0.7 (nm)**					**At t_{ox} = 0, $V_{FB} = \Phi_{ms}$ (V)**	**Φ_m (eV)**
	12	**14**	**20**	**22**	**27**		
10%	-0.61	-0.64	-0.79	-0.85	-0.95	-0.345 ± 0.010	4.61 ± 0.03
20%	-0.7	-0.75	-0.86	-0.9	-1.03	-0.415 ± 0.010	4.54± 0.03
30%	-0.82	-0.87	-1.02	-1.06	-1.17	- 0.565 ± 0.011	4.39 ± 0.03

In Table 5-5, the flatband voltages and work function values for the HfSiN gate MOS capacitors, for increasing gas flow ratios (10% to 30%) are shown. The extracted value of HfSiN work function is observed to decrease from 4.61 ± 0.03 to 4.39 ± 0.03. This indicates that the HfSiN work function decreases for an increase in gas flow ratios during the deposition.

5.3 Current-Voltage Characteristics

The current-voltage (IV) measurements were performed to assess the quality of the gate oxide. These measurements were carried out in an enclosed probe station in dark to avoid the electrical and optical noise. The measured current may arise from either a particle current or a displacement current. A particle current is a current which arises when electrons or holes, travel from one electrode to another, where the transport is via tunneling through dielectric layer, external excitation over energy barrier or some through trap assisted mechanisms. The displacement current results from the displacement of charge to and from the electrodes but not actually passing through the dielectric i.e. the charging and discharging of the plates of the capacitor.

In Figure 5-5, the current density (J_g) of several HfSiN gate MOS capacitors are shown. In this plot, the current density (J_g) was taken from capacitors with areas 2.5×10^{-3}, 4×10^{-4} and 1×10^{-4} cm^2. These data within the experimental error overlap suggesting a relatively uniform gate

oxide film. In Figure 5-6, the current density is shown as the function of the applied bias.

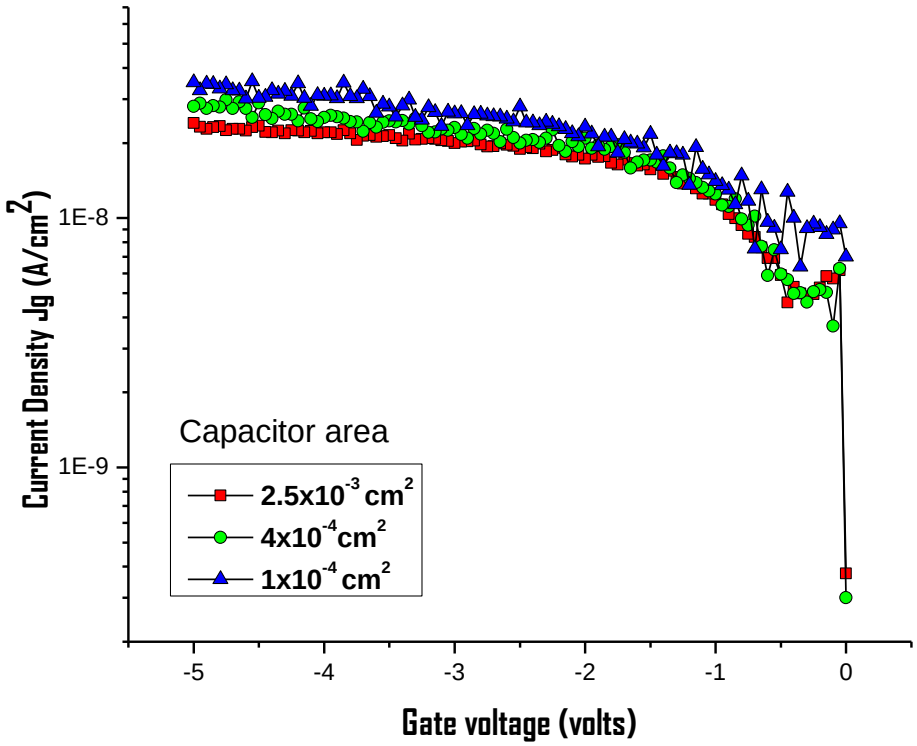

Figure 5-5: The current density response of HfSiN gate MOS capacitor with three different areas.

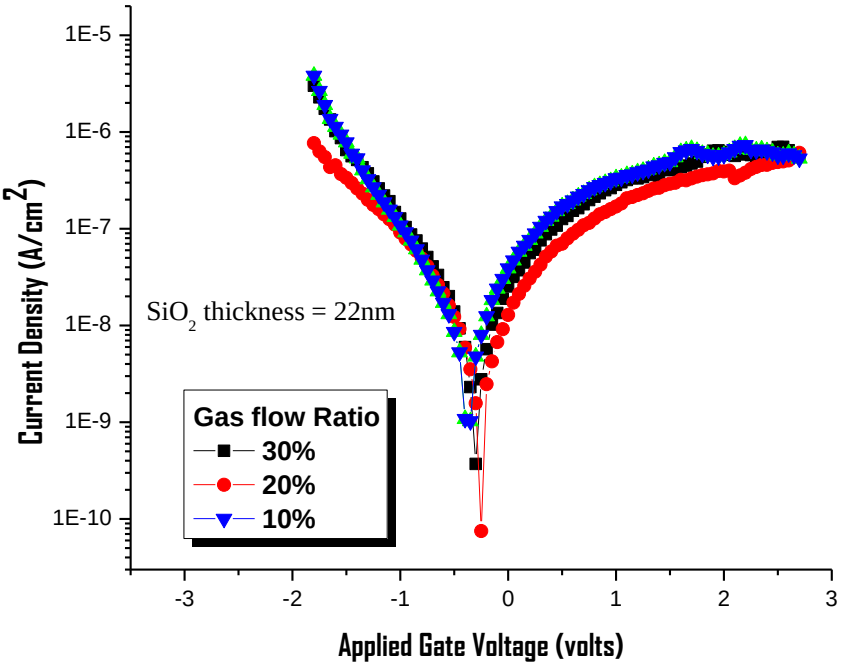

Figure 5-6: The current density is shown as a function of applied bias of HfSiN gated MOS capacitor for different gas flow ratios.

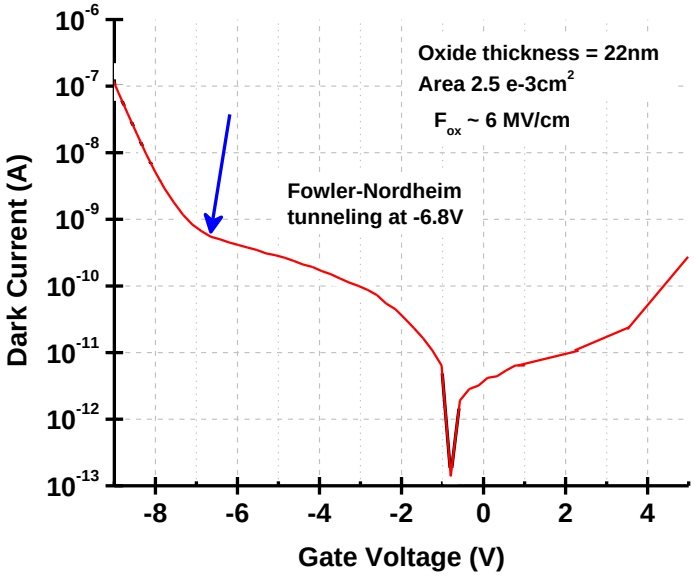

Figure 5-7: The leakage current due to FN tunneling for a HfSiN gate MOS capacitor with area 2.5×10^{-3} cm^2.

The leakage current in Figure 5-7, arises at high negative voltages is due to FN tunneling. With further increases in negative bias, the gate oxide may breakdown resulting in a very high leakage current.

5.4 Barrier height measurements

By definition, the barrier height in a MOS device is the energy difference between the metal Fermi level and the conduction band of insulator for the metal/insulator interface. For the semiconductor/insulator interface, the barrier height is the difference between the conduction bands of the semiconductor and insulator. As discussed in Chapter 2, internal photoemission (IPE) is a powerful technique, for measuring the barrier height (Φ_b) at the metal/oxide interface by optically exciting electrons over the energy barrier. The work function of the HfSiN metal gate is calculated using the extracted barrier height value. As an example, the barrier height

measurements for a 22nm SiO_2 MOS capacitor will be discussed in this chapter.. The experimental set up for the internal photoemission measurements was described in Chapter 4.

5.4.1 Optical measurements

In this work, a mercury (Hg) arc lamp (200W) was used as a light source. The spectrum of a mercury arc lamp has numerous high intensity light peaks at wavelengths corresponding to transitions between energy states in Hg gas. Therefore, the apparatus used for these measurements must be fully characterized for spectral response, bandwidth and transmission. A reference silicon photodiode (Newport 818-UV) was used for calibrating the measurement apparatus i.e. the mercury arc lamp and the monochrometer. A monochrometer was used to select a given wavelength. The spectrum of a mercury arc lamp, measured using photodiode is shown in Figure 5-8.

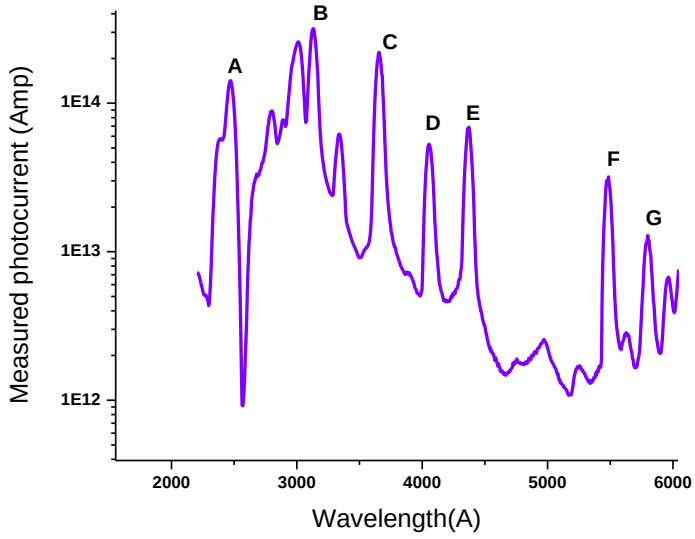

Figure 5-8: The mercury (Hg) arc lamp spectrum measured using a monochrometer as measured by a calibrated silicon photodiode.

The photon energy E_{ph} is given by the wavelength of the light used and is inversely related to the energy. It is given through the wavelength of the monochrometer. The wavelength

for each of the peaks and their peaks labelled from A to G with their associated wavelengths and corresponding photon energies (Eph) are listed in Table 5-6. The inverse relationship between the photon energy and the wavelength is given by:

$$E_{ph} = h\nu = \frac{hc}{\lambda},$$

where h is Planck's constant, ν is the optical frequency, and c is the speed of light.

Table 5-6: The wavelength and the photon energies of dominant peaks in the mercury arc lamp spectrum.

Peak	Known Wavelength (λ) (Å)	Photon Energy hν (eV) at Known Wavelength
A	2536.52	4.89
B	3129.00	3.96
C	3650.15	3.40
D	4046.57	3.06
E	4358.33	2.84
F	5460.74	2.27
G	5787.00	2.14

For this research, the input and output slits of the high resolution monochrometer were set to their maximum width (~2mm) for a maximized photocurrent increased transmission. Due to inverse relationship, when wavelength increases, the acceptable resolution also increases.

5.4.2 Responsitvity (R) and Incident Photon Flux (F_{ph})

The responsivity (R) values of a photodiode were provided by the manufacturer. The responsivity is defined as the ratio of the electrical output for a given optical input. To calculate the quantum yield(Y), the incident photon flux (F_{ph}) value is required.

The photon flux is defined as the number of incident photons per unit time. In practical terms, the incident photon flux (F_{ph}) is the ratio of total absorbed power (P_a) divided by the energy ($h\nu$) of each photon and is given by:

$$F_{ph} = \frac{P_a}{h\nu} = \frac{I_{diode}}{h\nu \times R},$$

where, Pa is the absorbed power of the incident photons.

The absorbed power (P_a) of the incident photons is the ratio of the photodiode responsivity (R) and the measured photodiode current (I_{diode}). The measured incident photon flux (i.e. the relative number of incident photons per second) and the responsivity (R) of the silicon photodiode are plotted in Figure 5-9.

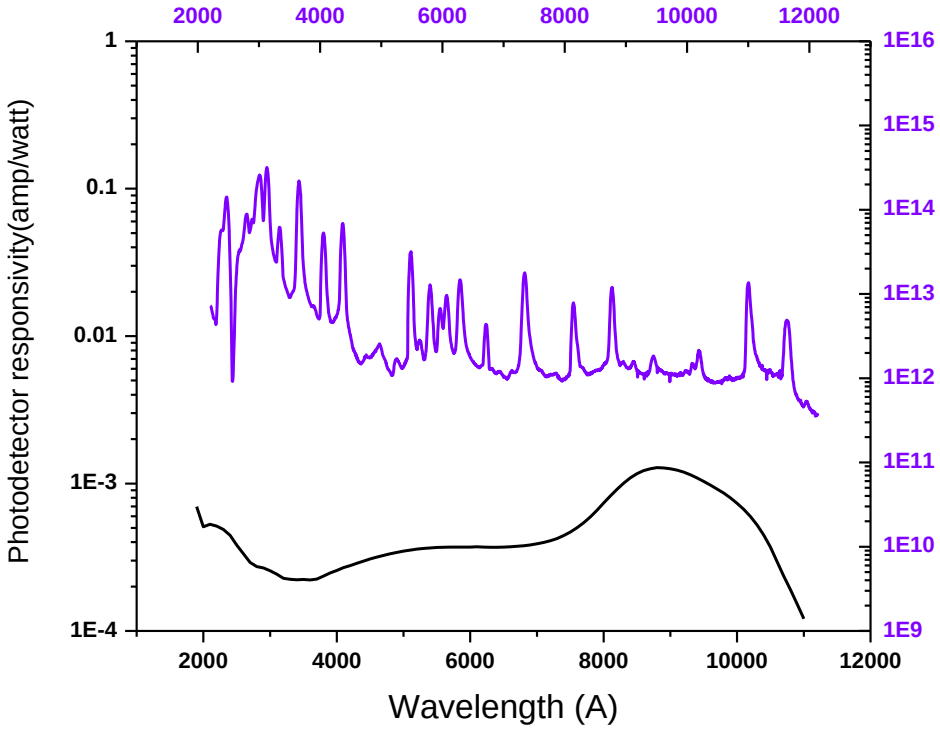

Figure 5-9: The responsivity (R) of the silicon photo-diode and the measured incident photon flux (F_{ph}) as a function of wavelength (λ) of incident light.

5.4.3 Gate Injection

For the barrier height between the gate and the oxide, photo-excited electrons are injected over the interfacial barrier. With a negative bias on the HfSiN gate electrode, electrons can be injected over the barrier. The photoinjection studies in this word, used photon energies ($h\nu$) ranging from 2 eV to 6 eV for illumination of metal gate electrode. When a bias was applied, the photons that were absorbed in the gate excite the electrons from the metal Fermi level over the barrier and into oxide conduction band. The measured photocurrent (I_{ph}) is due to the electrons which surmount the energy barrier with energies higher than the energy barrier (i.e. $h\nu > \Phi_b$).

In Figure 5-10, the photo-detector current is shown as a function of the photon energy ($h\nu$) for capacitors with area of 2.5×10^{-3} cm^2 and 4×10^{-4} cm^2. For the device shown, the applied

bias produced an oxide field of 2MV/cm. This capacitor had an HfSiN gate produced with a gas flow ratio R_N = 10 %. The leakage current as expected was found to scale with the device area. It was observed that the photocurrent intensity was significantly reduced for photon energies ($h\nu$ < 3.5 eV**)** because fewer electrons could surmount the interfacial energy barrier height at the applied electric field.

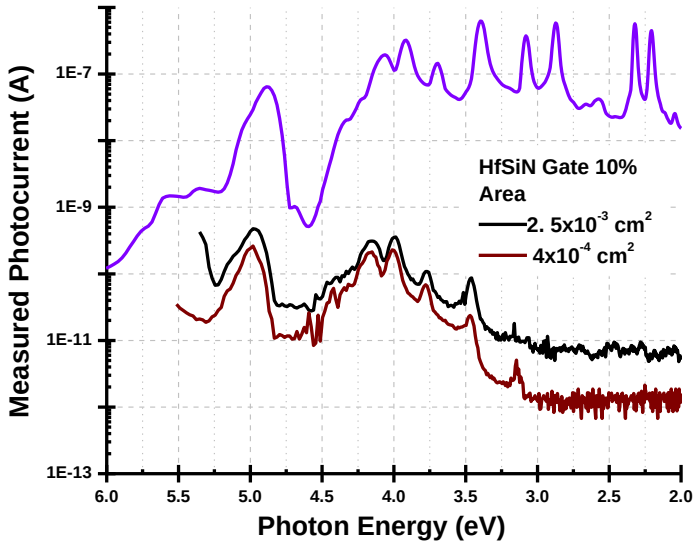

Figure 5-10: The photocurrent intensity as measured by the Si photo-detector is shown in the upper curve. The MOS capacitor current is also shown for two device areas for the gate with at 10% gas flow ratio.

5.4.4 Quantum Yield (Y)

The ratio of number of photo-excited electrons overcoming the energy barrier to the number of absorbed photons in the gate is known as the quantum yield(Y). In a MOS capacitor, the quantum yield was calculated from the photocurrent (I_{ph}) and the absorbed power of the incident photons (P_a). The relationship between the incident photon flux (F_{ph}) and the quantum yield is expressed as

$$Y = \frac{I_{ph}\, h\nu}{qP_a} = \frac{I_{ph}}{qF_{ph}}, \qquad (5.5)$$

where hν is photon energy (eV) and q is the electronic charge.

In Figure 5-11 below, the photocurrent is shown as a function of the photon energy for various oxide fields (F_{ox}). To avoid FN tunneling at high electric fields, the photocurrent was measured at electric fields (Fox) varying from 0.5 MV/cm to 4.5 MV/cm. As described earlier in chapter 2, with an increase in applied electric field across the oxide, the effective barrier height is lowered. To determine this effective barrier height, the number of photons and the measured photocurrent (I_m) were used to calculate the quantum yield. A lower barrier height allows lower energy electrons to overcome the barrier and results in higher photocurrent and hence, higher quantum yields (Y).

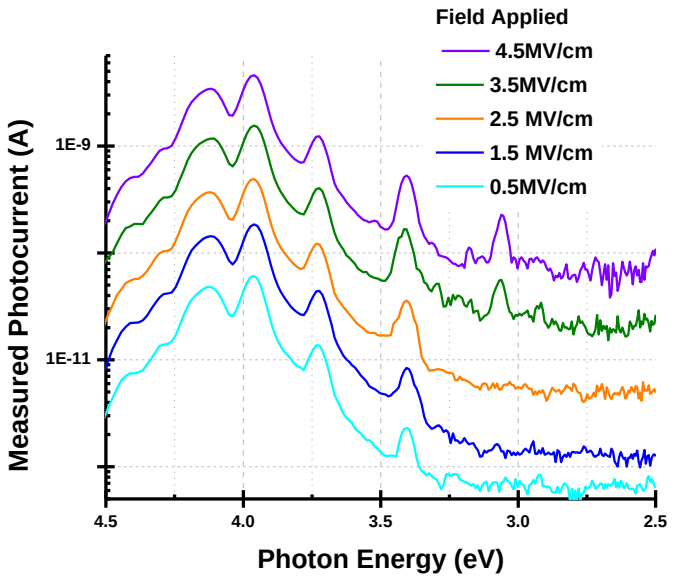

Figure 5-11: The measured photocurrent at different electric fields across the gate oxide.

For a 2.5x10^{-3} cm^2 MOS capacitor, a plot of square root of quantum yield ($Y^{1/2}$) as a function of the photon energy (hν) is shown in Figure 5-12. For this device, HfSiN metal gate was deposited with a 20% gas flow ratio. For barrier height measurements, the square root of relative yield is plotted as a function of the photon energy because the best model to use for an injecting

electrode that is a metal is a square root of a quantum yield [28]. The effective barrier height (Φ_{beff}) is related to quantum yield by equations through:

$$\sqrt[P]{\frac{I_m h\nu}{qP_a}} \propto h\nu - \Phi_{beff} \propto h\nu - \left(\Phi_b - K\sqrt{F}\right), \tag{5.6}$$

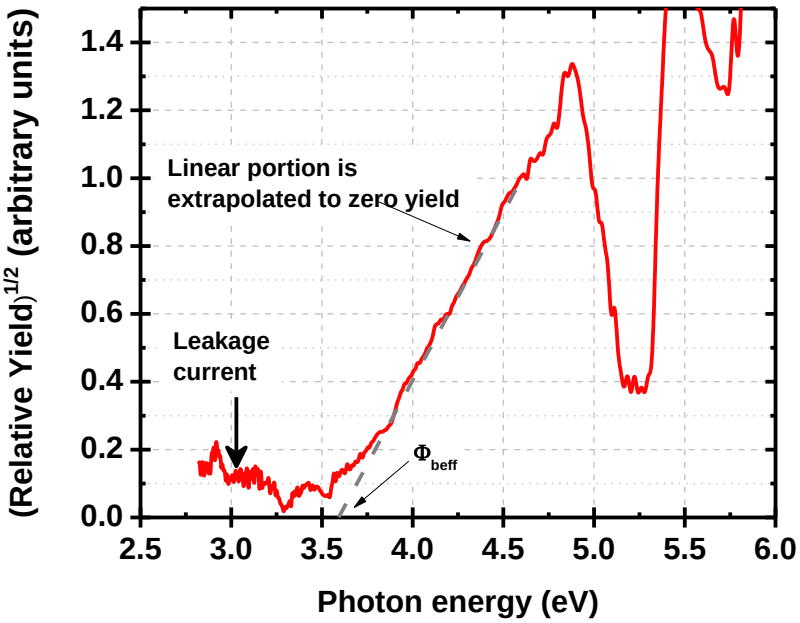

Figure 5-12: The typical plot of square root of quantum yield (Y) vs. photon energy (hν) for oxide field = 1.5 MV/cm. The HfSiN gate is deposited at 20% gas flow ratio and capacitor area =2.5x10^{-3} cm^2. The extrapolated effective barrier height (Φ_{beff}) = ~3.64 ± 0.02 eV.

In this research, a previously published procedure was used to analyse the internal photoemission data [31, 32]. For photon energies less than 3.2 eV, the photocurrent may be attributed to a tunneling current and this current is not useful for barrier height measurements. Therefore, a linear fit can only be made for the higher energy data. A linear fit to the data plot over a relatively large range of photon energies is also shown in Figure 5-12. The correlation coefficient for the fit was found to ~ (-1± 0.1). The extrapolation of these linear fits was used to extract the effective barrier height. The HfSiN/SiO_2 effective barrier height (Φ_{beff}) for this particular device extracted for a field of 1.5MV/cm was found to be ~ 3.64 ± 0.02 eV.

5.4.5 Barrier Height (Φ_b) Extraction

As previously discussed in Chapter 2, in presence of an external electric field, the effective barrier height is controlled by the applied field and the "Schottky effect". With an increase in electric field (F_{ox}), the effective barrier height was found to reduce due to Schottky effect or image force induced barrier lowering.

For HfSiN gates desposited with gas flow ratios (10% to 30%), the effective barrier height values can in turn be plotted as a Schottky plot (Φ_{beff}) versus $(F_{ox})^{1/2}$) and the F=0 intercept can be extrapolated to obtain the band offset as shown in Figure 5-13.

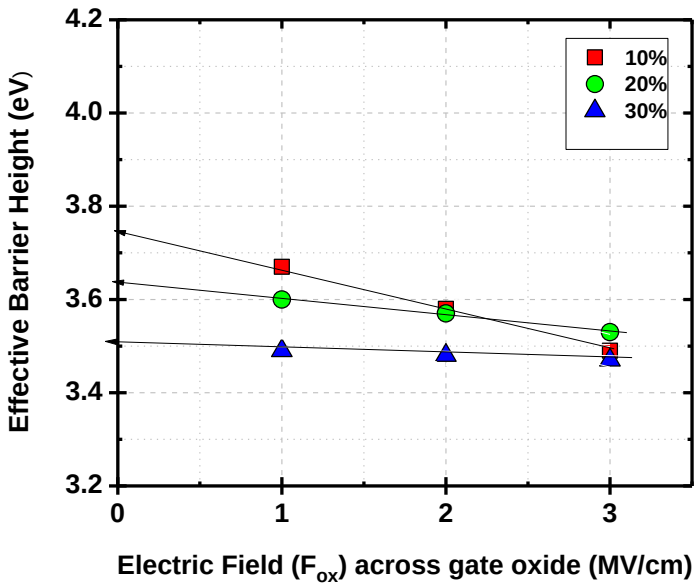

Figure 5-13: The effective barrier height (Φ_{beff}) is shown as a function of the oxide electric field (F_{ox}). The zero field barrier height (Φ_b) for the 10%, 20%, 30% gas flow ratios was found to be 3.74 ± 0.02 eV, 3.64±0.02 eV and 3.52±0.02 eV respectively..

5.5 HfSiN Work Function (Φ_m)

The HfSiN metal gate work function (Φ_m) was measured using the extracted barrier height (Φ_b) values. In Table 5-7, the effective barrier heights are tabulated along with the zero field barrier heights and the extracted work function for a given HfSiN/SiO_2 interface.

Table 5-7: The effective barrier heights (Φ_{beff}), zero field barrier height (Φ_b) and extracted work function (Φ_m) for the HfSiN gate deposited with varying gas flow ratios.

Gas Flow Ratio (%)	Effective barrier height (Φ_{beff}) (eV) Applied Electric Field F_{ox} (MV/cm)			Zero Field Barrier Height Φ_b (eV)	HfSiN Work Function (Φ_m) (eV)
	1	2	3		
10%	3.67	3.58	3.49	3.74 ± 0.02	4.64 ± 0.03
20%	3.6	3.57	3.53	3.64 ± 0.02	4.57 ± 0.03
30%	3.49	3.48	3.47	3.52 ± 0.02	4.42 ± 0.03

For gas flow ratios varying from 10% to 30%, the HfSiN work functions (Φ_m), were observed to decrease from ~ 4.64 ± 0.03 eV to ~ 4.42 ± 0.03 eV as shown in Table 5-7. On each test samples, the resultant values were an average of 4 different sized capacitors on each test sample.

5.6 Comparison: Extracted Work Function

These results show that the work function values obtained from internal photoemission measurements are in good agreement with the values obtained from the high frequency capacitance-voltage characterization technique as shown in Figure 5-13.

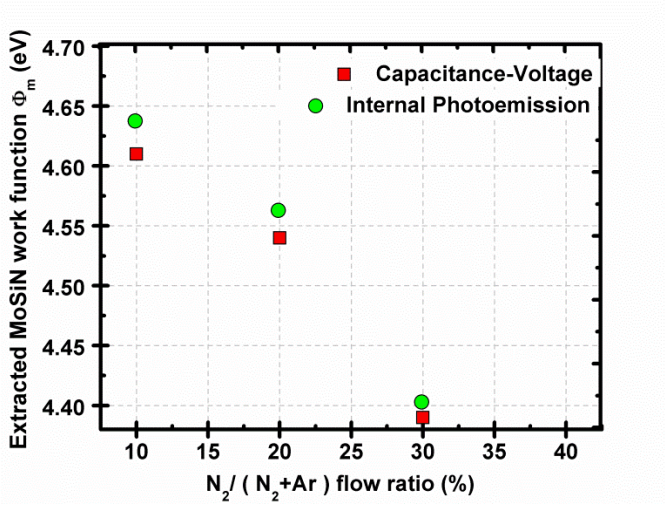

Figure 5-14: Extracted HfSiN work function using C-V and Photo IV measurements as a function of varying gas flow ratios.

Chapter 6 Material Characterization

6.1 Introduction

The material characterization techniques are typically used to investigate the physical and the chemical properties of a test sample. In this work, HfSiN gate MOS capacitors were analysed by X-ray Photoelectron Spectroscopy (XPS) technique. In order to obtain the important information regarding the elemental composition, the chemical bonding and the chemical structure, XPS depth profiling was performed.

The samples were prepared by co-sputtering Hf and Si targets in plasma consisting of sputtering gas mixture (N_2/ (N_2 + Ar)), varying from 10% to 30%. All samples were subjected to a forming gas (5% H_2in N_2) annealing at 400^{o}C for 30 minutes. As discussed in Chapter 2, any structural or chemical changes within the metal will affect its work function. Therefore, with different gas compositions, the HfSiN work function was expected to vary. This variation in the work function has been noted in Chapter 5, with an increase in gas flow ratios the barrier height measurements were found to be decreasing. Hence, to study the surface chemistry of HfSiN blanket films, an x-ray photoelectron spectroscopy (XPS) technique was employed.

6.2 X-ray Photoelectron Spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS), is an analysis technique that uses x-rays in an ultra-high vacuum environment to investigate the chemical compounds on the sample surface [43]. In this work, XPS was used to measure the elemental composition, the chemical states and the atomic concentration (%) of the elements present in the HfSiN gate metal films.

6.2.1 Basic Principle

An XPS analysis is obtained by a special form of photoemission, i.e. the ejection of an electron from a core level by an X-ray photon of energy hν. The electron spectrometer then

analyses the energy of the emitted photoelectrons by irradiating a sample surface with a beam of x-rays [43]. In Figure 6-1, the energy level diagram of the XPS process showing photoionization of an atom by the ejection of an electron is shown.

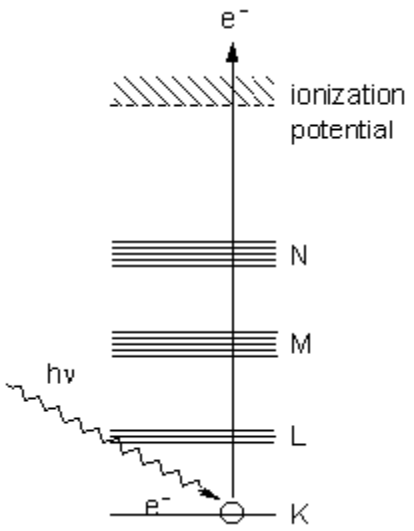

Figure 6-1: An energy-level diagram illustrating the basic principles of an x-ray photoelectron spectroscopy [43].

The kinetic energy (E_k) of these photo-emitted electrons is the experimental quantity measured by the spectrometer and is dependent on the photon energy of the x-rays. The kinetic energy is related to the energy of incident x-rays ($h\nu$) and the electron binding energy (E_b) by:

$$E_k = h\nu - E_b - \Phi, \qquad (6.1)$$

where E_k is the kinetic energy, $h\nu$ is the photon energy, E_b is the binding energy and Φ is the work function of the spectrometer. The binding energy (E_b) of the core electron is the minimum energy required to remove an electron from its atomic orbital to vacuum level [43, 44].

6.2.2 XPS Instrumentation

For the XPS system, a computer was responsible for collecting the data and analysis tools such as CASA, was used to perform the chemical characterization of the co-sputtered HfSiN

films. For XPS analysis, the HfSiN/SiO_2/Si test wafers were sized (~1×1 cm^2) to fit into the sample holder, provided with the XPS equipment. An x-ray beam was used to scan a small area (~2×2 mm^2) in the centre of each test sample. The samples were placed in an ultra-high (~ 1×10^{-10} Torr) vacuum chamber.

The XPS instrument, shown in Figure 6-2 includes Hemispherical analyser (HAS), an x-ray gun , transfer lenses and delay-line electron detector head [45].

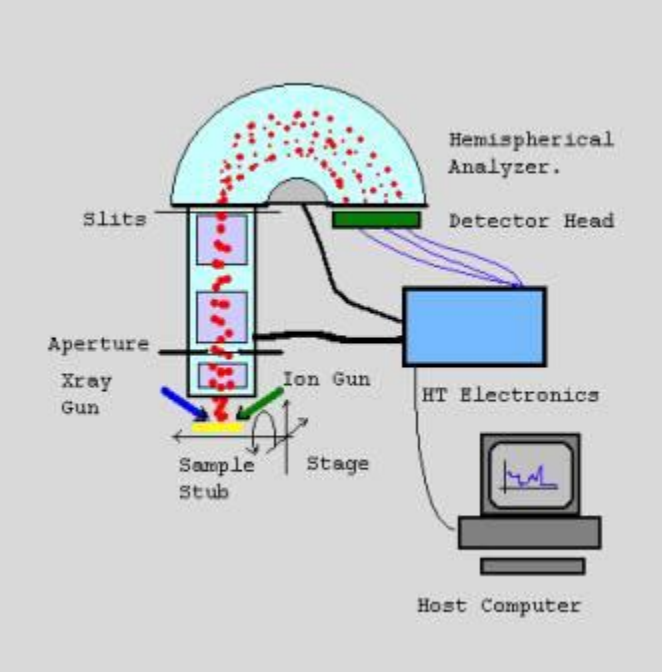

Figure 6-2: A schematic diagram of the XPS instrument [45].

The HfSiN film was irradiated with x-rays resulting in photoemission of core-level electrons from the sample. The HSA measured the kinetic energy (E_k) of the photoelectrons emitting from the sample. As the data that is collected is a measurement of kinetic energy of electrons. The kinetic energy of electrons depends on the energy of the incident rays. Since, not all the systems will have the same incident x-ray energy; hence, it will not be convenient to compare kinetic energies. However, each element has a characteristic binding energy (E_b). Almost all elements (excluding hydrogen and helium) can be verified by measuring the

corresponding binding energy of the photoelectrons emitted from an element. To determine the binding energies, we first need to collect the kinetic energies of the electrons. Once the spectrometer collects the data, the binding energies of the electrons can be calculated if the wavelength of the incident x-rays is known. The binding energy of the core electron changes with a change in chemical bonding structure of an atom. This change in binding energy corresponds to a chemical shift in the XPS peak. Hence, by measuring the shifts in the binding energy, the chemical and elemental compositions can be determined. The binding energy was obtained from the kinetic measured kinetic energy (E_k) using the relationship described in equation 6.1. The number of emitted photoelectrons i.e. the intensity (counts per sec) was determined by a delay-line-detector. The XPS measurement was used to investigate the composition of top ~7 nm of the film where the photoelectrons generated near the surface were available for detection [43, 44].

6.2.3 XPS Spectrum for Element Identification

To indentify the elements present on the HfSiN surface, a quick survey scan was performed. In Figure 6-3, the intensity (counts per sec) vs. the binding energy (eV) spectrum for the HfSiN blanket film, deposited at 10% gas flow ratio, is plotted. For a wide range of binding energies (0 to 800 eV), the top surface of the HfSiN blanket films was analyzed. All data is collaborated to the carbon (C 1s) peak (at binding energy = 285 eV).

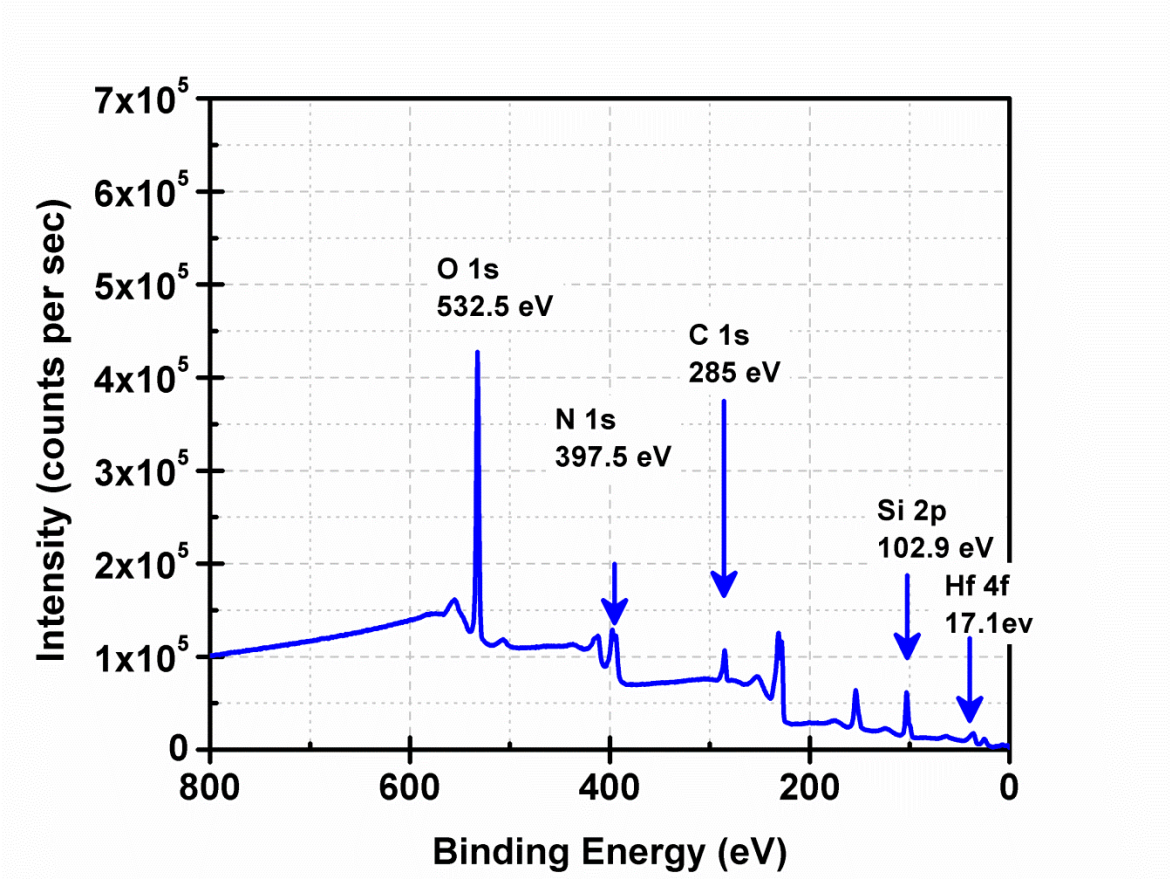

Figure 6-3: The raw XPS spectrum obtained by analysing the surface of blanket HfSiN films (co-sputtered at 10% gas flow ratio). The plot was calibrated by fixing the plot to the reference C 1s (285 eV) peak.

In Figure 6-3, the expected XPS peaks for carbon (C 1s), oxygen (O 1s), silicon (Si 2p), nitrogen (N 1s) and hafnium (Hf 4f) are shown. To identify the presence of these elements on the surface of the HfSiN test sample and to locate the peaks i.e. binding energy, compared with the values reported in reference books [46, 47] and NIST (National Institute of Standards and Technology) XPS reference database [48] were used.

6.2.4 XPS Spectrum of Individual Peaks

To verify key features of individual peaks, a high energy resolution scan was performed. The chemical bonding and the elemental composition of HfSiN films were observed from the height and shapes of the XPS peaks.

6.2.4.1 Oxygen (O 1s) peak

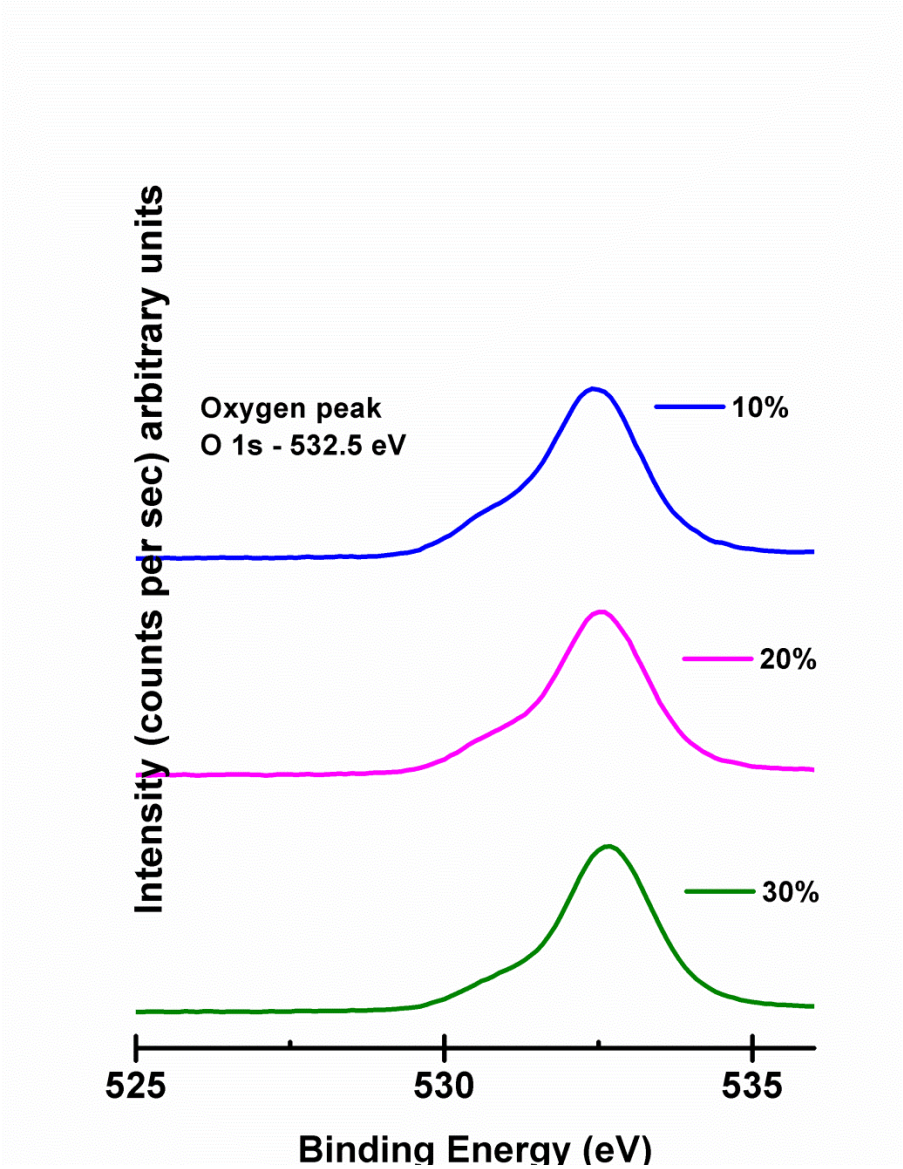

Figure 6-4: Individual XPS peaks for and Oxygen (O 1s) as a function of binding energy.

In Figure 6-4 and Figure 6-5, the high resolution spectra for oxygen (O 1s – 532.5 eV) and carbon (C 1s – 285 eV), shows no change for the reactive sputtering conditions (gas flow ratio - 10%, 20%, and 30%). These peaks were not seen after cleaning the HfSiN surface with an argon ion gun for 5 minutes, indicating possible contamination in the top few mono-layers due to exposure to air.

6.2.4.2 Carbon (C 1s) peak

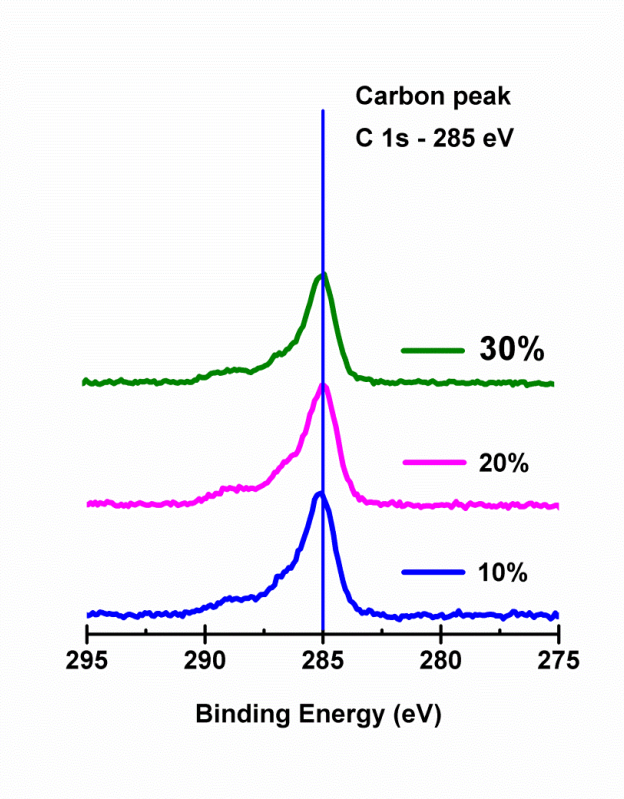

Figure 6-5: Individual XPS peaks for and Carbon (C 1s) as a function of binding energy.

6.2.4.3 Hafnium (Hf 4f) Peak

In Figure 6-6, the XPS spectra for hafnium (Hf 4f doublet) are shown, for all HfSiN films prepared in this study. The binding energy for Hf $4f^{7/2}$ (17.1 eV) and Hf $4f^{5/2}$ (21.3 eV) are in good agreement with the values reported in [47] where Hf $4f^{7/2}$ corresponded to Hf-Si bonds in $HfSi_2$ films and Hf $4f^{5/2}$ corresponded to Hf-N bonds for HfN_x films.

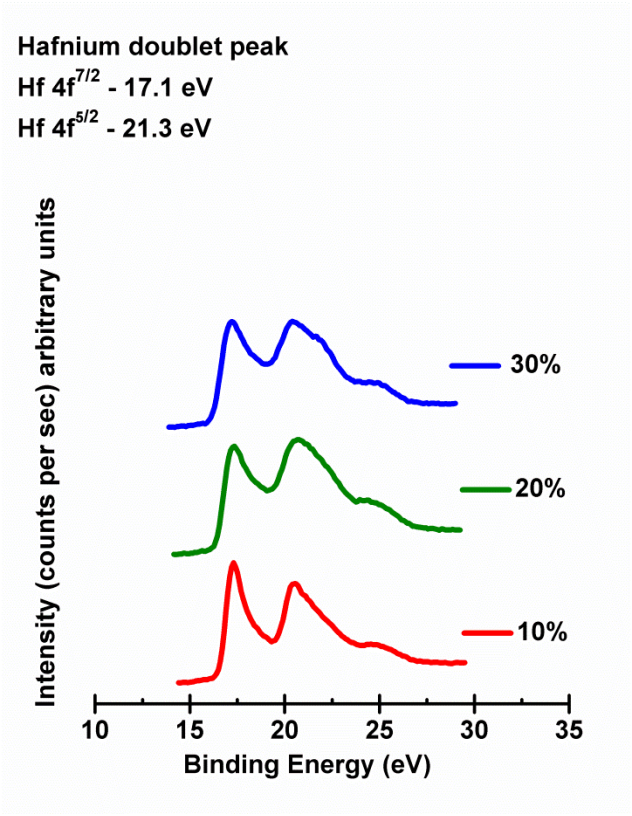

Figure 6-6: The XPS photoelectron peak for Hafnium (Hf 4f doublet) as a function of binding energy.

In Figure 6-6, the intensity of Hf $4f^{7/2}$ peak gradually decreases, i.e. reduction in Hf-Si bonds is observed as the nitrogen (N_2) partial pressure in the sputtering gas mixture ($N_2/(N_2$ + Ar)) is increased. A concurrent increase in the Hf-N bonds is confirmed by the asymmetric broadening of the Hf $4f^{5/2}$ peak for the gate deposition conditions mentioned above.

6.4.2.4 Silicon (Si 2p) Peak

In Figure 6-7, the XPS spectra obtained from the HfSiN films for the silicon (Si 2p) peaks is shown. For HfSiN films deposited at 10% gas flow ratio, peak 'A' corresponds to the binding energy of Si–N bond in Si_3N_4 [47] and peak 'B' corresponds to Si–Hf bond in Hafnium silicide ($HfSi_2$) [47].

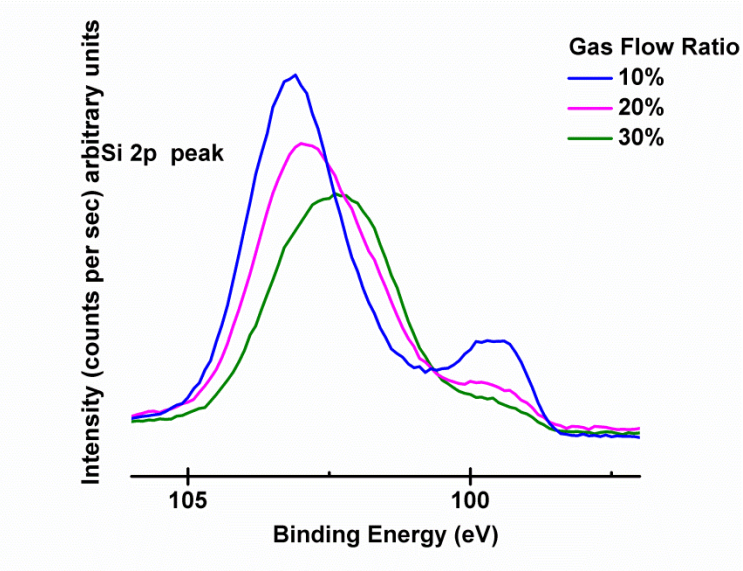

Figure 6-7: The XPS spectra for silicon (Si 2p) as a function of binding energy.

In Figure 6-7, the two Si 2p peaks (for 10% gas flow ratio) indicate that the silicon atoms are bonded to both hafnium and nitrogen atoms. With an increase in gas flow ratio (from 10% to 30%), the intensity of both peaks 'A' and 'B' is observed to decrease consistently. Further, this suggests a reduction in the formation of Si-Hf and Si-N bonds. The peak 'B', corresponding to Si-Hf bonds, is almost non-existent for HfSiN films deposited at 30% gas flow ratio, indicating that very few silicon atoms remain bonded to hafnium atoms. These results indicate that majority of the silicon atoms, in the HfSiN films deposited at 30% gas flow ratio, are either bonded to silicon or nitrogen with very few Si-Hf bonds.

6.4.2.5 Nitrogen (N 1s) Peak

In Figure 6-8 the XPS spectra for nitrogen (N 1s – 397.5 eV) are shown.

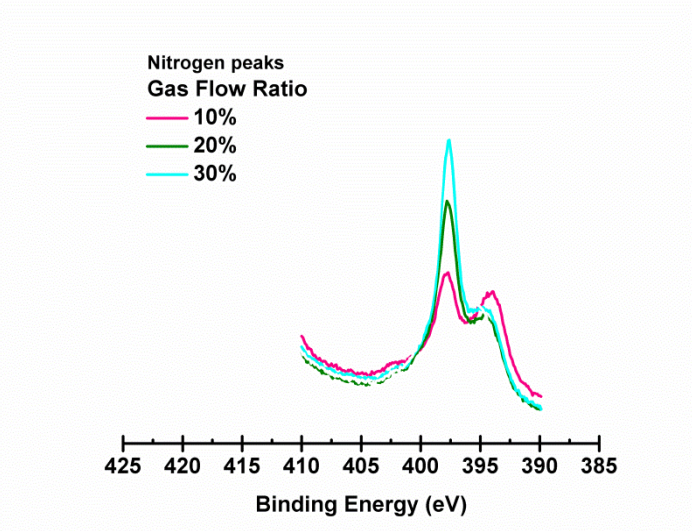

Figure 6-8: The XPS spectra for Nitrogen (N 1s) as a function of binding energy

In Figure 6-8, the binding energy for the nitrogen (N 1s) is shown. The N 1s peak intensity is observed to consistently increase with the gas flow ratio. The peak height or area under the peak is a direct measure of the amount of nitrogen absorbed in the HfSiN films. Therefore, it leads to a conclusion that increasing the nitrogen partial pressure in the sputtering gas mixture incorporated larger amounts of nitrogen in the reactively sputtered HfSiN films.

As indicated from above elemental peaks, it is clear that a larger percentage of nitrogen atoms, absorbed in the HfSiN films, have a tendency to bond with hafnium rather than to silicon atoms. In any case, the intensity variations in N 1s peak confirmed a steady increase in the total nitrogen concentration in the reactively sputtered HfSiN films.

6.3 Atomic Concentration from XPS Spectrum

The peak height or area under a raw XPS peak was used to calculate the relative amount of each element present within the analysis area on the HfSiN samples. For overlapping peaks, curve fitting and peak separation software was used to separate and estimate the contribution from each peak.

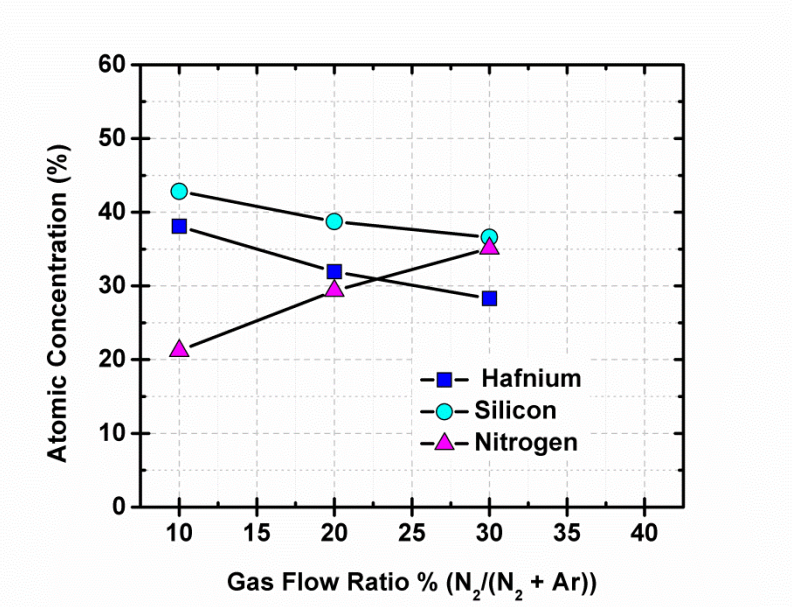

Figure 6-9: A plot of atomic concentration (%) vs. gas flow ratio (%) obtained from the Hafnium (Hf 4f), Silicon (Si 2p) and Nitrogen (N 1s) XPS spectras.

In Figure 6-9 the atomic concentration (%) of hafnium, silicon and nitrogen as a function of the gas flow ratio (N_2/ (N_2 + Ar)) is shown. The area under the individual peak was to estimate the atomic concentration (%) for each element detected during the XPS surface analysis of the HfSiN sample. This plot indicates that the atomic concentration of nitrogen increases (from ~21% to ~35%) with the gas flow ratio (varying from 10% to 30%). It may be speculated that the HfSiN films may begin to saturate and not absorb any more nitrogen, if higher (over 30%) gas flow ratios are used.

The plot indicated that the nitrogen content incorporated in HfSiN films increased linearly as the gas flow ratios were increases from 10%to 30%. As discussed in Chapter 5, steady decrease in the HfSiN work function (Φ_m) was observed with an increase in N_2 gas flow ratio during the gate deposition. It can be concluded that the high nitrogen concentration are likely responsible for the change in the properties of the metal gate and effectively, lowered the HfSiN

work function. Hence, it can be stated that by adjusting the nitrogen concentration in HfSiN films, the work function of HfSiN metal gate can be tuned over a wide range.

Chapter 7 Conclusion

7.1 Summary

The objective of this research was to produce and investigate the tuned metal gate electrodes integrated with SiO_2 as a gate dielectric. In this work, the HfSiN metal films were used as the metal gate electrode in a simple MOS capacitor structure. The metal-oxide-semiconductor (MOS) capacitors were fabricated using thermal SiO_2 as gate oxide on lightly doped p-type Si wafer. The HfSiN films were co-sputtered using Hf and Si targets at 10mTorr in presence of N_2 and Ar. The gas flow ratio $R_N = N_2/ (N_2+Ar)$ was adjusted from 10%- 30% to alter the nitrogen concentration in HfSiN films. A lift-off process was used to define these blanket HfSiN metal films. All the test wafers underwent a post-metallization anneal in forming gas (5% H_2 in N_2) at 400^oC for 30 minutes to reduce the fixed oxide charge and the interface trapped charge. Additionally, reference aluminum gate MOS capacitors were used to compare the extracted values of the metal work function (Φ_m).

High frequency capacitance voltage (HFCV) measurements were used to extract the gate work function using the V_{FB}-tox method. Interfacial barrier heights were measured using internal photoemission (IPE) as an independent confirmation of the HfSiN gate work function. The extracted work function of HfSiN gate electrode was found to decrease linearly from ~ 4.64 $\pm$ 0.03 eV to ~ 4.42 $\pm$ 0.03 eV for increasing gas flow ratios (10% to 30%).

X-ray Photoelectron Spectroscopy (XPS) technique was employed in this study to characterize the surface composition and chemical bonding in ultra-high vacuum (UHV). XPS surface analysis showed a steady increase in the total nitrogen concentration (from ~21% to 35%) in these films as gas flow ratio was increased. These results confirmed that the increase in

nitrogen concentration in HfSiN films corresponds directly with the lowering of HfSiN work function as shown in Figure 7-1. These data clearly shows that the work function of $Hf_xSi_yN_z$ can be varied ~0.2 eV by adjusting the nitrogen concentration.

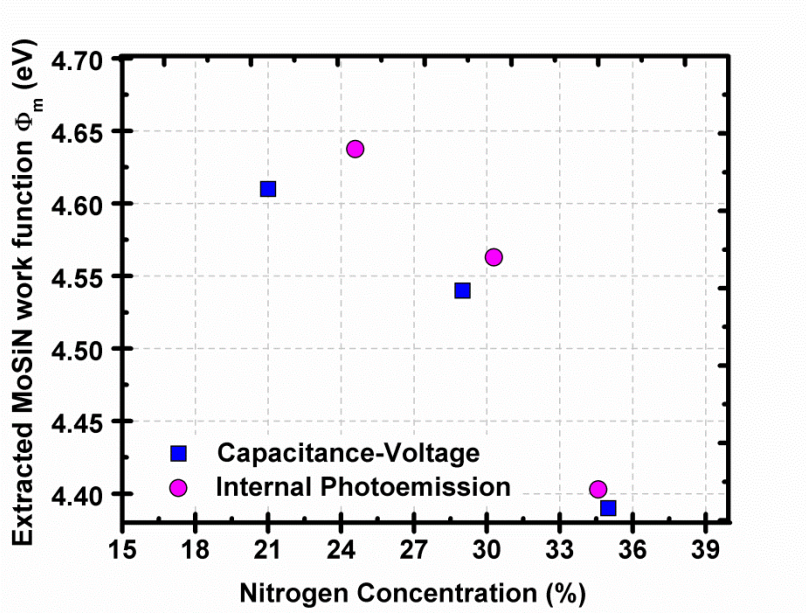

Figure 7-1: Extracted HfSiN work function using C-V and Photo IV measurements as a function of varying Nitrogen concentration.

From this research work, it is observed that reactively co-sputtered $Hf_xSi_yN_z$ (HfSiN) films validate as a promising material for gate work function engineering.

7.2 Suggestions for Future Work

The work function engineering of HfSiN metal films still requires a substantial amount of research. One of the areas that need extensive researches is the gate sheet resistance (Rs). In this work, the sheet resistance values of HfSiN films were higher than the values suggested by the ITRS and these may be reduced by an additional high temperature annealing step during fabrication.

Another interesting extension of this present research work would be the replacement of SiO2 gate dielectric with high dielectric constant (high-k) gate dielectrics.

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