Non-Invasive Internal Pattern Extraction of Integrated Circuits using Electrostatic Force Microscopy

by

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A Thesis
Submitted to the Faculty of Graduate Studies
in Partial Fulfilment of the Requirements
for the Degree of

Master of Science

Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Manitoba
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Tam Le Lam

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree

of

Master of Science

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ABSTRACT

Improvements in technology of the microelectronic areas have allowed researchers to develop Integrated Circuits (ICs) with higher speed and smaller size. However these improvements have also increased the difficulties for diagnostic testing of the circuits in the radio frequency (RF) range. The ideal measurement technique must be non-invasive with high spatial resolution, high temporal resolution, high sensitivity. It must be easy to use and cost effective. The current techniques do not meet the above combined criteria.

This thesis introduces a simple non-contact technique, based on the Electrostatic Force Microscope (EFM), for internal testing of microelectronic circuits. A heterodyne technique which utilizes short electrical pulses for sampling is implemented to extract an abitrary periodic digital pattern. This thesis also evaluates three narrow pulse generation techniques. An Integrated Circuit version of the Non-Linear Transmission Line (NLTL) was designed, fabricated and tested.

Using the heterodyne technique, measurements of 0.5 Gb/s and 1 Gb/s are performed on 50Ω transmission line as well as on internal nodes of BiCMOS and CMOS integrated circuits. Results show that the proposed technique is a capable tool for diagnostic tesing of high frequency microelectronic circuits while satifying the above requirements.

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OUTLINE

Abstract i

Acknowledgement ii

List of Figures vii

List of Tables xv

CHAPTER1

1. INTRODUCTION 1

1.1 Motivation 1

1.2 Thesis Outline 2

CHAPTER2

2. INTERNAL TESTING TECHNIQUE 3

2.1 On Wafer Contact Probing 3

2.2 Near Field Probing 6

2.3 Electron Beam and Photoemission Probing 9

2.4 Electro-Optic Sampling 11

2.5 Optoelectronic Sampling 14

CHAPTER3

3. ELECTROSTATIC FORCE MICROSCOPY 16

3.1 Scanned Probe Microscopes 16

3.2 Brief Overview of EFM 20

3.3 Experimental Set-Up of EFM 23

3.3.1 Micro-machined Probe Characterization 24

3.3.1.1 Spring Constant....25
3.3.1.2 Natural Resonat Frequency....26
3.3.1.3 Frequency Response....27
3.3.2 Deflection Sensors....28
3.3.2.1 Deflection Calculation using a Simple Model for the Tip....29
3.3.3 Beam Bounce Detection Technique....31
3.4 EFM Characterization....35
3.4.1 Spatial Resolution....35
3.4.2 Invasiveness....38
3.4.3 Voltage Sensitivity....39
3.5 Existing Voltage Measurement Schemes Using EFM....42
3.5.1 DC Measurement Technique....42
3.5.2 High Frequency Vector Waveform Measurement Technique....46
3.5.2.1 Sinusoidal Modulation....46
3.5.2.2 Square Wave Modulation....50

CHAPTER4

4. NARROW PULSE GENERATION TECHNIQUES....52
4.1 Non-Linear Transmission Line (NLTL)....52
4.1.1 Theory....52
4.1.1.1 Ideal Transmission Line....52
4.1.1.2 Diode Junction Capacitance....55
4.1.1.3 Non-linear Transmission Line....57
4.1.1.4 Fall Time Limiting Factor....61
4.1.2 Design Parameters....64
4.1.2.1 Co-Planar Waveguide Transmission Line Design....64
4.1.3 Evaluation and Construction of the Desing NLTL....66

4.1.3.1 Simulation and Calculation 67
4.1.3.2 Construction 71
4.1.4 Experimental 73
4.1.4.1 DC Measurement Experimental Set-up and Results 73
4.1.4.2 HF Measurement Experimental Set-up 74
4.1.4.3 HF Measurement Results 76
4.2 AND-Gate 77
4.2.1 Overview 78
4.2.2 Results 79
4.3 Impulse Generator (Comb Generator) 80
4.3.1 Introduction 80
4.3.2 Impluse Generation 81
4.3.3 Experiemental Set-Up and Results 83

CHAPTER5

5. PATTERN EXTRACTION TECHNIQUE 86
5.1 Overview of the Technique 86
5.2 Sensitivity of the Pattern Extraction Technique 92
5.3 Experimental Set-Up 93
5.3.1 Characterization of the Sampling Pulse 95
5.4 Experimental Results 97
5.4.1 Technique's Characterization using Microstrip Line 97
5.4.1.1 Rise and Fall Time Measurement and Pattern Extraction 97
5.4.1.2 Propagation Dealy Measurement Capability 101
5.4.1.3 Repetibility of the Technique 103
5.4.2 Measurements of the BiCMOS Integrated Circuit 104
5.4.3 Measurements of the CMOS Integrated Circuit 108

CHATER6

6. CONCLUSION 114

Appendix 116

References 124

List of Figures

Figure 2.1: Schematic diagram of the on-wafer probing technique............................4

Figure 2.2: 3 different types of microwave wafer probes (a) coaxial (b) microstrip (c) coplanar waveguide. 5

Figure 2.3: capacitive coupling between the circuit and the centre conductor of the coaxial probe..6

Figure 2.4: Inductive coupling [34] (a) microstrip (b) coplanar waveguide...............7

Figure 2.5: Double loop probe[34]. 7

Figure 2.6: (a) Diagram of the coplanar configuration of the combined SFM/coaxial tip (b)close-up view of the tip and electric field lines between two conductors[54] 8

Figure 2.7: Block diagram illustrating the e-beam operating principle [60] 9

Figure 2.8: Three possible probing geometries for electro-optic sampling (a)front side probing for coplanar geometry (b) front side probing for microstrip lines (c) external probing for coplanar waveguide device......12

Figure 2.9: Diagram for the operating principle of electrooptic sampling technique[49] 13

Figure 2.10: A drawing of the photoconductive probe. A typical probe consists of a titanium contact tip with 8μm in diameter and 3μm height, and a photoconductive switch with 2μm width and spacing. The tip and switch are usually deposited on a MBE-grown Low Temperature GaAs layer.[19] 15

Figure 3.1: Schematic view of the AFM operating principle 18

Figure 3.2: Schematic view of the Ballistic Electron Emission Microscopy (BEEM) 19

Figure 3.3: EFM illustration using the micro-machined probe and beam bounce sensor system 21

Figure 3.4: physical set-up of the EFM using the Beam Bounce System 23

Figure 3.5: (a) EFM cantilever with its principal parameters (b) SEM micrographs of Si3N4 cantilever (top) and pyramidal tip (bottom). [58] 24

Figure 3.6: moment of inertia for a rectangular cross section 26

Figure 3.7: Experimental and theoretical frequency response curve of a typical Si_3N_4 cantilever which has a resonant frequency of 12.275 kHz with Q of 32 [32]. 28

Figure 3.8: A spherical model is used to represent the tip and the circuit under test is modelled by a ground plane 29

Figure 3.9: Diagram of the beam bounce detection technique 31

Figure 3.10: Deflection of the optical beam 32

Figure 3.11a: Tip-circuit separation at different heights 37

Figure 3.11b: The simulated force density (force per effective area) at different tip-circuit separation, h(100nm, 200nm, 500nm) versus x-direction in nm.[27] 37

Figure 3.12: Block diagram of the null-force technique. The probe's tip is place as close to the circuit as possible. The deflection of the probe is detected using the beam bounce measurement system. The deflection is recorded by the lock-in amplifier which is reference to the probe signal frequency ω_p. The probe signal v_p is the summation between the ac component at $\omega_p \approx \omega_r$ and the integration of the output of the lock-in amplifier. 44

Figure 3.13: Block diagram of the heterodyne measurement technique. The technique is implemented to measure high frequency signal. A high frequency signal source is used to generate the circuit and probe signal. The phase shifter is used to adjust the phase applied at the probe. A sinusoidal signal is used as a modulation signal at the probe resonant frequency. 47

Figure 3.14: Relative cantilever deflection as a function of the probe-circuit phase difference for the case of $A = V_c$, $A > V_c$, and $A < V_c$. 49

Figure 4.1: Lumped Elements Modelled of the Transmission Line 53

Figure 4.2: Lumped element modelled of the transmission line connected to a source and terminated with a load 54

Figure 4.3: Diode physical structure and symbol [23]....55

Figure 4.4: Junction diode in reverse bias mode [23]....56

Figure 4.5: structure of a single NLTL section....58

Figure 4.6: Lumped Elements Representation of a single NLTL section....58

Figure 4.7: 1 GHz Sinusoidal Input Waveform....59

Figure 4.8: Output waveform of NLTL....60

Figure 4.9: Derivative of the Output Waveform....61

Figure 4.10: Sawtooth Waveform....62

Figure 4.11: Derivative of the sawtooth waveform....62

Figure 4.12: waveform at the output of the low pass filter....63

Figure 4.13: Derivative of the waveform at the output of the low pass filter....63

Figure 4.14: Top View of the Co-Planar Waveguide Transmission line structure....64

Figure 4.15: Zo of CPW vs. k....65

Figure 4.16: circuit used to simulate the cut-off frequency of the line....68

Figure 4.17: Frequency response of a single line section....68

Figure 4.18:comparison between the simulated and calculated compression time....69

Figure 4.19: Simulation results of the falltime and compression of 40 nltl sections with d=5.65mm for input signals ranging between 720MHz to 1.4GHz.......70

Figure 4.20a: Photograph of the nltl chip.......71

Figure 4.20b: Close-up view of the nltl chip.......72

Figure 4.20c: Close up view at the input terminal of the nltl circuit.......72

Figure 4.21: DC measurement set-up.......73

Figure 4.22: Current-Voltage characteristic of the NLTL for a dc input voltages.......73

Figure 4.23: HF measurement set-up.......74

Figure 4.24: 1 GHz sinusoidal input signal generate by HP Sweep Oscillator.......75

Figure 4.25: 1GHz sinusoidal input signal measure at the first input bond pad of NLTL and the output waveform using a contact probe.......75

Figure 4.26: Output waveform of the NLTL for a 1GHz sinusoidal input. 0-100% falltime is ~286ps. 10-90% falltime is 185ps, and 20-80% falltime is 130ps.......76

Figure 4.27: Derivative of the Compressed Waveform. The FWHM is 280 ps.......77

Figure 4.28: Function diagram for the two input AND gate Chip [29].......78

Figure 4.29: Input Signals to an AND Gate.......79

Figure 4.30: Output Signal of the 2 Input AND Gate 79

Figure 4.31: Schematic view of an ideal model of the Step Recovery Diode 80

Figure 4.32: Illustration of the fast step generation process of the SRD 81

Figure 4.33: A typical impulse generator circuit [50] 82

Figure 4.34: Typical output of an impulse generator [50] 82

Figure 4.35: Experimental set-up for testing the impulse generator. 83

Figure 4.36: Characteristic of the high pass filter. the -3dB cut-off frequency is 300MHz. 84

Figure 4.37: Experimental output of the impulse generator. The FWHM is 120 ps. 85

Figure 5.1: Block diagram of the pattern extraction technique using the heterodyne electrostatic force microscopy. 87

Figure 5.2: (a) an arbitrary waveform $v_c(x,y,t)$ (b) sampling signal $v_s(t)$ 88

Figure 5.3: (a) illustration of the sampling signal modulated by a periodic square signal with frequency f_r (b) zoom-in view of the sampling pulse train 89

Figure 5.4: Experimental-set up of the pattern extraction technique. 93

Figure 5.5: Sampling pulse at the probe tip as captured on the oscilloscope with the help of a 10:1 coaxial coupler. The pulse has a repetition rate of 250MHz and FWHM of 130ps. 95

Figure 5.6: 500MHz applied signal, sampling pulse with large ripples and the convolution output. 96

Figure 5.7: 500MHz applied signal, sampling pulse with small ripples and the convolution output. Also shown is the plus and minus 3% errror bars representing the errors of the applied signal. 96

Figure 5.8: Schematic diagram of the 50Ω microstrip line. 97

Figure 5.9: A 500 MHz digital test pattern (1010) with the EFM measured data (with 10 pts smoothing). 98

Figure 5.10: EFM measured data (with 10 pts smoothing) and convoluted signal between the sampling pulse and the signal applied to the DUT. 98

Figure 5.11: A closed up view of the applied test pattern, measured data from the EFM and the signal resulting from convolving the sampling pulse with the applied signal. 99

Figure 5.12: Applied signal and the deconvolved signal. 100

Figure 5.13: Applied signal, EFM data and convoluted signal of a 10101010 digital pattern at 1Gb/s. 100

Figure 5.14: Applied signal, EFM data and convoluted signal of a 00010001 digital pattern at 1Gb/s 101

Figure 5.15: (a), (c) Applied and EFM data of the rising edges with 0, 20, 50 and 100 ps delay, respectively. (b), (d) close up view of (a) and (c). 102

Figure 5.16: EFM data of the falling edge being sampled 10 times. 103

Figure 5.17: Photograph of the BiCMOS inverter 104

Figure 5.18: Schematic view of the BiCMOS inverter 104

Figure 5.19: Measurement of 8 bits, 0.5 Gb/s digital pattern (1010) at pad 1. The simulation (a), EFM data (b), and contact probe [32] (c) results are shown. 105

Figure 5.20: Propagation delay measurements from the sinulation (a), EFM data (b) at pad 1, 3, 5 along with the contact probe (c) [32] at pad 1, 3, 5, 7 results are shown. 107

Figure 5.21a: Photographic view of the CMOS inverter chain 108

Figure 5.21b: Schematic view of the CMOS inverter chain 108

Figure 5.22: Measurements of a 8 bits, 0.5 Gb/s digital pattern (1010) over unpassivated pads. The simulation (a), EFM data (b) (3 pts smoothing), and contact probe (c) results at pad up1 are shown. 109

Figure 5.23: Propagation delay measurement over unpassivated pads. Results from sinulation (a), EFM (b), and contact probe (c) are shown. 111

Figure 5.24: Measurement of an 8 bits, 0.5 Gb/s digital pattern. Results from the unpassivated pad up5 (a), 1.2 μm passivated line (b), and passivated pad pp5 (c) are shown. 112

Figure 5.25: Propagation delay measurement over passivated pad. Results from simulation (a), and EFM (b) are shown. 113

List of Tables

Table 1: Truth table for the AND gate 78

CHAPTER 1

INTRODUCTION

Over the past decade, continuing increase in speed and minimization of integrated circuits' size, made possible by the improvements in technology has benefited the microelectronic areas. Computers are now capable of operating at a 450 MHz rate and this is expected to go up to 1 GHz in the near future. However, advances in a particular technology can only go as far as the ability to perform testing on that technology. Thus it is imperative to develop a measurement scheme that enables accurate evaluation of these devices. Measurements obtained from such testing can be used to optimize the design parameters and ultimately lead to a better product. The Conventional method of testing the device externally after packaging is no longer adequate and can be expensive, especially at the early developmental stage. In most cases, the ability to record data within a device is crucial to the understanding of its performance and failure analysis. Internal testing becomes increasingly difficult due to the complexity of the Integrated Circuits (ICs). At high frequency, direct probing can cause large disturbances and alter the normal operation of the circuits. Thus, the ideal internal testing technique must be non-invasive, and have high spatial resolution, high temporal resolution, high sensitivity. It must be easy to use and cost effective. Existing techniques fail to meet the above combined criteria.

This thesis investigates the pulse sample waveform measurements technique (pattern extraction) which is based on the Electrostatic Force Microscopes (EFM). A member of a growing Scanned Probe Microscopes (SPM) family, EFM is a non-invasive instrument which has demonstrated high spatial resolution. Using the heterodyne electrostatic force microscopy, measurements of high frequency digital pattern are performed. Narrow pulse generation techniques are also discussed.

The primary reference used in understanding the operating principle of the EFM was a doctoral thesis by Dr. Raa Said [38]. Dr. Raa Said along with Dr. G.E. Bridges and Dr. D.J. Thomson are the originators of the on going research at the University of Manitoba, regarding the applications of the electrostatic force microscope for non-invasive internal probing of high frequency integrated circuits.

Following this introduction, a brief discussion on the existing probing techniques in terms of their advantages and disadvantages is presented in chapter 2. Chapter 3 introduces the Electrostatic Force Microscopy. A history of the Scanned Probe Microscopes is presented first. This is followed by a detailed characterization of the EFM. Existing measurement schemes using the EFM are also discussed. In chapter 4, three narrow pulse generation techniques are evaluated. The outputs of each technique are also given. Chapter 5 introduces the pulse sample waveform measurement technique for extracting periodic digital pattern. Measurements on a 50Ω transmission line, CMOS and BiCMOS integrated circuits are presented. Finally this thesis is closed with a few concluding remarks in chapter 6.

CHAPTER 2

Brief Review of Existing Probing Method

Currently, there exist a number of diagnostic techniques that are used to characterize high frequency integrated circuits. This chapter will give a brief review of each technique and also discussed their advantages and disadvantages.

2.1 ON-WAFER CONTACT PROBING

As the speed of integrated circuits increases, the cost of packaging becomes increasingly expensive, therefore the conventional method of testing the circuit after packaging is no longer economical. On wafer probing introduces a technique in which the circuit can be characterized prior to it being packaged thus saving time and money. Microwave wafer probes (passive probes) which provide very high bandwidth are used to measure the signal at a desired point on the circuit under test. Commercially available since 1985, wafer probes have been used in FET, passive element and Monolithic Microwave Integrated Circuits (MMIC) characterization [48]. Figure 2.1 illustrates this technique where the sharp tips of the conducting probes are directly touched on the test points.

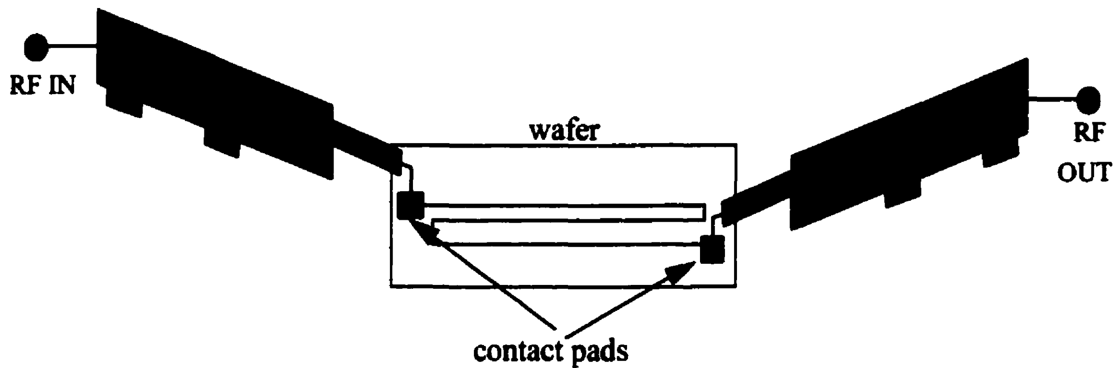


Figure 2.1: Schematic diagram of the on-wafer probing technique

It is desired for the probes to have 50Ω characteristic impedance for matching purposes since most types of measurement equipment use this impedance. Three main configurations of the wafer probes are coaxial, microstrip and co-planar waveguide[36]. In coaxial, the centre conductor is sharpened and extended beyond the outer shielding to form the probe tip. Figure 2.2a shows a schematic diagram of the coaxial probe. The probe provides a 50Ω impedance line to within 3mm of the tip. A major drawback of the coaxial probe is the difficulty in providing a good RF ground to the circuit under test. Low signal-level and capacitance measurements are the main application for this probe. For the microstrip configuration shown in figure 2.2b, a short needle probe is connected to the microstrip signal line. Similar to that of the coaxial, the microstrip probe does not provide good RF grounding thus limiting its use at high frequencies. One solution to eliminate the use of a short needle probe in the microstrip configuration is to reduce the width of the signal conductor to the size of the device pads. However, the fabrication process is proven to be very difficult. The third type of the wafer probe is the coplanar waveguide configuration where the signal line is located in the middle of the two ground planes. Figure 2.2c shows

a drawing of the coplanar waveguide probe. The signal line can be altered to match the size of the device test pad. Also, direct contact to the wafer is made by the tip thus eliminating the problems associated with inductive needles. The probe's large size is a disadvantage since only a limited number of them can be used simultaneously on a circuit and it also decreases accessibility to certain circuit test points. Wafer probing method has been used to characterize the S-Parameters of devices for MMIC development and manufacture at 26GHz [48].

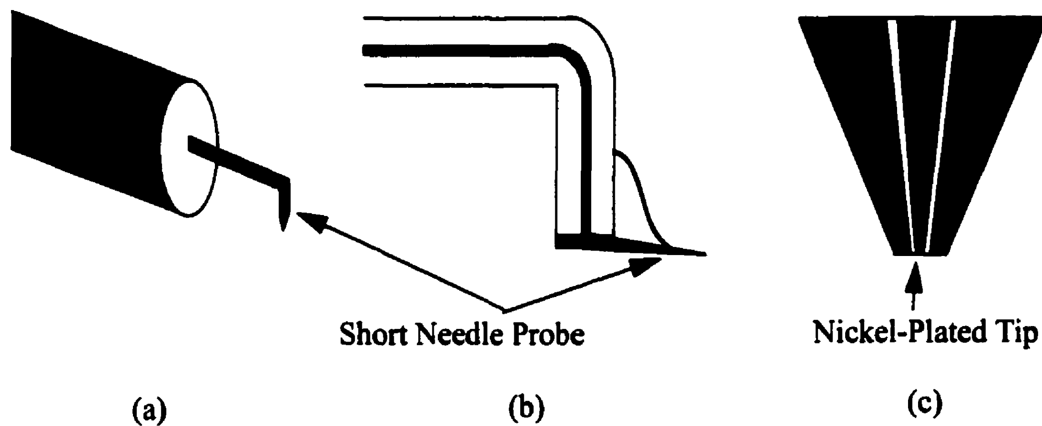


Figure 2.2: 3 different types of microwave wafer probes (a) coaxial (b) microstrip (c) coplanar waveguide

All of the probes discussed so far in the on-wafer probing techniques involve passive probes. However, active probes can also be used in this technique. Active probes which possess very high input impedance, are monolithic GaAs directional time-domain reflectometer integrated circuit (TDR) mounted on a low loss microwave wafer probes. The probes have been used in vector network analysis to 120GHz [62].

Disadvantages of the on wafer contact probing include disturbance of the normal circuit operation due to direct contact on the pads. Also limited number of points can be

tested on the circuit due to wafer space consideration. Thus a complete characterization on a circuit may not be possible.

2.2 NEAR FIELD PROBING

In near field probing, electromagnetic probes are used to measure the electrical and topographical characteristics of high frequency circuits. The technique utilizes coupling between the probes and the test point of the circuit under test. The two possible types of coupling are capacitive and inductive.

In the capacitive near field probing, measurements of the fringing electric field from the circuit to the probe are studied. An induced signal, generated when placing the probe close to the circuit, is measured. This induced signal can be related to the signal of the circuit under test. Illustration of this technique is shown in figure 2.3. The centre conductor of the coax cable is used as a coupling probe to the microstrip line. A spatial resolution of 15μm has been reported for micromachined probes in near field probing[5].

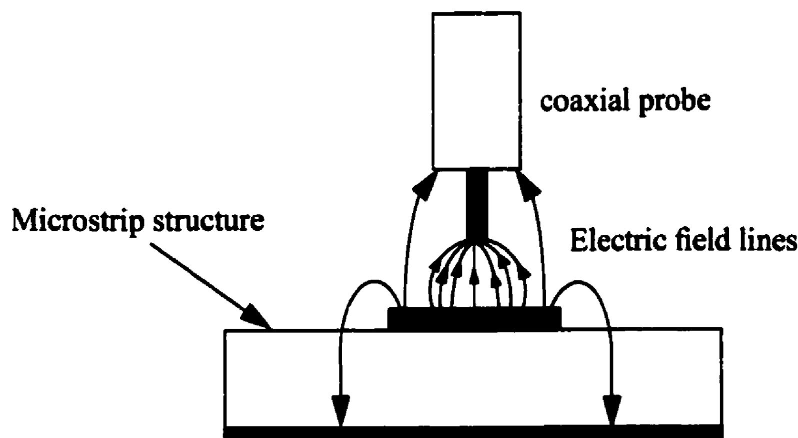


Figure 2.3: capacitive coupling between the circuit and the centre conductor of the coaxial probe

Inductive near field probing utilizes the coupling of the magnetic field lines between the circuit and a loop-shaped probe. The induce current which generated by the magnetic field lines is measured and can be used to characterize the test point of the circuit under test. Figure 2.4 a,b demonstrates the inductive coupling by showing the probe and the magnetic lines for the microstrip and coplanar waveguide configuration, respectively. To enhance the performance of the instrument, a double loop probe is recommended and is shown in figure 2.5.

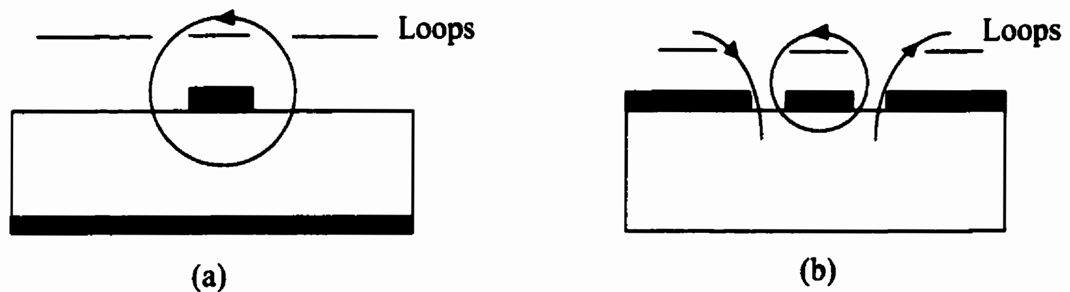


Figure 2.4: Inductive coupling [34] (a) microstrip (b) coplanar waveguide

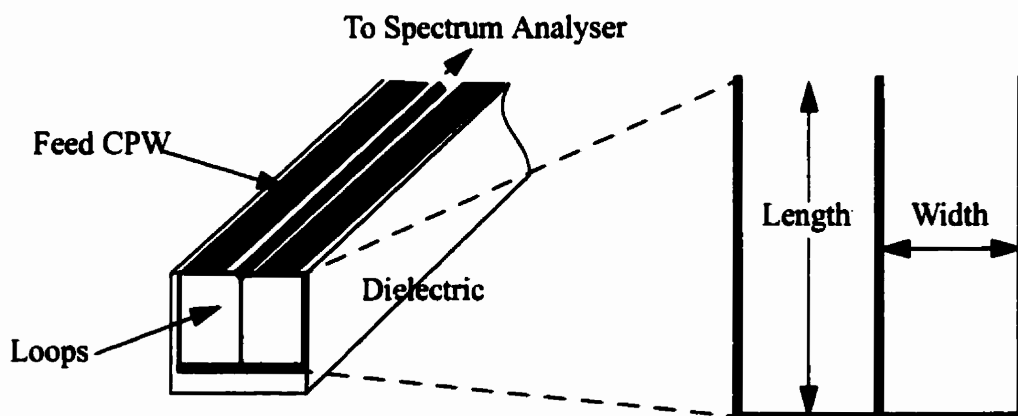


Figure 2.5: Double loop probe[34]

Near field probing has been demonstrated to be useful in circuit design and antenna diagnostics[15]. The miniature magnetic probe has proven to be a very capable tool for measuring the surface current distribution on high frequency planar circuits in the 1-20 GHz band [15].

Disadvantages of the near field probing technique include low spatial resolution and complex calibration required for absolute measurements.

Recently, a new concept is introduced where by combining the scanning force microscope (SFM) tip with a broadband near-field antenna, simultaneous measurement of topography and local AC electric fields can be obtained [54]. A diagram of the SFM tip with a planar transmission line integrated along the cantilever is shown in figure 2.6. This technique is capable of observing 30 ps edges of the waveforms along with the <10nm level topographical resolution. The spatial resolution depends on the radius of the tip.

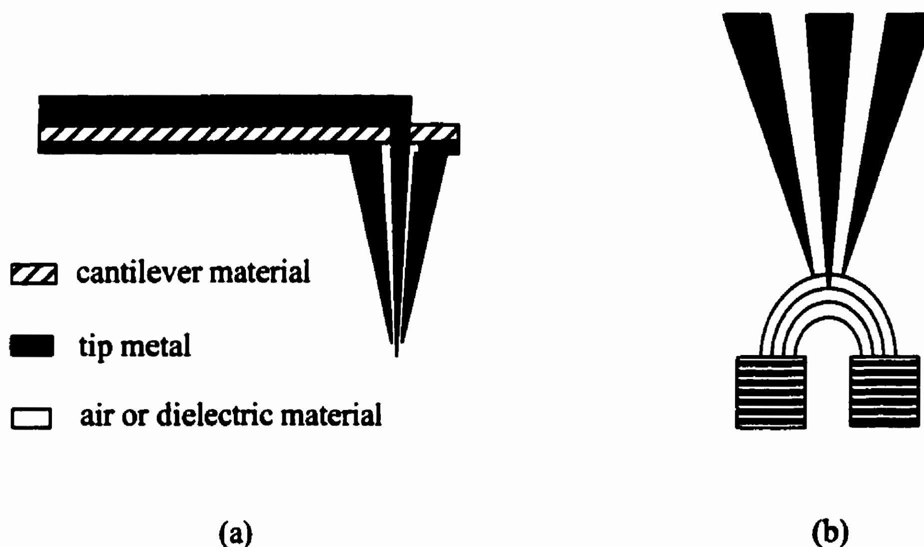


Figure 2.6: (a) Diagram of the coplanar configuration of the combined SFM/coaxial tip (b)close-up view of the tip and electric field lines between two conductors[54]

2.3 ELECTRON BEAM AND PHOTOEMISSION PROBING

Electron beam testing is an internal measurement technique. With the aid of an electron probe beam, this technique can be used to measure voltages on microelectronic circuits. Introduced to industry more than two decades ago, the E-beam testing has been used for verification and failure analysis of microelectronic circuits [61]. The operating principle of the E-beam technique is shown through figure 2.7 [60].

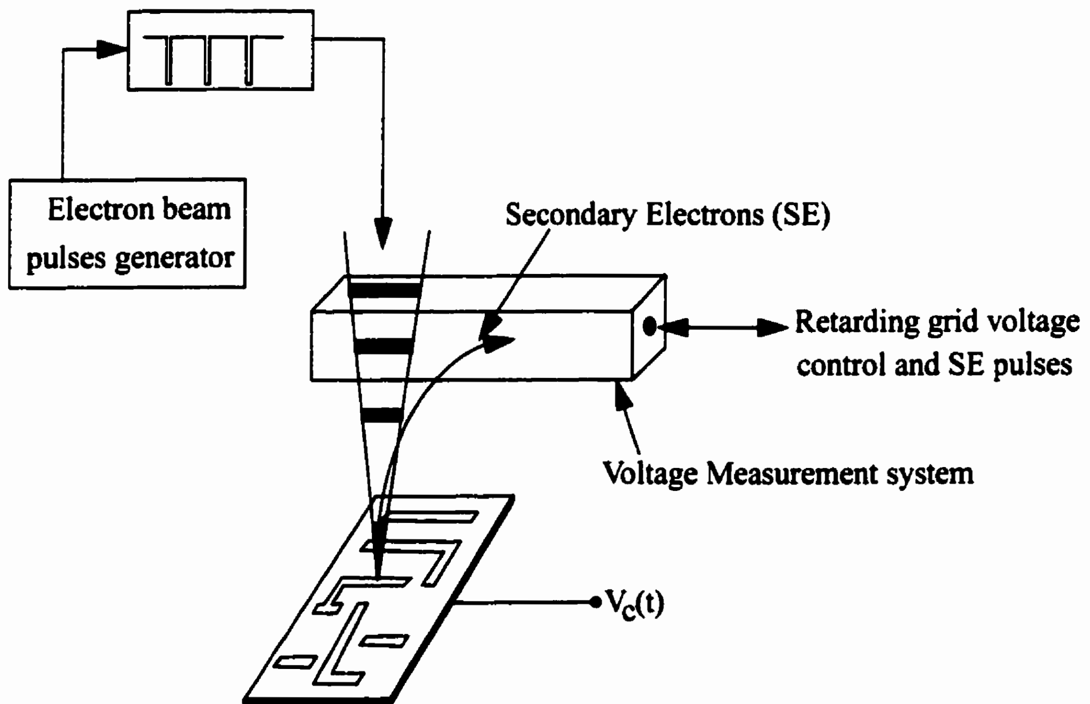


Figure 2.7: Block diagram illustrating the e-beam operating principle [60]

As the name suggested, E-beam testing technique involves the use of a pulsed electron beam. As demonstrated in figure 2.7, after focusing the electron pulses on the area of interest, an emission of the secondary electron is generated. A retarding grid spec-

trometer is placed in front of the detector which allows the analysis of the secondary electron beam, thus enabling the characterization of the voltage at the circuit's internal node. The voltage level of the probe dictates the number of the secondary electrons that can be detected by the detector. A feedback loop is used to keep a constant detector signal level by readjusting the retarding grid voltage. In this way, the retarding grid voltage can be used to track the voltage of the test area. In order to maintain a constant voltage to be sampled at a fixed phase relation, the beam control signal must be in synchronization with the repeated signal at the sample. The circuit's waveform is detected and thus recorded by shifting the phase relation between the circuit's signal and the electron-beam pulses.

By sampling the test signal with short electron pulses, the above E-beam probing technique can be used for waveform measurement in the high GHz frequency range [60]. Due to high spatial and voltage resolution, the E-beam technique is widely accepted for direct voltage measurement at the internal nodes of the integrated circuit (IC). Spatial resolution of under 1μm has been achieved for this technique [11]. The electron-beam pulse width dictates the temporal resolution of the technique.

The E-beam technique has demonstrated to be a very powerful tool for high frequency internal testing. However, draw backs of the technique include complex operation procedures and an expensive operating system. Measurements must be performed in a vacuum and thus complicated set-up are required. Other limitations of the technique include disturbance of the normal circuit operation by the impact of the electron beam irradiation.

A similar technique to that of the electron beam testing is photoemission probing[10]. In photoemission testing, the electron gun and the beam blanking system existing in the scanning electron microscopes is replaced by a pulsed/ photocathode combination. This technique operates by focusing a continuous(real time mode) or pulsed laser beam(sampling mode) onto a point of interest. Measurement procedures are similar to those of the E-beam technique. The temporal and spatial resolution of the photoemission technique has been reported to be 5ps and 0.1μm, respectively [24].

2.4 ELECTRO-OPTIC SAMPLING

Electro-optic sampling technique utilizes the changes in the birefringence properties of the crystal when in the presence of an electric field. This effect is known as the Pockel or electrooptic effect [53]. The result of the Pockel effect is an alteration of the polarization of light that travels through a crystal. The circuit's voltage can be determined by recording the change of polarization of an optical probe beam. Direct probing can be performed for materials which possess electrooptic characteristics such as GaAs and InP. This is shown in figure 2.8 a and b. External electrooptic probing is used for non-electrooptic materials as shown in figure 2.8 c.

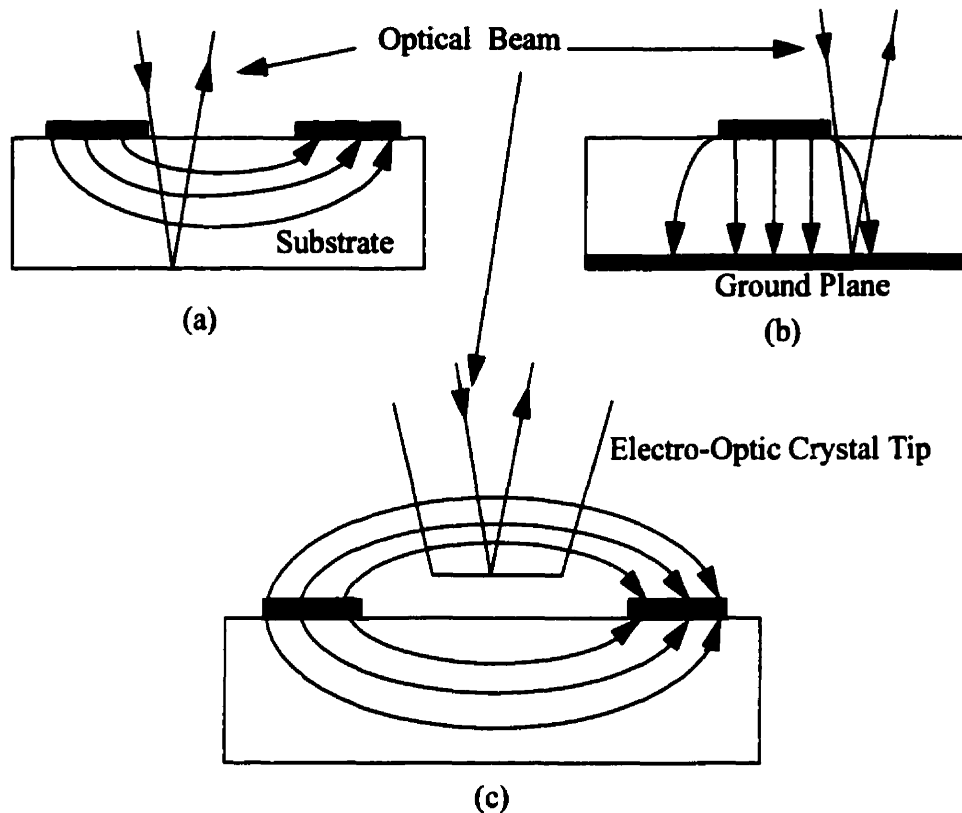


Figure 2.8: Three possible probing geometries for electro-optic sampling (a)front side probing for coplanar geometry (b) front side probing for microstrip lines (c) external probing for coplanar waveguide device.

Schematic diagram of the electrooptic sampling technique is shown in figure 2.9. In this set-up, a laser beam is focused directly onto the electro-optic crystal probe which is being held in close proximity to the desired test point. A mirror at the bottom of the probe causes the laser beam to reflect back to the polarizing beam splitter which is used to modulate the beam intensity. After passing through the crystal, the laser beam's polarization depends on the signal of the circuit. The beam is then detected and measured by using a lock-in amplifier or a digital oscilloscope resulting in the knowledge of the circuit signal.

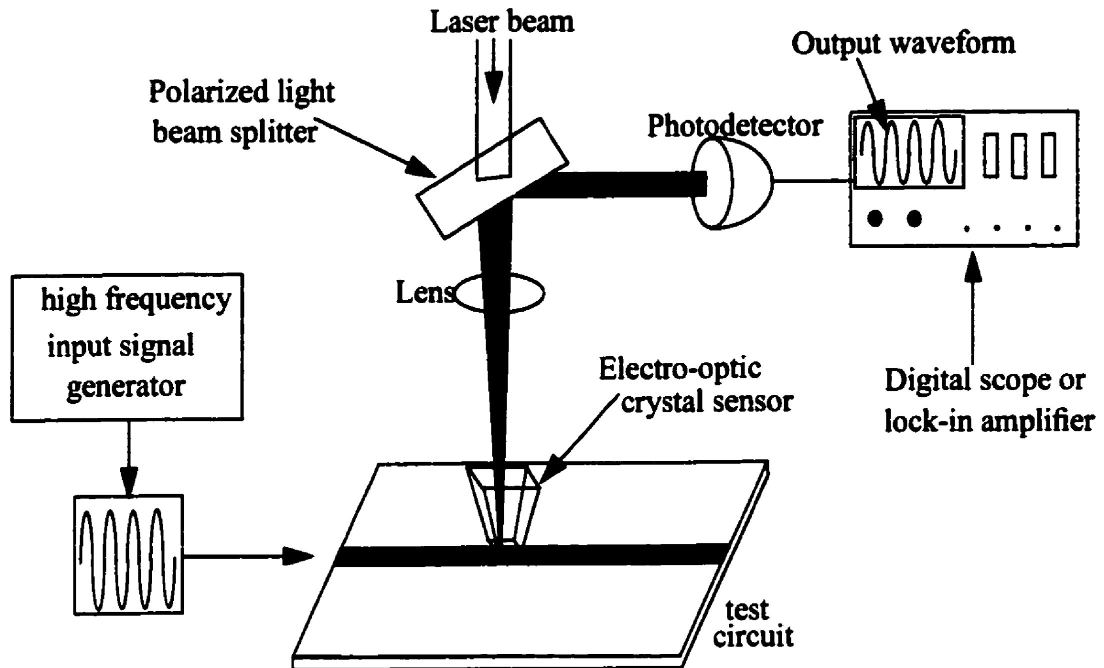


Figure 2.9: Diagram for the operating principle of electrooptic sampling technique[49]

In high frequency signal measurements, narrow laser pulses are used as sampling gates. Improvement in the laser technology have benefited the electrooptic sampling technique. pulses with sub-100 fs width have been used in some cases which results in a temporal resolution in the ten picosecond range [59]. Other factors contribute to the temporal resolution include the response time of the elctro-optic effect, transit time effects and timing jitter between the excitation signal and the probe pulse [59]. The spatial resolution depends on the spot size of the focused laser beam. Beam spot sizes of 0.5μm in diameter have been reported for the direct electrooptic sampling system [12]. It has been reported that the frequency bandwidth of the sampling technique is about 10 GHz with a minimum detectable voltage of 0.4 $mV/\sqrt{Hz}$ [49].

Applications of the electrooptic sampling can be seen in internal field mapping of MMIC's[25]. The technique has also been used for measurement of signals at internal nodes of integrated circuits [59] and evaluation of ultrafast pulses on MMIC devices[21].

As in E-beam, the electrooptic sampling system is quite complicated and cumbersome to operate. High cost and complex calibration procedures make the technique less attractive as a commercial tool for microelectronic testing.

2.5 OPTOELECTRONIC SAMPLING

Opotoelectronic sampling, often referred to as photoconductive sampling, is an ultra-fast pulse generation technique in which photoconductive switches are used. The technique is used to internally measure the signals in high speed electronic circuits. A typical photoconductive switch is normally fabricated by using a doped semiconductor material with metallic electrodes configured as transmission line. A small gap exists between the metal electrodes where by the optical beam is focused. Photoconductive switches are key components in making the photoconductive sampling probes. A metal-Semiconductor-metal photoconductive sampling probe is shown in figure 2.10. The probe consists of a titanium tip and photoconductive switch deposited on a low temperature GaAs layer.

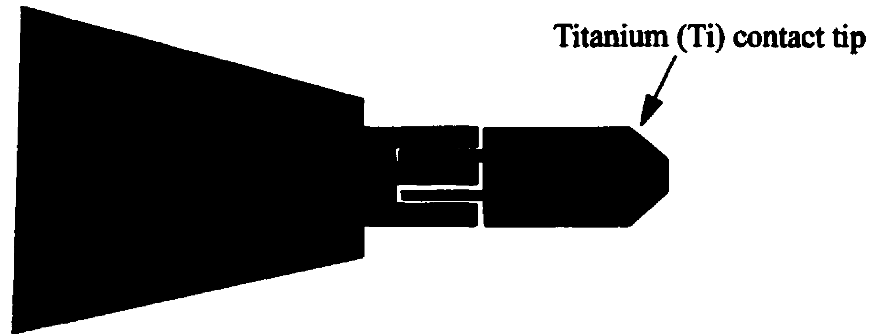


Figure 2.10: A drawing of the photoconductive probe. A typical probe consists of a titanium contact tip with 8μm in diameter and 3μm height, and a photoconductive switch with 2μm width and spacing. The tip and switch are usually deposited on a MBE-grown Low Temperature GaAs layer.[19]

Using a picosecond laser source to excite the photoconductive switch, this technique has been known to generate ultra-short duration pulse signals thus enabling high speed signals at test points of integrated circuits to be sampled. The photoconductive sampling technique has been demonstrated to be extremely useful in broadband characterization of monolithic microwave integrated circuits (MMIC) at GHz range [21].

The temporal resolution of this technique is limited by the carrier lifetime of the semiconductor material used to make the photoconductive gate. The photoconductive sampling probe shown in figure 2.10 is reported to have a temporal resolution of 2.3 ps[19]. Voltage sensitivity of 4 μV has also been demonstrated by the probe. The probe capacitance is less than 0.1 fF and its resistance of 100 MΩ, making it attractive to noninvasive testing of ultra-high speed devices and circuits.

CHAPTER 3

Electrostatic Force Microscope

In this chapter, a brief history of the Scanning Probe Microscope is given. Next, a member of the SPM group called the Electrostatic Force Microscope (EFM) is discussed. Operating principle of the EFM instrument used in this research along with its characterization are presented. Finally, existing measurement schemes using EFM are reviewed.

3.1 Scanning Probe Microscopes

Recent developments of the new scanning probe microscopy (SPM) technique [56] allows researchers to have a simple and direct observation of microscopic materials. The technique is capable of mapping electrical, magnetic, mechanical and thermal properties of surfaces. The operating principle of the SPM involves a tiny sharp probe with its tip positioned above the surface to be investigated. As the tip scans across the surface, the interaction of the tip and surface is monitored and recorded, thus yielding the surface's properties. The SPM technique has a remarkably high resolution due to the nanometer radius curvature of the tip. The high resolution of the technique allows observation of a single atom.

The Scanning Tunnelling Microscopes (STM), which was invented by G. Binnig and H. Rohrer, is the first scanned probe microscope developed. STM enables measurements at the atomic scale level. The general operating principle of the STM involves the tunnelling of current from tip to the surface. Beside having the ability to observe a single atom, STM can also be used to move each individual atom to a different location along the surface [51]. Stemming from the idea of the STM, a technique called Scanning Tunnelling Potentiometry (STP) is developed to allow simultaneous probing of the topographic image along with the potential distribution of the sample's surface [28]. STP is a major contributor to the study and understanding of local electron transport properties [58].

Following the success of the STM, Atomic Force Microscope (AFM) was developed to accommodate experiments involving non-conducting surfaces. The idea of a very sharp tip scanning across a surface is also employed in the AFM. A diamond tip is normally used in [57]. Figure 3.1 shows the schematic of AFM. The one major point separating the AFM from the STM is the interacting force between the tip and surface. In AFM, measurements are done by monitoring the repulsive forces existing between the tip and the surface. As the tip rasters across the surface, the probe deflects. The probe's deflection is detected and a control signal is produced. Using a feed back loop, the probe's deflection and thus the repulsive force is kept constant through out the entire scanning process. Topographic image of the surface is depicted by recording the variation in the vertical z position as the tip scans across the surface. In the early developmental stage of the AFM, tunnelling current has used to detect the probe's deflection. In subsequent years, in an effort to improve the deflection sensor, the tunnelling current detection technique has been replaced by the optical beam detection technique. As a result, more accurate measure-

ments were achieved.

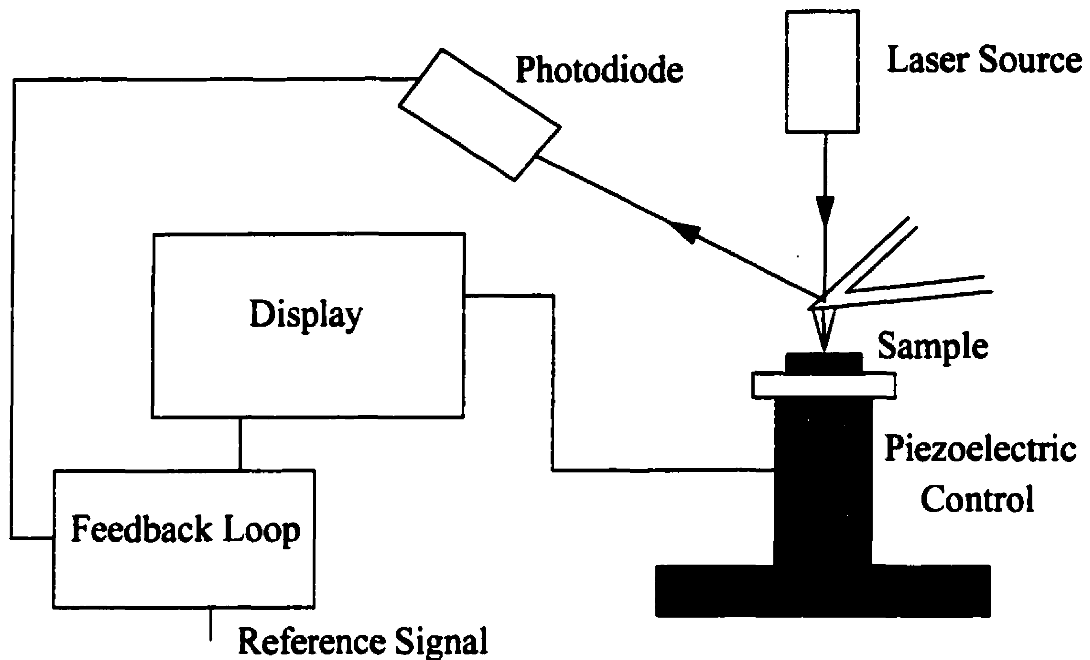


Figure 3.1: Schematic view of the AFM operating principle

Other techniques such as the Scanning Capacitance Microscopy (SCM) have been developed to allow dopant profiling of a semiconductor. This technique has a spatial resolution in the nanometer scale[18]. Another technique which is used for similar purpose as the SCM is the Scanning Resistance Microscopy (SRM).

The techniques mentioned so far are used to study the surface of the sample. However, in some cases, subsurface information is desired. A technique called Ballistic Electron Emission Microscopy (BEEM) has been introduced to allow the investigation of buried interfaces which are located far below the surface[3]. Since its invention, BEEM has been widely used to investigate the metal-semiconductor interfaces. A schematic diagram of the technique is shown in figure 3.2, where an STM tip is carefully placed close to the metal-semiconductor interface. As in STM, electrons tunnel from the tip to the metal

base resulting in the current I_{tip}. Some of the tunnelling electrons have energy which exceed the schottky barrier height of the metal-semiconductor and thus ballistically cross the barrier. The propagation of the ballistic electrons across the schottky barrier height allow the probing of the subsurface metal-semiconductor interface.

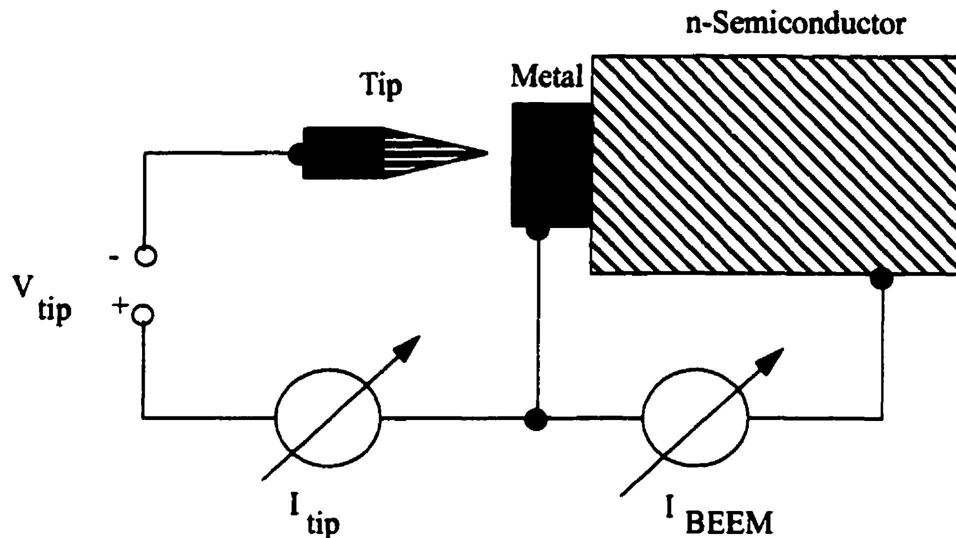


Figure 3.2: Schematic view of the Ballistic Electron Emission Microscopy (BEEM)

In diagnostic testing of microelectronic circuits, contact force microscopy can be destructive to the profiling of the circuit's surface. In some instances, disturbance of the circuit can lead to an alteration of the circuit's normal operation. Thus, non-contact measurement techniques play a vital role in probing and testing of such circuits. One example of the non-contact force microscopy is the Laser Force Microscopy (LFM) [57]. The LFM inspired by the Atomic Force Microscope, uses an optical detection sensor. The tip is positioned a few nanometers away from the sample surface. Forces involved in this technique are large due to the surface tension of water that condenses between the tip and sample. Van Der Wals forces also play a role in the LFM technique. The tip vibrates as it is being brought closer to the sample. The vibration of the tip is sensed by a sensitive laser probe

and a feedback mechanism is used to keep the probe-sample separation in a constant mode. Variation of the voltage signal used in the feedback mechanism corresponds to the surface profile.

Another example of the non-contact force microscopy is the Magnetic Force Microscopes which uses a sharp magnetic tip attached to the end of the cantilever probe [37]. Having the same concept to that of the LFM, the MFM is used to investigate the recording pattern's structure on a disk or other magnetic media.

In an effort to keep pace with the ever growing technology of microelectronic ICs design and manufacturing, a special instrument called Electrostatic Force Microscope (EFM) [56] has been developed for diagnostic internal testing. By monitoring the electrostatic force between the probe and the sample, the EFM instrument measures the surface's localized potential. Usage of the technique extends from dopant profiling of semiconductors [17] to depositing and imaging localized surface charge on insulators [46,47]. The microscopes have also been used for imaging ferroelectric domain walls [44]. Measurements of contact potential difference between different materials have also been investigated by the EFM. In this research, the instrument utilizes the idea of the Electrostatic Force Microscopy. In the next few sections, the general operating principle of the EFM along with the proposed instrument's characterization are presented.

3.2 A Brief Overview of EFM

The fundamental theory behind the EFM is the electrostatic force between the probe tip and the circuit test point. The existence of electrostatic force causes a mechanical deflection of the probe which is detected by the photodector placed near by. EFM is a

non-invasive diagnostic technique . A visual understanding of the EFM is shown in figure 3.3.

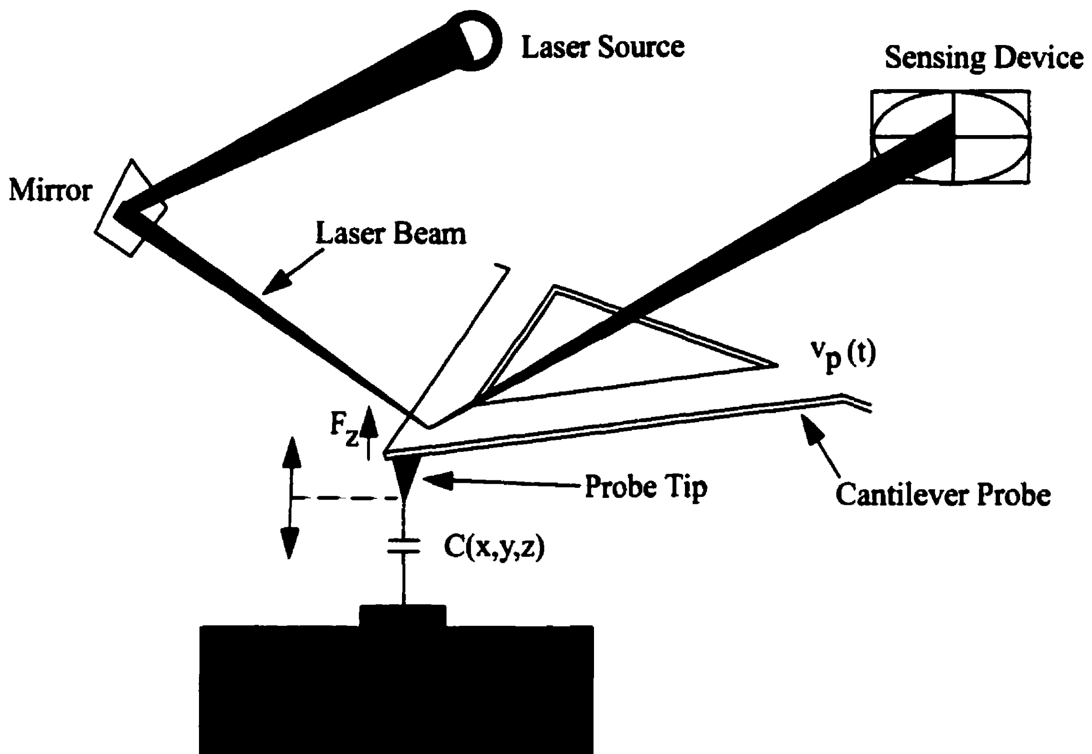


Figure 3.3: EFM illustration using the micro-machined probe and beam bounce sensor system

The probe's sharp tip is carefully positioned as close to the circuit's test point as possible without making contact. The separation between the tip and the test point is a contributing factor to the magnitude of the probe's mechanical deflection. The probe in figure 3.3 is mounted in such a way that it resembles a cantilever. In this way, the probe is allowed to deflect under an external applied force. A controllable voltage $v_p(t)$ is applied to the conducting probe. As the external voltage is applied to the probe, a small localized capacitance $C(x,y,z)$ is formed between the tip of the probe and the circuit test point. The potential difference between $v_p(t)$ and $v_c(x,y,t)$ charges up the localized capacitance. The

amount of work done in charging up the capacitor is given as

$$W = \frac{1}{2}C(x,y,z)\,[v_p(t) - v_c(x,y,t)]^2$$

Equation 3.1: Work done required to charge up the mutual capacitor

Since force is defined as the derivative of work with respect to distance, the electrostatic force in the z-direction has a non-linear dependence on the potential difference between the probe's tip and the circuit test point and can be expressed as:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\,[v_p(t) - v_c(x,y,t)]^2$$

Equation 3.2: Electrostatic Force between the probe tip and circuit test point

The electrostatic force F_z depends on the mutual capacitance *C(x,y,z)* between the probe and the circuit. The magnitude of the component *C(x,y,z)* is dependent on the circuit geometry, the probe's tip, and the separation between the probe with respect to the circuit's surface. It is essential to know the magnitude of the mutual capacitance *C(x,y,z)* in characterizing the spatial and temporal resolution of the instrument. However, the voltage measurement techniques used in this research do not required the knowledge of *C(x,y,z)*. The fringing capacitance, that exists in *C(x,y,z)*, minimizes due to the probe sharp tip geometry, thus maximizing the spatial resolution.

The electrostatic force F_z causes a deflection, *z*, of the probe cantilever. The amount of deflection by the probe cantilever depends on the mechanical properties of the probe and the magnitude of F_z. By recording this deflection using a photodetector, the force and ultimately the potential difference can be extracted. This is a brief overview of the operating principle behind Electrostatic Force Microscopy.

3.3 Experimental Set-Up of EFM

A physical set-up of the EFM instrument is shown in figure 3.4. An aluminium structure is used to support the system.

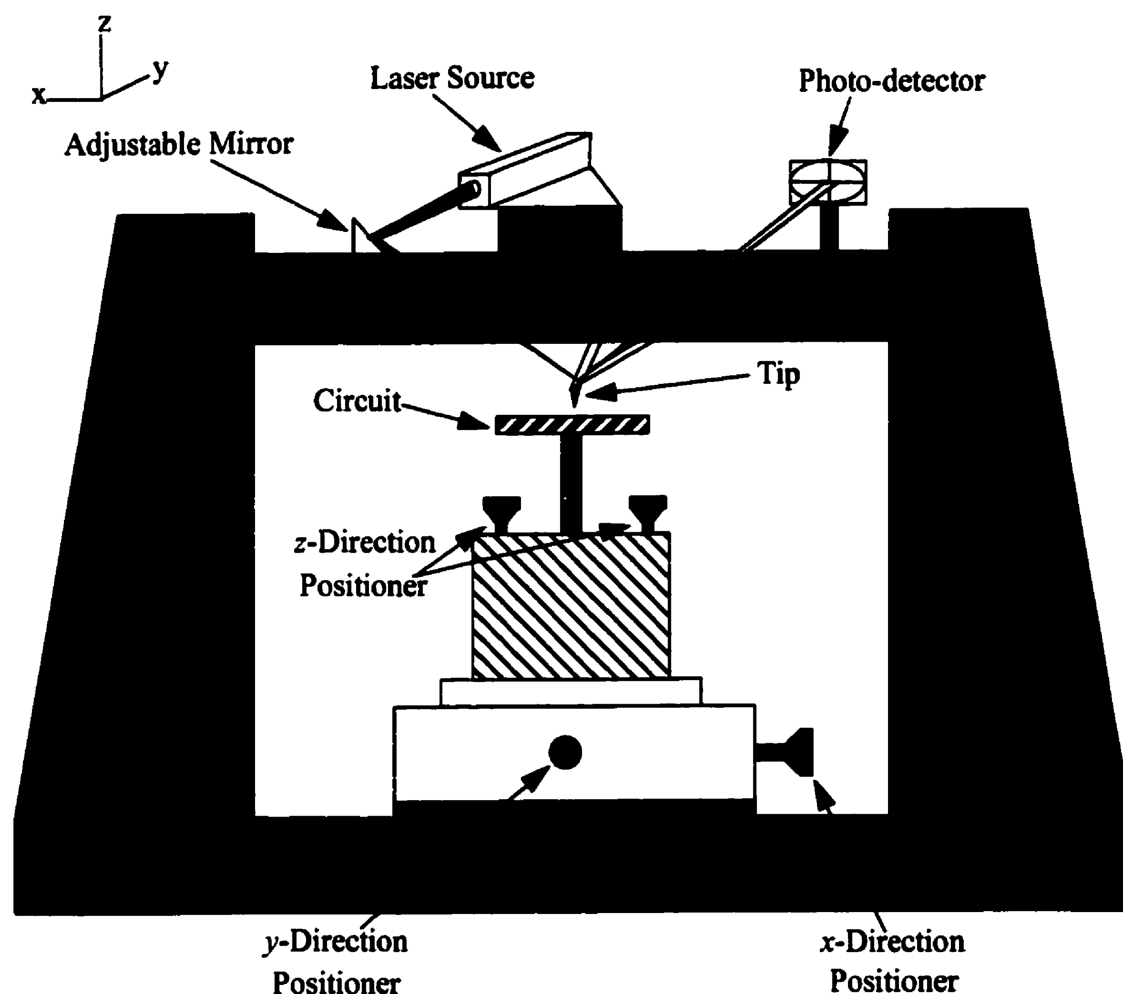


Figure 3.4: physical set-up of the EFM using the Beam Bounce System

The *x*, *y*, and *z* direction positioner can be used to adjust the circuit to a desirable position. These direction positioners are accurate to the order of a micrometer. The adjustable mirror is used to control the reflection angle of the laser beam so that the reflecting beam is directly hitting the end of the cantilever. The Photodetector can also be adjusted to

catch the beam as it is reflected off the end of the cantilever.

3.3.1 Micro-machined Probe Characterization

The cantilever probe, often known as a spring, is an essential part in the EFM experimental set-up. The cantilever is used to detect the vertical deflection caused by a potential difference in the probe signal and the circuit signal. The speed, accuracy and stability of the EFM depend on the properties of the cantilever. A typical cantilever is fabricated from silicon dioxide, silicon nitride(Si_3N_4), and pure silicon. In this project, a Si_3N_4 cantilever was used. Figure 3.5a shows a typical Si_3N_4 cantilever along with its typical properties. In figure 3.5b, a SEM micrographs of Si_3N_4 cantilever along with pyramidal tip is shown.

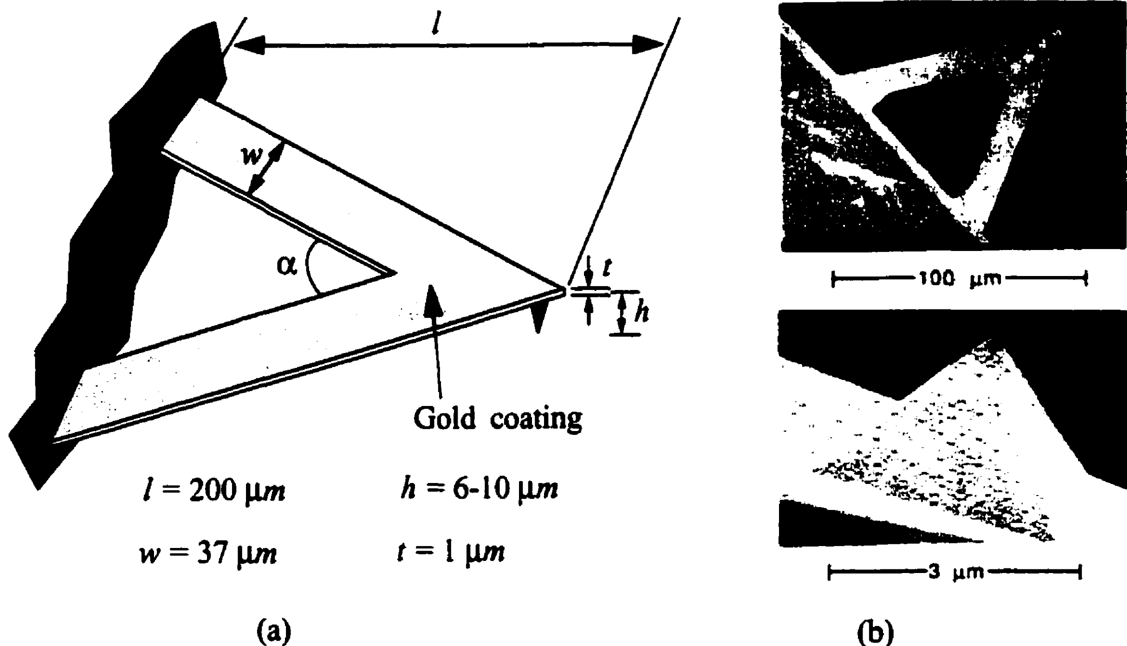


Figure 3.5: (a) EFM cantilever with its principal parameters (b) SEM micrographs of Si3N4 cantilever (top) and pyramidal tip (bottom). [58]

The pyramidal tip is located 4-8 μm from the end of the cantilever. The radius of curvature of the tip is approximately 300*nm*. The v-shape angle, α, is typically around 57^{0} . The cantilever is coated with a thin layer of gold film for conducting and reflecting purposes.

In the following sections, the mechanical properties of the cantilever used for this project will be discussed. The cantilever will be characterized in terms of its spring constant, natural resonant frequency and the frequency response.

3.3.1.1 Spring Constant

The spring constant, *k*, is defined as the amount of force required to deflect the cantilever. For a simple rectangular beam of length *l* and moment of inertia *I*, the spring constant is given as:

$$k = \frac{3EI}{l^3}$$

Equation 3.3: spring constant of a simple rectangular beam

where E is the Young's modulus of elasticity of the beam material. The moment of inertia is different for different cross sections. For a rectangular cross section as shown in figure 3.4 with a width "d" and thickness "t", the moment of inertia is $I = \frac{wt^3}{12}$. Substitute I into equation 3.3, the spring constant becomes

$$k = \frac{Ewt^3}{4l^3}$$

Equation 3.4: spring constant in term of the length, width and thickness of cantilever

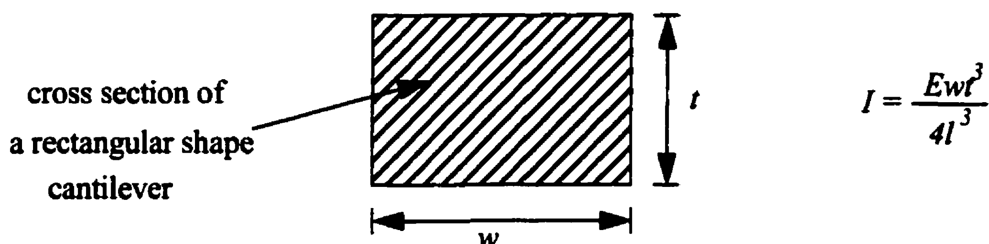


Figure 3.6: moment of inertia for a rectangular cross section

The effective spring constant for two identical beams mounted in parallel can be approximated by $2k$ [33], where k is the spring constant for one beam. The spring constant in figure 3.6 can be approximated using equation 3.4 and the above analogy. For a more accurate evaluation of the EFM spring constant, the readers can refer to reference [30]. Using E=1.5 x 10^{11} N/m^2, for an EFM rectangular beam of 200μm long, 37μm wide and 1μm thick, the spring constant is approximated at 0.347 N/m.

3.3.1.2 Natural Resonant Frequency

The resonant frequency of the cantilever is an integral property in force microscopes. For contact mode microscopy, the resonant frequency controls the speed of the microscope at which the surface can be tracked. In EFM, the knowledge of the resonant frequency helps to monitor the maximum vertical deflection of the cantilever. This is critical since the small vertical deflections at other frequencies are difficult to detect. For a rectangular beam, the resonant frequency is given by [43]:

$$\omega_r = \sqrt{\frac{Ewt^3}{4l^3(m_c + 0.24wtl\rho)}}$$

Equation 3.5: resonant frequency of a rectangular beam

where ρ represents the mass per unit length of the cantilever and m_c is the tip's mass. Other parameters in equation 3.5 are the same as those defined in section 3.3.1.1. The resonant frequency of two parallel beams can be approximated as $\sqrt{2}\omega_r$ [33]. Using ρ = 3100 kg/m^3, E = 1.5 x 10^{11} N/m^2, l = 200 μm, w = 37μm, t = 1 μm, and the above approximation, the resonant frequency is 19.6 *kHz*. This is not entirely accurate since the specified dimensions of the cantilever are not very accurate. Thus it is recommended that the resonant frequency should be determined experimentally.

3.3.1.3 Frequency Response

Consider a rectangular beam cantilever with an external applied time varying force of unit amplitude. The frequency response of this system is defined as the ratio of the cantilever vibration to the external applied force. At a driving frequency near resonance, a damped harmonic oscillator model can be used to represent the system[39]. Thus, for an external applied force of unit amplitude, the frequency response is given by:

$$|G(\omega)| = \frac{(Q/k)\ (\omega_r/\omega)}{\sqrt{1 + Q^2(\omega/\omega_r - \omega_r/\omega)^2}}$$

Equation 3.6: frequency response of a cantilever with an external applied force

The parameter ω_r in equation 3.6 represent the lowest resonant frequency of the cantilever with an applied external force [1]. Q is the cantilever's quality factor and is given as $\omega_r/\Delta\omega$, where $\Delta\omega$ is defined as the 3-dB bandwidth of the cantilever's frequency response. When the system is at resonance, that is $\omega = \omega_r$, equation 3.6 becomes

$|G(\omega = \omega_r)| = \frac{Q}{k}$. This means that the vibration of the cantilever is increased by a factor of Q/k. To experimentally determine the frequency response of the Si_3N_4 cantilever, only the oscillation from the thermal excitation is required due to the cantilever being extremely light in mass. Therefore, no external applied force is needed. The frequency response of a typical Si_3N_4 cantilever is shown is figure 3.7[32]. The theoretical frequency response is calculated and normalized and it is fitted onto the experimental curve. The quality factor of this cantilever, Q, is found to be 32. The resonant frequency is 12.275 *kHz*.

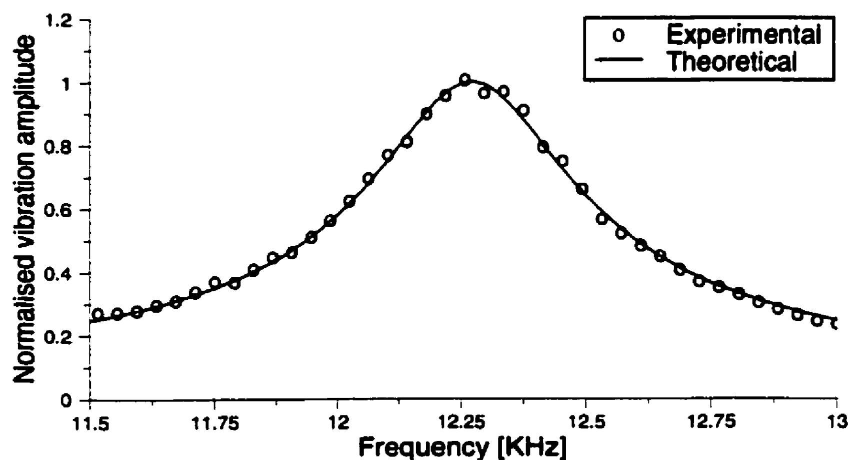


Figure 3.7: Experimental and theoretical frequency response curve of a typical Si_3N_4 cantilever which has a resonant frequency of 12.275 kHz with Q of 32 [32].

3.3.2 Deflection Sensors

In a typical EFM experiment, the deflection of the cantilever probe is usually very small and difficult to detect. Therefore, it is essential to have an accurate and easy to use detection technique to obtain fast and concise results. In the next section, a sample calcu-

lation of the probe deflection using a simple model for the tip, is presented.

3.3.2.1 Deflection Calculation using a Simple Model for the Tip

Figure 3.8 shows the model used to represent the tip of the cantilever probe over the sample. The tip is modelled as a sphere over a ground plane which represents the circuit under test.

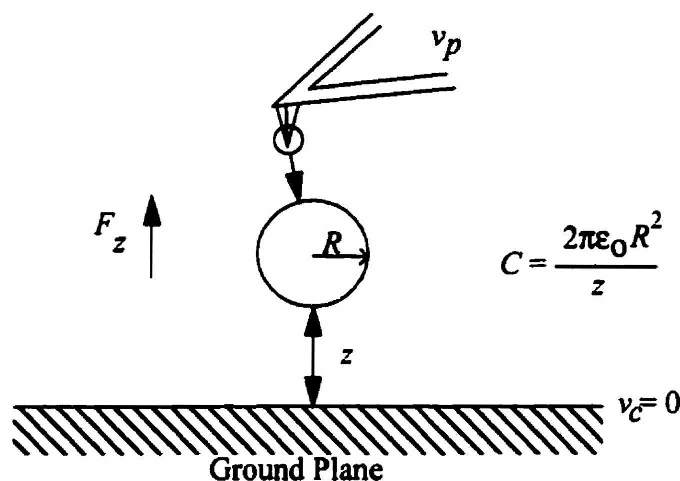


Figure 3.8: A spherical model is used to represent the tip and the circuit under test is modelled by a ground plane.

When $z << R$, the total capacitance between the probe and the plane is given as [15]:

$$C = \frac{2\pi\varepsilon_o R^2}{z}$$

Equation 3.7: total capacitance between tip and surface

The capacitance in equation 3.7 is calculated using a parallel plate capacitor

model. The approximate effective area for this model is $2\pi R^2$. The stored energy of this capacitor is given by:

$$W = \frac{1}{2}C(v_p - v_c)^2$$

Equation 3.8: stored energy of the total capacitance

The force between the probe and the surface is calculated by taking the derivative of equation 3.8 with respect to the separation distance between the probe and the surface.

$$F_z = \frac{1}{2}\frac{\partial C}{\partial z}(v_p - v_c)^2 = \frac{\pi\varepsilon_o R^2 v_p^2}{z^2}$$

Equation 3.9: electrostatic force between tip and surface

For a typical cantilever probe, the tip's radius is 200*nm*. If the separation distance between the probe and the surface is about 1μm and a potential difference is 1 *V*, the force is calculated to be:

$$F_z = \frac{\pi(8.85\times10^{-12})(200\times10^{-9})^2(1)}{(1\times10^{-6})^2} = 1.11\times10^{-12}N$$

Equation 3.10: magnitude of the force between tip and surface

Using the spring constant of 0.347 *N/m*, the deflection of the cantilever is $3.2\times10^{-3}nm$. For a maximum deflection, the probe's signal is modulated at resonant frequency. This maximizes the quality factor Q of 32 and gives a maximum probe deflection of 0.1024 *nm*. A deflection of such a small magnitude requires an accurate detection system. In the next section, a beam bounce detection technique is presented.

3.3.3 Beam Bounce Detection Technique

Figure 3.9 shows a diagram of the beam bounce detection technique. The optical beam, which is generated by a laser, is focused onto the end of the cantilever. A photodector is used to intercept the reflected optical beam which then is used to characterized the deflection of the cantilever. The parameters l and L in figure 3.9 represent the length of the cantilever and the lever-photodetector spacing, respectively.

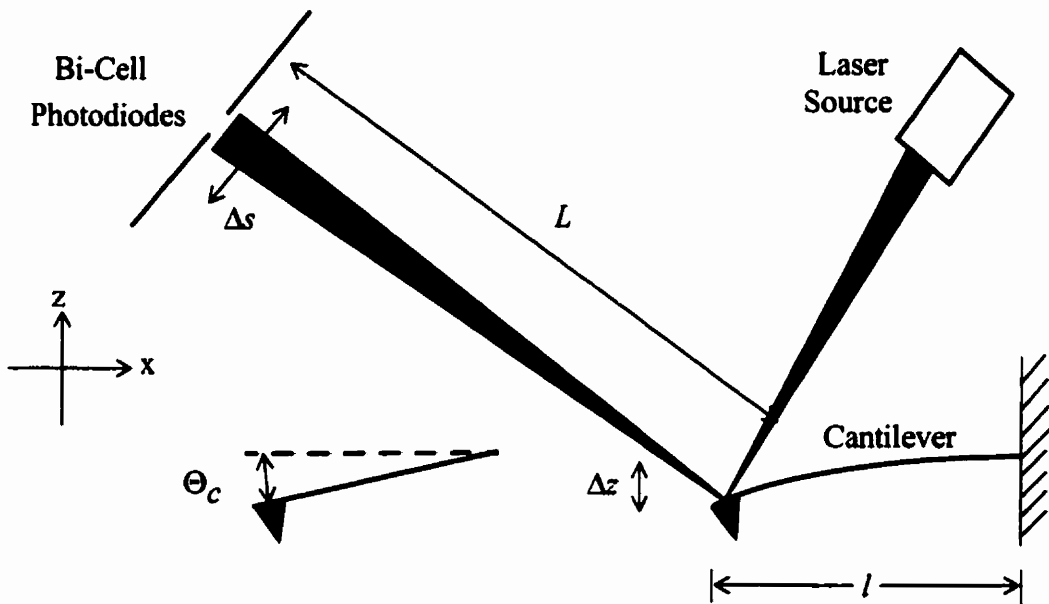


Figure 3.9: Diagram of the beam bounce detection technique

The deflection due to the force *F* applied at the end of the cantilever is given as [13]:

$$z(x) = \frac{1}{2}\left[3\left(\frac{x}{l}\right)^2 - \left(\frac{x}{l}\right)^3\right]\frac{Fl^3}{3EI}$$

Equation 3.11: Deflection of the cantilever when applied a force at tip

For a small deflection, the angle generated as the cantilever is bent is approximated by:

$$\Theta_c \approx \frac{d}{dx}z(x) = \frac{Flx}{EI} - \frac{Fx^2}{2EI}$$

Equation 3.12: Angle generate by a small deflection

Since force is applied at the end of the cantilever, $x=l$, equation 3.12 becomes:

$$\Theta_c \approx \frac{Fl^2}{2EI}$$

Equation 3.12a: Deflection angle when a force applied at the end of the cantilever

Substitutes $F=kz$ and $k = \frac{3EI}{l^3}$ into equation 3.12a gives:

$$\Theta_c \approx \frac{3\Delta z}{2l}$$

Equation 3.13: Deflections angle in relation with the vertical deflection Δz

As the cantilever is deflecting, the optical beam is reflected onto the surface of the photo-detector. This is illustrated in figure 3.10:

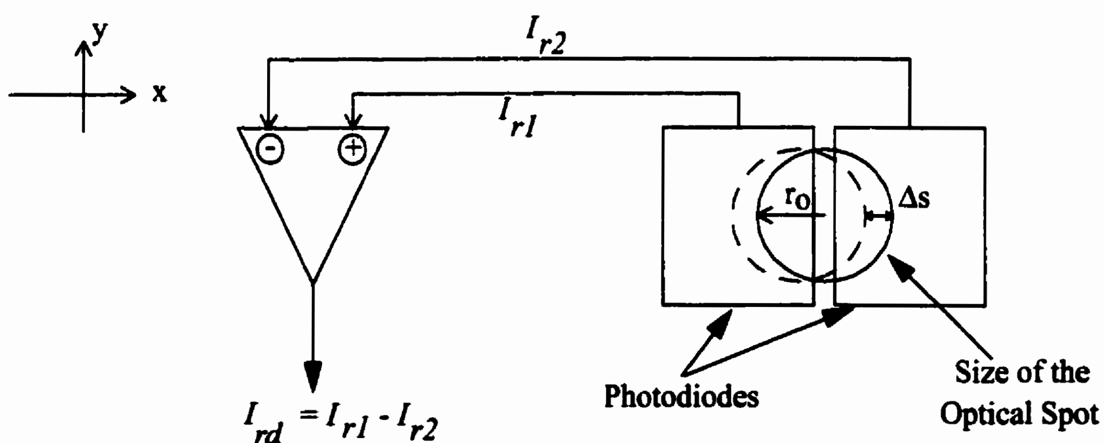


Figure 3.10: Deflection of the optical beam

The deflection of the optical beam is given as [18]:

$$\Delta s = \frac{3L\Delta z}{2l}$$

Equation 3.14: Optical beam's deflection

The deflection of the optical beam produces an inequality of the optical power in the bi-cell. That is, there is more optical power falling on one side of the bi-cell than the other. Before continuing to determine the resulting signal I_{rd} in relation to the cantilever deflection, some assumptions must be made. It is valid to assume that the optical beam is monochromatic and posses a characteristic of a gaussian distribution. The irradiance, which is the power incident per unit area, at the distance r from the center of the beam is given by [52]:

$$I_r = I_o e^{\frac{-2r^2}{r_o^2}} = I_o e^{-\frac{2}{r_o^2}(x^2+y^2)}$$

Equation 3.15: Irradiance of a laser beam

The parameter I_o in equation 3.15 represent the irradiance at the center of the beam. r_o is the beam edge at where the irradiance falls to $1/e^2$ of the center value. The power of the laser beam falling on the photodector can be determined by integrating the irradiance over the incidence surface. In order to solve for I_{rd}, the photocurrent of each side of the bi-cell must be determined. For a unit conversion efficiency, the photocurrent is equal to the number of photons falling on each side of the bi-cell per unit time multiplied by the unit charge, q. The power of the beam is proprotional to the number of phontons falling per unit time. Since the spacing of the two bi-cells is small, therefore it is to be neglected to further simplified the calculation process. The resulting signal I_{rd} is determined by the

integration of the normalized gaussian distribution in equation 3.15 as follows:

$$I_{rd} = 2Nq\int_{0}^{\Delta s}\int_{-Y}^{Y}\frac{e^{-\frac{2}{r_o}(x^2+y^2)}}{r_o^2(\pi/2)}dxdy$$

Equation 3.16: The output signal of the beam bounce deflection technique

N represents the total number of photons in the beam falling on the detector per unit time and q is the charge of an electron. Since $Y>>r_o$ equation 3.16 can be simplified as:

$$I_{rd} = \frac{4Nq}{r_o^2\pi}\int_{0}^{\Delta s} e^{\left(-\frac{2}{r_o^2}\right)x^2}dx\int_{-\infty}^{\infty} e^{\left(-\frac{2}{r_o^2}\right)y^2}dy = \frac{2\sqrt{2}Nq}{r_o\pi}\int_{0}^{\Delta s} e^{\left(-\frac{2}{r_o^2}\right)x^2}dx$$

Equation 3.16a: Simplified output signal

Using change of variable method of integration with $t = \frac{\sqrt{2}x}{r_o}$, equation 3.16a can be expressed as:

$$I_{rd} = \frac{2Nq}{\sqrt{\pi}}\int_{0}^{\sqrt{2}\Delta s/r_o} e^{-t^2}dt$$

Equation 3.17: Output signal as a result of variable substitution integration technique

Using a mathematical table, equation 3.17 can easily be solved and is given as:

$$I_{rd} = \frac{2\sqrt{2}Nq\Delta s}{r_o\sqrt{\pi}}$$

Equation 3.17: Output signal in term of the optical beam's deflection Δs

Substitute for Δs in equation 3.17 gives:

$$I_{rd} = \frac{3\sqrt{2}NqL}{r_o l\sqrt{\pi}}\Delta z \qquad \text{(Amps)}$$

Equation 3.18: Output signal in term of the cantilever deflection Δz

Equation 3.18 shows that the resulting signal I_{rd} is linearly proportional to the vertical deflection of the cantilever, Δz. Equation 3.18 also indicates that the signal I_{rd} can be increased by decreasing r_o. However, decreasing the spot size of the laser and ultimately decreasing r_o is difficult due to diffraction. The sensitivity of the beam bounce detection technique has been reported to be $7.9\times10^{-6} nm/\sqrt{Hz}$ [35].

The performance of the beam bounce detection technique is limited by two types of noise.The first of which is the 1/f noise which is produced by the changing of low frequency in the output power of the laser source. The second type of noise is the shot noise. Shot noise exists due to the random arrival of photons at the detector. Other type of noise such as 60/50 electromagnetic interference can be eliminated by good design.

3.4 EFM CHARACTERIZATION

In this section, several criteria used to evaluate the performance of the EFM, will be discussed. These criteria include: spatial resolution, invasiveness and the voltage sensitivity of the instrument.

3.4.1 Spatial Resolution

One of the essential criteria in evaluating the quality performance of the EFM and other force microscopes is the spatial resolution. Spatial resolution is defined as the degree of accuracy that the measurement results represent the actual distribution of the quantity under investigation. More specifically, it represents an evaluation of the locality of the

measurement done by the microscope[38]. It is ideal to have a situation where by measurement is being done at an infinitely small point without the disturbance of its neighbouring points. However, this is not realizable in EFM and other force microscopes, where tips of finite dimensions are used. Therefore, the voltage measurement at a point on the circuit is, in actuality, the weighted average at that particular test point and at other points on the circuit.

By modelling the interaction between probe and circuit, the spatial resolution of an instrument can be estimated. In [27], an electrostatic force interaction between the tip and a GaAs substrate test structure was modelled. The tip-circuit geometry was modelled as a parallel plate capacitor with the tip as one plate and the circuit as the other. By the conformal mapping technique using the Schwartz-Cristoffel transformation along with a few assumptions, the spatial resolution was evaluated. Figure 3.11 a, b shows the tip-circuit spacing at different heights and its force density(force per effective area) in terms of the x-direction, respectively.

The calculation in figure 3.11b was determined with the potential difference between the tip and the circuit of 1V. This figure illustrates that as the tip moves further up from the circuit (i.e.: as the separation between the tip and the circuit increases), the electric force density decreases. In [27], the spatial resolution is defined as the diameter of the circle, where the force density decreases to 1/e from its maximum. For a tip-circuit separation of 100nm, the spatial resolution was found to be 300nm.

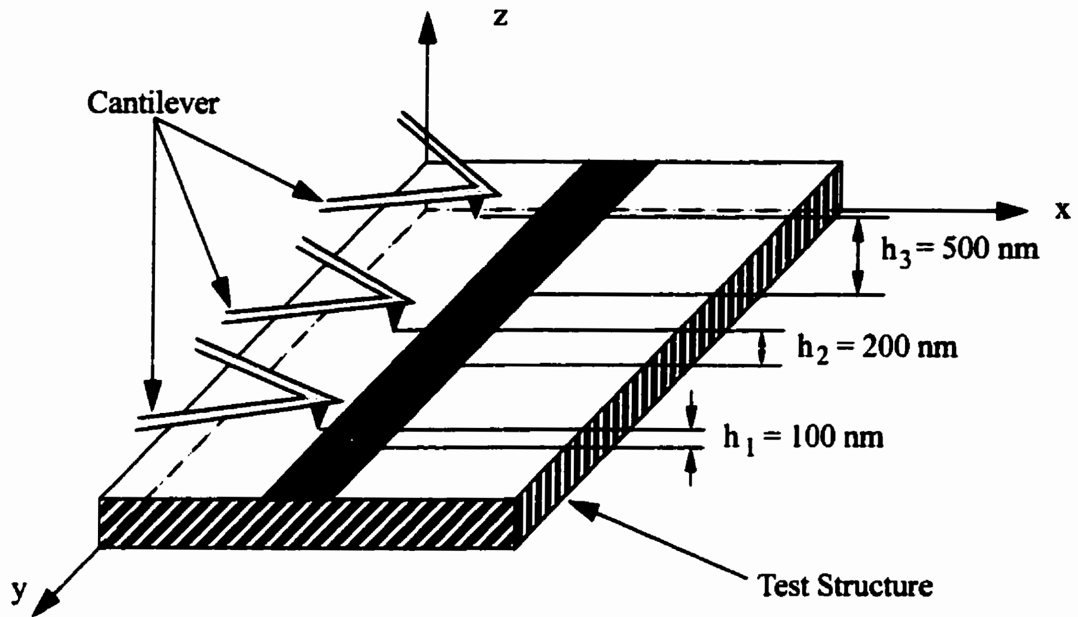


Figure 3.11a: Tip-circuit separation at different heights

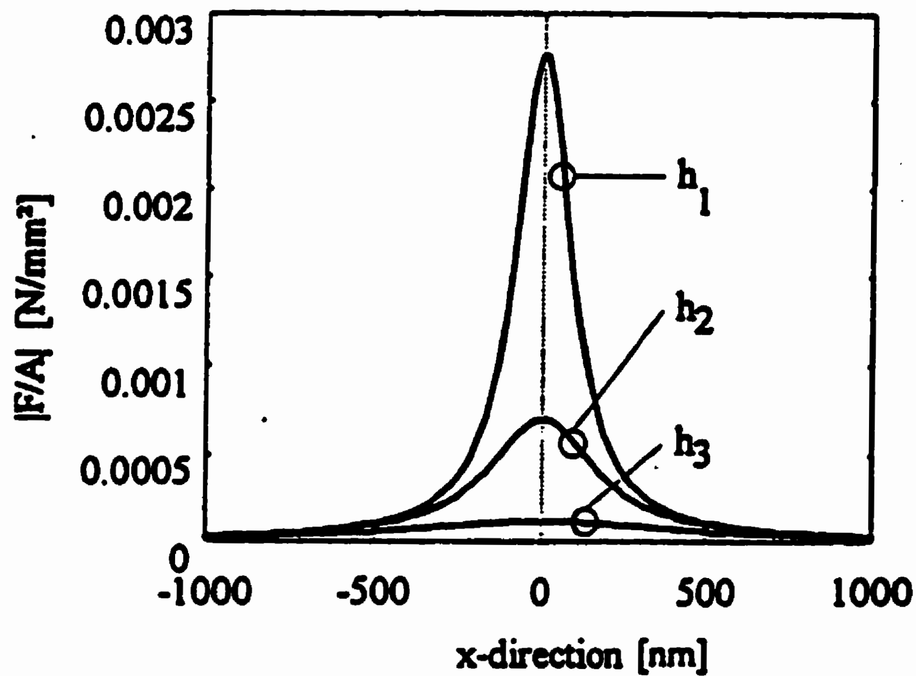


Figure 3.11b: The simulated force density (force per effective area) at different tip-circuit separation, h(100nm, 200nm, 500nm) versus x-direction in nm.[27]

3.4.2 Invasiveness

Invasiveness is defined as the amount of disturbance caused to the circuit's normal operation by the instrument. For different types of measurement techniques, the invasiveness criteria takes on different forms[20]. The invasiveness of the EFM instrument is considered in the form of signal distortion at the circuit's test point. This signal distortion is caused by the parasitic loading effect between the probe and the circuit. Since the EFM probe can be modelled as a *RLC* circuit, the instrument introduces disturbances of different types which causes a distortion in the signal. For example the resistive loading introduces shifts in dc bias and changes in circuit bias; inductive loading causes ringing effect while capacitive loading from the probe affects the timing measurements of the signal [dharman].

In EFM, the mutual coupling capacitance existing between the probe and the circuit's test point is a major contributing factor to the invasiveness of the instrument. The loading introduced by the coupling capacitance causes a deformation of the signal resulting in an increased delay. The coupling capacitance between the Si_3N_4 micro-machined probe and the circuit has been calculated [6]. For a typical Si_3N_4 probe positioned $1\mu m$ above an interconnect line of 3μm in width, the coupling capacitance is estimated at $235aF$. At $100GHz$, the parasitic shunt impedance ($1/2\pi fC$) introduced by the coupling capacitance is approximately $6.8K\Omega$. In applications where the resistive impedance of the circuit test point is less than $1K\Omega$, the parasitic impedance at $100GHz$ is considered as an open circuit and its effect can be neglected. In order to have a noticeable effect, the resistive impedance of the circuit's test point and the parasitic impedance must be comparable. Thus for applications with 50Ω systems, the frequency at which the EFM instrument

presents a noticeable distortion in the signal is 13.6 x 10^{12} Hz. Using the time constant definition of $\tau=2RC$, the time delay for a system with resistive impedance of 0.05 - 1 $K\Omega$ is ~ 0.024 - 0.47ps.

3.4.3 Voltage Sensitivity

Voltage sensitivity is simply stated as the smallest possible electrical potential that can be detected by a measurement instrument. As in any other instruments, noise in the system is a major limiting factor in the sensitivity of the EFM technique. In EFM, any signal arrived at the deflection sensor which is not induced by the electrostatic force acting between the probe and the circuit test point is interpreted as noise. To determine the sensitivity, an equivalent voltage corresponds to the probe deflection caused by the instrument's noise is required. In EFM, one possible source of noise is the beam bounce detection system where the dominant noise is the shot noise at the bi-cell photodetector. The noise level in the beam bounce detection system is approximately $1\times10^{-4} nm/\sqrt{Hz}$. Other sources of noise include the mechanical vibration of the probe/cantilever mechanism and electrical noise coupled to the probe from external sources. Noise stemming from the mechanical vibration can be minimized by placing the EFM instrument on top of the vibration isolated table. With proper shielding and better design, the electrical noise coupled to the probe from external sources can be neglected.

The most dominant noise in the EFM instrument is the thermal noise of the probe vibration which is generated by the equilibrium with the surrounding temperature. Taking into account the power spectral density of the thermal noise, the mean-square probe vibra-

tion written in term of the probe's frequency response is given by[38]:

$$\langle \Delta z_{th}^2 \rangle = \frac{4kk_B T_a B}{2\pi Q \omega_r} \int_0^{\infty} |G(\omega)|^2 d\omega$$

Equation 3.19: mean-square probe vibration cause by thermal noise

The parameter k_B in equation 3.19 is the Boltzman constant, B (*1/T*) is the measurement bandwidth and T_a represents the medium temperature. The root mean-square (rms) probe deflection at a particular frequency can be calculated by using the following:

$$\langle \Delta z_{th}^2(\omega) \rangle^{1/2} = \sqrt{\frac{4Qk_B T_a B}{k\omega_r}} \cdot \frac{(\omega_r/\omega)}{\sqrt{1 + Q^2(\omega/\omega_r - \omega_r/\omega)^2}}$$

Equation 3.20: root mean-square probe deflection as a function of frequency

Where the term $|G(\omega)|^2$ has been substitute by equation 3.6. From equation 3.20, the maximum probe vibration induced by the thermal noise occur at resonance and is given as follow

$$\langle \Delta z_{th}^2(\omega_r) \rangle^{1/2} = \sqrt{\frac{4Qk_B T_a B}{k\omega_r}}$$

Equation 3.21: root mean-square probe vibration at resonant frequency

For a typical micro-machined probe, ($Q = 32$, $k = 0.347 N/m$, $f_r = 12.275 kHz$) the deflection induced by the thermal noise is approximately 0.01 $nm / \sqrt{Hz}$. This number is 100 times larger than that of the shot noise in the beam bounce detection system proving that the thermal noise of the cantilever is the dominant noise in the EFM instrument. In a similar manner, the probe deflection due to the electrostatic force between the probe and the circuit test point is given as follows:

$$\langle \Delta z_F^2(\omega) \rangle^{1/2} = \langle F_z^2(\omega) \rangle^{1/2} \cdot \left(|G(\omega)| = \frac{(Q/k)\,(\omega_r/\omega)}{\sqrt{1 + Q^2 (\omega/\omega_r - \omega_r/\omega)^2}} \right)$$

Equation 3.22: probe vibration due to force between probe and circuit

$\langle F_z^2(\omega) \rangle$ in equation 3.22 represents the power spectral density of the force F_z in equation 3.2. The signal to noise ratio (SNR) can now be determined by dividing equation 3.22 by that of equation 3.20. Equating SNR to 1, the term $\langle F_z^2(\omega) \rangle^{1/2}$ can be expressed as

$$\langle F_z^2(\omega) \rangle^{1/2} = \sqrt{\frac{4kk_B T_a B}{Q\omega_r}}$$

Equation 3.23: power spectral density of electrostatic force between probe and circuit

From equation 3.2, the power spectral density in equation 3.23 can be written as

$$\langle F_z^2(\omega) \rangle^{1/2} = \frac{1}{2}\frac{\partial}{\partial z} C(x, y, z)\, \Delta V_{rms}(\omega)$$

Equation 3.24: power spectral density in term of the first derivative of the capacitance and ΔV_{rms}

where $\Delta V_{rms}(\omega)$ is the root mean square value of the probe-circuit electrical potential difference at the harmonic component ω. Using equation 3.24 and 3.23, the smallest possible voltage detectable by the EFM instrument can be calculated from the following:

$$\Delta V_{rms} = \frac{4}{\partial C(x, y, z)/\partial z} \cdot \sqrt{\frac{kk_B T_a B}{Q\omega_r}}$$

Equation 3.25: minimum voltage detectable by EFM

For a typical micromachined probe ($Q = 32$, $k = 0.347 N/m$, $f_r = 12.275 kHz$), the first derivative of the coupling capacitance C(x,y,z), for a probe positioned 1μm above the circuit's surface is approximated at $55 pF/m$ [6]. Substituting the obtained values into

equation 3.25 gives the minimum detectable voltage of approximately 2 $mV/\sqrt{Hz}$.

3.5 Existing Voltage Measurement Schemes Using EFM

Several voltage measurement methods have been developed using the EFM. In this section, a DC measurement method, which is used to measure the absolute voltage value, is presented. DC measurement method is operated using a nulling technique. To demonstrate the ability to measure high frequency signal, a heterodyne method is also discussed. For this project, measurement of an arbitrary periodic waveform using the pulse sampling technique is investigated. The theoretical and experimental results of this technique will be presented in chapter 5.

3.5.1 DC Measurement Technique

For DC measurement, the circuit voltage does not depend on the time and therefore can be written as $V_c(x,y)$. Thus, equation 3.2 representing the electrostatic force between the probe and the circuit point can be modified as follows:

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\,[v_p(t) - v_c(x,y) + \Delta\phi]^2$$

Equation 3.26: Electrostatic Force between probe tip and circuit point for dc measurement

The term $\Delta\phi$ is added to the electrostatic force equation to represent the dc offset and the contact potential differences. DC offset exists due to the surface charge [2,14] while the

contact potential differences [63] is caused by the difference in the probe and circuit's surface work function. From equation 3.26, determination of $V_c(x,y)$ through direct measurement of the electrostatic force requires the knowledge of the coupling capacitance C(x,y,z). To measure the coupling capacitance, accurate placement of the equipment is required thus making it a very difficult and unpleasant task. To decrease the complexity of the measuring technique, a nulling force method[40, 55] is used. A block diagram of the technique is shown in figure 3.12. The null-force technique is operated with a probe signal given by

$$v_p = A + K\cos(\omega_p t)$$

Equation 3.27: probe signal

The parameter A in equation 3.27 is a DC bias and K represents an adjustable parameter. The frequency component ω_p is chosen near the probe mechanical resonance frequency ω_r (i.e.: $\omega_p \approx \omega_r$). Substituting equation 3.27 into 3.26 and expanding the square term, the electrostatic force can be written as

$$\begin{aligned} F_z &= \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\left(A + K\cos(\omega_r t) - v_c(x,y) + \Delta\phi\right)^2 \\ &= \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\left\{\left[(A - v_c(x,y) + \Delta\phi)^2 + \frac{K^2}{2}\right]\right. \\ &\quad \left. + 2[A - v_c(x,y) + \Delta\phi]K\cos(\omega_r t) + \frac{K^2}{2}\cos(2\omega_r t)\right\} \end{aligned}$$

Equation 3.28: Electrostatic force equation

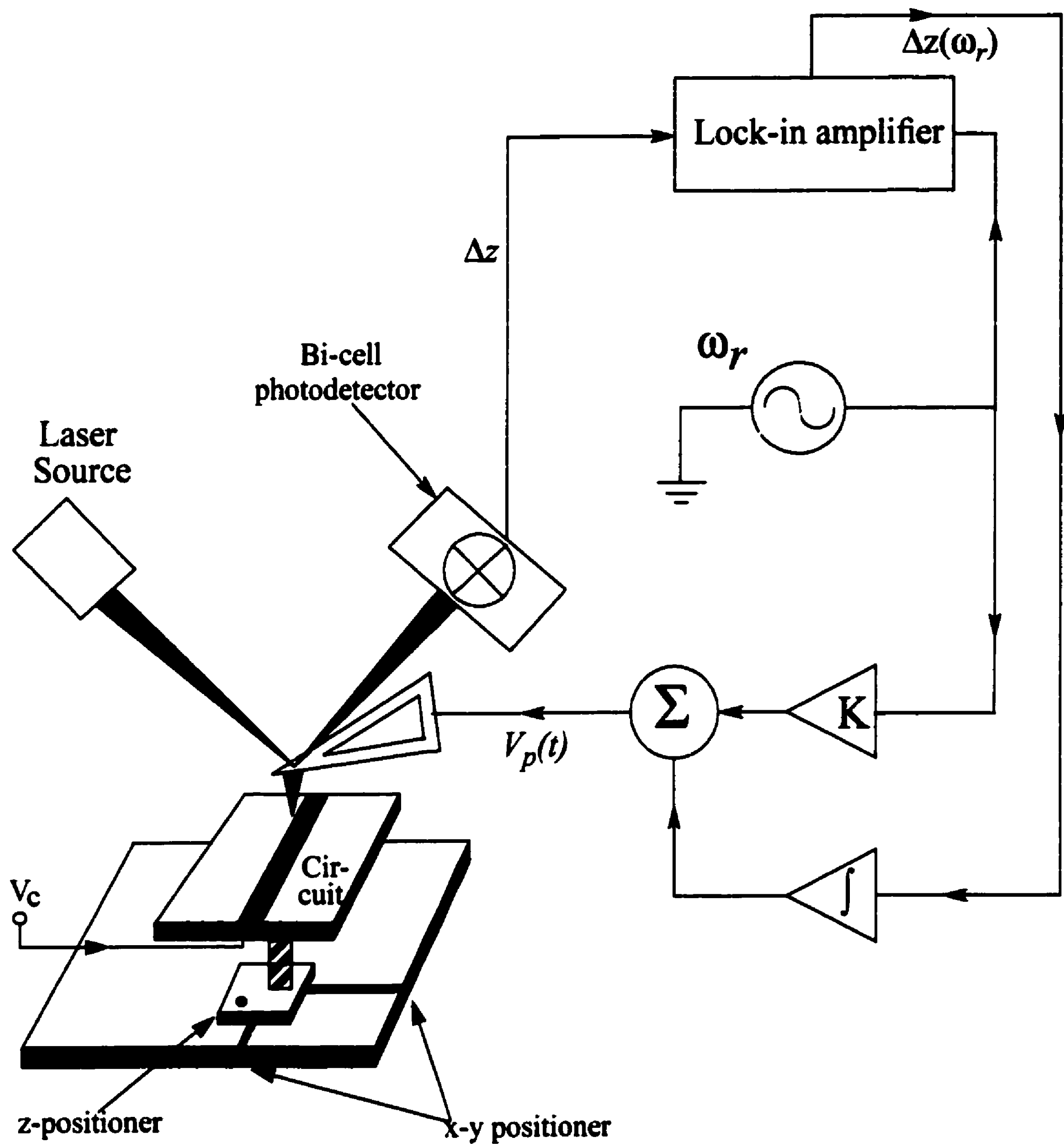


Figure 3.12: Block diagram of the null-force technique. The probe's tip is place as close to the circuit as possible. The deflection of the probe is detected using the beam bounce measurement system. The deflection is recorded by the lock-in amplifier which is reference to the probe signal frequency ω_p. The probe signal v_p is the summation between the ac component at $\omega_p \approx \omega_r$ and the integration of the output of the lock-in amplifier.

Equation 3.28 shows that the DC components as well as the components at ω_r and $2\omega_r$ will cause deflection in the probe cantilever. The electrostatic force component at $\omega_p \approx \omega_r$ is given by:

$$F_z\Big|_{\omega_p \approx \omega_r} = \frac{\partial}{\partial z} C(x, y, z)\ [A - v_c(x, y) + \Delta\phi]\ K\cos(\omega_r t)$$

Equation 3.29: Force component at $\omega_p \approx \omega_r$

Equation 3.29 suggests that nulling the force at the component $\omega_p \approx \omega_r$ by adjusting the dc bias parameter A, the term $v_c(x, y) + \Delta\phi$ can be determined without the knowledge of the coupling capacitance C(x,y,z). For a known value of $\Delta\phi$, the circuit potential can easily be extracted. By choosing ω_p to be close to the resonance frequency, the Q factor of the cantilever enhances, thus increasing the probe deflection. The probe cantilever deflection is given by

$$\Delta z\Big|_{\omega_p \approx \omega_r} \approx \frac{Q}{k}\frac{\partial}{\partial z} C(x, y, z)\ [A - v_c(x, y) + \Delta\phi]\ K\cos(\omega_r t)$$

Equation 3.30: Probe deflection at $\omega_p \approx \omega_r$

The result of the dc measurement technique can be seen in chapter 6 of [38]. Measurement over a 10μm wide transmission line, while applying potential was varied from -5V dc to +5V dc, was performed. The results shows that there is less than 10 mV difference between the applied and measured potential at +5V and a difference of 250mV at -5V [38].

3.5.2 High Frequency Vector Waveform Measurement Technique

The nulling force technique in the previous section is limited to measuring the dc voltage value. Thus, the null-force technique alone is unsuitable for measuring a high frequency sinusoidal signal. In this section a heterodyne electrostatic force technique will be presented. The heterodyne technique based on amplitude modulation is capable of accurate measurement of the amplitude and phase of high frequency signals. For a circuit under test driven at the frequency ω_0, the signal at a single test point on the circuit can be expressed as follows

$$v_c(x, y, t) = V_c \sin(\omega_0 t + \phi_c)$$

Equation 3.31 Circuit's signal driven at ω_0

Two type of modulations can be used to implement the heterodyne technique. These two methods will be presented next.

3.5.2.1 Sinusoidal Modulation

For sinusoidal modulation, the applied signal at the probe's tip is given by

$$v_p(t) = [A + K\cos(\omega_r t)] \sin(\omega_0 t + \phi_p)$$

Equation 3.32: Probe's signal for sinusoidal modulation

The parameter A, K, and ϕ_p in equation 3.32 are controllable by the user. Figure 3.13 shows the block diagram of the technique. Substituting equation 3.31 and 3.32 into 3.26, the force between the probe and the circuit is

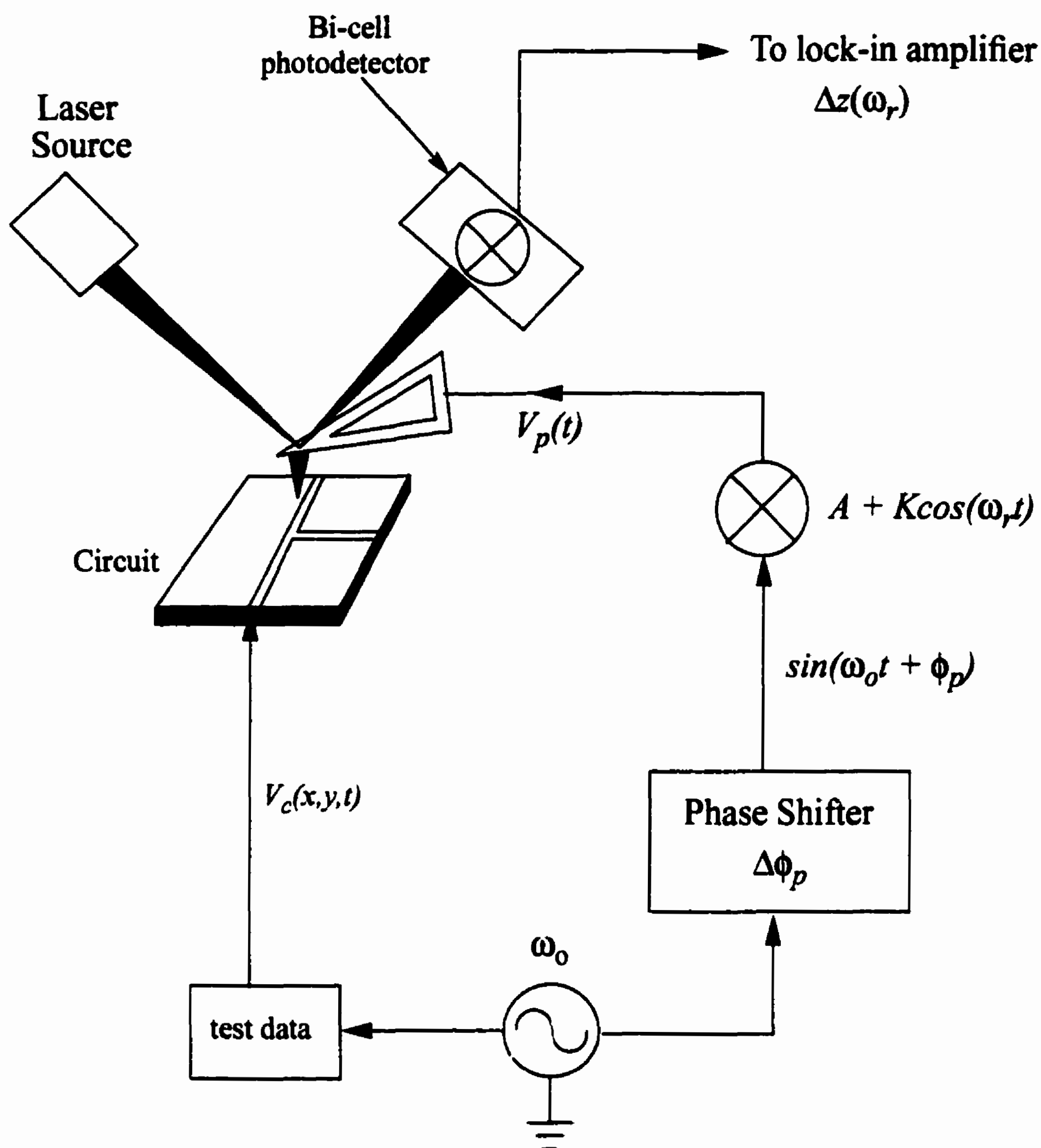


Figure 3.13: Block diagram of the heterodyne measurement technique. The technique is implemented to measure high frequency signal. A high frequency signal source is used to generate the circuit and probe signal. The phase shifter is used to adjust the phase applied at the probe. A sinusoidal signal is used as a modulation signal at the probe resonant frequency.

$$F_z = \frac{1}{2}\frac{\partial}{\partial z}C(x,y,z)\langle [A + K\cos(\omega_r t)]\sin(\omega_o t + \phi_p) - V_c\sin(\omega_o t + \phi_c) + \Delta\phi\rangle^2$$

Equation 3.33: Resulting force for heterodyne technique

When expanded, equation 3.33 contains the static force component as well as components at ω_r, $2\omega_r$, ω_0, $2\omega_0$, $\omega_0 \pm \omega_r$, $2\omega_0 \pm \omega_r$, and $2\omega_0 \pm 2\omega_r$. However the only component of interest is that at resonant frequency since it produces the maximum deflection. The force component at the probe's resonant frequency is

$$F_z(\omega = \omega_r) = \frac{1}{2}\frac{\partial C}{\partial z} \cdot K\cos(\omega_r t)\ [A - V_c\cos(\phi_p - \phi_c)]$$

Equation 3.34: Force component at probe resonant frequency

The corresponding probe deflection will be

$$\Delta z(\omega = \omega_r) = \frac{1}{2}\frac{\partial C}{\partial z} \cdot \frac{Q}{k} \cdot K\cos(\omega_r t)\ [A - V_c\cos(\phi_p - \phi_c)]$$

Equation 3.35: Cantilever deflection at resonant frequency

Equation 3.35 suggests that the probe deflection at resonant frequency will not be disturbed by the dc offsets since the term $\Delta\phi$ is not present. By controlling the parameter A and ϕ_p so that the force is nulled at resonant, the magnitude and phase of the circuit signal can be extracted. To determine an accurate value of the unknown circuit signal, let's look at a plot between the probe-circuit phase difference $(\phi_p - \phi_c)$ and $|\Delta z| \propto |A - V_c\cos(\phi_p - \phi_c)|$.

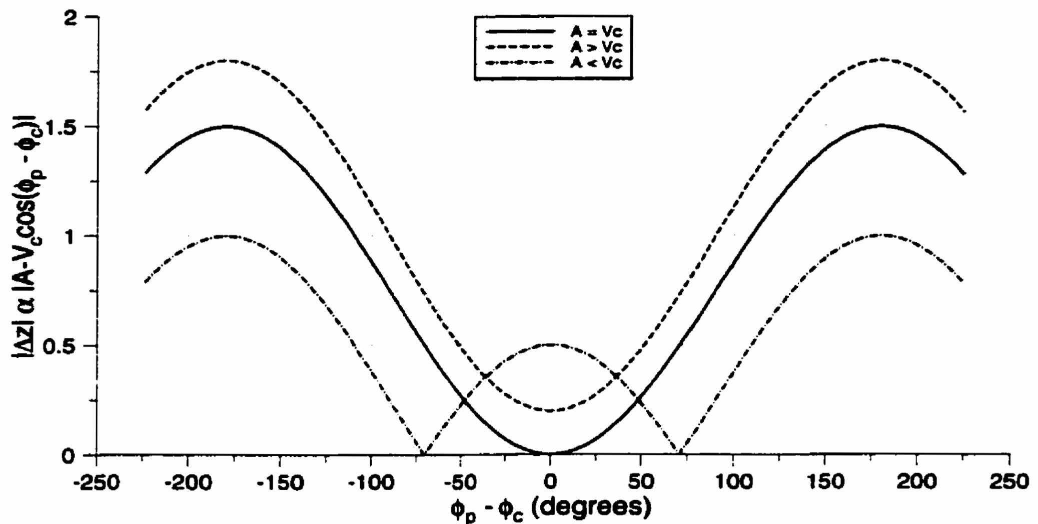


Figure 3.14: Relative cantilever deflection as a function of the probe-circuit phase difference for the case of $A = V_c$, $A > V_c$, and $A < V_c$.

Figure 3.14 shows that for $A > V_c$, the deflection is never nulled. For the case when $A = V_c$, the deflection is nulled when the phase difference is zero. However this is difficult to accomplish since the circuit value V_c is unknown to begin with. The third situation is when $A < V_c$, in this case the nulling point occurs at two different points. Figure 3.12 also shows that the phase difference is zero at the mean of the two null points when $A < V_c$.Thus by adjusting the probe phase to locate the two null points, the circuit signal phase is ultimately determined. The magnitude of the circuit signal can be found from the known phase.

3.5.2.2 Square Wave Modulation

At high frequency, sinusoidal modulation can be difficult to implement using simple electronics. Square wave modulation is easier and more feasible to implement at high frequency. The signal applied at the probe is

$$v_p(t) = [A + Ksqr(t)] \sin(\omega_0 t + \phi_p)$$

Equation 3.36: Probe signal for square wave modulation

The parameter A, K, and ϕ_p in equation 3.36 are controllable by the user. The fourier series representation for the signal *sqr(t)* is given as

$$sqr(t) = \frac{2}{\pi} \cdot \sum_{n=1}^{\infty} \frac{1}{n} \cdot \cos(n\omega_r t) \text{ , where n = odd number}$$

Equation 3.37: Fourier series representation of the signal *sqr(t)*

The resulting force when substituting equation 3.36 and 3.37 into 3.23 introduces the static force component as well as component at ω_0, $2\omega_0$, $n\omega_r$, and $2\omega_0 \pm n\omega_r$, where n = odd number. The maximum deflection occurs at ω_r and is given as

$$\Delta z(\omega = \omega_r) = \frac{\partial C}{\partial z} \cdot \frac{Q}{k} \cdot K \cdot \frac{1}{\pi} [A - V_c \cos(\phi_p - \phi_c)] \cos(\omega_r t)$$

Equation 3.38: Cantilever deflection at resonant frequency for square wave modulation

Equation 3.38 is the same as equation 3.35 except for the 2/π factor. The procedure in extracting the unknown circuit signal is the same as that of the sinusoidal modulation.

Experimental results of the heterodyne technique using the sinusoidal modulation can be found in [32]. Vector waveform measurement of TI-LNA at 1GHz using the EFM and contact probe are compared. The results are in very good agreement with each other.

CHAPTER 4.

Narrow Pulse Generation Techniques

A number of techniques are available for generating narrow-width pulses. This chapter will discuss 3 of those techniques in detail. First, non-linear transmission line method will be presented. Next, narrow pulse generation using AND-Gate is discussed. Finally, impulse generator using the Step recovery diode is evaluated.

4.1 NON-LINEAR TRANSMISSION LINE (NLTL)

4.1.1 Theory

4.1.1.1 Ideal Transmission Line

To better understand the operating principle behind the non-linear transmission line, we first need to be familiar with some of the basic theories of an ideal transmission line. Transmission lines are used to transmit electrical signals between two points in space. A section of a uniform transmission line can be modelled by the circuit representation in figure 4.1. The circuit consists of a series inductance and resistance as well as shunt capacitance and conductance. For this project, we'll be mainly concerned with the wave(phase)

velocity as it travels along the line, the characteristic impedance (Z_o) of the t-line, and the reflection coefficient. A detailed derivation of the transmission line characteristic can be seen in chapter 9 of [9].

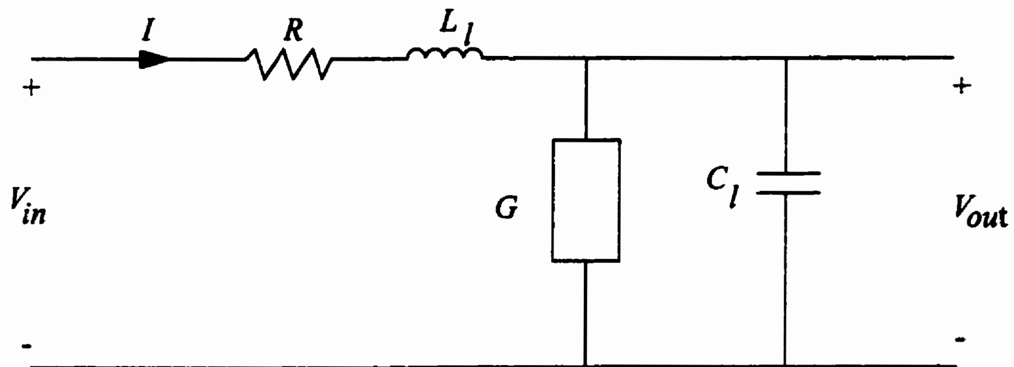


Figure 4.1: Lumped Elements Modelled of the Transmission Line

The time it take for the wave to travel from one end of the transmission line to the other depends on the speed at which it propagates. This speed is referred to as the phase velocity and is given as follows:

$$\vartheta = \frac{1}{\sqrt{L_l C_l}}$$

Equation 4.1: Transmission Line Phase Velocity

For a lossy transmission line, the phase velocity depends on the frequency. This means that the different frequency components of a wave propagate along the line with different velocity resulting in a distorted signal at the end. This phenomenon is referred to as dispersion. It is desirable in this project to have a transmission line that possesses a lossless characteristic.

The characteristic impedance of a transmission line is defined as the ratio of V to I

for the wave travelling on that line. The characteristic impedance, Z_o, of a lossy transmission line is a constant and is expressed as follows:

$$Z_o \approx \sqrt{\frac{R + j\omega L_l}{G + j\omega C_l}}$$

Equation 4.2: Characteristic Impedance of a Lossy Transmission Line

For a low-loss line, the Resistance and Conductance elements can be neglected. Therefore Equation 4.2 can be written as follows:

$$Z_o \approx \sqrt{\frac{L_l}{C_l}}$$

Equation 4.3: Characteristic Impedance of a Low-Loss Transmission Line

In most cases, it is desirable to have the amplitude of a signal at the output of the transmission line be identical to the input. The loss in the signal's amplitude depends on the load terminated at the end of the line. Figure 4.2 illustrates a transmission line connected to a source and terminated with a load.

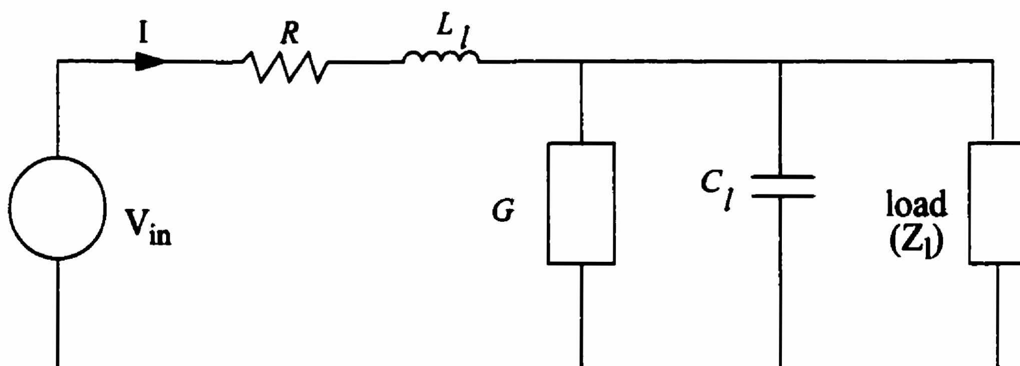


Figure 4.2: Lumped element modelled of the transmission line connected to a source and terminated with a load

A reflection coefficient is used to measure the loss in signal's amplitude. The reflection coefficient is a dimensionless constant and can be expressed as follows:

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o}$$

Equation 4.4: Reflection Coefficient

According to equation 4.4, to achieve a zero reflection (i.e.: the amplitude of the output signal is equal to the amplitude of the input signal) the load impedance must equal the characteristic impedance of the line. Further more, reflection at the output terminal of the transmission line may result in an undesirable output signal.

4.1.1.2 Diode Junction Capacitance

A junction diode is essentially a pn junction. It is made up of a p-type silicon which is denoted as the anode and an n-type silicon as cathode. Figure 4.3 shows the diode's physical structure and symbol.

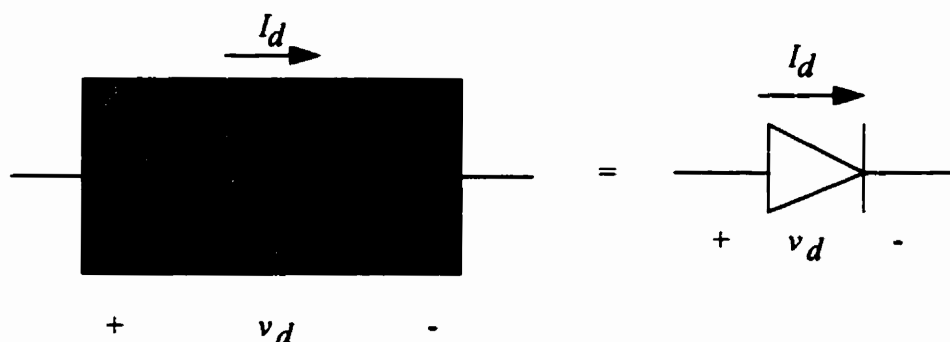


Figure 4.3: Diode physical structure and symbol [23].

$$I_d = I_s\left(e^{\frac{v_D}{V_T}} - 1\right)$$

Equation 4.5: Diode Equation

Equation 4.5 [23] represents the diode equation where $V_T = kT/q$ is the thermal voltage. I_s is the reverse saturation current.

For a reverse bias voltage case as shown in figure 4.4, when v_d is less than zero, the diode current $I_d = -I_s$. As the reverse bias voltage increases, the depletion region forms at the junction increases resulting in an increase amount of charge stored in this region. Since charge is directly related to capacitance, the diode in this mode behaves as a parallel plate capacitor.

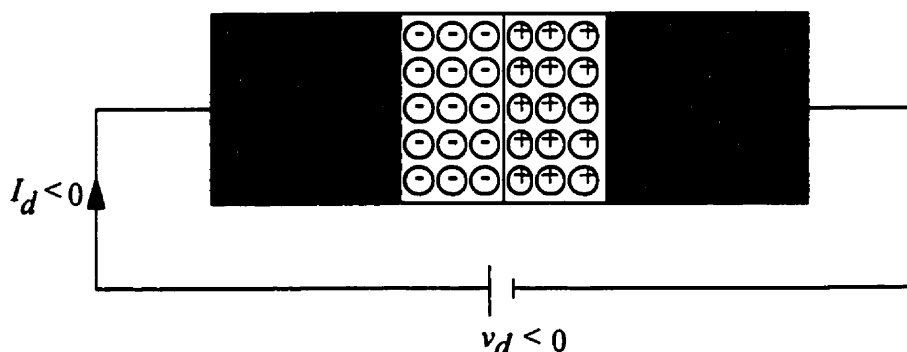


Figure 4.4: Junction diode in reverse bias mode [23]

Figure 4.4 also shows that as the depletion region increases, the separation between the *p*-type and *n*-type expands as well. Since the diode behave as a parallel plate capacitor in the reverse bias voltage mode, the capacitance of the structure is therefore inversely proportional to the separation distance between the *p*-type and *n*-type.

In summary, when the reverse bias voltage increases(becomes more negative), the depletion region expands less (ie: changes in depletion charges are smaller). Since the incremental capacitance is defined as, change in charge divided by change in voltage, thus the capacitance decreases. A Junction especially designed for operation in this manner is called a varactor diode. The junction capacitance can be calculated by using the expression given in equation 4.6 [45].

$$C_D(v_D) = \frac{C_{j0}}{\left(1 - \frac{v_D}{V_{j0}}\right)^m}$$

Equation 4.6: Junction Capacitance

In the above equation, V_{j0} is the built-in barrier potential, C_{j0} is the zero-voltage capacitance, and m is a constant called the grading coefficient. The value of V_{j0} and C_{j0} varies for different type of material. The value for the grading coefficient depends on the doping concentration. For the junction with abrupt changes in doping concentration, m is approximately 0.5. The grading coefficient is around 0.33 for junction with gradual changes in doping concentration. For this project, the values of V_{j0}, C_{j0}, and m are specified by Canadian Microelectronic Corporation (CMC). This will be discussed in detail in the Design Parameter section.

4.1.1.3 Non-Linear Transmission Line

The main idea behind the non-linear transmission line is to obtain an output signal that is not a scaled, but rather a distorted and compressed version of the input signal. To achieve this purpose, varactor diodes are placed periodically in shunt with the end of the

transmission line. Figure 4.5 shows a single section structure of a non-linear transmission line.

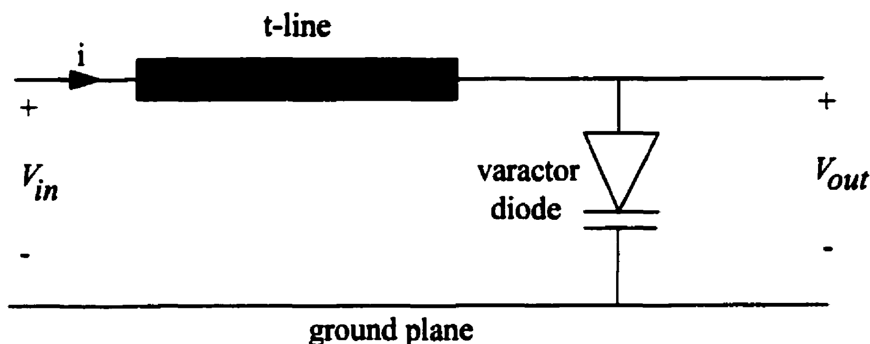


Figure 4.5: structure of a single NLTL section

The varactor diode is placed such that the anode and cathode are connected to the signal line and ground plane, respectively. A number of such sections are connected together to produce a desirable output waveform. As mentioned earlier, the varactor diodes behave as a voltage dependent capacitor, therefore the above NLTL section can be modelled as follow:

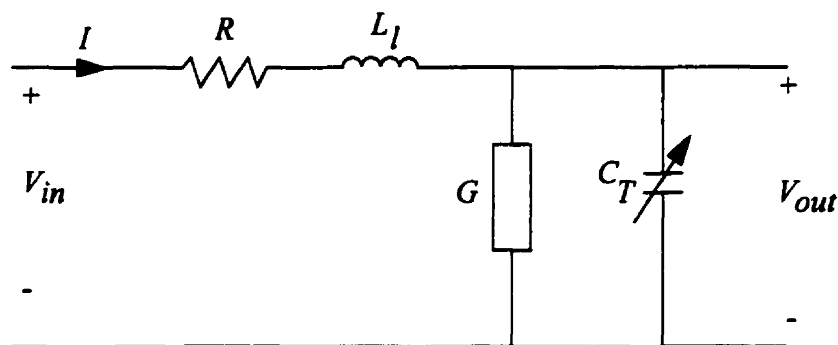


Figure 4.6: Lumped Elements Representation of a single NLTL section

The capacitance component C_T in figure 4.6 represents the sum of the line capacitance (C_l) and the diode junction capacitance (C_D). The model in figure 4.6 changes the phase velocity of the line, given in equation 4.1, as follows:

$$\vartheta(V) = \frac{1}{\sqrt{L_l \cdot C_T(V)}}$$

Equation 4.7: Voltage Dependent Phase Velocity

The total capacitance decreases as the voltage becomes more negative, therefore, according to equation 4.7, the phase velocity slows down when the voltage becomes more positive.

To have a better understanding of how the NLTL works, lets look at an example with a 1 GHz sinusoidal input shows in figure 4.7.

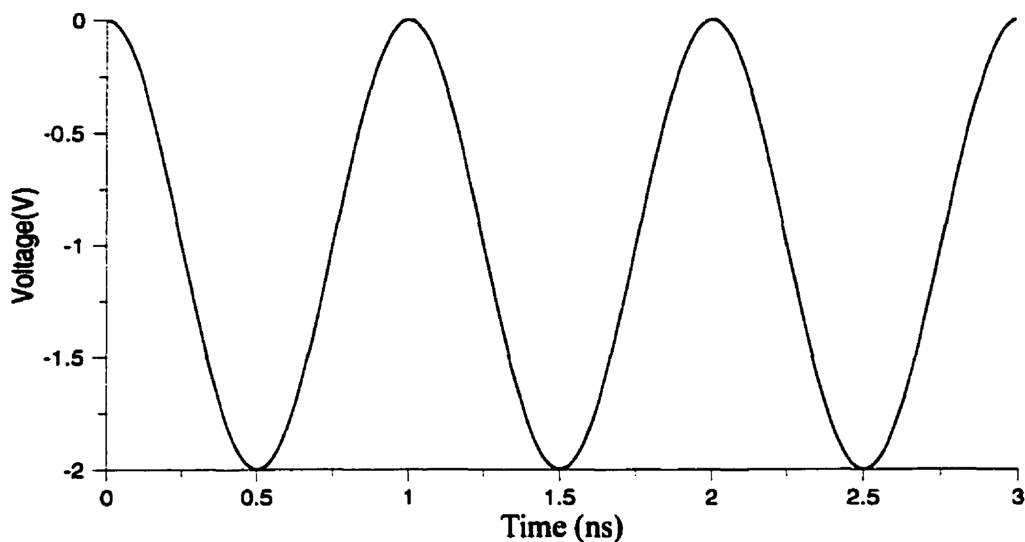


Figure 4.7: 1 GHz Sinusoidal Input Waveform

According to equation 4.7, the components of the input waveform with larger amplitude propagates slower than those with lower amplitude. This means that the component with an amplitude of 0V will take longer to reach the end of the transmission line than the component of 2V in amplitude. The resulting output is shown in figure 4.8

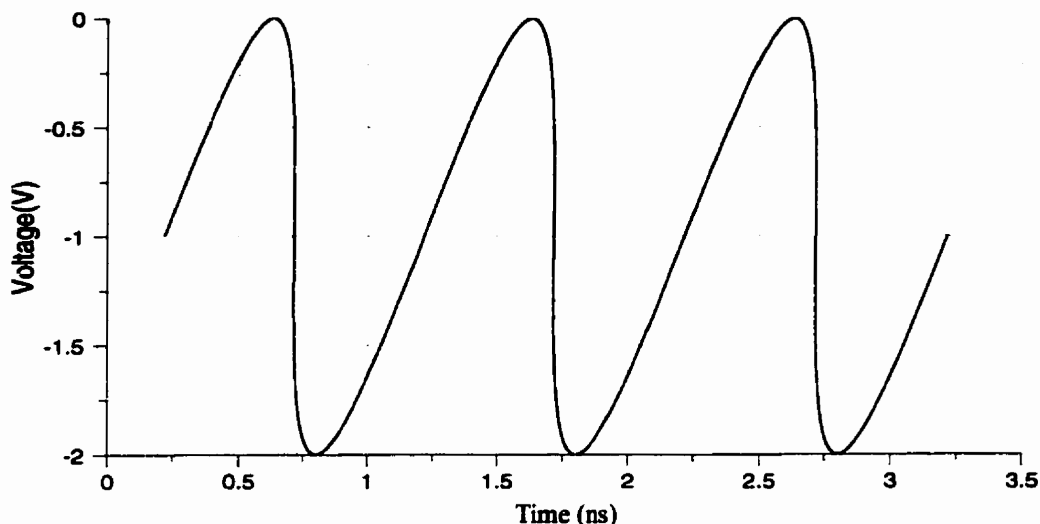


Figure 4.8: Output waveform of NLTL

Figure 4.8 shows that the output is a compressed version of the input sinusoid signal. The rise time of the sinusoid increases while the fall time decreases. The 0-100% fall time of the output signal is approximately 100 ps.The input signal has a fall time of 500 ps which means that the compression time for this example is 400 ps.The amount of compression in the falling edge of the output signal can be approximated by the following equation[42]:

$$\Delta T \approx d\left[\sqrt{L_l^{'} \cdot \left(C_l^{'} + \frac{n \cdot C_{j0}(V_u)}{d}\right)} - \sqrt{L_l^{'} \cdot \left(C_l^{'} + \frac{n \cdot C_{j0}(V_l)}{d}\right)}\right]$$

Equation 4.8: Approximation of Compression Amount

V_u and V_l in equation 4.8 correspond to the upper and lower limits of the input voltage. d is the length of the transmission line, and n represents the number of diodes. $L_l^{'}$ and $C_l^{'}$ denoted the line inductance per unit and capacitance per unit, respectively.

Narrow pulses are obtained by connecting the output of the transmission line to a

differentiator. The following figure is a result of taking the derivative of the waveform in figure 4.8.

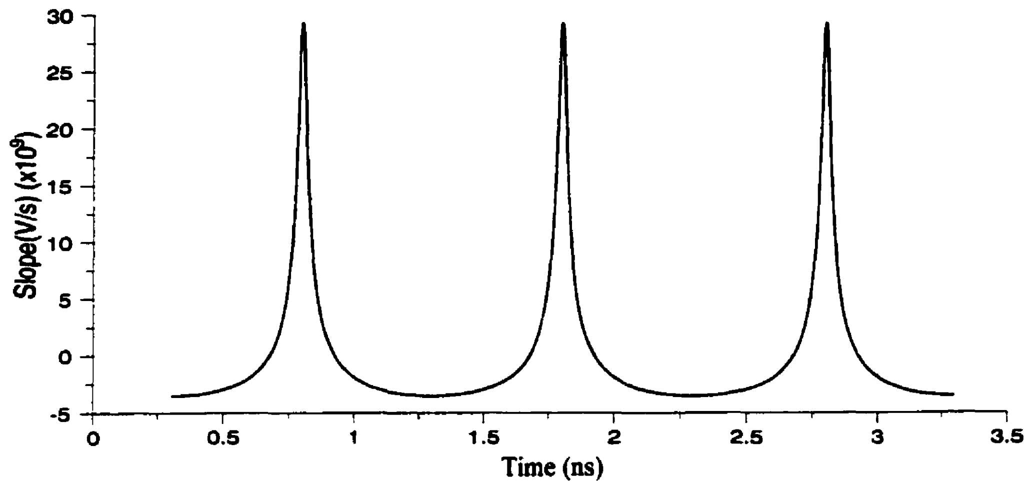


Figure 4.9: Derivative of the Output Waveform

4.1.1.4 Fall Time Limiting Factors

There are several factors contribute to the less than desirable edge rate of the output signal in the non-linear transmission line. One of which is the cut-off frequency. There are two types of cut-off frequency to take notice of; the first of which is the diode's cut-off frequency, the other being the cut-off frequency of the line section between the two diodes. From equation 4.7, one can make an assumption that the larger the capacitance, the faster the fall time will be obtained. This is not entirely true due to the low-pass filter behaviour of the NLTL model. The low pass filter eliminates the high frequency components that are needed to generate a fast edge rate. This means that the fall time of the output signal is controlled by the total capacitance C_T. The best way to describe the low-pass filter constraint is by an example. Figure 4.10 gives a sawtooth waveform with a period of

1 ns(1 GHz).

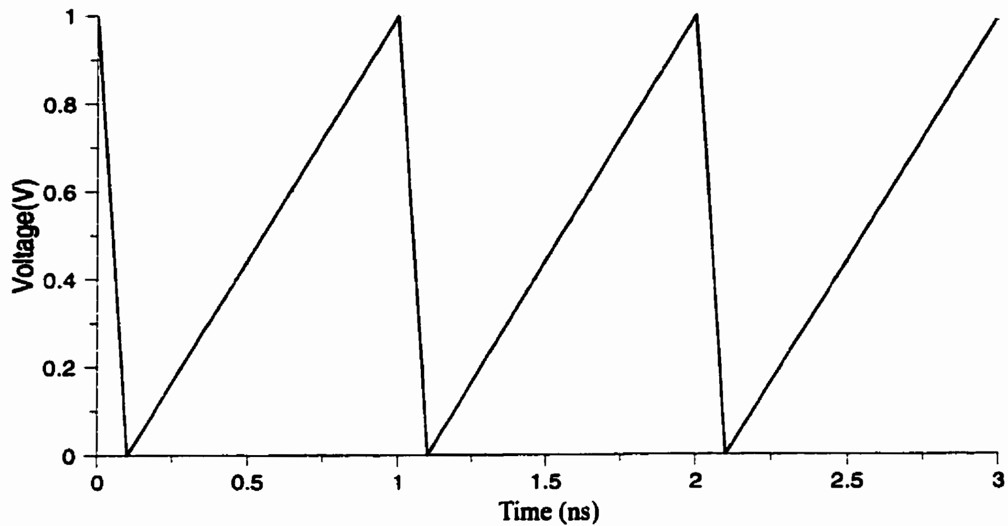


Figure 4.10: Sawtooth Waveform

The sawtooth waveform is an ideal output of the NLTL. The derivative of this the sawtooth waveform gives an ideal narrow pulse. This pulse is shown in figure 4.11

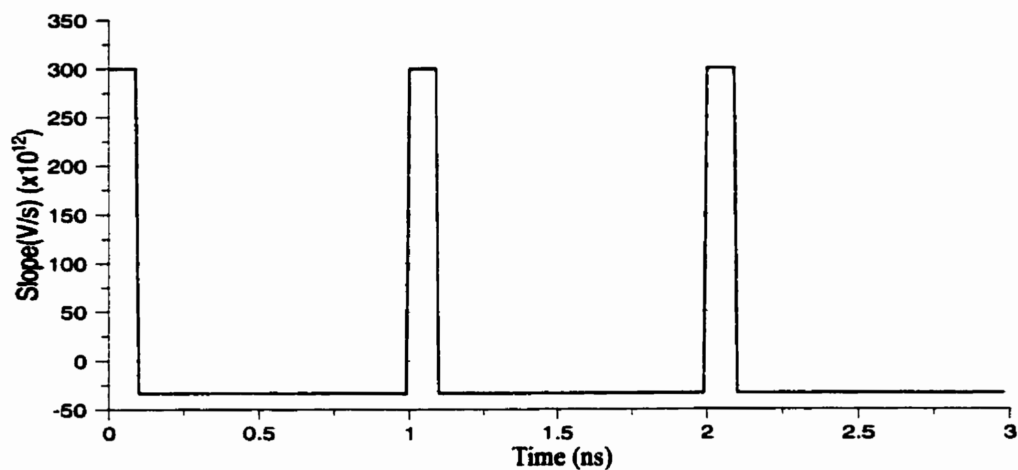


Figure 4.11: Derivative of the sawtooth waveform

Let say that the sawtooth waveform is an input signal to a low pass filter which has

a cut-off frequency of 5 GHz. This means that the low pass filter eliminates all but the first 5 harmonics of the input signal. The output of this low pass filter and its derivative are shown in figure 4.12 and 4.13, respectively.

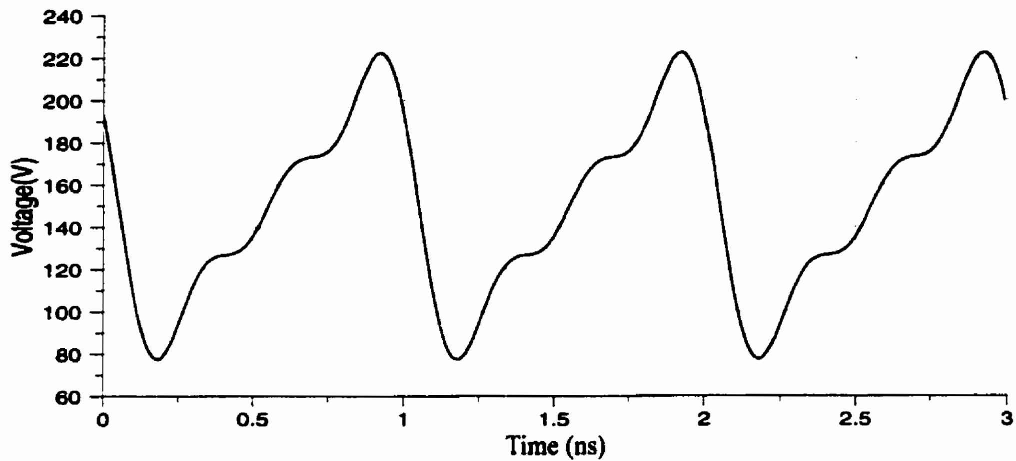


Figure 4.12: waveform at the output of the low pass filter

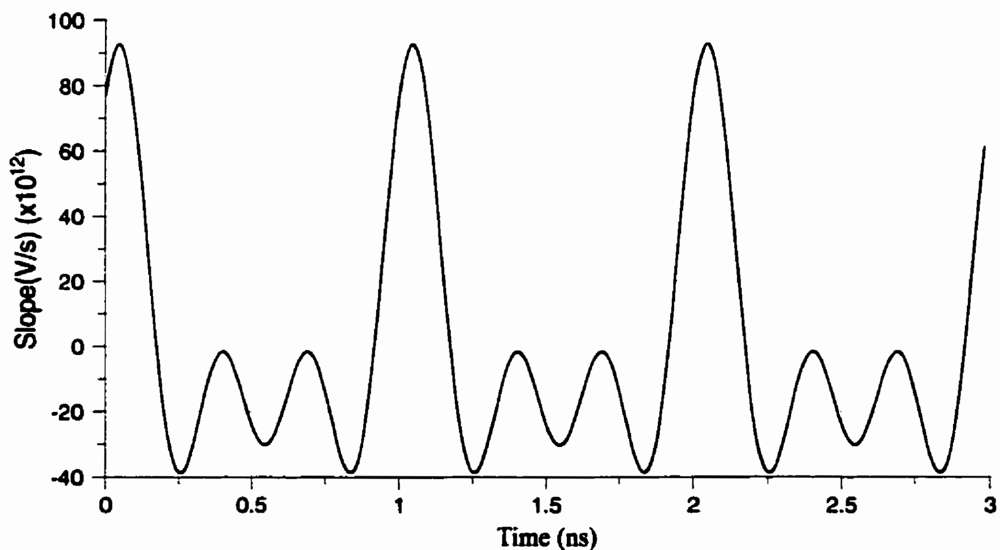


Figure 4.13: Derivative of the waveform at the output of the low pass filter

Figure 4.12 shows the effect of eliminating the high frequencies components. The fast edge rate of the sawtooth waveform becomes more rounded resulting in less desirable pulses.

Other factors in limiting the fast edge rate include dispersion and mismatch between the line and the load. Dispersion smooths out the edges of the wave as it travels along the line. Mismatch between the line and the load creates unwanted reflection which can lead to deformation of the output signal.

4.1.2 DESIGN PARAMETERS

4.1.2.1 Co-Planar Waveguide Transmission Line Design

A co-planar waveguide transmission line model [22] was chosen as the interconnect line with the varactor diodes. The line model is shown in figure 4.14. In this model, *s* is the centre conductor's width. *w* represents the gap separating the ground plane and the centre conductor. *l* is the length of the transmission line.

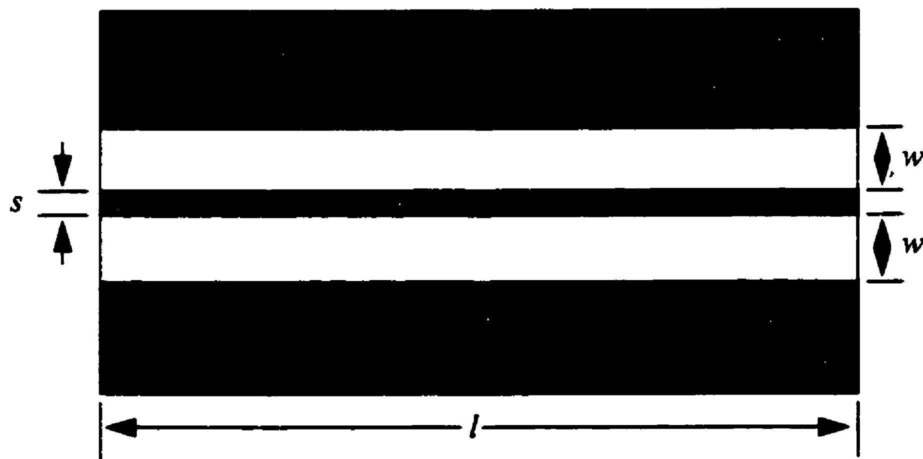


Figure 4.14: Top View of the Co-Planar Waveguide Transmission line structure

The characteristic impedance of the co-planar waveguide transmission line is given as follows[16]:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \cdot \frac{K'(k)}{K(k)}$$

where,

$$\frac{K'(k)}{K(k)} = \frac{\pi}{\ln\left[2 \cdot \frac{1+\sqrt[4]{1-k^2}}{1-\sqrt[4]{1-k^2}}\right]}$$

Equation 4.9: Characteristic Impedance of Co-Planar Waveguide Line

$\varepsilon_{re} = (\varepsilon_r + \varepsilon_{air})/2$ is the average dielectric constant. ε_r and ε_{air} represent the dielectric constants of the material and air(ε=1), respectively. For this project, GaAs which has a dielectric constant of 13.1, was chosen to be the line material. The variable *k* in equation 4.9 is the CPW design parameter. *k* is related to *s* and *w* by: $k=(s)/(s+2w)$. The characteristic impedance is plotted against *k* in figure 4.15.

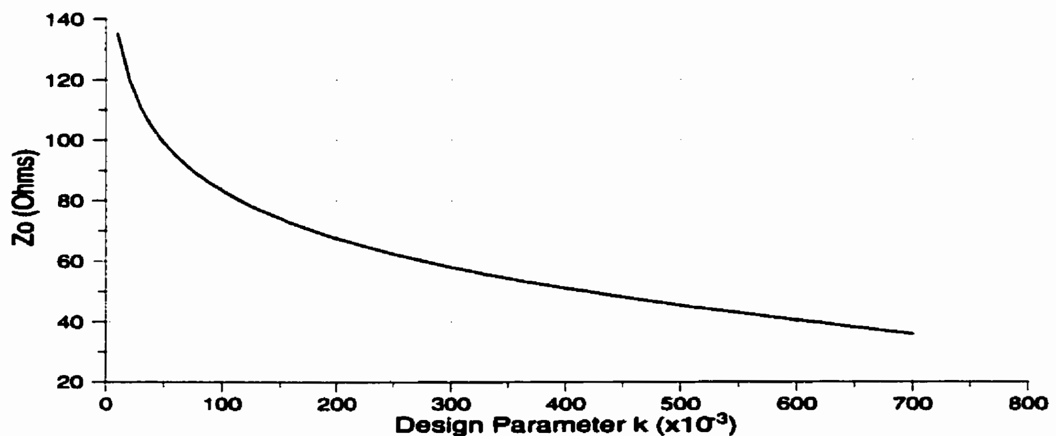


Figure 4.15: Zo of CPW vs. k

In the final non-linear transmission line design for this project, s, w, and l were chosen to be 15 μm, 31 μm and 100 μm, respectively. From the above relation, k=0.195 gives a characteristic impedance of the line to be 68 Ohms. The phase velocity can be calculated from the known average dielectric constant and the speed of wave travelling in free space. The phase velocity of the GaAs transmission line was calculated to be 1.13e8 m/s. Combining equation 4.1 and 4.3, the per unit inductance and capacitance of the t-line can be calculated as follow:

$$C_l' = \frac{1}{Z_o \vartheta} \quad \text{and} \quad L_l' = \frac{Z_o}{\vartheta}$$

Equation 4.10: Per Unit Capacitance and Inductance of the Line

The values of C_l' and L_l' for the final design were 130.16 pF/m and 601.84 nH/m, respectively. Since GaAs technology was chosen for the t-line, the characteristics of the diode given in this technology was used for this project. The diode has a zero bias voltage, V_{j0}, of 0.8V. The zero-bias junction capacitance of the diode, C_{j0}, is specified as $5.878 \times 10^{-15} F$ and m=1.248 represents the grading coefficient of the diode. In this project, 30 such diodes were constructed in parallel to increase the total capacitance and thus increase the amount of compression of the non-linear transmission line.

4.1.3 Evaluation and Construction of the Design NLTL

In this section, the performance of the NLTL is evaluated through the simulation and theoretical calculation. The fabrication process will also be presented.

4.1.3.1 Simulation and Calculation

Cadence version 9504(software simulation tool) was used to perform the schematic simulation of the non-linear transmission line. As mention in section 4.1.1.4, the most dominant factor in limiting the fast edge rate is the cut-off frequency. The diode cut-off frequency is given by[4]

$$f_{cd} = \frac{1}{2 \cdot \pi \cdot R_d(V) \cdot C_d(V)}$$

Equation 4.11: diode cut-off frequency

Using the parameters specified for the diode, the cut-off frequency is estimated at 300GHz. For a diode with high junction capacitance, the cut-off frequency is lower thus limiting the operating frequency of the non-linear transmission line. The cut-off frequency of the line section between two diodes is given as[4]

$$f_{cl} = \frac{1}{\pi \cdot \sqrt{L_l[C_l + C_d(V)]}}$$

Equation 4.12: cut-off frequency of the line section between two diodes

where L_l and C_l are the line inductance and capacitance respectively. For the prototype design, the line cut-off frequency is approximated at 298GHz. As the section of the line gets larger the cut-off frequency decreases. As an example, let d = 5.65mm (τ=50ps) instead of 100μm used in the prototype NLTL design. Using equation 4.12, the cut-frequency is calculated to be 6.366GHz. This cut-off frequency will definitely have an affect when an edge rate of 50ps is desired. Simulation of the line at this cut-off frequency was also performed. The simulated circuit is shown in figure 4.16.

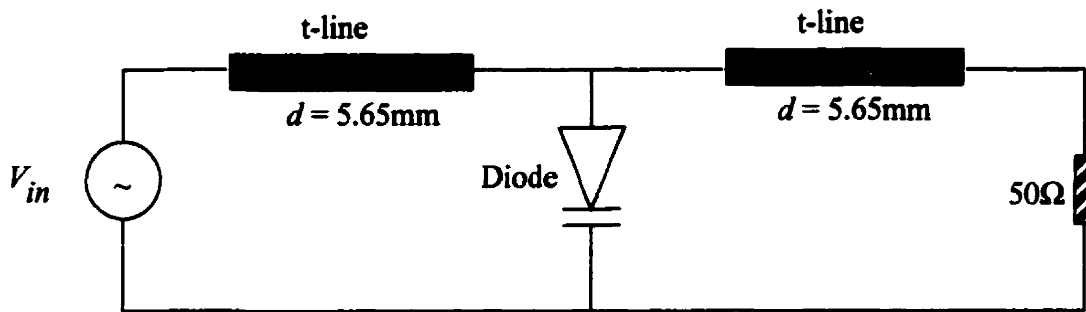


Figure 4.16: circuit used to simulate the cut-off frequency of the line

The circuit consists of a sinusoidal source and a 50 Ohms terminating load. A diode is located between the two linear transmission lines. The frequency, offset and amplitude of the input voltage V_{in} are 1GHz, -1V, and 1V respectively. The frequency response of a single non-linear transmission line section is shown in figure 4.17

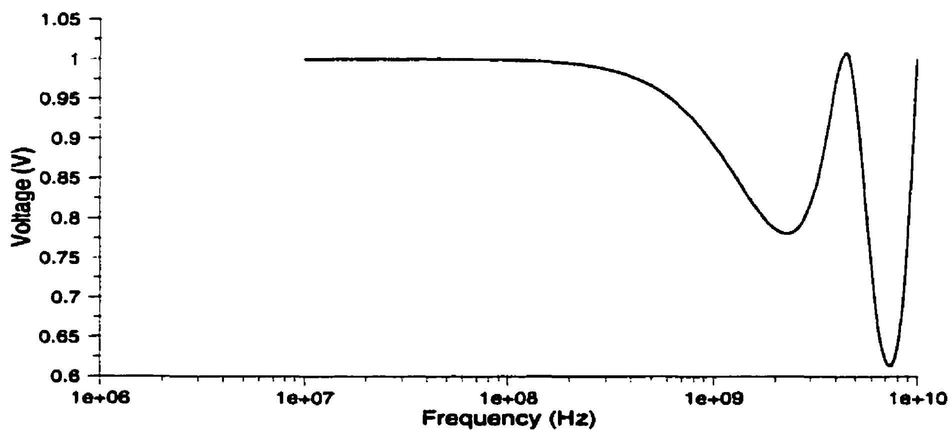


Figure 4.17: Frequency response of a single line section

The cut-off frequency is simulated to be 6.166GHz. This value is in close agreement with the calculated one.

Due to non-convergence error when using h-spice in Cadence 9504, simulations for the prototype design (i.e.: for transmission line section of 100μm long) were not able to perform. Thus equations will be used to predict the output signal of the prototype design. Simulations for longer transmission line sections were able to be obtained without encountering the non-convergence error. Therefore, to increase the validation of the calculated values, simulation results for d = 5.65mm (τ=50ps) will be compared with the calculated values at the same length. Figure 4.18 shows the comparison between the simulated and the calculated amount of compression for 10 nltl sections with transmission line length of 5.65mm.

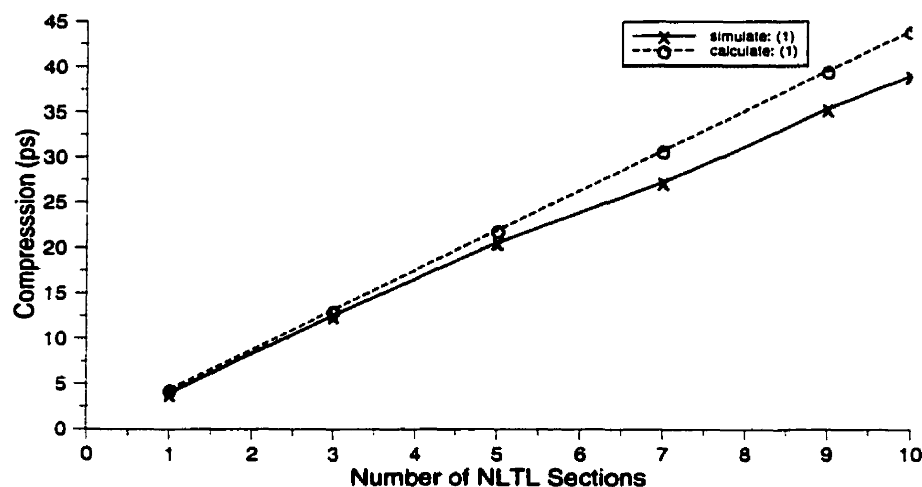


Figure 4.18: comparison between the simulated and calculated compression time

The average compression for the simulated results is 3.9ps while the calculated average gives 4.4ps. This is predictable since the calculated results do not take into account dispersion and mismatch. Figure 4.18 shows that as the signal travels further along the NLTL, dispersion and mismatch have a greater affect on the amount of compres-

sion. Thus the difference in the amount of compression between the calculated and simulated results increases with increasing t-line length. For the prototype design where the length of the line are much shorter, dispersion will have much less effect to the output signal. Using equation 4.8, the amount of compression for the prototype design (d = 100μm with 142 sections) with a 1GHz input sinusoidal signal, is predicted to be 233ps.

To further understand the behaviour of the NLTL, simulations for 40 NLTL sections were performed for input signals with frequency ranging from 720MHz to 1.4GHz with d = 5.65mm for each section. The falltime and compression is plotted against the period of the input signal in figure 4.19. As expected, the falltime increases with increasing period. The compression remains fairly constant at around 116ps.

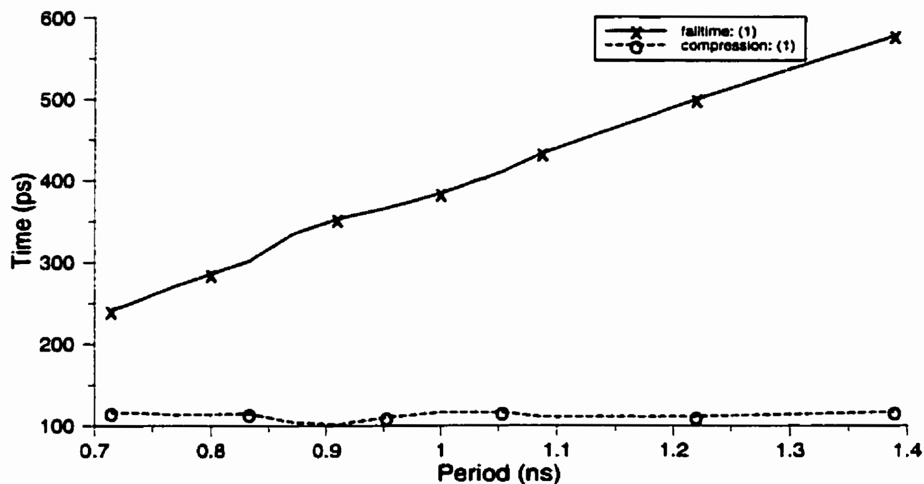


Figure 4.19: Simulation results of the falltime and compression of 40 nltl sections with d=5.65mm for input signals ranging between 720MHz to 1.4GHz.

4.1.3.2 Construction

Once the dimensions are known, the layout tool available in cadence 9504 was used to construct the circuit. The prototype NLTL design is a combination of 142 nltl sections. A photograph of the design is shown in figure 4.20a. Close-ups of the circuit are also shown in figure 4.20 b and c. A full layout view of the circuit can be seen in the Appendix. The layout of the design was sent to Canadian Microelectronic Corporation (CMC) for fabrication. An area of 2000μm by 2000μm was granted by CMC for this non-linear transmission line design. To accommodate the available space given while requiring a desired output, an s-like shape was used to layout the design. CMC uses the information specified in the layout to fabricate an IC version of the design. Bond wires are used to connect the IC chip to large pins for easier connection when testing is desired. However, bond wires introduce mismatch which lead to attenuation of the signal.

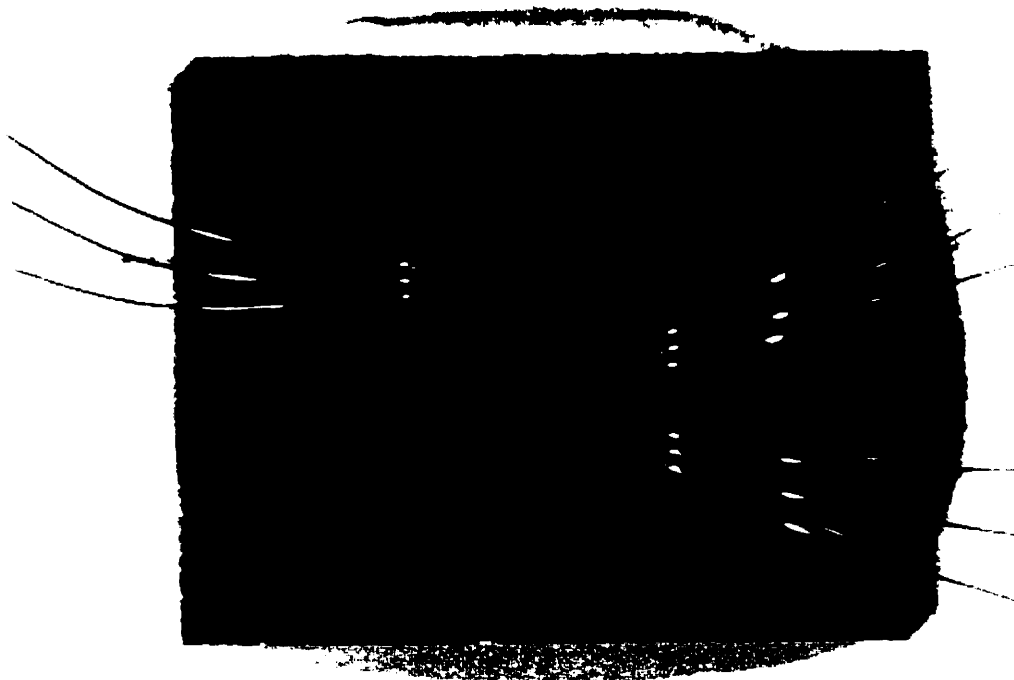


Figure 4.20a: Photograph of the nltl chip

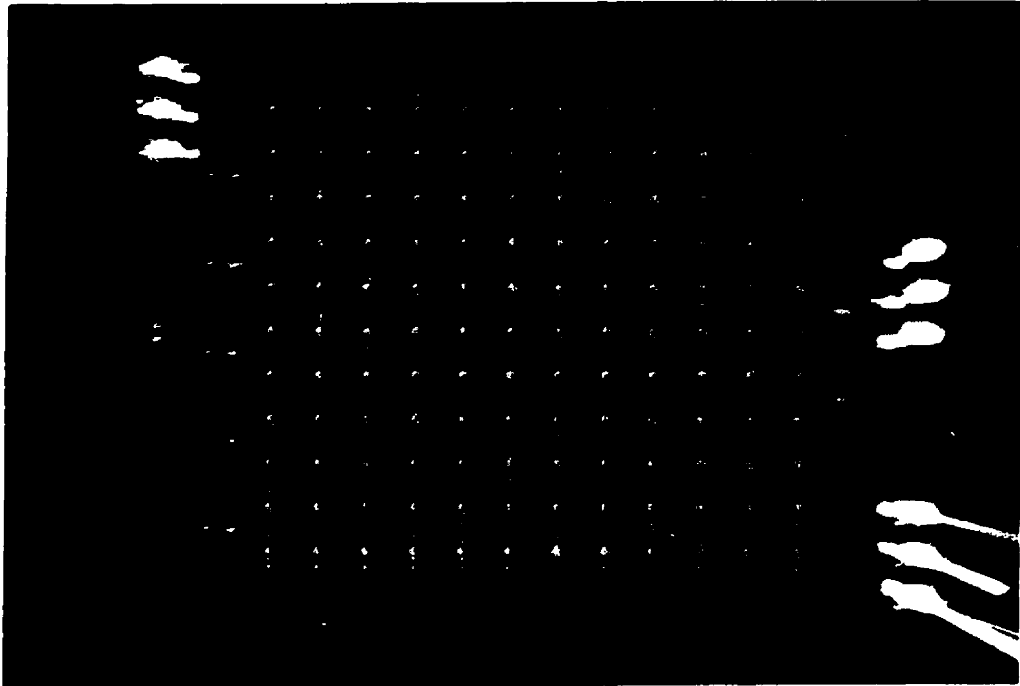


Figure 4.20b: Close-up view of the nltl chip

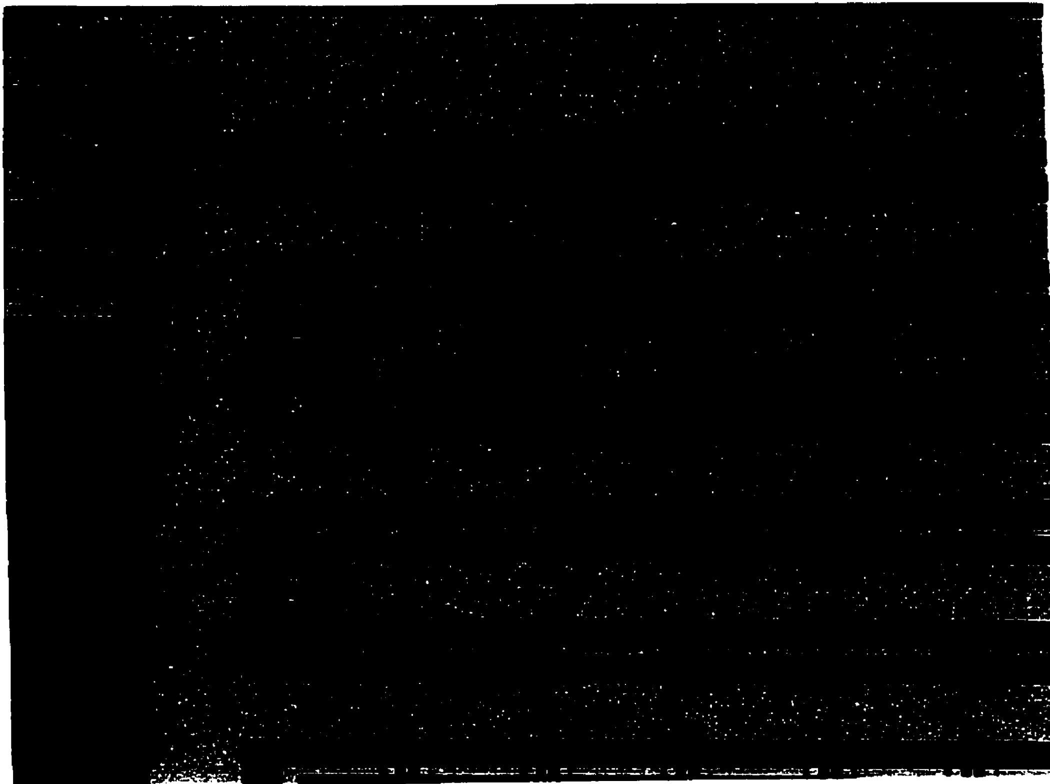


Figure 4.20c: Close up view at the input terminal of the nltl circuit.

4.1.4 Experimental

4.1.4.1 DC Measurement Experimental Set-Up and Result

The set-up for dc measurement is shown in figure 4.21. An HP 4145A Semiconductor Parameter Analyser was used to perform the measurements. From the equivalent circuit in figure 4.6, the NLTL's Current-Voltage characteristic is similar to that of a diode for a dc input voltage signal.

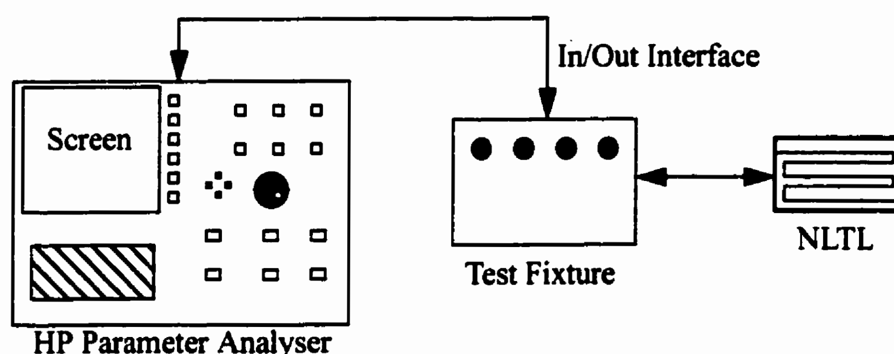


Figure 4.21: DC measurement set-up

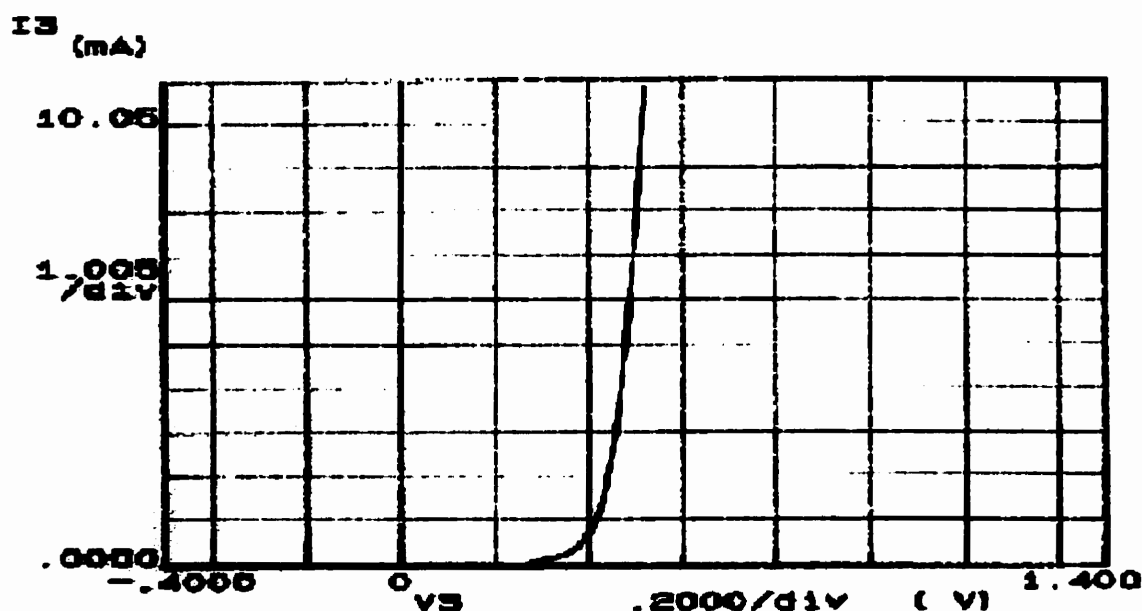


Figure 4.22: Current-Voltage characteristic of the NLTL for a dc input voltages

Figure 4.22 shows the I-V characteristic of the NLTL for a dc input voltage as predicted.

4.1.4.2 HF Measurement Experimental Set-Up

The set-up used to test the fabricated IC NLTL is shown in figure 4.23.

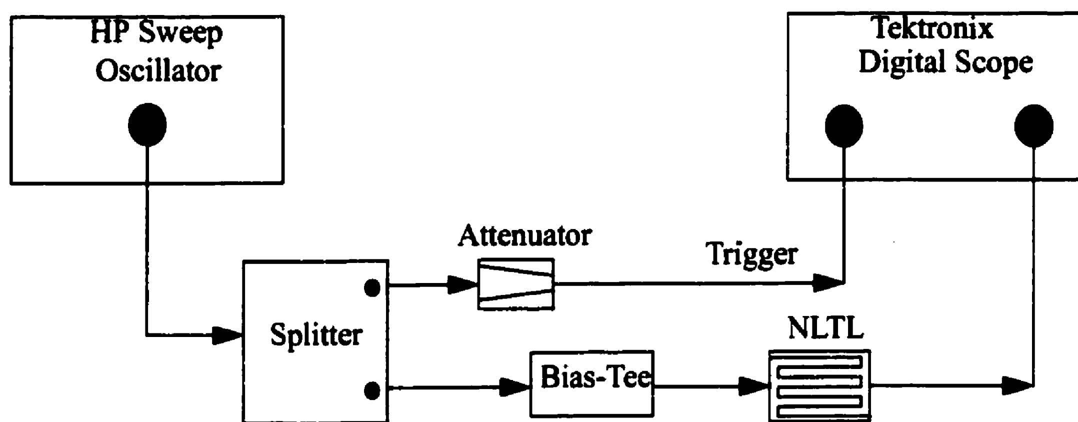


Figure 4.23: HF measurement set-up

The HP 8620C sweep oscillator was used to generate the input sinusoidal signal. In order to use the same signal from the HP sweep oscillator for triggering, a splitter was used. The purpose of the attenuator was to decrease the trigger signal's amplitude to prevent any damage done to the Tektronix digital scope. To control the amplitude range of the input signal, a bias tee was used. A Tektronix sampling scope was used to measure the output waveform of the NLTL.

Due to the low frequency limited packaged style used for the NLTL, the input signal is attenuated greatly just before it enters the first section of the NLTL. This is demonstrated in figure 4.24 and 4.25.

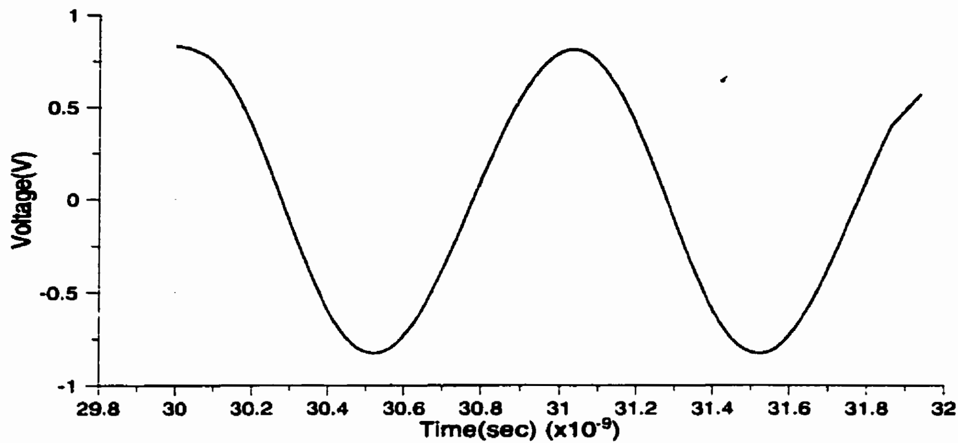


Figure 4.24: 1 GHz sinusoidal input signal generate by HP Sweep Oscillator

Figure 4.24 shows a 1GHz input signal generated from the HP Sweep Oscillator. Using a contact probe, the input signal is internally measured at the input bond pad just before it entering the first section of the NLTL. Figure 4.25 shows the measurement at the input bond pad of the IC NLTL for a 1GHz sinusoidal signal. Clearly, an attenuation of the input signal can be seen. This attenuation limits the amplitude of the output signal.

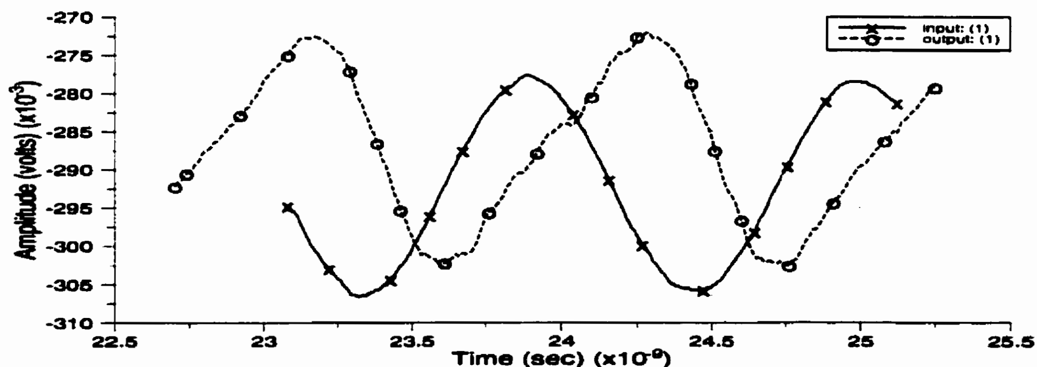


Figure 4.25: 1GHz sinusoidal input signal measure at the first input bond pad of NLTL and the output waveform using a contact probe.

4.1.4.3 HF Measurement Results

Measurements of the output waveforms were performed at varieties of frequencies. These data can be seen in Appendix. One of the best measurements is shown below. The output signal was measured for 1GHz sinusoidal input signal.

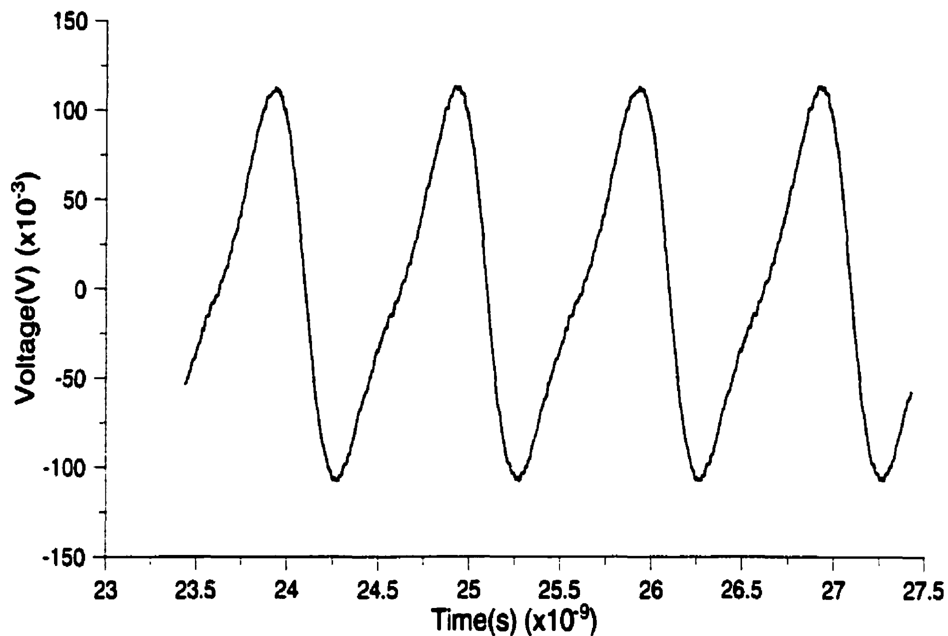


Figure 4.26: Output waveform of the NLTL for a 1GHz sinusoidal input. 0-100% falltime is ~286ps. 10-90% falltime is 185ps, and 20-80% falltime is 130ps.

The resulted waveform has a 0-100% falltime of 286 ps. A compression time of 214 ps was obtained. This result is a bit less than the estimated compression calculation of 233 ps. This is to be expected since non-idealities in the transmission line such as dispersion and reflection losses are unavoidable. The 10-90% and 20-80% falltime of the resulted waveform is 185 ps and 130 ps, respectively.

To obtain repetitive narrow pulses, the waveform in figure 4.26 is differentiated. This is illustrated in figure 4.27. The FWHM of the pulse is 280 ps.

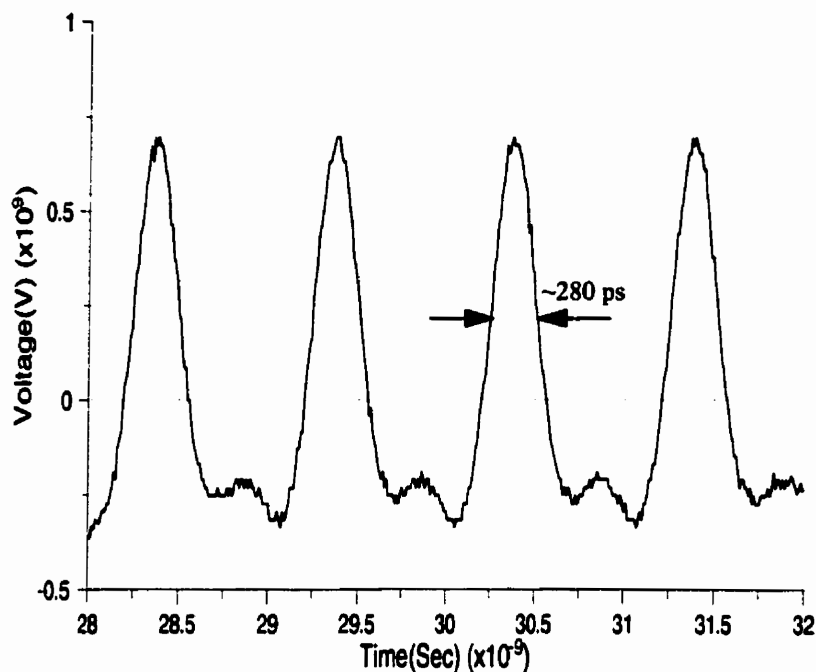


Figure 4.27: Derivative of the Compressed Waveform. The FWHM is 280 ps.

4.2 AND GATE

AND gate is often used in combination with other gates to produce large circuits such as switching networks, high speed comparator, gating circuits, etc. However, AND gate by itself can also be used to generate narrow pulses. The specification and application of this technique is currently being investigated by the SPM laboratory at the University of Manitoba. In this section, a brief overview of the technique along with the results are present.

4.2.1 Overview

The two inputs AND gate chip (NL4519-2) was purchased from NEL. The function diagram along with the truth table of the chip are shown in figure 4.28 and table 1, respectively.

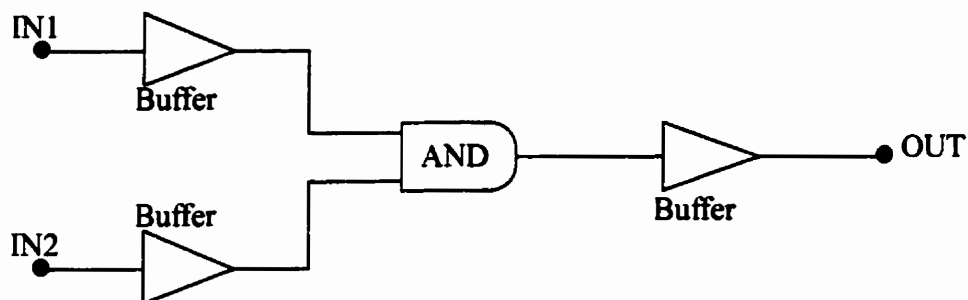


Figure 4.28: Function diagram for the two input AND gate Chip [29]

Table 1: Truth table for the AND gate

IN1	IN2	OUT
L	L	L
L	H	L
H	L	L
H	H	H

The high (H) and low (L) logic in table 1 correspond to 0V and -0.9V respectively (The chip's Vref is -0.5V while Vss is equal to -3.5V). From table 1, the delay between the two input signals is adjusted in order to obtain a desirable pulse at the output. The specification given by NEL has an output Full Width Half Max (FWHM) of about 150ps

4.2.2 Results

The HP data generator was used to generate the two input signals. The frequency of the input signal is 250 MHz. Figure 4.29 shows the input signals with 800 ps delay between them.

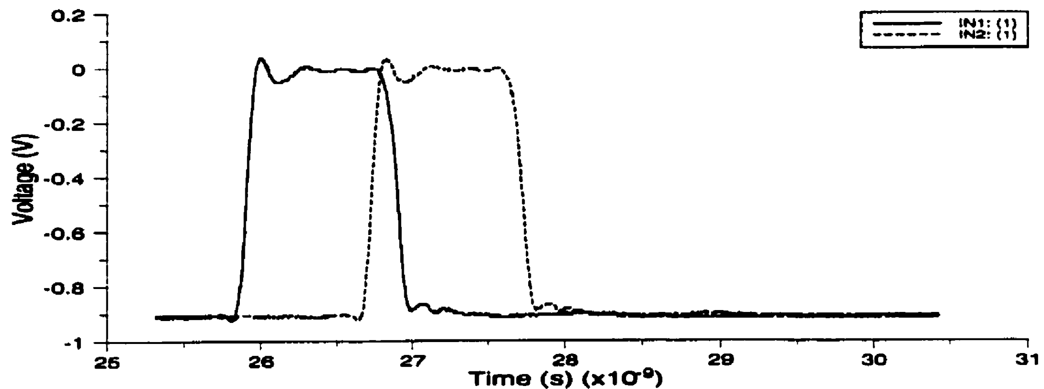


Figure 4.29: Input Signals to an AND Gate

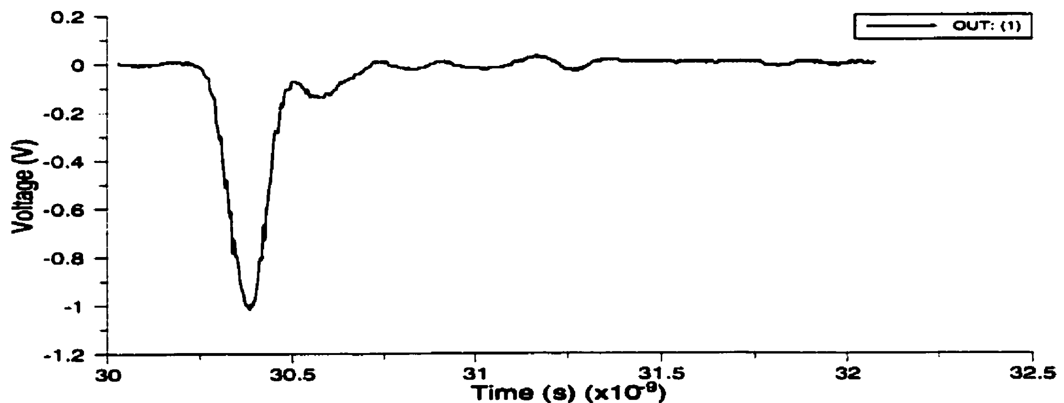


Figure 4.30: Output Signal of the 2 Input AND Gate

Figure 4.30 shows the output signal of the AND gate. The amplitude of the signal is approximately 1V. the signal's FWHM is ~150 ps.

4.3 IMPULSE GENERATOR (COMB GENERATOR)

4.3.1 Introduction

Impulse generator is used to generate narrow width pulses from sinusoidal input. The main component of this device is the Step Recovery Diode (SRD). Introduced in the late 50s, the SRD is a charge storage diode with a PIN construction [50]. The ideal model of the SRD is shown in figure 4.31. The SRD behaves as a two-states capacitors. The capacitance is large under forward bias and small in the reverse bias condition.

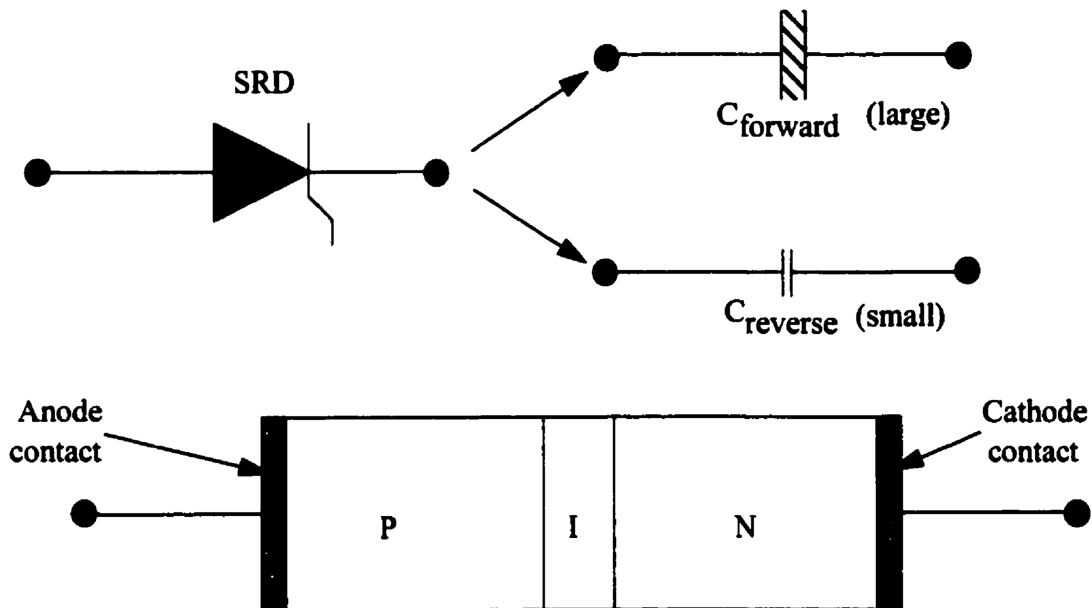


Figure 4.31: Schematic view of an ideal model of the Step Recovery Diode

During the forward conduction state from the positive half cycle of the sinewave (for example), the diode stores charge which must be removed by negative current before the diode can follow the input voltage. When the removal of the stored charge is completed, the generator voltage is quite low. Thus as the diode open, its terminal voltage

changes almost instantaneously to the negative voltage, generating a very fast step in the picosecond range. An illustration of this process is shown in figure 4.32. The fast transition time of the output waveform depends on the RC time constant [26]. R is the parallel combination of the generator and load resistance and C is the reverse bias capacitance of the diode.

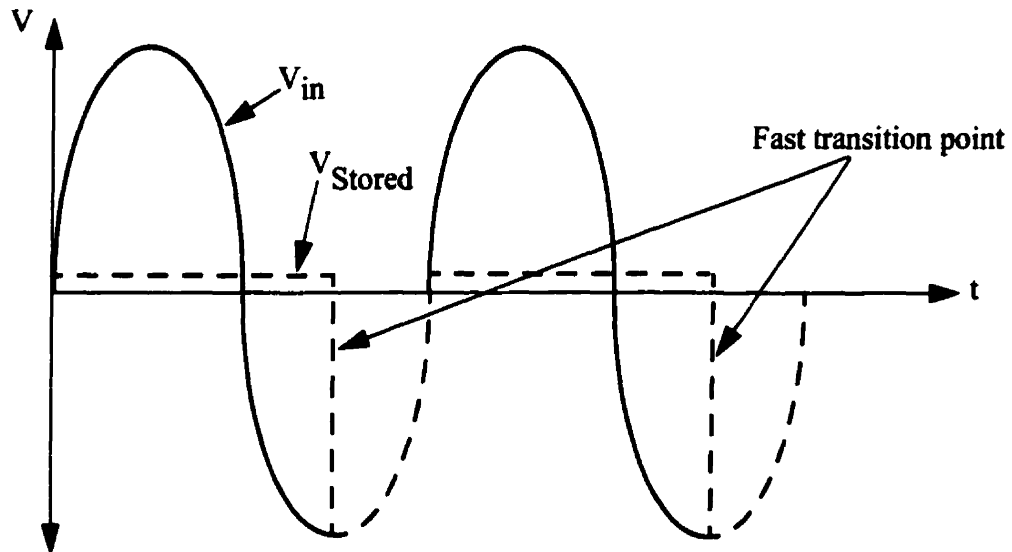


Figure 4.32: Illustration of the fast step generation process of the SRD

4.3.2 Impulse Generation

To generate a series of impulses, an inductive matching network is used so that the 50 Ohm source drive can be matched to the lower diode impedance. A typical impulse generator circuit is shown in figure 4.33. The circuit consists of an input impedance matching network, a Step Recovery Diode and a DC return. The main function of the DC return is to provide the self-biasing current return for proper operation. The DC return can be implemented internally or externally. A typical output of the impulse generator can be seen in figure 4.34.

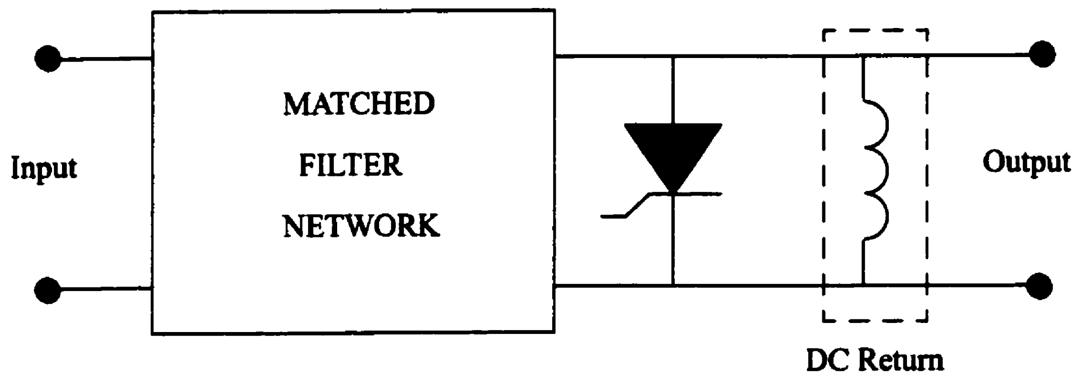


Figure 4.33: A typical impulse generator circuit [50]

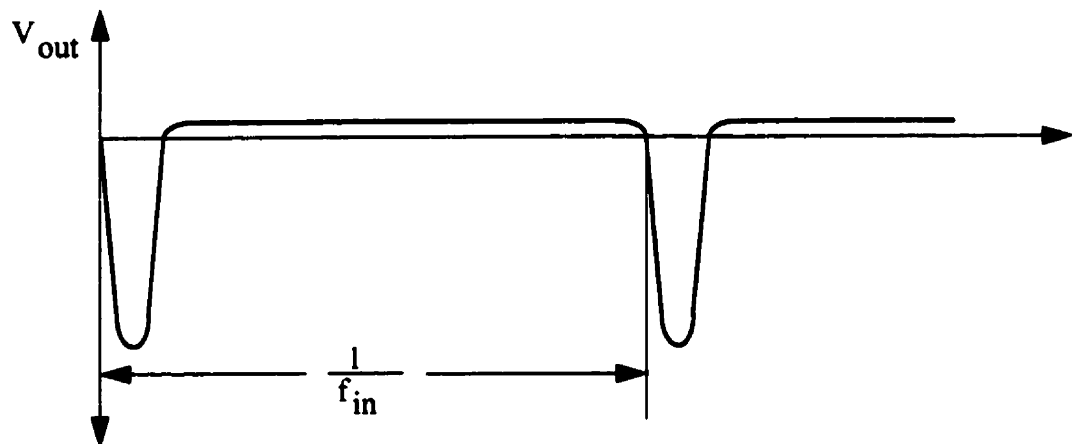


Figure 4.34: Typical output of an impulse generator [50]

Presently, impulse generators are commercially available for wide range of input frequencies driven at a power level of 1/2 watt referenced to 50 Ohms. Impulse generator can be built for input frequencies as high as 8 GHz with output capabilities up to 50 GHz [50].

4.3.3 Experimental Set-Up and Results

An impulse generator with an input frequency of 250 MHz was purchased from HEROTEK, INC. The circuit is driven at 1/2 watt referenced to 50 Ohms. The expected Half Max Full Width (HMFW) output of ~120ps is used as a sampling pulse for EFM testing in this research. The set-up used to test the impulse generator is shown in figure 4.35.

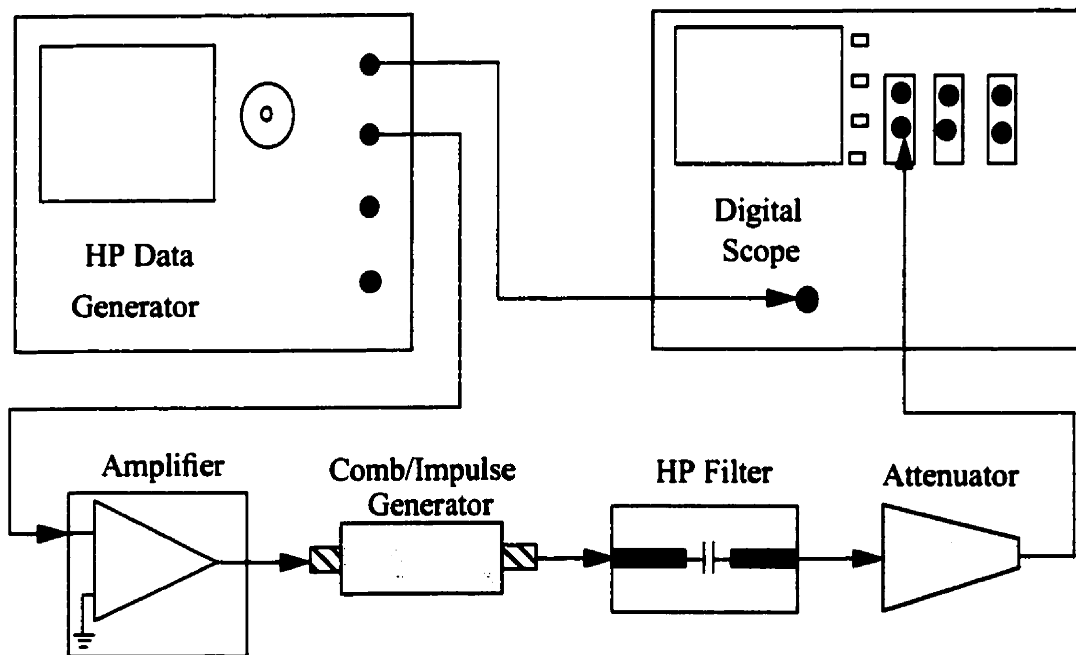


Figure 4.35: Experimental set-up for testing the impulse generator.

An HP data generator is used to generate a repetitive 250 MHz pattern. To ensure a sinusoidal signal with adequate amplitude at the input of the impulse generator, a dc to 500 MHz amplifier is used. The high pass filter is put in place to eliminate the fundamental harmonic of the output from the impulse generator. The high pass filter consists of a surface mount capacitor connected in series with a 50 Ohms microstrip line. The characteristic of the filter is shown in figure 4.36. The filter has a -3dB cut off frequency of ~300

MHz. An attenuator is used to prevent any damage done to the digital scope since large amplitude at the output is expected.

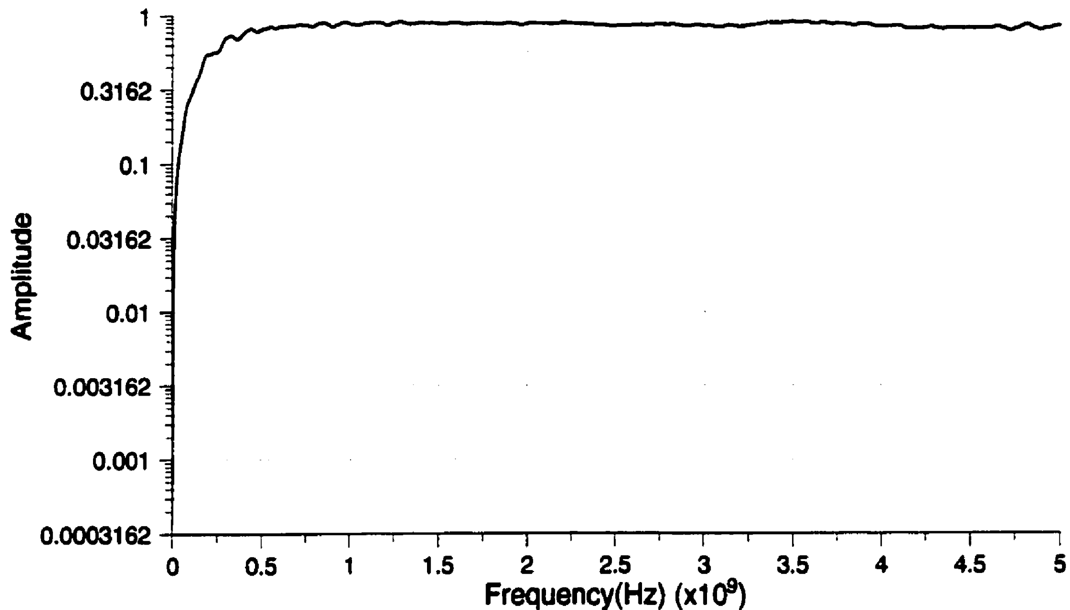


Figure 4.36: Characteristic of the high pass filter. the -3dB cut-off frequency is 300MHz.

An example of the comb generator output using the above set-up is shown in figure 5.36. Maximum output was obtained by using a 300 MHz high pass filter, an attenuator of 23 dB, and a 250 MHz pattern with 1.4V in amplitude from the HP data generator. A 1.4 V at the input of the amplifier produced a comb generator's output of approximately 11V. The output still possesses undersire non-idealities which can be further minimized by using a dc-5GHz switch. However, the trade off for minimization of these non-idealities is large reduction in amplitude of the output. This process is demonstrated in section 5.3. The FWHM of the output pulse is approximately 120ps.

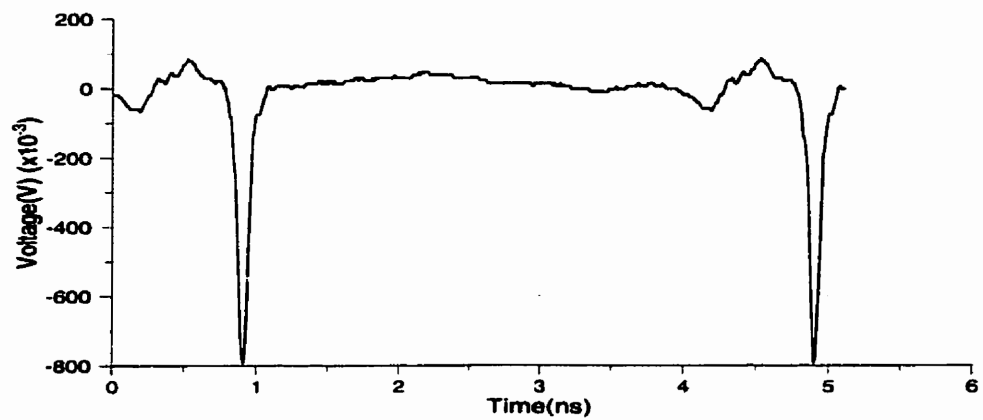


Figure 4.37: Experimental output of the impulse generator. The FWHM is 120 ps.

CHAPTER 5

PATTERN EXTRACTION TECHNIQUE

This chapter will introduce the theory behind the pattern extraction technique. Next, the sensitivity of the technique and the sampling signal are characterized. Finally, the experimental set-up and results are presented.

5.1 Overview of the Technique

In the pattern extraction technique, a modulated narrow pulse excitation is used as a sampling signal to the probe. A sampling technique [7] which is based on the heterodyne scheme is used. A block diagram of the technique is shown in figure 5.1. The signal $v_c(x,y,t)$ represents a known arbitrary test pattern which is generated and feeds to the circuit under test. An example of the $v_c(x,y,t)$ signal is shown in figure 5.2a. A beam bounce detection system along with a micromachined Si_3N_4 tip is used to enhance the measurement of the results. A sampling signal with a controllable delay, $v_s(t) = G_\delta(t\text{-}\tau)$, which is

shown in figure 5.2b is generated in synchronization with $v_c(t)$. The signal $v_s(t)$ is then fed to a high frequency analog switch which behaves as a modulator.

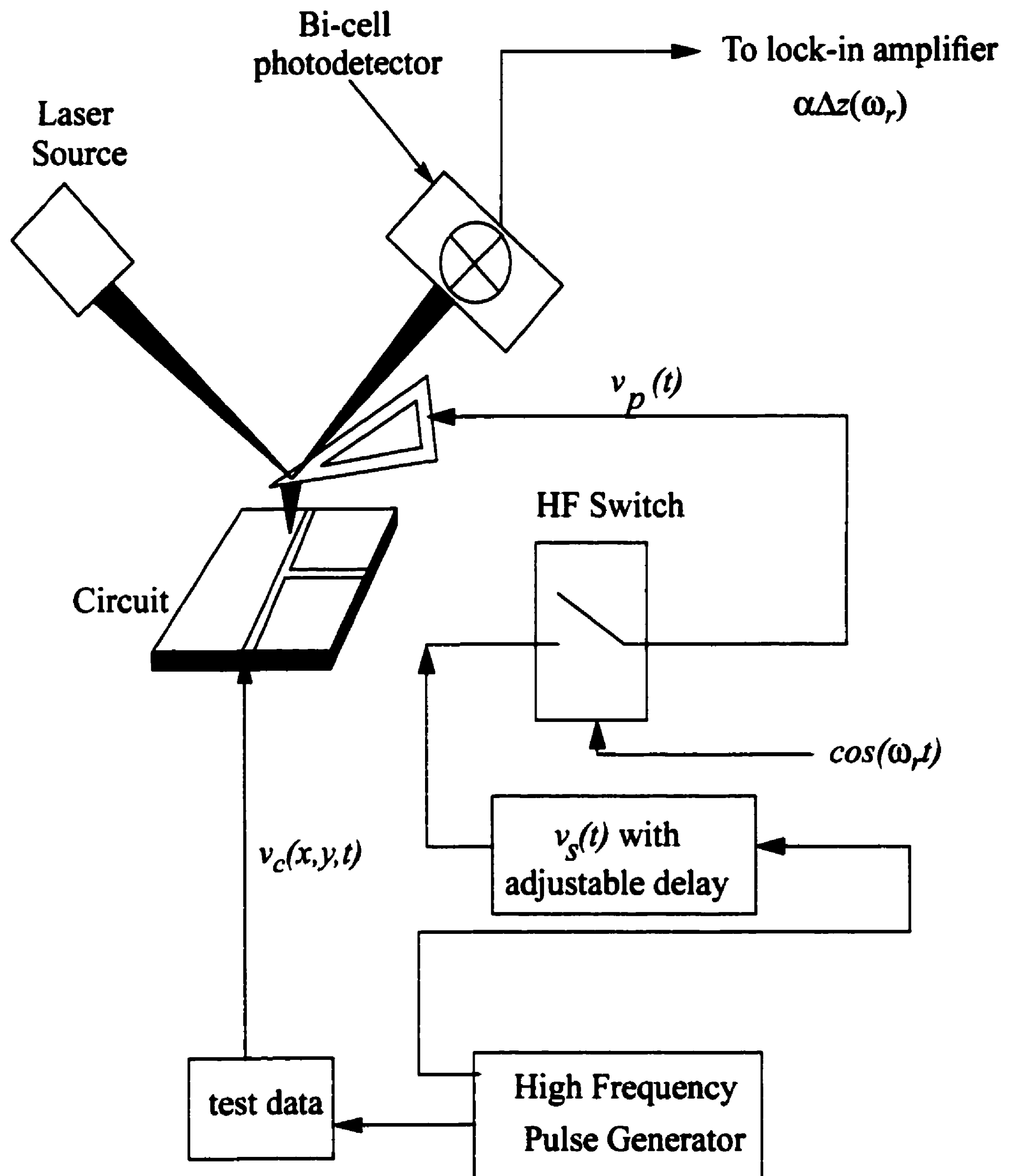


Figure 5.1: Block diagram of the pattern extraction technique using the heterodyne electrostatic force microscopy.

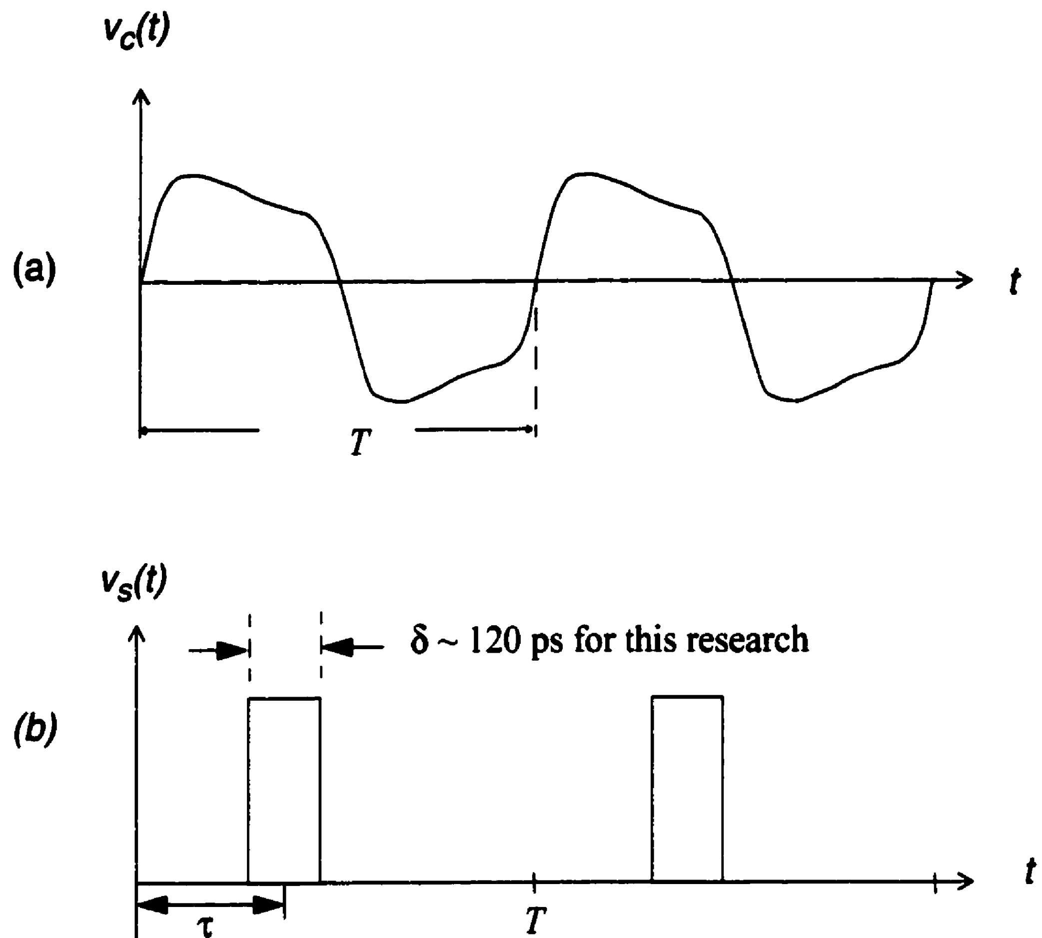


Figure 5.2: (a) an arbitrary waveform $v_c(x,y,t)$ (b) sampling signal $v_s(t)$

As discussed in chapter 3, best results will be obtained when the experiment is being performed at the resonant frequency of the probe. Thus using the high frequency analog switch, the sampling signal is modulated at the resonant frequency f_r to enable measurements to be performed at f_r. This is known as the heterodyne technique [41]. The output of the switch can be treated as a multiplication of its two inputs. Figure 5.3 illustrates the output of the sampling signal modulated at the resonant frequency f_r. Thus for f_r = 1KHz and T_s, the period of the sampling signal is equal to $(\delta * N)$ = (100ps * 8bits) =

0.8ns, then there will be $0.5T_r / T_s = 62500$ sampling pulses for every 0.5ms.

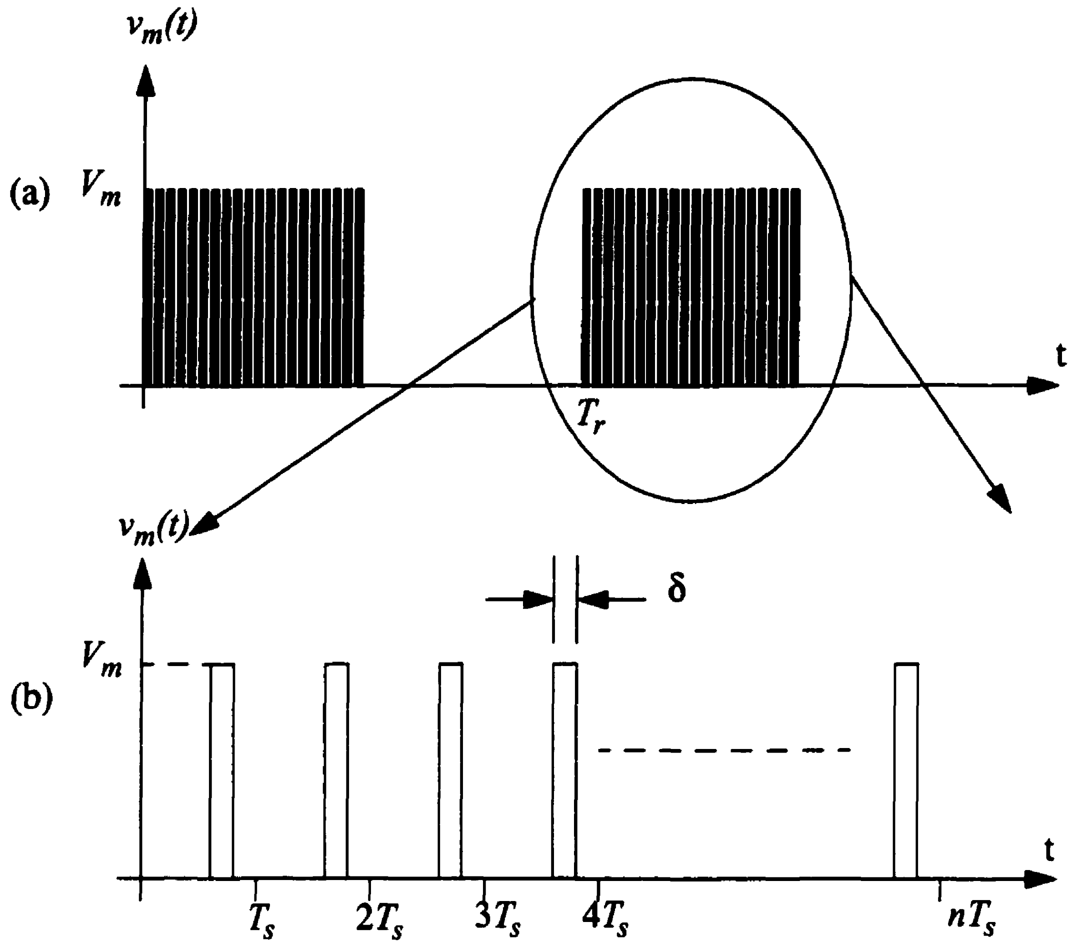


Figure 5.3: (a) illustration of the sampling signal modulated by a periodic square signal with frequency f_r (b) zoom-in view of the sampling pulse train

The modulated sampling signal is then sent to the probe and can be written as:

$$v_p(t) = [Krect(\omega_r t)] \bullet v_s(t) = \left[\frac{2K}{\pi} \sum_{n=1,odd}^{\infty} \frac{1}{n} \cos(n\omega_r t)\right] \bullet G_\delta(t-\tau)$$

Equation 5.1: probe signal in the pattern extraction technique

Substituting equation 5.1 into the expanded version of equation 3.26, the force and

the resulting deflection at the resonant frequency $\omega_r=2\pi f_r$ will be

$$F_z(\omega = \omega_r) = \frac{\partial}{\partial z}C(x,y,z)\ [\Delta\Phi\langle G_\delta(t-\tau)\rangle - \langle G_\delta(t-\tau), v_c(x,y,t)\rangle] \bullet \frac{K}{\pi}\cos(\omega_r t)$$

Equation 5.2: resulting force at resonant frequency

$$\Delta z(\omega = \omega_r) = \frac{Q}{k}\frac{\partial}{\partial z}C(x,y,z)\ [\Delta\Phi\langle G_\delta(t-\tau)\rangle - \langle G_\delta(t-\tau), v_c(x,y,t)\rangle] \bullet \frac{K}{\pi}\cos(\omega_r t)$$

Equation 5.3: resulting deflection at resonant frequency

where $\langle a(t), b(t)\rangle = \frac{1}{T}\int_0^T a(t)b(t)dt$,and $\langle a(t)\rangle = \frac{1}{T}\int_0^T a(t)dt$ represents the inner product and the average over period T, respectively. For an ideal sampling pulse with infinite rise and fall time along with narrow width, $\delta \ll T$, the inner product and the average of the sampling pulse over period T are as follow:

$$\langle G_\delta(t-\tau), v_c(x,y,t)\rangle \approx \delta/T \bullet v_c(x,y,t=\tau) \ \text{ and } \ \langle G_\delta(t-\tau)\rangle = \delta/T$$

Equation 5.4: inner product and average over period T for an ideal sampling pulse with $\delta \ll T$

δ/T is the duty cycle of the sampling pulse. Substituting equation 5.4 into equation 5.3, the resulting deflection for an ideal sampling pulse can be expressed as follow:

$$\Delta z(\omega = \omega_r) = \frac{Q}{k} \bullet \frac{\delta}{T} \bullet \frac{\partial}{\partial z}C(x,y,z)\ [\Delta\Phi - v_c(x,y,t=\tau)] \bullet \frac{K}{\pi}\cos(\omega_r t)$$

Equation 5.5: resulting deflection for ideal sampling pulse with $\delta \ll T$

In pattern extraction measurement where the waveshape rather than the absolute voltage level is considered, the term $\Delta\Phi$ will only add to the dc offset of the results. Thus $\Delta\Phi$ can

be neglected. As a result, equation 5.5 shows that the voltage of a point on the circuit under test is proportional to the resulting deflection of the probe at that particular point. Thus, the waveform $v_c(x,y,t)$ can be extracted by sweeping across the entire periodic signal $0 < \tau < T$. The measured signal is essentially the time domain convolution between the sampling signal and the signal of the test circuit. This technique enable measurements such as rise and falltime of the signal. Propagation delay between signals can also be evaluated using this technique.

To perform the absolute voltage measurement, a heterodyne/nulling force technique [8] is used where the modulated probe signal is as follow:

$$v_p = [A + K\cos(\omega_r t)] \bullet v_s(t)$$

Equation 5.6: modulated probe signal used in heterodyne/nulling force technique

where A and K are controllable parameters. Following the same mathematical step as in the pattern extraction technique, the resulting deflection for an ideal sampling pulse can be written as follow:

$$\Delta z(\omega = \omega_r) = \frac{Q}{k} \bullet \frac{\delta}{T} \bullet \frac{\partial}{\partial z} C(x, y, z)\ [A + \Delta\Phi - v_c(x, y, t = \tau)] \bullet K\cos(\omega_r t)$$

Equation 5.7: resulting deflection for heterodyne/nulling force technique for absolute voltage measurement

Voltage at a desired point on the test circuit can be obtained by adjusting the parameter A so that the deflection is nulled. However, this technique requires expensive electronics for calibration purposes. In this research, only the experiment for pattern extraction technique will be performed.

5.2 Sensitivity of the Pattern Extraction Technique

The voltage sensitivity of the technique is calculated by using the RMS force at the resonant frequency of the cantilever probe. Using equation 5.2 and for an ideal sampling pulse, the RMS force at the probe resonant frequency can be expressed as follow:

$$\langle F_z^2(\omega_r)\rangle^{1/2} \approx \frac{\delta}{T}\cdot\frac{4K}{\pi}\cdot\frac{\partial}{\partial z}C(x,y,z)\cdot\frac{1}{\sqrt{2}}\cdot v_c(x,y,t=\tau)$$

Equation 5.8: RMS force at the probe resonant frequency

The sampling pulse used in this research has a width of ~120ps, a period of 4ns and an amplitude of 1V. Thus the duty cycle, δ/T, is approximately 1.2 / 40. K represents the amplitude of the pulse at the probe tip. Since the sampling pulse sees the probe as an open circuit [38], the amplitude at the probe tip is approximately 2 V. Using Equation 3.23 the voltage sensitivity of the pattern extraction technique is given by

$$\Delta V_{rms} = \frac{\pi\cdot T}{2\cdot\delta\cdot K\cdot|\partial C/\partial z|}\cdot\sqrt{\frac{2kk_BT_a}{Q\omega_r}}$$

Equation 5.9: Voltage sensitivity of the pattern extraction technique

Measurements for the pattern extraction technique in this research are done with the tip-circuit separation of 1μm. At this distance the derivative of the capacitance with respect to z, $\partial C/\partial z$, is estimated as 55 pF/m [6]. Thus, for a typical micromachined probe ($Q = 32$, $k = 0.347 N/m$, $f_r = 12.275 kHz$), the voltage sensitivity is approximately 16.2 mV/ $\sqrt{Hz}$.

5.3 Experimental Set-Up

Schematic diagram of the experimental set-up for the pattern extraction technique is shown in figure 5.4. The narrow width sampling pulse is generated by using the comb/ impulse generator method.

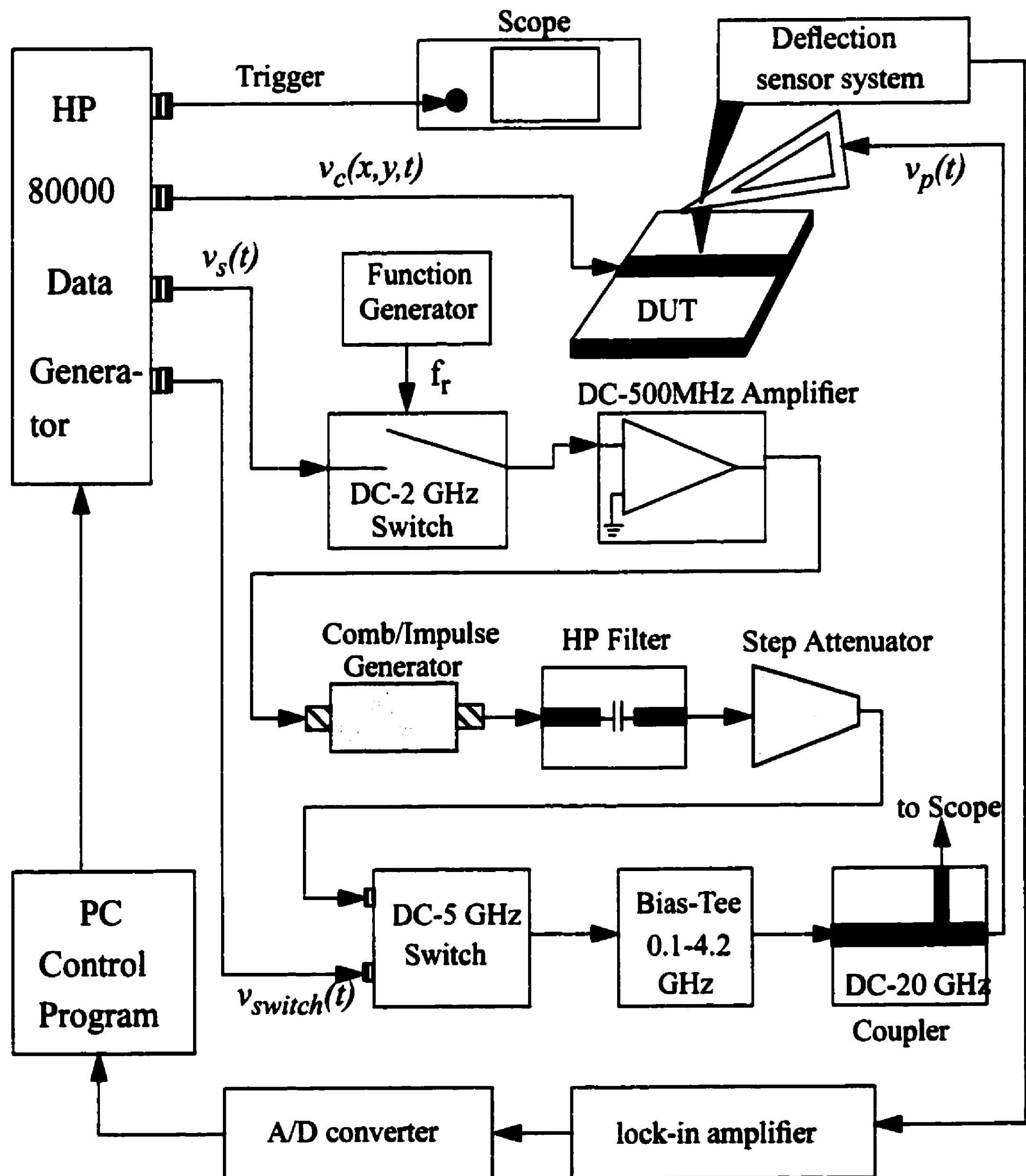


Figure 5.4: Experimental-set up of the pattern extraction technique.

In figure 5.4, a computer program is used to command the HP80000 data generator to generate the required high frequency signals. The data generator is capable of generating signal up to 1 Gb/s with a transition time of approximately 175ps. The HP80000 can generate signal with a delay ranging from -2ns to +2ns and a delay resolution of 2ps. Channel 1 and 2 of the HP80000 output signals to be used as an external trigger to the scope and repetitive test pattern to the circuit under test, respectively. The third channel is used to generate a repetitive sampling signal of 250MHz. The DC-2GHz switch functions as a modulator which modulates the sampling signal with a square wave signal. A function generator is used to output a square wave signal at the probe resonant frequency. The DC-500MHz amplifier, comb/impulse generator and hp filter are employed to produced an ultra fast pulse with large amplitude. The step attenuator is put in place to prevent any damage to the DC-5GHz switch which could be caused by amplitude of larger than 5V at the input. The HP80000 data generator's fourth channel outputs a signal which is used to control the DC-5GHz switch. By adjusting the delay of the switch's control signal, $v_{switch}(t)$, the non-idealities of the sampling pulse can be further minimized. However, the minimization of the non-idealities reduced the amplitude of the output generated by the comb generator system. The DC-5GHz switch is also acted as a 50Ω load to absorb the reflected sampling signal. This prevents multiple reflection in the sampling signal which could produced undesirable output. The bias tee is used to eliminate the dc offset and prevent any damage to the instruments used in this set-up. A 20:1 coaxial coupler allows the user to view the probe signal on the scope. This is very convenient when trying to achieve an ideal probe signal by adjusting various control parameters in the set-up. Analog measurements obtained by the lock-in amplifier is converted to digital by using an A/D con-

verter. Finally the computer program stores the data into a specified file.

Figure 5.5 shows the sampling signal at the probe tip. The graph is obtained from the scope with 3dB at its input. Thus the actual amplitude of the pulse is 1.4 times that shown in figure 5.5. This is much lower than the output obtained without the DC-5GHz shown in section 4.3.3. However the pulse is much cleaner thus enabling better data to be obtained. The pulse has a FWHM of 120ps. The repetition frequency is 250MHz.

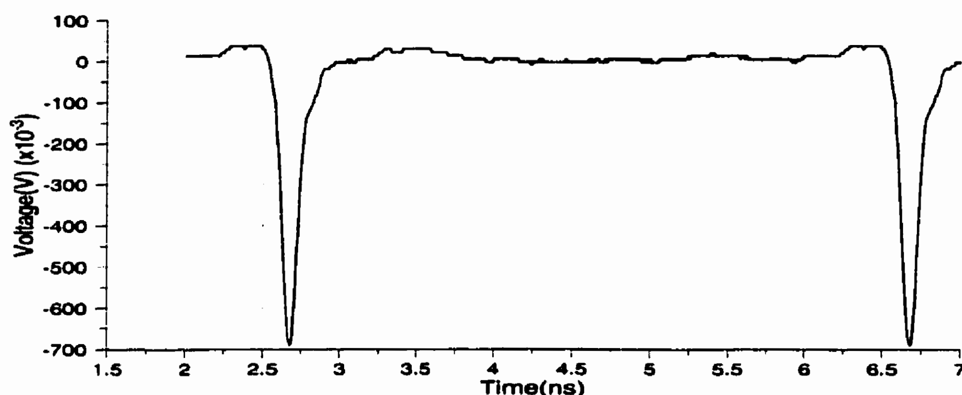


Figure 5.5: Sampling pulse at the probe tip as captured on the oscilloscope with the help of a 10:1 coaxial coupler. The pulse has a repetition rate of 250MHz and FWHM of 130ps.

5.3.1 Characterization of the Sampling Pulse

In this section, the non-ideality of the sampling pulse caused by the ripples exist around the base of the pulse is further investigated. As mentioned earlier, the EFM measured data is essentially the convolution between the sampling pulse and the applied signal. Thus a convolution program is written to generate simulated EFM data using the specified applied signal and the pulse at the probe. Figure 5.6 shows the sampling pulse and a square wave applied signal with a frequency of 500MHz. Also shown are the results from the convolution. The wave shape of the convoluted output is greatly distorted.

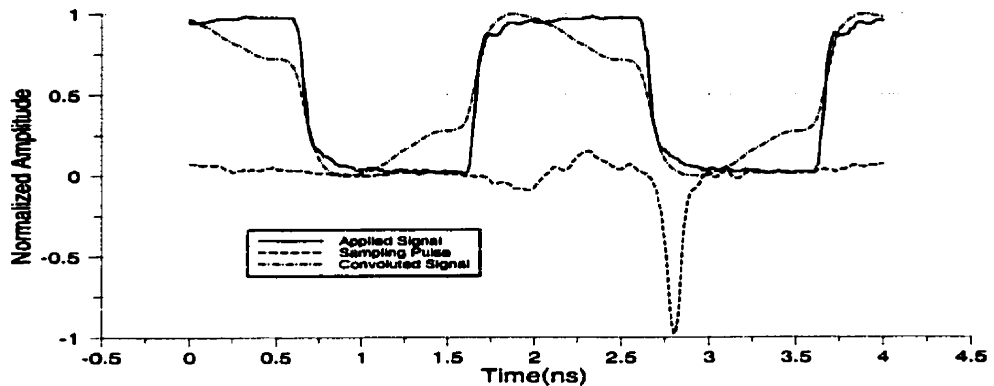


Figure 5.6: 500MHz applied signal, sampling pulse with large ripples and the convolution output.

To demonstrated the non-ideality effect, the ripples of the sampling pulse are decreased. A graph of the new sampling pulse along with the applied signal and the convolution output are shown in figure 5.7. The distortion of the output wave shape is largely reduced. This allows a more accurate measurement of the rise and fall time. Ultimately, better data will be obtained which enable a more accurate characterization of the circuit under test. In figure 5.7 the error bars at 1.5ns, 2ns, and 3ns represent plus and minus 3% errors (page 25 of the Tektronix Sampling Head SD-22 & Sd-26 User Manual) in the applied signal due to the aberrations of the digital scope's sampling head.

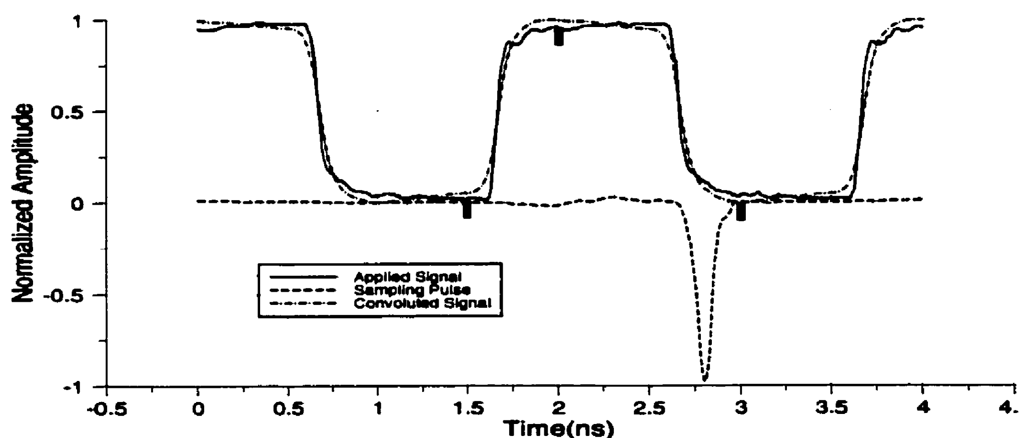


Figure 5.7: 500MHz applied signal, sampling pulse with small ripples and the convolution output. Also shown is the plus and minus 3% error bars representing the errors of the applied signal.

5.4 Experimental Results

In this section, measurement on the transmission line is presented and used to characterize the technique. Measurements on the BiCMOS as well as the CMOS integrated circuit are also shown.

5.4.1 Technique's Characterization using Microstrip Line

To evaluate the pattern extraction plus the rise and fall time measurement capability of the technique, A 50Ω microstrip interconnect is used. A schematic of the 50Ω line is shown in figure 5.8.

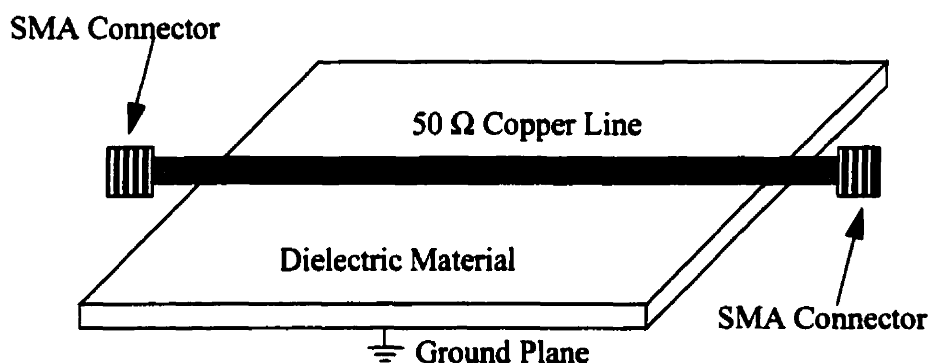


Figure 5.8: Schematic diagram of the 50Ω microstrip line.

5.4.1.1 Rise and Fall Time Measurement and Pattern Extraction

A 4-bit digital pattern [1010] at 0.5 Gb/s is applied to the line with the high and low logic set at +2V and -2V, respectively. A sampling pulse is modulated at the probe resonant frequency and is fed to the probe. To ensure that the entire pattern is to be measured, the computer program commanded the sampling pulse to shift from 0 to 8ns. The meas-

ured data is obtained with the sampling shift increment of 10ps. The applied signal along with the data from the EFM is plotted in figure 5.9. For comparison purpose, the signals are normalized to 0 and 1. The EFM data is plotted with a 10pts smoothing routine to reduce experimental noise. The results are in close agreement with each other.

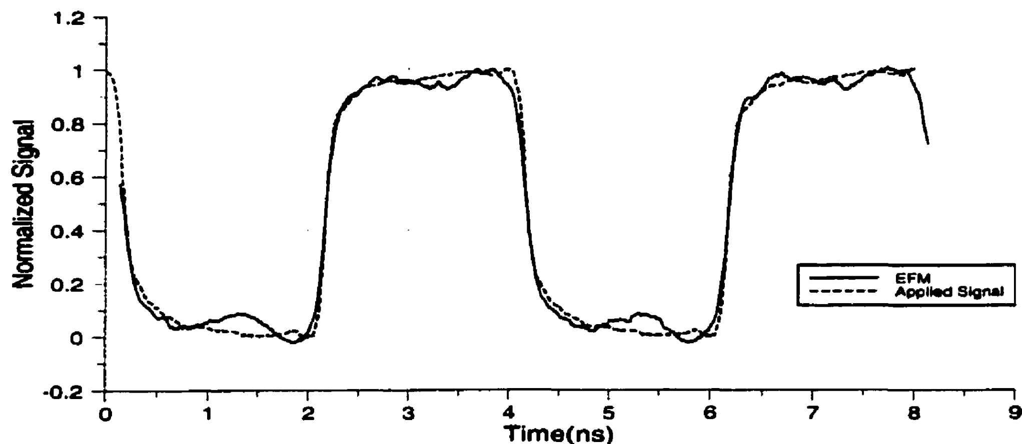


Figure 5.9: A 500 MHz digital test pattern (1010) with the EFM measured data (with 10 pts smoothing).

The measured data is further analysed by comparing it to the convoluted signal. This is shown in figure 5.10.

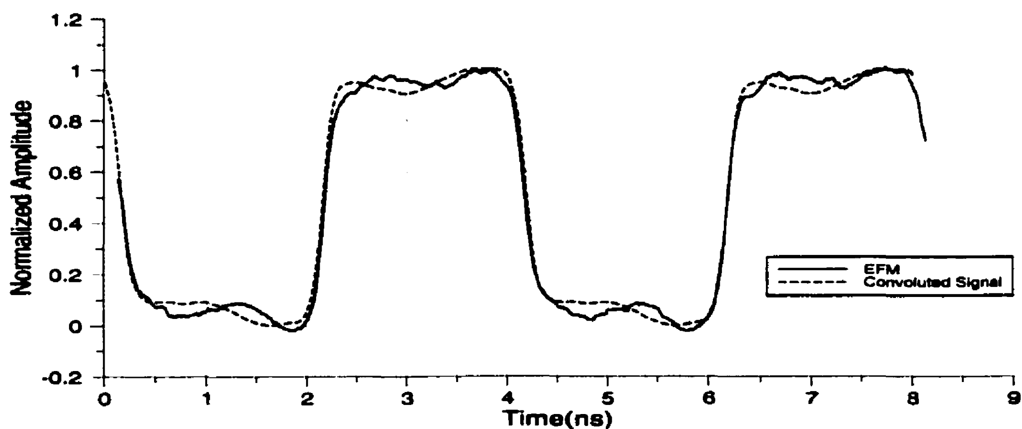


Figure 5.10: EFM measured data (with 10 pts smoothing) and convoluted signal between the sampling pulse and the signal applied to the DUT.

The convoluted signal is a result from convolving the sampling signal in figure 5.5

with the applied 500MHz digital test pattern. Again the two graph are in close agreement with a few discrepancies at the signal's high and low logic due to experimental noise. A close up of the rising edge with all three signals are shown in figure 5.11. The rise time(20%-80%) of the applied signal is estimated at 140ps while that of the EFM data is approximated at 170ps.

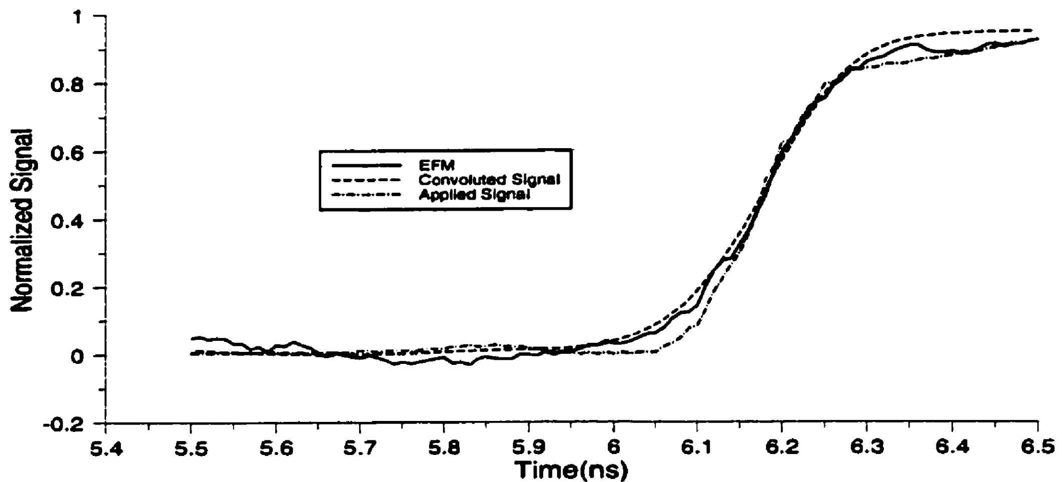


Figure 5.11: A closed up view of the applied test pattern, measured data from the EFM and the signal resulting from convolving the sampling pulse with the applied signal.

Next a deconvolution program is used to extract the applied signal from the measured data. This is done by deconvolving the sampling signal with the measured EFM data. First, the fourier transform of the sampling signal and EFM data is calculated and multiplied together. The convoluted signal is extracted by taking the inverse transform of the resulting product. A low pass filter routine is implemented into the deconvolution program to eliminate the experimental noise in the measured data thus enabling a clean deconvolved signal to be extracted. The deconvolved signal is compared to the applied signal and is shown in figure 5.12. The two signals are in good agreement with each other with

the exception at the high and low logic. The ripples effect existing in the deconvolved signal is due to the filter. The filter eliminated the higher harmonic of the pulse thus decreasing the accuracy of the reconstruction of the pulse. However, elimination of the filter resulted in a very noisy deconvolved signal.

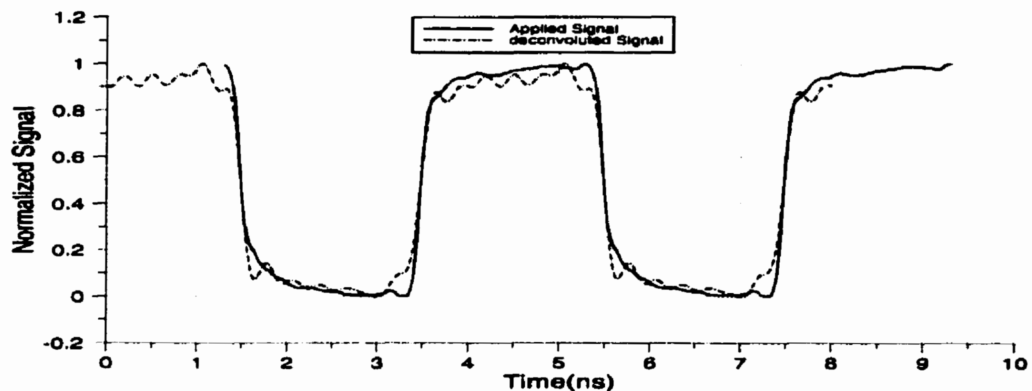


Figure 5.12: Applied signal and the deconvolved signal.

Next, measurement at a higher bit rate is presented. An 8 bit [10101010] digital pattern at 1Gb/s is applied to the line. the measurement specifications are same as the above. Results are shown in figure 5.13.

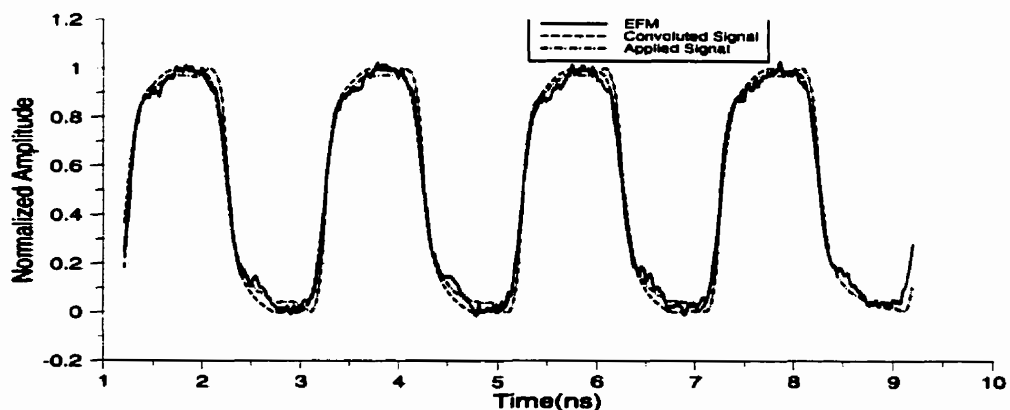


Figure 5.13: Applied signal, EFM data and convoluted signal of a 10101010 digital pattern at 1Gb/s.

Finally a 8 bit [00010001] digital pattern at 1Gb/s is fed to the microstrip line. Figure 5.14 shows the applied pattern, EFM data and the convolved signal. The graph demonstrates that the pattern extraction technique can be used to measure any arbitrary signal.

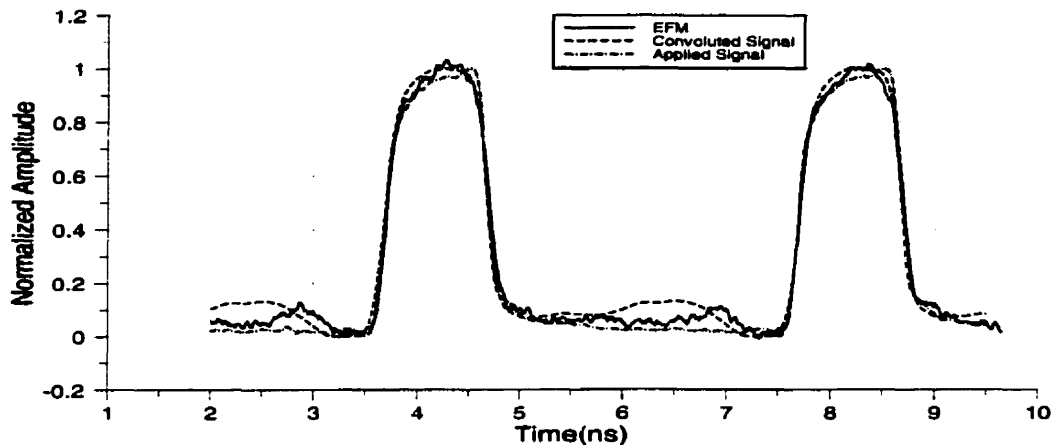


Figure 5.14: Applied signal, EFM data and convoluted signal of a 00010001 digital pattern at 1Gb/s

5.4.1.2 Propagation Delay Measurement Capability

The delay measurement capability of the technique is evaluated by sampling the same digital pattern with different delays. A program is written to command the HP80000 data generator to output digital patterns of delay 0, 20, 50 and 100ps. Again measurements were done on a 50Ω microstrip line.The EFM data were taken with a shift increment in the sampling signal of 10ps. Other experimental parameters remain the same as those given in the previous section. To reduced the experimental time only one of the falling edges was measured and examined. The results are shown in figure 5.15. Figure 5.15a, c show the applied and EFM measured data of the falling edges. For a better reading, close-up view of a and c are shown in figure 5.15 b, d, respectively.

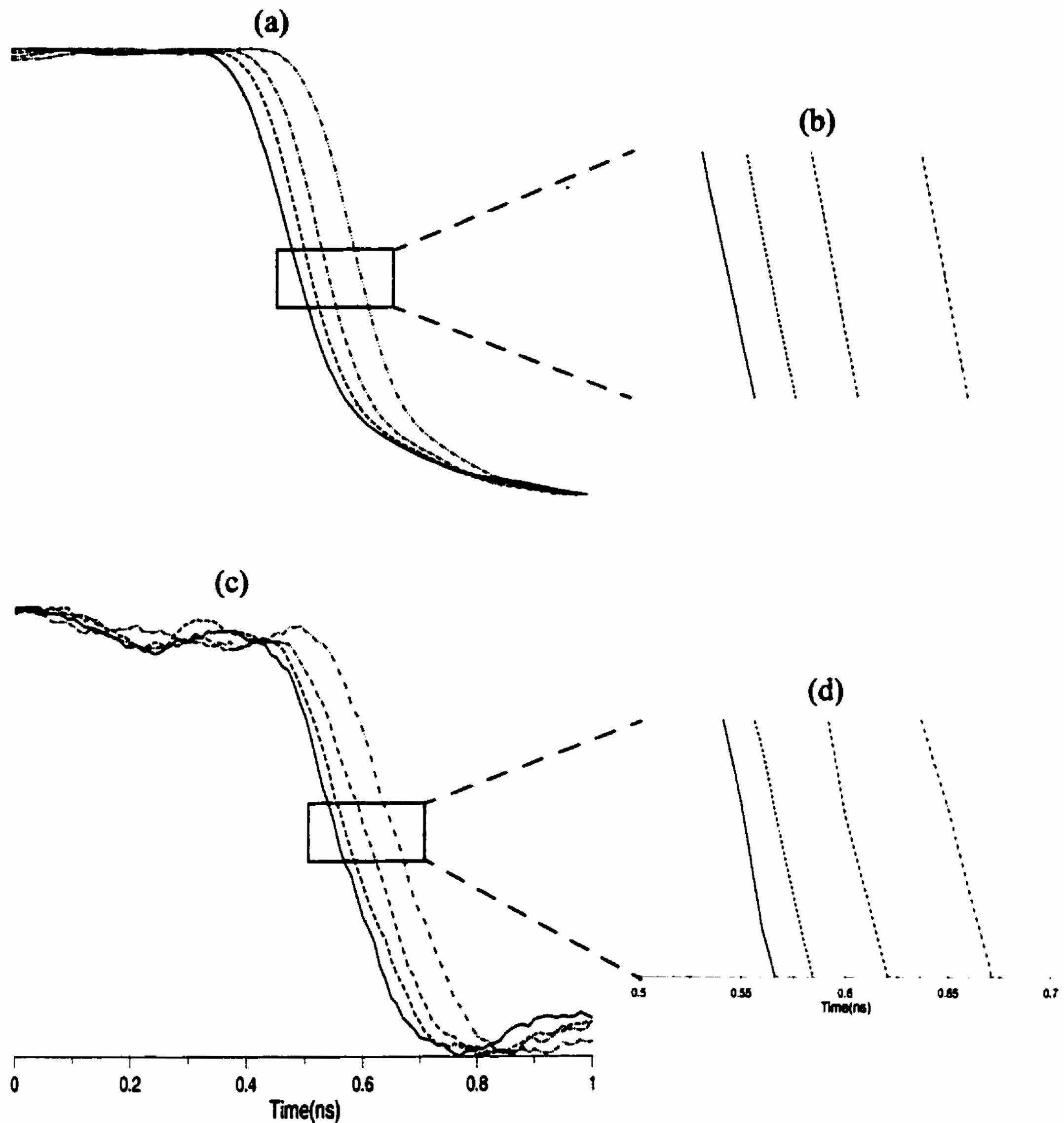


Figure 5.15: (a), (c) Applied and EFM data of the rising edges with 0, 20, 50 and 100 ps delay, respectively. (b), (d) close up view of (a) and (c).

Measurements show that this technique is capable of measuring the propagation delay within 20ps accuracy. Measurements of lower delay increments were also performed. However, poor results were obtained. The delay measurement accuracy is limited by jitter in the instrument and noise from coupling to probe from external sources. Other noise sources are probe deflection due to thermal noise and noise from deflection sensor.

5.4.1.3 Repeatibility of the Technique

In this section, evaluation of the accuracy of the pattern extraction technique in terms of Repeatibility will be presented. This is done by repeatedly sampling the same signal with all variables in the experiment held constant. Results will be used to characterize electrical as well as the mechanical noise. As in the previous two sections, measurements were performed on a 50Ω microstrip line. Again only one of the falling edge is sampled to reduce the experimental time. Figure 5.16 shows the EFM measured data of the same digital pattern being sampled 10 times.

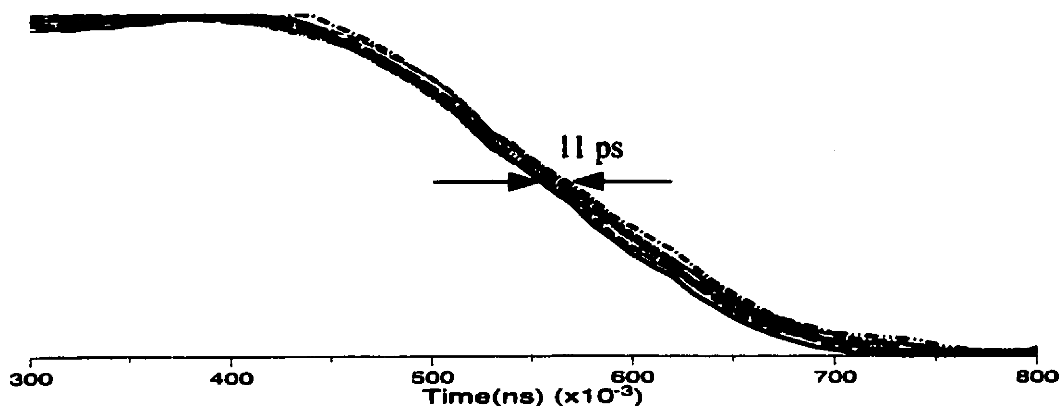


Figure 5.16: EFM data of the falling edge being sampled 10 times.

Measurements show that the pattern extraction technique has an excellent Repeatibility. The offset range between the signals is about 11ps. The offset between signals is due to the jittering effect of the HP data generator which has an upper limit of 10ps. The signal to noise ratio(SNR) is largely due to a large signal being applied to the circuit thus providing good characterization of the circuit under test. The amplitude of the measured data can also be increased by increasing the amplitude of the sampling signal. However

this will also increase the non-idealities thus reducing the accuracy presented by measured data.

5.4.2 Measurements of the BiCMOS Integrated Circuit

In this section, measurements on a chain of inverters are presented. The design was fabriacted on Nortel's 0.8 μm BiCMOS technology [31]. A photograph and a schematic diagram of the integrated circuit are shown in figure 5.17 and 5.18, respectively.

Figure 5.17: Photograph of the BiCMOS inverter

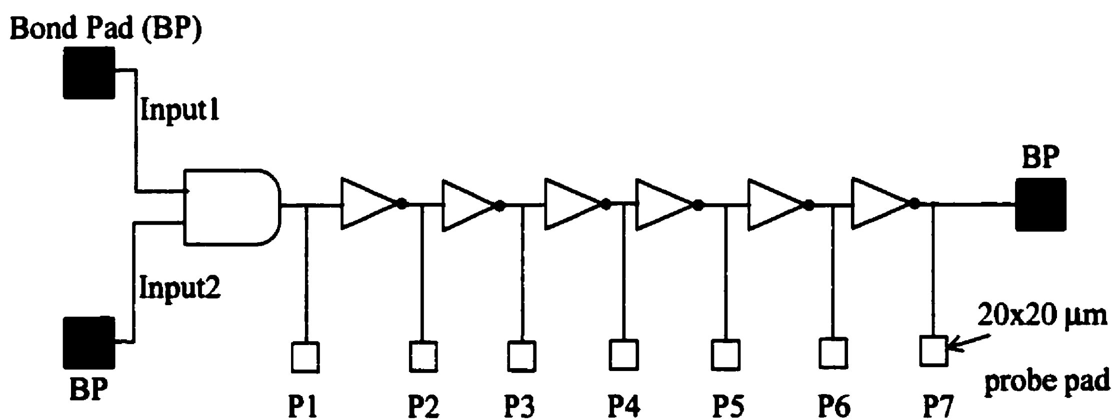


Figure 5.18: Schematic view of the BiCMOS inverter

The p-channel FET of this inverter has a gate width of 11.8 μm and the n-channel's gate width is 8.8 μm. For contact probing purpose, the 20 μm x 20 μm probe pads were added to the circuit. Measurements at the internal pads were obtained by applying a 8 bits, 0.5 Gb/s digital pattern (1010) at input1. A 5V dc is fed to the other input2 for power supply. The simulation result, EFM measured data and the contact probe at pad 1 are shown in figure 5.19 a, b and c respectively.

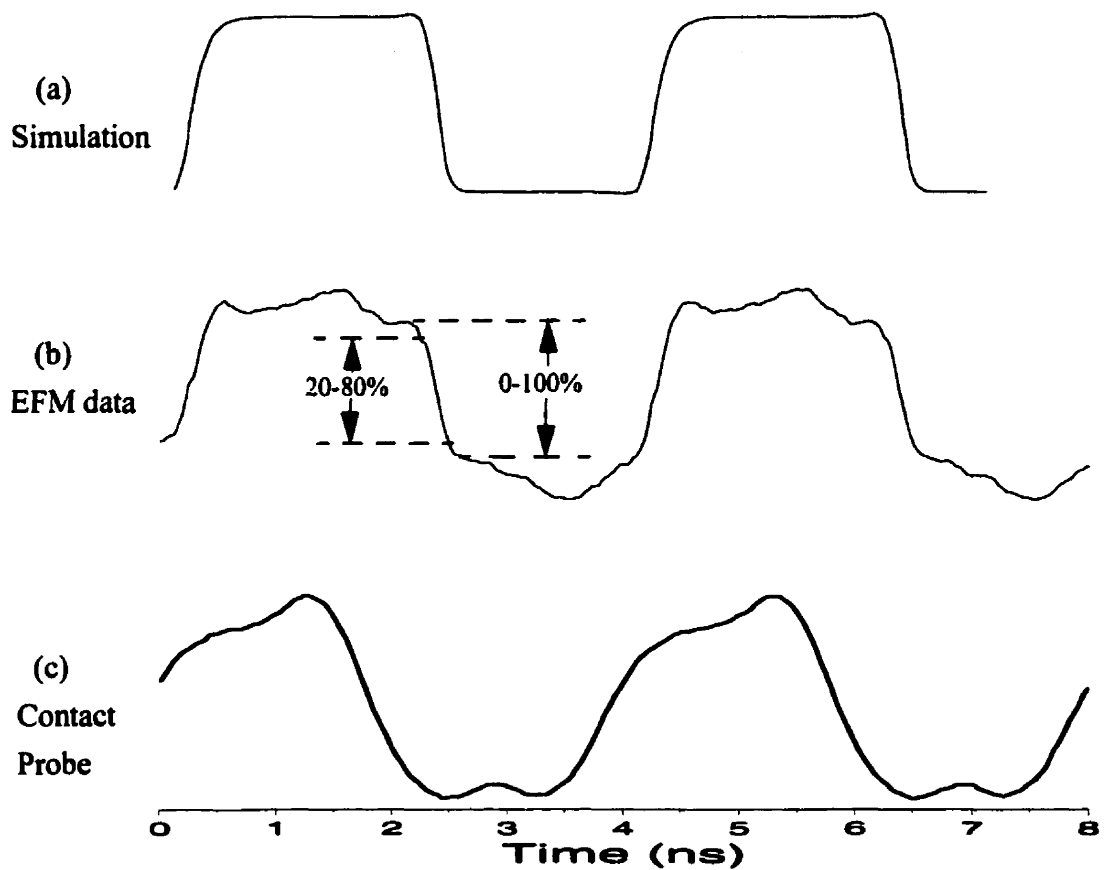


Figure 5.19: Measurement of 8 bits, 0.5 Gb/s digital pattern (1010) at pad 1. The simulation (a), EFM data (b), and contact probe [32] (c) results are shown.

Simulation outputs were obtained by simulating the circuit using Cadence SpectreS(software simulation tool). The EFM measured data were taken with a sampling shift increment of 10ps. The measured data are subjected to a 10 pts smoothing routine. Large ringing at the high and low logic of the EFM measured data can be related to the non-idealities of the sampling pulse. The ringing can also be attributed to the bond wire with in the integrated circuit. Again the results are normalized to 0 and 1. The 20%-80% rise and fall time of the simulated output is estimated at 184ps and 164ps respectively. The difference is due to the asymmetric gate width of the p and n channel of the FET. The 20%-80% (illustrate in figure 5.19b) rise time of the measured data is estimated at 204ps while the fall time is approximated at 188ps. The poor rise and fall time of the contact probe's result is attributed to the bandwidth limitation (1GHz) of the contact probe method.

Next, the simulated, EFM and contact probe data at pad 1, 3, and 5 are presented to characterize the propagation delay introduced by the inverters. These are shown in figure 5.20 a, b, c. A 4 bits (1010) at 0.5 Gb/s digital pattern is applied to the circuit and data were taken with a sampling shift increment of 10ps. Measurements of the propagation delay were extracted at the middle of the rise and fall edges. The delay between each pad of the inverter circuit is simulated to be 190ps. The delay as measured by using the EFM data is estimated at 161ps. The contact probe method provide poor data due to the parasitic loading capacitance.

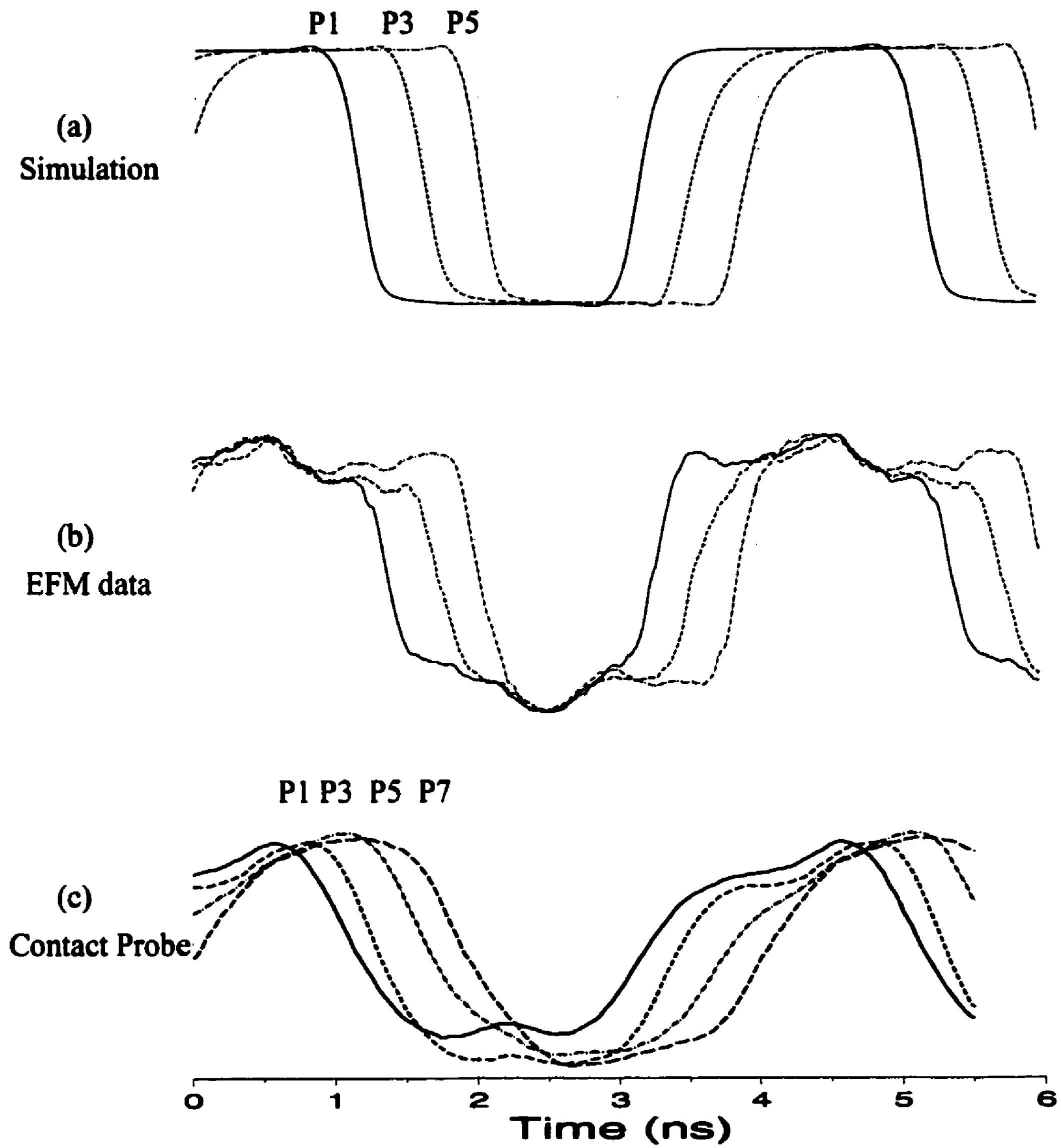


Figure 5.20: Propagation delay measurements from the sinulation (a), EFM data (b) at pad 1, 3, 5 along with the contact probe (c) [32] at pad 1, 3, 5, 7 results are shown.

5.4.3 Measurements of the CMOS Integrated Circuit

This section presents the measurements on the chain of CMOS inverter. The design was fabricated on CMOS technology. A photograph and schematic view of the circuit are shown in figure 5.21a, b, respectively. In figure 5.21a, pad 7 of the inverter is not shown, however it provides a photographic view of the circuit.

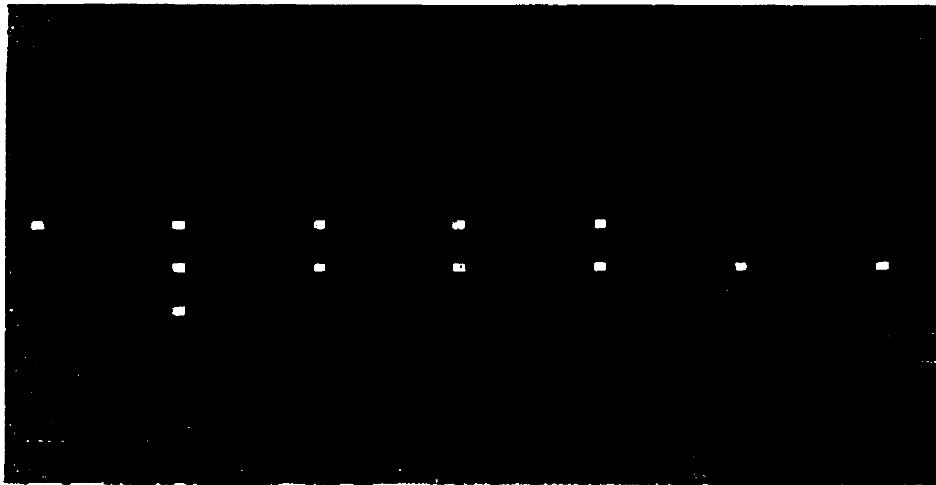


Figure 5.21a: Photographic view of the CMOS inverter chain

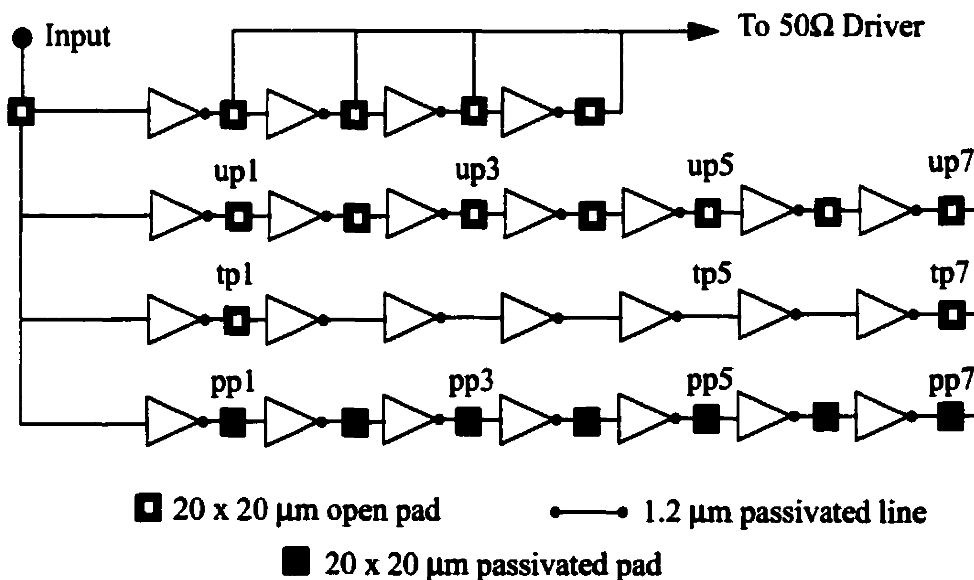


Figure 5.21b: Schematic view of the CMOS inverter chain

The gate width for both the p and n-channel FET of the inverter is 0.5 μm. A 1.2μm t-line is used to connect the output of one inverter to the input of another. The second row of the cicuit contains a chain of inverters with 20 x 20 μm unpassivated pads at the output of each inverter while the fourth row of the circuit is a chain of inverters with 20 x 20 μm passivated pads. Row 3 is a chain of inverters with no probing pads. The Vdd voltage of the circuit is 3.3 V. By applying a 8 bits, 0.5 Gb/s digital pattern (1010) at the input, measurements at the internal pads were recorded. The simulation result, EFM data, and the contact probe at pad up1 are shown in figure 5.22 a, b, c.

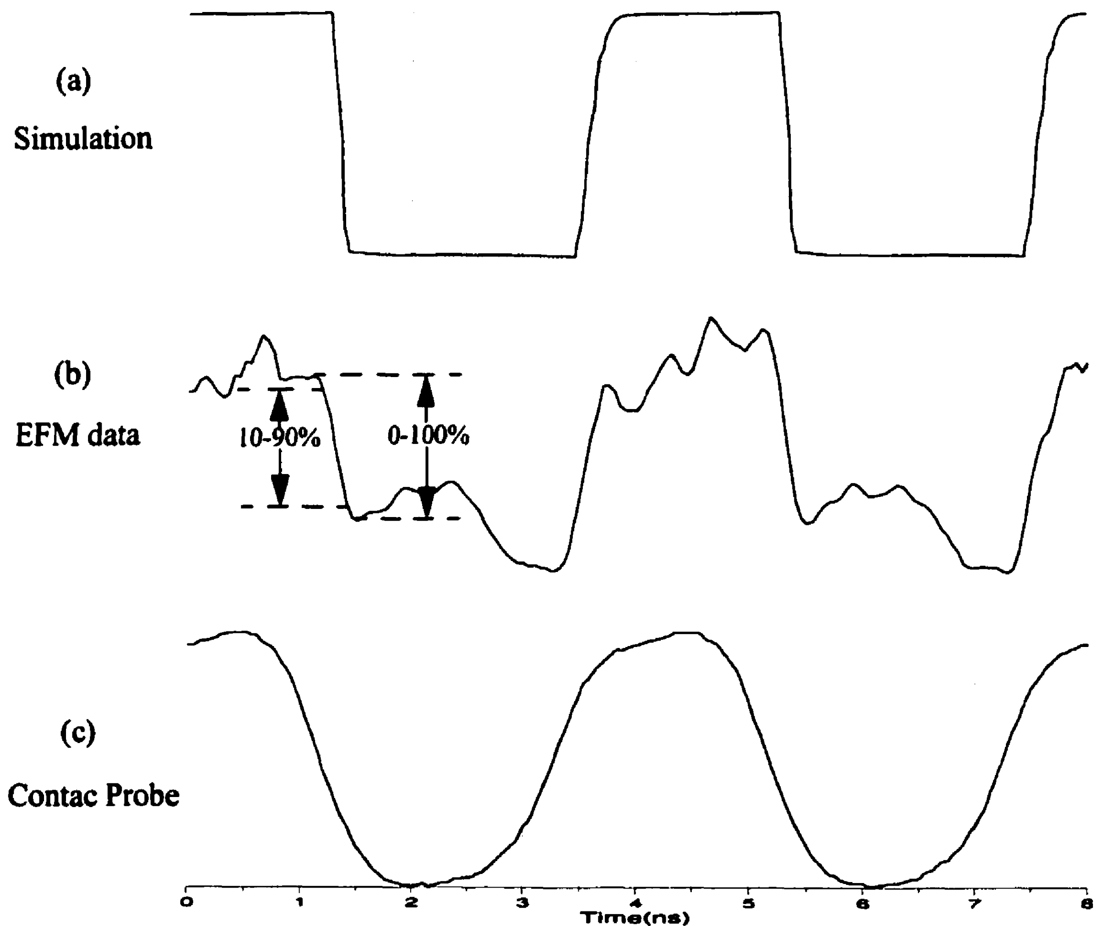


Figure 5.22: Measurements of a 8 bits, 0.5 Gb/s digital pattern (1010) over unpassivated pads. The simulation (a), EFM data (b) (3 pts smoothing), and contact probe (c) results at pad up1 are shown.

Hspice (simulation tool) was used to simulate the inverter chain. The EFM data were taken with a sampling increment of 50ps and are subjected to a 3 pts smoothing. Large noises at the high and low logic of the measured data are due to the non-idealities of the sampling pusle and the bond wire effect of the integrated circuit. The 10%-90% rise and fall time is simulated at 230 ps and 115 ps respectively. The 10%-90% (illustrate in figure 5.22b) rise time of the measured data is estimated at 271 ps while the fall time is approximated at 212 ps. The contact probe result has poor and rise time compare to that of the simulation.

Next the propagation delay introduced by the inverters is characterized by measuring the data at pad up1, up3, up5, up7. Results from the simulation, EFM, and contact probe are shown in figure 5.23 a, b , and c. A 4 bit, 0.5 Gb/s digital patter (1010) is applied to the inverter chain and data were taken with a sampling shift increment of 50 ps. The EFM data is subjected to a 3 pts smoothing. The propagation delay introduce by each inverter is simulated to be 90 ps. The measured propagation delay using the EFM data is estimated at 92 ps. The delay estimated by the contact probe results is 85 ps.

Since the EFM is a non-invasive technique, data over passivated pads are able to be measured. To verify this, the chain of inverters which contains the passivated pads were measured and characterized. Also measured were the chain of inverters which only has a 1.2μm interconnect line. The EFM results at pad up5, tp5 and pp5 are shown in figure 5.24 a, b, and c. The measured data over the tline (tp5) and passivated pad (pp5) are closely resembled to that at the unpassivated pad (up5).

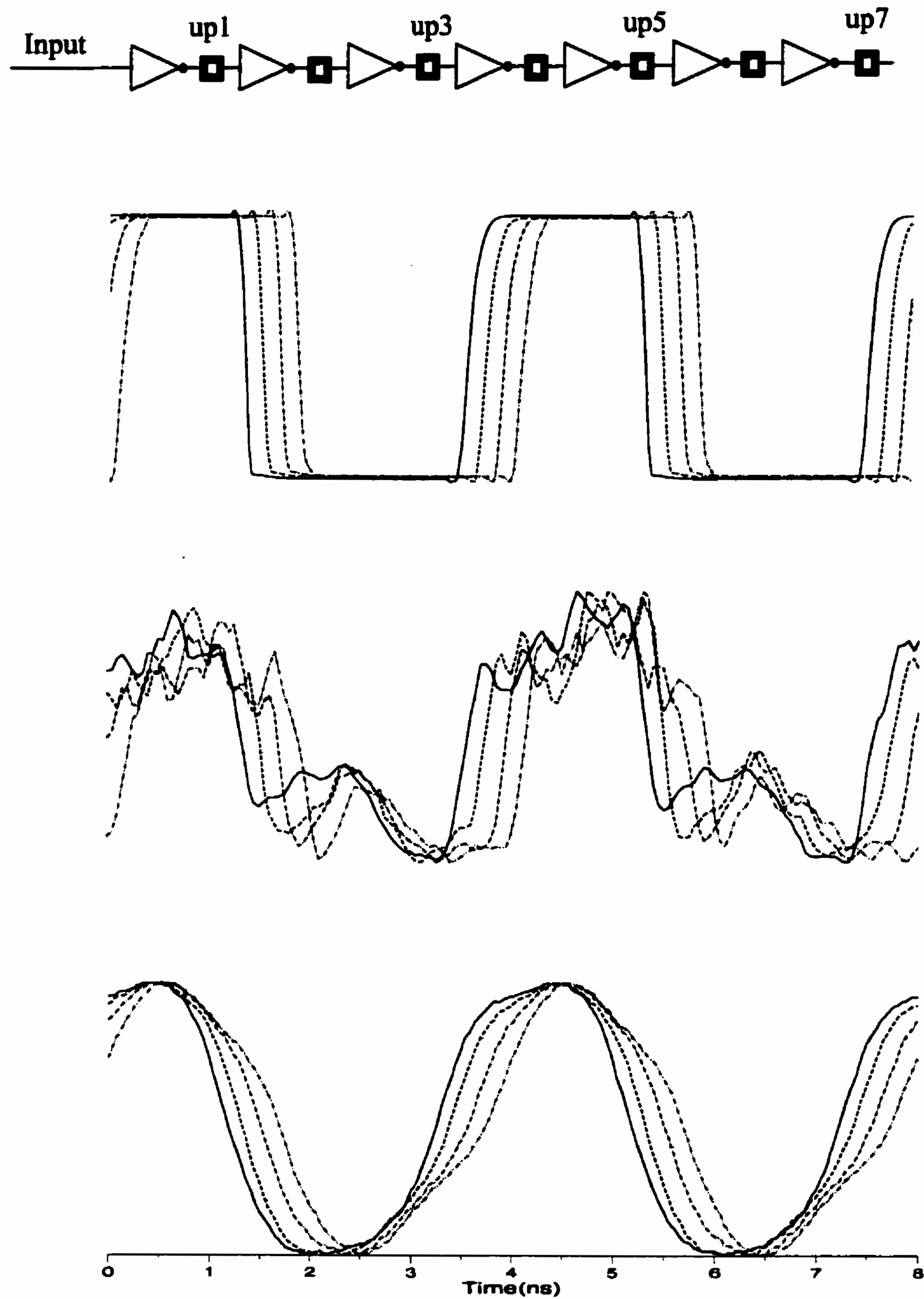


Figure 5.23: Propagation delay measurement over unpassivated pads. Results from sinulation (a), EFM (b), and contact probe (c) are shown.

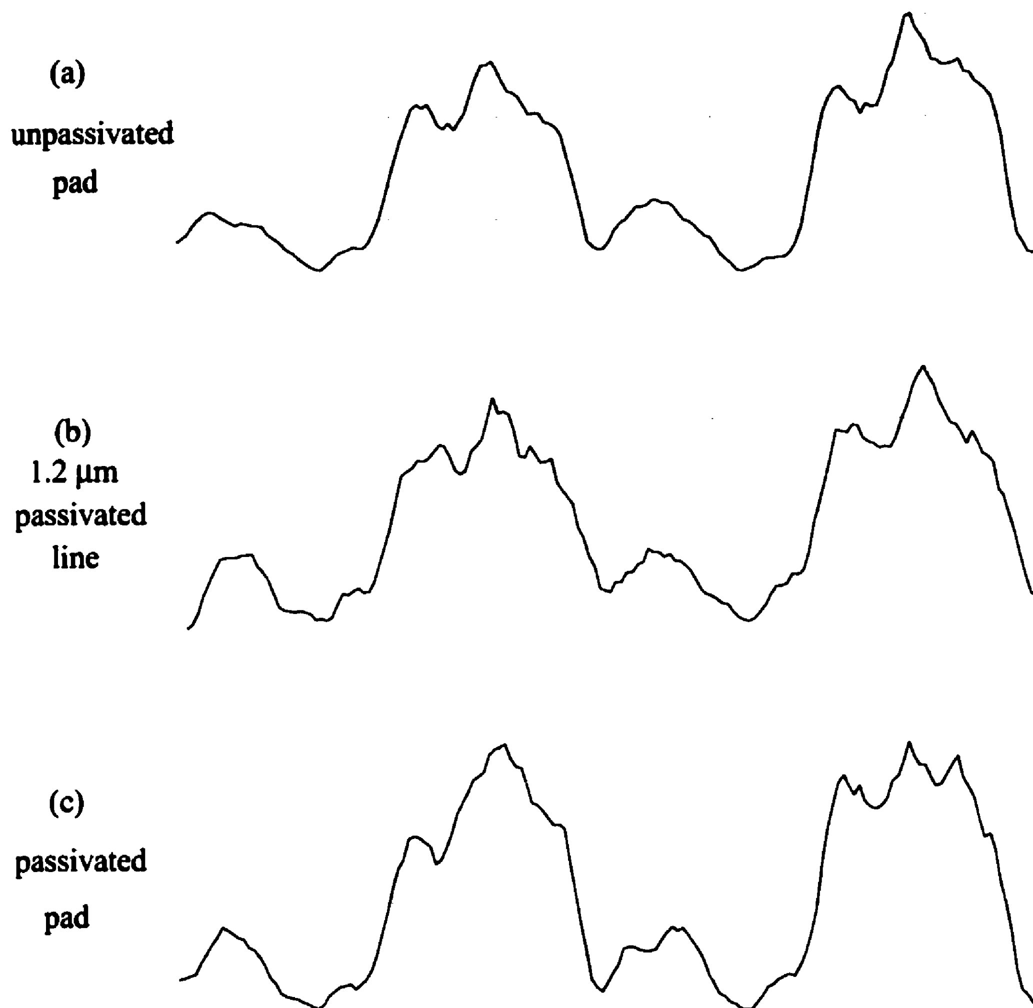


Figure 5.24: Measurement of an 8 bits, 0.5 Gb/s digital pattern. Results from the unpassivated pad up5 (a), 1.2 μm passivated line (b), and passivated pad pp5 (c) are shown.

Finally, the propagation delay across each passivated inverter pad is investigated. This is done by measuring the data at pad pp1, pp3, pp5, and pp7. The simulation, and EFM results are shown in figure 5.25 a, b.

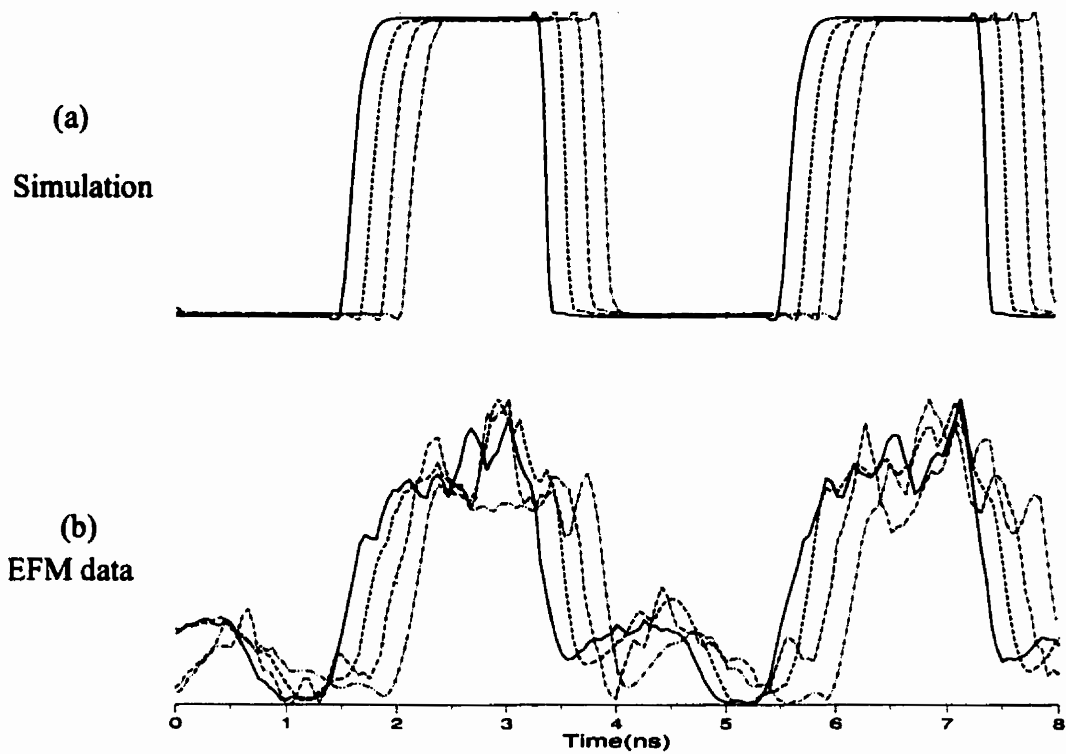


Figure 5.25: Propagation delay measurement over passivated pad. Results from simulation (a), and EFM (b) are shown.

The propagation delay across each inverter of the EFM data taken at the passivated pads is estimated at 93 ps.

CHAPTER 6

CONCLUSION

A brief discussion on the operating principle of the existing techniques for internal testing of Integrated Circuits were presented. Evaluation of each technique in term of their advantages and disadvantages were also discussed.

An electrostatic force microscope based, instrument for internal measurements of high frequency signals was analysed. A brief history of the SPM along with main idea behind the operation of the EFM were discussed. Characterization of the probe's mechanical properties along with the deflection sensor were presented. The spatial resolution, invasiveness, and voltage sensitivity of the presented instrument were determined to evaluate its performance. Using amplitude modulation and mixing of signals, a heterodyne technique was implemented. By incorporating the nulling method into the heterodyne technique, absolute voltage measurements were possible.

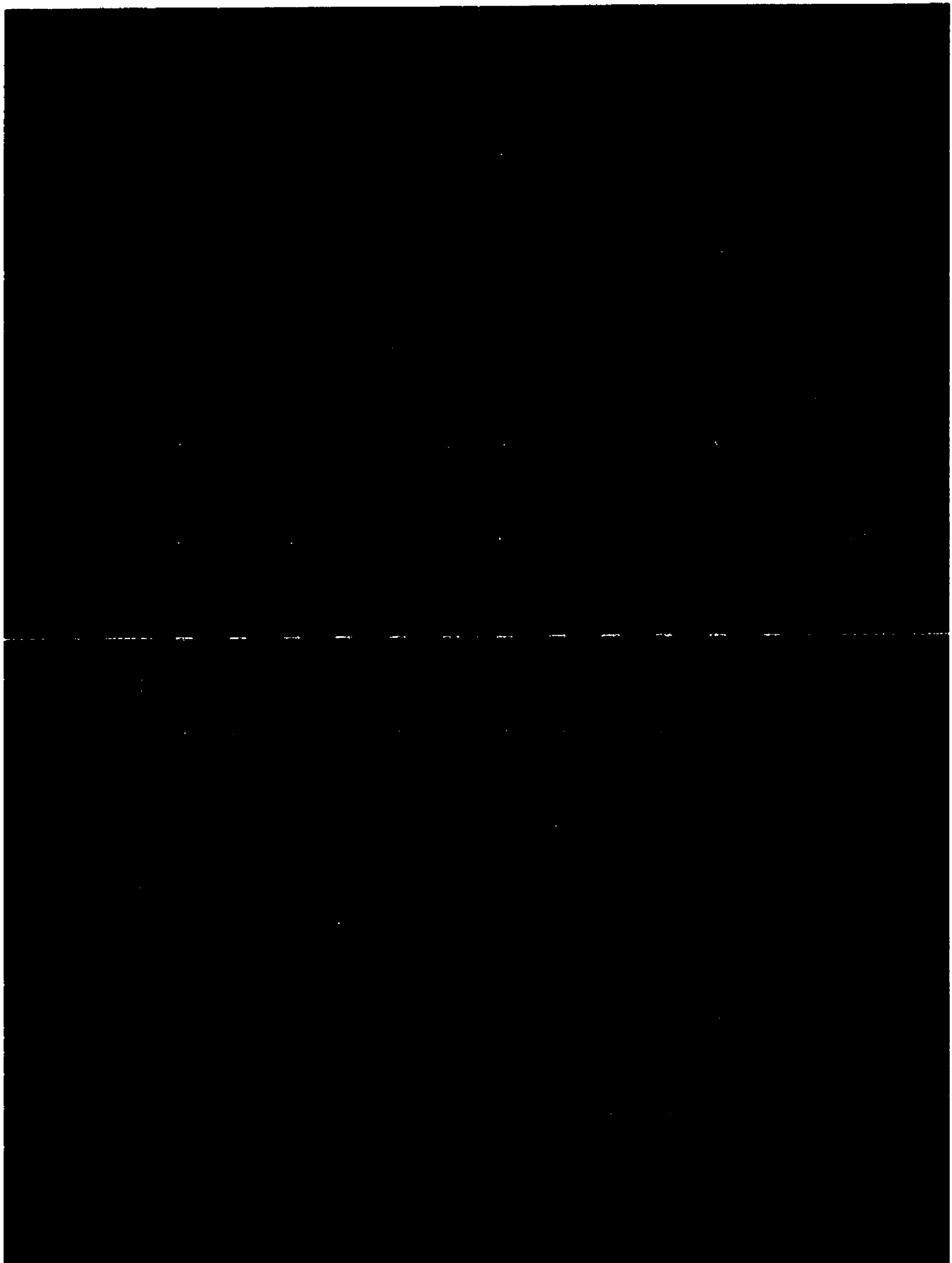
Three narrow pulse generation techniques were discussed. The theory behind the operating principle of the non-linear transmission line was described. An Integrated Circuit non-linear transmission line was designed, fabricated (by CMC) and tested. The experimental results compared well to those calculated. The low amplitude at the output is due to the low frequency packaging style used by CMC. The AND gate method was also

tested and 150 ps FWHM was obtained. The operation of the impulse generator method was briefly described. 120 ps FWHM pulses were obtained from this method. A high pass filter was used to eliminate the fundamental harmonic non-ideality of the output pulse. The output of the impulse generator method was used as a sampling pulse in the pattern extraction technique.

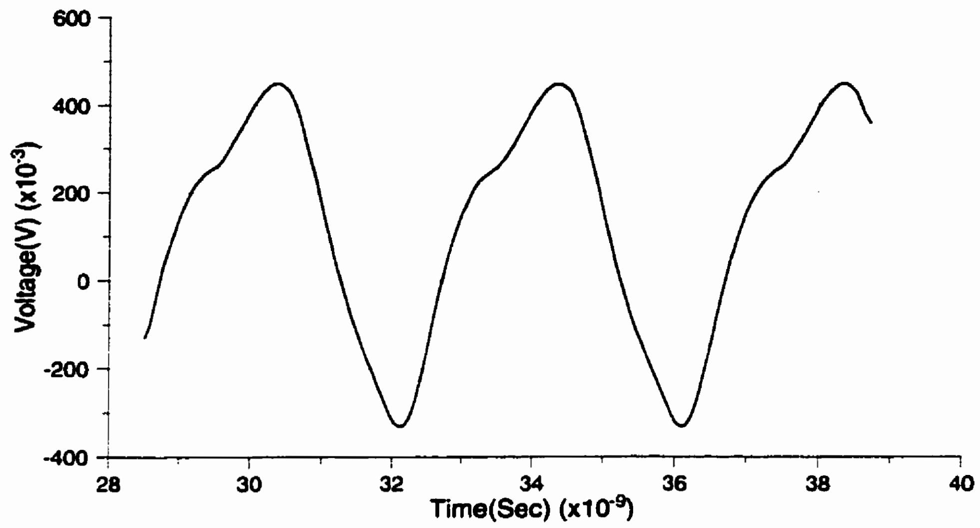
The heterodyne pulse sampling technique for high frequency digital pattern was described in detail. The specified test pattern was able to be extracted by shifting its entire N-bit pattern to enable sampling with the probe's pulse. A square wave amplitude modulation was used to implement the technique. The voltage sensitivity of this technique was calculated to be 16.2 mV with a measurement bandwidth of 1 Hz. The non-idealities of the sampling pulse were characterized. The use of sampling pulse with less non-idealities was found to provide much better data. Performance of the technique was evaluated on a 50Ω transmission line. Experiments involving digital patterns up to 1 Gb/s were performed. The technique demonstrated excellent rise and fall time measurement. The technique has a propagating delay measurement capability accurate to within 20 ps. Propagating delay of the BiCMOS along with the CMOS integrated circuits was conducted. The experimental results compared well with those of the simulation. Experiments over passivated pads were also conducted and results shown excellent agreement with those obtained over the unpassivated pads.

Appendix

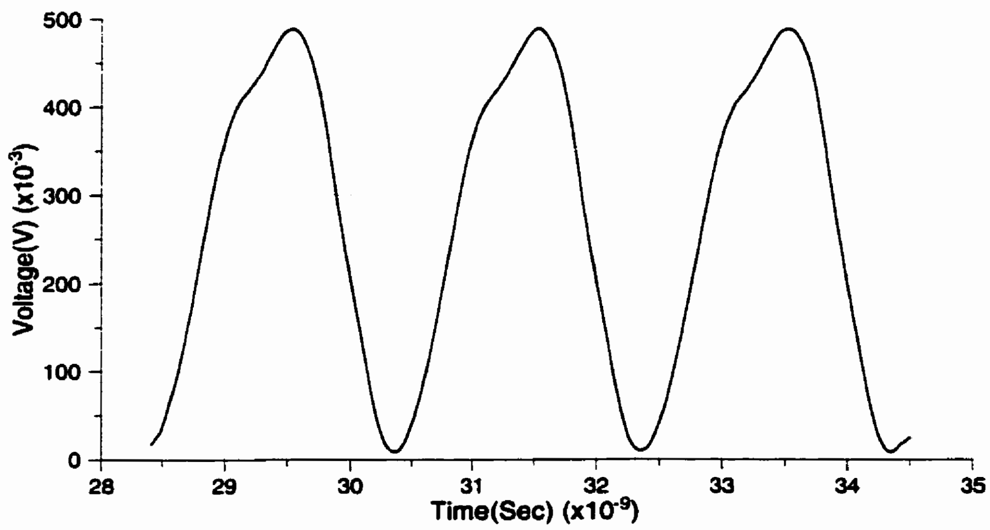
This appendix contains a full layout of the IC NLTL and its output waveforms. The output waveforms of the non-linear transmission line are recorded from the digital scope. The period and fall time of each waveform are specified.



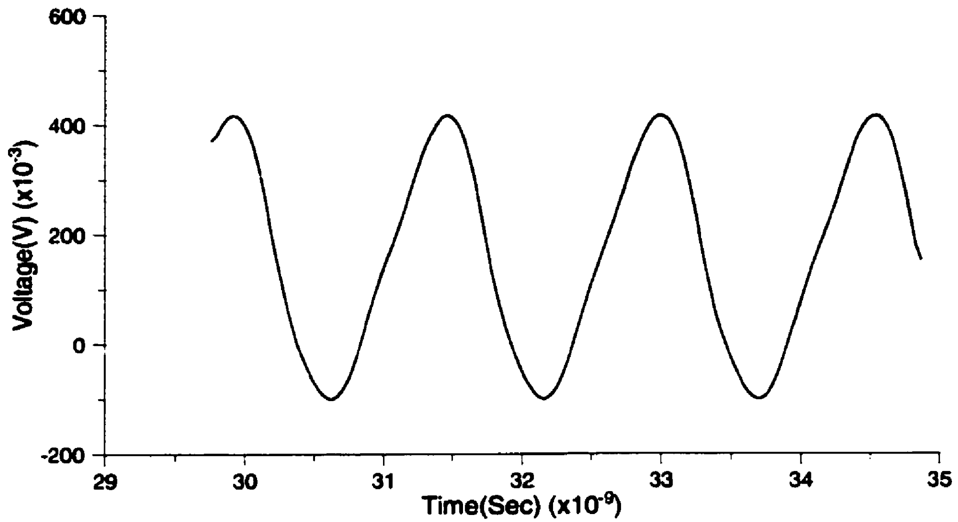
Full layout view of the IC NLTL



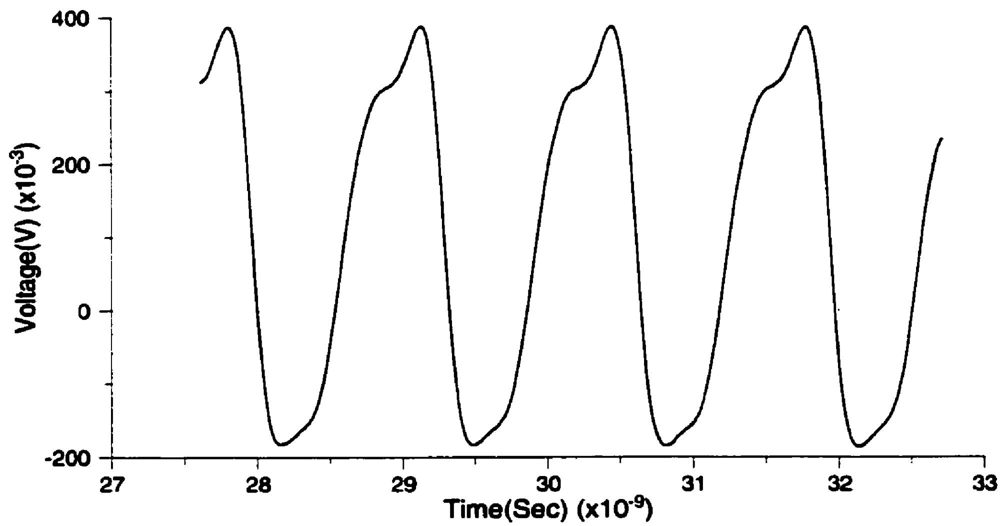
Period = 3.986 ns Falltime = 1.72 ns



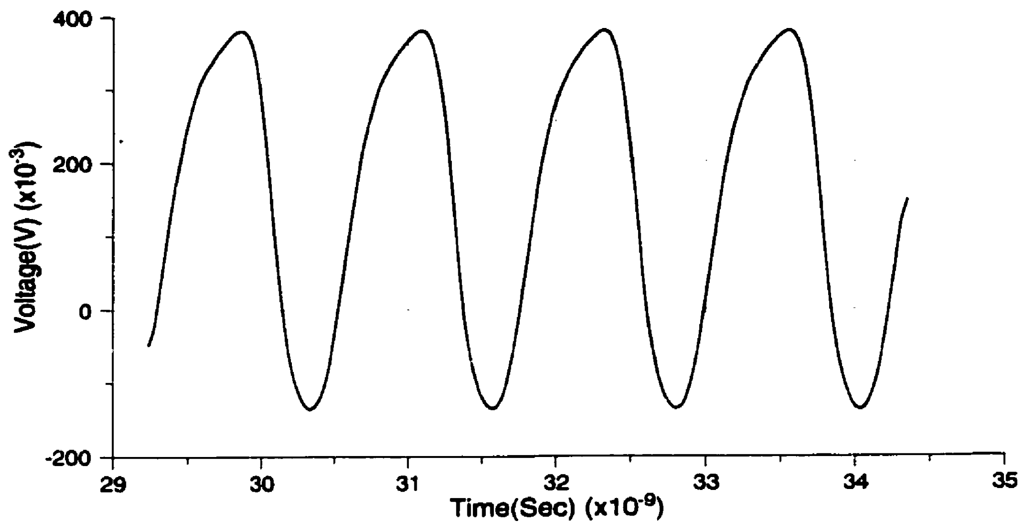
Period = 2ns Falltime = 820 ps



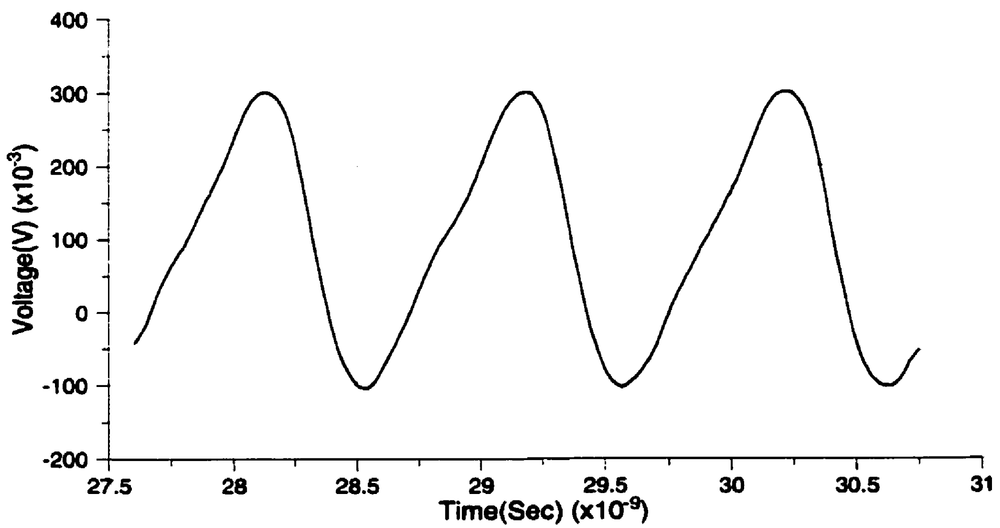
Period = 1.539 ns Falltime = 640 ps



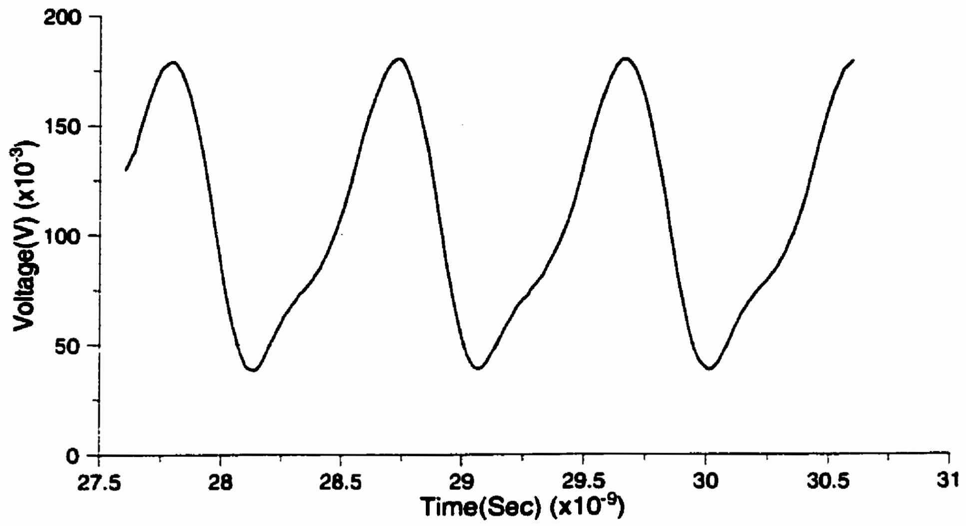
Period = 1.325 ns Falltime = 360 ps



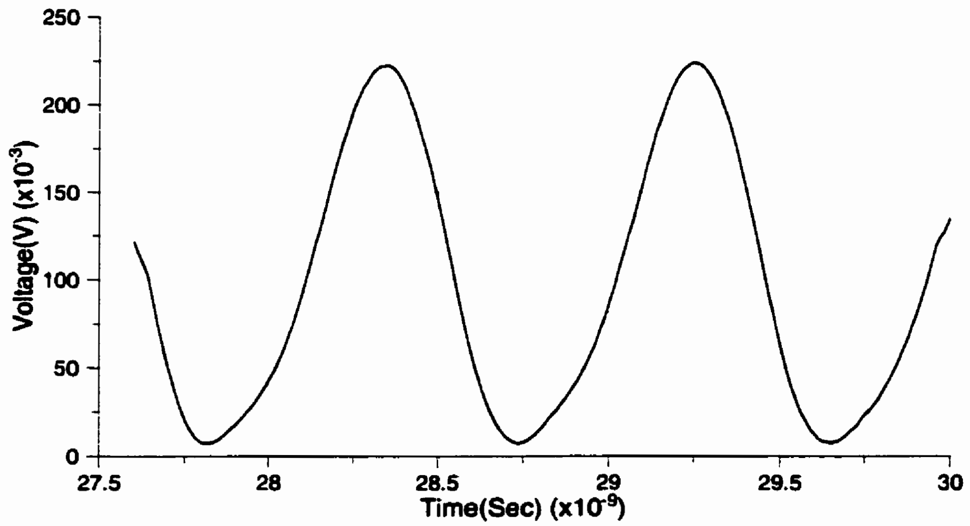
Period = 1.233 ns Falltime = 420 ps



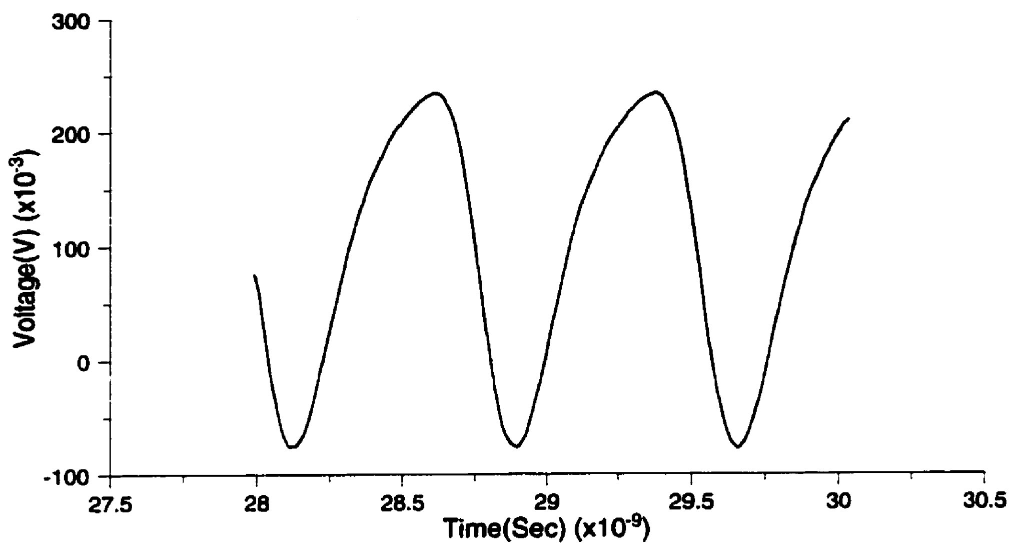
Period = 1.031 ns Falltime = 335 ps



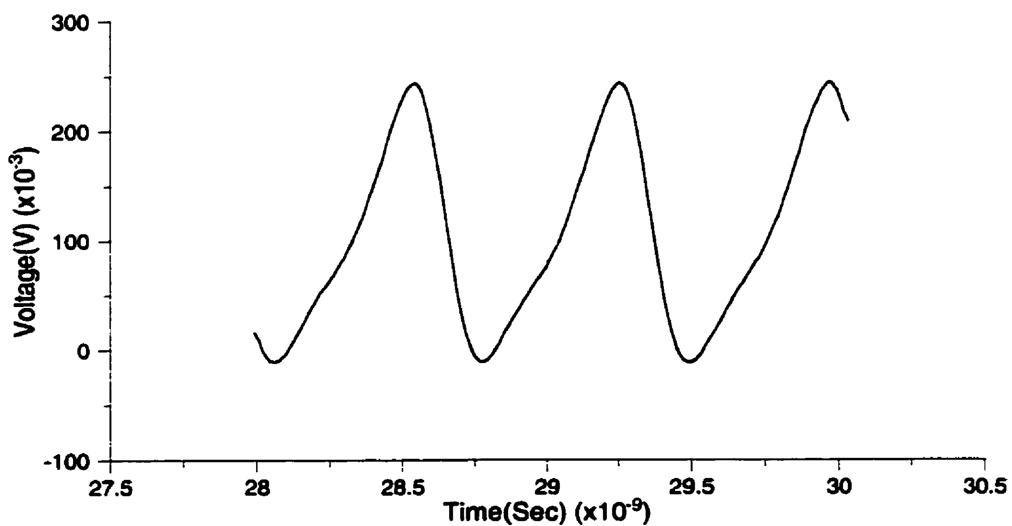
Period = 935 ps Falltime = 300 ps



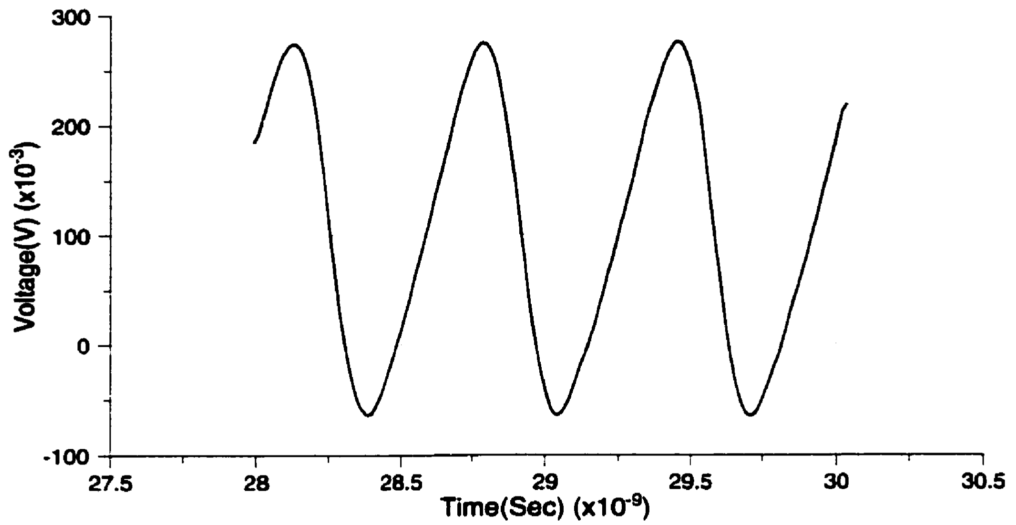
Period = 909 ps Falltime = 360 ps



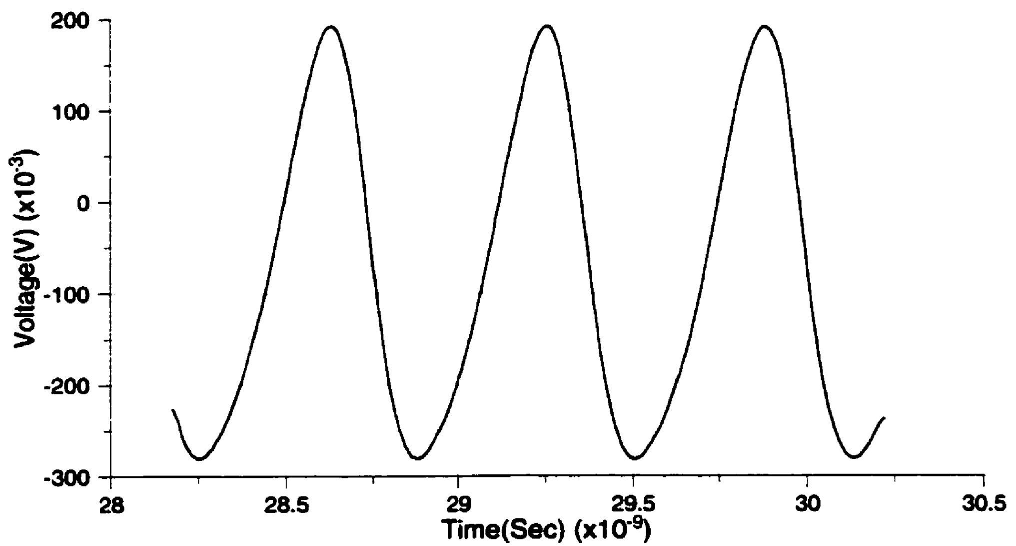
Period = 769 ps　　　　Falltime = 260 ps



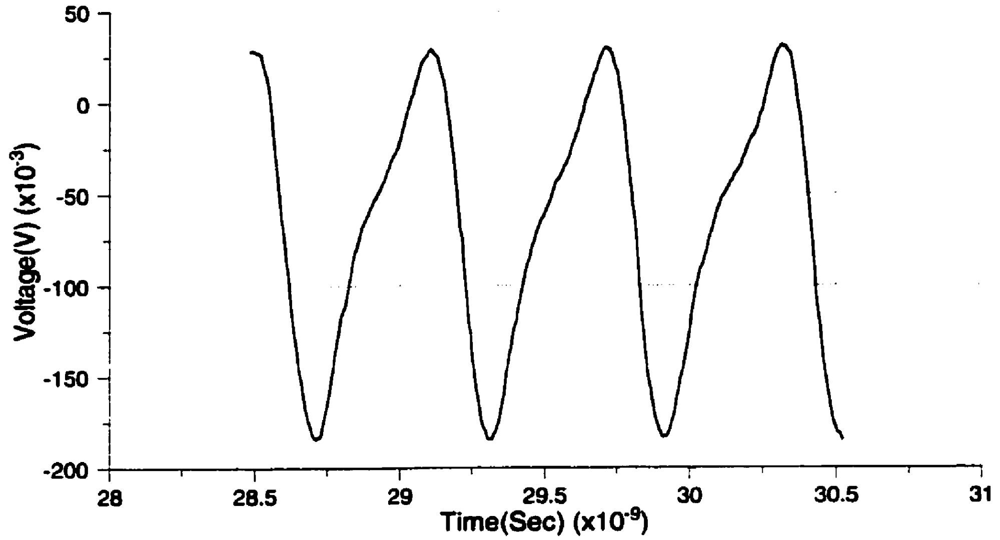
Period = 714 ps　　　　Falltime = 210 ps



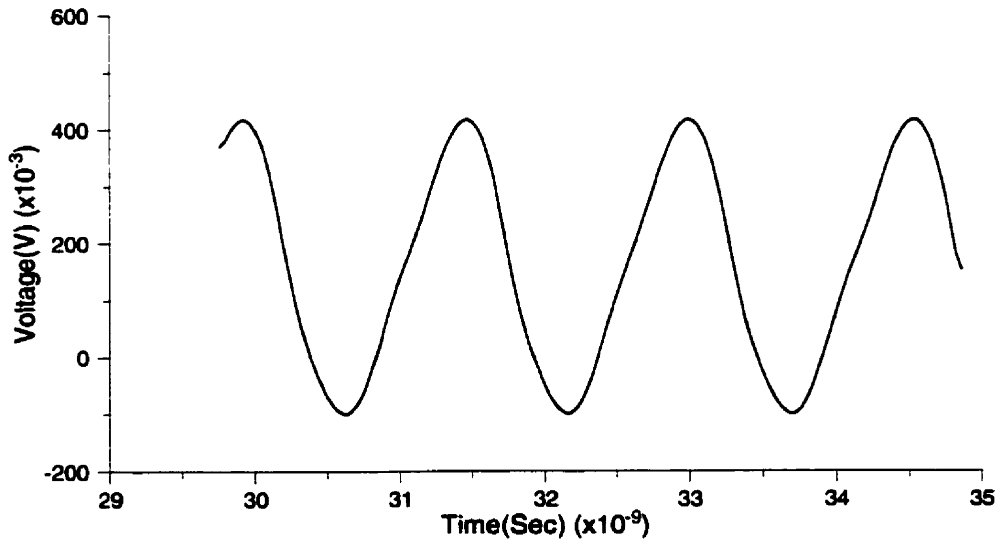
Period = 667 ps Falltime = 230 ps



Period = 625 ps Falltime = 225 ps



Period = 606 ps　　　Falltime = 180 ps



Period = 588 ps　　　Falltime = 230 ps

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