Improved Discrete-Time Switch Model for Electro-magnetic Transient Simulation of Voltage Sourced Converters

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Abstract

Switch modeling has always been a challenge in Electro-Magnetic Transient (EMT) type simulation. The commonly used traditional switch models are Resistor Switch Model (RSM) and Inductor LC Switch Model (LCSM). In the RSM, the on-state switch and off-state switch are modelled as a small and large resistor (R) respectively. In the LCSM, the on-state and off-state are represented by specially selected inductances (L) and capacitances (C) respectively. The RSM requires inversion of the system admittance matrix every time a switch operates resulting in a large computational burden. On the other hand, the admittance matrix remains invariant when switches operate for LCSM, thereby avoiding the computationally expensive matrix inversion.

Previous versions of the LCSM approach neglected the loss of stored energy in the L or C switch when the switch changed state. This resulted in a spurious switching loss. The purpose of this research is to develop new LCSM model, which permits efficient modelling of VSC topologies with large switch count and operating at high switching frequencies.

In order to develop the new model, firstly the spurious switching loss and oscillation are analyzed. Based on the analysis, an energy balance approach is developed to select the post switching current and voltage terms of LCSM so that the stored energy in the switch representation is continuous. This energy balance method helps to mitigate the spurious loss and oscillations in the simulation. In addition to energy balance approach, a new switch model, the RC/RL Switch Model (RC/RLSM) is also proposed. The RC/RL SM uses predictive subroutine and new configuration in order to avoid spurious losses and oscillations. For validation, EMT simulation cases using the proposed energy balance LCSM and RC/RLSM models in various

VSC configurations are simulated and compared with the RSM (assumed as the benchmark) for accuracy, losses and computational speed. The agreements of the resulting waveforms confirm that proposed models retain the simulation accuracy, show negligible switching loss and are extremely fast numerically.

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List of Acronyms

ac	Alternating Current
BEI	Backward Euler Integration
dc	Direct Current
DCMC	Diode Clamped Mutli-level Converter
dq0	Direct Quadrature Zero
LCSM	LC Switch Model
EMT	Electro-Magnetic Transient
GTO	Gate Turn Off
HVdc	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
MMC	Modular Multi-level Converter
NLM	Nearest Level Modulation

NPC	Neutral Point Clamped
PV	Photo Voltaic
PWM	Pulse Width Modulation
SM	Sub Module
SPWM	Sinusoidal Pulse Width Modulation
TLC	Two-Level Converter
TSA	Transient Stability Analysis
RSM	Resistor Switch Model
VSC	Voltage Sourced Converter

List of Symbols

C	Capacitor
C_{off}	Off-State Capacitor
C_{SM}	Submodule Capacitor
Δt	Simulation Time Step
G	Conductance
G_{SW}	Switch Conductance
G_{on}	Switch On-State Conductance
G_{off}	Switch Off-State Conductance
$homo$	Homogeneous Solution
i	Current
i_S	Current Source
i_L	Inductor Current
$i_{L_{on}}$	On-State Switch Inductor Current
i_C	Capacitor Current
i_{Coff}	Off-State Switch Capacitor Current

i_{0+}	Post Switching Switch Current
i_{0-}	Pre Switching Switch Current
i_d	d Axis Current
i_q	q Axis Current
i_{SW}	Switch Current
L	Inductor
L_{on}	On-State Inductor
L_{arm}	Arm Inductor
λ	Eigenvalue
λ'	Discrete Domain Eigenvalue
nrg	Energy
ω	Angular Frequency
$part$	Particular Solution
P_{off}	Off-State Switch Power
P_{on}	On-State Switch Power
R	Resistor
R_{off}	Off-State Switch Resistor

R_{on}	On-State Switch Resistor
T_{off}	Off-State Switch Period
T_{on}	On-State Switch Period
v	Voltage
v_S	Voltage Source
v_L	Inductor Voltage
$v_{L_{on}}$	On-State Inductor Voltage
v_C	Capacitor Voltage
v_{Coff}	Off-State Capacitor Voltage
v_{0+}	Post Switching Switch Voltage
v_{0-}	Pre Switching Switch Voltage
v_d	D Axis Voltage
v_q	Q Axis Voltage
v_{SW}	Switch Voltage
Y	Admittance

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1 Introduction

1.1 Background

Rapid development of power semiconductor switches have a major impact to everyday living. These are finding increasing usages in high power applications such as Voltage Sourced Converters (VSC). VSCs are commonly employed in High Voltage Direct Current (HVdc) transmission and Flexible AC Transmission (FACT) [1][2][3].

HVdc transmission is recognized for its ability to efficiently transfer power over long distances. Unlike the traditional alternating current (ac) transmission, line inductance and capacitance act as short circuit and open circuit elements in a direct current (dc) circuit, thereby greatly reducing the line impedance. dc is also able to interconnect networks with different frequencies [4][5][6].

Traditionally, the line commutated converter (LCC) is employed for HVdc operation [5][7]. LCC uses 12 pulse thyristor based Graetz bridges for power rectification and inversion. The thyristor bridge has the advantage of lower losses (in comparison with VSC alternatives) and uses more robust semiconductor devices capable of withstanding higher voltage and current stresses [8]. However, it has the drawback that the thyristor cannot be turned off by a control pulse. The turn off operation relies on the thyristor current's natural zero crossing from reverse biasing ac voltage. Hence the LCC is susceptible to "commutation failure". This is a phenomenon where the

outgoing thyristor valve fails to turn off and transfer its current to the oncoming valve when it should [8][9]. LCCs also have a poor power factor and require a large amount of reactive power (50%-60% of the real power at rated conditions)[6]. This reactive power must be provided by synchronous compensators, ac filters and shunt capacitors, which can escalate the cost and lead to problems such as load rejection over-voltages and harmonic instabilities.

Recently a new type of HVdc technology has emerged and grown ever popular. This is the self-commutated converter based HVdc. Examples include the HVdc Light technology from ABB or HVdc Plus from Siemens [7][10]. The self-commutated converter typically use VSCs. VSC employs fully controlled semiconductors to transmit electrical power. Unlike the LCC which has a mandatory lagging reactive power demand, the VSC can be used to control both bidirectional reactive and active power [7][8][9][10]. This means that VSC based HVdc can be directly connected to any load network, even one with a purely passive ac load. Besides self-commutation, the VSC can eliminate lower frequency harmonics by use of higher switching frequency and control the voltage levels [8][9]. The flexibility and quality of VSC based HVDC makes it a much more favorable option in the current power system market. It is evident that VSC is becoming more relevant in today's power system. This can be justified by the VSC installed capacity distribution throughout the past 18 years. From 2000 – 2005 only about 1% of the HVDC installed was VSC based. This ratio has increased to about 5% in 2006 – 2010, and about 10% in 2011 to 2015. In the period of 2016 – 2020 the VSC capacity ratio in HVDC network is expected to be about 25% and it is predicted in the year 2021 to 2025 this ratio will grow to 30% [11]. Based on the recorded growth of VSC based HVDC, one can anticipate the future of power system to be dominated by these self-commutating converters.

Renewable energy generation is another factor causing an increase in demand for VSC transmission. Rapid climate change and increase in earth pollution level has raised the awareness for clean energy. As a result, more and more renewable energy generation is being integrated into today's power network. Renewable energy sources tend to be located far away from the large load centers due to physical locations. A good example of this is wind power generation. Offshore wind turbines will generally yield 50% more energy than onshore ones and have a longer life span. This is due to lesser friction and lower turbulence in ocean locations [12]. LCC based transmission would have been a challenge in this case due to the weak (high impedance) ac network of the small isolated area and lack of a black start capability.

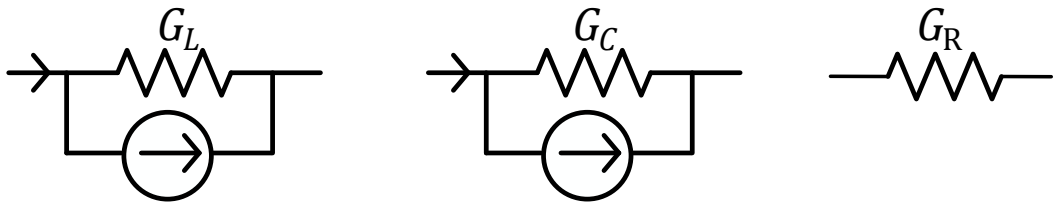
Besides wind power, another great example of renewable energy is photovoltaic (PV) generation. PV installation growth has been on a steady increase since 1986 [12]. Unlike hydro, wind, nuclear generation, the requirement for locating PVs is lax and this allows for installation in residential locations. In general PV cells can be grid connected or used to directly supply a passive load. Again, this forbids the use of the LCC type converters.

1.1.1 Electro-magnetic Transient Simulation

The control flexibility and lower system requirement makes VSC based HVdc more feasible in a wide variety of scenarios. However, simulation study and analysis must be conducted prior to commissioning of these devices. Typically, these type of simulation studies are done on Electro-magnetic Transient (EMT) simulators. EMT simulators represent the simulated case by modeling the

actual time domain behavior in detail [13], and can accurately reproduce the voltage/current transients. This is different from other simulation studies, for example transient stability analysis (TSA), in which the differential equations of the mechanical components (e.g., rotor dynamics of synchronous machines) are modeled, whereas the ac network is assumed to be in a quasi-steady state. They typically use a large time-step (5ms -10ms) and use a phasor-domain representation for the electrical network, which is recalculated in every time-step using the new excitation parameters as determined by the machine models.

EMT simulators discretizes the time domain equations of each circuit component and represents them as a companion circuit model consisting of an admittance in parallel with its history current term [14]. Examples of these components are the fundamental circuit component R, L, and C as shown in Fig. 1.1.



(a) (b) (c)

Figure 1-1 EMT model of passive elements a) Inductor; b) Capacitor; c) Resistor

The time domain equation (1.1a) for a capacitor can be discretized and represented as a difference equation (1.1b) using trazpoidal rule of integration, where i_C, and v_C is the capacitor current and v_C and capacitor voltage respectively.

$$C\frac{dv_C}{dt} = i_C \qquad (1.1a)$$

$$i_C[n] = \frac{2C}{\Delta t}v_C[n] - i_C[n-1] - \frac{2C}{\Delta t}v_C[n-1] \qquad (1.1b)$$

Equation (1.1b) can be separated into two components in terms of their time step. The present time step component, $i_C[n]$, $v_C[n]$ can be represented as admittance $\frac{2C}{\Delta t}$ and its voltage/current relation. On the other hand, the history time step component $i_C[n-1], v_C[n-1]$ can be represented as a parallel history current term to be injected into the current time step component and use to find $i_C[n]$. Once $i_C[n]$ is found it can be used to redefine as the $i_C[n-1]$ for the next simulation time step. This process will iterate until simulation ends. The inductor can be modeled in a similar way as shown by (1.2), where v_{L}, and i_{L} is the inductor voltage and current respectively.

$$L\frac{di_L}{dt} = v_L \qquad (1.2a)$$

$$i_L[n] = \frac{\Delta t}{2L}v_L[n] + \frac{\Delta t}{2L}v_L[n-1] + i_L[n-1] \qquad (1.2b)$$

The resistor's dynamic equation is not a differential equation therefore it can be directly

modeled in the EMT simulations as (1.3).

$$i_R[n] = \frac{1}{R} v_R[n] \qquad (1.3)$$

Once all circuit components are modeled as its EMT equivalent, simulation can be conducted by forming the admittance matrix, column vector of node voltages and branch currents as shown in equation (1.4). The column vector of node voltages is then solved by multiplying both side of (1.4) by the inverse of the admittance matrix as shown in (1.5). Although a faster method such as L-U factorization is usually used instead of an explicit inversion, it nevertheless is one of the more time-consuming processes. Operation of switches causes the refactorization to be initiated, and can slow down the simulation.

$$[Y][V] = [I] \qquad (1.4)$$

$$[Y]^{-1}[I] = [V] \qquad (1.5)$$

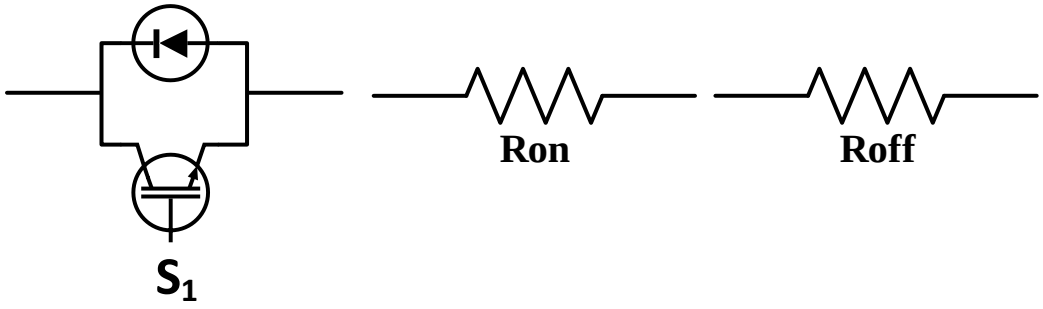
EMT simulators are categorized into real-time simulator and off-line simulator. The key points to differentiate the two simulators are the simulator speed and simulation output. In off-line simulation the run duration is defined prior to start of simulation, and all simulation results can be cached and presented to user at end of the simulation. On the other hand, real-time simulations are

meant to be ran continuously until termination by user. Simulation results are also required to be computed in the same amount of physical time as the set simulation time step. Due to the flexibility and less hardware requirement, the off-line EMT simulators are typically used for system studies. While the advantage of the real-time simulators allow physical power system controller/equipment to be tested by performing hardware in the loop testing (HIL) [15].

One of the challenges in EMT type simulation is semiconductor switch modeling. When one examines semiconductor switches in detail, different switches will have different behaviors due to specifications, materials and structures. It has been shown detailed semiconductor switch can be model using a finite state machine method in [16][17][18]. However, this approach has a hard limitations on memory usage, thus the amount of switch in the simulated network is limited. Also, a new state machine must be re-defined each time when simulating new topology. For most applications a simplified switch model is sufficient for simulation and test purposes [19]. When modeling VSC networks on the EMT simulator a major problem is to maintain the required high simulation speed. This is due to its fundamental components, the switches. Switch modeling has always been a complication in EMT type simulation programs due to the inherent nonlinear characteristic of the device, as every switch operation results in a change in the Y matrix and invokes the time-consuming refactorization process. Two widely accepted switch models commonly used today are the Resistor Switch Model (RSM) and the LC Switch Model (LCSM) [20][21]. Each having their own pros and cons.

1.1.2 Resistor Switch Model

The RSM represents the switch as a small resistor 'R_{on}' when the switch is in the on-state, and as a large resistor 'R_{OFF}' when the switch is in the off-state [13]. An example of the RSM is shown in Fig 1-2.



(a) (b) (c)

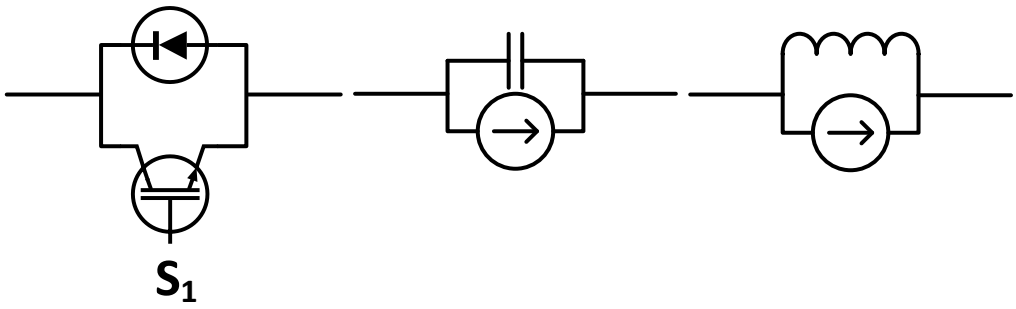
Figure 1-2 RSM switch model a) General bi-directional switch; b) On-state representation; c) Off-state representation

RSM works well when the simulated network contains a small number of switches. However, problems are encountered when the simulated network becomes larger. This is due to the variable switch admittance between the two switching states. Every time a switching action is performed, the simulated topology changes and a refactorization process is needed to obtain inverse of the new system admittance matrix [22]. For a large system this refactorization process can be computationally intensive, and requires a long computation time [23]. To reduce the computation time, particularly in some real-time simulators, one sometimes pre-inverts and stores all possible system admittance

matrices during initialization of simulation. However, this is not practical because for a system of N switches the number of possible matrices to be stored is 2^N [19]. Despite the fact RSM's noticeable drawback many users still prefer this for the high quality simulation waveforms and accurate dynamic behavior. In this research RSM will be used as the benchmark model for the testing and verification propose.

1.1.3 LC Switch Model

Beside RSM another notable switch model is LCSM. The LCSM represents switch as a Dommel's Companion Circuit, where an admittance is in parallel with a current source [14]. When switch is in the on-state, the circuit behaves as a small inductor 'L_{on}'; when switch is in the off-state, the circuit behaves as a small capacitor 'C_{off}'. An example of LCSM is shown in Fig 1-2



(a) (b) (c)

Figure 1-3 LCSM switch model a) General bi-directional switch; b) Off-state representation c) On-state representation

Switch admittance of LCSM is set such that the on-state admittance is equal to the off-state admittance. Therefore, system admittance matrix will not change regardless of switching. As a result, there will only be one system admittance matrix. The benefit of having one system admittance matrix is that there is no need for refactorization during every switching event. Therefore, one can just pre invert the system admittance matrix once during initialization of simulation and store it. The amount of computation saved compared to RSM is also 2^N where N is the number of switches in the network. For a large switch network this saving becomes enormous. In spite of all the benefit LCSM offers, it also has some serious drawbacks. Since the switch is modeled as 'L_{on}' or 'C_{off}', when switches are operating there is always spurious stored energy. As a result, when a switch transitions from on-state to off-state or vice versa, its representation changes from 'L_{on}' to 'C_{off}' or 'C_{off}' to 'L_{on}', which can result in generation of a spurious energy loss unless handled carefully. Also, the charging of the 'L_{on}' and 'C_{off}' elements to re-establish the stored energy level adds a delay to switching response and can produce spurious oscillations [24].

1.2 Motivation

The increasing popularity for VSC in both high and low power applications drove the rapid development in new topology and control methodology. One noticeable trend in the developments is increase in switch count and switching frequency [25][26]. Increasing switch count is seen more often in high power applications due to the high voltage magnitude. Voltage stress can be shared amongst each individual switch making the realization of the high voltage VSC possible. On the other hand, increased switching frequency can produce higher quality waveforms and reduce the size of magnetic

components in the VSC [27]. All these trends reflect as positive improvements in VSC technology but prove to be challenges from the EMT simulation perspective.

To effectively simulate high switching frequency the simulation time step needs to be much smaller than the switching period. In addition to smaller time steps, the increase of VSC complexity also means more component needs to be simulated. As a result, the amount of computation load is greatly increased. The simulation time for a large network with power-electronic switches can take hours even days just for a few seconds of run duration [28]. This hinders the process of power system analysis and development. In cases where there is a need for high-speed simulation, such as in real-time simulators, it may even become impossible to perform the simulation.

To accommodate for state of the art VSC technologies, a faster and more efficient switch model needs to be developed.

1.3 Objective

The main objective of this research is to develop an improved LCSM for EMT type simulation program such that its spurious loss and oscillation characteristic will be suppressed while maintaining its fast simulation characteristics.

In order to reach the goal of this research, objectives has been completed in the following chronological order:

1. Analyze spurious loss and oscillation characteristics of traditional LCSM, identify its cause and come up with mathematical representations.

2. Propose a solution to suppress the spurious loss and oscillation in the traditional LCSM.

3. Implement VSC using the proposed solutions.

4. Validate and compare simulation results between proposed solutions to traditional LCSM and benchmark RSM.

1.4 Outline

The outline of this thesis follows the order below:

Chapter 2 introduces various VSC topologies. This includes their structure and controls which will be used for implementation and testing of proposed switch model.

Chapter 3 identifies the cause of spurious loss and oscillation in traditional LCSM

Chapter 4 proposes a method to suppress the spurious loss and oscillation problem in LCSM, and a complete new constant admittance based switch model.

Chapter 5 explains how proposed method and switch model is implemented in VSC test circuits using a detailed step by step procedure.

Chapter 6 presents the validation of VSC simulation using proposed solutions. Simulation results are compared to traditional LCSM and benchmark RSM.

Chapter 7 concludes this thesis and propose a list of future work.

2 Voltage Sourced Converter

As discussed in chapter 1 the voltage sourced converter (VSC) use semiconductor devices such as insulated gate bipolar transistors (IGBT) and gate-turn-off thyristor (GTO) capable of self turn-on and turn-off to perform rectification and inversion of electrical power [29]. One of the earliest VSC topologies Two-Level Converter (TLC) is still in current use [3]. The TLC has a simple topology, low switch count, and easy to control. However due to the limitation of voltage blocking capability of individual switches, this topology is typically only used in low voltage applications. To accommodate for the high voltage applications multilevel converter topologies were developed. One of the commonly known multilevel converter topology is the diode clamped multilevel converter (DCMC). The DCMC indeed is able to resolve the voltage blocking capability issue of switches but it has also brought in a new complication. Increasing voltage level also raises the number of interconnect diodes making its structure more complex. This makes DCMC less favored for higher voltage implementation. A demand for simpler structure, scalability and modularity construction is thus raised. In 2003 Modular Multilevel Converter (MMC) was introduced in [25]. The MMC is scalable, applicable for wide voltage range and suitable for modular construction. MMC has opened up a new era for VSC type HVdc ever since.

This chapter will discuss these classic VSC topologies and typical control which will be employed for HVdc operation.

2.1 Two-Level Converter

The TLC is the most basic VSC topology that can be employed in HVdc transmission, and is often known as the first VSC topology used in HVdc transmission. This particular representative work is known as the Hellsjön Project. The Hellsjön is a 3 MW bipolar HVDC operating at $\pm 10kV$ over $10km$ connecting Hellsjön and Grängesberg [30]. The TLC is made of two switches connected in series. Fig. 2-1 shows one phase of the TLC. Switch S1/D1 connects the load to the positive dc voltage and S2/D2 to the negative voltage. By operation of these switches an alternating voltage is applied to load. The load voltage harmonics can be mitigated using high frequency pulse width modulation [31].

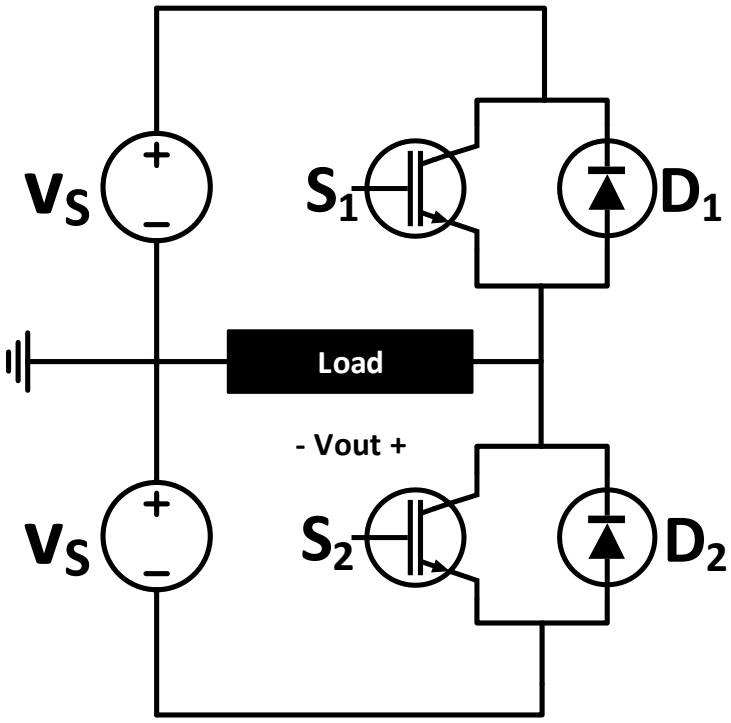


Figure 2-1 Structure of a TLC

As its name suggests the TLC can only produce two voltage levels, positive and negative. However, since there is an anti-parallel diode across every switch the TLC will have 4 operating modes. The switch state associated with each voltage level is tabulated below.

Table 2-1 Two-Level Converter Switch States Map

operating mode	output voltage	current direction	S1	D1	S2	D2
1	Vs	To AC side	On	Off	Off	Off
2	Vs	From AC side	Off	On	Off	Off
3	-Vs	To AC side	Off	Off	Off	On
4	-Vs	From AC side	Off	Off	On	Off

It can be observed that the operation of switches S1/D1 and S2/D2 is complementary. This means if the upper half of the converter is conducting then the lower half must be blocking and vice versa. The current path associated with each operating mode is shown in Fig. 2-2

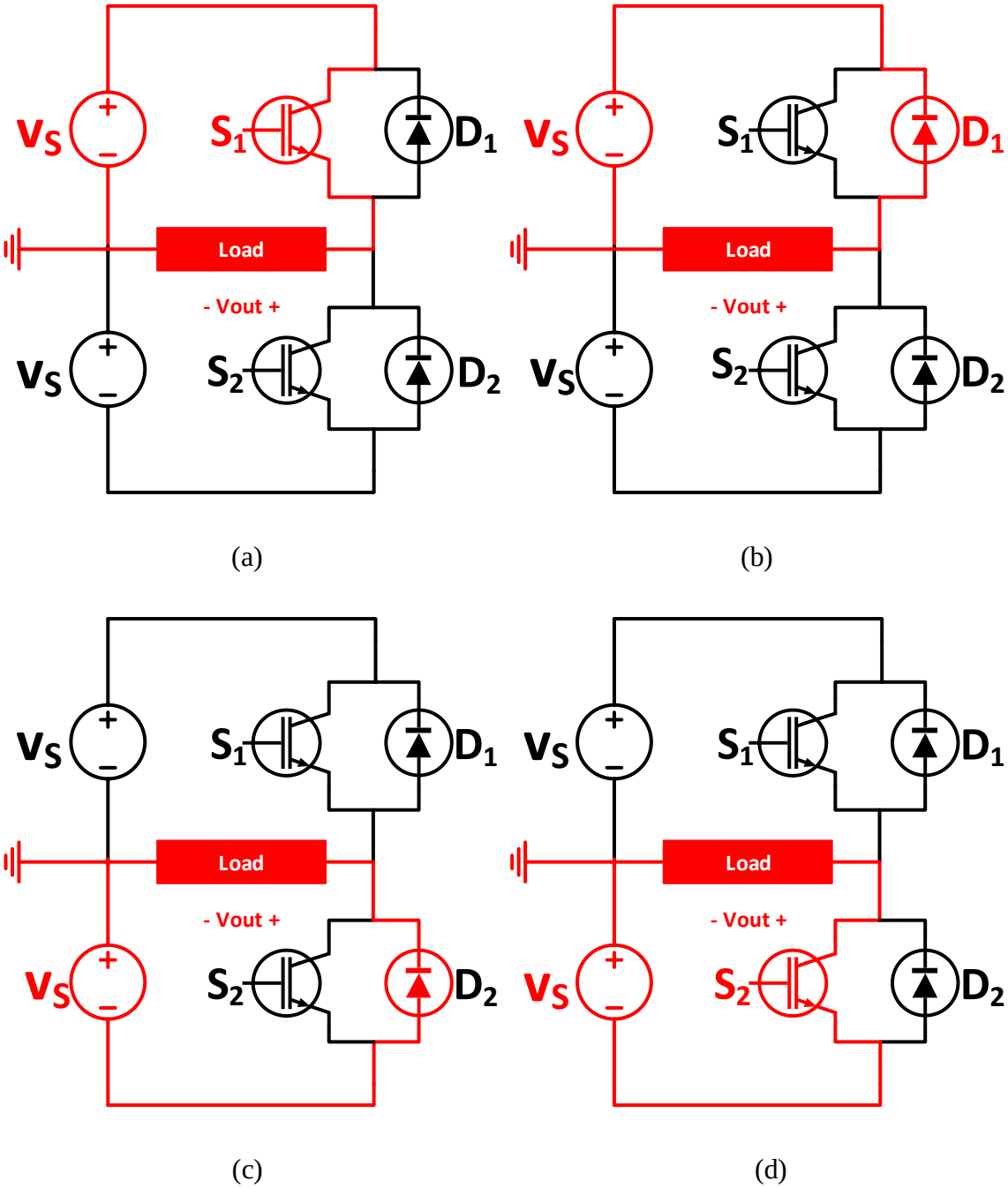


Figure 2-2 TLC operating modes a) Mode 1, b) Mode 2, c) Mode 3, d) Mode 4

The most common control method for the TLC is sinusoidal pulse width modulation (SPWM). The SPWM control operates using a modulation signal and a carrier signal. The modulation signal is

typically a sinusoid with desired output voltage frequency. On the other hand, the carrier signal will be a triangular wave of higher magnitude and much higher frequency then the modulation signal. During operation the modulation signal is constantly compared to carrier signal. If modulation signal is greater than carrier, controller will output a gate signal of '1', which represents turn on else a gate signal of '0', which represents turn off. The output is then fed to one of the switch and inverse of output is fed to its complement. An example of SPWM operation is shown in Fig. 2-3. In this example a 60 Hz sinusoidal modulation signal is modulated using a 2 kHz triangular carrier. In the case of the TLC one would connect the gate signal and its inverse to S1 and S2 respectively to ensure all operating mode comply with Table 2-1.

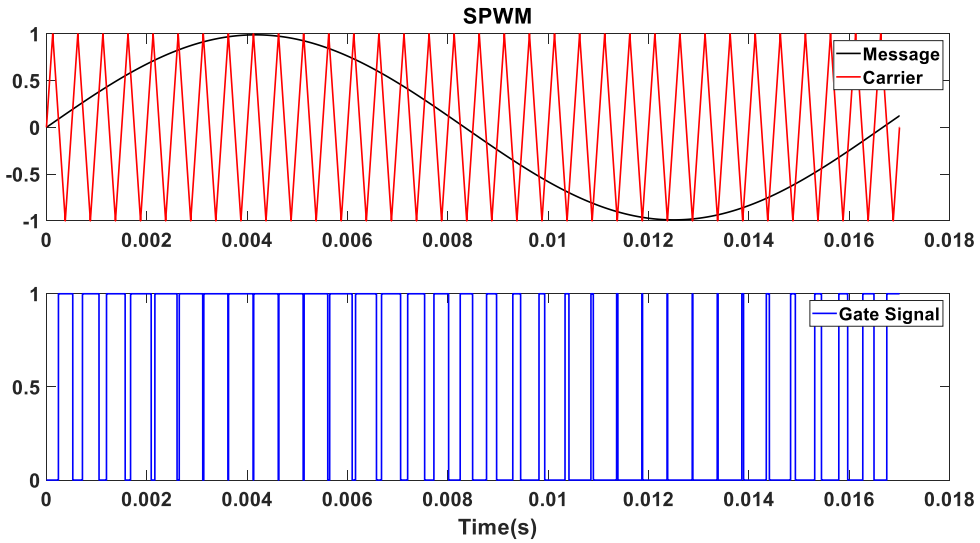


Figure 2-3 SPWM operation

The voltage output of the TLC and its frequency spectrum using the control signals above is shown in Fig. 2-4. Although the output is nowhere close to a sinusoidal waveform, but it can be seen from the frequency spectrum majority of the output contributes to a 60 Hz sinusoid.

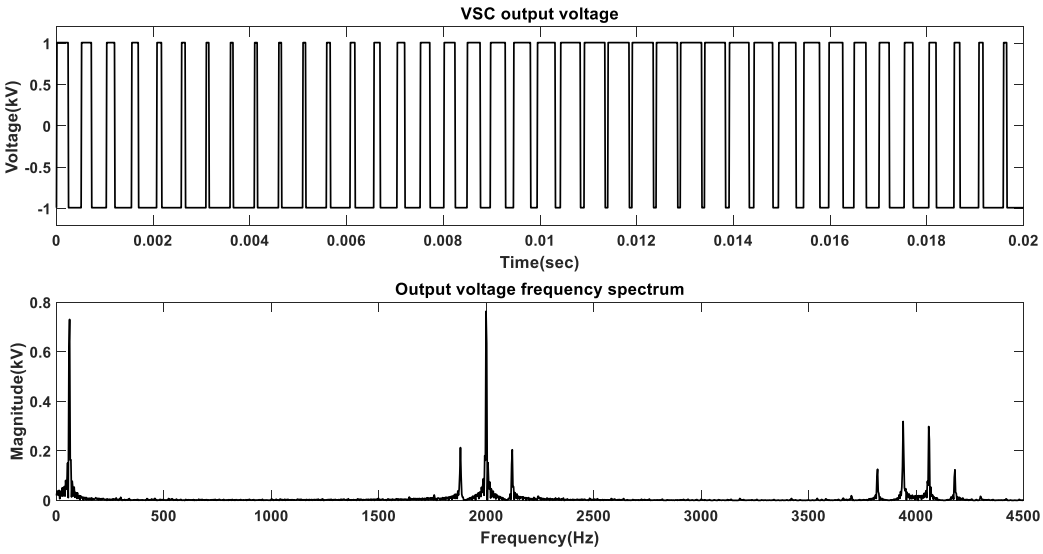


Figure 2-4 TLC output voltage and frequency spectrum

2.2 Multi-level Converter

The Multi-level VSC topology is an effective solution for high-rating converters. It is able to resolve the voltage blocking capability constraints of switches by sharing the voltage stress. This is realized by splitting the total dc link voltage down to intermediate dc levels, and selecting a specific combination of switches to conduct and block. As a result, the voltage stresses on each switch is reduced. This is unlike the TLC where each switch will always bear the full amount of dc voltage during its off-state. In addition to voltage stress improvement, another major advantage of having multilevel is that the level of ac side voltage harmonics is significantly reduced.

2.2.1 Diode Clamped Multi-level Converter

One of the earlier multilevel topologies is the DCMC. A commonly used topology is the three-level DCMC converter also called a neutral point clamped (NPC) converter. Clamping diodes are connected to mid points of series connected dc capacitors to provide the extra current path needed for producing different voltage levels. An example of typical 3 level NPC converter configuration is shown in Fig. 2-5. The switch state associated with each voltage level is tabulated below.

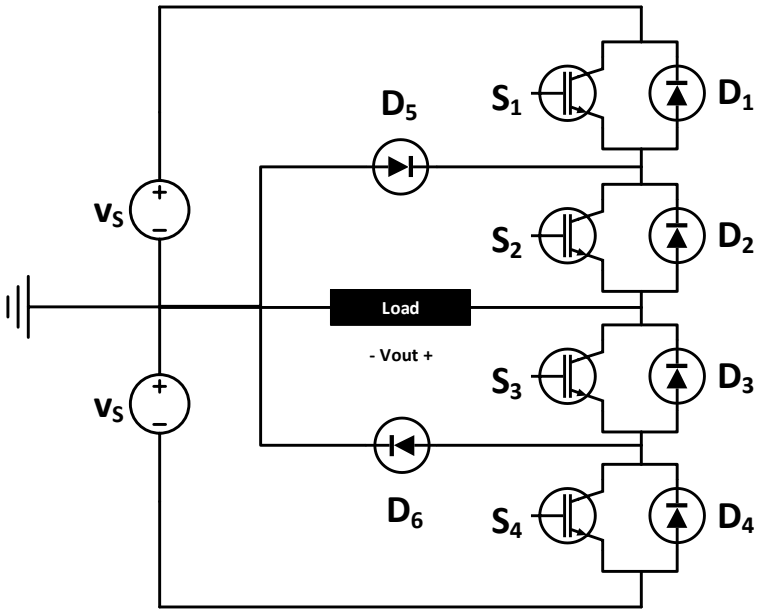


Figure 2-5 NPC configuration

Table 2-2 Neutral Point Clamped Converter Switch States Map

Converter operating mode	Converter output voltage	Converter current direction	S1	S2	S3	S4	D1	D2	D3	D4	D5	D6
1	Vs	To AC side	On	On	Off	Off	Off	Off	Off	Off	Off	Off
2		From AC side	Off	Off	Off	Off	On	On	Off	Off	Off	Off
3	0	To AC side	Off	On	Off	Off	Off	Off	Off	Off	On	Off
4		From AC side	Off	Off	On	Off	Off	Off	Off	Off	Off	On
5	-Vs	To AC side	Off	Off	Off	Off	Off	Off	On	On	Off	Off
6		From AC side	Off	Off	On	On	Off	Off	Off	Off	Off	Off

The current path associated with each operating mode is colored in red as shown in Fig. 2-6.

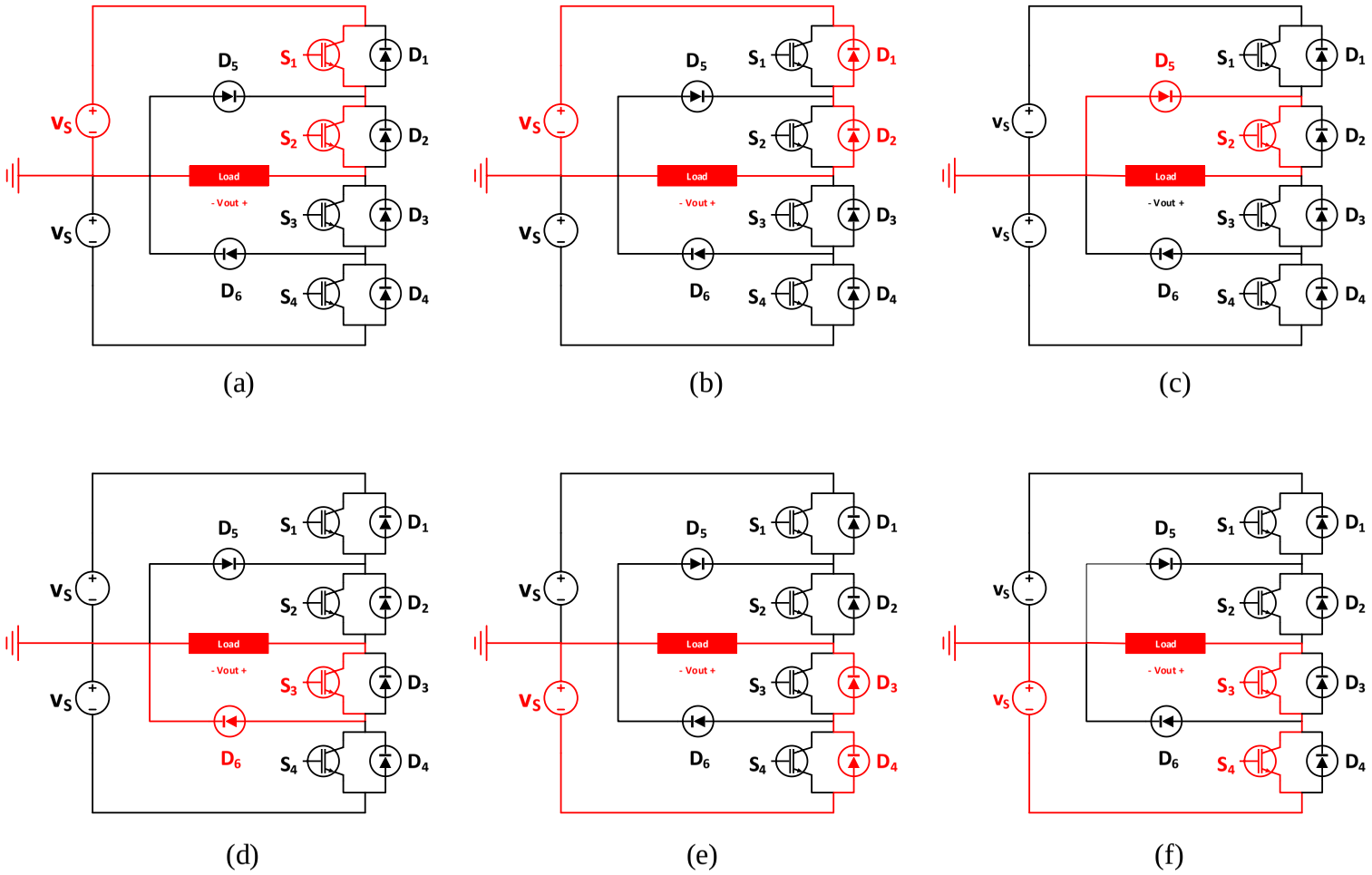


Figure 2-6 NPC operating modes a) mode 1, b) mode 2, c) mode 3, d) mode 4, e) mode 5, f) mode 6

One of the easier control method for NPC is using double carrier SPWM. This can be done by modulating the modulation signal with 2 triangular carriers of different magnitude. In Fig.2-7 a 60 Hz sinusoidal modulation signal is modulated by two 2 kHz triangular carrier. First carrier has a magnitude of positive half of message signal while second carrier has a magnitude of the negative half. S1 will receive a turn on signal if the top SPWM modulation produces a value of 1, else it will receive a turn off signal. Similarly Sw4 will receive a turn on signal if the bottom SPWM modulation produces a value of 0, else it will receive a turn off signal. Taking the complement of Sw1 and Sw4's gate signal will yield gate signal of S3 and S2 respectively.

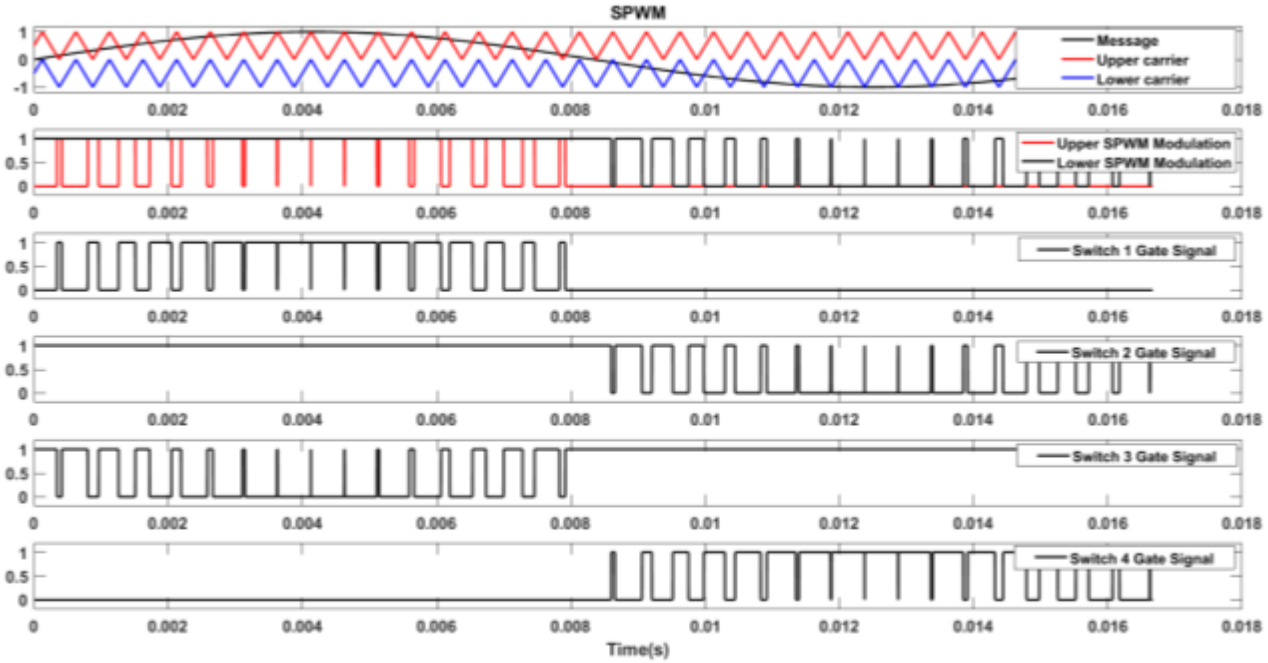


Figure 2-7 Dual carrier NPC control

The NPC's corresponding output voltage and its frequency spectrum using the above control signal is shown in Fig.2-8.

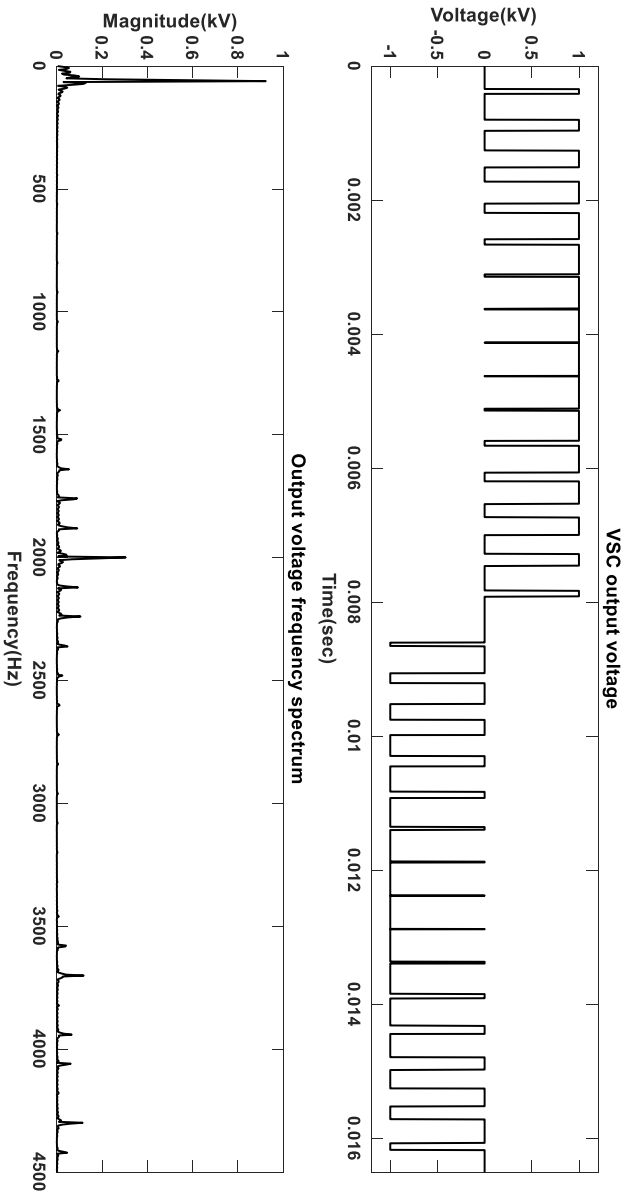


Figure 2-8 NPC output voltage and frequency spectrum

The DCMC can be configured for higher voltage levels operation however the complexity of converter structure and switch state increases significantly. Shown in Fig. 2-9 is an example of five level DCMC and the switching states associated with it is tabulated below.

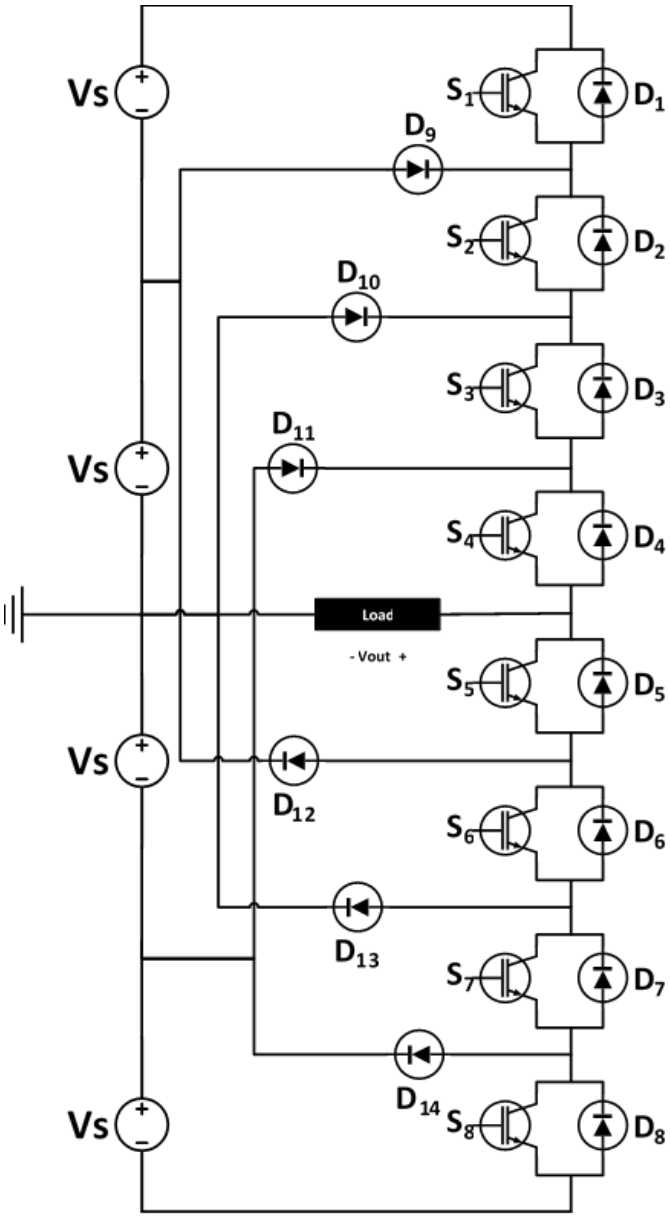


Figure 2-9 Five level DCMC converter configuration

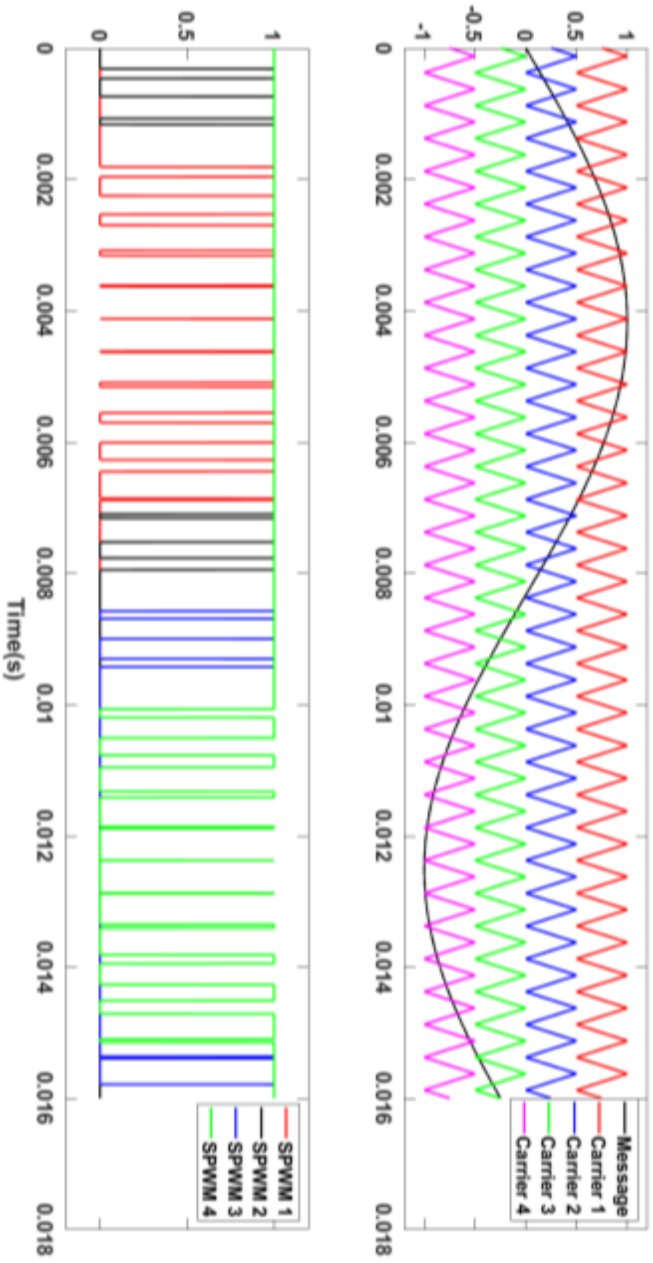
Table 2-3 Five Level Diode Clamped Converter Switch States Map

Converter output voltage	2Vs		Vs		0		-Vs		-2Vs	
Converter operating mode	1	2	3	4	5	6	7	8	9	10
Converter current direction	To AC side	From AC side	To AC side	From AC side	To AC side	From AC side	To AC side	From AC side	To AC side	From AC side
S1	On	Off	Off	Off	Off	Off	Off	Off	Off	Off
S2	On	Off	On	Off	Off	Off	Off	Off	Off	Off
S3	On	Off	On	Off	On	Off	Off	Off	Off	Off
S4	On	Off	On	Off	On	Off	On	Off	Off	Off
S5	Off	Off	Off	On	Off	On	Off	On	Off	On
S6	Off	Off	Off	Off	Off	On	Off	On	Off	On
S7	Off	Off	Off	Off	Off	Off	Off	On	Off	On
S8	Off	Off	Off	Off	Off	Off	Off	Off	Off	On
D1	Off	On	Off	Off	Off	Off	Off	Off	Off	Off

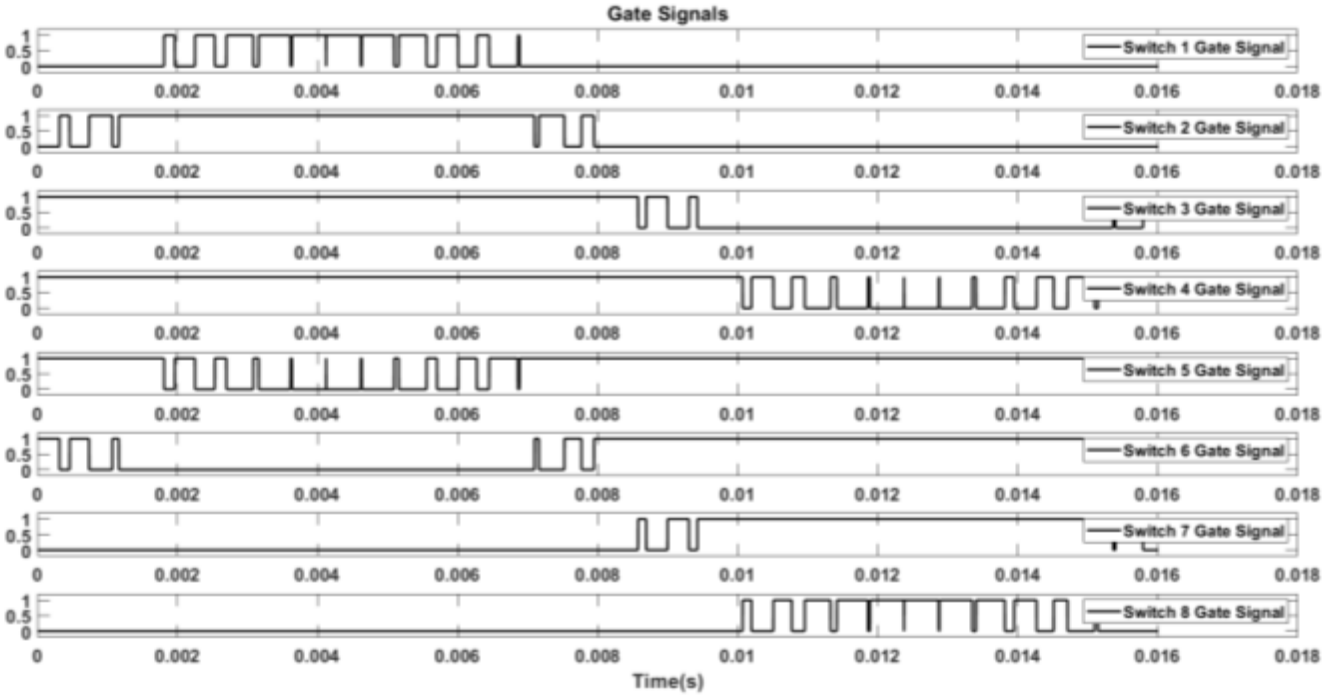
D2	Off	On	Off	Off	Off	Off	Off	Off	Off	Off
D3	Off	On	Off	Off	Off	Off	Off	Off	Off	Off
D4	Off	On	Off	Off	Off	Off	Off	Off	Off	Off
D5	Off	Off	Off	Off	Off	Off	Off	Off	On	Off
D6	Off	Off	Off	Off	Off	Off	Off	Off	On	Off
D7	Off	Off	Off	Off	Off	Off	Off	Off	On	Off
D8	Off	Off	Off	Off	Off	Off	Off	Off	On	Off
D9	Off	Off	On	Off	Off	Off	Off	Off	Off	Off
D10	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
D11	Off	Off	Off	Off	On	Off	On	Off	Off	Off
D12	Off	Off	Off	On	Off	Off	Off	Off	Off	Off
D13	Off	Off	Off	Off	Off	On	Off	Off	Off	Off
D14	Off	Off	Off	Off	Off	Off	Off	On	Off	Off

The complex structure off converter will also make the controller more complicated. Similar to the NPC the 5 levels DCMC converter can be controlled using a quadruple carrier modulation

method as shown in Fig.2-10. In this case a 60Hz modulation signal is modulated by four 2000 Hz triangular carrier. For this configuration gate signal for Sw1, Sw2, Sw3, Sw4 directly corresponds to the SPWM1, SPWM2, SPWM3, and SPWM4 output respectively. On the other hand gate signal for Sw5, Sw6, Sw7, and Sw8 is obtained by taking the complement of Sw1, Sw2, Sw3, and Sw4 respectively.


SPWM
Message
Carrier 1
Carrier 2
Carrier 3
Carrier 4
SPWM 1
SPWM 2
SPWM 3
SPWM 4
Time(s)

(a)



(b)

Figure 2-10 Five level DCMC controller a) Modulation waveforms b) Gating signals

The output voltage and its frequency spectrum of the 5 Level DCMC using the above control signal is shown below.

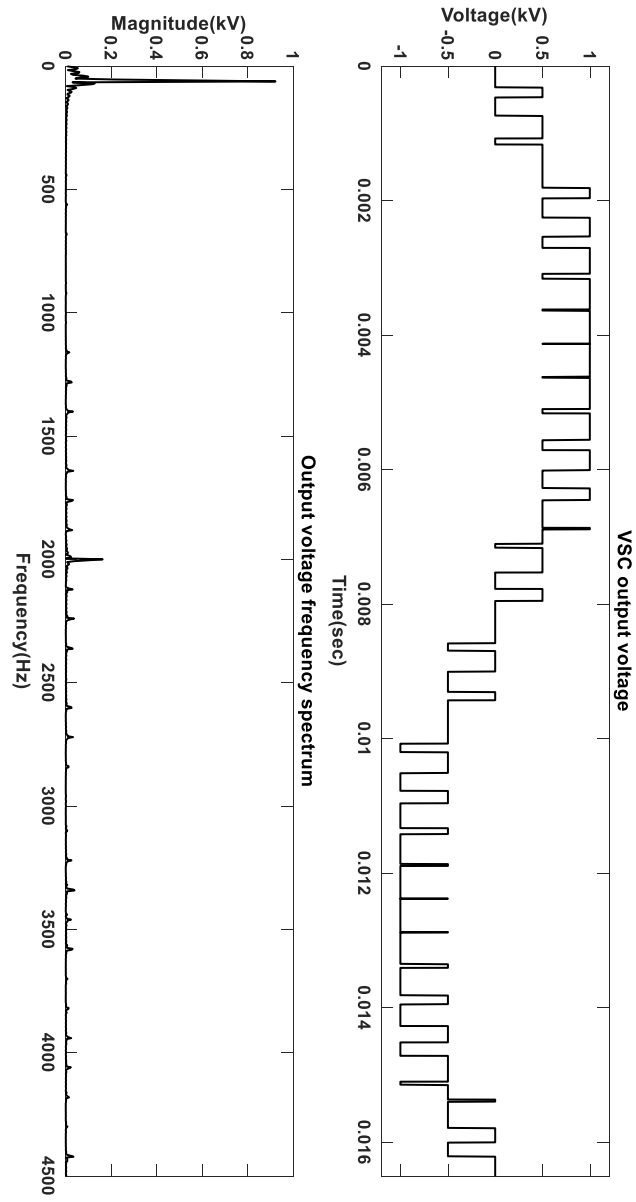


Figure 2-11 Five level DCMC converter output voltage waveform and frequency spectrum

In additional to the increased complexity of converter and controls, it is also worth mentioning that in real operation the dc side voltage sources will be replaced as DC link capacitors, and frequency of charge and discharge of capacitor is unbalanced due to the structure of converter. The closer capacitors are to the midpoint of converter the more frequently they will be active. This yields an unbalanced situation and will disrupt be balance in the dc link voltage.

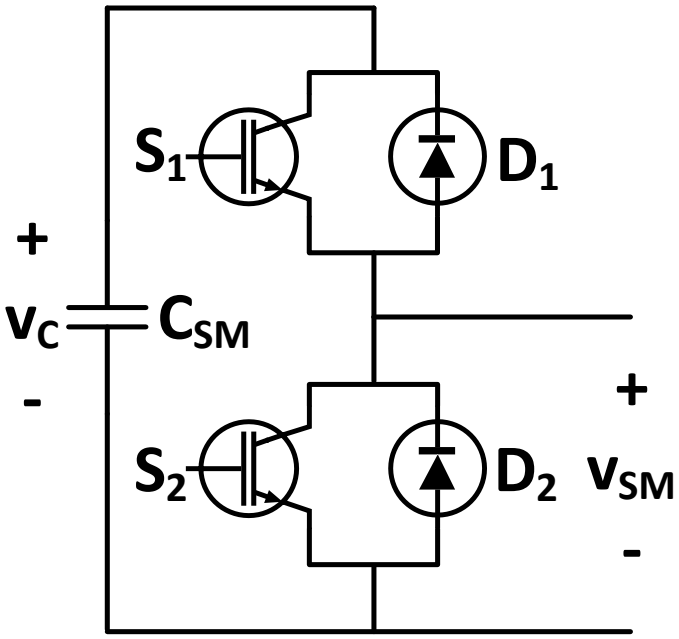
2.2.2 Modular Multi-level Converter

DCMC is capable of operating for higher voltage levels. However the number of voltage levels cannot be easily incremented due to structure, control complexity and DC link voltage balance. Thus a more convenient approach is desired such that the converter is more scalable and has a modular property. The Modular Multi-level Converter (MMC) is well known as the state of the art multilevel converter and is a much more suitable topology then DCMC for high voltage applications.

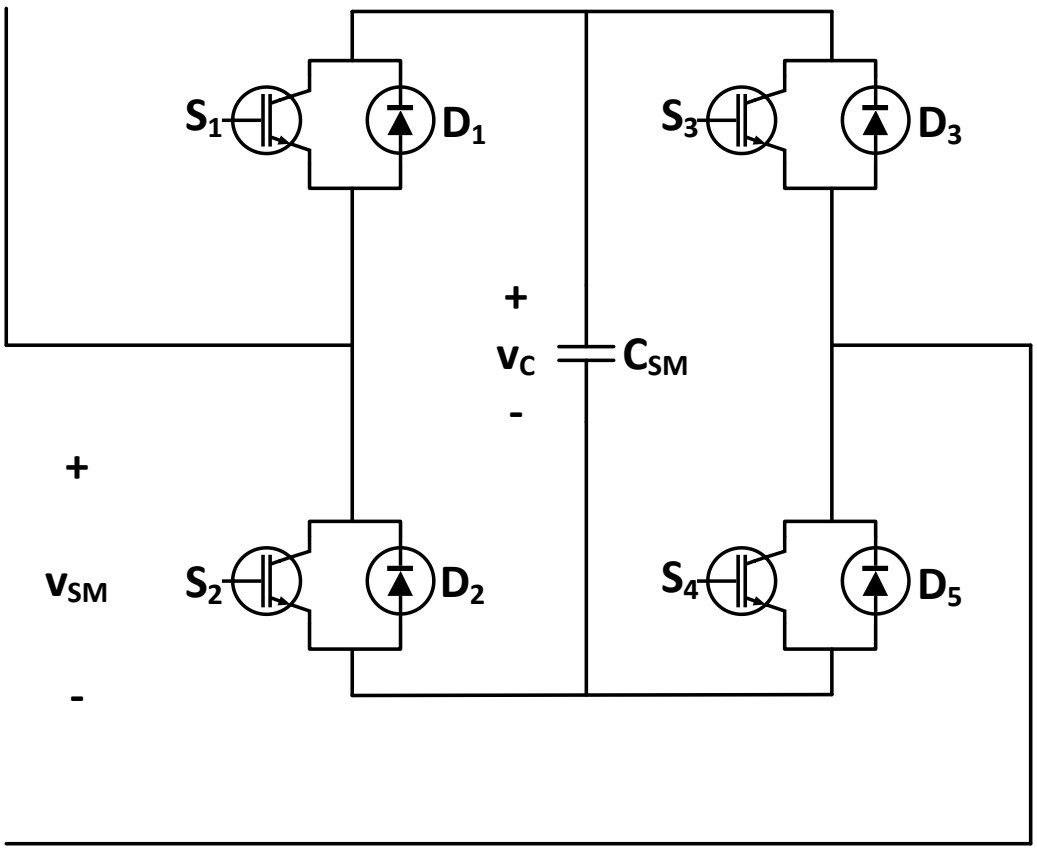
The MMC uses cascaded converter submodules (SM) in series to produce multiple voltage levels. As a result of the series connection, voltage stress on each SM is divided out. In addition to voltage stress distribution, higher amount of voltage levels also mean better quality AC waveform in terms of harmonics. Thus the AC side voltage is inherently closer to sinusoidal and with a sufficiently large number of levels, there is no need for any ac filters [32]. One main advantage of MMC over DCMC is that the voltage stress is shared more evenly across each capacitors, this is because the capacitors are located within each submodule. Also the same submodule can be used with different converter voltage ratings. For example, if you have 25 modules in each arm, each with a capacitor voltage of 1

kV, then the dc voltage is 25 kV. With 100 modules of the same type, the rating becomes 100 kV. Thus, the simpler structure also allows for easier increase of voltage level by adding additional SMs in series with the existing.

Two widely used SM topologies are the half-bridge and full-bridge topologies. Both SM's configuration is shown in Figure 2-12 a) and b) respectively.



(a)



(b)

Figure 2-12 MMC SM configurations a) Half-bridge, b) Full-bridge

One main difference between half-bridge SM and full-bridge SM is control flexibility. Full bridge SM provides additional current path which allows bipolar voltage level in each module. The Half and full bridge SM switch states are tabulated in Table 2-4. When current is conducting through the SM capacitor the SM is inserted else SM is blocked.

Table 2-4 Modular Multi-level Converter Sub-Module Switch States Map

SM voltage level	Vc		0		-Vc	
SM operating mode	1	2	3	4	5	6
SM current direction	Into midpoint of S1&S2	From midpoint of S1&S2	Into midpoint of S1&S2	From midpoint of S1&S2	Into midpoint of S1&S2	From midpoint of S1&S2
Half bridge SM						
Sw1	Off	On	Off	Off	n/a	n/a
Sw2	Off	Off	On	Off	n/a	n/a
D1	On	Off	Off	Off	n/a	n/a
D2	Off	Off	Off	On	n/a	n/a
Full bridge SM						
Sw1	Off	Off	Off	On	Off	On
Sw2	On	Off	Off	Off	Off	Off
Sw3	On	Off	On	Off	Off	Off
Sw4	Off	Off	Off	Off	Off	On
D1	Off	Off	On	Off	On	Off

D2	Off	On	Off	Off	Off	Off
D3	Off	On	Off	On	Off	Off
D4	Off	Off	Off	Off	On	Off

When N number of SMs are connected in series an arm is created and two arms in series makes a phase leg. In addition to sub modules there will also be arm inductors in each arm to limit the arm current's rate of change. An example of 1 phase MMC configuration is shown figure 2-13.

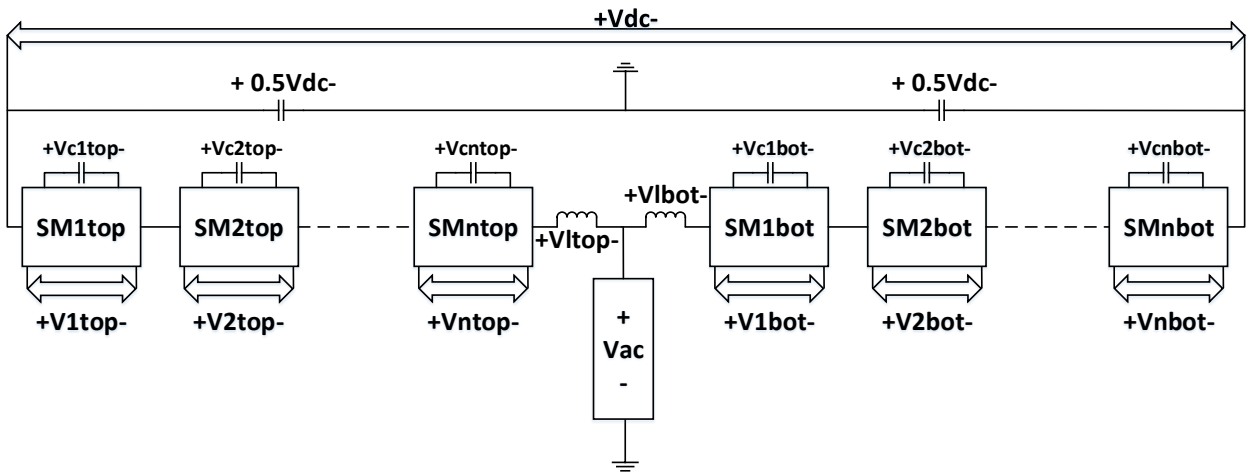


Figure 2-13 MMC configuration for one phase

The voltage output characteristic of MMC is derived by performing KVL on the upper and lower arm of the 1 phase MMC shown in figure 2-13. Performing KVL on the lower arm will yield equation (2.1) and upper arm will yield equation (2.2).

$$-0.5V_{dc} + \sum_{n=1}^{N} V_{nbot} + V_{lbot} + V_{ac} = 0 \qquad (2.1)$$

$$0.5V_{dc} - \sum_{n=1}^{N} V_{ntop} - V_{ltop} + V_{ac} = 0 \qquad (2.2)$$

Adding (2.2) with (2.1) yields (2.3)

$$V_{ac} = 0.5\left[\left(\sum_{n=1}^{N} V_{nbot} - \sum_{n=1}^{N} V_{ntop}\right) - V_{lbot} + V_{ltop}\right] \qquad (2.3)$$

If one considers the fact that the arm inductor's voltage is normally negligible compare to the total DC voltage of submodules under normal operating condition then equation (2.3) can be further simplified into equation (2.4) which indicates the output voltage as a function of inserted SM.

$$V_{AC} = 0.5\left(\sum_{n=1}^{N} V_{nbot} - \sum_{n=1}^{N} V_{ntop}\right) \tag{2.4}$$

When a SM is inserted current will flow through its capacitor. As result the capacitor voltage will either increase or decrease depending on the direction of current. In order to regulate the capacitor voltage a logical choice must be made when deciding on which SM to insert such that SM capacitors' voltage level are balanced. Using (2.4) the average voltage level of each submodule can also be derived as (2.5)

$$V_C = \frac{Vac_{pk-pk}}{N} \tag{2.5}$$

Various control method has been proposed for the MMC. For the sake of simplicity nearest level modulation (NLM) is used in this thesis to control the output voltage waveforms [25][33] and to ensure capacitor voltage balancing between all sub-modules. NLM control determines the number of SMs to be inserted to ensure the desired instantons voltage magnitude. This is done by comparing the modulating voltage signal to its corresponding voltage levels. After determining the instantaneous voltage level which is equivalent to the output ac voltage, the number of SM to be inserted can be found using (2.4). The NLM control then selects specific SM to insert by examining all SM's capacitor voltage information. An optimal selection is made such that the average voltage of each submodule can be maintained. A typical flow chart of NLM and capacitor balance control for MMC is shown in Fig 2-14.

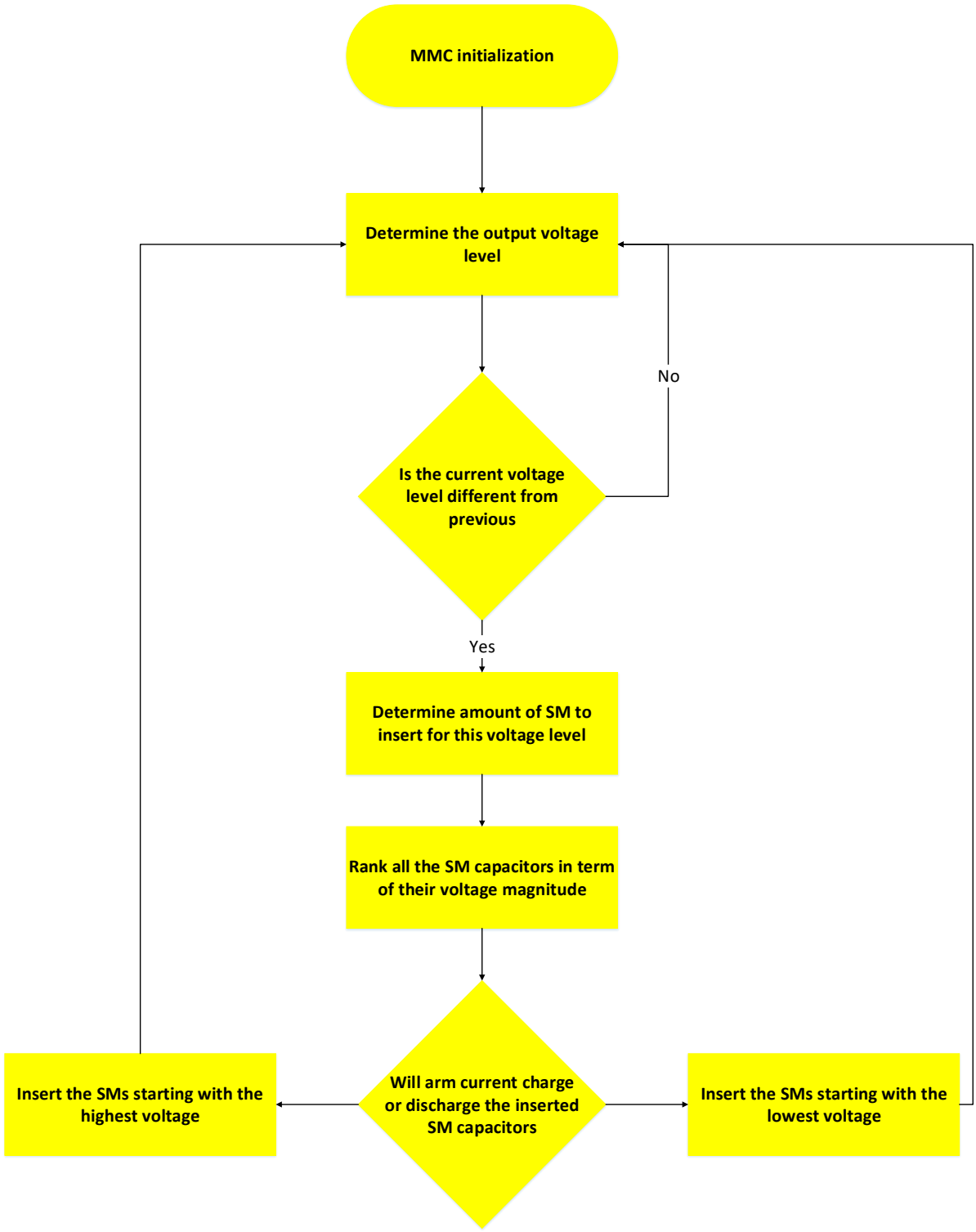


Figure 2-14 MMC NLM and capacitor balance flow chart

The voltage output and its frequency spectrum of a basic 11 levels MMC using NLM control I shown in Fig. 2-15.

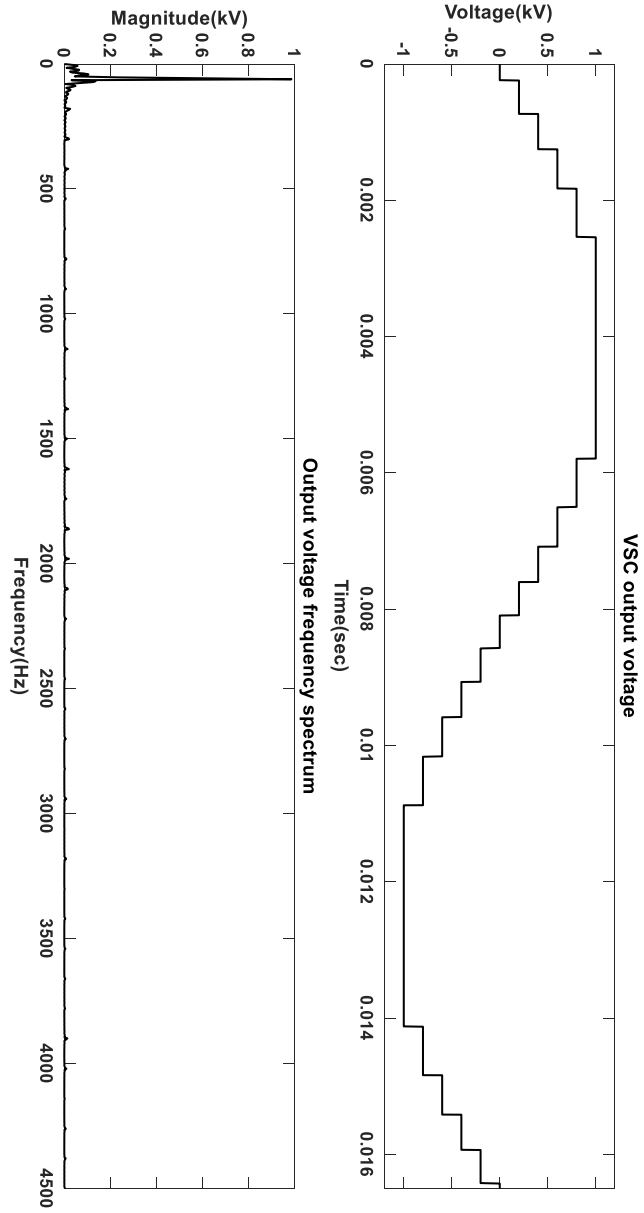


Figure 2-15 Eleven levels MMC voltage output and frequency spectrum

2.3 Decoupled control

The VSC controls introduced in this chapter operate using methods such as pulse width modulation (PWM) for the TLC and NLM for the MMC. In these schemes, a switching decision is made based on the instantaneous value of the modulation and carrier signal.

A common method for generating the modulation signal is decoupled control [34]. This is due to the frequent presence of three phase network in today's power system. In decoupled control the Direct Quadrature Zero (dq0) transformation is used to convert the three phase (abc) time varying quantities into two phase (dq) quantities. When real power P and reactive power Q of VSC is calculated using d, q quantities it can be found that the power can be described by (2.6).

$$P = v_d i_d \qquad (2.6a)$$

$$Q = v_q i_q \qquad (2.6b)$$

The real and reactive power can be controlled by adjusting the d axis current i_d and q axis current i_q of converter. In the decoupled control, i_d and i_q reference signal is generated from the P and Q error. This reference is compared to the measured i_d and i_q terms and the resulting error is used to generate the d axis voltage v_d and q axis voltage v_q references. These are further inverse

transformed to the phase reference voltages $v_{aref}, v_{bref}, v_{cref}$ for the converter. The feedforward cross coupling gains ωL provide decoupling between the d and q control loops, i.e., an ordered change in i_{dref} is achieved with minimal transient in i_{qref} and vice-versa. A typical decoupled controller for VSC is shown in Fig. 2-16

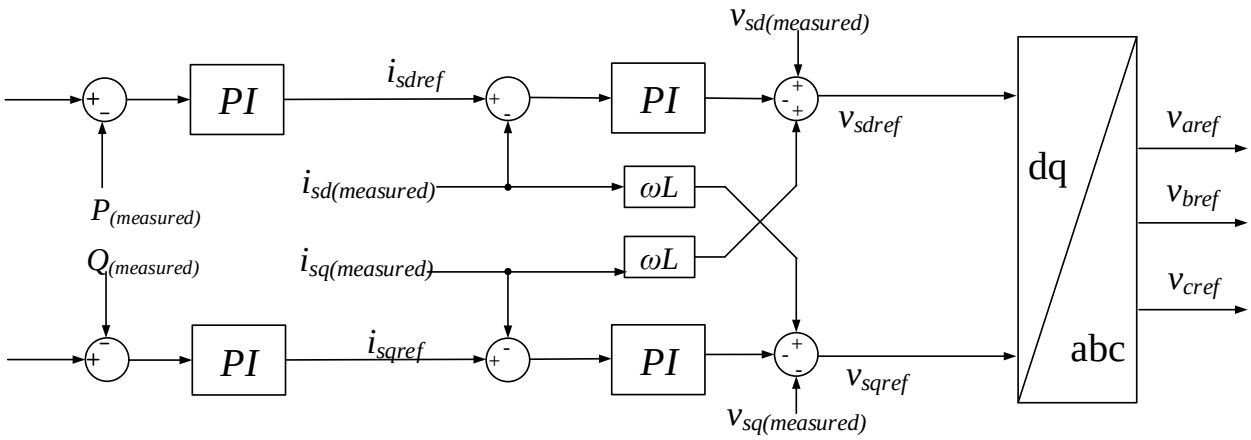


Figure 2-16 Decoupled control block diagram

3 Advantages and Disadvantages of LC Switch Model

Advantage:

Recall in chapter 1, the LC Switch Model (LCSM) represents switch as a small capacitor 'C_{off}' in the off-state, and as a small inductor 'L_{on}' in the on-state. By enforcing equation (3.1), the LCSM will result in the same admittance regardless of which state it is in. This eliminates the admittance matrix re-factorization process during switching, thus significantly enhancing the simulation speed.

$$G_{sw} = G_{on} = G_{off} \tag{3.1}$$

Disadvantage:

Unlike the Resistor Switch Model (RSM), the previous implementations of LCSM manifested a spurious loss and oscillation resulting from a switching [35][36][37].

This chapter identifies the cause of LCSM's spurious loss and oscillations. A mathematical representation of the undesired characteristic is formulated and analyzed. Furthermore, solutions to suppress LCSM's loss and oscillation is developed.

3.1 Analysis of spurious switching loss

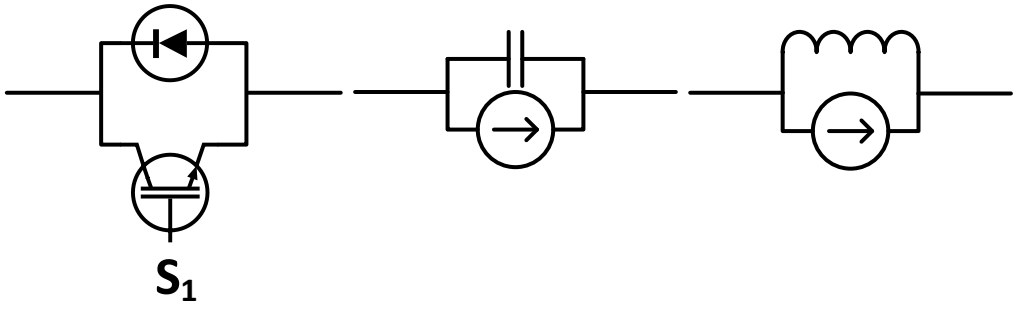


Figure 1-3 LCSM switch model a) General bi-directional switch; b) Off-state representation c) On-state representation

For ease of reference Fig 1-3 is redrawn above. Given a typical LCSM as shown. Let C be the capacitance used to represent the off-state switch and L be the inductance used to represent the on-state switch. In Dommel's companion matrix form [12], the switch's history current term is given by (3.2) assuming trapezoidal rule of integration. In (3.2), G_L and G_C are the conductance of the companion circuit for the inductor and capacitance respectively. $i_L[n]$, $v_L[n]$ are the inductor current and voltage to be computed for the present time step, and $i_L[n-1]$, $v_L[n-1]$ are the value from the previous time step. Similar parameters are also used for capacitor equations.

$$G_L = \frac{\Delta t}{2L} \tag{3.2a}$$

$$i_L[n] = G_L v_L[n] + G_L v_L[n-1] + i_L[n-1] \tag{3.2b}$$

$$G_C = \frac{2C}{\Delta t} \tag{3.2c}$$

$$I_C[n] = G_C V_C[n] - I_C[n-1] - G_C V_C[n-1] \tag{3.2d}$$

Assume a switch is initially in the off-state and a turn on signal is received. The switch then changes from capacitor representation to an inductor representation. As indicated by (3.2b), inductor mode of operation requires the inductor's history current and history voltage information. However, before switching occurred the switch was operating as a capacitor so this required history information is missing. A similar problem is encountered for a turn off operation. As a result, during the first time step after every switching event, the history voltage and current term of the LCSM is reset to zero due to lack of information. The act of resetting history term causes spurious switching loss in the LCSM. This is because during steady state operation, the switch is either represented as a fully energized capacitor or inductor. Reset of history term is equivalent of dumping the stored energy which is essentially an energy loss.

A test circuit of dc source connected to a resistor load through a switch is constructed as shown in Fig 3-1. Simulation is performed using both RSM and LCSM to demonstrate LCSM's spurious switching loss. The simulation parameters are tabulated in Table 3-1

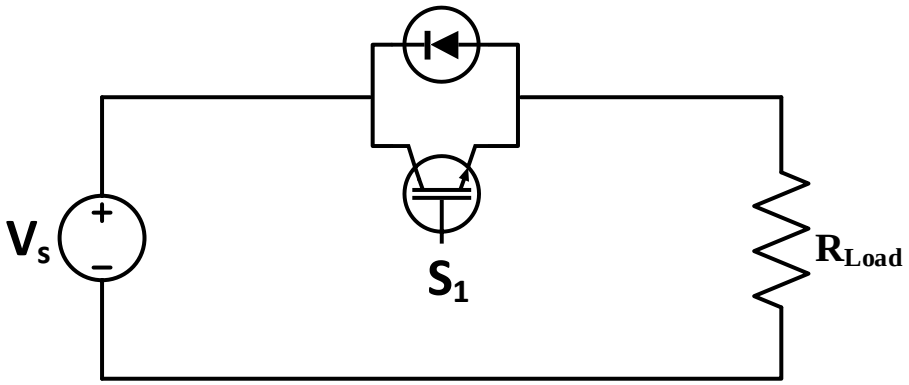
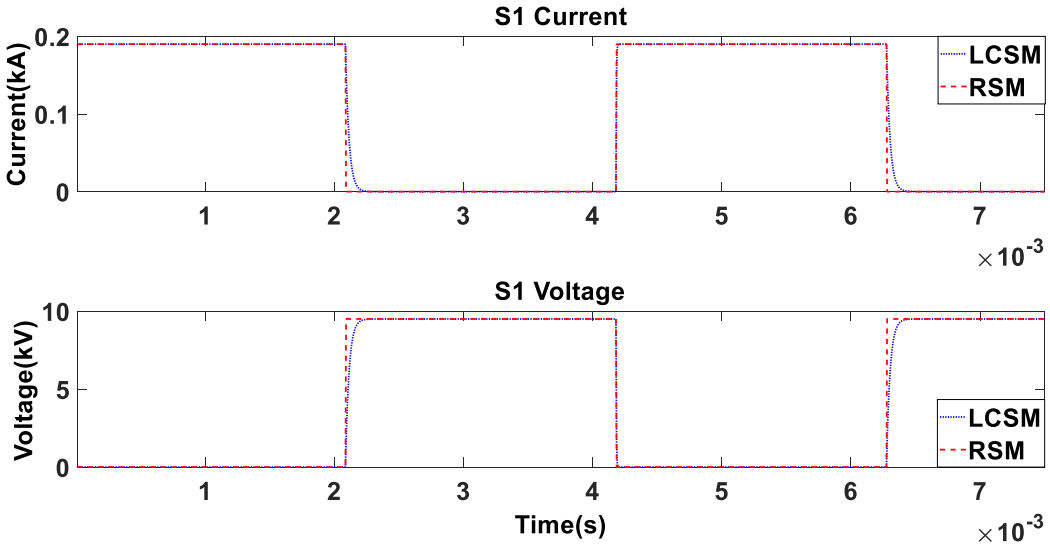


Figure 3-1 Single switch test circuit

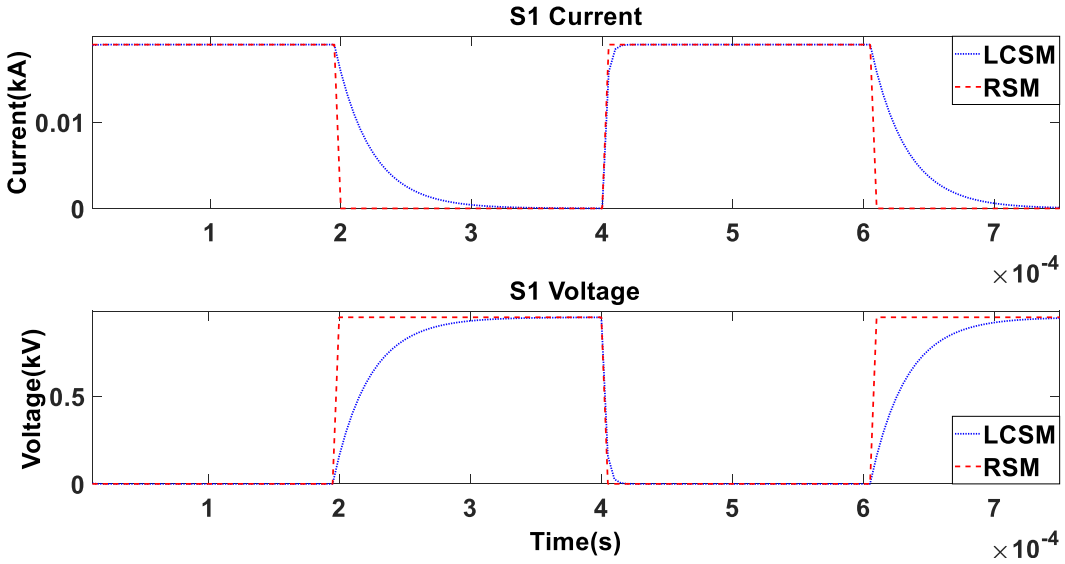
Table 3-1 Test Circuit Operation Parameters

Source Voltage (kV)	9.5
Load Resistance (Ω)	50
Simulation time step (μsec)	5
Switching Frequency 1 (Hz)	250
Switching Frequency 2 (Hz)	2500

The test circuit is being switched at both 250 Hz and 2500 Hz. Switch voltage and current is plotted in Fig 3-2. It can be observed that a transient charging period is shown by the LCSM when compared to RSM. This charging period is fixed and is not affected by the switching frequency. As a result, it will become more and more significant as switching frequency increase.



(a)



(b)

Figure 3-2 Simulation waveforms a) Switch current/voltage plot at 250 Hz; b) switch current/voltage plot at 2500 Hz

The switching loss can be calculated as a product of voltage and current during the charging period as shown in (3.3). Where T is the switching periods, v_{sw} and i_{sw} are the switching voltage and current respectively.

$$P_{loss} = \frac{1}{T}\int_0^T v_{sw}(t) \times i_{sw}(t)dt \qquad (3.3)$$

For the resistive load test circuit, the spurious loss can be calculated analytically. The turn on loss of LCSM can be described as equation (3.4), and turn off as equation (3.5). T_{on}, and T_{off} are the switch on and off periods respectively.

$$P_{on} = \frac{v_S^2 L}{TR^2}\left(0.5 - e^{-\frac{RT}{L}} + e^{\frac{2RT}{L}}\right) \qquad (3.4)$$

$$P_{off} = \frac{v_S^2 C}{T}\left(0.5 + 0.5e^{-\frac{2T}{RC}} - e^{-\frac{T}{RC}}\right) \qquad (3.5)$$

3.2 Analysis of spurious switching Oscillations

Beside spurious switching loss, another problem the LCSM will encounter is spurious switching oscillations. If there exists one set of complementary switch in the switching topology, then oscillation will occur after switching.

Complementary switches are the fundamental component of VSC. When one switch is turned off in a complementary switch set, its current will commutate to its compliment. For example consider the phase leg of a 2 level VSC shown in Fig 3-3(a), and assume that the load current is continuous. Two operating modes can be identified as shown in Fig 3-3(b) and (c). During mode 1, load current i_S flows through the switch S1. When converter enters mode 2, S1 is turned off and S2 is turned on and the load current will immediately commutate to the complementary switch S2. In this case the S1 and S2 form a set of complementary switches.

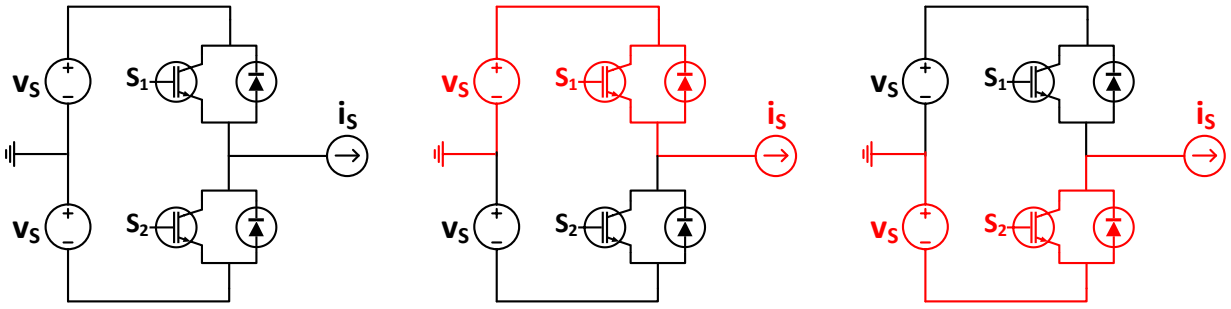
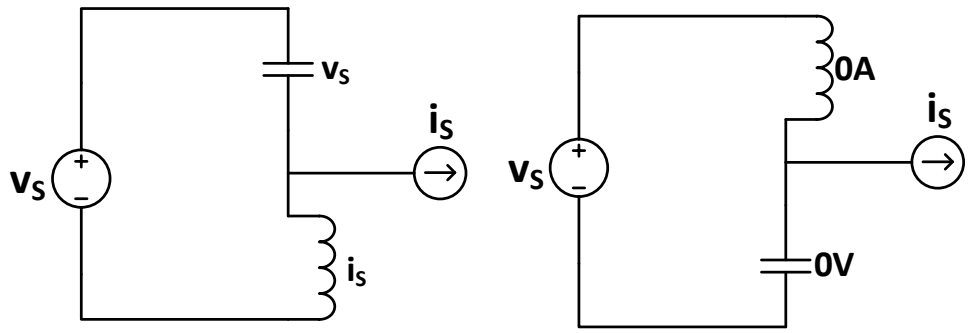


Figure 3-3 Complementary switch set of two-level converter a) topology configuration b) Mode 1 current path c) Mode 2 current path

The equivalent circuit of Fig.3-3 (b) and (c) using LCSM representation is shown in Fig. 3-4. Also, consider a large inductor is present in series with the load, so that the load current can be considered to be essentially constant and equal to i_S. The state space equation and eigenvalues can then be found.



(a) (b)

Figure 3-4 LCSM complementary switch a) pre-switching; b) post-switching

The state space equation for the LCSM switch set in Fig. 3-4 (a) is (3.6) and its eigenvalue is (3.7). The same eigenvalue is obtained for the circuit in Fig. 3-5 (b).

$$\begin{bmatrix} v_C{}' \\ i_L{}' \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} v_C \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} v_S \\ i_S \end{bmatrix} \tag{3.6}$$

$$\lambda = \pm \frac{j}{\sqrt{LC}} \tag{3.7}$$

The eigenvalues are on the imaginary axis which indicates an oscillatory response at angular frequency $\frac{1}{\sqrt{LC}}$. The post switching inductor current and capacitor voltages are as in (3.8). In this case $t = 0$ is the switching instance.

$$v_C(t) = [v_S - v_C(0)]\cos\left(\frac{t}{\sqrt{LC}}\right) + [i_S - i_L(0)]\sqrt{\frac{L}{C}}\sin\left(\frac{t}{\sqrt{LC}}\right) - v_s \qquad (3.8a)$$

$$i_L(t) = i_s + [v_S - v_C(0)]\sqrt{\frac{C}{L}}\sin\left(\frac{t}{\sqrt{LC}}\right) - [i_S - i_L(0)]\cos\left(\frac{t}{\sqrt{LC}}\right) \qquad (3.8b)$$

Due to lack of history information $v_C(0)$ and $i_L(0)$ is equated to zero when switching occur. However, being state variables, the instantaneous value of v_S and i_S do not change at the switching instant. This is equivalent of energizing an uninitialized LC circuit through an ac current and dc voltage source. As a result, oscillation occurs in the LC circuit and the magnitude of oscillation is directly proportional to the voltage, current source magnitude and switch admittance.

Equation (3.8) confirms a pair of complementary switches will produce oscillation during switching because it is a marginally stable system with eigenvalues located on the imaginary axis. In discrete domain the stability is preserved if trapezoidal integration method is used [38]. This means the same oscillation will be expected when performing EMT type simulation. In order to use the LCSM, damping must first be introduced to ensure complementary switches can eventually enter a steady state. In the discrete domain, damping can be easily added by applying Backward

Euler Integration (BEI) method [24]. If BEI method is used then the time domain state space equation in (3.6) is transformed to (3.10). Where Δt is the set simulation time-step. The constant admittance enforcement of (3.1) also becomes (3.11). Here, $[n]$ represents the current time-step and $[n-1]$ the previous time-step.

$$\begin{bmatrix} v_C[n] \\ v_L[n] \end{bmatrix} = \begin{bmatrix} \dfrac{1}{1+\dfrac{\Delta t^2}{LC}} & \dfrac{\Delta t}{C+\dfrac{\Delta t^2}{L}} \\ -\dfrac{\Delta t}{L+\dfrac{\Delta t^2}{C}} & \dfrac{1}{1+\dfrac{\Delta t^2}{LC}} \end{bmatrix} \begin{bmatrix} v_C[n-1] \\ i_L[n-1] \end{bmatrix} + \begin{bmatrix} \dfrac{\Delta t^2}{LC+\Delta t^2} & -\dfrac{\Delta t}{C+\dfrac{\Delta t^2}{L}} \\ \dfrac{\Delta t}{L+\dfrac{\Delta t^2}{C}} & \dfrac{\Delta t^2}{LC+\Delta t^2} \end{bmatrix} \begin{bmatrix} v_S[n] \\ i_S[n] \end{bmatrix} \quad (2.10)$$

$$\frac{\Delta t}{L} = \frac{C}{\Delta t} \qquad (3.11)$$

With the new discrete time state space equation, one can find the discrete eigenvalue of the complementary switch by solving $|\lambda I - A| = 0$. Equation (3.12) describes the new set of discrete eigenvalue λ' which is located within the unit circle in discrete domain, hence a damped sinusoidal response is expected [39].

$$\lambda'_{1,2} = 0.5 \mp j0.5 \qquad (3.12)$$

The discrete time state variable response can then be obtained using the discrete eigenvalues. The final closed form expression for v_C and i_L can be found as equation (3.13), where Δt is the set simulation time step, G_{SW} is the set switching admittance. $\Delta i = i_{0+} - i_s$ which represents the difference between pre and post switching switch current. On the other hand, $\Delta v = v_{0+} - v_s$ represents the difference between pre and post switching switch voltage, $\theta_1 = \tan^{-1}\left(\frac{G_{sw}\Delta v}{\Delta i}\right)$, $\theta_2 = \tan^{-1}\left(\frac{\Delta i}{G_{sw}\Delta v}\right)$. As expected from the position of the discrete eigenvalues, damping is observed in the post switching switch voltage and currents.

$$i_{s1}[n\Delta t] = 2 \times 0.707^n \sqrt{0.25(\Delta i^2 + G_{sw}^2 \Delta v^2)} \times \cos(45°n + \theta_1) + i_s \qquad (3.13a)$$

$$v_{s2}[n\Delta t] = 2 \times 0.707^n \sqrt{0.25\left(\frac{\Delta i^2}{G_{sw}^2} + \Delta v^2\right)} \times \cos(45°n + \theta_2) + v_s \qquad (3.13b)$$

One interesting phenomenon observed from (3.13) is that regardless of any simulation parameters, the attenuation introduced by BEI per time-step in LCSM is 0.707, therefore it requires 14 simulation time steps before a switching oscillation attenuates below 1% of initial peak.

4 Spurious loss and oscillation suppression

Recall the traditional LC Switch Model (LCSM) is known for its simulation speed due to elimination of system matrix re-factorization process during every switching time step. However the model has an inherent underdamped oscillatory response due to its LC resonance structure. Past solutions to the LCSM's spurious switching losses and oscillatory response is through the addition of damping via the Backward Euler integration (BEI) method [24]. In this research two new improved methods are proposed to suppress the spurious loss and oscillation in LCSM. The first method further reduces spurious loss and oscillation by selecting an optimal current injection value after the switching time step such that energy balance is achieved. The second method reduces loss and eliminate oscillation by introducing a novel constant admittance based topology, selecting an appropriate integration method, and use of predictive subroutine during switching.

4.1 Energy Balance Method

Chapter 3 summarizes switching loss as a result of the LCSM's energy recharge process at the start of every switching event. Therefore, if this recharge process is eliminated then so will the switching loss.

This thesis proposes Energy Balance Method to eliminate the recharging process which must occur when the LCSM changes state from L to C or visa-versa. The recharging of the LCSM

can be eliminated by enforcing the total energy of the complementary switches to be the same pre and post switching. This is done by enforcing (4.1) at the switching instance. On the left hand side of (4.1) is the pre switching total switch energy, and the total post switching switch energy is located on the right hand side. Since the net energy is zero during a switching event the switching energy loss is reduced to zero.

$$C \cdot {v_{0-}}^2 + L \cdot {i_{0-}}^2 = C \cdot {v_{0+}}^2 + L \cdot {i_{0+}}^2 \qquad (4.1)$$

It is true enforcing equation (4.1) will eliminate the spurious energy loss, but because i_{0+} and v_{0+} are both unknowns, there will always be infinite number of values of v_{0+} and i_{0+} to satisfy this equation. In this research two methods are proposed for selection of the post switching switch voltage and current terms. First method is direct energy balance enforcement and second method is optimized energy balance enforcement.

4.1.1 Direct Energy Balance Enforcement

In the direct energy balance method, the post switching on-state switch current i_{0+} is equated to the pre switching on-state switch current i_{0-} , and similarly for the off-switch voltages. This is reasonable, assuming continuity of the load current is instantaneously transfers from the pre switching on-state switch to the post switching on-state switch without a change in magnitude at the switching instant. The enforcement process is shown in Fig. 4-1

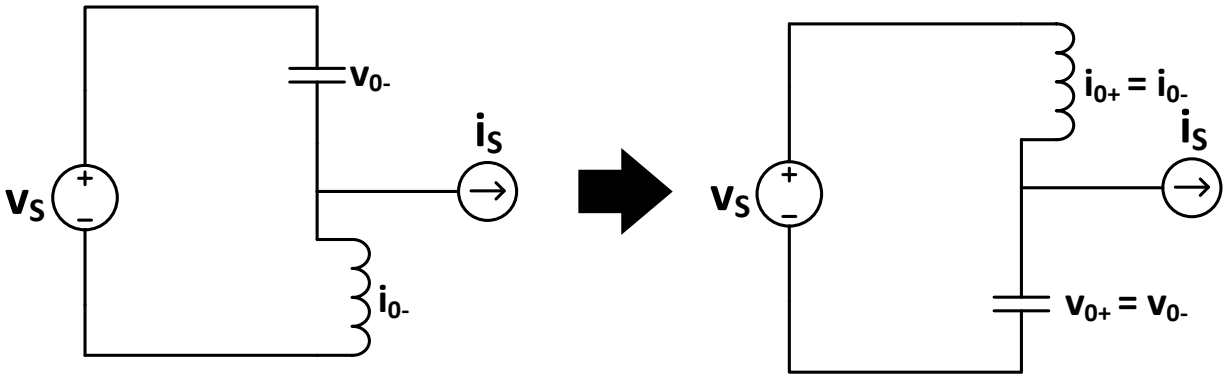


Figure 4-1 Direct energy enforcement

4.1.2 Optimized Energy Balance Enforcement

An alternative and potentially better solution to the post-switching initialization could be achieved through the process of optimization.

An optimization example is selection of post switching voltage and current values such that the current oscillation overshoot is minimized. Recall in the post switching switch current equation (3.13a) there is a dedicated component which reflects the oscillation overshoot. This oscillation component derived in equation (3.13a) is shown as equation (4.2) for ease of reference.

$$i_{sw(overshoot)} = \sqrt{(i_{0+} - i_S)^2 + G^2(v_{0+} - v_S)^2} \qquad (4.2)$$

Isolate v_{0+} to one side in (4.1) to obtain (4.3), where nrg is the total post switching switch energy which is (4.1)'s left hand side.

$$v_{0+} = \sqrt{\frac{nrg - Li_{0+}^2}{C}} \qquad (4.3)$$

Substituting (4.3) into (4.2) and reformulating to (4.4):

$$f(i_{0+}) = \sqrt{i_{0+}^2 - 2i_{0+}i_S + i_S^2 + G^2\left(\frac{nrg - Li_{0+}^2}{C}\right) - 2G^2 v_S\sqrt{\frac{nrg - Li_{0+}^2}{C}} + G^2 v_S^2} \qquad (4.4)$$

To find the minimum, we take the derivative of (4.4) and equate it to zero to obtain (4.5)

$$\begin{aligned} 0 = {} & i_{0+}(8i_S Cnrg - 8i_S G^2 Lnrg) \\ & + i_{0+}^2\left(4G^2 v_S^2 L^2 + 4i_S^2 LC - \frac{nrg4G^4L^2}{C} - 4Cnrg + 8G^2 Lnrg\right) \\ & + i_{0+}^3(8i_S G^2 L^2 - 8i_S LC) + i_{0+}^4\left(\frac{4G^4L^3}{C} + 4LC - 8G^2L^2\right) - 4i_S^2 Cnrg \end{aligned} \qquad (4.5)$$

Equation (4.5) is solved to give an i_{0+} which gives the global minimum for (4.4). i_{0+} is then substituted back into (4.3) to obtain a v_{0+}.

Different optimization methods can also be employed depending on the variable user want to optimize. For this research, energy balance enforcement will be based on the direct method because it provides an adequate amount of oscillation minimization with much less computational effort.

To demonstrate the effect of energy balance a simulation test is performed using the Two-Level Converter (TLC) shown on Fig. 3-3 (a). Fig. 3-3 a) is shown below for ease of reference.

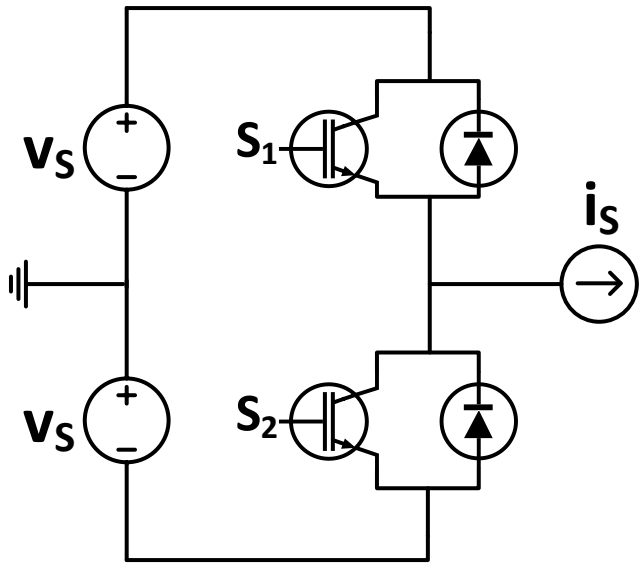
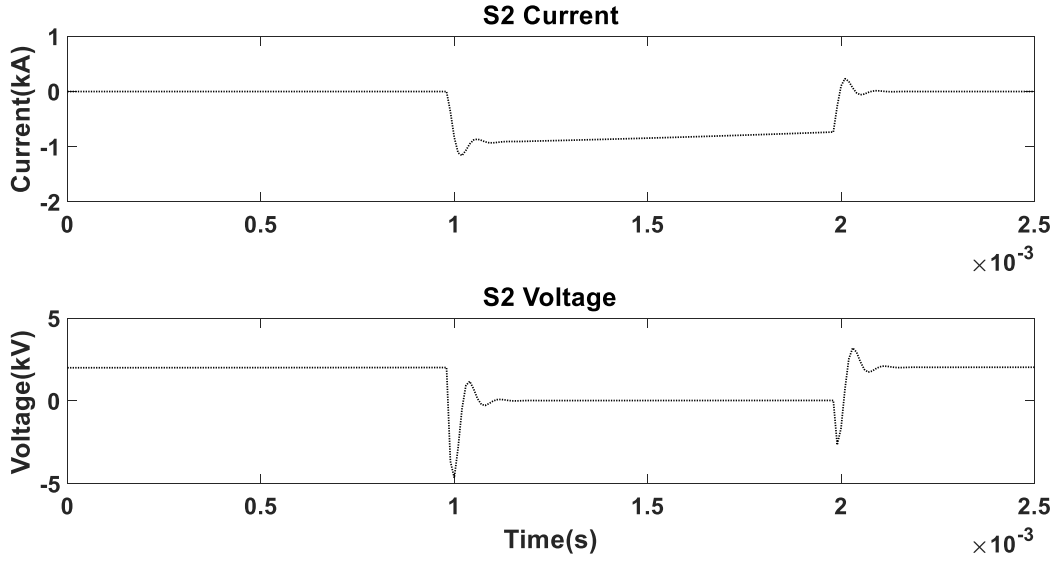
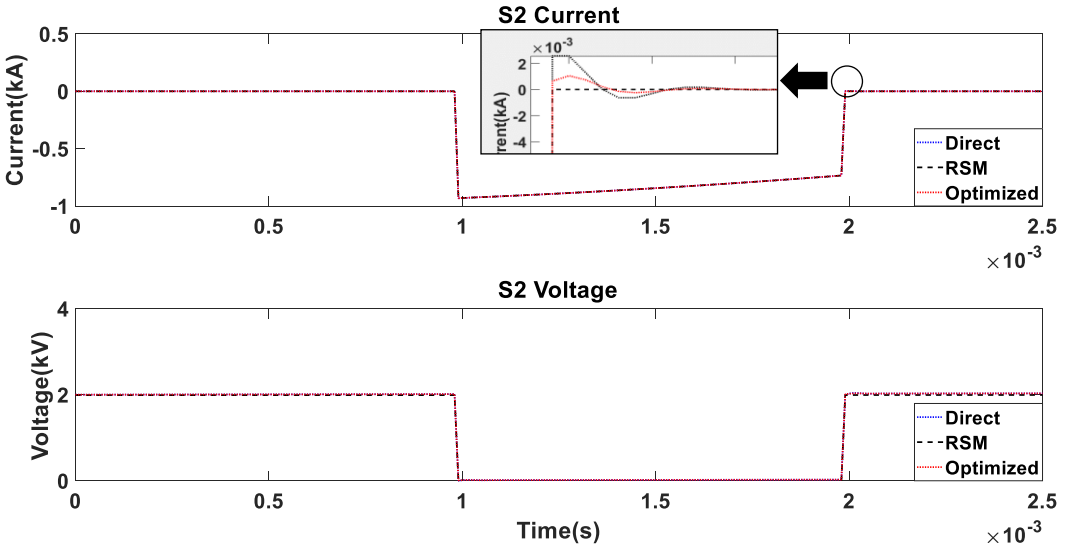


Fig. 3-3 TLC topology

In this simulation the dc voltage sources are set to $v_S = 1kV$ and ac current source is set to $i_S = \cos(2\pi 60t)\ kA$. Simulation is performed using i) the traditional LCSM, ii) energy balanced LCSM using the direct method and iii) energy balanced LCSM using optimization, and IV) the benchmark RSM. The spurious switching oscillations are shown on Fig 4-2.



(a)



(b)

Figure 4-2 Simulation waveforms a) Traditional LCSM switching oscillation; b) Energy balanced LCSM switching oscillation

Fig. 4-2 (b) shows that energy balance enforcement will significantly reduce the amount of spurious oscillations and eliminate the switching loss. Optimization applied successfully reduces the switch current oscillation however the direct energy balance method also provide an almost identical result, and so is the author's recommendation.

4.2 RC/RL Switch Model

In this research a new constant admittance-based switch topology, RC/RL (RC/RL SM) is proposed and the theory behind will be explained further in this subsection.

Like RSM and LCSM, RC/RL SM is a simplified switch model. It's designed to behave like an open circuit in off state and short circuit in on state. RC/RL SM is unique in its zero-magnitude discrete domain eigenvalue. One can claim the closer eigenvalue is to the center of unit in the discrete plane the higher the damping. Therefore, in theory a system with zero magnitude discrete time eigenvalue will be able to reach post switching Steady-State instantly without any oscillation. By changing the switch model topology and using specific integration method the RC/RL SM is able produce a zero magnitude discrete eigenvalue switch system.

The RC/RL SM consist of two versions, RCSM which uses a small resistor "R_{on}" for the on-state switch and, a small capacitor "C_{off}" for the off-state switch. The RLSM version uses a

small inductor "L_{on}" for the on-state switch and a large resistor "R_{off}" for the off-state switch. Both will be described in detail in the following subsection.

4.2.1 RC Switch Model

If the simulation of the switching network employs RCSM, then the switch is represented as a small resistor "R_{on}" in the on-state and a small capacitor "C_{off}" in the off-state. In the on-state, the switch will behave like an on-state RSM and the current will conduct through the switch as if it's a short circuit assuming the on-state admittance is negligible comparing to the rest of the circuit admittance. In off-state, if the off-state capacitor is fully energized it will behave as an open circuit just like an off-state LCSM. The RCSM also permits a constant admittance switch topology if the condition in (4.6) is enforced, where G_{Ron} and G_{Coff} are the on-state, and off-state switch conductance respectively.

$$G_{Ron} = G_{Coff} \qquad (4.6)$$

The unique difference between RCSM and LCSM is if trapezoidal integration method is applied to LCSM then a marginally stable system is formed. However, if trapezoidal rule of integration is applied to RCSM then the complementary switching topology results in a first order system which means oscillation free transient. To demonstrate RCSM's effectiveness the dynamics of the switch model will be analyzed next and compared against traditional LCSM and RSM using the elementary complementary switch set.

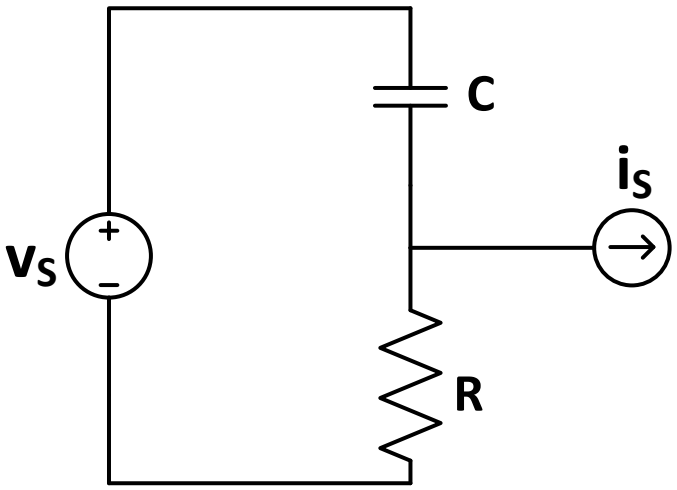


Figure 4-3 RCSM VSC cell

The state space of RCSM system shown in Figure 4-3 can be described as (4.7), where v_C the off-state capacitor voltage is.

$$\frac{d}{dt}[v_c] = \left[-\frac{1}{C_{off}R_{on}}\right][v_C] + \left[\frac{1}{C_{off}R_{on}} \quad \frac{1}{C_{off}}\right]\begin{bmatrix} v_S \\ i_S \end{bmatrix} \quad (4.7)$$

The eigenvalue of (4.7) is shown in (4.8). This represents a first order system which is as expected from a RC circuit topology.

$$\lambda = -\frac{1}{C_{off}R_{on}} \quad (4.8)$$

Applying trapezoidal rule of integration to discretize (4.7) into (4.9). The discrete eigenvalue can also be calculated as (4.10).

$$v_{\mathrm{C_{off}}}[n+1] = \frac{2C_{off}R_{on} - \Delta t}{2C_{off}R_{on} + \Delta t} V_{C_{off}}[n] + \frac{2\mathrm{C_{off}R_{on}}}{2C_{off}R_{on} + \Delta t}\left(\frac{v_S \Delta t}{C_{off}R_{on}} + \frac{i_S \Delta t}{C_{off}}\right) \quad (4.9)$$

$$\lambda' = -\frac{2 + \frac{-\Delta t}{C_{off}R_{on}}}{\frac{-\Delta t}{C_{off}R_{on}} - 2} \quad (4.10)$$

Equation (4.6) can be rewritten as (4.11) using trapezoidal integration method. Substituting (4.11) into (4.10) will yield (4.12) which confirms the discrete eigenvalue of the RCSM is zero.

$$G_{\mathrm{Ron}} = G_{Coff} = \frac{1}{R_{on}} = \frac{2C_{off}}{\Delta t} \quad (4.11)$$

$$\lambda' = -\frac{2 + \frac{-2\Delta t}{\Delta t}}{\frac{-2\Delta t}{\Delta t} - 2} = -\frac{2-2}{-2-2} = 0 \qquad (4.12)$$

Comparing (4.12) to the traditional LCSM discrete time eigenvalue (3.12), repeated below for reference, from chapter 3, it is safe to say during the switching dynamic RCSM is significantly shorter due to eigenvalue location.

$$\lambda'_{1,2} = 0.5 \mp j0.5 \qquad (3.12)$$

Assume the post switching voltage/current terms are set to zero due to lack of history information during switching. An analytical solution for equation (4.9) can be solved by finding its homogeneous and the particular solutions which satisfies this initial condition.

Homogeneous solution is defined as:

$$\mathrm{V}_{\mathrm{Chonmo}}[n] = C_1 0^n = 0 \qquad (4.13)$$

Particular solution is defined as:

$$\mathrm{V_{Cpart}}[n] = \beta \qquad (4.14)$$

Substituting into (4.9) to obtain (4.15) and further simplification to (4.16) using (4.11) gives.

$$\beta = \frac{2C_{off}R_{on} - \Delta t}{2C_{off}R_{on} + \Delta t}\beta + \frac{2\mathrm{C_{off}R_{on}}}{2C_{off}R_{on} + \Delta t}\left(\frac{v_S \Delta t}{C_{off}R_{on}} + \frac{i_S \Delta t}{C_{off}}\right) \qquad (4.15)$$

$$\beta = \frac{0}{2\Delta t}\beta + \frac{1}{2}(2v_S + 2R_{on}i_S) = v_S + R_{on}i_S \qquad (4.16)$$

The complete solution (4.17) is the summation of (4.13) and (4.16)

$$v_{\mathrm{C}}[n] = v_S + R_{on}i_S \quad (4.17)$$

Therefore, regardless of time step, the response of this model is instantaneous. Capacitor voltage will reach steady state instantly, i.e. without the oscillatory behavior of the original LC switch, and in steady-state the capacitor voltage will be exactly like in the RSM.

4.2.2 RL Switch Model

Just as its name suggest the RLSM represents the switch as a large resistor 'R_{off}' when in the off-state and a small inductor 'L_{on}' when in the on-state. Using similar steps as in section 4.2.1 for the RC version, the RLSM can also be shown to exhibit a zero-magnitude discrete eigenvalue characteristics in a switched system.

First consider a RLSM VSC cell shown in Figure 4-4. Its state space can be derived as (4.18) and its Eigenvalue is (4.19). In this case i_{Lon} is the on-state inductor current.

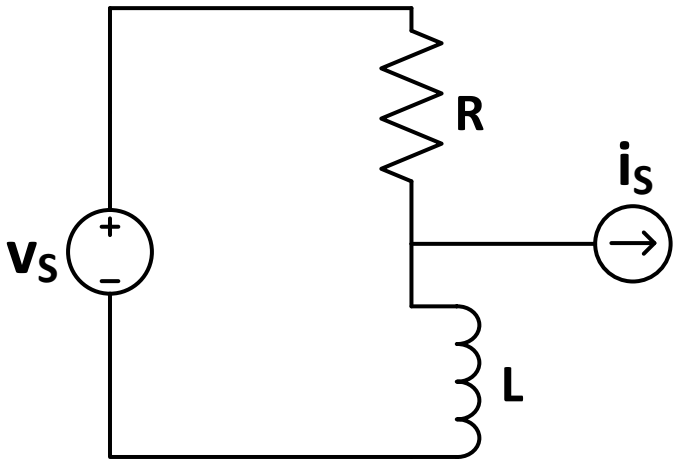


Figure 4-4 RL type LCSM VSC cell

$$[i'_{Lon}] = \left[-\frac{R_{off}}{L_{on}}\right][i_{Lon}] + \left[\frac{1}{L_{on}} \quad \frac{R_{off}}{L_{on}}\right]\begin{bmatrix} v_S \\ i_S \end{bmatrix} \qquad (4.18)$$

$$\lambda = -\frac{R_{off}}{L_{on}} \tag{4.19}$$

Applying trapezoidal integration to discretize the system and one can find the corresponding discrete eigenvalue to be as in (4.20) which can be further simplified to 0 when the constant admittance property (4.21) is invoked.

$$\lambda' = -\frac{2 - \frac{\Delta t R_{off}}{L_{on}}}{-\frac{\Delta t R_{off}}{L_{on}} - 2} = 0 \tag{4.20}$$

$$G_{\mathrm{Roff}} = G_{Lon} = \frac{1}{R_{off}} = \frac{\Delta t}{2\mathrm{L_{on}}} \tag{4.21}$$

After converting (4.18) to a difference equation and repeating the same steps from the previous subsection the post switching current equation is found to be (4.22), which again shows an instantaneous response, i.e., there is no oscillation due to the switching.

$$i_{Lon}[n] = \frac{v_S}{R_{off}} + i_S \tag{4.22}$$

4.2.3 Advantage and Disadvantage of RCSM

Advantage:

Like the LCSM, being a constant admittance type switch model eliminates the need for re-factorization during switching for the RC/RL SM too. Additionally, the RC/RL SM has a significantly shorter spurious transient period than the traditional LCSM. Spurious switching transient suppression of traditional LCSM using energy balance requires pre knowledge of simulated VSC topology. However, a predictive type algorithm can be employed to eliminate the switching transient of the RCSM and the pre knowledge of simulated VSC topology is not needed. Hence it is possible for RCSM to become general propose drag and drop type switch model for the EMT simulator.

Disadvantage:

The RC/RL SM's switch admittance is not as flexible comparing to the LCSM. This is because the on-state resistor in the RCSM and off-state resistor in the RLSM has a typical values R_{on} = 0.01Ω and $R_{off} = 10^6\Omega$ in EMT type simulation. The corresponding capacitance and inductance values for the RC and RL representations are as in (4.23) and (4.24) respectively.

$$C_{off} = 50\Delta t \qquad (4.23)$$

$$L_{on} = 5 \times 10^5 \Delta t \qquad (4.24)$$

This means the RC/RL SM can only adjust its on-state inductance for the RL type, and off-state capacitance for the RC type through simulation time step. On the other hand traditional LCSM can adjust both G_{SW} and Δt to reach a desired switch inductance/capacitance for its simulation network.

Another important point to note is that with a typical simulation time step of $\Delta t = 50\mu\text{sec}$ the on-state inductance of the RLSM has a value of $25H$. Which is most likely to be too large for the system to be simulated. In order to make sure the switch inductance of the RLSM is small enough such that it is negligible compare to the system its connected to an unrealistically small simulation time step is needed, hence only RCSM is recommended and used in this thesis.

Without any sort of compensation the RL/RC SM will produce voltage/current spikes during switching for both the RL and RC versions. This spike is due to the resetting of capacitor voltage (for the RC switch) to zero when the switch turns off, or inductor current (for RL switch) to zero when the switch turns on. If some knowledge of the post-switching state is available, it may be possible to select a suitable value for these reset quantities other than zero. However, without any such information, this is not possible. This voltage or current shows up as a history term when calculating the next time step solution. As a result, due to the 1 time step steady-state

characteristic of the RC/RL SM, the corresponding $i_{Coff} = C_{off}\frac{dv_{Coff}}{dt}$, and $v_{Lon} = L_{on}\frac{di_{Lon}}{dt}$ will be very high. However this spike can be eliminated using a predicative method which will be discussed in the following subsection.

4.2.4 Elimination of Spurious Switching Impulse Using Predictive Subroutine

Section 4.2.3 considered the advantages and drawbacks of RC/RL SM, and one of the main disadvantages is the spurious switching spike from resetting of switch voltage (in RC switch) or current (in RL switch) due to lack of information about the new state. This means if an appropriate post switching voltage and current can be selected for the RC/RL SM then elimination of the spurious spike is also possible. In this research a predictive type method is proposed to select a suitable post switching history term for the switches. This will be explained using the following VSC cell undergoing a switching event simulated using the RCSM as shown in Fig. 4-5. The red highlighted part of circuit is the current conduction path.

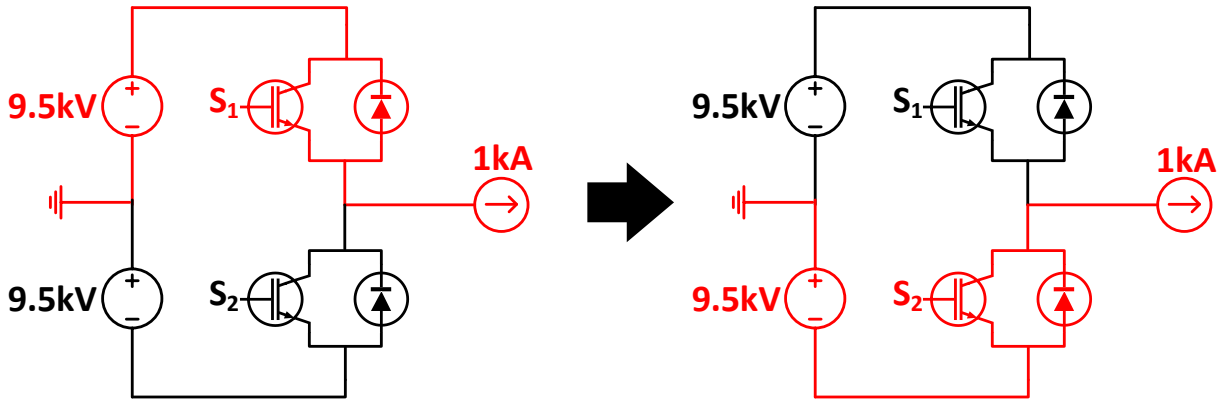


Figure 4-5 VSC cell switching

Simulation is ran for $70\mu sec$ at $1\mu sec$ simulation time step. The voltage and current waveform of S2 is plotted in Fig. 4-6. Pre-switching, S2 is in the off state (capacitor) and S1 is on. Assume an RC switch. The voltage across S2 is 19 kV and the current is 1 kA. A switching action is conducted at $35\mu sec$, by turning S1 off, i.e., going to capacitor representation and S2 off, i.e., resistor representation. Due to its capacitor voltage being reset to zero for S1 at switching, the simulation sees both switches as on resistances. As a result, the dc side voltage is divided equally across the two small resistor (the on-state value), producing the spurious current spike of 950 kA. In the next time-step, RCSM then converges immediately to the steady state with near-zero voltage and 1 kA current.

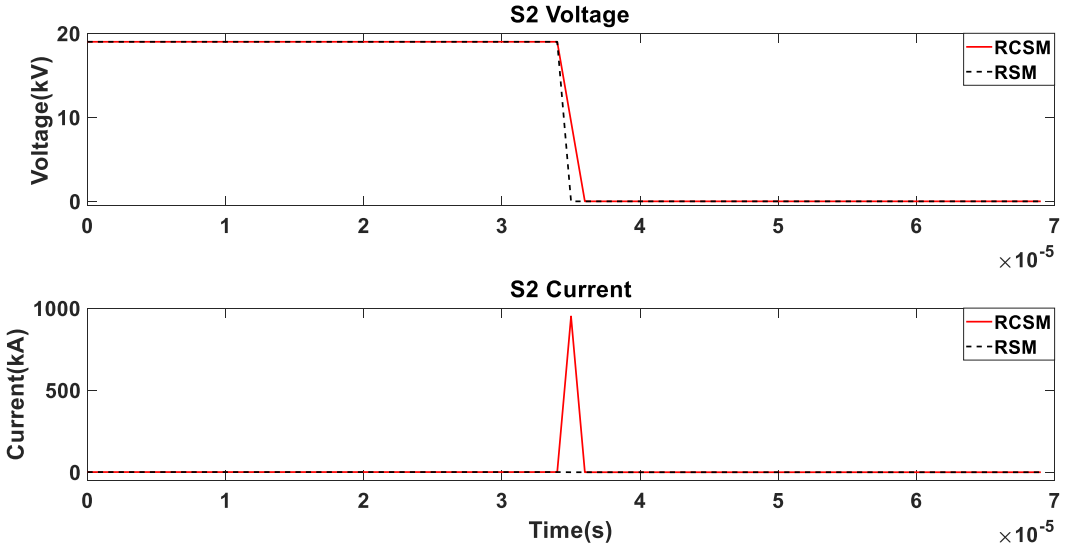


Figure 4-6 RCSM VSC cell switching waveforms with no compensation

The following algorithm is thus used to remove the spike. When the switching signal is received, a predictive subroutine is commenced without advancing the simulation time-step. The purpose of the subroutine is to estimate the post-switching voltage, i.e., capacitor voltage across the new off-state switch S1. A simplified model of the switch assembly is simulated in the predictive subroutine assuming external voltages and currents fixed at their pre-switching values. A one to two time-step simulation is carried out in the subroutine which gives a very good estimate of the post-switching voltage and current. The subroutine is exited and the calculated voltage or current value assigned to the initial voltage on the capacitor (or inductor). Now the main EMT simulator is allowed to advance its time-step and continue with the simulation. As the voltage across S1 is no longer zero, the current spike is essentially eliminated.

Fig. 4-7 repeats the simulation in Fig. 4-6, but this time with the setting of the capacitor value via the predictive subroutine. As before, S2's switch voltage and current is plotted in the figure. It can be seen that the spurious switching impulse is eliminated and RCSM's waveform matches the benchmark RSM waveform.

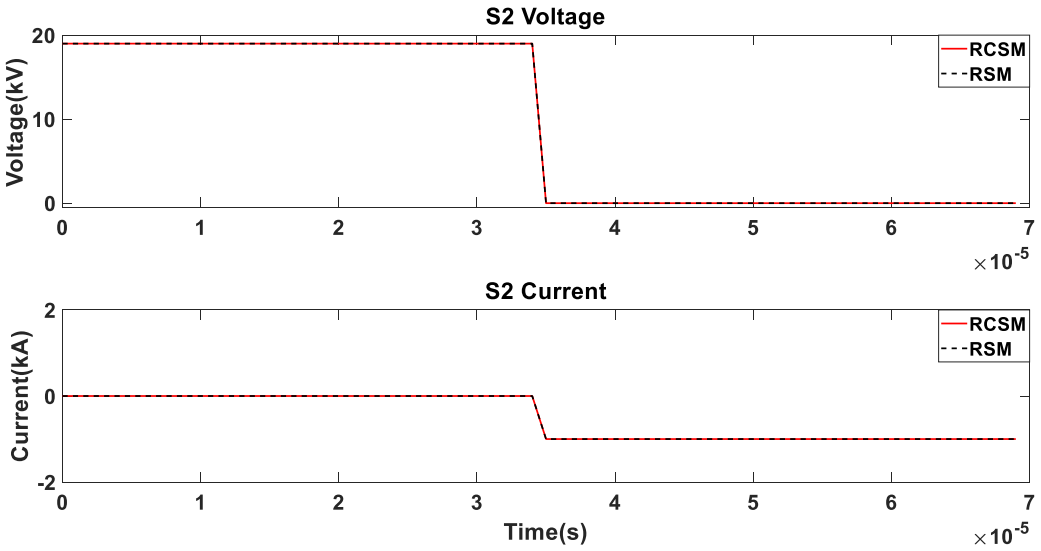


Figure 4-7 RCSM VSC cell switching waveforms with predictive subroutine

5 Model implementation

Chapter 3 introduced two methods to suppress spurious switching transient of the traditional LC Switch Model (LCSM). Furthermore the effectiveness of the methods were also demonstrated using the fundamental VSC cell. In this chapter a detailed sequential procedure on how the method is implemented on an Electro-Magnetic Transient (EMT) program is described. Implementation for some commonly seen VSC topologies are also explained. In this research all switches implemented are assumed to be bidirectional.

5.1 Energy Balance LC Switch Model Implementation

Section 4.1 has shown that the direct energy balance method can successfully mitigate the spurious energy loss and suppress the spurious oscillation of traditional LCSM. The direct energy balance method equates the post switching switch voltage and current to the pre switching switch voltage and current of its complement. Therefore, the first step of energy balance implementation is to identify the complementary switches of the simulated topology. This is done by examining all the different operating mode of the VSC and identify its current commutation path during all mode change.

Once all the complementary switches are determined, the next step is to create an energy exchange Table. When forming the energy exchange table there are two elements to consider: the

VSC's operating modes and its state transition logic. Once the energy exchange table is formulated then energy balance can be implemented accordingly to the Table.

5.1.1 Two-level converter energy balance LCSM implementation

Following the procedures presented in the previous subsection, we first determine all the complementary switch sets by examining the current commutation path during all mode changes. For the Two-Level Converter (TLC), the two possible operating modes are shown in Fig. 5-1. When operating modes changes from mode 1 to mode 2, current commutates from S1 to S2. The complementary commutation path also applies for mode 2 to mode 1. Therefore {S1, S2} is the only complementary switch set in the TLC.

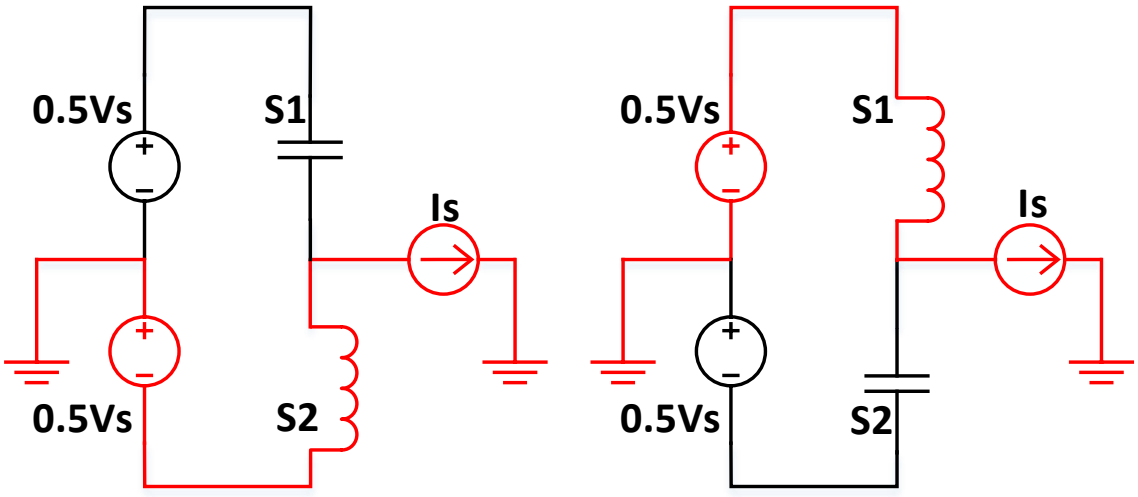


Figure 5-1 Two-level converter current path in a) mode 1; b) mode 2

After identifying all the complementary switch sets, the next step is to formulate the energy exchange table. Based on the current commutation path during mode change Table 5-1 is formulated below

Table 5-1 Two-Level Converter Energy Exchange Table

Mode Change	S1's complement	S2's complement
Mode 1 to Mode 2	S2	S1
Mode 2 to Mode 1	S2	S1

Table 5-1 acts as a look up table for the switches when switching occurs. The algorithm flow chart for the switches is shown in Fig. 5-2. This flowchart can be used to implement all energy balance LCSM. The only difference between each energy balance LCSM is the energy exchange look up Table as it varies from topology to topology.

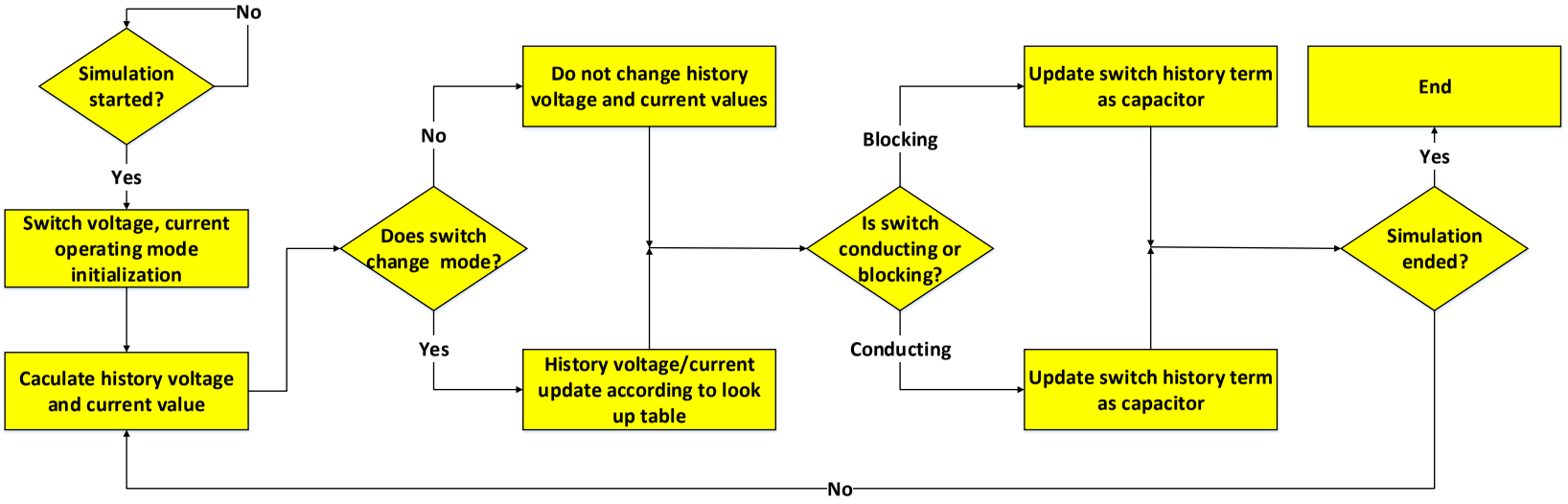


Figure 5-2 Energy balance LCSM simulation flowchart

The energy balance LCSM is implemented in PSCAD via the component wizard which allows one to develop the graphics and insert any additional custom FORTRAN code. In this case the variable RLC subroutine of PSCAD is used to realize the model by insertion of the switch conductance and switch history current injection into the admittance matrix and current matrix of the solution respectively. An addition of switch logic needs to be added to the subroutine where the individual switch's history voltage and current information is exchanged so the energy balance algorithm shown in Fig.4-1 is enforced. Fig.4-1 is shown below for ease of reference.

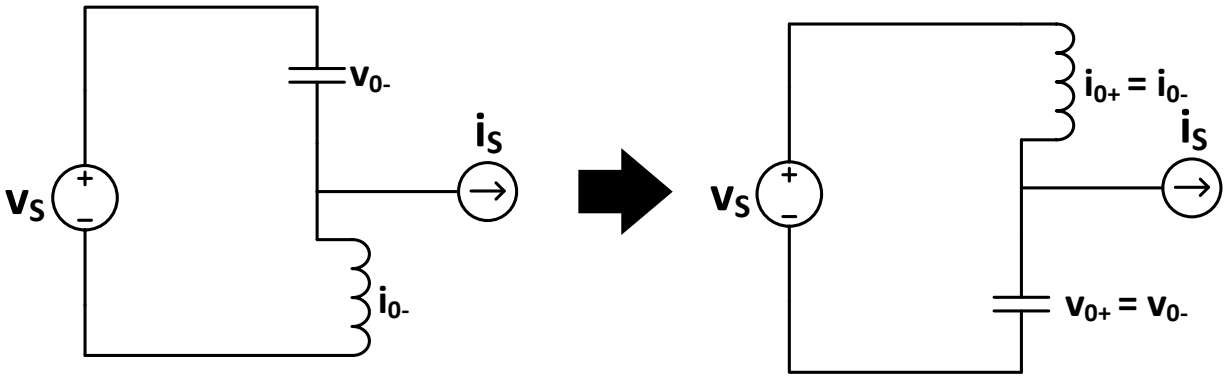


Figure. 4-1 Direct energy enforcement

Fig. 5-3 shows the customized switch component as it appears on the PSCAD palette for connection with other components. The switch component consist of 2 electrical ports {Pos, Neg} for circuit connection propose, 2 output signal ports $\{v_{out}, i_{out}\}$ for transfer of voltage and current information to its complement and 3 input signal ports $\{v_{in}, i_{in}, GS\}$ for receive voltage, current and gate signal respectively. This implementation method is valid for all energy balance LCSM.

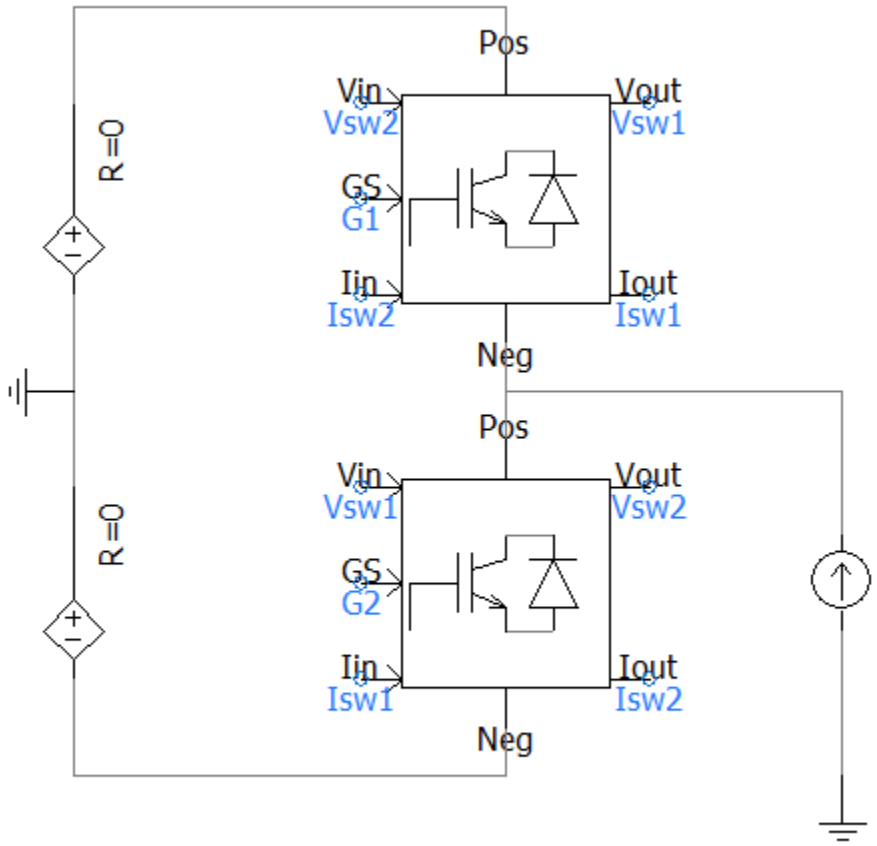
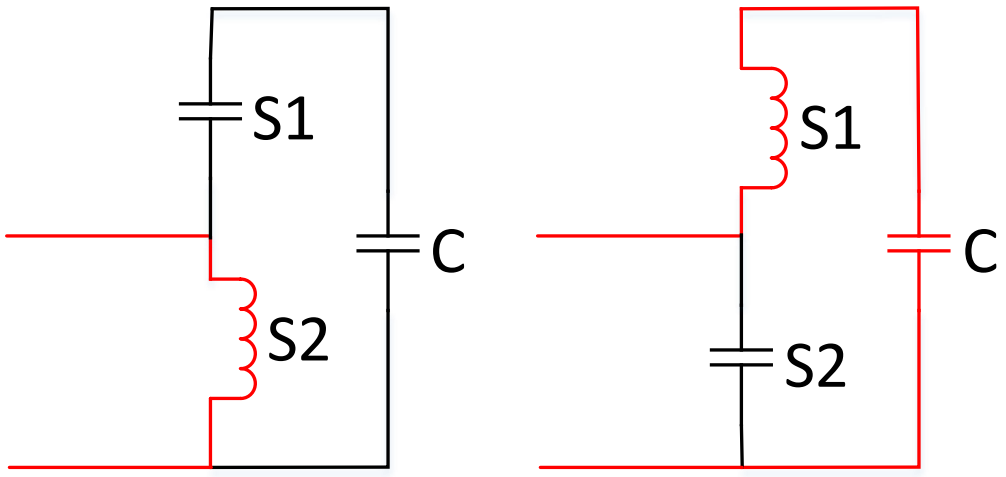


Figure 5-3 Energy balance LCSM realization in PSCAD

5.1.2 Modular Multi-level VSC energy balance LC Switch Model Implementation

Due to its modularity, the model for the Modular Multi-level VSC (MMC) LCSM implementation can be simplified significantly. Normally MMC consists of scores or even hundreds of switches in each arm. However, there is no need to derive each set of complementary

switch and all different modes. This is because all submodules (SM) are identical to each other and they operate independently. Therefore once the complementary switch set and energy exchange Table is derived for one SM then it can be used for all of the SM inside the converter. SM's operating modes are shown in Fig. 5-4 and energy exchange logic is tabulated in Table 5.2.



(a) (b)

Figure 5-4 MMC VSC a) bypass mode; b) insertion mode

Table 5-2 Modular Multi-level Converter Sub-Module Energy Exchange Table

	S1's complement	S2's complement
Bypass to insertion	S2	S1
Insertion to bypass	S2	S1

5.2 RC Switch Model Implementation

The RC/RL Switch Model (RC/RL SM) switch can also be implemented using the component wizard and RLC subroutine as was described for the LCSM in section 5.1. The only difference is the calculation of the injected current source which is done as described in section 4.2.4.

Unlike the LCSM, a switching/energy transfer Table need not be constructed for the RC/RL SM. As explained in Section 4.2.4, the post switching solution is essentially transient free, a tentative time-step is taken in the model to find the future solution, which gives the setting voltage and current values for the switches. Thus, the topology does not have to be pre-known. RCSM's simulation procedure is shown as a flowchart in Fig. 5-5.

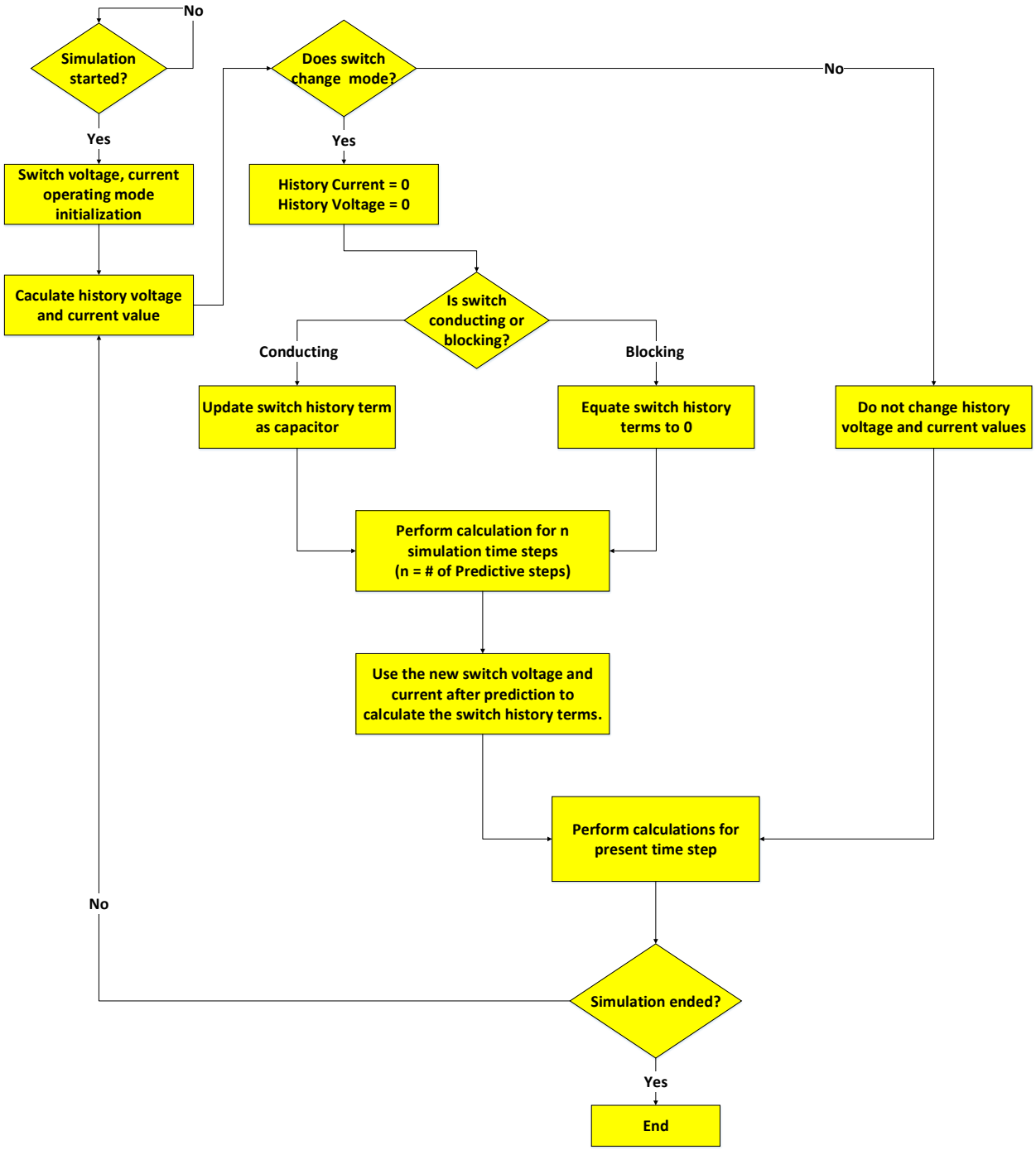


Figure 5-5 RCSM simulation flowchart

Following the procedures shown in Fig. 5-5 the proposed RCSM is implemented in both Matlab and PSCAD.

5.2.1 Three Phase Diode Bridge Rectifier RC Switch Model Implementation

As an exercise, a three phase diode bridge rectifier was modelled from scratch in an EMT algorithm implemented fully in MATLAB, i.e., both the switch and external circuit are implemented in MATLAB. The later MMC example is implemented using the same algorithm for the switch, but using the features of the commercial program PSCAD or implementing an arbitrary external circuit. The simulated topology is shown in Fig. 5-6. The general simulation procedure still follows EMT type simulation using modified nodal analysis. Since a switch model is used in place of diode, a gate signal is given to the switch when the condition for an equivalent diode to conduct is reached.

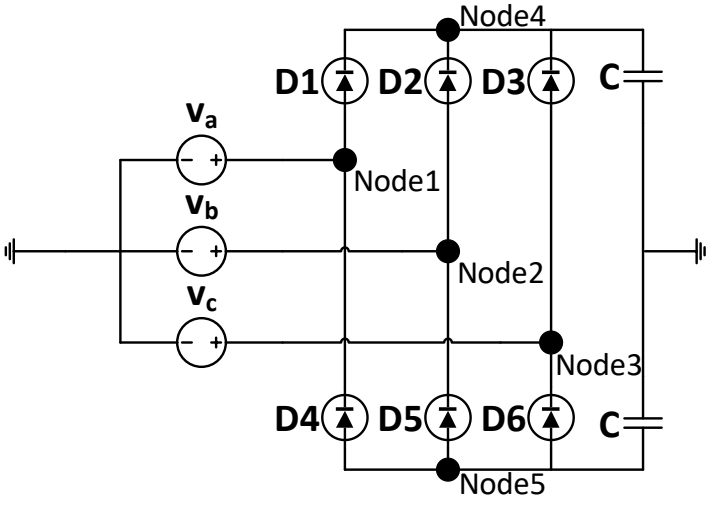


Figure 5-6 Three phase diode bridge rectifier

Firstly the simulation is initialized and appropriate values are given to $\{idhis_1$ to $idhis_6\}$, $\{ ichis_1, ichis_2\}$ which are the history current injection of the diodes and dc link capacitors respectively. Then admittance$[G]$, node voltage$[v]$, and current source $[i]$ matrix of simulated network is formulated in the form $[G][v] = [i]$ as (5.1), where $\{ G_{sw}\}$, $\{ G_C\}$, $\{ i_{va}, i_{vb}, i_{vc}\}$, $\{ v_1$ to $v_5\}$ is the switch admittance, load admittance, source currents, and node voltages respectively.

$$\begin{bmatrix} 2G_{sw} & 0 & 0 & -G_{sw} & -G_{sw} & 1 & 0 & 0 \\ 0 & 2G_{sw} & 0 & -G_{sw} & -G_{sw} & 0 & 1 & 0 \\ 0 & 0 & 2G_{sw} & -G_{sw} & -G_{sw} & 0 & 0 & 1 \\ -G_{sw} & -G_{sw} & -G_{sw} & 3G_{sw}+G_C & 0 & 0 & 0 & 0 \\ -G_{sw} & -G_{sw} & -G_{sw} & 0 & 3G_{sw}+G_C & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ i_{va} \\ i_{vb} \\ i_{vc} \end{bmatrix}$$

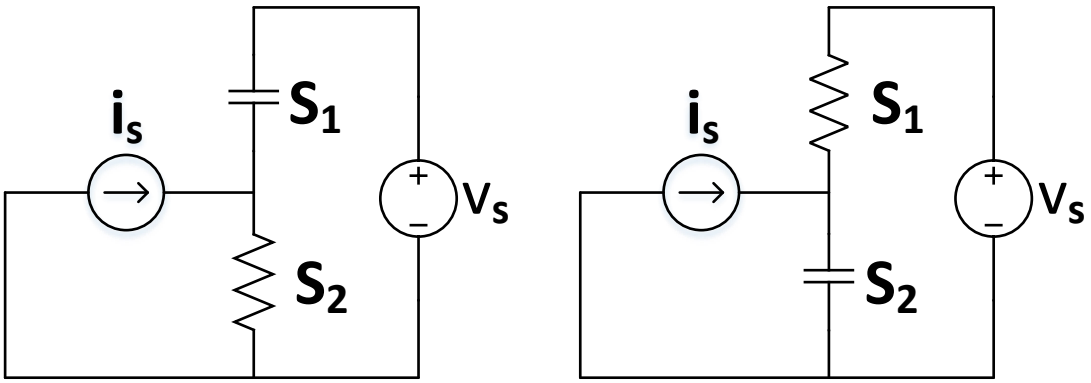
$$= \begin{bmatrix} idhis_1 - idhis_4 \\ idhis_2 - idhis_5 \\ idhis_3 - idhis_6 \\ ichis_1 - idhis_1 - idhis_2 - idhis_3 \\ idhis_4 + idhis_5 + idhis_6 - ichis_2 \\ v_a \\ v_b \\ v_c \end{bmatrix} \quad (5.1)$$

Then gate signal is formulated for the switches depending on the voltage across the RC/RL SM. For the upper arm when $v_n > v_4$ ($n\ from\ 1\ to\ 3$), the corresponding RC/RL SM is given an on signal or else an off signal. For the lower arm when $v_n < v_5$ ($n\ from\ 4\ to\ 6$), the corresponding RCSM is given an on signal or else an off signal.

After gate signals are formulated, individual RCSM then determine if switching event occurred. If no switching is to happen then simulation advances as normal EMT program by calculating the node voltage matrix performing $[A]^{-1}[i] = [v]$. The new set of voltage and current values are used to formulate the history current injection for next time step, which allows calculation of the voltages and currents in the next time-step. This process is continued until the simulation end time is reached. However if switching occurs as a result of the diode transitioning between forward and reverse bias conditions (i.e., by the voltage across it changing sign), then a predictive subroutine is entered where the history current of the individual switch which has been toggled is reset to zero. All corresponding source values are frozen during this operation and simulation is performed for the next n-time-steps by where n can be set by user. This is a calculation internal to the subroutine and the time-step of the wider EMT algorithm is not advanced. Typically n = 1 or 2 as described in section 4.2.4, with a steady-state solution s obtained after n-internal time-steps. On exiting the subroutine the new set of history current injection values which are formulated using the final voltage after n steps is returned. The simulation time-step for the EMT program is now advanced, and normal EMT simulation continues till the next switch operation.

5.2.2 Modular Multi-level VSC RC Switch Model Implementation

The same MMC HVdc network in section 5.1.2 is also simulated with the RCSM using PSCAD. This is done by representing each SMs as individual complementary sets. The SM is represented as the equivalent circuit shown in Fig.5-7 during switching. The predictive subroutine as described in the previous section is used to set the post-switching history currents.



(a) (b)

Figure 5-7 MMC SM RCSM equivalent circuit a) blocking mode b) insertion mode

Similar to section 5.1.1 the RCSM is implemented via custom component using FORTRAN in PSCAD. Based on the variable RLC subroutine, a switching logic needs to be added where the history voltage $v_S[t-\Delta t]$ and history current $i_S[t-\Delta t]$ is equated as (5.2) and (5.3) for S1 and S2 respectively for the off-state capacitor mode of operation. These equations are derived from the discrete time state space EMT update scheme of Fig 5-7.

$$i_{S1}[t-\Delta t]=0 \qquad (5.2a)$$

$$v_{S1}[t-\Delta t]=\ v_C-\frac{i_S}{G_{sw}} \qquad (5.2b)$$

$$i_{S2}[t - \Delta t] = 0 \qquad (5.3a)$$

$$v_{S2}[t - \Delta t] = v_C + \frac{i_S}{G_{sw}} \qquad (5.3b)$$

6 Validation of Proposed Model

In this chapter, the proposed approaches for efficient implementation of the power electronic switch are investigated. These include the energy balanced LC Switch Model (LCSM), and the RC Switch Model (RCSM). The behavior of the proposed model for simulating three common VSC topologies is examined. The viability of the energy balance LCSM using the Two-Level Converter (TLC) topology and the Modular-Multilevel Converter (MMC) topology is first investigated. Next, the viability of the RCSM using the three phase diode bridge rectifier topology and the MMC topology is considered.

6.1 Energy Balance LC Switch Model Validation

In order to verify energy balance LCSM, three simulation tests are performed.

The first simulation is an open loop controlled three phase TLC. The open loop control will ensure all switches receive the same gate signal at every time step. This is to compare the switching characteristics between models.

The second simulation is a TLC based STATCOM to improve the voltage profile of a connected ac network. This test is to verify the performance of the energy balance LCSM when connected to realistic ac systems with a full control system.

In the third simulation a MMC based HVDC link is simulated. This test is to verify whether the accuracy is improved and losses are reduced, when energy balance is applied in the simulation of a large network with semiconductor switches. Another purpose is to verify whether the traditional LCSM's speed advantage is retained when energy balance is applied.

6.1.1 Open Loop two level converter simulation

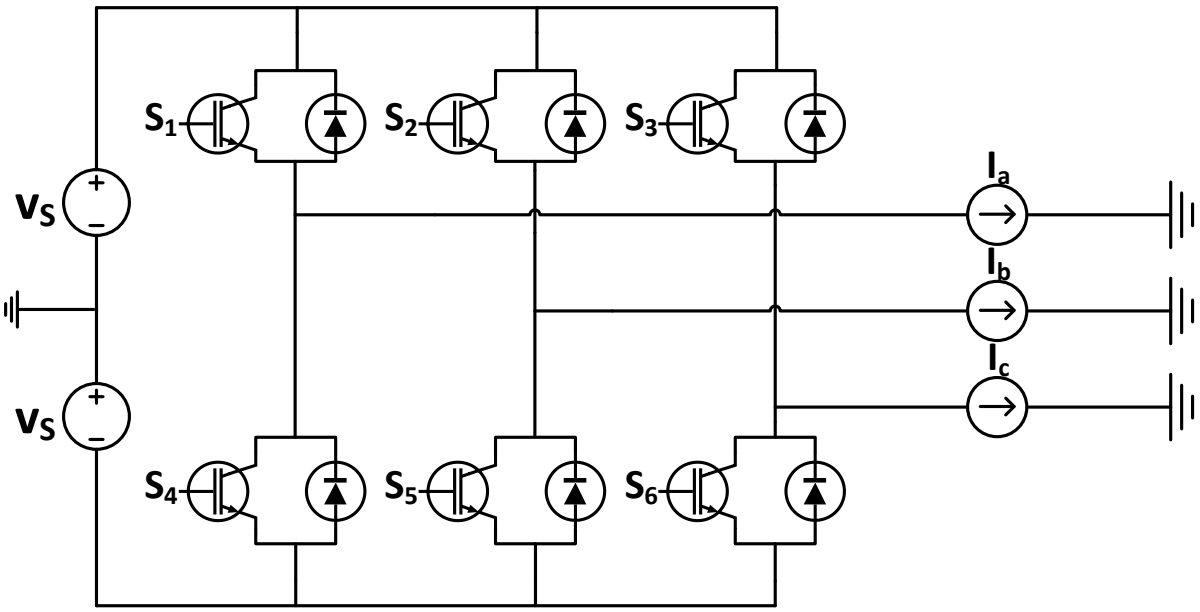


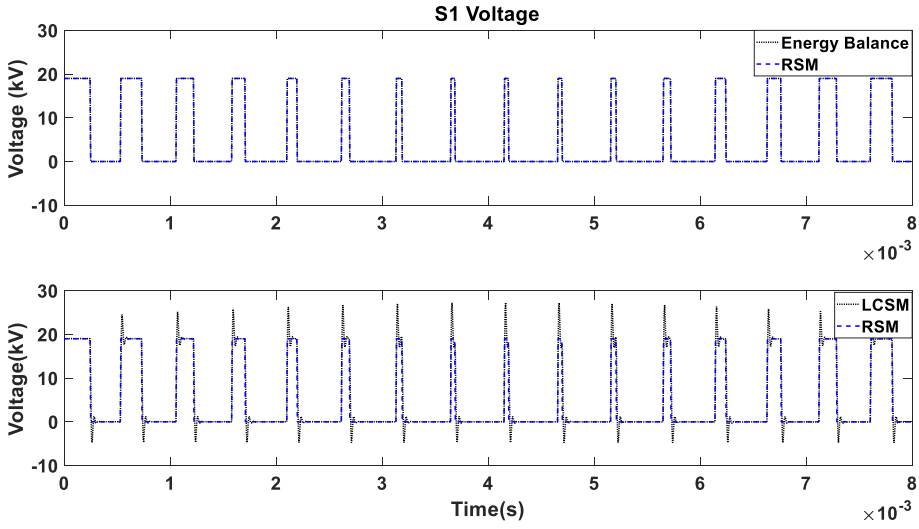
Figure 6-1 TLC PSCAD test case

In this section a Sinusoidal Pulse Width Modulator (SPWM) controlled TLC is simulated. For parametric testing, an idealized network is used as shown in Fig. 6-1. It has an ideal dc voltage source and the load modeled as an ideal current source. Also, the control is open loop meaning that real or reactive current control loops are not present. Instead, it is assumed that the switches are operated with a SPWM as described in section 2.1. A three phase balanced sinewave of 60 Hz frequency modulating signal is compared with a 1.98 kHz (33^{rd} harmonic of 60 Hz) triangular carrier to produce the switching signals. The modulation index is 0.8. System parameters are tabulated in Table 6.1. In all cases, the Resistor Switch Model (RSM) is used as the template for comparison.

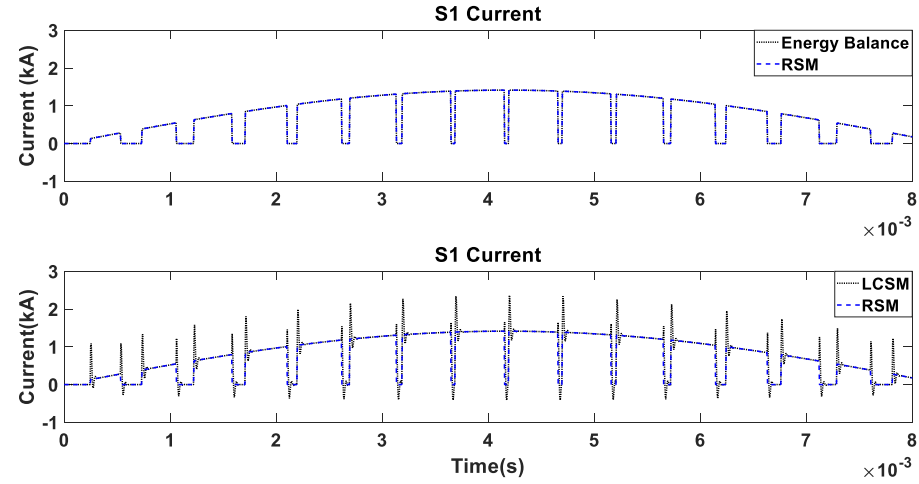
Table 6-1 Two-Level Converter Simulation Parameters

Parameters	Values
$v_S\ (DC - kV)$	9.5
$i_{abc}\ (RMS - kA)$	1
Base frequency	60 Hz
Simulation time step (μsec)	50
Switch admittance (S)	1
Switching frequency (kHz)	1.98

The current and voltage of S1 is plotted in Fig 6-2. As expected, when spurious switching loss and oscillation is suppressed the voltage and current of the energy balance LCSM completely overlays the benchmark RSM. On the other hand, the traditional LCSM displays significant amount of oscillation during every switching instance.



(a)



(b)

Figure 6-2 Switching waveform comparisons a) Switch voltage, b) Switch current

The maximum instantaneous overshoots are displayed in Table 6-2. Due to energy balance enforcement, the spurious switching loss and switching oscillation using the proposed energy-balance LCSM is essentially negligible. Whereas a 0.45 MW loss per switch is observed for the traditional LCSM! Hence using energy balance eliminates the spurious switching loss of the traditional LCSM. The RSM shows a small loss because of the non-zero resistance of the switch, but again is much smaller than the traditional LCSM. Of course, here we applied perfect energy balance to ensure zero energy loss. It is possible to modify the energy balance LCSM by estimating the conduction and switching loss of an actual switch and then reducing the stored energy by just that amount. However, this is not investigated further.

Table 6-2 S1 Instantaneous Simulation Deviations

Switch Model	Maximum Voltage Overshoot/Undershoot (kV)	Maximum Current Overshoot/Undershoot (kA)	Average Power Loss (MW)
LCSM	16.5693	1.6571	0.4536
Energy balance LCSM	0.0042	0.0026	1.32×10^{-6}
RSM	0	0	0.00086

In theory if the spurious energy loss is eliminated then regardless of switching frequency the amount of switching loss should always be zero for an ideal switch. This is confirmed by

operating the same VSC with different switching frequencies. The simulation results are tabulated in Table 6-3. As expected energy balance LCSM will always show a negligible amount of average power loss regardless of switching frequency. Due to the high frequency carrier used, this part of the simulation was done using time step of 1 μsec.

Table 6-3 S1 Average Power Loss vs Switching Frequency

Power (MW)	24 kHz	12 kHz	2.0 kHz	0.9 kHz
LCSM	1.1504	0.5498	0.0913	0.0415
Energy balance LCSM	9.73×10^{-8}	1.61×10^{-7}	3.61×10^{-8}	3.58×10^{-8}
RSM	0.00086	0.00086	0.00086	0.00086

Another important simulation parameter to look at is the simulation time step. It is expected that the spurious energy oscillation magnitude increases when simulation time step is larger for the energy balance LCSM. The reason for this is the $\Delta v = v_{0+} - v_S$ and $\Delta i\, \Delta i = i_{0+} - i_s$ term in the oscillation equation (3.13) increase with time step. As a result, the oscillation overshoot will also increase with time step. Equation (3.13) is repeated below for ease of referencing. Note in this case i_{S1} is the post switching on state switch current, and v_{S2} is the post switching off state switch voltage. This is confirmed when simulation is conducted using a simulation time step of 1 μsec and 10μsec. The simulation results for S1 is tabulated in Table 6-4.

$$i_{s1}[n\Delta t] = 2 \times 0.707^{n}\sqrt{0.25(\Delta i^2 + G_{sw}^2 \Delta v^2)} \times \cos(45°n + \theta_1) + i_s \qquad (3.13a)$$

$$v_{s2}[n\Delta t] = 2 \times 0.707^{n}\sqrt{0.25\left(\frac{\Delta i^2}{G_{sw}^2} + \Delta v^2\right)} \times \cos(45°n + \theta_2) + v_s \qquad (3.13b)$$

Table 6-4 S1 Instantaneous Simulation Deviations

	Maximum Voltage Overshoot/Undershoot (kV)		Maximum Current Overshoot/Undershoot (kA)		Average Power Loss (MW)	
	$\Delta t = 10\mu s$	$\Delta t = 1\mu s$	$\Delta t = 10\mu s$	$\Delta t = 1\mu s$	$\Delta t = 10\mu s$	$\Delta t = 1\mu s$
LCSM	16.5695	16.5695	1.6571	1.6571	0.934	0.913
Energy balance LCSM	0.0016	0.0016	0.0081	0.0005	4.11×10^{-6}	3.61×10^{-8}
RSM	0	0	0	0	0.00086	0.00086

6.1.2 Two-Level Converter STATCOM

In this section an application test of the TLC is performed by simulating a more realistic application that of a TLC based Static Synchronous Compensator (STATCOM). The STATCOM is used to improve voltage profile of connected ac network as shown in Fig. 6-3. The STATCOM automatically adjusts the reactive current injection at the PCC bus to regulate the ac voltage. The system parameters are tabulated in Table 6.5.

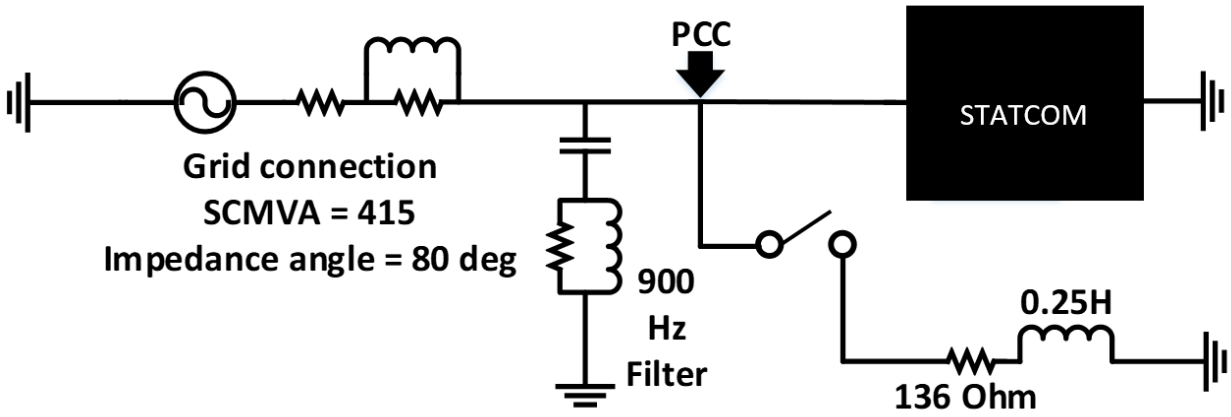


Figure 6-3 STATCOM network structure

Table 6-5 Statcom Network Parameters

Parameters and units	Value
AC source voltage (LL-RMS in kV)	115
Source Impedance (Ω-Ω || H)	5 - 10000 || 0.1
Network Frequency (Hz)	50
DC Bank (kV)	25
DC Capacitor (mF)	10
Load(Ω-H)	136 – 0.25
Simulation time step (μs)	50

Simulation is performed for 3sec. During the simulation, a 75MW RL load is connected to network at 1 sec and disconnected at 2 sec. The PCC voltage, real, and reactive power flow is shown below.

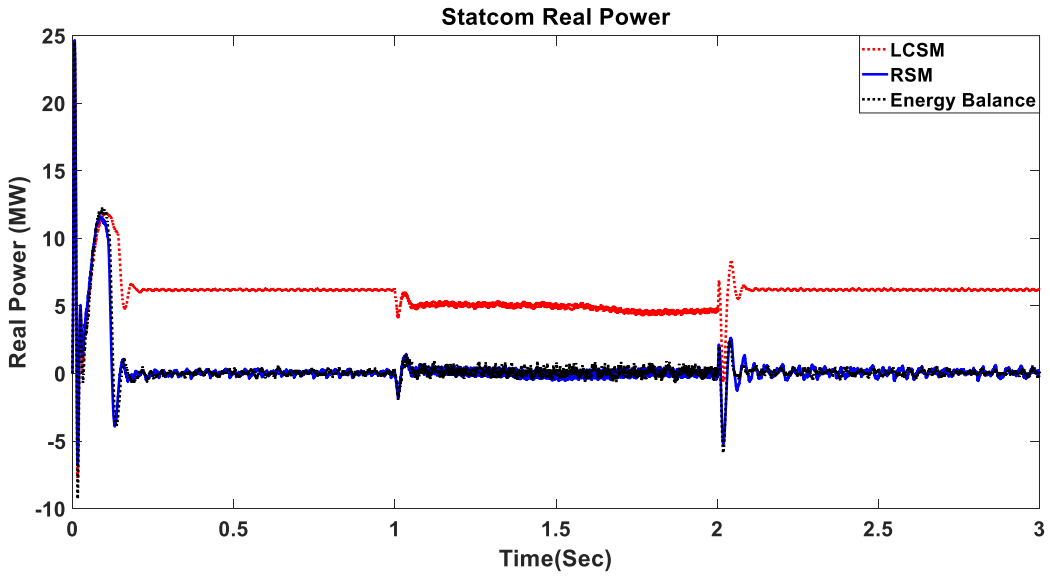


Figure 6-4 STATCOM real power vs time

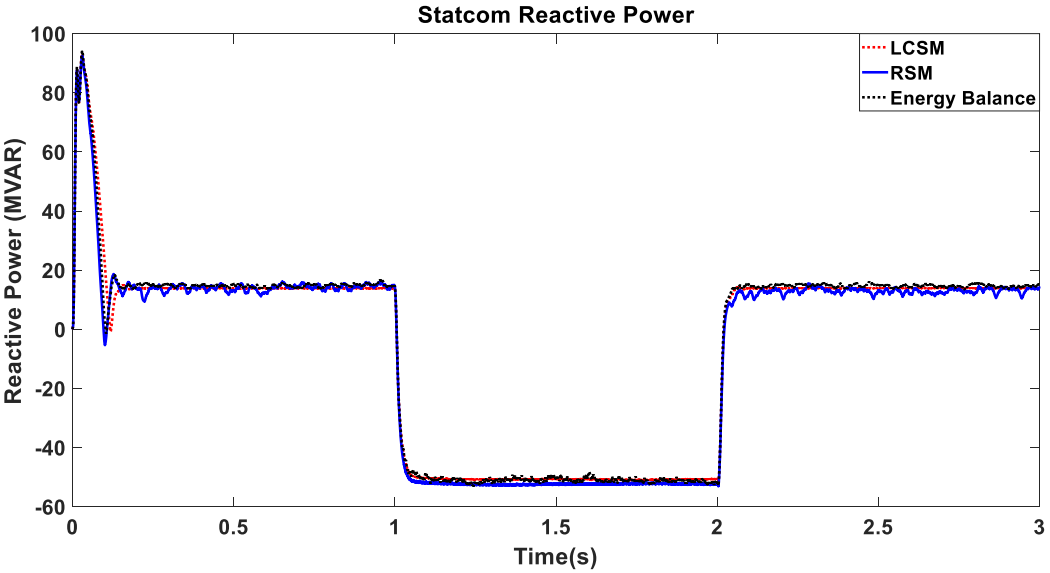


Figure 6-5 STATCOM reactive power vs time

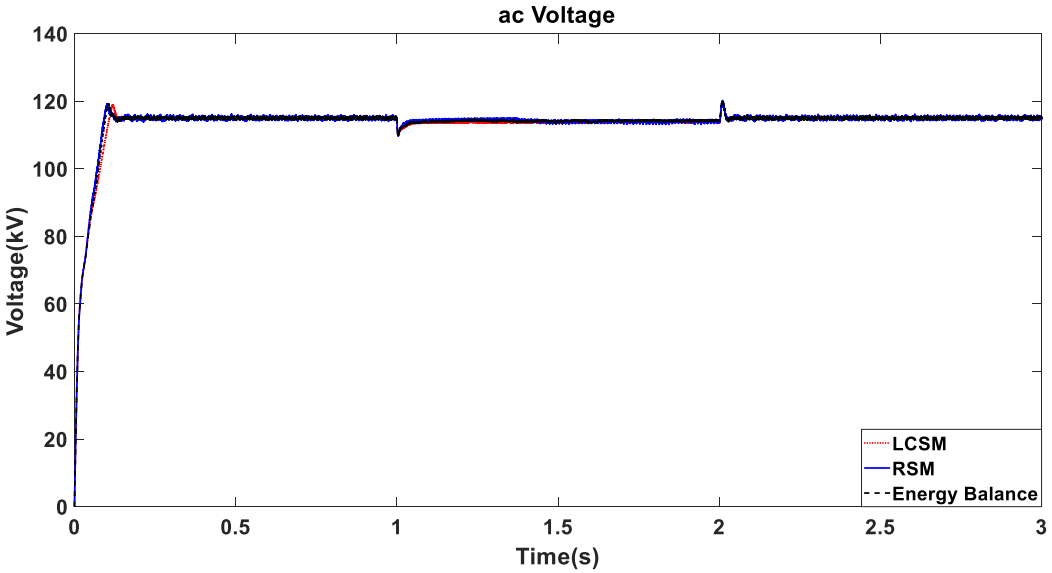


Figure 6-6 PCC RMS Voltage vs time

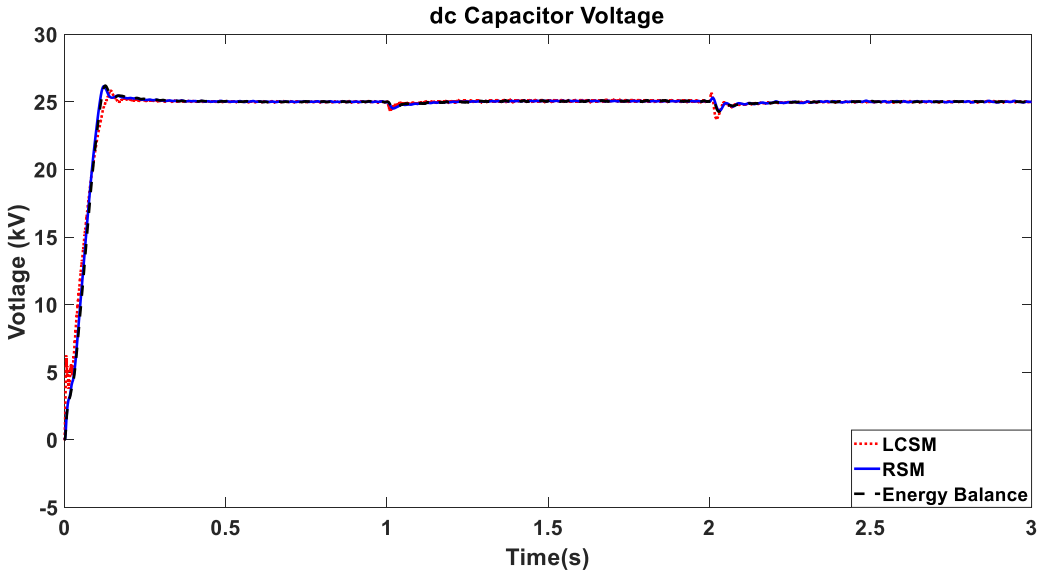


Figure 6-7 STATCOM capacitor voltage vs time

Fig. 6-4, 6-5, and 6-6 shows that PCC, and capacitor voltage is maintained through reactive power control for all 3 switch. However traditional LCSM's power loss is clearly reflected in the real power consumption of STATCOM as shown in Fig. 6-4. It is worth mentioning a traditional STATCOM's operation solely relies on reactive power control. However due to spurious switching loss of the traditional LCSM, the simulated STATCOM consumes a grossly erroneous amount of real power (between 5 and 8 MW!).

6.1.3 Modular Multi-level Converter HVdc link

The traditional LCSM excels at simulating large switching network due to elimination of matrix refactorization process during every switching event. As a result, the amount of computational savings is very significant when simulating the MMC, which has a very large number of switches. In order to demonstrate the effectiveness of LCSM, an eleven levels MMC based HVDC link is simulated. The network is shown in Fig. 6-8.

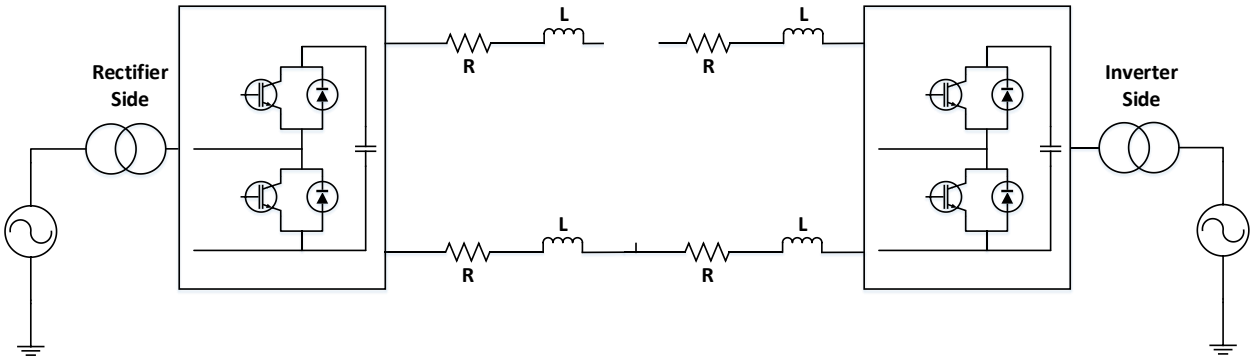


Figure 6-8 MMC HVDC link simulation case

The HVdc network is simulated for 8 sec using a $10\mu sec$ time steps. The SM capacitance is selected according to [40]. System parameters are tabulated in Table 6-6.

Table 6-6 Simulation Parameters

Parameters	Values
Rectifier side AC voltage $(LL-RMS-kV)$	10
Inverter side AC voltage $(LL-RMS-kV)$	9
Source Impedance $(\Omega - H)$	0.58236– 0.00692
Network Frequency (Hz)	50
Rated DC Voltage (kV)	10
Rated transmitted real power (MW)	3
SM Capacitance (F)	0.005
Arm Inductance (H)	0.004
Transmission line R(Ω)/L(H)	0.5/0.01
SMs / arm	10

The simulation results for the traditional LCSM, the proposed energy balance LCSM, and the benchmark RSM are plotted in Fig.6-9 to Fig.6-14. The plots includes: dc, ac side voltage, power transmitted, SM capacitor voltage, dc side current and average arm loss. As can be seen, the energy balance LCSM gives a good reproduction of the steady-state and startup transients.

The spurious oscillation across every traditional LCSM is cumulative due to the series structure of MMC phase legs. This cumulative effect is reflected on the dc terminal of the HVDC link. While energy balance LCSM can accurately track the benchmark RSM's dc voltage waveform, traditional LCSM's cumulative oscillation effect will produce large voltage ripples during operation as shown in Fig.6-9,13,14 which are the dc voltage, SM capacitor voltage, and ac voltage respectively.

Fig. 6-10 shows the significant improvement on spurious energy loss by measuring the average power across the phase A upper arm at the inverter side. In the benchmark RSM the energy loss is larger than in the energy balance LCSM. As explained earlier in section 6.1.1, this is as expected since the average power loss in the capacitors and inductors is zero, whereas there is a conduction loss in the RSM. Comparing to the RSM, the average arm loss using LCSM shows an acceptable higher loss of 0.105MW per inverter arm, or 0.63MW for the inverter.

Fig. 6-11 shows the power inverted by the MMC link is almost same for both LCSM and energy balance LCSM. However, this is due to the power controller of the inverter. In order to account for the spurious loss, the current in the link is higher by 22.2% as shown in Fig. 6-12, i.e., 396 A as opposed to 324 A.

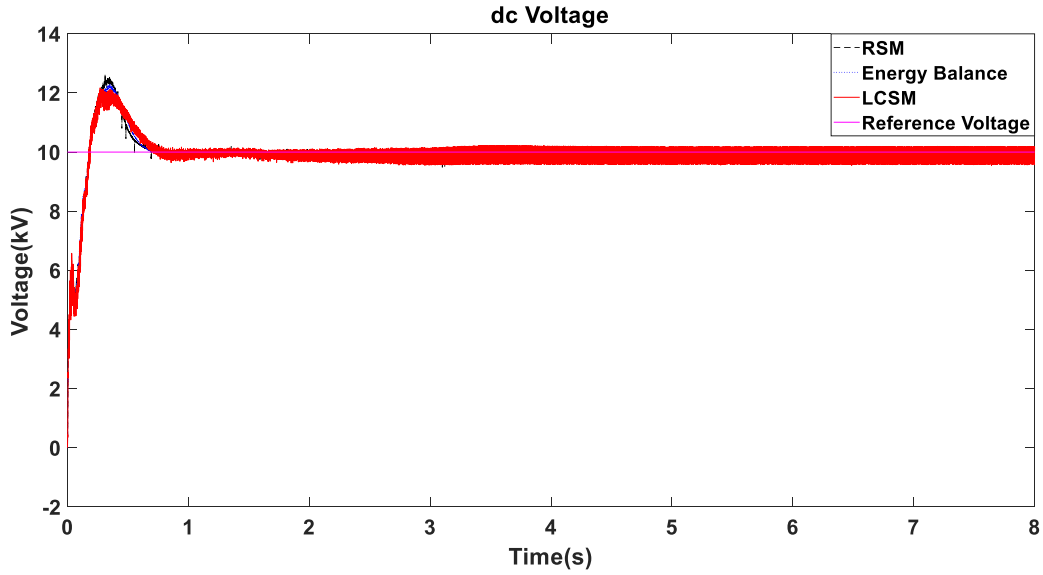


Figure 6-9 dc voltage vs time

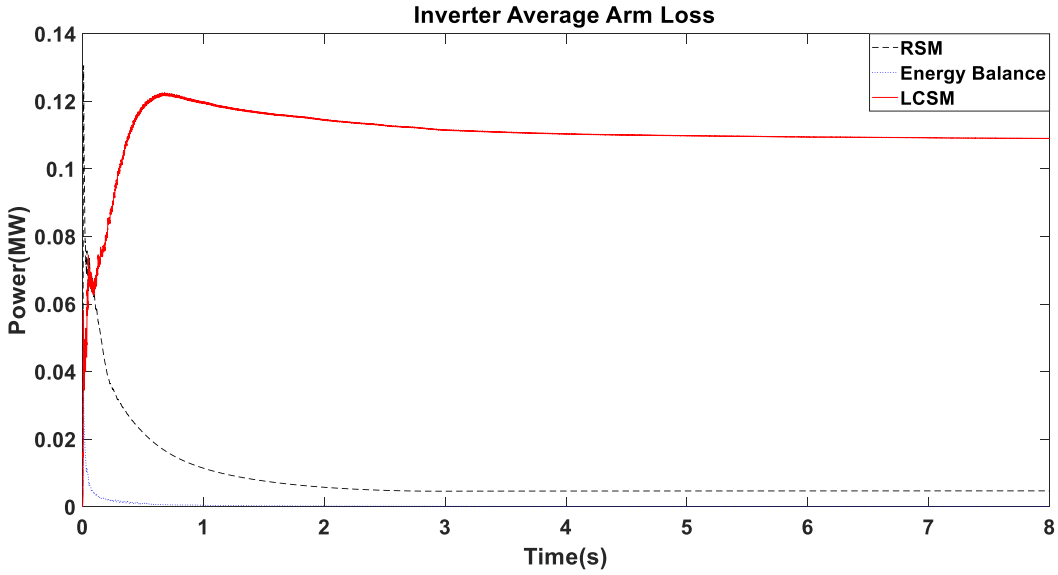


Figure 6-10 Average arm power loss vs time

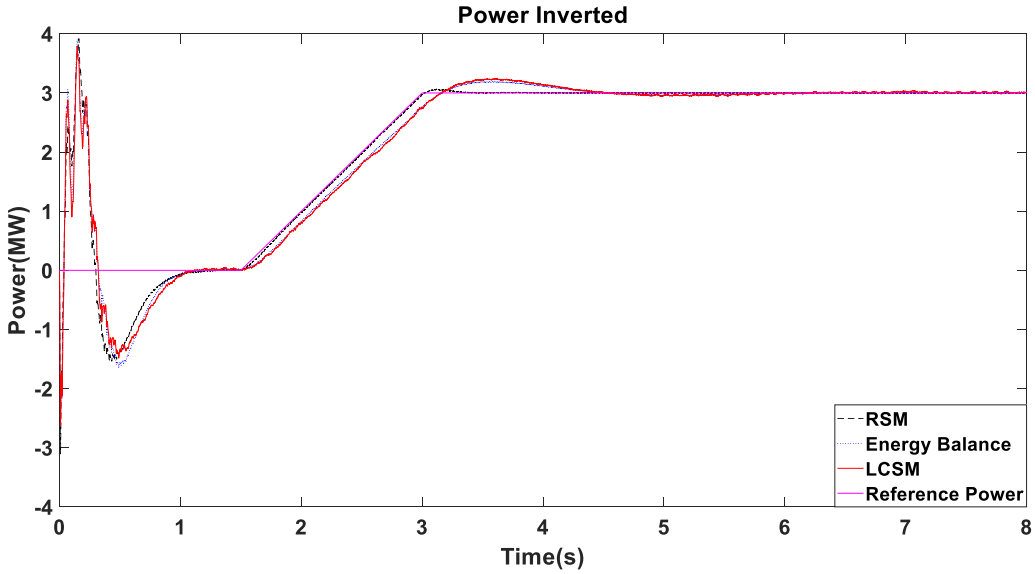


Figure 6-11 Power inverted vs time

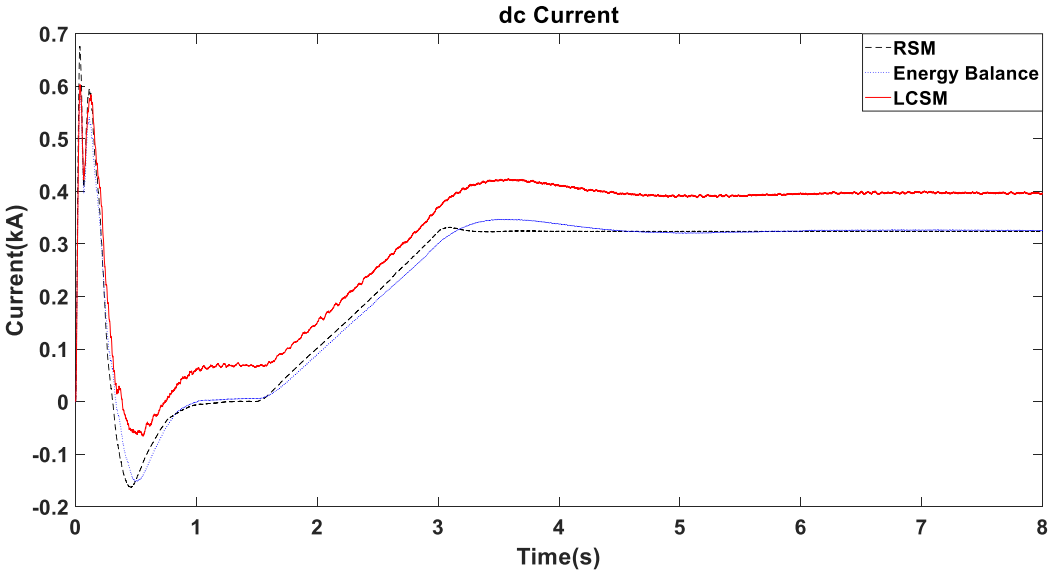


Figure 6-12 dc current vs time

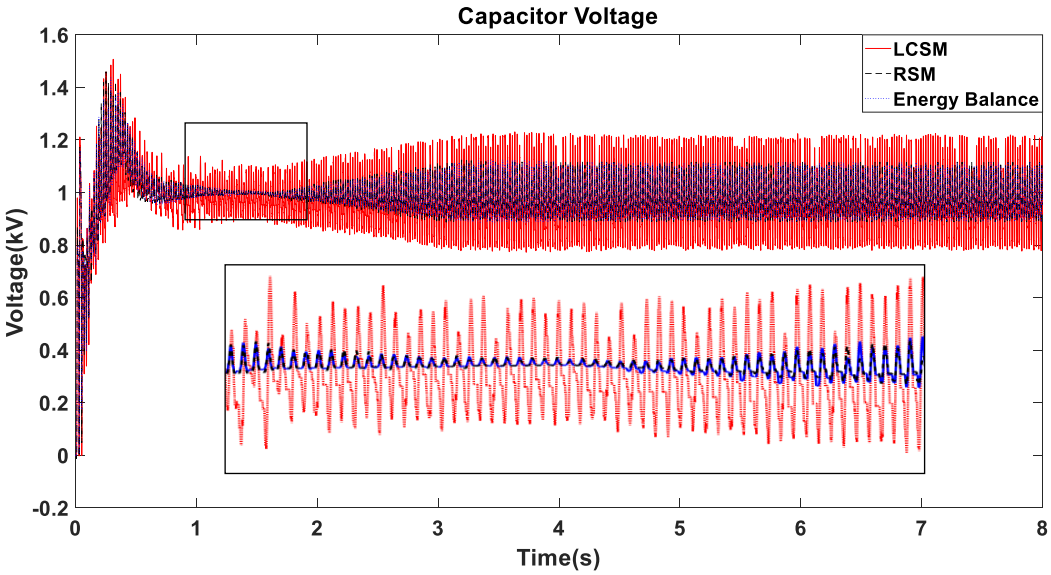


Figure 6-13 Capacitor voltage vs time

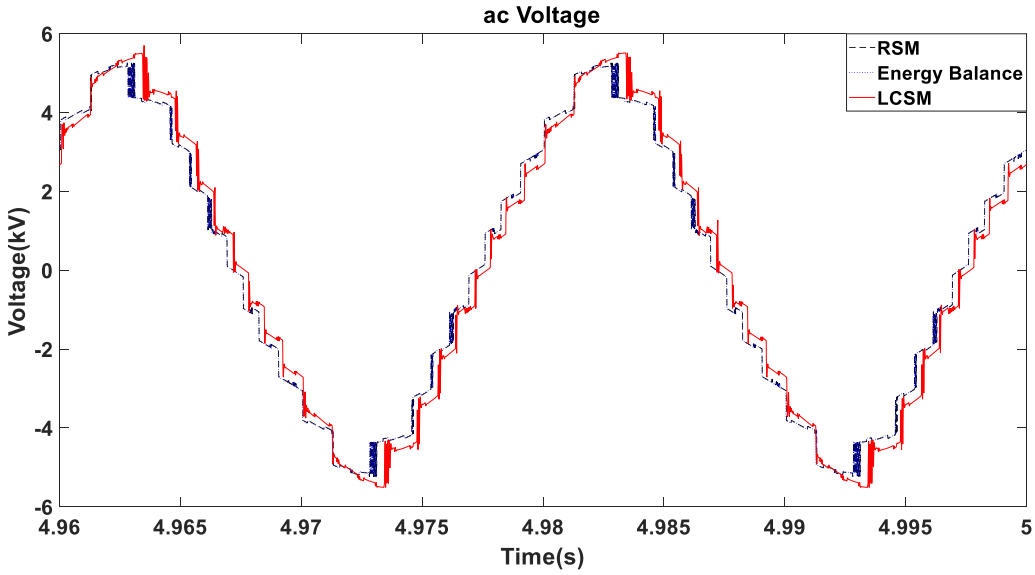


Figure 6-14 dc power vs time

It was shown simulation quality is significantly improved in MMC using the energy balanced LCSM as compared to the traditional LCSM. Another aspect besides the simulation quality is the simulation speed. The proposed model originated from traditional LCSM and thus has the benefit of avoiding admittance matrix re-factorization when the switch operates. This is reflected from the CPU time required for simulations when comparing to tradition RSM.

6.2 RC Switch Model Validation

Two VSC topologies are simulated for validation proposes. The first topology is a three phase diode bridge rectifier. The second simulation is more comprehensive, with a full set of controls. It is the same MMC HVdc link from previous subsection. Both topologies are validated with PSCAD's benchmark RSM model.

6.2.1 Three Phase Diode Bridge Rectifier

In this section a three Phase Diode Bridge Rectifier is constructed as shown in Fig.6-15. Simulation parameters are tabulated in Table 6-8. The bridge diode rectifier is constructed using the RSM diodes in PSCAD. On the other hand the RCSM version is implemented in Matlab. The implementation uses voltage dependent gate signal to achieve the same operational mode as PSCAD.

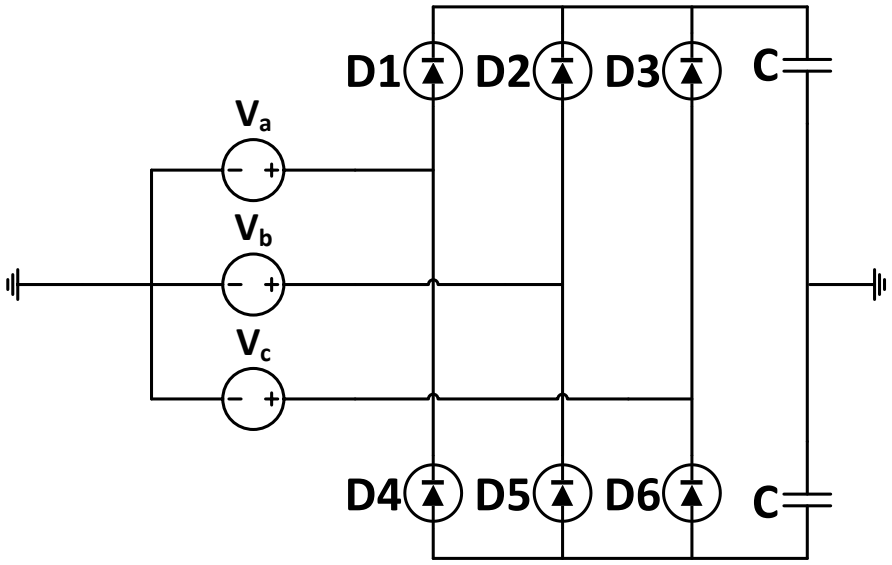


Figure 6-15 Three phase bridge rectifier configuration

Table 6-7 Diode Bridge Simulation Parameters

Parameters	Values
Simulation time step (μsec)	0.1
Switch admittance (S)	10
ac magnitude (Phase peak in kV)	1
ac frequency (Hz)	60
dc link capacitor capacitance (mf)	5
Simulation duration (Sec)	0.04
Subroutine simulation steps	2

One unique feature of the RCSM over the energy balance LCSM can be demonstrated in this topology. If one were to formulate the energy exchange table for the three phase bridge diode then a look up Table of size 6 by 6 is needed. However utilizing the predictive subroutine, the look up table is eliminated. As can be seen from Fig. 6-16 to 6-18, which show the plots of the dc capacitor voltage, D1 voltage, and current. The RCSM is able to reproduce essentially the same transient and steady-state waveform as RSM.

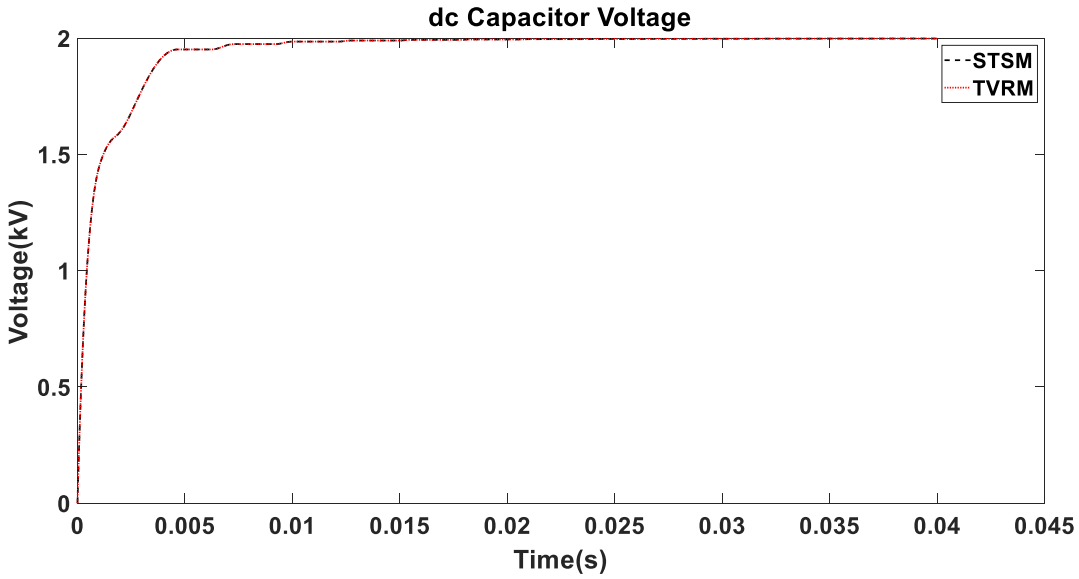


Figure 6-16 dc capacitor voltage vs time

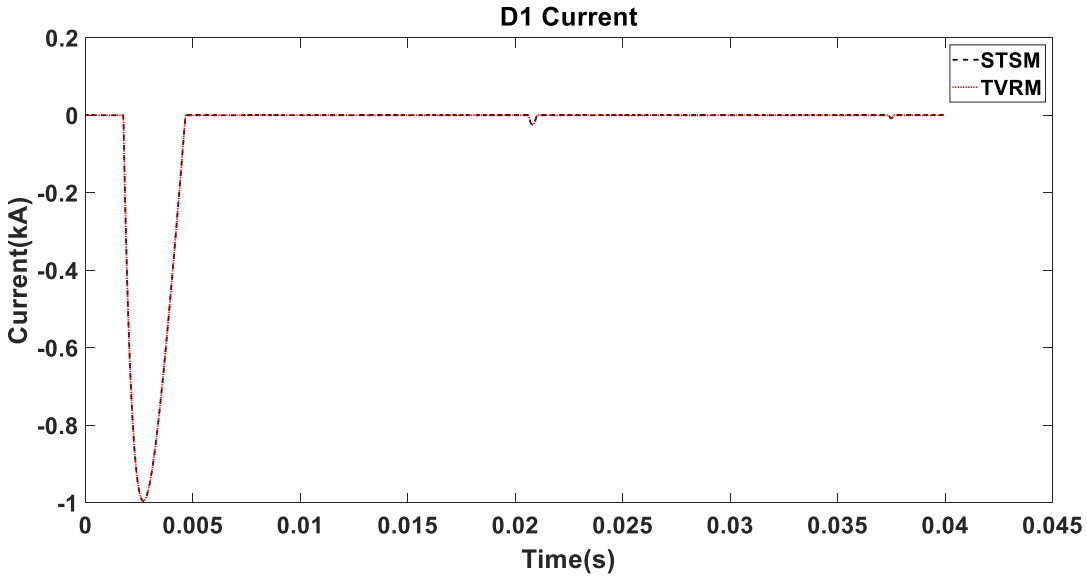


Figure 6-17 D1 current vs time

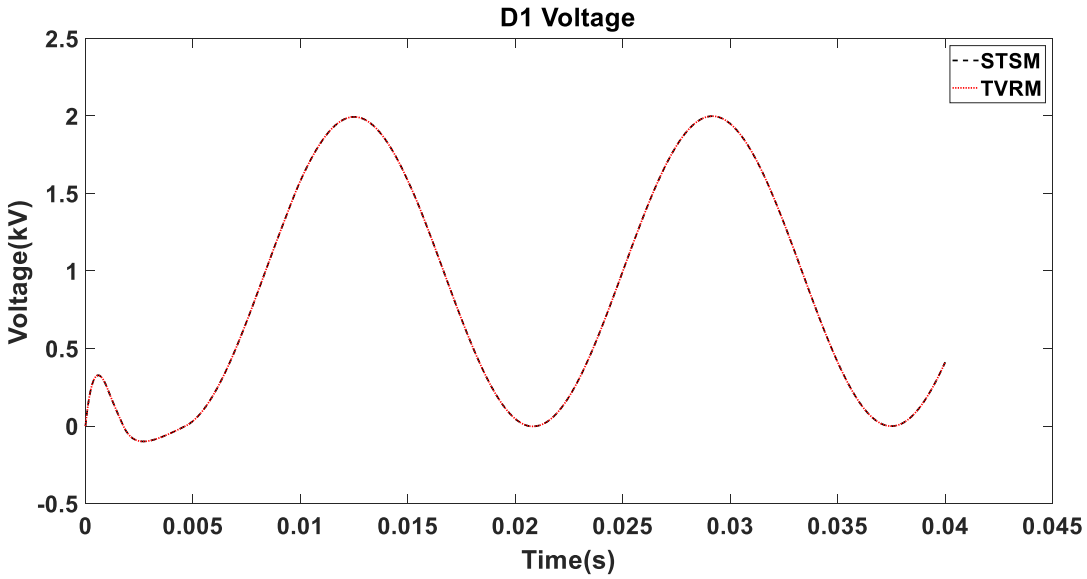


Figure 6-18 D1 voltage vs time

6.2.2 Modular Multi-level Converter HVdc link

The RCSM is also effective at simulating a large switching network due to elimination of matrix refactorization process during every switching event. As described in section 5.2.2 a new subroutine is used to predict a suitable post switching history term for the switches in PSCAD by representing the SM capacitor as a dc voltage source and arm current as dc current source.

Simulation quality is verified using the same MMC HVdc link configuration as section 6.1.3. The simulation comparisons of DC voltage, average arm loss, power transmitted, dc current, SM capacitor voltage, and ac voltage are shown in Fig. 6-19 to Fig. 6-24.

For the most part, the RCSM will produce similar waveform comparing to RSM. This can be seen from the voltage waveforms in Fig. 6-19, 23, 24. Due to controller command variation (ie. Instantaneous gating signals given to each individual switch) a slight variation in power inverted is observed in Fig. 6-21. The difference in power also changes the dc current proportionally in Fig. 6-22. The average loss of RCSM is almost the same as RSM and this is expected as they share the same conduction loss during the on-state, and both models has almost negligible switching and off-state conduction loss.

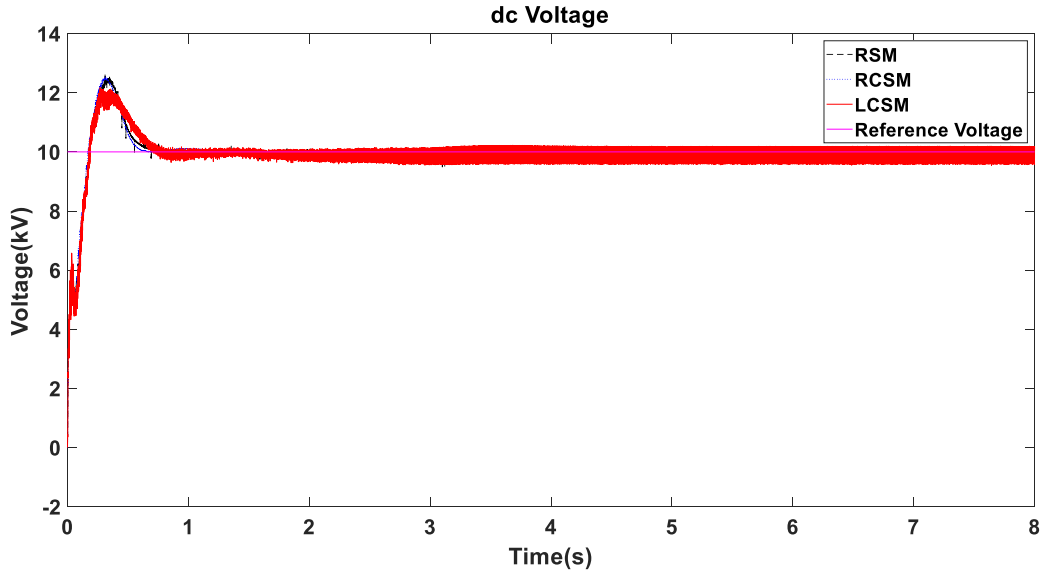


Figure 6-19 dc voltage vs time

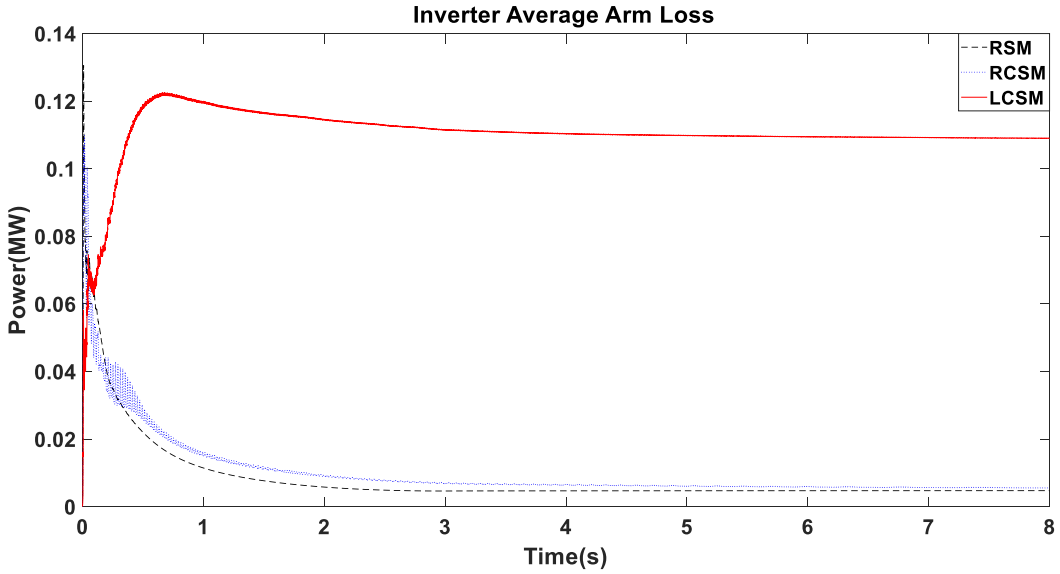


Figure 6-20 Average arm power loss vs time

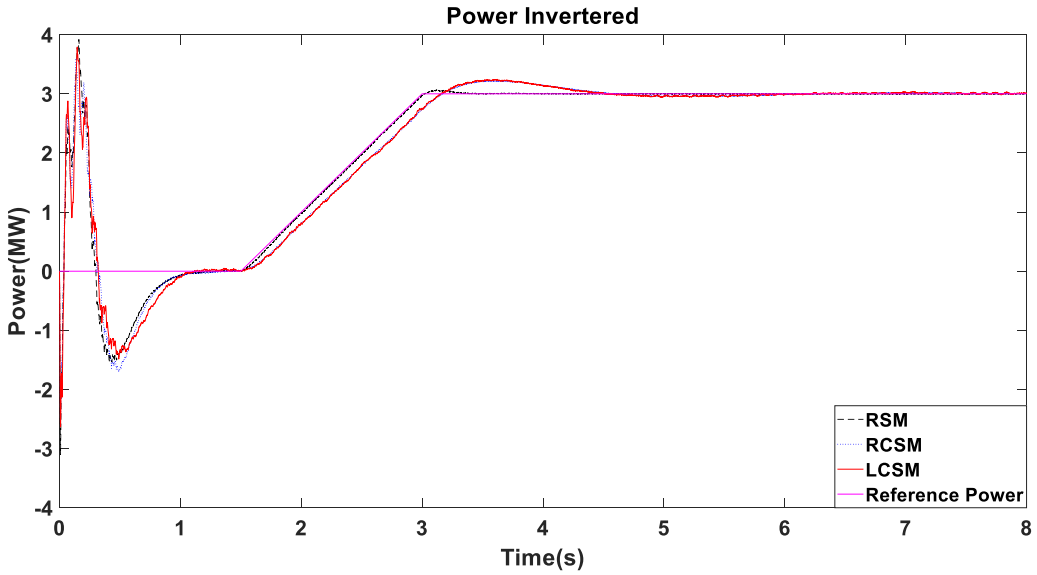


Figure 6-21 Power inverted vs time

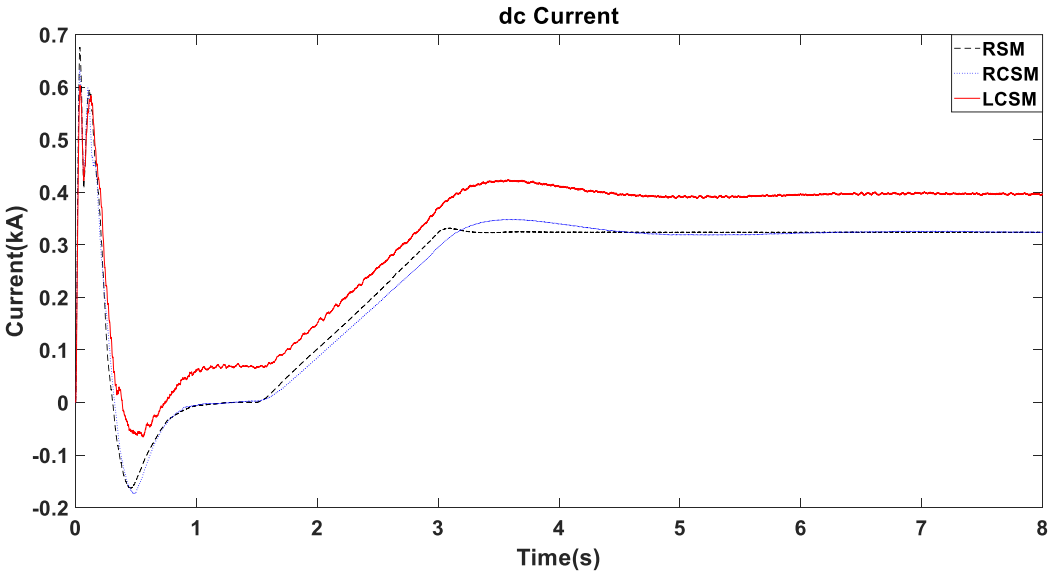


Figure 6-22 dc current vs time

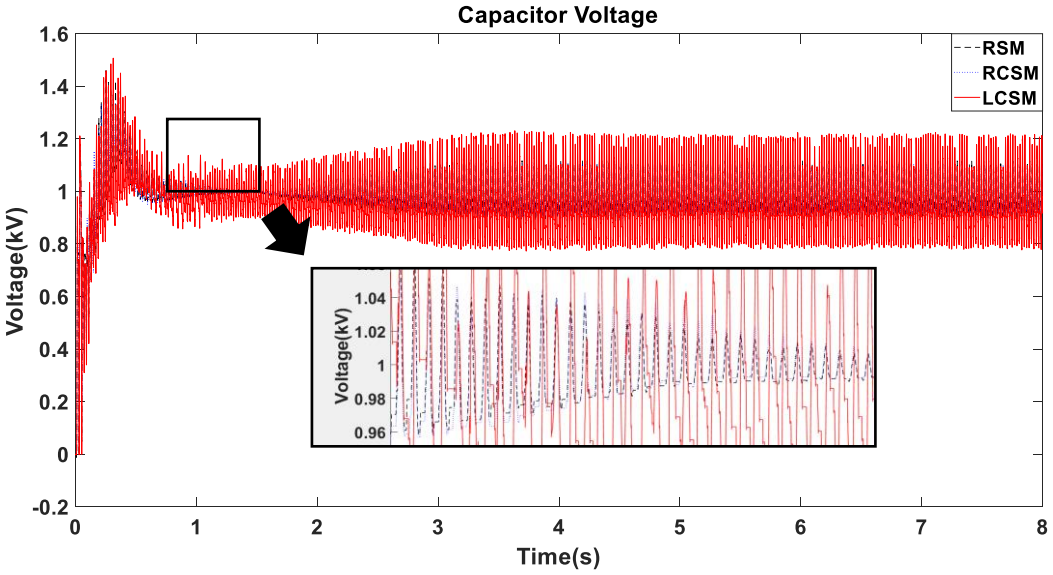


Figure 6-23 SM capacitor voltage vs time

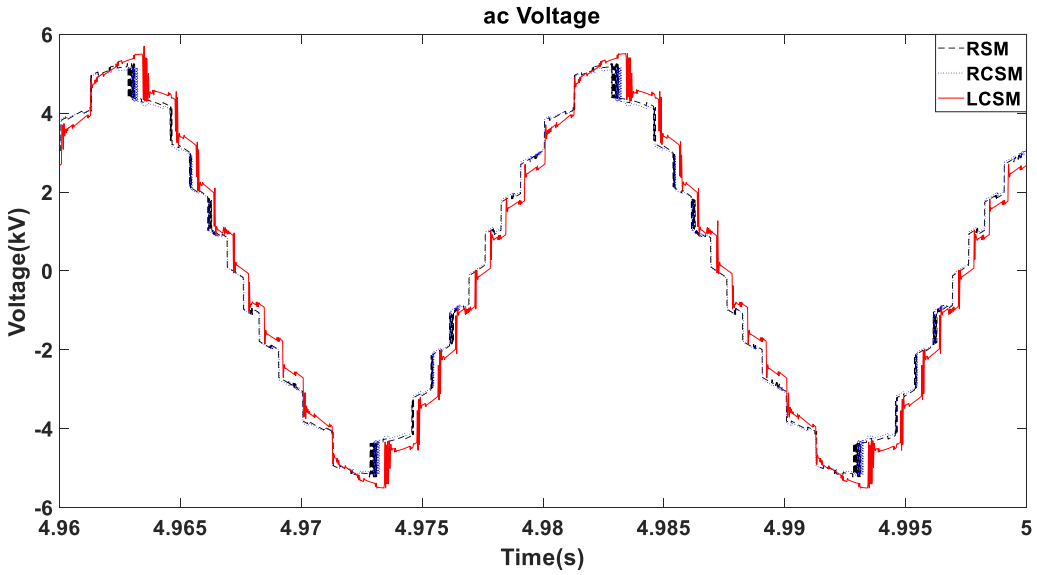


Figure 6-24 ac Voltage vs time

6.3 Simulation Speed Up Validation

It was said in the beginning of this thesis that simulation speed up was an important characteristics for LCSM and in this the proposed solutions has tried to retain this characteristics by enforcing the on-state and off-state admittance for both Energy balance LCSM and RCSM to be equal. This will effectively eliminate the need for matrix refactorization during switching. In order to validate this assumption additional SMs are added to the MMC HVdc link shown in 6.1.3 and 6.2.2 and the simulation speed up (in %) is shown below in Fig. 6-25. As expected, the speedup using RCSM as well as the LCSM (with energy balance) is considerable as compared to the traditional resistor switched model (RSM), approaching 40 times (4000%) for 40 submodules per arm. Also, these two proposed new approaches within improved accuracy and damping, have essentially the same speed as the traditional LCSM. The corresponding actual simulation times are plotted in Fig. 6-26.

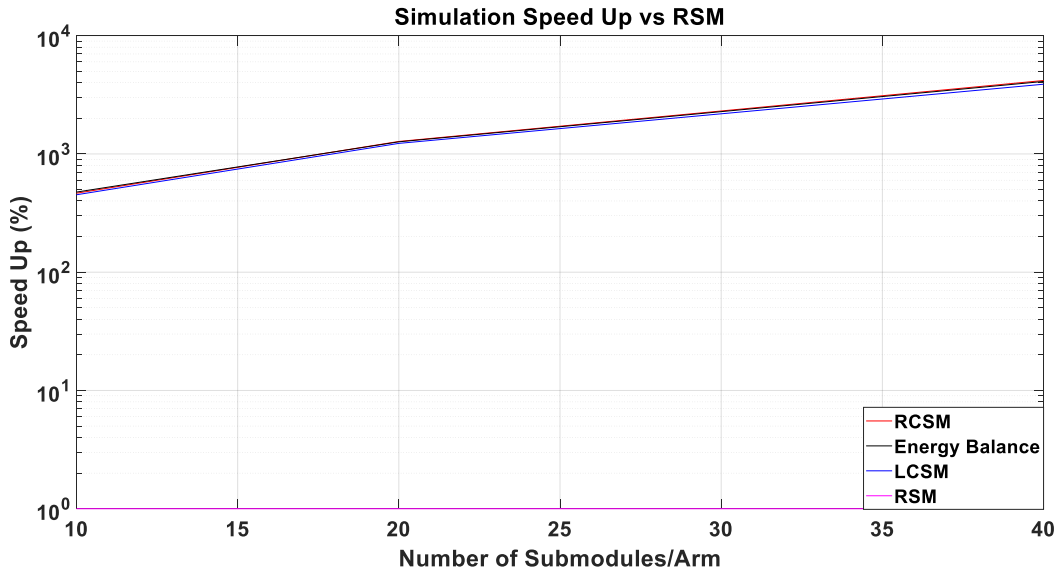


Figure 6 - 25 Switch Models Speed Up in % vs SM/Arm

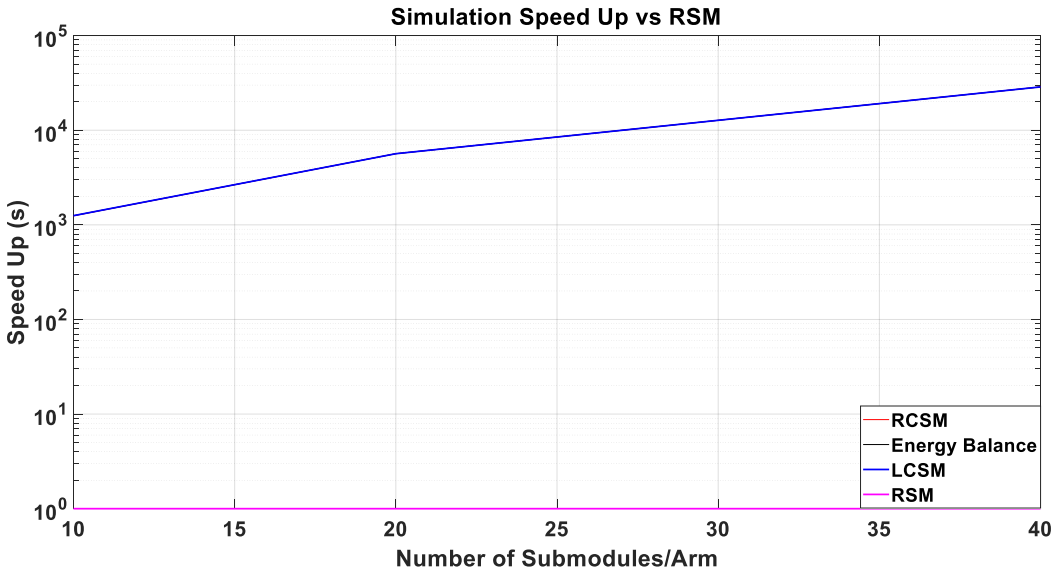


Figure 6 - 26 Switch Models Speed Up in Seconds vs SM/Arm

7 Conclusion and Future Work

The LC Switch Model (LCSM) is a fast switch model designed to simulate switch networks without the need of matrix refactorization during every switching event. However until now this model has shown spurious switching loss and underdamped transient response. The energy balance method and the RC/RL Switch Model (RC/RL SM) is proposed in this thesis to suppress the spurious switching transient while retaining the fast computational speed. The proposed method and model is further implemented on the popular EMT simulation platform PSCAD for validation. The simulation result showed negligible amount of switching oscillation and loss for energy balance LCSM. On the other hand RCSM was able to reproduce a similar amount of switching loss as Resistor Switch Model (RSM) while eliminating the switching oscillation.

7.1 Contribution of this Thesis

The main contribution of this thesis is as follows:

- Based on switch energy an "energy balance" algorithm is formulated to suppress the spurious switching transient of the traditional LCSM. This method calculates the post switching switch voltage and current such that the post switching switch energy equals to the pre switching switch energy in a complementary pair of switch.

- This thesis has also shown that optimization methods can be applied to select a more appropriate post switching switch voltage and current value however direct energy enforcement will produce results almost as good.

- A complete new switch model RC/RL SM is proposed where the on-state switch is modeled as a small resistor 'R_{on}' or small inductor 'L_{on}', and the off-state is modeled as a large resistor 'R_{off}' or small capacitor 'C_{off}' respectively. The RC/RL SM is mathematically proven to have a short switching transient due to the discrete eigenvalue having a magnitude of zero.

- Serval VSC topologies has been simulated using RSM, Traditional LCSM, energy balance LCSM, and RCSM. Both the energy balance LCSM and RCSM was able to show a good match of steady state and transient characteristics when comparing to the benchmark RSM. A speed up comparison is made simulating a 11 levels MMC HVdc link and LCSM has shown a speed up of 475.68%, energy balance LCSM has shown a speed up of 451.52%, and RCSM has shown a speed up of 465.52%. Simulation quality was improved using the proposed method and switch model while the fast simulation speed is retained.

7.2 Future Work

Some future works one may consider are listed below:

- Inclusion of diode model and blocking operation of converter.
- Using a dedicated hardware to implement proposed method and model such as FPGA. This way all computational process can be controlled and a much more accurate simulation time can be obtained without the overhead of OS.

- Implementation of other converter topologies using proposed model

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