DESIGN AND AN ANALYSIS OF THE STACKED MULTICELL CONVERTER WITH COMPARISON TO THE NEUTRAL POINT CLAMPED CONVERTER

By

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A Thesis
Submitted to the Faculty of Graduate Studies
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A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirement of the degree

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The author Want to express her respect and

appreciate to her beloved parents

Her father, Wang Renyu

Her mother, Peng Suhu

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Abstract

This study is the comparison of the design and analysis of the Stacked Multicell Converter (SMC) with the Neutral Point Clamped (NPC) converter. Multilevel converters are becoming increasingly popular for high power applications, because they can considerably reduce the output voltage and current harmonics by using several voltage levels while still switching the devices at the same frequency. The diode clamped converter (DCC) and the SMC converter are two types of multilevel converters which both use one DC bus subdivided into a number of voltage levels by a series string of capacitors. This kind of structure can reduce the blocking voltage requirement of each switching device. The three-level DCC converter, which is also called the NPC converter, has been put into practical use for large capacity ac motor drives in industry. Due to the voltage limitations of the switching devices, series connection of the devices is required in high-voltage and high-power applications with the NPC structure. Higher level DCC can solve this problem, but another problem of voltage unbalance between the outer dc capacitors and inner dc capacitors occurs. Although methods have been proposed to balance the capacitor voltage, they have not been put into practice by the industry.

In this thesis we present a new topology called the SMC which allows increasing input voltage level, while not increasing the switching device stresses by the use of floating capacitors. This thesis gives the design of the SMC including a method of pre-charging the floating capacitors, selection of the floating capacitors, and analysis of the commutation requirements. Both the converters are simulated using EMTDC and PWM techniques and compared in theory and experiment.

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CHAPTER 1

INTRODUCTION

1.1 Background

Power converters make use of a configuration of power semiconductor devices that function as switches. They have shown rapid development in recent years, primarily because of the development of semiconductor power devices that can switch larger currents at higher voltages, and so can be used for the conversion and control of electrical energy at higher power levels. The electrical energy is converted to make it suitable for various applications such as regulated power supplies, active power filters, heating and lighting control [1], dc and ac motor drive application, welding control, static VAR compensation and HVDC transmission.

During the past few decades of power electronic device and circuit development a number of concepts have been examined. Low blocking voltage (50V-500V) and medium voltage (500V-1800V) applications have found a number of satisfactory candidates, but at high voltage (2500V-9000V) compromises still seem to dominate and development work is necessary. Gate Turn Off Thyristors (GTO), Integrated Gate Commutated Thyristors (IGCT) and Insulated Gate Bipolar Transistors (IGBT) are the high power semiconductors currently available on the market which can be turned off actively. A short background review of the field's history may help to understand the root of this thesis work [2].

Introduced in the late 1950's, thyristors have been the only choice for power electronic applications requiring ≥2.5kV blocking for more than 20 years. With these elements only the moment of turn-on could be influenced by the gate drive, while turn-off had to be initiated by a reversal of the device current. As a consequence, realization of circuits transferring energy from AC sources to AC or DC loads was much easier at that time than realization of circuits with DC sources or DC voltage links.

The GTO thyristor, adding forced gate commutation to control the turn-off, was invented in 1960, but it was not developed for high power applications until the late 70's. At that time, the voltage source converter (VSI) topology entered the field, leading to a drastic increase in performance of important application areas like traction converters and industrial drives.

At the same time a number of innovations and changes were observed close to the GTO's domain at blocking voltages below 2000V. Before the GTOs really could establish themselves in that area, bipolar transistors entered, and were soon followed by the IGBT. Although the IGBTs suffered from a loss of control by undesired latching for many years, device development was continued to finally overcome that constraint. Then, the IGBT began its success in improving

current and voltage handling capability and switching performance step by step. But the IGBTs are still limited to medium power applications.

The quest in last ten years for high-power snubberless semiconductor switches to replace the conventional GTO has led to the IGCT technology. Currently the IGCT is the optimum combination of the proven, low-cost thyristor technology and the snubberless, cost-effective gate turn-off capability for demanding medium and high-voltage power electronic application [3]. The introduction of the IGCTs has substantially advanced the development of high power hard switching Pulse Width Modulation (PWM) Voltage Source Converters for industrial and traction applications. The switching frequencies are typically limited to about 500 to 1000Hz by the switching losses with snubberless operation.

The development of power semiconductor technology indicates a tradeoff in the selection of power devices in terms of switching frequency and voltage-sustaining capability [4]. Normally, the voltage-blocking capability of faster devices such as the IGBT, and the switching speed of high-voltage IGCT, are found limited.

1.2 Purpose

With respect to the design of the voltage source converter topology, the conventional two-level converter can not satisfy the market requirements of harmonic distortion and dynamic control. This leads to increasing interest in the multilevel power converter. These converters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better spectrum and attain higher voltages with a limited maximum device rating. To date the industry appears to have settled on the three-level NPC converter as the best compromise.

There are many possible circuit configurations for realizing a practical multilevel converter. This thesis will compare a five-level Stacked Multicell Converter (SMC) against a benchmark three-

level Neutral Point Clamped Converter (NPC) of similar ratings that are connected between an ac system and a dc load. The focal point of the investigation will be the number of switches, the device stresses, the harmonic performance of the output voltages and currents in the two types of converter. Along with this, the switching method and the capacitor performance are to be analyzed. The control system will be designed to regulate the dc voltage, as well as the reactive power production or absorption. The main tool used in this investigation is the electromagnetic transient simulation program called PSCAD/EMTDC^{TM} .

1.3 Thesis Outline

Chapter 2 of this thesis gives a general introduction to the voltage source inverter. The operating principle and the four-quadrant operating characteristic of the VSI is explained. The general control idea is introduced based on the basic two-level VSI, which can be also applied to the multilevel converters. Two types of pulse width modulation (PWM) are compared based on the basic VSI and carrier-based PWM is chosen as the switching method in later chapters.

In Chapter 3, a general introduction to multilevel converters is given. The detail configurations of the three-level NPC and the five-level 2x2 SMC are presented and extended to higher level. The advantages and constraints for both converter circuits are analyzed. The switching methods for the NPC and SMC converter are presented respectively and analyzed using MATHCAD software.

Chapter 4 describes the common specification for the three-level NPC and five-level SMC from the aspects of DC side capacitor, number of switches and device stresses. The output voltage spectrum of the two different structures are analyzed and compared. The advantages and disadvantages of each design are discussed.

Chapter 5 explains the performance of capacitors in the converters. First a basic theory about the capacitors is given. Then the voltage unbalance existing in the capacitors is analyzed and the design principle of voltage balance control is developed. Finally the principle to choose the size of the capacitors is presented.

Chapter 6 develops a mathematical model for the control system and pre-charging method for the converter. Simulation study for the control system are carried out using EMTDC which include test of start-up of the SMC, the voltage balance control for capacitors, steady state operation and transient operation.

Chapter 7 gives detailed simulation results for the three-level NPC and five-level SMC using EMTDC. The output voltage and current waveforms are presented and the harmonics are analyzed using LIVEWIRE software for both types of converter. The simulation results for the NPC and the SMC are compared with respect to the voltage level, harmonics in the supply voltage and current, and device voltage and current stresses.

CHAPTER 2

BASIC ANALYSIS OF THE VOLTAGE SOURCE INVERTER

Voltage source inverters (VSI) are commonly used to transfer real power from a dc source voltage to an ac load such as an ac motor [5]. The output current waveforms of the inverter must be as close as possible to a sinusoidal wave and therefore reducing the current harmonics is a major concern. The output voltage can be controlled by either the fundamental frequency switching (FFS) or PWM switching techniques, which controls the output voltage by altering the switching pattern with a constant dc voltage, or by varying the dc voltage with a fixed switching pattern. In this thesis, the focus is on the case with a constant dc capacitor voltage. This means the real component of the current flowing into the converter must be controlled. This is

accomplished by controlling the magnitude and phase of the converter ac voltage as will be discussed later.

The FFS technique has a limited switching pattern and hence a high harmonic content over much of the operating ranges. PWM techniques are simple to apply and are able to control harmonics over a wider operating range. Therefore, this thesis will restrict the switching methods to PWM techniques in this thesis.

2.1 Basic Operation for the VSI

The operating principle of the VSI can be best explained with the aid of the simplified model of the three-phase circuit shown in Figure 2.1a, which consists of a basic two-level VSI. Figure 2.1b shows the per-phase fundamental equivalent circuit of the system. An equivalent voltage source $\vec{V}_o$, which is the fundamental component of the converter output voltage, is connected to the ac main system through a reactor. The inductance L represents any series inductance between the inverter ac voltage and the ac system voltage and the resistance R represents any resistance associated with the converter and the supply as a lumped value as shown in figure 2.1b. Usually, R is small so that we can ignore it. From this simplified model, the output current $\vec{I}_o$ can be expressed as follow:

$$\vec{I}_o = \frac{\vec{V}_s - \vec{V}_o}{j\omega L} \tag{2.1}$$

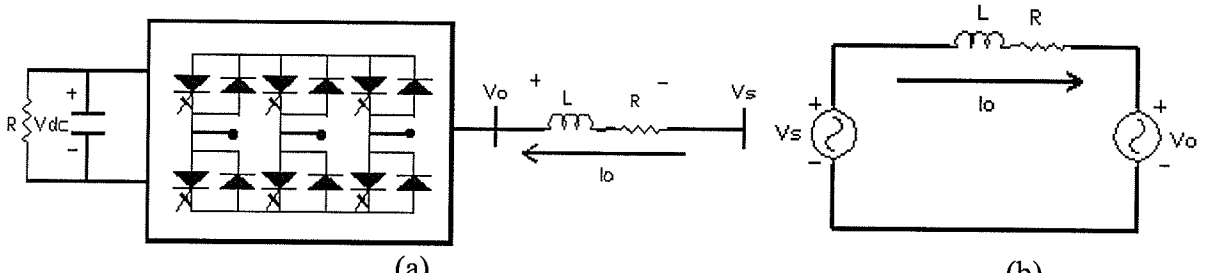

Figure 2.1 Circuit Diagram and Simplified Model of a Three-Phase Converter

The ac system voltage is assumed as the reference with a zero phase angle. It can easily be seen from Equation 2.1 that the magnitude and direction of the output current $\vec{I}_o$ can be regulated by the amplitude and phase angle of the variable converter output voltage $\vec{V}_o$. In general, we assume the converter output voltage $\vec{V}_o$ with a magnitude V_o and phase shift angle α with respect to V_s. Then the reactive component of the output current can be given as:

$$I_{oq} = \frac{-V_s + V_o \cdot \cos\alpha}{\omega L} \tag{2.2}$$

thus the corresponding reactive power is:

$$Q = \frac{-V_s^{\,2} + V_o \cdot V_s \cdot \cos\alpha}{\omega L}$$

Similarly, the active component of the output current can be given as:

$$I_{od} = \frac{-V_o \cdot \sin\alpha}{\omega L} \tag{2.3}$$

The corresponding active power is:

$$P = \frac{-V_o \cdot V_s \cdot \sin\alpha}{\omega L}$$

From Equation (2.2) and (2.3), we can easily see that both reactive and active current can be positive or negative. When $V_o \cdot \cos\alpha$ is larger than V_s, I_{oq} is positive. This means $-90^\circ < \alpha < 90^\circ$. In this operating region, I_{od} is positive for $-90^\circ < \alpha < 0^\circ$ and negative for $0^\circ < \alpha < 90^\circ$. When $V_o \cdot \cos\alpha$ is smaller than V_s, I_{oq} is negative. In this operating region, α can be any value between 0° and 360° and therefore I_{od} can also be positive or negative. Generally speaking, the VSI can operate in all the four quadrants. The phasor diagram of the VSI is shown in Figure 2.2.

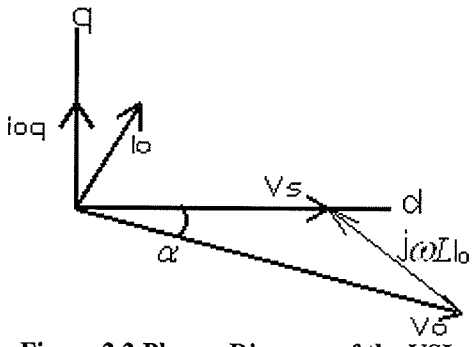

Figure 2.2 Phasor Diagram of the VSI

2.2 Basic Control for the VSI

The converter shown in Figure 2.1a is inherently two converters connected in inverse parallel and can be redrawn as Figure 2.3. Converter 1 acts as an uncontrolled rectifier to allow the real power flowing from the ac side to the dc side. Converter 2 operates in the converter mode, where the polarity of the voltage across the dc capacitor V_{dc} remains the same but the direction of the dc side current I_d is reversed. Initially, when converter 2 is not conducting, capacitor charges up to the peak value of the supply voltage through converter1. This characteristic of the VSI provides the possibility to pre-charge the dc capacitors directly through the ac system. Providing no real power transfer occurring between the circuit and the supply, the capacitor voltage remains at its initial charged voltage and acts as a constant dc source.

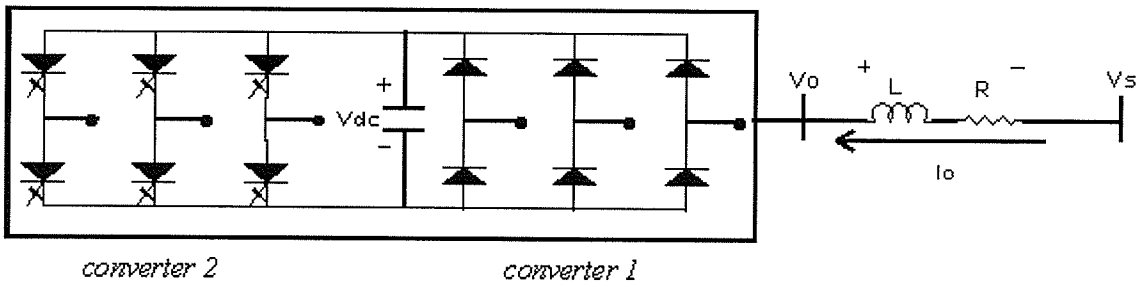

Figure 2.3 Two Converter Configuration Redrawn from Figure 2.1a

The control strategy adopted in this investigation is based on the PWM switching technique. As described in Section 2.1, both reactive power and active power should be controlled and the dc capacitor voltage should remain constant. Then, there are two main tasks that the control scheme

has to achieve. One is to control the converter input power factor or the reactive component of the current, and the other is to control the real power flowing into the dc load to maintain a constant voltage across the dc capacitors. Figure 2.4 shows the basic control diagram that was designed to perform the above tasks.

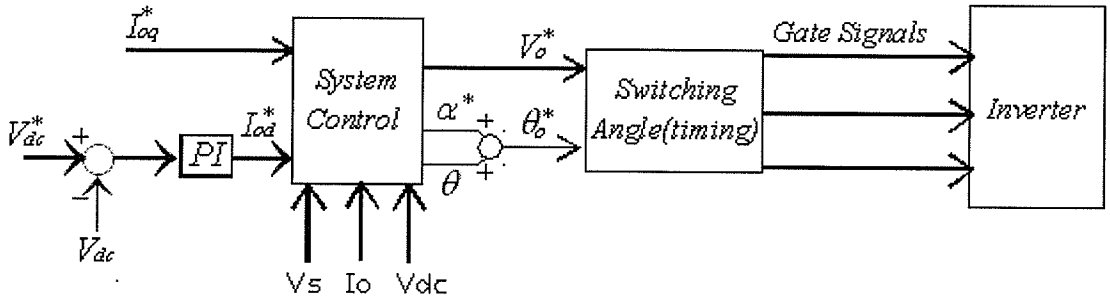

Figure 2.4 The Basic Control Diagram for VSI

Where V_{dc}^* is the reference dc voltage and V_{dc} is the measured voltage, I_{od}^* and I_{oq}^* are the reference active and reactive current respectively, V_o^* and α^* is the magnitude and phase angle of the reference output voltage respectively. θ comes from a phase locked loop (PLL) locked to the system frequency which is used to obtain the phase angle, α, the angle difference between converter output and ac system voltage.

Given a certain reactive and active current, from Equation 2.2 and 2.3, the magnitude and phase angle of the reference output voltage could be expressed as:

$$V_o^* = \sqrt{(I_{oq}^* \cdot \omega L + V_s)^2 + (I_{od}^* \cdot \omega L)^2} \tag{2.4}$$

$$\alpha^* = -\arctan\left(\frac{I_{od}^* \cdot \omega L}{I_{oq}^* \cdot \omega L + V_s}\right) \tag{2.5}$$

The control loop to maintain the constant capacitor voltage is implemented by comparing the actual dc voltage and the reference dc voltage. The error of the two signals passes through a PI controller and thus obtains the required real power to the dc capacitor. This real power divided

by the constant supply voltage provides the reference real component of the supply current. The reactive current component I_{oq}^{*} does not affect the dc voltage but does affect the power factor of the VSI as seen from the ac system. This component is normally set to zero, but may vary if some form of power factor control is required. These two reference currents are compared to the measured real and reactive current components of the input current, and the magnitude and phase of the converter voltage is adjusted according to Equations 2.4 and 2.5. This reference output voltage can then be used to calculate the switching signals of the converter by using PWM techniques. With above control, both the magnitude and phase angle of the output voltage can be continuously controlled to maintain a constant dc voltage and constant reactive current component. The detail mathematical model for the system control block will be presented in Chapter 6.

2.3 PWM Switching Techniques for the VSI

The PWM switching technique is the most common method to control output voltages of a voltage source converter due to its simplicity and ability to reduce the harmonic content. These techniques can be classified into two types: carrier-based PWM methods and optimal PWM methods. The carrier-based PWM methods include subharmonic PWM (SHPWM) and switching frequency optimization PWM (SFOPWM) [6]. These techniques have also been extended to various multilevel VSI topologies.

2.3.1 Carrier Based PWM Technique

In carrier based PWM techniques, the switches are operated many times in the fundamental ac cycle producing a pulsed waveform with reduced harmonic content. The switching instants are defined by the crossings of a carrier triangular wave and the sinusoidal reference signal.

The SHPWM method uses a set of triangular carriers to compare with the reference sinusoidal wave. The SFOPWM method is similar to the SHPWM method, except that the reference modulation waveform is a sinusoidal wave with a zero sequence voltage added. The zero sequence voltage can be expressed as the average value of the maximum and minimum values of the three reference modulation waveforms, or can be a third harmonic component added to the reference waveform. The advantage of this technique is that it will allow the modulation index to increase by about 15% before overmodulation and pulse dropping occurs and does not produce zero sequence currents in the three-phase, three-wire configuration.

The main parameters of the modulation process are:

1) The frequency ratio $k = \frac{f_c}{f_m}$, where f_c is the frequency of the carriers, and f_m is the frequency of the modulation wave.

2) The modulation index $M = \frac{A_m}{A_C}$, where A_m is the amplitude of the modulation wave, and A_c is the peak to peak of the carriers.

3) Usually, the frequency ratio is chosen as an odd number which is the multiple of three so that the triple harmonic will not occur in the line voltage even though some of them appear in the phase voltage.

For the basic two-level VSI, one triangular carrier waveform is compared with the reference waveform to get the device switching signals. The carrier and reference waveform for SHPWM are shown in Figure 2.5a. Figure 2.5b and 2.5c show an example for the corresponding output voltage and its spectrum using the above switching logic where f_m=60 Hz, k=15 and M=1.

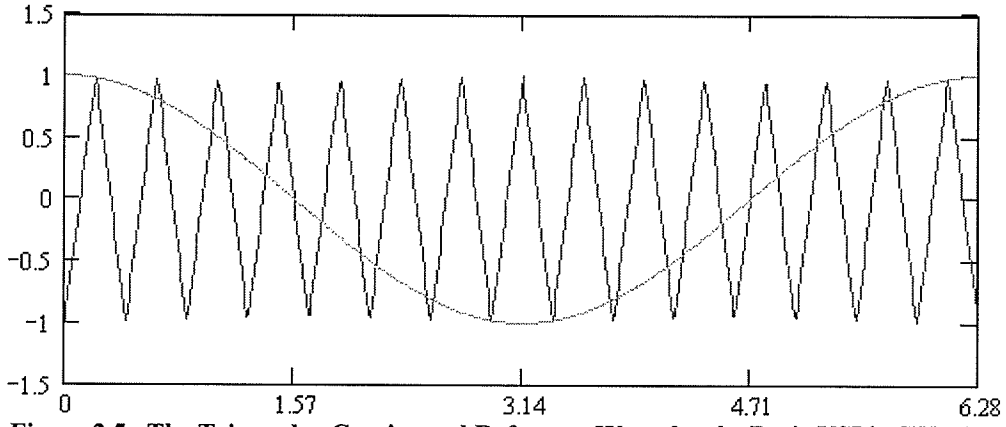

Figure 2.5a The Triangular Carrier and Reference Wave for the Basic VSI in SHPWM

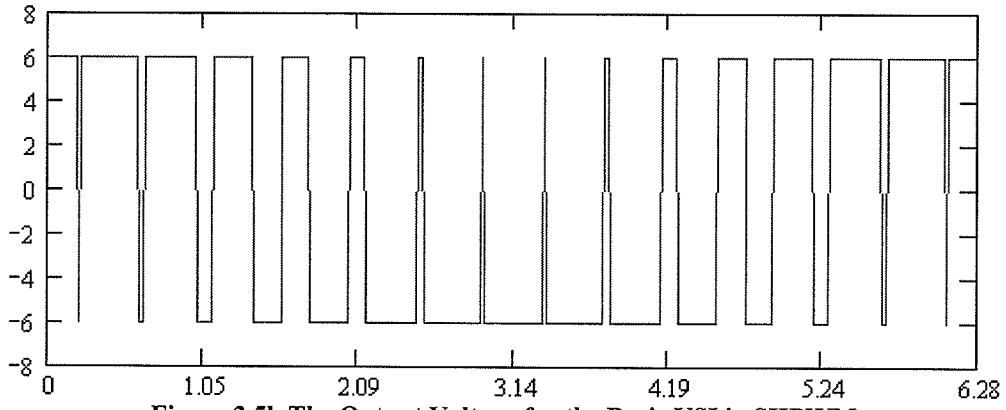

Figure 2.5b The Output Voltage for the Basic VSI in SHPWM

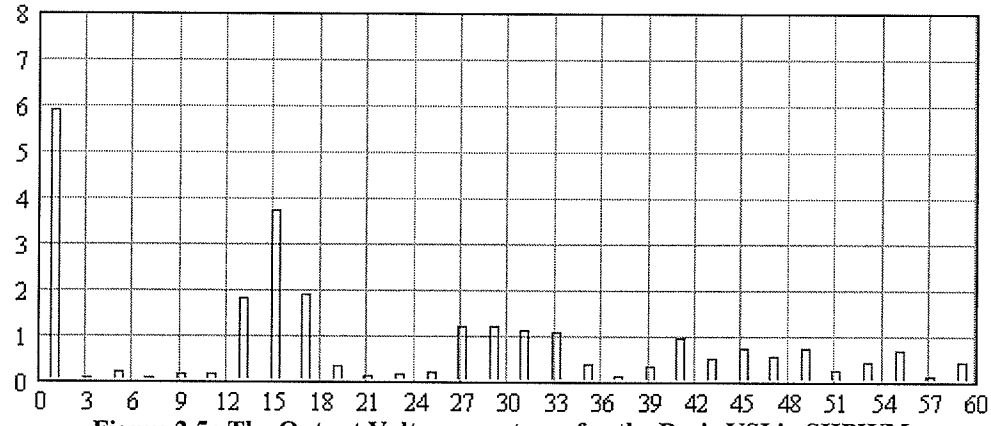

Figure 2.5c The Output Voltage spectrum for the Basic VSI in SHPWM

The carrier and reference waveform for SFOPWM are shown in Figure 2.6a. Figure 2.6b and 2.6c show an example for the corresponding output voltage and its spectrum using the above switching logic where f_m=60 Hz, k=15 and M=1.

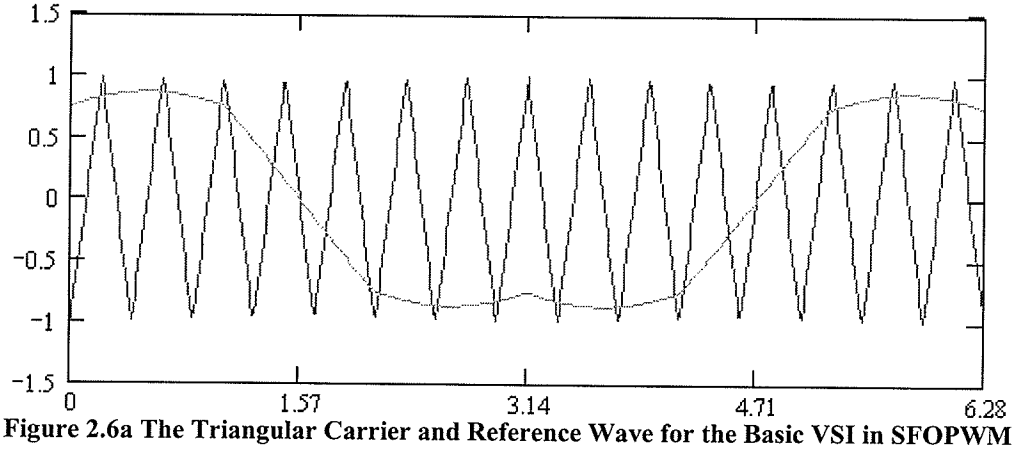

Figure 2.6a The Triangular Carrier and Reference Wave for the Basic VSI in SFOPWM

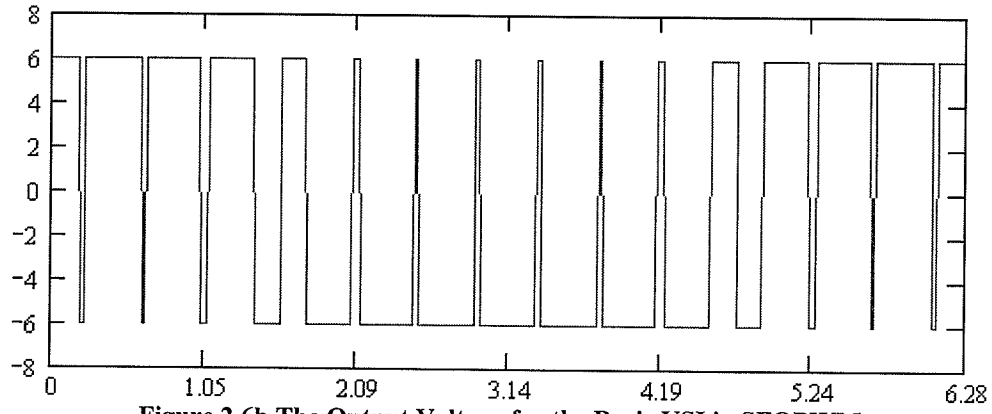

Figure 2.6b The Output Voltage for the Basic VSI in SFOPWM

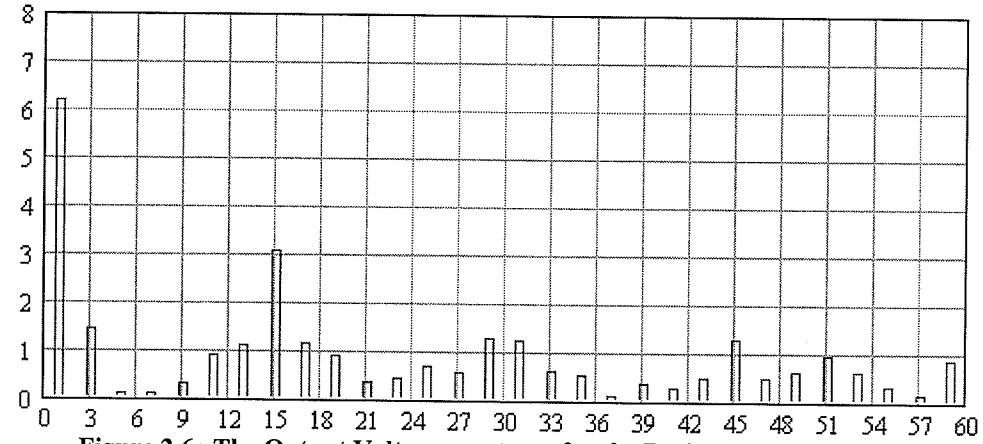

Figure 2.6c The Output Voltage spectrum for the Basic VSI in SFOPWM

Typical results for SHPWM and SFOPWM are shown in Table 3.5, which gives the total harmonic distortion factor (THD) for each case.

The total harmonic distortion factor was defined as the ratio of the root-mean-square of the harmonic content to the root-mean-square of the fundamental quantity, which is expressed as a percent of the fundamental, which gives:

$$THD = \left(\frac{\text{Sum of squares of amplitude of all harmonics}}{\text{Square of amplitude of fundamental}}\right)^{1/2}$$

Table 2.1 Calculated Percent Harmonic Voltage Content using Carrier-based PWM for Basic VSI

Harmonic	SHPWM	SFOPWM
1	95.5	1
5	3.1	1.9
7	0.8	1.4
11	2.4	14.8
13	30.7	17.7
17	31.8	18.3
19	5.3	14.7
23	2.8	7
25	3.5	11
29	20.4	20.4
31	19	19.7
35	6.2	8.3
37	2.2	1.7
41	15.7	4.5
THD_V%	0.602	0.518

It is seen from Table 2.1 that the first large harmonic occurs around 15 for both SHPWM and SFOPWM and then around 30. For SHPWM, 13th and 17th harmonics are significant. For SFOPWM, 11th, 13th, 17th and 19th harmonics are significant. These harmonics are all easily filtered. The fundamental component of these two types of carrier-based PWM is a good approximation to the desired reference waveform though still containing some quantities of the characteristic harmonics.

2.3.2 Optimal Pulse Pattern (OPP) Technique

The most important characteristic of the OPP technique is that it can provide the required harmonic reduction with the minimum number of switchings. As an example, for a two-level

PWM waveform with odd and half-wave symmetries which has n switchings per quarter cycle as shown in Figure 2.7, the magnitude of harmonics are given as follow:

$$b_k = \frac{4E}{k\pi}(1 - \sum_{j=1}^{n}(-1)^j 2 \cdot \cos k\alpha_j) \tag{2.6}$$

In which k=1,3,5,7,....., j=1,2,3,4.....n, b_k is the magnitude of the kth harmonic and α_j is the jth primary switching angle. Even harmonics do not appear because of the half-wave symmetry.

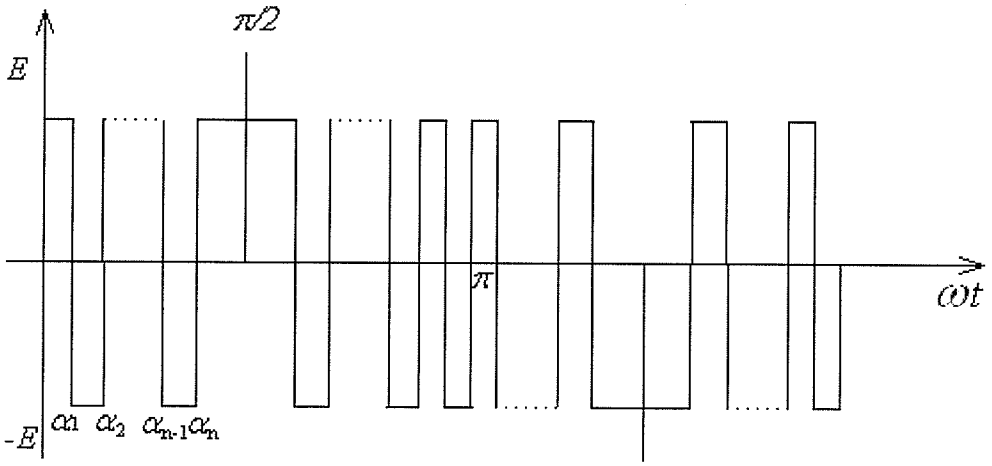

Figure 2.7 A Two Level PWM Waveform with Odd and Half-wave Symmetries

The n switchings in the waveform afford n degrees of freedom. Several control options are thus possible. For example n selected harmonics can be eliminated. Another option that is used here is to eliminate n-1 selected harmonics and use the remaining degree of freedom to control the fundamental frequency magnitude, b_1 of the ac voltage. To find the α's required to achieve this objective, it is sufficient to set the corresponding b_k's in the above equations to the desired values (0 for the n-1 harmonics to be eliminated and the desired ac magnitude for the fundamental) and solve for the α's.

The process of obtaining the correct switching angles for eliminating selected harmonics is normally accomplished in the following step [7]:

a. Decide on the number and order of harmonics to be eliminated.

b. By means of Fourier analysis obtain an expression that describes the harmonic content of the required waveform. Use this expression to assemble a set of equations and set to zero those harmonics selected for elimination.

c. Solve these equations off-line for a range of modulation index values.

d. Arrange for on-line access to these switching angles.

2.3.3 Comparison of Carrier-based PWM and OPP Techniques

As will be shown later, the dc voltage and reactive power are controlled by the converter output voltage. This control can be achieved only by changing the switching angles when the OPP method is used. As well known, it is always possible to solve the equations for various values of designed fundamental ac voltage and store the results in a large look-up table. But in this case it has the problem that there may be some granularity in the solution when the controlling parameter (ac voltage magnitude) falls in between the two contiguous magnitudes. Using PWM techniques, however, the magnitude of the fundamental component can also be changed by varying the modulation index, which gives a smooth continuous control and fast response. Moreover, from a dynamic control point of view, there are advantages in using PWM techniques. Therefore in the later analysis, we will focus on the carrier-based PWM technique.

2.4 Chapter Summary

This chapter presents the basic operating principle, control and PWM switching technique based on the basic two-level VSI, which can be applied to the multilevel converter. It gives a detailed explanation of the four quadrant operation for the VSI based on a simple equivalent circuit. There are two tasks for the control. One is to control the magnitude of the reactive input current

or its phase angle. The other is to maintain the dc voltage constant. The overall control scheme and the control principle are presented which will be the basis of the control for the multilevel converters discussed later. The carrier-based PWM and OPP techniques are discussed. The advantages and disadvantages of the two types of PWM are presented. The final decision is to focus on the carrier-based PWM.

CHAPTER 3

BASIC THEORY OF MULTILEVEL CONVERTER

Multilevel power converters have received tremendous attention in the past few years in the field of high-voltage and high-power applications such as railway traction, ship propulsion, renewable generation, FACTS and UPFC. To reach such power and such voltage levels (MW, kV), various techniques of association have been used in the past because of the technological limitation of the semiconductor voltage (6kV for the IGCTs at present).

Multilevel converters include an array of power semiconductors and capacitor voltage sources. The general structure of the multilevel converter is to synthesize sinusoidal voltage waveforms from several levels of voltages typically obtained from capacitor voltage sources. As the number of levels increase, the synthesized output waveform adds more steps, producing a staircase

waveform which approaches the sinusoidal wave with minimum harmonic distortion. However, increasing the level means introducing voltage imbalance problems on the capacitors at each level.

Three different topologies have been proposed for multilevel converters: the diode clamped, the cascaded multicell with separate dc sources, and the stacked multicell converter. The most attractive features of multilevel converters are as follows [8]:

a. They can generate output voltages with extremely low distortion and low dv/dt.
b. They draw input current with very low distortion.
c. They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated.
d. They can operate with a lower switching frequency.

3.1 Description of Diode Clamped Converter

3.1.1 Neutral Point Clamped Converter

The neutral point clamped (NPC) converter introduced by Nabae [9], is a three-level diode clamped multilevel converter, as shown in Figure 3.1. The three-level converter introduced a new zero voltage level (also called neutral point), other than the negative and positive voltage levels, in comparison to two-level converter. The most simple and well employed method of producing the neutral point is to split the DC link capacitor into two, creating a third level with a zero potential.

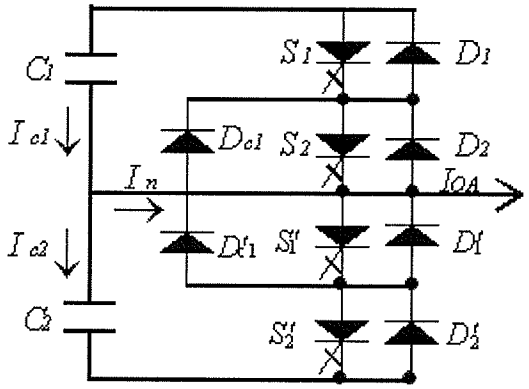

Figure 3.1 Three-level NPC Converter circuit

As shown in Figure 3.1, each arm of the three-level converter consists of four switching elements. By turning on upper, lower or middle two switching elements, the output can be clamped to the positive level, negative level or zero potential (neutral point) respectively, as shown in Figure 3.2.

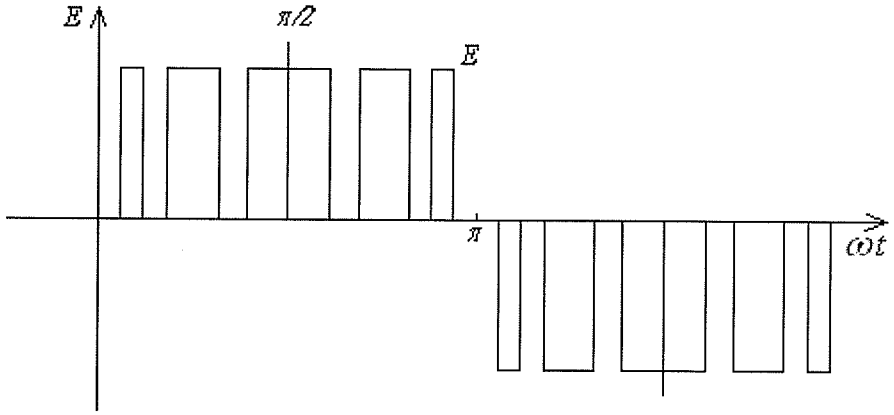

Figure 3.2 A Typical Voltage Waveform for the NPC

Compared with the output voltage waveform of the basic two-level VSI shown in Figure 2.7, it can be seen that for the same device ratings and switching frequency, the power load of the NPC converter has doubled, while each switching involves only half the dc bus voltage and thus power devices could be fully utilized in the high-voltage range. The three-level converter output voltage reduces the harmonic voltages and shows relatively lower harmonic contents in the line currents which result in smaller filter size. Thus, the three-level converter topology is widely

used in heavy power industrial applications due to its high voltage handling and good harmonic rejection capabilities with the currently available power electronics devices.

In summary, the NPC converter has shown a clear market in industrial applications because it offers significant advantages like [10]:

- Small number of additional components to increase the number of levels from 2 to 3(only 2 additional NPC diodes per phase leg)
- Two simple clamp circuits serving the whole 3 phase converter
- Low output voltage harmonics/reduced filter cost and losses because of the three level characteristics
- Simple mechanical design (which is crucial in converters with more than 3 levels)
- Well established direct torque control can be used
- Simple direct series connection of IGCTs to increase the output voltage

3.1.2 Multilevel Diode Clamped Converter (DCC)

As an extension of the three-level NPC, a simplified schematic of one phase of a 7-level DCC is presented in Figure 3.3. Two additional phases would be required for the three-phase converter. As may be seen from Figure 3.3, the general N level converter comprises $2(N-1)$ switches ($S_1 - S_6, S_1'-S_6'$) per phase with 2(N-2) diode clamps ($D_1 - D_5, D_1'-D_5'$) connected to each level of the dc voltage and $(N-1)$ dc capacitors which are common to all the three phases. The voltage across these capacitors is then equal to $V_{ci} = 2E/(N-1)$ in which E is half of the total voltage at the dc link of the DCC.

In this DCC structure, each IGCT thyristor is only required to block the voltage of $2E/(N-1)$ and is well protected against over-voltage by the clamping action of the dc capacitors. The lower group of IGCT thyristors requires the complementary gating pulses of the upper group of the

same number. That means if S_1 is on, then S_1' must be off. It should be noted here that, for each voltage step, only one thyristor must turn on and one thyristor turn off. For example, if S_1 is off, then $S_2, S_3 \ \ldots \ S_{N-1}$ and S_1' are on, and the terminal voltage $+(N-3)E/(\text{N-1})$ is connected to the output terminal through $D_1, S_2, S_3 \ \ldots \ S_{N-1}$ for positive current, or through S_1' and D_1' for negative currents. In other words, in every operating state, N-1 switches are in on state and the other N-1 are in off state. Different switching states provide different output voltages. The corresponding switching logic for the 7-level diode clamped converter is shown in Table 3.1.

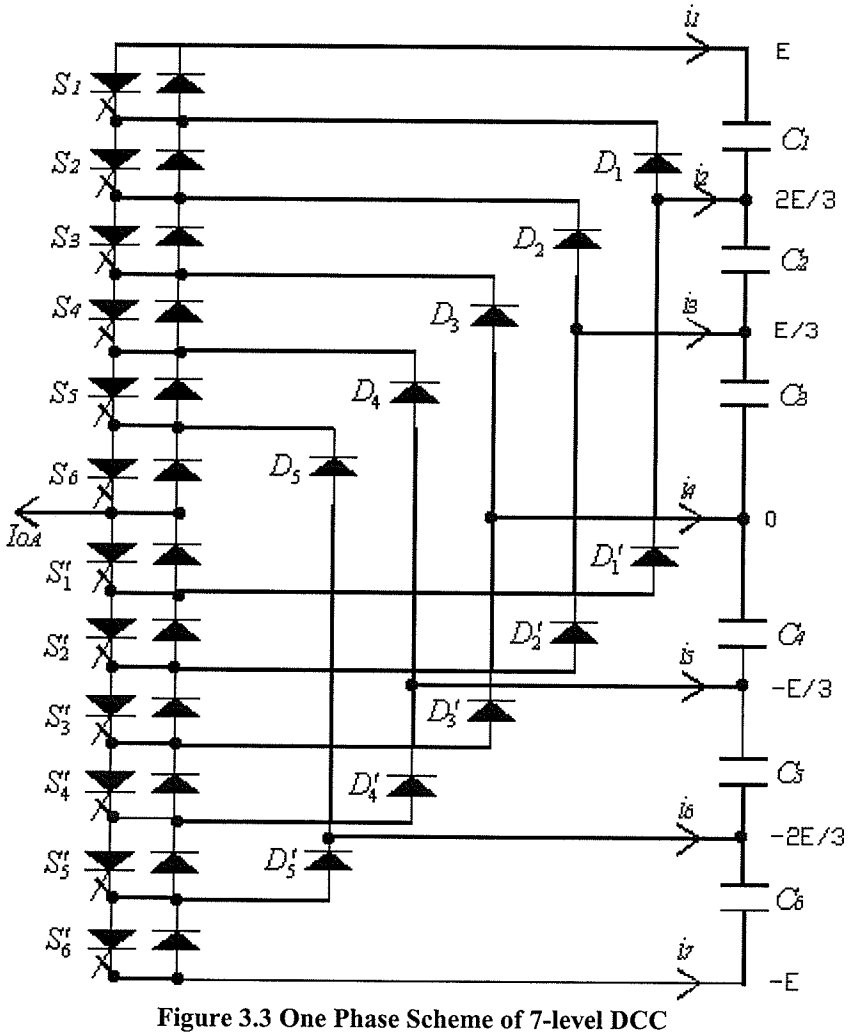

Figure 3.3 One Phase Scheme of 7-level DCC

Figure 3.4 shows the staircase output voltage waveform of the seven-level CDD. It should be mentioned that the clamping diodes are required to block different voltages. It is easy to see that D_2 must block $2 \cdot 2E/(N-1)$ and in general the D_i must block the voltage of $i \cdot 2E/(N-1)$.

Table 3.1 The Switching Logic for 7-level NPC

Thyristor State												Output voltage
S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	
1	1	1	1	1	1	0	0	0	0	0	0	E
0	1	1	1	1	1	1	0	0	0	0	0	2E/3
0	0	1	1	1	1	1	1	0	0	0	0	E/3
0	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	-E/3
0	0	0	0	0	1	1	1	1	1	1	0	-2E/3
0	0	0	0	0	0	1	1	1	1	1	1	-E

There is no doubt that more levels of the output voltage will produce less distortion and better output quality. But balancing the capacitor voltage at each level becomes a problem due to the fact that when establishing sinusoidal output waveform, charge of inner capacitors is much greater than that of outer capacitors [11]. The seven-level DCC is used as an example to explain this.

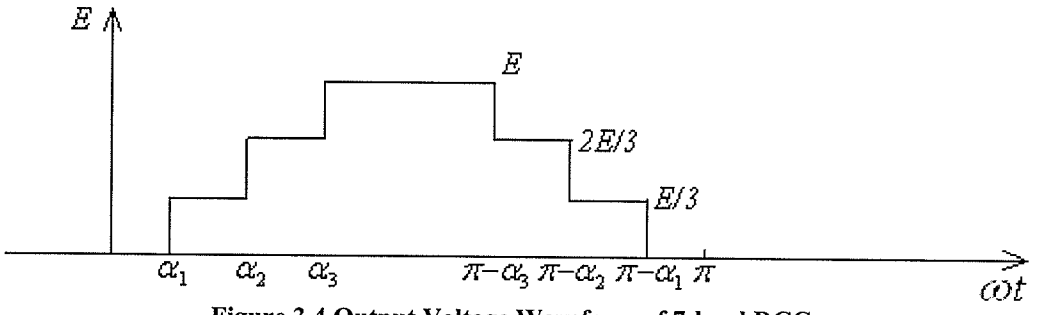

Figure 3.4 Output Voltage Waveform of 7-level DCC

Assuming the output current I_{OA} is a purely sinusoidal waveform with a power factor, $pf = \cos\beta$, it can be expresses as:

$$I_O = \sqrt{2}I\sin(\theta - \beta)$$

Thus, the average value $i1_{avg}$, of input node current $i1$, is given by:

$$i1_{avg} = \frac{1}{2\pi}\int_{\alpha 3}^{\pi-\alpha 3} I_o d\theta$$
$$= \frac{\sqrt{2}I}{\pi}\cos\beta\cos\alpha 3$$

Similarly, the average value $i2_{avg}$ of $i2$, and $i3$, $i3_{avg}$ are given by:

$$i2_{avg} = \frac{1}{2\pi}\int_{\alpha 2}^{\alpha 3} I_o d\theta$$
$$= \frac{\sqrt{2}I}{\pi}\cos\beta(\cos\alpha 2 - \cos\alpha 3)$$

$$i3_{avg} = \frac{1}{2\pi}\int_{\alpha 1}^{\alpha 1} I_o d\theta$$
$$= \frac{\sqrt{2}I}{\pi}\cos\beta(\cos\alpha 1 - \cos\alpha 2)$$

By symmetry, $i4_{avg} = 0$, $i5_{avg} = -i3_{avg}$, $i6_{avg} = -i2_{avg}$, $i7_{avg} = -i1_{avg}$.

Therefore, the average currents per cycle which should be supplied from each capacitor are as follows:

$I_{c1avg} = i1_{avg}$ which gives $I_{c1avg} = \frac{\sqrt{2}I}{\pi}\cos\beta\cos\alpha 3$

$I_{c2avg} = i1_{avg} + i2_{avg}$ which gives $I_{c2avg} = \frac{\sqrt{2}I}{\pi}\cos\beta\cos\alpha 2$

$I_{c3avg} = i1_{avg} + i2_{avg} + i3_{avg}$ which gives $I_{c3avg} = \frac{\sqrt{2}I}{\pi}\cos\beta\cos\alpha 1$

Obviously, $I_{c1avg} < I_{c2avg} < I_{c3avg}$ for $\alpha 1 < \alpha 2 < \alpha 3$. These result in unbalanced charging and hence, unbalanced voltage in the capacitors. The charge of the capacitor $C_3(C_4)$ is largest among the three capacitor groups. The second largest charge is from the capacitor $C_2(C_5)$. The charge of the capacitor $C_1(C_6)$ is the smallest. Also from above equation, it can be seen that the capacitor charge unbalance is independent of the control strategy. When any multilevel PWM is employed, the capacitor charge unbalance is always a problem. It should be noted that if $\cos\beta$ =0, it can operate as STATCOM, but it is a limiting case of operation.

Space Vector Modulation (SVM) and adding a DC offset are two possible solutions to correct the unbalance. But both of them have drawbacks. Employing some additional regulation circuitry can solve the problem [12], but has not met with industrial acceptance.

3.1.3 Switching Technique for the DCC Converter

For multilevel DCC converter, the carrier-based PWM techniques can be extended from the corresponding two-level carrier-based PWM methods. Usually, for an N-level converter in SHPWM or SFOPWM, there are (n-1) carriers with the same frequency f_c and peak to peak amplitude A_c for each phase. By comparing the amplitude of these (n-1) carriers with that of a sinusoidal modulation wave with a certain frequency f_m and amplitude A_m, the corresponding switching devices are switched. The intersections of these carriers with the reference modulation waveform produce the gate signals for the thyristors. In order that the bands they occupy are contiguous, the (n-1) carriers are disposed and the whole carrier wave set is distributed symmetrically on both sides of the zero reference. Figure 3.5 gives an example of the carriers and reference waveform for seven-level DCC.

For the three-level NPC converter, two triangular carriers are compared with the sinusoid reference modulation waveform to get the required switching control signal as shown in Figure 3.6a. The carriers and reference modulation waveform for SFOPWM method are shown in Figure 3.7a. It is easily seen that these two triangular carriers are mirror symmetrical around the zero reference. The intersections of the positive carrier with the positive modulation waveform produce the gate signals for S_1. The intersections of the negative carrier with the negative modulation waveform produce the gate signals for S_2. The complementary thyristor received the negative of these signals. That is S_1' and S_2' received the negative gate signal S_1 and S_2 separately. The gate switching logic to achieve the three voltage levels at the output terminal of the three-level NPC is shown in Table 3.2.

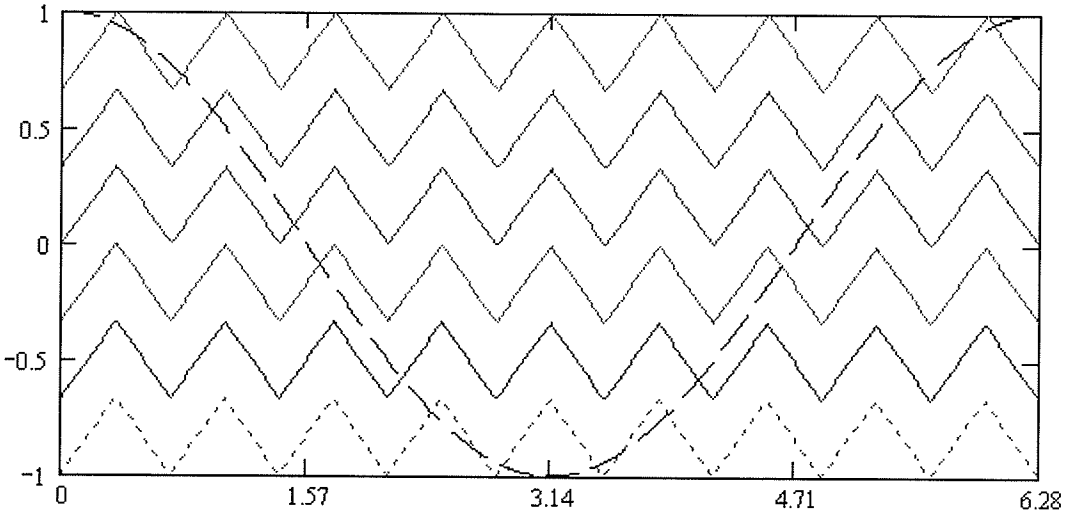

Figure 3.5 Carrier and Reference Waveforms for 7-level DCC

Table 3.2 The Switching Logic for Three-level NPC

State of IGCT thyristors				Output voltage
S_1	S_1'	S_2	S_2'	
1	0	1	0	E
0	1	1	0	0
0	1	0	1	-E

The frequency of the carriers and the magnitude of the modulation waveform will be changed with the changing of the frequency ratio k and the modulation index M. In other words, the magnitude of the fundamental component and harmonic content in the output voltage of the converter as well as the switching losses can be controlled by simply changing k and M. The output for NPC is analyzed further using Mathcad Program. Typical calculation results are shown in Table 3.3 which gives the number of GTO thyristors switched per fundamental cycle (S.No) when the frequency ratio k and the modulation index M are changed, and THD were compared for each case. Figure 3.6b and 3.7b show an example for the corresponding output voltage using the above switching logic for, where f_m=60 Hz, k=15 and M=1.

Table 3.3 Typical Calculation Results for the NPC Converter

frequency ratio	Modulation index	SHPWM		SFOPWM	
		S.No.	THD	S.No.	THD
k=3	M=0.6	4X2	0.297	4X2	0.304
	M=0.7	4X2	0.321	4X2	0.321
	M=0.8	4X2	0.32	4X2	0.313
	M=0.9	4X2	0.313	4X2	0.301
	M=1	4X2	0.307	4X2	0.294
k=9	M=0.6	20x2	0.489	20x2	0.501
	M=0.7	20x2	0.446	20x2	0.437
	M=0.8	20x2	0.4	20x2	0.405
	M=0.9	20x2	0.341	20x2	0.381
	M=1	20x2	0.331	20x2	0.358
k=15	M=0.6	28x2	0.401	28x2	0.381
	M=0.7	28x2	0.375	28x2	0.357
	M=0.8	28x2	0.353	28x2	0.35
	M=0.9	28x2	0.335	28x2	0.345
	M=1	28x2	0.307	28x2	0.303

Note: x2 in the table means that there are two switching devices in series which switched on and off at the same time.

It is easily seen from Table 3.3 that for three-level NPC, the frequency ratio k=15 or 3 and modulation index M=1 in SHPWM method gives better results among the other combination from the aspect of total harmonic distortion and high fundamental component. For SFOPWM

method, the frequency ratio k=15 or 3 and modulation index M=1 always gives better results among the other combinations. Comparing the results from SHPWM and SFOPWM, there is nearly no difference no matter what the frequency ratio and modulation index is.

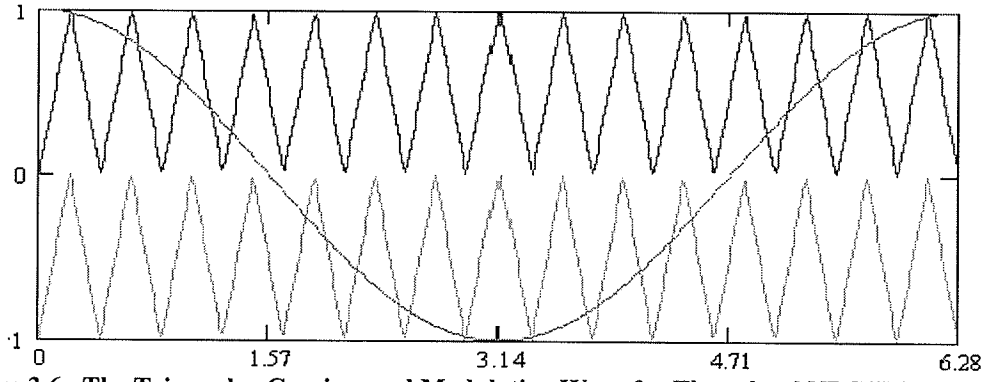

Figure 3.6a The Triangular Carriers and Modulation Wave for Three-level NPC Using SHPWM

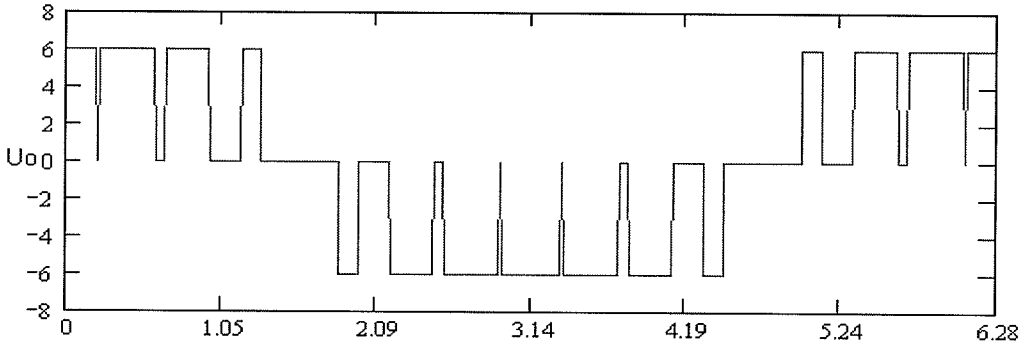

Figure 3.6b The Three-level Output Voltage for NPC Using SHPWM

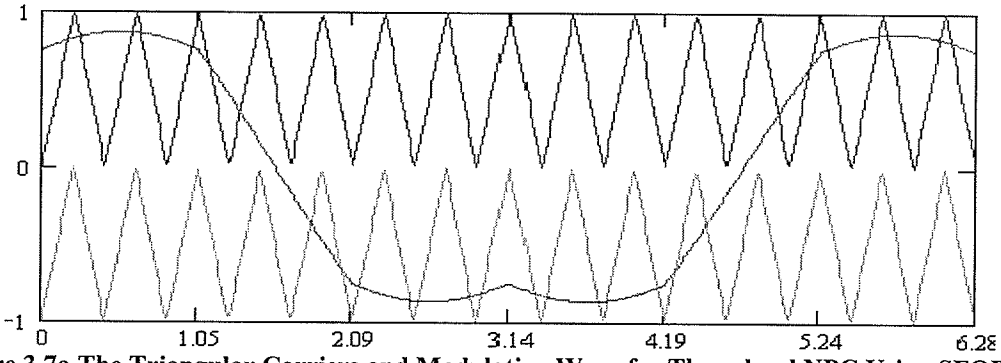

Figure 3.7a The Triangular Carriers and Modulation Wave for Three-level NPC Using SFOPWM

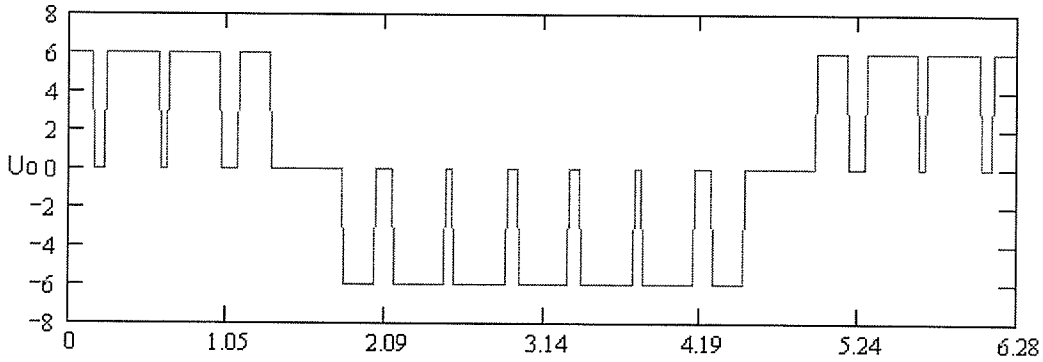

Figure 3.7b The Three-level Output Voltage for NPC Using SFOPWM

3.2 Description of Stacked Multicell Converter

3.2.1 Five-level 2x2 SMC Converter

The SMC topology is a very new structure of multilevel converter able to increase the voltage levels, while decreasing the stored energy in the converter. Basically, the SMC is a hybrid association of commutation cells making it possible to share the voltage constraint on several switches, and also improve the output waveforms of the converter in terms of number of levels and switching frequency. The original idea comes from Escaut [13]. The concept of Stacked Multicell Converter topology was first introduced by Meynard with a five-level 2x2 SMC [14] which is shown Figure 3.8.

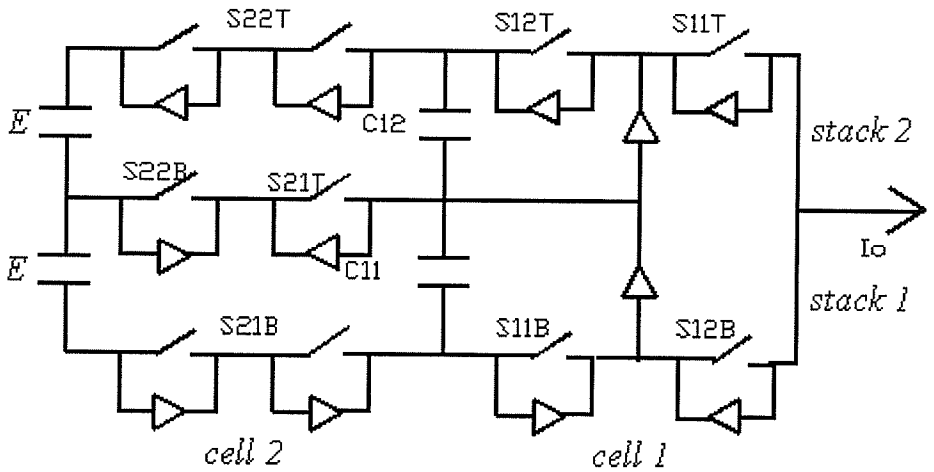

Figure 3.8 Topology of a 2x2 Stacked Multicell Converter

As shown in Figure 3.8, one single cell in one stack of the structure consists of two switches $SijT$ and $SijB$ which have complementary states. The subscript $i \in [1 \cdots n]$ is the number of cells and $j \in [1 \cdots p]$ is the number of stacks. In the steady balanced state, the voltage across the floating capacitors C12 and C11 is one quarter of the dc link voltage 2E [15]. The observation of the above figure shows us that the switches S22T and S21B consist of two devices receiving the same firing signals. To explain this difference, Figure 3.9 shows the voltage across switches for SMC converter.

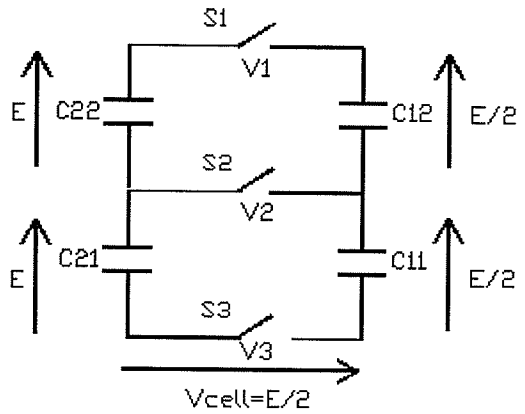

Figure 3.9 Voltage Constraints on Switches

We can see that if the switch S2 is on and S3 is off, and the voltage constraint of the switch S1 is E/2. But if S3 is on and S2 is off, the constraint of S1 is E. This is also true for switch S3 when S1 is on and S2 is off. In conclusion, the voltage constraint V1 (V3) on switch S1 (S3) and V3 depend on the state of other switches S2 and S3 (S1). Therefore S1 and S3 need an additional switch respectively in series to distribute the voltage constraint. But the direct series association of the two switches in the upper and lower branches is not a problem in our case. In fact they switch together only at E/2, and the E is only a static rating. For example, during a half period of modulation, the switches in the upper branch are continuously blocking and the voltage varies between E/2 and E as a consequence of the switching of the bottom cell. Thus the additional series switch could be an ordinary thyristor.

It is now for us to describe the realization of the final cell named cell 1 which is nearest to the AC system. There are two solutions available for the realization of this cell. The first consists in simply replacing the capacitors connected to the AC system by short-circuit. For the second solution, it is possible to replace the final cell by a NPC topology. With the second solution, the number of the controlled power switches is reduced because two IGCT are replaced by the two diodes of the clamp.

3.2.2 Multilevel SMC Converter

As an extension, a generalized structure of one phase for an N-level SMC is shown in Figure 3.10. Another two phases would be required for the three-phase converter, with the dc capacitors common to all the three phases. For the $n \times p$ SMC converter, there are $n \times (p-1)$ floating capacitors C_{ij} with $i \in [1 \ldots n]$ and $j \in [1 \ldots p-1]$ in which p is the stack number and n is the cell number. Each voltage across these capacitors is then equal to $V_{Cij} = \dfrac{i \times 2E}{n \times p}$ in which E is half of the dc link voltage of the SMC. The number of levels for the output voltage equal to:

$N_{level} = (n \times p) + 1$

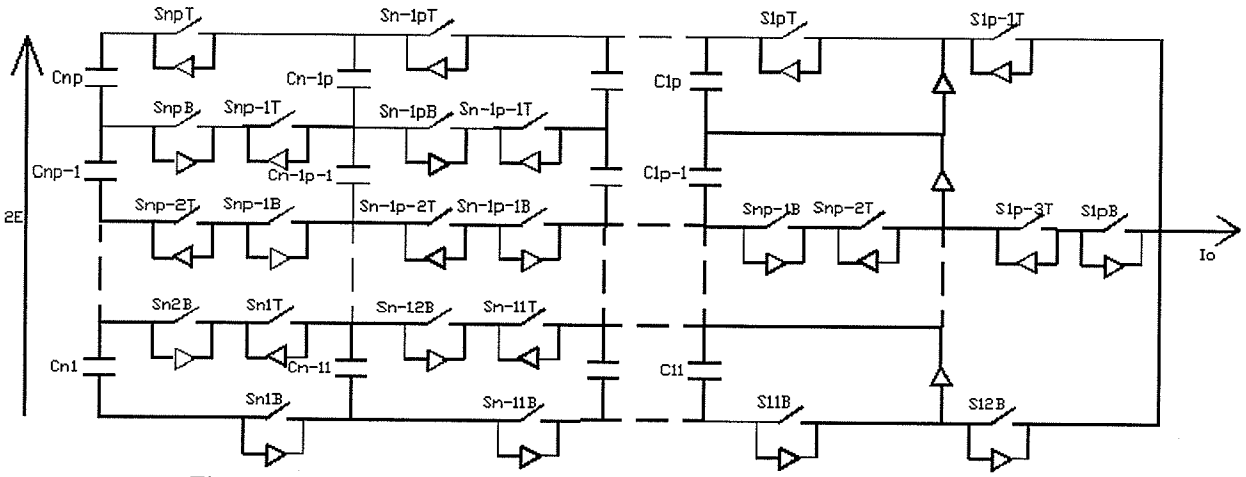

Figure 3.10 A Generalized Structure of One Phase for an N-level nxp SMC

The same voltage constraint applies to all the semiconductors in the structure and is equal to:

$$V_{switches} = \frac{2E}{n \times p}$$

The lower group of IGCT thyristors requires the complementary gating pulses of the upper group of the same number. That means if $SijT$ is on, then $SijB$ must be off. It should be noted here that, for each voltage step, only one thyristor must turn on and one thyristor turn off. For example, if $S_{1_p}T$ is off, then $S_{2_p}T$,... $S_{np}T$, $S_{n1}T$, ... $S_{np-1}T$ and $S_{1_p}B$ are on, and the terminal voltage $+E(n \times p-2)/(n \times p)$ is connected to the output terminal through $S_{2_p}T$,... $S_{np}T$, $S_{n1}T$, ... $S_{np-1}T$ for positive current, or through $S_{1_p}B$ and the reverse diode of other IGCT thyristors for negative currents. In order to carry on the various output voltage levels, the corresponding switching logic is shown in Table 3.4.

Table 3.4 The Switching Logic for N-level SMC

Thyristor State										Output voltage
$S_{np}T$	$S_{np}B$	.....	$S_{1p}T$	$S_{1p}B$	$S_{np-1}T$	$S_{np-1}B$	.....	$S_{n1}T$	$S_{n1}B$	
1	0	.....	1	0	1	0	.....	1	0	E
1	0	.....	0	1	1	0	.....	1	0	(nxp-2)E/(nxp)
.	.	.....	.	.	.	.	.....	.	.	.
.	.	.....	.	.	.	.	.....	.	.	.
.	.	.....	.	.	.	.	.....	.	.	.
1	0	.....	0	1	0	1	.....	1	0	2E/(nxp)
0	1	.....	1	0	1	0	.....	1	0	0
0	1	.....	1	0	1	0	.....	0	1	-2E/(nxp)
.	.	.....	.	.	.	.	.....	.	.	.
.	.	.....	.	.	.	.	.....	.	.	.
.	.	.....	.	.	.	.	.....	.	.	.
0	1	.....	1	0	0	1	.....	0	1	-(nxp-2)E/(nxp)
0	1	.....	0	1	0	1	.....	0	1	-E

It should be noted that n configurations could be used to produce the same level of output voltage. For example, for the level (nxp-2)E/(nxp), the switches $S_{1P}T - S_{np}T$ are switched on and off in turn with one off each time, thus there are n switching states to produce the same voltage

level. It should be mentioned that the floating capacitors are discharged or charged in the different switching states. As an example, for the output level E/2 in the 2x2 SMC shown in Figure 2.8, there are two optional switching states. When $S_{22}T$ is off, the positive output current flows through C12, $S_{12}T$ and $S_{11}T$ discharging capacitor C12. When $S_{12}T$ is off, the positive current flows through $S_{22}T$, C12 and $S_{11}T$ charging capacitor C12. To keep the voltage across the floating capacitors constant, a suitable control strategy should be developed to ensure the discharge and charge are the same. The detail control strategy will be developed in a later chapter.

3.2.3 Switching Technique for the SMC converter

We will limit the discussion of the multilevel SMC to two stacks and n cells. For N-level SMC converter with n cells using carrier-based PWM, there are (N-1) carriers with the same frequency f_c and peak to peak amplitude A_c for each phase. (N-1)/2 oscillate between -1 and 0 with a phase shift of $360^\circ / n$ for cell 1 to cell n at stack 1, and (N-1)/2 between 0 and 1 with a phase shift of $360^\circ / n$ for cell 1 and cell n at stack 2.

For the five-level SMC converter, four triangular carriers are used. As shown in figure 3.11a and 3.12a, two oscillate between -1 and 0 with a phase shift of 180° for cell 1 and cell 2 at stack 1, and two between 0 and 1 with a phase shift of 180° for cell 1 and cell 2 at stack 2. The intersections of the positive two triangular carriers with the positive modulation waveform produce the gate signals for S22T and S12T separately. Similarly, the intersections of the negative two triangular carriers with the negative modulation waveform produce the gate signals for S21B and S11B. The complementary thyristor received the negative of these signals. The

gate switching logic to achieve the five voltage levels at the output terminal of the five-level SMC is shown in table 3.5.

Table 3.5 The Switching Logic for Five-level 2x2 SMC

State of IGCT thyristors								Output voltage
S11T	S11B	S12T	S12B	S22T	S22B	S21T	S21B	
1	0	1	0	1	0	1	0	E
1	0	0	1	1	0	1	0	E/2(mode 1)
1	0	1	0	0	1	1	0	E/2(mode 2)
1	0	0	1	0	1	1	0	0
1	0	0	1	0	1	0	1	-E/2(mode 2)
0	1	0	1	0	1	1	0	-E/2(mode 1)
0	1	0	1	0	1	0	1	-E

Figure 3.11b and 3.12b show an example for the corresponding output voltage using the switching logic in Table 3.5 using SHPWM and SFOPWM respectively, where f_m=60 Hz, k=15 and M=1.

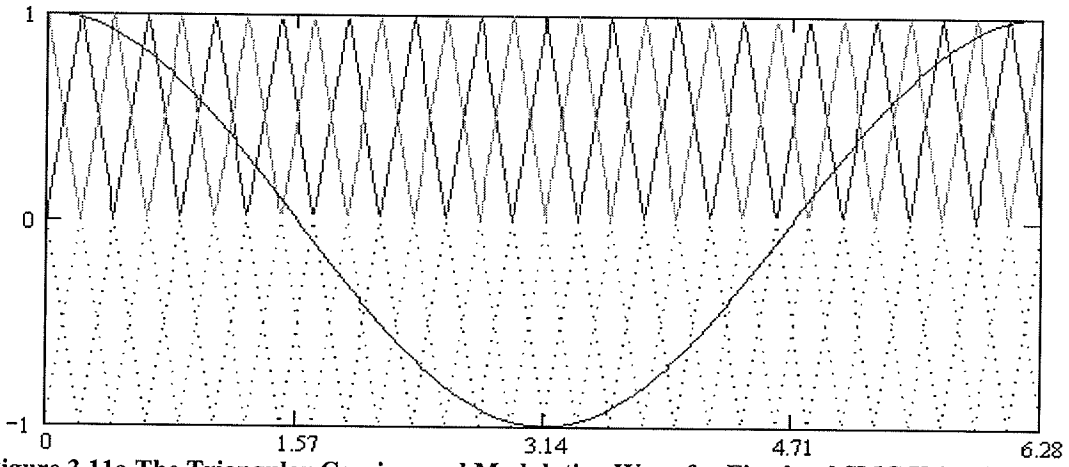

Figure 3.11a The Triangular Carriers and Modulation Wave for Five-level SMC Using SHPWM

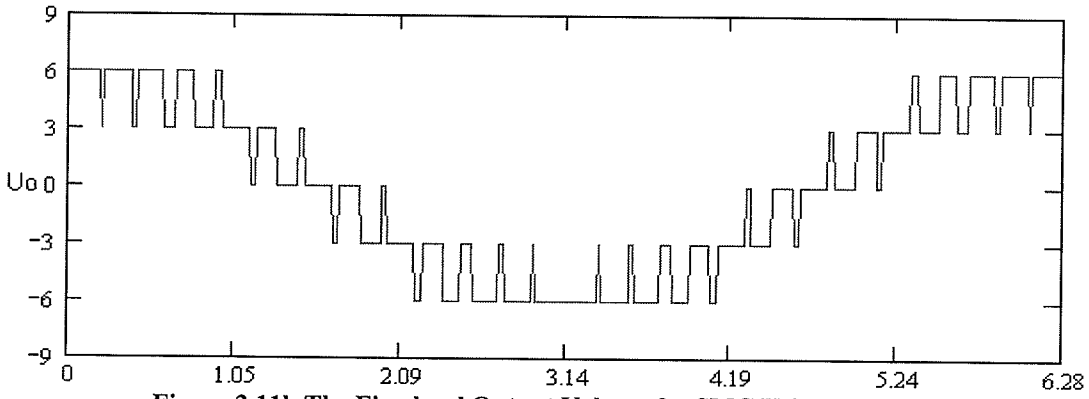

Figure 3.11b The Five-level Output Voltage for SMC Using SHPWM

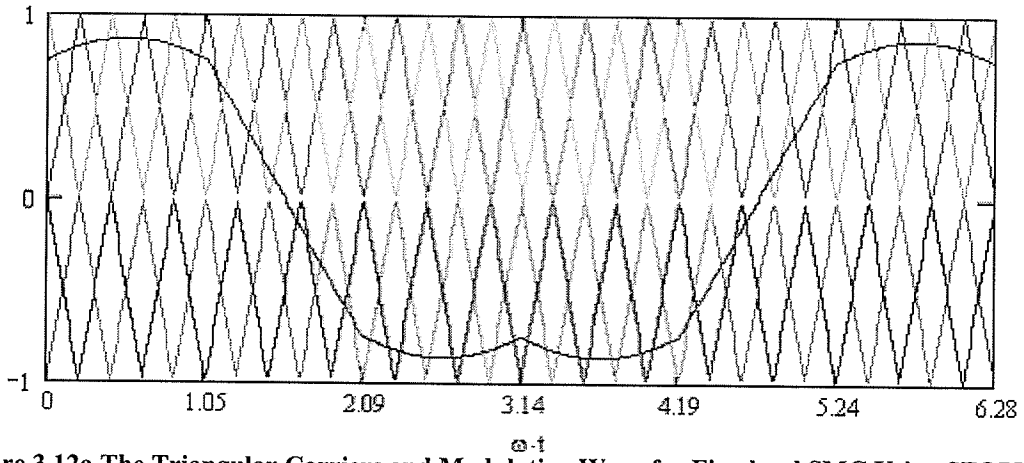

Figure 3.12a The Triangular Carriers and Modulation Wave for Five-level SMC Using SFOPWM

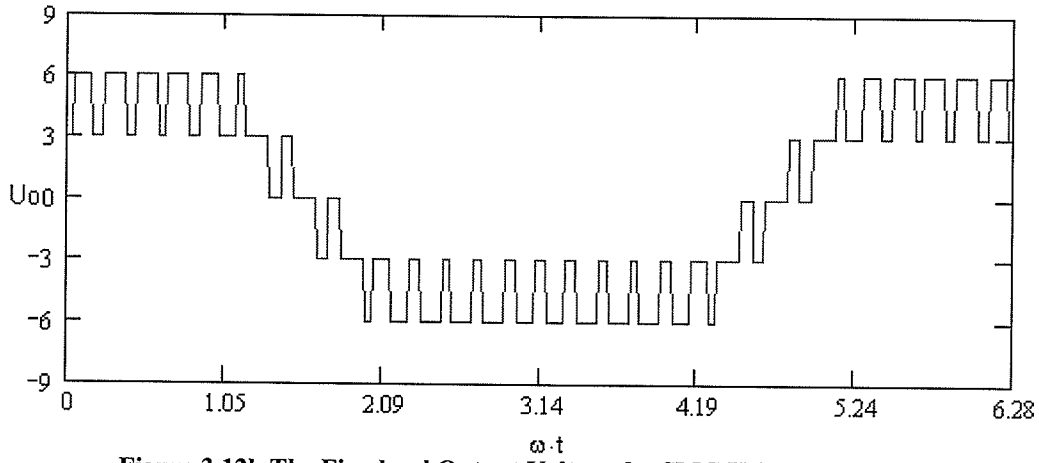

Figure 3.12b The Five-level Output Voltage for SMC Using SFOPWM

As discussed for the NPC converter, we also analyze the five-level SMC using MATHCAD. Typical calculation results are shown in Table 3.6 which also gives the number of GTO thyristors switched per fundamental cycle (S.No) when the frequency ratio k and the modulation index M are changed, and THD were compared for each case.

It can be seen from Table 3.6 that for five-level SMC, the worst condition occurs around M=0.8 for the three different frequency ratios and decreasing or increasing M gives better results for both SHPWM and SFOPWM. The case of k=3, M=1 gives the best result. There is not much difference in total harmonic distortion for M=1 for any of the frequency ratios with SFOPWM technique.

Table 3.6 Typical Calculation Results for the SMC Converter

frequency ratio	Modulation index	SHPWM		SFOPWM	
		S.No.	THD	S.No.	THD
k=3	M=0.6	6X2	0.201	6X2	0.196
	M=0.7	6X2	0.29	6X2	0.31
	M=0.8	6X2	0.242	6X2	0.319
	M=0.9	6X2	0.222	6X2	0.292
	M=1	4X2	0.16	6X2	0.259
k=9	M=0.6	18X2	0.213	18X2	0.25
	M=0.7	18X2	0.253	18X2	0.335
	M=0.8	18X2	0.273	18X2	0.354
	M=0.9	18X2	0.269	18X2	0.322
	M=1	16X2	0.253	18X2	0.274
k=15	M=0.6	30X2	0.139	24X2	0.196
	M=0.7	30X2	0.216	30X2	0.274
	M=0.8	30X2	0.259	30X2	0.318
	M=0.9	30X2	0.251	30X2	0.312
	M=1	28X2	0.217	30X2	0.273

Note: x2 in the table means that there are two switching devices which are switched on and off alternatively.

3.3 Chapter Summary

A brief overview of the structure of the Neutral Point Clamped Converter and the Stacked Multicell converter has been presented in this chapter. The advantages of using the SMC converter were discussed, and will be examined in detail in later chapter.

The Diode Clamped Converter is described. In summary, for an N-level DCC, it comprises $2(N-1)$ switches per phase with $2(N-2)$ diodes and $(N-1)$ DC capacitors. Voltage across these capacitors and the constraint of the IGCT thyristor is equal to $V_{c_i} = 2E/(N-1)$ in which E is the half of total dc link voltage. The clamping diodes are required to block different voltages but this can be solved by series connection to get equal constraint on these clamped diodes. The voltage unbalance on the dc capacitors for multilevel DCC is a problem. Although some methods were developed to solve this, it was not acceptable in industry. The switching technique is presented in detail based on the three-level NPC.

The Stacked Multicell Converter was designed and extended to N-level structure. For a $n \times p$ SMC converter, there are $n \times (p-1)$ flying capacitors. The voltage across each capacitor is $V_c = \frac{i \times 2E}{n \times p}$. The output voltage level equals to $N_{level} = (n \times p) + 1$. The constraint on all the semiconductors is $V_{switches} = \frac{2E}{n \times p}$. Suitable control strategy needs to be developed to keep the voltage across the floating capacitors constant. The switching technique is presented in detail based on the five-level SMC.

CHAPTER 4

COMMUTATION STUDY OF THREE-LEVEL NPC AND FIVE-LEVEL SMC CONVERTER

4.1 Common Specifications for NPC and SMC converter

The study system is a 4.2 MW, 12 kV dc converter for both types of structure. Figure 2.4 and 2.8 show an arrangement of the three-level NPC and the five-level 2×2 SMC separately for one phase, in which the ac system is connected through a wye/wye transformer to the converter. The transformer provides the required isolation voltage to match the converter's output to the power system.

The device we use in both circuits is a reverse conducting IGCT 5SHX 10H6004 whose main parameters are:

V_{DClink}= 3300V, $di/dt = 340A/\mu s$, $I_{TAVM} = 355A$, $I_{TGQM} = 900A$

The clamping diodes used here are 5SDF 04F6004 whose main parameters are:

V_{DClink}= 3300 ~ 3900V, $di/dt = 400A/\mu s$, $I_{TAVM} = 380A$

where

V_{DClink} —the permanent DC voltage the device can block

di/dt—the maximum rate of rise of on-state current and maximum rate of decay of on-state current

I_{TAVM} —the maximum average on-state current

I_{TGQM} —the maximum controllable turn-off current

The detailed parameters for the devices are shown in APPENDIX B.

Usually, the capacitor voltage should be able to vary by $\pm 10\%$. According to the analysis in Section 2.1, the dc voltage is chosen as 12kV. The supply and transformer are rated 4.2MVA with the primary side voltage at 23kV, 60Hz and the secondary voltage at 7.2kV. The main parameters for the transformer are as follows:

$X_T = 0.12pu$, $R_w = 0.003pu$, $X_h = 100pu$

where

X_T—the leakage reactance of the transformer

R_w—the equivalent winding reactance of the transformer

X_h—the magnetizing reactance of the transformer

All the above values are in per unit. Based on the above parameters, the base voltage, current and impedance for the per unit system which is the peak phase voltage and peak phase current are given:

For the primary: $U_{b1} = 18.779kV, I_{b1} = 149.1A, Z_{b1} = 126\Omega$

For the secondary: $U_{b2} = 5.879kV, I_{b2} = 476.3A, Z_{b2} = 112.343\Omega$

The supply impedance was chosen as 0.05pu at an impedance angle of 80°, giving $Z = 1.09 + j6.2\Omega$ or $R = 1.09\Omega, L = 16.5mH$. The dc load resistance should be set at $R_{dc} = 36\Omega$ to get the rated power at rated dc voltage.

4.2 Basic Design Principle for the Current Limiting Circuit

During the preliminary simulation studies, there were some numerical problems which resulted in very high voltage across the switching devices. At first this was attributed to switching stresses in the devices. Hence, a careful study of the commutation paths for the various switchings and the device stresses was carried out.

The current limiting circuit which is shown in Figure 4.1 consists of a capacitor, C_s, inductor, L_s, diode, D_s, and resistor, R_s. The inductance L_s limits the di/dt upon IGCT turn-on to V_{dc} / L_i. This limitation is absolutely essential for the protection of the free wheeling diode during turn-off. Because the diode has no dv/dt limiting snubber, the power density during diode turn-off must be held within safe limits by limiting the reverse recovery current which strongly depends on the di/dt. In order to limit the voltage overshoot across the IGCT during turn-off, the inductance L_s must be appropriately clamped. This may be done using diode D_s and the resistor R_s [16]. In summary, the function of the components in the current limiting circuit is turn-off capacitor C_s for dv/dt limitation, turn-on inductor L_s for di/dt limitation, resistor R_s for resetting clamping inductor and capacitor. The value of the resistor R_s is determined by a reasonable time to dissipate the energy. The main design rules are stated below [17]:

- $L_s = V_{dc}/(di/dt)$ with V_{dc} being the DC link voltage for IGCT.
- $C_s \approx 1.1-1.3L_s$
- $R_s = (0.6-1.1)\cdot(L_s/C_s)^{0.5}$

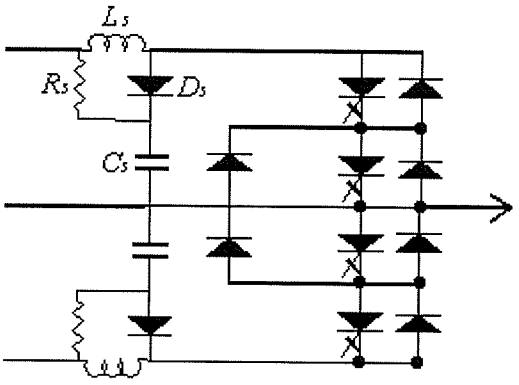

Figure 4.1 The Current Limiting circuit

4.3 Steady Analysis of Three-level NPC

4.3.1 Voltage Stress

In Section 3.1, we have summarized the switching logic for three-level NPC in Table 3.1.

First, the voltage stress of the device will be analyzed in detail with reference to Figure 3.1. In the case of full output voltage of 6kV, there is positive output current flowing through the switches S_1 and S_2 or negative output current flowing through the reverse diodes D_1 and D_2. At this voltage level, the clamping diode D_{c1}' balances out the voltage sharing between S_1' and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. It is also easily seen that the voltage across the clamping diode D_{c1} is the same as S_1' and S_2'. Therefore the switches S_1', S_2' and the clamping diodes D_{c1}, D_{c1}' all need to block 6kV; In the case of zero output voltage, there is positive output current flowing through the devices D_{c1} and S_2 or

negative output current flowing through devices D_{c1}' and S_1'. At this voltage level, the clamping diode D_{c1} pulls the intermediate voltage to one side of the switch S_1, S_1 should block the voltage across capacitor C_1 in positive current. Similarly, when the current is negative, the clamping diode D_{c1}' pulls the intermediate voltage to one side of the switch S_2', S_2' should block the voltage across capacitor C_2. Therefore the switches S_1, S_2' all need to block 6kV; At the negative voltage level of -6kV, there is positive output current flowing through the reverse diode D_1' and D_2' or negative output current flowing through the S_1' and S_2'. The clamping diode D_{c1}' balances out the voltage sharing between S_1 and S_2 with S_1 blocking the voltage across C_1 and S_2 blocking the voltage across C_2. It is also easily seen that the voltage across the clamping diode is the same as S_1 and S_2. The above analysis shows that all the switches and diodes in the NPC circuit should have the ability to block the voltage of 6kV. According to the parameters of the device used in the circuit, direct series connection of two devices is needed for all the switches and clamping diodes in the NPC converter. Therefore, the NPC circuit requires 8 IGCTs and 4 diodes per phase.

4.3.2 Current Stress

Now we analyze the current stresses for the devices. S_1 is switched on and off symmetrically to get full voltage and zero voltage, we can examine the effect of switching each device individually for each direction of current flow as follows:

An initial full output voltage is assumed, if the output current I_o is positive, when S_1 switched off, the current is commutated to D_{c1} at the rate at which the IGCT is switched off. From IGCT

data sheet and assuming a peak current of 600 A, the maximum rate of turn off of the IGCT current would be about 300A/μs.

The clamping circuit is designed to limit the di/dt to 300A/μs. Then for the designed bus voltage of 6kV the required total inductance is 20 μH for the two series IGCT in one switch. The current in the inductor can circulate in the clamp circuit which will increase the thyristor forward voltage by no more than 1400V above the value for the zero voltage. For safety, the inductance could be increased to about 24μH to ensure that the rate of change of current never exceeds 340A/μs. The energy in the inductor will decay with a time constant of L/R in less than 10 μs, so the resistor in the snubber circuit can be chosen as 2.4 Ω. When S_1 is switched back on, the current is transferred from D_{c1} to the thyristor of S_1 through the inductor L, therefore limiting di/dt to full voltage (E) divided by L. The switching on and off of S_1' does not affect the circuit in this case.

If the output current I_o is negative, when S_1 switched off, the load current will be flowing through the reverse diodes of S_1 and S_2. Commutation of the load current from the diode of S_1 to the thyristor of S_1' and the clamping diode D_{c1}' will be determined by the inductor L. Again the voltage across C_1 will increase the current in S_1' at the rate of E/L, and hence control di/dt. When S_1 is switched back on, and S_1' switched off, the current can commutate back at the rate at which S_1' switches off through the circuit S_1 diode, S_2 diode, D and R of clamp, and C_1. Again the di/dt rating of both these diodes should not be exceeded.

4.4 Steady Analysis of Five-level SMC

4.4.1 Voltage Stress

The switch group in one phase is S11T, S12T, S22T, S21T (which is the top stack group) and S11B, S12B, S22B, S21B (which is the bottom stack group), as shown in Figure 3.8 We have summarized the switching logic in Table 3.2.

In the case of full voltage of 6kV, there is positive output current flowing through the switches $S_{22}T$, $S_{12}T$ and $S_{11}T$ or negative output current flowing through the reverse diodes of $S_{22}T$, $S_{12}T$ and $S_{11}T$. Through the voltage clamping by capacitor C12 and C11, the voltage across the switch $S_{22}B$ and the upper clamping diode D_1 is 3kV, however, the voltage across the switch $S_{21}B$ is 6kV. The lower clamping diode D_2 balances out the voltage 6kV sharing between $S_{11}B$ and $S_{12}B$, thus each of these two switches need to block 3kV. In the case of voltage output of 3kV, if the circuit operates in mode 1, there is positive output current flowing through the switches $S_{22}T$, C12, D_1 and $S_{11}T$ or negative output current flowing through the reverse diodes of $S_{12}B$ and $S_{22}T$, D_2 and C12. The voltage across $S_{22}B$, $S_{21}B$ is the same as that of the full output voltage condition. The voltage across $S_{11}B$, $S_{12}T$ is 3kV through the voltage clamping of C11 and the clamping diode; If the circuit operates in mode 2, there is positive output current flowing through $S_{22}B$, $S_{21}T$, C12, $S_{12}T$ and $S_{11}T$ or negative output current flowing through $S_{22}B$, the reverse diodes of $S_{21}T$, $S_{12}T$ and $S_{11}T$, and C12. The voltage across $S_{11}B$, $S_{12}B$ the upper clamping diode D_1 is the same as that of the full output voltage condition. The voltage across $S_{22}T$ is 3kV through the voltage clamping of C12. In the case of intermediate voltage condition of 0kV, there is positive output current flowing through the reverse diode of $S_{22}B$,

$S_{21}T$, D_1 and $S_{11}T$ or negative output current flowing through the reverse diodes of $S_{12}B$ and $S_{21}T$, D_2 and $S_{22}B$. It is clear that the voltage across $S_{12}T$, $S_{22}T$, $S_{21}B$ and $S_{11}B$ all is 3kV. The similar analysis can be carried on for the negative voltage levels. In the above mentioned switching logic, it is noted that $S_{21}T$ is always on during positive voltage period and $S_{22}B$ is always on during negative voltage period. The switches $S_{22}T$ and $S_{21}B$ both block 6kV in negative and positive full output voltage respectively, thus need another common equally rated thyristor in series with the IGCT. According to the above analysis, we can summarize that all the IGCT and clamping diodes only need to block the voltage of 3kV in steady state. Therefore, the SMC circuit requires 10 IGCTs and 2 diodes per phase.

4.4.2 Current Stress

In the full voltage condition, there is positive output current flowing through thyristors $S_{22}T$, $S_{12}T$ and $S_{11}T$. Thyristor $S_{21}T$ is always on but has no current (reverse biased) flowing through it. Then there is no current flowing through the floating capacitors. Now to achieve half voltage, $S_{22}T$ and $S_{12}T$ are switched on and off symmetrically and we can examine the effect of switching each device individually for each direction of current flow as follows:

If the output current I_o is positive, when $S_{12}T$ switched off, the current is commutated to D2 at the rate at which the IGCT is switched off. As for the three-level NPC, we also assume a peak current of 600A and the maximum rate of turn off of the IGCT current would be also about $300A/\mu s$. This assumption gives the inductance in the snubber circuit as $10\mu H$. The current in the inductor can circulate in the clamp circuit which will increase the thyristor forward voltage by no more than 700V above the value for the intermediate voltage, 3000V. For safety, the inductance could be increased to about $12\mu H$ to ensure that the rate of change of current never

exceeds 340A/μs with transient intermediate voltages of 4000V. The energy in the inductor will decay with a time constant of L/R (10μs) which gives $R = 1.2\Omega$. When $S_{12}T$ is switched back on, the current is transferred from D2 to the thyristor of $S_{12}T$ through the inductor L, therefore limiting di/dt to the intermediate voltage (E/2) divided by L which gives 300A/μs. The switching on and off of $S_{12}B$ does not effect the circuit in this case.

If the output current I_o is positive, when $S_{22}T$ switched off, the current is commutated to the thyristor of $S_{21}T$ and the diode of $S_{22}B$ at the rate at which $S_{22}T$ can switch off at about 300A/μs. The current in the inductance is clamped as in the previous case. When $S_{22}T$ is switched back on, the current is transferred from thyristor of $S_{21}T$ and the diode of $S_{22}B$ to the thyristor of $S_{22}T$ through the inductor L, therefore limiting di/dt to the cell voltage (E-E/2) divided by L. The switching on and off of $S_{22}B$ does not effect the circuit in this case.

If the output current I_o is negative, when $S_{12}T$ switched off, the load current will be flowing through the diode of $S_{22}T$, $S_{12}T$ and $S_{11}T$. Commutation of the load current from the diode of $S_{12}T$ to the thyristor of $S_{12}B$ and D1 will be determined by the inductor L which is not clamped with negative current. Again the voltage across C12 will increase the current in $S_{12}B$ at the rate of E/2L, and hence control di/dt. When $S_{12}T$ is switched back on, and $S_{12}B$ switched off, the current can commutate back at the rate at which $S_{12}B$ switches off through the circuit $S_{11}T$ diode, $S_{12}T$ diode, D and R of clamp, and C12. Again the di/dt rating of both these diodes should not be exceeded.

If the output current I_o is negative, when $S_{22}T$ switched off, commutation will take place from the diode of $S_{22}T$ to the thyristor of $S_{22}B$ and the diode of $S_{21}T$. The inductor current is not

clamped in this case, and hence the transient current will increase at the rate of E/2L which can control di/dt. When switching $S_{22}T$ back on and $S_{22}B$ off, the current will transfer back to the diode of $S_{22}T$ through the transient circuit of $S_{22}T$, D and R of the clamping circuit, C22, $S_{21}T$ and C12 which has no current limiting. The transient current is again controlled by the rate at which the IGCT of $S_{22}B$ switches off the current which would be within the specifications provided the peak current does not exceed about 700A.

4.5 Converter Output Analysis

To show a comparison between the three-level NPC and five-level SMC later, the two types of converter should have similarity in switch and diode number, voltage stress and current stress. Typical results are tabulated in Table 4.1 where the number of IGCTs and diodes, and the voltage stress and the current limiting circuits in the converter are compared.

To be consistent, based on the analysis in Section 4.1 and 4.2, we set the parameters in the current limiting circuit for the three-level NPC and five-level SMC as follows:

For NPC: $L_s = 24\mu H$ with V_{dc}=6kV, $R_s = 2.4\Omega$, $C_s = 4\mu F$

For SMC: $L_s = 12\mu H$ with V_{dc}=6kV, $R_s = 1.2\Omega$, $C_s = 2\mu F$

Table 4.1 Similarity between NPC and SMC

converter type	IGCT	Diodes	voltage stress(kV)	current limiting circuits
NPC	24	12	3	2
SMC	30	6	3	8

As seen from Table 4.1, the number of devices is very similar, as are the stresses on the devices, so the switching losses in the two converters are also very similar. The SMC converter needs six more current limiting circuits at half the size than the NPC, but the losses due to the resistors in the circuit is also similar because the resistor in the NPC converter is twice that of the SMC

converter. This means the output of the two converters can be compared on the basis of all the above similarity.

In Chapter 3, detailed analysis of the output voltage of the three-level and five-level converters has been completed using different switching methods, which are shown in APPENDIX A. We only tabulate the results for three-level and five-level converters at M=1 using SHPWM technique here which are shown in Table 4.2. In Table 4.2 different frequencies ratios k and the percentage of the fundamental component based on the value produced by the three-level converter (F.P.) are considered. The output voltage frequency spectra for three-level and five-level converters are shown in Figure 4.1 and Figure 4.2 separately in which M=1 and k=15.

It is easily seen from Table 4.2, Figures 4.1and 4.2 that:

a. When the converter level is increased from three to five, the harmonic distortion is reduced greatly no matter what the frequency ratio is. This is especially noticeable at low frequency ratios.

b. For all the frequency ratios shown in the Table, the difference between the percentage of the fundamental components for the three-level and five-level converters is very little.

c. The first significant harmonic occurs at 11 and 23 for three-level and five-level level converter respectively.

Table 4.2 Typical Results Using SHPWM Method (M=1)

frequency ratio	three-level NPC		five-level SMC	
	THD	F.P.	THD	F.P.
k=3	0.307	1	0.16	1.207
k=9	0.331	1	0.253	1.016
k=15	0.307	1	0.217	0.996

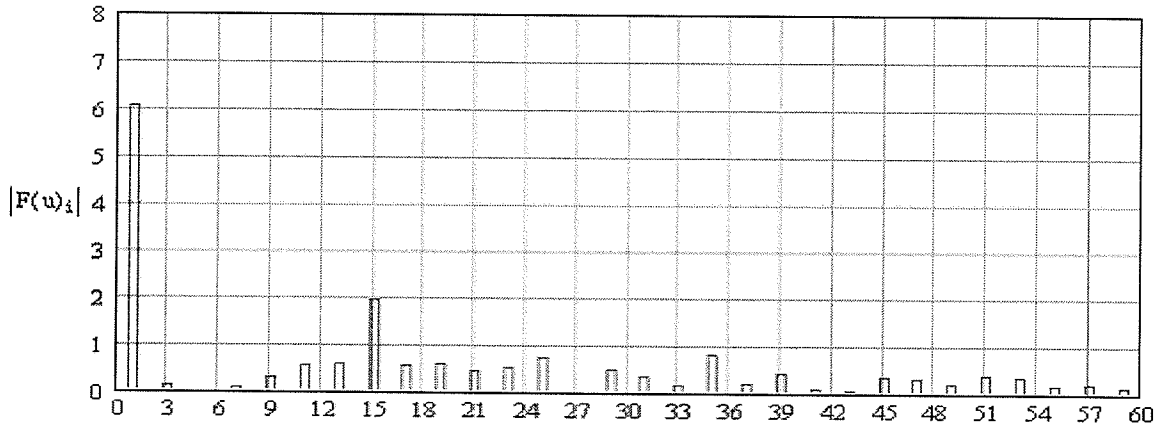

Figure 4.1 The Output Voltage Frequency Spectrum for Three-level Converter

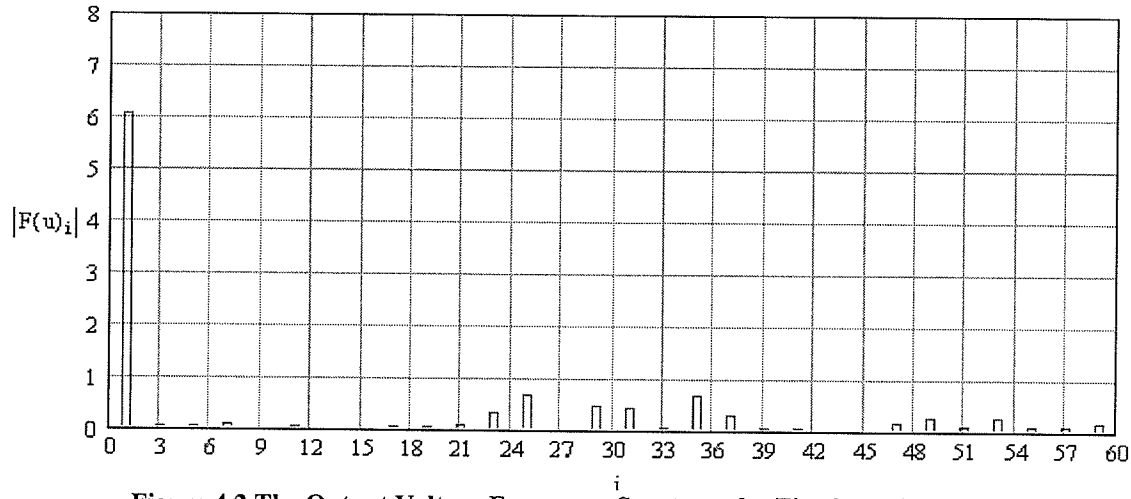

Figure 4.2 The Output Voltage Frequency Spectrum for Five-level Converter

4.6 Chapter Summary

This chapter presents a theoretical comparison between three-level NPC and five-level SMC. It may be concluded that both types of converters have the same number of switching devices (thyristors) and diodes, and the same voltage and current stresses on the devices. The only difference is that the five-level SMC needs six more current limiting circuits of half the size and six floating capacitors compared with the three-level NPC. However, because the capacitors are energy storage devices and do not consume energy, we can say that the losses of the two kinds of converters are nearly the same at the same power rating. Then we can compare the output

voltage characteristics for three-level NPC and five-level SMC on the same bases. For the same modulation index and frequency ratio, the output voltage spectrum produced by the five-level SMC is better than that produced by the three-level NPC, all other characteristics remaining the same. As mentioned above, the five-level SMC shows clear advantages over the three-level NPC for the same fundamental voltage, switching losses and device stresses, but better results for harmonic elimination in theory.

CHAPTER 5

PERFORMANCE OF DC CAPACITORS AND FLOATING CAPACITORS

5.1 Basic Ripple Analysis on the Capacitor

While it is often assumed that the voltage on the dc capacitors and floating capacitors remain constant in analysis, there is always a ripple voltage which must be limited to a reasonable range. The ripple voltage will introduce non-characteristic harmonics into the output voltage spectrum. The method of analysis of the ripple on the capacitor is the same for three-level and five-level converters and for dc capacitors or floating capacitors. For simplicity, we consider a basic

voltage pulse of the converter as shown in Figure 5.1, in which the capacitor voltage is equal to E and the firing angle is α for $0 < \alpha < \pi/2$.

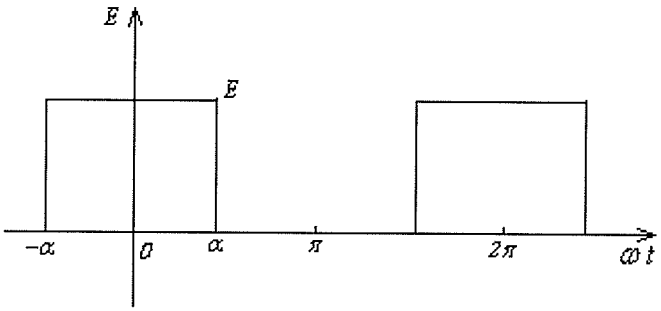

Figure 5.1 Basic Voltage Pulse of the Converter

Performing the Fourier Transformation for this waveform, we have:

$$V_a(\omega t) = \sum_{n=0}^{\infty} b_n \cos(n\omega t) \tag{5.1}$$

Where: $b_0 = \frac{1}{2\pi} \cdot \int_{-\alpha}^{\alpha} E d\omega t = \frac{E}{\pi} \cdot \alpha$

$$b_n = \frac{1}{\pi} \cdot \int_{-\alpha}^{\alpha} E \cdot \cos(n \cdot \omega t) d\theta = \frac{2 \cdot E}{\pi} \cdot \frac{1}{n} \cdot \sin(n \cdot \alpha)$$

And: $n = 0,1,2,...,\infty$

Then we have the voltage for phase b and phase c:

$$V_b(\omega t) = V_a(\omega t - \frac{2\pi}{3}) \tag{5.2}$$

$$V_c(\omega t) = V_a(\omega t + \frac{2\pi}{3}) \tag{5.3}$$

All harmonics in the phase current are neglected here and the load current I_a is approximated by its fundamental component:

$$I_a = I \cdot \cos(\omega t + \phi) \tag{5.4}$$

Similarly, the current for phase b and c are given as:

$$I_b = I\cos(\omega t + \phi - \frac{2\pi}{3}) \tag{5.5}$$

$$I_c = I\cos(\omega t + \phi + \frac{2\pi}{3}) \tag{5.6}$$

According to the power balance principle, the current flowing in the dc capacitor can be expressed as:

$$ic(\omega t) = \frac{V_a(\omega t)I_a(\omega t)}{E} + \frac{V_b(\omega t)I_b(\omega t)}{E} + \frac{V_c(\omega t)I_c(\omega t)}{E} \tag{5.7}$$

Then, the dc voltage ripple produced by the current flowing through the DC capacitor $ic(\omega t)$ is:

$$Vr(\omega t) = \frac{1}{C}\cdot\int_0^{\theta} ic(\omega t)d\omega t \tag{5.8}$$

Where C is the DC capacitor in the converter.

For floating capacitor in the five-level SMC circuit, there is only current in one phase flowing through the capacitors in each phase. Therefore similarly, we can get the voltage ripple on the floating capacitor as follow:

$$Vfra(\omega t) = \frac{1}{C}\cdot\int_0^{\theta}\frac{V_a(\omega t)i_{ca}(\omega t)}{Vc} \tag{5.9}$$

$$Vfrb(\omega t) = \frac{1}{C}\cdot\int_0^{\theta}\frac{V_b(\omega t)i_{cb}(\omega t)}{Vc} \tag{5.10}$$

$$Vfrc(\omega t) = \frac{1}{C}\cdot\int_0^{\theta}\frac{V_c(\omega t)i_{cc}(\omega t)}{Vc} \tag{5.11}$$

Where C is the floating capacitor in the SMC converter.

5.2 Voltage Unbalance Analysis

5.2.1 Voltage unbalance on the floating capacitor

It is usually assumed that the cell element in the converter is commutated to provide a constant full, intermediate and zero voltage. However in a typical cell converter, the cell voltage is not constant, as it is the voltage across the floating capacitor whose voltage will fluctuate during a commutation cycle because of the time difference between charging and discharging capacitors. The circuit that will be used as the basis for the following discussion is shown in Figure 5.2.

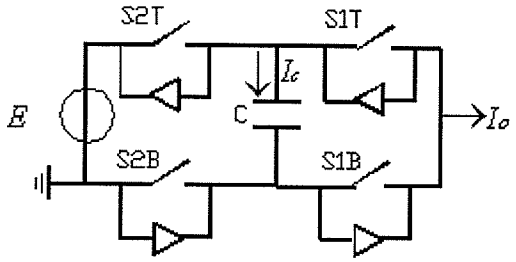

Figure 5.2 Simple model of 2-cell Multicell Converter

The following analysis is based on the assumptions that PWM switching techniques are used and ideal switches are used, implying that the on-state voltage, off-state current, dead-time, delays and switching times are all zero.

To analyze the above circuit, it is necessary to define the switching function s1 and s2 as following:

$$s1 = \begin{cases} 1 & \text{when S1T is on} \\ 0 & \text{when S1B is on} \end{cases} \tag{5.12}$$

$$s2 = \begin{cases} 1 & \text{when S2T is on} \\ 0 & \text{when S2B is on} \end{cases} \tag{5.13}$$

It is easy to see that the output voltage V_o can be expressed as the following:

$$V_o = E \cdot s2 + V_c \cdot (s1 - s2) \tag{5.14}$$

where V_c is the voltage across the floating capacitor.

The current flowing into the floating capacitor I_c is given by:

$$I_c = (s2 - s1) \cdot I_o \quad \textbf{(5.15)}$$

It should be noted that when the status of s1 and s2 is the same which means s1 and s2 are both on or both off, there is no current charging or discharging the capacitor. Therefore this current will not lead to charging and discharging of the floating capacitors. It is only when s1 and s2 are in opposite states that there is current flowing through the floating capacitors to charge or discharge them. If s1 on and s2 off, the current will discharge the capacitors; If s2 on and s1 off, the current will charge the capacitors. The above discussion means the sign of (s1-s2) determines the current flowing through the floating capacitor. We define the switching function for the capacitor current as $S_c = s2 - s1$.

When in ideal switching conditions, s1 and s2 have the same switching waveform except that they are phase-shifted by half the carrier frequency as shown in Figure 3.11a. Therefore, the switching function S_c will have an average value of zero, which implies no charging or discharging of the floating capacitors. However, with low frequency ratios, the switching function S_c, does not average to zero as will be shown below and this causes the drifting in the voltage of the capacitors.

The switching function for $s1$ and $s2$ with frequency ratio of 9 is shown in Figure 5.3. The resulting capacitor switching function S_c is shown in Figure 5.4.

To simplify the analysis of the capacitor voltage imbalance, we approximate the output phase current by its fundamental component. This approximation is reasonable as the switching function is usually selected such that the lower order harmonics are minimized and hence the ac current waveform is as close as possible to a pure sine wave. All harmonics in the phase current

are neglected and I_a is approximated by its fundamental component which is in phase with the fundamental output voltage. The quadrature component of the output current does not affect the analysis.

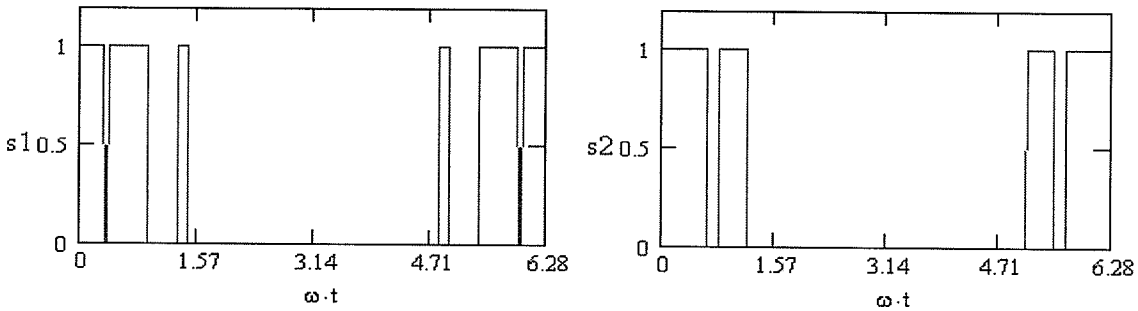

Figure 5.3 Switching Waveform Using PWM with M=1 and k=9

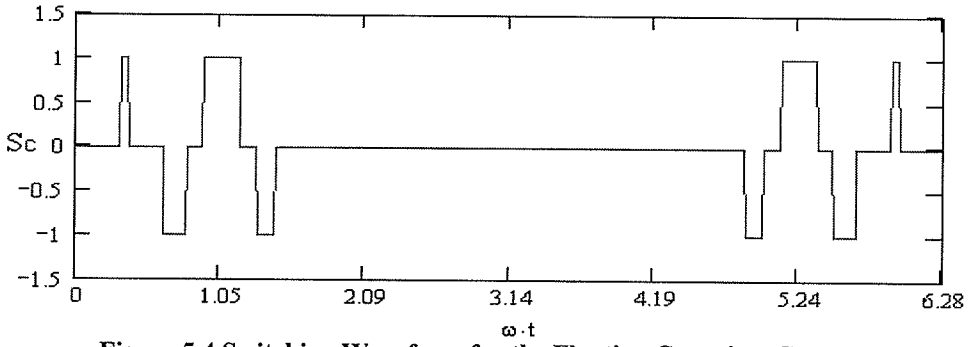

Figure 5.4 Switching Waveform for the Floating Capacitor Current

With $I_a \approx I \cdot \cos(\omega t)$, the change of the voltage across the floating capacitors in charging period in one cycle will be:

$$V_{c1} = \frac{2}{C}\left(\int_{\alpha 1}^{\alpha 2} I \cdot \cos(\omega t)d\omega t + \int_{\alpha 5}^{\alpha 6} I \cdot \cos(\omega t)d\omega t\right) = \frac{2I}{C}[\sin(\alpha 2) + \sin(\alpha 6) - \sin(\alpha 1) - \sin(\alpha 5)] \quad (5.16)$$

Similarly the change of the voltage in discharging period in one cycle will be given as:

$$V_{c2} = \frac{2}{C}\left(\int_{\alpha 3}^{\alpha 4} I \cdot \cos(\omega t)d\omega t + \int_{\alpha 7}^{\alpha 8} I \cdot \cos(\omega t)d\omega t\right) = \frac{2I}{C}[\sin(\alpha 4) + \sin(\alpha 8) - \sin(\alpha 3) - \sin(\alpha 7)] \quad (5.17)$$

Therefore the total change of the voltage across the floating capacitor is:

$$\Delta V_c = V_{c2} - V_{c1} \tag{5.18}$$

When V_{c1} tends to be smaller than V_{c2}, the positive ΔV_c produces the decreasing trend of the capacitor voltage. When V_{c1} tends to be larger than V_{c2}, the negative ΔV_c results in the increasing trend of the capacitor voltage.

As an example, one set of the switching angles for s1, s2 and S_c are calculated using MATHAD as follow:

For s1: $\alpha 11 = 18.984°, \alpha 12 = 21.797, \alpha 13 = 52.734, \alpha 14 = 75.235, \alpha 15 = 82.97$

For s2: $\alpha 21 = 36.563, \alpha 22 = 46.406, \alpha 32 = 68.205$

Then for S_c: $\alpha 1 = 18.984°, \alpha 2 = 21.797°, \alpha 3 = 36.563°, \alpha 4 = 46.406°$
$\alpha 5 = 52.734°, \alpha 6 = 68.205°, \alpha 7 = 75.235°, \alpha 8 = 82.97°$ **(5.19)**

Substituting Equations 5.16, 5.17 and 5.19 into Equation 5.18, the change of the capacitor voltage in one cycle is $\Delta V_c = -0.063 \cdot \frac{2I}{C}$ which means a steady increase of the capacitor voltage during the whole simulation period.

The above analysis shows that even with all the harmonics in the phase current neglected, there is still a significant drift of the voltage across the floating capacitor. The magnitude of this drift depends on the magnitude of phase current. The above analysis can be repeated for phase b and c with the same results.

This drift should be compensated to some extend by changing the intermediate voltages and the resulting load currents. As shown in Figure 5.2, if the voltage across the floating capacitor is a little bit higher than the designed value, the output voltage will be smaller with $s2$ on and $s1$ off according to Equation 5.14 which results in a smaller current charging the floating capacitor. On the other hand, the output voltage will be larger with $s1$ on and $s2$ off which results in a larger

current discharging the floating capacitor. Similar analysis can be presented if this voltage is a little bit lower than the designed value. This characteristic can give some compensation to the voltage drift.

5.2.2 Principle of Voltage Balance Control

From the discussion in Section 5.2.1, it is clear that the switching functions $s1$ and $s2$ must have the same average value and this is not possible with PWM at low frequency ratios. If the on time of the two switch states is same in some period, we can control the amount of change in the floating capacitor voltage to 0 as an average. We notice that the switching waveform for s1 and s2 are symmetrical about π from Figure 5.4. If we exchange the switching signals of s1 and s2 every half cycle or every cycle, the output voltage waveform will not be changed according to the switching logic discussed in the former chapter. The analysis of exchanging the switching signals every half cycle is presented as an example. The new switching states of s1 and s2 at the later half cycle after exchanging is shown in Figure 5.5, The corresponding switching function S_c for the capacitor current is shown in Figure 5.6.

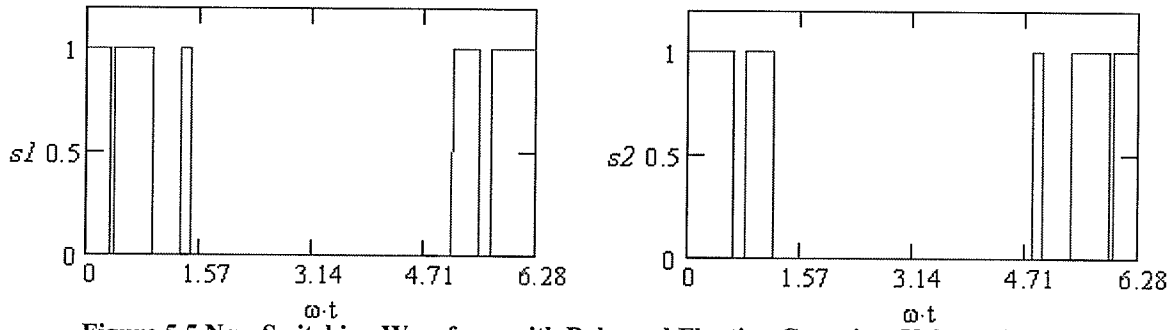

Figure 5.5 New Switching Waveform with Balanced Floating Capacitor Voltage Control

Based on the same assumption used in Section 5.2.1, the change of the voltage across the floating capacitors in the charging period in one cycle now is given as:

$$V_{c1} = \frac{1}{C}\left(\int_{\alpha 1}^{\alpha 2} I \cdot \cos(\omega t)d\omega t + \int_{\alpha 5}^{\alpha 6} I \cdot \cos(\omega t)d\omega t + \int_{2\pi-\alpha 4}^{2\pi-\alpha 3} I \cdot \cos(\omega t)d\omega t + \int_{2\pi-\alpha 8}^{2\pi-\alpha 7} I \cdot \cos(\omega t)d\omega t\right)$$
$$= \frac{I}{C}[\sin(\alpha 2) + \sin(\alpha 6) - \sin(\alpha 1) - \sin(\alpha 5) + \sin(\alpha 4) + \sin(\alpha 8) - \sin(\alpha 3) - \sin(\alpha 7)] \quad (5.20)$$

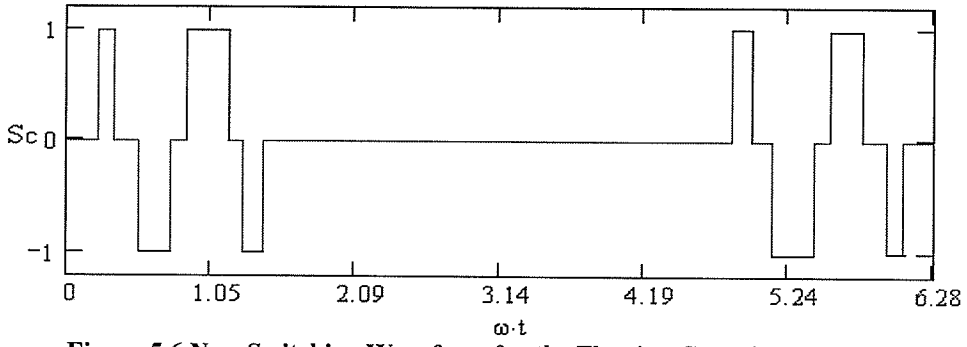

Figure 5.6 New Switching Waveform for the Floating Capacitor Current

Similarly the change of the voltage across the floating capacitors in the discharging period in one cycle now is:

$$V_{c2} = \frac{1}{C}\left(\int_{\alpha 3}^{\alpha 4} I \cdot \cos(\omega t)d\omega t + \int_{\alpha 7}^{\alpha 8} I \cdot \cos(\omega t)d\omega t\right) + \int_{2\pi-\alpha 2}^{2\pi-\alpha 1} I \cdot \cos(\omega t)d\omega t + \int_{2\pi-\alpha 6}^{2\pi-\alpha 5} I \cdot \cos(\omega t)d\omega t$$
$$= \frac{I}{C}[\sin(\alpha 4) + \sin(\alpha 8) - \sin(\alpha 3) - \sin(\alpha 7) + \sin(\alpha 2) + \sin(\alpha 6) - \sin(\alpha 1) - \sin(\alpha 5)] \quad (5.21)$$

It is easily seen that Equations 5.20 and 5.21 have the same expression. This means the voltage fluctuation in discharging and charging period is the same, thus resulting in the zero average voltage change across the floating capacitor and avoiding the voltage unbalance problem. The principle of exchanging the switching signals every cycle is the same. The only difference in changing the switching signals every cycle is that the zero average current is obtained in every two cycles, not in one cycle.

All the above discussion is based on the assumption of positive current which is defined as the current direction from the converter to the AC system. Negative current would result in discharging instead of charging and vice versa.

5.3 Size Selection of DC Capacitors and Floating Capacitors

We know the dc off-state rating of the thyristor is in the range of 3300-3900V. Based on this rating, while leaving a 20% safety margin, the maximum steady state dc voltage of the converter can be set to 12kV which gives 3kV per level.

Basically, the size of the capacitor depends on the magnitude of ripple voltage and capacitor current. For example, when the converter current is positive, the capacitor is charged. When the converter current is negative, the capacitor voltage is discharged. During charging and discharging, the charging frequency is twice the ac system frequency.

For the dc capacitors, it is generally required that the converter has the ability to generate full negative-sequence var for unbalanced loads or in case of phase fault [18]. Therefore, the required dc capacitors C_{dc} should accommodate this design principle and the energy balance equation can be expressed as:

$$\frac{1}{2}C_{dc}(V^2{}_{dc\max} - V^2{}_{dc\min}) = \int_0^{T/4} Q_{\text{var}} \sin 2\omega t dt \qquad \textbf{(5.22)}$$

From the above equation, the required dc capacitor is given as:

$$\begin{aligned} C_{dc} &= \frac{2Q_{\text{var}}}{\omega(V^2{}_{dc\max} - V^2{}_{dc\min})} \\ &= \frac{Q_{\text{var}}}{2\omega\varepsilon V^2{}_{dc}} \end{aligned} \qquad \textbf{(5.23)}$$

where $V_{dc\max}$ and $V_{dc\min}$ represent the maximum and minimum values of dc voltage respectively, Q_{var} is the var rating of the converter, T is the period of the ac system cycle and ω is the ac system frequency. V_{dc} is the average dc voltage which can be calculated by $V_{dc} = (V_{dc\max} - V_{dc\min})/2$. ε is the regulation factor of dc voltage which is given as $\varepsilon = (V_{dc\max} - V_{dc\min})/(2V_{dc})$, whose value may range from 5-20% for practical use. Therefore, given an allowable regulation factor ε, average dc voltage V_{dc} and var rating Q_{var}, the required capacitance C_{dc} can be obtained from Equation 5.23.

For the floating capacitor in the SMC, since each phase has its own separate floating capacitors, calculation of the required capacitance in each phase is straightforward and automatically covers both positive-sequence and negative-sequence reactive power.

Figure 5.7 illustrates the voltage and current out from the converter in which V_o is the converter output voltage and I_o is the current flowing out of the converter. The darker area under current waveform represents the discharging period of the floating capacitor. The lighter area under current waveform represents the charging period of the floating capacitor. Only the fundamental components of both voltage and current are, consequently, considered. Generally, the relationship of the capacitance, total charge and ripple voltage can be given as:

$$C_{dc} = \frac{Q}{\Delta V_{dc}} \tag{5.24}$$

As shown in Figure 5.7, the maximum ΔV_{dc} occurs in the period of $\theta 1$ to $\theta 2$. The total Q, the area under current waveform can be expressed as follows:

$$Q = \int_{\theta 1}^{\theta 2} \sqrt{2} \cdot I_{rms} \cdot \cos(2\pi ft)dt \tag{5.25}$$

where I_{rms} is the rms current of the converter and f is the fundamental frequency.

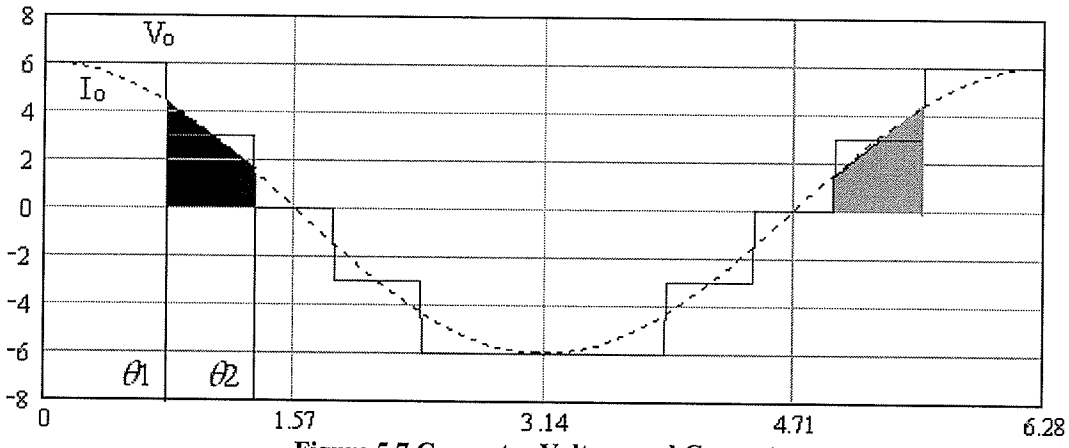

Figure 5.7 Converter Voltage and Current

From Equation 5.24 and 5.25, the dc capacitance requirement becomes:

$$C_{dc} = \frac{I_{rms}}{\sqrt{2} \cdot \pi \cdot f \cdot \Delta V_{dc}} \tag{5.26}$$

Then for a given ΔV_{dc} and operating rms current, the dc capacitance requirement for the given system can be determined using Equation 5.26. And the total energy stored in the capacitor can be determined:

$$E_c = \frac{1}{2} \cdot C \cdot V_{dc}^{\ 2}$$

As a conclusion, given an allowable value for the ripple voltage, then the required capacitance value can be calculated from the average capacitor voltage V_{dc}, the rms output current, and the length of the switching period. The worst case switching period is when the modulation index is 0.5pu which means when s1 and s2 in Figure 5.2 alternate status every half period of the carrier waveform.

Then for a 60Hz-476A peak reactive current and 6kV dc bus voltage, the capacitance and the total energy stored in the floating capacitors for several values of worst case ripple is shown in Table 5.1.

Table 5.1 The Required Capacitance in the Worst case

Voltage ripple	Capacitance	Total energy stored
10%	882μF	23.81kJ
20%	441μF	11.91kJ
30%	294μF	7.94kJ

It is noted that the actual voltage ripple is about half of the maximum calculated ripple in simulation and hence we could choose a ripple of 20% to 30%. The floating capacitors could then be in the range of 300 to 450 μF. We will choose 400 μF capacitors which gives 10.8kJ of stored energy for all the floating capacitors. The dc capacitors are set at 600 μF for both the NPC and SMC, which gives 21.6kJ of stored energy on the dc bus.

5.4 Chapter Summary

In this chapter we study a common method to analyze the voltage ripple on the dc and floating capacitors of the converter which is suitable for the analysis of all kinds of converter configurations. The voltage unbalanced problem of the floating capacitor in the SMC converter has been presented. The conclusions indicate that even with the fundamental component of the phase current is considered, there is still a significant drift of the voltage across the floating capacitor whose magnitude depends on the magnitude of phase current. To eliminate this unbalanced voltage problem in the floating capacitor, a new voltage balance control is introduced. This method exchanges the switching status every half cycle or one cycle for the switching devices. The study shows us that this method can solve the unbalanced voltage problem effectively in theory. A simulation test will be carried out in next Chapter. Additionally, a basic theory to choose the size of the capacitor is presented and the results will be used in later simulation cases. The conclusion indicates that the size of the capacitor mainly depends on the required voltage ripple across the capacitor and the rms current at the rated operation condition.

CHAPTER 6

CONTROL SYSTEM ANALYSIS

The power output and the dynamic performance of the converter can be improved if the control system has been designed to achieve fast dynamic control of the instantaneous current drawn from the power system. This capability ensures that the converter will function usefully during transmission line and load disturbances.

Generally, the aim of the control system is to control the dc voltage to a defined reference and to control the phase angle of the ac current into the converter. This can be achieved by controlling the magnitude (M) and phase (α) of the converter ac voltage. The control system allows the instantaneous values of both M and α to be varied.

The main control system for the NPC and SMC converter is the same. However, the SMC need additional voltage control for the floating capacitors to avoid the voltage drift and complicated start-up of the converter to charge the floating capacitors.

6.1 Mathematical Model and Main Control Loop of the Control System

Figure 6.1 shows the equivalent circuit of the system, where Vs is the source voltage, V_o is the output voltage of the converter, I_o is the current drawn by the converter, and L and R are the total ac inductance and resistance. These voltages and currents are instantaneous quantities and represented in the $\alpha\beta$-phase frame through the abc-$\alpha\beta$ transformation [C] as follows [19]:

$$V_{s\alpha\beta} = \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = [C] \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix}, \quad V_{o\alpha\beta} = \begin{bmatrix} v_{o\alpha} \\ v_{o\beta} \end{bmatrix} = [C] \begin{bmatrix} v_{oa} \\ v_{ob} \\ v_{oc} \end{bmatrix}, \quad i_{o\alpha\phi} = \begin{bmatrix} i_{o\alpha} \\ i_{o\beta} \end{bmatrix} = [C] \begin{bmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \end{bmatrix}$$

$$[C] = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$$

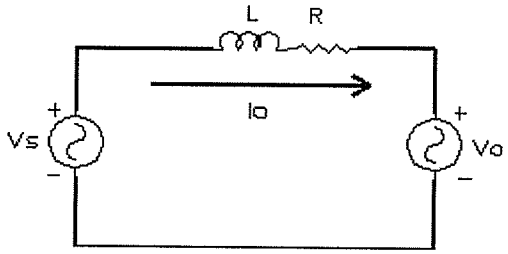

Figure 6.1 Equivalent Circuit of the System

From the equivalent circuit of Figure 6.1, we have:

$$L\frac{di_c}{dt} + Ri_c = V_s - V_o \qquad \textbf{(6.1)}$$

Assuming that the source voltage is a pure sinusoidal without harmonics:

$$V_{sa} = V_s \cdot \cos\theta$$

$$V_{sb} = V_s \cdot \cos(\theta - \frac{2\pi}{3})$$

$$V_{sC} = V_s \cdot \cos(\theta + \frac{2\pi}{3})$$

Then through the above transformation, $V_{s\alpha\beta}$ can be represented as

$$v_{s\alpha\beta} = \frac{3}{2} V_s \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} \quad \textbf{(6.2)}$$

where V_s is the peak value of the phase voltage, and θ is the phase angle. Furthermore, we can apply dq-coordinate transformation [T] to Equations (6.1) and (6.2) as following:

$$V_{sdq} = \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = [T] v_{s\alpha\beta}, V_{odq} = \begin{bmatrix} V_{od} \\ V_{oq} \end{bmatrix} = [T] v_{o\alpha\beta}, I_{odq} = \begin{bmatrix} I_{od} \\ I_{oq} \end{bmatrix} = [T] i_{o\alpha\beta}$$

$$[T] = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}$$

resulting in

$$L\frac{dI_{odq}}{dt} + L\omega \times I_{odq} + Ri_{od} = V_{sdq} - V_{odq} \quad \textbf{(6.3)}$$

which can also be expressed as:

$$L\frac{d}{dt}\begin{bmatrix} I_{od} \\ I_{oq} \end{bmatrix} + L\omega\begin{bmatrix} -I_{oq} \\ I_{od} \end{bmatrix} + R\begin{bmatrix} I_{od} \\ I_{oq} \end{bmatrix} = \begin{bmatrix} V_{sd} - V_{od} \\ V_{sq} - V_{oq} \end{bmatrix} \quad \textbf{(6.4)}$$

and

$$V_{sdq} = \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} Vs \\ 0 \end{bmatrix} \quad \textbf{(6.5)}$$

Figure 6.2 shows the dq ω coordinates where $\omega = d\theta dt$ – both θ and ω are vectors. "x" in Equation (6.3) denotes the vector or cross product. Since $V_{sd} = V_s$ and $V_{sq} = 0$, the instantaneous

active power P flowing into the converter, and instantaneous reactive power Q drawn by the converter, can be obtained as

$$P=\frac{3}{2}V_s \cdot I_{od},\ Q=\frac{3}{2}V_s \cdot I_{oq} \tag{6.6}$$

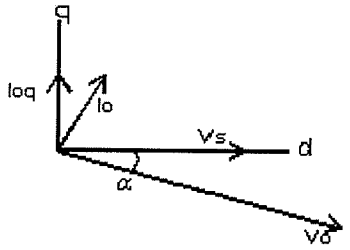

Figure 6.2 The Vector Diagram in $dq\omega$ Coordinates

Therefore, I_{od} and I_{oq} are the active current component and the reactive current component of the output current respectively. Both I_{od} and I_{oq} can be positive or negative. Active current flows out from the converter for positive I_{od} and into the converter for negative I_{od}. The converter generates leading reactive power when I_{oq} is positive and lagging reactive power when I_{oq} is negative. For most cases, it is required that we can directly and independently control the instantaneous active current component and reactive current component I_{od} and I_{oq}.

It is straightforward from Equation (6.4), that in order for the converter to generate the desired current components $I_{od}*$ and $I_{oq}*$, the references of the converter output voltages V_{od} and V_{oq}, and $V_{od}*$ and $V_{oq}*$, should be given as:

$$\begin{bmatrix} V_{od}* \\ V_{oq}* \end{bmatrix} = \begin{bmatrix} V_{sd}+L\omega I_{oq}*-(L\frac{d}{dt}I_{od}*+RI_{od}*) \\ V_{sq}-L\omega I_{od}*-(L\frac{d}{dt}I_{oq}*+RI_{oq}*) \end{bmatrix} \tag{6.7}$$

and

$$V_o* = \sqrt{V_{od}*^2 + V_{oq}*^2},\ \alpha* = \tan^{-1}(\frac{V_{oq}*}{V_{od}*}) \quad \textbf{(6.8)}$$

Based on Equation 6.7 and 6.8, the detail configuration for the system control is shown in Figure 6.3. In this figure, the active current reference I_{od}^* is generated from a PI controller, which regulates the dc voltage of converter. Under normal condition, R is much smaller than ωL and can be neglected.

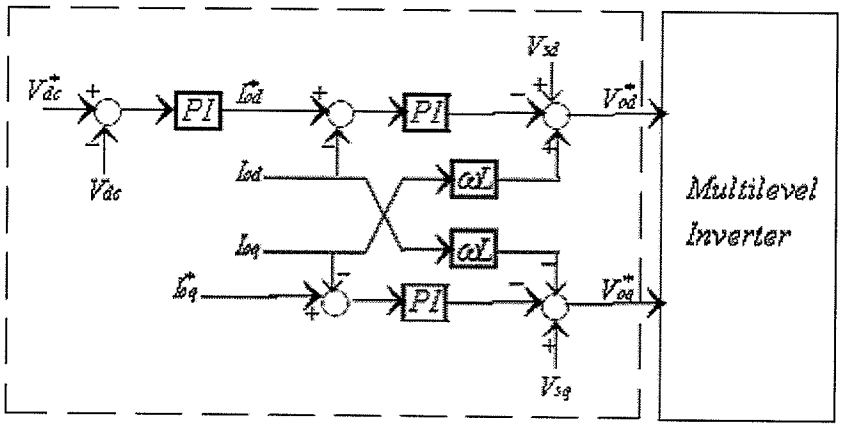

Figure 6.3 Detail Diagram for the Main System Control

In principal, each dc capacitor voltage can be controlled to be exactly the dc command voltage V_{dc}^*. The control loop for V_{dc} controls the total power flow to the converter. If V_o is controlled so that it lags V_s by α, then the real power flowing into the converter can be expressed as:

$$P = \frac{V_s \cdot V_o \cdot \sin\alpha}{X_{LC}}$$

The reactive current reference I_{oq}^* is given according to different compensation aims. The converter may be required to operate at unity power factor when I_{oq}^* is zero, or at some other power factor in order to compensate for other kinds of load. The components of source voltage $V_s = [V_{sd}, V_{sq}]^t = [V_s, 0]^t$ are obtained from the directly sensed source voltage V_{sa}, V_{sb} and V_{sc} through the abc-$\alpha\beta$ transformation—[C] and the synchronous reference frame transformation

[T] as previously mentioned. The phase angle of the source voltage can be obtained from a vector phase-locked loop (PLL) circuit which maintains synchronism between the output voltage and the ac system voltage.

The output control parameters V_{od}^{*} and V_{oq}^{*} as shown in Figure 6.3 are used to generate the modulation reference waveform, V_r for the PWM switching technique by applying the dq-abc transformation.

6.2 Floating Capacitor Voltage Control Loop

Besides the main control loop and dc capacitor voltage control loop discussed above, the floating capacitors in the SMC will require additional control loops because the voltage across the floating capacitors is subject to drift.

In order to maintain the voltage balance across the floating capacitors, a simple principle for the balance control of the floating capacitor voltages is shown in Figure 6.4 in which the switching signals for s1 and s2 are exchanged every cycle. The voltage balance control is required to measure and compare the reference waveform out from the main vector control loop to adjust the switching function of the thyristors. In order to avoid double switching during the exchange, the exchange occurs at the zero crossing of the modulation waveform, when there is no intersection of the modulation and carrier waveform. A zero detector is used on the reference waveform to get the clock signal in the JK flip-flop whose outputs go to two selectors to choose the right carrier. The selected carrier is compared to the reference waveform and produces the switching signals.

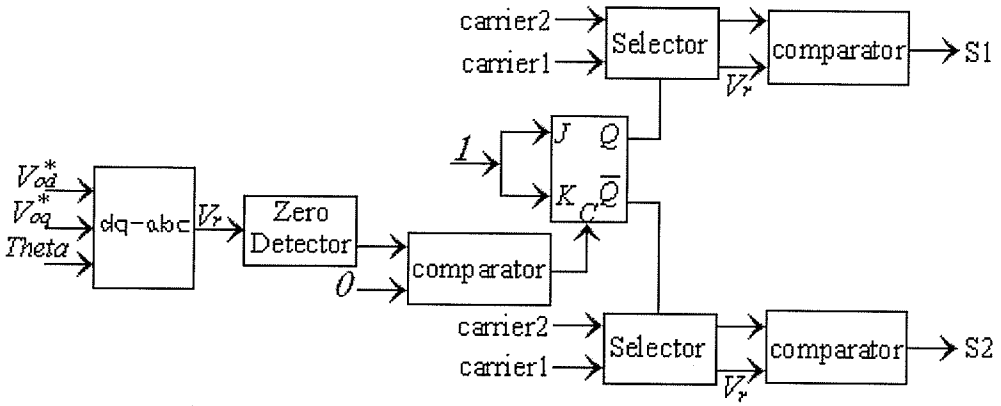

Figure 6.4 The Floating Capacitor Voltage Control Loop

6.3 Start-up of the Converters

The simulation models used for the 3-phase NPC and SMC converter are shown in Figure 6.5 and 6.6 respectively. The only addition to the single-phase circuits discussed earlier is the voltage clamping circuits across the dc capacitors. This circuit will switch on if the dc voltage exceeds 110% of the rated voltage and will quickly discharge the dc capacitors. It will switch off again at 100% of the rated voltage.

Start-up of the converters is often difficult because the capacitors are not charged. The traditional method is to use a charging circuit to charge individual capacitors to their specified voltage levels and then energize the connected transformer. However, this will not only increase the total system cost, but complicate and slow down the process as well. One economic and convenient approach is to use the ac system to start-up the converter system directly because the reverse-conducting diodes of the IGCT in the converters form an ideal six-pulse bridge rectifier. If the converter is connected to the ac system while the IGCT thyristors are blocked, the dc capacitor of the converter will be charged by the ac system through the reverse-conducting diode of the IGCT thyristors, thereby the constant dc capacitor voltage can be established. However, there may be overcurrent problems caused by the charging current of the dc capacitor or overcharging

of the capacitors because of the leakage reactance of the transformer. To avoid the first problem, a pre-insertion resistor can be used to limit the charging current. The voltage limiting circuit used in our models limit the overcharging of the dc capacitors.

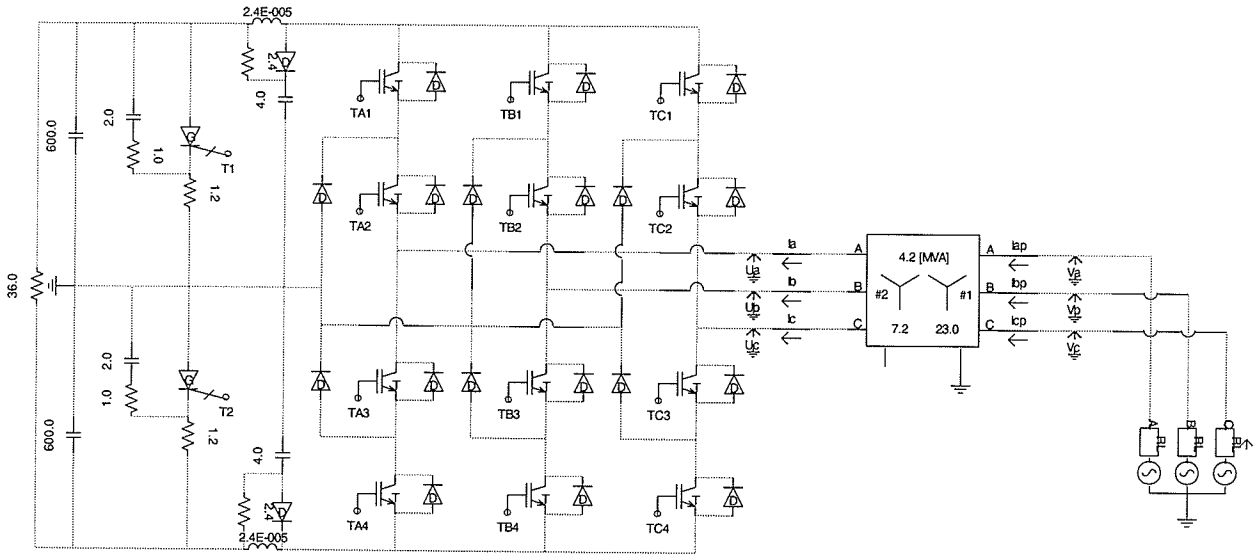

Figure 6.5 Configuration of the Three-level NPC

The dc capacitors of the SMC are charged in a similar fashion to the NPC converter circuit, but the SMC circuit presents further complication as the floating capacitors can not be charged through the reverse conducting diodes. One solution can be realized by initially turning on thyristors S22T and S21B in each phase. This places the floating capacitors in parallel to the dc capacitors. Once the voltage across the capacitors reaches Vdc/4, these thyristors should be switched off. Therefore the dc voltage monitoring circuit was used during the initialization stage to switch off these devices when the capacitors became charged to Vdc/4. The dc capacitors will continue to charge through the diodes to the specified voltage Vdc/2.

6.4 Test Study for the Control System

To confirm the validity of the proposed new SMC and controller design, a simulation model was implemented and tested. A 2x2 five-level SMC using PWM technique is employed as a

candidate in the simulation. The investigation will focus on the following aspect: start-up of the converter, test of balance control for the capacitors, steady state operation and transient operation.

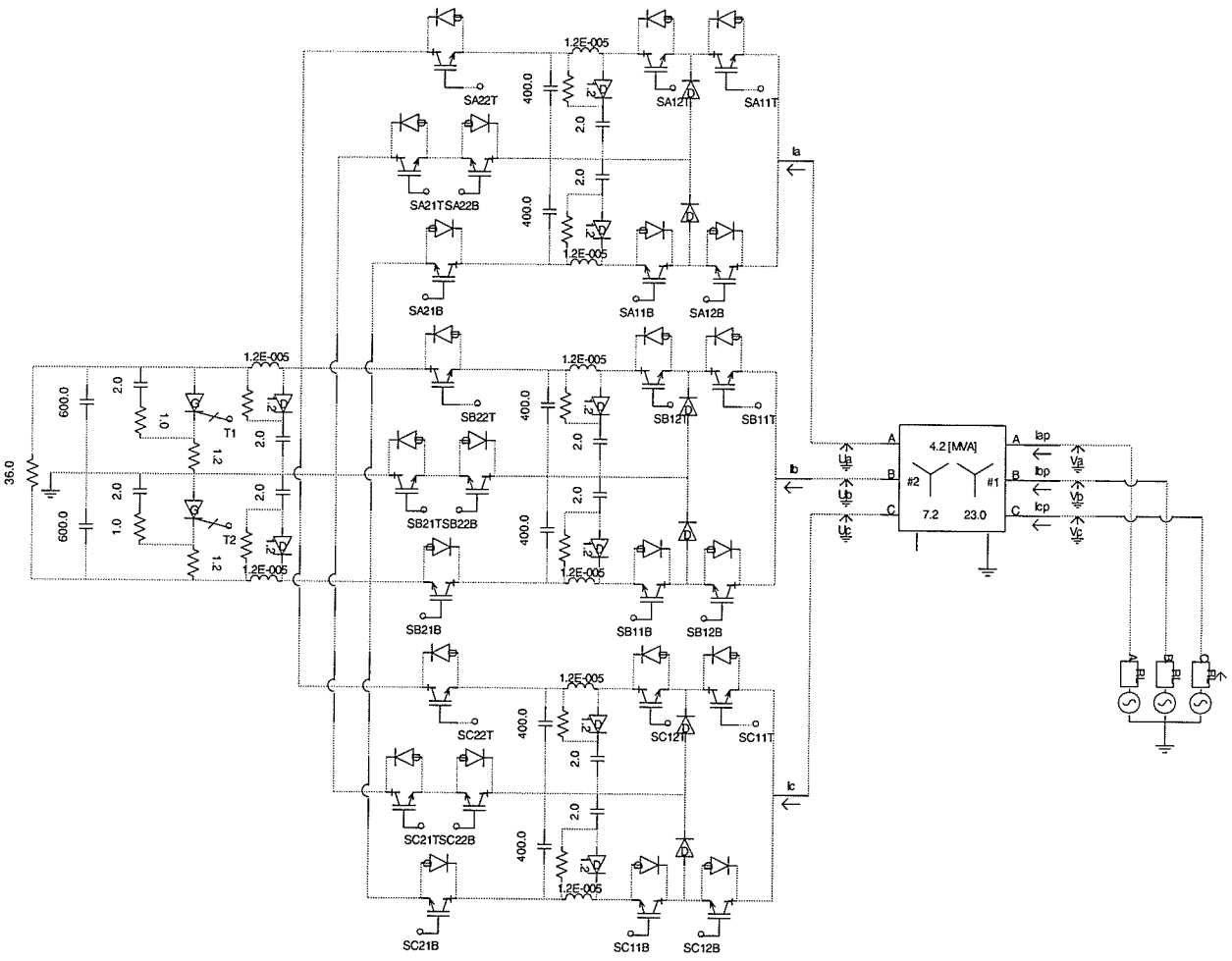

Figure 6.6 Configuration of the Five-level SMC

6.4.1 Start-up of the Converter

In the test system, there is a breaker between the ac system and the SMC, which is turned on at 0.01s. After this time and before the firing of the SMC, the voltage across the floating capacitors is established, and the dc capacitors are charged through the reverse diode of the IGCT. The SMC is fired at 0.05s. The dc capacitors are continuously charged to the required voltage in a short time. The result is shown in Figure 6.7. It is easily seen from Figure 6.7 that the voltage across the floating capacitors and dc capacitors rise at the same rate at the beginning. After the

voltage across the floating capacitor reaches 3kV, the dc voltage continues to be charged to the required value at a faster rate.

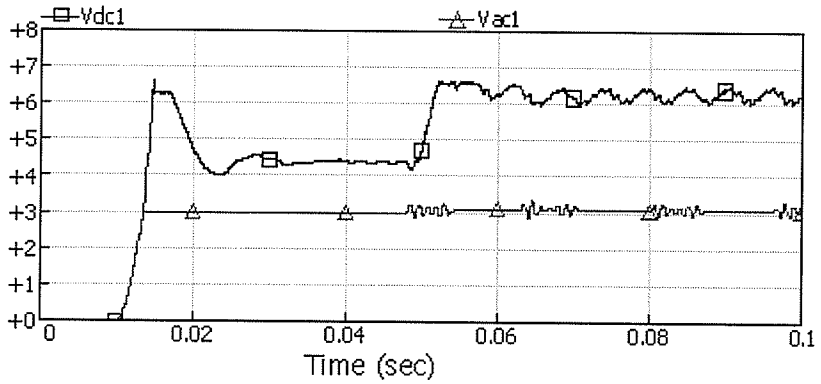

Figure 6.7 The Voltage across the DC Capacitors and Floating Capacitors

Figure 6.8 shows the primary current and voltage of the SMC during the start-up period. It is noticed that the pre-charging current of the converter gives the peak around 1.8pu. Increasing the leakage reactance of the transformer or the inductive reactance in the system can decrease the peak value of the pre-charging current.

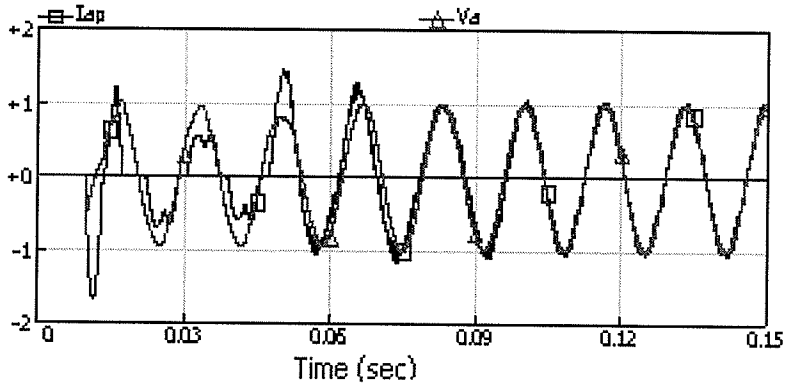

Figure 6.8 The Primary Current and Voltage During the Start-up

6.4.2 Test of Balance Control for the Floating Capacitors

To demonstrate the balance control for the floating capacitors, two tests are performed without and with the balance switching technique. Figure 6.9 shows the voltage across the floating capacitors without balance switching technique. As expected in Section 5.2.1, the voltage across

the two floating capacitors both drift from the rated value and always decreases with the simulation time in the case we tested. As a comparison, the same result with the balance switching technique is shown in Figure 6.10. It can be seen that the voltage has some fluctuation in a very short time at the beginning, but the voltage can be maintained at about 3kV because of the efficient control of the balance switching method. This solves the increased voltage device stresses problem due to the voltage drifting without balance control.

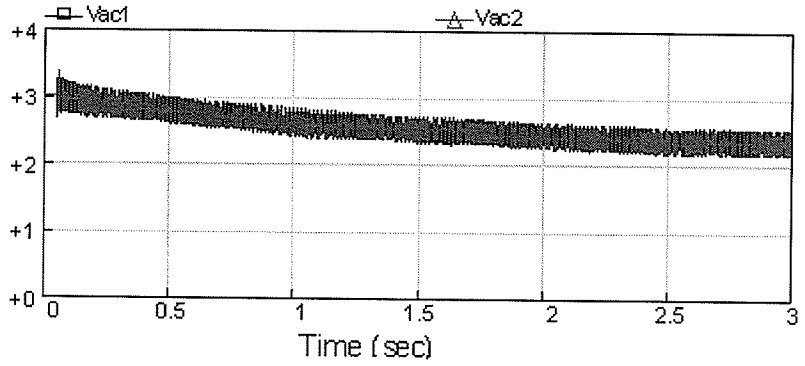

Figure 6.9 The Floating Capacitors Voltage Without the Balance Control

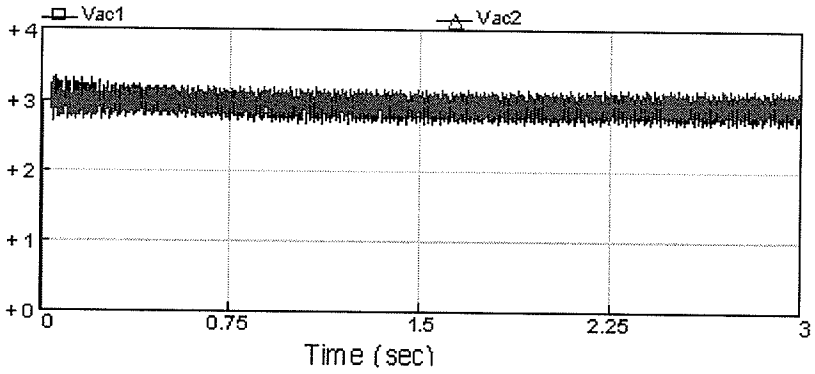

Figure 6.10 The Floating Capacitors Voltage with the Balance Control

The output voltage and current spectra without and with balance control is shown in Table 6.1. The result in the table indicates that the output voltage and current spectrum have been both improved with balance control, especially the low order harmonics.

Table 6.1 Voltage and Current Spectrum Comparison without and with Balance Control

control type	without balance		with balance	
harmonics	voltage	current	voltage	current
5	1.2	1.3	1.2	0.9
7	0.8	0.9	0.3	0.4
11	2	1.6	0.3	0.1
13	1.9	1	0.2	0.1
17	1.4	0.7	0.3	0.1
19	2.4	1	0.3	0
23	4.7	1.8	4.6	1.6
25	12.3	4.1	12.1	4
29	8.8	2.5	9	2.6
31	8.1	2.2	8.2	2.3
35	12.2	2.9	11.9	2.8
37	4.5	1.1	4.6	1
41	0.7	0.1	0.1	0
43	0.9	0.2	0.2	0
47	2.5	0.5	2.1	0.4
49	3.6	0.7	4.5	0.8
THD%	23.389	7.103	23.118	6.481

6.4.3 Steady State Operation

Two sets of measured waveforms from the model are presented in Figure 6.11 and 6.12 to illustrate the SMC behavior under steady state operation. Figure 6.11 shows the converter output voltage and current in a capacitive operating mode. In this case, the current leads the voltage by an angle in which the reference iq is set as -0.8. Figure 6.12 shows the same voltage and current at inductive operation mode. In this case, the current lags the voltage by an angle in which the reference iq is set as 0.8. The reference V_d is set as 1 in both cases. As expected, the multilevel converter voltage is clearly seen with the application of the PWM technique and designed control. The output currents are very sinusoidal without filters which validate the efficiency of this new type of converter design and control strategy.

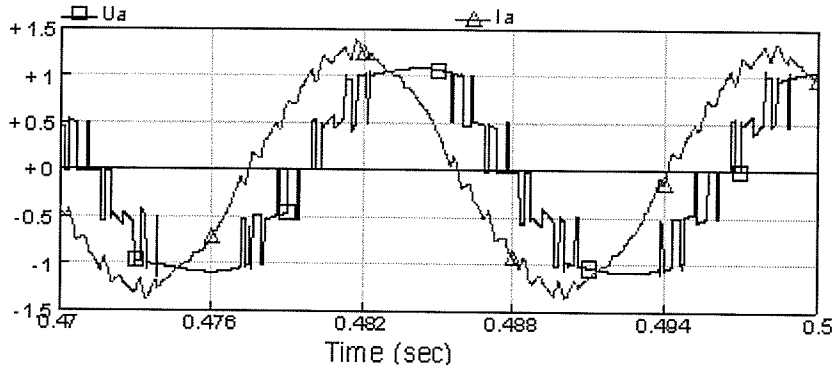

Figure 6.11 The Output Voltage and Current of the 2x2 SMC Using PWM in Capacitive Mode

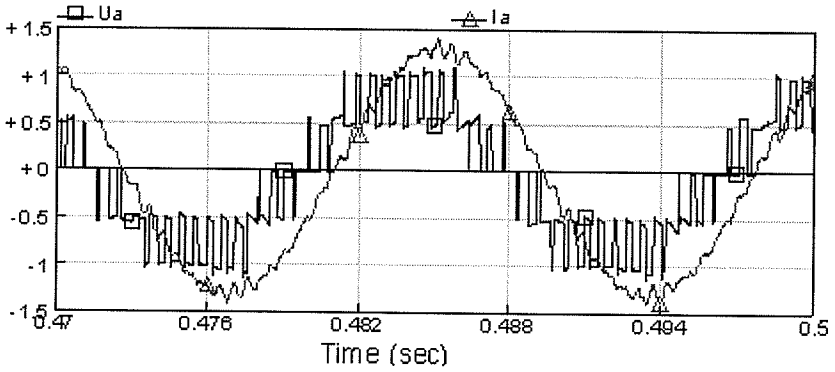

Figure 6.12 The Output Voltage and Current of the 2x2 SMC Using PWM in Inductive Mode

6.4.4 Transient Operation

To examine the dynamic behavior of the control system, the reference reactive current demand signal receives an abrupt change from 0 to 0.8 pu. The response of the SMC is shown in Figure 6.13. As can be seen, iq can catch up with the ordered value in just a few cycles. Although the decoupling in the control system reduces the effect of change in iq on id, there are still some variations in the active current component id for a short time after the transient period, as well the same variation to the dc capacitor voltage V_{dc} in Figure 6.14. This is mainly because of the finite response time of the control system and the quite large harmonics produced by the converter during the transient [20]. It is also easily seen from Figure 6.14 that the average voltage across the floating capacitors can be maintained at about 3kV, but there is larger ripple

on the capacitors because of the change of the amplitude and angle of the output current. The corresponding output voltage and current are shown in Figure 6.15.

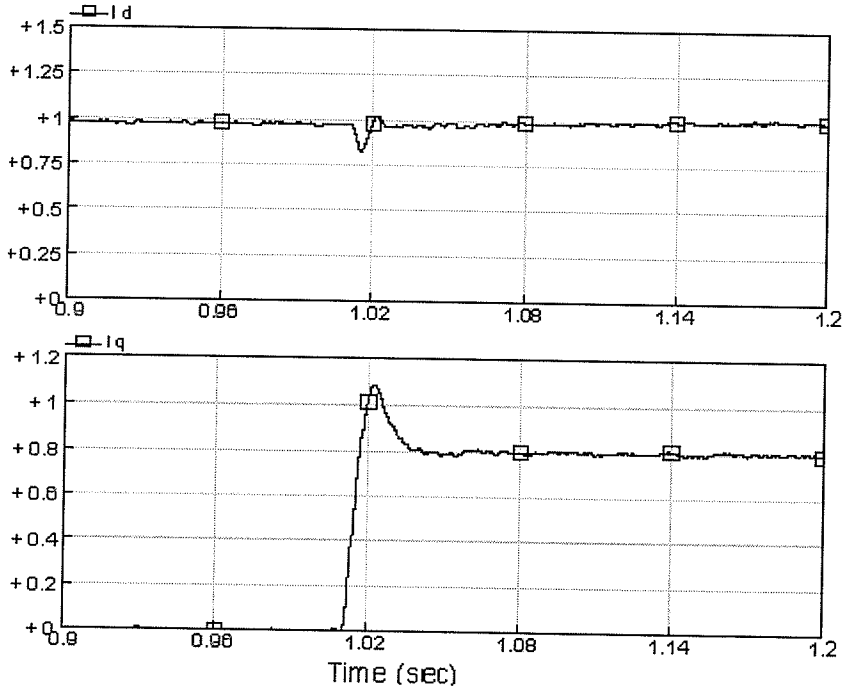

Figure 6.13 Transient Response of the SMC

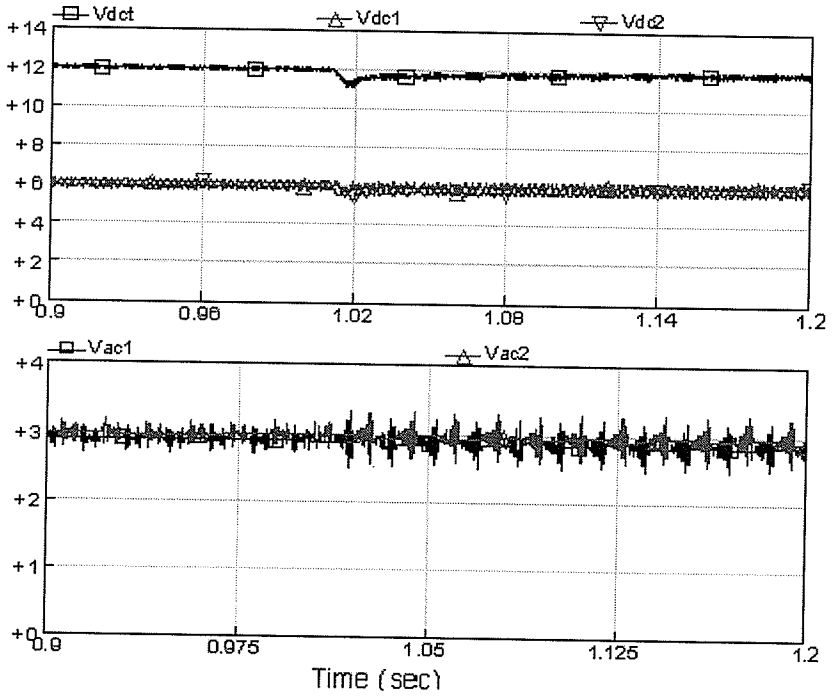

Figure 6.14 Voltage Variations on the dc and Floating Capacitors during Transient Operation

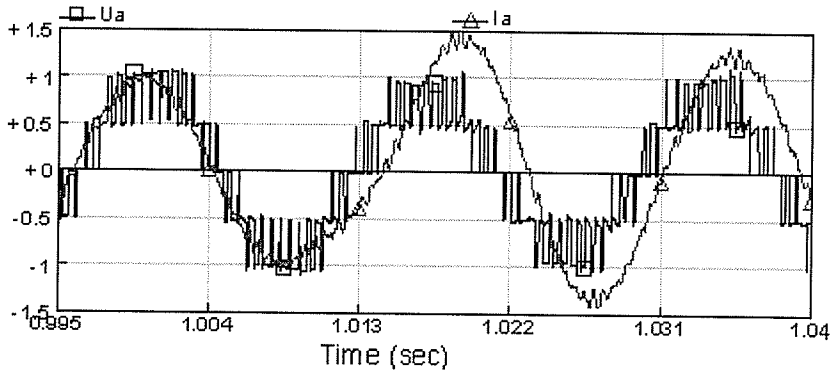

Figure 6.15 The Output Voltage and Current of the SMC during Transient Operation

6.5 Chapter Summary

In this chapter, a mathematical model of the control system using abc-dq transformation is developed which is suitable to all kinds of multilevel converters. Based on the model, the main control system was designed for the converter system. In order to control the balance voltage across the floating capacitors in the SMC, a special switching control was developed. Additionally, the start-up method of the SMC from the ac system side was investigated to reduce the overall size and cost.

The validity of the designed control system and SMC are proven by the experimental test with a candidate design of 2x2 five-level SMC. The simulation results indicate that the design of the control system and the SMC is technically and practically feasible. We can summarize the conclusions as follows:

a. The start-up of the SMC can be realized from the ac system side directly.

b. The special balance switching control of the floating capacitors is proven to be very effective.

c. The steady state operation of the SMC shows superior performance whether in capacitive or inductive mode with the designed control system.

d. The response of the SMC to the dynamic operation is fast and effective. The continuous variation of the output reactive current is possible

CHAPTER 7

EXPERIMENTAL COMPARISON OF SMC TO NPC

An experimental comparison will be made between a three-level NPC converter and a five-level SMC converter under identical operating conditions. This comparison will be done with basic PWM modulation with no filters. Identical ac sources, dc loads and controls will be used for both circuits. The detail control parameters are shown in APPENDIX C. Both circuits are initially charged by connecting the ac source to the converters and charging through diode action. The same vector controls discussed in Chapter 6 will be used to control the system. The detail NPC and SMC circuits have been shown in Figure 6.5 and 6.6 respectively.

7.1 Voltage and Current Spectrum Comparison

The voltage, current waveforms and spectra at frequency ratios of k=15 and 9 for the NPC are shown in Figures 7.1-7.6. The same simulation results at frequency ratios of k=15 and 9 for the SMC are shown in Figures 7.7-7.12. In the above figure, we only extract the odd harmonics for the output current, which should be given main concerns, and compare them with IEEE 519 Standard that is shown in APPENDIX D. The percentage harmonic voltage and current contents up to the 49th harmonic with respect to the peak fundamental frequency component of the NPC and SMC converters at different frequency ratios are shown in Table 7.1 and 7.2.

Table 7.1 Voltage Spectrum Comparison between NPC and SMC

Converter Type	NPC		SMC	
harmonic order	k=15	k=9	k=15	k=9
5	1.2	13.3	1.2	1.3
7	2.2	8	0.3	0.5
11	10.9	11.3	0.3	4
13	8.2	13.2	0.2	12.1
17	8.7	8.5	0.3	8.9
19	10.7	7.6	0.3	8.7
23	3.3	12.1	4.6	9.9
25	11	1.2	12.1	0.9
29	8.4	4.9	9	2.9
31	8.5	2.1	8.2	0.8
35	10.2	5.5	11.9	2.6
37	5.2	4.9	4.6	6.3
41	3	0.8	0.1	0.4
43	2.5	4.7	0.2	1.3
47	1.6	6.8	2.1	3.5
49	6.9	5	4.5	2
THD_V%	29.857	32.211	23.118	22.64

Table 7.1 and 7.2 show us that the output voltage and current total distortion decreases with increase of the frequency ratio for the NPC converter. However, for the SMC converter, the voltage and current total distortion is very similar when k=9 or 15. Based on discussion in Chapter 3 and 4, we know that the power losses and device switching frequency in both circuits

are similar when the same frequency ratio is used for both circuits. The output voltage and current spectrum of the SMC converter is always better than that of the NPC converter at the condition of similar power losses and device switching frequency, especially at the lower frequency ratio. All the above results from the simulation are compatible with the theoretical analysis results.

Table 7.2 Current Spectrum Comparison between NPC and SMC

Converter Type	NPC		SMC	
harmonic order	k=15	k=9	k=15	k=9
5	1.3	18	0.9	1.1
7	2.3	8	0.4	0.4
11	7.8	7.6	0.1	3
13	5.2	8.1	0.1	0.2
17	4.1	4.2	0.1	4.2
19	4.7	3.3	0	0.1
23	1.1	4.4	1.6	4.3
25	3.8	0.4	4	1.5
29	2.4	1.6	2.6	0.1
31	2.3	0.6	2.3	0.2
35	2.5	1.3	2.8	0.3
37	1.2	1.1	1	1.7
41	0.6	0.1	0	0.2
43	0.5	1	0	0.2
47	0.3	1.2	0.4	0.2
49	1.2	0.9	0.8	0.6
THD_I%	13.086	23.879	6.481	7.4674

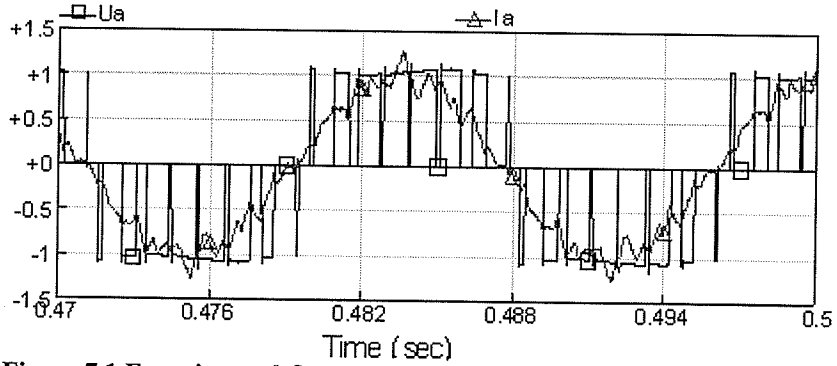

Figure 7.1 Experimental Output Voltage and Current for NPC with k=15

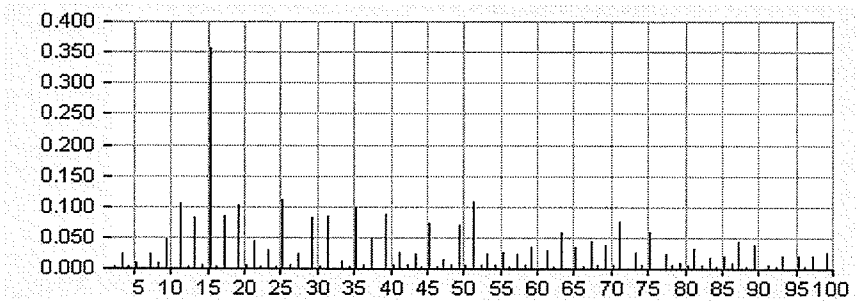

Figure 7.2 Experimental Output Voltage Spectrum for NPC with k=15

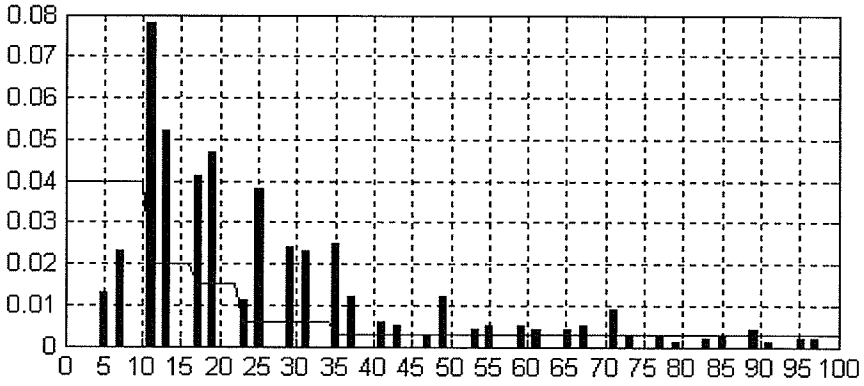

Figure 7.3 Experimental Output Current Spectrum for NPC with k=15

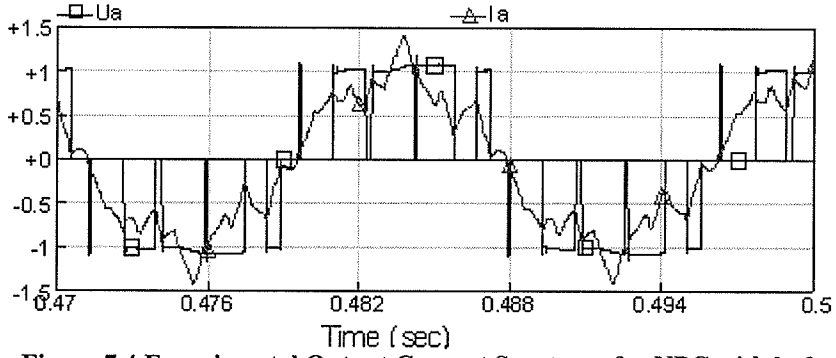

Figure 7.4 Experimental Output Current Spectrum for NPC with k=9

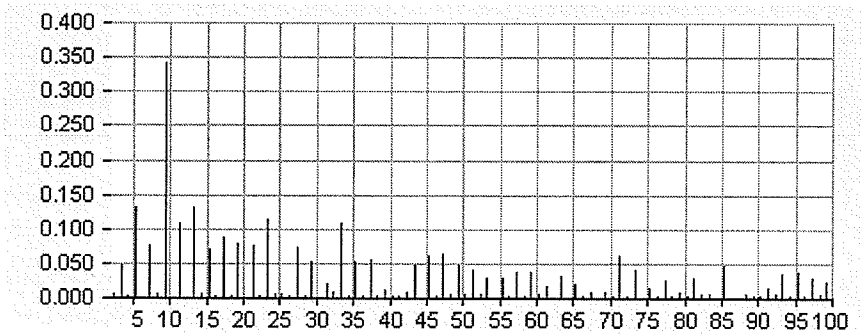

Figure 7.5 Experimental Output Voltage Spectrum for NPC with k=9

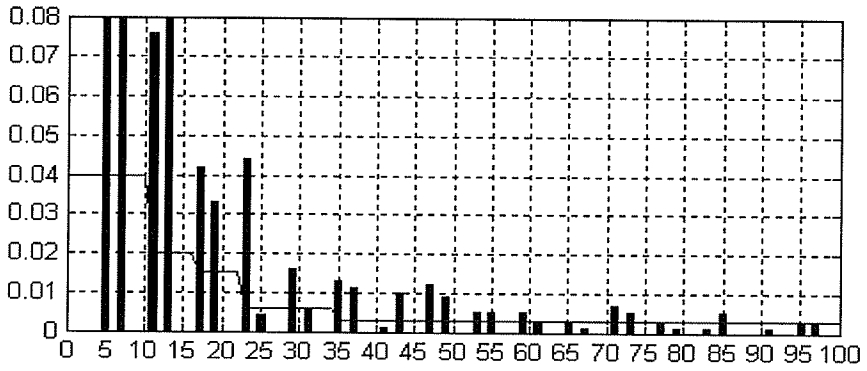

Figure 7.6 Experimental Output Current Spectrum for NPC with k=9

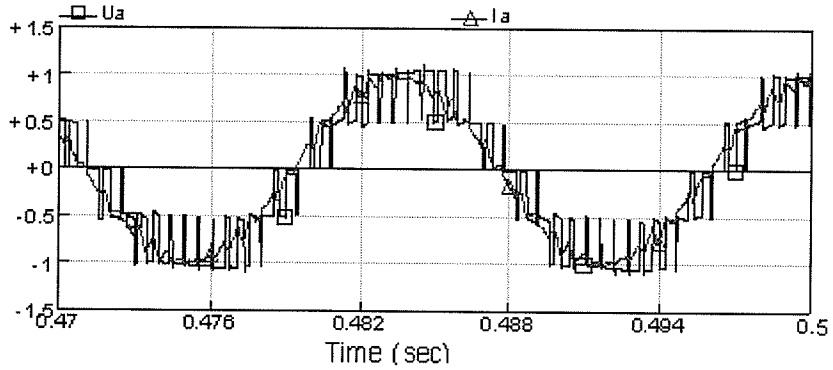

Figure 7.7 Experimental Output Voltage and Current for SMC with k=15

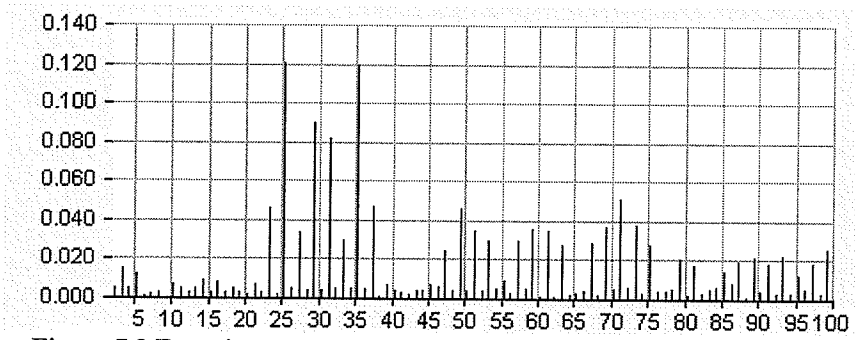

Figure 7.8 Experimental Output Voltage Spectrum for SMC with k=15

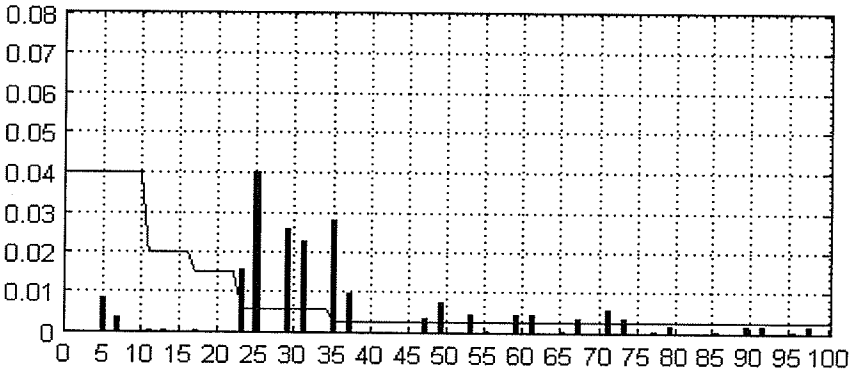

Figure 7.9 Experimental Output Current Spectrum for SMC with k=15

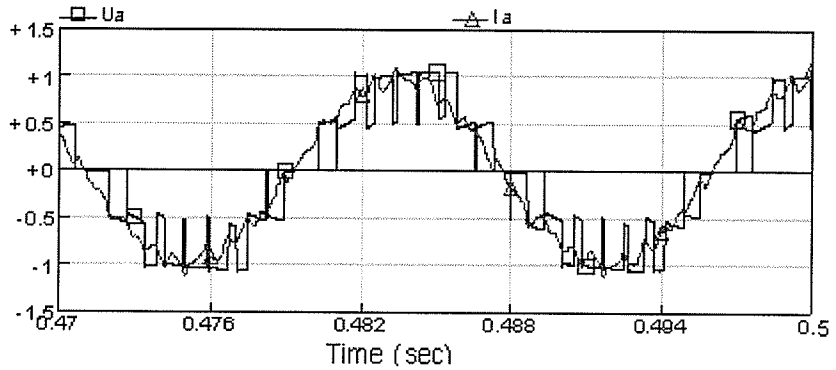

Figure 7.10 Experimental Output Voltage and Current for SMC with k=9

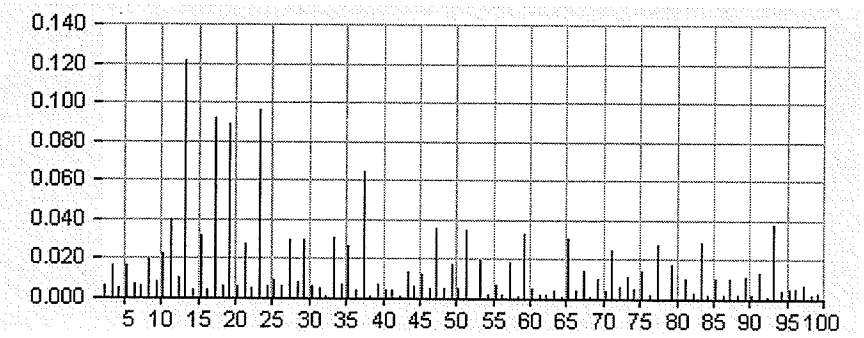

Figure 7.11 Experimental Output Voltage Spectrum for SMC with k=9

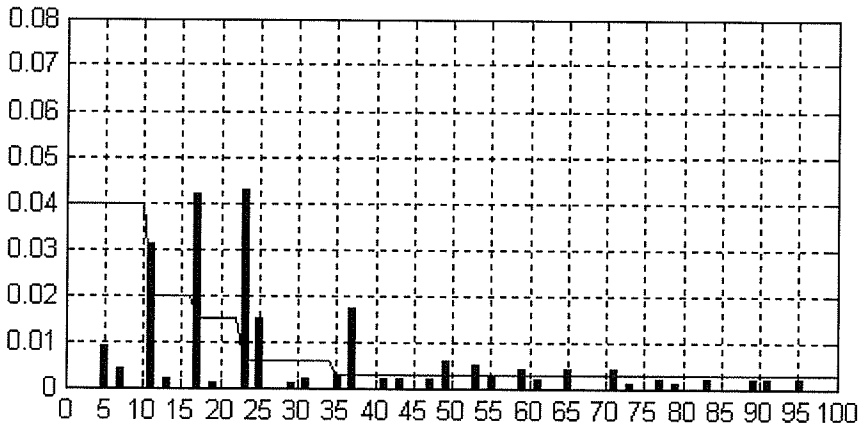

Figure 7.12 Experimental Output Current Spectrum for SMC with k=9

With respect to Tables 7.1 and 7.2 and Figures of the current spectrum, the conclusions can be given as follow:

(1) For the NPC converter, the larger frequency ratio (k=15) is always the better choice.

(2) For the SMC converter, the voltage and current total distortions are similar, but the switching losses at k=15 are much more than those at k=9. This indicates that the case for k=9 shows advantage with respect to the switching losses and output spectrum over the case for k=15. It should be noted that there is larger ripple on the floating capacitors when k=9 than that for k=15, because of the longer charging and discharging time. This ripple is possible to cause increased voltage stresses on the switching devices.

(3) The SMC converter shows advantage over the NPC converter from the aspect of output spectrum with similar switching losses when the same frequency ratio is used, especially in low frequency ratio. This is also obvious from the output current output waveform. The output waveform for the SMC converter is far more sinusoidal than that of the NPC converter.

(4) For high frequency ratio, there is little difference between the output current of the two converters in the high order harmonic spectrum of the odd harmonics, especially those that exceed the IEEE 519 Standard. But some significant differences in the low order harmonic spectrum of the odd harmonics which resulting in better waveform quality of the SMC converter over the NPC converter. For the low frequency ratio, the difference between the output current of the two converters in the harmonic spectrum of the odd harmonics is significant.

7.2 Device Stresses Comparison

The current stresses were analyzed for the operating condition of unity power factor and full dc load. With respect to Figure 6.5, the current stresses for the devices of the NPC converter can be grouped as follow:

With positive current situation, the thyristors of devices T1 carry no current at unity power factor no matter for full voltage or zero voltage. The same conclusion can obtain for the thyristors of devices T4 with negative current.

The diodes of devices T1 and T2 carry the same input current for full voltage for positive current. So do the diodes of devices T3 and T4 for negative current. The actual rms current is shown in Figure 7.13 which gives 210A. The average current is 95A.

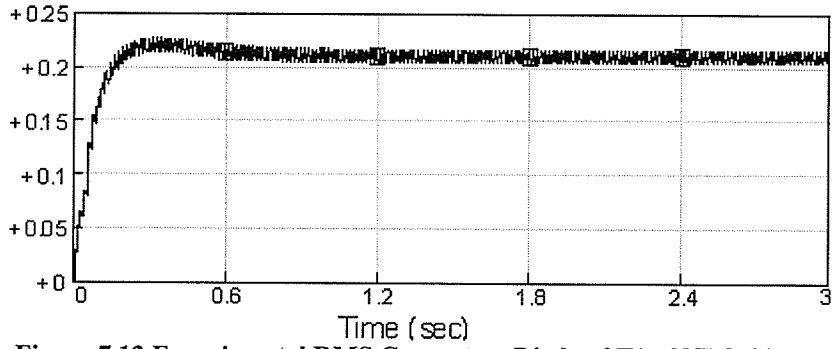

Figure 7.13 Experimental RMS Current on Diode of T1 of NPC Circuit

The thyristor of T3 and the lower clamping diode D2 carry the same current for zero voltage and positive current which are the same for the thyristor of T2 and the upper clamping diode D1 at negative current. The actual rms current is shown in Figure 7.14 which gives 105A. The average current is 47.2A.

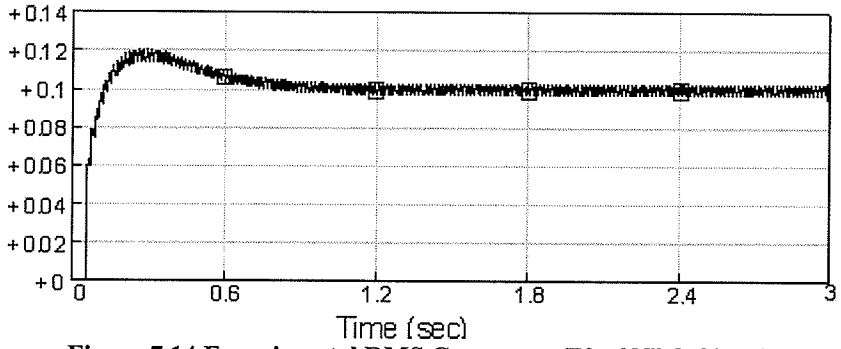

Figure 7.14 Experimental RMS Current on T3 of NPC Circuit

According to the analysis in Chapter 4, the voltage stresses are 6000V for all the devices in the NPC converter which is shown in Figure 7.15(for devices T1 and T4, but with a phase shift of π with each other) and 7.16(for devices T2 and the lower clamping diode, T3 and the upper clamping diode, but with a phase shift of π with each group), and therefore two identical devices in series are required according to the device parameter.

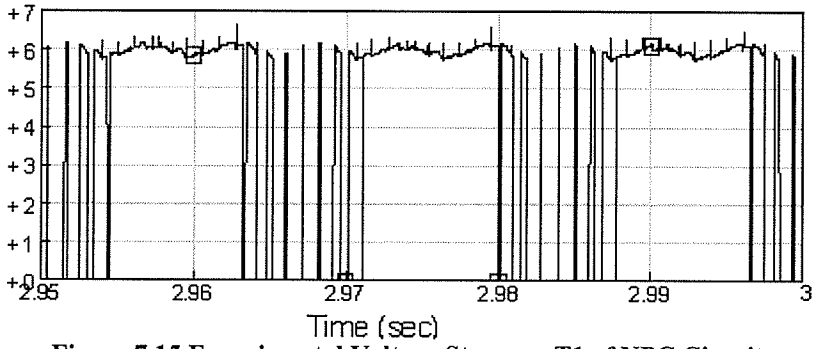

Figure 7.15 Experimental Voltage Stress on T1 of NPC Circuit

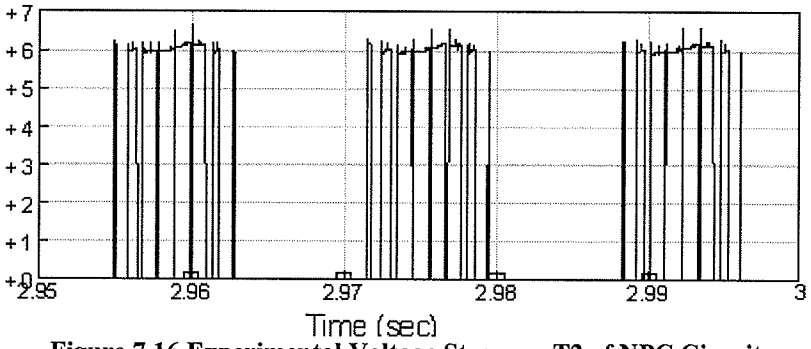

Figure 7.16 Experimental Voltage Stress on T2 of NPC Circuit

With respect to Figure 6.6, the current stresses for the devices of the SMC converter can be grouped as follow:

With positive current situation, the thyristors of devices S11T, S12T and S22T carry no input current at full and half voltage. Similarly for the thyristors of devices S12B, S11B and S21B at negative half cycle.

The diodes of devices S11T, S12T and S22T carry the same input current at positive full or half voltage. This current is shown in Figure 7.17 which is identical to Figure 7.13 for the diode of T1 in NPC converter. According to the circuit symmetry characteristic, the same rms current can obtain for the diodes of devices S12B, S11B and S21B at negative full or half voltage.

The diode of S21T, thyristors of devices S12B, S22B and the lower clamping diode carry current at positive half voltage or zero voltage. This current is shown in Figure 7.18 which is identical to

Figure 7.14 for the thyristor of T3 in NPC converter. The same rms current can obtain for the diodes of devices S22B, thyristors of devices S11T and S21T at negative half or zero voltage.

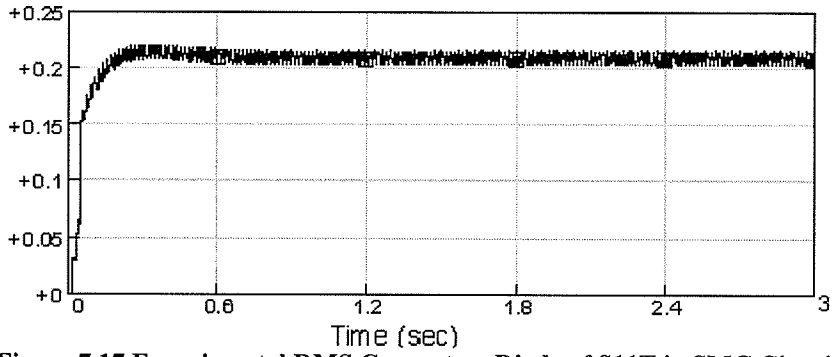

Figure 7.17 Experimental RMS Current on Diode of S11T in SMC Circuit

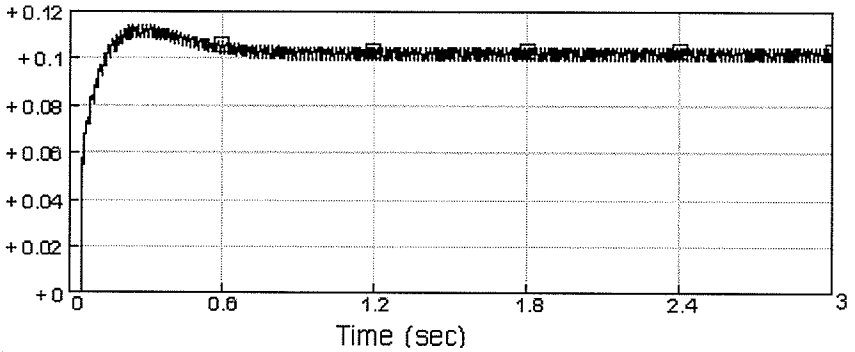

Figure 7.18 Experimental RMS Current on Thyristor of S12B in SMC Circuit

For the voltage stresses in the SMC converter, similarly, according to the analysis in Chapter 4, the voltage stresses are 3000V for the SMC devices except for S22T and S21B which are 6000V. It is noticed that these two devices do not switch while blocking 6000V and therefore one normal power thyristor and reverse conducting diode could be placed in series. As discussed in chapter 6, the floating capacitor voltages are stable at about the specified 3000V due to the use of the balance control. This also can be seen from the device voltage stresses which do not exceed their ratings in the simulation, thus proving the efficient of the designed control further. The actual voltages across the devices are shown in Figures 7.19(for device S11T and the lower clamping diode, S12B and the upper clamping diode with a phase shift of π with each group), 7.20(for devices S12T and S11B with a phase shift of π with each other), 7.21(for devices S21T, S22B

with a phase shift of π with each other) and 7.22(for devices S22T and S21B with a phase shift of π with each other).

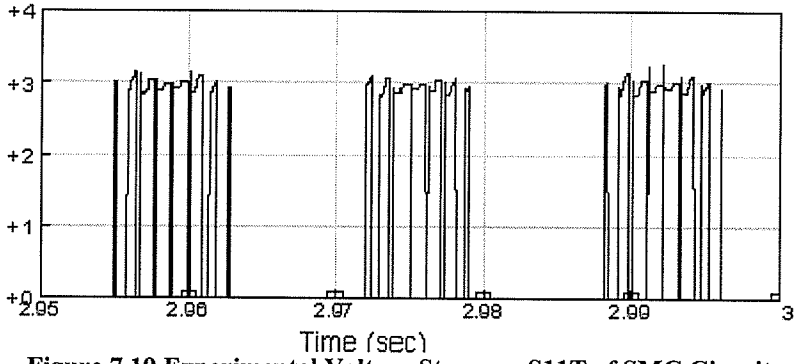

Figure 7.19 Experimental Voltage Stress on S11T of SMC Circuit

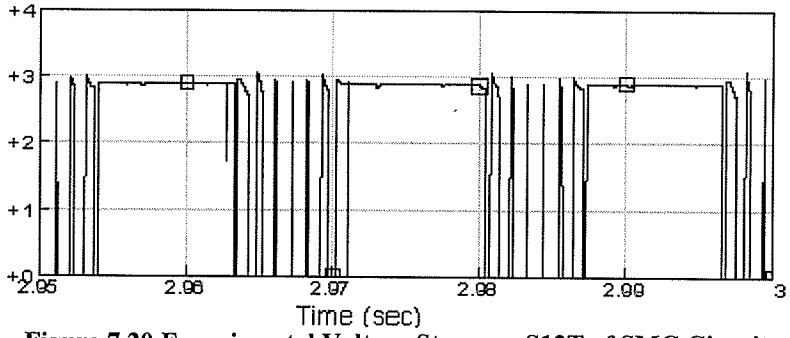

Figure 7.20 Experimental Voltage Stress on S12T of SMC Circuit

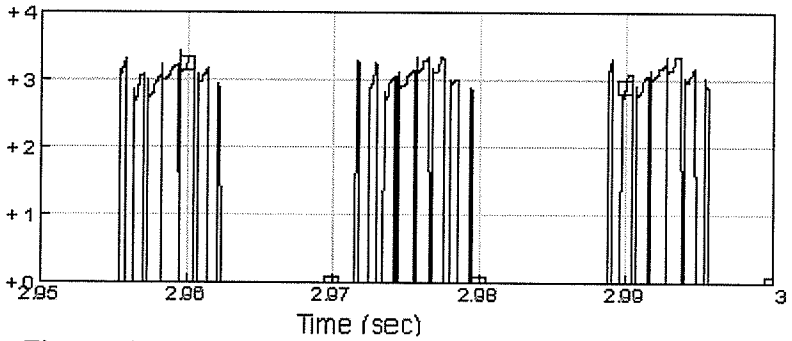

Figure 7.21 Experimental Voltage Stress on S21T of SMC Circuit

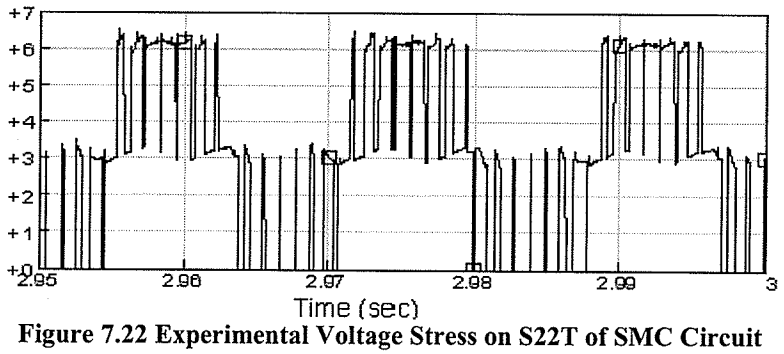

Figure 7.22 Experimental Voltage Stress on S22T of SMC Circuit

It can clearly see from the figures shown above that the device stresses are very similar. Devices S12T, S22T, S11B, S21B of the SMC converter and the upper and lower devices T1, T4 of the NPC converter carry no thyristor current. The inner devices T2, T3 of the NPC, S11T and S12B of the SMC carry an rms current of 105A which gives an average current 47.2A. This same current is carried by the clamping diode of NPC and the thyristors and diodes of S21T and S22B of the SMC. The rms diodes current of all other IGCTs is 210A which gives an average current 95A. In summary, the current stresses on the devices are far less than the stress ratings and very similar for both circuits, as are the number of switching (with and without current). The voltage stresses are also similar for the NPC and SMC converter in the specified device connection in this thesis.

7.3 Chapter Summary

In this chapter the NPC and SMC circuits using similar PWM techniques were simulated on PSCAD/EMTDC, analyzed and compared. From the circuits used in the simulation, it is easily seen that both have similar energy storage requirements for the capacitance on the dc side, but parameters of the NPC converter are twice that of the SMC converter for di/dt limiting circuit. The SMC requires additional two di/dt limiting circuits between the two cells in each phase and about 50% additional stored energy in the floating capacitors. The simulation results proved that the device stresses are essentially similar and they are switching at the same rate, so should have the same switching losses including the resistance loss in the di/dt clamping circuit. The advantage of the SMC over the NPC is in the improved output voltage and current spectrum, especially when using PWM with low frequency ratio.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

There is growing requirement for higher voltage, higher power converter systems with reduced harmonic components in their output. Several multilevel converter topologies have been developed which demonstrated superiority for various applications. The main objective of this thesis, as stated in Chapter 1, was to explore a new multilevel converter, the Stacked Multicell Converter (SMC) and to compare it with an existing three-level NPC converter which has found many applications in industry. After a brief investigation of the configuration and operation principle of the NPC and the SMC converters, detailed design and analysis are carried out based on a three-level NPC and a five-level 2x2 SMC.

The three-level NPC converter is widely used in high power industrial applications due to its high voltage handling and good harmonic rejection capabilities with the currently available power electronics devices. Higher level diode clamped converters will produce less distortion and better output quality, but balancing the capacitor voltage at each level becomes a problem. Employing additional regulation circuitry can solve the problem, but has not met with industrial acceptance.

The SMC topology is a new structure of multilevel converter which uses a hybrid association of commutation cells making it possible to share the voltage constraint on several switches, and also improve the output waveforms of the converter in terms of levels and switching frequency.

The PWM technique was chosen to be used in the simulation due to its simplicity, fast response and small ripple on the capacitors. Both circuits were analyzed using the PWM techniques in theory. After a lot of calculation and analysis work was carried out, it is concluded that the five-level SMC has advantage over the three-level NPC in a lower total harmonic distortion no matter what kind of PWM switching technique was used.

The overall control system for both circuits can be the same as those of conventional two-level converter. The dc capacitors and the floating capacitors in both circuits can be pre-charged through the reverse diode conduction from the ac system. It is concluded that good control response can be obtained by using vector control in dq coordinates. However, the floating capacitor voltage would drift using standard PWM techniques. A main contribution of this thesis was to develop a new control algorithm which can stabilize and balance the floating capacitor voltage at the required normal value. This technique was shown to work well over all operating ranges.

The final simulation results are extremely compatible with the theoretical results. It is indicated that the voltage and current stresses on the devices were very similar as well as the number of the devices required. Both have similar energy storage requirements on the dc side, but the SMC needs 2 additional current limiting circuits and floating capacitors which have 50% additional stored energy between the two cells in one phase. The advantage of the SMC over the NPC is the better quality of the output voltage and current spectrum which indicates that the SMC is a good candidate for high-voltage and high-power applications.

8.2 Future work

This thesis provided a feasible method to stabilize and balance the floating capacitor voltages which works well for the sinusoidal PWM. Similar techniques would have to be developed for optimal pulse pattern method. Additionally, filter design to get better output spectrum which meets the IEEE 519 Standard will have to be developed.

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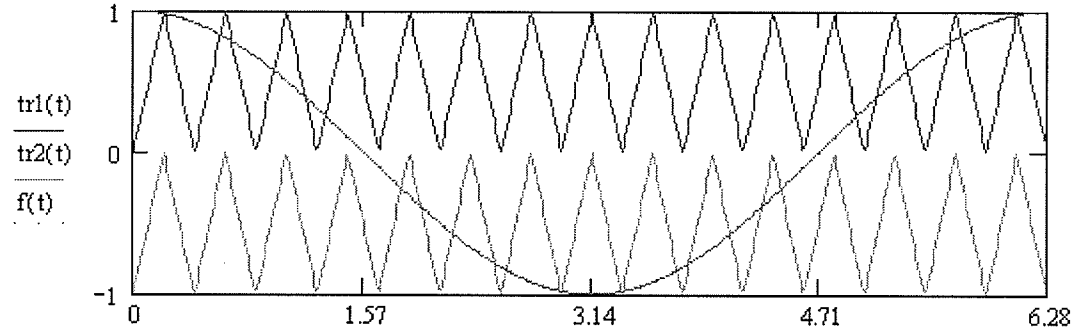
APPENDIX A

SHPWM Technique for Three-level NPC Converter

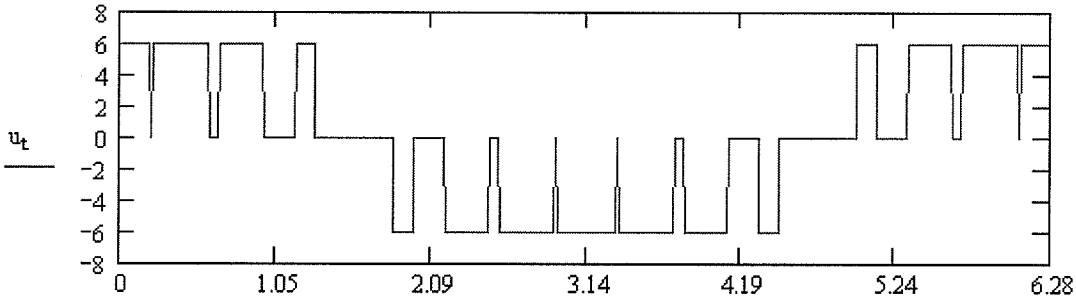
$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 15$ $E := 6$

$$tr0(t) := \frac{\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi} \qquad tr(t) := \frac{-1\cdot\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$$

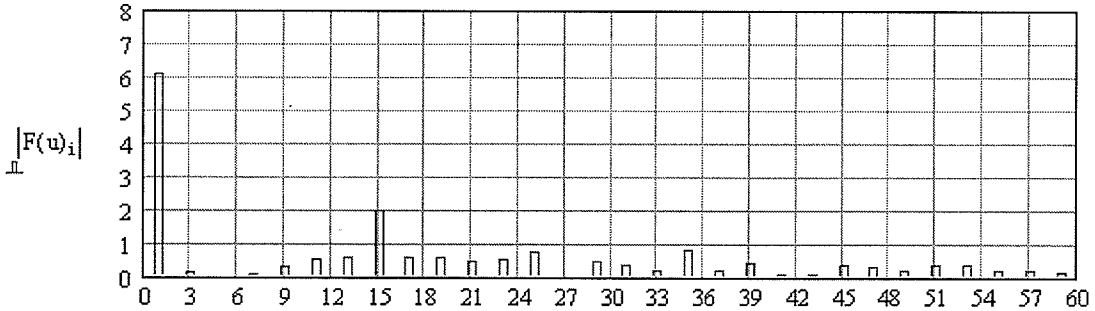
$tr1(t) := 0.5 + tr0(t)$ $tr2(t) := -0.5 + tr0(t)$ $f(t) := m\cdot\cos(\omega\cdot t)$



$u1(t) := \Phi(f(t) - tr1(t))$ $u2(t) := \Phi(tr2(t) - f(t))$ $u_t := E\cdot(u1(t) - u2(t))$



$i := 0..60$ $F(u) := \frac{2j}{\sqrt{512}}(\mathrm{fft}(u) - 2j\cdot\mathrm{Im}(\mathrm{fft}(u)))$



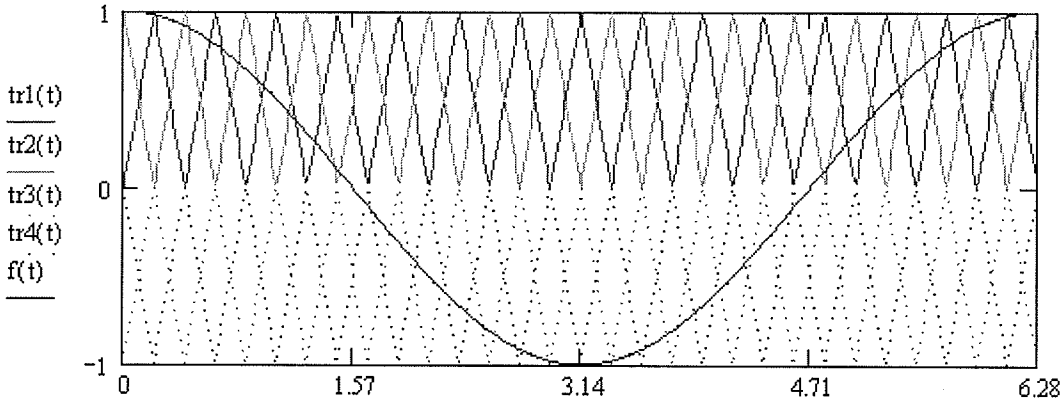
$p := 5,11..60$ $q := 7,13..60$ $DF := \frac{\sqrt{\left[\sum_p \left(|F(u)_p|\right)^2\right] + \sum_q \left(|F(u)_q|\right)^2}}{|F(u)_1|}$ $DF = 0.307$

SHPWM Technique for Five-level SMC Converter

$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 15$ $E := 3$

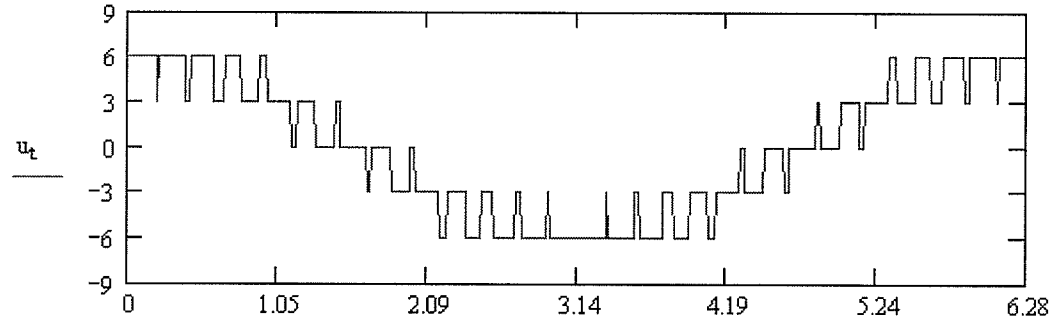
$$tr0(t) := \frac{\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi} \qquad tr(t) := \frac{-1\cdot\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$$

$tr1(t) := 0.5 + tr0(t)$ $tr2(t) := 0.5 + tr(t)$ $tr3(t) := -0.5 + tr0(t)$ $tr4(t) := -0.5 + tr(t)$ $f(t) := m\cdot\cos(\omega\cdot t)$

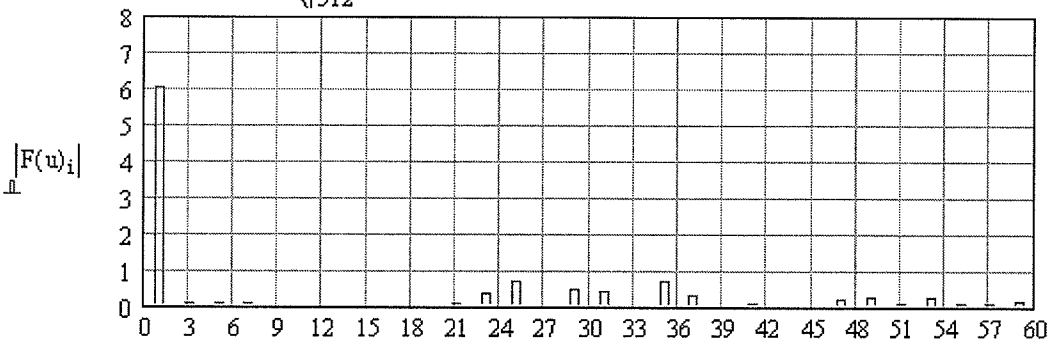


$u1(t) := \Phi(f(t) - tr1(t))$ $u2(t) := \Phi(f(t) - tr2(t))$ $u3(t) := \Phi(tr3(t) - f(t))$ $u4(t) := \Phi(tr4(t) - f(t))$

$u_t := E\cdot(u1(t) + u2(t) - u3(t) - u4(t))$



$i := 0..60$ $F(u) := \frac{2j}{\sqrt{512}}(\mathrm{fft}(u) - 2j\cdot\mathrm{Im}(\mathrm{fft}(u)))$



$p := 5,11..60$ $q := 7,13..60$ $DF := \frac{\sqrt{\left[\sum_p \left(|F(u)_p|\right)^2\right] + \sum_q \left(|F(u)_q|\right)^2}}{|F(u)_1|}$ $DF = 0.217$

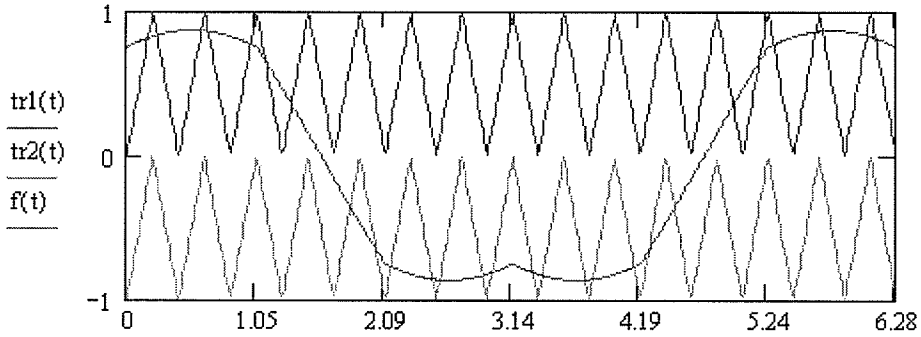
SFOPWM Technique for Three-level NPC Converter

$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 15$ $E := 6$

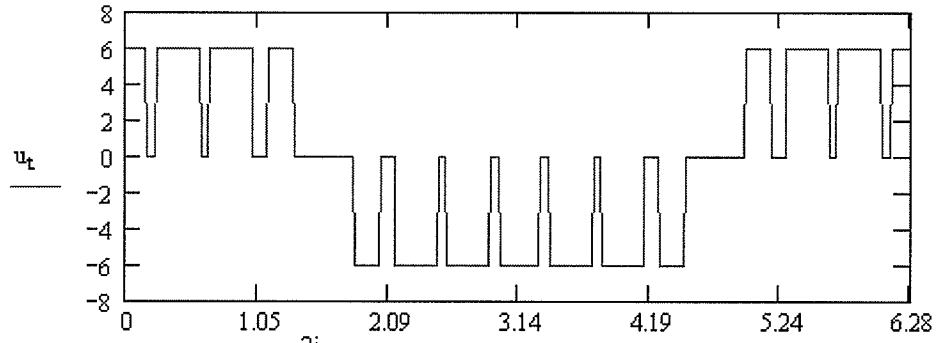
$tr0(t) := \frac{\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$ $tr(t) := \frac{-1\cdot\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$ $fr(t) := \begin{pmatrix} m\cdot\cos(\omega\cdot t) \\ m\cdot\cos\left(\omega\cdot t - \frac{2\pi}{3}\right) \\ m\cdot\cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix}$

$tr1(t) := 0.5 + tr0(t)$ $tr2(t) := -0.5 + tr0(t)$ $f1(t) := m\cdot co$

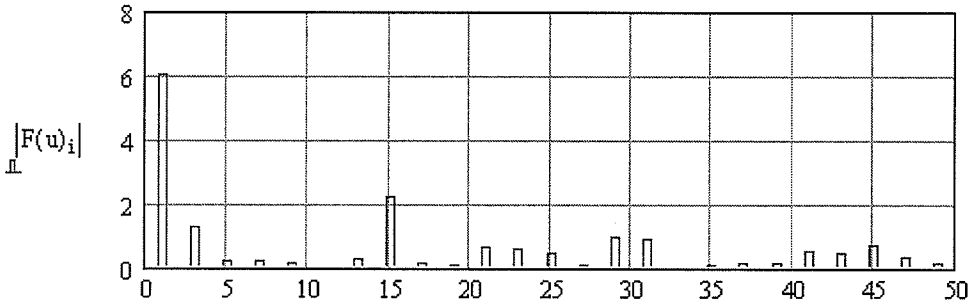
$f0(t) := \frac{\max(fr(t)) + \min(fr(t))}{2}$ $f(t) := f1(t) - f0(t)$



$u1(t) := \Phi(f(t) - tr1(t))$ $u2(t) := -\Phi(tr2(t) - f(t))$ $u_t := E\cdot(u1(t) + u2(t))$



$i := 0..50$ $F(u) := \frac{2j}{\sqrt{512}}(\mathrm{fft}(u) - 2j\cdot\mathrm{Im}(\mathrm{fft}(u)))$



$p := 5,11..60$ $q := 7,13..60$ $DF := \frac{\sqrt{\left[\sum_p \left(|F(u)_p|\right)^2\right] + \sum_q \left(|F(u)_q|\right)^2}}{|F(u)_1|}$ $DF = 0.303$

SFOPWM Technique for Five-level SMC Converter

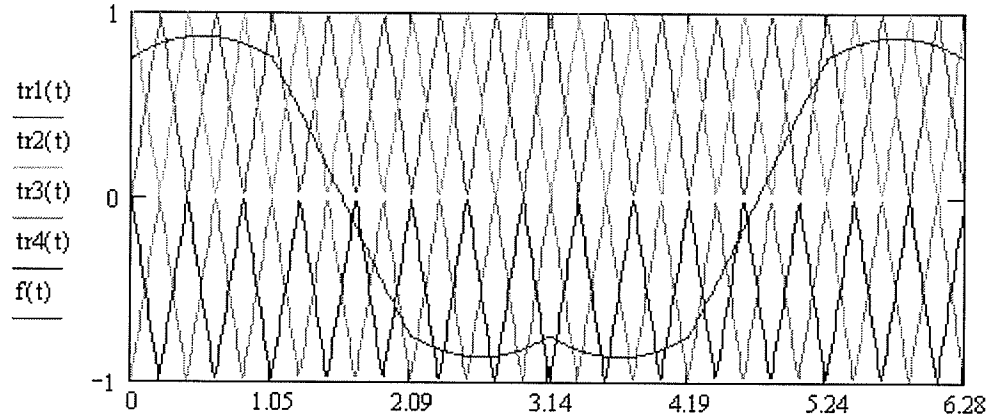
$\omega := \frac{\pi}{256}$ $t := 0..511$ $m := 1$ $k := 15$ $E := 3$

$tr0(t) := \frac{\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$ $tr(t) := \frac{-1\cdot\operatorname{asin}\left(\sin\left(k\cdot\omega\cdot t - \frac{\pi}{2}\right)\right)}{\pi}$ $fr(t) := \begin{pmatrix} m\cdot\cos(\omega\cdot t) \\ m\cdot\cos\left(\omega\cdot t - \frac{2\pi}{3}\right) \\ m\cdot\cos\left(\omega\cdot t + \frac{2\pi}{3}\right) \end{pmatrix}$

$tr1(t) := 0.5 + tr0(t)$ $tr2(t) := 0.5 + tr(t)$ $f1(t) := m\cdot\cos(\omega\cdot t)$

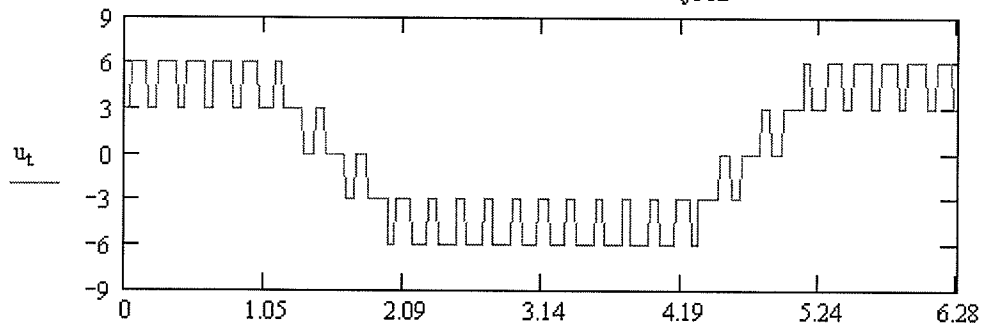
$tr3(t) := -0.5 + tr0(t)$ $tr4(t) := -0.5 + tr(t)$

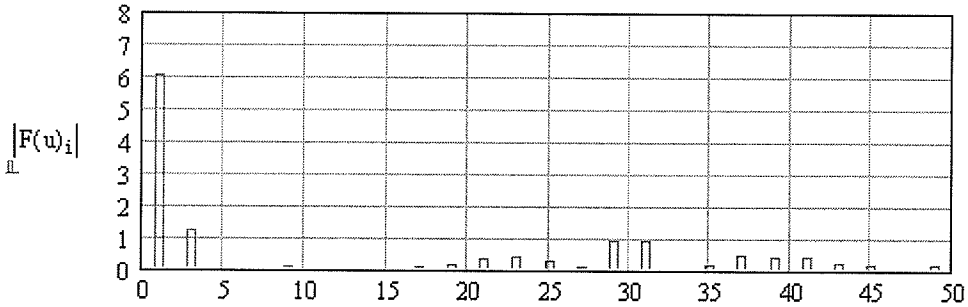
$f0(t) := \frac{\max(fr(t)) + \min(fr(t))}{2}$ $f(t) := f1(t) - f0(t)$



$u1(t) := \Phi(f(t) - tr1(t))$ $u2(t) := \Phi(f(t) - tr2(t))$ $u3(t) := -\Phi(tr3(t) - f(t))$ $u4(t) := -\Phi(tr4(t) - f(t))$

$u_t := E\cdot(u1(t) + u2(t) + u3(t) + u4(t))$ $i := 0..50$ $F(u) := \frac{2j}{\sqrt{512}}(\mathrm{fft}(u) - 2j\cdot\mathrm{Im}(\mathrm{fft}(u)))$





$p := 5,11..60$ $q := 7,13..60$ $DF := \frac{\sqrt{\left[\sum_p \left(|F(u)_p|\right)^2\right] + \sum_q \left(|F(u)_q|\right)^2}}{|F(u)_1|}$ $DF = 0.273$

APPENDIX B

V_{DClink}: Permanent DC voltage for 100 FIT failure rate

I_{TAVM}: Max. average on-state current for GCT

I_{TRMS}: Max. RMS on-state current for GCT

V_T: On-state voltage for GCT

V_{T0}: Threshold voltage for GCT

r_T: Slope resistance for GCT

di/dt: Max. rate of rise of on-state current

I_{FAVM}: Max. average on-state current for diode

I_{FRMS}: Max. RMS on-state current for diode

V_F: On-state voltage for diode

V_{F0}: Threshold voltage for diode

r_F: Slope resistance for diode

The Device Parameters in the Circuit

5SHX 10H6004				5SDF 04F6004	
GCT		Reverse diode			
V_{DClink}		3300V		V_{DClink}	3300V
I_{TAVM}	355A	I_{FAVM}	165A	I_{FAVM}	380A
I_{TRMS}	555A	I_{FRMS}	260A	I_{FRMS}	600A
V_T	≤3.45V	V_F	≤6.4V	V_F	≤5.2V
V_{T0}	1.65V	V_{F0}	2.53V	V_{F0}	2.7V
r_T	2mΩ	r_F	4.3mΩ	r_F	2.8mΩ
di/dt	340A/μs	di/dt	340A/μs	di/dt	340A/μs

APPENDIX C

The Parameters of the Control System

The Detail Parameters of Controls

PI Regalator	Proportional Gain	Time Constant(ms)
Phase Locked Loop	60	60
DC Voltage Control	0.1	90
dq Current Control	0.1	90

Low Pass Filter	Gain	Damping Ratio	Cut-off Frequency
DC Voltage	1	0.7	50
dq Current	1	0.7	150

APPENDIX D

IEEE 519 Standard

Harmonic Current Limits for Non-Linear Load at the Point-of-Common-Coupling with Other Loads, for Voltages 120-69,000 volts

Maximum Odd Harmonic Current Distortion in % of Fundamental Harmonic Order

I_{sc}/I_L	<11	11≤h<17	17≤h<23	23≤h<35	35≤h	TDD
<20*	4	2	1.5	0.6	0.3	5
20<50	7	3.5	2.5	1	0.5	8
50<100	10	4.5	4	1.5	0.7	12
100<1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20

*All power generation equipment is limited to these values of current distortion, regardless of actual Isc/I_L.
Where Isc=Maximum short circuit current at point-of-common-coupling.
And IL=Maximum demand load current (fundamental frequency) at point of common coupling.
TDD=Total demand distortion (RSS) in % of maximum demand, is the equivalent of THD for the voltages.