Research on Modern Power Semiconductor Modelling Methodology for Efficiency Evaluation of Power Electronic Systems in Electromagnetic Transient Simulation

by

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Abstract

Power electronics technology has rapidly developed during the past decades. Power electronics systems aim to achieve high efficiency as power conversion interfaces while fulfilling the performance and reliability requirements. The key to achieving these objectives is power semiconductors, which dictate the power electronics system's efficiency, power density, and reliability. In recent years, traditional Silicon (Si) devices are reaching their material limits. Meanwhile, new Wide-Bandgap (WBG) devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) devices have been commercialized, featuring high breakdown voltage, fast switching speed, and high thermal capability. On the other hand, semiconductor devices are typically exposed to repetitive heat pulses and are often the most critical components affecting system reliability. Consequently, a comprehensive modelling method for modern power semiconductors that can describe various devices' switching behaviors is highly desirable by power electronics engineers and manufacturers.

This research focuses on developing a simulation-based modelling methodology for modern power semiconductors to evaluate the power electronics system's efficiency. A multi-level simulation strategy has been proposed and implemented in PSCAD/EMTDC. A generalized transient semiconductor model has been developed, which can reproduce the device's switching behaviors. Subsequently, the power losses are obtained to form a multi-dimensional power loss look-up table under a wide range of operating conditions.

A dynamic thermal model for temperature estimation, and a typical electrical network using simple switch models for semiconductor devices have been implemented. The junction temperature is updated every switching cycle by the power loss with a thermal model and influence back to the electrical simulation. In this way, a closed-loop electro-thermal simulation is formed to evaluate both electrical and thermal performances in a single simulator with a range of acceptable accuracy. A double pulse test platform has been designed and built for device characterizations and power loss verifications. Moreover, a single-phase grid-tied buck-boost type inverter application has been selected as a case study and built to study the proposed method. The measured results indicate that the proposed approach is highly promising for power electronics engineers to evaluate and optimize a system during the early design stage.

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Dedication

“To my loving parents, Mr. Fuliang Xu and Ms. Tuying Ding, as well as my supportive sister, Wenyan Xu!”

Table of Contents

List of Tables

List of Figures

Nomenclature

List of Symbols

A_{cu}	Cross-sectional area of copper wire
A_{e}	Cross-sectional area of the core
A_{L}	Minimum inductance factor
A_{w}	Window area of core
a	Geometric parameter of AMCC core
a_{core}	Core loss fitting coefficient
B_{max}	Maximum flux density
B_{pk}	AC flux swing
ΔB	AC flux ripple
b	Geometric parameter of AMCC core
b_{core}	Core loss fitting coefficient
C_{A}	Capacitance between the grid and DC link in a PV inverter
C_{B}	Output load capacitance
C_{CM}	Equivalent common mode capacitor in a PV inverter
C_{ce}	Collector-emitter capacitance
C_{D}	Equivalent diode capacitance
C_{DC}	DC link capacitance in a PV inverter
C_{ds}	Drain-source capacitance
C_{F}	Equivalent forward capacitance
C_{gc}	Gate-collector capacitance
C_{gd}	Gate-drain capacitance

C_{ge}	Gate-emitter capacitance
C_{gs}	Gate-source capacitance
C_{hv}	Parasitic capacitance at a high-voltage range
C_{in}	Input source capacitance
C_{iss}	Input parasitic capacitance
C_{o}	Output DC capacitance in PFC
C_{oss}	Output parasitic capacitance
C_{rss}	Reverse parasitic capacitance
$C_{\mathrm{th}i}$	General thermal capacitance
$C_{\mathrm{thC}i}$	Cauer-type thermal capacitance
$C_{\mathrm{thF}i}$	Foster-type thermal capacitance
c_{core}	Core loss fitting coefficient
D	Duty cycle
D_1	Diode associated with a high-frequency switch
D_2	Diode associated with a high-frequency switch
D_3	Diode associated with a line-frequency switch
D_4	Diode associated with a line-frequency switch
D_{F}	Ideal diode
D_{H}	High-side diode
d	Geometric parameter of the AMCC core
$\mathrm{d}i_{\mathrm{F}}/\mathrm{d}t$	Slew rate of the diode current
E_{F}	Diode capacitive energy loss
E_{irr}	Diode reverse recovery loss
E_{off}	Turn-off energy loss

E_{offi}	Turn-off current loss
E_{offm}	Measured turn-off loss
E_{offv}	Turn-off voltage loss
E_{on}	Turn-on energy loss
E_{oni}	Turn-on current loss
E_{onm}	Measured turn-on loss
E_{onv}	Turn-on voltage loss
E_{oss}	Output capacitive energy loss
E_{tail}	Turn-off tail current loss
E_{ts}	Total energy loss
E_{vioff}	Turn-off V-I overlap energy loss
E_{vion}	Turn-on V-I overlap energy loss
$\bar{\mathrm{e}}$	Average error
$\mathrm{f}(t)$	Voltage function in the switching function model
f_{sw}	Switching frequency
$\mathrm{g}(t)$	Current function in the switching function model
g_{fs}	Trans-conductance
ΔH	AC magnetizing field ripple
I_{cav}	Average conduction current
I_{crms}	RMS of the conduction current
I_{G}	Amplitude of the grid current
I_{L}	Inductive load current
I_{max}	Maximum device current
I_{rm}	Diode reverse recovery peak current

I_{rm0}	Fitting constant of diode reverse recovery peak current
I_{tail0}	IGBT initial tail current
i_{CF}	Parasitic capacitive current
i_{CM}	Leakage current
i_{c}	IGBT collector current
i_{ch}	Conductive channel current
i_{DC}	DC link current
i_{d}	Forward drain current
i_{ds}	drain-source current
i_{F}	Diode forward current
i_{G}	AC grid current
i_{g}	Gate current
i_{gd}	Gate-drain current
i_{IGBT}	IGBT equivalent current
i_{ins}	Input current in the switching function model
i_{L}	Instantaneous inductor current
i_{L1}	Current flowing through the inductor L_1
i_{L2}	Current flowing through the inductor L_2
i_{Lmax}	Maximum RMS inductor current
Δi_{L}	Inductor current ripple
Δi_{Lmax}	Maximum inductor current ripple
i_{mos}	MOS channel equivalent current
i_{oss}	Capacitive current
i_{outs}	Output current in the switching function model

i_{re}	Diode reverse recovery current
i_{S}	Equivalent current source
i_{s}	Input source current
i_{tail}	IGBT tail current
K_{IGBT}	Equivalent trans-conductance of IGBT
K_{Qrr}	Fitting constant of diode reverse recovery charge
K_{rm}	Fitting constant of diode reverse recovery peak current
K_{rr}	Fitting constant of diode reverse recovery charge
K_{trm}	Fitting constant of diode reverse recovery peak current
K_0	Fitting constant of trans-conductance of IGBT
k_{a}	Fitting constant for transfer curve
k_{b}	Fitting constant for transfer curve
k_{ca}	Fitting constant for parasitic capacitance
k_{cb}	Fitting constant for parasitic capacitance
k_{cc}	Fitting constant for parasitic capacitance
k_{cd}	Fitting constant for parasitic capacitance
k_{cea}	Fitting constant for on-state voltage
k_{ceb}	Fitting constant for on-state voltage
k_{cu}	Copper filling factor
k_{ga}	Fitting constant for trans-conductance
k_{gb}	Fitting constant for trans-conductance
k_{gTa}	Temperature-dependent fitting constant for trans-conductance
k_{gTb}	Temperature-dependent fitting constant for trans-conductance
k_{ona}	Fitting constant for on-state resistance

k_{onb}	Fitting constant for on-state resistance
k_{R}	Fitting constant for on-state resistance
k_{T}	Fitting constant for threshold voltage
k_{Ta}	Fitting constant for threshold voltage
k_{Tb}	Fitting constant for threshold voltage
k_{Tc}	Fitting constant for threshold voltage
L_1	Inductor in the PE converter
L_2	Inductor in the PE converter
L_{B}	Boost converter Inductance
L_{cs}	Common source parasitic inductance
L_{S}	Stray parasitic inductance
l	Length of wire
l_{g}	Air gap length
l_{e}	Magnetic path length
l_{i}	Inner perimeter of the toroid core
l_{o}	Outer perimeter of the toroid core
MTL	Mean turn length
m_{L}	Core weight
N	Number of turns
N_{max}	Maximum number of turns
N_{min}	Minimum number of turns
P_{CS}	Conduction power loss of the capacitive switch
P_{CHF}	Conduction power loss of the HF switch
P_{CLF}	Conduction power loss of the LF switch

P_{t}	Total power dissipation
p_{avgt}	Instantaneous average power loss
p_{con}	Conduction loss power
p_{core}	Core loss power
p_{cu}	Conduction power of copper wire
p_{ld}	Core loss density
p_{S}	Instantaneous power of active switch
p_{total}	Total inductor loss
p_{ts}	Instantaneous total power loss
Q_{F}	Diode equivalent charge
Q_{rr}	Diode reverse recovery charge
Q_{rr0}	Fitting constant of diode reverse recovery charge
R_{AC}	AC resistance of a conductor
R_{B}	Output load resistance
R_{D}	Diode on-state resistance
R_{DC}	DC resistance of a conductor
$R_{\mathrm{DS(on)}}$	Drain-source on-state resistance
R_{Fr}	GaN device on-state resistance in the third quadrant
R_{G}	Total gate resistance
R_{gext}	External gate resistance
R_{gint}	Internal gate resistance
R_{o}	Output load resistance
R_{on}	General on-state resistance
$R_{\mathrm{th}i}$	General thermal resistance

$R_{\mathrm{thC}i}$	Cauer-type thermal resistance
$R_{\mathrm{thF}i}$	Foster-type thermal resistance
r	Radius of the conductor
r_0	Fitting constant for IGBT on-state voltage
Δr_0	Fitting constant for IGBT on-state voltage
r_{c}	Equivalent on-state resistance of IGBT
r_{cea}	Fitting constant for on-state voltage
r_{ceb}	Fitting constant for on-state voltage
r_{ona}	Fitting constant for on-state resistance
r_{onb}	Fitting constant for on-state resistance
S_1	High-frequency switch in PFC
S_2	High-frequency switch in PFC
S_3	Low-frequency switch in PFC
S_4	Low-frequency switch in PFC
S_{A}	Positive capacitive switch
S_{A1}	Back-to-back positive capacitive switch
S_{A2}	Back-to-back positive capacitive switch
S_{B}	Negative capacitive switch
S_{B1}	Back-to-back negative capacitive switch
S_{B2}	Back-to-back negative capacitive switch
S_{C}	Low voltage capacitive switch
S_{H}	High-side switch
S_{HF}	High-voltage high switching frequency switch
S_{L}	Low-side switch

S_{LF}	High-voltage line switching frequency switch
T_{a}	Ambient temperature
T_{c}	Case temperature
T_{C}	Switching period
T_{j}	Device junction temperature
T_{max}	Maximum operating temperature
T_{off}	Off-state period
T_{on}	On-state period
t_{doff}	Turn-off delay time
t_{don}	Turn-on delay time
t_{f}	Current falling time
t_{offi}	Turn-off current time interval
t_{offv}	Turn-off voltage time interval
t_{oni}	Turn-on current time interval
t_{onv}	Turn-on voltage time interval
t_{Qrr}	Fitting constant of diode reverse recovery charge
t_{r}	Current rising time
t_{re}	Diode reverse recovery starting time
t_{rm}	Diode reverse recovery peak time
t_{rm0}	Fitting constant of diode reverse recovery peak current
t_{rr}	Diode reverse recovery time
t_{tail}	IGBT current tailing time
$t_{0\sim9}$	Switching time interval
V_{ce0}	On-state threshold voltage

V_{cesat0}	Fitting constant of IGBT on-state threshold voltage
$\Delta V_{\mathrm{cesat0}}$	Fitting constant of IGBT on-state threshold voltage
V_{dd}	Circuit voltage
V_{goff}	Turn-off gate drive voltage
V_{gon}	Turn-on gate drive voltage
V_{L}	Core volume
V_{ov}	Turn-off overvoltage
V_{T0}	Fitting constant for threshold voltage
v_{BD}	Diode reverse breakdown voltage
v_{CM}	Common mode voltage in PV inverter
v_{CS}	Forward voltage drop of the capacitive switch
Δv_{C}	Capacitance voltage ripple
v_{ce}	IGBT collector-emitter voltage
v_{cesat}	IGBT on-state saturation voltage
v_{D0}	Diode threshold voltage
v_{DC}	DC output voltage of PV array
v_{ds}	Drain-source voltage
v_{F}	Diode forward voltage
v_{G}	AC grid voltage
v_{GF}	Gate drive voltage of a diode
v_{g}	Gate drive voltage
v_{gd}	Gate-drain voltage
v_{ge}	IGBT gate-emitter voltage
v_{gs}	Gate-source voltage

v_{HF}	Forward voltage drop of the high-frequency switch
v_{IGBT}	IGBT equivalent voltage
v_{ins}	Input voltage in the switching function model
v_{L}	Voltage drop of stray inductance
v_{Lcs}	Equivalent voltage of common-source inductance
v_{LF}	Forward voltage drop of the line-frequency switch channel
v_{LFD}	Forward voltage drop of the line-frequency switch diode
v_{mil}	Miller plateau equivalent voltage
v_{mos}	MOS equivalent voltage
v_{o}	Output load voltage
v_{on}	General on-state voltage
v_{outs}	Output voltage in switching function model
v_{S}	Equivalent voltage source
v_{s}	Input source voltage
v_{sd}	Source-drain voltage
v_{T}	Threshold voltage
v_{thF}	GaN device threshold voltage in the third quadrant
Z_{jc}	Thermal impedance from junction to case
α_{20}	Copper temperature coefficient @20℃
β	Current gain of BJT
ρ	Resistivity of conductor
ρ_{20}	Copper resistivity @20℃
δ	Skin depth
μ	Permeability of material

μ_0	Permeability of air
τ_{g}	Gate charge time constant
τ_{iss}	Input charging time constant
τ_{re}	Diode reverse recovery decay time constant
τ_{tail}	IGBT carrier transit time constant
$\tau_{\mathrm{thF}i}$	Foster-type thermal time constant

List of Abbreviations

1-D	One-dimensional
2-D	Two-dimensional
2DEG	Two-Dimensional Electron Gas
A	Anode
AMCC	Amorphous Metal C-Core
AWG	American Wire Gauge
BJT	Bipolar Junction Transistor
C	Collector terminal
CM	Common-Mode
D	Drain terminal
DPT	Double Pulse Test
DSP	Digital Signal Processing
DUT	Device Under Test
E	Emitter terminal
EMT	Electromagnetic transient
EPC	Efficient Power Conversion Corporation
ETM	Electro-thermal model
EV	Electric vehicle
eGaN	Enhancement mode Gallium Nitride
FB	Full-bridge
FDM	Finite-Difference Method
FEM	Finite Element Method
FPGA	Field-Programmable Gate Array

G	Gate terminal
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
HF	High-frequency
IGBT	Insulated-Gate Bipolar Transistor
K	Cathode
kW	Kilowatts
L	Line terminal of grid
LED	Light-Emitting Diodes
LF	Line frequency
LUT	Look-Up Table
MBI	Manitoba inverter
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MW	Megawatts
ms	Millisecond
N	Neutral terminal of grid
ns	Nanosecond
PCB	Printed Circuit Board
PE	Power Electronics
PFC	Power Factor Correction
PV	Photovoltaics
RC	Resistance and capacitance
RF	Radio frequency

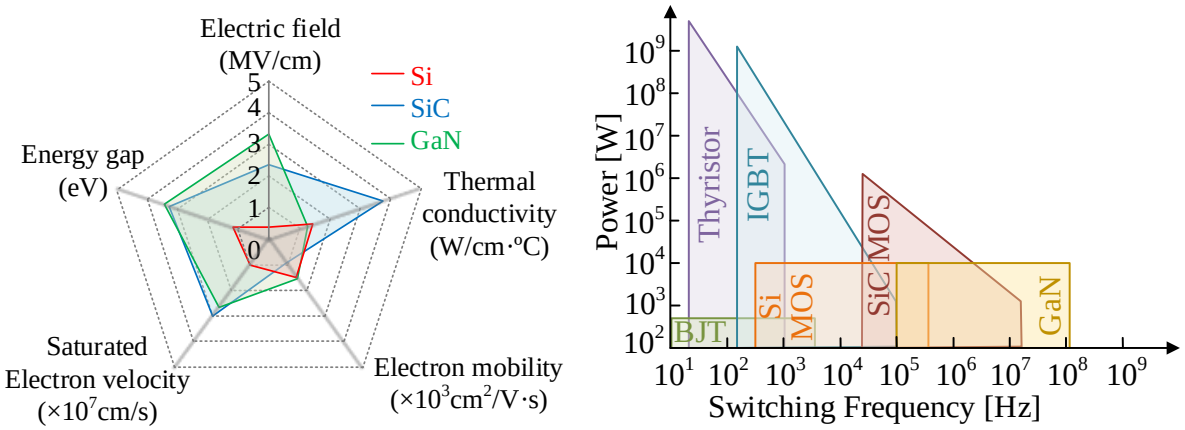
S	Source terminal
SBD	Schottky Barrier Diode
SD	Switch-diode
Si	Silicon
SiC	Silicon Carbide
SMD	Surface-mount device
TIM	Thermal interface material
TSEP	Thermo-Sensitive Electrical Parameter
WBG	Wide-Bandgap
µs	Microsecond

Chapter 1 Introduction

1.1. Background

Electrical energy is the main medium for storing, transmitting, and utilizing energy in modern society. Power Electronics (PE) system allows efficient electrical energy processing and plays a crucial role in its generation-storage-distribution cycle [1]. It also facilitates evolutions of the way of using energy in our daily life, e.g., from light bulbs to Light-Emitting Diode (LED) lighting, from centralized power generation to decentralized renewable energy power supplies, from gasoline cars to electric vehicles (EVs). The most considerable portion of the power losses in a PE system is dissipated in power semiconductor devices, limiting the switching frequency, system efficiency, power density, and reliability. Currently, commercial power semiconductors are dominated by mature Silicon (Si) technology. Si-based devices have gone through many generations of development from thyristor to metal oxide semiconductor field-effect transistor (MOSFET) and Insulated-Gate Bipolar Transistor (IGBT) in the past few decades. However, Si-based devices exhibit unavoidable physical limitations regarding blocking voltage capability, operating temperature, and switching frequency, hindering the overall performance of a PE system [2].

Recently, Wide-Bandgap (WBG) materials-based devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) devices have been emerged and commercialized with superior material properties in Figure 1-1(a) [3]. SiC and GaN materials have improved properties than Si material regarding the energy gap, electric field, thermal conductivity, electron mobility, and saturated electron velocity. Concretely, a higher electric field leads to a higher breakdown voltage, while a wider bandgap and higher thermal conductivity enable WBG devices to operate at high temperatures. Furthermore, excellent electron mobility and high electric field result in low specific on-state resistance and low conduction loss. High saturated electron velocity with small junction capacitances leads to the fast switching speed of WBG devices. In summary, WBG devices offer fast switching speed, high operating temperature, and high-voltage capabilities. These superior properties allow a WBG devices-based PE system to operate at a high switching frequency, achieving high efficiency and power density.



(a) (b)

Figure 1-1 Power semiconductor (a) material properties and (b) application areas [4].

Figure 1-1 (b) provides an overview of today's application areas of power semiconductor technologies, including thyristors, Bipolar Junction Transistors (BJTs), IGBTs, MOSFETs, and GaN High-Electron-Mobility Transistors (HEMTs) concerning power rating and switching frequency [4]. In general, unipolar power devices, such as MOSFETs and GaN HEMTs, can operate at high switching frequencies because the switching transients are mainly related to junction capacitances. While it highly depends on the build-up and removal of the stored excess carriers for bipolar power devices, such as BJTs, thyristors, and IGBTs. Also, higher voltage requires more stored carriers. As a result, most bipolar devices have slower switching speeds and typically operate at lower switching frequencies though they can handle high power. Concretely, several orders of magnitude increase in switching frequency are demonstrated for WBG based devices comparing with Si devices. Although GaN material theoretically offers better high-frequency (HF) and high-voltage performances, the lack of good-quality bulk substrates needed for vertical devices and the lower thermal conductivity lend SiC material a better position for high-voltage devices. In summary, Si IGBTs are typically popular in the medium frequency range with power ratings from few kilowatts (kW) up to several megawatts (MW). Meanwhile, SiC MOSFET and GaN HEMT target HF high-power (600V, kW or above) and HF low-power (600V, kW or below) applications.

These new WBG devices are bringing a significant breakthrough in PE systems. However, lots of further developments are still required to utilize the merits of the materials thoroughly. A considerable research effort on device characterization and electro-thermal modelling is highly needed for device selection, PE system evaluation, and system optimization.

1.2. Statement of the Problem

It is a fact that there is a trend in PE system research towards high efficiency and high power density. This trend is driven by cost considerations, environmental concerns, and performance requirements. One straightforward efficiency evaluation approach is measurements in an actual hardware setup based on the power difference between input and output. An advanced power analyzer is typically used for power measurements in a complex PE system. It is purpose-built to guarantee measurement accuracy for industrial standards and has been used for decades in electrical product testing applications. However, apart from the high cost of the measuring instrument, it is inconvenient and time-consuming for PE engineers to evaluate the efficiency in the final stage of hardware implementation and make modifications to improve its performance. Also, only the overall efficiency or total power losses can usually be obtained by the measurements. Most of the time, each component's detailed power loss breakdown is not attainable, which is more informative and helpful for PE system improvements.

The importance of computer simulation in designing and analyzing a PE system has been well recognized. It is convenient and widely used, primarily at the preliminary design stage, to overcome the limitations of measurements. Since power semiconductor devices are the critical components and determinant factors for an efficient PE system, a great effort on simulation-based methods has been made. Often, a PE system contains numerous switching devices with a complex control strategy. Thus, a good understanding of the device's characteristics is necessary. Various concerns need to be taken into account by PE engineers and manufacturers in PE system simulation, which are categorized as follows:

- **Switching transients behaviors of power semiconductor devices**

The switching transients typically involve not only active switches (e.g., IGBT and MOSFET) and passive switches (e.g., freewheeling diode) but also other parasitic elements of the devices and the Printed Circuit Board (PCB). These transients commonly occur within hundred nanoseconds (ns). Still, they can engender stressful transient behaviors such as over current/voltage leading to the destruction of the device with the surrounding elements. Hence, it is critical and challenging to reproduce such informative but short behaviors, which are highly related to various devices' static and dynamic characteristics. Consequently, an accurate

semiconductor model considering different effects is highly desirable to understand the device behaviors and further optimize the design of the PE system for a proper operation.

- **Properties of WBG devices**

Generally, WBG materials have a higher energy gap, breakdown electric field, thermal conductivity, melting point, and electron velocity, allowing WBG semiconductors to operate at much higher voltage, switching frequency, and temperature than Si-based devices. As a result, the impacts of parasitic elements on the switching behaviors of WBG devices become more significant. They need to be considered due to the high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ during the switching transients. Apart from the dynamic behaviors of Si-based devices such as tail current for IGBT, reverse recovery current for PIN diode, there is also particular concern about the properties of WBG devices themselves. For instance, the junction capacitances of a SiC MOSFET are smaller than a Si IGBT, resulting in cross-talk issues [5], and are more influenced by the parasitic inductances due to the faster switching speed. Besides, there is no physical body diode in a GaN HEMT, but it still can operate in the third quadrant because of the Two-Dimensional Electron Gas (2DEG) and the symmetric structure. Manufacturers often provide a datasheet of the device with limited information, which is insufficient to fully understand and utilize devices' superior properties in various regions. Therefore, proper characterization and modelling of the device is an effective way for PE engineers to learn about these emerging devices and improve system performance.

- **Power loss analysis and thermal impacts**

With the switching frequency and power rating increments, many total power losses are generated by switching devices. Thus, semiconductor switching loss estimation is a basis for system efficiency improvement, and it is critical to ensure the safe operation of machines. As the power cycles are applied to the switching devices periodically, a fluctuation of junction temperature (T_j) results accordingly. This thermal transient can quickly affect the safe operation area by worsening the electrical performance. Also, it reduces the device lifetime on a long time scale by augmenting the soldering fatigue among the bond-wire, chip, and base plates. It is reported that power devices account for 34% of failures in a PE system. Over half of the failures result from thermal stress, including device degradation, thermal runaway failure, and thermo-mechanical failure [6]. As a result, the performance and reliability of the

PE system are significantly affected. Hence, an accurate estimation of power losses and a good knowledge of thermal impacts on device behaviors are crucial to determine the device's survival and lifetime. Also, it is a critical factor in improving the safety, reliability, and performance of the PE system.

- **Electro-thermal integration**

As the power devices and PE systems are trending towards compact size with high power density, the heat dissipation, in turn, becomes more difficult, and new challenges are imposed on thermal management [7]. It is necessary to determine the switching devices' thermal profiles to ensure they operate within a safe operating area. The self-heating effect and thermal impacts on devices' electrical characteristics need to be considered. Therefore, it is critical to bring electrical and thermal analysis together, forming an electrical and thermal simulation integration, namely electro-thermal model (or co-simulation). Electrical and thermal simulations are typically under microseconds (μs) and milliseconds (ms) time scales. Thus it is challenging to synthesize and synchronize all the information generated from both simulations. Different specific platforms or simulators are typically used for electrical and thermal simulation, resulting in convergence issues and inconveniences for PE designers. Consequently, an integrated electro-thermal model is highly desirable, considering both features with fast simulation speed and acceptable accuracy.

1.3. Motivation

Generally, efficiency, power density, and reliability are critical factors in PE applications. High power losses typically result in low efficiency in a PE system. Also, these losses lead to a sizeable cooling system and increased thermal stress on devices, which hinders the power density and reliability of a PE system. Therefore, a simulation-based approach for efficiency evaluation in a PE system urgently needs PE engineers at the design stage, avoiding hardware implementation and laborious measurements.

Furthermore, power semiconductor devices play significant roles in the efficient PE system. The power losses of semiconductor devices typically are the main contributors to the total system losses. Generally, the device manufacturers only provide the essential information in the datasheet, and the measured loss data is also limited under specific testing conditions. Hence, it is a general reference, but a noticeable loss deviation can result in a particular

complex PE application. Consequently, it is necessary to have an accurate power loss model for various semiconductors considering various aspects, such as the impacts of parasitics, diode, and temperature. A great prior effort on the semiconductor loss models has been made from different perspectives using different methods. This thesis aims to develop a comprehensive approach with a balanced trade-off among accuracy, simulation speed, and complexity by combining the best state-of-the-art methods with newly-developed techniques. It is significantly promising for PE system design and optimization.

1.4. Thesis Objectives and Contributions

- **Objectives**

This thesis's ultimate goal is to develop a simulation-based modern power semiconductor modelling approach to evaluate a PE system's efficiency. PE engineers can use this approach to predict the power loss profile and optimize the PE system by selecting suitable devices, designing appropriate control strategies, and operating in the optimal region. Specific objectives followed in this research are listed as follows,

(1) Prior-arts review

Review the basic structures and characteristics of different semiconductors, including diodes, MOSFETs, IGBTs, and GaN HEMTs devices.

Review the existing semiconductor models, including physical models and behavioral models, for various semiconductors to reproduce devices' static and dynamic behaviors.

Review the power loss estimation technology, including measurement-based methods, empirical models, integration models, and analytical models, to understand the advantages and disadvantages of different ways.

Review the electro-thermal modelling techniques, including the thermal dependent properties, thermal network, and existing approaches to understand various devices' electrical and thermal performances.

(2) Behavioral transient models development

Develop datasheet-based transient models to represent the static and dynamic characteristics for different semiconductor devices and simulate detailed switching waveforms under different operating conditions.

(3) Power loss analysis

Conduct the power loss analyses analytically for various devices, including conduction loss, switching losses, reverse recovery diode loss, and other parasitic-related loss under different voltage, current, and temperature conditions.

(4) Electro-thermal integration

Study thermal impacts on various devices' switching behaviors and combine the thermal network and electrical network to form an electro-thermal simulation for power losses and junction temperature estimations in a PE system.

(5) PE system evaluation and optimization

Apply the electro-thermal simulation method to a complex PE application as a case study to evaluate the system efficiency and optimize the PE system by selecting an appropriate device combination with the lowest total power losses.

- **Contributions**

This thesis proposes a multi-level electro-thermal simulation approach to estimate the power losses and evaluate the efficiency of a PE system using modern semiconductors. In the device-level simulation, the transient switching waveforms are reproduced by the behavioral device model in a Double Pulse Test (DPT) circuit, considering the impacts of parasitics, diode, and temperature. A multi-dimensional power loss Look-Up Table (LUT) is further generated under a wide range of voltage, current, and temperature based on the switching waveforms. Moreover, in the system-level simulation, an electrical network and a thermal network are implemented with simple switch models for semiconductor devices. As a result, the instantaneous power losses are obtained by LUT based on the operating conditions, and subsequently, the system efficiency is determined. In this way, the accuracy is guaranteed by the device simulation with nanoseconds time-step; meanwhile, the simulation speed is still maintained in system simulation with microseconds or larger time-step.

This approach is developed based on prior research works and applies to various semiconductor devices. It also provides a comprehensive insight into the electro-thermal modelling area and helps PE engineers design and optimize PE systems.

1.5. Thesis Outline

This thesis's content comprises material published in IEEE conferences and journals to form most of the chapters. In total, this thesis contains seven chapters structured in the following ways.

Chapter 1 introduced modern semiconductor devices in PE systems and their device features and the application area. Further, the device modelling area's problems were addressed, and the motivations behind this work were also identified. Besides, the objectives and contributions of this thesis were provided.

Chapter 2 reviews the semiconductor modelling-related techniques in the past decades. The basic operating principles and characteristics of different semiconductor devices are introduced briefly. Also, various semiconductor models and power loss estimation methods are discussed with their advantages and applicability. The electro-thermal modelling techniques are also provided, along with a discussion on existing models' pros and cons.

Chapter 3 presents a transient behavioral model of Si IGBT for loss estimation in a PE system. A multi-level simulation strategy is proposed, and the IGBT device model is developed along with a detailed switching process and power loss analysis. Furthermore, the proposed method is experimentally verified by a DPT bench and a boost converter application in switching transients and power losses for a wide range of operating conditions.

Chapter 4 focuses on an electro-thermal simulation for SiC MOSFET based on the previous IGBT model. A dynamic thermal model is added to the multi-level simulations to form a close-loop simulation for power loss and temperature estimations. The device characteristics of SiC MOSFET are studied and modelled in detail with the parameter extraction procedures. Further, a DPT platform for SiC MOSFET and a Power Factor Correction (PFC) prototype are designed and built to verify the developed approach concerning the electrical and thermal performances.

Chapter 5 presents a generalized modelling methodology for switch-diode cells, which applies to Si-based IGBTs, MOSFETs, PIN diodes, and WBG devices such as SiC MOSFETs, GaN HEMTs. The transient switching modelling and the power loss analyses for various devices under different operating conditions are discussed in detail with crucial parameter

extraction methods from device datasheets. Different DPT boards for different devices are designed and tested respectively for switching transients and power loss verifications. Besides, a discussion on the accuracy, efficiency and applicability of the model is illustrated.

Chapter 6 provides a case study using simulation-based device models in a single-phase grid-tied PV inverter for efficiency evaluation. The principle of operation is reviewed along with the static characteristic analysis. Also, three sets of switching devices with different operating features are identified, and their device requirements are further determined. Subsequently, a device comparison in terms of static and dynamic characteristics of different devices is conducted, and the inductor design guideline is also demonstrated. Further, a power loss analysis for various device combinations with designed inductors is carried out. Consequently, a mixed device combination is determined with the lowest power loss and experimentally validated in the PV inverter prototype.

Chapter 7 concludes the thesis by discussing the achieved objectives and pointing out the possibility of extending the research work in the future.

Finally, the references used in this research are listed with numbers representing the cross-referencing location pointing to the corresponding text in this thesis.

Chapter 2 Literature Review

2.1. Background of Modern Semiconductors

Power semiconductors are critical components in Power Electronics (PE) systems classified into two- and three-terminal devices in Figure 2-1[8]. Power diodes, including PIN diodes and Schottky Barrier Diodes (SBDs), are two-terminal devices made from Si or SiC materials. Three-terminal devices include Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs), Insulated-Gate Bipolar Transistors (IGBTs), Bipolar Junction Transistors (BJTs), and thyristors [9]. In general, IGBTs, BJTs and thyristors are Si-based devices, while Wide-Bandgap (WBG) materials[10], e.g., Silicon Carbide (SiC) [11] and Gallium Nitride (GaN) [12], are more commonly used in MOSFETs and High-Electron-Mobility Transistors (HEMTs)[13]. Besides, IGBTs, BJTs, thyristors and PIN diodes are minority carrier devices, providing excellent conduction performances. While MOSFETs, HEMTs, and SBDs are typically majority carrier devices with superior switching performances. Consequently, to make a proper device selection for a PE system, it is necessary to consider various aspects such as device cost, dynamic performance, thermal capability, and power rating.

Power semiconductors typically behave as single-pole single-throw switches to facilitate the power flow. However, a simple ideal switch can not fully represent the device's switching behavior. Switching losses are noticeable contributors to the total system losses, especially in high-frequency (HF) PE applications. The essential characteristics and operation principles of widely used power devices, including diodes, MOSFETs, IGBTs and GaN HEMTs, are reviewed in the following section. Note that the device's physical behaviors, fabrication and packaging are beyond the scope of this study and are not discussed in this chapter.

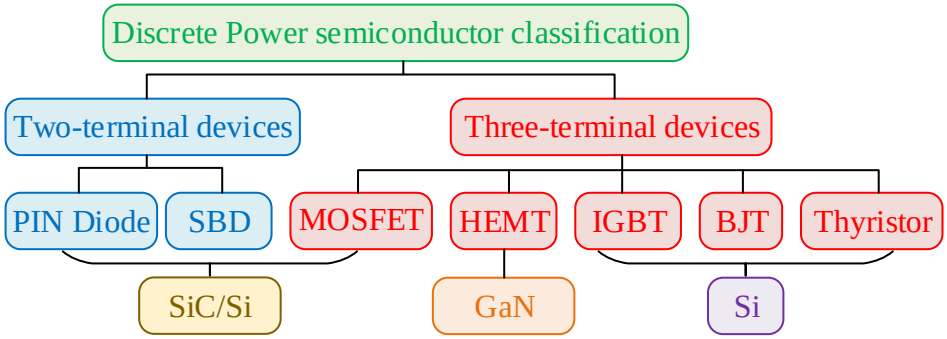
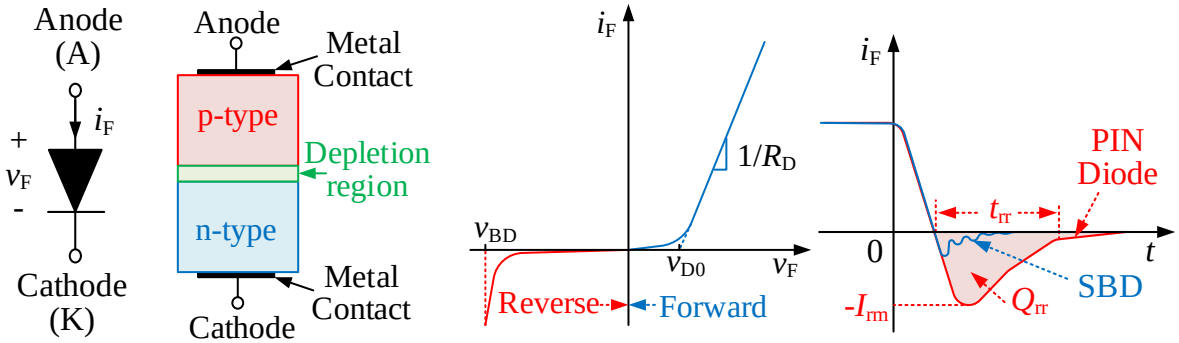


Figure 2-1 Discrete power semiconductor classification [8].

2.1.1 Power Diode Overview

Power diodes such as PIN diodes and SBDs are among the most widely used power semiconductor devices in PE systems [14]. The PIN diode's circuit symbol in Figure 2-2(a) consists of terminal Anode (A) and Cathode (K). In a PIN diode, a junction is formed between the p-type and the n-type layers shown in Figure 2-2(b). In contrast, the junction is formed between the n-type layer and the metal plate in an SBD. Nevertheless, both diodes' typical I-V curves are similar, as shown in Figure 2-2(c). When a diode is forward biased, namely, the forward voltage (v_{F}) is positive, a forward current (i_{F}) starts flowing through the device with a small voltage drop (typically less than 1V). This forward characteristic of a diode is expressed as a threshold voltage (v_{D0}) with a linear incremental or slope resistance (R_{D}). By contrast, when the diode is reverse biased, only a negligible leakage current can flow in the reverse direction until the reverse breakdown voltage (v_{BD}) is reached and avalanche occurs.

In practice, when a diode switches from the forward conduction state to the reverse-biased state, i_{F} is reduced to zero and then continues to flow in the reverse direction due to the stored minority carriers in the diode. These minority carriers require a specific time to recombine with opposite charges and to be neutralized. This time is called reverse recovery time (t_{rr}) and the number of charge carriers that flow across the diode is defined as reverse recovery charge (Q_{rr}) as shown in Figure 2-2(d). Note that the diode initially is inactive and not capable of blocking the reverse current flow until i_{F} reaches the peak value (I_{rm}). Afterwards, the diode voltage starts to reverse. This reverse recovery behavior of the diode results in overcurrent issues and considerable losses, especially for HF applications. Since SBD is a majority-carrier device, this period is mainly limited by the junction capacitance and thus significantly shorter [15].



(a) (b) (c) (d)

Figure 2-2 PIN diode (a) symbol; (b) structure; (c) I-V curves; (d) reverse current [14].

2.1.2 Power MOSFET Overview

Power MOSFET is one of the most popular voltage-driven switching devices with the merits of fast and efficient switching in PE systems. It is a majority carrier-based unipolar device and is typically classified into the p-channel and n-channel enhancement MOSFET. Generally, the latter is more widely used due to the higher mobility of electrons. The circuit symbol of an n-channel MOSFET is illustrated in Figure 2-3(a), which consists of three terminals, gate (G), drain (D) and source (S). The forward drain current (i_d) flows through the conductive channel between D and S. This current is controlled by the gate-source voltage (v_{gs}) as shown in Figure 2-3(b). Notice that an inherent PIN body diode is formed parallel with the channel, allowing a bidirectional switch implementation [16].

Furthermore, the output and transfer curves of a MOSFET are provided in Figure 2-3 (c) and (d), respectively [17]. A MOSFET can operate in three distinct regions, 1) ohmic, 2) saturation and 3) cut off regions, according to the conditions of v_{gs}, drain-source voltage (v_{ds}) and threshold voltage (v_T). For $v_{gs}<v_T$, the device operates at the cut-off region where no current is conducting. As v_{gs} increases above v_T, the conductive channel is built and i_d starts rising following the curve in the saturation region. Eventually, when $v_{ds} < v_{gs} - v_T$, the MOSFET enters the ohmic region and behaves as a resistor called on-state resistance ($R_{DS(on)}$). Notice that in the reverse direction, the body diode plays a crucial role in conducting current. If a positive v_{gs} is given during the reverse conduction, the conductive channel still can be built as the same $R_{DS(on)}$ in the forward operation. The relationship between i_d and v_{gs} is described by the transfer curves in Figure 2-3 (d). In the following chapter, the static and dynamic characteristics of the MOSFET are studied in detail.

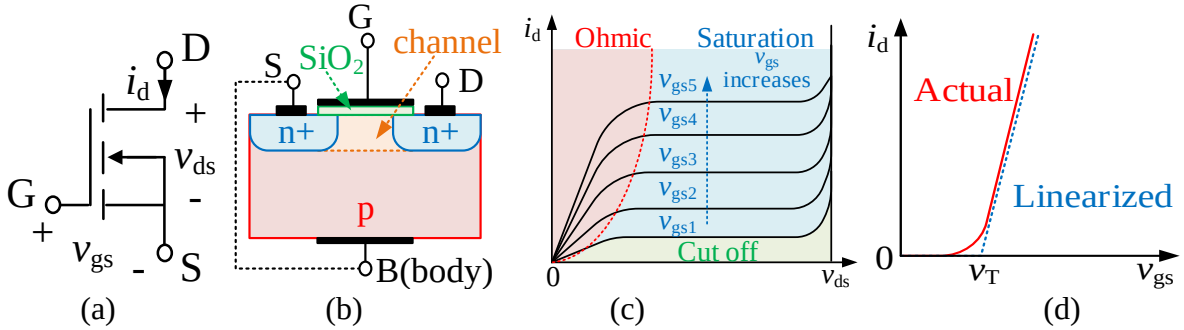


Figure 2-3 Typical MOSFET (a) circuit symbol; (b) physical structure; (c) output characteristic; (d) transfer characteristic [16].

2.1.3 IGBT Overview

IGBT is a hybrid device with the Darlington configuration [18] of a MOSFET and a BJT. It consists of three terminals Gate (G), collector (C) and emitter (E), as shown in Figure 2-4 (a) [19]. It can switch in the same manner as a MOSFET, and the BJT handles the primary current due to its physical structure in Figure 2-4(b). As a result, both merits of fast switching and superior conduction performance are achieved along with high breakdown voltage. Like a MOSFET, an IGBT can operate at three regions: Saturation, Active and Cut-Off regions, as shown in Figure 2-4(c). If the gate-emitter voltage (v_{ge}) is below v_T, the IGBT is in the Cut Off region, and no current is conducting. As v_{ge} increases above v_T, the IGBT enters the Active region and the collector current (i_c) can rise almost linearly with v_{ge} as shown in Figure 2-4(d). When the conductive channel is entirely established, the IGBT maintains in the saturation region with an on-state saturation voltage drop (v_{cesat}). The gate voltage is typically provided as 0V to turn off the IGBT, and subsequently, the channel current decreases until it reaches zero. Different from MOSFETs, IGBTs can not turn off immediately. In fact, i_c decays gradually known as the tail current because of the recombination of the excess carriers. On the one hand, the inherent BJT in the IGBT enables the conductivity modulation and leads to low v_{cesat}. On the other hand, this current tailing behavior prolongs the turn-off time, resulting in an additional loss. Also, a note from the physical structure of IGBT is that there is no inherent body diode like in the MOSFET. As a result, a single IGBT theoretically cannot conduct in the reverse direction. Thus an additional anti-parallel diode is typically required and configured with IGBT to facilitate reverse conduction. Besides, the anti-parallel diode usually is better than the body diode of MOSFET, resulting in reducing the reverse recovery loss.

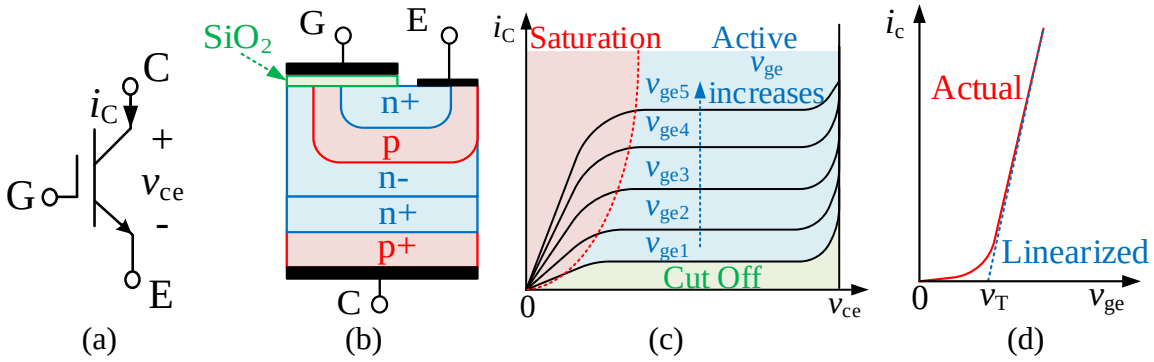


Figure 2-4 Typical IGBT (a) circuit symbol; (b) Physical structure; (c) output characteristic; (d) transfer characteristic [19].

2.1.4 GaN Overview

GaN HEMTs have recently gained popularity due to their advantages of faster switching speed, smaller output charge, and lower switching losses than Si-based devices [20]. Enhancement mode GaN (eGaN) HEMTs are widely used and borrow the same terminology as Si MOSFETs: G, D and S, as shown in Figure 2-5(a) [21]. A Two-Dimensional Electron Gas (2-DEG) [22] is generated at the interface between the AlGaN and GaN layers, as shown in Figure 2-5(b), resulting in low on-state resistance. Its forward characteristic in Figure 2-5(c) is similar to a MOSFET, and i_d is determined by v_{gs} and v_{ds}. Thus it is not discussed here to avoid repetition, while the third quadrant characteristic in Figure 2-5(d) is discussed.

Unlike the MOSFET, there is no PN junction within the lateral structure of eGaN HEMT. Namely, no body-diode physically exists in an eGaN HEMT. However, it can still conduct in the reverse direction with the symmetrical structure and the 2DEG channel. Hence, it is unnecessary to pair an additional anti-parallel diode with eGaN HEMT, which leads to extra output capacitance and switching losses. Basically, in the third quadrant operation, the source terminal and drain terminal can equivalently change positions. As a result, the gate-drain voltage (v_{gd}), instead of v_{gs}, becomes the driving force for the reverse conduction of eGaN HEMT. Like a diode, the reverse channel self commutes, and the source-drain voltage drop (v_{sd}) is self-biased by v_T-v_{gs} which increases with the reverse current. If a positive gate signal is provided during reverse conduction, v_{gd} equals to the sum of v_{sd} and v_{gs}, which is typically higher than v_T, enabling the channel fully on with the same on-state resistance as in the first quadrant. Consequently, both superior conduction and switching performances can be achieved in eGaN HEMT with an appropriate control strategy and gate drive design [21].

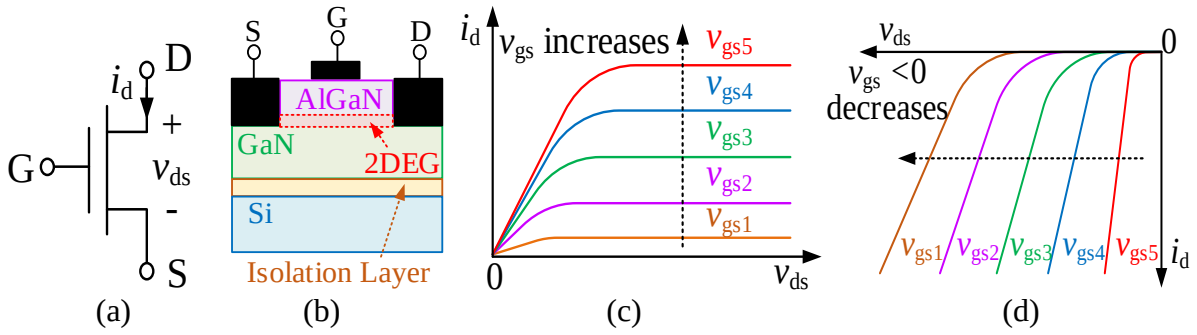


Figure 2-5 Typical eGaN HEMT (a) circuit symbol; (b) Physical structure; (c) forward characteristic; (d) third quadrant characteristic [21].

2.2. Semiconductor Modelling Techniques

Power semiconductors are critical components in a PE system. Generally, it is the component that limits switching frequency, efficiency, power density and sometimes reliability in converter design. As a result, power semiconductor models are highly desirable by PE engineers to predict device behaviors, understand internal device mechanisms and optimize the system design. According to the modelling method used, semiconductor models in PE systems are classified into device-level and system-level models.

2.2.1 Device-level Model

The device model's primary objective is to predict the static and dynamic device behaviors under different operating conditions (voltage, current and temperature). A good approximation of the electrical variables' actual relationship needs to be obtained for the device model, and a compromise between computational speed and model accuracy is usually made. It is well known that a simple device model generally provides fast simulation speed but loses the physical insights into device behaviors and the simulation accuracy. On the other hand, a complicated physics-based model is usually preferred due to its high accuracy, but it is time-consuming and unsuitable for large-scale system simulations.

It is necessary to consider the devices' static and switching characteristics in the power device models. For instance, the nonlinear junction capacitances of devices have significant impacts on the device's dynamic behaviors. For bipolar power devices, such as PIN diode and IGBT, conductivity modulation is the crucial effect that reduces the on-state resistance. Over the years, a remarkable research effort has been put into semiconductor modelling from different objectives, aspects, and performances using different methods categorized as physical and behavioral models. Other classifications such as mathematical models, semi-mathematical models, and semi-numerical models were also used in the literature [23]-[26]. The choice of the device model depends on the required accuracy and complexity.

- **Physical model**

Physical models are based on semiconductor physics, and the descriptions of electrical and thermal behaviors are obtained by solving physics equations with some simplifications. As a result, high accuracy is typically achieved though it is complicated and requires numerous

physical parameters, usually not attainable for PE engineers. An introduction of the physical models for various devices is provided as follows.

For IGBT physical model, Hefner *et al*. [27] proposed the one-dimensional (1-D) charge-controlled model. It was widely used and implemented into the general-purpose simulator Saber. The currents between the terminal nodes were expressed using the system variables, and the nonlinear capacitances were also considered. Kraus *et al*.[28] provided an analytical solution for charge carrier distribution, taking the two-dimensional (2-D) effect and thermal impact into account. This model was also implemented into Saber, and similar SPICE models were further developed with different features for different applications [29]-[30]. This 2-D effect was analytically studied by Sheng *et al*. [31] and was expressed either in series form by Feiler *et al*. [32] and Napoli *et al*.[33] or Laplace form in [34]. However, most of these models are complicated, requiring device physics knowledge.

Recently, more research efforts have been put into WBG device modellings, such as SiC MOSFETs and GaN HEMTs. Based on the traditional Si MOSFET models, many SiC MOSFET models have been developed considering different effects. For example, the interface trap's impact was taken into account in [35], and the influence of traps on the threshold voltage was discussed in [36]. Potbhare *et al*. [37] developed a comprehensive model considering more device physics such as interface trap densities, Coulombic interface trap scattering and their dependences on temperature and bias. A compact model in [38] and a datasheet-driven model in [39] were proposed to reduce the complexity.

GaN HEMTs, as a relatively emergent technology, lag behind the mature si-based technology. Several analytical models of GaN HEMT were developed in [40]-[41], focusing on accurately determining 2-DEG charge density. By linearizing this 2-DEG charge, Karumuri *et al.* [42] proposed a compact model for drain current of HEMTs. Further, Vitanov *et al.* [43] provided a mobility model accounting for electron transport specifics in GaN material. A computational modelling approach was adopted in [44] for GaN HEMT to extend the Sentaurus TCAD-based numerical simulation [45]. However, these device models were developed mainly to achieve high accuracy in describing the device physics. As a result, these models often require great computational efforts and are hardly feasible to be used in a PE system simulation.

- **Behavioral model**

Generally, behavioral or empirical models focus on the devices' external characteristics without considering their physical operation mechanism. These models are typically implemented using mathematical fitting methods and model parameters, which usually have no physical meaning. The resultant expressions, databases or components are then used in a simulator to model the device. As a result, fast simulation speed and simple implementation are achieved. Nevertheless, the model's accuracy is limited, especially when the operating conditions are beyond the available range provided in the device datasheet. In the following, behavioral models for various devices are reviewed.

For IGBT behavioral models, Hsu *et al.*[46] considered the IGBT as a nonlinear system using Hammerstein configuration, and the output characteristics of IGBT were modelled by a current source with passive components in [47]. Furthermore, IGBT losses were estimated in [48] by the curve fitting approach without considering the device switching behaviors. The model proposed in [49] took a hybrid pair of an IGBT and a SiC diode into account with empirical parameter extractions. The high-frequency impact on switching transients was studied in [50], and the parameter extraction algorithm was provided in [51]. A single IGBT model was extended to a multi-chip power module forming a compact model [52]. However, the impacts of circuit parasitic elements and temperature were not fully considered in these models.

To model the dynamic characteristics of SiC MOSFETs, Alexakis *et al.*[53] used a variable drain-source resistance with three constant junction capacitances, and the device losses were estimated in [54] using polynomial functions. 10-kV SiC MOSFET was characterized and modelled by Wang *et al.* [55] based on the commercial SPICE MOSFET model. The temperature dependence was considered in [56] and [57]. Duan *et al*. [58] improved existing models by taking junction capacitances into account and implementing the SPICE language model. Nevertheless, the interaction between diode and switch was hardly considered in these models, significantly impacting HF application.

Most of the GaN models focus on radio frequency (RF) applications or analytical solutions for loss estimation. Several GaN HEMT models have been developed based on existing MOSFET models. Okamoto *et al*. [59] improved the Efficient Power Conversion

Corporation's (EPC) device models. They developed the SPICE-based GaN HEMT model for loss estimation in AC-AC direct converter, while Huang *et al*. [60] focused on the loss of GaN HEMT in cascade configuration with Si MOSFET. Further, the dynamic on-state resistance of GaN HEMT was studied in [61]-[62]. Endruschat *et al*.[63] generalized the behaviors of MOSFET and GaN HEMT and proposed a universal SPICE field-effect transistor model.

In conclusion, those device models have different complexity, computation speed, accuracy, and model parameters' attainability. The model selection should be based on the specific accuracy and computation speed requirements.

2.2.2 System-level Model

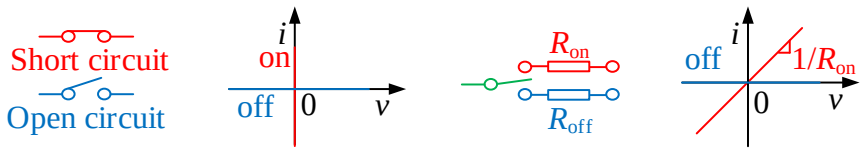
The system-level model mainly considers the essential switching function rather than the device's switching transient behaviors. It is widely used in electromagnetic transient (EMT) programs such as PSCAD and SIMULINK, based on nodal analysis or state-space solution of linear ordinary differential equations using numerical integration rules. Power semiconductors in those simulators are usually modelled as ideal switches, resistors, switching function models or averaged models for system-level study.

- **Ideal switches and resistance models**

The equivalent circuit and switching characteristics for an ideal switch were provided in Figure 2-6 (a) and (b), respectively, [64]-[65]. When a switching device turns on, it is typically considered a short circuit with a zero voltage drop. It becomes an open circuit when it turns off. Therefore, it is lossless without considering the switching transients and conduction behavior. Besides, the system admittance matrix needs to be re-calculated when the switching status changes.

Furthermore, the two-state resistance model was also widely used in PE simulations for all semiconductor devices. Figure 2-6 (c) and (d) illustrated the diagram and I-V curve of the resistance model, respectively. A two-valued resistor represented a switching device on and off states with the typical values $1\mathrm{m}\Omega$ for $R_{\mathrm{on}}$and $1\mathrm{M}\Omega$ for R_{off}, respectively. Notice that compared with the ideal model, the circuit matrix dimension was independent of the switching status. Hence, the simulation time was reduced significantly, and conduction loss could also be considered roughly by R_{on}. In conclusion, ideal switches and resistance models were

straightforward and widely used for preliminary system and control design. They could provide a fast response for topology and control strategy verifications.



(a) (b) (c) (d)

Figure 2-6 Diagrams of (a) Ideal switch (b) ideal I-V curve; (c) resistance model diagram; (d) I-V curve [64]-[65].

- **Switching function models**

Switching function models used controlled voltage and current sources to represent the switching devices' external output voltage and current [66]-[67]. The equivalent circuit of the switching function model is illustrated in Figure 2-7. Notice that the input voltage (v_{ins}) and current (i_{ins}) together with the output v_{outs} and i_{outs} were linked by the controlled sources with the switching function f(t) and g(t). Typically, f(t) and g(t) were highly related. As a result, the simulation was much faster, and the high-frequency effect could also be considered. However, since individual switches no longer existed, the transient voltage and current of individual switches were not available.

- **Averaged models**

The circuit's switching devices still turn on and off at high switching frequencies in the above models. Averaged models [68]-[69] have been developed to speed up the simulation by only considering low-frequency components in the circuit. During one switching period, the switching function was averaged, and thus the switching behaviors and harmonic components were excluded. Typically, the averaged model was obtained directly by replacing all the switching functions with their averaged counterparts. Since there were no switching transients and the circuit topology was invariant, the simulation was accelerated significantly. However, an individual switch's behavior was not attainable, and the switching harmonic effects were not considered. Hence, it was mainly used in controller design and small-signal analysis for switching-mode converters.

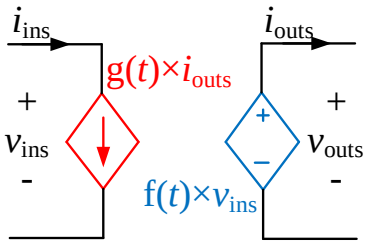


Figure 2-7 Equivalent circuits of the switching function model [67].

2.3. Power Loss Estimation Techniques

A PE converter's power loss analyses are critical for efficiency and performance evaluation, requiring an accurate power loss model of the semiconductor device, including conduction loss and switching losses. The static characteristic of the device is used to estimate the conduction loss. Meanwhile, switching losses require considering the dynamic behavior of the device, parasitic elements and operating conditions such as temperature, gate resistance, voltage and current. Generally, methodologies proposed in the literature on power loss estimation are broadly classified as measurements, empirical models, integration models and analytical models.

2.3.1 Measurement

Doule pulse test (DPT) is a widely accepted method to characterize the dynamic performance and measure switching losses of power semiconductors [70]-[72]. Two pulses were sent to the lower switch, namely the Device Under Test (DUT), in a diode-clamped inductive load circuit, as shown in Figure 2-8 (a). During the first pulse, DUT was on, and the DC source charged the load inductor. Simultaneously, the load current gradually increased until it reached the desired value I_L at the end of the first pulse. The turn-off switching waveforms along with the corresponding power loss was obtained. During the short interval between the first and second pulses, I_L flowed through the upper freewheeling diode and remained almost constant. When the second pulse was given, DUT turned on again, and thus the turn-on switching behavior along with the turn-on loss was evaluated. After the second pulse, DUT was turned off, and the inductor's energy was naturally decayed and dissipated. Consequently, by adjusting the DC bus voltage and the first pulse duration, the power losses under different desired conditions were obtained.

A typical implementation of the DPT setup was illustrated in Figure 2-8 (b) [73]. The DPT board included main power switches, DC capacitor bank, gate drive, protection circuit and peripheral interfaces to connect with external DC power supply and load inductor. The double-pulse signals with adjustable pulse widths were typically provided by a microcontroller or signal generator. The switching waveforms and the power losses were measured by probes and oscilloscopes and exported to a computer for post-data processing. Eventually, a multi-dimensional power loss table of the DUT was generated.

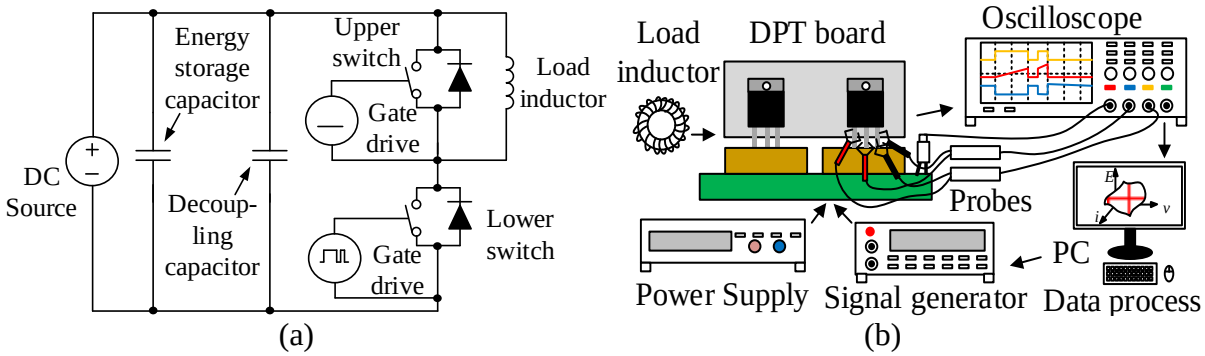


Figure 2-8 DPT (a) schematic, and (b) physical implementation [73].

Generally, measurement is an accurate method for power loss estimation. However, this method is time-consuming with repetitive tests. Apart from the tedious processes for different permutation of test conditions, it has to be a well-designed setup with low parasitics. High bandwidth probes are needed, especially for WBG devices.

2.3.2 Empirical Model

The Empirical models in [74]-[75] used loss equations to fit the power loss curves from datasheets or experimental measurements. Typically, power loss equations, including conduction loss and switching losses, were expressed by operating voltage, current and temperature. During the device simulation, the power losses for a specific switching event were approximately estimated by computing the loss equations or the power loss Look-Up Table (LUT) based on the operating conditions. Therefore, the empirical model was a simple mathematical method and thus required a reasonable computation effort. Since the power loss curves from datasheets were the measurements under specific test conditions by manufacturers, the accuracy of loss estimation beyond the available range or in different operating conditions was limited. Besides, the impacts of parasitic parameters in the circuit were not fully considered. Many additional experiments were needed to obtain accurate power

loss curves in a wide range of operating conditions. Therefore, empirical models were suitable for roughly estimating the power losses of semiconductors with fast speed.

2.3.3 Integration Model

Integration model [76]-[78] was a straightforward power loss estimation method by integrating the product of the voltage across the device and the flowing current based on the transient switching waveforms from experiments or circuit simulations. A physical device model such as the SPICE model was often used to obtain accurate switching waveforms. However, the physical model's internal parameters were difficult to obtain. Using the detailed device model in a PE system simulation was time-consuming, along with convergence problems. Therefore, it was more suitable for device-level estimation than overall system-level estimation, which involved massive data processing and computation burden.

2.3.4 Analytical Model

The analytical power loss model aims to derive a series of analytical power loss equations for each switching process interval based on the switching devices' equivalent circuits and the simulated or typical switching waveforms. Approximation formulas describe the analytical model's device parameters, and the fitting coefficients are extracted from datasheets or measurements.

A piecewise linear analytical loss model was commonly used for its simplicity [79]-[80]. However, the parasitic capacitances and inductances were not fully considered resulting in low accuracy, especially for high-frequency applications. Rajapakse *et al.*[81] developed an analytical model by "filling-in" the device's current and voltage waveforms between the simulation time-step. It conformed to the physical switching process, and mathematical algebraic power loss equations were derived. However, it involved complicated formulas, and the accuracy was limited by the operating conditions and circuit parameters.

Recently, various impacts on the device's switching behaviors have been taken into account to improve the model accuracy. These impacts included the effects of parasitic elements [82], the interaction of the PIN diode or SBD [83] and other new insights (e.g. carrier-trap influences [84], ringing losses [85], non-flat miller plateau [86] and displacement current [87]). Li *et al.*[88] developed a model considering the effect of parasitic capacitances, and

Christen *et al.*[89] proposed a loss model in a half-bridge configuration. Nevertheless, the temperature-dependent parameters [90] were not mentioned, and iterative processes for solving equations were normally involved in those models. The idea of conservation of energy [91] was applied to the losses calculation, requiring numerical calculations (e.g., Laplace transform [92] and state equations [93]).

Furthermore, the entire switching process of eGaN HEMT in synchronous buck converter application was presented in [94]-[95], considering the third quadrant operation with the help of the 2DEG. However, it was complicated, involving a heavy computational burden, not to mention the convergence issues. The measuring techniques and loss distribution, including the capacitive losses for GaN HEMT, were illustrated in [96]-[97]. The scalable loss estimation method was further proposed based on the measured loss data. However, the datasheet's measured data was typically under specific conditions. Thus, the applicability and the accuracy were limited.

2.4. Electro-thermal Modelling Techniques

With the development of semiconductor devices, modern WBG devices such as SiC MOSFET and GaN HEMT enable a higher switching frequency in PE systems, resulting in a considerable reduction of the passive components' size and thermal management effort. High efficiency, power density and reliability can also be achieved. As the devices and PE systems become smaller and more compact, the heat dissipation resulting from the increased power losses becomes more severe, which is more challenging on thermal management. In general, both the electrical and thermal performances of semiconductor devices are critical for PE systems' safety, reliability and performance. In order to ensure the switching devices operating at the safe operation area, it is necessary to consider the junction temperature profile at the the early design stage of a PE system. Hence, the traditional device models need to take the thermal impact into account, and an electro-thermal model for switching devices is highly desired for system design, integration and optimization.

The basic idea of an electro-thermal model in Figure 2-9 used a semiconductor device model to map the device losses in a wide range of operating conditions [98]. Then the operating junction temperature was obtained by thermal modelling method feeding back to the electrical network. Besides, the parameters of the device model were updated for the instantaneous

junction temperature. In this way, a closed-loop electro-thermal co-simulation was achieved, and both the electrical behaviors and thermal performance were linked in a PE system. Typically, a switching event for a semiconductor device could last within a few microseconds. In contrast, the slow load and thermal variations were usually maintained during the converter's regular operation minutes or hours. Therefore, one challenge in these scenarios was dealing with very different timescales and coordinate devices' different dynamic behaviors.

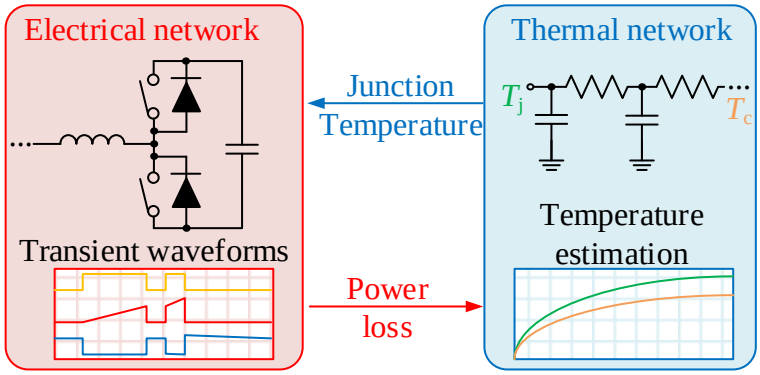


Figure 2-9 Typical schematic of electro-thermal model [98].

2.4.1 Thermo-Sensitive Electrical Parameter

The concept of the Thermo-Sensitive Electrical Parameters (TSEPs) have been developed to describe the electrical parameters of a semiconductor device related to the T_j [99]-[101]. These parameters were used as indicators of T_j and case temperature (T_c) to monitor the devices' health state. On the other hand, the temperature could influence the electrical performance of devices by TSEPs. In the past decades, many works have been done to discuss the dependency of various TSEPs upon the T_j and each TSEP has been characterized by its own sensitivity and linearity to the temperature.

v_T was defined as the gate voltage required to create a conductive channel allowing a current to flow. In [102]-[103] , v_T was a nearly negative linear behavior over the whole temperature range. It was found that v_T typically reduced with increasing temperature and specifically, the sensitivity was in the range of -2 to -10 mVK^{-1}[104].

Another commonly used TSEP was v_{cesat} for the case of IGBT [105]. Apart from the temperature dependency, it was also found that v_{cesat} was slightly current dependent. A negative temperature coefficient was observed at a low current range, while a positive

temperature coefficient was found for a high current range. The sensitivity of v_{cesat} decreased as the current increased and became zero at a medium current range. As for other devices, $R_{\mathrm{DS(on)}}$ was more widely used as a TSEP. It was found in [106] that the temperature dependency of $R_{\mathrm{DS(on)}}$ in SiC MOSFET was low and nonlinear, while the counterpart in Si MOSFET was much higher. Furthermore, Felgemacher *et al*. [107] mentioned the temperature dependence of the intrinsic gate resistance (R_{gint}) and the sensitivity was approximately 1.5m$\Omega\mathrm{K}^{-1}$. In addition, the reverse recovery charge Q_{rr} increased with temperature due to the positive temperature coefficient of minority carrier lifetime, which had the effect of increasing the stored charge in the diode drift region [108].

Besides, several pieces of research have provided more insights into various indirect TSEPs of devices, such as the turn-on delay (t_{don}) and turn-off delay time (t_{doff}) [109]-[110]. The definitions of t_{don} and t_{doff} were the time period from the change of gate drive voltage to the actual change of the channel current. Typically, the temperature dependency of t_{don} lied in the range of 0.5-1.0 nsK^{-1} which in fact was also influenced by the switching voltage and current. On the other hand, t_{don} showed largely independent of operating current with a much lower sensitivity less than 0.1 nsK^{-1}. To reflect the thermal impacts on the switching transients of devices, more temperature-dependent parameters such as the trans-conductance (g_{fs}), carrier lifetime and the peak reverse recovery current, need to be considered based on the specific device and operating conditions.

2.4.2 Thermal Modelling Techniques

The thermal analysis of PE systems is imperative, as the power density and switching frequency continuously increase. In a modern PE system, power cycles are applied to the devices leading to a rise and fall of the temperature during regular operations. A high junction temperature occurring during the abnormal loads or short-circuit operation may result in an extremely high thermal stress in the devices. Consequently, it causes reliability issues, such as wire bond lift-off, solder fatigue and semiconductor failure [111]. Therefore, an accurate thermal model is critical for T_{j} prediction and thermal performance evaluation. Numerous thermal modelling and analysis methods have been established in the past, categorized as numerical and thermal equivalent circuit models.

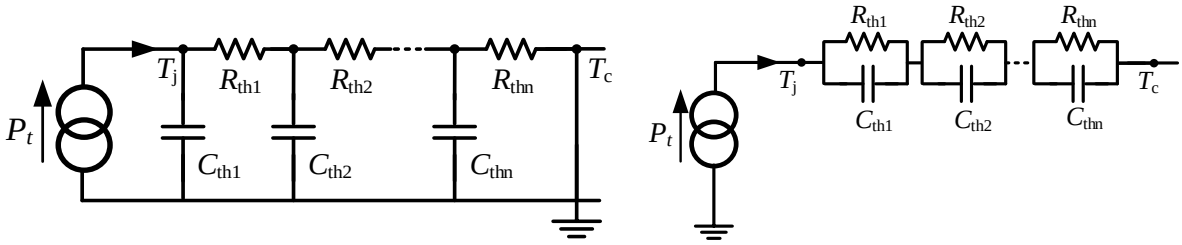
- **Numerical method**

There were two main numerical methods for steady and dynamic thermal analysis, including the Finite Element Method (FEM) [112]-[113] and the Finite-Difference Method (FDM) [114]. These methods were commonly used for precise 3-D modelling and simulation of device packages with many finite elements, boundary conditions, and heat sources. Drofenik *et al*. [115] developed a 3D FEM model for an IGBT power module, and also the sensitivity of the model parameters on simulated results was analyzed. A similar 3D FEM model was demonstrated in [116]. It used a MOR for simplification and was implemented in the CASPOC circuits simulator and the ANSYS workbench. Several compact FEM-based thermal models were developed to reduce the model order using mathematical manipulation of linear matrix [117] or a generalized minimized residual algorithm [118]. Fourier-series-based thermal models [119]-[120] have been developed to obtain each physical layer's thermal impedances. The structural and temperature-independent material properties were parameterized, and the thermal distribution of each layer was identified. Although the numerical methods could provide sufficient accuracy with the detailed material properties and the exact physical dimensions, it was not applicable for long-term reliability assessment. That was because of the heavy computational burden. Thus it could not co-exist with an electrical simulation, making a dynamic electro-thermal model. Besides, the thermal capacitance contributions from the heat sink and thermal grease were ignored during the transient thermal simulations.

- **Thermal equivalent circuit model**

As for the thermal performance evaluation, simple thermal resistances between different layers are commonly used to represent the heat transfer process for steady-state thermal analysis and T_j is further computed. While for dynamic thermal analysis, thermal impedances are required to be taken into consideration. Resistance-capacitance (RC) thermal networks, including Cauer-type [121] and Foster-type [122] in Figure 2-10, were widely used for steady and dynamic thermal analysis in a PE system. These two types of networks could be transformed into each other by mathematical method. R and C were based upon discretizing the heat diffusion equation for various 3D coordinate system symmetry conditions in the RC thermal models. The thermal distributions among the devices, packages, and heat sinks were computed in analogy with the calculation of currents and voltages over the electrical network.

As a result, both the thermal and electrical networks were coupled with the total power loss dissipation (P_t) and operating conditions.



(a) (b)

Figure 2-10 RC thermal model (a) Cauer-type [121], (b) Foster-type [122].

A Cauer-type thermal-impedance model was constructed in [123] based on the geometry and the packaging structure of semiconductor devices. Therefore, the parameters such as the nodes, thermal resistances and capacitances had their physical meanings. These parameters were also adjusted during the semiconductor's ageing process or by considering the temperature dependence of the materials' properties. Conversely, the Foster thermal-impedance models developed in [124]-[125] were equivalent counterparts fitted from measured or simulated thermal results. It was convenient to extract Foster-type parameters, which were usually available in the datasheet. A high or low-order RC thermal model was used based on the required accuracy of characterizing semiconductor devices' thermal behaviors. However, a high-order RC model usually led to high computational complexity and convergence problem in simulation. The temperature dependencies of the thermal conductivity and specific heat capacity in an RC model were often not included for simplicity.

2.4.3 Existing Electro-thermal Simulation

Over the years, numerous electro-thermal models (ETMs) have been developed and implemented into various simulators. A physics-based dynamic ETM for IGBT was developed in Saber by Hefner [126], predicting the IGBT electrical characteristic's temperature dependence and the dynamic self-heating. However, several physical model parameters were difficult to obtain. Furthermore, the model was extended to SiC MOSFET in LTspice [127] and SPICE [128]. Zarebski *et al.*[129] developed a large-signal ETM for a power MOS transistor in SPICE. Besides, a layer-based ETM for integrated PE modules in PSpice was proposed in [130] to consider short-circuit conditions [131]. Rajapakse *et al*. [132]-[133]

presented an ETM by deriving the power loss equations mathematically in the simulation. Hence, the device's heat generation and the heatsink's cooling performance were determined by solving differential equations. However, the TSEPs of IGBT were omitted, and the complicated mathematical equations were limited to specific applications.

Several ETMs were developed from the device level to large PE system applications to consider the impacts of parasitic circuit parameters on device behaviours. A lumped dynamic ETM for an IGBT module was proposed in [134] with a 3-D RC network and time-dependent average power losses. Further, Tang *et al*. [135] extended the model to paralleled IGBT modules. The relationships of power losses, junction temperature, and unbalanced parasitic elements were characterized to describe the interactions of current distributions and thermal dissipations between paralleled modules. However, it was challenging to implement the model in a large-scale PE simulation because of the complex FEM simulation. An electro-thermal analysis for a three-phase half-bridge two-level SiC power module was conducted in [136]. Shen *et al*. [137] applied the model to a complex power system using the parallel operation on a Field-Programmable Gate Array (FPGA) to reduce the time cost. Nevertheless, the switching transients and loss information were typically based on the datasheet. Thus it was suitable for large-scale system simulation with limited accuracy.

Apart from the common ETMs of IGBTs and MOSFETs, the counterparts for diodes and new GaN devices also have been developed recently. Mijlad *et al*. [138] introduced a diode ETM in SIMULINK, combining PIN diode's behavioral model with a fourth-order Foster network. However, experimental validation was not provided, and the diode's TSEPs were also not fully considered. An improvement of ETM from the behavioral model in [139] for the SiC MPS diode was achieved in [140], considering its junction capacitance. An ETM for GaN HEMT was recently proposed in [141], considering the trapping effect but mainly for RF applications. Besides, Wu *et al*.[142] demonstrated a simple behavioral ETM for GaN FET in SPICE, taking the self-heating and thermal effects into account.

2.5. Chapter Conclusion

This chapter provided a general overview of the state-of-the-art semiconductor modelling methodologies, power loss estimations, and electro-thermal simulation techniques. Initially, a brief introduction of different modern semiconductors was presented concerning the operating principles, static and dynamic characteristics. Furthermore, various semiconductor models, including device- and system-level models, were demonstrated. Comprehensive discussions were presented from various aspects in terms of complexity, accuracy and applicability. Concretely, a device-level model aimed to reproduce the device's switching behaviors with high accuracy. In contrast, a system-level model focused more on the device's basic functionality as a switch in the PE system to achieve fast simulation speed.

Moreover, a review of power loss estimation methods was illustrated with discussions on the advantages and disadvantages. Eventually, the electro-thermal related techniques, including TSEPs and thermal networks, were presented. Consequently, this chapter demonstrated the big picture of these semiconductor modelling research areas, and there was always a trade-off among accuracy, speed and applicability.

Chapter 3 A Behavioral Transient Model and Loss Simulation of IGBT-Diode Switching Cell

- A Part of the work presented in this chapter is the result of original work published under **Y. Xu**, C. N. M. Ho, A. Ghosh and D. Muthumuni, "An Electrical Transient Model of IGBT-Diode Switching Cell for Power Semiconductor Loss Estimation in Electromagnetic Transient Simulation," *IEEE Trans. Power Electrons*, vol. 35, no. 3, pp. 2979-2989, Mar. 2020.
- A Part of the work presented in this chapter is also the result of original work published under **Y. Xu**, C. N. M. Ho, A. Ghosh and D. Muthumuni, "A behavioral transient model of IGBT for switching cell power loss estimation in electromagnetic transient simulation," in *Proc. IEEE APEC*, Mar. 2018, pp. 270-275.

This chapter's main objective is to introduce a Silicon (Si) Insulated-Gate Bipolar Transistor (IGBT) behavioral model with a PIN diode for estimation power losses in Power Electronics (PE) systems. The proposed modelling process and power loss analytical equations are given in this chapter. The transient switching waveforms are also simulated, and the corresponding power losses Look-Up Table (LUTs) is further obtained. Besides, the model is implemented in PSCAD/EMTDC and experimentally verified. The details of the work are followed in the subsequent sections.

3.1. Introduction

Si IGBT is one of the most widely used devices among modern power switches, especially in medium-frequency PE applications ranging from medium to high power [143]. Typically, a converter can contain one IGBT, e.g. a boost converter [144], [145], to a few IGBTs, e.g. a full-bridge (FB) inverter [146], to tens of IGBTs, e.g. a Modular Multilevel Converter (MMC) [147]. An IGBT is typically paired with a diode in a PE converter to provide a current commutation for hard switching. This pair is called "Switching Cell" and configured with two structures, namely Negative-Cell and Positive-Cell, shown in Figure 3-1 [148]. The Positive-cell has the switching device connected to the positive voltage terminal and the common junction connected to the current source or inductor. On the other hand, the Negative cell's

switching device is connected to the voltage source's negative terminal. Notice that the switching device can be an IGBT, a Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) or other controlled devices. During switching transition, heat energy, due to switching losses, is generated in both the IGBT and the diode. The operating junction temperature (T_j) can vary widely over a long time, leading to fatigue failure and reduction in the reliability of the entire system [149].

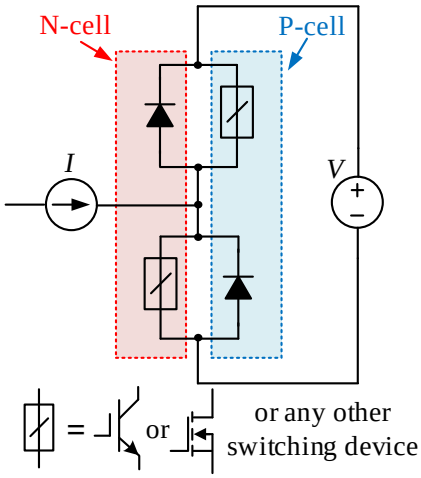


Figure 3-1 Diagram of the switching cell.

Therefore, an accurate model of IGBT with diode is highly desirable for PE converter design engineers, researchers and device manufacturers to study its dynamic behavior and estimate power losses. It is a primary technological booster for high power applications, increase efficiency, and optimize the overall system design.

Over the years, a great effort on IGBT modelling has been proposed. Physical models typically were based on the device physics and could obtain switching waveforms by solving physics equations. However, these models were generally complicated and limited in the device-level study, not to mention that the physical parameters usually were not attainable for PE engineers. In contrast, behavioral models could achieve fast simulation speed by ignoring the device physics and focusing on the external characteristics. Hence it was widely used for a rough loss estimation though the accuracy was typically sacrificed due to ignorance of the circuit parasitic elements. Besides, analytical models were developed by deriving the loss equations based on the equivalent circuits during the switching process. The effects of parasitic elements and other impacts such as Thermo-Sensitive Electrical Parameters (TSEPs) were considered to improve the accuracy. Nevertheless, a heavy computation burden along with

convergence issues hindered the models' applicability and performance. In summary, there is always a tradeoff between complexity, accuracy and speed.

3.2. Simulation Strategy

To provide fast speed and accurate IGBT loss estimation in a PE application, a simulation strategy is provided in Figure 3-2, including two stages, namely device- and system-level simulations. It is implemented in an electromagnetic transient (EMT) simulator (e.g. PSCAD/EMTDC). In the following, a detailed description of the strategy is presented.

3.2.1 Device-level Simulation

The device-level simulation aims to reproduce the switching waveforms of an IGBT and generate a multi-dimensional power loss LUT. Initially, the model parameters are extracted from the datasheet by curve fitting or empirical formulas. Afterwards, the IGBT behavioral transient model can simulate the switching waveforms, including gate-emitter voltage (v_{ge}), collector current (i_{c}) and collector-emitter voltage (v_{ce}) based on the input model parameters and circuit operating conditions. Subsequently, the power losses, including turn-on loss (E_{on}), turn-off loss (E_{off}), diode reverse recovery loss (E_{irr}) and conduction loss (p_{con}), are computed under different operating conditions, namely T_{j}, circuit voltage (V_{dd}) and inductive load current (I_{L}). The computed power losses can also be exported as a power loss LUT and extended for power loss estimation in a PE system simulation. Besides, the device-level simulation time-step is recommended to be set as nanoseconds (ns) for high accuracy.

3.2.2 System-level Simulation

The obtained power loss LUT in the device-level simulation works as an interface between the device- and circuit-level simulations. In the system-level simulation, the PE network is built in the PSCAD/EMTDC using the ideal switch model for power semiconductors under microseconds (μs) simulation time-step to achieve fast speed. During each switching action, the switch's instantaneous T_{j}, V_{dd}, and I_{L} are input to the power loss LUT. Subsequently, additional instantaneous power loss information is obtained. Note that this information is independent of the PE network. It is a simple search method and will not significantly increase the additional time than the typical PE simulation using an ideal switch.

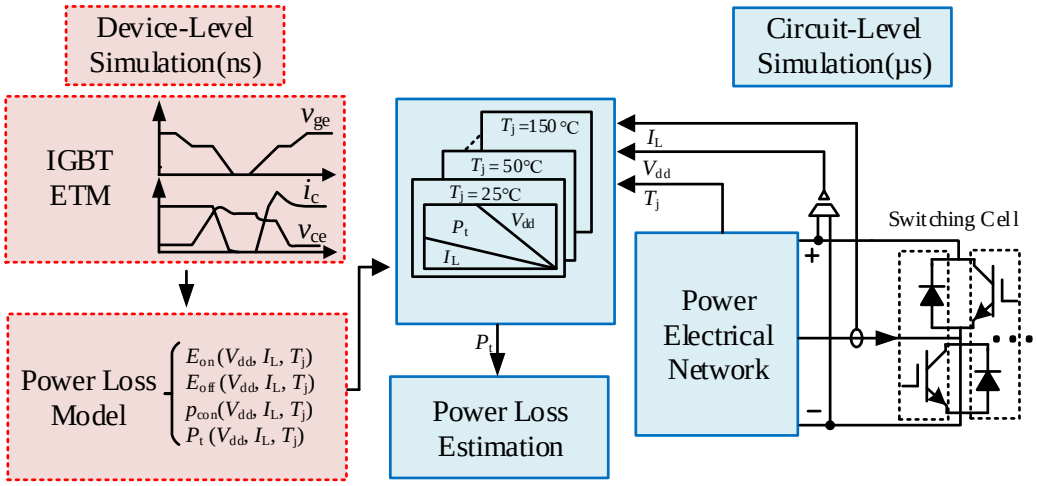
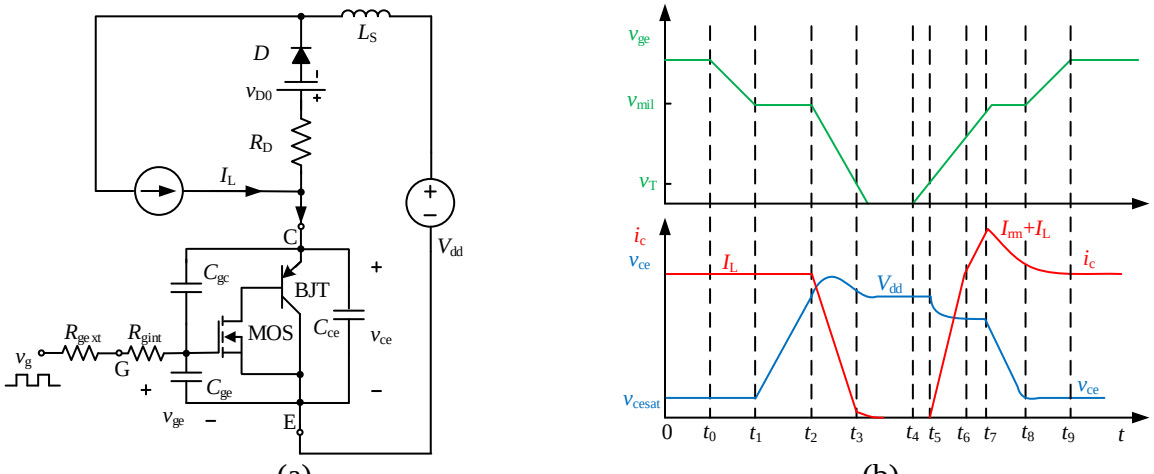


Figure 3-2 Block diagram of the simulation strategy.

3.3. Model Description

A diode-clamped inductive load test circuit in Figure 3-3 (a) is used to investigate the IGBT's dynamic behavior. The typical switching waveforms of an IGBT are demonstrated in Figure 3-3 (b). An IGBT is generally configured as a Darlington structure by a MOS channel, a Bipolar Junction Transistor (BJT) and the junction capacitances, including gate-collector capacitance (C_{gc}), gate-emitter capacitance (C_{ge}) and collector-emitter capacitance (C_{ce}). A gate drive voltage (v_g) is provided to control the switch through a gate resistance (R_G) which consists of the external gate resistance (R_{gext}) and the internal gate resistance (R_{gint}). In addition, the PIN diode is represented by an ideal diode (D) in series with a forward resistance (R_D) and a diode threshold voltage (v_{D0}). Also stray inductance (L_S) is considered in the circuit.



(a) (b)

Figure 3-3 IGBT switching cell (a) equivalent circuit, and (b) typical switching waveforms.

3.3.1 Switching Process Analyses and Modelling.

- **Turn-on period (t_4~t_9)**

At t_4 in Figure 3-3(b), a turn-on gate voltage (V_{gon}), typically 15V for Si IGBT case, is given as v_{g} through R_{G} to charge the input capacitance (C_{iss}=C_{gc}+C_{ge}). Subsequently, v_{ge} starts rising which is approximated by a first-order RC circuit. The corresponding time constant of v_{ge} is $\tau_{\mathrm{g}} = R_{\mathrm{G}} \cdot C_{\mathrm{iss}}$. Accordingly the gate current (i_{g}) is expressed as,

$$i_{\mathrm{g}} = C_{\mathrm{iss}} \cdot \frac{\mathrm{d}v_{\mathrm{ge}}}{\mathrm{d}t} = \frac{v_{\mathrm{g}} - v_{\mathrm{ge}}}{R_{\mathrm{G}}}. \tag{3.1}$$

Once v_{ge} crosses the turn-on threshold voltage (v_{T}), the conductive channel is built, and the conduction current mainly is controlled by v_{ge} and v_{ce}. Concretely, the IGBT's static characteristic in the regions of cut-off, active and saturation is expressed by the following equations, where i_{IGBT} is the equivalent current flowing through the MOS channel and BJT. Instead of using the typical trans-conductance g_{fs} in MOS and current gain (β) in BJT, the equivalent trans-conductance K_{IGBT} is used, which equals to $(1+\beta) \cdot g_{\mathrm{fs}}$. Both K_{IGBT} and v_{T} are extracted directly from the output and transfer curves in the datasheet [150].

$$i_{\mathrm{IGBT}} = \begin{cases} 0, v_{\mathrm{ge}} < v_{\mathrm{T}} \\ K_{\mathrm{IGBT}} \cdot \left(v_{\mathrm{ge}} - v_{\mathrm{T}} - 0.5 \cdot v_{\mathrm{ce}}\right) \cdot v_{\mathrm{ce}}, v_{\mathrm{ce}} \le v_{\mathrm{ge}} - v_{\mathrm{T}}. \\ 0.5 \cdot K_{\mathrm{IGBT}} \cdot \left(v_{\mathrm{ge}} - v_{\mathrm{T}}\right)^2, v_{\mathrm{ce}} > v_{\mathrm{ge}} - v_{\mathrm{T}} \end{cases} \tag{3.2}$$

As i_{IGBT} rises to I_{L}, there is a voltage drop (v_{L}) on the L_{S} and thus the v_{ce} during this interval is expressed by,

$$v_{\mathrm{ce}} = V_{\mathrm{dd}} - v_{\mathrm{L}} = V_{\mathrm{dd}} - L_{\mathrm{S}} \cdot \frac{\mathrm{d}i_{\mathrm{c}}}{\mathrm{d}t}. \tag{3.3}$$

As for the nonlinear parasitic capacitances in IGBT, C_{gc} is a voltage-dependent capacitance. It increases significantly as v_{ce} declines according to the capacitance curve and gate charging curve in the datasheet. Consequently, most of the charging i_{g} flows to C_{gc} , instead of C_{ge}. v_{ge}, as a result, is clamped at the miller plateau, as shown in Figure 3-3 (b) ($t_1 - t_2$ and $t_7 - t_8$). During these periods, the IGBT keeps conducting and operates in the saturation region. Hence, v_{mil} is expressed as,

$$v_{\mathrm{mil}} = \sqrt{2 \cdot I_{\mathrm{L}} / K_{\mathrm{IGBT}}} + v_{\mathrm{T}}. \tag{3.4}$$

As I_{L} commutates from the low-side IGBT to the up-side diode, the diode current i_{F} drops accordingly to zero. Since there are minority carriers stored on both sides of the PN junction, the diode cannot switch off immediately. In fact, once i_{IGBT} reaches I_{L}, the diode starts entering into the reverse recovery period ($t_6 - t_8$), as shown in Figure 3-3 (b). The corresponding diode curves are presented in Figure 3-4. i_{F} is the diode forward conducting current and it decreases with the slew rate of $\mathrm{d}i_{\mathrm{F}}/\mathrm{d}t$. In addition, t_{rr} and Q_{rr} are the reverse recovery time and charge respectively. When i_{F} decreases to zero and enters into reverse recovery at t_{re}, it continues decreasing with almost same decline rate. Once i_{F} reaches the reverse peak I_{rm} at t_{rm}, it starts decay with the time constant (τ_{re}). It is assumed that this period ends when i_{F} bellows 10% of I_{rm}. To represent this diode's reverse recovery characteristic, an additional equivalent dependent current source (i_{re}) is used and it is expressed as,

$$i_{\mathrm{re}} = \begin{cases} \frac{\mathrm{d}i_{\mathrm{F}}}{\mathrm{d}t} \cdot (t - t_{\mathrm{re}}), t_{\mathrm{re}} < t < t_{\mathrm{rm}} \\ I_{\mathrm{rm}} \cdot e^{-\frac{t - t_{\mathrm{rm}}}{\tau_{\mathrm{re}}}}, t > t_{\mathrm{rm}} \end{cases} . \tag{3.5}$$

This diode's reverse recovery behavior results in a current bump to i_{c} with additional losses. The diode parameters are computed from the device datasheet [151].

$$\begin{cases} \tau_{\mathrm{re}} = \frac{1}{\ln 10} \cdot (t_{\mathrm{rr}} - I_{\mathrm{rm}}/(\mathrm{d}i_{\mathrm{F}}/\mathrm{d}t)) \\ I_{\mathrm{rm}} = \sqrt{Q_{\mathrm{rr}} \cdot \mathrm{d}i_{\mathrm{F}}/\mathrm{d}t} \\ t_{\mathrm{rr}} = 2 \cdot \sqrt{Q_{\mathrm{rr}}/(\mathrm{d}i_{\mathrm{F}}/\mathrm{d}t)} \end{cases} . \tag{3.6}$$

As soon as i_{F} reaches I_{rm}, v_{F} transfers from positive to negative and v_{ce} decreases to v_{cesat} simultaneously. Meanwhile, v_{ge} continues climbing to V_{gon}.

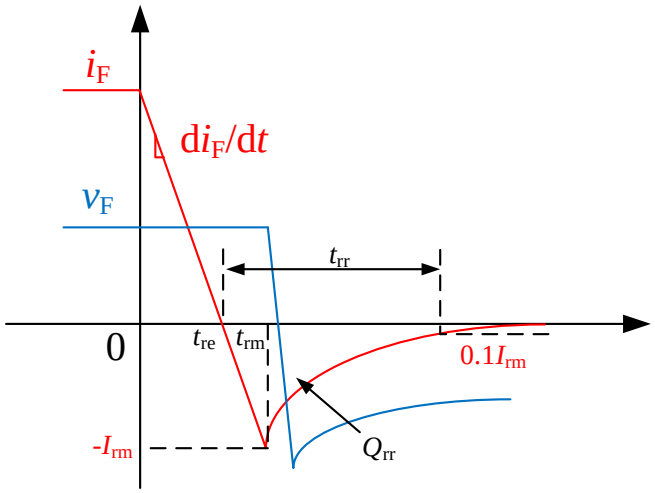


Figure 3-4 The diode's reverse recovery characteristic [151].

- **Turn-off period ($t_0 - t_3$)**

The turn-off process is almost the inverse sequence of the turn-on process, except for the current tailing period. The turn-off gate signal (V_{goff}), typically 0V for IGBT, is provided at t_0. Subsequently, v_{ge} starts decreasing. Meanwhile v_{ce} starts rising with the slew rate as

$$\frac{\mathrm{d}v_{\mathrm{ce}}}{\mathrm{d}t} = \frac{v_{\mathrm{G}} - v_{\mathrm{mil}}}{R_{\mathrm{G}} \cdot C_{\mathrm{gc}}}. \tag{3.7}$$

During this voltage transition period, v_{ge} keeps at v_{mil} again and thus i_{c} maintains at I_{L} level. Once v_{ce} reaches V_{dd}, I_{L} begins commutating from the IGBT to the diode, and i_{c} starts decreasing, similar to the turn-on process. During this current transition interval, the effect of excess base carrier recombination in the IGBT prolongs the turn-off time resulting in extra power losses. Typically this tail current (i_{tail}) is described approximately by the exponential function,

$$i_{\mathrm{tail}} = I_{\mathrm{tail0}} \cdot e^{-\frac{t - t_{\mathrm{tail0}}}{\tau_{\mathrm{tail}}}}, \tag{3.8}$$

where I_{tail0} and t_{tail0} are the collector current at the beginning of the tail stage and the corresponding time. τ_{tail} is the carrier transit time constant.

3.3.2 Temperature Sensitivity Consideration

TSEPs, as mentioned previously, are today widely used for the measurement of T_{j}. As T_{j} changes, the corresponding parameters of an IGBT, such as on-state voltage (v_{cesat}), v_{T}, and τ_{tail}, will also change, affecting the dynamic behavior of the IGBT. Hence these parameters should also be under consideration. A series of analytical equations are provided to describe the TSEPs in the IGBT and the diode. All the equations are based on the experimental measurements and curve-fitting as a function of temperature and various coefficients [152].

$$v_{\mathrm{T}} = V_{\mathrm{T0}} - k_{\mathrm{T}} \cdot (T_{\mathrm{j}} - T_{\mathrm{a}}). \tag{3.9}$$

$$K_{\mathrm{IGBT}} = K_0 \cdot (T_{\mathrm{a}}/T_{\mathrm{j}})^{0.8}. \tag{3.10}$$

$$\tau_{\mathrm{tail}} = 5 \times 10^{-7} \cdot (T_{\mathrm{a}}/T_{\mathrm{j}})^{1.5}. \tag{3.11}$$

$$v_{\mathrm{cesat}} = (V_{\mathrm{cesat0}} + r_0 i_{\mathrm{c}}) + (\Delta V_{\mathrm{cesat}} + \Delta r_0 i_{\mathrm{c}})\big(T_{\mathrm{j}} - T_{\mathrm{a}}\big). \tag{3.12}$$

$$I_{\mathrm{rm}} = I_{\mathrm{rm0}} + t_{\mathrm{rm0}} \frac{\mathrm{d}i_{\mathrm{F}}}{\mathrm{d}t} + \left(K_{\mathrm{rm}} + K_{\mathrm{trm}} \cdot \frac{\mathrm{d}i_{\mathrm{F}}}{\mathrm{d}t}\right)\big(T_{\mathrm{j}} - T_{\mathrm{a}}\big). \tag{3.13}$$

$$Q_{\mathrm{rr}} = Q_{\mathrm{rr0}} + t_{\mathrm{Qrr}} \frac{\mathrm{d}i_{\mathrm{F}}}{\mathrm{d}t} + \left(K_{\mathrm{rr}} + K_{\mathrm{Q_{rr}}} \cdot \frac{\mathrm{d}i_{\mathrm{F}}}{\mathrm{d}t}\right)\big(T_{\mathrm{j}} - T_{\mathrm{a}}\big). \tag{3.14}$$

Table 3-1TSEPs of the IGBT and the diode.

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
V_{T0}	5.812	k_{T}	0.01	K_0	2.834	V_{cesat0}	0.9715
r_0	0.022	$\Delta V_{\mathrm{cesat}}$	-0.001	Δr_0	0.0001	I_{rm0}	17.77
t_{rm0}	0.0123	K_{rm}	0.041	K_{trm}	0.000035	Q_{rr0}	3.602
t_{Qrr}	0.0003	K_{rr}	0.03	K_{Qrr}	0.0000072	T_{a}	25℃

Where V_{T0}, k_{T}, K_0, V_{cesat0}, r_0, $\Delta V_{\mathrm{cesat}}$, Δr_0 are the IGBT fitting coefficients and T_{a} denotes the ambient temperature. Also, I_{rm0}, t_{rm0}, K_{rm}, K_{trm}, Q_{rr0}, t_{Qrr}, K_{rr}, K_{Qrr} are the diode fitting constants. All the curve fitting parameters are obtained from the datasheet. The TSEPs of the model for IGBT (IKW40T120) from Infineon, as an example, were extracted from the datasheet using MATLAB. The parameter results were listed in Table 3-1.

3.3.3 Behavioral Model Circuit of IGBT

A Si IGBT consists of an N-channel MOSFET and a PNP BJT. Its base current is controlled by the MOSFET's gate voltage, as shown in Figure 3-3 (a) previously. Based on that, the schematic of the behavioral IGBT model is illustrated in Figure 3-5. In the gate loop, the nonlinear capacitances are merged as C_{iss} in parallel with an equivalent dependent voltage source, especially for miller plateau. In the power loop, the IGBT's static and dynamic characteristics are represented by the equivalent dependent current source i_{IGBT} and the voltage source v_{IGBT}. Concretely, during switching transients, the change of i_{c} is reflected by i_{IGBT} and likewise, the change of v_{ce} including v_{cesat} for the on-state is realized by v_{IGBT}. Furthermore, the PIN diode is modelled by an ideal diode in series with R_{D} and V_{D0}. Additionally, the diode's reverse recovery behavior is also realized by the equivalent dependent current source i_{re}. This model circuit is implemented in PSCAD/EMTDC, including the main circuit, user-defined programmed modules and other control components. TSEPs are updated and calculated based on the input operating conditions. The IGBT's nonlinear features and the body diode's reverse recovery characteristic are modelled using FORTRAN to control the voltage and current source, respectively. Thus, the transient waveforms of the switching cell are simulated. The switching time and other transient parameters are obtained and extended to the power loss calculation model.

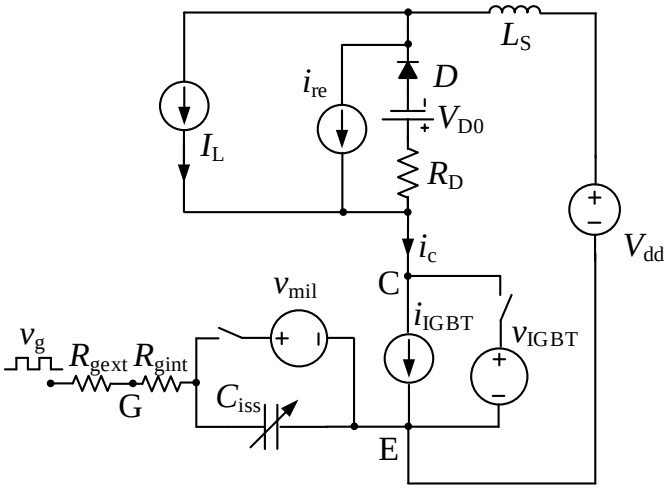


Figure 3-5 The behavioral model circuit of IGBT.

3.4. Power Loss Analyses

Once the transient switching waveforms are obtained in the IGBT behavioral model circuit, power loss analyses are conducted. For simplicity, in Figure 3-3(b), the voltage and current are assumed piecewise linearly changing except for the diode reverse recovery and tailing current periods. The tailing time t_{tail} is defined as the time interval when i_{c} decreases from 10% I_{L} to 1% I_{L}. In addition, the diode reverse recovery decay interval is relatively short. Thus the corresponding loss is neglected in this work. All the parameters in the following analytical equations for each switching sub-stages are obtained simultaneously in the IGBT model simulation [153].

The primary power losses during IGBT switching transients include turn-on current loss (E_{oni}), turn-on voltage loss (E_{onv}), diode reverse recovery loss (E_{irr}), turn-off current loss (E_{offi}), turn-off voltage loss (E_{offv}) and IGBT tail current loss (E_{tail}). The detailed analysis is provided as follows.

3.4.1 Turn-off Loss Analysis

In the interval from t_1 to t_3, v_{ce} rises from 0 to V_{dd}, meanwhile i_{c} keeps almost constant as I_{L}. Hence, power loss during this period is given by,

$$E_{\mathrm{offv}} = I_{\mathrm{L}} \cdot V_{\mathrm{dd}} \cdot t_{\mathrm{offv}}, \tag{3.15}$$

where t_{offv} is the corresponding transition time.

Once v_{ce} reaches V_{dd}, the current falling period begins. During the interval $[t_2, t_3]$, a voltage drop is applied on L_{S} due to the change of current and thus the power loss is,

$$E_{\mathrm{offi}} = I_{\mathrm{L}} \cdot V_{\mathrm{dd}} \cdot t_{\mathrm{offv}}/2 + L_{\mathrm{S}} \cdot I_{\mathrm{L}}^2/2. \tag{3.16}$$

With the assumption that the tail current starts at 10% of I_{L} and τ_{tail} equals to $t_{\mathrm{tail}}/\ln 10$, the corresponding tail loss is estimated as,

$$E_{\mathrm{tail}} = V_{\mathrm{dd}} \cdot \int_0^{t_{\mathrm{tail}}} I_{\mathrm{tail0}} \cdot e^{-\frac{t}{\tau_{\mathrm{tail}}}} \mathrm{d}t = 0.456 \cdot I_{\mathrm{L}} \cdot V_{\mathrm{dd}}/t_{\mathrm{tail}}. \tag{3.17}$$

3.4.2 Turn-on Loss Analysis

Likewise, the turn-on power losses have resulted during the interval $[t_5, t_8]$. Initially, i_{c} rises from 0 to I_{L}, meanwhile v_{ce} keeps almost constant with a voltage drop on L_{S}. Hence, the power loss for the interval $[t_5, t_6]$ is expressed as

$$E_{\mathrm{oni}} = I_{\mathrm{L}} \cdot V_{\mathrm{dd}} \cdot t_{\mathrm{oni}}/2 - L_{\mathrm{S}} \cdot I_{\mathrm{L}}^2/2. \tag{3.18}$$

Assuming that i_{c} equals to I_{L} during the voltage falling period from t_7 to t_8. At the same time, v_{ce} drops to v_{cesat} and thus the power loss during this period is computed by

$$E_{\mathrm{onv}} = I_{\mathrm{L}} \cdot V_{\mathrm{dd}} \cdot t_{\mathrm{onv}}/2. \tag{3.19}$$

As for the diode reverse recovery loss during the period t_{rr}, it is relatively short compared with the voltage falling period. Hence, the power loss is calculated by,

$$E_{\mathrm{irr}} = (V_{\mathrm{dd}} - L_{\mathrm{S}} \cdot I_{\mathrm{L}}/t_{\mathrm{oni}}) \cdot (I_{\mathrm{L}} \cdot (t_{\mathrm{rm}} - t_{\mathrm{re}}) + Q_{\mathrm{rr}}). \tag{3.20}$$

3.4.3 Conduction Loss Analysis

From the output characteristics of IGBT and diode in the datasheet, v_{cesat} is represented in terms of an on-state threshold voltage V_{ce0} and an equivalent resistance r_{c},

$$v_{\mathrm{cesat}} = V_{\mathrm{ce0}} + r_{\mathrm{c}} \cdot i_{\mathrm{c}}. \tag{3.21}$$

If the average current is I_{cav} and the root-mean-square value is I_{crms}, then the average conduction loss of IGBT (p_{con}) is expressed as follows, where f_{sw} is the switching frequency.

$$p_{\mathrm{con}} = f_{\mathrm{sw}} \int_0^{1/f_{\mathrm{sw}}} v_{\mathrm{ce}} \cdot i_{\mathrm{c}} \mathrm{d}t = V_{\mathrm{ce0}} \cdot I_{\mathrm{cav}} + r_{\mathrm{c}} \cdot I_{\mathrm{crms}}^2. \tag{3.22}$$

The total switching losses E_{ts} is estimated as the sum of the loss equations above,

$$E_{\mathrm{ts}} = E_{\mathrm{offv}} + E_{\mathrm{offi}} + E_{\mathrm{tail}} + E_{\mathrm{oni}} + E_{\mathrm{onv}} + E_{\mathrm{irr}}. \tag{3.23}$$

Noted that, V_{dd} and I_{L} are the keys affecting the power losses. Besides, the effects of diode reverse recovery current, L_{S} and i_{tail} should also be considered, especially for HF applications.

3.5. Experimental Verification

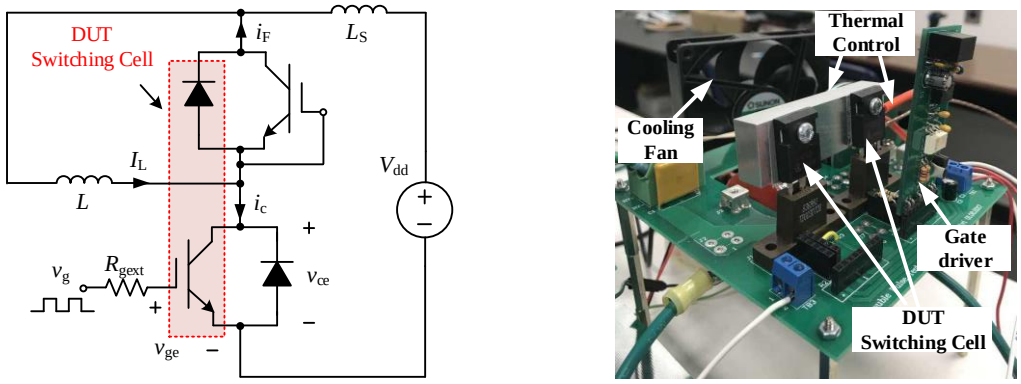
The IGBT-diode switching cell's behavioral model and the power loss estimation method were implemented in PSCAD/EMTDC and validated by comparing with the experimental results from a DPT bench and a boost converter application. This method's key objective is to predict the device's power dissipation in a PE system simulation. The selected IGBT device's model parameters are initially extracted from the device datasheet by curve fitting or empirical formula as discussed previously. Afterwards, the device-level simulation runs with ns time-step multiple times based on the operating conditions' required range. Subsequently, the power loss information based on the simulated waveforms is obtained, exported and reformatted as a LUT for further power loss estimation in a PE system simulation.

3.5.1 Device-level Verification

According to the circuit in Figure 3-6 (a), a DPT bench was designed and implemented to characterize the devices [154]. The test setup consisted of a power supply, a Digital Signal Processing (DSP) control system, a thermal control system, a cooling fan and the devices under test (DUTs), as shown in Figure 3-6 (b). A thermocouple was placed between the heatsink and the DUTs to measure the temperature. Through the thermocouple amplifier AD595, the temperature value was further read by the analog pin of DSP. The temperature in the DPT was controlled by the DSP controller, cooling fan and the heater attached to the heatsink. A thermal imager (Fluke, Tis40) was used in the DPT to monitor the device's junction temperature. Tektronix High-voltage differential probe THDP0200, current probe TCP0030A, and the 350MHz oscilloscope MSO5034B were used to capture the switching waveforms.

Table 3-2 Key parameters of the device and testbed.

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
R_{gint}	6Ω	C_{iss}	2500pF	v_{T}	5.8V	C_{rss}	110pF
K_{IGBT}	2.83 $\mathrm{A/V^2}$	R_{gext}	15Ω	V_{dd}	0-1kV	L	5mH
I_{L}	0-80A	L_{S}	180nH	v_{cesat}	1.7V	v_{g}	15V/0V

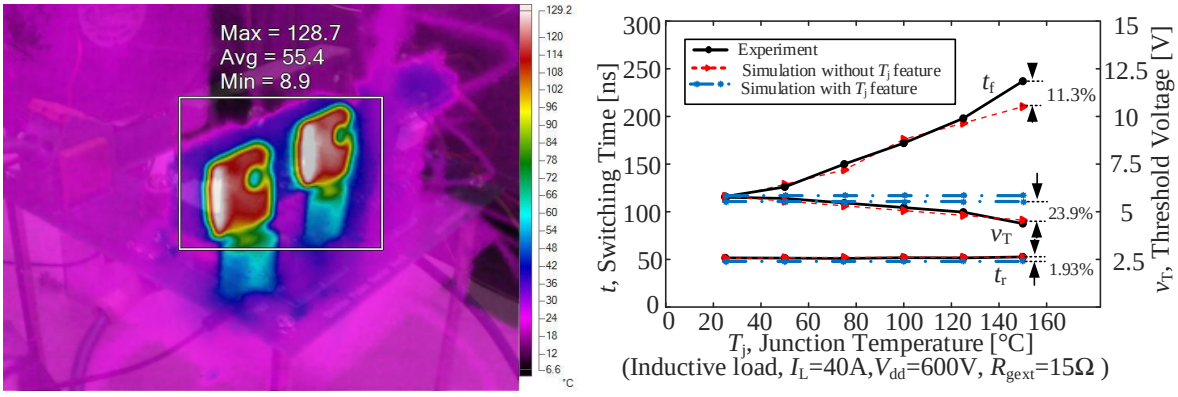


(a) (b)

Figure 3-6 Loss evaluation setup, (a) circuit schematic, (b) DPT bench.

The Infineon IKW40T120 IGBT device (TO-247 package) was chosen as the DUT. The critical parameters of the model and the test bench are listed in Table 3-2. The capacitors are initially charged to the desired voltage level. Subsequently, the DSP gives the gate signal to test the switching cell. The transient switching waveforms are captured by oscilloscope.

To study the temperature-dependent features, the operating T_j of DUT is controlled by the thermal system and monitored by a thermal imager to the desired test condition, as shown in Figure 3-7(a). As the T_j increases, the TSEPs are changing and affecting the dynamic behavior of the switching cell. As a result, the turn-on and turn-off time (t_r and t_f) and v_T change accordingly as shown in Figure 3-7(b). Since the traditional model only considers the specific operating conditions, it cannot represent the dynamic changes in various T_j resulting in deviations. The simulation results with the temperature feature show a good agreement with the experimental results. As T_j change from 25℃ to 150℃, t_f increases more than two times, while t_r increases slightly. In contrast, v_T declines slightly as T_j rises to 150℃.



(a) (b)

Figure 3-7 (a) Thermal image of DUT in DPT, (b) Switching time and v_T Vs T_j.

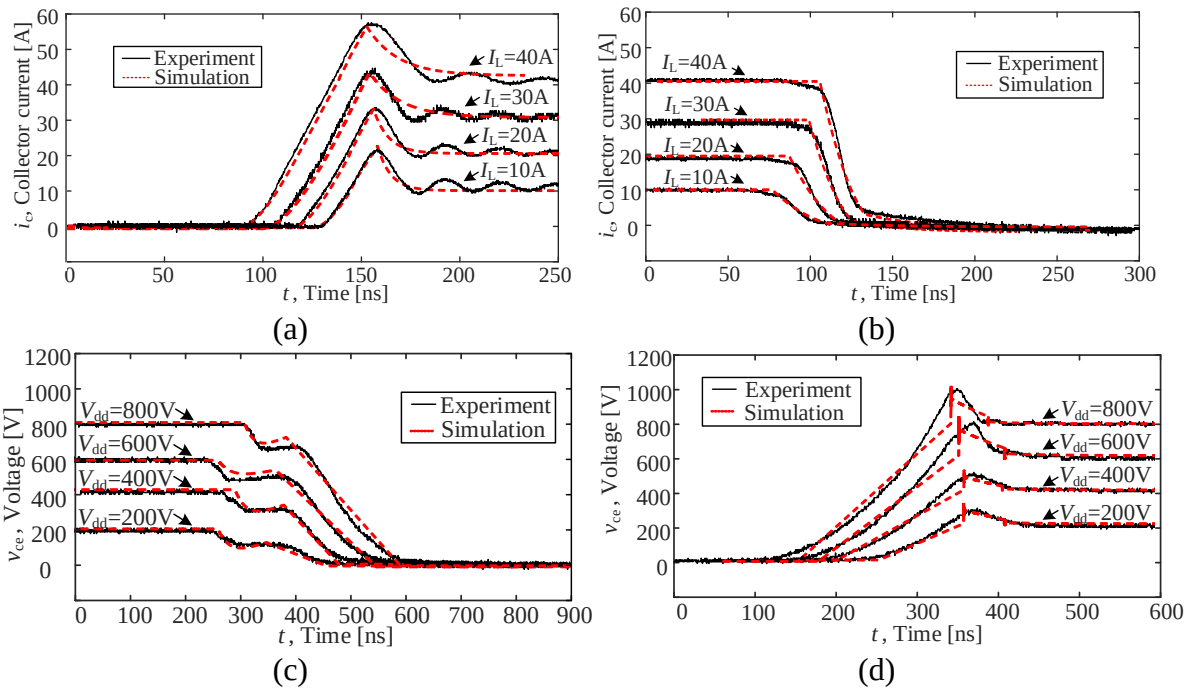


Figure 3-8 (a) turn-on i_c; (b) turn-off i_c; (c) turn-on v_{ce}; (d) turn-off v_{ce}@ 150℃, 15Ω.

The IGBT's switching waveforms are illustrated in Figure 3-8 under the test conditions of 150℃ T_j and 15Ω R_{gext}. The simulated results are compared with the measurements in the DPT, and good agreements are achieved. Concretely, the switching details such as transient spikes, tail current, diode behavior, and the parasitic elements' impacts are observed. Note that there are some current oscillations after the IGBT completely turns on. These oscillations mainly result from the resonance of the testbed's parasitic inductances, which is not considered in the model for simplicity. In fact, during these oscillations, v_{ce} maintains at v_{cesat}, which is relatively low level. Thus the resulting power loss is not significant.

The computed power losses results are also compared with the measured results by integrating the product of measured v_{ce} and i_c during the switching process in Figure 3-9. A series of V_{dd} and I_L are set to obtain the power loss LUT by the multiply-run function in PSCAD. Notice that the switching losses and the proportion of E_{on} and E_{off} change accordingly, as V_{dd}, I_L and T_j increase. The simulation results have reasonable accuracy with the variations of V_{dd} and I_L. The average errors are within an acceptable range (below 10%). Figure 3-9 (d) shows an example of a 3-D plot of losses. Although only one layer for the condition of 25℃ is graphically demonstrated, multiple layers with various T_j are generated in the simulator. A multi-dimensional table is stored and ready for circuit simulations.

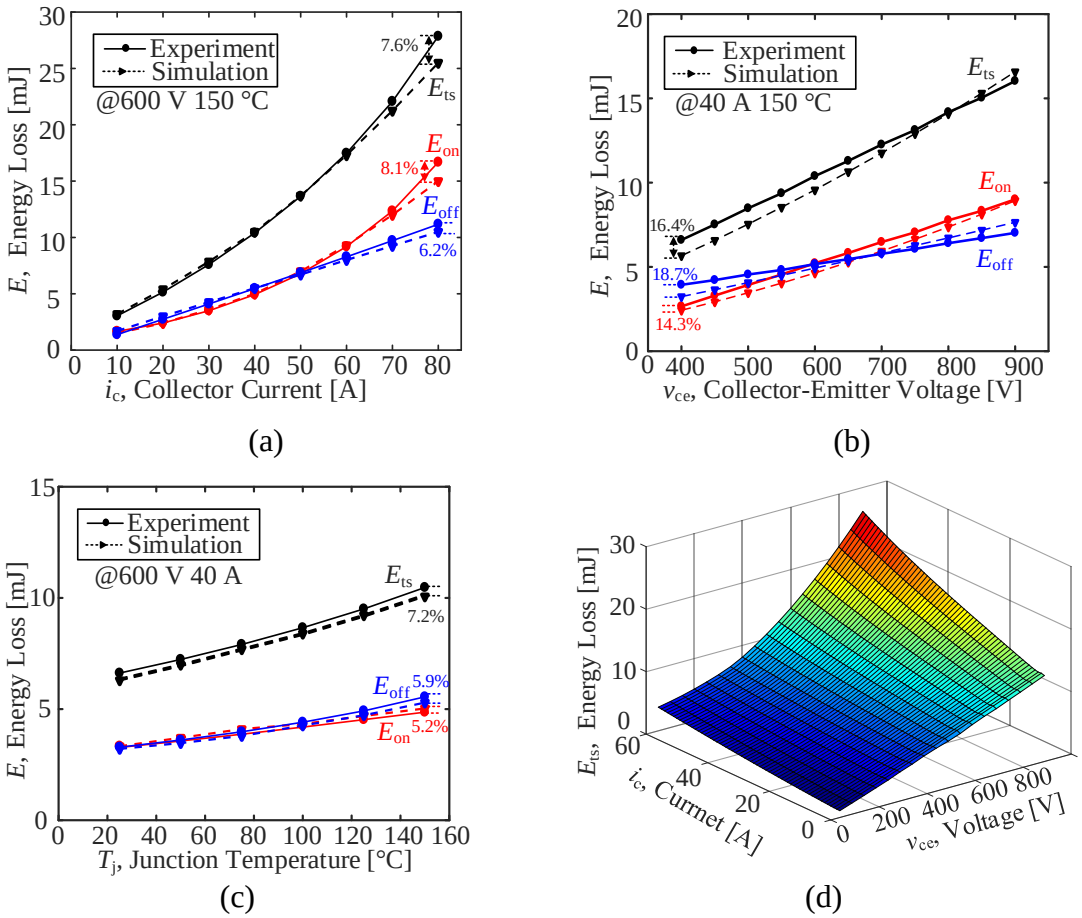


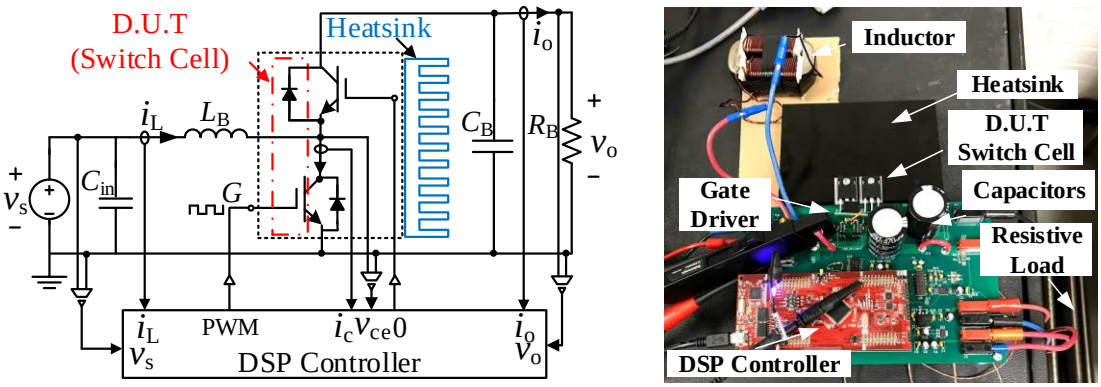
Figure 3-9 IGBT switching energy loss (a) vs i_c, (b) vs v_{ce}, (c) vs T_j, (d) 3-D LUT@15Ω.

3.5.2 System-level Verification

The obtained power loss LUT is applied to various PE applications such as buck or boost converter for device loss estimation. Hence, a boost converter in Figure 3-10 (a) was implemented in PSCAD and built with a cooling system, as shown in Figure 3-10 (b). The designed boost converter setup includes the main circuit board, DC power supply, oscilloscope, resistive load and other measure equipment. The same semiconductor, Infineon IKW40T120 IGBT, is used for testing. Wakefield-Vette 394-2AB heat sink is chosen as the cooling system. The main parameters of the testbed are listed in Table 3-3.

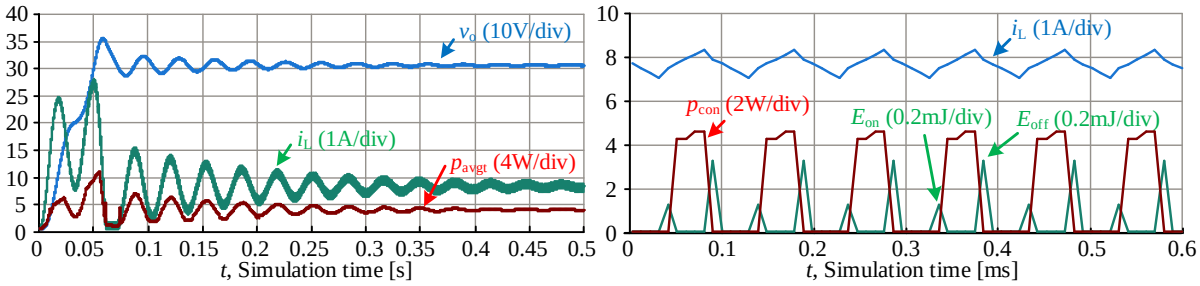
Table 3-3 Key parameters of the boost converter.

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
v_s	150V	v_o	300V	L_B	7.17mH	C_B	940μF
R_B	77Ω	f_{sw}	10kHz	D	0.5	R_{gext}	15Ω



(a) (b)

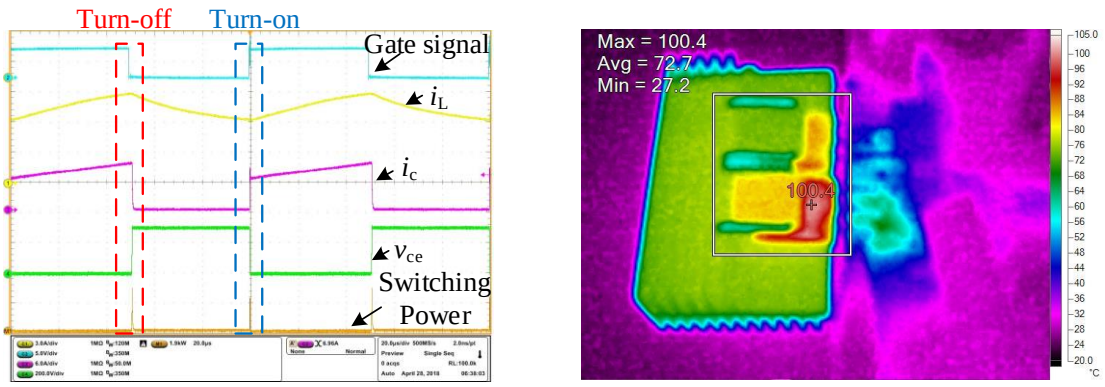
Figure 3-10 Boost converter setup, (a) block diagram, and (b) testbed.



(a) (b)

Figure 3-11 System simulation (a) overall performance, and (b) detail loss information.

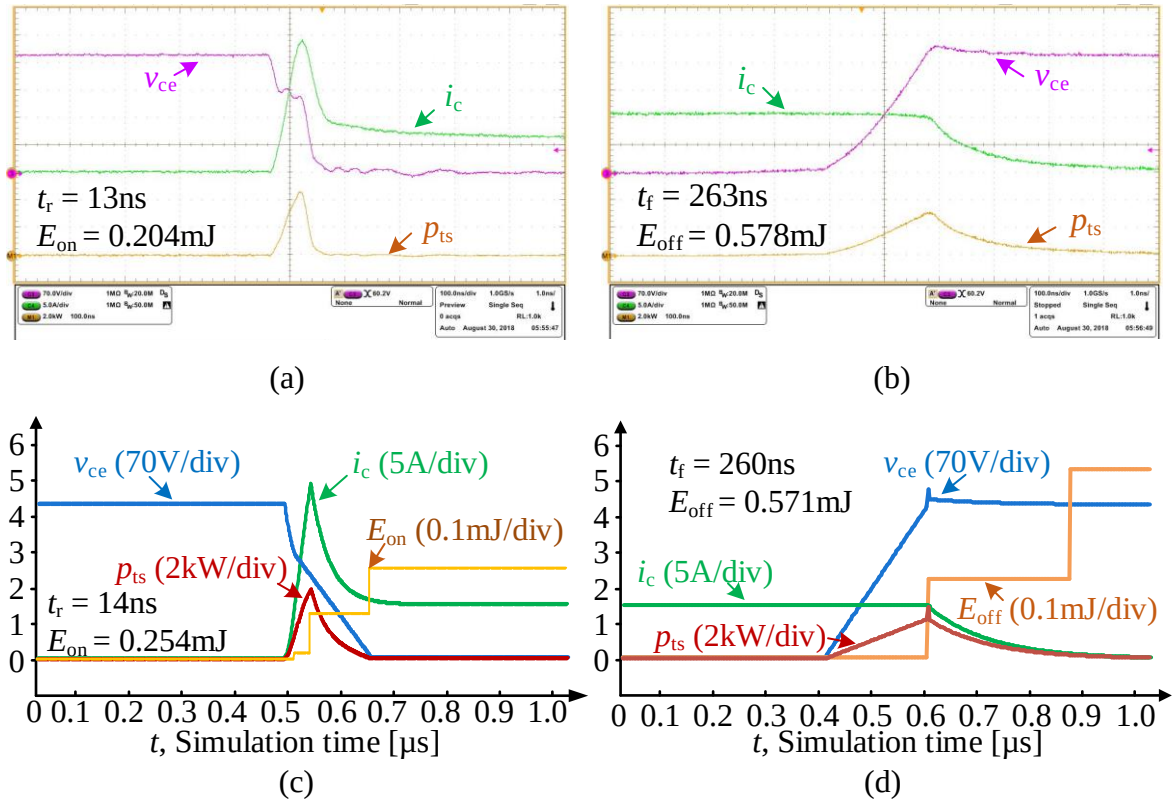
The experiments were conducted at various voltages with a fixed 10kHz switching frequency controlled by DSP. The same circuit and conditions were simulated in PSCAD/EMTDC using an ideal switch with an additional power loss LUT under the typical μs time-step. The overall system performance waveforms and the details of power loss estimation in the simulation are shown in Figure 3-11. It is observed that the detailed power losses, including E_{on}, E_{off} and p_{con} are well estimated during each switching cycle. Concretely, Figure 3-11(a) shows the start-up transient waveforms in the PSCAD simulation. As the output voltage (v_{o}) and instantaneous current (i_{L}) reach steady-state, there is a current ringing in i_{L} during the switching transients. The average power (p_{avgt}) denotes the average power loss of power semiconductor in one switching cycle. The instantaneous p_{avgt} is estimated and change accordingly. Figure 3-11 (b) demonstrates the simulated losses in a switching cycle scale for the IGBT. During each switching cycle, E_{on} and E_{off} are obtained from the power loss LUT based on the instantaneous operating conditions at the beginning and the end of the switching cycle, respectively. Likewise, p_{con} is obtained and updated based on the operating conditions which validates the power loss estimation method.



(a) (b)

Figure 3-12 (a) Measured overall system waveforms; (b) thermal image.

Figure 3-12 (a) illustrates the measured overall system waveforms in the boost converter test bench, and the device temperature was monitored by a thermal imager, as shown in Figure 3-12 (b). The switching power p_{ts} is obtained by the product of v_{ce} and i_c using MATH function in oscilloscope. Subsequently, p_{ts} is exported and integrated for power loss computation. It is observed that p_{ts} keeps in a low level during on- and off-state while a significant increase of p_{ts} occurs during each switching transient.



(a) (b)

(c) (d)

Figure 3-13 Measured results (a) on-state; (b) off-state; Simulated results (c) on-state; (d) off-state.

Furthermore, the detailed turn-on and turn-off waveforms of the IGBT were captured by an oscilloscope, as shown in Figure 3-13 (a) and (b), respectively. The transient waveforms under the same test conditions in PSCAD/EMTDC are shown in Figure 3-13(c) and (d) to verify the proposed approach's accuracy. Notice that the overlap of v_{ce} and i_c during switching process correspond to E_{on} and E_{off}, which are significant, especially for high-frequency applications. It is observed that the simulated results agree with the experimental results in terms of the dynamic switching time and the switching losses.

Besides, the simulated power loss results for different v_o are compared with the measured results and the estimated results by curve fitting the loss curves in the device datasheet as shown in Figure 3-14(a). It is observed that significant loss deviations are found in the curve fitting results, especially E_{on}. The deviations result from the limited range of the loss information provided in the datasheet. A simple linear estimation of the loss can also result in considerable deviations, especially for low voltage or low current range. In contrast, the results by the proposed method match well with the measured results in a wide range of v_o which validates the proposed approach. Moreover, Figure 3-14 (b) illustrates the switching loss results for different T_j. The traditional curve fitting method is only linearly scaled of the effects of temperature and other conditions. The proposed results show better agreements with the experimental and curve-fitted results in a wide range of operating conditions. Generally, the overall power losses, including E_{on} and E_{off}, increase slightly as T_j rises to 100℃. It should be mentioned that the power losses are analytically estimated by the additional loss table and will not affect the electrical circuit simulation.

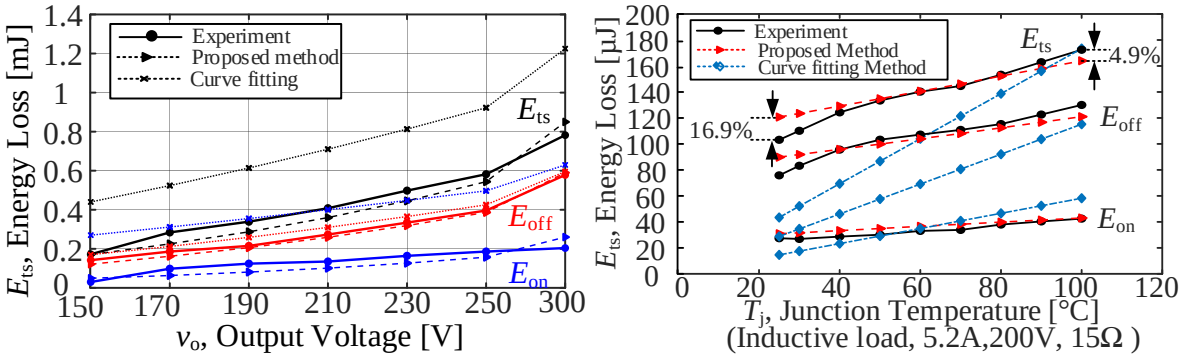


Figure 3-14 Switching loss of boost converter (a) vs v_o; (b) vs T_j

3.5.3 Discussion

- **Applicability and Limitation**

The proposed model is applied to an EMT simulator with user-defined functions (e.g. PSCAD/EMTDC, MATLAB/Simulink). The modelling approach, including the parameter extraction sequence and the power loss estimation method, applies to various Si IGBT devices and other types such as MOSFET and GaN devices with necessary modifications. Nevertheless, the displacement current caused by charging and discharging the nonlinear capacitances during voltage transition is neglected for simplicity. Besides, T_j is considered a given constant value. The internal common source inductance effect is not fully considered, negatively influencing the gate loop and affecting the switching time.

- **Efficiency**

As for the efficiency of the model, it is a tradeoff between accuracy and speed. The device simulation is recommended to run under the ns simulation time-step for reasonable accuracy. Therefore, the running time and LUT data capacity are highly dependent on the simulation time-step. Figure 3-15 demonstrates the running time results of using various models under different time-steps. It is observed that the running time of using the proposed method is almost ten times less than using a detailed model directly in a PE system simulation under the same 1ns time-step. However, both cases are only suitable for a short duration simulation due to the out-of-memory problem. Notice that the proposed approach can also run under μs time-step with reasonable accuracy. In this way, the system simulation can run for a more extended period. Meanwhile, the simulation speed is comparable with the ideal switch case.

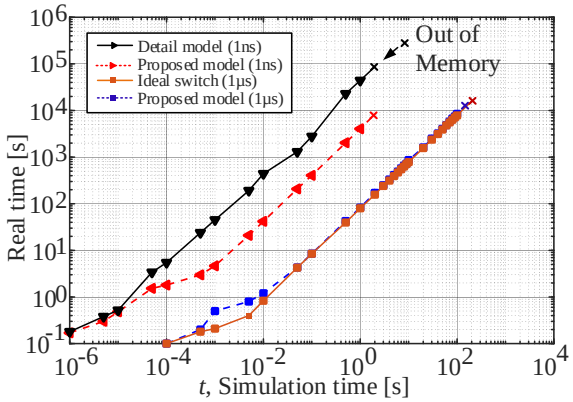


Figure 3-15 System simulation time using various models and time-steps.

3.6. Chapter Conclusion

This chapter presented an IGBT-diode cell behavioral model for estimating power losses of power electronics converters in the electromagnetic transient simulation. A comprehensive simulation strategy was introduced, and a relatively balanced trade-off between simulation speed and accuracy was achieved. The IGBT model's modelling process was analytically provided considering various impacts, and the parameter extraction sequences were also introduced. As a result, the switching cell's transient switching waveforms were reproduced in device-level simulation using the device model. According to the system application's operating range, a multi-dimensional power loss look-up table was obtained through a multiple-run simulation in PSCAD/EMTDC.

The electrical network was typically implemented in simulation with simple switch models for semiconductors in the circuit-level simulation. The power losses were obtained in every switching cycle by searching from the power loss table based on the instantaneous operating conditions. The proposed method was supported by a good agreement of simulated and experimental results from the DPT bench and a boost converter in terms of switching transients and power losses. Furthermore, the applicability, limitation and efficiency of the proposed approach were discussed. A reasonable accuracy and a fast simulation speed were achieved without convergence issues by selecting a nanosecond time-step for the device-level simulation and a microsecond for the circuit-level simulation. Besides, the modelling and the power loss calculation methods were applicable to a switching cell. The counterparts for the other cases, such as SiC MOSFETs and GaN devices, will be presented in Chapter 4 and Chapter 5.

Chapter 4 An Electro-thermal Model of SiC MOSFET for Power Loss and Temperature Predictions

- A Part of the work presented in this chapter is the result of original work published under **Y. Xu**, C. N. M. Ho, A. Ghosh and D. Muthumuni, "A Datasheet-Based Behavioral Model of SiC MOSFET for Power Loss Prediction in Electromagnetic Transient Simulation," in *Proc. IEEE APEC*, Mar. 2019, pp. 521-526.
- A Part of the work presented in this chapter is also the result of original work published under **Y. Xu**, C. N. M. Ho, A. Ghosh and D. Muthumuni, "Design, Implementation and Validation of Electro-Thermal Simulation for SiC MOSFETs in Power Electronic Systems," *IEEE Trans. Ind Appl.*, vol. 57, no. 3, pp. 2714-2725, May-June 2021.

This chapter's key objective is to develop a datasheet-based electro-thermal model of SiC MOSFET with PIN diode or SBD for power losses and temperature estimations in a PE system. The comprehensive modelling approach is based on the transient switching analysis in a double pulse test circuit. The model parameters extraction procedures from the device datasheet are also given. The impacts of various parasitic elements and the interaction of diode on switching transients are discussed in detail. Further, the thermal network modelling method is presented to reproduce the device's dynamic thermal behavior. Finally, a closed-loop electrical-thermal simulation was implemented in PSCAD/EMTDC and experimentally verified by a DPT bench and a PFC system. The details of the work are followed in the subsequent sections.

4.1. Introduction

Nowadays, SiC MOSFET, as one of the most popular Wide-Bandgap (WBG) semiconductor devices, has been rapidly developed with superior features such as high breakdown voltage, fast switching speed and high thermal conductivity [155]. As a result, it is increasingly used in many modern PE applications (e.g. photovoltaic (PV) [156], Power Factor Correction (PFC) [157], and power supply [158]). On the one hand, the higher switching frequency leads to higher power density for PE systems. On the other hand, the increases in switching losses and thermal stress and the intense impacts of parasitic circuit components result in device fatigue failure. Thus the merits of using SiC devices are alleviated. Hence a

correct approach for evaluating the power losses and thermal performance of SiC MOSFETs in a PE system is highly desirable and promising for system design.

One straightforward method of determining the power loss of semiconductors is capturing the switching transients using the DPT setup [159]. Apart from the tedious process for different permutations of the operating conditions, high bandwidth probes for the voltage and current measurements are required due to the fast switching speed of SiC MOSFETs. Several simulation models have been proposed to reproduce the switching behaviors of SiC MOSFETs, avoiding repetitive measurements. Built-in SPICE-based MOSFET models [160]-[161] were commonly used, which provided a physical description of the channel current and internal capacitances. The model's physical parameters were usually unavailable in the device datasheet, and the diode's behavior was typically neglected. Several analytical loss models [162]-[163] were developed to improve the model's accuracy. The mathematical loss equations were derived based on the transient equivalent circuits for each switching sub-stages. However, complicated numerical calculations were often involved with convergence issues.

Simple thermal resistances between different thermal layers are commonly used to describe the heat transfer process for steady-state thermal analysis, and the junction temperature is computed. Thermal impedances instead of resistances are required to be considered to represent the dynamic thermal behaviors. RC thermal networks such as the Cauer network [164] and the Foster network [165] have been widely used and can be transformed into each other using mathematical methods. Further, by combining a circuit simulator with a thermal model, several electro-thermal models [166]-[168] have been proposed. However, most of these models require proprietary software or external solvers to accomplish the simulation.

Comprehensive electro-thermal simulation methods for SiC MOSFETs in PE systems have been proposed to solve those issues. Both the power losses and thermal performance were evaluated in the same simulator without convergence issues. The commutation unit in Figure 4-1 is considered in this chapter. This phase-lag configuration is widely used as a basic switching cell in a PE system. S_L stands for a SiC MOSFET and S_H can be a PIN diode (Conf.1), an SBD (Conf.2), or a SiC MOSFET with/without an SBD (Conf.3/4). V_{dd} and I_L denote the circuit voltage and current, respectively.

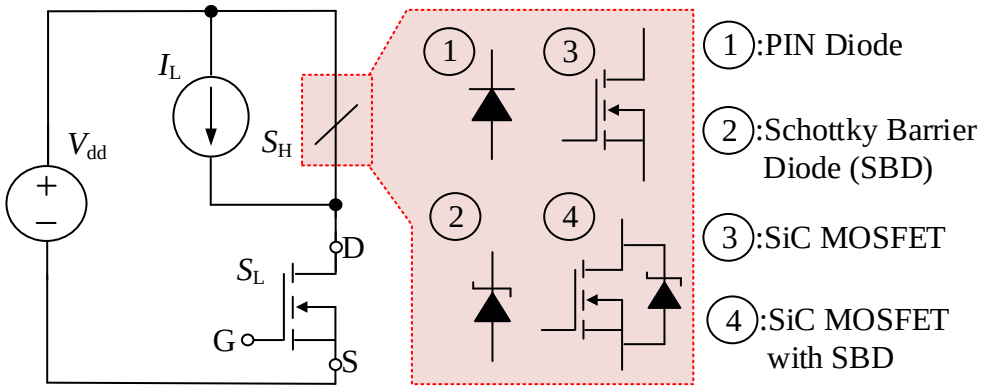


Figure 4-1 Basic SiC MOSFET switching commutation unit.

4.2. Simulation Strategy

The electro-thermal simulation's primary objective is to provide fast and accurate power losses and junction temperature estimations of SiC MOSFET in a PE system. Figure 4-2 illustrates a block diagram of the overall simulation strategy, which includes two stages, device simulation and system simulation. The corresponding flow chart is presented in Figure 4-3.

- **Device-level Simulation**

A SiC MOSFET is initially selected in the device simulation based on the PE application's power rating requirements. The model parameters are extracted from the device datasheet by curve fitting methods and empirical formulas. Afterwards, the PE application's operating range is identified and set in the device simulation with the extracted model parameters. A DPT circuit in Figure 4-1 is implemented in a simulator for device simulation. Subsequently, this device simulation runs multiple times to cover the whole operating range. Since the switching time of SiC MOSFET is typically within a hundred nanoseconds (ns), the simulation time-step is recommended to 1 ns or less for high accuracy. During each device simulation run, the SiC MOSFET's switching waveforms are obtained. The corresponding power losses are computed simultaneously by integrating the product of the device voltage and current. As a result, a multi-dimensional (T_j, V_{dd} and I_L) power losses LUT are generated and further exported for system simulations.

- **System-level Simulation**

A PE circuit with simple switch models is implemented in another simulation file with a microseconds (μs) time-step in the system simulation. The power loss LUT and the dynamic

thermal model are integrated with the electrical circuit. Therefore, at each switching action, the instantaneous power losses (p_{ts}) of SiC MOSFET are computed through power loss LUT interpolation based on the instantaneous operating conditions (V_{dd}, I_L) as well as T_j from the additional dynamic thermal model. Moreover, T_j is also updated based on obtained p_{ts}. This closed-loop simulation is a simple search method and mathematical calculation. Thus, it will not significantly increase extra computational time than the current method in PSCAD that uses two-value resistances for the switching device.

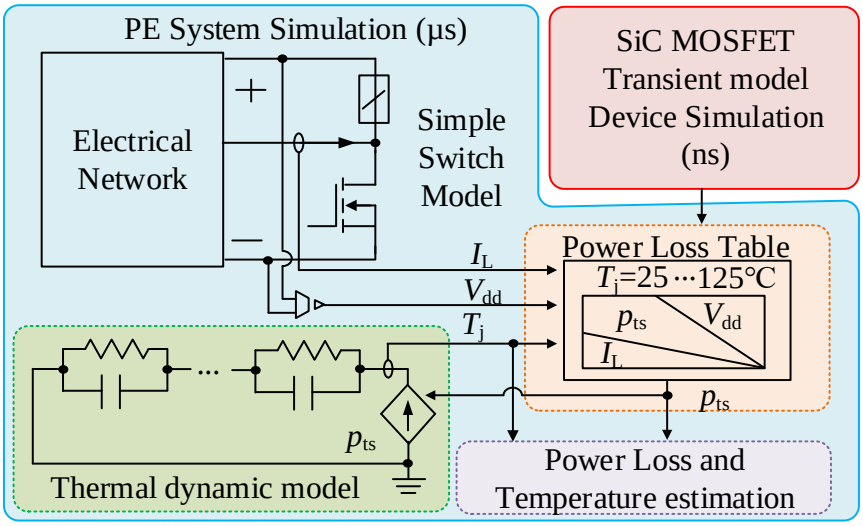


Figure 4-2 Block diagram of the electro-thermal simulation strategy

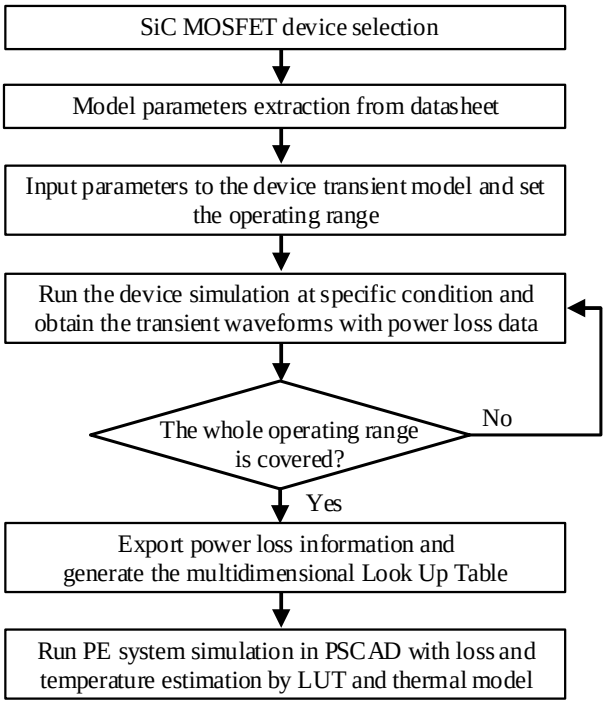


Figure 4-3 Flow chart of the electro-thermal simulation approach.

4.3. Model Description

4.3.1 Model Circuit of SiC MOSFET

The DPT equivalent circuit and the detailed behavioral model circuits of the SiC MOSFET and the diode are illustrated in Figure 4-4 (a) and (b), respectively. The low-side switch S_L is SiC MOSFET and the high-side switch S_H serves as a freewheeling diode. Note that these switches are realized by the four configurations mentioned previously. A gate drive voltage v_g is provided to control the S_L through R_{gext}. C_{gd}, C_{gs} and C_{ds} are the junction capacitances among gate, drain and source nodes of S_L. Based on the realization of the switch S_L and S_H, the corresponding forward parasitic capacitance (C_F) is expressed as,

$$C_F = \begin{cases} C_{oss} & \text{, Conf.1 and Conf.3} \\ C_D & \text{, Conf.2} \\ C_{oss}+C_D & \text{, Conf.4} \end{cases}, \tag{4.1}$$

where C_{oss} is the output capacitance of the SiC MOSFET and C_D is the diode capacitance of the SBD. Notice that the equivalent capacitance of S_L equals to C_{oss} for the case of a single SiC MOSFET in the following consideration. Besides, by applying Kirchoff's Law for the drain terminal of S_L, the drain current (i_d) is expressed by,

$$i_d = i_{ch} + i_{gd} + i_{ds}, \tag{4.2}$$

where i_{ch}, i_{gd} and i_{ds} are the MOS channel current, gate-drain current and drain-source current, respectively. The behavioral model of SiC MOSFET is presented in detail as follows.

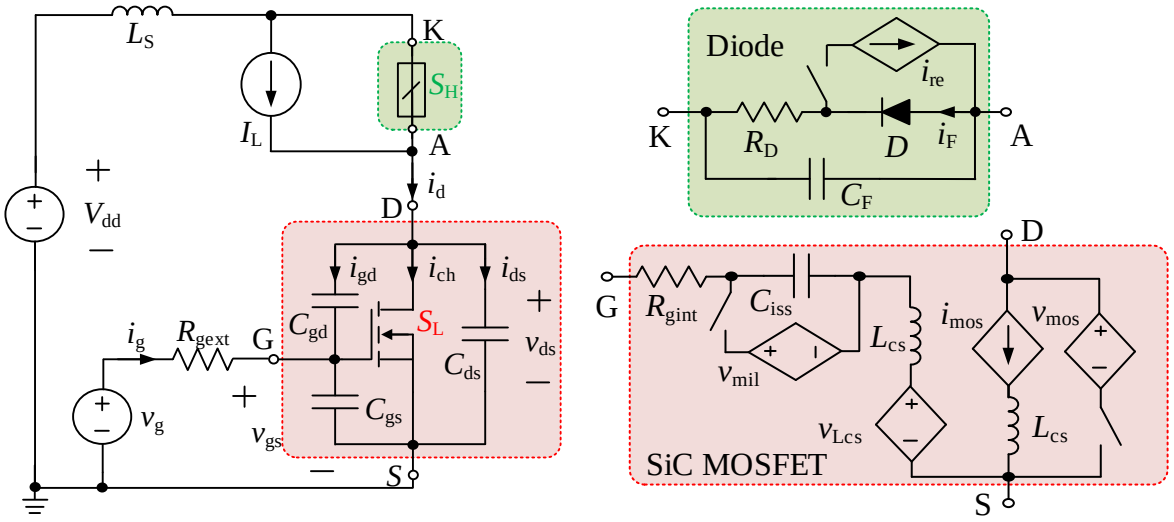


Figure 4-4 (a) DPT equivalent circuit; (b) Behavioral model of SiC MOSFET.

- **Gate loop part**

A gate-drive voltage v_g is assumed to flip between V_{goff} (e.g. -5V) and V_{gon} (e.g. 20V). The internal gate resistance R_{gint} and the external gate resistance R_{gext} form the total gate resistance R_G. And the nonlinear junction capacitance is represented by the input capacitance C_{iss} with the equivalent voltage source v_{mil} for miller plateau [170].

$$v_{\mathrm{mil}} = \frac{i_{\mathrm{mos}}}{g_{\mathrm{fs}}} + v_{\mathrm{T}}, \tag{4.3}$$

where g_{fs} denotes the trans-conductance of SiC MOSFET and i_{mos} is the total current flowing through the SiC MOSFET.

Different from the analyses in Chapter 3, a common-source parasitic inductance (L_{cs}) is taken into account, and its influence is more significant than the case of a Si IGBT due to the faster switching speed for a SiC MOSFET. It is observed from Figure 4-4(b) that, L_{cs} exists both in the gate loop and MOS channel part to decouple both components. Additionally, an equivalent voltage source v_{Lcs}, is added in the gate loop to reflect the interactive effect resulting from the change of i_{d},

$$v_{\mathrm{Lcs}} = L_{\mathrm{cs}} \cdot \mathrm{d}i_{\mathrm{mos}}/\mathrm{d}t. \tag{4.4}$$

- **MOS channel part**

The MOS channel part mainly consists of the dependent current source i_{mos} and the dependent voltage source v_{mos} representing the current and voltage performances of SiC MOSFET, respectively. The on-state voltage drop v_{on} typically is expressed by the function of the drain-source on-state resistance ($R_{\mathrm{DS(on)}}$) and I_{L}.

$$v_{\mathrm{on}} = R_{\mathrm{DS(on)}} \cdot I_{\mathrm{L}}. \tag{4.5}$$

Detailed derivation of i_{mos} is discussed in section 4.3.2. All the stray inductances in the power loop are lumped and represented by L_{S}. Moreover, the gate inductance in the gate loop circuit is neglected here for simplicity.

- **Diode part**

The forward resistance R_{D} can roughly represent the static characteristic of the body diode. It is obtained from the diode I-V curve in the datasheet. Besides, the equivalent current source i_{re} is also employed in this part to describe the diode's reverse recovery behavior. The

analytical equation for i_{re} can be found in the previous section 3.3.1. The reverse recovery characteristic commonly exists in the PIN diode and body diode of SiC MOSFET. In contrast, the reverse recovery time is ignored for majority-carrier devices (e.g. SBD). In that case, the junction capacitance C_F is the primary concern of SBD.

The typical switching waveforms are illustrated in Figure 4-5(a), which includes turn-on ($t_0 - t_4$) and turn-off ($t_5 - t_8$) period [169]. The equivalent circuit for the voltage transition period is also shown in Figure 4-5(b). The modelling process is presented in detail as follows.

4.3.2 Switching Transient Modelling

Generally, the SiC MOSFET as S_L operates in the same manner as the case of Si IGBT. However, the impacts of parasitic inductances and nonlinear capacitances on the switching behaviors are more significant for SiC MOSFET due to its fast switching speed. Besides, the parasitic elements usually are inevitable in PE systems. Hence, the effects of parasitic elements are considered in the transient model and discussed in detail in this section. It is assumed that during the switching transients, V_{dd} and I_L remain constant, which is reasonable for such a short switching period.

- **Turn-on period ($t_0 \sim t_4$)**

A gate drive voltage V_{gon} is provided through R_G to charge C_{iss}. Subsequently, v_{gs} starts increasing. Once v_{gs} reaches v_T, the conductive MOS channel is built. During this period, i_d is modelled as a current source i_{mos}, which is linked by g_{fs} and v_{gs}.

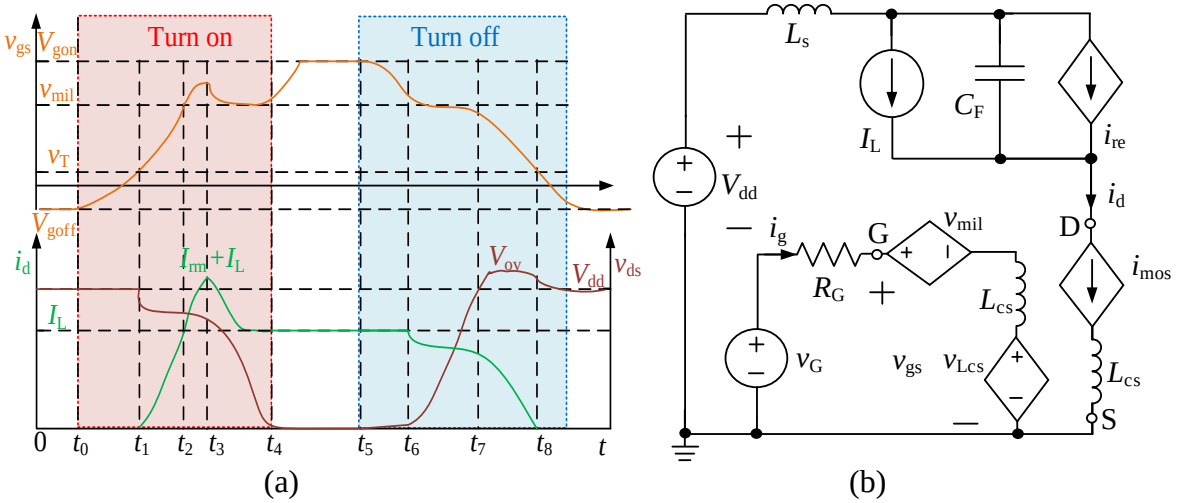


Figure 4-5 (a) Typical switching waveforms; (b) Equivalent circuit during voltage transition.

$$i_{\mathrm{mos}} = g_{\mathrm{fs}} \cdot (v_{\mathrm{gs}} - v_{\mathrm{T}}). \tag{4.6}$$

It is noted that L_{cs} provides negative feedback from the power loop to the gate loop. This introduces an extra voltage drop v_{Lcs} associated with the fast change of i_{d}. As shown in Figure 4-6(c), the slew rate of i_{d} is influenced by L_{cs} and as a result, the turn-on time and power losses of the device are affected accordingly.

As soon as i_{d} rises to I_{L}, v_{gs} is clamped at v_{mil}. Meanwhile, an additional current is added to i_{mos} because of the reverse recovery behavior of the high-side diode. During the current rising period, v_{ds} is almost constant with a slight decline due to the voltage drop across L_{S} as shown in Figure 4-6 (a). Once i_{re} hits the peak I_{rm}, the voltage transition period begins, and the equivalent circuit is shown in Figure 4-5(b). Thereby, v_{ds} starts decreasing as,

$$\frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t} = -(v_{\mathrm{g}} - v_{\mathrm{mil}})/(C_{\mathrm{gd}} \cdot R_{\mathrm{G}}). \tag{4.7}$$

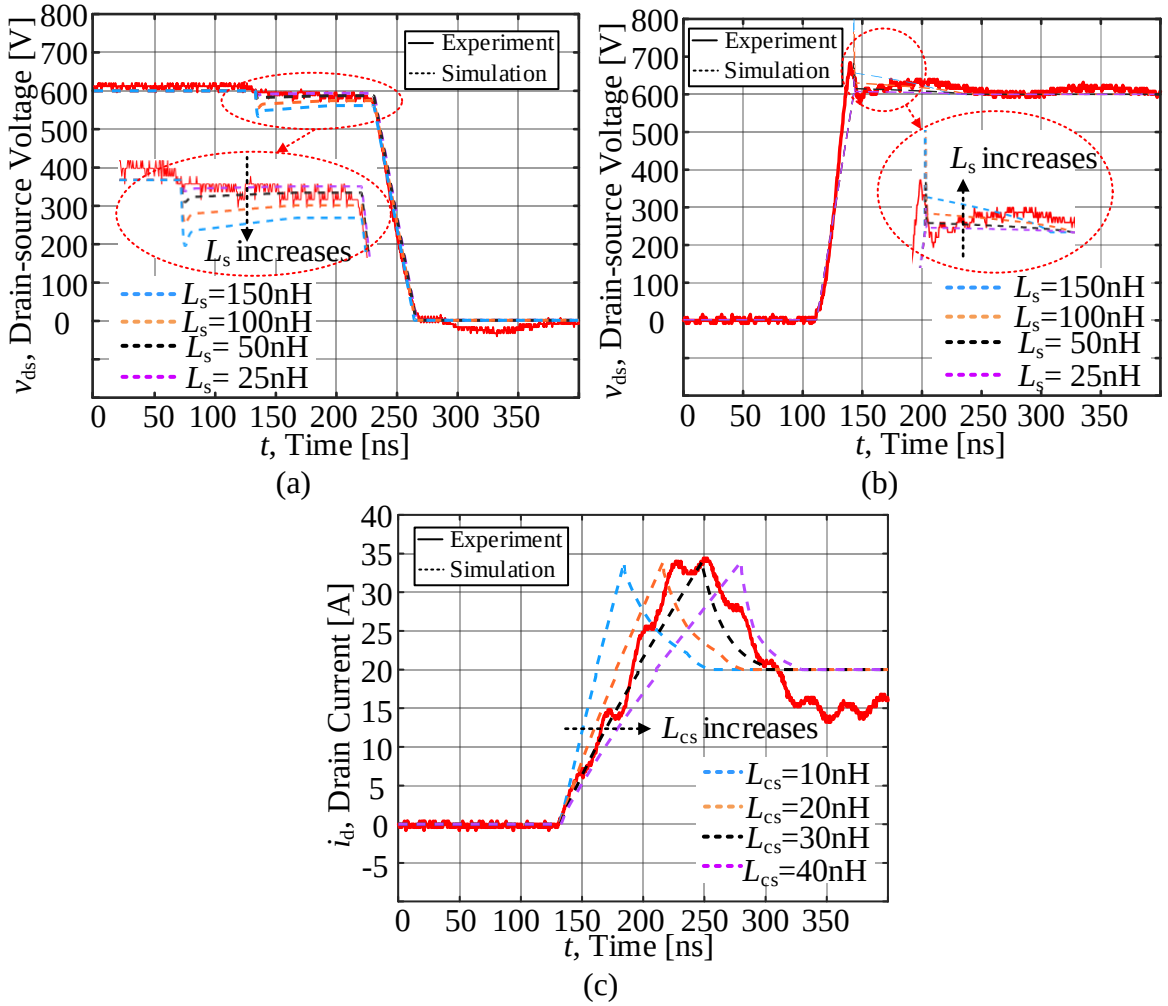


Figure 4-6 Effect of L_{S} on v_{ds} (a) turn-on; (b) turn-off, and effect of L_{cs} on i_{d}.

As v_{ds} drops significantly, a particular concern of the impacts of parasitic capacitances in both switches (i.e. C_{oss} for S_{L} and C_{F} for S_{H}) are required to be considered. A displacement current is generated due to the charging and discharging processes. Based on the definition of output capacitance of S_{L} ($C_{\mathrm{oss}} = C_{\mathrm{gd}} + C_{\mathrm{ds}}$), the capacitive current (i_{oss}) is expressed by

$$i_{\mathrm{oss}} = i_{\mathrm{gd}} + i_{\mathrm{ds}} = C_{\mathrm{oss}} \cdot \frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t}. \tag{4.8}$$

During this period, v_{ds} decreases to on-state voltage drop v_{on}. Meanwhile, C_{oss} and C_{F} are discharged and charged, respectively. Since the sum of these parasitic capacitances' voltages are clamped to V_{dd}, they share the same absolute value of voltage slope ($\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$). Applying Kirchhoff's law to the drain node of S_{L}, i_{d} also is expressed as

$$i_{\mathrm{d}} = i_{\mathrm{mos}} = I_{\mathrm{L}} + i_{\mathrm{re}} - C_{\mathrm{F}} \cdot \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t. \tag{4.9}$$

According to the above equations, i_{ch} is further obtained,

$$i_{\mathrm{ch}} = i_{\mathrm{mos}} - i_{\mathrm{oss}} = I_{\mathrm{L}} + i_{\mathrm{re}} - (C_{\mathrm{oss}} + C_{\mathrm{F}}) \cdot \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t. \tag{4.10}$$

As a result, v_{mil} is also changing according to the following equation,

$$v_{\mathrm{mil}} = \frac{i_{\mathrm{ch}}}{g_{\mathrm{fs}}} + v_{\mathrm{th}} = \frac{I_{\mathrm{L}} + i_{\mathrm{re}} - (C_{\mathrm{oss}} + C_{\mathrm{F}}) \cdot \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t}{g_{\mathrm{fs}}} + v_{\mathrm{T}}. \tag{4.11}$$

At t_4 in Figure 4-5(a), SiC MOSFET turns on completely. Subsequently, v_{gs} continues climbing until it reaches V_{gon}. The on-state device is modelled as v_{mos} with the value of v_{on}.

- **Turn-off period ($t_5 \sim t_8$)**

The turn-off process is almost the inverse sequence of the turn-on process. As a negative V_{goff} is applied at t_5, v_{gs} begins decreasing by discharging C_{iss}. At the same time, v_{ds} starts to rise. Again, the displacement current occurs, resulting in a reduction of current accordingly.

$$i_{\mathrm{mos}} = I_{\mathrm{L}} - C_{\mathrm{F}} \cdot \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t. \tag{4.12}$$

Once v_{ds} rises to V_{dd}, the current commutation between S_{L} and S_{H} begins. A resultant overvoltage V_{os} is induced by L_{S}. Figure 4-6(b) shows that this voltage spike is significant, leading to the device's damage. Therefore, a proper layout design to reduce L_{S} or sacrifice the switching speed may be the solution to alleviate this overvoltage issue.

Based on the above analyses, the i_{mos} of SiC MOSFET is summarized as,

$$i_{\mathrm{mos}} = \begin{cases} 0, v_{\mathrm{gs}} < v_{\mathrm{T}} \\ g_{\mathrm{fs}} \cdot \left(v_{\mathrm{gs}} - v_{\mathrm{T}}\right), \ v_{\mathrm{gs}} > v_{\mathrm{T}} \text{ and } i_{\mathrm{mos}} < I_{\mathrm{L}}. \\ I_{\mathrm{L}} - C_{\mathrm{F}} \cdot \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t + i_{\mathrm{re}}, \mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t > 0 \end{cases} \tag{4.13}$$

4.3.3 Thermal Dynamic Model

In a PE system, a SiC MOSFET is typically mounted on a heat sink. This configuration is separated into four thermal layers, as shown in Figure 4-7. The power loss heat energy generated from the junction is transmitted to the case and heatsink with thermal interface material (TIM). Eventually, this energy is dissipated to the ambient. For steady-state analysis, this heat transfer process is represented typically by thermal resistances between different layers. Meanwhile, T_{j} of power device is computed based on the power dissipation $\mathrm{p_{ts}}$ and the ambient temperature $\mathrm{T_a}$ which is considered as constant in this chapter.

For modelling the device's dynamic thermal behavior, thermal capacitances are essential for forming a dynamic thermal model with thermal resistance. RC thermal networks in Cauer-type and Foster-type are commonly used. In essence, the former is based on the device's internal physical layers and thus computationally complex to implement. On the other hand, the latter is a mathematical model, and the thermal parameters are obtained from the device datasheet. The dynamic thermal model of SiC MOSFET is developed and implemented in PSCAD based on both Cauer and Foster RC networks, as shown in Figure 4-7(b). The Foster-type RC element of thermal impedance from junction to case Z_{jc} are preliminarily extracted by curve fitting the transient thermal curve in the datasheet as

$$Z_{\mathrm{jc}} = \sum_{i=1}^{n} R_{\mathrm{thF}i} \cdot \left(1 - e^{-\frac{t}{\tau_{\mathrm{thF}i}}}\right). \tag{4.14}$$

Notice that the number of exponential terms n equals two in this chapter to form a 2nd order Foster network for simplicity and $\tau_{\mathrm{thF}i}$ ($R_{\mathrm{thF}i} \cdot C_{\mathrm{thF}i}$) are time constants.

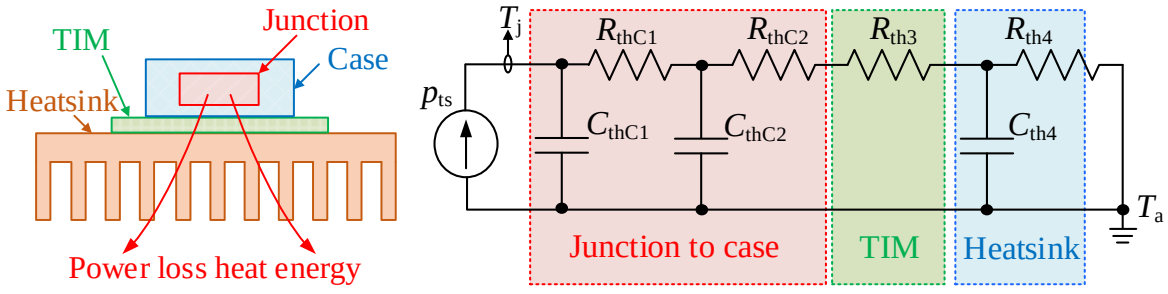


Figure 4-7 Thermal dynamic model (a) schematic diagram; (b) RC equivalent circuit.

A thermal pad (Sil-Pad® 400 [171]) as a TIM is used and attached between the device case and heatsink. The corresponding R_{th3} is obtained from the datasheet. Besides, an individual heatsink from Wakefield-Vette (OMNI-UNI-27-25) is adopted. R_{th4} and C_{th4} are further obtained based on the heatsink datasheet and the material (Aluminum 6063-T5) data [172]. All the thermal-related parameters are illustrated in Table 4-1.

4.3.4 Parameter Extraction Procedure

The device's main parameters are extracted from the device datasheet by curve fitting or empirical formulas. As an example, the SiC MOSFET (SCT2080KEC) from ROHM is selected, which is typically operated at $V_{\mathrm{dd}} = 600\mathrm{V}$ and I_{L} varies in the range of [0A, 40A].

- **MOSFET Parameters**

To describe the SiC MOSFET's switching behavior, v_{T} and g_{fs} are typically assumed as constants. In fact, v_{T} is a thermal-dependent parameter that is fitted by a quadratic function of T_{j}. k_{Ta}, k_{Tb} and k_{Tc} are fitting constants.

$$v_{\mathrm{T}}(T_{\mathrm{j}}) = k_{\mathrm{Ta}} \cdot T_{\mathrm{j}}^2 + k_{\mathrm{Tb}} \cdot T_{\mathrm{j}} + k_{\mathrm{Tc}}. \tag{4.15}$$

Table 4-1 Key Parameters of SiC MOSFET Model

Parameter	Value	Parameter	Value	Parameter	Value
R_{gint}	6.3Ω	k_{Ta}	0.0000312	R_{D}	0.214Ω
k_{Tb}	-0.01217	k_{Tc}	3.257	k_{a}	0.1314
L_{cs}	30nH	L_{S}	50nH	R_{th3}	1.13 K/W
k_{b}	-1.993	k_{R}	1.396	C_{thF1}	0.2006
R_{th4}	5 K/W	C_{th4}	28.13 J/K	C_{thC1}	0.0098
R_{thF1}	0.2366	R_{thC1}	0.2296	C_{thF2}	0.01026
R_{thF2}	0.2083	R_{thC2}	0.2153	C_{thC2}	0.2102
Heat Capacity		0.900 J/(g·K)	Heatsink Density		2.7 g/cm^3
	C_{hv}	k_{ca}	k_{cb}	k_{cc}	k_{cd}
C_{iss}	2239	38.17	39.04	64.47	3.001
C_{oss}	77	35.45	104.1	90.48	0.8351
C_{rss}	16	26.47	68.47	96.76	2.279

Moreover, g_{fs} is nonlinear and related to i_{ch} which has been given little attention in the literature. According to the transfer curve from the datasheet, i_{mos} and g_{fs} are fitted by the following equations, where k_{a} and k_{b} are the curve fitting coefficients.

$$i_{\mathrm{mos}} = k_{\mathrm{a}} \cdot \left(v_{\mathrm{gs}} - v_{\mathrm{T}}\right)^2 + k_{\mathrm{b}}, \tag{4.16}$$

$$g_{\mathrm{fs}} = i_{\mathrm{mos}} \cdot \sqrt{k_{\mathrm{a}}/(i_{\mathrm{mos}} - k_{\mathrm{b}})}, \tag{4.17}$$

It is well known that C_{iss}, C_{oss} and C_{rss} of a SiC MOSFET, are a function of v_{ds}. While C_{D} in the SiC SBD is related to the reverse voltage. Based on that, all the capacitances are obtained by fitting the capacitance curves using the following equation, where C_{hv} is the capacitance at a high-voltage range. k_{ca}, k_{cb}, k_{cc} and k_{cd} are all fitting constants [173].

$$C(v) = C_{\mathrm{hv}} + k_{\mathrm{ca}}/(1/k_{\mathrm{cb}} + v^{k_{\mathrm{cd}}}/k_{\mathrm{cc}}), \tag{4.18}$$

As mentioned previously, the on-state voltage v_{on} is related to $R_{\mathrm{DS(on)}}$ and I_{L}. It is noted that $R_{\mathrm{DS(on)}}$ is also a crucial temperature-dependent parameter. The following equation can fit it from the datasheet, where k_R is a fitting constant.

$$R_{\mathrm{DS(on)}}(T_{\mathrm{j}}) = R_{\mathrm{DS(on)}}(T_{\mathrm{a}}) \cdot \left(\frac{T_{\mathrm{j}}+273}{T_{\mathrm{a}}+273}\right)^{k_{\mathrm{R}}}. \tag{4.19}$$

- **Diode parameters**

Note that the forward conducting and reverse recovery behaviors of a diode are considered in the diode model. The effect of reverse recovery current is ignored for the SiC SBD case, as mentioned previously. The reverse peak current I_{rm} and time constant τ_{re} are extracted from the diode I-V curve and the charging curve in the datasheet based on the same equations as previously provided in section 3.3.1.

- **Parasitic inductances**

To accurately extract the parasitic inductance from the device datasheet is rather challenging. Often, only the device module's internal parasitic inductance is given by the manufacturer. While the other parasitic inductances, such as L_{S} and L_{cs}, are dependent on the specific Printed Circuit Board (PCB) design and the corresponding device package. These parasitic inductances are challenging to measure and are computationally extracted by ANSOFT or Maxwell Q3D [174]. In this model, L_{S} and L_{cs} are preliminarily estimated based on the PCB trace length of the power loop and gate loop [175] as well as the device package

(e.g. 2-5nH for TO-247 [176]). If the measured switching waveforms are attainable, the parasitic inductances are further calibrated and determined approximately. For example, it is seen from Figure 4-6, the simulated results with the conditions of $L_S = 50\text{nH}$ and $L_{cs} = 30\text{nH}$ match well with the experimental results comparing with other conditions. Therefore, the corresponding inductance values are determined.

4.4. Experimental Verification

The proposed approach's key objective is to evaluate the power dissipation and the thermal performance of SiC MOSFETs in a PE system simulation with acceptable accuracy and relative fast simulation speed.

4.4.1 Device-level Verification

A DPT setup was designed and implemented based on Figure 4-1 to characterize the device and validate the proposed SiC MOSFET model. The DUT is the low-side SiC MOSFET (SCT2080KEC, Rohm). The high-side device uses the body diode of the same SiC MOSFET as a freewheeling diode. Both devices are placed on top and bottom sides respectively to reduce the parasitic inductance. The driver IC with the type IXDN609SI is adopted as the gate driver providing 20V/-5V drive voltage. One 0.1Ω current shunt resistor (SDN-414-01) is inserted to measure the switching current of the DUT. And v_{ds} is measured directly by a high-bandwidth passive voltage probe (TTP800). Besides, the DSP-controlled thermal heater and a cooling fan are implemented for the operating junction temperature control. Also, the temperature is monitored by a thermal imager (Tis40, Fluke).

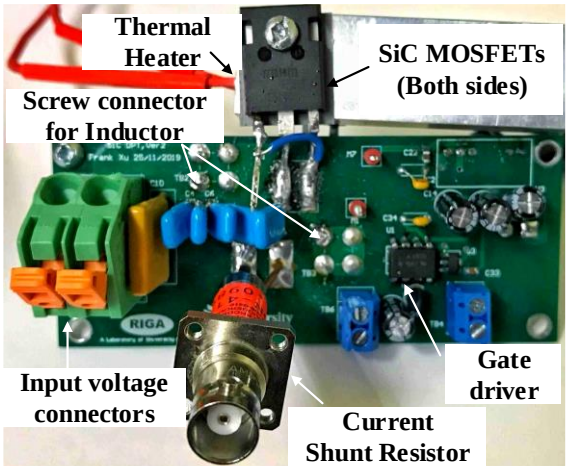


Figure 4-8 The DPT bench for SiC MOSFET.

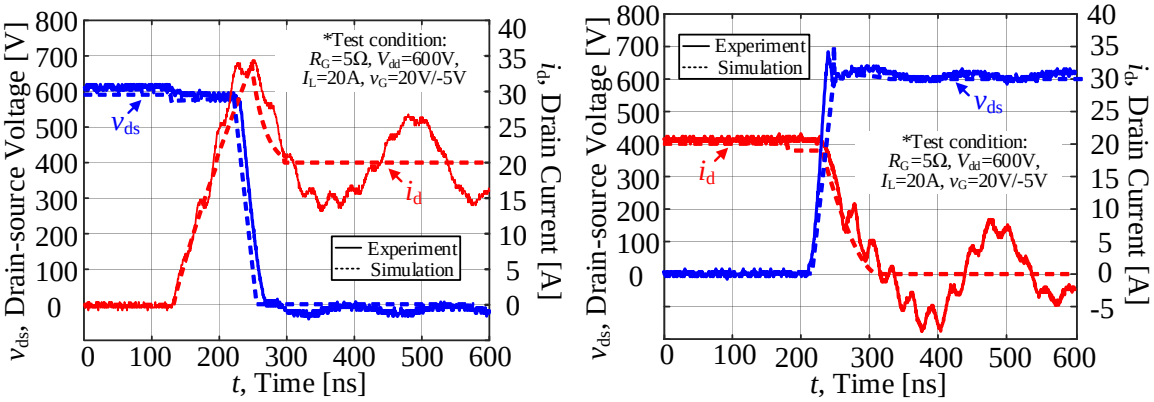


Figure 4-9 Transient switching waveforms (a) turn on; (b) turn off @ 25℃.

- **Switching transient verification**

The simulated results of DPT switching waveforms using the proposed model in PSCAD/EMTDC are compared with experimental results in Figure 4-9(a) for turn-on transient and (b) for turn-off transient. It is observed that during the current rising period, around 50V voltage drop of v_{ds} occurs due to the impact of L_{S} .The additional overcurrent of i_{d} caused by the diode's reverse recovery behavior also is observed. During the turn-off period, the peak voltage of v_{ds} can reach 700V due to transient voltage across L_{S}. Therefore, a special concern should be paid to reduce the parasitcs in the PCB design process. Generally, the results indicate that the dynamic changes of voltage and current in simulation match well with the experimental results, which validates the proposed model's accuracy. However, the current has a ringing period because of parasitic elements' resonance, which is ignored for simplicity. Further investigation is needed.

- **Switching loss verification**

The switching losses of SiC MOSFET were evaluated for different operating conditions, as shown in Figure 4-10. In general, the power losses under various operating conditions are estimated using the proposed method with reasonable accuracy. It is found that the turn-on loss is more significant than the turn-off loss, and the latter has fewer changes than the former. The average error is within 10% and the loss discrepancy increase for high-temperature condition. The main reasons can be the ignorance of ringing loss and the non-ideal recharging process of parasitic capacitance for simplicity. Apart from the error of parasitic extraction, the thermal-dependent g_{fs} and diode parameters cannot be fully considered [177]-[178].

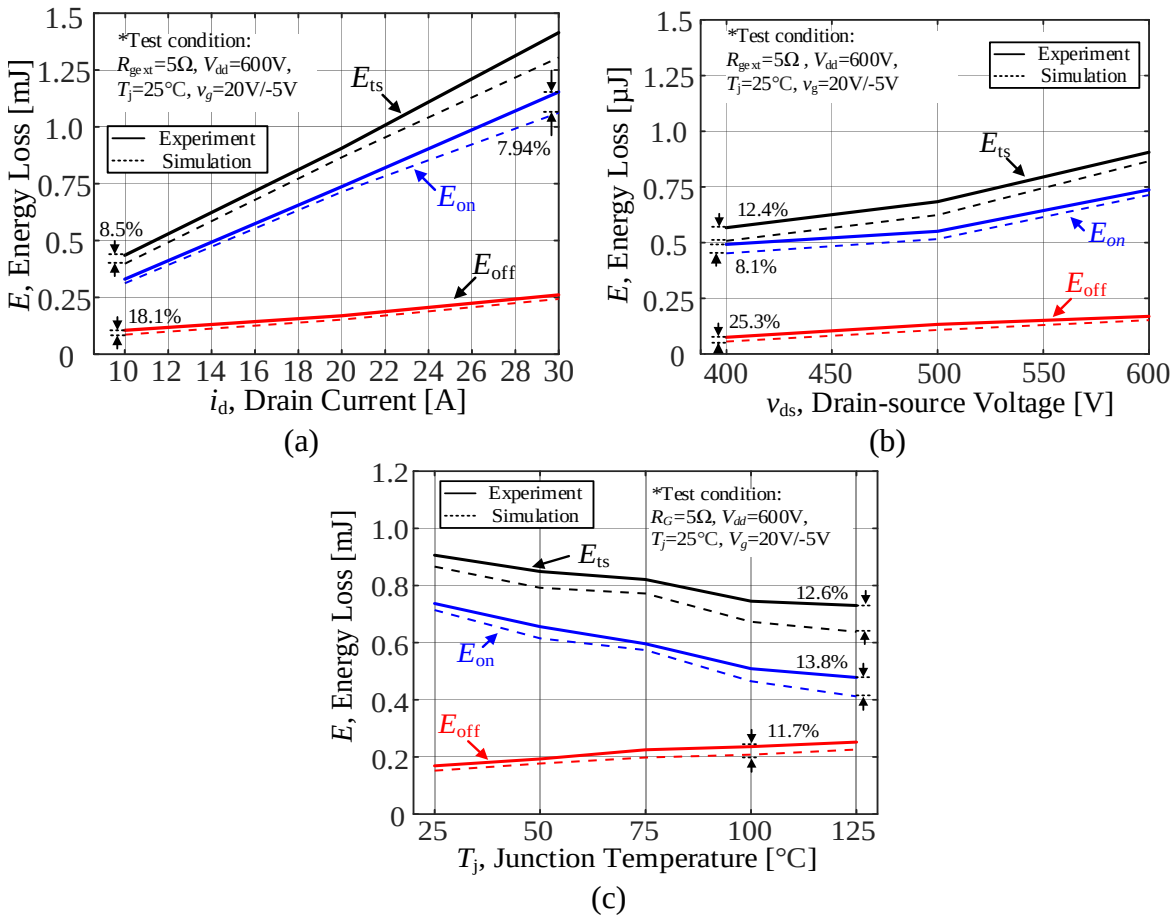
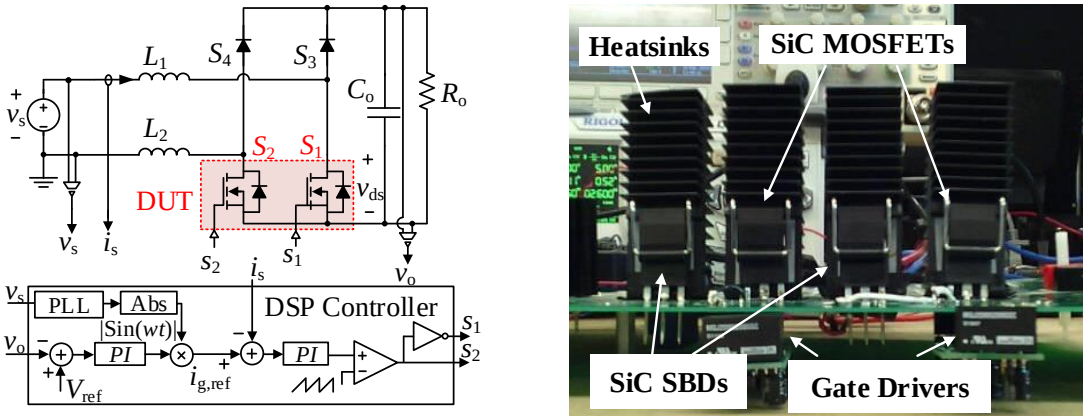


Figure 4-10 Switching losses results of the SiC MOSFET under various (a) i_d; (b) v_{ds}; (c) T_j.

4.4.2 System-level Verification

To further validate the proposed approach for power losses and thermal estimations in a PE system, a bridgeless PFC converter [179], as an example in Figure 4-11, was built and implemented in PSCAD/EMTDC, using simple switch models with an additional loss LUT and a dynamic thermal model. This designed PFC converter uses SiC MOSFETs as HF switches (S_1 and S_2) in paired with SiC SBD (S_3 and S_4), and runs under different voltage and power conditions. The switching devices operate as the complementary pairs S_1/S_3 and S_2/S_4 in accordance with grid voltage v_s. In addition, two PI control loops were employed and implemented in DSP to control the output voltage v_o and grid current i_s. Two identically designed inductors were used for L_1 and L_2 cooperating with the switching cell. The PFC system was tested and simulated under three different v_o and resistive load R_o(Case 1: 400V, 267Ω; Case 2: 500V, 400Ω; Case 3: 600V, 680Ω). The key parameters are listed in Table 4-2.



(a) (b)

Figure 4-11 PFC application (a) schematic diagram; (b) hardware setup.

Table 4-2 Key parameters of PFC application

Parameter	Value	Parameter	Value	Parameter	Value
v_s(rms)	120V,60Hz	v_o	400-600V	f_{sw}	50kHz
L_1&L_2	1.03mH	C_o	453.33μF	R_o	226.67-680Ω
S_1&S_2	SCT2080KEC	S_3&S_4	C4D20120D	R_{gext}	5Ω

- **Power loss estimation**

Figure 4-12 shows the steady-state waveforms of the PFC converter. It is observed that i_s synchronizes well with v_s. The switching cell operates well at high-frequency switching and continuous conducting alternatively. Notice that a positive cycle is selected for conduction power loss computation. Since the current of S_1 is the same as i_s when S_1 is on, the corresponding p_{con} is obtained by the product of i_s and v_{ds} for each on-state period. As the PFC starts running and reaches the steady state, p_{con} keeps changing due to the thermal-dependent $R_{DS(on)}$. Hence, p_{con} at 10s and 1200s (considered as the thermal steady-state) were measured respectively and compared with the simulated results in Figure 4-12 and Table 4-3. It is noticed that the proposed model shows great reproducibility of the instantaneous p_{con}. As v_o rises from 400V to 600V, the average conduction power decreases because of the decrement of the current. On the other hand, comparing the results at 10s and 1200s, a slight increment of conduction loss is observed, which can be explained by the positive correlation between $R_{DS(on)}$ and T_j. Overall, the average error is below 10% for various operating conditions which verifies the accuracy of the proposed model.

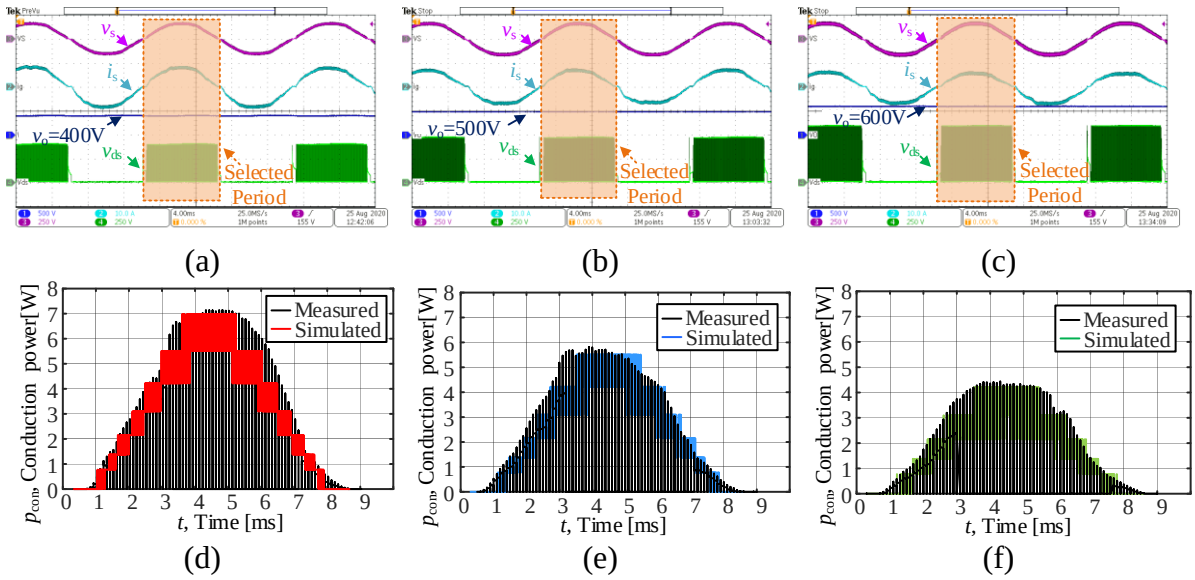


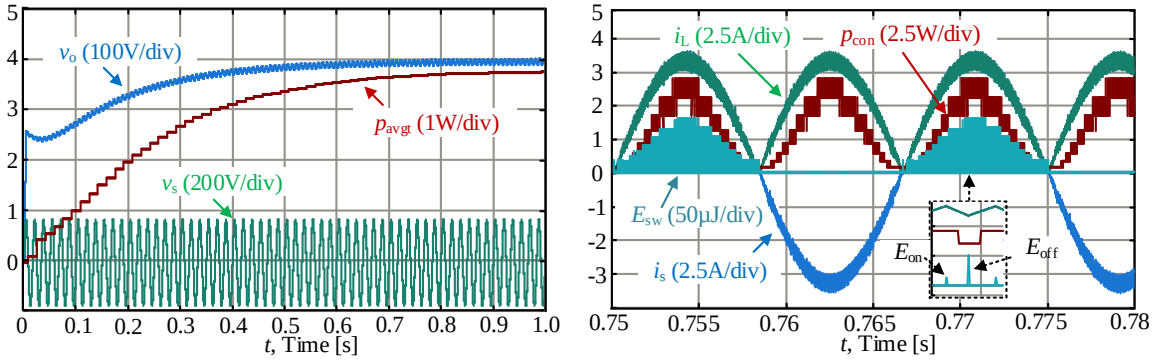
Figure 4-12 Measured PFC system waveforms under (a) case-1; (b) case-2; (c) case-3; Conduction power results of PFC at 10s (d) case-1; (e) case-2; (f) case-3.

Table 4-3 Conduction power loss results of PFC application

Condition	Case-1		Case-2		Case-3	
Time	10s	1200s	10s	1200s	10s	1200s
Measured	2.24W	3.12W	1.93W	2.61W	1.42W	1.94W
Simulated	2.41W	3.39W	2.01W	2.78W	1.51W	2.09W
Error	7.59%	8.65%	4.14%	6.51%	6.33%	7.73%

- **Thermal performance**

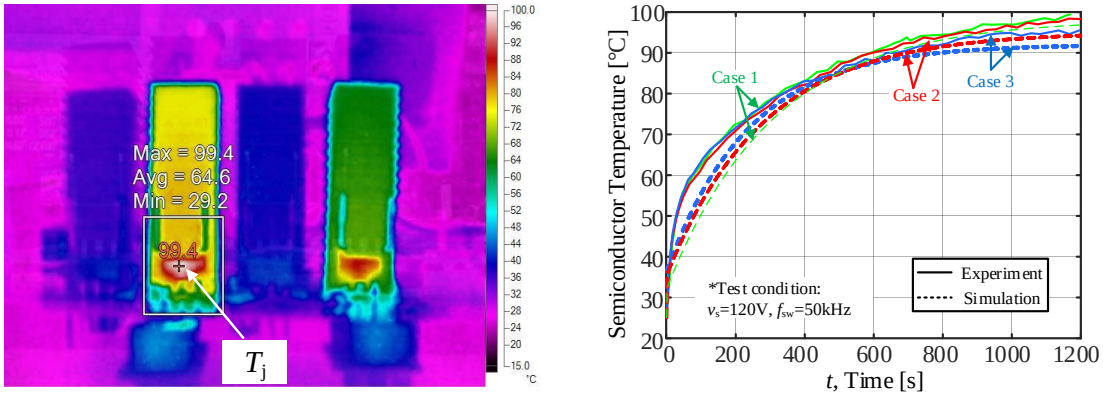
The simulated results of overall system performance and the detailed power loss estimations are demonstrated in Figure 4-13. Note that the computed average power losses of SiC MOSFET in one switching cycle p_{avgt} rises to steady state in accordance with v_{o}. Moreover, the detailed device losses breakdown, including p_{con}, E_{on} and E_{on} can also be predicted during each switching cycle and updated based on the instantaneous operating conditions. E_{on} and E_{off} are obtained at turn-on and turn-off transient, respectively, while p_{con} keeps changing in phase with the current. Since all the power loss data are pre-obtained from the power loss LUT in the device DPT simulation, the power loss estimations' accuracy within the available operating range is promised with fast simulation speed. It should be mentioned that this additional loss information will not affect the electrical circuit simulation.



(a) (b)

Figure 4-13 Simulated results for case 1(a) overall waveforms; (b) detailed loss waveforms.

Furthermore, the dynamic thermal model was also implemented in PSCAD/EMTDC for PFC electro-thermal simulation. All the switching devices were attached to the heatsink individually through the TIMs. The transient T_j of SiC MOSFET, which is the hottest spot, was monitored by the thermal imager, as shown in Figure 4-14(a). It is seen that SiC MOSFETs have a much higher junction temperature up to 100 ℃ than the SiC SBD. Hence, the losses of HF switching devices are more significant and are of particular concern for device selection and thermal management. Moreover, the simulated transient T_j of SiC MOSFET are compared and illustrate a good agreement with the experimental results in Figure 4-14 (b). It is observed that the T_j for all cases increase gradually from the initial 25ºC and reach to different steady-state at the 1200s due to the power loss difference. Nevertheless, the average error of the proposed model at 1200s is within 10%. Besides, it is also seen that the simulated thermal trajectories slightly deviate from the experimental results. The reasons can be the underestimation of thermal capacitance and the power losses in the low current range.



(a) (b)

Figure 4-14 Thermal results of PFC (a) thermal image; (b) transient T_j estimation.

4.4.3 Discussion

Applicability-The proposed model in this chapter applies to the EMT simulator for the device DPT simulation and is used to estimate the losses of the four types of the commutation unit in Figure 4-1. Further modifications are needed when it extends for other devices, such as Si IGBT and GaN devices. However, the parameter extraction procedures and simulation strategies are still applicable. The power loss database can also come from the device simulation or other device simulators (e.g. SPICE-like software) or measurements.

Efficiency- Generally, a reasonable accuracy of power loss estimation typically requires a complex device model considering massive impacts with a ns time-step. However, it is difficult for a PE system simulation to run with such a small time-step until the steady-state due to out-of-memory issues and inefficiency. Moreover, a simulation comparison of different methods was conducted for the PFC converter, as illustrated in Table 4-4. As noticed, the simulation in LTspice using the manufacturer's device model runs at the 1ns time-step instead of 1μs due to the convergence problem. As a result, it can obtain accurate loss information by sacrificing much more time for simulating only 100 ms compared to the same simulations in PSCAD using the proposed method and simple-switch model. Since the simple-switch model only uses two-state resistances to represent the switching devices, the average power losses are much lower than the other two methods due to the lack of switching losses. In short, Comparing with the other two methods, by using the proposed method in PSCAD, both fast simulation speed and acceptable accuracy of power estimations are achieved with additional transient temperature information of semiconductor devices.

Table 4-4 Simulation comparison of the PFC application

CPU: Quad 3.60GHz Intel Core i7-4790		Case1		Case 2		Case3	
Simulator	Time-step	Time (s)	p_{avgt} (W)	Time (s)	p_{avgt} (W)	Time (s)	p_{avgt} (W)
Simple-switch in PSCAD	1μs	10.6	2.37	10.3	1.96	10.8	1.48
Proposed method in PSCAD	1μs	11.2	3.82	10.9	3.66	11.4	3.36
Device model in LTspice	1ns	12866	3.93	12466	3.71	13191	3.67

4.5. Chapter Conclusion

In this chapter, a datasheet-based electro-thermal modelling approach for SiC MOSFET was developed and implemented in PSCAD/EMTDC and further validated by experiments to estimate the power losses and junction temperature in PE applications. Similar to Chapter 3, the primary simulation strategy includes the device-level and the system-level simulations.

A transient behavioral model of SiC MOSFET was developed in the device simulation to generate the device power loss table taking the schottky diode into account. This model provided insights into the impacts of parasitic elements, temperature and diode. In particular, the displacement currents caused by the nonlinear capacitances during the voltage transition period were also considered in the model. Further, the impacts of parasitic inductances on switching transients were discussed in detail. Besides, the parameter extraction procedures from a datasheet were also investigated. The simulated switching waveforms and the power loss results were consistent with the DPT measured results (the average error was below 10%).

In the system simulation, the bridgeless power factor correction system was implemented using simple-switch models along with the power loss look-up table and the dynamic thermal model. Eventually, the average power losses of SiC MOSFET and the switching losses for each switching cycle were predicted. Moreover, the simulated transient junction temperature results were in good agreement with measurements in a wide range of operating conditions. Besides, a discussion of the applicability and efficiency of the proposed approach was also presented. It was found that the proposed method had better reproducibility of the transient power losses, indicating its advantage of fast simulation speed as the simple-switch model and comparable accuracy with the device model from the manufacturer.

Chapter 5 A Generalized Behavioral Modelling Method of Switch-Diode Cell for Power Loss Prediction in Electromagnetic Transient Simulation

- A Part of the work presented in this chapter is the result of original work published under **Y. Xu**, C. Ho, A. Ghosh, and D. Muthumuni, "Generalized Behavioral Modelling Methodology of Switch-Diode Cell for Power Loss Prediction in Electromagnetic Transient Simulation," *Energies*, vol.14, no.5, pp.1500, Mar. 2021.

This Chapter's main objective is to provide a generalized behavioral modelling method of a Switch-diode (SD) cell for power loss estimation. This generalized model summarizes the behavioral models of Si IGBT and SiC MOSFET in the previous Chapter 3 and Chapter 4. Additionally, the switching behavior of GaN devices is also considered. The detailed model description and switching transient modelling process are illustrated for all the cases of different combinations of SD cells, including Si IGBT, SiC/Si MOSFET, eGaN HEMT, PIN diode and SiC SBD. Besides, the parameter extraction sequences from the device datasheet are also presented. Furthermore, the experimental verifications of the switching transients and power losses for various devices are given using different DPT apparatus in this chapter. A discussion on the accuracy, efficiency and applicability of the generalized model is conducted in the end. The details of the work are followed in the subsequent sections.

5.1. Introduction

A PE system plays a key role in the process of efficient energy control, conversion and management. Power semiconductor devices are the core components of PE systems and significantly impact system efficiency, reliability, and cost [180]. For decades, silicon-based devices, such as IGBTs [181], MOSFETs [182], are dominated and widely used in various modern PE applications (e.g. PV inverter [183], PFC [184], and power supply [185]). However, the PE system performance and efficiency are hindered by Si-based devices due to the fundamental material limits. Recently, WBG devices [186], such as SiC MOSFETs [187], eGaN HEMTs [188]-[189], have emerged and gained great popularity with superior features of fast switching speed and low switching losses. Thereby, the switching frequency is further

increased, bringing the merits of high power density and efficiency. However, devices' increased power losses are still the main contributors to the total losses, especially for high-frequency applications. The generated heat energy during switching transition may lead to fatigue failure and affecting reliability. Hence, an accurate power loss model is highly desirable for device selection and PE system optimization. This model needs to be applicable for different semiconductors and provide a deep insight into the switching process.

Generally, conduction loss and switching losses are the main contributors to the total power losses. The former is directly determined by the datasheet's output characteristic curve, while the latter is more complicated and can be measured in Double Pulse Tests (DPTs). Although the DPT is widely used and highly accurate, it is time-consuming and typically involves expensive probes and several peripheral bulky equipment. Recently, a lot of analytical loss models have been proposed [190]-[191]. Piecewise linearizing the device's switching process was commonly used to enable rapid loss estimation [192]. However, the parasitic elements were not fully considered, and thus the accuracy was still limited. The entire switching process of GaN HEMTs in totem-pole PFC converters was discussed in [193], considering the junction capacitances and stray inductances. The transient analytical equations were solved by mathematical tools. Further, a datasheet-based analytical model of GaN HEMTs was proposed in [194], taking the impacts of parasitics and the unique reverse characteristics into account. However, these methods were complicated, involving a heavy computational burden, and the effect of the temperature was not fully considered.

A power switch is typically paired with a diode as an SD cell in a PE system to provide current commutation. This basic commutation cell in Figure 5-1 is widely used in PE applications. It consists of the active power switch (S_{L}), diode (D_{H}), equivalent circuit voltage (V_{dd}) and load current (I_{L}). Note that, four configurations of S_{L}, namely Si/SiC MOSFET, Si IGBT and eGaN HEMT, are taken into account in this chapter. D_{L} is a single PIN diode, a SiC SBD, a body diode of MOSFET or an equivalent diode of eGaN HEMT (i.e. the third quadrant operation). During switching transitions, power losses result mainly from the switching and conduction losses of S_{L} as well as the conduction loss and reverse recovery loss of D_{H}. Detailed model descriptions are provided in the following section.

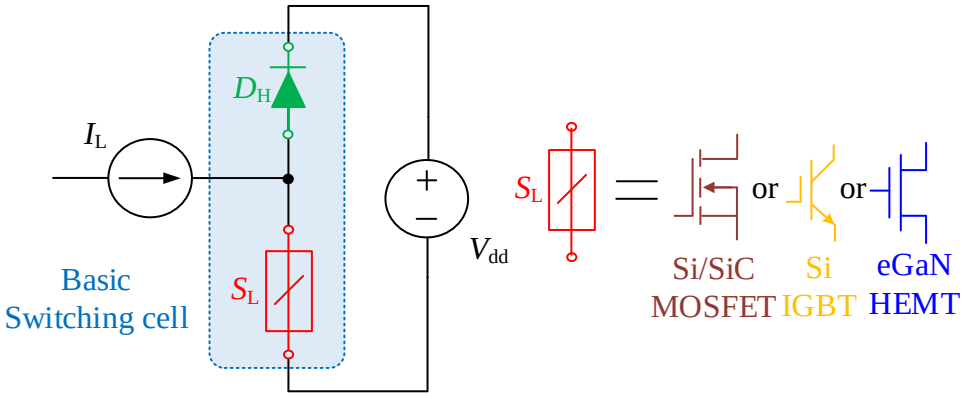


Figure 5-1 Schematic of a basic switching cell.

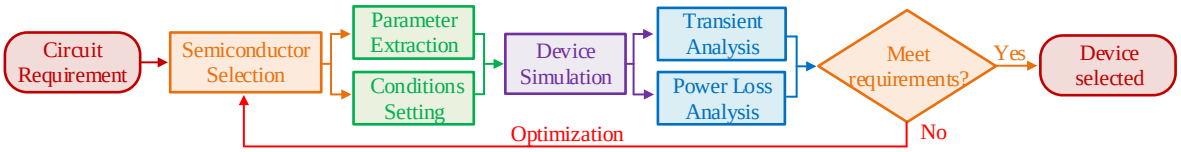


Figure 5-2 Flow chart of the modelling procedure.

5.2. Model Description

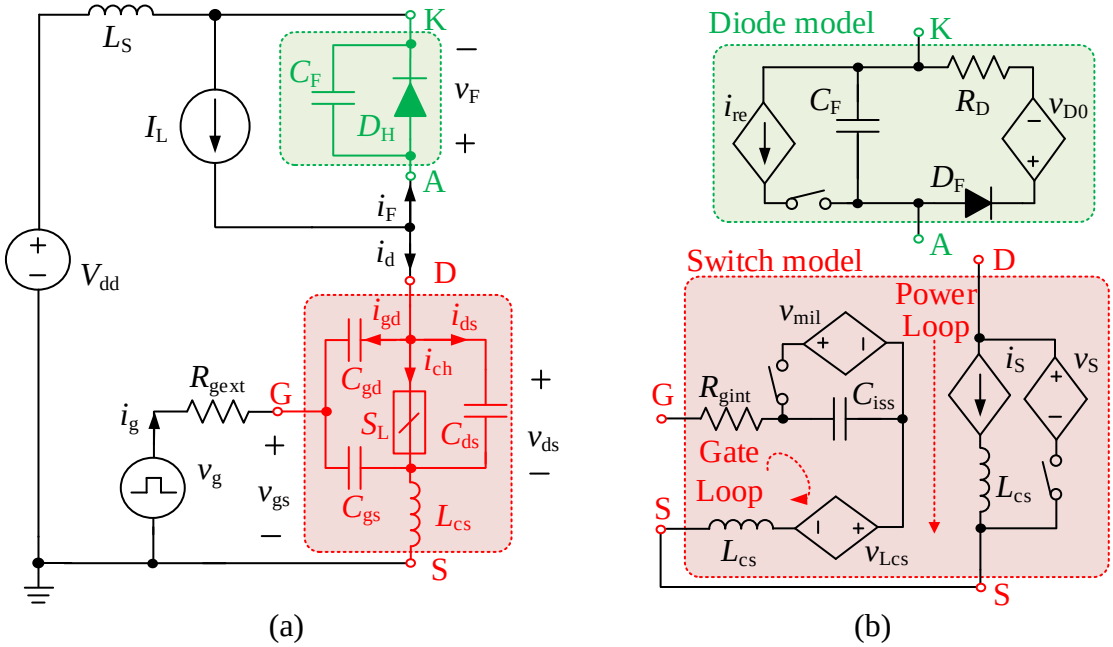
The proposed model's simulation procedure is demonstrated in Figure 5-2. Initially, the desired PE application's device requirements are determined. Based on these requirements, a specific semiconductor is preliminarily selected for modelling and characterization. According to the device's datasheet, the critical model parameters are extracted by the curve fitting method. Afterwards, the model parameters and the operating conditions are input to the proposed device model, and a DPT simulation using the proposed model is further carried out. Subsequently, the switching waveforms are obtained, and simultaneously device's power losses are computed. If the simulated results meet the acceptable range requirements, then the semiconductor is eventually selected for this application. Otherwise, it is necessary to reselect another device and evaluate the performance until the design is optimized.

To understand the SD cell's switching behaviors, a diode-clamped inductive load circuit, namely the DPT circuit, is taken as an example, which is widely used for device characterization. The basic commutation unit in Figure 5-3(a) consists of two complementary switches. One operates as a freewheeling diode D_H and the other is an active switch S_L controlled by v_g and R_{gext}. In a typical hard-switching PE system, S_L is identified by a positive drain current i_d (collector current i_c for IGBT) direction matching with the direction of I_L.

Since the commutation time is sufficiently short, I_{L} and V_{dd} are hardly changing during switching transition, and thus they are treated as a constant current source and voltage source.

The crucial circuit parasitic elements are also included, as shown in Figure 5-3(a). All the stray inductances in the power loop, including the PCB trace and device package inductances, are lumped and represented by L_{S}, while the L_{cs} of S_{L} is considered separately. In addition, the parasitic capacitances of S_{L} include C_{gd}, C_{gs} and C_{ds}. C_{F} of D_{H} denotes for the junction capacitance of the diode. It should be mentioned that when D_{H} is configured as the body diode of a switch rather than a single diode, C_{F} will be the corresponding parasitic capacitance of the switch.

During a switching transition, I_{L} commutates between S_{L} and D_{H}. When a positive v_{g} is given, the v_{gs} starts increasing to turn on S_{L}. Subsequently, i_{d} (as the sum of the i_{ch}, i_{gd} and i_{ds}) begins rising, meanwhile the i_{F} declines gradually. When S_{L} turns on completely, the v_{ds} decreases to v_{on}And the forward diode voltage v_{F} rises to V_{dd} simultaneously. The behavioral model of the SD cell, as illustrated in Figure 5-3(b), is proposed, which includes the active switch model and the diode model to reproduce the switching behaviors of S_{L} and D_{H}, respectively.



(a) (b)

Figure 5-3 (a) Equivalent DPT circuit; (b) behavioral switch-diode model.

5.2.1 Active Switch Model

Figure 5-3(b) shows that the proposed active switch model consists of two parts: the gate and power loops. It is noted that L_{cs} is shared by both loops to decouple both loops. Additionally, a corresponding v_{Lcs} is added in the gate loop to reflect the interaction impact of i_{d} on L_{cs} as mentioned in the previous chapter.

- **Gate loop part**

The external v_{g} is typically flipped between V_{gon} (20 or 15V) and V_{goff} (-5 or 0V) based on the specific gate drive requirements of the switch. For instance, v_{g} equals 15V/0V for the case of Si IGBT, 10V/0V for Si MOSFET, 18-20V/-5V for SiC MOSFET and 6V/0-3V for eGaN HEMT. The internal R_{gint} is merged into R_{gext} as the total gate resistance R_{G}. Furthermore, the sum of C_{gd} and C_{gs} are represented together as C_{iss} and an additional v_{mil}. This equivalent v_{mil} becomes valid only when the miller plateau occurs on v_{gs}. It is noticed that the gate inductance is neglected here for simplicity, although it can introduce a slight delay on v_{gs}. In fact, this delay mainly results from L_{cs} and v_{Lcs} with the fast change of i_{d}. Besides, the gate drive circuit usually is placed close to S_{L} to minimize the potential oscillation introduced by the gate inductance. Thus this inductance is negligible. Also, notice that the gate and power loop are linked by L_{cs} with v_{Lcs} and share the same source terminal.

- **Power loop part**

In the power loop part, i_{d} is represented by the dependent current source (i_{S}) which is the sum of i_{ch}, i_{gd} and i_{ds}. Note that, most of the time, i_{S} is the same as i_{ch} except for the voltage transition period when displacement currents are introduced due to the charging and discharging of parasitic capacitances. To reflect the change of voltage during switching transition as well as the on-state voltage v_{on} of S_{L}, a dependent voltage source (v_{S}) is adopted accordingly. v_{on} is determined by $R_{\mathrm{ds(on)}}$ with I_{L} or the v_{cesat} for IGBT case.

Besides, L_{cs} is also included in the power loop part, which is associated with L_{S} to influence the switching waveforms. Thereby, the gate loop and power loop parts are decoupled. Their interactions are represented by the equivalent dependent sources instead of nonlinear junction capacitances, resulting in reduced model complexity.

5.2.2 Diode Model

The static model of a diode typically is represented by an ideal diode (D_{F}), forward resistance (R_{D}) and the diode threshold voltage source (v_{D0}) based on the output characteristic of the diode in the datasheet. Typically, v_{F} for diode, on-state is computed by

$$v_{\mathrm{F}} = R_{\mathrm{D}} \cdot i_{\mathrm{F}} + v_{\mathrm{D0}}. \tag{5.1}$$

It should be mentioned that, for the case of eGaN HEMT as D_{H}, the diode behavior is realized by 2DEG and v_{F} is based on the reverse conduction characteristic of the GaN device [195], which is highly affected by the gate drive voltage (v_{GF}) of GaN device, as expressed by

$$v_{\mathrm{F}}(\mathrm{GaN}) = R_{\mathrm{Fr}} \cdot i_{\mathrm{F}} + v_{\mathrm{thF}} - v_{\mathrm{GF}}, \tag{5.2}$$

where R_{Fr} and v_{thF} are the on-resistance in the third quadrant and threshold voltage of the GaN device, respectively. Since negative v_{GF} is typically provided to avoid cross-talk issues, higher v_{F} and an increase of the conduction loss of D_{H} are resulted. If a positive v_{GF} is provided, enabling the conductive channel fully on, R_{Fr} will be the same value in the first quadrant.

Moreover, the dynamic behavior of D_{H} is described by C_{F} in parallel with the dependent current source i_{re} for the reverse recovery behavior. When D_{H} switches from forwarding conduction to off-state, i_{F} cannot be eliminated immediately. It takes a while to extinguish the excess carriers. This time is called reverse recovery time t_{rr}. The reverse recovery process occurs as soon as i_{F} becomes negative, which has been discussed in the previous chapters.

Notice that this reverse recovery behavior commonly exists in PIN diodes and body diodes of S_{L}, while the reverse recovery loss is almost eliminated for SBD or eGaN HEMT. Thus i_{re} is neglected for simplicity. In fact, in these cases, the effect of C_{F} is the primary concern that can introduce displacement current resulting in additional losses.

5.3. Switching Transient Modelling

The switching process of the SD cell in the DPT circuit is thoroughly analyzed based on the switching waveforms and the equivalent circuits to understand and model the SD cell's switching behaviors. In the following, a stepwise analysis of the modelling process is presented.

5.3.1 Turn-on Transition

The typical turn-on waveforms and power loss information are illustrated in Figure 5-4, considering the case of PIN or body diode and the case of SBD or eGaN HEMT. The equivalent circuits during this period are also provided in Figure 5-5.

Initially, S_L is in the off-state and all I_L flows through D_H. At t_0, the gate charging period begins with a positive V_{gon} applying to v_g and C_{iss} is charged up through R_G. Subsequently, v_{gs} will increase accordingly with the time constant ($\tau_{iss} = R_G \cdot C_{iss}$). It is seen from the gate charging circuit in Figure 5-5 that the existence of L_{cs} in the gate loop slows down the increase of v_{gs} and as a result prolongs the turn-on time, causing more power losses. The current rising period begins when v_{gs} goes beyond v_T. During this interval, the conductive channel of S_L is forming and i_S starts rising from zero to I_L according to the transfer characteristic of S_L.

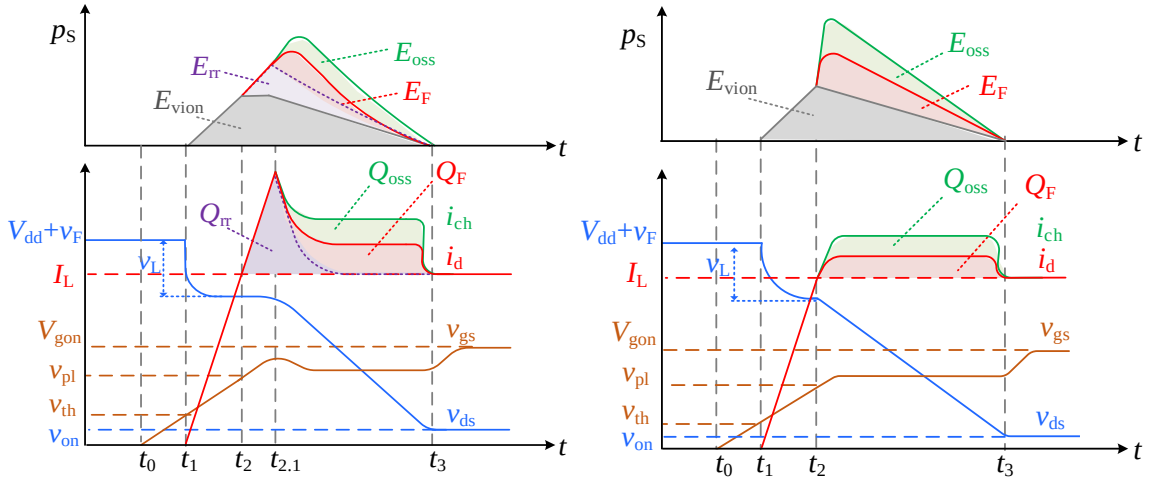


Figure 5-4 Typical turn-on waveforms with (a) PIN or body diode; (b) SBD or eGaN HEMT.

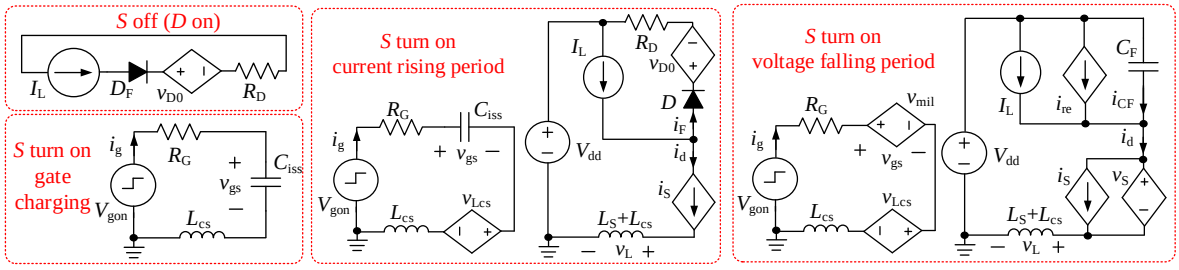


Figure 5-5 Simplified equivalent circuits during S turn-on transition, (a) off and gate charging period, (b) current rising period, (c) voltage falling period.

The fast change of i_S on the one hand, introduces a negative feedback v_{Lcs} from the power loop to the gate loop, which further delays the turn-on process. On the other hand, it results in a total voltage drop v_L on L_S and L_{cs}, which is also reflected on v_{ds} as shown in Figure 5-4.

As I_L commutates from D_H to S_L, i_S reaches I_L at t_2 and v_{gs} is clamped at v_{mil}. At the same time, i_F decreases to zero and D_H enters into reverse recovery as shown in Figure 5-4(a). This additional i_{re} will add to i_S resulting in a current spike and thus a bump in v_{gs}. When i_{re} reaches I_{rm}, it starts declining, and the voltage falling period begins. Subsequently, v_{ds} starts decreasing.This is controlled by v_S and its slew rate is determined by,

$$\frac{dv_{ds}}{dt} = \frac{dv_S}{dt} = -\frac{V_{gon} - v_{mil} - v_{Lcs}}{C_{gd} \cdot R_G}. \tag{5.3}$$

As v_{ds} keeps decreasing and v_F increases simultaneously, the C_{oss} of S_L and C_F of D_H are discharged and charged, respectively. Since the voltage of C_{oss} and C_F are clamped to V_{dd}, they share the same absolute value of voltage change. The resultant capacitive displacement current for C_{oss} (i_{oss}) and the counterpart for C_F ($i_{CF} = -C_F \cdot dv_{ds}/dt$) will affect i_d as seen in Figure 5-4. By applying Kirchhoff's law, i_d is further determined and i_S is modified accordingly to consider these displacement currents.

Consequently, during this period, i_d includes I_L, i_{re} and i_{CF}, while the additional i_{oss} is further added to i_{ch}. As a result, v_{mil} changes accordingly. This period ends when v_{ds} drop to v_{on} at t_3. After that, v_{gs} continues climbing until it reaches V_{gon}.

Furthermore, since the reverse recovery behavior is neglected for SBD or eGaN HEMT, i_{re} keeps zero, and the voltage falling period starts right after i_d reaches I_L as shown in Figure 5-4(b). Apart from that, the turn-on modelling and analysis are the same as the PIN diode case.

5.3.2 Turn-off Transition

The turn-off process is considered the opposite of turn-on transition. The typical transient waveforms and the equivalent circuits are illustrated in Figure 5-6 and Figure 5-7, respectively. To turn off S_L, the negative V_{goff} is provided as v_g and C_{iss} is discharged through R_G resulting in a reduction of v_{gs}. As v_{gs} drops to v_{mil}, the C_{gd} absorbs nearly all the i_g, meanwhile v_{ds} begins to rise, leading to a decline of i_d. When v_{ds} reaches V_{dd}, the miller plateau disappears and i_d begins decreasing with v_{gs}, resulting in an additional v_L on v_{ds} as shown in Figure

5-6(a). As v_{gs} drops below v_T, i_d becomes zero and S_L turns off completely. However, for IGBT case, the tail current (i_{tail}) needs to be considered due to the recombination of the excess carriers and the modelling detail for i_{tail} was presented in Chapter 3.

As shown in Figure 5-6(b), a notable difference for the case of eGaN HEMT is v_{gs} keeps decreasing until it reaches V_{goff} rather than clamping to the miller plateau. As a result, i_{ch} quickly declines synchronized with v_{gs}. Meanwhile, v_{ds} rises slightly and the slew rate is limited by the relatively high C_{oss} at low v_{ds}. In fact, the channel turns off thoroughly before v_{ds} significantly rises. However, i_d does not follow the fast decreasing i_{ch} since its change rate is limited by L_S and L_{cs} in the power loop. Besides, C_{oss} is charged by the current difference between i_d and i_{ch} resulting in a slight increase of v_{ds}, which is expressed as,

$$\frac{dv_{ds}}{dt} = \frac{dv_S}{dt} = \frac{i_d - i_{ch}}{C_{oss}}. \tag{5.4}$$

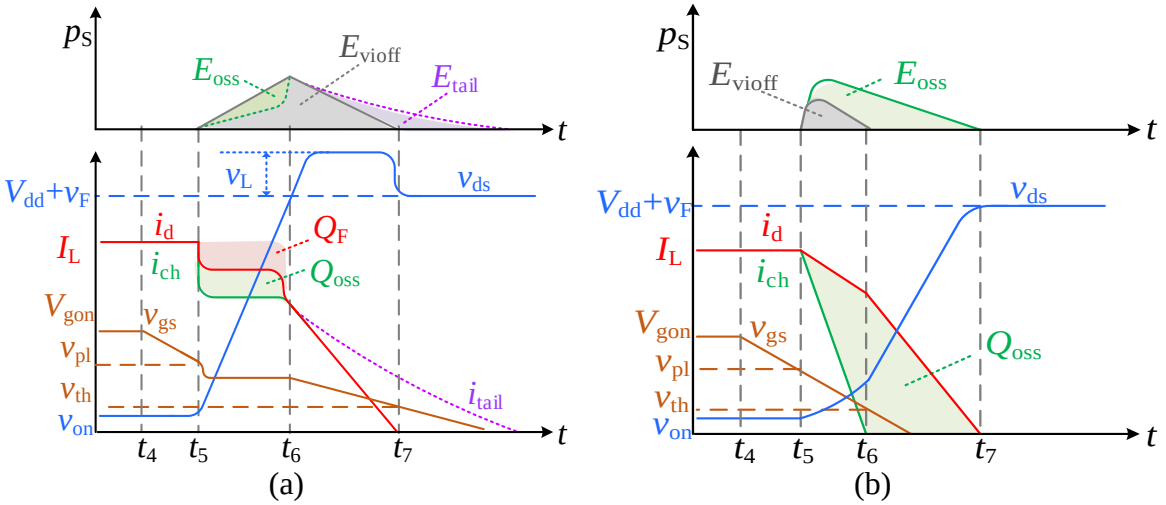


Figure 5-6 Typical turn off waveforms (a) Si IGBT or Si/SiC MOSFETs; (b) eGaN HEMT.

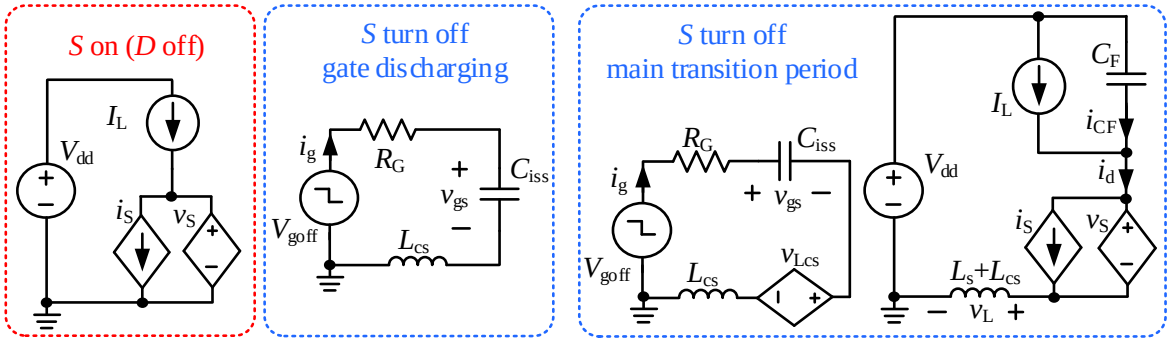


Figure 5-7 Simplified equivalent circuits during *S* turn-off transition,(a) On-state and gate discharging period, (b) main transition period.

Meanwhile, C_{F} is discharged, resulting in a reduction of v_{F}. Thus, i_{d} is obtained by

$$i_{\mathrm{d}} = i_{\mathrm{S}} = I_{\mathrm{L}} - C_{\mathrm{F}} \cdot \frac{\mathrm{d}v_{\mathrm{F}}}{\mathrm{d}t}. \tag{5.5}$$

When v_{gs} drops below v_{T}, namely i_{ch} becomes zero, the channel shuts down and I_{L} is shared by C_{oss} and C_{F}. When v_{ds} rises to V_{dd}, I_{L} commutes to D_{H} and the S_{L} turn-off transition finishes. Notice that, if large R_{G} is used for eGaN HEMT, the corresponding turn-off analysis will be the same as the case of Si/SiC MOSFET shown in Figure 5-6 (a).

Based on the above analyses, v_{S} is considered as an open circuit except for voltage rising/falling periods and S_{L} on-state. The key expressions of i_{S} is summarized as

$$i_{\mathrm{S}} = \begin{cases} 0, v_{\mathrm{gs}} < v_{\mathrm{T}} \\ g_{\mathrm{fs}} \cdot \left(v_{\mathrm{gs}} - v_{\mathrm{T}}\right), i_{\mathrm{d}} < I_{\mathrm{L}} \\ I_{\mathrm{L}} + i_{\mathrm{re}} - C_{\mathrm{F}} \cdot \frac{\mathrm{d}v_{\mathrm{ds}}}{\mathrm{d}t}, i_{\mathrm{d}} > I_{\mathrm{L}} \\ I_{\mathrm{tail0}} \cdot \exp\left(-\frac{t - t_{\mathrm{tail0}}}{\tau_{\mathrm{tail}}}\right), \text{tail current for IGBT} \\ I_{\mathrm{L}} - C_{\mathrm{F}} \cdot \frac{\mathrm{d}v_{\mathrm{F}}}{\mathrm{d}t}, \text{turn off for eGaN HEMT} \end{cases}. \tag{5.6}$$

It is noted that when v_{gs} is less than v_{T}, the conduction channel is not established, and theoretically, no current is flowing through the device. As a result, i_{S} is modelled with zero amperes under this condition in PSCAD/EMTDC, considered an open circuit.

5.4. Power Loss Analyses

In general, the power losses of an SD cell mainly include conduction loss and switching losses. Typically the conduction losses of S_{L} and D_{H} are calculated directly as the product of operating current (i.e. I_{L}) and the v_{on} of the device. Also, the reverse recovery loss of D_{H} is estimated based on the reverse recovery charge Q_{rr} and v_{F} from the device datasheet. The switching losses of S_{L} are analyzed in detail as follows.

5.4.1 Turn-on Loss

The instantaneous power of S_{L} (p_{S}) along with E_{on} are presented in Figure 5-4. Basically, E_{on} consists of the turn-on V-I overlap loss (E_{vion}), reverse recovery related loss (E_{irr}) and capacitive losses (E_{oss} and E_{F}) for C_{oss} and C_{F}, respectively. E_{vion} is graphically divided into the i_{d} rising period and v_{ds} falling period. Hence, E_{vion} is expressed as

$$E_{\mathrm{vion}} = \int_{t_1}^{t_2} v_{\mathrm{ds}} \cdot i_{\mathrm{d}}\,\mathrm{d}t + I_{\mathrm{L}} \cdot \int_{t_2}^{t_3} v_{\mathrm{ds}}\,\mathrm{d}t. \tag{5.7}$$

Since the reverse recovery behavior of D_{H} and the displacement current of C_{oss} already have been considered in the modelling of i_{S}. Therefore the sum of E_{vion}, E_{irr} and E_{oss}, which is the measured turn-on loss (E_{onm}), is directly obtained by integrating the product of i_{d} and v_{ds}. It significantly reduces the complexity comparing with the analytical loss model by computing the switching time for each sub-stages. Moreover, both the discharging current of C_{oss} and charging current of C_{F} are flowing through the channel of S, and thus these capacitive energy losses (i.e. E_{oss}, E_{F}) are dissipated into the channel. Based on the capacitance curves, E_{oss} is expressed as

$$E_{\mathrm{oss}} = \int_0^{V_{\mathrm{dd}}} v_{\mathrm{ds}} \cdot C_{\mathrm{oss}}\,\mathrm{d}v_{\mathrm{ds}}. \tag{5.8}$$

Since the charging current of C_{F} is provided by V_{dd} and part of the energy is stored in C_{F}, thus the loss dissipated in the channel (i.e. E_{F}) is derived based on the charge of C_{F} (Q_{F}),

$$E_{\mathrm{F}} = V_{\mathrm{dd}} \cdot Q_{\mathrm{F}} - \int_0^{V_{\mathrm{dd}}} v_{\mathrm{F}} \cdot C_{\mathrm{F}}\,\mathrm{d}v_{\mathrm{F}} = \int_0^{V_{\mathrm{dd}}} (V_{\mathrm{dd}} - v_{\mathrm{F}}) \cdot C_{\mathrm{F}}\,\mathrm{d}v_{\mathrm{F}}. \tag{5.9}$$

Consequently, E_{F} theoretically should also be included in E_{on} which is expressed as,

$$E_{\mathrm{on}} = E_{\mathrm{onm}} + E_{\mathrm{F}} = \int_{t_1}^{t_3} i_{\mathrm{d}} \cdot v_{\mathrm{ds}}\mathrm{d}t + E_{\mathrm{F}}. \tag{5.10}$$

5.4.2 Turn-off Loss

Generally, the power losses during the turn-off transition occur from t_5 to t_7, which include the turn-off V-I overlap loss (E_{vioff}), E_{oss} and E_{tail} for the case of IGBT. The analysis of E_{vioff} is significantly different for the slow-switching scenario in Figure 5-6(a) and the typical fast-switching for eGaN HEMT in Figure 5-6(b). As for the former case, v_{gs} is fixed at v_{mil} and thus i_{d} maintains relatively constant throughout the voltage-rising period. After that, i_{d} decreases significantly, meanwhile v_{ds} keeps relatively constant. Hence, E_{vioff} for this case is graphically calculated as

$$E_{\mathrm{vioff}} = \int_{t_5}^{t_6} v_{\mathrm{ds}} \cdot i_{\mathrm{d}}\,\mathrm{d}t + \int_{t_6}^{t_7} (V_{\mathrm{dd}} + v_{\mathrm{L}}) \cdot i_{\mathrm{d}}\,\mathrm{d}t. \tag{5.11}$$

Similarly, the sum of E_{vioff} and E_{tail}, namely the measured turn-off loss (E_{offm}), is typically an integral of the product of i_{d} and v_{ds}. It is noticed that the discharging energy of C_{F} is transferred to the inductive load during the voltage-rising period, resulting in a reduction

of i_{d}. Meanwhile, the charging energy of C_{oss} (i.e. E_{oss}) is stored and will be dissipated in the next cycle. Therefore, E_{oss} should be theoretically excluded from E_{off} as expressed

$$E_{\mathrm{off}} = E_{\mathrm{offm}} - E_{\mathrm{oss}} = \int_{t_5}^{t_7} v_{\mathrm{ds}} \cdot i_{\mathrm{d}}\,\mathrm{d}t - E_{\mathrm{oss}}. \tag{5.12}$$

As for the typical eGaN HEMT scenario, v_{gs} skips the plateau period. The channel turns off quickly before v_{ds} rises significantly. Afterwards, the energy is commutating between the inductive load and the two capacitances (i.e. C_{F} and C_{oss}), which is almost lossless. The resistive overlap loss occurs as long as the channel is on. It is significantly reduced for this case due to the low v_{ds}. Nevertheless, E_{off} still can be calculated by the above loss equations.

5.5. Parameter Extraction Procedure

The critical model parameters are directly extracted from the device datasheet's characteristic curves by curve fitting [196]-[197], to avoid the unpractical supplementary measurements. This method applies to different devices and provides a balanced trade-off between accuracy and practicability. As an example, different types of semiconductors from different manufacturers, as listed in Table 5-1, are selected to model and validate the proposed method. An extraction example is provided in the Appendix A.

5.5.1 Static Characteristic

To reproduce the switching behavior of the S_{L}, v_{T} and g_{fs} are considered first. Since v_{T} typically is a temperature-dependent parameter rather than a constant value, it is fitted by a second-order polynomial of T_{j} from the corresponding curve in the datasheet. Likewise, the transfer characteristic of S are fitted by the quadratic function of v_{gs} and subsequently g_{fs} is further determined as, where k_{ga}, k_{gb}, k_{gTa}, and k_{gTb} are fitting constants.

$$g_{\mathrm{fs}} = i_{\mathrm{s}} \cdot \sqrt{k_{\mathrm{ga}}/(i_{\mathrm{s}} - k_{\mathrm{gb}})} \cdot k_{\mathrm{gTa}} \cdot (T_{\mathrm{j}}/T_{\mathrm{a}})^{k_{\mathrm{gTb}}} \tag{5.13}$$

Table 5-1 Semiconductor selection for modelling and validation.

Device Type	Si IGBT	SiC MOSFET	Si MOSFET	eGaN HEMT	SiC SBD
Part Number	IKW40T120	SCT2080KE	NVHL072N65S3	GS66506T	SCS220KG
Manufacturer	Infineon	Rohm	On Semi.	GaN Sys.	ROHM

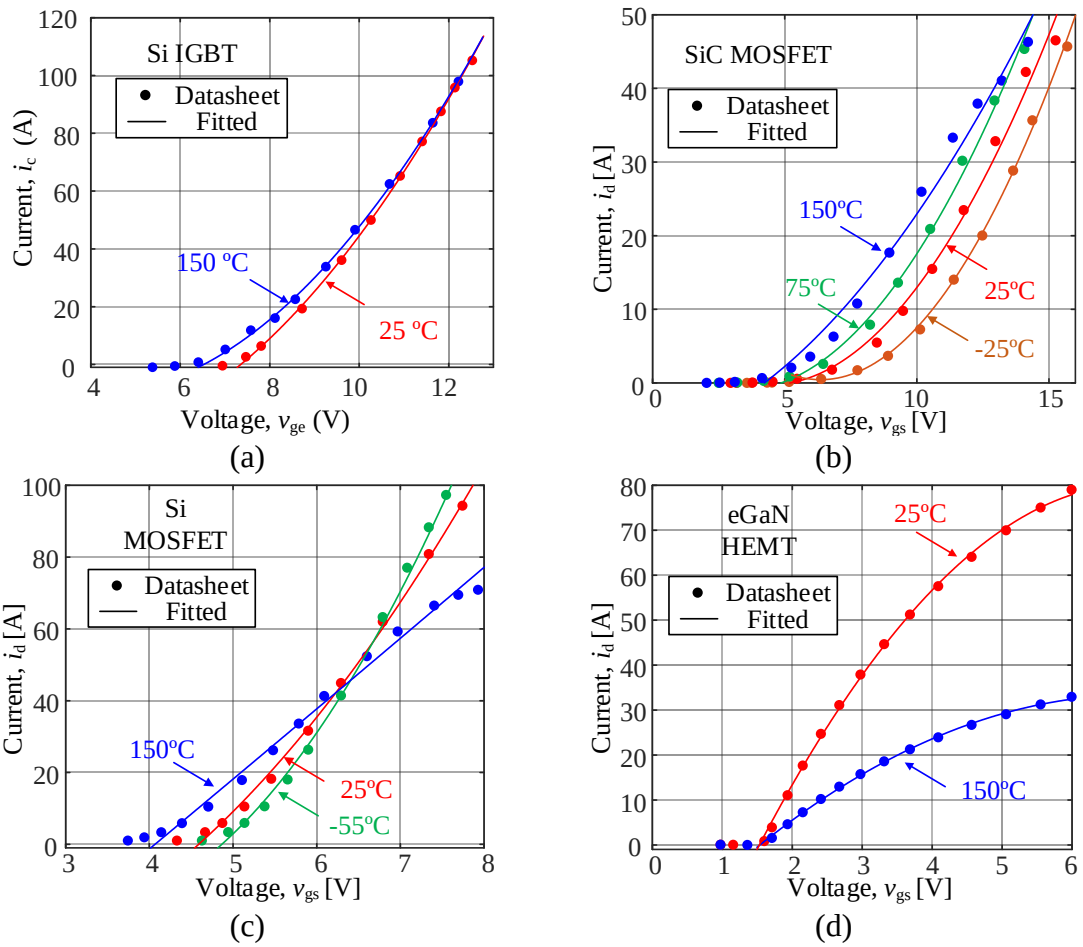


Figure 5-8 Transfer curves results for (a) IGBT; (b) SiC/ (c) Si MOSFET (d) eGaN HEMT.

In this way, the g_{fs} under the given T_{j} in the datasheet is obtained and the counterparts for other T_{j} cases are estimated by linear interpolation. The fitted results of transfer curves are compared and show good agreement with the datasheet in Figure 5-8. It is also found that there are positive correlations between T_{j} and g_{fs} for Si IGBT and Si/SiC MOSFET, while it shows a negative correlation for the case of eGaN HEMT.

Furthermore, to represent the on-state characteristic of S_{L}, the parameter v_{cesat} for IGBT or $R_{\mathrm{DS(on)}}$ for other cases is needed to be obtained. Typically, both of v_{cesat} and $R_{\mathrm{ds(on)}}$ are affected by T_{j} and i_{S} according to the curves in the datasheet. Therefore, v_{cesat} is obtained by the following equation,

$$v_{\mathrm{cesat}} = (k_{\mathrm{cea}} + r_{\mathrm{cea}} \cdot i_{\mathrm{S}}) + (k_{\mathrm{ceb}} + r_{\mathrm{ceb}} \cdot i_{\mathrm{S}}) \cdot (T_{\mathrm{j}} - T_{\mathrm{a}}), \tag{5.14}$$

where k_{cea}, r_{cea}, k_{ceb} and r_{ceb} are the fitting coefficients. T_{a} is the ambient temperature. Note that the gate voltage is assumed as a constant in the parameter extraction for simplicity.

Table 5-2 Key fitting parameters of different semiconductors.

Parameter	k_{ga}	k_{gb}	k_{gTa}	k_{gTb}	$k_{\mathrm{cea}}, k_{\mathrm{ona}}$	$r_{\mathrm{cea}}, r_{\mathrm{ona}}$	$k_{\mathrm{ceb}}, k_{\mathrm{onb}}$	$r_{\mathrm{ceb}}, r_{\mathrm{onb}}$
Si IGBT	2.05	-6.96	14.2	-0.012	-0.001	$1 \cdot 10^{-4}$	0.972	0.0215
SiC MOSFET	0.42	-0.35	2.96	-0.086	$4.1 \cdot 10^{-4}$	$1.12 \cdot 10^{-6}$	0.073	$5.1 \cdot 10^{-4}$
Si MOSFET	3.72	-19.2	13	-0.57	0.048	$2.87 \cdot 10^{-3}$	0.034	0.0012
eGaN HEMT	0.23	-777	0.51	-0.31	0.067	$7.2 \cdot 10^{-5}$	$8.4 \cdot 10^{-4}$	$4 \cdot 10^{-6}$

Likewise, $R_{\mathrm{DS(on)}}$ for the cases of MOSFET and eGaN HEMT are extracted by

$$R_{\mathrm{DS(on)}} = (k_{\mathrm{ona}} + r_{\mathrm{ona}} \cdot i_{\mathrm{S}}) + (k_{\mathrm{onb}} + r_{\mathrm{onb}} \cdot i_{\mathrm{S}}) \cdot (T_{\mathrm{j}} - T_{\mathrm{a}}), \tag{5.15}$$

where k_{ona}, r_{ona}, k_{onb} and r_{onb} are fitting coefficients. Based on the above equations, the critical parameters for different devices are extracted and illustrated in Table 5-2.

5.5.2 Parasitic Capacitance and Inductance

It is a fact that nonlinear capacitances are the key to the dynamic characteristic of the devices. Typically, the capacitance curves provided in the datasheet is in the form of $C_{\mathrm{iss}}, C_{\mathrm{oss}}$ and C_{rss}, which can be mathematically converted to the junction capacitances. Generally, these capacitances are voltage-dependent and are extracted by fitting the curves as,

$$C(v) = f(v), \tag{5.16}$$

where f is the fitting function for capacitance. Various f are used for different devices to fit the corresponding curves in Figure 5-9. It is observed that the parasitic capacitances of Si IGBT are generally higher than others. Concretely, C_{iss} of MOSFET and eGaN HEMT are comparable with C_{oss}. C_{rss} of eGaN HEMT is much smaller than the other three cases.

The device's internal inductances are usually provided in the datasheet. While the stray inductances are highly related to the device package and PCB design. There are two widely used methods for inductance extraction, namely the calculation method and the experimental method. The inductance is computationally obtained with calculation tools such as the Ansoft Q3D Extractor software based on the specifications. Based on the previous switching transient analysis, it is also extracted from the slew rate of current along with v_{L} during S_{L} turn-on transition or from the resonant frequency of the power loop in the measured results. This work's inductances are estimated based on the PCB trace length and the device package and further calibrated from the previous Chapter's switching waveforms.

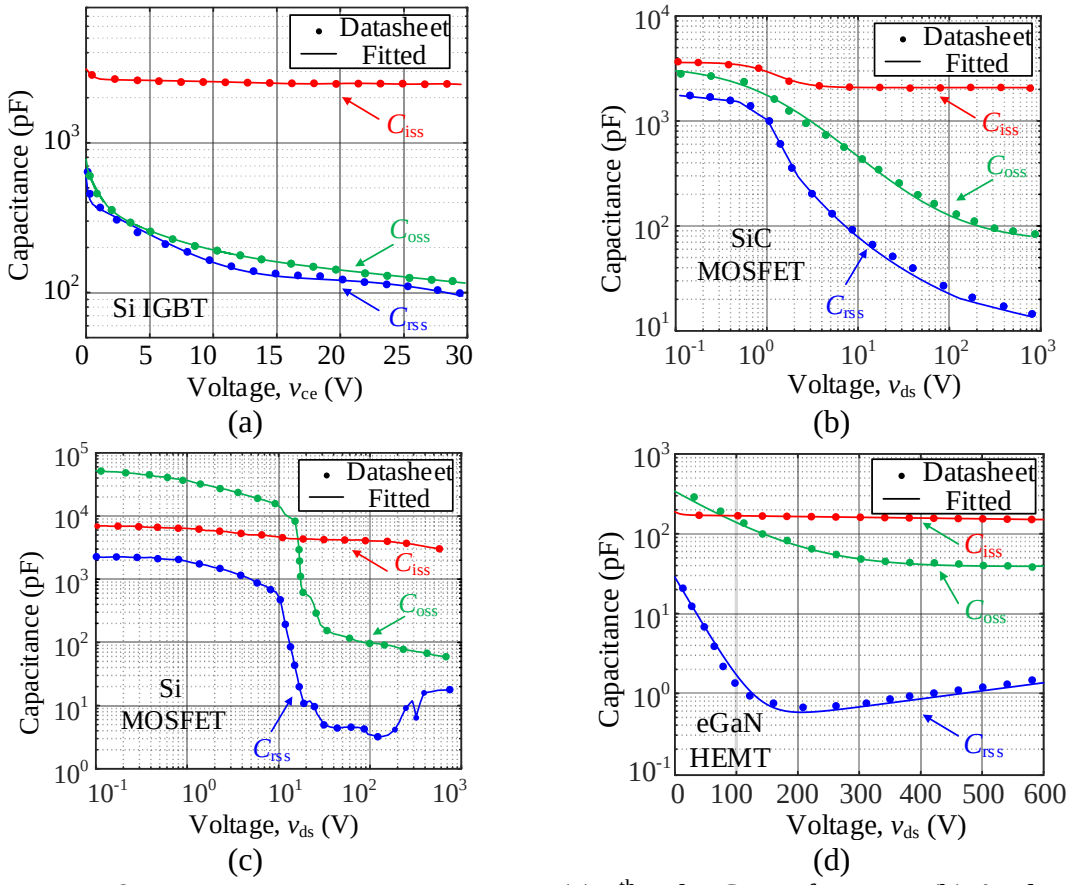


Figure 5-9 Parasitic capacitance extraction, (a) 5th order Gauss function; (b) Analytical equations in [198]; (c) Interpolant LUT; (d) 3nd order exponential function.

5.5.3 Diode Parameter

In general, R_{D} and v_{D0} are extracted directly from the diode I-V curve in the datasheet, and the values for various temperatures are estimated by linear interpolation. Furthermore, for the case of eGaN HEMT as D_{H}, the voltage drop should be fitted based on the v_{GF} of D and the output curves in the third quadrant from the datasheet. The diode I-V curve fitted results for different devices are compared with the datasheet in Figure 5-10. Notice that the conduction performance of the body diode in SiC MOSFET is generally worse than the diode of IGBT and SiC SBD. Also, the reverse voltage drop for eGaN HEMT is relatively higher due to the typical v_{GF} (i.e. -3V) resulting in considerable conduction loss. Besides, C_{F} is obtained using the same method as mentioned above for S_{L} from the capacitance curve in the datasheet. As for the diode's reverse recovery behavior, the main parameters I_{rm} and Q_{rr} are extracted from the diode curves in the datasheet as a function of T_{j} and $\mathrm{d}i_{\mathrm{F}}/\mathrm{d}t$. The details have been presented in the previous Chapter 3.

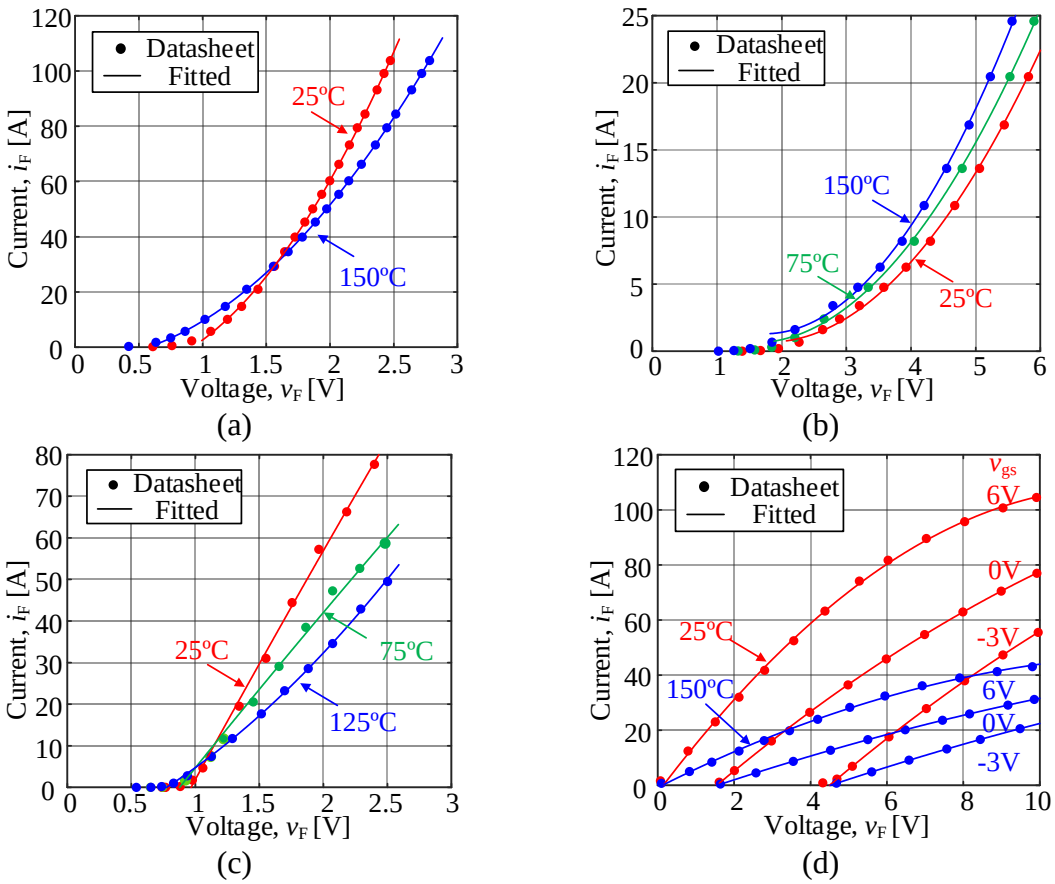


Figure 5-10 Diode parameters extraction of (a) Si IGBT; (b) SiC MOSFET; (c) Si MOSFET; (d) eGaN HEMT.

5.6. Experimental Verification

The proposed method aims to reproduce the SD cell's switching behaviors and generate the corresponding power loss LUT with reasonable accuracy and fast simulation speed. The models were implemented in PSCAD/EMTDC and validated by comparing with the experimental waveforms and power loss results in the DPT bench for different combinations.

5.6.1 Setup Description

An automatic DPT bench was designed and built for device characterization and loss measurements. Since the gate-drive requirements and device package are different for various devices, three daughter boards were designed accordingly with external input voltage (up to 1kV) and the inductive load (5mH). The daughterboard for eGaN HEMT is illustrated in Figure 5-11, and other boards for IGBT and MOSFET have been given in previous chapters.

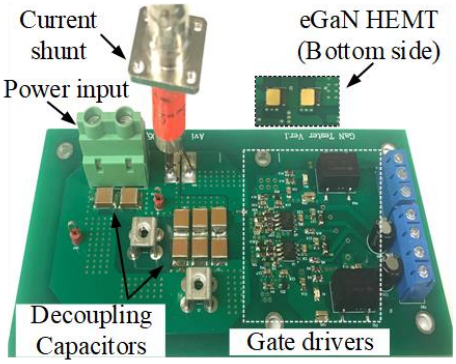


Figure 5-11 Device characterization DPT setup for eGaN HEMT.

Probes and oscilloscopes of adequate bandwidth are necessary to capture the switching transients. Tektronix voltage differential probe THDP0200 and current probe TCP0030A are used for Si IGBT/MOSFET measurements. Passive voltage probe (TTP800) and 0.1Ω current shunt resistor (SDN-414-01) are adopted for SiC MOSFET and eGaN HEMT measurements. Also, a 350 MHz Oscilloscope MSO5034B is used to record the switching waveforms. The temperature is controlled by a heating block and monitored by a thermal imager (Fluke, TiS40).

In the DPT, the desired test conditions are initially set in the computer, and the Arduino gives all the control signals. Afterwards, the DC capacitor bank is charged to the desired voltage, and the device is heated to the desired temperature. When voltage and temperature conditions are ready, two gate pulses are given in sequence to switch the Device Under Test (DUT). The switching waveforms are obtained by oscilloscope and processed in the computer for further analyses. It is necessary to calibrate the probes to mitigate measurement errors due to the asynchrony of voltage and current. Additional delay time adjustments for the transient waveforms are also needed. The calibration time of probes and waveforms is provided in Table 5-3, taking the current as the reference. The calibrating fixture (067-1686-02) from Tektronix was used to calibrate the probes. 10 MHz sinusoidal signals were applied to both probes, and the deskew time for the voltage probes is adjusted until both measurements are synchronized.

Table 5-3 Calibration time of probes and waveforms.

DUT case	Si IGBT	SiC MOSFET	Si MOSFET	eGaN HEMT
Probes calibration (ns)	48	26	45	23
Turn-on calibration(ns)	35	13	26	14
Turn-off calibration(ns)	31	18	25	12

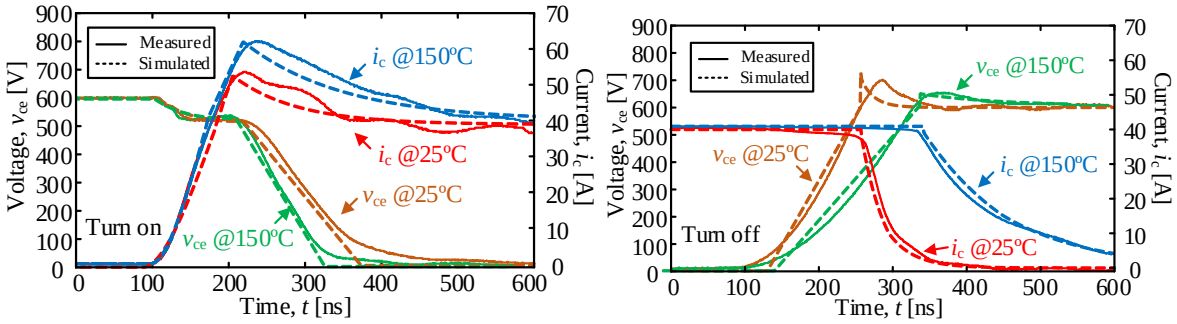


Figure 5-12 Switching waveforms of Si IGBTs (a) turn-on; (b) turn-off.

5.6.2 Switching Transient Verification

- **Si IGBT**

The daughterboard in Section 3.5 was used for Si IGBT and MOSFET test, and v_g is flipped between 15V and 0V to control the S_L on and off, respectively. The simulated results of the switching waveforms for IKW40T120 are compared with the DPT measurements in Figure 5-12. The results demonstrate good agreement between the simulated and measured switching waveforms under 25℃ and 150℃. The switching details such as tail current and the current spike resulting from the reverse recovery of D_H is clearly observed. In addition, v_{ce} slightly drops to 500V during the current rising period and reaches a peak of 700V during turn-off transition because of the parasitic inductances. Besides, as T_j increases from 25℃ to 150℃, the reverse recovery behavior of D_H becomes more obvious resulting in higher current peak (up to 60A). Also, the rise of v_{ce} and the decline of i_c during turn-off period slow down, resulting in an increased switching power losses.

- **SiC MOSFET**

As given in Section 4.4, a more compact DPT daughterboard was designed to mitigate the parasitics' effect, resulting from the fast switching SiC MOSFET. Additionally, the IC (IXDN609SI) was adopted as the gate driver to provide 20V/-5V drive voltage for the SiC MOSFET. Figure 5-13 shows the simulated switching waveforms of SiC MOSFET under the conditions of 600V and 20A, which match well with measured results. It is observed that there is only a slight impact of T_j on the switching transients in terms of turn-on and turn-off time. Nevertheless, the current can still reach almost 40A during the turn-on transition due to the diode's reverse recovery behavior. It is found that a current ringing occurs during switching

transitions because of the parasitic resonance. The high-frequency damping resistance generally consumes this energy in the circuit. Since the voltage or current has dropped to a low level, this loss is considered lossless and negligible for simplicity.

- **Si MOSFET with SiC diode**

Figure 5-14 provides the Si MOSFET's DPT results with the SiC diode using the same daughterboard for the Si IGBT case. In general, the simulated results are in good agreement with the measured results for different R_{gext} conditions. As R_{gext} increases from 10Ω to 33Ω, a half less voltage drop of v_{ds} is observed during the turn-on transition due to the slower current rising speed. Likewise, only a slight increase of v_{ds} is seen after v_{ds} climbs to V_{dd}. Moreover, it is noticed that the current spike is significantly limited comparing with the previous test results using PIN diode due to the merit of zero reverse recovery for SiC SBD. However, there is still a slight current bump causing by the resonance of parasitic elements and the capacitive displacement currents, as discussed previously.

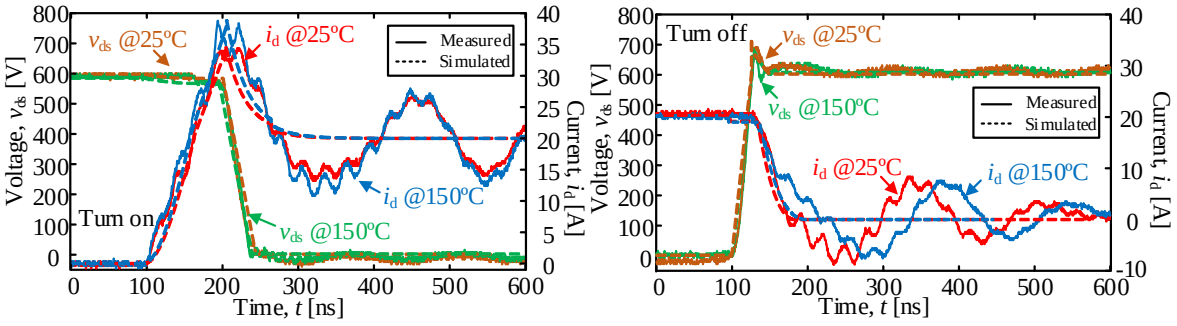


Figure 5-13 Switching waveforms of SiC MOSFETs (a) turn-on; (b) turn-off.

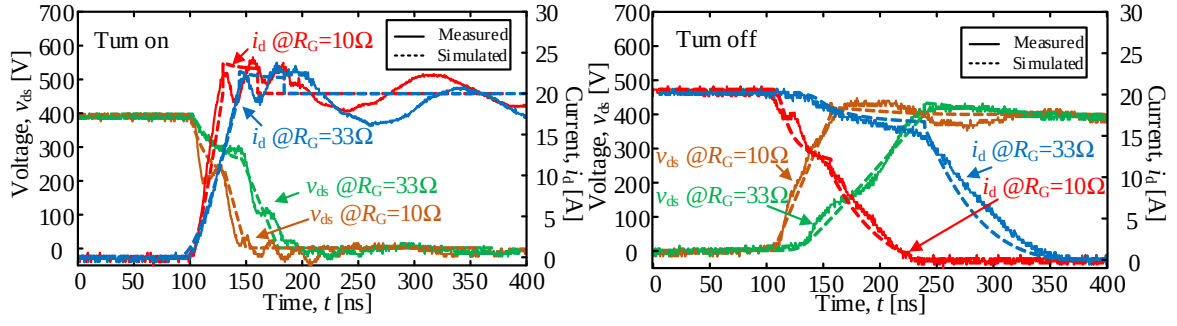


Figure 5-14 Switching waveforms of Si MOSFET with SiC SBD (a) turn-on; (b) turn-off.

- **eGaN HEMT**

A specific DPT daughterboard was built to fulfill the requirement of eGaN HEMT as a surface-mount device (SMD). The gate driver provides 6V/0V as v_g to control the low-side GaN switch S_L, while the high-side SiC SBD serves as a freewheeling diode when S_L turns off. The simulated switching results are compared with the measurements for the two operating conditions, namely, $v_{ds} = 300\text{V}, i_d = 10\text{A}$ and $v_{ds} = 150\text{V}, i_d = 5\text{A}$, as shown in Figure 5-15. It is observed that the simulated results are consistent with the experimental results. From the turn-on waveforms in Figure 5-15(a), it is observed that the current rising time is only tens of nanoseconds. After i_d reaches I_L, it behaves in the similar manner as previous test using Si MOSFET with SiC SBD, and the current ringing is still observed. However, during the turn-off period, it is observed that, i_d declines significantly and drops to zero almost the same time as v_{ds} reaches steady state. While for the other cases of the devices, the fast decrease of current typically occurs after v_{ds} climbs to V_{dd}. This is mainly because the conductive channel of eGaN HEMT shuts down very fast before v_{ds} increase significantly as discussed previously. Hence, when the channel turns off completely, the apparent i_d is dominated by the capacitive displacement current, which is highly related to the change of v_{ds}.

5.6.3 Power Loss Verification

With the aim of power loss verifications for various devices, the switching losses, including turn-on and turn-off losses, are measured in the DPT and compared with the simulation using the proposed approach. During the switching transients, p_S, which is the product of voltage and current, is obtained using math function in the oscilloscope. Similarly the E_{onm} and E_{offm} are further obtained by integrating p_S.

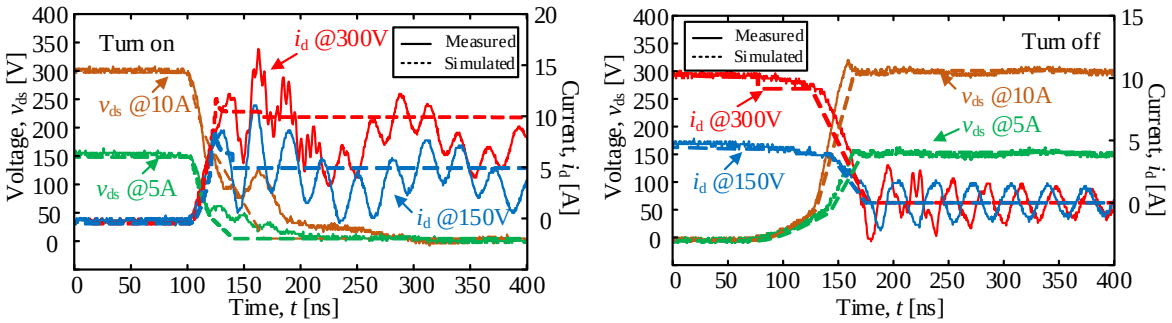


Figure 5-15 Switching waveforms of eGaN HEMT with SiC SBD (a) turn-on; (b) turn-off.

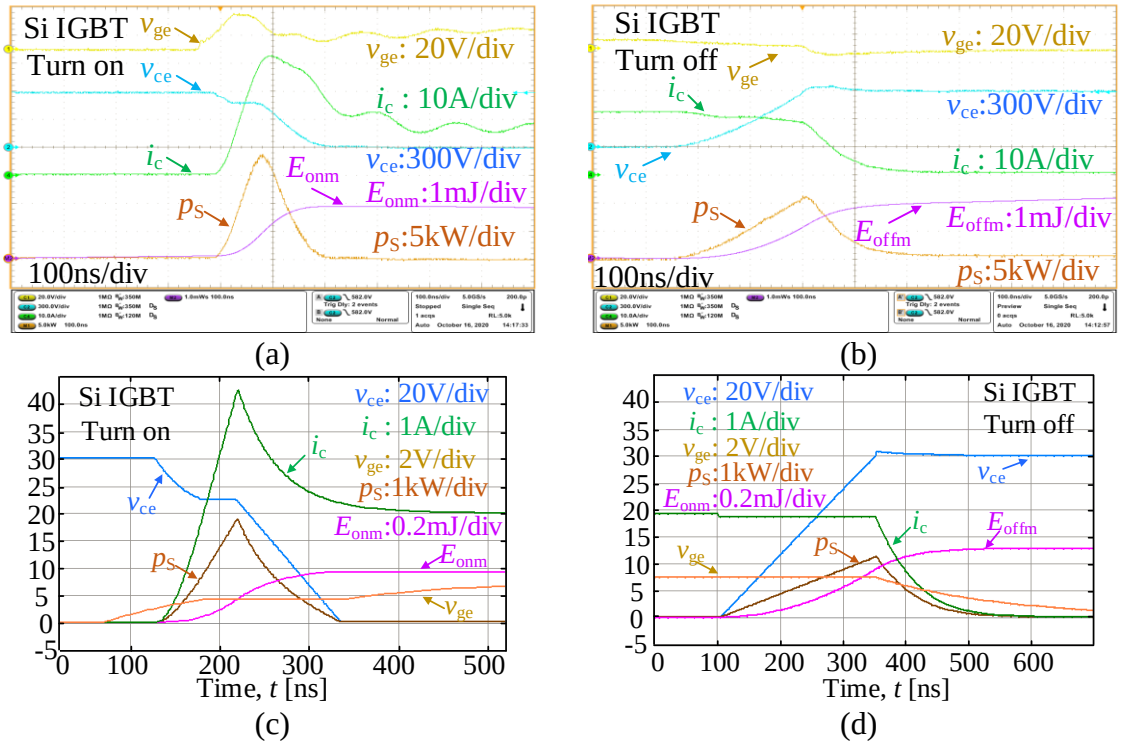
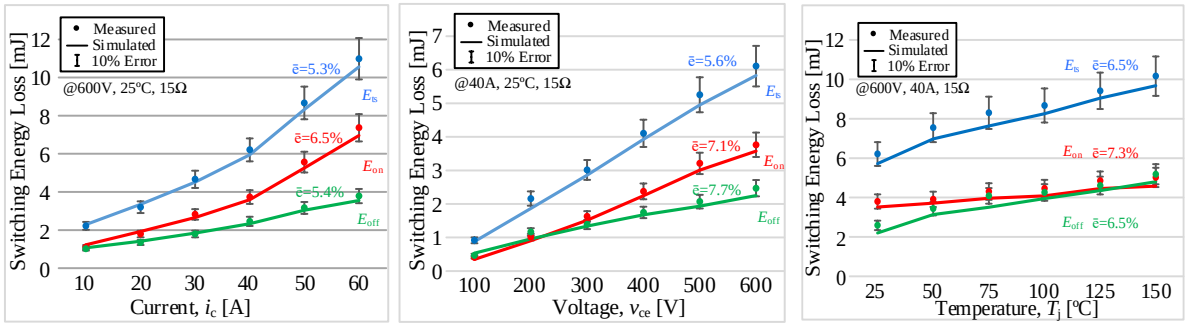


Figure 5-16 Si IGBT measured (a) turn-on and (b) turn-off waveforms, and simulated (c) turn-on and (b) turn-off waveforms @600V, 20A, 25℃, 15Ω.

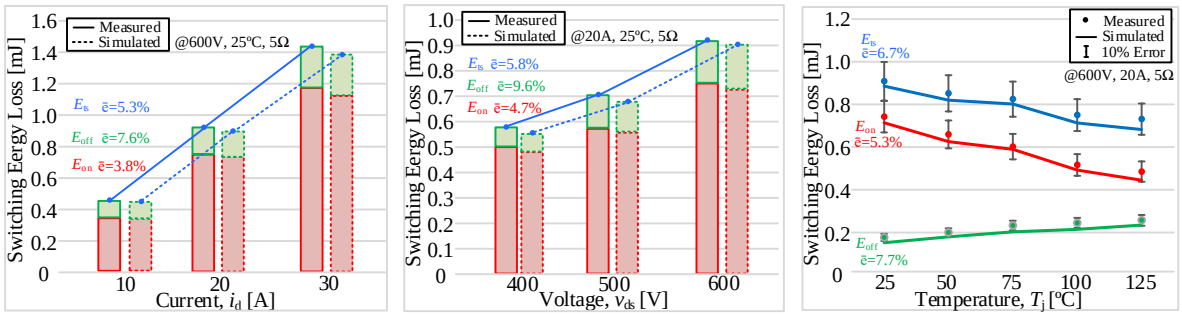
As mentioned previously, the current and voltage probes are calibrated for each test. The additional delay time is added to the waveforms to keep transient voltage and current synchronous. The captured test waveforms and simulated waveforms under the same test conditions are demonstrated in Figure 5-16, taking Si IGBT as an example. By comparing the measured results with the simulated results, a good agreement is seen in terms of not only transient v_{ce} and i_c waveforms but also computed p_S, E_{onm} and E_{offm}. Notice that, a significant bump of p_S occurs due to the overlap of the v_{ce} and i_c during switching transition. Furthermore, the measured power loss results are compared with the simulated loss results for different devices under various operating conditions to validate the proposed method. The average error ($\bar{e}$) is calculated by averaging the error's absolute value in each case.

Figure 5-17 shows the power loss results of Si IGBT under different currents, voltage, and temperature conditions. Generally, E_{ts} increases as the operating voltage and current increase, and E_{off} is less than E_{on} except for high temperature conditions. From the comparison results, it is seen that the average errors of E_{ts} are within 7%, namely 5.3%, 5.6%, and 6.5% for different operating conditions of current, voltage, temperature, respectively.



(a) (b) (c)

Figure 5-17 Si IGBT loss results under different (a) I_L; (b) V_{dd}; (c) T_j.



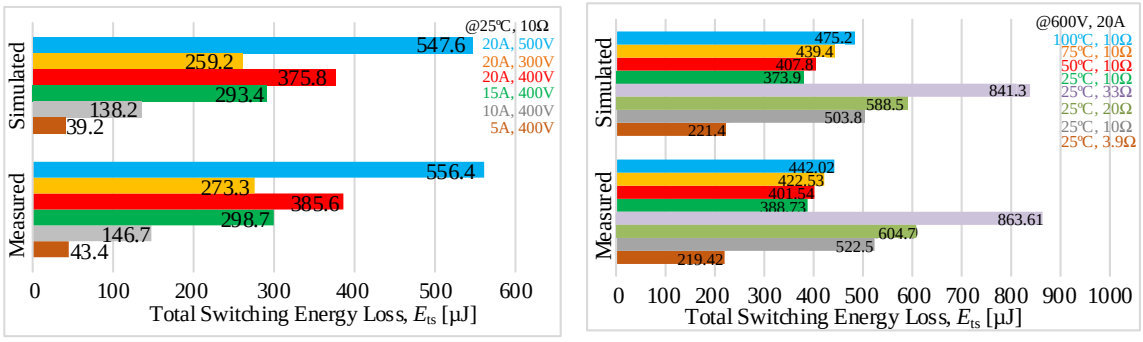
(a) (b) (c)

Figure 5-18 Power loss results of SiC MOSFET under different (a) I_L; (b) V_{dd}; (c) T_j.

Likewise, the power loss comparison results for the SiC MOSFET are illustrated in Figure 5-18. Notice that E_{ts} for SiC MOSFET is typically less than 1mJ, which is much less than the counterpart of Si IGBT for similar conditions. It is also found from Figure 5-18(c) that there is a negative correlation between E_{on} and T_j. Since E_{on} is the dominated loss, as T_j rises, E_{ts} reduces accordingly though E_{off} increases slightly. It is also noted that $\bar{\varepsilon}$ of E_{off} for various conditions are more than 7%, while $\bar{\varepsilon}$ for E_{on} and E_{ts} are still within acceptable range. The reasons for the loss deviation are the underestimations of parasitics, ringing loss and measurement error. A relatively small amount of loss deviation can still result in a high error percentage when the overall loss is relatively low.

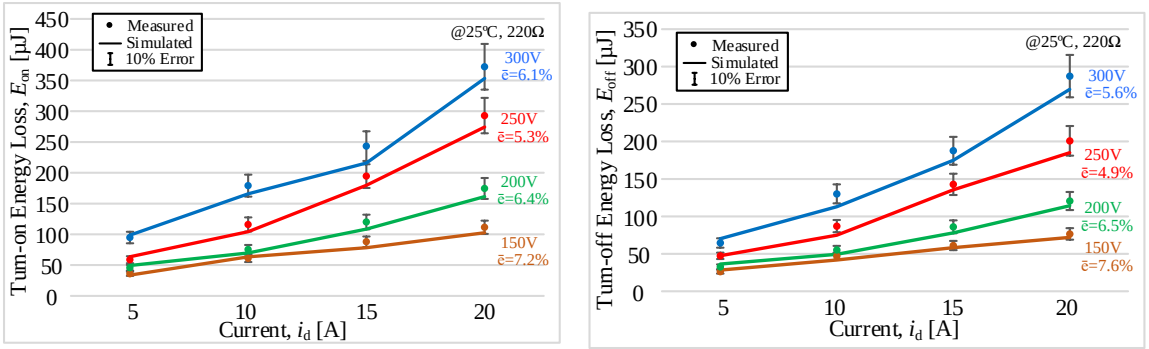
Figure 5-19 shows the E_{ts} results for the combination of Si MOSFET and SiC SBD as the SD cell under various voltage and current conditions using 10Ω as R_{gext}. It is observed that E_{ts} increases two times as the voltage rises from 300V to 500V. Also, a significant increase of E_{ts} is observed as current rises from 5A to 20A, while only a slight increase of E_{ts} is found as the operating temperature rise from 25℃ to 150℃. However, E_{ts} increases significantly when 33Ω R_{gext} is used comparing with the counterpart for 3.9Ω, which indicates the importance of R_{gext}

selection to control the switching loss. Overall, the proposed approach enables the attainability of loss information under various conditions. Moreover, the power loss results for the case of eGaN HEMT with SiC SBD are illustrated in Figure 5-20. It should be mentioned that, to capture the switching waveforms and the power loss with reasonable accuracy, a 220Ω R_{gext} is used to relatively sacrifice the switching speed and avoid shoot through issues due to the very low v_{T} of GaN. A good agreement is achieved at various testing conditions comparing with the simulated and measured results. The error is within an acceptable range, although the ē of E_{off} is slightly higher.



(a) (b)

Figure 5-19 Power loss results of Si MOSFET under various (a) V_{dd} and I_{L}, (b) T_{j}.



(a) (b)

Figure 5-20 Power loss results of eGaN HEMT with SiC SBD (a) turn on, (b) turn off.

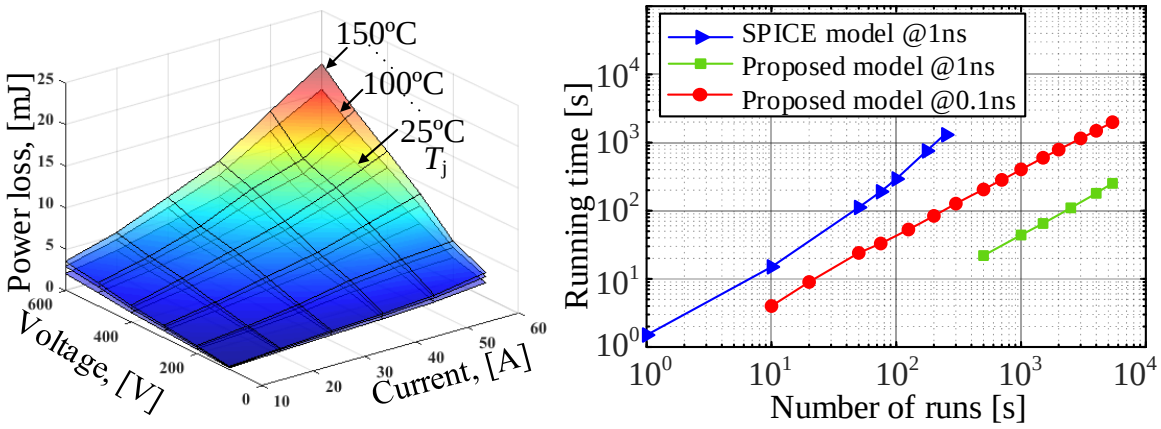
5.6.4 Discussion

Accuracy- Compared with the original two-state resistance switch model in PSCAD/EMTDC, the proposed model can reproduce the transient switching waveforms considering various impacts of parasitics, diode behavior and temperature. The multi-dimensional power loss LUT in Figure 5-21 (a) also is obtained simultaneously. The average error is within 10% comparing with measured results for various devices under various

conditions. No significant advantage is found in the modelling accuracy using the proposed model comparing to the traditional physical models or analytical models due to the ignorance of parasitic resonance and some linear assumptions. Nevertheless, the proposed model's complexity is reduced significantly with no state equations and numerical calculations. Moreover, all the model parameters are extracted from the datasheet.

Efficiency- The proposed model uses equivalent dependent sources to represent the device's characteristics based on the analytical equations. Complicated numerical calculations and solving physical equations are unnecessary, which can boost simulation efficiency and avoid convergence. There are numerous permutations to be considered to obtain an accurate power loss LUT with a wide range of operating conditions. Thus thousands of simulation runs are required instead of repetitive DPTs. For example, it requires around 5400 simulation runs to cover the operating range, namely 20V to 600V(20V step), 2A to 60A(2A step), and 25℃ to 150℃ (25℃ step). Figure 5-21(b) demonstrates the time cost of using the manufacturer's SPICE model and using the proposed model in PSCAD. The simulation time-step requires to be set one nanosecond or less to achieve reasonable accuracy. Notice that it takes thousands of seconds to finish around 200 runs in SPICE. In contrast, less than ten times the running time is needed using the proposed model with a smaller time-step. Furthermore, to cover the whole operating range, the proposed model takes less than 300s without any convergence issues, which shows the merit of time-saving in generating the power loss LUT.

Applicability- The proposed approach can reproduce the switching waveforms and obtain the power loss LUT of the SD cell. It applies to various devices such as Si IGBT, Si/SiC MOSFET, eGaN HEMT, and SiC SBD. When it comes to other devices with a new structure, such as Cascade GaN, modifications are needed. For a specific device, the curve fitting functions and algorithms for parameter extraction are required to be adjusted for good fitting results. Apart from PSCAD, the proposed approach can also be applied to simulators such as Simulink and PLECS with modifications. The proposed model also provides insights into the device behaviors with clear descriptions. As a result, it is more easily apprehensible than mathematical equations. Conversely, analytical loss models usually are limited to a specific device type or combination, and thus it is difficult to extend the models to various PE applications for loss estimation. Loss measurements are time-consuming, costly, and challenging, especially for WBG devices due to the fast switching speed.



(a) (b)

Figure 5-21 (a) Generated power loss LUT for Si IGBT; (b) Time cost comparison.

5.7. Chapter Conclusion

In this Chapter, a generalized behavioral modelling approach of the switch-diode (SD) cell for power loss prediction was proposed, implemented in PSCAD/EMTDC and validated by experimental results in DPT benches. This SD cell model consisted of an active switch model and a diode model. It was used for different semiconductors, including Si IGBTs, Si/SiC MOSFETs, eGaN HEMTs and SiC SBDs. This chapter's modelling approach and power loss analyses were based on the switching analyses in the DPT circuit. Further, the SD cell's static and dynamic characteristics were modelled by dependent sources with passive components. The impacts of the parasitic elements, diode and temperature-dependent parameters on switching performance were considered. Besides, the extraction procedures of the model parameters were introduced by curve fitting from the device datasheets. Moreover, the switching transients and power loss verifications were conducted for different devices under a wide range of operating conditions. A good agreement between the simulated and measured results in DPTs was achieved with less than 10% average error.

The model in this chapter was a generalization of the counterparts in Chapter 3 and Chapter 4. It further extended to the case of eGaN HEMT. Consequently, this modelling approach was able to provide a good balance in terms of accuracy and efficiency.

Chapter 6 Case Study- Efficiency Evaluation of a Single-Phase Grid-Tie PV Inverter Using Modern Semiconductors in Electromagnetic Transient Simulation

- A part of the work presented in this chapter is the result of original work published under **Y. Xu**, C. N. M. Ho, and K. K. M. Siu, "The Efficiency Enhancement of a Single-phase Single-stage Buck-boost type Manitoba Inverter Using SiC MOSFETs for Residential PV Applications," in *Proc. IPEMC ECCE Asia*, Nov. 2020, pp. 729-734.

This chapter's main idea is to apply the simulation methods from Chapter 3 to Chapter 5 to evaluate and optimize a PE system. A single-phase grid-tie PV inverter [199] is selected as a case study. The reason is that the topology requires various switching devices operating at a wide range of switching frequency (f_{sw}) and input voltage. In order to find a suitable device selection for various switching devices, a comparative study on the static and dynamic characteristics of SiC/Si MOSFETs, Si IGBTs and diodes has been conducted. Also, a power loss analysis of various switches has been developed using the previous simulation approaches. As a result, a mixed device combination including various switches is determined for this application to fully utilize different devices' characteristics and achieve low power losses. Consequently, a PV inverter prototype has been built to evaluate the simulated efficiency and validate the proposed methods.

6.1. Introduction

Solar photovoltaic (PV) is one of the most promising energy resources because it is eco-friendly, noiseless and inexhaustible. In many countries, such as Germany and Switzerland, grid-tie PV inverters are widely used as the necessary interfaces between PV panels and utilities [200]-[202]. It is a fact that solar irradiance keeps varying throughout the day, as shown in Figure 6-1 [203]. As a result, the output DC voltage of PV panels can fluctuate typically between 120V to 500V. It is found that less than half of the peak power is generated for PV inverters most of the day. Hence, in most cases within the design range of 1-2kW, residential PV inverters are required to have the ability to operate in both buck and boost modes.

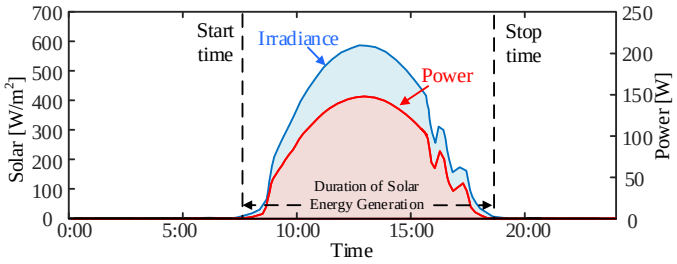


Figure 6-1 Measured irradiance and PV output power [203].

In the past few decades, various types of efficient PV inverters have been developed, classified into single-stage and two-stage topologies. A single-stage PV system typically contains one DC/AC stage, which is generally cost-effective and efficient. A two-stage PV system, including DC/DC and DC/AC stages, is a mature technology and is straightforward for controller design. Nevertheless, more switches are required resulting in higher device losses comparing to the single-stage counterpart. A family of new single-stage transformer-less topologies for grid-tie PV systems [204]-[206] has been developed considering both system structures' advantages and drawbacks. Those topologies could eliminate Common-Mode (CM) voltage and mitigate leakage current. However, as switching frequency f_{sw} increases, the increased switching losses become significant. Therefore, a suitable device selection is highly desirable for efficiency enhancement and further system optimization.

6.2. System Configuration

The topology of the Manitoba inverter (MBI) [199] is illustrated in Figure 6-2. It is capable of converting the DC output voltage of PV arrays (v_{DC}) into AC grid voltage (v_G), meanwhile delivering sinusoidal grid current (i_G) to grid with low harmonics. Basically, there are three types of switches, namely high-frequency (HF) switches (S_{HF}), line-frequency (LF) switches (S_{LF}) and capacitive switches (S_C). Notice that S_{HF} consists of switches S_1 and S_2 along with anti-parallel diodes D_1 and D_2. Likewise, S_{LF} is comprised of switches S_3 and S_4 with associated diodes D_3 and D_4. In addition, S_C includes switches S_A and S_B connecting to the Line (L) and Neutral (N) of grid, respectively, which are realized by two back-to-back switches (S_{A1}, S_{A2}, S_{B1}, and S_{B2}) to provide bi-directional blocking and conducting functions. Besides, the PV output DC link, name DC capacitor (C_{DC}) is connected with the AC grid through an additional capacitor (C_A) and S_C. And two inductors (L_1 and L_2) are used for shaping the grid current. One works with C_A forming a LC filter and the other operates as a power inductor.

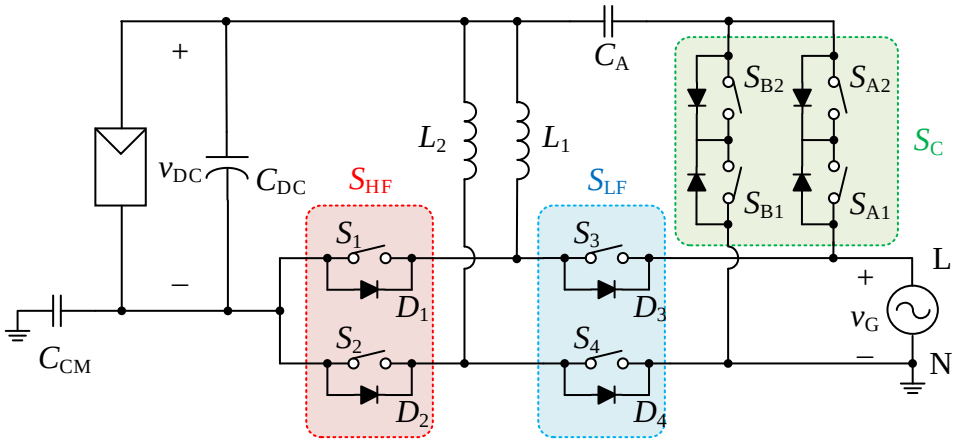
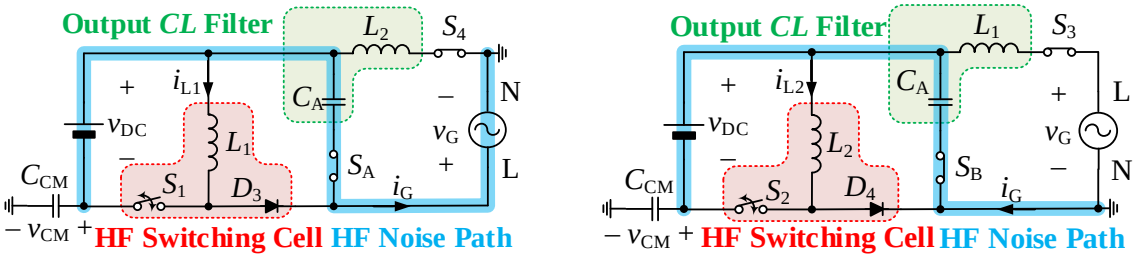


Figure 6-2 The schematic of Manitoba Inverter [199].

6.2.1 Principle of Operation

The equivalent circuits and steady-state waveforms of MBI are given in Figure 6-3 and Figure 6-4. In this MBI, the switching devices are operated as the complementary pairs $S_1/D_3/S_A/S_4$ and $S_2/D_4/S_B/S_3$ in accordance with the polarity of the grid voltage v_G. Notice that, in each half line cycle, there is only one S_{HF} that is under HF switching operation for shaping the inductor current, while others (i.e. S_C and S_{LF}) operate at LF. Essentially, the PV inverter is converted into an equivalent buck-boost converter. All the time, one inductor acts as the converter-side inductor, while the other inductor cooperates with C_A forming a *CL* filter to achieve low differential mode current ripple in the grid. Since C_A is always coupled between DC link and AC grid, the potential difference (v_{CM}) across the parasitic common mode capacitor (C_{CM}) is clamped. Thus the system leakage current is alleviated.

As shown in Figure 6-3(a) and Figure 6-4, in the positive half-line cycle, a buck-boost switching cell is formed by S_1, D_3 and L_1, while S_4 keeps conducting to provide a current return path of the circuit. Similarly, S_A also keep on-state to help linking up the connection between C_A and L terminal of grid. During turn-on period (T_{on}) of S_1, L_1 is charged by v_{DC}. The current (i_{L1}), flowing through S_1, increases gradually. Meanwhile, i_G is provided by the discharging current of C_A and filtered by the grid-side inductor L_2. When S_1 is in the turn-off period (T_{off}), i_{L1} commutes from S_1 to D_3, and C_A begins being charged by the difference between i_{L1} and i_G. Consequently, the additional capacitor helps to filter the HF current ripple in the system, and a low noise rectified grid voltage is always applied across C_A. In the negative half cycle, the other set of switching cell cooperates with C_A and L_1 as CL filter.



(a) (b)

Figure 6-3 Equivalent circuits of MBI, (a) Positive and (b) Negative cycles.

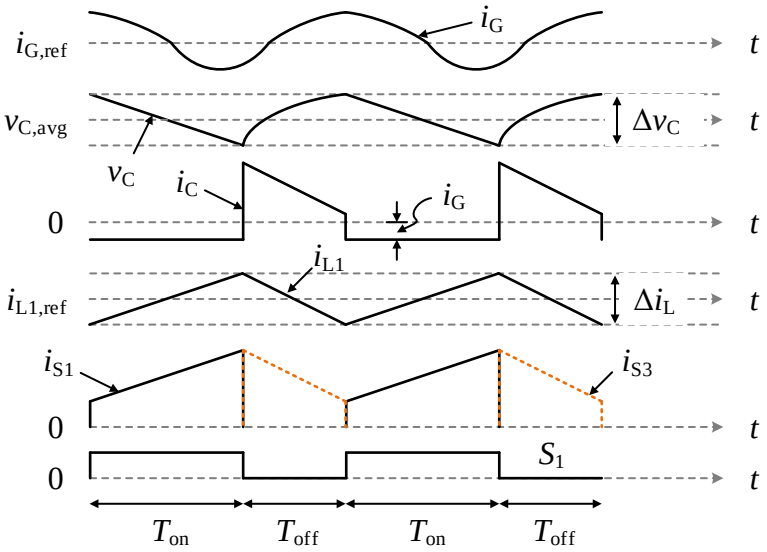


Figure 6-4 Steady-state waveforms in the positive cycle.

6.2.2 Static Characteristics Analysis

As mentioned above, the MBI system is modelled as a buck-boost converter in each half-line cycle. Hence, the static characteristics are described by the characteristics of the buck-boost converter. The critical parameters of the MBI are studied as follows.

- **Duty Ratio**

According to the circuits in Figure 6-3, the operation of MBI is considered as a simple buck-boost converter with an additional CL filter. Hence, the duty ratio D is expressed as

$$D = |v_G|/(|v_G| + v_{DC}). \tag{6.1}$$

- **Output AC Grid Current**

Since the control objective of MBI is to provide sinusoidal output current in phase with v_G, thus i_G is considered as following equation, where I_G is the amplitude of i_G.

$$i_G = I_G \cdot \sin\omega t. \tag{6.2}$$

- **Buck-boost Inductor Current**

Notice that, during each half cycle, the inductor current i_{L} is the same as the dc current (i_{DC}) when S_{HF} is on. Under the assumption of no power losses, i_{L} is computed as

$$i_{\mathrm{L}} = i_{\mathrm{DC}}/D = |i_{\mathrm{G}}| \cdot (v_{\mathrm{DC}} + |v_{\mathrm{G}}|)/v_{\mathrm{DC}}. \tag{6.3}$$

Further, the inductor current ripple is expressed as,

$$\Delta i_{\mathrm{L}} = v_{\mathrm{DC}} \cdot D/(f_{\mathrm{sw}} \cdot L). \tag{6.4}$$

6.2.3 Device Requirements

This work focuses on the commercial single-phase residential PV applications, and the specification is presented in Table 6-1. In the MBI system, there are three different sets of power switches (i.e. S_{HF}, S_{LF} and S_{C}) for different usages. Their requirements, including voltage and current stress, are discussed based on the specification as follows.

- **Main HF Switches (S_{HF})**

According to the equivalent circuits, the voltage across S_{HF} is the sum of v_{DC} and v_{G}. Thus the required breakdown voltage of the devices for S_{HF} is determined, namely, around 700V for 345V DC voltage and 325V AC peak voltage with a 10% grid voltage variation. 1200V semiconductor devices are selected for S_{HF} with adequate margins.

Further, the current going through S_{HF} is the same as the inductor current when S_{HF} is on. Hence, the peak current (I_{max}) of S_{HF} is computed by the maximum inductor RMS current (I_{Lmax}) with respective ripple (Δi_{Lmax}) as expressed in the following equation. Based on the above i_{L} and Δi_{L} equations, the maximum current value is obtained for the conditions of 150V DC voltage with full power and the respective result is illustrated in Table 6-2.

$$I_{\mathrm{max}} = i_{\mathrm{Lmax}} + 0.5 \cdot \Delta i_{\mathrm{Lmax}}. \tag{6.5}$$

Table 6-1 Electrical specification of residential PV inverter.

Parameter	Value	Parameter	Value	Parameter	Value
v_{DC}	150-345V	Power	1200W	C_{A}	5.6μF
v_{G}	230V/50Hz	L_1/L_2	1.03mH	T_{j}	100℃
f_{sw}	20kHz	T_{a}	25℃	C_{CM}	100nF

- **Main LF Switches (S_{LF})**

The voltage across S_{LF} is related to both v_{DC} and v_G, the same requirement as S_{HF}. Therefore, the same 1200V voltage stress is required for S_{LF}.

Notice that, $i_L$is commuted between S_{HF} and S_{LF}, depending on the switching status. S_{LF} provides a current return path for i_G. Therefore, the maximum current going through S_{LF} is determined as the higher current between the calculated results of I_{max} and the peak of i_G. Typically the former is higher than the latter. Thus the current stress for S_{LF} is the same as S_{HF} The corresponding results are listed in Table 6-2.

- **Capacitive Switches (S_C)**

The voltage of S_C is typically considered as a rectified v_G with HF ripple Δv_C, which is 325V with a 10% grid voltage variation according to the specification in Table 6-1. Additionally, the current of S_C equals to i_G when S_{HF} is on, meanwhile it equals to the difference between i_L and i_G when S_{HF} is off. Thus, the current requirement is determined by the maximum current for both cases.

Based on the above analyses and the specification in Table 6-1, 1200V/40A rated devices are required for both S_{HF} and S_{LF} in this application, while 650V/30A rated devices are adequate for S_C with enough margins. Consequently, Si IGBTs and SiC MOSFETs are two available options for S_{HF} and S_{LF} to fulfill the high-voltage and power rating requirements. While Si-based IGBTs or MOSFETs are cost-effective options for the case of S_C where low voltage and conduction loss are more considered. The detailed requirements of different devices are summarized in Table 6-2. The specific device selection for this application needs to be determined based on the device comparison and power loss analyses.

Table 6-2 Electrical requirements of switching devices.

Switching Device		S_{HF}	S_{LF}	S_C
Voltage	Requirement	702V	702V	308V
	Selection	1200V	1200V	650V
Current	Requirement	26A	26A	18A
	Selection	40A	40A	30A

6.3. Power Semiconductor Comparison

In the following, a comparative device study, including static and dynamic characteristics comparisons of various devices, is conducted to determine the most suitable combination.

According to the previous device requirements, 1200V devices, including Si IGBTs and SiC MOSFETs from various manufacturers, are selected for S_{HF} and S_{LF}. Likewise, various 650V devices of Si IGBTs and MOSFETs are also selected for S_{C}. It is noted that the discontinued switching current of S_{LF} results in a reverse recovery loss of diode. To reduce this loss, a comparable SiC SBD is also chosen accordingly. Consequently, the available devices are illustrated in Table 6-3 based on two criteria: similar electrical rating and the MBI application's suitability with the specification. It is noted that SiC SBD serves as the anti-parallel diode of IGBT3 for this application, while other switches all use their body diodes as anti-parallel diodes. Moreover, Si IGBT7 is selected as a benchmark switch for later experimental verifications. Detailed device comparison is provided as follows.

Table 6-3 Devices specification for PV inverter.

Switch	Type	Part Number	Manufacturer
S_{HF} and S_{LF}	Si IGBT1	IKW25N120T2	Infineon
	Si IGBT2	STGW25S120DF3	ST
	Si IGBT3	IGW25T120	Infineon
	SiC SBD	IDWD20G120C5	Infineon
	SiC MOS1	SCT2080KEC	Rohm
	SiC MOS2	C2M0080120D	CREE
	SiC MOS3	IMW120R060M1H	Infineon
S_{C}	Si IGBT4	IKW30N65EL5	Infineon
	Si IGBT5	FGH40T65SPD	Fairchild
	Si IGBT6	STGW30M65DF2	ST
	Si MOS1	NVHL072N65S3	On Semiconductor
	Si MOS2	IPW65R045C7	Infineon
	Si MOS3	IXTH48N65X2	IXYS
Benchmark	Si IGBT7	FGA25N120ANTD	Fairchild

6.3.1 Static Characteristic Comparison

The objective of the static characteristic comparisons is to evaluate various devices' conduction performance, which is critical for system efficiency improvement. Since the designed operating junction temperature is 100℃, the static data of different devices shown in the following comparisons are extracted from the device datasheets and linearly converted to 100℃ condition for good results in this application.

- **Static Characteristics of 1200V Devices**

Figure 6-5(a) shows the output characteristics of 1200V Si IGBTs and SiC MOSFETs. It is observed that Si IGBTs generally provide a better on-state performance above 20A conduction current than SiC MOSFETs. Meanwhile, SiC MOSFETs have lower forward voltage drop typically, especially in a low current range. Furthermore, according to the forward characteristics of 1200V diodes in Figure 6-5(b), the body diodes of SiC MOSFETs have much higher conduction losses comparing with the counterparts of anti-parallel diodes in Si IGBTs. It is also found that SiC SBD provides a similar promising feature as the anti-parallel diodes of Si IGBTs. Since the conduction loss for the case of S_{LF} is the dominant loss, which consists of diode loss and conducting channel loss. Thus using Si-based IGBTs and anti-parallel diodes or SiC SBD is a superior option than using SiC MOSFETs with their body diodes. On the other hand, the switching losses of semiconductors become the key contributor to the total losses for the case of S_{HF}. Thus further dynamic characteristics analysis of these devices is required for the corresponding device selection.

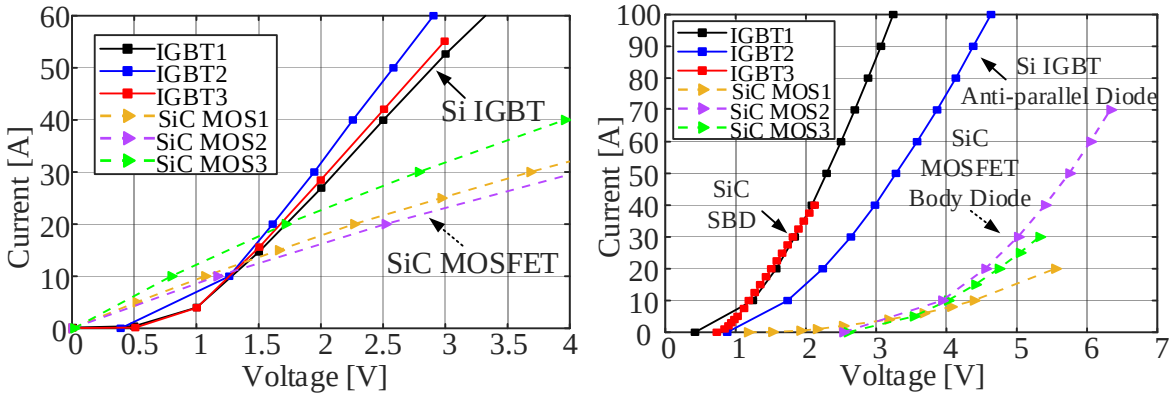
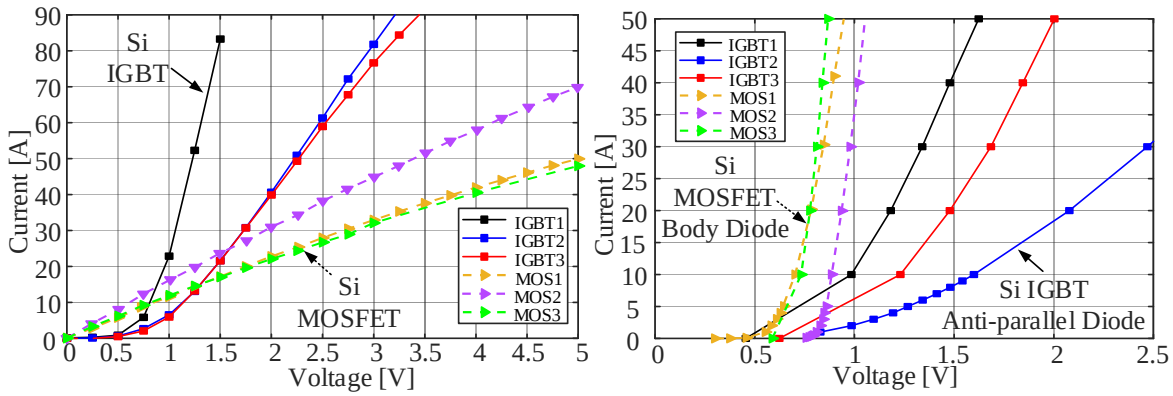


Figure 6-5 (a) Output characteristics of 1200V Si IGBTs and SiC MOSFETs, and (b) forward characteristics of 1200V diodes @100℃.



(a) (b)

Figure 6-6 (a) Output characteristics of 650V Si IGBTs and Si MOSFETs, and (b) forward characteristics of 650V diodes @100℃.

- **Static Characteristics of 650V Devices**

Figure 6-6 (a) shows the output characteristics of 650V devices, including Si IGBTs and Si MOSFETs. By comparing both Si-based devices at the same reference point, it is observed that Si MOSFETs generally can provide lower voltage drop, namely better conduction performance below 20A conduction current range which is the primary operating range for the case of S_C in this application. Likewise, Si MOSFETs' body diodes have much lower conduction losses than the anti-parallel diodes of Si IGBTs in a wide range of current. In fact, in the case of S_C, which is in the realization of two bi-directional Si MOSFETs, only the two MOS channels are conducting rather than the body diodes due to the constant positive gate drive voltage during conducting half-cycle. Hence, the corresponding conduction loss is further reduced compared to one conducting Si IGBT with a diode. Consequently, Si MOSFETs are more suitable than Si IGBTs for the case of S_C, which is opeating at LF switching and is conduction losses dominated.

6.3.2 Dynamic Characteristic Comparison

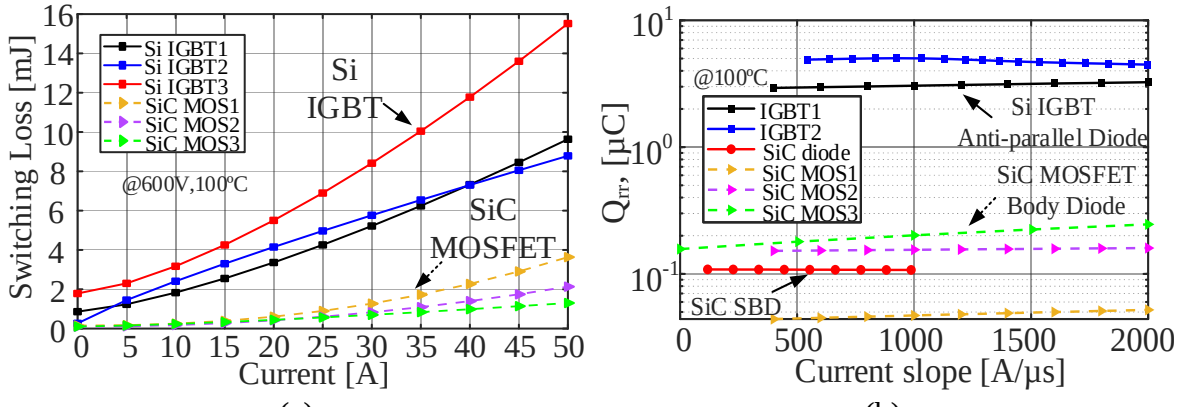
In practice, the dynamic characteristics of semiconductors are typically obtained by DPTs. However, it involves several peripheral equipment and laborious measurements. In this section, the switching loss and reverse recovery charge information are preliminarily obtained from the device datasheets' corresponding curves for simplicity. Notice that all the data are converted to the designed thermal condition 100℃ by linear interpolation. The detailed power loss analyses in this application are provided in section 6.5.

- **General Switching Losses Comparison**

Figure 6-7(a) shows the switching energy losses of different 1200V devices based on the corresponding device datasheets. It is observed that SiC MOSFETs have much lower switching losses compared to Si IGBTs because of the WBG material's superior features. For example, the switching losses of SiC MOSFETs are generally below one mJ at 20A conduction current. In contrast, the counterparts of Si IGBTs are four times higher (i.e., four mJ) at the same current condition. SiC MOSFETs also provide comparable conduction losses below 20A current, as shown in Figure 6-7 (a). Consequently, by comparing with both devices in terms of conduction and switching loss performances, SiC MOSFETs are advantageous for the case of S_{HF}, which operates at HF switching condition.

- **Reverse Recovery Charge Comparisons of Diodes**

It is necessary to take the reverse recovery losses of diode into account for the case of S_{LF} due to the HF discontinued operating current as mentioned previously. Figure 6-7(b) shows the Q_{rr} of 1200V diodes based on the corresponding curves from the device datasheets. It is found that SiC SBD offers a similar and negligible amount of Q_{rr} with the body diodes of SiC MOSFETs. In contrast, the Q_{rr} of the anti-parallel diodes in Si IGBTs are considerably higher than the other two devices, which lead to noticeable power losses for the case of S_{LF}. Consequently, SiC SBD or the body diode of SiC MOSFETs is more beneficial than using the anti-parallel diodes of IGBT directly in terms of reverse recovery losses. Nevertheless, to determine a suitable selection, a comprehensive power loss analysis for S_{LF} is necessary considering not only reverse recovery loss but also other conduction loss.



(a) (b)

Figure 6-7 1200V device curves of (a) Switching loss; and (b) Reverse recovery charge.

6.4. Inductor Design Analyses

In general, magnetic components such as transformers and inductors play a significant role in the PE system. Concretely, the power losses resulting from the two inductors in MBI are critical contributors to the total loss. It is well-known that the inductor losses, including core loss and copper loss, are determined by the operating conditions and the device parameters. These parameters are highly affected by the operating switching frequency. Therefore, it is also necessary to design the inductor based on the working conditions to achieve low power loss and improve system efficiency.

6.4.1 Copper Loss

The copper loss is calculated as the product of wire resistance and the square function of current. Concretely, this wire resistance is dependent on the length, thickness, and material of the wire. Typically, the resistivity of the conductor (ρ) is expressed by,

$$\rho = \rho_{20} \cdot [1 + \alpha_{20}(T_{\max} - 20)], \tag{6.6}$$

where ρ_{20} and α_{20} are the copper resistivity and temperature coefficient @20℃, respectively. $T_{\max}$ denotes the maximum operating temperature.

Also, the length of wire (l) is determined by the number of turns (N) and the mean turn length (MTL) for different cores such as Toroid and Amorphous Metal C-Core (AMCC) series,

$$l = N \cdot MTL = \begin{cases} 2N \cdot (l_{\mathrm{o}} - l_{\mathrm{i}}), \text{for Toroid core} \\ 2N \cdot (a + 2b + d), \text{for AMCC core'} \end{cases} \tag{6.7}$$

where l_{o} and l_{i} are the outer and inner perimeter of the toroid core, respectively. a, b and d are all the geometric parameters of the AMCC core, which is obtained from the datasheets.

Subsequently, the DC resistance (R_{DC}) is computed directly as,

$$R_{\mathrm{DC}} = \rho \cdot l / A_{\mathrm{cu}}\ , \tag{6.8}$$

where A_{cu} is the wire's cross-sectional area, respectively.

Apart from R_{DC}, the AC resistance (R_{AC}) of the wire should also be considered due to the skin effect, especially for HF switching applications. Typically, this skin effect is represented by the skin depth (δ), which is expressed as,

$$\delta = \sqrt{\rho / (\pi \cdot f_{\mathrm{sw}} \cdot \mu)}, \tag{6.9}$$

where μ is the permeability of the material ($\mu_0 = 4\pi \times 10^{-7}$ H/m is the permeability of air).

Thereby, R_{AC} is computed by,

$$R_{\mathrm{AC}} = \rho \cdot \frac{l}{\pi r^2 - \pi(r-\delta)^2}, \tag{6.10}$$

where r is the radius of the conductor and δ is highly dependent on the frequency. Consequently, the conduction power of the copper wire (p_{cu}) is determined as,

$$p_{\mathrm{cu}} = R_{\mathrm{DC}} \cdot I_{\mathrm{L}}^2 + R_{\mathrm{AC}} \cdot \Delta i_{\mathrm{L}}^2, \tag{6.11}$$

where I_{L} and i_{Lac} are the DC bias and AC ripple of the inductor current, respectively. It should be mentioned that for the case of using Litz wire, the skin effect is typically alleviated since the radium of a single wire is comparable to δ and thus R_{AC} is almost the same as R_{DC}.

6.4.2 Core Loss

Since no magnetic materials exhibit a perfectly efficient magnetic response, the inductor's core loss results from the material's changing magnetic flux field. Typically, the core loss density p_{ld} ($\mathrm{mW/cm^3}$) is calculated by the Steinmetz equation as a function of the AC flux swing B_{pk} (Tesla (T)) and f_{sw} (kHz), where a_{core}, b_{core} and c_{core} are the fitting coefficients obtained from measurements or provided from the datasheet [207].

$$p_{\mathrm{ld}} = a_{\mathrm{core}} \cdot B_{\mathrm{pk}}^{b_{\mathrm{core}}} \cdot f_{\mathrm{sw}}^{c_{\mathrm{core}}}. \tag{6.12}$$

It is known that B_{pk} is half of the AC flux ripple (ΔB), which is highly dependent on the AC magnetizing field ripple (ΔH). ΔH is a function of winding number N, current, and magnetic path length (l_{e}), which is expressed as,

$$\Delta H = N \cdot \Delta I_{\mathrm{L}} / l_{\mathrm{e}}. \tag{6.13}$$

Subsequently, B_{pk} is further determined for each switching cycle as

$$B_{\mathrm{pk}} = \mu_0 \cdot \Delta H / 2. \tag{6.14}$$

Consequently, the core loss power (p_{core}) is computed by p_{ld} with either core volume (V_{L}) or weight (m_{L}) based on the specification.

$$p_{\mathrm{core}} = p_{\mathrm{ld}} \cdot V_{\mathrm{L}}(m_{\mathrm{L}}). \tag{6.15}$$

6.4.3 Design Procedure

The key assembling components of an inductor are core and wire. A practical design procedure of an inductor is shown in Figure 6-8, which includes core material selection, wire selection and power loss calculation.

- **Core Selection**

Typically, the power inductor gap is realized in two fashions, discrete or distributed (powder core). In this application, toroid high flux magnetic powder core [208] and Metglas AMCC C-core [209] are considered. Both of them can provide high saturation flux density and have superior performance in high-power HF applications. To select an inductor core, two parameters of the design application, including inductance (L) and the dc current (I) are required to be determined based on the requirements. After that, the core size, the number of turns N, airgap length is determined.

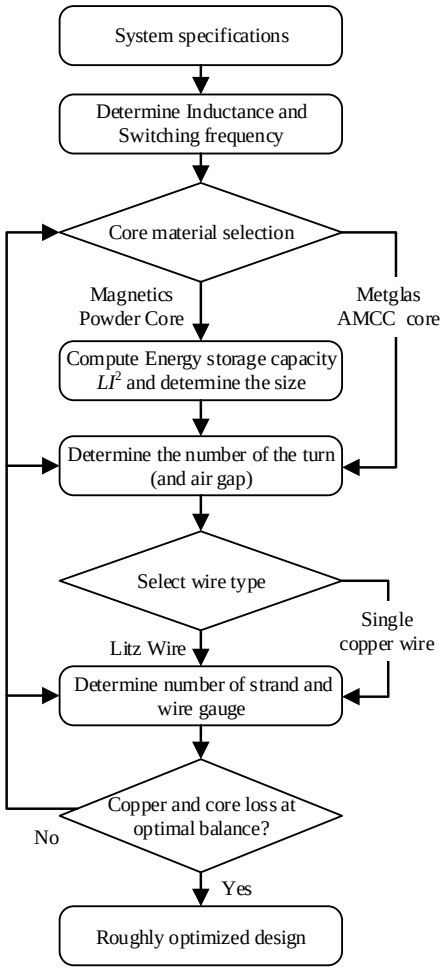


Figure 6-8 Flow chart of inductor design.

For high flux Magnetics powder core, the core size is determined by computing the required energy storage capacity (i.e. $L \cdot I^2$) and locating the appropriate size from the recommended core selector chart in the datasheet [208]. As for the AMCC core, it is more based on the required L and core dimensions to meet the winding requirements.

For the case of toroid core, the minimum inductance factor (A_{L}) is used to calculate N for the worst-case negative tolerance (generally -8%), and thus N is further determined,

$$N = \sqrt{L \cdot 10^3 / A_{\mathrm{L}}}. \tag{6.16}$$

As for the case of AMCC core, there are two degrees of freedom to fulfill the requirement, N and the air gap length (l_{g}). Initially, the maximum turns (N_{max}) is determined as,

$$N_{\mathrm{max}} = A_{\mathrm{w}} \cdot k_{\mathrm{cu}} / A_{\mathrm{cu}}, \tag{6.17}$$

where A_{w} stands for the area of window area and k_{cu} is the copper filling factor, which typically equals 0.4.

Further, the minimum number of turns (N_{min}) is obtained by,

$$N_{\mathrm{min}} = L \cdot (I_{\mathrm{L}} + 0.5 \cdot \Delta I_{\mathrm{L}}) / (B_{\mathrm{max}} \cdot A_{\mathrm{e}}), \tag{6.18}$$

where I_{L} and ΔI_{L} are the DC bias inductor current and current ripple, respectively. B_{max} and A_{e} denote the maximum flux density and the cross-sectional area of the core.

Accordingly, l_{g} is computed based on the specific N and L as

$$l_{\mathrm{g}} = \mu_0 \cdot A_{\mathrm{e}} \cdot N^2 / (2 \cdot L). \tag{6.19}$$

- **Wire Selection**

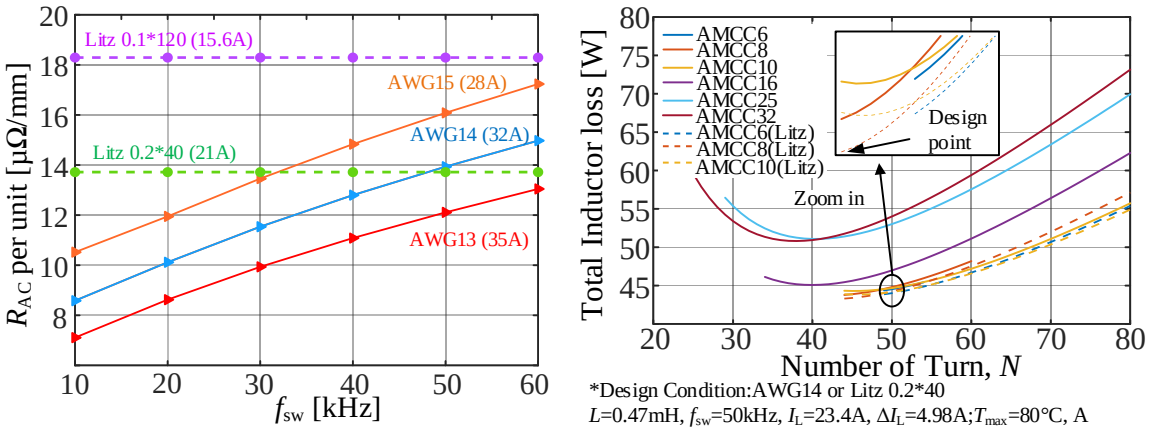
Single standard solid-round copper wire is selected from the American Wire Gauge (AWG) table based on the required current rating. The ac resistance of various wires for different frequencies is further calculated considering the skin effect.

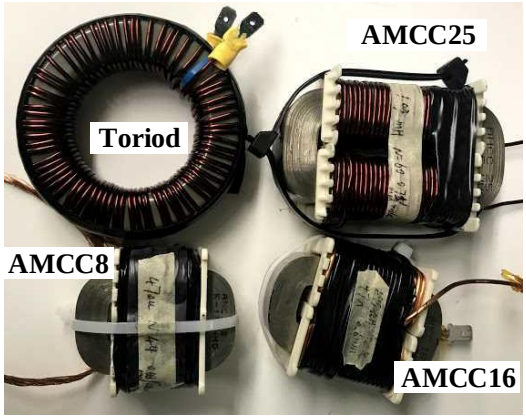
Figure 6-9 (a) illustrates the ac resistance results for various single copper wires and the Litz wire solution. It is observed that generally, the single copper wire with a higher current rating can result in lower ac resistance due to the larger A_{cu}. As f_{sw} rises from 10 to 50kHz, R_{AC} of single copper wires increases significantly because of the skin effect. Besides, the merit of using Litz wire with a similar current rating becomes promising when f_{sw} is higher than 40kHz. Hence, the wire should be selected reasonably based on the operating specification.

- **Design Finalization**

Based on the above analyses, an inductor design tool has been implemented in MATLAB to evaluate the loss performance of various design options and finalize the optimal design for the specific operating conditions with the lowest total inductor losses.

For instance, the inductor design results using AMCC core under 50kHz switching frequency are provided in Figure 6-9 (b). It is observed that AMCC8 with a Litz wire design can achieve the lowest total inductor losses. Likewise, different inductors with the same current ripple requirement are custom-made using appropriate core and wire selection according to the operating conditions. Consequently, the designed inductors for the MBI application are shown in Figure 6-9 (c), and the key parameters are listed in Table 6-4. On the one hand, as f_{sw} increases, the size of the inductor is typically reduced due to the lower inductance requirement. On the other hand, an increase in copper loss is also resulted due to the skin effect. Therefore, a proper design is necessary to balance this trade-off and achieve the lowest loss.





(c)

Figure 6-9 (a) wire resistance results; (b) HF AMCC core design; (c) designed inductors.

Table 6-4 Key parameters of inductors

Inductance	1.03mH	0.695mH	0.57mH	0.47mH
Core Type	High flux 58907	AMCC16A	AMCC10	AMCC8
Number of Turns	77	47	56	44
Air Gap Length	distributed	0.6mm	0.88mm	0.68mm
Wire Type	AWG14	AWG14	0.2×40 Litz	0.2×40 Litz
Mass	720g	248g	198g	172g
Frequency	20kHz	30kHz	40kHz	50kHz

6.5. Power Loss Analyses

In this section, the preliminary device selection is further improved to determine the specific devices with the lowest power loss based on the simulation results in PSCAD/EMTDC. A comprehensive power loss analysis at the system level, including semiconductor losses and passive inductor losses, is also conducted for the MBI application.

6.5.1 Semiconductor Loss Analysis

- **Conduction Loss**

According to the equivalent circuits in Figure 6-3, when S_{HF} is conducting, most of the i_{L} flow through S_{HF} and no conduction current occurs in the half-off cycle. Hence, the resulting conduction loss P_{CHF} during one switching period (T_{C}) is calculated by,

$$P_{\mathrm{CHF}} = f_{\mathrm{sw}} \cdot \int_0^{T_{\mathrm{c}}} D \cdot v_{\mathrm{HF}} \cdot i_{\mathrm{L}} \, \mathrm{d}t, \tag{6.20}$$

where v_{HF} denotes the forward voltage of S_{HF} which equals to v_{cesat} of IGBT or the product of i_{L} and $R_{\mathrm{ds(on)}}$ of SiC MOSFET.

Notice that, during each switching cycle, one diode conducts i_{L} when S_{HF} is off, and one conductive channel of S_{LF} provides the return path of i_{G}. Thus, the resulting conduction losses of S_{LF} (P_{CLF}) is determined by,

$$P_{\mathrm{CLF}} = f_{\mathrm{sw}} \cdot \int_0^{T_{\mathrm{c}}} [v_{\mathrm{LF}} \cdot |i_{\mathrm{G}}| + (1 - D) \cdot v_{\mathrm{LFD}} \cdot i_{\mathrm{L}}] \, \mathrm{d}t, \tag{6.21}$$

where v_{LF} and v_{LFD} stand for the voltage drop of the channel and diode for S_{LF}, respectively.

Besides, the diode reverse recovery loss for S_{LF} is also considered, which is computed approximately by the product of Q_{rr} and voltage drop during each switching cycle.

Based on the previous analyses, the current of the switch S_{C} (i_{C}) is swinging based on the switching state of S_{HF}. Accordingly, the conduction loss (P_{CS}) is expressed as,

$$P_{\mathrm{CS}} = f_{\mathrm{sw}} \cdot \int_0^{T_{\mathrm{c}}} v_{\mathrm{CS}} \cdot [|i_{\mathrm{G}}| \cdot D + |i_{\mathrm{L}} - i_{\mathrm{G}}| \cdot (1 - D)]\, \mathrm{d}t, \tag{6.22}$$

where the total voltage drop of S_{C} (v_{CS}) consists of either two voltage drop across MOSFETs or one diode voltage drop along with one v_{cesat} of IGBT based on the realization of S_{C}.

- **Switching Losses**

Since only S_{HF} operates at HF switching, and the others run at LF, namely 50Hz. thus only the switching losses of S_{HF} are taken into account. The counterparts of the other switches are insignificant compared with the conduction losses. In the simulation, the switching losses of S_{HF} are obtained from the power loss LUTs generated by the previous approaches.

- **Simulated Loss Results**

The targeted MBI application was simulated in PSCAD/EMTDC using different device combinations. The simulated results of power losses under the full power (1.2kW) condition with 200V DC input voltage are shown in Figure 6-10.

It is found from Figure 6-10(a) that SiC MOSFETs generally provide much lower total losses due to superior switching performance. In particular, minimum power losses are achieved by using SiC MOS3 for the case of S_{HF}. As for the case of S_{LF}, the total losses of Si IGBTs are comparable with SiC MOSFETs, and diode losses are more critical than channel losses, as shown in Figure 6-10 (b). It is also noted that the use of SiC diode significantly reduces the diode losses, which helps the combination of Si IGBT3 and SiC diode standing out from the rest with the lowest total losses. Furthermore, it is found in Figure 6-10 (c) that Si MOSFETs generally produce lower losses than IGBTs because of the merit of the bi-directional conduction channel for S_{C}. And the best performance is given by Si MOS2 resulting lowest amount of losses. Consequently, the optimal device combination is determined, namely, using SiC MOS3 for S_{HF}, Si IGBT3 along with SiC diode for S_{LF} and Si MOS2 for S_{C}. Further experimental verification for this combination is provided in Section 6.6.

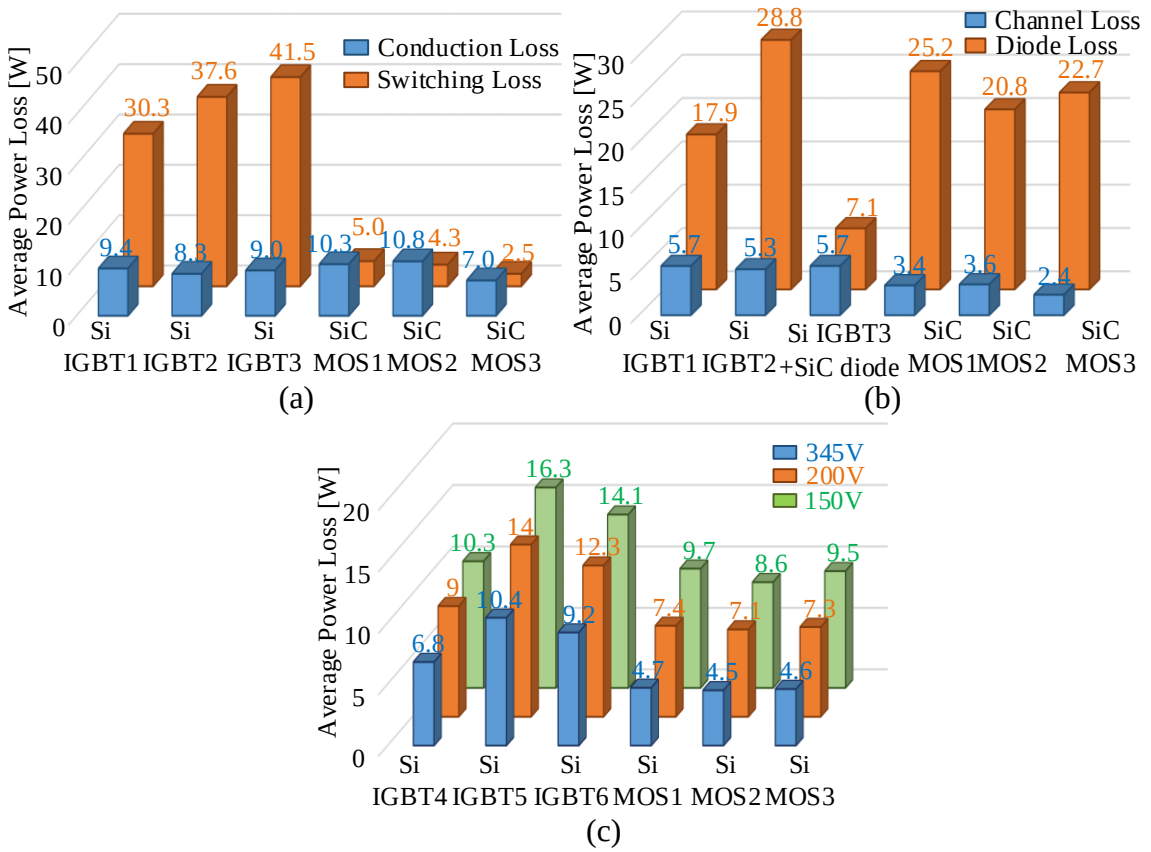


Figure 6-10 Simulated power losses of different devices under the full power condition for the case of (a) S_{HF} at 200V DC input, (b) S_{LF} at 200V DC input, and (c) S_{C}.

6.5.2 Inductor Loss Analysis

Notice that, apart from the switches' power losses, there are still enormous losses resulting from other passive components in this application. Therefore, a concrete inductor loss analysis for this application is conducted in this section based on the simulated results. Notice that these inductors are designed explicitly with the same current ripple as mentioned previously and further optimized by selecting the proper parameters (e.g. l_{g}, N and wire type) to achieve the lowest inductor losses under the corresponding switching frequency.

The simulated inductor loss results for the MBI application are given in Figure 6-13 under various operating conditions. It is observed that the AMCC25 inductor generally provides lower total loss (p_{total}) above 600W range though its p_{core} is higher, comparing with the toroid inductor design for the case of 20kHz. Further, as v_{DC} increases from 150V to 345V, p_{total} for all the inductors decline accordingly due to the reduction of conduction current and thus copper losses. Besides, the inductor for 30kHz can achieve the lowest p_{total} among all the designs.

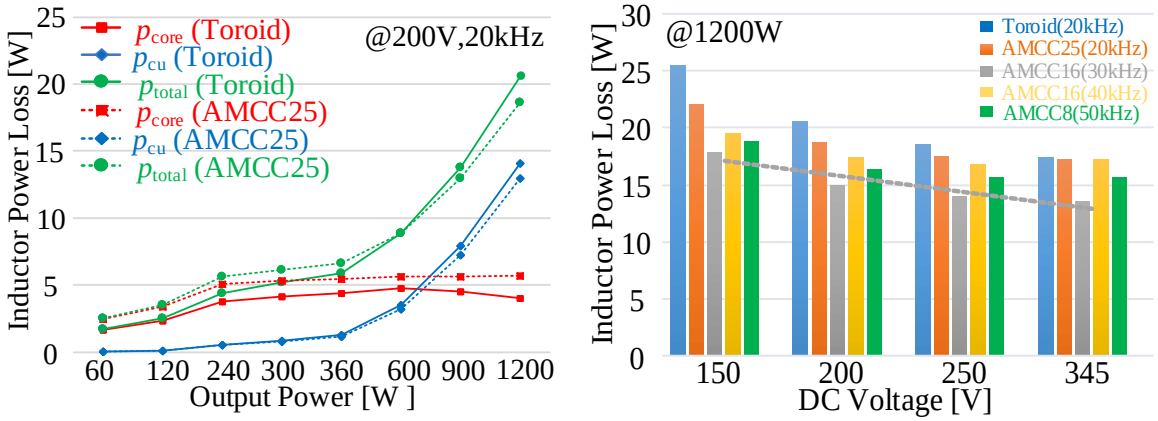


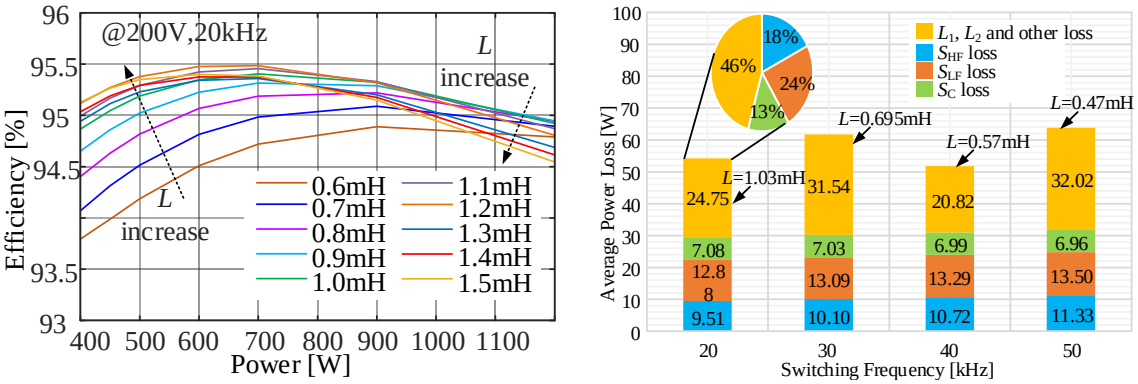
Figure 6-11 Simulated inductor power loss of MBI (a) vs output power; and (b) vs v_{DC}.

6.5.3 Total System Loss Analysis

A comprehensive power loss simulation is conducted using the mixed device combination with various inductor designs, as mentioned previously. Figure 6-12(a) shows the simulated efficiency results under 20kHz, 200V. As inductance increases, the efficiency increases initially and then declines in the high power range. Larger inductance can limit the current ripple, resulting in reduced core loss, which is the dominant loss in the low power range. Higher copper loss in the high power range results from the increase of N for larger inductances. Hence, the proposed method is promising for inductor selection to achieve desirable performance.

Further, the simulated power loss breakdown results are illustrated in Figure 6-12(b). It is observed that the inductor losses are almost half of the total losses for the case of 20kHz. Additionally, the losses of S_{LF} are slightly higher than the losses of S_{HF}. The loss of S_C is the lowest (less than 15%). Furthermore, as f_{sw} increases to 50kHz, the losses of S_{HF} and S_{LF} both increase accordingly, while the loss of S_C shows almost irrelevant to f_{sw}. Also notice that the inductor losses change irregularly with f_{sw}. That is because, for various f_{sw}, although ΔI_L is designed with a similar value, the wire resistances are changing as N and wire type change. Moreover, the core loss is related to not only f_{sw} but also the inductors size.

Based on the above simulation loss analysis, the overall power loss behaviors for both switches and inductors in this application are predicted in a wide range of operating conditions. It is helpful for PE engineers to select devices as well as operating conditions.



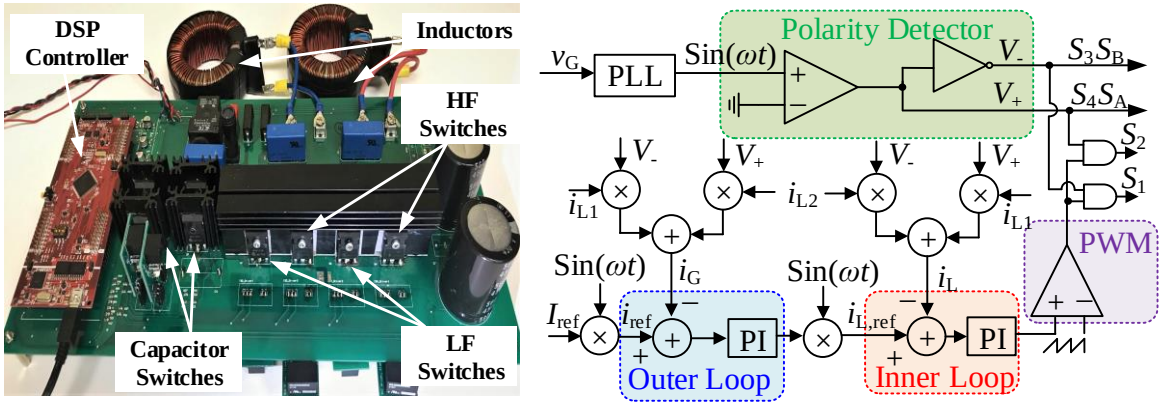
(a) (b)

Figure 6-12 Simulated (a) efficiency curve; (b) power loss breakdown at 200V, 1200W.

6.6. Experimental Verification

6.6.1 Prototype Description

To further verify the proposed approach in efficiency evaluation and system optimization for residential PV applications, a 1.2-kW hardware platform has been built based on the circuit in Figure 6-2 and the specification in Table 6-1. The prototype in Figure 6-13(a) includes the main power board, gate driving circuits, semiconductor switches, inductors and other passive components. The control strategy is illustrated in Figure 6-13(b) and implemented in the DSP. There are two PI control loops in the system, namely the outer and inner loops. i_G is regulated to synchronize with v_G by the outer loop, while i_L is controlled by the inner loop for power balance. In addition, the inner loop operates under five times higher frequency than the outer loop for high accuracy and fast response. Besides, the operating temperature is monitored by Fluke TiS-40 infrared camera. Four device combinations, including Si-based and SiC-based devices, are tested under a wide range of operating regions, as illustrated in Table 6-5.



(a) (b)

Figure 6-13 Manitoba inverter (a) prototype, and (b) control block diagram.

Table 6-5 Key semiconductor switches under test

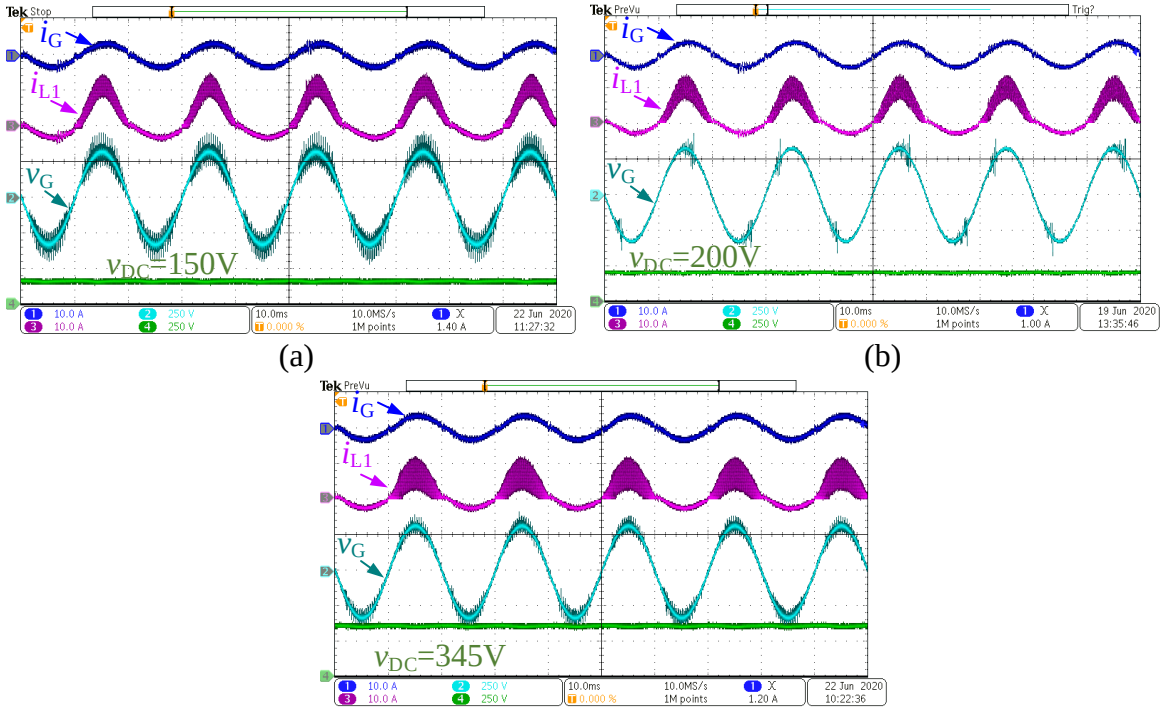
Comb. #	Switch Type	S_C	S_{LF}	S_{HF}
Comb.1	All Si IGBTs	Si IGBT7	Si IGBT1	Si IGBT7
Comb.2	Si IGBTs+SiC MOS	Si IGBT7	Si IGBT1	SiC MOS3
Comb.3	Si MOS+Si IGBT+SiC MOS	Si MOS2	Si IGBT1	SiC MOS3
Proposed Comb.4	Si MOS+(Si IGBT+SiC diode)+SiC MOS	Si MOS2	Si IGBT3+ SiC diode	SiC MOS3

6.6.2 Steady State waveforms

Figure 6-14 (a)-(c) show the experimental results of the MBI prototype operating at 600W power level with different input v_{DC} from 150V to 345V. It is observed that the prototype can operate accordingly in boost mode for lower v_{DC} and buck mode for higher v_{DC}. In addition, i_G is kept as sinusoidal current with a slight current ripple, and it is also synchronized with v_G resulting in up to 0.98 power factor. It is also noticed that i_L is an asymmetrical waveform due to the changing roles between the buck-boost inductor and the grid CL filter every half-line cycle. In the positive half cycle, S_{HF} (S_1) operates at HF switching along with L_1 to form buck-boost converter, which results in HF inductor current ripple. While in the negative cycle, S_{HF} keeps in off-state and i_L is identical to i_G.

Figure 6-15(a) illustrates the voltage stress of different switching devices in this application. It is observed that, during the positive cycle, both S_{HF} and S_{LF} suffer from the sum of v_{DC} and v_G (typically less than 700V), consistent with the theoretical analysis, while only v_G with the peak 325V is applied across S_C. Hence, 1200V devices for the case of S_{HF} and S_{LF} and 650V devices for S_C are reasonable with enough margins. In fact, 900V devices are also adequate for S_{HF} and S_{LF}, though there is no significant merit in terms of cost and performance.1200V devices, in turn, have more available selections in the market.

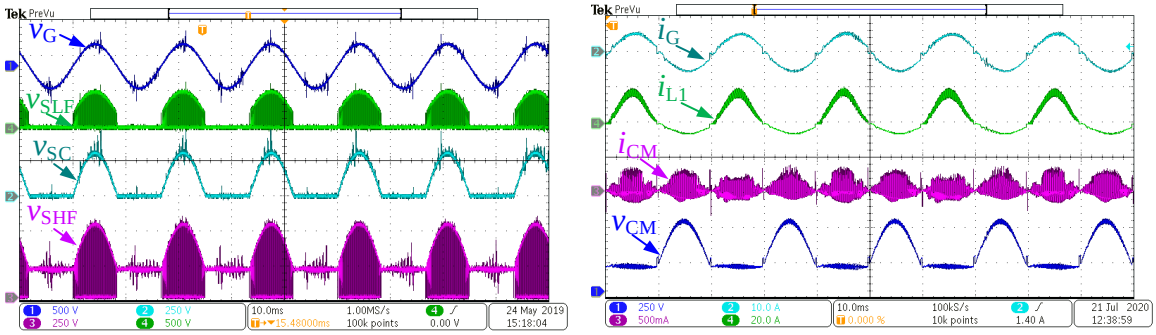
Besides, the leakage current measurement of this application is given in Figure 6-15(b). A 100 nF capacitor is added between the input DC link and output AC grid to emulate the parasitic capacitor C_{CM}. Notice that the leakage current i_{CM} is generally limited within 300mA, and the voltage v_{CM} across C_{CM} is nearly sinusoidal with a negligible ripple. Consequently, both low leakage current and CM voltage are achieved by this MBI topology.



(a) (b)

(c)

Figure 6-14 Steady-state waveforms at 600W power, v_{DC} (a) 150V, (b) 200V, and (c) 345V.



(a) (b)

Figure 6-15 (a) Voltage stress of various devices; (b) Measurements of i_{CM} and v_{CM}.

6.6.3 Efficiency Evaluation

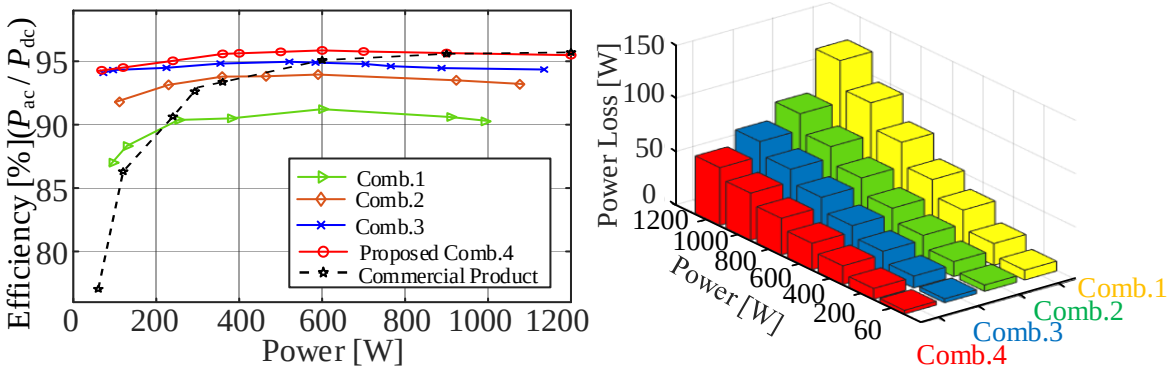
A series of efficiency tests with varying conditions are conducted to verify the proposed combination's efficiency improvement. The YOKOGAWA-WT1800 power analyzer was used to measure the system's efficiency. Notice that only the converter stage is considered in the measurement, and the auxiliary power is excluded.

The system efficiency results using various combinations are provided in Figure 6-16(a). Notice that the efficiency curves of the commercial product (two-stage PV inverter) from ABB [210] are also included. It is observed that a noticeable efficiency improvement in a wide range

of operating regions is achieved by replacing Si-based devices with SiC-based devices. Concretely, the overall efficiency by using Comb.4 is 4% higher than Comb.1, and the peak efficiency is up to 95.86%. Comparing with the commercial product, Comb.4 provides comparable efficiency results in the high power region. However, a significant efficiency enhancement is achieved in the low power region, the PV inverter's primary operating region. For example, the efficiency below 100W boosts from 77.04% to 94.23%.

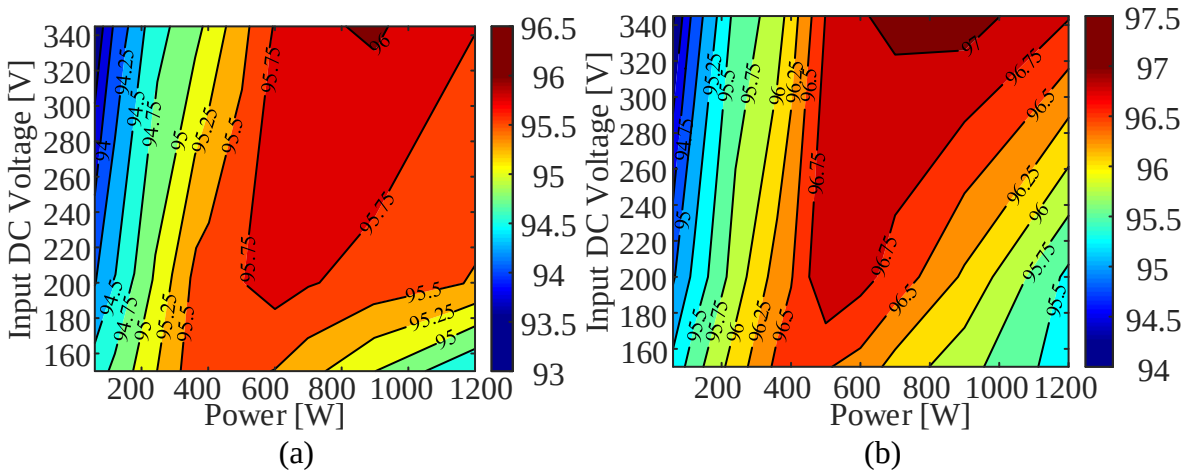
Further, the total power loss results are illustrated in Figure 6-16 (b). It is observed that a considerable loss reduction is achieved by using Comb.4 comparing with the other combinations. For instance, the total loss of using Comb. 4 is approximately half of the loss using Comb.1 in full power condition. Thus, the benefits of various devices are well utilized.

Figure 6-17 (a) shows the measured efficiency chart in a whole range of v_{DC} and output power. The maximum measured efficiency can go up to 96%, and the efficiency declines slightly as the power decreases and v_{DC} increases. In addition, better performance is achieved when MBI operates at medium and high power range. With the MBI topology and SiC-based devices' help, the prototype can generally provide more than 94% efficiency in most operating regions. Further, the simulated efficiency chart is also provided in Figure 6-17 (b). It is found that the simulated and measured efficiency results share a similar manner in terms of efficiency change trend and distribution. However, the simulated results are generally higher than the measured results. The deviations may result from various impacts such as measurement errors, parasitics in the circuit and capacitance losses. Nevertheless, the average error is generally acceptable, and the proposed method can have a good reproducibility of the power loss and efficiency behaviors in MBI applications.



(a) (b)

Figure 6-16 Measurements of (a) efficiency and (b) loss of different comb. at 200V v_{DC}.



(a) (b)

Figure 6-17 Efficiency chart of MBI using a mixed combination (a) measured; (b) simulated.

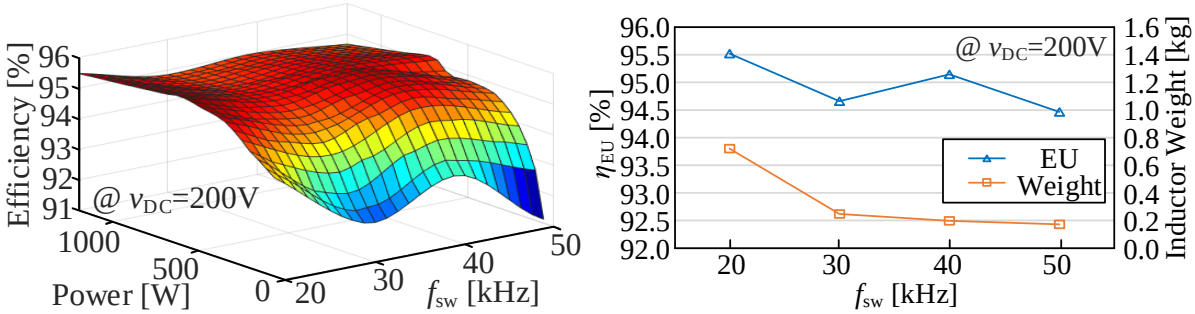
6.6.4 Discussion

Generally, high efficiency and power density are achieved with a high switching frequency. A discussion on the impacts of various factors on efficiency performance is provided in this section based on a series of efficiency tests under different conditions.

Figure 6-18(a) shows the 3-D efficiency results of the prototype using the mixed combination. It is observed that the prototype can provide more than 94% efficiency in most operating regions. Note that the designed inductance in this application is reduced from 1.03mH (20 kHz) to 0.47mH (50 kHz) to maintain the same ΔI_{L}. This leads to a significant inductor weight reduction from 0.72 kg to 0.172 kg, as shown in Figure 6-18(b). As f_{sw} changes from 20 kHz to 30 kHz, the European (EU) efficiency declines more than 0.5% due to the increased switching loss and core losses. Nevertheless, the efficiency becomes more than 95% again for 40 kHz. That is because of the reduction of the size of the inductor and the benefit of using Litz wire. However, for 50 kHz, these merits become less dominant than the increasing switching frequency and thus, the EU efficiency decline slightly.

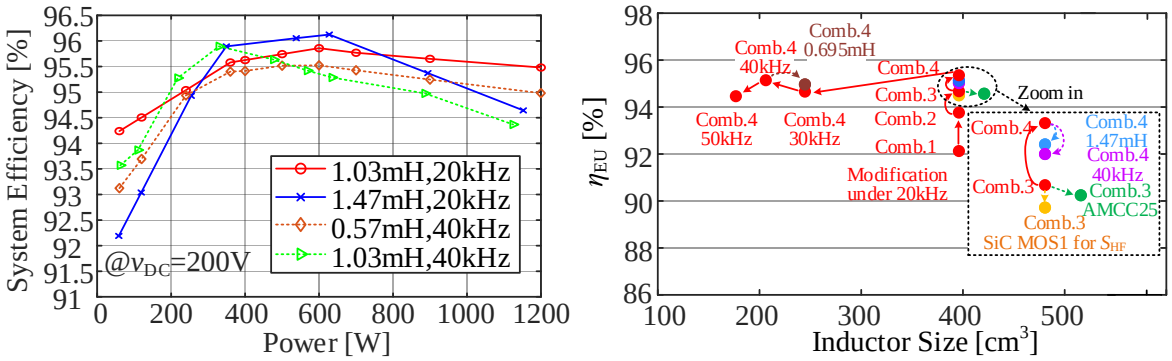
Furthermore, it is also observed from Figure 6-19(a) that, if the identical inductors (1.03mH) are used for both cases of 20 kHz and 40 kHz or using a large inductor (1.47mH) for the case of 20kHz, higher peak efficiency is achieved because of the reduced current ripple. However, the efficiency declines significantly in the high and low power range. Moreover, the overall efficiency optimization chart is illustrated in Figure 6-19(b). It is found that the EU efficiency of the prototype is initially improved by changing the device combination from Comb.1 to Comb.4 and further enhanced by optimizing the f_{sw} and reducing the inductor size

accordingly. Eventually, the operating condition of 40 kHz switching frequency with 0.57mH inductors is an optimal option for this application, which offers a good trade-off between efficiency and power density in a wide range of operating regions. It is also found that modifications by changing one parameter (e.g. inductor or f_{sw}) at a time based on trial and error method can result in a negative impact on the efficiency.



(a) (b)

Figure 6-18 MBI prototype (a) 3-D efficiency results; (b) η_{EU} and inductor mass results.



(a) (b)

Figure 6-19 Efficiency results (a) various conditions; (b) overall optimization.

6.7. Chapter Conclusion

This chapter presented a case study applying the previous simulation-based approaches from Chapter 3 to Chapter 5 in a PV inverter application for efficiency evaluation and system optimization. Based on a detailed device comparison and the power loss analyses, a mixed device combination including Si and SiC-based devices was determined to fulfill the device requirements and achieve the lowest power losses. It was found that SiC MOSFETs were advantageous in high-frequency switching conditions, while Si IGBTs along with SiC SBDs were a cost-effective selection for line-frequency switches. Besides, Si MOSFETs provided superior conduction performance when they acted as the bi-directional conducting channels at the low current condition. Further, the inductor designer procedure and loss analyses were conducted, and various inductors were designed according to the operating conditions.

Moreover, comprehensive power losses and efficiency analyses in PSCAD/EMTDC were conducted and experimentally verified by a 1.2kW PV inverter prototype. It was found that, by using the mixed combination in this application, the prototype could operate under a wide range of input voltage with high system efficiency. Over 4% of overall efficiency improvement was achieved comparing with all Si-based solutions. Besides selecting the appropriate switching frequency for this application and designing inductors accordingly, a good trade-off between efficiency and power density was further achieved.

Consequently, the proposed simulation-based approaches can reproduce the loss behaviors of switching devices and magnetic components in PE systems. It helps PE engineers enhance efficiency and optimize the system by selecting appropriate devices and operating conditions in the PE system design stage.

Chapter 7 Conclusion and Future Work

7.1. Conclusion

A simulation-based modelling methodology of modern power semiconductor devices was proposed and investigated in this thesis. This approach could reproduce various devices' static and dynamic behaviors in simulation, generate a multi-dimensional power loss table, and evaluate a power electronics system's efficiency. This thesis has been broken down into seven chapters to comprehensively analyze various research aspects from a theoretical background, device model development, power loss analyses, system implementations, and experimental verifications. It filled the gap between electrical and thermal simulation, generalized the transient behavioral models for different semiconductors, and provided a promising solution for PE system evaluation with a balanced trade-off among accuracy, complexity, and speed. The state of art semiconductor modelling techniques was reviewed. Besides, the advantages and disadvantages of different device models and power loss estimation methods were identified and discussed from various perspectives in Chapter 2.

Based on the literature review, a multi-level simulation strategy for loss prediction in a PE system using an IGBT-diode cell has been proposed and studied comprehensively in Chapter 3. In the device-level simulation, a transient behavioral model of IGBT has been developed considering the impacts of parasitics, tail current, and the reverse recovery behavior of diode. As a result, the transient switching waveforms of IGBT in the double-pulse test circuit were simulated under a wide range of operating conditions with a nanosecond time-step. A multi-dimensional power loss table was further generated. In the system-level simulation, the PE system was implemented with simple switch models under a microsecond time-step. Thus, the instantaneous power loss was obtained by the power loss look-up table based on the input operating conditions. Hence, the accuracy could be promised by the device-level simulation. Meanwhile, the simulation speed was still maintained in the system-level simulation.

Furthermore, in Chapter 4, a dynamic thermal model has been added to the previous system-level simulation to form a closed-loop electro-thermal simulation for power loss and junction temperature estimations. Besides, the IGBT-diode model was further extended to SiC

MOSFET and SBD, taking the charging and discharging process of the junction capacitances and the thermal-dependent features into account. The DPT bench experimentally verified the proposed method for switching transients and loss estimations of SiC MOSFETs under various operating conditions. Moreover, both the electrical and thermal performances of the PFC application were evaluated and validated by comparing with simulated and measured results.

Furthermore, a generalized behavioral model for a switch-diode cell was proposed in Chapter 5, considering the dynamic characteristics and the third quadrant operation of eGaN HEMT apart from Si- and SiC-based devices' counterparts. The switching process and power loss analyses for different semiconductor devices and operational scenarios have been discussed. Besides, the model parameter extraction procedures from the device datasheet were also demonstrated. Three specifically designed DPT circuits were built to fulfill the respective gate drive and test requirements for different devices. Consequently, both the switching transients and power loss estimations were obtained by the proposed method and experimentally verified by the DPT circuit in a wide range of operation regions.

The proposed electro-thermal simulation method was eventually applied to a single-phase grid-tied PV inverter as a case study for efficiency evaluation and system optimization in Chapter 6. Three sets of switching devices with different device requirements were identified, and a preliminary device selection for all the switches was made accordingly. Further, a device characteristics comparison and power loss analyses in this application were conducted by simulation. Subsequently, a Si-SiC-mixed device combination was determined with the lowest total loss. Besides, the magnetic inductors were also specifically designed and optimized based on system requirements and the switching frequency. Consequently, this PV inverter's efficiency was obtained based on the computed inductor losses, simulated semiconductor losses, and validated by the hardware prototype.

In contrast to prior related work in this area, this thesis provided a comprehensive simulation-based modelling approach of modern semiconductors to simulate the devices' behaviors and evaluate a PE system's efficiency, considering electrical and thermal performances. All the simulations were implemented in a single simulator PSCAD/EMTDC, without convergence issues. All parameters were attainable in the device datasheet without

extra hardware measurements. The model could apply to various semiconductor devices and achieve fast simulation speed with acceptable accuracy.

7.2. Contributions

The critical contributions of the research work presented in this thesis are listed below. Thus, it is concluded that these thesis objectives have been achieved.

(1) This thesis provided a solid reference for researchers working on the power semiconductor modelling area and further provided a guideline for device selection, PE system design and optimization.

(2) A comprehensive study on the static and dynamic characteristics of Si IGBT, SiC MOSFET, and eGaN HEMT devices, considering the impacts of parasitic elements, diode, and temperature, have been presented, which helps understand the dynamic behaviors of devices.

(3) A detailed switching process and power loss analysis for different semiconductor devices in the DPT circuit have been discussed. The modelling and parameter extraction procedures were illustrated. The model was implemented in PSCAD/EMTDC to reproduce switching waveforms and generate power loss LUT in various operating conditions. This intensive work provided significant insights into semiconductor modelling study.

(4) A multi-level electro-thermal simulation method was proposed to evaluate a PE system using modern semiconductor devices, which could achieve a balanced trade-off among accuracy, complexity, applicability, and simulation speed. To the best of the author's knowledge, such model development and verification approach has not been reported in the existing literature.

(5) Several DPT benches and respective gate drive boards have been designed and built for switching transient and power loss verifications of different semiconductor devices. Such an experimental validation method was one of the contributions and could reference new device characterizations and power loss LUT extractions.

(6) A case study applying the proposed method to estimate the power losses and evaluate the efficiency in a single-phase single-stage grid-tied PV inverter has been presented. A mixed device combination and specifically designed inductors were determined based on device comparisons and power loss analyses with the lowest total loss objective. Also, the proposed

approach was experimentally verified by a PV inverter prototype with a considerable efficiency improvement. The use of the electro-thermal simulation method in this application was the first such reported PE application. The PE system design, verification, and optimization procedures were significantly helpful for PE engineers.

7.3. Future Work

With the development of power semiconductors, new devices with specific features will be used in PE applications. Meanwhile, PE systems are also rapidly developed with more advanced topologies and control strategies. Hence, it is foreseen that the simulation-based modelling method of semiconductors for the efficiency evaluation of the PE system presented in this thesis can gain more popularity and give a noticeable contribution. The current research work is further improved with the following possible extensions, catering to the demands.

(1) The diode model is improved by considering the voltage-dependent junction capacitance. Also, the reverse recovery behavior and loss of diode were mainly based on the empirical model. The dynamic behaviors, especially during the reverse recovery decay period, is further improved by accurately extracting the decay time constants. Besides, the diode parameters such as I_{rm}, Q_{rr} and t_{rr} are temperature-dependent. These impacts are not fully considered in the current work and can also be improved.

(2) The parameter extraction procedures for parasitic capacitances and inductances are more accurate using advanced fitting methods or other numerical methods. Some parasitic inductances and resistances in the gate loop or power loop are included, such as gate inductance, device lead inductance and trace resistance.

(3) The current and voltage ringings during switching transient are not considered in the proposed model for simplicity. However, these ringings can result in additional power loss and impact the devices' switching performance in some cases. Hence, further research can be conducted to develop the RLC resonance model and study the influences accordingly.

(4) The switching transient modelling is enhanced by taking more new device insights into account. For example, during turn-on and turn-off periods, the miller plateau is assumed to have constant miller capacitance. Some studies implied that a non-flat miller plateau [86] was found in some WBG devices, affecting the devices' switching behaviors. The crosstalk

issue [5] sometimes could not be neglected due to the parasitic capacitances. Hence, the proposed model is modified accordingly to reflect these impacts.

(5) In the presented work, a second order Foster/Cauer thermal network was used, extended to higher-order for higher accuracy. The heatsink counterpart also can consider the case of multi-chips condition with airflow.

(6) More new devices with novel configurations such as GaN HEMT with cascaded Si MOSFET [69] can be studied and included in the generalized semiconductor model to extend the applicability. More types of inductor cores and wires also can be considered in the inductor design with a comprehensive comparison to determine the optimal design. The HF transformer model can also be developed to extend the PE component library in PSCAD/EMTDC.

7.4. List of Publication

- **Journal/Transaction Papers**

1) Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, "An Electrical Transient Model of IGBT-Diode Switching Cell for Power Semiconductor Loss Estimation in Electromagnetic Transient Simulation," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2979-2989, Mar. 2020.
2) Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, "Design, Implementation and Validation of Electro-Thermal Simulation for SiC MOSFETs in Power Electronic Systems," *IEEE Trans. Ind Appl.*, vol. 57, no. 3, pp. 2714-2725, May-June 2021.
3) Y. Xu, C. Ho, A. Ghosh, and D. Muthumuni, "Generalized Behavioral Modelling Methodology of Switch-Diode Cell for Power Loss Prediction in Electromagnetic Transient Simulation," *Energies*, vol.14, no.5, pp.1500, Mar. 2021.
4) A. Ghosh, C. N. M. Ho, J. Prendergast, and Y. Xu, "Conceptual Design and Demonstration of an Automatic System for Extracting Switching Loss and Creating Data Library of Power Semiconductors," *IEEE OJ-PEL*, vol. 1, pp. 431-444, Sept. 2020.

- **Conference Papers**

5) Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, "A behavioral transient model of IGBT for switching cell power loss estimation in electromagnetic transient simulation," in *Proc. IEEE APEC*, Mar. 2018, pp. 270-275.

6) Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, “A Datasheet-Based Behavioral Model of SiC MOSFET for Power Loss Prediction in Electromagnetic Transient Simulation,” in *Proc. IEEE APEC*, Mar. 2019, pp. 521-526.
7) Y. Xu, C. N. M. Ho, and K. K. M. Siu, “The Efficiency Enhancement of a Single-phase Single-stage Buck-boost type Manitoba Inverter Using SiC MOSFETs for Residential PV Applications,” in *Proc. IPEMC ECCE Asia*, Nov. 2020, pp. 729-734.

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Appendix A

In this appendix, an example of parameter extraction for the proposed generalized semiconductor model is presented. The Si IGBT (IKW40T120) is selected as an example. Two main software tools (WebPlotDigitizer-3.8-Desktop and MATLAB-Curve fitting toolbox) are used for the parameter extraction. The detail of the procedure is presented as follows.

A.1. Capacitance characteristics

(1) Generally, the nonlinear capacitance curves can be found in the datasheet as follows. Capture the curves and save them as an image.

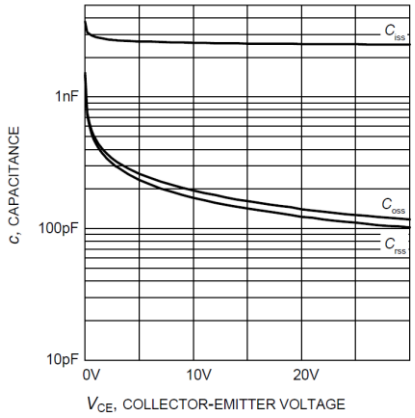

Figure A-1 Typical capacitance as a function of collector-emitter voltage ($V_{GE} = 0V$)

(2) Import the capacitance curve image to WebPlotDigitizer. Calibrate the axes and scale, and then the capacitance data can be acquired and exported. Typically, the unit of capacitance and voltage are pF and V, respectively.

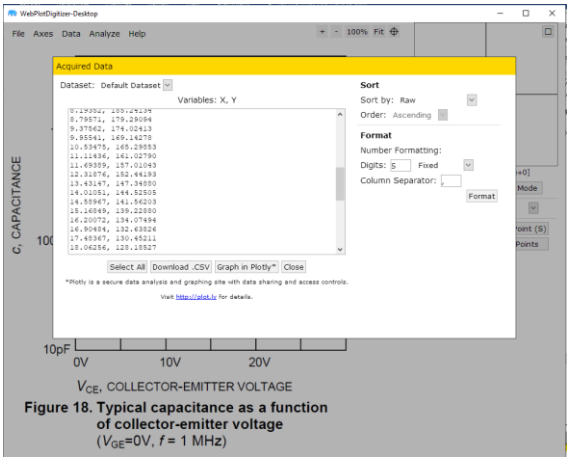

Figure A-2 Capacitance data extraction by software

(3) Reform the capacitance data and create the capacitance look-up table as follows.

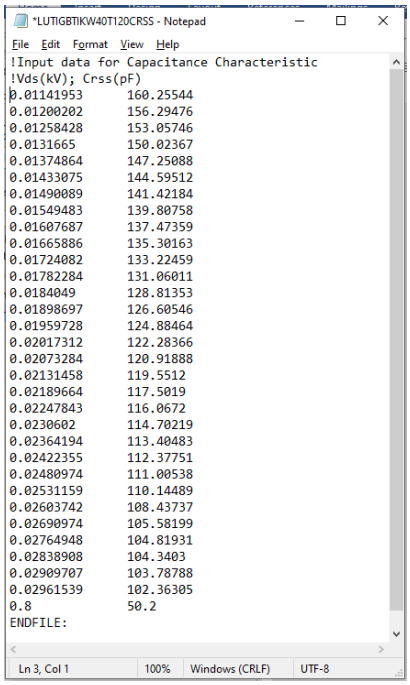

Figure A-3 Capacitance look-up table format

(4) Obtain and save all the capacitance tables.

(5) Use the loop-up table by an X-Y transfer function from the master library in PSCAD. Set the parameters such as the File name and Pathname. Typically, Relative pathname is selected, and in this case, all the tables are put under the same folder of the simulation file. The input of the X-Y transfer function is the DC link circuit voltage, and the output is the corresponding capacitance value.

A.2. On-state characteristic

For the on-state characteristic, the on-state saturated voltage v_{cesat} is typically used for the case of IGBT while on-state resistance $R_{\mathrm{DS(on)}}$ is used for the case of MOSFET or eGaN HEMT. The parameter extraction procedure is similar, and here v_{cesat} is used as an example.

(1) The on-state curves can be found in the datasheet as follows. Capture the curves and save them as an image.

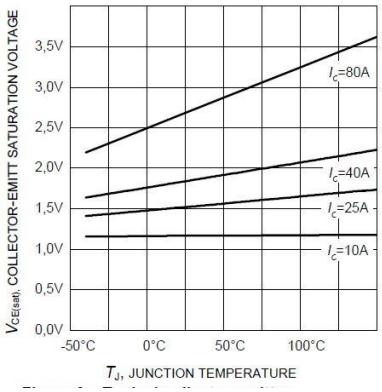

Figure A-4 Typical saturation voltage as a function of junction temperature (v_{GE} = 15V)

(2) Import the voltage curves image to WebPlotDigitizer. Calibrate the axes and scale, and then the voltage data can be acquired and exported. Typically, the unit of v_{cesat}, testing current and junction temperature are V, A, and ℃, respectively.

(3) Import the parameter data, including voltage current and temperature, into MATLAB. Use the curve fitting toolbox in MATLAB to obtain the fitting coefficients. The fitting method, algorithm, and robust setting can be adjusted for better results. For this case, the fitting equation was mentioned in Chapter 5-equation (0.1).

(4) Set the fitting coefficients in the switch model.

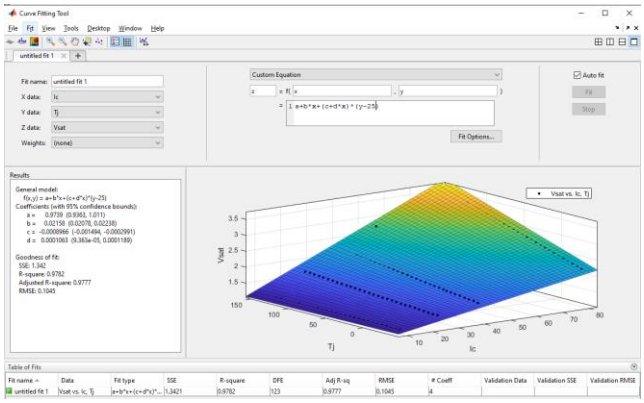

Figure A-5 Curve fitting for saturation voltage parameter using the toolbox

A.3. Turn on threshold voltage

Generally, the turn-on threshold voltage v_{T} curve is provided in the datasheet, which is temperature-dependent. If this curve is not available, v_{T} can be considered as constant with the typical value provided in the datasheet.

(1) Capture the v_{T} curve and save as an image.

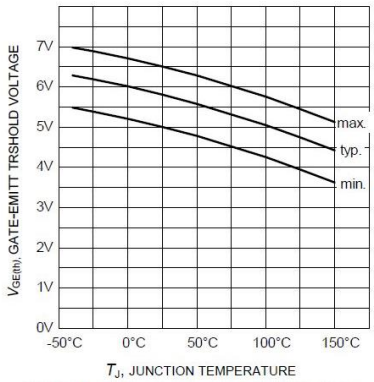

Figure A-6 Gate-emitter threshold voltage as a function of junction voltage

(2) Import the V_t curve image to WebPlotDigitizer. Calibrate the axes and scale, and then the corresponding data can be acquired and exported. Typically, the units of v_T and junction temperature are V and ℃, respectively.

(3) Import the parameter data, including voltage current and temperature, into MATLAB. Use the curve fitting toolbox in MATLAB to obtain the fitting coefficients. The fitting method, algorithm, and robust setting can be adjusted for better results.

(4) Set the fitting coefficients in the switch model.

A.4. Transfer characteristic

Generally, the trans-conductance (g_{fs}) can be obtained based on the transfer curves in the datasheet, which is temperature-dependent. For simplicity, g_{fs} can be considered as constant or temperature independent.

(1) Capture the transfer curves and save them as an image.

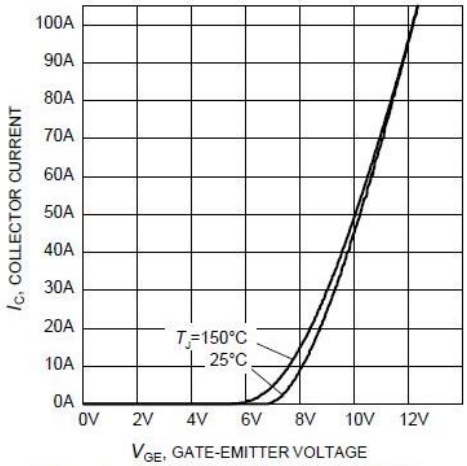

Figure A-7 Typical transfer characteristic of IGBT from the datasheet

(2) Import the transfer curve image, calibrate the axes and scale, and then the corresponding data can be acquired and exported. Typically, the unit of $v_{\mathrm{ge}}(v_{\mathrm{gs}})$, current and junction temperature are V, A, and ℃, respectively.

(3) Import the parameter data, including voltage current and temperature, into MATLAB. Use the curve fitting toolbox in MATLAB to obtain the fitting coefficients. The fitting method, algorithm, and robust setting can be adjusted for better results. Note that the parameter of v_{T} has been extracted first and used in the fitted equation. Also, the fitted equation can be 1^{st} or 2^{nd} order for better results.

(4) The values of g_{fs} for different temperature conditions are obtained. Furthermore, the temperature-dependent coefficients of g_{fs} can be obtained by using exponential or 2^{nd} order polynomial function.

(5) Set the fitting coefficients in the switch model.