The Design and Construction of An Ultra High Speed Functional Digital IC Tester

by

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THE DESIGN AND CONSTRUCTION OF AN ULTRA HIGH SPEED FUNCTIONAL DIGITAL IC TESTER

BY

ROCCO MATRICARDI

A Thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

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Abstract

Testing high speed (> 1 GHz) digital ICs is not a trivial task. Clean and fast edge rates (< 150 ps) as well as a controlled impedance DUT (Device Under Test) environment are required for proper IC characterization. Unfortunately, in a university setting a high speed tester (HP, Tektronix, IMS) is not financially feasible and hybrid or ad hoc testing techniques are utilized. These techniques provide limited IC characterization results and are very inflexible. This thesis will illustrate the design and construction of an ultra high speed functional digital IC tester capable of providing adequate IC characterization and much more flexibility and variability than hybrid or ad hoc testing techniques. High speed design issues such as PCB design, transmission line design and crosstalk will be discussed and some experimental impedance and crosstalk measurements will be presented. Some tester (pin driver) output waveforms will be illustrated and analyzed if they are suitable for testing. Also, a GaAs 2:1 multiplexer will be tested with the constructed tester and the results will be compared to results acquired from a hybrid test setup.

Acknowledgments

I would like to thank my thesis advisor Dr. Greg Bridges, whose guidance and infinite patience would not have made this thesis possible. Every graduate student should have the opportunity to work with such an understanding supervisor. Many thanks go to my family whose love and motivation helped me complete this thesis. I would also like to thank the department of electrical engineering technicians and Brad Brown who provided many excellent design suggestions and who were always there to lend a helping hand. Finally, I would like to thank Micronet for providing funding during my studies.

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Chapter 1.0

Introduction

Silicon logic families (TTL, FAST, CMOS, etc...), which offer toggle rates below 100 MHz and rise (t_r) and fall (t_f) times of 5 ns, are the mainstay of the electronic industry. Functionally testing these relatively low speed circuits and systems is fairly routine. Functional testing a circuit or system is defined as applying inputs which would verify whether a system's designed functions were indeed performed correctly. This type of testing is the brute force method of testing circuits and is only practical for SSI (small scale integration) circuits. Fault characterization and fault testing of high speed logic, specifically GaAs logic, will not be discussed in this thesis but can be found elsewhere [1-2]. There are numerous companies that produce multiple-pin (> 256) low speed testers. HP (Hewlett Packard), IMS and Teradyne are but just a few of many companies that produce such testers.

In the late 1980's high speed GaAs SSI circuits, from such companies as Triquint, Gazelle, Gigabit and Vitesse, became commercially available and offered maximum toggle rates ranging from one to three GHz and sub-nanosecond (150 ps) rise and fall times. Also, current silicon (Si) devices such as BiCMOS are slowly reaching these levels as well. Functionally testing these high speed digital ICs at their maximum clock rate is not a trivial task. A high speed tester, specifically the pin electronics, must provide clean waveforms to the Device Under Test (DUT) with fast

rise and fall times (< 150 ps) and a minimal amount of skew between inputs. A tester must also be capable of capturing, usually with a high bandwidth comparator, fast rise time signals with sub 50 ps timing errors. A low speed tester can be used to perform functional testing on higher speed ICs at the lower speeds or at "DC testing". A GaAs IC vendor defines "DC testing" as the parametric and functional testing of a high speed IC, such as digital GaAs, with present low speed testers [22].

Since the late 80's, a handful of companies and research groups have constructed high speed digital testers or pattern generators. Prices range from US $500 000 for a 10 Gb/s single channel pattern generator (Adventest or Anritsu) to US $5 million for a multiple pin (24 channel) 1.20 Gb/s digital IC tester (Photon Dynamics). If one does not have the financial means, as the situation often is in the university setting, one is forced to set up a hybrid test system. A hybrid test system would consist of a custom DUT board, RF signal generator, power splitters and a high frequency scope. Unfortunately, this does not allow much variability in test pattern generation.

This constraint in test pattern variability is the impetus for designing a high frequency digital tester for a thesis project. Initially, the goal of this thesis was to design a "proof of concept", two to four channel ultra high speed functional digital IC tester. This would be comprised of a four channel pattern generator and a four channel DUT capture and store. After careful evaluation of the effort required to design, assemble and test the system as well as some difficulties encountered during the initial PCB layout phase, the tester design objectives were scaled down to a two channel high speed pattern generator. The DUT outputs would be viewed using a high bandwidth (400 MHz bandwidth) DSO (Digital Scope Oscilloscope) instead of a capture and store system. Although the tester construction has been scaled down, the DUT capture and store system will still be discussed.

The KISS (Keep It Simple Stupid) philosophy was emphasized while planning

the pattern generator. The tester (pattern generator) was to utilize off-the-shelf components, as mentioned previously, and commercially available PCB (FR-4) materials. The tester will utilize a memory-multiplexer architecture and have a maximum NRZ (Non Return to Zero) test vector or bit rate of 1.20 Gb/s. The tester must be able to operate in *continuous* and *one shot* testing modes. In *continuous* mode, the tester repeats or continuously loops through a test vector set until the user terminates the process. This mode permits the viewing of the DUT outputs with an oscilloscope. In *one shot* mode, the tester terminates operation after cycling through a set of test vectors once. This testing mode is advantageous when testing state machines.

On board tester operation would be controlled by a microcontroller which in turn is a slave to a 80486 PC. A Microsoft WINDOWS^{TM} interface will allow a user control the bit rate and test vector patterns. Since the tester is designed to test any GaAs or Si logic family, the pin driver's output voltage levels must be adjustable and able to drive both high impedance ($> 1\ M\Omega$) and 50 Ω loads with sub-nanosecond (< 150 ps) rise and fall times.

This thesis will first discuss some of digital GaAs MESFET test circuits designed at the U of M and illustrate a hybrid test setup. The hybrid setup was inflexible and as mentioned previously was the impetus for designing a tester for a thesis project. Chapter three will overview a generic architecture found in both high and low speed testers, followed by a brief overview of a few ultra high speed testers that have been developed by university research groups and industry. The remainder of the chapter will discuss the chosen tester architecture and all the modules, such as power supply and PLL clock generation, which comprise the tester system.

Chapter four discusses high speed design issues that must be addressed to complete a successful system design. The discussion and analysis will be from a system designer's point of view. Issues such as crosstalk, transmission line design, ground/power distribution and ground noise will be discussed. A noise budget and a

worst case timing analysis will also be presented.

Chapter five will illustrate the system verification of a portion of the tester and present some tester output patterns. A GaAs 2:1 multiplexer will be tested and its results will illustrate the tester's versatility over hybrid test methods. Finally, chapter six will provide some recommendations to improve the tester architecture and present some conclusions.

Chapter 2.0

Digital GaAs Circuit Design and Hybrid Testing

This chapter will begin by discussing two digital GaAs (Gallium Arsenide) MESFET projects designed at the U of M. These projects consisted of various types of digital test circuits and utilized a popular digital GaAs logic family which will be briefly described. The DC transfer characteristics and some transient test results of a 2:1 multiplexer will be illustrated as well as some transient test results. The transient analysis was carried out using a hybrid test setup. The hybrid setup can provide some useful transient information but, as will be illustrated, it is very inflexible and has its limitations. These limitations are the impetus for designing a custom tester for this thesis.

2.1 U of M GaAs Circuit Design Projects

Digital GaAs MESFET integrated circuit design has been available at the University of Manitoba since 1991. Two GaAs circuit design projects have been submitted and fabricated. The first, in July 1991 (coordinated and funded by the Canadian Microelectronics Corporation) and a second submission in July 1992 (U of M funded). A die photograph of the 1991 submission, which was designed by the author, is shown in Figure 2.1. The die area is approximately one mm^2 and contains two 2:1 multiplexers

(right side of die), two D Flip Flops (left side), one five stage ring oscillator (bottom center) and a large depletion mode (multifinger) MESFET with coplanar pads for on wafer probing (center). The second submission contained a VCO (voltage controlled oscillator), T-Flip Flop, backgating structure, resistors and a clock generator (seven stage R.O.) with variable phase shift. A receiver (ECL-to-GaAs translator) and driver (GaAs-to-ECL translator), which were used in a majority of the test circuits, were provided by the CMC (Canadian Microelectronics Corporation). The driver's output logic levels are ECL compatible (VSWING $\approx$ 1V) and are capable of driving 50 Ω loads. The chips were packaged in a twenty-eight pin LDCC (Leaded Chip Carrier) and will be illustrated later on in this chapter.

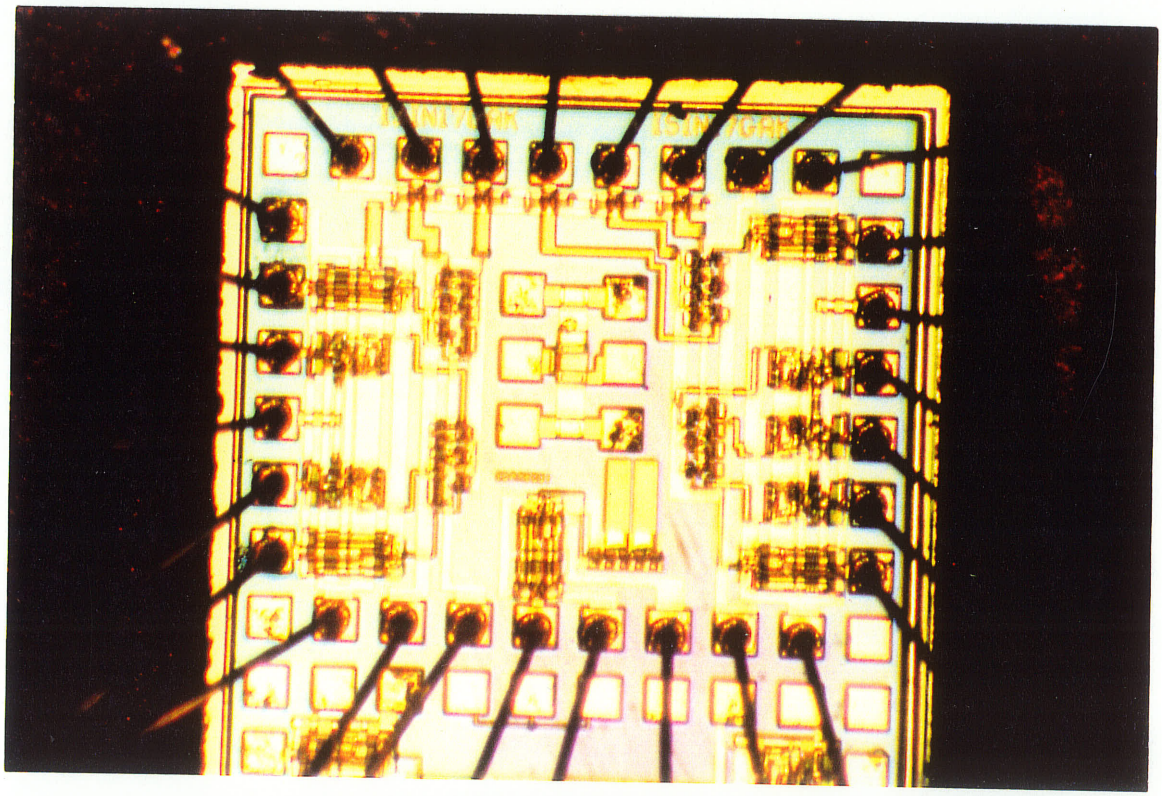

Figure 2.1: Die photograph of 1991 GaAs test circuit submission.

Both submissions were fabricated at Vitesse Semiconductor Corporation (Camarillo, CA), which is one of among a handful of digital GaAs MESFET foundries worldwide. The circuits were fabricated with Vitesse's H-GaAs II process. H-GaAs II

is a three metal layer enhancement/depletion (E/D) process, which offers an 0.8 μm effective gate length. Vitesse currently uses their third generation process, H-GaAs III, which offers four metal layers and a 0.6 μm effective gate length [3]. Their fourth generation process (H-GaAs IV) is currently under process review and will be available in late 1994 [4].

The logic family utilized in both submissions was the popular DCFL (Direct Coupled FET Logic) family. DCFL is a viable candidate for the VLSI arena because of its compact size and low power dissipation [5] and is the logic family utilized by Vitesse in most of their products (gate arrays & communication ASICs). Typical delays for a MESFET DCFL inverter are 85 ps [5] and 50 ps delays for GaAs HFET inverters. An HSPICE equivalent circuit for a MESFET and a DCFL inverter with a fanout (F.O.) of one are illustrated in Figure 2.2.

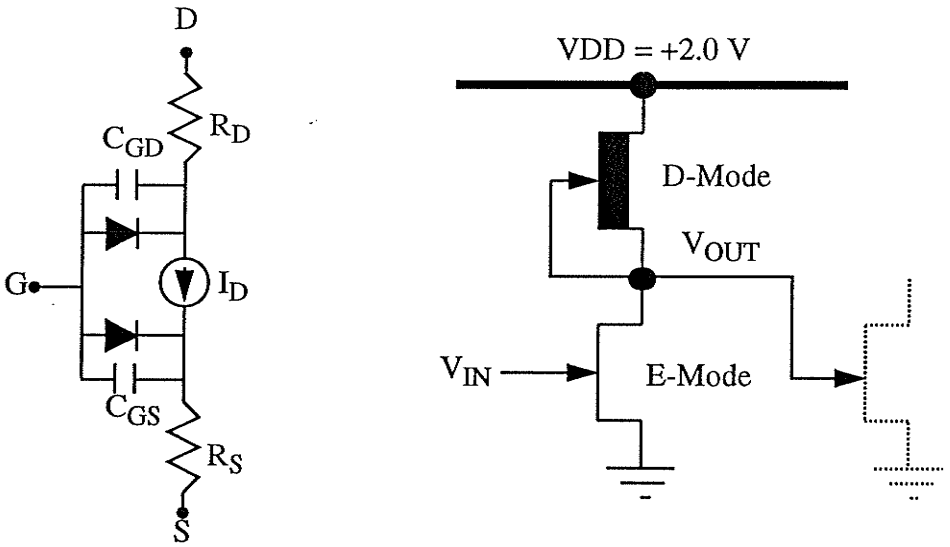

Figure 2.2: HSpice™ equivalent GaAs MESFET circuit and a DCFL inverter.

The d-mode (depletion) transistor has its gate and source tied together and acts as a current source. The e-mode (enhancement) transistor acts as a switch, by sinking current from the current source or steering it to the MESFET of the next stage. The DCFL structure is similar to Si NMOS logic. The simulated HSPICE DC transfer char-

acteristics of a typical DCFL inverter with a fanout of one, two, four and eight loads is illustrated in Figure 2.3. V_{OH} (Logic High) and V_{OL} (Logic Low) are 0.65 V and 0.05 V respectively and typical noise margins are for a fan out of one.

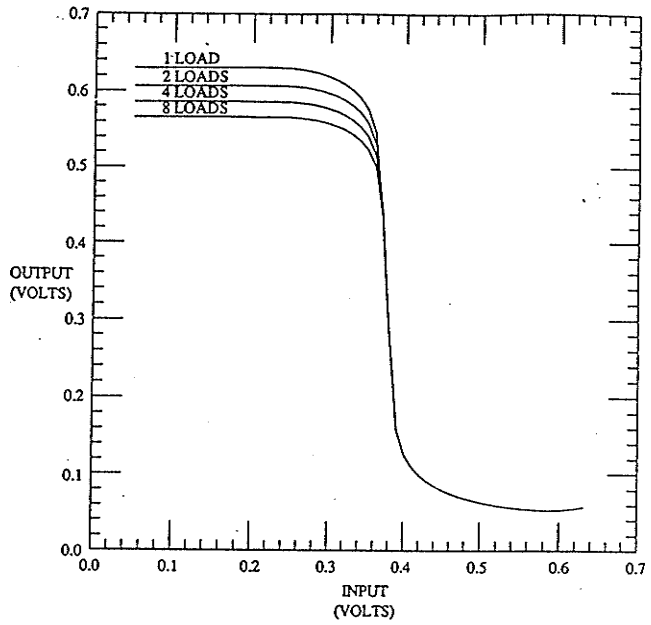

Figure 2.3: HSpice DC transfer curves for a DCFL inverter [5].

As the fanout increases the V_{OH} level decreases. This is due to the current source's (d-mode transistor, see Figure 2.2) maximum current capability. As the fanout increases, each fanout gate will source a smaller current from the current source and hence the voltage across its gate to source diode (V_{OH} = 0.55 - 0.65 V) will be smaller. The resulting gate to source diode is the reason for the small voltage swing and low noise margins in DCFL. Detailed analysis of DCFL and other digital GaAs MESFET logic families can be found elsewhere [32] and will not be discussed further.

A test circuit that was thoroughly tested, and also functioned properly, was a 2:1 multiplexer. Table 2.1 illustrates the logic table for a 2:1 multiplexer and Figure 2.4 illustrates its circuit diagram. The DC transfer characteristics of the multiplexer

were measured with an HP4145A parameter analyzer.

Table 2.1: Truth Table of a 2:1 multiplexer.

Select	B	A	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

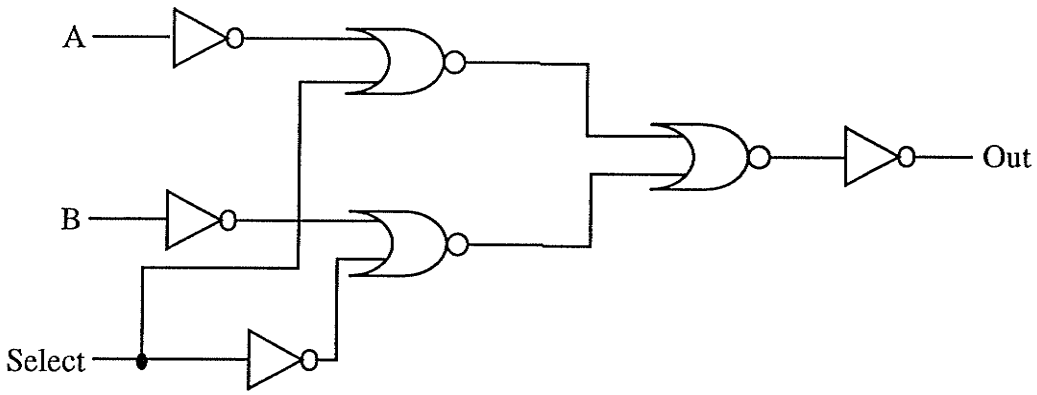

Figure 2.4: Circuit diagram of a 2:1 multiplexer.

In this particular test, Input A of the multiplexer was selected (Select = logic "0") as the output and Figure 2.5 illustrates the resulting DC transfer characteristics (V_A vs. V_{OUT}) of the multiplexer driving a 50 Ω load. As mentioned previously, (GaAs-to-ECL) drivers were connected to most digital circuits as is the case with this

multiplexer. The output voltage swing is approximately 1.1 V which is similar to an ECL voltage swing. The threshold voltage is 0.3 V and the V_{OH} and V_{OL} are 1.1 V and 0.05 V respectively The multiplexer, according to HSpice^{TM} simulations, is expected to function up to 300 MHz.

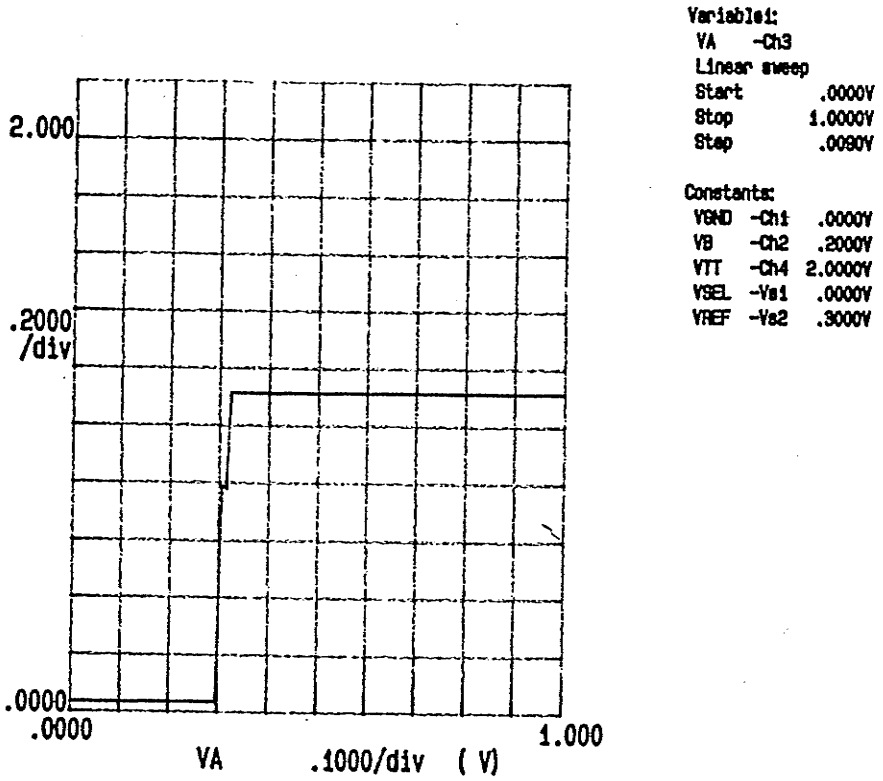

Figure 2.5: DC transfer curve for a GaAs 2:1 multiplexer.

Transient testing of the multiplexer was completed utilizing a hybrid setup which is illustrated in Figure 2.6. The setup consists of a Tektronix 7S12 oscilloscope with a plug in sampling and pulse generator head. A pulse generator (S-6) provides a 200 mV rising pulse with a 35 ps rise time (20-80%) and a period of approximately 20 μs. The pulse is viewed on the scope by using a sampling head (S-52). A pulse swing of at least 0.45 V is needed to produce an input high level (V_{IH}) for a DCFL circuit. A wideband amplifier (ZFL2000) and a programmable attenuator (HP11716A) are used to provide the 0.45 V swing. The attenuator is needed to attenuate the pulse (5 db) into the amplifier so that the amplifier's maximum output power specification are not

exceeded. With this particular setup the multiplexer's rise and fall times can be measured.

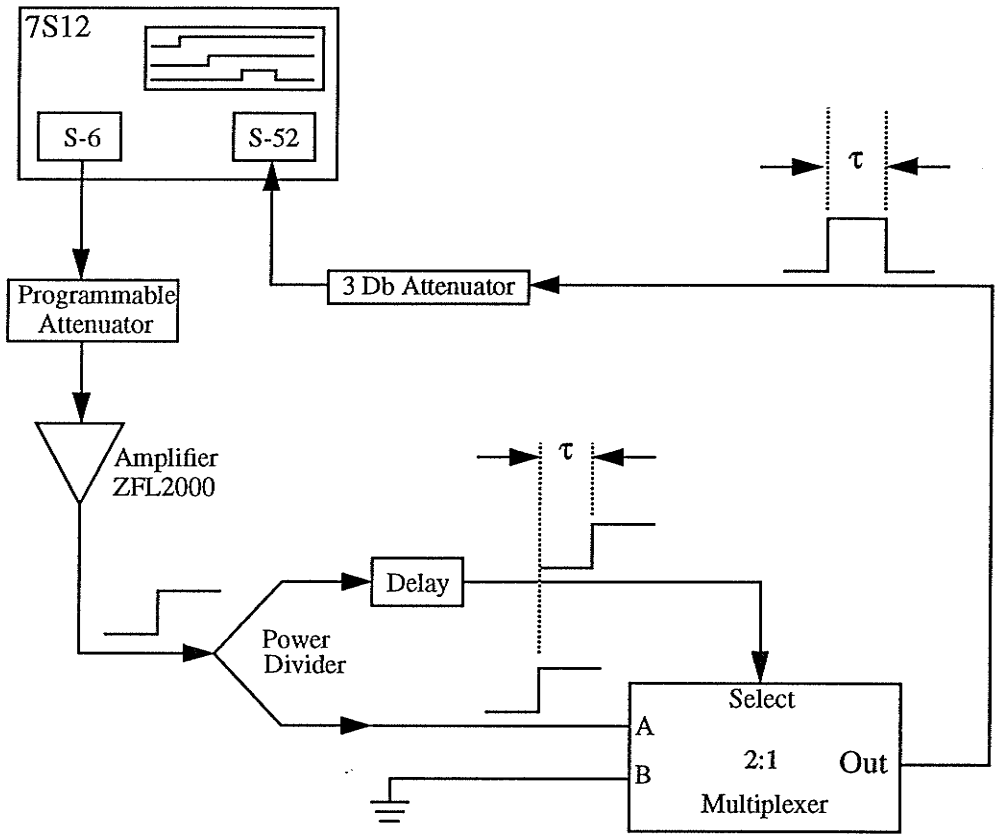

Figure 2.6: Hybrid test system used to characterize a 2:1 multiplexer.

Figure 2.6 illustrates, a method of testing the rise and fall times of the multiplexer. Input (B) is set to logic "0" (grounded) and a rising pulse is fed into Input A. The pulse is first attenuated and then amplified (ZFL2000). As mentioned previously, the attenuation is required to prevent damage to the amplifier. The pulse is then split in two by a power splitter and the resulting pulse amplitude out of the divider is approximately 450 mV. One of the pulses is delayed with a length of coaxial cable and fed to the Select input. As shown in Figure 2.6, the Select line is initially at logic "0" (grounded) and therefore Input A is selected at the output (Out). The output will then switch from logic "0" to logic "1". As the Select line switches to logic "1", input B is

selected and the output switches from logic "1" to logic "0" as illustrated in Figure 2.6. Figure 2.7 illustrates the resulting oscilloscope photo and the rise and fall times are 350 ps and 400 ps respectively.

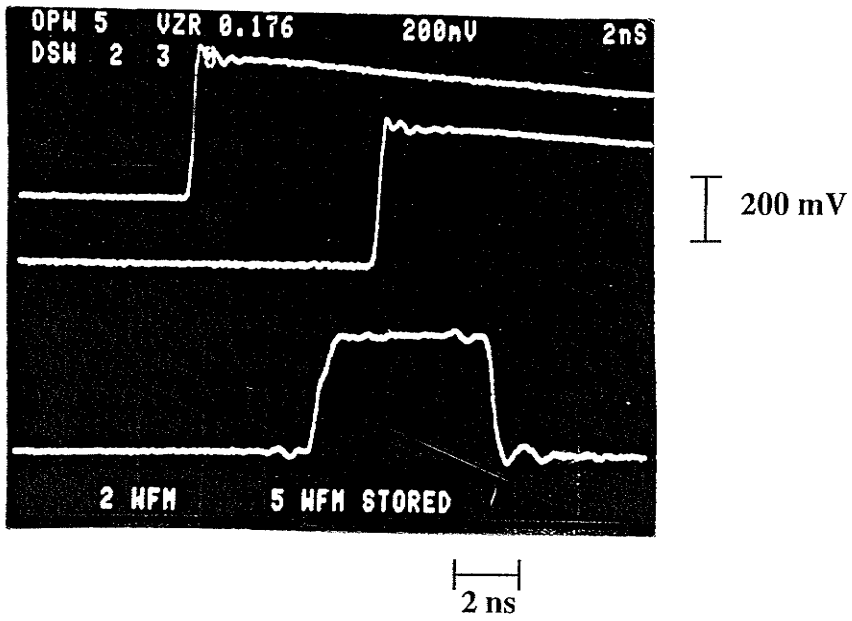

Figure 2.7: Scope photograph of a 2:1 multiplexer transient test output.

Figure 2.8 illustrates a photograph of the hybrid system. The DUT (Device Under Test) board and the 28 pin LDCC package clamped are shown. The DUT board was purchased from the UCSB (University of California Santa Barbara) and utilizes 50 Ω microstrip transmission lines. The test setup is quite bulky and its testing capabilities are limited. The hybrid test system does not offer pattern variability, which is essential for functionally testing circuits.

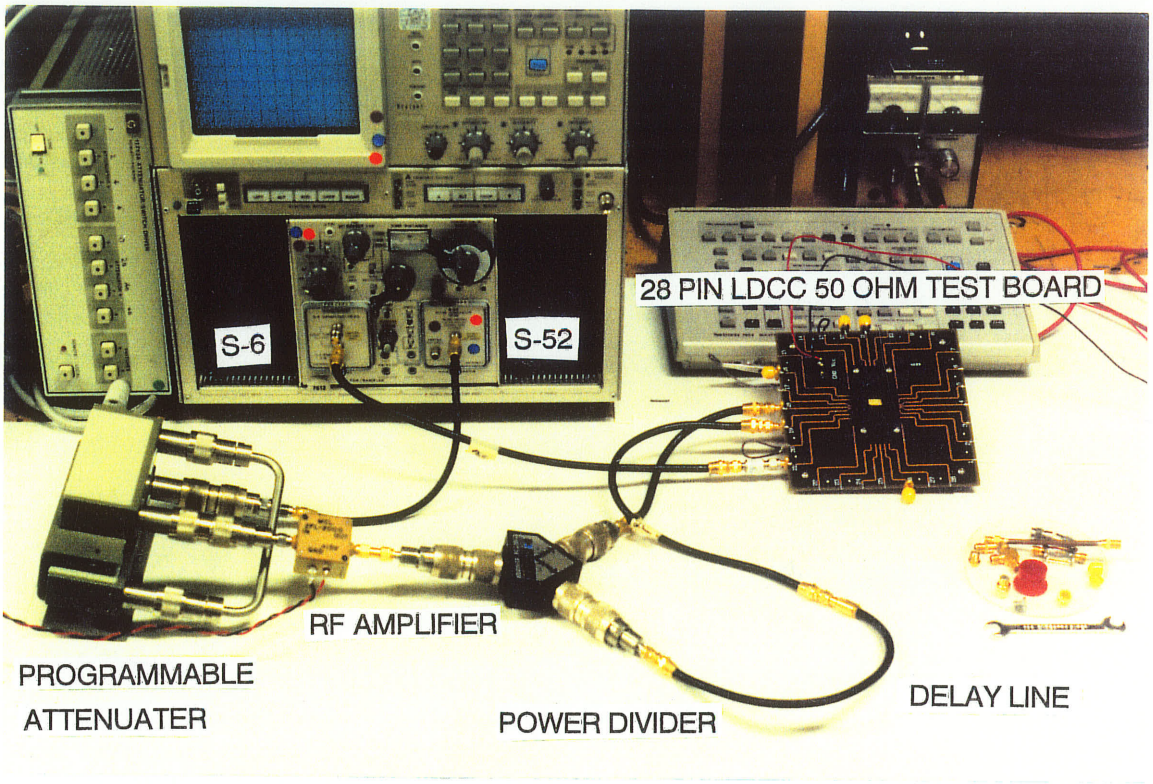

Figure 2.8: Photograph of a hybrid test system and the DUT board.

Chapter 3.0

Tester Architecture Overview

This chapter will begin by briefly reviewing the architecture of a generic tester, specifically the pin electronics. The pin electronics are the heart of a tester and this generic structure can be found in the majority of commercially available high and low speed testers. Three unique ultra high frequency testers designed in the mid and late eighties will be briefly described. The remainder of the chapter will discuss the proposed tester architecture and the modules that comprise the system. The architecture and each module will be thoroughly discussed.

3.1 Generic Tester Architecture

The key elements in a low speed digital IC tester (<200 MHz) or ATE (Automatic Test Equipment) as they are called in industry are the pin electronics. The function of the pin electronics is to drive DUT input pins and to measure outputs. The pin electronics are usually designed to support both drive and measure functions [6]. Figure 3.1 illustrates a generic pin electronics configuration that is prevalent in most testers (< 200 MHz). It consists of a pin driver, dynamic load and dual comparators. Pin drivers provide the inputs to the DUT. Also, pin drivers typically have programmable logic high and logic low levels and usually have a high impedance state or off

state. The programmable logic levels, typically from -2V to +7V, provide compatibility with TTL, ECL and CMOS voltage levels. When measuring DUT outputs, the test system switches the pin drivers to an off state and measures the output levels with the comparators [6-7]. The dual comparators can verify data-book specifications such as minimum logic high and maximum logic low levels.

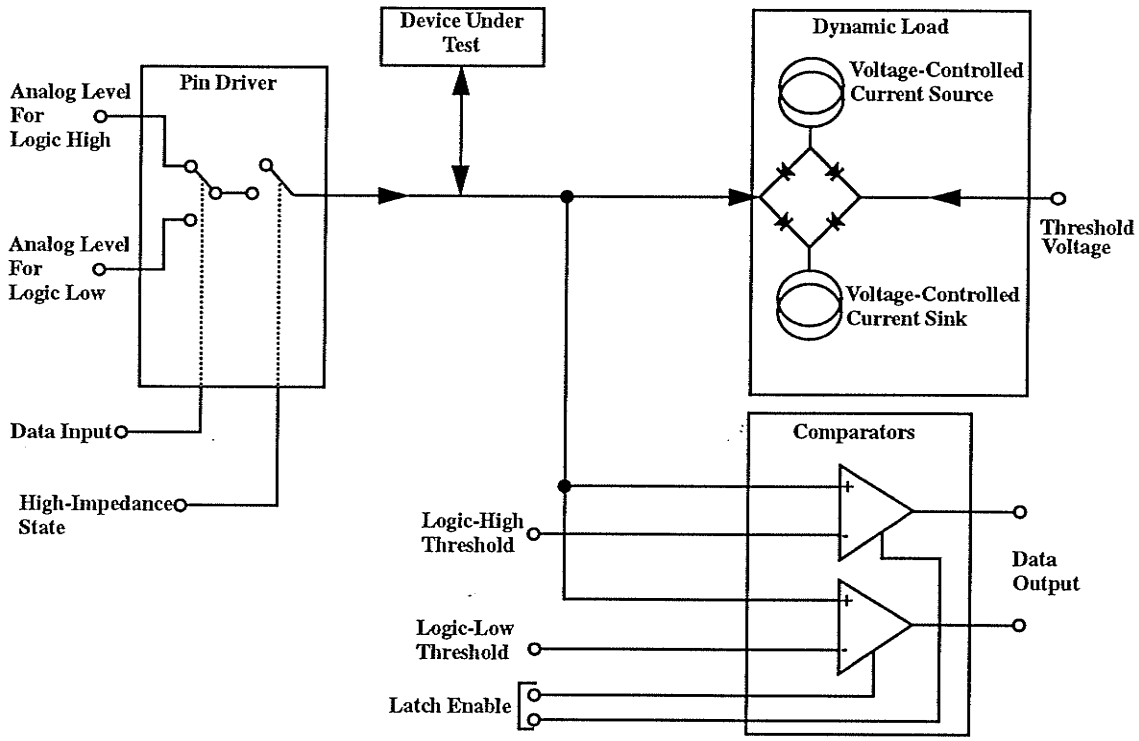

Figure 3.1: The basic ATE pin-electronic are drivers, comparators and dynamic loads [7].

3.2 Ultra High Speed Tester Architectures

In the late eighties, GaAs and high speed Si logic families such as ECL reached rates much greater than 200 MHz. This made "at speed" testing impossible with current digital low speed testers. What usually occurs in the testing arena is the high speed logic that requires testing is utilized in the testing equipment itself. Since

the mid eighties, there have only been a few high speed testers constructed to functionally test high speed logic families in the GHz range. Three unique architectures found in the literature will be briefly discussed.

A research group at UCSB (University of California Santa Barbara), headed by Dr. Steven Long and Dr. Steven Butner, have been involved in digital GaAs circuit design since the early eighties. In 1987 [8], this group constructed a GaAs digital IC tester to functionally test (maximum 1 GHz NRZ) the digital GaAs logic circuits they had developed through Vitesse Semiconductor. They investigated numerous architectures, but decided on a shift register architecture that is illustrated in Figure 3.2.

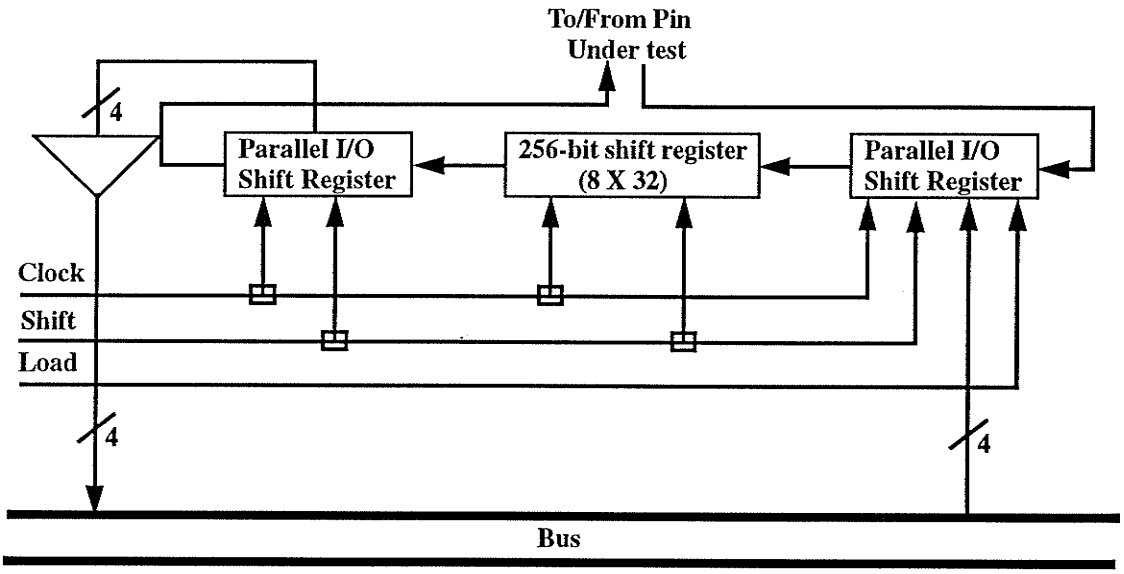

Figure 3.2: Shift register architecture [8].

A high speed channel consists of shift registers (264 bits long, 8 X 32 bit serial I/O shift registers and 2 X 4 bit parallel/serial I/O shift registers) and clock phasing and fan-out ICs. The clock phasing IC synchronizes the high frequency clock (maximum 1 GHz), which is distributed to each channel, and provides the edge placement resolution of 50 ps. The shift registers and clock phasing and fan-out ICs, which were custom built GaAs ICs designed at UCSB, are the only parts of the tester that are run-

ning at high frequency.

These GaAs ICs were then placed in *hybrid semiconductor modules*, which are built on a 10 layer polymide PCB (Printed Circuit Board). A module, along with slower speed Si ICs, were then placed on a *high speed interface* PCB (seven layer glass-epoxy). There is one *high speed interface* board for each pin of the device under test. Each *high speed interface* board (one I/O channel) can be connected to a device-under-test (DUT) input pin (high speed input) or its output pin (high speed output). The tester is constructed around a VME system card and backplane. A Motorola MC68000 microprocessor, aboard the VME card, controls the operation of the tester. The microprocessor loads and read test vectors from the *high speed interface* boards at low speed (8 MHz). A Colby pulse generator was used as a high frequency clock.

A second group, Photon Dynamics [9-12], developed a very sophisticated and expensive (US $5 million) commercially available ultra high speed tester. This group designed a twenty channel tester capable of a 1.2 Gb/s NRZ (non-return-to-zero) or RZ (Return-to-Zero) test vector rate. The tester architecture utilized a memory-multiplexer architecture which consisted of GaAs ICs, which where custom fabricated, and commercially available ECL ICs. A PLL (phase-locked loop) per pin architecture was utilized to distribute and synchronize the master clock between channels. This type of clocking distribution provides very good synchronization between channels. The clock exhibited very low jitter because of the utilization of a very stable ND:YG mode-locked laser as a PLL reference frequency [11]. The DUT measuring scheme, capture and store, used a very elaborate electro-optic measuring system that utilizes the Pockels effect [9]. The tester was used to compare performance characteristics between high speed commercially available (vendors unnamed) GaAs and Si ICs [10]. The results illustrated some of second order effects digital GaAs logic circuits suffer, particularly the "GaAs MESFET hysteresis" or drain lag effect which will be discussed in chapter five.

A third group involved with ultra-high frequency tester development is headed by Dr. David Keezer at the University of South Florida [13-17]. This group modified an HP8200B (maximum 200 MHz) tester by retrofitting it with modules containing commercially available GaAs ICs (Gigabit Logic). They utilized the HP8200B's fifty ps edge placement capability and GaAS XOR ICs (10G002) and a GaAs pin driver (16G061A) to interleave eight channels at 200 MHz in to one ultra high frequency channel running at 1.6 Gb/s as illustrated in Figure 3.3. The group also designed a real time data capture with GaAs ICs (D-FF) to achieve data capture rates of up to 1.20 Gb/s.

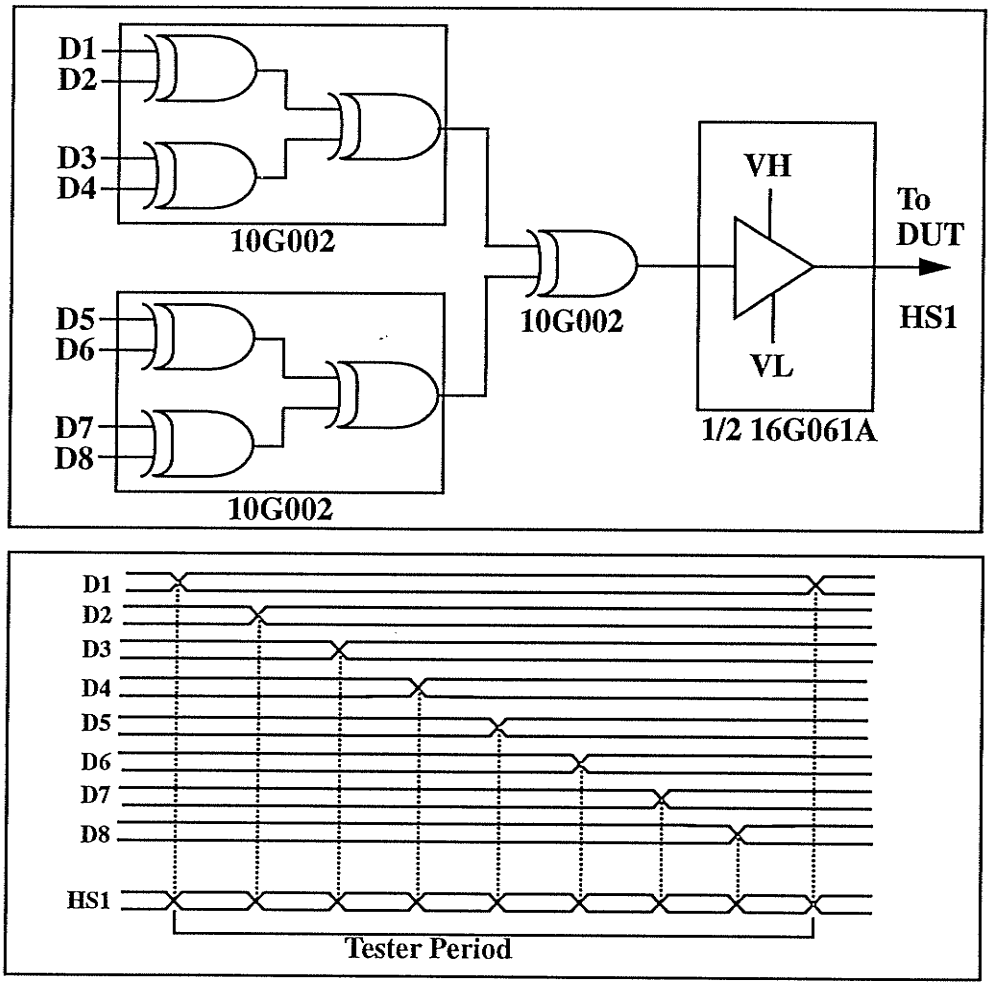

Figure 3.3: XOR tree for 8:1 multiplexing [13].

3.3 Tester Architecture

The **initial** objective of this thesis was to design a "proof of concept" four channel tester (pattern generator and capture and store). A multi-pin tester (20 pin) - pattern generator and capture and store system - similar to a generic low speed tester or the previously mentioned projects was not financially feasible or appropriate for a thesis. The tester will **only** utilize commercially available ICs. Designing custom GaAs ICs, similar to the UCSB and the Photon Dynamics projects, would be extremely risky and would be a thesis in itself.

Initially, the option of retrofitting the U of M ASIX tester similar to what Keezer's team had accomplished was considered. The ASIX tester is a multipin tester capable of test vector rates of thirty MHz. To multiplex one high speed data channel (1.2 Gb/s) would require twenty XORs gates. This solution would be impractical and extremely expensive if GaAs ICs were utilized. Also, the ASIX tester would be very difficult to modify since schematics were not readily available. Another problem is that the ASIX's software is very difficult to use and inflexible.

There are currently a handful of digital GaAs vendors that offer a large variety of SSI, LSI and VLSI ASICs and gate arrays. Vendors such as Gigabit (now owned by Triquint), Triquint and Vitesse currently offer a variety of SSI ICs such as XORs, D-flip flops as well 12:1 multiplexers and 1:12 demultiplexers. These ICs operate well above one GHz and some up to three GHz. With so many different ASICs currently available the option of designing a custom made tester was chosen. Some system design goals must now be established and they are as follows:

1) Maximum NRZ (Non Return to Zero) test vector rate of 1.20 Gb/s

2) The tester's output voltage levels (V_{OH} & V_{OL}) must be variable to allow testing of any GaAs or Si logic family.

3) Design with commercially available ICs.

4) Use common PCB laminates (glass expoxy, $\varepsilon_r = 4.2$) and limit the layer count to 4-6 layers. No expensive or exotic PCB laminates such as PTFE or Cyanate Ester.

5) Local tester control is provided by a microcontroller (DS5000) and global control through a 80486 PC. The PC allows a user to input test vector patterns and control the test vector bit rate.

6) A simple HF (high frequency) clock distribution (1:N buffer) scheme to each tester channel.

7) Allow test vector variability and a deep test vector set.

8) Allow fine output edge placement (~ 50 ps resolution) capability.

9) Allow *one shot* and *continuous* test mode operation.

Once the system design goals have been set an architecture must be chosen. A memory-multiplexer architecture somewhat similar to one investigated by Long and Butner [8] was chosen.

As mentioned previously, a four channel tester (pattern generator & capture and store) was desired. Two PCBs (four layers), one for the pattern generator and the other for the capture and store, were being considered for fabrication. Since developing both a pattern generator and a capture and store would be a large undertaking, it was decided to develop only the pattern generator. The DUT (Device Under Test) outputs would be viewed with a high bandwidth oscilloscope. Nonetheless, the proposed capture and store options will still be discussed. For the remainder of this thesis the pattern generator will be defined as the **tester**.

Problems surfaced during the initial IC placement and routing of the four channel tester PCB. An initial timing analysis also revealed that a four channel tester utilizing the current architecture was unrealizable with a four layer PCB. Also, four PCB layers would be required just to accommodate the numerous power planes and split power planes. Consequently, the numerous power planes and timing requirements

forced the tester to be scaled down further to only two channels. A six layer twelve by twelve inch PCB would be required for the two channel tester. The estimated cost for six copies of the six layer PCB was $3300.00. Adding additional PCB layers would achieve the timing requirements for a four channel tester (pattern generator). On the other hand, designing a ten to twelve layer PCB would increase the cost by 200 - 300% over a six layer PCB. These cold financial facts are another factor to limit the tester to a two channel pattern generator. Figure 3.4 illustrates the proposed tester system. Each section or module will be thoroughly discussed in the proceeding sections of this chapter.

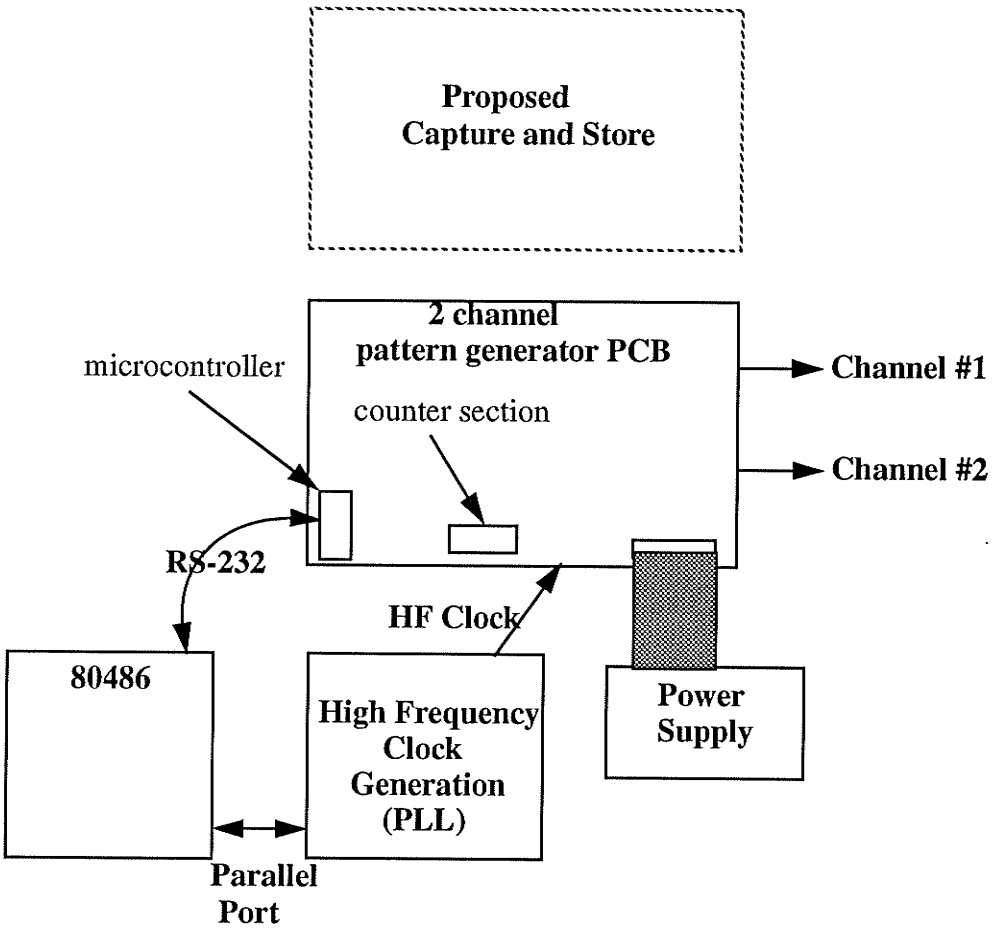

Figure 3.4: Proposed Tester system configuration.

3.3.1 Memory Multiplexer Pattern Generation Architecture

Figure 3.5 illustrates the proposed memory-multiplexer architecture. The heart of the tester architecture is the 12:1 multiplexer. The multiplexer is a data conversion device that converts 12-bit wide parallel data (max 206 Mb/s) to serial data up to 1.25 Gb/s. The majority of the ICs used are GaAs, BiCMOS and ECL ICs. Dotted lines emphasize the ultra high frequency sections (600-1200 MHz or 600 - 1200 Mb/s). GaAs ICs are exclusively used in the high frequency section. The GaAs ICs consist of a 1:4 fanout buffer (Gigabit 10G011-3), 12:1 multiplexer (Vitesse VS8001) and a pin driver (Triquint TQ6330M). All the GaAs and BiCMOS ICs are compatible with F100K series ECL (Emitter Coupled Logic) logic levels and noise margins.

When in *test* mode a high frequency clock, from an RF generator or PLL (Phased Locked Loop), is distributed to each multiplexer's high frequency clock input (CLK) with a 1:4 fanout buffer. The term *test* mode refers to when the tester is driving test vectors to a DUT. The CLOCK12 output from the channel two multiplexer is distributed to both multiplexer's DCLOCK inputs and the ECL counter section. The CLOCK12 output, which is the high frequency clock (CLK) divided by twelve, allows the accommodation of various timing constraints which will be discussed in chapter four. In the tester's case, the CLOCK12 output triggers the counters to the next SRAM address and hence presents a new twelve bit address to the multiplexer's parallel data inputs (D_{11} - D_0). Very fast (five ns access time) BiCMOS 4K x 4 bit SRAMs were required to meet system timing requirements. Each channel then consists of three SRAMs (4K x 12 bits) and provides 49152 bits or test vectors.

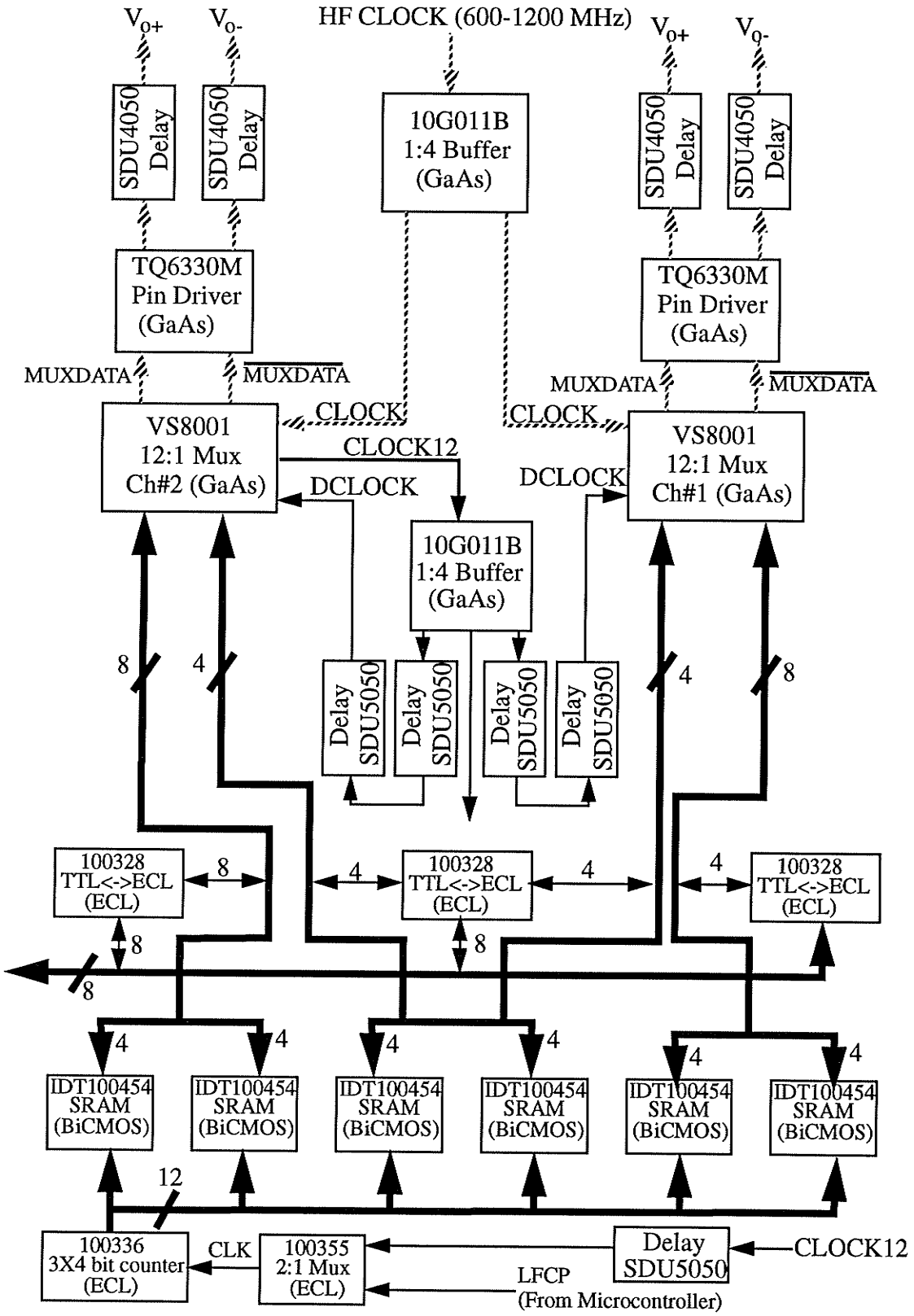

Figure 3.5: Tester memory-multiplexer architecture.

3.3.2 HF (High Frequency) clock distribution and PLLs

A high frequency clock capable of operating up to 1.20 GHz is required to provide test vectors up to 1.20 Gb/s. The noise and jitter of the clock must be as small as possible because it will be directly transferred to the data at the output of the pin driver. Jitter on a pulse edge is illustrated in Figure 3.6 and is defined as the random time uncertainty of a waveform event relative to a particular point [18].

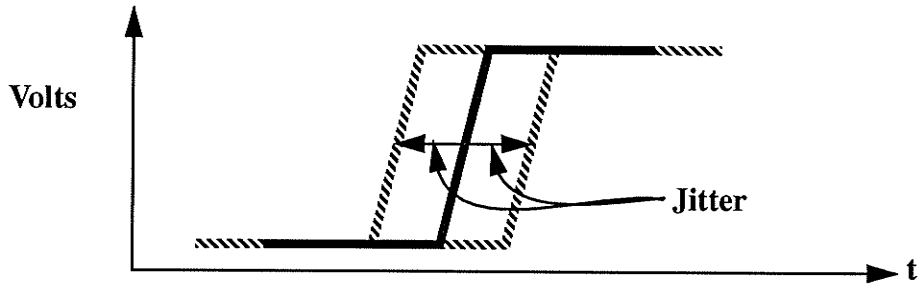

Figure 3.6: Jitter on a pulse edge.

This random uncertainty of the edge will cause timing errors at a DUT, especially if the pattern is repetitive such as an alternating one and zero pattern (50% duty cycle).

An HP8350 wideband RF generator (.1 - 10 GHz) is available at the U of M. Unfortunately, the generator is very bulky and its frequency resolution is only 0.1 MHz. Wideband Phase-Locked Loops (PLL) have been used as microwave frequency synthesizers for decades [19-20] will offer better jitter (stability) performance than the RF generator, which uses mixing techniques. Figure 3.7 illustrates a basic PLL topology used for frequency synthesis.

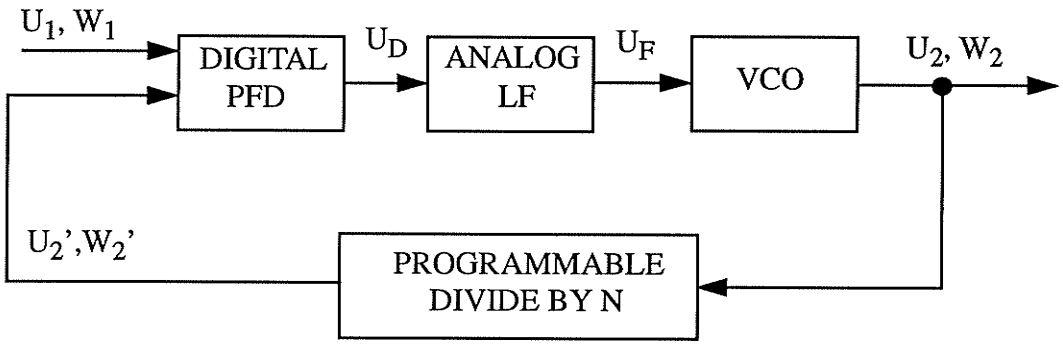

Figure 3.7: Typical digital PLL frequency synthesizer configuration.

The basic components that comprise a PLL frequency synthesizer are a phase/ frequency detector (PFD), programmable divider, VCO (voltage controlled oscillator) and a loop filter (low pass). The basic function of the PLL is as follows. A reference frequency (W_1), which is also the step size or resolution of the frequency synthesizer, is provided to one input of the PFD. The output signal from the VCO (W_2) is then divided by N (W_2') and compared to the reference frequency. The PFD then compares both signals for phase and frequency differences. A frequency difference would be caused by changing the programmable divider (N), which in turn changes the frequency of the divided VCO signal (W_2').

If there is a difference (phase/frequency error), the PFD develops an output signal (U_f) proportional to the phase error. The output signal of the PFD consists of an AC component and a DC component. The undesired AC component is filtered by the loop filter and the resulting DC component will then be applied to the VCO. The VCO's output frequency (W_2) will then be increased or decreased depending on the phase error until the frequency or phase error between its divided signal (W_2') and the reference signal (W_1) is near zero. Hence, the output frequency is changed by varying N the programmable divider.

The choice then for a high frequency clock (600-1200 MHz) was a PLL

(Phase-Locked Loop) Frequency Synthesizer evaluation board (Q0410) from Qualcomm [21]. The PLL evaluation board is designed to provide an output (sine wave) with a frequency ranging from 600-1200 MHz. In reality, the PLL output frequency ranges from 675 - 1200 MHz. Some fine tuning of the loop filter is still needed to increase the frequency range. Also, the evaluation board provides a connector footprint so a (Centronics port) parallel port can be used to vary the dividend (N) in the PLL, which in turn changes the operating frequency of the PLL. The reference frequency used is 2.5 MHz, which was due to PLL stability constraints encountered in designing wideband PLLs. Therefore, this particular PLL frequency synthesizer did not offer a better frequency resolution than the HP RF generator. A much finer clock resolution or step size (~1 Hz) can be quickly realized if DDS (Direct Digital Synthesis) is employed as the PLL reference frequency [21]. This would require another daughter board that can be purchased from Qualcomm.

The PLL should still provide a much better jitter performance than the RF generator. This is important because any jitter on the clock is directly transferred to the data because the high speed clock clocks the data out of the 12:1 multiplexer. The distribution of the PLL high frequency clock on the tester board was kept very simple. The clock is first AC coupled to a GaAs 1-to-4 fanout buffer. A GaAs 1-to-4 fanout buffer (Gigabit 10G011B-3) was used to distribute the HF clock to both multiplexers CLK inputs. The trace lengths to both CLK inputs were identical and typical skew between outputs on the buffer is specified as 30 ps. Also, the traces were spaced far apart from each other and other traces, so electrical issues such as crosstalk (See Chapter four) will not be a factor.

3.3.3 Counter Section

One of the design goals was to have the tester operate in both a *one shot* and *continuous* mode. The *one shot* mode would allow testing of state machines, and allow

the tester to stop at any particular state. The *continuous* mode repeats the test vectors in a looping action and conveniently allows viewing of both the input test vectors and the DUT outputs with an oscilloscope. Three four-bit synchronous (100336 four bit parallel load serial ECL shift/counter) counters are cascaded to provide the twelve bits of the SRAM address (A_{11} -A_0) bus. Figure 3.8 illustrates the counter section and extra circuitry needed to provide *one shot* and *continuous* mode. The counter's complementary outputs ($\overline{Q}_{11}$-$\overline{Q}_0$) are used to drive the twelve bit address bus since the outputs (Q_{11}-Q_0), specifically the four least significant counter bits (Q_3-Q_0), are required to provide the *one shot* and *continuous* mode capability.

The ECL quad 2:1 multiplexer allows the counter to be switched between a *load* mode and *test* mode. In *load* mode, the microcontroller has control of the counter's select inputs (S_2 -S_0) and the counter's clock (CCLK). Table 3.1 illustrates the functions of certain Select Inputs.

Table 3.1: ECL Counter's Function Select Table.

S_2	S_1	S_0	Function
0	0	0	parallel load
1	0	0	count down

The S_1 and S_0 inputs are connected directly from the microcontroller, but the S_2 and clock (CCLK) inputs are first routed through an ECL quad 2:1 multiplexer. The multiplexer permits switching the counter's clock (CCLK) input between the CLOCK12 input, used in *test* mode, and the LFCP input used in *load* mode. Once the counter is under microcontroller control, the starting twelve bit address can be loaded via TTL/ ECL bidirectional latches into the counter's preset inputs (P_{11}-P_0) with a low frequency clock (LFCP). The latches always present the starting address to the preset inputs (P_{11}-P_0), which is a crucial factor for the tester to operate in *continuous* mode.

Once the starting address is loaded, the counter is switched over to *test* mode. The address loading action sets S_2 high and sets the counter in a count down mode (S_2-S_0 = 100) and ready to proceed testing.

While in *test* mode the counter's clock (CCLK) will utilize the CLOCK12 output of the GaAs 12:1 multiplexer (via the 1:4 buffer) and also utilize the S_2 value provided by the "extra circuitry". Also, either *continuous* or *one shot test* mode can be chosen. The O/C (O/C = 1 *one shot* & O/C = 0 *continuous*) input controls this option from the microcontroller. While in *continuous* mode the counter section works as follows. For the special circuitry to work the counter must be in countdown mode (S_2-S_0=100). As the counter reaches zero (Q_{11}-Q_0=000000000000), $\overline{TC}$ switches low and forces S_2 to switch low. The counter will then be in parallel load mode (S_2-S_0=000). As mentioned previously, the starting address is always present at the counter's preset inputs (P_{11}-P_0) because of the TTL/ECL latch. At the next rising clock edge, the starting address will be loaded into the counters and the D-FF switches the S_2 input from high to low, which allows the counter to resume counting down.

The "special circuitry" must meet certain timing requirements, specifically the S_2 (select input) setup and hold times relative to the counter clock. The timing requirements were met through careful IC positioning and trace layout. The "one shot" operation is somewhat similar. If O/C is set high, then the "one shot" mode is enabled. As the count reaches Q_{11}-Q_0=000000000001, one of the four input OR/NOR ($\overline{TC}$ • (Q_3-Q_1)) gates switches low and eventually propagates through another OR/NOR gate to force $\overline{CET}$ (count enable) to switch high. The counter is then stopped at Q_{11}-Q_0=000000000001 and will then signal the microcontroller ($\overline{CET}$ also routed to the microcontroller) that the test has been completed.

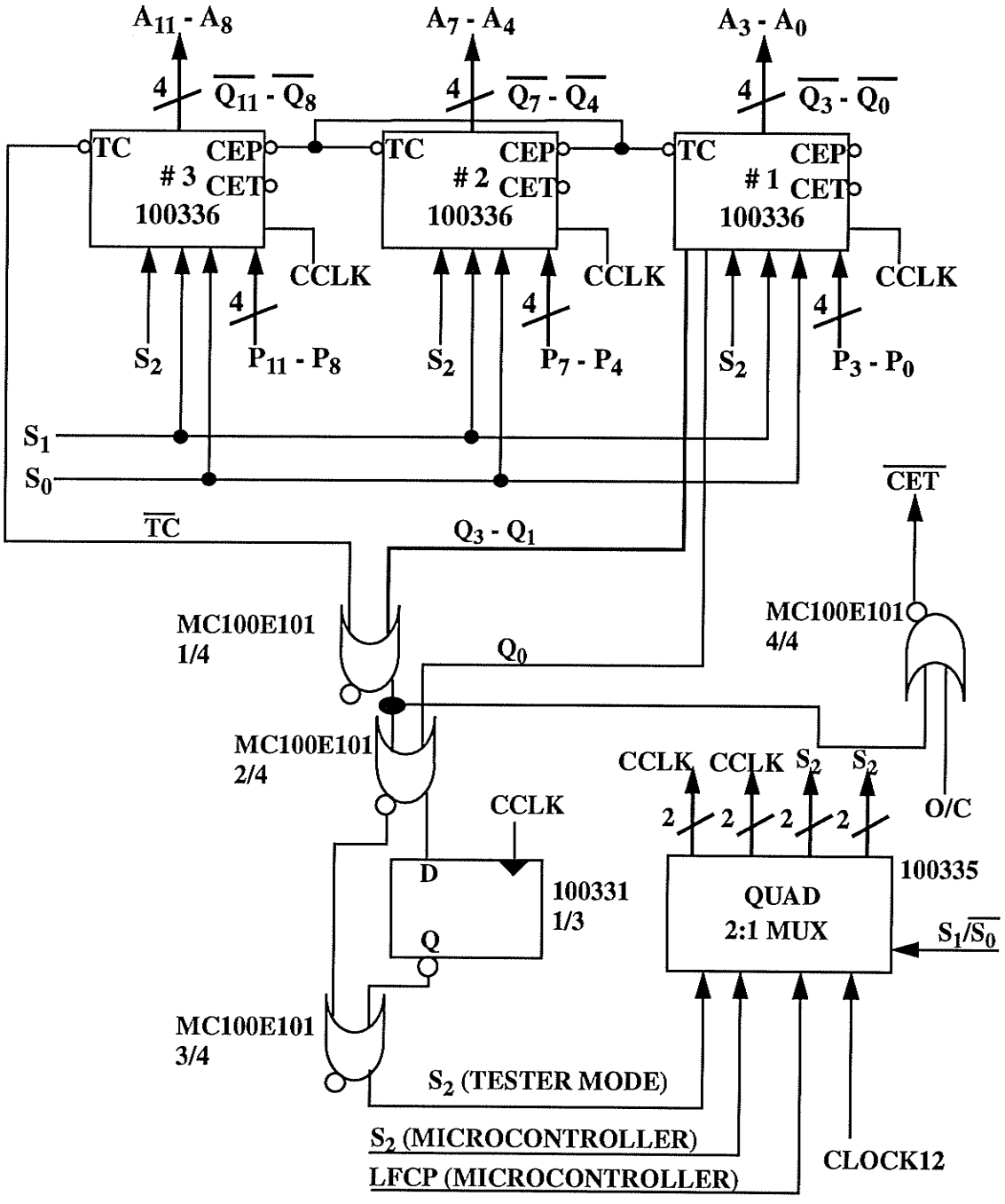

Figure 3.8: Schematic of counter and special circuitry.

3.3.4 Microcontroller algorithm

One of the design goals was to have the tester designed around a microcontroller. The microcontroller used is the 8-bit DS5000 (Dallas Semiconductor) which is pin per pin compatible with the popular INTEL 8051. The DS5000, located on the tester board, was chosen because it can be quickly programmed through an RS-232 serial port - no EPROMs need to be burned. Figure 3.9 illustrates the DS5000 and all of the tester's low speed control signals. The control signals are translated from TTL to ECL with 100324 Hex TTL to ECL translators. Two GALs (Generic Array Logic) were needed to provide some control signals (SRAMs WE*X* and CS*X*) because of a shortage of port pins. Table 3.2 specifies the tester control signals, their functions and the ICs that require them.

The microcontroller itself acts as a non-intelligent controller and is a slave to a 80486 personal computer (PC). The PC issues codebytes (commands) (i.e. BITXER1) to the microcontroller and it then takes control of the tester and loads or retrieves test vectors from either channel or initiates a test. A set of codebytes (8 bit) were developed and a few of these codebytes and there definitions are illustrated in Table 3.3.

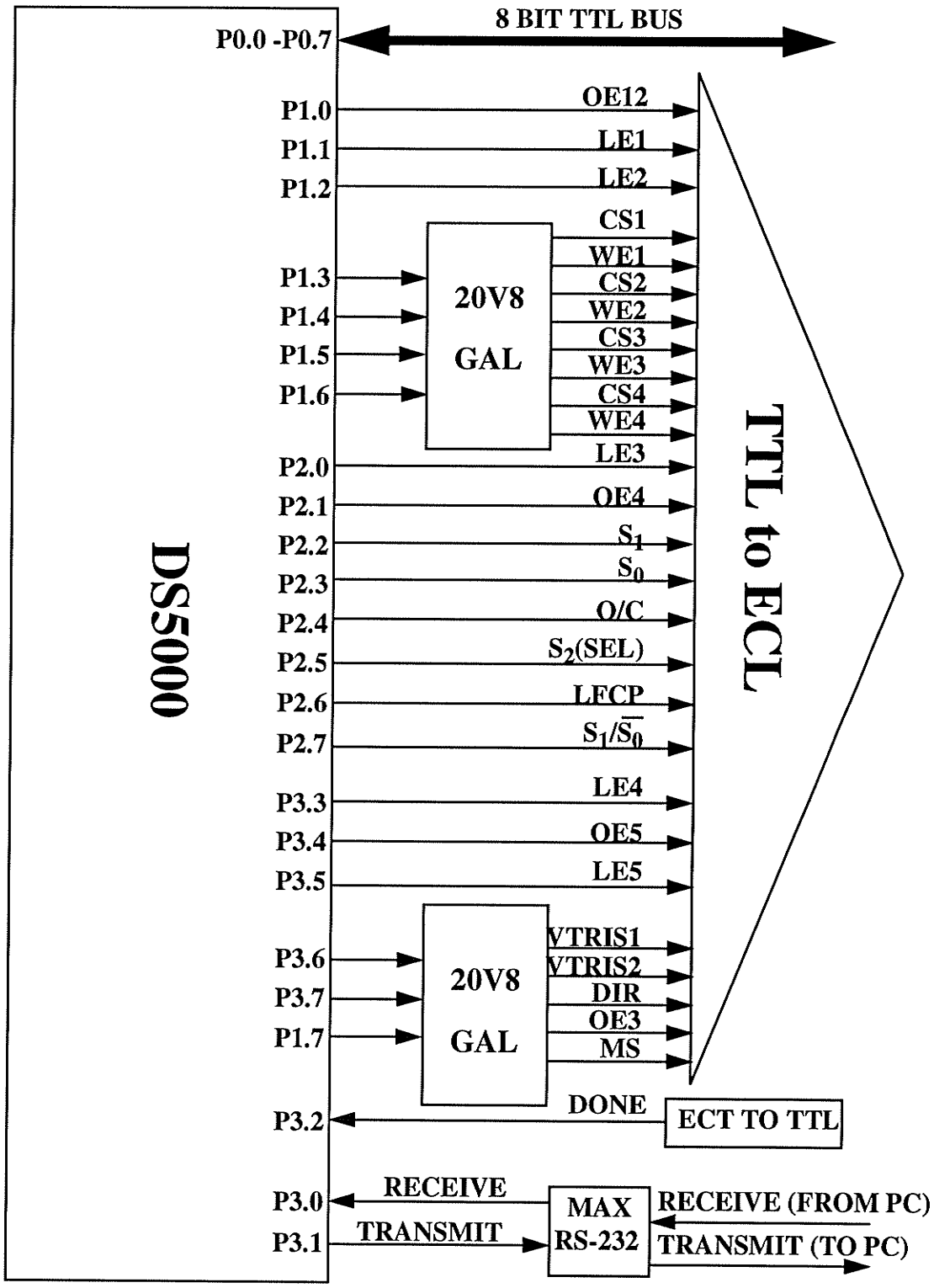

Figure 3.9: DS5000 microcontroller and all the tester's low speed control signals.

Table 3.2: List of low speed tester control signals.

Pin Name	Part Description	Function
LE*X*	100328 ECL/TTL bidirectional translator latch	Latch Enable Input
OE*X*	100328	Output Enable Input
CS*X*	IDT 100A454 4K x 4 bit SRAM	Chip Select
WE*X*	IDT100A454	Write Enable
S_X	100336 4 bit counter	Select Inputs
VTRIS*X*	TQ6300M pin driver	Tristate Enable
LFCP	100336 4 bit counter	Low Frequency Clock
DIR	100328	Direction Control Input
S_1/S_0	100355 quad 2:1 mutiplexer	Select Inputs

Table 3.3: List of codebytes.

Codebyte	Definition
BITXER*X*	Load (write) test vectors into channel # *X*.
MEMTEST*X*	Retrieve (read) test vectors in channel # *X*.
OSHOT*X*	"One shot" test mode, channel # *X*.
NUMBYTE	Number of bytes to be loaded or retrieved.
STOP	Stop tester operation.

The PC and microcontroller communicate through a RS-232 serial port and utilize an ACK - ACK protocol. For example, when the PC sends a codebyte, the microcontroller acknowledges receiving it by responding with an ACK. If it is an unrecognized codebyte, due to a transmission error, the microcontroller responds with

a NACK. Once the PC receives the ACK from the microcontroller, other codewords or a databyte can then be sent. For example, if the codeword NUMBYTE was transmitted and the microcontroller acknowledged with an ACK. The PC will then send the NUMBYTE databyte value. The microcontroller will be expecting the NUMBYTE databyte. If a codebyte is transmitted instead, an error will occur and the microcontroller responds with an NACK. A programmable ninth bit on the serial ports provides a convenient method of distinguishing between a codebyte and a databyte. If the ninth bit is set high then the microcontroller recognizes this incoming byte as a codebyte otherwise it is a databyte.

Figure 3.10 illustrates an example of a typical transmission frame from the PC to the microcontroller. The first codebyte, BITXER1, will notify the microcontroller that databytes, test vectors in this case, will be transmitted and loaded into channel one. Along with the codeword BITXER1 (see Table 3.3), other information or codewords must be included. Codebytes such as (NUMBYTES) the number of databytes that will be transferred, and the approriatte counter starting address (ADRESSL and ADDRESSH) must also be provided. Finally, a CRC (Cyclic Redundancy Check) calculated on all the data bytes is sent once all the data bytes have been transmitted.

An example of the BITXER1 (load test vectors into channel # 1) operation would go as follows. Once, the BITXER1 codeword is transmitted the ADDRESSL and ADDRESSH codewords and databytes will follow. The tester in then put in to *load mode* as mentioned in Section 3.3.3. The counters latches must first be enabled (OE12 = 1) so they can be read data off the TTL bus. Figure 3.11 illustrates the bus and the bidirectional TTL/ECL translator latch. The ADDRESSL databyte is then loaded onto the TTL bus and latched (LE1, 0 -> 1) into the appropriate latch. The microcontroller's bidirectional 8-bit port (P0.0-P0.7) is used as a TTL 8-bit data bus. The bus is used to load (write) and read data from the SRAMs and load address values to the counter's preset inputs (P_{11}-P_0).

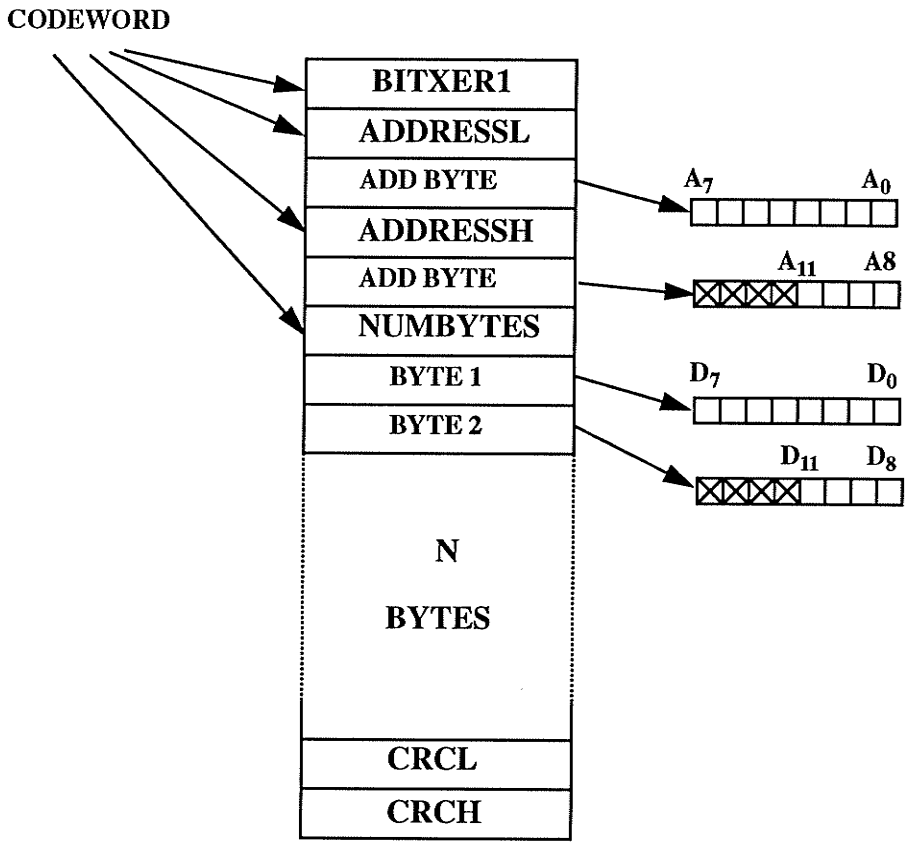

Figure 3.10: Typical transmission frame.

The ADDRESSH databyte is then put on the bus and latched (LE2, 0 -> 1). Once the ADDRESS*X* databytes are latched, the address databytes can then loaded into the counter's preset inputs. The microcontroller then sets the counter in a parallel load (S_2-S_0=000) mode and then applies a rising edge clock (LFCP) pulse to load the starting address. Once the starting address is loaded, the counter is then set to count down (S_2-S_0=100). The next codebyte transmitted is the NUMBYTE command. The NUMBYTE databyte will then follow. The databyte is then put in a counter-register on the microcontroller to allow counting of the incoming databytes.

The loading of the databytes (test vectors) into the SRAMs can then begin. First, the latches/translators must be set to translate from the TTL to ECL direction (DIR = 1). The incoming databytes are then buffered in a sixty byte FIFO (First-In-

First-Out) memory buffer created in the microcontroller's RAM. The databytes (test vectors) are then pulled out of the buffer and loaded on the 8-bit TTL bus. Once on the bus, the microcontroller enables the appropriate latch (OE3 = 1) and then loads it into the latch (LE3, 0 -> 1). The second byte is then loaded on the bus and latched (OE4 = 1) into the appropriate latch.

Take note that two databytes (Figure 3.11) are needed to load one memory location (12 bits). The first byte is loaded into data locations D_7-D_0 and the second byte (only 4 bits) are loaded into the D_{11} - D_8 (Channel 1). Once the data is latched and present at the SRAMs (D_7 - D_0) data write input pins, the microcontroller then selects (CS1 = 1) the appropriate SRAMS and then writes the data (D_7-D_0) into the SRAMs (WE1 = 1). The SRAMs (D_7-D_0) are then deselected and the remaining SRAM (D_7-D_4) is selected (CS2=1) and the second databyte is written (WE2 = 1). The counter is then clocked to advance the address value. This process is then repeated until all the databytes (test vectors) have been written. The data is written into the tester's memory "on the fly".

The SRAMs are dual port, that is they have separate data inputs and data output pins. This is common with high speed SRAMs. The data inputs and data output pins are tied together so the SRAM data can be read and written using only a bidirectional bus. This allows the memory to be checked (MEMTEST*X*) to verify that the test vectors were written correctly into the SRAM. During MEMTEST*X*, the databytes (test vectors) are transferred back to the PC, similar to the BITXER*X* operation. The transferred databytes are then compared to the original databytes that were transferred using the BITXER*X* command. The MEMTEST*X* command allows for some diagnostics or self checking of the SRAMs, but this is also under the assumption that the microcontroller, and the TTL/ECL latches are functionally properly.

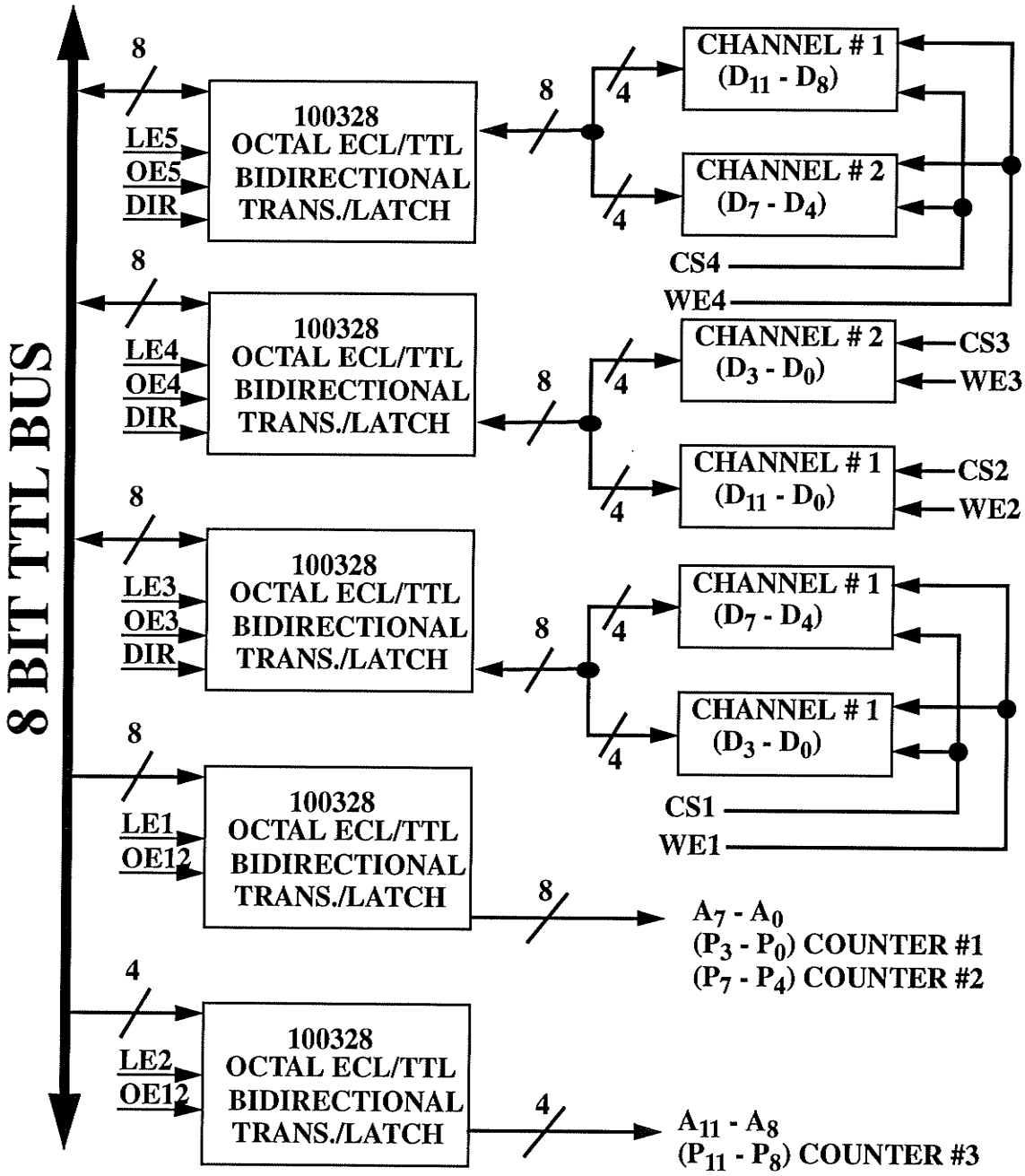

Figure 3.11: Eight bit TTL bus and bidirectional ECL/TTL translator-latches.

Once all the BITXER*X* transmissions are completed the tester is ready to be put in to *test* mode as mentioned previously in Section 3.3.3. The PC will then send

the microcontroller a codebyte (OSHOT*X* or CONT*X*) to configure the tester in either a *one shot* or *continuous* mode. Once the test mode is chosen, the counters are put in count down mode, pin drivers are enabled (VTRIS*X* = 0) and the ECL 2:1 multiplexer switches (S_1/S_0) the counter's clock (CCLK) from LFCP to CLOCK12. If the tester is in *continuous* mode the tester will continually loop until the user terminates the test. The test will be terminated by switching the counter's clock input from CLOCK12 to LFCP. If in *one shot* mode, the microcontroller will signal the tester once the test has been completed.

3.3.5 The PC algorithm

As mentioned in the previous section an 80486 personal computer is a master to the microcontroller. Along with the microcontroller, the PC also controls the PLL evaluation board through an eight bit parallel port (Centronics). The software for the personal computer was written in C++ code and also includes a Microsoft WINDOW-S^{TM} based interface. Unfortunately, both parts of the software are incomplete and therefore untested. Even so, the purpose of the PC software was to allow the user to do the following:

1) Enter the test vectors in either channel.

2) Specify *one shot* or *continuous* test mode.

3) Specify the test vector rate range and the specific test vector rate.

4) Start and stop a test during mid test.

5) Do a memory test to check the integrity of the test vectors written into the SRAMs and provide some diagnostic checking of the SRAMs.

The user must first enter the test vectors into the particular channel. The user must then choose one of the three test vector rates (*f*) available. The data rate of 600-1200 Mb/s is limited by the (600 - 1200 MHz) octave bandwidth of the PLL. One way

to generate lower vector rates is to repeat the test vector sequence. That is, to write the test vectors two or three times, consecutively in memory. Unfortunately, this does not preserve the maximum test vector length capability of 49152 bits. Table 3.4 illustrates the different test vector rates available.

Table 3.4: Choice of test vector rate ranges

f	test vector rate (Mb/s)
1	600 - 1200
2	300 - 600
3	150 - 300

Once the user has inputted all the test vectors, test vector rate and test mode, the PC software must then format the data. The twelve bit constraint (12:1 multiplexer) causes a bit of a problem. Another problem is that the data must be formatted depending on testing mode.

For example in *continuous* mode, if the test vector length is not a multiple of twelve the test vectors must be written (repeated) in memory R times. The formula used to find R is seen in Equation 3.2

$$1 \leq M \leq 4096 \tag{3.1}$$

$$R = (12 \times \frac{M}{(f \times N)}) \tag{3.2}$$

Where R is an integer, N is the number of test vectors, f is the test vector rate range and M (Equation 3.1) is a value from 1 to 4096. For example, if a test vector of seven bits long was to be used in continuous mode with test vector rate range $f = 1$, using Equation 3.2, R would then be twelve. That is the test vectors would have to be written twelve times and it would occupy seven memory locations.

To operate in *one shot* mode some formatting is also needed. Zero padding or

ones padding is needed because of the twelve bit constraint. For example, if a nine bit length test vector is to be tested in a *one shot* mode the first three bits of the twelve bit multiplexer word would be padded with zeroes or ones.

3.3.6 System Power Supply

Providing power to a system with standard supply voltage levels is usually a mundane task and a trivial part of the system design. A typical worst case scenario occurs when analog circuitry is mixed together on a PCB with standard Si logic families. This usually calls for +12, -12 V and +5 V voltage supply levels. Commercially available power supplies, be it linear or switching (DC-DC converters), are easily available in the standard +12 V, -12 V and +5 V flavors, and usually satisfy current and power noise requirements. Unfortunately, the tester required nine power supply voltage levels! The Triquint pin drivers and Gigabit Logic ICs are the main culprits. Table 3.5 illustrates the tester's required voltage supply levels and tolerances as well as typical and worst case current requirements.

Table 3.5: Tester's supply voltage levels, tolerances and current requirements.

Supply Voltage (V)	Tolerance ($\pm V$)	Supply Current (Typical) mA	Supply Current (Worst) mA
-8.0	0.5	120	180
-6.0	0.5	200	400
-5.2	0.2	930	1200
-4.5	0.2	2500	3450
-3.4	0.1	250	400
-2.0	0.1	1280	1500
-1.32	0.02	negligible	negligible

Table 3.5: Tester's supply voltage levels, tolerances and current requirements.

Supply Voltage (V)	Tolerance ($\pm V$)	Supply Current (Typical) mA	Supply Current (Worst) mA
+5	0.5	720	1000
+6	0.5	280	420

Gigabit Logic offered a linear power supply specifically tailored for their GaAs ICs supply voltage levels (-5.2 V, -2.0 V, -1.32 V, -3.4 V, -4.5 V). Purchasing this board would be very expensive and it still would not satisfy the tester's requirements. Since there was no single commercial power supply - linear or switching - that fulfilled the tester's requirements, the other option was to design a custom power supply board. The power supply board would also include some control circuitry needed for the pin drivers.

Gigabit Logic's proven power supply topology was utilized to provide five supply voltage supplies (-1.32 V, -2 V, -3.4 V, -4.5 V, -5.2 V). The schematic for the power supply was conveniently provided in the 1991 Gigabit Logic Data Book [22]. A photo of the power supply connected to the tester board is illustrated in Figure 3.12. Off the shelf linear voltage regulators would then provide the remaining four (-6V, -5V, +5V, +6V) supply voltages. A two layer PCB was constructed (see Appendix for PCB artwork). The power supply would generate all the required voltage levels and provide power to other control circuitry from only two laboratory supplies set at -12 V, +12 V(1 supply) and -8 V.

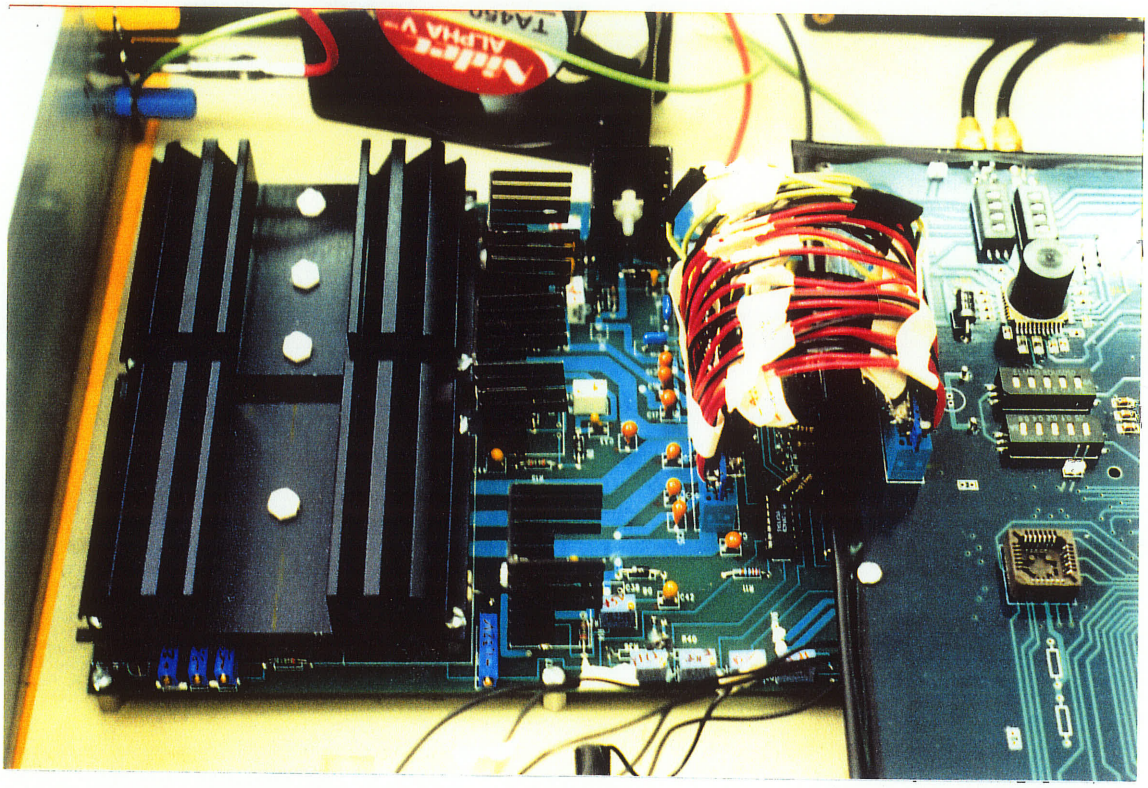

Figure 3.12: Photograph of power supply board connected to the tester.

The power supply is capable of providing five amps of current (for -5.2 V, -4.5 V, -3.4 V -2.0 V levels only) and is limited by the heatsinking capabilities. As illustrated by the photo in Figure 3.12, a lot of heat sinking is involved. This illustrates the high power requirements of ECL and GaAs ICs and one of the pitfalls of designing high speed systems. Table 3.6 illustrates static power dissipation for a few of the high powered ICs.

Table 3.6: Typical power and voltage supply levels for a few ICs.

Part	Function	Logic	Typical Power Dissipation (W)	Supply Voltages (V)
VS8001	12:1 Multiplexer	GaAs	2.6	-5.2,-2
10G011-3	1:4 Fanout Buffer	GaAs	.69	-3.4,-5.2,-2.0
TQ6330M	Pin Driver	GaAs	2.0	-8,-6,+5,+6

Table 3.6: Typical power and voltage supply levels for a few ICs.

Part	Function	Logic	Typical Power Dissipation (W)	Supply Voltages (V)
IDT100A484	4K x 4-bit SRAM	BiCMOS	1.5	-4.5

Circuitry was also needed to vary the logic high and logic low levels of the two pin drivers The output voltage levels are controlled by driving the level-control inputs (Force Inputs). Sense outputs are provided so that the user may provide a level control input to achieve the desired output, either as a calibration procedure or in a feedback loop using an op amp [23]. The output voltage can be adjusted between +3.0 V and -3.0 V when driving 50 Ω load resistors and between 0 V and +5 V when driving high impedance loads (CMOS or TTL). The pin driver outputs can be differential or single-ended and can be switched to a "Tri-State" mode (VTRIS*X*) where they become 50 Ω resistors connected to -2 V.

Additional circuitry was also needed to provide negative output voltage swings while driving grounded 50 Ω loads. The Triquint pin drivers outputs are source followers and therefore only able source current and unable to sink current. One solution was to sink additional current from the source follower through the voltage high force pin (V_{H2}) with a pull down resistor to a negative potential. An adjustable current sink with standard bipolar transistors and was designed to sink the current.

3.3.7 Capture and Store

A proposed capture and store will be briefly discussed even though there is no intention of constructing this portion of the system. A block diagram of the proposed capture and store interfaced with a DUT and the pattern generator is shown in Figure 3.13. A high speed Gigabit GaAs comparator (bandwidth=3 GHz) will be utilized to capture a high or a low from the DUT output. A second comparator could also be

added so that V_{OH} and V_{OL} levels can be investigated. The store portion is identical to the pattern generator architecture with the obvious exception of a 1:12 Demultiplexer used instead of a 12:1 Multiplexer.

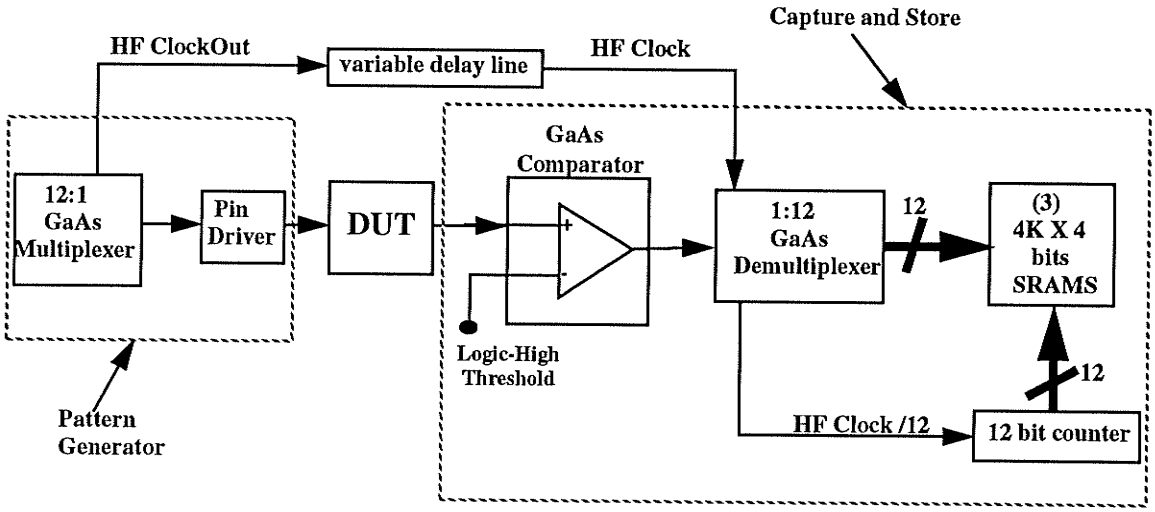

Figure 3.13: Proposed capture and store system.

The 1:12 Demultiplexer requires a HF Clock to allow capture of the incoming data stream from the DUT. As Figure 3.13 illustrates, the HF Clock would be provided by delaying the HF ClockOut from the pattern generator. It would obviously take some experimental effort to find the appropriate delay.

Chapter 4.0

High Speed System Design

This chapter illustrates the many facets of high speed system design. Issues such as high speed PCB design, transmission line design, impedance control and crosstalk will be discussed. Some impedance and crosstalk measurements will be presented and analyzed. A noise budget analysis of the tester's two major buses will be presented. Finally, a thorough worst case timing analysis of the tester will be presented.

4.1 Transmission Line Design

In high speed systems, the majority of PCB traces can not be treated as lumped (capacitors and inductors) elements but as distributed elements or transmission lines. Since the tester utilizes ASICs with low nanosecond and sub-nanosecond rise or fall times all PCB traces will exhibit transmission line behavior. From a systems point of view, knowing when to treat a trace as a transmission line is required. An in depth analysis of transmission line characteristics and modelling is beyond the scope of this thesis but can be found elsewhere [24-33].

A PCB trace or interconnection is treated as a transmission line if the time required for the signal to travel the length of the interconnect, one way propagation delay (τ), is 1/8th the signal rise (t_r) **or** fall (t_f) time (t_r/τ =8:1). In this case, the rise

or fall time is defined as the time required for a full amplitude (0% to 100%) swing. Analog circuits must strictly adhere to the transmission line definition. Since digital logic circuits are more tolerant of transmission line effects than analog circuits a conservative rise time to one way propagation delay (t_r/τ) of four is used. In the frequency domain, an interconnect is treated as a transmission line if the length of the interconnect is greater than 1/15th (1/8th for digital circuits) of the wavelength of the maximum frequency (f_{max}) present in the signal [34]. The maximum frequency (f_{max}) present in a signal is defined in is defined in Equation 4.1.

$$f_{max} = \frac{0.56}{t_r} \tag{4.1}$$

Table 4.1 illustrates the rise and fall times of the logic families utilized on the tester, and the maximum length a trace or interconnect can be treated as a lumped element.

Table 4.1: Rise and Fall times and critical trace lengths

Logic Family	Nominal t_r or t_f (10% - 90%) (ps)	Nominal t_r or t_f (0% - 100%) (ps)	Maximum Trace Length (in)
Gigabit [22]	150	188	0.35
Motorola ECLiPS [38]	450	563	1.0
National 100K ECL [37]	750	934	1.7
IDT ECL [35]	1000	1250	2.3

Although there are many types of transmission line structures the two most popular are microstrip and stripline and are illustrated in Figure 4.1.

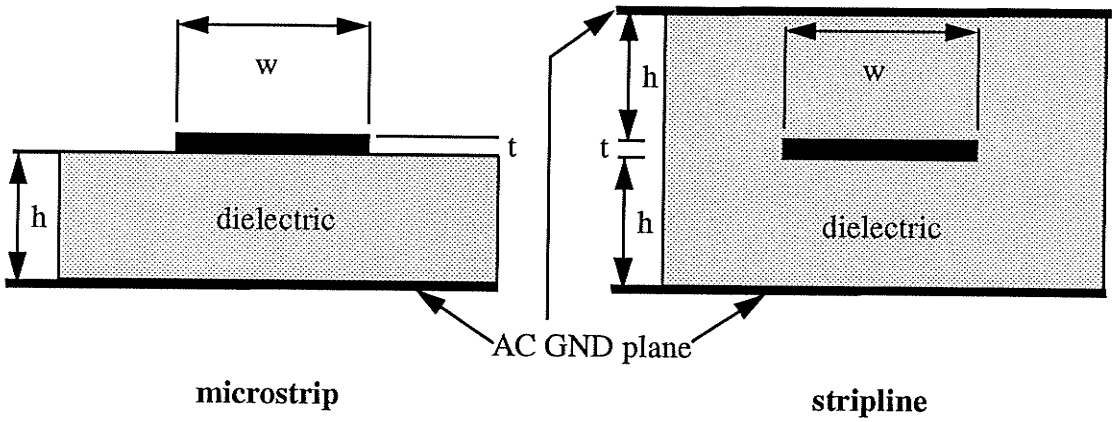

Figure 4.1: Microstrip and stripline transmission line structures.

Ideally, stripline would have been the transmission line of choice (see Recommendations) because of lower crosstalk characteristics due to the true TEM waveform. Also, stripline has better impedance control over microstrip since stripline is buried and will not be affected by the plating process or solder mask. Plating is a process of chemically or electrochemically depositing metal on a surface. This process is used to deposit the metal needed to form the via walls. Consequently, this metal deposition may also add to an interconnects trace copper thickness traces (t) on outer layers. Solder mask, which is a non-conductive coating applied over bare copper or copper traces to prevent short circuits during the soldering process, alters the dielectric constant of the substrate. Both these processes will have an affect on a microstrip's characteristic impedance (Z_0).

Nevertheless, microstrip was chosen primarily because of the previously mentioned goal of limiting the PCB to six layers (Chapter three) and lower propagation delay. Also, using stripline would complicate routing and also require the use of layers reserved for power planes. This would split the power planes and would limit the planes effectiveness (higher inductance & higher resistance). Also, the striplines would have to utilize DC power planes instead of system ground as an AC ground (GND) planes. Using DC power planes as AC ground (GND) planes is possible if a thorough

noise analysis is carried out proving that the power supply noise will not feedthrough and exceed the driving or receiving gate's noise margins.

A microstrip transmission line impedance (Z_0) formula, which is found in the Motorola MECL System Design Handbook [36] and many other high speed digital logic data books [37-38], is illustrated in Equation 4.2.

$$Z_O = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right) \tag{4.2}$$

Where:

ε_r = relative dielectric constant of the substrate.

w = width of signal trace (see Figure 4.1)

t = thickness of signal trace (see Figure 4.1)

h = thickness of dielectrics (see Figure 4.1)

is accurate to within +/- 5% when:

$$0.1 < \frac{w}{h} < 2.0 \text{ and } 1 < \varepsilon_r < 15.$$

Edward's [30] or Wheeler's [28] microstrip equations are more precise than Equation 4.2. But, Wadell [24] states that Equation 4.2 can be used in place of Wheeler's equation **if** the w/h ratio restriction is followed and **only** for impedances of 50 Ω or greater.

The PCB manufacturer (Network Circuits) provided a substrate (prepeg or core) dielectric constant (ε_r) of 4.2 which is measured at 1 MHz [25,26,40]. Unfortunately, ε_r is frequency dependent and decreases with increasing frequency which in turn affects the impedance (Z_0). The dielectric constant (ε_r) ranges between 3.8 and 4.0 at frequencies at or near 1 GHz [40]. Since sub-nanosecond edge rates are utilized, the variation in the FR-4s dielectric constant (ε_r) should be taken into account. Transmission lines should then be designed at the corresponding F_{knee} frequency of the logic family driving the transmission line [40]. Any circuit or interconnect having a frequency response up to and including the F_{knee} frequency point will pass a digital sig-

nal practically undistorted [41]. The equation for F_{knee} is calculated as follows:

$$F_{knee} = \frac{0.5}{t_r} \tag{4.3}$$

Where:

t_r is the digital logic family's 10%-90% rise time.

Using F_{knee} = 1 GHz (ECL rise times), the appropriate dielectric constant to design the transmission lines would be $\varepsilon_r = 4.0$.

Even designing a transmission line at the proper ε_r will not guarantee a +/- 5% impedance specification. As mentioned previously, excess plating (increase t) and other manufacturing processes will affect the resulting impedance. A reputable PCB manufacturer, with a stable PCB process, will offer **controlled impedance** services which **guarantee** the requested impedance value with a +/- 5% tolerance. The PCB manufacturer will then vary *w*, *t* or *h* to fit their manufacturing process and achieve the required impedance. This is very difficult if more than one impedance value is required on the same layer. Controlled impedance services also comes with a hefty financial cost. The financial cost is due to the many iterations a PCB manufacturer may have to go through to create a controlled impedance and also the cost of testing the impedances. Unfortunately, Network Circuits does not offer controlled impedance services and the only method of predicting the possible impedance variation was to perform an impedance tolerance analysis.

4.1.1 Stackup and Impedance Control

The next step was to choose the appropriate microstrip impedances and trace widths and perform an impedance tolerance analysis. As mentioned previously, a dielectric constant (ε_r) value of 4.0 will be used to calculate the nominal track width and thickness for the desired nominal impedances. The high frequency lines (DUT

interface, HF clock distribution and CLOCK12 distribution) were chosen to be 50 Ω with a track width of twenty mils using 1/2 oz. copper (t = 0.7 mils). This track width provides low resistivity since some of the divide by twelve (CLOCK12) clock distribution are required to run up to eight inches. Therefore, DC losses would be kept to a minimum. Obviously, the pin driver to DUT (Device Under Test) interconnect is required to be 50 Ω, since all high speed DUT systems are 50 Ω systems. Also, the variable delay lines, which are used in the clock distribution and the DUT paths, require 50 Ω tracking since its input and output impedance is 50 Ω (+/- 10%).

The SRAM Data bus was chosen to be a bidirectional or multidrop bus and to utilize the minimum manufacturable trace width (8 mils) possible because of routing density requirements around the SRAM socket. Figure 4.2 illustrates the SRAM bidirectional Data bus, the gates tapped on the bus and the terminating resistors at both ends of the bus.

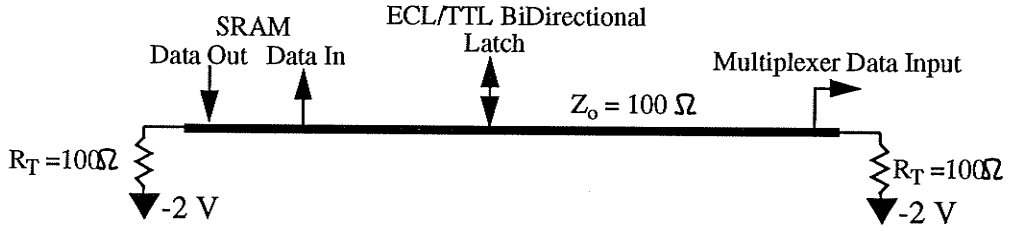

Figure 4.2: SRAM bidirectional Data bus.

The Data bus's characteristic impedance (Z_0) was chosen to be 100 Ω. Since it is a multidrop (multiple loads) bus, the bus driver (SRAM Data Out OR Latch) actually "sees" a 50 Ω impedance due to the 100 Ω bus and parallel 100 Ω resistors.

The SRAM Address bus was chosen to be 68 Ω and is illustrated in Figure 4.3. This impedance value allows the bus to be routed on both layer one and six with trace widths of twelve and sixteen mils respectively.

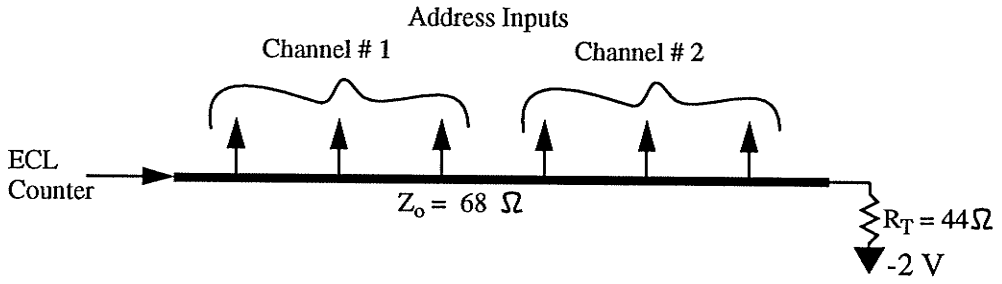

Figure 4.3: SRAM Address bus.

The remaining traces on the PCB were designed as 75 Ω. Table 4.2 illustrates the track description and layer location and Table 4.3 illustrates the physical parameters of the microstrip transmission lines.

Table 4.2: Nominal designed trace impedances and layer location

Bus or Track Description	Designed Z_o (Ω)	Layer
HF and HF/12 (CLOCK12) Clocks	50	1
HF Data Out	50	1
12 Bit Wide Data Bus (SRAM to 12:1 Mux)	100	6
12 Bit Wide Address Bus (SRAM)	68	1 & 6
ECL Select, Enable and Counter Section	75	1 & 6

Table 4.3: Microstrip parameters and layer location.

Signal Layer	Ground (A.C.) Layer	Nominal Impedance (Z_o) (Ω)	Nominal Trace Width (Mils) (w)	Nominal Dielectric Thickness (Mils) (h)
1	2	50	20	11
		68	12	
		75	10	
6	5	68	16	18
		75	18	
		100	8	

As Table 4.3 illustrates the dielectric thickness (**h**) of the two signal layers (1 and 6) are not identical and therefore the board stackup is not symmetrical. This occurs because an eight mil, 100 Ω trace is not realizable with the proposed dielectric thickness needed for signal layer one. Therefore, 100 Ω traces are routed only on layer six. Other trace impedance values, such as 68 Ω and 75 Ω are routed on both signal layers. This stackup unbalance will cause the board to experience warping. Nevertheless, since it is only a protoyping board and will not be inserted into any housings or cabinets potential warping will be disregarded. Figure 4.4 illustrates the stackup for the twelve by twelve inch six layer tester PCB. The power layers (layers 2-5), which utilize 1 oz. (0.0014 inches) copper, were spaced appropriately to achieve the standard 62.5 mils PCB thickness. The PCB artwork for the tester can be found in the Appendix.

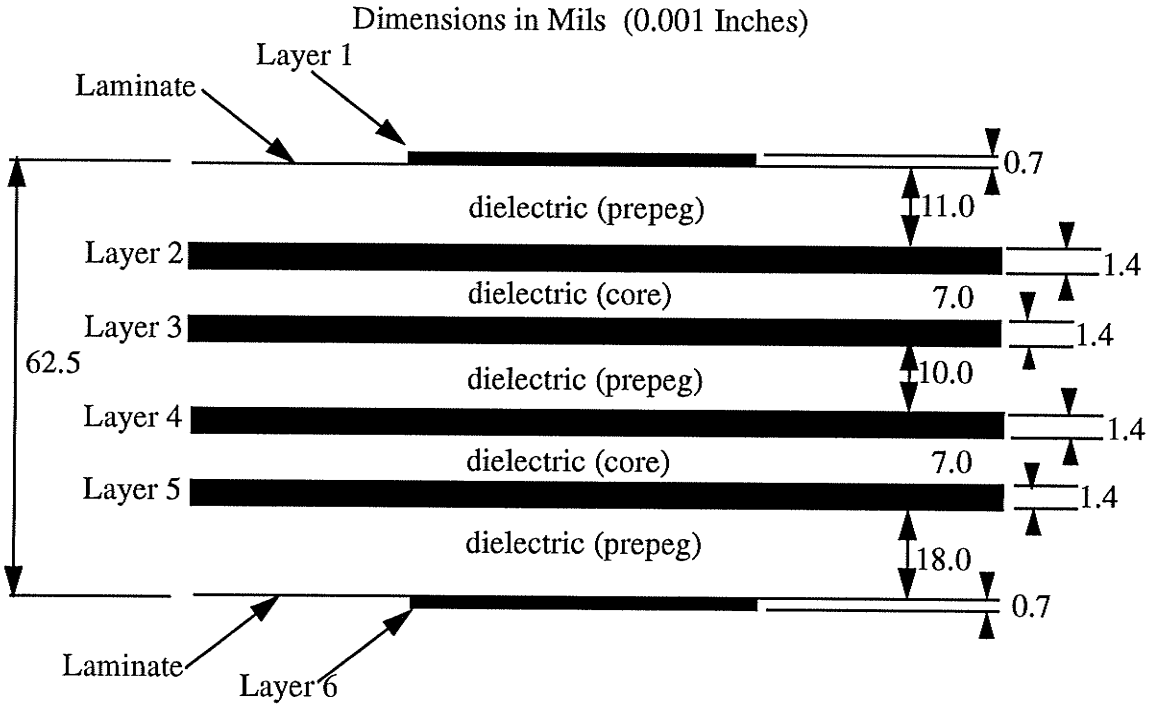

Figure 4.4: Tester PCB stackup

Once the desired trace impedances and physical parameters are chosen, an impedance tolerance analysis was performed to estimate the possible impedance variation due to manufacturing tolerances. Table 4.4 illustrates the manufacturer's tolerances of the trace width and thickness, dielectric thickness and the range of the substrate dielectric constant (ε_r).

Table 4.4: PCB tolerances. [39]

Parameter	Tolerances
Trace Width (**w**)	± 1.0 mils
Trace Thickness (1/2 oz.) (**t**)	0.7 ± 0.2 mils
Dielectric Thickness (**h**)	± 1.0 mils
Effective Dielectric Constant (ε_r)	3.8 - 4.2

Table 4.5 illustrates the resulting impedance variations and the measured

impedances of certain traces on the PCB.

Table 4.5: Calculated impedance variation and measured Z_o.

Calculated Z_o			Measured Z_o (Ω)
Min.(Ω)	Nom. (Ω)	Max. (Ω)	
45	50	58	62
61	68	78	79
66	75	85	84
93	100	112	106

The trace impedances were measured with a Tektronix dual-channel SD-24 twenty GHz sampling/TDR (Time Domain reflectometer) head which is a plug in unit for a Tektronix 11801A digital sampling oscilloscope (forty GHz). The TDR provides a 250 mV rising or falling (differential output) pulse with a 35 ps (20% - 80%) rise or fall time, which is effectively a ten GHz signal. TDR is similar to radar, the sampling/TDR head sends out a pulse (V_{inc}) and then measures the voltage reflected back (V_{refl}) to the head. The ratio of incident to reflected voltage at the sampling head determines the reflection coefficient ρ and is shown in Equation 4.4.

$$\rho = \frac{V_{refl}}{V_{inc}} \tag{4.4}$$

Equation 4.5 illustrates the relationship of ρ to the resulting impedance (Z) of the inter-connect under test.

$$Z = Z_{ref} \cdot \frac{1+\rho}{1+\rho} \tag{4.5}$$

Where Z_{ref} is 50 Ω (system impedance) and ρ is the reflection coefficient. The spatial resolution of the TDR is illustrated below.

$$\Delta x = \frac{c \cdot t_r}{2 \cdot \sqrt{\varepsilon_{eff}}} = \frac{(3 \cdot 10^8) \cdot (35 \cdot 10^{-12})}{2 \cdot \sqrt{2.49}} = 130 mils \tag{4.6}$$

Where:

c is the speed of light

t_r is the (10%-90%) rise time of the TDR pulse

ε_{eff} is the effective dielectric constant of the transmission line.

The SD-24 TDR head can distinguish impedance discontinuities which are 130 mils apart. This point will be discussed later when measuring the impedances of the multi-drop busses.

The impedance control, as shown in Table 4.5, was terrible and impedance values were skewed toward the high end of the tolerance scale, where the dielectric constant value is 3.8. Since, a wide bandwidth TDR was used for impedance measurements it is expected that ε_r will be lower and therefore the impedance value would be increased. Unfortunately, it also appears that the dielectric thicknesses for the signal layers were larger than requested. This error in dielectric thickness would produce larger than expected impedance values.

Since microstrip has an air-dielectric interface an effective dielectric constant (ε_{eff}) is used to model this interface. A simple method of verifying the effective dielectric constant (ε_{eff}) is to measure the propagation velocity of a test trace. Equation 4.7 illustrates the relation, where c is the velocity of light (11.8 in/ns) and v is the propagation velocity of a test trace.

$$\varepsilon_{eff} = \left(\frac{c}{v}\right)^2 \tag{4.7}$$

The effective relative dielectric constant (ε_{eff}) is defined in terms of the relative dielectric constant (ε_r) as follows [36-38]:

$$\varepsilon_{eff} = 0.475 \cdot \varepsilon_r + 0.67 \tag{4.8}$$

The propagation delay of a "designed" 75 Ω 7.732 inch long trace was mea-

sured using the TDT (Time Domain Transmission) capability of the SD-24 TDR/sampling head. The propagation delay of the trace was measured to be 1.034 ns. The resulting propagation velocity is then 7.477 ns/inch and the effective dielectric constant (ε_{eff}) is 2.49. The dielectric constant (ε_r) of the PCB material is then 3.8, which is much lower than the quoted 4.2. The TDT measurement utilizes the same pulse (35 ps) as previously mentioned TDR/sampling head. Since the TDR pulse is a wide bandwidth pulse (10 GHz) the resulting ε_r illustrates the laminates frequency dependence.

4.1.2 Transmission Line Loading and Terminations

Once the trace impedances have been measured, the distributed per unit length transmission line elements, such as the intrinsic capacitance (C_0), instrinsic inductance (L_0) and can be calculated. The distributed per unit length transmission line parameters are defined in the following equations:

$$C_O = \frac{\sqrt{\varepsilon_{eff}}}{Z_O \cdot c} = \frac{T_{PD}}{Z_o} \tag{4.9}$$

$$L_O = \frac{Z_O \cdot \sqrt{\varepsilon_{eff}}}{c} = T_{PD} \cdot Z_o \tag{4.10}$$

$$Z_O = \sqrt{\frac{L_O}{C_O}} \tag{4.11}$$

$$T_{PD} = \sqrt{L_O \cdot C_O} \tag{4.12}$$

Where:

C_o = pF per inch

L_o = μH per inch

c = velocity of light

ε_{eff} = effective dielectric constant

T_{PD} = trace propagation delay, ps per inch

Table 4.6 illustrates the distributed parameters for various trace impedances utilizing a dielectric constant of (ε_r) 4.0. The resulting propagation delay (T_{PD}) is 136 ps/inch.

Table 4.6: FR-4 (ε_r =4.0) microstrip Intrinsic parameters

Z_0 (Ω)	C_0 (pf /inch)	L_0 (μH / inch)
50	2.70	0.0069
62	2.19	0.0084
68	2.00	0.0092
75	1.81	0.0102
79	1.72	0.0108
84	1.62	0.0114
100	1.36	0.0136
106	1.28	0.0145

To prevent ringing or reflections on a transmission line proper termination is required. Two types of terminations which are popular with ECL or GaAs systems are parallel and series terminations and are shown in Figure 4.5.

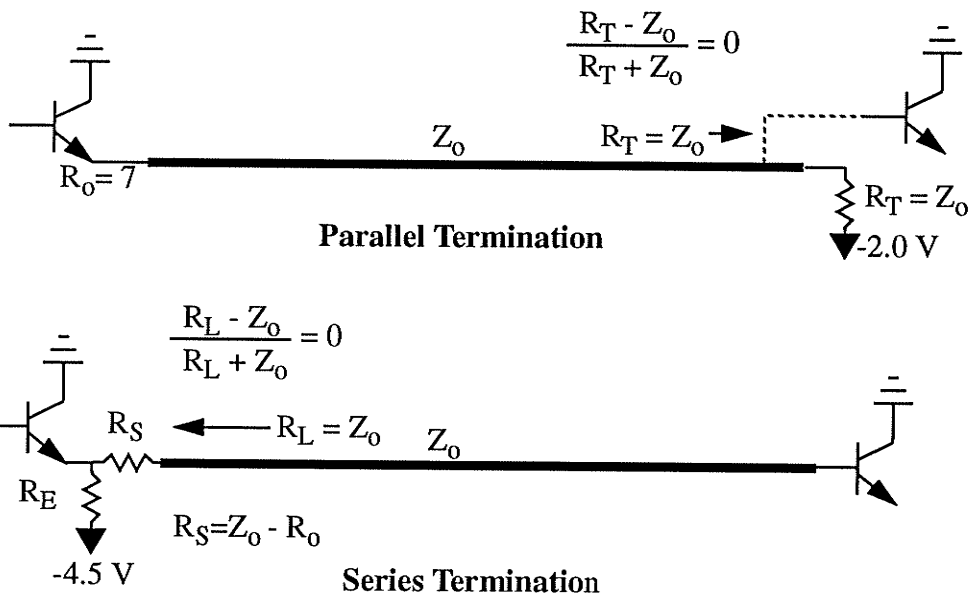

Figure 4.5: Parallel and series termination schemes.

Parallel termination is the preferred scheme and involves terminating the end of a line with a SMT resistor (R_T) which has a value of the transmission line characteristic impedance (Z_o) and is connected to a -2.0 V biasing supply. No reflections will occur if there is a proper match. The output impedance (R_o) of ECL and GaAs output buffers is very low, nominally 7 Ω for ECL and 10 Ω for GaAs, which is virtually a short circuit. Any reflections returning back to the driving gate would be almost reflected back ($\rho \approx -1$) to the receiving gate and cause ringing on the line.

Series termination is a technique which places the termination resistor between the driving gate and the transmission line. The terminating resistor (R_S) and the output impedance (R_o) equals the line characteristic impedance (Z_o). The value of a bias resistor (R_E) determines the quiescent V_{OH} and V_{OL} levels. The signal travels down the transmission line at half amplitude because of the voltage divider at the driving end. The receiving gate(s) can be modelled as a high impedance ($>> Z_o$) capacitive input. Therefore, as the signal hits the end of the line it doubles ($\rho \approx 1$) (see) and travels toward the driving gate. Once the returning signal reaches the driving end it will be

absorbed by the combination of the series resistor (R_S) and the ECL gates output impedance (R_o) which equal the line's characteristic impedance (Z_o). Hence, no further reflections will occur. One of the advantages of series over parallel termination is in terms of crosstalk. Since only half the wave goes down the line it would impose smaller crosstalk on an adjacent victim line.

Figure 4.5 illustrated the terminating scheme of a point-to-point transmission line. That is, there are no loads along the line but only at the terminus of the line. Unfortunately, the SRAM Address and Data buses are multidrop and contain many capacitive loads (gate inputs) distributed along the line. A typical input capacitance for an ECL or BiCMOS gate is 3 pF and a typical socket capacitance is 1 pF, for a total per gate capacitance of 4 pF. For example, the SRAM Address bus has six (6) loads evenly distributed along the transmission line. Terminating the bus with the bus's characteristic impedance is not sufficient to prevent reflections.

The capacitive loads effectively lower the bus impedance, which was designed at 68 Ω but measured at 79 Ω, and increases the propagation delay. The distributed capacitance (C_D) due to the loads is illustrated in Equation 4.13. C_L is the load capacitance (6 loads* 4pF = 24 pF) and l (5.990 inches) is the length of bus where the loads (gates) are connected.

$$C_D = \frac{C_L}{l} = \frac{24\text{pF}}{5.990} = 4.01\text{pF/inch} \tag{4.13}$$

The change in impedance (Z_o') and increase in propagation (T_{PD}') due to the stray capacitance are as follows:

$$Z_o' = \frac{Z_o}{\sqrt{1 + C_D/C_O}} \tag{4.14}$$

$$T_{PD}' = T_{PD} \cdot \sqrt{1 + C_D/(L_O \cdot C_O)} \tag{4.15}$$

The resulting change in the address bus's impedance and increase in propagation delay is illustrated in Equation 4.16 and Equation 4.17 respectively.

$$43\Omega = Z_o' = \frac{79\Omega}{\sqrt{1+\frac{4.01}{1.72}}} \tag{4.16}$$

$$248\text{ps/inch} = T_{PD}' = 136 \cdot \sqrt{1+\frac{4.01}{1.72}} \tag{4.17}$$

The bus must then be terminated with a 43 Ω SMT resistor to properly match the line impedance and prevent reflections.

Figure 4.6 illustrates the TDR setup to measure the line impedance of one ($\overline{A}_1$ bit) line of the Address bus, which is parallely terminated (R_T). The SRAM sockets (6) were soldered onto the PCB and SMT capacitors (3.3 pF) were soldered between each (6) SRAM's through-hole (socket pin) via and a nearby ground via to mimic the input capacitance to ground of the SRAM Address gate input ($\cong 3pF$). A 39 Ω 0805 SMT resistor was used to terminate the line.

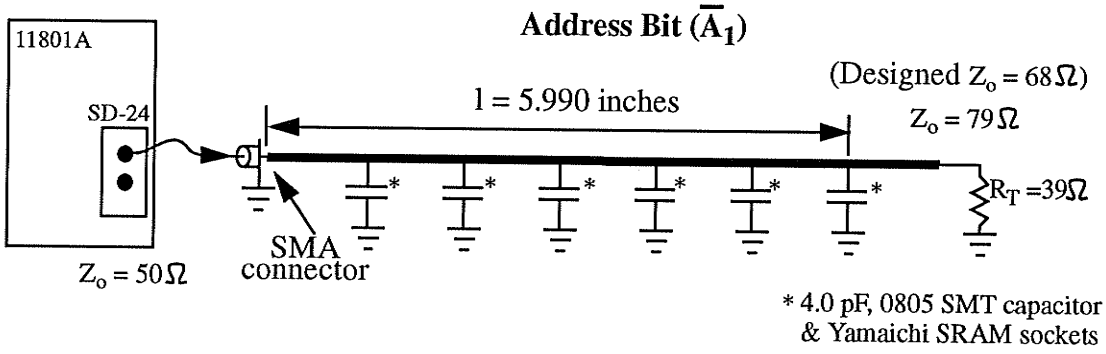

Figure 4.6: Address ($\overline{A}_1$) bus TDR setup.

As mentioned previously, a TDR unit measures the impedance of a DUT or a transmission line by utilizing Equation 4.4 and Equation 4.5. Unfortunately, these equations are not accurate if there are many discontinuities along the line because the discontinuities will cause multiple reflections and hence errors in the impedance values.

These errors were evident when measuring the impedance of the Address and Data buses. Figure 4.7 illustrates the TDR impedance measurements of an unterminated and unloaded (no mimic caps) Address ($\overline{A}_1$ bit) bus line. The capacitance to ground of the vias (6) and the SMA connector signal pin driving the line create large discontinuities. The first "dip" is due to the capacitance to ground of the SMA connector signal pin (25 Ω). The first "spike" is the impedance of the transmission line from the SMA connector to the first via (trace length ~ 1.1 inches). As the pulse moves down the line the via impedance value increases (smaller "dips") and the transmission line impedance between vias decreases. These results are somewhat erroneous and are caused by multiple reflections and also due to the decrease in the pulse rise time and hence the spatial resolution (see Equation 4.6). Tektronix has developed a DSP software package called Z-Profile to remove errors caused by multiple reflections [42]. Figure 4.8 illustrates the TDR trace of a loaded (SMT capacitors and SRAM sockets) and unterminated $\overline{A}_1$ line. The impedance of the line is decreased to below 40 Ω. This illustrates the decrease in impedance caused by the distributed capacitive loads. A 39 Ω to 44 Ω SMT resistor should be adequate to properly terminate the line. For the TDR experiments a 39 Ω 0805 SMT resistor was used due to availability.

As was discussed previously, the TDR head provides a pulse with a very fast rise time (35 ps). Consequently, the TDR rise time does not resemble the actual rise time (nominal 750 ps) of the ECL counter driving the address bus. It would be more realistic to investigate the discontinuities caused by the loads with a pulse with a 750 ps rise time. The Tektronix 11801A DSO [43] provides a *Filter* option that allows any trace (pulse rise time) to be filtered. That is, the trace will have a rise time (bandwidth specification) applied to it via DSP algorithms. Therefore, the TDR pulse trace (waveform) can have a 750 ps filter applied on it to approximate the nominal rise time (10-90%) of the ECL counter driving the address bus. Figure 4.9 illustrates the resulting TDR traces for a loaded, terminated address ($\overline{A}_1$) line for various input rise times

including the actual TDR pulse rise time (35 ps). The discontinuities decrease dramatically as the rise time is increased. For a 1.0 ns rise time, the discontinuities along the line are small but also indicates a resistor value larger than 39 Ω is required to properly terminate the line.

Figure 4.10 illustrates the voltage waveforms at the address line's terminating resistor. A Tektronix SD-14 high impedance probe sampler, plug in unit for the 11801A, was used to take the measurements. The probe has a bandwidth of 3 GHz and a capacitance of < 0.5 pF. The waveform in Figure 4.10 exhibits slight ringing with an overshoot and undershoot voltage of approximately 20 mV. This is caused by a mistermination (39 Ω) and a slight "tweaking" of the resistor termination (R_T) value will reduce the ringing.

A similar TDR setup, shown in Figure 4.11, was used to measure the impedance of one (Channel #1, D_{11}) line of the SRAM Data bus. Similar to the Address bus, "mimicing" capacitors and IC sockets were soldered on to the appropriate socket footprints. The resulting TDR waveforms for a loaded and terminated line for various input rise times is illustrated in Figure 4.12. The impedance mismatch due to the SMA connector is very large but the remaining sections of the line exhibit small impedance variations. Figure 4.13 shows the voltage waveform at the Data bus's terminating resistor (R_{T2}) located nearest the GaAs multiplexer. There is an overshoot and undershoot of 30 mV. As stated previously, tweaking of resistor values will minimize the ringing that have been ulcerated previously.

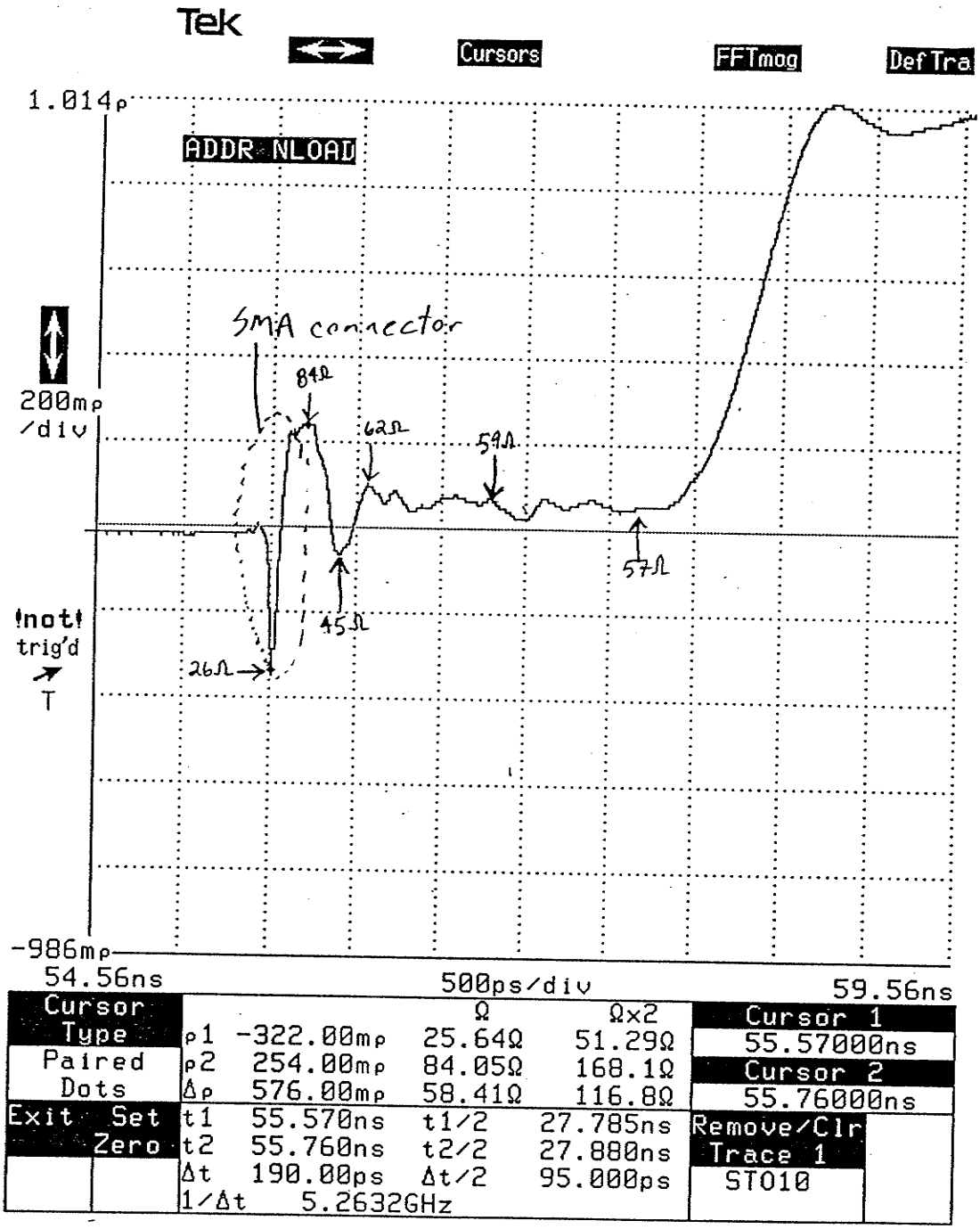

Figure 4.7: TDR trace of an unterminated and unloaded Address bus ($\overline{A}_1$) line.

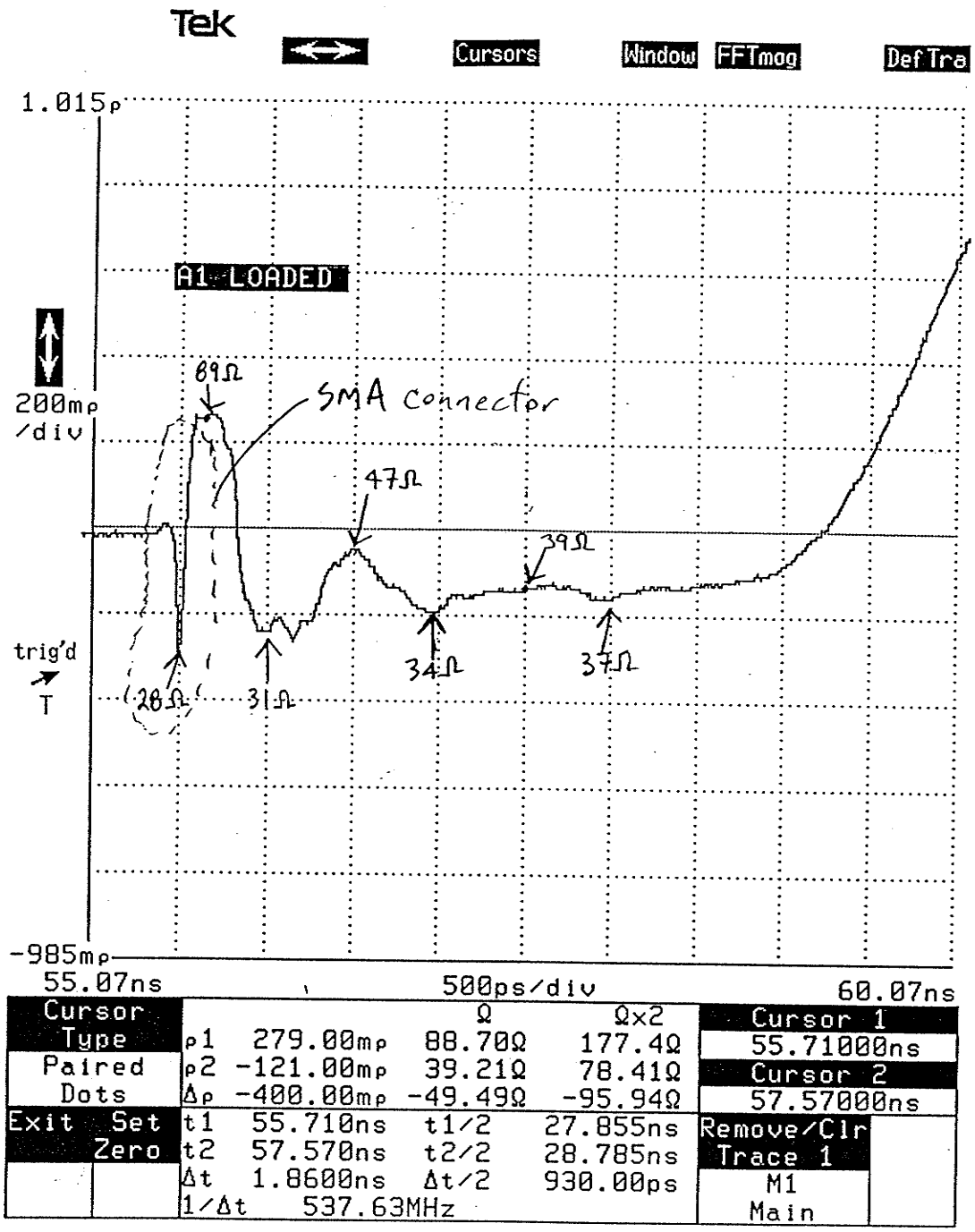

Figure 4.8: TDR trace of an unterminated and loaded Address bus ($\overline{A}_1$) line.

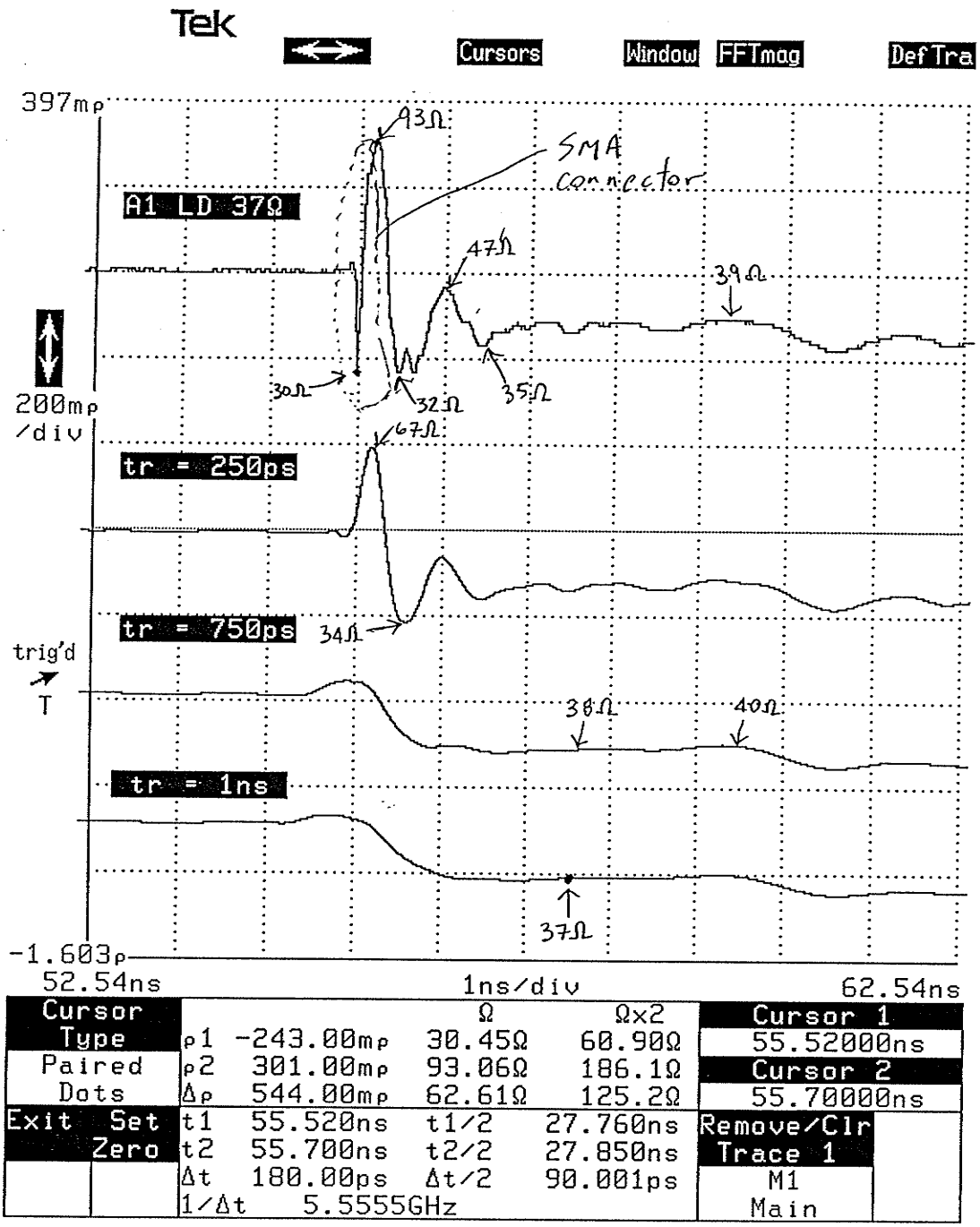

Figure 4.9: TDR trace of a terminated and loaded Address bus ($\overline{A}_1$) line for various input rise times.

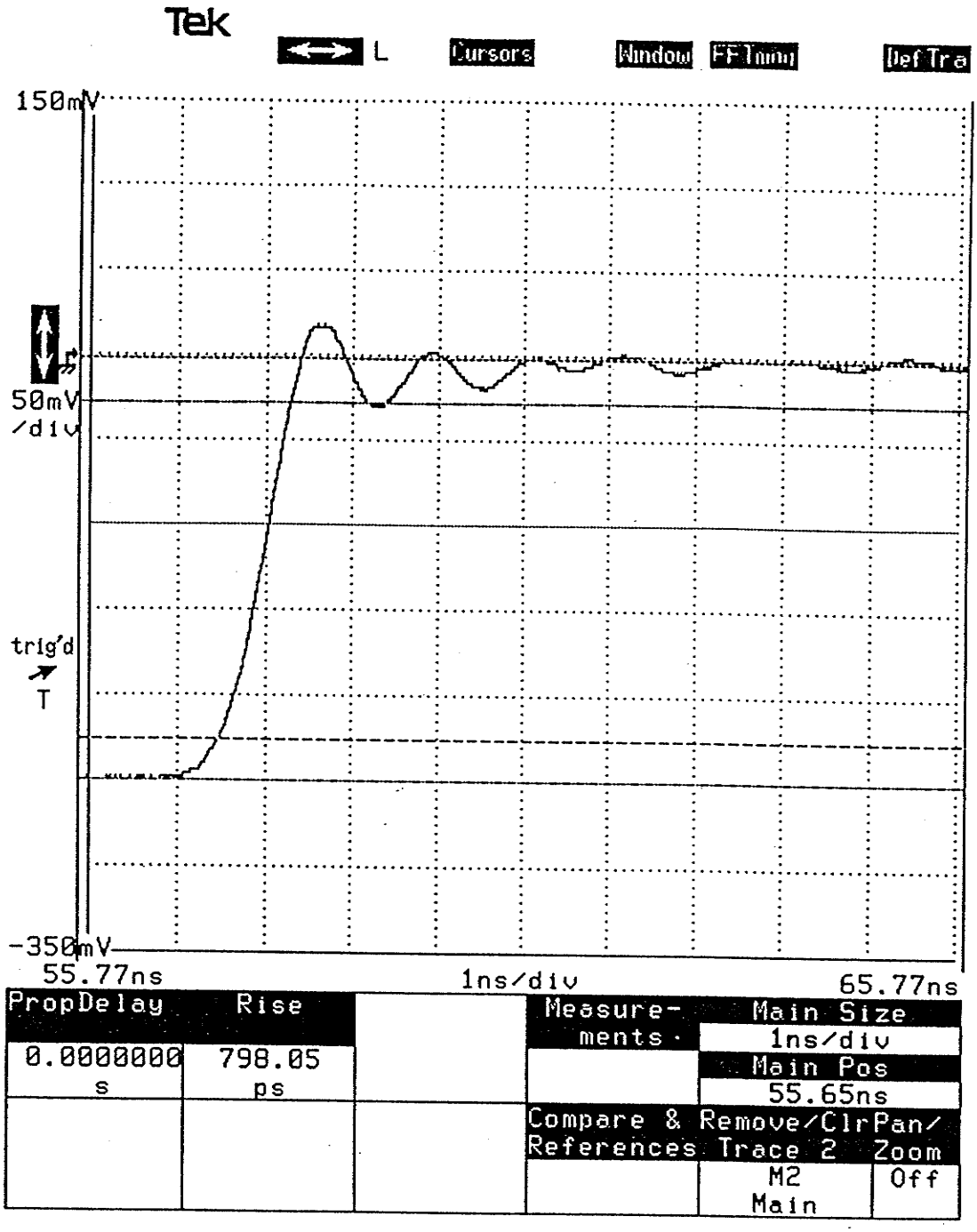

Figure 4.10: Voltage waveform at the terminating resistor (R_T) of a loaded Address bus ($\overline{A}_1$) line.

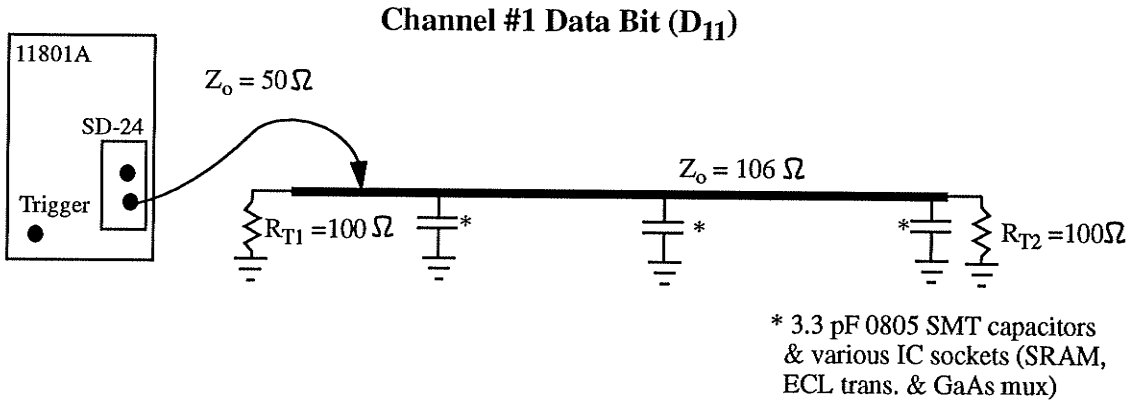

Figure 4.11: TDR setup of a Data (Channel #1, D_{11}) bus line.

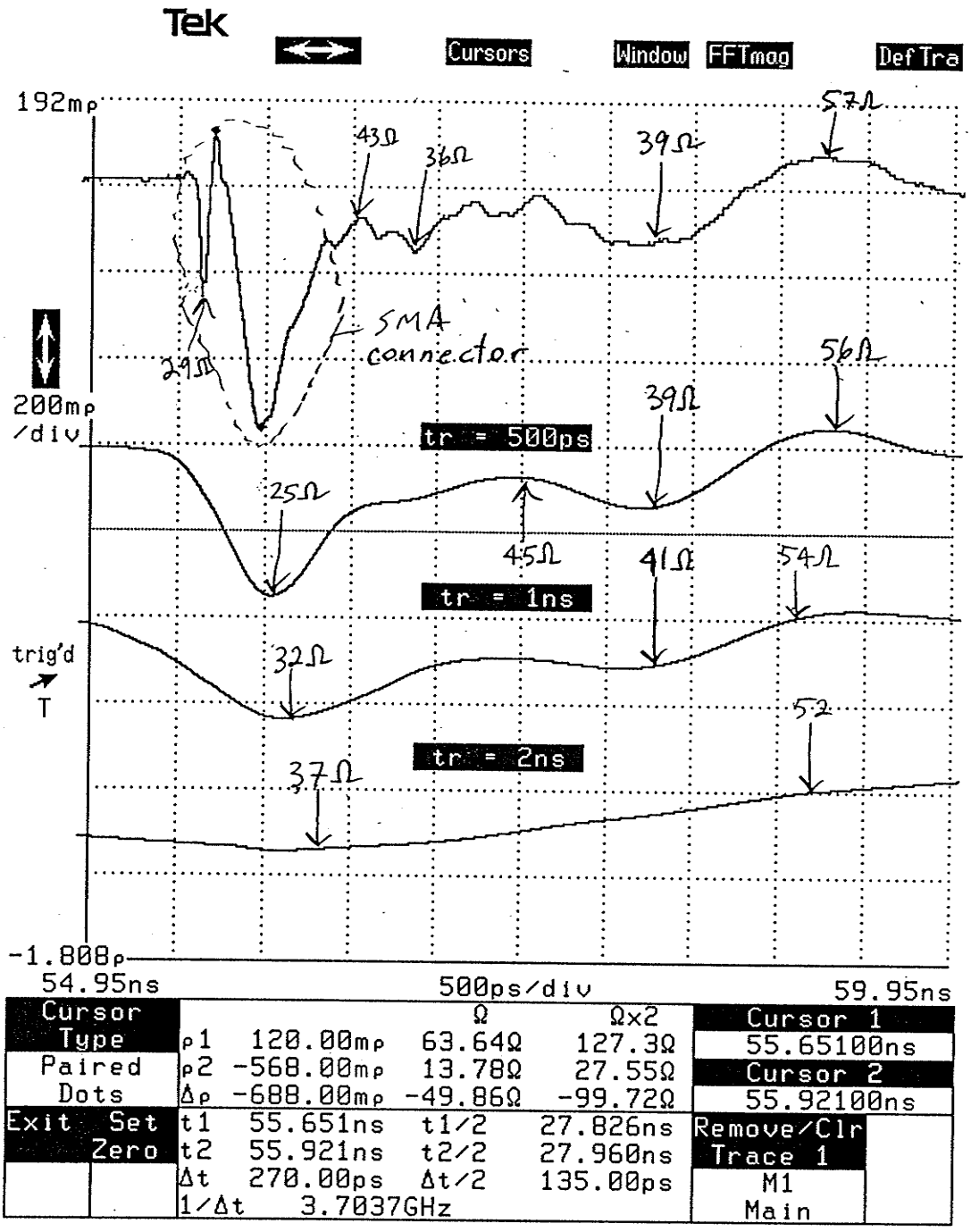

Figure 4.12: TDR trace of a loaded and terminated (Ch #1, D_{11}) Data bus line for various input rise times.

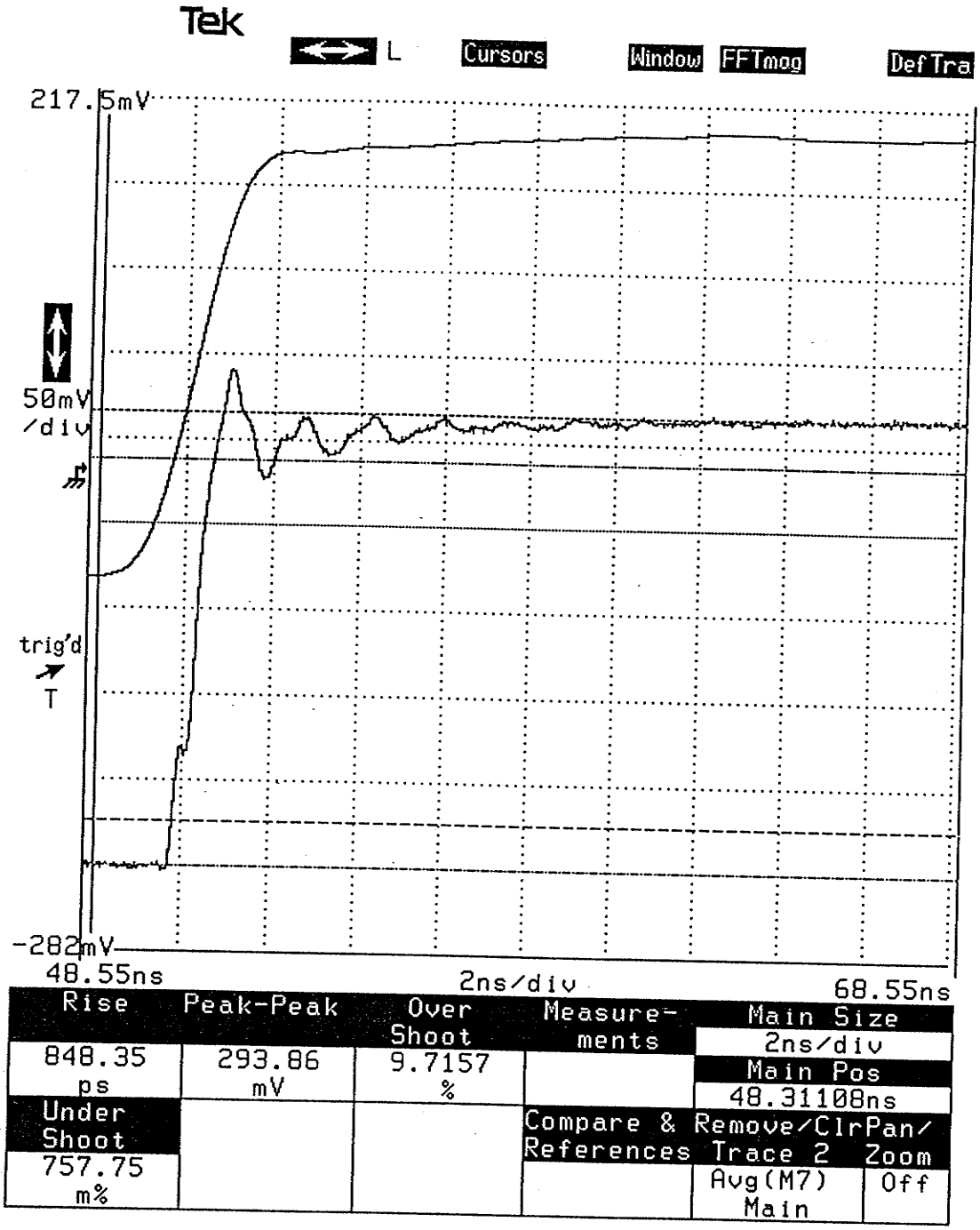

Figure 4.13: Voltage waveform at the terminating resistor (R_{T2}) of a Data (Ch #1, D_{11}) bus line.

4.1.3 Vias

Vias (plated through holes) in multilayer PCBs will have a capacitance to ground and because of their small sizes can be modeled as a lumped circuit element [41]. The capacitance is dependent on the ground clearance around a via, the diameter of the pad surrounding the via and the thickness of the PCB. Figure 4.14 illustrates the physical parameters of a via and Equation 4.18 illustrates a simple formula to estimate, to within an order of magnitude, the via capacitance to ground.

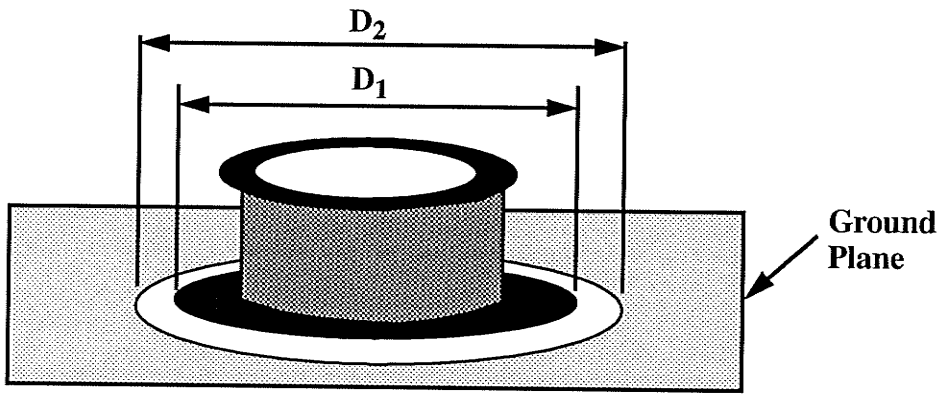

Figure 4.14: PCB via (PTH) physical parameters.

$$C_{via} = \frac{1.41 \cdot \varepsilon_r \cdot T \cdot D_1}{D_2 - D_1} \tag{4.18}$$

Where:

D_2 = diameter of clearance in ground plane(s) (inches).

D_1 = diameter of pad surrounding via (inches).

T = thickness of printed circuit board (inches).

ε_r = relative dielectric constant of circuit board material

C_{via} = parasitic via capacitance, pF.

All the high frequency data outputs (1.2 Gb/s) and clock inputs (1.2 GHz) utilize SMA

connectors for interface purposes. Unfortunately, the ground clearance (D_2) around the SMA signal pin via was not large enough and resulting capacitance to ground (C_{via}) is too large. The calculated and the measured SMA signal pin via capacitance to ground was 1.2 pF and 0.8 pF respectively. Since the via is a lumped element its impedance will vary with the signal rise time driving the via. The discontinuity is shown in Figure 4.15 for various input rise times (35, 100, 150 or 200 ps 10%-90% rise times). Even a pulse with a 200 ps rise exhibits a large discontinuity (40 Ω). The discontinuity will cause large reflections and ringing on the high speed data outputs and high frequency clock input lines. The resulting high speed data output waveforms would be almost useless for testing purposes.

The solution was to enlargen the (D_2) ground clearance by drilling out the SMA signal pin via. The SMA connector was then resoldered to the board and a short piece of wirewrap wire was soldered between the SMA signal pin and the disconnected PCB trace. The discontinuity was decreased dramatically (46 Ω) as illustrated in Figure 4.16. There is still a slight mismatch but the expected ringing will be tolerable as system verification proved later on (chapter five).

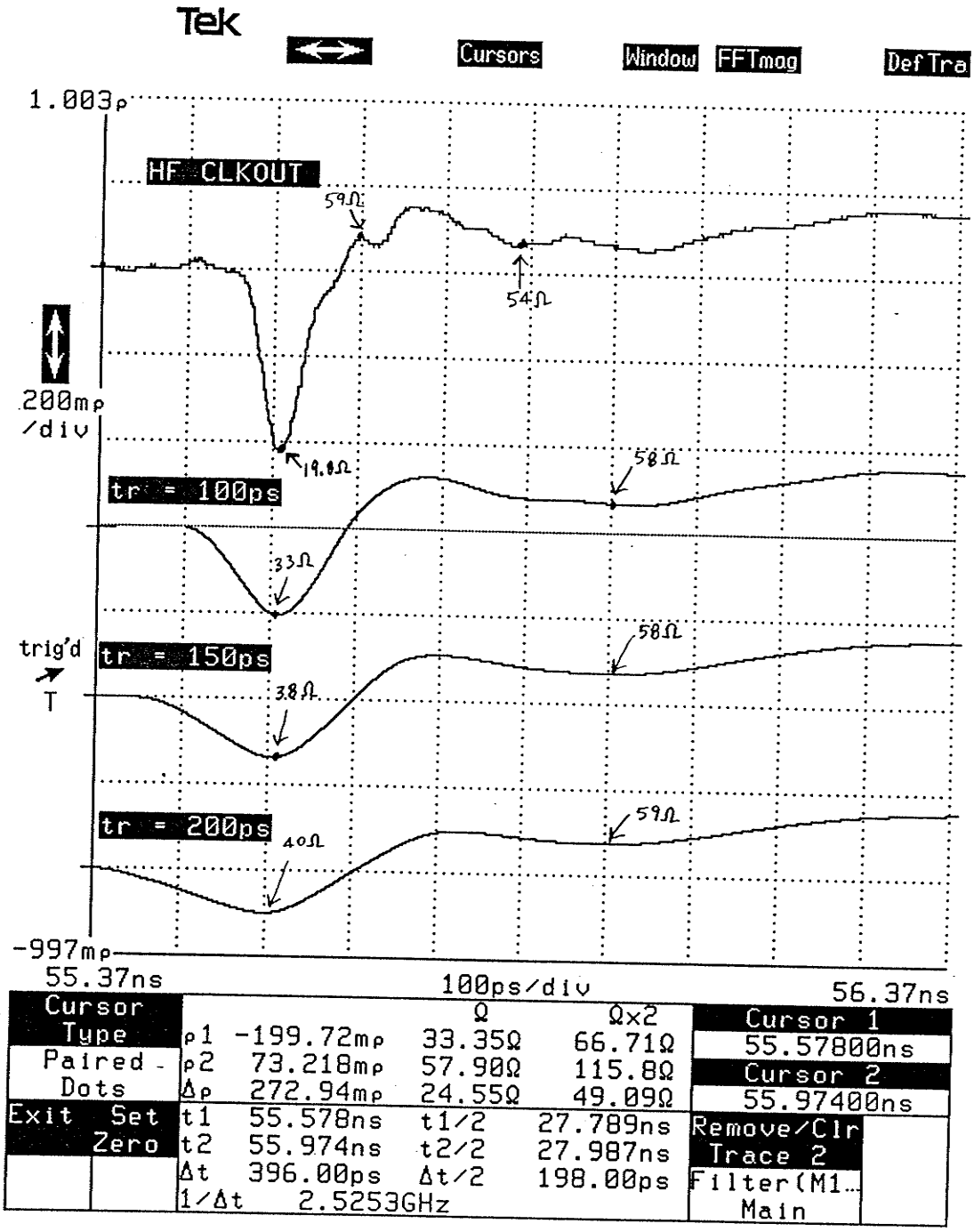

Figure 4.15: SMA signal via discontinuity for various (t_r) rise times (10%-90%).

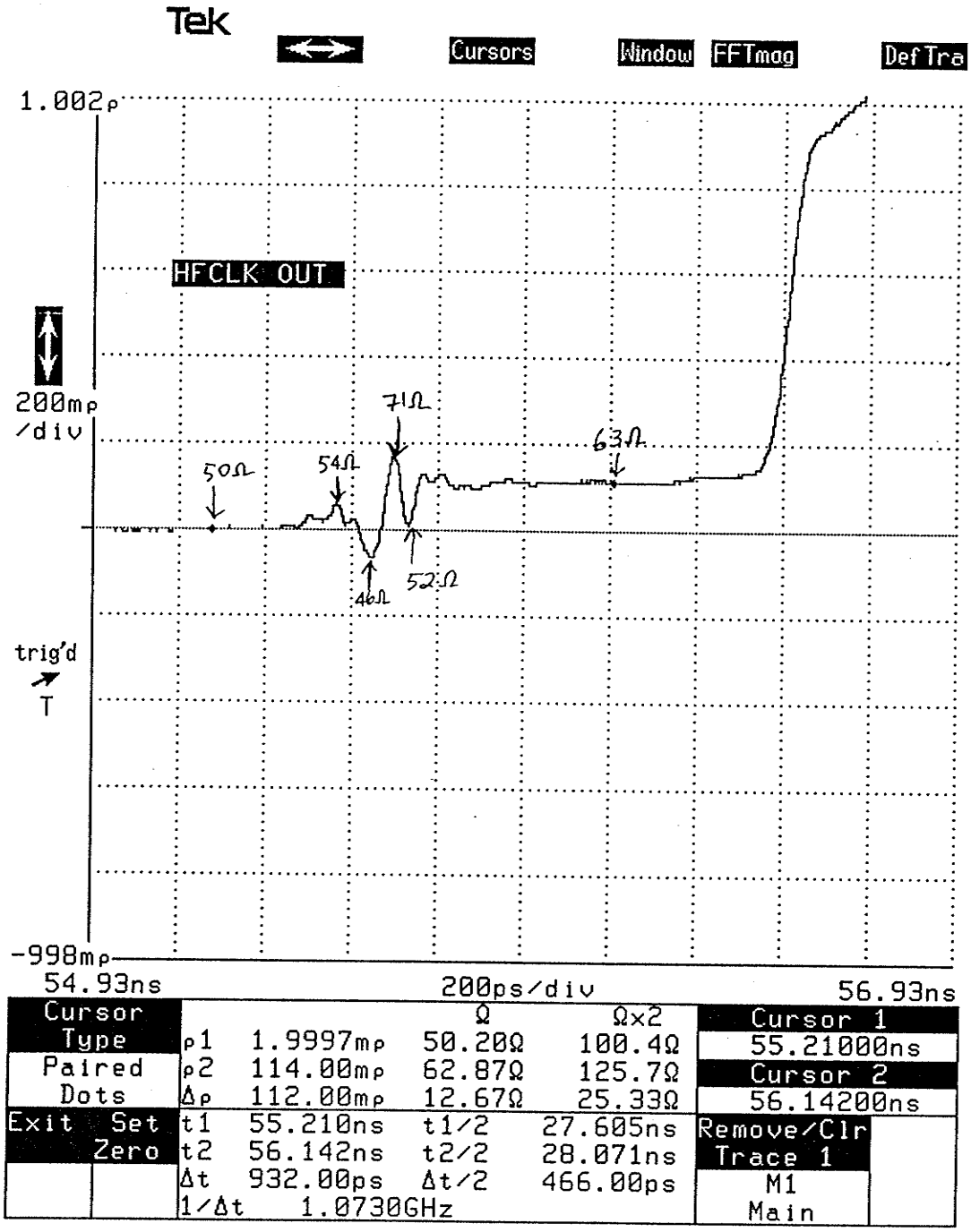

Figure 4.16: SMA signal via discontinuity after "fixup".

4.2 Crosstalk

Crosstalk is the capacitive and inductive coupling between a nearby or adjacent PCB, IC package or socket pin interconnect. This coupling induces (inductive) currents and (capacitive) voltages and a system can become non-functional if the induced voltage exceeds the noise margin of any logic gate connected to the "victim" trace. The discussion of crosstalk models and calculation of crosstalk coupling coefficients is beyond the scope of this thesis but can be found elsewhere [44-47]. From a system's perspective, an estimation of the worst case crosstalk is required. Experimental methods, which will duplicate actual system performance, will be used to estimate the worst case crosstalk. Crosstalk evident on the tester PCB is due to a combination of the following:

1) adjacent transmission lines

2) adjacent IC socket pins

3) adjacent IC package pins

Experimentally, only the crosstalk caused by the combination of adjacent transmission lines and IC socket pins will be presented. The crosstalk due to IC packaging will be estimated and added to the measured crosstalk contributed by the transmission line and the socket.

Transmission line crosstalk is categorized as near or far end as illustrated in Figure 4.17. Near end is the resulting crosstalk voltage on a victim line near the driver position and far end is the crosstalk voltage at the end of the victim transmission line. Crosstalk is always greater in microstrip than in stripline transmission lines because of the non-homogeneous air-dielectric interface.

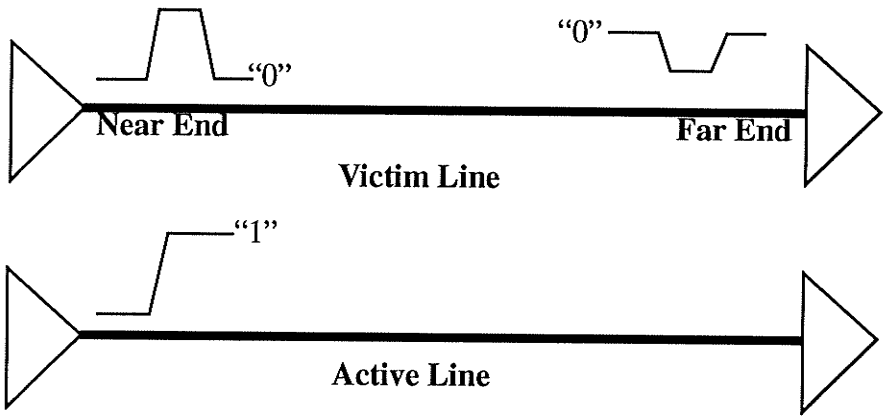

Figure 4.17: Near and far end crosstalk.

Also, near end crosstalk is always greater than far end crosstalk in microstrip than strip-line transmission lines. Crosstalk (coupling coefficients) is dependent on the following:

1) edge to edge spacing (w) of adjacent traces.

2) dielectric constant (ε_r) of the substrate.

3) dielectric thickness (h).

4) rise or fall time of driving pulse.

5) length of parallel transmission lines.

6) transmission line termination conditions (near and far end).

Figure 4.18 illustrates the physical parameters of adjacent microstrip transmission lines.

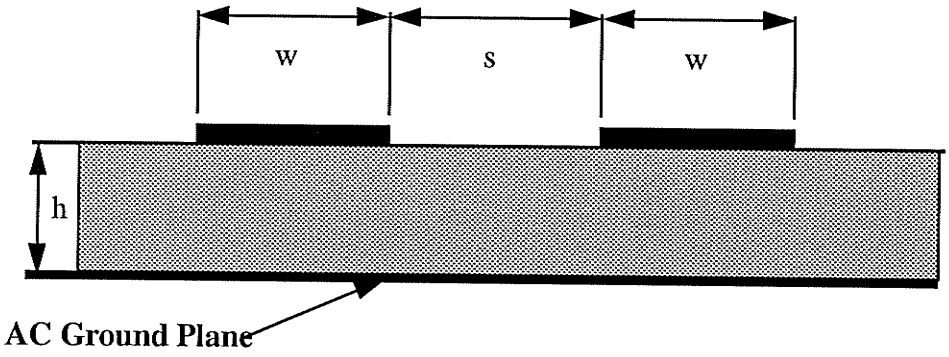

Figure 4.18: Crosstalk physical parameters of adjacent microstrip lines.

Lower impedance transmission lines have lower crosstalk characteristics than higher

impedance lines. This is due to the thinner dielectric (h is smaller) and hence the greater coupling to the ground plane than to the adjacent trace.

The tester's SRAM Data and Address busses have traces that run parallel for approximately four and six inches respectively. The Address bus layout was constrained by the spacing of the SRAM socket footprint, which has a fifty mils pitch. Every effort was made to maximize the edge to edge spacing(s) between address bus bits. As mentioned previously, the counter's complimentary outputs are used to drive the Address bus. The worst case edge to edge spacing occurs between Address bits $\overline{A}_3$, $\overline{A}_4$ and $\overline{A}_5$ and is 38 mils. Address bits $\overline{A}_2$ and $\overline{A}_6$ (> 100 mils edge to edge spacing) are sufficiently far away that they can be ignored. Also, as with the TDR measurements, SMT capacitors were placed on all signal pins along the bus to "mimic" the input capacitance of the SRAM address gates.

The situations when the worst case crosstalk occurs on the Address bus is when the tester is in *continuous* (looping) mode (chapter two) and switches from $\overline{A}_{11}$-$\overline{A}_0$ = *11111111111* to $\overline{A}_{11}$-$\overline{A}_0$ = *XXXXXX000XXX* (*X* =don't care state) or when $\overline{A}_{11}$-$\overline{A}_0$ = *XXXXX0111111* switches to $\overline{A}_{11}$-$\overline{A}_0$ = *XXXXX1000000*. Hence, the three Address bits ($\overline{A}_5$-$\overline{A}_3$) of interest switch from high to low. As Address bits $\overline{A}_3$ and $\overline{A}_5$ switch (high to low) they will couple onto $\overline{A}_4$, which is also switching high to low. The expected near and far end crosstalk waveforms coupled onto $\overline{A}_4$ are shown in Figure 4.19. These waveforms would be added (subtracted) to the falling edge of the pulse on $\overline{A}_4$. The near and far end crosstalk waveforms shown in Figure 4.19 occur only when both the near and far end terminations match the impedance of the transmission line. This situation will never occur with ECL logic if a parallel termination scheme is utilized.

As mentioned previously, near and far end crosstalk is a function of line terminations. The output impedance of an ECL or GaAs gate is nominally low (~7 Ω). This causes the near end crosstalk (see Figure 4.19) to reflect off the ECL ($\overline{A}_4$) gate driving the line ($\rho \approx -1$), invert and then propagate toward the far end of the victim line. The

near end crosstalk becomes far end crosstalk and combines with the original far end crosstalk waveform. Experimentally, to approximate the low output impedance of an ECL gate the near end termination of Address bit $\overline{A}_4$ will be shorted to ground as shown in Figure 4.20. Figure 4.21 illustrates the expected near and far end crosstalk waveforms due to the transmission lines. If the crosstalk is large enough it will cause $\overline{A}_4$ to go above the threshold voltage, as shown in Figure 4.22, and therefore become logic one and cause the wrong address to be read on the bus. The expected crosstalk due to the combination of the sockets and transmission lines will be more complex, but similar to what is shown in Figure 4.21.

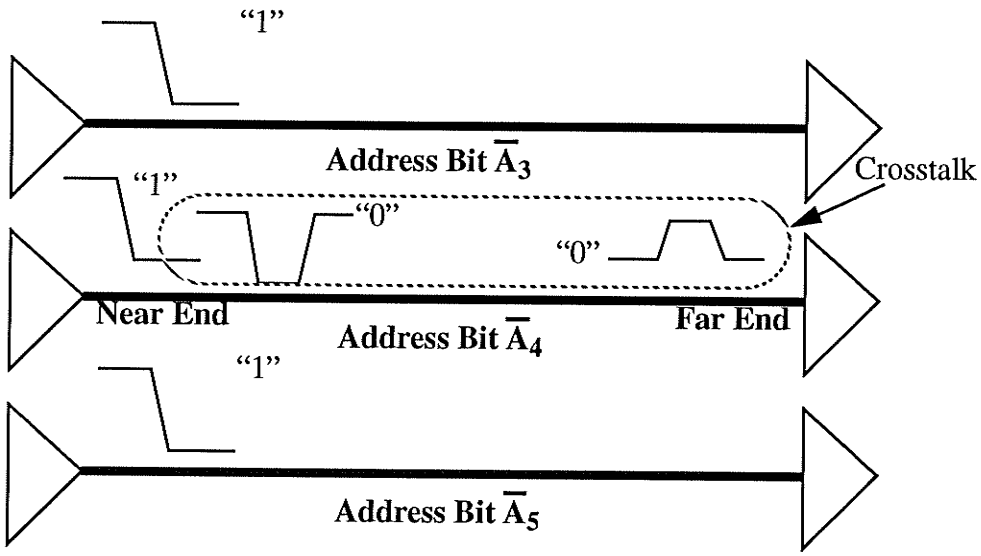

Figure 4.19: Worst case address bus crosstalk.

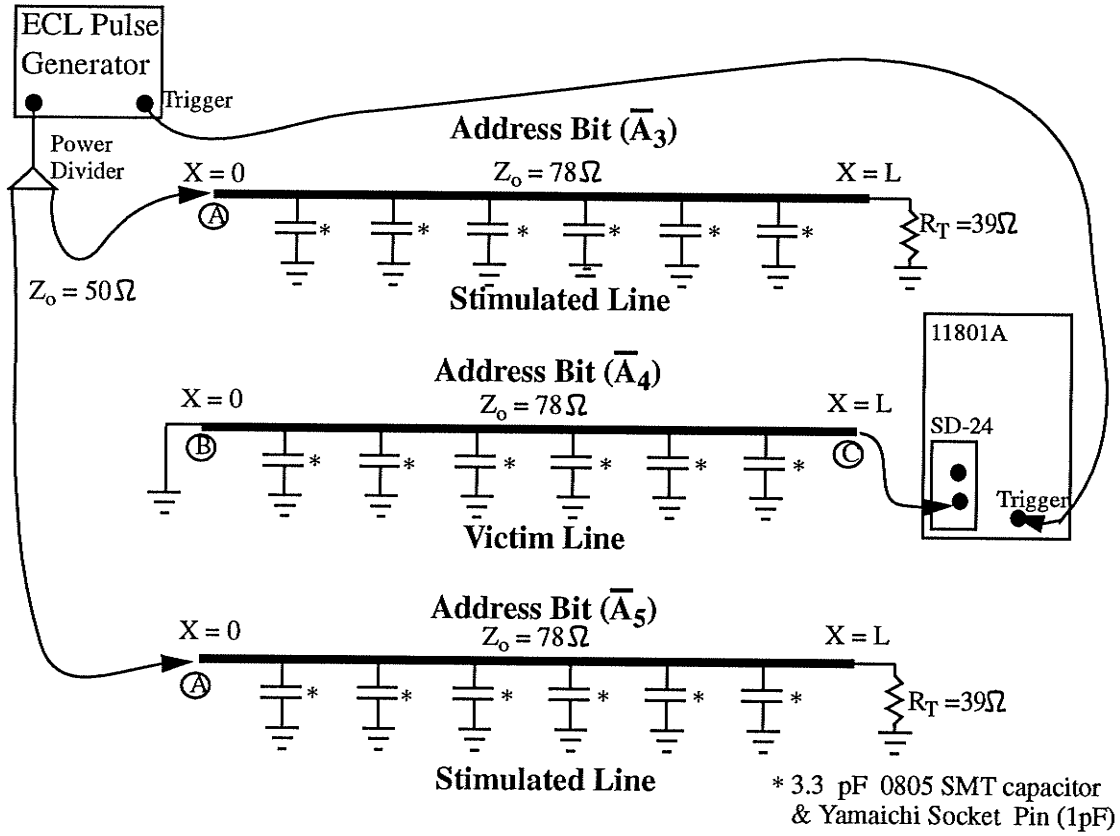

Figure 4.20: Far End crosstalk measurement setup.

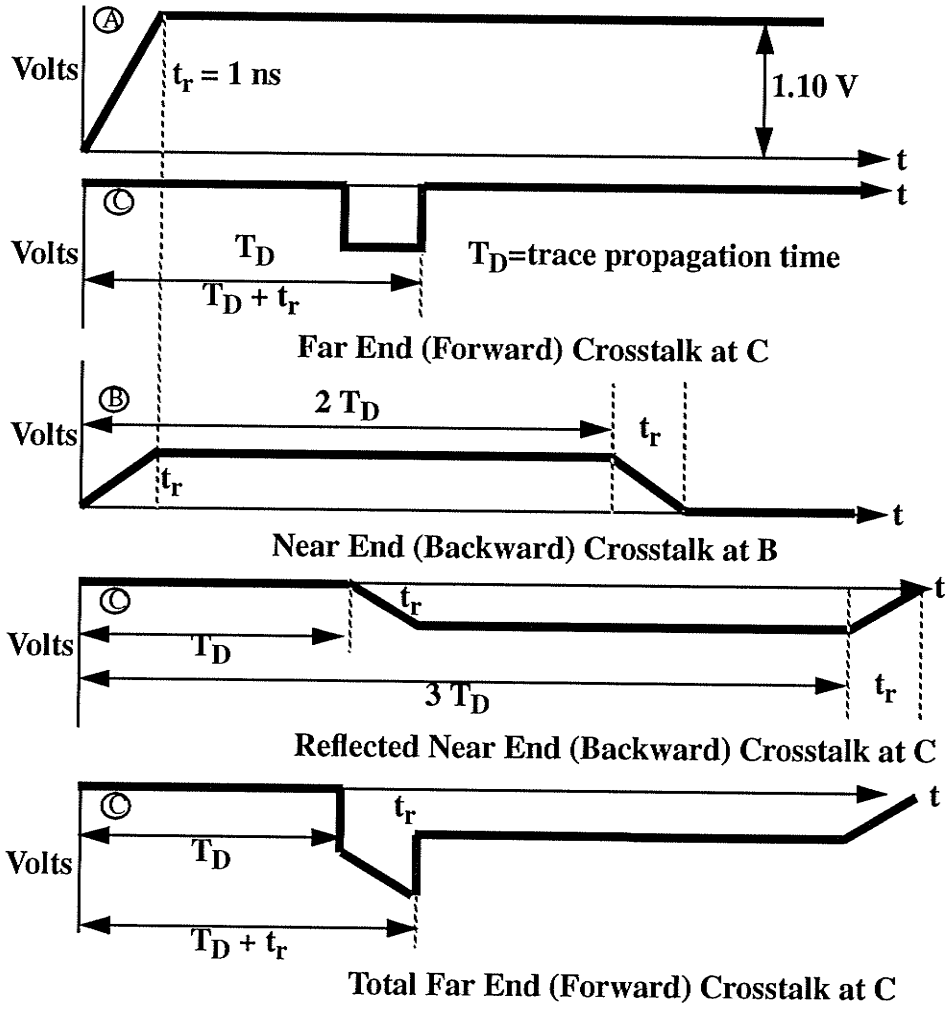

Figure 4.21: Victim line near and far end crosstalk voltage waveforms for a rising pulse.

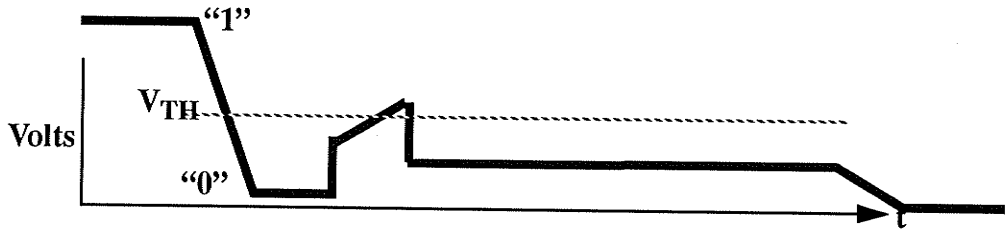

Figure 4.22: Expected voltage at the far end of $\overline{A}_4$.

Figure 4.23 shows a 1.07 V (ECL-like) square pulse train (823 ps 10-90% rise time) used to stimulate address bits $\overline{A}_3$ and $\overline{A}_5$. This input pulse is similar to the output waveform of the ECL counter driving the address bus.

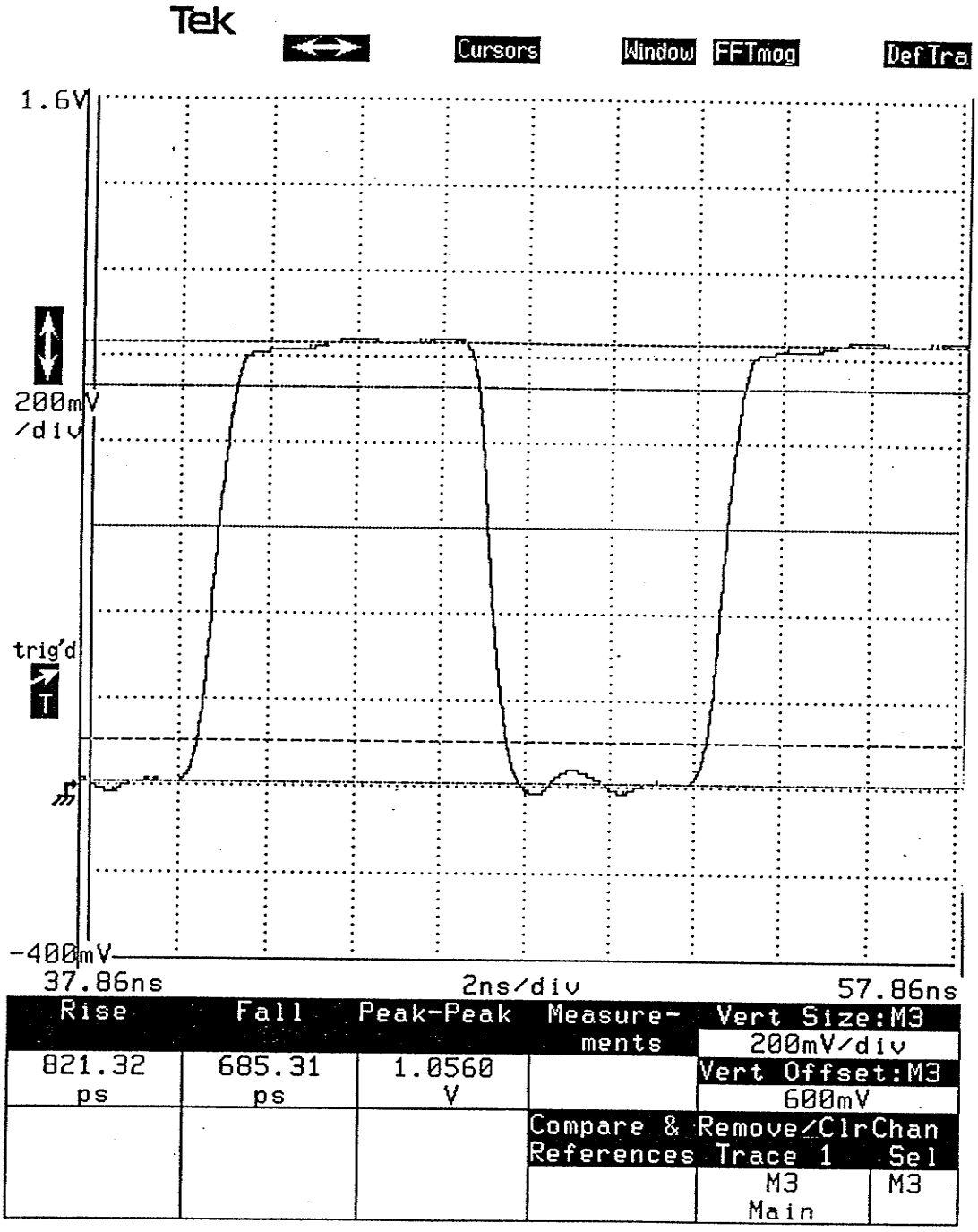

Figure 4.23: ECL-like input pulse train fed into Address bus traces $\overline{A}_3$ and $\overline{A}_5$.

The victim line ($\overline{A}_4$) will be monitored at the far end with a Tektronix Dual SD-24 TDR/sampling head. The sampling head's 50 Ω internal termination will terminate the near end of the victim line and will cause some reflections. Figure 4.24 shows the resulting crosstalk on $\overline{A}_4$ with no SRAM sockets soldered onto the Address bus. The crosstalk has a maximum and a minimum voltage peak of 58.4 mV and 49.6 mV respectively. The maximum peak voltage is of interest, since this is the result of the one to zero transition. The crosstalk ratio, which is the resulting crosstalk voltage divided by the input or stimulating voltage, is (0.0584/1.07) 0.055 or 5.5%. Also, take note that the far end crosstalk waveforms resemble the predicted waveforms shown previously in Figure 4.21.

Figure 4.25 shows the resulting far end crosstalk with all six SRAM sockets soldered onto the Address bus. The maximum and minimum crosstalk voltages are 90.0 mV and 106 mV respectively. The maximum peak is of interest, and the resulting crosstalk ratio is 0.084 or 8.4%. This is more than a 60% increase in crosstalk over the previous measurement in which no SRAM sockets were on the PCB. The crosstalk consumes almost 2/3 of an ECL's gates noise margins.

Since crosstalk due to adjacent ICs package pins was not measured a rough estimate can be calculated. Figure 4.26 illustrates the mutual capacitance between IC package pins.

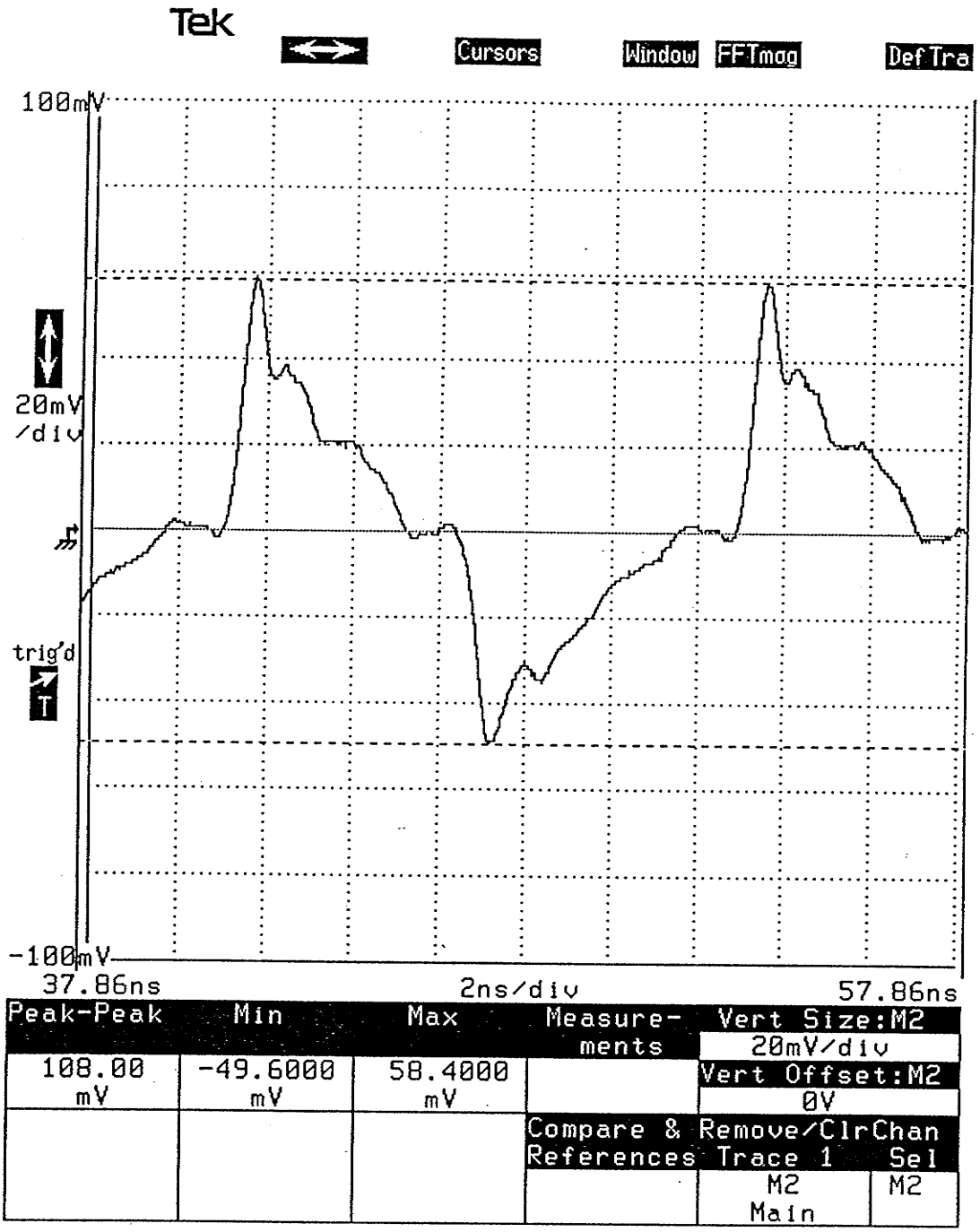

Figure 4.24: Far End crosstalk voltage on Address trace $\overline{A}_4$ - without SRAM sockets.

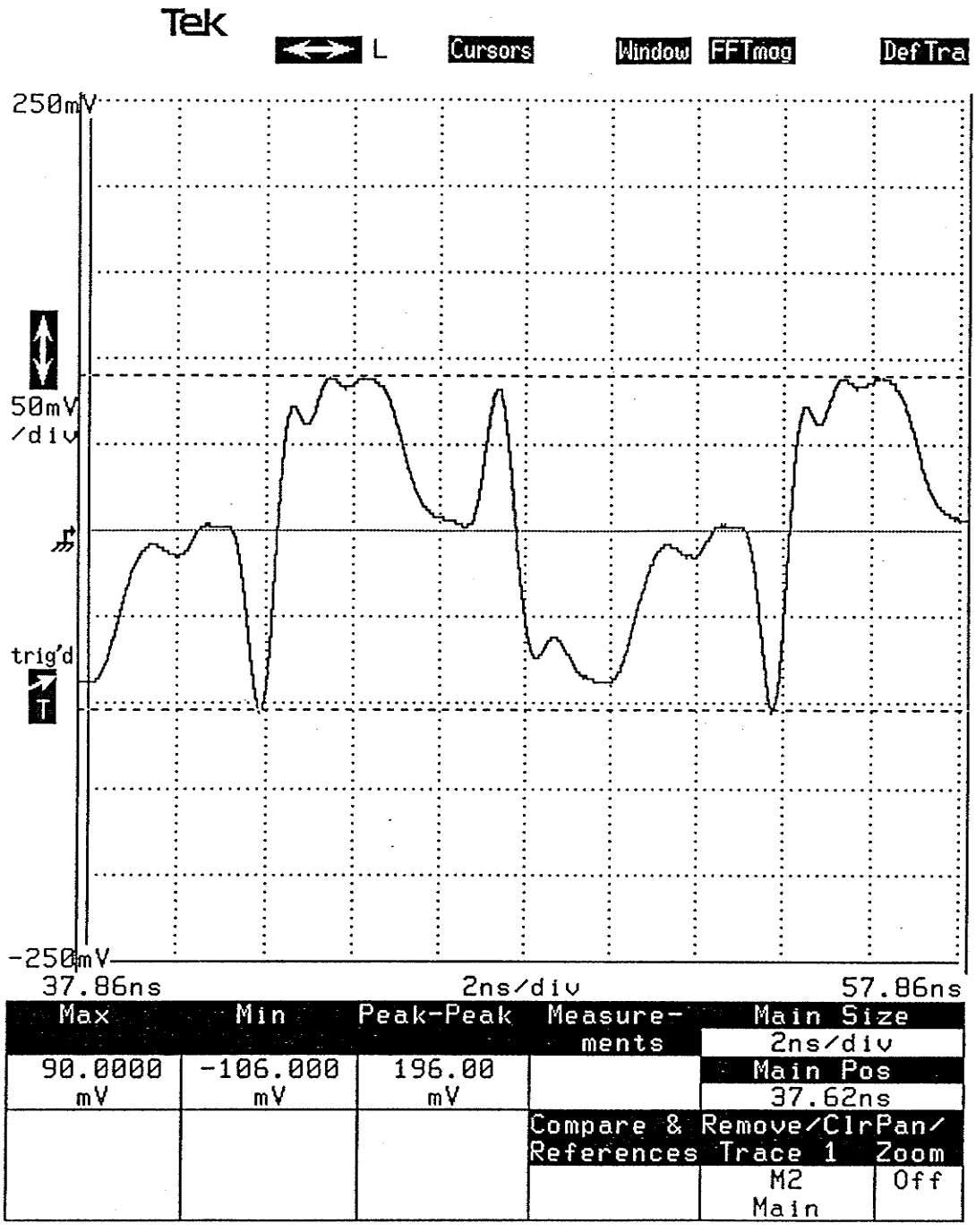

Figure 4.25: Far End crosstalk voltage on Address trace $\overline{A}_4$ -with SRAM (6) sockets.

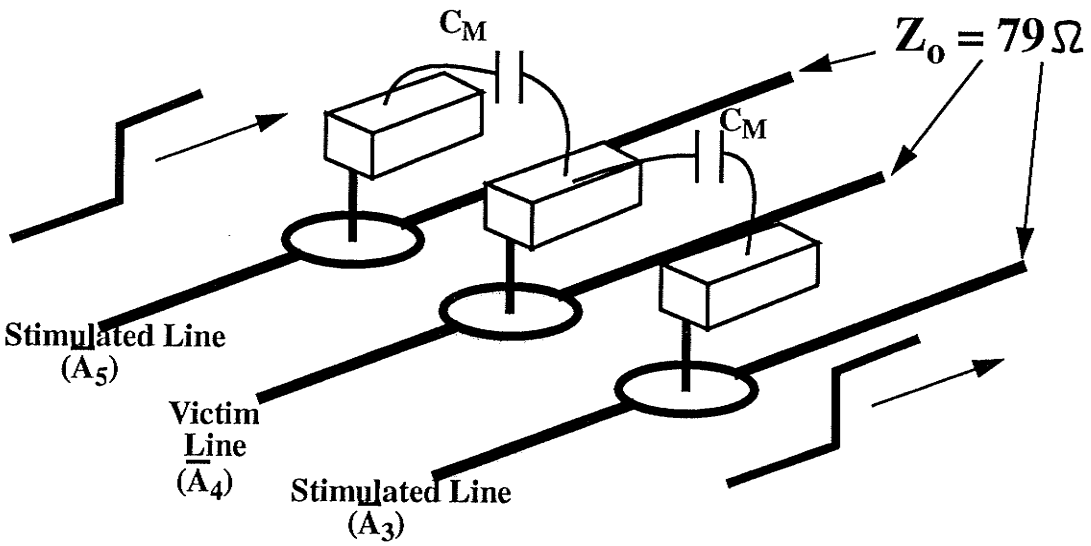

Figure 4.26: Mutual pin to pin package capacitance.

The percentage crosstalk introduced on $\overline{A}_4$ by $\overline{A}_3$ ($\overline{A}_5$) can be calculated as follows:

$$Crosstalk = \frac{R \cdot C_M}{T_{10\text{-}90}} \tag{4.19}$$

Where:

R = 39 Ω (the coupled voltage "sees" the 79 Ω bus in parallel)

C_M = 0.5 pF (mutual capacitance of pin $\overline{A}_3$ and $\overline{A}_4$)

$T_{10\text{-}90}$ = 850 ps (the voltage rise (fall) time of the signal on pin $\overline{A}_3$ or $\overline{A}_5$).

The resulting crosstalk is then 2.3% as calculated in Equation 4.20.

$$\frac{39 \cdot 0.5 \cdot 10^{-12}}{0.85 \cdot 10^{-9}} = 0.023 \tag{4.20}$$

The resulting crosstalk voltage from $\overline{A}_3$ is then (0.023*1.1 V) 25 mV. The total crosstalk from both $\overline{A}_5$ and $\overline{A}_4$ is then approximately 50 mV. Table 4.7 is a compilation of the various contributors of crosstalk on $\overline{A}_4$.

Table 4.7: Crosstalk voltage coupled onto $\overline{A}_4$ by $\overline{A}_3$ and $\overline{A}_5$.

Crosstalk contributor	Crosstalk voltage coupled onto $\overline{A}_4$ (mV)
parallel transmission lines ($\overline{A}_3$ & $\overline{A}_5$)	58.4
adjacent SRAM IC socket pins	31.6
adjacent SRAM IC package pins (estimated)	50.0
Total	140.0

The total crosstalk is 140 mV and matches the ECL noise margin of 140 mV. The SRAMs must be used without the sockets for the system to function properly. Therefore the address bus must be redesigned (a new PCB) to allow placement of the SMT SRAMs. Another solution, which will be discussed in the recommendations section, is to utilize stripline transmission lines.

The SRAM Data bus was laid out with the maximum allowable edge to edge spacing. For a major portion of the bus the edge to edge spacing is greater than 400 mils (0.4 inches). The worst case spacing occurs between channel # 1 data bit D_{11} and channel # 2 data bit D_0 where they are routed parallely for approximately an inch and with edge to edge spacing of 42 mils. The expected crosstalk is small due to the large spacing between data lines and because both ends of the bus are terminated (bidirectional). Like the Address bus, the situation of near end crosstalk becoming far end crosstalk does occur. The near end crosstalk test setup is illustrated in Figure 4.27 and the low ouput impedance of the SRAM Data ouput pin is represented by shorting the near end of the Data bus to ground. Similar to the TDR tests, SMT capacitors (4.4 pF) were soldered onto the via holes to mimic the input capacitances of various gates along the data bus. The various sockets on the bus (SRAM, GaAS multiplexer and ECL translator) were not soldered on the PCB for this measurement.

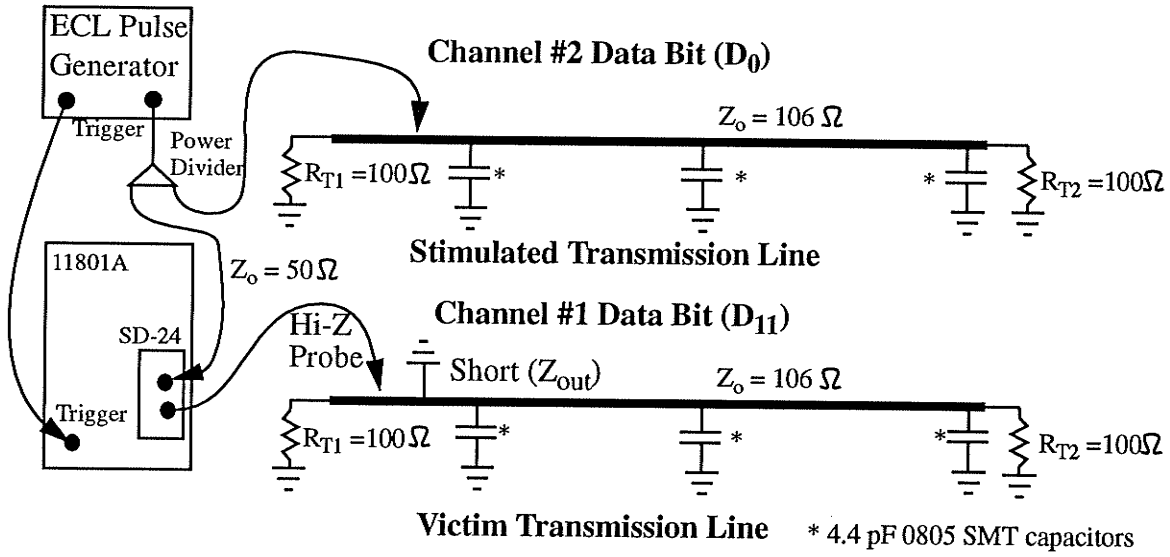

Figure 4.27: Data bus near end crosstalk test setup.

The input into the bus was a 900 mV pulse train with a 800 ps (10-90%) rise time and the resulting crosstalk has a minimum and maximum voltage of 25.2 mV and 22.8 mV respectively. The resulting crosstalk ratio is (0.025/0.9) 0.028 or 2.8%. The resulting crosstalk voltage when all the IC sockets were soldered on was approximately 55 mV. The estimated crosstalk due to adjacent IC pins is 50.0 mV. Therefore, the total crosstalk with and without IC sockets is 105 mV and 75 mV respectively.

4.3 Ground and Power Distribution

It is essential that a high frequency system (PCB) have at least one complete copper layer dedicated to ground (ground potential). A complete plane will lower DC resistance and prevent any voltage differences (IR Drop) between ground pins on ICs. Digital logic inputs and outputs use ground (logic) directly or indirectly as the reference voltage for logic thresholds. For example, when two logic circuits are connected together in a single-ended mode, any difference in ground potentials will decrease noise margins [37]. If the drop exceeds noise margins then system functionality is jeopardized.

A ground plane also acts a current return path, or AC ground plane, in a transmission line as illustrated in Figure 4.28.

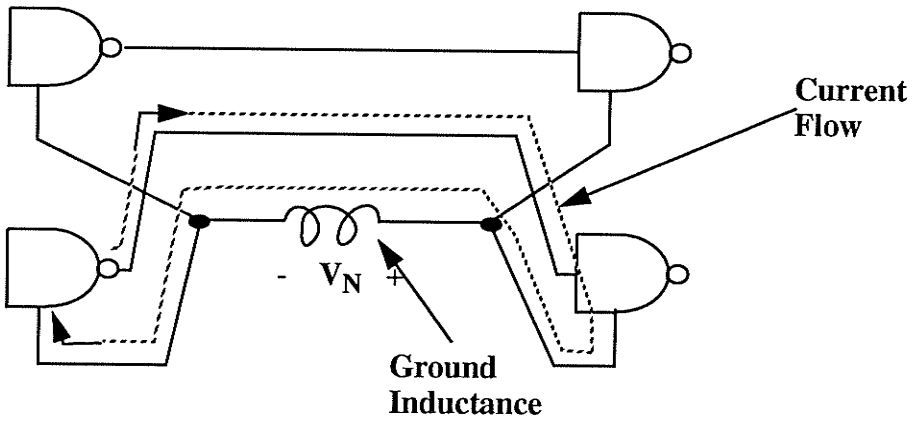

Figure 4.28: Ground current flow and ground inductance.

The transmission line returning current will follow the path of least inductance which is directly beneath the transmission line signal conductor. Any cutouts in the ground plane or lack of a complete copper plane beneath a transmission line will increase inductance and hence the impedance ($Z_o = \sqrt{L_o/C_o}$). Also, if there are numerous returning currents, a high inductance ground plane will create noise voltages (V_N) and hence decrease noise margins.

Power planes should also be distributed, especially for the GaAs power supplies, as complete copper planes or split planes to minimize DC voltage drop. All the tester's power supplies were designed as either complete planes or split planes. Unfortunately, as the tester PCB artwork in Appendix A illustrates, the power planes were fabricated as a mesh pattern. Four point probe measurements indicated a resistance of 25 mΩ across the largest meshed power plane (+5 V). Therefore, the DC (V=IR) drop will then be minimal but a slight increase in inductance would be expected.

Looking from an ICs power terminals, a good power distribution network should have an AC impedance vs. frequency behavior that resembles the curve in Figure 4.29. The impedance should be flat for a wide frequency range.

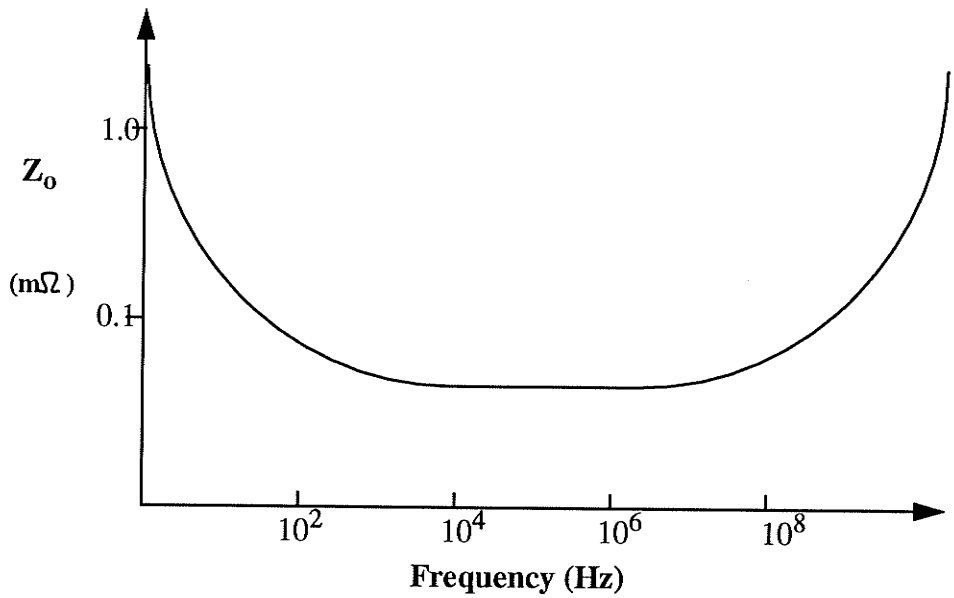

Figure 4.29: Desired power distribution impedance as a function of frequency [29].

This power distribution AC behavior is achieved with many levels of decoupling or bypassing capacitors. Bypass capacitors reduce power-supply-level fluctuations by charging up at steady state and then assuming the role of a power supply during current switching [29]. The selection of capacitor values for bypassing and capacitor modelling will not be discussed in this thesis, but can be found elsewhere [22,41,48-49]. The three levels of bypassing are:

1) Board Level Filtering.

2) IC Level or Local Filtering.

3) Capacitance of Power and Ground Planes.

At the board level, as the power supply enters the board, a large tantalum (10 μF) SMT (surface mount) capacitor is placed to filter low frequency noise. Smaller tantalums (1 μF) are placed near groups of ICs to provide further low frequency filtering. These tantalums provide the (low) impedance behavior at the low frequency end illustrated in Figure 4.29.

IC level or local filtering is achieved by placing a ceramic SMT decoupling capacitor as close as possible to each ICs power pin. SMT capacitors are used because

of very small ESR (Equivalent Series Resistance) and inductance (5 nH) parameters [41]. This level of bypassing will provide the (low) impedance behavior in the mid frequency section of the impedance vs. frequency curve. It is crucial that the capacitors are placed as close as possible to the power supply pins to minimize inductance and maximize effectiveness. Figure 4.30 illustrates a photo of the placement of bypass capacitors for the Gigabit GaAs parts. The capacitors were placed on the secondary side (layer 6) on pads that were connected, through vias, to the ICs power pins.

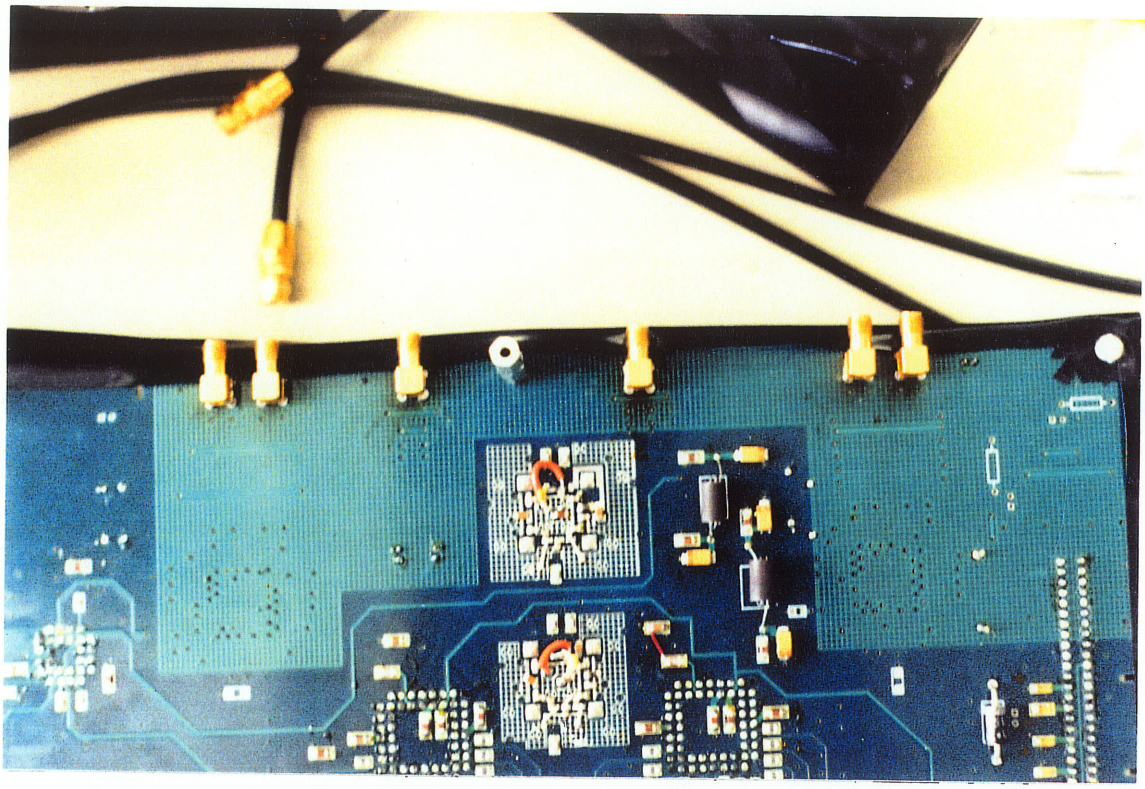

Figure 4.30: Photo of bypass capacitors placed on the backside of a GaAs IC.

The third level of bypassing takes advantage of the PCB itself as a bypass element [50]. Placing power and ground planes extremely close (dielectric thickness < 0.010") creates an effective zero lead inductance and zero ESR capacitor. This helps reduce power and ground noise at extremely high frequencies. A high speed system requires all three levels of bypassing to minimize power supply noise as much as possible and hence maintain system functionality.

The biasing power supply (-2 V) connected to termination resistors must also be bypassed. Figure 4.31 illustrates the bypassing of a typical parallel termination being driven by an ECL output gate. The -2.0 V supply is decoupled to ground via a bypass capacitor. The decoupling of the -2.0 V supply to ground ensures that the transmission line return will continues to ground and then returns to the ground pin of the driving gate as shown in Figure 4.31.

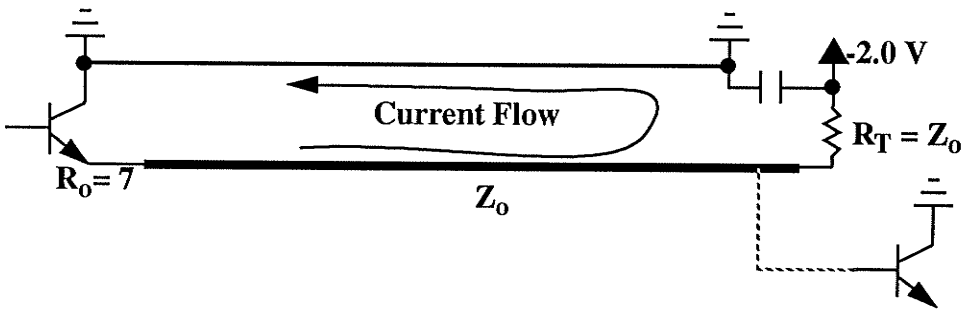

Figure 4.31: Bypassing of termination resistor biasing voltage supply.

The high frequency clock (1.2 GHz) is the major source of high frequency noise in the system. Good system practice is to prevent the clock system from interfering with other parts of the system [37]. The clock noise must therefore be isolated from the rest of the system via isolation of the clock's power supply. Figure 4.32 illustrates a noise filter which is comprised of a ferrite bead and a couple of capacitors shunted to ground. Ferrite beads are inductive at low frequencies but become extremely lossy at higher frequencies, Ferrite beads have a frequency dependent resistive component ($R(\omega)$) [51]. The ferrite bead chosen for the tester has a resistive component of nearly 200 Ω at 1 GHz [52]. This filter will attenuate any high frequency noise from polluting the rest of the system.

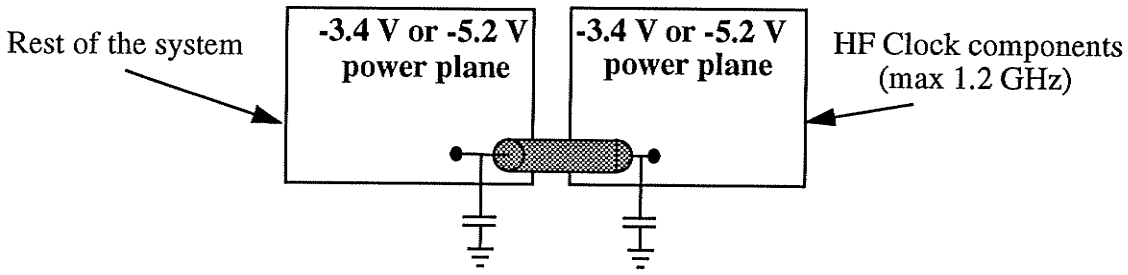

Figure 4.32: Noise filter isolates high frequency clock power supply from the rest of the system.

4.4 Noise Budget Analysis

A noise budget analysis [40] must be performed on each major section - the SRAM Data and Address busses - of the tester to verify that noise margins have not been violated. Factors that decrease noise margins are as follows:

1) Ground or Voltage Plane DC (IR) Drop

2) Ground Bounce

3) Voltage Supply Fluctuations

4) Crosstalk

5) Trace and IC package resistance

6) Transmission line ringing or reflections

Each section utilizes ECL levels and Table 4.8 illustrates all the ECL logic parameters including the logic low (V_{NL}) and high (V_{NH}) noise margin levels. As Table 4.8 shows the noise margins are very small.

Table 4.8: F100K series ECL logic levels and noise margins.

Parameter	Volts
V_{OH}(max)	-0.870
V_{OH}(min)	-1.025
V_{OL}(max)	-1.62
V_{OL}(min)	-1.83
V_{IH}(max)	-1.475
V_{IH}(min)	-1.165
V_{NH}	***0.140***
V_{NL}	***0.145***

4.4.1 Ground IR Drop

Ground (0 V potential) is used as a reference, directly or indirectly, by all the digital logic on the tester. It is essential that there is no potential difference between ground pins on the PCB ICs. The potential difference (ΔV) is caused by the resistance differential (ΔR) between the power connector and two (or more) IC ground pins (R_1 & R_2) and the ground current (I) as shown in Figure 4.33.

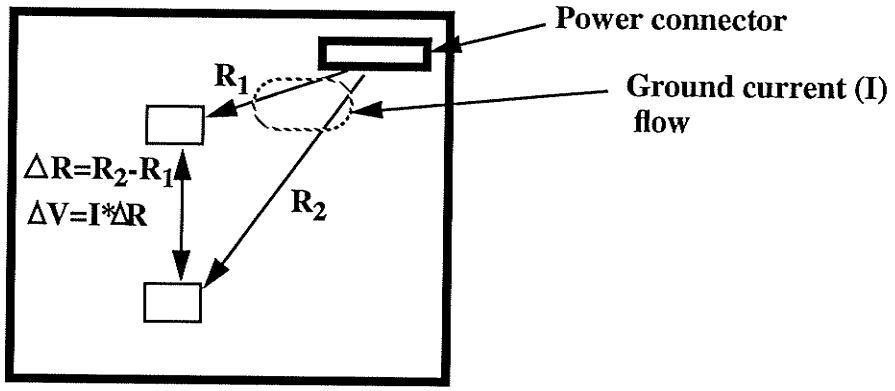

Figure 4.33: Ground (IR) voltage drop.

The resistance differential (ΔR) should be kept small by using a complete power plane as was done on the PCB ground plane. The resistance of the ground plane (layer two) from one corner of the tester PCB to the opposite corner (16.9 inch diagonal) was measured with a four point probe ohmmeter and was found to be 2.53 mΩ. The resistance between the ground pins of the ECL counter and the furthest SRAM is 0.28 mΩ. The resistance differential for the SRAM Data bus section, SRAM to multiplexer ground pins, was also very small (< 0.20 mΩ). Therefore, the ground IR drop on both the SRAM Data and Address bus sections will be insignificant and can be ignored.

4.4.2 Ground Bounce

Unlike with CMOS circuits [53-54], ground bounce or simultaneous switching noise is relatively small for ECL ICs because of two factors. The first is that most modern ECL ICs have separate ground pins for the internal circuitry (logic) and the output buffer stages (emitter follower) as shown in Figure 4.34. Also, the inductance of the packaging is decreased by including many ground pins. For example, a 28 pin PLCC ECL four bit counter has three ground pins, one for the output drivers and the remaining two for the logic structure.

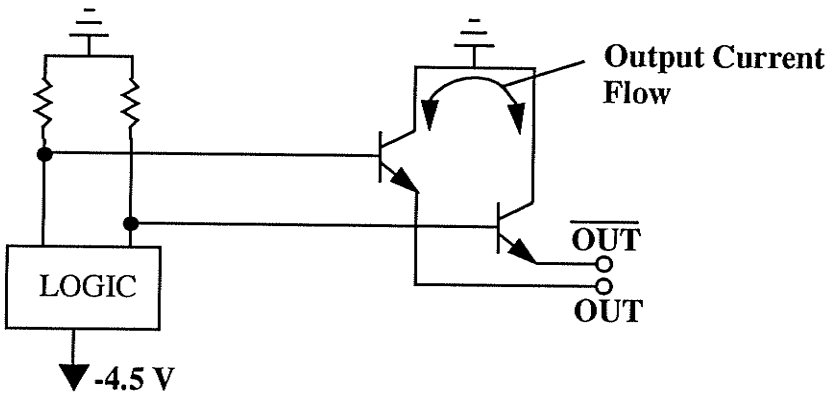

Figure 4.34: ECL differential output structure

The second factor that reduces ground bounce is the differential structure of ECL output stages. As one output switches from a low to a high state the other switches from a high to a low simultaneously. The resulting current change through the ground pin is zero because the current supply switches between the two outputs as shown in Figure 4.34. This is assuming balanced loads on the outputs, which in practice due to component and PCB tolerances is extremely difficult to achieve. So, evidently there will be some ground bounce due to the imbalance. A value of < 10 mV will be allocated to both the Address and Data bus noise budgets.

4.4.3 Crosstalk

As shown in Section 4.2 crosstalk is a major problem with the Address bus. With the SRAM sockets the crosstalk alone exceeded the SRAM's ECL noise margins. The resulting crosstalk without the SRAM sockets is 108.0 mV. The crosstalk on the SRAM Data bus with and without sockets is estimated to be 75 mV and 105 mV respectively.

4.4.4 Power Supply Voltage Fluctuations

ECL parts are voltage compensated and its supply voltage can range from -4.2

to -5.7 V without affecting any of its specified input or output voltage parameters. Therefore, it is safe to assume that power supply voltage fluctuations will have no effect on the noise margin.

4.4.5 Termination Reflections

As seen in section the voltage reflections due to termination mismatch on the Address and Data busses were both approximately 20 mV. The reflections can be reduced slightly by tweaking the resistor values until they are optimized.

4.4.6 Resistive, Dielectric and Skin Effect Losses

The microstrip transmission lines used on the two busses will exhibit losses due to the following [22,55]:

1) Dielectric losses (loss tangent = 0.020)

2) Skin Effect

3) Resistive losses

Table 4.9 illustrates the calculated losses per inch of both busses at various frequencies. The skin effect will have little effect at frequencies < 1GHz, but the dielectric losses should be taken into account because of the lossy nature of FR-4 substrates. The attenuation at higher frequencies attenuates the higher harmonics and hence slows the rise time of a pulse edge as it travels down the bus.

Table 4.9: Losses (dB/inch) of Address and Data busses at various frequencies.

Frequency (MHz)	Address Bus (dB/inch) (76 Ω)	Data Bus (dB/inch) (106 Ω)
100.0	0.26	0.26
250.0	0.44	0.44
500.0	0.70	0.70

Table 4.9: Losses (dB/inch) of Address and Data busses at various frequencies.

Frequency (MHz)	Address Bus (dB/inch) (76 Ω)	Data Bus (dB/inch) (106 Ω)
1000.0	0.113	0.122

Experimental data showed the loss for a six inch Address and four inch Data bus lines were 10 mV and 12 mV respectively.

4.4.7 SRAM Address and Data Bus Noise Budget Summary

Table 4.10 illustrates a summary of the noise budget for the Address Bus. Also, take note that the crosstalk contribution is tabulated with and without SRAM sockets. The noise budget is exceeded by 8 mV even without the use of IC sockets. The design of the Address bus must be reconsidered to assure system functionality.

Table 4.10: SRAM Address bus noise budget summary.

Noise Sources	Voltage (mV)
Ground IR drop	N/A
Ground Bounce	< 10.0
Crosstalk without sockets (with sockets)	108 (140)
Power Voltage Fluctuations	N/A
Termination Reflections	< 20.0
Microstrip Losses	10.0
Total Noise	***148 (180)***
ECL Noise Margin (V_{NL})	***140.0***
Remaining Noise Margin	***-8.0 (-40.0)***

The SRAM Data bus noise budget summary is shown in Table 4.11. The remaining noise margin is 23.0 mV without utilizing sockets and is exceeded by 7.0 mV with the use of sockets.

Table 4.11: SRAM Data bus noise budget summary.

Noise Sources	Voltage (mV)
Ground IR drop	N/A
Ground Bounce	<10.0
Crosstalk without sockets (with sockets)	75 (105)
Power Voltage Fluctuations	N/A
Termination Reflections	< 20
Microstrip Losses	12.0
Total Noise	***117.0 (147.0)***
ECL Noise Margin (V_{NL})	***140.0***
Remaining Noise Margin	***23.0 (-7.0)***

4.5 System Timing

A timing analysis of the system using the best and worst case IC timing parameters must be performed to ensure system operation at the highest CLK frequency (1.2 GHz). The timing analysis assumes that noise margins have not been violated (Section 4.4) and the system will remain functional up to the highest operating frequency (bit rate). The analysis will take into account all trace propagation delays. The GaAs VS8001 12:1 multiplexer is the heart of the tester and is the IC that drives the system timing requirements. The multiplexer's block diagram, timing waveforms and AC characteristics are illustrated in Figure 4.35, Figure 4.36 and Table 4.12 [56] respectively. The multiplexer's major timing constraint is that the parallel data (D_{11}-D_0) inputs must meet the DCLOCK's data setup time (t_{SSU}) and data hold time (t_{DSU}) specifications. The DCLOCK can be an independent clock, which can be aligned with the data (D_{11}-D_0) using the SET input (synchronization input).

According to Vitesse, a delayed version of the CLOCK12 (CLOCK12 = CLK/

12) output can be used as the DCLOCK input as long as it is synchronized with the CLKOUT (NCLOCKOUT) output as illustrated in Figure 4.36 [57]. The tester will utilize a delayed version of the CLOCK12 output as a DCLOCK input. variable delay lines in the CLOCK12 path will provide the delay to achieve the alignment of the CLOCKOUT output with the CLOCK12 output.

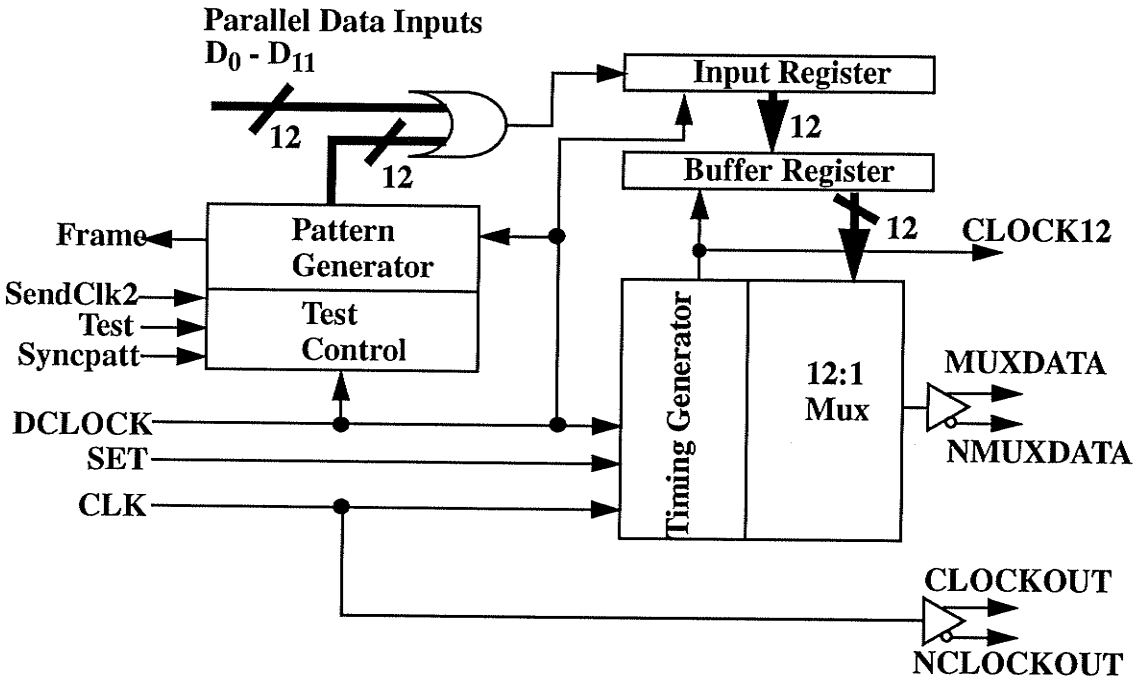

Figure 4.35: VS8001 12:1 multiplexer block diagram [56].

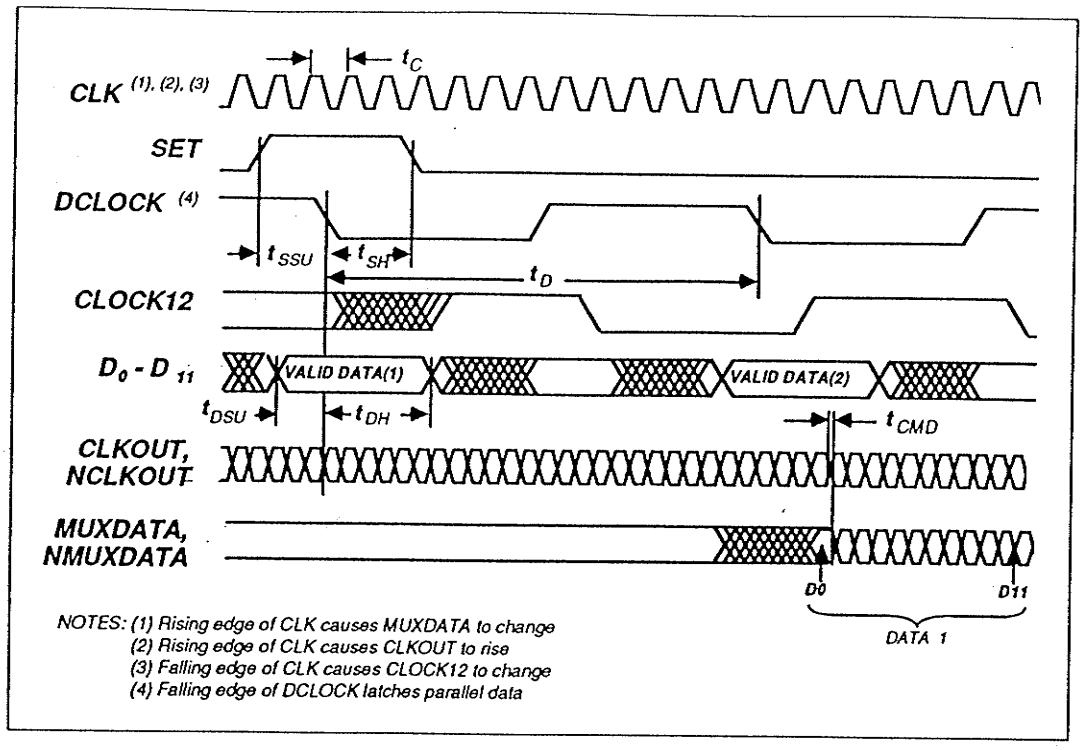

Figure 4.36: VS8001 12:1 multiplexer timing waveforms [56].

Table 4.12: VS8001 AC characteristics [56].

Parameter	Description	MIN	TYP	MAX	Units
t_C	CLK period	0.80	-	-	ns
t_D	DCLOCK period	9.6	-	-	ns
t_{SSU}	Set set-up time	2.0	-	-	ns
t_H	Set hold time	3.0	-	-	ns
t_{DSU}	Data set-up time	2.0	-	-	ns
t_{DH}	Data hold time	3.0	-	-	ns
t_{CMD}	Clock Output (CLKOUT,NCLK-OUT) to muxed data output (MUX-DATA,NMUXDATA) timing	-50	-	+150	ps

Table 4.12: VS8001 AC characteristics [56].

Parameter	Description	MIN	TYP	MAX	Units
jitter	CLK to MUXDATA, NMUXDATA (max-min), (HIGH to LOW) same part, same pin as constant conditions	-	<50	-	ps

The variable delay lines (ELMEC SDU5050) [58], which are used to delay the CLOCK12, have a variable delay time range of 0 - 1.55 ns with a 50 ps resolution (32 variable steps). The delay line have a worst case residual delay of 400 ps or less and have a worst case (at max delay) bandwidth of 1 GHz or more. A scope photo of an SDU4050 delay line, which has a delay range from 0 - 750 ps (16 variable steps), is shown in Figure 4.37 and illustrates the 50 ps edge placement capability.

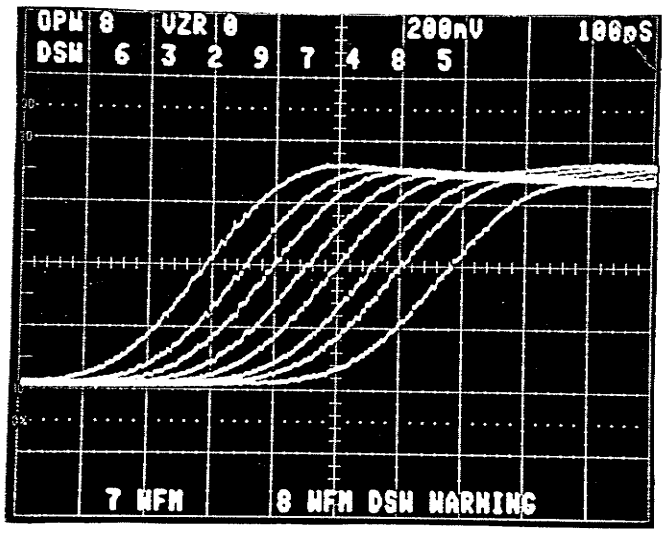

Figure 4.37: Scope photo of the 50 ps edge placement capability of the SDU4050 delay line.

The tester's crucial timing requirement is to have the CLOCK12 output toggle the counter to the next SRAM address value and have the SRAMs new data outputs present at the multiplexer's data parallel (D_{11}-D_0) inputs so it meets the multiplexer's DCLOCK's data setup (t_{SSU} = 2 ns) and hold time (t_{DSU} = 3 ns) constraints. This tim-

ing requirement will be known as the *cycle time*. For the tester to operate at 1.20 Gb/s, the maximum test vector rate, the CLK frequency is 1.20 GHz and the DCLOCK (100 MHz) period (*cycle time*) is 10.0 ns. Figure 4.38 shows all the ICs and trace delays involved in the cycle and Table 4.13 illustrates the trace propagation delays and worst and best case IC propagation delays respectively.

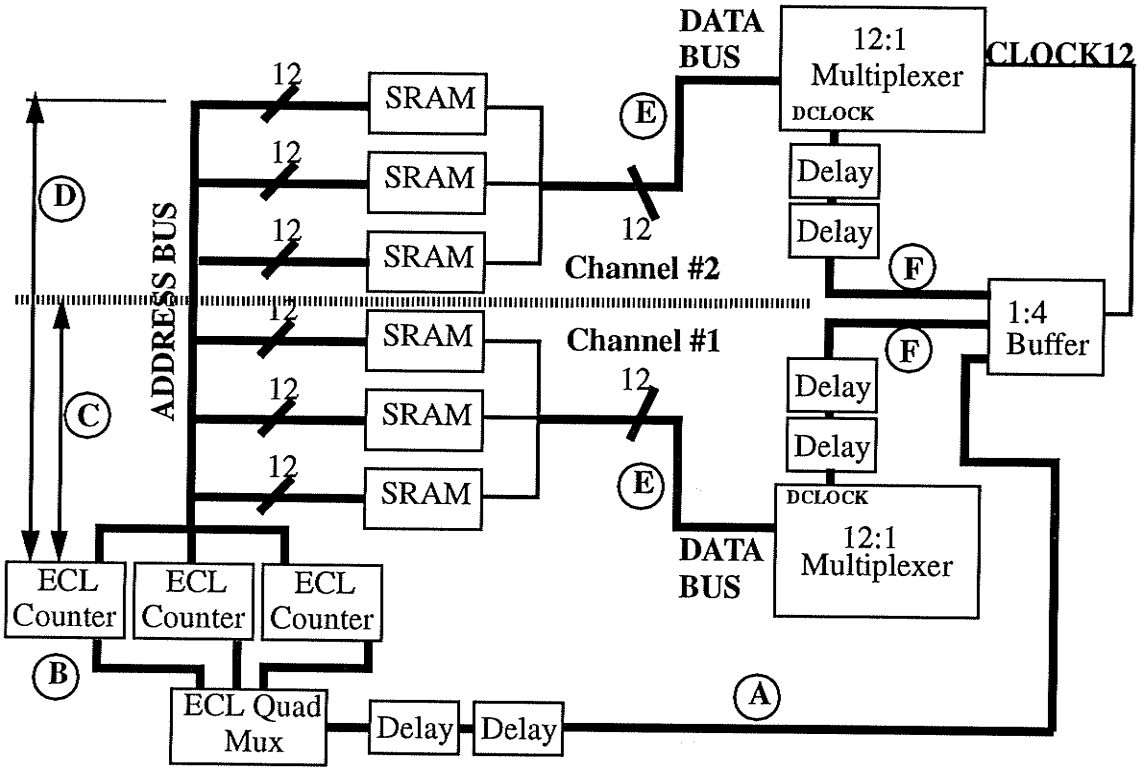

Figure 4.38: Tester transmission line delay paths.

Table 4.13: Tester transmission line propagation delays.

Path	Description	Delay (ns)
A	1:4 Buffer to ECL quad Mux trace delay	1.4700
B	ECL Quad mux to 4-bit ECL counter trace delay	0.4730
C	ECL counter to Channel #1 SRAM address input trace delay	0.7865

Table 4.13: Tester transmission line propagation delays.

Path	Description	Delay (ns)
D	ECL counter to Channel #2 SRAM address input trace delay	1.5730
E	SRAM data output to GaAs 12:1 multiplexer trace delay	1.1300
F	1:4 Buffer to GaAs 12:1 multiplexer DCLOCK input trace delay	1.0710

Table 4.14: Best and worst Case propagation delay parameters.

Part	Best (ns)	Worst (ns)
ELMEC delay line (residual delay)	-	0.40
ECL 100355 quad multiplexer	0.60	1.70
ECL 100336 4-bit counter	1.00	1.80
SRAM (data access)	-	5.00

Figure 4.39 illustrates the timing diagram for a 10.0 ns *cycle time* taking into account the best and worst case IC propagation delays and all trace delays. The timing diagram is best understood by also viewing Figure 4.38 which illustrate all the trace paths and the ICs. The first waveform illustrates the CLOCK12 pulse at the DCLOCK input pins of the multiplexers (equalized). In this example, the (CLOCK12) rising edge is placed at the **0 ns** point. The second waveform is the CLOCK12 at the ECL mux input pin. The CLOCK12 trace delay to the ECL Mux is slightly longer (trace **A** - **F**) than to the DCLOCK input.

Waveform #3 illustrates the CLOCK12 once it has propagated through the ECL multiplexer (best and worst case). The inversion of CLOCK12 is required to achieve the required timing constraints. Waveform #4 displays the trace delay between the ECL multiplexer output and the counter clock input pin. The fifth and sixth waveforms illustrate the propagation (best and worst case) and trace delay of the counter's LSB (least significant bit) output to channel # 1 and # 2 SRAM address inputs respectively.

The counter toggles on a positive edge, so it effectively divides CLOCK12 by two.

Waveforms # 7 and # 8 shows the best and worst case times of Data present at the multiplexer's parallel data inputs for channel # 1. The SRAM's data access time (5.0 ns) and trace delay is taken into account. The VALID "window" is the period where the SRAMs data is valid and present at the multiplexer's parallel inputs (D_{11}-D_0). The crosshatched "window" indicates invalid data. Waveforms # 9 and # 10 show the best and worst case times of Data present at the multiplexer's parallel data inputs for channel # 2. Again as before, the SRAM's data access time and trace delay is taken into account. The propagation delay difference between channel # 1 and channel #2 (best vs. best or worst vs. worst) is the extra delay in the bus trace (D -C) which is 785 ps.

Finally, the eleventh waveform illustrates the required delay (add delay to waveform #1) of the CLOCK12 signal at the GaAs multiplexer's DCLOCK pins. For proper tester operation of **both channels** the DCLOCK's (dotted lines) setup (t_s) and hold (t_h) time constraints (window) **must be within the VALID time window** for **both** channels. For this example, to place the DCLOCK window in both channel's **Best Case** VALID window a DCLOCK delay of ~ 1.8 ns is needed. This will not be a problem since the two delay lines can provide a maximum delay of 3.1 ns. A 3 ns delay would be needed to place the DCLOCK in the **Worst Case** window of both channels. The timing diagram illustrates that the tester will operate at the maximum CLK frequency for both best and worst case conditions.

A four channel tester utilizing the same multiplexer architecture and multidrop SRAM address would not meet the tester's timing requirements. It would be impossible for the DCLOCK window to fit in the VALID window if four channels were required. This is assuming that the address bus delay could not be addressed any further. This preliminary timing analysis caused the scaling down of the tester from four channels to two.

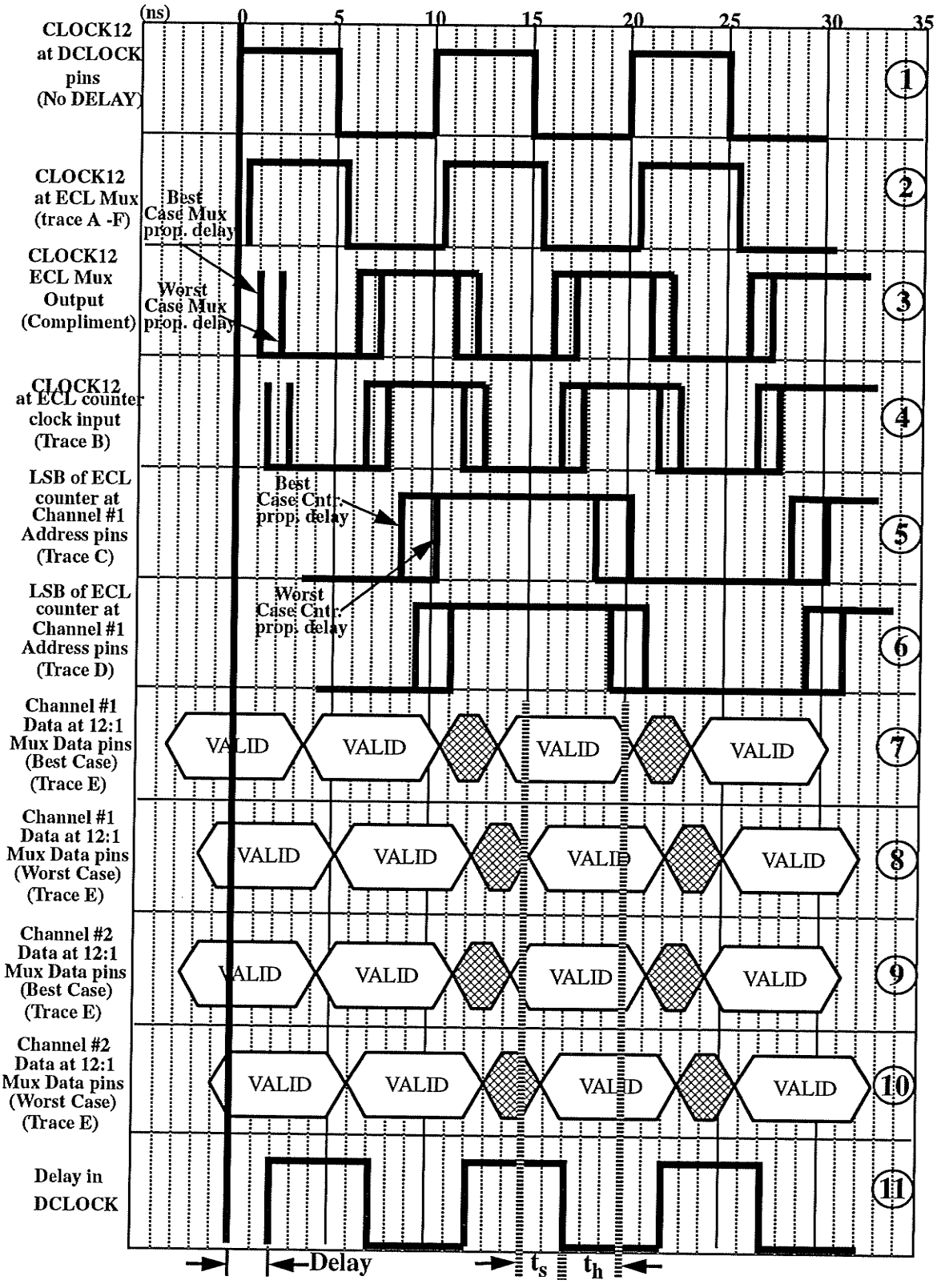

Figure 4.39: Best and Worst case timing diagram for a 10.0 ns *cycle time*.

Chapter 5.0

System Verification Results

This chapter deals with the system verification and performance evaluation of the tester. First, measurement errors due to oscilloscope bandwidth limitations will be discussed as well as crude calculations to approximate rise times from these erroneous measurements. To illustrate system functionality a high frequency path of one tester channel will be tested. Two twelve bit patterns will be used to illustrate tester functionality ranging from lower bit rates to the maximum bit rate of 1.20 Gb/s. The GaAs 2:1 multiplexer previously tested with the hybrid system will be retested and the results may illustrate the tester's versatility. Finally, a brief discussion of future system verification required to thoroughly characterize the tester's performance.

5.1 Oscilloscope Bandwidth Limitations

A majority of the signals on the tester that require monitoring have rise times below 200 ps, which effectively represents a signal with a 2.4 GHz (BW $\cong$ $0.35/t_r$) bandwidth. To **accurately** measure these waveforms an oscilloscope with a bandwidth extending up to the signal's third harmonic is required ($\cong 8\text{GHz}$). Equation 5.1 illustrates this relationship.

$$Bandwidth_{scope} \cong 3 \cdot Bandwidth_{signal} \tag{5.1}$$

Using an oscilloscope with a bandwidth lower than described in Equation 5.1 will not accurately measure a sub 200 ps rise time signal. The lack of bandwidth will reduce the input signal's high frequency content and mask any "glitches" or ringing. Figure 5.1 illustrates the measurement error for oscilloscopes of various bandwidths.

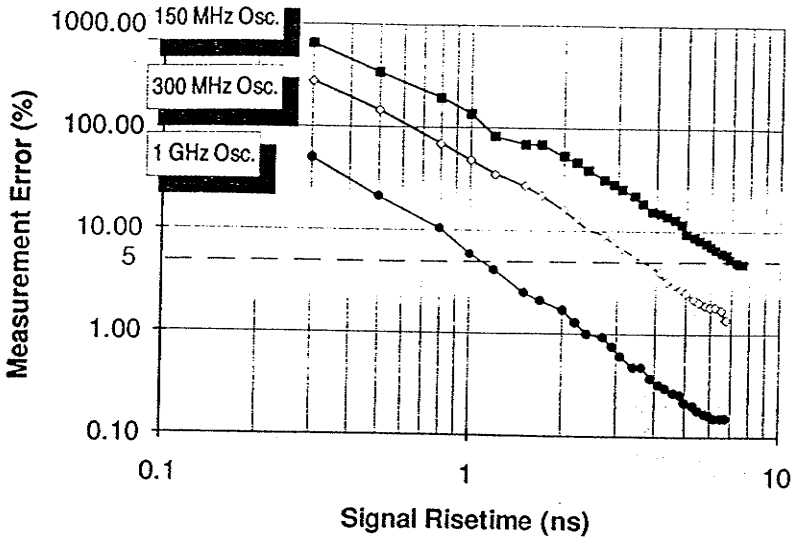

Figure 5.1: Risetime response of various oscilloscopes [59].

Unfortunately, a high bandwidth oscilloscope is not available at the U of M. The only equipment available was a Tektronix DSA 601A digital oscilloscope which houses a 200 MHz (11A34) and 400 MHz (11A32) plug in amplifier. For example, for a 150 ps rise time, which is the pin driver's edge rate, the resulting error for a 400 MHz bandwidth oscilloscope (11A32 amplifier) is greater than 100%. The pin driver's rise time will be estimated (Section 5.3) using composites from the measured rise time. Nevertheless, the available bandwidth will provide adequate signal integrity details to distinguish between catastrophic signal integrity problems and system functionality.

5.2 Test Setup and Results

Testing and verifying the entire tester system was out of the question due to the magnitude of the task and the time required. System verification would consist of testing high frequency sections of a single tester channel and latter if time allowed. Figure 5.2 illustrates the test setup and all the ICs and components that comprise the *high frequency path* of the channel under test (channel # 2). The *high frequency path* is comprised of the following:

1) High frequency (HF) clock distribution.

2) Divide by 12 (Clock12) clock distribution.

3) Channel #2 12:1 GaAs multiplexer.

4) Channel #2 pin driver.

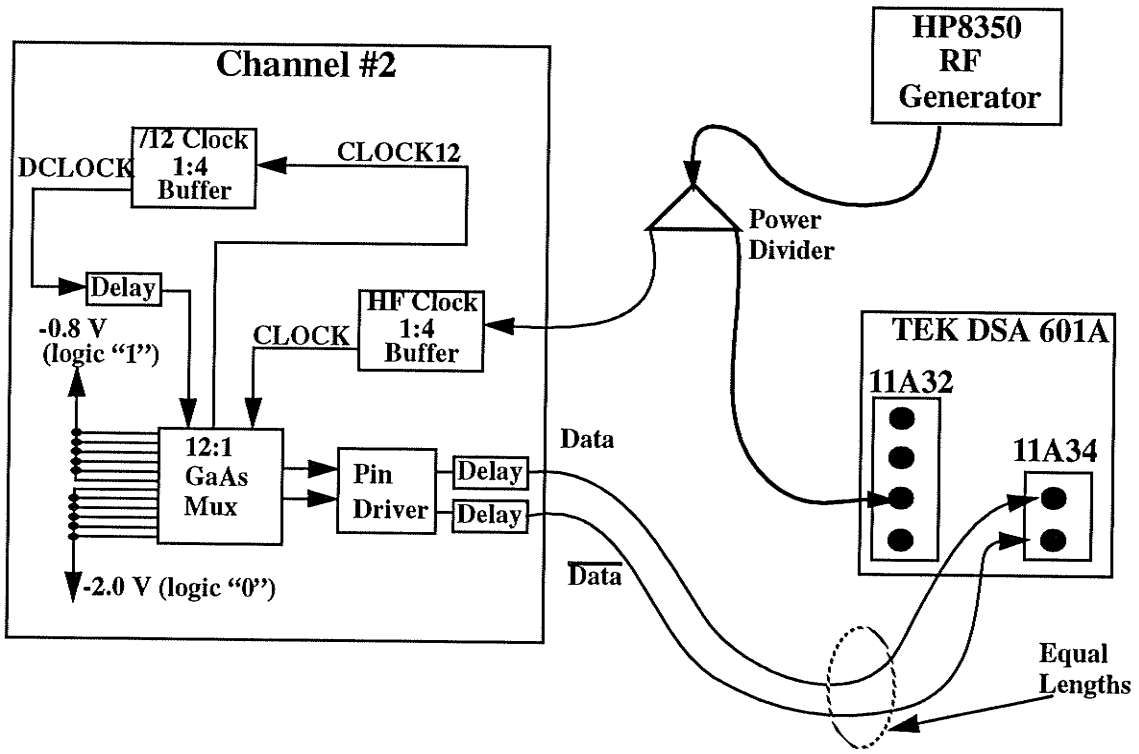

Figure 5.2: Test setup of Channel #2 high frequency path.

Since the SRAM section will not be tested, the multiplexer's data inputs (D_{11}-D_0) will

be set at logic "0" (-2.0 V) or "1" (-0.8 V) using voltage regulators. The longest bit pattern will then be twelve bits long. The HF clock is provided by an HP8350 RF signal generator and split with a power divider to allow viewing by the oscilloscope as illustrated in Figure 5.2. The pin driver's differential outputs are viewed by the oscilloscope via the 400 Mhz (11A34) plug in amplifier. The coaxial cables (~5 feet long) connecting the pin driver's and the oscilloscope were constructed to be of equal length (< 0.25 inch difference) to minimize skew between differential outputs.

The goals of testing the high frequency path of channel #2 were to investigate some of the tester's output characteristics and verify some design objectives put forth in chapter two. The testing goals are as follows:

1) Drive 50 Ω loads with ECL-like voltage swings ($\cong 0.8 - 1.0V$).

2) Drive 1 MΩ loads with CMOS-like voltage swings ($\cong 5.0V$).

3) Investigate pin driver's output signal integrity and verify that the waveform's are suitable for functional testing ICs.

4) Verify that the tester can provide a maximum data bit rate of 1.20 Gb/s.

5) Estimate the pin driver's rise time from the previously mentioned erroneous measured rise time.

Initial trouble shooting of the tester uncovered one issue that was not treated thoroughly at the system level. During a low frequency test (< 10 Mb/s) the pin driver's voltage swing would be constant for approximately one minute and then slowly decrease until the pin driver became non-functional. The problem seemed to be a thermal issue since all ICs in the *high frequency path*, especially the pin driver, were extremely hot. Heat sinks were attached to all the ICs and this allowed the pin driver to function for approximately five minutes before the pin driver again became non-functional. The only solution was to use the brute force method of forcing air over

the ICs using "muffin" fans. This remedied the problem and points out the fact that thermal issues are just as critical as electrical issues in high speed system design. Figure 5.3 illustrates a photo of the heatsinks mounted onto the ICs in the *high frequency path.*

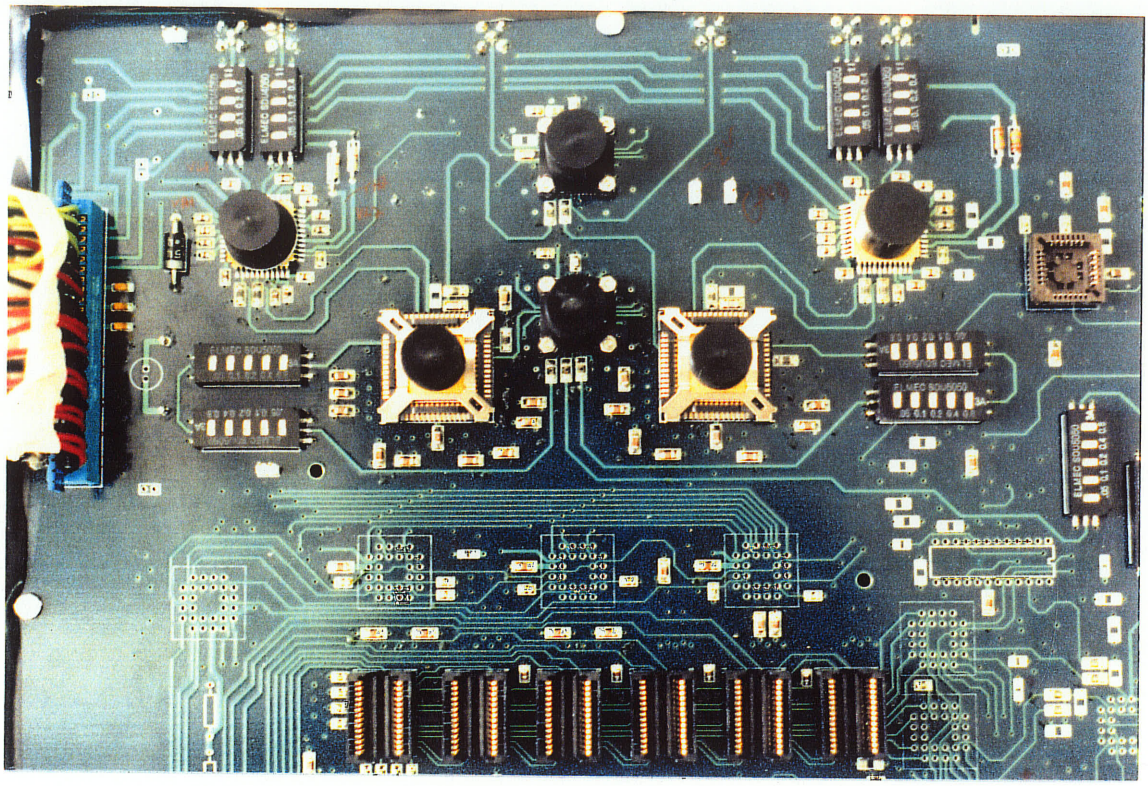

Figure 5.3: Photo of heatsinks attached to *high frequency path* ICs.

As mentioned previously, the maximum allowable pattern length during the testing stage is twelve bits. Two patterns have been chosen to illustrate the operation of the tester. One pattern consists of an alternating pattern of ones and zeroes (D_{11}-D_0=010101010101), a 50% duty cycle, and the second pattern will have a 25% duty cycle (D_{11}-D_0=000100010001). Initial testing was conducted at lower frequencies or bit rates (< 10 Mb/s) and eventually ramped up to the maximum bit rate of 1.2 Gb/s.

Figure 5.5 illustrates the differential pin driver (VO+ & VO-) driving the

scope's 1 MΩ internal termination load with a 1 Mb/s (frequency = 500 KHz), 50% duty cycle pattern. The pattern has a 5.12 V peak-to-peak swing and illustrates the pin driver's capability of driving high impedance load at CMOS levels. The **remaining** test results discussed in this section were performed with the pin driver driving the scope's (amplifier) 50 Ω internal termination with an ECL-like ($\cong 0.8 - 1.0V$) voltage swing. A 50 Ω environment and termination, as well as ECL-like voltage swings, are more typical of high speed systems and DUT test jigs, than 5 V swings and 1 MΩ loads.

Figure 5.6 illustrates the pin driver output waveform of a 100 Mb/s pattern with a 50% duty cycle and a peak-to-peak voltage swing of approximately 800 mV (ECL-like). The duty cycle for the Vo+ waveform is 50.26% which is close to the desired value of 50% (D_{11}-D_0=010101010101). The Vo- duty cycle is also very close to the desired 50% value. Slight ringing (overshoot and undershoot readings) is present on the waveforms and is expected since the trace impedance from the pin driver output to the DUT SMA connector is not 50 Ω, but 62 Ω. Also, the Vo+ output is biased slightly more positive ($\cong 40mV$) than the Vo- output. This will cause the switching point of a **differential** DUT to be offset as illustrated in Figure 5.4 and therefore the (**differential** only) duty cycle will not be the desired 50%.

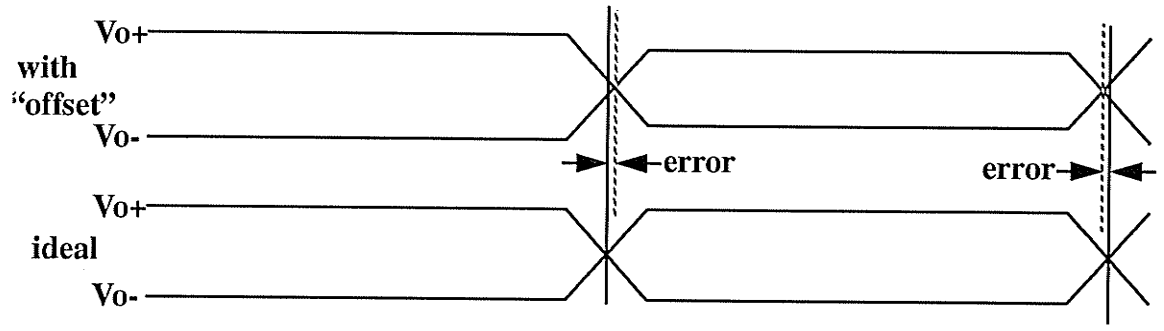

Figure 5.4: Pulse width distortion error.

This non-50% duty cycle is called *pulse width distortion* and will cause timing errors

if this waveform is used as an input into a differential DUT. The offset maybe caused by unbalanced bypassing or perhaps the differential inputs into the pin driver are unsymmetrical. This problem was not investigated any further, but it manifests itself even further at higher bit rates.

Figure 5.7 illustrates the pin driver output waveform of a 500 Mb/s pattern with a 50% duty cycle. The peak to peak voltage swing for the Vo- and Vo+ output is 1.072 V 0.990 V respectively. The Vo+ ouput's logic "zero" level (V_{OL}) is higher than the Vo- output logic "zero". There is also more ringing, undershoot and overshoot, on the Vo- output than an the Vo+ output. This may be due to a larger discontinuity at the Vo- SMA connector pin via. As mentioned in chapter four, wire wrap wire was soldered between the SMA signal pin and the disconnected trace. Also, the threshold crossing of the differential outputs do not occur at the center of the waveforms. This is caused by the previously mentioned offset but also because the cable lengths may be off and also the tolerances of the transmission lines. This error may be removed with the use of the variable delay lines.

Figure 5.8 illustrates the pin driver output waveform of a 1.0 Gb/s pattern with a 50% duty cycle and also the 1.0 GHz HF clock (CLKIN). The peak to peak voltage swing of the Vo+ and Vo- output is 780 mV and 824mV respectively. As before, this unequal peak to peak swing will cause a non 50% duty cycle for a differential DUT. Also, the pulses have become rounded and are effectively sine waves due to the scope bandwidth. Figure 5.9 illustrates the pin driver output waveform of a 1.20 Gb/s pattern with a 50% duty cycle. The offset on the Vo+ is even larger than on previous measurements.

Figure 5.10, Figure 5.11 and Figure 5.12 illustrate the pin driver output of a 25% (D_{11}-D_0=000100010001) duty cycle (Vo- = 75% duty cycle) pattern at 500, 750 and 1200 Mb/s respectively. The offset problem is still visible in all the waveforms. Figure 5.13 illustrates the 1.2 Gb/s pattern at a different time base (500 ps/division)

and as seen the unequal threshold voltage is still evident.

In summary, the pin driver's output waveforms would be unsuitable for differetial circuits because of the pulse width distortion it would cause. As mentioned, this problem was not investigated further. The pin driver's waveforms would be suitable for testing **single ended** circuits. The duty cycle of a single ended pin driver output, be it either Vo+ or Vo-, were stable and did not exhibit pulse width distortion as they do when the outputs are combined as a differential pair. Although the signal integrity of the outputs indicate that they are suitable for testing, the ringing must be quantified with a higher bandwidth scope.

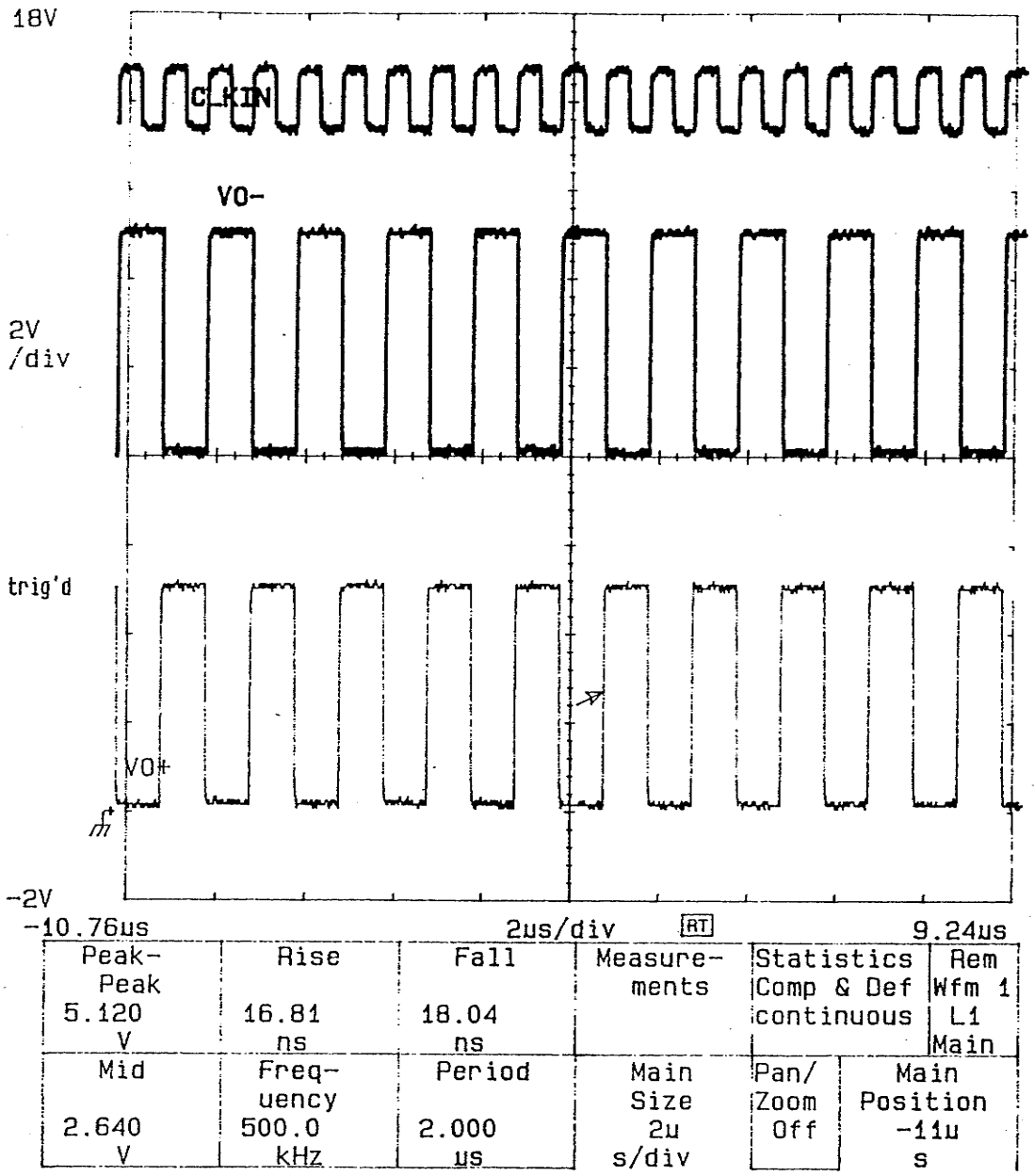

Figure 5.5: A 50 % duty cycle (D_{11}-D_0=010101010101) 1 Mb/s pattern with a 5.12 V (CMOS-like) peak-to-peak swing .

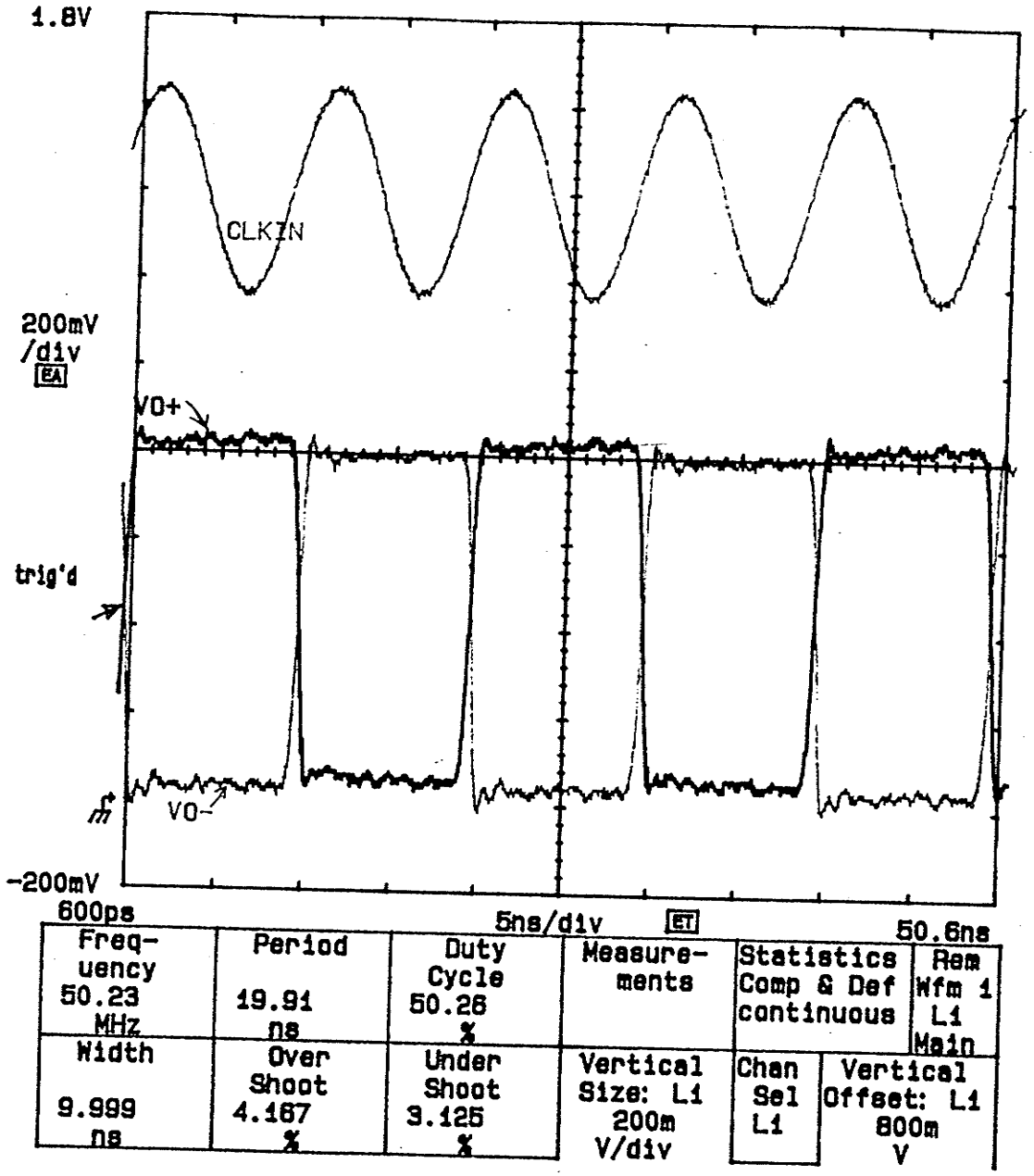

Figure 5.6: A 50 % duty cycle (D_{11}-D_0=010101010101) 100 Mb/s pattern with a 0.810 V (ECL-like) peak-to-peak swing .

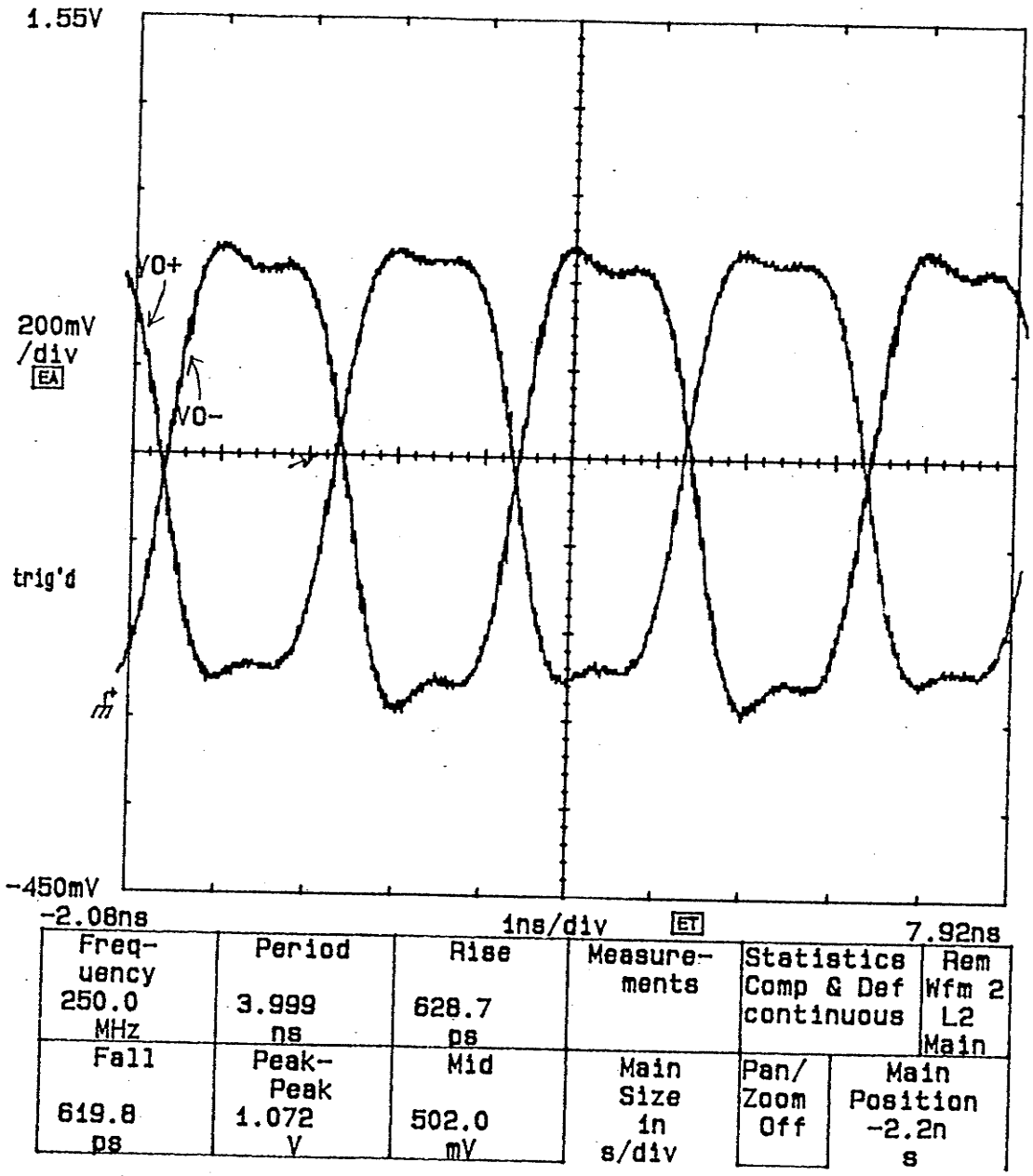

Figure 5.7: A 50 % duty cycle (D_{11}-D_0=010101010101) 500 Mb/s pattern with a 1.072 V (Vo-,ECL-like) peak-to-peak swing .

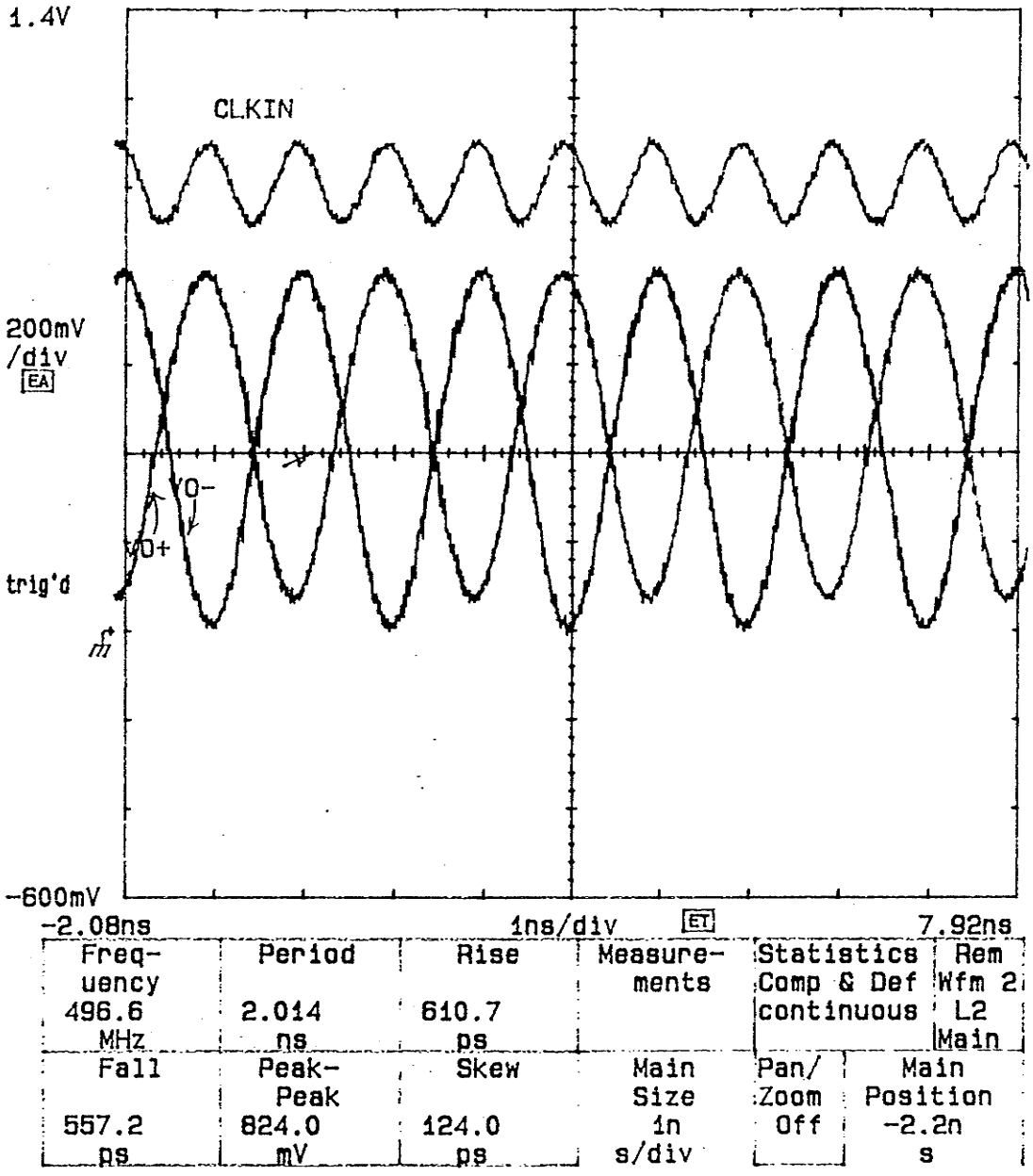

Figure 5.8: A 50 % duty cycle (D_{11}-D_0=010101010101) 1000 Mb/s pattern with a 0.824 V (Vo-,ECL-like) peak-to-peak swing .

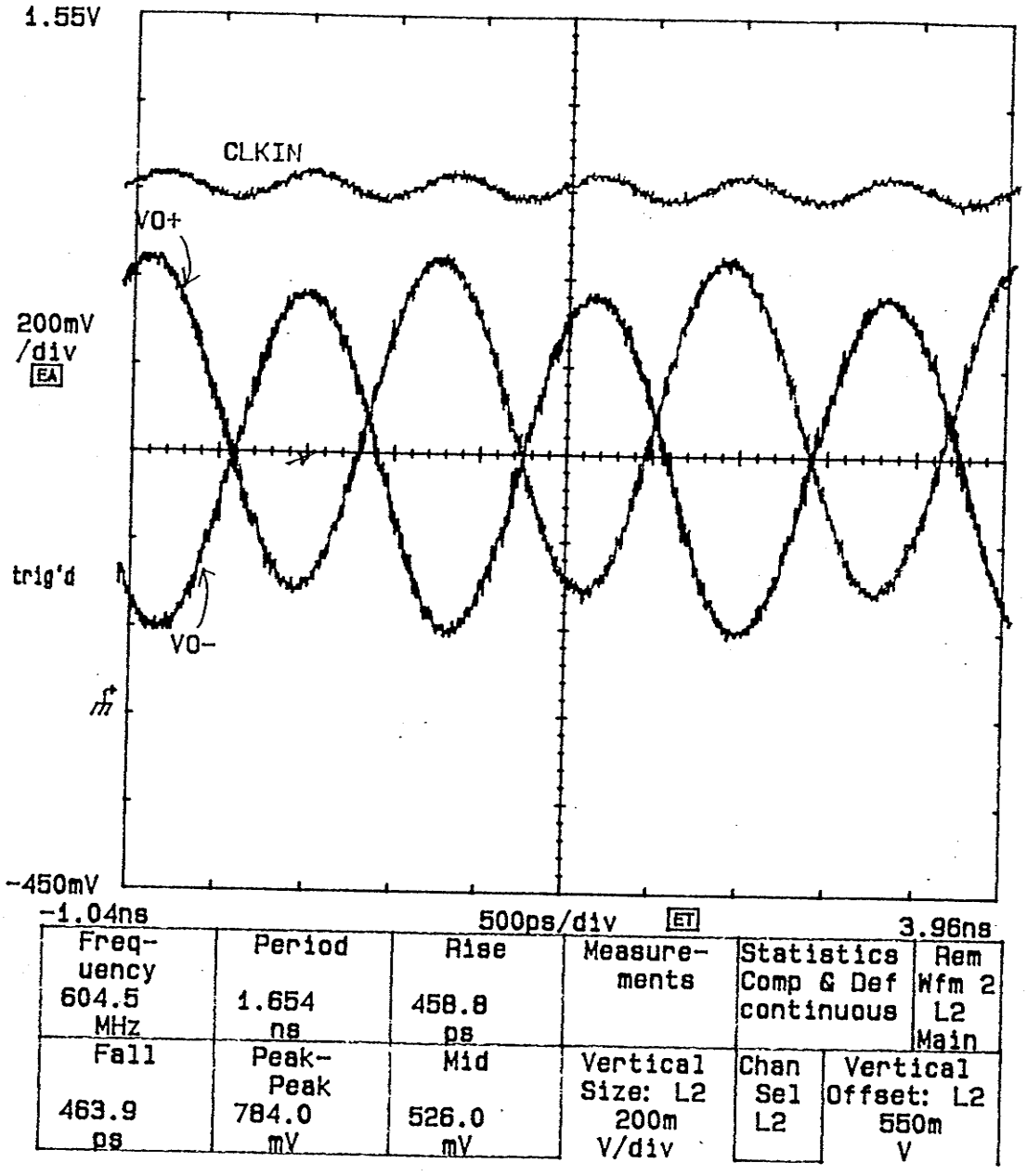

Figure 5.9: A 50 % duty cycle (D_{11}-D_0=010101010101) 1200 Mb/s pattern with a 0.784 V (Vo-,ECL-like) peak-to-peak swing .

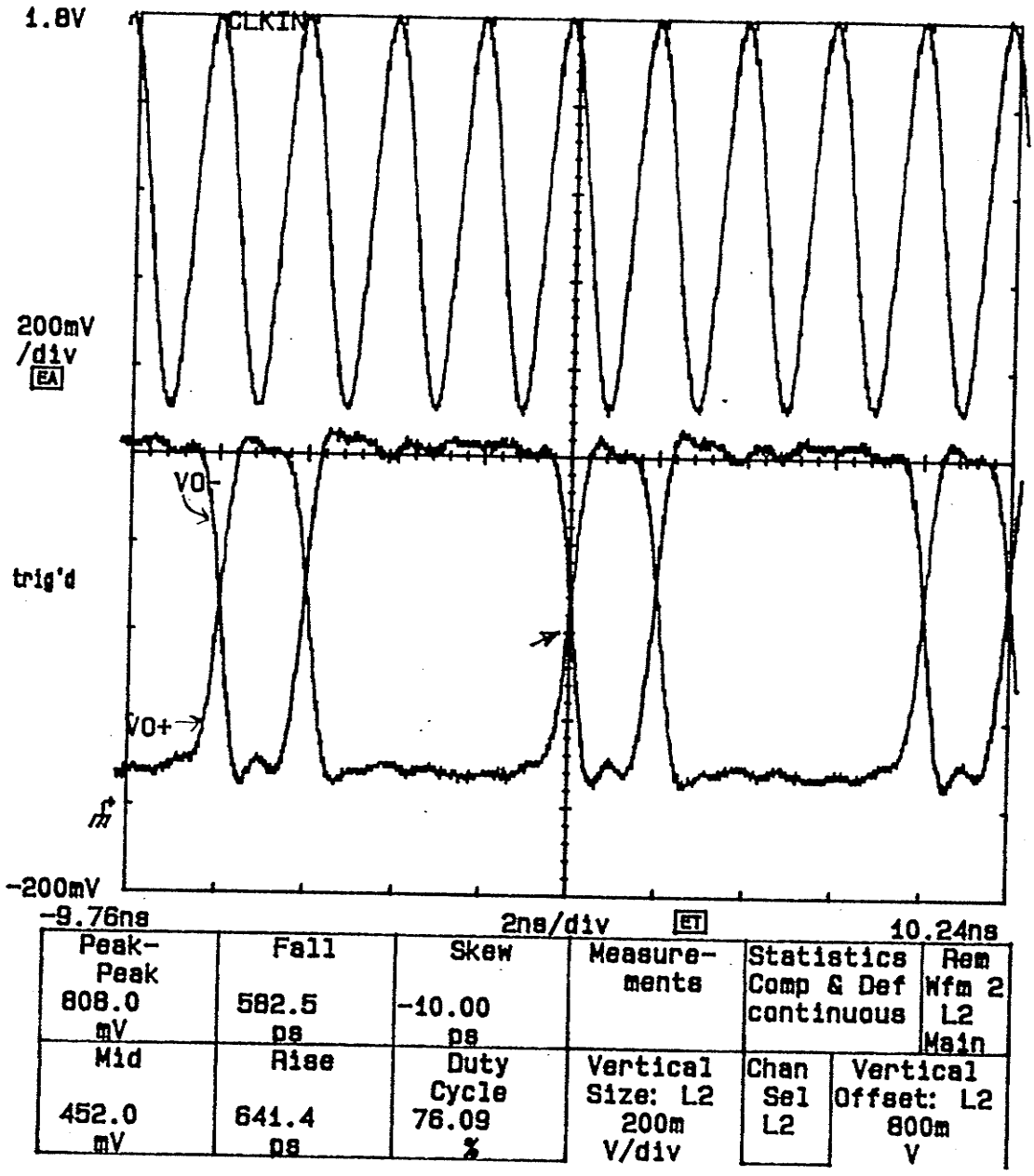

Figure 5.10: A 25 % duty cycle (D_{11}-D_0=000100010001), 500 Mb/s pattern with a 0.808 V (ECL-like) peak-to-peak swing.

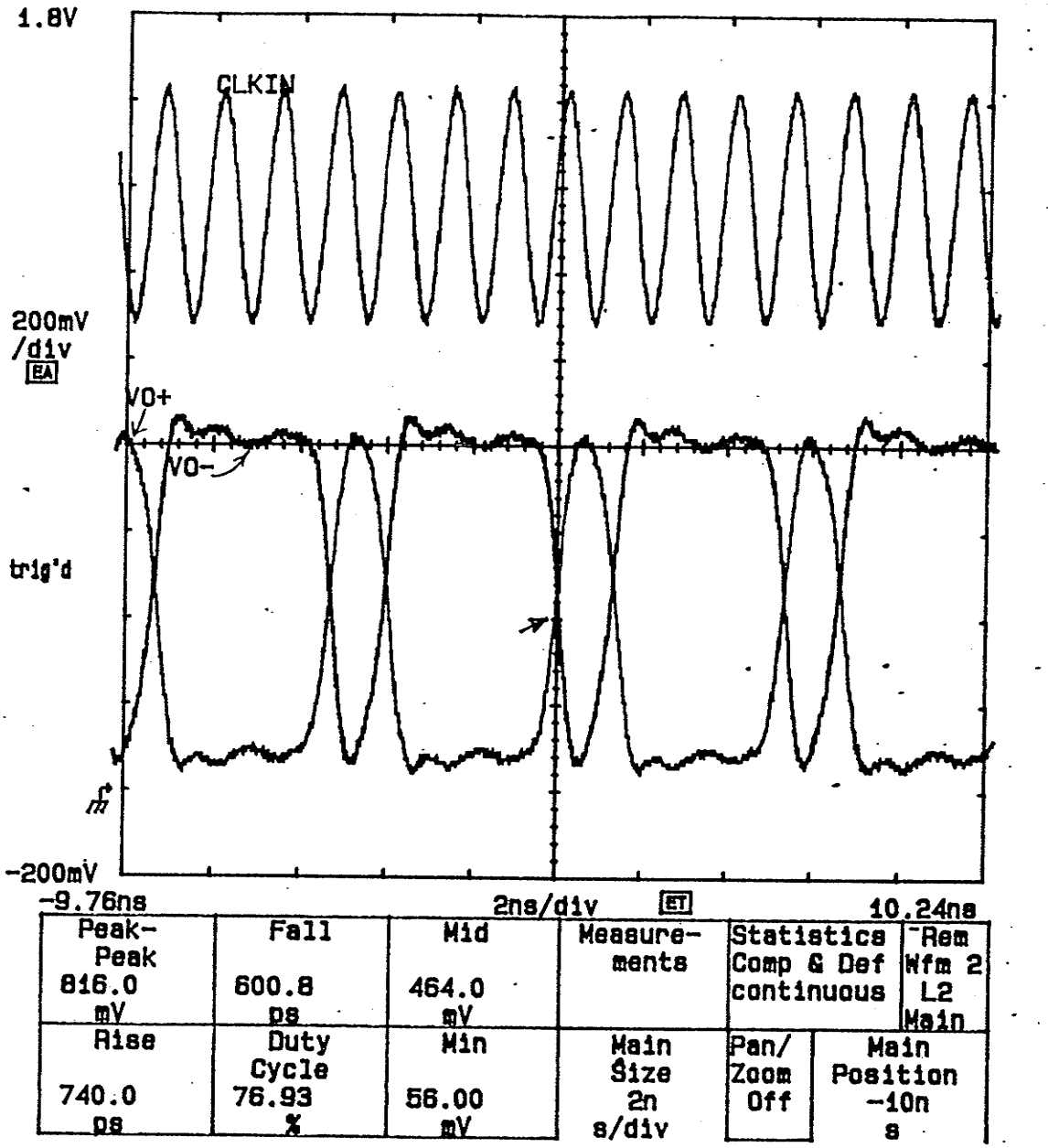

Figure 5.11: A 25 % duty cycle (D_{11}-D_0=000100010001), 750 Mb/s pattern with a 0.816 V (Vo-,ECL-like) peak-to-peak swing.

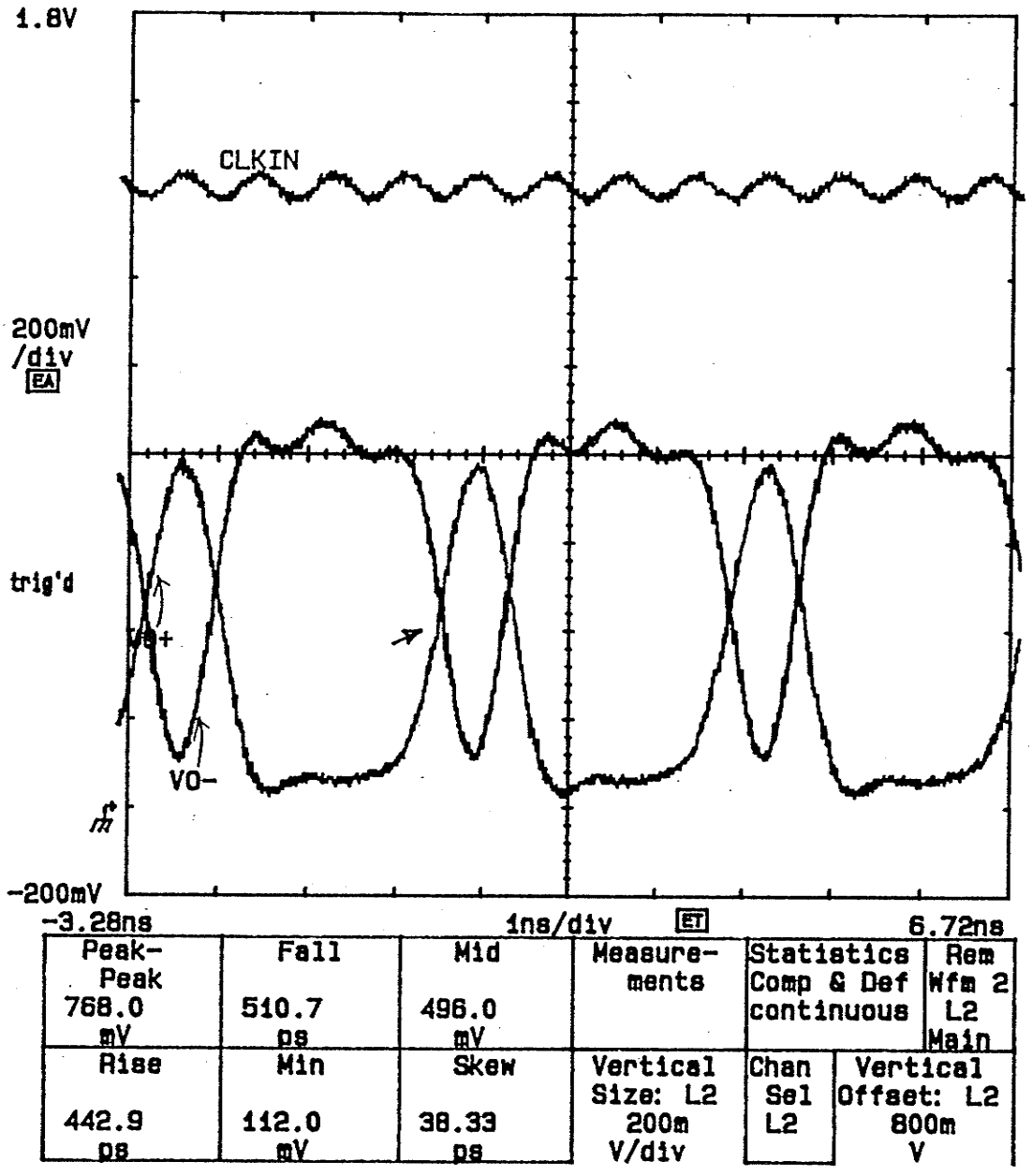

Figure 5.12: A 25 % duty cycle (D_{11}-D_0=000100010001), 1200 Mb/s pattern with a 0.768 V (Vo-,ECL-like) peak-to-peak swing.

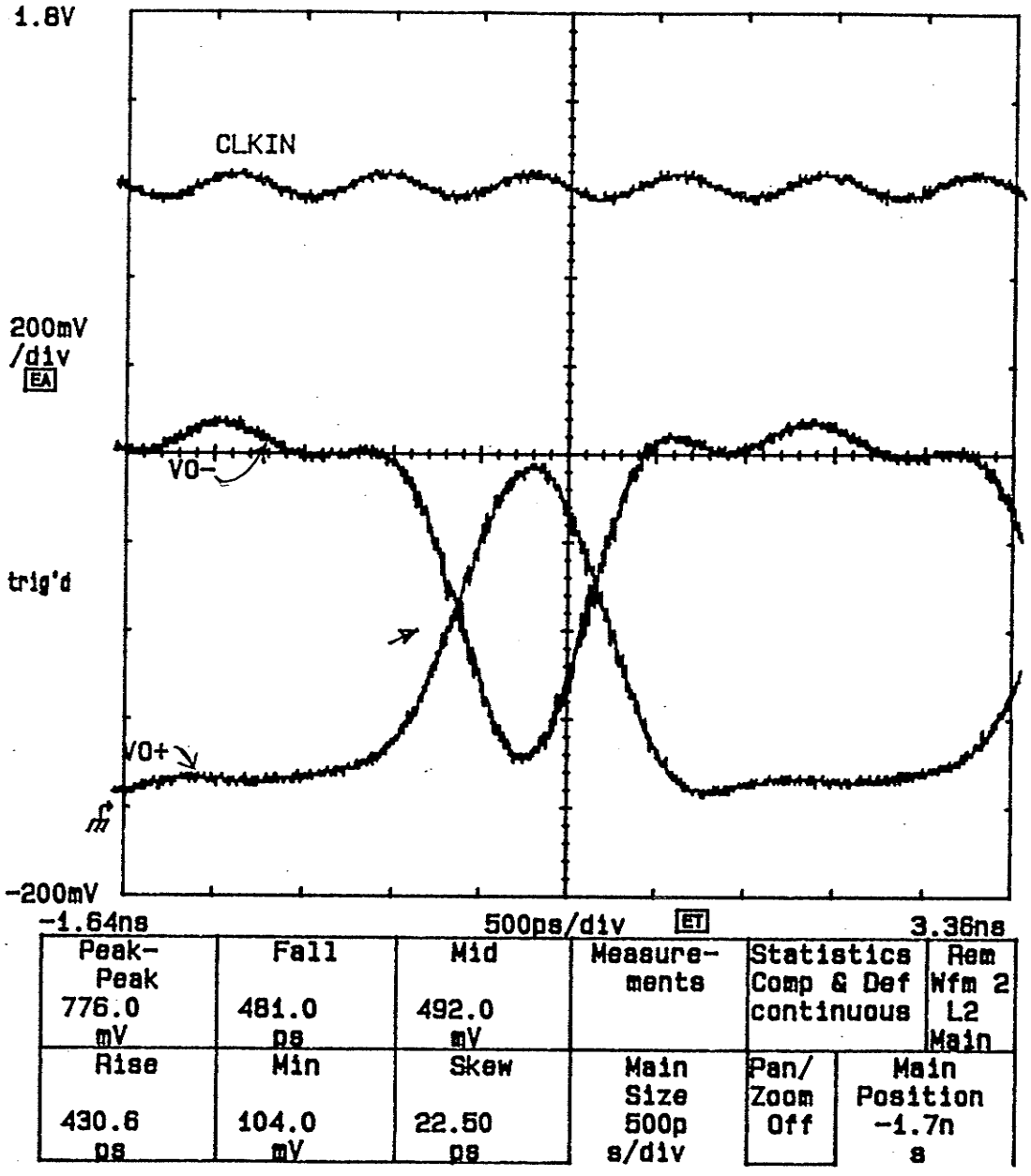

Figure 5.13: A 25 % duty cycle (D_{11}-D_0=000100010001), 1200 Mb/s pattern with a 0.776 V (Vo-,ECL-like) peak-to-peak swing (500ps/div).

5.2.1 Variable Delay Lines

The variable delay lines can be used to align the edges on the pin driver's differential output to compensate any imbalances in loading and cable length differentials which were evident in the pin driver output waveforms previously discussed. A practical example is when one tester channel is driving a different capacitive load than the second channel. Typically, DUT clock or select inputs have a larger capacitive load (~ 5pf for ECL) than data inputs (1-2.5 pF for ECL). The input waveform at the DUT clock (or select) input will have its rising or falling edge degraded (delay=Z_o*C_{Load}) more than the input waveform at the DUT data input. Hence, the switching points (threshold voltage) between data and clock (select) inputs will be misaligned and this results in a timing error. The delay lines can minimize the error caused by the load imbalance by aligning the edges or switching points to within 50 ps.

The variable delay lines also provide the capabilities of verifying asynchronous circuit parameters such as set up (t_s) and hold (t_h) times. Figure 5.14 illustrates a configuration to test a D flip flop where both tester channels are required. One channel (channel #2) is configured as the flip flop's clock (CLK) and the other channel (channel #1) as the data input (D). The delay lines provide the capability of shifting the clock or data to measure, within 50 ps, the setup (t_s) and hold (t_h) time of the D flip flop.

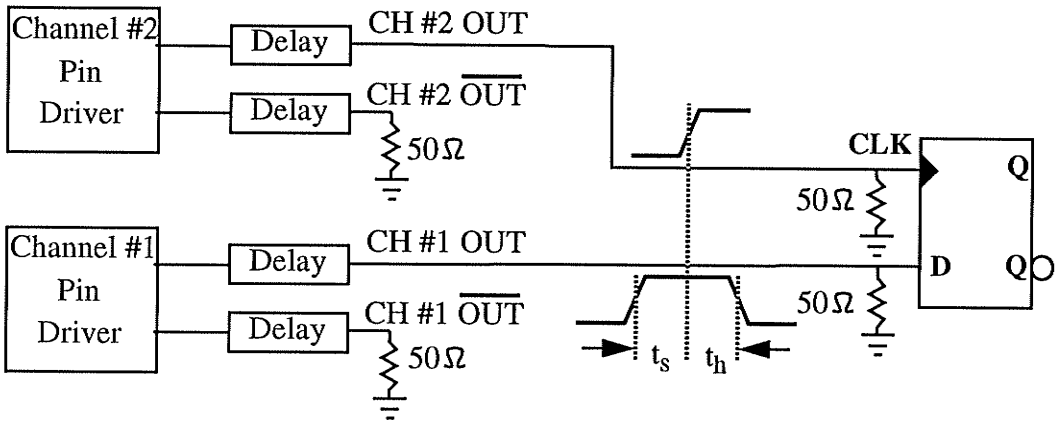

Figure 5.14: D flip flop set up and hold measurement setup.

5.2.2 Pin Driver Rise and Fall Time

The rise and fall time of the Triquint pin driver is specified at 150 ps (20 - 80%) while driving a 50 Ω load (1 V swing & <1pf load) [60]. For an ECL-like voltage swing (~800 mV) the measured 20-80% and 10-90% rise time is 684 ps and 912 ps respectively and shown in Figure 5.15. This measurement is erroneous since the oscilloscope (amplifier) is bandwidth limited at 400 MHz. A rough estimation of the pin driver rise time can be calculated using composites [41]. This method is often used to approximate the rise time of an input waveform into a scope or chain of amplifiers. Each component between the pin driver and the oscilloscope will degrade the rise time of the pin driver input. Since the components are in series, each component's rise time (t_r = 0.35/bandwidth) is squared and then added together as shown in Equation 5.2.

$$T_{composite} = \sqrt{T_1^2 + T_2^2 + \ldots + T_N^2} \tag{5.2}$$

The actual rise time is calculated by subtracting the composite rise time ($T_{composite}$) from the rise time displayed ($T_{displayed}$) by the oscilloscope and is given in the equa-

tion below.

$$T_{\text{actual}} = \sqrt{T^2_{\text{displayed}} - T^2_{\text{composite}}} \tag{5.3}$$

Figure 5.16 illustrates all the components in the chain and Table 5.1 shows all respective composite rise times.

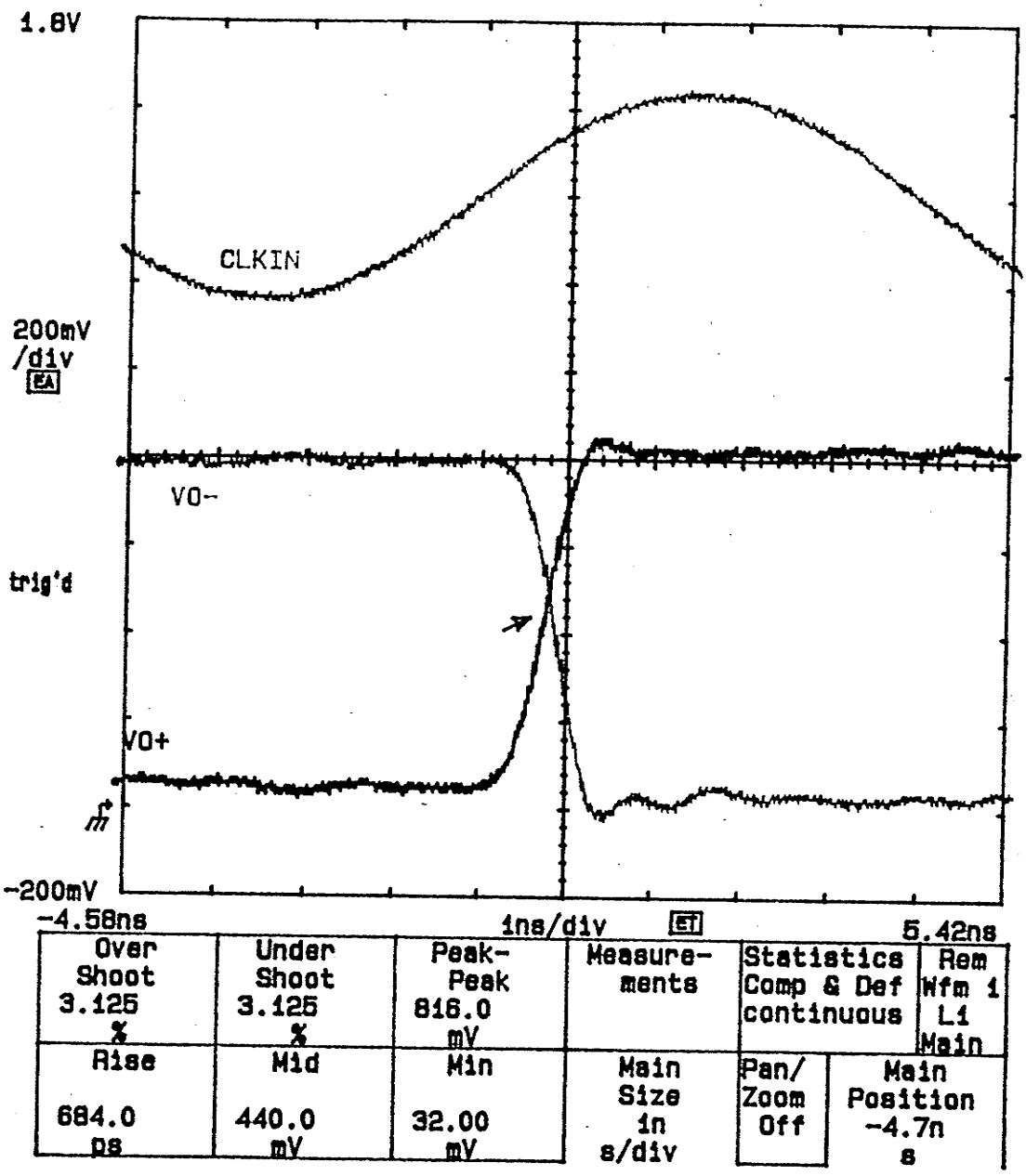

Figure 5.15: Pin driver rise time measurement.

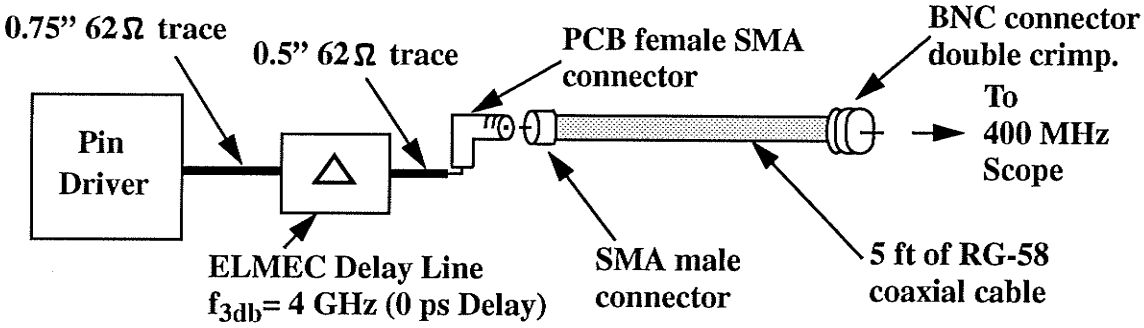

Figure 5.16: Components in the delay path.

Table 5.1: Composite rise times of components in the pin driver chain.

Component	Composite t_r (10-90%) (ps)
ELMEC Delay Line (4 GHz @ 0ps delay)	87.5
SMA PCB female connector	13
SMA male connector	13
5 ft. RG-58 coax	38
1.25 inches of trace (BW 2.5 GHz)	140
BNC male coax (RG-58) connector	22
Tektronix 11A32 input amplifier (400 MHz)	875
	$T_{composite} = 892\ ps$

The calculated rise time (10-90%) is presented in Equation 5.4.

$$191\text{ps} = \sqrt{(912\text{ps})^2 - (892\text{ps})^2} \tag{5.4}$$

The resulting 20-80% rise time is 143 ps and is very close to the specified 150 ps. The calculated rise time is a very crude estimation since one of the requirements for using composites is that the input waveform have no overshoot or undershoot and be taken in a noise free environment. Nevertheless, it offers some insight into the actual rise time of the pin driver and is a quick method of approximating measurements when

high bandwidth measuring equipment is not available.

5.2.3 GaAs 2:1 Multiplexer Revisited

Since the purpose of designing the tester was to test high speed ICs, the 2:1 GaAs multiplexer discussed in chapter two was retested. The results will illustrate the advantages of the tester over the hybrid test setup discussed previously. A 200 Mb/s data stream with a 50% duty cycle was inputted into channel A of the multiplexer and the resulting output is illustrated in Figure 5.17.

The output waveform has a peak-to-peak voltage of ~ 1.1 V and reveals a characteristic of the multiplexer that was impossible to measure with the hybrid test equipment. The data stream inputted into the multiplexer duty cycle is approximately 50%, but the resulting multiplexer output has a 58% duty cycle. This shows that there is an imbalance in the delays within the 2:1 multiplexer. This imbalance causes the multiplexer to stay in the high state longer than the low state and hence the higher duty cycle. The high-to-low transition takes longer to propagate through the multiplexer than the low-to-high transition. This is probably due to the unbalanced loading, from parasitic capacitances, within the IC.

This effect becomes more evident as the bit rate is increased to 500 Mb/s as displayed in Figure 5.18. The multiplexer output resembles more of a triangle rather than a square pulse. The functionality of the multiplexer degrades drastically as the bit rate is increased further. A difference between the multiplexer output waveforms in Figure 2.7 and Figure 5.17 are the rise time portion of the pulses. Due to the lack of bandwidth with the current equipment, the "kink" in the rise portion which is visible in Figure 2.7 is not evident in Figure 5.17.

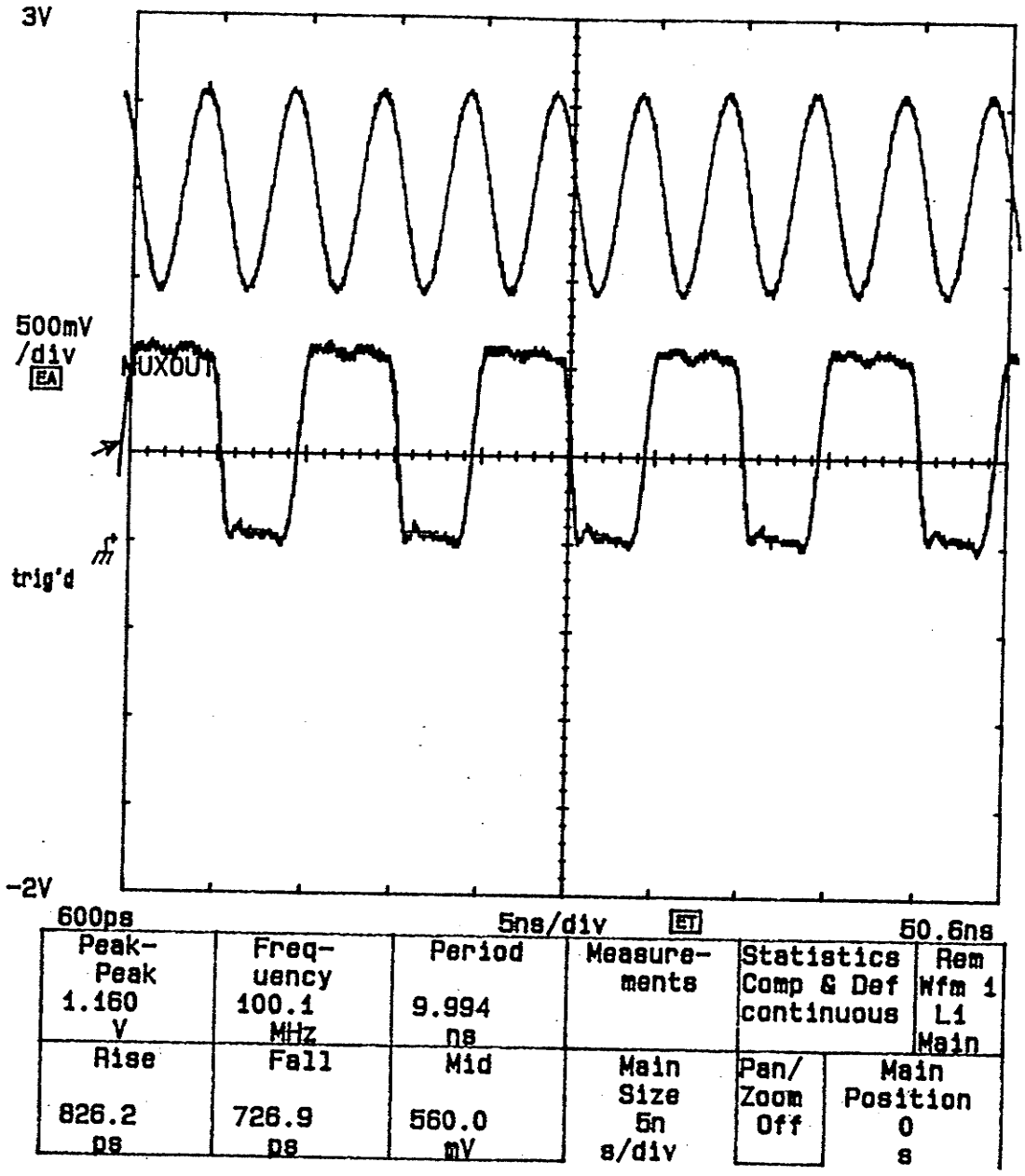

Figure 5.17: GaAs 2:1 Multiplexer output at 200 Mb/s.

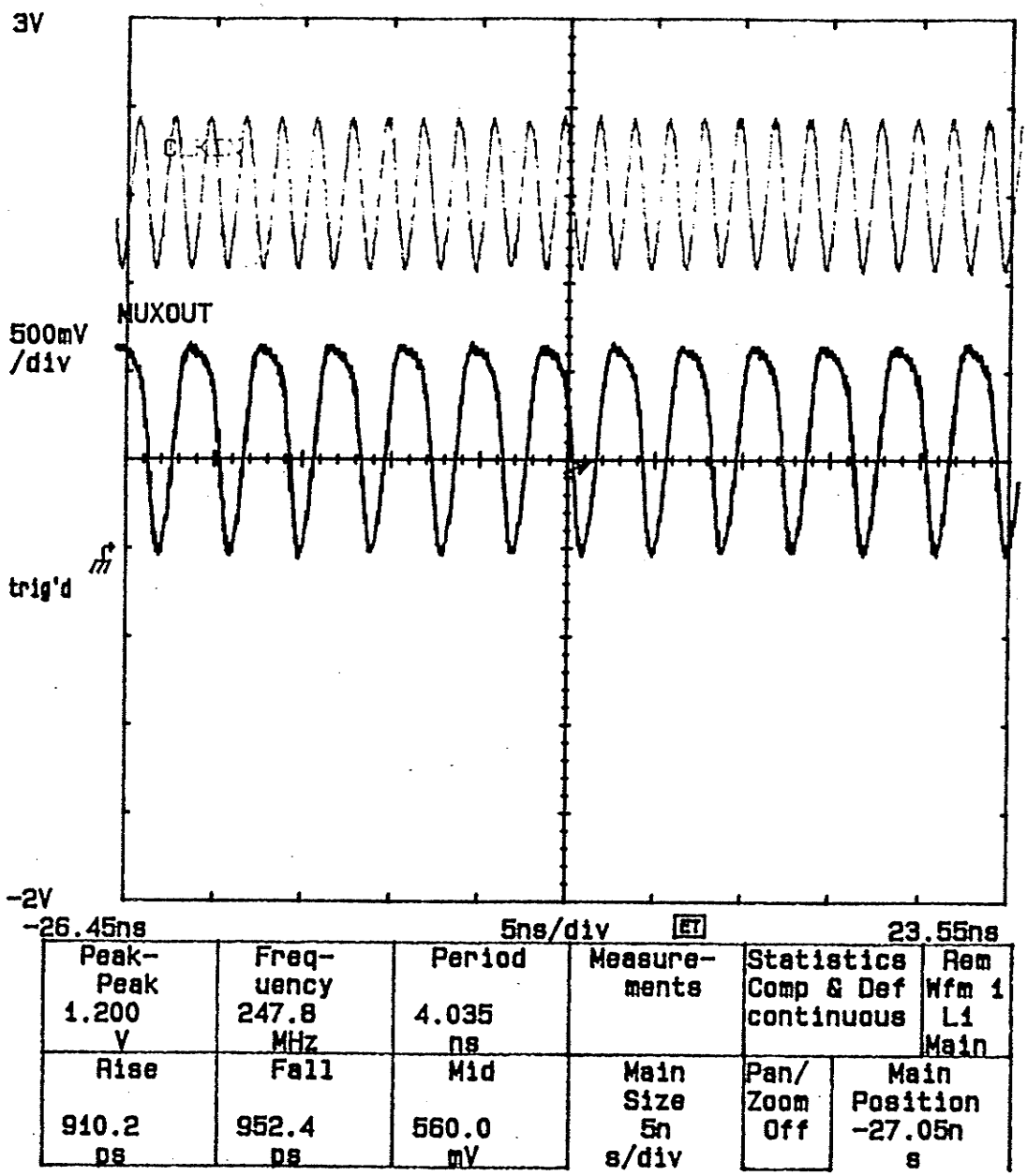

Figure 5.18: GaAs 2:1 Multiplexer output at 500 Mb/s.

5.3 Future Testing

The previous sections illustrated that the tester can provide waveforms which are suitable for functional testing of **single ended** high speed ICs. At higher frequencies (>1 Gb/s) the tester's output waveforms would not be suitable if tight timing accuracy was required. Ultimately, the true measure of a tester is timing accuracy. The timing accuracy of a complete test system would include errors introduced by the pattern generator and the capture and store. Typically, the major part of timing errors are from the capture and store section. In the tester's case, only timing errors due to the pattern generator will be discussed. The whole system must be completely operational to completely characterize the tester. The software - microcontroller and Microsoft Windows^{TM} (PC) interface - must be completely integrated into the system. Once that is completed the tester characterization can be accomplished.

One problem that must be investigated, which is a GaAs IC anomaly, is a pulse narrowing effect. This pulse narrowing effect, caused by the "GaAs MESFET hysteresis", has been well documented [10,61-62] and is an issue that must be addressed when utilizing GaAs ICs in the pattern generation section of an ATE. The pulse narrowing effect occurs because a GaAs circuit seems to remember the "off" state for some time and slowly adjusts to the continuous switching state. For testing applications, this turns into pattern sensitivity, the first pulses in a starting pulse train are smaller than succeeding pulses. So whenever the duty cycle of the signal varies with time, the edge placement varies [61] as illustrated in Figure 5.19. This effect can lead to an edge placement error of hundreds of picoseconds [10,61]. IC fabrication process methods and the utilization of control loops circuitry have been utilized to decrease the edge placement error to below 35 ps [61-62]. Since the *high frequency path* uses GaAs ICs exclusively, it is imperative that the pulse narrowing effect be quantified. This effect would probably be the pattern generator's largest error in terms of edge placement.

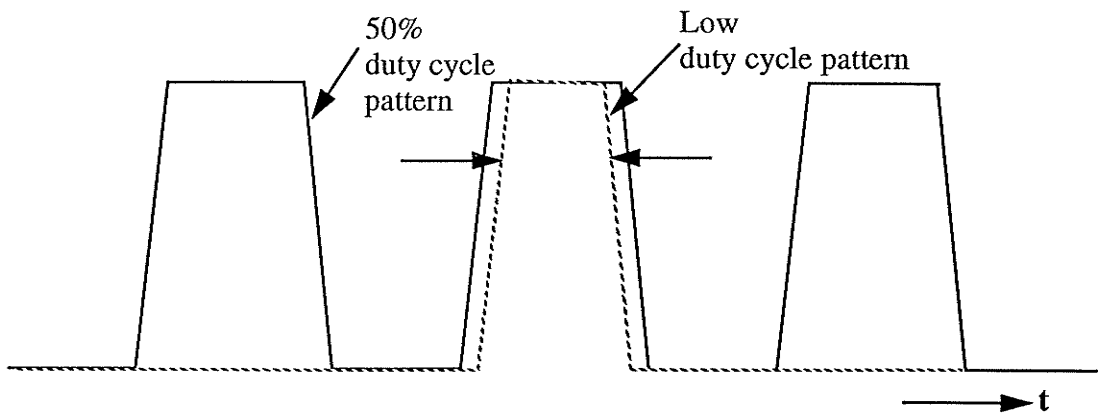

Figure 5.19: Pulse narrowing effect caused by MESFET hysteresis.

Another part of the system that must be thoroughly tested is the proposed PLL board. A phase noise and jitter analysis is required and can be performed with a high bandwidth scope or a RF spectrum analyzer. Also, once the PLL has been characterized an eye diagram analysis must be performed. This requires the tester to output a pseudo random test pattern out of one channel and a low frequency clock out of the other channel. The low frequency clock, bit rate divided by twelve for example, is required to trigger an oscilloscope so that the pseudo random pattern can be viewed. The oscilloscope will display the pattern, or eye diagram, similar to that shown in Figure 5.20. The eye diagram will illustrate any pulse narrowing effects and jitter which results in edge placement timing errors.

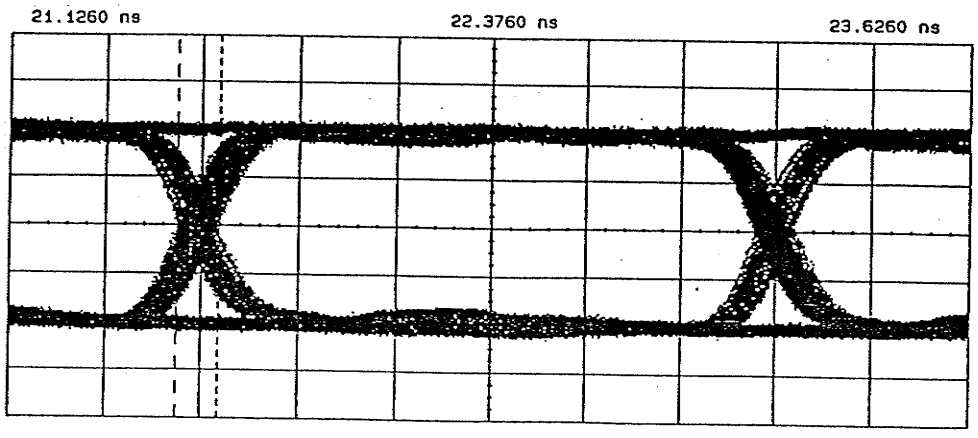

Figure 5.20: Eye diagram of a pseudo random pattern [61].

Chapter 6.0

Conclusions and Recommendations

This thesis has illustrated the design and construction of an ultra high speed functional digital IC tester. Some of the design goals discussed in chapter two have been met, but due to a lack of time complete system integration (software, PLL clock generation) was not possible. One *high frequency path* (channel) was successfully tested. The pin driver's output waveforms were suitable for testing single ended circuits up to the maximum bit rate of 1.20 Gb/s. Unfortunately, the pin driver's differential output's were unsuitable for testing differential circuits at higher bit rates (> 750 Mb/s). The worst case timing criteria was met (Section 4.5) and most electrical design specifications were met. Unfortunately, one issue that is crucial for system functionality and must be addressed is the design of the Address bus. As discussed in chapter four, under worst case operating conditions crosstalk and other noise sources are large enough to violate the ECL noise margin of the SRAM inputs. A new Address bus eliminating the SRAM IC sockets and utilizing stripline transmission lines is required. Hence, another tester PCB must be proposed and manufactured.

To provide four tester channels (pattern generator), utilizing the same architecture, a twelve layer PCB as illustrated in Figure 6.1 is proposed. Stripline transmission lines would be used exclusively and the use of IC sockets would be eliminated. Utilizing more signal layers, four rather than two, would allow routing of the Address bus on four layers and hence isolate adjacent bus lines. This would eliminate the Address bus crosstalk problem discussed in chapter four. Also, the first

and twelfth layers (component layers) would be used exclusively for component placement - no signal tracking allowed. This would allow closer placement of ICs and hence shorter propagation delays due to the shorter tracking required. The increase in the number of signal layers would also allow more efficient routing of both busses (Address and Data) and clock signals.

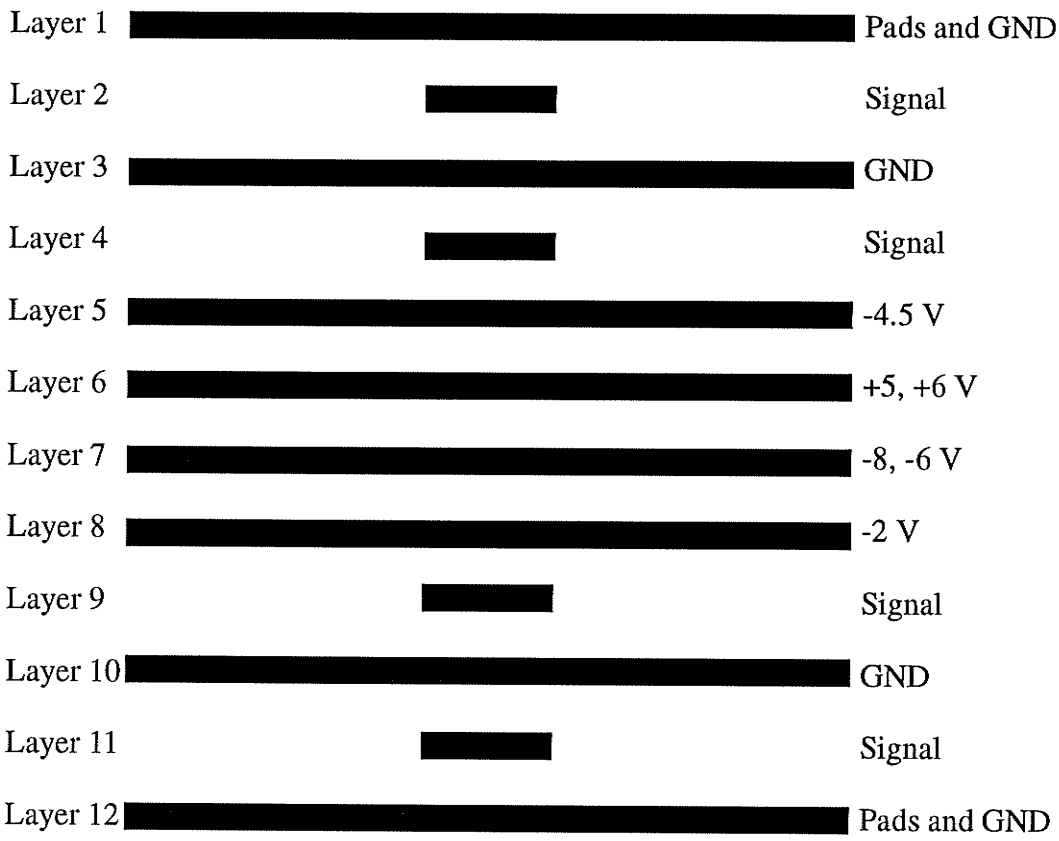

Figure 6.1: Proposed tester PCB stackup.

Another issue that would be addressed is the use of GaAs ICs on the tester. Recently, Motorola has developed an ECL 12:1 multiplexer and a 1:9 buffer capable of operating up to 1.20 Gb/s. The Gigabit (1:4 buffer) and Vitesse (12:1 multiplexer) GaAs ICs would be replaced by these Motorola ICs. This would eliminate the need for three power supply voltage levels (-3.4 V, -5.2 V and -1.32 V). The supply voltage levels required would be -4.5 V, -2 V, -6 V, -8V, + 5 V and +6V as illustrated in Figure 6.1. Another benefit of using ECL rather than GaAs ICs is that they are cheaper

and dissipate less power than the GaAs ICs. Also, the expected pulse narrowing caused by the MESFET hysteresis in GaAs ICs would be decreased since the pin driver would be the only GaAs IC remaining in the *high frequency path.*

Appendix

Figures A.1 - A.6 : Tester PCB artwork (layers 1 to 6).

Figures A.7 - A.8 : Power Supply PCB artwork (layers 1 to 2).

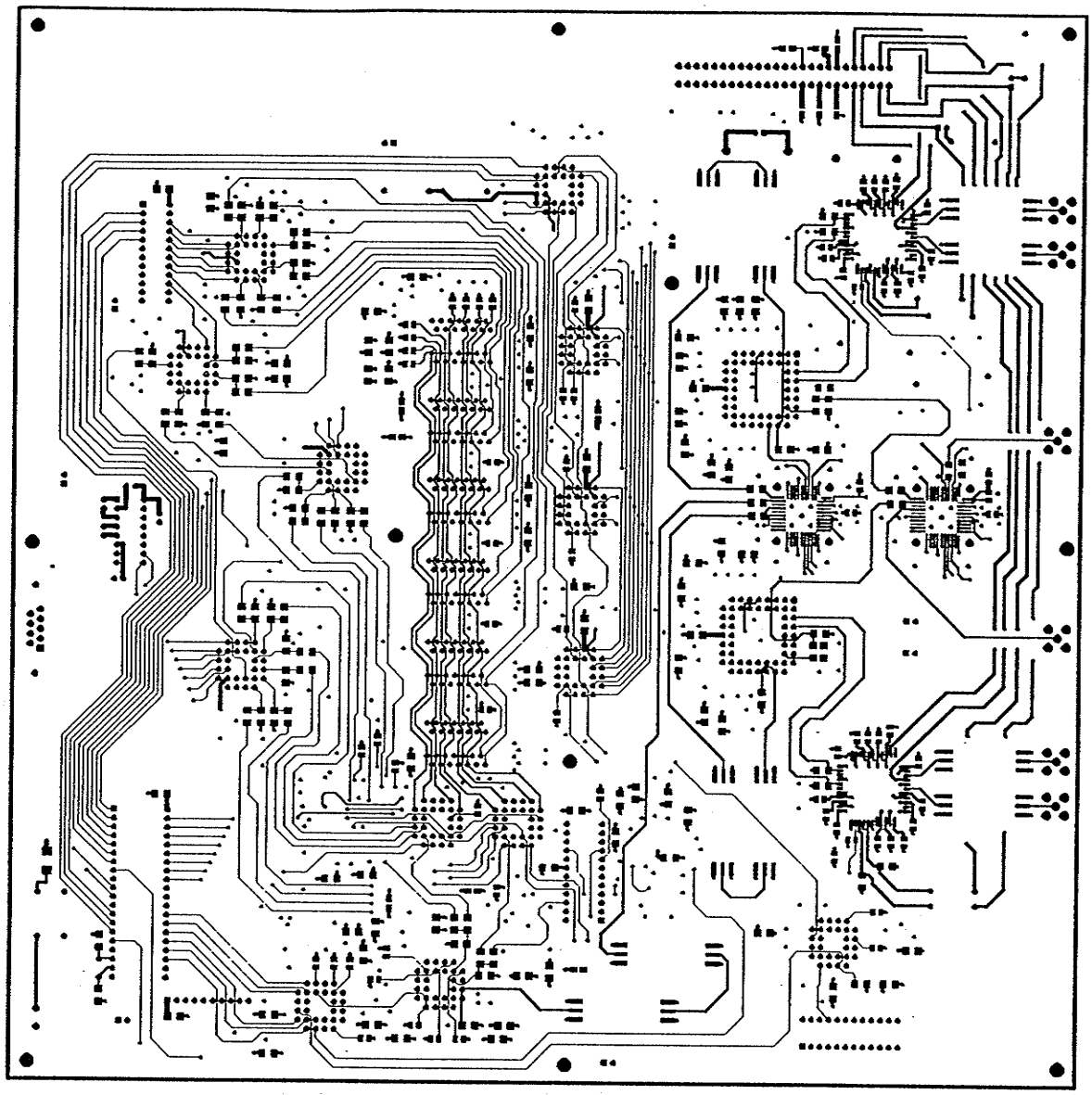

Figure A.1: Tester PCB artwork, layer 1 (2:1 scale).

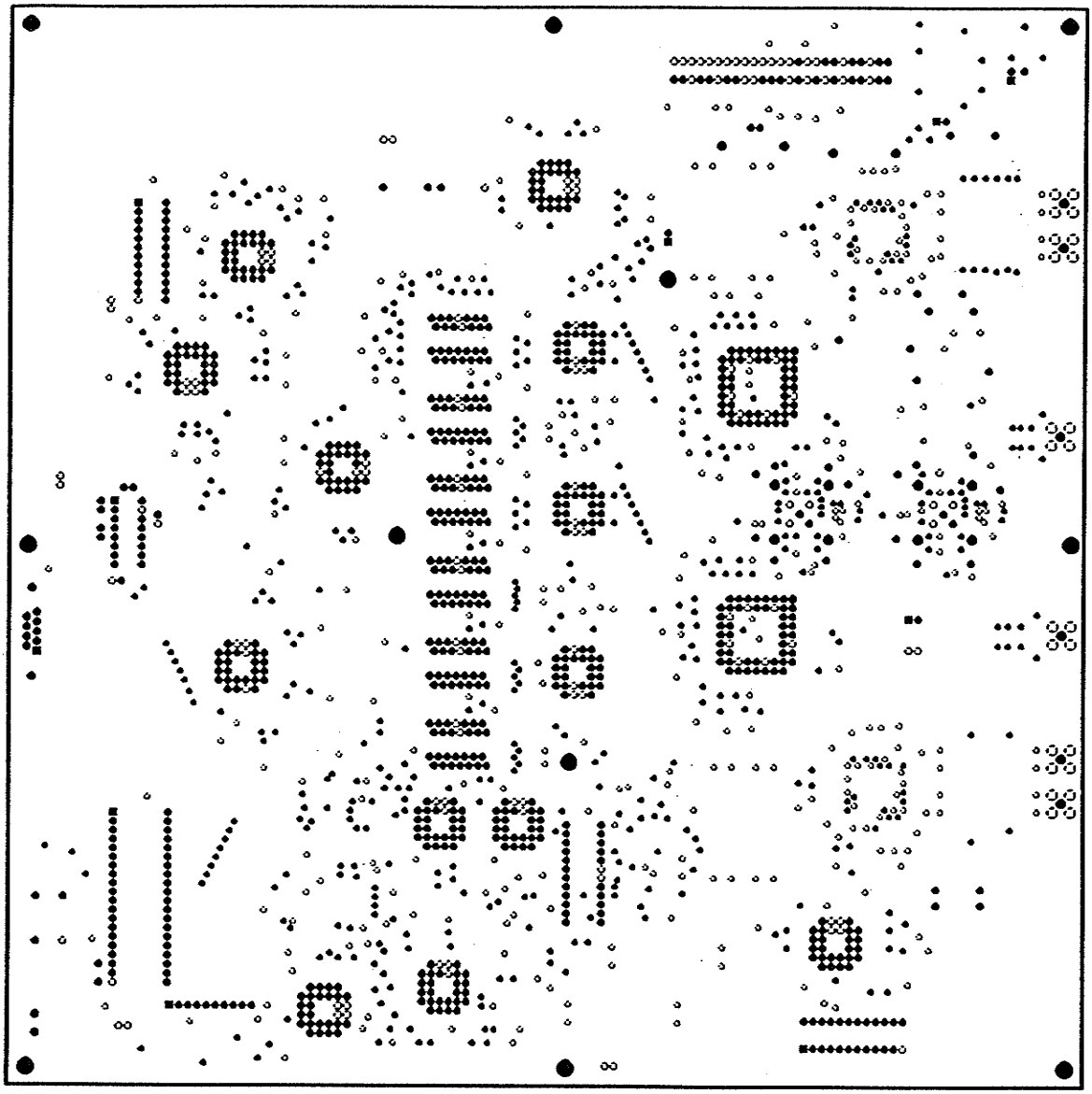

Figure A.2: Tester PCB artwork, layer 2 (2:1 scale).

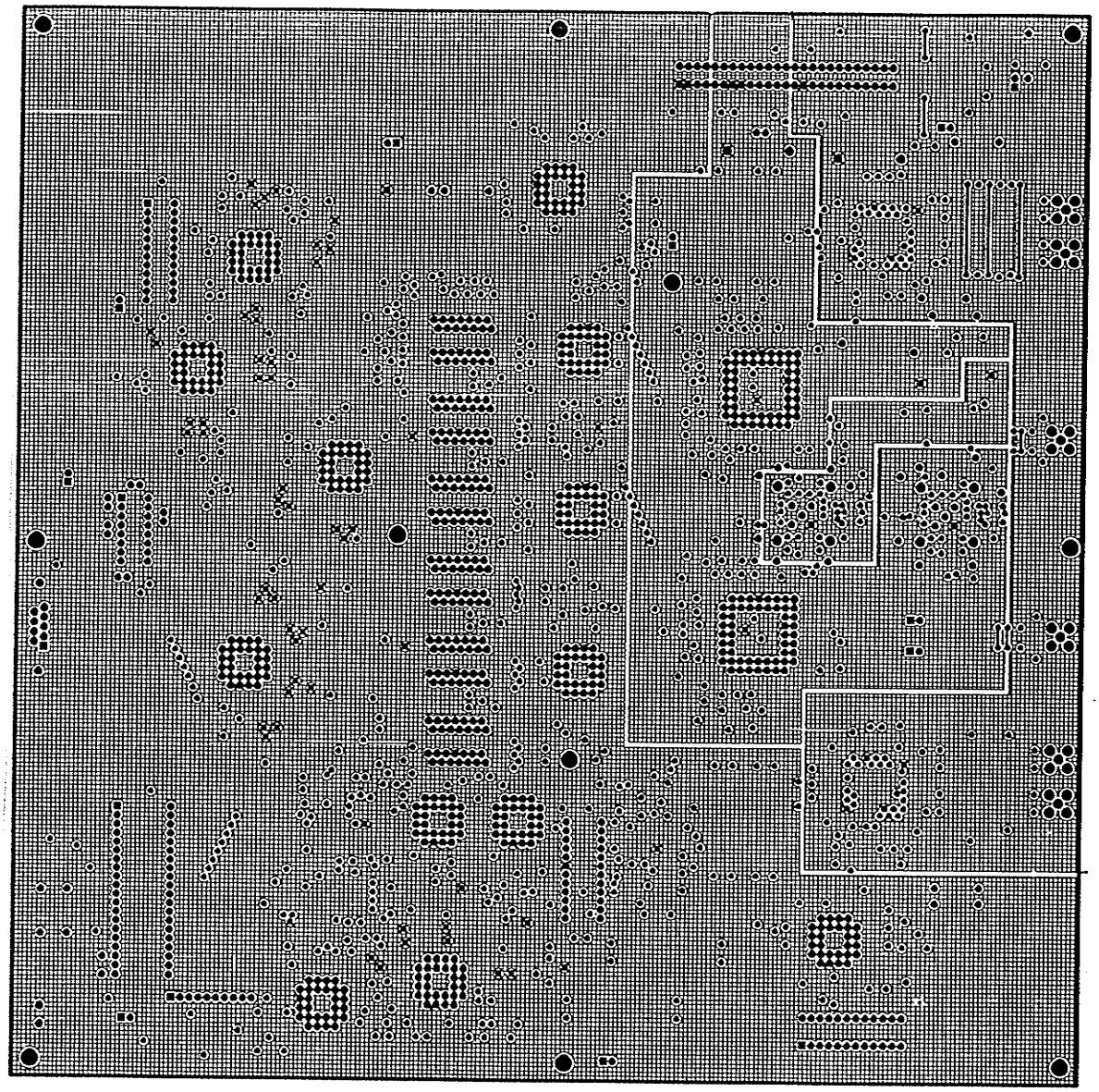

Figure A.3: Tester PCB artwork, layer 3 (2:1 scale).

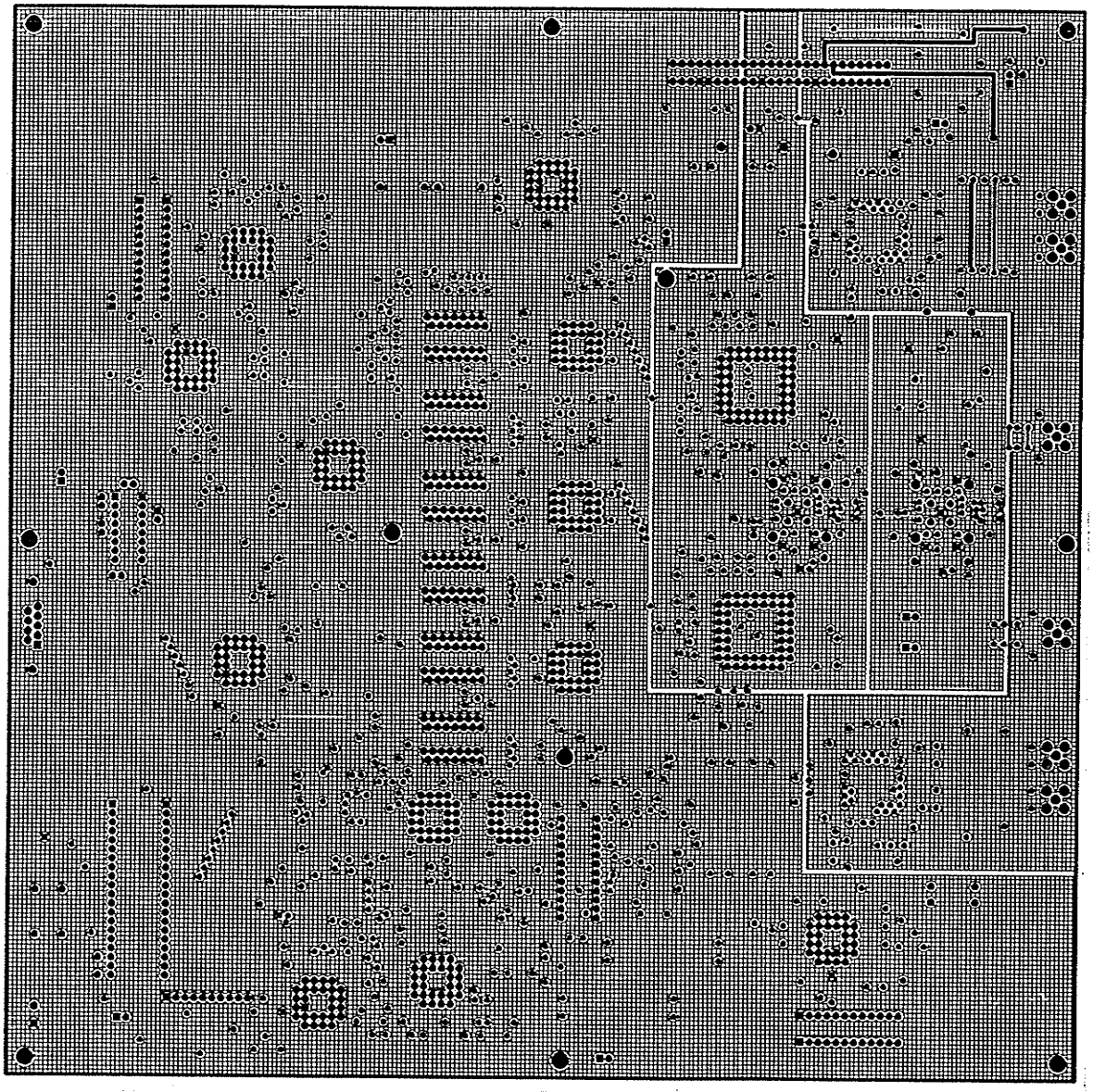

Figure A.4: Tester PCB artwork, layer 4 (2:1 scale).

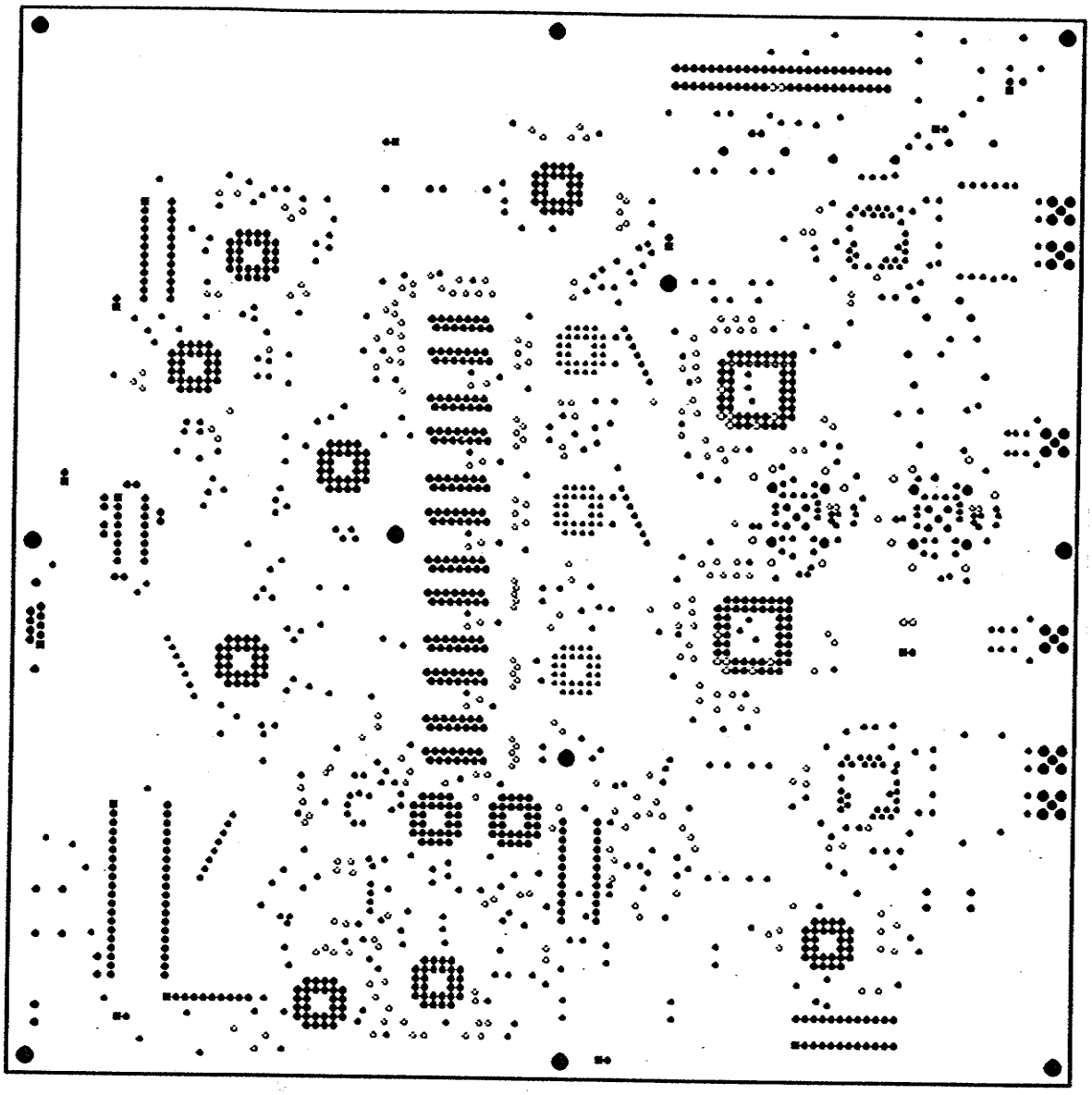

Figure A.5: Tester PCB artwork, layer 5 (2:1 scale).

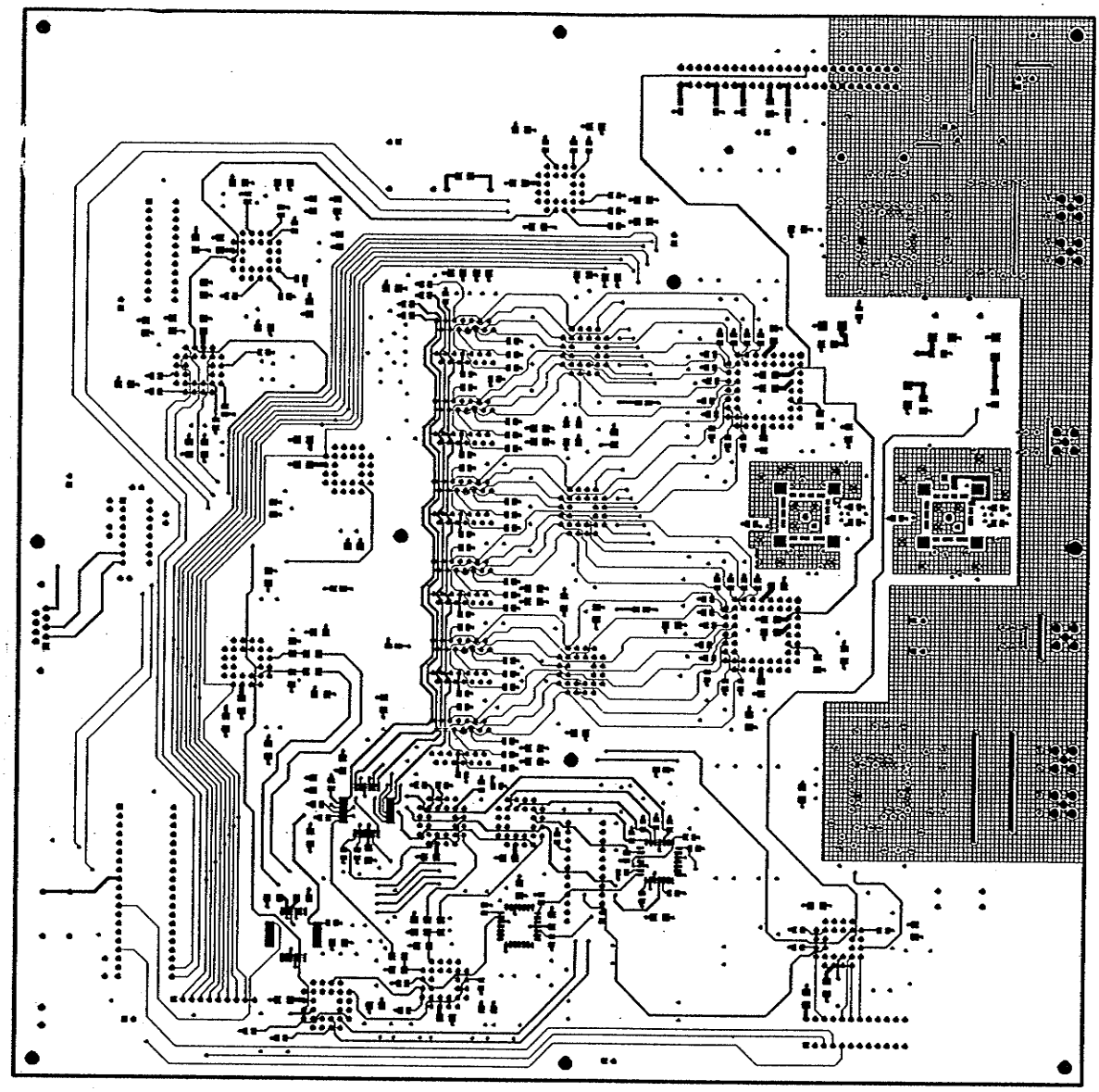

Figure A.6: Tester PCB artwork, layer 6 (2:1 scale).

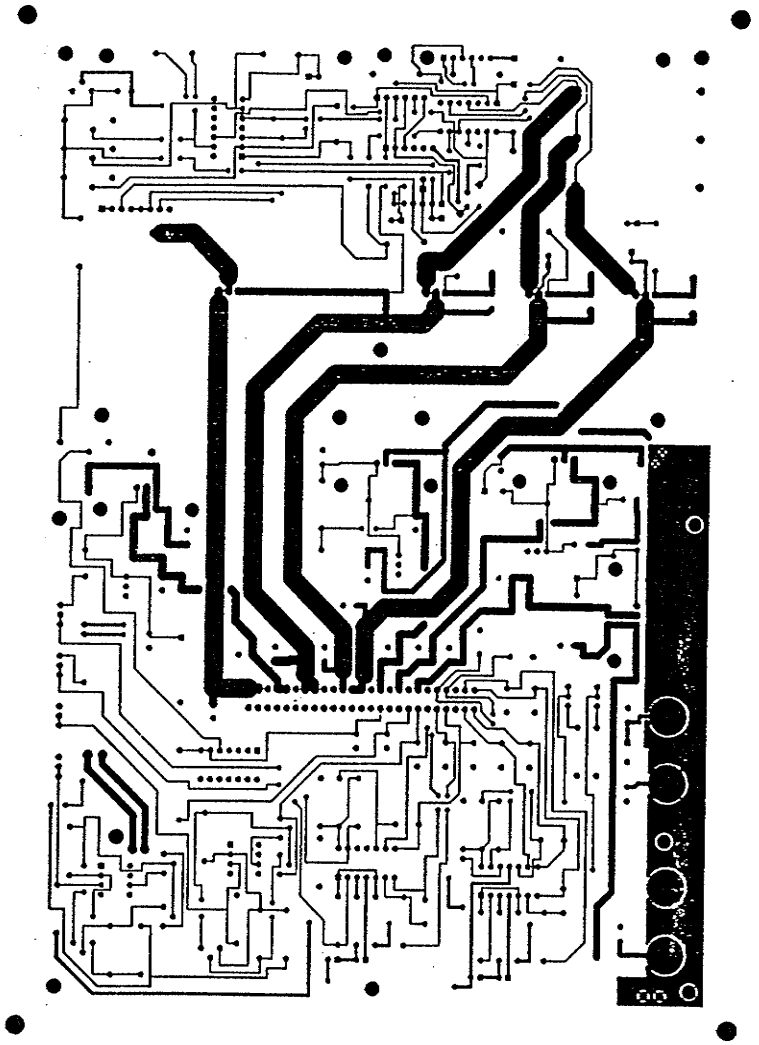

Figure A.7: Power Supply PCB artwork, layer 1 (2:1 scale).

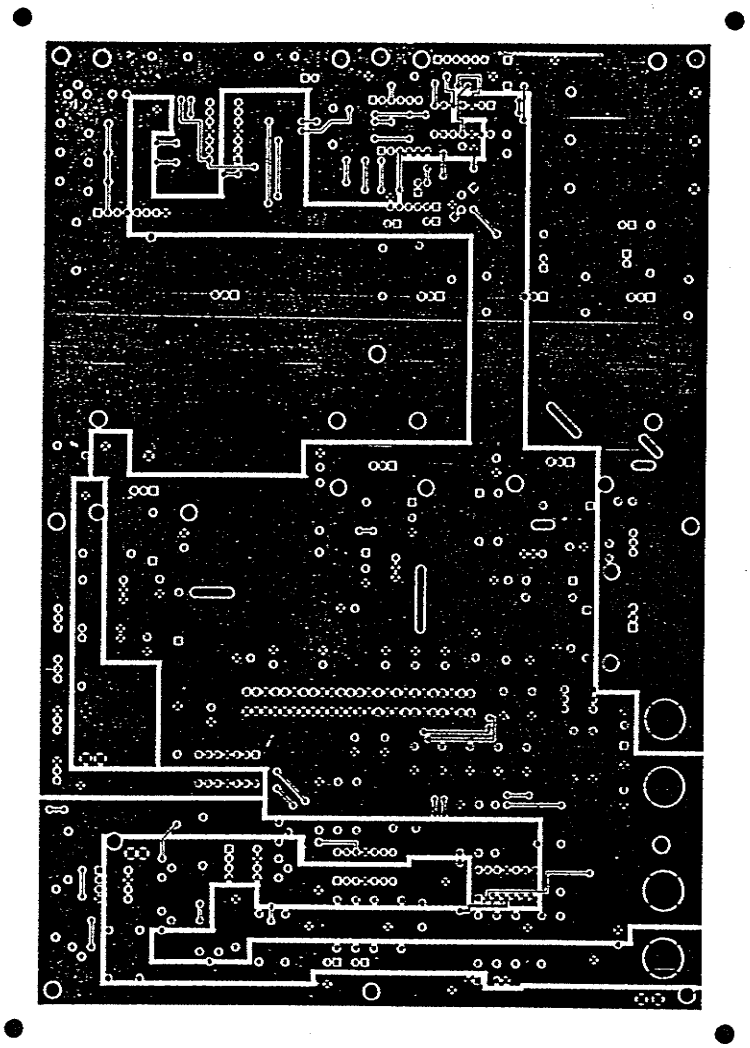

Figure A.8: Power Supply PCB artwork, layer 2 (2:1 scale).

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